Bonding constraints and defect formation at interfaces between crystalline silicon and advanced single layer and composite gate dielectrics

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An increasingly important issue in semiconductor device physics is understanding of how departures from ideal bonding at silicon–dielectric interfaces generate electrically active defects that limit performance and reliability. Building on previously established criteria for formation of low defect density glasses, constraint theory is extended to crystalline silicon–dielectric interfaces that go beyond $Si–SiO_2$ through development of a model that quantifies average bonding coordination at these interfaces. This extension is validated by application to interfaces between Si and stacked silicon oxide/nitride dielectrics demonstrating that as in bulk glasses and thin films, an average coordination, N_{av}, greater than three yields increasing defective interfaces. © *1999 American Institute of Physics.* [S0003-6951(99)00414-3]

As integrated circuits are aggressively scaled to increase device packing, channel lengths in field effect transistors (FETs) are projected to decrease to ~50 nm by 2012 with the oxide-equivalent thickness ($t_{ox\text{-}eq}$) for gate dielectrics decreasing proportionally to <1 nm. For $t_{ox\text{-}eq}<2.5$ nm direct tunneling in SiO_2 becomes important in off-state leakage. Since tunneling increases exponentially with decreasing oxide thickness, this necessitates introduction of alternative insulators such as Si_3N_4, and Ta_2O_5 with dielectric constants>SiO_2. These provide scaled-down values of $t_{ox\text{-}eq}$ required to maintain FET current drive, while reducing tunneling through increases in film thickness.

For oxides <2.5 nm, interfacial defects such as Si dangling bonds, can limit performance and reliability, making it important to establish relationships between interface bonding chemistry and defect properties. Experiments on stacked silicon oxide/nitride dielectrics prepared by remote plasma-enhanced chemical vapor deposition (RPECVD) have provided insights into these issues. RPECVD, followed by rapid thermal annealing (RTA) at 900 °C in a nonoxidizing ambient has yielded device-quality nitrides for *n*- and *p*-channel FETs with $t_{ox\text{-}eq}\sim 2$ nm.[1,2] Minimization of Si and N atom dangling bonds in annealed bulk RPECVD nitrides derives from low levels of bonded H, ~15 at. %.[3,4]

Figure 1 displays current–voltage ($I–V$) curves for *p*-channel FETs for different gate dielectrics with $t_{ox\text{-}eq}$ ~2 nm: (i) a 4 nm RPECVD nitride, (ii) a 0.5 nm plasma oxide with a 2.4 nm RPECVD nitride, and (iii) a 1.5 nm thermal oxide with a 1.0 nm RPECVD nitride. $I–V$ traces for (ii) and (iii) display excellent turn-on behavior and the same current drive, with differences in threshold voltage derived primarily from differences in substrate doping. In contrast, for the FET with the 4 nm nitride: (i) threshold voltage is shifted negative by >1 V, (ii) turn-on is soft, and (iii) channel drive current is reduced by a factor of ~50. Figure 2 displays capacitance–voltage ($C–V$) characteristics for *p*-type metal-oxide-semiconductor (PMOS) devices with $t_{ox\text{-}eq}\sim 4.3$ nm: one with a plasma oxide, and two with stacked dielectrics with RPECVD nitride interface layers of 0.4 and 0.8 nm, respectively. Shifts in threshold (and flat band) voltage relative to $Si–SiO_2$ indicate increased fixed charge for devices with nitride interfaces: $\Delta q_f = C_{ox}\Delta V_{th}$ (or ΔV_{fb}). Qualitatively similar results have been obtained for *n*-type metal-oxide-semiconductor (NMOS) devices with nitride layer interfaces.[4]

Three factors can play a role in promoting interfacial defects: (i) interfacial dipoles due to charge transfer between the Si substrate and gate dielectric,[5] (ii) molar volume differences between the Si substrate and gate dielectric, and (iii) over-constrained bonding due to large values of average coordination in the interfacial region.[6] Charge transfer is smaller at nitride interfaces so that interfacial dipoles cannot

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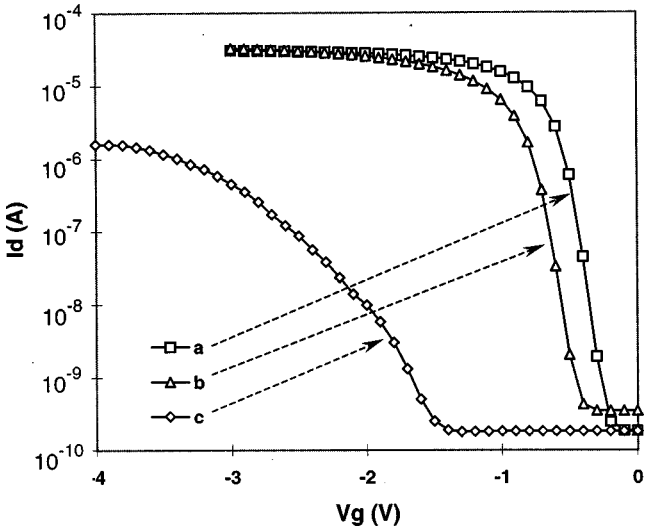

FIG. 1. Drive current-gate voltage ($I_d - V_g$) characteristics for PMOSFETs with $t_{ox\text{-}eq} \sim 2$ nm: (a) a 1.5 nm oxide separating a 1.0 nm nitride from the Si substrate, (b) a 0.6 nm oxide separating a 2.4 nm nitride from the Si substrate, and (c) a 4 nm nitride layer. The threshold voltage shift between (a) and (b) is due in part to substrate doping differences (0.16 V) and in part to positive charge at the oxide–nitride interface (0.04 eV).

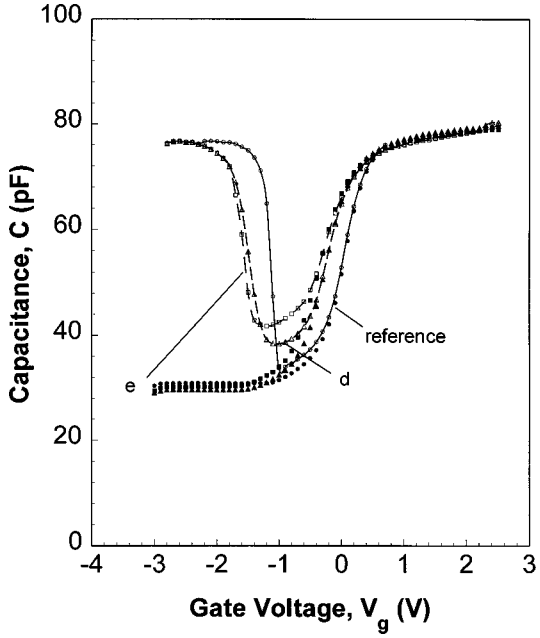

FIG. 2. $C-V$ characteristics demonstrate shift in flat band voltage due to positive charge, and increased separation between high frequency and quasistatic plots due to interface trapping accompanying direct deposition of thin nitride films onto Si. Each of these capacitors has $t_{ox\text{-}eq} \sim 4.3$ nm: (i) a reference oxide, and (ii) two stacked NO structures with the nitride layer in contact with the Si substrate. The nitride layer thickness is 0.4 nm for (d), and 0.8 nm for (e).

play the determinant role in increased defect densities.[5] Since the molar volume mismatch between Si_3N_4 and Si is reduced with respect to that of SiO_2 and Si, residual interface strain is smaller and cannot be the origin of higher defect concentrations at $Si-Si_3N_4$ interfaces. The remainder of this letter focuses on interfacial bonding constraints.

The abruptness of $Si-SiO_2$ interfaces suggests that the defect density of thermally grown oxides and optimally annealed deposited oxides is a characteristic function of their bonding chemistry and structure. Experience with good glass formers such as SiO_2 and As_2Se_3 has shown that as long as only single bonds are present charge transfer plays a minor part in determining structure. The major factor is the network stress which arises for a given space-filling bonding topology.

Constraint theory has provided a remarkably accurate description of network stress and its consequences.[6,7] The theory is based on the idea that all the bonding forces (stretching, bending, etc.) in the network can be arranged in a hierarchy from strong to weak. The constraining effects of these forces are a linear function of the average coordination number, N_{av}. If both bond-bending and stretching forces are present, the optimal average coordination number, N_{av}^*, which matches constraints to degrees of freedom is 2.4 as in $As_2S(Se)_3$, however, for SiO_2, $N_{av}^* = 2.67$ is optimal because bond-bending forces at O atoms are too weak to function as significant constraints at growth or annealing temperatures.[8] For over-constrained networks such as Si_3N_4 ($N_{av} = 3.43$), Si-atom stretching constraints are stronger than bending constraints, so that strain energy accumulates along the bending constraints. The average Si–N–Si bond angle θ_{ij} is distorted from the ideal local value θ_{ij}^* by an amount

$$\delta\theta \propto \delta N_{av}^* = N_{av} - N_{av}^*. \quad (1)$$

Since total strain energy is proportional to $(\delta\theta)^2$,[9] it is then anticipated that defect creation, e.g., dangling Si or N bonds, will be proportional to $\{N_{av} - N_{av}^*\}^2$. Experiments have shown that $N_{av} \sim 3$ represents a criterion between low defect density ($\sim 10^{16}\,cm^{-3}$), and increasingly defective materials.[10]

Extension of constraint theory to Si-dielectric interfaces considers three interfacial contributions to N_{av}: (i) the Si substrate represented by one-half a Si atom, (ii) an ultrathin oxide or nitride interfacial layer (0.3–0.6 nm), and (iii) the bulk dielectric by one-half a molecular layer. Table I includes calculations of N_{av} for representative Si-dielectric interfaces. When a demarcation level $N_{av} \sim 3$ is applied, these calculations are in excellent agreement with experiment (see Figs. 1 and 2). The model confirms that $Si-SiO_2$ interfaces are expected to display excellent interface properties ($N_{av} \sim 2.8$), whereas $Si-Si_3N_4$ interfaces are not ($N_{av} \sim 3.5$). Equally important, the calculations demonstrate that interposition of ultrathin SiO_2 layers between Si and Si_3N_4 results in values of $N_{av} \leqslant 3$, whereas interposition of ultra thin Si_3N_4 layers between Si and SiO_2 results in $N_{av} > 3$. Figure 3 is based on the data of Figs. 1 and 2, and demonstrates that defect scaling for bulk films, Eq. (1), also holds at interfaces.

Nitride layers have been produced by techniques other than RPECVD. For example, films have been prepared by jet vapor deposition (JVD) yielding excellent electrical results.[13] However, nitride films produced in this way can have oxygen concentrations as high as 15–18 at. %, and as such gate stacks incorporating these films are expected to have significant $Si-SiO_2$ bonding at the Si-dielectric interface. Without more detailed characterizations of interfacial oxide concentrations in the JVD films, it is not possible to make direct comparisons between the performance of these devices and the quantitative aspects of constraint theory.

The model has also been applied to interfaces between Si and (i) silicon oxynitride alloys and (ii) alternative high-K

TABLE I. Average bonding coordination at Si-dielectric interfaces.

Material system	Average coordination (N_{av})	Electrical quality
$Si-SiO_2$ (1.5 molecular layers)	2.8	excellent, thermal oxides
$Si-Si_3N_4$ (1.5 molecular layers)	3.5	very poor [Ref. 4]
$Si-\{SiO_2\}(t)-Si_3N_4$	$t=0.6$ nm: 3.0	very good [Fig. 1]
$t=$ oxide layer thickness	$t=1.5$ nm: 2.9	excellent [Fig. 1]
$Si-\{Si_3N_4\}(t)-SiO_2$	$t=0.4$ nm: 3.3[d]	poor [Fig. 2]
$t=$ oxide layer thickness	$t=0.8$ nm: 3.4	poor [Fig. 2]
$Si-N-SiO_2$ {1 monolayer (ML)}	2.8	excellent [Ref. 5]
$Si-(SiO_2)_{0.977}\{Si_3N_4\}_{0.023}$	2.3 at. % N: 2.8	excellent [Ref. 14]
$Si-(SiO_2)_{0.89}\{Si_3N_4\}_{0.11}$	11 at. % N: 3.0	poor [Ref. 14]
$Si-TiO_2\}$[a] (1.5 molecular layers)	4.0	unreported
$Si-Ta_2O_5\}$[b] (1.5 molecular layers)	3.5	unreported
$Si-Al_2O_3\}$[c] (1.5 molecular layers)	3.6	unreported

[a]Average coordination [Ti]=6, [O]=3.0 [rutile/anatase bonding].
[b]Average coordination: [Ta]=6, [O]=2.4 [Ref. 11].
[c]Average coordination: Al=[4.5], [O]=3.0 [3:1 ratio of tetrahedral to octahedral sites, see Ref. 12].
[d]Sample calculation of N_{av} for $Si-\{Si_3N_4\}(t)-SiO_2$: $t=0.4$. Substrate: 1/2 atomic layer: 0.5 atoms, 2 bonds. Interface layer: 1 molecular layer: 7 atoms (Si_3N_4), 24 bonds. Dielectric film: 1/2 molecular layer: 1.5 atoms (SiO_2), 4 bonds. 30 bonds/9 atoms$=N_{av}=3.3$ bonds/atom.

dielectrics. For oxynitride alloys, Vogel *et al.*,[14] reported only a small reduction in electron channel mobilities in an alloy with about 2.3% nitrogen corresponding to $N_{av}\sim 2.8$. While the criterion developed by the application of constraint theory predicts that the interfacial defect density should not become appreciable until the alloy concentration exceeds approximately 15–20 at. % *N*, interfacial defects in *n*-channel FETs degrade channel mobilities by more than a factor of two at a nitrogen concentration of only 11 at. % corresponding to $N_{av}\sim 3.0$. This demonstrates that factors other than interfacial bonding constraints can contribute in a significant way to the formation of interfacial defects. However, it is important to note that for the oxynitride alloys of Ref. 14, the experimentally determined defect levels are higher than what is predicted by the application of constraint theory, so that constraint theory may still provide a guideline for estimating the minimum defect densities. The model calculations for Ta_2O_5, TiO_2, and Al_2O_3 explain the necessity for ultrathin SiO_2 layers between the Si substrate and these high-*K* oxides. As such the model suggests important limitations for gate dielectric interfaces other than $Si-SiO_2$. Specifically: (i) Si_3N_4 cannot be directly substituted for SiO_2 at Si substrates; and (ii) substitution of more highly coordinated high-*K* dielectrics such as Ta_2O_5, etc., will generally require SiO_2, or monolayer nitrided SiO_2 interfaces, thus establishing a limitation on the extent to which $t_{ox\text{-}eq}$ can be reduced below 1 nm. Finally, the bonding constraint model should be taken as a guideline for anticipating differences in interface quality that arise solely from differences in average bonding coordination. As such it focuses on one important aspect of interfacial bonding and structure. It is anticipated that as for the oxynitride dielectrics of Ref. 12, additional aspects of interface bonding and structure will also generate significant concentrations of electrically active defects at other Si-dielectric interfaces.

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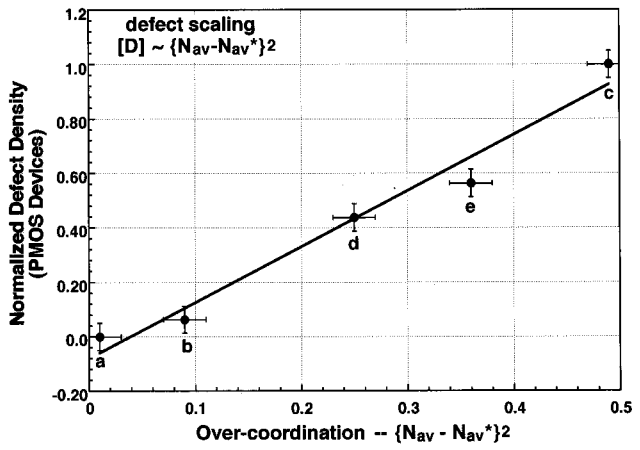

FIG. 3. Plot of normalized defect density as a function of $\{N_{av}-N^*_{av}\}^2$. Data points *a*, *b*, and *c* are from Fig. 1, and *d* and *e* from Fig. 2.

[1] C. G. Parker, G. Lucovsky, and J. R. Hauser, IEEE Electron Device Lett. **19**, 106 (1998).
[2] Y-D Wu and G. Lucovsky, IEEE Electron Device Lett. **19**, 357 (1998).
[3] Z. Lu, M. J. Williams, P. F. Santos-Filho, and G. Lucovsky, J. Vac. Sci. Technol. A **13**, 607 (1995).
[4] V. Misra, Z. Wang, H. Lazar, Y. Wu, H. Niimi, G. Lucovsky, J. J. Wortman, and J. R. Hauser (unpublished).
[5] G. Lucovsky and H. Z. Massoud, J. Vac. Sci. Technol. B **16**, 2191 (1998), and references therein.
[6] J. C. Phillips, J. Non-Cryst. Solids **34**, 153 (1979); **47**, 203 (1983).
[7] H. He and M. F. Thorpe, Phys. Rev. Lett. **54**, 2107 (1985).
[8] J. C. Phillips (unpublished).
[9] J. H. Van der Merwe, J. Appl. Phys. **34**, 123 (1963).
[10] G. Lucovsky and J. C. Phillips, J. Non-Cryst. Solids **227**, 1221 (1998).
[11] F. L. Galeener, W. Stutius, and G. T. McKinley, in *The Physics of MOS Insulators*, edited by G. Lucovsky, S. T. Pantelides, and F. L. Galeener (Pergamon, New York, 1980), p. 77.
[12] G. Lucovsky, A. Rozaj-Brvar, and R. F. Davis, in *The Structure of Non-Crystalline Materials 1982*, edited by P. H. Gaskell, J. M. Parker, and E. A. Davis (Taylor and Francis, London, 1983), p. 193.
[13] T. P. Ma, IEEE Trans. Electron Devices **45**, 680 (1998).
[14] E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, J. J. Wortman, J. R. Hauser, P. Morfouli, G. Ghibaudo, and T. Ouisse, IEEE Trans. Electron Devices **43**, 753 (1996).