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Surface passivation of *n*-GaN by nitrided-thin-Ga_2O_3/SiO_2 and Si_3N_4 films

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The electrical characteristics of *n*-GaN/nitrided-thin-Ga_2O_3/SiO_2 and *n*-GaN/Si_3N_4 metal-insulator-semiconductor (MIS) capacitors have been compared, and the work-function difference ϕ_{ms} and effective dielectric-fixed charge density $Q_{f,eff}$ have been determined. Oxide samples showed lower interface trap level density D_{it}, lower leakage current, and better reproducibility compared to the nitride samples. The superior properties of the oxide samples are partially attributed to the nitrided-thin-Ga_2O_3 layer (~0.6-nm-thick). ϕ_{ms} and $Q_{f,eff}$ were determined, respectively, as 0.13 V and $1.0\times10^{12}\,q\,cm^{-2}$ in oxide and 0.27 V and $-3.6\times10^{11}\,q\,cm^{-2}$ in nitride samples using flatband voltage versus dielectric thickness data. True dielectric-fixed charge density and location of the major amount of fixed charge are discussed based on $Q_{f,eff}$, D_{it}, and spontaneous polarization of *n*-GaN. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1772884]

I. INTRODUCTION

Gallium nitride/insulator interfaces have been investigated for application in GaN-based metal-insulator-semiconductor field effect transistors (MISFETs) and AlGaN/GaN high electron mobility transistors (HEMTs).[1–3] Many researchers have reported promising *n*-GaN/insulator interfaces showing a reduced interface trap level density D_{it} as compared to MIS structures on other compound semiconductors (Ref. 1 and references therein). Among the promising insulating materials on GaN—mainly formed by plasma-assisted amorphous film deposition, epitaxial film growth, and oxidation of the GaN surface—SiO_2 and Si_3N_4 are potentially the most valuable as they have supported the Si-based MIS device industry.

The electrical properties reported for *n*-GaN/SiO_2 and *n*-GaN/Si_3N_4 structures depend on GaN surface preparation and insulating film deposition method and gave rise to controversy concerning Fermi level pinning at the *n*-GaN/SiO_2 interface (Ref. 1 and references therein). When the oxide layer is formed by deposition rather than oxidation of the substrate, the cleaning method of the GaN surface is crucial for a reproducible interface featuring low D_{it}, because that very surface, buried under the deposited layer, becomes the GaN/dielectric interface. While the investigated and established *in situ* cleaning methods of the GaN surface have been successfully applied for surface studies of GaN and metal contacts in ultrahigh vacuum (UHV), most dielectrics in GaN-based MIS structures have been deposited after *ex situ* wet chemical treatment.

Ex situ or *in situ* removal of the air-grown native oxide on GaN does not guarantee the absence of an interfacial oxide in the *n*-GaN/SiO_2 structure because the presence of oxidant and excitation during processing very often leads to parasitic oxide growth on the substrate surface. During plasma-assisted SiO_2 deposition, a N_2-plasma-treated, nearly oxygen-free (oxygen coverage below 0.1 monolayer) *n*-GaN substrate was slightly consumed by plasma-activated oxygen species that diffused through the thickening SiO_2 layer and oxidized the underlying substrate; online Auger-electron spectroscopy (AES) indicated a ~0.7-nm-thick subcutaneous oxide.[4] Hashizume *et al.*[3] ascribed poor capacitance-voltage (C-V) characteristics of GaN/SiO_2 structures to unexpected and uncontrollable oxidation of the GaN surface during plasma-assisted SiO_2 deposition. Interface defects in GaN/SiO_2 MIS structures thus depend (among other factors) on the uncontrolled formation of interfacial gallium oxide during SiO_2 deposition and postdeposition annealing steps.

The GaN/Si_3N_4 structure has been the first choice when substrate oxidation is to be completely avoided. In GaN/Si_3N_4 MIS capacitors (MIS-Cs), reduced D_{it} was obtained by a NH_4OH cleaning followed by electron cyclotron resonance (ECR) N_2-plasma treatment.[3] However, Si_3N_4 appears to be a worse candidate than SiO_2 to gate dielectric due to trap levels in the lower half of the band gap as well as a small band offset with respect to GaN. Moreover, the *n*-GaN/Si_3N_4 interface does show a small amount of residual gallium oxide (oxygen coverage below 0.5 monolayer) after a conventional wet cleaning followed by nitride deposition.[5]

Parasitic oxidation of GaN during plasma-assisted SiO_2 deposition has been prevented by intentional plasma-assisted oxidation of the substrate prior to dielectric deposition.[4] Such two-step process at 300 °C—(i) remote-plasma-assisted oxidation (RPAO) to form an interfacial oxide (~0.6 nm thick) and (ii) remote-plasma-enhanced chemical-vapor deposition (RPECVD) to deposit SiO_2—significantly reduced interfacial trapping as compared to single-step SiO_2 deposition.[4] The RPAO process at low temperature also provides *in situ* surface cleaning, e.g., reducing the level of residual carbon.

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Of relevance to the electrical characterization of Al-gated MIS structures on *n*-GaN, the metal-semiconductor work-function difference ϕ_{ms} has been chosen as 0 V by assuming[6] that the work function of Al and *n*-GaN are both 4.1 eV. Theoretical C-V curves for Al-gated *n*-GaN MIS-Cs have been drawn under that assumption. Although an accurate value of ϕ_{ms} must be known to determine the dielectric-fixed charge density Q_f and little is known about the work function of GaN, there has been no effort to measure ϕ_{ms} for Al-gated MIS structures on *n*-GaN.

Assuming negligible dielectric-trapped charge density Q_{ot} and mobile dielectric charge density Q_m in a MIS structure, the flatband voltage V_{FB} is given by[7,8]

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_{it}(\psi_s) + Q_{pol}}{C_{ox}} = \phi_{ms} - \frac{Q_{f,eff}}{\varepsilon_{ox}} t_{ox}, \qquad (1)$$

where Q_f is the dielectric-fixed charge density, Q_{it} is the interface-trapped charge density, ψ_s is the semiconductor band bending, Q_{pol} is the polarization charge density, C_{ox} is the accumulation capacitance per unit area ($C_{ox}=\varepsilon_{ox}/t_{ox}$, where ε_{ox} is the permittivity of SiO_2 and t_{ox} the equivalent SiO_2 thickness of the dielectric), and $Q_{f,eff}$ is the effective dielectric-fixed charge density. After measurement of V_{FB} as a function of t_{ox}, ϕ_{ms}, and $Q_{f,eff}$ can be obtained from a linear fit to the experimental data; the intercept at the V_{FB} axis is ϕ_{ms}, and the slope is $-Q_{f,eff}/\varepsilon_{ox}$. If $Q_{f,eff}$ results from different types of charging, possible compensation effects must be considered to extract Q_f. In particular, Q_{pol} has been ignored in the analysis of MIS-Cs on GaN.

In their wurtzite structure, group III nitrides show spontaneous polarization along the [0001] direction, which induces bound surface/interface charges and gives rise to a strong internal electric field. The spontaneous polarization in GaN leads to a negative-bound charge at the Ga face and a positive-bound charge at the N face. Epitaxial GaN layers grown by metal organic chemical-vapor deposition (MOCVD), as in this work, are typically Ga face. The theoretical value[9] for the spontaneous polarization P_{sp} of GaN is -0.029 C m^{-2}, corresponding to a bound charge density of -1.73×10^{13} q cm^{-2} (where q is the elementary charge, 1.6022×10^{-19} C) at the Ga face. Piezoelectric polarization, which occurs in group III nitrides in addition to the spontaneous polarization, can be neglected if the GaN layer is above a critical thickness. In most previous reports on Al-gated *n*-GaN/SiO_2 MIS structures, the measured V_{FB} is close to 0 V, and the reported Q_f is on the order of 10^{11} q cm^{-2}. This indicates that Q_{pol} has been ignored despite its recognized and key effect in GaN/AlGaN heterostructures, because neutralization of the theoretical negative-bound charge requires ~100 times higher positive-charge density. Matocha *et al.*[8] reported on Q_{pol} in *n*-GaN-based MIS structures. An observed positive shift of V_{FB} with increasing temperature was attributed to changes in Q_{pol}; however, there was no consideration of Q_{pol} itself. In the Al/SiO_2/GaN/$Al_{0.4}Ga_{0.6}N$/GaN heterojunction MIS structure studied by Chen *et al.*,[10] a wide C-V hysteresis window and a positive V_{FB} shift corresponding to a charge density of -2.9×10^{12} q cm^{-2} were attributed to Q_{pol}.

The surface passivation of AlGaN is emerging as an important issue in AlGaN/GaN (HEMT) applications. Frequency-dependent current degradation attributed to trap levels between gate and drain was almost eliminated in devices incorporating Si_3N_4 or SiO_2.[2,11] Also, increased charge density in two-dimensional electron gases (2DEGs) was obtained by surface passivation of AlGaN using Si_3N_4 and SiO_2 layers.[12,13] Although the analysis of AlGaN-based MIS structures can be expected to be more complex than that of their GaN counterparts, it seems to be clear that the latter constitutes the basic research tool to understand the former.

We report the electrical characteristics of Al-gated *n*-GaN/nitrided-thin Ga_2O_3/SiO_2 and *n*-GaN/Si_3N_4 MIS-Cs as determined by C-V, ac conductance, and current-voltage (I-V) measurements. For conciseness, we refer to these structures as "SiO_2" and "Si_3N_4" samples. SiO_2 samples feature a three-step process designed for optimal interface formation—RPAO followed by remote-plasma-assisted nitridation (RPAN) and SiO_2 deposition—whereas Si_3N_4 samples feature the conventional single-step dielectric deposition on wet-etched substrate. We determine D_{it}, ϕ_{ms}, and $Q_{f,eff}$, for both sets of samples, discuss the results based on interface structure, and consider the effect of Q_{pol} on our findings.

II. EXPERIMENTAL PROCEDURE

A homoepitaxial Fe-doped insulating GaN/unintentionally doped GaN/Si-doped GaN structure was grown on sapphire by MOCVD. The thickness of the Si-doped GaN epilayer was ~1 μm, and its bulk carrier density was 3.3×10^{17} cm^{-3}. The *n*-GaN substrates were etched in NH_4OH/H_2O 1:5 solution at 80 °C for 15 min prior to introduction in the processing tool.

For the SiO_2 samples, the as-loaded *n*-GaN substrate was oxidized by remote O_2/He plasma at 0.3 Torr for 30 s to form a thin superficial Ga_2O_3 layer, which was then nitrided by remote N_2/He plasma at 0.3 Torr for 90 s. SiO_2 films were deposited by RPECVD using SiH_4 (2% in He) and an O_2/He gas mixture at 0.3 Torr.[4,5,14,15] For the Si_3N_4 samples, the dielectric was directly deposited on wet-etched GaN by RPECVD using SiH_4 (2% in He) and an N_2/He gas mixture at 0.2 Torr.[14] In all remote plasma processing, the substrate temperature was 300 °C and radio frequency (rf) power was 30 W at 13.56 MHz.

After SiO_2 or Si_3N_4 deposition, the samples were rapid-thermal annealed at 900 °C for 30 s in Ar atmosphere. A 300-nm-thick Al layer was evaporated onto the samples and defined by a conventional lithographic process. Postmetallization annealing (PMA) was performed at 400 °C for 30 min in forming gas (N_2/H_2). The electrical properties of MIS-Cs on *n*-GaN were investigated using HP 4284A and 4140B meters. The area of the devices under test was $(1-4)\times10^{-4}$ cm^2.

III. RESULTS AND DISCUSSION

A. Interface trap level density

Figure 1 displays measured and simulated C-V characteristics of (i) a SiO_2 and (ii) a Si_3N_4 sample. Contrary to their SiO_2 counterparts, Si_3N_4 samples showed a large run-

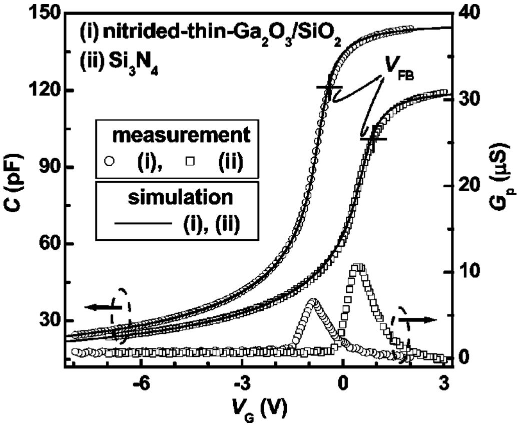

FIG. 1. Measured and simulated C-V curves for Al-gated (i) n-GaN/nitrided-thin-Ga_2O_3/SiO_2 and (ii) n-GaN/Si_3N_4 MIS-Cs at 25 °C and 1 MHz; t_{ox} and V_{FB} are (i) 9.4 nm and −0.4 V and (ii) 11.4 nm and 0.9 V, respectively. Also shown is parallel conductance.

to-run variation. Optimal Si_3N_4 samples were chosen for comparison with SiO_2 in this article. The equivalent SiO_2 thicknesses t_{ox} are (i) 9.4 and (ii) 11.4 nm. C-V curves were acquired at 1 MHz, at room temperature, in the dark, and with the gate voltage V_G being swept from positive to negative. In the evaluation of expressions for the theoretical C-V curves,[7,16] the same fundamental constants as in a previous report[6] were used. Because MIS-Cs on the wide-bandgap n-GaN showed deep depletion instead of inversion, the net donor concentration N_D in the semiconductor substrate was obtained as 4.2×10^{17} cm^{-3} for both samples from data fitting to the partial range of the C-V characteristics in which $1/C^2$-V is linear, as shown in Fig. 2. Simulated ideal (i.e., without considering oxide or interface defects) C-V curves were shifted along the voltage axis until they showed good agreement with the measured data.

The C-V data obtained from the Si_3N_4 sample shows larger deviation from the simulated curve. Discrepancies are attributed to stretch-out of the experimental data along the V_G axis due to changes in the occupancy of interface states. In the negative V_G direction starting at a point below V_{FB}, the measured C-V data are intrinsically well described by the simulated curves because interface states cannot follow changes in V_G quasi-statically.[17] The measured V_{FB} is (i) −0.4 V for the SiO_2 and (ii) 0.9 V for the Si_3N_4 sample. Such V_{FB} data is used in the next section to determine ϕ_{ms} and $Q_{f,eff}$.

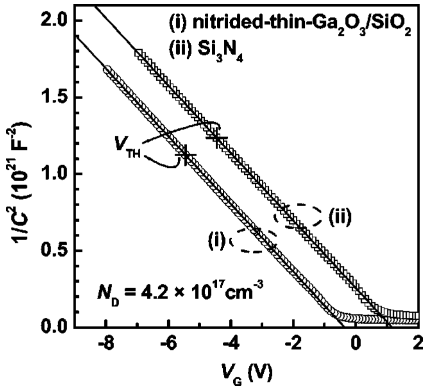

FIG. 2. Plot of $1/C^2$ versus V_G data for Al-gated (i) n-GaN/nitrided-thin-Ga_2O_3/SiO_2 and (ii) n-GaN/Si_3N_4 MIS-Cs. Net doping concentration N_D obtained from the slopes is 4.2×10^{17} cm^{-3} for both samples. Threshold voltages V_{TH} are (i) −5.3 V and (ii) −4.4 V. Both samples clearly show deep depletion below V_{TH}. Symbols are experimental data, lines are fit to the data.

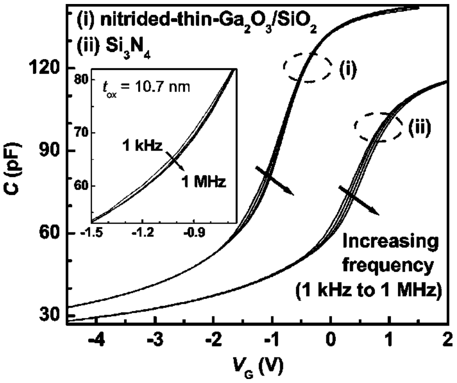

FIG. 3. Frequency dependence of the C-V characteristics of the MIS-Cs that originated Fig. 1. The inset displays data from the n-GaN/nitrided-thin-Ga_2O_3/SiO_2 MIS-C showing the lowest D_{it} among the samples fabricated.

Figure 1 also shows the measured parallel conductance G_p for both SiO_2 and Si_3N_4 samples, evidencing clear peaks of interface trap loss and negligible dielectric loss. The conductance peak of the Si_3N_4 sample is about 1.5 times higher than that of the SiO_2 sample. Because these samples showed similar values of series resistance (~200 Ω) and C_{ox}, D_{it} is nearly proportional to the measured conductance peak height.

We refrain from estimating D_{it} using the Terman method. The N_D for n-GaN in MIS-Cs was obtained by fitting the measured C-V data. In this case, stretch-out due to changes in the occupancy of interface traps can be misinterpreted as increased doping concentration, also leading to the underestimation of D_{it} as determined by the Terman method. The high-low frequency C-V and ac conductance methods[16] were used to extract a more reliable D_{it}, within their limitations when applied to n-GaN MIS devices.[18,19]

Figure 3 shows the frequency dependence (1, 10, 100 kHz and 1 MHz) of the C-V characteristics of the (i) SiO_2 and (ii) Si_3N_4 samples that originated Fig. 1. The inset displays C-V characteristics of the sample showing the lowest interface trap level density among the SiO_2 samples fabricated. In the high-low frequency C-V method, D_{it} as a function of gate voltage is calculated from[16]

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right), \qquad (2)$$

where C_{lf} is the capacitance measured at low frequency ($f = 1$ kHz) and C_{hf} is the capacitance measured at high frequency ($f = 1$ MHz). In our samples, the actual D_{it} is higher than estimated using this method because 1 kHz is not sufficiently low to allow the response of slow interface traps. The V_G at which high- and low-frequency C-V curves show the maximum capacitance difference ΔC_{max} corresponds to an energy level at which D_{it} can be extracted without severe underestimation.[4] The extracted D_{it} rapidly decreases below $V_G(\Delta C_{max})$ because, as noted earlier,

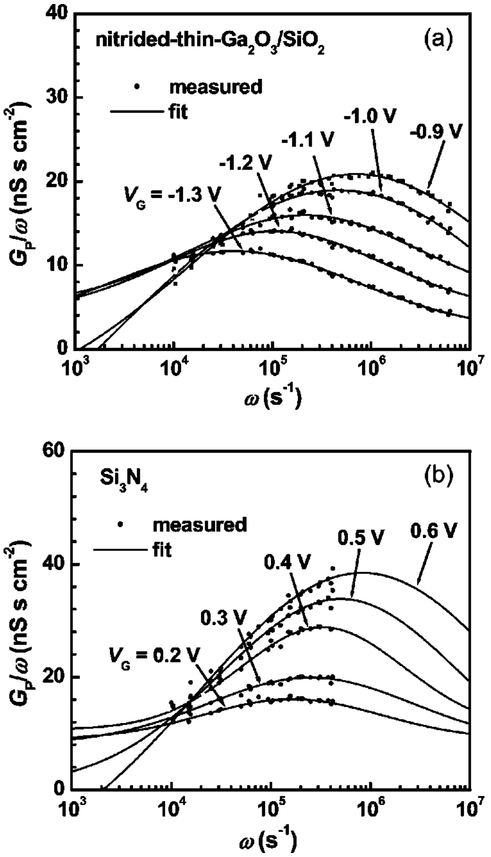

FIG. 4. Parallel conductance G_p/ω versus angular frequency ω from (a) n-GaN/nitrided-thin-Ga$_2$O$_3$/SiO$_2$ and (b) n-GaN/Si$_3$N$_4$ MIS-Cs. Points are experimental data; lines are Gaussian fit to the data.

interface states cannot follow changes in V_G quasi-statically and thus become undetected. The D_{it} from ΔC_{max} is 4×10^{11} cm^{-2} eV^{-1} at $V_G=-1.1$ V for the SiO$_2$ sample and 9×10^{11} cm^{-2} eV^{-1} at $V_G=0.4$ eV for the Si$_3$N$_4$ sample. We present the energy distribution of D_{it} according to the high-low frequency method after considering ac conductance measurements.

Figure 4 displays parallel conductance G_p/ω *versus* angular frequency $\omega=2\pi f$ curves at selected gate voltages. From the graphically determined standard deviation of band bending σ_s and universal function f_D as a function of σ_s, the D_{it} of each sample was extracted using[16]

$$D_{it}=\left(\frac{G_p}{\omega}\right)_{f_p}[qf_D(\sigma_S)]^{-1}, \tag{3}$$

where f_p is the frequency corresponding to the peak value of G_p/ω. The determined values of f_D were 0.18–0.20 for the SiO$_2$ and 0.19–0.24 for the Si$_3$N$_4$ sample. The D_{it} from the ac conductance and high-low frequency C-V methods is shown in Fig. 5 as a function of energy relative to the GaN conduction band edge E_C. The SiO$_2$ sample shows lower D_{it} according to both methods in the whole energy interval under consideration. As noted earlier, Si$_3$N$_4$ samples presented poor reproducibility; the result shown is from an optimal sample. For the SiO$_2$ sample that originated the inset in Fig. 3, D_{it} from the high-low frequency C-V method at $E_C-E\approx0.3$ eV is 1×10^{11} cm^{-2} eV^{-1}; the ac conductance method could not be used for this sample due to a small signal-to-noise ratio, as observed for an optimized SiO$_2$/Si$_3$N$_4$/SiO$_2$ (ONO) structure on n-GaN.[18] The rapidly decreasing D_{it} for both SiO$_2$ and Si$_3$N$_4$ samples at $E_C-E>0.3$ eV $\approx qV_G(\Delta C_{max})$ is not realistic, as discussed earlier.

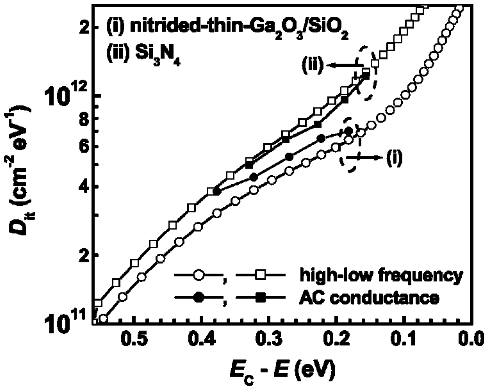

FIG. 5. Interface trap level density D_{it} for (i) n-GaN/nitrided-thin Ga$_2$O$_3$/SiO$_2$ and (ii) n-GaN/Si$_3$N$_4$ MIS-Cs as determined using the ac conductance and high-low frequency C-V methods.

Table I summarizes the parameters extracted from the electrical characterization of SiO$_2$ samples featuring various t_{ox}. All MIS-Cs were fabricated under the same conditions, but the sample featuring $t_{ox}=20.3$ nm showed higher D_{it} and a significantly wider, positive hysteresis window as compared to the others. Implications will be noted in the following section.

B. Dielectric-fixed charge density and metal-semiconductor work-function difference

Figure 6 shows V_{FB} versus t_{ox} data for Al-gated [(i) and (ii)] SiO$_2$ and (iii) Si$_3$N$_4$ samples. For the SiO$_2$ samples, linear fitting was performed (i) excluding and (ii) including the sample with $t_{ox}=20.3$ nm; ϕ_{ms} and $Q_{f,eff}$ were thus determined as (i) 0.13 ± 0.09 V and $(1.0\pm0.1)\times10^{12}$ q cm^{-2} and

TABLE I. Summary of parameters extracted from n-GaN/nitrided-thin-Ga$_2$O$_3$/SiO$_2$ MIS-Cs featuring various t_{ox}. The hysteresis window is reported at flatband capacitance, and minimum D_{it} was obtained at $E_C-E\approx0.3$ eV using the high-low frequency C-V and the ac conductance (data in parentheses) methods.

t_{ox} (nm)	N_D (10^{17} cm^{-3})	V_{FB} (V)	V_{TH} (V)	Hysteresis window (V)	D_{it} (10^{11} cm^{-2} eV^{-1})
5.8	4.0	−0.02	−4.34	−0.03	3.3
9.4	4.2	−0.46	−5.43	−0.02	4.3 (5.4)
10.5	4.0	−0.39	−5.36	−0.03	2.0
20.3	3.9	−0.43	−7.17	0.50	8.5
35.2	4.1	−1.50	−10.72	−0.02	6.3 (6.8)

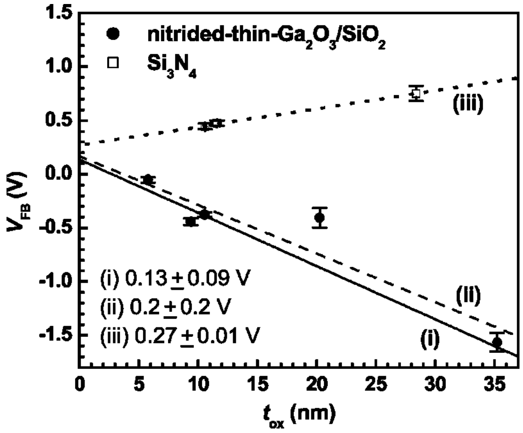

FIG. 6. Linear fits to flat band voltage V_{FB} versus equivalent oxide thickness t_{ox} data from n-GaN/nitrided-thin-Ga_2O_3/SiO_2 MIS-Cs [(i) excluding and (ii) including the point at 20.3 nm] and from (iii) n-GaN/Si_3N_4 MIS-Cs. The displayed error bars are standard deviations of V_{FB} measured for different capacitors on each sample. Standard deviations of t_{ox} are below ±1% of t_{ox}.

(ii) 0.2 ± 0.2 V and $(1.0 \pm 0.2) \times 10^{12}\ q\ \mathrm{cm}^{-2}$, respectively. We note that for the proper extraction of ϕ_{ms}, it is an essential requirement that all samples considered present the same amount of charge at the semiconductor-oxide interface. The sequential etching of SiO_2 can be seen as an alternative method to produce samples with different t_{ox} satisfying the requirement of a constant amount of charge at the semiconductor-oxide interface.

To evaluate Al/n-GaN/Si_3N_4 structures, samples with relatively low D_{it} were chosen. Si_3N_4 samples with high D_{it} (mid-$10^{12}\ \mathrm{cm}^{-2}\ \mathrm{eV}^{-1}$) showed more positive V_{FB}, whose proper extraction was made difficult by significant electron trapping. Large positive V_{FB} was also reported on nonoptimized n-GaN MIS structures with high D_{it} using SiO_2 and ONO dielectrics.[4,18] For the selected Si_3N_4 samples with relatively low D_{it}, ϕ_{ms} and $Q_{f,eff}$ extracted from our data are 0.27 ± 0.01 V and $(-3.6 \pm 0.2) \times 10^{11}\ q\ \mathrm{cm}^{-2}$, respectively.

Focusing on $Q_{f,eff}$ results, Fig. 7 illustrates that in the case of a MIS-C on n-type substrate at V_{FB}, most of the interface trap levels are occupied. We assume that interface traps at the upper (lower) half of the band gap are acceptor-(donor-) type. Acceptor-type (neutral when empty) interface traps below the Fermi energy E_F appear as negative Q_{it}, whereas acceptor-type interface traps above E_F and donor-type (positive when empty) interface traps do not contribute to Q_{it} because they are both neutral. Furthermore, we momentarily neglect Q_{pol} in Eq. (1). Then

$$Q_f = Q_{f,eff} - Q_{it,e} \approx Q_{f,eff} + qD_{it}\left[\frac{E_g}{2} - (E_C - E_F)\right], \tag{4}$$

where $Q_{it,e}$ is the interface-trapped charge density ($Q_{it,e} < 0$) and E_g is the band gap energy of GaN, $E_C - E_V$. Using $Q_{f,eff}$ reported earlier, taking D_{it} from ac conductance results in Fig. 5 at $E_C - E = 0.3$ eV and using $E_C - E_F = 0.1$ eV, Q_f becomes $\sim 1.7 \times 10^{12}\ q\ \mathrm{cm}^{-2}$ in SiO_2 samples and $\sim 5.5 \times 10^{11}\ q\ \mathrm{cm}^{-2}$ in Si_3N_4 samples. Therefore, although SiO_2 samples present lower D_{it} and better reproducibility than Si_3N_4 samples, they apparently present higher dielectric fixed charge density. We recall that all calculations shown earlier assume this fixed charge to be at the semiconductor/dielectric interface (as verified for the Si/SiO_2 system). If such charge density is distributed over the dielectric film thickness, the figures just presented for $Q_{f,eff}$ and Q_f are overestimated. That could be the case for the Si_3N_4 samples (even though they have not been subjected to electrical stress before measurements). In the case of SiO_2 samples, we speculate that the major amount of fixed dielectric charge is located at the nitrided-thin-Ga_2O_3/SiO_2 interface.

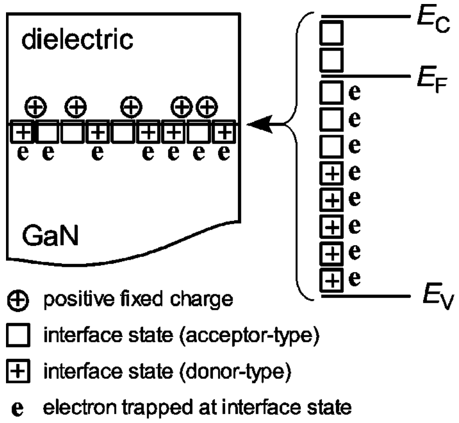
dielectric
GaN
E_C
E_F
E_V
e
⊕ positive fixed charge
□ interface state (acceptor-type)
⊞ interface state (donor-type)
e electron trapped at interface state

FIG. 7. Interface trap level configuration in an MIS structure on n-type substrate at V_{FB}.

We now consider the possible effect of Q_{pol} on Q_f. The theoretical value of upward surface band bending at the Ga-face of GaN is 3.4 V.[20] The experimentally obtained upward band bending is lower and dependent on the cleaning method of GaN via structural defects, surface states, and contamination causing Fermi level pinning or additional charge screening.[20] For example, Bermudez[21] found that practical n-GaN surfaces prepared by cleaning in aqueous NH_4OH show an upward band bending of 0.4 ± 0.2 V, less than the value of 0.9 V obtained after cleaning in UHV. Tracy *et al.*,[22] who performed *in situ* chemical vapor cleaning (CVC), reported an upward band bending of ~ 0.3 V. Consider n-GaN-based MIS structures showing a low density of donor-like surface states and negligible upward band bending, i.e., D_{it} on the order of $10^{11}\ \mathrm{cm}^{-2}\ \mathrm{eV}^{-1}$ and V_{FB} close to 0 V, as in the present work. One possible screening mechanism of Q_{pol} is positive Q_f. Including Q_{pol} corresponding to the theoretical P_{sp} in (4) as per (1), Q_f in our MIS structures could be as high as $\sim 2 \times 10^{13}\ q\ \mathrm{cm}^{-2}$. In SiO_2 samples, we suggest the Ga_2O_3/SiO_2 interface as the location of the major amount of positive Q_f. The preparation of n-GaN/nitrided-thin-Ga_2O_3/Al_2O_3 samples is underway. Lower Q_f at the Ga_2O_3/Al_2O_3 interface as compared to Ga_2O_3/SiO_2 could lead to incomplete neutralization of Q_{pol} and appear as a significant positive shift of V_{FB}.

We finally examine the possibility of Q_{pol} screening due to the presence of hydrogen, a ubiquitous impurity. First-principles calculations indicate that the H^- configuration is favored over H^+ and H^0 for hydrogen in GaN with E_F close to E_C, as in our substrate.[23] Therefore, H in n-GaN is not expected to screen Q_{pol}. It has been established that interstitial atomic H is amphoteric at the Si/SiO_2 interface, inducing a characteristic D_{it} peak 0.2 eV above the Si midgap level.[24] First-principles calculations indicate the H^+ configuration to be favored in SiO_2 for $E_F - E_V < 3.5$ eV.[25] Given the available information on band alignment at the SiO_2/GaN interface[26] and E_F in our substrate, it is unlikely that hydrogen in SiO_2 contributes to Q_{pol} screening. We have no account of H-charge state behavior in nitrided-thin-Ga_2O_3 or Si_3N_4. Charge configuration changes, as long as occurring for E_F within the semiconductor band gap, should appear as D_{it}. Such interface states, however, could be out of the energy range probed by standard measurement techniques.

Regarding ϕ_{ms}, we obtain 0.13 V from the SiO_2 samples, which is close to the 0 V assumed in most previous reports on n-GaN/SiO_2 MIS-Cs. An n-GaN/SiO_2 interface without detectable Ga_2O_3 was prepared by annealing GaN at 860 °C for 15 min in 1.0×10^{-4} Torr of NH_3 (CVC process), depositing an ultrathin Si sacrificial layer, and oxidizing it.[27] There is no report on metal-oxide-semiconductor (MOS) capacitors featuring such an n-GaN/SiO_2 interface without interfacial Ga_2O_3. Using ultraviolet photoelectron spectroscopy (UPS) and x-ray photoelectron spectroscopy (XPS), the conduction band offset ΔE_C was deduced as 3.6 eV. If the work function of Al ϕ_m and the electron affinity of SiO_2 χ are taken as 4.1 and 1.1 eV, respectively, ϕ_{ms} for the direct n-GaN/SiO_2 MOS structure with Al gate should be close to −0.7 V, according to[7]

$$q\phi_{\text{ms}} = \phi_m - [\chi + \Delta E_C + (E_C - E_F)], \tag{5}$$

where $E_C - E_F$ is again taken as ~ 0.1 eV. Note that to keep up with common practice, we report ϕ_{ms} in electric potential and the quantities in the right-hand side of Eq. (5) in energy units.

In metallurgical junctions, partial charge transfer between interface states of the two materials results in interface dipoles. Our methodology to determine ϕ_{ms} yields an effective value that incorporates any interface-dipole effects.[28] At n-GaN/dielectric interfaces, the interface dipole ranged from 1.3 to 2.0 V when SiO_2, Si_3N_4, or HfO_2 was used as a dielectric.[26,27,29] Although that is included (through ΔE_C) in the estimation above, the interface dipole between the Al gate and SiO_2 should make the effective ϕ_{ms} higher (i.e., less negative or more positive) than −0.7 V. We therefore ascribe the difference between −0.7 V and our result of 0.13 V to the combined effect of interface dipoles (i) between Al and SiO_2 and (ii) involving the interfacial nitrided-thin Ga_2O_3 in our samples. A more conclusive discussion will be possible after we determine (i) ϕ_{ms} using Al-gated MIS-Cs featuring the direct n-GaN/SiO_2 interface and/or (ii) ΔE_C between n-GaN and nitrided-thin Ga_2O_3/SiO_2 using UPS and XPS.

Using n-GaN/Si_3N_4 structures, ΔE_C for the direct interface has been determined[27] as 2.5 eV. Taking $\chi = 1.8$ V in (6) to account for the electron affinity of Si_3N_4 leads to $\phi_{\text{ms}} \approx -0.3$ V for Al-gated samples. Again, the difference between −0.3 V and our result of 0.27 V should be due to the combined effect of interface dipoles (i) between Al and Si_3N_4 and (ii) involving parasitic interfacial gallium oxide in our Si_3N_4 samples. Such interface dipoles must also account for the difference in ϕ_{ms} as obtained from SiO_2 and Si_3N_4 samples (0.13 and 0.27 V, respectively). With interface dipoles properly taken into account, ϕ_{ms} should be independent of dielectric as its textbook definition requires.

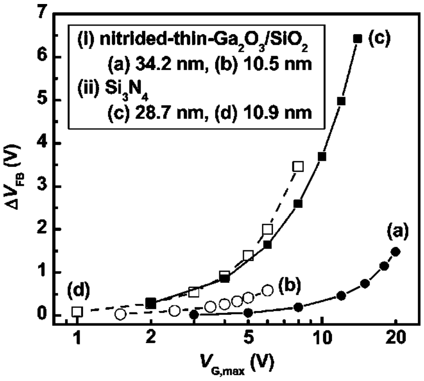

FIG. 8. Flatband voltage shift ΔV_{FB} as a function of maximum gate bias $V_{G,\text{max}}$ as determined for (i) n-GaN/nitrided-thin-Ga_2O_3/SiO_2 and (ii) n-GaN/Si_3N_4 MIS-Cs.

C. Electron trapping and electrical conduction

C-V characteristics of n-GaN MIS structures have been measured (before and in this study) by sweeping V_G from positive to negative. Substrate electron injection into dielectric traps due to the starting positive bias would cause positive ΔV_{FB}. As shown in Fig. 8, that is indeed observed, with Si_3N_4 samples showing several times larger ΔV_{FB} than SiO_2 samples under comparable maximum (starting) positive bias $V_{G,\text{max}}$. For an Si_3N_4 sample showing $t_{\text{ox}} \approx 11$ nm, N_D obtained from $1/C^2$-V data increased from 4.2 to 4.4×10^{17} cm^{-3} for $V_{G,\text{max}} = 0$ to 6 V due to the emission of trapped electrons. When $V_{G,\text{max}}$ was reduced from 3 to 0 V, V_{FB} and hysteresis window were reduced from 0.9 to 0.5 V and from 0.1 to 0.02 V, respectively. Significant electron trapping in our Si_3N_4 samples is ascribed to an elevated density of traps in the bulk Si_3N_4 film and a small conduction band offset between Si_3N_4 and GaN. As for SiO_2 samples, electron trapping should take place mostly at or near the interface with GaN, in trap levels out of our detection range. The absence of bulk electron traps in plasma-enhanced chemical vapor deposition (PECVD) SiO_2 can be inferred from its demonstrated performance on Si substrates.

Figure 9 displays gate current density J versus effective oxide field E_{ox} for (i) SiO_2 ($t_{\text{ox}} = 10.7$ nm) and (ii) Si_3N_4 ($t_{\text{ox}} = 10.5$ nm) samples under a V_G sweep rate of 0.05 V s^{-1}. E_{ox} is given by

$$E_{\text{ox}} = V_{\text{ox}}/t_{\text{ox}} = (V_G - V_{\text{FB}} - \psi_s)/t_{\text{ox}}, \tag{6}$$

in which V_{ox} is the voltage drop across the dielectric film and ψ_s is the semiconductor band bending, negligible under accumulation. The solid lines in Fig. 9 result from using V_{FB} as (i) −0.35 V for the SiO_2 and (ii) 0.5 V for the Si_3N_4 sample. These V_{FB} were obtained from C-V curves showing negligible ΔV_{FB} induced by positive gate bias. The dashed lines take into account ΔV_{FB} data from Fig. 8. Whereas J for the SiO_2 sample remains in the displacement current range up to $E_{\text{ox}} \approx 4.5$ MV cm^{-1}, the onset of significant leakage through Si_3N_4 appears at $E_{\text{ox}} \approx 3$ MV cm^{-1}. Note that the principal breakdown mode of both samples is extrinsic, occurring be-

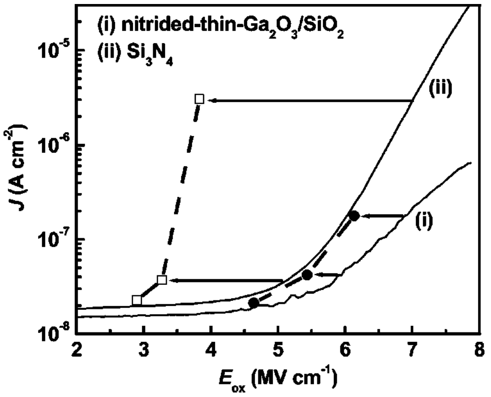

FIG. 9. Current density J versus electric field E_{ox} from (i) n-GaN/nitrided-thin-Ga_2O_3/SiO_2 ($t_{ox}=10.7$ nm) and (ii) n-GaN/Si_3N_4 ($t_{ox}=10.5$ nm) MIS-Cs. Solid lines are obtained by using V_{FB} as (i) -0.35 V and (ii) 0.5 V; dashed lines are obtained by applying V_{FB} shown in Fig. 8.

low 10 MV cm^{-1}, and $J-E_{ox}$ data were chosen among 20 breakdown events.

At present, there are few available reports on $J-E_{ox}$ characteristics of MIS structures on n-GaN and SiO_2 or Si_3N_4. For an ONO structure on n-GaN, the tunneling current was observed above 6 MV cm^{-1}, and the extracted barrier height from the Fowler-Nordheim model was 2.3 eV.[18] For Si_3N_4 on n-GaN, $J \approx 1\times10^{-5}$ A cm^{-2} at 6 MV cm^{-1}, and the conduction-band offset energy was deduced as 0.5 eV based on XPS data.[30] Ga_2O_3 (20–80 nm)/SiO_2 (20 nm) insulator stacks analyzed under the Frenkel-Poole model yielded a forward breakdown field of 2.64–3.56 MV cm^{-1} and a barrier height of 0.63–1.21 eV.[31] Our results lie well within the general framework. A detailed discussion of electrical conduction in our samples, including band offset energy determination will be possible after we obtain improved electron trapping and breakdown behavior.

IV. CONCLUSIONS

We have compared Al-gated n-GaN/nitrided-thin Ga_2O_3/SiO_2 and n-GaN/Si_3N_4 MIS-Cs using C-V, ac conductance, and I-V measurements. On wet-cleaned n-GaN surfaces, nitrided-thin-Ga_2O_3/SiO_2 yielded reduced density of interface defects, electron trapping, and leakage current as compared to Si_3N_4. Reproducibility also distinguishes n-GaN/nitrided-thin-Ga_2O_3/SiO_2 from n-GaN/Si_3N_4 structures. Without separate *in situ* surface cleaning at high temperature, the RPAO-RPAN process provides excellent control of ultrathin interfacial layers that passivate the GaN substrate.

From linear fittings to V_{FB} versus t_{ox} data, ϕ_{ms} and $Q_{f,eff}$ were determined as 0.13 V and $1.0\times10^{12}\ q$ cm^{-2} for SiO_2 and as 0.27 V and $-3.6\times10^{11}\ q$ cm^{-2} for Si_3N_4 samples. The ϕ_{ms} was compared to estimates obtained from spectroscopic data and discussed in terms of interface dipole effects. Both $Q_{f,eff}$ and D_{it} were used to estimate Q_f, and a possible contribution of Q_{pol} was considered. Most of the dielectric-fixed charge in SiO_2 samples should be located at the Ga_2O_3/SiO_2 interface, whereas in Si_3N_4 it could be distributed over the insulating film. At comparable t_{ox}, SiO_2 samples provide lower leakage current and higher breakdown field.

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