optical properties. For example, veins and arteries can be imaged using the different absorption characteristics of blood. Other tissue structures such as nerves and tumours may be imaged using the differences in their light-scattering characteristics [5, 6]. A large percentage of cancers occur inside the body and can be reached and viewed using various types of endoscopes. The endoscopic imaging approach discussed in this Letter could provide information on the presence of cancer not only when it is located on the surface but also, and most important, when cancer is located below the surface. Stomach, cervix, uterus, colon, rectum, bronchus and bladder cancers that are not visible using conventional endoscopic methods could be detected at early stages. In addition, such an endoscopic screening system could assist in monitoring the development of a cancerous tumour(s) for an assessment of the success of the treatment of the patient and during surgery by providing information on the depth of penetration of the tumour. In laparoscopic surgical applications, this method may be used to provide information regarding the presence of tissue structures that need to be preserved such as veins, arteries and nerves.

This endoscopic imaging method may only require small modifications to existing endoscopes to provide inexpensive technology which the medical personnel are already familiar with. As a result, this technology can become an easily accessible screening and diagnostic tool to the medical community due to the anticipated low cost of acquisition and operation and the limited expertise and training required.

Acknowledgments: This work was made possible by funds received from the Cancer Research Fund, under Interagency Agreement 97-12013 (University of California, Davis, contract 98-00924V) with the Department of Health Services, Cancer Research Section. This work was performed under the auspices of the US Department of Energy by the University of California, Lawrence Livermore National Laboratory, under Contract No. W-7405-Eng-48.

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25 June 2001

Electronics Letters Online No: 20020125

DOI: 10.1049/el:20020125

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Reliability degradation of ultra-thin oxynitride and Al₂O₃ gate dielectric films owing to heavy-ion irradiation

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The charge-to-breakdown of 3.3 nm oxynitride films shows significant degradation after irradiation with 342 MeV Au ions. In contrast, 5.4 nm Al₂O₃ films exhibit much less degradation for similar heavy-ion stress.

Introduction: Single-event gate rupture (SEGR) is a catastrophic failure mechanism for MOS structures exposed to heavy ions in space and avionics applications [1, 2]. While this effect has received considerable attention, long-term reliability issues associated with exposure to energetic ions have received little attention [3]. Recently, the study of radiation-induced leakage current (RILC) has shown a fluence dependence (and/or total dose effect) of oxide reliability following heavy-ion irradiation [4]. The purpose of this Letter is to show that heavy-ion irradiation of ultra-thin (<4 nm) gate dielectrics can degrade the reliability as measured through charge-to-breakdown (Q_{BD}). A comparison with 5.4 nm (2.6 nm equivalent oxide thickness) Al₂O₃ thin films is presented.

Experiments: Oxynitride and Al₂O₃ metal-insulator-semiconductor capacitors were fabricated on *p*-type (100) silicon wafers using remote plasma enhanced chemical vapour deposition [5]. Heavy-ion irradiation was performed at the Brookhaven National Laboratory Tandem Van de Graaff facility using 342 MeV Au ions at normal incidence. Fig. 1a shows the measured leakage current increase with Au ion fluence for 3.3 nm oxynitride films. The leakage current, which has been attributed to trap assisted tunnelling [6] or strongly localised breakdown paths [7], had little correlation with the gate bias condition during ion exposure. In addition, degradation of voltage-to-breakdown with ion fluence was observed during linear voltage ramp testing for the oxynitride films. Interestingly, the same amount of heavy-ion stress did not produce any significant change in 5.4 nm Al₂O₃ films as shown in Fig. 1b.

Fig. 1 Gate current against gate voltage after 342 MeV Au ion irradiation at various fluences with gate grounded

a Oxynitride 3.3 nm film
b Al₂O₃ 5.4 nm film
Capacitor area: 100×100 μm², *p*-type substrate
● pre-irradiation
○ 2.5×10⁵ ions/cm²
▼ 2.5×10⁶ ions/cm²
▽ 2.5×10⁷ ions/cm²
■ 1.0×10⁸ ions/cm²

Q_{BD} values were extracted following ion irradiation by numerical integration of measured gate current under a voltage step stress. Fig. 2 shows Weibull plots based on Q_{BD} measurements for both device types after exposure to 342 MeV Au ions. After a fluence of 1.8×10^7 ions/cm², the devices with 3.3 nm oxynitride films showed two orders of magnitude degradation of Q_{BD} , which possibly means significant lifetime shortening of MOS devices. Conversely, the capacitors with 5.4 nm Al₂O₃ gate dielectrics did not exhibit significant degradation after a fluence of 4.3×10^7 ions/cm².

Discussion: Fig. 3 shows the measured log slope of the gate leakage current of the 3.3 nm oxynitride films obtained by linear regression of the current-voltage characteristics obtained between voltage steps during the Q_{BD} measurements. According to leakage current models [6, 7] for ultra-thin oxide gate dielectric films, the log slope of leakage current is said to be related to the transmission coefficient or tunnelling probability of latent breakdown paths. After high energy Au ion irradiation, the log slope changed significantly in contrast to the pre-irradiation results, as shown in Fig. 3. This comparison of the log slope of gate leakage current before and after irradiation supports the existence of a large and variable density of precursor defects that

cause premature breakdown in the 3.3 nm oxynitride films after heavy-ion irradiation. These are likely to be associated with displacement damage to the oxide, and can be significant even for relatively low fluences of 342 MeV Au ions.

Fig. 2 Weibull distribution of charge to breakdown before and after 342 MeV Au ion irradiation

Capacitor area: $50 \times 50 \mu\text{m}^2$, p -type substrate
 ● oxynitride 3.3 nm films before irradiation
 ○ oxynitride 3.3 nm films after 1.8×10^7 ions/cm² fluence
 ▼ Al_2O_3 5.4 nm films before irradiation
 ▽ Al_2O_3 5.4 nm films after 1.8×10^7 ions/cm² fluence

Fig. 3 Measured log slope of leakage current for 3.3 nm oxynitride films at gate voltage of -2.5 V between voltage step stresses for data of Fig. 2

Capacitor area: $50 \times 50 \mu\text{m}^2$, p -type substrate
 Amount of injected charge calculated by numerical integration of measured current during voltage step stresses
 ● oxynitride 3.3 nm film before irradiation
 ○ oxynitride 3.3 nm film after 342 MeV Au 1.8×10^7 ions/cm² irradiation

Conclusions: 3.3 nm oxynitride gate films show significant charge-to-breakdown degradation after energetic ion fluence. In contrast, 5.4 nm Al_2O_3 films show better reliability under the same amount of heavy-ion stress. The increased resistance of the Al_2O_3 films to ion-induced leakage is likely to occur since it is harder for the ion damage to create a completed leakage path across this thicker physical layer than for thinner oxynitride films of equivalent electrical thickness. These results are promising for the use of alternative high- k dielectric films for future MOS technologies in space applications.

Acknowledgment: This work was supported in part by the US Air Force Office of Scientific Research through a Multidisciplinary University Research Initiative (MURI) and by the Defense Threat Reduction Agency through contract number DTRA01-00-C-0010. Research at North Carolina State University is supported by the Office of Naval Research, Air Force Office of Scientific Research, and SEMATECH/SRC Front End Processes Center.

© IEE 2002
 Electronics Letters Online No: 20020119
 DOI: 10.1049/el:20020119

3 November 2001

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Sandia is a multiprogramme laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000

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Design of low-power high-speed bipolar frequency dividers

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A low-power current mode bipolar frequency divider is discussed. Low-power consumption is achieved owing to the design strategy being based on a progressive reduction of bias currents through stages without affecting divider operation speed. The strategy is independent of the process used and simple to design, avoiding the trial-and-error approach based on simulations.

Introduction: The bipolar current mode logic (CML) static frequency divider is a key component in circuits for mobile or satellite communication systems and multiple-Gbit/s optic fibre systems [1-3].

A generic $1/2^n$ static frequency divider consists of n cascaded divide-by-two stages, the topology of which (shown in Fig. 1) includes two cross-coupled D latches, with each input D directly connected to the output of the other latch, and an enabling input CK driven by a level shifter stage. The latter avoids the saturation of transistors $Q1-Q2$ in the CML D-latch circuit, shown in Fig. 2. Differential inputs and outputs are assumed.

The maximum operation frequency f_{max} of a $1/2$ frequency divider characterised by delay τ_{PD} is equal to

$$f_{max} = \frac{1}{2\tau_{PD}} = \frac{1}{2(\tau_{PD,latch} + \tau_{PD,level_shifter})} \quad (1)$$

given that, as seen from Fig. 1, τ_{PD} is the sum of the D-latch delay $\tau_{PD,latch}$ and the level shifter delay $\tau_{PD,level_shifter}$. For high speed