Modeled Tunnel Currents for High Dielectric Constant Dielectrics

Eric M. Vogel, Khaled Z. Ahmed, Brian Hornung, W. Kirklen Henson, Peter K. McLarty, *Senior Member, IEEE*, Gerry Lucovsky, John R. Hauser, *Fellow, IEEE,* and Jimmie J. Wortman, *Senior Member, IEEE*

***Abstract*— The effect of dielectric constant and barrier height on the WKB modeled tunnel currents of MOS capacitors with effective oxide thickness of 2.0 nm is described. We first present the WKB numerical model used to determine the tunneling currents. The results of this model indicate that alternative dielectrics with higher dielectric constants show lower tunneling currents than SiO_2 at expected operating voltages. The results of SiO_2/alternative dielectric stacks indicate currents which are asymmetric with electric field direction. The tunneling current of these stacks at low biases decreases with decreasing SiO_2 thickness. Furthermore, as the dielectric constant of an insulator increased, the effect of a thin layer of SiO_2 on the current characteristics of the dielectric stack increases.**

I. Introduction

As MOSFET device dimensions continue to scale into the sub-0.1-μm regime, the required SiO_2 gate dielectric thickness is projected to reduce below 2.5 nm and the voltage supply ($V_{\rm dd}$) is projected to be from 0.8 to 1.8 V [1]. At these thicknesses and voltages, a large direct tunnel current density flows between the gate electrode and the silicon substrate [2]–[4]. This large direct tunnel current increases power consumption and reduces device performance making SiO_2 undesirable in this thickness regime [4]. Therefore, there has been much interest in finding a high-permitivity gate insulator with equivalent SiO_2 thickness and sufficient barrier height as a replacement for SiO_2. However, since the barrier height tends to decrease with increasing dielectric constant [5], strong tradeoffs exist between various alternative dielectrics.

In this work we provide a comparison of the WKB modeled tunneling currents of various representative dielectrics including: SiO_2, Si_3N_4, SiO_xN_y (silicon oxynitride), high dielectric constant (25–30) insulators, and insulators formed with a layer of SiO_2 and a high dielectric constant dielectric. The modeled tunneling currents do not include the trap-assisted or Frenkel–Poole conduction mechanisms. Therefore, the results indicate the effect of changing the dielectric constant and barrier height of the insulator. Also, some authors have shown small trap densities for some of these dielectrics which would result in predominantly electron tunneling [5]–[8]. Overall, the goal of this study was to provide some initial first-order relationships for various dielectrics that may be used when considering development of any alternative dielectric for the gate insulator of MOS transistors.

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E. M. Vogel, K. Z. Ahmed, B. Hornung, W. K. Henson, J. R. Hauser, and J. J. Wortman are with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695-7911 USA.

P. K. McLarty is with Texas Instruments Inc., Dallas, TX 75625 USA.

G. Lucovsky is with the Department of Physics, North Carolina State University, Raleigh, NC 27695-7911 USA.

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II. Tunneling Model

The following is a description of the model used to calculate the tunneling currents of n$^+$p capacitors in accumulation for a Semiconductor Insulator Semiconductor (SIS) system based on a simple numerical calculation of the WKB transmission coefficient assuming equilibrium in the substrate and gate and no trap-assisted conduction.

The first part of the numerical calculations was to determine the SIS parameters with an insulator whose dielectric constant and band gap varies as a function of distance. The insulator capacitance (C_i) was calculated using

$$C_i = \left[\int_0^{t_{\rm ox}} \frac{dx}{\varepsilon(x)}\right]^{-1} \tag{1}$$

where $t_{\rm ox}$ is the physical oxide thickness and $\varepsilon(x)$ is the dielectric constant as a function of distance in the insulator. The flatband voltage ($V_{\rm fb}$) was calculated from the difference between the gate and substrate Fermi potentials which were determined using full Fermi–Dirac statistics [9], [10]. The gate and substrate surface potentials $(\psi_{\rm gate}, \psi_{\rm sub})$ were numerically solved from the potential and charge balance equations, [2], [9]

$$V_g = \psi_{\rm gate} + \psi_{\rm sub} + V_{\rm fb} - \frac{Q_{\rm sub}(\psi_{\rm sub})}{C_i} \tag{2}$$

$$Q_{\rm sub}(\psi_{\rm sub}) + Q_{\rm gate}(\psi_{\rm gate}) = 0 \tag{3}$$

where $Q_{\rm sub}$ and $Q_{\rm gate}$ are the substrate and gate semiconductor charge found using full Fermi–Dirac statistics [9], [10] and V_g is the gate voltage. The oxide charge was assumed to be zero ($Q_{\rm ox} = 0$). The potential distribution inside the insulator $[V_i(x)]$, total insulator potential drop ($V_{\rm ins}$) and average insulator electric field ($F_{\rm ins} = V_{\rm ins}/t_{\rm ox}$) were then found by solving the Poisson equation. Finally, the insulator conduction band distribution $[E_{\rm ci}(x)]$ was determined using

$$E_{\rm ci}(x) - E_{\rm cg} = \phi_g(x) - qV_i(x) \tag{4}$$

where $E_{\rm cg}$ is the calculated polysilicon gate conduction band energy at the gate/insulator interface and $\phi_g(x)$ is the electron

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affinity difference between the dielectric and polysilicon (i.e., insulator conduction band distribution at flatband). The effects of image forces were ignored.

The second part of the numerical analysis was the calculation of the tunneling current based on these SIS parameters and insulator conduction band. It was assumed that the tunneling current is due only to conduction band electrons which is a good assumption for an n^+p system biased in accumulation [11]. The tunneling current density from the gate (J_g) was calculated assuming an independent electron approximation and an elastic tunneling process [12] using the following formula [2], [10]

$$J_g = \frac{4\pi q m_t}{h^3} \int_0^{E_{\text{fg}}} dE \int_0^{E} T_t(E, E_t)\, dE_t \tag{5}$$

where E_t is the transversal energy, m_t is the transversal effective mass ($\sim 0.19 m_e$), E_{fg} is the gate Fermi level at the gate/insulator (injecting) interface, E is the total energy of the tunneling electron measured from E_{cg}, T_t is the tunneling transmission probability, q is the electronic charge, and $\hbar$ is Planck's constant. Assuming a one-band parabolic dispersion relation for the insulator conduction band, T_t can be calculated using the WKB approximation as [2], [13]

$$T_t(E, E_t) = \exp\left[-\frac{2}{\hbar}\int \sqrt{2m_t E_t - 2m_i[E - E_{\text{ci}}(x)]}\, dx\right] \tag{6}$$

where m_i is the insulator effective mass which is assumed constant. The integration in (6) is over all real values of the argument since we are assuming an elastic tunneling process. We have also assumed as in [10] that a single transmission probability $T_t(E, E_t) = T_t(E_{\text{cg}}, E_{\text{cg}})$ applies to all transitions in calculating the tunneling current. This approximation reduces (5) to

$$J_g = \frac{4\pi q m_t}{h^3} \frac{(E_{\text{fg}} - E_{\text{cg}})^2}{2} T_t(E_{\text{cg}}, E_{\text{cg}}). \tag{7}$$

The goal in using the above numerical model is to provide an indication of the trends expected when changing the dielectric constant and barrier height of the insulators. These tunneling calculations have a number of approximations that must be considered. Quantum-mechanical quantization effects in the semiconductor were not included. However, these quantum-mechanical effects have been shown to not strongly effect calculated tunneling currents due to compensating effects if the calculations are performed relative to insulator potential [3]. However, for devices with thicknesses in this regime, these quantization effects must be considered when calculating surface potentials, oxide potentials, etc., as a function of gate voltage. Another issue is in the use of the WKB solution for these structures. Although the WKB solution has been shown to provide a reasonable fit to experimental data by fitting the effective mass and barrier height [2], [10], [11], the physical basis for this model for ultrathin dielectrics has been debated [3]. Furthermore, we have used a constant effective mass for all energies, thicknesses and dielectrics which may not be appropriate. There is a lack of reliable effective mass values for various dielectrics. The effective masses of the alternative dielectrics may be different and could change the magnitude of the differences in tunneling current. However, these WKB numerical calculations will provide a first order indication of the impact of dielectric constant and barrier height on tunneling currents to be used to indicate general trends expected for future dielectrics.

III. Results and Discussion

To check the accuracy of our numerical calculations, the current density for an SiO_2 layer with thickness of 2.0–4.0 nm was calculated using our numerical model and compared with the current density calculated using a full numerical integration of (5) with analytical expressions for the transmission coefficients. This was done to ensure that our numerical solution correctly fit other similar WKB formulations. The transmission coefficients previously determined for direct and Fowler–Nordheim tunneling (T_{fn}, T_d) into SiO_2 with a constant barrier height (ϕ_g) and constant dielectric constant are shown at the bottom of the page in (8) and (9) [2]. Table I gives the parameters assumed for the gate electrode and Si substrate and Table II contains the parameters assumed for the SiO_2 insulator. We have fit this numerical model to experimental data for SiO_2 down to 2.0 nm using an effective mass of $m_i = 0.32 m_e$. A constant effective mass of $m_i = 0.32$ was assumed for these calculations [2]. The results shown in Fig. 1 indicate good agreement between the models suggesting that our numerical formulation is in agreement with other WKB calculations.

The tunneling model described in the previous section was used to compare the tunneling currents of a variety of insulators termed: SiO_2, Si_3N_4, SiO_xN_y, D1, and D2. Dielectric/SiO_2 stacked structures were also examined.

$$T_{\text{fn}}(E, E_t) = \exp\left[-\frac{4(2\pi)}{3}\frac{\sqrt{2m_i}}{qh}\frac{\left(\phi_g + E_{\text{fg}} - E + \frac{m_t}{m_i}E_t\right)^{3/2}}{F_{\text{ins}}}\right] \tag{8}$$

$$T_d(E, E_t) = \exp\left[-\frac{4(2\pi)}{3}\frac{\sqrt{2m_i}}{qh}\frac{\left(\phi_g + E_{\text{fg}} - E + \frac{m_t}{m_i}E_t\right)^{3/2} - \left(\phi_g + E_{\text{fg}} - E + \frac{m_t}{m_i}E_t + qV_{\text{ins}}\right)^{3/2}}{F_{\text{ins}}}\right] \tag{9}$$

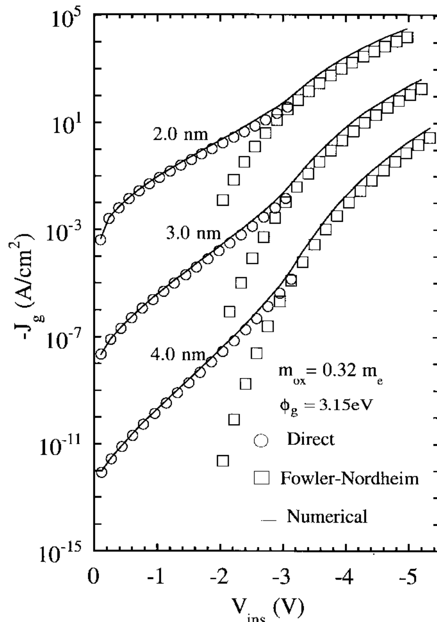

Fig. 1. Comparison of our numerical WKB model of calculating tunneling current for SiO_2 (2.0–4.0 nm) to a full numerical integration of (5) using the previously determined analytical transmission coefficients for direct and Fowler–Nordheim tunneling into SiO_2 [2].

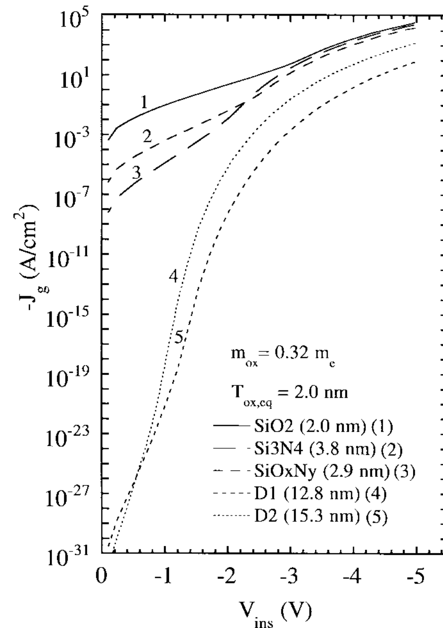

Fig. 2. Tunneling current versus insulator potential for n^+p capacitors with various dielectrics having equivalent oxide thickness of 2.0 nm.

TABLE I
GATE ELECTRODE AND Si SUBSTRATE SEMICONDUCTOR PARAMETERS USED IN CALCULATING THE TUNNELING CURRENTS

	Gate Electrode	*Si Substrate*
Dielectric Constant (ε)	$11.8\varepsilon_o$	$11.8\varepsilon_o$
Doping (N_d, N_a)	$1.00 \cdot 10^{20}$ cm^{-3}	$2.00 \cdot 10^{17}$ cm^{-3}
Dopant Ionization Energy (E_c-E_d, E_c-E_a)	0.045 eV	1.075 eV
Energy Gap (E_g)	1.12 eV	1.12 eV
Effective Density of States in Conduction Band (N_c)	$2.80 \cdot 10^{19}$ cm^{-3}	$2.80 \cdot 10^{19}$ cm^{-3}
Effective Density of States in Valence Band (N_V)	$1.04 \cdot 10^{19}$ cm^{-3}	$1.04 \cdot 10^{19}$ cm^{-3}
Intrinsic Carrier Concentration (n_i)	$1.45 \cdot 10^{10}$ cm^{-3}	$1.45 \cdot 10^{10}$ cm^{-3}

TABLE II
INSULATOR DIELECTRIC CONSTANT AND BARRIER HEIGHT USED IN CALCULATING THE TUNNELING CURRENTS. THE BARRIER HEIGHT IS DEFINED AS THE CONDUCTION BAND DISCONTINUITY BETWEEN THE INSULATOR AND SILICON

	Dielectric Constant (ε)	*Barrier Height*
SiO_2 [9]	$3.9\varepsilon_o$	3.15 eV
Si_3N_4 [9]	$7.5\varepsilon_o$	2.10 eV
SiO_xN_y	$5.7\varepsilon_o$	2.60 eV
D1	$25.0\varepsilon_o$	1.30 eV
D2	$30.0\varepsilon_o$	1.00 eV

Table II indicates the dielectric constant and barrier height used for each of the insulators. The barrier height is defined as the conduction band discontinuity (electron affinity difference) between the insulator and silicon. Note that the oxynitride film (SiO_xN_y) has an assumed dielectric constant and barrier height halfway between the values for Si_3N_4 and SiO_2 [9]. The values chosen for D1 and D2 are representative of several higher dielectric constant (high-k) alternative insulators (e.g., TiO_2, Ta_2O_5) [5]–[7], [14]–[20]. The total thickness of each of the insulators was chosen to achieve an SiO_2 equivalent thickness of 2.0 nm. The effective mass was assumed constant for each insulator ($m_i = 0.32m_e$) so that the effect of barrier height and dielectric constant could be easily discerned. The tunneling currents from the gate were calculated assuming an n^+p capacitor with the parameters given in Table I.

Fig. 2 shows the tunneling currents calculated for each of the dielectrics as a function of total insulator potential drop. The results indicate that for very low voltages, the insulators with the highest dielectric constant show the lowest tunneling currents. The currents for D1 and D2 are observed to cross at $|V_{\rm ins}| = \sim 0.6$ V. This cross-over can be qualitatively explained by considering that the current (7) is proportional to the transmission coefficient (6). The transmission coefficient is inversely and exponentially dependent on an integration of the square root of the insulator conduction band in which the electron travels under (which we will call barrier area). Therefore, the cross-over occurs when the increase of barrier area due to the tunneling distance of D2 is compensated for by the increase in barrier area due to the barrier height of D1. A large increase of current for each of the insulators is observed for $|V_{\rm ins}| > \phi_g$ because the tunneling electrons begin to tunnel through less of a distance and enter the insulator conduction band (Fowler–Nordehim tunneling). The results suggest that to reduce the expected tunnel current, it is more beneficial to have a high-k dielectric with ϕ_g slightly higher than the expected supply voltage ($V_{\rm dd} \approx 1$ V) for $T_{\rm ox,\,eq} = 2.0$ nm, than to have an insulator with slightly higher dielectric constant but lower ϕ_g. It is also observed that Si_3N_4 and SiO_xN_y show modest improvements over SiO_2. However, these insulators with $\phi_g > V_{\rm dd}$ do not have the high dielectric constant needed to further reduce the current.

The results of Fig. 2 indicate that replacement of SiO_2 with an alternative dielectric results in a reduction of tunnel current

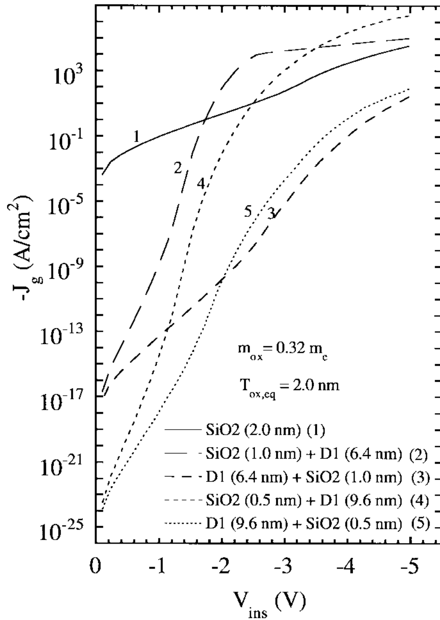

Fig. 3. Tunneling current versus insulator potential for n^+p capacitors with $D1/SiO_2$ stacked dielectrics having equivalent oxide thickness of 2.0 nm.

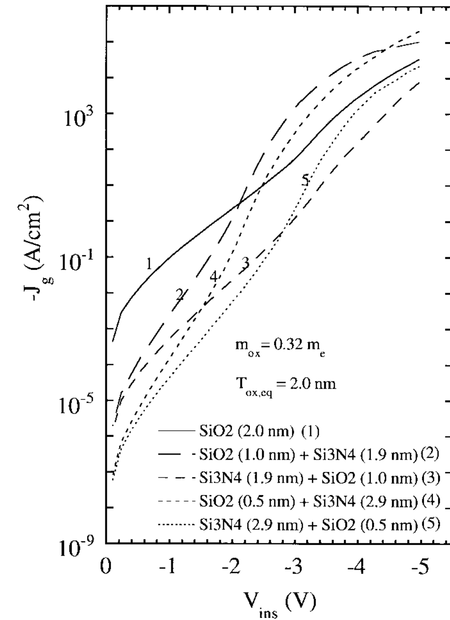

Fig. 4. Tunneling current versus insulator potential for n^+p capacitors with Si_3N_4/SiO_2 stacked dielectrics having equivalent oxide thickness of 2.0 nm.

which is most significant at lower voltage. However, instead of using only and alternative dielectric, many researchers have used SiO_2/alternative dielectric stacks [6], [21]–[23]. The reasons for this include controlling interface state density and modifying barrier properties. Also, the SiO_2 in these stacked structures can be present as a native oxide at the Si interface [18]. Figs. 3 and 4 show the calculated tunneling currents for $D1/SiO_2$ and Si_3N_4/SiO_2 stacked structures, respectively. The insulator which is listed first is the dielectric which the electron first tunnels through. The change in the order of the insulator stack is equivalent to changing the electric field direction on this stack.

It is observed that the tunneling currents change dramatically depending on which insulator the electron first tunnels through. Specifically, the tunnel current is much higher if the electron first tunnels through the higher barrier height material (SiO_2). This can be best understood by considering the insulator conduction band diagrams given in Fig. 5 for the SiO_2 (1.0 nm)/D1 (6.4 nm) stacks for $V_{\rm ins} = -2.38$ V. It is observed that at this voltage (and above), an electron which first tunnels through the SiO_2, no longer tunnels through any of the D1 barrier so that the tunneling is determined only by the 1.0 nm SiO_2 barrier. However, an electron which first tunnels through the D1 barrier, will also tunnel through the SiO_2 barrier for these voltage ranges. The insulator voltage at which the electron will no longer tunnel through the second barrier approximately corresponds to the condition when the SiO_2 layer drops a voltage equivalent to the barrier height of the second layer.

Fig. 6 shows the insulator conduction band for SiO_2 (0.5 nm)/D1 (9.6 nm) stacks for the same voltage ($V_{\rm ins} = -2.38$ V). Comparison of Figs. 5 and 6 indicate that for this insulator potential, an electron will tunnel through a larger portion of the barrier for stacks with thinner SiO_2

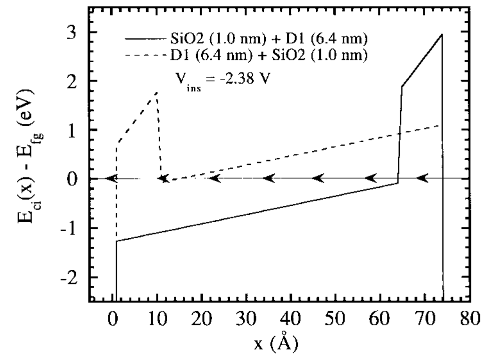

Fig. 5. Insulator conduction band distribution referenced to the gate Fermi level for SiO_2 (1.0 nm)/D1 (6.4 nm) stacked dielectrics at an insulator potential of -2.38 V.

regions. When the bias is increased further, an electron which first tunnels through the 0.5 nm SiO_2 barrier will no longer tunnel through the D1 barrier so that the tunneling is determined only by the 0.5 nm SiO_2 barrier. Therefore, for very high biases, the tunneling current for the SiO_2 (0.5 nm) + D1 (9.6 nm) stack will be greater than the tunneling current for the SiO_2 (1.0 nm) + D1 (6.4 nm) since the tunneling distance is shorter.

Comparing Figs. 3 and 4 shows that stacked insulators using Si_3N_4 result in smaller current changes than in using D1. This is simply because the current for biases when the electron is tunneling through the entire barrier is closer to the current for biases when the electron is tunneling only through the SiO_2. Furthermore, the barrier heights and dielectric constants of the Si_3N_4 and SiO_2 insulators are much closer than D1 and SiO_2 so that the total barrier for the electron is less affected for the Si_3N_4/SiO_2 stacked structures. This result indicates that a thin layer of SiO_2 with Alt1 results in a drastic difference in current as compared to Si_3N_4.

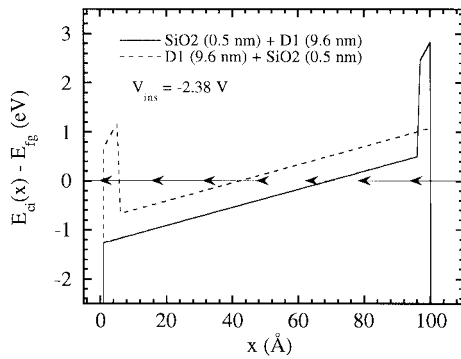

Fig. 6. Insulator conduction band distribution referenced to the gate Fermi level for SiO_2 (0.5 nm)/D1 (9.6 nm) stacked dielectrics at an insulator potential of −2.38 V.

IV. Summary

The tunneling currents for insulators with an effective oxide thickness of 2.0 nm were modeled using a numerical calculation of the WKB tunneling current. Our model was shown to agree with previously determined analytical WKB formulations of tunneling current for SiO_2. The numerical tunneling model was first applied to alternative dielectrics having different barrier heights and dielectric constants. The results indicated that alternative dielectrics with higher dielectric constants resulted in lower currents at low biases. However, it was concluded that it is more beneficial to have a high-k dielectric with barrier height slightly higher than the expected supply voltage, than to have an insulator with slightly higher dielectric constant. The numerical tunneling model was then applied to SiO_2/alternative dielectric stacks. The results indicated that the tunnel current changes dramatically for these stacks with change in electric field direction (change in which barrier the electron first tunnels through). It was observed that the tunneling current of these stacks at low biases decreases with decreasing SiO_2 thickness. Furthermore, as the dielectric constant of an insulator increased, the effect of a thin layer of SiO_2 on the current characteristics of the dielectric stack increased.

Overall, the modeled tunneling current characteristics for these ideal alternative dielectrics (no trap-assisted current) have provided an indication of the trends expected when modifying the dielectric constant and barrier height of insulators. The above calculations show that if an alternative high dielectric constant material is to replace SiO_2, then it will be necessary to find one with a barrier height greater than the applied voltage and one that can be fabricated with a few atomic layers (or less) of SiO_2 at the interface. This may prove to be a difficult challenge for future IC manufacturing.

References

[1] *The National Technology Roadmap for Semiconductors.* Semiconductor Industry Assoc., Austin, TX, 1997.

[2] M. Depas, B. Vermeire, P. W. Mertens, R. L. Meirhaeghe, and M. M. Heyns, "Determination of tunneling parameters in ultra-thin oxide layer poly-Si/SiO_2/Si structures," *Solid State Electron.,* vol. 38, pp. 1465–1471, 1995.

[3] F. Rana, S. Tiwari, and D. A. Buchanan, "Self-consistent modeling of accumulation layers and tunneling currents through very thin oxides," *Appl. Phys. Lett.,* vol. 69, pp. 1104–1106, 1996.

[4] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S.-I. Nakamura, M. Saito, and H. Iwai, "1.5 nm direct-tunneling gate oxide Si MOSFET's," *IEEE Trans. Electron Devices,* vol. 43, pp. 1233–1242, Dec. 1996.

[5] S. A. Campbell, D. C. Gilmer, X.-C. Wang, M.-T. Hsieh, H.-S. Kim, W. L. Gladfelter, and J. Yan, "MOSFET transistors fabricated with high permitivity TiO_2 dielectrics," *IEEE Trans. Electron Devices,* vol. 44, pp. 104–109, Jan. 1997.

[6] G. Q. Lo, D. L. Kwong, and S. Lee, "Metal-oxide-semiconductor characteristics of chemical vapor deposited Ta_2O_5 films," *Appl. Phys. Lett.,* vol. 60, p. 3286, 1992.

[7] X.-W. Wang, T.-P. Ma, G.-J. Cui, T. Tamagawa, J. W. G. S. Karechi, B. H. Halpern, and J. J. Schmitt, "Highly reliable silicon nitride films made by jet vapor deposition," *Jpn. J. Appl. Phys.,* vol. 34, p. 955, 1995.

[8] X. Wang, M. Khare, and T. P. Ma, "Effects of water vapor anneal on MIS devices made of nitrided gate dielectrics," in *1996 Symp. VLSI Technol. Dig. Tech. Papers,* pp. 226–227.

[9] S. M. Sze, *Physics of Semiconductor Devices,* 2nd ed. New York: Wiley, 1981.

[10] N. G. Tarr, D. L. Pulfrey, and D. S. Camporese, "An analytic model for the MIS tunnel junction," *IEEE Trans. Electron Devices,* vol. ED-30, pp. 1760–1770, Dec. 1983.

[11] S. Nagano, M. Tsukiji, K. Ando, E. Hasegawa, and A. Ishitani, "Mechanism of leakage current through the nanoscale SiO_2 layer," *J. Appl. Phys.,* vol. 75, p. 3530, 1994.

[12] W. A. Harrison, "Tunneling from an independent-particle point of view," *Phys. Rev.,* vol. 123, p. 85, 1961.

[13] E. Merzbacher, *Quantum Mechanics.* New York: Wiley, 1961.

[14] L. K. Han, G. W. Yoon, D. L. Kwong, V. K. Mathews, and P. C. Fazan, "Effects of post-deposition annealing on the electrical properties and reliability of ultrathin chemical vapor deposited Ta_2O_5 films," *IEEE Electron Devices Lett.,* vol. 15, p. 280, Aug. 1994.

[15] S. Shibata, "Dielectric constants of Ta_2O_5 thin films deposited by r.f. sputtering," *Thin Solid Films,* vol. 277, pp. 1–4, 1996.

[16] K. Kukli, J. Aarik, A. Aidla, O. Kohan, T. Uustare, and V. Sammelselg, "Properties of tantalum oxide thin films grown by atomic layer deposition," *Thin Solid Films,* vol. 260, pp. 135–142, 1995.

[17] A. Pignolet, G. M. Rao, and S. B. Krupanidhi, "Rapid thermal processed thin films of reactively sputtered Ta_2O_5," *Thin Solid Films,* vol. 258, pp. 230–235, 1995.

[18] J. L. Autran, P. Paillet, J. L. Leray, and R. A. B. Devine, "Conduction properties of amorphous Ta_2O_5 films prepared by plasma enhanced chemical vapor deposition," *Sens. Actuators A,* vol. 51, pp. 5–8, 1995.

[19] W. S. Lau, K. K. Khaw, P. W. Qian, N. P. Sandler, and P. K. Chu, "Defect states responsible for leakage current in Ta_2O_5 films on Si due to Si contamination from the substrate," *J. Appl. Phys.,* vol. 79, pp. 8841–8843, 1996.

[20] H. Shimada and T. Ohmi, "Current drive enhancement by using high-permittivity gate insulator in SOI MOSFET's and its limitation," *IEEE Trans. Electron Devices,* vol. 43, pp. 431–435, Mar. 1996.

[21] R. A. B. Devine, "Nondestructive measurement of interfacial SiO_2 films formed during deposition and annealing of Ta_2O_5," *Appl. Phys. Lett.,* vol. 68, pp. 1924–1926, 1996.

[22] S. K. Madan, "DRAM plate electrode bias optimization for reducing leakage current in UV-O_3 and O_2 annealed CVD deposited Ta_2O_5 dielectric films," *IEEE Trans. Electron Devices* vol. 42, pp. 1871–1873, Oct. 1995.

[23] S. Mori, Y. Y. Araki, M. Sato, H. Meguro, H. Tsunoda, E. Kamiya, K. Yoshikawa, N. Arai, and E. Sakagami, "Thickness scaling limitation factors of ONO interpoly dielectric for nonvolatile memory devices," *IEEE Trans. Electron Devices,* vol. 43, pp. 47–53, Jan. 1996.

Eric M. Vogel was born in Charleroi, PA, in 1972. He received the B.S. degree in electrical engineering with honors from The Pennsylvania State University, University Park, in 1994. He is currently pursuing the Ph.D. degree in the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh. His research interests include gate dielectrics, interface physics, device reliability, oxynitrides, and rapid thermal processing.

Khaled Z. Ahmed was born in Cairo, Egypt, in 1968. He received the B.S. and M.S. degrees in electrical engineering with honors from Ain Shams University, Cairo, in 1991 and 1994, respectively. He is currently pursuing the Ph.D. degree in the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh. His research interests include gate dielectrics, device physics, modeling, and characterization.

Brian Hornung was born in Elkin, NC, on September 27, 1969. He received the B.S., M.S., and Ph.D. degrees in electrical engineering in 1992, 1993, and 1997, respectively, all from North Carolina State University, Raleigh, where he worked on advanced tunnel dielectrics for floating gate nonvolatile memory applications.

He is currently with the Semiconductor Technologies Laboratories at Motorola, Inc., Austin, TX.

W. Kirklen Henson was born in Gastonia, NC, in 1972. He received the B.S. and M.S. degrees in electrical engineering from North Carolina State University in 1994 and 1995, respectively, where he is currently pursuing the Ph.D. degree. His research involves ultrathin dielectrics, device physics, and rapid thermal processing.

Peter K. McLarty (M'90–SM'95) was born in Kingston, Jamaica, on February 12, 1962. He received the B.Sc. degree in pure and applied physics in 1983 from the University of the West Indies, Jamaica, and the M.Sc. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1986 and 1989, respectively.

In August 1989, he joined the Electrical and Computer Engineering Department, North Carolina State University, Raleigh, as an Assistant Professor, where his main research efforts were focused on the fabrication and characterization of new semiconductor devices and materials. In 1996, he joined Texas Instruments, Dallas, TX, where he is currently working in productization.

Gerry Lucovsky received the B.S. and M.A. degrees in physics from the University of Rochester, Rochester, NY, in 1956 and 1958, respectively, and the Ph.D. degree in physics from Temple University, Philadelphia, PA, in 1960.

He spent several years in industry. From 1958 to 1965, at Philco Corporation in Blue Bell, PA, and from 1965 to 1980, at Xerox Corporation at the research centers in Webster, NY, and in Palo Alto, CA (PARC), where he was a Senior Research Fellow and Manager of the General Sciences Laboratory. In 1980, he joined the Department of Physics at North Carolina State University (NCSU), Raleigh, as a University Professor of Physics. He is also a member of the Departments of Materials Science and Engineering, and Electrical and Computer Engineering. His research activities at NCSU span a broad range from basic studies of electronic materials to the application of plasma processing in the fabrication of electronic devices: a-Si thin film transistors (TFT's) and dielectrics and gate electrodes for c-Si FET's. He is a Research Center Coordinator in the NSF sponsored Engineering Research Center for the Advanced Electronic Materials Processing which is also supported by SRC and SEMATECH.

John R. Hauser (S'59–M'60–SM'78–F'87) was born near Mocksville, NC, on September 19, 1938. He received the B.S. degree in electrical engineering from North Carolina State University (NCSU), Raleigh, in 1960, and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, in 1962 and 1964, respectively.

In 1960 and 1961, he joined Bell Telephone Laboratories, Winston-Salem, NC, where he worked on the design of electronic circuits. In June 1962, he joined the Research Triangle Institute, Durham, NC, where he conducted research work on semiconductor and microelectronic devices. He joined the faculty at NCSU in September 1966, where he is presently a Professor in Electrical Engineering and Director of the Solid State Electronics Laboratory. His present interests are in the areas of microelectronics and solid state devices.

Dr. Hauser is a member of Eta Kappa Nu, Sigma Xi, and the American Physical Society.

Jimmie J. Wortman (M'72–SM'88) was born in North Carolina on February 23, 1936. He received the B.S. degree (with honors) in nuclear engineering from North Carolina State University (NCSU), Raleigh, in 1960, and the M.S. and Ph.D. degrees from Duke University, Durham, NC, in 1962 and 1965, respectively.

He was with Bell Telephone Laboratories as a Member of the Technical Staff from 1960 to 1962. From 1962 to 1980, he worked at the Research Triangle Institute, Research Triangle Park, NC. During that period, he held the positions of Research Engineer, Senior Scientist, manager of several departments, and Director of the Engineering Division. He is currently a Professor in the Electrical and Computer Engineering Department at NCSU. His current research interests include rapid thermal processing, rapid thermal oxides, and stacked gate dielectric structures.