ABSTRACT

KE, HAOTAO, 3-D Prismatic Packaging Methodologies for Wide Band Gap Power electronics Modules (Under the direction of Dr. Douglas C. Hopkins)

With the development of advanced Wide Band Gap (WBG) devices, power electronic systems with higher frequency, temperature, and voltage are becoming the trend due to their higher efficiency and potentially lower system cost than Si counterpart.

To fully utilized the advantage of WBG power devices for the application, improvement are greatly needed for power packaging mechanism. Efforts have been made by researchers in improving traditional power module layout and building new double sided power module.

In this work, investigation into 3D methodology for power packaging is carried out. New 3D prismatic packaging concept is proposed for WBG power device, in which the devices are mounted vertically on the side wall of the module with 3D interconnect inside to achieve elevated electrical/thermal/mechanical performance.

For validation of the 3D prismatic packaging methodology, different Additive Manufacturing (AM) processes have been evaluated for the compatibility with power electronic packaging. A 1200V/50A SiC half bridge power module is fabricated and tested. The result has been analyzed with simulation and discussed, together with possible future work in the area.

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3-D Prismatic Packaging Methodologies for Wide Band Gap Power electronics Modules

by
Haotao Ke

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APPROVED BY:

Douglas Hopkins
Chair of Advisory Committee

Ola Harrysson

Jayant Baliga

Subhashish Bhattacharya

DEDICATION

I dedicate this dissertation work to my beloved parents, for their guidance throughout my
life.

BIOGRAPHY

Haotao Ke received his BS in Electrical Engineering from Tsinghua University in 2011 China. Then he joined the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center as a research assistant. He is also a member of the Packaging Research in Electronic Energy Systems (PREES) Laboratory. His primary focus is power electronics packaging for wide band gap power devices. He is exploring the potential of additive manufacturing technology to develop new topologies and processes for next generation WBG power electronics package in 3D.

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Chapter 1 Introduction

Power modules shield the power semiconductor devices against the environment, provide electrical interconnection, and thermal management. Since the establishment of the power module in late last century, the mature wire bonded structure has little change throughout the era when the silicon-based power devices dominated the market [1]. Now the situation has changed with the development of new Wide Band Gap (WBG) power semiconductors. Compared with silicon-based power electronics systems, WBG-based systems are faster, more energy efficient, and compact in size. As a key influence in system performance, the packaging technology is also improving.

1.1 Background

Novel WBG power semiconductor devices (SiC, GaN, and Diamond in the future) are innovating the depth and breadth of the power electronics technology with simpler circuit configurations and new applications, such as for electric vehicles and smart grid. It is believed that as material process mature, the price of the WBG power device will be sufficiently low to allow the system to compete more cost-effectively with silicon [2].

The new WBG material has better properties (bandgap, mobility, etc.) than the Si, which means the WBG-based power devices can operate at much higher voltage and current ratings at a faster speed than the silicon ones [3]. Most of the SiC power devices are used in application over 900V for its high voltage blocking capability. The GaN-based device is attractive in application of lesser voltage due to its high carrier mobility. Also, the working temperature of the WBG devices are higher. The SiC device operates at a junction temperature as high as 500-

550 °C as compared to a typical 125-150 °C maximum junction temperature of silicon devices [4].

Most SiC power module packaging has been following traditional silicon design module with wire bonding as the interconnect method (figure 1.1(a)), while wire bonds bring in parasitic inductances that cause voltage overshoot during the switching. Also, the wire-bonded side of the chip, which is usually close to the heat source, disallows direct double-sided cooling. Since GaN devices operate at much higher current density and frequency, the drawback of wire bondings is more serve. Thus, the GaN-based package usually has a wire bondless design, e.g. ball grid array (BGA), to enable high speed switching. Figure 1.1 (b) shows the GaN HEMT package with wire bondless design, which utilized the copper inside the substrate to serves as electrical signal interconnect and thermal heat spreader.

Figure 1.1(a) 1200V/50A SiC MOSFET power module (b) 650V/30A GaN HEMT package

To achieve higher WBG performance (e.g. higher frequency and lower loss) through advanced packaging, it is well accepted [5] that a WBG power module should meet the following criteria:

1. Low parasitic inductance, which is the key to reducing device switching loss and improving the module speed.
2. Better thermal management, which is the key to elevate the power rating and long term reliability of the module.
3. Better packaging materials, which is the key to exploit the high working temperature and high voltage blocking capability for the power module.

Ultra-low inductance is one of the major challenges for future WBG power modules. This dissertation provides a new approach to ultra-low inductance through 3D prismatic power module.

1.2 Dissertation Objectives

The object of this research is to utilize the 3D printing process to design a new 3D structure, based on the concept of mutual inductance cancelation, meanwhile the module is capable of working at a higher temperature.

The content will start with the discussion on current path optimization in 3D space based on theoretical reasoning. A basic switching topology will be used for studying the current flow inside the module. The inductances of each current path will be determined and the effect of field cancellation will be utilized for deriving a 3D power flow path with low stray inductance. Then, a 3D printing process will be evaluated for physical realization of a proposed 3D structure. The present 3D-printing processes have limited usage in power electronics packaging. However, new materials and processes are constantly being introduced. Within the confines when this research began, investigation and experiments were carried out based on materials primarily used in a power module. This provided a certain level of continuity and confidence

to designers in the power module industry, and provided easier understanding. Certain 3D printing processes that fit well for power packaging were selected for building the 3D prismatic module.

After evaluation of 3D printing processes, a SiC MOSFET half-bridge module was redesigned using a 3D prismatic packaging concept. Other types of devices could also benefit from this 3D packaging concept as well. New processes for fabricating the module were evaluated and tested. Problems found during testing are described, and solved before final module design.

The 3D redesigned half-bridge module was modeled in the COMSOL Multiphysics, an FEA solver that can deal with coupled physical fields. Also, the Ansoft Q3D Extractor, an electromagnetic simulation tools for calculating parasitic parameters, was used for extracting the inductance inside the designed structure. The design of the 3D geometry was optimized by using these tools for evaluating the electrical, thermal, and mechanical performance during the design cycle.

After the 3D structure was determined for the module, a circuit simulation was carried out for the dynamic performance of the module. LTspice was used as the simulation tool for its fast and relatively accurate simulation for power devices. The dynamic electrical performance of the module was characterized by measuring the turn-on and turn-off behaviors through a double-pulse tester (DPT) circuit. Parasitic electrical elements of the DPT circuit was also extracted and used in the simulation. Thermal and electrical tests were performed on the fabricated module. The thermal resistance was calculated with the measured temperature difference through the module and the power dissipation. The electrical parameters will be obtained from the test result of the DPT. Comparison will be made between the test result and simulation.

1.3 Dissertation Outline

Based on the discussion above, the outline of the dissertation is organized as the following sequence:

Chapter 2 is the literature review for current work towards WBG power semiconductor packaging. The improvements in material, structure, and new design are reviewed.

Chapter 3 discusses the structural design of the 3D prismatic module. The design comes from the concept of mutual inductance cancellation. A three phase full bridge design is proposed.

Chapter 4 introduces the 3D printing process for the power packaging process. The evaluation of different 3D printing process and experiments carried out are discussed. An investment metal casting process with 3D wax model is chosen for building 3D prismatic module.

Chapter 5 demonstrate the design and fabrication of a 1200V/50A SiC MOSFET half bridge 3D prismatic module. Various simulations are carried out through the design process. The experimental test for the module is also documented, including the component test, thermal test, and dynamic switching test. The result is compared with the simulation and discussed.

Chapter 6 summarized the work done through the dissertation, main contribution from the research and the potential future work

1.4 Reference

- [1] C. Neeb, L. Boettcher, M. Conrad and R. W. De Doncker, "Innovative and Reliable Power Modules: A Future Trend and Evolution of Technologies," in IEEE Industrial Electronics Magazine, vol. 8, no. 3, pp. 6-16, Sept. 2014.
- [2] H. A. Mantooth, M. D. Glover and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 374-385, Sept. 2014.
- [3] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014.
- [4] P. Ning, T. Guangyin Lei, F. Wang, G. Q. Lu, K. D. T. Ngo and K. Rajashekara, "A Novel High-Temperature Planar Package for SiC Multichip Phase-Leg Power Module," in IEEE Transactions on Power Electronics, vol. 25, no. 8, pp. 2059-2067, Aug. 2010.
- [5] J. Schuderer, U. Vemulapati and F. Traub, "Packaging SiC power semiconductors — Challenges, technologies and strategies," 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, 2014, pp. 18-23.

Chapter 2 Literature Review

This research investigates a new fundamental approach to power module. Traditionally power module are essentially 2D, i.e. flat, planar structures. Even recent 3D approaches are using “stacked” 2D planar structures. This work investigates the use of 3D structure, with a primary focus on orthogonal component placement.

A graphic of a traditional power electronics module is shown in Fig. 2.1. The primary parts are: baseplate, metal clad ceramic substrate, terminals, power semiconductor chip, bonding wires, encapsulation, and housing. A recent variation uses an organic resin to replace the ceramic [1]. The module can be viewed as a four terminal box with high power electrical energy entering and exiting, low power (gate drive) electrical energy entering and exiting, and thermal and mechanical energy exiting. The semiconductor chip is the source of the electric to thermal conversion. Thus the main function the power module is to conduct energy safely (electric/thermal) between terminals. While at the same time the heat generated by the devices should be dissipated out through the baseplate to assure the temperature of the devices do not exceed their limitations.

Figure 2.1 Structure of the power module

The baseline for the package is that the package should not limit the performance of the power device inside. The electrical and thermal aspects are two main concerns during the design. One key aspect of the module is thermal energy dissipated from the power semiconductor. Based on the thermal equation

$$\Delta T = Q \times R_{\theta(total)} \quad (2.1)$$

In which ΔT is temperature rise between the chip and the ambient, Q is the heat flux generated by the device, and $R_{\theta(total)}$ is the total thermal resistance on the heat flow path. For WBG devices, which have a much higher switching frequency than Si devices, the heat flux generated is higher. Also the WBG material could work at an elevated temperature than silicon devices. While current material systems in the power module have limitation on its maximum operation temperature. To elevate the working temperature of the power module, the module material systems is updated. For the ceramic substrate, material like silicon nitride and process as active metal brazed (AMB) substrate have been evaluated for the high temperature reliability [2]. Nano silver sintering is developed for lower temperature and less pressure requirement [3]. For the encapsulation, different state of art high temperature encapsulation is characterized [4] and work is carried out other materials like Bismaleimide (BMI), Polyimide (PI), Cyanate Ester (CE), and Benzocyclobutene (BCB). But there is still a long way to go [5]. Parylene HT coating, with 400C working temperature, is also investigated, with special process limitation [6].

The electrical performance of a module is greatly affected by the parasitic inductances introduced by the module architecture. Considering a half-bridge power module, the key parasitics are commutation loop stray inductance, gate loop inductance, and gate circuit coupling

inductance. The commutation loop stray inductance is responsible for the voltage overshoot during turn-off, slower commutation switching, and increase EMI emission [7]. While the gate loop inductance and gate circuit coupling inductance affects the performance of the gate circuit, which is mainly considered with gate driver design. The WBG power modules need to fit for high speed switching, which requires low parasitic inductance for the designed architecture. In such case, some discrete packages like TO-247, with a 3.2nH [8] measured inductance between the power terminals, would bring in additional parasitic inductance in the converter. Thus a power module with low stray inductance desired. In general, reduction of the stray inductance could be achieved by modifying the design of the electrical conductors. For example, a shorter and wider conductor pattern, like a thicker and shorter wire, and paralleled terminals will work. Traditional DBC substrates are easy to be routed, while the wide spacing between the traces is hard to be shrunk due to the voltage isolation and manufacture process [9]. Current development for the power module is mainly happens on the power module's architecture, which could be grouped as three categories: conventional 2D power package, new planar 2D power package, and the developing 3D power package.

2.1 Conventional 2D power package structure

To make the full use of the current power module structure, optimization based on the traditional module is done. The wire bonds are the main interconnection method on the device top metallization in 2D structure. Suppression of the stray inductance is achieved with the 2D structure by utilizing the spacing above the substrate for placing returning current.

Figure 2.2 ABB 1.2kV/700A LinPAK [10]

ABB presented their 1.2kV/700A LinPAK with improved structure on DBC substrate. Their solution is to use a stack-ceramic-substrate structure inside the module to distribute the power in different layers of metals, as figure 2.2 shows. By which a mutual inductance cancellation is achieved and enhanced electrical performance of 11nH stray inductance was got from their result [10]. GE has presented their 1.7kV/500A power module with a stray inductance reported as low as 4.5nH [11]. Laminated bus bar is used inside the module to provide the field cancellation effect. Bus bar structure could also be used on the substrate structure by placing additional layer of conductor inside. A 43% reduction of the module inductance was achieved on a SiC MOSFET module, with 21% increase in the thermal resistance [12]. For 2D structure, there is only one side for cooling. Liquid cooling has been used for lower thermal resistance. Work has been done in this with jet impingement cooling for the 600V/50A SiC JFET module, which enabled the module to operate with 120°C ambient temperature [13]. Also there is work on putting the fluid micro channel inside the ceramic substrate, which has the potential for ultra-low thermal resistance for the shortest thermal path [14]. Few works are done for the GaN

based 2D power module. There is one 270V/56A GaN HEMT power module reported, which is made by paralleling 2A devices [15].

2.2 Planar 2D power package structure

Besides the efforts on optimizing the 2D power package structure, new packaging structures have been proposed for the WBG packaging. Inside a traditional power module, power devices only take small part of the volume. While most of the volume is taken by the passive parts, which means a lot of spacing to be shrunk by removing some parts like wire bonds. A planar 2D power package structure is achieved by substituting the wire bonds with integrated topside for lower inductance connection. By applying planar 2D package structures in the power packaging, more significant enhancement in electrical performance and power density are achieved. A lot of work has been done in this area. Power overlay is introduced by GE in last century showed the capability of 2D package with 1200V IGBT devices [16]. Metal post interconnect and flip chip on flex is made as well for the bondless power module design [17, 18]. IGBT device is thinner to 70 μm and used with Cu-clip on to achieve lower resistance [19]. Semikron introduced SKiN package structure, in which the wire bonds are replaced with sintered two layer flex circuit (with via) for the topside connection of the devices. With this structure low inductive connotation path with high current capability is achieved by having smaller loop and larger contact area than the wire bonds. A 1200V 400A SiC SKiN module presented in 2016 shows a commutation inductance less than 5nH [20].

Researchers at the Oak ridge national lab (ORNL) proposed a new structure named Planar-Bond-All (PBA) package. In which the devices are sandwiched between two DBC substrates. This enables very low inductance in power loop and low thermal resistance [21].

Figure 2.3 Planar bond all package [21]

Another method for achieving planar 2D package is through the embedded component. The active and passive components are placed in the substrate with connection between to form low inductance loop. The concept has already been applied to GaN power device package. The Embedded Component Packaging (ECP) process from AT&S is used in 600V GaN HEMT device from GaN system, which has a very small footprint. Thus the electrical performance is ensured by having low inductance [22]. A hybrid of 2D and planar 2D embedded package is used for SiC JFET power module with the power loop inductance close to the planar structure [23]. Alumina substrate was used as the dielectric to build the embedded power module with 7nH stray inductance [24]. Researchers also made embedded inductor with LTCC process [25].

Figure 2.4 Embedded Planar 2D power module [24]

The main challenge for the embedded planar 2D packaging is the thermal stress management. Compact planar 2D package gets a higher heat flux with component distributed on a large surface, which is a thermal barrier for the development. Regarding the thermal management of the planar 2D structure, double sided cooling is the main stream as it provides multiple thermal path. Early work is done regarding the cooling for the double sided module by directly braze heat sink on the back of the substrate, which doubled the current capability of the IGBT due to the low thermal resistance [26]. Impingement cooling method is also used on a double sided module, which further suppress the thermal resistance with loop inductance as low as 17nH [27]. For the management of the stress on the chip, copper cylinder bump was used as spacer to deal with CTE mismatch occurred on the solder joint [28]. Some works do not use the sandwich structure with substrate on the top of the devices. Instead conductor such as copper clip and heat pipes are used, which serve as electrical connector, as well as heat spreader [29, 30]. There are also planar 2D power modules commercially available in the market with 200°C rating, which is from CREE (now Wolfspeed) [31]. A ceramic-based embedded module is design with the liquid cooling mechanism with 45% to 60% improvement in thermal resistance than single sided cooling [32]. Fraunhofer shows a 650V/600A Si IGBT PCB embedded module design. Copper with 500 μm thickness was used as heat spreader with acceptable thermal resistance. The tested dc link inductance for the module is 2.8nH [33].

2.3 3D power package structure

Meanwhile there is a new trend in power packaging area, namely 3D packaging concept, being developed for achieving higher switching speed and power density. In planar 2D package

structure, power devices are placed in a plane with low inductance connection between them and the terminals. While in 3D package structure, the power devices is no longer limited in one plane, by which the parasitics are further reduced. Early attempt was done by folding the flip chipped flexible circuit into a roll shape to form a 3D structure [34]. 3D structure is also achieved by stacking of the devices. Power chip on chip structure is made by stacking IGBT and diode between copper bus bars with compression [35]. In the power electronics packaging, there is few proposed concept on this. Researchers have used the Si MOSFET to stack in GaN HEMT for building the cascode structure to get a normally off device [36]. Similar work could be done with the quilt packaging concept [37]. Work has been done by direct bonding dies on the metal and vertically connect the pair on the substrate, by which the low switching cell parasitic inductance is achieved [38]. 3D stack is used to silicon interposers to cool processors, with 20W power dissipation at low stack and 0.5 W for 2 memory chips on top [39].

Figure 2.5 (a) Si MOSFET stacked on GaN HEMT [36] (b) vertical power device [38]

Introducing new packaging technologies can be difficult as shown conceptually in figure 2.6. To achieve high densities, either component and spacing need to shrink, or new technology is needed. Close range of 3D reduction in parasitic parameters, smaller foot print for higher power density with similar thermal-mechanical performance. When the size of the module gets

small, all the problem is going to have conflict with each other. The designer cannot introduce new problem when solved one.

Figure 2.6 Cost versus technology based on feature size and resolution [40]

The work proposed in the report is aimed to improve the performance of the power module by utilizing 3-D prismatic packaging concept.

2.4 Reference

- [1] S. Inokuchi et al., "A new high capacity compact power modules for high power EV/HEV inverters," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 468-471.
- [2] A. Fukumoto, D. Berry, K. D. T. Ngo and G. Q. Lu, " Effects of Extreme Temperature Swings (-55°C to 250°C) on Silicon Nitride Active Metal Brazing Substrates," in IEEE Transactions on Device and Materials Reliability, vol. 14, no. 2, pp. 751-756, June 2014.

[3] J. G. Bai, Z. Z. Zhang, J. N. Calata and G. Q. Lu, "Low-Temperature Sintered Nanoscale Silver as a Novel Semiconductor Device-Metallized Substrate Interconnect Material," in IEEE Transactions on Components and Packaging Technologies, vol. 29, no. 3, pp. 589-593, Sept. 2006.

[4] Y. Yao, Z. Chen, G. Q. Lu, D. Boroyevich and K. D. T. Ngo, "Characterization of Encapsulants for High-Voltage High-Temperature Power Electronic Packaging," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 2, no. 4, pp. 539-547, April 2012.

[5] Y. Yao, G. Q. Lu, D. Boroyevich and K. D. T. Ngo, "Survey of High-Temperature Polymeric Encapsulants for Power Electronics Packaging," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 5, no. 2, pp. 168-181, Feb. 2015.

[6] S. Diaham, M. L. Locatelli, R. Khazaka, H. Hourdequin and R. Kumar, "Electrical conduction in parylene HT: transient and steady-state analyses at high temperature," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 22, no. 4, pp. 2329-2338, August 2015.

[7] J. Schuderer, U. Vemulapati and F. Traub, "Packaging SiC power semiconductors — Challenges, technologies and strategies," 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, 2014, pp. 18-23.

[8] K. Hasegawa, K. Wada and I. Omura, "Mutual inductance measurement for power device package using time domain reflectometry," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

- [9] Y. S. Sun and J. C. Driscoll, "A new hybrid power technique utilizing a direct Copper to ceramic bond," in IEEE Transactions on Electron Devices, vol. 23, no. 8, pp. 961-967, Aug 1976.
- [10] S. Kicin et al., "A new concept of a high-current power module allowing paralleling of many SiC devices assembled exploiting conventional packaging technologies," 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 467-470.
- [11] L. Stevanovic et al., "High performance SiC MOSFET module for industrial applications," 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 479-482.
- [12] A. Imakiire et al., "Investigation of prototype SiC power module structure for low inductance and high heat operation," 2017 IEEE International Workshop On Integrated Power Packaging (IWIPP), Delft, 2017, pp. 1-4.
- [13] K. Gould, S. Q. Cai, C. Neft and A. Bhunia, "Liquid Jet Impingement Cooling of a Silicon Carbide Power Conversion Module for Vehicle Applications," in IEEE Transactions on Power Electronics, vol. 30, no. 6, pp. 2975-2984, June 2015.
- [14] Shan Yin, King Jet Tseng, Jiyun Zhao, Design of AlN-based micro-channel heat sink in direct bond copper for power electronics packaging, Applied Thermal Engineering, Volume 52, Issue 1, 2013, Pages 120-129, ISSN 1359-4311,
- [15] S. Cheng and Po-Chien Chou, "Investigation on the parallel operation of All-GaN power module and thermal performance evaluation," 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), Hiroshima, 2014, pp. 3425-3431.

[16] R. Fisher, R. Fillion, J. Burgess and W. Hennessy, "High frequency, low cost, power packaging using thin film power overlay technology," Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual, Dallas, TX, 1995, pp. 12-17 vol.1.

[17] S. Haque et al., "An innovative technique for packaging power electronic building blocks using metal posts interconnected parallel plate structures," in IEEE Transactions on Advanced Packaging, vol. 22, no. 2, pp. 136-144, May 1999.

[18] Xingsheng Liu, S. Haque, Jinggang Wang and Guo-Quan Lu, "Packaging of integrated power electronics modules using flip-chip technology," APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058), New Orleans, LA, 2000, pp. 290-296 vol.1.

[19] H. R. Chang, J. Bu, G. Kong and R. Labayen, "300A 650V 70 um thin IGBTs with double-sided cooling," 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, 2011, pp. 320-323.

[20] T. Stockmeier, P. Beckedahl, C. Göbl and T. Malzer, "SKiN: Double side sintering technology for new packages," 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, 2011, pp. 324-327.

[21] Z. Liang, P. Ning, F. Wang and L. Marlino, "Planar bond all: A new packaging technology for advanced automotive power modules," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 438-443.

[22] “3D Embedded Substrate Technologies Increase Density and Performance of Power Supplies”, Internet: <https://www.slideshare.net/DesignWorldOnline/3d-embedded-substrate-technologies-increase-density-and-performance-of-power-supplies>, [July 10, 2017].

[23] R. Wang, Z. Chen, D. Boroyevich, L. Jiang, Y. Yao and K. Rajashekara, "A Novel Hybrid Packaging Structure for High-Temperature SiC Power Modules," in IEEE Transactions on Industry Applications, vol. 49, no. 4, pp. 1609-1618, July-Aug. 2013.

[24] Zhenxian Liang et al., "Integrated packaging of a 1 kW switching module using a novel planar integration technology," in IEEE Transactions on Power Electronics, vol. 19, no. 1, pp. 242-250, Jan. 2004.

[25] Y. Su, Q. Li and F. C. Lee, "Design and Evaluation of a High-Frequency LTCC Inductor Substrate for a Three-Dimensional Integrated DC/DC Converter," in IEEE Transactions on Power Electronics, vol. 28, no. 9, pp. 4354-4364, Sept. 2013.

[26] C. Gillot, C. Schaeffer, C. Massit and L. Meysenc, "Double-sided cooling for high power IGBT modules using flip chip technology," in IEEE Transactions on Components and Packaging Technologies, vol. 24, no. 4, pp. 698-704, Dec 2001.

[27] C. M. Johnson et al., "Compact Double-Side Liquid-Impingement-Cooled Integrated Power Electronic Module," Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's, Jeju Island, 2007, pp. 53-56.

[28] J. Li, A. Castellazzi, T. Dai, M. Corfield, A. K. Solomon and C. M. Johnson, "Built-in Reliability Design of Highly Integrated Solid-State Power Switches With Metal Bump Interconnects," in IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2587-2600, May 2015.

- [29] T. J. Martens, G. F. Nellis, J. M. Pfotenhauer and T. M. Jahns, "Double-sided IPEM cooling using miniature heat pipes," in IEEE Transactions on Components and Packaging Technologies, vol. 28, no. 4, pp. 852-861, Dec. 2005.
- [30] D. R. M. Woo, H. H. Yuan, J. A. J. Li, L. J. Bum and Z. Hengyun, "Miniaturized Double Side Cooling Packaging for High Power 3 Phase SiC Inverter Module with Junction Temperature over 220°C," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, 2016, pp. 1190-1196.
- [31] Z. Cole, B. McGee, J. Stabach, C. B. O'Neal, and B. Passmore (2015) A High Temperature, High Power Density Package for SiC and GaN Power Devices. Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT): July 2015, Vol. 2015, No. HiTEN, pp. 000208-000213.
- [32] B. C. Charboneau et al., "Double-Sided Liquid Cooling for Power Semiconductor Devices Using Embedded Power Packaging," in IEEE Transactions on Industry Applications, vol. 44, no. 5, pp. 1645-1655, Sept.-Oct. 2008.
- [33] C. Neeb, J. Teichrib, R. W. De Doncker, L. Boettcher and A. Ostmann, "A 50 kW IGBT power module for automotive applications with extremely low DC-link inductance," 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, 2014, pp. 1-10.
- [34] P. Clot, J. F. Zeberli, J. M. Chenuz, F. Ferrando and D. Styblo, "Flip-chip on flex for 3D packaging," Twenty Fourth IEEE/CPMT International Electronics Manufacturing Technology Symposium (Cat. No.99CH36330), Austin, TX, 1999, pp. 36-41.

- [35] E. Vagnon, P. O. Jeannin, J. C. Crebier and Y. Avenas, "A Bus-Bar-Like Power Module Based on Three-Dimensional Power-Chip-on-Chip Hybrid Integration," in *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 2046-2055, Sept.-Oct. 2010.
- [36] W. Zhang et al., "A New Package of High-Voltage Cascode Gallium Nitride Device for Megahertz Operation," in *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1344-1353, Feb. 2016.
- [37] Q. Zheng, D. Kopp, M. A. Khan, P. Fay, A. M. Krizan and G. H. Bernstein, "Investigation of Quilt Packaging Interchip Interconnect With Solder Paste," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 3, pp. 400-407, March 2014.
- [38] B. Letowski et al., "Towards vertical power device 3D packaging on 8-inch wafer," 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 135-138.
- [39] N. Khan et al., "Development of 3-D Stack Package Using Silicon Interposer for High-Power Application," in *IEEE Transactions on Advanced Packaging*, vol. 31, no. 1, pp. 44-50, Feb. 2008.
- [40] J. B. Jacobsen and D. C. Hopkins, "Optimally Selecting Packaging Technologies and Circuit Partitions based on Cost and Performance," *Applied Power Electronics Conference*, New Orleans, LA, February 6-10, 2000. Plenary Session Paper

Chapter 3 The 3D Power Path Concept

3.1 Introduction

The WBG semiconductor device offers high speed switching, which enables high frequency operation of converters. However, under hard switching, for example during, turning off, there is a voltage overshoot (ΔV) caused by the module stray inductance (L_s) and current change (di/dt), i.e.

$$\Delta V = L_s \frac{di}{dt} \quad (3.1)$$

Since the voltage overshoot limits the range of device and module operation, having as small an oscillation as possible is desired. Decreasing the switching speed may reduce the oscillation, while the dynamic loss increases, but this reduces the benefit of using a WBG power device. Therefore, a preferred solution is to reduce parasitic inductance inside the module, as shown by many researchers [1], [2]. In this chapter the source of power loop inductance in 2D planar packages is discussed, then reduction with 3D prismatic structure is quantified.

3.2 Power Pathways in 2D and 3D Power Modules

3.2.1 Electrical Current Path in 2D

In a traditional Si-based power module, these devices are attached onto the DBC substrate by soldering to form “back-side” electrical (and thermal) connections. Wire bonds of Al or Cu wires connect the topside metallization of the device to other Cu traces on the DBC substrate to form the electrical switching pathway. Such structures have large stray inductance ($\sim 50\text{nH}$)

[3], mainly caused by bonding wires and length of the Cu-trace pathway. New packaging structures designed for WBG power devices, need lower stray inductance to realize the higher performance capabilities of the devices.

To provide a simple, but directly scalable, structure for discussion, a half bridge (or phase-leg) circuit is selected as in Fig. 3.1(a), which contains two switches and two diodes. The current flows through the upper and lower switches in the phase leg during the commutation transient when the lower device turning off. The stray inductance along the current path induces the voltage overshoot. To focus on the analysis of the stray inductance. The schematic is further simplified as Fig. 3.2(b), in which each pair of devices are simplified as a single switch. Since for each pair of devices, the distance between diode and switch are close. The parasitic inductance inside the pair is much smaller than the inductance along the current path inside the module. Also, there is a trend for merging switch and diode into a single device [4], which would eliminate the inductance inside the pair.

Figure 3.1 (a) Schematic of half bridge circuit. (b) Simplified schematic of half bridge circuit

The parasitic inductances within the circuit path is shown in Fig. 3.2, where L_1 , L_2 , L_3 , and L_4 represent the inductances between the switches and terminals, which are from the terminals, bonding wires, and traces inside the module. A commutation current occurs during turn off period of the lower switch, which conduct through the circuit and induces a voltage spike (ΔV) along the path, and can be calculated through (3.1). A simple inductor matrix can be formed of the series inductances along the pathway, as shown in (3.2), and the resulting voltages from the changing currents can be represented as in (3.3) and (3.4). However, this does not include any mutual inductance as would be found in a physical module.

Figure 3.2 Commutation current in the circuit.

$$L = \begin{bmatrix} L_1 & & & \\ & L_2 & & \\ & & L_3 & \\ & & & L_4 \end{bmatrix} \quad (3.2)$$

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & & & \\ & L_2 & & \\ & & L_3 & \\ & & & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} L_1 \frac{di}{dt} \\ L_2 \frac{di}{dt} \\ L_3 \frac{di}{dt} \\ L_4 \frac{di}{dt} \end{bmatrix} \quad (3.3)$$

$$\Delta V = v_1 + v_2 + v_3 + v_4 = (L_1 + L_2 + L_3 + L_4) \frac{di}{dt} \quad (3.4)$$

Options exist in packaging to reduce the inductances, thus reducing the overshoot voltages. For example, a more compact power module has shorter Cu-trace pathways on the DBC substrate giving less trace inductance. Unfortunately, module manufacturers tend to use a certain “Package Outline” and “Footprint” regardless how semiconductor die size might change within a range, which does not create the lowest inductance package. Shorter wire bonds, lower bonding profile, and ribbon bonds can provide lower wire inductance. Further reduction in inductance of the flexible welded interconnect approach would use wire-bondless modules, like Power Overlay (POL), that eliminates the wire bond [5] in 2D planar packaging, or Power Chip on Bus (PCoB) [6].

Another approach to reducing the package inductance is to introduce mutual inductance cancellation into the design, which is not available to simple single layer 2D planar structures. The cancellation of inductance is achieved by placing the returning current path close to the sourcing current path. Hitachi utilized the mutual inductance between the positive and negative terminals in their power module. By this method the internal stray inductance could be reduced to as low as 10nH [7].

To develop this, the mutual inductance of two parallel wires, Fig. 3.3, of length l and distance d with current running through can be described in (3.5) [8]:

Figure 3.3 Two parallel wires

$$M = \frac{\mu_0}{2\pi} \left[l \log \frac{l + \sqrt{l^2 + d^2}}{d} - \sqrt{l^2 + d^2} + d \right] \quad (3.5)$$

When l is greater than the distance d , it can be written as (3.6). The mutual inductance will be greater as the distance gets shorter, which means the coupling effect of two wires are stronger, too.

$$M = \frac{\mu_0}{2\pi} l \left[\log \frac{2l}{d} - 1 + \frac{l}{d} \right] \quad (3.6)$$

For the half bridge circuit, the suppression of stray inductance is done by placing two current paths (Positive to Output & Output to Negative) close to each other. There are mutual inductances between L_1 & L_4 / L_2 & L_3 , due to the coupling effect.

Figure 3.4 Half bridge circuit parasitic inductance with mutual inductance

The inductor matrix is updated with the mutual inductance M_{14} , M_{41} , M_{23} , and M_{32} . The "-" sign represents the suppression for the total inductance due to an opposing direction of current. The influence between L_1 & L_3 is neglected because the spacing between them is large (copper trace distance is much smaller than the length of the switching devices).

$$L = \begin{bmatrix} L_1 & & & -M_{14} \\ & L_2 & -M_{23} & \\ & -M_{32} & L_3 & \\ -M_{41} & & & L_4 \end{bmatrix} \quad (3.7)$$

Substituting (3.7) into (3.1) yields (3.8). The total increase in voltage is then shown in (3.9)

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & & & -M_{14} \\ & L_2 & -M_{23} & \\ & -M_{32} & L_3 & \\ -M_{41} & & & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} (L_1 - M_{14}) \frac{di}{dt} \\ (L_2 - M_{23}) \frac{di}{dt} \\ (L_3 - M_{32}) \frac{di}{dt} \\ (L_4 - M_{41}) \frac{di}{dt} \end{bmatrix} \quad (3.8)$$

$$\begin{aligned} \Delta V &= v_1 + v_2 + v_3 + v_4 \\ &= (L_1 - M_{14}) \frac{di}{dt} + (L_2 - M_{23}) \frac{di}{dt} + (L_3 - M_{32}) \frac{di}{dt} + (L_4 - M_{41}) \frac{di}{dt} \\ &= (L_1 + L_2 + L_3 + L_4) \frac{di}{dt} - 2(M_{14} + M_{23}) \frac{di}{dt} \end{aligned} \quad (3.9)$$

As (3.9) shows, a decrease in voltage occurs by using a mutual inductance cancellation. This method is used for reducing inductance in 2D-planar, e.g. in SiC MOSFET power modules in [9], by paralleling the upper and lower phases inside a module.

3.2.2 Electrical Current Path in Planar 2D

On a planar 2D planar module layout some cancellation is achieved by alternating the copper traces (on the DBC substrate) as shown in Fig. 3.5(a), and is modeled in Fig. 3.5(b).

(a)

(b)

Figure 3.5 (a) Internal layout of Rohm BSM120D12P2C005 [10] (b) Current path in horizontal plane.

Unlike the method above which keeps the devices and interconnect planes on the same level, another approach keeps devices on the same plane, but sandwiches the devices between two large Cu planes. The high-side MOSFET sits next to but upside down to the low-side MOSFET, as graphically shown in Fig. 3.6(a), with the electrical schematic shown in Fig. 3.6(b). This “Planar-Bond-All” structure from ORNL has a low stray inductance of less than 10nH [11], and will be used to best compare a planar 2D approach to the 3D approach developed in this research.

(a)

(b)

Figure 3.6 (a) Current path in vertical plane. (b) 3D Planar-bond-all module [11]

3.2.3 Electrical Current Path in 3D

The question posed for research, is if one would want to approach further mutual inductance cancellation in the physical topology interconnecting the semiconductor die (which are thin, flat, square or rectangular, crystalline plate objects), but not use 2D planar packaging structures, then is there and to what extent can one use true 3D placement of the semiconductors in a packaging structure? That is to say, structures where the components and interconnects are on orthogonal planes.

A 3D current path for a half bridge schematic is shown in Fig. 3.7(a), where switch pairs (S_1 and S_2) are placed next to each other on a plane. Each current path from devices to terminals

is closely coupled to get enough field cancellation effect. The current direction and mutual inductance is shown in Fig. 3.7(b).

Figure 3.7 (a) Current path in 3D. (b) Mutual inductance seen from L_1

By placing the current path “close”, each current on each conducting path has mutual inductances with the others. The current on path 1 (L_1) has mutual inductance M_{12} , M_{13} , and M_{14} . Since currents on L_2 and L_4 have different current direction, there is a “negative” mutual inductance, meaning cancellation effect. While the current on L_3 has the same current direction, there is a “positive” on the mutual inductance, meaning enhancement effect. The inductor matrix is updated as (3.9)

$$L = \begin{bmatrix} L_1 & -M_{12} & M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix} \quad (3.9)$$

Substituting (3.9) into (3.1) yields (3.10). The total increase in voltage is then shown in (3.11). From (3.5), it is derived that M_{13} is smaller than M_{12} , since the distance between L_1 and L_3 is greater than that between L_1 and L_2 (also for M_{34} and M_{24}). This means an additional

reduction of stray inductance is in the loop, and would further decrease the voltage difference.

Thus, theoretically 3D is an option for lowering the inductance of a half bridge WBG module.

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_1 & -M_{12} & M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix} \begin{bmatrix} \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \\ \frac{di}{dt} \end{bmatrix} = \begin{bmatrix} (L_1 - M_{14}) \frac{di}{dt} - (M_{12} - M_{13}) \frac{di}{dt} \\ (L_2 - M_{23}) \frac{di}{dt} - (M_{21} - M_{24}) \frac{di}{dt} \\ (L_3 - M_{32}) \frac{di}{dt} - (M_{34} - M_{31}) \frac{di}{dt} \\ (L_4 - M_{41}) \frac{di}{dt} - (M_{43} - M_{42}) \frac{di}{dt} \end{bmatrix} \quad (3.10)$$

$$\begin{aligned} \Delta V &= v_1 + v_2 + v_3 + v_4 \\ &= (L_1 - M_{14}) \frac{di}{dt} - (M_{12} - M_{13}) \frac{di}{dt} + (L_2 - M_{23}) \frac{di}{dt} - (M_{21} - M_{24}) \frac{di}{dt} + \\ &\quad (L_3 - M_{32}) \frac{di}{dt} - (M_{34} - M_{31}) \frac{di}{dt} + (L_4 - M_{41}) \frac{di}{dt} - (M_{43} - M_{42}) \frac{di}{dt} \\ &= \left[(L_1 + L_2 + L_3 + L_4) \frac{di}{dt} - 2(M_{14} + M_{23}) \frac{di}{dt} \right] \\ &\quad - \left[2(M_{12} - M_{13}) \frac{di}{dt} + 2(M_{43} - M_{42}) \frac{di}{dt} \right] \end{aligned} \quad (3.11)$$

Simulation validation is carried out in Ansoft Q3D Extractor for comparing the stray inductance between 2D and 3D structure. Copper traces with cross section of 12mil (0.3mm) thickness by 15 mm width is chosen to represent the current path in a power module, which includes the DBC traces, wire bonds, and power devices. A 10 mm spacing is chosen considering the voltage blocking requirement. This spacing could be further shrunk to get more mutual inductance. For the 2D module, the layout of the conducting trace is drawn based on existing power module design, The regions for high and low side devices are shown in Fig 3.8(a), with the current returning point 60mm away from the input (positive/negative) terminals. The output terminal is placed 30 mm away (90 mm away from the input). For the 3D power path,

the output terminal is brought to the input terminal side, with $2mm$ spacing between the conductors.

Figure 3.8 (a) Current path pattern in 2D. (b) Current path pattern in 3D

The parasitic inductance between positive and negative terminal is extracted at $1MHz$. The result for 2D power path is $41.2nH$, while the 3D power path gives $28.3nH$ stray inductance. Thus, the further reduction of the stray inductance via 3D power path is proved.

To utilize the 3D power path concept in a packaging design, a basic 3-phase full bridge circuit, which is widely used in motor drive units, is chosen. Figure 3.9(a) is the schematic of the circuit, together with a top view of the actual layout in a power module, as shown in Fig. 3.9(b) [12].

A 3-phase full bridge consists of three paralleled half-bridge schematics. There are 6 switches (MOSFET, JFET, IGBT etc.) and 6 anti-parallel diodes. These devices are in the same plane. While interconnects are in a parallel, but displaced plane. The drawback is the long current path for connecting each phase which brings additional parasitic inductances.

(a)

(b)

Figure 3.9 (a) Schematic of 3-phase full bridge circuit. (b) Layout of 3-phase full bridge module [12]

Also, it is important to consider the cooling, which is in series and will result in uneven temperature distribution along the cooling direction that is shown in Fig. 3.10 (a). The devices near the outlet will operate at higher temperatures than near the inlet, and determines the thermal management limitations. Parallel cooling (Fig. 3.10(b)) is a better option. An example single-switch module by GE utilized such a cooling concept (Fig. 3.11).

(a)

(b)

Figure 3.10 Parallel placed 3D structure on (a) series cooling plane and (b) parallel cooling plane

Inside the module the devices are packaged in the POL structure and attached to a cooling baseplate inside. This type of structure has the benefit of lower inductance and good thermal performance [13].

Figure 3.11 Coaxial power module [13]

The physical schematic of new 3D three-phase full-bridge power module proposed in the research reported here is shown in Fig. 3.12(a). Switch Pairs (e.g. MOSFET and diode) are placed vertically on the sidewall, sandwiched between the inner structure and outside conductive planes (e.g. DBC substrates). The positive and negative ports are placed in the center part of the module, with three phase outputs surrounding the outside (Fig. 3.12(b)).

The switch pairs are mounted on the substrate, which is being placed vertically around the inner terminals (positive and negative). The switch pair on the high side is flip chipped onto the output plane. The inner terminals are attached to the bottom substrate (not shown in the figure) and connected to the busbar or PCB at the top. The gap between the center terminals is for voltage isolation, which could be realized by encapsulation materials or ceramic. To further reduce the inductance, the inner structure could be built as a coaxial structure as Fig. 3.12(b).

(a)

(b)

(c)

(d)

Figure 3.12 (a) Terminal assignments of the module. (b) Proposed 3 phase full bridge structure. (c) Schematic showing the parallel cooling. (d) Current path for each phase.

In the three-phase bridge module, each phase is placed in a 120 degree sector area. Each conductive plane (substrate) has individual cooling for thermal dissipation as Fig. 3.12(c)

shows. 3D power path was used in each section. The parasitic inductance along a single phase is shown in Fig. 3.12 (d). As discussed in previous part, such arrangement will utilize the mutual inductance cancellation for each phase's stray inductance. The influence between each phase is also reduced. Since the current directions (on the inner terminals) between two phases are opposite. More topologies could be achieved through such a prismatic structure with a 3D power path concept in the future.

Regarding the influence of the device size on the module volume. As shown in Fig. 3.12, the foot print area of the power module is determined by the width of the sidewall DBC substrates, which are limited by the thyristor and diode mounted on. Apparently the volume of the module will be bigger as the single device size getting larger for higher current rating. To determine the critical impact fact for module volume versus chip dimension, a quick evaluation is carried out. Assuming the dimeson of thyristor and diode to be the same with a width of w and length of l . The sidewall dimension is set to be 2 times of the device width and 4 times of the device length, in average. The devices are mounted vertically along the sidewall (with width side horizontally). The volume of the three phase prismatic module is then expressed as (3.12).

$$Volume = Area \times height = \left(\frac{3\sqrt{3}}{2} \times (2w)^2 \right) \times (2 \times 2l) \quad (3.12)$$

According to (3.12), the volume of the module versus chip dimension is plotted with power devices area ranging from 25mm^2 to 225mm^2 , as Fig. 3.13 shows.

Figure 3.13 Volume versus chip dimensions for three phase prismatic module

The volume of the module increase as the chip size gets larger, in which the width of the device (horizontal side) plays more important role on enlarging the volume. Thus for a 3 phase prismatic power module, mounting the devices with its long side vertical is preferred when a smaller volume is desired. In some situation when a single device cannot meet the need of current capability, paralleling multiple devices is a solution. On the sidewall DBC substrates, the devices could be placed in two directions: vertical and horizontal. Vertical placement is preferred for its low impact on module size increase. But in some case there is limitation to the height. Also when considering the dynamic current sharing between the devices, horizontally placed devices is better for its uniformity in parasitics. There should be a tradeoff when designing such module with paralleled devices. More work could be done in this area in the future.

3.3 Summary

This chapter discusses the parasitic inductance influence on a power module and methods to suppress the voltage overshoot. The present methods, based on mutual inductance cancellation, are summarized regarding the current flow path. The structure with a current path on the horizontal plane has limited mutual inductance cancellation due to the spacing between the conductors. The structure with a current path through interconnects placed on a parallel plane, but physically displaced, has a mutual inductance cancellation effect. However, a 3D prismatic structure is proposed for a three-phase full-bridge module, utilizing orthogonal component placement that has the lowest inductance design.

3.4 Reference

[1] R. Letor, "Static and dynamic behavior of paralleled IGBTs," in *IEEE Transactions on Industry Applications*, vol. 28, no. 2, pp. 395-402, Mar/Apr 1992.

doi: 10.1109/28.126748

[2] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "P-cell and N-cell based IGBT module: Layout design, parasitic extraction, and experimental verification, " in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2011, pp. 372–378.

[3] Z. Liang, "Planar-bond-all: A technology for three-dimensional integration of multiple packaging functions into advanced power modules," *2015 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, Chicago, IL, 2015, pp. 115-118.

[4] W. Sung and B. J. Baliga, "Monolithically Integrated 4H-SiC MOSFET and JBS Diode (JBSFET) Using a Single Ohmic/Schottky Process Scheme," in *IEEE Electron Device Letters*, vol. 37, no. 12, pp. 1605-1608, Dec. 2016.

[5] Fisher, R.; Fillion, R.; Burgess, J.; Hennessy, W. High frequency, low cost, power packaging using thin film power overlay technology. In *Proceedings of the Applied Power Electronics Conference and Exposition*, Dallas, TX, USA, 5–9 March 1995; pp. 12–17.

[6] XU, YANG. "Development of Advanced SiC Power Modules," PhD thesis, URI: <http://www.lib.ncsu.edu/resolver/1840.20/34547>

[7] D. Kawase, M. Inaba, K. Horiuchi and K. Saito, "High voltage module with low internal inductance for next chip generation - next High Power Density Dual (nHPD2)," *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2015, pp. 1-7.

[8] E. B. Rosa, "The self and mutual inductances of linear conductors, " *Bull. Bur. Standards*, vol. 4, no. 2, pp. 301–344, 1908.

[9] A. Imakiire et al., "Investigation of prototype SiC power module structure for low inductance and high heat operation," *2017 IEEE International Workshop On Integrated Power Packaging (IWIPP)*, Delft, 2017, pp. 1-4.

[10] S. Tiwari, O. M. Midtgård and T. M. Undeland, "Experimental performance evaluation of two commercially available, 1.2 kV half-bridge SiC MOSFET modules," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 1106-1111.

[11] Fei Yang, Z. Liang, Zhiqiang Wang and F. Wang, "Parasitic inductance extraction and verification for 3D Planar Bond All Module," 2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), Raleigh, NC, 2016, pp. 1-11.

[12] <http://www.powerguru.org/wordpress/wp-content/uploads/2012/12/Large-DBC-substrate.jpg>

[13] Eladio Clemente Delgado, "Coaxial power module." U.S. Patent 8487416 B2, issued July 16, 2013

Chapter 4 Additive Manufacturing Processes for Power Packaging

4.1 Introduction

The term 3D printing, or Additive Manufacturing (AM), refers to a process of building objects by adding layer upon layer of material at selected locations. Since the 1980s, multiple AM processes have been developed, and include stereolithography (SLA), selective laser sintering (SLS), inkjet printing, fused deposition modeling (FDM), laminated object manufacturing (FOM), ink-based direct writing (nozzle dispensing/aerosol jet), laser transfer direct writing, beam deposition (electron beam/focused ion beam) and so on [1]. By utilizing AM processing, highly complex parts and assemblies can be fabricated often in a significantly shorter time than through traditional processes. The AM technology is also being used in areas requiring high reliability, such as aerospace, automotive, and medical, and may provide opportunities to provide increased reliability in the “low volume” power electronics area.

The approach of 3D prismatic power packaging calls for a diversity of materials to create relatively complex three-dimensional (3D) structures within a small footprint. This fits well with AM for building functional and true-3D components and assemblies. Most electrical designs are based on 2D signal propagation limited in the x-y directions. In the microelectronics industry, where very high speed signal transmission is needed, 2D, Stacked-2D and Embedded-2D circuits and structures are used. If an orthogonal or out-of-plane 3D path is applied in the packaging, similar to processes as described in Chapter 3, the signal could have a much

shortened path. This same approach is applied to power modules for application to high switching speeds of Wide Band Gap devices.

Improvement could also be found in thermal and mechanical aspects by using AM produced 3D prismatic parts. For the thermal issues, stacked-2D, and embedded-2D approaches use essentially a layering of planar circuits or materials [2], with each layer adding an additional thermal resistance, thereby increasing temperature or limiting power or performance. The 3D structures can provide shorter paths, or intricate heat-sink structures, to improve the heat transfer efficiency. A printed structure can also provide graded or flexible mechanical interfaces, and hence, allow stress management for increased reliability.

In this chapter, an investigation of known state of art AM processes applicable to power module packaging is provided. Also, included is a short description of an early module fabrication and design of an ‘Intelligent Power Module’ using 3D printing techniques for the housing and embedding of a gate drive circuit. The design, mimicking a Vincor DC/DC micro-family converter, provides a vehicle for thorough exploration of application of 3D printing to traditional modules. The full design of the IPM is provided in the Appendix A. Key findings and contributions are outlined below.

4.2 Evaluation of AM Processes for Power Packaging

A typical power module, shown in Fig. 1.1 in Chapter 1, consists of a power semiconductor chip, baseplate, metal clad ceramic substrate, terminals, housing, bonding wires, and encapsulation. Each element could be discussed for the feasibility of using AM, including, design for manufacturability, reliability, cost, and variations in material and interfaces. However, most

of these topics are beyond the scope of this research. Therefore, only key points are selected and discussed.

Potential materials are divided into two electrical functions as electrically conductive or electrically isolating. Since the 3D printing processes do not deal with power semiconductor material, direct semiconductor printing is not considered. Insulators, such as housing and encapsulation, provide mechanical protection, voltage isolation, or thermal conduction. Electrically conductive parts, such as bonding wires and conductive traces, serve as a bridge between the power devices, and components, and next level terminals.

4.2.1 Polymer-Based AM Processes for Isolations in Power Packaging

The needed electrically isolating parts inside the module are encapsulation, mechanical housing, and substrates. Encapsulation (silicone gel/Epoxy Resin) fills the spacing between conductors and housing for voltage isolation and stress management. Some AM processes, such as FDM, can be used during the dispensing process. The housing provides the module with its overall strength, electrical and environmental isolation, and mechanical integrity, as well as containing all of the inner electronic components. There is a wide option in AM material for creating housings, which will be discussed in this chapter. A ceramic material (Al_2O_3 , AlN ...) beneath the power chips is used for voltage isolation and thermal conduction. Ceramic AM processes, such as laser sintered ceramic, are under development but years away for commercial application to meet the needs of a power electronic substrate [3]. Still, some work done in printing metal on ceramic shows the potential of using AM in making metal-cladded substrates, which will be introduced later in the chapter.

Polymer-based AM material, such as ABS, PLA, and UV-cured resin, are widely used in consumer and light commercial 3D printing. Based on these mature materials, researchers utilize the printed polymer parts as substrates and make electrically functional circuits. Also, 3D direct writing is used, which is one of the lowest cost methods for building a complex circuit [4]. Researchers in the UK have thoroughly summarized the technologies of such processes; some example applications are shown as Fig. 4.1. Their conclusion is that additive manufacturing is a progressive and effective “micro fabrication” technology for achieving 3D structures, but the process needs more enhancement [5]

Figure 4.1 AM parts in microelectronics [5]

Their cited processes are relatively applicable to insulation and isolation processes for power electronic. Unfortunately, the processes are very limited for power packaging due to the lack of high current carrying capacity. One approach that has some applicability uses a 3D direct write conductive material albeit with a high resistance compared with the bulk metal conductor (i.e. Cu). For example, a cured silver ink from Electroninks has a conductivity of $6 \sim 8 \times 10^{-6} \Omega \cdot \text{cm}$ (4~5 times of Cu) and 1.5 ~ 2 micron thickness (1/100 times of 8mil Cu). The resistance of the printed Ag trace is 400~500 times higher than an 8mil Cu trace with same length. The Ag wire can only carry 0.1A current, while a traditional Cu trace can carry 40A for the same power loss. So the direct write process is not recommended for printing traces

that carry “high” current from the power chip to the terminals. However, this 3D direct write process may be used for low power embedded control and gate-drive circuit. Such processes might also be used to embed the drives and controls within a housing.

The selection of AM processes and materials, based on ready availability non-custom formulations (at the time of this investigation, circa 2015), were evaluated for potential use as either an electrical conductor or dielectric at the temperatures needed by power modules. Traditional power module housings, which provide environmental protection for the device during operation, are typically fabricated with materials, such as thermoset allyls/epoxy, Diallyl Phthalate (DAP), thermoplastic polyester, and Polybutylene terephthalates (PBT). These materials provide the housing with overall mechanical strength, electrical isolation, and sufficient thermal conductivity. Therefore, tensile strength, Young’s modulus, electrical and thermal conductivity, and the coefficient of thermal expansion are the criteria when bringing in AM technology to the housing fabrication process. In Fig 4.2, a comparison of AM materials and traditional housing material was compiled from online technical data comparing tensile strength and heat deflection temperature for commercial AM materials versus traditional housing materials. The tensile strength vs heat deflection temperature is measured following ASTM D-638 and ASTM D-648 standards.

From Fig. 4.2 it can be concluded that most of the AM materials stay between DAP and PBT type materials when considering the heat deflection temperature. Two SLA materials show better temperature withstand capability than epoxy. These materials could be potentially useful in high temperature power electronics packaging. For the tensile strength, most AM materials are close to DAP/PBT; yet none of these exceed the tensile strength of the more

commonly used epoxy, which is cured by chemical reaction and has not yet been investigated for use in 3D printers.

Figure 4.2 Comparison of AM materials and traditional housing materials

4.2.2 Evaluation of Printing Resolution Requirements

The printing resolutions for different methods are evaluated. In this research an “intelligent power module (IPM) is also considered in evaluating 3D printing approaches. The IPM is a module that hosts both the power semiconductors and a gate drive circuit and some controls. The smallest parts that defines the finest features and printing requirements are in the gate-driver circuits. (Though, those features are generally considered large features compared to

processes used in the microelectronics industry). Evaluation results of resolutions and feature sizes are given in Table 4.1 for the selected methods.

Table 4.1 Comparison of Polymer AM Methods

AM METHODS	LAYER THICKNESS (mm)	RESOLUTION (mm)	COST
Fuse Deposition Modeling (Makerbot)	0.10	0.40	Low
Stereolithography (3D system)	0.05	0.25	High
Selective Laser Sintering (3D system)	0.08	0.76	High
Inkjet 3D Printing	Varies by system	Varies by system	Depends on ma- terial
Laminated Object Manufacturing (SD300)	0.16	1.00	Low

To provide context for the above table as applied to Power Packaging, the IPM given in Appendix A shows the smallest component in the control circuit design is a 0805 (80mil x 50mil, 2.3mm x 1.27mm) surface mount resistor. The smallest geometry is the lead pitch of the gate drive chip (0.85mm). To mount the component in the printed lid, the resolution and layer thickness should be smaller than the component geometry. As discussed in [6], FDM methods do not provide a surface with desirable smoothness. The rough textures on the surface

make it difficult to dispense conductor traces and place components. A now-common process to smooth the surface uses an alcohol (e.g. acetone) solution as a surface treatment that dissolves and smooths the surfaces; though diminishes some fine printed features.

An alternative to the FDM process is the SLS process, which has the capability to achieve the accuracy needed for placing small 0805 components. However, the cost is higher when compared to a similar housing printed by FDM or SLA methods, where the cost of the latter is 10 times lower. The LOM process uses a binder between printed layers, which affects the thermal stability and water absorption of the housing material making it not suitable for power packaging. Based on these drawbacks, SLA and 3D direct write methods are the preferred choice to produce AM housings.

Appendix A provides the design specifics of the IPM. However, a short summary is given below. The 3D printed power module housing was created with a Stratsys Objet350 Connex 3D printer using VeroClear-RGD810 and TangoPlus FLX930. The housing contains a gate driver circuit printed into the housing lid. The entire IPM and electrical performance are shown in Fig. 4.3.

(a)

(b)

Figure 4.3 (a) Module Lid with Housing and (b) Electrical Test Waveform

New designs, layouts, and structures can easily be produced making way for true 3D power modules that could include orthogonal components and structures. The work performed focused on rapid prototyping of power electronic modules that have similar net shaping and terminations as found in other high volume commercial products.

4.2.3 Evaluation of Printing Costs

A cost analysis of the IPM is enlightening to determine a break point when prototyping versus small volume manufacturing should be considered. The analysis followed the projected costs as anticipated by the Center for Additive Manufacturing and Logistics (CAMAL) at NC State. In regards to cost efficiency, the Objet material is not well suited for mass production due to its high cost (at the time of this investigation, circa 2015). The production of the housing body and lid cost is approximately \$200. The material portion of the cost was responsible for less than ten percent of the overall housing production cost. The majority of the cost is due to the machine time, as Fig. 4.4 shows. This machine cost is primarily composed of the maintenance contract and replacement cost.

Figure 4.4 Cost Comparison for Object 350 in Low Volume Situation

For a prototype of the module housing, another acceptable process is FDM. Thanks to the maturity of the FDM process, the total cost is low ($\sim 1/10$ of Objet) for small prototype quantities.

Considering the poor resolution of the FDM process, it is recommended for designs with large tolerances. The main drawback to the FDM process is the lack of heat resistance of commercially available ABS and PLA material. For housing material, the maximum working temperatures depend on application, and range from $+105^{\circ}\text{C}$ to $+175^{\circ}\text{C}$. A future focus will be $+250^{\circ}\text{C}$ to accommodate new wide bandgap power semiconductors, such as GaN and SiC. Recently developed FDM Polyether ether ketone (PEEK) material fits this range with greater than 300°C melting temperature, Fig. 4.5. At the time of this publication the PREES Laboratory and CAMAL center at NC State jointly took position of a PEEK printer and is still under commissioning.

(a)

(b)

Figure 4.5 (a) AM Housing with FDM ABS (b) AM Housing with FDM PEEK

New AM materials with more desirable properties, such as low water absorption, high chemical resistance, high dielectric strength, good flame retardance, and most importantly, low

economic cost, are needed if AM materials are going to become commonly used in harsh environments, like those found in and around power packages. Unfortunately, most AM material attributes for electrical applications are not given nor tested. On the other hand, material properties of thermoset plastics prove they are worthy of being used as AM material for power packaging applications due to their similar performance with the DAP/PBT material. Based on the work done here for investigating present AM material and processes, it is known that direct printing an entire power module is unrealistic, since the materials and processes are not yet available.

For WBG power module, one challenge in the design is the selection of encapsulation material. Since the WBG semiconductors can operate at temperature up to 600 °C [7]. The temperature in the encapsulation would be close to the device temperature for the heating sources is placed all around. It also need to have high dielectric strength due to the close distance between the conductors. That means the material should ensure its high dielectric strength at high temperature. Meanwhile the inner post inside the module is designed to absorb the thermal stress. The encapsulation material with, preferably, soft property is needed for not constraining the movement of the beams. After comparing different materials, a high temperature silicone gel, Wacker 915HT is selected as the encapsulation material. A test module is made to evaluate the material.

The module is designed with 10kV voltage blocking capability. Alumina DBC substrate with 12/40/12mil thickness from STELLAR industries, is selected for voltage isolation (with 50% margin). Two small DBC mechanical dies were attached to the DBC substrates with Sn10Pb88Ag2 solder. The mechanical dies were 40mil Alumina with 12 mil copper on each

side. 12 mil Al wire is bonded on the topside of the mechanical dies. Thermistor is mounted on another DBC isle for temperature measurement. The test package with two ceramic mechanical dies is shown in Fig. 4.6. In this module, the encapsulation process is accomplished in the high temperature mold instead of housing fabricated by 3D printed PEEK.

Figure 4.6 Test module for high temperature encapsulation

Figure 4.7 Leakage current at different temperatures

15kV power supply is connected to the terminals through banana plugs to a current measuring unit (KEITHLEY 238) which connects to the ground. The module is placed on a hot

plate to be heated to different temperatures. When the reading from the thermistor is steady for 5 minutes, a voltage sweep from 0 to 12kV is applied between the terminals. The testing results are exhibited in Fig. 4.7, showing a 10nA leakage current at 12 kV when the module temperature is 225°C. Thus this material is suitable for providing high temperature encapsulation to the prismatic module.

4.2.4 Metal-Based AM Process for Power Packaging

Metal-Based AM material, such as titanium alloy, copper alloy, and stainless steel, are widely accepted in applications like aerospace structures and medical implants, regardless of its high cost. The 3D printing process provides structure with lower weight, at a similar or better mechanical performance, by utilizing optimized 3D shapes. By utilizing different 3D structures, such as a lattice, string, or column, desired mechanical performance can be tuned for different applications. This attribute provides an attractive option to solve the thermal stress problems within the power electronic module. Researchers from Germany used Selective Laser Melting (SLM) process to print Al columns on the pad of an IGBT device for thermal stress management [8]. One early investigation undertaken in this dissertation was printing copper as an interconnection and stress management. (Disclosures filed). Experiments were done for building up copper posts on a DBC substrate by an electron beam (E-beam) process. The result is shown in Fig. 4.8(a). Copper patterns with 3mm height, 2mm spacing, and feature size ≤ 750 microns, were formed on a double-sided Direct Bonded Copper (DBC) substrate. A similar aluminum structure was printed on alumina ceramic, shown in Fig. 4.8(b). A critical challenge to the fabrication was stress management within the ceramic by controlling the time rate of

change of the thermal gradient within the structure. The pattern is representative of a Vivaldi antenna array used in RF systems.

Figure 4.8 (a) Printed copper posts on DBC substrate by E-beam method [9] (b) Printed Aluminum on Alumina Ceramic

The results demonstrate the possibility of a printed metal on ceramic system for more complex interconnections or intricate structures. Further work will optimize the printing process and electrically characterize the printed metal patterning for power packaging. Early work was done in this area with printed copper on ceramic [10]. Little work has been done in hybrid printing of metal and ceramic. The possible reason could be the melting temperature difference between ceramic and metal. One of the possible solutions for this could be a combination of indirect 3D printing process with Low Temperature Co-fire Ceramic (LTCC) process. The 3D printing process could be used for dispensing a green ceramic with a metal ink. Then the entire piece is post-sintered to get the final structure.

Another area that adopted metal AM is for thermal management, which need thermally conductive structures such as heat sinks with complex liquid channels. A topology optimization based on a numerical top-down method created a heatsink design that an AM process would build. Test results showed better performance for 3D optimized heat sink [11].

The metal-based AM techniques could also be used to print interconnects within the module. A list of metals to consider in AM for power electronics is contained in Table 4.2. For power electronics modules, the metal inside is mainly for current conduction. There is little mechanical or thermal concerns for these metals, which is the function that a 3D structure best addresses. As it's been discussed in the previous chapter, the mutual inductance cancelation effect could be beneficial to the electrical performance of future WBG power electronic module. A 3D power path, which is physically built with interleaved metal and ceramic in an RF strip line approach may be essential to realize the highest performance power modules.

Table 4.2 Comparison of Metal AM Methods

AM METHODS	LAYER THICKNESS (mm)	RESOLUTION (mm)	COST
Selective Laser sintering (EOSINT M 280)	0.02	$\pm 0.02 - 0.05$	High
E-Beam (Arcam A2)	0.13	± 0.2	High
Binder Jetting (ExOne X1-Lab)	0.05	± 0.0635	Low
Shapeways Brass (3D Printed Investment Casting)	0.03[MJP]	± 0.125	Low
Metal Clay (COPPRclay)	0.12 (Powder size)	± 0.4 (FDM)	Low

4.2.5 Metal-Based AM Approach for Advanced Power Packaging Prototyping

In jewelry making, which is low to medium volume production, a lost wax casting process (investment casting) has been used for many years. The process makes a wax model as an

original part. A casting is then created of the wax model, and a metal part is created from the casting. This process has been updated with 3D wax printing. The optimized 3D structure is first printed in UV curable wax. The wax structure is placed into a container with liquid plaster poured around. The plaster sets, and the wax is melted away leaving a plaster mold for the casting process. The material used for investment casting, such as gold and bronze, is used in building electronic interconnect parts for this research, and would should be considered for building parts in power electronics packaging with other metals. Initial work has been done by printing 3D toroid coils for high frequency converters [12]. The attribute of the 3D printed investment casting (low cost, good resolution, and potentially wide choice of metal) makes it a good choices for building 3D metal structure in the prismatic module. Work based on this indirect metal AM process will be further discussed in the following chapter.

4.3 Summary

This chapter discussed different AM processes for making 3D structures in power electronics modules. The present AM process based on polymer and metal material were summarized and discussed. A polymer-based AM process could be used for printing housing parts for its short lead time, while the material selection is limited. Details were excerpted from Appendix A that described the fabrication of an Intelligent Power Module (IPM) using AM processing. Details referring to materials and cost were reviewed. Metal-based AM processes could be used for thermal management, such as heat spreader and sinks. By using an optimized 3D structure would provide better thermal performance. For the metal part used for energy conduction, direct AM and indirect AM processes are compared and discussed. One of the indirect

metal AM processes, 3D printed investment casting, was chosen for building the inner structure of the 3D prismatic power module.

4.4 Reference

[1] T. J. Horn and Ola Harrysson, “Overview of current additive manufacturing technologies and selected applications,” *Science Progress*, vol. 95, no. 3, pp. 255–282, 2012.

[2] Sayan Seal and Homer Alan Mantooth, “High Performance Silicon Carbide Power Packaging—Past Trends, Present Practices, and Future Directions,” *Energies* 2017, 10(3), 341; doi:10.3390/en10030341

[3] Jan Wilkes, Yves-Christian Hagedorn, Wilhelm Meiners, Konrad Wissenbach, (2013) "Additive manufacturing of ZrO₂-Al₂O₃ ceramic components by selective laser melting", *Rapid Prototyping Journal*, Vol. 19 Issue: 1, pp.51-57,

[4] A. Lopes, E. MacDonald, and R.B. Wicker, “Integrating Stereolithography and Direct Print Technologies for 3D Structural Electronics Fabrication,” *Rapid Prototyping Journal*, Volume 18, Issue 2, 2012, pages 129-143.

[5] Vaezi, M., Seitz, H. & Yang, “A review on 3D micro-additive manufacturing technologies” *International Journal of Advanced Manufacturing Technology* (2013) 67: 1721.

[6] H. Ke, Y. Xu, D. C. Hopkins, Conceptual Development Using 3D Printing Technologies for 8kV SiC Power Module Package, 46th International Conference and Exhibition on Microelectronics, Orlando, FL, Sep 30 – 03 Oct, 2013

- [7] J. M. Li. Packaging design & manufacturing of high temperature electronics module for 225oC applications utilizing hybrid microelectronics technology. International Conference on High Temperature Electronics, Santa Fe, NM, May 17-20, 2004.
- [8] M. Conrad, R. W. De Doncker, M. Schniedenharn and A. Diatlov, "Packaging for power semiconductors based on the 3D printing technology Selective Laser Melting," 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, 2014, pp. 1-7.
- [9] Haotao Ke, Adam Morgan, Ronald Aman, and Douglas C Hopkins, "Investigation of Rapid-Prototyping Methods for 3D Printed Power Electronic Module Development." International Symposium on Microelectronics: FALL 2014, Vol. 2014, No. 1
- [10] Christopher Kaestle, "Investigations on the Wire Bonding Capability on Selective Laser Melted Structures", IMAPS 2016 - 49th International Symposium on Microelectronics - Pasadena, CA USA - Oct. 10-13, 2016
- [11] Dede EM, Joshi SN, Zhou F. Topology Optimization, Additive Layer Manufacturing, and Experimental Testing of an Air-Cooled Heat Sink. ASME. J. Mech. Des. 2015;137(11):111403-111403-9.
- [12] M. Chinthavali, C. Ayers, S. Campbell, R. Wiles and B. Ozpineci, "A 10-kW SiC inverter with a novel printed metal power module with integrated cooling using additive manufacturing," 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, 2014, pp. 48-54.

Chapter 5 Module Design, Fabrication and Test

5.1 Introduction

In Chapter 3, a 3D prismatic power packaging concept is discussed for WBG power modules focusing on reduction of inductance. In this chapter, the physical realization of a 3D prismatic module is carried out to demonstrate the process feasibility. 3D printed investment metal casting process is chosen for one type of termination after an evaluation of various AM processes as discussed in Chapter 4.

The introduction of a new 3D prismatic packaging structure using 3D conductor layouts and orthogonal DBC substrate structures inside the module makes it necessary to conduct a thorough investigation into materials and layout design, which is covered later in the chapter. A test module to validate the process is first made to reveal potential problems in process, design and material selection.

Then, a fully functional half-bridge 1200V/50A SiC MOSFET 3D prismatic module is built for final testing. Device characterization is carried out. Finite Element Analysis (FEA) is used during the design for evaluation of electrical, thermal, and mechanical properties. A double-pulse tester was designed and applied for testing dynamic performance of the ultra-low inductance module. After the module is made, testing is carried out to verify the thermal and electrical stimulations.

5.2 Half bridge prismatic structure

The half-bridge (i.e. phase-leg) circuit is chosen for implementation, which is a common topology used in converters and has an upper and lower switch connected in a serial arrangement as shown in Fig. 5.1.

Figure 5.1 Half bridge module schematic

It has seven terminals: a positive and negative DC bus input, midpoint output, and two gate driver inputs with corresponding source connections (to form a Kelvin connection). In the layout of a 3D prismatic module, these terminals must be placed in such a way to be compatible with the next level-of packaging, yet also accommodate the 3D placement of components inside the module. Since the example circuit has four devices (two MOSFETS and two diodes), the optimum prismatic structure is a cube with four sidewalls with a device on each side. This provides maximum cooling and current carrying capacity. An alternative approach could place the MOSFETS and anti-parallel diodes together on each sidewall, and then a single-phase full-bridge could be realized. It is possible for other shapes if more devices are used. In a prismatic

module, it's desired to place the positive and negative terminals in the center for lower stray inductance, as well enabling placement of decoupling capacitors between the terminals. For the ease of manufacturability, the output terminal is placed in the center with the DC bus input on the sidewalls, as shown in Fig. 5.2.

Figure 5.2 Cross-section view of a 3D prismatic half bridge power module

The basic physical design of the 3-D prismatic half bridge power module is graphically shown in Fig. 5.2. Only few terminals (Output, G_U , and G_L) in Fig. 5.1 are shown in such cross section view. More detailed structures will be illustrated in the following part. Inside the module four chips are mounted on a patterned and scribed DBC substrate by solder or sintered silver. Then, the DBC is folded to form an orthogonal structure. The inner metal post serves as electrical connection and thermal path. The topside of the full module is connected to the PCB, and is the electrical port for the positive, negative, output, and gate terminals, while the other five DBC outer sides of the full module have connected heat spreaders or sinks.

For each DBC pattern inside the module, the source and gate pads of the lower bridge MOSFET, and the anode of the diode are attached to the substrate with a flip-chip method using solder, solder ball, or a 3D printed post. The drain pad of the chip is connected to the inner metal post (output terminal) by either soldering or a pressure contact. For upper bridge chips, the drain of the MOSFET and diode are attached to the substrate by soldering or silver sintering. The sources and anodes of the MOSFET and diode respectively are connected to the inner post by solder or pressure contact. The gate pad of the transistor could be connected by a wire bond or flex circuit.

The center Cu pad of the patterned DBC is for attachment of the center output post. The same Cu also connects to the sidewalls. 3D printed investment casting process is used for fabricating the inner metal post structure. The use of the 3D printing approach is not required, since a traditional method, such as CNC machining could provide a similar result. However, the 3D printing can provide a ‘porous’ structure at the electrical contact points to the chips, which would provide mechanical stress relief while making electrical connections (disclosure submitted). To demonstrate manufacturing feasibility of the half-bridge prismatic module, a test module without devices is built first.

5.3 Process Verification Module

The DBC substrates use two layers of copper clad to each side of a ceramic plate. The “frontside” copper layer is etched with patterns for mounting power devices and terminals. The “backside” copper layer is mounted directly on a baseplate (or heatsink). The ceramic is serving as electrical isolation as well as a thermal conductor.

5.3.1 Enhancements to the DBC substrate

Enhancements to the DBC substrate, such as through-hole ceramic vias, integrated terminals, and fluid-cooled DBC are possible [1]. Through-hole vias in the ceramic can provide access to the inner conductors for voltage sensing, gating, or allowing layering. Integrated terminals can include a Cu plane extending out from the DBC plate and may be combined with the through-hole vias. The cube can contain an electrically isolating, heat absorption material (e.g. phase change material) to absorb heat due to transient thermal heating. Fluid cooling can be added to flow fluid through the center of the cube providing dielectric isolation of the semiconductors while extracting heat. Other cooling methods can also be integrated into/onto the cube through heat-pipes embedded on the inside and/or outside of the cube. The entire approach using DBC can be replaced with other metal-clad electrically isolating materials, including for example, metal clad polymers, silicones or other organic materials. The DBC can be replaced with glass-epoxy boards or variations thereof, or metal-clad epoxy resin. Any electrically isolating material that can be metal clad, and processed where one side can be scribed and snapped (i.e. cracked, fractured, etc.) similar to the DBC processed described here, while the opposite side maintains electrical interconnection, can be substituted for the DBC described here. Also, the “Direct Bonded Copper” DBC (or “Direct Copper Bonded” DCB) does not exclude the use of other cladding metals on any ceramic, such as Aluminum in “Direct Bonded Aluminum” (DBA). Further discussion of details is beyond the scope of this research. The simpler cubic module will be used as suitable for verification and demonstration.

5.3.2 Design of the Process Verification Module

The DBC process that is used with the 3D prismatic packaging is 3-Dimensional DBC (Fig. 5.3), which was originally used to allow non-power components to be placed on the sidewalls. In the present 3D prismatic power package, such a structure hosts power devices on the sidewalls in order to achieve a low inductance path within the inner 3D metal structure.

Figure 5.3 3-Dimensional DBC substrate [1]

A test module without a semiconductor device is designed and fabricated for the purpose of process validation, and used for inductance measurement, in which the connectors are directly bonded to the DBC substrate. Since the evaluation of the soldering attachment between the post and devices is needed, solderable surfaces on both sides of the device are needed. A metal sheet of a similar size can be used to mimic the power devices in the test module. The parasitic inductance is simulated in Q3D for comparison with inductance measurement results.

The test module is used to describe the fabrication and simulated performance of the cubic 3D prismatic structure. The one process with little historical documentation is the folded DBC,

so fabrication details will be given. The remaining assembly processes and materials are relatively known in modern DBC processing, and used to minimize the risk of failure in this part of the research.

A 13x13x25 mm copper block with four 3x3x3 mm protrusions, i.e. posts, is machined on Haas TM-1 computer numerical control (CNC) milling machine, as Fig. 5.4 shows.

Figure 5.4 Dimensions for the center metal post

To mimic a power device for use in making inductance measurements, a metal copper plate is cut from a 0.254mm copper sheet into a 6mm x 6mm square, and then plated with nickel in the PREES Lab. The false power chips and inner post are mounted on the DBC substrate. The substrate is, then, folded and the false-chips are connected to the inner post forming electrical connection. (This completely mimics the final functional module if the devices are considered to be electrically “on”.) Two types of solders with different melting points are used for attaching the false-chips. The selection of the solder alloy is based on the melting temperature. A solder hierarchy is needed so more than 40°C temperature difference should exist between the melting temperatures of the two solders to avoid the movement of the part in the second reflow.

Use of a silver sintering process could eliminate the usage of different solders. Since the silver sintering is processed in a temperature (250°C) lower than its melting point (960°C), and should be employed in future work.

Figure 5.5 DBC layout design of the (a) Front side (b) Back side

The cube design begins with the DBC substrate layout shown in Fig. 5.5. The outline of the DBC substrate is designed as a cross-shape, which is produced from a single larger DBC plate. The four arms of the cross connect to the DBC center by topside metal. The center of the DBC substrate is patterned for mounting the inner post, while the MOSFET and diodes, or false-chips, are mounted on the arms.

5.3.2.1 An Alternative DBC Layout Using a Z-Pattern

Another DBC outline for making a cubic structure after folding is a Z-shaped pattern (Fig. 5.6). There are only two sides (top/bottom) of center DBC used for connection. The sidewall DBC substrates are connected with each other on the long side. By reducing the area needed on the center DBC substrate, the module size can be reduced. The issue for this type of outline is that an additional folding process is needed after forming the orthogonal structure, which

could bring in more misalignment in the position. Thus, only the cross-shaped outline is used. However, this approach very efficiently uses DBC boards (i.e. 5”X7” DBC boards).

Figure 5.6 Alternative DBC layout design

5.3.2.2 An Alternative Connection Using Pressure Contact

The interconnection of the power devices could use pressure contacts. For the pressure contact method, a beveled sidewall (Fig. 5.7(a)) would be preferred. The module only requires a small amount of vertical force to leverage a horizontal force to form the pressured contact, as Fig. 5.7(b) shows.

Figure 5.7 (a) Beveled sidewall for pressure contact (b) Pressure force for devices

5.3.3 Simulation of the Process Verification Module

A 3D model of the test module is built in SolidWorks and the extraction for the inductance between the positive and output terminal is carried out in Ansoft Q3D Extractor. The inductance result is 8.2nH. Test of the inductance is shown in the following part.

The current density distribution in Fig. 5.8 shows the current flowing through the inner post, with the current crowded on the side and upper arms of the structure. Thus a smaller spacing could be used for reducing the inductance. For the final module, a more thorough simulation is described in the following chapter.

Figure 5.8 Current density distribution during di/dt transition

5.3.4 Module Fabrication

To make the 3D prismatic cubic test module with DBC, an 8/12.5/8 mil DBC substrate is chosen for its thin ceramic thickness. A diamond tipped scribe is used to form a thin groove at the back of the ceramic. A uniform breaking line is acquired when bending the DBC substrate towards the front. The copper left at the front side will be the connection, which can be further bent to make the 90-degree structure needed. The material selected for the test module is listed in the Table 5.1. Encapsulation material for high temperatures is carefully selected for the module as well [2].

Table 5.1 Test Module Material

Component	Material
DBC substrate	8/12.5/8 mil Cu/Al ₂ O ₃ /Cu
Inner post	Cu
Metal sheet (mimic device)	6x6x0.254 mm Cu
1 st Solder	Sn10/Pb88/Ag2 (T _m =268~290°C)
2 nd Solder	Sn63/Pb37 (T _m =183°C)

A 5.5X7.5 inch Cu clad ceramic board (i.e. DBC) is patterned with a UV curable film as shown in Fig. 5.9a. The exposed copper is etched in a sodium persulphate solution. Some unused square areas remain, which are merely for reducing the etching time. The DBC board is then separated with a UKAM 6001 cutting saw into 3 square substrates. Grooves are scribed along the backside of the DBC square substrates and the square substrates are snapped to form

the cross structures or cubic-module substrates. The substrates (cross structures) are cleaned by acetone and Isopropyl alcohol (IPA) to remove the contaminations in the PREES Lab. Electro-nickel plating (Ni sulfate and boric acid) process is applied on the copper parts (substrates, inner post, false-chips, and terminals) to prevent the oxidation on the copper surface. The finished parts are shown in Fig. 5.9 (b).

(a)

(b)

(c)

(d)

Figure 5.9 (a) Etched pattern on DBC substrates. (b) Parts after nickel plating (c) Test module after first reflow (d) Test module after encapsulation

The false-chips, terminals, and inner post are attached onto the DBC substrate with Sn10/Pb88/Ag2 solder. Then, the entire structure goes through the reflow process with a Sika Falcon 5C oven. The oven is profiled as 150/250/335/180°C with 5 minute intervals and then cool-down to room temperature. The module after first reflow is shown in Fig. 5.9(c). The flux is removed by ultrasonic cleaning with IONX I3302 for 10 mins at 40°C. Second Sn63/Pb37 solder paste is applied on the tip of the post structure. The DBC sidewalls are folded towards the center along the snapped fold line until the orthogonal structure is formed. The second reflow process is done on the hot plate at 220°C with each side at the bottom. The reason for not doing reflow at once is to prevent solder from flowing vertically down onto the bottom. The use of solder masking would prevent the vertical flow and allow for single step soldering. An SMA connector is soldered between the terminals for connecting to the impedance analyzer later, as Fig. 5.9(d) shows.

The process verification module demonstrates the feasibility of building a prismatic module structure with “snap and fold” DBC substrate process. During the fabrication process, some issues remain. The metal post structure is made of large pieces of metal in the center, which takes a very long time to heat up during reflow. Also the large volume of copper would cause thermal stress on the device. Thus, a hollow structure of less mass is preferred. The snapped ceramic has a poor edge quality caused by hand scribing, which makes the module not fully foldable. An automatic dicing process is used for the final module. Also, the current loop inside the module could be further decreased by reducing the size of the module. Thus, the final module is designed and built based on these experiences.

5.3.5 Parasitic Inductance Measurement of the Process Verification Module

The parasitic inductance is extracted for the process validation module based on the simulation by Q3D Extractor. The test module is fabricated and tested to verify the result. Since the simulated inductance value is less than 10nH, which is challenging for measuring accurately. Thus a high precision impedance measurement equipment, Agilent E5071C vector network analyzer (VNA) is used. It has a frequency range from 7 kHz to 20 GHz, with impedance measurement range from m Ω to k Ω . The reactance of the module inductance is around 50 m Ω at 1 MHz, which fall into the test range of the equipment. S-Parameter test port was used for impedance measurement. Smith chart is used to display the impedance of the port. Calibration is carried out to the test port with open/short/load. The module is then connected to the test port with SMA connector. Measurement is conducted at 1MHz for the impedance. The testing result showed 11.5nH for the inductance of module and RF connector (Fig. 5.10).

Figure 5.10 Impedance measurement of the test module

For the comparison of the test and simulated impedance. Since there is no fixture compensation for the connector. The residue impedance of the connector is included in the test result. Considering the distance between RF port and power module, which has around 1nH on each terminal. The parasitic inductance between the module positive and output terminal is ten around 9.5nH, which meet the simulation result of 8.2nH.

5.4 1200V/50A SiC MOSFET Half Bridge Module

After the fabrication and testing of the process validation module, a working module is designed and built with 1200V SiC MOSFET and Schottky Barrier Diode (SBD). A more compact design is achieved with lower loop inductance. A finite element simulation is carried out during the design process for optimizing the module's thermal and mechanical performance. The dynamic behavior of the module is critical. Thus, the SPICE simulation is carried out with double pulse test circuits. The following mainly discusses the design, simulation, and fabrication process for the half bridge module.

5.4.1 Design of the Half Bridge Module

The exploded view of the module is shown in Fig. 5.11. The inner post is mounted on the center DBC substrate. Two MOSFETs and two SBD are attached orthogonally on the side DBC structures. Two thermistors (not listed) are mounted near the SBD. Orthogonal DBC substrates are folded along the center DBC substrate as sidewalls. The module is connected to PCB board by soldering the top terminals.

Figure 5.11 Exploded view of the prismatic half bridge module

The new DBC pattern is designed as Fig 5.12 shows. The material of the DBC board chosen is 12/25/12 mil thickness with Al_2O_3 ceramic, which proves sufficient mechanical strength for the orthogonal DBC sidewalls during and after the fabrication process. The prismatic module

is 15x15x15 mm (0.6inch each side). Thus, the center DBC substrate is 15mm by 15mm. For the DBC sidewalls, an additional 5mm long lead is placed at the edge. It folds outward to form the electrical terminals at the topside of the module. Four test patterns are placed around the cross-shaped substrate for process testing. The entire DBC substrate is 57mm by 57 mm. Gold on nickel plating is applied for better soldering and bonding performance. Solder masks are used for constraining the position of the devices during reflow process, as well as the voltage isolation for the flip chipped devices (shown in chapter 5.4.2).

Figure 5.12 DBC pattern design for final module

For the power devices to be attached on the substrates, SiC MOSFETs and SiC SBDs are used in the module. The topside of the devices must be solderable to form the connection, though most commercial power devices are designed for wire bonding and only have Al metallization on top. Work has been done by researchers for altering the Al top metal to solderable

metal, including electroless plating, metal sputtering, silver ink dispensing and so on. These processes have a high chance of device failure. Another issue is that the topside metal pad design for power MOSFETs is for wire bonding, which means the distance between gate and source pads could be very close (80 micron for Wolfspeed CPM2-1200-0025B). To avoid these issues, a new type of top-side solderable SiC MOSFET is acquired from Wolfspeed. The distance between the gate and source pads are increased to meet the flip chip design, which makes it possible to build a kelvin connection for the flipped low side MOSFET in the prismatic module. The topside solderable SBDs are provided from Global Power Technology with double sided Ag metallization. The flip chip process is investigated in the next chapter regarding its influence on voltage blocking capability.

To reduce the length of the current loop path between the terminals through the chip, a 45 degree rotation for the device placement is applied in the pattern design. This moves the joint on the inner post up and reduces the loop length. Also, the distance between the post and side-walls is reduced to have a smaller loop size. It also reduces the size of a DBC substrate to around nine times of the chip, which should be sufficient for heat spreading. The spacing created at the corner is used for the kelvin gate of the MOSFET. Gate driver chips can also be placed in this area, if needed. Two thermistors (-55 to 220 °C) are placed next to the SBDs for built-in temperature measurement.

For the orthogonal DBC, the fabrication process is different compared to the test module. Since the ceramic has doubled the thickness, it is difficult to snap the ceramic along the scribed line made by hand. Meanwhile, the edge of the prismatic module needs to be straight and smooth for a good mating with the heatsink, essential for a low thermal resistance. Thus, an

improved process is used with an automatic dicing machine normally used for separating the semiconductor devices on the wafer. The process is illustrated later in the following part.

The inner post structure of the prismatic power module is made by the 3D printed investment casting process, which permits the freedom in designing the structure in 3D. In order to design the structure with optimized geometry, investigation into the fundamental electrical and thermal-mechanical issues is carried out during the design cycle.

For the electrical aspect, current between the power ports will flow to the inner post through the source of the U-MOSFET, the anode of U-SBD, the drain of L-MOSFET, and the cathode of L-SBD. Since the inner post material is made of brass, the current path have low enough resistance for carrying high current, e.g. 100A. The key issue is to arrange the current path in the 3D prismatic power module. Low inductance path between ports are the first design target. This could be done by connecting each electrical interface with the shortest possible path, with enough isolation. Also, as stated in chapter 3, the mutual inductance cancelation effect should also be utilized by placing the conductors close. As for the design of the half bridge module, current paths exist through the upper and lower switches during operation and a commutation current exists during switching. These current loop inductances could be reduced by having less distance between the 3D post and the devices. Considering the wire bonds clearance of the U-MOSFET, a 2mm long column with 1mm radius is chosen as the contacting post. A more complex structure could be used for stress management at the joint point with the devices, such as spring or pins. Regarding the voltage isolation between the post and sidewall, the silicone gel encapsulation material can withstand more than 20kV/mm, which satisfies the requirement.

5.4.2 Device characterization

As the encapsulation material proves its capability at high temperature. Other components' performance should also be evaluated. The SiC MOSFET device has an operation temperature to 175 °C on the datasheet, while the SiC SBD devices does not have enough information regarding the high temperature performance. Thus the static test for the SBD device for high temperature is essential.

The SBD is first electrically tested as a bare die using probe station filled with Fluorinert dielectric fluid. Reverse bias characteristics were extracted to observe the bare die leakage current performance up to 1.4kV. The die is processed using a flip-chip approach similar to what is done in the microelectronics industry. Firstly, a Kapton spacer is laid out on the bottom metal test substrate to each the desired spacing. Secondly, high temperature solder paste (Sn5/Pb95) is dispensed onto a metal test substrate and the SBD is “flipped”, anode-side (top-side) down onto the solder paste. Next, a solder reflow process is performed. Lastly, a lower temperature solder paste (Sn95/Sb5) is dispensed onto the cathode-side (backside) of the SBD and a metal interconnect is placed on top before a final solder reflow process. Flux cleaning process is done in the ultra-sonic cleaning machine. A standard cleaning process (Acetone – Methanol – IPA – DI water – N₂) is applied before the module is encapsulated with Wacker 915HT silicone gel.

Figure 5.13 Reverse Characteristics for Double Ag SiC SBD

The reverse blocking test result is acquired for the double side SBD. The leakage current of this device is smaller than that of CPW5-1200-Z050B at temperature over 125 °C, which means a less power loss from SBD in high temperature operation.

The test sample is also using the same equipment for observing the package effects of the double- sided interconnect on the reverse bias performance by measuring the leakage current. The test results show very little difference in the leakage current for the unpackaged versus packaged SBD, particularly in the high voltage region (Fig. 5.14). This could be due to good side quality of the tested SBD, as this is atypical of what is expected [3], [4]. Further investigation is carried out for the influence of packaging structure on SBD guard ring performance in Sentaurus TCAD. It was figured out in simulation that the electric field distribution inside the device's guard ring is affected by the close-up metal structure, which could potentially bring into more leakage. This could worth more investigation in the future.

Figure 5.14 Reverse characteristic comparison between bare die and flipped chip

The forward characterization of the device is tested with Tektronix 371A curve tracer as Fig. 5.15 shows. Fig. 5.16 is the result of the device, which showing a very similar performance with CPW5-1200-Z050B SBD. Considering the similarity of these devices' static curve, the SPICE model of CPW5-1200-Z050B is used as the model for double Ag SBD in the double pulse simulation. Though more accurate model could be acquired through dynamic test.

Figure 5.15 Test set up for forward characterization

Figure 5.16 Forward characteristics for double Ag SiC SBD

5.4.3 Simulation of the Half Bridge Module

5.4.3.1 Thermal Simulation

Besides the electrical function, the inner post could also be designed to benefit from 3D in the thermal-mechanical aspect. An interconnecting technique called Press-fit pins is used in a power module by manufacturers like Vincotech [5], which provides a highly reliable connection by absorbing the thermal induced stress with the mechanical deformation of the pins. This concept is used within the post design.

The final design of the inner post structure is shown in Fig. 5.17. A 9x9x2 mm foundation is used to secure the center copper isle. Four beams, 11mm long, 3mm wide with 0.8 mm thickness, stand vertically up from the side of the metal base. On the middle of each beam, a contacting column connects to the corresponding power device. All the beams are united to a cross-shaped platform at the top end, where five 3.5 mm long hole pins with 2.54 mm spacing

are placed. The bevel on the edge of the platform is used to increase the pitch between the output pins for higher voltage isolation.

Figure 5.17 Inner post structure design

In order to make sure that the beams absorb the thermal stress, a thermal stress simulation is carried out in COMSOL Multiphysics 4.4. The post design is imported into the simulator as an IGS file. Since there are no material properties available for the 80Cu15Zn5Sn brass, 85Cu15Zn red brass is used. The material properties for simulation is listed as UNS 23000 red brass alloys [6]. Prescribed displacement constraints are applied on the contacted surface (four surfaces attaching to chip, one surface attaching to DBC, and one surface attaching to PCB). The temperature on the surfaces attached to the chips is 200°C and the bottom surface is 100°C. The simulation result of the von Mises stress (N/m^2) is shown in Fig.5.18.

The yield strength of the red brass material is 69-434MPa (depending on post process). It can be seen from the simulation that the stress inside the beam structure is lower than the yield point. Though there is some stress concentration at the sharp edge connecting the base and top

platform, it can be improved by thickening the material here. From the mechanical simulation, the beam will deform elastically to absorb the thermal stress when the module is heating up and will return to the original shape once the temperature gets back to room temperature. The stress management performance could be improved with a thinner beam made with a harder conductor. As for the current design, more works could be done in the future. Since the selection of the material are limited by the manufacturer.

Figure 5.18 Strain stress for the structure @ 200°C

The thermal design for the module is another critical part in the system. A pin-fin heatsink with a 1.5x1.5x7.5 mm pin size is applied on the five sides of the prismatic module. By placing

the heat source on the sidewall of the module, it is possible to achieve parallel cooling for the devices. A simulation is carried out in COMSOL Multiphysics 5.1 for the thermal performance. The heatsink design is imported in the simulator together with the air around. Four chips are mounted on the inside of the heatsink. The reason for not using the entire module is to reduce the complexity of the fluid simulation. Complex details would have chance lead to convergence issues. Total power loss of 30W is applied on two opposite devices to mimic the power dissipation from the MOSFETs. The air is blowing to the heatsink from two sides at 45 degree angles with a velocity of 7m/s at room temperature. The simulation result is shown in the Fig. 5.19(a). To compare with heatsink with one cooling direction, a regular pin-fin heatsink with the same pin area is simulated as well. Four chips are placed on the heatsink as two pairs of switch, with 20 mm spacing in between each pair. The 30W power loss is applied to the bottom two chips representing the MOSFETs. There is no heat dissipation on the diodes. Air flow is blown in from the shorter side of the pin-fin heatsink. The simulation result is shown in Fig. 5.19(b).

As it is shown in the simulation result of the 3D heatsink, the maximum temperature is 100 °C on the chip. The maximum temperature is 190°C for the planar heatsink, located at the chip placed near the far end of the air income. An approximate 10°C difference, between two chips, is due to the heating up of the air through the fins.

Thermal testing is carried out for validating the thermal performance of the module. Detailed description will be found in the flowing chapter.

(a)

(b)

Figure 5.19 Surface temperature of (a) Parallel-cooled Heatsink and (b) Series-cooled Heatsink

5.4.3.2 Electrical Simulation

The physical geometry of the prismatic module is designed and simulated and the electrical performance evaluation of the module is carried out. Dynamic switching performance is one of the most widely used criteria for evaluating a power module. In order to look into the turn-on and turn-off transient of a prismatic module, the double pulse test circuit is used, which is basically a step down converter utilizing one MOSFET and one SBD inside the module with an inductive load. Simulation is carried out in LTspice for the dynamic performance of the entire circuits with the circuit shown in Fig. 5.20.

The prismatic module parasitic inductance is extracted by Q3D with the same procedure described as the process validation module. Simulation results are shown in table 5.2 with DC and AC inductance. The AC excitation frequency is 100 kHz with skin effect consideration.

According to the simulation, the commutation loop inductance for the module is 12.4nH, similar to the planar module. The positive to output inductance is 7.1nH for both phases, which utilized the mutual inductance cancelation effect with approximately 2nH reduction. The symmetric geometry of the module letting each current path run with the same inductance. The distance between the inner post and sidewalls could be further reduced for more inductance cancellation.

Figure 5.20 Double pulse tester schematic circuit

Figure 5.21 Q3D simulation for the prismatic module

Table 5.2 Simulation result of the module parasitic inductance

Current path	DC value (nH)	AC value (nH)
Positive-Negative (via S_1 and D_2)	13.2	12.4
Positive-Output (via S_1)	7.9	7.1
Positive- S_1	4.0	3.8
S_1 -Output	6.4	5.6
Output-Positive (via D_1)	7.9	7.1
Output-Negative (via S_2)	8.1	7.2
G_H - S_H	10.4	10.0
G_L - S_L	5.9	4.6

To get an accurate simulation, parasitic parameters from the PCB board and the device models are needed. For the SPCE model of the solderable devices, Wolfspeed SiC device library is used for selecting the model of a similar device as substitution. SiC MOSFET model, C2M0025120D, has a similar power rating and chip size with the solderable device. The model chosen for SiC SBD is CPW51200Z050B. The double Ag SBD from Global Power is similar in size to Wolfspeed CPW51200Z050B. The forward and reverse characteristic for the SBD is shown in the next chapter as well.

The PCB for double pulse tester is designed in Altium Designer, as showed in Fig. 5.22. The DC power supply is connected to the test module through the bus capacitors. The test prismatic module is mounted upside down on the PCB board, with several decoupling capacitors. Gate driver boards are used for triggering the low MOSFET. The copper traces between

the module and decoupling capacitors is carefully routed to minimize the parasitic inductances. The PCB file could be exported from Altium Designer directly as DWG or DXF file, but, an issue with the complex shape transferring to Q3D exists. Some fine geometries must to be modified manually. Thus, the PCB board is rebuilt in SolidWorks and imported into Q3D Extractor as an IGS file. The simulation result of the power loop parasitic inductance is implemented into the LTspice simulation circuit.

Figure 5.22 Double pulse test PCB layout

Based on the parasitic extracted from the design, a double pulse test circuit is built in the LTspice IV. The parameter of the test circuit is shown in table 5.3. The simulation is carried

out under 1050V/50A. The result is used in the next chapter to make a comparison with the actual test waveform.

Table 5.3 Double pulse tester parameters

Component	Parameters
DC Voltage	1050V
DC decoupling capacitor	100 nF
L_{load}	1.9 mH
L_1, L_2, L_3, L_4	3.5nH
L_{trace1}	5.9nH
L_{trace2}	2.0nH
L_{bus}	20.8nH
L_{sensor}	51.8nH

5.4.4 Half Bridge Module Fabrication

The previous design and simulation defined the physical geometry of the module. Then, the assembly process is carried out for the functioning module. Few 3D printed inner posts are made by Shapeways based on the design. The dimensions of the part is measured by caliper to ensure the accuracy was met for assembly.

Figure 5.23 3D investment printed inner posts

The material list for the module is shown in table 5.4.

Table 5.4 1200V/50A SiC MOSFET Module Material list

Component	Material
DBC substrate	12/25/12 mil Cu/Al ₂ O ₃ /Cu
Inner post	Casting Brass (80Cu15Zn5Sn)
SiC MOSFET	1200V/85A MOSFET (double Au)
SiC SBD	1200V/50A GW1-S12050(double Ag)
Thermistor	US Sensor MM104J1F
Device and post attachment	Sn5/Pb95 ($T_m=312^{\circ}\text{C}$)
Device topside attachment	Sn95/Sb5 ($T_m=240^{\circ}\text{C}$)
Heatsink attachment	Sn63/Pb37 ($T_m=183^{\circ}\text{C}$)

The DBC substrate with patterns is mounted on an adhesive tape topside down. Then, the film is mounted on the machine for the diamond saw to cut a groove on the ceramic. The depth of the groove is designed to be about half of the thickness of the ceramic. The groove should not reach the copper at any time. After the grooves are diced, the adhesive tape is removed and the DBC substrate can go through the follow up processes. Several tests are carried out ahead of time to validate this process.

Figure 5.24 Process for dicing groove on backside of DBC substrate

The DBC substrate is made by Yinhe Co. from China with electroless Au finishing on top. The first process is grooving the DBC, which is done by DISCO DAD321 dicing machine with 0.2mm thick diamond blade. Three grooves for the extended terminals are made first. Then, the ceramic strip between the grooves can be removed by mechanical method (diamond sanding wheel) to ensure enough spacing when bending the terminals outwards.

After all DBC substrates are grooved at their backsides, all the components (MOSFET, SBD, thermistor, and inner post) are attached onto the substrate with Sn5/Pb95 solder paste. Four pieces of Kapton spacer (2x2 mm) are used at the corners of each lowside device before the reflow process. They are removed later with the spacing created for voltage withstanding.

The oven, for first attachment, is profiled as 150/250/350/180°C with five-minute intervals. The flux is removed by soaking the module with IONX I3302 for 30 minutes at 40°C, then ultrasonic for 5 minutes at 40°C. The sonic time should be short to avoid damaging the gate connection of the MOSFET. There should be no flux residue left beneath the low side devices.

Figure 5.25 (a) Diced grooves on ceramic. (b) Flip chipped L-MOSFET. (c) Wire bonded U-MOSFET.

Fig. 5.25(b) shows the low side MOSFET after the reflow process. The next step is wire bonding from the high side MOSFET gate and auxiliary source pads to the copper traces, which form the Kelvin connection for the driver. The bonding process is carried out on Hesse-Mechatronics BJ939 automatic wire bonder with 4 mil Al wire. The bonding parameter is carefully set up to form a low profile bonding (less than 2mm) to keep the electrical clearance inside the module.

The DBC substrate is then snapped along the grooves to get the cross shape outline. The side DBC substrates are folded inwards the center post to approximately 80 degree first with a piece of thin metal at the bending line, which could avoid the peering-off of the copper and help align the side DBC substrates. It is also helpful if a shallow groove is made on the topside copper corresponding to the grooves.

(a)

(b)

(c)

(d)

(e)

(f)

Figure 5.26 (a) DBC substrate after attachment. (b) DBC substrate after snapping. (c) Module starting to be fold. (d) Folded DBC substrate. (e) Module after encapsulation. (f) Module with heatsink

The test patterns around the cross shaped outline are snapped off as Fig. 5.26(a) shows, which could be used for device test and process optimization. The terminal pads are then bent

outward to form the terminals that connect to the PCB. Then, the Sn95/Sb5 solder is dispensed on the inner post at the contacting surface of the power chips. A small amount of the solder is required for the solder to stay at the joint area during reflow. A good practice for this is a size smaller than the column cross-section area.

A square fixture is used for the second reflow process. The module slides into the fixture and goes through the second reflow process. The oven, for second the attachment, is profiled as 120/230/290/150°C with five-minute intervals. The flux is removed by soaking the module with IONX I3302 for 30 minutes at 40°C, then ultrasonic cleaning for five minutes at 40°C.

The module is now clean and ready for encapsulation. Wacker 915 HT silicone gel is used as the encapsulation material. Two parts are mixed with 10:1 ratio and vacuumed to remove the air captured inside. The module is sealed by the Kapton tape at the edge. Then silicone gel is poured into the module and cured in the oven at 100°C for 30 minutes. Fig. 5.26(c) shows the module after the encapsulation process. The 3D printed heatsink is attached to the module by Sn63/Pb37 solder, which is done with a hot air gun and heat plate at 300°C. The final module is shown in Fig. 5.26 (d).

The process could be improved by attaching the heatsink in the second reflow process and then do the encapsulation. Thus, the module could work at a higher temperature. Also, the side wall design for the heatsink can be improved with bevel, which could utilize pressure contact for the device's interconnection.

5.4.5 Test for the Half Bridge Module

5.4.5.1 Double Pulse Test

During a double pulse test, two pulses are used to get the device's dynamic performance. The inductor is charged to the desired current, and the device is turned off. Thus the turn off characteristic is acquired. Then the device turns on after few micro seconds for getting the turn on waveform. During the switching process, ringing across the positive and negative terminal are reduced by the decoupling capacitor. Simulation has already carried out in section 5.4.3.2. This part is mainly on the experimental set up and test result.

Figure 5.27 Double pulse test board set up

Fig. 5.27 shows the setup of the double pulse tester. A $90\mu\text{F}$ capacitor bank is attached between the DC buses for providing enough energy to module. The test module is mounted on the PCB through the mounting holes and pads. Three 100nH ceramic capacitors are placed close to the module as the decoupling capacitor. Jump wire (18 AWG) are used for current measurement. The rise time of the SiC MOSFET is usually over 25ns , which correspond to a

frequency of 10MHz ($0.25/t_r$). Thus The Tektronix TCP0150 current probe was used, with a 20MHz band width. Isolated gate driver boards (Wolfspeed CRD-001) was used to power the module. The voltage V_{ds} is measured by Tektronix THDP0200 high voltage differential probe.

The turn off voltage and current waveforms are shown in figure (a) and figure (a) at 1050V, 50A condition. The highest voltage of the module is 1250V, which means 200V in voltage overshoot. The turn off current slope is calculated as 2.63A/ns ($20A / 7.6ns$). Thus the stray inductance is calculated to be 76nH, the sum of the inductance between decouple capacitor and voltage measurement point is 66.7nH (mostly from the jump wire), which meet the calculation.

The turn on voltage and current waveform are shown in figure (a) and figure (a). Comparing these simulation result with the test waveform, they match with each other for the voltage overshoot, turning on and off slope, and the reverse recovery current. There are more oscillation in the simulation, which may due to the resistance parts in the test circuits.

Self-capacitance of the inductor is acquired through test, which is 33.5pF. The simulation shows little influence of the switching waveform. Thus it's not considered.

(a) MOSFET turn off voltage from test

(b) MOSFET turn off voltage from simulation

Figure 5.28 Comparison of experiment and simulation MOSFET turn off voltage

(a) MOSFET turn off current from test

(b) MOSFET turn off current in simulation

Figure 5.29 Comparison of experiment and simulation MOSFET turn off current

(a) MOSFET turn on voltage from test

(b) MOSFET turn on voltage from simulation

Figure 5.30 Comparison of experiment and simulation MOSFET turn on voltage

(a) MOSFET turn on current from test

(b) MOSFET turn on current in simulation

Figure 5.31 Comparison of experiment and simulation MOSFET turn on current

5.4.5.2 Thermal Test

Thermal test for the packaged module is carried out for evaluating the heatsink performance. A 20 A current is conducted through the low side SiC SBD to observe the temperature distribution in and outside of the module. In the test, a constant air flow is running through the heatsink to take the heat away. The temperature is recorded by the thermistor inside the module and by the thermal couple on the heatsink.

Figure 5.32 Thermal test set up

The test set up is shown in Fig. 5.32. The module under test is placed at the top of two piece of aluminum bar, which are used to get the uniform air flow. 2 layer of Kapton tapes are applied on the bar to prevent thermal conduction. Also the area of heatsink that contacting the supporting material is minimized by placing the heatsink at the edge. The test module is connected to a TDK Lambda ZUP 36-24 DC power supply through the wire. The thermistor ports are connected to a Tektronix DMM 4050 precision multimeter for the resistance measurement during the test. Thermal couple (Type-K) is attached on the heatsink with thermal grease at the center of the heatsink, right beneath the SBD area. A fan (Delta AFC1212DE) is supplied with

12V/1.5A for generating air flow to the module. Air flow sensor (UAS1200XS) is used to collect the real-time air velocity and temperature.

The initial room temperature was measured. The thermistor resistance is 105.6 k Ω value, corresponding to 25°C. The reading of the thermal couple at the heatsink is 26°C. Then the power is turned on with 20 A current running through the SBD device. The temperature reading of all the equipment gets stable after 1 minute. The measurement is started on 5 minutes. The air flow sensor is placed 2cm in the front of the heatsink while the data is being collected through USB port to computer. The air velocity and temperature is recorded for 1 minute. The collected air velocity and temperature is shown in Fig. 5.33.

Figure 5.33 Inlet air velocity and temperature

Figure 5.34 IR image of the module surface temperature

The reading from the thermal couple is 46°C, which represents the temperature of the heatsink beneath the device. Thermal image is taken by IR camera (FLIR T62101), as shown in Fig. 5.34, which showing an even temperature distribution with a highest temperature of 45.2°C. This meet the test result of the thermal couple. The temperature inside the module is measured by the thermistor. The resistance of the thermistor is 9.06kΩ at steady state, which corresponds to 90°C according to the manufacturer's R-T chart.

The thermal resistance of the package from junction to ambient could be calculated by equation (6.1):

$$R_{\theta} = \frac{T_j - T_a}{P_{loss}} \quad (6.1)$$

Where R_{θ} is the thermal resistance from junction to ambient, T_j is the junction temperature, and T_a representing the ambient temperature. P_{loss} is the power loss from the device. In the test,

SBD is conducting 20A current through, which would have 1.3V voltage drop at 75°C from figure 6.6. Thus the power dissipation from SBD would be 26W. The calculated thermal resistance is from junction to ambient is 1.69 °C/W. If a maximum junction temperature of 175°C is considered with 40°C ambient temperature, the module could dissipated at most 80W.

For a SiC MOSFET, the device has a 13mΩ drain to source on state resistance, 1.5 mJ and 1.0 mJ turn-on/turn-off switching energy (800V/75A). The total loss for an operating power MOSFET can be calculated by equation (6.2):

$$P_{loss} = P_{on} + P_{switch} = I^2 R_{ds-on} + f(E_{on} + E_{off}) \quad (6.2)$$

In which f represent the switching frequency. For a 30A operation condition, the on-state loss would be 11.7W. Each MOSFET could dissipate 40 W power. Thus the switching frequency of the MOSFET should not exceed 11.32 kHz.

The power density calculated for the module is 12 kW/in³ (including heatsink). It could be higher with a better thermal solution. New 3D design for the inner post with focusing on integrated cooling could be used in the future design. Also the improvement could done by using void-free reflow process, and using thinner ceramic with higher thermal conductivity for DBC substrate.

5.5 Summary

This chapter describes the validation of a 3D prismatic packaging concept by building a 1200V/50A SiC MOSFET module, which is designed in 3D for the first time. The 3-dimensional DBC process is tested first through a test module. The design for a functioning module is proposed after evaluating the process of building a test module. A 3D printed structure with a

capability of absorbing thermal stress is proposed, with a thermal mechanical simulation carried out. Thermal simulation for the 3D heatsink performance is done. The result is compared with that of a planar heatsink sink. Parasitic inductance of the current path is extracted in the module, together with the PCB board. Electrical simulation is carried out for evaluating the module's dynamic performance. The procedure for fabrication of the module is recorded. Testing of the module is carried out. Component tests was carried out prior to module fabrication. The static performance of the SBD is measured, together with the voltage blocking capability of the flip chip structure. The inductance measurement of the test module was carried out. Since the inductance is small, a precision impedance measurement was carried out with VNA. The measurement result agrees with the simulation. Thermal test for the module is set up and carried out for getting the module's thermal resistance, which is $1.69\text{ }^{\circ}\text{C/W}$ from junction to ambient. Module with working devices are mounted on the DPT board for characterizing of the module switching performance. The voltage and current across the module was tested. The analysis for the result was carried out, showing a number that meet with the simulation. The waveform of the test also meet with the simulation.

5.6 Reference

- [1] D.C.Hopkins. "Making of Direct Bond Copper." Internet: http://www.dchopkins.com/professional/open_seminars/DirectBondedCopper.pdf, 2003 [July 10, 2017].
- [2] Xin Zhao, Haotao Ke, Yifan Jiang, Adam Morgan, Yang Xu, and Douglas C. Hopkins (2016) A High Performance Power Module with >10kV capability to Characterize and Test In Situ SiC Devices at >200°C Ambient. Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT): May 2016, Vol. 2016, No. HiTEC, pp. 000149-000158.

[3] J. Xu, "Issues and Options for Planar Packaging of High-Voltage SiC Diodes," 5th International Conference on Integrated Power Electronics Systems, Nuremberg, Germany, 2008, pp. 1-7.

[4] P. Kanschat, I. Paul, "Semiconductor Module and Process for ITS Fabrication", U.S. Patent 20100127400A1, May, 27, 2010.

[5] M. Thoben, I. Graf, M. Hornkamp, R. Tschirbs: "Press-Fit Technology, a solderless method for mounting power modules" Proc. PCIM, Nuremberg, 2005

[6] "Red Brass UNS C23000." Internet: <http://www.azom.com/article.aspx?ArticleID=6338>, Aug 6, 2012 [July 10, 2017].

Chapter 6 Conclusion and Future Work

6.1 Conclusion

6.1.1 Summary of the Work

This dissertation focuses on WBG power module package design based on the 3D prismatic packaging concept and the process for building the 3D structure inside the module utilizing 3D printing process.

In chapter 2, the basic structure of a power module is reviewed. Then the challenge of WBG power electronics packaging is introduced. Efforts on material and structure improvement in the power module package is summarized and discussed.

In chapter 3, the concept of WBG power module is introduced. The reduction of the stray inductance in the commutation loop of a phase leg is exploited. A current path in 3D is proposed to further reduce the stray inductance. A 3D prismatic shaped power module is then proposed based on this 3D current path.

In chapter 4, the 3D printing processes are summarized for the power electronics packaging. First the polymer-based 3D printing process are evaluated for the feasibility to power packaging process. The process of building a printed housing with embedded gate driver is demonstrated. The disadvantage of the polymer-based processes is summarized. Silicone gel is characterized with low leakage current through the test module at high temperature. Then the metal-based 3D printing process is reviewed with initial attempt in printing metal on ceramic. The advantage and disadvantage of the direct metal printing process is discussed. Finally an investment casting process with 3D model is selected for the making of the prismatic power module.

In chapter 5, to develop the process for building prismatic module. Test module is built first, with the parasitic inductance simulated by Q3D extractor. After the process validation, the function module in a half bridge schematic is designed with the aid of COMSOL software regarding the thermal-mechanical performance of the printed structure. Simulation of the 3D printed heatsink is done and is used as comparison with the flat heat sink. The simulation for the parasitic inductance is carried out for each current path inside the module. With the parasitics extracted from the PCB, circuit simulation is carried out in LTspice for double pulse tester to get the dynamic performance of the module. The module is made then with the desired 3D structure. Before the module fabrication, the components inside are tested separately. Double side solderable device is characterized for its static performance in the room and high temperature. The result matches with the device model to be used in the circuit simulation. The flip chip process is tested for the voltage blocking capability. After the module is fabricated. Thermal test is done with thermistor and thermal couple. The measurement result is used to calculate the thermal resistance of the module. The experimental result shows a $1.69\text{ }^{\circ}\text{C/W}$ thermal resistance. The electrical test is carried out on the double pulse tester. The simulated waveform meets with the test waveform with an over shoot less than 20% during the turn off process.

6.1.2 Design rules for 3D prismatic module

Based on the experience gained during the design, fabrication, and test process in the dissertation, several design rules for designing prismatic shaped module are summarized as following:

- Think in 3D in the design process, which means all the spacing inside the power module could be used for placing active and passive components.
- The electrical ports and thermal ports need to be defined first based on the next level system requirement, such as heat spreader plane, liquid terminal fittings, and electrical terminal nuts. If there is no specific regulation, electrical ports should be placed close could with enough creepage distance, to reduce the inductance between. The rest area should be used as much as possible for thermal dissipation to increase the power rating of the module.
- The power device should be placed close to the electrical port if possible to minimize the resistance and inductance along the electrical path, the different 3D conductor path should be carefully arranged considering the electromagnetic interference (EMI), which could be an issue.
- The thermal conduction path for dissipating the heat should be low. Highly thermal conductive material or structure could be utilized in the module to get a low thermal resistance between the chip and the thermal boundary.
- The 3D structure that on the heat dissipation path should have a deformable design for absorbing the mechanical stress induced by the heat. Another option is to have zero CTE mismatch inside the module by carefully design of the structure or the material combination.

6.1.3 Contribution of the dissertation

The contributions of this work are summarized as following:

- The state of art 3D printing process is evaluated and summarized for the power packaging process, introducing the 3D printed part in prototyping power module packaging.
- Proposed a novel 3D prismatic package structure for WBG power electronics. The material and process for building the structure is validated. The working module is tested with its electrical and thermal functionality.
- Proposed a 3D power path concept for further suppress the commutation inductance in a power module.

6.2 Future Work

The possible follow up works that could be studied in the future are:

1. The proposed module is validated with the half bridge schematic, which is not fully utilized the advantage of field cancelation on the 3D power path. An H-bridge module or 3 phase module could be evaluated with the DC bus placing inside.
2. The bevel edge design could achieve pressure contact and self-alignment during assembling process, which is attractive considering the reliability of the press pack and the manufacturability.
3. The 3D printing process is still growing rapidly with expected new material and process available (and the cost reduction) in the near future. More parts in the power module, such as substrates, could be built with potential hybrid metal-ceramic printing process. By the 3D printing process, there will be more freedom in designing power module.

4. The integration of different components by 3D structure. In this work the integration of mechanical and electrical function is demonstrated as the center post structure. While there are more opportunities with more integration by 3D structures, such as 3D liquid cooling pipe as electrical terminals, gate driver integration with power devices. As the 3D structure entitle more freedom in design as well as the power density of the module gets higher. There should be less part with sole function. More passive components with balanced electrical, thermal, and mechanical performance and more integrated active components are expected within the future power electronics modules.

Appendix A. Fabrication of Gate Driver Embedded Housing

Production of the full module is summarized in Fig. A-1. The DBC substrate is processed with traditional power module assembly processes, such as a two-level solder hierarchy. The substrate could have been secured to a baseplate also. The lid is printed with an embedded circuit pattern; components are placed lead-side upward, and an Ag-loaded polymer is dispensed into/onto the component leads to form the traces and interconnection. Also, terminations are connected and secured to the lid traces with the conductive polymer. The housing is fitted over the substrate and secured with a standard epoxy process. The lid is fitted onto the housing with the substrate leads protruding through the lid openings. The substrate leads are ‘folded’ onto the lid. The gate lead and any sensor leads (from the substrate) are connected with Ag-loaded polymer. To provide greater connection strength, caverns can be patterned into the lid to allow an Ag-loaded epoxy to flow in and form a stronger, stress-relieved bond. The final step is to fill the housing through the lid with silicone, which is vacuum cured.

For the material and equipment used in the experiment, a FAN3122TMX gate driver (SOIC8 package) is used in the embedded circuit. A Si power MOSFET (IRFC3205, 55V/110A) and diode (IR135DM12CCB, 1200V/8A) are used as the controlled devices. The following materials and equipment are used for their respective applications listed: Orthodyne M20 wedge bonder with 4mil Al wire interconnection, EFD solder paste S10D502B2 (Sn10/Pb88/Ag2) and 63NCLR (Sn63/Pb37) for die attachment and terminal attachment,

Wacker SEMICOSIL 921 for silicone encapsulation, DuPont 5025 silver conductor for the conductive traces in the control circuit, and Nordson EFD dispensing system for trace dispensing.

Figure A-1. Design process flow chart

This “housing” design was chosen to mimic a Vincor HDC300B Converter Brick Module to show compatibility with current power module technology. SolidWorks was used to draft STL (stereolithography) files required by many 3D printers, including the Objet printer.

Figure A-2. SolidWorks design for power module (a) lid and (b) housing

A housing lid was designed to cap off the internal power electronics, giving mechanical strength to the gate, source, and drain terminals, and to incorporate an embedded gate driver circuit that would otherwise be stationed separately from the module, e.g. on an external PCB. Greater power densities and switching speeds are obtained by embedding such circuits into the power module.

The drain, source, and gate terminal holes were labeled A, B, and C, respectively, using the Objet printer. A separate “silk screen labeling” step is not required. The gate driver circuit was routed on the lid’s surface between terminal holes A, B, and C. Holes A and B are rectangular and aligned with the brass terminals on the DBC substrate. Adjacent to each of these are indents for the nuts and screws used to connect the drain and source terminals to an external circuit. The gate hole allows for a circular gate lead on the substrate to pass through, bend, and be soldered into the gate driver circuit.

The FAN3122TMX gate driver IC (8 pin SOIC), is mounted upside down in its respective receptacle. Passive components, such as the capacitors and resistors, are mounted on top of pedestals within the connecting trenches to inhibit the flow of conductive silver paste underneath the components, which may lead to short circuits. A side view of the connecting trench is shown in Fig. A-3.

Figure A-3. Trench dimensions with pedestal

The trench is set 0.25mm below the lid's surface to provide an overflow region for the conductive silver paste to contain possible surface over-accumulation of printed silver paste.