ABSTRACT

RAMANAN, NARAYANAN. Investigation of ALD Dielectrics for Improved Threshold Voltage Stability and Current Collapse Suppression in AlGaN/GaN MOS-HFETs. (Under the direction of Dr. Veena Misra).

Owing to a high critical electric field and high electron mobility, GaN based lateral Heterojunction Field Effect Transistors (HFETs) are sought after for high voltage power and RF applications. But, device reliability continues to be a critical challenge to be overcome before successful commercialization. In this work, different dielectrics deposited by Atomic Layer Deposition are investigated for improving the threshold voltage stability and dynamic reliability of AlGaN/GaN based Metal-Oxide-Semiconductor-HFETs (MOS-HFETs). But more importantly, this work includes a first-of-its-kind comprehensive analysis of electrical characterization techniques and physics-based models required to evaluate and recommend any dielectric for mitigating surface trapping phenomena in the gate stack or the access-regions.

In an investigation of the impact of MOSHFET device structure on the efficacy of different methods for characterization of dielectric/AlGaN interface traps, it is found that the popular conductance method has a severely constrained detection limit when the AlGaN barrier offers high resistance to the de-trapping electrons. A capacitance-based method is immune to the issue of barrier resistance, but is still restrictive in its range. To improve the range and accuracy of trap detection, a novel pulsed-IV-based methodology is developed and demonstrated to be applicable for detecting both shallow and deep traps.

Identical electrical thickness of different high-k and low-k ALD dielectrics are evaluated for gate leakage and magnitude and stability of threshold voltage. It is established that the high-k dielectrics (Al_2O_3, HfO_2 and HfAlO) harbor a high density of shallow traps at the dielectric/AlGaN interface. In contrast, ALD SiO_2, annealed in N_2 at 700°C, creates a very low density of interface traps ($< 2\times10^{12}$ cm^{-2}) and is an excellent candidate for a gate dielectric. It provides strong gate leakage suppression, minimal threshold voltage shift and highly reliable ON-state characteristics.

With the use of physics-based simulation models, it is identified that the leakage at the surface of the AlGaN, whether through the passivation dielectric bulk or the dielectric/AlGaN interface, must be minimized to restrict the formation of a “virtual gate” and minimize current collapse. An optimal passivation dielectric must also create a high density of shallow interface donor traps to quicken the de-trapping of electrons from the “virtual gate” and the recovery of the channel underneath.

In order to create a high density of shallow interface donor traps a thin ALD HfAlO film is used. Surface leakage is also minimized by capping with a thick layer of PECVD SiO_2 and annealing in N_2 at 700°C. The effectiveness of the resulting optimal dual dielectric passivation stack in mitigating current collapse and ensuring contact isolation is also demonstrated.

Therefore, the optimal ALD dielectrics for a reliable gate stack and access-region passivation in an AlGaN/GaN MOSHFET are identified to be SiO_2 and HfAlO, respectively, annealed at 700°C in N_2.

© Copyright 2014 by Narayanan Ramanan

All Rights Reserved

Investigation of ALD Dielectrics for Improved Threshold Voltage Stability and Current Collapse Suppression in AlGaN/GaN MOS-HFETs

by
Narayanan Ramanan

A dissertation submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Electrical Engineering

Raleigh, North Carolina
2014

APPROVED BY:

Dr. Veena Misra Committee Chair	Dr. John Muth
Dr. Griff Bilbro	Dr. Zlatko Sitar

DEDICATION

"We are always surrounded by ignorance at some level or another. If you are going to assign God to that ignorance and you lose your curiosity to investigate it, solutions will always elude you."

- Neil deGrasse Tyson

in *The Inexplicable Universe with Neil deGrasse Tyson*

Dedicated to all my teachers and, in particular, my gurus of Physics, Prof. R. Ananthan and Mr. C. S. Ravi Shankar, who nurtured my curiosity to investigate and never give up.

Prof. R Ananthan

Mr. C. S. Ravi Shankar

BIOGRAPHY

Vita:

1986	Born in Chandigarh, India
Aug. 2004 – July 2009	B. Tech in Electrical Engineering,
	M. Tech in Power Systems and Power Electronics,
	Indian Institute of Technology-Madras, Chennai, India
Aug. 2009 – Sep. 2014	Ph.D. in Electrical Engineering,
	North Carolina State University, Raleigh, NC, USA

Publications:

[1] N. Ramanan, B. Lee and V. Misra, "Comparison of Methods for Accurate Characterization of Interface Traps in GaN MOS-HFET Devices," to be submitted to *IEEE Trans. Electron Devices*, Sep 2014.

[2] N. Ramanan, B. Lee and V. Misra, "ALD Dielectrics for Improved Gate Stack and Passivation Reliability of AlGaN/GaN MOS-HFETs in power Applications," to be submitted to *IEEE Electron Device Lett.*, Sep. 2014.

[3] N. Ramanan, B. Lee and V. Misra, "Device Modeling for Understanding AlGaN/GaN HEMT Gate Lag," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2012-2018, June 2014.

[4] N. Ramanan, B. Lee and V. Misra, "A Novel Methodology using Pulsed-IV for Interface of Border Traps Characterization on AlGaN/GaN MOSHFETs," *IEEE 26th Int. Symp. On Power Semiconductor Devices and IC's (ISPSD)*, Hawaii, pp. 366-369, 15-19 June 2014.

[5] C. Kirkpatrick, B. Lee, N. Ramanan and V. Misra, "Flash MOS-HFET operational stability for power converter circuits," *physica status solidi (c)*, vol. 11, no. 3-4, pp. 875-878, April 2014.

[6] B. Sarkar, N. Ramanan, S. Jayanti, N. Di Spigna, B. Lee, P. Franzon and V. Misra, "Dual Floating Gate Unified Memory MOSFET with Simultaneous Dynamic and non-volatile operation," *Electron Device Lett.*, vol. 35, no. 1, pp. 48-50, Dec. 2013.

[7] N. Ramanan, B. Lee, C. Kirkpatrick, R. Suri and V. Misra, "Properties of atomic layer deposited dielectrics for AlGaN/GaN device passivation," invited in *Semiconductor Sci. Technology*, vol. 28, no. 7, pp. 074004, 2013.

[8] N. Ramanan and V. Misra, "Multivalued Logic using a Novel Multichannel GaN MOS Structure," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1379-1381, 2011.

[9] N. Ramanan, S. Khatchadourian, J-C. Prevotet and L. Kessal, "Neural Network Hardware Architecture for Pattern Recognition in the HESS2 Project," *Proceedings of European Symposium on Artificial Neural Networks*, Bruges, Belgium, 23-25 April 2008. Available. [Online]. https://www.elen.ucl.ac.be/Proceedings/esann/esannpdf/es2008-107.pdf

ACKNOWLEDGMENTS

There are some things in life beyond your grasp of understanding. Fate is one among them. Some people call it coincidence, others providence. Whatever it is, I am thankful to all the good souls who have helped me through my journey and contributed one way or another in making my stay at NCSU a fulfilling experience.

My first thanks are due to the J. N. Tata Endowment for helping finance my first semester at NCSU. I may not have taken the big step of studying abroad, if not for them.

I am deeply indebted to my advisor Dr. Veena Misra, for having faith in me and providing me the opportunity to work on this exciting research project. She has been a great mentor, always lending a keen ear to my troubles and offering her guidance, all the while letting me choose my own path. She is undeniably, my role model of a dedicated scientist who is also a great human being.

I would like to also thank Dr. John Muth, Dr. Griff Bilbro and Dr. Zlatko Sitar for serving on my committee and offering critical comments and feedback. Special thanks go to Dr. Bongmook Lee and Dr. Casey Kirkpatrick for introducing me to the weird world of GaN and providing all the training I needed for device fabrication and characterization. Dr. Lee has always been my first 'go-to' person whenever I have had trouble in my research, and somehow, he almost always has an answer to everything!

I express my sincere appreciation to the staff members of the NCSU Nanofabrication Facility (NNF) and the Shared Materials Instrumentation Facility (SMIF) at Duke University. Without their dedicated efforts in keeping the cleanroom facilities functional, I would have gone nowhere. ☺ I would also like to acknowledge the help and support of my past and present group members Dr. Srikant Jayanti, Dr. Rahul Suri, Dr. Steven Novak, Xiangyu Yang, Steven Mills, Michael Lim and Biplab Sarkar. A lot of my work is inspired from discussions we have shared regarding device physics, processes and characterization

techniques. They have also been hugely responsible for maintaining all our lab equipment with sincere dedication.

Although I express my sincere gratitude to Dr. Rama Vetury for giving me the opportunity of working with him as an intern at RFMD, Charlotte, NC, I only wish I had more time to spend under his mentorship. His PhD dissertation, submitted in 2000 at UC Santa Barbara, was instrumental in giving me insights of the phenomenon of current collapse in GaN, which is also the main focus of this work. I learnt a lot about the GaN industry during my short time at Charlotte, but there is still so much more to learn from him.

There is no way I can fully repay the unconditional love and affection showered by parents and my “motherly” sister. I am also blessed with caring cousins, uncles and aunts who never stop appreciating and encouraging all my endeavors. For some unknown reason, they all have blind faith in whatever I do. ☺ I hope I have done them justice with this work.

I have made a lot of friends in Raleigh and cherished some of my best moments with them here. Most notably, the Sivaji gang, with Dr. Vikram Seshadri and Dr. Rajagopal Panchapakesan. We rocked! And I hope we continue our good run in the future. I have a lot of fond memories of the times with my roommates, Dr. Vikram Seshadri and Dr. Mahendra Dia, and have learnt a lot from them. Special thanks also go to Vinodh Kotipalli, Ayush Jain, Biplab Sarkar and Amir Hassani for ‘tolerating’ me through this time. I would also like to thank Dr. Gayatri Venugopal, Anirudh Venugopal, Bharath Sampath, Sudarshan Nallan Chakravarthy, Sahil Dahiya, Sudarshan Prasad, Vivek Devarajan, Srikrishna Gopu and Sankalp Nimbhorkar for making this place a home, away from home. I also owe gratitude to Dr. Vijay Srinivasan and his wife Jayalakshmi Narasimhan for offering me their beautiful home to stay and peacefully write my dissertation during the final stages of my stay.

Finally, I would like to express my gratitude to Dr. Paul Maki, at the Office of Naval Research (Award No. N00014-11-1-0945), and National Science Foundation (Award No. ERC FREEDM EEC-08212121) for the funding and RFMD for some of the GaN substrates used in this work.

TABLE OF CONTENTS

LIST OF TABLES……………………………………………………......x
LIST OF FIGURES……………….. xi

CHAPTER 1 : Introduction...1
1.1 Overview of GaN based electronics market 1
1.2 Background of lateral GaN device physics.. 6
1.3 Technical challenges to lateral GaN device adoption.. 8
1.3.1 Challenges associated with access regions 9
1.3.2 Challenges associated with gate stack 12
1.4 Key technological solution: Dielectrics deposited by Thermal Atomic Layer Deposition 14
1.5 Dissertation goals and organization 14

CHAPTER 2 : Experimental Methods 16
2.1 Transistor Fabrication 16
2.1.1 Substrate properties.. 16
2.1.2 Atomic Layer Deposition (ALD) process 17
2.1.3 HFET fabrication flow 18
2.1.4 MOSHFET fabrication flow 20
2.2 Characterization Equipment... 21
2.2.1 Cascade probe-station 21
2.2.2 DC I-V and LCR meters 23
2.2.3 Pulsed-IV meter 23

CHAPTER 3 : Methods for Accurate Characterization of Interface Traps in GaN MOSHFET Devices 26
3.1 Introduction... 26
3.2 Background... 28
3.2.1 Fabrication Flow 28
3.2.2 Simulation Framework... 28
3.2.3 Equivalent small-signal circuit model 31
3.3 Theoretical Comparison of Interface Trap Characterization Methods 33
3.3.1 Conductance Method 34
3.3.2 Capacitance Method... 37
3.3.3 Pulsed-IV Method... 39
3.3.4 Inferences.. 42
3.4 Experimental Demonstration of Accurate Interface Trap Characterization 43
3.4.1 Introduction... 43
3.4.2 Quasi-steady state characterization.. 45

3.4.3 Trap density measurement 45
3.4.4 Trap depth estimation 47
3.4.5 Final trap density profile reconstruction and validation 49
3.5 Summary 49

CHAPTER 4 : Characterization of Traps at ALD Dielectric/AlGaN Interface 51
4.1 Introduction 51
4.2 Sample preparation 51
4.3 Extraction of gate stack capacitance 52
4.4 Interface traps at ALD HfO_2/AlGaN interface 53
4.5 Interface traps at ALD HfAlO/AlGaN interface 54
4.6 Interface traps at ALD Al_2O_3/AlGaN interface 55
4.7 Interface traps at ALD SiO_2/AlGaN interface 56
4.8 Interface traps at PECVD silicon nitride/AlGaN interface 57
4.9 Summary 60

CHAPTER 5 : ALD Dielectrics for Gate Stack 61
5.1 Introduction 61
5.2 Dielectric/AlGaN gate stack leakage 61
5.2.1 Introduction 61
5.2.2 Gate leakage trends 62
5.3 ON-state gate stack reliability 63
5.4 MOSHFET threshold voltage 65
5.4.1 Influence of gate dielectric on threshold voltage 65
5.4.2 Threshold voltage trends 66
5.5 Summary 69

CHAPTER 6 : Role of Surface Passivation for Improved Access-Region Reliability 71
6.1 Introduction 71
6.2 Gate-lag measurement: A window into surface trapping 72
6.3 Impact of passivation dielectric on gate-lag 73
6.3.1 Introduction 73
6.3.2 Preliminary experiment 1 74
6.3.3 Preliminary experiment 2 76
6.3.4 Preliminary conclusions 76
6.4 Device Modeling for Understanding AlGaN/GaN HEMT Gate-Lag 77
6.4.1 Introduction 77
6.4.2 Simulation Framework 78
6.4.2.1 Background 78
6.4.2.2 Model development 79
6.4.2.3 Gate-lag simulation 82

6.4.3 Modeling results 82
6.4.3.1 Passivation dielectric 82
6.4.3.2 Barrier material properties 89
6.4.3.3 HFET structure 91
6.5 Summary 93

CHAPTER 7 : ALD Dielectrics for Access-Region Reliability 94
7.1 Introduction 94
7.2 ALD dielectrics for HFET passivation 95
7.3 ALD dielectrics for MOSHFET passivation 97
7.3.1 Drain stress measurements 98
7.3.2 Gate-drain isolation 102
7.4 Summary 102

CHAPTER 8 : Conclusions and Future Work 104
8.1 Conclusions 104
8.2 Future Work 108

REFERENCES 110

LIST OF TABLES

Table 1.1: Material parameters of Si, SiC and GaN. Figures of Merit are normalized with respect to Si [4], [5]. 4

Table 1.2: Key advantages of thermal ALD over other techniques for this dielectric reliability investigation. 13

Table 2.1: Properties of the AlGaN/GaN substrates used in this work. 16

Table 2.2: ALD deposition conditions used for different dielectrics. 18

Table 3.1: Parameters used for the MOS-HFET TCAD simulations. 30

Table 3.2: Summary of the pros and cons of different trap characterization methods: conductance (GV), capacitance (CV), pulsed-IV (PIV) and a combination of PIV and GV (PIV+GV). 43

Table 4.1: Thickness of different layers of the fabricated MOSHFETs. 52

Table 4.2: Minimum total measured density of traps for different dielectrics and annealing conditions. 59

Table 5.1: Interface and bulk charge densities extracted for different ALD dielectrics from measured values of threshold voltage from Figure 5.5 using (5.2). 69

Table 8.1: Simplistic comparison of performance of different ALD dielectrics evaluated in this work for use as a gate dielectric or as a thin passivation dielectric in a dual dielectric stack. 108

LIST OF FIGURES

Figure 1.1: Typical voltage and current ratings of different electrical systems in use around us. 2
Figure 1.2: Simplified sketch of the typical transient waveforms of current, voltage and power loss in a power switch. 3
Figure 1.3: Comparison of ideal specific ON-resistance between different material systems over breakdown voltage. 5
Figure 1.4: Simple schematic of an AlGaN/GaN based HFET and MOSHFET. 6
Figure 1.5: Crystal structure at the interface between AlGaN and GaN. Also shown are the polarization components and the resulting equivalent fixed charge at the AlGaN barrier boundaries. 7
Figure 1.6: Conduction band diagram of an AlGaN /GaN HEMT device along the depth from the metal gate when the a) AlGaN barrier is thin, and b) AlGaN barrier is thick. Also shown is the resulting 2DEG at the AlGaN/GaN interface. 8
Figure 1.7: Simple schematic of an AlGaN/GaN based MOSHFET illustrating the locations of the gate stack and the access regions. 9
Figure 1.8: (a) Development of a virtual gate in an AlGaN/GaN HFET under the application of a high negative gate bias; (b) Typical current collapse between AC and DC, observed in an AlGaN/GaN HFET. 11
Figure 2.1: Simple schematic of the AlGaN/GaN substrates procured from vendors, as listed in Table 2.1. 17
Figure 2.2: (a) Cross-sectional schematic of the fabricated HFET device. L_{GD} = gate-drain spacing; L_G = gate length; L_{SG} = gate-source spacing. (b) Top view image of the fabricated line device. 19
Figure 2.3: Simple schematic showing the HFET fabrication flow. 20
Figure 2.4: Simple schematic showing the MOSHFET fabrication flow. 21
Figure 2.5: (a) Picture of the Cascade on-wafer probe station with heated chuck. (b) Image of a fabricated sample under measurement in the probe station. 22

Figure 2.6: Equipment used for DC IV, CV and GV measurements. 22
Figure 2.7: Picture of the custom built pulsed-IV setup with a Tektronix TDS-420 oscilloscope and two HP pulse generators (HP 8112A, HP 8116A) as the voltage sources. 25
Figure 2.8: Simple schematic of the custom built pulsed-IV setup with an oscilloscope and a pulse generator. 25
Figure 3.1: A cross section of the fabricated MOSHFET device with HfAlO gate dielectric. 27
Figure 3.2: Measured and simulated I_D-V_G curves for the fabricated MOS-HFET. 30
Figure 3.3: Energy band diagram under the MOS-HFET gate stack, illustrating the construction of the equivalent small-signal circuit. 32
Figure 3.4: Various representations of the MOS-HFET small-signal equivalent circuit: (a) same as Figure 3.3; (b) combines all the semiconductor components into an equivalent parallel capacitance and conductance, C_P and G_P; (c) represents the equivalent capacitance and conductance of the device as measured, C_m and G_m. 32
Figure 3.5: Conductance, G_P/ω, calculated for the circuit model in Figure 3.4a over a range of barrier resistance values, for two different trap densities: (a) 5×10^{12} cm^{-2} eV^{-1}; (b) 10^{13} cm^{-2} eV^{-1} 35
Figure 3.6: (a) Trap density, D_{it}, and (b) error in the response time, τ, estimated from the peak positions and values of the tallest peaks of the calculated conductance in the frequency range 1 Hz - 1 MHz. 35
Figure 3.7: TCAD simulation results of the conductance method on the MOS-HFET device with different interface trap densities distributed uniformly in energy: estimated trap density (a) without and (b) with AlN layer; error in the estimated trap response time (c) without and (d) with AlN layer. 36
Figure 3.8: Schematic showing the extraction of the gate voltage shift, ΔV_f, of the second CV step in Figure 3.2b, for the capacitance method of extracting interface trap density. 38

Figure 3.9: (a) Trap density estimated using TCAD simulations of the capacitance method for the barrier with/without the AlN layer. The lowest detectable trap density was $\approx 3\times10^{12}$ cm^{2} eV^{-1}. (b) Trap density estimated using (3.9) with capacitance calculated with the circuit model in Figure 3.4a. 39
Figure 3.10: Energy band diagram under the MOS-HFET gate stack (with donor traps) at an applied quiescent gate voltage, $V_{G,Q}$, with an interface charge n_{it}. 41
Figure 3.11: (a) Trap density estimated using TCAD simulations of the pulsed-IV method for the barrier with/without the AlN layer. (b) Contour plot of error in estimated D_{it} as a function of the channel resistance, R_G, and the estimate of the device series resistance, R_S. 42
Figure 3.12: (a) CV measured from 0V to -10V at 1 MHz under UV; (b) GV measured at room temperature and 200°C with a drain voltage of 0.2V. 44
Figure 3.13: (a) Two transient pulse measurements, under UV, at quiescent gate voltages of 3V and -2V and a fixed V_{ON} (for time T_{ON}). (b) S-D conductance measured at 1 µs into the measurement pulse at V_{ON} over a quiescent gate voltage, $V_{G,Q}$, sweep with a hold time of 1 s. 46
Figure 3.14: Trap density extracted using (3.12) from the S-D conductance values measured in Figure 3.13b. 46
Figure 3.15: (a) Extracted GPω curves and curve-fits for different applied quiescent gate voltages at 23°C; (b) Trap depth extracted using the peak position of the conductance curves.. 47
Figure 3.16: Plot of the constructed trap depth and the rate of band bending curves over different gate voltages. 48
Figure 3.17: (a) Trap density experimentally estimated using a combination of pulsed-IV and conductance methods vs. trap depth. (b) Plot of the estimated rate of band bending vs. estimated trap density. 48
Figure 4.1: Lines show the interface trap density detected at the ALD HfO_2/AlGaN interface using pulsed-IV method for different anneal conditions.................................... 53

Figure 4.2: Lines show the interface trap density detected at the ALD HfAlO/AlGaN interface using pulsed-IV method for different anneal conditions. 54
Figure 4.3: Lines show the interface trap density detected at the ALD Al_2O_3/AlGaN interface using pulsed-IV method for different anneal conditions. 55
Figure 4.4: Conductance curves obtained at 200°C with the MOSHFET having ALD Al_2O_3 gate dielectric after a 700°C PMA. 56
Figure 4.5: Lines show the interface trap density detected at the ALD SiO_2/AlGaN interface using pulsed-IV method for different anneal conditions. 57
Figure 4.6: Lines show the interface trap density detected at the PECVD silicon nitride/AlGaN interface using pulsed-IV method for the as-deposited condition. 58
Figure 4.7: Conductance curves obtained at 200°C with the MOSHFET having PECVD silicon nitride gate dielectric in the as-deposited state. 59
Figure 4.8: Bar graph showing the minimum total measured density of traps for different dielectrics and annealing conditions from Table 4.2. 60
Figure 5.1: Best case gate leakage curves measured for different dielectrics in Table 4.1 with identical EOTs. 62
Figure 5.2: Gate leakage (I_G-V_G) measured for the MOSHFETs with ALD dielectrics, before and after anneals as described in Table 4.1: (a) SiO_2; (b) Al_2O_3; (c) HfO_2; and (d) HfAlO. 63
Figure 5.3: DC I_D-V_G curves measured for the following MOSHFETs, at low V_{DS}: HfAlO after 700°C PMA, HfO_2 after 600°C PMA, Al_2O_3 after 700°C PMA, SiO_2 after 700°C PMA and PECVD Si_3N_x as-deposited. 64
Figure 5.4: Threshold voltage, V_T, extracted using the linear extrapolation method on I_D-V_G curves at low V_D, for different dielectrics and two different annealing conditions listed in Table 4.1. 67
Figure 5.5: Threshold voltage of MOSHFETs with dielectrics of varying thickness after a PMA at 400°C, extracted using CV curves in UV vs. equivalent oxide thickness (EOT) of the gate dielectric. 67

Figure 6.1: A sketch showing an HFET device cross section and the trapping phenomena during a gate lag measurement. 71

Figure 6.2: Experimental transient drain current, in symbols, and gate voltage, normalized to their respective dc values, for an HFET device (on GaN-SiC_2 wafer, Table 2.1) before and after passivation with 200 nm of PECVD SiO_2. 72

Figure 6.3: A sketch of the generic AlGaN/GaN HFET structure, with large negative gate voltage. Current paths $I_{SURFACE}$ (along the AlGaN surface) and $I_{SCHOTTKY}$ (Schottky leakage under the gate) constituting the total gate leakage are also illustrated. 73

Figure 6.4: Gate-lag curves for HFET fabricated on GaN-SiC_2 wafer (Table 2.1) with a passivation stack comprising 10 nm ALD HfAlO and 200 nm PECVD SiO_2.... 75

Figure 6.5: Gate-lag curves for HFETs fabricated on GaN-SiC_2 wafer (Table 2.1) with different passivation dielectrics: 8 nm ALD Al_2O_3, 10 nm ALD HfAlO and 200 nm PECVD SiO_2. 76

Figure 6.6: Sketch of the generic AlGaN/GaN HEMT structure under investigation. Most simulation results in this section use these device parameters unless mentioned otherwise. 79

Figure 6.7: (a) Sketch of the critical physical models required to obtain a realistic simulation of gate-lag. (b) Sketch of the simplified physical models adopted in this work. 79

Figure 6.8: Measured gate-lag curves from the HFET at stage 4 in subsection 6.3.2. (a) Enhancement in recovery owing to PF field-enhanced emission with higher drain voltages. (b) Enhancement in recovery with higher ON gate voltages. 81

Figure 6.9: Gate-lag for devices simulated with different passivation dielectric bulk resistivities, ρ, in the structure shown in Figure 6.6.. 83

Figure 6.10: Electron concentration versus distance along the AlGaN/GaN interface at $V_{G,DC}$ = -8 V for passivation dielectrics of different resistivities. 84

Figure 6.11: Electron density evolution with time along the AlGaN/GaN interface after the removal of $V_{G,OFF}$. 84

Figure 6.12: Gate-lag for different surface trap energies. 85
Figure 6.13: Gate-lag simulated for traps at two different trap energies in the same device. 86
Figure 6.14: Gate-lag versus dielectric constant of the passivation dielectric. 86
Figure 6.15: (a) Conduction band profiles, for different passivation bulk resistivities, ρ , at the drain side edge of the gate, at $V_{G,OFF} = -8$ V. (b) Simulated gate leakage from the Schottky gate ($I_{SCHOTTKY}$, tunneling across AlGaN barrier) and the sides ($I_{SURFACE}$, through the passivation dielectric). 88
Figure 6.16: Gate-lag simulated for different Al concentrations in the AlGaN barrier layer. 89
Figure 6.17: Simulated gate-lag versus AlGaN barrier thickness. [76] © 2014 IEEE. 90
Figure 6.18: (a) Gate-lag measured for HFETs fabricated on GaN-SiC_1, GaN-SiC_2 and GaN-Sap substrates with different barrier properties mentioned in Table 2.1. (b) Gate-lag for HFETs simulated with the same AlGaN barrier properties and using lateral dimensions from Figure 6.6. 90
Figure 6.19: Gate-lag simulated for different values of L_{GS} and L_{GD}. 92
Figure 6.20: Gate-lag simulated for different values of L_G. 92
Figure 7.1: Gate-lag for HFETs with a double stack of 8 nm ALD SiO_2 and 200 nm PECVD SiO_2 as passivation, with and without PDA (at 600°C and 700°C). 95
Figure 7.2: Gate-lag for HFETs with a double stack of 8 nm ALD Al_2O_3 and 200 nm PECVD SiO_2 as passivation, with and without PDA (at 600°C and 700°C). 96
Figure 7.3: Gate-lag for HFETs with a double stack of 8 nm ALD HfAlO and 200 nm PECVD SiO_2 as passivation, with and without PDA (at 600°C and 700°C). 97
Figure 7.4: Waveforms illustrating a new drain voltage stress reliability measurement methodology using a Keithley 4200 DC measurement setup. 99
Figure 7.5: I_D-V_G sweep measurements at the end of each drain stress, illustrated in Figure 7.4, on a MOSHFET with Al_2O_3 gate and passivation dielectric, after post-metallization annealing at 700°C. L_G = 9 µm, L_{SG} = 4 µm and L_{GD} = 12 µm. . 100

Figure 7.6: Recovery time, t_r, measured for different MOSHFETs as $0.3\times\Delta V_T$ s. Stress measurements were performed after PMA at 700°C in the case of ALD SiO_2, ALD Al_2O_3 and ALD HfAlO and 600°C in the case of ALD HfO_2. The MOSHFET with PECVD Si_3N_x gate dielectric was not annealed. 100
Figure 7.7: Percentage of current collapse with respect to a fresh device, measured at V_G = 0V during the I_D-V_G sweep after each drain stress. 101
Figure 7.8: OFF-state (a) gate and (b) drain leakage measured over a drain voltage sweep for different MOSHFETs with L_{GD}=12 μm. 101

CHAPTER 1: Introduction

1.1 Overview of GaN based electronics market

According to an analysis by the Lawrence Livermore National Laboratory and the Department of Energy, of the total raw energy from many resources, almost 55% was wasted due to conversion and transmission losses in the US alone in 2009 [1]. Conversion losses from petroleum usage in transportation constituted almost half of this wasted energy, while the rest was primarily losses in electricity generation and transmission. With diminishing stable oil reserves and surging oil prices, governments are increasingly promoting the use of "green" energy like solar and wind power. Further, they are also providing tax breaks promoting the use of hybrid and electric vehicles, due to which their popularity is on a steady rise today. All these measures are introduced with the belief that electricity, however generated, is a much more controllable source of power that can be more efficiently utilized for any utility. Since these developments are bound to increase the contribution of electricity in the overall share of the energy market in the future, there is a rapidly rising demand for innovation in the power electronics industry to minimize the losses in power generation, conversion and transmission by enabling higher voltage operation at minimum losses.

The variety of electrical systems in use today is optimized for best efficiency at different voltage and current levels. Power transmission is typically at high voltages in order to minimize transmission losses. In contrast, due to issues of safety, most consumer electronics and electrical equipment run at much lower voltages. Figure 1.1 shows the ranges of voltage and current ratings of different electrical systems [2]. Power converter circuits perform the crucial role of interfacing between the wide variety of power supply systems and the load systems.

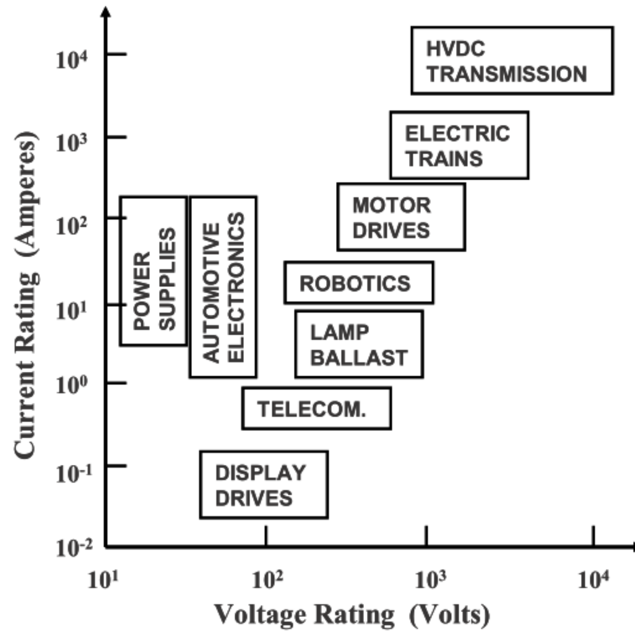


Figure 1.1: Typical voltage and current ratings of different electrical systems in use around us. [2] © 2008 Springer Science.

Any power electronic circuit which conditions power for a load consists of passive capacitive and inductive elements which store energy in the form of voltage $\left(E_{cap} = \frac{1}{2}CV^2\right)$ or current $\left(E_{ind} = \frac{1}{2}LI^2\right)$. The work horse of this circuit is a switch which is driven to convert one form of energy to another and produce the rated voltage and current for the load. While the capacitive and inductive elements can be, in principle, made lossless, the power loss in this circuit is dominated by losses in conversion between E_{cap} and E_{ind} through the power switch.

Figure 1.2 shows the typical waveforms of voltage, current and the power dissipated in a power transistor, used as the power switch. There are three main components of power loss in the switch during operation: ON state conduction loss, P_{ON}; OFF state isolation loss, P_{OFF}; and switching losses, $P_{SW,ON} + P_{SW,OFF}$. Typically, the OFF state isolation losses are orders of magnitude lower than the conduction or switching losses. The conduction loss can be reduced by a reduction in the ON state resistance of the device. Switching losses can be

minimized with a reduction in the voltage/current waveform transition times, ie. the responsiveness of the device to the drive voltage. A reduction in device switching time can also afford a higher operating frequency for the circuit, which affords a significant reduction in the size of the passive elements and the harmonic distortions in the output waveforms.

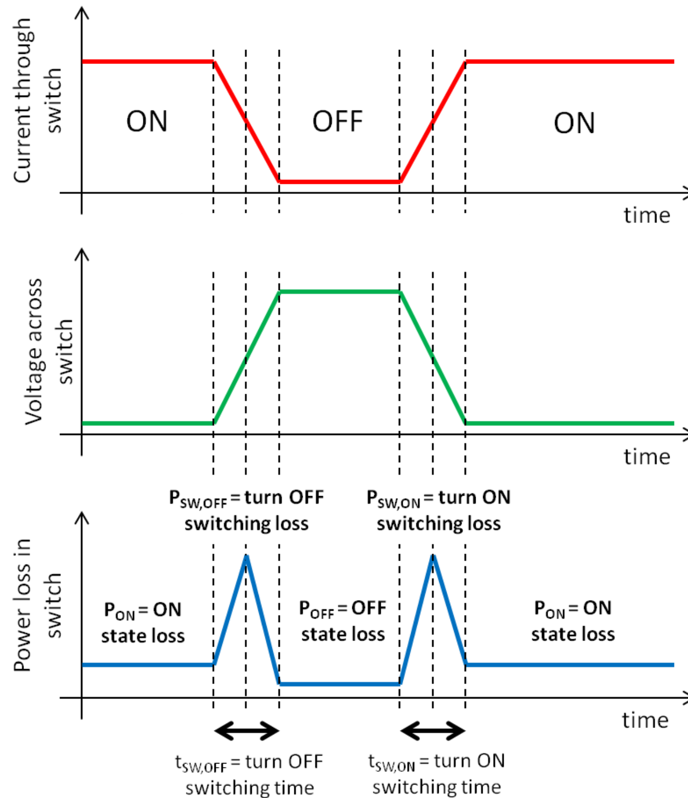


Figure 1.2: Simplified sketch of the typical transient waveforms of current, voltage and power loss in a power switch.

Silicon power devices have dominated the power electronics field from the 1950s with significant improvements introduced to push device efficiency to silicon's theoretical limits. The industry has migrated from the early bipolar transistors through thyristors and MOSFETs to insulated gate bipolar transistors (IGBTs) and super-junction MOSFETs. But in order to further improve performance, other material systems like SiC and GaN are being extensively

explored. Table 1.1 compares a few key material parameters of Si, SiC and GaN and shows that GaN outperforms the rest in the Baliga Figure of Merit (BFOM) for high voltage power operation, which applies to systems operating at lower frequencies where conduction losses are dominant [4]. GaN also outperforms the rest at the Baliga High Frequency Figure of Merit (BHFFOM) for high frequency operation, dominated by switching losses [5]. Unfortunately, fabrication of high breakdown voltage vertical GaN MOSFET devices is complicated by the difficulty in p-doping and sub-optimal inversion mobility along with the possibility of a high interface trap density at the dielectric/GaN interface [5]. In comparison, a lateral GaN High-Electron-Mobility-Transistor (HEMT) relies purely on electron transport along a channel at a high-quality hetero-interface, away from the surface. The presence of a high density 2-D electron gas at this high-mobility interface affords a further improved ideal specific ON-resistance, shown in Figure 1.3 [6]. A HEMT also requires ohmic contacts with electrons as majority carriers, which are relatively much simpler to form [5].

Table 1.1: Material parameters of Si, SiC and GaN. Figures of Merit are normalized with respect to Si [4], [5]. Values in '*' correspond to conduction at GaN hetero-structure interface.

	Si	*4H-SiC*	*GaN*
Band gap, E_g (eV)	1.1	3.3	3.4
Critical field E_C (MV/cm)	0.3	3	3.3
Saturation velocity ($\times 10^7$ cm/s)	1	1.8	1.5-2
Mobility μ ($cm^2 (V.s)^{-1}$)	1400	800	1000-2000*
Thermal Conductivity ($W (cm.K)^{-1}$)	1.5	4.9	1.5
BFOM ratio $\left(\propto \varepsilon\mu E_g^3\right)$	1	12	17-34*
BHFFOM ratio ($\propto \mu E_C^2$)	1	57	86-172*

While GaN substrates are significantly more expensive than Si, recent advances in the growth of GaN on large diameter Si substrates have cleared the path towards obtaining highly competitive and cheap GaN on Si wafers and lateral HEMT based power transistors on them. The GaN on Si epiwafer supplier base is also steadily increasing (Azzurro, DOWA,

NTT, EpiGaN, Soitec, etc.), indicating significant market competition. Therefore, while GaN HEMTs were originally considered for adoption in the high power high frequency RF market [4] (wireless base stations, military radar, etc.), they are now being positively considered for power device applications as well, by various manufacturers and developers like Avogy, EPC, Fujitsu, GaN Systems, International Rectifier, Micro GaN, NXP, POWDEC, RFMD and Transphorm. According to various market surveys and production cost estimates, GaN devices would provide the best performance/cost benefit for <900V power electronics applications and dominate the power supply and photo-voltaic inverter markets by 2019 [7], beside other markets like electric vehicles, industrial motor drives and wind turbines.

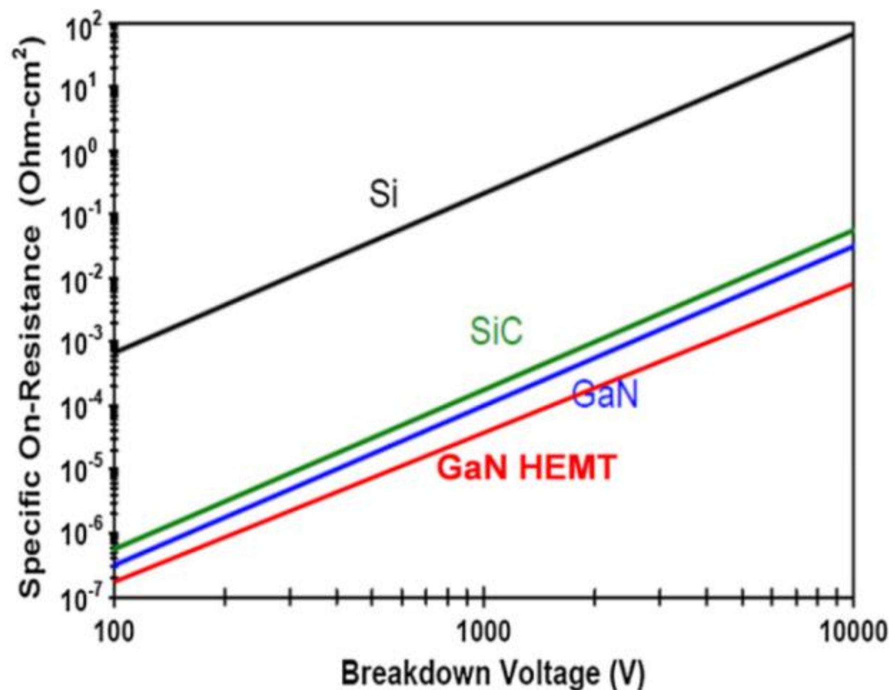


Figure 1.3: Comparison of ideal specific ON-resistance between different material systems over breakdown voltage [6].

1.2 Background of lateral GaN device physics

GaN is a III-V semiconductor with a band gap of 3.4 eV. Figure 1.4 shows the sketch of typical lateral AlGaN/GaN Heterojunction Field Effect Transistor (HFET) and Metal-Oxide-Semiconductor HFET (MOS-HFET) devices where the source and drain are connected with a 2-D Electron Gas (2DEG) channel, a part of which is controlled by a gate.

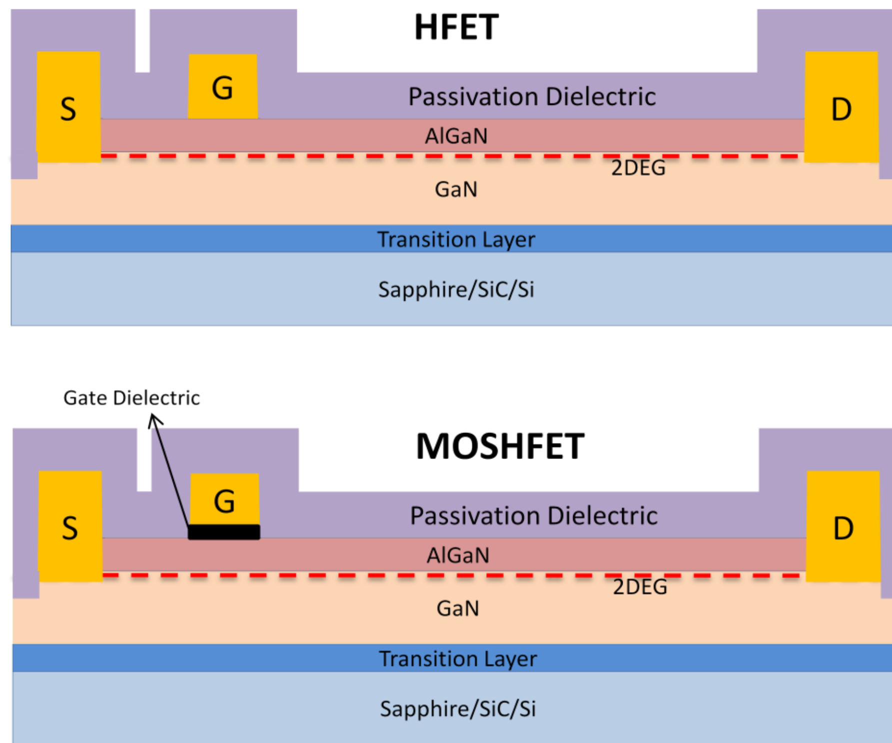


Figure 1.4: Simple schematic of an AlGaN/GaN based HFET and MOSHFET.

The Ga-face GaN and AlGaN crystal structure is polar in nature as shown in Figure 1.5. This manifests in the form of spontaneous (inherent) and piezo-electric (lattice strain induced) polarization along the c-axis in the direction out of the bulk substrate [4]. A significantly higher total polarization in the AlGaN barrier results in a higher inbuilt electric field and band bending in the AlGaN, with respect to the GaN. In the gate-drain and gate-

source access regions, the existence of a large number of surface states at the AlGaN surface, due to dangling bonds or surfacial oxides [8], pins the surface at the Fermi level. The resulting unoccupied surface donor states provide the equal and opposite positive charge to compensate for the 2-D electron gas (2DEG) that forms at the AlGaN/GaN hetero-interface. This helps maintain charge neutrality and a zero electric field outside of the AlGaN layer. For a very thin AlGaN barrier, these surface donors are completely filled and neutral, resulting in no channel formation as shown in Figure 1.6a [9]. Once the AlGaN thickness is increased beyond a critical point, when the surface donor level reaches the Fermi level, the electrons from the surface donors get transferred to the AlGaN/GaN interface forming the 2DEG channel, shown in Figure 1.6b.

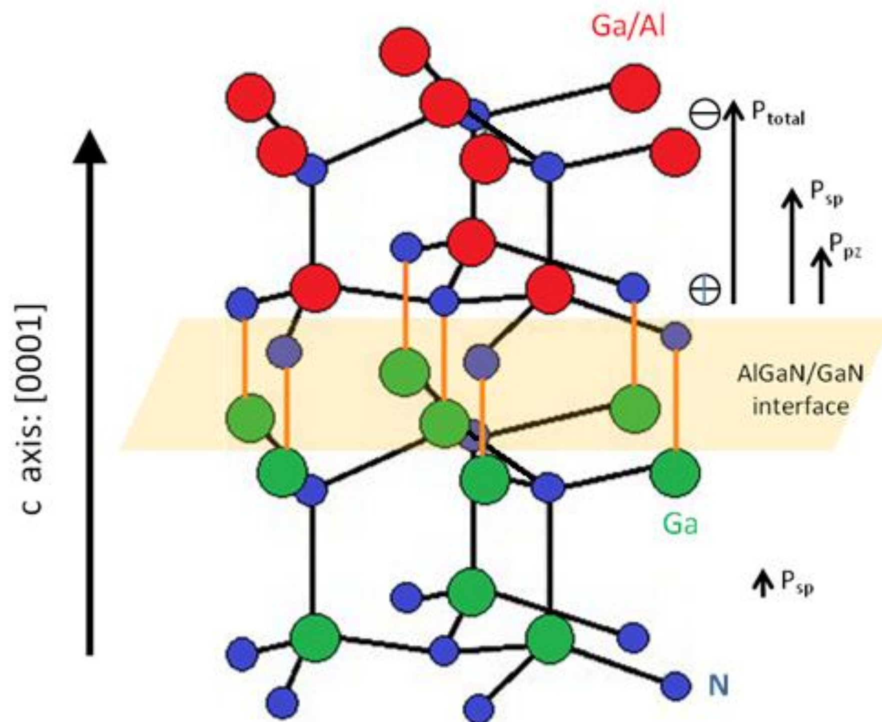


Figure 1.5: Crystal structure at the interface between AlGaN and GaN. Also shown are the polarization components and the resulting equivalent fixed charge at the AlGaN barrier boundaries [4].

The 2DEG concentration under the gate can be controlled by applying a gate voltage. Although, the threshold voltage (V_T) of the device can be controlled by choosing a gate metal of an appropriate work function, achieving a positive V_T, along with a high 2DEG in the access regions, with only the use of high work function metals, is very hard. Thus, the simple HFET device is normally-ON, i.e. a depletion mode device.

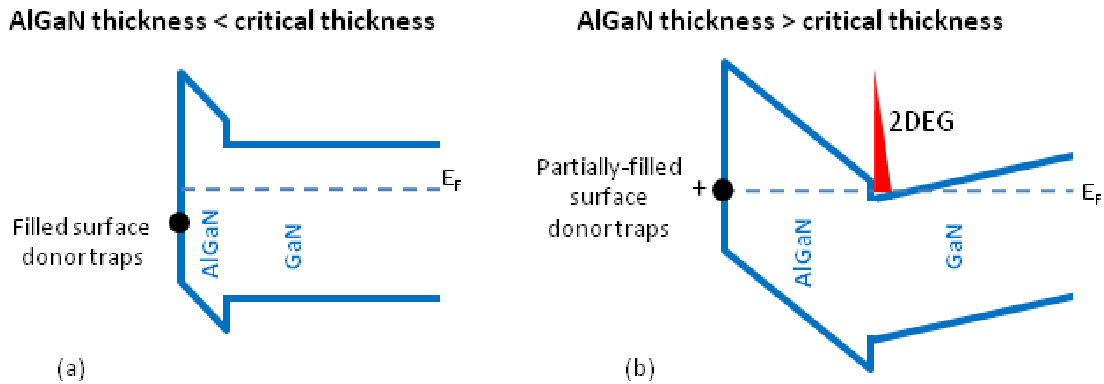


Figure 1.6: Conduction band diagram of an AlGaN /GaN HEMT device along the depth from the metal gate when the a) AlGaN barrier is thin, and b) AlGaN barrier is thick. Also shown is the resulting 2DEG at the AlGaN/GaN interface [9].

1.3 Technical challenges to lateral GaN device adoption

Replacing even the state-of-the-art Si power devices with GaN based power transistors can result in significant performance advantages like enabling higher frequency operation, minimizing power converter circuit losses and size, ability for higher operation temperature and radiation hardness. Despite these advantages, establishing **device operation reliability** is currently the most important concern for GaN HEMT manufacturers aiming to compete with the well-established Si super-junction MOSFET in the high power market and the Si and GaAs devices in the high power RF market. Several other associated issues also need solutions or “work-arounds” in order to propose lateral GaN devices as serious contenders to

displace Si power MOSFETs. Each of these issues can be tied to phenomenon in the gate stack or access regions, illustrated in Figure 1.7 and explained in subsections 1.3.1 and 1.3.2.

It is to be noted here that the primary focus of this dissertation is an investigation of the phenomena at the surface of the AlGaN or at the interface between a dielectric and the AlGaN. While issues due to the substrate bulk properties are also important, they are dependent on the substrate growth parameters. Since the AlGaN/GaN substrates used in this work are high quality substrates, obtained from commercial vendors like RFMD, KOPIN and AZZURRO, reliability issues due to the AlGaN/GaN bulk or the buffer layers are not emphasized.

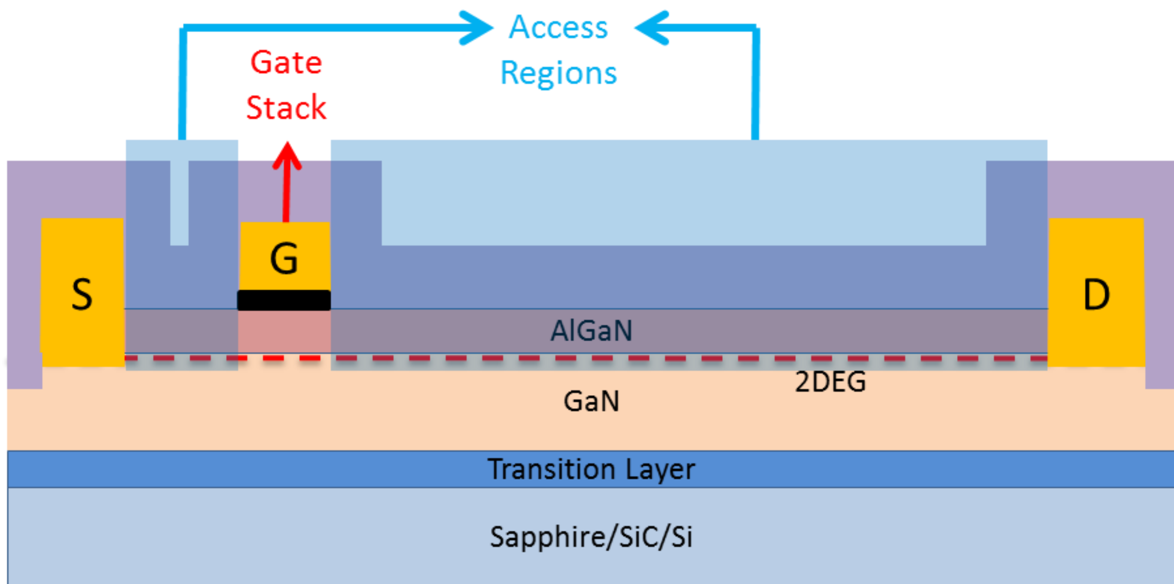


Figure 1.7: Simple schematic of an AlGaN/GaN based MOSHFET illustrating the locations of the gate stack and the access regions.

1.3.1 Challenges associated with access regions

Variation in the device characteristics during operation is detrimental to the performance of any circuit. Lateral GaN devices suffer from gate or drain-voltage stress-induced, short-term reversible and long-term irreversible degradation of drain current. The

sharp edges of a rectangular gate create a region of high electric field, especially at the drain side of the gate. This high field stress can result in long-term irreversible degradation of the barrier morphology via TDDB (Time Dependent Dielectric Breakdown) or inverse-piezo effect [10], [11], [91], [92]. Short term reversible current collapse (Figure 1.8b) is the degradation of the drain current during ac operation, compared to DC [4], [12]. *This phenomenon is called "current collapse".* The primary cause of this degradation has been found to be the formation of a "virtual gate" in the access regions (Figure 1.7a), especially near the drain edge of the gate, due to the trapping of electrons in the donor states at the AlGaN surface [12]. A gate, with a high negative voltage, can supply electrons which can migrate through the passivation dielectric bulk [18] or hop at the passivation dielectric/AlGaN interface [19] and get trapped at the surface traps. The resultant reduction of the surface positive charge leads to the reduction of the 2DEG density, in order to maintain electrostatic equilibrium. After the removal of the negative voltage, this reduction of the access-region 2DEG results in a temporarily degraded R_{ON}. This recovers slowly as the electrons detrap from the surface states. The increase in the device response time to a gate turn-ON pulse significantly increases the switching losses and reduces the efficiency of the power converter.

Silicon nitride is commonly used as a passivation dielectric as it is known to significantly reduce "current collapse" associated with surface traps [13]. To this effect, unconventional dielectrics like Teflon that keep ambient moisture away, have also been proposed [36]. Leakage through the dielectric bulk and at the dielectric/AlGaN interface [18], [37] has been found to play a crucial role in improving/worsening current collapse behavior.

Compared to ambient air, silicon nitride has a high dielectric constant (> 6) [14]-[16]. It has also been predicted that passivation dielectrics with a lower dielectric constant can further reduce current collapse by reducing the access region fields and potentially minimizing ionization of air [17]. (A lower passivation dielectric constant can also afford a lower parasitic gate capacitance and an improved power gain cut-off frequency, f_{max}, for RF applications.) Additionally, field plates are often used to further reduce the surface electric

fields at the gate edge and reduce current collapse [35]. While all such methods of device structure engineering can help, the exact role of the passivation dielectric bulk, dielectric/AlGaN interface and the substrate material properties are still unclear. *Thus, a critical investigation into the impact of the device structure and the material properties of the passivation dielectric bulk, dielectric/AlGaN interface and the substrate is needed. Further, the proposal of a passivation dielectric that minimizes current collapse and has a lower dielectric constant than silicon nitride is also desired.*

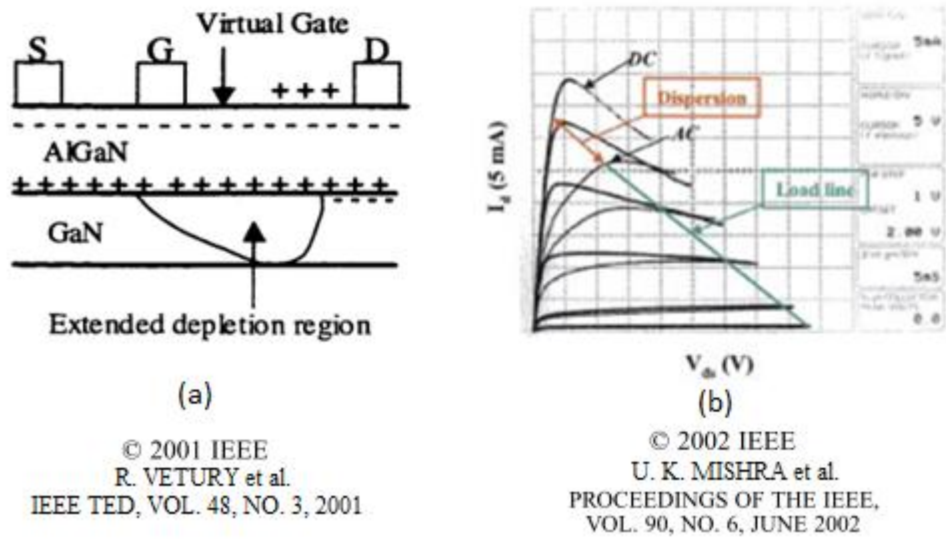


Figure 1.8: (a) Development of a virtual gate in an AlGaN/GaN HFET under the application of a high negative gate bias [12]; (b) Typical current collapse between AC and DC, observed in an AlGaN/GaN HFET [4].

In order to provide serious competition to Si MOSFETs, *a passivation dielectric must not degrade the breakdown voltage inherently afforded by the AlGaN/GaN system.* A passivation dielectric that minimizes surface trapping and current collapse by minimizing surface leakage is also generally expected to provide an improved breakdown voltage. This is because a shorter virtual gate reduces the field at the edge of the drain and results in a more moderate field distribution near the drain edge of the gate [20].

1.3.2 Challenges associated with gate stack

Gate leakage via trap-assisted-tunneling is promoted by the presence of high electric fields at the drain edge of the gate. The high field and the injection of high energy electrons from the gate can generate or enhance defects at certain sites along the edge. These defect sites, in turn, can further enhance gate leakage and thus, eventually, lead to premature permanent breakdown of the device [10], [21], [91], [92]. The insertion of an additional thin dielectric between the gate and the AlGaN has been observed to reduce gate leakage by orders of magnitude [22]-[26]. Such a reduction in gate leakage is expected to significantly delay the onset of time-dependant-dielectric-breakdown (TDDB) mechanism and improve the life of the device. An AlGaN/GaN MOSHFET device has already been demonstrated by Fujitsu Inc. to provide more than 100 W output power with a lifetime exceeding a million hrs [27]. Additionally, for power applications, a reduced forward bias gate leakage is very useful as it provides a larger positive gate bias window to maintain the device in an overdrive (ON) state and potentially, further reduce ON resistance.

While there is a critical need to use a gate dielectric for the AlGaN/GaN system, identifying the right dielectric becomes a significant challenge due to the factors highlighted herewith.

1. A high conduction band offset between the dielectric and AlGaN is required to minimize tunneling and thermionic current, dominated by electron transport. A high dielectric constant material helps maintain good gate control over the channel and is especially useful for smaller gate lengths which help reduce R_{ON} and gate charge. Typically, a material with lower dielectric constant has a higher band gap. But, a higher band-gap may not imply a high band offset with AlGaN. *Hence, a trade-off exists in choosing a relatively higher dielectric constant material with a reasonably high band offset for the gate dielectric.*
2. The gate dielectric may host positive charge in the dielectric bulk or at the dielectric/AlGaN interface. Additionally, donor traps at the dielectric/AlGaN interface

may act as positive charge, when unoccupied. The presence of positive charge can shift the threshold voltage in the negative direction. Circuit designers prefer to use an enhancement mode normally-OFF device with a positive threshold voltage. Such a device is inherently safer to operate in a power electronic circuit, in case of a failure. While the HEMT is inherently a normally-ON device*, the presence of a large density of donor traps or fixed positive charge can make even it harder to achieve normally-OFF operation* using other techniques like recessed gate [28], fluorine treatment [29], p-GaN gate [30], flash gate [31] or piezo-neutralization layers [32]. It is to be noted, though, that circuit approaches to normally-OFF operation like Cascode [33], [34] are increasingly being championed as a near-term solution to this issue. Transphorm [33] and International Rectifier [34] have already begun commercializing GaN HEMT technology for power applications with the Cascode architecture.

3. Traps in the dielectric bulk and at the dielectric/AlGaN interface can influence dynamic reliability, ie. threshold voltage instability, depending on their energy depth and response time. *It is critical to ensure that the gate dielectric minimizes the concentration of bulk and interface traps and provides a reliable ON state dynamic operation.*

Table 1.2: Key advantages of thermal ALD over other techniques for this dielectric reliability investigation. PVD = Physical Vapor Deposition; CVD = Chemical Vapor Deposition; ALD = Atomic Layer Deposition. RED = undesirable; YELLOW = moderately constrained; GREEN = desirable.

	Thin film thickness control	Plasma damage	Dielectric variety	Conformality and uniformity
PVD-Sputtering				
PVD-others				
Thermal Oxidation				
Low temperature CVD				
Plasma Enhanced CVD				
Plasma Enhanced ALD				
Thermal ALD				

1.4 Key technological solution: Dielectrics deposited by Thermal Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a thin film deposition technique that *provides monolayer control over the film thickness* and is well established in modern CMOS technology. It is similar in chemistry to chemical vapor deposition (CVD) except that in CVD the surface is exposed to both reactants at the same time whereas in ALD, only one reactant is present at a time. ALD film growth is self-limited and based on surface reactions, which makes monolayer growth control possible. The use of self-limited reactions means that ALD is surface-controlled process where process parameters other than the reactants, such as temperature, pressure and substrate, have little influence. This surface control guarantees *extremely conformal films, uniform in thickness* [38].

ALD can enable the exploration of a variety of high quality dielectrics, low-k and high-k, both for the gate and passivation, like Al_2O_3, SiO_2, HfO_2 and HfAlO. Since thermal ALD does not use plasma, there is no damage to the AlGaN surface during the dielectric deposition. Hence, the 2DEG density and mobility are not expected not deteriorate. Table 1.2 summarizes the advantages of thermal ALD over other methods in this reliability study.

1.5 Dissertation goals and organization

The goal of this dissertation is to identify the optimal ALD dielectrics for use in the gate stack and access-regions for reliable operation, primarily as a power switch. But, this process involves the development of some key experimental and modeling methods to improve the fundamental understanding of the physical phenomena at the AlGaN surface in the two regions.

CHAPTER 2 describes the details of the device fabrication flow and the equipment utilized for electrical characterization of the fabricated devices. All the experimental results examined in this work are based on the methods described here.

Any investigation of device reliability is incomplete without an investigation of traps at the dielectric/semiconductor interface. CHAPTER 3 is a critical investigation of techniques for electrical characterization of traps at dielectric/AlGaN interface in a MOSHFET device. Here, a new methodology is developed for accurate characterization of both shallow and deep traps at this interface. Subsequently, the method is successfully utilized for characterization of traps at different ALD dielectric/AlGaN interfaces in CHAPTER 4.

In CHAPTER 5, MOSHFET devices fabricated with different gate dielectrics are evaluated for gate leakage, ON-state dynamic reliability and threshold voltage performance. Along with critical inputs from the interface traps measurement in CHAPTER 4, a recommendation for an optimal gate dielectric is made.

CHAPTER 6 investigates the crucial role of the passivation dielectric in mitigating surface trapping phenomena for improved reliability of access regions. Armed with critical experimental gate-lag results, a sound simulation model to emulate surface leakage and surface trapping is developed. This is utilized to identify the requirements of the passivation dielectric, substrate and device structure to minimize current collapse.

In CHAPTER 7, using the recommendations of CHAPTER 6, a dual dielectric stack incorporating ALD dielectrics is evaluated for access-region passivation and contact isolation. Along with critical inputs from the interface traps measurement in CHAPTER 4, a recommendation for an optimal passivation dielectric stack is made.

The final conclusions of this work and recommendations for future work are provided in CHAPTER 8.

CHAPTER 2: Experimental Methods

2.1 Transistor Fabrication

This section presents the details of transistor fabrication. While subsections 2.1.3 and 2.1.4 provide an overview of the entire HFET/MOSHFET fabrication process flow, subsection 2.1.2 provides specific detail on the ALD process used for the dielectric deposition. The properties of the AlGaN/GaN substrates used in this work are provided in subsection 2.1.1.

2.1.1 Substrate properties

High quality AlGaN/GaN substrate wafers were procured from different vendors. Combinations of different substrates have been used for different sections of the work. Appropriate references are made in the dissertation to the specific wafers outlined in Table 2.1. Fig. 2.1 shows a schematic of a typical substrate which has a Si (111), sapphire or SiC carrier wafer with 1.5-2 μm of semi-isolating GaN. The barrier is composed of the following layers.

1. AlN layer to improve 2DEG carrier confinement with reduced alloy scattering [39], [40].
2. The undoped AlGaN layer which is the primary barrier material with polarization charge.
3. GaN cap layer, added to improve dynamic reliability of the HFET device [41], [42].

Table 2.1: Properties of the AlGaN/GaN substrates used in this work.

Wafer ID	*Substrate*	*Aluminium composition*	*Total barrier thickness*	*GaN cap thickness*	*AlN layer thickness*	*Substrate source*
GaN-SiC_1	GaN on SiC	23.5 %	25 nm	Unknown	Unknown	RFMD
GaN-SiC_2	GaN on SiC	21 %	27 nm	Unknown	Unknown	RFMD
GaN-Sap	GaN on sapphire	25 %	21 nm	2.5 nm	Unknown	KOPIN
GaN-Si	GaN on 1.5 mm Si	23 %	25 nm	4 nm	< 1 nm	AZZURRO

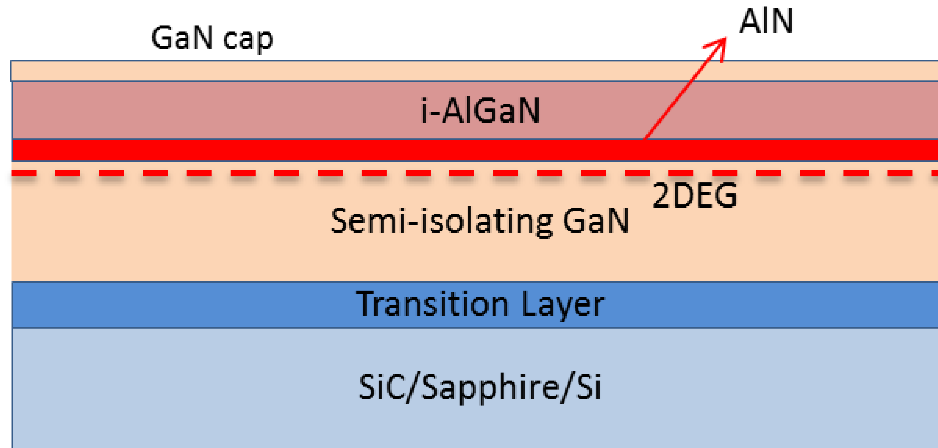


Figure 2.1: Simple schematic of the AlGaN/GaN substrates procured from vendors, as listed in Table 2.1.

2.1.2 Atomic Layer Deposition (ALD) process

In this work, ALD dielectric films were deposited in a commercial Savannah S100 system from Cambridge Nanotech. Details on the system and chamber design are available in [38] and [43]. The deposition process involves the repeated cyclic execution of four critical steps:

1. A metalorganic precursor compound is flown in the ALD chamber by an inert carrier gas like N_2. Sufficient time is provided for the precursor molecules to get chemisorbed on the hydroxylated/oxidized surfaces of the substrate. This is a self-limited reaction which stops once the entire surface is saturated by the precursor molecules.
2. The unreacted precursor molecules are purged out of the chamber.
3. An oxidizing precursor like water or ozone is flown into the chamber by the carrier gas. Given sufficient time, this precursor oxidizes the new surface and eliminates the organic ligand as a gaseous by-product.
4. The unreacted precursor and the gaseous by-products are purged out of the chamber.

Table 2.2: ALD deposition conditions used for different dielectrics.

Dielectric	*Metalorganic precursor*	*Oxidizing precursor*	*Metalorganic precursor cylinder temperature*	*Chamber temperature*
Al_2O_3	Tri-methyl Aluminium (TMA)	H_2O	23°C	200°C
HfO_2	Tetrakis-dimethyl-amino-hafnium (TDMAH)	H_2O	75°C	200°C
SiO_2	3-amino-propyl-triethoxy-silane (APTS)	H_2O, O_3	100°C	150°C

Depending on the reactivity of the metalorganic precursor, multiple oxidizing chemistries may be required to ensure completeness of the oxidizing step. Also, an optimization of the ALD process recipe is required to ensure sufficient precursor quantity and reaction time for each precursor step. This may also require heating the precursor cylinder to increase the vapor pressure. Details of the specific precursors and the recipe conditions used for different ALD dielectrics are provided in Table 2.2. Note that for a mixed dielectric like HfAlO, an HfO_2 cycle was followed immediately by an Al_2O_3 cycle.

2.1.3 HFET fabrication flow

Figure 2.2 shows a cross-sectional schematic and a top view image of the fabricated 100 μm wide HFET device. The HFET fabrication process is illustrated in Figure 2.3 and comprises of the processes explained here.

1. CLEAN: The sample is cleaned using solvents (acetone, methanol, iso-propylalcohol), followed by HCl (20% by volume) and HF (1% by volume). This clean process has been found to reduce the surface carbon and native oxide concentrations [38], [47].
2. OHMIC: A source-drain ohmic contact pattern is formed using deposition of Ti/Al/Ni/Au metal stack by RF-sputtering and e-beam evaporation followed by lift-off in NMP. The ohmic contact is formed by annealing the sample in a Rapid Thermal Anneal (RTA) furnace at 850 °C for 30 s in N_2 ambient.
3. ISO: Isolation is achieved by the formation of a mesa around the device using Reactive Ion Etching (RIE) with BCl_3 gas.

4. GM: The gate is formed by the deposition of TaN, capped with W, by RF-sputtering which is followed by lift-off in NMP.
5. PASS: Passivation dielectric is deposited by ALD or Plasma Enhanced Chemical Vapor Deposition (PECVD), as appropriate. The conditions for ALD dielectric deposition are specified in section 2.1.2. PECVD deposition is performed in an Advanced Vacuum Vision 310 PECVD system at a temperature of 250°C. Typical growth rates are 10 nm/min and 35 nm/min for silicon nitride and SiO_2, respectively.
6. CONTACT: Contact holes are etched through the passivation dielectric using Buffered Oxide Etch (BOE) wet-etch or RIE dry etch with BCl_3 gas.
7. ANNEAL: Annealing of the dielectrics are performed at temperature <= 700°C for 60 s in an RTA furnace in N_2 ambient, as needed. In case of the HFET, this anneal is also referred to as a post-deposition-anneal (PDA).

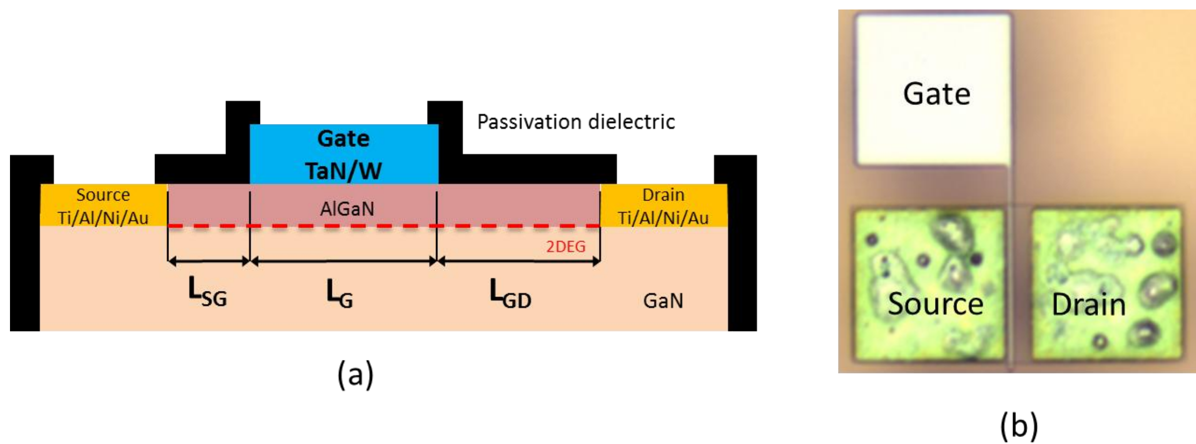


Figure 2.2: (a) Cross-sectional schematic of the fabricated HFET device. L_{GD} = gate-drain spacing; L_G = gate length; L_{SG} = gate-source spacing. (b) Top view image of the fabricated line device.

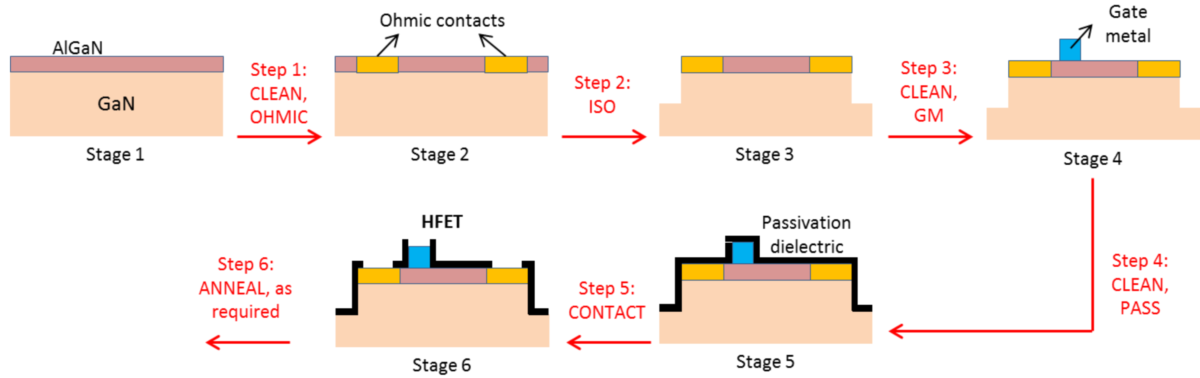


Figure 2.3: Simple schematic showing the HFET fabrication flow.

2.1.4 MOSHFET fabrication flow

The MOSHFET fabrication process is illustrated in Figure 2.4, with stages 1, 2 and 3 common as the HFET process flow in Figure 2.3. While the processes required here are the same as those listed in section 2.1.3, a few additional ones are listed here.

1. GD: The gate dielectric deposition is performed by ALD or PECVD, as appropriate.
2. ETCH: The dielectric is wet-etched by diluted HF or BOE.

The main difference here is that the fabrication of the gate stack involves two steps, 3a and 3b. Here, before the formation of the gate metal, a gate dielectric is deposited and annealed (PDA), if required. Next, there are two potential fabrication schemes. In scheme A, the gate dielectric is etched from the access regions and a new passivation dielectric is deposited. In scheme B, the gate dielectric is not removed and an additional passivation dielectric is deposited, as needed. An additional anneal, referred to as a post-metallization anneal (PMA), may also be performed at step 6, as required. The fabricated MOSHFET devices look similar to the HFET shown in Figure 2.2b and are 100 μm wide.

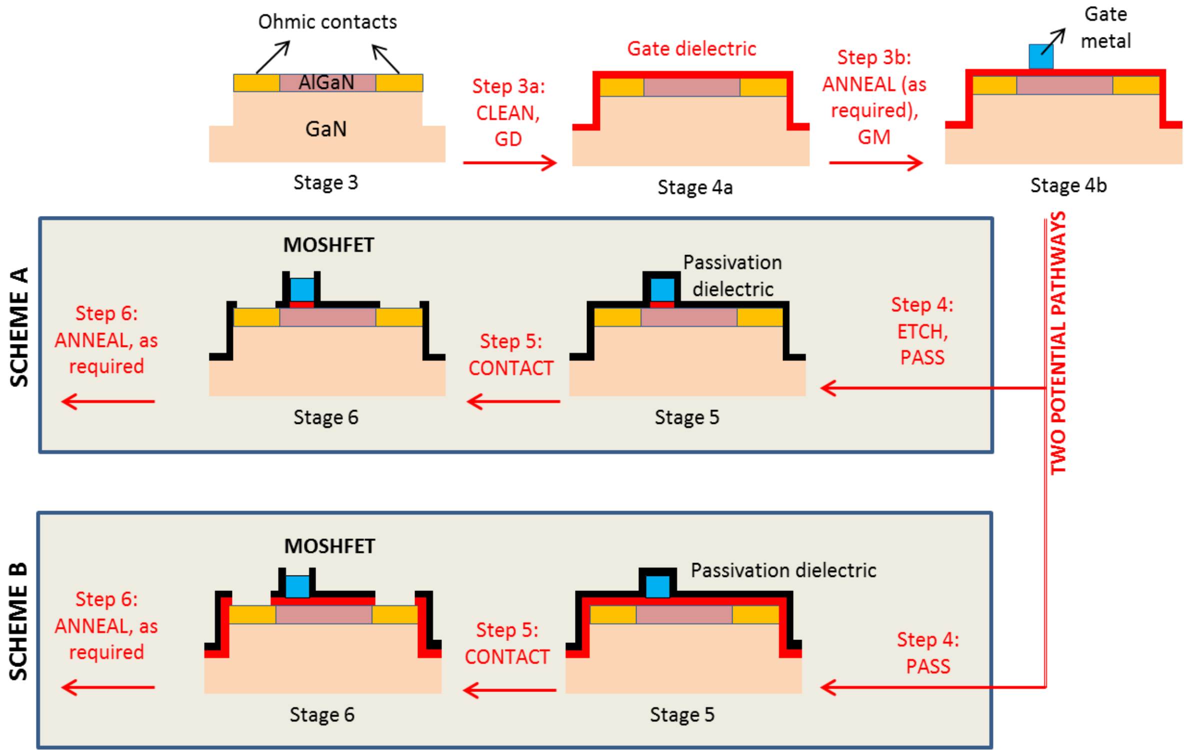


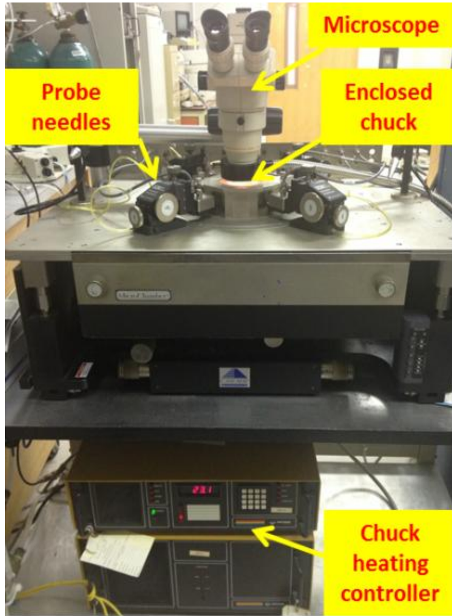
Figure 2.4: Simple schematic showing the MOSHFET fabrication flow.

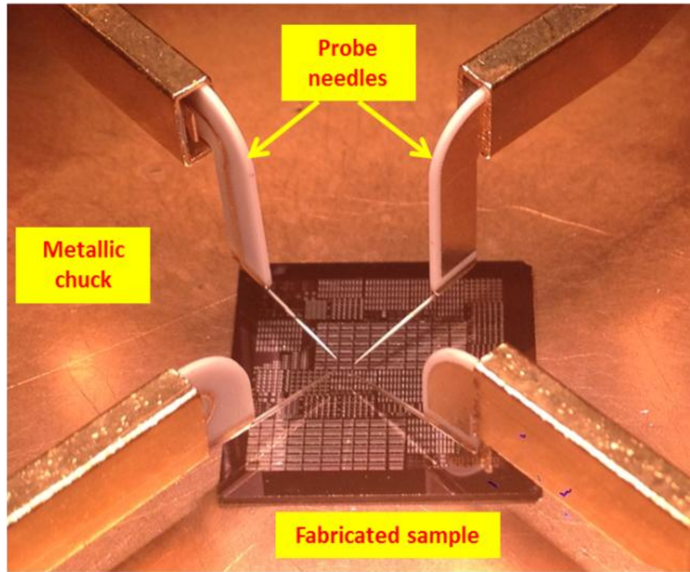
2.2 Characterization Equipment

In this section, details of the instrumentation used for characterization of the fabricated devices are presented.

2.2.1 Cascade probe-station

On wafer characterization of the fabricated devices is performed on a versatile Cascade probe station, shown in Figure 2.5a, which has a provision for a heated chuck (23°C - 250°C). The station is placed on a vibration-free air-table. Figure 2.5b shows an image of the probe needles, inside the enclosed chuck, which are capable of low noise gate leakage measurements (fA range). The station is also capable of high voltage measurements upto 200 V with a safety interlock capability.





(a) (b)

Figure 2.5: (a) Picture of the Cascade on-wafer probe station with heated chuck. (b) Image of a fabricated sample under measurement in the probe station.

Figure 2.6: Equipment used for DC IV, CV and GV measurements.

2.2.2 DC I-V and LCR meters

Figure 2.6 shows the equipment used for the DC current-voltage (IV), capacitance-voltage (CV) and conductance-voltage (GV) measurements. The Keithley 4200-SCS is a versatile IV measurement tool capable of 2 W of power with currents in the 10 pA - 100mA range and a maximum applied voltage of 200V. IV measurements are useful for evaluating the device transfer characteristics. This tool is also capable of applying stress currents/voltage (stress time > 500 ms) in conjunction with IV measurements. This is useful for high drain voltage stress measurements, discussed in subsection 7.3.1. The HP 4155b IV meter is capable of low noise gate leakage measurements with 10 fA resolution. CV and GV measurements are performed with an HP 4284 LCR meter, which is capable of measuring frequencies in the 20 Hz – 1 MHz range. These measurements are used for estimating layer thicknesses in the gate stack and for characterization of interface traps in section 4.3. A Keithley 8x8 line switching matrix makes it convenient to switch between different connections and equipment by software, for different measurements on the device under test, without manually altering the connections.

2.2.3 Pulsed-IV meter

At any applied bias voltage, a pulsed-IV meter measures the current response of the transistor to an applied voltage perturbation. In this work, we use a pulsed-IV meter to measure the source-drain current response to a gate voltage perturbation. These measurements are useful for reliability and interface traps characterization as explained in sections 3.3.3 and 6.2.

Figure 2.8 and Figure 2.8 show an image and a schematic of the custom built pulsed-IV measurement setup comprising of the following elements.

1. Gate pulse voltage source (HP 8112A): This instrument is used to apply a gate pulse train with a voltage range of (-16 V, 16V) and a resolution of 0.2 V. A rise time of 100 ns

ensures minimum ripple in the measured transient currents. The maximum pulse period is 990 ms.

2. DC drain voltage source (HP 8116A): While this instrument can be used to apply pulses as well, here it is used to apply a DC drain voltage in the range (-16 V, 16V) with a resolution of 0.2 V.
3. Source resistor: The use of a source resistor helps in making a low noise source voltage measurement and current estimation ($I_{SOURCE} = R_{SOURCE} * V_{SOURCE}$). The value of the source resistor, $R_{SOURCE} = 10\ \Omega$, is chosen to be much smaller than that of the transistor devices fabricated using the methods in Chapter 2 (> 50 Ω).
4. Oscilloscope (Tektronix TDS-420): A powerful oscilloscope with a full bandwidth of 50 MHz is used to acquire gate, drain and source voltage waveforms with a minimum time resolution of 1 ns and a 16-bit Analog-to-Digital-Converter (ADC) accuracy. Measurement error due to thermal noise at low voltages is reduced by averaging over multiple acquisitions of the gate pulse train.
5. Desktop computer: Custom designed software compiled with Visual C++ is used to control the oscilloscope and the voltage sources using GPIB interfaces and generate transient current waveforms or pulsed-IV curves. The software is capable of acquiring and stitching together waveforms over multiple timescales for high temporal resolution. Algorithms are built in to automatically estimate the required sense voltage range for maximum voltage/current resolution. Moving average filters are used to further improve measurement noise immunity.

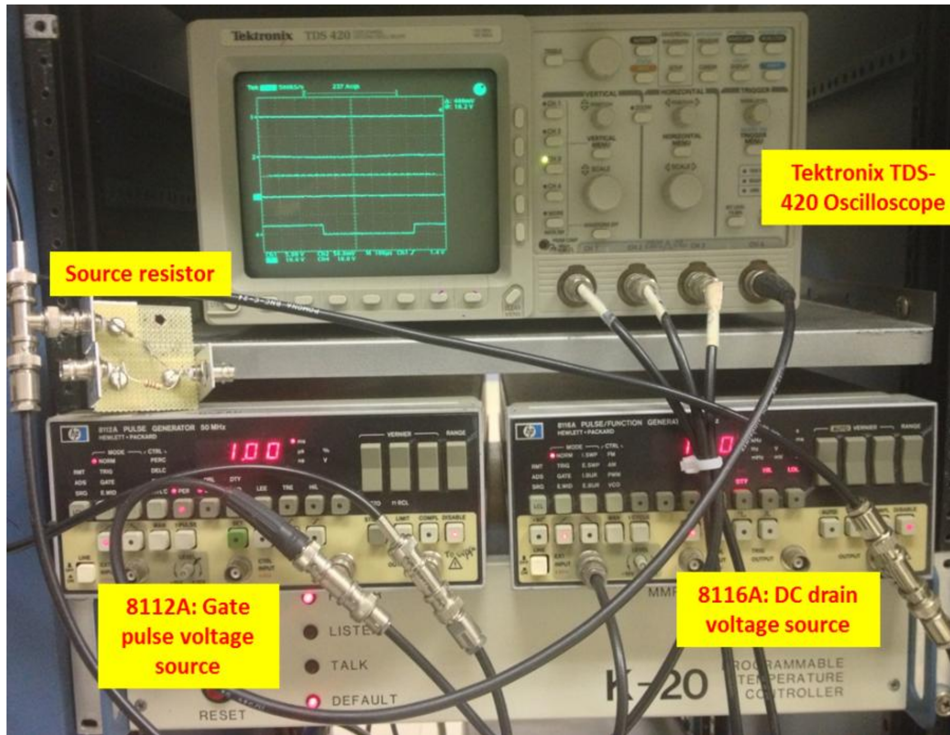


Figure 2.7: Picture of the custom built pulsed-IV setup with a Tektronix TDS-420 oscilloscope and two HP pulse generators (HP 8112A, HP 8116A) as the voltage sources. Also seen is a simple source resistor (10 Ω) for the source-drain current measurement.

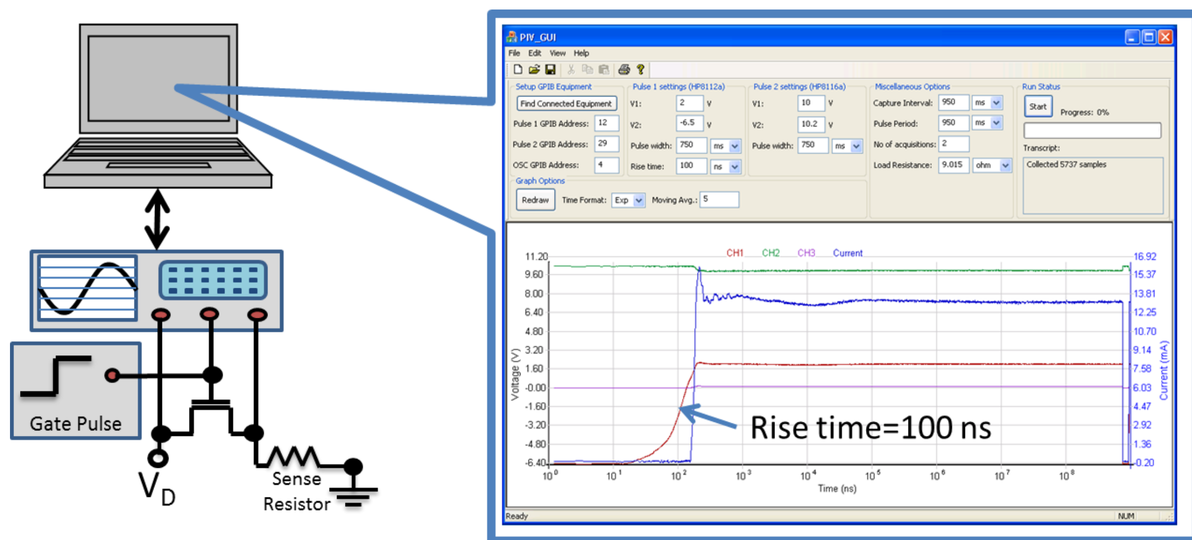


Figure 2.8: Simple schematic of the custom built pulsed-IV setup with an oscilloscope and a pulse generator. Also shown is the custom designed software graphical user interface on a PC to control the instruments and acquire the transient current response.

CHAPTER 3: Methods for Accurate Characterization of Interface Traps in GaN MOSHFET Devices

3.1 Introduction

High critical electric field with high electron mobility makes GaN-based Heterojunction-Field-Effect Transistors (HFETs) very attractive for high voltage power and RF applications [4]. But, reliability is a critical concern preventing their widespread adoption. Different dielectrics have been explored in the access region for surface passivation and improvement of dynamic reliability [44]-[47]. Further, gate dielectrics have been used to reduce gate leakage and improve long term reliability [25], [45], [48]-[50]. In either case, an accurate assessment of traps at the interface between the dielectric and the barrier material is necessary in order to evaluate the effectiveness and reliability of the dielectric.

At present, conventional methods of interface trap characterization using capacitance (CV) and conductance (GV) measurements are often replicated on the GaN MOS-HFET (Metal-Oxide-Semiconductor HFET) system [48]-[53]. These methods were originally developed for the SiO_2/Si MOS system where it was reasonable to assume relatively slow variations of trap capture cross-sections and energy distributions [54]. In contrast, dielectrics on III-V semiconductor systems have often shown very high and rapidly varying density of states and capture cross sections, especially near band edges [55]. Therefore, these methods are potentially prone to significant error when used on GaN. Being a wide bandgap system, additional care is needed to ensure that the sweep measurements are slow enough for deeper traps to achieve quasi-steady state before the ac measurement is taken. Most importantly, in the GaN MOS-HFET system, the dielectric/barrier interface that contains the traps responding to the ac voltage is separated from the barrier/GaN interface which hosts the 2-D

electron gas (2DEG) underneath. This structural difference compared to the SiO_2/Si MOS system behooves a critical investigation into the accuracy of these methodologies when used with the GaN MOS-HFET system.

Even at elevated temperatures, electrical measurements are restricted to probing shallow traps within ~1 eV away from the conduction band (E_C) [56]. In order to probe interface traps deeper in the barrier band gap, optical methods like Deep Level Optical Spectroscopy (DLOS) are often used [56]. In this chapter, a novel methodology to characterize dielectric/AlGaN interface and border trap density extraction is demonstrated using common electrical measurement techniques such as DC CV, IV and pulsed-IV. With the use of a generic ultra-violet (UV) lamp, this method can easily be used for accessing traps across the entire AlGaN band gap, without the need for sophisticated optical instrumentation that is typically required for DLOS. The method is demonstrated on a MOS-HFET device and a critical assessment of its accuracy in comparison to the traditional capacitance and conductance based techniques is conducted. Analytical models and TCAD simulations are used to theoretically compare the accuracy limits of capacitance, conductance and pulsed-IV techniques for the GaN MOS-HFET system. While AlGaN/GaN substrates are used for this work, the conclusions are easily translated to the InAlN/GaN system as well.

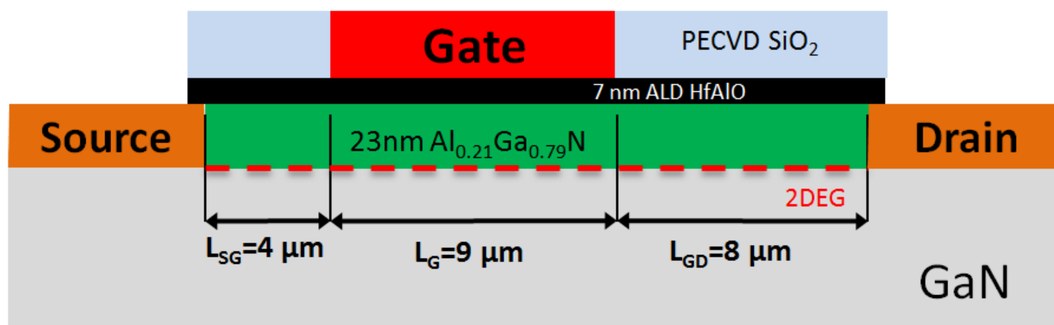


Figure 3.1: A cross section of the fabricated MOSHFET device with HfAlO gate dielectric.

3.2 Background

3.2.1 Fabrication Flow

MOS-HFET devices were fabricated on AlGaN/GaN on SiC substrate samples (GaN-SiC_1) with the SCHEME B fabrication flow specified in Figure 2.4. A 7 nm HfAlO dielectric deposited by thermal Atomic Layer Deposition was used as the gate dielectric. An additional 200 nm layer of PECVD SiO_2 was also added to improve device passivation. The dielectric received a post-deposition anneal (PDA) at 600°C for 60 s in a Rapid Thermal Anneal furnace in N_2 ambient. Subsequent IV and CV characterization was used for calibrating simulated curves, described in subsection 3.2.2. Figure 3.1 shows a cross-sectional view of the final device structure with a gate length of 9 μm and gate width of 104 μm.

3.2.2 Simulation Framework

The MOS-HFET device structure in Figure 3.1 was simulated with Synopsys Sentaurus TCAD. Fixed charge sheets of opposite polarities ($\pm 1.154\times10^{13}$ cm^{-2}) were used on either side of the AlGaN barrier to emulate the polarization charges. For ease of convergence, quantization and tunneling models were disabled and simple Fermi-Dirac statistics were used. A total donor trap concentration of 5.24×10^{13} cm^{-2} is placed at the HfAlO/AlGaN interface in order to match the threshold voltage (V_T = -7.8V) extracted from the DC I_D-V_G curve measured for the device, shown in Figure 3.2a. Figure 3.2b shows a good agreement between measured and simulated CV curves at the first CV step, near V_T. We also observe a shift of the second CV step towards more negative voltages with lower ac frequencies.

The value of the dielectric capacitance (C_{ox}), extracted at positive gate voltages corresponding to electron accumulation at the interface, is underestimated by about 15%. This has been experimentally observed before in other III-V material systems as well [55] and is attributed to the low conduction band density of states in GaN and AlGaN compared to

traditional Si. Errors in trap extraction due to the error in C_{ox} estimation can be minimized by extracting the C_{ox} from the accumulation or inversion capacitance on Si.

At gate voltages below V_T, traps at the dielectric/AlGaN interface are typically unoccupied. Since acceptor traps are neutral when unoccupied, their presence is expected to have negligible impact on V_T. In contrast, unoccupied donor traps act as positive charge, thereby shifting the V_T in the negative direction, as seen in Figure 3.2a. Since donor traps alone were found to sufficiently describe the IV and CV characteristics near both the CV steps, acceptor traps have not been considered in this work. Regardless, all the trap extraction methods considered here cannot distinguish between donor and acceptor traps and acceptor traps are expected to follow similar trends as the donor traps.

Most commercially available AlGaN/GaN substrates have an additional thin AlN layer at the AlGaN/GaN interface to increase 2DEG concentration and confinement and reduce interface alloy scattering [39], [40]. The incorporation of this layer can significantly affect the resistance of the barrier and alter the observed CV and GV characteristics, as will be explained in section 3.2.3. A realistic simulation requires the inclusion of tunneling models to accurately predict the barrier resistance for a given AlN layer thickness. But, since this work is a first order attempt at investigating the effect of the MOS-HFET structure on the efficacy of interface trap characterization methods, tunneling models have not been included. Hence, in simulations that include the AlN layer, the total barrier resistance is dominated by the high Schottky barrier on either side, and is therefore very large. The total barrier thickness was kept unchanged to ensure a constant barrier capacitance, C_B, throughout the study.

The matching at the second CV step in Figure 3.2b can be improved by incorporating a more sophisticated trap distribution in the simulation, closer to the measured distribution, as will be discussed in section 3.4. Also, while this simple CV simulation did not include the AlN barrier, a better model for the barrier resistance is required. All the parameters used for the simulations are listed out in Table 3.1.

It is to be noted here that rapid variations in interface trap density and trap capture cross-section are known to affect the accuracy of CV and GV based trap measurement techniques [54], [57], [59]. But, in this work, we focus on traps at a single energy level or uniformly distributed, along with a constant capture cross-section, to simplify the analysis of the effect of the MOS-HFET structure on trap estimation.

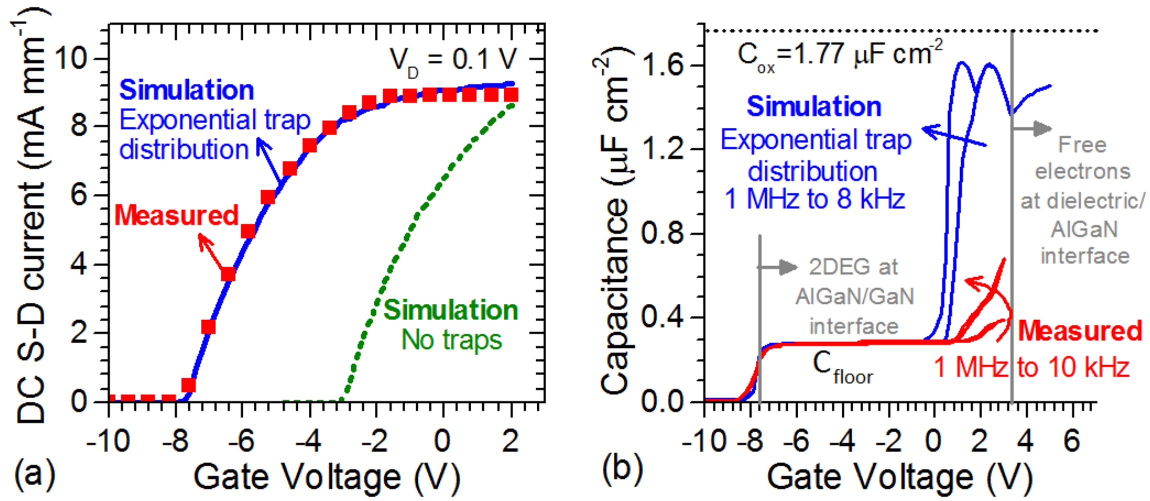


Figure 3.2: Measured and simulated I_D-V_G curves for the fabricated MOS-HFET. An exponential trap distribution was used, with the form D_{it}=1.6×10^{14} exp(-E_T/0.5), where E_T is trap depth in eV.

Table 3.1: Parameters used for the MOS-HFET TCAD simulations.

Parameter	*Value*
GaN bandgap (eV)	3.4 [53]
GaN electron affinity (eV)	3 [53], [57]
GaN electron mobility ($cm^2V^{-1}s^{-1}$)	1230
GaN buffer acceptor doping (cm^{-3})	1×10^{17}
Gate work function (eV)	4.6
Al percentage in AlGaN (%)	21
AlGaN thickness (nm)	23
AlGaN E_C density of states, 23°C (cm^{-3})	3.14×10^{18}
AlGaN electron mobility ($cm^2V^{-1}s^{-1}$)	400
AlN and AlGaN dielectric constant	9
Trap capture cross-section (cm^2)	1×10^{-17}
Electron thermal velocity (cm s^{-1})	2.6×10^7 [48]
MOS-HFET series resistance (Ω.mm)	6.45

3.2.3 Equivalent small-signal circuit model

An equivalent small-signal circuit model, illustrated in Figure 3.3, was developed for the AlGaN/GaN system based on the theory formulated in [54]. The circuit includes two paths: (a) the capacitive path; and (b) the trapped charge path. For simplicity, all the circuit models are derived for traps at a single energy level, E_T below E_C, with a characteristic response time given by (3.1).

$$\tau = \frac{\exp\left[-\frac{E_T}{k_B T}\right]}{\sigma v_{th} N_C} \tag{3.1}$$

Here σ is the trap capture cross-section, v_{th} is the electron thermal velocity and N_C is the density of states in the AlGaN E_C. The capacitance contribution due to trapped charge is given by $C_{it} = qD_{it}$, where D_{it} is the density of traps. The resistance contribution due to trapped charge, R_{it}, is derived from the characteristic response time as $R_{it} = \tau / C_{it}$ [52], [54]. Depending on the growth parameters, the barrier may also add an additional R-C impedance to the de-trapping electron path [52]. The barrier resistance R_B is negligible when the bulk AlGaN mobility is high and there is no AlN layer. But, in reality, it can be significantly higher, especially when the barrier includes an AlN layer. Additionally, while the parallel R-C impedance is expected to be a distributed R-C network, the circuit shown in Figure 3.3 and Figure 3.4a is a simplification.

Figure 3.4 shows reductions of the equivalent circuit into various representations, used for extracting the trap density. C_P and G_P in Figure 3.4b are the equivalent capacitance and conductance of the semiconductor. When $R_B \rightarrow 0$, they are expressed by (3.2), which are the same as those derived for n-Si MOS capacitor under depletion [54].

$$C_{P,0} = C_B + \frac{C_{it}}{1+(\omega\tau)^2}; \quad \frac{G_{P,0}}{\omega} = \frac{C_{it}\tau\omega}{1+(\omega\tau)^2} \tag{3.2}$$

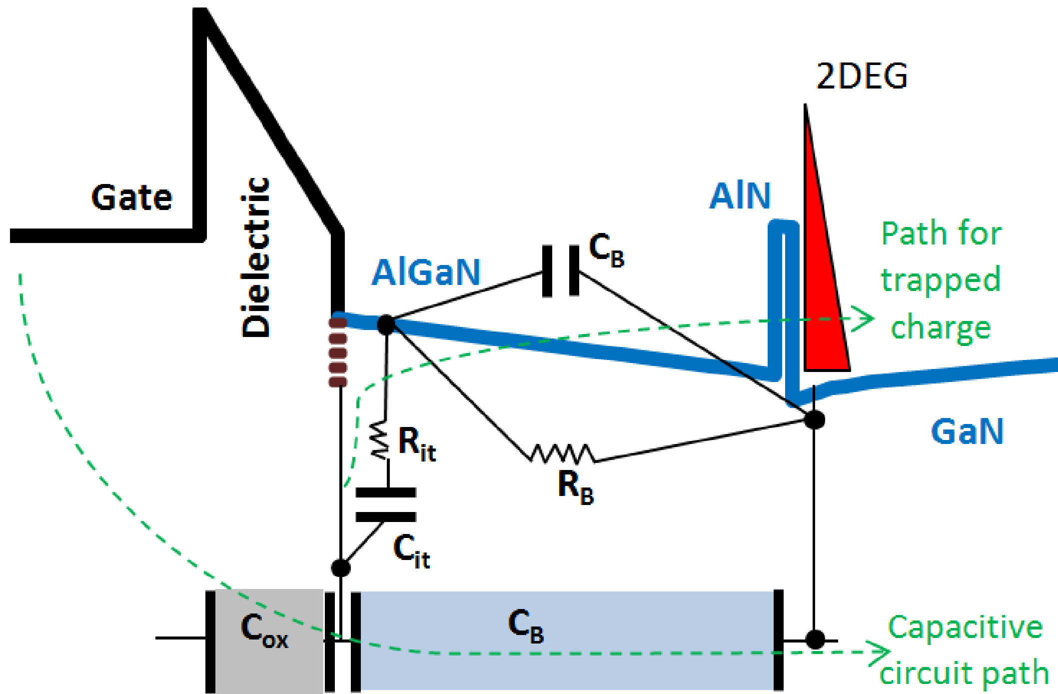


Figure 3.3: Energy band diagram under the MOS-HFET gate stack, illustrating the construction of the equivalent small-signal circuit.

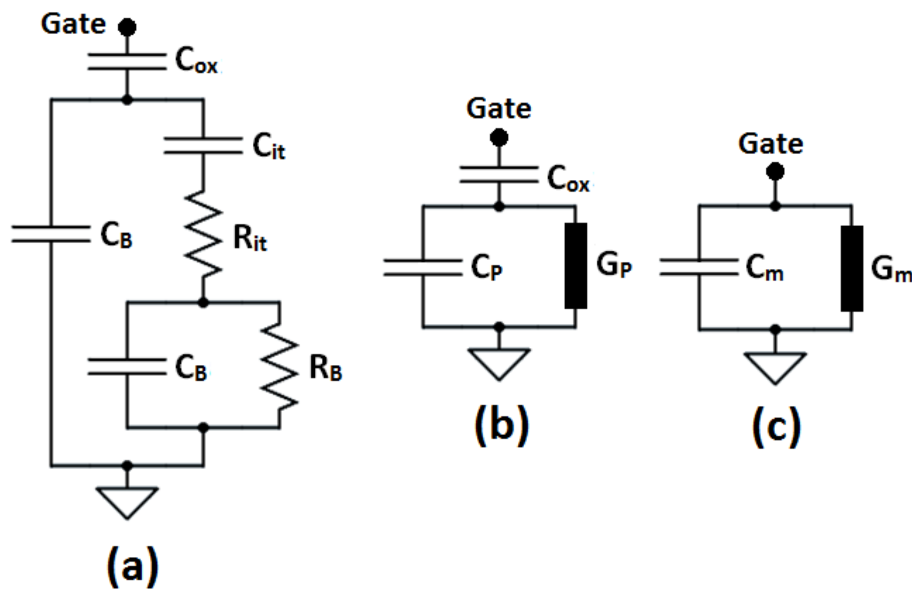


Figure 3.4: Various representations of the MOS-HFET small-signal equivalent circuit: (a) same as Figure 3.3; (b) combines all the semiconductor components into an equivalent parallel capacitance and conductance, C_P and G_P; (c) represents the equivalent capacitance and conductance of the device as measured, C_m and G_m.

The same equation is modified to (3.3) for a continuous trap distribution [54].

$$C_{P,0} = C_B + \frac{C_{it}}{\omega\tau}\tan^{-1}(\omega\tau);\ \frac{G_{P,0}}{\omega} = \frac{C_{it}}{2\omega\tau}\ln\left[1+(\omega\tau)^2\right] \tag{3.3}$$

When $R_B \rightarrow \infty$, a factor $\alpha = C_B/(C_{it} + C_B)$ is introduced to express C_P and G_P as (3.4).

$$C_{P,\infty} = C_B + \frac{\alpha C_{it}}{1+(\omega\alpha\tau)^2};\ \frac{G_{P,\infty}}{\omega} = \frac{\alpha^2 C_{it}\tau\omega}{1+(\omega\alpha\tau)^2} \tag{3.4}$$

Figure 3.4c represents the simplified equivalent circuit of the device during a CV or GV measurement. The equivalent semiconductor capacitance and conductance, C_P and G_P, can be extracted from the measured capacitance and conductance, C_m and G_m, using (3.5) and (3.6).

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}{}^2}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2} \tag{3.5}$$

$$C_P = C_{ox}\left[\frac{\omega^2 C_m (C_{ox} - C_m) - G_m{}^2}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2}\right] \tag{3.6}$$

3.3 Theoretical Comparison of Interface Trap Characterization Methods

Three popular methods for characterizing interface traps are investigated. The use of frequency dependence of CV curves for D_{it} extraction has been demonstrated in [50], [52]. Interface trap characterization using the frequency and amplitude of conductance peaks is very popular in Si MOS characterization and has been used with AlGaN/GaN MOS-HFETs in [48], [49] and [51]. The use of pulsed-IV measurements for traps characterization is demonstrated in section 3.4. In this section, equivalent small-signal circuit models derived in section 3.2.3 are used to predict accuracy limitations for the methods using CV and GV

measurements. For each method, simulations of the appropriate trap extraction measurements are also performed to confirm the predicted trends. A comparison between the trap concentrations set at the dielectric/AlGaN interface and the value extracted from the measurement simulation is used as an indicator of the accuracy expected from each method. Note that, *in this section, the terms 'measurement' or 'measured' refer to the simulation of the measurement*, unless specifically stated to be an experimental measurement.

3.3.1 Conductance Method

The conductance method is a very popular technique for traps characterization, especially with Si MOS [54]. This is because the peak value and peak frequency extracted from the fits of the semiconductor conductance with (3.2) or (3.3) can be directly used to calculate C_{it} and τ, and consequently D_{it} and E_T. This works well for the GaN MOS-HFET system also, but only if $R_B \rightarrow 0$. In reality, the value of R_B is higher, especially when there is an AlN layer sandwiched between the GaN and AlGaN. Therefore, in most situations, there is potentially a gross underestimation of D_{it}, unless it is corrected for. Figure 3.5 illustrates the effect of R_B on the frequency location and value of the conductance peak. For any given D_{it} with a certain characteristic time constant, two peaks are observed: the main peak corresponding to the interface traps at the dielectric/AlGaN interface, and the other an artefact due to the presence of C_B in the trapped charge path illustrated in Figure 3.4a. In cases of high R_B, the main peak of interest may well be pushed beyond the measurement frequency. As a result, the value of the secondary peak could be mistranslated into a constant D_{it} of C_B/q.

Figure 3.6a shows a contour plot of the extracted D_{it} by using the highest conductance peak in the measurement range of 1 Hz-1 MHz for a trap time constant $\tau=10^{-4}$ s. It is evident here that as R_B increases to large values, for a device with large D_{it}, the extracted D_{it} saturates at C_B/q, resulting in a large error of almost 3 orders of magnitude. Figure 3.6b shows a contour plot of the error in extracted trap response time, τ, indicating a wide swing of around

3 orders of magnitude in both faster and slower directions. The faster and slower time constants correspond to the secondary and the main peak, respectively.

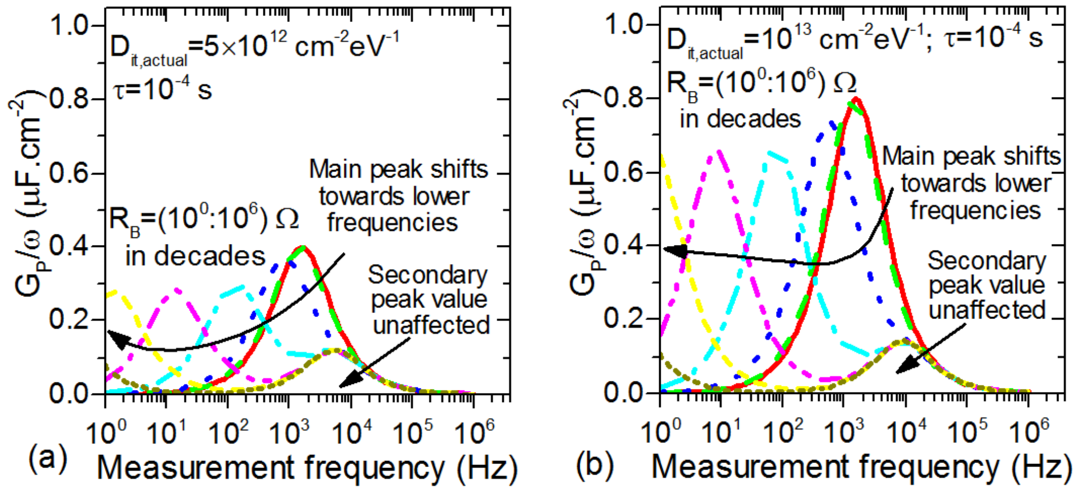


Figure 3.5: Conductance, G_P/ω, calculated for the circuit model in Figure 3.4a over a range of barrier resistance values, for two different trap densities: (a) 5×10^{12} cm^{-2} eV^{-1}; (b) 10^{13} cm^{-2} eV^{-1}. A representative trap characteristic response time of 10^{-4} s was chosen to obtain a main peak within the typical measurement frequency range of 100 Hz - 1 MHz.

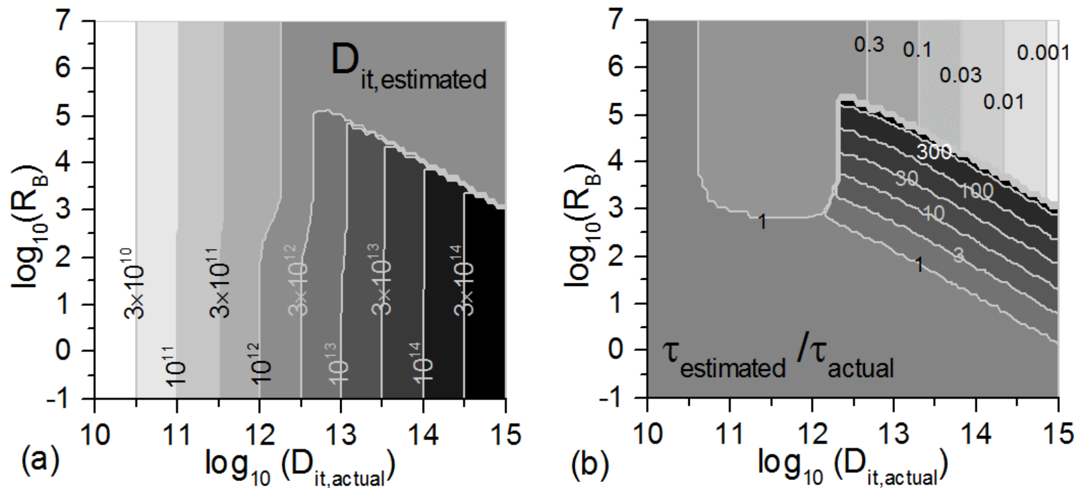


Figure 3.6: (a) Trap density, D_{it}, and (b) error in the response time, τ, estimated from the peak positions and values of the tallest peaks of the calculated conductance in the frequency range 1 Hz - 1 MHz. The contour plots are made over a range of actual trap density and barrier resistance values used for the circuit.

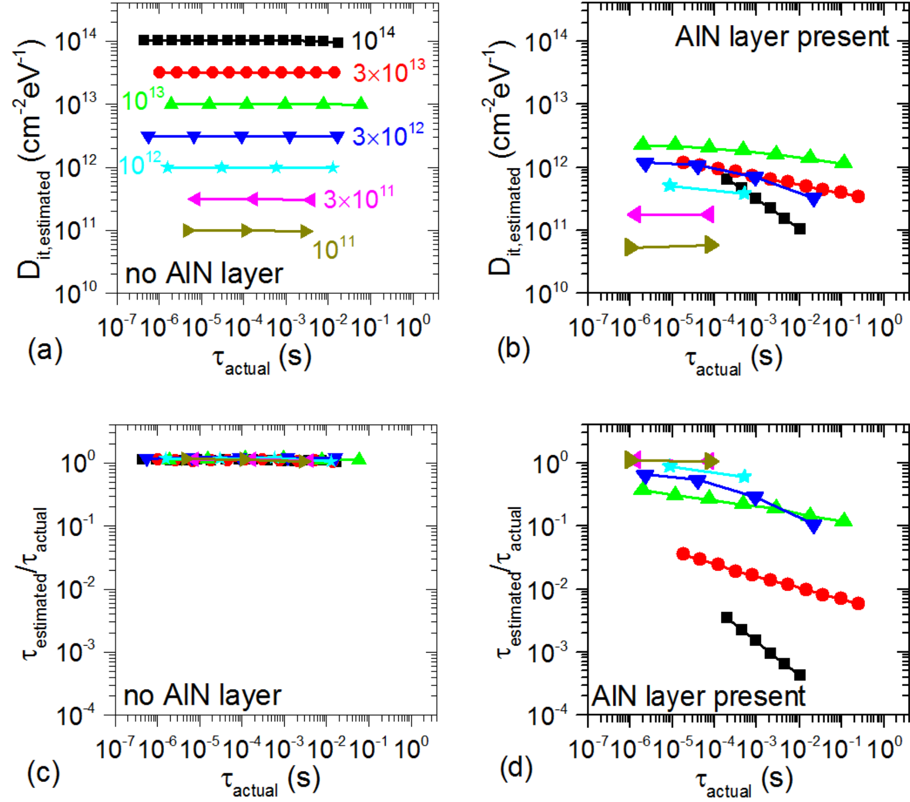


Figure 3.7: TCAD simulation results of the conductance method on the MOS-HFET device with different interface trap densities distributed uniformly in energy: estimated trap density (a) without and (b) with AlN layer; error in the estimated trap response time (c) without and (d) with AlN layer.

Simulations of the MOS-HFET device were performed with/without the AlN layer, representing the limiting cases $R_B\rightarrow\infty$ or 0, respectively. Different trap concentrations uniformly distributed over the band gap were placed at the dielectric/AlGaN interface and the conductance method was used, with fits to (3.3), to estimate the trap density, $D_{it,estimated}$, and the trap time constant, $\tau_{estimated}$. In the absence of the AlN layer, there is negligible error in estimation of the trap parameters. In contrast, with the introduction of the AlN layer, $D_{it,estimated}$ is never above C_B/q. The trap time constant is also severely underestimated by 3 orders of magnitude at high D_{it}. Thus, the equivalent circuit model has been able to successfully predict the trends in error derived from the simulations for the two limiting cases of R_B.

3.3.2 Capacitance Method

The use of the CV for trap estimation was proposed in [50] and [52] to avoid the error in the conductance arising of out interference from a finite and unknown R_B. This method is illustrated in Figure 3.8 and involves the use of the gate voltage shift, ΔV_f, with measurement frequency, f_m, of the second CV step to estimate D_{it}. We assume that only traps near the Fermi level with a response time, τ_m, below $1/f_m$ can respond to the ac measurement signal. Hence, the second CV step starts rising at a gate voltage that produces sufficient band bending to bring the traps with response time, $\tau = \tau_m$, to the Fermi level. From (3.1), interface traps in the energy range ΔE_T can be probed by two measurement frequencies, f_1 and f_2, such that:

$$\Delta E_T = k_B T \ln \frac{\tau_{m,2}}{\tau_{m,1}} = k_B T \ln \frac{f_1}{f_2} \tag{3.7}$$

The total charge at the interface corresponding to this energy range is $\Delta Q_{it} = D_{it}.\Delta E_T$. Using electrostatic equations, this charge can also be expressed in terms of ΔV_f as (3.8), with which D_{it} can be estimated as in (3.9).

$$\Delta Q_{it} = \Delta V_f.C_{ox} - \left(C_{ox} + C_B\right)\frac{\Delta E_T}{q} \tag{3.8}$$

$$D_{it} = \frac{\Delta V_f}{\Delta E_T}.C_{ox} - \frac{\left(C_{ox} + C_B\right)}{q} \tag{3.9}$$

MOS-HFET simulations with/without the AlN barrier confirmed that this method is relatively unaffected by the value of R_B (Figure 3.9a). But, its efficacy critically hinges on the resolution of the CV measurement, illustrated in Figure 3.8. An accurate extraction of ΔV_f requires a noise-free measurement of a capacitance increase, ΔC_{detect}, which is to be chosen to be lower than the capacitance corresponding to the traps, $C_{T,max}$. Further, the gate voltage sweep resolution, $V_{G,RES}$, should be low enough, such that $\Delta V_f > V_{G,RES}$. Finally, ΔE_T depends on the measurement frequency step, according to (3.7). Figure 3.9b shows the error

in D_{it} extraction by using (3.9) for different values of $V_{G,RES}$, with the circuit model described in Figure 3.4a. The measurement frequencies were chosen to be 1 kHz and 2 kHz. It is evident from Figure 3.9b that the minimum detectable trap density reduces with a reduction in $V_{G,RES}$. Additionally, for any given D_{it}, the resolution of trap density estimation improves as well.

It is also to be noted that (3.10) derived in [52], for trap density estimation using this method significantly underestimates the trap density, as is also shown in Figure 3.9b.

$$D_{it} = \left(\frac{C_{ox}C_B}{C_{ox}+C_B}\right)\frac{\Delta V_f}{\Delta E_T} = C_{floor}\frac{\Delta V_f}{\Delta E_T} \tag{3.10}$$

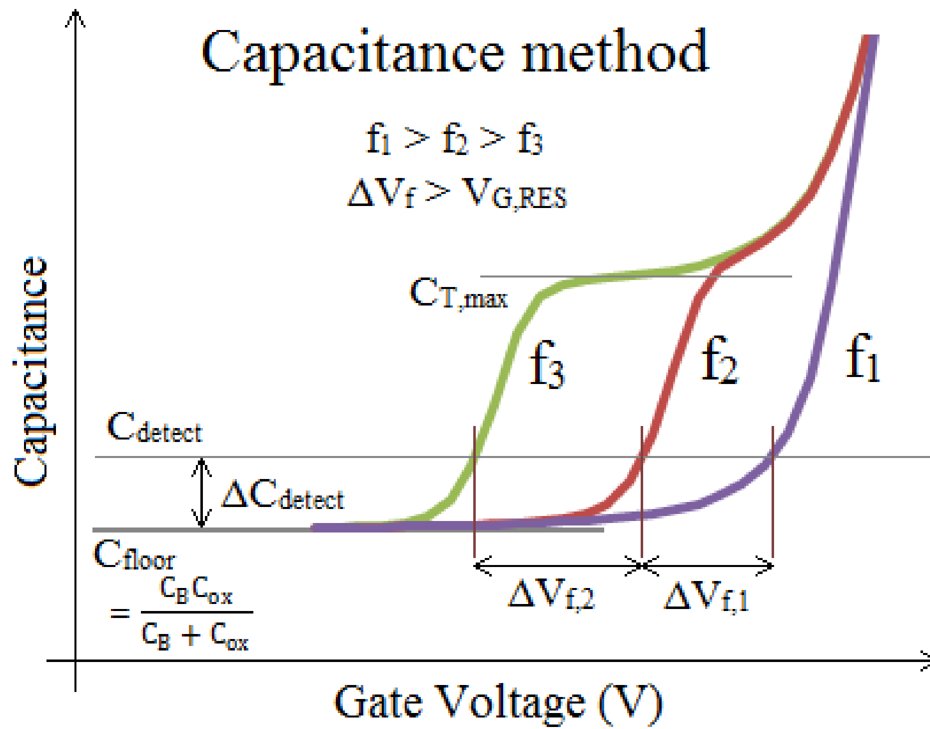


Figure 3.8: Schematic showing the extraction of the gate voltage shift, ΔV_f, of the second CV step in Figure 3.2b, for the capacitance method of extracting interface trap density.

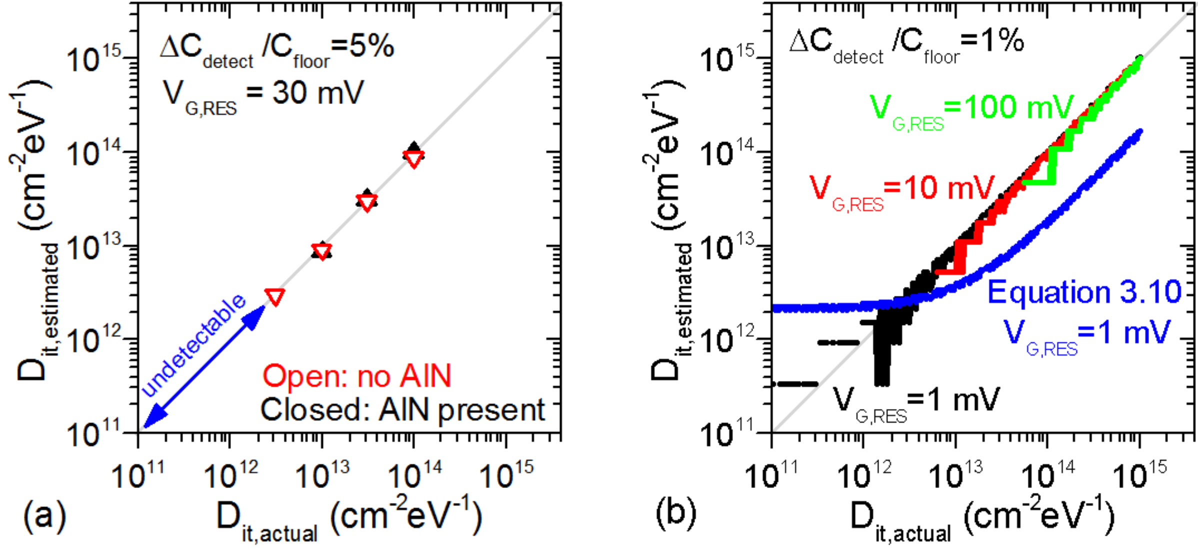


Figure 3.9: (a) Trap density estimated using TCAD simulations of the capacitance method for the barrier with/without the AlN layer. The lowest detectable trap density was $\approx 3\times10^{12}$ cm^2 eV^{-1}. (b) Trap density estimated using (3.9) with capacitance calculated with the circuit model in Figure 3.4a. The calculated ΔV_f was forced to be an integral multiple of $V_{G,RES}$ before the calculation of D_{it}, in order to model the effect of the sweep resolution. Also shown is the estimated D_{it} using (3.10). The grey line in both the plots is a visual guide for the curve: estimated D_{it} = actual D_{it}.

3.3.3 Pulsed-IV Method

The pulsed-IV method, illustrated in Figure 3.10, takes advantage of the fact that the MOS-HFET's conducting channel is separated from the traps at the dielectric/AlGaN interface. During a negative gate voltage sweep, change in the interface charge density, n_{it}, by the addition of positively charged unoccupied traps above the Fermi level or the reduction of negatively charged acceptor traps below the Fermi level, affects the threshold voltage of the device. Thus, by keeping track of the device V_T over a quiescent gate voltage ($V_{G,Q}$) sweep, the trap density can be conveniently back-calculated as (3.11).

$$n'_{it} = -\frac{\Delta n_{it}}{\Delta V_{G,Q}} = \frac{C_{ox}}{q}\frac{\Delta V_T}{\Delta V_{G,Q}} \tag{3.11}$$

The pulsed-IV system shown in section 2.2.3 can be used to perform a quiescent gate voltage sweep with quick and short perturbations to a fixed voltage, V_{ON}. By making the perturbation quicker than the response time of the interface traps, a measurement of the channel conductance, G_G, during the perturbation can be used to track the changing V_T, and the rate of change of interface charge, n_{it}', as given by (3.12). The trap density, D_{it}, can be subsequently calculated by multiplying n_{it}' with the rate of band bending, $dV_{G,Q}/dE_T$, in (3.13).

$$n'_{it} = -\frac{C_{ox}}{C_{floor}} \frac{L}{q\mu W} \frac{\Delta G_G}{\Delta V_{G,Q}} \tag{3.12}$$

$$q\frac{dV_{G,Q}}{dE_T} = -\frac{C_{ox} + C_B}{C_{ox} - qn'_{it}};\ D_{it} = -qn'_{it}\frac{dV_{G,Q}}{dE_T} \tag{3.13}$$

Pulsed-IV simulations of the MOS-HFET device were performed with different magnitudes of trap density uniformly distributed in energy. Figure 3.11a shows minimal error in estimated D_{it}, using this method, for both the cases with/without the presence of the AlN barrier.

The channel resistance, R_G, used in (3.12) as $G_G=1/R_G$, is calculated from the measured source-drain resistance, R_{SD}, by subtracting the series resistance, R_S. This series resistance is a combination of the resistances due to the ohmic contacts and the access regions. In calculating n'_{it}, using (3.12), the correct estimation of the channel mobility, μ, and R_S, is therefore very critical. Both μ and R_S can be extracted by using a fit of the transistor I_D-V_G characteristics to (3.14). Errors can appear in this process due to the interference of high density of interface traps in the I_D-V_G characteristics. For any given source-drain resistance, R_{SD}, calculated from the I_D-V_G sweep, an overestimation of R_S by dR_S results in an overestimation of μ by $d\mu$, according to (3.15).

$$R_{SD} = R_G + R_S;\ R_G = \frac{L}{\mu W C_{floor}\left(V_{GS} - V_T\right)} \tag{3.14}$$

$$\frac{d\mu}{\mu} = \frac{dR_S}{R_G} \tag{3.15}$$

Figure 3.11b shows a plot of the error in D_{it} estimation over different values of R_G and estimated R_S. The error in estimated mobility has been calculated using (3.15). A trivial observation from the plot is that if R_S is accurately estimated, D_{it} is also always accurately estimated, along the x=0 line. For $R_G<R_{S,actual}$, D_{it} can potentially be under/over-estimated. For higher values of R_G, the error is small and relatively insensitive to errors in R_S estimation. Therefore, if it is ensured that the channel resistance during the V_{ON} pulse is higher than R_S throughout the quiescent gate voltage sweep, one can simply assume $R_S = 0$ and extract μ using the peak trans-conductance method, illustrated in section 3.4.2.

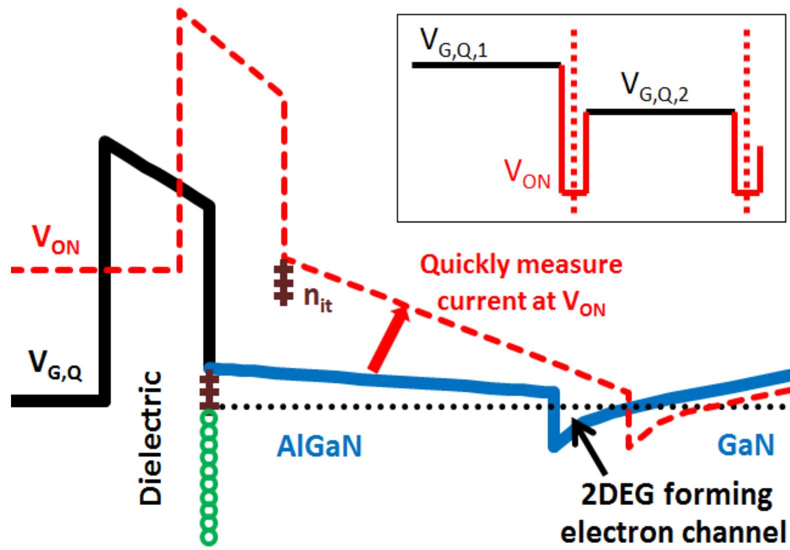


Figure 3.10: Energy band diagram under the MOS-HFET gate stack (with donor traps) at an applied quiescent gate voltage, $V_{G,Q}$, with an interface charge n_{it}. Also shown is the sequence of applied pulses over time to measure the channel current at a fixed voltage V_{ON}, the band diagram for which is shown in red.

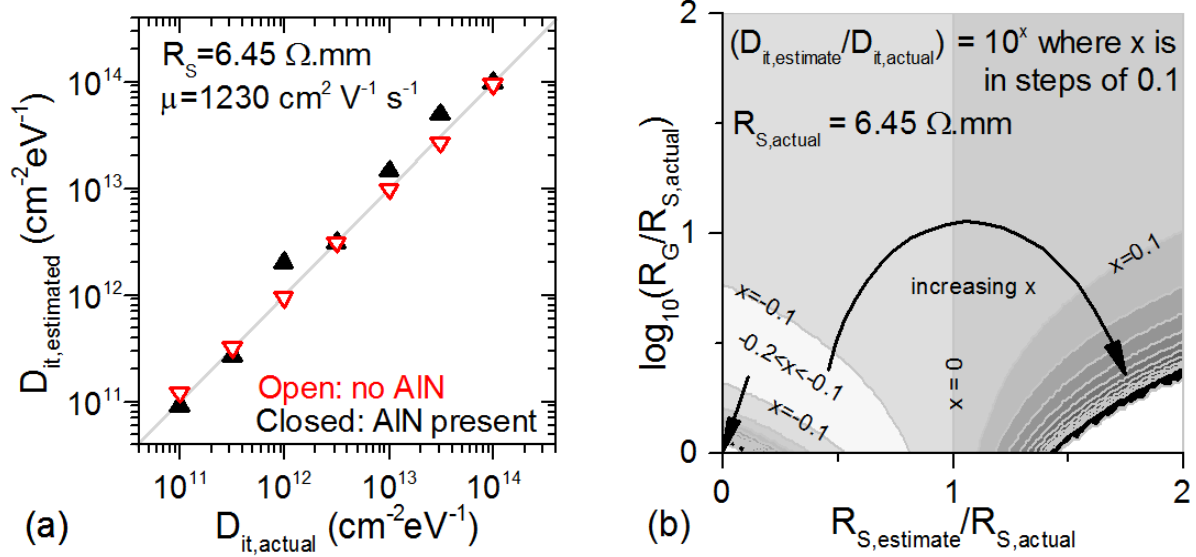


Figure 3.11: (a) Trap density estimated using TCAD simulations of the pulsed-IV method for the barrier with/without the AlN layer. (b) Contour plot of error in estimated D_{it} as a function of the channel resistance, R_G, and the estimate of the device series resistance, R_S. As an example, an actual D_{it} value of 10^{13} cm^{-2} eV^{-1} was used for the calculation.

It is important to note that the pulsed-IV method, as explained here, cannot distinguish between traps located at different spatial positions in the gate stack. It is assumed that the GaN substrate is defect-free and that the trap density at the dielectric/barrier interface is much higher than in the barrier.

3.3.4 Inferences

Table 3.2 summarizes the pros and cons of each method discussed in this section. The conductance method has a severely low upper limit of detection (C_B/q) of interface traps when the barrier resistance is significant. While the capacitance method is relatively unaffected by the barrier resistance, it has a high lower limit of detection determined by the resolution of the voltage sweep. In contrast, the pulsed-IV method is expected to be accurate over a wide range of trap densities, irrespective of the barrier resistance.

Table 3.2: Summary of the pros and cons of different trap characterization methods: conductance (GV), capacitance (CV), pulsed-IV (PIV) and a combination of PIV and GV (PIV+GV). Red indicates restrictive, while green indicates favorable.

Feature	*GV*	*CV*	*PIV*	*PIV +GV*
Trap density detection lower limit	Green	Red	Green	Green
Trap density detection upper limit	Red	Green	Green	Green
Total trap density detection range	Red	Red	Green	Green
Ability for E_T estimation vs. V_G	Green	Red	Red	Green
Ability to detect deep traps	Red	Red	Green	Green

While the conductance and capacitance techniques have been used only for shallow traps, the pulsed-IV method can be used for detecting deep traps as well, as is demonstrated in section 3.4.

Regardless, the pulsed-IV technique has to be used in conjunction with the conductance technique in order to estimate D_{it} as a function of E_T, instead of V_G. Although the conductance method can significantly underestimate the response time, τ, it only creates a small shift in estimated E_T, according to (3.1). *Therefore, a combination of the pulsed-IV technique for D_{it} estimation and the conductance method for E_T estimation is suggested for accurate interface trap characterization.*

3.4 Experimental Demonstration of Accurate Interface Trap Characterization

3.4.1 Introduction

In this section, the MOSHFET device fabricated in section 3.2.1 is used to demonstrate the effectiveness of the combination of pulsed-IV and conductance method for accurate interface traps characterization. This involves the following four steps, which are elaborated in this section:

1. Quasi steady state I_D-V_G and C-V characterization to extract the channel mobility for use in (3.12).
2. Pulsed-IV measurements to extract the trap density as a function of gate bias, for use in (3.12).
3. Conductance measurements for estimating trap depth as a function of gate bias.
4. Estimation of trap density vs. trap depth.

In the pulsed-IV measurements, the gate voltage sweep is performed from positive to negative with a 1 s hold time under 365 nm 10 mW/cm^2 UV illumination. This ensures that all the traps are filled to begin with. Then, during the slow sweep in the negative direction, the illumination provides sufficient stimulus for electrons above Fermi level to detrap and help the device reach quasi-steady state faster. This method is also applicable for deep trap measurement because the UV irradiation can excite electrons from traps more than 3 eV deep.

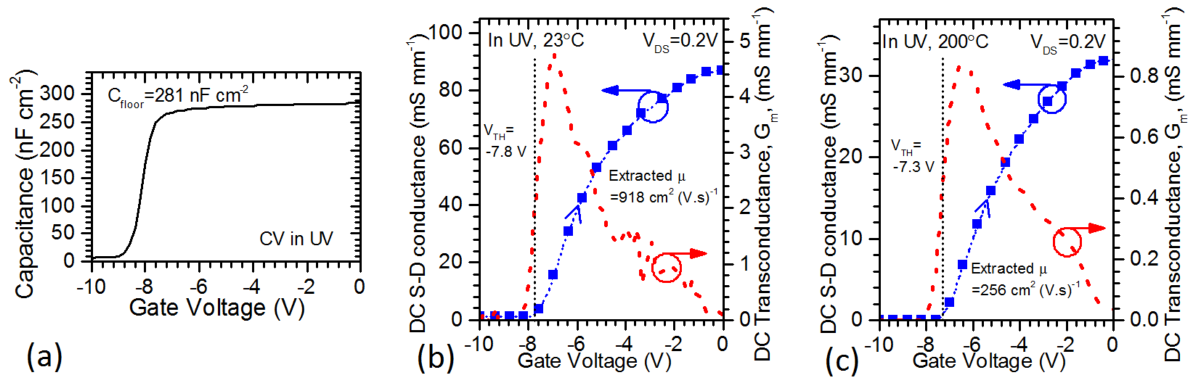


Figure 3.12: (a) CV measured from 0V to -10V at 1 MHz under UV; (b) GV measured at room temperature and 200°C with a drain voltage of 0.2V. Channel mobility was extracted using the peak trans-conductance in (3.16).

3.4.2 Quasi-steady state characterization

DC source-drain conductance-voltage (GV) measurements at low drain bias were obtained under UV illumination at room temperature and 200°C, as shown in Figure 3.12. The accumulation capacitance from a CV measurement is used in (3.16) to extract the channel mobility from the value of the peak trans-conductance (dI_D/dV_G).

$$\mu = \frac{L\left(\frac{dI_D}{dV_G}\right)_{peak}}{WC_{floor}V_{DS}} \tag{3.16}$$

3.4.3 Trap density measurement

Figure 3.13a shows the transient pulse response of the device from two extreme quiescent gate biases of 3 V and -2 V. It is observed that when $V_{G,Q}$=3V, the recovery current during the 5 μs pulse of V_{ON}=-4V is almost zero. But, when $V_{G,Q}$=-2V, the recovery current during same pulse reaches the maximum DC value. These two cases indicate that the HfAlO/AlGaN interface and border traps are mostly occupied with electrons at $V_{G,Q}$=3V and a significant number are empty at $V_{G,Q}$=-2V, thereby temporarily shifting the device threshold voltage in the positive or negative direction, respectively. The measurements shown in Figure 3.13a are performed as a progressive gate voltage sweep and the transient S-D conductance at time T_0=1 μs from the pulse rise is noted down for each $V_{G,Q}$, shown in Figure 3.13b. In order to minimize the error associated with the series resistance, three different ON voltage ranges were chosen to ensure that the channel resistance was higher than the series resistance. Elevated temperature at 200°C was also used in order to improve the efficiency of electron de-trapping and ensure a faster attainment of quasi-steady state. The pulsed-IV measurements from Figure 3.13b were subsequently used in (3.12) to estimate trap density n'_{it}, shown in Figure 3.14. Note that at very high D_{it}, the dielectric/AlGaN interface can get pinned. Under such circumstances, any additional gate charge is compensated purely by these interface traps. Thus, the oxide capacitance limits the maximum detectable trap density, by any method.

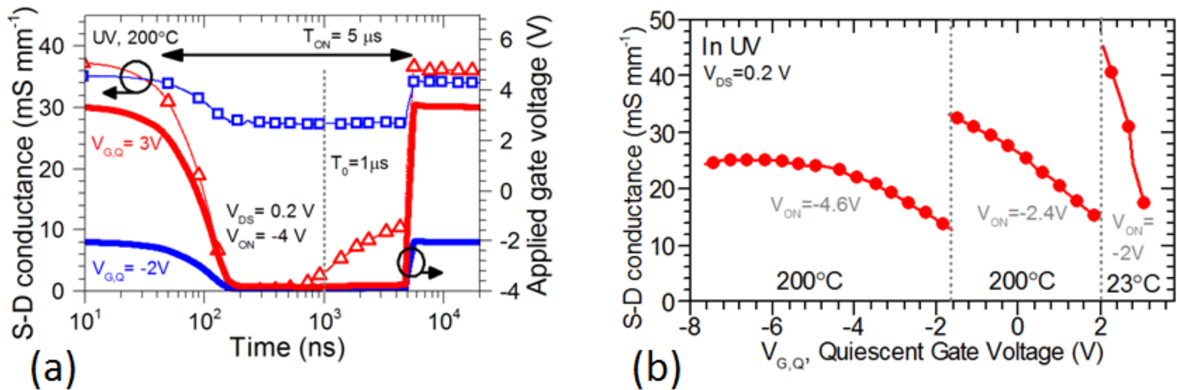


Figure 3.13: (a) Two transient pulse measurements, under UV, at quiescent gate voltages of 3V and -2V and a fixed V_{ON} (for time T_{ON}). The pulsed-IV measurement is taken at T_0 = 1 µs. (b) S-D conductance measured at 1 µs into the measurement pulse at V_{ON} over a quiescent gate voltage, $V_{G,Q}$, sweep with a hold time of 1 s.

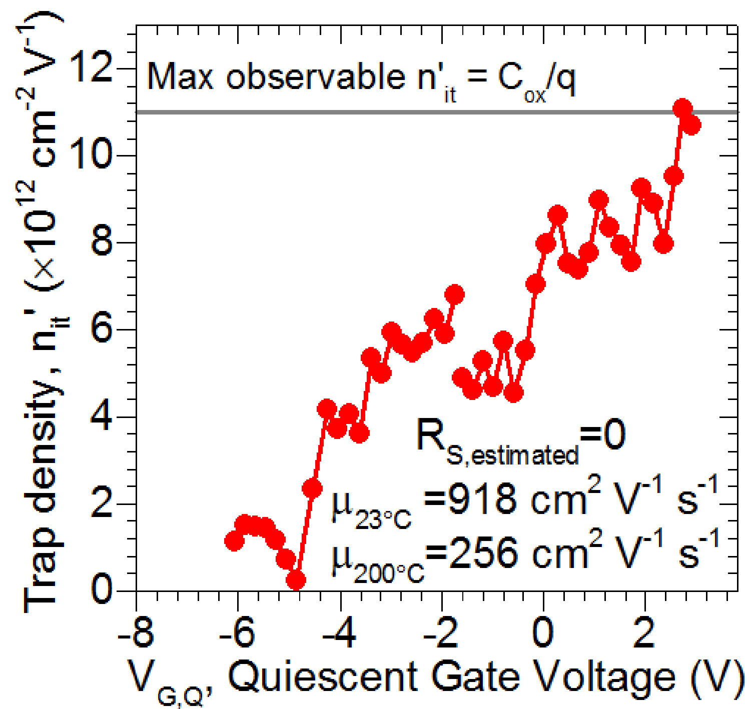


Figure 3.14: Trap density extracted using (3.12) from the S-D conductance values measured in Figure 3.13b.

3.4.4 Trap depth estimation

The rate of band bending, $dV_{G,Q}/dE_T$ can be evaluated by using the estimated n'_{it} in (3.13). But, at high D_{it}, error in n'_{it} can significantly amplify the error in $dV_{G,Q}/dE_T$. Therefore, the use of (3.13) is restricted to more negative gate voltages with n'_{it} below 40% of C_{ox}/q. Conductance method was used to estimate E_T and $dV_{G,Q}/dE_T$ for shallow energies, as shown in Figure 3.15. In order to obtain a continuous and differentiable relation between E_T and $V_{G,Q}$, a linear interpolation of the band bending rate was performed over the intermediate region. Subsequently, the E_T-$V_{G,Q}$ relation was reconstructed, as shown in Figure 3.16.

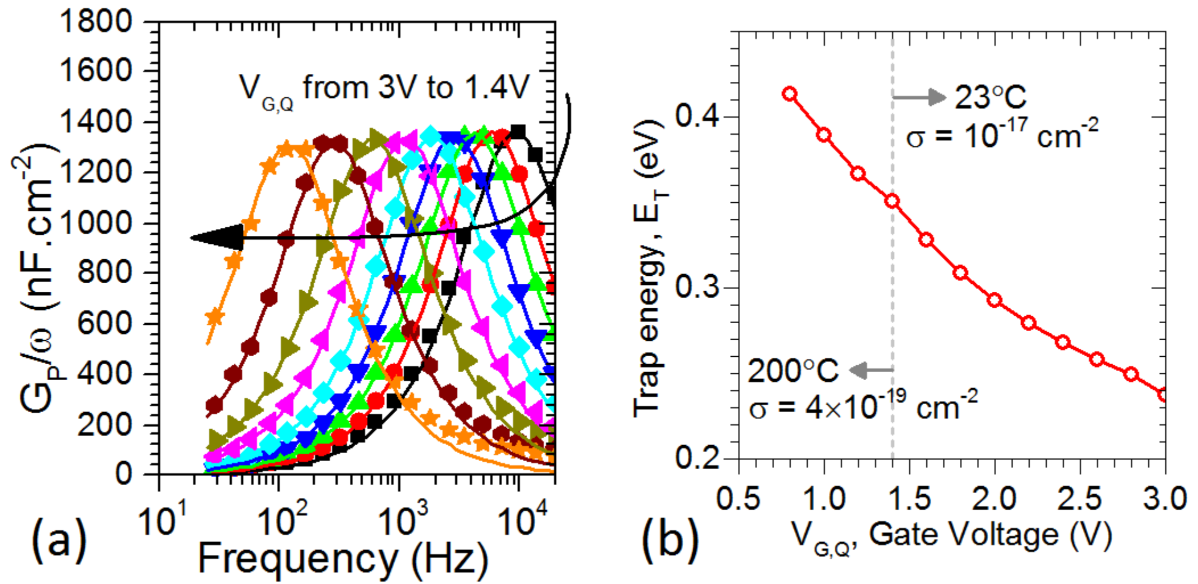


Figure 3.15: (a) Extracted G_P/ω curves and curve-fits for different applied quiescent gate voltages at 23°C; (b) Trap depth extracted using the peak position of the conductance curves. Two different capture cross sections have been used at different temperatures to ensure continuity of the curve.

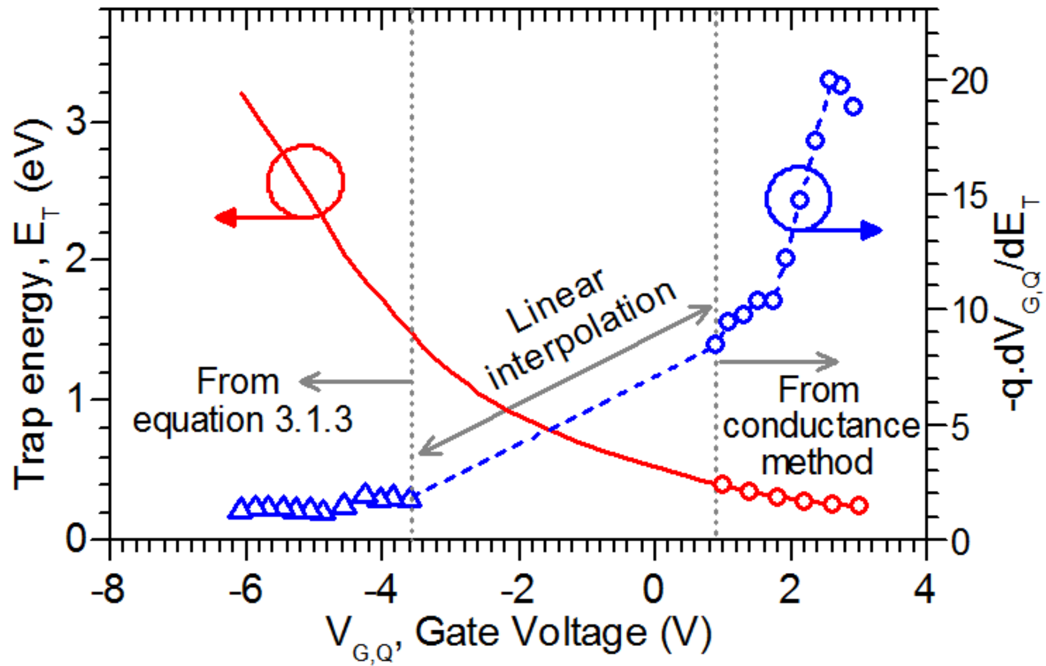


Figure 3.16: Plot of the constructed trap depth and the rate of band bending curves over different gate voltages. Open symbols are data points extracted directly from measurements.

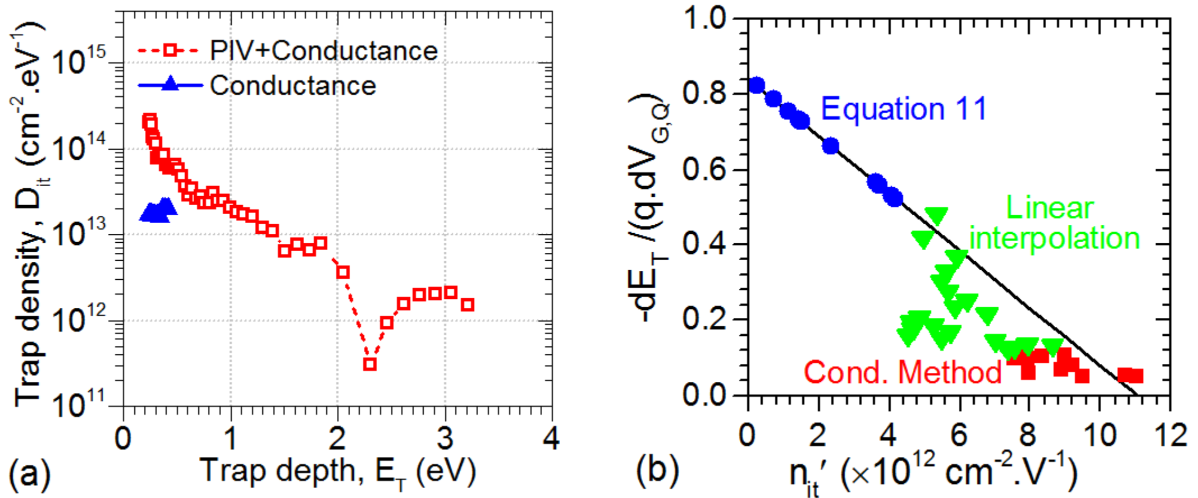


Figure 3.17: (a) Trap density experimentally estimated using a combination of pulsed-IV and conductance methods vs. trap depth. Also shown is the trap density estimated by the conductance method. (b) Plot of the estimated rate of band bending vs. estimated trap density. The solid line shows the ideal theoretical expectation predicted by (3.13).

3.4.5 Final trap density profile reconstruction and validation

The results in Figure 3.14 and Figure 3.16 were combined to obtain the final trap density plot over the trap depth, E_T, as shown in Figure 3.17a. It is evident here that the exclusive use of conductance method grossly underestimated the trap density and is hence, unreliable.

For a given estimated trap density, Figure 3.17b demonstrates a reasonable adherence of the estimated band bending rate with the theoretically expected value predicted by (3.13). This is a critical indicator to the success of this method at accurately characterizing interface traps.

3.5 Summary

While conductance (GV) and capacitance (CV) methods have been used with GaN MOS-HFET devices for characterization of traps at the interface between the dielectric and the barrier material, these methods are limited in their scope. Due to the presence of a thin AlN layer between the barrier and GaN or the substrate growth parameters, the barrier can offer a resistive path to the trapped electrons. Under such circumstances, the conductance method can severely underestimate the trap density, especially in devices with high D_{it}. The exclusive use of CV sweeps for trap density estimation is relatively immune to interference from the barrier resistance. But, both the resolution and the lower detection limit of the method are limited by the resolution of the CV sweep. In addition, both the methods are developed only for probing shallow energy depths and are, therefore, insufficient for describing interface traps spread across the wide bandgap of the barrier material.

The use of pulsed-IV measurements, for both shallow and deep traps characterization, was found to be immune from issues of barrier resistance and applicable over a wide range of trap density values. The use of this method, along with conductance method, was experimentally demonstrated on an AlGaN/GaN MOS-HFET with HfAlO gate dielectric. A good match between the estimated band bending and the theoretically predicted value,

accounting for interface traps, confirms a superior accuracy of this method over exclusive use of CV or GV methods. Henceforth, this method is used for characterizing dielectric/AlGaN interface traps for different dielectrics in Chapter 4.

CHAPTER 4: Characterization of Traps at ALD Dielectric/AlGaN Interface

4.1 Introduction

In this chapter, different dielectrics deposited by ALD are investigated for traps at the dielectric/AlGaN interface. Silicon nitride, a common passivation dielectric, deposited by PECVD is also looked at, for the sake of comparison. A combination of pulsed-IV and conductance methods, as elaborated in section 3.4, is used for this purpose. The findings of this chapter have a direct bearing on the choice of the best gate dielectric and passivation dielectric for the AlGaN/GaN MOSHFET device.

4.2 Sample preparation

MOS-HFET devices were fabricated on AlGaN/GaN on Si substrate samples (GaN-Si) with the SCHEME B fabrication flow specified in Figure 2.4. Different dielectrics (ALD SiO_2, ALD Al_2O_3, ALD HfAlO, ALD HfO_2 and PECVD silicon nitride) with a nominal electrical thickness of 5 nm were used as the gate dielectric. The electrical thickness of a dielectric film, commonly referred to as the Equivalent Oxide Thickness (EOT), is the thickness of SiO_2 that has the same capacitance as that of the dielectric film. An additional 200 nm layer of PECVD SiO_2 was also added to the samples with ALD gate dielectrics in order to improve device passivation. Details of the process conditions are provided in section 2.1.2 and 2.1.4. The dielectrics do not receive any anneal until step 6 in Figure 2.4, when the device fabrication is complete. The effect of a couple of subsequent post-metallization anneals (PMA, step 6) at increasing temperatures is also investigated. Figure 3.1 shows the lateral dimensions of the fabricated MOSHFETs with a gate length of 9 µm and gate width of 104 µm.

4.3 Extraction of gate stack capacitance

Accurate knowledge of the capacitance of the deposited dielectric, C_{ox}, is critical for extraction of trap characteristics. The accumulation capacitance measured on the fabricated AlGaN/GaN MOSHFET devices is underestimated due to the lower density of states in the AlGaN conduction band, as mentioned in section 3.2.2. Therefore, accumulation capacitance from capacitors made on monitor n-Si wafers was used for accurate EOT determination. These monitor wafers were inserted along with the AlGaN/GaN samples during the gate dielectric deposition step. Post capacitor fabrication, these monitor samples underwent the same anneal conditions as their corresponding MOSHFET counterparts.

The total capacitance of the gate stack, C_{floor}, is estimated from CV measurements of the fabricated MOSHFET device as illustrated in Figure 3.2. The EOT of the AlGaN barrier layer can be calculated by subtracting the dielectric EOT from the EOT of the entire gate stack. Details of the extracted gate stack EOTs for different anneal conditions are provided in Table 4.1. Physical thickness of as-deposited dielectrics was measured by ellipsometry on control Si wafers.

Table 4.1: Thickness of different layers of the fabricated MOSHFETs.

As dep. physical thickness	AlGaN EOT (nm)	Anneal condition	Dielectric EOT (nm)
22.6 nm ALD HfO_2	14.1	As deposited	3.6
		400°C PMA	4.8
		600°C PMA	4.8
10.4 nm ALD Al_2O_3	13.6	As deposited	4.2
		600°C PMA	4.5
		700°C PMA	4.3
15.7 nm ALD HfAlO	13.9	As deposited	4.3
		600°C PMA	4.4
		700°C PMA	4.1
5.1 nm ALD SiO_2	14.4	As deposited	3.3
		600°C PMA	3.9
		700°C PMA	3.9
9.7 nm PECVD Si_3N_x	15.1	As deposited	4.6

4.4 Interface traps at ALD HfO_2/AlGaN interface

The fabricated MOSHFET with ALD HfO_2 gate dielectric was characterized for interface traps using the method described in section 3.4. Figure 4.1 shows a high density of shallow traps before and after PMA at 400°C and 600°C. The density of deeper traps is seen to increase with every anneal. But, it is also very likely that an anneal-related improvement in passivation quality permits the measurement of deeper traps, which were always present. The total measured density of traps for the as-deposited, 400°C PMA and 600°C PMA are 5.75×10^{13} cm^{-2}, 4.59×10^{13} cm^{-2} and 5.11×10^{13} cm^{-2}, respectively.

As predicted in section 3.3.1, it is found that the conductance method severely underestimates the trap density.

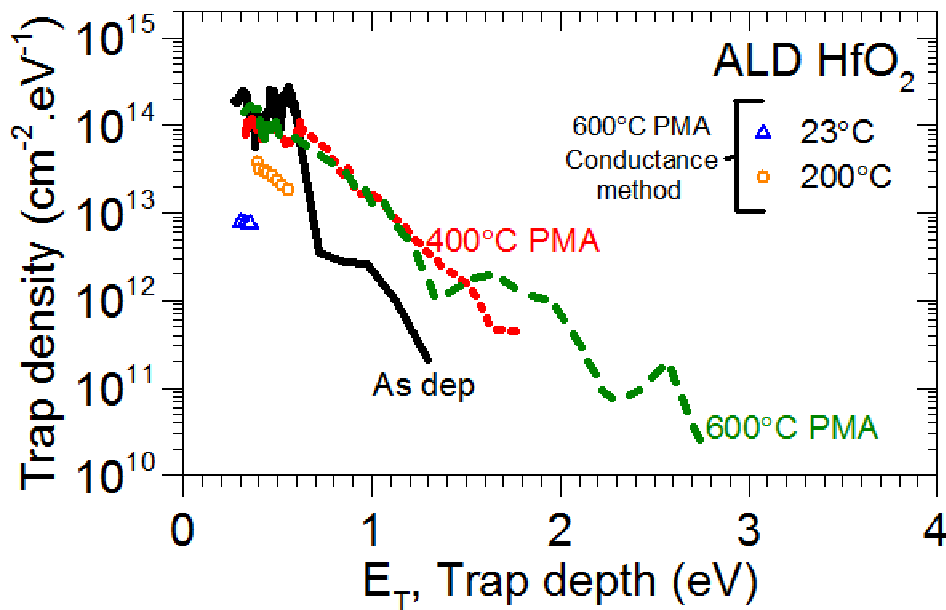


Figure 4.1: Lines show the interface trap density detected at the ALD HfO_2/AlGaN interface using pulsed-IV method for different anneal conditions. Open symbols are the estimates from the conductance method only for 600°C PMA. Similar estimates are obtained by conductance method for other anneal conditions.

4.5 Interface traps at ALD HfAlO/AlGaN interface

The fabricated MOSHFET with ALD HfAlO gate dielectric was characterized for interface traps using the method described in section 3.4. Figure 4.2 shows a high density of shallow traps before and after PMA at 600°C and 700°C. The density of deeper traps is seen to increase with every anneal. But, it is also very likely that an anneal-related improvement in passivation quality permits the measurement of deeper traps, which were always present. The total measured density of traps for the as-deposited, 600°C PMA and 700°C PMA are 5.28×10^{13} cm^{-2}, 5.14×10^{13} cm^{-2} and 6.05×10^{13} cm^{-2}, respectively.

As predicted in section 3.3.1, it is found that the conductance method severely underestimates the trap density.

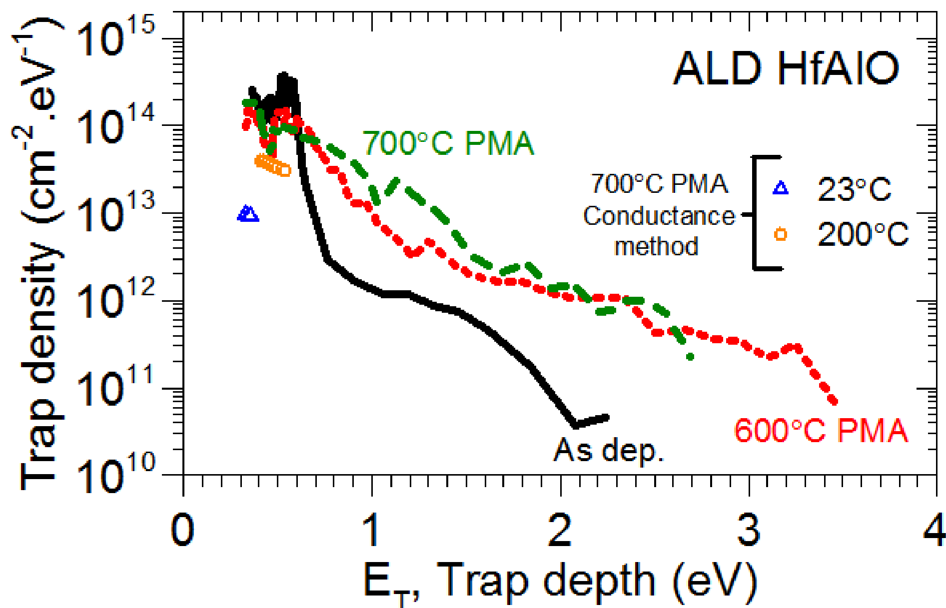


Figure 4.2: Lines show the interface trap density detected at the ALD HfAlO/AlGaN interface using pulsed-IV method for different anneal conditions. Open symbols are the estimates from the conductance method only for 700°C PMA. Similar estimates are obtained by conductance method for other anneal conditions.

4.6 Interface traps at ALD Al_2O_3/AlGaN interface

The fabricated MOSHFET with ALD Al_2O_3 gate dielectric was characterized for interface traps using the method described in section 3.4. Figure 4.3 shows two distinct shallow peaks of high trap density in the as-deposited case, which are strongly suppressed and spread out deeper after PMA at 600°C and 700°C. The density of deeper traps is seen to increase with every anneal. But, it is also very likely that an anneal-related improvement in passivation quality permits the measurement of deeper traps, which were always present. The total measured density of traps for the as-deposited, 600°C PMA and 700°C PMA are 2.38×10^{13} cm^{-2}, 2.59×10^{13} cm^{-2} and 2.16×10^{13} cm^{-2}, respectively.

On the average, it is found that the conductance method estimates are reasonably accurate for the device after the 600°C or 700°C PMA. But in this case, we are fortunate that the main conductance peak is well visible and higher than the secondary peak artifact (explained in section 3.3.1) at around 1 kHz, shown in Figure 4.4.

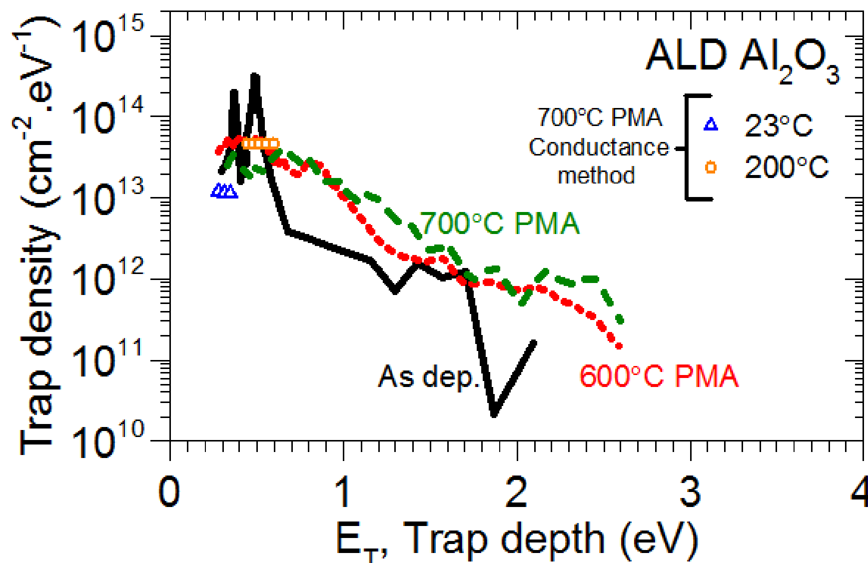


Figure 4.3: Lines show the interface trap density detected at the ALD Al_2O_3/AlGaN interface using pulsed-IV method for different anneal conditions. Open symbols are the estimates from the conductance method only for 700°C PMA. Similar estimates are obtained by conductance method for other anneal conditions.

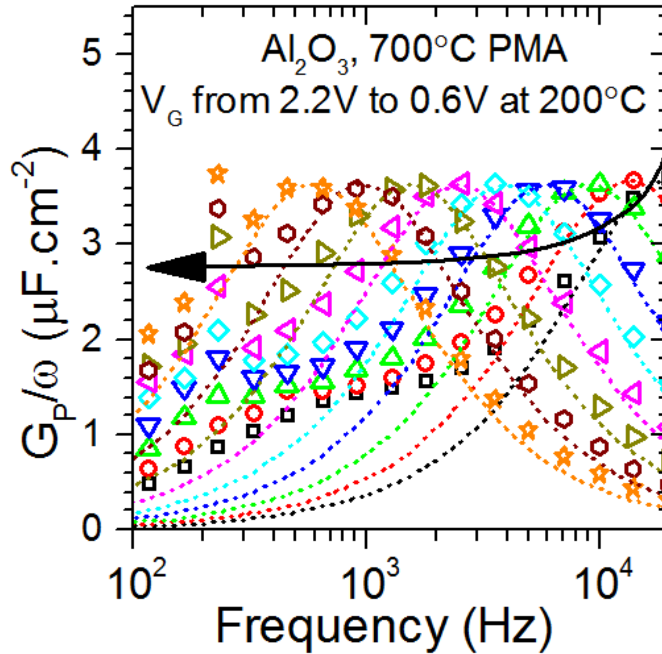


Figure 4.4: Conductance curves obtained at 200°C with the MOSHFET having ALD Al_2O_3 gate dielectric after a 700°C PMA.

4.7 Interface traps at ALD SiO_2/AlGaN interface

The fabricated MOSHFET with ALD SiO_2 gate dielectric was characterized for interface traps using the method described in section 3.4. Figure 4.5 shows a high shallow trap density peak in the as-deposited case, which is strongly suppressed and spread out deeper after PMA at 600°C and 700°C. The density of deeper traps is seen to increase with every anneal. But, it is also very likely that an anneal-related improvement in passivation quality permits the measurement of deeper traps, which were always present. The total measured density of traps for the as-deposited, 600°C PMA and 700°C PMA are 8.46×10^{12} cm^{-2}, 1.73×10^{12} cm^{-2} and 1.63×10^{12} cm^{-2}, respectively. It is remarkable that after a PMA, the total interface trap density at the ALD SiO_2/AlGaN interface is more than an order of magnitude lower than that of high-k dielectrics like ALD Al_2O_3, ALD HfO_2 and ALD HfAlO. This low trap density results in a significantly reduced hysteresis in I_D-V_G measurements, in section 5.3, and hence, proving to be an excellent gate dielectric.

Conductance method is found to significantly overestimate the trap density in the case of ALD SiO_2/AlGaN interface, especially after subsequent anneals. This is possibly due to a rapid variation of trap capture cross-section close to the conduction band [54], [59].

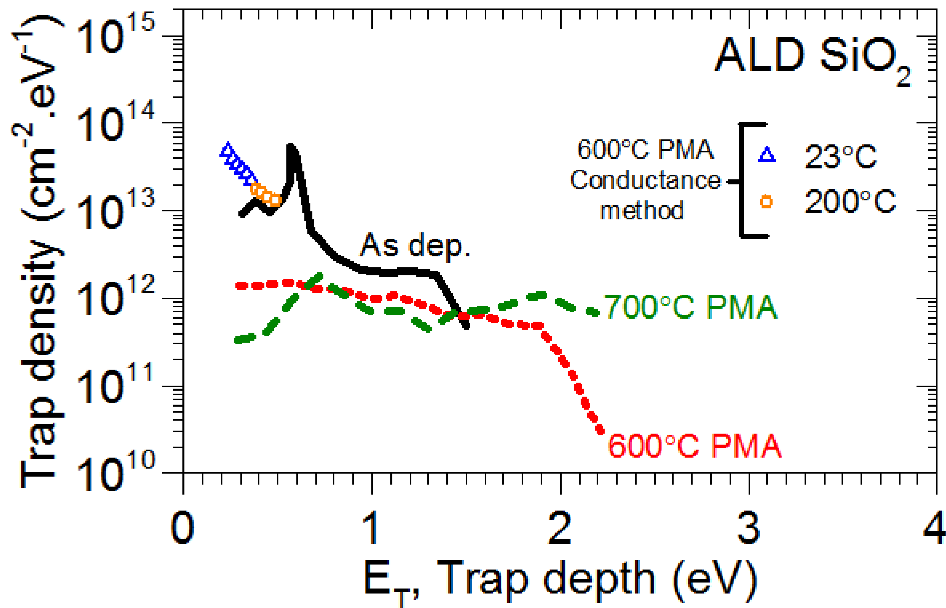


Figure 4.5: Lines show the interface trap density detected at the ALD SiO_2/AlGaN interface using pulsed-IV method for different anneal conditions. Open symbols are the estimates from the conductance method only for 600°C PMA. Similar estimates are obtained by conductance method for other anneal conditions.

4.8 Interface traps at PECVD silicon nitride/AlGaN interface

The fabricated MOSHFET with PECVD silicon nitride gate dielectric was characterized for interface traps using the method described in section 3.4. Figure 4.6 shows a low density of interface traps below 10^{13} cm^{-2} eV^{-1}. The total measured density of traps is found to be 4.08×10^{12} cm^{-2}. This is significantly lower than that in high-k dielectrics, but is still about 2.5 times higher than that with ALD SiO_2 after a 700°C PMA. Regardless, like ALD SiO_2, PECVD silicon nitride shows a significantly reduced hysteresis in I_D-V_G

measurements, in section 5.3. Unfortunately, since it is much leakier than ALD SiO_2 (section 5.2), it is not a strong candidate for a gate dielectric.

Conductance method is found to slightly overestimate the trap density in the case of PECVD silicon nitride/AlGaN interface. More interestingly, Figure 4.7 shows that during a negative gate sweep, the location of the conductance peak is seen to move to lower frequencies and then rise up again. This is possibly due to a rapidly increasing trap capture-cross section with deeper traps.

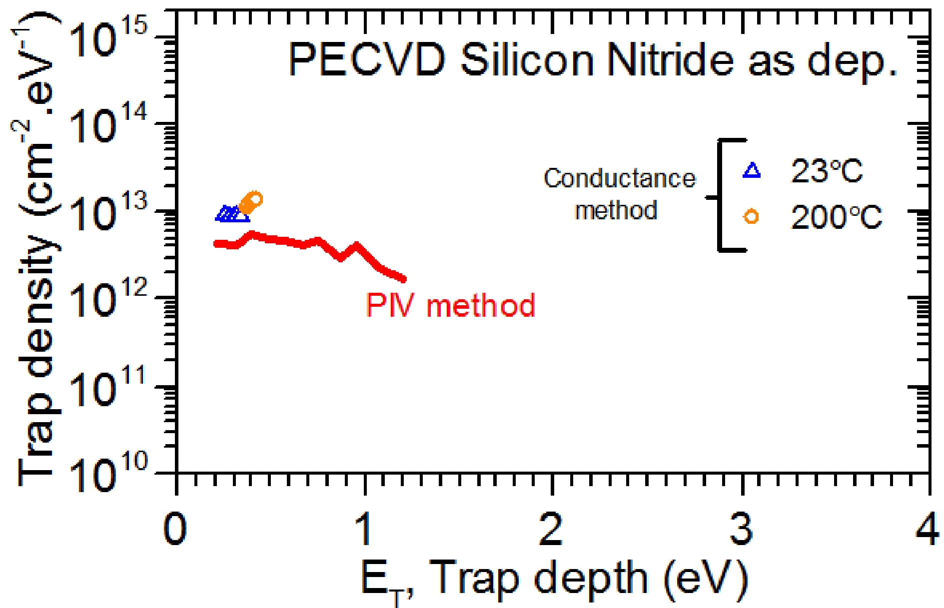


Figure 4.6: Lines show the interface trap density detected at the PECVD silicon nitride/AlGaN interface using pulsed-IV method for the as-deposited condition. Open symbols are the estimates from the conductance method, until $V_G = 0$ V, corresponding to the tallest observed peak.

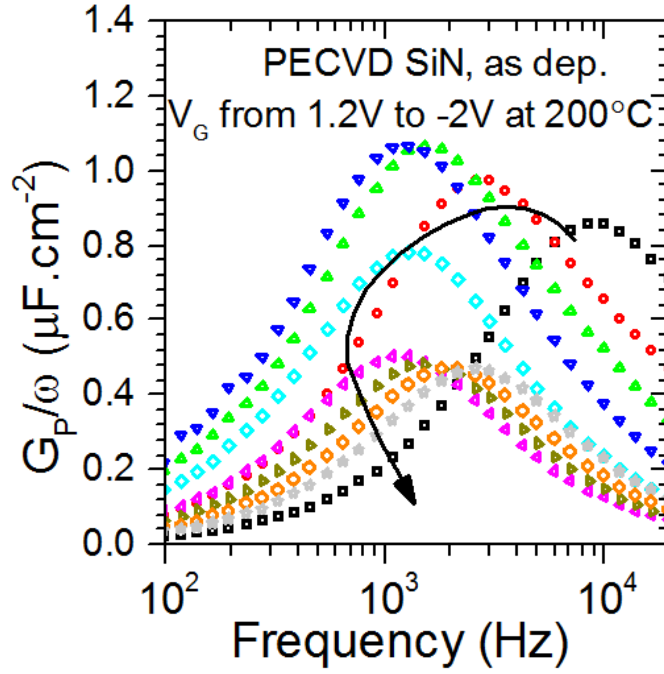


Figure 4.7: Conductance curves obtained at 200°C with the MOSHFET having PECVD silicon nitride gate dielectric in the as-deposited state.

Table 4.2: Minimum total measured density of traps for different dielectrics and annealing conditions.

Dielectric	Anneal condition	Total D_{it} (cm^{-2})
ALD SiO_2	As dep.	8.46×10^{12}
	600°C PMA	1.73×10^{12}
	700°C PMA	1.63×10^{12}
PECVD Si_3N_x	As dep.	4.08×10^{12}
ALD Al_2O_3	As dep.	2.38×10^{13}
	600°C PMA	2.59×10^{13}
	700°C PMA	2.16×10^{13}
ALD HfO_2	As dep.	5.75×10^{13}
	400°C PMA	4.59×10^{13}
	600°C PMA	5.11×10^{13}
ALD HfAlO	As dep.	5.28×10^{13}
	600°C PMA	5.14×10^{13}
	700°C PMA	6.05×10^{13}

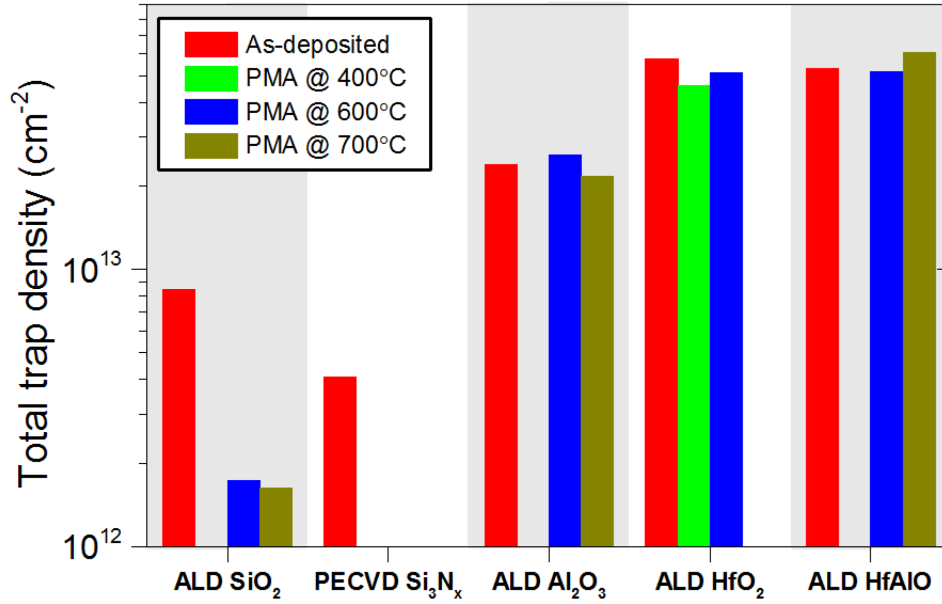


Figure 4.8: Bar graph showing the minimum total measured density of traps for different dielectrics and annealing conditions from Table 4.2.

4.9 Summary

Table 4.2 and Figure 4.8 summarize the total trap density measured for all the dielectric and anneal conditions explored in this work. High-k ALD dielectrics like Al_2O_3, HfO_2 and HfAlO are found to create a high density of interface traps with AlGaN. In comparison, ALD SiO_2 creates a significantly lower interface trap density ($< 2\times10^{12}$ cm^{-2}), after post-metallization annealing in N_2 at 700°C.

CHAPTER 5: ALD Dielectrics for Gate Stack

5.1 Introduction

In this chapter, ALD dielectrics are evaluated for threshold voltage stability and gate leakage performance on AlGaN/GaN substrates. Additionally, the impact of the dielectric on the magnitude of the threshold voltage is also investigated. Using the results of Chapter 4 and the findings of this chapter, a recommendation for an ideal gate dielectric is made.

5.2 Dielectric/AlGaN gate stack leakage

5.2.1 Introduction

Gate leakage in AlGaN/GaN devices is typically dominated by electron transport. A high conduction band offset between the dielectric and AlGaN is required to minimize thermionic emission. Increasing the dielectric physical thickness increases the tunneling distance for electrons and hence, can effectively reduce the tunneling component of leakage. But, a greater physical thickness reduces the gate capacitance and the gate's control over the conducting channel. A higher dielectric constant material can help improve gate control over the channel. But, typically, a dielectric with higher dielectric constant has a lower band gap. Overall, a trade-off exists in choosing a relatively higher dielectric constant material with a reasonably high band offset for the gate dielectric.

In order to evaluate dielectrics with different dielectric constants for their effectiveness in gate leakage suppression, MOSHFETs were fabricated with identical gate capacitance. The electrical thickness of a dielectric film, commonly referred to as the Equivalent Oxide Thickness (EOT), is the thickness of SiO_2 that has the same capacitance as that of the dielectric film. By using different dielectrics with identical EOT on AlGaN/GaN substrate samples from the same wafer (GaN_Si, Table 2.1), the impact of band offsets and physical thickness on gate leakage is more clearly visible. Details of the fabrication process for the

MOSHFETs and extraction of EOTs for the different dielectrics are mentioned in sections 4.2 and 4.3, respectively.

5.2.2 Gate leakage trends

The addition of any dielectric between the AlGaN and the gate metal reduces gate leakage by orders of magnitude, as seen in Figure 5.1. A greater dielectric physical thickness helps reduce gate leakage by increasing the tunneling distance for the electrons. This trend is seen clearly in Figure 5.1 with the physically thicker higher-k films providing much lower leakage levels. ALD SiO_2 and ALD HfAlO are exceptions as they are expected to have a much higher conduction band offset with AlGaN, compared to PECVD Si_3N_x and ALD HfO_2, respectively [38], [53]. Additionally, as-deposited PECVD Si3Nx may also host a high density of bulk traps assisting Poole-Frenkel conduction or trap-assisted tunneling.

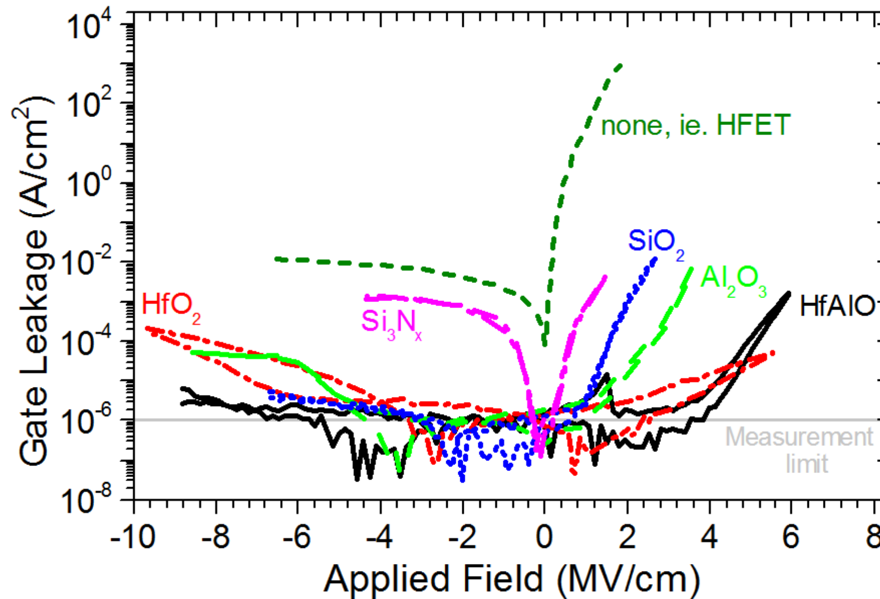


Figure 5.1: Best case gate leakage curves measured for different dielectrics in Table 4.1 with identical EOTs. Also included for comparison is the HFET, which has no gate dielectric. The curves for ALD SiO_2, HfAlO and Al_2O_3 gate dielectrics are after a PMA at 600°C. The curve for ALD HfO_2 is after a PMA at 400°C and that of PECVD Si_3N_x is in the as-deposited state. Hysteresis is observed in the I_G-V_G due to the changing conduction band shape from the changing dielectric/AlGaN interface trap occupancy during positive and negative gate voltage sweeps.

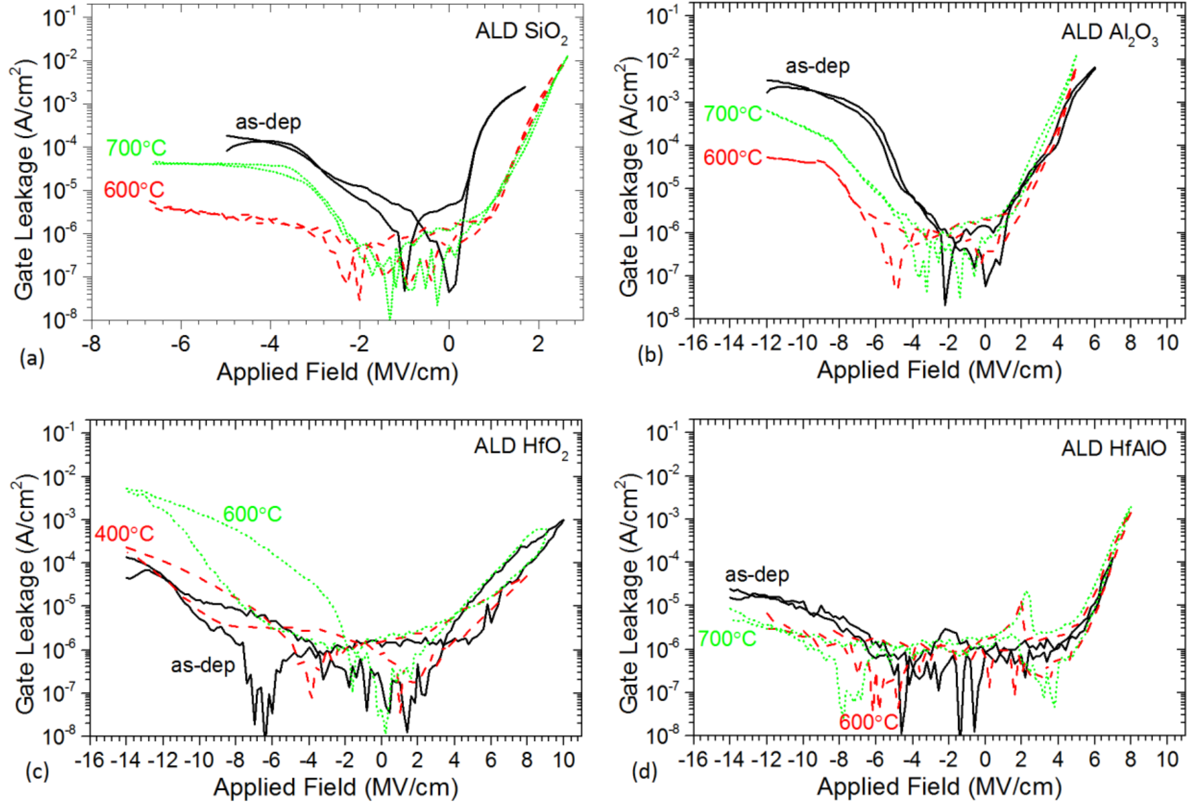


Figure 5.2: Gate leakage (I_G-V_G) measured for the MOSHFETs with ALD dielectrics, before and after anneals as described in Table 4.1: (a) SiO_2; (b) Al_2O_3; (c) HfO_2; and (d) HfAlO.

Figure 5.2 shows a general trend of reduction in leakage with a PMA, possibly due to a reduction in bulk trap density leading to a reduction in Poole-Frenkel or trap-assisted tunneling leakage. But, a consecutive higher temperature anneal is found to increase leakage, potentially indicating densification, re-crystallization, and a reduction in the physical thickness of the dielectric layer.

5.3 ON-state gate stack reliability

An assessment of ON-state gate stack reliability was performed by looking for signs of hysteresis in DC I_D-V_G measurements, and the resulting threshold voltage instability. MOSHFET devices fabricated in section 4.2 were used for this purpose. Measurements in the dark, at room temperature, can only reveal the effect of shallow traps on I_D-V_G hysteresis.

While symptoms of deeper traps are not visible in such relatively fast gate voltage sweeps, a change in their occupancy over longer timescales can result in changing device characteristics during long term use. The use of UV illumination during I_D-V_G sweeps can excite electrons from deeper traps and reveal their presence more clearly in I_D-V_G hysteresis.

DC I_D-V_G transfer curves at low drain bias, under UV illumination, were obtained for the MOSHFET devices fabricated in section 4.2. Figure 5.3 shows the representative measurements for ALD dielectrics after post-metallization anneal (PMA). Similar hysteresis was observed in all the other conditions mentioned in Table 4.1, as well. Significant clockwise hysteresis was observed with the high-k ALD dielectrics, Al_2O_3, HfO_2 and HfAlO. ALD SiO_2 showed much lower hysteresis, both before and after anneals. Clockwise hysteresis indicates electron trapping in the high density of interface traps with the high-k dielectrics. The size of the hysteresis window, for each dielectric, is found to be proportional to the density of traps characterized in Table 4.2.

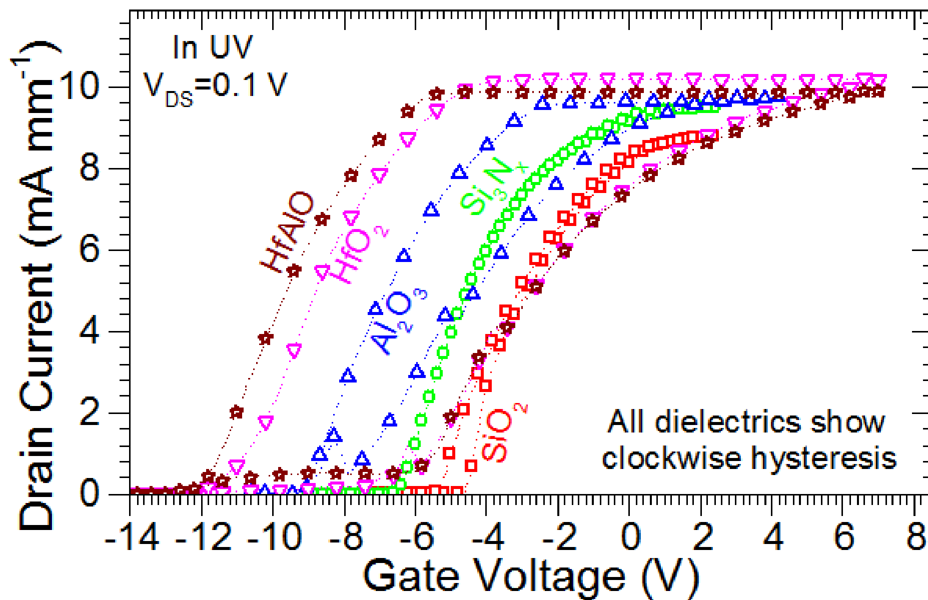


Figure 5.3: DC I_D-V_G curves measured for the following MOSHFETs, at low V_{DS}: HfAlO after 700°C PMA, HfO_2 after 600°C PMA, Al_2O_3 after 700°C PMA, SiO_2 after 700°C PMA and PECVD Si_3N_x as-deposited. Saturation current levels showed minor change before and after anneals.

Figure 5.3 also reveals a saturation of drain current ≈ 4 V beyond the threshold voltage during the positive gate voltage sweep. This phenomenon is observed with all the attempted dielectrics. In the case of high-k dielectrics with high density of shallow interface traps, the saturation could be caused due to a pinning of the dielectric/AlGaN interface and a loss of gate control over the channel. Further, a low interface-mobility may make any additional conduction due to free electrons, at the dielectric/AlGaN interface, insignificant compared to the channel current in the AlGaN/GaN 2DEG. The presence of a 2DEG-confining AlN layer [39], [40] between the AlGaN and GaN may further increase the barrier layer resistivity. Therefore, unless the AlGaN barrier conductivity is improved and the dielectric/AlGaN interface is made a high mobility trap-free interface, it is not possible to obtain a MOSHFET ON-resistance significantly lower than that of an HFET, even at high positive gate overdrive.

5.4 MOSHFET threshold voltage

5.4.1 Influence of gate dielectric on threshold voltage

Using models developed for Si-MOS and AlGaN/GaN HFETs [60], [61], the threshold voltage (V_T) of the MOSHFET device is given by (5.1).

$$V_T = \psi_{GaN,MOS} + \psi_{pol} + \psi_{charge} \quad (5.1)$$

- $\psi_{GaN,MOS} = \frac{\phi_{MS}}{q} + \psi_{s,max} + \frac{Q_D}{C_{floor}}$ = threshold voltage component for an ideal MOS gate stack without any polarization in the barrier. Φ_{MS} is the work function difference between the gate metal and the GaN bulk. $\Psi_{s,max}$ is the potential drop in the depleted GaN bulk required for the formation of the 2DEG and is approximated as $E_C - E_F$. Q_D is the depletion charge in the semi-isolating GaN bulk and C_{floor} is the total capacitance of the gate stack. $\Psi_{s,max}$ and Q_D are dependent on the nature of the GaN bulk and can be ignored for an unintentionally n-doped GaN buffer layer.

- $\psi_{pol} = -\frac{q\sigma_{pol}}{C_B}$ = threshold voltage component accounting for the polarization charge, σ_{pol}, across the AlGaN barrier having capacitance C_B.
- $\psi_{charge} = -\frac{t_{ox}}{\varepsilon_{ox}}\left(Q_{it} + Q_F + \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho_{ox}(x)dx\right)$ = threshold voltage component due to dielectric charges. Q_{it} is the areal charge density due to traps at the dielectric/AlGaN interface. Note that unoccupied donor interface traps contribute positive charge to Q_{it} and unoccupied acceptor interface traps are neutral. Q_F is the areal charge density due to fixed charge at the dielectric/AlGaN interface. $\rho_{ox}(x)$ is the volume fixed charge density in the dielectric bulk.

5.4.2 Threshold voltage trends

For a fixed gate capacitance, the threshold voltage is a strong indicator of the charges in the dielectric or the dielectric/AlGaN interface. Threshold voltage was extracted by linear extrapolation of the I_D-V_G curve at low V_{DS} for the different dielectrics with identical EOTs listed in Table 4.1, and is shown in Figure 5.4. In order to observe the potential impact of deep traps on V_T, the sweep was done under UV illumination from negative to positive gate voltages such that the deep traps were unoccupied before $V_G = V_T$. It is seen that ALD SiO_2 provides the least change in V_T from the HFET. The overall trend in V_T is seen to be HFET > annealed ALD SiO_2 > as-deposited PECVD SiO_2 > annealed ALD Al_2O_3 > annealed ALD HfO_2 > annealed ALD HfAlO.

In order to acquire a more accurate picture of the spatial distribution of charge with the high-k dielectrics, a new set of samples was prepared from the GaN_Si wafer (Table 2.1) with gate dielectrics of varying thickness. MOSHFETs were fabricated by scheme B in Figure 2.4. At stage 4a, after a blanket deposition of thick ALD gate dielectric, a timed wet-etch of parts of the sample by dipping in diluted HF/BOE provided MOSHFETs with varying gate dielectric thicknesses on the same sample. After completing MOSHFET fabrication, a post-metallization anneal at 400°C was performed in step 6.

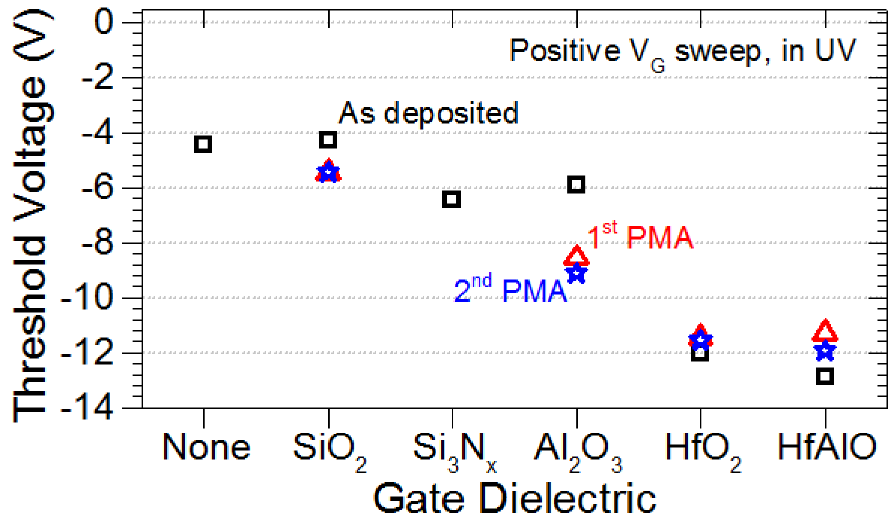


Figure 5.4: Threshold voltage, V_T, extracted using the linear extrapolation method on I_D-V_G curves at low V_D, for different dielectrics and two different annealing conditions listed in Table 4.1.

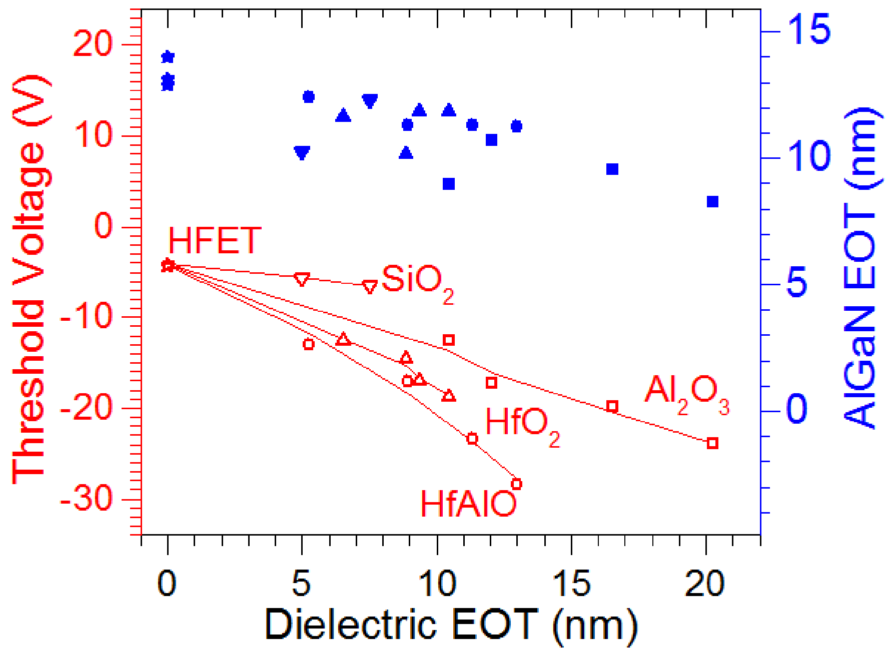


Figure 5.5: Threshold voltage of MOSHFETs with dielectrics of varying thickness after a PMA at 400°C, extracted using CV curves in UV vs. equivalent oxide thickness (EOT) of the gate dielectric. The lines connect the corresponding threshold voltage values predicted by the fit. Gate dielectric EOT was estimated using CV measurements of capacitors on monitor-Si wafers which went through the same gate dielectric deposition/etch/anneal processes. Also shown is an estimate of the AlGaN barrier EOT obtained by subtracting the dielectric EOT from the EOT of the total stack, measured from MOSHFET CV.

CV measurements of large gate area MOSHFETs were taken under UV illumination with a positive direction gate sweep. An estimate of the threshold voltage was extracted as the gate voltage corresponding to a gate capacitance of $0.5*C_{floor}$. Figure 5.5 shows a plot of the same as a function of dielectric EOT. By assuming a uniform bulk fixed charge density in the dielectric and normalizing all thicknesses to EOTs, (5.1) can be reduced as (5.2).

$$V_T = \left[\frac{\phi_{MS}}{q} + \psi_{s,max}\right] + Q_D \frac{\left(t_{ox,EOT} + t_{B,EOT}\right)}{\varepsilon_{SiO_2}} - \frac{q\sigma_{pol} t_{B,EOT}}{\varepsilon_{SiO_2}} - \frac{t_{ox,EOT}}{\varepsilon_{SiO_2}}\left[Q_{it} + Q_F + \frac{\left(\rho_{ox}\frac{\varepsilon_{SiO_2}}{\varepsilon_{ox}}\right) t_{ox,EOT}}{2}\right] \tag{5.2}$$

While the same trend in V_T is seen between the dielectrics for all dielectric thicknesses, prediction of spatial charge using (5.2) is complicated by variation in the AlGaN thickness over the wafer. Therefore, to minimize potential errors in fitting, a larger set of dielectric thickness values is recommended. But, in the current scenario, in order to obtain reliable fits, the term $\left[\frac{\phi_{MS}}{q} + \psi_{s,max}\right]$ and $\frac{q\sigma_{pol}}{\varepsilon_{SiO_2}}$ are set to constant values of 1.6 V and 0.5878 V/nm, assuming:

- ϕ_M = metal work function = 4.6 eV;
- ϕ_S = GaN work function = electron affinity + band gap = 3+3.4 = 6.8 eV [57];
- $\psi_{s,max}$ = maximum potential drop in semi-isolating GaN = band gap = 3.4 eV;
- σ_{pol} = 1.2685E13 cm^{-2} corresponding to 23% Al concentration in the barrier.

In Figure 5.5, connecting lines show the threshold voltage values predicted by the extracted fitting parameters, taking into account the variation of the AlGaN thickness. A good match is observed with the measured values. Further, the background GaN acceptor doping concentration back-calculated from the estimate of Q_D is also found to be reasonable

and uniform across samples. These are good indicators of a reliable fit. The interface and bulk charge densities extracted for different dielectrics are listed in Table 5.1.

All the attempted ALD dielectrics are found to create a positive interface charge of similar magnitudes (1-3 $\times 10^{13}$ cm^{-2}). The interface positive charge extracted by this method is a combination of positively charged donor traps and fixed charges. While a clear trend in trap densities has been observed in Figure 4.8, the exact contribution of donor traps to the extracted interface charge is currently unknown. More significantly, Table 5.1 shows a wide variation in bulk dielectric fixed charge between the different dielectrics. ALD HfO_2 and HfAlO are found to possess a high density of positive bulk charge. In contrast, ALD Al_2O_3 contains negligible bulk charge and ALD SiO_2 potentially has a high density of negative bulk charge.

Table 5.1: Interface and bulk charge densities extracted for different ALD dielectrics from measured values of threshold voltage from Figure 5.5 using (5.2). All the dielectrics have been annealed in N_2 at 400°C. The asterisk ('*') indicates a fit for the ALD SiO_2 case assuming no bulk fixed charge. The reliability of fit can be improved by having a larger set of dielectric thicknesses, especially in the case of SiO_2.

Dielectric	Dielectric constant	Interface charge (cm^{-2})	Uniform bulk charge (cm^{-3})	Root mean square error	Back-calculated GaN acceptor doping (cm^{-3})
ALD SiO_2	3.9	2.23×10^{13}	-3.03×10^{19}	0.155	3.03×10^{17}
ALD SiO_2*	3.9	1.19×10^{13}	0	0.4431	2.94×10^{17}
ALD Al_2O_3	9.6	2.63×10^{13}	2.29×10^{17}	0.868	2.91×10^{17}
ALD HfO_2	18.5	2.97×10^{13}	3.78×10^{19}	0.469	2.92×10^{17}
ALD HfAlO	14	2.90×10^{13}	7.96×10^{19}	1.000	2.65×10^{17}

5.5 Summary

The use of high-k dielectrics enables a significant reduction in gate leakage by allowing a physically thicker dielectric that increases the tunneling distance, for the same gate capacitance. But, in Chapter 4, all the high-k ALD dielectrics (Al_2O_3, HfO_2 and HfAlO)

are found to create a high density of donor traps at the dielectric/AlGaN interface. These traps are found to make the ON-state characteristics unreliable.

Owing to a high conduction band offset with AlGaN, ALD SiO_2 after a post-metallization anneal at temperature $\geq$ 600°C, is found to reduce the gate leakage more than three orders of magnitude below that of a HFET. A low density of traps at the SiO_2/AlGaN interface helps achieve very reliable ON-state characteristics. Additionally, the smallest interface charge density with the possible presence of a negative bulk fixed charge ensures a minimal negative shift in device threshold voltage. Therefore, this is a highly suitable candidate for use as a MOSHFET gate dielectric.

CHAPTER 6: Role of Surface Passivation for Improved Access-Region Reliability

6.1 Introduction

While Chapter 5 investigates dielectrics for gate stack reliability, Chapters 6 and 7 are dedicated towards understanding the issues of access region reliability. In this chapter, we use gate-lag measurements to develop a fundamental understanding of the parameters that affect surface trapping phenomena in the access regions. We then use this knowledge to identify the best ALD dielectrics for improved access region reliability in Chapter 7.

Note that in a MOSHFET, trapping phenomena at the dielectric/AlGaN interface in the gate stack can interfere with signals associated with access region trapping. But in contrast, the HFET has a very reliable Schottky gate which screens any traps located at the gate metal/AlGaN interface. Therefore, the HFET structure is preferred over the MOSHFET for investigation of access region trapping. All the results in this chapter are from HFETs fabricated by the process flow outlined in section 2.1.3.

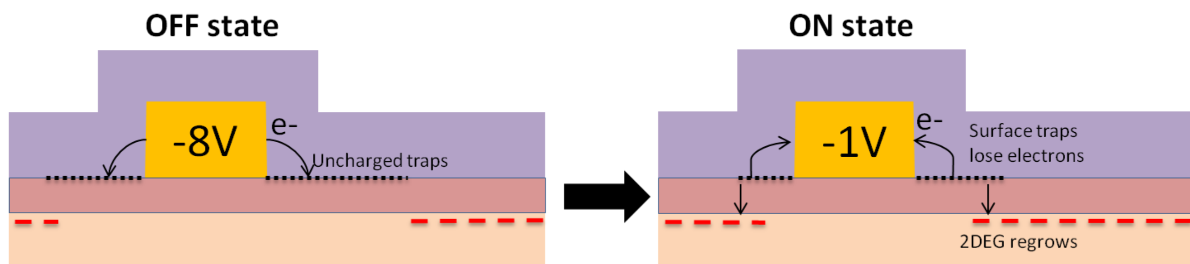


Figure 6.1: A sketch showing an HFET device cross section and the trapping phenomena during a gate lag measurement. Here, the HFET $V_T \approx$ -3 V. The gate is kept at V_T-5V, when OFF, and V_T + 2V, when ON.

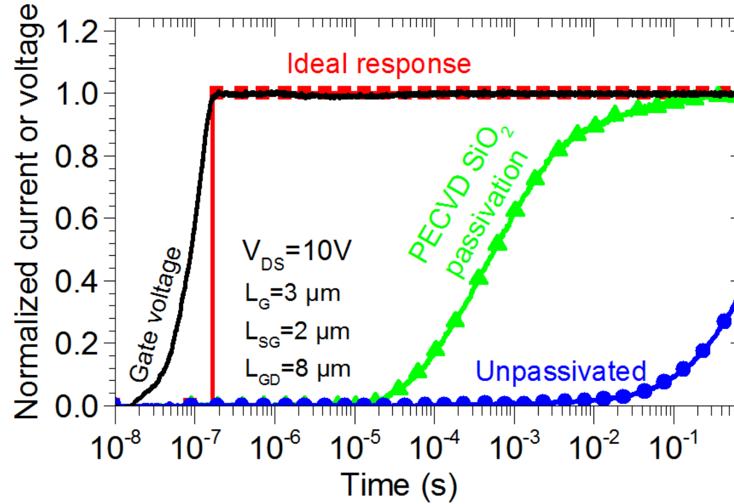


Figure 6.2: Experimental transient drain current, in symbols, and gate voltage, normalized to their respective dc values, for an HFET device (on GaN-SiC_2 wafer, Table 2.1) before and after passivation with 200 nm of PECVD SiO_2. Also shown is the ideal current response expected in a reliable HFET device. The HFET $V_T \approx -3$ V. The gate voltage is kept at V_T-5V for 250 ms, when OFF, and $V_T + 2$V for 750 ms, when ON.

6.2 Gate-lag measurement: A window into surface trapping

Surface traps are believed to be the primary cause for "current collapse" due to the formation of a "virtual gate" [4], [12], as has been highlighted in section 1.3.1. Gate-lag measurements have been used as an effective technique for evaluating the characteristics of surface trapping and the extent of current collapse [62], [63].

The gate-lag measurement involves two steps. In the first step (Figure 6.1), the channel is turned off with a gate voltage much lower than the device threshold. Electrons trickle at the AlGaN surface from the gate, which is at a higher energy, to the traps at the AlGaN surface, which are at a lower energy. In order to maintain charge neutrality, this "virtual gate" [12] creates an equal opposite charge at the 2DEG underneath, depleting the 2DEG. After reaching steady state, Figure 6.1 shows the application of a quick voltage pulse to turn the device on, a few volts above threshold voltage. The transient drain current response to this gate pulse is now influenced by the slow de-trapping of the surface traps, reduction of the "virtual gate" and a replenishment of the access-region 2DEG, as shown in Figure 6.2. The

drain voltage is held at a constant voltage (10 V) throughout the measurement. The faster the transient drain current reaches steady state, the lower the current collapse or the AC-DC IV dispersion is expected to be. Figure 6.2 shows that, ideally, the current should recover fully and immediately to the steady state value by the end of the gate pulse rise time. But in reality, for a fabricated HFET device, an unpassivated sample shows a complete collapse of current at 1 μs after the pulse and only recovers ≈ 40 % of the steady state value in 1 s. When passivated with PECVD SiO_2, the same device shows significant improvement in time of recovery, ≈ 90% recovery in 10 ms.

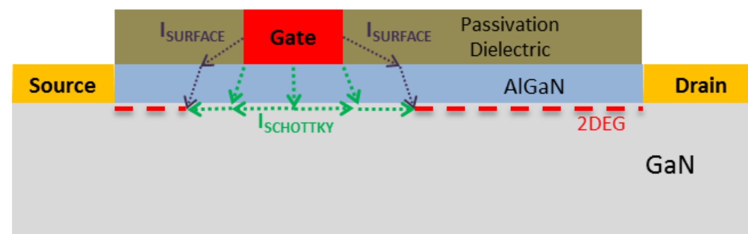


Figure 6.3: A sketch of the generic AlGaN/GaN HFET structure, with large negative gate voltage. Current paths $I_{SURFACE}$ (along the AlGaN surface) and $I_{SCHOTTKY}$ (Schottky leakage under the gate) constituting the total gate leakage are also illustrated.

6.3 Impact of passivation dielectric on gate-lag

6.3.1 Introduction

As evident in Figure 6.2, the use of a passivation dielectric has been found to subdue current collapse, with PECVD SiN being the most popular choice among many dielectrics under active investigation [17], [18], [36], [44]-[47], [64]-[66]. Some of the previously proposed mechanisms of current collapse are leakage at the AlGaN surface [18], [19], [66], ionization of air under high electric field at the gate edge [17] and interaction of the AlGaN surface or the passivation dielectric with moisture [36]. Although seemingly unrelated, they all point toward the same issue of a worsening passivation quality and a promotion of

leakage either through the passivation bulk or the passivation dielectric/AlGaN interface, when the device is turned off. Both these leakage paths are commonly referred to as leakage at the AlGaN surface [18], [19], $I_{SURFACE}$, as shown in Figure 6.3, which can enable the gate to interact with the surface traps and cause current collapse. Therefore, a reduction of the surface current, with the use of an optimal passivation dielectric, can be expected to minimize current collapse.

In effect, in a simple HFET device with a rectangular gate, the nature of a passivation dielectric (composition, thickness, etc) and the fabrication process (PECVD, ALD, additional post-deposition anneals) can affect the following fundamental properties of the access region.

1. Magnitude of surface leakage, either through the passivation dielectric bulk or at the dielectric/AlGaN interface.
2. Profile and density of traps at the dielectric/AlGaN interface and the dielectric bulk.
3. Dielectric constant of the passivation dielectric.

Two preliminary experiments were performed to assess the impact of these factors in the resulting gate-lag behavior.

6.3.2 Preliminary experiment 1

An HFET was fabricated on the GaN-SiC_2 wafer (Table 2.1) with a passivation stack comprising 10 nm ALD HfAlO and 200 nm PECVD SiO_2. Gate-lag measurements were performed on the device at the following five stages and are shown in Figure 6.4:

Stage 1: Fresh HFET device is fabricated with *10 nm ALD HfAlO and 200 nm PECVD* SiO_2 as passivation dielectric.

Stage 2: 140 nm PECVD SiO_2 is wet-etched using a Buffered Oxide Etch (BOE) solution. So, the passivation dielectric comprises of *10 nm ALD HfAlO and 60 nm PECVD* SiO_2.

Stage 3: All the PECVD SiO_2 is wet-etched using the BOE solution. So, the passivation dielectric comprises of *10 nm ALD HfAlO*.

Stage 4: The sample is annealed at 600°C in N_2 for 60 s in a rapid thermal anneal furnace. So, the passivation dielectric comprises of *annealed 10 nm ALD HfAlO*.

Stage 5: 200 nm PECVD SiO2 was re-deposited on the sample. So, the passivation dielectric comprises of *annealed 10 nm ALD HfAlO and as-deposited 200 nm PECVD SiO_2*.

Leakage current measured between contacts, isolated by mesa etching, is relatively unaffected between stages {1-2-3} or {4-5}, but shows a reduction of around three orders of magnitude after annealing, between stages {3-4}. Since annealing is not expected to change the substrate properties, this leakage is expected to be predominantly at the surface of the etched GaN.

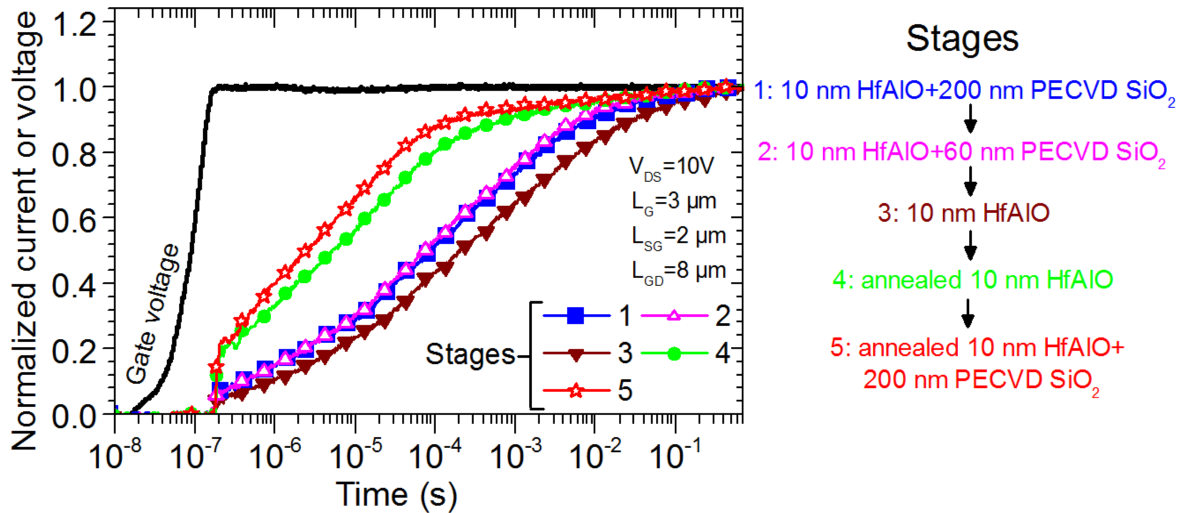


Figure 6.4: Gate-lag curves for HFET fabricated on GaN-SiC_2 wafer (Table 2.1) with a passivation stack comprising 10 nm ALD HfAlO and 200 nm PECVD SiO_2. Stages 1-5 refer to measurements after different process steps and are elaborated in this subsection 6.3.2.

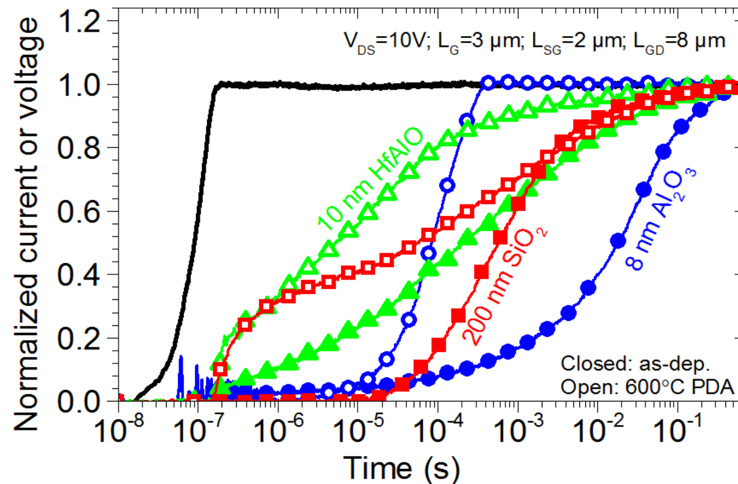


Figure 6.5: Gate-lag curves for HFETs fabricated on GaN-SiC_2 wafer (Table 2.1) with different passivation dielectrics: 8 nm ALD Al_2O_3, 10 nm ALD HfAlO and 200 nm PECVD SiO_2. Also shown are the gate-lag curves measured after post-deposition annealing at 600°C.

6.3.3Preliminary experiment 2

Two more HFET samples were fabricated on the GaN-SiC_2 wafer (Table 2.1) with two different passivation dielectrics: 8 nm ALD Al_2O_3 and 200 nm PECVD SiO_2. The results of gate lag measurements on these devices, before and after annealing, are shown in Figure 6.5, along with the results from stages 3 and 4 of the ALD HfAlO passivated device in subsection 6.3.2.

6.3.4 Preliminary conclusions

The following hypotheses can be used to explain the gate-lag curves measured in Figure 6.4 and Figure 6.5.

1. Comparing stages (1, 3) and (4, 5) in Figure 6.4, it is likely that the thick PECVD SiO_2 layer slightly reduces the surface leakage through the bulk of the passivation stack and results in an improvement in recovery current.
2. Comparing stages 1 and 2 in Figure 6.4, no change in gate-lag is seen after etching 140 nm of PECVD SiO_2. But, the curve slightly worsens after removing the remaining 60 nm

of SiO_2. Therefore, it appears here that the surface leakage through the passivation bulk is limited to within 60 nm of the PECVD SiO_2.

3. Comparing stages 3 and 4 in Figure 6.4, a post-deposition anneal is seen to significantly improve both the recovery time and the recovery current. Additionally, a reduction in leakage measured between isolated contacts indicates that annealing results in a significant reduction of surface current. Therefore, the improvement in gate-lag characteristics could be attributed primarily to a reduction in surface leakage. Further, a change in the trap profile at the dielectric/AlGaN interface, during annealing, may also affect the recovery time of the traps and the current.
4. It is evident from the results in Figure 6.5 that post-deposition annealing (PDA) significantly improves gate-lag behavior in all the attempted passivation dielectrics. The annealing step is expected to densify as well as improve the quality of the passivation dielectric bulk [23], [25], [26], [67], thereby reducing the surface leakage and improving the current collapse behavior.
5. Significant difference of recovery times and gate-lag curve shapes between different dielectrics is observed in Figure 6.5. This may be due to a combination of variation in magnitude of surface leakage, difference in the profile and density of traps at the dielectric/AlGaN interface or a difference in the dielectric constant.

6.4 Device Modeling for Understanding AlGaN/GaN HEMT Gate-Lag

6.4.1 Introduction

None of the attempted passivation dielectrics in Figure 6.5 are able to provide the quick recovery of an ideal device portrayed in Figure 6.2. In order to identify the reasons for the same, there is a critical need to develop fundamental understanding of how different device parameters influence the gate-lag curve shape. In this section, a simulation approach, with experimental validation, is used to model the surface leakage and assess its impact on gate-lag. The framework is then used to develop a critical understanding of how parameters like

the device structure, AlGaN barrier and the passivation dielectric can be engineered for minimum gate-lag. The conclusions from this exercise are then used to propose the optimal passivation dielectric stack for the access regions in Chapter 7. The results and discussions in this section are adapted from the original publication in [76].

6.4.2 Simulation Framework

6.4.2.1 Background

Figure 6.6 shows a sketch of the generic AlGaN/GaN HEMT structure under consideration. The high piezoelectric and spontaneous polarization of AlGaN results in the formation of a 2-dimensional electron gas (2DEG) at the AlGaN/GaN interface. It is widely believed that donor traps at the AlGaN surface are the primary source of electrons for the 2DEG [9], [68]. Measurements of gate-lag over different drain voltages reveal that the de-trapping process from these traps is thermionic in nature, but is enhanced by an external field, because of the Poole Frenkel (PF) effect [63], [69]. Surface acceptor-type traps are considered to be sufficiently compensated by donors in fresh devices, not subject to long-term stressing, and have therefore been ignored in this study [68], [70], [71].

Kelvin probe measurements of the AlGaN surface during stress indicated that electrons can migrate to lengths of 0.5–1 μm from the gate edge [72]. Since gate-lag is observed even under low drain biases [63], [69], electron migration to such lengths during gate stress is likely due to low-field conduction processes like variable range hopping (VRH) at the (dielectric or air)/AlGaN interface [19] or PF field-enhanced conduction through bulk traps in the passivation dielectric [18].

Figure 6.7a shows a sketch of the critical physical models required to obtain a realistic simulation of gate-lag. Figure 6.7b summarizes the simplified set of physical models, used in this work and described in the next subsection.

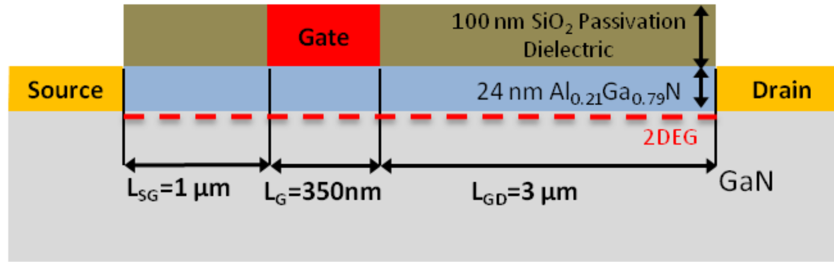


Figure 6.6: Sketch of the generic AlGaN/GaN HEMT structure under investigation. Most simulation results in this section use these device parameters unless mentioned otherwise.

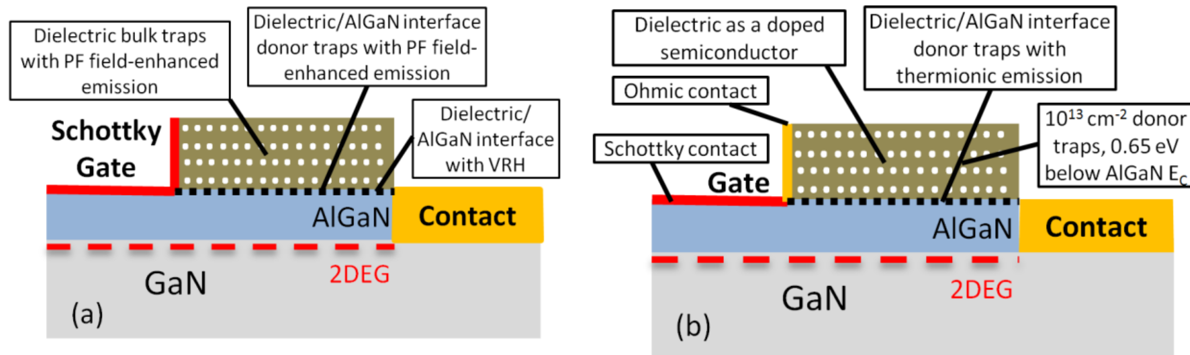


Figure 6.7: (a) Sketch of the critical physical models required to obtain a realistic simulation of gate-lag. (b) Sketch of the simplified physical models adopted in this work. [76] © 2014 IEEE.

6.4.2.2 Model development

The AlGaN/GaN HEMT structure in Fig. 1 is simulated with Synopsys Sentaurus TCAD. Fixed charge sheets of opposite polarities ($\pm 1.15\times10^{13}$ cm^{-2}) are used on either side of the AlGaN barrier to emulate the AlGaN polarization charges. The passivation dielectric is chosen to be 100 nm of SiO_2 and modeled as a semiconductor with appropriate band structure such that Sentaurus solves for the current through the dielectric [73].

The inclusion of the PF model of trap emission requires significant computational overheads. This being a fundamental study aimed at understanding the physics behind the gate-lag phenomenon, a simpler model is devised to reduce the system to a more reasonable

computational complexity that is sufficient to predict the general trends of gate-lag. Both VRH current at the dielectric/AlGaN interface and PF field-enhanced conduction current through the dielectric bulk [74], [75] can be expressed as (6.1).

$$J = qn\mu F \tag{6.1}$$

Here J is the areal or volume current density, n is the areal or volume free electron density, μ is the electron mobility, and F is the applied field. Sophisticated models have been developed to incorporate the additional dependence of μ and n on temperature and applied field [74], [75]. Yet, both these conduction mechanisms are combined together and represented by a simpler drift model by emulating the passivation dielectric with a lightly doped semiconductor. For consistency, the gate metal contact with the passivation dielectric is also made ohmic. At a given temperature, these simplifications ignore the additional exponential dependence of the PF current on the applied field [75] from the negative gate voltage, and therefore underestimate the surface current. Although this can underestimate the gate-lag, for a given AlGaN/GaN substrate condition, we expect that this model is sufficient to show the important trends with the varying device parameters, within the confines of this work.

With the presence of a passivation dielectric, de-trapping of electrons from traps, both at the dielectric/AlGaN interface and in the dielectric bulk, can potentially contribute to the observed gate-lag. For simplicity, both these contributions are combined and represented by thermionic emission of electrons from the traps only at the dielectric/AlGaN interface. At a given temperature, this simplification ignores the additional PF field-enhanced emission from the traps, with a high drain or gate voltage, as shown in measurements from a sample fabricated HFET in Figure 6.8. Although this can overestimate the gate-lag recovery, we expect that it is sufficient to predict the important trends with the varying device parameters.

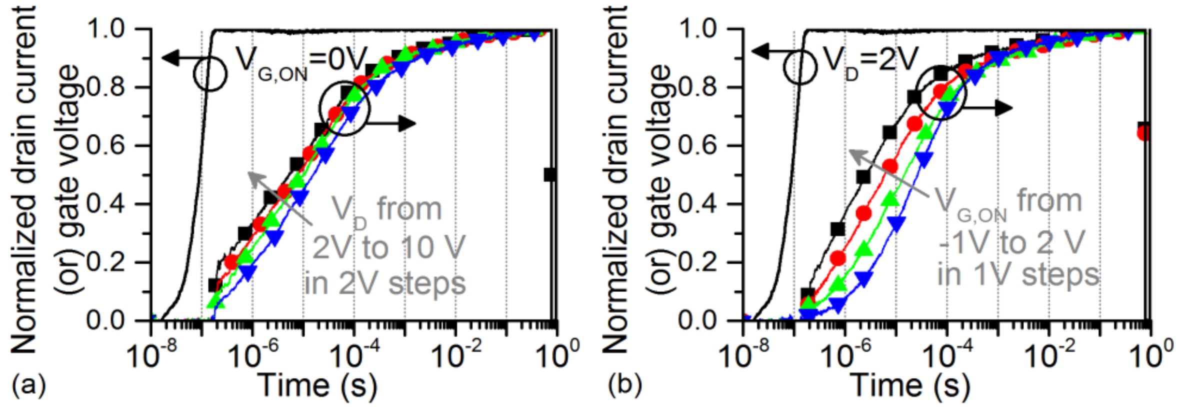


Figure 6.8: Measured gate-lag curves from the HFET at stage 4 in subsection 6.3.2. (a) Enhancement in recovery owing to PF field-enhanced emission with higher drain voltages. (b) Enhancement in recovery with higher ON gate voltages. [76] © 2014 IEEE.

To model a bulk resistivity $\geq 10^6$ Ω.cm, with a reasonable bulk dielectric electron mobility of 20 $cm^2V^{-1}s^{-1}$ [77], a donor concentration per unit area less than 3.12×10^6 cm^{-2} is required. This donor concentration is many orders of magnitude lower than the donor trap density placed at the dielectric/AlGaN interface (10^{13} cm^{-2}, [9], [62]) and the resulting 2DEG sheet concentration (8.5×10^{12} cm^{-2}). This ensures that the contribution of the charge state of the dielectric bulk to the virtual gate formation or reduction is insignificant. Therefore, with the aforementioned simplifications, the physics behind the gate-lag phenomenon is conveniently represented with two decoupled processes. During the OFF state, electrons are supplied to the traps at the dielectric/AlGaN interface through a conductive passivation dielectric of a fixed resistivity. After the removal of negative gate voltage, the thermionic emission of electrons from these traps results in a delayed recovery of the access region 2DEG and the drain current.

It should be noted that the use of a high bandgap SiO_2 passivation dielectric, with no PF model in the bulk traps, inadvertently forces the electrons from the dielectric/AlGaN interface to de-trap only across the relatively lower bandgap material, the AlGaN barrier. But, this is expected to be the preferred direction of de-trapping even in a real device, when the electric field at a surface site in the direction across the thin AlGaN barrier is much

higher than in the direction along the surface. This is the typical operation scenario of an AlGaN/GaN HEMT when the gate is at or below a reasonable positive overdrive (V_{GS} < Schottky gate turn-on voltage ~ 2 V), the drain has a high positive bias and the virtual gate length is much longer than the AlGaN barrier thickness [72]. Therefore, although this reduced model is expected to closely emulate the PF or thermionic emission de-trapping behaviors observed in most literature [63], [69], [70], [78], [79], it is insufficient to describe cases where de-trapping is found to happen back to the gate via surface conduction [80].

6.4.2.3 Gate-lag simulation

The device is solved for a steady state gate voltage 5 V below the threshold voltage, at $V_{G,OFF} = -8$ V and $V_D = 1$ V. It is followed by a gate-lag transient simulation for a gate step going to $V_G = 0$ V, bringing the device to the linear region of operation at DC. The surface donors with capture cross section of 4×10^{-13} cm^2 [48] were kept 0.65 eV below conduction band (E_C) for most simulations, to minimize the initial recovery current at $t_0 = 1$ μs, I_0. Hence, any improvement in gate-lag with variation in a parameter is more easily visible. Although other trap energies are explored in Fig. 8, this value is chosen to be similar to those extracted in [63], [69], [81] and from Figure 6.5 (≤ 0.7 eV) using the same capture cross section, density of states in E_C and thermal velocity as in [48]. The choice of t_0 is representative of an intended application in a switch mode power supply circuit, at around 1 MHz operation frequency [82], [83].

6.4.3 Modeling results

6.4.3.1 Passivation dielectric

A wide range of bulk resistivities (10^6 - 10^{21} Ω.cm) have been reported for many dielectrics at dc or ac [84]-[87]. In subsection 6.3.4, it was proposed that the reduction of bulk traps in the passivation dielectric owing to high temperature anneals can significantly improve gate-lag. Figure 6.9 corroborates our hypothesis by using simulations and shows that I_0 is close to the dc value, I_{DC}, only when the equivalent dielectric bulk resistivity ≥ 10^{10}

Ω.cm. This is because with a higher dielectric bulk resistivity, the access region sees lower influence from the gate, as is indicated by the reduction of the depletion region distance at the gate edges under $V_{G,OFF}$ (Figure 6.10). Figure 6.11 shows the development of the electron density in the channel with time, illustrating the depletion of the 2DEG in the access regions owing to the filled surface donor traps (virtual gate [12]). Eventually, it recovers to the dc profile after the surface donor electron de-trapping process by thermionic emission is complete. Note that in these simulations, $I_{SURFACE}$, through both the dielectric bulk and the dielectric/AlGaN interface, are represented by a simplified bulk leakage through the dielectric. While the contribution of each component may vary in a real device depending on the properties of the dielectric, these simulations suggest that the total $I_{SURFACE}$ must be minimized to eliminate gate-lag.

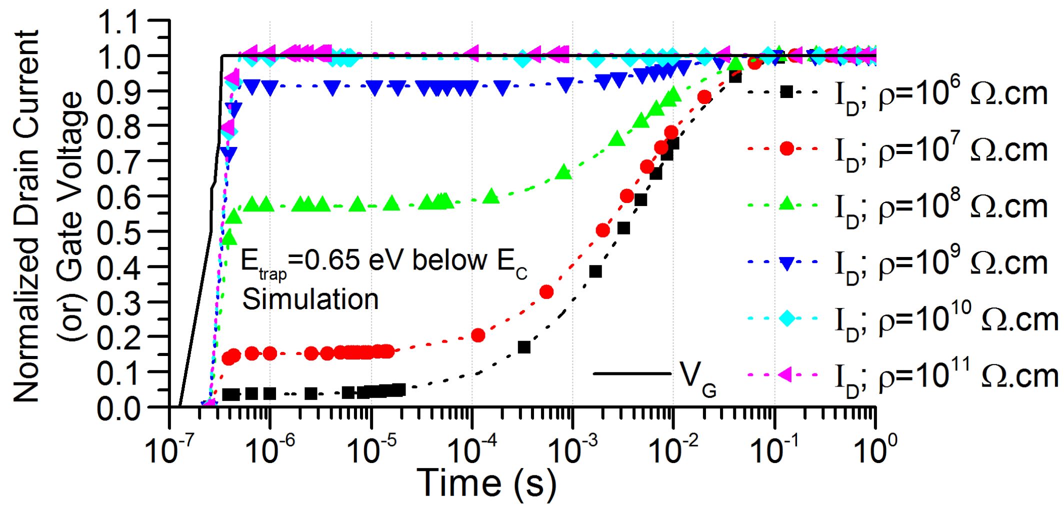


Figure 6.9: Gate-lag for devices simulated with different passivation dielectric bulk resistivities, ρ, in the structure shown in Figure 6.6. [76] © 2014 IEEE.

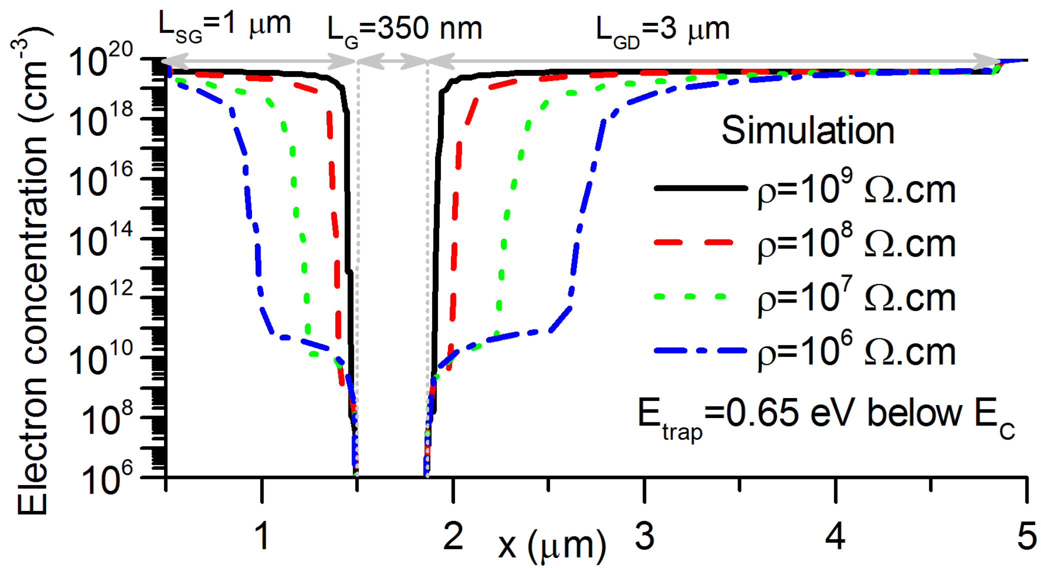


Figure 6.10: Electron concentration versus distance along the AlGaN/GaN interface at $V_{G,DC}$ = -8 V for passivation dielectrics of different resistivities. Worst case depletion region, for $\rho = 10^6$ Ω.cm, extends up to 1.25 μm from the drain edge of the gate (measured as distance at which the electron density is one tenth of the equilibrium concentration). [76] © 2014 IEEE.

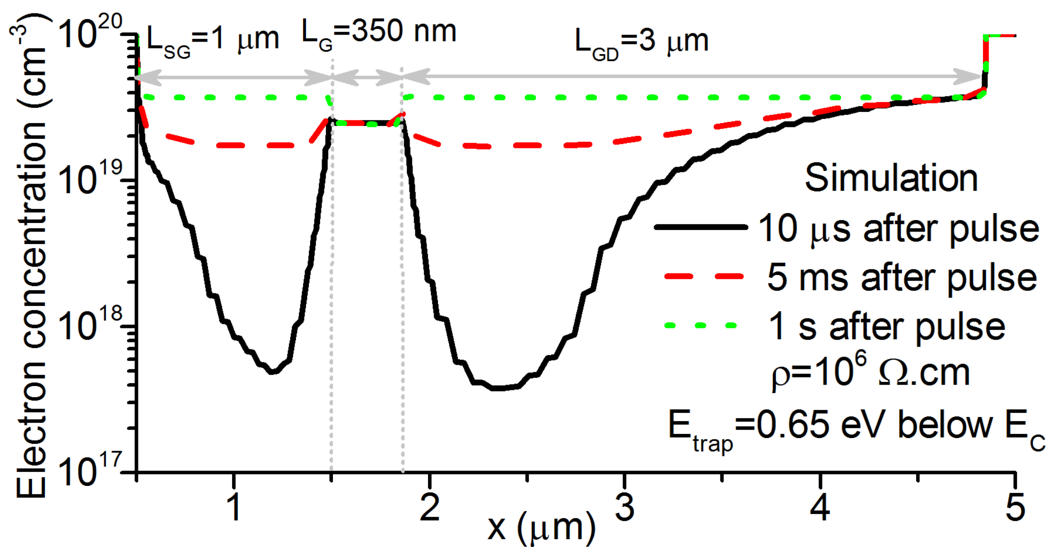


Figure 6.11: Electron density evolution with time along the AlGaN/GaN interface after the removal of $V_{G,OFF}$. While the density under the gate recovers immediately, the access regions take time to reach equilibrium concentrations. This shows up as a reduced drain current that recovers in time (gate-lag). [76] © 2014 IEEE.

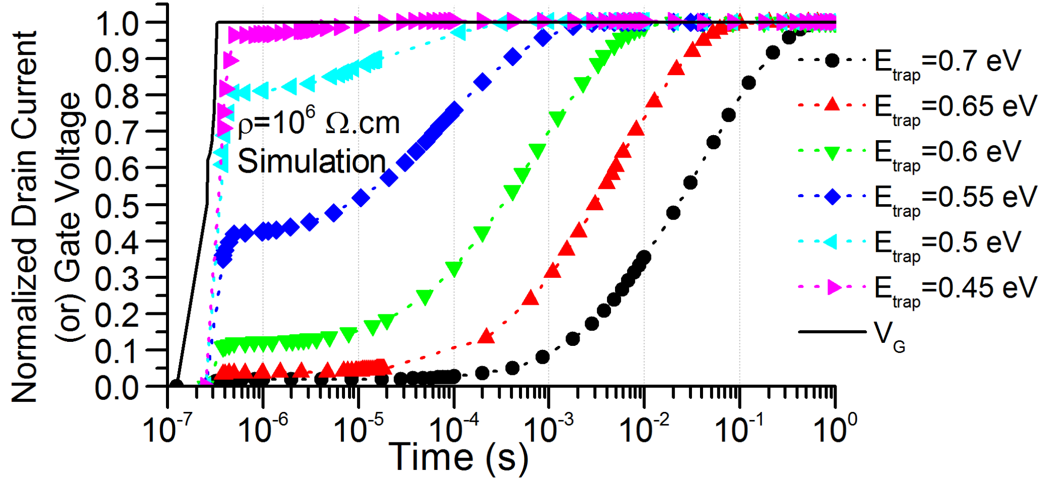


Figure 6.12: Gate-lag for different surface trap energies. A deeper trap is more likely to hold on to an electron during the application of $V_{G,OFF}$. Therefore, deeper traps create a longer depletion region and reduce I_0. The de-trapping process is primarily through leakage across the AlGaN barrier. Therefore, depending on the AlGaN properties, every trap energy corresponds to a unique characteristic time of recovery, t_{DC}. [76] © 2014 IEEE.

The passivation dielectric deposition process can also strongly affect the energy distribution of the surface donors. Although this distribution is complex, a simulation of surface traps at a single discrete energy location with respect to the AlGaN conduction band shows a strong influence on t_{DC}, as well as I_0 (Figure 6.12). Electrons from deeper traps find it harder to de-trap. Since this process is exponential with respect to the trap energy depth [63], [69] and given by (3.1), even a 60 meV deeper trap can result in an order of magnitude increase in recovery time. Further, a deeper trap is more likely to hold its electron and therefore, results in a longer virtual gate and a lower I_0. Experimentally measured curves in Figure 6.5 showing quicker recovery after a PDA indicate a changing surface chemistry and a trap distribution becoming shallower in the case of high-k passivation. With the PECVD SiO_2 passivation, the rise in I_0 and the negligible change in recovery time indicate that the surface leakage reduction with the PDA dominates the enhanced recovery over any trap distribution changes. All the measured curves show dispersion in the curve shape which is representative of the energy dispersion of the surface traps.

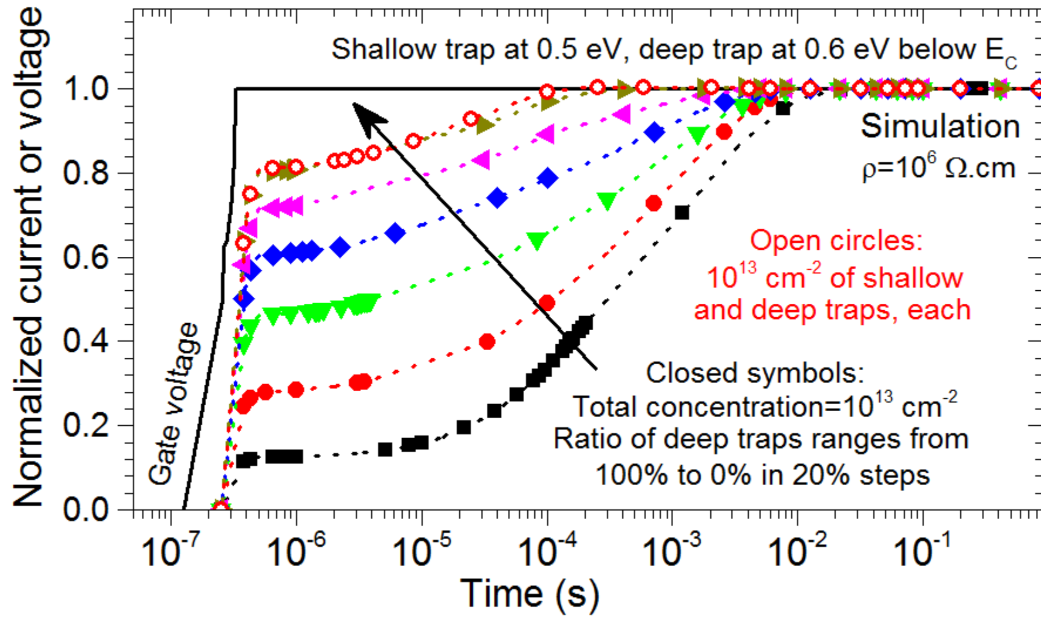


Figure 6.13: Gate-lag simulated for traps at two different trap energies in the same device.

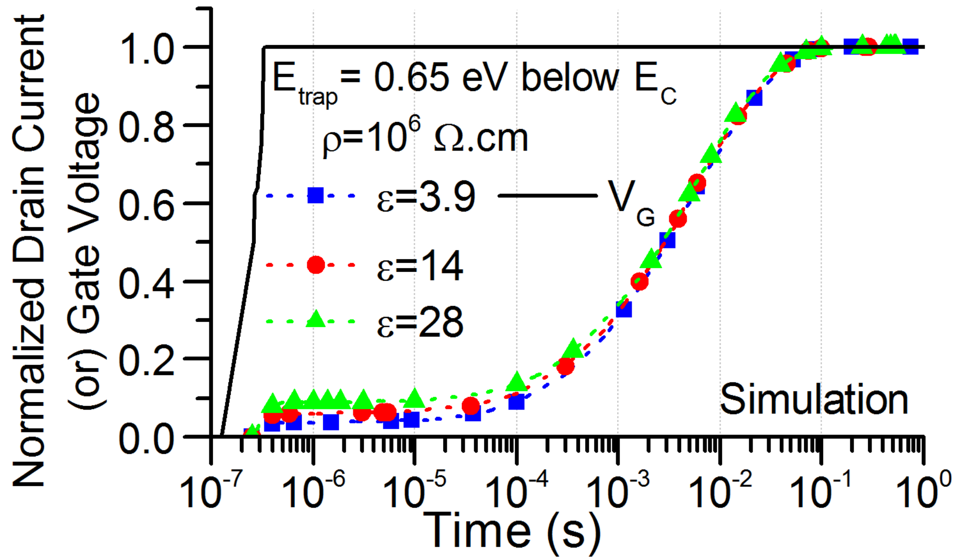


Figure 6.14: Gate-lag versus dielectric constant of the passivation dielectric. A higher capacitive coupling (high-k) with the gate helps in lowering the potential of the surface traps close to the gate edge, after the removal of $V_{G,OFF}$. This results in a minor improvement in the access region 2DEG and I_0. Regardless, t_{DC} is unaffected and is determined only by E_{trap}. [76] © 2014 IEEE.

In a real device, traps at the dielectric/AlGaN interface are spread out in energy, as has been found in Chapter 4. In order to understand the effects of a trap distribution on gate-lag, a simple simulation with traps at two energy levels was performed. The 'shallow' and 'deep' traps were placed at 0.5 eV and 0.6 eV below E_C. Figure 6.13 shows simulated gate-lag curves for multiple trap energy levels with a fixed total concentration of 10^{13} cm^{-2}. It is observed that both I_0 and t_{DC} show progressive improvement with higher ratios of shallow traps.

More importantly, it is found that a device with 10^{13} cm^{-2} each of shallow and deep traps shows exactly the same gate-lag response as that with 10^{13} cm^{-2} of only shallow traps. In section 1.2, the physics behind the formation of the 2DEG at the AlGaN/GaN interface has been elaborated. Surface donors above Fermi level are positively charged and result in the formation of the 2DEG with equal and opposite charge. The charge density in the 2DEG is always less than the total barrier polarization charge [9]. In this case, the 2DEG concentration is $< 10^{13}$ cm^{-2}. In the presence of 10^{13} cm^{-2} each of shallow and deep traps, the shallow trap concentration is more than sufficient to lose their electrons and compensate the entire 2DEG electron density. The deeper traps stay permanently occupied and benign. Hence, in the gate-lag measurement of Figure 6.13, since only the shallow traps actively participate in trapping and de-trapping, the visible gate-lag is close to the case which has only shallow traps. Thereby, it is also concluded that for a quick current recovery, irrespective of the presence of deep traps, the presence of a high density of shallow traps is highly desirable.

The dielectric constant of the passivation dielectric only had a minor effect on the gate-lag curves (Figure 6.14), but favors a low-k dielectric to minimize the parasitic gate capacitance and maximize the switching frequency.

With the use of a high resistivity passivation dielectric, a reduction in the virtual gate length implies a smaller potential drop across it, during the application of $V_{G,OFF}$. This leads to a higher field at the gate edges owing to a higher potential drop across the AlGaN barrier. The resulting reduction in the tunneling distance promotes tunneling current at the gate

edges, which dominates the total Schottky gate leakage [88]-[90], $I_{SCHOTTKY}$, as shown in the simulated conduction band profiles and the corresponding leakage currents shown in Figure 6.15. Figure 6.15b also shows a saturation of Schottky gate leakage both at low ($<10^8$ Ω.cm) and high ($>10^{12}$ Ω.cm) passivation resistivities, because of the potential dropping primarily across the virtual gate or the AlGaN barrier, respectively.

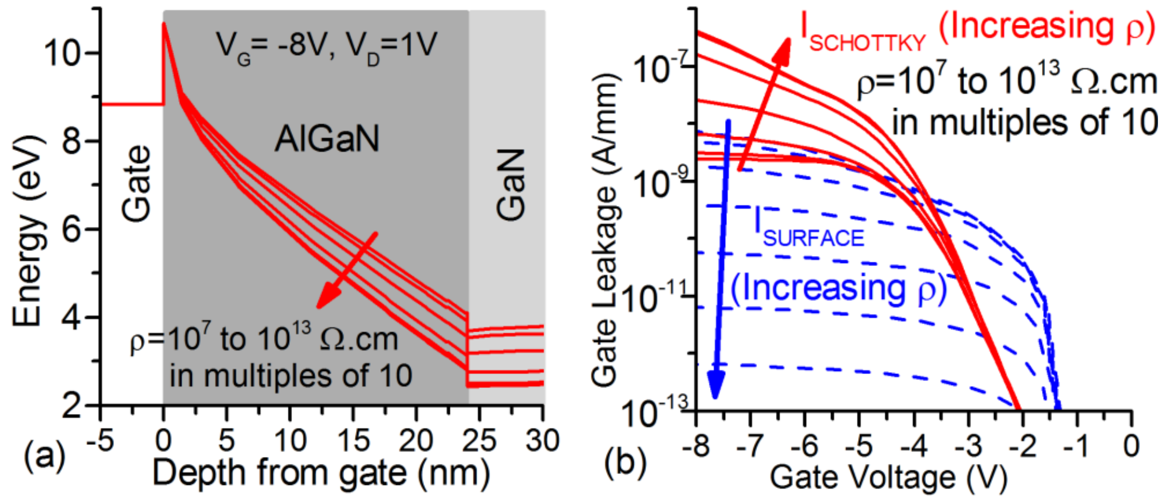


Figure 6.15: (a) Conduction band profiles, for different passivation bulk resistivities, ρ , at the drain side edge of the gate, at $V_{G,OFF} = -8$ V. (b) Simulated gate leakage ($I_G - V_G$) from the Schottky gate ($I_{SCHOTTKY}$, tunneling across AlGaN barrier) and the sides ($I_{SURFACE}$, through the passivation dielectric). [76] © 2014 IEEE.

This phenomenon of gate leakage increase with the deposition of passivation dielectrics has been previously observed and systematically studied by Tan et al. [18], [66], over different temperatures. Tunneling leakage across the Schottky barrier is relatively more temperature independent than drift-diffusion transport in the depletion region, created by the virtual gate [88]. Therefore, a change in the observed gate leakage activation energy from their unpassivated (0.2 eV) to the well-passivated SiN samples (0.05 eV, i.e., relatively temperature independent) confirms a higher contribution of the virtual gate to the gate leakage in the unpassivated case. The authors also confirmed a correlation between a low surface leakage and good current collapse behavior [66]. Further, a significant difference in

leakage current between different passivated samples indicates that certain dielectrics in [18], deposited by PECVD, do have an equivalent effective bulk resistivity lower than 10^{12} Ω.cm.

6.4.3.2 Barrier material properties

For traps located at the dielectric/AlGaN interface, the surface trap energy profile can be assumed to be relatively immune to small changes in the AlN content in the AlGaN barrier and determined more by the dielectric/AlGaN interface chemistry [8]. Hence, a higher AlN concentration in the AlGaN barrier reduces the electron affinity of AlGaN and increases the depth of the trap profile below the conduction band. This scenario is shown in Figure 6.16, where a change in AlN concentration from 21% to 25% increases the trap depth by 60 meV, thereby increasing t_{DC} by an order of magnitude, according to (3.1), and reducing I_0. The AlN concentration has a relatively minor impact on I_{DC} owing to a small change in the 2DEG from the AlGaN polarization charge. Regardless, it is also seen that a passivation dielectric with a high resistivity ($\rho \geq 10^{10}$ Ω.cm) can completely eliminate gate-lag. While a thicker AlGaN barrier improves the 2DEG concentration and I_{DC}, it has minimal impact on I_0, as is shown in Figure 6.17.

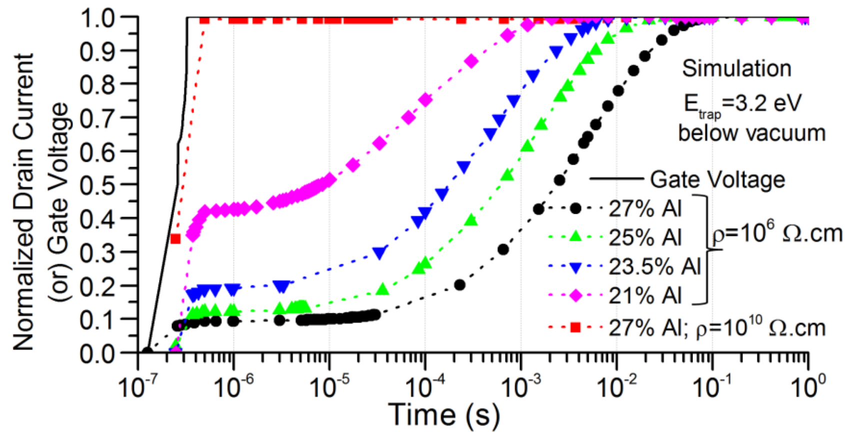


Figure 6.16: Gate-lag simulated for different Al concentrations in the AlGaN barrier layer. E_{trap} of 3.2 eV below vacuum is the same as 0.55 eV below E_C of $Al_{0.21}Ga_{0.79}N$. Also shown is the excellent gate-lag curve for a passivation dielectric with $\rho = 10^{10}$ Ω.cm and a 27% Al concentration. This indicates that passivation dielectric quality is more dominant than substrate properties in determining gate-lag. [76] © 2014 IEEE.

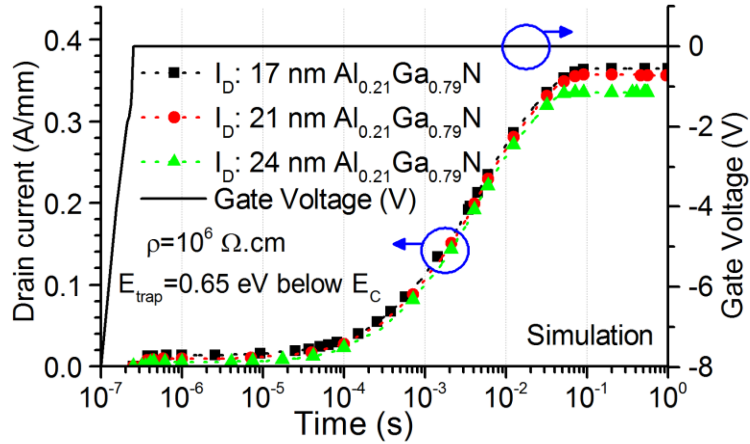


Figure 6.17: Simulated gate-lag versus AlGaN barrier thickness. [76] © 2014 IEEE.

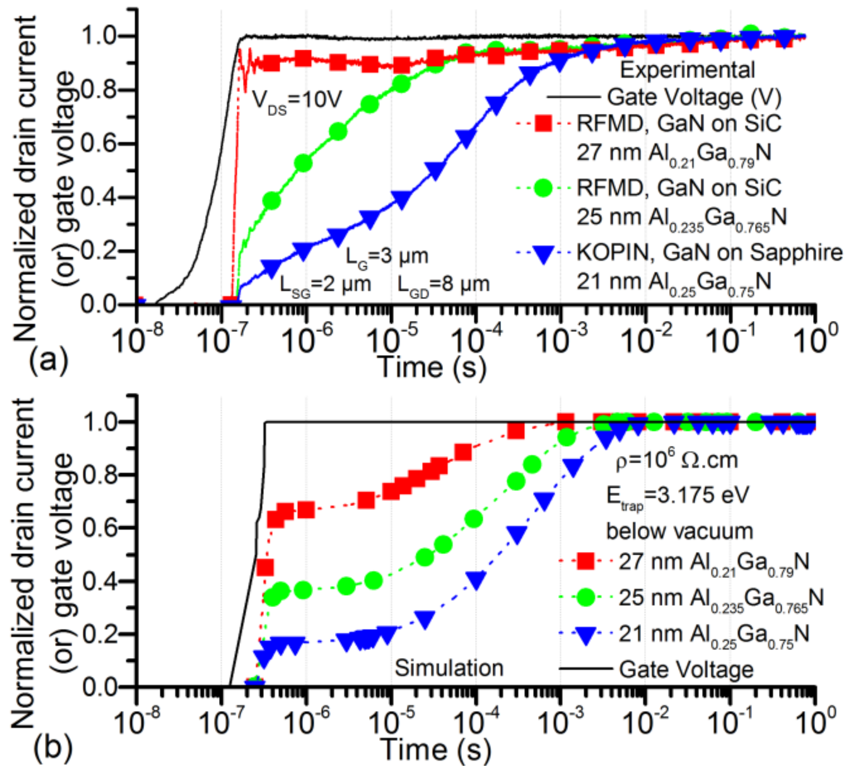


Figure 6.18: (a) Gate-lag measured for HFETs fabricated on GaN-SiC_1, GaN-SiC_2 and GaN-Sap substrates with different barrier properties mentioned in Table 2.1. (b) Gate-lag for HFETs simulated with the same AlGaN barrier properties and using lateral dimensions from Figure 6.6. Because of the difference in device lateral dimensions, dispersion in realistic trap energies and the lack of FP field-enhanced emission model, it is difficult to accurately match the simulated result with the experiments from (a). Nevertheless, the experiments follow the same trends as the simulations. [76] © 2014 IEEE.

Following the fabrication and measurement process outlined in section 2.1.3 and 6.2, gate-lag was measured on PECVD silicon nitride passivated HFETs, fabricated on three substrates, from Table 2.1, with different AlGaN barrier properties, as shown in Figure 6.18a. These experimental curves follow the same trend as predicted by gate-lag simulations with the same set of substrate properties, shown in Figure 6.18b, thereby confirming the findings of the model. Note here that I_0 normalized to I_{DC} is dependent on both the energy location of the trap and the AlGaN thickness. Yet, it appears that the trap energy is the more dominant factor, especially since the 2DEG is already maximized with a sufficiently thick AlGaN barrier in each of the three cases. The time of recovery is purely dependent on the trap energy location. Therefore, we find that, for example, the device with 25% AlN in the AlGaN creates a deeper trap and provides a longer t_{DC} than the one with 21% AlN. Since the barrier properties are experimentally found to influence the trap energy depth, we also conclude that, for the PECVD silicon nitride passivated devices, the surface traps are primarily located at the dielectric/AlGaN interface.

6.4.3.3 HFET structure

A reduction in the source-gate (L_{SG}) and gate-drain (L_{GD}) spacing improves I_{DC} (Figure 6.19). As trapping in the access regions is the dominant mechanism for gate-lag, we also find an improvement in I_0 if we reduce L_{SG} or L_{GD} below the virtual gate length (maximum of 1.25 μm, from Figure 6.10), at the expense of breakdown voltage. Gate length (L_G) can have a strong impact on the I_0/I_{DC} ratio (Figure 6.20). This is primarily because while I_0 is relatively constant, I_{DC} is dominated by the resistance of the channel under the gate, which is proportional to L_G, when short channel effects are negligible.

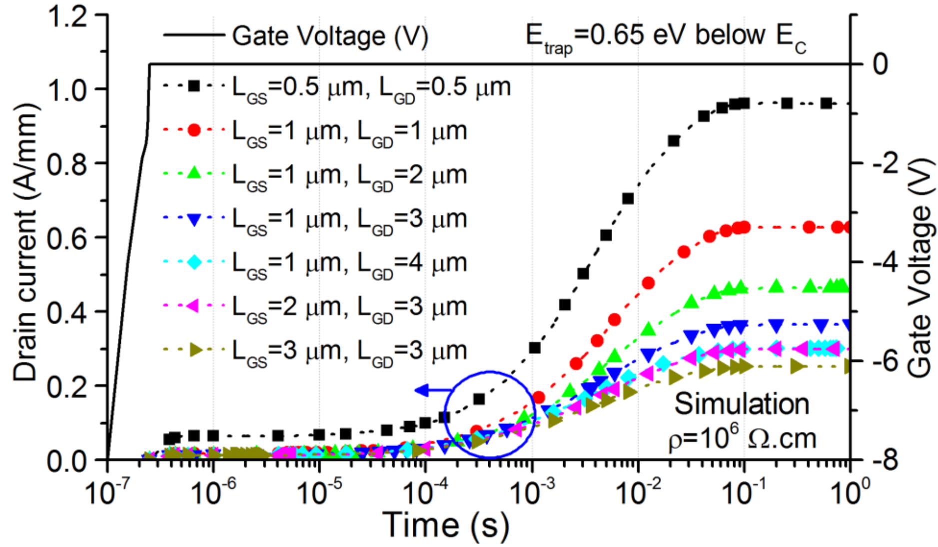


Figure 6.19: Gate-lag simulated for different values of L_{GS} and L_{GD}. In general, an increase in either of these values increases the overall distance between the source and the drain, thereby resulting in a reduction of I_{DC}. An improvement in I_0 becomes visible only when both L_{GD} and L_{SG} are ≤ 1 μm. [76] © 2014 IEEE.

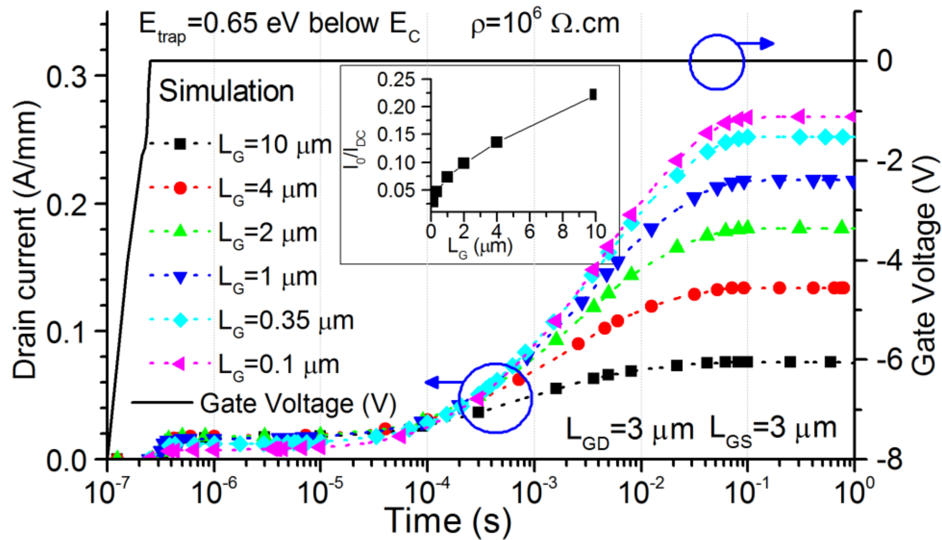


Figure 6.20: Gate-lag simulated for different values of L_G. Inset: that the I_0/I_{DC} ratio follows approximately a straight line versus L_G. A large gate only impacts the resistance of the channel under the gate, and therefore results in a reduction in overall I_{DC}. At 1 μs, the effective resistance between the source and the drain is primarily dominated by the length of the virtual gate. Since the virtual gate length is relatively unaffected by L_G, it has minimal impact on I_0. The reduction in I_0 seen at L_G=0.1 μm is due to edge effects when short channel effects start becoming more dominant. Under such conditions, additional tunneling models at the gate edges should be included to further improve our understanding of the correlation between gate-lag and L_G. [76] © 2014 IEEE.

6.5 Summary

On the basis of the hypothesis that surface leakage is the major cause of gate-lag [18], [19], [66], this chapter has provided a much needed simulation framework with which important device parameters that can potentially influence gate-lag have been studied. The inclusion of more sophisticated physics models like the PF field-enhanced emission is essential to improve the correlation between the simulated and experimental gate-lag curves. The optimal passivation dielectric must minimize surface leakage, through both the passivation dielectric bulk and the dielectric/AlGaN interface, and create a high density of shallow traps at the surface. While controlling both these parameters may be difficult, reducing surface leakage with a high-quality passivation dielectric having an equivalent bulk resistivity more than 10^{10} Ω.cm may be sufficient to eliminate gate-lag. Such a dielectric with low surface leakage could also potentially minimize long-term device degradation.

In an ideal Field Effect Transistor, the choice of the passivation dielectric should not influence the gate leakage. Owing to the creation of a virtual gate, this is not true in the AlGaN/GaN HEMT system. Use of a passivation dielectric with minimal surface leakage (equivalent bulk resistivity > 10^{12} Ω.cm) increases the total gate leakage because of higher fields and current crowding at the gate edge, but potentially makes the device more reliable and reproducible by eliminating the virtual gate.

AlGaN barrier properties like thickness and AlN concentration are also expected to affect the observed gate-lag. Nevertheless, the resulting variation may be minimized by choosing a passivation dielectric that reduces surface leakage. Improvements in the device structure, like access region scaling can further improve gate-lag. If L_{GD} scaling is not possible owing to breakdown voltage concerns, at least L_{SG} scaling is critical to minimize the virtual gate formation near the source edge of the gate. Considerable effort is required in evaluating different passivation dielectrics and substrates for best performance (ac or dc), but it is essential to characterize current collapse with short gate lengths, in order to maximize the observable gate-lag and ensure that any evidence of gate-lag is not missed.

CHAPTER 7: ALD Dielectrics for Access-Region Reliability

7.1 Introduction

In section 6.4, it was concluded that a passivation dielectric, used for improving the access-region reliability of an HFET device, must reduce the leakage between the gate and the donor traps at the AlGaN/GaN interface. Also, the donor traps must be shallow in order to ensure that they can respond to a gate pulse faster and quickly restore the charge in the access region 2DEG channel. In preliminary experimental investigations of section 6.3, it was observed that a post-deposition anneal significantly reduced surface leakage and also improved the gate-lag recovery time. But, while a post-deposition anneal always improved gate-lag, none of the attempted dielectrics in Figure 6.5, thick or thin, provided an ideal gate-lag response. This may have been due to a combination of sub-optimal surface leakage or dielectric/AlGaN interface properties.

In this chapter, a dual stack approach for the passivation dielectric is investigated, aimed at creating an optimal combination of low surface leakage and dielectric/AlGaN interface properties. The first layer is a thin ALD dielectric, which is used to optimize the dielectric/AlGaN interface properties and create shallow traps. The second layer is a thick PECVD SiO_2 layer, which is expected to densify and reduce the extent of surface leakage after post-deposition annealing. The use of thick SiO_2 as the bulk of the passivation dielectric also helps reduce the effective bulk dielectric constant and the resulting parasitic gate capacitance, for RF applications.

The dual stack approach is first investigated on a simple HFET device, using gate-lag measurements, in section 7.2. This section is adapted from the original publication in [47].

Subsequently, it is also verified on MOSHFET devices, using drain-stress measurements up to 200 V, for power applications.

7.2 ALD dielectrics for HFET passivation

HFETs were fabricated on GaN-SiC_1 wafer with the fabrication flow outlined in subsection 2.1.3. The passivation stack consists of 8 nm of dielectric (Al_2O_3, HfAlO or SiO_2) by ALD followed by a thick 200 nm layer of SiO_2 by PECVD. A control HFET sample with the popular PECVD silicon nitride as passivation was also fabricated, for comparison.

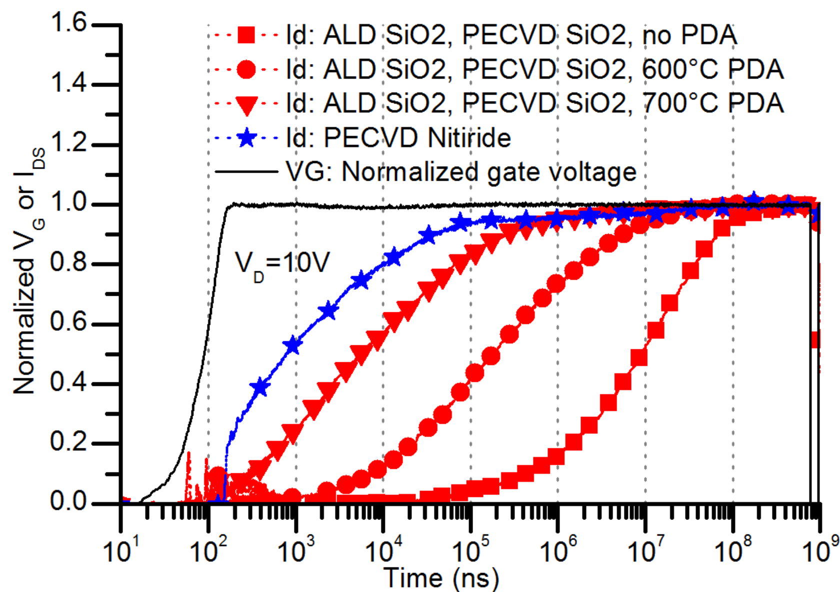


Figure 7.1: Gate-lag for HFETs with a double stack of 8 nm ALD SiO_2 and 200 nm PECVD SiO_2 as passivation, with and without PDA (at 600°C and 700°C). Also shown is the similar plot for the PECVD silicon nitride passivated HFET. Parameters for the measurement are mentioned in Figure 6.2. L_G = 3 μm, L_{SG} = 2 μm and L_{GD} = 8 μm.

Figure 7.1, Figure 7.2 and Figure 7.3 show the results of gate-lag measurement on these devices, before and after post-deposition annealing at different temperatures. In all the three cases, every post-deposition anneal (PDA) improved the gate-lag behavior by

quickening the recovery. In the case of a dual stack with thin ALD SiO_2, the recovery did not become faster than the control sample passivated with PECVD silicon nitride, even after a PDA at 700°C. In contrast, dual stack comprising of high-k dielectrics, Al_2O_3 or HfAlO, after PDA, were found to be as fast as, or even faster, in recovery than the control. Interestingly, while the HFETs with ALD SiO_2 or ALD HfAlO showed their best recovery after a PDA at 700°C, the HFET with ALD Al_2O_3 showed improvement after a PDA of 600°C but slightly degraded with a PDA at 700°C.

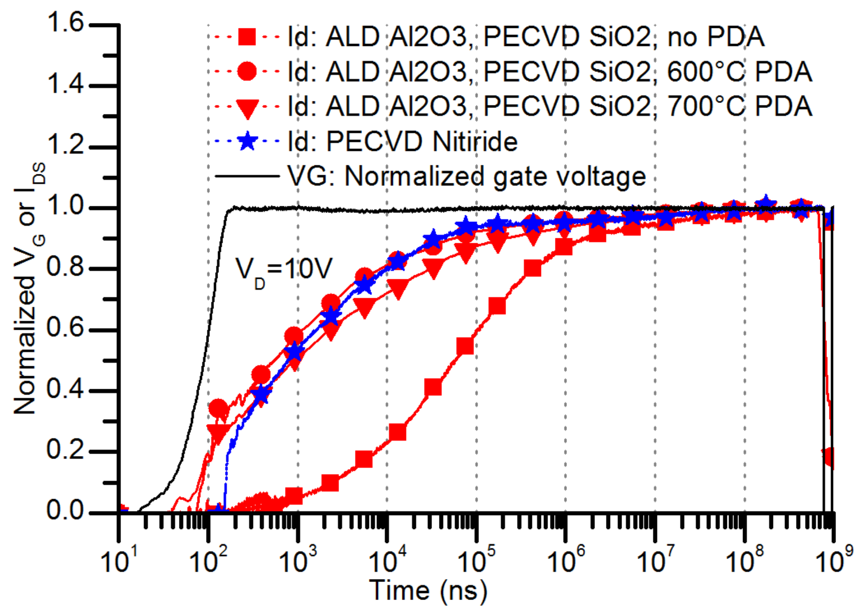


Figure 7.2: Gate-lag for HFETs with a double stack of 8 nm ALD Al_2O_3 and 200 nm PECVD SiO_2 as passivation, with and without PDA (at 600°C and 700°C). Also shown is the similar plot for the PECVD silicon nitride passivated HFET. Parameters for the measurement are mentioned in Figure 6.2. L_G = 3 µm, L_{SG} = 2 µm and L_{GD} = 8 µm. [47] © 2013 IOP Publishing Ltd.

The overall trend in the recovery time for these dual stack passivated samples after a PDA at 700°C is seen to be ALD HfAlO < ALD Al_2O_3 < ALD SiO_2. The exact opposite trend in dielectric/AlGaN interface trap density was observed in Figure 4.8 and Table 4.2. The trap extraction results had also revealed that the total interface trap density was

dominated by shallow traps, most of which are expected to be donor-like owing to their proximity to the conduction band. This confirms the findings of Figure 6.12 and Figure 6.13 that the presence of shallow donor traps quickens current recovery.

In summary, a dual passivation stack comprising of a thin ALD HfAlO layer capped with a thick PECVD SiO_2 layer, after a post-deposition anneal at 700°C, is recommended as the best candidate for access region passivation.

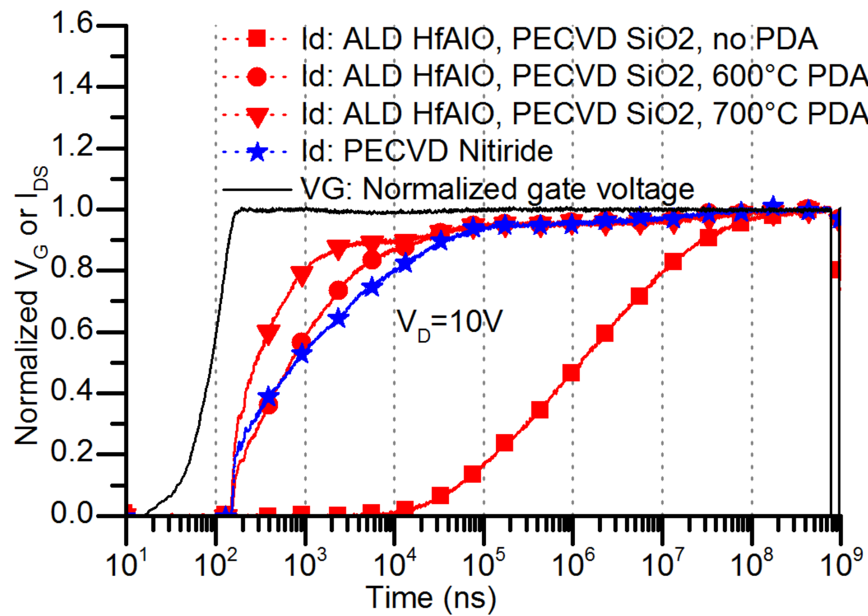


Figure 7.3: Gate-lag for HFETs with a double stack of 8 nm ALD HfAlO and 200 nm PECVD SiO_2 as passivation, with and without PDA (at 600°C and 700°C). Also shown is the similar plot for the PECVD silicon nitride passivated HFET. Parameters for the measurement are mentioned in Figure 6.2. L_G = 3 µm, L_{SG} = 2 µm and L_{GD} = 8 µm. [47] © 2013 IOP Publishing Ltd.

7.3 ALD dielectrics for MOSHFET passivation

Having identified the trends of access region reliability with different dual passivation dielectric stack combinations on HFETs, the same combinations have to be qualified for the final MOSHFET application. To this effect, MOSHFETs were fabricated on a GaN-Si wafer

with scheme B in the fabrication flow outlined in subsection 2.1.4. These samples are the same as used for the trap characterization experiment in section 4.2. Reliability measurements were performed on the MOSHFETs with ALD dielectrics after the second post-metallization anneal (PMA), ie. 700°C in the case of ALD SiO_2, ALD Al_2O_3 and ALD HfAlO and 600°C in the case of ALD HfO_2. The MOSHFET sample with PECVD SiN dielectric was not annealed.

7.3.1 Drain stress measurements

Compared to an HFET, the MOSHFET has a gate that is separated from the dielectric/AlGaN interface by the gate dielectric. The magnitude of surface leakage depends on the quality, band offset and thickness of this dielectric. The gate-lag measurements using the pulsed-IV setup, described in subsection 2.2.3, are restricted to a total pulse period below 1s. This includes both the negative gate pulse and the ON recovery window where the transient gate-lag measurement is taken. In the case of the fabricated MOSHFETs, when the device is turned OFF, this total time duration may be insufficient for the surface leakage current to provide electrons to the surface traps and reach steady state. Additionally, this pulsed-IV setup is incapable of high drain voltage measurements. In order to make a more rigorous measurement of access region reliability at high drain voltages, a new measurement scheme using the Keithley 4200 SCS system (subsection 2.2.2) for long-time drain-stress testing up to 200 V is devised.

The new measurement scheme for MOSHFET access region reliability testing is illustrated in Figure 7.4. A fast I_D-V_G sweep at low V_{DS} is performed for a fresh device. The device threshold voltage, V_T, is defined as the voltage at which the drain current is at 0.1% of the maximum ON current, $I_{ON,0}$, at a gate voltage, $V_{G,ON}$ = 0V. Next, the device is turned off with a gate voltage, 5V below the threshold voltage of the fresh device, $V_{T,0}$. Also, the drain voltage is incremented by 10V for a stress time of 60 s. Immediately after the application of this OFF-state drain voltage stress, a positive direction I_D-V_G sweep at low-V_{DS} is performed

up to $V_{G,ON}$ =0V. A threshold voltage can be extracted from this sweep as the voltage at which the drain current starts recovering and is at 0.1% of the maximum ON current of the fresh device. With the application of increasing drain stress, the visible threshold voltage is also seen to progressively increase, as shown in Figure 7.5. This is because the electrons trapped in the access regions take a finite time to de-trap and create a recovery in the drain current. The current recovery time, t_r, can be estimated as the product of the change in apparent threshold voltage, ΔV_T, and the sweep rate (0.3 s/V) used in the I_D-V_G measurement.

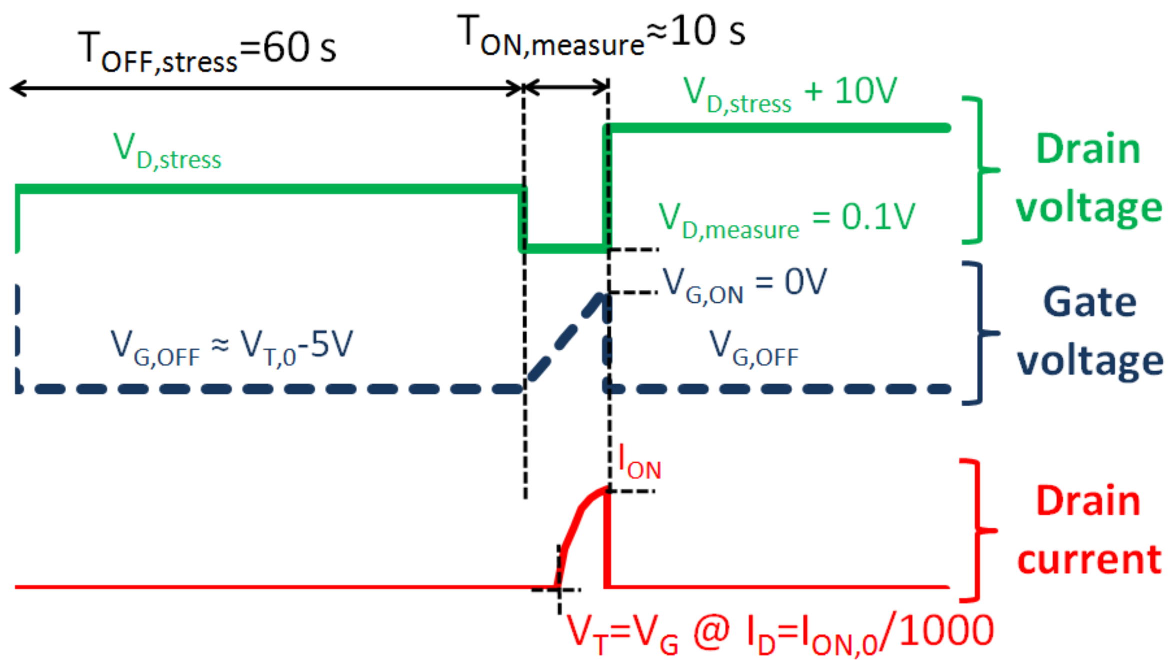


Figure 7.4: Waveforms illustrating a new drain voltage stress reliability measurement methodology using a Keithley 4200 DC measurement setup. Subscript 0 indicates fresh device.

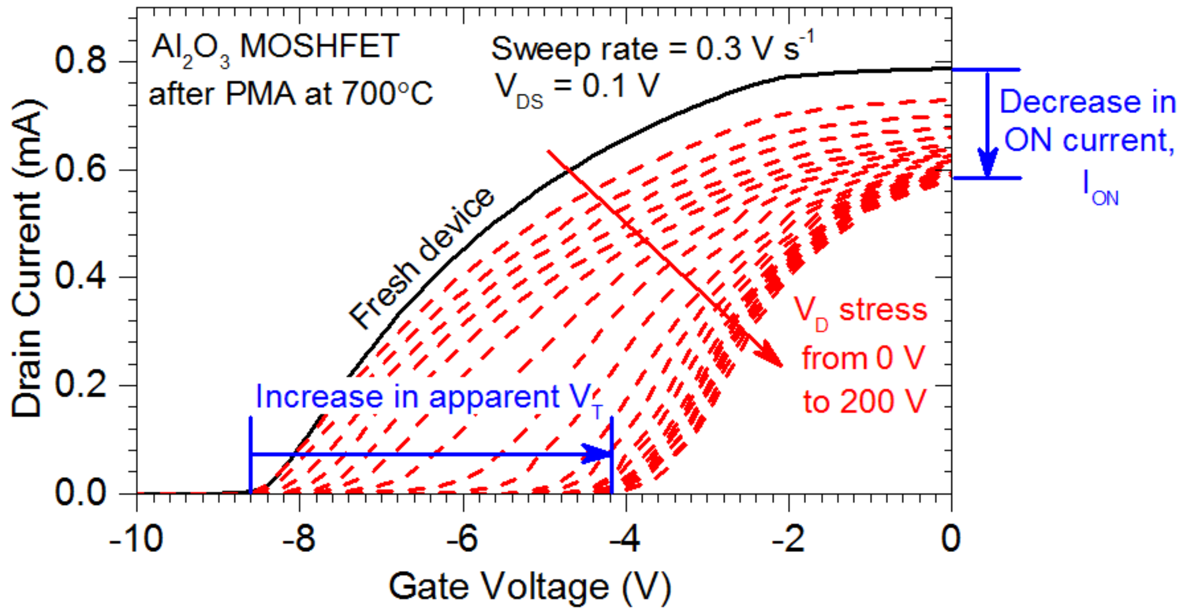


Figure 7.5: I_D-V_G sweep measurements at the end of each drain stress, illustrated in Figure 7.4, on a MOSHFET with Al_2O_3 gate and passivation dielectric, after post-metallization annealing at 700°C. L_G = 9 µm, L_{SG} = 4 µm and L_{GD} = 12 µm.

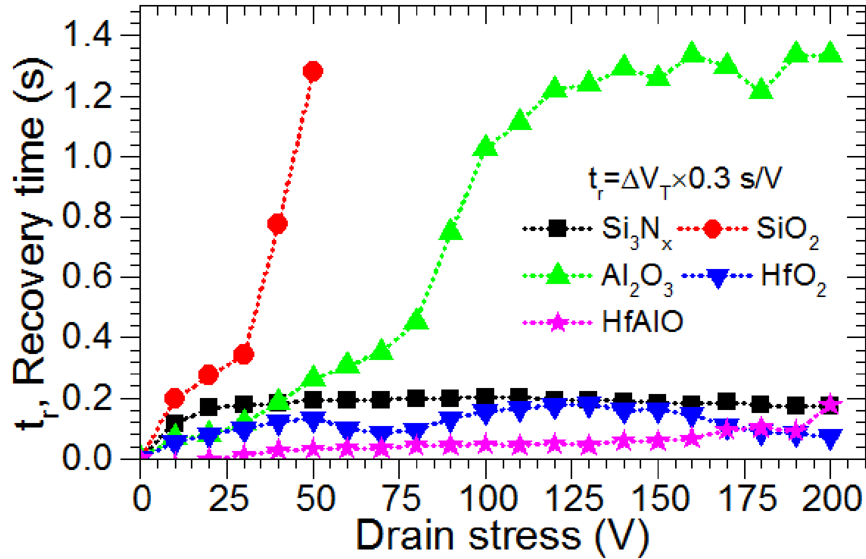


Figure 7.6: Recovery time, t_r, measured for different MOSHFETs as 0.3×ΔV_T s. Stress measurements were performed after PMA at 700°C in the case of ALD SiO_2, ALD Al_2O_3 and ALD HfAlO and 600°C in the case of ALD HfO_2. The MOSHFET with PECVD Si_3N_x gate dielectric was not annealed. In case of SiO_2, beyond a drain stress of 50 V, ΔV_T was outside the range of the I_D-V_G sweep. L_G = 9 µm, L_{SG} = 4 µm and L_{GD} = 12 µm.

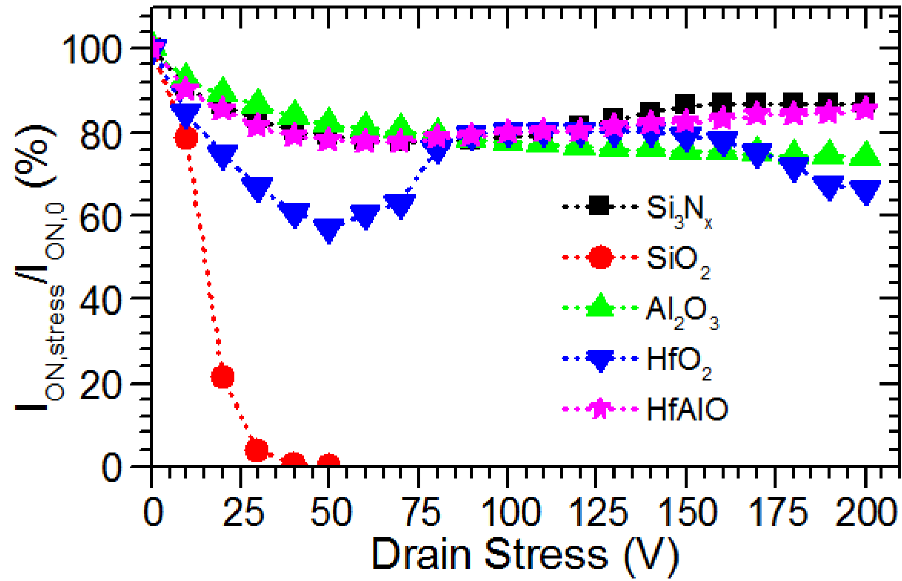


Figure 7.7: Percentage of current collapse with respect to a fresh device, measured at V_G = 0V during the I_D-V_G sweep after each drain stress. Stress measurements were performed after PMA at 700°C in the case of ALD SiO_2, ALD Al_2O_3 and ALD HfAlO and 600°C in the case of ALD HfO_2. The MOSHFET with PECVD Si_3N_x gate dielectric was not annealed. In case of SiO_2, complete current collapse was seen beyond 50 V of drain stress. L_G = 9 µm, L_{SG} = 4 µm and L_{GD} = 12 µm.

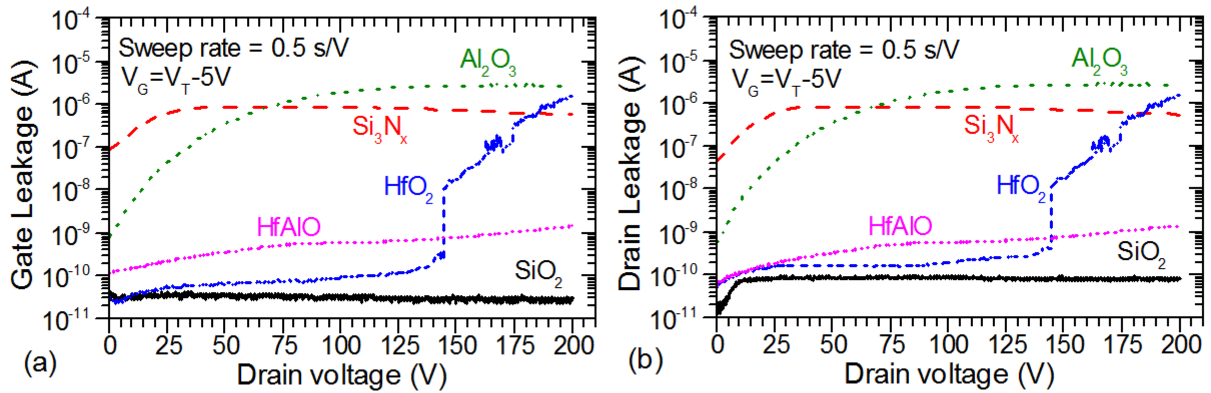


Figure 7.8: OFF-state (a) gate and (b) drain leakage measured over a drain voltage sweep for different MOSHFETs with L_{GD}=12 µm. Measurement was performed after PMA at 700°C in the case of ALD SiO_2, ALD Al_2O_3 and ALD HfAlO and 600°C in the case of ALD HfO_2. The MOSHFET with PECVD Si_3N_x gate dielectric was not annealed. L_G = 9 µm, L_{SG} = 4 µm and L_{GD} = 12 µm.

Figure 7.6 shows a trend in recovery time as ALD HfAlO < ALD HfO_2 < PECVD Si_3N_x < ALD Al_2O_3 < ALD SiO_2. The same trend has been observed in section 7.2 where

these passivation dielectrics were tested on HFETs. The exact opposite trend in dielectric/AlGaN interface trap density was observed in Figure 4.8 and Table 4.2. The trap extraction results had also revealed that the total interface trap density was dominated by shallow traps, most of which are expected to be donor-like owing to their proximity to the conduction band. This confirms the findings of Figure 6.12 and Figure 6.13 that the presence of shallow donor traps quickens current recovery.

Figure 7.7 shows the percentage of current collapse with respect to a fresh device, measured at $V_G = 0$ V during the I_D-V_G sweep after each drain stress. A comparison between Figure 7.6 and Figure 7.7 can be used as an estimate of dispersion in the gate lag recovery shape. The current collapse trend seen here is ALD SiO_2 > ALD HfO_2 > ALD Al_2O_3 > ALD HfAlO ≈ PECVD Si_3N_x. Comparing with the trend in recovery time, it is observed that although HfO_2 starts recovery soon, at drain stress values below 75 V and above 160 V, it takes a longer time to de-trap some deeper traps and recover completely.

7.3.2 Gate-drain isolation

The passivation dielectric strongly influences the surface leakage and the resulting contact isolation. This is a critical parameter that influences device breakdown. The lower the surface leakage, the higher the device breakdown is expected to be. Figure 7.8 shows the measurement of MOSHFET OFF-state gate and drain leakage for different dielectrics with the gate biased at 5 V below V_T. It is observed here that both ALD SiO_2 and ALD HfAlO, after PMA at 700°C, provide the best isolation with a breakdown voltage much beyond 200V.

7.4 Summary

Gate-lag measurements on HFETs and drain-stress measurements up to 200 V on MOSHFETs confirm that an optimal passivation dielectric must minimize surface leakage and create a high density of shallow traps at the dielectric/AlGaN interface in the access

regions. This helps in minimizing “virtual gate” length and ensuring a quick recovery of interface traps and the access region 2DEG after the removal of a gate and drain stress.

A dual dielectric stack approach, comprising of a thin ALD dielectric capped with a thick PECVD SiO_2 layer, was investigated for improved passivation capabilities compared to the popular PECVD silicon nitride. The thin ALD dielectric was used to optimize the properties of the dielectric/AlGaN interface, while the thick SiO_2 helped reduce the magnitude of bulk surface leakage. Additionally, the effect of post-metallization annealing on access region reliability was also investigated.

Owing to a high density of shallow traps, dual dielectric passivation stacks containing high-k dielectrics (ALD HfAlO, ALD HfO_2 and ALD Al_2O_3) provided significantly quicker recovery in drain current than that containing low-k ALD SiO_2, after post-metallization annealing (PMA). Overall, a dual stack containing ALD HfAlO and PECVD SiO_2, after PMA at 700°C, provided a faster current recovery and lower current collapse than PECVD silicon nitride passivation.

Next, passivation stacks containing ALD SiO_2 or ALD HfAlO, after PMA at 700°C, were both found to provide much better source-drain isolation compared to PECVD silicon nitride.

Overall, a dual dielectric passivation stack comprising of a thin ALD HfAlO layer capped with a thick PECVD SiO_2 layer, annealed at 700°C, is recommended as the best candidate for reliable passivation of the access regions and providing good device isolation/breakdown properties.

CHAPTER 8: Conclusions and Future Work

8.1 Conclusions

The objective of this dissertation research is to investigate different dielectrics for improving the reliability of the gate and the access-regions in AlGaN/GaN devices. Atomic layer deposition (ALD) was chosen as the preferred method of dielectric deposition since it is a well-established process that affords the growth of high quality uniform films, low-k and high-k. First, an accurate and comprehensive pulsed-IV based measurement methodology was adopted to characterize traps at the interface between the AlGaN and each different dielectric. Subsequently, MOSHFETs with different gate dielectrics, deposited by ALD, were investigated for gate stack reliability. Next, focusing on the reliability of access-regions, simulation models were used to identify the requirements for an ideal passivation dielectric. This know-how was then utilized to design an optimal passivation dielectric stack incorporating ALD dielectrics. The conclusions of each effort are highlighted herewith. A comparison of results for the different ALD dielectrics is also summarized in Table 8.1.

Characterization of traps at the dielectric/AlGaN interface:

1. Traditional conductance measurement technique for characterizing traps at the dielectric/AlGaN interface has severe limitations when the AlGaN barrier is highly resistive. This is especially so, when an additional thin AlN layer is intentionally sandwiched between the AlGaN and GaN. The exclusive use of capacitance measurements for trap estimation is also restricted in scope by the resolution of the C-V sweep. Additionally, these methods are only capable of measuring shallow traps.
2. A novel methodology using pulsed-IV measurements, under UV illumination, was developed to characterize both shallow and deep traps. This method is found to be immune from issues of barrier resistance and is applicable over a wide range of trap

density values. The accuracy of the novel method was successfully experimentally demonstrated and validated on an AlGaN/GaN MOSHFET device.

3. High-k dielectrics are found to harbor a high density of traps at the dielectric/AlGaN interface, both before and after post-metallization annealing. The overall trend in total trap density is seen to be ALD HfAlO ≈ ALD HfO_2 > ALD Al_2O_3 > as-deposited PECVD silicon nitride > ALD SiO_2, where all the ALD dielectrics have been annealed in N_2 at or above 600°C. ALD SiO_2, after annealing at 700°C, has the lowest total interface trap density below 2×10^{12} cm^{-2}.

ALD dielectrics for a reliable gate stack

1. The use of high-k dielectrics enables a significant reduction in gate leakage by allowing a physically thicker dielectric that increases the tunneling distance, for the same gate capacitance. But, owing to the high density of interface traps, all the high-k ALD dielectrics (Al_2O_3, HfO_2 and HfAlO) are found to make the ON-state characteristics unreliable. Owing to a high conduction band offset with AlGaN, ALD SiO_2 after a post-metallization anneal at 700°C, reduces the gate leakage more than two orders of magnitude below that of a HFET. A low density of traps at the SiO_2/AlGaN interface also helps achieve very reliable ON-state characteristics. Therefore, this is a highly suitable candidate for use as a MOSHFET gate dielectric.
2. All the attempted ALD dielectrics (SiO_2, Al_2O_3, HfO_2 and HfAlO) are found to create similar magnitudes of positive charge (1-3 $\times10^{13}$ cm^{-2}) at the dielectric/AlGaN interface. The exact contribution of donor traps to the extracted interface charge is currently unknown. But more importantly, a wide variation in bulk dielectric charge between the different dielectrics is observed. ALD HfO_2 and HfAlO are found to possess a high density of positive bulk charge. In contrast, ALD Al_2O_3 contains negligible charge and ALD SiO_2 potentially possesses a high density of negative charge. This, again, makes ALD SiO_2 a preferred gate dielectric candidate for achieving minimal negative threshold voltage shift, compared to an HFET.

Requirements for reliable access-region operation

1. The optimal passivation dielectric must minimize surface leakage, through both the passivation dielectric bulk and the dielectric/AlGaN interface, and create a high density of shallow donor traps at the surface. This helps in minimizing "virtual gate" length and ensuring a quick recovery of interface traps and the access region 2DEG after the removal of a gate stress. While controlling both these parameters may be difficult, reducing surface leakage with a highly resistive passivation dielectric may be sufficient to eliminate gate-lag. Such a dielectric with low surface leakage could also potentially minimize long-term device degradation.
2. The requirement of an optimal passivation dielectric/AlGaN interface to possess a high density of shallow traps immediately makes it unsuitable as a gate dielectric. Therefore, it is to be expected that the recommendations of the dielectrics for use in gate stack and the access regions are invariably, different. This is expected to add complexity to the fabrication process of a MOSHFET with different gate and passivation dielectrics.
3. AlGaN barrier properties like thickness and AlN concentration are also expected to affect the surface trapping/de-trapping characteristics. Nevertheless, the resulting current collapse may be minimized by choosing a passivation dielectric that reduces surface leakage.
4. Improvements in the device structure, like access region scaling can further improve gate-lag. If L_{GD} scaling is not possible owing to breakdown voltage concerns, at least L_{SG} scaling is critical to minimize the virtual gate formation near the source edge of the gate.

ALD dielectrics for reliable access-regions

1. A post-deposition anneal is found to significantly improve the gate-lag characteristics of all the ALD dielectrics. This is attributed to a strong reduction in the surface leakage enabled by the densification of the film and a reduction in the bulk traps. The optimal

annealing temperature, in N_2, is different for different ALD dielectrics: 600°C for ALD Al_2O_3 and 700°C for ALD SiO_2 and ALD HfAlO.

2. None of the attempted single passivation dielectrics provided a quick HFET current recovery close to ideal, or that of PECVD silicon nitride passivation. This may have been due to a combination of sub-optimal surface leakage or dielectric/AlGaN interface properties. Hence, a dual stack approach for the passivation dielectric is proposed, in order to create an optimal combination of low surface leakage and dielectric/AlGaN interface properties. The first layer is a thin ALD dielectric, which is used to optimize the dielectric/AlGaN interface properties and create shallow donor traps. The second layer is a thick PECVD SiO_2 layer, which is expected to densify and reduce the extent of surface leakage after post-deposition annealing. The use of thick SiO_2 as the bulk of the passivation dielectric also helps reduce the effective bulk dielectric constant and the resulting parasitic gate capacitance, for RF applications.
3. Gate-lag measurements on HFETs and drain-stress measurements up to 200 V on MOSHFETs confirm that an ideal passivation dielectric must minimize surface leakage and create a high density of shallow donor traps at the dielectric/AlGaN interface in the access regions. Owing to a high density of shallow traps, dual dielectric passivation stacks containing high-k dielectrics (ALD HfAlO, ALD HfO_2 and ALD Al_2O_3) provided significantly quicker recovery in drain current than the low-k ALD SiO_2, after post-metallization annealing (PMA). The dual stack containing ALD HfAlO, after PMA in N_2 at 700°C, provided a faster current recovery and lower current collapse than PECVD silicon nitride passivation.
4. The dual dielectric passivation stacks containing ALD SiO_2 or ALD HfAlO, after PMA in N_2 at 700°C, were both found to provide much better source-drain isolation compared to PECVD silicon nitride.
5. Overall, a dual dielectric passivation stack comprising of a thin ALD HfAlO layer capped with a thick PECVD SiO_2 layer, annealed in N_2 at 700°C, is recommended as the best candidate for an optimal combination of reliable access-region passivation and good device isolation/breakdown properties.

Table 8.1: Simplistic comparison of performance of different ALD dielectrics evaluated in this work for use as a gate dielectric or as a thin passivation dielectric in a dual dielectric stack. The color range red → orange → green indicates undesirable to desirable. The matrix considers the best curves obtained in this work for the different dielectrics at different annealing conditions.

Region	*Performance metric*	*SiO_2*	*Al_2O_3*	*HfO_2*	*HfAlO*
Gate stack	Reduction of gate leakage, for a given gate capacitance				
	Threshold voltage stability				
	Minimal V_T shift to negative direction, for a given gate capacitance				
Access region passivation	Current collapse suppression				
	Gate-drain isolation				

8.2 Future Work

This work lays a solid foundation for investigating dielectrics for gate stack and access-region reliability. While the focus here has been the AlGaN/GaN system, all the methodologies and know-how, developed in this work, are also applicable to other GaN based systems with different barrier materials like AlN or InAlN. These barrier materials are under active investigation to achieve much higher 2DEG concentrations and lower ON-resistance, along with a higher gate capacitance.

In this work, only four different ALD dielectrics, deposited after surface-cleaning in HCl/HF and annealed in N_2 at different temperatures have been explored on AlGaN/GaN. But, ALD offers much more variety in dielectric options than attempted in this work, ranging from binary compounds to ternary/quaternary alloys. The properties of the dielectric/AlGaN interface can also be strongly affected by a different surface preparation technique (eg. plasma pre-treatment with different gases, NH_4OH clean) or a different annealing ambient (eg. N_2O, NH_3, NO_2, O_2, H_2). Thus, this work has only revealed the tip of the iceberg that is

the variety of different combinations of dielectrics, surface preparation and annealing conditions.

Within the limited options explored in this work, ALD SiO_2 annealed in N_2 at 700°C, is recommended as the optimal gate dielectric. But, ALD HfAlO, annealed in N_2 at 700C, is recommended for use in the optimal dual dielectric passivation stack. Incorporating different dielectrics for the gate and the access-regions can potentially add significant fabrication challenges. In this particular case, since SiO_2 is easily wet-etched by a dilute HF solution, the gate metal could be used as a hard mask for etching the SiO_2 gate dielectric from the access regions. Then a new film of ALD HfAlO could be deposited for the dual dielectric passivation stack. This process has been illustrated in scheme A of Figure 2.4. This approach for fabricating an optimal MOSHFET with both a reliable gate and a reliable access-region operation needs to be investigated and validated.

Using the concept of FLASH memory, enhancement mode MOSHFET devices have been fabricated on AlGaN/GaN in [31]. ALD SiO_2 was deposited on AlGaN and used as a tunnel dielectric. Reliable gate stack operation was also demonstrated. But, since the gate dielectric was also used as a passivation dielectric, the ALD SiO_2/AlGaN interface in the access-regions has a low density of shallow traps and can be expected to create significant current collapse. Using the gate metal as a hard mask, the gate dielectric from the access regions could be etched and new film of ALD HfAlO could be deposited for the dual dielectric passivation stack. This process has been illustrated in scheme A of Figure 2.4. This approach for fabricating an enhancement mode FLASH-MOSHFET with both a reliable gate and a reliable access-region operation needs to be investigated and validated.

REFERENCES

[1] Lawrence Livermore National Laboratory and US Department of Energy. (2010). *Estimated US Energy Use in 2009: ~94.6 Quads* [Online]. Available: https://www.llnl.gov/news/newsreleases/2010/images/energy-flow-annotated.pdf

[2] B. J. Baliga, "Introduction," in *Fundamentals of Power Semiconductor Devices*, New York: Springer Science, 2008, ch. 1, pp. 1-22

[3] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol.10, no.10, pp. 455-457, Oct. 1989

[4] U. K. Mishra, P. Parikh, Y.F. Wu, "AlGaN/GaN HEMTs - An Overview of Device Operation and Applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022-1031, 2002

[5] Y. Cordier, T. Fujishima, B. Lu, E. Matioli and T. Palacios, "Nitride-based electron devices for high-power/high-frequency applications," in *III-Nitride Semiconductors and their Modern Devices*, New York: Oxford University Press, 2013, ch. 11

[6] B. J. Baliga, "Gallium Nitride Devices for Power Electronic Applications," *Semiconductor Sci. and Technology*, vol. 28, pp. 074011, June 2013

[7] Richard Eden. (2013). *Market Forecasts for Silicon Carbide and Gallium Nitride Power Semiconductors* [Online]. Available: http://www.apec-conf.org/wp-content/uploads/2013/09/is1.4.2.pdf

[8] M. S. Miao, J. R. Weber and C. G. Van de Walle, "Oxidation and the origin of the two-dimensional electron gas in AlGaN/GaN heterostructures," *J. Appl. Physics*, vol. 107, pp. 123713, 2010

[9] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Appl. Physics Lett.*, vol. 77, no. 2, pp. 250-252, 2000

[10] G. Meneghesso et al., “Reliability issues of Gallium Nitride High Electron Mobility Transistors,” *International Journal of Microwave and Wireless Technologies*, vol. 2, no. 1, pp. 39-50, 2010

[11] U. Chowdhury et al., “TEM Observation of Crack- and Pit-Shaped Defects in Electrically Degraded GaN HEMTs,” *IEEE Electron Device Lett.*, vol. 29, pp. 1098-1100, 2008

[12] R. Vetury, N. Q. Zhang, S. Keller and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE. Trans. Electron Devices*, vol. 48, no. 3, pp. 560-566, 2001

[13] W. S. Tan, P. A. Houston, P. J. Parbrook, G. Hill and R. J. Airey, “Comparison of different surface passivation dielectrics in AlGaN/GaN heterostructure field-effect transistors,” *J. of Physics D: Appl. Physics*, vol. 35, no. 7, pp. 595-598, 2002

[14] D. Guerra, M. Saraniti, D. K. Ferry, S. M. Goodnick and F. A. Marino, “Carrier Dynamics Investigation on Passivation Dielectric Constant and RF Performance of Millimeter-Wave Power GaN HEMTs,” *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3876-3884, Nov. 2011

[15] K. M. Chang, C. C. Cheng, C. C. Lang, “Electrical Properties of SiN/GaN MIS Diodes formed by ECR-CVD,” *Solid State Electronics*, vol. 46, no. 9, pp. 1399-1403, Sep. 2002

[16] C. Ye, Z. Ning, M. Shen, S. Cheng, Z. Gan, “Microstructure and dielectric properties of silicon nitride films deposited by electron cyclotron resonance plasma chemical vapor deposition,” *J. Appl. Physics*, vol. 83, no. 11, pp. 5978, 1998

[17] Y. Pei, S. Rajan, M. Higashiwaki, Z. Chen, S. P. DenBaars and U. K. Mishra, “Effect of Dielectric Thickness on Power Performance of AlGaN/GaN HEMTs,” *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 313-315, April 2009

[18] W. S. Tan, M. J. Uren, P. A. Houston, R. T. Green, R. S. Balmer and T. Martin, “Surface Leakage Currents in SiNx Passivated AlGaN/GaN HFETs,” *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 1-3, 2006

[19] J. Kotani, M. Tajima, S. Kasai and T Hashizume, "Mechanism of surface conduction in the vicinity of Schottky gates on AlGaN/GaN heterostructures," *Appl. Physics Lett.*, vol. 91, no. 9, pp. 093501, 2007

[20] Y. Ohno, T. Nakao, S. Kishimoto, K. Maezawa and T. Mizutani, "Effects of surface passivation on breakdown of AlGaN/GaN high-electron-mobility transistors," *Appl. Physics Lett.*, vol. 84, pp. 2184, 2004

[21] G. Xie, E. Xu, B. Zhang, W. T. Ng, "Study of the breakdown failure mechanisms for power AlGaN/GaN HEMTs implemented using a RF compatible process," *Microelectronics Reliability*, vol. 52, no. 6, June 2012

[22] M. A. Khan, X. Hu, G. Sumin, A. Lunev, J. Yang, R. Gaska and M. S. Shur, "AlGaN/GaN Metal Oxide Semiconductor Heterostructure Field Effect Transistor," *IEEE Electron Device Lett.*, vol. 21, no. 2, pp. 63-65, 2000

[23] P. D. Ye et al., "GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al_2O_3 as gate dielectric," *Appl. Physics Lett.*, vol. 86, pp. 063501, 2005

[24] Y. Z. Yue, Y. Hao, Q. Feng, J. C. Zhang, X. H. Ma and J. Y. Ni, "GaN MOS-HEMT Using Ultra-Thin Al_2O_3 Dielectric Grown by Atomic Layer Deposition," *Chinese Physics Lett.*, vol. 24, no. 8, pp. 2419, 2007

[25] B. Lee, C. Kirkpatrick, Y. Choi, X. Yang, Y. Wang, X. Yang, A. Huang, and V. Misra, "Impact of ALD Gate Dielectrics (SiO_2, HfO_2, and SiO_2/HAH) on Device Electrical Characteristics and Reliability of AlGaN/GaN MOSHFET Devices," *ECS Trans.*, vol. 41, no. 3, pp. 445-450, 2011

[26] C. Kirkpatrick, B. Lee, X. Yang and V. Misra, "Performance improvement of AlGaN/GaN high electron mobility transistors with atomic layer deposition (ALD) of SiO_2 and HfAlO dielectrics," p*hysica status solidi (c)*, vol. 8, no. 7-8, pp. 2445-2447, July 2011

[27] M. Kanamura, T. Kikkawa, T. Iwai, K. Imanishi, T. Kubo and K. Joshin, "An over 100 W n-GaN/n-AlGaN/GaN MIS-HEMT power amplifier for wireless base station

applications," *IEEE Int. Electron Devices Meeting Tech. Dig.*, Washington, DC, pp. 572-575, Dec. 2005

[28] T. Oka and T. Nozawa, "AlGaN/GaN Recessed MIS-Gate HFET With High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 668-670, July 2008

[29] K. J. Chen and C. Zhou, "Enhancement-mode AlGaN/GaN HEMT and MIS-HEMT technology," *physica status solidi (a)*, vol. 208, pp. 434-438, 2010

[30] O. Hilt, F. Brunner, E. Cho, A. Knauer, E. Bahat-Treidel, and J. Wurfl, "Normally-off high-voltage p-GaN gate GaN HFET with carbon-doped buffer," *Proc. of 23rd Int. Symp. Power Semiconductor Devices & IC's*, San Diego, CA, pp. 239-242, May 2011

[31] B. Lee; C. Kirkpatrick, X. Yang, S. Jayanti, R. Suri, J. Roberts and V. Misra, "Normally-off AlGaN/GaN-on-Si MOSHFETs with TaN floating gates and ALD SiO_2 tunnel dielectrics," *IEEE Int. Electron Devices Meeting Tech. Dig.*, San Francisco, CA, pp. 20.6.1-20.6.4, 6-8 Dec. 2010

[32] K. Ota, K. Endo, Y. Okamoto, Y. Ando, H. Miyamoto, H. Shimawaki, "A normally-off GaN FET with high threshold voltage uniformity using a novel piezo neutralization technique," *IEEE Int. Electron Devices Meeting Tech. Dig.*, Baltimore, MD, pp. 1-4, 7-9 Dec. 2009

[33] P. Parikh, Y. Wu and L. Shen. (2013). *Commercialization of High 600 V GaN-on-Silicon Power Devices* [Online]. Available. http://www.transphormusa.com/sites/default/files/transphorm/news/ISCRM_Sep2013_Parikh_TransphormInvited_0.pdf

[34] M. A. Briere. (2013). *The Status of GaN-on-Si based Power Device Development at International Rectifier* [Online]. Available. http://www.irf.com/product-info/ganpowir/ganapec.pdf

[35] W. Saito et al., "Field-Plate Structure Dependence of Current Collapse Phenomena in High-Voltage GaN-HEMTs," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 659-661, July 2010

[36] F. Gao et al., “Impact of Moisture and Fluorocarbon Passivation on the Current Collapse of AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1378-1380, Oct. 2012

[37] A. Koudymov, V. Adivarahan, J. Yang, G. Simin, M. A. Khan, “Mechanism of current collapse removal in field-plated nitride HFETs,” *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 704-706, Oct. 2005

[38] R. Suri, “Investigation of MOS Interfaces with Atomic-Layer-Deposited High-k Gate Dielectrics on III-V Semiconductors,” Ph.D. dissertation, Dept. Elect. Eng., North Carolina State Univ., Raleigh, NC, pp. 28-31, 2010.

[39] I. P. Smorchkova et al., “AlN/GaN and (Al,Ga)N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy,” *J. Appl. Physics*, vol. 90, pp. 5196, 2001

[40] R. Tulek et al., “Comparison of the transport properties of high quality AlGaN/AlN/GaN and AlInN/AlN/GaN two-dimensional electron gas heterostructures,” *J. Appl. Physics*, vol. 105, pp. 013707, 2009

[41] P. Ivo et al., “Influence of GaN cap on robustness of AlGaN/GaN HEMTs,” *IEEE Int. Reliability Physics Symp.*, pp. 71-75, Montreal, QC, Canada, 26-30 April 2009

[42] S. Arulkumaran et al., “Studies on the Influences of i-GaN, n-GaN, p-GaN and InGaN Cap Layers in AlGaN/GaN High-Electron-Mobility Transistors Oxidation and the origin of the two-dimensional electron gas in AlGaN/GaN heterostructures,” *Japanese J. Appl. Physics*, vol. 44, pp. 2953, 2005

[43] B. Lee, “A Study of Group III Elements (La, Gd, Eu, and Al) Incorporation on Metal Gate/High-k Stacks for Advanced CMOS Applications,” Ph.D. dissertation, North Carolina State Univ., Raleigh, NC, 2010

[44] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo and Y. Sano, “Surface passivation effects on AlGaN/GaN high-electron-mobility transistors with SiO_2, Si_3N_4, and silicon oxynitride,” *Appl. Physics Lett.*, vol. 84, no. 4, pp. 613, 2004

[45] C. Liu, E. F. Chor and L. S. Tan, "Enhanced device performance of AlGaN/GaN HEMTs using HfO2 high-k dielectric for surface passivation and gate oxide," *Semiconductor Sci. and Technology*, vol. 22, no. 5, pp. 522, 2007

[46] X. Wang et al., "Atomic layer deposition of Sc_2O_3 for passivating AlGaN/GaN high electron mobility transistor devices," *Appl. Physics Lett.*, vol. 101, pp. 232109, 2012.

[47] N. Ramanan, B. Lee, C. Kirkpatrick, R. Suri and V. Misra, "Properties of atomic layer deposited dielectrics for AlGaN/GaN device passivation," *Semiconductor Sci. and Technology*, vol. 28, no. 7, pp. 074004, 2013

[48] X-H. Ma et al., "Quantitative characterization of interface traps in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by dynamic capacitance dispersion technique," *Appl. Physics Lett.*, vol. 103, pp. 033510, 2013

[49] X. Sun et al., "Study of gate oxide traps in HfO_2/AlGaN/GaN metal-oxide-semiconductor high electron-mobility transistors by use of ac transconductance method," *Appl. Physics Lett.*, vol. 102, pp. 103504, 2013

[50] Y. Hori, Z. Yatabe and T. Hashizume, "Characterization of interface states in Al_2O_3/AlGaN/GaN structures for improved performance of high-electron-mobility transistors," *J. Appl. Physics*, vol. 114, no. 24, pp. 244503, 2013

[51] P. Kordos, R. Stoklas, D. Gregusova, S. Gazi and J. Novak, "Trapping effects in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistor investigated by temperature dependent conductance measurements," *Appl. Physics Lett.*, vol. 96, pp. 013505, 2010

[52] S. Yang et al., "Mapping of Interface Traps in High-Performance Al_2O_3/AlGaN/GaN MIS-Heterostructures Using Frequency- and Temperature-Dependent C-V Techniques," *IEEE Int. Electron Devices Meeting Tech. Dig.*, Washington, DC, pp. 6.3.1-6.3.4, 9-11 Dec. 2013

[53] B. S. Eller, J. Yang and R. J. Nemanich, "Electronic surface and dielectric interface states on GaN and AlGaN," *J. Vacuum Sci. Technol. A*, vol. 31, no. 5, pp. 050807, 2013

[54] E. H. Nicollian and J. R. Brews, "Extraction of Interface Trap Properties from the Conductance," in *MOS(Metal Oxide Semiconductor) Physics and Technology*, New Jersey: Wiley, 2003, ch. 5, pp. 176-231

[55] R. E. Herbert, Y. Hwang and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces," *J. Appl. Physics*, vol. 108, pp. 124101, 2010

[56] C. M. Jackson et al., "Interface trap characterization of atomic layer deposition Al_2O_3/GaN metal-insulator-semiconductor capacitors using optically and thermally based deep level spectroscopies," *J. Appl. Physics*, vol. 113, pp. 204505, 2013

[57] T. E. Cook, "Photoemission investigation of the electronic properties of Ga-face GaN(0001)-dielectric interfaces," Ph.D. dissertation, North Carolina State Univ., Raleigh, NC, 2003

[58] J. A. Cooper, Jr., and R. J. Schwartz, "Electrical characteristics of the SiO_2-Si interface near midgap and in weak inversion," *Solid State Electronics*, vol. 17, pp. 641-654, 1974

[59] H. Deuling, E. Klausmann and A. Goetzberger, "Interface states in Si-SiO_2 interfaces," *Solid State Electronics*, vol. 15, pp. 559-571, 1972

[60] D. K. Schroder, "Oxide and interface trapped charges, oxide thickness," in *Semiconductor Material and Device Characterization*, New Jersey: Wiley, 2006, ch. 6, pp. 327

[61] Y. Cai, Y. Zhou, K. M. Lau and K. J. Chen, "Control of Threshold Voltage of AlGaN/GaN HEMTs by Fluoride-Based Plasma Treatment:From Depletion Mode to Enhancement Mode," *IEEE. Trans. Electron Devices*, vol. 53, no. 9, 2006

[62] J. M. Tirado, J. L. Sanchez-Rojas and J. I. Izpura, "Trapping Effects in the Transient Response of AlGaN/GaN HEMT Devices," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 410-417, April 2007

[63] O. Mitrofanov and M. Manfra, "Mechanisms of gate-lag in GaN/AlGaN/GaN high electron mobility transistors," *Superlattices and Microstructures*, vol. 34, no. 1-2, pp. 33-53, 2003

[64] B. Gila et al., “Oxide Dielectrics for Reliable Passivation of AlGaN/GaN HEMTs and Insulated Gates,” *ECS Trans.*, vol. 3, no. 5, pp. 141-150, 2006

[65] C. Zhang, Y. Hao and Q. Feng, "Effective surface passivation of AlGaN/GaN heterostructures by using PH_3 plasma treatment and HfO_2 dielectric,” *physica status solidi (c)*, vol. 9, no. 3-4, pp. 934-937, 2012

[66] W. S. Tan, P. A. Houston, P. J. Parbrook, G. Hill and R. J. Airey, “Comparison of different surface passivation dielectrics in AlGaN/GaN heterostructure field-effect transistors,” *J. Physics D: Appl. Physics*, vol. 35, pp. 595-598, 2002

[67] D. Hiller et al., “Low temperature silicon dioxide by thermal atomic layer deposition: Investigation of material properties,” *J. Appl. Physics*, vol. 107, pp. 064314, 2010

[68] G. Koley and M. G. Spencer, “On the origin of the two-dimensional electron gas at the AlGaN/GaN heterostructure interface,” *Appl. Physics Lett.*, vol. 86, pp. 042107, 2005

[69] O. Mitrofanov and M. Manfra, “Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors,” *J. Appl. Physics*, vol. 95, pp. 6414, 2004

[70] J. M. Tirado, J. L. Sanchez-Rojas and J. I Izpura, “Simulation of surface state effects in the transient response of AlGaN/GaN HEMT and GaN MESFET devices,” *Semiconductor Sci. and Technology*, vol. 21, pp. 1150-1159, 2006

[71] M. Faqir, G. Verzellesi, G. Meneghesso, E. Zanoni and F. Fantini, “Investigation of High-Electric-Field Degradation Effects in AlGaN/GaN HEMTs,” *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1592, 2008

[72] G. Koley, V. Tilak and L.F. Eastman, “Slow transients observed in AlGaN/GaN HFETs: Effects of SiNx passivation and UV illumination,” *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 886, 2003

[73] *Sentaurus Device User Guide*, Version C-2009.06, Synopsys Inc., Mountain View, CA, June 2009, pp. 195

[74] N. F. Mott and E. A. Davis, “Theory of Electrons in a Non-Crystalline Medium,” in *Electronic Process in Non-Crystalline Materials*, 2nd edition, New York, CA: Oxford University Press, 1979, pp. 32

[75] W. Vollman, "Poole-Frenkel Conduction in Insulators of Large Impurity Densities," *physica status solidi (a)*, vol. 22, no. 1, pp. 195, 1974

[76] N. Ramanan, B. Lee and V. Misra, "Device Modeling for Understanding AlGaN/GaN HEMT Gate-Lag," *IEEE Trans. Electron Devices*, vol. 61, no. 6, June 2014

[77] H.-J. Fitting and J.-U. Frieman, "Monte-Carlo Studies of the Electron Mobility in SiO_2," *physica status solidi (a)*, vol. 69, pp. 349, 1982

[78] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi and E. Zanon, "Current Collapse and High-Electric-Field Reliability of Unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, 2001

[79] F. Li-Hua, L. Hai, C. Dun-Jun, Z. Rong, Z. You-Dou, W. Ke and L. Xin-Yu, "High-field-induced electron detrapping in an AlGaN/GaN high electron mobility transistor," *Chinese Physics B*, vol. 21, no. 10, pp. 108503, 2012

[80] G. Meneghesso, M. Meneghini, D. Bisi, I. Rossetto, A. Cester, U. K. Mishra and E. Zanoni, "Trapping phenomena in AlGaN/GaN HEMTs: a study based on pulsed and transient measurements," *Semiconductor Sci. and Technology*, vol. 28, pp. 074021, 2013

[81] T. Mizutani, A. Kawano, S. Kishimoto and K. Maeazawa, "Drain current DLTS of normally-off AlGaN/GaN HEMTs," *physica status solidi (c)*, vol. 4, no. 4, pp. 1536-1539, 2007

[82] I. Omura, W. Saito, T. Domon and K. Tsuda, "Gallium Nitride Power HEMT for High Switching Frequency Power Electronics," in *Int. Workshop on Physics of Semiconductor Devices*, pp. 781-786, 16-20 Dec. 2007

[83] S. Karmalkar, M. S. Shur and R. Gaska, "GaN-Based Power High Electron Mobility Transistors," in *Wide Energy Bandgap Electronic Devices*, Singapore: World Scientific, 2003, ch. 3, sec. 1.1, pp. 177

[84] M. Ieda, G. Sawa and S. Kato, "A Consideration of Poole-Frenkel Effect on Electric Conduction in Insulators," *J. Appl. Physics*, vol. 42, no. 10, pp. 3737, 1971

[85] N. Golego, S. A. Studenikin and M. Cocivera, "Properties of Dielectric $BaTiO_3$ Thin Films Prepared by Spray Pyrolysis", Chemistry of Materials, vol. 10, pp. 2000-2005, 1998

[86] I. Yucedag, S. Altindal and A. Tataroglu, "On the profile of frequency dependent series resistance and dielectric constant in MIS structure," *Microelectronic Engineering*, vol. 84, no. 1, pp. 180–186, 2007

[87] S. P. Murarka, "Dielectric Properties," in *Interlayer Dielectrics for Semiconductor Technologies*, San Diego, CA: Academic Press, 2003, pp. 15

[88] J. Si, J. Wei, W. Chen and B. Zhang, "Electric Field Distribution Around Drain-Side Gate Edge in AlGaN/GaN HEMTs: Analytical Approach," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3223, 2013

[89] Rik Jos, "A semi-analytical, two-dimensional model for AlGaN/GaN high-electron-mobility-transistor Schottky currents at high reverse voltages," *J. Appl. Physics*, vol. 114, pp. 074512, 2013

[90] L. Yuan et al., "On the Operation Mechanism and Device Modeling of AlGaN/GaN High Electron Mobility Transistors (HEMTs)," *World Academy of Science, Engineering and Technology*, vol. 69, pp. 127-130, 2012

[91] D. Marcon et al., "Reliability Analysis of Permanent Degradations on AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3132-3141, 2013

[92] M. D. Hodge, E. R. Heller, R. Vetury, J. B. Shealy, "Analysis of Time Dependent Electric Field Degradation in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3145-3151, 2014