ABSTRACT

CHARLES, GARY. Design, Model and Analysis of TSV-based On-Chip PDN Interconnects for 3-D Integrated Circuits. (Under the direction of Professor Paul D. Franzon.).

In traditional design of power delivery networks (PDNs), the impedance property of the network is required to be less than the target impedance across a broad range of frequencies to ensure IR-drop is minimized and simultaneous switching noise (SSN) is suppressed. It is becoming increasingly more challenging to meet the electrical constraints and performance of modern integrated circuit (IC) design using conventional interconnect technology. However, three-dimensional (3-D) stacking using through-silicon via (TSV) technology has emerged as a viable solution to reduce interconnect delay, power supply noise and achieve heterogeneous IC module integration. A major advantage to using TSVs is the shortened interconnect path to pass data signals and deliver clean power at a fast rate between chips. A low impedance return path in the PDN guarantees negligible interference or noise into other sensitive timing and signaling circuits (e.g. signal generation circuits and PLLs). In an effort to keep up with scaling technology and robust PDN designs, TSV technology is a promising option relative to the other interconnect options available today.

The research outlined in this dissertation focuses on the development, modeling and analysis of TSV-based PDN using on-chip decoupling capacitors. A combination of CAD simulation tools and analytical formulas was used to create the TSV-based PDN models and estimate its impedance property. The work outlined here focuses on a multi-tier chip-stacking case-study. The case study is formulated around the effect different chip stacking topology has on the impedance property of TSV-based PDNs. The 3 distinct chip stacking topologies are listed as follows: (1) face-to-face (F2F); (2) face-to-back (F2B) and (3) back-to-back (B2B) chip stacking topologies. Quantitatively speaking, the study compared the impedance noise level between three stacking topologies and found the impedance noise of F2F chip stacking to be relatively lower than F2B and B2B. Among the power grid structure and power/ground TSV pair models presented in this research work, we also present and implement a metal-insulator-metal (MIM) capacitor model written as a complex impedance equation. Based on the physical dimensions of the MIM capacitor, we estimated the capacitance density (per unit area) range from 0.062 $fF/\mu m^2$ to 5.325 $fF/\mu m^2$. We also

modeled metal-oxide semiconductor (MOS) capacitors in this work. Conclusively, the research provides a modeling framework to design TSV-based PDNs with the intent of minimizing on-chip inductance. Overall, the goal is to advance the state-of-the-art in 3-D IC TSV-based PDN design.

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Design, Model and Analysis of TSV-based On-Chip PDN Interconnects for 3-D Integrated Circuits

by
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DEDICATION

I dedicate my dissertation to my family.

My mother Annalia "Maya" Charles most amazing woman in my life; love you always for your strength, wisdom, humility and grit.

To my older siblings,

Jocelyn, Dieune, Nicole, Armand and Abraham,

and my younger siblings,

Diana and Gertrude.

Without your love, support, prayers and encouragement none of this would be possible.

BIOGRAPHY

Gary Charles was born in Miami, Florida to Haitian parents Dicelien Simeon and Annalia Charles. He grew-up attending primary school in the heart of the city downtown Miami. As a young teenager, he was accepted into an engineering magnet program called Florida Action for Minorities in Engineering (FL.A.M.E). He was exposed to an array of college engineering courses as a high school senior which afforded him an early exposure to university life. After receiving his high school diploma, Gary attended Florida International University for his undergraduate studies and received a Bachelor's of Science in Electrical Engineering. Immediately after receiving his B.S., Gary was accepted into the Electrical and Computer Engineering Master of Science program at North Carolina State University located in downtown Raleigh, North Carolina. He successfully completed his M.S. in Electrical Engineering and continued at North Carolina State for the doctoral program. Gary is a member of the Microelectronics Systems Laboratory (MSL) group where his research interest focused on the design, model and characterization of power delivery systems, on-chip interconnect structures and 3-D IC architecture.

Gary participated in several internships and co-op opportunities with companies ranging from Intel Corporation, Cisco Systems to International Business Machines (IBM). The work-experiences afforded Gary the opportunity to work with industry experts and leaders in various areas that includes signal integrity (at Cisco), power integrity (at Intel) and electromagnetic compatibility (EMC) (at IBM). Gary received several awards while in the doctoral program at North Carolina State. He was awarded the National Consortium for Graduate Degrees for Minorities in Engineering and Science (GEM) Ph.D. fellowship, Intel Scholar award, diversity enhancement grant and doctoral dissertation completion grant. Gary served as a reviewer for IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT), has submitted and presented at several conferences and has served on several graduate panel discussions throughout his tenure as a graduate student at North Carolina State University.

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Gary Charles
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Raleigh, North Carolina, USA

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TERMS AND ABBREVIATIONS

3D: Three-Dimensional.

2D: Two-Dimensional.

IR drop: Voltage drop caused by resistance of the circuit due to current load.

Ldi/dt noise: Noise caused by inductance of the circuit due to switching of load.

TSV: Through-Silicon-Via.

I/O: Input/Output.

GHz: Gigahertz.

PDN: Power Distribution Network.

IC: Integrated Circuit.

PCB: Printed Circuit Board.

P/G: Power/Ground.

ITRS: International Technology Road Map for Semiconductors.

CMOS: Complementary Metal Oxide Semiconductor.

D2D: Die-to-Die.

KGD: Known Good Dies.

D2W: Die-to-Wafer.

W2W: Wafer-to-Wafer.

F2B: Face-to-Back.

B2B: Back-to-Back.

F2F: Face-to-Face.

FEOL: Front End of Line.

BEOL: Back End of Line.

LC: Inductance, and Capacitance.

RLC: Resistance, Inductance, and Capacitance.

ESR: Effective Series Resistance.

ESL: Effective Series Inductance.

CHAPTER I

Introduction

1.1 Motivation and Overview

A limiting performance factor in high-speed integrated circuits (ICs) is power delivery noise found throughout the power supply chain ecosystem (e.g. board + package + on-chip). With billions of transistors demanding large amounts of instantaneous switching currents all at one time, a significant amount of simultaneous switching noise (SSN) at the package and on-chip-levels are generated. SSN has become a significant source of timing jitter and skew problems at the high-speed serial I/O lanes and clock distribution lines. To make matters more cumbersome, increase demand for more functionality, smaller form factor, higher bandwidth and lower power features have presented incredible challenges for IC designers, signal and power integrity engineers.

Already faced with multiple challenges, the semiconductor industry has to combat the on-chip interconnects and wire scaling problems. As transistor devices maintain scaling technology trends, interconnect wires have difficulty keeping up. Wire scaling technology has become another critical factor of IC performance because of the parasitic capacitance accounting for 50% of the chip power consumption and the effects of RC (resistance/capacitance) delay affecting CMOS gate timings [1.1]. A large percentage of RC delay is influenced by wire resistance. Buffers (repeaters) are typically used to reduce propagation delay. However, while the insertion of buffers has certain advantages, it also leads to increased area and power dissipation thus affecting the overall system performance.

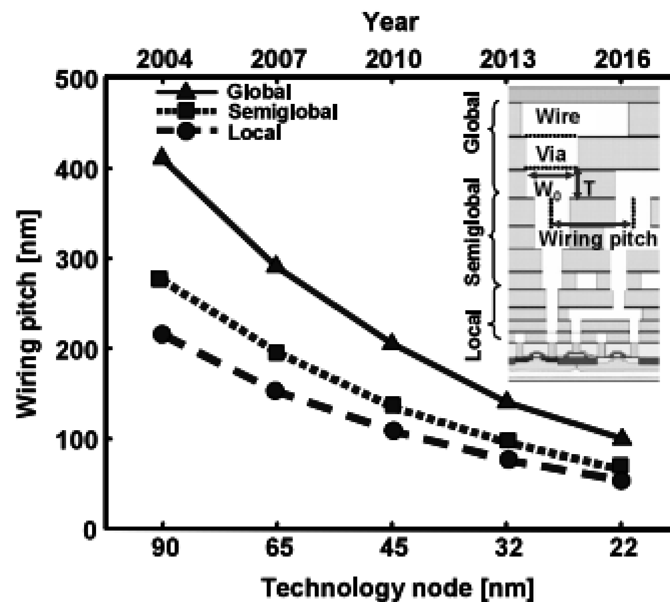


Fig. 1. A trend of on-chip interconnect [1.2].

Fig. (1): show three on-chip interconnect curves classifying local, semi-global and global wire lines for deep sub-micron VLSI (Very Large Scale Integration) designs [1.2]. The wire interconnect and power supply noise issues can be addressed together using an emerging wire interconnect methodology known as through silicon via (TSV) technology. TSV technology has emerged as a viable response to the physical interconnects limitations and performance bottlenecks affecting modern system-on-chip (SoC) designs. More specifically, TSVs can also improve the power consumption, power supply noise and dissipation problems that exist in today's package and on-chip designs. The semiconductor industry has already begun using TSV structures for stacking memory-on-memory and are investigating methods of stacking memory-on-logic [1.3]-[1.6]. The semiconductor industry has identified several key benefits to using TSVs which are listed as follows: (1) increased bandwidth performance, (2) more functionality, (3) smaller form factor or improved miniaturization, (4) lower power consumption and (5) finally low cost [1.7]. These key advantages allow the semiconductor industry the capability of extending Gordon Moore's Law and to strive for the highest achievable performance gains. The contributions of this study are focused on

modeling TSV-based power delivery networks (PDNs), estimating and suppressing impedance noise while achieving minimal power supply noise. Moreover, the study investigates the effects of various on-chip stacking orientations and the implementation of on-chip decoupling capacitor models (e.g. metal-insulator-metal (MIM) capacitors) into the TSV-based PDN.

In order to facilitate a relatively smooth transition to TSV-based 3-D ICs, it is important for industry experts as well as academia researchers to develop a standard for 3-D IC design. The focus of the standardization of 3-D IC should be placed on CAD or electronic design automation (EDA) development for thermal and power delivery modeling and analysis. Several universities such as North Carolina State University, UCLA, University of Minnesota and Georgia Tech are a few of the recognized universities involved in this initiative. It is apparent that 3-D integration using TSV technology will be an inflection point in the semiconductor industry for extending Gordon Moore's law. 3-D integration enables the reduction of power and increase bandwidth for several technological areas. TSVs require a multi-physics modeling approach that will aid in the understanding of the electrical and electromagnetic properties of the TSV. In this thesis, the power delivery challenges and proposed ideas for modeling, design and analysis of TSV-based PDN systems are discussed.

1.2 Power Delivery Challenges in 3-D IC

One of the advantages of 3D IC technology is that with smaller footprint dimensions more circuitry can be packed into a small area. Albeit, this also means that supply current increases significantly resulting in high current density with hundreds of amperes of current passing through a limited footprint. Table 1.1 shows with each technology node the max thermal design power trend for Intel microprocessor in a two-dimensional (2-D) design:

Table 1.1 Intel Microprocessor Trends of last decade [1.8].

YEAR	CPU Generation	Process	# of FETs	Clock (Hz)	Max. TDP
1993	Pentium	0.8μm	3.1 million	66M	8W
1995	Pentium Pro	0.6μm	5.5 million	200M	15.5W
1997	Pentium II	0.35μm	7.5 million	300M	43W
1999	Pentium III	0.25μm	9.5 million	600M	42.8W
2000	Pentium IV	0.18μm	42 million	2G	71.8W
2005	Pentium D	90nm	230 million	3.2G	130W
2007	Core 2 Duo	65nm	410 million	2.33G	65W
2008	Core 2 Quad	45nm	820 million	2.83G	95W
2010	Six-Core Core i7-970	32nm	1170 million	3.2G	130W
2011	10-Core Xeon	32nm	2600 million	2.4G	130W
2012	Ivy Bridge Core i5-3570 (Tri-gate FETs)	22nm	4310 million	3.4G	155W

Given the max thermal design power (TDP) for 2-D design, industry experts have estimated higher TDP requirements for TSV-based 3-D ICs [1.9]. The ITRS prediction for 3D integration technology shows the latest design challenges it faces in the coming years in Table 1.2:

Table 1.2 shows a design challenge roadmap for 3-D integration technology [1.9].

Year	2011-2013	2013-2017	2017-2020
3D Technology	Homogenous stack of silicon using interposers	Tight integration of memory and logic	Heterogeneous 3D, monolithic 3D IC.
Product	DRAM stack with high yield and small size	Mobile memory-on-logic with significant power saving and bandwidth enhancement	Highly integrated and optimized system with no memory wall and cost issues.
Design Challenges	Power integrity using TSVs, Heat removal, stress caused by TSVs, standards and formats for chip-package co-design for thermal and power integrity, cost and yield.	-Power integrity and IR drop with TSVs to 10mV accuracy. -Thermal, stress and switching noise driven transients	-More than 100A current delivery with 10mV accuracy. - Complex tradeoffs for heterogeneous system of more than ten dies.

With on-chip power delivery, there are different types of interconnects associated with back-end-of-line (BEOL). With TSV integrated into BEOL on-chip power distribution design, the PDN design becomes a lot more stringent. The inductance of on-chip power grids increases

significantly. With the increase of inductance coupled with transistors switching on and off very fast result in large ground bounce effects. The simultaneous switching of I/O drivers causes fluctuation in the voltage level power lines. The interconnect space for 3-D IC is extremely critical and must be managed and understood to ensure that power delivery challenges are not exacerbated. The roadmap interconnects are shown in Table 1.3 and 1.4.

Table 1.3 Emerging Global Interconnect Level Roadmap for TSVs [1.9]

Global Level	2011-2014	2015-2018
Min. Height (µm)	20-50	20-50
Min. Diameter (µm)	4-8	2-4
Min. Pitch (µm)	8-16	4-8
Max. Aspect Ratio (AR) (height/diameter)	5:1-10:1	10:1-20:1
No. of Dies/Stack	2-5	2-8

Table 1.4 Emerging Intermediate Interconnect Level Roadmap for TSVs [1.9]

Global Level	2011-2014	2015-2018
Min. Height (µm)	6-10	6-10
Min. Diameter (µm)	1-2	0.8-1.5
Min. Pitch (µm)	2-4	1.6-3
Max. Aspect Ratio (AR) (height/diameter)	5:1-10:1	10:1-20:1
No. of Dies/Stack	2-5	8-16

1.3 Research Objectives

The objective of this research is to investigate and understand the behavior of the voltage supply system for three-dimensional (3-D) stack of dies. Power integrity, at least at the on-chip level, is dictated by the resistive and inductive properties of the network. The IR-drop (resistive) and Ldi/ dt (inductive) noise are critical issues that can cause the power integrity for 3-D ICs to be more complex than 2-D ICs. Therefore, the resistive and inductive interconnect contributions should be accurately understood.

The on-chip interconnects in 3-D PDN which includes power-grids (BEOL), TSVs, micro-bumps, I/O pads all contribute additional resistance and inductance that generate noise that will propagate to I/O drivers and internal switching logic circuits while carrying high frequency noise content. The fast switching events of the core logic and I/O drivers will cause the voltage to fluctuate. This fluctuation on the voltage lines is known as simultaneous switching noise (SSN) effects and SSN is much more severe for 3-D stacked power distribution networks than 2-D. The output impedance property of the power delivery network corresponds to SSN and is a helpful way to assess the severity of the SSN found in the power supply system. Typically, the output impedance of the power distribution network should be well below the target impedance within the operating frequency range in order to ensure the power integrity of the system. It is critical to manage the output impedance to a minimum level since it reflects SSN. To control the output impedance of 3-D stack PDNs, each individual tier-level containing on-chip interconnects must be accurately modeled.

In this research, we study the physical sizing of on-chip interconnects and its impact on the output impedance. We also investigate and show how different stacking orientations can alter the impedance characteristics assuming a homogenous topology for each individual die. The different die stacking orientation can be arranged as Face-to-Back (F2B), Face-to-Face (F2F) and Back-to-Back (B2B). The simulation model used here combines EM simulation methods for piece-wise PDN models and segmentation method to reconstruct unit size PDN models and estimate the overall impedance properties. The segmentation method

makes it possible to combine the on-chip decoupling capacitor models (e.g. metal-insulator-metal (MIM) caps) into the 3-D PDN design. There are several different on-chip decoupling capacitor models we discuss in this thesis, however, MIM and metal-oxide-semiconductor (MOS) caps were implemented in this work. Optimum budgeting of on-chip decoupling capacitance is necessary because of the limited area footprint that exists with 3-D IC. Decoupling capacitance has been known to consume chip real estate particularly MOS capacitors. Therefore, careful tradeoff between decoupling capacitors for processor versus memory (DRAM dies) should be handled with meticulous consideration and solid design practices.

This dissertation work investigates issue(s) surrounding TSV-based 3-D stacked power delivery design. We perform a parametric study to understand how adjusting the physical dimensions can affect the resistive and inductive properties. Different stacking orientations of TSV-based PDN models are proposed to estimate the output impedance. A comparative study is performed between the different stacking orientations. We discuss the implementation of on-chip decoupling capacitors and its ability to reduce resonant spikes. The techniques used in this study to understand the power integrity challenges of TSV-based 3-D IC PDN design and research results are adequately discussed.

1.4 Overview of Dissertation Chapters

In this section, a brief summary of each chapter is presented to capture a description of the topic relating to the research problem and how it was undertaken.

Chapter 2:

The state of the art in 3-D IC technology is presented in this chapter along with an account of the other types of bonding approaches used in today's microelectronic design. We briefly discuss the electromagnetics of interconnects and show analytical formula representing each parasitic element. A review and detail comparison of wire-bonding, solder bump (flip-chip applications) and TSV interconnect methodologies is discussed. We briefly discuss the different types of interconnect levels in back-end-of-line (BEOL). We talk about the collective impact of TSVs from the perspective of noise coupling to cross-talk affects. We outline the pros and cons associated with its performance and scalability. There are a myriad of TSV circuit element models, physical scalable models and analytical models also covered in this chapter as part of the literature review study.

Chapter 3:

A parametric study on certain on-chip interconnect is performed in this chapter. The effects of varying the physical geometries of the interconnect structures are studied for TSVs and the on-chip power grid. The other interconnects are not included in this study such as I/O pads and micro-bumps since the resistive and inductive properties are negligible relative to the other larger interconnect structures. Some of the physical parameters we look at include height, pitch, metal thickness, TSV oxide thickness just to name a few. A comprehensive table is put together to summarize how physical size of certain TSV parameters affect some electrical parasitics (e.g. *RLGC* circuit elements). Finally, in this chapter, we cover the analytical impedance models used to estimate the output impedance property of a generic PDN model and extend its use in solving the impedance of a TSV-based PDN system. We

present analytical models to explain the concept of the segmentation method. The segmentation concept can be applied to solving cavity and on-chip PDN models.

Chapter 4:

TSV-based PDN systems are constructed based on the different on-chip stacking orientations. We constructed three types of TSV-based PDN systems for a comparative study to assess the output impedance property of each orientation. The physical size of interconnects was based on the parametric study of the previous chapter. The goal here is to ensure that resistive and inductive characteristics from on-chip interconnects are kept to a minimal. The three different orientations are listed as follows: face-to-back, face-to-face and back-to-back. The comparative study determines, at least quantitatively, which stacking orientation has the lowest output impedance property with and without the implementation of on-chip decoupling capacitors. SPICE simulation results are included in this chapter for each stacking orientation as well.

Chapter 5:

Finally a summary of the research work and contributions are presented along with future directions and continued research on the subject matter is discussed in this chapter.

CHAPTER II

Interconnect Background and TSV Technology

2.1 Literature Review of On-Chip Interconnects for Power Delivery

Wire interconnects play a critical part in today's power and signal integrity arena. In earlier years of circuit design, the effects from wire interconnects were negligible because of relatively slow operating speeds and lower transistor count integrated inside a circuit package. Nowadays, the electromagnetics surrounding wire interconnects have changed tremendously. Signal and power integrity engineers cannot afford to ignore these effects as feature sizes of technology nodes shrink and clock frequencies creep into the Giga-hertz (GHz) regime with considerable ease [2.10]. The electrical adverse effects associated with wire interconnects include RC delays, timing jitter, cross-talk noise, transmission-line effects (ISI), IR-drop (resistive), SSN and voltage fluctuation (inductive). Consequently, wire interconnects present a bottleneck for increasing system speed, improving performance, reducing power and shrinking system size of electronic systems [2.11],[2.12].

The electromagnetic field components in a wire are perpendicular to each other and in the direction of the wave of propagation known as the Traverse Electro-Magnetic (TEM) mode waves shown in Fig. (2). All electromagnetic behaviors can be explained using four simple formulas developed by James Clerk Maxwell's (e.g. Maxwell's equations). For non-uniform geometries and structures, field solvers based on numerical techniques are employed to solve Maxwell's four fundamental equations. As a wire is excited by an electrical signal it will produce an electric field and magnetic field due to the potential difference and current

flow in a wire, respectively. The parasitic elements are shown in Fig. (2). Most general wire models are represented using capacitive, resistive, inductive and conductive circuit elements.

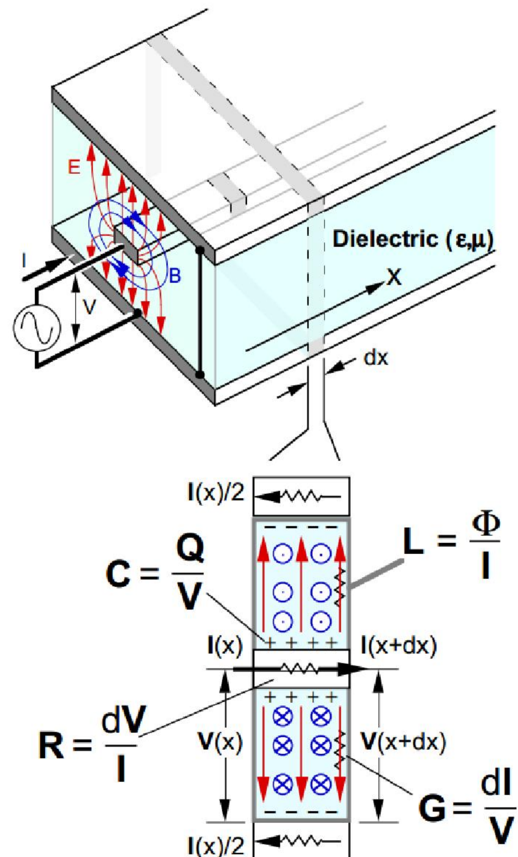


Fig. 2. Electromagnetic view of a wire [2.13]. If the current (*I*) and voltage (*V*) change at the drive point, the magnetic (*B*) and electric (*E*) change as well; disturbance propagates away from the drive point at the speed of light.

Fig. (3): shows an example of a rising trend of interconnect delay in metal-1 wire versus process technology node. The figure above demonstrates how propagation delay worsens as transistor sizing decreases over technology generations. For a long-term solution, a promising interconnect method that will potentially replace traditional wire interconnections is TSV technology. This opens up the possibilities for various interconnect alternatives. In

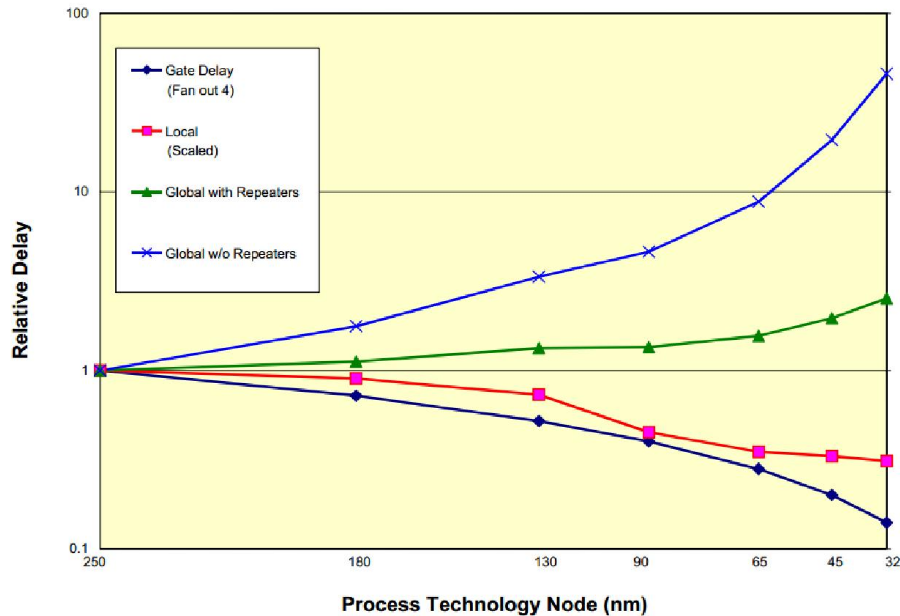


Fig. 3. Delay for metal-1 and global wiring versus feature size. From 180nm to 15nm, the delay of scaled wires increases by approximately 10ps while that of fixed length wires increases by approximately 2000ps. If these wires are modified with repeaters, the delays substantially reduces to roughly single digit (~ 3ps) for scaled wires and 40ps for fixed length wires [2.12].

today's electronic systems, the common wire interconnect solutions available that were developed for 2-D circuit design applications include: 1) wire-bonding technology, 2) flip-chip technology and adhesive bumps. 3-D integration, however, enables the possibility to not only use TSV technology but also a combination of the 2-D interconnect solutions. Wire-bonding and flip-chip technology remains the workhorse of the semiconductor industry and has been estimated to be packaged on 70% of electronic components [1.9]. However, from a power integrity point of view, these chip bonding options present electrical issues. For instance the loop inductance is directly proportional to the length of the wire-bond. The shorter the interconnect length, the lower the inductance. A lower power inductance in the power-ground path will decrease ground bounce and switching noise. Generally speaking, the wire-bond has approximately 1nH/mm or 25nH/inch [2.14]. If for instance, a wire-bond

is 50mils in length, it will have an inductance of 1.3nH. The interconnects interface primarily to the die is required to provide a low impedance path for the power distribution system so as to keep the switching noise within specification and controlled impedance for the signal leads to allow adequate signal integrity. Pak et al. conducted a study where wire-bonding was applied to a multi-stack chip design. Similarly, work was performed for a multi-

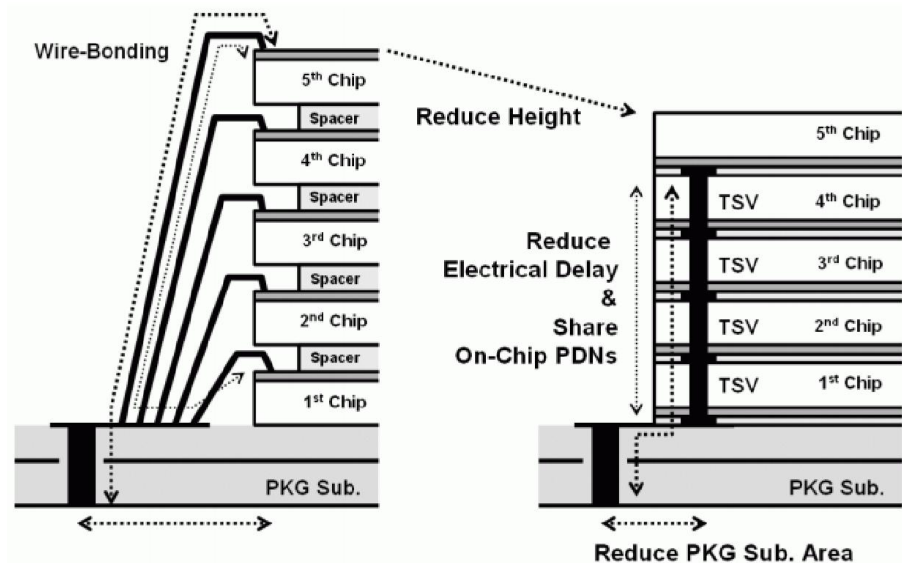


Fig. 4. Side-by-side comparison of wire-bond technology versus TSV technology [2.15].

stack TSV design. Pak compared both multi-stack designs which are illustrated in Fig. (4) side-by-side cross-sectional view. Pak et al. demonstrated through this work that TSVs provided more power integrity stability than wire-bonding or any other interconnection methods currently being used [2.15]. The loop inductance for wire-bonding is greater than TSV by a minimum of $\sqrt{2}$ term. Furthermore, wire-bonding needs extra vertical space between chips. Flip-chip (FC) technology is an alternative bonding approach to wire-bonding technology. Flip-chip provides lower switching noise than wire-bonding technology

due to lower lead inductance. The typically short length of the FC bonding means less power and ground inductance. Other advantages include higher pad count for power and ground pads and the potential to decrease the impedance of the power and ground distribution network. The primary motivation behind FC is the large input/ output (I/O) count which increases the signal bandwidth for a small die size area. Flip-chip technology utilizes solder bumps to carry large amounts of current for high speed clock applications. The solder bumps introduce negligible parasitic inductance and capacitance at its connections compared to conventional wire-bond connections [2.16]. The advantages of the solder bump interconnection technology over wire bonding technique are listed below [2.16]:

- Carry large currents with negligible parasitic inductance and capacitance and low resistance due to short solder bumps.
- Capable of achieving better reliability by reducing thermal stress by optimizing solder joint geometry, using underfilling and compliant substrate.
- Easy integration to multilayered structures
- Robust packaging

Table 2.1 summarizes the parasitic properties of solder bump and wire-bond interconnects. The values show a considerable decrease in parasitic values in solder bumps. The solder bumps are mounted face to face onto the interconnect substrate. This is usually viewed as flipped orientation, hence the name, flip chip.

Table 2.1 Summary of Electrical Properties for Wire Bond vs. Solder Bump

	mΩ/ inch	**nH/ inch**	**Length**	**Resistance**	**Inductance**
Wire Bond	1	25	50-100 mils	50-100 mΩ	1.2 - 2.5 nH
Solder Bump	0.08	18	3-6 mils	< 1mΩ	< 0.1 nH

The performance at high frequency applications makes solder bump a superior interconnect compared to the other forms of wire-bond because the connection path length is reduced. Although solder bump offers great benefit over other interconnects, there are disadvantages: These disadvantages are listed as follows: 1) difficult testing of bare dies, 2) limited availability of bumped chips, 3) low reliability for some substrates, 4) high assembly accuracy is required and 5) weak process compatibility with SMT. The evolution of the next generation interconnect technology is TSV for complex 2.5D and 3-D system integration design. TSVs have an advantage compared to other interconnect bonding approaches shown in Table 2.2. The academic research community and semiconductor industry are pushing for TSV interconnect as the choice for 3D integration applications.

Table 2.2 Comparison of TSVs and current interconnect options [2.17].

Technology	**Advantages**	**Disadvantages**
Wire-bonding	• Flexible Connections • High reliability • Mature processing • Cost effective	• Low density • Long thin wire • Large pad area • Poor signal integrity • Poor power integrity
Solder Bumps (FC)	• Short Length • Low resistance • More Connections	• Large solder balls • May short circuit with each other in the long run
Through Silicon vias (TSVs)	• Small height • Small footprint • High density • Low resistance	• Complex fabrication • Capacitive coupling to substrate, devices and TSVs in vicinity • Mechanical stresses to thin substrate and devices
Contactless i.e. inductive or capacitive coupling	• Small electric path length • Easy to fabricate	• Low reliability • Cross talk and coupling issues • Size of inductor for inductive coupling

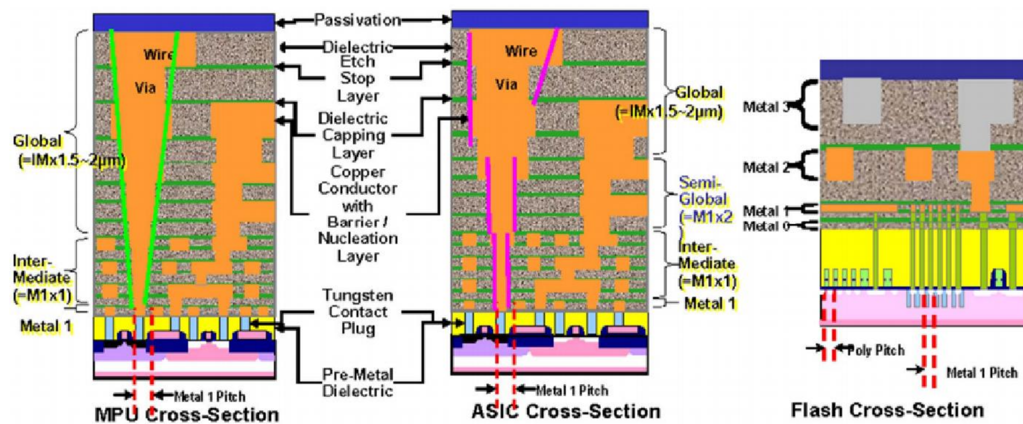


Fig. 5. BEOL Technology requirement for Logic (MPU/ASIC) and NAND flash memory [1.9]

Three-dimensional integration using TSV is one of the future IC packaging technologies that can eliminate copper wire between silicon chips by vertically stacking chips on top of each other. Through silicon vias with heights comparable to the substrate thickness, can pass through the substrate and can be placed anywhere in the chip thus offering additional I/O flexibility compared to copper wires which can only be placed along the peripheral area [2.18].

The back-end-of-line (BEOL) is a semiconductor process step often used to form metal interconnects and dielectric material. Fig. (5): shows BEOL interconnect level. The BEOL consists of three types of metal layers that include: 1) **Global interconnect** wiring provides the clock and signal distribution between functional blocks and also it distributes power-ground to the functional blocks, 2) **Intermediate Interconnect** wiring provides clock and signal information within functional blocks. Intermediate interconnects have wider traces and are taller than local interconnects to ensure the resistance path is as low as possible and 3) **Local interconnect** wiring are used to connect to transistor devices (front-end-of-line or FEOL) within a functional block. Local interconnect often occupy layers-1 and -2. BEOL interconnects are used for power and ground lines in the design of on-chip power distribution network design. The global interconnect metal layer is used to distribute the current across the die to local and intermediate interconnect metal layers. The power grid metal lines

should be designed to provide a low impedance path for the power current to pass through to prevent static IR drop and transient noise issues. There are several power grid structure types to choose from for on-chip power distribution network design. There are advantages and disadvantages associated with each configuration type. In this research, we used a grid structured power distribution network design. The grid PDN are commonly used in high complexity, high performance integrated circuits and also used in our study [2.19].

2.2 Background of TSV Technology

Through silicon via allow interconnection of multiple chips in a vertical direction. The fabrication process and design of TSVs vary significantly and are dependent on the target application. Fig. (6): illustrate a drawing of three different TSV structures consisting of substrate, electrical conductor and dielectric insulator to separate conductor from substrate.

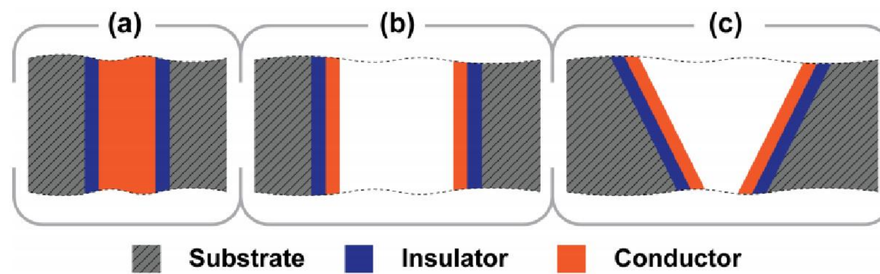


Fig. 6. Cross-section view of TSV designs. A) solid metal filled TSV, b) annular metal-lined TSV and c) TSV with tapered side wall [2.20].

The physical geometries of the TSV are important because they all influence the TSV's electrical characteristics (e.g. resistance, inductance, capacitance and conductance). The metal filling typically used in TSVs is Cu with a dielectric material of silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) to isolate the copper cylinder from the substrate material. The important physical parameters of a TSV are the TSV's height, diameter, aspect ratio, oxide layer thickness and pitch between other TSV structures.

The inductance and resistance of a TSV is directly proportional to the height of the TSV. TSVs with large heights will generally have higher losses. But the height of the TSV is dictated by the thickness of the substrate which produces higher substrate conductance and capacitance. The radius and height of a particular TSV is dependent on several factors. Typically, 3D ICs with several TSVs that link components at a low hierarchy level will have TSVs with a smaller radius. Yet, 3D ICs with a fewer TSV that connect bigger components will have TSVs that are bigger. The radius of a TSV is directly proportional to its cross-

sectional area. The cross-sectional area of the TSV is inversely proportional to its resistance. To keep the resistance of the TSV minimum will require keeping the cross-section area low. TSVs can be formed at different stages of the fabrication process. TSVs can be formed before BEOL metallization is performed (via-first), between different BEOL metallization steps (via-middle) or after all BEOL metallization is complete (via-last). The detail of each via process step is explained in the following manner: In a via-first process, the vias connect to the local interconnect layer of the BEOL which is used for local routing. In a via-middle process, the vias connect to a higher interconnect layer but uses less local routing a little more global routing. In a via-last process, the vias connect to the highest metal layer which is the global interconnect layer. The global interconnect layer connects to the redistribution layer (RDL) which is at the top of the regular interconnect layers.

2.3 TSV Benefits

With SoC technology developed to miniaturize two-dimensional IC design and boost functionality a little more, the performance, form-factor, scalability and power reduction specifications are becoming increasingly difficult to meet. TSV technology is a conceptual leap from SoC designs and a realization in some technology areas like DRAM memory. In the next few sections, the costs benefits of applying TSV technology over conventional approaches are listed as follows:

2.3.1 Performance:

Maximizing performance, particularly in the memory and logic space, is very difficult to accomplish. In the case of memory, some of the memory bottlenecks often encountered are bandwidth and memory size. However, a more critical factor limiting performance for memory is latency. Nearly all microprocessors are capable of reaching their maximum throughput their memory system can feed them. But, they all suffer from the memory latency. By alleviating the limitations on memory size and I/O bandwidth, it was estimated

that memory performance benefits of up to 25% could be realized [2.21]. These improvements are realizable with TSV technology and chip stacking methodologies.

2.3.2 Form-factor:

Over several decades, shrinking transistor size has shown to be very successful method for cramming more switching devices onto a single chip. However, the laws of physics prevent continued shrinkage of switching devices. Some key advantages of small form factor systems include portability, low power consumption, increase functionality and increase I/O bandwidth. Furthermore, Davis *et al.* reported a 3x reduction in total silicon area and a 12x reduction in chip footprint for a monolithic 3D-IC with 4 device layers when compared to a 2D-IC [2.24]. A quantitative comparison of 3D-IC and 2D-IC design and performance is shown in Table 2.3 to demonstrate the benefits of 3D-IC form factor.

Table 2.3 Monolithic 3D-IC versus 2D-IC using similar technology node [2.25].

22 nm mode	2D-IC	3D-IC
Frequency	600 MHz	600 MHz
Metal Levels	10	10
Average Wire Length	6μm	3.1μm
Av. Gate Size	6 W/L	3 W/L
Die Size (active silicon area)	50mm²	24mm²
Power	Logic = 0.21W Reps. = 0.17W Wires = 0.87W Clock = 0.33W Total = 1.6W	Logic = 0.1W Reps. = 0.04W Wires = 0.44W Clock = 0.19W Total = 0.8W

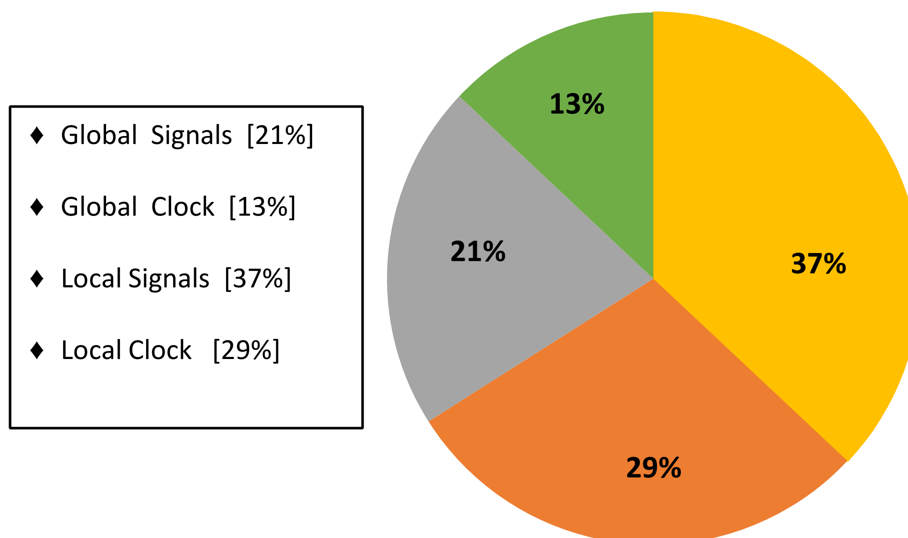


Fig. 7. Interconnect total dynamic power breakdown [2.26]

2.3.3 Scalability:

Interconnect scaling using TSVs enable wire interconnects the capability to keep up with technology node scaling. TSVs can be reduced down in geometry (e.g. height and radius) whereas wire-bond technology struggles. Table 2.3 show the area and power benefits.

2.3.4 Interconnect Power Reduction:

Interconnect power studies and analysis shows that interconnection accounts for over 50% of the dynamic power consumption in high-performance microprocessor [2.22], [2.23]. As a first order approximation, the interconnections are divided into two categories based on the design hierarchy (local and global interconnects). The local and global interconnects show different capacitance characteristics as a function of length. The local interconnects have approximately 25% of interconnect capacitance while the global interconnect capacitance component have about 80%. Although global interconnect capacitance is larger, the interconnect-power peak for the local interconnect nets is higher and it dissipates more dynamic power than global interconnect nets. This is mainly due to the local clock and signal nets. With 3-D integration using TSV technology, TSV parasitics such as capacitance

and resistance by controlling the physical dimensions of the TSV. This is investigated further in chapter 3.

2.4 Electrical Modeling of TSVs

A myriad number of research literatures on packaging technology and interconnect structures that affects power and signal integrity has been published in the last two decades [2.26]-[2.69]. Today several semiconductor companies and national laboratories are investigating approaches to enhance their fabrication process of TSV-based technology for developing stacked systems. Although TSV technology is a critical interconnect component in the development of 3-D integration and replacement of wire-bond technology, accurate electrical characterization of TSV is essential and needed to address power delivery and signal integrity challenges in the future.

The fabrication of TSV process vary due to a number of factors that includes type of metal used to fill TSV, the silicon height, aspect ratio of the TSV, TSV shape and other physical design parameters. Moreover, there are different TSV methods that can be implemented during the IC fabrication process: (1) via-first, (2) via-middle and (3) via-last. The most common TSV shape is cylindrical. However, TSVs can be fabricated in either cylindrical or in a square shape. Once the shape is formed, a barrier is formed to prevent metal from diffusing into the silicon substrate. Tantalum (Ta), Titanium Nitride (TiN) or the most often used silicon dioxide (SiO_2) is used as barrier materials. Copper-based metals are used to fill the TSVs because they have lower resistivity than aluminum (Al), Tungsten (W) and Polysilicon material [2.57], [2.65].

There is a wide range of published works on how TSVs are modeled. There are papers that model an array of TSVs using various numerical modeling techniques that require solving large matrices to study their electrical properties at the system level [2.26],[2.54]. On the other hand, there are published literatures that model a single or a pair of TSVs that are

arranged in different signal-power configurations e.g. P/G, GSG, GSSG, GPPG (G-ground, P-power and S-signal) [2.29]-[2.36],[2.48]-[2.53] and [2.55]-[2.64]. These papers do not require using large matrix solution techniques but they study the properties of basic TSV configurations and their parasitic characteristics (*RLGC*). Finally, there are published works

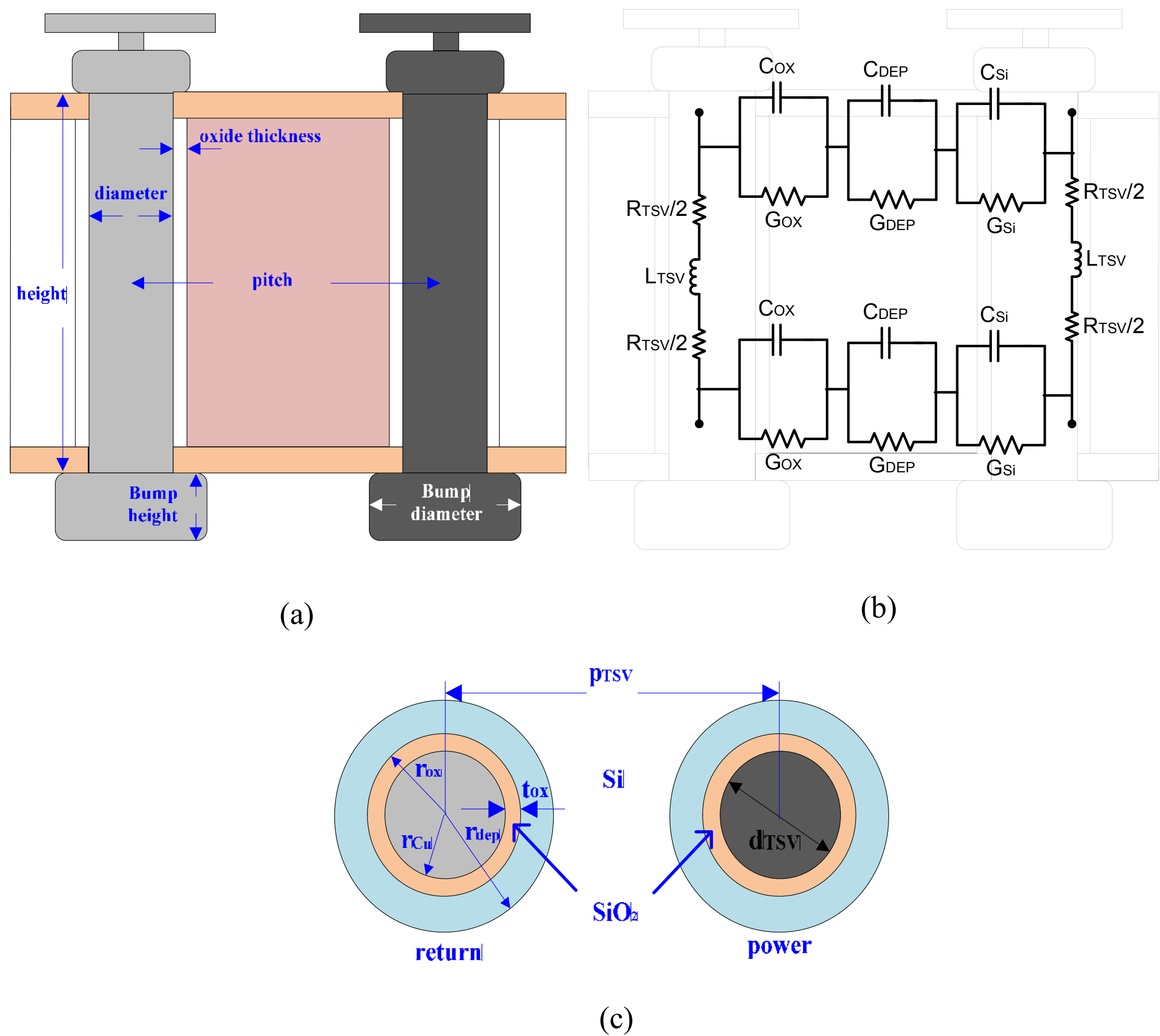


Fig. 8. (a) Power and ground TSV pair including, (b) equivalent circuit parasitic model and (c) top view with radius outlined.

that study the impedance properties of TSV-based power delivery networks and interconnect structures affecting the on-chip signal integrity [2.60], [2.62],[2.65]-[2.70]. Fig. (8): shows a power-ground TSV pair and equivalent circuit parastic model used to characterize the impedance property of the TSV. The equivalent circuit parasitic model includes parasitic resistance, inductance, capacitance and conductance. Each parasitic is described below including a general closed form expression considering the TSV diameter, TSV length, TSV dielectric liner thickness, TSV pitch and silicon conductivity. The closed form expression offers a fast and accurate method to calculate the TSV impedance of the network.

(i) Resistance:

The TSV resistance is a function of the length of the TSV, cross-sectional area of the TSV and the conductivity of the silicon material. The parameters affecting the resistance of the TSV are surface scattering, boundary scattering and the skin effect. There are two types of resistance: (1) the static resistance or DC resistance of the TSV and (2) high-frequency resistance of the TSV [2.30].

$$R_{DC} = \frac{l_{TSV}}{\sigma \pi^2} \qquad \textbf{(2.1a)}$$

$$R_{HF} = \frac{l_{TSV}}{\sigma \pi (2r - \delta)\delta} \qquad \textbf{(2.1b)}$$

$$R_{TSV} = R_{DC} + R_{HF} \qquad \textbf{(2.1c)}$$

where $\delta = 1/\sqrt{\pi f \mu \sigma}$. Eqn. (2.1a) describes the dc resistance of a non-magnetic cylindrical wire. The high frequency effect of the TSV resistance is primarily based on the skin effect. At DC, the current density is uniformly distributed across the cylindrical wire. As the frequency increases, the current density becomes non-uniform

and reduces exponentially with distance. The skin effect which reduces the effective cross-sectional area of TSV lowers the TSV resistance. Eqn. (2.1b) describes this behavior.

(ii) Inductance:

The TSV inductance is determined by the TSV length, TSV diameter and current return path. The inductance is primarily based on the loop formed as current travels into and out of the TSV. The inductance in an integrated circuit is very difficult to determine because of multiple current return paths (tens or even hundreds of returns paths). There are a few effects at high-frequency that changes the current distribution inside a TSV. The first effect is the skin effect and the other effect is the proximity effect. When current flows in the same or opposite direction, the proximity effect reduces the overall inductance in a TSV. Moreover, there is another high-frequency effect that changes the inductance of a TSV and that is the multiple current in the return paths. When the current is redistributed among the many return paths, the overall impedance of the path is minimized. Conclusively, given the frequency, certain return paths will minimize the total impedance than other return paths.

The loop inductance is characterized by two components: (1) self-inductance and (2) mutual inductance. An expression for the self-inductance is [2.30], [2.35] and [2.52]:

$$L_{self} = \frac{\mu_o}{2\pi}\left[ln\left(\frac{l_{TSV}+\sqrt{l_{TSV}^2+r^2}}{r}\right)l_{TSV} + r - \sqrt{l_{TSV}^2 + r^2} + \frac{l_{TSV}}{4}\right] \qquad \textbf{(2.2a)}$$

The mutual inductance between two TSVs e.g. power-ground (P/G) TSV pair is described using the following closed-form expression:

$$L_{mutual} = \frac{\mu_o}{2\pi}\left[ln\left(\frac{l_{TSV}+\sqrt{l_{TSV}^2+p_{TSV}^2}}{p_{TSV}}\right)l_{TSV} + p_{TSV} - \sqrt{l_{TSV}^2 + p_{TSV}^2}\right] \quad \textbf{(2.2b)}$$

To calculate the total loop inductance, one must combine the self and mutual inductance expressions of Eqns. (2.2a) and (2.2b). The total loop inductance is:

$$L_{TSV} = L_{self1} + L_{self2} - 2L_{mutual21} \quad \textbf{(2.2c)}$$

(iii) Capacitance

Similar to the previously mentioned components, the TSV capacitance is characterized by the material properties and physical dimensions of TSV. However, there is another important effect beyond the physical characteristics and material properties that affects the capacitance. This is the effect of the electric field lines and how they terminate to nearby metals and TSVs. The field lines radiate from the TSV conductor and terminate to a back metal reference (ground) plane. A depletion region is formed around the TSV and is considered into the closed-form expressions published in several

The analytical expressions used for electrically characterizing the different capacitor models of a TSV are shown in Eqn. **(2.3)**. The closed-form capacitor model for Cox describes a capacitance that is isolated from the conductive silicon and represents half of the whole oxide capacitance.

$$C_{ox} = \frac{1(2\pi\varepsilon_o\varepsilon_{ox})}{2} \cdot \frac{l_{TSV}}{ln\left(\frac{d_{TSV}/_2+t_{OX}}{d_{TSV}/_2}\right)} \quad \textbf{(2.3a)}$$

where the TSV physical design and material parameters are TSV length, l_{TSV}, TSV diameter, d_{TSV}, the pitch between TSV pair, p_{TSV}, and the silicon dioxide thickness, t_{ox}. The depletion region capacitance is characterized by:

$$C_{dep} = \frac{2\pi\varepsilon_{ox} l_{TSV}}{ln\left(\frac{r_{dep}}{r_{ox}}\right)} \tag{2.3b}$$

where r_{dep} is the maximum depletion radius, r_{ox} is the radius from the center of TSV conductor to the oxide layer and r_{Cu} is the radius of the TSV.

$$C_{Si} = \frac{\pi\varepsilon_{o}\varepsilon_{Si}}{cosh^{-1}\left(\frac{p_{TSV}}{d_{TSV}}\right)} \cdot l_{TSV} \tag{2.3c}$$

The total capacitance of the TSV structure is expressed using the following closed-form expression:

$$C_{TSV} = \frac{C_{OX} \cdot C_{dep}}{C_{OX} + C_{dep}} + \frac{1}{C_{Si}} \tag{2.3d}$$

In later works, more closed-form expressions of the TSV capacitance were developed based on TSV bundling where self and inter-via coupling capacitance between each and every TSV are defined.

(iv) Conductance

The TSV conductance change with different levels of resistivity in the silicon substrate (low-, medium- and high-resistivity). We focus on two conductive components of the TSV. The first component is the silicon substrate conductance of the TSV, G_{Si}. The

conductance of the silicon substrate is primarily based on the amount of majority carrier concentration. The closed-form expression of the silicon substrate conductance is represented in Eqn. (2.4a):

$$G_{Si} = C_{Si}\frac{\sigma_{Si}}{\varepsilon_{si}} \tag{2.4a}$$

where σ_{si}, is the conductivity of the silicon substrate and ε_{si} is silicon permittivity. The oxide conductance is characterized using the following expression:

$$G_{ox} = C_{ox}\frac{\sigma_{ox}}{\varepsilon_{ox}} \tag{2.4b}$$

The depletion conductance expression used considers the threshold voltage, V_{TH}, the applied voltage, V_{app} and the depletion region width, w_{dep}.

$$G_{dep} = \frac{\sigma_{Si}}{ln\left(\frac{r_{Cu}+t_{ox}+w_{dep}}{r_{Cu}}\right)} \cdot \frac{1}{\sqrt{1-\frac{V_{app}}{V_{TH}}}} \cdot 2\pi l_{TSV} \tag{2.4c}$$

The total TSV conductance is estimated using the following expression.

$$G_{TSV} = \frac{G_{Si}G_{Ox}}{G_{Si}+G_{Ox}} + \frac{1}{G_{dep}} \tag{2.4d}$$

Other TSV conductance models consider the loss tangent of a lossy material where the capacitance is strongly dependent on the frequency and the complex permittivity. The expressions for TSV conductance can be used to compare with other TSV conductance expressions that consider other physical material or frequency dependent phenomena.

Chapter Summary

In summary, a detail discussion on the state of the art on on-chip interconnect technology was presented. We briefly reviewed a background in TSV technology and discussed prior works pertinent to the area. From traditional 2D system integration to 3D system integration, there exist a trend to shrink the physical geometry of wire-bond technology or transition from traditional 2D interconnect design so that semiconductor companies are able to keep up with technology scaling and design TSV-based 3-D integrated systems. The chapter covered previous works related to the characterization of TSV electrical properties and presented some closed-form expressions used to estimate the RLGC characteristics of TSVs. The chapter briefly discussed the performance, scalability, form-factor and interconnect power reduction TSV provides.

CHAPTER III

Parametric Modeling of On-Chip Interconnects

3.1 Back-End of Line (BEOL) for Power Grid Structures

Back-end of line (BEOL) interconnects are used in integrated circuits for the purpose of distributing clocks, high-speed signals and provide power-ground to various logic circuitry across the chip. There are three types of interconnects: local, intermediate and global.

- Local interconnects include very thin lines, connecting gates, and transistors within a functional block. They usually span a few gates and occupy the bottom 1st and 2nd layer-levels. The resistance is usually higher at these layers.

- Intermediate interconnects are wider and taller than local interconnects. The intermediate interconnects have lower resistance than local interconnects because the widths are wider.

- Global interconnects contain clock and signal distribution between functional blocks. Global interconnects deliver power-ground to all functional blocks. The global interconnects reside on the top level of the BEOL layer usually the 1st and 2nd layer levels from the top. The global interconnects are longer and wider than intermediate and local interconnect layers. Moreover, global interconnects contain lower resistivity than intermediate and local interconnect layers.

The characteristics of BEOL interconnects at all levels are critical, particularly the local interconnect level. The RC delay of the transistor is determined by the design of the local interconnect layer. Since the resistivity at the local interconnect level is higher than the other interconnect levels (e.g. intermediate and global), the preferred metal material to use in BEOL interconnect process is copper (Cu) instead of aluminum (Al). Copper has a lower resistivity property than aluminum and it's highly conductive. A lower resistivity interconnect means the RC delay is reduced and the IC speed is increased. The interconnect characteristics for the power grid structure are described in this section. We investigate the variation in power grid dimensions and monitor the parasitic elements (resistance, inductance and capacitance) that directly affect the RC delay and SSN noise (L***di/dt***) behaviors.

In the parametric study, we vary the metal width, metal thickness and metal pitch of the BEOL power grid structure. We begin the parametric study with global interconnect and scale the physical dimensions down to the physical dimensions of at the local interconnect level. The main goal of this analysis is to determine how the metal width, metal pitch and metal thickness affect the inductive, resistive and capacitive characteristics of the BEOL power grid structure. The performance at the IC level is dictated by the electrical characteristics of the BEOL interconnects.

The power grid structure is constructed with paired power-ground lines. Depending on the pitch of the power grid structure, the capacitive coupling could potentially increase due to the close proximity of the power-ground pair. The paired power-ground lines for global and local BEOL interconnect levels are illustrated in Fig. (9). An example of a unit cell structure based on the power grid structure Fig. (9), is shown in Fig. (10). The physical design parameters are declared in Fig. (10). These design parameters of the grid are denoted as follows: metal thickness (T), metal width (W), metal pitch (P) and dielectric thickness (H). The dielectric thickness of the material was excluded in this study because we were primarily focused on the physical size variation of the BEOL metal-line interconnects. The effect of the dielectric thickness on mobility has been studied extensively. The reduction in dielectric thickness is a promising technique to improve IC performance but leads to

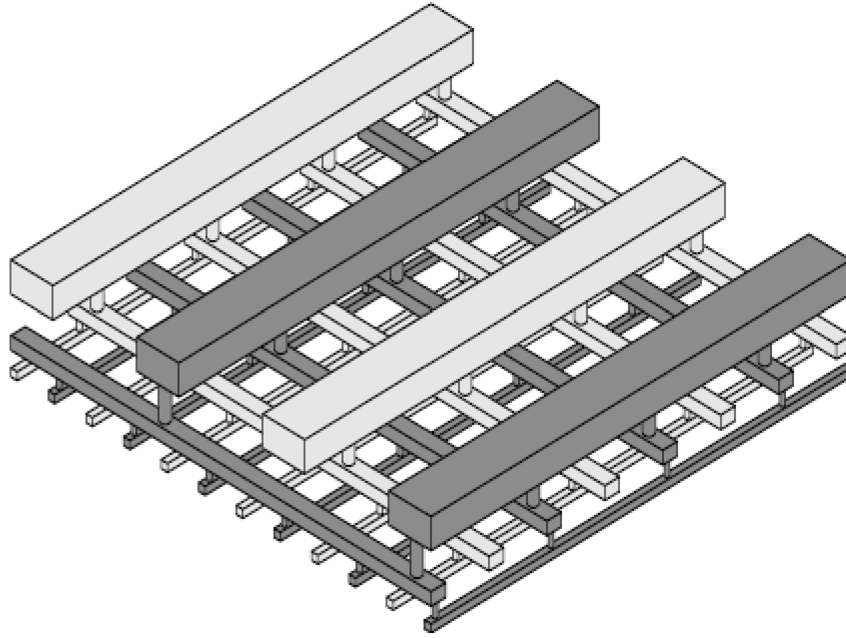


Fig. 9. Interdigitated power/ground pair showing global (top layer) and local (bottom layer) interconnect level [2.19].

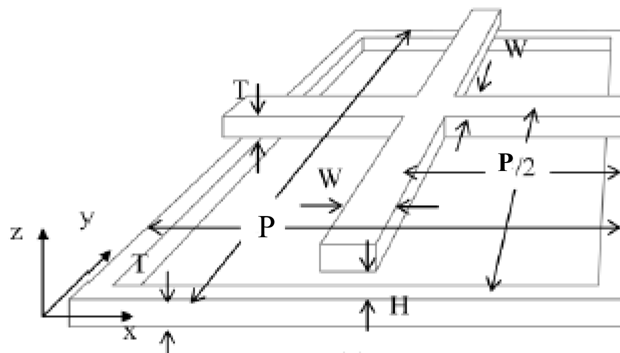


Fig. 10. Defined parameters of a unit cell power grid structure used in the parametric study [3.1].

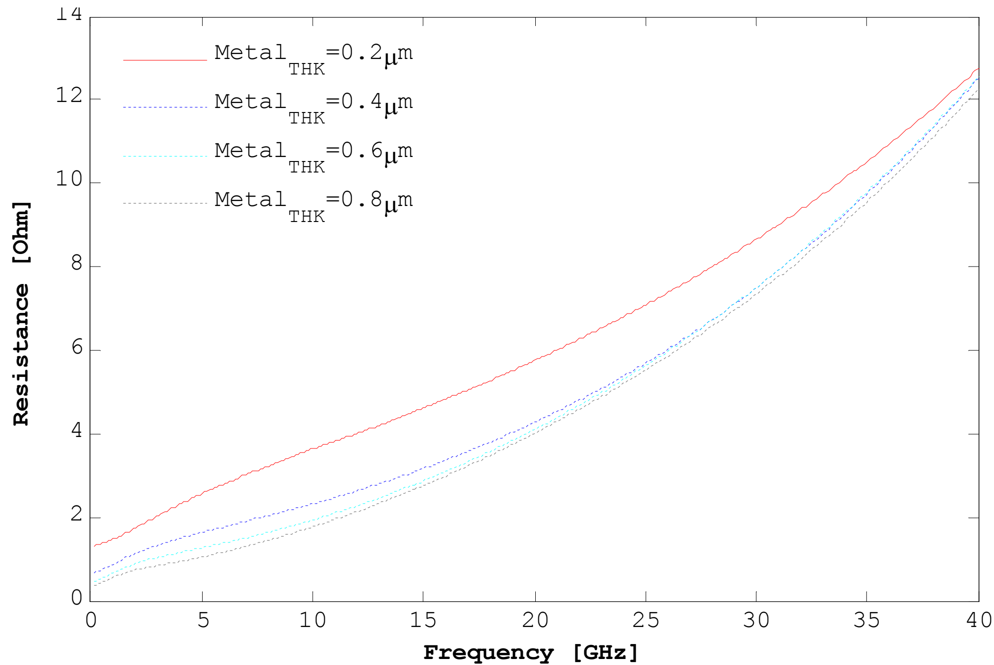


Fig. 11. Parasitic resistance versus frequency for a given metal thickness.

higher dielectric capacitance (C*i* per unit area). This results in reduction in operating voltages through reduction in threshold voltage [3.2]. The dielectric thickness was fixed at 0.2-µm. However, the dielectric thickness was varied and increased up to 0.8-µm. The result show the dielectric thickness is inversely proportional to intrinsic capacitance.

The scaling of the metal thickness from 0.2-µm – 0.8-µm is shown in Fig. (11). The figure illustrates the electrical resistance versus frequency for a given metal thickness. The trend suggests that as the metal thickness increases the electrical resistance reduces. This is important to underscore because one aspect of controlling the parasitic resistive properties is through the thickness of the metal structure. Local-level BEOL interconnects can be designed to be thicker to keep parasitic resistance low. Transistor devices stand to benefit from thicker metal lines to improve RC delay and overall chip performance. However,

thicker metal lines at the local interconnect level means sidewall capacitance increases which raises another signal integrity issue in crosstalk. There is a delicate balance between RC

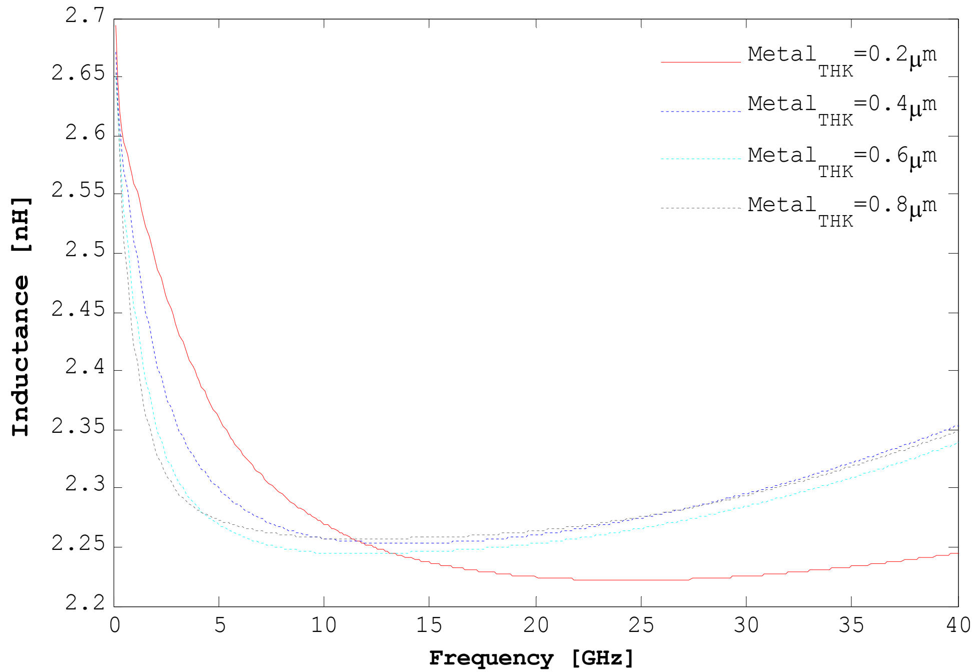


Fig. 12. Parasitic inductance of unit cell power grid for a given metal thickness.

delay and crosstalk wherein on-chip PDN designers must consider the optimal PDN design and metal routing strategies for local-level interconnects to avoid crosstalk and increase RC delay issues. In this study, we kept the metal thickness fixed at 0.5-µm for the local level.

The effect of metal thickness on inductance as a function of frequency is simulated in Fig. (12). With the metal thickness ranging from 0.4-µm to 0.8-µm, the simulated inductance waveform for the different metal line thickness converged to roughly similar inductance value as the frequency is simulated up to 40 GHz. However, with the metal thickness at 0.2-µm, the inductance is lowered by 5%. The trend with metal thickness and inductance is that as the metal thickness decreased, the inductance is lowered. In the previous analysis with parasitic resistance, we observed a different behavior where decreasing metal thickness

increased resistance. Techniques to lower the inductance on interconnects should be applied to ground interconnect structures so as to minimize the area of the current loop. As far as the interconnect sidewall capacitance, it can be mitigated by reducing the metal thickness. In summary, reducing the metal thickness lowers parasitic inductance and capacitance. However, the opposite affect is seen with parasitic resistance. In an effort to reduce the RC delay for local-level interconnects, we kept the metal thickness below 0.5-μm to ensure the parasitic capacitance is lowered. This will ensure the overall impedance of the PDN at the local-level is kept low. Conclusively, reducing the metal thickness of the local level interconnect, particularly, the ground interconnect structures will ensure no inductive and capacitive contribution to the PDN.

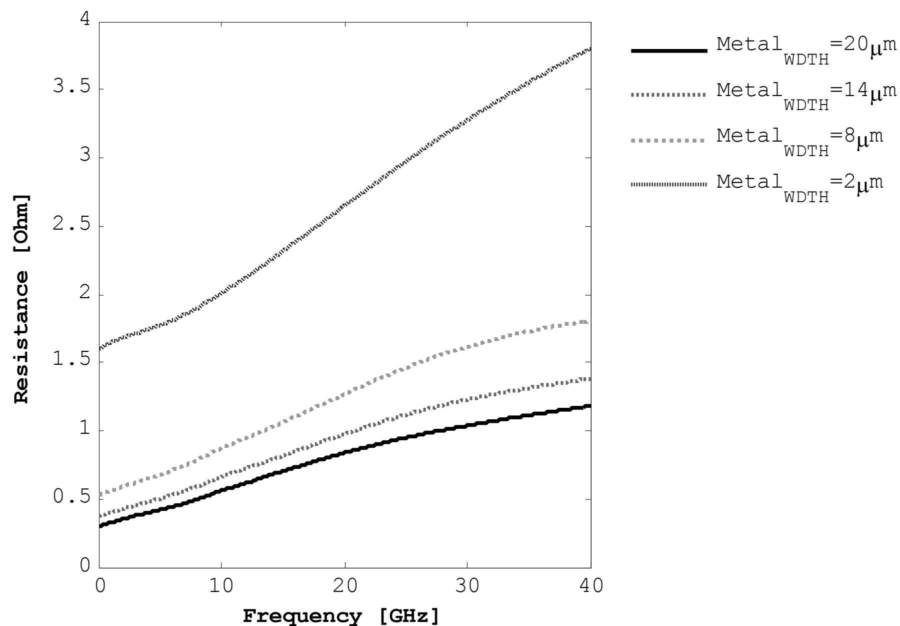
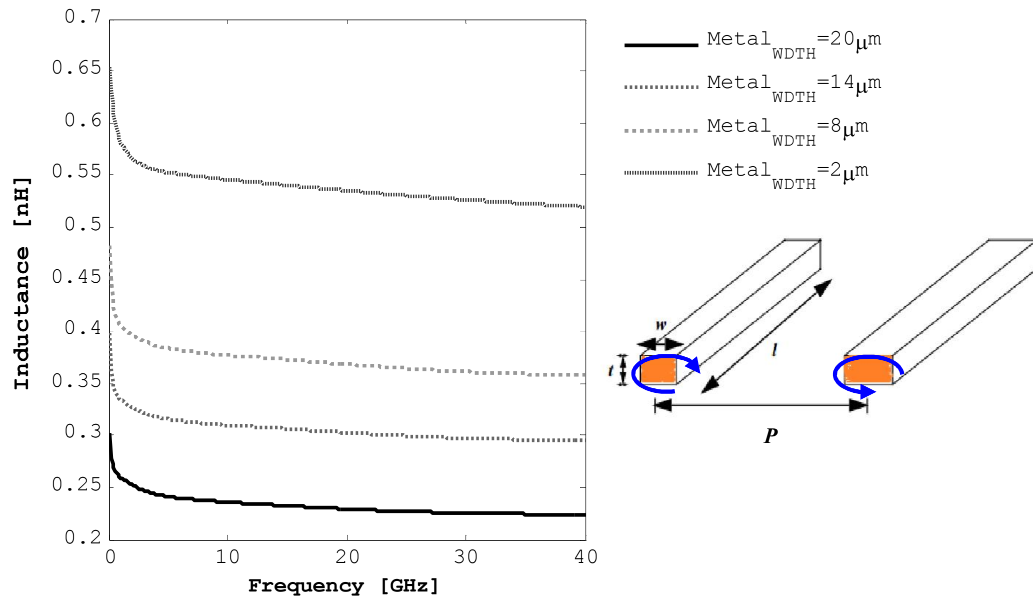


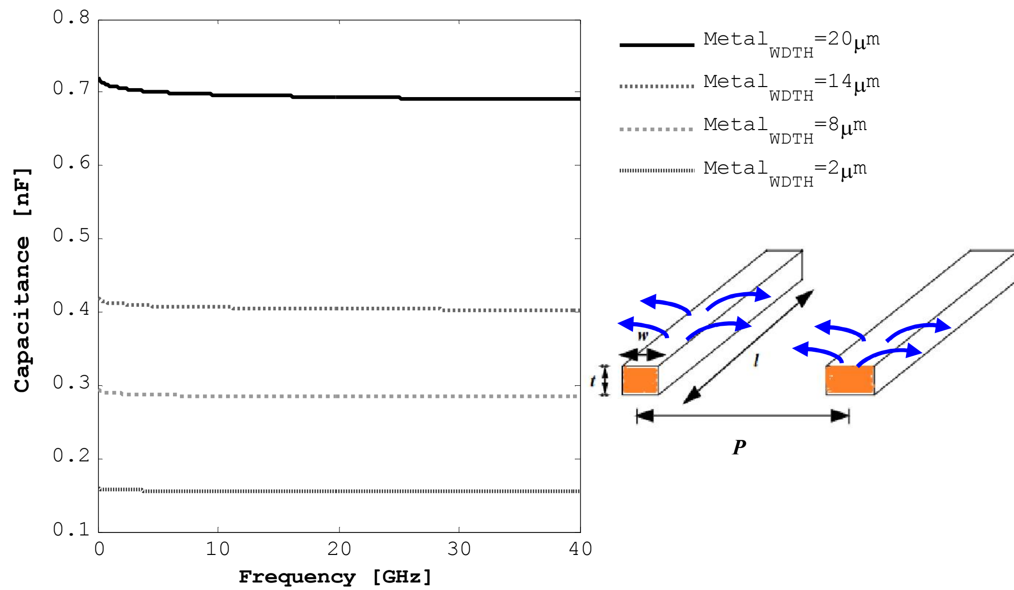
Fig. 13. Parasitic resistance versus frequency for a given metal width.

In this section, the metal width of the unit cell power grid structure was scaled. Figure (13) show results of the parasitic resistance versus frequency as the metal width varied. The

increase of the metal width has an inverse effect on the parasitic resistance. This is explained when looking at the cross-sectional area of the power grid interconnect. The cross-sectional



(a)



(b)

Fig. 14. Inductance and capacitance versus frequenncy for a given metal width.

area is the product of the thickness times width. The resistance is inversely proportional to the cross-sectional area given the following expression: $R = \rho l / A$, where l is the interconnect of the metal line length, ρ is the material resistivity of copper and A is the cross-sectional area of the interconnect denoted by the metal width, w and metal thickness, t. Figure (14) depicts a simulated parasitic inductance and capacitance of a unit cell power grid structure. The metal width is inversely proportional to the parasitic inductance. The behavior of the inductance was observed for a given metal width. As the metal width increased the parasitic inductance decreased. This was not the case for the parasitic capacitance. The width of the power grid interconnect is proportional to the parasitic capacitance. As the metal width increased, the parasitic capacitance increased due to the fringe capacitance. Conclusively, the metal width is another knob that can be used to control the parasitic resistance, inductance and capacitance of the interconnect structure. Also, in figure 14, we show a pair of power ground interconnects where ***t***, represents the interconnect thickness, ***w*** is the width and ***p*** is the interconnect pitch

Lastly, the pitch of a unit cell power grid was varied. The pitch or spacing values were obtained from the International Technology Roadmap for Semiconductors (ITRS). We used the following pitch to separate the return and power metal line, 90-µm, 120-µm, 150-µm and 180. Figure 15 shows the parasitic inductance versus metal pitch. In this plot, we observed marginal increase in parasitic inductance of the unit cell power grid structure. The proximity of the power-ground pair constitutes the strength of the inductive and capacitive coupling between the two wires. However, irrespective of the pitch value, the metal pitch has little effect on the parasitic inductance. The dependence of the parasitic inductance relies heavily on the metal line length rather than on the metal pitch [2.19].

The variation of the resistance, inductance and capacitance as a function of frequency in high performance distribution is investigated in this section. The variation of the metal

width, metal thickness and metal pitch were analyzed for a unit cell power grid using HFSS. The parametric sweep results of the power grid structure support the design of area efficient and robust power distribution grids in high speed integrated circuits. The results of this section are summarized as follows:

- The inductance of power distribution grids decreases with increasing signal frequency.
- The parasitic resistance of the power distribution grids is controlled using the cross-section area (metal thickness and metal width). The metal width and thickness are inversely proportional to the parasitic resistance.
- The parasitic capacitance of the power distribution grid is proportional to the metal thickness and metal width.
- The smaller the metal pitch (separation) between the power and ground metal lines and the wider the lines, the more significant the proximity effects become and the greater the relative decrease in inductance with frequency.

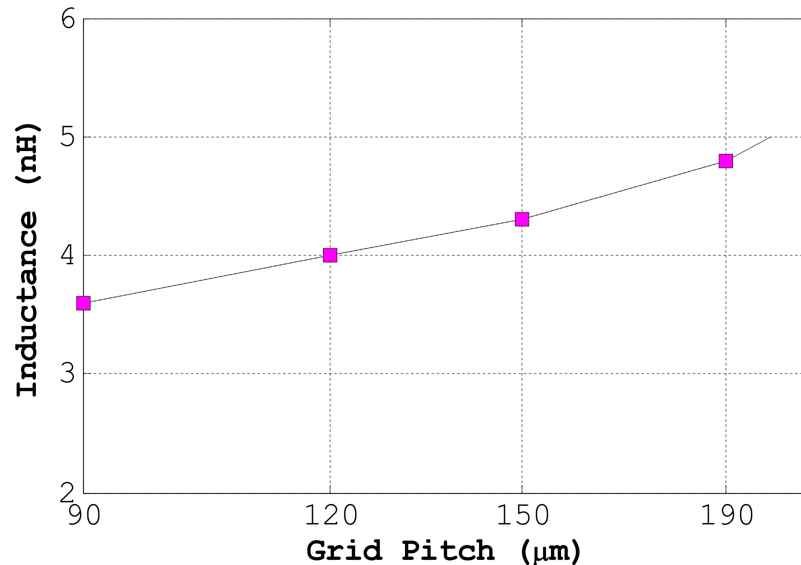


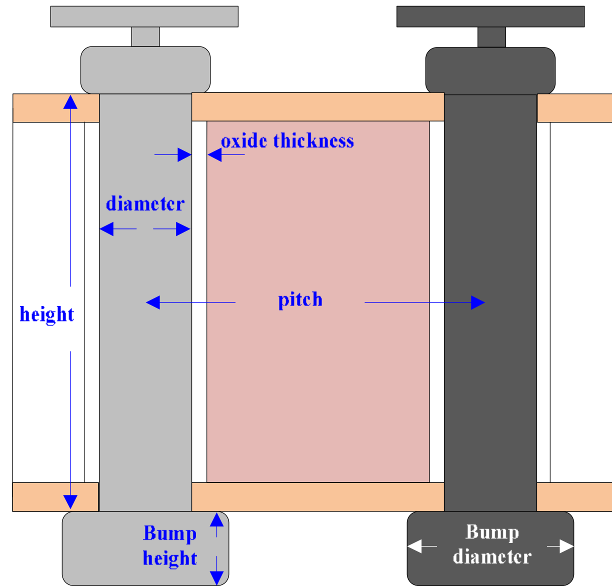
Fig. 15. Inductance for a given pitch variation over a wide range of frequencies.

3.2 Power-Ground TSV Interconnect Pair

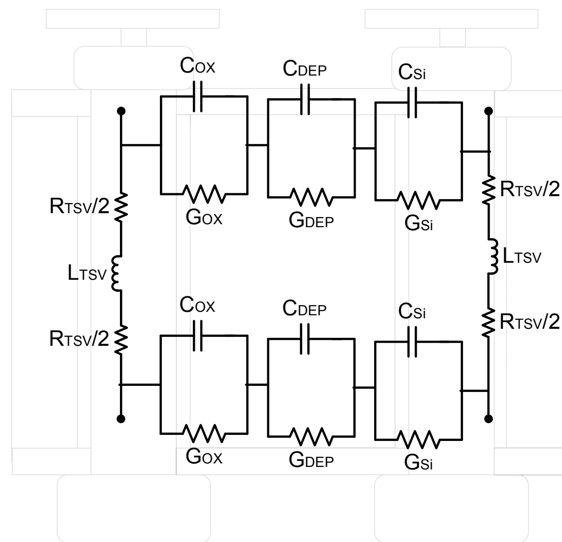
In this section, a high-frequency parametric study of a power-ground TSV pair is performed. The power grid model includes a micro-bump and redistribution layer (RDL). The physical dimensions of the RDL and micro-bump have remained constant for the construction of the power deliver network. For the scalability of the power-ground TSV pair, the model is proposed with structural parameters and material properties as indicated in Table 3.1. The analytical RLGC equations of the TSV pair are derived from the physical configuration of the design parameters.

Table 3.1
VALUE OF INTERCONNECT COMPONENTS OF A UNIT CELL

Parameter	Value
TSV diameter	$2x10^{-6}$ m – 30 $x10^{-6}$ m
TSV height	$20x10^{-6}$ m – 110 $x10^{-6}$ m
TSV pitch	$80x10^{-6}$ m – 200 $x10^{-6}$ m
TSV Oxide thickness	$0.5x10^{-6}$ m - $1x10^{-6}$ m
RDL pad diameter	$4x10^{-6}$ m
RDL thickness	$1x10^{-6}$ m
PDN grid width	$2x10^{-6}$ m - $25x10^{-6}$ m
PDN grid spacing	$90x10^{-6}$ m - 200 $x10^{-6}$ m
PDN grid thickness	$0.2x10^{-6}$ m
PDN grid length	200 $x10^{-6}$ m
Substrate conductivity	10-S/m
Micro-bump diameter	$20x10^{-6}$ m
Micro-bump height	$15.4x10^{-6}$ m
Micro-via height	$0.5x10^{-6}$ m
Micro-via diameter	$0.25x10^{-6}$ m
Cu resistivity	$1.68x10^{-8}$ m



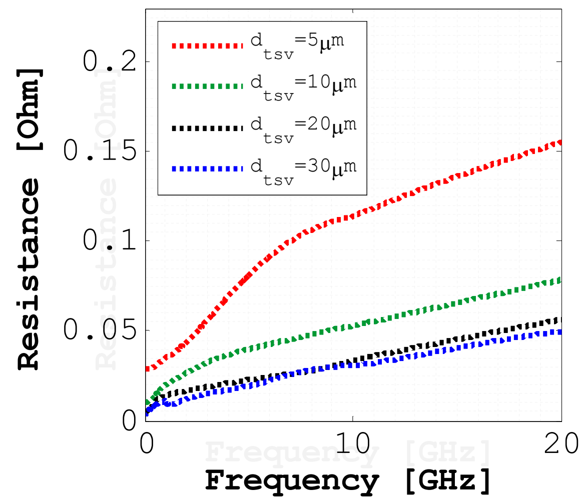
(a)



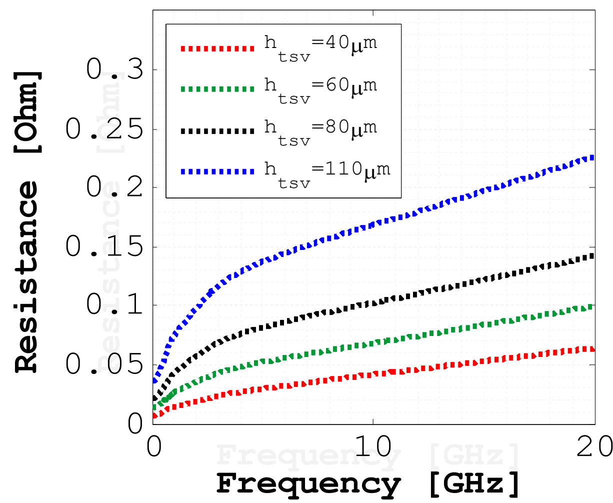
(b)

Fig. 16. A structure of a power TSV and ground TSV with micro-bump showing the structural parameters and (b) shows the electrical RLGC components.

The table above shows the physical design parameters used to construct a unit cell power grid structure. The values for the TSV height, diameter, pitch and oxide thickness used during the parametric study will denote the parasitic resistance, inductance and capacitance characteristics. The results of the parametric study are used to design TSV-based power grid.



(a)



(b)

Fig. 17. Variation of TSV resistance with its (a) diameter and (b) height.

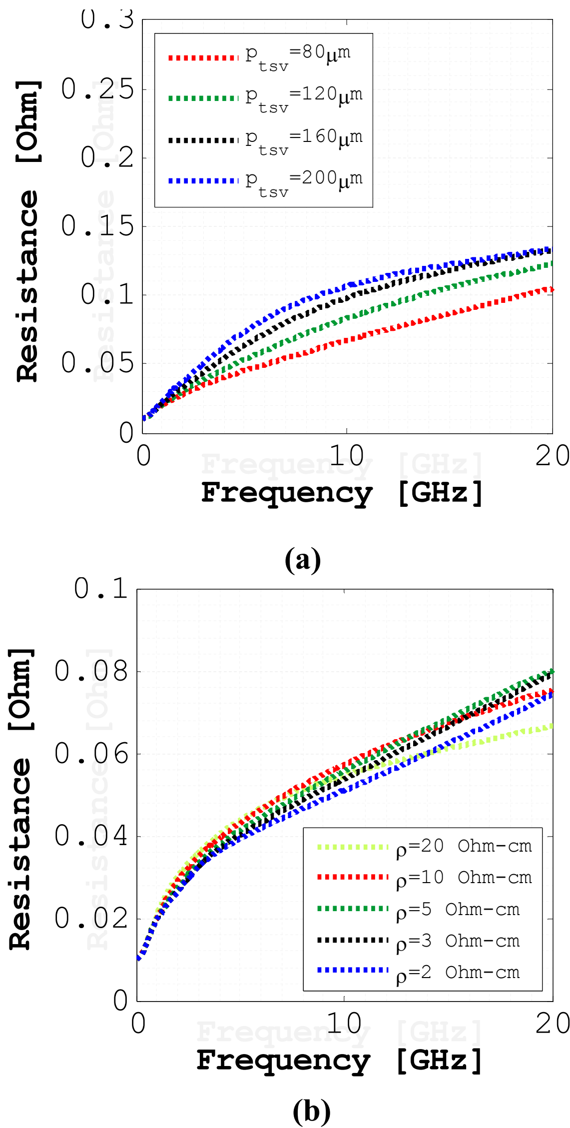


Fig. 18. Variation of TSV resistance with its (a) pitch and (b) resistivity.

In figure 16, the structure and parameters of the power grid line, ground grid line and micro-bump interconnect for a power-ground TSV pair is shown. High-frequency analytical equations of the TSV parasitic resistance, inductance, capacitance and conductance can be derived based on the physical configuration of the TSV. Figure 17, 18 and 19 shows the variation of TSV resistance based on the physical design parameters (e.g. diameter, height,

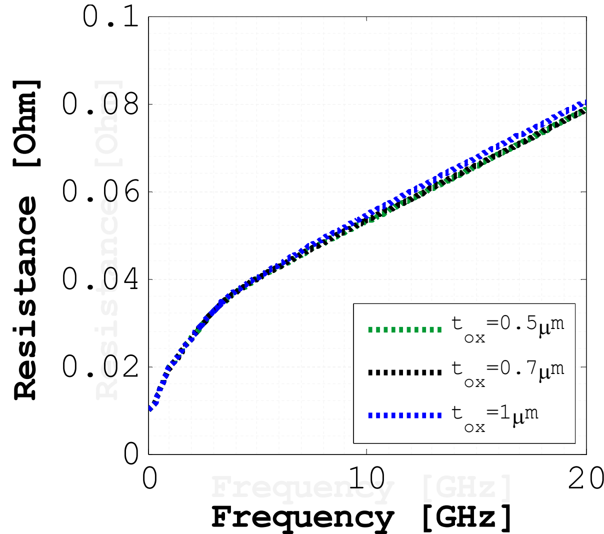


Fig. 19. Variation of TSV resistance with oxide thickness.

pitch and oxide thickness) as a function of frequency. For each physical design parameter, the values were swept using 3D field solver, HFSS of Ansoft. Figure 17(a) shows a plot of the TSV resistance for a given TSV diameter, d_{TSV}. By increasing the TSV diameter, the resistance of the P/G TSV is decreased. The TSV diameter ranged from 5-µm to 30-µm. The other design parameters were constant during the sweep.

The overall TSV-based PDN impedance at low frequency is also lowered. This is discussed in more details in chapter 4. In figure 17(b), we showed that the height of the TSV is directly proportional to the TSV resistance. The TSV resistance monotonically rises over the frequency range up to 20 GHz for a given TSV height. The range of the TSV height goes from 40-µm and increased by increments of 20-µm up to the maximum TSV height,110-µm. The minimum TSV-to-TSV pitch is 80-µm. The TSV pitch is incremented by increments of 40-µm up to 200-µm. However, based on figure 18(a), there is marginal increase in TSV resistance for the different pitch sizes. This shows that the TSV pitch has little effect on the TSV resistance. The TSV pitch can be determined by the following expression Eqn. (3.1). The expression considers the design of the TSV to minimize the size and maximize the TSV

pitch without exceeding the maximum resistance allowed for a given design application.where WA is the wafer-to-wafer alignment overlay and S_{m2m} is the minimum metal-to-metal spacing, R is the TSV resistance, θ is the taper angle of the TSV cavity, t_{ox} is the oxide thickness of the TSV and h_{TSV} is the TSV height.

Figure 18(b) is a plot of the TSV resistance for a given silicon resistivity, ρ_{Si} (or conductivity, $\sigma_{Si} = 1/\rho_{Si}$). The silicon resistivity is a material property that is capable of having significant effect on the electrical characteristics of the P/G TSV. The resistive loss from a TSV is through the silicon substrate. The parameters G_{Si} and G_{ox} determine the overall insertion loss of the P/G TSV channel. As the silicon resistivity increases from 2 Ohm-cm to 20 Ohm-cm the conductance (G_{Si} and G_{ox}) of the silicon substrate decreases. As a result, the overall insertion loss of the P/G TSV channel decreases. In conclusion, the physical design parameters for the P/G TSV aren't the only physical parameters that affect TSVs but the material property of the silicon substrate has an impact on the electrical characteristics of the TSV.

The TSV resistance for a given oxide thickness is plotted in Figure 19. The variation in oxide layer thickness goes from 0.5-µm to 1-µm. The oxide layer thickness protects the TSV from the influence of the conductivity of the silicon substrate layer. The TSV resistance is marginally affected by the oxide layer thickness since the radius between the TSV metal copper area, r_{Cu} and r_{ox} is marginal. To observe a considerable increase in TSV resistance, the TSV radius, r_{Cu}, value has to be large.

$$P = 2WA + 2 \cdot t_{ox} + S_{m2m} + h_{TSV} \cdot tan\theta + \sqrt{\left((h_{TSV} \cdot tan\theta)^2 + (\rho h_{TSV}/R)\right)} \qquad \textbf{(3.1)}$$

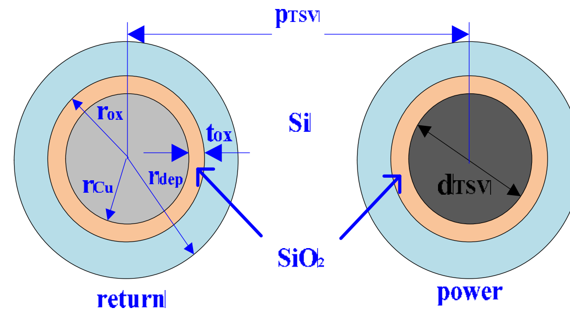


Fig. 20. Top view of P/G TSV pair with radius and material property outlined.

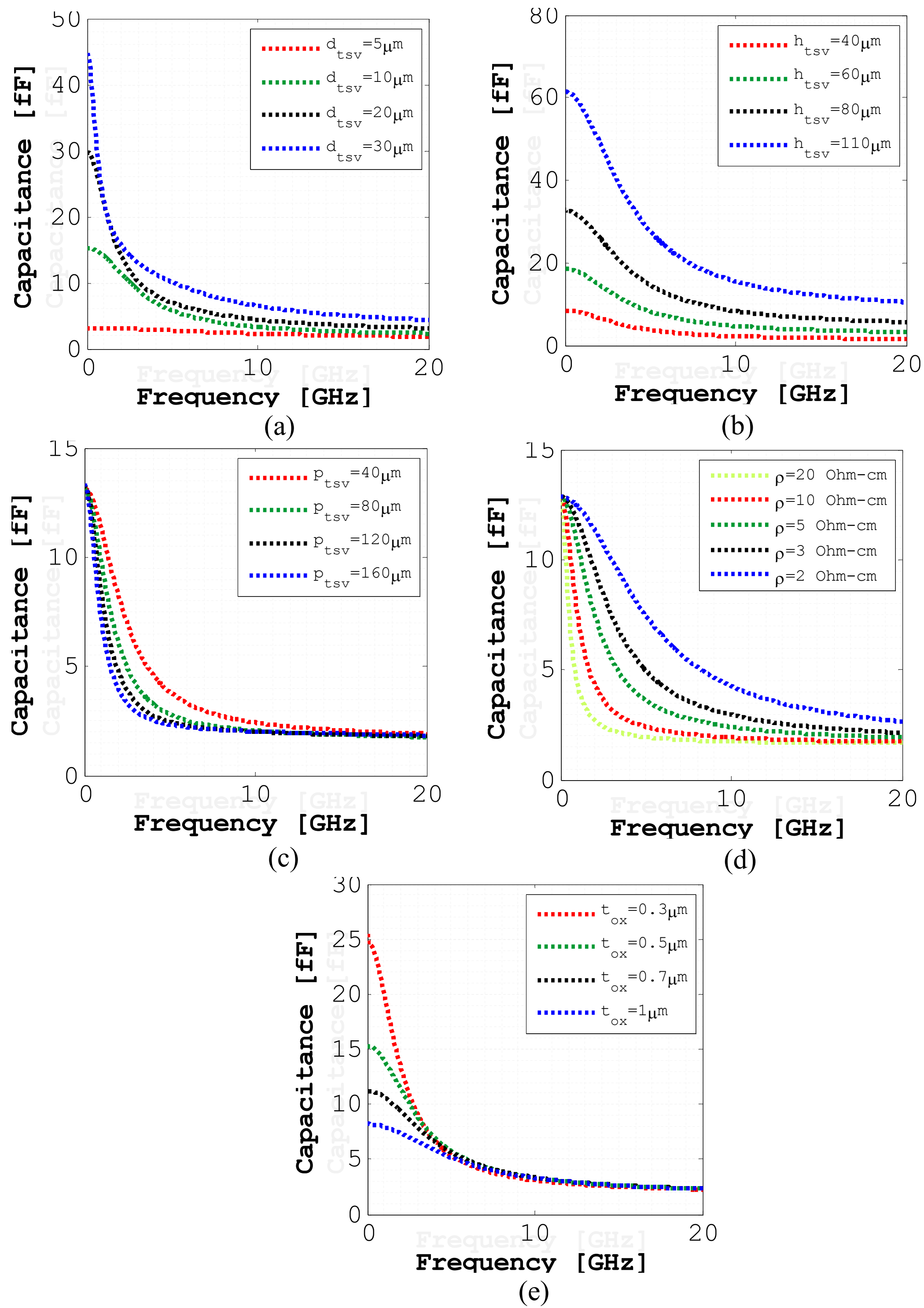


Fig. 21. TSV Capacitance parametric sweep of design parameters (a) d_{TSV}, (b) h_{TSV}, (c) p_{TSV}, (d) ρ_{Si} and (e) t_{ox}.

Figure 21 shows the simulated TSV capacitance between two TSVs as a function of the diameter, height, pitch, silicon resistivity and oxide layer thickness. The TSV capacitance consist of two components: (1) the oxide layer capacitance formed between the TSV copper and the silicon substrate layer, C_{ox} and (2) the capacitance formed between two TSV structures where the silicon substrate separated the P/G TSVs, C_{Si-sub}. The TSV capacitance is the total parasitic capacitance of the P/G TSV pair.

The diameter of the TSV is swept from 5-µm to 30-µm. Figure 21 shows the TSV diameter is a function of the TSV capacitive property and is directly proportional to each other. As the diameter increases, so does the overall TSV capacitance as the TSV pitch and height between P/G TSV pair remains fixed. By increasing TSV diameter, in effect, C_{ox} and C_{Si-sub} parameters are increased. At low frequency the overall TSV capacitance is high but drops significantly as the frequency increases.

The height of the TSV is simulated from 40-µm to 110-µm. The TSV height takes on a similar behavior as the TSV diameter. As the TSV height increases, the capacitive property of the TSV increases. The TSV height has the largest impact on the capacitive property relative to d_{TSV}, t_{ox}, or p_{TSV}. The spacing between P/G TSV has an effect on the TSV capacitance. The strength of the electric field is dictated by the TSV pitch. As the TSV pitch increases, the TSV capacitance reduces. This is more apparent at frequencies between 2 GHz and 7 GHz. At frequencies above 10 GHz, the TSV capacitance converges to a single value of 3 GHz.

The material property of the silicon substrate is inversely proportional to the TSV capacitance. The frequencies between 2 GHz and 12 GHz show a gradual reduction in TSV capacitance for a given material property. Since the silicon resistivity is inversely proportional to the silicon conductivity, the TSV capacitance is shown to be directly proportional to the conductivity. Therefore, the material property of the silicon substrate also affects the TSV capacitance. The oxide layer thickness at low frequencies, particularly at frequencies < 3 GHz, shows that as oxide layer thickness increases the TSV capacitance decreases. As frequencies get higher the impact of oxide thickness layer is negligible.

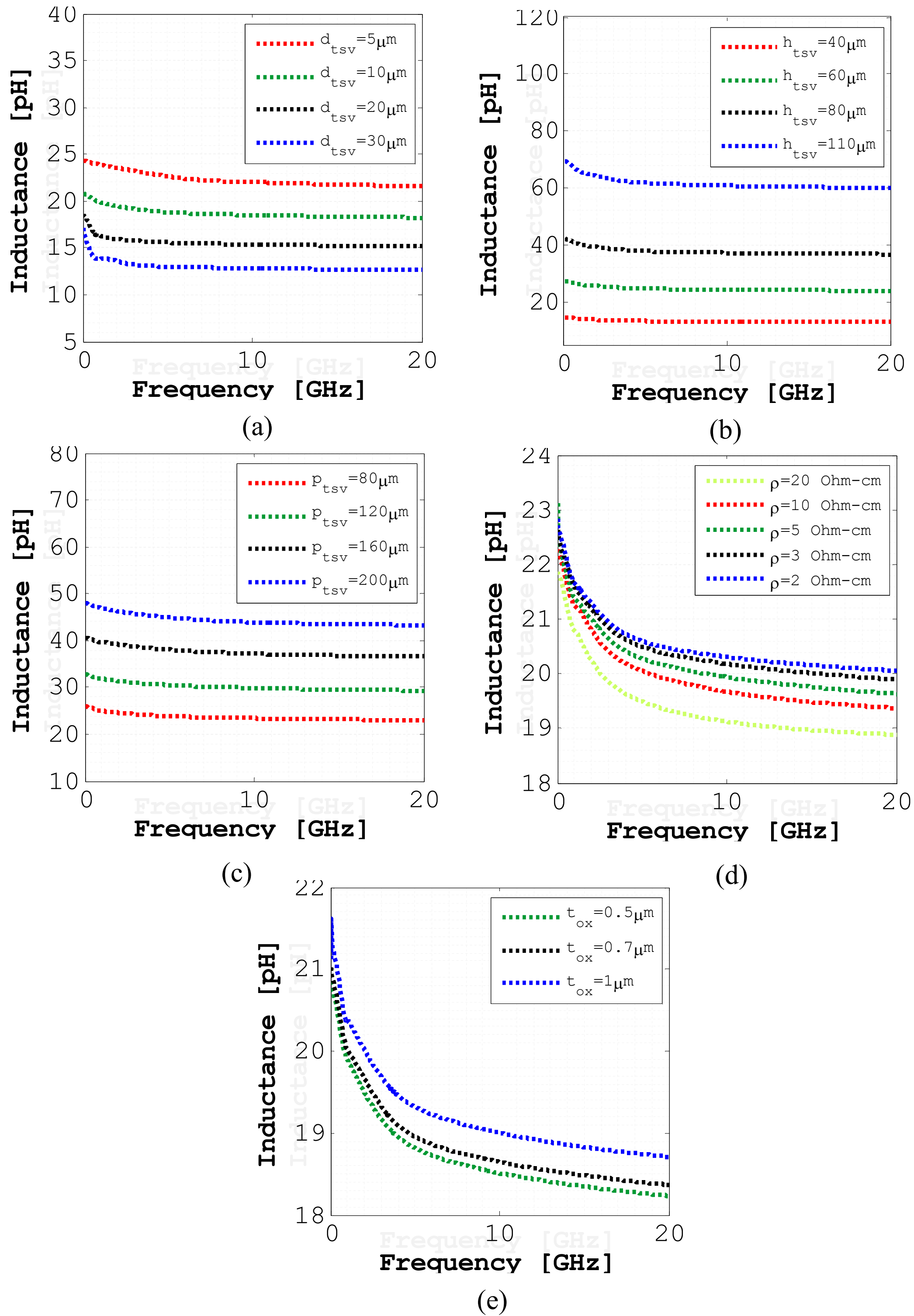


Fig. 22. TSV Inductance parametric sweep of design parameters (a) d_{TSV}, (b) h_{TSV}, (c) p_{TSV}, (d) ρ_{Si} and (e) t_{ox}.

The inductive property of the P/G TSV with variation in height, diameter, pitch and material property is described in Figure 22. We use the same physical design parameters used during the analyses of the TSV resistance, R_{TSV}, and TSV capacitance, C_{TSV}, to analyze the behavior of the TSV inductance. The inductance for a single TSV structure is mainly determined by the TSV height, diameter and material property. For a P/G TSV pair, the TSV pitch becomes an important parameter because of the formation of the inductive loop (coupling inductance and self-inductance) given the spacing of the return path.

We begin our analysis of the diameter with a P/G TSV model. As the TSV diameter increases (similarly, increasing radius), the TSV inductance decreases. It can be observed, in the figure, that the TSV inductance decreases and flattens as the frequency increases. The results show that having a large TSV diameter will minimizes the inductive property of the TSV structure 25pH to 14pH. The TSV height plays a dominant role on the inductive property of the TSV structure. The TSV height is directly proportional to the TSV inductance based on the equation Eqn. **(2.2c)**. A TSV height set at 110-μm corresponds to a TSV inductance of 75pH at low frequency and eventually converge to an inductance value of 60pH at high frequency. When designing the TSV-based PDN, it is important to keep the TSV height < 60-μm to ensure minimal inductive contribution from TSVs. The TSV pitch is another strong design parameter affecting TSV inductance. This is mainly due to the formation of the inductance loop. As the TSV pitch increases, the TSV inductance increases. The inductance is approximated at 45pH which corresponds to a TSV height of 200-μm and 25pH with respect to a TSV pitch of 80-μm. Since the TSV height and pitch are the parameters with considerable impact to TSV inductance, it is critical to keep them as low as possible to ensure robust power integrity for 3D IC power delivery design. The material property of the silicon substrate has an inverse affect on the TSV inductance. As the silicon resistivity of the silicon substrate increases, the TSV inductance decreases. However, the impact of the silicon resistivity on TSV inductance is minimal relative to the impact the TSV height and pitch has on the TSV inductance. Finally, the oxide layer thickness is proportional to the TSV inductance. Yet, t_{ox} has minimal impact on the TSV inductance.

The TSV conductance is another electrical component capable of changing the electrical characteristics of the TSV. The conductance of the TSV is composed of two distinct parameters which are: (1) the silicon dioxide conductance, G_{ox} and (2) the silicon substrate conductance, G_{Si}. The TSV conductance has been simulated and plots have been generated. The simulated plots of the TSV conductance can be found in Appendix A. In summary, we present in Table 3.2 of the parasitic circuit element (*RLGC*) with respect to the variation in physical design parameters based on a P/G TSV model. The table shows how TSV resistance, inductance, capacitance and conductance respond when physical size of the TSV and material property of the silicon substrate change.

Table 3.2
TSV Design Parameter Impact on *RLGC* elements

	↑ t_{ox}	↑ P_{TSV}	↑ h_{TSV}	↑ d_{TSV}	↑ ρ_{Si}
R_{TSV}	↑	↑	↑	↓	↑
L_{TSV}	↑	↑	↑	↓	↓
G_{TSV}	↓	↓	↑	↑	↓
C_{TSV}	↓	↓	↑	↑	↓

Note: Increase and decrease of design parameters are denoted by direction of arrow.

In summary, the electrical properties (e.g. *RLGC* elements) of the power grid and TSV models were analyzed to mainly control the inductive, resistive and capacitive effects. The results of the parametric study were used to build TSV-based PDN models. A summary of the overall electrical behavior of the TSV are summarized in Table 3.2. We determined that the physical design parameters and RLGC elements have a considerable effect on the impedance of the power delivery network. Alternatively, the capacitance of the micro-bump (C4), redistribution layers (RDL) and other minor interconnect components were also modeled but show a lesser impact on the impedance of the power delivery network.

3.3 Modeling and Characterization of Other On-Chip Interconnects

In the previous sections, we discussed the power grid and TSV interconnect structures. In this section, we discuss the remaining interconnect components used in an on-chip power distribution network. The other on-chip interconnect components are redistribution layer (RDL) and micro-bump (C4). A redistribution layer is an interconnect layer that is used in 3D integration for the purpose of adding additional routing to connect various elements and stack differently size on-chip dies. The RDL layer is deposited on the top of the Inter-Metal Dielectric (IMD) after silicon wafer process is completed. Figure 23 shows an illustration of an RDL structure.

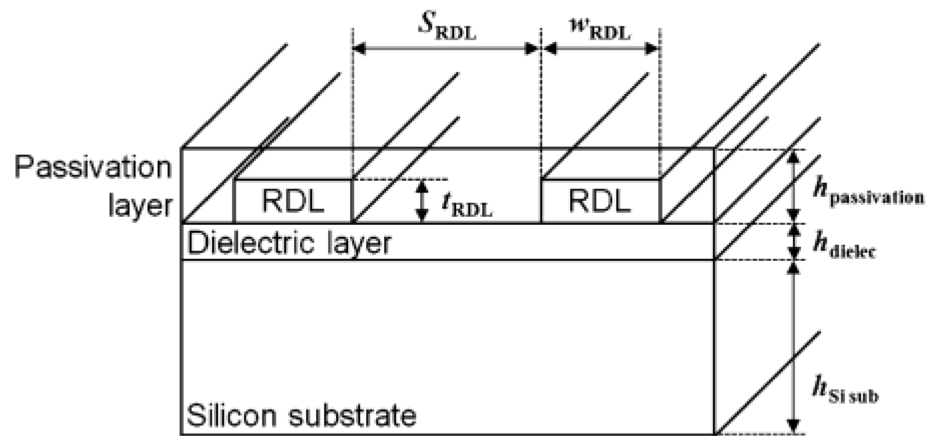


Fig. 23. Illustration of a single-ended power RDL and ground RDL on top of the dielectric layer [2.62].

A two tier stacked die with TSVs integrated vertically, uses am RDL to redistribute power-ground or signals that connects to I/Os between the two tier die. The modeling of the redistribution layer is expressed analytically using an *RLC* equation. The individual elements forming the *RLC* equation are frequency dependent. The formula used to describe the resistance of the RDL has a low and high-frequency component. The resistance of the RDL

is based on the current path as frequency increases the skin depth effect influences the resistive property. The RDL resistance is calculated by assuming that the current distribution is concentrated on the bottom of the RDL edge. The electric field between the power RDL and silicon substrate extracts the charges toward the bottom edge. If the pitch ratio between the power and ground RDLs is smaller than the height ratio between the power RDL and silicon substrate, then the current distribution is concentrated at the edge of the RDLs. Therefore the resistance of the RDL, R_{RDL} is modeled in Eqn. (3.2):

$$R_{dc,RDL} = \rho_{RDL} \frac{1}{w_{RDL} \times t_{RDL}} \tag{3.2a}$$

$$R_{ac,RDL} = \rho_{RDL} \frac{1}{w_{RDL} + \delta_{skinD,RDL}} \tag{3.2b}$$

Where the skin depth is expressed as: $\delta_{skinD,RDL} = \frac{1}{\sqrt{\pi f \mu_{RDL} \sigma_{RDL}}}$

Combining the low and high frequency resistance the total RDL resistance of a power-ground model pair is expressed:

$$R_{RDL} = \sqrt{\left(R_{dc,RDL}\right)^2 + \left(R_{ac,RDL}\right)^2} \tag{3.2c}$$

The inductance of the redistribution layer is modeled using the loop inductance model by approximating a two wire transmission line model. The expression for the RDL inductance is shown below:

$$L_{RDL} = \frac{1}{2}\left(\frac{\mu_o \mu_{r,RDL}}{2\pi} \cdot \left[2 \cdot ln\left(\frac{S_{RDL}}{t_{RDL}}\right) + \frac{1}{2}\right]\right) \tag{3.3}$$

The RDL inductance consists of self-inductance from the power metal line and ground metal line. The mutual inductance characteristic is derived from the interaction between the power

and ground metal lines. The RDL capacitance consists of the following parasitic capacitances such as the fringe capacitance, air, passivation and dielectric layer.
The expression for the RDL capacitance is taken directly from [2.62] using the capacitor model shown in Figure (24):

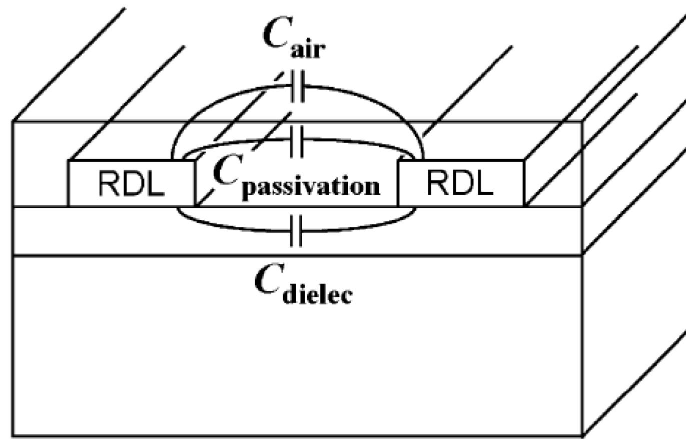


Fig. 24. RDL model with RDL capacitor components [2.62].

$$C_{air} = \varepsilon_o \varepsilon_{r,air} \frac{K\prime(k_o)}{K(k_o)} \quad \textbf{(3.4a)}$$

$$C_{passivation} = \varepsilon_o \left(\varepsilon_{r,passivation} - \varepsilon_{r,air}\right) \frac{K\prime(k_1)}{K(k_1)} \quad \textbf{(3.4b)}$$

$$C_{dielec} = \varepsilon_o \left(\varepsilon_{r,dielec} - \varepsilon_{r,passivation}\right) \frac{K\prime(k_2)}{K(k_2)} \quad \textbf{(3.4c)}$$

$$C_{RDL} = C_{air} + C_{passivation} + C_{dielec} \quad \textbf{(3.4d)}$$

The micro-bump (C4) is another on-chip interconnect element that has been analytically modeled. The expressions used to describe the micro-bump can be found in [2.62] as well. The overall impedance of the TSV-based power delivery network accounts for all elements.

3.4 Segmentation Method and Analytical Impedance Models

The modeling approached used to calculate the PDN impedance in this research is based on the segmentation method. The segmentation method and its implementation to solve hierarchical PDN models were presented in [2.68]. The segmentation method was proposed to analyze two-dimensional planar circuits and calculate the impedance, although the power delivery network may be composed of a power and ground plane of arbitrary shape.

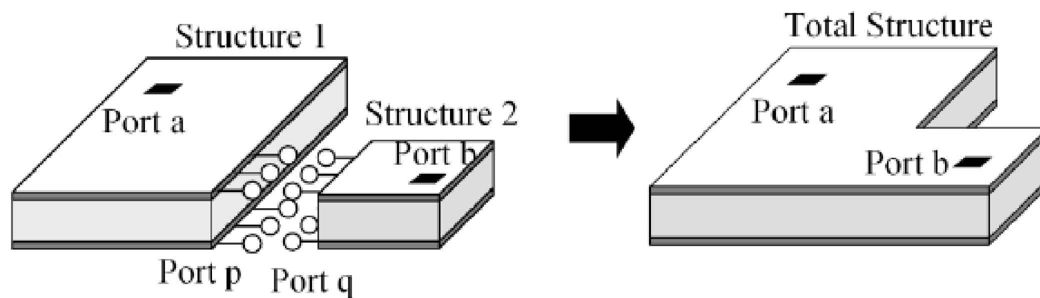


Fig. 25. A simple illustration of the segmentation method. To calculate the impedance matrix of the total structure, the total structure is decomposed into the two independent structures, e.g. structure 1 and structure 2. After calculating the impedance matrices of the two independent structures the impedance matrix of the total structure is calculated by using the segmentation method [2.68].

In Figure (25), the basic concept of segmentation method is described where two independent PDNs form a single PDN of an arbitrary shape. The two independent structures are called structure 1 and structure 2 has rectangular shaped PDNs with arbitrary dimensions. Ports such as the port a and port b are called the external ports. Meanwhile port p of structure 1 and port q of structure 2 are used for assigning interconnections (internal ports) between the two independent PDNs, referred to as the internal ports.

As shown in figure (26), the total PDN structure is comprised of the two independent, rectangular shaped structures. The PDN impedance of each independent structure can be derived with a matrix form as presented in Eqn. (3.5) and Eqn. (3.6).

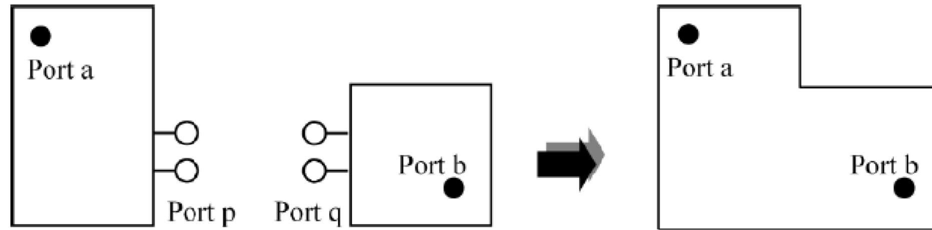


Fig. 26. Overall PDN structure composed of two independent rectangular shaped structures. The impedance matrix of the total structure can be determined using the impedance matrix of the two independent structures and with boundary conditions generated [2.68].

$$\begin{bmatrix} V_a \\ V_p \end{bmatrix} = \begin{bmatrix} Z_{aa} & Z_{ap} \\ Z_{pa} & Z_{pp} \end{bmatrix} \begin{bmatrix} I_a \\ I_p \end{bmatrix} \quad \textbf{(3.5)}$$

$$\begin{bmatrix} V_b \\ V_q \end{bmatrix} = \begin{bmatrix} Z_{bb} & Z_{bq} \\ Z_{qb} & Z_{qq} \end{bmatrix} \begin{bmatrix} I_b \\ I_q \end{bmatrix} \quad \textbf{(3.6)}$$

The two matrices in Eqn. (3.5) and Eqn. (3.6) contain four equations as presented in Eqn. (3.7a)-Eqn. (3.7d).

$$\boldsymbol{V_a = Z_{aa}I_a + Z_{ap}I_p} \quad \textbf{(3.7a)}$$

$$\boldsymbol{V_p = Z_{pa}I_a + Z_{pp}I_p} \quad \textbf{(3.7b)}$$

$$\boldsymbol{V_b = Z_{bb}I_b + Z_{bq}I_q} \quad \textbf{(3.7c)}$$

$$\boldsymbol{V_q = Z_{qb}I_b + Z_{qq}I_q} \quad \textbf{(3.7d)}$$

When the internal ports of the two structures are interconnected, the complete impedance matrix with boundary conditions to determine the total impedance matrix is calculated. The boundary condition is described in Eqn. (3.8a) and Eqn. (3.8b).

$$\boldsymbol{V_p = V_q} \quad \textbf{(3.8a)}$$

$$\boldsymbol{I_p = -I_q} \quad \textbf{(3.8b)}$$

By replacing V_q to V_p and I_q to $-I_p$ in Eqn. (3.7), a new set of equations describing the total structure is presented in Eqn. (3.9a) – Eqn. (3.9d).

$$\boldsymbol{V_a = Z_{aa}I_a + Z_{ap}I_p} \quad \textbf{(3.9a)}$$

$$\boldsymbol{V_p = Z_{pa}I_a + Z_{pp}I_p} \quad \textbf{(3.9b)}$$

$$\boldsymbol{V_b = Z_{bb}I_b - Z_{bq}I_p} \quad \textbf{(3.9c)}$$

$$\boldsymbol{V_p = Z_{qb}I_b - Z_{qq}I_p} \quad \textbf{(3.9d)}$$

Since Eqn.(3.9b) and Eqn. (3.9d) are similar, a new equation of I_p in terms of I_a and I_b can be induced by Eqn. (3.10a) – Eqn. (3.10c):

$$\boldsymbol{Z_{qb}I_b - Z_{qq}I_p = Z_{aa}I_a + Z_{ap}I_p} \quad \textbf{(3.10a)}$$

$$\boldsymbol{\left(Z_{pp} + Z_{qq}\right)I_p = -Z_{pa}I_a + Z_{qb}I_b} \quad \textbf{(3.10b)}$$

$$\boldsymbol{I_p = \left(Z_{pp} + Z_{qq}\right)^{-1}\left(-Z_{pa}I_a + Z_{qb}I_b\right)} \quad \textbf{(3.10c)}$$

By substituting Eqn. (3.10c) into Eqn. (3.9a) and Eqn. (3.9c), V_a and V_b can be induced in terms of I_a and I_b and presented in Eqn. (3.11a) and Eqn. (3.11b):

$$\boldsymbol{V_a} = \boldsymbol{Z_{aa}I_a} + \boldsymbol{Z_{ap}}\left[\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\left(-\boldsymbol{Z_{pa}I_a} + \boldsymbol{Z_{qb}I_b}\right)\right]$$

$$=\left[\boldsymbol{Z_{aa}} - \boldsymbol{Z_{ap}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{pa}}\right]\boldsymbol{I_a} + \left[\boldsymbol{Z_{ap}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{qb}}\right]\boldsymbol{I_b} \quad \textbf{(3.11a)}$$

$$\boldsymbol{V_b} = \boldsymbol{Z_{bb}I_b} + \boldsymbol{Z_{bq}}\left[\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\left(\boldsymbol{Z_{pa}I_a} - \boldsymbol{Z_{qb}I_b}\right)\right]$$

$$=\left[\boldsymbol{Z_{bq}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{pa}}\right]\boldsymbol{I_a} + \left[\boldsymbol{Z_{bb}} - \boldsymbol{Z_{bq}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{qb}}\right]\boldsymbol{I_b} \quad \textbf{(3.11b)}$$

Finally the impedance matrix of the total PDN is derived in Eqn. (3.12),

$$\begin{bmatrix}\boldsymbol{V_a}\\ \boldsymbol{V_b}\end{bmatrix} = \begin{bmatrix}\boldsymbol{Z_{aa}} - \boldsymbol{Z_{ap}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{pa}} & \boldsymbol{Z_{ap}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{qb}}\\ \boldsymbol{Z_{bq}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{pa}} & \boldsymbol{Z_{bb}} - \boldsymbol{Z_{bq}}\left(\boldsymbol{Z_{pp}} + \boldsymbol{Z_{qq}}\right)^{-1}\boldsymbol{Z_{qb}}\end{bmatrix}\begin{bmatrix}\boldsymbol{I_a}\\ \boldsymbol{I_b}\end{bmatrix}$$

$$= \begin{bmatrix}\boldsymbol{Z'_{aa}} & \boldsymbol{Z_{ab}}\\ \boldsymbol{Z_{ba}} & \boldsymbol{Z'_{bb}}\end{bmatrix}\begin{bmatrix}\boldsymbol{I_a}\\ \boldsymbol{I_b}\end{bmatrix} \quad \textbf{(3.12)}$$

Consequently, the impedance matrix of the total structure can be derived by using the impedance matrices of the independent structures and the segmentation method. In this research study, the segmentation method is used to calculate the impedance of a two-tier TSV-based PDN model.

Chapter Summary

In summary, this chapter described the physical dimensions of TSV-based on-chip interconnect structures. A parametric simulation study was performed on on-chip power grid (BEOL) structures. We analyzed the change in physical dimensions of the power grid structure and its effect and impact on the parasitic elements (*RLGC*). We specifically observed the resistance and inductance of the power grid structure for local-level metal interconnects to reduce the *RC*-delay issue and simultaneous switching noise *L*di/dt. We then performed a similar study on a pair of P/G TSV structure. We presented several plots of the resistance, inductance and capacitance of the TSV structure. We also presented several analytical expressions characterizing the RLGC elements which can be used to generate an approximation of the electrical characteristics. We summarized the electrical characteristics of the TSV by presenting a table that shows how physical sizing and material property of the silicon substrate influence the passive elements of the RLGC for a P/G TSV pair. Other interconnect models were briefly discussed e.g. redistribution layer (RDL) and micro-bump. Finally, we conclude the chapter presenting the methodology used to calculate the impedance of an on-chip PDN and its application to solving the impedance of a TSV-based PDN.

CHAPTER IV

Case-study: Various TSV-based PDN Stacking Topologies

The design and development of power delivery networks is expected to be a major challenge as power and current transient levels increase with corresponding decrease in power supply voltage and noise margin. As more devices are integrated into a single chip-package, delivering clean power to fast switching devices become very critical. With the threat of gross voltage fluctuations and droop at power and ground (P/G) terminals, accurate PDN modeling methodologies and estimation techniques are necessary to meet the rigid constraints. With tier-to-tier (T2T) PDN connections using through silicon via (TSV) technology, one can explore different on-chip stacking combination [4.1]. However, very little work on the different on-die stacking topologies and effect on PDN have not been studied as much except for in [2.69]. In this chapter, we fully explore how various on-die stacking topologies affect the on-chip PDN impedance. Previous investigations in PDN modeling included scalable electrical models derived from physical dimensions of on-chip interconnect structures, the effects of P/G TSV arrangement, the number of paired P/G TSVs used per layer and a detailed approach to calculate and analyze the impedances of multi-stack PDNs using segmentation method can all be found in [2.60], [2.62],and [4.2].

The various PDN stacking types are described in details in this chapter. We discuss three different stacking topologies: (1) face-to-back (F2B), (2) face-to-face (F2F) and back-to-back (B2B). These are the possible combinations that one can realize with TSV technology. Throughout this chapter we use the terms “face” and “back” to describe the active device layers and substrate layer respectively. Furthermore, in this chapter, the segmentation method used in [2.60] is applied here. The impedance properties of different

stacking topologies are estimated and analyzed throughout this study. The sections of this chapter include detail discussions in (1) on-die stacking topologies, (2) on-chip decoupling solutions for TSV-based PDNs, (3) impedance estimation using analytical models and lastly (4) case-study comparative analysis of various TSV-based PDNs.

4.1 On-Chip Stacking Topologies: F2F, F2B and B2B

In three-dimensional (3-D) stacking, dies can be bonded using different bonding approaches. In this section, we briefly discuss the different chip stacking options available in 3-D IC. Delivering power to the layers requires adequate power and ground TSVs. In order to supply clean power to the TSV-based 3-D structure, we assume that at least 30% of the available TSV must be reserved for power and ground to avoid significant voltage swings during operation. The PND impedance requirements are governed by a number of factors from physical size of interconnect to the type of multi-stack bonding method used.

A. Face-to-back (F2B) is a method that is based on bonding the "face" (e.g. active device layer) of chip layer-1 to the substrate layer (e.g. back) of chip layer-2. This is illustrated in Figure (27). The height of the TSV in chip layer-2, the topmost die, is depended on the substrate thickness. The substrate thickness can directly impact the number of possible interconnects between the two on-chip layers [4.3]. This in turn can affect the PDN impedance. In F2B topology, multiple tiers of transistor dies can be stacked. A large number of TSVs are inserted in F2B topology which increases signal bandwidth. However, this is contrary with face-to-face topology. In F2B topology, TSVs are etched through the back (substrate-layer) of the die and the etching process has low resolution compared to the face-to-face bonding approach.

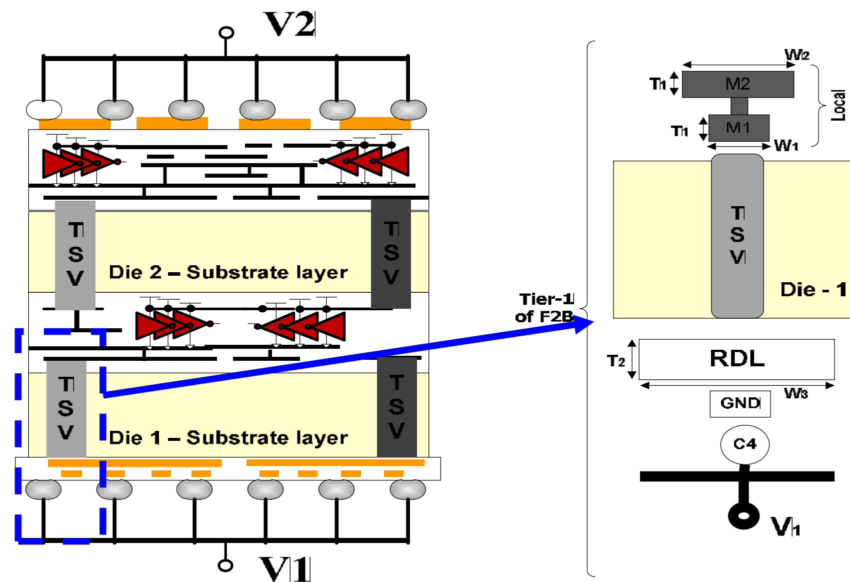


Fig. 27. Face-to-back (F2B) chip stacking.

B. Face-to-face (F2F) assembly focuses on combining the face of both chip layer-1 and chip layer-2 directly. This is shown in Figure (28). An advantage of F2F assembly is the ability to split TSVs between interconnections. Thus, TSVs on one chip layer is sufficient in a F2F assembly scheme. The active layers of the two dies are facing each other in a Face-to-Face bonding methodology. Even though F2F bonding allows only to be bonded but cannot provide higher TSV density due to similarly of synthesizing on die interconnects.

C. Back-to-back (B2B) approach is a process of combining the substrate layers of chip-1 with chip-2. Figure (29) illustrates this 3-D stacking configuration. The active device layers between both chips are at its furthest distance. The substrate thickness between both chips in a B2B configuration will determine the length of the TSVs. A long TSV height is indicative of a longer path to deliver power and perhaps higher impedance noise is encountered.

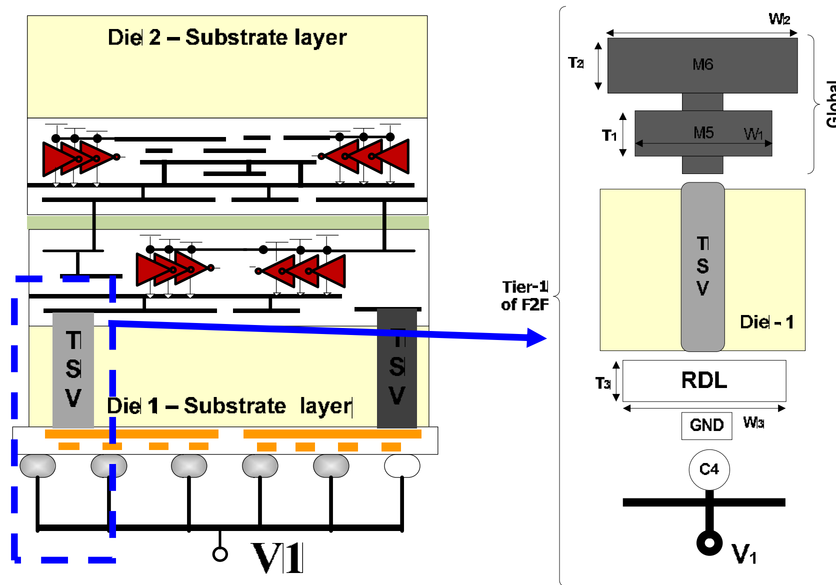


Fig. 28. Face-to-face (F2F) chip stacking.

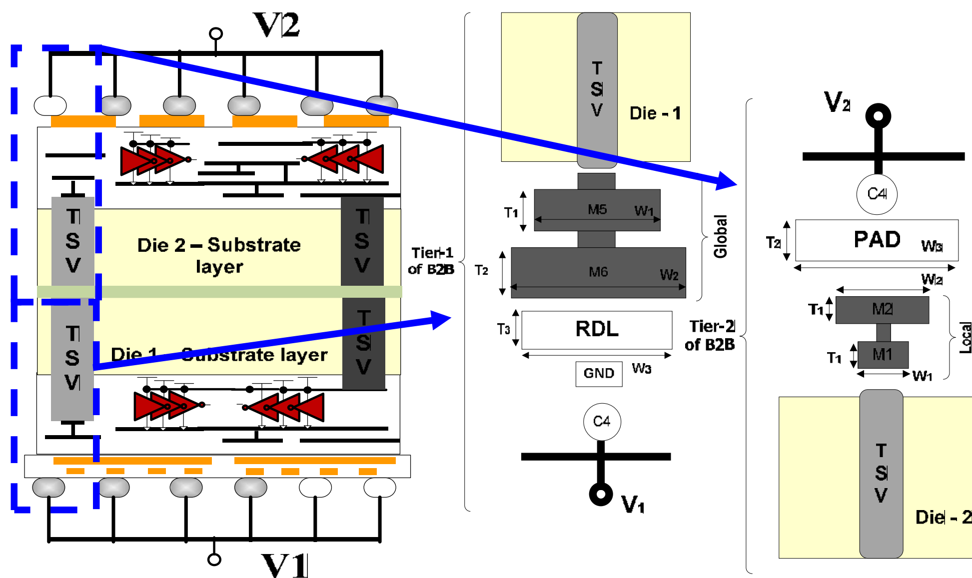


Fig. 29. Back-to-back (B2B) chip stacking.

The interconnect wire scheme implemented for each stacking topology is distinct. This is illustrated in figures (30) and (31). In Fig. 30(a), we show the interconnect arrangement for F2B which uses the wire interconnects at the local-level. The wire widths at the local-level are smaller with respect to the wire widths at the intermediate- and global-levels. The F2F approach uses interconnect wires at the global-level. The interconnect wiring at the global-, intermediate- and local-levels present different physical dimensions and this results in distinctive *RLGC* parasitic properties. The B2B methodology shows tier-1 and tier-2 interconnects arrangement. B2B was modeled to use both global- and local-level interconnect wiring.

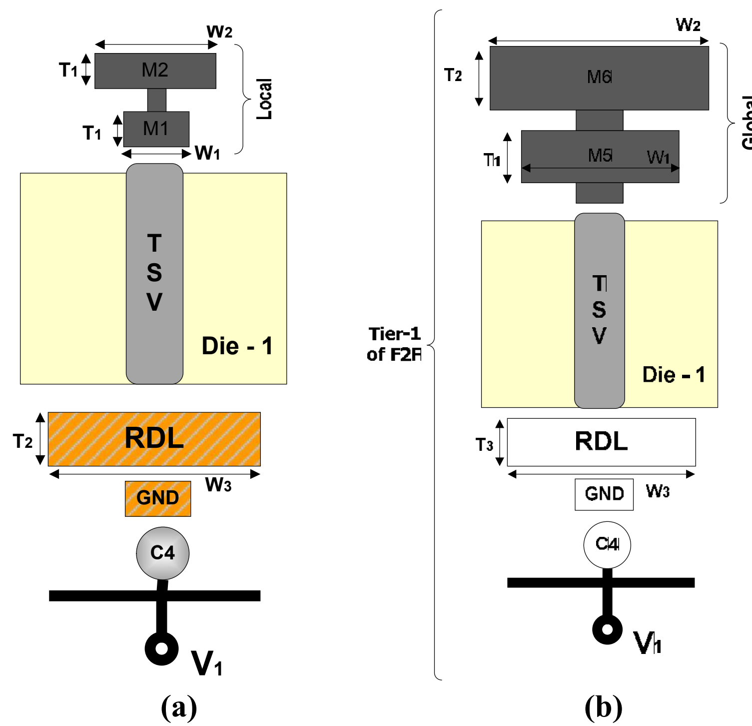


Fig. 30. On-chip interconnect including RDL, micro-bump, and BEOL (power grid) and TSV. The arrangement of the interconnects using via-first approach for (a) F2B and (b) B2B topologies. The F2B topology showing local interconnect levels and F2F using global.

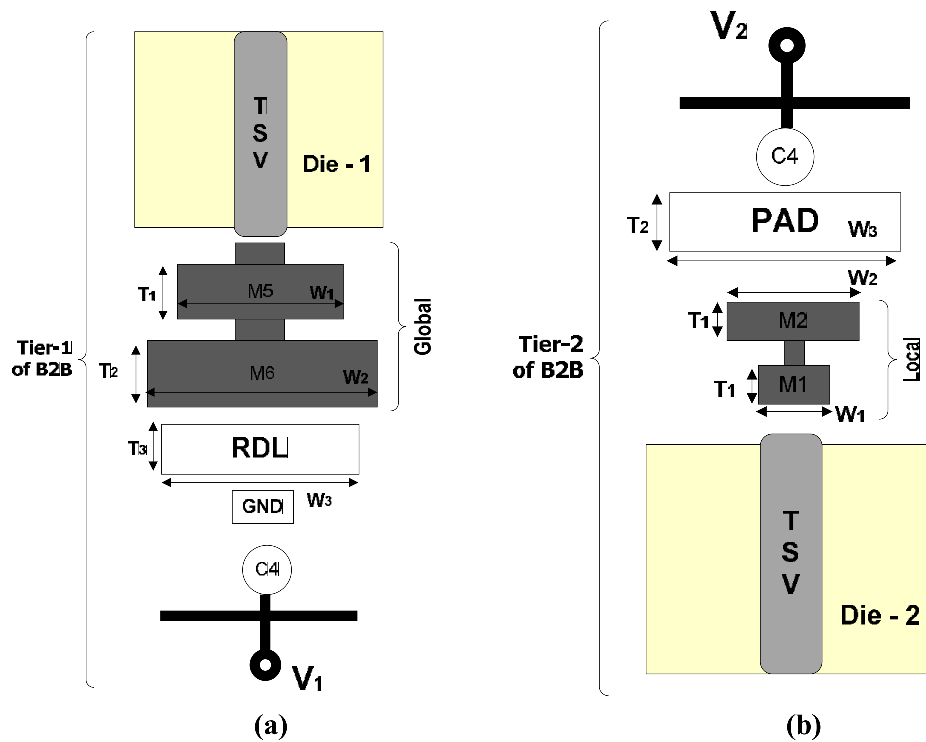


Fig. 31. On-chip interconnect including RDL, micro-bump, and BEOL (power grid) and TSV for a two-tier back-to-back topology. The combination of global and local interconnects.

The arrangement of interconnects (global, intermediate and/ or local) in F2B, F2F and B2B stacking topology is dependent on the device wafer fabrication process. Figures (30) and (31) show metal interconnects that include redistribution layers (RDLs), micro-bumps (C4) and metal layers of various levels. In the TSV process there are three distinct ways TSVs are inserted into the wafer fabrication process; they are denoted as (1) “Via-first” – fabrication of TSVs before the silicon or front-end of line (FEOL) devices are fabricated into the process, (2) “Via-middle” – fabrication of TSVs after the silicon FEOL devices are fabricated before the BEOL interconnect process and (3) “Via-last” – fabrication of TSVs after or in the middle of the silicon BEOL interconnect process. The fabrication process consist of three basic steps, namely wafer thinning, TSV etching and filling, and finally tier-bonding. The sequence of the TSV fabrication steps can occur in any order. Given the

stacking style used, the inter-chip connection can be used to construct multiple tiers as demonstrated in figures (30) and (31). Power delivery in three-dimensional integrated systems is a challenging task especially when delivering large current demands to stacked devices. The different stacking orientations will generate different impedance characteristics. The focus of this chapter is on the different impedance characteristics of the different stacking orientation. The chapter also provides a quantitative comparative analysis of the amount of noise estimated for each stacking topology. In the next section, we cover on-chip decoupling capacitors.

4.2 On-Chip Decoupling Solution for TSV-based PDNs

The power distribution network is made up of a power supply, a power load, power planes and other physical interconnect structures. To ensure a small fluctuation in the power distribution network under critical current load, a power distribution must maintain a small impedance path for a given frequency range of interestest. The power integrity of the power delivery network is based on the network impedance. The impedance property in the network will determine the power supply noise level.

Decoupling capacitors are frequently utilized to manage or eliminate the power supply noise at the package and on-chip levels. The operation of a particular integrated circuit has to be ensured according to the design specifications. Decoupling capacitors are generally used to help meet those design specs and lower the impedance properties of the power distribution system. Many different types of decoupling capacitors contribute to the overall power integrity of a power distribution system. There are bulk and ceramic decoupling capacitors for the voltage regulator module (VRM) and board level. At the package level, ceramic capacitors are mainly used. At the on-chip level, metal-oxide-semiconductor (MOS), deep trench and metal-insulator-metal (MIM) capacitors are used primarily. There are also intrinsic decoupling capacitance which is a type of parasitic capacitance that exist

between the power and ground terminals within an on-chip structure. This chapter focuses mainly on the on-chip decoupling capacitance used to to construct TSV-based PDN designs. On-chip decaps are realizedd in many ways depending on the fabrication process for which metal layers and devices are are used to implement on-chip capacitors. In the next section, we cover the different analytical models used to characterize on-chip MOS and MIM decoupling capacitors.

4.2.1 Modeling MOS Decoupling capacitors

A MOS capacitor is a certain type of capacitor structure fabricated in CMOS integrated circuits (ICs) where the top metal plate is referred to as the gate, the bottom metal plate forms as an ohmic contact is referred to as the bulk-substrate contact and the oxide layer separating the gate-metal from the bulk-substrate. The MOS capacitor can be implemented as a nMOS, pMOS and CMOS decaps. In digital circuits, CMOS decaps are commonly used within standard cells. Figure (32) shows a description of three different decap configuration models and they are listed as follows: nMOS, pMOS, and CMOS decaps.

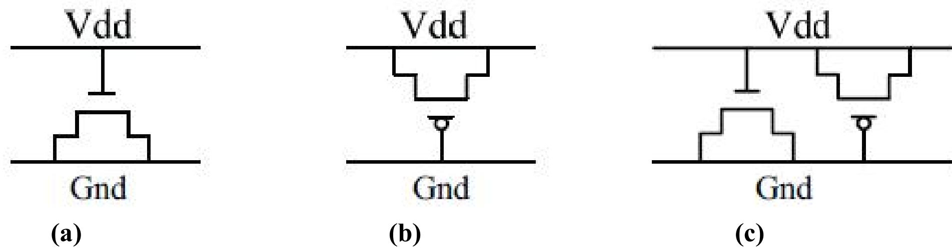


Fig. 32. Configurations for (a) nMOS decap, (b) pMOS decap and (c) CMOS decap.

A circuit equivalent of the general model decap is shown in Figure (33). The model consists of fringe capacitive component, C_{fringe}, coupling capacitive component, $C_{coupling}$, the area capacitance, C_A, leakage resistance, $R_{leakage}$, equivalent series resistance, ESR, and equivalent series inductance, ESL. The ESR is an equivalent resistance based on the conducting electrode plates. The presence of additional inductance, ESL, can further

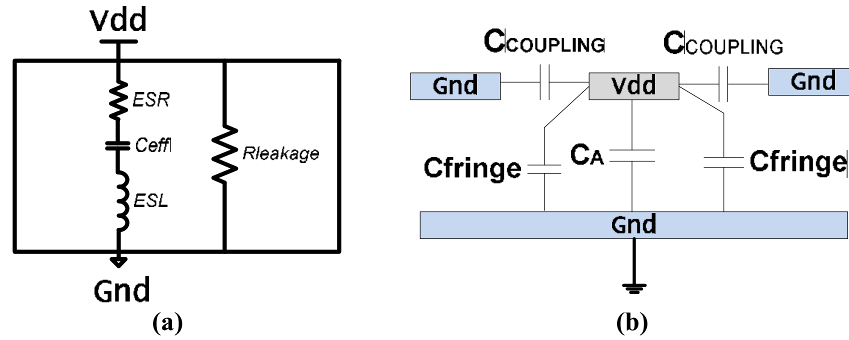


Fig. 33. (a) Equivalent circuit model and (b) capacitive component of MOS parallel plate decap.

increase the impedance of the decap. The ESL of on-chip decaps is small and its effects are generally neglected from the MOS decap impedance formula. The capacitive component, in Figure 33(a), C_{eff}, is composed of the coupling, fringe and area capacitance components. The decap impedance model, Z_{MOS}, is given by Eqn. (4.1):

$$Z_{MOS} = \frac{R_{leakage}\left(ESR + \frac{1}{j \cdot \omega \cdot C_{eff}}\right)}{R_{leakage} + ESR + \frac{1}{j \cdot \omega \cdot C_{eff}}} \quad \textbf{(4.1a)}$$

At frequencies above 100 MHz, the MOS decap can be simplified to:

$$Z_{MOS} \approx \frac{R_{leakage}}{R_{leakage} + ESR}\left(ESR + \frac{1}{j \cdot \omega \cdot C_{eff}}\right) \quad \textbf{(4.1b)}$$

MOS decaps with the gate terminal made of polysilicon material has a thin oxide layer that causes leakage current to pass through. Because the leakage resistance, $R_{leakage}$ >> ESR, the MOS decap impedance of Eqn. (4.1b) is simplified to:

$$Z_{MOS} \approx ESR + \frac{1}{J \cdot \omega \cdot C_{eff}} \quad \textbf{(4.2)}$$

The impedance decap formula for an nmos and pmos are essentially the same when using the simplified Eqn. (4.2). The primary benefit of the MOS capacitors is its fabrication compatibility with with CMOS technology. MOS capacitors offer a cost-effective high capacitance density on-chip decouplng solution [4.4]. The performance of the MOS capacitors is limited at high frequencies because of the large diffusion-to-substrate parasitic capacitance. With technology scaling down, the leakage currents of MOS capacitors increases considerably. High leakage current is the main issue with MOS capacitors.

4.2.2 Modeling MIM Decoupling capacitors

Metal-insulator-metal (MIM) capacitors are typically used in mixed signal and RF applications for noise decoupling purposes. We extend its usage into 3-D IC power integrity applications. There are various types of MIM capacitors which are represented as trench and planar structures proposed in [4.5] for copper back-end-of-line (BEOL). Here we use a physically-based frequency-dependent compact analytical MIM capacitor model based on planar structure. The decap model is expressed as a complex impedance formula [4.6] and a description of the planar capacitor structure is shown in Figure (34),

$$Z_{MIM}(W,L,f) \cong \frac{\rho_{bmp} \cdot t_{bmp} + \rho_{tmp} \cdot t_{tmp}}{W \cdot L} + \frac{L}{3 \cdot W} \cdot \left(\frac{\rho_{bmp}}{t_{bmp}} + \frac{\rho_{tmp}}{t_{tmp}} \right) + j \frac{t_{ox}}{2 \cdot \pi \cdot f \cdot \varepsilon_r \cdot W \cdot L} \quad \textbf{(4.3)}$$

The deposisted dielectric layer material used between the two metal layers is silicon nitride (Si_3N_4). The capacitance can be increased by lowering the dielectric thickness but this is at the risk of increased leakage current which is highly undesirable. MIM capacitors with a capacitance density approximately two times greater than the capacitance of MOS capacitors have been fabricated [4.7]. The complex impedance Eqn. (4.3) is expressed in real and imaginary parts where the real term represents the total capacitance. Z_{MIM} is a function of

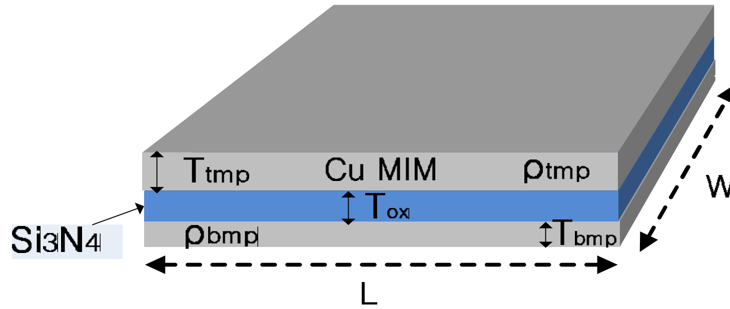


Fig. 34. Simple planar MIM capacitor model is represented. The geometrical parameters and dielectric material property, Si_3N_4, is also included in the model.

metal width, W, metal length, L, and the frequency, f. The remaining parameters are denoted as follows: ε_r is the relative dielectric constant, t_{tmp} is the top metal plate thickness, ρ_{tmp} is the resistivity of the top metal plate, $t_{bmp}$is the bottom metal plate thickness, ρ_{bmp} is the resistivity of the bottom metal plate and t_{ox} is the dielectric insulator layer thickness. Now that we have a closed-form expression for a planar MIM capacitor, the formula can be embedded into an impedance matrix form and solved. We employ the segmentation methd [2.69],[4.2] because of its fast computation time and ability to accurately characterize the impedance network of multi-level TSV based PDNs. The impedance matrix of the power delivery system contains pre-defined port locations of decoupling capacitors where voltage and current vectors are considered locations of interest. The voltages and currents are written in a block matrix form Eqn. (4.4). The terms $\widetilde{v_1}$ and $\widetilde{i_1}$ represent the voltage and current vectors corresponding to locations containing observation ports. The other terms $\widetilde{v_2}$ and $\widetilde{i_2}$, represent the voltage and current locations corresponding to the pre-defined port locations for on-chip decaps. Hence, the pre-defined port locations are where the MIM capacitor models, Z_{MIM}, are placed. The elements inside the matrix described the self-impedance, $\widetilde{Z_{11}}$ and $\widetilde{Z_{22}}$, and the remaining elements $\widetilde{Z_{12}}$ and $\widetilde{Z_{21}}$ are the transfer impedance. We characterized the electrical properties of the network by combining Eqn. (4.4) and (4.5) to get a new impedance matrix in Eqn. (4.6). The impedance matrix of MIM decoupling capacitor with diagonal form is expressed in Eq. (4.5) where the ith diagonal element is the impedance matrix of the decoupling capacitor. A zero entry for an element along the diagonal indicates

that there isn't a port location for decoupling capacitor or simply no decoupling capacitor placed at that location:

$$\begin{bmatrix} \widetilde{V_1} \\ \widetilde{V_2} \end{bmatrix} = \begin{bmatrix} \widetilde{Z_{11}} & \widetilde{Z_{12}} \\ \widetilde{Z_{21}} & \widetilde{Z_{22}} \end{bmatrix} \begin{bmatrix} \widetilde{I_1} \\ \widetilde{I_2} \end{bmatrix} \quad \textbf{(4.4)}$$

$$\widetilde{V_2} = \sum a_{ii} \vec{Z}_{ii} = diag(Z_{MIM})_{m \times m} \cdot \tilde{I}_2 \quad \textbf{(4.5)}$$

Where Z_{MIM} is:

$$Z_{MIM} = \begin{bmatrix} Z_{MIM,11} & 0 & 0 & 0 & 0 \\ 0 & Z_{MIM,22} & 0 & 0 & 0 \\ 0 & 0 & \cdot & 0 & 0 \\ 0 & 0 & 0 & \cdot & 0 \\ 0 & 0 & 0 & 0 & Z_{MIM,ii} \end{bmatrix}$$

With Eqn. (4.6) below, one can solve for the power delivery network once the self-impedance and transfer impedance of the network is known.

$$Z_{n \times n} = \tilde{Z}_{11} - \tilde{Z}_{12} \cdot \left(diag(Z_{MIM})_{ii} + \tilde{Z}_{22} \right)^{-1} \cdot \tilde{Z}_{21} \quad \textbf{(4.6)}$$

To this end, each and every on-chip PDN interconnect component that we discussed so far has been discussed individually. So far, the analytical models for the power-ground TSV structure, BEOL power grid metal structures and planar MIM decoupling capacitors have been discussed.

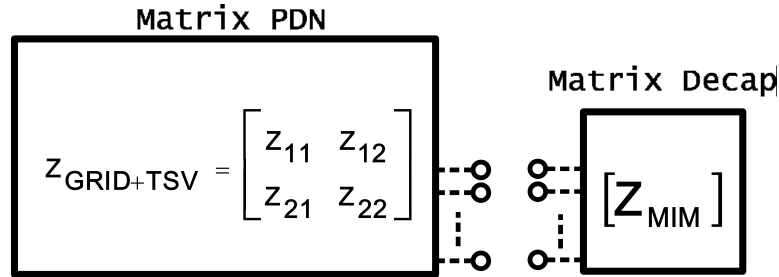


Fig. 35. Illustration of Eqn. (4.6) using impedance matrices of PDN and decap model.

Figure (35) shows a simple illustration of segmentation method being used to combine the TSV-based PDN model and on-chip decoupling capacitors i.e. MIM decap are used to reduce the impedance effects. In the next section, we estimate the impedance properties using the analytical models of TSV, power-grid and other on-chip interconnect structures. There are several analytical scalable TSV and power grid models in literature today but they have become too complex and countless expressions to use for analyzing the electrical behaviors of multi-stack PDNs. In previous studies like in [2.69], commercially available full-wave tools and segmentation method was used to build an entire multi-stack PDN. In this work we used simple equivalent circuit compact models to construct and analyze an entire multi-stack TSV-based PDN module. This is discussed further in section 4.3. We present two types of compact analytical models; one for the interdigitated power grid and the other for the P/G TSV structures. The formulas can be used to model global and local-level BEOL interconnects because in essence the formulas are scalable. Furthermore, the unit cells are defined based on parametric study to keep the *RLGC* parasitics low as long as the physical size are within a certain range of values.

4.3 Case-Study: Impedance of Various TSV-based PDNs Topologies

In this section, we analyze the effects of various on-die stacking topologies. We use the analytical formulas from the previous section and segmentation method to calculate the impedance curves of the TSV-based PDN system. As mentioned in previous sections, the 3-D arrangement of two silicon dies can be formed as Face-to-Face, Face-to-Back and lastly Back-to-Back using through-silicon vias (TSVs). We compare the impedance curve profile of each stacking topology to determine which PDN topology is noisy.

The TSV-based PDN model was built using the complex impedance formulas mentioned above for the different stacking configurations. Each PDN system consists of two separate chips with micro-bumps and RDL models. Pre-defined ports are placed at the corner and center positions of the 1st and 2nd tier chips. Also, observation ports are placed near the corner and center positions of the 1st and 2nd tier chips. The on-die interconnects were arranged according to their respective on-die stacking configuration. Figure (36) shows an example of a F2B block diagram model corresponding to the on-die interconnects.

Table 4.1

ON-DIE INTERCONNECT VALUE OF UNIT CELL PDN

σ_{Si-Sub}	POWER GRID	TSV	RDL	μBUMP
10 S/m	$L = 200\mu m$	$P_{TSV} = 120\mu m$	$L = 80\mu m$	$D = 20\mu m$
	$W = 25\mu m$	$H_{TSV} = 60\mu m$	$W = 15\mu m$	$H = 15.4\mu m$
	$T = 0.2\mu m$	$D_{TSV} = 10\mu m$	$T = 6\mu m$	
	$P = 120\mu m$	$t_{ox} = 0.5\mu m$	$P = 120\mu m$	

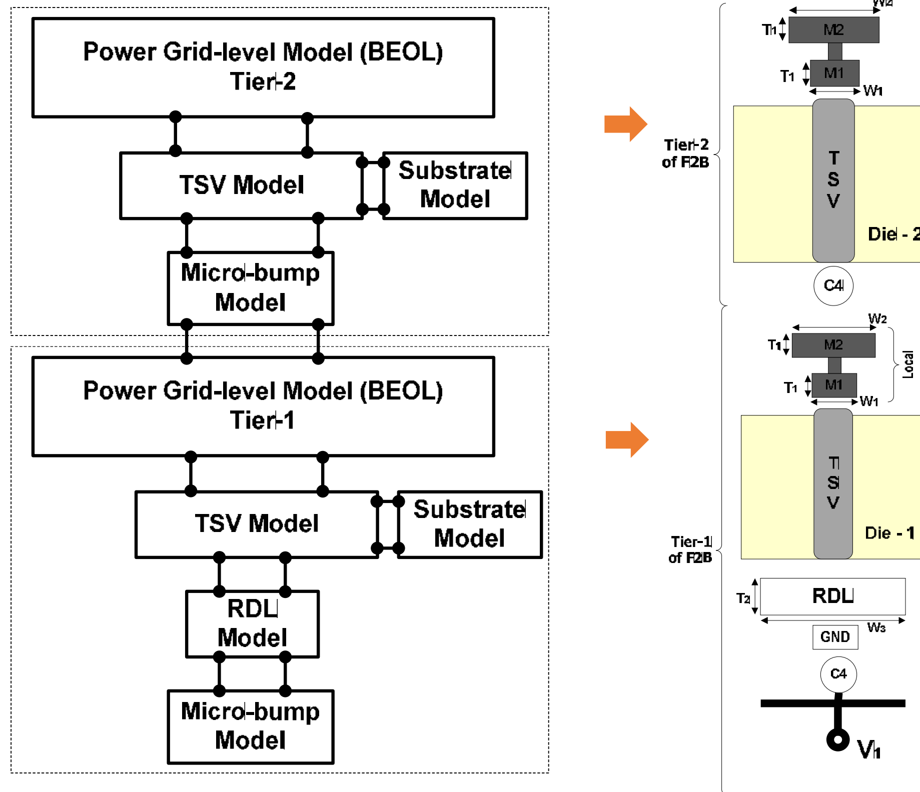


Fig. 36. F2B on-die block model and interconnect arrangement.

Table 4.1 shows a list of physical and material values used to construct a TSV-based PDN unit cell model. For the power grid structure, one can employ the information from a 0.18μm 6-metal CMOS technology. The BEOL metal layer thickness used is 200nm, metal length 200-μm, metal width and metal pitch between power-power line being 25-μm and 120-μm respectively. The dielectric thickness material used is 800nm with a dielectric constant of 4.1. Also the silicon substrate material is fixed at 10 S/m. The die size is $2mm \times 2mm$.

The numerical properties of the impedance matrices and the number of internal ports used for the interconnections. The number in the box corresponds to the size of the impedance matrix. The numbers are broken down as follows according to Figure (37): the first number in the box represent port in the x-direction, the second number in the box represent port in the y-direction and the number of frequency samples. The third number in the box represents fixed frequency sample points ~ 350. The frequency range goes from 0.1

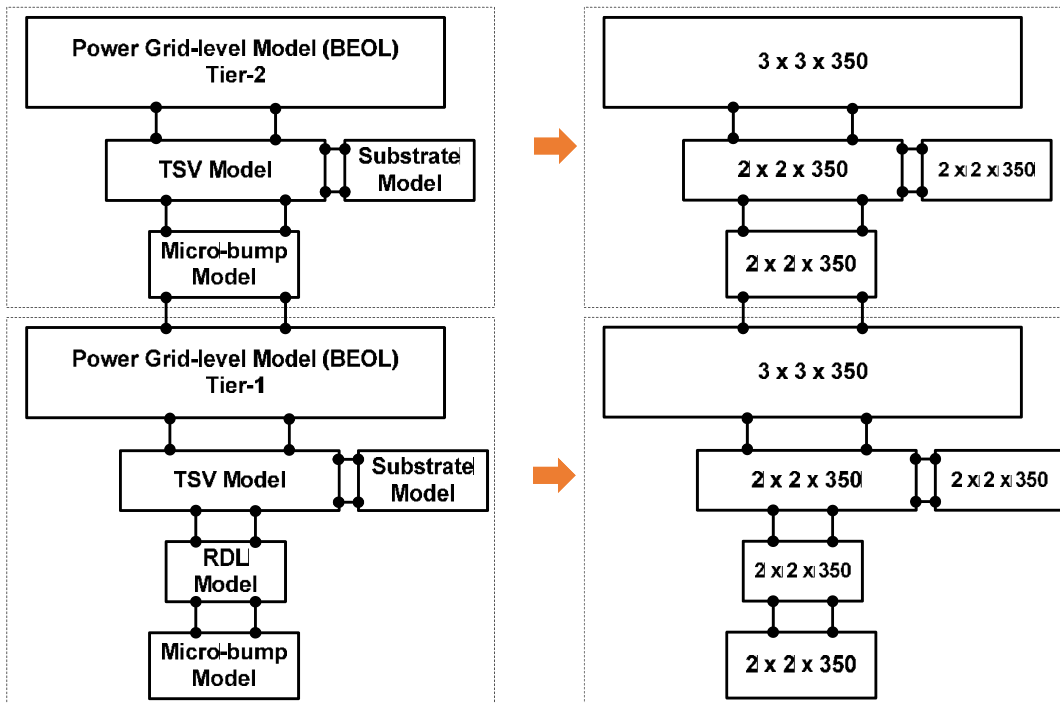


Fig. 37. The numerical properties of impedance matrices and the number of internal ports used for the interconnections.

GHz to 20 GHz on a log scale. The number of internal ports for the power-grid model is 170 internal ports, TSV model has 2 internal ports, micro-bump 2 internal ports and RDL has 2. To estimate the impedance properties in the TSV-based PDN model, the segmentation method is employed. This is a simple and fast methodology to estimate the PDN impedance. When two or more different on-die TSV-based PDNs are merged together, they form a single hierarchical PDN as a new TSV-based PDN model. The two TSV-based PDN models generates a electromagnetic coupling effect.

The impedance result for two-tier TSV-based PDN system for the different stacking topologies is shown in Figure (38). In Figure (38), the solid black line represents the self-impedance, Z_{11}, of F2B, dashed grey line represent the PDN impedance of B2B and finally the dotted grey line describes the PDN impedance of F2F. The impedance curves contain upper peaks generated between 3 – 15 GHz. The upper peaks suggest a considerable amount of inductance in the network. The differences in impedance curves is due to the different

stacking orientations (e.g. F2F, F2B and interconnect arrangement), and PDN loop created by P/G TSV pair. The impedance variation shows the B2B has a higher PDN impedance curve at 100 MHz relative to the other stacking orientations. However, between 3 – 8 GHz the upper peaks for F2F and B2B are observed. The frequency domain analysis of the inductance is dominant.

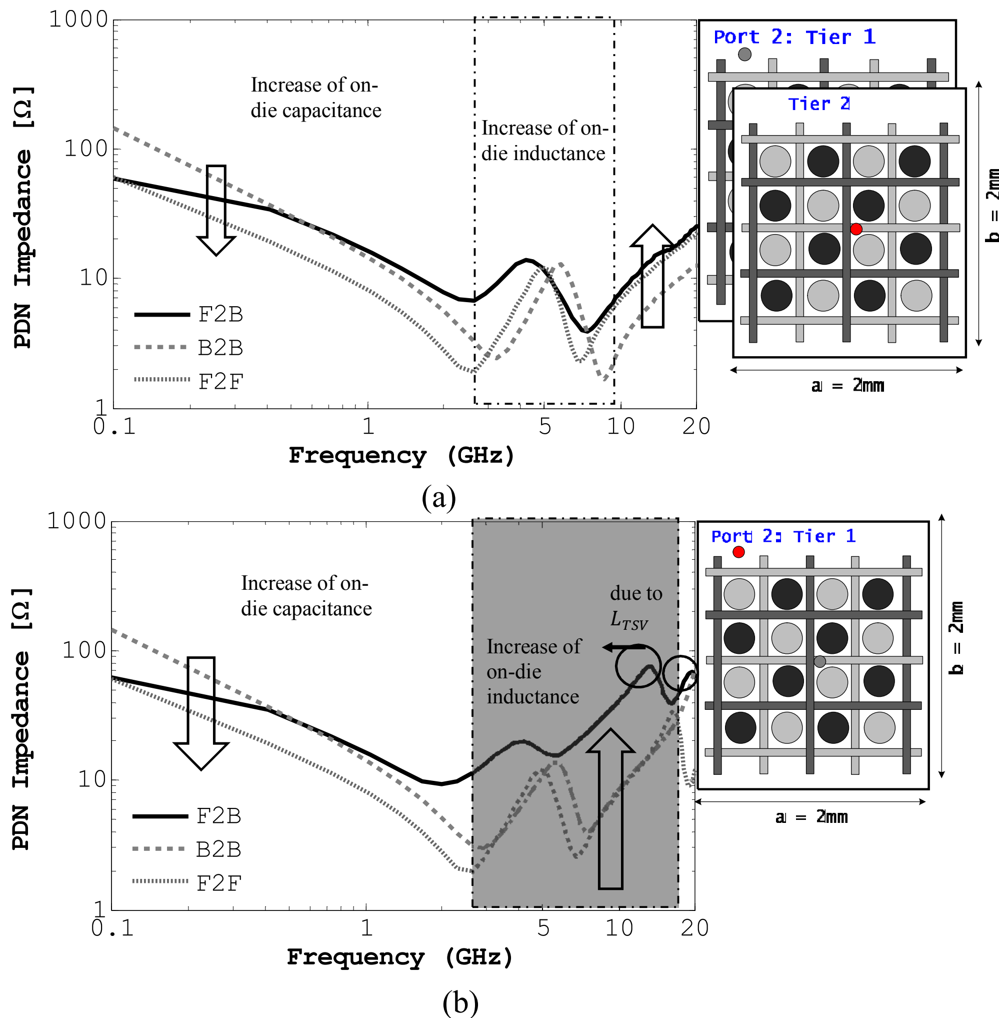


Fig. 38. TSV-based PDN impedance curves of two stacked PDN without decoupling capacitors (a) center location red dot and (b) corner location red dot.

The inductance generated in the PDN is primarily due to the inductive nature of the P/G TSV pair and the power-grid structure. In F2F topology, TSVs can be inserted into and less substrate noise respectively than F2B topology where TSV penetrate both substrate layers [4.8].The port locations are located at the corner of PDN tier-1 and center of PDN tier-2; this is indicated by the red dot placed on the TSV-based power grid structure. The TSV structures are uniformly distributed throughout the power grid structure. The RDL model used in F2B, B2B and F2F topology are located only on tier-1. The anti-resonant peaks that appear in Figure 38(b) of F2B are due to the inductive characteristics of the TSV structure. Figure 38(b) shows the simulated impedance observed at the corner location with resonant mode behavior in F2B and B2B PDN stacking topologies. The resonant mode and high impedance curve for F2B and B2B are due to the penetration of P/G TSVs in a noisy substrate.

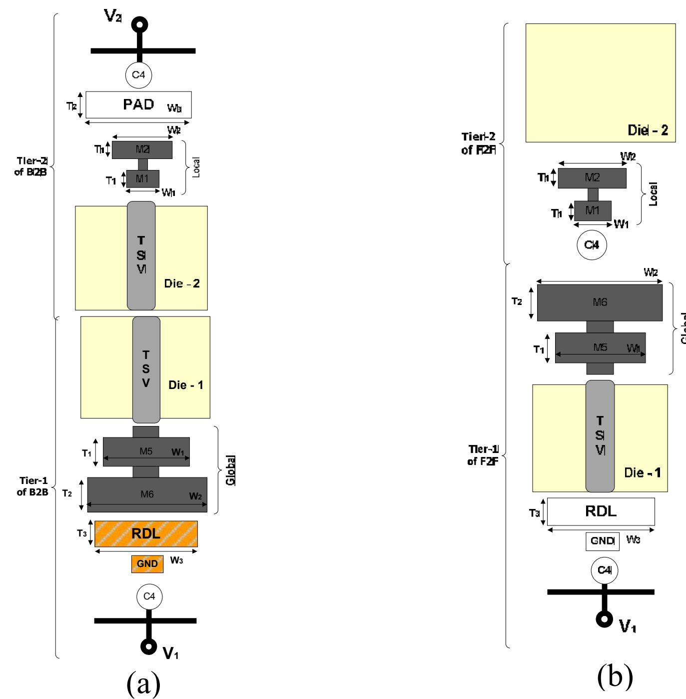


Fig. 39. Interconnect arrangement for (a) B2B topology and (b) F2F topology

The P/G TSVs does not penetrate the substrate in F2F PDN stacking topology. In other words, F2F has a lower impedance property and lower PDN loop inductance at the corner and center locations because the TSVs does not pass thru substrate layer. The anti-resonant peaks become a major issue of on-chip power integrity for TSV-based PDN design if the supply current amplitude level coupled with the impedance amplitude will cause a significant voltage drop (dip) on the power supply line. To avoid these issues, we employ on-chip decoupling capacitors to lower the impedance curve. The analysis is discussed in details in the next section.

In this section, the impedance curve results for the three stacking topologies with on-chip decoupling capacitors are calculated up to 20 GHz. Figure (41) shows a 3x2 arrangement of plots and in each plot there are three distinctive curves that show the impedance response as a result of decoupling capacitor implementation. Figure 41(a) represents the impedance response for F2F topology with and without the use of decaps. The set of plots in the first column of Figure 41((a), (c) and (e)) are the impedances observed from the center position of the PDN. The second column ((b), (d) and (f)) are the impedances observed from the corner position. The impedance curve showing upper peaks (or parallel resonant) is the result of combining two or more TSV-based PDNs and the PDN loop inductance generated by P/G TSV pairs in the network. As more PDN dies are stacked vertically on top of each other, upper-peaks or mode resonances are produced and shifted towards lower frequencies. To prevent this behavior embedded on-chip decoupling models are implemented. We also utilize MOS capacitor models as part of the on-chip decaps solution.

We begin our analysis with the impedance curve of F2F topology shown in Figure 41(a) and (b). The goal here is to eliminate or shift the parallel resonances (e.g. upper peaks). The PDN inductance loop ($L_{ON-CHIP}$) is generated from the P/G TSV pairs (L_{TSV}) and from PDN interconnects in die-1 and die-2 ($L_{INTRCNT}$). F2F PDN stacking does not contain P/G TSV pairs in die-2. Since the P/G TSVs are the primary contributor of on-chip inductance, the on-chip inductance present in F2F topology is relatively lower than in F2B

and B2B topologies. This is illustrated in the results of Figure (41). The solid black line represents the impedance curve without the implementation of decoupling capacitor models. The solid black line represents no decap, the dash-dotted grey line represents the impedance curve using MIM-type decaps and the solid grey line represents the impedance curve using MOS-type decaps. The decap values range from $0.062\, fF/\mu m^2$ - $5.325\, fF/\mu m^2$ between MOS and MIM decap models. A total of 16 decap models (4×4) were evenly placed across the PDN as depicted in Figure (40).

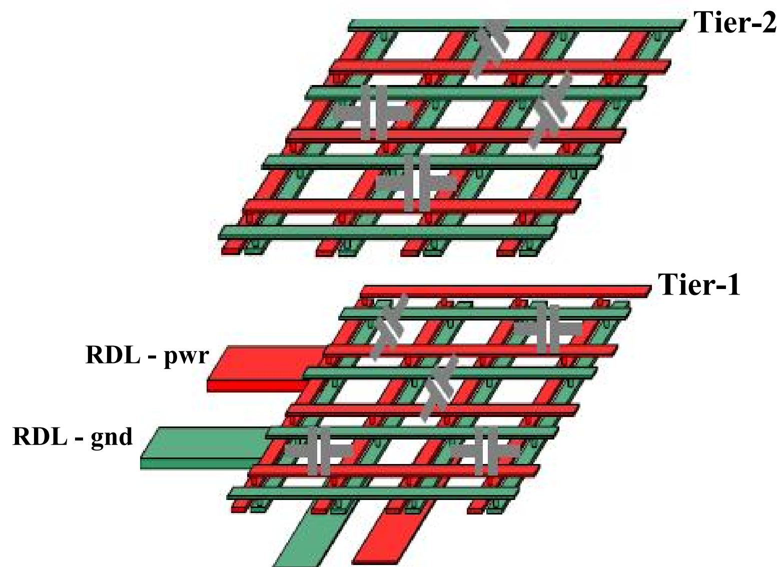


Fig. 40. Power grid tier-1 and tier-2 showing decoupling capacitors uniformly distributed across the power grid structure. The decap symbol represent MIM and MOS decaps [4.9].

The impedance for F2F was estimated at 60-Ω; with decoupling capacitance implemented, the lower frequency (0.1 GHz) impedance has been reduced to 4-Ω using MOS and 0.4-Ω using MIM decap. The upper-peaks were shifted to frequencies above 9 GHz or they were completely eliminated with MIM decaps. The total allowable impedance of the power distribution network has to be reduced to assure that the voltage excursions on the power rail are maintained within allowable limits from dc to desired frequency. Fig. 41(c) and (d) show

the impedance profiles of F2B stacking topology. The inductive characteristics are slightly higher due to the additional power and ground TSVs located at the top and bottom die layers which increases L_{TSV} . The impedance at 0.1 GHz for F2B was estimated at 70-Ω. With the implementation of MOS and MIM decaps, the impedance reduced to 11-Ω and 1-Ω respectively, at the lower frequencies up to 5 GHz. A 59-Ω impedance reduction in the power delivery path of F2B topology was observed. Similarly, the impedance response of B2B stacking topology after using MOS and MIM decaps was similar in outcome. B2B impedance reduced to 15-Ω and 1-Ω using the MOS and MIM decap models, respectively. This is observed in Figure 41(e) and (d). To lower the on-chip impedance for F2B and B2B stacking topology below the 1-Ω value, we need to reduce the resistive properties of the P/G TSVs and other interconnect structures (RDL, C4 bumps, i.e.). The reduction of the PDN impedance can begin with the resistance of the TSV-based PDN (R_{PDN}). From the TSV parametric study performed in previous section, we showed that by increasing the TSV height, pitch and insulator thickness can cause the resistance of the TSV interconnect to increase. Furthermore, since F2F topology only contains P/G TSVs in a single chip tier versus TSV pairs placed on two-tiers like F2B and B2B, indicates less resistive property. As a result, we managed to reduce the impedance for F2F below 1-Ω as shown in Figure 41(a) and (b) up to 0.8 GHz. However, this was not the case for F2B and B2B stacking topologies. Several combinations of decoupling capacitor placement techniques have been implemented and decoupling capacitor values have been used to reduce the impedance beyond 1-Ω for F2B and B2B. The resistive properties make it difficult to bring down the overall PDN impedance. Furthermore, resistive contribution from the on-chip BEOL wire interconnects (e.g. power grid) played an additional role in limiting the reduction of the impedance below 1-Ω for F2B and B2B which is described in Figure 41(c)-(f). To further reduce the impedance below 1- Ω, one can explore a die-size MIM (or MOS) decoupling capacitor model. This has not been explored in this case-study. A die-size decap can be placed anywhere along the die-stacking tier. The most effective location for the die-size decoupling

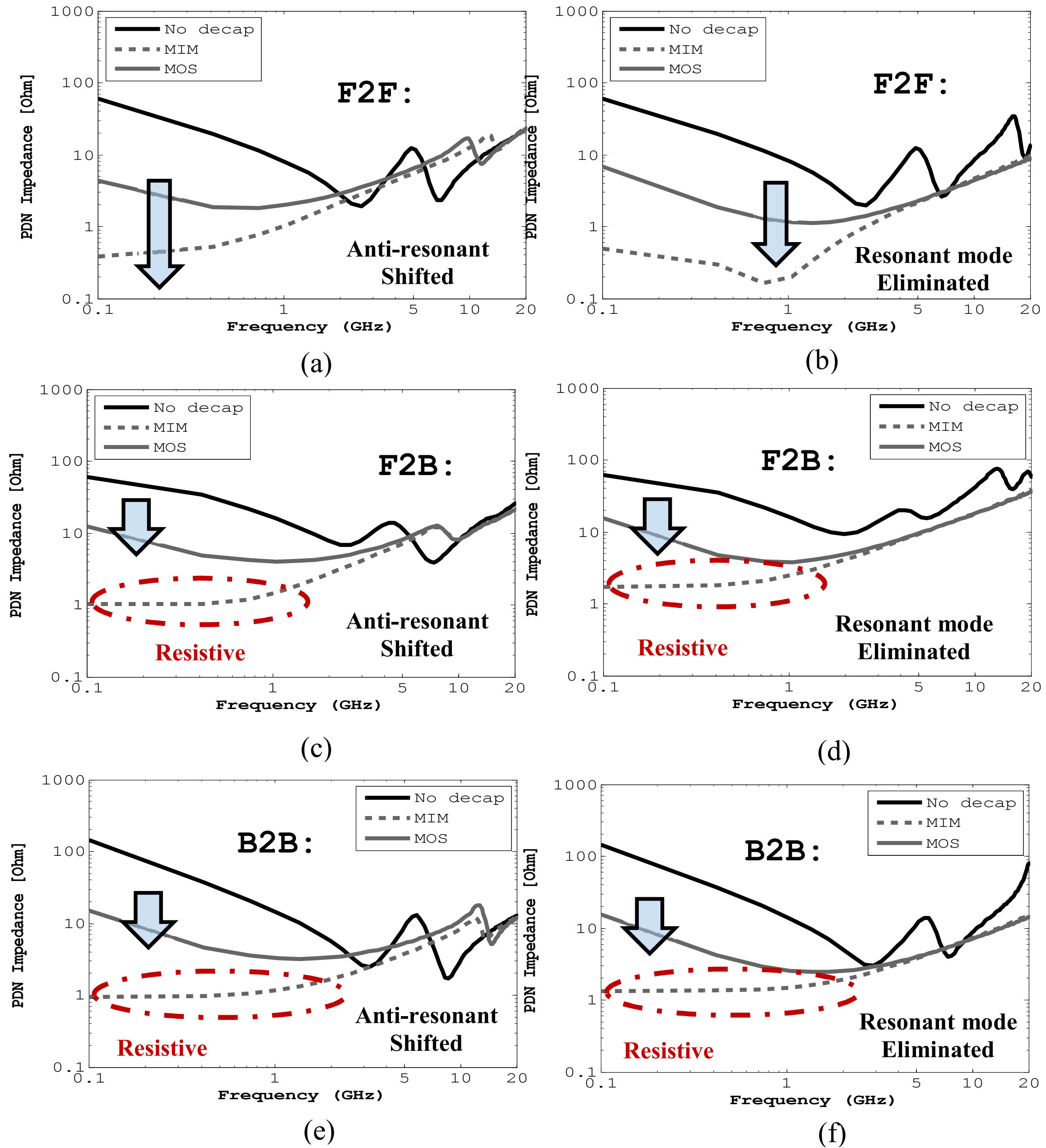


Fig. 41. Three-cases of TSV-based impedances with on-chip decoupling capacitors implemented. Impedance estimated at center [(a),(c) & (e)] and at corner [(b), (d) & (f)] are located.

capacitor is to be placed near the die with the most switching activity in the stack-up. Depending on the complexity of the 3-D stack-up, one can insert multiple die-size decap models. Furthermore, the analysis discussed is based on impedance at the die level. We purposely omitted packaging impact which will be part of our future works discussion.

4.4 Power Supply Noise of TSV-based PDN

Since different die stacking topologies are unavaible in two-dimensional design, we investigate and analyze the supply noise in 3-D integration for F2F, F2B and B2B on-die stacking orientations. The focus of this section is to simulate, quantify and analyze the noise measured for each on-die stacking topology using a simple on-chip circuitry design. Furthermore, the use of circuit design measures the robustness of the TSV-based PDN for each on-die stacking topology. The TSV-based PDN impedances of each power network topology is extracted and included in the circuit model. An example of this is shown in Figures (42) and (43). The simple circuit model used is a ring oscillator circuit. A ring oscillator circuit is a cascaded stage of delay stages and is used to prodcue a timing signal to synchronize functional logic blocks.

Table 4.2 shows the length and width of the transistors within the ring oscillator for 500MHz clock frequency. The total delay time in the decay and rise for an m-stage ring oscillator is $m(\tau_{dhl} + \tau_{dlh})$ and oscillation frequency is:

$$f_o = \frac{1}{m(\tau_{dhl}+\tau_{dlh})} \quad \textbf{(4.7)}$$

Where τ_d is the propagation delay per stage and the number of stages used in the ring structure. The expression for the propagation delay for an NMOS device:

$$\tau_{dhl} = \frac{C}{g_N(V_{DD}-v_{TN})}\left[\frac{2v_{TN}}{(V_{DD}-v_{TN})} + ln\left(\frac{3V_{DD}-4v_{TN}}{V_{DD}}\right)\right] \quad \textbf{(4.8)}$$

For PMOS, the propagation delay is

$$\tau_{dhl} = \frac{C}{g_P(V_{DD}-v_{TP})}\left[\frac{2v_{TP}}{(V_{DD}-v_{TP})} + ln\left(\frac{3V_{DD}-4v_{TP}}{V_{DD}}\right)\right] \quad \textbf{(4.9)}$$

The transconductance parameter of the PMOS and NMOS are denoted by g_N, g_P. The number of inverter stages used in the ring structure and the propagation delay of the delay

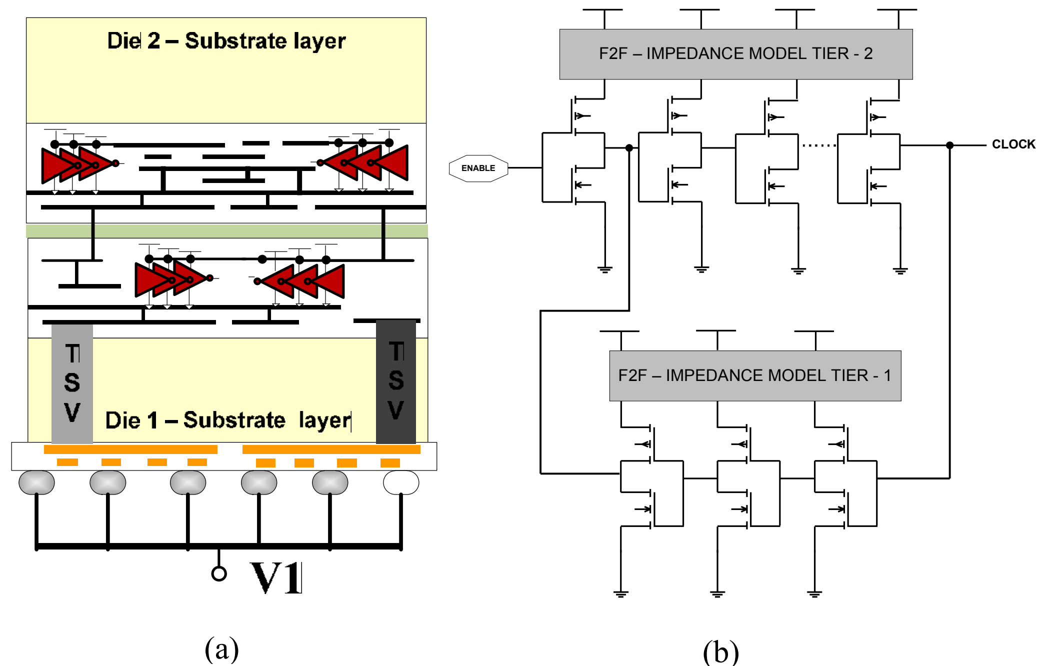
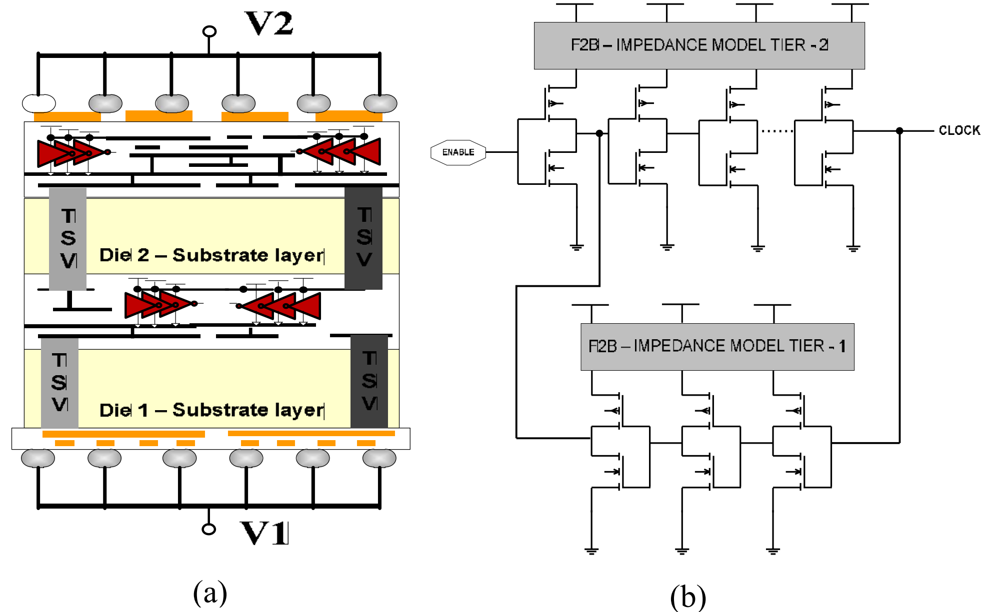


Fig. 42. (a) Cross-sectional view of a two-tier F2F topology (b) schematic capture of a ring oscillator circuit using F2F impedance model.



(a) (b)

Fig. 43. (a)Cross-sectional view of a two-tier F2B topology (b) schematic capture of a ring oscillator circuit using F2B impedance model.

Table 4.2
Transistor physical dimensions used for the Ring Oscillator.

Ring Oscillator	DEVICE	Type	L (nm)	W (nm)
Frequency (ex. 500MHz)	M1… M(2K-1)	NMOS	300, 800	600, 1000, 1500, 3000
	M2… M(2L)	PMOS	300, 800	600, 1000, 1500, 3000

stages limit the oscillation frequency of the ring oscillator. The parameter, C, represents the output capacitance, v_{TN}/v_{TP} represent the threshold voltages of an NMOS/PMOS and V_{DD} is the supply voltage. An HSPICE simulation model of a noisy circuit based on NCSU's FreePDK 45nm technology was developed. A number of switching inverter stages was employed to stress the power rails. The parasitic impedance of the TSV-based PDN network from the case-study produced slight fluctuations. This behavior is visible in figure 44(d).

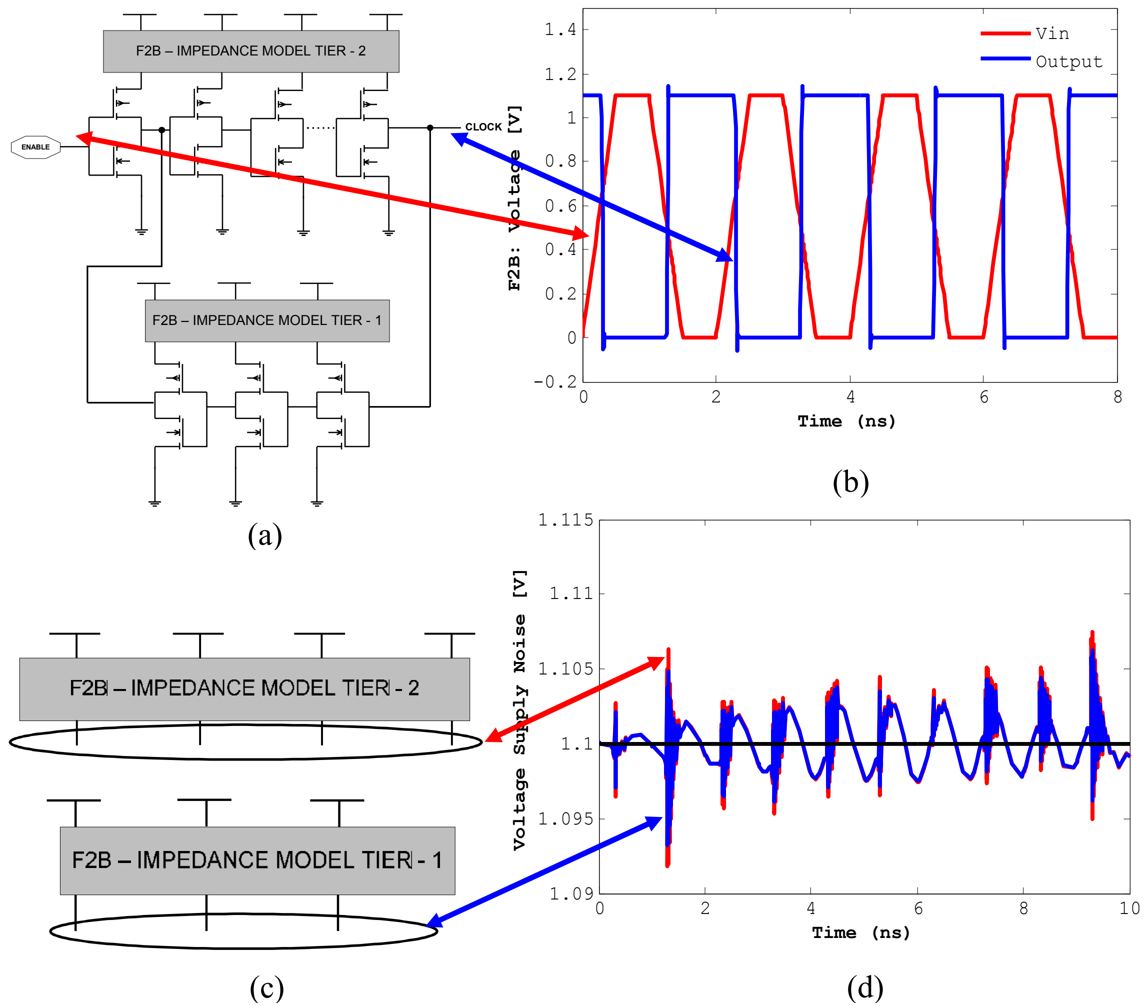


Fig. 44. (a) two-tier ring oscillator (b) clock waveform (c) measured points (d) noisy rail.

With decoupling capacitors, the max. and min. voltage power supply levels are 1.106V and 1.093V respectively. The nominal voltage rail of the power delivery system is 1.1V for all three distinct cases. This is observed by the constant black line in the figures. The total allowable tolerance (TOT) is a little over ±1 % versus typcal TOT for CORE supply rails being ±5 %. The ±1 % tolerance is attributed to the careful design of the on-die physical interconnect structures (power grid, TSVs, micro-bumps and RDL) with the use of on-die decoupling capacitors.

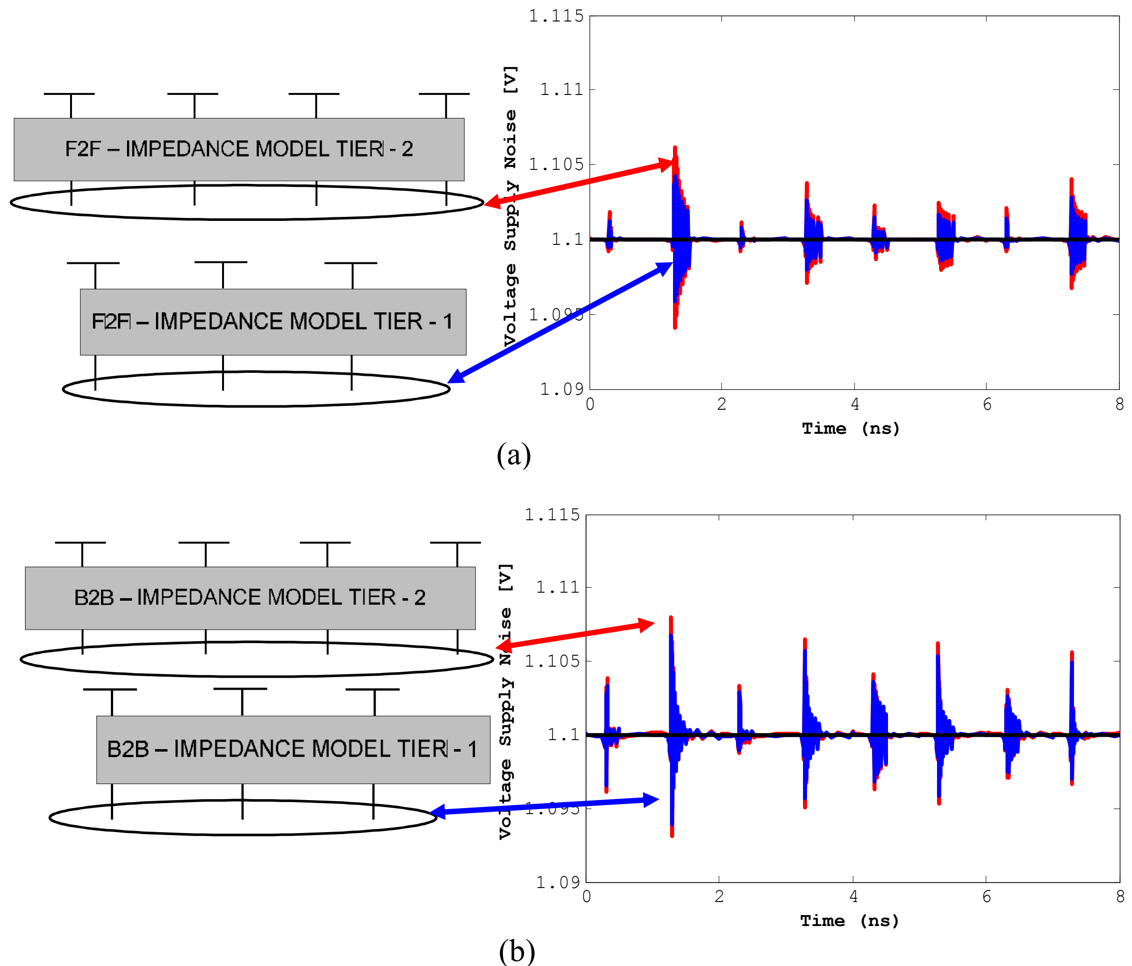


Fig. 45. (a) F2F and (b) B2B supply noise simulation using on-die decoupling capacitors.

However, the chip packaging impedance has been omitted. With the chip packaging impedance contribution, the supply rail fluctuation would increase considerably to higher noise levels. The time-domain HSPICE simulations are plotted for the three different on-die stacking topologies. Simulating the power supply noise demonstrated which of the three on-die stacking topologies produced the worst switching noise on their rails. We observed in each waveform, voltage ringing. The voltage ringing is due to the lack of on-die resistance available to dampen the ringing during the rising edge of the clock signal. According to figure 44(a), F2F on-die stacking topology, generated a slightly lower noise condition than

the other two on-die stacking topologies. We measured a peak-to-peak noise voltage of 12 mV. This is consistent with the impedance curve we estimated for F2F on-die topology. F2B and B2B had a peak-peak noise at 13mV and 15mV respectively. The noise differences between the on-die stacking topologies are marginal where their differences could be considered negligible. However, a difference is observed that is consistent with the estimated impedance of the network prior to simulating the supply voltage. Therefore, one can conclude using the estimated impedance curve that the power delivery system of F2F on-die stacking topology produces relatively less supply rail noise than the other two on-die stacking topologies.

Chapter Summary

We have shown that the PDN impedance curve varies with different on-chip stacking orientations. To best understand the TSV-based power delivery network, we study the on-chip parasitic interconnects. We first performed a parametric study on the circuit element properties e.g. *RLGC*. The parametric study was simulated for some of the on-chip interconnect components that include power grid (global and local-level BEOL interconnects) and P/G TSV pair with frequencies up to 20 GHz. The study described the inductive behavior of the network parasitic as the PDN stacking orientation changed and the interconnect dimensions varied. We created table for TSVs to show the impact circuit elements, RLGC, have on TSV physical dimension. The SSN effects in multi-stacked PDNs can be controlled by limiting the inductance of the network e.g. PDN loop. The number of power and ground TSV pins determines the size of the PDN loop. This is critical, particularly, when large and fast transient current travel throughout the power delivery network. Scalable analytical formulas for the power grid structure, P/G TSV pair and on-chip decoupling capacitors were presented and briefly discussed in this paper. The formulas were written in complex impedance form where they were connected using segmentation method to calculate the overall PDN impedance profile. In all this investigations and modeling performed in this paper, a comparative analysis between the different TSV-based PDN stacking was discussed. The PDN impedance curve for F2B, F2F and B2B were slightly similar in the sense that all impedance curves contained an upper peak (or anti-resonant). However, the impedance curve show F2F PDN chip stacking topology has a lower impedance value than F2B and B2B. This is due to TSVs penetrating noisy substrate layers in F2B and B2B. Furthermore, PDN impedance is limited by PDN resistance.

CHAPTER V

Concluding Remarks and Future Works

The realization of 3-D integration requires a robust power distribution network to ensure reliable operation of circuits on a chip. The power distribution plays a vital part in the success of three-dimensional (3-D) integrated circuits. At the core logic level, the switches operate at high speeds producing switching noises that poses solution challenges especially when multiple dies vertically stacked on top of each other. This dissertation focuses on developing an efficient and reliable technique for modeling TSV-based power delivery networks and their simultaneous switching noise (SSN) for various on-die stacking schemes. This approach combines the implementation of mathematical models for the power grid, TSV, decoupling capacitors and other on-die interconnect components. The segmentation method was used as a basic modeling approach to combine different on-die interconnects structures. To understand how the on-die stacking topologies affect the PDN impedance, we studied three kinds of on-die stacking orientations. For modeling of packaging and PCB level, we recommend using resonant cavity model. In order to optimize the physical design parameters, we performed a parametric study on the power grid and TSV structures to ensure peak ground noise across the power distribution with decoupling capacitors implemented was kept to a minimum. An HSPICE time domain analysis was performed. The result shows that the peak ground noise is a function of the rise time and directly proportional to the peak switching current. The time domain analysis suggests that the peak ground noise of TSV-based PDN occurs at the worst case rise time in the time domain analysis which corresponds to the frequency domain analysis for the estimated impedance properties of the different on-die stacking topologies. The worst case rise time depends on the on-die inductance of the TSV-based PDN and the type and amount of decoupling capacitance used. The on-die MIM and MOS capacitance was used to suppress the switching noise. The impedance of the

power distribution network was below the target impedance for optimum TSV-based PDN design. In order to fully understand 3-D integration PDN effects requires successful characterization, accurate modeling and fast simulation techniques.

Future Works

As an extension to the research and methods described in this dissertation, the following related technical research topics require valuable attention:

1. 3D-IC Chip-Package Co-Modeling and Co-Simulation:
Effective on-chip reduction of SSN and IR-drop demands several types of decoupling capacitors placed between power and ground rails. However, adding decoupling solutions on-chip will produce parallel resonances at mid frequencies due to interconnect dissimilarities where package inductance and on-chip decoupling capacitor interact. To eliminate parallel resonances, a more effective approach is to integrate chip-package co-design flow by co-modeling and co-simulating their PDN systems. One of major challenge is creating a framework or an approach that will ensure chip-package interface with little to no design issues and will remain resonant free. The power distribution should address chip-package and board hierarchical power integrity issues.

2. **Exploring On-die size decoupling capacitors of different types (MIM, Trench and MOS):** Different decoupling capacitor footprint should be explored for 3-D integration design and robust power delivery systems. The on-die size decoupling capacitor can be placed anywhere in the on-die stack up. MIM capacitors and trench capacitors are the leading choices because of their performance and lower ESR properties.

3. Integration of Active Circuits as Decoupling Capacitors in PDN systems: The implementation of active circuits such as operational amplifiers as decoupling capacitor versus passive decoupling capacitors to suppress worst SSN in complex power delivery networks. This will take up on-die real-estate but this can be implemented for high performance complex core logic design requiring unconventional decoupling capacitor solutions.

4. On-Chip switching voltage regulator using capacitors: On-chip decoupling capacitor's performance can be optimized by implementing an on-chip switching capacitor regulator for 3-D integration application. The switching capacitor's charges can increase or decrease depending on how much charges are transferred from the capacitor to the load as the supply voltage reduces below the nominal level. Instead of using a fixed connection in parallel as in typical non-switching cases, the connection of the capacitors to the power and ground networks can be modified from a parallel to series using switches. The switched capacitance can be uniformly distributed throughout the die to maintain a uniform power supply voltage. The objective of the switching circuitry is designed to keep the short-current low when the capacitor is switching. The switching capacitor blocks are connected directly to the global interconnect level of the power distribution grid. The swiched decoupling capacitor is capable of decreasing the on-chip power noise by a factor of two.

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APPENDICES

APPENDIX A

MATLAB CODE:

```
% Gary Charles
% 3DIC Research Group
% 06-29-2011

% TSV-based chip grid element model is used to calculate the
% PDN impedance at the on-chip level.  There are two unit cell
% (s-parameter files) that are arranged in a 10x10 matrix array.
% The files are extracted and converted to z-parameters and
% arranged as a huge array and segmentation method is applied.

close all;
clear all;
clc;

% Importing S-parameter files & Extracing data files:
h=read(rfdata.data,'Power_mesh/Power_Mesh_GridA_TSV_1P1G_F2F.s4p');
h1=read(rfdata.data,'Power_mesh/Power_Mesh_GridB_TSV_1P1G_F2F.s5p');
z0=50;

s_paramsA=extract(h,'S_PARAMETERS',z0);
s_paramsB=extract(h1,'S_PARAMETERS',z0);

freq=h.Freq;
z_paramsA=s2z(s_paramsA,z0);
z_paramsB=s2z(s_paramsB,z0);

% UnitCellA: Z-matrix elements
zppA=z_paramsA(1,1,:);
zpqA=z_paramsA(1,2,:);
zprA=z_paramsA(1,3,:);
zpsA=z_paramsA(1,4,:);

zqpA=z_paramsA(2,1,:);
zqqA=z_paramsA(2,2,:);
zqrA=z_paramsA(2,3,:);
zqsA=z_paramsA(2,4,:);

zrpA=z_paramsA(3,1,:);
zrqA=z_paramsA(3,2,:);
zrrA=z_paramsA(3,3,:);
zrsA=z_paramsA(3,4,:);

zspA=z_paramsA(4,1,:);
zsqA=z_paramsA(4,2,:);
zsrA=z_paramsA(4,3,:);
```

```
zssA=z_paramsA(4,4,:);

ZmatA=[zppA, zpqA, zprA, zpsA;...
       zqpA, zqqA, zqrA, zqsA;...
       zrpA, zrqA, zrrA, zrsA;...
       zspA, zsqA, zsrA, zssA];

% UnitCellB: Z-matrix elements
zppB=z_paramsB(1,1,:);
zpqB=z_paramsB(1,2,:);
zprB=z_paramsB(1,3,:);
zpsB=z_paramsB(1,4,:);
zptB=z_paramsB(1,5,:);

zqpB=z_paramsB(2,1,:);
zqqB=z_paramsB(2,2,:);
zqrB=z_paramsB(2,3,:);
zqsB=z_paramsB(2,4,:);
zqtB=z_paramsB(2,5,:);

zrpB=z_paramsB(3,1,:);
zrqB=z_paramsB(3,2,:);
zrrB=z_paramsB(3,3,:);
zrsB=z_paramsB(3,4,:);
zrtB=z_paramsB(3,5,:);

zspB=z_paramsB(4,1,:);
zsqB=z_paramsB(4,2,:);
zsrB=z_paramsB(4,3,:);
zssB=z_paramsB(4,4,:);
zstB=z_paramsB(4,5,:);

ztpB=z_paramsB(5,1,:);
ztqB=z_paramsB(5,2,:);
ztrB=z_paramsB(5,3,:);
ztsB=z_paramsB(5,4,:);
zttB=z_paramsB(5,5,:);

ZmatB=[zppB, zpqB, zprB, zpsB, zptB;...
       zqpB, zqqB, zqrB, zqsB, zqtB;...
       zrpB, zrqB, zrrB, zrsB, zrtB;...
       zspB, zsqB, zsrB, zssB, zstB;...
       ztpB, ztqB, ztrB, ztsB, zttB];

% Setup matrix blocks with internal/external port assignment
% center with internal ports:
Mat11=ZmatA(1:4,1:4,:);                 % Center only internal port
Mat55=ZmatB(1:5,1:5,:);

% corner with internal ports:
```

```
Mat21=ZmatA([1 4],[1 4],:);              % Corner right top
Mat23=ZmatA([2 3],[2 3],:);              % Corner left bottom
Mat12=ZmatA([1 2],[1 2],:);
% corner with external port:
Mat25=ZmatB(3:5,3:5,:);                  % Corner left top
Mat27=ZmatB([1 2 5],[1 2 5],:);          % Corner right bottom

% edge with internal ports:
Mat31=ZmatA([1 3 4],[1 3 4],:);          % Edge top
Mat32=ZmatA([1 2 4],[1 2 4],:);          % Edge right
Mat33=ZmatA([2 3 4],[2 3 4],:);          % Edge left
Mat34=ZmatA(1:3,1:3,:);                  % Edge bottom

% Converting from Matrix to Cell:
G11=Group_Mat2Cell([1 1 1 1],Mat11);
G55=Group_Mat2Cell([1 1 1 1 1],Mat55);

G21=Group_Mat2Cell([1 1],Mat21);
G23=Group_Mat2Cell([1 1],Mat23);
G12=Group_Mat2Cell([1 1],Mat12);

G25=Group_Mat2Cell([1 1 1],Mat25);
G27=Group_Mat2Cell([1 1 1],Mat27);

G31=Group_Mat2Cell([1 1 1],Mat31);
G32=Group_Mat2Cell([1 1 1],Mat32);
G33=Group_Mat2Cell([1 1 1],Mat33);
G34=Group_Mat2Cell([1 1 1],Mat34);

% Small PDN structure combining small unit cells into a large PDN grid:
G_combine_1mmx1mm=Group_Cell2Cell([3 3 3 3 2 ...
                           3 4 4 4 3 ...
                           3 4 4 4 3 ...
                           3 4 4 4 3 ...
                           3 4 5 4 3 ...
                           3 4 4 4 3 ...
                           3 4 4 4 3 ...
                           3 4 4 4 3 ...
                           3 4 4 4 3 ...
                           2 3 3 3 2],...
                           {G25 G31 G31 G31 G21 ...
                            G33 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G32 ...
                            G33 G11 G55 G11 G32 ...
                            G33 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G32 ...
                            G23 G34 G34 G34 G12});
```

```
% Calculating the impedance of the entire structure:
Zout_1mmx1mm=Port_Calculation(G_combine_1mmx1mm,[2 4;5 7;8 10;11 13;...
                                 3 15;6 19;9 23;12 27;14 31;...
                                 16 18;20 22;24 26;28 30;...
                                 17 33;21 37;25 41;29 45;32 49;...
                                 34 36;38 40;42 44;46 48;...
                                 35 51;39 55;43 59;47 63;50 67;...
                                 52 54;56 58;60 62;64 66;...
                                 53 69;57 73;61 77;65 82;68 86;...
                                 70 72;74 76;78 81;83 85;...
                                 71 88;75 92;79 96;84 100;87 104;...
                                 89 91;93 95;97 99;101 103;...
                                 90 106;94 110;98 114;102 118;105 122;...
                                 107 109;111 113;115 117;119 121;...
                                 108 124;112 128;116 132;120 136;123
140;...
                                 125 127;129 131;133 135;137 139;...
                                 126 142;130 146;134 150;138 154;141
158;...
                                 143 145;147 149;151 153;155 157;...
                                 144 160;148 163;152 166;156 169;159
172;...
                                 161 162;164 165;167 168;170 171;]);


% Combining the entire structure into a huge cell:
G_combine=Group_Cell2Cell([3 3 3 3 3 3 3 3 3 2 ...
                           3 4 4 4 4 4 4 4 4 3 ...
                           3 4 4 4 4 4 4 4 4 3 ...
                           3 4 4 4 4 4 4 4 4 3 ...
                           3 4 4 4 5 4 4 4 4 3 ...
                           3 4 4 4 4 4 4 4 4 3 ...
                           3 4 4 4 4 4 4 4 4 3 ...
                           3 4 4 4 4 4 4 4 4 3 ...
                           3 4 4 4 4 4 4 4 4 3 ...
                           2 3 3 3 3 3 3 3 3 2],...
                           {G25 G31 G31 G31 G31 G31 G31 G31 G31 G21 ...
                            G33 G11 G11 G11 G11 G11 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G11 G11 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G11 G11 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G55 G11 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G11 G11 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G11 G11 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G11 G11 G11 G11 G11 G32 ...
                            G33 G11 G11 G11 G11 G11 G11 G11 G11 G32 ...
                            G23 G34 G34 G34 G34 G34 G34 G34 G34 G12});

% Calculating the impedance of the entire structure:
Zout=Port_Calculation(G_combine,[2 4;5 7;8 10;11 13;14 16;17 19;20 22;23
25;26 28;...
```

```
                                  3 30;6 34;9 38;12 42;15 46;18 50;21 54;24
58;27 62;29 66;...
                                  31 33;35 37;39 41;43 45;47 49;51 53;55
57;59 61;63 65;...
                                  32 68;36 72;40 76;44 80;48 84;52 88;56
92;60 96;64 100;67 104;...
                                  69 71;73 75;77 79;81 83;85 87;89 91;93
95;97 99;101 103;...
                                  70 106;74 110;78 114;82 118;86 122;90
126;94 130;98 134;102 138;105 142;...
                                  107 109;111 113;115 117;119 121;123
125;127 129;131 133;135 137;139 141;...
                                  108 144;112 148;116 152;120 156;124
160;128 164;132 169;136 173;140 177;143 181;...
                                  145 147;149 151;153 155;157 159;161
163;165 168;170 172;174 176;178 180;...
                                  146 183;150 187;154 191;158 195;162
199;166 203;171 207;175 211;179 215;182 219;...
                                  184 186;188 190;192 194;196 198;200
202;204 206;208 210;212 214;216 218;...
                                  185 221;189 225;193 229;197 233;201
237;205 241;209 245;213 249;217 253;220 257;...
                                  222 224;226 228;230 232;234 236;238
240;242 244;246 248;250 252;254 256;...
                                  223 259;227 263;231 267;235 271;239
275;243 279;247 283;251 287;255 291;258 295;...
                                  260 262;264 266;268 270;272 274;276
278;280 282;284 286;288 290;292 294;...
                                  261 297;265 301;269 305;273 309;277
313;281 317;285 321;289 325;293 329;296 333;...
                                  298 300;302 304;306 308;310 312;314
316;318 320;322 324;326 328;330 332;...
                                  299 335;303 338;307 341;311 344;315
347;319 350;323 353;327 356;331 359;334 362;...
                                  336 337;339 340;342 343;345 346;348
349;351 352;354 355;357 358;360 361;]);


% Magnitude of small PDN impedance w/o TSV:
mag_z11=abs(Zout_1mmx1mm(1,1,:));
mag_z22=abs(Zout_1mmx1mm(2,2,:));

% Magnitude of large PDN impedance w/o TSV:
magZ11=abs(Zout(1,1,:));
magZ22=abs(Zout(2,2,:));

% Combining 2 power grid structures using segmentation method:
A=Group_Mat2Cell([1 1],Zout);
B=Group_Mat2Cell([1 1],Zout);

M_combine=Group_Cell2Cell([2 2],{A B});
```

```
Zhier2=Port_Calculation(M_combine,[2 3]);
z11_tier2=abs(Zhier2(1,1,:));
z22_tier2=abs(Zhier2(2,2,:));

figure(1)
loglog(freq/1e9,mag_z11(:),'k')
ylabel('PDN Impedance [  \Omega ]')
xlabel('Frequency (GHz)')
hold on;
loglog(freq/1e9,mag_z22(:),'-.r')
% loglog(freq/1e9,mag_z22(:),':k')
% loglog(freq/1e9,magZ11(:),'Color',[0.4 0.4 0.8],'LineStyle','-')
% loglog(freq/1e9,magZ22(:),'Color',[0.4 0.4 0.8],'LineStyle',':')
hold off;
axis([.1 20 10^0 10^2.1])
set(gca, 'YTick', [1 10 100])
set(gca, 'YTickLabel', [1, 10, 100]);
set(gca, 'XTick', [.1 1 10 20])
set(gca, 'XTickLabel', [.1, 1, 10, 20]);
hs=legend('Z_1_1','Z_2_2');
```

HSPICE SIMULATION using MATLAB:

```
% Procesing Transient simulation:
close all;
clear all;
clc;

SSN_results =
textread('Hspice_sims/B2F_NoiseCaseStudy_no_decap.txt','%f');

% var_Time=SSN_results(1:7:end);
% var_node_V5=SSN_results(2:7:end);
% var_node_V3=SSN_results(3:7:end);
% var_node_Vdd=SSN_results(4:7:end);
% var_node_V2=SSN_results(5:7:end);
% var_node_V4=SSN_results(6:7:end);
% var_node_V6=SSN_results(7:7:end);

% F2B power supply noise
% var_Time=SSN_results(1:9:end);
% var_node_V7=SSN_results(2:9:end);
% var_node_V5=SSN_results(3:9:end);
% var_node_V3=SSN_results(4:9:end);
% var_node_Gnd=SSN_results(5:9:end);
% var_node_V2=SSN_results(6:9:end);
% var_node_Vdd=SSN_results(7:9:end);
% var_node_V6=SSN_results(8:9:end);
% var_node_V8=SSN_results(9:9:end);
```

```
% F2F power supply noise
% var_Time=SSN_results(1:7:end);
% var_node_V5=SSN_results(2:7:end);
% var_node_V3=SSN_results(3:7:end);
% var_node_Vdd=SSN_results(4:7:end);
% var_node_V2=SSN_results(5:7:end);
% var_node_V4=SSN_results(6:7:end);
% var_node_V6=SSN_results(7:7:end);

% B2B power supply noise
var_Time=SSN_results(1:7:end);
var_node_V5=SSN_results(2:7:end);
var_node_V3=SSN_results(3:7:end);
var_node_Vdd=SSN_results(4:7:end);
var_node_V2=SSN_results(5:7:end);
var_node_V4=SSN_results(6:7:end);
var_node_V6=SSN_results(7:7:end);

myfig1=figure('Position',[500 340 550 350]);
plot((var_Time(:))*1e9,var_node_V4(:),'Color',[1 0
0],'Linewidth',2.5,'LineStyle','-')
ylabel('Voltage Supply Noise
[V]','Fontsize',10.5,'fontweight','b','FontName','FixedWidth')
xlabel('Time
(ns)','Fontsize',10.5,'fontweight','b','FontName','FixedWidth')
hold on;
plot((var_Time(:))*1e9,var_node_V2(:),'b','LineStyle','-','Linewidth',2.5)
plot((var_Time(:))*1e9,var_node_V6(:),'Color',[0 0 0],'Linewidth',2.5)
%text(28,1.115,'F2B Topology','Fontsize',10.5,'fontweight','b','Color',[0
0 0],'FontName','FixedWidth')
%text(2,0.004,'Z_t_a_r_g_e_t','Fontsize',12,'fontweight','b','Color',[0 0
1],'FontName','FixedWidth')
%axis([0.5 20 0.001 10^2.5])
%set(gca, 'YTick', [0.001 0.01 0.1 1 10 100])
%set(gca, 'YTickLabel', [0.001, 0.01, 0.1, 1, 10, 100]);
%set(gca, 'XTick', [1 5 10 20])
%set(gca, 'XTickLabel', [1, 5, 10, 20]);
set(gca,'FontName','FixedWidth')
%hs=legend('@ node:5','Ideal case:Vdd!');
%set(hs,'Box','off')
%set(hs,'Location','Northwest')
set(gca,'FontSize',10.5)
hold off;
```

HFSS Unit cell Model with dimensions: