ABSTRACT

MEDFORD, JOHN A. Electrical Characterization of Continuous-Czochralski Grown Silicon for Photovoltaic Applications. (Under the direction of Dr. Lewis Reynolds, Dr. John Muth and Dr. Justin Schwartz).

The high cost of photovoltaic cells limits the adaption of solar electricity as an alternative to traditional non-renewable sources. An emerging technology in photovoltaic substrate production, the *Continuous*-Czochralski growth process, has the potential to increase the efficiency of photovoltaic cells compared to traditional Czochralski growth while decreasing the cost of monocrystalline silicon solar cells. This work examines several issues which may prevent these goals from being realized. The material properties and minority carrier lifetime of *Continuous*-Czochralski grown wafers were studied to understand sources of efficiency loss and provide insight on the underlying mechanisms.

A material analysis was performed on four sets of *Continuous*-Czochralski grown n-type wafers with varying resistivity to understand and predict changes in the minority carrier lifetime and solar cell efficiency due to materials parameters. Field effect passivation of wafer surfaces by Al_2O_3 is verified for n-type silicon, validating this passivation technique for solar cell structures with an n-type base. Remnant damage from the wafer sawing process is found to extend at least 25 µm below the surface, which is expected to affect the efficiency of solar cells. Minority carrier lifetime, photoluminescence, and light beam induced current mapping techniques show changes in the distribution of lifetime through cell processing and suggest minimal residual stress from the growth process. Stress measurements confirm the absence of residual stress effects across the wafers, and no crystal defects are observed after preferential

etching. The absence of stress and defects indicates the *Continuous*-Czochralski growth process produces high quality crystals. Minority carrier lifetime of wafers as determined by electron beam induced current remains unchanged after a boron emitter implantation and a 1000°C anneal, decreases after phosphorus back-side implantation and a subsequent 840°C anneal, then increases again to its maximum value after solar cell passivation and contact formation. Transient spectroscopy measurements found that an oxygen-hydrogen complex forms with energy levels at $E_v + 0.35$ eV and $E_c – 0.14$ eV along with a lower-energy thermal donor species. Although the source of hydrogen was attributed to sample preparation, this effect must be carefully considered and studied further to determine if the observed complex affects minority carrier lifetime in the solar cell.

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Electrical Characterization of Continuous-Czochralski Grown Silicon for Photovoltaic Applications

by

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DEDICATION

I dedicate this work to my wife, partner, and best friend Kristina for all her love and support.

BIOGRAPHY

John Medford was born in Knoxville, Tennessee to parents Jim and Lana and grew up in Harrisburg, North Carolina. After graduating from Hickory Ridge High School, he attended North Carolina State University where he graduated with a Bachelor of Science degree in Materials Science and Engineering. Continuing his education, John pursued a Master of Science degree in Materials Science and Engineering at North Carolina State University under the direction of Dr. George Rozgonyi, during which he married his wife Kristina. Upon Dr. Rozgonyi's medical leave, Dr. Lewis Reynolds took his place as mentor and advisor.

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CHAPTER I: INTRODUCTION

Motivation

With a global dependence on non-renewable fossil fuels for energy, the world has seen increasing interests in renewable, environmentally friendly energy sources in the past few decades.[2-3] Among such energy sources, solar energy presents an attractive option because it is harvested directly from Earth's only renewable energy source, the Sun. While many methods exist for converting photonic energy into forms we can use, direct conversion to electricity via the photovoltaic effect allows us to power our modern electrical technology. Photons from the sun are converted to electricity using solar cells, which rely on large-area semiconductor wafers. Solar cells are becoming increasingly popular as an alternative energy source to provide clean electricity compared to traditional sources.[4] Figure 1.1 shows the increasing installed capacity for solar power production in the United States, indicating future demand for cost-effective photovoltaic energy conversion. Figure 1.2 compares the decreasing cost to increasing production of photovoltaic energy. According to the depicted future projections, the cost of solar energy will fall lower than that of coal in the coming years. This represents a turning point in the photovoltaic market, in which solar energy will present a more economical alternative to fossil fuels. With renewable solar energy less expensive than coal, solar energy can begin to replace fossil fuels as the standard energy source. However, the cost of solar energy must continue to decrease in order to facilitate these changes.

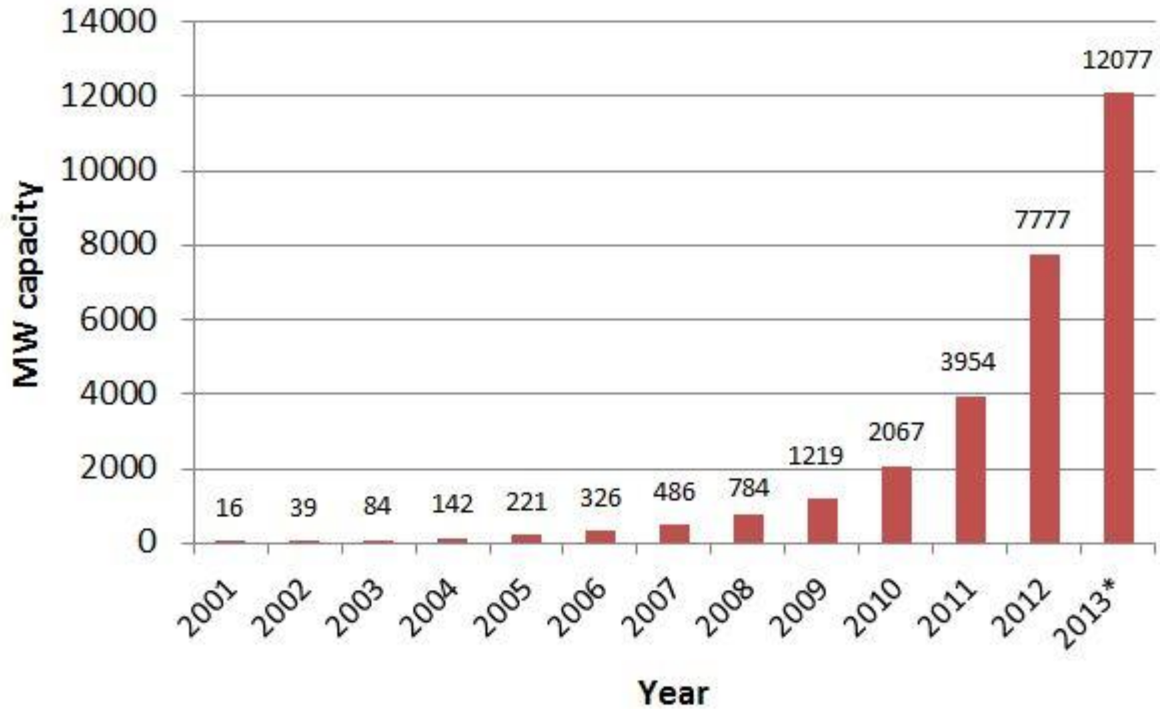

Figure 1.1: Installed capacity for electricity production by solar conversion in the United States compiled by the European Photovoltaic Industry Association. The recent increase indicates the growing market demand for solar energy. Reproduced from Reference 4.

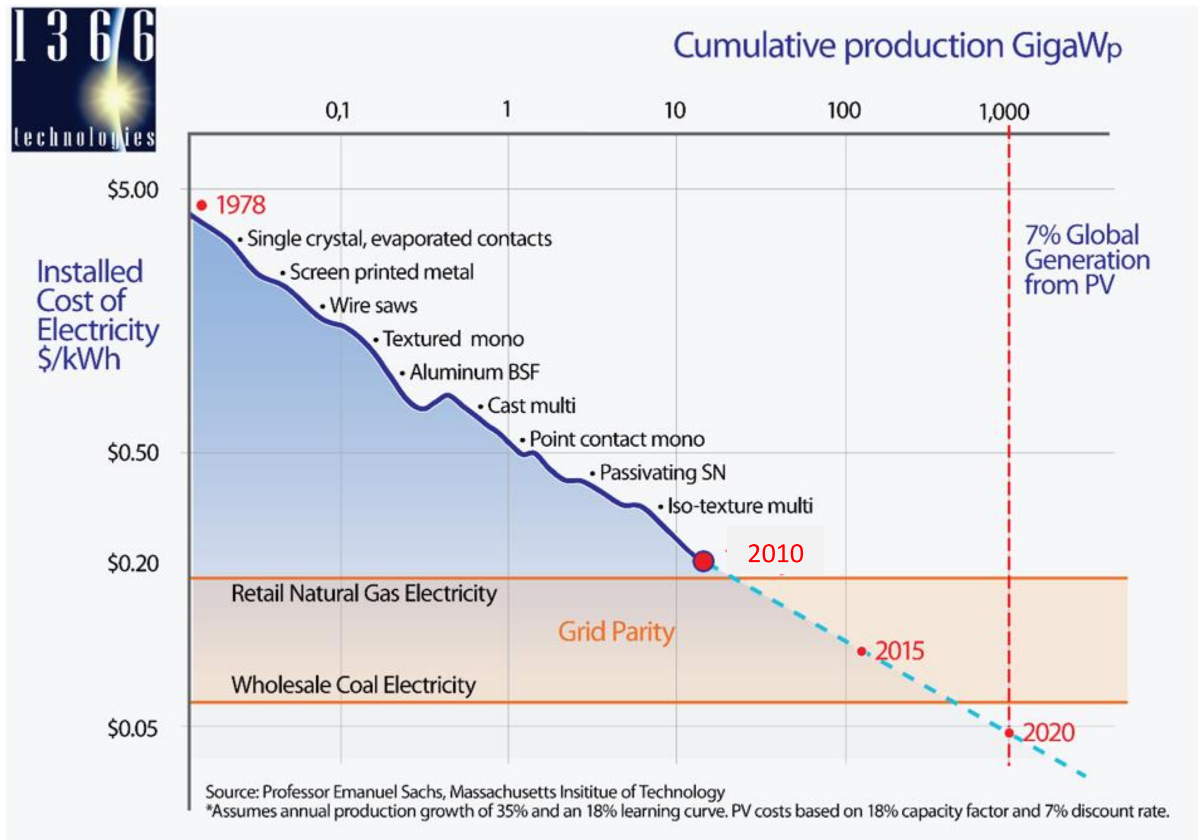

Figure 1.2: Relationship between cost and production of solar energy as of 2010 presented with a future projection through 2020, indicating the potential for "grid parity" in the coming years. Technological advancements which have historically decreased costs are also indicated. Created by E Sachs, reproduced from Reference 5.

As indicated by the advancements in silicon technology responsible for decreasing the cost of solar energy, silicon has dominated the photovoltaics market. Historically, scrap silicon wafers from the microelectronics industry have supplied the photovoltaic industry with substrates for solar cells. These device-grade silicon wafers are grown in the Czochralski (CZ) process, which is very expensive but produces the highest quality material. In this process, high purity silicon feedstock material is melted in a crucible and a cooled seed crystal is

lowered into the melt. As the seed cools the melt, the single crystal grows while maintaining orientation. The crystal is pulled upward from the melt while rotating in one direction and the crucible is rotated in the opposite direction, resulting in a long cylindrical crystal. This process is illustrated in Figure 1.3. Common sources for defects include thermal gradients and turbulence in the melt which leads to residual stress in the crystal[6] or varying concentrations of dopant and impurities along the crystal axis due to segregation during growth.

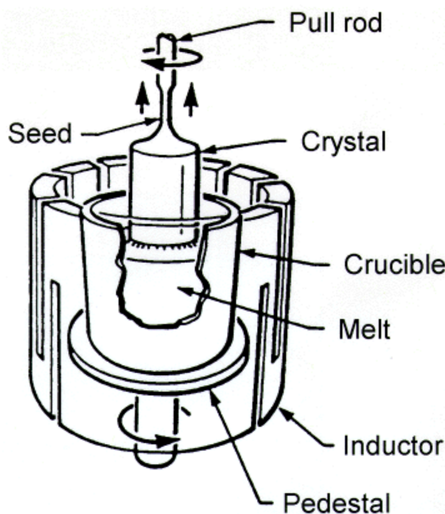

Figure 1.3: Diagram illustrating the principles of CZ crystal growth, with all main components labeled. Notice the opposite rotations of the crucible and crystal. Image reproduced from Reference 7.

As the market for solar energy grows, the demand for low-cost silicon wafers exceeds the supply of microelectronic byproducts. New, low cost methods are being developed to produce silicon wafers suitable for photovoltaic applications yet less expensive than the

device-grade CZ process.[8] Unfortunately, these methods tend to yield solar cells inferior to device-grade CZ cells. The record efficiency of a cast-multicrystalline silicon solar cell is near 20%, while that of a monocrystalline CZ cell is near 25%.[4] Researchers are constantly attempting to mitigate the effects of the lower quality of photovoltaic silicon without increasing cost. A comparison of various photovoltaic technologies in Table 1.1 shows the superior efficiency of monocrystalline CZ silicon to other silicon growth methods. Should the production of solar-grade silicon wafers by the CZ technique become as affordable as other techniques, the cost of solar energy production would decrease significantly, increasing motivation to switch from fossil fuels to solar energy.

Table 1.1: Confirmed photovoltaic cell efficiencies measured under 1000 W/m^2 at 20˚C. Reproduced from Reference 9.

Silicon technology	Efficiency (%)	Area (cm^2)	V_{oc} (V)	Jsc (mA/cm^2)	Fill Factor (%)	Tested:	Description
Monocrystalline	25.0 ± 0.5	4.00	0.706	42.7	82.8	Sandia 3/99	UNSW PERL
Multicrystalline	20.4 ± 0.5	1.00	0.664	38.0	80.9	NREL 5/04	FhG-ISE
Thin film transfer	20.1 ± 0.4	243	0.682	38.1	77.4	NREL 10/12	Solexel 43 μm
Thin film submodule	10.5 ± 0.3	94.0	0.492	29.7	72.1	FhG-ISE 8/07	CSG Solar (1-2 μm on glass)

Continuous-Czochralski (C-CZ) growth process

To reduce the cost of CZ silicon for solar and microelectronic applications, many methods for a more continuous system have been proposed.[10-11] Some methods for *Continuous*-Czochralski (*C*-CZ) growth involve the use of expensive equipment such as baffled crucibles or siphons drawing from feeding crucibles.[12] Unfortunately, the cost of such methods is not consistent with the goal of a lower cost growth technique. Instead, *C*-CZ growth can be achieved by replenishing the silicon melt with regular sized pieces of feedstock added carefully, such that turbulence and temperature gradients can be minimized.[13] This *C*-CZ growth process is shown in Figure 1.4. Crystals can be continuously pulled one after the other while adding small pellets of feedstock far away from crystal growth. Pellets must be added slowly to minimize thermal gradients from cooling and agglomeration of chunks in the melt yet fast enough to maintain growth rate. As a result, crystals can be grown continuously, allowing for faster production. Reducing time between crystals reduces the high thermal budget required for maintaining molten silicon. This also increases the number of crystals which can be produced from a given crucible, which is expensive and must be replaced often.

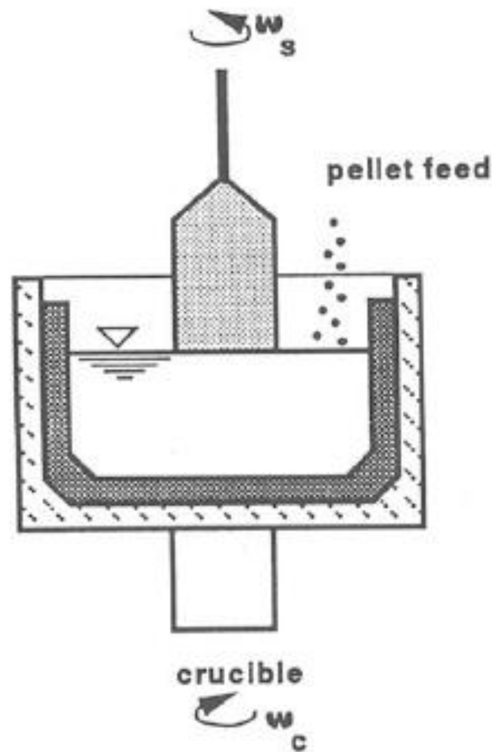

Figure 1.4: Diagram of *C*-CZ growth process. Reproduced from Reference 10.

In comparison to CZ growth, *C*-CZ growth yields more uniform and consistent crystals. Towards the end of the CZ process, dopant species and undesirable impurities which have been concentrated in the melt by segregation will be included in the crystal. Thus, wafers from the tails of CZ crystals will be of lower purity which decreases the quality of the wafer and photovoltaic cell.[14] As the dopant concentration changes, the electrical properties of the wafer vary as well. As the electrical properties deviate from the target, the photovoltaic cell will not perform as designed and efficiency will be limited.[15] By continuously feeding the crucible instead of feeding with a single charge, the melt level and turbulence can be held steady and impurity content is more constant in *C*-CZ crystals.[16] Doping can be held constant through

growth, or varied by changing the rate of dopant addition. Furthermore, turbulence and thermal gradients in CZ growth lead to residual thermal stress in the crystal, manifesting as crystalline dislocations which decrease wafer quality and may still remain after photovoltaic cell processing.[12] Because the *C*-CZ process maintains a constant melt volume, the occurrence of these dislocations can be limited. However, thermal gradients may arise due to addition of cold feedstock and high pull rates if these parameters are not carefully controlled. The understanding and control of stress resulting from the crystal growth is critical to the production of high quality photovoltaic silicon wafers.

Background

Semiconductors and doping

All photovoltaic technologies rely on the unique properties of semiconductors to convert photons into energy. Figure 1.5 compares the band diagrams of insulators, semiconductors and metals. Insulators have a very large gap in energy between the conduction and valence bands. Valence electrons cannot gain enough energy to reach the conduction band. Semiconductors have a similar band gap, but the gap is narrow enough that electrons can gain sufficient energy to be excited into the conduction band.

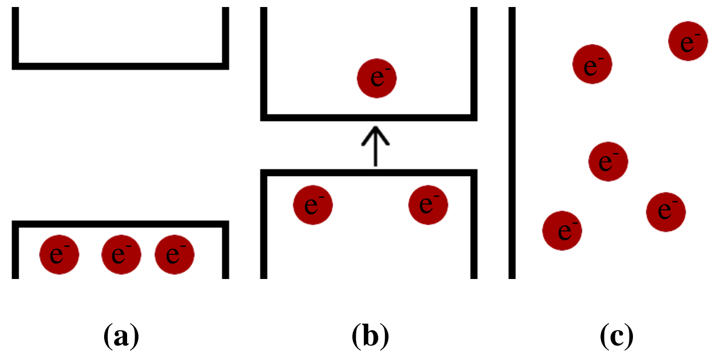

Figure 1.5: Comparison of band diagrams typical of (a) insulators, (b) semiconductors and (c) metals.

When an electron in a semiconductor moves from the valence band to the conduction band, a positive hole is left in the valence band due to the absence of the electron. As other electrons take the place of this hole, the hole can move about the semiconductor and transport its positive charge. Therefore we treat holes as charge carriers of equal magnitude and opposite charge to electrons. In a region of semiconductor, electrons can be freely donated or accepted by intentionally incorporating impurity elements to introduce a concentration of electron or hole charge carriers, respectively. These impurities, called dopants, can be grown into semiconductors to produce uniform doping or added to select regions by chemical or ion-implantation techniques. Changing the concentration of carriers in a semiconductor modifies the conductivity and resistivity. The resistivity ρ of a semiconductor is related to the concentration of charge carriers N and its charge q by Equation 1.1. If charge carriers are only provided by the dopant and 100% of the dopant is ionized, then N will be equal to the doping concentration. The carrier which is added by doping will be in a much greater concentration

than the opposite carrier and is called the majority carrier. The carrier of opposite charge is the minority carrier.

In addition to charge carrier contributions by dopant species, oxygen in silicon is known to form a variety of electron donor complexes from various precipitates and complexes in silicon.[17-25] These oxygen precipitates can be grown by holding the silicon at intermediate temperatures near 350˚C – 400˚C, or dissolved at temperatures above 600˚C to eliminate the defect states. Because of the strong dependence of oxygen donors on thermal treatment, they are called thermal donors. Oxygen can also participate in electrically active defect states with other elements, such as hydrogen.

$$\rho = \frac{1}{\mu N q} \qquad \text{Equation 1.1}$$

The mobility μ of an ionized carrier describes its ability to move and conduct within the semiconductor. At a fixed temperature, mobility is dependent on the dopant species and concentration according to Equation 1.2.[26] For phosphorus, the substrate dopant species used in this study, μ_{min} = 68.5 cm^2/Vs, μ_{max} = 1414 cm^2/Vs, N_r = 9.20 x 10^{16} cm^{-3}, and α = 0.771. N is the donor concentration used to calculate mobility. Resistivity, which can be easily measured, can therefore be used to determine N for a given sample by substituting Equation 1.2 into 1.1 and solving for N.

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1+\left(\frac{N}{N_r}\right)^{\alpha}} \qquad \text{Equation 1.2}$$

Carrier generation and recombination

Besides doping, carriers can be generated by exciting electrons from the valence to conduction band, creating both a positive and negative carrier. Sufficient energy for excitation can be provided by an incident photon or electron and absorbed by a valence electron, facilitating the event. This process is illustrated in Figure 1.6. When this process occurs in a doped semiconductor, the concentration of the majority carriers does not change significantly as long as carrier generation is less than the doping concentration. The minority carrier concentration is very low at equilibrium, and will therefore be completely dependent on the number of carriers injected. This condition is referred to as "low level injection." As the concentration of injected carriers surpasses that of the doping concentration, the sample is in a "high level injection" condition. The behavior of the carriers is very dependent on the injection level.[27]

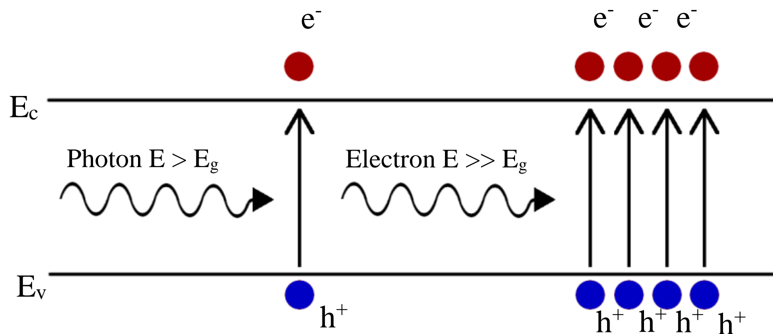

Figure 1.6: Excitation of electrons from the valence band to the conduction band by absorption of a photon (left) or high energy electron (right). Photons create one electron-hole pair, while high energy electrons can create many.

After excitation, the electron and hole are not stable and will eventually recombine by one of three mechanisms: Auger, radiative, or Shockley-Read-Hall. As a result, the electron returns to the valence band and its energy is released. These three processes are illustrated in Figure 1.7. The time between generation and recombination of an electron-hole pair is called the carrier lifetime. Only the minority carrier concentration is effected by generation and recombination under low level conditions, so the carrier lifetime is often referred to as the "minority carrier lifetime."

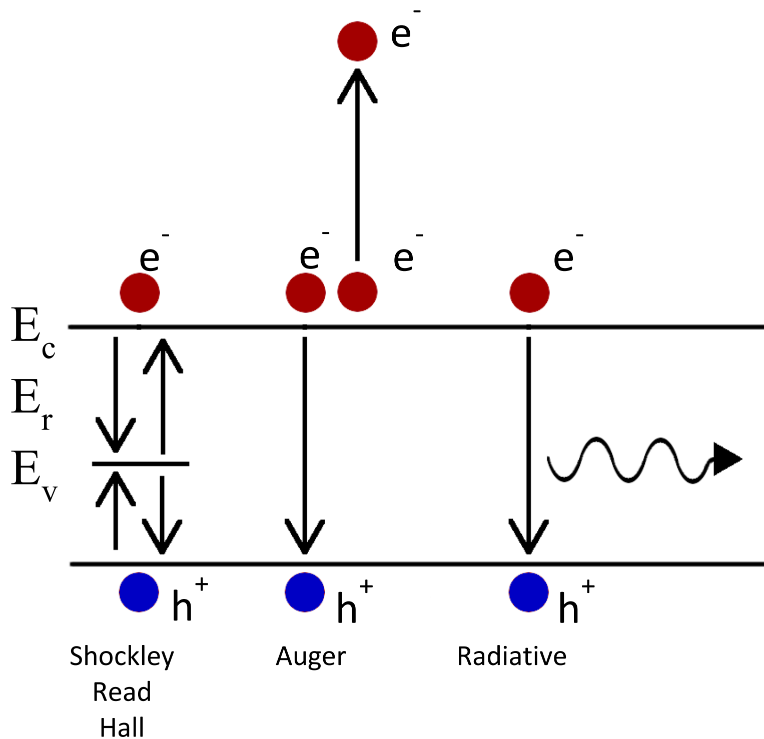

Figure 1.7: Shockley-Read-Hall, Auger and Radiative recombination mechanisms shown on a band diagram.

In the Auger recombination process the energy released from recombining carriers is transferred to another conduction electron, which is excited as the first electron relaxes. This excited electron is already in the conduction band, and thus no new carriers are created. The time from carrier generation to Auger recombination is called the Auger lifetime, τ_A.

Similar to Auger recombination, radiative recombination occurs when the energy of a recombination event is released as a photon. The released photon has energy equal to the band gap of the material. The radiative recombination process is essentially the opposite of carrier generation by photon absorption. The light emitted can be captured by a detector and used to measure relative rates of radiative recombination. The time from generation to radiative recombination is the radiative lifetime, τ_r. For indirect band gap materials radiative recombination is significantly less efficient compared to direct band gap materials, and can often be neglected for silicon.

Alternatively, electron-hole pairs can recombine by the Shockley-Read-Hall process. This process relies on the presence of energy levels in the band gap called impurity or defect levels. These energy levels are introduced by impurities or defects in the material, similar to donor and acceptor impurities but typically located closer to the middle of the band gap. If located near the conduction band, energy levels tend to trap electrons and if located near the valence band tend to trap holes. These levels are called electron or hole traps, respectively, and typically do not participate in Shockley-Read-Hall recombination. Impurity levels near the middle of the band gap efficiently trap both holes and electrons, forcing them to recombine. These levels are called deep level recombination centers due to their deep location in the band gap. Recombination energy is transferred in several steps as carriers move to these levels,

eventually lost to thermal energy. This process can dominate in impure materials such as photovoltaic grade silicon. Due to the effects of impurities on carrier lifetime by the Shockley-Read-Hall process, thermal treatments during photovoltaic cell fabrication must be understood to maximize post-processing carrier lifetime. The time from generation to Shockley-Read-Hall recombination is the Shockley-Read-Hall lifetime, τ_{SRH}.

Defect levels can also be introduced by dangling bonds resulting from crystalline dislocations introduced by thermal stress or mechanical work. In the context of silicon wafers, mechanical damage is typically introduced when the wafers are sawn from a crystal or when the surfaces are ion implanted for doping. Sawing leaves a field of dislocations penetrating several micrometers below the sawn surface as the cutting abrasive moves across the material. The nature and extent of this damage depends primarily on the details of the sawing process such as cutting rate, abrasive type, and the sawing technique employed.[28-32] Ion implantation also leaves a dislocation field produced by the impact of high energy ions. The nature of damage left by ion implantation is dependent on the species implanted, dose, and implant energy.[33] The effects of dangling bonds within a crystal can be reduced or eliminated through various treatments called passivation. Their electrical state can be changed by chemical interaction with hydrogen[34] which diffuses to the dislocation sites at elevated temperatures.

The aforementioned recombination processes all contribute to the total lifetime of carriers generated in a sample and are known as the bulk lifetime τ_b. The bulk lifetime and its relationship to the Auger, radiative and Shockley-Read-Hall lifetimes is given in Equation 1.3.[27] If one recombination process is unlikely then its lifetime will be high and its inverse will approach 0, thus having negligible effect on bulk lifetime. For those recombination processes

which occur more quickly than the others, the inverse lifetime will be much larger and will dominate bulk lifetime.

$$\frac{1}{\tau_b} = \frac{1}{\tau_A} + \frac{1}{\tau_r} + \frac{1}{\tau_{SRH}} \qquad \text{Equation 1.3}$$

Effective carrier lifetime

The bulk lifetime of a sample assumes the carriers are in a semi-infinite volume of material and never interact with surfaces. Of course this is not the case when considering the thin wafers used for solar cell substrates; thus the effective lifetime is not necessarily the same as the bulk lifetime. Recombination becomes much more likely at crystal edges such as grain boundaries or surfaces where defects and dangling bonds introduce defect levels and facilitate Shockley-Read-Hall recombination.[27] Therefore, the average carrier lifetime in a sample with limited dimensions can never reach that of a very large sample with no dimensional constraints. The effective lifetime τ_{eff} of a sample will depend on τ_b as well as sample dimensions and the recombination probability at the surface described by the surface recombination velocity S. These parameters are described by surface lifetime τ_s. The effective carrier lifetime τ_{eff} is related to the surface lifetime τ_s and bulk lifetime τ_b by Equation 1.4.[27] Equation 1.4 shows that if τ_s becomes very large, $\tau_{eff} = \tau_b$ and the measured lifetime is not affected by sample dimensions. As τ_s decreases, τ_{eff} will become completely dependent on τ_s. For thin samples with large S, τ_b can be neglected and $\tau_{eff} = \tau_s$, which is rather small in that case.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \qquad \text{Equation 1.4}$$

For a sample with one limiting dimension (such as a wafer) with surface recombination velocity S, thickness t and minority carrier diffusivity D τ_s can be calculated according to Equation 1.4.[35] This relationship shows that a high S will decrease τ_s to the extent that τ_{eff} is dependent only on the wafer thickness. Small S values will increase τ_s, and decrease the effects of thickness.

$$\tau_S = \frac{t}{2S} + \frac{1}{D}\left(\frac{t}{\pi}\right)^2 \qquad \text{Equation 1.4}$$

While D is a material constant and t is easily measured, S depends on sample surface conditions. Surfaces that are damaged by sawing, grinding or sandblasting have a very high S approaching infinity due to the high density of defects and dislocations just below the surface which dramatically reduce τ_s.[27] Once defects and dislocations below the surface have been removed by chemical etching or careful polishing, the dangling bonds at the silicon surface can be passivated to further reduce S. For silicon, passivation is typically performed by soaking in a solution of iodine and ethanol[36] or hydrofluoric acid[37] to temporarily passivate dangling bonds at the surface. Alternatively, one carrier type can be repelled from the surface by depositing a layer of material with a fixed charge in a technique called field-effect passivation.[38] In comparison to the other common passivation techniques, field effect passivation can reduce the effects of any electrically active defect, including dangling bonds. Field effect passivation offers a more permanent solution to surface passivation for photovoltaic devices.

By separating charge carriers excited by incident photons before the carriers recombine, the energy released by their recombination can be collected and used. Carriers of opposite charge can be separated using an electric field. Electrons will move opposite to the

electric field, while holes move in the same direction as the field. An electric field can be created across the surface of a semiconductor by forming a junction of p-type and n-type materials. Near this p-n junction, holes in the p-type side are drawn to the n-type side, and electrons to the p-type. This diffusion across the p-n junction leaves ionized dopant atoms with static charges on either side of the junction. The proximity of these charges to each other creates a built-in electric field. This field will only allow current to flow from the p-type to the n-type. This property is called rectification, and can only be overcome if sufficient voltage is applied to overcome the built-in electric field. The region between the two sides is called the depletion region or space charge region because carriers in that region diffuse out of the electric field and leave the region depleted of charge. If carriers are generated near a p-n junction on either side, one carrier can diffuse across and the other cannot. This separation of charge allows for collection of the energy of the excited carriers by connecting leads to either side of the p-n junction, thus producing power from incident photons.

Besides p-n junctions, a metal-semiconductor interface can also provide a rectifying barrier. If the Fermi level in the metal is higher than the conduction band in the semiconductor, electrons can flow freely from the metal to the semiconductor due to the drop in energy level. Carriers also move from the semiconductor to the metal due to the absence of band gap in the metal. If the Fermi level of the metal is lower than that of the semiconductor, electrons can still pass from the semiconductor to the metal but electrons in the metal do not have sufficient energy to enter the conduction band of the semiconductor. Because holes rely on the opposite flow of electrons, the opposite is true for hole carriers. This prevents current from flowing from the semiconductor to the metal, and allows current to flow from the metal to the semiconductor.

Such a barrier is referred to as a Schottky barrier or Schottky contact. Schottky barriers can be created as test structures on sample surfaces, allowing for the testing of many electrical properties. Unlike p-n junctions, Schottky barriers do not require high temperature processing.

Objective

To increase the value of their solar cell products, SunEdison, a SiSoC industrial member, has employed a *Continuous*-Czochralski crystal growth process to produce silicon wafers. This goal has motivated the current study to investigate the physical properties of *C*-CZ silicon and their impact on silicon photovoltaic performance. By employing a *C*-CZ growth process for the production of photovoltaic substrates, SunEdison's goal is to increase the efficiency of their solar cells as well as decreasing cost. This study examines material properties of novel *C*-CZ wafers which affect minority carrier lifetime and solar cell efficiency. Comparing minority carrier lifetime measured using various optical and electrical techniques before, during and after solar cell fabrication allows for identification of issues which may affect minority carrier lifetime in the resultant solar cell. It is anticipated that the results of this study will reduce the cost of photovoltaic energy produced by *C*-CZ solar cells, increasing the efficacy of renewable solar energy.

CHAPTER II: METHODS

Sample acquisition and preparation

Four sets of wafers taken from two crystals grown consecutively from the same crucible by the *C*-CZ method were provided by SunEdison. Sample sets (in order from seed to tail) B3, B5, and B7 were taken from one crystal while Sample set CD was taken from a later crystal grown from the same melt. Each set of wafers was sawn from the same short segment of the crystal, so properties of wafers from the same segment are assumed to be the same. SunEdison used thick slices cut from the ends of each sample segment to determine resistivity ρ, donor concentration N_d and minority carrier (hole) lifetime τ_h. Concentrations of interstitial oxygen and substitutional carbon impurities were also determined by Fourier transform infrared spectroscopy using ASTM standards.[39-40] The characterization slices were then annealed at 700°C for 20 min and quickly cooled to room temperature in order to annihilate thermal donors present in the slices. The resistivity was measured again so that the donor concentration due to the phosphorus donors only could be estimated. The difference in N_d before and after anneal would then indicate the concentration of thermal donors. These properties determined by SunEdison are provided in Table 2.1. The crystals were grown under experimental conditions in which dopant levels were varied, accounting for differences in N_d between segments.

Table 2.1: Wafer properties measured by SunEdison

Segment ID	ρ pre-TDA (Ω-cm)	ρ post-TDA (Ω-cm)	Average [P] (10^{14} cm^{-3})	Average [TD] (10^{14} cm^{-3})	Lifetime Range (μs)	[O_i] Range (10^{16} cm^{-3})	[C_s] Range (10^{16} cm^{-3})
B3	2.21	2.70	17.1	2.00	4757-4663	63.8-63.7	2.35-2.65
B5	2.84	3.76	12.1	2.05	4663-4675	62.5-63.7	2.65-2.57
B7	3.52	5.38	8.39	2.31	4695-4349	62.5-63.1	2.57-2.68
CD	12.38	19.70	2.23	0.670	4373-4037	63.2-63.0	3.62-3.42

Samples smaller than the whole wafers were removed by cleaving the wafers into rectangular pieces. Wafer samples are referred to by their location relative to the top of the stack received, with wafer 1 being on the top and wafer 50 on the bottom. For example, CD-01 refers to the first wafer of segment CD.

Surface polishing

Sample polishing techniques varied over the course of this study based on the purpose of polishing and the materials available. In general, a small sample was cleaved from the desired location of the wafer and its unique sample ID scribed into one side. The sample was then mounted with the inscription down on a polishing mount by heating the mount and applying mounting wax. Round mounts ~4 cm in diameter were used for automated or manual polishing, while custom 1.2 x 7 cm^2 mounts were used to polish longer strips. Automatic polishing was performed using a Buehler Ecomet II Grinder/Polisher equipped with 8 inch, 600 grit grinding discs, followed by 1200 grit paper and finally a 0.05 μm Syton colloidal

amorphous silica solution. Manual polishing was performed on a LECO 8 inch grinding/polishing station using similar grinding discs. Afterwards, various diamond and alumina polishing suspensions were used on nylon cloth before finishing with Syton. Select wafers were also prepared by Aptek Industries, in which 30 μm was ground away from one surface which was then finished with a high quality polish.

Chemical etching

All chemical etching was performed in a fume hood with appropriate protective equipment for safety. Before chemical etching, each sample was rinsed in deionized water, followed by a heated soak and a final rinse in acetone. This wash was repeated with methanol and deionized water. For some etches, the sample was chemically oxidized using a Piranha solution (see Table 2.2) and/or rinsed in a fresh 7% HF solution to remove surface oxide and impurities just prior to subsequent etching. After etching, the sample was quenched by adding excess deionized water to the etch solution while dumping, or moving the sample to a beaker with deionized water or dilute sodium bicarbonate solution to stop the etch process. After at least one more rinse in deionized water, the surface of interest was dried with a jet of dry nitrogen or compressed air. The recipes in Table 2.2 describe the various etchants used. Note that many of the chemicals are toxic or hazardous and must be used only with proper training and protection.

Table 2.2: Chemical Etchants

Etchant	Composition	Uses	Notes
Piranha	~50% Sulfuric Acid (H_2SO_4) ~50% Hydrogen Peroxide (H_2O_2 30%)	Remove metallic impurities, form oxide layer	Soak for several minutes to hours at 25-100°C. Peroxide rapidly oxidizes surface, catalyzed by acid. Hydrogen gas bubbles form during reaction, sometimes causing samples to float.[41]
HNA	50% Glacial Acetic Acid (CH_3COOH >99.5%) 32% Nitric Acid (HNO_3 70%) 18% Hydrofluoric Acid (HF 49%)	Isotropically etch silicon for wafer thinning and polishing	HNO_3 oxidizes silicon which is attacked by HF, diluted with acetic acid. Etch rate ~10 µm/min, isotropic removal results in polished surface. Brown gas and excess heat released.[42]
KOH	Potassium Hydroxide (KOH >99%) Deionized Water	Wafer thinning or texturing	Concentration and temperature determine the total and relative etch rates of different crystal planes. 40 wt% at 80°C produces a more isotropic etch at ~1 µm/min, dilute and cooler solutions texture the surface.[41]
Schimmel	66% Chromic Acid (H_2CrO_4 0.75 M) 33% Hydrofluoric Acid (HF 49%)	Reveal sub-surface damage	Attacks {110} and {111} planes preferentially, making this etch ideal for defects on {100} surfaces.[43]
Secco	66% Potassium Dichromate ($K_2Cr_2O_7$ 0.15 M) 33% Hydrofluoric Acid (HF 49%)	Delineate defects and dislocations	Etches at ~1.5 µm/min, 3 to 5 min typical etch time. Reveals slip planes, low angle grain boundaries, stacking faults, and twin boundaries on the (100) plane. Ultrasonic agitation during etch is necessary to properly remove bubbles.[44]

Differential interference contrast (DIC) microscopy

DIC microscopy, or Nomarski microscopy, uses offset polarized images to give the illusion of depth to features that otherwise appear flat. Although DIC microscopy is traditionally used to study thin transparent samples such as biological material, it is used in the semiconductor industry to quickly observe etch pits and other features on a flat reflective surface such as polished silicon. In the DIC microscope, the beam of light from the source is collimated and split into two beams, one polarized 90° and slightly offset from the other. Both beams are incident on a reflective sample surface, where small deviations in topography lead to phase shifts in the polarized images. These two polarizations are then rotated by a prism to produce interference between the two. The polarization can be rotated by manually turning the prism.

Because the images are slightly offset, regions where the phase shift (and topography) changes will be dark due to destructive interference on one side and bright due to constructive interference on the other side. This effect gives the optical illusion of a light source shining on the bright side of the feature and a shadow cast across the dark side. The apparent position of this light source can be moved from one side of the sample to the other by rotating the prism, sometimes called sunrise and sunset conditions. Besides assisting in the interpretation of topography to the human eye, DIC microscopy greatly enhances topographical contrast and separates raised from impressed features (bumps vs. pits) using only optical microscopy. In this study DIC microscopy was performed using a Carl Zeiss Differential Interference Contrast Microscope.

Vickers microhardness and fracture toughness

The Vickers microhardness test measures the hardness of a flat surface by pressing a pyramid-shaped diamond tip into the surface under an applied load. Vickers microhardness H_V is calculated by dividing the indentation load L by the measured area of indentation A:

$$H_V = \frac{L}{A} \qquad \text{Equation 2.1}$$

In this study, a Buehler Microhardness tester equipped with a Vickers diamond tip was used at 100 g or 50 g mass to apply load. Area of indentation was measured using scanning electron microscopy.

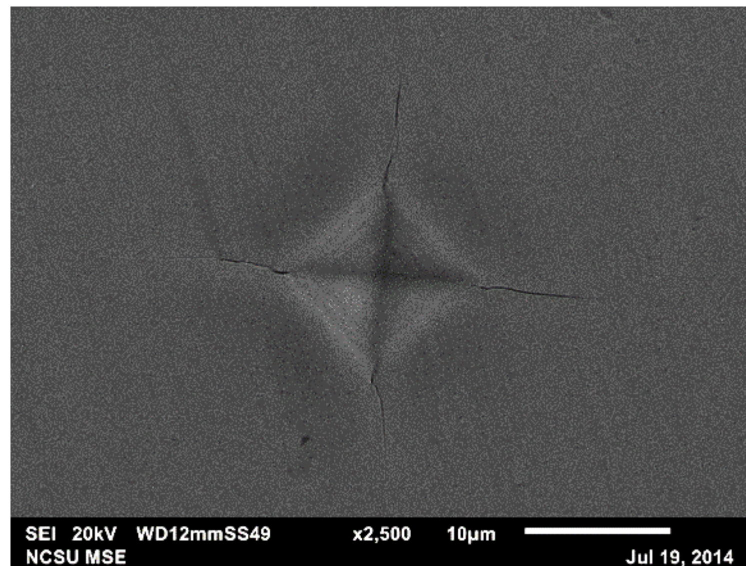

Figure 2.1: Scanning electron micrograph of a microindent representative of those used to calculate hardness and fracture toughness. Notice the cracks propagating from the corners of the indent.

For brittle materials such as silicon, the Vickers microhardness indentations also produce cracks radiating from the indent corners. Previous reports[45-46] have shown that the

average length of these cracks c can be used to estimate fracture toughness K_{IC} according to Equation 2.2:

$$K_{IC} = \alpha \left(\frac{E}{H_V}\right)^{\frac{1}{2}} \frac{P}{c^{\frac{3}{2}}} \quad \text{Equation 2.2}$$

where α is a geometrical constant (0.016 for the Vickers diamond tip), E is the elastic modulus, and P is applied load. K_{IC} was calculated for each sample segment by measuring crack lengths radiating from each indentation using scanning electron microscopy.

Angle polishing

Angle polishing removes material from a sample at a shallow angle to allow for the macroscopic study of the microscopic structure near the sample surface using an optical microscope. This technique is useful in depth profiling of defects because more area is exposed per depth leading to more visible features. An angle-polished surface is useful in measurements of junction depth, defect distribution, and damage depth from sawing or texturing.

ASTM standard F950-02[47] was followed for damage depth measurements. Angle polishing was performed using a polishing jig consisting of a hollow, cylindrical brass guide, a solid stainless steel cylinder which slides in the guide only loose enough to slide freely, and an angled sample mount which fastens to the latter cylinder. The sample is mounted such that one edge of the sample is presented to the polishing surface at a shallow angle. The polishing jig setup is illustrated in Figure 2.2. To protect the top surface and ensure an edge without rounding, approximately 1 μm thick SiN_x was deposited on the sample surface by plasma-enhanced physical vapor deposition. The sample was fixed to the polishing mount using

cyanoacrylate epoxy with two dummy wafers fixed on top of the sample by the same method. The two top wafers and extra epoxy ensure that the polished sample surface is very flat with a sharp angle. Once mounted, the sample is polished as previously described using Syton for only ~5 min to prevent the solution from etching the interface.

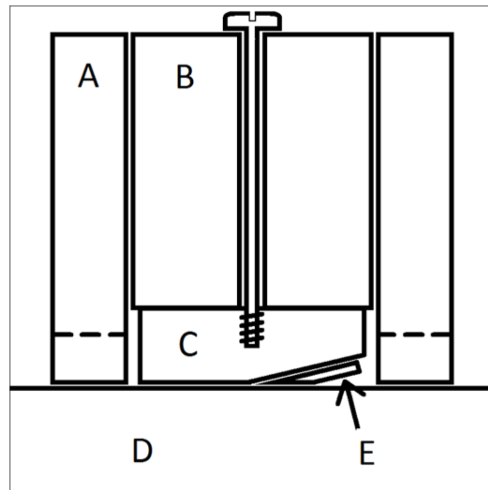

Figure 2.2: Schematic depicting angle polishing jig, featuring the brass guide (A), inner cylinder (B), angle polish sample mount (C), polishing surface (D), and mounted sample (E).

Once polished, the epoxy was removed by soaking in acetone overnight and cleaning thoroughly. The sample was chemically polished by soaking in Piranha solution for several minutes followed by an HF dip, and Schimmel etched for 3 min to delineate dislocations. The polished angle was measured and quality of the interface was confirmed by scanning electron microscopy. DIC microscopy was used to observe the etched surface by placing the etched sample loosely on the polishing mount to maintain the polished surface in the focal plane.

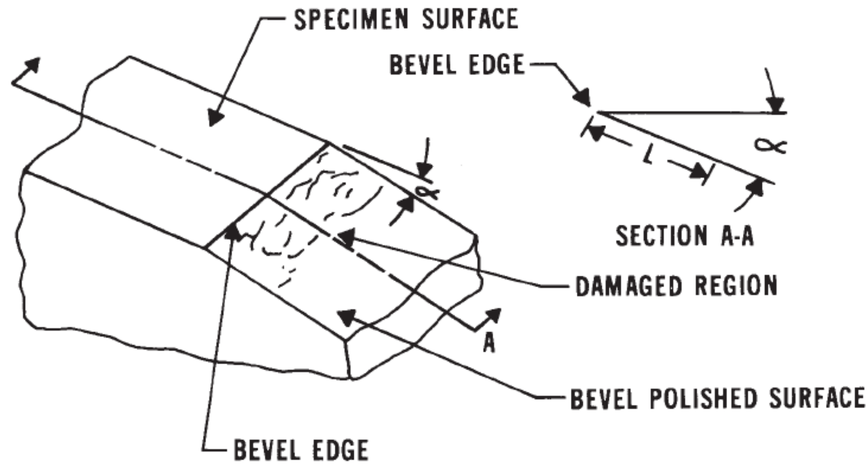

Figure 2.3: Diagram illustrating measurement of damage and polished angle α. Reproduced from Reference 47.

Using the polished angle α measured by scanning electron microscopy, a right triangle is formed with one side *d* perpendicular to the surface representing the depth of damage and the hypotenuse formed by the length of deepest damage *L* (see Figure 2.3). Depth of damage *d* can be calculated by the following:

$$d = L \sin(\alpha) \qquad \text{Equation 2.2}$$

Scanning electron microscopy (SEM)

SEM uses electrons to image a sample, as opposed to photons in an optical microscope. Electrons used for imaging are ejected into the SEM column using an electron gun. The freed electrons are accelerated down a column in vacuum toward the sample by means of high tension called the accelerating voltage and manipulated along the way by magnetic fields. Round electromagnetic lenses focus the beam while scan coils deflect the beam across the

sample. This electron beam is focused on the surface of a sample, generating secondary electrons. The focused electron beam is rastered across the sample by scan coil deflection, and a secondary electron detector collects the image. Secondary electrons yield images that are easy to interpret because of their similarity to photographs. Features facing the detector appear bright due to their increased collection while features facing away yield less signal and appear dark or shadowed. The point of perspective is from inside the objective lens where the beam is focused. This allows for topographical analysis of etched samples, but the bias applied to the detector means secondary electrons generated in shallow features on a flat surface will be captured equally, yielding little or no contrast. Scanning electron micrographs were collected throughout this study using a JEOL 6010LA InTouchScope.

Four point probe

The four point probe measurement is used to quickly apply a test current to a sample and measure the resulting voltage from which sheet resistance can be determined, allowing for determination of resistivity. Four sharp probes, each separated by probe spacing s, are arranged in a linear fashion and pressed onto the surface of a sample. Current I is applied across the outer two probes by a current source, while voltage V is measured across the inner two probes using a voltmeter. The schematic of a four point probe measurement system is shown in Figure 2.4. Assuming Ohmic behavior characterized by a linear I-V relationship, Equation 2.3 can be applied to I and V to determine sheet resistance R_s. The resistivity ρ can then be determined by Equation 2.4 using the measured sheet resistance and thickness t. Therefore, the four point

probe measurement may be used to determine resistivity if thickness is known, or thickness if resistivity is known.

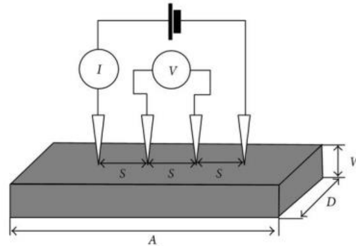

Figure 2.4: Schematic depicting the four point probe measurement technique. [48]

$$R_s = 4.532\frac{V}{I} \quad \text{Equation 2.3}$$

$$\rho = R_s t \quad \text{Equation 2.4}$$

The above technique is accurate for thin or thick samples of semi-infinite area. As real samples deviate from these conditions, correction factors must be applied. Due to the number and complexity of the various correction factors, they will not be discussed in detail here. Such corrections can be made by referencing published works on the subject, such as that by Schroder.[49]

To measure a wafer by four point probe a sample wafer is cleaved sufficiently large to avoid edge effects. The sample is rinsed in acetone and methanol to remove organic deposits and dipped in dilute HF to remove any surface oxide. The cleaning ensures the surface presented to the probe head is the same for all samples and sample regions. To ensure a linear relationship between current and voltage, sheet resistance was measured on one sample using

a range of values for current. In this study 1 mA of current across the outer probes was used to measure resistance. A correction factor was applied to account for proximity to sample edges with a value of 0.85 near the sample edge and approaching 1 within approximately 1 cm.

Schottky barrier preparation

The formation of a Schottky barrier on a sample surface allows for electrical characterization techniques such as capacitance-voltage, deep level transient spectroscopy, and electron beam induced current measurements. Gold was selected as the Schottky barrier metal for this study because it forms a rectifying contact with n-type silicon. Gold deposition was performed via a thermal evaporation technique. Polished samples dipped in HF within 1 hour were taped to a stainless steel mask using carbon tape. Holes in the mask 1 mm in diameter allow for the formation of diodes of the same size on the silicon surface. The masked samples were secured in the evaporation chamber face-down with a weight, and were approximately 15 cm above a tungsten filament boat. A charge of gold was placed in the boat, and a shutter positioned between the samples and boat. The evaporation chamber was sealed and evacuated to a pressure of 10^{-5} - 10^{-6} torr, and gold was evaporated by increasing the current applied across the boat. Once a steady temperature was reached and any volatile impurities evaporated, the shutter was moved to expose the sample to the gold source. Once formed, diodes were stored in the same vacuum chamber to prolong useful life, which was usually 5-10 days after evaporation.

Capacitance-voltage measurement

Carrier concentration N_c can be calculated by varying voltage V over a reverse-biased Schottky barrier or p-n junction by varying the space charge region width and measuring the resulting change in capacitance C. As the reverse bias is increased, the width of the space charge region will increase as well. The absence of charge carriers between the metal contact and the bulk semiconductor (in the case of the Schottky barrier) leads to a parallel plate capacitor-like behavior. As in a parallel plate capacitor, the capacitance decreases with increasing width. This relationship is used to determine the slope of C^{-2} vs V, dC^{-2}/dV, which is used along with the area of the barrier A, dielectric permittivity constant ε, permittivity of free space ε_0, and carrier charge q in Equation 2.5:

$$N = \frac{2}{q\varepsilon\varepsilon_0 A^2\left(\frac{dC^{-2}}{dV}\right)} \qquad \text{Equation 2.5}$$

Because of the strong dependence on Schottky barrier area, significant error can be introduced if the area is not known with great precision. For a more complete explanation of the capacitance voltage measurement, see Chapter 2 of Semiconductor Material and Device Characterization by Schroder.[27]

When performing Deep Level Transient Spectroscopy (DLTS), N_c at the local region of the test diode must be known so a capacitance-voltage measurement is made on each gold Schottky barrier using the BioRad DL8000 Deep Level Transient Spectrometer probing station and Boonton Capacitance Meter. Capacitance is measured over the voltage range from -5 to 0 V, and the area used in calculation is taken as the area of the mask holes, which were 1 mm in diameter.

Deep level transient spectroscopy (DLTS)

DLTS describes a system of measuring capacitance differentials over a rectifying contact at various temperatures.[50-51] Peaks in differential capacitance, or capacitance transients, indicate a defect energy level in the semiconductor band gap. Analysis of the peaks allows for determination of trap concentration, activation energy, concentration depth profile and capture cross-section. Some impurities can be detected in concentrations as low as 10^9 cm^{-3}, which enables for otherwise undetectable impurities to be studied.[51] Therefore, DLTS is a critical technique in the study of electrical defects in impure semiconductors such as solar silicon.

The DLTS signal arises from the change in capacitance across a reverse-biased or unbiased diode as minority or majority carriers are captured. In pulse-bias mode, reverse bias is quickly applied to a diode to create a depletion region and thus capacitance over the diode. As the bias is removed and the carriers return to equilibrium, the rate at which the depletion region is refilled with carriers is dependent on the presence and nature of traps within the depletion region. To measure the change in capacitance for a given measurement, two measurements are made across a "rate window", and the difference between the two is the capacitance transient. For a given trap, the capture and emission rate, and therefore the capacitance decay is dependent on temperature. Figure 2.5 demonstrates this principle, showing the formation of a peak in the plot of capacitance transients vs. temperature. Notice the effects of varying the location of the rate window.

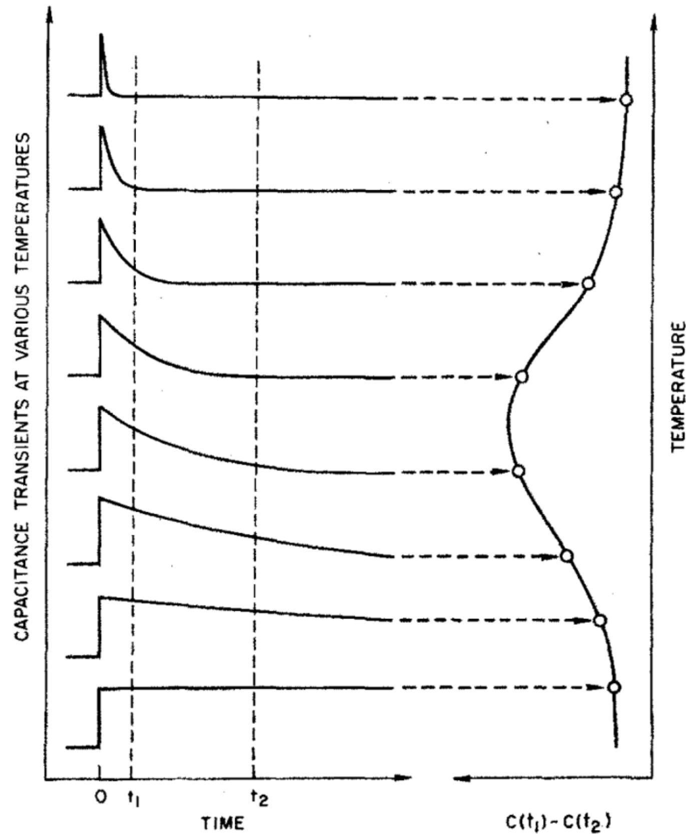

Figure 2.5: Demonstration of DLTS peak formation based on changing capacitance transient measurements. Reproduced from Reference 50.

From this peak in capacitance transients, the activation energy and capture cross-section can be obtained by comparing the thermal emission rate of the trap to temperature for several points in the curve. Trap concentration can be determined on the basis the intensity of the trap peak.

The defect states characterized by this technique are located only in the depletion region of the biased diode and allow for the determination of depth of the trap sampled relative to the junction. By varying constant bias U_b and pulse bias U_p, different depths of the sample can be observed. In this manner, a concentration profile of traps along the depth of the sample can be

constructed. Due to the complexity of calculating trap characteristics from a DLTS scan, the mathematics behind calculation are not discussed here. For a complete discussion of the DLTS technique, see Benton[51] or Lang.[50]

The DLTS measurement is made by mounting a diode sample such as a Schottky barrier or p-n junction to a stage on a cryogenic cold finger and probing the top contact. The sample chamber is pumped to 10^{-2} torr to allow for low temperature scanning and kept dark to prevent the photovoltaic effect on the sample. Temperature is stepped up or down for each measurement or ramped continuously if the rate is slow enough. Measurements are made with a precision capacitance meter, and calculations are all performed using instrument software.

DLTS was performed at NCSU using a BioRad DL8000 Deep Level Transient Spectrometer System equipped with a helium compressor capable of reaching 18 K and a Boonton Capacitance meter. DLTS was performed at the University of Manchester by Dr. Markevich using TrapView software and a helium-cooled stage under vacuum controlled by a Lakeshore 340 temperature controller and UMIST Capacitance meter. Schottky barriers were formed on polished samples as described above, and the back of each sample was scratched with a diamond scribe to break any oxide layer. The backside of the sample was then coated in InGa liquid eutectic metal and bonded to the stage using either silver paste or more eutectic metal. A probe was placed on the diode of interest, and secured with a very small amount of silver paste or eutectic metal. After probing, the leakage current and capacitance of the diode were checked to ensure suitable contact. Capacitance-voltage measurements were made to determine carrier concentration N_c, and a current vs. voltage curve was collected and used to determine the ideality factor of the diode. The desired U_b and U_p biases, pulse width t_p and

period width were set. The sample stage was placed under vacuum and scanned from 300 K to 20 K.

Electron beam induced current (EBIC)

The EBIC technique is a measurement of excess carriers generated in a semiconductor sample by an incident electron beam. When high-energy electrons such as those used in an SEM impact a semiconductor, most of the electrons are absorbed by the material, which results in valence electrons being ejected to produce an electron-hole pair. The number of electron-hole pairs generated per incident electron is approximated by dividing the beam energy, typically 1 - 20 keV, by the bandgap of the semiconductor (1.12 eV for silicon). Even a modest beam current generates significant excess carrier concentrations, most likely into a state of high injection. However, these carriers will simply recombine if not collected. The EBIC signal relies on some sort of a rectifying barrier such as a p-n junction or Schottky barrier to collect the current. Therefore, EBIC can only be performed on or near such rectifying structures. The EBIC signal is collected at each scanned point of the SEM image, allowing for the parallel collection of EBIC and secondary electron images.

For electron beams incident directly on a rectifying junction, the probability of collection of the generated carriers approaches unity. However, the collection probability decays as the beam travels farther from the junction. At a distance x from the junction, the probability of collection is dependent on all factors which affect the recombination of excited carriers. Of course, the minority carrier lifetime τ affects collection probability away from the junction because carriers need time to travel. In addition, because carriers are generated very

close to the surface by the electron beam (see Figure 2.6), the surface recombination velocity S_e and S_h of electrons and holes, respectively, is also a key factor in calculating collection probability. Bonard and Ganière[52] have mathematically analyzed the collection efficiency as a function of distance away from an interface using a model of an electron beam with electron range σ_x in the x-y plane and σ_z in the z direction, incident onto a sample surface with respective electron and hole surface recombination velocities S_e and S_h. The sample has hole and electron diffusion lengths L_h and L_e, respectively, with a p-n junction parallel to the beam and perpendicular to the scan direction that has a width of d_j and is located a distance x from the incident beam. A schematic of the experimental configuration is illustrated in Figure 2.6, and the resulting EBIC data are analyzed using Equation 2.6. For a more complete treatise on the topic including all calculations, see Reference 52.

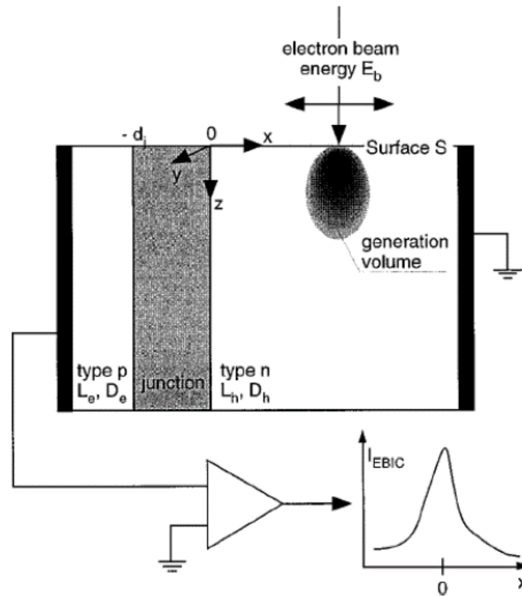

Figure 2.6: Sample geometry used in the EBIC analysis of τ and $S_{e,h}$ with the Bonard Ganière model, Equation 2.6.

Lifetime is not directly used in the Bonard Ganière model but is directly related to minority carrier diffusion length and diffusivity, respectively L_h and D_h, in the case of n-type silicon according to Equation 2.7. By fitting a curve of collection probability to an EBIC intensity scan travelling perpendicular to a rectifying barrier on n-type material, both τ and S_h can be determined in the same measurement by curve fitting. This gives EBIC a unique advantage in lifetime measurement because all other quantitative lifetime measurements require some knowledge of S for interpretation of bulk lifetime from effective lifetime.

$$\eta(x) = \frac{1}{\pi}\int_0^\infty \left[\frac{S_h}{D_h}\upsilon_h(k,x) + \frac{S_e}{D_e}\upsilon_e\big(k,-(x+\ d_j)\big)\right] dk + 0.5\left[erf\left(\frac{x+d_j}{\sigma_x}\right) - erf\left(\frac{x}{\sigma_x}\right)\right]$$

Equation 2.6a

where

$$\upsilon_{h,e}(k,x) = \frac{1}{k^2 + \left(\frac{S_{h,e}}{D_{h,e}}\right)^2} erfc\left[\frac{\sigma_x}{2}\left(\mu\big(k,L_{h,e}\big) - \frac{2x}{\sigma_x^2}\right)\upsilon b\right] \cdot \exp\left[\frac{\sigma_x\mu\big(k,L_{h,e}\big)}{2}\right]^2 \cdot \exp\big[-\mu\big(k,L_{h,e}\big)x\big]\frac{1}{(1+k^2\sigma_z^2)^3} \cdot \left[1 + 3\frac{S_{h,e}\sigma_z}{D_{h,e}} - k^2\left(\frac{S_{h,e}\sigma_z^3}{D_{h,e}} + 3\sigma_z^2\right)\right]$$

Equation 2.6b

and

$$\mu(k,L) = \sqrt{k^2 + \frac{1}{L}}$$

Equation 2.6c

$$\tau = L_h^2 D_h$$

Equation 2.7

EBIC measurements were performed using a Gatan SmartEBIC system installed on a JEOL JSM 6400 SEM. In place of a p-n junction oriented parallel to the electron beam, Schottky contacts perpendicular to the beam deposited on the sample surfaces were used to provide full collection efficiency. Aluminum foil was used to create a mask with a straight,

sharp edge which was used to form gold Schottky barriers that would be ideal for EBIC lifetime measurement. The sample was mounted using conductive carbon tape onto the EBIC stage, and the Schottky barrier was probed using one of the two stage probes. The EBIC signal of both probes is combined for the final signal, allowing for two samples to be tested at a given time. First, a digital EBIC image of a probed barrier and surrounding area was collected and saved. ImageJ software was then used to construct a scaled line intensity plot perpendicular to the edge of the barrier, such that the constant intensity of the barrier as well as the decaying intensity along the bare sample surface is captured. Approximately 20 line scans from each sample were imported into Microsoft EXCEL where they are normalized for a maximum intensity of 1 and shifted such that the maximum intensity at the interface is located at $x = 0$. With all scans lined up, they are averaged for the final profile for decay of intensity. This method gives a better representation of the sample than a single line scan and reduces noise in the signal. The intensity profile was then opened in MATLAB, and a simulated EBIC profile of intensity was fitted to the data with a modified code provided by Dr. Chad Parish using manual fitting and the MATLAB Curve Fitting Toolbox.

Bonard and Ganière use tabulated values for the electron ranges based on material and accelerating voltage. However, Parish and Russell[53] showed that beam diameter has a significant impact on σ_x. Particularly on the JEOL 6400 SEM used, maximum resolution was limited due to environmental interference, which is indicative of a large beam diameter. As a solution, Parish and Russell showed that Monte Carlo simulations of electron beam energy loss using CASINO software can be used to directly calculate electron ranges taking beam diameter into account to improve accuracy in simulation.

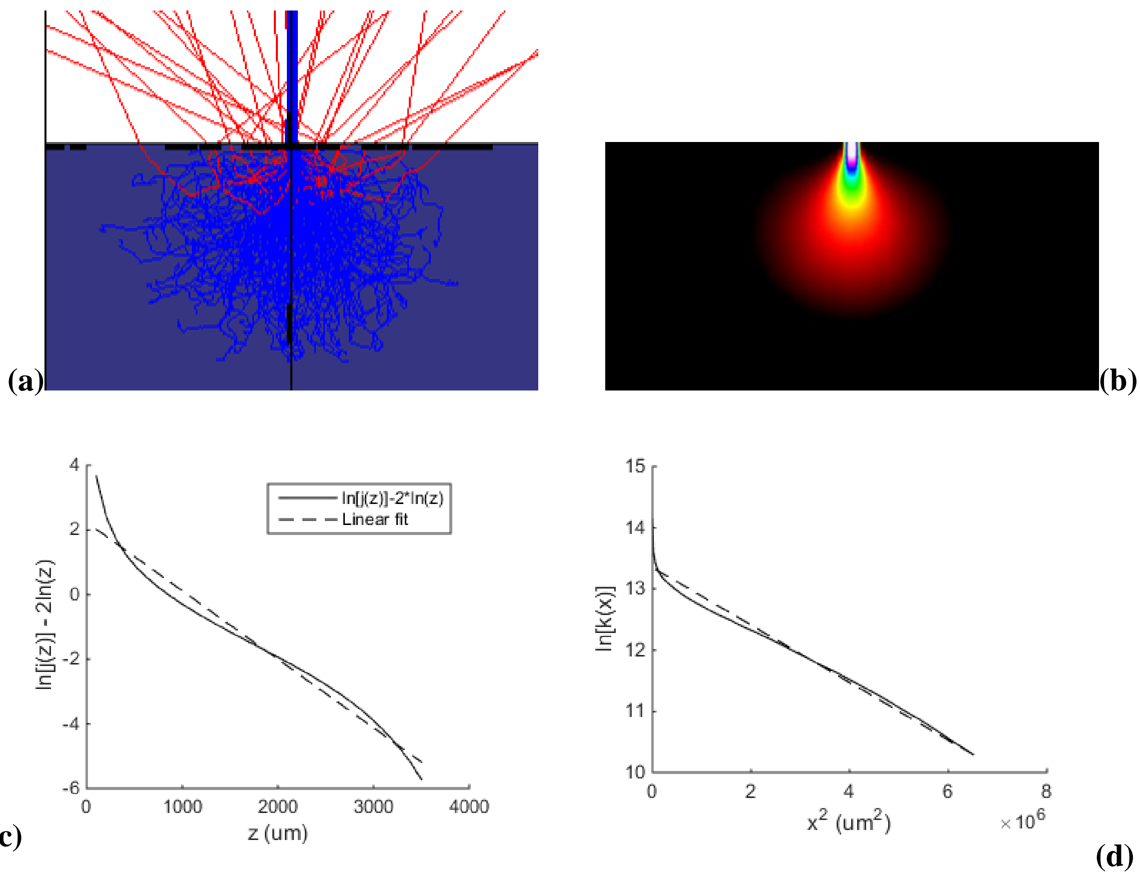

Figure 2.7: **(a)** CASINO simulation of 160 nm wide electron beam incident on a silicon surface at 19 keV. Red lines are backscattered trajectories, blue lines are absorbed electrons, and blue background is silicon. The visible sample is 4 µm deep and 8 µm wide. **(b)** Energy loss distribution calculated by CASINO simulation in **(a)** with the same dimensions used to calculate σ_x **(c)** and σ_z **(d)**.

For each image studied, a sharp feature such as a cleaved silicon edge hanging over a region of much lower contrast was used to measure beam diameter. An intensity profile was made perpendicular across the edge using ImageJ software, and the distance between the pixel of 80% maximum edge contrast and 20% maximum edge contrast was taken as an estimate of the beam diameter. CASINO 3D software was then used to simulate 10^6 electrons with the

beam energy from the accelerating voltage incident on a silicon cube of large enough dimension that all or almost all of the incident electrons (excluding backscattered) are captured in the volume. A three-dimensional map of electron energy loss was exported from CASINO to MATLAB, which was summed over the y and z axes to yield energy absorption along the x axis $k(x)$ and summed over x and y axes to yield energy absorption along the z axis $j(z)$. The slopes of $ln[k(x)]$ vs. x^2 and $ln[j(z)] - 2ln(z)$ vs. z were used to calculate σ_x and σ_z for each image by Equations 1.11 and 1.12.[53] A summary of the CASINO results for an example sample is presented in Figure 2.7. These ranges were then used with Equation 2.6 to simulate the EBIC intensity profile.

$$\sigma_x = \sqrt{-\frac{d(x^2)}{d\ln[k(x)]}} \qquad \text{Equation 2.8}$$

$$\sigma_z = -\frac{dz}{d(\ln[j(z)] - 2\ln(z))} \qquad \text{Equation 2.9}$$

Reverse bias recovery testing

Reverse recovery of a p-n junction diode directly measures the time that generated carriers spend before recombining in the depletion region of the junction. In a forward biased p-n junction, the space charge region is filled with injected charge carriers, allowing current to flow. In reverse bias, this space charge region is devoid of carriers, thus only a rectifying current in the reverse direction. When the p-n junction is rapidly switched from forward current to reverse current, the injected charge carriers are still present and the diode will therefore yield full conduction in the reverse direction for some period without rectification. As carriers recombine, the junction bias will decrease. When the junction bias reaches 0, the current

permitted to flow in the reverse direction begins to decay until it reaches the steady-state reverse bias current. The time between bias switching and recovery of reverse current is the reverse recovery time t_{rr}. Although the definition of t_{rr} varies and different methods of measuring t_{rr} from different pulse shapes exist,[27, 54] this work takes t_{rr} to be the time of 10% of the maximum reverse current along the decay region of reverse current.

Reverse recovery testing requires a p-n junction, and therefore could only be performed on p-n junction diode samples formed by the lithography technique discussed in Appendix A. The circuit diagram of the test is shown in Figure 2.8. The top AlSi contact was probed with a copper wire wet with InGa eutectic such that current could pass through the copper or eutectic, whichever path minimizes capacitance. The rear contact was made by placing the sample on a drop of InGa eutectic on a copper stage, which was scratched through the eutectic to ensure good contact. In making all connections, good contact was ensured and interfaces of differing metals in the circuit were avoided in order to minimize capacitance from Schottky effects.

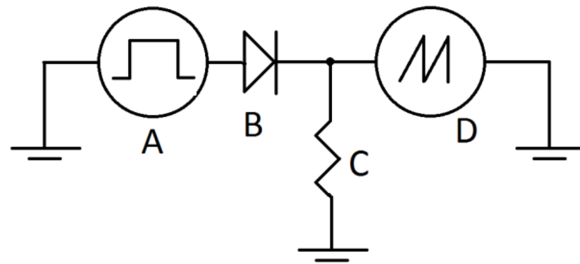

Figure 2.8: Reverse recovery measurement circuit using (A) pulse generator, (B) test diode, (C) 1000 Ω resistor, and (D) oscilloscope.

(a)

(b)

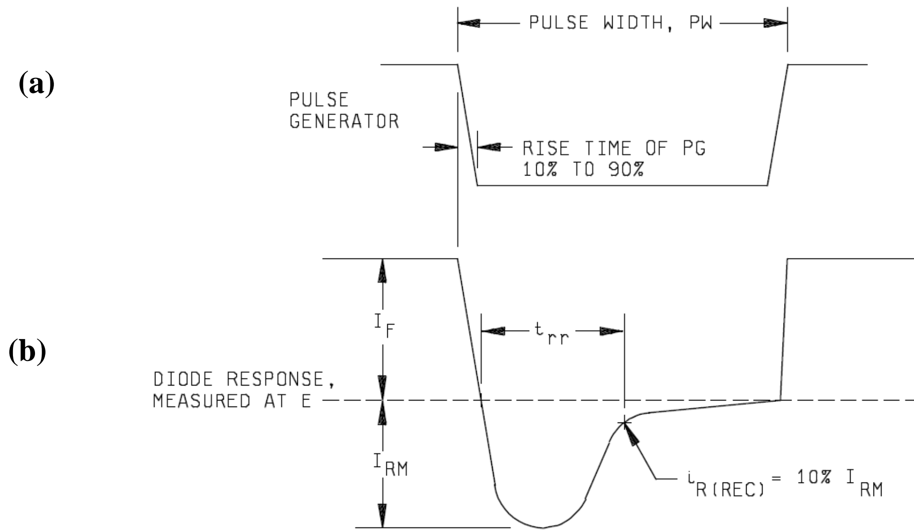

Figure 2.9 (a): waveform applied to the test diode in Figure 2.8 using a pulse generator, note that bias is switched from forward to reverse. **(b)**: expected current response from the diode, indicating the measurement of t_{rr}.[54]

Figure 2.9 shows the waveform applied to the test circuit along with an example of a typical waveform expected on the oscilloscope. The charge storage time t_s (not shown) represents the time from current switching to the onset of decay and can be used to calculate lifetime τ according to

$$erf\sqrt{\frac{t_s}{\tau}} = \frac{1}{1+\frac{I_f}{I_r}} \qquad \text{Equation 2.10}$$

where *erf* is the error function, and I_f and I_r are the steady state forward current and maximum reverse current, respectively. The reverse recovery time t_{rr} is also measured on the oscilloscope screen along with the time from current switching to peak reverse current t_p. These times are then used with Equation 2.10 to approximate minority carrier lifetime τ:

$$\tau \approx \sqrt{t_p t_{rr}} \qquad \text{Equation 2.11}$$

CHAPTER III: MATERIAL ANALYSIS OF *C*-CZ WAFERS

Stress and crystal defects

The quality of silicon crystal grown by the *Continuous*-Czochralski process was investigated by studying the presence of crystal defects within *C*-CZ wafers using several techniques. Crystal defects were revealed by preferential etching of pristine surfaces and the resulting etch pits were observed by DIC microscopy and SEM. Raman spectroscopy, the obvious choice for measuring stress in silicon, was attempted but inconsistencies with spectrometer calibration indicate that stress measurements are very inaccurate, so they will not be included in this discussion. The presence of dislocations resulting from residual thermal stress was investigated using nanoindentation scans of each sample segment by colleagues Schiessl and Dr. Youssef along the wafer radius where stress is expected. These nanoindentation scans were compared to Vickers microhardness measurements made in select sample regions.

Preferential etching of C-CZ wafers

Several samples were polished and preferentially etched using a variety of etchants as described in Chapter II to reveal crystal defects and dislocations. Through all of these samples, no etch pits were conclusively identified or imaged. To ensure proper etch procedure and reduce artifacts from the saw cut surface, one sample from segment CD was polished on one side by Aptek Industries to ensure a pristine scratch-free polished surface. This sample was cleaned by ultrasonic agitation several times in detergent solutions, solvents and deionized

water to ensure complete cleanliness. The sample was etched for 3 min in Secco under ultrasonic agitation to produce etch pits at defect locations. Resulting DIC microscopy (Figure 3.1) only shows minimal contamination and no etch pits were observed. To ensure etching occurred under proper conditions, the process was repeated on a scrap sample of multicrystalline silicon (Figure B1, Appendix B). This test revealed many defects in the multicrystalline sample as expected, confirming the proper etch conditions.

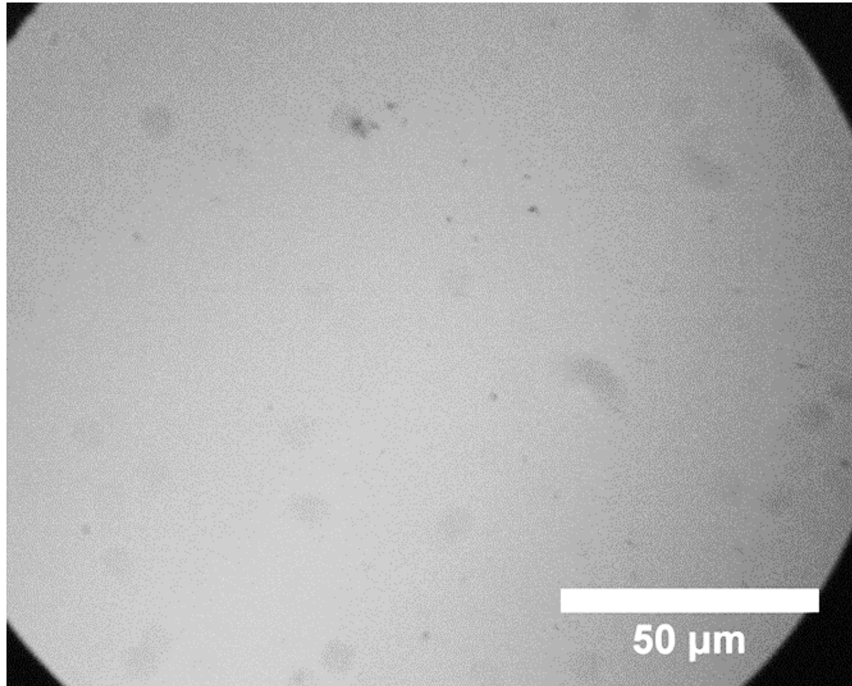

Figure 3.1: Representative DIC micrograph of a polished *C*-CZ silicon surface from segment CD after preferential etching (Secco 3 min). The dark irregular features are surface contaminants used to focus the image.

The absence of etch features in Figure 3.1 and other DIC micrographs indicate the *C*-CZ crystals were grown with a very low density of defects resulting from the crystal growth

process. This is consistent with the expectation that the continuous nature and steady melt volume associated with *C*-CZ growth reduces melt fluctuation and resulting thermal stress in the final crystal.[10] In order to validate this result, hardness was measured across wafer radii by nanoindentation.

Dislocation presence determined by nanoindentation

Decreases in hardness across a uniform crystal plane can be attributed to local phase transformation associated with dislocations.[55] Therefore, hardness measurements on polished wafer surfaces can indicate the presence of dislocations resulting from thermal stress during crystal growth. Nanoindentation scans across polished, radial samples were made on wafers from each as-received sample set, performed by colleagues Schiessl and Dr. Youssef. The highest quality scans shown in Figure 3.2b, taken from wafers B7-08 and CD-08, are obscured by polishing artifacts but show no features indicative of stress variations along the wafer radius. Nanoindentation scans measured across samples from other wafers (Figures B2, B3 and B4, Appendix B) are more affected by polishing artifacts, but indicate that the features discussed in Figure 3.2 are indeed artifacts and give no indication of dislocation-induced phase transformation.

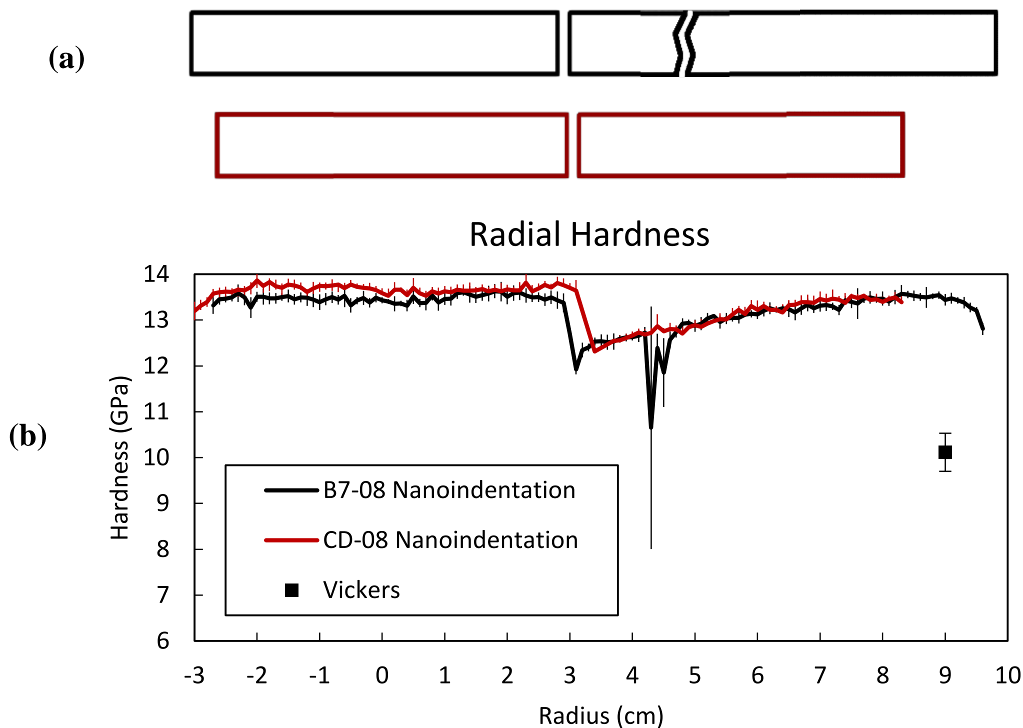

Figure 3.2: (b) nanoindentation scans of samples B7-08 (black) and CD-08 (red) indicate no detectable variation in stress across the wafer radius. Note the two polishing artifacts between 3 and 10 cm, and their correspondence with locations of sample features **(a)**. The result of several Vickers microhardness tests (square) from various wafers from segment CD is plotted for comparison. All vertical lines indicate standard deviation. Nanoindentation measurements performed by colleagues Schiessl and Dr. Youssef.

Comparing the location of the polished samples to the nanoindentation scan is critical in separating artifacts from true variations in hardness. The sample piece cleaved from the center of the wafer includes radii from approximately -3 to 3 cm, with the border between the two samples indicated by the sharp change in hardness near 3 cm. Across the samples farther from the center, hardness appears to increase (~8%) steadily with radius and decrease abruptly near the wafer edges. Artifacts from other nanoindentation measurements (Figures B2, B3 and

B4, Appendix B) show that hardness tends to be much lower towards the edges of the sample pieces. By comparing regions of the same segment using different polished samples in Figure B2, this slope is shown to be dependent on the individual sample measured and not on wafer properties. Therefore the hardness variation in both measurements shown in Figure 3.2 between $r = 3 - 10$ cm is attributed to inconsistent polishing, and most likely to the presence of dislocations remaining from the grinding and polishing process. The slope in hardness over a particular sample may be caused by inconsistent manual polishing across the long, narrow samples. The sharp decrease in hardness near 4.5 cm for wafer B7-08 is associated with a crack spanning the width of the sample at this radial location. This may have occurred during polishing or perhaps during indentation. Nevertheless, residual stress is clearly not responsible for this sharp decrease.

Average hardness measured by nanoindentation across center samples (free from visible polishing artifacts) is 13.5 ± 0.1 GPa for wafer B7-08 and 13.7 ± 0.1 GPa for wafer CD-08 at 7 mN loading. This number is slightly higher than 11.9 and 13 GPa measured using the same tip geometry at 15 and 0.2 mN, respectively, reported by literature for undoped silicon.[56] The increase in hardness may be due to the phosphorus doping present in the *C*-CZ wafers, which was not present in the undoped samples studied in the literature.

Vickers microhardness measurements

Vickers microhardness and fracture toughness measurements were made on polished samples taken from select regions of wafers from each sample segment using loads of 50 – 100

g. Table 3.1 shows the calculated Vickers microhardness H_V and fracture toughness K_{IC} using 10 indentations per sample.

Table 3.1: Vickers microhardness and fracture toughness of *C*-CZ wafers

Segment	H_V (GPa)	K_{IC} (MPa)
B3	10.2 ± 0.68	0.84 ± 0.12
B5	10.2 ± 0.35	0.90 ± 0.09
B7	10.1 ± 0.41	1.03 ± 0.16
CD	9.9 ± 0.66	0.99 ± 0.66

Vickers microhardness measurements are very consistent between segments, near 10 GPa, and there was no significant difference in hardness determined using different loadings over the range investigated. Literature values for Vickers microhardness on (100) silicon vary from 11.3 GPa at 100 g load[57] to 16.4 GPa at 50 g load.[58] The discrepancy between the results in Table 3.1 and literature is not known, but may be related to the phosphorus dopant present in *C*-CZ samples which is not present for those samples reported in the literature. If the lower hardness measured for *C*-CZ samples is somehow related to residual stress within the wafers, such properties are consistent along the crystal axis as indicated by segments B3, B5 and B7. Segment CD, which was taken from the tail of a subsequent crystal, exhibits a very similar hardness suggesting mechanical properties between crystals are similar.

Fracture toughnes, K_{IC}, was calculated by measuring cracks radiating from Vickers indents and is shown in Table 3.1. Despite a high standard deviation due to varying crack lengths, K_{IC} values are similar to the reported value of 0.95 MPa for (100) silicon as measured by the same Vickers microindentation technique.[59] A more in-depth study of fracture toughness may yield an indication of dislocations or residual stress, but the results above are not sufficiently precise to draw such conclusions.

Sub-surface damage

In addition to dislocations remaining from thermal stress during crystal growth, dislocations are introduced near the surface of wafers as wafers are sawn from the crystal. This sub-surface damage must be removed before beginning any device processing; hence, the extent of this damage must be well understood. Sub-surface damage resulting from wafer sawing was determined to extend approximately 22 μm below the wafer surface by applying the angle polish and etch method described in Chapter II on wafer CD-21. Figure 3.3 shows a DIC micrograph of the angle-polished plane used to measure the distance of etched dislocations caused by mechanical saw damage from the angle polished interface. Figure 3.4 shows an SEM image of the angle polished sample with overlaid measurements used in calculations.

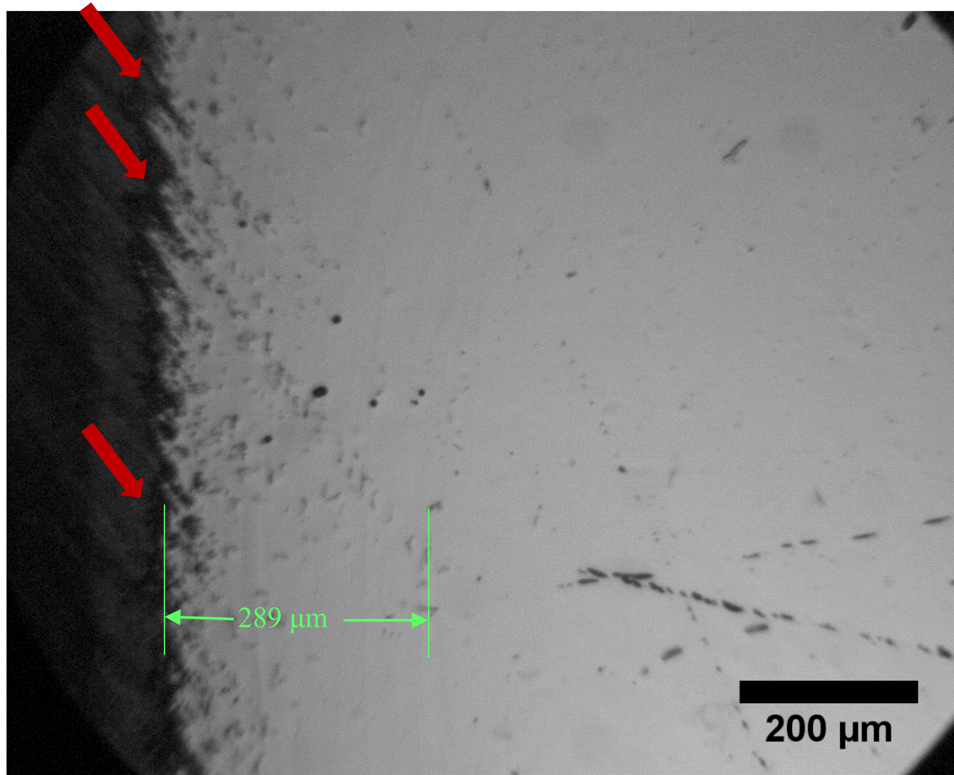

Figure 3.3: DIC micrograph of an angle-polished sample (wafer CD-21) showing the interface between the angle polished surface (bright, right side) and the original wafer surface (dark, left side). Polishing artifacts appear as features of isotropic direction. Penetrating saw damage appears as straight parallel etch pit clusters on the angle polished surface near the interface. Some etch pit clusters are indicated by overlaid red arrows. The measured distance to the deepest observed damage is indicated by the horizontal green dimension.

DIC micrographs (Figure 3.3) reveal that dislocations resulting from saw damage penetrate much deeper than visible surface roughness. Depth of damage was calculated using the distance from the angle interface to the deepest dislocation clusters on the angle polished surface. The distribution of damage depth is very broad with most of the damage only penetrating a few micrometers and intermittent dislocations extending to the 15 - 20 μm range. The observation of deeper damage at 22 μm was rare in these measurements. Due to the broad

distribution of damage depth and the small sample size of a few linear centimeters compared to the ~500 cm^2 area of the entire wafer, saw damage may penetrate even deeper than 22 µm in some locations across the wafer which were not measured.

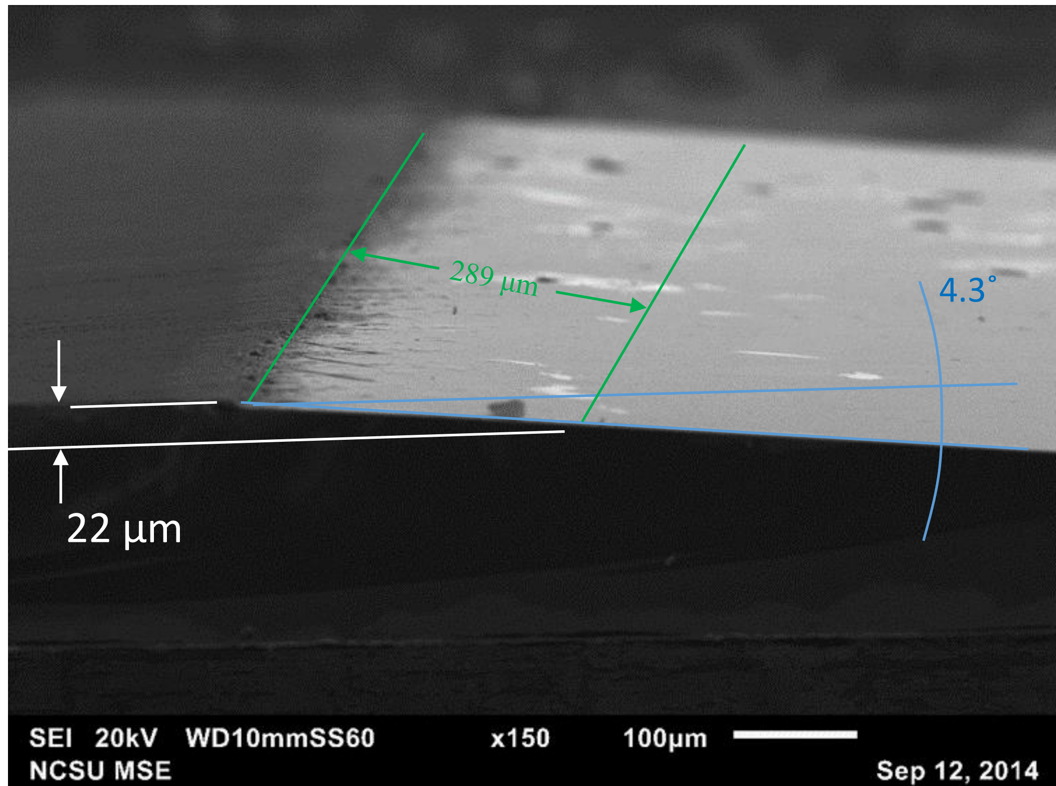

Figure 3.4: Scanning electron micrograph of an angle polished sample (wafer CD-21), tilted such that the polished surface (bright region) can be seen. The darker region to the left is the wafer surface, coated in SiN_x. Overlaid dimensions mark the polished angle (blue), distance from angle interface to deepest damage (green), and calculated depth of damage(white). Dimensions are not to scale.

Figure 3.4 shows a scanning electron micrograph of an angle polished sample which was used to measure the angle between the polished surface and the original surface, which

was used to calculate the depth of delineated dislocations seen in plan view (Figure 3.3). This region was also imaged to confirm the quality of the edge, as a rounded edge would make the true location of the interface difficult to distinguish and skew depth measurements.

The wafer sawing process used by SunEdison is a fixed-diamond abrasive wire saw technique, which has been reported to cut wafers 2.5 times faster than traditional loose abrasive slurry sawing, with a significant decrease in the depth of damage from approximately 15 μm with loose abrasive to 7 μm with fixed abrasive.[28] However, the results of the angle-polish measurement of damage depth here indicate that some mechanical damage penetrates significantly deeper than 7 μm. With the state of saw damage present in the *C*-CZ wafer samples, etch time must be increased to remove a greater amount of material to avoid decreasing solar cell conversion efficiency. This increase in etching is not consistent with SunEdison's goal to reduce power conversion costs by reducing kerf loss with a fixed abrasive sawing technique.[1] Modifications to the current SunEdison fixed abrasive wafer sawing process must be made in order to meet this goal, such as a controlled distribution of diamond grains along the cutting wire to maximize cutting in the sawing direction and minimize cutting across the wafer faces.[32] Some damage which remains below the surface after etching may be passivated by chemical interaction with hydrogen[34] during thermal processing whereas shallow damage may be passivated by field effect surface passivation.[38]

Surface passivation

Field effect surface passivation by fixed charge deposition was applied to one wafer from each sample segment to demonstrate permanent passivation of shallow mechanical saw

damage and the wafer surface. In comparison to chemical surface passivation techniques, field effect passivation prevents recombination at and *near* the surface where some dislocations may exist. To perform field effect passivation, 30 nm of Al_2O_3 were deposited by atomic layer deposition by the research group of Dr. Hahn at the University of Konztanz. The lifetimes of these wafers were then measured by quasi-steady state photoconductance (QSSPC), the results of which are shown in Figure 3.5. Average carrier lifetimes are plotted against the total electron donor concentrations reported by SunEdison in Figure 3.6.

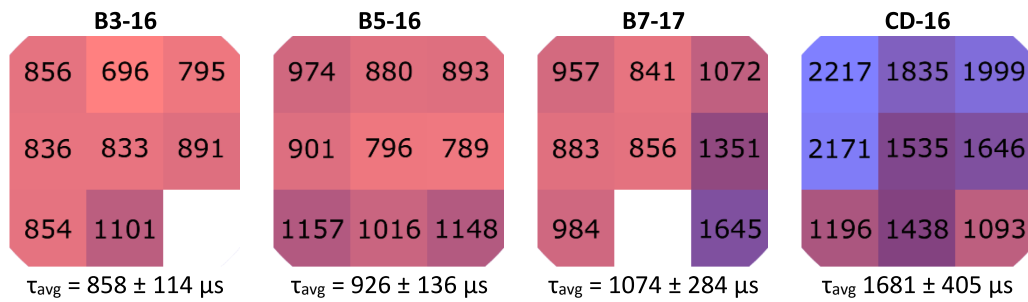

Figure 3.5: QSSPC carrier lifetime measurements of *C*-CZ wafers. The color scale is common to all maps, with pink denoting the lowest lifetime and blue denoting the highest lifetime. Overlaid numbers indicate the lifetime (µs) measured at that location. Empty squares indicate unmeasured locations. QSSPC measurements were performed under Dr. Hahn at the University of Konstanz.

Minority carrier lifetime measured by QSSPC at the University of Konstanz in Figures 3.5 and 3.6 yields lifetimes ranging from approximately 800 – 2000 µs, compared to approximately 4000 – 4800 µs measured using QSSPC by SunEdison on bulk samples from each segment (Table 2.1). The difference between the two measurements is attributed to surface effects, which are insignificant in SunEdison's thick 4 cm samples but become

dominant in the thin, 180 μm wafers sent to the University of Konstanz.[35] The average carrier lifetimes of the thin wafers treated with field effect passivation is dependent on the measured electron donor concentration N_d, as demonstrated by the regression fit shown in Figure 3.6. Considering the contributions to the measured effective lifetime given in Equations 1.4 and 1.5, it is postulated that the surface recombination velocity S is responsible for the dependence of lifetime on donor concentration since bulk lifetime measurements do not exhibit such a dependence on N_d.

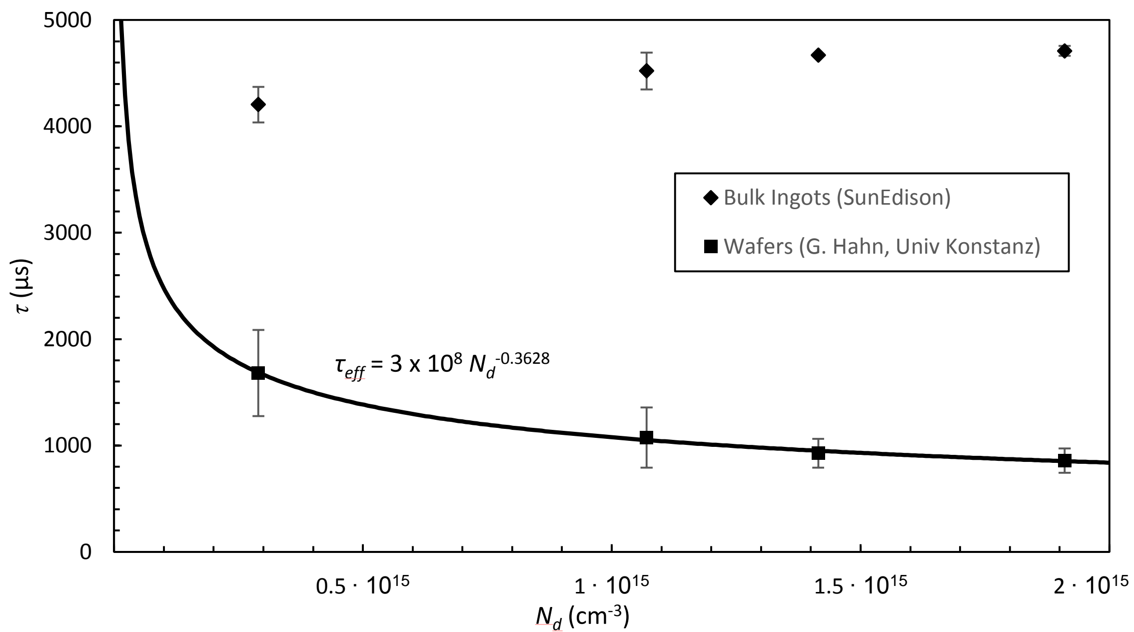

Figure 3.6: Average τ_{eff} measured by QSSPC (squares, University of Konstanz) plotted against N_d and fitted to a power function consistent with Equation 3.1. Average τ_b measured by QSSPC (diamonds, SunEdison) are also plotted for comparison.

The surface recombination velocity S was calculated using Equations 1.4 and 1.5 with measured thickness t, calculated diffusivity D for minority carriers in silicon, bulk lifetime τ_b measured by SunEdison, and effective lifetime τ_{eff} measured by QSSPC at the University of Konstanz. The calculated surface recombination velocities are plotted against the total electron donor concentration for each sample segment in Figure 3.7. Surface recombination velocity S also shows excellent correlation with electron donor concentration N_d from Al_2O_3-passivated wafers measured by QSSPC. The regression fit in Figure 3.7 is represented by Equation 3.1 with S_0 = 6.00 x 10^{-8} cm/s and γ = 0.533.

$$S = S_0 {N_d}^{\gamma} \qquad \text{Equation 3.1}$$

This model is in agreement with a similar model published by Kray, et al[60] relating effective S to N_d and the pitch of laser fired contacts on a laser fired solar cell. When terms in their equation dependent on contact pitch are eliminated by forcing the pitch to infinity or 0, their model is consistent with Equation 3.1 and representative of the data presented here. Kray, et al reported similar values for the parameters in Equation 3.1 (S_0 = 1.1 x 10^{-8} cm/s and γ = 0.55). In comparison, Dicker[61] published results fitting this model for solar cell back contacts by varying S to fit measured V_{oc} to simulation. Dicker's fit yielded S_0 = 1.57 x 10^{-8} cm/s and γ = 0.42. In contrast to the n-type C-CZ silicon wafers of the present work, the investigations of Kray, et al and Dicker were performed on p-type CZ silicon wafers.

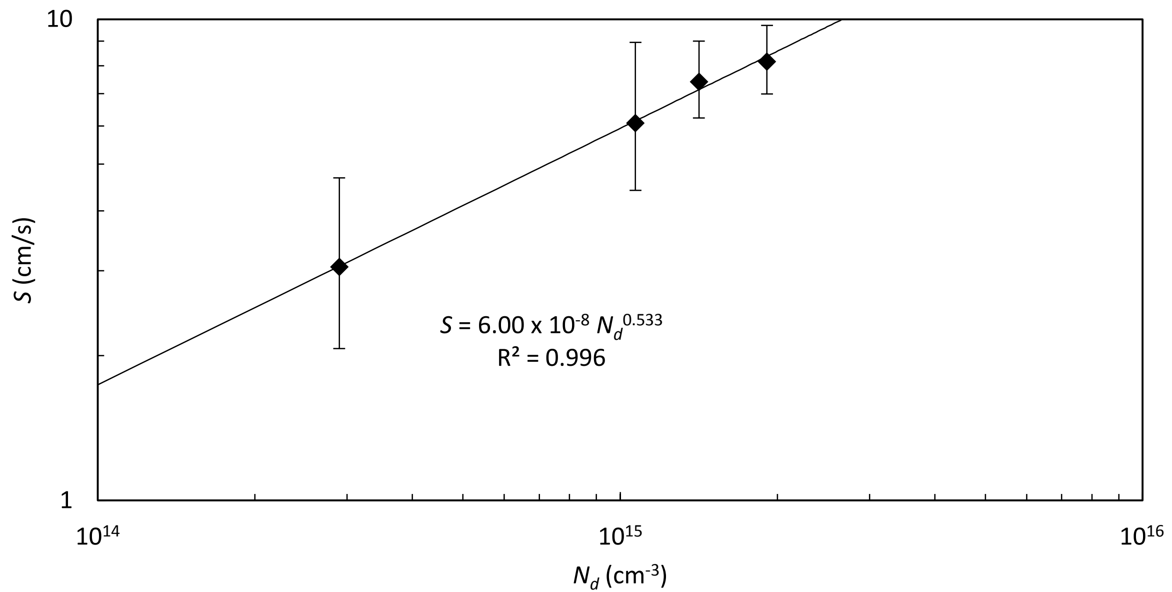

Figure 3.7: Dependence of S on N_d using Equation 1.4, τ_{eff} and τ_b measured at the University of Konstanz and SunEdison, respectively. Note the high correlation coefficient of the fitting line and agreement with Equation 3.1.

Based on the principles of field effect passivation, the negative fixed charge present in deposited Al_2O_3 layers repels electrons from the near-surface region, preventing recombination with holes which may still be trapped by defect states present near the surface. In p-type materials, electrons are the minority carriers versus n-type materials where electrons are majority carriers. Because of this difference, the passivation effect varies between p-type and n-type. Although Al_2O_3 passivation deposited by atomic layer deposition has been reported to be more effective when applied to n-type silicon wafers,[38, 62-63] relatively little work has been published studying this n-type passivation. Because the vast majority of industrially produced solar cells use p-type silicon substrates[64] many works on Al_2O_3 surface passivation have focused on p-type silicon wafers.[65-67] However, n-type wafers are expected to become more

popular in the future as substrates for high-efficiency photovoltaic cells due to their higher potential efficiency.[64] To date, fitting surface recombination velocity of Al_2O_3-passivated n-type wafers to carrier concentration using Equation 3.1 has not been reported.

Variations in donor concentration

Due to the dependence of surface recombination velocity on electron donor concentration N_d, the analysis of N_d is important when considering wafer properties. Furthermore, photovoltaic cell structures are designed around a particular base wafer carrier concentration such that efficiency is maximized. Deviation from target values may lead to decreases in cell efficiency.[15] N_d is known to vary with wafer radius depending on the rotation of the crystal and crucible during growth.[14] To investigate radial variations in N_d and confirm measurements made by SunEdison using four point probe on thick samples, the resistivity of one wafer (CD-24) was profiled along the full 8 in diameter of the original round wafer using four point probe measurements. Sheet resistance measurements were used to calculate N_d (see Equations 2.3 and 2.4) every 2.5 mm across the diameter of the wafer, which is plotted in Figure 3.8 against radius r such that 0 is the wafer center. Also shown in Figure 3.8 is N_d extracted from capacitance-voltage measurements of gold Schottky barriers on polished samples taken from the indicated radial locations, and N_d reported by SunEdison. Similar measurements made on all sample segments are shown in the Appendix (Figure B5, Appendix B), but are not accurate due to effects of sample geometry. Figure B5 does indicate that all samples exhibit behavior similar to Figure 3.8.

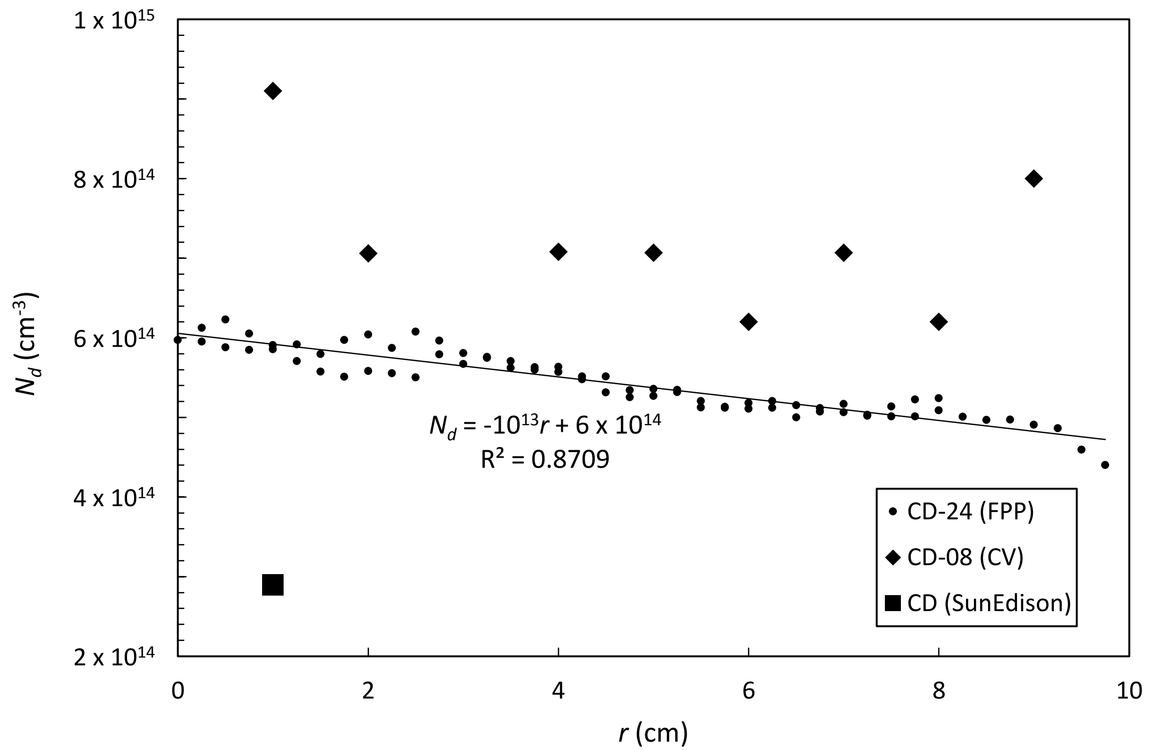

Figure 3.8: N_d determined by four point probe (circles), and capacitance-voltage (diamonds) measurements plotted against wafer radius r and compared to N_d reported by SunEdison (square) using a single four point probe measurement. Four point probe measurements of wafer CD-24 were performed across a diameter, leading to two measurements per radius.

Four point probe measurements indicate that N_d decreases linearly from $N_0 = 6 \times 10^{14}$ cm^{-3} at the center to edge with a slope $s = -10^{13}$ cm^{-4} according to equation 3.2.

$$N_d = s\,r + N_0 \qquad \text{Equation 3.2}$$

This observation is consistent with similar results reported by Zulehner[14] who reported that such variations arise from crystal growth conditions and are very dependent on crystal rotation during growth. Based on Figure 3.8, wafer suppliers should consider measuring resistance at a radius r_m which better represents the average properties of the wafer. The crystal

rotation conditions could then be constrained such that the range of N_d across the wafer does not decrease photovoltaic conversion efficiency beyond acceptable tolerance. To estimate r_m, the pseudo-square wafer is first approximated as a circle with radius r_c whose area A is equal to that of the wafer (240 cm^2):

$$r_c = \sqrt{\frac{A}{\pi}} = \sqrt{\frac{240\ cm^2}{\pi}} = 8.7\ cm$$

To determine the average carrier concentration N_{avg} across the wafer Equation 3.2 is solved for r, revolved about $r = 0$ out to r_c with edge carrier concentration N_{edge}. This integral is then divided by the area of the wafer and added to N_{edge} to yield N_{avg}.

$$r(N_d) = \frac{N_d - N_0}{s}$$

$$N_{edge} = s\, r_c + N_0 = -10^{13}\ cm^{-4} \cdot 8.7\ cm + 6 \times 10^{14}\ cm^{-3} = 5.13 \times 10^{14} cm^{-3}$$

$$N_{avg} = \frac{\pi \int_{N_{edge}}^{N_0} \left(\frac{N_d - N_0}{s}\right)^2 dN_d}{A} + N_{edge}$$

$$= \frac{\int_{5.13\times10^{14} cm^{-3}}^{6\times10^{14}\ cm^{-3}} \left(\frac{N_d - 6 \times 10^{14}\ cm^{-3}}{-10^{13}\ cm^{-4}}\right)^2 dN_d}{240\ cm^2} + 5.13 \times 10^{14} cm^{-3}$$

$$= 5.42 \times 10^{14} cm^{-3}$$

By entering N_{avg} into equation 3.2, the radius r_m at which carrier concentration will be representative of the wafer average can be calculated:

$$r_m = r(N_{avg}) = \frac{N_{avg} - N_0}{s}$$

$$r_m = \frac{5.42 \times 10^{14} cm^{-3} - 6 \times 10^{14} cm^{-3}}{-10^{13} cm^{-4}} = 5.8\ cm$$

By measuring wafer properties approximately 5.8 cm from the wafer center, calculated resistivity and carrier concentration will be more representative of the entire wafer. Although this calculation was made using data specific to segment CD, the location of ideal measurement r_m will hold for any pseudo-square wafer assuming the carrier concentration varies linearly with radius.

Figure 3.8 also includes some values of N_d calculated from capacitance-voltage measurements made on gold Schottky diodes evaporated onto polished samples and cleaved near the indicated radii. The lower precision in these measurements is likely due to variations in diode area. Because capacitance depends on the square of diode area,[27] minor imperfections or inconsistencies between the holes in the diode mask could easily be responsible for variation between measurements. Similarly, the higher N_d measured by CV compared to four point probe techniques may be attributed to a consistent error in the area measurement. If the diodes formed just slightly smaller than the mask holes or if the mask hole diameters are uniformly less than 1 mm, the estimation of N_d would yield consistently higher values for all samples measured. Alternatively, the four point probe measurements may be inaccurate due to sub-surface damage from wafer sawing. If the damage near the surface increases the local resistivity due to scattering, the effective thickness though which resistance was measured would be lower and the resulting N_d would be higher. Despite the low precision of capacitance-voltage measurements, the linear decrease of N_d with radius r is supported.

SunEdison reported $N_d = 2.9 \times 10^{14}$ cm^{-3} for the center of segment CD measured by four point probe, which is significantly lower than measurements reported in Figure 3.8. The cause for this discrepancy is unclear at present, but is likely related to sample geometry. Four

point probe and capacitance-voltage measurements made across wafer diameters were performed on thin samples 180 μm thick or less while SunEdison measurements by four point probe were made on samples 4 cm thick. However, we should point out that four point probe measurements on other segments resulted in donor concentrations consistent with those determined by SunEdison.

Thermal donors

Radial distribution of thermal donors by four point probe

The concentration of ionized carriers in a semiconductor is a sum of contributions from multiple sources. While phosphorus doping is the primary source of conduction electrons in the *C*-CZ samples studied, oxygen is known to form small precipitates which act as electron donors and add to the total donor concentration.[18-20, 22, 68] These precipitates form in the 350˚C – 400˚C range and can be dissolved by heating above 600˚C.[19-20, 69] By calculating resistivity from four point probe measurements before and after annealing to dissolve thermal donors, the concentration of thermal donors can be studied in the same manner as total donor concentration. Wafer CD-23 was annealed at 700˚C for 20 minutes to dissolve thermal donor precipitates and measured by four point probe along the diameter with the same technique used to profile resistivity across wafer CD-24 in Figure 3.8. The difference between the electron donor concentration at each measurement location along the radius yields a profile of the thermal donor concentration, as shown in Figure 3.9.

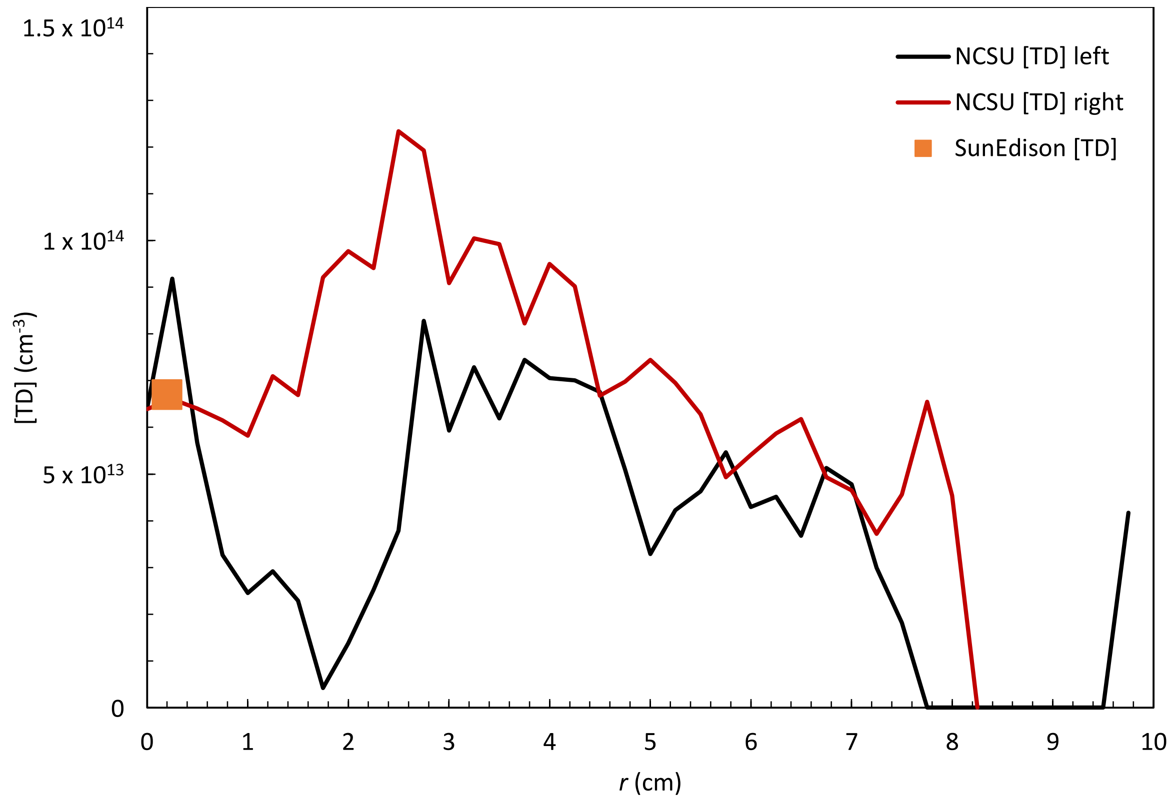

Figure 3.9: Calculated thermal donor concentration [TD] along the diameter of segment CD, plotted against radius *r*. Measurements near the wafer edges yielded negative concentrations, indicating the [TD] is lower than the noise of the measurement and were therefore omitted. The decrease in [TD] near $r = 2$ cm is believed to be a local thermal donor deficiency. The square represents the thermal donor concentration determined by SunEdison.

The thermal donor profile reveals a fairly constant ~6 x 10^{13} cm^{-3} thermal donor profile out to $r = 8$ cm, which is followed by a sharp decrease below detectable levels across the outer 2 cm of the wafer. This is attributed to the distribution of temperature in the crystal during cooling after growth. The outside of the crystal should cool fastest and spend the least time in the critical temperature range for thermal donor growth. The center of the crystal cooled slower and allowed more time for thermal donor precipitates to nucleate and grow. Alternatively,

variations in oxygen content resulting from crystal rotation, similar to the linear decrease in total electron donor concentration observed in Figure 3.8, could be responsible for this observation. The decrease in thermal donor content near $r = 2$ cm may indicate a local oxygen and/or thermal donor deficiency. A symmetrical, radial difference in concentration would be indicated by a symmetrical feature in measurements made on the opposite side of the wafer (plotted at the same radii).

SunEdison made similar measurements also using the four point probe and annealing technique, see Table 2.1. For segment CD, they estimated the thermal donor content to be 6.7 x 10^{13} cm^{-3} compared to 6.0 x 10^{13} cm^{-3} average thermal donor concentration for $r < 8$ cm of the data presented here. This suggests that test methods at both locations are consistent. However, the lower thermal content at the outer radii may be important to consider when using *C*-CZ grown wafers. Comparing the N_d and thermal donor content of the wafers studied, thermal donors will have a minimal effect on wafer properties. However, higher oxygen content from lower quality feedstock or wafers with doping concentrations similar to thermal donor concentrations will be much more affected by thermal donor variations across the wafer. Additionaly, due to the pseudo-square shape of wafers for solar cells, the variations within 2 cm of the wafer edge (Figure 3.9) are limited to the wafer corners which contribute little to the total wafer properties. However, seemingly random variations such as that seen near $r = 2$ cm in the CD segment must be considered when designing solar cells and mapping cell or wafer properties which depend on resistivity.

Radial distribution of thermal donors by transient spectroscopy

The exact nature of the various thermal donors present in the *C*-CZ samples was also studied by measuring their energy levels in the silicon band gap via DLTS. Thermal donors appear as traps in DLTS spectra and are located at the lower end of the temperature spectrum due to their proximity to the conduction band. Based on the radial dependence of thermal donor concentration demonstrated earlier in this chapter, several small samples along the radius of all four sample segments were prepared with Schottky barriers for DLTS measurement. The resulting spectra are presented in Figure 3.10.

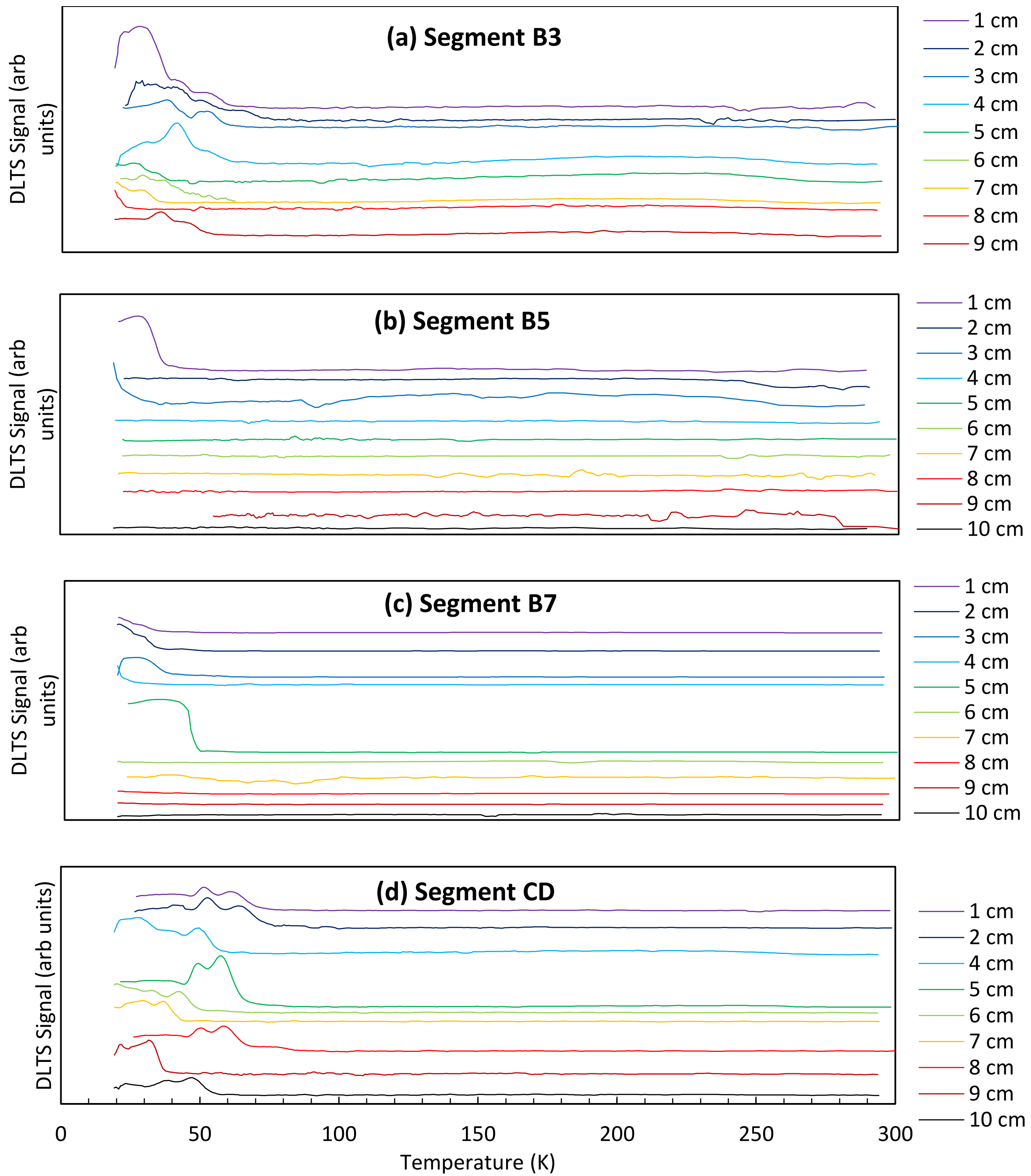

Figure 3.10: DLTS scans from segments **(a)** B3, **(b)** B5, **(c)** B7 and **(d)** CD. Samples taken from every cm along the wafer radius were measured, and each set of scans for a given segment shows scans taken with increasing radius from top to bottom (see labels). Low temperature peaks are attributed to thermal donors but system resolution prevents proper identification. U_p = 0 V, U_b = -3 V, t_p = 5 ms, period width = 50 ms.

In samples from B3 and CD segments, a series of superimposed positive peaks is seen at low temperatures, indicating their proximity to the conduction band. The relative peak intensities vary between B3 and CD and are not observed at all in segments B5 and B7. The location of these peaks indicates that they are likely related to thermal donors, but the lack of consistency prevented unambiguous identification of the traps observed. However, a qualitative assessment can be made. In segments B3 and CD, note the relative intensities of the samples taken at different radii. For segment CD in particular, the same segment tested by four point probe, measurements show that the peak intensity may be higher towards the center and decreases near the edge. This is consistent with the four point probe results reported above, supporting the identification of these peaks as thermal donors. The absence of significant peaks at higher temperatures indicates no detectable deep-level traps, which are the most detrimental to carrier lifetime via a Shockley-Read-Hall mechanism. DLTS is by far the most sensitive technique to identify such traps, and their presence would be easily detected. The DLTS results suggest that the *C*-CZ silicon investigated is relatively high quality material that is suitable for photovoltaic applications.

To properly identify and characterize all traps in the samples, further measurements were performed on samples at the University of Manchester by Dr. Markevich, including DLTS and MCTS spectra of Schottky barriers from the center of each sample segment (see Figure 3.11 and Figure 3.12). The DLTS spectra reveal 4 donor levels identified as E_1, E_2, E_3 and E_4, which are in the same temperature range as those observed in Figure 3.10 for the measurements performed here. E_1 is attributed to a thermal donor, while E_2, E_3 and E_4 are attributed to an oxygen–hydrogen complex.[70-71] The thermal donor identified in CD-16 is

present in much higher concentrations in the B crystal segments. In contrast to NCSU DLTS data, the Manchester data indicate that thermal donors are present in all segments at similar concentrations across the B crystal. The relative intensities of the thermal donor signal in both DLTS and MCTS correlate well with the thermal donor concentrations identified by SunEdison (Table 2.1). This correlation is demonstrated in Table 3.2.

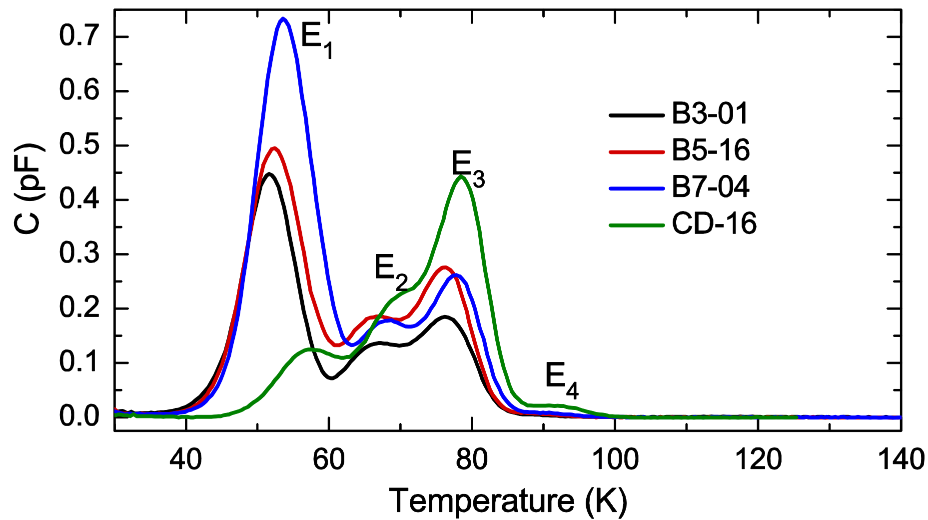

Figure 3.11: DLTS spectra measured from one wafer of each segment. The intensity of electron traps E_2, E_3, and E_4 is highest in the CD segment and fairly constant in the B crystal, while the thermal donor intensity (E_1) is lowest in the CD crystal. U_b = -3 V, U_p = 0 V, t_p = 1 ms. Measurements made by Dr. Markevich at the University of Manchester.

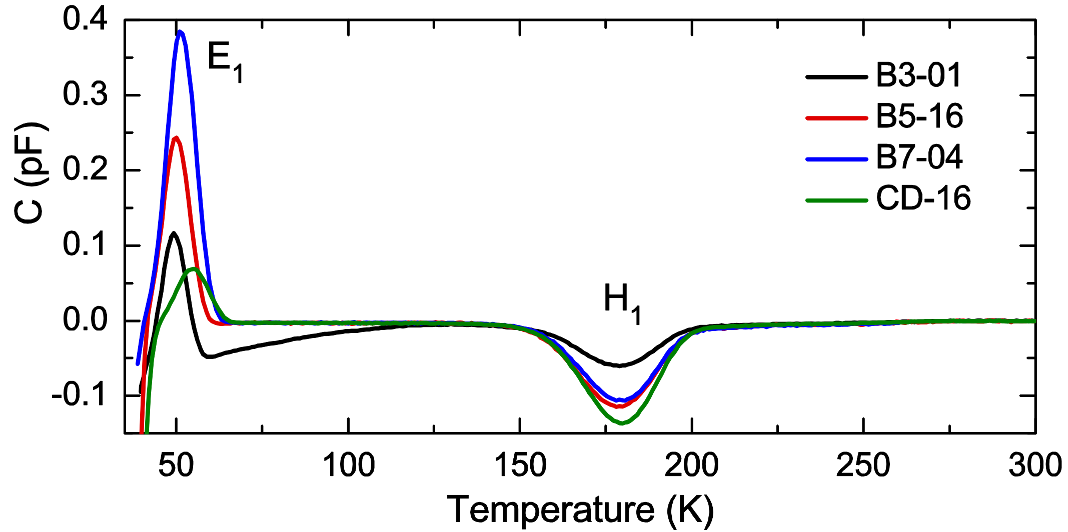

Figure 3.12: MCTS spectra from one wafer of each sample segment indicate lower H_1 content in the B crystal compared to the CD segment. The variation in thermal donor content is also confirmed, indicated by the decreasing 55 K signal intensity from B3 to CD. Backside LED 850nm, U_b = -5 V, t_p = 10 ms. Measurements made by Dr. Markevich at the University of Manchester.

Table 3.2: Relative thermal donor content measured by four point probe, DLTS and MCTS

Sample	SunEdison four point probe [TD] (AU)	DLTS 55 K intensity (AU)	MCTS 55 K intensity (AU)
B3-01	0.866	0.616	0.316
B5-16	0.887	0.685	0.632
B7-04	1.00	1.00	1.00
CD-16	0.290	0.164	0.184

Transient spectroscopy analysis of oxygen-hydrogen complex

The MCTS H_1 peak in Figure 3.12 was determined to have an energy of $E_v + 0.35$ eV, with a significant hole capture cross section 10 times greater than the electron cross section and at a concentration near 10^{13} cm^{-3}. This energy level may have a significant impact on the lifetime of the sample wafers because the hole lifetime dominates recombination in the n-type material. The nature of this complex is explored by varying the constant bias and pulse bias, allowing for the sampling of different depths below the Schottky barrier (Figure B6, Appendix B). This process was repeated for the electron trap E_3 and both concentration profiles are compared in Figure 3.13. The location of the electron trap E_3 was determined to be located at $E_c - 0.14$ eV. The concentration of both E_3 and H_1 traps are highest at the surface and decay at a similar rate with increasing depth. The similarities between the concentration profile of these two traps indicate that they are related and most likely originate from the same complex. The depth dependence indicates that these defects are not present in the crystal during growth, but have developed due to surface treatment during or after wafering. Because these samples were not subjected to any high-temperature treatment for diffusion of impurities to occur, hydrogen is identified as the source. Hydrogen diffuses quickly at relatively low temperatures (~200˚C)[72] and is known to form defect levels in this range upon reaction with oxygen.[70] Although the source of this hydrogen is not certain, it is likely introduced during HF cleaning prior to Schottky barrier deposition.

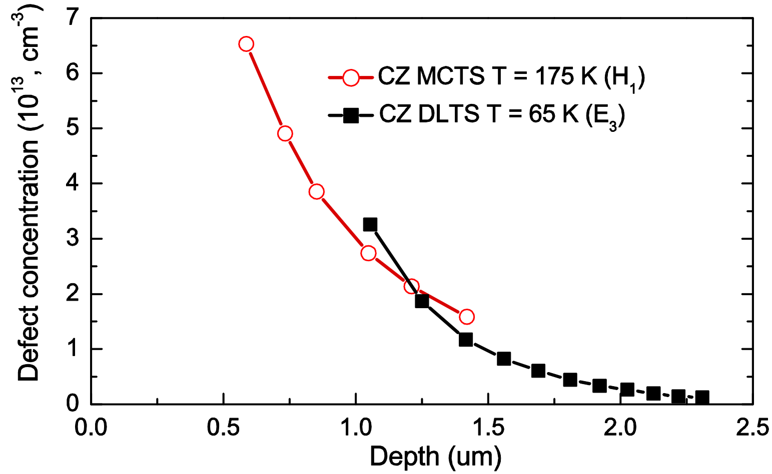

Figure 3.13: Concentration of the oxygen-hydrogen complex as a function of depth by varying bias and pulse bias of DLTS measurement at 80 K (black) and MCTS at 175 K (red) as demonstrated in Figure B7 in Appendix B.

Due to the high diffusivity of hydrogen and the low temperature formation of the oxygen-hydrogen complex, the complex is expected to disassociate after low temperature thermal treatment. A sample from CD-16 was annealed for 20 min at 200°C and measured again using DLTS (Figure B7, Appendix B) by Dr. Markevich. The E_3 peak assigned to the oxygen-hydrogen complex is completely removed by this treatment, demonstrating the low temperature nature of its formation and dissociation. Although this defect is quickly removed with thermal processing, hydrogen is intentionally introduced during the SiN_x passivation/antireflection layer deposition common to most modern solar cell fabrication processes. This hydrogen is introduced to passivate dangling silicon bonds in the bulk of the wafer, but Figure 3.12 indicates that this hydrogen may also contribute to minority carrier

recombination. This hydrogen-oxygen complex must be studied further to determine its effects in n-base solar cells, and whether or not the energy level can be passivated.

CHAPTER IV: LIFETIME ANALYSIS OF *C*-CZ WAFERS THROUGH SOLAR CELL PROCESSING

The minority carrier lifetime of the substrate wafer used in solar cell production is a limiting factor in power conversion efficiency. Minority carrier lifetime of substrate wafers before processing can be a good indication of carrier lifetime after processing, but to understand the effects of each processing step the carrier lifetime must be measured after each thermal treatment during fabrication. This chapter discusses several techniques used to analyze the minority carrier lifetime as it changes with processing in a typical passivated emitter and rear cell (PERC) fabrication process.

Minority carrier lifetime measured by electron beam induced current

Electron Beam Induced Current (EBIC) images were used to calculate the minority carrier lifetime of samples between each significant thermal processing step in the solar cell fabrication process. The advantage of measuring carrier lifetime with an EBIC technique is the separation of carrier lifetime τ from the surface recombination velocity S, which presents problems in all other measurement techniques discussed in this work. Figure 4.1 compares EBIC data of samples from the B7 segment with the corresponding Bonard Ganière models used to simulate the EBIC data. Figure 4.2 shows a comparison of carrier lifetimes measured by EBIC between samples from each segment after each thermal treatment in the solar cell fabrication process.

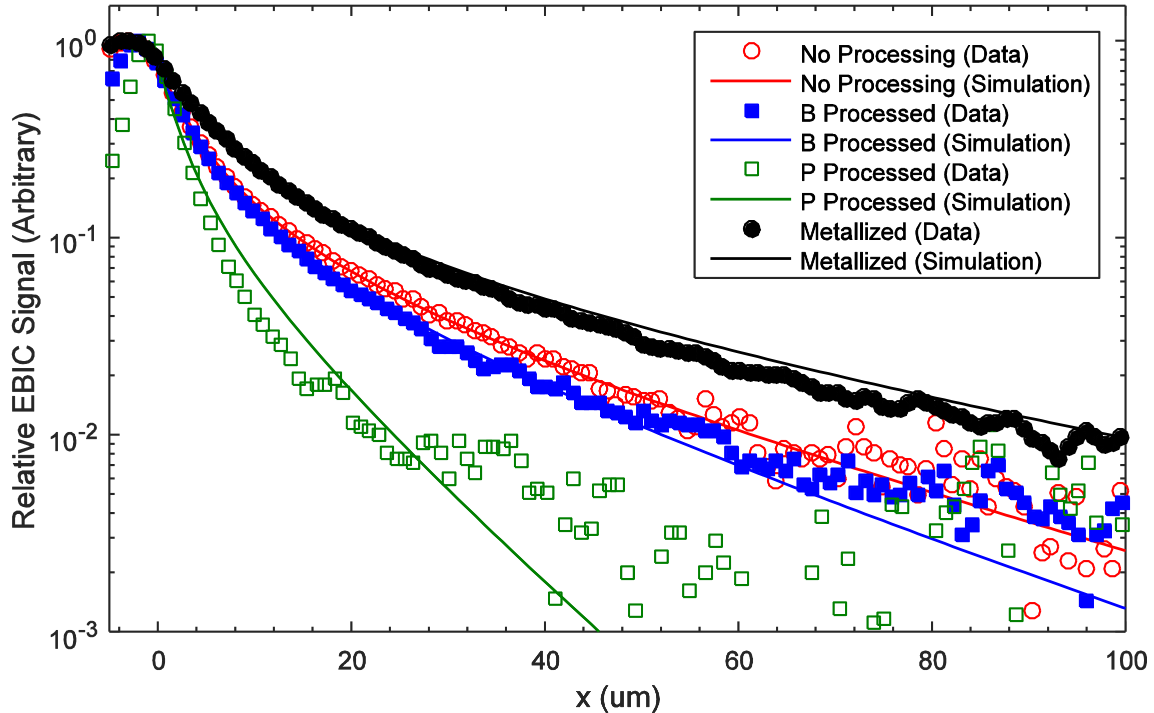

Figure 4.1: EBIC signal vs. measured distance x from the Schottky barrier edge (data points) compared to the Bonard Ganière model of collection efficiency (lines) fitted to each EBIC profile by hole lifetime τ_h and surface recombination velocity S for samples from segment B7.

The carrier lifetimes extracted from EBIC simulations have significant error and cannot be compared quantitatively to other measurement techniques because of the vastly differing injection levels. However, EBIC lifetime measurement yields unique information compared to other techniques: S is separated from τ_h in the simulation process, and therefore does not interfere with τ_h interpretation. By removing the factor of S from τ_h, carrier lifetimes can be compared between segments. Data on segments B5 and B7 in Figure 4.2 reveal that the changes in lifetime before and after the boron implant and anneal are within experimental error, and suggest that no significant lifetime change occurs during this step. The same segments also indicate that lifetime decreases significantly (~10X) after phosphorus implantation and anneal,

although the difference from before processing to after treatment seen in segment B3 contrasts slightly with this observation.

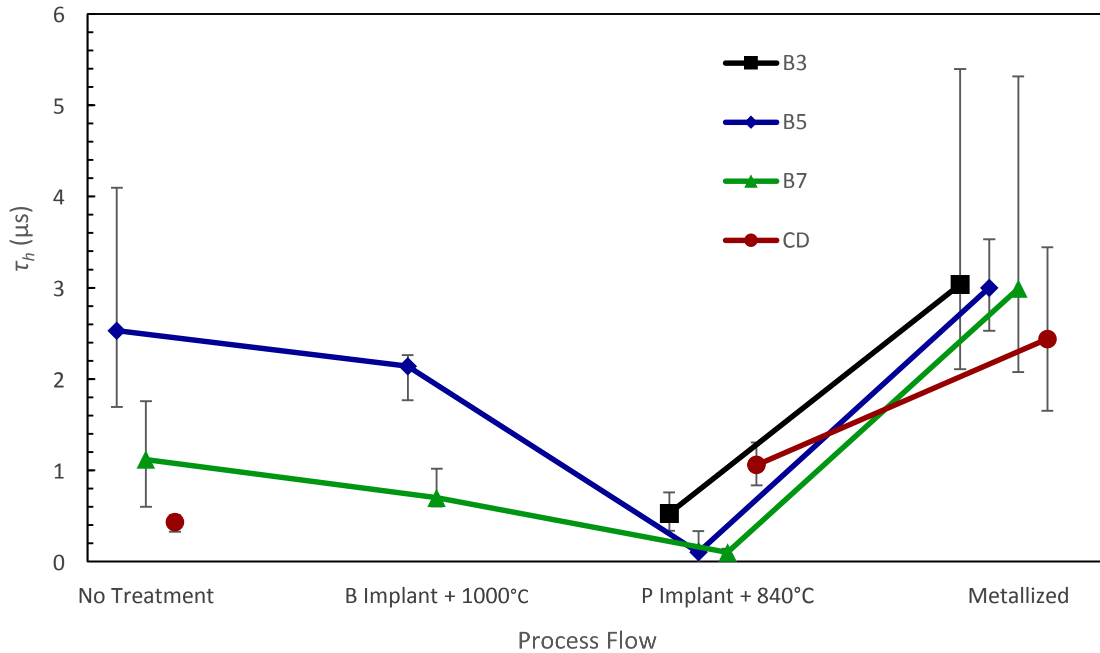

Figure 4.2: Changes in hole lifetime τ_h for wafers from segments B3 (black squares), B5 (blue diamonds), B7 (green triangles), and CD (red circles). Data points indicate best fitting hole lifetime τ_h for EBIC profiles while error bars denote range of τ_h that could possibly fit the measured profiles.

Ion implantation creates a field of damage near the surface with many dangling silicon bonds, which introduce defect levels in the band gap and facilitate Shockley-Read-Hall recombination. The extent of this damage is dependent on implant energy, dosing, and ion mass.[33, 73] The atomic mass of phosphorus (31.0 g/mol) is approximately three times larger than that of boron (10.8 g/mol), indicating that phosphorus implantation may introduce more severe damage than boron. This damage may create more defect energy levels or be more

difficult to remove. The damage introduced by ion implantation steps in the solar cell fabrication process was partially removed by thermal annealing after implantation. However, the anneal temperature after boron implantation was 1000˚C compared to 840˚C after phosphorus implantation. The higher anneal temperature after boron implantation may be responsible for maintaining lifetime, while the lower anneal temperature after phosphorus implantation may not fully remove damage introduced by the phosphorus implant.

The carrier lifetimes of the completed solar cells are higher than at any other stage in processing. This is an important discovery, which was not obtained from other measurement techniques. This increase is attributed to the hydrogen passivation step included at the end of cell processing. After deposition with the SiN_x, hydrogen diffuses through the cell during the contact firing and curing steps, which passivates deep-level recombination centers introduced by crystal defects.[74] Hydrogen passivation should passivate implantation damage, as well as any other crystal defects present before processing which would decrease lifetime. This theory is consistent with the observation that after metallization, lifetime increases beyond the original lifetime prior to processing.

Minority carrier lifetime measured by reverse bias recovery

To assess the carrier lifetime at the p-n junction in the finished solar cell, a square sample of a solar cell from segment B7 was processed into individual diodes and measured by the reverse recovery technique. After diode isolation and contact evaporation, the diode was tested and the resulting oscilloscope waveform is shown in Figure 4.3. To improve contact quality, the diode sample was annealed at 600˚C for 60 s to form eutectic silicide contacts on

either side of the diode, mounted on the test apparatus and aged four months at room temperature. The sample was tested again, with the resulting oscilloscope waveform shown in Figure 4.4.

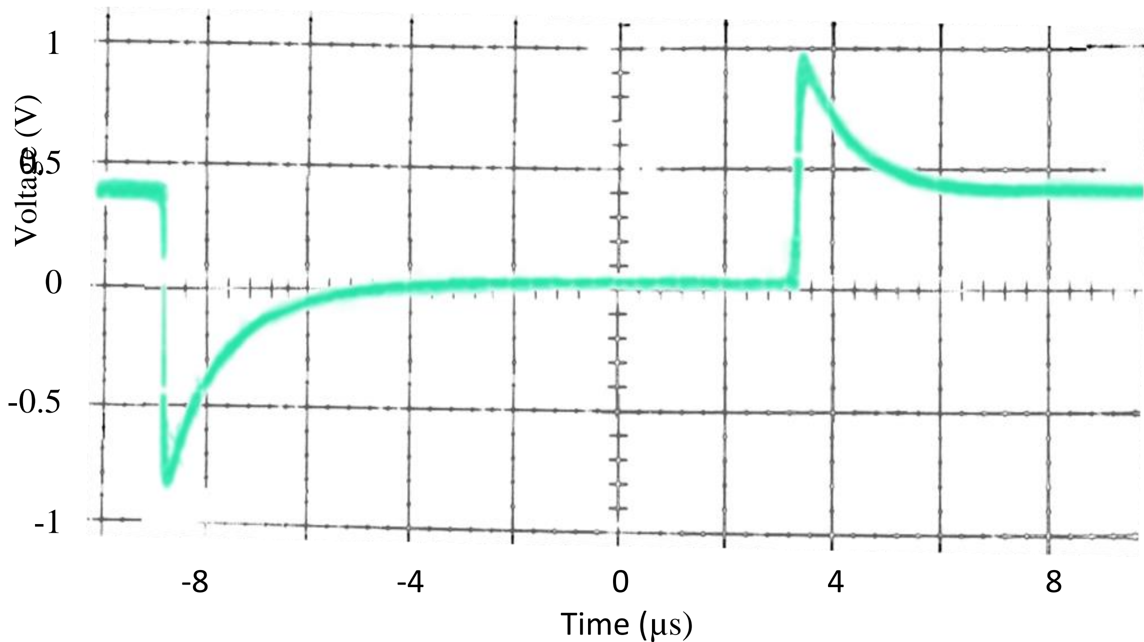

Figure 4.3: Waveform of voltage indicating current flowing across the solar cell p-n junction, as bias is changed from forward to reverse (left side) and from reverse to forward (right side).

The waveform initially obtained from reverse recovery testing is not as expected. A constant reverse current for some period after the switch to reverse bias as seen in Figure 2.9 was expected from which one can obtain a reliable carrier lifetime measurement. Instead, the signal immediately after reverse biasing is obscured by the large voltage decay seen in Figure 4.3. This decay is clearly not due to charge storage in the depletion region because a similar decay is observed when switching to forward bias. This feature was believed to be caused by

contact capacitance. To eliminate this capacitance introduced by contacts gold was evaporated onto the sample backside and annealed to form a silicide layer between each contact and the silicon, and aged to ensure a high quality connection.

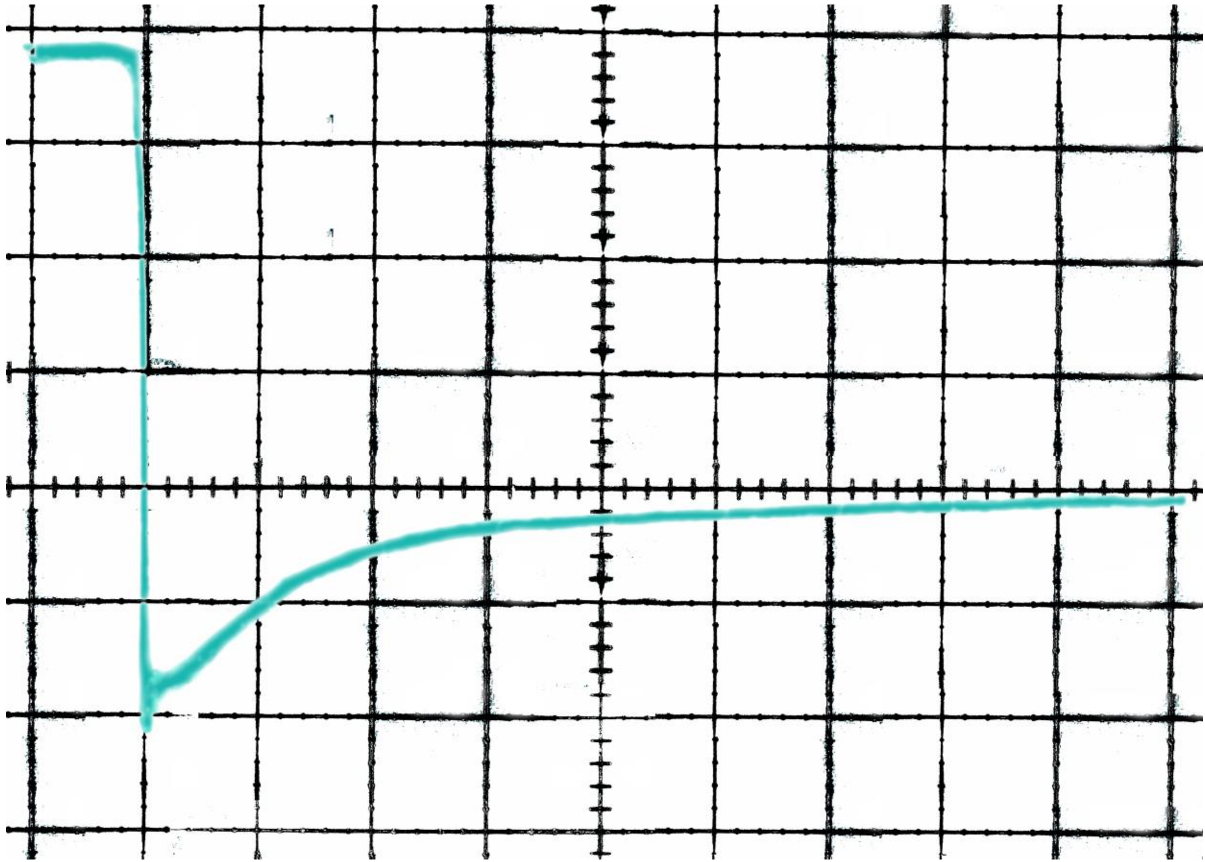

Figure 4.4: Oscilloscope trace of voltage indicating current across the diode as bias is switched from forward to reverse. The charge storage time is calculated from the period of negative voltage immediately following the switch from forward to reverse bias.

Figure 4.4 shows the waveform observed on the oscilloscope during reverse recovery testing of the diode sample with improved contacts. Unlike the waveform in Figure 4.3, the voltage does not increase beyond its steady-state value upon switching from reverse to forward bias (Figure C1, Appendix C). This indicates that the reverse voltage must be due to charge storage and not stray capacitance. The shape of the reverse voltage decay is rather different, as well. Upon close inspection, the point of maximum reverse current can be identified as "ringing", an artifact introduced by the pulse generator. The voltage quickly increases from this artifact, and remains fairly constant for a very brief period before beginning to decay to the steady-state value. The length of time between switching from forward to reverse bias is charge storage time t_s, and is approximately 0.175 μs for the test in Figure 4.4. This measurement can be used to approximate carrier lifetime τ using Equation 2.10, yielding τ = 0.52 μs.

Alternatively the carrier lifetime can be approximated using the time from reverse biasing to the time at which the reverse current has decayed to 10% of its greatest magnitude, the reverse recovery time t_{rr}. Carrier lifetime is then determined using t_{rr} and the time to peak reverse current t_p with Equation 2.11. Taking t_{rr} = 3.4 μs and t_p = 0.03 μs, τ is approximately 0.32 μs.

These carrier lifetime measurements on solar cell diodes are less than those measured by EBIC on solar cells, but greater than the lifetime of samples between phosphorus annealing and metallization. The lower solar cell lifetime could be related to the annealing step performed to form front and rear contacts for the sample. Due to the high diffusivity of hydrogen in

silicon[72] the hydrogen which was passivating defects may be partially removed, thus decreasing the lifetime.

Carrier lifetime may also be measured directly by techniques such as μPCD or QSSPC. While QSSPC can only create very coarse distributions of lifetime using single-point measurement (Figure 3.5), μPCD measurements can be used to create a lifetime map to identify regions and features of different lifetime. μPCD measurements were performed by Dr. Markevich on unprocessed wafers, post-boron, and post-boron/phosphorus processed wafers. The μPCD lifetime maps of each segment at each processing step are shown in Figure 4.5.

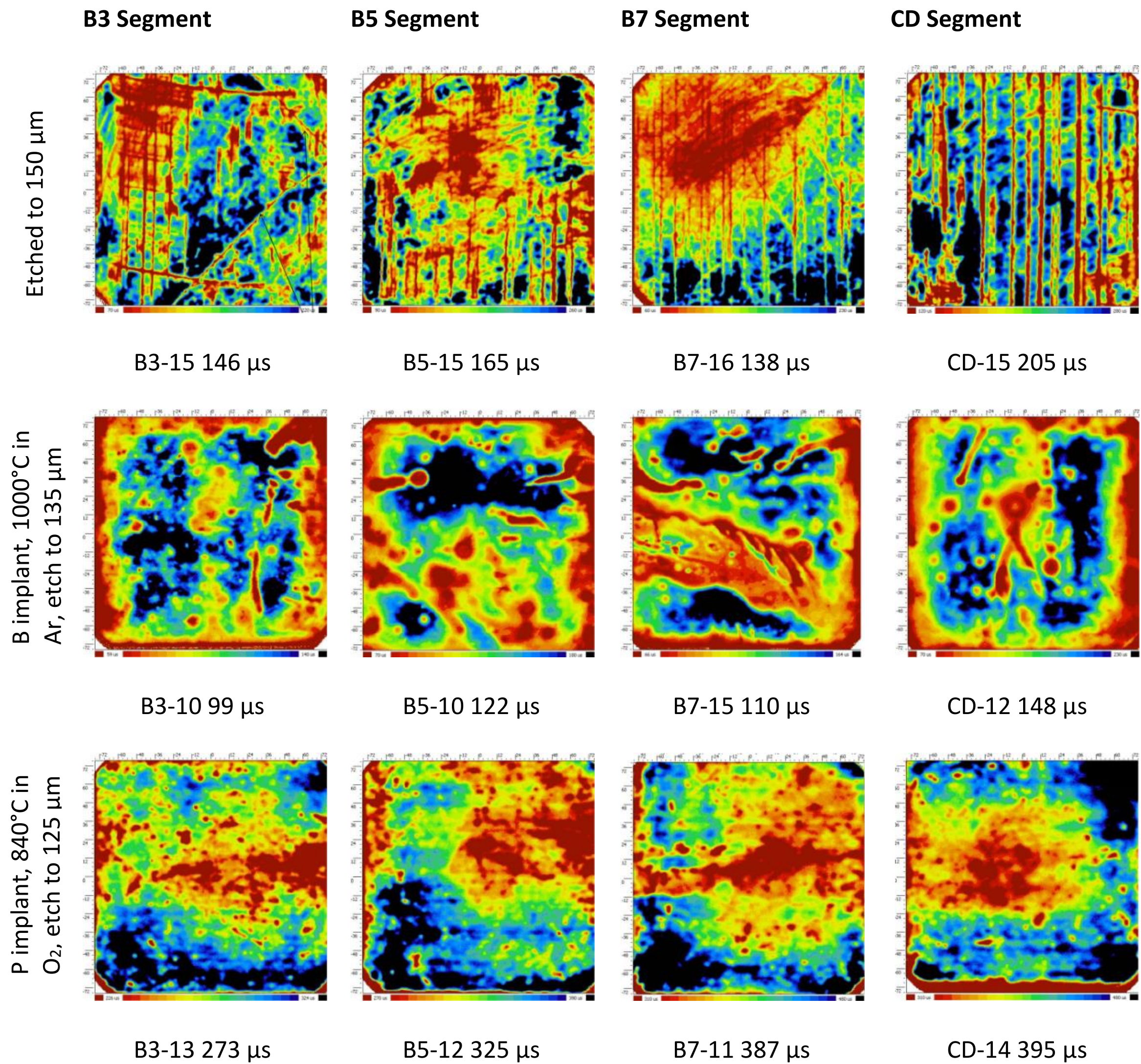

Figure 4.5: Lifetime maps measured by µPCD for all sample sets after each thermal processing step with average lifetime. Maps are 150 mm on each side, omitting ~3 mm on each side of the 156 mm pseudo-square wafers. Color scale is relative to each map and not common to all maps. µPCD lifetime measurements were made by Dr. Markevich at the University of Manchester.

The lifetime maps in Figure 4.5 give average carrier lifetime across each wafer. According to these results, lifetime decreases after boron implantation and anneal and increases beyond the original values after phosphorus implantation and anneal. These results are in sharp

contrast to those obtained by EBIC, which show that lifetime changes little after boron processing and decreases significantly after phosphorus processing. However, unlike EBIC, μPCD lifetime measurements are dependent on surface recombination velocity *S*.

The understanding of surface recombination velocity *S* of wafers passivated by iodine and ethanol would allow for the determination of bulk lifetime τ_b of samples implanted and annealed during processing, and their comparison with the unprocessed samples. However, this passivation seems much less consistent than the Al_2O_3 passivation and yields sporadic results. Table 3.3 shows calculated *S* for each as-received sample set, note that these values are ~5-10 times higher than those deduced from the QSSPC data in Figure 3.6.This inconsistency is due to the strong dependence of the surface passivation on passivation solution concentration, light exposure, native oxide and time spent soaking.[36] The time required to measure a sample (~45 min), possible minor variations in the iodine/ethanol solution and inconsistent light exposure due to ambient light can therefore lead to a dramatic effect on the measured effective minority carrier lifetime.

Table 4.1: ***S*** **calculated for μPCD measurements of unprocessed wafers**

Segment	τ_b **(μs)**	N_d **(cm^{-3})**	***t*** **(cm)**	τ_{eff} **(μPDC, μs)**	***S*** **(cm/s)**
B3	4710	1.91×10^{15}	0.015	146	50.4
B5	4670	1.42×10^{15}	0.015	165.3	44.3
B7	4520	1.07×10^{15}	0.015	138	53.4
CD	4210	2.90×10^{15}	0.015	204.9	35.1

While using *S* values of 30-50 cm/s yields some reasonable values for bulk lifetime τ_b of boron implanted and annealed samples, after phosphorus implantation and anneal the wafers must have *S* somewhere below 20 cm/s otherwise the calculated τ_b becomes unreasonably high. The inconsistencies observed in the iodine/ethanol samples compared to Al_2O_3 passivated samples suggest variation in the degree of passivation by iodine/ethanol, which prevents any discussion of lifetime changes during thermal processing. The changes in carrier lifetime through the cell process in Figure 4.5 cannot be valid, and therefore cannot be compared to the EBIC measurements.

Although μPCD lifetime maps cannot be used to determine changes in lifetime with processing, they reveal the spatial distribution of carrier lifetime across each wafer. The unprocessed wafers all exhibit bands of low lifetime which are parallel to the sawing direction. Therefore, these bands are attributed to sub-surface damage from wafer sawing. This conclusion is supported by the thickness etched from each side of the wafer before measurement of unprocessed samples. The unprocessed wafers were etched to a thickness of

150 μm, meaning that only 15 μm were removed from each side. Compared to the depth of subsurface damage determined to be 22 μm in Chapter III, 7 μm may remain below the wafer surface. Subsequent wafer samples measured by μPCD were etched to a thickness of 135 μm or less, such that at least 22 μm are removed from each surface. The absence of low-lifetime features parallel to saw marks in the processed samples after this deeper etch supports the depth of damage of 22 μm determined in Chapter III.

The distribution of high and low lifetimes after boron implantation and annealing is unclear at present, but the diffuse nature of lifetime variation compared to other maps in Figure 4.5 suggests that the 1000˚C anneal after implantation may have facilitated some diffusion which affected lifetime. After phosphorus implantation and annealing, the distribution changes and again shows features parallel to the saw marks originally present on the wafers. However, these features exhibit only slight variations in carrier lifetime and are attributed to surface roughness and thickness variation remaining from the saw marks. Because these features are visible and not obscured by other features as with the boron treated samples, the samples measured after phosphorus processing are believed to exhibit a better representation of the true distribution of lifetime across the wafers. Besides the variations in lifetime arising from surface features, the lifetime appears lower near the center of all samples measured after phosphorus processing. This feature may be due to the crystal growth process, but is not perfectly symmetric about the wafer center. Therefore, the exact cause for the lower lifetime in the center of the wafers remains unknown.

Light beam induced current (LBIC) mapping of C-CZ solar cells

While μPCD is an effective technique for mapping lifetime changes across wafer samples, LBIC can be used to qualitatively map the efficiency of solar cells. The local efficiency is dependent on minority carrier lifetime, among other factors, and is used to identify flaws in the solar cell from substrate quality or processing. LBIC maps were measured by Brian Rounsaville at the Georgia Institute of Technology. Figure 4.6 presents one LBIC scan of a solar cell from each sample segment.

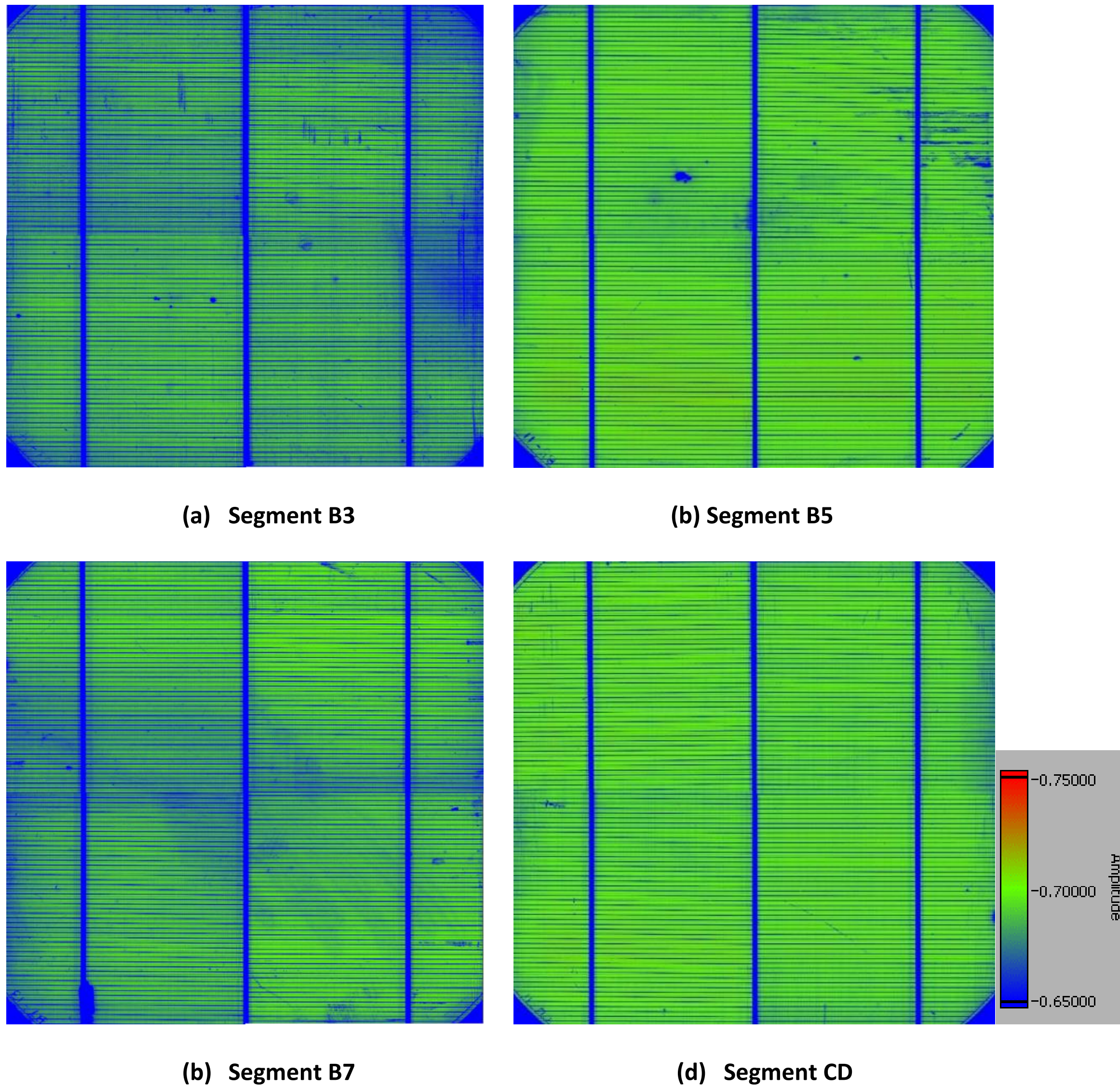

Figure 4.6: Light beam induced current maps of solar cells from wafers **(a)** B3-14, **(b)** B5-11, **(c)** B7-13 and **(d)** CD-11. Color scale represents relative current intensity, each map is approximately 6 inches square. The regular, symmetrical pattern of dark lines is the front metal contact. LBIC measurements performed by Brian Rounsaville at Georgia Institute of Technology.

The regions of low contrast in these LBIC scans indicate a lower current and therefore lower efficiency. Some features such as the center region of B7-13 appear to be processing

defects due to their irregular shape, which are not representative of the commercialized process used by SunEdison because the cells were processed in an experimental environment. However, short and rough features of low current also appear on each map in vertical and horizontal orientations. These features are consistently parallel to only the saw marks visible for each wafer, and not screen printed front contacts. Therefore, these regions of low contrast are attributed to sub-surface damage remaining from the sawing process. In order to determine how much damage potentially remains after solar cell fabrication, the thickness of the solar cell substrates was measured with a barrel micrometer after removing front and back contacts with Piranha solution. The thickness of the solar cells was determined to be 152 ± 3 μm, indicating that 8 μm of damage remains below the surface. The damage is not so profound and visible as that of the unprocessed wafer samples mapped by μPCD in Figure 4.5 because of the hydrogen passivation during solar cell fabrication. Although the damage appears to have been passivated, it clearly affects solar cell efficiency based on the lower signal in the LBIC scans (Figure 4.6). Comparison of these *C*-CZ solar cells to traditional CZ solar cells (Table A1, Appendix A) shows that *C*-CZ solar cells are 19.5% efficient, compared to the 20.0% efficient CZ solar cells. As discussed in Chapter III, the issue of sub-surface damage present in these *C*-CZ wafers must be addressed to maximize power conversion efficiency.

CHAPTER V: CONCLUSIONS AND FUTURE WORK

Silicon wafers grown by the *Continuous*-Czochralski process for photovoltaic applications were characterized to better understand the material and identify potential causes for efficiency loss in photovoltaic cells. A minority carrier lifetime study was performed on these samples after each thermal processing step of a modern passivated emitter and rear solar cell (PERC) fabrication process. The carrier lifetime analysis revealed changes in lifetime through the solar cell fabrication process. The material analysis of these samples provides insight on the growth methods used to produce the sample wafers and and on how they are passivated.

The residual thermal stress of the *Continuous*-Czochralski crystals was measured by nanoindentation and preferential etching techniques while the depth of mechanical damage from the sawing process was measured by angle polishing and subsequent SEM examination after defect etching. Field-effect surface passivation of the *C*-CZ wafers by Al_2O_3 was investigated using quasi-steady state photoconductance carrier lifetime measurements. Variations in electron donor concentration were determined along wafer radius by four point probe, and thermal donors were analyzed using deep level transient spectroscopy. Changes in carrier lifetime through solar cell fabrication were determined using an electron beam induced current technique, and carrier lifetime within a solar cell structure was measured using a reverse bias recovery technique. Microwave photoconductance decay measurements were used to generate lifetime maps at various stages in the fabrication, and light beam induced current measurements were used for qualitative mapping of solar cell efficiency.

Residual stress analysis of the *C*-CZ wafers indicates very low thermal stress remaining from the growth process, and subsequent lifetime maps do not exhibit any features characteristic of residual stress. The absence of residual stress may arise from the low melt level and steady-state nature of the C-CZ growth process and suggests that these wafers are suitable for photovoltaic applications. However, angle polished samples indicate that mechanical saw damage can penetrate as deep as 22 μm in some regions which may affect solar cell efficiency if not removed or passivated. This is much deeper than previously reported for fixed-abrasive wafer sawing, which suggests that the sawing process used to cut these wafers requires modification. In agreement with prior investigations on p-type Si, Al_2O_3 field-effect surface passivation was found to depend on electron donor concentration. However, this work is the first to report such a relationship for n-type silicon, which is currently gaining popularity as a photovoltaic substrate. Electron donor concentration was determined to vary linearly across the wafer radius due to crystal rotation during growth, and calculations indicate that the ideal location to measure electron donor concentration is 5.8 cm from the wafer center. The contribution of thermal donors was also found to depend on radius, and the thermal donor concentration was found to decrease significantly along the outer 2 cm of these wafers. Deep level transient spectroscopy confirmed this observation and revealed two significant energy levels at $E_c - 0.14$ eV and $E_v + 0.35$ eV which are attributed to a complex of oxygen and hydrogen. Because hydrogen is introduced into the solar cell during fabrication, these energy levels may have a significant effect on carrier lifetime (and therefore efficiency) of the solar cells.

The carrier lifetime of the wafer substrates was found to decrease by ~10X after phosphorus implantation and an 840˚C anneal, likely due to the relatively large mass of phosphorus creating damage in the lattice and low anneal temperature. The lifetime increased after passivation and contact formation of the solar cells because the diffused hydrogen passivates dislocations, such as those introduced during ion implantation. Lifetime measured by the reverse recovery techniqe is only slightly higher than that of samples after phosphorus implantation and anneal, suggesting that the hydrogen passivation may have been partially removed during sample preparation. Carrier lifetime in the fabricated solar cells may be increased by modifying the order of implantations such that more dislocations are removed before passivation and metalliation. Lifetime maps of unprocessed wafers after the removal of 15 µm from each surface show significant saw damage remaining below the surface, which supports the depth of saw damage measured by angle polishing and etching. After the phosphorus implant and anneal, the carrier lifetime is notably lower towards the center of the wafers. This feature may arise from the crystal growth process, or during solar cell fabrication. Solar cells fabricated from the sample wafers were tested and determined to be 19.5% efficient, compared to traditional CZ solar cells at 20.0% efficiency. While 19.5% is high, it is far from SunEdison's reported goal of 20.4% efficiency.[1] Light beam induced current mapping reveals lower efficiency in select regions of *C*-CZ solar cells which appears to be related to saw damage. This theory is supported by the thickness of the solar cell substrate, which is 152 µm. With only 14 µm removed from each side, 8 µm of damage still remains below the surface according to angle polish measurements. This sub-surface damage is responsible for at least some of the difference in efficiency between the *C*-CZ and CZ based solar cells.

In continuation of this work, the reverse recovery technique of lifetime measurement should be repeated on the same samples measured by EBIC. With the exception of the first set of samples taken before processing, all samples have p-n junctions formed on one surface and are therefore suitable for reverse recovery measurement. Repeating the results in Figure 4.2 using the reverse recovery method will reinforce the EBIC results and allow for proper comparison between the two techniques. For additional quantitative measurement of lifetime through the cell process, the wafers measured by microwave photoconductance decay should be etched further to ensure all saw damage is removed, passivated by Al_2O_3, and measured again using the same technique and conditions. Surface recombination velocity would then be calculated as discussed in Chapter III, allowing for quantitative comparison of bulk carrier lifetimes. This experiment would also yield spatial variations in carrier lifetime across wafers, unobscured by any saw damage. This study would benefit from transient spectroscopy analysis of defect energy levels in samples from each stage in the fabrication process to confirm sources of lifetime changes such as remnant saw damage, implantation damage, and/or hydrogen passivation. Finally, the solar cell fabrication process should be repeated after etching the *C*-CZ wafer samples to 135 μm or less to properly remove saw damage. Subsequent comparison with traditional CZ cells would then provide a quantitative comparison of efficiency.

The fixed-abrasive sawing process used to cut these wafers should be modified to reduce the depth of subsurface damage and thus effects on solar cell efficiency. Alternatively, the chemical etching process in which sub-surface damage is removed before solar cell fabrication may be lengthened to remove more material. To reduce the effects of ion implantation damage, performing the boron implantation and anneal after the plosphorus

implantation and anneal may reduce the effects of implantation damage due to the higher post-boron anneal temperature.

This findings presented in this work indicate that silicon wafers grown by the *Continuous*-Czochralski process may be suitable for use as photovoltaic cell substrates, but several issues have been identified. Further investigation of these wafers is necessary to determine the efficacy of *Continuous*-Czochralski silicon wafers for photovoltaic applications.

REFERENCES

1. Mehta, S. The Roadmap to El Dorado: SunEdison's PV Module Technology Strategy *Greentech Solar* **2013**.
2. SEIA. *Solar Energy Facts: Q3 2014*; www.seia.org, **2014**.
3. S Esterly, R. G. *2013 Renewable Energy Data Handbook*; United States Department of Energy: www.doe.gov, **2013**.
4. Haaren, R. Massive Growth of Wind and Solar in the USA (Graphs) *Divvy Green* **2013**.
5. Wray, P. Cutting PV Costs, Part 2: Process Improvements Vs. Science Breakthroughs **2009**.
6. Kölker, H., The Behaviour of Nonrotational Striations in Silicon. *Journal of Crystal Growth* **1980**, *50*, 852-858.
7. Li, B. Q., Solidification Processing of Materials in Magnetic Fields. *The Journal of Minerals, Metals and Materials Society* **1998**, *50*.
8. NREL *PV Faqs*; United States Department of Energy: www.doe.gov, **2004**.
9. Green, M. A.; Emery, K.; Hishikawa, Y.; Warta, W.; Dunlop, E. D., Solar Cell Efficiency Tables (Version 41). *Prog. Photovoltaics* **2013**, *21*, 1-11.
10. Anselmo, A.; Prasad, V.; Koziol, J.; Gupta, K. P., Numerical and Experimental Study of a Solid Pellet Feed Continuous Czochralski Growth Process for Silicon Single Crystals. *Journal of Crystal Growth* **1993**, *131*, 247-264.

11. Wang, C.; Zhang, H.; Wang, T.; Zheng, L., Solidification Interface Shape Control in a Continuous Czochralski Silicon Growth System. *Journal of Crystal Growth* **2006**, *287*, 252-257.

12. Lin, W.; Benson, K. E., The Science and Engineering of Large- Diameter Czochralski Silicon Crystal Growth. *Annual Review of Materials Science* **1987**, *17*, 273-298.

13. Anselmo, A.; Koziol, J.; Prasad, V., Full-Scale Experiments on Solid-Pellets Feed Continuous Czochralski Growth of Silicon Crystals. *Journal of Crystal Growth* **1996**, *163*, 359-368.

14. Zulehner, W., Czochralski Growth of Silicon. *Journal of Crystal Growth* **1983**, *65*, 189-213.

15. Ryu, K. In *Understanding and Experimental Validation of Resistivity/Lifetime Specification for Promising High Efficiency N-Type Si Solar Cell Architectures* Silicon Solar Consortium Review, **2012**.

16. Anselmo, A.; Koziol, J.; Prasad, V., Full-Scale Experiments on Solid-Pellets Feed Continuous Czochralski Growth of Silicon Crystals. *Journal of Crystal Growth* **1996**, *163*, 359-368.

17. Simoen, E.; Claeys, C.; Loo, R.; Degryse, O.; Clauws, P.; Job, R.; Ulyashin, A.; Fahrner, W., Characterisation of Oxygen and Oxygen-Related Defects in Highly- and Lowly-Doped Silicon. *Materials Science and Engineering B* **2003**, *102*, 207-212.

18. Job, R.; Ulyashin, A. G.; Fahrner, W. R.; Simoen, E.; Claeys, C.; Tonelli, G., Hydrogen Enhanced Thermal Donor Formation in Oxygen Enriched High Resistive

Float-Zone Silicon. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms* **2002**, *186*, 116-120.

19. Yakimov, E.; Feklisova, D.; Castaldini, A.; Cavallini, A.; Cadeo, S.; Pizzini, S., Oxygen Precipitate Precursors and Low Temperature Gettering Processes. II: DLTS Analysis of Deep Levels Associated to Oxide Precipitates. *Materials Science in Semiconductor Processing* **1999**, *2*, 69-74.

20. Cadeo, S.; Pizzini, S.; Acciarri, M.; Cavallini, A., Oxygen Precipitate Precursors and Low Temperature Gettering Processes. I. Segregation of Oxygen and Thermal Donor Generation in the 600–850°C Range. *Materials Science in Semiconductor Processing* **1999**, *2*, 57-68.

21. Gregorkiewicz, T.; Bekman, H. H. P. T., Thermal Donors and Oxygen-Related Complexes in Silicon. *Materials Science and Engineering: B* **1989**, *4*, 291-297.

22. Götz, W.; Pensl, G.; Zulehner, W., Observation of Five Additional Thermal Donor Species TD12 to TD16 and of Regrowth of Thermal Donors at Initial Stages of the New Oxygen Donor Formation in Czochralski-Grown Silicon. *Physical Review B* **1992**, *46*, 4312-4315.

23. Lee, Y. J.; von Boehm, J.; Nieminen, R. M., Interstitial Oxygen Loss and the Formation of Thermal Double Donors in Si. *Applied Physics Letters* **2001**, *79*, 1453.

24. Lee, Y. J.; von Boehm, J.; Pesola, M.; Nieminen, R. M., Aggregation Kinetics of Thermal Double Donors in Silicon. *Physical Review Letters* **2001**, *86*, 3060-3063.

25. Antonova, I. V.; Popov, V. P.; Shaimeev, S. S., DLTS Study of Nucleation Stage of Oxygen Precipitate in Silicon. *Physica B: Condensed Matter* **1998**, *253*, 123-130.

26. Zeghbroeck, V., *Principles of Semiconductor Devices and Heterojunctions*; Prentice Hall PTR, 2007.

27. Schroder, D., *Semiconductor and Material Device Characterization*, Third ed.; Wiley-IEEE Press, 2006.

28. Watanabe, N.; Kondo, Y.; Ide, D.; Matsuki, T.; Takato, H.; Sakata, I., Characterization of Polycrystalline Silicon Wafers for Solar Cells Sliced with Novel Fixed-Abrasive Wire. *Progress in Photovoltaics: Research and Applications* **2010**, *18*, 485-490.

29. Meinel, B.; Koschwitz, T.; Blocks, C.; Acker, J., Comparison of Diamond Wire Cut and Silicon Carbide Slurry Processed Silicon Wafer Surfaces after Acidic Texturisation. *Materials Science in Semiconductor Processing* **2014**, *26*, 93-100.

30. Chen, W.; Liu, X.; Li, M.; Yin, C.; Zhou, L., On the Nature and Removal of Saw Marks on Diamond Wire Sawn Multicrystalline Silicon Wafers. *Materials Science in Semiconductor Processing* **2014**, *27*, 220-227.

31. Chen, K.; Liu, Y.; Wang, X.; Zhang, L.; Su, X., Novel Texturing Process for Diamond-Wire-Sawn Single-Crystalline Silicon Solar Cell. *Solar Energy Materials and Solar Cells* **2015**, *133*, 148-155.

32. Chung, C. H.; Tsay, G. D.; Tsai, M. H., Distribution of Diamond Grains in Fixed Abrasive Wire Sawing Process. *Int. J. Adv. Manuf. Technol.* **2014**, *73*, 1485-1494.

33. Holland, O. W.; Xie, L.; Nielsen, B.; Zhou, D. S., Implantation of Si under Extreme Conditions: The Effects of High Temperature and Dose on Damage Accumulation. *Journal of Electronic Materials* **1996**, *25*, 99-106.

34. Trucks, G. W.; Raghavachari, K.; Higashi, G. S.; Chabal, Y. J., Mechanism of HF Etching of Silicon Surfaces - a Theoretical Understanding of Hydrogen Passivation. *Physical Review Letters* **1990**, *65*, 504-507.

35. Luke, K. L.; Cheng, L.-J., Analysis of the Interaction of a Laser Pulse with a Silicon Wafer: Determination of Bulk Lifetime and Surface Recombination Velocity. *Journal of Applied Physics* **1987**, *61*, 2282.

36. Batra, N.; Vandana; Kumar, S.; Sharma, M.; Srivastava, S. K.; Sharma, P.; Singh, P. K., A Comparative Study of Silicon Surface Passivation Using Ethanolic Iodine and Bromine Solutions. *Solar Energy Materials and Solar Cells* **2012**, *100*, 43-47.

37. Msaad, H.; Michel, J.; Lappe, J. J.; Kimerling, L. C., Electronic Passivation of Silicon Surfaces by Halogens. *Journal of Electronic Materials* **1994**, *23*, 487-491.

38. Hoex, B.; Heil, S. B. S.; Langereis, E.; van de Sanden, M. C. M.; Kessels, W. M. M., Ultralow Surface Recombination of C-Si Substrates Passivated by Plasma-Assisted Atomic Layer Deposited Al_2O_3. *Applied Physics Letters* **2006**, *89*, 042112.

39. ASTM, Determination of Radial Interstitial Oxygen Variation in Silicon Wafers. In *F951 - 01*, 2001.

40. ASTM, Substitutional Atomic Carbon Content of Silicon by Infrared Absorption. In *F1391 - 93*, 2000.

41. Williams, K. R.; Muller, R. S., Etch Rates for Micromachining Processing. *Journal of Microelectromechanical Systems* **1996**, *5*, 256-269.

42. Zandi, K.; Arzi, E.; Izadi, N.; Mohajerzadeh, S.; Haji, S.; Abdi, Y.; Soleimani, E. A., Study of Bulk Micromachining for <100> Silicon. *Eur. Phys. J.-Appl. Phys* **2006**, *35*, 7-12.

43. Schimmel, D. G., A Comparison of Chemical Etches for Revealing <100> Silicon Crystal Defects. *Journal of The Electrochemical Society* **1976**, *123*, 734-741.

44. Secco d' Aragona, F., Dislocation Etch for (100) Planes in Silicon. *Journal of The Electrochemical Society* **1972**, *119*, 948-951.

45. Pharr, G. M., Measurement of Mechanical Properties by Ultra-Low Load Indentation. *Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing* **1998**, *253*, 151-159.

46. Anstis, G. R.; Chantikul, P.; Lawn, B. R.; Marshall, D. B., A Critical-Evaluation of Indentation Techniques for Measuring Fracture-Toughness .1. Direct Crack Measurements. *J. Am. Ceram. Soc.* **1981**, *64*, 533-538.

47. ASTM, Measuring the Depth of Crystal Damage of a Mechanically Worked Silicon Slice Surface by Angle Polishing and Defect Etching. In *F950 - 02*, **2002**.

48. Ummartyotin, S.; Juntaro, J.; Wu, C.; Sain, M.; Manuspiya, H., Deposition of PEDOT: PSS Nanoparticles as a Conductive Microlayer Anode in OLEDS Device by Desktop Inkjet Printer. *Journal of Nanomaterials* **2011**, *2011*, 7.

49. Topsoe, H., Geometric Factors in Four Point Resistivity Measurement. **1968**.

50. Lang, D. V., Deep-Level Transient Spectroscopy: A New Method to Characterize Traps in Semiconductors. *Journal of Applied Physics* **1974**, *45*, 3023.

51. Benton, J. L., Characterization of Defects in Semiconductors by Deep Level Transient Spectroscopy. *Journal of Crystal Growth* **1990**, *106*, 116-126.

52. Bonard, J. M.; Ganière, J. D., Quantitative Analysis of Electron-Beam-Induced Current Profiles across P–N Junctions in GaAs/Al0.4Ga0.6As Heterostructures. *Journal of Applied Physics* **1996**, *79*, 6987-6994.

53. Parish, C. M.; Russell, P. E., On the Use of Monte Carlo Modeling in the Mathematical Analysis of Scanning Electron Microscopy–Electron Beam Induced Current Data. *Applied Physics Letters* **2006**, *89*, 192108.

54. United States DoD., Test Methods for Semiconductor Devices. In *MIL-STD-750D*, 1995.

55. Hu, J.; Merkle, L.; Menoni, C.; Spain, I., Crystal Data for High-Pressure Phases of Silicon. *Physical Review B* **1986**, *34*, 4679-4684.

56. Bhushan, B.; Li, X. D., Micromechanical and Tribological Characterization of Doped Single-Crystal Silicon and Polysilicon Films for Microelectromechanical Systems Devices. *J. Mater. Res.* **1997**, *12*, 54-63.

57. Ebrahimi, F.; Kalwani, L., Fracture Anisotropy in Silicon Single Crystal. *Materials Science and Engineering: A* **1999**, *268*, 116-126.

58. Johansson, S.; Schweitz, J. A., Contact Damage in Single-Crystalline Silicon Investigated by Cross-Sectional Transmission Electron-Microscopy. *J. Am. Ceram. Soc.* **1988**, *71*, 617-623.

59. Puech, P; Demagneot, F; Pizani, S. *Strain Determination around Vickers Indentation on Silicon Surface by Raman Spectroscopy*; Cambridge University Press: Cambridge, ROYAUME-UNI, **2004**; Vol. 19, p 8.

60. Kray, D.; Glunz, S., Investigation of Laser-Fired Rear-Side Recombination Properties Using an Analytical Model. *Progress in Photovoltaics: Research and Applications* **2006**, *14*, 195-201.

61. Dicker, J., Analyse Und Simulation Von Hocheffizienten Silizium-Solarzellenstrukturen Fur Industrielle Fertigungstechniken. Thesis, *University of Konstanz* **2003**.

62. Dingemans, G.; Seguin, R.; Engelhart, P.; Sanden, M. C. M. v. d.; Kessels, W. M. M., Silicon Surface Passivation by Ultrathin Al_2O_3 Films Synthesized by Thermal and Plasma Atomic Layer Deposition. *physica status solidi (RRL) – Rapid Research Letters* **2010**, *4*, 10-12.

63. Dingemans, G.; Kessels, W. M. M., Status and Prospects of Al_2O_3-Based Surface Passivation Schemes for Silicon Solar Cells. *Journal of Vacuum Science & Technology A* **2012**, *30*, 040802.

64. Cotter, J. E.; Guo, J. H.; Cousins, P. J.; Abbott, M. D.; Chen, F. W.; Fisher, K. C., P-Type Versus N-Type Silicon Wafers: Prospects for High-Efficiency Commercial Silicon Solar Cells. *Electron Devices, IEEE Transactions on* **2006**, *53*, 1893-1901.

65. Schmidt, J.; Veith, B.; Brendel, R., Effective Surface Passivation of Crystalline Silicon Using Ultrathin Al_2O_3 Films and Al_2O_3/SiN_x Stacks. *physica status solidi (RRL) – Rapid Research Letters* **2009**, *3*, 287-289.

66. Schmidt, J.; Merkle, A.; Brendel, R.; Hoex, B.; de Sanden, M. C. M. v.; Kessels, W. M. M., Surface Passivation of High-Efficiency Silicon Solar Cells by Atomic-Layer-Deposited Al_2O_3. *Progress in Photovoltaics: Research and Applications* **2008**, *16*, 461-466.

67. Hoex, B.; Schmidt, J.; Bock, R.; Altermatt, P. P.; van de Sanden, M. C. M.; Kessels, W. M. M., Excellent Passivation of Highly Doped P-Type Si Surfaces by the Negative-Charge-Dielectric Al_2O_3. *Applied Physics Letters* **2007**, *91*, 112107.

68. Lamp, C. D.; Jones, B. D., Changes in the Silicon Thermal Donor Energy Level as a Function of Anneal Time. *Applied Physics Letters* **1991**, *58*, 2114.

69. Götz, W.; Pensl, G.; Zulehner, W.; Newman, R. C.; McQuaid, S. A., Thermal Donor Formation and Annihilation at Temperatures above 500°C in Czochralski-Grown Si. *Journal of Applied Physics* **1998**, *84*, 3561.

70. Rashkeev, S. N.; Di Ventra, M.; Pantelides, S. T., Hydrogen Passivation and Activation of Oxygen Complexes in Silicon. *Applied Physics Letters* **2001**, *78*, 1571-1573.

71. Andersen, O. S. Electrical Properties of Hydrogen-Related Defects in Crystalline Silicon. Thesis, *Universiy of Manchester*, **2002**.

72. Van Wieringen, A.; Warmoltz, N., On the Permeation of Hydrogen and Helium in Single Crystal Silicon and Germanium at Elevated Temperatures. *Physica* **1956**, *22*, 849-865.

73. Cowern, N. E. B.; Janssen, K. T. F.; Jos, H. F. F., Transient Diffusion of Ion-Implanted B in Si - Dose, Time, and Matrix Dependence of Atomic and Electrical Profiles. *Journal of Applied Physics* **1990**, *68*, 6191-6198.

74. Sopori, B. L.; Jones, K. M.; Deng, X.; Matson, R.; Al-Jassim, M.; Tsuo, S.; Doolittle, A.; Rohatgi, A. In Hydrogen in Silicon: Diffusion and Defect Passivation, *Photovoltaic Specialists Conference*, **1991**., Conference Record of the Twenty Second IEEE, 7-11 Oct 1991; **1991**; pp 833-841 vol.2.

75. Hoex, B.; Schmidt, J.; van de Sanden, M. C. M.; Kessels, W. M. M. In Crystalline Silicon Surface Passivation by the Negative-Charge-Dielectric Al_2O_3, *Photovoltaic Specialists Conference*, **2008**. PVSC '08. 33rd IEEE, 11-16 May 2008; 2008; pp 1-4.

76. Takeda, M.; Ohnuki, S.; Watanabe, S.; Abe, H.; Naramoto, H.; Okamoto, P. R.; Lam, N. Q., Effect of Stress and Impurities on Preferential Amorphization on Grain Boundaries in Polycrystalline Silicon. In *Microstructural Processes in Irradiated Materials*, Zinkle, S. J.; Lucas, G. E.; Ewing, R. C.; Williams, J. S., Eds. Materials Research Society: Warrendale, **1999**; Vol. 540, pp 37-42.

77. Follstaedt, D. M.; Knapp, J. A.; Myers, S. M., Mechanical Properties of Ion-Implanted Amorphous Silicon. *J. Mater. Res.* **2004**, *19*, 338-346.

78. Youssef, K.; Yu, X.; Seacrist, M.; Rozgonyi, G., Understanding the Effect of Impurities and Grain Boundaries on Mechanical Behavior of Si Via Nanoindentation of (110)/(100) Direct Si Bonded Wafers. *J. Mater. Res.* **2011**, *27*, 349-355.

79. Brunwin, R.; Hamilton, B.; Jordan, P.; Peaker, A. R., Detection of Minority-Carrier Traps Using Transient Spectroscopy. *Electronics Letters* **1979**, *15*, 349-350.

APPENDICES

Appendix A

Solar cell fabrication

Solar cells from all four segments were fabricated by Brian Rounsaville at the Georgia Institute of Technology which is our SiSoC partner university. Wafers were first etched in 40% KOH at 80°C to clean the wafer and remove sub-surface damage. This was followed by a slow etch to form a random pyramid texture on the surface. Boron was implanted to a concentration of 5 x 10^{19} cm^{-3} on the front surface to form the emitter, annealed at 1000°C in an inert ambient, and then covered by a protective layer of SiN_x. The back surface is chemically planarized, and the protective SiN_x on the front side is removed along with the boron-rich layer at the surface while leaving the emitter. Phosphorus was implanted on the back side to 10^{20} cm^{-3} and annealed at 840°C in an oxidizing ambient to form a back surface field passivation and oxidize both sides. SiN_x was then deposited on both sides to complete the passivating anti-reflective layers. The bus bar pattern on the front surface and dot arrays on the back side of each cell were screen printed using Ag/Al paste and quickly co-fired around 700°C for a few seconds to form front and back contacts. Silver paste is applied to the rear face and cured at 200°C for 3 min to form a solderable rear contact. The process flow is illustrated in Figure A1.

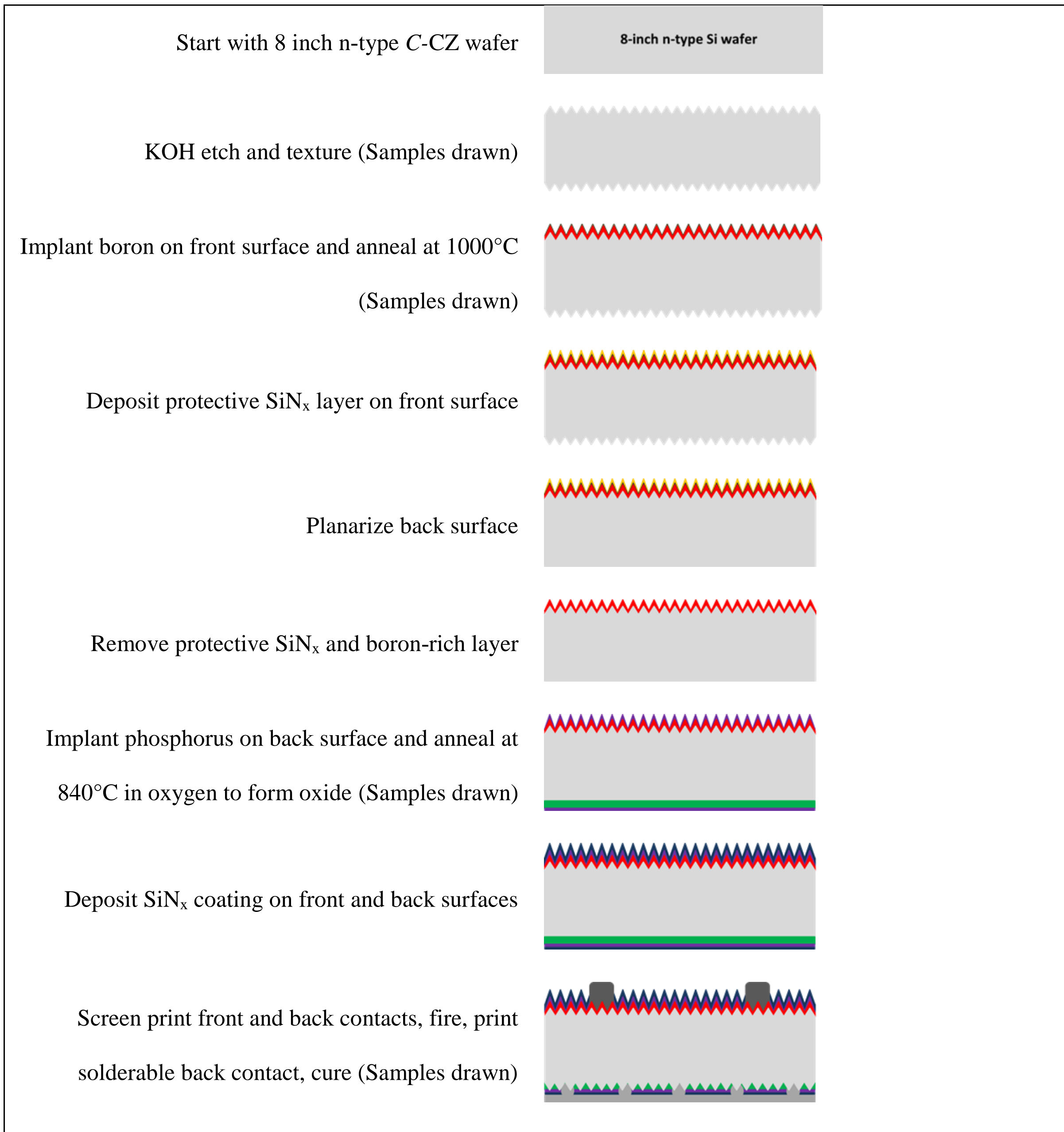

Figure A1: Process flow for fabrication of solar cells from C-CZ wafers produced at the Georgia Institute of Technology. Note the locations in the process sequence where wafer samples were drawn for testing.

Three solar cells were produced by the above fabrication sequence from each of the four sample segments, for a total of 12 cells. These cells were characterized after fabrication by the Georgia Institute of Technology to determine open circuit voltage (V_{oc}), short circuit current (I_{sc}), short circuit current density (J_{sc}), fill factor (FF), efficiency and ideality factor, as well as series and shunt resistances. A summary of these data averaged for each segment is presented in Table A1.

Table A1: Properties of C-CZ solar cells fabricated by the Georgia Institute of Technology

Segment	V_{oc} (V)	I_{sc} (A)	J_{sc} (A/m^2)	FF (%)	Efficiency (%)	Ideality factor	R_{series} (Ω-cm^2)	R_{shunt} (Ω-cm^2)
B3	0.643	9.09	38.04	79.91	19.55	1.05	0.543	7730
B5	0.645	9.11	38.14	79.50	19.56	1.07	0.587	9610
B7	0.643	9.13	38.19	79.42	19.49	1.08	0.573	10134
CD	0.645	9.12	38.14	79.01	19.44	1.10	0.607	11357

p-n junction diode formation

For the study of wafers by minority carrier transient spectroscopy and reverse recovery techniques, it was necessary to form p-n junction diodes from the fabricated solar cells. The following process isolates small regions of the p-n junction emitter of the solar cell for local study. A soft mask was ordered, consisting of a solid fill with 1 mm diameter holes, separated from each other by 2 mm in a hexagonal pattern. A 4 in by 4 in square sample was cleaved

from the center of a fabricated solar cell and soaked in Piranha solution to remove all metal contacts. The wafer was then soaked in an HF solution to remove the SiN_x and SiO_2 antireflective coating. This was followed by an extended soak in Piranha to remove metallic contamination and a final HF dip to remove the oxide layer. This cleaned wafer was taped to a sturdier dummy wafer using kapton tape. The mounted wafer was coated in JSR NFR 16D2 55cp negative photoresist and exposed using the mask and rinsed in NMP solvent to leave only 1 mm discs of photoresist covering the eventual diode locations. A reactive ion etch was performed at room temperature to remove approximately 8 μm of material, leaving the diodes on mesas. This step removes all p-type doping on the exposed regions, thus leaving the p-type layers of the diodes isolated from one another. To passivate the vertical walls of newly formed diodes, pressure-enhanced chemical vapor deposition of silicon oxide was performed to deposit approximately 50 nm SiO_2 on top of the sample. Note that this oxide also covers the photoresist remaining on top of the diodes, which is used to remove the oxide over the diodes. The top of each diode was manually scraped with a sharp glass rod to remove a spot, approximately 0.5 mm diameter, of the oxide layer covering each diode. The mounted sample was then soaked in acetone, which dissolved both the kapton tape and the newly exposed photoresist. After cleaning in methanol, the sample was re-taped onto the substrate with more kapton tape, masked and coated in Shipley S1813 positive photoresist. After exposure, photoresist covered all sample area except the tops of the diodes. To form an ohmic contact for probing on the top layer, aluminum was thermally evaporated onto the masked sample and the mask dissolved beneath the metal to leave isolated contacts. To prevent alteration of the electrical state of the samples due to thermal processing, temperatures were maintained near

room temperature during all processing steps. All work from the first lithography step to the contact formation was performed by the staff at the NCSU Nanofabrication Facility.

In order to ensure the best possible contact with minimal contact capacitance, 50 to 100 nm Au was deposited onto the back surface of the sample. The sample was then fired at 400°C for 60 s to form AlSi on the front contact and AlAu on the rear contact.

Sample preparation for optical lifetime measurements

Wafer sample surfaces must be properly prepared to limit the effects of surface recombination on effective lifetime before performing optical measurement techniques which are discussed later. To provide sufficient surface passivation, all mechanical damage initially present must be removed by etching in KOH or HNA solutions. After damage removal, the high recombination potential of dangling surface bonds must also be negated. A solution of iodine in methanol or ethanol can be used to directly interact with these dangling bonds and reduce surface recombination.[27] To maintain surface passivation throughout a measurement scan, a wafer is sealed in a transparent plastic bag with the solution and no air, and the measurement is performed through the bag. Although this method is simple, fast, safe and cost effective, many variable factors affecting the consistency of the passivation reduce the precision of the technique.[36]

Alternative to the iodine passivation, a field effect passivation technique can be employed which indirectly reduces the surface recombination velocity by preventing one charge carrier type from coming near the surface by placing a thin film on the surface containing a static charge. While many films are used for passivation, Al_2O_3 deposited by

Atomic Layer Deposition (ALD) was chosen because of its high passivation qualities and reproducibility. ALD deposited Al_2O_3 contains a fixed negative charge, which repels negative electrons.[75]

Al_2O_3 passivation is performed by cycling trimethylaluminum and water vapor at 170°C until 30 nm are deposited, which is followed by an anneal at 425°C in N_2 to densify the film and activate the passivation. Field effect passivation by Al_2O_3 was performed under the direction of Dr. Hahn at the University of Konstanz.

Nanoindentation measurements

Stress in a silicon wafer can be measured indirectly by measuring the hardness. Under applied stress, silicon is known to undergo phase transformation upon applied pressure to β-Sn phase[55] near 11 GPa, which is unstable below 2 GPa. Upon formation of this phase transformation near dislocations, defects or precipitates, some of the material relaxes to form areas of amorphous silicon.[76] The hardness of silicon is dependent on its crystal structure, 12 - 13 GPa for the (100) surface of diamond cubic silicon[56] to 10 GPa the amorphous phase.[77]

Hardness measurements can therefore be used to locate dislocation fields in silicon by the decrease in hardness resulting from the local presence of amorphous silicon. Previous studies[78] have shown that nanoindentation can be used to compare hardness and therefore stress across a wafer. A Hysitron TriboIndenter was selected to perform nanoindentation measurements due to its automated mapping function, allowing many points to be measured automatically to form a map or profile. 7 mN loading was used for indentation to maintain consistency with references.[56, 78] Calibration was performed before measuring each sample to

ensure consistent results. Hardness was measured every 1 mm along the radius of each unprocessed sample wafer after sufficient polishing, with 8 indents made at each radial location. All nanoindentation measurements were performed by colleagues Schiessl and Dr. Youssef.

Minority carrier transient spectroscopy (MCTS)

Minority Carrier Transient Microscopy (MCTS) involves the same principles as DLTS, but employs optical stimulation to generate minority carriers as opposed to majority carriers[79] and was performed at the University of Manchester. The barrier must be thin enough such that above-bandgap light may penetrate to the junction and generate carriers via the photovoltaic effect. Under reverse bias, no current will flow from the semiconductor into the metal of a Schottky barrier because the majority carriers are held out of the depletion region. Minority carriers, should they be present in the semiconductor, will cross the barrier. Stimulating the generation of minority carriers on the semiconductor side by backside illumination causes current to flow across the Schottky barrier, which is then detected by the capacitance meter. As the illumination is instantly switched off, the illuminated capacitance value decays back to that value measured in the dark. This the capacitance decay is used in the same manner as DLTS to characterize defect levels. It is important to distinguish, though, that DLTS of Schottky barriers measures only majority carrier traps while MCTS only measures minority carrier traps. Because solar cells are limited by the minority carrier lifetime, MCTS measurements are a critical supplement to DLTS. All MCTS measurements were made by Dr. Markevich at the University of Manchester.

Microwave photoconductance decay (μPCD)

μPCD measures the minority carrier lifetime of a sample point by point to create a high resolution lifetime map ideal for identifying features of low or high lifetime across a wafer or sample. μPCD employs a laser light source which quickly pulses to generate electron-hole pairs in the semiconductor. As the laser pulse ends, the minority carriers generated in the sample begin to recombine, and thus, their concentration decays with time. This concentration can be instantaneously measured via the conductivity of the sample region. To maintain a contactless measurement, μPCD employs a microwave probe incident on the sample region. The intensity of reflected microwave signal relative to the incident probe, which depends on the conductivity of the material, is detected and converted to the instantaneous minority carrier concentration. This measurement is made at a high frequency, and a plot of minority carrier concentration vs. time is constructed. Software associated with the instrument automatically calculates minority carrier lifetime from this decay curve, and lifetime is reported for a specific measurement location. Typically, both the light source and microwave probe are fixed to a measurement head, which is scanned across a sample to generate a lifetime map. For a more detailed description of μPCD, see Chapter 7 of Semiconductor Material and Device Characterization by Schroder.[27] In this study, μPCD was performed by Dr. Markevich at the University of Manchester using a Sinton WT2000-PVN.

Quasi steady-state photoconductance (QSSPC)

Lifetime can also be measured by the QSSPC technique, in which the sample is exposed to an incandescent flash lamp to excite carriers. The generated minority carrier concentration is

measured using inductive coupling from below the sample to determine conductivity. The flash lamp is turned off and with a time constant of several ms the intensity of emitted light decays as the filament cools. Although the light (and therefore generated carriers) decays with time, the carrier concentration behaves in a steady-state manner as long as the time constant of the flash lamp is larger than the carrier lifetime. With a known flash lamp decay constant and the excess carrier concentration continuously measured by the inductive probe, the decay constant of the excess carriers (minority carrier lifetime) can be calculated. A complete description of the mechanism for calculating carrier lifetime by the QSSPC technique is covered in Chapter 7 of Semiconductor Material and Device Characterization by Schroder.[27] Note that unlike μPCD, QSSPC is not a focused point measurement and instead measures lifetime over a diffuse region. Therefore QSSPC cannot be used to create a true lifetime map, but instead point measurements or a very coarse distribution by manual point measurement can be made. QSSPC measurements were made under the direction of Dr. Hahn at the University of Konstanz using a Sinton WT2000 PVN and by SunEdison using a Sinton WT2000 PVN.

Light beam induced current (LBIC)

LBIC is a very simple technique used to assess variations in the quality of a solar cell. A light source such as a laser is focused onto a small location of a cell, which generates current in short-circuit mode via the photovoltaic effect. The generated photocurrent is collected using the front and back contacts applied to the solar cell during fabrication. The exact amount of current generated depends on the quality of the solar cell in the local region sampled. By scanning this light beam over the sample cell while mapping the resulting current, a map of

solar cell quality is produced. LBIC measurements were performed by Brian Rounsaville at the SiSoC partner Georgia Institute of Technology on a custom instrument.

Appendix B

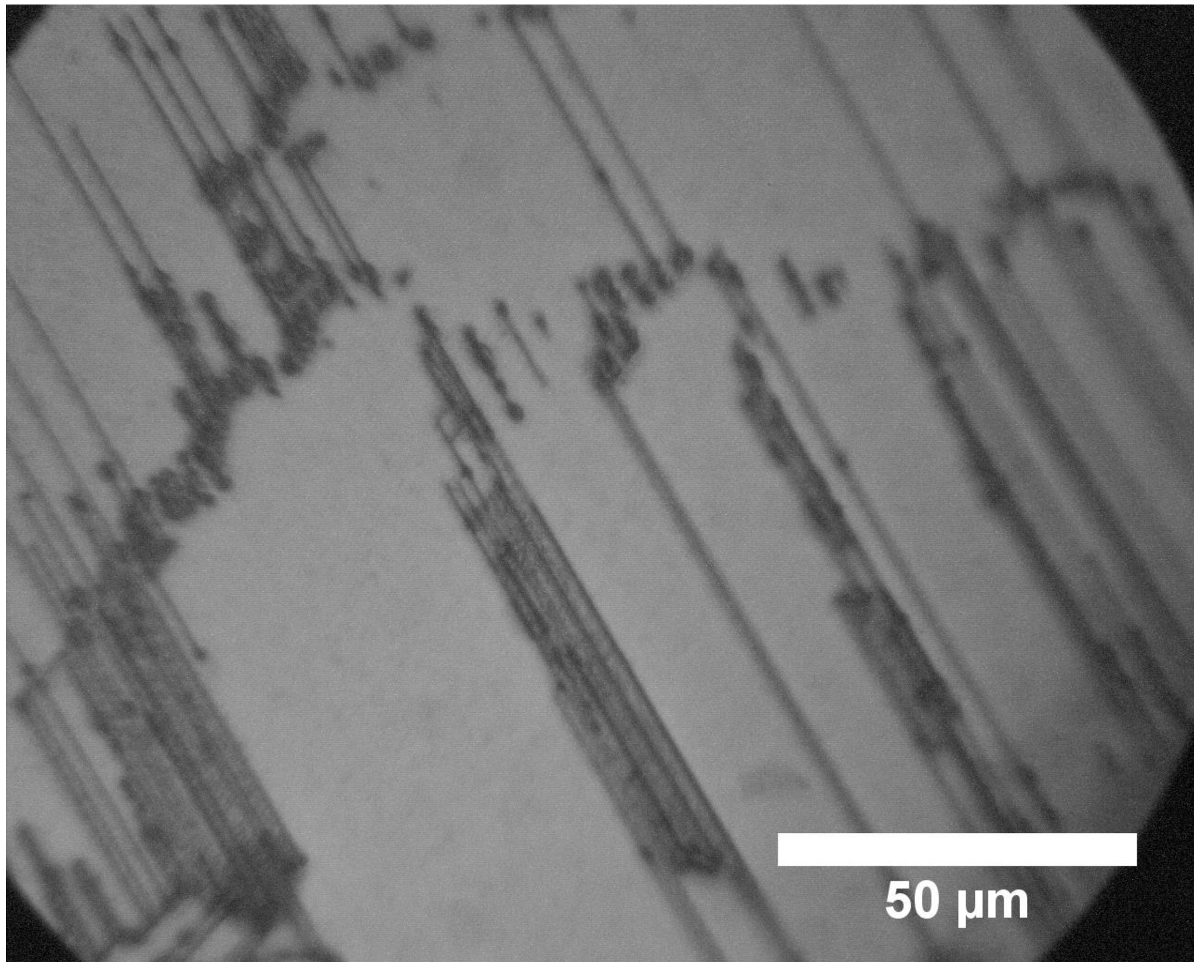

Figure B1: DIC micrograph of a scrap multicrystalline wafer etched in Secco solution for 3 min to ensure proper etch conditions used with *C*-CZ samples. All dark pits and lines represent crystal defects, proving that the etch conditions produce features on defects.

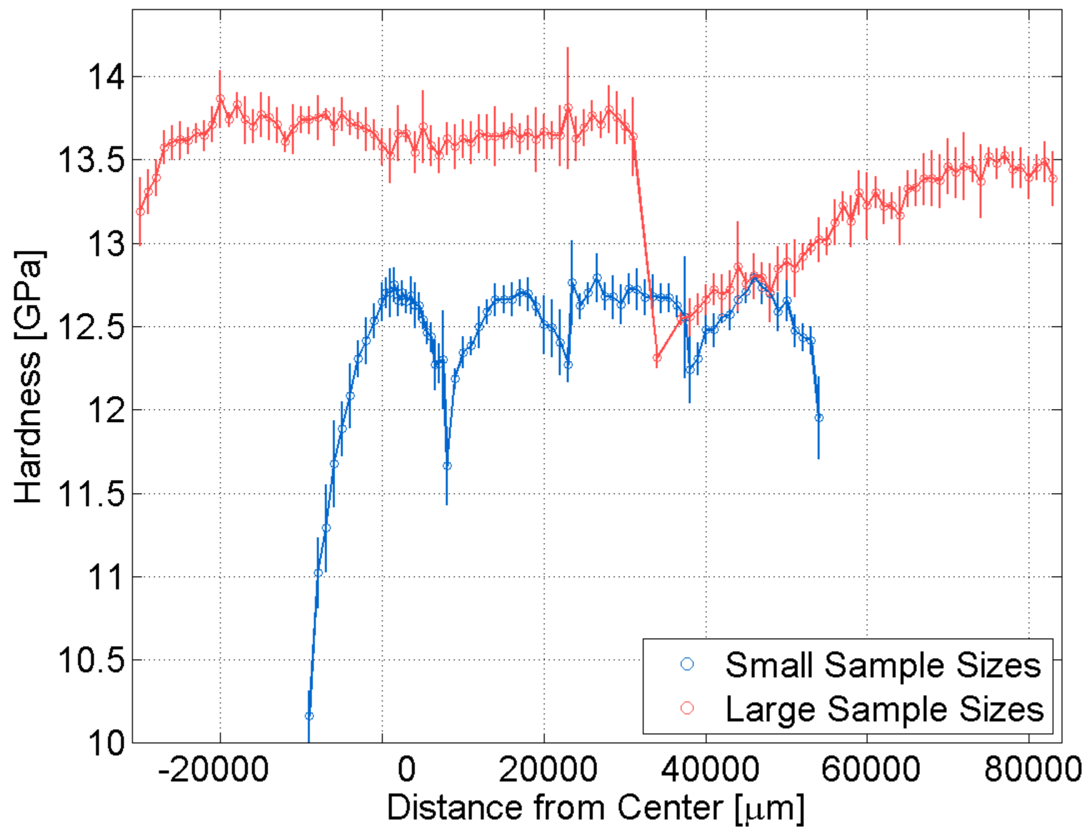

Figure B2: Nanoindentation scans across two samples from wafer CD-08 (red) and four samples from wafer CD-05 (blue). Hardness was much lower at the edges of each sample, indicating the position of all sample pieces. CD-05 hardness remains fairly constant across r = 20000 – 5000 μm, indicating that the varying hardness in CD-08 is an artifact and not representative of the wafer. These measurements do not indicate the presence of dislocations from residual stress. Vertical lines represent standard deviation at each measurement location. All nanoindentation scans performed by colleagues Schiessl and Dr. Youssef.

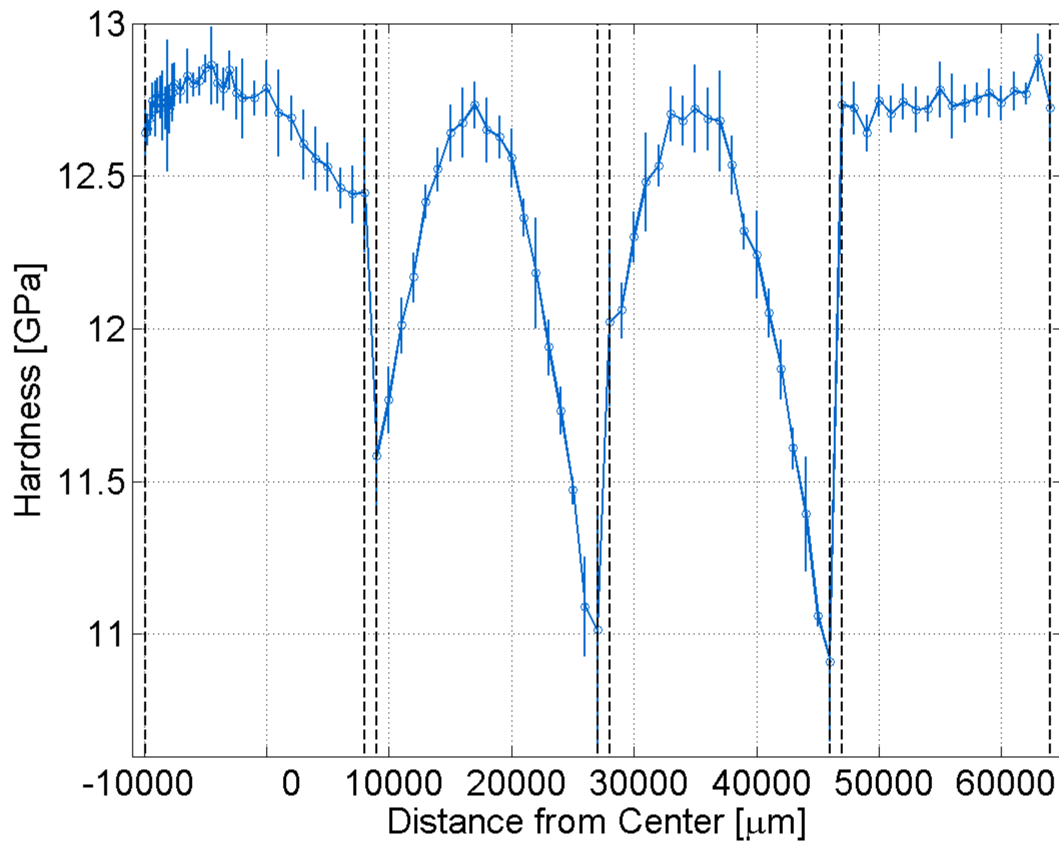

Figure B3: Nanoindentation scan across four samples from wafer B5-06. The locations of the sample edges are indicated by vertical, dashed lines. Despite abrupt decreases in hardness due to polishing artifacts, the peak hardness is fairly constant across the wafer indicating no measurable dislocations from residual stress. All nanoindentation scans performed by colleagues Schiessl and Dr. Youssef.

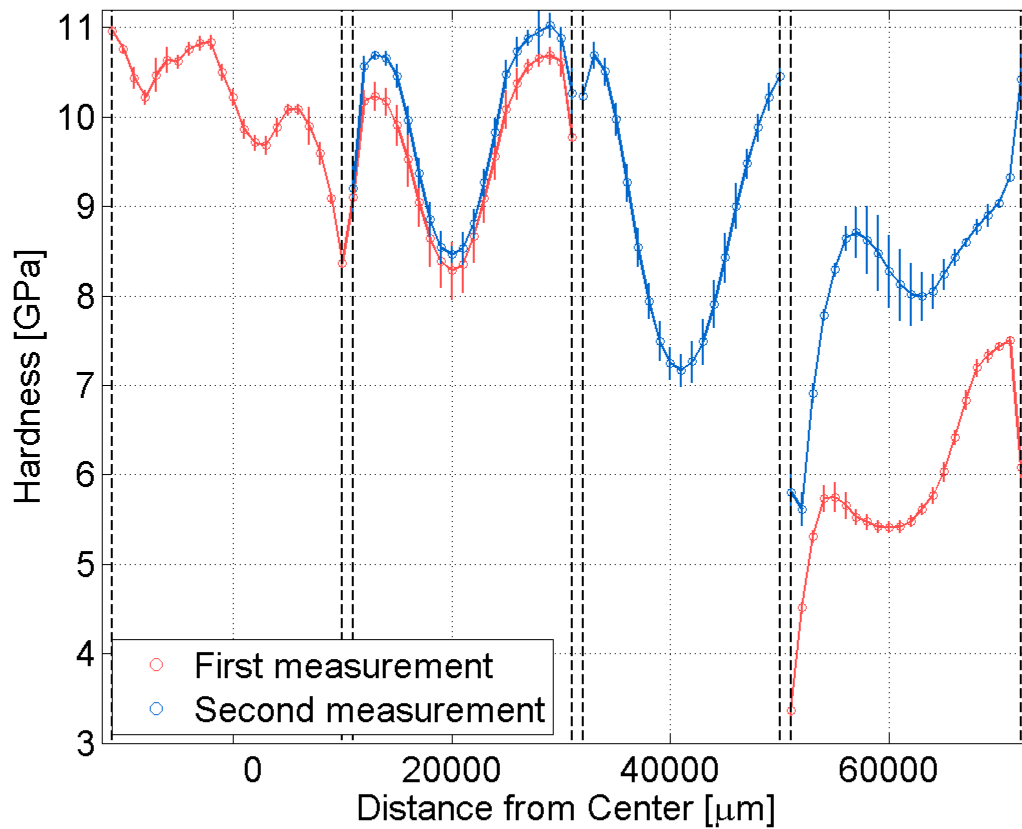

Figure B4: Two nanoindentation scans taken on the same four samples from wafer B3-06 show that while there are notable decreases in hardness across *r,* these features correspond well to the location of the samples, the edges of which are indicated by vertical dashed lines. Comparing repeated measurements that were made on the same sample pieces show that the hardness results of this sample are not always reproducible. All nanoindentation scans performed by colleagues Schiessl and Dr. Youssef.

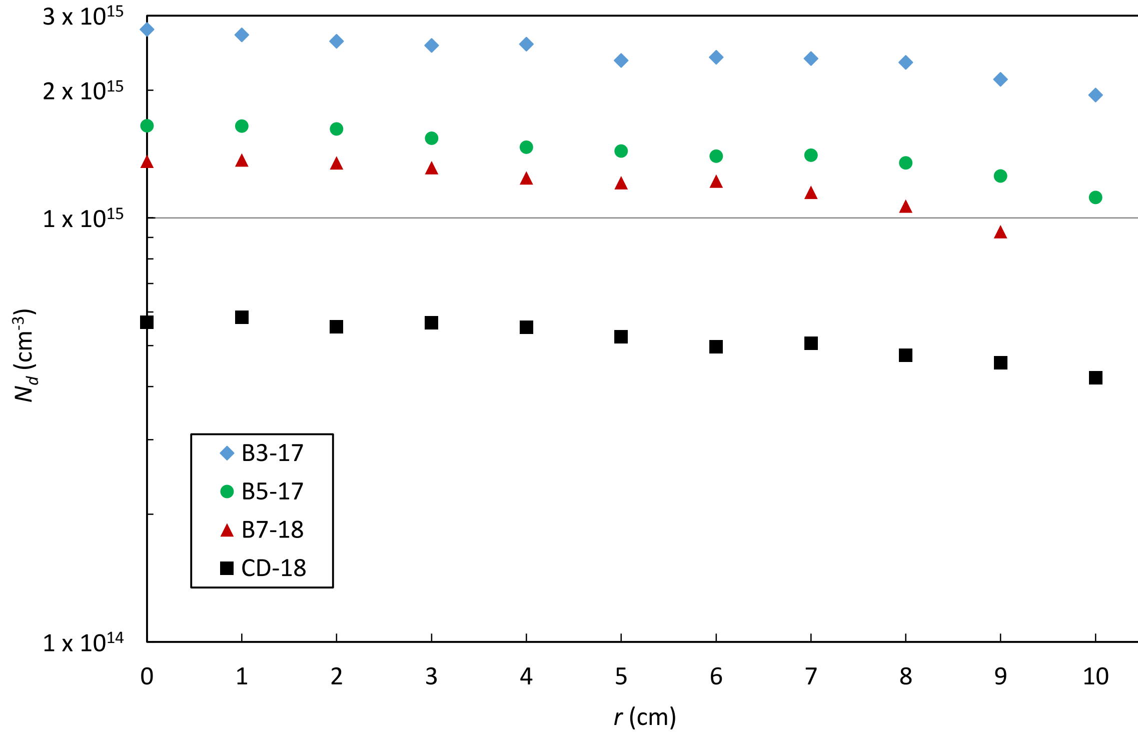

Figure B5: Electron donor concentration N_d calculated from four point probe resistivity measurements taken along the radius r of wafers from each sample segment. Because the samples used to make these measurements were narrow enough that edge effects significantly altered the calculation, these results show that all sample segments exhibit the same electron donor properties. This indicates that the N_d vs. r relationship proposed in Figure 3.8 for segment CD will hold for all other sample segments.

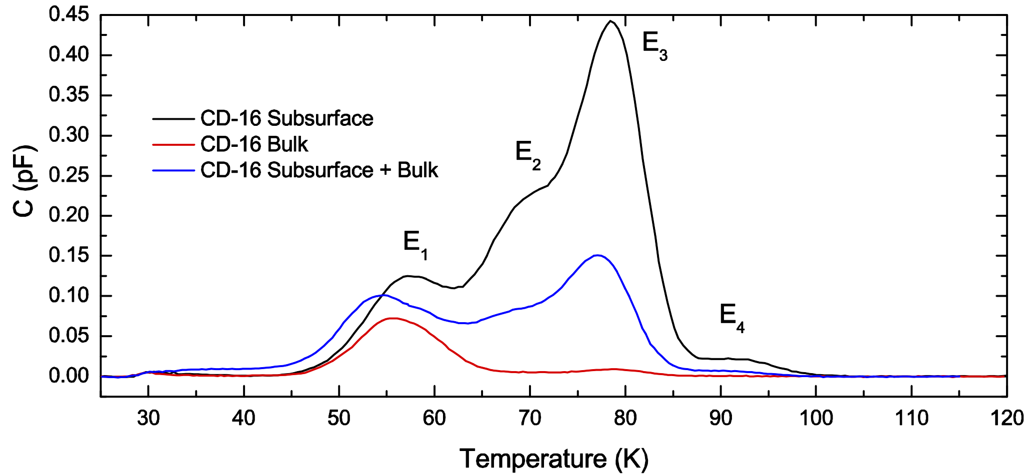

Figure B6: DLTS spectra varying bias and pulse bias samples the sub-surface (black) and bulk (red) regions, as well as a mixture of both (blue). The relative stability of the E_1 thermal donor (55 K peak) indicates little or no dependence on depth. The E_2, E_3, and E_4 oxygen-hydrogen trap, however, is only present near the surface. t_p = 1 ms. Subsurface: U_b = -3 V, U_p = 0 V. Bulk: U_b = -9 V, U_p = -4 V. Mixture: U_b = -7 V, U_p = 0.2 V. Measurements made by Dr. Markevich at the University of Manchester.

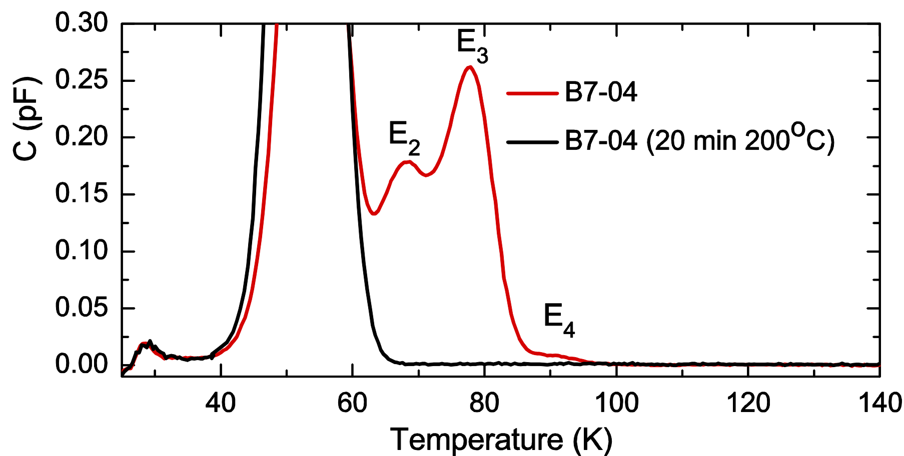

Figure B7: DLTS spectra of sample CD-16 before (red) and after (blue) annealing at 200°C. The complete elimination of energy levels E_2- E_4 indicates that all are related to the O2i-H complex, which is formed and removed below 200°C. U_b = -3 V, U_p = 0 V, tp = 1 ms. Measurements made by Dr. Markevich at the University of Manchester.

Appendix C

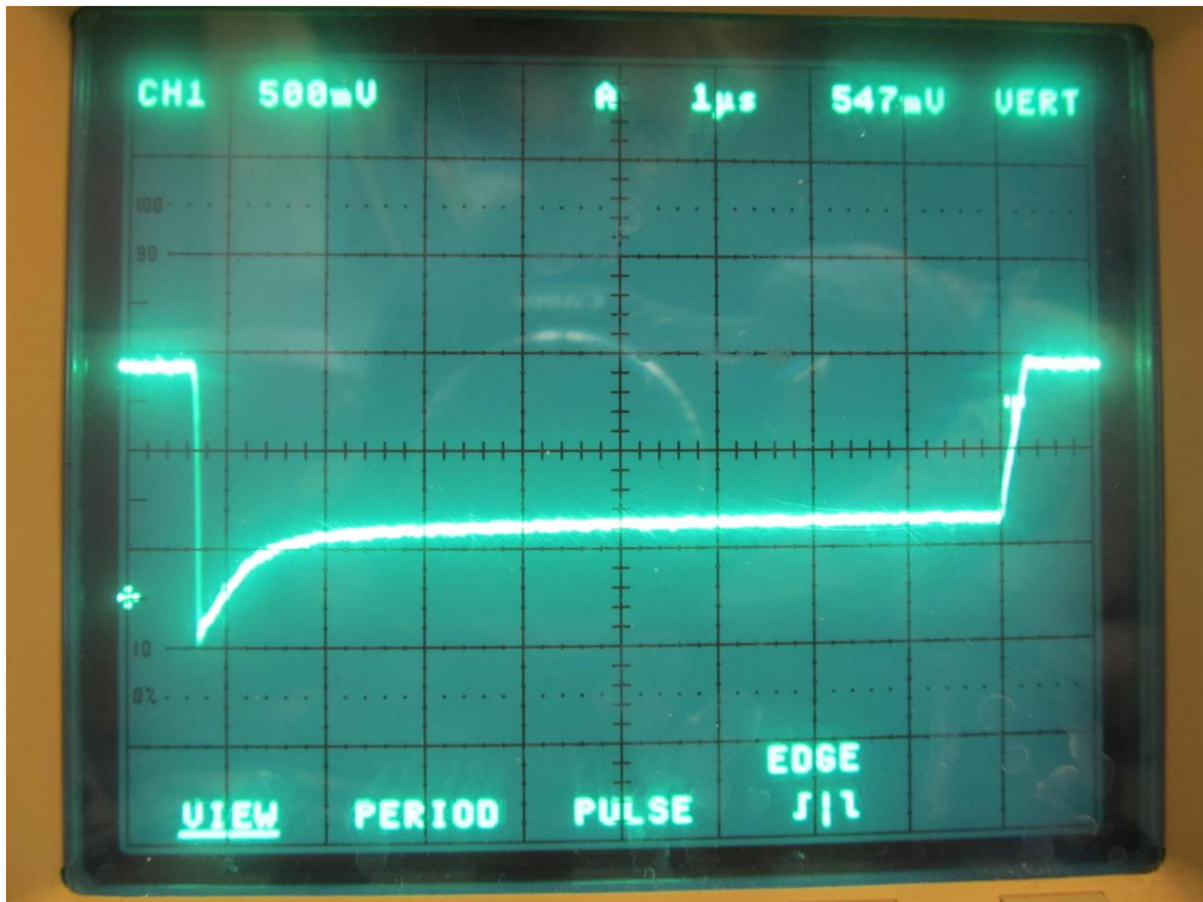

Figure C1: Photograph of oscilloscope trace indicating reverse bias recovery of the same diode tested in Figure 3.4. The absence of a spike in voltage upon return to forward bias indicates that the reverse voltage seen immediately upon reverse bias is due to charge storage in the depletion region, as opposed to the capacitance effects seen in Figure 3.3.