ABSTRACT

ZHANG, LIQI. Design, Fabrication and Test of SiC MOSFET-Gate Driver Co-packaged Power Module. (Under the direction of Dr. Alex Q. Huang)

With the increasing interest and application of wideband gap devices, due to the Figure of Merit of conduction loss and output capacitance, higher switching speed could be achieved. However, the parasitic parameters from the package as well as the circuit will cause large voltage overshoot and ringing or undershoot, which introduces more switching losses or even damage the devices, causing system reliability issue.

To eliminate this influence and realize better switching performance, a 1200V 80mΩ CREE SiC MOSFET-gate driver co-packaged power module is designed, fabricated and tested. Compared with discrete TO247 packaged SiC MOSFET of same ratings, bare die SiC MOSFET has far less parasitic parameters, and it can be packaged together with gate driver closely, thus is used in the co-packaged module development. It is designed to have a small power loop thus the parasitic parameters from the module is minimized. By using Kelvin connection, common source stray inductance is reduced to zero. Zero external gate resistance is also applied to guarantee fast switching. Double pulse test under 510 kHz, 800V, 10A with zero-voltage-switching (ZVS) turn-on and hard switching turn-off shows the module has far less ringing and lower turn-off loss than TO-247 package. It can be used for ultrahigh frequency switching with noise free operation.
Design, Fabrication and Test of SiC MOSFET-Gate Driver Co-packaged Power Module

by
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A thesis submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the degree of Master of Science

Electrical Engineering

Raleigh, North Carolina

2015

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_______________________________
Dr. Srdjan Lukic
DEDICATION

To my great parents, Chunxia and Shunbao.

To my beloved girlfriend, Lisha.
BIOGRAPHY

Liqi Zhang was born in Ma’anshan, Anhui, P.R.China in 1991. He obtained bachelor’s degree of Electrical Engineering and Automation from Chongqing University, Chongqing, P.R.China in 2013. Then he joined North Carolina State University as a master student in Electrical Engineering. Now he is pursuing Ph.D. under Dr. Alex Q. Huang.
ACKNOWLEDGMENTS

Thanks to Dr. Alex Q. Huang. Dr. Huang’s great thoughts in the cutting edge power electronics technology and overall blueprint of the future smart grid have inspired me to think harder and deeper. I have also learnt to think systematically from him as well.

Thanks to Dr. Wensong Yu for prompt and kind guidance on the research road. And thanks Dr. Srdjan Lukic to be my committee member.

Thanks to all my friends and best wishes to all!
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CHAPTER 1 INTRODUCTION: WHY SiC? WHY CO-PACKAGE?

1.1 Silicone V.S. Silicone Carbide

SiC (Silicon Carbide) is a compound semiconductor comprised of silicon (Si) and carbon (C). Compared to Si, SiC has ten times the dielectric breakdown field strength, three times the bandgap, and three times the thermal conductivity, which enable SiC to be an attractive material from which to manufacture power devices that can far exceed the performance of their Si counterparts [1].

Table 1 Properties comparison of Silicon and 4H-SiC [2]

<table>
<thead>
<tr>
<th>Properties</th>
<th>Silicon</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Band Gap (eV)</td>
<td>1.11</td>
<td>3.26</td>
</tr>
<tr>
<td>Relative Dielectric Constant</td>
<td>11.7</td>
<td>9.7</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm-K)</td>
<td>1.5</td>
<td>3.7</td>
</tr>
<tr>
<td>Electron Affinity (eV)</td>
<td>4.05</td>
<td>3.7</td>
</tr>
<tr>
<td>Density of States Conduction Band (cm⁻³)</td>
<td>2.80×10¹⁹</td>
<td>1.23×10¹⁹</td>
</tr>
<tr>
<td>Density of States Valence Band (cm⁻³)</td>
<td>1.04×10¹⁹</td>
<td>4.58×10¹⁸</td>
</tr>
</tbody>
</table>

Silicon carbide exhibits a critical breakdown field approximately 10X that of silicon;
enabling the development of a thinner device structure for a stated breakdown voltage, which in turn reduces the on-resistance per unit area of the device by some two orders of magnitude compared to a silicon device, thus Si has a larger on resistance than SiC when they are of the same area. So usually the device area of Si is made to be much larger than SiC in order to minimize on resistance. However, this turns out to larger capacitor in Si device, which leads to slower switching speed and higher switching losses. This higher breakdown field also enables the development of SiC MOSFETs with voltage ratings as high as 10 kV.\textsuperscript{[2]} Silicon carbide also has a thermal conductivity 2.8X higher than silicon, providing a much higher current density at a given junction temperature than a comparably-rated silicon device. With a bandgap that is approximately 3X wider than silicon, SiC devices also exhibit significantly lower leakage current at high temperature operation – by more than two orders of magnitude.\textsuperscript{[3]} The larger bandgap also means SiC devices can operate at higher temperatures. The guaranteed operating temperature of current SiC devices is from 150°C - 175°C.

\textbf{Figure 1 Comparison of silicon and 4H-SiC}
SiC also shows advantages in lower on-state losses and higher frequency switching than Si, see in Figure 2.

Figure 2 Conduction and switching loss comparison of Si and SiC with variation of junction temperature ($V_{ds} = 800$ V, $I_d = 20$ A, $R_g = 10$ $\Omega$)\cite{3}
Besides device comparison, SiC takes great advantage to Si when comparing power electronics system. First, volume and price of passive components using in SiC based system will be much less due to the higher switching speed of SiC devices. Second, less losses will generate less heat, less chip area needs less area for heat dissipation, thus the cooling size and number for SiC devices can be significantly reduced, as well as a reduction or elimination of cooling fans. Last but not least, energy cost reduction over the equipment lifecycle of SiC based system is much more than Si based system. Looking beyond the simple component costs and manufacturing expenses of a system, the true value proposition of SiC technology comes only if the overall energy savings over the lifecycle of the equipment is considered; and in some cases can be the majority of the savings potential. In systems such as a solar inverter, where cost savings are directly dependent on inverter technology, the elimination of 40% to 50% of switching losses can be the determining factor in the adoption of SiC technology.

To have some real comparison, CREE’s comparison of its own 1200V Si MOSFET and 1200V SiC MOSFET products is shown. It can be seen that SiC MOSFET shows supreme advantage than Si MOSFET with lower on resistance, more than 2X turn on loss reduction, and more than 3X turn off loss reduction. As shown in Fig. 2, the silicon MOSFET’s normalized on-state resistance (RDS(on)) increases by more than 250% from 25C to 150C, while the RDS(on) of the SiC MOSFET increase just 20% over the same temperature range. The impact of this characteristic on the thermal design of a power electronics system is significant, including the reduction of up to 50% of the thermal management hardware (fans and/or heatsinks), shown in Figure 3 and Figure 4.
Figure 3 Comprehensive comparisons of Si-based and SiC-based Inverters [4]

Industry demonstrations of SiC advantages over Si power devices

Figure 4 Comparison between Si-based and SiC-based PFC converter [5]
1.2 Issues of SiC fast switching

As demonstrated above, SiC devices have much lower conduction and switching losses compared with Si devices. To benefit from this supreme property, SiC devices are made to switch much faster than Si devices, which not only reduce the volume, size and weight of the passive components, but also improve the system efficiency with less overall cost.

However, many commercial SiC products are in either TO-247, TO-220 package or half-bridge module, full-bridge module. These packages introduce external resistance and stray inductance to the device, for example, the aluminum leads. These parasitic will, in high frequency switching, e.g., >MHz, generate large voltage overshoot or undershoot and voltage and current ringing because of its high dV/dt and dI/dt, which will lead to power loss. What is worse is that in TO-247 and TO-220 package, large common source stray inductance, lead #7 shown in Figure 5, can sometimes cause false turn-on, destroying the device in less than a second, causing reliability issue to the whole system.
Figure 5 DMOSFET structure and TO-247 package with inner view[6][7][8]

6~15nH
1.3 Analysis and Simulation: Discrete V.S. Co-package

The spice model of CREE SiC MOSFET is implemented in the simulation. According to the spice models of TO-247 and bare die device, detailed parameters are given, shown below in Table 2. It includes active device and parasitic device capacitance, as well as the 4.6Ω internal gate resistor $R_{g,int}$. Especially, the stray inductances of TO-247 package, namely $L_g$, $L_d$, and $L_s$ are much larger than those of the bare die, whereas there is almost no stray inductance in bare die devices. Influences of these stray inductances are simulated and analyzed. The external gate resistor $R_{g,ext}$ ($R_g$ in simulation) between the driver and power device, which is another factor that slower the switching speed, is also simulated.

<table>
<thead>
<tr>
<th>Device terminals</th>
<th>Device parameters</th>
<th>Discrete TO-247</th>
<th>Bare die</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate</td>
<td>$L_g$</td>
<td>15nH</td>
<td>1fH</td>
</tr>
<tr>
<td>Drain</td>
<td>$L_d$</td>
<td>6nH</td>
<td>1fH</td>
</tr>
<tr>
<td>Source</td>
<td>$L_s$</td>
<td>9nH</td>
<td>1fH</td>
</tr>
</tbody>
</table>

Table 2 Device parameters of TO-247 and bare die SiC MOSFET\cite{9}
Figure 6 Simulation Schematics

Gate signal is switching between -5V and 20V. SiC MOSFET is switching under 800V and 20A. The variable values in the simulation are shown in the table below. As from the CREE library, stray inductances vary from 6nH~15nH, thus 0~20nH are chosen in the simulation study the influence of stray inductances, particularly in case of discrete devices to the circuit performance.
Table 3 Variable values in the simulation

<table>
<thead>
<tr>
<th>Terminals</th>
<th>Parameters</th>
<th>Parameter name</th>
<th>Simulation value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate</td>
<td>$R_g$</td>
<td>External gate resistance</td>
<td>0, 5, 10, 15, 20</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td>$L_g$</td>
<td>Gate stray inductance</td>
<td>0, 5, 10, 15, 20</td>
<td>nH</td>
</tr>
<tr>
<td>Drain</td>
<td>$L_{dl}$</td>
<td>Drain inductance</td>
<td>0, 5, 10, 15, 20</td>
<td>nH</td>
</tr>
<tr>
<td>Source</td>
<td>$L_s$</td>
<td>Common source stray inductance</td>
<td>0, 5, 10, 15, 20</td>
<td>nH</td>
</tr>
</tbody>
</table>

Simulation results are shown below. $R_g$ is selected to be 0, 5, 10, 15, and 20 $\Omega$; and stray inductances are selected to be 0, 5, 10, 15, 20 nH. Turn-on and turn-off losses are calculated. $E_{on}$ and $E_{off}$ losses in Figure 7 (zero parasitic inductance) represent the minimum dynamic losses that can be achieved in the simulated MOSFET for a given $R_g$. It is important to stress that $R_g=0$ represent zero external gate resistance while a $R_{g,int}=4.6$ $\Omega$ still exists in the simulated device model. The loss result plotted has correctly subtracted $E_{oss}$ (30uJ at 800V) from the $E_{off}$ data and added $E_{oss}$ to the $E_{on}$ data \cite{10}\cite{11}. 
Figure 7 Switching waveforms and switching losses under different external $R_g$
It can be seen that increasing $R_g$ will slow the $V_{gs}$ and $I_g$ transient in both turn-on and turn-off. It results in slower $V_{ds}$ and $I_d$ transient. Both turn-on and turn-off losses increase with increasing $R_g$. The total switching loss increases by 1.5X comparing $R_g=0$ and 20Ω. It can be observed that $E_{off}$ under zero external $R_g$ is 10uJ. From above, it is concluded that zero external $R_g$ is desired to reduce switching losses. Also it is important to notice that $E_{off}$ is much lower than $E_{on}$ and this is related to the dynamic switching process in turn-on and turn-off \[10\]. At very low $R_g$ and low load current ($I_{Load} < I_{critical}$), the $E_{off}$ can actually be close to zero, enabling SiC MOSFET to reach zero turn-off energy operation.

**Figure 8** Switching waveforms under different $L_g$
In terms of $L_g$, as shown in Figure 8, increasing $L_g$ will slower $V_{gs}$ and $I_g$ transient and cause overshoot in $V_{gs}$. When $L_g=20\text{nH}$, it will cause $V_{gs}$ overshoot to 23.4V and undershoot to -9.9V, approaching the recommended $V_{gs}$ margin for the device, which is between -10V to 25V. It also results in slower $V_{ds}$ and $I_d$ transient, especially under turn-off. Its impact on losses is minimum, thus is not plotted in the figure. From above, it is concluded that larger $L_g$ is not desired.

For $L_d$, increasing $L_d$ results in voltage undershoot of $V_{ds}$ and delay of $I_d$ transient during turn-on, and causes large overshoot and ringing during turn-off. When $L_d=20\text{nH}$, it will cause $V_{ds}$ overshoot of more than 200V during turn-off. It will exceed the device rating if higher DC voltage is used. It will also generate other losses in ESR of inductors and capacitors in the circuit due to large ringing, thus larger $L_d$ is not desired.

![Switching waveforms under different $L_d$](image)

**Figure 9 Switching waveforms under different $L_d$**
In terms of common $L_s$, increasing $L_s$ results in delay of $V_{ds}$ and $I_d$ transient. It can be seen that both turn-on and turn-off losses increase with the increasing of the common $L_s$. The total switching loss increases by 3.5X comparing $L_s=0$ and 20nH. It is concluded that zero common $L_s$ is needed. It can be achieved by Kelvin connection, which allows an external
driver device to cleanly driver the intrinsic source free of the inductive \( L \times \text{di/dt} \) noise generated by the high current fluctuations of the source lead \(^{12}\).

As a conclusion from these simulations, external \( R_g \) and common \( L_s \) need to be zero to achieve fast switching speed; \( L_g \) and \( L_d \) need to be minimized in order to reduce \( V_{gs} \) and \( V_{ds} \) oscillations and EMI noise. Thus bare die is used with Kelvin connection. By using bare die devices, power loop can also be minimized, resulting in reduced drain stray inductance. By co-package together with the gate driver, external gate resistance and gate stray inductance can be greatly minimized.


1.4 Thesis Organization

The thesis is organized with the order of design, fabrication and test of the co-packaged power module.

Chapter 2 shows the design of the module. Layout optimization is included. Optimized components and materials are selected according to the application demand.

Chapter 3 shows the details of the module fabrication. It is a fabrication method which is developed and applied to the co-packaged module and many other power modules in FREEDM Systems Center. Materials, tools, and methods are illustrated step by step.

Chapter 4 demonstrates the testing results of the co-packaged module. It includes static and dynamic test of module. The half-bridge module is also tested in continuous operation under 500 kHz, 800V, 10A with ZVS turn on.

Conclusion and Future works are stated in the last two chapters.
CHAPTER 2 DESIGN OF THE CO-PACKAGED MODULE

2.1 Power Electronics Packaging

A commonly used stack of power semiconductor module is shown in Figure 11. Direct Bonded Copper (DBC), also called Direct Copper Bonded (DCB), is chosen as the substrate for mounting chip dies on. DBC consists of two copper layers and one ceramic layer between them. Chip die is soldered on one copper layer of the DBC. Bond wires connect copper layer and chip die to form circuit loop. DBC is soldered on baseplate, which will be attached on heat sink using thermal grease. A top view of SEMIKRON module is shown in Figure 12.

![Stack overview of a power semiconductor module](image)

*Figure 11 Stack overview of a power semiconductor module* [13]
Some other advanced power electronics module includes copper deposition, 3D packaging, SKiN technology, and sinter process. Copper deposition forms a copper layer on bare die devices. Copper wire bonds are connected between DBC copper layer and chips \(^{[15]}\). Thus there is no stress on the wire joints, which leads to reduced thermal stress of the bonds and
longer lifetime of the module, shown in Figure. 3D packaging \cite{16} is bondless packaging process after copper deposition. Pads of bare die devices are soldered together so there is no wire bond in the module. It can achieve high power density by double-sided cooling.

Figure 14 SKiN and sinter technology of SEMIKRON \cite{17}

Sinter technology uses certain heat and pressure to attach bare die devices on DBC layout. There is no solder layer between device and DBC, thus much less stress than solder, which increases the lifetime of the module. Also there is much less thermal resistance than soldering devices on DBC, which increases the power density by about 35%. SKiN technology also uses the sintering process, which connects the device pads, that allows 25% larger surge current to flow and longer lifetime of the module.
Figure 15 Performance overview of different substrate materials \[18\]

Substrate is the first thing taken into consideration as they are the foundation of power modules. Performance overview of different substrate materials is shown in Figure 15. Comparing with conventional PCB substrate, DBC Al$_2$O$_3$ performs much better ampacity and thermal conductivity, which means it can carry more current thus more power and cool the module faster. It can also provide high voltage insulation. AlN, AMB Si$_3$N$_4$, and DBC HPS perform better than DBC Al$_2$O$_3$ in either ampacity or thermal conductivity. However, due to their higher cost, shown in Table 4, DBC Al$_2$O$_3$ is chosen here for the co-packaged power module development.
Table 4 Price comparison of different substrates \cite{19}

<table>
<thead>
<tr>
<th>Substrate materials</th>
<th>Price (USD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃ Substrate 5.4&quot; × 7.5&quot; × .015&quot;</td>
<td>40</td>
</tr>
<tr>
<td>DBC Cu .005&quot; Both Sides</td>
<td></td>
</tr>
<tr>
<td>AlN Substrate 5.4&quot; × 7.5&quot; × .015&quot;</td>
<td>100</td>
</tr>
<tr>
<td>DBC Cu .005&quot; Both Sides</td>
<td></td>
</tr>
<tr>
<td>AMB Si₃N₄ Substrate 5.4&quot; × 7.5&quot; × .015&quot;</td>
<td>120</td>
</tr>
<tr>
<td>DBC Cu .005&quot; Both Sides</td>
<td></td>
</tr>
<tr>
<td>HPS Substrate 5.4&quot; × 7.5&quot; × .015&quot;</td>
<td>60</td>
</tr>
<tr>
<td>DBC Cu .005&quot; Both Sides</td>
<td></td>
</tr>
</tbody>
</table>

Figure 16 shows a conventional component layout of power electronics system. The gate driver, which is mounted on the gate driver board, is far from the SiC module, leading to large external gate resistance and gate driver loop inductance.

![Figure 16 Conventional component layout of power electronics system \cite{20}](image-url)
To minimize the influence of the large external gate resistance and gate driver loop inductance, the CREE 1200V 31.6A SiC MOSFET (CPM212000080B) is integrated with Texas Instruments gate driver UCC 27531, shown in Figure 17, into one power module which reduces the gate loop of the MOSFETs as well as the power loop.

**Figure 17 CREE 1200V SiC MOSFET (left), TI driver UCC27531 (right)**
2.2 DBC Layout Design

There are design rules of DBC layouts.

<table>
<thead>
<tr>
<th>Minimum width of Copper lines</th>
<th>Min. Width</th>
<th>Copper Thickness</th>
<th>Minimum Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical .012&quot;</td>
<td>@≤.005&quot;</td>
<td>.024&quot;</td>
<td></td>
</tr>
<tr>
<td>Minimum .010&quot;</td>
<td>@≤.005&quot;</td>
<td>.020&quot;</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Minimum width of spaces</th>
<th>Min. Width</th>
<th>Copper Thickness</th>
<th>Minimum Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical .020&quot;</td>
<td>@≤.008&quot;</td>
<td>.040&quot;</td>
<td></td>
</tr>
<tr>
<td>Minimum .0160&quot;</td>
<td>@≤.008&quot;</td>
<td>.032&quot;</td>
<td></td>
</tr>
</tbody>
</table>

Tighter tolerance are possible but not guaranteed in volume production

<table>
<thead>
<tr>
<th></th>
<th>Min. Width</th>
<th>Copper Thickness</th>
<th>Minimum Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical .0275&quot;</td>
<td>@≤.010&quot;</td>
<td>.056&quot;</td>
<td></td>
</tr>
<tr>
<td>Minimum .020&quot;</td>
<td>@≤.010&quot;</td>
<td>.040&quot;</td>
<td></td>
</tr>
</tbody>
</table>

Design of the co-packaged power module is based on the Design Rules above. Top layout of the Gen-1 and Gen-2 co-packaged module is shown below. To verify the advantage of co-packaged module over TO-247 based settings, a half-bridge using same gate driver is carefully designed to have power loop and gate loop as small as possible.
Figure 18 Gen-1 co-packaged module ($R_{g,ext} = 2\Omega$)

Figure 19 Gen-2 co-packaged module ($R_{g,ext} = 0$)
Figure 20 TO-247 based settings (R_{g,ext} = 0\Omega)
Estimated loop comparison of gate loop and power loop are shown in Figure 21.

**Figure 21 Loop area comparison of TO-247 based half-bridge, co-packaged module Gen-1 and Gen-2** \(^{[\text{11}]}\)

In TO-247 based setup, due to the large size of the package, power loop is pretty large, approximately 200 mm\(^2\), and the gate loop is about 100 mm\(^2\).

In Gen-1, the power loop is 132 mm\(^2\), and there are 2Ω gate resistors for both turn-on and turn-off. Signal terminals are the same type with power terminals. The large SW area can cause abnormal turn-on during switching sometimes when the driver circuit is not strong enough to support a positive signal on the IN terminal of the gate driver, shown in Figure 22. During turn-on, drain current starts to flow through the device after \(V_{gs}\) increases to \(V_{th}\), charging the device parasitic capacitance \(C_{gs}\). Then \(V_{ds}\) drops when \(C_{gd}\) is being charged, and shrinks the current from the input node of the driver through coupling of ceramic capacitors.
underneath the SW pad and the input signal pad, pulls down the input signal and causes ‘abnormal’ turn-off.

**Figure 22 Influence of ceramic parasitic capacitance** [11]

Gen-2 module shrinks the power loop area to 42mm², with more clearance distance between VDC+, VDC- and SW power terminals, which guarantee more safety during operation. Layout is symmetric along the diagonal line and SiC MOSFETs are put in the middle so that the majority of heat are generated here, which enables more efficient heat transfer. Smaller pins are used for the signal terminals to reduce cost. Terminals are also aligned much better than Gen-1 to facilitate assembly with PCB board.
2.3 Stack Design of Module-based Converter

![Stack design module-based converter](image)

**Figure 23** Stack design module-based converter

![Temperature profile and physical structure](image)

**Figure 24** (a) Temperature profile of a layer structure with heat spreading; (b) physical structure[^22]
From the temperature profile, it could be seen that the thermal interface material (TIM) is where the major thermal resistance comes. For a module with heat sink, the majority of thermal resistance results from the TIM and the heat sink. It also contains a large portion of thermal resistance of DBC ceramic layer. In the stack design, a combination of heat sink and fan which has very low thermal resistance about 1˚C/W is chosen for the converter buildup.

The final version of top view of the co-packaged module is shown below. Top and side view of all layers and SolidWorks 3D view are shown in Figure 25-27.

![Figure 25 Top view of designed stack](image)
The components are soldered on top copper layer of DBC, while the bottom copper layer of DBC is soldered on the copper baseplate (1 mm thick). The baseplate is then screwed tightly on the heatsink with thermal grease between.

Figure 26 Side view of designed stack

Figure 27 3D view of designed stack (not showing the wire bond, screw hole and fan)
CHAPTER 3 FABRICATION OF THE CO-PACKAGED MODULE

The fabrication process of the co-packaged power module is divided into two parts: DBC patterning process and DBC module process.

3.1 DBC Pattern Processing

DBC pattern processing is transferred from PCB processing technology, shown in Figure 28.

![Figure 28 PCB processing technology](image-url)
PCB Editor is used to design and draw the layout, shown in Figure 29. The layout mask is printed on transparency film using monochrome mode, two films are attached together to enhance the contrast (one film is too thin to tell the difference), which will benefit the following step. It is critical in this step to avoid the static electricity on the transparency film when printing, which will result in a vague layout of poor solution.

![Figure 29 Layout drawing in PCB Editor (left) and printed mask of DBC layout (right)](image)

The blue paint film consists of three layers: one paint layer is between two plastic layers. One of the plastic layers is peeled off and attached to both sides of the DBC using a heated laminator. After the paint film is attached firmly to both sides of the DBC, it is put into the UV oven covered by the printed masks. An optimal setting of the UV oven is 50% light density for 4 seconds. Figure 30 shows the top view of the DBC after the UV process. Areas covered by black mask remain previous color, while areas covered by transparent mask turn to dark blue.
Figure 30 UV oven (left); DBC after UV exposure (right)

The remained plastic layer is pill off after the UV exposure and the whole DBC is immersed into Na$_2$CO$_3$ solution. Figure 31 shows the top view of the DBC after the develop process. Areas of dark blue stay the same. Blue paint on other areas are wiped out by the developer, so that the copper layer is exposed. The arrow shows copper exposed though it is not very clear in the figure. The exposed copper is supposed to be etched in the next step.

Figure 31 Developer powder (left); DBC copper are exposed after developing process (right)

After the develop process, the DBC is put into the etching tank. As a result, the exposed copper areas are etched away. The etch powder used here is Na$_2$S$_2$O$_8$. The reaction is: Cu + Na$_2$S$_2$O$_8$ → CuSO$_4$ + Na$_2$SO$_4$. Figure shows the DBC after the etching process. It achieves a
minimum width of 0.2mm and minimum spacing of 0.1mm on copper trace, which guarantees very high density integration of the gate driver.

![Figure 32 Etching tank (left); DBC after etching process (right)](image)

Auto-strip follows the etching process. NaOH powder is used here to remove the remaining blue paint on the DBC. Figure 33 shows the DBC after the auto-strip process.

![Figure 33 Auto-strip powder (left); DBC after auto-strip process (right)](image)

The above steps demonstrate the DBC patterning process. Fabrication of module using the patterned DBC is illustrated below.
3.2 DBC Module Processing

Before the module processing, it is recommended to wash the DBC using Hydrochloric Acid, to remove the oxidized copper during pattern process and storage. Bare dies soldered using Sn20/Au80 with melting point of 280°C. Hot plate is heated up to 300°C, which melts the solder paste, and attaches the bare dies on the DBC copper. Figure 34 shows the DBC with bare dies after the process. 12 mil aluminum wires are bonded between pads of bare dies and copper traces using Hesse bonding machine. Figure 34 shows the DBC with wire bonds.

Figure 34 DBC with soldered bare dies (left); DBC with bonded bare dies (right)

Then, other components, e.g. power pins, signal pins, drivers, and capacitors are soldered on the DBC with the same process as bare dies except that a different solder paste Sn63/Pb37 is used, which has a lower melting temperature 183°C. Hot plate is heated up to 200°C, which melts the solder paste, and attaches the components on the DBC copper. This ensures the previous solder paste Sn20/Au80 used for bare dies doesn’t melt in this step. Figure 35 shows the DBC after placing and soldering all other components. Due to small area of the module, wire bonder machine can hardly reach and bond the supposed pads without influencing other components, solder paste of different melting point is used to facilitate the manufacturing
process. The DBC is soldered onto the nickel plated copper baseplate at the same time using solder paste Sn63/Pb37. Size of the copper baseplate is a 45mm×45mm×1mm, shown in Figure 36 as well as the baseplate after nickel plated.

Figure 35 DBC with all components placed (left), DBC with all components soldered (right)

Figure 36 Copper baseplate (left), copper baseplate with electrolytic Ni plated (right)

Followed by soldering all components, a 3D printed case is attached and glued to the DBC to provide a barrier for the silicone gel ( SEMICOSIL®915HT ), which is encapsulated into the case to provide mechanical strength of the wire bonds and high voltage insulation within the module. It cures about 8 hours in room temperature. Figure 37 shows the overall module after housing and encapsulation. Red rectangle shows the power loop of the half bridge, and
yellow circles show the power terminals of the module. Two packs of 6 signal pins are on each side.

Figure 37 Co-packaged module (Gen-2)

According to the module stack design, overview and side view of the module with baseplate, heat sink and fan is shown below. Fan is blowing air up towards the heatsink.

Figure 38 Overview and side view of the module with baseplate, heat sink and fan
CHAPTER 4 TEST OF THE CO-PACKAGED MODULE

4.1 Static Test of the Power Module

After the packaging process, static reverse blocking and forward conduction characteristics of the MOSFET as well as the characteristics of the body diode are tested under room temperature on the M370 curve tracer, shown in Figure 39 to make sure that the packaging process does not degrade or destroy the characteristics of the bare dies. Leakage current of the MOSFET under 1200V is 46.5uA.

Figure 39 Static reverse (left) and forward (right) characteristics of the SiC MOSFET after co-package under RT
4.2 Dynamic Test of the Power Module

4.2.1 Double Pulse Test

Double pulse test (DPT) was conducted on both low-side device for TO-247 based setup, Gen-1 module and Gen-2 module. Figure 41-42 show the DPT test topology, test settings, and test results of the bottom MOSFET under 800V, 10A. Because there is very small area to locate a current sensor in the module, the inductor current $I_L$ is measured instead of the device current $I_D$. Other measurements include $V_{GS}$ and $V_{DS}$.

![Figure 40 DPT topology and measurements of bottom MOSFET of the module][11]
Detailed turn-on and turn-off waveforms of bottom MOSFET is shown in Figure 42 below. Red line is $V_g$ and blue line is $V_{ds}$. Device current for TO-247 setup and inductor current for co-packaged module are shown in green.

In terms of TO-247 based setup, there is large ringing and ~30V $V_{ds}$ overshoot caused by large $L_d$ and ~3V $V_{gs}$ undershoot caused by common $L_s$. Gen-1 has larger undershoot in $V_{ds}$ and ‘abnormal’ turn-off during turn-on due to the parasitic capacitance of the large SW pad. Less overshoot in $V_{ds}$ when turn-off is observed due to minimized $L_d$. For Gen-2, it shows smooth switching transient due to minimized SW pad and minimized power loop and gate
loop. No undershoot in $V_{ds}$ when turn-on and no overshoot and ringing in $V_{ds}$ when turn-off indicates optimally reduced $L_d$; smooth $V_{gs}$ transient indicates optimally reduced $L_g$ and $L_s$.

Both TO-247 and Gen-2 are using $R_{g,ext} = 0$ thus has same switching speed, while $R_{g,ext} = 2\Omega$ is used in Gen-1. So Gen-1 is showing slower $dV_{ds}/dt$, shown in Table 6.

<table>
<thead>
<tr>
<th>dV_{ds}/dt</th>
<th>Turn-on</th>
<th>Turn-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen-1</td>
<td>60kV/us</td>
<td>30kV/us</td>
</tr>
<tr>
<td>Gen-2</td>
<td>96kV/us</td>
<td>39kV/us</td>
</tr>
</tbody>
</table>

Table 6 $dV_{ds}/dt$ comparison of Gen-1 and Gen-2 $^{[11]}$
Figure 42 Switching waveforms of bottom MOSFET under 800V, 10A under RT \cite{11}
4.2.2 Continuous Test

A half bridge based reactive power converter is built to evaluate losses and efficiency. The circuit topology is shown in Figure 43. The co-packaged module is shown in the yellow dashed line.

![Topology of application circuit](image)

**Figure 43 Topology of application circuit**

The assembly order is illustrated in Figure 44. The module is attached on the power PCB board by soldering the signal and power pins. Signal pins are also soldered on the driver PCB board. Side view of the whole system is shown in Figure 45.
Figure 44 Circuit assembly of the converter using co-packaged module
According to the converter stack design, side view of the converter is shown below.

**Figure 45 Side view of the converter** [11]

**Table 7 Continuous test conditions**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DC}$ (DC input voltage)</td>
<td>800 V</td>
</tr>
<tr>
<td>$I_{pk-pk}$ (inductor current)</td>
<td>46 A</td>
</tr>
<tr>
<td>$f_{SW}$ (switching frequency)</td>
<td>510 kHz</td>
</tr>
<tr>
<td>Turn on</td>
<td>Turn off</td>
</tr>
<tr>
<td>$dV/dt$</td>
<td>80 V/ns</td>
</tr>
<tr>
<td></td>
<td>60 V/ns</td>
</tr>
</tbody>
</table>
Figure 46 Continuous 510 kHz test results of the integrated module (Measurement on low side MOSFET) [11]
Switching waveforms of the continuous test at 510 kHz are shown in Figure 16. $V_{gs}$ is in yellow, $V_{ds}$ is in blue. Pink line is the input DC voltage. It can be seen that the integrated module can operate at high frequency under high voltage and high current switching condition with close to zero ringing. Detailed switching waveforms show fast and smooth switching transient is achieved by the integrated module with 80kV/us when turn-on and 60kV/us when turn-off. The noise free operation enables the devices switching at even higher switching frequency [24].

4.2.3 Thermal Evaluation and Loss Comparison

To estimate its turn-off loss, thermal distribution is tested first. A DC current is injected through the body diode of SiC MOSFET and generate heat. Thermal camera is used to read temperature on the bare die and heatsink, shown in Figure 47. Gate driver is not functioning in this calibration. So the heat is generated from only from the MOSFET. DC current and voltage between the terminals are measured and calculated for power loss.

![Figure 47 Thermal calibration setup](image-url)
Figure 48 shows the calibration relationship of power loss and junction temperature of SiC MOSFET $T_{\text{die}}$ and heatsink temperature $T_{\text{hs}}$. Both TO-247 setup and co-packaged module are tested under 800V, 10A switching. TO-247 is under DPT, and co-packaged module is under 510 kHz continuous operation with ZVS turn-on. As shown in Chapter 1, $E_{\text{off}}$ and $R_{\text{ds,on}}$ of SiC MOSFET increases with increasing temperature, thus the co-packaged module is in worse condition due to higher junction temperature resulted from the continuous operation.

For TO-247 setup,

$$\text{Turn-off loss} = \int V_{\text{ds}} \times I_d - E_{\text{oss}} \, (\sim 30\text{uJ})^{[10]}$$

For co-packaged module,

$$\text{Turn-off loss} = P_{\text{total}} - P_{\text{deadtime}} - P_{\text{conduction}}^{[24]}$$
Turn-off loss is compared in Figure 49. Even at higher junction temperature, the co-packaged module is showing much less turn-off energy loss with a reduction of 31.7uJ than that of the TO-247 setup under room temperature. Under certain condition [10], turn-off energy loss can be reduced to zero to realize lossless switching operation.

Figure 49 $E_{off}$ comparison of TO-247 and co-packaged module
CHAPTER 5 Conclusions

A SiC MOSFET-gate driver co-packaged power module is designed, fabricated and tested. Compared with discrete TO-247 packaged SiC MOSFET of same ratings, it has minimized drain stray inductance and gate stray inductance, no common source stray inductance and zero external gate resistance. Comparisons are made between TO-247 and co-package under double pulse test of 800V, 10A and zero external gate resistance. The co-packaged module results in smoother transient compared to TO-247. Continuous test of 510 kHz, 800V, 46A_{pk-pk} with zero-voltage-switching (ZVS) turn on is conducted. Turn-off loss comparison between TO-247 and co-packaged module is conducted under 800V, 10A. It is observed that the co-packaged module results in 10.3uJ turn-off loss, much less than 41.9uJ in the TO-247 package even the co-packaged module is operating at higher temperature. The noise-free operation can enable >MHz operation with low losses with the lossless switching concept of SiC MOSFET.
CHAPTER 6 Future Works

1. Reliability improvement of the co-packaged module.

Reliability is one concern of the power module. [25] lists several weak points which may lead to system failure, shown in Figure 50. The co-packaged module needs to be further studied according to the listed failure mechanism.

Figure 50 Weak points in packaging technologies to be addressed [25]

2. Multichip module.

Figure 51 Toyota Prius inverter IGBT module [26]
When the demand of current rating or voltage rating of power module increases, one option is to design and fabricate HV module. Another option is put devices in parallel or series. The co-packaged module can be developed further to meet these demands.

3. Double-sided cooling.
In one side cooling, heat-blocking silicone gel is used so that heat can be dissipated in only one direction from the junction to ambient. With double side cooling, heat can be dissipated in two directions from junction to ambient, resulting in higher temperature the device can hold and more power the device can carry within its rating. Possible solutions for double side cooling can be using heat-conductive silicone gel with high voltage isolation or stack package.

![Figure 52 One-sided cooling and double-sided cooling](image)

4. Online diagnosis and protection
NTC resistors and sensors can be packaged in the module to better diagnose and protect the module. Several parameters of the device, such as junction temperature, current, voltage, etc can be measured. This will improve the reliability of the module.
REFERENCES


[5] CREE: Demonstration of SiC MOSFET.
http://www.cree.com/~media/Files/Cree/Power/Articles%20and%20Papers/Power_Article_1.pdf

http://www.globalspec.com/learnmore/semiconductors/discrete/transistors/power_mosfet

[7] CREE 1200V SiC MOSFET C2M0080120D.


[10] Xuan Li; Liqi Zhang; Suxuan Guo; Yang Lei; Alex Q. Huang, Bo Zhang. Understanding Switching Losses in SiC MOSFET: Toward Lossless Switching. 3rd IEEE Workshop on Wide Bandgap Power Device and Application (WIPDA 2015).

[11] Liqi Zhang, Suxuan Guo, Xuan Li, Yang Lei, Wensong Yu, Alex Q. Huang. Integrated SiC MOSFET Module With Ultra Low Parasitic Inductance for Noise Free Ultra High Speed
Switching. 3rd IEEE Workshop on Wide Bandgap Power Device and Application (WIPDA 2015).


[13] Failure mechanisms during power cycling, January 2013, Powerguru


[18] Rogers curamik. DBC substrate property comparison.

[19] Rogers curamik. DBC substrate price comparison (courtesy from Rogers).

[20] Chen, Zheng. Wang, Ruxi ; Yao, Yijing ; Danilovic, Milisav ; Zhang, Wenli ; DiMarino, Christina ; Boroyevich, Dushan ; Burgos, Rolando ; Ngo, Khai ; Rajashekar, Kaushik A 50kW SiC Three-phase AC-DC Converter Design for High Temperature Operation. PCIM Europe 2015.


[22] SEMIKRON. Power Semiconductors Application Note.


[25] Suxuan Guo, Liqi Zhang, Yang Lei, Xuan Li, Wensong Yu, Alex Q. Huang. 3.38 Mhz Operation of 1.2kV SiC MOSFET With Integrated Ultra-Fast Gate Drive. 3rd IEEE Workshop on Wide Bandgap Power Device and Application (WIPDA 2015).
