## ABSTRACT

REZAEI, MOHAMMAD ALI. Design, Implementation and Control of A High Efficiency Interleaved Flyback Micro-Inverter for Photovoltaic Applications. (Under supervision of Dr. Alex Q. Huang)

Photovoltaic (PV) micro inverters have been gaining attention for the grid-connected PV systems because of improved energy harvest, friendly "Plug-N-Play" operation, and enhanced modularity and flexibility. Various inverter topologies for PV micro-inverters applications have been introduced in the literature that perform the maximum power point tracking (MPPT) of PV module, high step-up voltage amplification, output current shaping, and galvanic isolation. Among them, the flyback based micro-inverter is one of the most attractive solutions due to its simple structure and control and also its inherent galvanic isolation.

The conventional flyback micro-inverter consists of decoupling capacitor, interleaved flyback converter, unfolding bridge, and CL filter. The unfolding bridge is switched at line frequency by a simple square-wave control, generating a rectified sinusoidal waveform at the dc-link between the interleaved flyback converter and unfolding bridge. The decoupling capacitor maintains the power balance between the constant input power and variable output power oscillating at double-line-frequency. All the other functionalities required in PV micro-inverter are performed by the flyback converter. Therefore, the flyback converter has been widely scrutinized to improve its performance in terms of efficiency, reliability, and cost.

The aim of this thesis is to develop a new control and clamping mechanism in order to increase the efficiency of the flyback micro-inverter at the lowest possible cost. To achieve that goal, a hybrid switching strategy is adopted for the inverter. The adopted switching

strategy controls the inverter in the Boundary Conduction Mode (BCM) in order to exploit the natural resonance of the flyback transformer to achieve Zero Voltage Switching (ZVS) during the turn-on process. At low load and near the zero-crossing of the grid voltage, the switching frequency of the inverter is then limited by transitioning to Discontinuous Conduction Mode (DCM) to limit the switching loss. Although this hybrid switching strategy ensures the ZCS turn-on for every switching cycle and ZVS turn-on for most of the grid cycle, it does not provide any mechanism to limit the turn-off switching loss, which is the major source of loss in the flyback converter.

In order to limit the turn-off switching loss, a novel adaptive snubber is developed in this thesis which ensures soft switching during the turn-off process. The developed adaptive snubber requires the minimum number of components and operates only at double-line frequency, which makes the control system easy and straight forward. Using the proposed adaptive snubber technology, a maximum efficiency of 96% is achieved.

Based on the proposed adaptive snubber with the associated hybrid switching method, the operation of the inverter is then further optimized in order to achieve the maximum CEC efficiency. The presented efficiency optimization procedure accurately takes into account the transformer and switching losses of the inverter and optimizes the parameters of the hardware and controller. The optimized hardware achieves the CEC efficiency of 94.96%, which is on-par with the available commercial products

# Design, Implementation and Control of A High Efficiency Interleaved Flyback Micro-Inverter for Photovoltaic Applications.

by

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## DEDICATION

To my wife:

Dr. Maedeh Heidarpourroushan

And to my parents and parents-in-law.

## BIOGRAPHY

Mohammad Ali Rezaei was born in Esfahan, Iran. He received his B.Sc. and M.Sc. degrees in electrical engineering from University of Tehran, Tehran, Iran in 2008 and 2011 respectively. In fall 2011, he joined the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center of North Carolina State University, Raleigh, to pursue his Ph.D. degree. His main research interests is in the area of power electronics including: digital control of power converters, high frequency DC-DC converters, application of GaN and SiC devices in power electronics and power electronics for renewable energy applications.

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# 1. Introduction and Background

## 1.1 Introduction

This chapter is an introduction on the Photovoltaic (PV) renewable energy systems. We explain different parts of such systems and demonstrate why the "PV inverter" is one of their most important parts. At the end of this chapter, we should be able to answer the following important questions regarding the PV energy and PV inverter systems:

- Why PV energy is important in the world of fossil fuels and nuclear energy?
- What are the different types of PV inverter systems for residential and commercial applications?
- Why PV micro-inverter is an interesting solution for residential applications?
- What is the aim of the current research work?
- What is the impact of presented research work on the PV systems?

### 1.1.1 Background and motivation

The increasing concerns about the fossil fuel reserves and the environmental issues of burning them have led the renewable energies to become the perspective of the power generation. As the increasing power demand restricts the planning and installation of large centralized power units, distributed renewable energy generation units are increasingly used to produce green electricity.

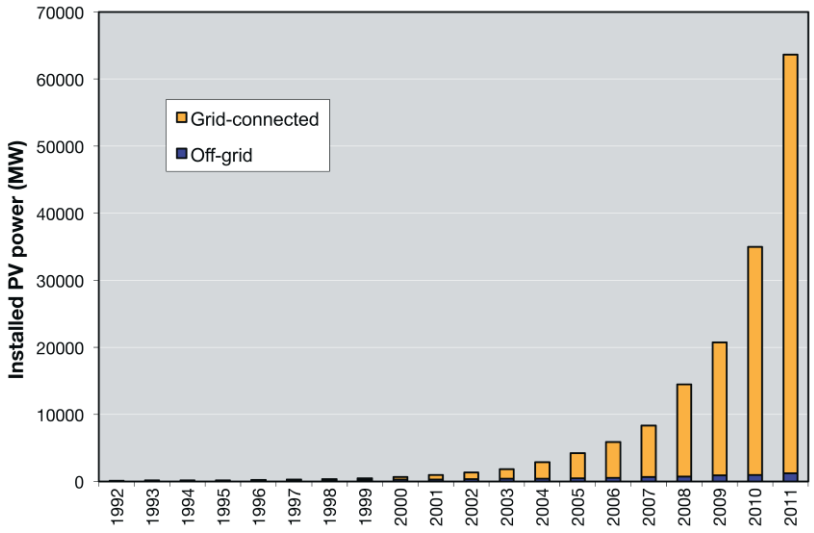


**Fig. 1.1: Cumulative installed grid connected and off-grid PV power in reported countries between 1992 and 2011**

Among different types of renewable energy sources, photovoltaic (PV) energy is becoming more and more popular. As it is reported in [1] and illustrated in Fig. 1.1, the cumulative installed grid connected and off-grid PV power in the reported countries has increased from essentially zero, in 1992, to more than 63 GW in 2011. The downward tendency in the price of PV modules due to massive increase in production capacity has played a major role in this increase.

Fig. 1.2 illustrates the cost of PV modules over the year span of 1976 to 2009 in comparison with the cost onshore wind farms. The gradual decrease in the cost of PV modules is visible in this figure whereas the cost of wind farms has stayed almost the same during this period.

In addition to reduced price, the durability of PV modules is an important factor in popularity of PV energy. A PV module does not contain any moving parts, as opposed to

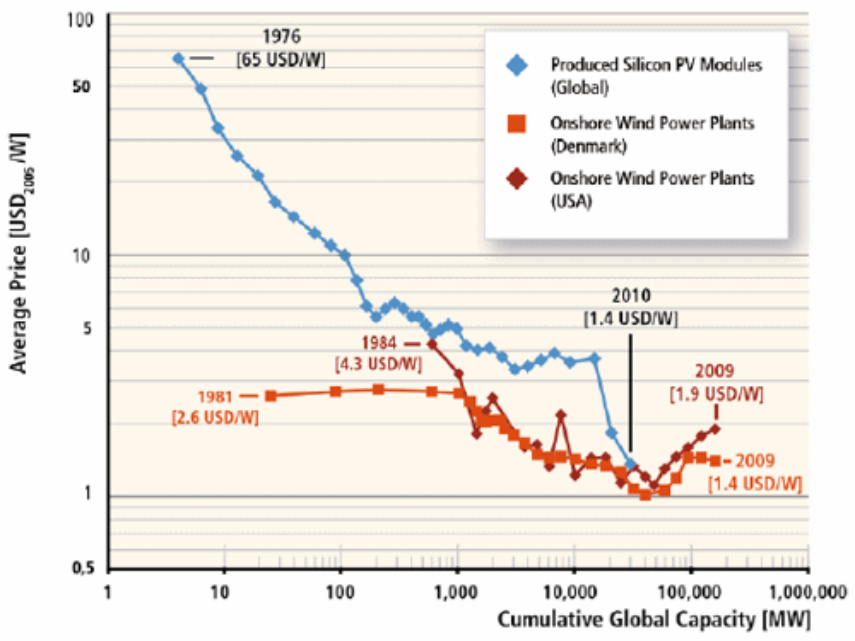


**Fig. 1.2: Average cost of silicon PV modules from 1976 to 2009 in comparison with average price of onshore wind farms.**

some of the other renewable energy sources such as wind. A long lifetime is therefore guaranteed, without almost any tear-and-wear and maintenance. For example, Isofoton offers a 10 year warranty on products and 30 years linear output power warranty [2].

As the cost of PV module decreases year by year, the cost of inverters is becoming more visible in the total cost of the PV systems. It is worth mentioning that in addition to the cost of inverter itself, installation of the inverter plays a major role in the total cost of the PV system. As a result, special effort has been made in the past decade to reduce the cost of PV inverters. These efforts have been streamlined in two directions, one is changing the system architecture and the other is changing the PV inverter topology. Next section of this thesis introduces different approaches that authors and industries have followed in the past years to

reduce the total cost of the PV inverter system and maintaining a high efficiency at the same time.

### 1.1.2 PV inverters

The power electronic interface that converts the Direct-Current (DC) power generated by PV panel to Alternating-current (AC) power required for grid and loads is called a PV inverter. A PV inverter system has two main tasks:

- To amplify and invert the generated DC power into a suitable AC current [3] or voltage for the grid. A standard PV module generates approximately 100 W to 250 W at a voltage around 23 V to 38 V, whereas the grid mostly requires 120, 230 or 240 volts at 50Hz or 60Hz.
- To ensure that of PV panels work at their maximum power point at different conditions. This functionality is called Maximum Power Point Tracking or MPPT.

Due to changes in the ambient conditions (i.e. changes in irradiance and temperature), PV inverters are required to do these tasks at highest possible efficiency over a wide range of power.

If the PV inverter is interfacing with a single phase grid, its output power fluctuates between zero and twice the average power. The PV module cannot be operated at the MPP if this alternating power is not decoupled by means of an energy buffer, as will be seen later on in chapter 2. However, if the grid is a three phase one, its output power is constant and the requirement for energy buffer is much lower. Finally, the current injected into the grid must

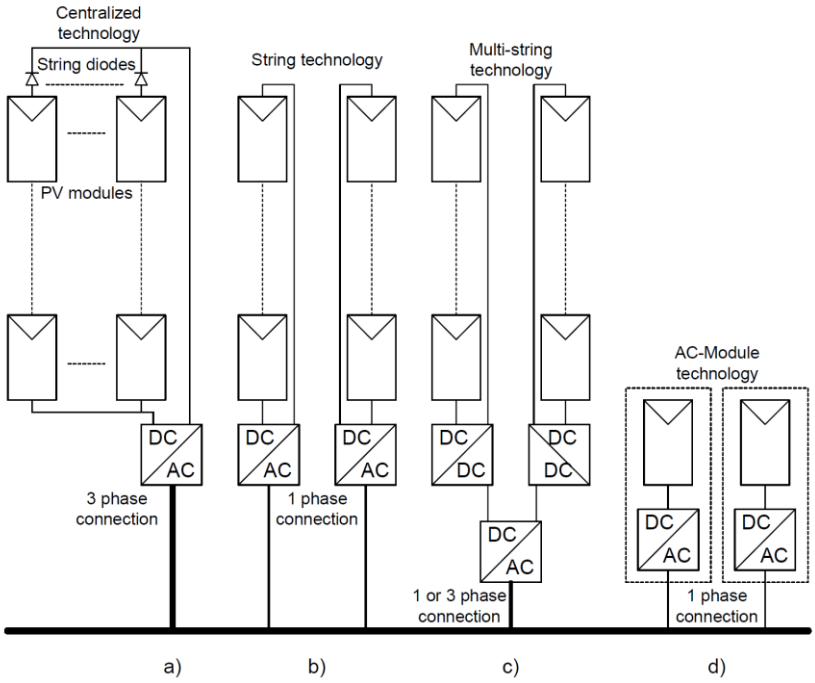


**Fig. 1.3: Photovoltaic system technologies. A) Past centralized technology, b) Present string technology, c) Present multi-string technology, d) Latest AC-Module technology.**

obey the regulations, such as the IEEE std. 1547 [4], which states the maximum allowable amount of injected current harmonics. In addition to these regulations, PV inverter must be able to determine the islanding mode and ground faults which are not allowed due to personnel safety requirement. Table summarizes three standards dealing with the interconnections of PV system and the grid [5].

In the next subsections, the past, present and future technologies for PV inverters are introduced. Since the focus of this work is on residential PV systems, only residential PV inverters are considered.

**Table 1.1: Brief summary of requirements of different standards for grid connected PV systems**

| Issue | IEC61727 | IEEE1547 | EN61000-3-2 |
|---|---|---|---|
| Nominal power | 10kW | 30kW | 3.7kW |
| Current Harmonics | (3-9)4% | (2-10)4% | (3)2.3A |
| | (11-15)2% | (11-16)2% | (5)1.14A |
| | (17-21)1.5% | (17-22)1.5% | (7).77A |
| | (23-33).6% | (>35).3% | (9).4A |
| | | | (11).33A |
| | | | (13).21A |
| | | | (15-39)2.25/h |
| Maximum Current THD | 5% | | - |
| Power Factor at 50% load | .9 | | |
| DC Current Injection | Less than 1.0% of rated current | Less than .5% of rated current | <.22A |
| Voltage Range | 85%-110% (196V-253V) | 88%-110% (97V-121V) | - |
| Frequency Range | 50±1Hz | 59.3Hz – 60.5Hz | - |

#### 1.1.2.1 Residential PV inverters: The Past

The past technology, illustrated in Fig. 1.3(a), was based on centralized inverters. In the centralized inverter technology, a large number of modules are interfaced to the grid using a single inverter [5]. In order to provide the required voltage on the dc bus of the inverter, PV modules are connected in series which is called a “string” of PV modules. A

diode is also connected in series with the PV string to protect it from reverse current. The strings are then connected in parallel in order to provide the required power for the inverter. This string configuration suffers from some disadvantages that make it a bad choice for residential applications. These disadvantages include: high-voltage DC cables between modules which raises some safety concerns and complicates the process of licensing, power loss due to centralized MPPT, mismatch losses between PV modules, losses on string diodes and non-flexible design which makes it hard for mass production [5]. The inverter in this technology was usually a line commutated inverter with a poor power quality. In order to cope with these limitations and also satisfy the current standards, new inverter topologies and systems structures have been invented which is discussed in the next to sub-sections.

#### 1.1.2.2 The Present

The present technologies for the PV inverters are the string inverters, multi-string inverters and also ac-modules [6],[7]. The string inverter, shown in Fig. 1.3(b) is a reduced version of the centralized inverter, where a single string of PV modules is connected to the inverter. The input voltage of the inverter may be enough to avoid an extra dc voltage amplification stage or, as it is shown in Fig. 1.3(c) a dc-dc converter is required to provide sufficient voltage for the inverter and perform the MPPT function. The normal operating input voltage in European systems is between 375 V and 525 V and in the US system this voltage is between 200 and 300 volts. There are no losses associated with string-diodes and a

separate MPPT [8] can be applied for each string. This is assumed to increase the overall efficiency, when compared to the centralized inverter.

The multi-string technology, as it is shown in Fig. 1.3 (c), is a further development of the string inverter and can provide a higher power compared to the single string technology [9]. Since a dc-dc converter is connected to each string, the mismatch losses between the strings are eliminated but it does not provide a solution for the mismatch losses within one string. Also, this technology improves the system modularity and scalability as several strings can be connected in parallel to one inverter and the owner can add more strings and scale up the system size and power.

The ac-module technology, as it is demonstrated in Fig. 1.3(d), is the integration of a single phase inverter and a single PV module. This configuration provides an individual MPPT for PV module and eliminates any mismatch losses and can increase the maximum power output of the system by 20%[10]. The scalability of the entire PV system is also improved using this technology. If the system owner needs to scale up the system to have more power, he can simply add as many PV panel with ac-module to the system as structurally possible. The ac module technology also eases the mass production and as a result can lead to lower system cost.

The most important feature of the ac-module technology is the Plug-N-Play (PNP) ability. The consumer can (theoretically) buy his/her own PV panel with ac-module and simply plug it into the house just like any other appliance. The next sub-section discusses this feature in more detail.

#### 1.1.2.3 The Future

As it is mentioned in the previous sub-section, ac-module technology comes with features that make it suitable for residential applications. The most interesting feature of this technology is its PNP ability which means it can be used by persons without any knowledge of electrical installations. However, with the current standards and regulations for the grid tied equipment it is not legal for untrained individuals to buy and install a PV system without inspection so what PNP really means is that it eases the installations and inspection procedures thus reducing the labor and inspector costs.

Due to the aforementioned flexibility and feature of the ac-modules, it is believed that the ac-module will be the future technology for residential applications. According to [11], An ac-module is an electrical product and is the combination of a single module and a single power electronic inverter that converts sunlight into alternating electrical (AC) power when it is connected in parallel to the network. The inverter is mounted on the rear side of the module or is mounted on the support structure and connected to the module with a single point to point DC-cable. Protection functions for the AC side (e.g. voltage and frequency) are integrated in the electronic control of the inverter.

Due to the growing interest in ac-modules for residential applications, this subject has been extensively studied during the past decade [12]. The available topologies have been categorized based of different criteria including the number of conversion stages, design specifications[13], transformer type [14] and dc-link type[12]. The next section introduces the different inverter topologies for ac-module application.

## 1.2 Inverter topologies for ac-module application

This section reviews the possible inverter topologies for ac module applications based on the type of dc link [12].

All of the available topologies for ac-module or micro-inverter applications can be classifies into three different categories:

- Inverter with a dc link
- Inverter with a pseudo ac link
- Inverter without dc link

It is also very common to characterize the performance of ac-modules topologies base on the following four different criteria:

1. Power density, which is the indicator of compactness of ac module. The goal for the next generation of ac modules aim at 1 W/cm$^3$.
2. Efficiency, which is the primary target of every ac-module design. AC-modules usually have smaller efficiency compared to large inverters.
3. Reliability, since the ac-modules are mounted on PV panels, it is important that their lifetime is somewhat close to the PV module lifetime. PV module manufacturers usually warranty their products for up to 25 years so it is expected that ac-modules have the same lifetime.
4. System cost, as the price of PV modules drop each year, the inverter cost plays an important role in the total cost of the system. In today's market, the

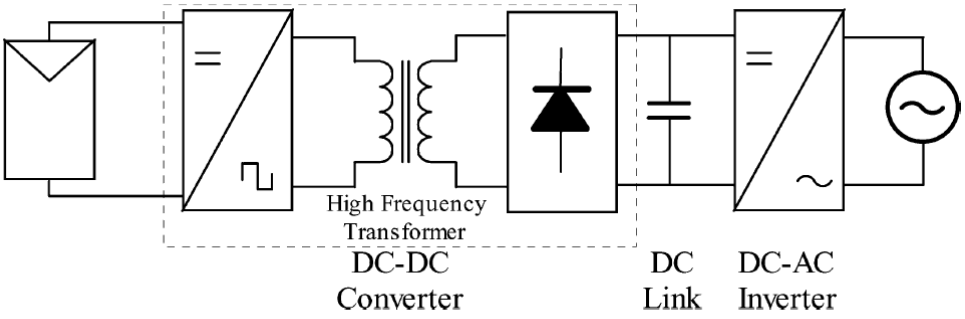


**Fig. 1.4: general form of ac-modules with a dc link.**

price of $.7 per peak watt has been achieved and the goal for next five years is $.25 per watt.

Considering the abovementioned four criterion, different ac-module designs have been proposed. Some of these designs provide the isolation and voltage amplification trough an isolated transformer and others rely on non-isolated step-up topologies to boost the PV voltage to the voltage required for inverters. In the next sub-sections, some of the most interesting topologies for ac-modules are illustrated and characterized based on the aforementioned criteria.

### 1.2.1 Topologies with ac-dc link

A general form of these types of ac-modules is shown in Fig. 1.4. In this type of topologies, the PV voltage is amplified to a higher voltage required by grid using a dc-dc converter. Four topologies have been proposed in this category, which are demonstrated in Fig. 1.5.

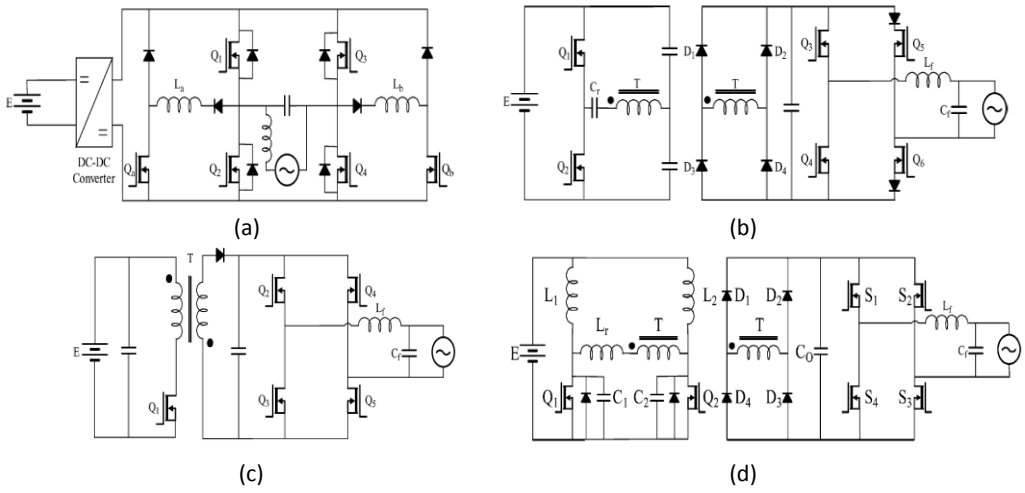


**Fig. 1.5: Topologies with dc-link**

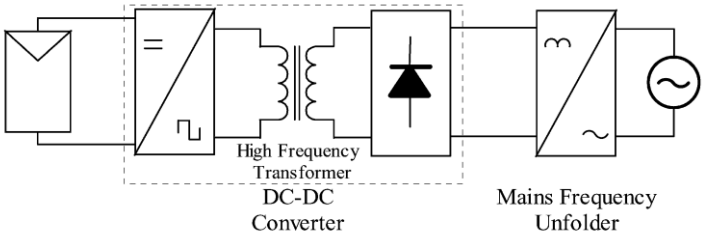


**Fig. 1.6: general form of an ac-module topology with pseudo dc link**

Topology in Fig. 1.5(a) utilizes a soft switched dc-ac converter [15]. The detailed schematic of dc-dc stage is not provided as the contribution of the paper was on the dc-ac stage.

Topology in Fig. 1.5(b) employs a series resonant half bridge converter in the dc–dc conversion stage [16]. The dc–ac converter is a modified full bridge inverter, with two additional diodes. The left leg switches operate at high frequencies to control the current injected to the grid while the right leg switches are controlled by the polarity of the grid voltage and switch synchronously with the zero crossings of the grid voltage.

**Table 1.2: comparison of ac-modules with dc-link**

| Topology | Rated Power | Component Count | | | | Max Efficiency | PCB Size $mm^2$ |
|---|---|---|---|---|---|---|---|
| | | Active switch | Diode | Magnetic core | Copper winding | | |
| Fig. 1.5 (a) | 200W | >6 | >4 | >2 | >2 | 96% | 100 ×480 |
| Fig. 1.5 (b) | 250W | 6 | 6 | 1 | 2 | - | - |
| Fig. 1.5(C) | 100W | 5 | 1 | 1 | 2 | - | - |
| Fig. 1.5 (d) | 100W | 5 | 4 | 4 | 5 | 90% | - |

The inverter in Fig. 1.5(c) is a flyback converter as the dc–dc conversion stage cascaded with a current controlled PWM inverter as the inverter stage [17].

The topology shown in Fig. 1.5(d) employs a ZVS two-inductor boost converter in the dc–dc conversion stage [18]. A conventional PWM converter follows to convert the dc voltage to the grid compatible ac voltage.

Several key parameters of these topologies are listed in Table 1.2. Among the four topologies listed in Table II, the converter shown in Fig. 1.5(c) has the smallest component count and this could lead to a lower converter cost and greater converter reliability. However, both the dc–dc and the dc–ac conversion stages in employ the hard-switching solutions, which will make it impossible to maintain high converter efficiencies under high switching frequencies. The converters shown in Fig. 1.5(a), (b) and (d) are able to remove the switching losses either in the dc–dc or the dc–ac conversion stages or both by employing the soft switching technologies. High efficiencies can be obtained but at the cost of higher component

counts. The switches in these converters also demand higher voltage and current ratings due to the nature of the resonant circuit.

### 1.2.2 Topologies with pseudo dc link

Fig. 1.7 illustrates the general structure of an ac-module topology with pseudo dc link. In this topology, a modulated dc-dc converter produces a rectified sinusoidal voltage on the dc-link. A square wave controlled inverter then unfolds the rectified sinusoidal voltage to a sinusoidal voltage.

Topology presented in Fig. 1.7(a) uses a boost converter to increase the input voltage and then a push-pull converter is used to generate the rectified sinusoidal current at its output which is finally unfolded using an unfolding bridge [19].

Topology if Fig. 1.7(b) is a current fed push-pull converter, which boosts the voltage level, followed by a modulated buck converter, which produces a rectified sinusoidal waveform [20]. This is finally unfolded by a CSI.

The inverter in Fig. 1.7(c) employs a modulated flyback converter to generate a rectified sinusoidal waveform, which is unfolded by the following CSI [21], [22] .This topology is very similar to that shown in Fig. 1.5(c) except for the control strategy. The sinusoidal modulation is applied to the operation of the flyback converter in this topology therefore a grid-commutated line frequency unfolder can be utilized. This topology features simple design and control and also reduced number of components. Several other topologies that have been derived from flyback will be discussed later.

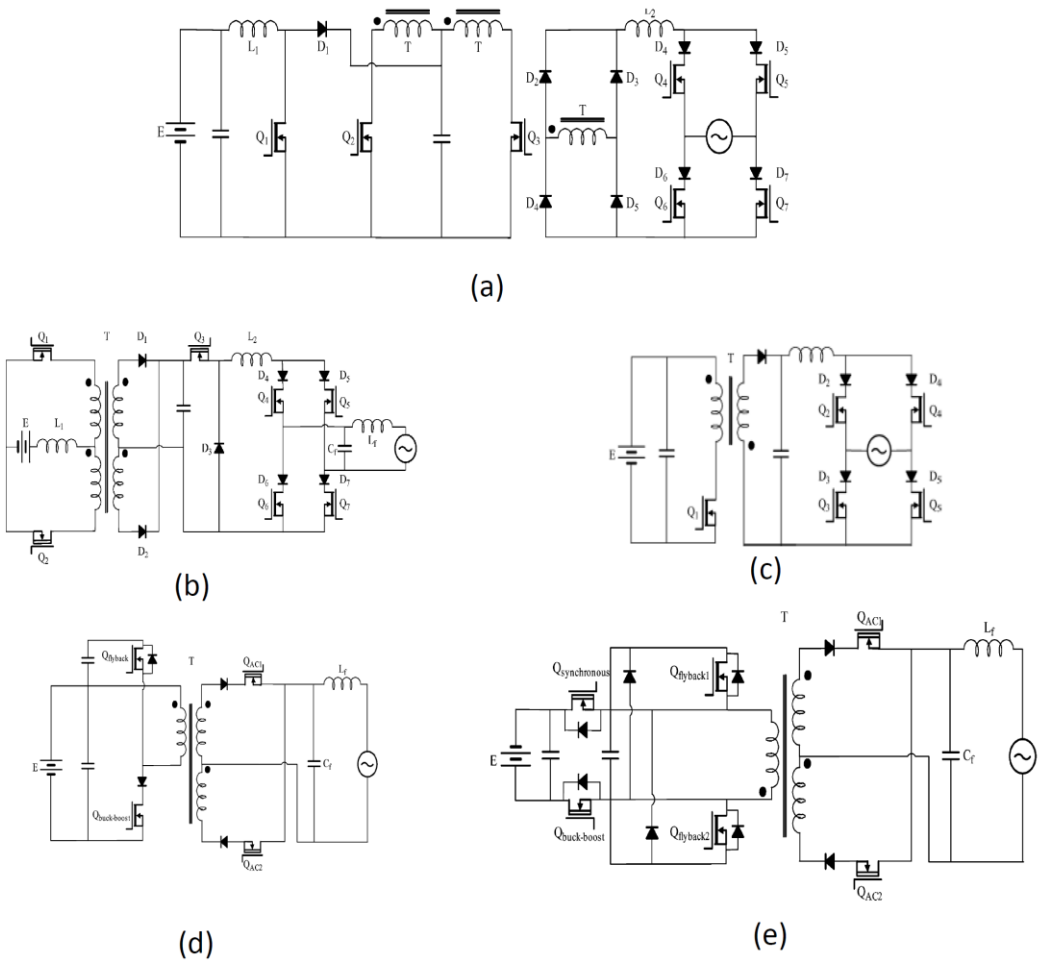


**Fig. 1.7: Topologies with pseudo dc-link configuration.**

The topology shown in Fig. 1.7(d) is based on the cascade of the buck boost and the flyback converters [23], [24]. In this topology, the energy is transferred to the transformer magnetizing inductance through the buck boost switch and then to the intermediate capacitor through the flyback switch. Finally, the energy is transferred to the output grid through the center-tapped transformer and the two switches. The buck boost switch and the two switches on the transformer secondary side are required to be series connected with the diodes to block the reverse current.

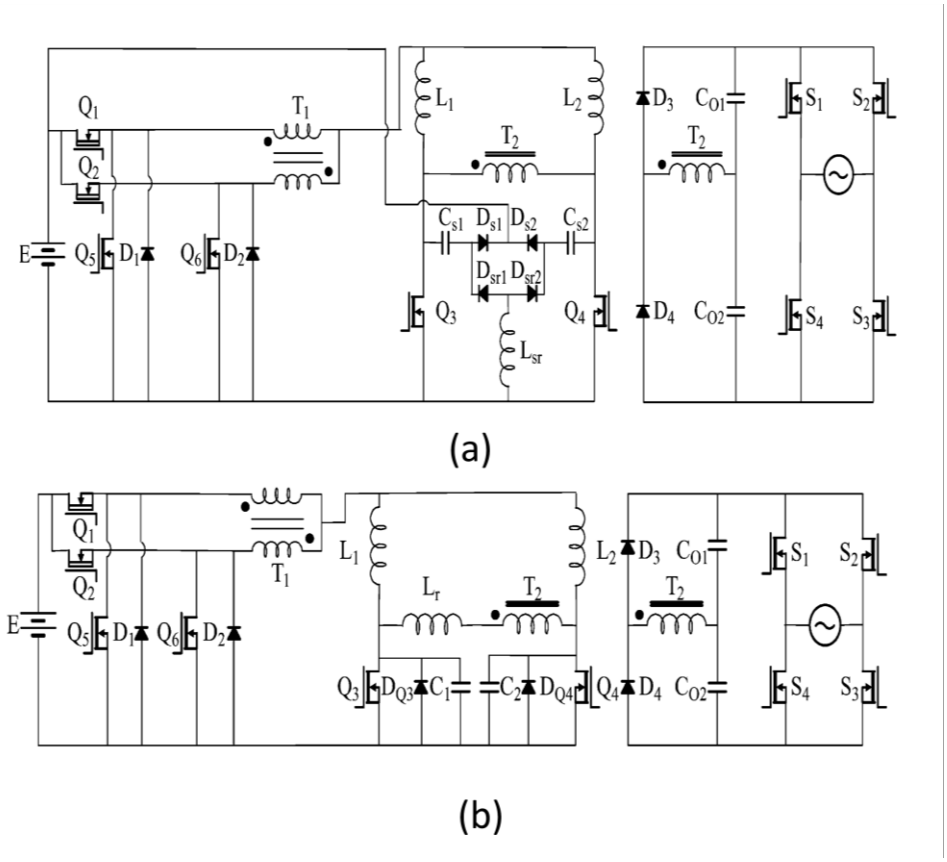


**Fig. 1.8: Topologies with pseudo dc-link configuration, continued.**

The topology shown in Fig. 1.7(e) is a variation of Fig. 1.7(d). Compared with Fig. 1.7(d), this topology offers the important feature of recovering the stored energy in the leakage inductance of the flyback transformer.

Fig. 1.8 (a) employs a highly efficient, sinusoidal modulated two-phase synchronous buck converter cascaded with a two-inductor boost converter to produce a rectified sinusoidal waveform and a voltage unfolding stage follows [25], [26]. Passive non-dissipative snubbers are also used in the converter to partly recover the switching loss in the hard switched two-inductor boost converter. The ZVS two-inductor boost topology shown in Fig. 1.5(d) can also

**Table 1.3: comparison of topologies with pseudo dc-link**

| Topology | Rated Power | Component Count | | | | Max Efficiency | PCB Size $mm^2$ |
|---|---|---|---|---|---|---|---|
| | | Active switch | Diode | Magnetic core | Copper winding | | |
| Fig. 1.7(a) | 350W | 6 | 5 | 3 | 5 | 90% | 100 ×480 |
| Fig. 1.7 (b) | 300W | 7 | 7 | 3 | 6 | 80% | - |
| Fig. 1.7(c) | 150W | 5 | 1 | 2 | 3 | - | - |
| Fig. 1.7 (d) | 100W | 4 | 3 | 1 | 3 | - | - |
| Fig. 1.7 (e) | 160W | 6 | 4 | 1 | 3 | 86.7% | - |
| Fig. 1.8 (a) | 100W | 10 | 8 | 3 | 7 | 92% | 125×200 |
| Fig. 1.8 (b) | 100W | 10 | 4 | 4 | 7 | 91% | 125×225 |

be employed as part of the dc–dc conversion stage in order to avoid the switching loss in the two-inductor boost converter under high frequency operations. This results in topology shown in Fig. 1.8(b).

Several key parameters of the presented micro-inverter topologies with pseudo dc-link are presented in Table 1.3.

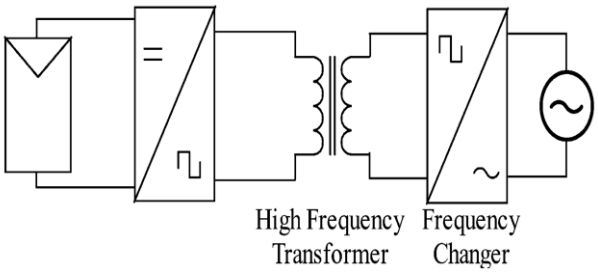


**Fig. 1.10: general form of an ac-module topology without dc link**

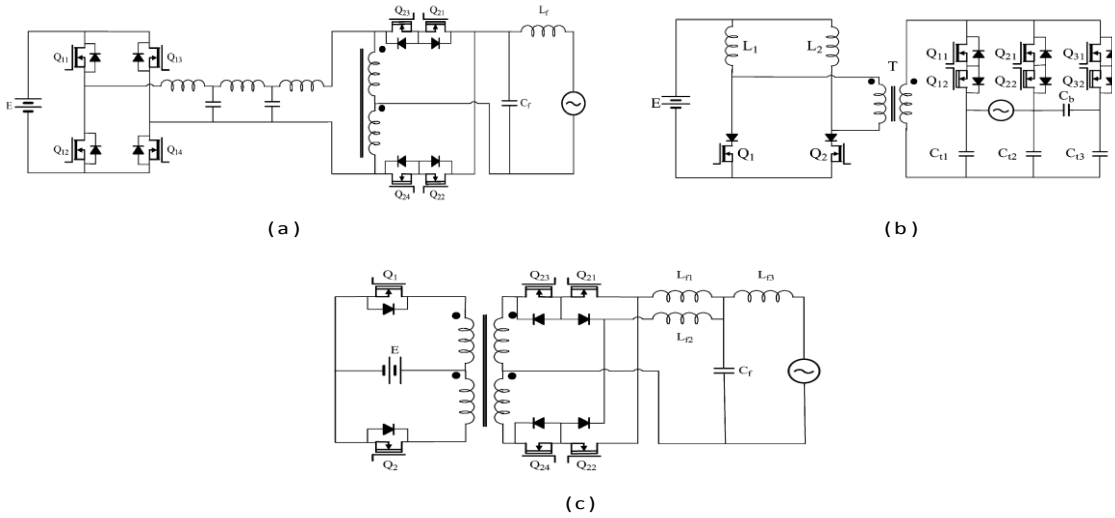


**Fig. 1.9: Topologies without dc-link.**

### 1.2.3 Topologies without dc-link

Fig. 1.10 illustrated the general configuration of ac-module topologies without dc-link. In this configuration, the dc voltage is transformed to a high frequency voltage and then amplified to a higher level using a high frequency transformer. The amplified high frequency voltage is then transformed to the grid frequency current or voltage using a frequency changer. The most interesting topologies in this category are presented in Fig. 1.9.

**Table 1.4: several key parameters of micro-inverter without dc link.**

| Topology | Rated Power | Component Count | | | | Max Efficiency | PCB Size $mm^2$ |
|---|---|---|---|---|---|---|---|
| | | Active switch | Diode | Magnetic core | Copper winding | | |
| Fig. 1.9(a) | 30W | 8 | 0 | 4 | 5 | - | 100 ×480 |
| Fig. 1.9(b) | 300W | 6 | 0 | 1 | 4 | - | - |
| Fig. 1.9 (c) | 100W | 8 | 2 | 1 | 2 | - | - |

In Fig. 1.9(a), an H-bridge inverter transforms the dc voltage into a high frequency ac voltage. The high frequency voltage is then converted into a current source through impedance-admittance conversion [27]. Finally a forced-commutated cyclo-converter transforms the high frequency current to the line-frequency current.

The topology shown in Fig. 1.9(b) is a push-pull converter, which transforms the dc voltage to the ac waveform [28]. The high frequency ac voltage is then converted directly to the ac voltage of the grid frequency through a forced-commutated cyclo-converter.

The topology shown in Fig. 1.9(c) is based on the two-inductor boost converter [12], [29]. The two-inductor boost converter first transforms the dc voltage to the high frequency ac current. A frequency changer made up of three bidirectional switches then converts the ac current of the high frequency to the ac voltage of the grid frequency. Another attractive feature of this converter is the non-polarized capacitor as a second phase in the load, which provides the power balance and removes the need of the electrolytic capacitor normally required at the converter input to handle the current ripple at twice the line frequency

common to the single phase inverter applications. However, a diode is required to be series connected with the primary side MOSFET in the practical implementation as negative drain source voltages exist due to bidirectional power flow. Several key parameters of these type of micro-inverters are summarized in Table 1.4 [12].

## 1.3 Selecting the suitable topology for residential applications

As it is mentioned in the previous sections, the goal of this thesis is to design and implement a low cost, high efficiency PV inverter system for residential applications. The inverter topology that is selected for this purpose has to satisfy: low cost, high efficiency, compact design and inherent isolation conditions. By comparing the key parameters of the Tables 1.2, 1.3, and 1.4 it is evident that the flyback topology presented in Fig. 1.7(c) offers the best solution.

A flyback micro-inverter can be realized with the minimum number of silicon devices. It has a single high frequency MOSFET and one diode. It also has a single high frequency magnetic component (i.e. flyback transformer), as a result, it offers a low cost and high efficiency. In terms of converter control, the flyback is a current source converter so it is able to control the grid current directly, thus, no complicated current controller is needed and the entire controller can be implemented in a low cost microprocessor (rather than a costly DSP or FPGA). The current source nature of the flyback converter makes it extremely easy to connect micro-inverters in parallel. Due to these interesting properties of flyback micro-inverter, a lot of efforts has been made by researchers to improve the efficiency and lower the cost of this converter [30]–[38].

One of the main sources of power loss in the flyback converter is the transformer leakage inductance. The energy stored in the leakage inductance during the ON time of the main switch does not transfer to the secondary side and it appears as power loss in the converter. It also causes a voltage spike across the drain-source of the flyback's main switch. It also causes a high EMI during the turn-off process that can interfere with the control circuit. Numerous efforts have been made by various authors to get around these problems and recover the stored energy of the leakage inductance and increase the total efficiency of the flyback micro-inverter system. In the following, we review some of these efforts.

### 1.3.1 Flyback micro-inverter

As it is mentioned before, because of its low cost, control simplicity and inherent galvanic isolation, the flyback micro-inverter is one of the most attractive topologies for the residential PV applications. In this section, we summarize some of the recent efforts by various authors to increase the efficiency of the flyback micro-inverter.

The first approach to improve the efficiency of the converter is to reduce the leakage inductance energy loss [30]. The conventional RCD clamp circuit absorbs the leakage energy and dissipates it in the snubber resistor. If the leakage inductance is large, the dissipated energy is much larger than the energy stored in the leakage inductance due to part of the magnetizing energy fed to the snubber circuit during the commutation time, which deteriorates the efficiency. The lossless snubber for single-end converter was proposed to recycle the leakage energy, but the snubber parameters makes the circulating energy relatively large during normal operation, which limits the efficiency improvement [39].

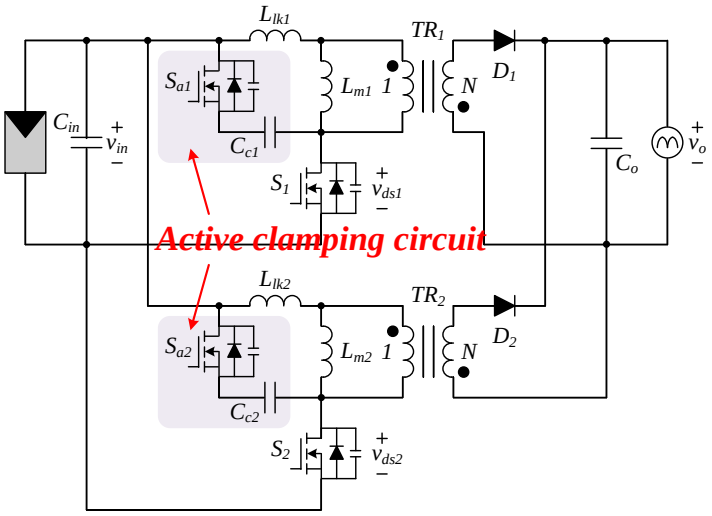


**Fig. 1.11: Conventional active clamping circuit in flyback micro-inverter**

Another solution for recovering the stored energy in the leakage inductance of the flyback transformer is using active clamp circuits. The conventional active clamped flyback is demonstrated in Fig. 1.11. The active clamp can recycle the energy in the leakage inductor and achieve soft switching for both primary and auxiliary switch [30], [36], [40], [41]. It also clamps the voltage overshoot of the MOSFET to a certain level enabling the use of lower voltage MOSFET which leads to lower conduction loss. Since the auxiliary switch does not share the same source pin with the main switch, these active clamp circuits either require an isolated gate driver for the auxiliary switch which makes the system complicated and costly or they require a P-channel MOSFET which reduces the efficiency due to poor $R_{ds(on)}$ performance of these switches compared with the N-channel MOSFETS.

As it is shown in Fig. 1.12, a non-complementary active clamp control method has been also proposed to achieve high efficiency both for full-load and light-load condition by reducing a circulating energy [30]. Furthermore, appropriate design parameters under DCM

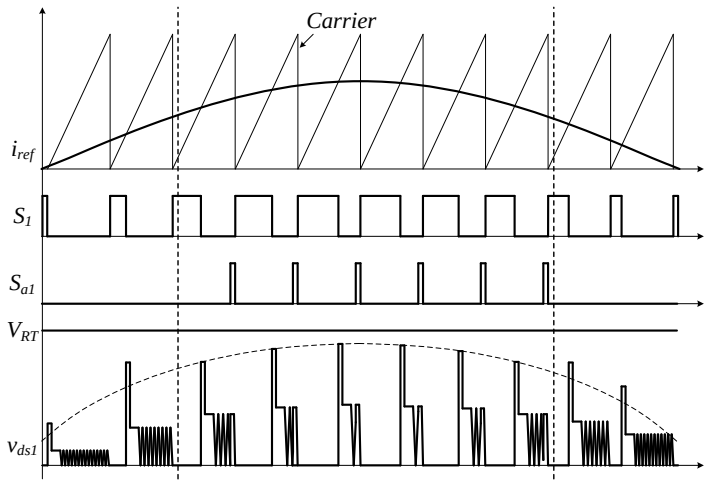


**Fig. 1.12: Main operation waveforms of the active clamp circuit with non-complementary gate drive signal.**

operation have been specified to obtain maximum weighted efficiency through analytical loss calculation [37]and adaptive active clamping and phase control method [36] and hybrid control strategy combing two-phase and one-phase DCM control [38] have been proposed to improve weighted efficiency according to the output power of a PV module. Using a center-tapped transformer and bidirectional switched on the grid-side, a turn-on ZVS approach is proposed in [42] which utilizes snubber to maintain the voltage spike within limits.

In [32], an open-loop control based on the feedback of the primary current in the continuous conduction mode (CCM) operation has been proposed to accommodate a right half plane (RHP) zero in the control to output current transfer function, thus it showed an efficiency improvement compared to the DCM scheme. A through dynamic modeling and control of an interleaved flyback micro-inverter along with a two-step controller design based on realistic fourth-order system modeling including the dynamics of the output CL filter is presented in [43] which aims to compensate the instability issue of the converter working in

CCM. Also, in order to reduce the cost and complexity of the flyback micro-inverter system, the idea of multiple-integrated converter modules sharing a single unfolding bridge is presented in [44] based on the flyback micro-inverter operating in CCM.

In this thesis, a novel snubber circuit for the flyback micro inverter is proposed. The proposed snubber only utilizes a small N-channel MOSFET that shares the same source with the main flyback switch and also a small capacitor (.5nF ~ 2nF) capacitor. The proposed snubber limits the voltage overshoot across the main switch and also recovers the stored energy in the leakage inductance of the transformer. It also exploit the parasitic elements of the flyback circuit, including the transformer winding capacitances and also the secondary rectifier capacitance in order to further reduce the voltage overshoot and increase the efficiency of the converter.

## 1.4 Presented innovative approaches in this thesis

As we mentioned in the previous section, this thesis presents a novel adaptive snubber circuit for the flyback micro-inverter. In association with the presented adaptive snubber, a novel controller is also proposed that aims to increasing the efficiency of the micro-inverter system.

Based on the presented adaptive snubber, an optimization procedure is introduced that aims to optimize the parameters of the micro-inverter to achieve the maximum CEC efficiency. The presented optimization procedure accurately takes into account the switching, conduction and the transformer losses of the converter.

In the following sections of this thesis, these innovations in the inverter stage of the IFMI are presented in detail.

# 2. Inverter Stage Innovation

## 2.1 Introduction

This chapter introduces the design of the micro-inverter and presents the innovations in the control and structure of the inverter that lead to a higher efficiency and lower overall cost [45].

As it is mentioned in the previous chapter, the inverter to be designed is an Interleaved Flyback Micro-Inverter (IFMI). The basic structure of the IFMI is presented in Fig. 2.1. The IFMI is composed of decoupling capacitors, interleaved flyback inverter, unfolding bridge and CL filter.

The decoupling capacitors are used to filter the 120Hz current drawn by the inverter and provide a stable voltage for the PV panel to work at the MPP. The interleaved flyback inverter provides galvanic isolation between input and output of the micro-inverter while injecting a rectified sinusoidal current to the output. It is also worth mentioning that the "interleaved" topology is used in order to achieve the maximum power of 250W with highest possible efficiency. The unfolding bridge, as its name implies, unfolds the rectified sinusoidal current of the interleaved flyback inverter to a sinusoidal current and injects that current to the grid. The CL filter, filters the current harmonics and provides a low distortion current for the grid.

**Table 2.1: basic design specifications**

| | |
|---|---|
| Nominal output power | 250W |
| Input voltage range | 22 - 40V |
| Maximum input current | 9.5A |
| PV side over voltage protection | 45 V |
| Nominal grid voltage | 230 & 240 V(RMS) |
| Nominal grid frequency | 50 & 60 Hz |
| Current harmonics | According to IEEE1547 |
| Maximum efficiency | >96% |

The requirements and standards for the IFMI are very high, thus every aspect of the design, including silicon devices, magnetic components, capacitors, gate drivers and controller performance should be carefully considered. The basic requirements of this design are listed in Table 2.1.

## 1.1 Innovative IFMI

In this section, the innovations on the circuit structure of the IFMI are presented.

One of the main advantages of the flyback converter is its low cost and compact design and also inherent galvanic isolation. The flyback transformer serves a dual purpose of providing energy storage and also galvanic isolation, thus minimizing the magnetic component count compared to other types of isolated converters, for example, forward converter. In spite of these advantages, the flyback converter has several drawbacks, namely,

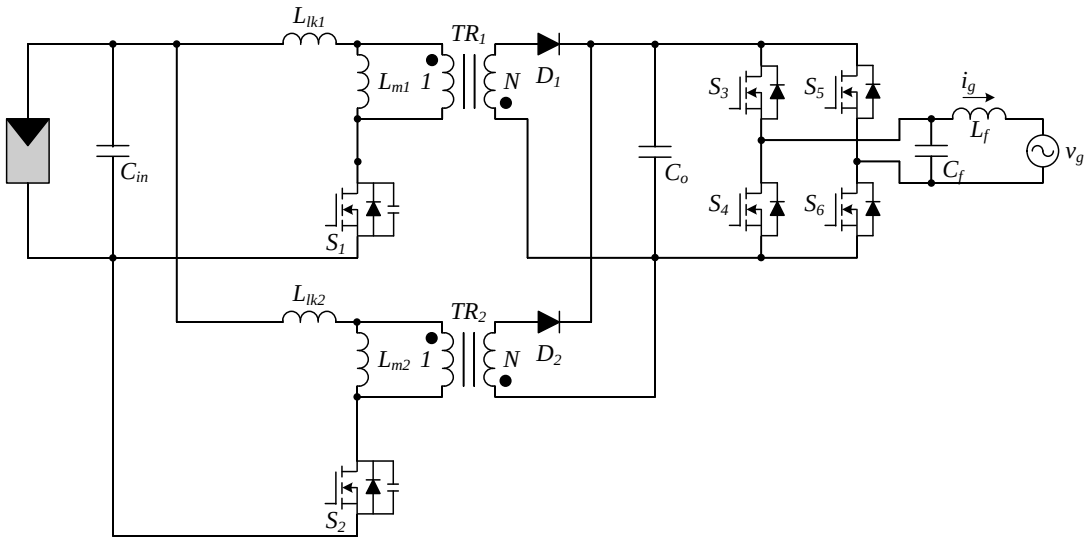


**Fig. 2.1: Basic configuration of an interleaved flyback micro-inverter.**

- relatively high voltage and current stress experienced by the switching components
- high peak and RMS current stress which is the primary detriment for the maximum output power
- leakage inductance of the flyback transformer, which leads to voltage spikes and power loss.

These drawbacks limit the application of the flyback converter and reduce its maximum efficiency. So, in order to reduce the effects of these problems, we propose several novel solutions to address each one.

### 1.1.1 IFMI mode of conduction

As it is already mentioned, one of the major drawbacks of the flyback converter is the excessive peak and RMS current stress on its switching components including the main

MOSFET and also the secondary rectifier. This problem is typically due to the fact that the flyback converter does not exploit its magnetic component (flyback transformer) to its full capacity. This problem becomes specifically worse when the converter works in the Discontinuous Conduction Mode (DCM) where for a period of time, no energy is being stored in the transformer and no energy is transferred to the output side [46].

In order to reduce the peak and RMS current stress on the switching components and energy storage elements, Continuous Conduction Mode (CCM) and also Boundary Conduction Mode (BCM) can be employed.

Several authors have explored the possibility of controlling IFMI in CCM [32], [43]. These researches show that the application of CCM in IFMI is not a good solution as the inverter tends to act as a load independent voltage source due to incomplete discharge of the magnetizing inductance [42]. Additionally, the presence of the right-half-plane zero in the output current to the duty cycle transfer function introduces a challenge in controlling the output current in CCM. This problem is mitigated using the charge control to control the primary current instead of the secondary current in [32]. However, the charge control scheme may result in sub-harmonic oscillations. It may also result in periodic change in the operation mode of the converter between CCM and DCM under certain operation conditions.

The BCM operation mode is a special case of the DCM (or CCM) where the magnetizing current becomes zero just before the start the next switching cycle. Operation of the flyback converter in the BCM has a lot of advantages including:

- Lower current stress on flyback switch and transformer compared to the DCM

- Zero current turn on which results in lower switching loss
- Zero voltage turn on due to natural resonant of the magnetizing inductance with the MOSFET's output capacitance ($C_{oss}$)
- Simple control algorithm

All these benefits lead to a low cost and efficient PV inverter system. However the increased switching frequency near the zero crossing of the grid voltage due to small instantaneous power leads to increased switching and magnetics loss. To solve this problem, a hybrid switching strategy is adopted in this thesis which uses the DCM operation in the vicinity of the grid voltage zero crossing and then switches to BCM operation when the instantaneous transferred power is beyond a certain level. As a result, the switching frequency of the converter is limited to a certain interval and thus an optimum design for the magnetic components and filter capacitors can be achieved.

Using the hybrid switching strategy, the problem of increased switching frequency and also turn on losses is addressed. However, the main problems of the flyback converter which is the voltage overshoot across the main MOSFET and also the associated turn off losses have not been addressed. In order to solve these problems and reach a high efficiency of the PV inverter system, an innovative adaptive snubber is developed which is introduced in the next sub-section.

### 1.1.2 Innovative adaptive snubber

Fig. 2.2 illustrates the circuit configuration of the proposed flyback micro-inverter with the novel adaptive snubber which is suitable for use in converter operating with hybrid

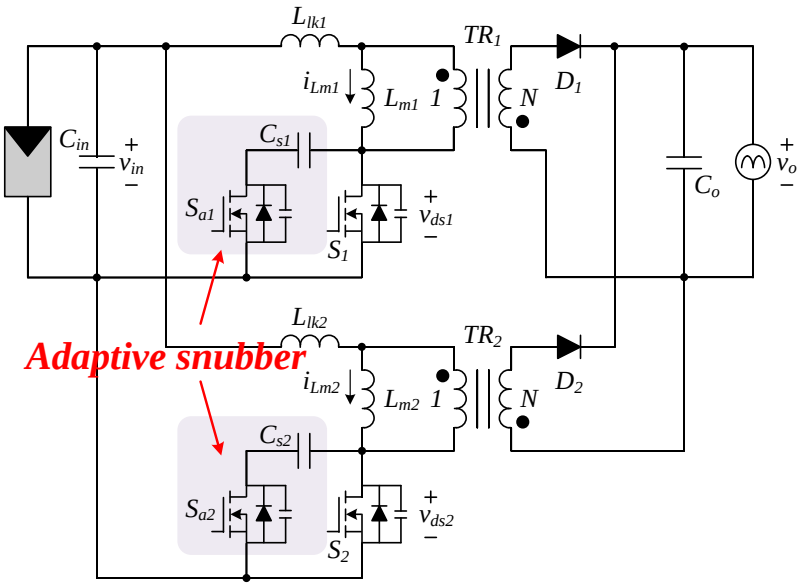


**Fig. 2.2: Circuit configuration of the proposed adaptive snubber scheme in flyback micro-inverter.**

conduction mode. The main operation waveforms of this converter are demonstrated in Fig. 2.3. The configuration of the adaptive snubber is similar to the previous active clamping circuit. However, the control scheme and the design procedure of the proposed adaptive snubber are entirely different.

The BCM operation of the flyback converter has several advantages compared to DCM operation in terms of power density and conversion efficiency. Since the BCM operation provides a natural ZVS turn-on for the main switch, the reduced switching loss allows higher switching frequency and compact design. However, it still has the turn-off switching loss that limits the maximum allowable switching frequency. Also, during the BCM operation of the converter and near the peak grid voltage where the instantaneous transferred power is high, the leakage inductance in flyback converter causes voltage

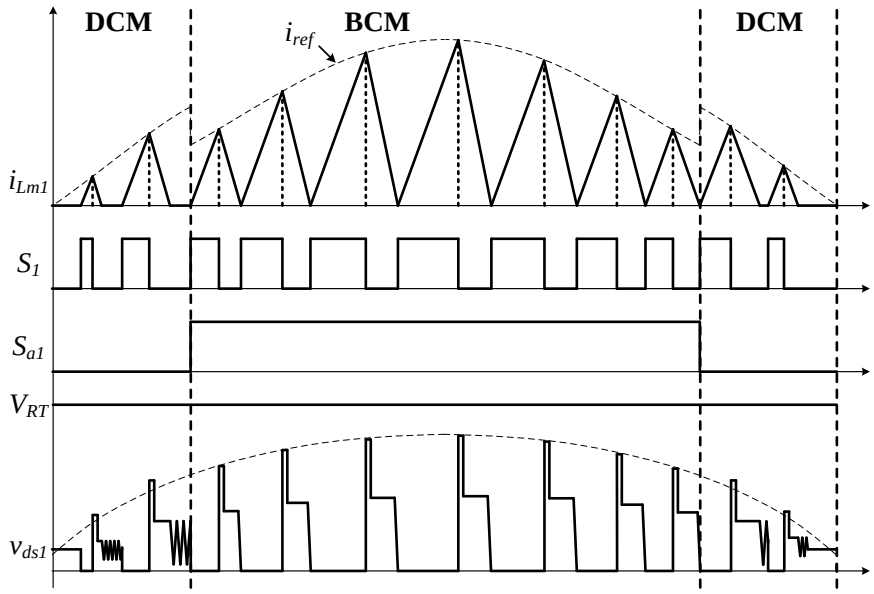


**Fig. 2.3: Main operation waveforms of the flyback inverter with the proposed adaptive snubber**

overshoot across the main switch at turn-off and the turn-off switching loss becomes more severe.

The proposed snubber solves these problems by adding additional capacitor in parallel with the main switch. This capacitor reduces the voltage overshoot and also lowers the rising slope of the turn-off voltage. These effects allow low conduction loss from the usage of lower voltage rating device and also reduce the turn-off switching loss of the main switch. This additional capacitor does not affect the soft-switching of the main switch at turn-on if enough time delay is applied between zero crossing of magnetizing current and the next turn-on switching signal.

Since natural turn on ZVS is not provided during the DCM operation of the flyback micro-inverter, the turn-on switching loss associated with the additional capacitor becomes

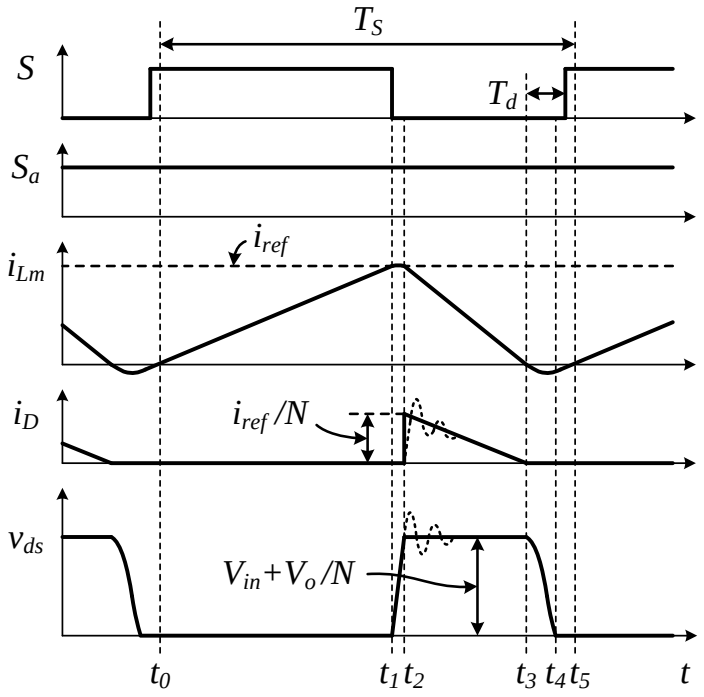


**Fig. 2.4:** **Theoretical operation waveforms under BCM.**

dominant and the reduction of turn-off switching loss becomes marginal. Therefore, to improve the overall efficiency of the flyback micro-inverter, as shown in Fig. 2.3, an auxiliary switch is employed to disconnect the snubber capacitor from the circuit when the converter works in the DCM mode. As a result, during the DCM operation of the converter the auxiliary switch ($S_a$) is off and during the BCM operation, when the natural turn-on ZVS is achievable, the auxiliary switch is always on, effectively adding the capacitor $C_s$ across the drain-source terminals of the main switch.

The proposed adaptive snubber provides the same advantages as the conventional active clamping method in terms of zero voltage switching and also limiting the voltage spike across the main switch at turn-off at a much lower cost. Furthermore, the auxiliary switch is

operated at only double line frequency and the required snubber capacitance is very small, in range of ten of nano-farad, which is almost hundred times smaller than the required capacitance value in the conventional active clamping. Also, the additional isolated power supply for driving the auxiliary switch is not required any more since an N-channel MOSFET can be used that shares the same source terminal with the main MOSFET. All these advantages reduce the cost and complexity and also increase the overall efficiency of the PV micro-inverter system.

#### 1.1.2.1 Operation principle

Fig. 2.4 shows the theoretical operational waveforms of the proposed flyback micro-inverter under BCM during one switching period $T_S$, and Fig. 2.5 shows the equivalent circuits for each operational mode.

To simplify the analysis of the operational modes, only one flyback converter is considered due to the fact that converters operate in the same manner in interleaved mode. Also, the voltages $V_{in}$ and $V_o$ and the reference current $i_{ref}$ are assumed to be constant during $T_S$. Furthermore, the auxiliary switch $S_a$ is always in the ON state, since the converter operates under BCM. Each operation mode is described next.

1) Mode1 ($t_0 - t_1$)

Just before $t_0$, the switch $S$ has turned on, and the magnetizing inductor current $i_{Lm}$ increases linearly from zero until it reaches $i_{ref}$. At this moment, the switch $S$ turns off and *Mode 1* ends. The required time in this mode is:

$$t_{01} = \frac{L_{tot}}{V_{in}}.i_{ref}$$
$$L_{tot} = L_m + L_{lk} \approx L_m \quad \textbf{(2.1)}$$

Although the $i_{ref}$ is assumed to be constant during $T_S$, the actual value of the $i_{ref}$ is continuously changing across the grid period [38], [41], as:

$$i_{ref} = \begin{cases} \sqrt{\frac{2T_{DCM}P_o}{L_m}} \cdot \sin \omega t & in\ DCM \\ \left( \frac{\sqrt{2}V_o \sin \omega t}{V_{in}} + N \right) \cdot \sqrt{2}\frac{P_o}{V_o} \sin \omega t & in\ BCM \end{cases} \quad (2.2)$$

where $T_{DCM}$ is the switching period in DCM, $P_o$ is the output power of the interleaved converter, $\omega$ is the angular frequency of the grid voltage, and $N$ is the transformer turns ratio.

2) Mode 2 ($t_1$ - $t2$)

At $t_1$, switch $S$ turns off and the resonance between inductors ($L_m$, $L_{lk}$) and capacitors ($C_s$, $C_{oss}$) begins where $C_{oss}$ is the parasitic capacitor of the switch $S$. The resonant frequency is given by:

$$f_{res} = \frac{1}{2\pi\sqrt{L_{tot}C_{tot}}}$$
$$C_{tot} = C_s + C_{oss} \approx C_s \quad (2.3)$$

The duration of this mode is relatively short compared to the whole resonant period due to the large value of the magnetizing inductor current at turn-off, thus the voltage $v_{ds}$ increases almost linearly. This mode ends when the voltage $v_{ds}$ reaches $V_{in}+V_o/N$. Duration of this mode can be approximated by:

$$t_{12} = \frac{C_{tot}}{i_{ref}} \cdot \left( V_{in} + \frac{V_o}{N} \right) \tag{2.4}$$

As it is shown in (2.4), addition of the snubber capacitor $C_s$ causes $t_{12}$ to increase, which affectively reduces the rising slope of the voltage $v_{ds1}$ and allows the turn-off process to be soft and almost loss-less.

3) Mode 3 ($t_3 - t_4$)

The energy stored in the magnetizing inductor Lm is transferred to the output side. The output diode current $i_D$ linearly decreases to zero, thus the reverse-recovery effect of D is minimized. If the leakage inductance is assumed to be zero as ideal condition to simplify the operational analysis, the voltage $v_{ds}$ maintains the constant value of $V_{in}+V_o/N$ during this mode. However, in the real case, the leakage inductance causes a high frequency oscillation at the beginning of this mode as it is shown in the dotted waveforms of Fig. 2.4. The conduction path of the oscillating current is also shown in Fig. 2.5(c) with dotted lines. Without a snubber or clamping circuit to protect the main switch, this voltage spike enforces the use of a high voltage rated switching device which has normally a high $R_{ds(on)}$. Therefore, by adding the snubber capacitor Cs and limiting the voltage overshoot, a MOSFET with lower voltage rating can be used for the main switch, resulting in reduction of the conduction loss. The duration of this mode can be calculated as:

$$t_{23} = \frac{L_m}{V_o / N} \cdot i_{ref} \tag{2.5}$$

4) Mode 4 ($t_3 - t_4$)

This is a resonant mode similar to Mode 2. If the steady state value $v_{ds}$ at during Mode 3 satisfies the following equation:

$$\begin{aligned} & V_{in} + V_o / N > 2V_{in} \\ \rightarrow \quad & V_o > N V_{in} \end{aligned} \tag{2.6}$$

the voltage $v_{ds}$ decreases to zero with a resonant manner within the maximum of half resonant period as shown in (2.7) regardless of the amount energy stored in the magnetizing inductance.

$$t_{34} \leq \pi \sqrt{L_{tot} C_{tot}} \tag{2.7}$$

While the current $i_{Lm}$ flows negatively through the anti-parallel diode of the switch *S*, the gating signal of the switch *S* is applied, thus satisfying the ZVS turn-on. The time delay $T_d$ between the zero magnetizing current and the turn-on of switch *S* is given by the half the resonant period which is the maximum value of (2.7)

#### 1.1.2.2 Improved current reference

In the flyback micro-inverter, the reference current is very important because it directly affects the output current THD. The reference current in (2.2) is obtained by assuming the ideal conditions without considering the resonant modes in Mode 2 and 4. However, in the proposed flyback micro-inverter, these resonant modes cannot be ignored during BCM operation due to the added snubber capacitor. In particular, since the resonant

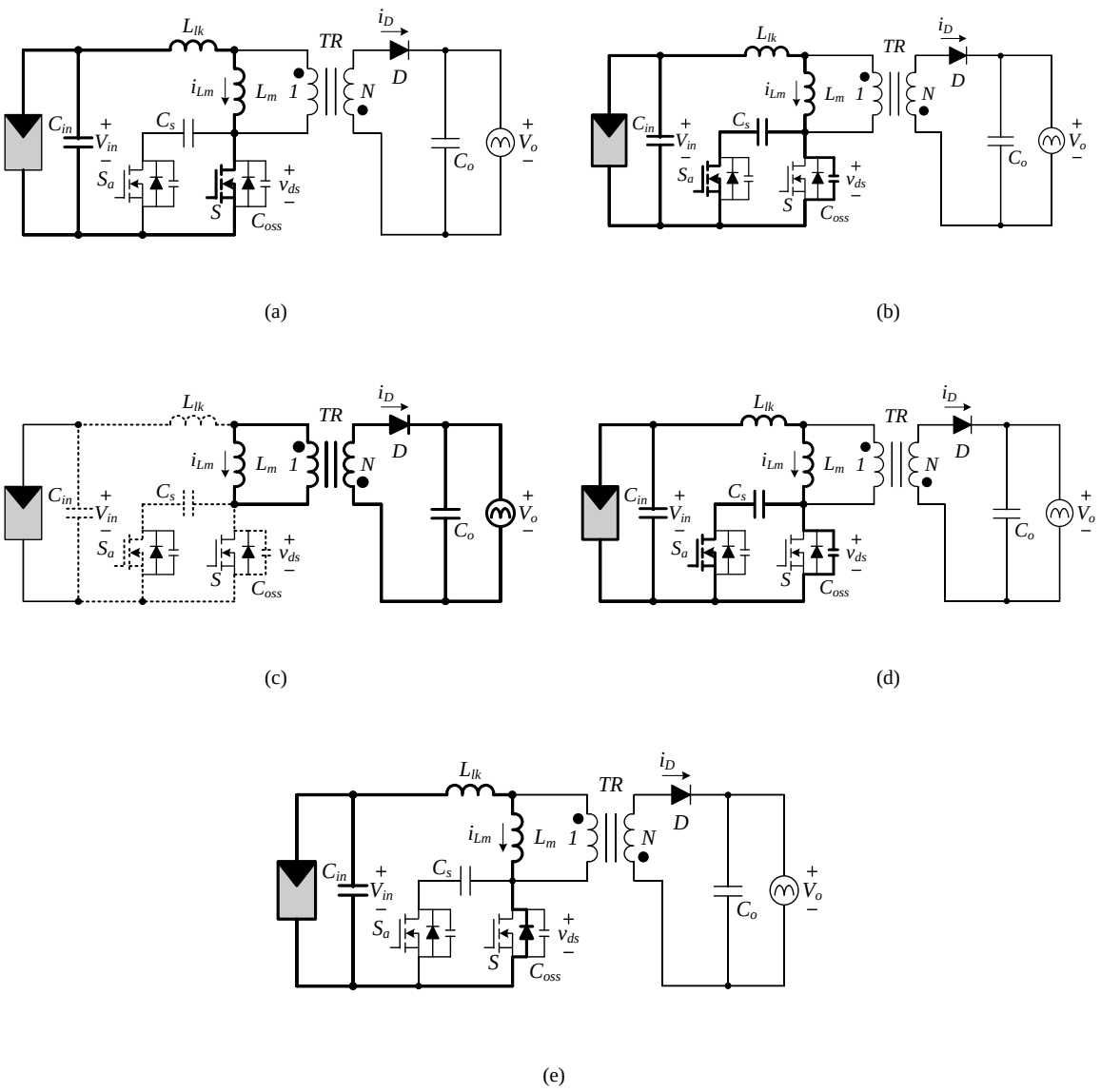


**Fig. 2.5: Equivalent circuits for each operational mode: (a) Mode 1 [$t_0$-$t_1$]. (b) Mode 2 [$t_1$-$t_2$]. (c) Mode 3 [$t_2$-$t_3$]. (d) Mode 4 [$t_3$-$t_4$]. (e) Mode 5 [$t_4$-$t_5$].**

period $t_{34}$ of (2.7) is dominant compared to the $t_{12}$ of (2.4), the reference current is modified only considering $t_{34}$ here.

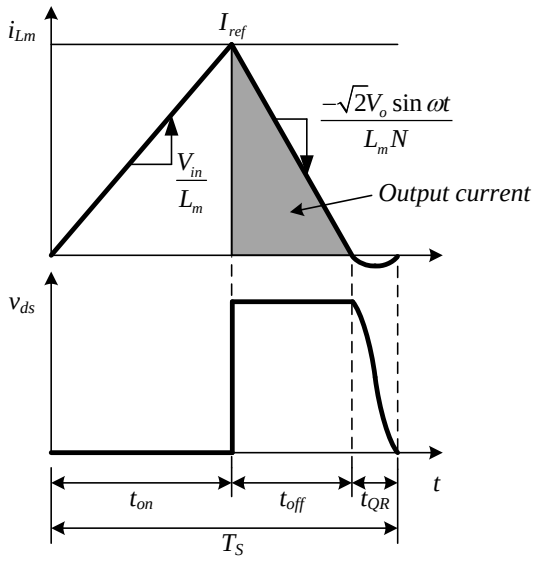


**Fig. 2.6: average output current during the BCM operation**

Fig. 2.6 shows the average output current during BCM operation with quasi resonant mode. The average output current proportional to the shaded triangle area. Therefore, it can be obtained as

$$i_{g\_avg} = \frac{t_{off} i_{ref}}{2TN}, \quad T = t_{on} + t_{off} + t_{QR} \tag{2.8}$$

From (2.8), the improved reference current can be obtained as

$$\begin{aligned} i_{ref} &= \frac{2TN}{t_{off}} i_{g\_avg} \\ &= \frac{A + \sqrt{A^2 + 4B}}{2} \end{aligned} \tag{2.9}$$

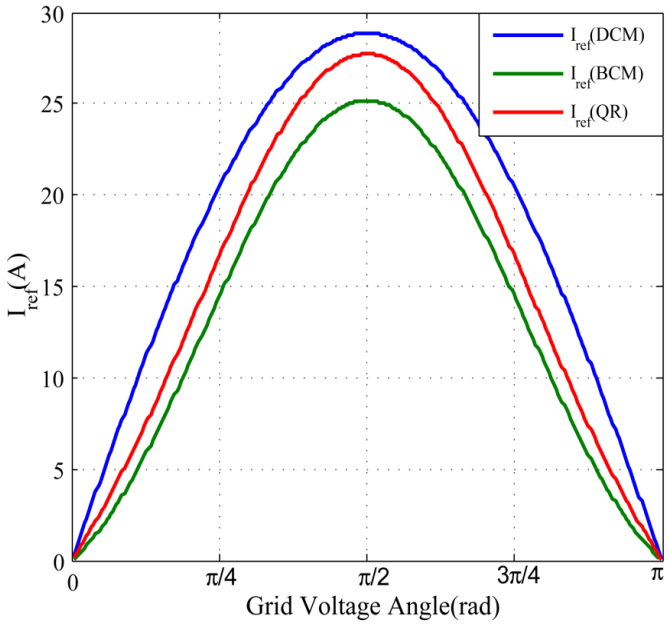


**Fig. 2.7: Reference current considering $F_{DCM}$=100kHz, N=6, $P_o$=250W, $V_o$=240V, $L_{tot}$=6μH and $C_{tot}$=10nF. Comparison between DCM, ideal BCM and BCM considering $t_{QR}$ in mode 4**

$$A = 2\left(\frac{\sqrt{2}V_g \sin \omega t}{V_{in}} + N\right)\left(\sqrt{2}\frac{P_o}{V_o}\sin \omega t\right)$$

$$B = 2\pi\sqrt{\frac{C_{tot}}{L_m}}\sqrt{2}V_g \sin \omega t \cdot \left(\sqrt{2}\frac{P_o}{V_o}\sin \omega t\right)$$

Fig. 2.7shows the original reference current of (2) in each operational mode and the improved one of (9) in BCM operation. Basically, two reference values in BCM are lower than DCM, and the improved one in BCM is a little higher than the original. Furthermore, Fig. 2.8 shows the amplitude ratio of the improved to the original reference in BCM. It can be noticed that the ratio is almost constant for the middle range of grid period corresponding to actual BCM operation. Therefore, for simple implementation, a constant value of around 1.1 can be multiplied to the original reference in BCM instead of directly using the complex equation of (9).

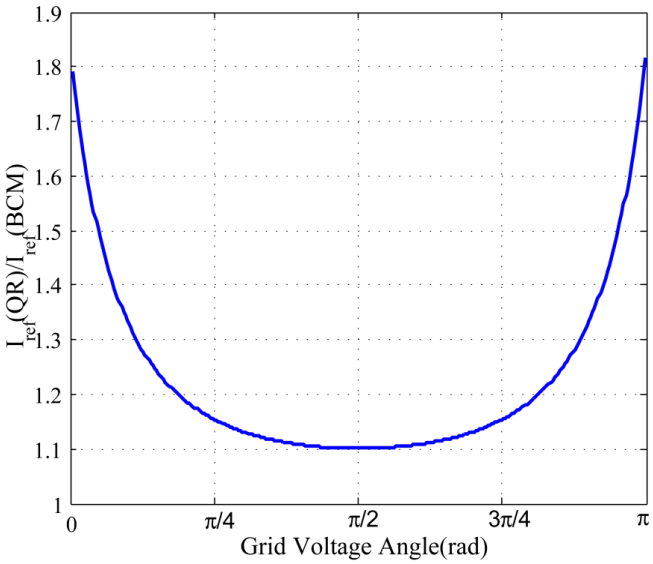


**Fig. 2.8: Reference current considering $F_{DCM}$=100kHz, N=6, $P_o$=250W, $V_o$=240V, $L_{tot}$=6μH and $C_{tot}$=10nF. Amplitude ratio of improved to original reference in BCM.**

Another issue that should be carefully considered regarding the harmonic content of the output current in the IFMI is the effect of oscillations in the DCM operation on the output current. In the DCM operation, after the rectifier's current reaches zero, there is an oscillation between the magnetizing (and leakage) inductance and Coss and primary winding's parasitic capacitance. During this oscillation, the energy is transferred back and forth between the primary and secondary windings affecting the total amount of energy transferred in each switching cycle. If the frequency of this oscillations is much higher than the switching frequency, then the effects are negligible. However, if the switching frequency and oscillation frequency are in the same range, then the total transferred energy in each switching cycle is affected which leads to distortion in the injected current to the grid.

# 3. Design and Implementation of IFMI

## 3.1 Design of the System Components

In this section, the design procedure of the IFMI to achieve the specifications of Table 2.1 is presented.

### 3.1.1 Electrolytic capacitors

Electrolytic capacitors are one of the most important factors in the design of the micro-inverter. The reason for that importance is threefold:

1. Electrolytic capacitors are among the biggest component in the IFMI design. They take up a lot of volume so in order to achieve a proper power density and inverter form factor, this component has to be selected carefully.
2. Electrolytic capacitors have to handle a large double-line-frequency (120 Hz) ripple current, so the ESR of these capacitors should be low enough to achieve high efficiencies.
3. Electrolytic capacitor are the major source of failure in PV inverter. Especially in micro-inverters where they are installed outdoors and without any active cooling, they are exposed to high temperatures. Thus in order to achieve high reliability, the designer should make sure that these capacitors are able to handle the ripple current at high temperatures.

The maximum ripple current in the electrolytic decoupling capacitors can be calculated as:

$$I_{ripple} = \frac{P_o(\max)}{V_{in}(\min)} \qquad \textbf{(3.1)}$$

where $I_{ripple}$ is the120Hz ripple current amplitude, $P_o(\max)$ is the maximum output power and $V_{in}(\min)$ is the minimum input dc voltage. Assuming $P_o(\max) = 250\ W$ and $V_{in}(\min) = 25\ V$, the maximum current ripple is $I_{ripple} = 10\ A(\max) = 7.071\text{A(RMS)}$. The selected capacitor(s) should be able to handle this maximum ripple current.

The size of the decoupling capacitor can be calculated knowing that the power into the dc link is constant and the power from the dc link follows a $\sin^2(\omega t)$ waveform.

$$C_{dc} = \frac{P_o(\max)}{2\omega V_{dc}\Delta V_{dc}} \qquad \textbf{(3.2)}$$

Where $\omega$ is the angular frequency of the grid and $\Delta V_{dc}$ is the voltage ripple amplitude. Assuming 50Hz grid frequency operation, $V_{dc} = 25\ V$ and $\Delta V_{dc} < 1.5V$ the required dc capacitor is $C_{dc} = 10.6\ mF$.

By comparing over 200 different capacitors, the best choice on terms of form factor, maximum ripple current, working temperature and ESR is parallel connection of four 63V, $3300\ \mu F$ capacitors from Nichicon. The part number of the selected capacitor is

**UVZ1J332MRD**. The operating temperature range of this capacitor is $-50\ ^{\circ}C \sim 105\ ^{\circ}C$ which is suitable for the micro-inverter application.

Based on (3.1), the effective RMS current of each capacitor is $I_{ripple} = 7.071/4 = 1.76\text{A}$ which is lower than the maximum allowable ripple current of the selected capacitors (1.95*mA*). Based on the Nichicon datasheet, the expected life of these capacitors can be calculated by

$$L_{op} = M_v L_b 2^{\frac{T_m - T_a}{10}} \tag{3.3}$$

Where $L_{op}$ is the expected operating life in hours, $M_v$ is the unit less voltage multiplier for the operating voltage, $L_b$ is the expected operating life in hours for full load rated voltage and temperature, $T_m$ is the maximum permitted internal voltage temperature in $^{\circ}C$ and $T_a$ is the actual internal working temperature. Most manufacturers use this model to predict the life of capacitors however, the parameters vary by capacitor type and also manufacturer. It is advised that for case diameters larger than 25*mm* with the significant ripple current take into account the temperature rise of the capacitor element over its case. Also, the parameter $M_v$ can be calculated as:

$$M_v = 4.3 - 3.3 \times \frac{V_{dc}}{V_r} \tag{3.4}$$

Where $V_r$ is the rated voltage of the capacitor and $V_{dc}$ is the applied dc voltage. Thus, based on (3.3) and (3.4) the expected life of the selected capacitors is:

$$L_{op} = 1000 \times (4.3 - 3.3\frac{45}{63}) \times 2^{\frac{105-50}{10}} = 87794\text{h} \approx 10\text{yrs} \quad \textbf{(3.5)}$$

So the expected life of this capacitors is greater than 10 tears however, this value is calculated based on the worst case conditions. Since the micro-inverter works only during the day and its voltage and ripple current are not maximum, the actual life of the capacitors will be much higher than this value.

### 3.1.2 Primary and snubber MOSFETs

The selection of active switches for the IFMI is a trade-off between cost, effective $R_{ds(on)}$, drain-source breakdown voltage and switching speed. In micro-inverter application, the major weight for selecting the components should be loss reduction; as a result, a higher weight should be given to the lower $R_{ds(on)}$ and also lower turn-off time of the MOSFETs.

During the DCM operation of IFMI, the snubber circuit is not operating and as a result, the turn-off loss of MOSFETs are high. Also, during the BCM operation, it is important to turn off the MOSFETs as fast as possible to minimize the turn off loss.

The turn-off time of the MOSFET is affected by its total gate charge and also the current sink capability of the gate driver, but due to design constraints, MOSFETs with lower gate charge usually have a higher $R_{ds(on)}$. So, in order to overcome with this problem, it is proposed to use multiple MOSFETs with low gate charge in parallel.

According to simulations and also design constraints, the maximum voltage overshoot on the MOSFETs is below 120V so at least a 150V MOSFET is needed in this design.

By comparing numerous MOSFETs through the vendor's website (DigiKey and Mouser) the best choice is "BSC190N15NS3 G" from Infineon. This device features an excellent gate charge × $R_{ds(on)}$ product (figure of merit), very low $R_{ds(on)}$ and high operation temperature. The on state resistance of this MOSFET is $R_{ds(on)} = 19\ m\Omega$ so in order to achieve lower losses, two parallel MOSFETs are used in each IFMI phase.

The specifications for the snubber switch in this application are not very high and this is an advantage of this design compared to IFMI designs with active clamp. The MOSFET in the proposed adaptive snubber switches with double-line frequency and it only conducts during the turn-off transient of the main switch in the BCM operation. As a result, a small MOSFET with the same voltage rating as the main switch is required for the snubber switch.

The main criteria for selecting the snubber switch is the breakdown voltage and form factor. The selected MOSFET for this application is "IPD320N20N3 G" from Infineon.

### 3.1.3 Flyback transformer core type and material

As it is demonstrated later in this chapter, the flyback transformer is the biggest source of power loss in the IFMI. As a result, the overall efficiency of the system highly depends on the selection of this component.

A variety of parameters should be taken into account when selecting the core shape, size and material. Also, a trade off should be made in selecting the effective switching frequency of the converter as higher switching frequency helps reducing the core loss (in some occasions) and shrinking the core size and at the same time increases the switching and MOSFET driver loss.

In the IFMI design, the compactness and the leakage of the flyback transformer is of great importance, so the RM shape is selected for this application. The RM core is not as optimized as pot cores in terms of the leakage but they have a more compact design and allow us to have a higher power density for the IFMI.

In order to choose the core material the most important factor is the operating frequency range of the IFMI. The operating frequency is also a function of the target efficiency and size and volume of the converter. Later in this chapter, we will demonstrate that the optimum frequency of the converter is between 100 kHz to 300 kHz. For this operating range, there are several ferrite materials that can be used including: N87, N88, N95, N96, N97 and PC47 all from EPCOS. It is also worth mentioning that there are other materials available from other manufacturers but they all have the same properties as the cores listed here and they can be replaced by EPCOS materials using the ferrite materials cross reference table. Other requirements for the core material for the IFMI application include:

- Low power loss at high temperatures
- Very High saturation with low dependence on temperature

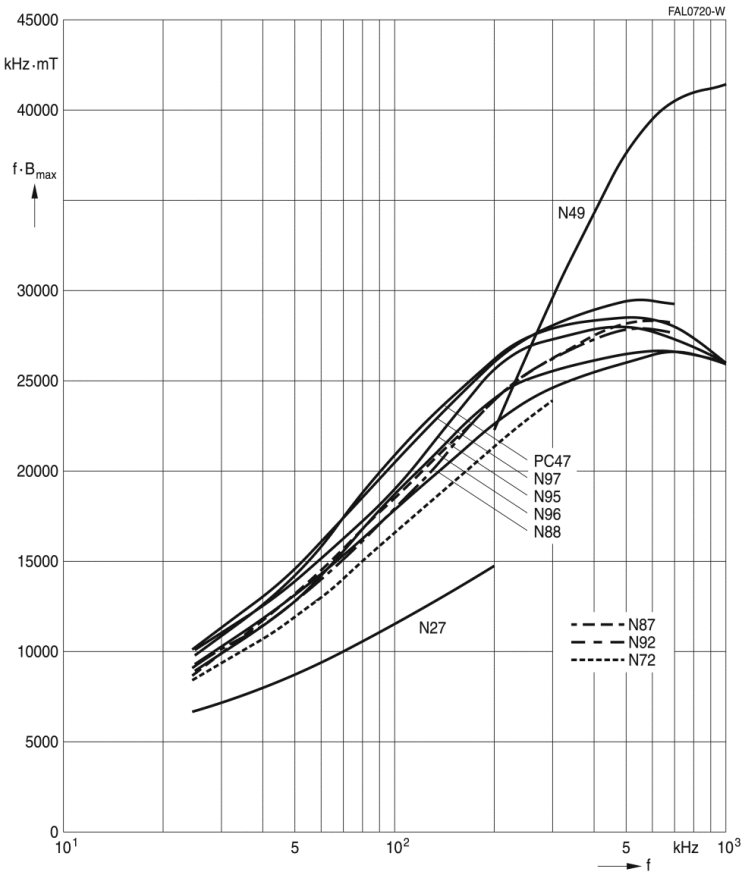


**Fig. 3.1: Performance factor versus frequency for EPCOS core materials measured at $T$=100˚C and $P_v$ = 300kW/m$^3$**

- Gapped core

Another restriction that limits the capabilities of the designer in terms of selecting the core material and shape is the availability of the specific cores. As we previously mentioned, due to a better form factor and reduced leakage, RM core is the most suitable off-the-shelf core shape for IFMI application. The RM cores are only available in N87, N95 and N97 materials, so we only consider these materials here.

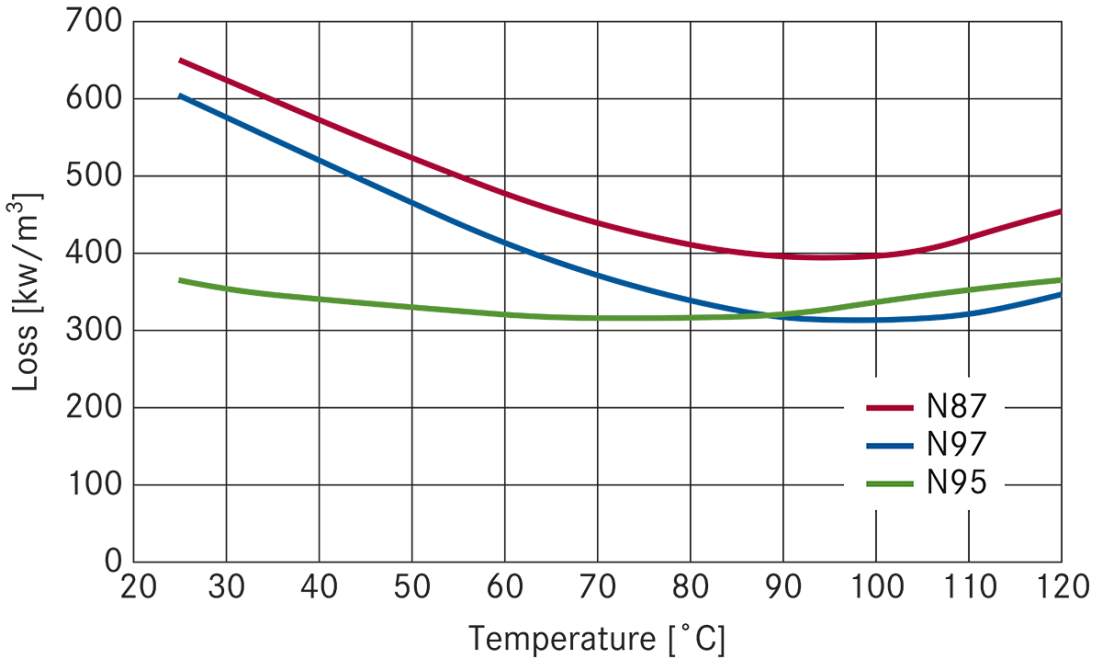


**Fig. 3.2: comparison of power loss in three different core materials**

Fig. 3.1 illustrates the performance factor of different core materials at 100˚C. The ferrite material performance factor is the product of $B_{max}$×f (maximum flux × frequency) at some pre-defined core loss density and temperature. From the performance factor of Fig. 3.1, we can deduce that at 100˚C all these materials have good performance and N97 outperforms the others. However, at lower temperatures, as it is demonstrated in Fig. 3.2, the N95 material has lower loss compared to the others. Also, the flat temperature profile of the N95 material helps reducing the core loss at lower output powers, where the core temperature is also lower and as a result achieves higher CEC efficiency. So, the N95 material is the best choice for this application. However, for the selected core shape of RM14, the N95 material was not available and as a result, we use the N97 material instead.

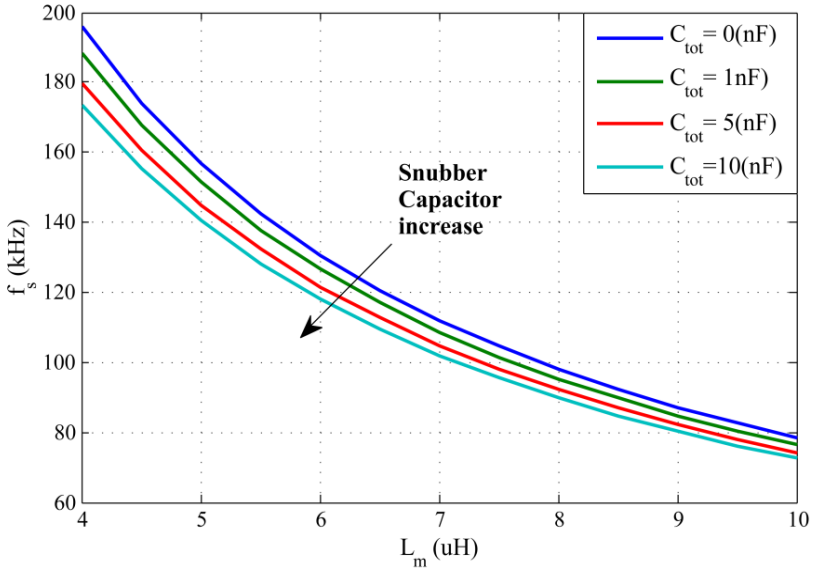


**Fig. 3.3: Minimum value of switching frequency in BCM versus magnetizing inductance for maximum power of 250 W in a 240V system.**

### 3.1.4 Magnetizing inductance value

The value of magnetizing inductance $L_m$ is an important parameter in the BCM due to the direct relationship to the switching frequency. In this PV micro-inverter application, the switching frequency becomes the lowest value near the peak grid voltage. Therefore, the lowest switching frequency can be determined in that point. From the previous mode analysis, the switching frequency can be approximately obtained as:

$$f_s = \frac{1}{T_s} \approx \frac{1}{t_{01} + t_{12} + t_{23} + T_d} \tag{3.6}$$

Fig. 3.3 shows the lowest switching frequency according to the snubber capacitance by using **(3.6)** where the leakage inductance is assumed to be 1% of the magnetizing inductance. Compared to the ideal case of $C_{tot}$ =0$nF$, the actual switching frequency decreases due to the additional resonant period of Mode 2 and Mode 4. Here, the

magnetizing inductance is selected as 6μH considering some margins based on the lowest switching frequency of 100 kHz since the actual power conversion loss requires a little higher reference current compared to the ideal case.

### 3.1.5 Snubber capacitor $C_s$

The value of snubber capacitor $C_s$ is selected to minimize the spike voltage across the main switch during Mode 3. Although a relatively large snubber capacitor can effectively reduce the spike voltage, it increases the duration of oscillations during the turn off process which results in low overall efficiency. Large snubber capacitor also increases the resonant time of Mode 4 ($t_{QR}$) which can result in lower switching frequency and higher output current THD. Furthermore, it causes high cost and bulky volume so it should be appropriately restricted to the lowest possible value. The peak voltage across the main switch $S$ is calculated as [36]:

$$v_{ds\_peak} = v_{in} + \frac{v_o}{N} + v_{spike}$$
$$v_{spike} = i_{Lm\_peak}\sqrt{\frac{L_{lk}}{C_{tot}}} \quad \textbf{(3.7)}$$

Where $v_{spike}$ is the spike voltage caused by the resonance of $L_{lk}$ and $C_{tot}$, and $i_{Lm\_peak}$ is the peak magnetizing inductance current.

Fig. 3.4 shows the peak voltage across the main switch according to the leakage inductance by using (3.7) with $P_o$=*250W*, $v_{in}$=30.6*V*, $v_o$=240$V_{rms}$, $N$=6, and $L_m$=6$\mu H$. Fig. Fig. 3.4 shows the relationship between $v_{ds\_peak}$ and $C_{tot}$ with the fixed grid angle (=π/2 rad) and Fig. 3.5 shows the relationship between $v_{ds\_peak}$ and grid angle with the fixed $C_{tot}$ =10$nF$. The

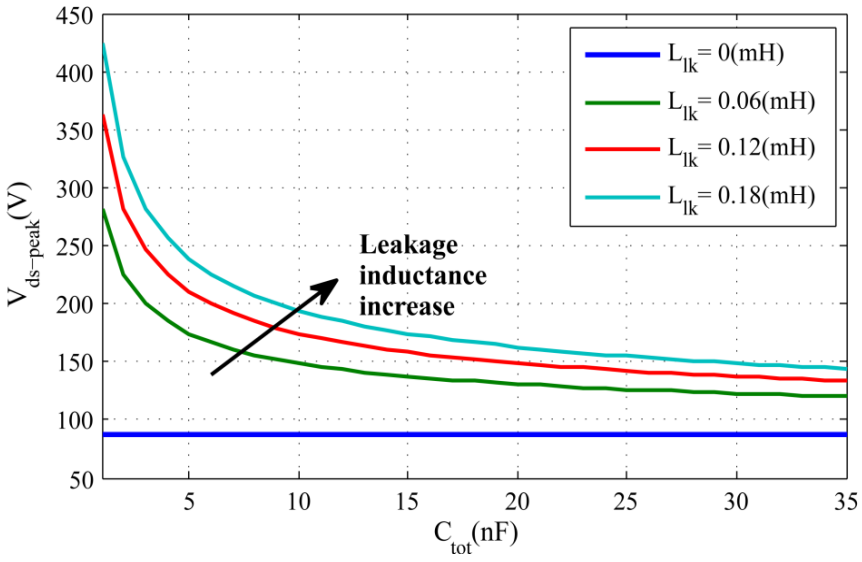


**Fig. 3.4: Peak voltage across the main switch for different leakage inductance values at grid angle = $\pi/2$ and for $P_o$ =250 W, $v_{in}$ =30.6 V, $v_o$ =240 $V_{rms}$, $N$ =6, and $L_m$ =6 uH.**

solid blue line in Fig. 3.4 and Fig. 3.5 shows the ideal case corresponding to the zero leakage inductance. However, as shown in Fig. 3.4 the peak voltage is not only proportional to the leakage inductance but also extremely increased with only a few percent leakage inductances in case of small snubber capacitance. Therefore, based on the leakage inductance of the designed transformer, the relevant snubber capacitance can be selected by Fig. 3.4. For example, if the leakage inductance is assumed to be 0.06µH corresponding to the 1% magnetizing inductance, it requires at least 10$nF$ of $C_{tot}$ to maintain $v_{ds\_peak}$ below 150 V.

In order to select the proper value for the snubber capacitor it is important to calculate the required $C_{tot}$ based on (3.7). However, it should be considered that since the required capacitance is usually in order of nano-Farads, the stray capacitances of a real hardware can be exploited to further reduce the value of the snubber capacitor. Specifically, as it is mentioned in [36] and [47], the capacitance of the primary winding of transformer and also

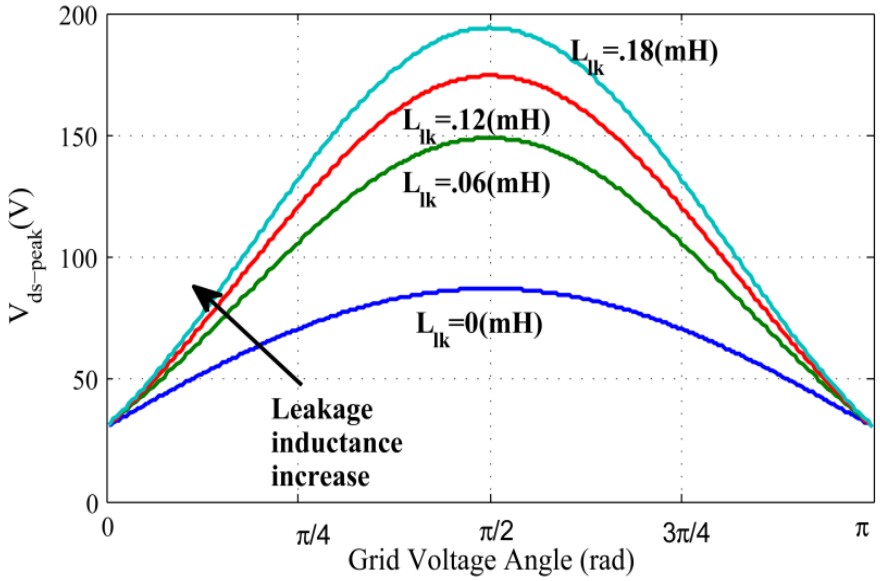


**Fig. 3.5: Peak voltage across the main switch for $C_{tot}$ = 10 (nF).and for $P_o$ =250 W, $v_{in}$ =30.6 V, $v_o$ =240 $V_{rms}$, $N$ =6, and $L_m$ =6 uH.**

the reflected anode-cathode capacitance of the secondary rectifier are effectively in parallel with $C_{oss}$ during the switching transients, so, the most suitable equation for calculating the required snubber capacitance can be deduced as:

$$v_{spike} = i_{Lm\_peak}\sqrt{\frac{L_{Lk}}{C_{oss}\left\|C_s\right\|C_{pw}\left\|N^2 C_D\right.}} \qquad \textbf{(3.8)}$$

Where $C_{pw}$ is the primary winding capacitance of the flyback transformer and $C_D$ is the anode-cathode capacitance of the secondary rectifier. This equation is derived from the equivalent circuit of the flyback converter during the turn off resonant period which is shown in Fig. 3.6.

Another important property of a real hardware that can be exploited to reduce the required snubber capacitance is the non-linearity of a MOSFET's $C_{oss}$. The value of $C_{oss}$ at

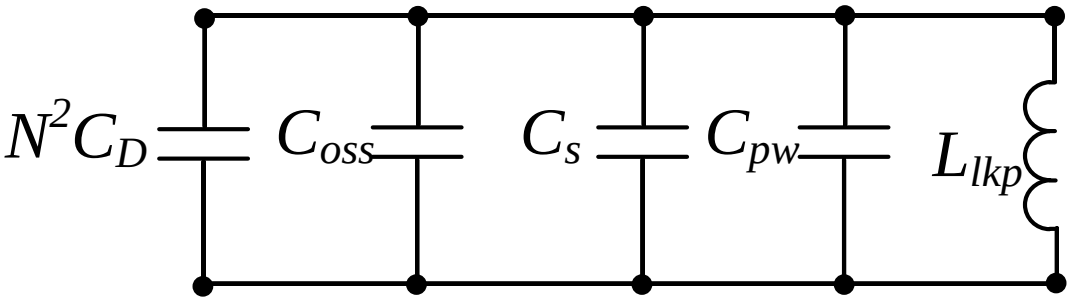


**Fig. 3.6: Equivalent circuit of the flyback converter during the turn off resonant period.**

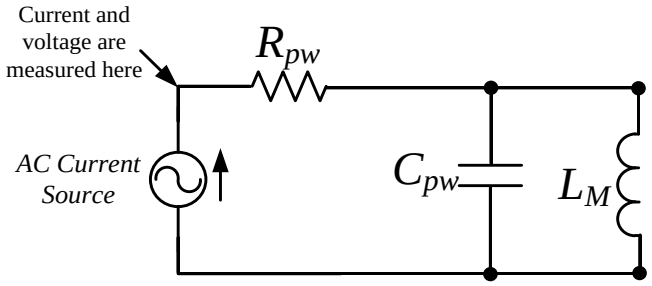


**Fig. 3.7: Equivalent circuit of the impedance measurement test setup.**

low voltages can be more than 10 time higher than its value in higher voltages which further helps to damp the voltage overshoot and reduce the value of required snubber capacitor.

As we can see in (3.8), the values of the secondary rectifier capacitance and also the primary winding capacitance have a great impact in the value of the required snubber capacitor. The secondary rectifier output capacitance can be extracted from its datasheet, so, in order to have an idea of how large the primary winding capacitance is, we measured this capacitance using a custom made impedance measurement setup which is basically a high frequency high power amplifier. The equivalent circuit for this setup is illustrated in Fig. 3.7. This high frequency amplifier uses a MOSFET operating in the active region to drive a 1A current with controllable frequency through the primary of the transformer and then voltage

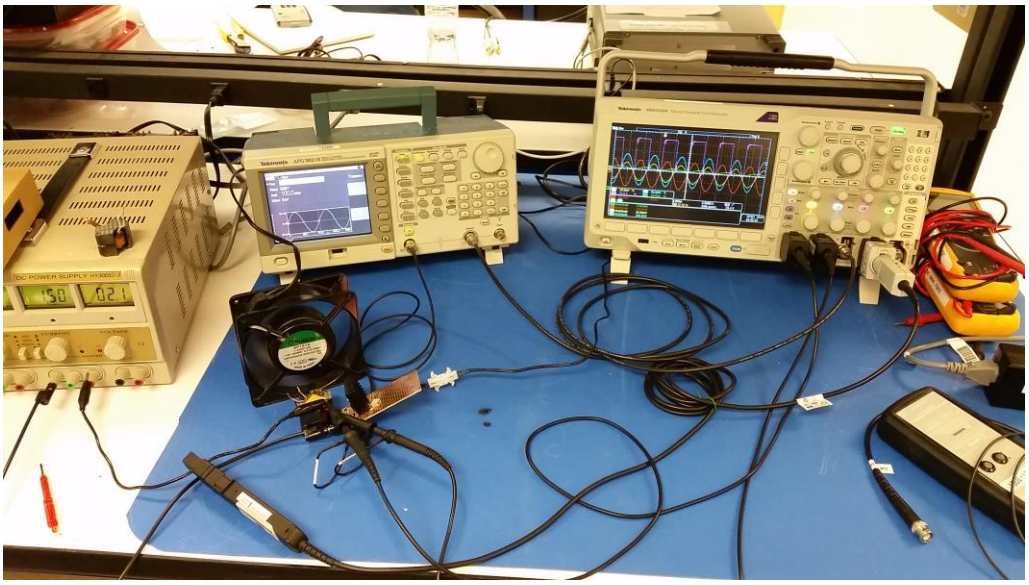

**Fig. 3.8: picture of the hardware setup for measuring the impedance of the transformer primary**

and current probes are used to read the RMS value of the voltage at the primary of the transformer and also the current through the primary and deduce the equivalent impedance of the primary at different frequencies.

Fig. 3.9 shows the experimental data extracted from the transformer. Based on these data, the resonant frequency of the parallel LC network of the primary leakage inductance and the primary winding capacitance is around 1.5 MHz, as a result, the value of the primary winding capacitance can be deduced as:

$$\omega = \frac{1}{\sqrt{LC}} \Rightarrow C = \frac{1}{\omega^2 L} = \frac{1}{(2\pi \times 1.5 \times 10^6)^2 \times (6 \times 10^{-6})} = 1.88\ nF \qquad \textbf{(3.9)}$$

We can see here that this capacitance is not small compared to the required snubber capacitor and as a result has a great importance in calculating the snubber capacitor according to (3.8).

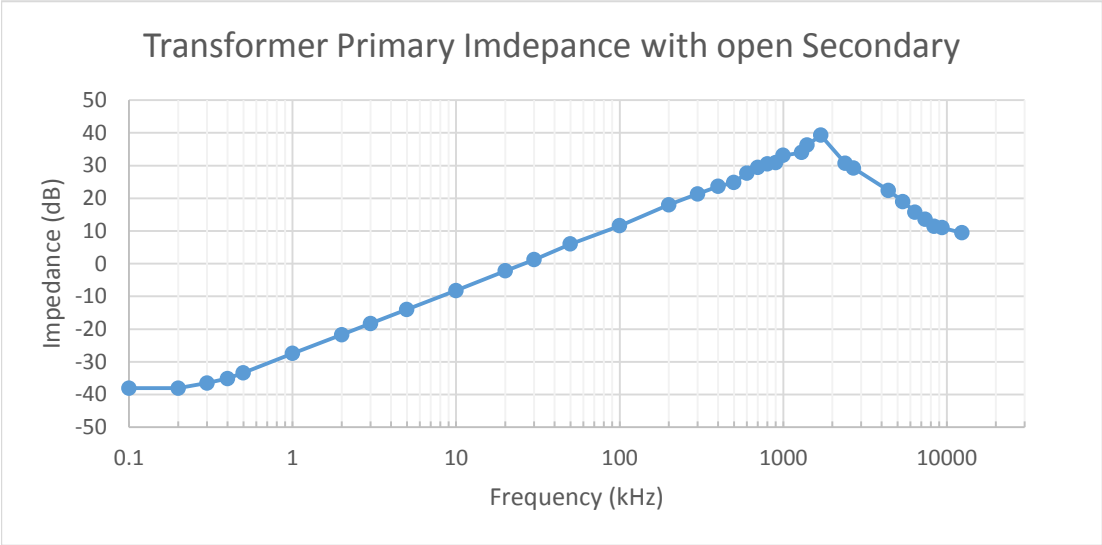


**Fig. 3.9: Measured frequency response of the transformer's primary winding.**

### 3.1.6 Auxiliary switch

The current rating of the auxiliary switch $S_a$ is small because it only has to handle the high frequency resonant current during Mode 2, Mode 3, and Mode 4. Furthermore, the switching frequency is quite low so the switching loss can be ignored. Therefore, a very slow MOSFET with low $R_{ds(on)}$ can be used. The operation of the auxiliary switch can be determined by the operational mode. During the BCM operation, the turn-on of the $S_a$ does not cause extra turn-on switching loss of the main switch in the range of (2.6) due to the natural ZVS operation. Although, the perfect ZVS operation is not achieved any more in the other range, the turn-on switching loss of the main switch is not much increased due to the quasi-resonant switching. However, during the DCM operation, the turn-off switching loss of the main switch is not only small even without snubber but also the effect of the snubber is cancelled out by the more capacitive energy dissipation at turn-on. As a result, the switching

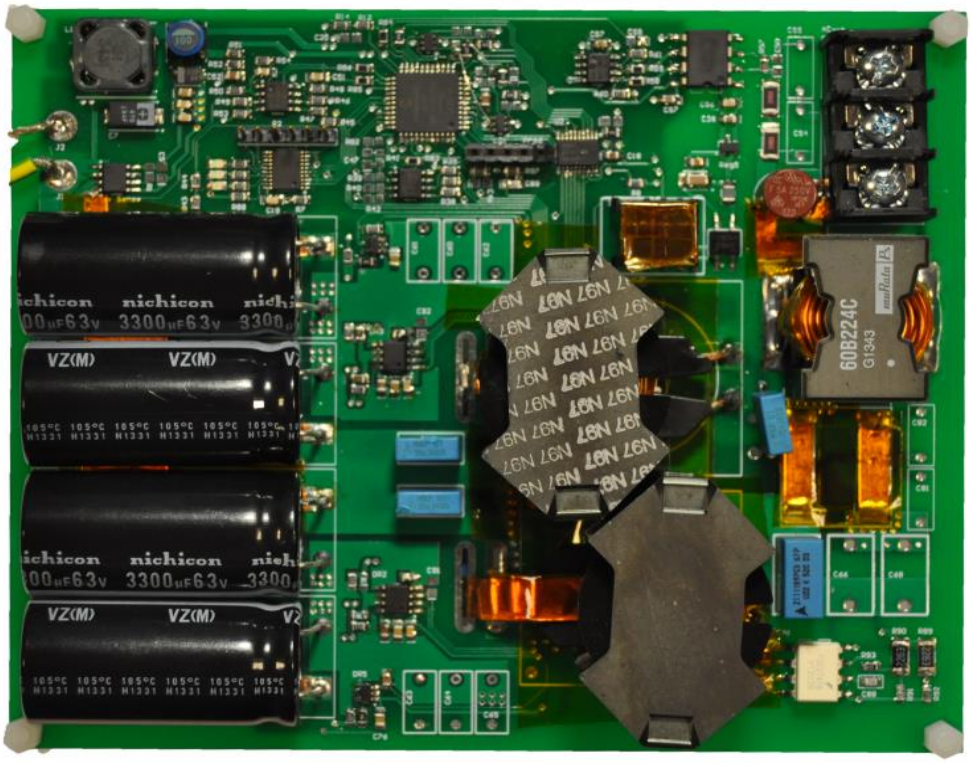


**Fig. 3.10: Photograph of the experimental prototype.**

of the $S_a$ can be implemented based on the operational mode. However, it should be noticed that the voltage across the main switch should be maintained below the designed value even without the snubber capacitor.

## 3.2 Experimental Results

In order to verify the effectiveness of the proposed adaptive snubber, a 250W flyback micro-inverter prototype has been built as shown in Fig. 3.10. The interleaved flyback topology is chosen in order to lower the current stress on the transformer and silicon devices and also to increase the efficiency and reduce the size of the magnetic components. Also, with the ripple current cancelling of the interleaved flyback topology, the ripple current RMS

**Table 3.1: Specifications and ratings of the experimental setup**

| SYSTEM SPECIFICATIONS | | |
|---|---|---|
| Output Power ($P_o$) | | 250 W |
| Input Voltage ($v_{in}$) | | 24 ~ 35 V |
| Grid Voltage ($v_g$) | | 240 Vrms |
| Grid Frequency ($f_g$) | | 60 Hz |
| Switching Frequency ($f_s$) | DCM | 100 kHz |
| | BCM | 100 ~ 300 kHz |

of the filter capacitors is reduced so smaller capacitors can be selected for the primary and secondary high frequency current filtering which leads to smaller volume, lower cost and higher efficiency.

Table 3.1 and Table 3.2 show the system specifications and the major component list used in the hardware, respectively. Based on (3.8) and the measured values of $C_{pw}$*=1.88nF*, $C_D$*=35pF*, $C_{oss\text{-}20V}$=3.8nF (*accumulative* $C_{oss}$ of two parallel MOSFETs at 20V) and the maximum overshoot of 130V on the MOSFETs, the final snubber capacitance was selected as *1.68nF*.

The overall control schemes were implemented based on dsPIC microcontroller *dsPIC33FJ16GS504* as shown in Fig. 3.11. This micro controller has all the necessary functionalities for controlling the IFMI including: four analog comparators, four Digital to Analog Converters (DACs), high speed PWM controller with 1.04ns resolution, current reset functionality in PWM module for variable frequency control in BCM mode and also high speed Analog to Digital Converters (ADC). The choice of this low cost microcontroller also helps reducing the overall cost of the system.

**Table 3.2: list of major components in the hardware setup.**

MAJOR COMPONENT LIST

| | | |
|---|---|---|
| Main Switch ($S_1$, $S_2$) | | BSC190N15NS3 × 2 |
| Output Diode ($D_1$, $D_2$) | | IDB06S60C |
| Auxiliary Switch ($S_{a1}$, $S_{a2}$) | | IPD320N20N3G |
| Unfolding Bridge Switch ($S_3$ – $S_6$) | | TK39J60W5 |
| Transformer ($TR_1$, $TR_2$) | Core Type | RM14 – N97 |
| | Turns Ratio ($N$) | 6 |
| | Magnetizing Inductance ($L_{m1}$, $L_{m2}$) | 6.15$\mu$H, 6.18$\mu$H |
| | Leakage Inductance ($L_{lk1}$, $L_{lk2}$) | 0.033$\mu$H, .037$\mu$H |
| Snubber Capacitor ($C_s$) | | 1.68 nF |
| Output Filter | Inductor ($L_f$) | 220 $\mu$H |
| | Capacitor ($C_f$) | 220 nF |

During the DCM and BCM operation, the turn-off timings of the main switches are determined by comparing the reference current with the instantaneous current of the primary side of each transformer. The constant frequency operation determines the turn-on timings of the switches in the DCM. However, in BCM, the turn-on timing of the main switch $S_1$ is determined by detecting zero voltage across $v_{ds1}$, instead of sensing the output diode current, and the turn-on timing of the main switch $S_2$ is synchronized to the turn-off timing of $S_1$ for simple interleaved operation. This scheme helps eliminating the use of current transformer on the secondary side of the flyback transformer, reducing the overall cost of the system.

The experimental results of the micro-inverter with the proposed adaptive snubber and without considering the MPPT [48], [49] operation are presented in Fig. 3.12 through

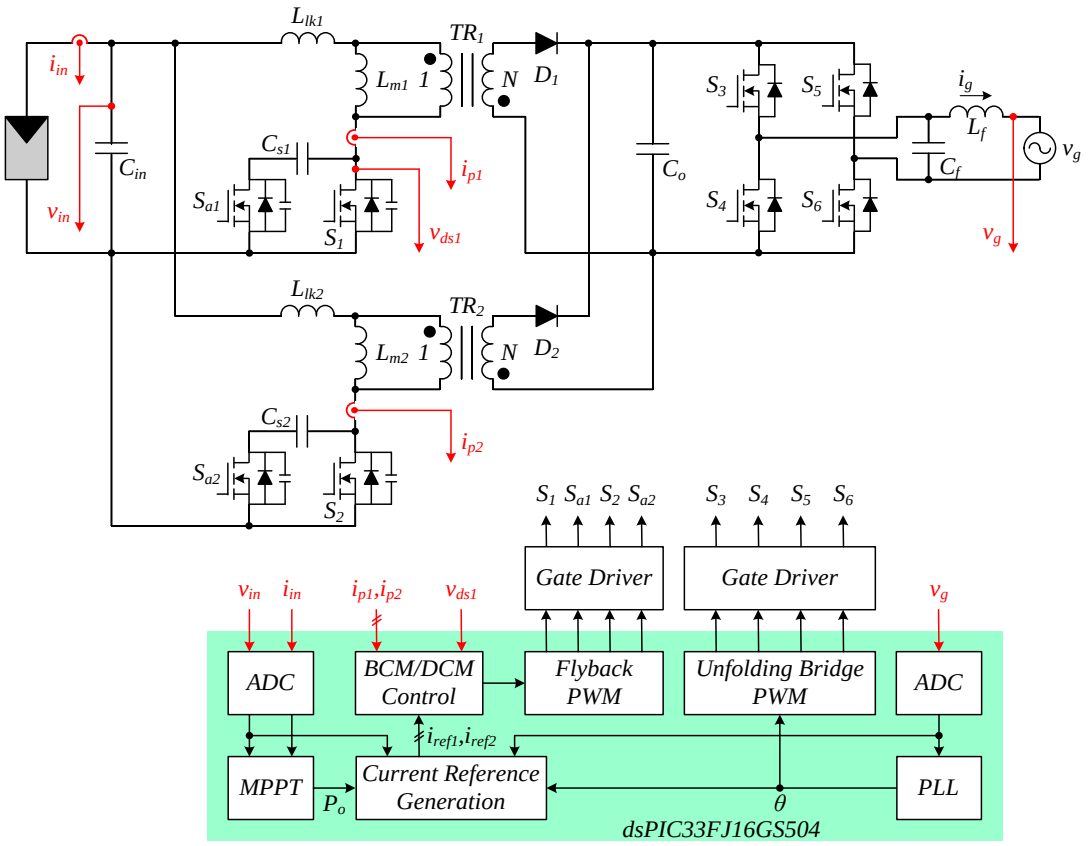


**Fig. 3.11: control block diagram of the flyback micro-inverter.**

Fig. 3.17 for the output power of 210W which corresponds to the maximum efficiency of the converter.

Fig. 3.12 and Fig. 3.13 show the overall operational waveforms across the grid cycle. The grid current is synchronized with the grid voltage by Phase-Locked Loop (PLL). The auxiliary switch $S_{a1}$ gating signal in Fig. 3.13 illustrates the 120Hz operation of this switch and also the DCM-BCM mode transition during the operation of the converter.

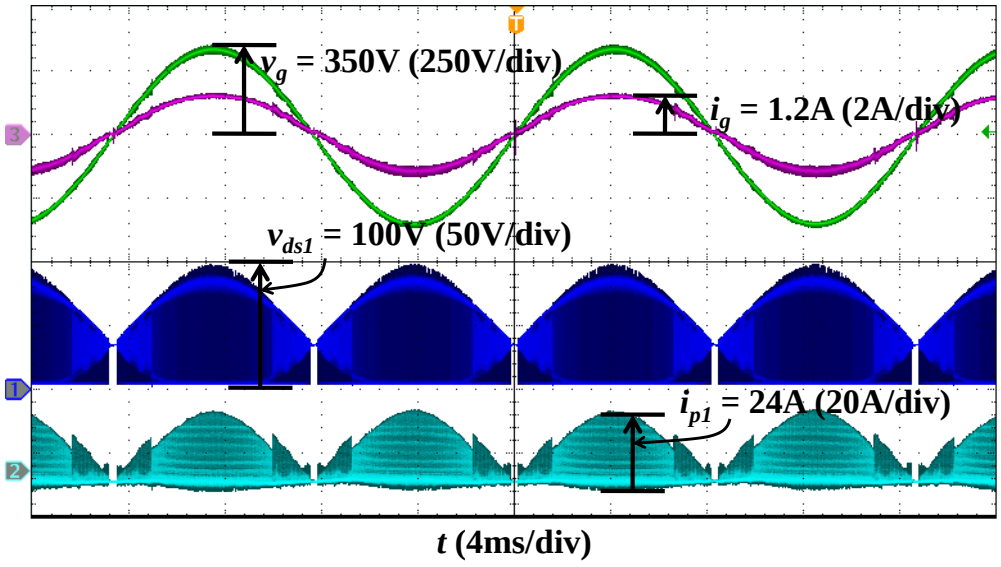


**Fig. 3.12: Experimental waveforms of grid voltage $v_g$, grid current $i_g$, gate-to-source voltage of the main switch $S_1$, and gate-to-source voltage of the auxiliary switch $S_{a1}$.**

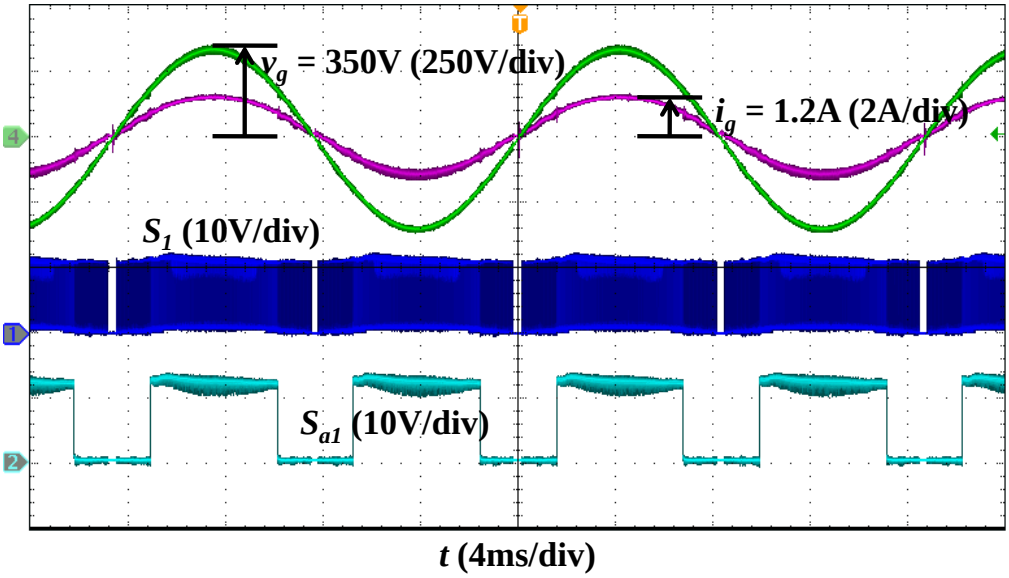


**Fig. 3.13: experimental waveforms of grid voltage $v_g$, grid current $i_g$, drain-to-source voltage of $S_1$ $v_{ds1}$, and primary side current of the transformer $i_{p1}$.**

Fig. 3.14 illustrates the interleaved operation of the converter in the BCM. It is shown in this figure that the turn-on timing of the main switch $S_2$ is synchronized with the turn-off timing of the main switch $S_1$.

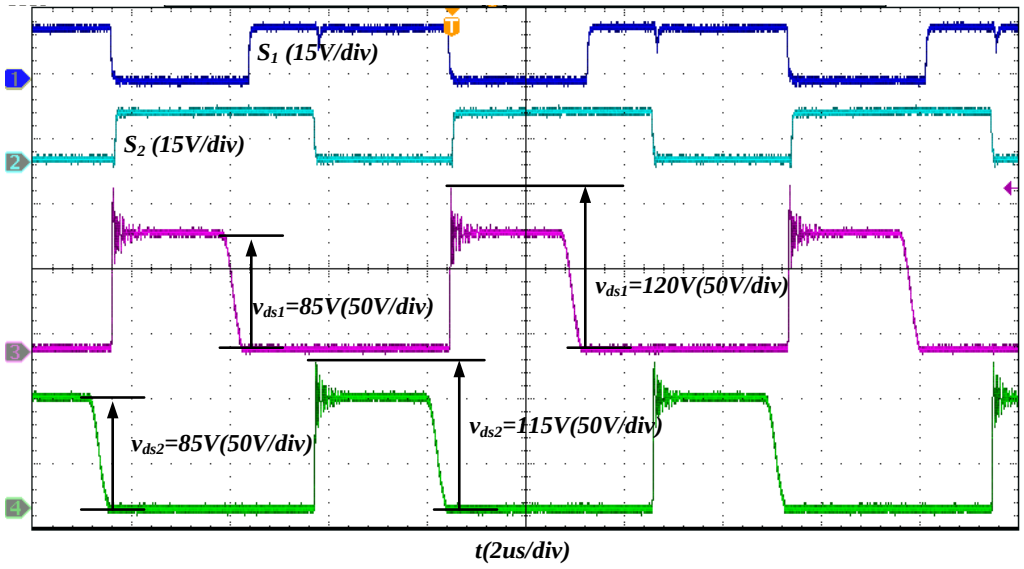


**Fig. 3.14L Interleaved operation during BCM.**

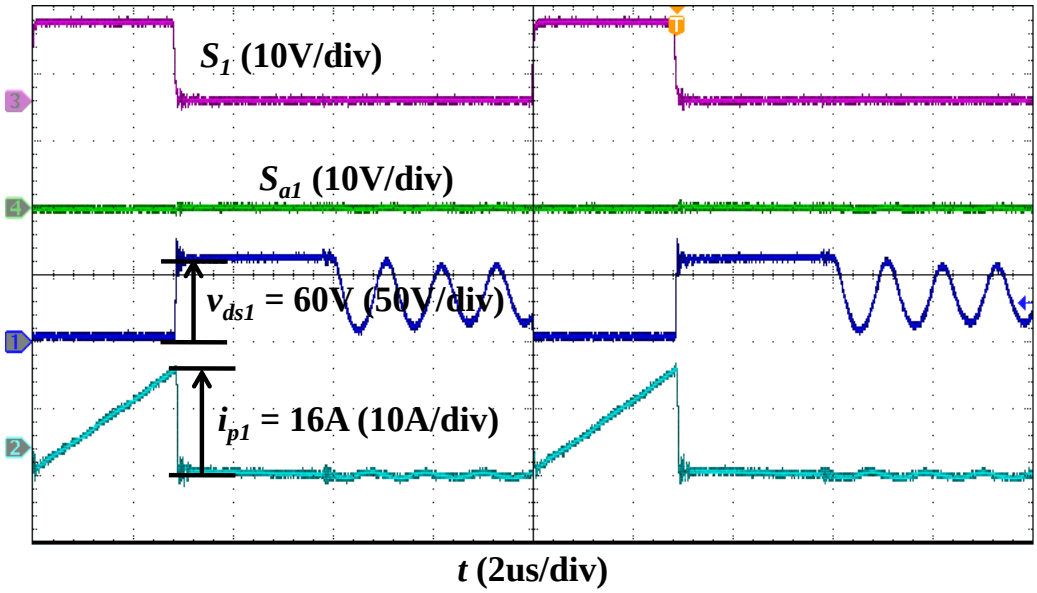


**Fig. 3.15: Operation Waveforms in BCM.**

Fig. 3.15 and Fig. 3.16 show the detailed waveforms in each operation mode. Fig. 3.15 and Fig. 3.16 show the DCM and the BCM operation, respectively. In DCM, the

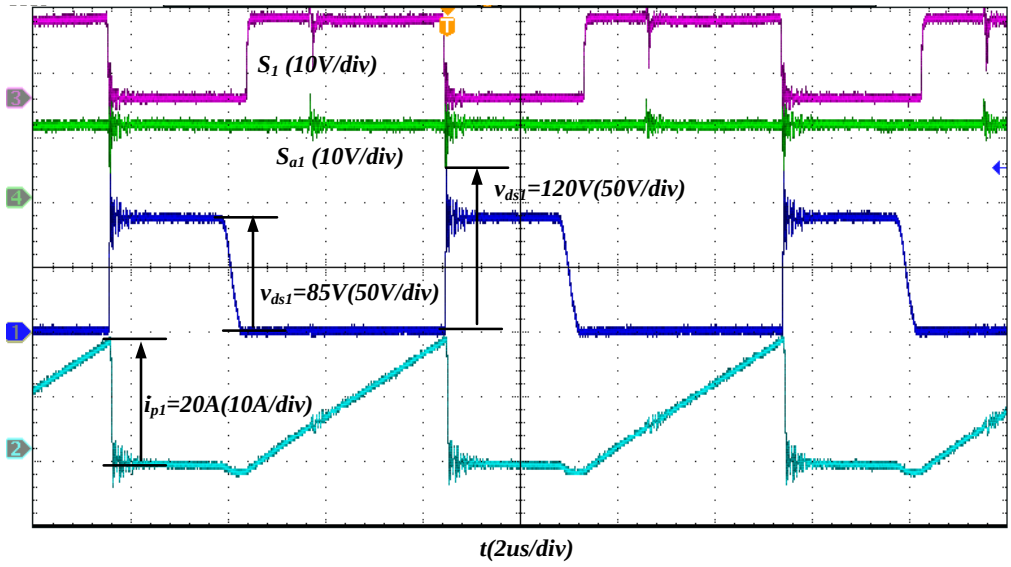


**Fig. 3.16: Operation waveforms in BCM.**

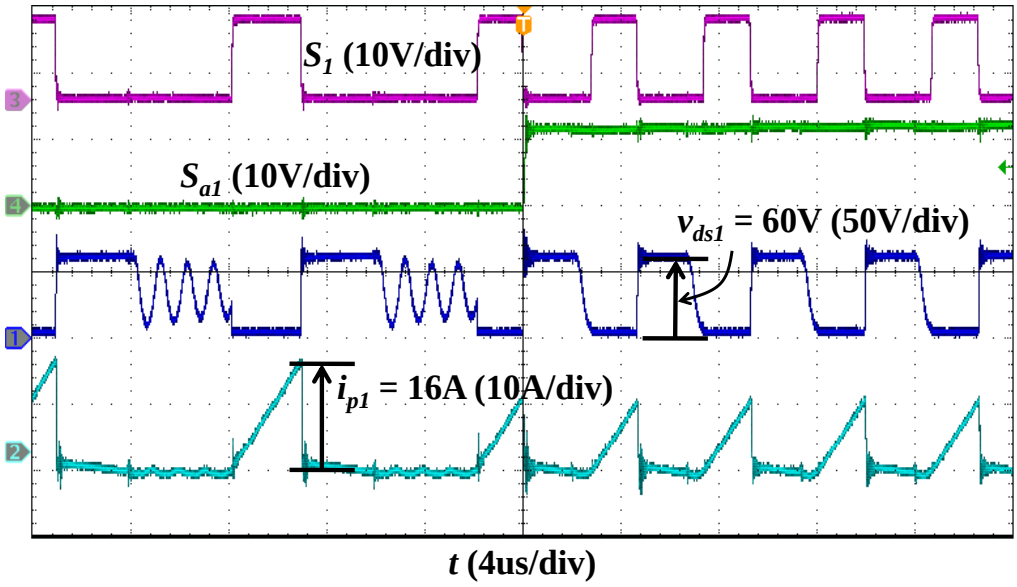


**Fig. 3.17: Operation waveform during mode transition between DCM and BCM.**

auxiliary switch $S_{a1}$ is turned off, switch $S_1$ is hard switched. However, in BCM, the auxiliary switch $S_{a1}$ is turned on so that the snubber capacitor helps to decrease the overshoot of the

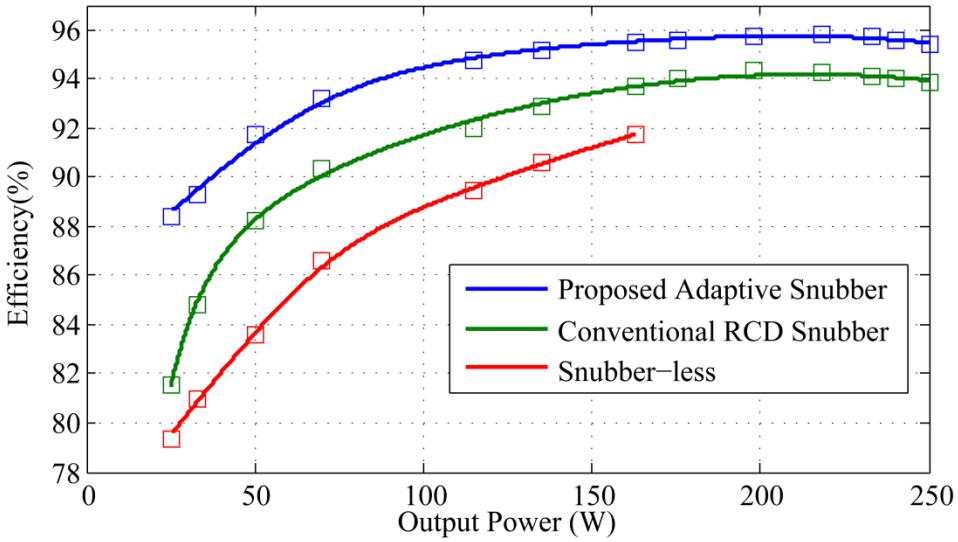


**Fig. 3.18: Efficiency curve.**

voltage $v_{ds1}$ as well as the turn-off switching loss by slow rising slope of the voltage $v_{ds1}$. Also, the capacitance energy is fully transferred to the input source by resonance with the magnetizing inductance before the next turn-on of the main switch $S_1$, so it does not cause any additional loss. Fig. 3.17 shows the mode transition waveform from DCM to BCM.

The efficiency of the prototype from the input port to the output port (including the micro-processor and driving power) was measured as shown in Fig. 3.18. The maximum efficiency is 95.8% and the CEC weighted efficiency is 94.6%.

The efficiency of the converter is also measured using a conventional RCD snubber ($C_{snub}$=*1.68nF* and $R_{snub}$ = *4.3kΩ)* and it is shown in Fig. 15. The maximum achieved efficiency in this case is 94.4% with the CEC efficiency of 92.6%.

The operation of the flyback micro-inverter without any type of snubber or clamp circuit is evaluated and the resulted efficiency is demonstrated in Fig. 3.18. It should be

mentioned that without snubber, the operation of the inverter was only possible up to 65% of the nominal power (160W) as the maximum voltage overshoot reached the break down voltage of the MOSFETs.

# 4. Optimization

## 4.1 Introduction to the optimization process for the IFMI

The IFMI system (including hardware and control software) is a relatively complex system with many variables that can be optimized. Out of all the variables that are available for optimization in the system, in the previous chapter we only optimized for the core shape, turns ratio and the magnetizing inductance and the maximum efficiency that was achieved was by far the best in the technical literature and was on-par with the available commercial micro-inverters.

Optimizing a PV inverter system based on only a single operating point is not a realistic practice. A solar inverter system has to process a very wide range of PV output power through the day, from extremely low power all the way up to the full power. It is virtually impossible for a PV inverter to maintain its maximum efficiency throughout the full output power range, so, the efficiency of the inverter system has to be optimized based on the entire power range. I order to do that; researchers and manufacturers consider a performance factor called the Weighted Efficiency.

Weighted efficiency is basically an average efficiency by considering a specific weighting factor for each power level and is a better representation of the inverter's operating profile. There are two mainly used weighed efficiency functions, the American weighted

efficiency or $\eta_{CEC}$ and the European weighted efficiency or $\eta_{EU}$. The averaging formula for calculating the $\eta_{CEC}$ and $\eta_{EU}$ are shown in and respectively.

$$\eta_{CEC} = .04 \times eff_{10\%} + .05 \times eff_{20\%} + .12 \times eff_{30\%} + .21 \times eff_{50\%} + .53 \times eff_{75\%} + .05 \times eff_{100\%} \quad (4.1)$$

$$\eta_{EU} = .03 \times eff_{5\%} + .06 \times eff_{10\%} + .13 \times eff_{20\%} + .1 \times eff_{30\%} + .48 \times eff_{50\%} + .2 \times eff_{100\%} \quad (4.2)$$

The basic aim of this chapter is to establish a methodology based on the weighted efficiency optimization to accurately design all the parameters of the IFMI topology and the control system. This task requires inverter loss calculation at different power levels. However, power losses depend on many parameters that correlate directly to the topology components as well as various operational variables, so, in order to establish the optimization algorithm, it is necessary to clearly define the design parameters and the dependent variables.

Every component and variable in the IFMI system, including all the active and passive components, can be considered as a design variable, but, by having a fair understanding of the system operation, we can pre-determine some of these design parameters and make the optimization a more straightforward task. A detailed description of the selected design variables and defined parameters will be introduced later in this chapter.

In addition to pre-defining some of the variables for the optimization procedure, defining an accurate loss model for each and every component of the system is another important step that has to be done before starting the optimization process. In the following sub-chapter, we introduce the best available methods for calculating the loss of the components in the IFMI system and we introduce a proper way to model these losses in the MATLAB environment.

## 4.2 IFMI loss modeling in MATLAB

As it is mentioned before, it is critical to have an accurate loss model for the system components in order to be able to perform a meaningful optimization.

Unlike a dc-dc converter where system variables, including voltages and currents, are constant, the IFMI system tracks a rectified sinusoidal waveform, namely the rectified grid voltage. As a result, it is crucial to calculate the losses for a full operation cycle (half of grid cycle) and average it throughout the cycle. There are two possible methods that can be used to perform this task. One is to calculate the average and RMS values of the system variables including voltages and currents throughout the operation cycle and use these values to estimate the losses [37]. The other method is to calculate the losses for each switching cycle independently and then add them together to calculate the average loss. The benefit of the first method is reduced computational burden and programming simplicity but it lacks accuracy, specially in calculating the magnetic losses. As we know, the magnetic system in ferrites is an extremely non-linear system [50], thus superposition principle cannot be used. The second method however, is computationally demanding as all the system variables should be calculated in a cycle by cycle basis for each switching cycle but it gives us the most accurate prediction of the IFMI system losses. Since we have access to powerfull computer systems, computational burden is not an issue here thus we opt to use the later method in combination with the averaging method in favor of accuracy. The detail are explained I the following.

The most important sources of loss in the IFMI system are the magnetic losses in the ferrite core including the hysteresis and eddy current losses and also the switching loss. These two biggest sources of loss are non-linear as well so we use the cycle by cycle calculation method to evaluate these losses.

The calculation of switching loss is straightforward. Due to operation of the adaptive snubber presented in this thesis, the switching losses are present only in the DCM operation mode. So, the current and voltage of switch is calculated at each switching instance and then the equations presented in [37] are used to calculate the switching loss.

In order to calculated the core loss in a cycle by cycle basis, the method presented in [50] is used which will be elaborated in the following sub-section.

There are other sources of loss present in the IFMI system including

- the micro-processor and gate drive loss that are assumed to be constant
- Conduction loss in the transformer, silicon devices, secondary filter inductor, fuse and PCB. These losses are calculated using their RMS current.
- ESR loss of the primary capacitors which are calculated using their RMS current.
- Leakage inductance losses which are calculated in a cycle by cycle basis.

The following section explains the procedure for calculating the core loss using the modifies Steimentz equation.

### 4.2.1 IFMI transformer loss calculation

An exact prediction of transformer magnetics loss is very critical for the optimization process of the IFMI as the transformer is the source of more than %30 of losses in the IFMI. The conventional way of determining the transformer loss is using the Steinmetz equation. However, this approach does not give us an exact prediction of the losses since this equation is for magnetics under sinusoidal excitation, which is not the case in the flyback transformer.

Several approaches have been introduced in the literature to calculate the magnetic losses under non-sinusoidal excitation. Authors in [51] used the Fourier expansion of an arbitrary waveform in combination with Steinmetz equation to calculate the magnetic losses. However, this superposition method is only valid for linear system whereas the magnetization loss is extremely non-linear so this method is mathematically not feasible.

A novel approach has been presented in [52] which uses the physical understanding taken from dynamic hysteresis models. It has been shown [53] that the macroscopic re-magnetization rate is directly related to the core losses, therefore the empirical loss parameter of frequency (*f*) has to be replaced by physical loss parameter (*dM/dt*) which is proportional to the rate of change of *dB/dt*.

As the first step, the induction change rate *dB/dt* is averaged over a complete re-magnetization cycle, from $B_{max}$ to $B_{min}$ and back:

$$\dot{B} = \frac{1}{\Delta B}\oint \frac{dB}{dt} dB \,, \Delta B = B_{\max} - B_{\min} \tag{4.3}$$

Which can be transformed to:

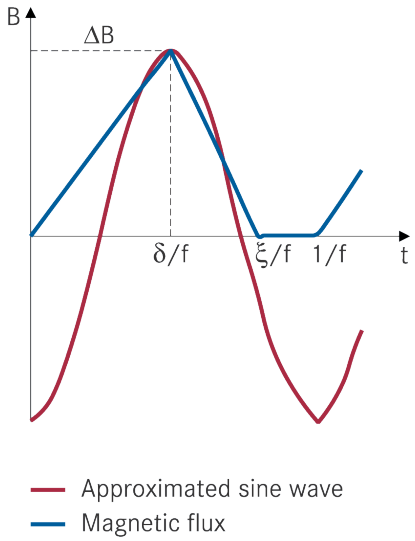


**Fig. 4.1: Magnetic flux of a flyback transformer in the DCM operation.**

$$\dot{B} = \frac{1}{\Delta B}\int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{4.4}$$

The second step consists of finding a relationship between the re-magnetization frequency (*f*) and the average re-magnetization rate $\dot{B}$ . It has been shown in [51] that (4.4) can be normalized with respect to sinusoidal case. From the averaged re-magnetization rate, an equivalent frequency rate $f_{eq}$ can be calculated using the normalized constant $\frac{2}{\Delta B \pi^2}$ .

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2}\int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{4.5}$$

Now, similar to the empirical formula of the Steinmetz, the specific energy loss $w_v$ of every re-magnetization cycle can be determined using this equivalent frequency:

$$w_v = C_m f_{eq}^{\alpha-1} \hat{B}^{\beta}, \hat{B} = \frac{\Delta B}{2} \tag{4.6}$$

This equation can be solved for each switching cycle and then accumulated over the entire grid cycle to calculate the total magnetic loss.

The integration of (4.5) can be calculated using MATLAB in each switching cycle. But, in order to make it easier to compute this integral and reduce the computation time, with the assumption that the converter works in the DCM mode (BCM is special case of DCM) and with reference to Fig. 4.1, we can calculate (4.6) as following:

$$f_{eq} = r \times f_{sw}, r = \frac{2}{\pi^2} \frac{\xi}{\sigma(\zeta - \sigma)} \tag{4.7}$$

Where $f_{sw}$ is the switching frequency of the converter for that specific cycle. By using a combination of (4.6) and (4.7), a very exact estimation of the magnetic power losses can be achieved. We use this estimation in software written in MATLAB to optimize the operation of the converter and increase its maximum and also CEC efficiency.

### 4.2.2 Filter capacitor loss calculation

The input filter capacitor that is used in order to filter the double line frequency harmonic that is present on the DC bus is another important source of loss in the IFMI. Fortunately, this loss can be accurately predicted using the manufacturer provided data in the datasheet. However, optimization can't do anything to reduce this type of loss as it is inherent to the topology of IFMI, no matter what type of control we use. The only thing that can be done is to choose a capacitor(s) that has low ESR.

The input capacitor ESR loss can be calculated using the following set of equations:

$$\Delta V_{dc} = \frac{P_o(\max)}{2\omega V_{dc} C_{dc}} \tag{4.8}$$

$$\Delta I_{dc} = 240\ \pi \times C_{dc} \Delta V_{dc} \tag{4.9}$$

$$P_{loss} = R_{ESR} I^2 = \frac{\tan\ \delta}{240\ \pi C_{dc}} (\Delta I_{dc})^2 \tag{4.10}$$

The above equations have been implemented in the MATLAB program to accurately take into account the losses.

## 4.3 Optimization procedure

The optimization procedure that is used in this thesis, is based on a comprehensive analytical model of the IFMI system with simultaneous consideration of the part-load efficiency is targeted at $\eta_{CEC}$>%94 and ηmax>%96.

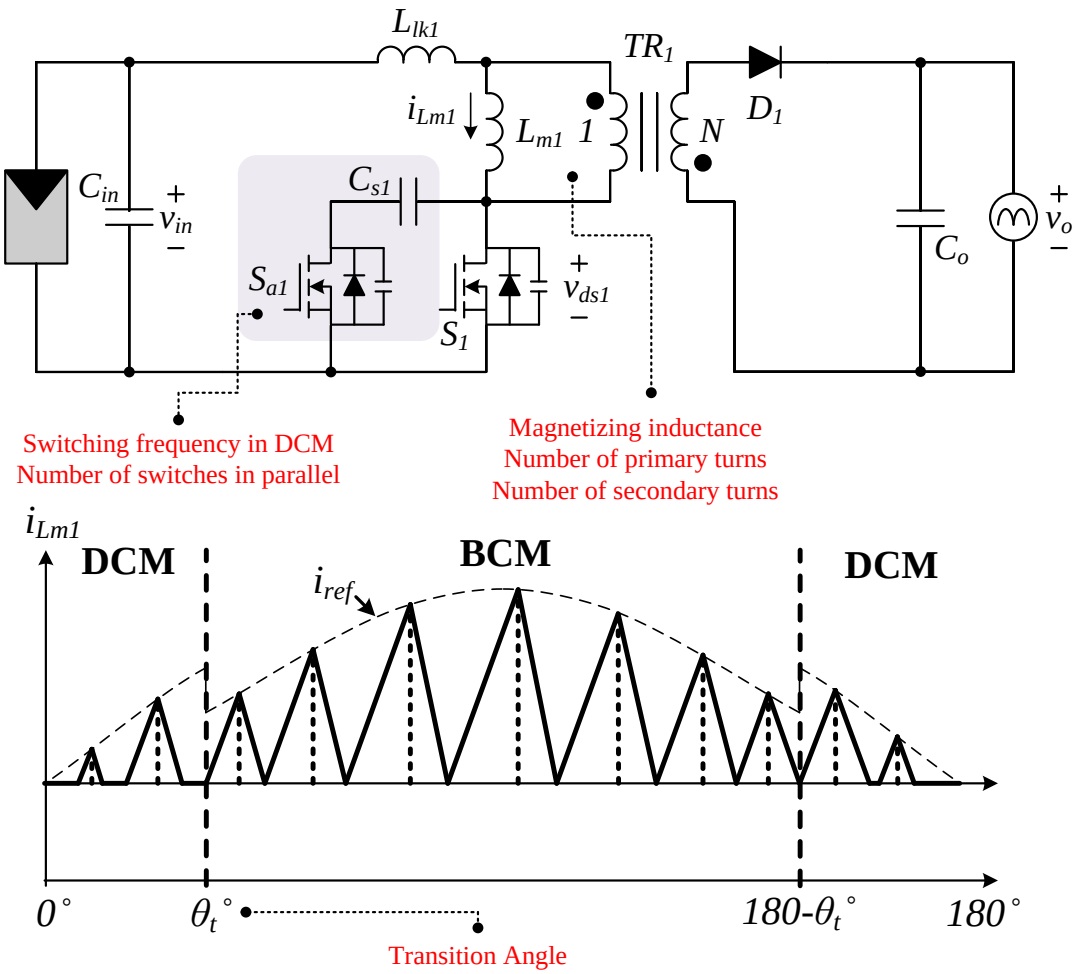


**Fig. 4.2: Schematics of IFMI (one phase) and magnetizing current reference. The free design**

The design of the converter system has many degrees of freedom, even though the topology of the IFMI is a simple flyback converter. The major design parameters that we are considering to optimize the CEC efficiency of the converter are denoted in red in Fig. 4.2 beneath the schematic of the converter and the magnetizing current waveform.

The switching frequency of the converter in the DCM greatly affects the switching loss in this operation mode as there is no soft switching in this mode. While increased switching frequency reduces the core loss to some degree, it increases the switching loss so a

perfect balance between these two has to be found. The number of switches is parallel increases the switching loss in DCM but reduces the conduction loss in the entire operation of the converter.

As it is mentioned before, the flyback transformer is the greatest source of losses in the IFMI, as results, it should be greatly optimized. The losses in the magnetic components are core and winding losses considering the high frequency losses as well. The material and shape of the ferrite core can be pre-determined considering the cores that are easily available in the market and with some preliminary analysis on the performance of the converter. Our analysis showed that the RM14 core with N97 material from EPCOS is the best available option, so, in the optimization procedure, we consider this core. However, the number of turns on the primary and secondary and also the magnetizing inductance of the transformer can be subjected to the optimization. Another important factor regarding the optimization of the transformer is the winding structure. It is very hard to get to numerically calculate the performance of various winding structures in terms of consumed space, leakage inductance, and winding resistance without the help of finite element analysis software. However, some relatively easy experiments with various structures can give us an idea of the best option, so, through experimentation with various core shapes and winding structures, we determined that the RM shape with the foil on the primary and Litz wire on the secondary is the best option. Also, to achieve the minimum leakage inductance, it is essential to sandwich the primary winding between two sections of the secondary winding as it is shown in Fig. 4.3. The optimal foil thickness of the primary winding is calculated based on a one dimensional

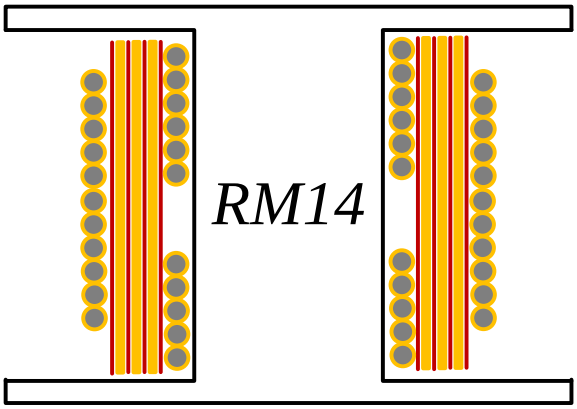


**Fig. 4.3: Flyback transformer winding structure**

approach as it is presented in [54]. Considering the available choices in the marked and the bobbin window, the foil thickness is chosen to be 3 mils (.003 inch).

These design parameters are highly dependent on each other and it is critical to evaluate the performance of the system for the entire load spectrum and not just one point. If the system is optimized only for maximum load, its performance can be really poor at low-load, thus affecting the CEC efficiency.

An automatic optimization procedure, as it is shown in Fig. 4.4, considering the entire IFMI system is applied as the solution for this challenging design procedure. The optimization algorithm loops through all the system variables noted in Fig. 4.2 to find the highest CEC efficiency possible.

In Fig. 4.4, the proposed efficiency optimization procedure is depicted [55]. In the beginning of the procedure, the fixed parameters are defined. As it is mentioned before, these fixed parameters include ferrite core shape and material, semiconductor data, capacitors data and input and output voltages. This step of the procedure can be easily done by studying the

**Table 4.1: Fixed parameters for the optimization procedure.**

| FIXED PARAMETERS | | |
|---|---|---|
| Main Switch ($S_1$, $S_2$) | | BSC190N15NS3 × 2 |
| Output Diode ($D_1$, $D_2$) | | IDB06S60C |
| Auxiliary Switch ($S_{a1}$, $S_{a2}$) | | IPD320N20N3G |
| DC Capacitors | | 4x UVZ1J332MRD |
| Transformer ($TR_1$, $TR_2$) | Core Type | RM14 – N97 |
| | Winding Structure | Litz-Coil-Litz |
| Snubber Capacitor ($C_s$) | | 1.68 nF |
| Output Filter | Inductor ($L_f$) | 60B224C- 220 $\mu$H |
| | Capacitor ($C_f$) | B32671P522-220 nF |
| Input voltage | | 30V |
| Output voltage RMS | | 240V |

available components in the market and selecting the right ones based on the design needs and it help to reduce the optimization time. In the next step, some arbitrary values are selected for the free design parameters shown in Fig. 4.2. In the next step, the operation point of the IFMI for 10%, 20%, 30%, 50%, 75% and 100% load is calculated and passed to the next step. In the next step, the process monitor the calculated operation point of the converter and makes sure that it is a feasible operation point by checking the switching frequency of the IFMI in the BCM mode and making sure it is between 100kHz and 400kHz (enforced by the magnetic material) and also makes sure that the DCM operation of the converter is actually possible using this parameters and that the converter does not operate in the CCM. If everything checks out, all the component losses are calculated in the next step and the efficiency for each load in calculated. In the next step, the optimization procedure calculates the CEC efficiency and stores the highest calculated efficiency then loops through all the feasible values to make sure the highest CEC efficiency is achieved.

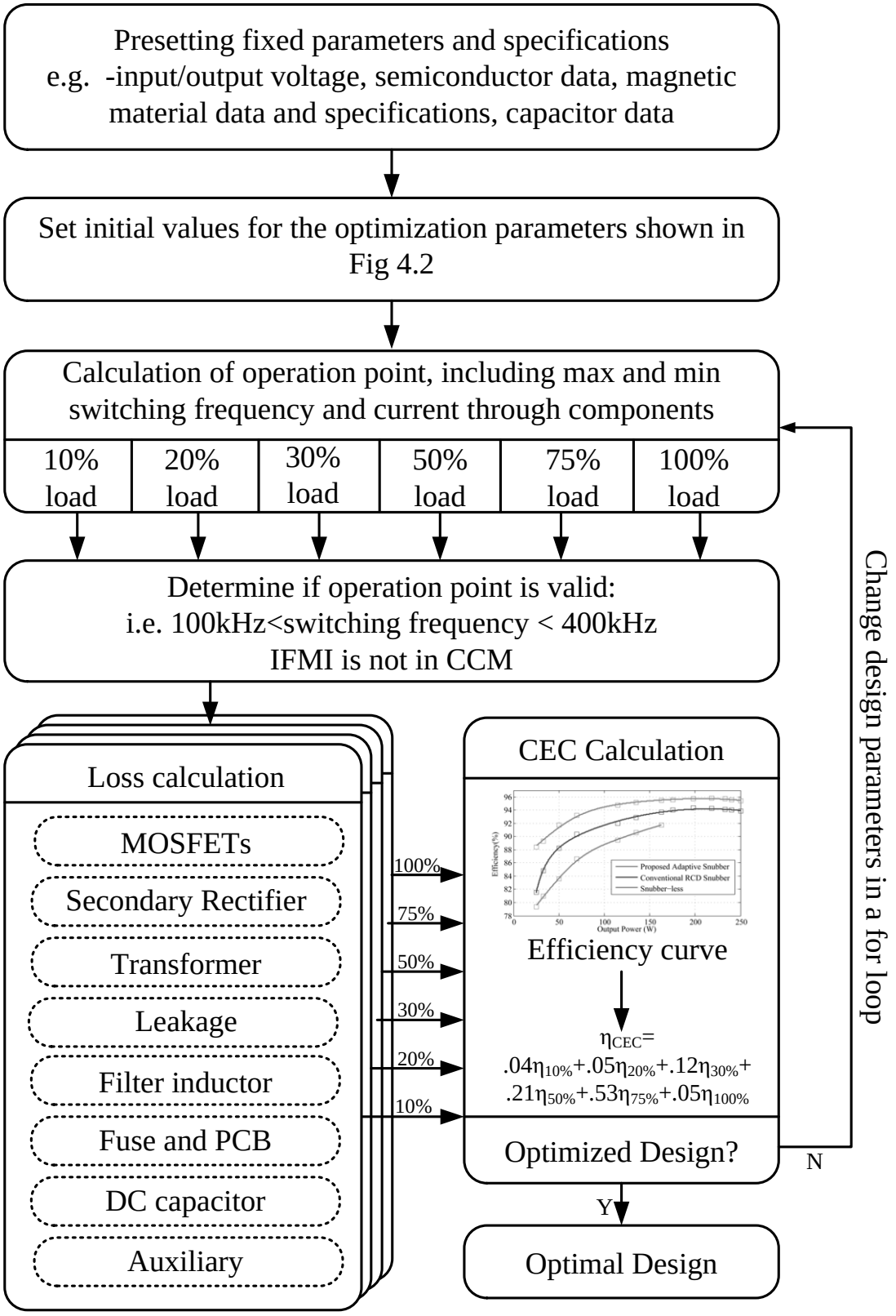


**Fig. 4.4: Automatic CEC efficiency optimization procedure for the IFMI.**

**Table 4.2: Results of optimization for individual power levels in the CEC formula**

OPTIMIZATION RESULTS

| Power level | $F_{DCM}$ | $\theta_t^\circ$ | $L_m$ | $N_p$ | $N_s$ |
|---|---|---|---|---|---|
| 10% | 100kHz | 48° | 9.5µH | 3 | 25 |
| 20% | 100kHz | 48° | 7.5µH | 3 | 25 |
| 30% | 100kHz | 48° | 5.5µH | 3 | 25 |
| 50% | 100kHz | 46° | 5µH | 3 | 24 |
| 75% | 100kHz | 40° | 4.6µH | 3 | 21 |
| 100% | 100kHz | 34° | 4.5µH | 3 | 18 |

The fixed parameters, including components and materials, are listed in Table 4.1. only integer values are considered for the number of primary and secondary turns and also the number of switches in parallel.

The auxiliary power loss in the optimization procedure is considered to be constant and is measured experimentally during the no-load operation of the IFMI. This power loss tend to affect the performance specifically in the light load conditions.

### 4.3.1 Optimization results

In this section, the results of the optimization process are explained.

If the optimization was to be performed individually for each power level in the CEC formula, the results would have been like what is presented in Table 4.2. The minimum switching frequency for this optimization has been set to 100 kHz in order to limit the size of the transformer core. As it can be seen in this table, at low power level higher inductance value for the transformer is desirable in order to limit the maximum switching frequency of

the converter in BCM. However, as the power level increases the optimum value for the magnetizing inductance value decreases because high inductance values correspond to higher switch on-time which in turn corresponds to higher flux density in the transformer.

Another important observation in Table 4.2 is that the optimum $\theta_t^\circ$ increases as the output power of IFMI decreases. The physical reason behind this observation is the fact that at lower power levels, the average switching frequency of the converter increases in the BCM operation, so the optimization process increases the $\theta_t^\circ$ in order to increase the average power that is being converted in the BCM affectively decreasing the average switching frequency of the IFMI in the BCM operation.

It is also interesting to see that at lower power levels, higher secondary to primary turns ratio is desirable in order to decrease the effective switching voltage of the MOSFETs and increase the efficiency, however, this leads to higher primary RMS current and as a result, at higher power levels, it would me more beneficial to decrease the turn ratio and limit the primary RMS current. This is why we see that the optimization process has selected lower secondary turns at higher power levels.

The presented results in Table 4.2 are very interesting and give us an idea of how the optimum values for the optimization parameters change as the output power of the IFMI changes. However, these results are not beneficial as they are not aimed at increasing the CEC efficiency of the converter. Since the output power of the IFMI changes significantly based on the PV panel working conditions, if we choose any of the rows in Table 4.2 as the

**Table 4.3: Results of automatic optimization procedure for the CEC efficiency**

OPTIMIZATION RESULTS

| Power level | $F_{DCM}$ | $\theta_t^\circ$ | $L_m$ | $N_p$ | $N_s$ |
|---|---|---|---|---|---|
| 10% | 100kHz | NA | 5.3µH | 3 | 20 |
| 20% | 100kHz | NA | | | |
| 30% | 100kHz | 77° | | | |
| 50% | 104kHz | 37° | | | |
| 75% | 110kHz | 37° | | | |
| 100% | 140kHz | 37° | | | |

final optimized values, the efficiency of the converter would be optimized only for that power level and not the whole CEC spectrum.

In order to optimize the CEC efficiency of the IFMI, the automatic optimization process of Fig. 4.4 is executed using MATLAB. The optimized parameters are shown in Table 4.3. The results of this table are obtained by considering two MOSFETs in parallel.

As it can be seen in Table 4.3, if the output power of the IFMI is below 20% of its maximum power, it is best to not use the BCM operation in order to limit the switching frequency of the converter. It is also demonstrated in this table that as the power level increases, it is better to increase the switching frequency of the IFMI in the DCM in order to decrease the core loss. This result basically tells us that at higher power levels, the increase in switching loss by increasing the switching frequency is smaller than the decrease in the core loss so it is beneficial to increase the switching frequency in the DCM as the power of the converter increases.

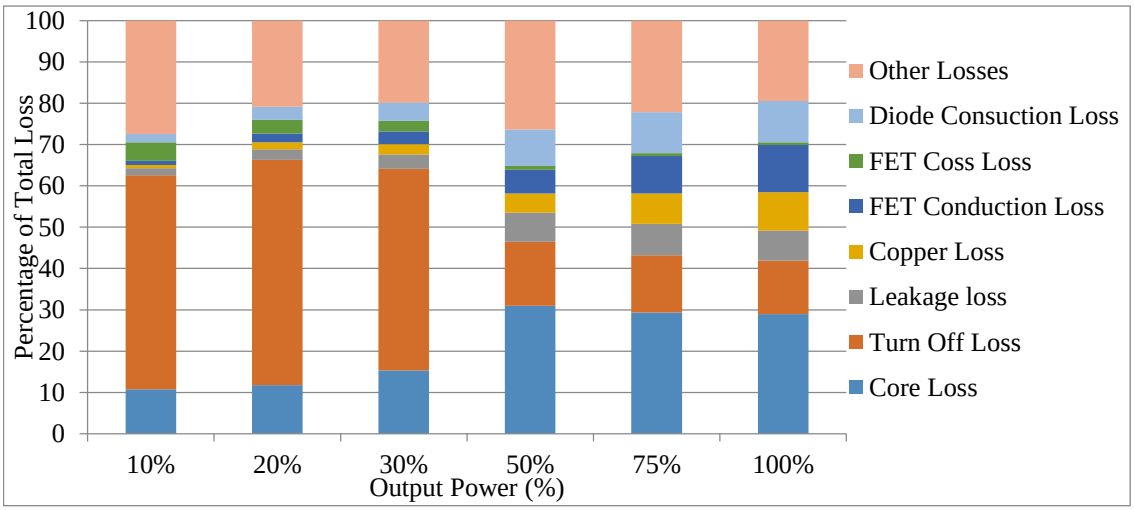


**Fig. 4.5: Distribution of power loss at different power levels for the optimized hardware**

The loss breakdown chart of the IFMI at different power levels is shown in Fig. 4.5. As it can be seen in chis chart, the power levels below 30% of the maximum power, the MOSFET turn off loss is the dominating source of losses but as the power level increases, the core loss becomes more dominant. The reason for this observation is the fact that at lower power level, the converter operates in DCM for most of the time and since the snubber is turned off in this mode, the turn off loss become dominant.

The calculated CEC efficiency of the IFMI using the parameters of Table 4.3 is 94.85% which is higher than 92.6% achieved in the previous chapter. In the next section, we implement the parameters of Table 4.3 in the experimental setup and measure the achieved CEC efficiency to verify the effectiveness of the optimization procedure.

### 4.3.2 Experimental results

The transformer in the IFMI setup is redesigned based on the parameters indicated in Table 4.3. Also, the switching frequency of the converter in the DCM is implemented in the

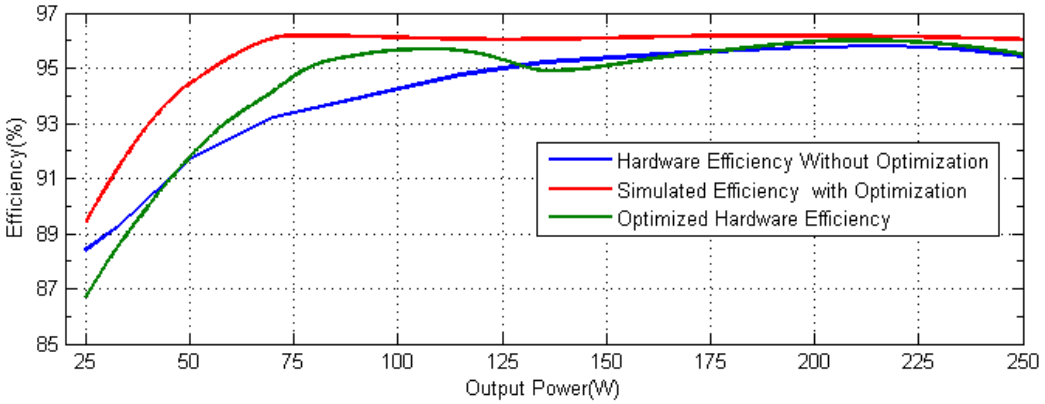


**Fig. 4.6: Efficiency curves.**

hardware based on what appears in Table 4.3 using linear approximation. The DCM to BCM transition angle is also implemented in the hardware between 30% and 50% of maximum power using linear approximation while considering the transition angle to be 70˚ at 30% load in order to limit the overshoot across the MOSFETs. It should also be mentioned that even though the optimization algorithm dictates DCM only operation below 30% of the maximum power, in order to prevent voltage overshoot across MOSFETS, we limit the maximum angle of the DCM operation to 70˚.

The calculated CEC efficiency for 250W IFMI is 95.72%. According to experimental results, the CEC efficiency of the optimized hardware is 94.96% which is .3% greater than the achieved CEC efficiency in the original hardware. The optimized hardware also demonstrates a 96% maximum efficiency which has a .2% bump compared to the non-optimized hardware.

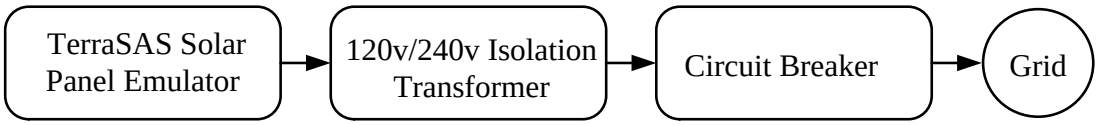


**Fig. 4.7: Overview of the test setup for commercial micro-inverters efficiency testing**

## 4.4 Comparison to available commercial products

Several commercial micro inverter products have been tested in the FREEDM lab for the efficiency curve and CEC efficiency data [56]. The overview of the test setup is presented in Fig. 4.7. As it can be seen in this figure, a PV panel emulator is used as the input source of the micro-inverters to further simulate the real world situation. In the following sections, the results of efficiency test on three micro-inverters from Enphase, Solar Bridge and Lead solar are presented.

### 4.4.1 Enphase M250 micro-inverter

This micro-inverter utilizes the IFMI topology which is the focus of this thesis, as a result, it can present a good benchmark data for comparing the solution presented in this thesis with commercial solutions.

The maximum power of this micro inverter is 250W and based in its datasheet, it has a maximum efficiency of 96.5% as well as the CEC efficiency of 96.5%. The test result for this micro-inverter is shown in Fig. 4.8. The efficiency test demonstrates a maximum efficiency of 96.5% but the measured CEC efficiency is 95.33% which has more than 1.2% difference with the data provided in the inverter's datasheet.

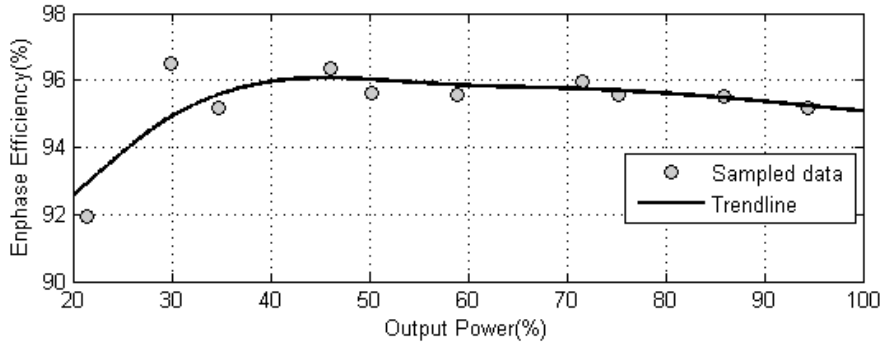


**Fig. 4.8: Efficiency curve of Enphase M250 micro-inverter**

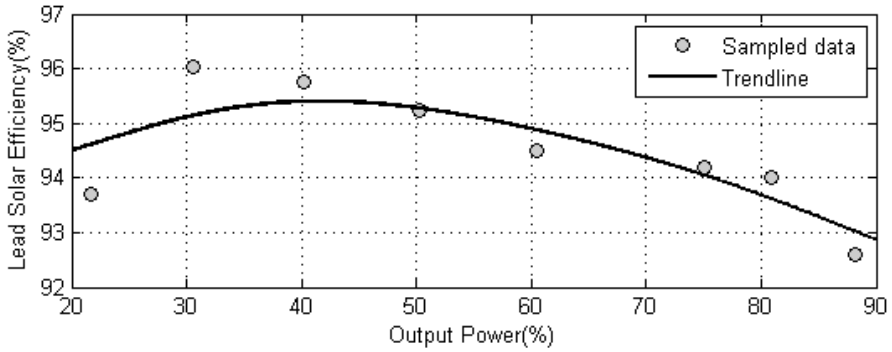


**Fig. 4.9: Efficiency test results for Lead Solar micro-inverter**

### 4.4.2 Lead Solar LS250 micro inverter

Just like the M250 inverter from Enphase, this micro-inverter also utilizes the IFMI topology and it rated power is 250W as well. The measured efficiency of the inverter is shown in Fig. 4.9. this inverter demonstrates a maximum efficiency of 96% which is somewhat in line with the advertised maximum efficiency of 96.2%, given the different test conditions. The measured CEC efficiency of this inverter is 94.5% which is 1% lower the advertised CEC efficiency of 95.5%.

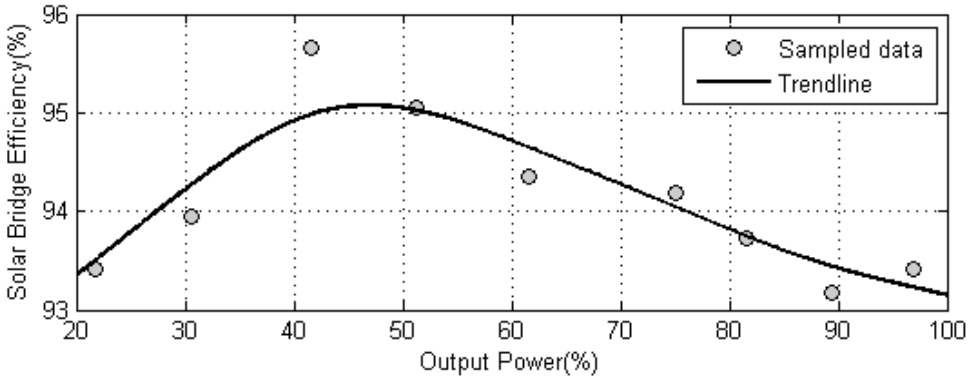


**Fig. 4.10: Efficiency curve of Solar Bridge micro-inverter**

### 4.4.3 Solar Bridge Pantheon P250LV-208/240 micro-inverter

This micro-inverter has a name-plate maximum efficiency of 95.7% and a CEC efficiency of 95%. The result of the efficiency test for this micro-inverter is shown in Fig. 4.10. The test results show the maximum efficiency of 95.6% and a CEC efficiency of 94.2%

# 5. Conclusion and Future Work

## 5.1 Conclusion

With the increasing concerns about fossil fuel reserves and the environmental issues of burning them, there is a worldwide movement toward renewable energy resources. Among different types of renewable energy sources, photovoltaic (PV) energy is becoming more and more popular due to its availability, low cost and ease of use. As the cost of PV module decreases year by year, the cost of inverters is becoming more visible in the total cost of the PV systems. As a result, special effort has been made in the past decade to reduce the cost of PV inverters and labor associated with installing them.

During the past decade, the PV micro-inverters have been gaining attention for grid connected PV systems due to their improved energy harvest, plug-and-play operation and enhanced modularity and flexibility.

In this thesis, we presented a novel approach to increase the efficiency of vastly popular flyback micro-inverter by employing an adaptive snubber and hybrid control strategy. The proposed adaptive snubber only requires a small capacitor in the range of several nano-Farads and it makes use of parasitic capacitances in the circuit. It also only requires a small MOSFET which shares the same source with the main flyback switch which leads to reduced cost and complexity.

The effectiveness of the proposed adaptive snubber circuit in association with the hybrid control strategy is verified through experimentation using a 250W hardware prototype.

An optimization procedure is then introduced which aimed at increasing the maximum and CEC efficiency of the inverter using detailed loss model of the inverter. The hardware setup was then modified using the parameters that were calculated using the optimization procedure. The modified hardware was able to achieve the maximum efficiency of 96% and CEC efficiency of 94.96%.

The archived efficiency and performance in this thesis is on-par with commercial micro inverters and proves the effectiveness of the proposed adaptive snubber.

## 5.2 Future work

Even though the achieved efficiency in this thesis is quite high for the IFMI topology, there is still room for improving the CEC efficiency of the topology. As the hybrid control method dictates, the IFMI has to operate in DCM near the zero crossing of the grid voltage. The switching loss in the DCM operation can be increased by implementing valley switching in this operation mode. Further improvement of the performance of the IFMI can be done using custom magnetics.

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# APPENDICES

# Appendix A

MATLAB program for the CEC efficiency optimization:

```
clc;
clear;
effmax1   = [0 0 0 0 0 0];
eff1      = effmax1;
error1    = eff1;
CECmax1   = 0;
cecPower1 = 125*[.1 .2 .3 .5 .75 1];
N97;
%%Grid Specs
Fg = 60;
Tg = 1/Fg;
Wg = 2*pi*Fg;
%%DC Cap Specs
Cdc = 4 * 3300 * 10^-6;
tand = .15;
Aave = 170 * 10^-6; %RM14
N = 3;%primary turns
Vin = 30;
Vo = 240;
Rdcp = 6.45/(1000*1.000);%not considering the skin effect
Rdcs = 106 /(1000*1.000);%
Nsw = 2; %Switches in parallel
Rdson = 20/1000;%@60oc
Coss = Nsw * 250 * 10^-12 + 3*10^-9;
Tturnoff = 28*10^-9;
%diode Information
Vf0 = .9;
Rf  = .1;
%output filter characteristics
Rfuse = 16*10^-3;
Rind = 50*10^-3;
for(Lm1=(5:.001:7)*10^-6)
for(Nsec1=18:1:22)
tic;
parfor(powerIndex1=1:6)
for( Fdcm1 = 100000:2000:150000 )
for(boundaryAngle1=30:1:80)
if( boundaryAngle1<(180/pi* asin(30*Nsec1/(3*240*sqrt(2)))) ||
(30*Nsec1/(3*240*sqrt(2)))>1 )
```

```
continue;
else
if(boundaryAngle1==80)
 [temp1 temp2]=lossFunction(cecPower1(powerIndex1), Fdcm1, 88,
Lm1, Nsec1);
eff1(powerIndex1) = temp1;
if(temp2<.5 && eff1(powerIndex1)>effmax1(powerIndex1) )
effmax1(powerIndex1)=eff1(powerIndex1);
opt(powerIndex1, :)=[cecPower1(powerIndex1), Fdcm1,
boundaryAngle1, Lm1, Nsec1];
end
else
Po= cecPower1(powerIndex1);
Fdcm=Fdcm1;
boundaryAngle=boundaryAngle1;
Lm=Lm1;
Nsec=Nsec1;
errorNO = 0;
Findex=0;
Bindex=0;
Llk=.6/100*(6.2*10^-6/Lm)*Lm;
n = Nsec/N;%turns Ratio
Tdcm = 1/Fdcm;
t=0;
operationMode = 0;
%Transformer information
Ploss = 0;
Eloss = 0;
Eleak = 0;
%Switch Information
Pcoss = 0;
Pturnoff = 0;
refcurrent = 0;
time = 0;
deltaFlux = 0;
baseBm = 0;
baseF = 0;
actualF = 0;
Irmsp = 0;
Iavep = 0;
Iaves = 0;
Irmss = 0;
for i=1:1000000
switch(operationMode)
```

```
case(0)
t = t + Tdcm;
vg = sqrt(2) * Vo * sin(Wg*t);
Iref = 2*sqrt(Po*Tdcm/Lm)*sin(Wg*t);
d  = Lm * Iref / (Vin);
if( (d+dc)>Tdcm )
errorNO = 1;
break;
end
DB = Vin* d / (N * Aave);
Bmax = DB /2;
r= Tdcm * 2/pi^2*(d+dc)/(d*dc);
error = 10^10;
for ii=1:6
error = abs(f(ii)-r*Fdcm);
Findex = ii;
end
end
error = 10^10;
for j=1:4
if( abs(Bm(Findex,j)-Bmax) < error )
error = abs( Bm(Findex,j) - Bmax );
Bindex = j;
end
end
loss = pvsin(Findex, Bindex) *
(r*Fdcm/f(Findex))^(alpha(Findex, Bindex)-1) *
(Bmax/Bm(Findex,Bindex))^beta(Findex)*(Fdcm/f(Findex));
Ploss = loss;
Eloss = Eloss + Ploss / Fdcm;
Eleak = Eleak + .5*Llk*Iref^2;
Pcoss = Pcoss + .5 * Coss * vReflected^2;
Pturnoff = Pturnoff + Iref * vReflected * Tturnoff;
Irmsp = Irmsp + Iref^2 * d / 3;
Irmss = Irmss + (Iref/n)^2 * dc / 3;
Iavep = Iavep + Iref * d * .5;
Iaves = Iaves + Iref/n * dc * .5;
if(Fg*t*360 >= boundaryAngle)
operationMode = 1;
end
case(1)
vg = sqrt(2) * Vo * sin(Wg*t);
Iref = 2*(vg/Vin+n)*sqrt(2)*Po/Vo * sin(Wg*t);
d = Lm * Iref/Vin;
```

```
dc = Lm * Iref / (vg/n);
Fbcm = 1/(d+dc);
if(Fbcm>500000)
errorNO = 1;
break;
end
DB = Vin * d / (N * Aave);
Bmax = DB /2;
r= 2/pi^2*(d+dc)^2/(d*dc);
error = 10^10;
for j=1:length(f)
if( abs(f(j)-r*Fbcm) < error)
error = abs(f(j)-r*Fbcm);
Findex = j;
end
end
error = 100000;
for j=1:4
if( abs( Bm(Findex,j) - Bmax ) <= error)
error = abs( Bm(Findex,j) - Bmax );
Bindex = j;
end
end
loss = pvsin(Findex, Bindex) *
(r*Fbcm/f(Findex))^(alpha(Findex, Bindex)-1) *
(Bmax/Bm(Findex,Bindex))^beta(Findex) * (Fbcm/f(Findex));
Ploss = loss;
Eloss = Eloss + Ploss / Fbcm;
Eleak = Eleak + .5*Llk*Iref^2;
Irmsp = Irmsp + Iref^2 * d / 3;
Irmss = Irmss + (Iref/n)^2 * dc / 3;
Iavep = Iavep + Iref * d * .5;
Iaves = Iaves + Iref/n * dc * .5;
t = t + 1/Fbcm;
if(Fg*t*360 >= 90)
break;
end
end
end
Irmsp = sqrt(1/t*Irmsp);
Irmss = sqrt(1/t*Irmss);
Iavep = Iavep/t;
Iaves = Iaves/t;
```

```
Pcore = Eloss * 1000*14000*10^-9*240; % volume tacken into
effect
Pleak = Eleak*240;
Pcopperp = Rdcp*Irmsp^2;
Pcoppers = Rdcs*Irmss^2;
Pcondsw = Rdson/Nsw*Irmsp^2;
Pcoss = Pcoss * 240;
Pturnoff = Pturnoff*240;
Pcondd = Vf0 * Iaves + Rf*Irmss^2;
Poutfilter = (Rfuse+Rind) * (2*Po/Vo)^2;
dVdc = Vin - sqrt(Vin^2 - Po/(4*Fg*Cdc));
dIdc = Cdc/4 * dVdc * 240 * pi;
Pcdc = 4 * .5 * tand/(2*pi*120*Cdc/4) * (dIdc)^2;
Plosst = Pcore + Pcopperp + Pcoppers + Pcondsw + Pcoss +
Pcondd + Poutfilter + Pcdc + Pleak +.6;
Eff = Po/(Po+Plosst)*100;
eff1(powerIndex1) = Eff;
error1(powerIndex1) = errorNO;
if( error1(powerIndex1)<.5 &&
eff1(powerIndex1)>effmax1(powerIndex1) )
effmax1(powerIndex1)=eff1(powerIndex1);
opt(powerIndex1, :)=[cecPower1(powerIndex1), Fdcm1,
boundaryAngle1, Lm1, Nsec1];
end
end
end
end
end
end
toc;
CEC= effmax1 * transpose([.04 .05 .12 .21 .53 .05]);
if(CEC > CECmax1)
CECmax1 = CEC;
optMax = opt;
end
effmax1   = [0 0 0 0 0 0];
eff1      = effmax1;
end
end
```