ABSTRACT

NAJM, ELIE MICHEL. Design and Implementation of an Innovative Residential PV System. (Under the direction of Alex Q. Huang).

This work focuses on the design and implementation of an innovative residential PV system. In chapter one, after an introduction related to the rapid growth of solar systems' installations, the most commonly used state of the art solar power electronics' configurations are discussed, which leads to introducing the proposed DC/DC parallel configuration. The advantages and disadvantages of each of the power electronics' configurations are deliberated. The scope of work in the power electronics is defined in this chapter to be related to the panel side DC/DC converter. System integration and mechanical proposals are also within the scope of work and are discussed in later chapters.

Operation principle of a novel low cost PV converter is proposed in chapter 2. The proposal is based on an innovative, simplified analog implementation of a master/slave methodology resulting in an efficient, soft-switched interleaved variable frequency flybacks, operating in the boundary conduction mode (BCM). The scheme concept and circuit configuration, operation principle and theoretical waveforms, design equations, and design considerations are presented. Furthermore, design examples are also given, illustrating the significance of the newly derived frequency equation for flybacks operating in BCM.

In chapters 3, 4, and 5, the design implementation and optimization of the novel DC/DC converter illustrated in chapter 2 are discussed. In chapter 3, a detailed variable frequency BCM flyback design model leading to optimizing the component selections and transformer design, detailed in chapter 4, is presented. Furthermore, in chapter 4, the method

enabling the use of lower voltage rating switching devices is also discussed. In chapter 5, circuitry related to Start-UP, drive for the main switching devices, zero-voltage-switching (ZVS) as well as turn OFF soft switching and interleaving control are fully detailed. The experimental results of the proposed DC/DC converter are presented in chapter 6.

In chapter 7, a novel integration method is proposed for the residential PV solar system. The proposal presents solutions to challenges experimented in the implementation of today's approaches. Faster installation time, easier system grounding, and integration of the power electronics in order to reduce the number of connectors' and system cost are detailed. Installers with special skills as well as special tools are not required for implementing the proposed system integration. Photos of the experimental results related to the installation of a 3kW system, which was fully completed in less than an hour and a half, are also presented.

Design and Implementation of an Innovative Residential PV System

by
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DEDICATION

In memory of my loved ones that I have lost during and before my PhD journey; may they all rest in peace. I dedicate this dissertation work to my father, Michel I. Najm (1931-2012), my mother-in-law Saada G. Maalouf (1945-2013), and to my late uncles and grandparents. I will never forget that in the midst of a war devastated country, my grandfather, Khalil A. Jabbour, drove me to the Beirut International Airport in August 21, 1978, under the wrath of fighting, waiting for hours until he made sure that my plane to the U.S. has safely left the airport. His courageous sacrifices continue to hearten and inspire me.

BIOGRAPHY

Elie Najm operated as a technical leader at IBM Power Electronics System for the Networking Hardware Division from 1982 to 1996. He has held senior management positions in the construction industry, in the U.S. and overseas, from 1997 to 2010. He was admitted as a PhD student in 2010 at North Carolina State University (NCSU) and has performed as a research assistant at NCSU FREEDM Systems Center.

Elie's research areas are solar energy, power electronics, analog electronic circuits and systems, power system architecture, and system integration. At FREEDM, he has led the System Integration and Demonstration as well as the Electrical System Improvements' teams for the "Cost Effective, Residential Plug and Play Photovoltaic System," sponsored by the U.S. Department of Energy (DOE) SunShot Initiative. He has designed and developed a low cost solar converter in line with the SunShot cost target of $0.12 per watt. He has also directed the system engineering for the NSF supported FREEDM Systems Center's Green Energy Hub project (GEH). Furthermore, he has led activities such as the performance evaluation and test box designs for a Solar powered 40kW UPS developed by Eaton Corp. He has published several papers as a result of his research.

While working for IBM, Elie has received 6 patents and 21 technical disclosures as well as multiple awards to include the "IBM Invention Achievement Award" and the "IBM Outstanding Innovation Award." He was featured numerous times in the IBM Vital Signs publication.

Elie Najm received his B.Sc. degree from the University of Dayton, Dayton, Ohio in 1981 and his M.Sc. degree from Duke University, Durham, North Carolina in 1986, both in electrical engineering. He received a Graduate Certificate in Renewable Electric Energy Systems from NCSU in 2014.

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I would like to thank my advisor and mentor, Professor Alex Q. Huang for his continuous guidance and support throughout the process. I am grateful for his efforts in bringing out the best in me in this sound North Carolina State University's PhD program. The dedication that Dr. Huang offers to all his students is beyond all expectations. It has been a great experience serving under the leadership of a scholar such as Professor Huang.

I would also like to extend my appreciation to my committee members, Dr. Mesut Baran, Dr. Subhashish Bhattacharya, and Dr. John Mackenzie for their assistance, direction, and support. Under Dr. Baran's leadership, I was able to complete and receive the Graduate Certificate in Renewable Electric Energy Systems in 2014.

My gratefulness also goes to all members in the FREEDM Systems Center. The support that I have received from Drs. Iqbal Hussein (FREEDM director), Wensong Yu, Douglas Hopkins, David Lubkeman, Rogelio Sullivan, Ewan Pritchard, and all the other FREEDM faculty and staff, has been instrumental. The lab manager, Hulgize Kassa, and his assistant Gregory Norris, have persistently upheld a positive and safe lab environment. The continuous assistance from Colleen Reid and Karen Autry has been essential in my long PhD journey.

I would like to express my indebtedness to my long time good friend, Charles Weant. Charles played a crucial role in the DOE solar PnP project's prototyping and system integration. Furthermore, post doctorates, such as Dr. Ruiyang Yu, aided me on several occasions, while so many great students, such as Mohammad Ali Rezaei, Md Tanvir Arafat Khan, Qingyun Huang, Dr. Fei Wang, and several others that I have worked with, have greatly contributed to the elevated outcomes of many key FREEDM Systems Center projects.

I have been blessed to have the love and support of my family. I am grateful to my caring and beautiful wife, Rita; to my 6 children: Yvone, Michael (Micho), Joseph (whom I have been constantly praying for), Rita (Rattout), Christian (#7), and Julian (the angel of the family); to my daughter-in-law, Eya, and to my grandchildren: Elie (Leo) and Aiden (Addouni). Yvone, who has also graduated from NCSU, did carry us financially throughout my NCSU journey. It brings tears to my eyes just to think about the sacrifices that she has made; I am so proud of her.

I am also blessed for my heavenly gift: My mother. She has always been there for me, my brothers, and the big family. The Lord has indeed been so kind to me with such a loving family, which is much more than I deserve.

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1-1 Introduction

In its 2014 medium-term renewable energy market report [1], the International Energy Agency (IEA) has published that the global renewable electricity generation has increased by an estimated 240 terawatt hours (TWh) in 2013, which represent a growth of 5% from the prior year. Furthermore, the report also indicated that with such a growth, the renewable electricity generation has reached nearly 5070 TWh, which accounted for approximately 22% of total power generation. Moreover, it has also indicated that the renewable capacity rise due to the deployment of hydropower and solar PV was faster than expected. *Fig. 1.1* illustrates the historical and projected global renewable electricity production by region [1].

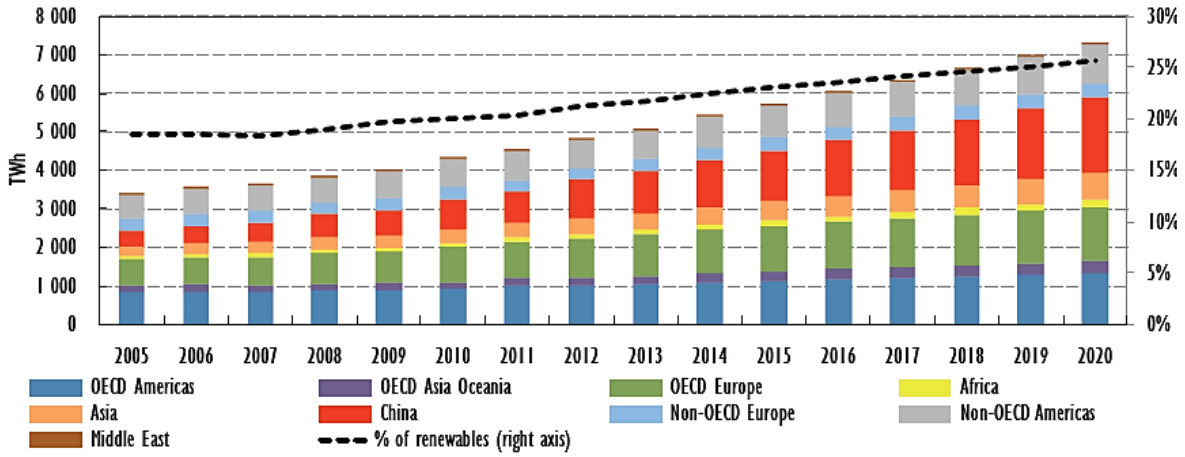


Figure 1.1: Global renewable electricity production by region, historical and projected [1].

On the other hand, the Renewable Energy Policy Network for the 21st Century (REN21), in their Renewables 2014 Global Status Report [2], stated that "Around the world,

major industrial and commercial customers are turning to renewables to reduce their energy costs while increasing the reliability of their energy supply." Furthermore, the REN21 report agreed with the REA above referenced report regarding the rapid growth of Solar PV installations. It stated that "Solar PV has continued to expand at a rapid rate, with growth in global capacity averaging almost 55% annually over the past five years." *Table 1.1* illustrates the years 2012 and 2013 figures of the global utilization of renewable energy [2].

Table 1.1: Renewable Energy Indicators 2013 as provided by REN21. [2]

		START 2004[1]	END 2012	END 2013
INVESTMENT				
New investment (annual) in renewable power and fuels[2]	billion USD	39.5	249.5	**214.4** (249.4)
POWER				
Renewable power capacity (total, not including hydro)	GW	85	480	**560**
Renewable power capacity (total, including hydro)	GW	800	1,440	**1,560**
Hydropower capacity (total)[3]	GW	715	960	**1,000**
Bio-power capacity	GW	<36	83	**88**
Bio-power generation	TWh	227	350	**405**
Geothermal power capacity	GW	8.9	11.5	**12**
Solar PV capacity (total)	GW	2.6	100	**139**
Concentrating solar thermal power (total)	GW	0.4	2.5	**3.4**
Wind power capacity (total)	GW	48	283	**318**
HEAT				
Solar hot water capacity (total)[4]	GW_{th}	98	282	**326**
TRANSPORT				
Ethanol production (annual)	billion litres	28.5	82.6	**87.2**
Biodiesel production (annual)	billion litres	2.4	23.6	**26.3**
POLICIES				
Countries with policy targets	#	48	138	**144**
Feed-in Number of states / provinces / countries	#	34	97	**98**
RPS / quota policies Number of states / provinces / countries	#	11	79	**79**
Tendering Number of states / provinces / countries	#	8	45	**55**
Heat obligations / mandates Number of countries	#	n/a	19	**19**
Biofuel obligations / mandates[5] Number of countries	#	10	52	**63**

Moreover, [2] indicated that countries like United States, China, Germany, Canada, and Brazil, have maintained their status as the topmost countries that have deployed renewable power capacity. As of the end of 2013, the list of the top five countries' investment in renewable power and fuels is illustrated in *Table 1.2*, while the total capacity or generation is illustrated in *Table 1.3*.

Table 1.2: Top five countries' annual investment/net capacity additions/production in 2013. [2]

	1	2	3	4	5
Investment in renewable power and fuels	**China**	United States	Japan	United Kingdom	Germany
Share of GDP 2012 (USD) invested[1]	**Uruguay**	Mauritius	Costa Rica	South Africa	Nicaragua
Geothermal power capacity	**New Zealand**	Turkey	United States	Kenya	Philippines
Hydropower capacity	**China**	Turkey	Brazil	Vietnam	India
Solar PV capacity	**China**	Japan	United States	Germany	United Kingdom
CSP capacity	**United States**	Spain	United Arab Emirates	India	China
Wind power capacity	**China**	Germany	United Kingdom	India	Canada
Solar water heating capacity[2]	**China**	Turkey	India	Brazil	Germany
Biodiesel production	**United States**	Germany	Brazil	Argentina	France
Fuel ethanol production	**United States**	Brazil	China	Canada	France

Table 1.3: Top five countries' total capacity or generation as of the end of 2013. [2]

	1	2	3	4	5
POWER					
Renewable power (incl. hydro)	**China**	United States	Brazil	Canada	Germany
Renewable power (not incl. hydro)	**China**	United States	Germany	Spain / Italy	India
Renewable power capacity *per capita* (not incl. hydro)[3]	**Denmark**	Germany	Portugal	Spain / Sweden	Austria
Biopower generation	**United States**	Germany	China	Brazil	India
Geothermal power	**United States**	Philippines	Indonesia	Mexico	Italy
Hydropower[4]	**China**	Brazil	United States	Canada	Russia
Hydropower generation[4]	**China**	Brazil	Canada	United States	Russia
Concentrating solar thermal power (CSP)	**Spain**	United States	United Arab Emirates	India	Algeria
Solar PV	**Germany**	China	Italy	Japan	United States
Solar PV capacity *per capita*	**Germany**	Italy	Belgium	Greece	Czech Republic
Wind power	**China**	United States	Germany	Spain	India
Wind power capacity *per capita*	**Denmark**	Sweden	Spain	Portugal	Ireland
HEAT					
Solar water heating[2]	**China**	United States	Germany	Turkey	Brazil
Solar water heating capacity *per capita*[2]	**Cyprus**	Austria	Israel	Barbados	Greece
Geothermal heat[5]	**China**	Turkey	Iceland	Japan	Italy

1-2 U.S. Residential Solar Energy Installations

Based on its 2014 second quarter Solar Market Insight Report [3], the Solar Energy Industries Association (SEIA) has claimed that as much as 1,133 MW_{dc} of solar PV was installed in the United States in the second quarter of 2014. The report also claimed that such a figure represents an increase of 21% in solar installations over the second quarter of 2013, which is the 4th largest quarter in the history of the market. Furthermore, the report also stated that "PV installations will reach 6.5 GW_{dc} in 2014, up 36% over 2013 and more than three times the market size of just three years ago." Moreover, the report also claimed that the U.S. residential solar market has seen steady growth, up 45% over the second quarter of 2013, where over 100 MWdc were installed in the second quarter of 2014, without any state incentive. *Fig. 1.2* illustrates the U.S. PV installations' trend from the second quarter of 2010 up to the second quarter of 2014 [3].

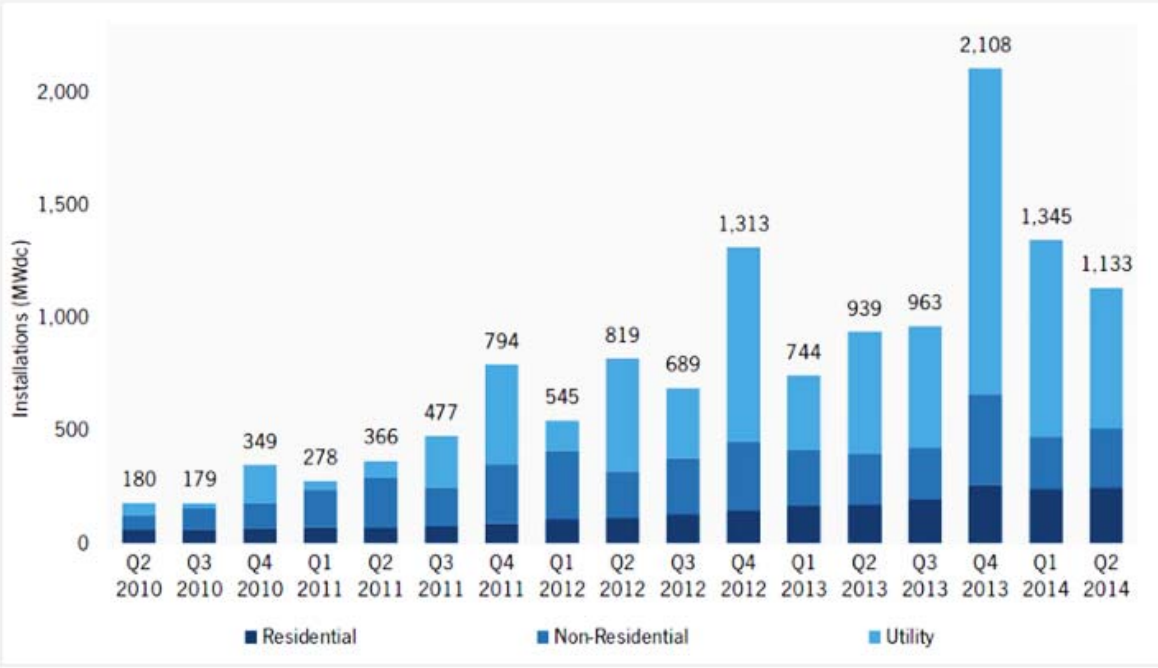


Figure 1.2: U.S. PV installations, Q2 2010-Q2 2014. [3]

1-3 U.S. Residential Solar Energy Installations Cost Trend

A major factor behind the steady growth of solar installations in the U.S. residential market is related to cost. In addition to the government incentives, the residential solar system cost has decreased a great deal in the past several years. Based on [3], "the cost of solar has come down enough that more customers can afford to pay the cash." *Fig. 1.3* illustrates the related cost reduction in one quarter only (first quarter of 2014 to second quarter of 2014) of the residential turnkey solar system pricing.

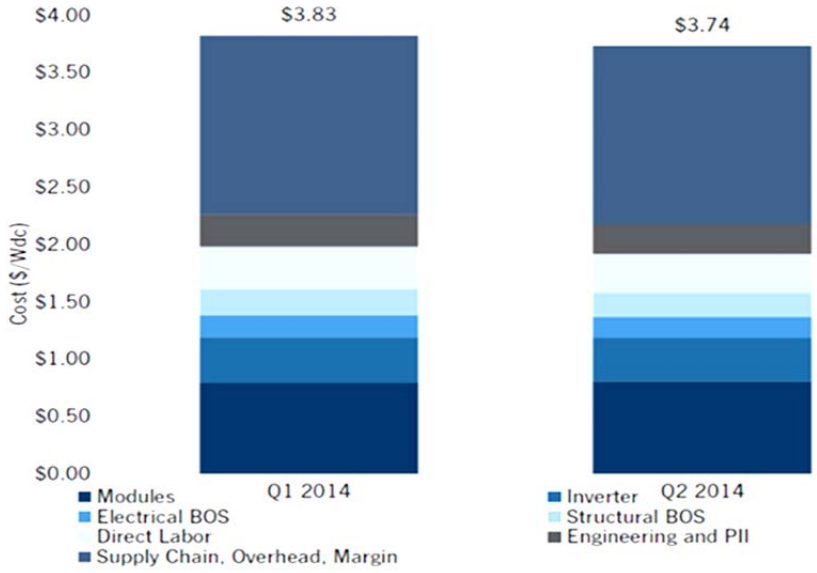


Figure 1.3: Modeled residential turnkey system pricing with cost breakdown, Q1 2014-Q2 2014. [3]

The history of reducing the cost of residential solar installations is also provided by the National Renewable Energy Laboratory (NREL) in its September 2014 report [4]. NREL claimed that the median pricing for residential and small commercial (≤ 10 kW) PV system installations completed in 2013, "based in part on data reported to PV incentive programs," was $4.69/W. Furthermore, the report also indicated that the "reported system prices of residential and commercial PV systems declined 6%–7% per year, on average, from 1998–

2013, and by 12%–15% from 2012–2013, depending on system size." *Fig. 1.4* illustrates the cost trend as provided by the said report.

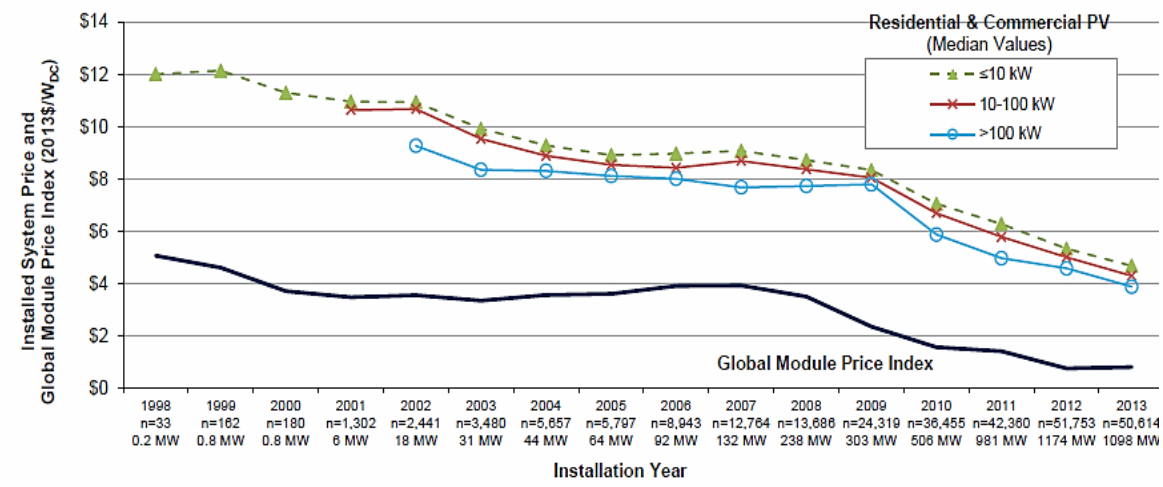


Figure 1.4: Median reported installed prices of residential and commercial PV systems over time. [4]

Moreover, [4] also provided a curve related to the projected average of the U.S. PV system prices over time. The said curve is illustrated in *Fig. 1.5*, where the brown line illustrates the reported median residential system price. In addition, the reported system price shown in *Fig. 1.5* assumes that the residential market median price is for systems that are less than or equal to 10 kW. The shown modeled residential system price exemplifies a 5 kW as an approximate residential system.

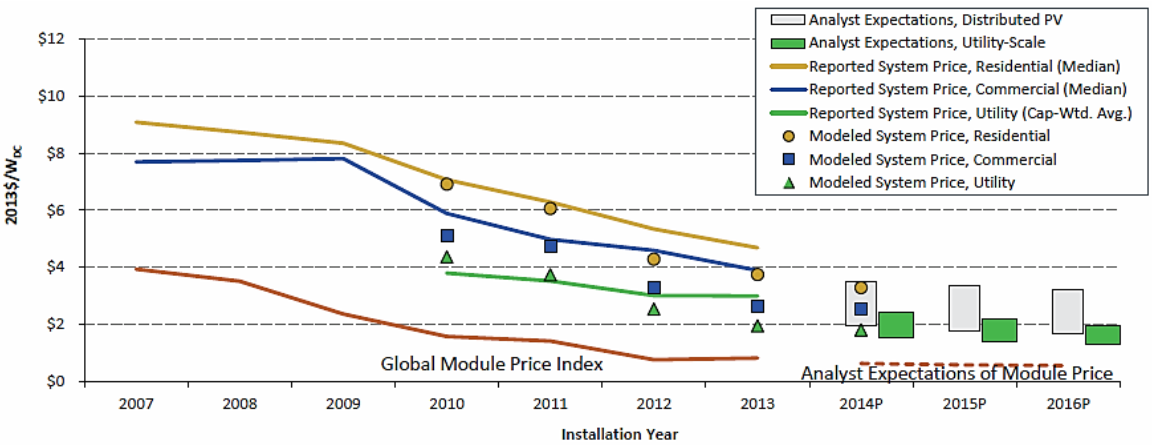


Figure 1.5: Reported, bottom-up, and analyst-projected average U.S. PV system prices over time. [4]

1-4 Solar System State of the Art Configurations – Power Electronics

Several solar system architectures are currently utilized in residential applications (as well as commercial applications). The following is a brief description as well as highlight summary of the advantages and disadvantages of each.

1-4-1 String or Center Inverter Configuration

Fig. 1.6 exemplifies the string (central) inverter approach, which does not require power converter modules per panel. Instead, a central-inverter box to include communication and control per string is installed. In such configuration, the solar panels are connected in series to form an array, with a typical output voltage rating of 300 to 600VDC. The array output is connected to a single inverter, with an AC output that is typically tied to the grid. All communication circuitry are embedded in the central inverter. The following is a list of some of the main advantages and disadvantages of the string inverter configuration:

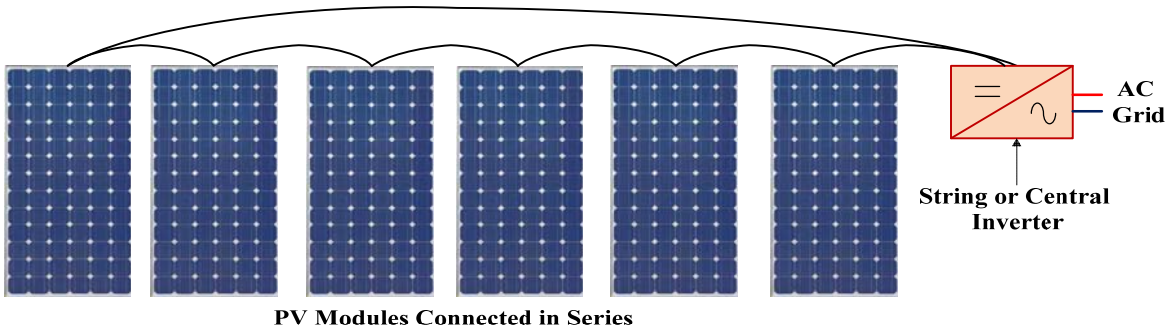


Figure 1.6: String (central) inverter configuration.

Advantages:

- Well established single stage configuration.
- Built-in isolation for solar panels.

- Lowest system component cost approach.

Disadvantages:

- Lack of distributed maximum power point tracking (MPPT), which results into lower system efficiency.
- The maximum output performance is limited by the worst performing solar panel (partial shading, manufacturing defect, dust, etc.).
- Presence of high DC voltage (sum of string of PV panel voltages) that necessitates additional protection steps, as required by national electric code (NEC) regulations.

1-4-2 AC Parallel (Micro-Inverter) Configuration

The AC parallel (micro-inverter) configuration, illustrated in *Fig. 1.7*, consists of several parallel PV modules that each includes a DC/AC inverter. Such parallel DC/AC inverters are connected to form an AC grid connected solar energy system. The maximum power point (MPP) operation of each panel can be guaranteed with this configuration and modular design is easily achievable. The market available DC/AC inverter products, such as the one provided by Enphase Energy, embed communication circuitry in each of the micro-inverters, which communicates with its system gateway.

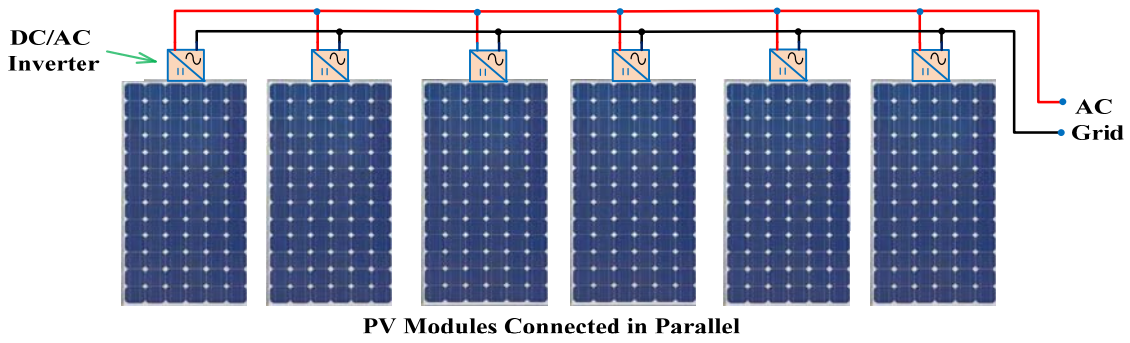


Figure 1.7: AC parallel (micro-inverter) configuration.

Advantages:

- Isolation is easily achieved in the DC/AC parallel configuration
- The DC/AC inverter can be PV panel integrated (typically at the back), where no centralized inverter is needed, which could lead to easier installation.
- Independent MPPT control could be implemented to maximize the solar energy output for each PV panel.
- Single stage conversion approach (DC/AC inverter between the panel and the grid), which is a potentially higher efficiency system.
- Each DC/AC inverter has its own control, which makes it simple to add and remove panels to the system.
- Absence of high system DC voltage, which eliminates the need to adhere to related stringent NEC requirements.

Disadvantages:

- Higher system cost due to redundant circuitry, such as communication, control, etc.
- More connectors are used in the system, which increases cost and installation time.

1-4-3 AC Series Configuration

One interesting approach, which is being developed at the North Carolina State University's FREEDM Center, is the AC series configuration, which is illustrated in *Fig. 1.8*. The AC series configuration consists of several series PV modules that each includes a DC/AC inverter. The MPP operation of each panel can also be guaranteed with this configuration while modular design is achievable.

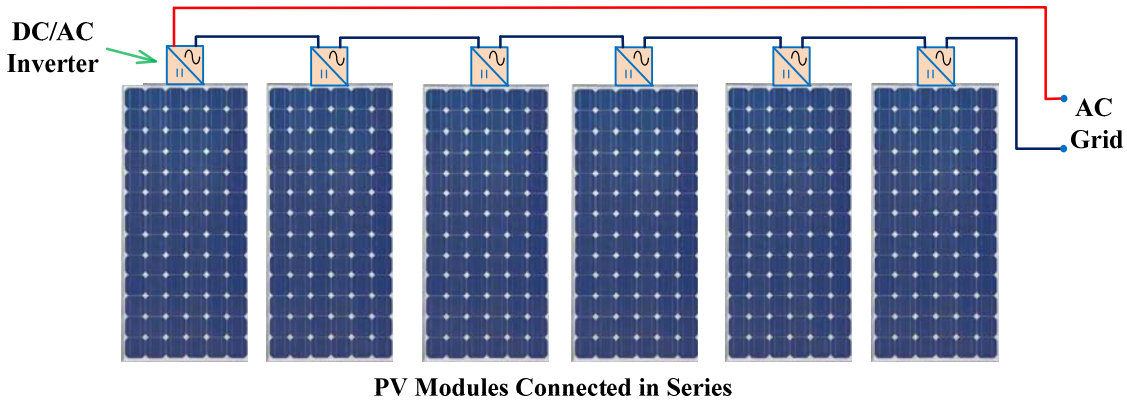


Figure 1.8: AC series configuration.

Advantages:

- The DC/AC inverter can be integrated at the back of the PV panel and no centralized inverter is needed, which would lead to easier installation.
- Independent MPPT control can be employed to maximize the solar energy output for each PV panel.
- Single stage DC/AC inverter can eliminate one stage of power conversion, hence potentially increase the efficiency of the system.
- Series connected modules allow transformerless connection to the grid, which contributes to lowering the cost and an approximate reduction of 1% in electrical losses.

Disadvantages:

- The system is not isolated if the transformerless approach is adopted in the DC/AC inverters.
- The system reliability is reduced due to the series connection configuration.
- The control circuitry is technically more challenging in the AC series approach.

- Potentially low system cost (but higher than the string inverter approach) due to redundant circuitry, such as communication, control, etc.

1-4-4 DC Series Configuration

The DC Series configuration is shown in *Fig. 1.9*. It consists of several series PV modules where each includes a DC/DC converter (optimizer). Unlike the DC Parallel configuration illustrated later in this chapter, the DC Series output voltage is relatively low, which allows for the use of low voltage switching devices. This presents advantages in cost and efficiency. Furthermore, the efficiency is further optimized since each of the DC/DC converters includes its own MPPT function. However, the efficiency is reduced by 1 to 2% due to the need of the 2-stage system, as this configuration requires a DC/AC inverter placed between the panel string and the grid. The market available DC/DC converter products, such as the one provided by Tigo Energy, Incorporation, embed communication circuitry in each of the converters, which communicates with its system gateway and energy management unit.

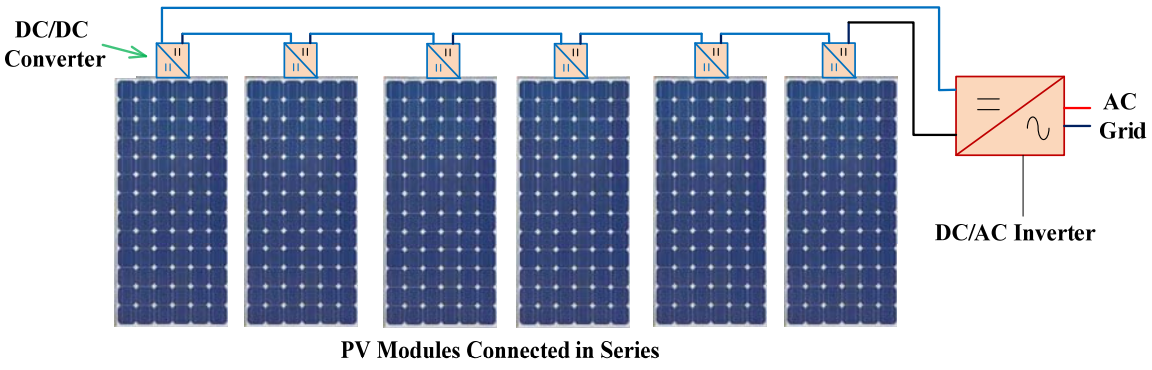


Figure 1.9: DC series configuration.

Advantages:

- Independent MPPT control can be implemented for each PV panel.
- DC/DC converter panel mounted modules are very efficient due to the use of relatively low voltage switching devices.

Disadvantages:

- Power sharing in the series DC/DC converters represents design challenges.
- Uses two-stage architecture. Therefore, some of the efficiency gain at the DC/DC converter module level is lost at the second stage.
- The system reliability is reduced due to the series connection configuration.
- Higher system cost (but lower than the DC/AC parallel approach) due to redundant circuitry, such as communication, control, etc.
- More connectors are used in the system, which increase installation time.

1-5 Proposed System Configuration – Power Electronics

1-5-1 Desirable Residential PV System

From section 1-3 we see that the residential solar system cost reduction is the main driver behind its continuous growth. Furthermore, as of the past few years, the U.S. Department of Energy (DOE) has been funding activities associated with cost reducing the residential solar systems. An example of the related DOE activities is the launch of the SunShot initiative, which includes the residential Plug and Play (PnP) solar system. In 2013, The FREEDM Center at North Carolina State University (NCSU) was awarded a segment of the related grant. In response to the said initiative's cost objectives of a total of $1.50 per Watt for the residential PnP solar system, the FREEDM Center has developed the following

target cost breakdown for the system that would make it possible for the $1.50/W target to be realized. Such cost breakdown is illustrated in *Table 1.4*.

Table 1.4: Residential PnP solar system cost table as developed in 2013 by NCSU FREEDM Systems Center in response to the DOE SunShot initiative grant.

System Details		End of Project Cost Target
PV Module		$0.50
Power Electronics		$0.12
Balance of System	Installation	$0.15
	Racks and Accessories	$0.11
	Permitting	$ -
	Inspection	$ -
	Component Interconnection	$0.05
	Gird Connection	$0.03
	Controls and Interfaces	$0.07
	Overhead (9%)	$0.09
	Profit (25%)	$0.28
	Taxes (7%)	$0.10
TOTAL		**$1.50**

Therefore, an innovative low cost system configuration, along with its innovative low cost components, is anticipated. On the other hand, prior to proposing a new solar system configuration, having in mind that the residential market is the main focus of this research, it is desired to introduce a list of commonsense requirements that would lead to an optimum residential solar system. While there is no such thing as a perfect structure, the desired system would need to meet the following sequentially prioritized list:

1. Safe
2. Low cost
3. Reliable
4. Flexible

5. Scalable
6. Simple to implement and Easy to install

A detailed discussion in relation to the above points in a desired residential PnP PV system will be presented in a later chapter. While an innovative low cost mechanical system is a key element of the PnP system, the focus of this chapter is to introduce the proposed innovative low cost power electronics' system topology and architecture. A low cost mechanical proposal, suitable for the residential PnP PV system is introduced in a later chapter.

1-5-2 Proposed Power Electronics' Configuration – Integrated DC Parallel

From section 1.4 of this chapter, each of the state of the art power electronics' configurations presents advantages and disadvantages. As an introduction to the succeeding chapters, in this section, the DC parallel configuration is introduced. Such an approach, illustrated in *Fig. 1.10*, consists of 4-in-1 or 6-in-1 or 8-in-1 (as suitable for the application) integrated parallel DC/DC converters, where each converter is associated with one PV module. Hence, the MPP operation of each PV panel is optimized. The outputs of the said parallel converters are connected to a proportional second stage DC/AC inverter, which is integrated with the related DC/DC converters in one mechanical enclosure.

While the inverter's function is to transfer the solar energy to the grid, it is proposed to also be designed where its DC input ($V_{DC,IN}$) be regulated to a voltage level slightly higher than the peak of the maximum AC grid voltage that it is connected to, such that $V_{DC,IN} > V_{AC,peak,\max}$. In order to simplify the design of the system, elimination of costly redundant functions needs to be pursued. This could be done by adopting the following

proposal:

1) Provide isolation (where required) in the DC/DC converters, where it is no longer needed in the inverter.
2) All outside communications (from the output of the inverter to the rest of the world) to be incorporated in the inverter and only limit the DC/DC converter's embedded communications, or functions, to:
    a. Enabling start-up and activating shutdown through sensing for the presence of the grid voltage by sensing the presence of the inverter's DC input voltage.
    b. Ability to react to instructions from the inverter, as directed by the utility companies, to perform power curtailment and other as such features.
    c. Since the proposed system is a DC parallel system, sensing the proper operation of each PV panel and/or its related DC/DC converter could easily be done at the inverter's level. Hence, no special communication features need to be provided by the DC/DC converter.
3) Each DC/DC converter to have its own overcurrent and input/output overvoltage protection.

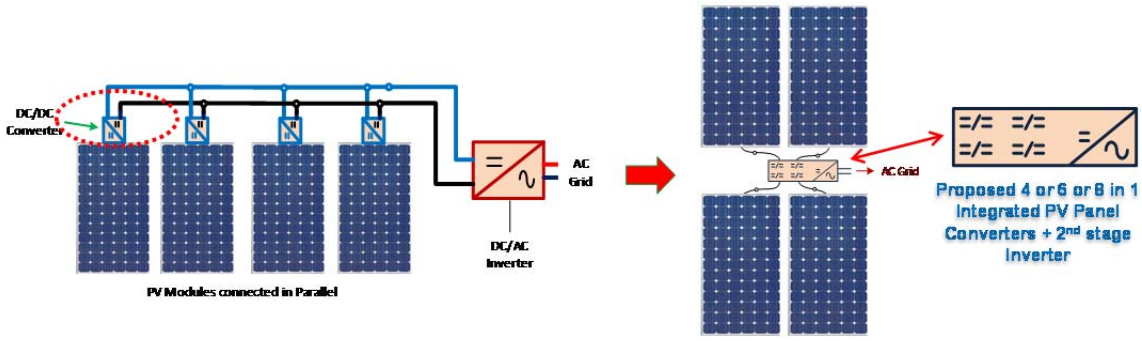


Figure 1.10: Proposed integrated DC parallel configuration.

Advantages:

- The parallel configuration guarantees the high reliability of the PV system.
- The cost of the said integrated configuration is potentially low due to:
  - ✓ Reducing the number of connectors needed for the system
  - ✓ Reducing the number of power electronics' mechanical enclosures
  - ✓ Potentially reducing the number of components related to the power electronics' circuitry and lowering the cost of the employed printed circuit board (PCB)
- Independent MPPT control can be implemented for each PV panel.
- System isolation from the grid is realizable.
- High DC voltage is not exposed. Hence, eliminating the need for meeting related stringent NEC requirements.
- Each DC/DC converter has its own control and plug-and-play can be realized easier.

Disadvantages:

- In the absence of circuit innovations, higher system cost is a concern since the DC/DC converter is needed for each PV panel.
- The efficiency of the system suffers due to the two stage architecture.

The residential PnP PV system illustrated in the remaining chapters, proposes novel solutions to each of the above disadvantages. In order for the power electronics to be low cost, the DC/DC converter design needs to be innovative and supportive to the implementation of straightforward second stage DC/AC requirements. Furthermore, since this is a two-stage system, it is imperative to come up with an innovative high efficient DC/DC converter design. Hence, the low cost and the efficiency of the panel side DC/DC inverter, in this proposed DC/DC parallel configuration approach, becomes a major research

target and is the focus and scope of the power electronics' design in this dissertation.

1-6 Conclusion

In this chapter, an introduction to illustrate the trend and progress of renewable energy generation performed in the United Stated and worldwide is presented. A major factor behind the headway of solar installations in the U.S. residential market is related to cost. The U.S. residential solar market has seen steady growth, up 45% over the second quarter of 2013, where over 100 MWdc were installed in the second quarter of 2014, without any state incentive.

Furthermore, major PV solar system architectures that are currently utilized in residential and commercial applications were presented in this chapter, where the advantages and disadvantages of each were introduced. Moreover, a low cost DC/DC parallel system configuration was proposed, which introduced the scope of work of the power electronics' innovative scheme that is detailed in a later chapter of this dissertation.

Chapter 2: Operation Principle of a Novel Low Cost PV Converter Based on Analog Interleaving Method

2-1 Overview

In this chapter, a novel simplified low cost analog implementation of a master/slave methodology resulting in efficient soft-switched interleaved variable frequency flybacks, operating in the boundary conduction mode (BCM), is presented [5]. The scheme is suitable for PV converters or micro-inverters as well as other applications such as battery chargers. The method is adaptive to high ratio of input and output voltages as well as output load variations. The circuit allows for master/slave synchronization while copying the ON time of the master flyback to the slave one, which result in component count and cost reductions.

The adopted discrete analog implementation utilizes a drive winding embedded in the master flyback transformer, which also controls the start of the ON time of the slave flyback. Hence, a voltage control oscillator (VCO) method is embraced. Such technique helps simplify the control and reduces the losses of the drive circuits while eliminating the need for an auxiliary startup supply. Furthermore, in addition to enabling the use of lower voltage rating switching devices, benefits also include soft switching, output rectifiers' zero current switching, isolation, reduced input current and output voltage ripples, and output voltage and input power detection for phase shading implementation. Operation procedure, design equations and considerations are presented in this chapter. Experimental results, illustrating the implementation simplicity of the scheme at low cost, are demonstrated in chapter 6.

2-2 Prior Arts

The flyback topology is a popular topology due to its minimal magnetic and semiconductor components' requirement while providing isolation. It has been researched and used in applications such as PC adapter, LED powering [6], solar [7-13], off-line converters, as well as many others. It is generally a low cost approach but it is mostly used in low power applications primarily due to the high current stresses on its switching device(s), output rectifier(s), and capacitors. However, interleaving the flyback inverter (or converter) [12-15] facilitated the use of the topology in higher power applications.

References [12-13] present control methods for photovoltaic (PV) grid-tied-interleaved flyback micro-inverters where [12] focuses on achieving high efficiency in a wide load range and [13] proposes a leak inductance energy recovery circuit. Both methods [12-13] implement 180° phase shift control strategies. While [12] promotes operating in the discontinuous conduction mode (DCM), which is suitable for a lower power level than that of the boundary conduction mode (BCM), [13] emphasizes operating in BCM while implementing a resonant zero voltage switching (ZVS) technique. References [14-15] propose adding an auxiliary inductor, shunted between the output rectifiers, in order to reduce its reverse recovery losses while achieving ZVS in the active switches. Furthermore, burst-mode operation is used at light load conditions [14]. Moreover, [16] proposes a multi-mode IC control scheme for its soft-switched flyback converter to achieve load regulation with 80% efficiency at 2.5W and 88.8% at full load, while [17] proposes an interleaved flyback DC/DC converter using a common clamp capacitor where all components and devices are ideal. The benefit of the method used is that it recycles the transformer leakage inductance energy and reduces voltage stress of the power switches.

Methods proposed in the above referenced papers involve relatively costly and complex control schemes, especially when featuring interleaving. Other references propose fixed frequency continuous conduction mode of operation (CCM). CCM typically presents significant challenges in reaching main switching device's turn ON soft switching. On the other hand, reverse recovery issues of the output rectifiers are inherent in flybacks operating at CCM. Furthermore, current methods use either costly digital controllers, which offer design flexibility, or mixed controllers in order to implement flyback interleaving [18].

In this chapter, a novel scheme that is simple and relatively easy-to-implement, low cost and efficient soft-switched interleaved variable frequency flybacks, operating in BCM, is proposed. The proposal offers analog implementation, which features higher bandwidth and faster responses to input and output changes, at a significantly lower cost. In later chapters, it will be proven that considerably less component count as well as the ability to use a 2-sided printed circuit board (PCB) is achievable in the analog implementation pursued.

The circuit allows for master/slave synchronization while copying the ON time of the master flyback to the slave one. The main switching device ON and OFF circuits are separated and utilize a drive winding embedded in the master flyback transformer, which also controls the start of the ON time of the slave flyback. Such technique helps simplify the control and reduce the losses of the drive circuits. Furthermore, as further detailed in a later chapter, the scheme allows for the use of lower voltage rating main switching devices, where experimental results were achieved by using 80V rated MOSFETs with applied input voltage up to 45V. 150V and higher rated MOSFET devices are currently used in the micro-inverter PV market. Consequences of using lower voltage rated MOSFET devices typically result in reducing cost while decreasing the devices' ON resistance ($r_{ds,on}$) and gate charge

requirements. Moreover, in order to boost the efficiency, phase shading is implemented at light load. The execution of the proposed method was implemented by using discrete analog components, which significantly reduces cost.

2-3 Configuration and Operation Principle of the Proposed Circuit

2-3-1 Scheme Concept and Circuit Configuration

In *Fig. 2.1*, the proposed scheme concept is displayed, which illustrates its simplicity. Once the reference voltage (V_{REF}) is attained through any desired control scheme – MPPT, voltage regulation, or any other application driven control methodology, the master/slave operation is established in the following sequence:

1. V_{REF} is compared to the master flyback's ramp (V_{Ramp1}).
2. The ramping start point of V_{Ramp1} occurs at the master flyback's zero-current-detection (ZCD). The ramp up duration of V_{Ramp1} is defined as t_{Ramp1}.
3. After reaching the zero-voltage-crossing delay set point, the master gate drive (T_{ON1}) becomes high during t_{Ramp1}.
4. Once T_{ON1} is terminated, the slave flyback's ramp (V_{Ramp2}) increases to reach V_{REF} with a duration (t_{Ramp2}), where:

$$t_{Ramp1} \approx t_{Ramp2} \tag{1}$$

5. The slave gate drive (T_{ON2}) is high during t_{Ramp2}; hence a copy of the T_{ON1} is established:

$$t_{ON1} \approx t_{ON2} \tag{2}$$

A detailed illustration of the scheme's operation principle and theoretical waveforms are presented in section 2-3-2 of this chapter.

In *Fig. 2.2*, the proposed simplified interleaving circuit configuration is illustrated, which consists of two flyback inverters (or converters). The top flyback, referred to as the master flyback in the remainder of this document, consists of transformer T_1, MOSFET Q_1, and output rectifier D_1. The bottom flyback, referred to as the slave flyback, comprises of transformer T_2, MOSFET Q_2, and output rectifier D_2. Furthermore, T_1 includes an additional winding, which serves as the drive winding for both Q_1 and Q_2. Moreover, the block labeled *"Q_1 Turn ON Circuit"* includes a soft-switching circuit based on delaying the start of the Q_1 ON time until its drain voltage reaches zero-volt-switching (ZVS) or the quasi-resonant voltage switching (more on this later in this chapter).

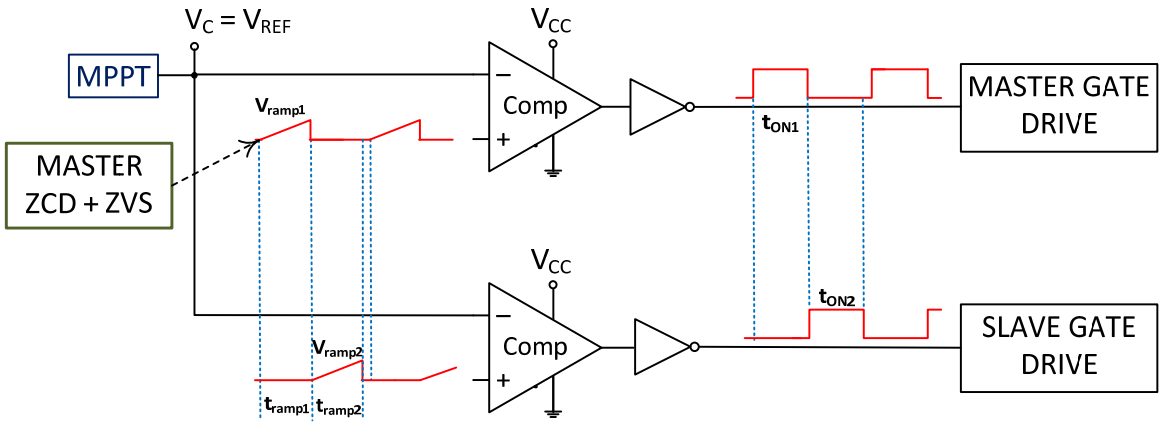


Figure 2.1: Proposed scheme concept [5].

On startup, in lieu of requiring an auxiliary power source, R_1, a relatively high impedance resistor designed for minimum dissipation, charges capacitor C_1 to a voltage level sufficient to trigger the startup circuit. Such circuit provides the voltage source needed for activating the master and slave flybacks' ramp circuits. Furthermore, the drive winding

discharges C_{Ramp1} and C_{Ramp2} via the ramp reset circuit blocks *"Ramp Reset Circuit 1"* and *"Ramp Reset Circuit 2"* shown in *Fig. 2.2*. Moreover, blocks labeled as *"Q1 Turn ON Circuit," "Q1 Turn OFF Circuit," "Q2 Turn ON Circuit,"* and *"Q2 Turn OFF Circuit"* are also illustrated in *Fig. 2.2*. The scheme purposely separates the ON and OFF circuits due to the following considerations:

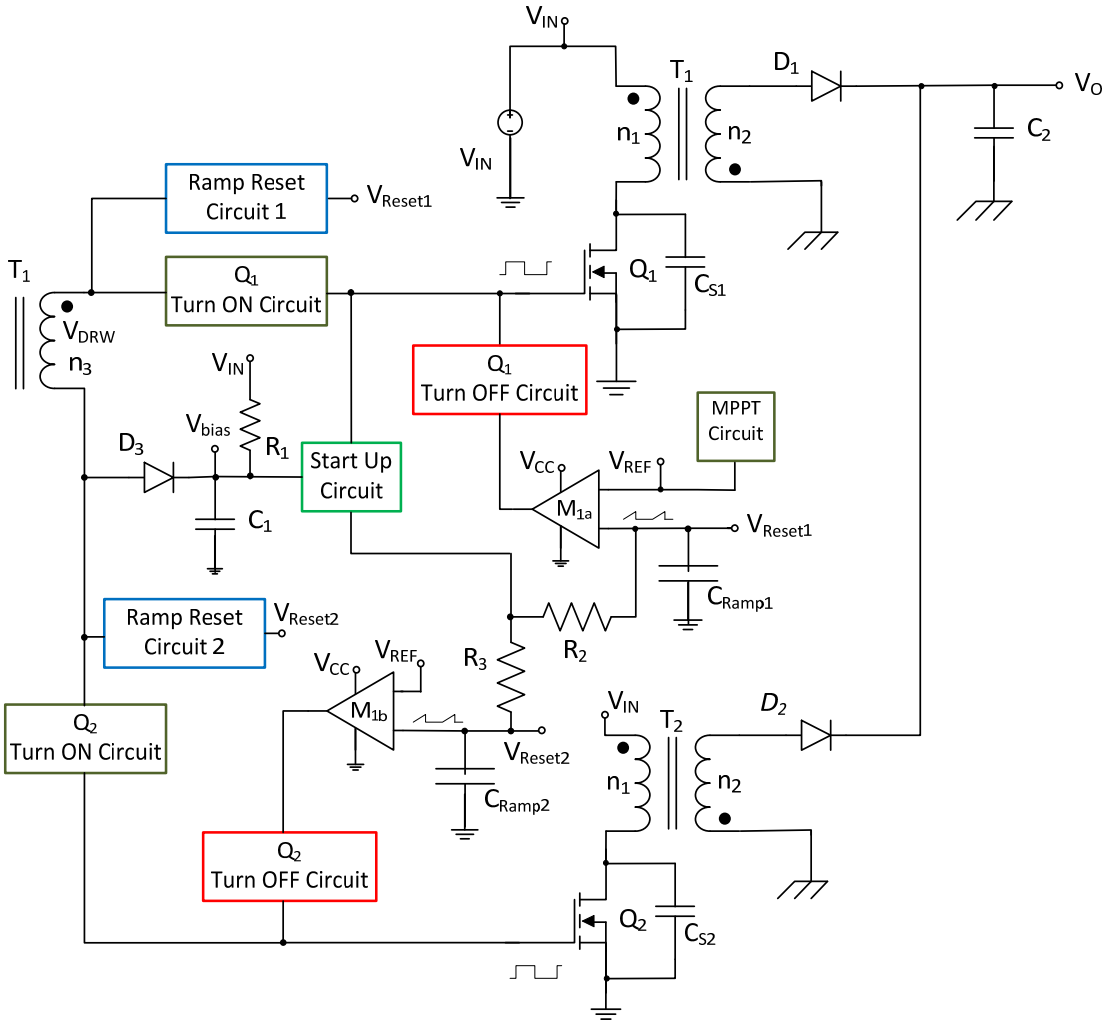


Figure 2.2: Novel Low Cost PV Converter (or Micro-Inverter) Based on Analog Interleaving Method [5].

1. Typically, the OFF circuit is required to insure an ultra-fast turn OFF to the main switching device, which is exemplified as a MOSFET in *Fig. 2.2*.

2. However, in each cycle, the said MOSFET's current starts from zero in a flyback BCM operation.
3. Hence, the rise time of the said MOSFET's gate drive voltage (V_{GS}) is not required to be ultra-fast.
4. Therefore, the OFF and ON circuits are purposely separated, which would result into less gate drive power dissipation.

2-3-2 Operation Principle and Theoretical Waveforms

In one switching cycle, the theoretical waveforms are illustrated in *Fig. 2.3*. Once the master's zero current detection (ZCD) is reached at t_0, during the interval $t_0 < t < t3$, the drive winding holds capacitor C_{Ramp2} down while allowing capacitor C_{Ramp1} to be charged with a time constant equal to the product of R_2 and C_{Ramp1}, as illustrated in *Fig. 2.2*. At this interval, the dot end of the drive winding voltage (v_{DRW}), which is in phase with the primary winding of T_1, becomes positive to a value proportional to the input voltage and the ratio of n_3 and n_1, where:

$$v_{DRW} = V_{IN} \frac{n_3}{n_1} \tag{3}$$

Similarly, the soft-switching delay circuit is activated at t_0. The timing in the delay circuit is designed to be equal to half of T_1's magnetizing and leakage inductances' resonance with the combined capacitance at the node of Q_1's drain [19]. Since the magnetizing inductance (L_{m1}) is typically much larger than the leakage inductance (L_{l1}), only L_{m1} will be considered. Likewise, Q_1's C_{oss} and the snubber ($C_{snubber}$) capacitances are normally dominant at the drain node of Q_1; hence, let C_{S1} be the equivalent capacitance at the drain

node of Q_1. Therefore, the parasitic winding capacitance and other capacitances at that node are ignored. Hence,

$$C_{S1} \approx C_{oss} + C_{snubber} \tag{4}$$

Furthermore, to reach ZVS (or quasi-resonant voltage switching occurring at V_{IN} - V_{REFL}, where V_{REFL} is the reflected voltage from the secondary to the primary and if designed to be less than V_{IN}), Q_1's turn ON should occur at half of t_{RES}, at the resonance minimum end. Let t_{OFF2} be at half of the resonant time (t_{RES}), equation (5) provides a very close approximation for t_{RES} at the said node.

$$t_{RES} \approx 2\pi\sqrt{L_{m1}C_{S1}} = 2t_{OFF2} \tag{5}$$

Assuming that the forward voltage drops of the output rectifiers (D_1 and D_2) are approximately equal, where:

$$V_{D1} \approx V_{D2} \tag{6}$$

Hence, V_{REFL} is given in equation (7):

$$V_{REFL} = \frac{n_1}{n_2}(V_{D1} + V_O) \approx \frac{n_1}{n_2}(V_{D2} + V_O) \tag{7}$$

On the other hand, the switching cycle (T_s) is given in equation (8), where, t_{ON1} is the ON time of Q_1 (as defined earlier in this chapter), t_{OFF1} is the time while the energy is being delivered to the load, and f is the switching frequency. Hence;

$$T_s = t_{ON1} + t_{OFF1} + t_{OFF2} = \frac{1}{f} \tag{8}$$

Let δ_1 be the duty cycle of the master, δ_1' be the ratio of t_{OFF1} over T_s, and δ_1'' be the ratio of t_{OFF2} over T_s. Hence;

$$\delta_1 = \frac{t_{ON}}{T_s} = t_{ON} f \tag{9}$$

$$\delta_1' = \frac{t_{OFF1}}{T_s} = t_{OFF1} f \tag{10}$$

$$\delta_1'' = \frac{t_{OFF2}}{T_s} = t_{OFF2} f = \frac{t_{RES}}{2} f = \pi f \sqrt{L_{m1} C_{S1}} \tag{11}$$

And,

$$\delta_1 + \delta_1' + \delta_1'' = 1 \tag{12}$$

From (9) and from the volt-second balance equation (more on this in section 2-3-3), neglecting the voltage drops across the MOSFET's drain to source during the ON time and across the output rectifier while forward biased, we have:

$$\frac{V_O}{V_{IN}} = \frac{n_2}{n_1} \frac{\delta_1}{\delta_1'} = \frac{n_2}{n_1} \frac{\delta_1}{(1 - \delta_1 - \delta_1'')} \tag{13}$$

Hence the duty cycle (δ_1) is achieved by manipulating equations (5), (7), and (13):

$$\delta_1 = \frac{V_{REFL}(1 - \delta_1'')}{V_{IN} + V_{REFL}} = \frac{V_{REFL}(1 - \pi f \sqrt{L_{m1} C_{S1}})}{V_{IN} + V_{REFL}} = (f)(t_{ON}) \tag{14}$$

The duty cycle (δ_2) of the slave flyback is simply a copy of δ_1 .

Q_1's ON time starts at t_1. Since Q_1's drain current (i_{DS1}) ramps from zero at t_1, and since the proposed scheme separates the ON and OFF circuits, there is no need for the current provided to charge Q_1's gate to be high. This results into less power dissipation, especially at light load. At t_3, V_{Ramp1} reaches the reference voltage (V_{ref}) set by the control circuit (MPPT, etc.) and the Q_1 OFF circuit is activated, which results into polarity change of the drive winding. At this instant, the Q_2 ON circuit is activated and Q_2 gate drive is established via the said drive winding. Also at t_3, C_{Ramp2} starts charging until V_{Ramp2} reaches the same V_{ref} at t_5, which activates the Q_2 OFF circuit.

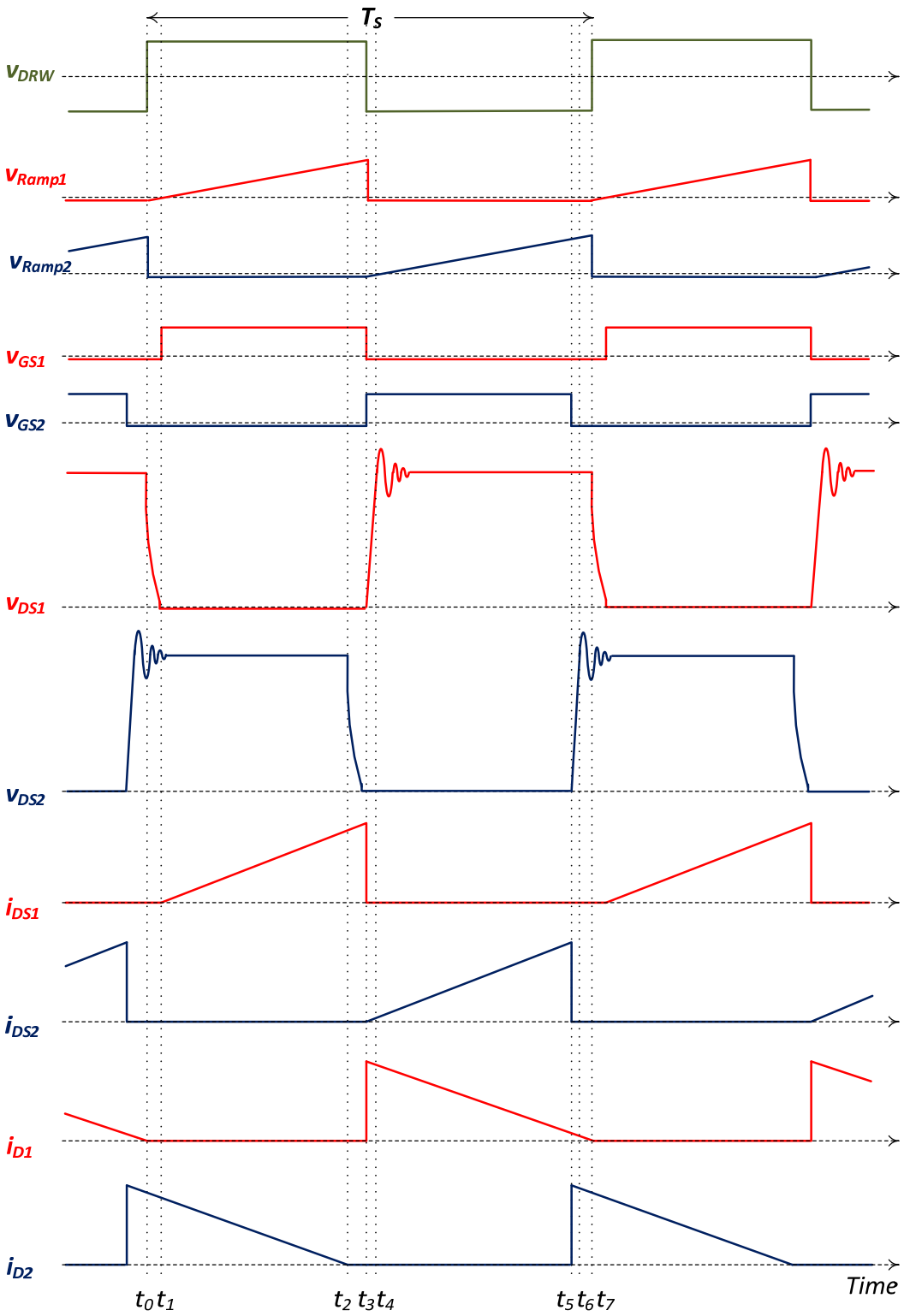


Figure 2.3: Detailed operation of the proposed scheme [5].

Once T_1 releases all its stored energy, during Q_1's ON time, i_{D1} goes to zero and a new cycle start. During the OFF time of Q_1 and Q_2, in addition to the ringing voltage caused by the uncoupled energy due to the primary winding leakage inductance and parasitic capacitances, for each T_1 and T_2, the drain to source voltages are given in equation (15):

$$V_{DS1} \approx V_{DS2} \approx V_{IN} + \frac{n_1}{n_2}(V_o + V_{D1}) \approx V_{IN} + \frac{n_1}{n_2}(V_o + V_{D2}) \tag{15}$$

2-3-3 Design Equations

In a basic BCM flyback configuration, illustrated in *Fig. 2.4*, transformer T_1 balance and other relevant design equations are derived in this section. *Fig. 2.5(a)* illustrates the basic flyback configuration during t_{ON}, while *Fig. 2.5(b)* and *Fig. 2.5(c)* display the relevant circuits during t_{OFF1} and t_{OFF2} (half of t_{RES}) respectively.

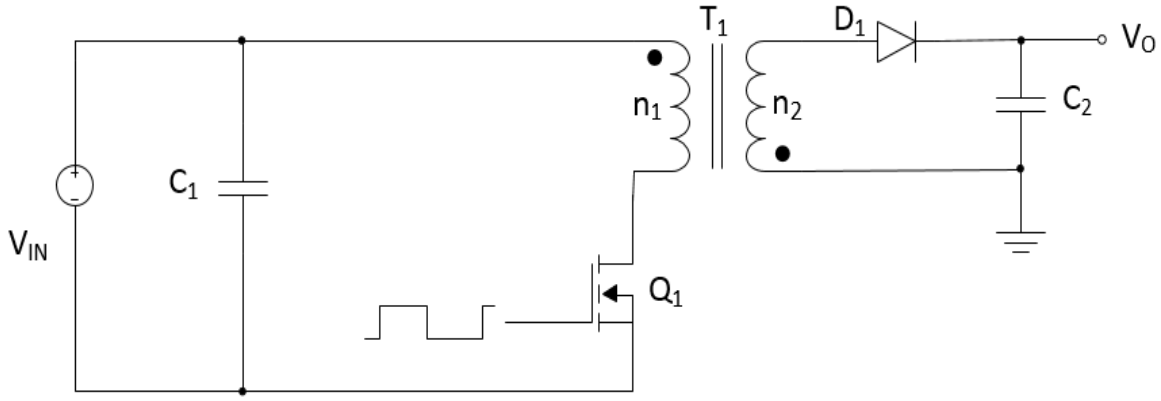


Figure 2.4: BCM flyback basic configuration.

During the interval t_{ON}:

The primary magnetizing inductance stores energy while the output rectifier (D_1) is back biased. From *Fig. 2.5(a)*,

$$v_L = V_{IN} - V_{Q1,ON} \tag{16}$$

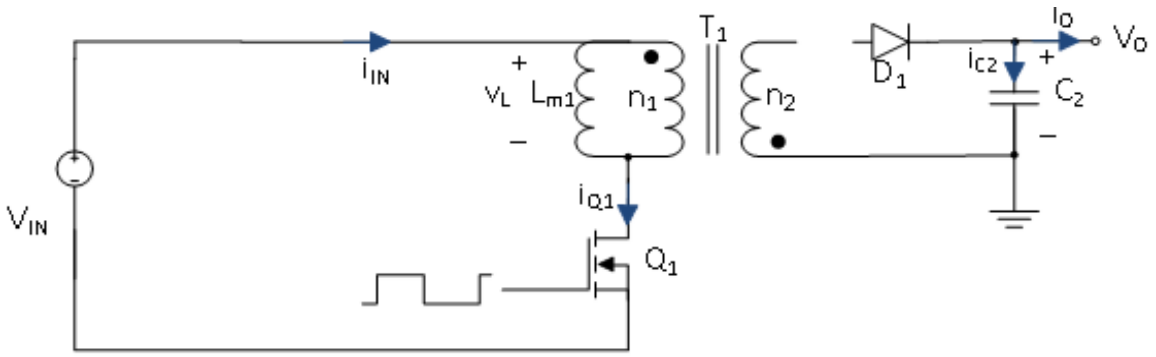


Figure 2.5(a): BCM flyback basic configuration during t_{ON}.

Where V_L is the voltage across T_1's primary winding and V_{Q1} is the voltage drop across Q_1 during t_{ON}. Furthermore, during t_{ON}, the input current is equal to the drain current of Q_1 and the output capacitor current is given below:

$$i_{IN} = i_{Q1} \tag{17}$$

$$i_{C2} = -I_o \tag{18}$$

During the interval t_{OFF1}:

The energy stored during t_{ON} is transferred to the output via D_1 and the output voltage is reflected to the primary winding. Hence, from *Fig. 2.5(b)*,

$$v_L = -\frac{n_1}{n_3}(V_O + V_{D1}) \tag{19}$$

Furthermore,

$$i_{IN} = 0 \tag{20}$$

And,

$$i_{C2} = i_{D1} - I_o \tag{21}$$

The output rectifier's current, which is equal to the secondary current (i_S), is given in equation (22), where i_P is the primary current.

$$i_S = i_{D1} = \frac{n_3}{n_1} i_P \tag{22}$$

Hence, (21) becomes:

$$i_{C2} = \frac{n_3}{n_1} i_P - I_O \tag{23}$$

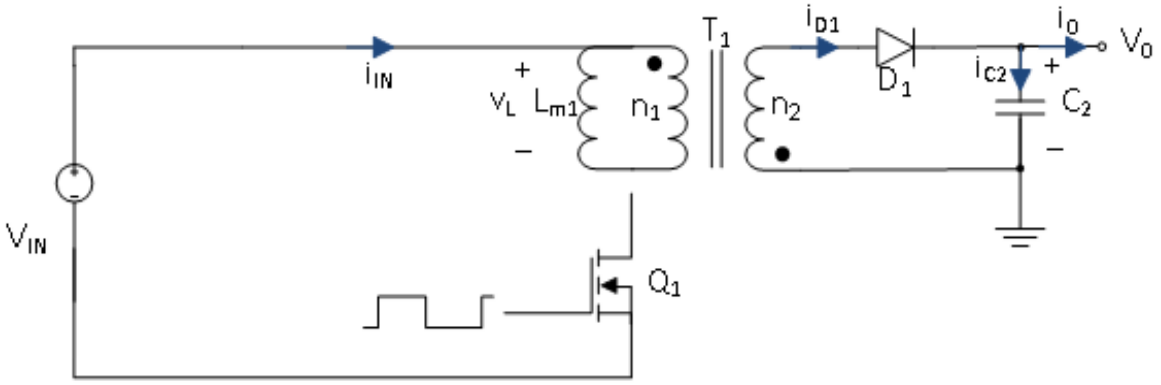


Figure 2.5(b): BCM flyback basic configuration during t_{OFF1}.

During the interval t_{OFF2}:

As described earlier in this chapter, t_{OFF2} is defined as half of T_1's magnetizing and leakage inductances' resonance with the combined capacitance at the node of Q_1's drain. Rewriting equation (5), an expression for t_{OFF2} is achieved:

$$t_{OFF2} = \frac{1}{2} t_{RES} = \pi \sqrt{L_{m1} C_{S1}} \tag{24}$$

As illustrated in *Fig. 2.5(c)*, neither Q_1 nor D_1 are conducting during this period. Hence,

$$v_L = 0 \tag{25}$$

$$i_{IN} = 0 \tag{26}$$

$$i_{C2} = -I_o \tag{27}$$

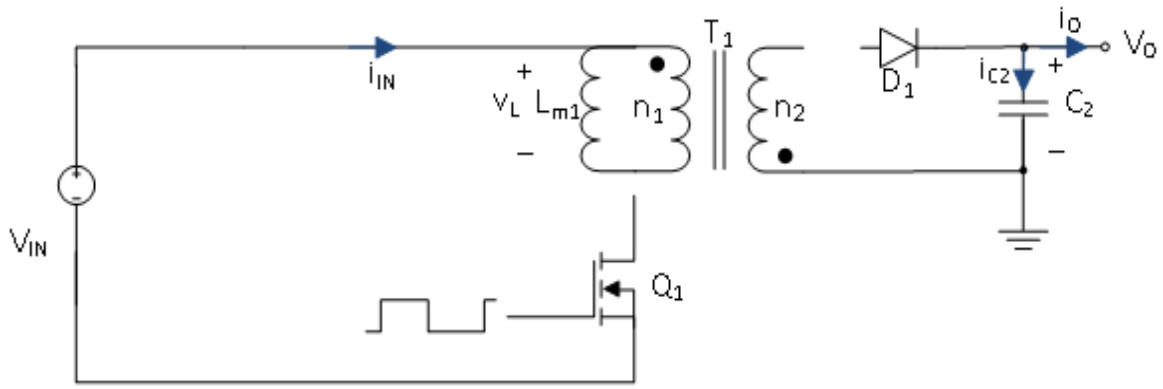


Figure 2.5(c): BCM flyback basic configuration during t_{OFF2}.

Fig. 2.6 illustrates the current waveforms of the primary and secondary of transformer T_1 during the period T_S. I_{PP} is defined as the peak primary current and I_{SP} is the peak secondary current. During the t_{ON} interval, with a proper transformer design, the primary current increases linearly from zero to I_{PP}. Throughout such interval, the voltage across the primary winding is $V_{IN} - V_{Q1,ON}$. Therefore;

$$I_{PP} = \frac{(V_{IN} - V_{Q1,,ON})t_{ON}}{L_{m1}} \tag{28}$$

Furthermore, the energy stored in the primary inductance of transformer T_1 (W_P) during t_{ON} is given by:

$$W_P = \frac{1}{2} L_{m1} (I_{PP})^2 \tag{29}$$

Since the input power (P_{IN}) is a function of the energy and the operating frequency, where;

$$P_{IN} = W_P f \tag{30}$$

Consequently,

$$P_{IN} = \frac{1}{2} L_{m1} (I_{PP})^2 f \tag{31}$$

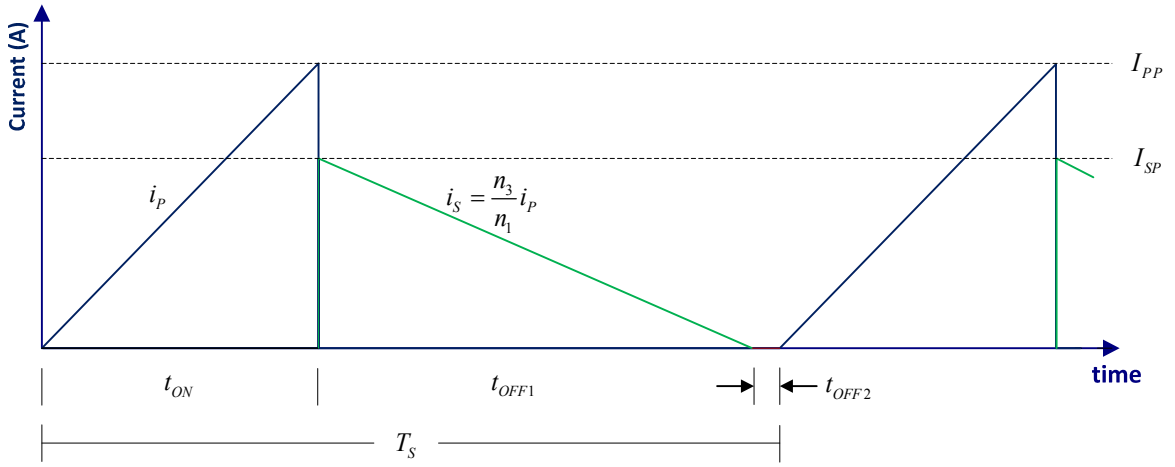


Figure 2.6: BCM flyback primary and secondary current waveforms.

Combining equations (28) and (31) leads to an expression for the input power in terms of the operating frequency, input voltage, ON time of *Q1*, and the primary inductance:

$$P_{IN} = \frac{f(V_{IN} - V_{Q1,ON})^2 (t_{ON})^2}{2L_{m1}} \tag{32}$$

Equation (32) could also be rewritten as an expression for t_{ON}:

$$t_{ON} = \frac{1}{(V_{IN} - V_{Q1,ON})} \sqrt{\frac{2L_{m1}P_{IN}}{f}} \tag{33}$$

On the other hand, *Fig. 2.7* illustrates the primary winding voltage waveform.

It is inherent that the core of the transformer in a flyback operating in the boundary conduction mode resets to zero during each cycle. For the reset to occur, equal volt seconds must be applied to the core during the ON and OFF times of *Q1*. Therefore, from the volt-second balance equation, where the primary winding voltage (v_L) is approximated to zero during t_{OFF2}, hence;

$$\delta_1(V_{IN} - V_{Q1,ON}) - \delta_1' V_{REFL} + \delta_1''(\approx 0) = 0 \tag{34}$$

Manipulating equations (13) and (34);

$$\delta_1 = \frac{V_{REFL}(1-\delta_1'')}{V_{IN}+V_{REFL}-V_{Q1,ON}} \tag{35}$$

Therefore, an expression for the duty cycle (δ_1) is achieved by combining equations (11) and (35);

$$\delta_1 = \frac{V_{REFL}\left(1-\pi f\sqrt{L_{m1}C_{S1}}\right)}{V_{IN}+V_{REFL}-V_{Q1,ON}} = (f)(t_{ON}) \tag{36}$$

Hence,

$$t_{ON} = \frac{V_{REFL}\left(1-\pi f\sqrt{L_{m1}C_{S1}}\right)}{f(V_{IN}+V_{REFL}-V_{Q1,ON})} \tag{37}$$

Combining equations (33) and (37):

$$2L_{m1}P_{IN}f\left(V_{IN}+V_{REFL}-V_{Q1,ON}\right)^2 = V^2{}_{REFL}\left(V_{IN}-V_{Q1,ON}\right)^2\left(1-\pi f\sqrt{L_{m1}C_{S1}}\right)^2 \tag{38}$$

Since typically;

$$1 \gg \pi f\sqrt{L_{m1}C_{S1}} \tag{39}$$

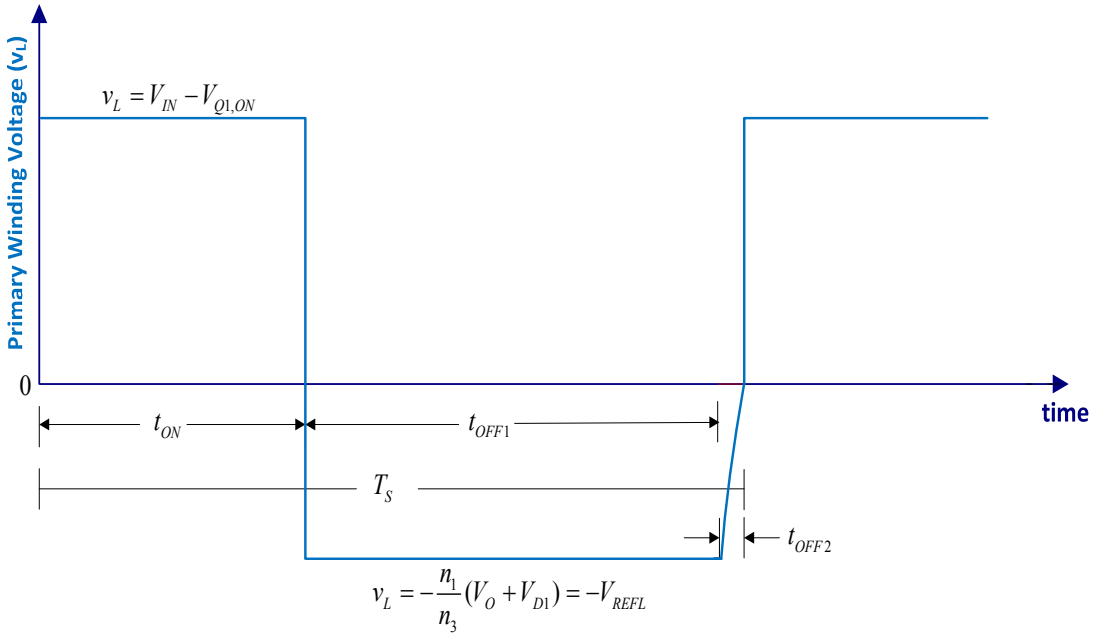


Figure 2.7: BCM flyback primary winding voltage waveform.

An approximate solution for L_{m1} may be achieved by neglecting the term $\pi f\sqrt{L_{m1}C_{S1}}$.

Therefore,

$$L_{m1} \approx \frac{(V_{REFL})^2 (V_{IN} - V_{Q1,ON})^2}{2fP_{IN}(V_{IN} + V_{REFL} - V_{Q1,ON})^2} \geq L_{m2} \tag{40}$$

Furthermore, $V_{Q1,ON}$ is defined as:

$$V_{Q1,ON} = r_{DS,ON}(i_{D,RMS}) \tag{41}$$

Where, $i_{D,RMS}$ is Q_1's RMS drain current and $r_{DS,ON}$ is the ON resistance of Q_1, which is typically in the few milliohms. Therefore, $V_{Q1,ON}$ is usually insignificant compared to V_{IN} and could be ignored in all derived equations listed in this document. Hence equation (40) could be rewritten, such that;

$$L_{m1} \approx \frac{(V_{REFL}V_{IN})^2}{2fP_{IN}(V_{IN} + V_{REFL})^2} \geq L_{m2} \tag{42}$$

Or,

$$f \approx \frac{(V_{REFL}V_{IN})^2}{2L_{m1}P_{IN}(V_{IN} + V_{REFL})^2} \tag{43}$$

However, if a more accurate expression for f is desired, a solution for equation (38) is required, such that;

$$f_1 = \frac{-B + \sqrt{B^2 - 4AC}}{2A} \tag{44}$$

$$f_2 = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \tag{45}$$

Where;

$$A = \pi^2 L_{m1} C_{S1} \tag{46}$$

$$B = -\left[\left(\frac{2L_{m1}P_{IN}(V_{IN} + V_{REFL} - V_{Q1,ON})^2}{(V_{REFL})^2 (V_{IN} - V_{Q1,ON})^2}\right) + 2\pi\sqrt{L_{m1}C_{S1}}\right] \tag{47}$$

$$C = 1 \tag{48}$$

Since f_1 given in equation (44) does not converge, such that:

$$\lim_{C_{S1} \to 0} f_1 \to \infty \tag{49}$$

While f_2 given in equation (45) does converge to the value of f derived in equation (43), such that:

$$\lim_{C_{S1} \to 0} f_2 \to f \tag{50}$$

Hence, f_2 is the viable solution for equation (38):

$$f = f_2 = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \tag{51}$$

Where A, B, and C are defined in equations (46), (47), and (48).

Frequency equations for the BCM flyback are previously referred to, as shown in [16]. However, the one illustrated in (51) is more accurate and is in the terms of normally specified parameters, such as the input voltage (V_{IN}) and the input power (P_{IN}). Other elements shown in (51) could easily be selected or calculated, as it will be further discussed in chapter 3.

On the other hand, an equation for the peak primary current is obtained by combining equations (28), (32), and (40) while neglecting $V_{Q1,ON}$;

$$I_{PP} \approx \sqrt{\frac{2P_{IN}}{fL_{m1}}} \tag{52}$$

Furthermore, I_{PP} could also be expressed in terms of V_{IN} and V_{REFL} by combining equations (42) and (52);

$$I_{PP} \approx 2P_{IN}\left(\frac{V_{IN} + V_{REFL}}{V_{IN}V_{REFL}}\right) \tag{53}$$

Equation (53) is very useful since it is independent of the operating frequency (f) and the primary inductance (L_{m1}) of transformer T_1. Additionally, (53) indicates that I_{PP} increases as V_{REFL} decreases. More equations to include the RMS value for the primary and secondary currents are derived in the next chapter.

2-3-4 Operating Frequency vs. Q_1's Drain Node Capacitance

Equation (51) provides a relation between the boundary conduction mode (*BCM*) flyback's operating frequency (f) and the capacitance at the drain node of Q_1 (C_{S1}). *Fig. 2.8* illustrates the effect of C_{S1} on f, as multiple values for C_{S1} are assumed. Note that when C_{S1} is approaching zero (except for zero), f converges to the value provided by equation (43), which is a 100 kHz by using the parameters provided in the example below.

As a design example, let $L_{m1} = 4.5\mu H$; $V_{REFL} = V_{IN} = 30V$; $P_{IN} = 250\ W$. From *Fig. 2.8*, we see that C_{S1} could have a significant effect on the operating frequency of a *BCM* flyback. This is especially true as it is typical to increase C_{S1} in power electronics' soft-switching designs and practices, aiming to reduce the switching losses. A value of 10nF for C_{S1} is a reasonable assumption in today's related applications. Furthermore, it is worth noting that C_{S1} contributes to reducing the voltage spike seen at Q_1's and Q_2's drain to source at turn OFF. Such voltage spikes are caused primarily by the leakage inductances of T_1 and T_2 respectively.

Moreover, from *Fig. 2.8*, with $C_{S1}=10nF$, f is reduced from a value of a 100 kHz (if C_{S1} is ignored) to around 88.55 kHz (when C_{S1} is considered). This represents an 11.45%

decrease of the operating frequency, when comparted to results achieved by equation (43). This is due to t_{OFF2}, which is caused by C_{S1} and the parameters revealed in equation (24).

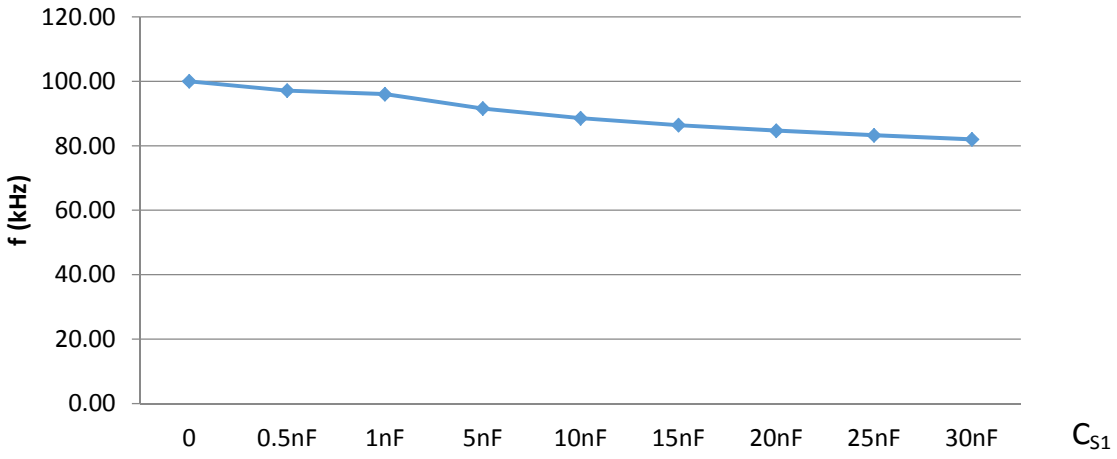


Figure 2.8: BCM flyback operating frequency versus Q_1's drain node capacitance.

2-3-5 Operating Frequency vs. Input Power

Based on equations (43) and (51), the operating frequency in a variable frequency BCM flyback changes with the input voltage and power. The maximum operating frequency (f_{max}) occurs at maximum input voltage ($V_{IN,max}$) and at minimum input power ($P_{IN,min}$). Correspondingly, the minimum operating frequency (f_{min}) occurs at minimum input voltage ($V_{IN,min}$) and maximum input power ($P_{IN,max}$). On the other hand, if we ignore the Q_1's drain node capacitance (C_{S1}), hence using equation (43) in order to determine the operating frequency, we reach a value for f that is linearly inverse proportional to P_{IN}.

As a design example, which was demonstrated experimentally, let $L_{m1} = 15\mu H$; $V_{REFL} = V_{IN} = 30V$; and $C_{S1} \approx$ 10nF. Equation (43) indicates that f decreases 10:1 (300 kHz to 30 kHz) as P_{IN} increase 10:1 (25W to 250W). However, as demonstrated in *Fig. 2.9*, equation (51) provides a much closer approximation to the lab's experimental results. Furthermore, in

this example, the frequency variations, based on equation (51) is approximately 6.5:1 (182 kHz to 28 kHz) while it was 6.26:1 (174 kHz to 27.8 kHz) when compared to the experimental results.

The slight difference between the experimental results and the calculations achieved based on equation (51), is due to component tolerances as well as corrections for the approximations made while deriving (51). Such made approximations include ignoring the winding capacitances. This would partially explain why the measured frequencies are actually slightly smaller than the results calculated using equation (51), as C_{S1} is essentially somewhat larger once the winding capacitances were to be included.

It is worth noting that it is typical to have lower losses at lower operating frequencies. Hence, C_{S1} provides several benefits that are summarized as follows:

1. Clamps the overshoot voltage at the drain of the employed switching MOSFET(s)
2. Act as a snubber by slowing down the drain to source voltage rise at turn OFF.
3. Limits the operating frequency increase at light load, which results into lower switching losses.

On the other hand, it is sometimes desirable to have equations in terms of the output power (P_O), output voltage (V_O), and/or the output load current (I_O). This is easily accomplished by realizing that the output power is a function of the input power and the efficiency (η), where:

$$P_O = \eta P_{IN} \tag{54}$$

The output load (I_O) is a function of P_O, where:

$$I_O = \frac{P_O}{V_O} \tag{55}$$

Hence, equation (43) could be rewritten as:

$$f \approx \frac{\eta \left(V_{REFL} V_{IN}\right)^2}{2L_{m1} P_O (V_{IN} + V_{REFL})^2} \approx \frac{\eta \left(V_{REFL} V_{IN}\right)^2}{2L_{m1} V_O I_O (V_{IN} + V_{REFL})^2} \tag{56}$$

And, equation (51) becomes:

$$f = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \tag{57}$$

Where,

$$A = \pi^2 L_{m1} C_{S1} \tag{58}$$

$$C = 1 \tag{59}$$

$$B = -\left[\left(\frac{2L_{m1} P_O (V_{IN} + V_{REFL} - V_{Q1,ON})^2}{\eta (V_{REFL})^2 (V_{IN} - V_{Q1,ON})^2}\right) + 2\pi\sqrt{L_{m1} C_{S1}}\right] \tag{60}$$

Or,

$$B = -\left[\left(\frac{2L_{m1} V_O I_O (V_{IN} + V_{REFL} - V_{Q1,ON})^2}{\eta (V_{REFL})^2 (V_{IN} - V_{Q1,ON})^2}\right) + 2\pi\sqrt{L_{m1} C_{S1}}\right] \tag{61}$$

Where the maximum BCM operating frequency (f_{max}) occurs at maximum input voltage ($V_{IN,max}$) and minimum output load ($I_{O,min}$) or output power ($P_{O,min}$). Likewise, the minimum BCM operating frequency (f_{min}) occurs at minimum input voltage ($V_{IN,min}$) and maximum output load ($I_{O,max}$) or output power ($P_{O,max}$).

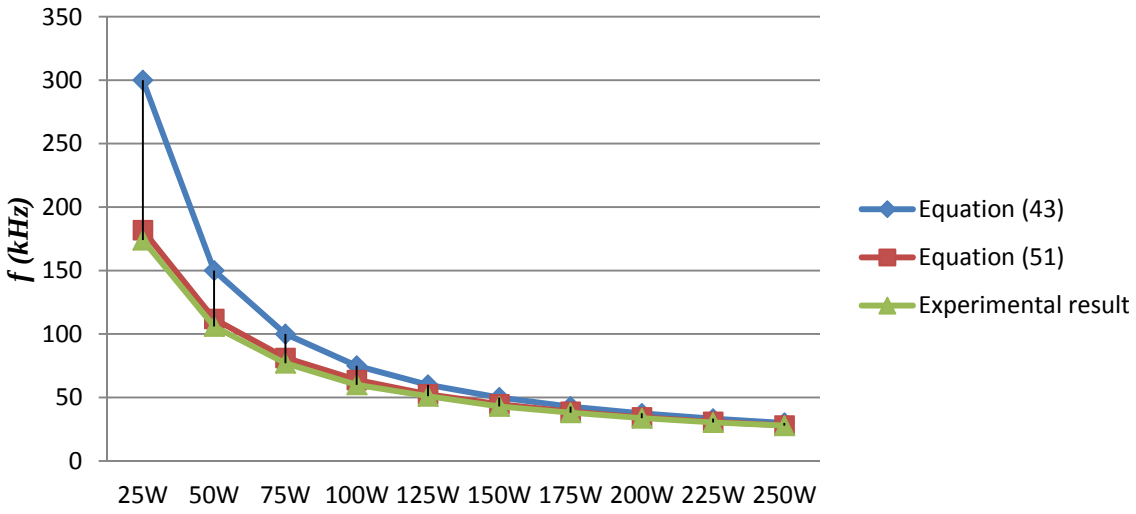


Figure 2.9: BCM flyback operating frequency versus input power (P_{IN}). The blue line illustrates the frequency variations while ignoring C_{S1}. The burgunday line shows the frequency while taking C_{S1} into account. The green line illustrates the experimental results, which agrees with the results provided by (51).

2-4 Design Considerations of the Proposed Circuit

The primary inductance of the master transformer T_1 (L_{m1}) and the primary inductance of the slave transformer (L_{m2}) are to be designed equal. However, since it is not possible to guarantee that exact equality is achieved in production, due to tolerances, L_{m2} needs to be designed at the minimum end of the tolerance of L_{m1}. This would guarantee that the slave flyback does not operate in the continuous conduction mode. Hence,

$$L_{m2,\max} \le L_{m1,\min} \tag{62}$$

Similarly, referring to *Fig. 2.2*, despite the advantage of having C_{Ramp1} and C_{Ramp2} be charged from the same voltage source through R_2 and R_3 respectively, and despite that V_{Ramp1} and V_{Ramp2} are both compared to the same reference voltage (V_{ref}), the tolerances of such components need to be considered. Hence, in order to ensure that both the master and the

slave flybacks do operate at BCM, a viable approach is to design for trimming R_3 during manufacturing, which would offset the said tolerances.

On the other hand, based on *Fig. 2.2*, in order to insure that both the master and slave flybacks do share the load equally, when phase shading is not implemented, the master flyback's duty cycle (δ_1) needs to be designed for a maximum value of 50%. Hence, based on equation (7), V_{REFL} needs to be designed accordingly. However, if desired, greater than 50% duty cycle could be realized with a minor modification to the scheme. This could be achieved by making the slave flyback ramp reset circuit (V_{Reset2}) be independent of the master flyback drive winding while maintaining that the start of the ON time of Q_2 occur at the end of Q_1's ON time.

More design consideration strategies related to the novel simplified low cost analog implementation of a master/slave methodology are included in the following chapter.

2-5 Conclusion

In this chapter, a novel low cost simplified analog interleaving implementation technique for PV micro-inverters and for converters suitable for wide range applications has been detailed. The scheme is based on a master/slave methodology resulting into an efficient soft-switched interleaved variable frequency flybacks operating at BCM. The illustrated control method is suitable for real-world applications while it is simpler and lower cost than what has been previously proposed.

The scheme does not require an auxiliary startup supply. In addition to featuring reduced drive circuit losses, the scheme allows for the use of lower voltage rating switching

devices, which will be further discussed in a later chapter. Configuration, operation principle, design equations and considerations were detailed in this chapter.

Chapter 3: Design Model for the Novel Low Cost PV Converter Based on Analog Interleaving Method

3-1 Overview

In this chapter, a design model for the novel low cost PV converter, operating in the boundary conduction mode, discussed in chapter 2 is undertaken. Parameters required for optimizing the component selections as well as the variable frequency BCM flyback transformer design are the outcome of the said model, which are further discussed in chapter 4. The method illustrated by the model also includes necessary design considerations that enables the use of lower voltage rating MOSFET employed as the switching device.

On the other hand, numerous publications discuss the topic of optimizing the flyback transformer design. Reference [20] addresses the case of flyback transformer wound with litz wire with the aim of improving the design of the winding in order to reduce the transformer losses, introducing a new optimization method that leads to optimizing the strand size and number of litz wire while considering cost and losses. Furthermore, [20] indicates that its proposed method is valid with two or three dimensional fields and different non-sinusoidal currents in each winding. Moreover, reference [20] claims that the method was tested and validated in a flyback converter, where lower losses were resulted.

Reference [21] proposes a low profile design of distributed transformers for grid-tied PV inverters, presenting an analytical loss model aiming to optimize the value of the magnetizing inductance and achieving 96% efficiency in its experimental results. The distributed transformers include a current sense windings applied in a dual flyback converter,

allowing a boundary conduction mode (BCM) and discontinuous conduction mode (DCM) operation.

Reference [22] presents an optimization of the winding strategy of the transformer in a flyback converter to include design rules in order to minimize the leakage inductance and AC resistance, presenting several winding interleaving techniques. Furthermore, in order to reduce the AC resistance of the windings, [22] recommends placing the winding conductors as far as possible from the core and the air gap. On the other hand, [23] discusses the transformer design considerations for non-continuous mode boost and flyback converters and proposes 8 optimization steps for the transformer.

While in some areas of the transformer design, the referenced publications do present useful means and practices, a more comprehensive method is needed in the design of low cost and high performance variable frequency BCM flybacks. A design model is discussed in this chapter that covers all necessary elements required for proper BCM flyback transformer and other components' design. The model leads to optimization, which is further discussed in chapter 4.

3-2 Variable Frequency BCM Flyback Design Model Digest

There is a lack of an available comprehensive design friendly model suitable for optimizing the design of a variable frequency flyback operating in the boundary conduction mode (BCM). *Fig. 3.1* offers a proposed design model diagram that implements the derived equations explored in chapter 2 and in this chapter. The model is comprised of 12 sequential steps, simply requiring information such as the specified input voltage and power. Key

design variables that are required for the converter's (or inverter) component selections are featured as the output of the said model.

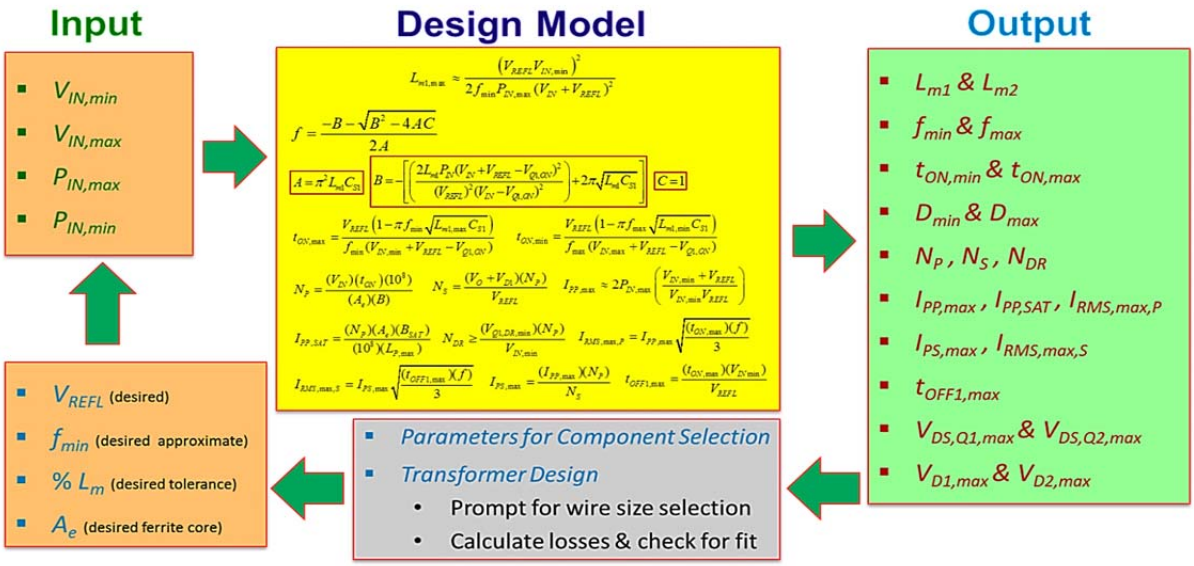


Figure 3.1: Proposed variable frequency BCM flyback design model diagram.

3-2-1 BCM Flyback Design Model Procedure – Component Selections' Guide

In this section the design model procedure for the BCM flyback converter is comprehensively presented. The process involves 12 steps that are detailed below:

Step 1

Select the desired minimum operating frequency (f_{min}) of the BCM flyback. As discussed in section 2-3-5, where f_{min} occurs at the minimum input voltage ($V_{IN,min}$) and maximum input power ($P_{IN,max}$).

Step 2

Select the secondary reflected voltage to the primary (V_{REFL}); keeping in mind that in addition to the voltage spike caused by the uncoupled energy, the voltage seen at the drain of

the MOSFET used as the primary switching device is the sum of V_{IN} and V_{REFL}. Therefore, the lower V_{REFL} is, the lower the required voltage rating of the switching device is. On the other hand, based on equation (53), the lower V_{REFL} is, the higher the primary peak current is. Hence, V_{REFL} needs to be optimized based on the application, which will be further discussed in chapter 4.

Step 3

Use equation (42) to calculate the maximum primary inductance ($L_{m1,max}$). Where, V_{IN} is at $V_{IN,min}$ and P_{IN} is at $P_{IN,max}$. Hence,

$$L_{m1,\max} \approx \frac{\left(V_{REFL} V_{IN,\min}\right)^2}{2 f_{\min} P_{IN,\max} (V_{IN} + V_{REFL})^2} \tag{63}$$

Typically, 15% to 20% is the tolerance of the inductance that is realistically held during manufacturing. Such tolerance is due to variations in the ferrite characteristics from one batch to another, not having the exact air gap thickness, and variations of the primary and secondary windings' positioning in the transformer bobbin. Therefore, if the specified tolerance is set at 15%, the nominal primary inductance value needs to be quantified such that:

$$L_{m1} = \frac{L_{m1,\max}}{1.15} \pm 15\% \tag{64}$$

Furthermore,

$$L_{m1} \geq L_{m2} \tag{65}$$

It is worth noting that it is reasonable to assume that the ferrite core sets for the master and slave flybacks' are from the same batch, hence variations in the ferrite material characteristics for the master and slave transformers are minimal, if any. Furthermore, the number of turns and the winding structure design need to be identically specified.

Step 4

From the value of V_{REFL} selected in Step 2, L_{m1} found in Step 3, and from equation (51), rewritten below, calculate the minimum (f_{min}) and maximum (f_{max}) operating frequencies, keeping in mind that f_{min} occurs at $L_{m1,max}$, $V_{IN,min}$ and $P_{IN,max}$ while f_{max} occurs at $L_{m1,min}$, $V_{IN,max}$ and $P_{IN,min}$.

$$f = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \tag{66}$$

Where;

$$A = \pi^2 L_{m1} C_{S1} \tag{67}$$

$$B = -\left[\left(\frac{2L_{m1}P_{IN}(V_{IN} + V_{REFL} - V_{Q1,ON})^2}{(V_{REFL})^2 (V_{IN} - V_{Q1,ON})^2}\right) + 2\pi\sqrt{L_{m1}C_{S1}}\right] \tag{68}$$

$$C = 1 \tag{69}$$

In most applications, $V_{Q1,ON}$ could be ignored since it is typically much less than V_{IN}.

Step 5

From equation (37), calculate the ON-time (t_{ON}) of the primary switching MOSFET device (Q_1). The maximum ON-time ($t_{ON,max}$) occurs at f_{max} while the minimum ON-time ($t_{ON,min}$) occurs at f_{min}.

Hence,

$$t_{ON,\max} = \frac{V_{REFL}\left(1 - \pi f_{\min}\sqrt{L_{m1,\max}C_{S1}}\right)}{f_{\min}(V_{IN,\min} + V_{REFL} - V_{Q1,ON})} \tag{70}$$

And,

$$t_{ON,\min} = \frac{V_{REFL}\left(1 - \pi f_{\max}\sqrt{L_{m1,\min}C_{S1}}\right)}{f_{\max}(V_{IN,\max} + V_{REFL} - V_{Q1,ON})} \tag{71}$$

Again, in most applications, $V_{QI,ON}$ could be ignored since it is typically much less than V_{IN}. On the other hand, $t_{ON.min}$ found in equation (71) is not required for the transformer design. However, $t_{ON.min}$ should be compatible with the minimum ON-time that the control and turn OFF circuits can respond to.

Step 6

Calculate the minimum required primary turns (N_P), using:

$$N_P = \frac{(V_{IN})(t_{ON})(10^8)}{(A_e)(B)} \tag{72}$$

Where, A_e is the effective core cross sectional area in cm^2 and B is the flux density in *Gauss*. Furthermore, N_P needs to be calculated at $t_{ON,max}$, which occurs at f_{min} and $V_{IN,min}$.

Step 7

Calculate the primary saturation current ($I_{PP,SAT}$), using:

$$I_{PP,SAT} = \frac{(N_P)(A_e)(B_{SAT})}{(10^8)(L_{P,\max})} \tag{73}$$

Where, B_{SAT} is the saturation flux density in *Gauss*, as specified by the ferrite core material manufacturer. Finding $I_{PP,SAT}$ is crucial in the design process. The control circuit needs to be designed where the maximum ON time, for both the master and slave flybacks, needs to be limited such that $I_{PP} < I_{PP,SAT}$. Limiting the peak primary current to less than $I_{PP,SAT}$ would prevent saturation of the transformer. Furthermore, Q_1 and Q_2 current ratings need to be higher than that of the maximum I_{PP} that could potentially be seen by either of the devices.

Step 8

From equation (53), calculate the maximum peak primary current ($I_{PP,max}$), which occurs at $V_{IN,min}$ and $P_{IN,max}$.

$$I_{PP,\max} \approx 2P_{IN,\max}\left(\frac{V_{IN,\min}+V_{REFL}}{V_{IN,\min}V_{REFL}}\right) \tag{74}$$

Step 9

Calculate the secondary number of turns (N_S), using:

$$N_S = \frac{(V_O + V_{D1})(N_P)}{V_{REFL}} \tag{75}$$

Where V_O is the output voltage, V_{D1} is voltage drop during t_{OFF1} of the diode employed to rectify V_O, and V_{REFL} is the reflected voltage found in Step 2.

Step 10

Find the drive winding number of turns (N_{DR}), using:

$$N_{DR} \geq \frac{(V_{Q1,DR,\min})(N_P)}{V_{IN,\min}} \tag{76}$$

Where V_O is the output voltage, $V_{Q1,DR,min}$ is the minimum gate voltage required to insure that Q_1 is properly driven into saturation. Furthermore, Since the said drive winding is not only supplying the gate drive voltage for Q_1, as shown in *Fig. 2.2,* but is also providing the gate drive voltage for Q_2 during the OFF-time of Q_1, where its voltage is proportional to the output voltage times the turns ratio:

$$N_{DR} \geq \frac{(V_{Q2,DR,\min})(N_S)}{(V_O + V_{D1})} \tag{77}$$

Since it is desirable to have $V_{Q1,DR,min}$ to be equal to $V_{Q2,DR,min}$, the right hand term of equations (76) and (77) needs to be equal. For this to occur, V_{REFL} needs to be set to be equal to $V_{IN,min}$. In applications where V_{IN} varies significantly, it is preferable to add a drive winding to transformer T_2 in order to supply the turn ON drive for Q_2, while maintaining the turn ON synchronization through the drive winding of T_1. However, in solar applications, the variation of the input voltage is not substantial.

Step 11

Find the transformer windings' RMS currents, using:

$$I_{RMS,\max,P} = I_{PP,\max}\sqrt{\frac{(t_{ON,\max})(f)}{3}} \tag{78}$$

Where $I_{RMS,max,P}$ is the RMS current of the primary winding.

$$I_{RMS,\max,S} = I_{PS,\max}\sqrt{\frac{(t_{OFF1,\max})(f)}{3}} \tag{79}$$

And $I_{RMS,max,S}$ is the RMS current of the secondary winding. Furthermore, the peak secondary current ($I_{PS,max}$) is found such that,

$$I_{PS,\max} = \frac{(I_{PP,\max})(N_P)}{N_S} \tag{80}$$

Moreover, $t_{OFF1,max}$ is found as follows:

$$t_{OFF1,\max} = \frac{(t_{ON,\max})(V_{IN\min})}{V_{REFL}} \tag{81}$$

Step 12

Based on the RMS current in each of the windings, find the required wire sizes using a litz wire table. From the above steps, all needed parameters to optimize the component selections and transformer design will be produced by the model. Design iterations would need to be performed by adjusting the desired V_{REFL}, f_{min}, and A_e parameters until satisfactory results are reached. Such results include the proper component selections that are compatible with the model outcome.

3-3 Variable Frequency BCM Transformer Design

This section proposes a detailed design method, to include calculations and optimizations of the flyback transformer losses. The technique is intended to enhance the said

transformer design in terms of leakage inductance, capacitance among windings, and related design considerations that enable the use of lower voltage rating MOSFET employed as the switching device, which is further discussed in chapter 4. The method includes a step by step design process that leads to optimizing the master and slave transformers of the interleaved flyback DC/DC converter operating in BCM, resulting in the selection of the smallest but application suitable transformer core size, while achieving high efficiency and improved performance.

3-3-1 Undesired Transformer Performance Design Summary

High frequency transformer design is a crucial step in power electronics. Inadequate design could lead to adding unwanted losses and voltage spikes. Below is a summary list of some of the known undesired transformer performance:

1) Poor coupling among the windings. This leads to the increase of the leakage inductance, which would result into uncoupled energy transfer that could result in losses. Furthermore, poor coupling do also results in higher voltage spikes seen by the switching devices. If not corrected by adding related circuits, higher voltage rated switching devices would be required as a result.
2) Ferrite material is used in today's high switching transformers. Such material has losses dependent on the selected type, the operating frequency, and the flux density magnitude swing (B_{swing}) used in the application. Not paying special attention to B_{swing} will result into additional losses. Furthermore, if B_{swing} exceeds the maximum flux density (B_{max}) specified for the ferrite material used, saturating the said transformer is resulted, which could lead to damaging its associated switching device(s).

3) Ordinary solid copper magnet wire is not suitable for high frequency switching transformer windings, due to the skin effect phenomena, which causes losses. Therefore, not using appropriately selected Litz wire will add to the list of avoidable losses. Furthermore, preventable losses are added if the winding wire is not properly sized to carry the applied RMS current.

3-3-2 BCM Flyback Transformer Ferrite Material Selection

In order to reduce the transformer losses, the selected ferrite material needs to be suitable and optimized based on the minimum and maximum operating frequencies, as calculated from Step 4 of the above section. As an example, searching through the EPCOS online catalog [25], as presented in *Fig. 3.2*, it is suggested that for power transformers operating below 100 kHz, the N27, N41, and N51 material would be suitable. The use of each type is based on the application, where the N27 material is most useful for low cost and high power, the N41 is most suitable as a current transformer, and the N51 offers minimum loss at 40°C temperature.

The EPCOS catalog suggests, as also presented in *Fig. 3.2*, that for operations higher than 100 kHz but less than 500 kHz, the following suitable material: N87 as a standard; N88 offering minimum loss at 140°C temperature; N95 and N96 presenting flat temperature behavior; N97 offering lower losses; and PC47 presenting the lowest losses of the series. Furthermore, the said online catalog presents the N49 material for applications higher than 500 kHz.

Therefore, it is critical that the selected ferrite material be optimized to reduce the core losses based on the minimum and maximum operating frequencies of the converter or

inverter. While the referenced catalog categorizes its ferrite material based on frequency ranges, pinpointing the optimum material for the application remains the work of the designer. For example, while the catalog suggests that the N87, N88, N95, N96, N97, and PC47 would be suitable for applications operating anywhere from 100 to 500 kHz, some of the said material are more suitable than others at specific operating points.

From *Fig. 3.2*, the core loss in the N96 material at 2000 mT, 50 kHz, and 25°C is approximately150 kW/m^3. The same material core loss at 2000 mT and 25°C is slightly over 300 kW/m^3 and 1000 kW/m^3 at 100 and 200 kHz respectively. On the other hand, the N97 and PC47 materials are shown to have core losses of approximately 250 and 300 kW/m^3 respectively at 2000 mT, 50 kHz, and 25°C. The N97 and PC47 have similar core loss of approximately 600 kW/m^3 at 100 kHz, 2000 mT, and 25°C, while it is approximately 1700 kW/m^3 at 200 kHz, 2000 mT, and 25°C.

At higher temperatures, the N97 and PC47 material becomes more efficient than the N96. From *Fig.3.2*, at 100°C, 2000 mT, and 50 kHz, the core losses are approximately 160 kW/m^3 for N96 while it is 100 kW/m^3 for N97 and for PC47. At 100°C, 2000 mT, and 100 kHz, the core losses are approximately 350 kW/m^3 for N96, 300 kW/m^3 for N97, and 280 kW/m^3 PC47. Furthermore, At 100°C, 2000 mT, and 200 kHz, the core losses are approximately 1200 kW/m^3 for N96, 1000 kW/m^3 for N97and for PC47.

Hence, based on the curves presented in *Fig. 3.2*, as an example, if the volume of the core used is 14000 mm^3, as is the case for the EPCOS RM14 core set [26], the corresponding core loss calculation is shown in *Table 3.1.* From the said table, it is apparent that while some materials are more efficient than others at higher temperatures and frequencies, it is also obvious that core losses do increase significantly at higher frequencies if the operating flux

density (B) remains the same. On the other hand, from (70) and (72), lower flux density swing is achieved, resulting into lower core losses, if the primary number of turns (N_P) is kept constant while increasing the operating frequency (f).

Therefore, using the same RM14 core set example given in *Table 1*, and maintaining the same number of turns while doubling the operating frequency, which would result into lowering the flux density swing in half (to 1000 mT), will lead to the results shown in *Table 3.2*. Hence, from the transformer design standpoint, the core loss is minimized as follows:

1) Select the core size and material, such as:
    a. To have the maximum effective cross sectional area for the application. This is necessary to minimize the primary number of turns while minimizing the core flux density (B) swing.
    b. To have the minimum possible effective volume (V_e). This is due to the fact that the core losses are directly proportional to *Ve*.
    c. The selected core set is offered in low loss ferrite material based on the desired operating frequency (not all core shapes, and sizes are offered in all ferrite material types by the manufacturers).
2) From *Table 3.2*, the core losses are reduced by lowering B. Increasing the operating frequency in order to lower B present core loss advantages. However, since increasing the operating frequency could result in additional losses in other areas of the converter or inverter, such as the main switching MOSFET Gate drive, turn ON and turn OFF switching losses, etc., optimization of the said operating frequency need to be considered and implemented in order to minimize the overall losses. Such topic is further discussed in chapter 4.

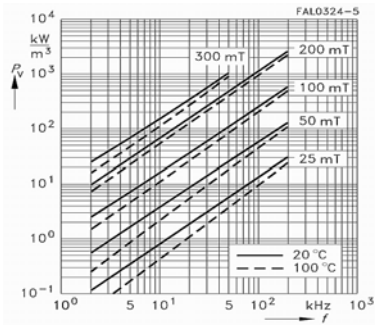
Based on [25], the purpose for the graphs shown in *Fig. 3.2* is to "provide the user with improved means for comparing different materials." Furthermore, the data is based on sinusoidal waveforms, which are not accurately applicable to most switch mode power supplies, including the BCM flyback. Moreover, the data shown in *Table 3.1* and *Table 3.2* that is based on the curves provided in *Fig. 3.2*, do not exactly match the ones for RM14 provided by the EPCOS catalog. A more accurate core loss analysis is offered in chapter 4.

Table 3.1: Ferrite material approximate core losses using the RM14 core set operating at B = 2000 mT and loss curves as provided by EPCOS [25-26].

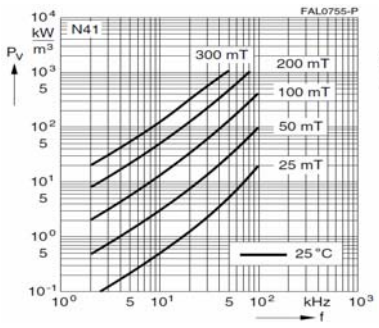
RM14; Effective Core Volume per set (Ve) = 14000 mm3; Operation Example: B = 2000 mT	**Operating Frequency & Temperature**					
	50 kHz		100 kHz		200 kHz	
Ferrite Material	25°C	100°C	25°C	100°C	25°C	100°C
	Core Power Dissipation (W)					
N96	2.10	2.24	4.20	4.90	14.00	16.80
N97	3.50	1.40	8.40	4.20	23.80	14.00
PC47	4.20	1.40	8.40	3.92	23.80	14.00

Table 3.2: Ferrite material approximate core losses using the RM14 core set operating at B = 1000 mT while doubling the frequencies shown in Table 3.1, and loss curves as provided by EPCOS [25-26].

RM14; Effective Core Volume per set (Ve) = 14000 mm3; Operation Example: B = 1000 mT	**Operating Frequency & Temperature**					
	100 kHz		200 kHz		400 kHz	
Ferrite Material	25°C	100°C	25°C	100°C	25°C	100°C
	Core Power Dissipation (W)					
N96	0.77	0.77	2.38	2.66	8.82	14.00
N97	1.82	0.63	4.34	2.10	14.00	9.10
PC47	2.10	0.52	4.90	2.10	14.00	9.10



SIFERRIT material N27



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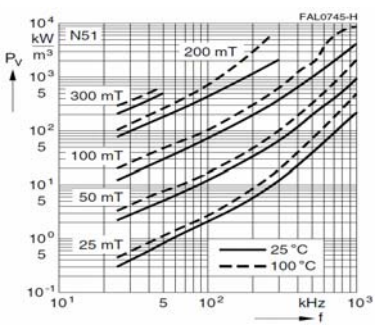

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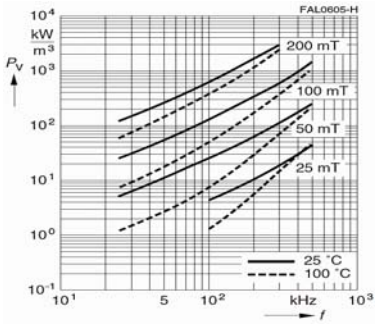

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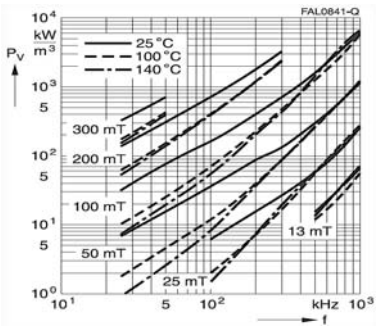

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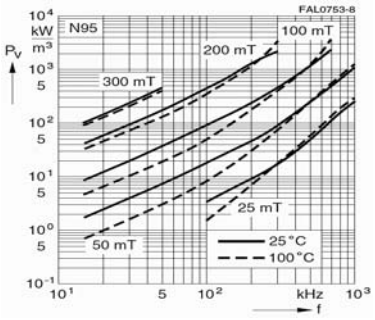
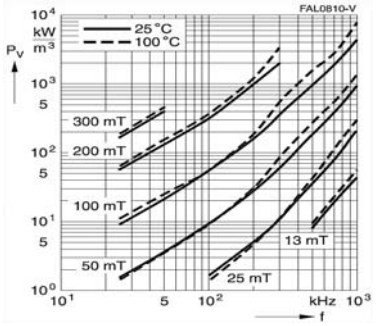


SIFERRIT material N95



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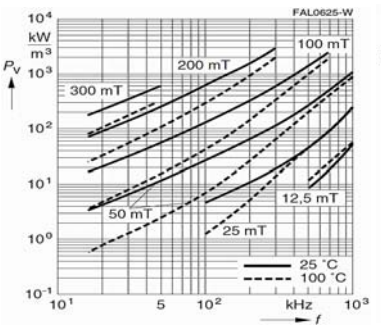

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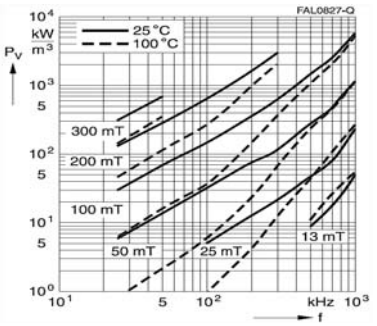
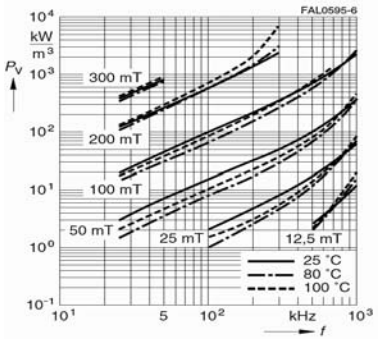


SIFERRIT material PC47



SIFERRIT material N49

Figure 3.2: Ferrite material loss curves as provided by EPCOS [25].

3-3-3 Winding Transformers for Minimum Leakage Inductance

In addition to applying the transformer design procedure detailed in section 3-2-2, winding the transformer for minimum leakage inductance and coupling capacitances among windings is a critical step in a transformer design. While copper foil is sometimes used in high current carrying windings with low number of turns, which minimizes the leakage inductance to adjacent windings, it also increases the capacitances among the said windings. Such capacitances are as undesirable as the leakage inductances and also need to be minimized. In this section, an optimization step is presented in addition to the commonly used and well known low leakage winding methods, while winding with properly sized litz wires is assumed.

1. Perform the steps in section 3-2-1 and select the core and bobbin.
2. Select the wire sizes, according to the applied RMS current. Furthermore, increase the said wire sizes such that each significant (power carrying) winding fills the full bobbin width in the layers it occupies.
3. Interleave the windings as needed in order to minimize the leakage inductances

3-5 Design for 250W PV Panel

While the Novel Low Cost PV Converter Based on Analog Interleaving Method topology is suitable for 300W PV panels, in this section, a detailed design procedure of a BCM flyback transformer suitable for a 250W solar panel (ISOFOTON ISF-250) is presented [29]. The design will be based on a set of specifications that are illustrated in *Table 3.3*. The specified 250V output voltage is based on the assumption that the second stage DC/AC inverter is tied to 120VAC, which is one of the grid phases connected to a residential dwelling.

3-5-1 DC-DC Converter Electrical Specifications

Table 3.3: Electrical specifications for the DC/DC converter in a DC parallel approach

DC-DC Converter Electrical Specifications					
Parameters	**Condition & Description**	**Min**	**Nom**	**Max**	**Unit**
Input Voltage Range	Output Current (min to max)	22.00	30.60	31.00	VDC
Max input Power	at Input Voltage = 30.6V			250.00	W
	at Input Voltage = 27.5V			181.00	W
Under-voltage Lockout (UVLO)	ON for Input Voltage less than 22V				VDC
	OFF for Input Voltage equal or greater than 22V				VDC
Input Over-Voltage Protection	Inverter must shutdown and restart once the input OV condition is removed	45.00			VDC
Output Voltage	Determined by the central inverter. The DC-DC converter should not start if the output voltage is not present.	237.50	250.00	262.50	VDC
Output Current		0.10	1.00	1.05	A
Output Over-Voltage Protection	Converter to shut down and restart once the OV condition is removed	287.50		300.00	VDC
No Load Protection (Grid not present)	Converter to shut down and should restart once the grid is reinstated	0.00		0.25	A
Output Short Circuit Protection	No damage shall occur to the converter in the case of a short circuit on its output. The converter must restart once the short circuit condition is removed.				
Operating Temperature Range		-25.00		60.00	°C
Primary to Secondary isolation is required. PCB and transformer's Primary to Secondary min. spacing's are to meet appropriate UL requirements. All primary to secondary components must be UL approved.					
DC-DC converter to operate only when the grid voltage is present. On startup, the converter must check for the presence of the 250VDC (nominal) output first. Furthermore, after normal operating conditions are established, the DC-DC converter must shutdown once the grid is no longer available. In the case where the solar voltage is within range, the converter must restart once the grid voltage returns. No communication wire between the converter and the central inverter is permitted.					

3-5-2 Design Implementation

Following the steps provided in section 3-2-1 and using the specification requirements provided in *Table 3.3* would lead to a straightforward design for the master (T_1) and slave (T_2) transformers, keeping in mind that T_1 and T_2 will equally share the load at the maximum input power (P_{IN}) of 250W. Therefore, the maximum power under normal operation that T_1 and T_2 would see is 125W each. Furthermore, for this design iteration, let the core set selected be the EPCOS RM 14, where the core specifications are shown in *Fig. 3.3* [26] and its associated bobbin dimensions is shown in *Fig. 3.4* [26], as copied from the EPCOS catalog. It is worth noting that the RM 14 is offered in the N97 but not the N95 material.

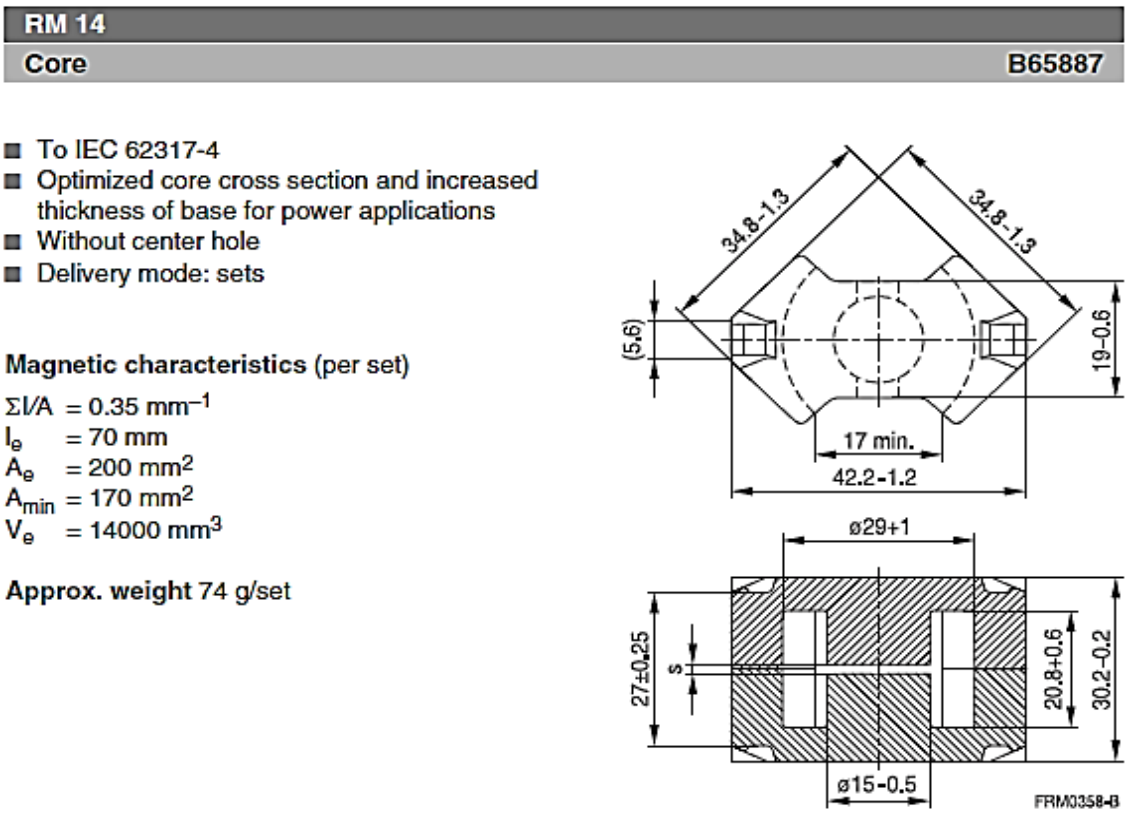


Figure 3.3: RM 14 core set specifications as provided by the EPCOS catalog [26].

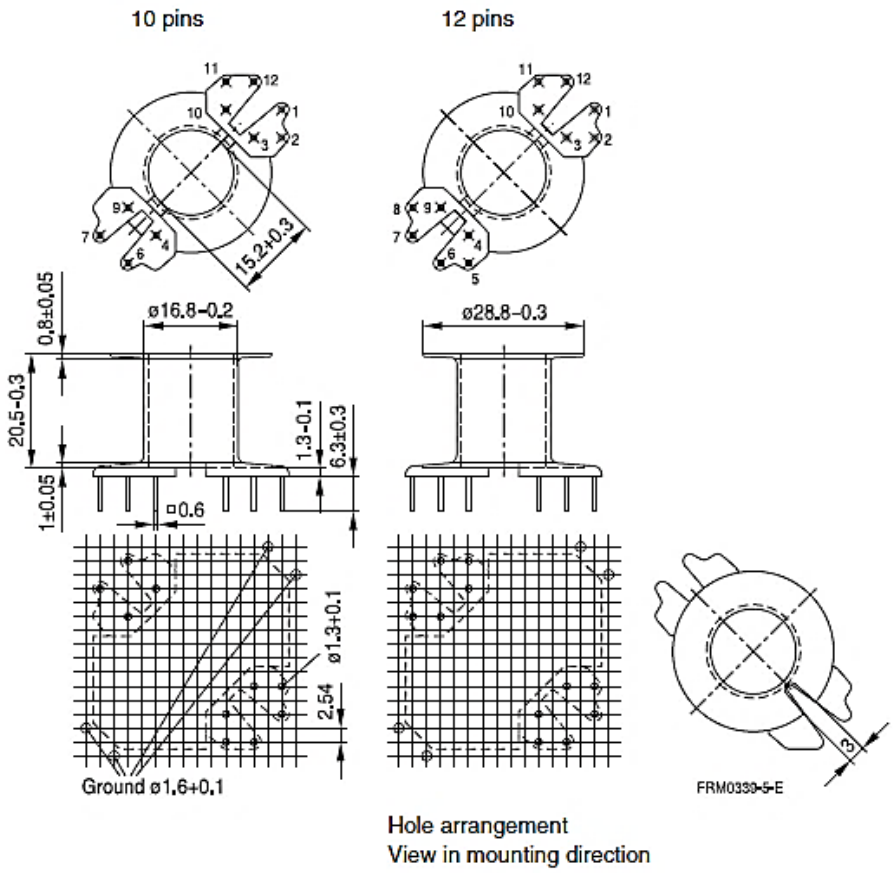


Figure 3.4: One of the suitable bobbin specifications for the RM 14 core set, as provided by the EPCOS catalog [26].

Step 1

Let f_{min} be 50 kHz.

Step 2

Based on the specifications provided in *Table 3.3*, the maximum input power at 30.6V is 250W and at 27.5V is given as 181W. Hence in order to reach or be near the desired zero-voltage-switching (ZVS) at the start of the ON-time, let:

$$V_{REFL} = 26.5V \tag{82}$$

Step 3

$$L_{m1,\max} \approx 16.134\mu H \tag{83}$$

In order to maximize the yield, assume 15% is the desired manufacturing inductance tolerance. Hence let:

$$L_{m1} = 14\mu H \pm 15\% \tag{84}$$

Therefore, for the master transformer (T_1), the primary inductance (L_{m1}) is given in equation (84). Furthermore, for the slave transformer (T_2), the maximum value of the primary inductance (L_{m2}) needs to be set where its maximum value need to be less than or equal to the minimum value of L_{m1}.

Step 4

To find the minimum (f_{min}) and maximum (f_{max}) operating frequencies, keeping in mind that f_{min} occurs at $L_{m1,max}$, $V_{IN,min}$ and $P_{IN,max}$ while f_{max} occurs at $L_{m1,min}$, $V_{IN,max}$ and $P_{IN,min}$.

$$f_{\min} = 43.59kHz \tag{85}$$

And,

$$f_{\max} = 191.1kHz \tag{86}$$

Hence, while the maximum to minimum power ratio is 10, the corresponding frequency ratio is only 4.38 due to the influence of C_{S1} (where C_{S1} = 15 nF).

Step 5

$$t_{ON,\max} = 9.93\mu S \tag{87}$$

And,

$$t_{ON,\min} = 1.8\mu S \tag{88}$$

Step 6

Calculate the minimum required primary turns (N_P), setting $B = 2000\ Gauss$, which would result in core losses of approximately 1% (1.25W at 43.59 kHz). While such core

losses may be on the high side in solar applications, they are acceptable in most other applications.

$$N_P = \frac{(30.6)\left(9.3\times10^{-6}\right)(10^8)}{(200\times10^{-2})(2000)} = 7.11 turns \tag{89}$$

Rounding up,

$$N_P = 8 turns \tag{90}$$

At $N_P = 8$ *turns*, the flux density is reduced to 1777.5 *Gauss* (177.75 *mT*), which would reduce the above calculated core losses.

Step 7

$$I_{PP,SAT} = 29.81A \tag{91}$$

Step 8

$$I_{PP,\max} = 17.6A \tag{92}$$

Step 9

$$N_S = 76 turns \tag{93}$$

Step 10

$$N_{DR} = 4 turns \tag{94}$$

Step 11

$$I_{RMS,\max,P} = 6.687A \tag{95}$$

$$I_{RMS,\max,S} = 0.756A \tag{96}$$

Where,

$$I_{PS,\max} = 1.853A \tag{97}$$

And,

$$t_{OFF1,\max} = 11.467\mu S \tag{98}$$

Step 12

Based on the RMS current in each of the winding, *Table 3.4* illustrates the selected wire sizes along with the calculated winding, core, and total transformer losses.

Table 3.4: Transformer losses breakdown.

Winding	Number of Turns	Wire Size	Wire Diameter (in)	Wire Ohm/1000 ft	Wire Length per Turn (ft)	Total Wire Length (ft)	Ohm per Winding	RMS Current per Winding (A)	Losses per Winding (W)
Primary	8	200 # 38	0.088	3.588	0.199	1.594	0.0057	6.687	0.256
Secondary	76	175 # 46	0.030	27.600	0.186	14.109	0.3894	0.756	0.223
								Total Winding Losses:	0.479

Core Volume (cm3)	Core Dissipation per mW/cm3	Total Core Dissipation (W)	Total Transformer Losses (W)	Losses %
14.00	60.00	0.840	1.319	1.05%

Furthermore, the bobbin buildup for the master transformer is shown in *Table 3.5* below. The bobbin buildup for the slave transformer is the same without the drive winding.

Table 3.5: Transformer bobbin buildup.

Bobbin Min. Dept (mm)	Buildup (mm)				Balance (mm)
	Primary	Secondary	Drive	Total	
6.000	2.235	0.762	0.762	4.521	1.479
Layers	1	2	1		

3-6 Conclusion

In this chapter, a design model for the novel low cost PV interleaved flyback converter, operating in the boundary conduction mode (BCM) was detailed. The model is based on a step by step approach, producing all necessary design parameters for the topologies' component selection and for the transformer design, which serves in optimization. The chapter also included details related to the ferrite material selection,

undesired transformer performance summary, and steps for winding the flyback transformer for minimum leakage inductance.

The DC-DC converter electrical specification was offered in section 3-5-1, while a design implementation example was discussed in section 3-5-2. A detailed transformer losses breakdown was presented and methods to design for the selection of lower voltage ratings of the main switching devices were discoursed. More details related to the optimization of key components are discussed in chapter 4.

Chapter 4: Design Optimization for the Novel Low Cost PV Converter Based on Analog Interleaving Method

4-1 Overview

In this chapter, the design optimization for the Novel Low Cost PV Converter Based on Analog Interleaving Method is discussed. The said optimization is based on prioritizing component cost and efficiency performance for key components, such as the power switching devices (MOSFETs) and the high frequency transformers used. Several commercially available MOSFET devices will be compared, illustrating the advantages of using lower voltage rating devices. Furthermore, this chapter also includes optimization of the duty cycle and the operating frequency of the BCM flyback in an effort to reduce the transformer core and switching losses. This chapter will also discuss optimization of the implementation of phase shading at light load.

4-2 Design Optimization for the BCM Flyback Power MOSFETs

Efficiency and cost are key elements to be considered while optimizing the selection of power MOSFETs suitable for use in the Novel Low Cost PV Converter Based on Analog Interleaving Method as well as any efficiency driven low cost power electronic converters or inverters. For a given power conversion level, such as for a 250W PV panel output, each one of the interleaved flybacks handles approximately half of such power (125W) and operates at the conditions shown in *Table 3.3*.

4-2-1 MOSFET Voltage Ratings' Selection

In order to reach the desired optimization, the devices' voltage and current ratings are essential. While some of the industries do use 200V voltage MOSFETs in their 250W PV inverter applications, most others do incorporate the 150V voltage rating ones in their products. *Table 4.1* exemplifies the unit cost and device parameters of few selected 200V voltage rating metal oxide N-channel MOSFETs. *Table 4.2* illustrates the unit cost and device parameters' comparison among various 80V, 100V, and 150V voltage rating metal oxide N-channel MOSFETs that are suitable for the application.

Based on *Table 4.2*, for a comparable drain to source ON resistance ($r_{DS,ON}$), the device's unit cost becomes higher once the voltage rating increases. While an 80V voltage rated MOSFET that has an $r_{DS,ON}$ equal to 4.3 mΩ costs slightly less than a 100V voltage rated MOSFET, which has an $r_{DS,ON}$ equal to 4.8 mΩ ($2.22 compared to $2.66), the 150V rated MOSFET with the closest $r_{DS,ON}$ (7.5 mΩ) has a unit cost of $6.05. From *Table 4.1*, the unit cost for a 200V voltage rated device that has an $r_{DS,ON}$ of 9.7 mΩ is $8.07. Hence, the ability to use a lower voltage rated MOSFET in the converter (or inverter) do present cost advantages at a lower drain to source ON resistance.

Table 4.1: Unit cost and device parameters of few selected 200V voltage rating metal oxide N-channel MOSFETs, where the data are extracted from the Digi-Key Electronics' website [30].

Manufacturer	Manufacturer Part Number	Unit Price (USD)	Drain to Source Voltage (Vdss)	Current - Continuous Drain (Id) @ 25°C	Rds On (Max) @ Id, Vgs	Gate Charge (Qg) @ Vgs	Input Capacitance (Ciss) @ Vds	Power - Max
International Rectifier	IRFP4668PBF	$8.07	200V	130A (Tc)	9.7 mΩ @ 81A, 10V	241nC @ 10V	10720pF @ 50V	520W
Infineon Tech.	IPP110N20NA	$7.12	200V	88A (Tc)	10.7 mΩ @ 88A, 10V	87nC @ 10V	7100pF @ 100V	300W
Infineon Tech.	IPP110N20N3 G	$6.64	200V	88A (Tc)	11 mΩ @ 88A, 10V	87nC @ 10V	7100pF @ 100V	300W
Infineon Tech.	IPP120N20NFDAKSA1	$6.34	200V	84A (Tc)	12 mΩ @ 84A, 10V	87nC @ 10V	6650pF @ 100V	300W

Table 4.2: Unit cost and device parameters' comparison among various voltage rating MOSFETs that are suitable for the proposed converter, where the data are extracted from the Digi-Key Electronics' website [30].

Manufacturer	Manufacturer Part Number	Unit Price (USD)	Drain to Source Voltage (Vdss)	Current - Continuous Drain (Id) @ 25°C	Rds On (Max) @ Id, Vgs	Gate Charge (Qg) @ Vgs	Input Capacitance (Ciss) @ Vds	Power - Max
Infineon Tech.	IPB035N08N3 G	$3.08	80V	100A (Tc)	3.5 mOhm @ 100A, 10V	117nC @ 10V	8110pF @ 40V	214W
Toshiba Semi.	TK72E08N1,S1X	$2.22	80V	72A (Ta)	4.3 mOhm @ 36A, 10V	81nC @ 10V	5500pF @ 40V	192W
Infineon Tech.	IPB054N08N3 G	$2.08	80V	80A (Tc)	5.4 mOhm @ 80A, 10V	69nC @ 10V	4750pF @ 40V	150W
Infineon Tech.	IPP057N08N3 G	$2.03	80V	80A (Tc)	5.7 mOhm @ 80A, 10V	69nC @ 10V	4750pF @ 40V	150W
Infineon Tech.	IPB067N08N3 G	$1.91	80V	80A (Tc)	6.7 mOhm @ 73A, 10V	56nC @ 10V	3840pF @ 40V	136W
Toshiba Semi.	TK46E08N1,S1X	$1.41	80V	80A (Tc)	8.4 mOhm @ 23A, 10V	37nC @ 10V	2500pF @ 40V	103W
Toshiba Semi.	TK35E08N1,S1X	$1.06	80V	55A (Tc)	12.2 mOhm @ 17.5A, 10V	25nC @ 10V	1700pF @ 40V	72W
Infineon Tech.	IPB039N10N3 G	$3.40	100V	160A (Tc)	3.9 mOhm @ 100A, 10V	117nC @ 10V	8410pF @ 50V	214W
Toshiba Semi.	TK65E10N1,S1X	$2.66	100V	148A (Ta)	4.8 mOhm @ 32.5A, 10V	81nC @ 10V	5400pF @ 50V	192W
Infineon Tech.	IPP072N10N3 G	$2.04	100V	80A (Tc)	7.2 mOhm @ 80A, 10V	68nC @ 10V	4910pF @ 50V	150W
Toshiba Semi.	TK40E10N1,S1X	$1.81	100V	90A (Tc)	8.2 mOhm @ 20A, 10V	49nC @ 10V	3000pF @ 50V	126W
Infineon Tech.	IPB70N10S3-12	$1.61	100V	70A (Tc)	11.3 mOhm @ 70A, 10V	66nC @ 10V	4355pF @ 25V	125W
Infineon Tech.	IPP70N10S3-12	$1.56	100V	70A (Tc)	11.6 mOhm @ 70A, 10V	66nC @ 10V	4355pF @ 25V	125W
Infineon Tech.	IPD122N10N3 G	$1.54	100V	59A (Tc)	12.2 mOhm @ 46A, 10V	35nC @ 10V	2500pF @ 50V	94W
Toshiba Semi.	TK22E10N1,S1X	$1.37	100V	52A (Tc)	13.8 mOhm @ 11A, 10V	28nC @ 10V	1800pF @ 50V	72W
Infineon Tech.	IPA075N15N3 G	$6.05	150V	43A (Tc)	7.5 mOhm @ 43A, 10V	93nC @ 10V	7280pF @ 75V	39W
Infineon Tech.	IPB108N15N3 G	$3.89	150V	83A (Tc)	10.8 mOhm @ 83A, 10V	55nC @ 10V	3230pF @ 75V	214W
Infineon Tech.	IPP111N15N3 G	$3.78	150V	83A (Tc)	11.1 mOhm @ 83A, 10V	55nC @ 10V	3230pF @ 75V	214W
Infineon Tech.	BSC190N15NS3 G	$2.61	150V	50A (Tc)	19 mOhm @ 50A, 10V	31nC @ 10V	2420pF @ 75V	125W
Infineon Tech.	IPB200N15N3 G	$2.41	150V	50A (Tc)	20 mOhm @ 50A, 10V	31nC @ 10V	1820pF @ 75V	150W

On the other hand, excluding the overshoot voltage, the drain to source voltage (V_{DS}) seen by the power MOSFET in a flyback is given in (15) and is rewritten below:

$$V_{DS} = V_{IN} + \frac{n_1}{n_2}(V_o + V_D) \tag{99}$$

Rewriting (7),

$$V_{REFL} = \frac{n_1}{n_2}(V_O + V_D) \tag{100}$$

Combining (99) with (100) leads to:

$$V_{DS} = V_{IN} + V_{REFL} \tag{101}$$

Let $V_{DS,max}$ be the maximum drain to source voltage seen by the MOSFET in the said application, where the turn OFF voltage switching overshoot (V_{OS}) is considered, as shown in *Fig. 4.1*. Hence,

$$V_{DS,\max} = V_{IN} + V_{REFL} + V_{OS} \tag{102}$$

V_{OS} is a variable that is based on how well the turn OFF switching voltage overshoot is clamped. In the circuit illustrated in *Fig. 2.2*, capacitor C_{S1} serves as the MOSFET's voltage clamp. Since $\frac{dv}{dt}$ is inverse proportional to C_{S1}, V_{OS} decreases as C_{S1} increases. Therefore, assuming that C_{S1} is sized such that V_{OS} is limited to 20% voltage overshoot, with a designed V_{REFL} to be equal to V_{IN}, which is given in *Table 3.3* to be approximately 30V, hence:

$$V_{IN} \approx V_{REFL} = 30V \tag{103}$$

Therefore, V_{OS} becomes 12V and the maximum drain to source voltage seen turns out to be:

$$V_{DS,\max} \approx 72V \tag{104}$$

Hence, with the theoretical $V_{DS,max}$ value of 72V (which is experimentally achieved and demonstrated in Chapter 6), an 80V voltage rated MOSFET is feasible and could be selected for the application. This presents a cost advantage in selecting a commercially available device that has a relatively low drain to source ON resistance ($r_{DS,ON}$). Therefore, the lower V_{REFL} is, the lower the required voltage rating for the switching MOSFET is. However, based on (53), the lower V_{REFL} is, the higher the peak primary current (I_{PP}) is. As discussed in the following section, this would increase the MOSFET's drain to source RMS current, which could increase the device's conduction loss. Hence, V_{REFL} needs to be optimized based on the application.

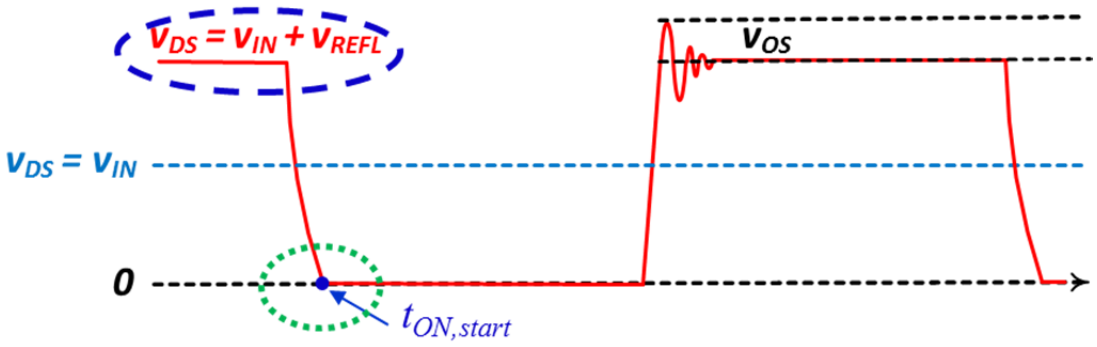


Figure 4.1: BCM flyback main switching MOSFET drain to source voltage (V_{DS}) waveform, where the maximum voltage seen is the sum of the input, reflected, and the overshoot voltages.

4-2-2 Optimization for the MOSFET's Conduction Losses

Conduction losses of the power MOSFET is related to the drain to source ON resistance and the square of the RMS current, as shown below:

$$P_{COND,\max,M} = (r_{DS,ON})(I_{RMS,\max,D}{}^2) \tag{105}$$

Where, $P_{COND,max,M}$ is the MOSFET's maximum conduction loss and $I_{RMS,max,D}$ is the maximum RMS drain to source current, where both occur at the maximum input power. On

the other hand, the MOSFET's drain current is the same as that seen by the switching transformer's primary current ($I_{RMS,max,P}$). Hence, by using the results achieved in (78), $I_{RMS,max,D}$ becomes:

$$I_{RMS,\max,D} = I_{RMS,\max,P} = I_{PP,\max}\sqrt{\frac{(t_{ON,\max})(f)}{3}} \tag{106}$$

However, $I_{PP,max}$ is a function of the maximum input power ($P_{IN,max}$), minimum input voltage ($V_{IN,min}$), and the reflected voltage (V_{REFL}) as given in (74). Therefore, combining (74) and (106) results into a function for the maximum drain current in terms of $P_{IN,max}$, $V_{IN,min}$, V_{REFL}, ON time (t_{ON}), and the operating frequency (f). Furthermore, t_{ON} and f can be found using the equations presented in chapters 2 and 3.

$$I_{RMS,\max,D} \approx 2P_{IN,\max}\left(\frac{V_{IN,\min}+V_{REFL}}{V_{IN,\min}V_{REFL}}\right)\left(\sqrt{\frac{(t_{ON,\max})(f)}{3}}\right) \tag{107}$$

Assuming that a 250W PV panel is used as the input to the converter, where V_{IN} is approximately 30V, each of the interleaved BCM flybacks sees a maximum input power of 125W. *Table 4.3* illustrates the changes that occur to the duty cycle (δ) and to $I_{RMS,max,D}$ when varying V_{REFL} from 10V to 80V while maintaining constant values for $P_{IN,max}$ and $V_{IN,min}$. The drain node capacitance (C_{S1}), described in Chapter 2, was also held constant at 10nF.

Table 4.3: Effect on the duty cycle and the RMS drain current as V_{REFL} varies from 10V to 80V while holding V_{IN} at 30V, $P_{IN,max}$ for each of the interleaved flybacks at 125W, and C_{S1} at 10nF.

V_{REFL} (V)	10	20	30	40	50	60	70	80
δ	24.39%	38.47%	47.66%	54.12%	58.92%	62.62%	65.56%	67.96%
$I_{RMS,max,D}$ (A)	9.5	7.46	6.64	6.19	5.91	5.71	5.57	5.45

From *Table 4.3*, as V_{REFL} increases, δ increases while $I_{RMS,max,D}$ decreases. To further illustrate the findings, *Fig. 4.2* and *Fig. 4.3* are presented where *Fig. 4.2* demonstrates that the MOSFET drain current increases faster at the lower end of V_{REFL} while the variation is smaller as V_{REFL} gets larger. Fig. 4.3 illustrates the relation between V_{REFL} and the duty cycle.

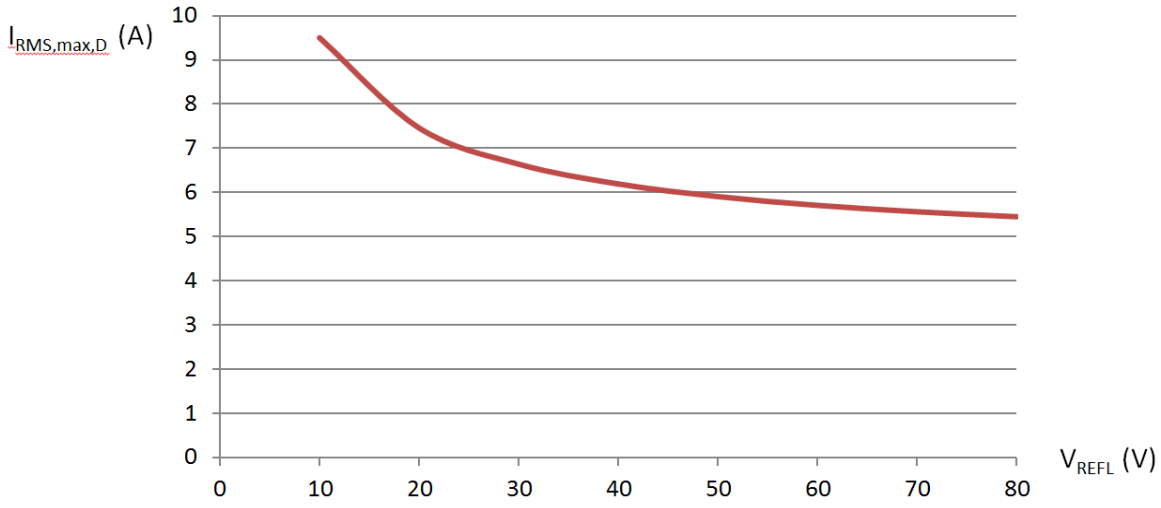


Figure 4.2: BCM flyback main switching MOSFET drain to source RMS current as V_{REFL} varies from 10V to 80V while holding V_{IN} at 30V, $P_{IN,max}$ for each of the interleaved flybacks at 125W, and C_{S1} at 10nF.

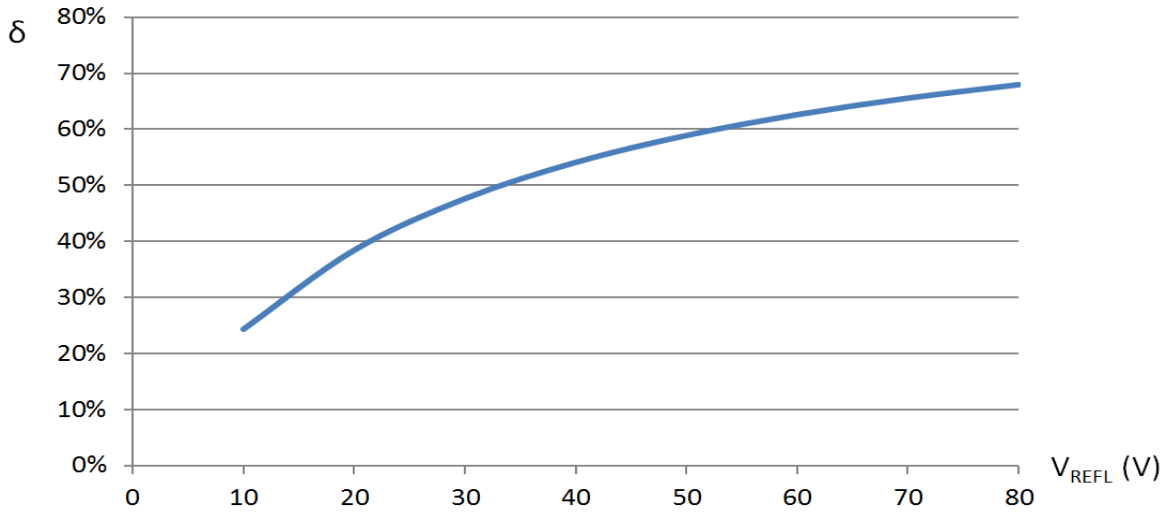


Figure 4.3: BCM flyback duty cycle (δ) increases as V_{REFL} increases from 10V to 80V while holding V_{IN} at 30V, $P_{IN,max}$ for each of the interleaved flybacks at 125W, and C_{S1} at 10nF.

Combining (105) and (107) leads to an expression for the MOSFET's conduction loss in terms of $r_{DS,ON}$, P_{IN}, V_{IN}, V_{REFL}, t_{ON}, and the operating frequency (f).

$$P_{COND,\max,M} \approx 4 r_{DS,ON} P_{IN,\max}{}^2 \left[\left(\frac{V_{IN,\min} + V_{REFL}}{V_{IN,\min} V_{REFL}} \right) \left(\sqrt{\frac{(t_{ON,\max})(f)}{3}} \right) \right]^2 \tag{108}$$

Where t_{ON} is given in (66) and f is calculated using (70).

Using the $r_{DS,ON}$ range found in *Table 4.2* and applying (108) to calculate the MOSFET's conduction loss ($P_{COND,max,M}$), it is found that $P_{COND,max,M}$ increases rapidly as V_{REFL} becomes smaller than V_{IN}, as illustrated in *Table 4.4* and *Fig. 4.4*.

Table 4.4: MOSFET conduction loss ($P_{COND,max,M}$) calculations based on (117), using the $r_{DS,ON}$ values in the data range provided in Table 4.1 while varying the output reflected voltage (V_{REFL}) from 10V to 80V. The input voltage (V_{IN}) is held at 30V, the input power ($P_{IN,max}$) for each of the interleaved flybacks at 125W, and C_{S1} at 10nF.

$r_{DS,ON}$ (Ω)	V_{REFL} (V)							
	10	20	30	40	50	60	70	80
	$P_{COND,max}$ (W)							
0.003	0.27	0.17	0.13	0.12	0.10	0.10	0.09	0.09
0.006	0.54	0.33	0.26	0.23	0.21	0.20	0.19	0.18
0.009	0.81	0.50	0.40	0.35	0.31	0.29	0.28	0.27
0.012	1.08	0.67	0.53	0.46	0.42	0.39	0.37	0.36
0.015	1.35	0.83	0.66	0.58	0.52	0.49	0.46	0.45
0.018	1.63	1.00	0.79	0.69	0.63	0.59	0.56	0.54
0.021	1.90	1.17	0.93	0.81	0.73	0.68	0.65	0.62
0.024	2.17	1.34	1.06	0.92	0.84	0.78	0.74	0.71
0.027	2.44	1.50	1.19	1.04	0.94	0.88	0.84	0.80

On the other hand, since;

$$V_{Q1,ON} \ll V_{IN} \tag{109}$$

And

$$\pi f \sqrt{L_{m1} C_{S1}} \ll 1 \tag{110}$$

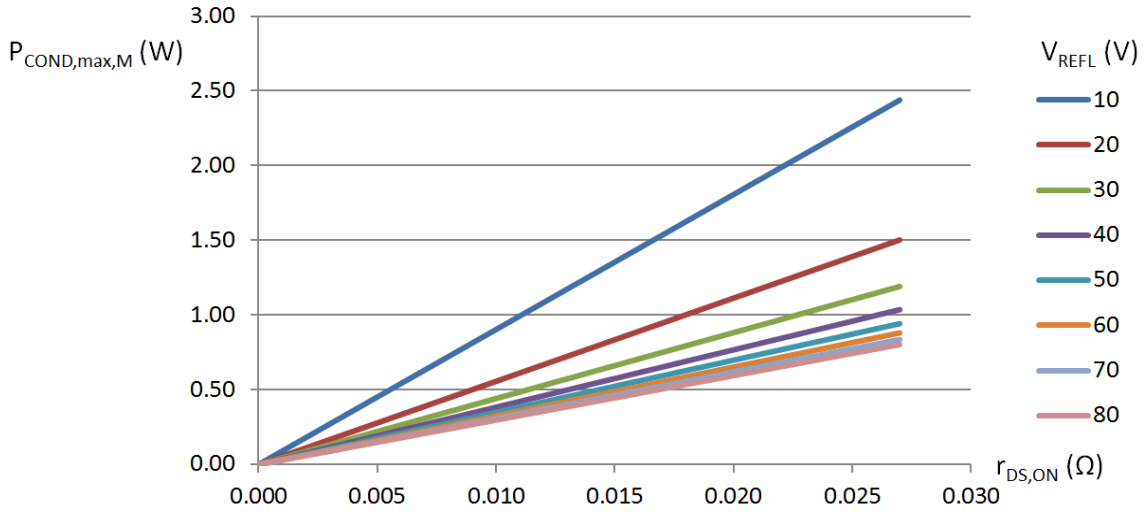


Figure 4.4: MOSFET conduction loss ($P_{COND,max,M}$) calculations based on (117), using the $r_{DS,ON}$ values in the data range provided in Table 4.1 while varying the output reflected voltage (V_{REFL}) from 10V to 80V. The input voltage (V_{IN}) is held at 30V, the input power ($P_{IN,max}$) for each of the interleaved flybacks at 125W, and C_{S1} at 10nF.

A simplified expression for t_{ON} is achieved:

$$t_{ON} \approx \frac{V_{REFL}}{f(V_{IN}+V_{REFL})} \tag{111}$$

Hence, simplifying (108), the MOSFET conduction loss expression is rewritten to be approximated in terms of $r_{DS,ON}$, P_{IN}, V_{IN}, and V_{REFL}:

$$P_{COND,\max,M} \approx \frac{4}{3} r_{DS,ON} \left(\frac{P_{IN,\max}}{V_{IN}}\right)^2 \left(\frac{V_{IN,\min}+V_{REFL}}{V_{REFL}}\right) \tag{112}$$

Applying (112) leads to the results presented in *Table 4.5*, with values that diverge from 2.46% to 6.55% when compared to the ones provided in *Table 4.4*.

It is worth noting that the data deviation of the said tables, at the lower values for V_{REFL}, is reduced when compared to the case where V_{REFL} is at its high end. Furthermore, when ignoring C_{S1}, as is the case in (112), the calculated MOSFET conduction loss becomes slightly higher than the case when C_{S1} is considered.

Table 4.5: MOSFET conduction loss ($P_{COND,max,M}$) is based on (121), using the $r_{DS,ON}$ values in the data range provided in Table 4.1 while varying the output reflected voltage (V_{REFL}) from 10V to 80V. The input voltage (V_{IN}) is held at 30V, the input power ($P_{IN,max}$) for each of the interleaved flybacks at 125W, and C_{S1} is ignored.

$r_{DS,ON}$ (Ω)	V_{REFL} (V)							
	10	20	30	40	50	60	70	80
	$P_{COND,max}$ (W)							
0.003	0.28	0.17	0.14	0.12	0.11	0.10	0.10	0.10
0.006	0.56	0.35	0.28	0.24	0.22	0.21	0.20	0.19
0.009	0.83	0.52	0.42	0.36	0.33	0.31	0.30	0.29
0.012	1.11	0.69	0.56	0.49	0.44	0.42	0.40	0.38
0.015	1.39	0.87	0.69	0.61	0.56	0.52	0.50	0.48
0.018	1.67	1.04	0.83	0.73	0.67	0.63	0.60	0.57
0.021	1.94	1.22	0.97	0.85	0.78	0.73	0.69	0.67
0.024	2.22	1.39	1.11	0.97	0.89	0.83	0.79	0.76
0.027	2.50	1.56	1.25	1.09	1.00	0.94	0.89	0.86

Hence, as a result of the data shown in *Table 4.4* and *Table 4.5*, the options revealed in *Table 4.2* could be narrowed down to the selections displayed in *Table 4.6*, where the corresponding conduction loss comparison is illustrated in *Fig. 4.5*.

Table 4.6: Unit cost and device parameters' comparison among MOSFET devices selected from Table 4.2 [30].

Manufacturer	Manufacturer Part Number	Unit Price (USD)	Drain to Source Voltage (Vdss)	Current - Continuous Drain (Id) @ 25°C	Rds On (Max) @ Id, Vgs	Gate Charge (Qg) @ Vgs	Input Capacitance (Ciss) @ Vds
Toshiba Semi.	TK72E08N1,S1X	$2.22	80V	72A (Ta)	4.3 mΩ @ 36A, 10V	81nC @ 10V	5500pF @ 40V
Toshiba Semi.	TK65E10N1,S1X	$2.66	100V	148A (Ta)	4.8 mΩ @ 32.5A, 10V	81nC @ 10V	5400pF @ 50V
Infineon Tech.	IPA075N15N3 G	$6.05	150V	43A (Tc)	7.5 mΩ @ 43A, 10V	93nC @ 10V	7280pF @ 75V

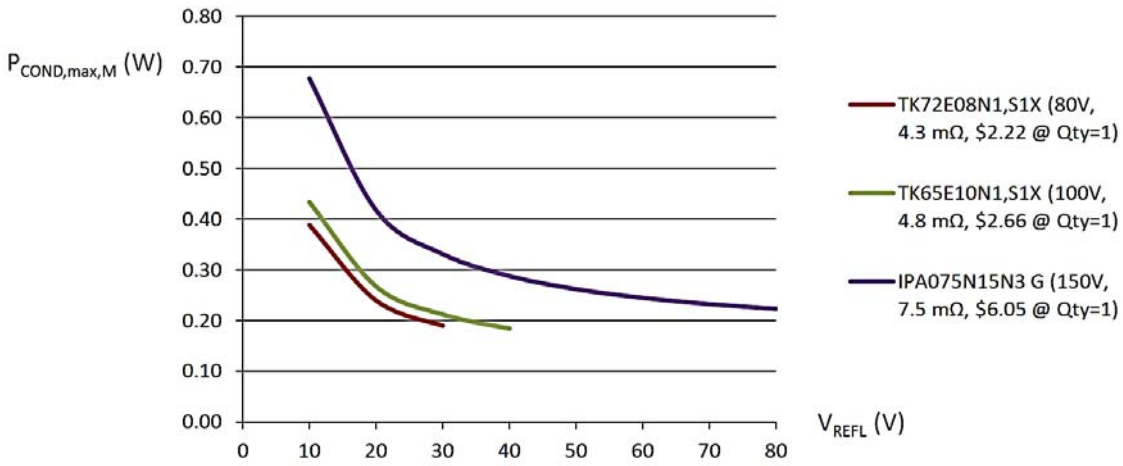


Figure 4.5: MOSFET conduction loss ($P_{COND,max,M}$) calculations based on (117), using the devices illustrated in Table 4.6, while varying the output reflected voltage (V_{REFL}) from 10V to 30V for the 80V device, 10V to 40V for the 100V device, and from 10V to 80V for the 150V device. The input voltage (V_{IN}) is held at 30V, the input power ($P_{IN,max}$) for each of the interleaved flybacks at 125W, and C_{S1} at 10nF.

From *Fig. 4.5*, it is conceivable to use the 80V MOSFET device (P/N: TK72E08N1,S1X; $r_{DS,ON}$ = 4.3 mΩ; cost = $2.2 at QTY = 1) while designing for V_{REFL} = 30V. Furthermore, the 100V MOSFET device (P/N: TK65E10N1,S1X; $r_{DS,ON}$ = 4.8 mΩ; cost = $2.66 at QTY = 1), which has a similar conduction loss at V_{REFL} = 40V (compared to the 80V device at V_{REFL} = 30V), should be the next choice for a V_{REFL} up to 40V. Moreover, the 150V device (P/N: IPA075N15N3 G; $r_{DS,ON}$ = 7.5 mΩ; cost = $6.05 at QTY = 1) costs significantly more with a higher conduction loss despite allowing V_{REFL} to reach 80V. Hence, the MOSFET selection optimization based on cost and conduction loss is achieved.

4-2-3 MOSFET Gate Charge Requirements

Typically, gate drive losses do increase with larger MOSFET's gate charge (Q_g) characteristics. However, since the Novel Low Cost PV Converter Based on Analog Interleaving Method MOSFET turn ON, starts at zero drain current and increases with the

slope illustrated in *Fig. 2.6*, as is the case in a BCM flyback, the turn ON gate current does not need to be high. Furthermore, since the gate drive at turn ON is separated from the turn OFF drive, as illustrated in the innovative drive circuits shown in chapter 5, the speed of the gate drive turn ON is less critical.

On the other hand, as illustrated in *Table 4.1 and Table 4.2*, at a given $r_{DS,ON}$, the gate charge requirements for the metal oxide N-channel MOSFETs increase as the device's voltage rating increases. Furthermore, for a given voltage rating metal oxide N-channel MOSFET, the gate charge requirements increase as the $r_{DS,ON}$ decreases. Moreover, the device's cost does increase with higher voltage ratings and lower $r_{DS,ON}$. Likewise, for the sake of cost and efficiency optimization, it is to the designer's advantage to select a low cost but suitably rated device, with the lowest possible $r_{DS,ON}$ and Q_g.

Hence, from *Table 4.6*, the gate charge requirements for the 80V and 100V devices are lower than that of the 150V. Optimizing for the unit cost and Q_g, it would be appropriate to select the 80V MOSFET device (P/N: TK72E08N1,S1X; $r_{DS,ON}$ = 4.3 mΩ; Q_g = 81 nC @ 10V; cost = $2.2 at QTY = 1) while designing for V_{REFL} = 30V. At a slightly higher cost and $r_{DS,ON}$, as a second optimization option, it would also be suitable to select the 100V MOSFET device (P/N: TK65E10N1,S1X; $r_{DS,ON}$ = 4.8 mΩ; Q_g = 81 nC @ 10V; cost = $2.66 at QTY = 1) while designing for V_{REFL} = 40V.

4-2-4 Metal Oxide versus Gallium Nitride

While the Gallium Nitride (GaN) devices are becoming less expensive, its cost is still relatively high, especially when applied in the cost sensitive PV converters or inverters. As an example, a 100V GaN (Digi-Key P/N: 917-1035-1-ND [30]) that is rated for a continuous

drain current of 25A, with a $r_{DS,ON}$ = 7 mΩ, is listed at a unit price of $12.82. This presents a significant cost disadvantage when compared to the $2.66 unit cost of a metal oxide device (P/N: TK65E10N1,S1X) that has an $r_{DS,ON}$ = 4.8 mΩ.

On the other hand, the GaN device presents some significant advantages in its lower gate charge requirement ($Q_{g,max}$ = 10nC at 5V), where the TK65E10N1,S1X requires a Q_g = 81 nC @ 10V. Furthermore, the input and output capacitances of the 917-1035-1-ND GaN device (C_{iss} = 850 pF; C_{oss} = 450 pF) are negligible when compared to the TK65E10N1,S1X metal oxide device (C_{iss} = 5400 pF; C_{oss} = 950 pF). This gives the GaN device noteworthy benefits in switching speeds when compared to that of the metal oxide. This could allow the operation in higher switching frequencies, which could result into smaller size magnetics. However, as an example that is illustrated in *Table 4.7*, the cost of a smaller size ferrite core (RM12) versus a one larger size (RM14) does not offset the price differential of using a gallium nitride versus a compatible metal oxide MOSFET. Therefore, the potential savings due to smaller size magnetics do not yet offset the cost differential of gallium nitride versus the metal oxide.

Furthermore, GaN does not have avalanche capability while the Silicon device does. Hence, while selecting a GaN device for a given application, a higher drain to source voltage margin must be considered, allowing for worse case voltage overshoot ($V_{DS,OS}$) that typically occurs at startup and at overcurrent conditions. This could impose the selection of a higher voltage rated GaN device than what could have been feasible if a silicon device was to be used, resulting into an even higher cost differential.

Table 4.7: 100V GaN & RM12 core set versus 100V silicon & RM14 core set comparison [30].

Manufacturer Part Number	**Core size**	**Ve (mm3)**		**Ae (mm2)**		**Unit Price (USD)**
B65815E0000R097	RM12	8320 or 6195		146		$4.74
Type (Manufacturer Part Number)	**Drain to Source Voltage (Vdss)**	**Current - Continuous Drain (Id) @ 25°C**	**Rds On (Max) @ Id, Vgs**	**Gate Charge (Qg) @ Vgs**	**Input Capacitance (Ciss) @ Vds**	**Unit Price (USD)**
GaN (EPC2801)	100V	25A (Ta)	7 mOhm @ 25A, 5V	10nC @ 5V	950pF @ 50V	$12.83
Total 100V rated GaN + RM12 cost						**$17.57**
Manufacturer Part Number	**Core size**	**Ve (mm3)**		**Ae (mm2)**		**Unit Price (USD)**
B65887E0000R097	RM14	14000 or 10230		200		$7.92
Type (Manufacturer Part Number)	**Drain to Source Voltage (Vdss)**	**Current - Continuous Drain (Id) @ 25°C**	**Rds On (Max) @ Id, Vgs**	**Gate Charge (Qg) @ Vgs**	**Input Capacitance (Ciss) @ Vds**	**Unit Price (USD)**
Silicon (TK65E10N1,S1X)	100V	148A (Ta)	4.8 mΩ @ 32.5A, 10V	81nC @ 10V	5400pF @ 50V	$2.66
Total 100V rated silicon MOSFET + RM14 cost						**$10.58**

4-3 Magnetic Design Optimization

Cost, size, and losses are the key elements considered in the design optimization of the magnetics used in power electronics' converters or inverters. In this Novel Low Cost PV Converter Based on Analog Interleaving Method, the two switching transformers, which are operating as interleaved BCM flybacks, are the magnetics used. In order to minimize the core losses, while reducing the transformers' cost and printed circuit board (PCB) footprints, the duty cycle and operating frequency need to be optimized.

4-3-1 Ferrite Core Losses

The core loss curves shown in *Figure 3.2* are based on ideal sinewave applications [27]. However, in most switch mode power supplies (SMPS) the waveforms are not sinusoidal but are mostly rectangular, triangular, etc. Since the applied waveform shapes, the amplitude of the cyclical flux density, the hysteresis of the selected material, and the operating temperature determine the selected core magnetic power dissipation, it is imperative that a more relevant method be used in order to determine the core losses in a given application.

An accessible "Ferrite Magnetic Design Tool" is offered by EPCOS [27] that provides a mathematical model designed for the calculation of core losses. The model greatly assists in the selection of the ferrite material that is most appropriate for the application. It takes into account the actual applied waveform of the magnetic flux and the model is based on equations derived in [27], starting from the Steinmetz equation that is based on a sinusoidal waveform such that:

$$p_{v\sin} = C_m f^x B^y (c_{t2} T^2 - c_{t1} T + c_{t0}) \tag{113}$$

Where, p_{vsin} is defined as the loss density in a ferrite core with a sinusoidal waveform applied, B is the magnetic flux density amplitude, f is the operating frequency, T is the operating temperature, x and y are the Steinmetz frequency and induction exponents respectively defined for the operating condition, and C_m, C_{t1}, C_{t2} and C_{t0} are material constants. Furthermore, [27] uses Albach, Durbaum and Brockmeyer equation extended for non-sinusoidal waveforms of the magnetic flux density in order to derive an equation for the ratio (r^{x-1}) of the actual core loss to its sinusoidal signal value while maintaining identical

operating temperature, frequency, and amplitude of the flux density. The derivations in [27] for r^{x-1} resulted in the following:

$$r^{x-1} = \frac{p_{vgen}}{p_{v\sin}} \tag{114}$$

Where p_{vgen} is defined as the general non-sinusoidal waveforms of the magnetic flux density and is provided by [27] as:

$$p_{vgen} = fC_m f_{\sin eq}{}^{x-1} B^y (c_{t2}T^2 - c_{t1}T + c_{t0}) \tag{115}$$

Also given in [27] that f_{sineq} is defined as the equivalent sinusoidal frequency, such that:

$$f_{\sin eq} = \frac{2}{\pi^2} \sum_{k=2}^{k} \left(\frac{B_k - B_{k-1}}{B_{\max} - B_{\min}} \right)^2 \frac{1}{t_k - t_{k-1}} \tag{116}$$

And the variable r as,

$$r = \frac{f_{\sin eq}}{f} \tag{117}$$

Conveniently, [27] provides an equation for r for the flyback converter with discontinuous current path, which is also applicable to the BCM flyback where t_{OFF2} is the dead time.

$$r = \frac{2}{\pi^2} \frac{\xi}{\delta(\xi - \delta)} \tag{118}$$

Such that,

$$0 < \delta < \xi \leq 1 \tag{119}$$

Where, δ is the duty cycle of the converter (or inverter), ξ is defined as the extinction cycle and could be found from equation (118) and is illustrated in *Fig. 4.6* as follows:

$$\xi = \frac{t_{ON} + t_{OFF1}}{T_S} = 1 - \frac{t_{OFF2}}{T_S} \tag{120}$$

Assuming that V_{REFL} = V_{IN} = 30V, L_{m1} = 14 μH, and C_{S1} = 15 nF, using the EPCOS "Ferrite Magnetic Design Tool ver.5.2.1." for the core and material selection [28], selecting 50 kHz as the operating frequency, 200 mT as the flux density, and 80°C as the operating temperature, the resulted core losses for the N95 and N97 ferrite materials in a DCM flyback are shown in *Fig. 4.7*.

Based on *Fig. 4.7*, at the assumed values given above, the core losses of the N97 material are higher than that of the N95 material for frequencies below 200 kHz. For example, at 50 kHz, the core losses for the N97 material are 117 kW/m^3 while it is 107 kW/m^3 for the N95 material. Similarly, the losses for N97 = 57.2 kW/m^3 while for N95 = 48.4 kW/m^3 at 30 kHz. Hence, the core losses calculations presented in *Table 3.1* and *Table 3.2*, which are based on a sinusoidal signal, are higher than what is shown in *Fig. 4.7*.

On the other hand, based on the results of the core losses versus operating frequency presented in *Fig. 4.7*, for a given flux density (*B*), it becomes obvious that lower losses are achieved at lower operating frequencies. Conversely, from *Table 3.1* and *Table 3.2*, we have learned that increasing the operating frequency in order to lower *B* present core loss advantages. However, since increasing the operating frequency could result in additional losses in other areas of the converter or inverter, such as the main switching MOSFET Gate drive, turn ON and turn OFF switching losses, etc., optimization of the said operating frequency need to be considered in order to minimize the overall losses.

Since many interdependent variables (cost, losses, and physical dimensions of the main switching MOSFETs, transformers, gate drive circuit, output rectifiers, etc.) are involved, optimization is rarely achievable by a single iteration. Hence, the steps described in sections 3-2-1 and 3-5-2 need to be implemented.

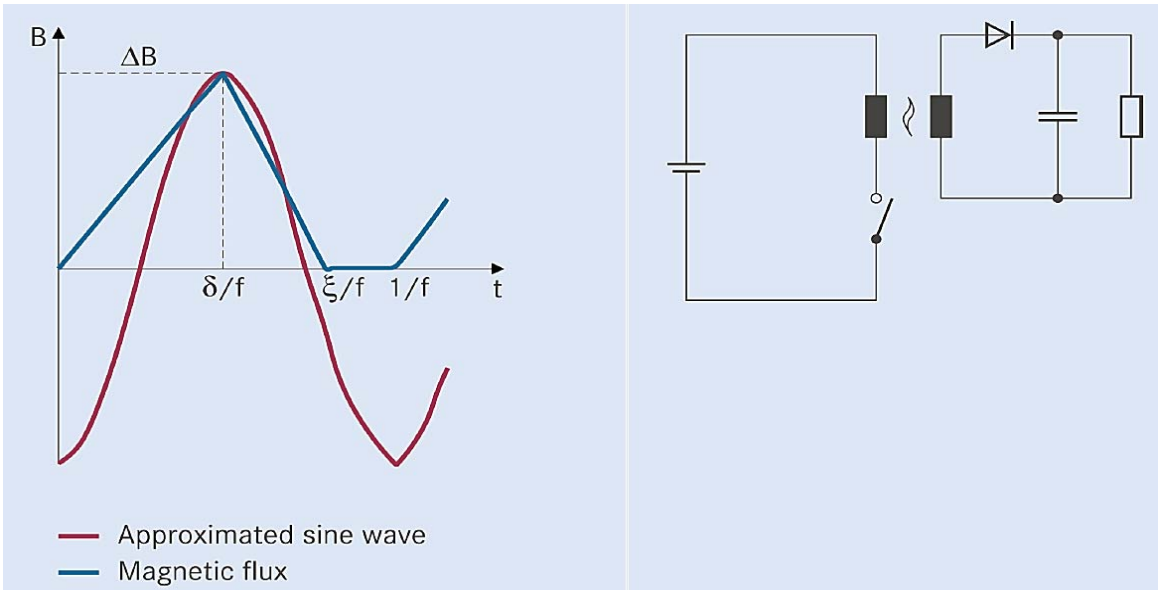


Figure 4.6: Flyback converter with discontinuous current path [27]. This is also applicable to BCM flyback where the deadtime is equal to t_{OFF2} given in equation (24).

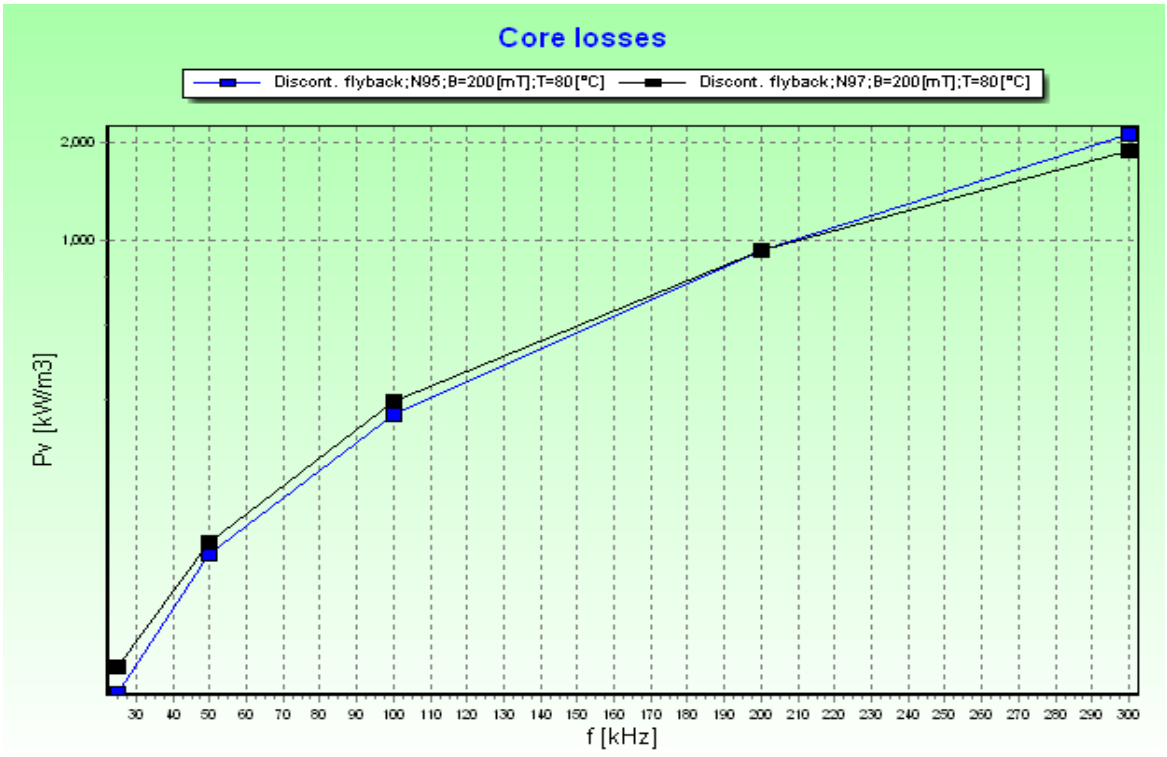


Figure 4.7: Core losses versus operating frequency, N97 and N95 comparison, using the EPCOS "Ferrite Magnetic Design Tool ver.5.2.1." for the core and material selection for the DCM Flyback converter [28], which is also applicable for a BCM flyback with a deadtime equal to t_{OFF2}, as given in equation (24). Assuming that $V_{REFL} = V_{IN} = 30$V, $L_{m1} = 14$ µH, $C_{S1} = 15$ nF, $f = 50$ kHz, $B = 200$ mT, and T = 80°C.

4-3-2 Duty Cycle Optimization for Minimum Core Losses

An additional interesting feature provided by [28] is related to core losses versus the duty cycle of the converter or inverter. *Fig. 4.8* is an illustration of the said feature, where the ratio of the actual core loss to its sinusoidal signal value (r^{x-1}) is less than one, for both the N95 and N97 materials, for values of the duty cycle from 0.3 to 0.62. Based on *Fig. 4.8*, minimum core losses occur where the duty cycle is from 40% to 50%. Using *Table 4.3*, this translates to V_{REFL}, where:

$$23V < V_{REFL} < 34V \tag{121}$$

Therefore, having V_{REFL}, as defined in (121), not only allows for an optimizing the duty cycle for reducing the ferrite core losses, but it also coincides with section 4-2 findings.

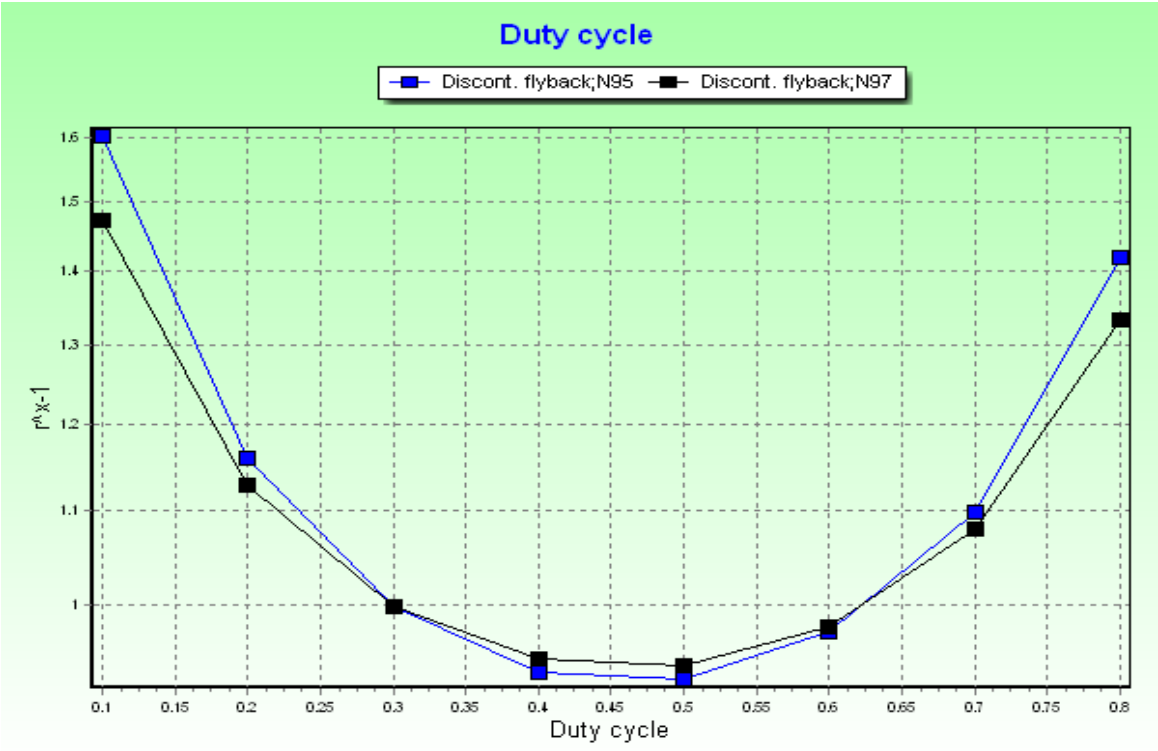


Figure 4.8: Ratio of the actual core loss to its sinusoidal signal value (r^{x-1}) versus the duty cycle, N97 and N95 comparison using the EPCOS "Ferrite Magnetic Design Tool ver.5.2.1." for the core and material selection for the DCM Flyback converter [27], which is also applicable for a BCM flyback with a deadtime equal to t_{OFF2}, as given in equation (25). Assuming that $V_{REFL} = V_{IN} = 30V$, $L_{m1} = 14$ µH, $C_{S1} = 15$ nF, $f = 50$ kHz, $B = 200$ mT, and T = 80°C.

4-4 Minimum Operating Frequency Selection Optimization

The proper selection of the minimum operating frequency (f_{min}) of the variable frequency BCM flyback, referred to in section 3-3-1, is a crucial design optimization step. As previously discussed, increasing the operating frequency leads to increasing the switching losses while potentially decreasing the size of the switching transformers. As illustrated in *section 4-2-4*, the potential savings due to smaller size magnetics do not yet offset the cost differential of gallium nitride versus the metal oxide. Hence, the use of a metal oxide device is assumed in this section.

From the experimental results that are detailed in chapter 6, as illustrated in *Fig. 4.9*, the MOSFET's turn OFF losses is the area of the approximately isosceles triangle, shown encircled in red, times the operating frequency (f). Let $P_{off,M}$ be the MOSFET's turn OFF losses, b and h be the base and height of the said triangle respectively. Based on *Fig. 4.9*, b is approximately 100 *ns* and h is around 200W. Hence,

$$P_{off,M} \approx \frac{bh}{2} f = \frac{200 \times 100 \times 10^{-9}}{2} f = 10^{-5} f = kf \tag{122}$$

The 10^{-5} factor (k) needs to be adjusted based on the selected MOSFET and how well the turn OFF circuit performs. However, in this application, it is assumed that this is a typical turn OFF crossover for the selected 80V voltage rated metal oxide device. Furthermore, as commonly known, the associated turn OFF losses is directly proportional to the operating frequency.

In section 3-3-2, it was discussed that with a selected ferrite core size and material, increasing the operating frequency, while holding the same number of winding turns, resulting in decreasing the core flux density (B) swing, lowers the core losses. *Table 3.1*

indicated that 1.4W @ 100ºC would be the losses for an RM14 size core, N97 material, operating at a flux density of 2000 mT and an operating frequency of 50 kHz. Furthermore, *Table 3.2* showed that 0.63W @ 100ºC would be the losses for the same ferrite core if the flux density were to be 1000 mT at an operating frequency of a 100 kHz, a gain of 0.77W.

However, based (122) and *Fig. 2.9*, the MOSFET's turn OFF losses at higher frequencies significantly exceed the aforementioned 0.77W gain, especially that it is doubled due to the presence of 2 MOSFETs, namely Q_1 and Q_2, as shown in *Fig. 2.2*. *Fig. 2.9* indicated that with a design example, which was demonstrated experimentally, starting at f_{min} of a 28 KHz, letting $L_{m1} = 15\mu H$; $V_{REFL} = V_{IN} = 30V$; and $C_{S1} \approx$ 10nF, the frequency variations based on equation (51) is approximately 6.5:1 (182 kHz to 28 kHz) as the input power varied from 250W down to 25W. *Fig. 4.10* illustrates that the turn OFF losses at 182 KHz is 1.82W for Q_1 and 3.64W for Q_1 and Q_2 combined.

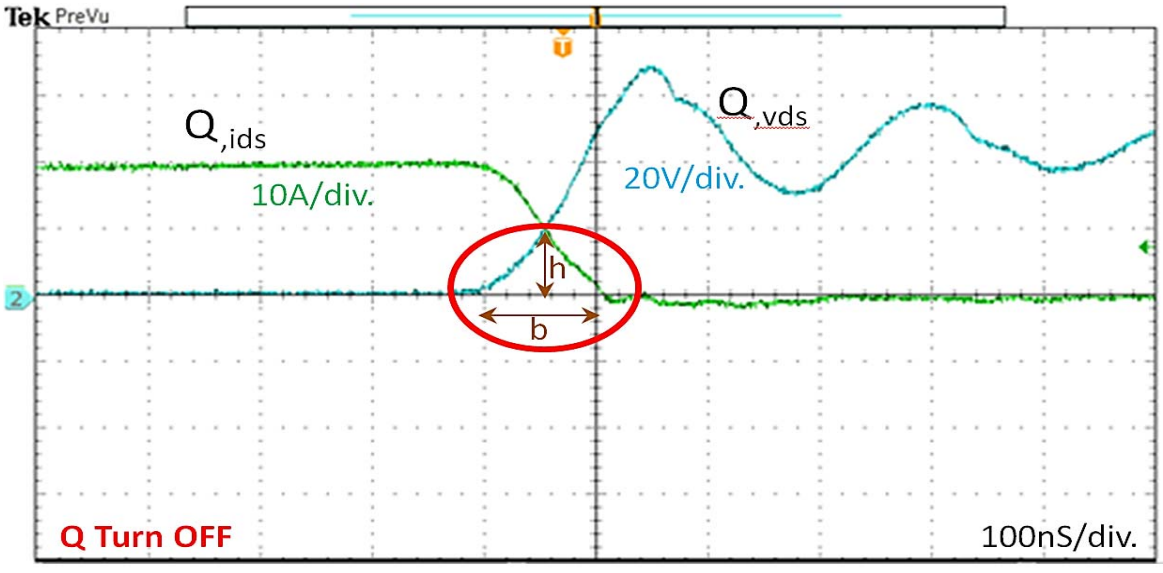


Figure 4.9: Experimental results showing the drain to source voltage and current waveforms crossover of a power MOSFET used in the Novel Low Cost PV Converter Based on Analog Interleaving Method at turn OFF. The time scale is at 100nS/div., the voltage and current scales are 20V/div. and 10A/div. simultaneously. The data was taken at full input power of 250W, where each of the interleaved flyback sees 125W. The input voltage V_{IN} = 30V.

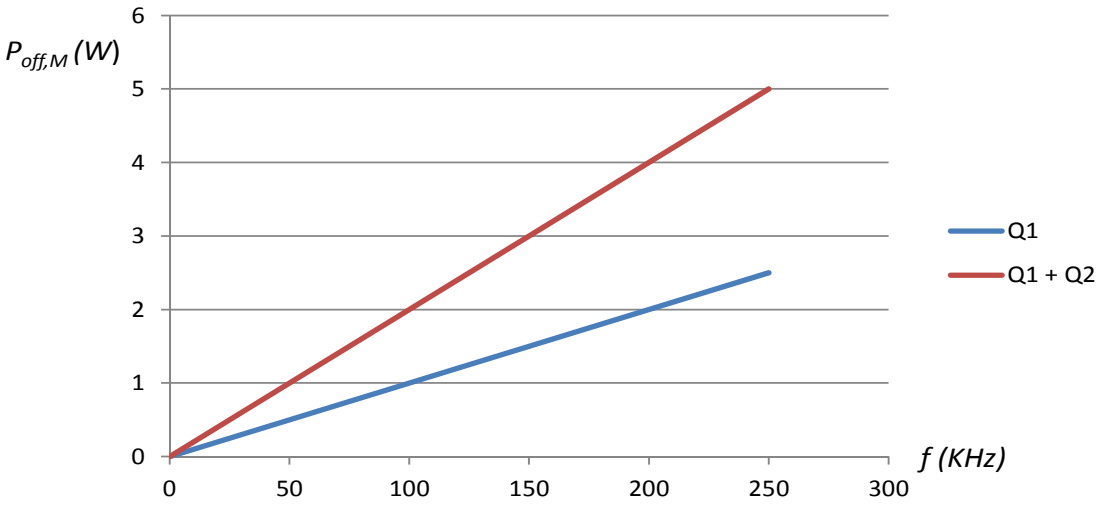


Figure 4.10: Turn OFF losses of Q_1 and $Q_1 + Q_2$ versus the operating frequency in an interleaved BCM flyback.

Therefore, in order to optimize the selection of the minimum operating frequency, the following steps need to be considered:

1) Since the total MOSFET losses are the sum of the conduction losses ($P_{COND,max,M}$), the turn OFF losses ($P_{off,M}$), and the turn ON losses ($P_{on,M}$) that includes the gate losses [34], such that:

$$P_{total,M} = P_{cond,M} + P_{off,M} + P_{on,M} \tag{123}$$

Where, in this section the turn ON gate losses are ignored (including such losses would only support the argument presented). Select the minimum operating frequency to be as low as needed to insure that $P_{off,M}$ is sufficiently low such that $P_{total,M}$ does not cause the device's temperature rise, under worst case operating conditions, to reach the associated maximum datasheet specified temperature.

2) Once the MOSFET and the minimum operating frequency are chosen, select the appropriate ferrite core size based on the procedures described in chapter 3. Iterations might be necessary in order to achieve the desired optimization results.

4-5 Phase Shading Optimization

Phase shading is employed in order for the converter or inverter to become more efficient at lower input power conditions. The converter's operating frequency increases, as previously discussed in this document, due to input power decrease that occurs at lower PV irradiations. The point where only one of the interleaved flyback operates, which effectively doubles the power of such a flyback in order to cut the operating frequency in approximately half, is defined as phase shading.

In order to optimize the operating point where phase shading is employed, equations (43), (112) and (122) along with the core losses shown in *Fig. 4.7* and the frequency versus input power results illustrated in *Fig. 2.9* could be used. Phase shading should occur where the transformer and MOSFET losses are optimized at a given operating frequency, as defined in (51) and approximated in (43). Therefore, assuming that P_{total} is the sum of the MOSFET conduction losses ($P_{COND,max,M}$), MOSFET turn OFF losses ($P_{off,M}$), MOSFET turn ON losses ($P_{on,M}$), gate drive losses ($P_{dr,M}$), transformer core losses (P_{core}), and transformer winding losses (P_{wd}). Hence,

$$P_{total} = P_{cond,M} + P_{off,M} + P_{on,M} + P_{dr,M} + P_{core} + P_{wd} \tag{124}$$

The optimum phase shading point occurs where the derivative of P_{total} with respect to the input power (P_{IN}) or with respect to the operating frequency (f) is equal to zero. Such that,

$$\frac{dP_{total}}{dP_{IN}} = \frac{d}{dP_{IN}}(P_{cond,M} + P_{off,M} + P_{on,M} + P_{dr,M} + P_{core} + P_{wd}) = 0 \tag{125}$$

Based on (125), $r_{ds,ON}$ and the k factor defined in (122) significantly affect the phase shading point. However, for a meaningful solution, additional losses are dependent and introduced by the board layout. This includes the routings and the thickness of the lands on

the PCB, where such losses need to be added as additional losses in (124). Since such losses are not easily predictable, due to the uniqueness of each PCB layout, the phase shading optimization point is best achieved experimentally. Once the PCB layout is completed and sufficient prototype testing is achieved, the control parameters related to phase shading could be set based on experimental results. Such method should provide much more accurate results than that of a theoretical one, which typically lacks details related to the layout, component selections, and component characteristics.

4-6 Silicon versus SiC for the Output Rectifier

Fig. 4.11 illustrates the waveforms for T_1's primary and secondary windings' voltage as well as the output rectifier's (D_1) current, where T_1 and D_1 are shown in *Fig 2.2*.

Prior to the start of the ON time of the master flyback's MOSFET (Q_1), as shown in *Fig. 4.11*, just after the current in D_1 reaches zero, T_1's primary voltage resonates down to zero during t_{OFF2}. As stated in chapter 2, the said resonance is mainly due to C_{S1} and the primary magnetizing inductance. Simultaneously, by transformer action, a voltage resonance is also seen at the secondary winding during t_{OFF2}. Therefore, immediately after its current reaches zero, the *dv/dt* seen by D_1 during t_{OFF2} is reduced, which makes the typical reverse recovery concern to be less of an issue. *Fig. 4.*12 presents the experimental results using an ultra-fast recovery glass passivated rectifier, 821-HS3K [31], for D_1. In the said figure, the current waveforms of D_1 and Q_1's drain to source, along with Q_1's drain to source voltage are shown.

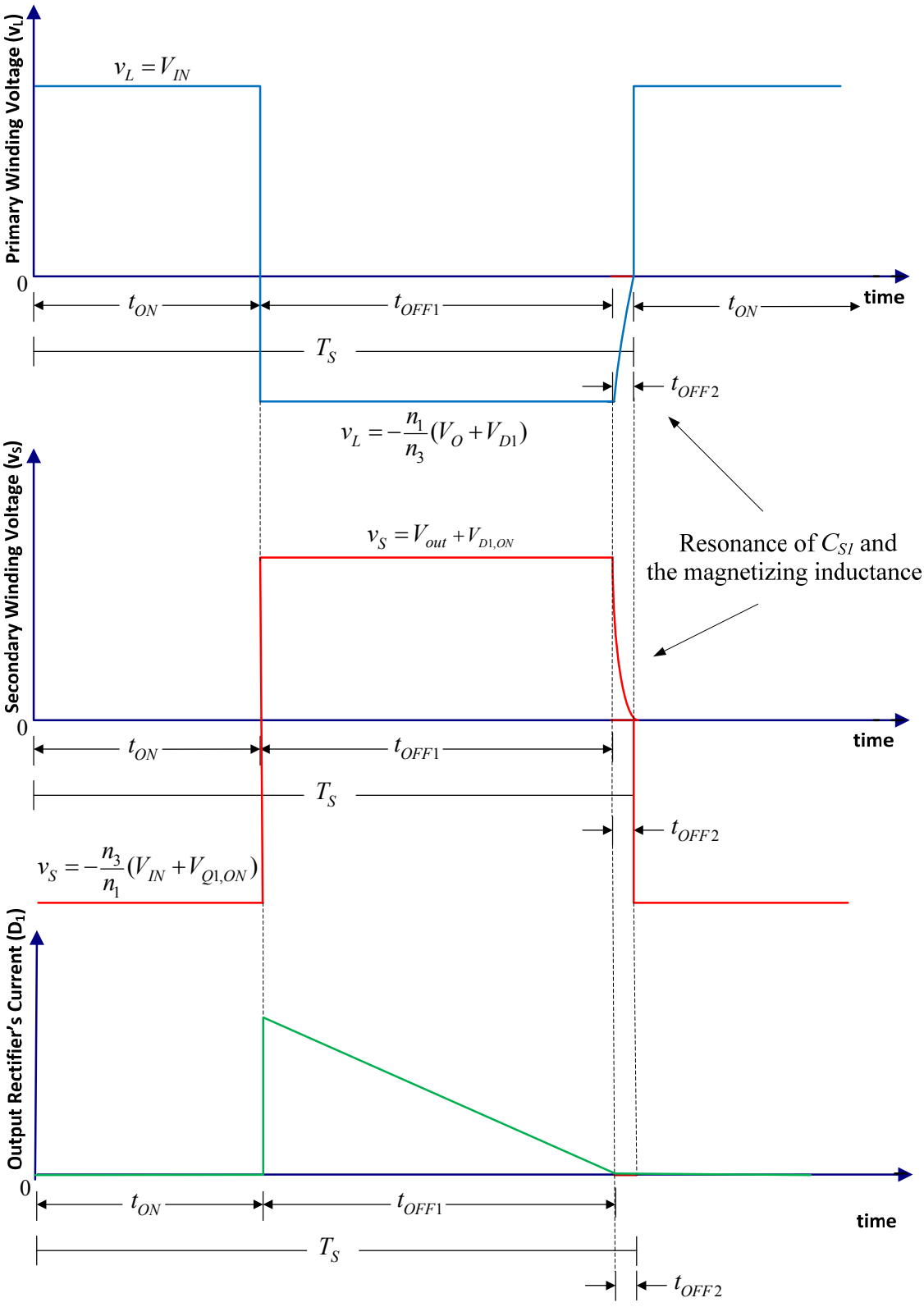


Figure 4.11: waveforms for T_1's primary and secondary voltage as well as D_1's current.

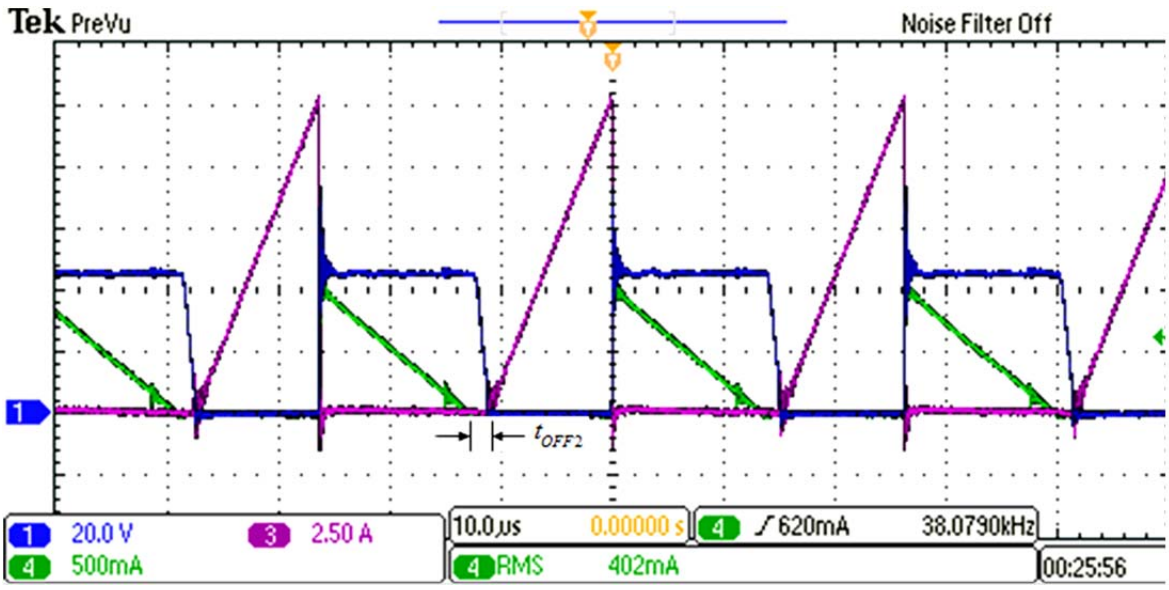


Figure 4.12: Experimental results illustrating the master flyback's current waveforms of the output rectifier (D_1 in green) and the drain to source of MOSFET (Q_1 in pink) along with Q_1's drain to source voltage (in blue).

From the current waveforms illustrated in *Fig. 4.12*, it is evident that the reverse recovery for D_1 and D_2 are approximately zero. On the other hand, *Table 4.8* presents a comparison between the Silicon Carbide (SiC) and the ultra-fast recovery glass passivated rectifiers.

Table 4.8: Comparison between the Silicon Carbide (SiC) and the ultra-fast recovery glass passivated rectifiers.

Supplier's Part Number	Unit Price (USD)	Reverse Voltage	Forward Current	Max Surge Current	Recovery Time	Forward Voltage	Technology
821-HS3K	$0.41	800V	3A	150A	75nS	1.7V	Glass passivated junction chip
941-C3D03065E	$1.54	650V	3A	26A		1.8V	SiC

By comparing the 2 rectifiers, illustrated in Table 4.8, the 75 nS recovery time is the only disadvantage that the glass passivated type has. However, as presented in *Fig. 4.12*, one

of the benefits of the proposed scheme is that the reverse recovery is either eliminated or greatly reduced. Hence, the added cost presented by using the SiC device ($1.54 versus $0.41) is not justified, especially that it would need to be used twice (D_1 and D_2).

4-7 Conclusion

In this chapter, the design optimization for the Novel Low Cost PV Converter Based on Analog Interleaving Method was detailed. Design optimization considerations and related derivations for the selection of the BCM flybacks power MOSFETs were discussed. This included the optimization for the MOSFET's conduction losses, gate charge requirements, and a comparison between the metal oxide and the gallium nitride devices. The study illustrated the cost and performance advantages of suitable lower voltage rated MOSFETs over the higher voltage rated ones, where several commercially available MOSFET devices were compared. Furthermore, it was determined that the advantages of having slightly lower switching losses, as offered by the gallium nitride, do not as of yet offset the significantly lower cost featured by its metal oxide counterpart.

Optimization of the magnetics was also discussed to include the core selection based on minimizing the cost, losses, and printed circuit board's footprints. Moreover, the optimization of the duty cycle in an effort to reduce the core losses in a BCM flyback was discussed. Additionally, optimizing the selection of the output rectifier was detailed, illustrating the advantages of the scheme in significantly reducing the reverse recovery, allowing for the use of a low cost glass passivated device.

Chapter 5: Circuit Design Innovations Implemented In the Novel Low Cost PV Converter Based on Analog Interleaving Method

5-1 Overview

In order for the power electronics to be low cost, the panel side DC/DC converter design needs to be supportive to the implementation of a straightforward second stage DC/AC inverter's requirements (or second stage DC/DC central converter, as required by the application). Furthermore, since this is a two-stage system, it is imperative to come up with an innovative low cost panel side DC/DC converter. In line with such objectives, in this chapter, low cost analog innovative circuits that perform critical functions for implementing the proposed master/slave interleaved flyback methodology are presented. Such novel circuits relate to start-up, turn ON, turn OFF, and control, where some of the said circuits are integrated and serving multiple functions while eliminating the need for an auxiliary start up power supply. Furthermore, by using the said circuits, no clock or pulse width modulator chips (PWM) are needed, which further serve in reducing the cost.

On the other hand, power electronics' high efficiency is a critical feature in PV solar applications. Therefore, soft switching is a key element in the performance of the proposed interleaved variable frequency flybacks operating in the boundary conduction mode. The turn ON circuit presented in the chapter includes a zero voltage switching (ZVS) arrangement that insures that each of the flyback initiates its turn ON when the MOSFET's drain voltage is very close to zero.

5-2 Novel Startup Circuit

Not requiring an auxiliary startup supply would result into lowering the cost and eliminating related undesired losses. The innovative startup circuit presented in *Fig. 5.1* is a low cost circuit, suitable for the proposed novel low cost PV converter based on analog interleaving method, which does not require the said auxiliary startup supply. Furthermore, the circuit does not require a pulse width modulator chip (PWM chip). It uses very low cost discrete components that not only serves for the converter's startup but it also establishes a bias voltage that also works for other functions, which will be described in later sections of this chapter.

The sequence of the startup circuit is shown in *Fig. 5.2*, which functions as follows:

1) Once the input voltage becomes available, capacitor C_1 charges through the high impedance resistor, R_1.
2) Once the voltage across C_1 (V_{bias}) reaches the breakpoint of the zener diode D_4 ($V_{D4,th}$), the current through R_2 and R_3 starts flowing until the voltage across R_2 becomes sufficient to turn ON the pnp bipolar transistor Q_3.
3) The turn ON of Q_3 results into:
    a. The turn ON of the npn bipolar transistor Q_4, which pulls the voltage across D_4 down to the saturation voltage of Q_4.
    b. The turn ON of the npn bipolar transistor Q_5, which turns ON the pnp bipolar transistor Q_6.
4) Once Q_6 turns ON, V_{bias} minus the voltage drops across R_9 and the saturation voltage of Q_6 becomes available at the gate of MOSFET Q_1, which results into Q_1's turn ON. R_9 serves to limit the current supplied by C_1.

5) Once Q_1 turns ON, the input voltage (V_{IN}) will be seen across the primary winding n_1, where the dot end of the winding n_1 is positive.

6) By transformer action, the dot end of the drive winding (n_3) will be positive to a voltage level equal to V_{IN} times the ratio of n_3 and n_1, as described in (76).

7) This results into reinforcing Q_1's drive until its ON time is terminated, which is described in a later section of this chapter.

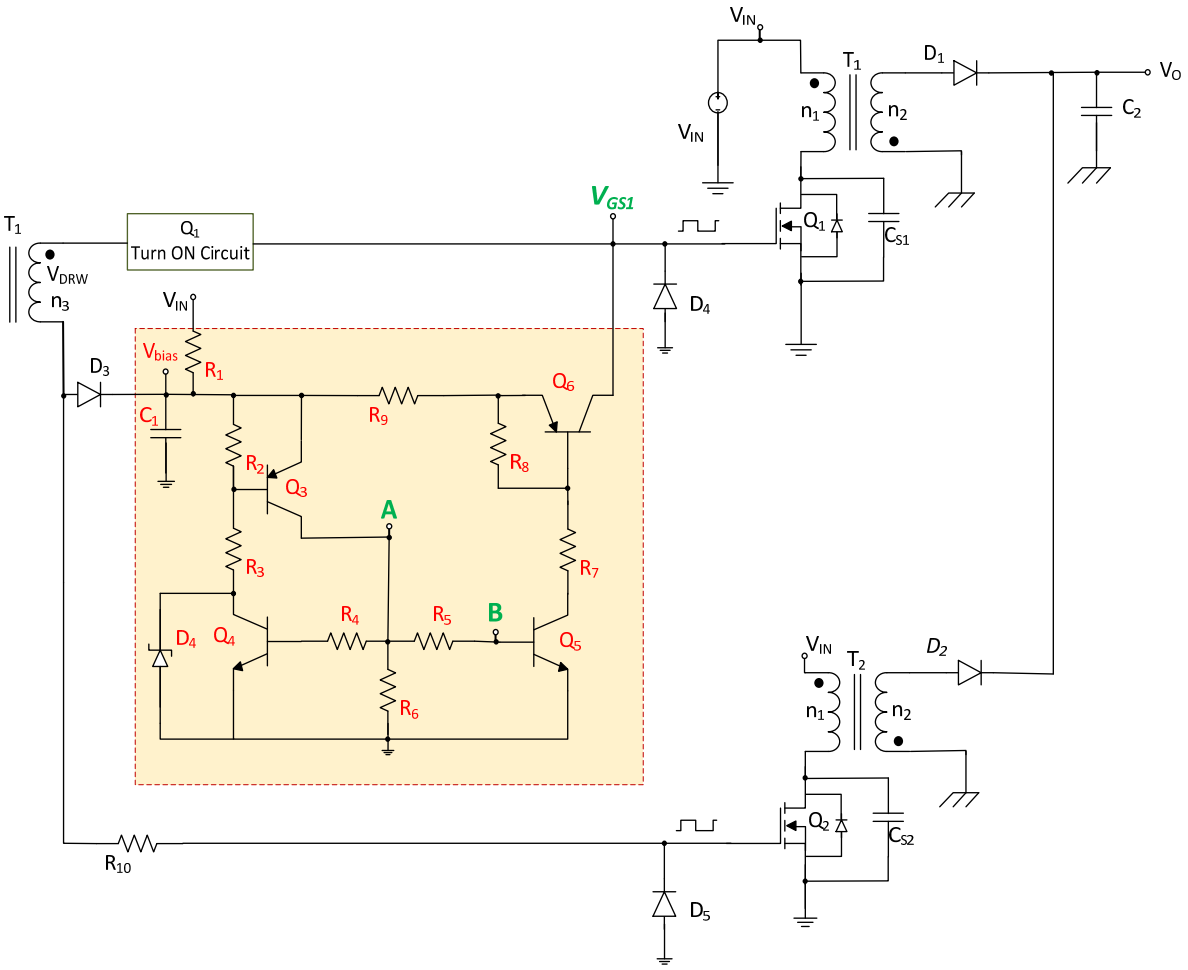


Figure 5.1: Novel startup circuit.

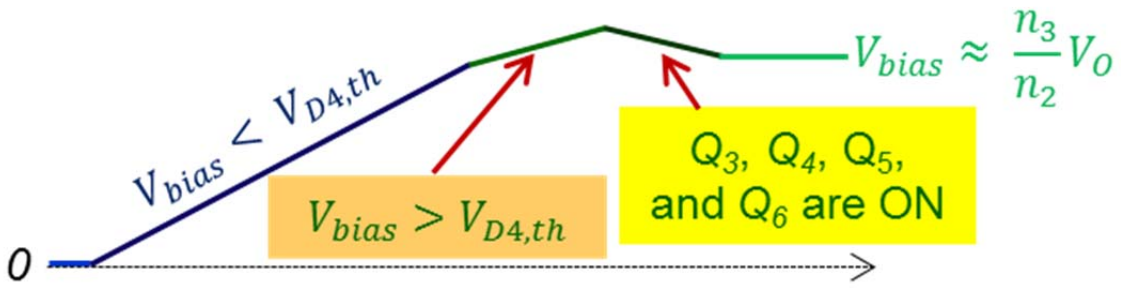


Figure 5.2: Novel startup circuit sequence.

5-3 Main Switching Devices Novel Turn ON Circuit

Fig. 5.3 illustrates an innovative turn ON circuit for the main switching devices, Q_1 and Q_2. No clock or PWM or driver module chips are used; the circuit uses low count of very low cost discrete components instead.

After the startup sequence is established, the turn ON circuit functions as follows:

1) As shown in *Fig. 5.4*, once all the stored energy in the primary winding is delivered to the secondary, hence accomplishing the master flyback's zero-current-detection (ZCD), the primary voltage dot end of the drive winding (n_3) becomes positive to a voltage level equal to V_{IN} times the ratio of n_3 and n_1.
2) At that instant, the pnp bipolar transistor Q_8 is OFF while D_6 blocks the drive winding from reinforcing Q_1's gate drive. However, C_3 gets charged through D_5, R_{10}, the drive winding, and R_{10} path. Once the voltage across C_3 reaches the emitter to base turn ON threshold of Q_7, it turns ON to cause Q_8 to turn ON. This allows the drive winding to supply the necessary voltage in order to drive the gate of Q_1 to establish $t_{ON,Q1}$. In order to achieve Q_1's zero voltage switching (ZVS), the time to charge C_3 that enables Q_8 to turn ON is designed to be equal to t_{OFF2}, which is discussed in chapter 2.

3) Once $t_{ON,Q1}$ is terminated, the drive winding changes polarity where the non-dotted end becomes positive. This establishes the D_4, D_6, drive winding, R_{10}, and $V_{GS,Q2}$ path, hence starting the ON time for Q_2. As further discussed in section 5-5, the ON time of Q_2 is simply a copy of that of Q_1.

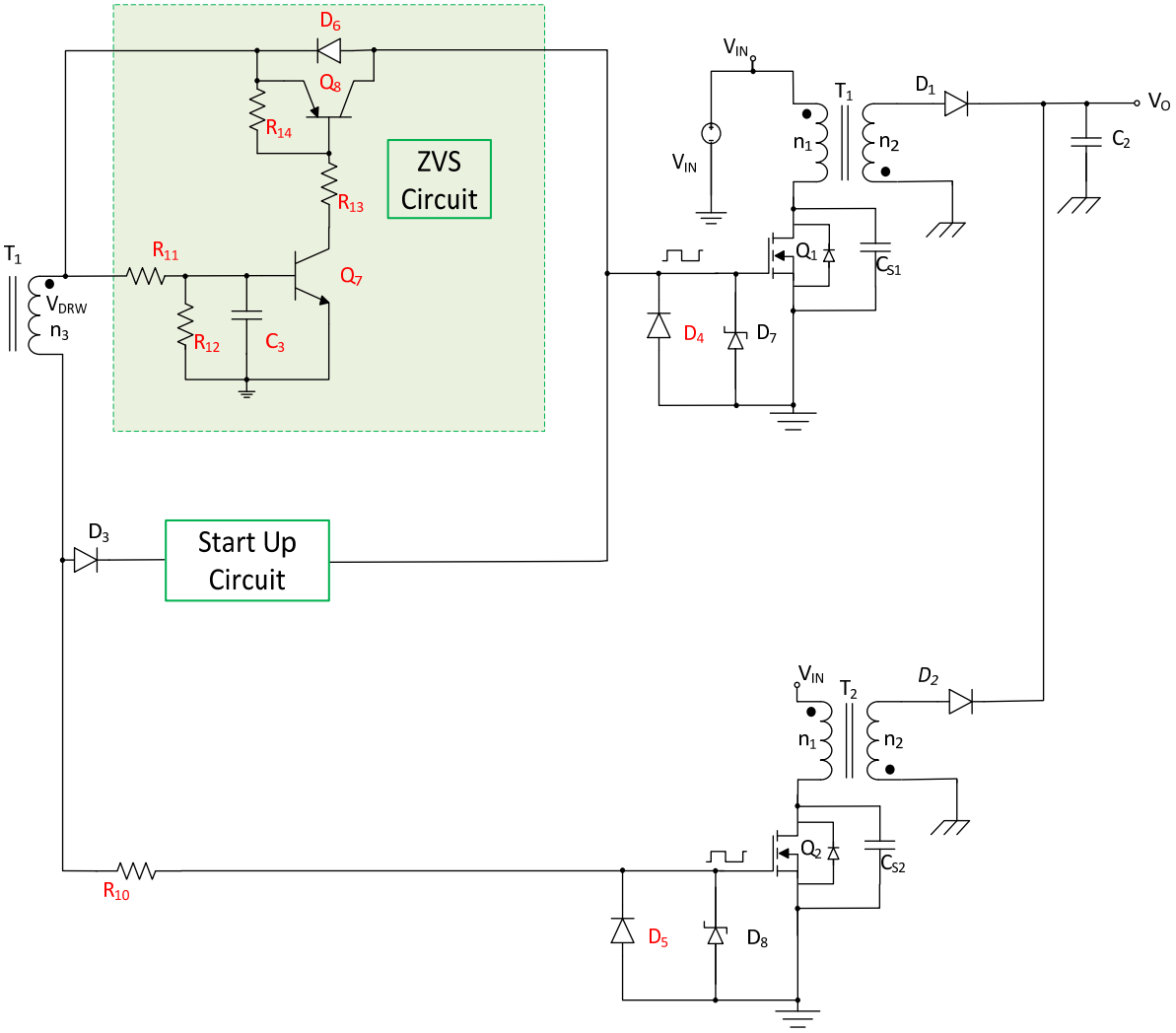


Figure 5.3: Novel turn ON circuit.

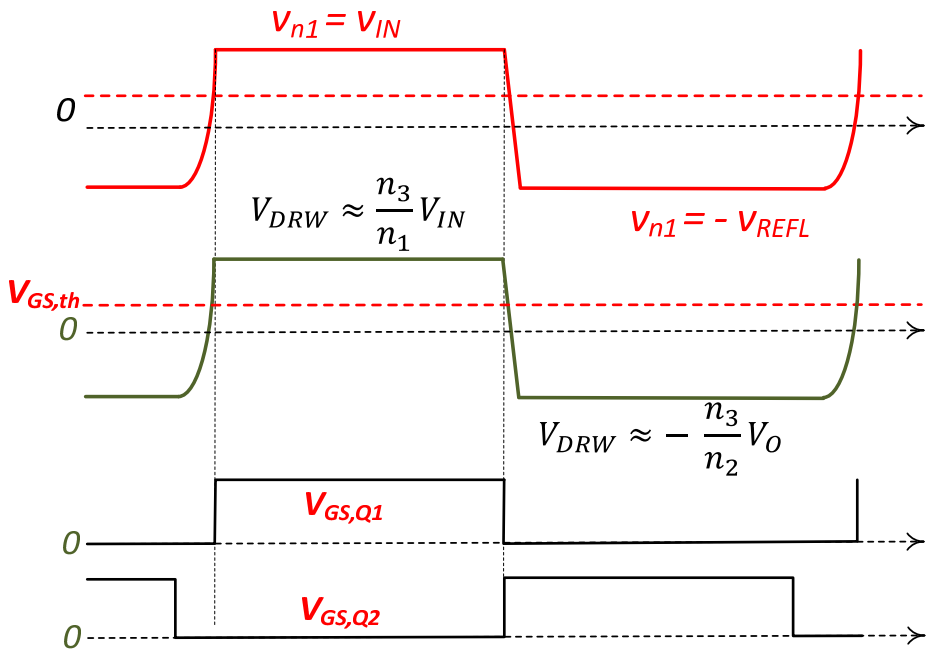


Figure 5.4: Novel turn ON circuit waveforms.

5-4 Main Switching Devices Novel Turn OFF Circuits

Fig. 5.5 illustrates an innovative turn OFF circuit for the main switching devices, Q_1 and Q_2, implemented in the proposed Novel Low Cost PV Converter Based on Analog Interleaving Method. No clock or PWM or driver module chips are used; the circuit uses low count of very low cost discrete components instead.

The turn OFF circuit functions as follows:

1. Once the T_{OFF1} signal is high, npn bipolar transistor Q_9 turns ON.
2. Once Q_9 is ON, the base of pnp bipolar transistor Q_{10} is pulled down, starting its turn ON.

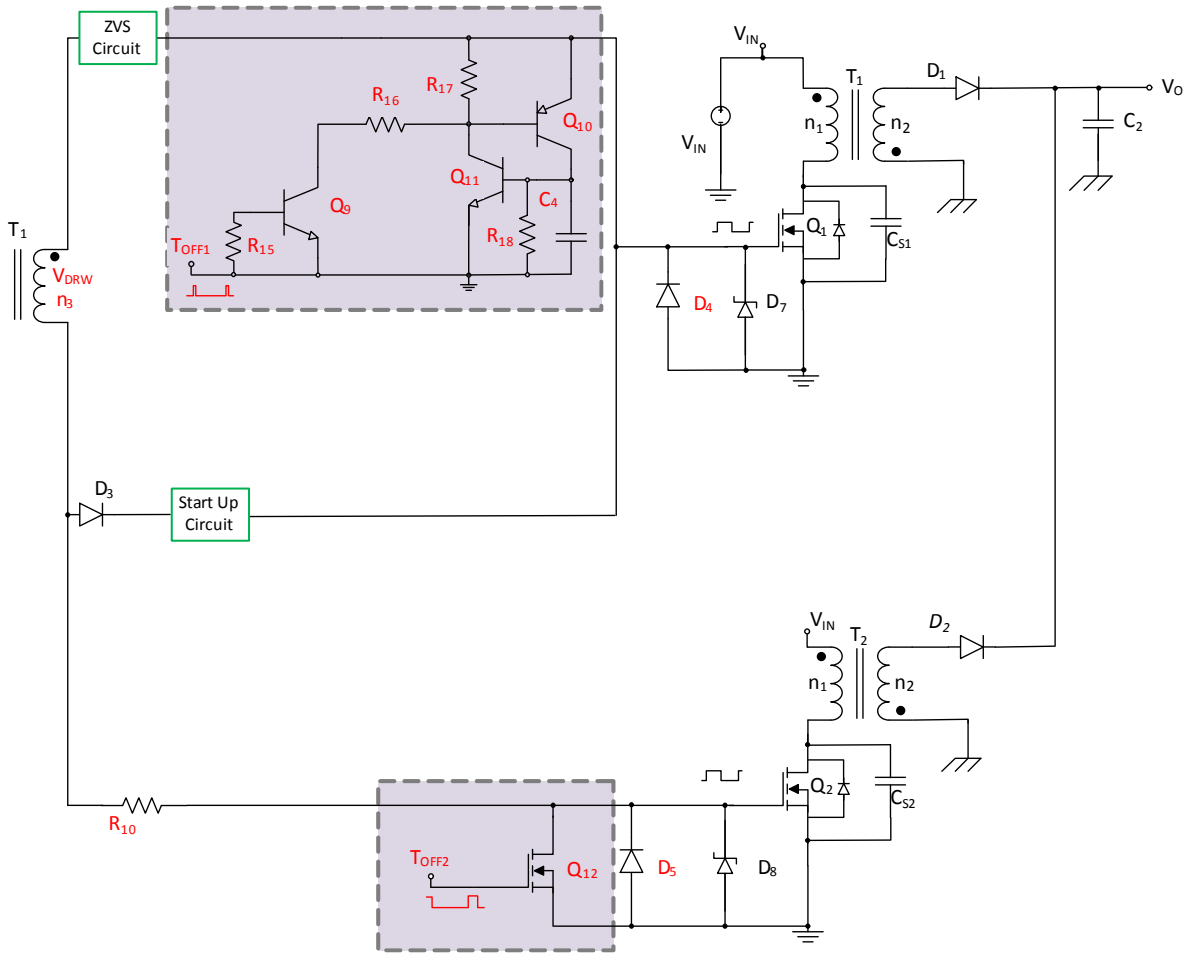


Figure 5.5: Novel turn OFF circuit.

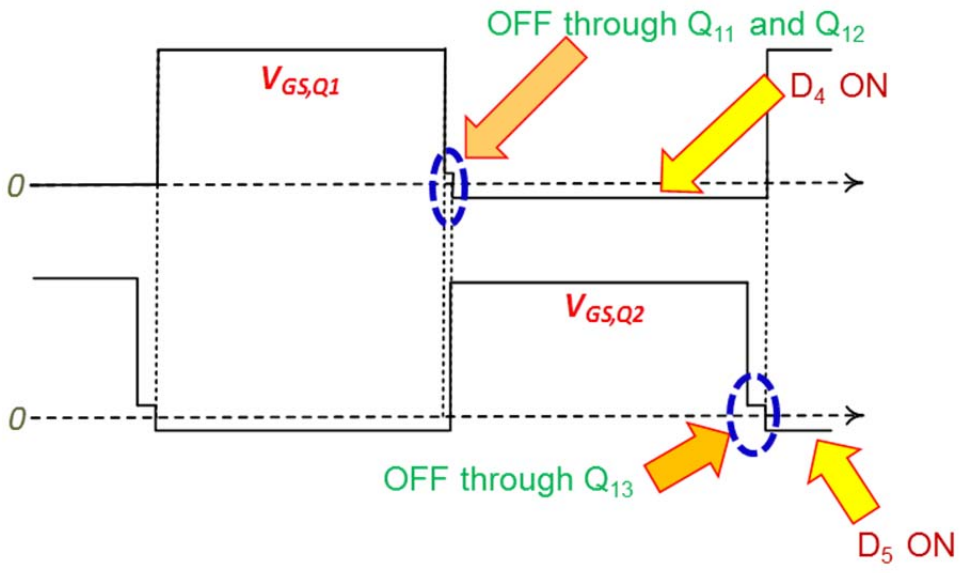


Figure 5.6: Novel turn OFF circuit waveforms.

3. npn bipolar transistor Q_{11} turns ON as a result of Q_{10} turning ON. This will further pull down the base of Q_{10} to $V_{CE,SAT}$ of Q_{11}. This positive feedback established by Q_{10} and Q_{11} result into fast and solid Q_1's turn OFF.
4. As illustrated in *Fig. 5.6*, Q_{10} and Q_{11} remain ON until the drive winding reverses its polarity due to the turn OFF of Q_1, which causes a voltage polarity change across the primary winding. This results in the turn ON of D_4, which resets Q_{10} and Q_{11} while pulling the gate voltage of Q_1 further down to the forward voltage drop of D_4.
5. This turns ON Q_2 until T_{OFF2} becomes high, signaling the end of $t_{ON,Q2}$ by turning Q_{12} ON.
6. Q_{12} remains ON, holding Q_2 OFF, until the master flyback's transformer (T_1) drive winding reverse polarity again, at a time when all the energy stored in T_1 is delivered to the load.
7. This result into the turn ON of D_5, which resets Q_{12} while pulling the gate voltage of Q_2 further down to the forward voltage drop of D_5.

5-5 Novel Control Circuit

Fig. 5.7 illustrates an innovative control circuit for the proposed Novel Low Cost PV Converter Based on Analog Interleaving Method. Again, no clock or PWM or driver module chips are used; the circuit uses low count of very low cost discrete components instead.

The control circuit functions as follows:

1. During the ON time of Q_1, the bias voltage (V_{bias}) charges capacitor C_{Ramp1} through resistor R_{19}. Once the voltage across C_{Ramp1} reaches the reference voltage V_{REF}, the output of comparator M_{1a} goes high to cause Q_9 to turn ON, which terminates the ON

time of Q_1 and initiates its OFF time. Once the drive winding reverses its polarity, as described in section 5-4 of this chapter, V_{RESET1}, which connects via a diode (not shown in *Fig. 5.7*) goes down and remains in the down stage throughout the OFF time of Q_1.

2. As soon as the drive winding reverses its polarity, just after Q_1's OFF time is initiated, V_{RESET2}, which was held down during the ON time of Q_1, via a diode connected to the drive winding (not shown in *Fig. 5.7*), becomes high.
3. As soon as V_{RESET2} becomes high, V_{bias} start charging C_{Ramp2} via resistor R_{20} during the ON time of Q_2.

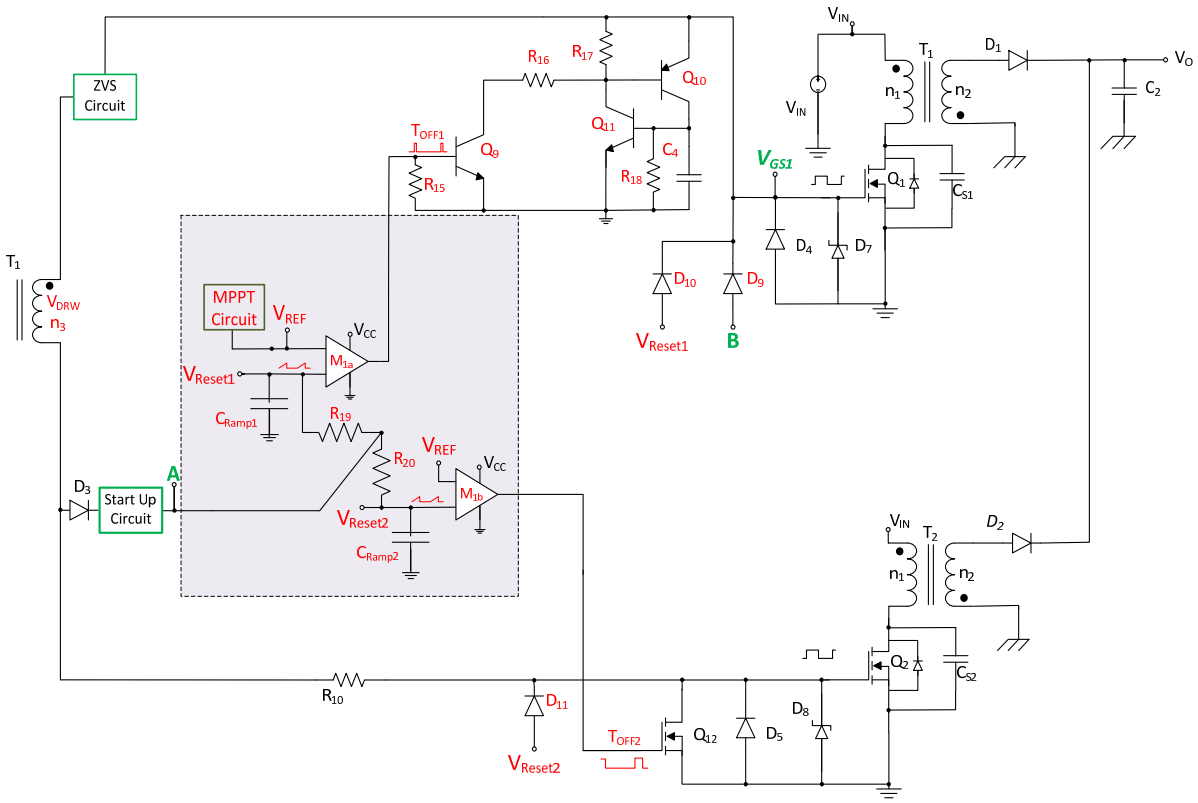


Figure 5.7: Novel control circuit.

4. Once the voltage across C_{Ramp2} reaches the reference voltage V_{REF}, the output of comparator M_{1b} goes high to cause Q_{12} to turn ON, which terminates the ON time of Q_2 and initiates its OFF time. Q_2 stays OFF until its next cycle established by the end of the next ON time of Q_1.

Based on what is described above, Q_1 and Q_2 share the same gate drive established by master transformer's drive winding and this simple and low cost control circuit.

5-6 Short Circuit Protection

Short circuit protection is one of the advantages that the Novel Low Cost PV Converter Based on Analog Interleaving Method features. The startup circuit shown in *Fig. 5.1* requires capacitor C_1 to charge through resistor R_1 to a voltage level sufficient to overcome the threshold voltage of the Zener diode D_4 ($V_{D4,th}$). Hence,

$$V_{C1,start} = V_{D1,th} + V_{Q3,\mathrm{EB,th}} + I_{R3}R_3 \tag{126}$$

The time required reaching $V_{C1,start}$ is:

$$V_{C1,start} = V_{IN}(1 - e^{-t/R_1C_1}) \tag{127}$$

Where R_1 is a high impedance resistor and is designed for a few milli-watts dissipation. Hence, the R_1C_1 time constant could advantageously be selected to be long. On the other hand, capacitor C_1, which charges on a cycle by cycle basis, establishing the bias voltage, is mainly charged from the drive winding (n_3) through diode D_3 during t_{OFF1}. With a proper transformer design, where minimum leakage is attained, in the case of an output short circuit, the drive winding is shorted during t_{OFF1}. After few cycles, this will cause the voltage across C_1 to drop to a level where Q_3 turns OFF. Hence, the gate drive to the main switching devices, Q_1 and Q_2, is no longer available. This would force the converter to stay in the OFF

state until capacitor C_1 charges again to the $V_{C1,start}$ threshold. Hence a hiccup mode is established.

Furthermore, during an output short circuit, Q_{10} and Q_{11} remain in the ON state until the voltage across C_1 is sufficiently low. Since C_1's discharging impedance (approximately R_9) is much lower than that of the charging one (R_1), the duty cycle of the said hiccup mode is very low. Moreover, the hiccup duty cycle could easily be designed to be less than 3% or whatever is required to prevent heating/destroying the output rectifiers and the utilized MOSFETs. Thus, an effective short circuit protection feature is provided by the technique without adding additional circuitry and cost.

5-7 Analog versus Digital Circuits

Unlike digital controllers, the adopted analog control method provides fast response to PV irradiance and load changes. This has been experimentally proven as is demonstrated in chapter 6. On the other hand, typically, digital controllers (or micro-controllers) do require a 4 or more layer printed circuit board (PCB) in order accomplish the required layout. However, the circuits discussed in this chapter are all discrete and can be easily implemented with a single or double sided PCB. This analog approach does offer a great cost advantage over the digital one, especially that the low component count of the proposed analog method allows for the use of a similar size PCB that is required by the digital implementation approach.

One of the considered low cost digital controllers [44], listed in *Table 5.1*, do have a unit cost of $6.21. As illustrated in the controllers' datasheet [45] and shown in *Fig. 5.8*, a noise rejection inductor is needed as well as other additional required components when

applying the controller in the application. Such components include the MOSFET gate drivers, example of which [46] is listed in *Table 5.1* and illustrated in *Fig. 5.9*. Moreover, an auxiliary supply is required to power the microcontroller with a specified operating supply voltage of 3V to 3.6V.

Table 5.1: Cost of using a digital microcontroller. [31]

Supplier P/N	Manufacturer:	Description	Unit Cost
579-DSPIC336GS504EPT	Microchip Technology	Digital Signal Processors & Controllers - DSP, DSC 16B MCU/DSP 40MIPS 16 KB FLASH	$6.21
689-MD1210K6-G	Microchip Technology	Gate Drivers Dual High Speed	$1.62
495-TCK-046	TRACO Power	Inductor (18 uH +/-20%, DCR (max) = 150 mOhm)	$2.27
81-LXDC2SCAAB-352	Murata Electronics	Non-Isolated DC/DC Converters 2.8x2.9 Buck/boost 3.3Vo 2.8-5Vin 1.2A	$3.76
Total required for the use of a digital microcontroller (ignoring the cost of associated capacitors, resistors, and other components)			**$13.86**

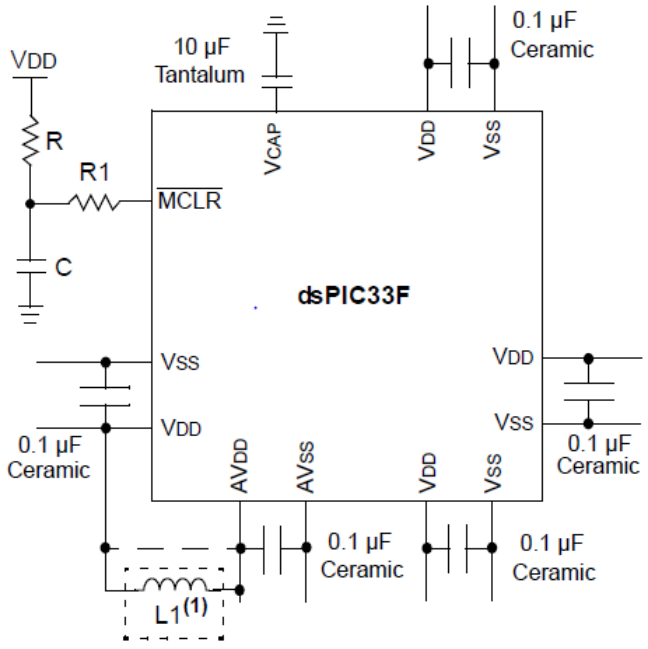


Figure 5.8: Digital microcontroller's manufacturer recommended minimum connection, where L_1 is specified to have an impedance of less than 1Ω. [45]

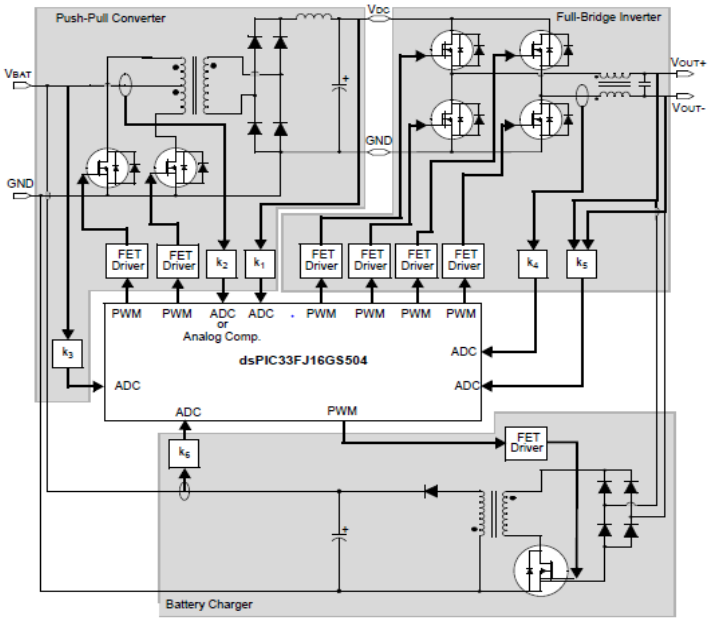


Figure 5.9: Digital microcontroller's manufacturer exemplified application example illustrating the need to add FET driver modules. [45]

In a direct comparison, $1.58 is the total cost of the innovative analog circuitry presented in *Figures 5.1*, *5.3*, *5.5*, and *5.7*, as illustrated in *Table 5.2*. Hence, ignoring the savings gained by enabling the use of a double sided PCB, implementing such innovative circuits would result into a $12.28 cost advantage over the digital microcontroller approach.

Table 5.2: Cost of using the employed innovative analog circuits. [31]

Supplier P/N	Manufacturer:	Description	Qty Used in Circuits	Unit Cost	Total Per Item
863-MMBT2222ALT1G	ON Semiconductor	Bipolar Transistors - BJT SS SOT23 GP XSTR NPN 40V	5	$0.10	$0.50
863-MMBT2907ALT1G	ON Semiconductor	Bipolar Transistors - BJT 600mA 60V PNP	4	$0.10	$0.40
583-BZX84C8V2-T1	Rectron	Zener Diodes 8.2V	1	$0.09	$0.09
583-1N4148-T	Rectron	Diodes - General Purpose, Power, Switching 100V If/300mA	1	$0.03	$0.03
511-LM339DT	STMicroelectronics	Analog Comparators Lo-Pwr Quad Voltage	1	$0.32	$0.32
511-LM2904AYPT	STMicroelectronics	Op Amps Low-PWR Dual 100dB 1.1MHz 20nA Op Amp	1	$0.24	$0.24
Total required for the employed analog approach (ignoring the cost of associated capacitors, resistors)					**$1.58**

5-8 Conclusion

Innovative startup, turn ON, turn OFF, and control analog circuits were presented in this chapter. Each of the said circuits uses very low cost and efficient components, resulting in a very low cost and efficient converter. The said circuits allowed the converter to operate without the need for clock, PWM or driver chips. On the other hand, the discrete components' implementation of the circuits eliminated the need for 4 or more layers printed circuit board (PCB). Hence, as described in the upcoming chapter, a double sided PCB was used for prototyping the converter, which further reduces the cost.

Furthermore, in this chapter, the short circuit protection that is offered by the scheme, without the use of additional components, is described. Moreover, a detailed cost comparison between the adopted analog approach and the use of a digital microcontroller was also discussed. The comparison illustrated the significant cost advantage of using the innovative analog circuitry described in this chapter.

Chapter 6: Experimental Results of the Novel Low Cost PV Converter Based on Analog Interleaving Method

6-1 Overview

The Novel Low Cost PV Converter Based on Analog Interleaving Method was prototyped and tested at various input power conditions. The test setup included a PV emulator as an input, and a constant voltage electronic load as the output. The said prototype was designed according to the specification requirements provided in chapter 3, section 3-3-1. Hence, the converter's input power varied from 250W down to 25W and the converter's output voltage was 250V with an input voltage of 30V. This chapter covers the experimental results of the said prototype.

6-2 250W Prototype

A low cost 2-sided printed circuit board (PCB) illustrated in *Fig. 6.1* and *Fig. 6.2* was designed and prototyped. As presented in *Fig. 6.1*, the said PCB was established using a 3.8" by 5.1" dimensions. Furthermore, for ease of debugging, through hole components were used, as shown in *Fig. 6.3*. The implemented design did not require an auxiliary startup circuit, a pulse width module, driver or a clock chips. Except for an operational amplifier and comparator chips, the prototype used only low cost discrete analog components.

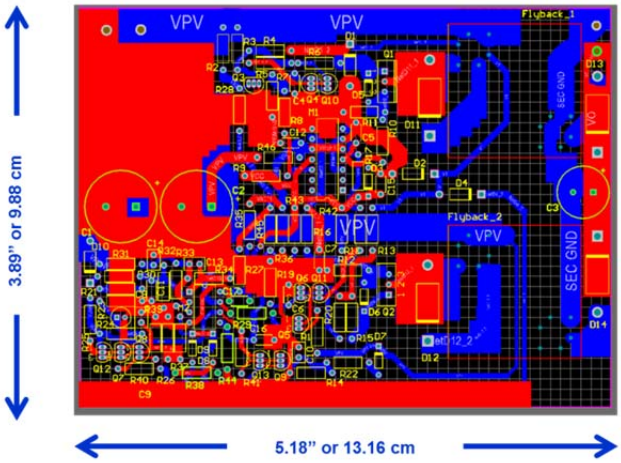


Figure 6.1: Scheme PCB top layer.

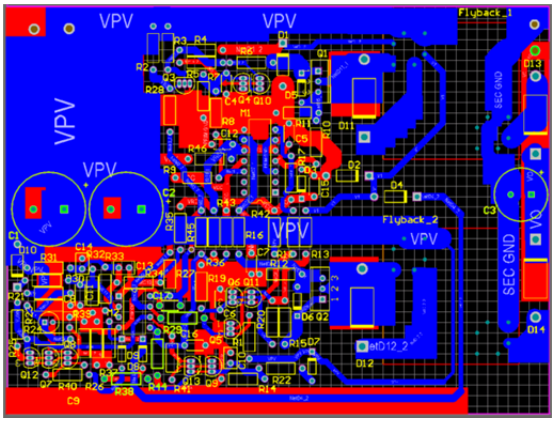


Figure 6.2: Scheme PCB bottom layer.

Figure 6.3: Scheme 250W prototype.

6-3 250W Prototype Bill of Material

The component bill of material (BOM) for this low cost converter, shown in *Fig. 6.3*, is illustrated in *Table 6.1* and *Table 6.2*. *Table 6.1* presents a cost summary where the prototype components are categorized while *Table 6.2* displays the detailed cost where all components are listed.

It is worth noting that the prototype BOM cost at medium quantities is $14.13. The converter's BOM cost is $0.0565/W at only medium quantities, using the prices available from a distributer [31]. However, typically, the industries purchase the components directly from the source at high quantities. Therefore, much lower manufacturing BOM cost is expected.

Table 6.1: Prototype BOM cost summary.

Item	Cost Based on QTY of 1	Cost Based on Average QTY of 10K
Capacitors	$9.03	$2.94
Resistors	$5.08	$1.08
Transistors	$6.45	$2.40
Diodes	$4.21	$1.33
Magnetics	$10.00	$6.00
ICs	$1.31	$0.38
Total	**$36.08**	**$14.13**

Table 6.2: Prototype BOM.

Item	Item QTY	Type	Family	Value	Supplier	Supplier P/N	Manufacturer	Manuf. P/N	Unit Cost ($)		Cost per Medium QTY		
									Per Unit	Per BOM	QTY	$	$
C1	1	Capacitor	Aluminum Electrolytic	2700uF	Digikey	493-1630-ND	Nichicon	UHE1H272MHD	2.350	2.350	25K	0.855	0.855
C2, C3, C4, C18	4	Capacitor	Film Capacitors	4.7uF	Mouser	667-ECW-FD2W475J	Panasonic	ECW-FD2W475J	1.340	5.360	25K	0.439	1.756
C5, C9, C13, C15, C17	5	Capacitor	MLCC	0.1uF	Mouser	594-K104K15X7RF5TH5	VISHAY	K104K15X7RF5TH5	0.100	0.500	20K	0.030	0.150
C6, C7, C10, C12, C14, C16	6	Capacitor	MLCC	1000pF	Mouser	594-K102K15X7RH53L2	VISHAY	K102K15X7RH53L2	0.100	0.600	30K	0.022	0.132
C11	1	Capacitor	MLCC	470pF	Mouser	594-K471K15X7RF53H5	VISHAY	K471K15X7RF53H5	0.050	0.050	50K	0.022	0.022
C8	1	Capacitor	Aluminum Electrolytic	47uF	Mouser	ESH476M025AC3AA	Kemet	ESH476M025AC3AA	0.170	0.170	5K	0.029	0.029
Cumulative Total			**Low Qty:**	**$9.030**		**Med. Qty:**	**$2.944**	Caps Total:	$9.030			$2.944	
R1	1	Resistor	Carbon Film	24K	Digikey	CF18JT24K0CT-ND	Stackpole Electronics Inc	CF18JT24K0	0.090	0.090	2500	0.008	0.008
R2	3	Resistor	Carbon Film	24K	Digikey	CF18JT24K0CT-ND	Stackpole Electronics Inc	CF18JT24K0	0.090	0.270	2500	0.008	0.025
R3	1	Resistor	Carbon Film	20K	Digikey	CF18JT20K0CT-ND	Stackpole Electronics Inc	CF18JT20K0	0.090	0.090	2500	0.008	0.008
R4, R42	2	Resistor	Carbon Film	1K	Digikey	1.0KH-ND	Yageo	CFR-50JB-52-1K	0.100	0.200	5000	0.011	0.022
R5,R7, R8,R14, R18,R19, R20,R25, R26,R39, R40,R41	12	Resistor	Carbon Film	1.1K	Digikey	CF18JT1K10CT-ND	Stackpole Electronics Inc	CF18JT1K10	0.090	1.080	2500	0.008	0.100
R6, R15	2	Resistor	Carbon Film	10	Digikey	CF14JT10R0CT-ND	Stackpole Electronics Inc	CF14JT10R0	0.080	0.160	2500	0.007	0.014
R9, R17, R24	3	Resistor	Carbon Film	3K	Digikey	CF18JT3K00CT-ND	Stackpole Electronics Inc	CF18JT3K00	0.090	0.270	2500	0.008	0.025
R10, R16, R22, R28, R29, R34, R38	7	Resistor	Carbon Film	100	Digikey	CF18JT100RCT-ND	Stackpole Electronics Inc	CF18JT100R	0.090	0.630	2500	0.008	0.059
R11, R12	2	Resistor	Metal Element CS	0.005	Mouser	588-620HR005E	Ohmite	620HR005E	0.520	1.040	2500	0.350	0.700
R13	1	Resistor	Carbon Film	820	Digikey	CF14JT820RCT-ND	Stackpole Electronics Inc	CF14JT820R	0.080	0.080	2500	0.007	0.007
R21	1	Resistor	Carbon Film	33K	Digikey	CF18JT33K0CT-ND	Stackpole Electronics Inc	CF18JT33K0	0.090	0.090	2500	0.008	0.008
R23, R27, R32, R33, R37, R43	6	Resistor	Carbon Film	10K	Digikey	CF18JT10K0CT-ND	Stackpole Electronics Inc	CF18JT10K0	0.090	0.540	2500	0.008	0.050
R30, R31, R45, R46	4	Resistor	Carbon Film	5.1K	Digikey	CF18JT51K0CT-ND	Stackpole Electronics Inc	CF18JT51K0	0.090	0.360	2500	0.008	0.033
R36	1	Resistor	Carbon Film	120	Digikey	CF18JT120RCT-ND	Stackpole Electronics Inc	CF18JT120R	0.090	0.090	2500	0.008	0.008
R44	1	Resistor	Carbon Film	5.1K	Digikey	CF18JT5K10CT-ND	Stackpole Electronics Inc	CF18JT5K10	0.090	0.090	2500	0.008	0.008
Cumulative Total			**Low Qty:**	**$14.110**		**Med. Qty:**	**$4.021**	Resistors Total	$5.080			$1.077	
Q1, Q2	2	MOSFET		100V	Mouser	757-TK72E12N1S1X	Toshiba	TK65E10N1,S1X	2.650	5.300	10000	1.070	2.140
Q3, Q4, Q5, Q6, Q7, Q8, Q9	7	NPN		40V	Mouser	512-KSP2222ATF	Fairchild Semiconductor	KSP2222ATF	0.070	0.490	10000	0.018	0.126
Q10, Q11, Q13	4	PNP		60V	Mouser	512-KSP2907ATA	Fairchild Semiconductor	KSP2907ATA	0.060	0.240	2000	0.018	0.072
Q12	1			60V	Mouser	512-BS170D27Z	Fairchild Semiconductor	BS170_D27Z	0.420	0.420	2000	0.060	0.060
Cumulative Total			**Low Qty:**	**$20.560**		**Med. Qty:**	**$6.419**	Transistor Total	$6.450			$2.398	
D1, D2, D4	3	Diode		50V	Mouser	821-HER101	Taiwan Semiconductor	HER101	0.180	0.540	10000	0.037	0.111
D3	1	Zener		15V	Digikey	568-5889-1-ND	NXP Semiconductors	NZX15X,133	0.210	0.210	5000	0.032	0.032
D5, D6	2	Zener		17V	Mouser	512-1N5247BTR	Fairchild Semiconductor	1N5247BTR	0.040	0.080	2500	0.010	0.020
D7	1	Zener		43V	Mouser	512-1N5260B_T50A	Fairchild Semiconductor	1N5260B_T50A	0.120	0.120	10000	0.017	0.017
D8	1	Zener							0.120	0.120	10000	0.017	0.017
D9	1	Zener							0.120	0.120	10000	0.017	0.017
D10	1	Diode		50V		512-1N4001	Fairchild Semiconductor	1N4001	0.080	0.080	10000	0.014	0.014
D11, D12	2	Diode		150V	Mouser	625-EGP50C-E3/73	Vishay Semiconductors	EGP50C-E3/73	0.830	1.660	2000	0.377	0.754
D13, D14	2	Diode		400V	Mouser	512-EGP30G	Fairchild Semiconductor	EGP30G	0.640	1.280	10000	0.174	0.348
Cumulative Total			**Low Qty:**	**$24.770**		**Med. Qty:**	**$7.749**	Diode Total	$4.210			$1.330	
T1	1	XFMR			Custom				5.000	5.000		3.000	3.000
T2	1	XFMR			Custom				5.000	5.000		3.000	3.000
Cumulative Total			**Low Qty:**	**$34.770**		**Med. Qty:**	**$13.749**	XFMR Total	$10.000			$6.000	
M1	2	Dual Comp.		36V	Mouser	512-LM319N	Fairchild Semiconductor	LM319N	0.560	1.120	50000	0.144	0.288
M2	1	Dual Op-Amp		3 to 26V	Mouser	595-LM2904P	Texas Instruments	LM2904P	0.190	0.190	1000	0.093	0.093
Cumulative Total			Low Qty:	$36.080		**Med. Qty:**	**$14.130**	IC Total	$1.310			$0.381	

6-4 Key Waveforms

Using a PV simulator and a 250V (fixed voltage) electronic load output, the figures below illustrate the experimental results of the prototype of the Novel Low Cost PV Converter Based on Analog Interleaving Method. In *Fig. 6.4*, the gate to source voltages of the master MOSFET ($Q_{1,vgs}$) and the slave MOSFET ($Q_{2,vgs}$) are illustrated. The figure shows the gate drive synchronization, where $Q_{2,vgs}$ is only permitted to be in the high stage, approximately 10V, once $Q_{1,vgs}$ goes down to approximately 0V. Since the duty cycles of the mater and slave flybacks are shown to be less than 50%, the figure illustrates a period of time where both $Q_{1,vgs}$ and $Q_{2,vgs}$ are in the down stage, indicating that both flybacks are OFF.

Furthermore, the time where the state when both flybacks are OFF could be reduced to approximately zero, if desired. The design could be done to have both flybacks run at about 50%, which would reduce the primary peak currents slightly, as described in chapter 3. Moreover, as indicated in chapter 2, if a duty cycle greater than 50% is desired, the slave flyback would need to be driven by a separate driving winding that would need to be added to the slave transformer (T_2). However, not modifying the circuit presented in *Fig. 2.2* would result in limiting the duty cycle for each of the master and slave flybacks, to a maximum of 50%.

On the other hand, *Fig. 6.4* also shows the drain to source voltage waveforms for Q_1 and Q_2. It is worth mentioning that the overshoot voltage (V_{OS}) in each of the MOSFETS is shown to be less than 20V. The measured operating frequency is displayed as 35.62 kHz, where the converter was operating at the maximum input power of approximately 250W.

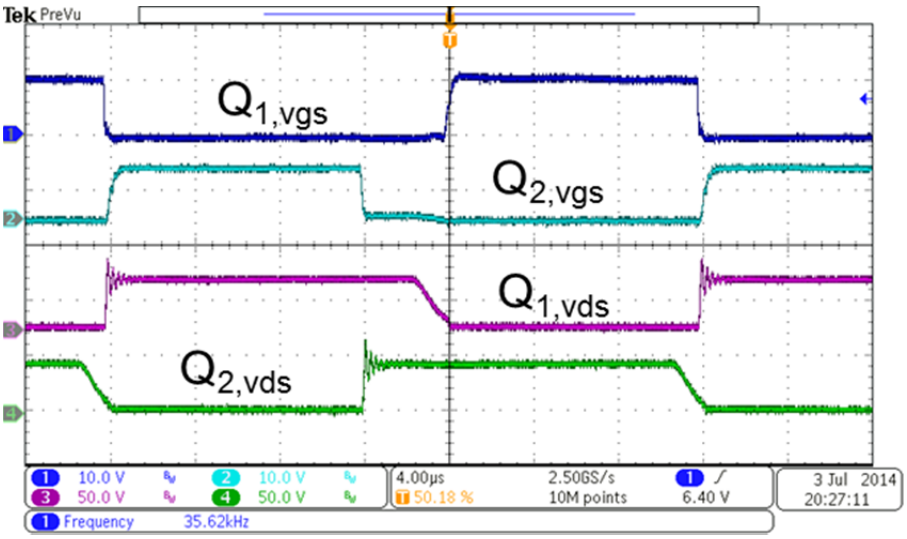


Figure 6.4: Gate to source and drain to source waveforms of the master and slave main switching MOSFETs at full load.

Fig. 6.5 illustrates the current waveforms of the master and slave flybacks. Again, as the figure shows, once $Q_{1,ids}$, representing the master flyback MOSFET's drain to source current, goes down to zero, indicating the end of the master's ON time, the slave flyback's drain to source current of its main switching device ($Q_{2,ids}$) starts to increase. As the figure presents, both $Q_{1,ids}$ and $Q_{2,ids}$ start from zero, which is in line with the theoretical analysis presented in chapter 2. Thus, *Fig. 6.5* verifies that the zero current detection (ZCD) is achieved for both the master and the slave flybacks.

Fig. 6.5 displays the experimental results for the master and slave flybacks' output rectifiers' currents, namely i_{D1} and i_{D2} respectively. As indicated in the theoretical analysis and equations presented in prior chapters of this document, in each of the schemes' interleaved flybacks, the output rectifier start conducting once its associated primary switching device turns OFF. As the said flybacks are operating in the boundary conduction mode, the start of the ON time of Q_1 or Q_2 do not occur until the associated rectifier's current reaches zero.

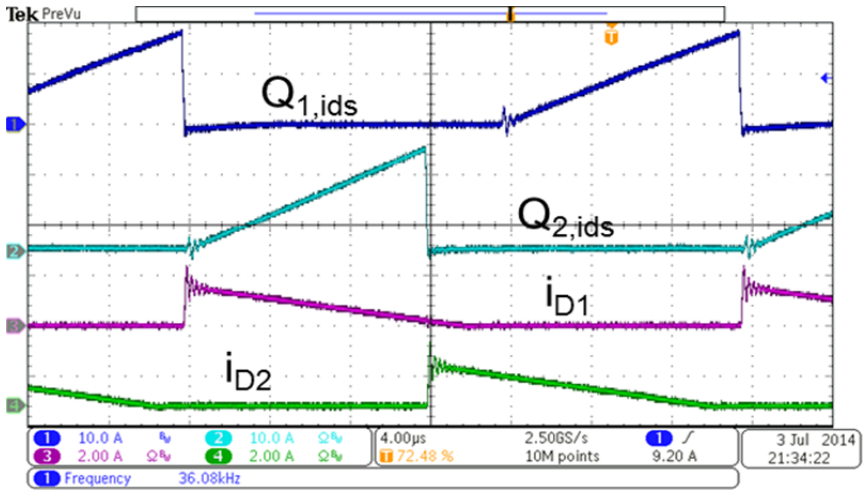


Figure 6.5: Master and slave main switching MOSFETs' drain and output rectifier current waveforms at full load.

Fig. 6.6 shows the master flyback's voltage and current waveforms in one snapshot. As $Q_{1,vgs}$ goes down to approximately 0V, indicating the end of the ON time, $Q_{1,vds}$ increases to its maximum value while $Q_{1,ids}$ decreases to 0A. In the meantime, due to transformer action (T_1), i_{D1} goes up to its maximum value. Furthermore, once $Q_{1,vgs}$ goes up, indicating the start of the ON time, $Q_{1,vds}$ decreases to $V_{ds,Q1,ON}$ while $Q_{1,ids}$ start ramping up, as illustrated in the *Fig. 2.3*. *Fig. 6.7* illustrates the same results for the slave flyback.

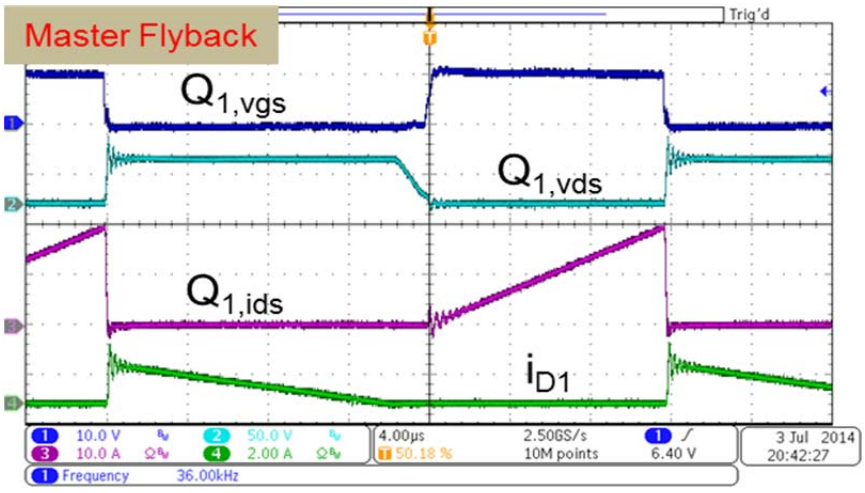


Figure 6.6: Master's output rectifier current; main switching MOSFETs' drain current and gate & drain voltage waveforms at full load.

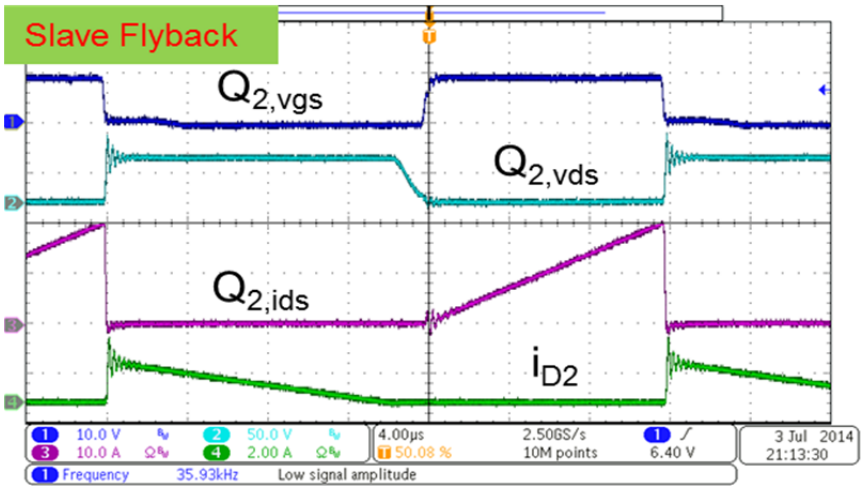


Figure 6.7: Slave's output rectifier current; main switching MOSFETs' drain current and gate & drain voltage waveforms at full load.

In the prototype shown in *Fig. 6.3*, a 100V voltage rated MOSFET was used for Q_1 as well as Q_2. However, 80V voltage rated MOSFET was employed in the updated scheme's prototype version, which is illustrated in *Fig. 6.8*. The said prototype was designed using a low cost 2-sided printed circuit board (PCB), with 2" by 7.7" dimensions. Furthermore, the converter's bill of material (BOM) cost was $13.6 ($0.544/W) at 10K quantities. Moreover, while it could still be optimized, the prototype's California Energy Commission (CEC) weighted efficiency [17] reached 96.42%.

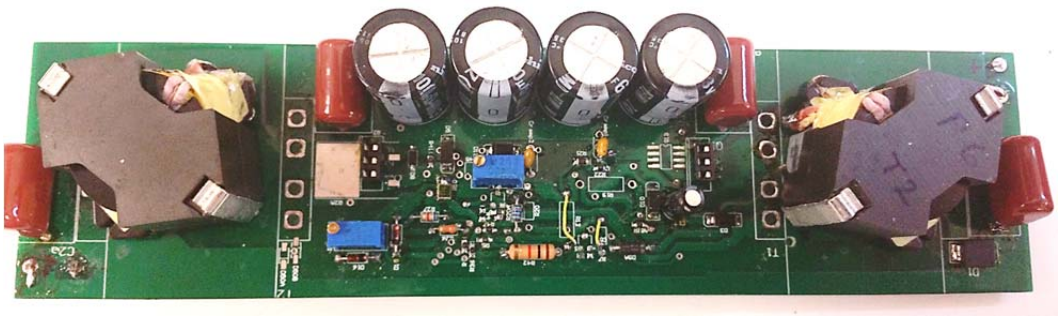


Figure 6.8: Scheme's updated 250W prototype (2" by 7.7").

Figures 6.9 through 6.12 illustrate the voltage and current switching waveforms at full load, which agrees with the theoretical calculations based on the equations presented in prior chapters. It is worth noting that the peak drain to source voltage of Q_1 and Q_2 is each shown to be less than 70V at full load, which would allow the use of 80V devices. This presents significant advantages in cost and efficiency due to lowering of the MOSFET's ON resistance ($r_{ds,ON}$) and gate charge requirements. Furthermore, *Fig. 6.11* and *12* illustrate the ZVS performance of the converter at the master and slave flyback's turn ON.

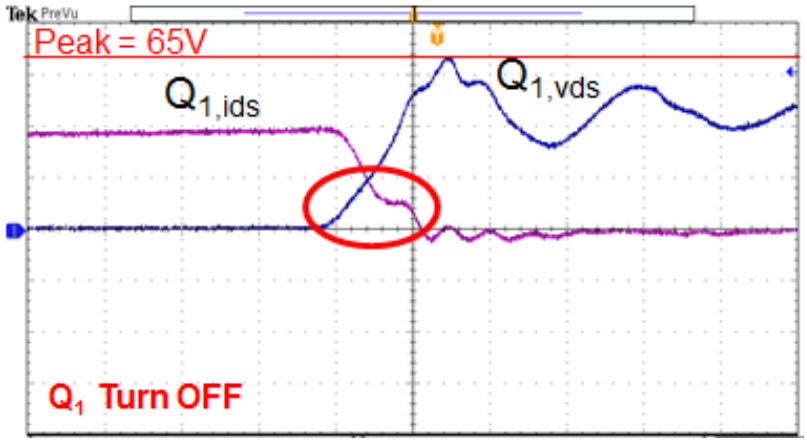


Figure 6.9: The peak drain to source voltage of the master flyback's MOSFET is shown to be 65V at full load. The turn OFF drain to source current ($Q_{1,ids}$) and voltage ($Q_{1,vds}$) crossover is measured at 100*ns* per division.

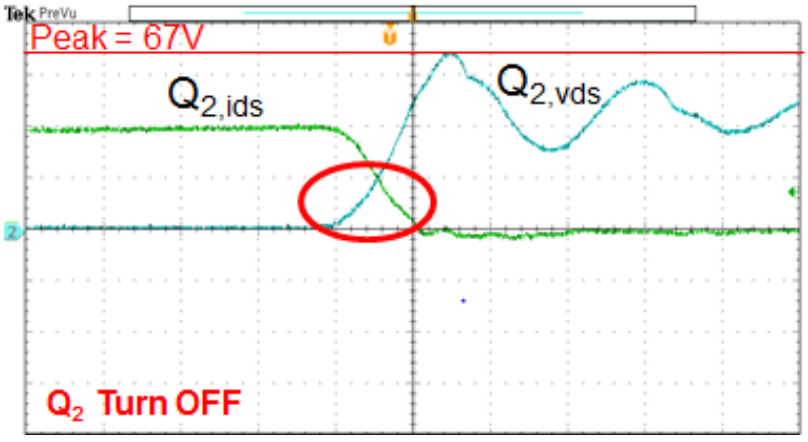


Figure 6.10: The peak drain to source voltage of the slave flyback's MOSFET is shown to be 67V at full load. The turn OFF drain to source current ($Q_{2,ids}$) and voltage ($Q_{2,vds}$) crossover is measured at 100*ns* per division.

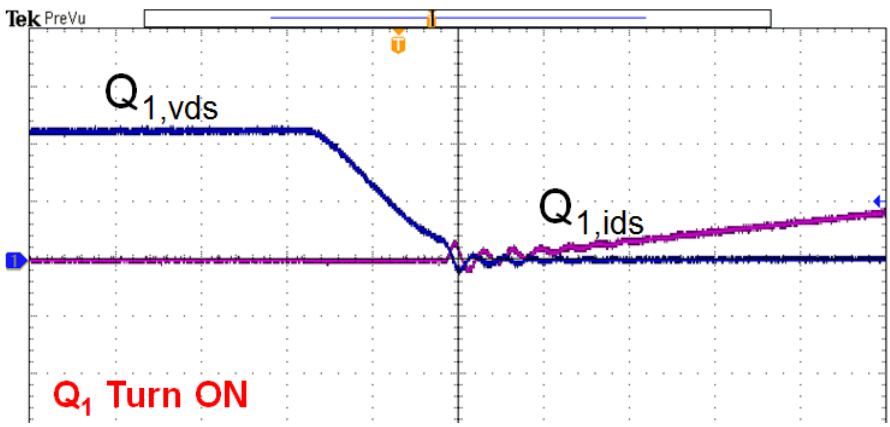


Figure 6.11: Drain to source current ($Q_{1,ids}$) and voltage ($Q_{1,vds}$) crossover is measured at 1µs per division. The figure illustrates the ZVS turn ON at full load.

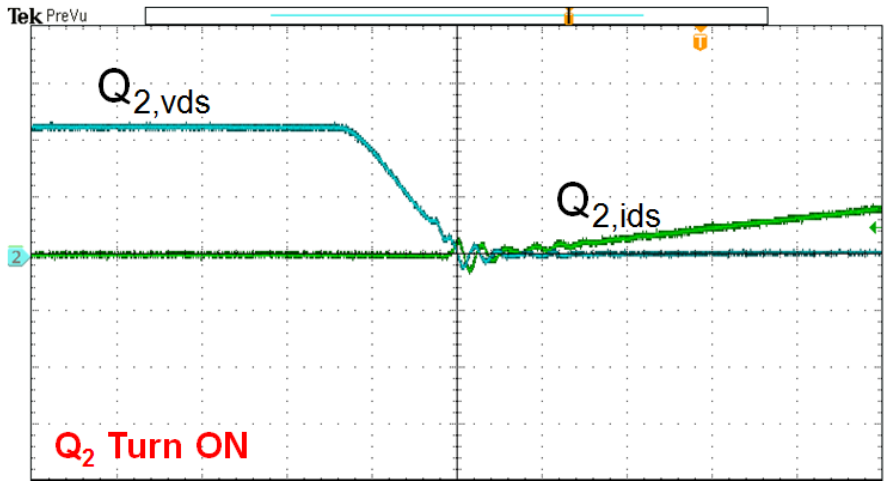


Figure 6.12: Drain to source current ($Q_{2,ids}$) and voltage ($Q_{2,vds}$) crossover is measured at 1µs per division. The figure illustrates the ZVS turn ON at full load.

Unlike digital controllers, the adopted analog control method provides fast response to PV irradiance and load changes. *Fig. 6.13* illustrates the converter's fast response by measuring the input and output currents simultaneously as the PV irradiance increases. Furthermore, *Fig. 6.14* shows the output response with a decrease of the PV irradiance.

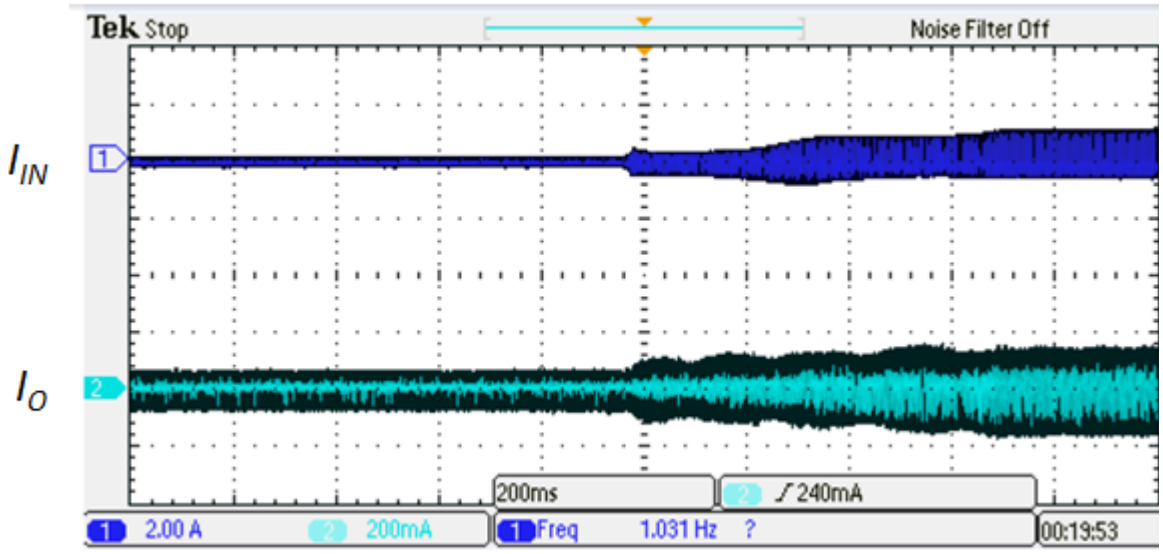


Figure 6.13: Adopted analog control method response to PV irradiance increase. The input current change is almost immediately followed by that of the output.

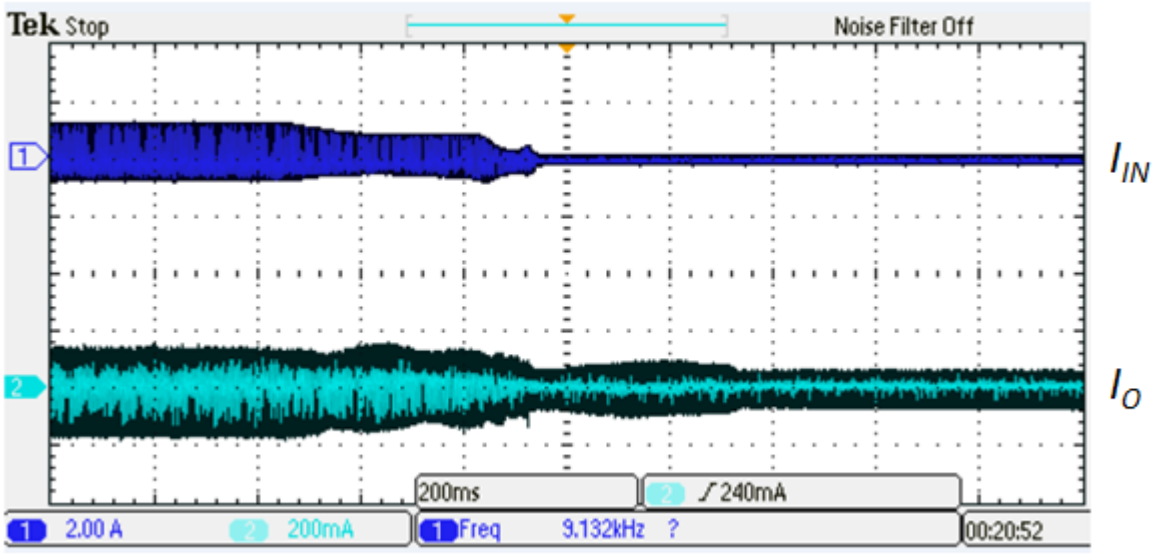


Figure 6.14: Adopted analog control method response to PV irradiance decrease. The input current change is almost immediately followed by that of the output.

6-5 Efficiency

The prototype shown in *Fig. 6.3* performed with a maximum efficiency that was measured, as shown in *Fig. 6.15*, to be 96.67% while the California Energy Commission (CEC) weighted efficiency was calculated to be 96.31%.

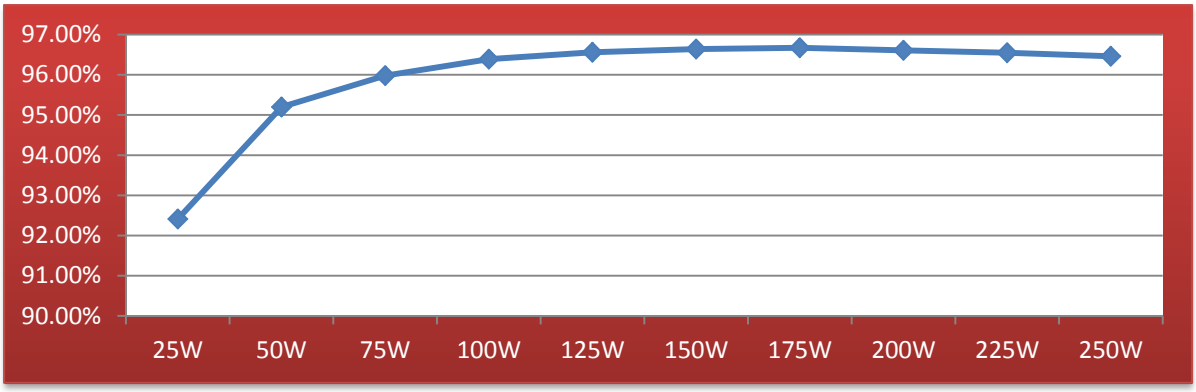


Figure 6.15: Efficiency performance of prototype presented in Fig. 6.3.

However, the updated prototype, illustrated in *Fig. 6.8*, has shown a slight efficiency improvement (CEC = 96.42%), where the related results are shown in *Fig. 6.16*.

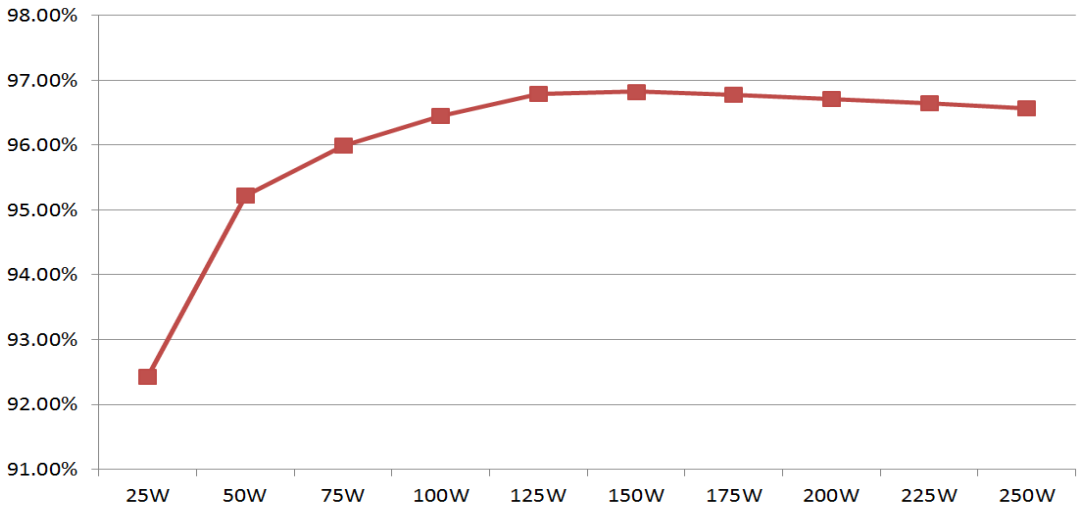


Figure 6.16: Efficiency performance of the updated prototype presented in Fig. 6.8.

6-6 Conclusion

The Novel Low Cost PV Converter Based on Analog Interleaving Method was prototyped and tested. This chapter presented some of the results that included voltage and current waveforms of the main switching devices of the converter. All the novel circuitries, discussed in chapter 5, were tested and were proven to perform satisfactorily. It was experimentally proven that 80V and 100V voltage rated MOSFETs can be used by adopting the design model presented in chapter 3.

All of the newly derived, mostly presented in chapter 2 and 3, were experimentally verified. An updated prototype version was also tested. When compared to the earlier scheme's version prototype, the CEC efficiency was slightly improved from 96.31% to 96.42%. The BOM cost was an impressive $0.056/W and $/0.0544 for the first pass and the updated prototypes, respectively. The updated prototype achieved a 23.57% size reduction over the first pass (20.15 sq.in down to 15.4 sq.in).

Chapter 7: Innovative Plug and Play Residential PV System Design and Implementation

7-1 Overview

Current implementations of the residential PV solar system are costly and do require multiple iterations in order to achieve installation completion. Such iterations include making multiple measurements and adjustments while on the roof, utilizing too many connectors, requiring a licensed electrician to wire the system to the house's electrical panel, involving installers with special skills and in most cases involve locating the dwellings' roof rafters, which is time consuming and do require specials tools. In this chapter, a novel low cost installation method is demonstrated, which offers a system integration technique resulting in reducing the number of electrical connectors used and eliminating the installation adjustments and iterations, resulting in a significant reduction of the installation time. Furthermore, the proposed procedure is in line with the plug and play (PnP) objectives.

7-2 Proposed Innovative Mechanical Integration of Residential Roof Mount Racking System Digest

One example of the state of the art PV solar roof mount racking system, offered by IRONRIDGE [35] is shown in *Fig. 7.1*. While such system offers many advantages, including the so-called XR rails that have a unique curved profile that increases structural strength and spanning capability, locating and adjusting the positioning of the said rails requires iterations while working on the roof. On the other hand, the proposed innovative

mechanical integration of roof mount residential racking system is not dependent on a single style commercially available racking products. Hence, the XR rails as well as most other rails offered by other companies, such as UNIRAC [36], are compatible with the proposed system.

In this chapter, a 3kW residential roof mount system, using the UNIRAC racks integrated with flashing material offered by the Zilla Company, is demonstrated. The said Zilla flashing material [37], shown in *Fig. 7.2*, does not require attachment to roof rafter, which eliminates the need to have special tools required for locating the said rafters.

Figure 7.1: Residential roof mount racking PV solar racking system provided by IRONRIDGE. [35]

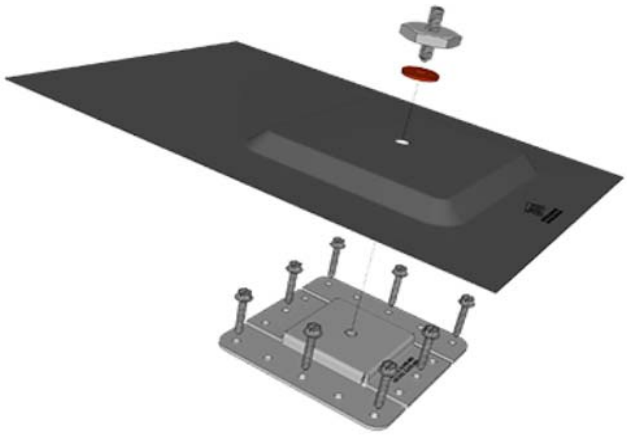


Figure 7.2: The Zilla® Double Stud XL Flashing attaches to sheathing or structural members of the roof, not required to be fastened to the roof rafters. [37]

As an introduction to the upcoming sections in this chapter, the proposed method introduces low cost spacers, exemplified in *Fig. 7.3*, which present the benefits of linking the system ground to various parts of the racking system as well as eliminating measurements and iterations while on the roof. The said spacers are attached to the ends of the rails to form a rectangle per sub-system. Once such rectangle is formed, installing the market available Zilla flashing's bottom plate, which does not require locating the roof rafters for installation, becomes simple. Furthermore, *Fig. 7.3* illustrates the integration of other spacers that serve to hold the integrated power electronics' enclosure and for cable management.

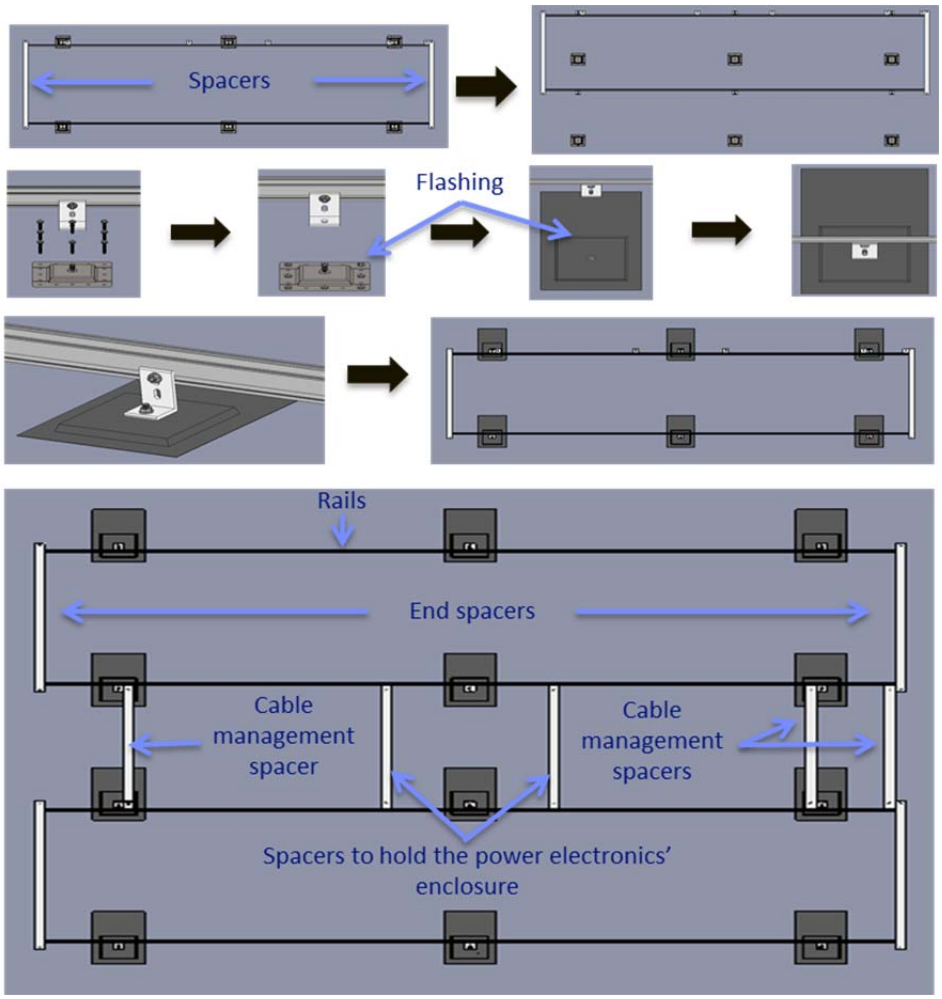


Figure 7.3: Proposed use of spacers to form the racks, cable management, and to integrate the power electronics.

7-3 Proposed Innovative PnP Integration System Configuration

In order to reduce the number of connectors the system uses, and to support faster installation time, *Fig. 7.4* illustrates the proposed methodology that involves modifications and improvements to the PV panel wiring, racking system, and integration of the power electronics. The presented configuration exemplifies a 3kW PV residential system, which is made up af a combination of 1kW and 2kW sub-systems. The proposal is also suitable for larger systems, where combinations of several 2kW and 1kW sub-systems could be integrated. Incorporating each of the power electronics' sub-system in a single mechanical enclosure would reduce the number of connectors needed and eliminate the exposure to high DC voltage, as each produces an AC output voltage.

On the other hand, as shown in *Fig. 7.4*, in lieu of the MC4 connectors used in today's PV panels, this chapter proposes the use of a single 3-pin connector per panel, where two pins are used for the PV power connections and the third pin for grounding the PV panel frame. Not only does the proposed connector lowers the cost and installation time, it also reliably and easily enables grounding the system while in line with the PnP objectives. Experimental results, illustrated in a later section of this chapter, clearly illustrate the cost and PnP advantages of the proposed system. Furthermore, in the system integration exemplified in *Fig. 7.4*, the 2kW power electronics' enclosure is designed to feedthrough the AC output of the 1kW power electronics' enclosure, where parallel connectivity is achieved while facilitating scalability of the proposed configuration.

The "Cable Reeling and Junction Box," shown in *Fig. 7.4*, simply connects to the last enclosure'(s) output in the proposed configuration. The box houses a cable that could be

pulled to the needed length in order to reach and connect to the cable in conduit already tied to the PV Interface (PUI), which is developed by the FREEDM Systems Center at North Carolina State University. The PUI is designed to communicate with the said second stage inverters and the associated utility. Furthermore, the PUI includes the ground fault as well as other protection detection circuits.

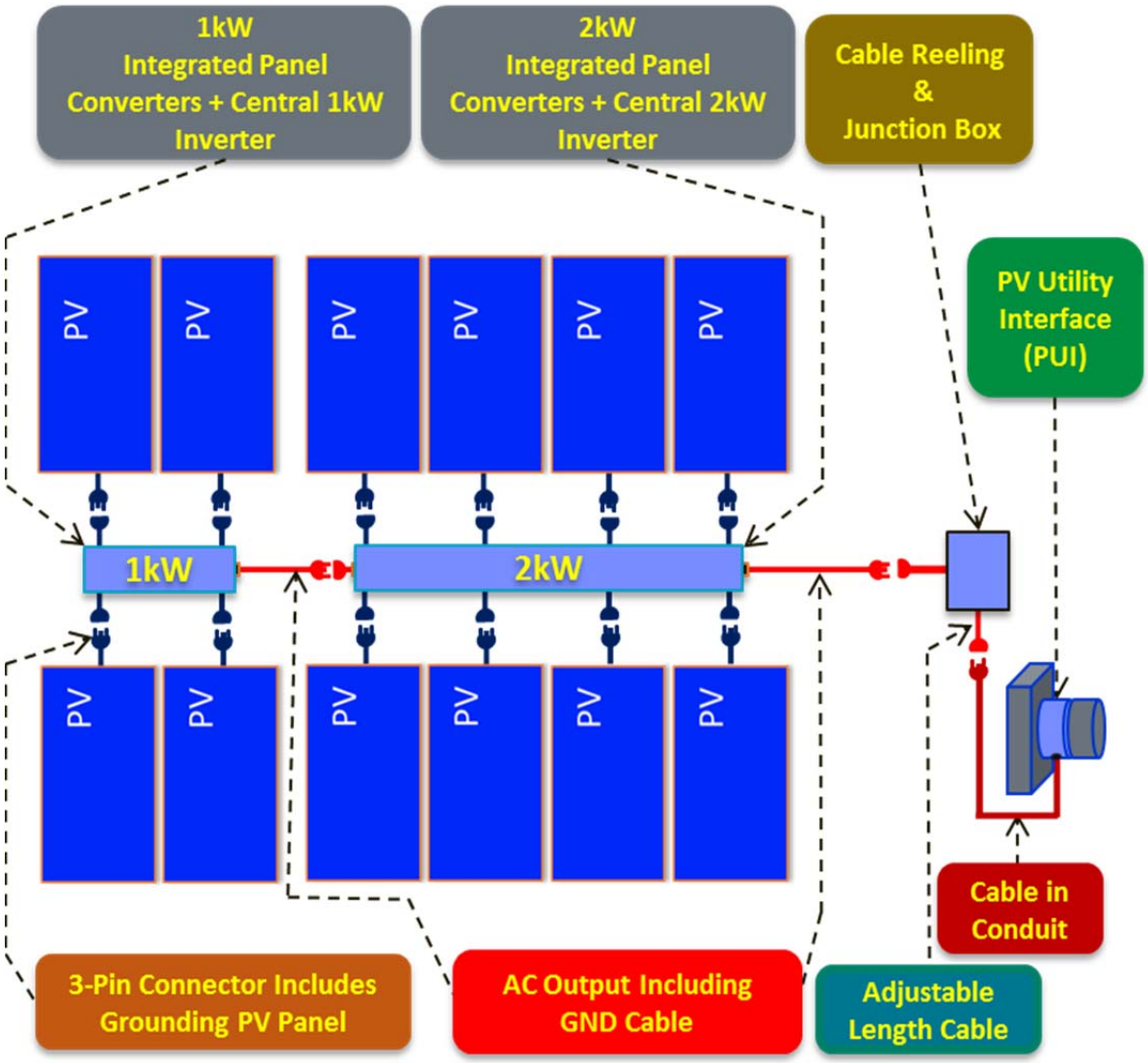


Figure 7.4: Illustration of the proposed PnP system configuration of the integrated DC/DC parallel (suitable for any power electronics' topology architecture).

7-4 Proposed Innovative PnP Integration System Installation Procedure

The installation procedure of the proposed PnP roof mount residential solar PV integrated system is presented in this section. The illustrated system is based on a 3kW system, where it could easily be scaled for higher output system. *Table 7.1* presents the racking related bill of material (BOM) followed by a step by step implementation method required to eliminate the need for installation iterations and for establishing system grounding.

Table 7.1: Bill of material (BOM) of the proposed integrated PnP system.

Components	Quantity
1KW Integrated Power Electronics Enclosure	1
2KW Integrated Power Electronics Enclosure	1
Connector Modified PV Module	12
168''Rail	4
88'' Rail	4
End Clamp	16
Mid Clamp	16
L Foots	50
Cable Reeling & Junction Box	1
End Spacers (1/8")	8
Cable Management Spacers (1/8")	3
Power Electronics Holder Spacers (1/4")	4
Power Utility Interface (PUI)	1

7-4-1 2kW Racking System

Step 1: Insert 5 L foots in the first rail, facing the bottom of the roof (*Fig. 7.5*).

1.1 Tighten the 1st L at the very edge on the left (for the left end spacer).

1.2 Tighten the 2nd L at 16" from the left edge of the rail (for flashing).

1.3 Tighten the 3rd L at approximately the center (83" from either end of the rail) (for flashing).

1.4 Tighten the 4th L at 16" from the right edge of the rail (for flashing).

1.5 Tighten the 5th L at the very edge on the right (for the right end spacer).

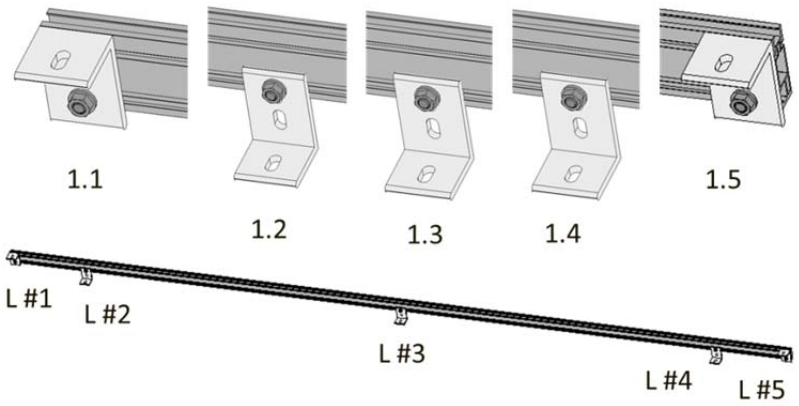


Figure 7.5: Installation procedure step 1.

Step 2: Insert 10 L foots in the second rail, facing the top of the roof (*Fig. 7.6*).

2.1 Tighten the 1st L at the very edge on the left (for the left end spacer).

2.2 Tighten the 2nd L at 16" from the left edge of the rail (for flashing).

2.3 Tighten the 3rd L just to the right of the 2nd L (for cable management).

2.4 Tighten the 4th L at 67" from the left of the rail (for holding the integrated power electronics' enclosure).

2.5 Tighten the 5th L at approximately the center (83” from either end of the rail) (for flashing).

2.6 Tighten the 6th L at 67” from the right of the rail (for holding the integrated power electronics’ enclosure).

2.7 The 8th L to be located 16” from the right edge of the rail (for flashing).

2.8 The 7th L to be located just to the left of the 8th L (for cable management).

2.9 The very right L (10th L) is for the spacer (Type 1) between the first and second rail.

2.10 The 9th L is for the spacer (Type 2) between the second and third rail (for cable management).

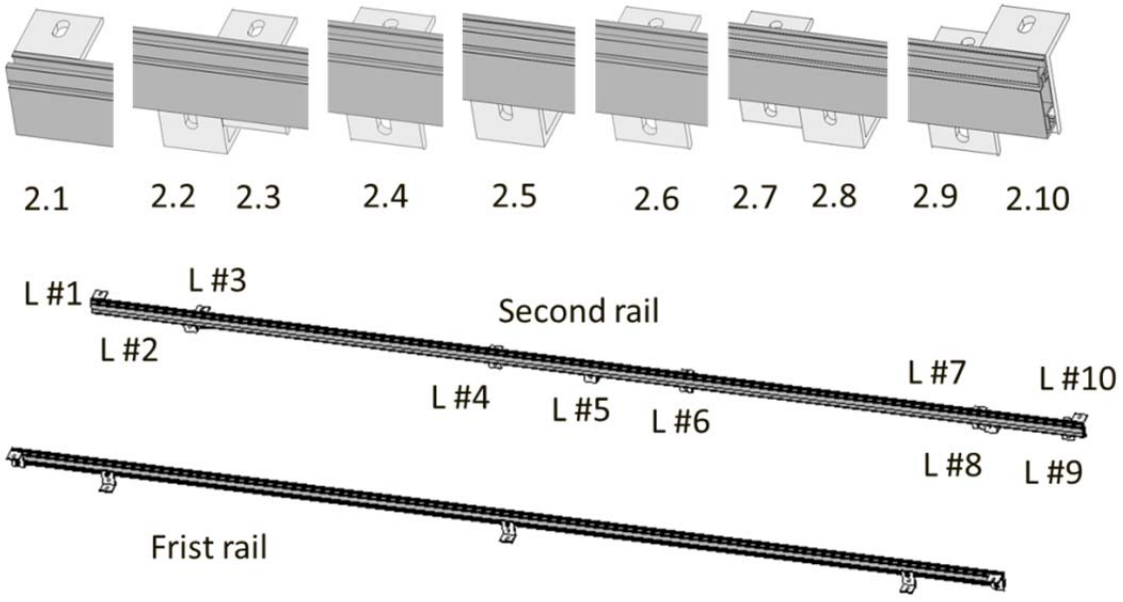


Figure 7.6: Installation procedure step 2.

Step 3: Attach the two end spacers (*Fig. 7.7*).

3.1 Tighten one end spacer on the very left of the first and second rails.

3.2 Tighten one end spacer on the very right of the first and second rails.

3.3 Align the formed rectangle at the desired starting point on the roof.

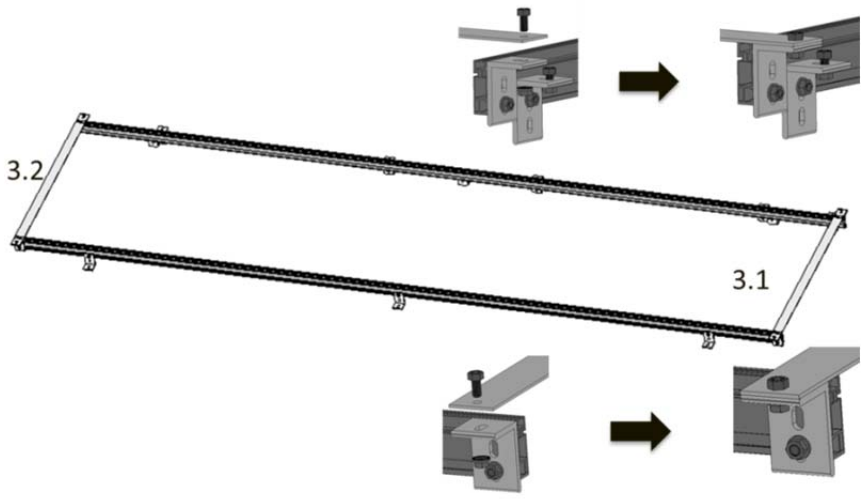


Figure 7.7: Installation procedure step 3.

Step 4: Repeat step 1 and 2 for the 3rd and 4th rails.

Step 5: Install the bottom part of the flashings for the rectangle formed by the first 2 rails (*Fig. 7.8*).

5.1 Install only 2 screws in each flashing.

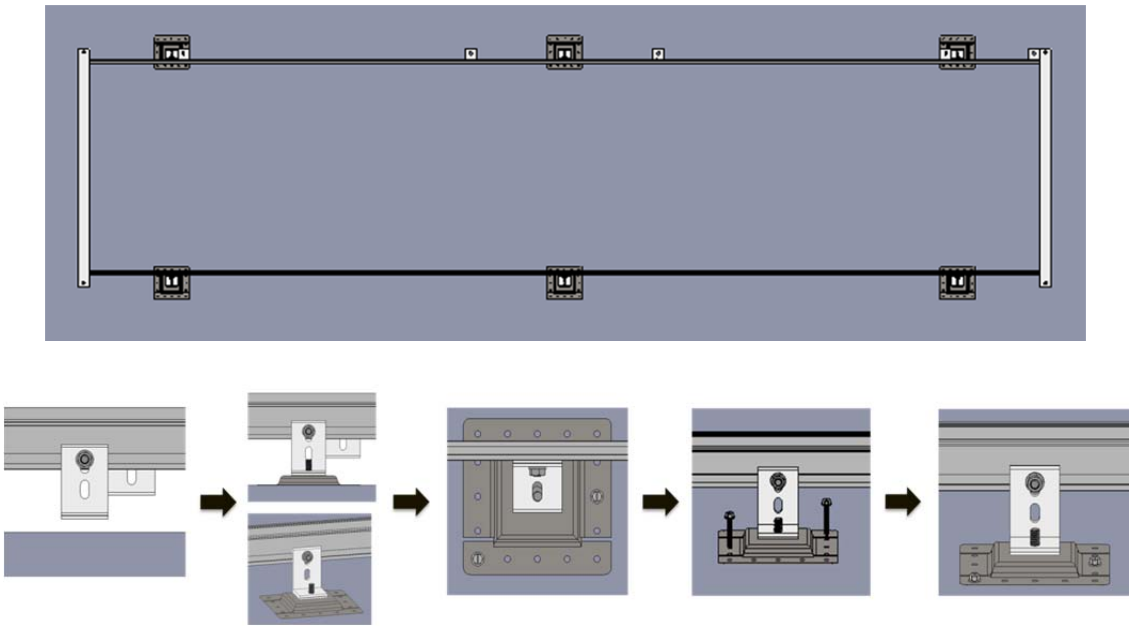


Figure 7.8: Installation procedure step 5.

Step 6: Finish installation of the rectangle formed by the first and second rails (*Fig. 7.9*).

6.1 Move the said rectangle by about 2’ as shown.

6.2 Install all the bottom flashing screws as shown.

6.3 Install the top part of the flashing as shown.

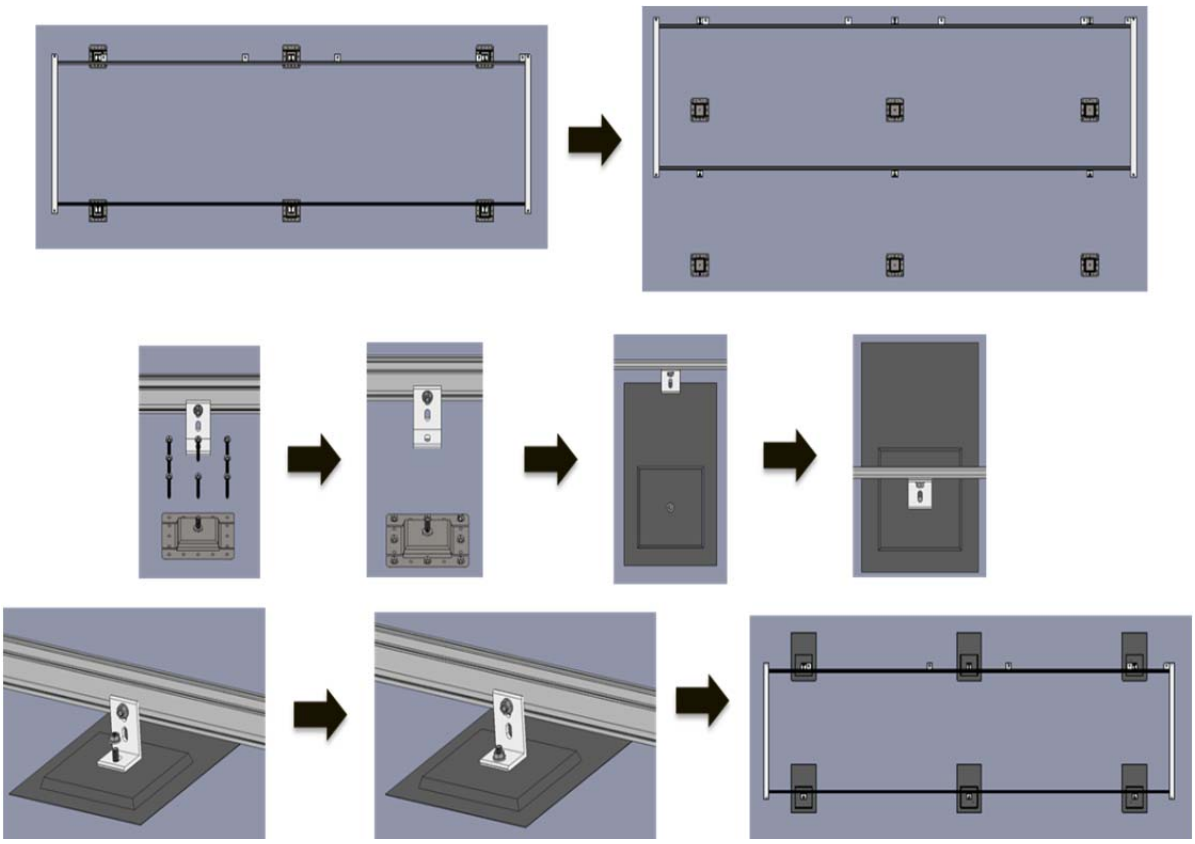


Figure 7.9: Installation procedure step 6.

Step 7: Lineup the rectangle formed by the third and fourth rails to be adjacent to the one formed by the first and second rails (*Fig. 7.10*).

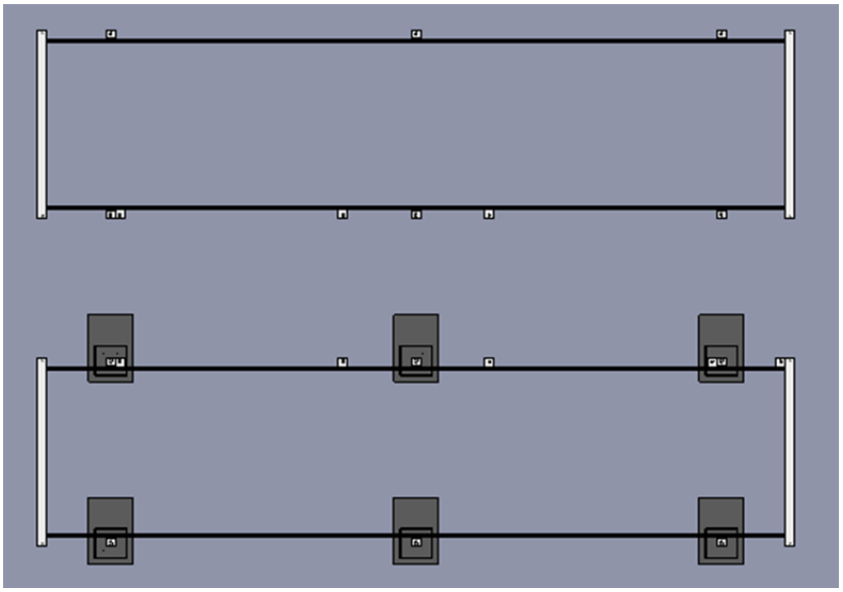


Figure 7.10: Installation procedure step 7.

Step 8: Position the 2 spacers holding the integrated power electronics' enclosure (*Fig. 7.11*) to fit properly (approximately 90 degree angle) between rail 3 and rail 4.

8.1 Do not yet tighten the said spacers but make sure that it is aligned properly prior to performing the following step.

8.2 Tighten the 4th L and 6th L on the third rail.

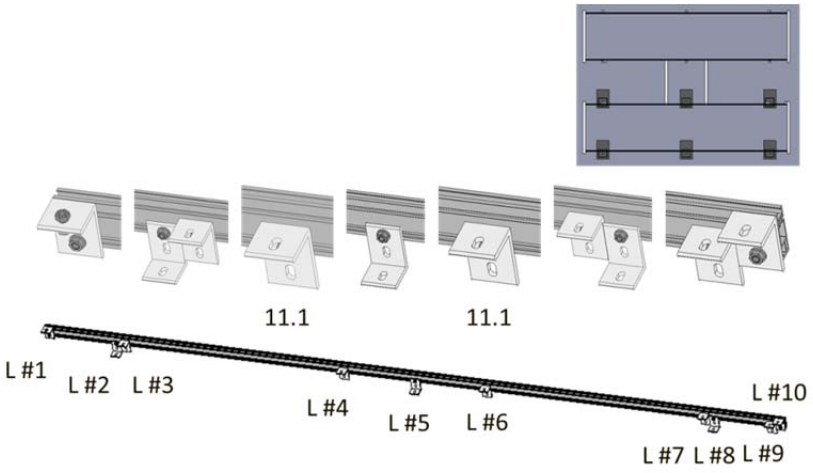


Figure 7.11: Installation procedure step 8.

Step 9: Install the bottom part of the left flashing of the third rail, installing only 2 screws in each (*Fig. 7.12*).

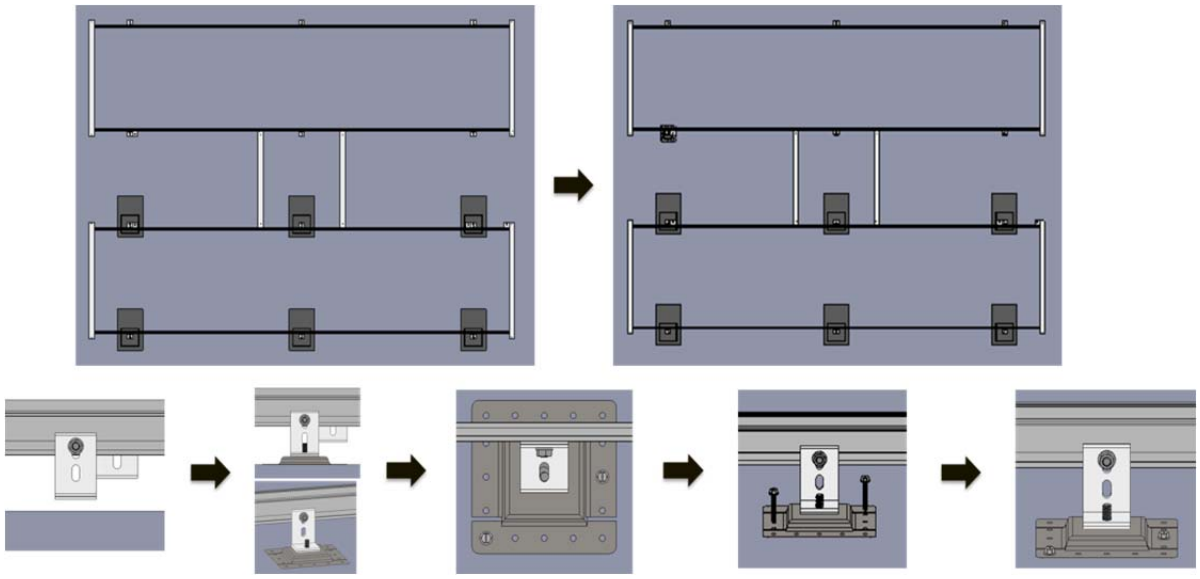


Figure 7.12: Installation procedure step 9.

Step 10: Double check that the 2 spacers used in step 8 are still lined up properly. Then tighten all the remaining Ls (*Fig. 7.13*).

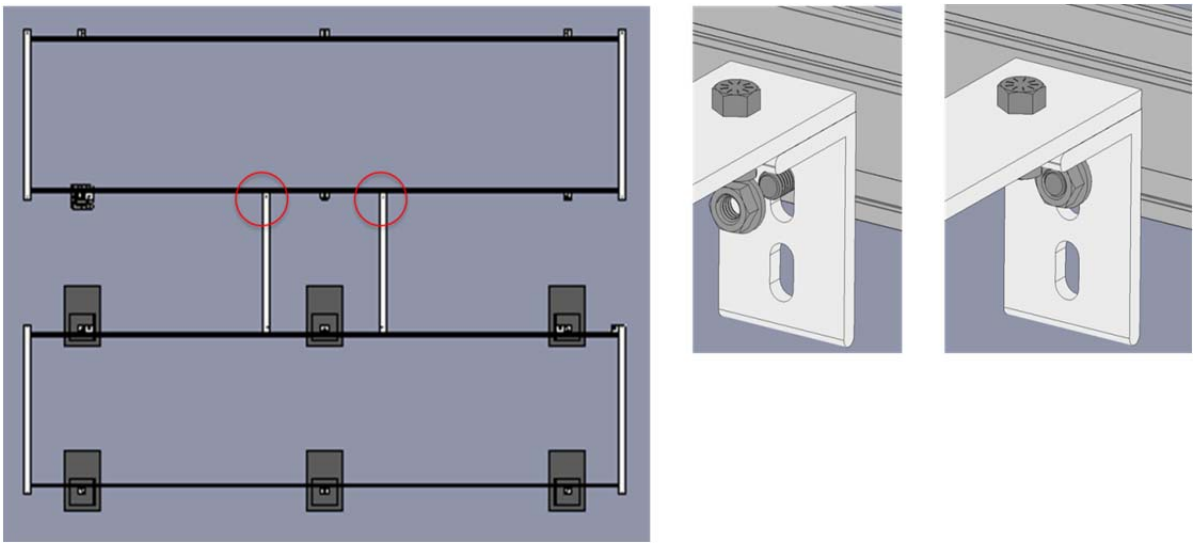


Figure 7.13: Installation procedure step 10.

Step 11: Install the bottom part of the right flashing of the third rail, installing only 2 screws in each (*Fig. 7.14*).

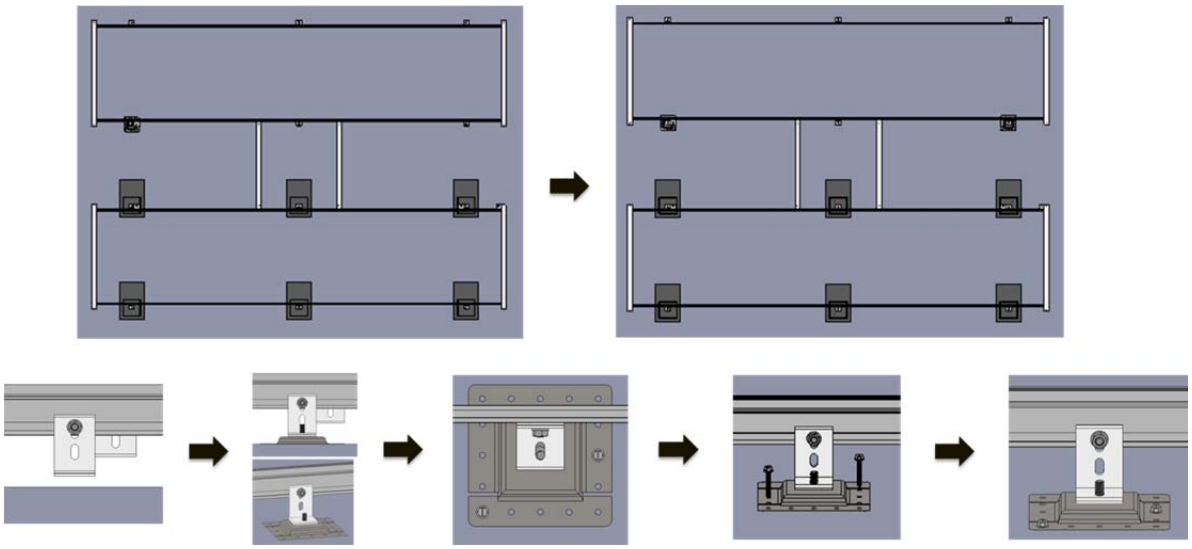


Figure 7.14: Installation procedure step 11.

Step 12: Continue installing the flashings on the third and fourth rails in a similar way performed for the first and second rail (*Fig. 7.15*).

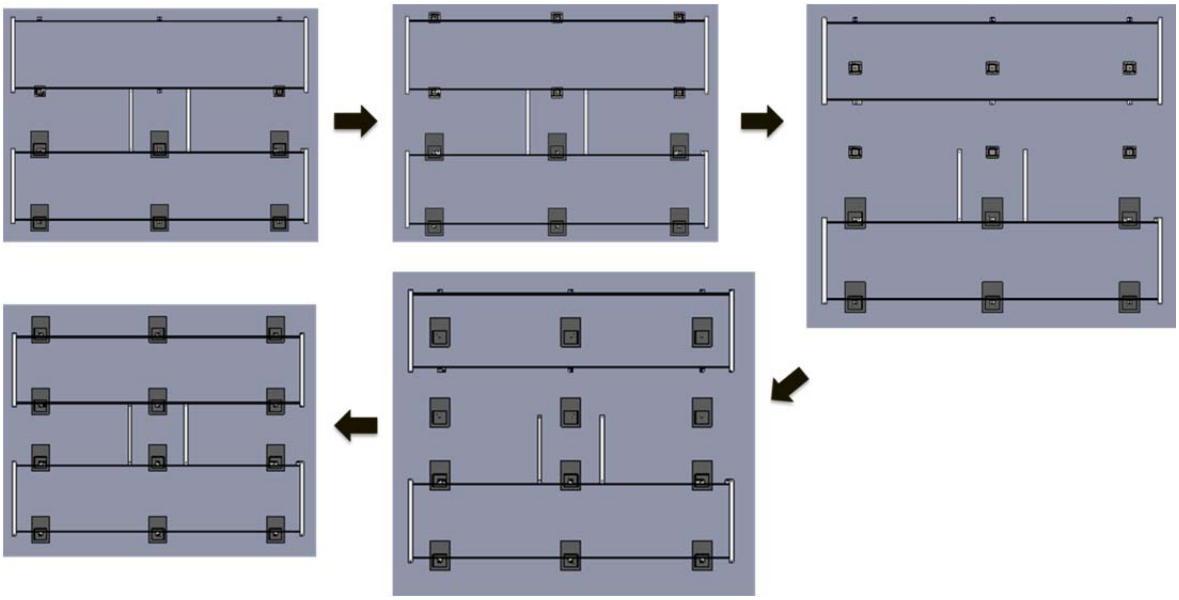


Figure 7.15: Installation procedure step 12.

Step 13: Tighten all remaining related spacers as shown (*Fig. 7.16*).

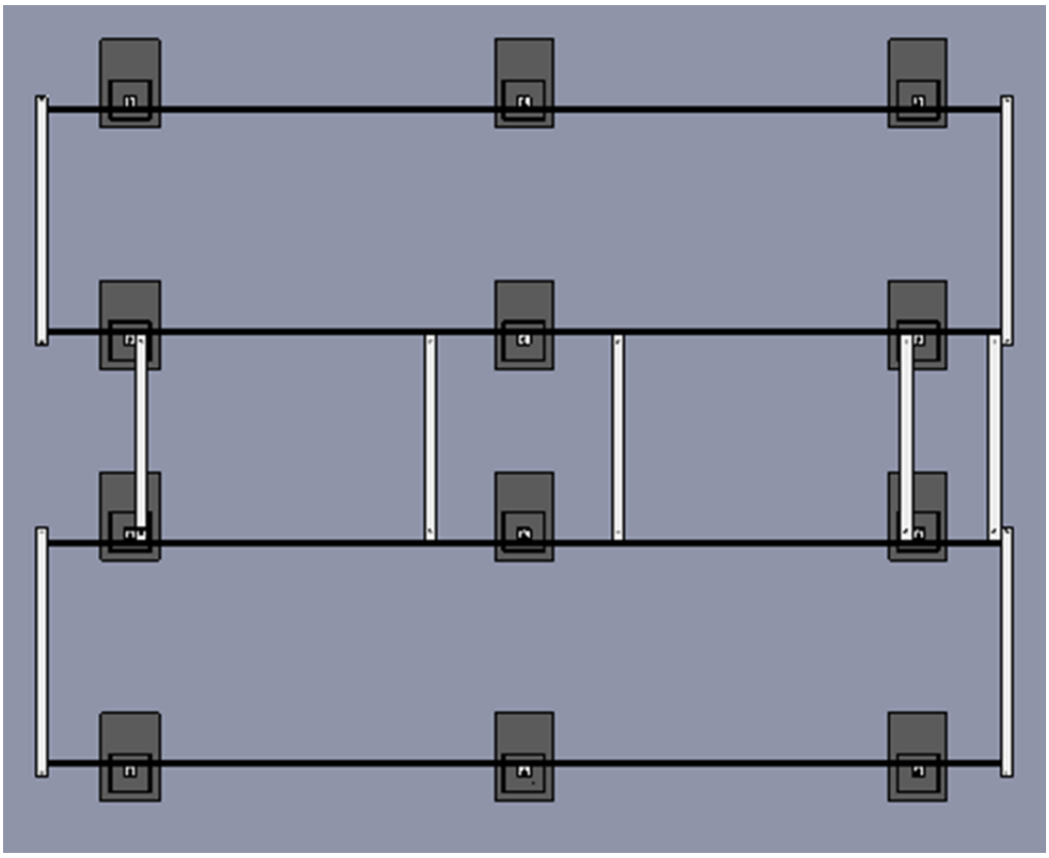


Figure 7.16: Installation procedure step 13.

7-4-2 1kW Racking System

Step 14: Insert 4 L foots in the first rail, facing the bottom (*Fig. 7.17*).

14.1 Tighten the 1st L at the very edge on the left (for the left end spacer) [facing up; the same level as the top of the rail].

14.2 Tighten the 2nd L at 16" from the left edge of the rail (for flashing) [facing down].

14.3 Tighten the 3rd L at 16" from the right edge of the rail (for flashing) [facing down].

14.4 Tighten the 4th L at the very edge on the right (for the right end spacer) [facing up; the same level as the top of the rail].

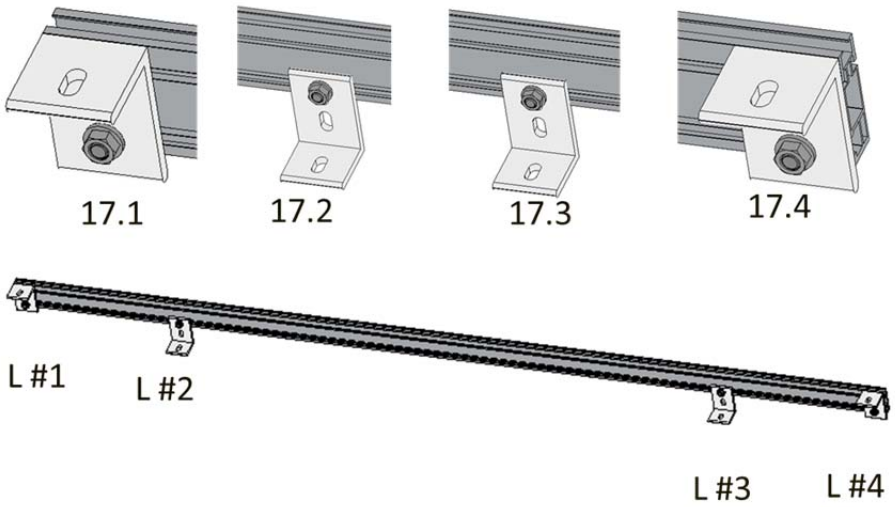


Figure 7.17: Installation procedure step 14.

Step 15: Insert 6 L foots in the second rail, facing away from the first rail (*Fig. 7.18*).

15.1 Tighten the 1st L at the very edge on the left (for the left end spacer) [facing up; the same level as the top of the rail].

15.2 Tighten the 2nd L at 16'' from the left edge of the rail (for flashing) [facing down].

15.3 Tighten the 3rd L at 16'' to the right of the 2nd L. (for the spacer holding the power electronics' enclosure) [facing down; more than 1/4'' from the rail.]

15.4 Tighten the 6th L at the very edge on the right (for the right end spacer) [facing up; the same level as the top of the rail].

15.5 Tighten the 5th L at 16'' from the right edge of the rail (for flashing) [facing down].

15.6 Tighten the 4th L at 16'' to the left of the 5th L. (or the spacer holding the power electronics' enclosure) [facing down; more than 1/4'' from the rail].

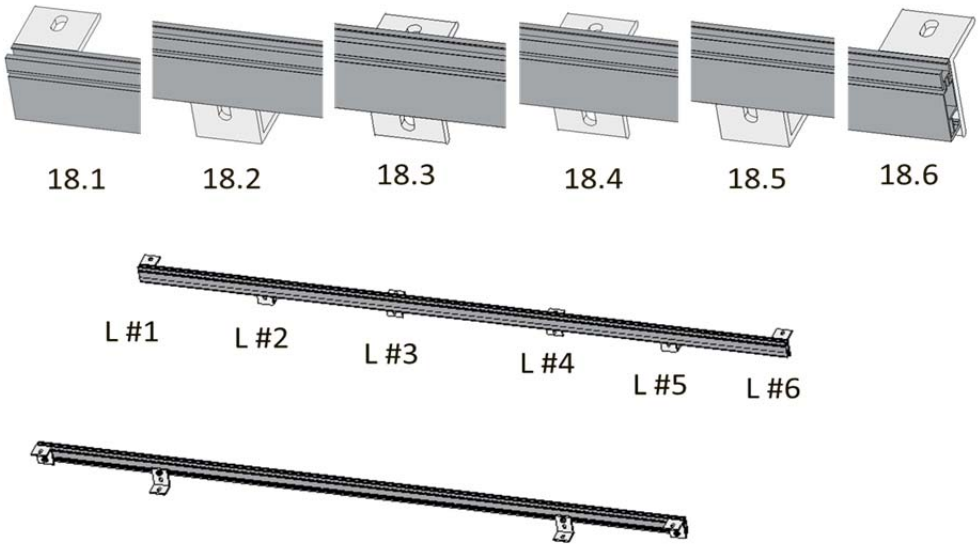


Figure 7.18: Installation procedure step 15.

Step 16: Attach the two end spacers (*Fig. 7.19*).

16.1 Tighten one end spacer on the very left of the first and second rails.

16.2 Tighten one end spacer on the very right of the first and second rails.

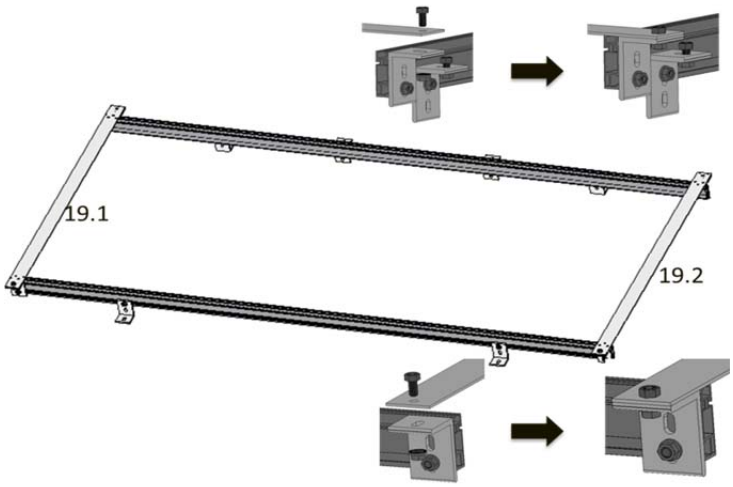


Figure 7.19: Installation procedure step 16.

Step 17: Align the rectangle formed by rail 1 and rail 2 for 1 kW system to be in line with the rail 1 and rail 2 for 2kW system (*Fig. 7.20*).

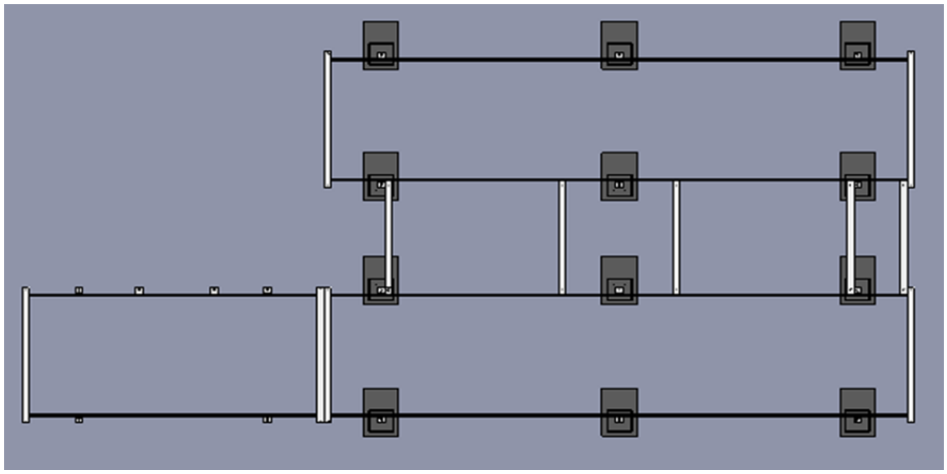


Figure 7.20: Installation procedure step 17.

Step 18: Install the bottom part of the flashings for the first 2 rails for 1 kW system (*Fig. 7.21*).

18.1 Install only 2 screws in each flashing.

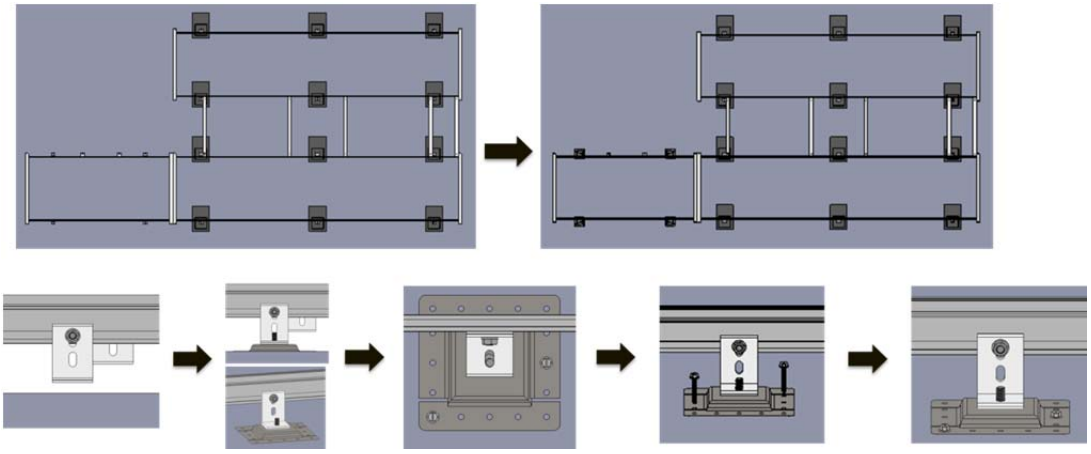


Figure 7.21: Installation procedure step 18.

Step 19: Repeat step 14 through 16 for the triangle formed with the 3rd and 4th rails.

Step 20: Finish installation of the rectangle formed by the first and second rails (*Fig. 7.22*).

20.1 Move the said rectangle by about 2' as shown.

20.2 Install all the bottom flashing screws as shown.

20.3 Install the top part of the flashing as shown.

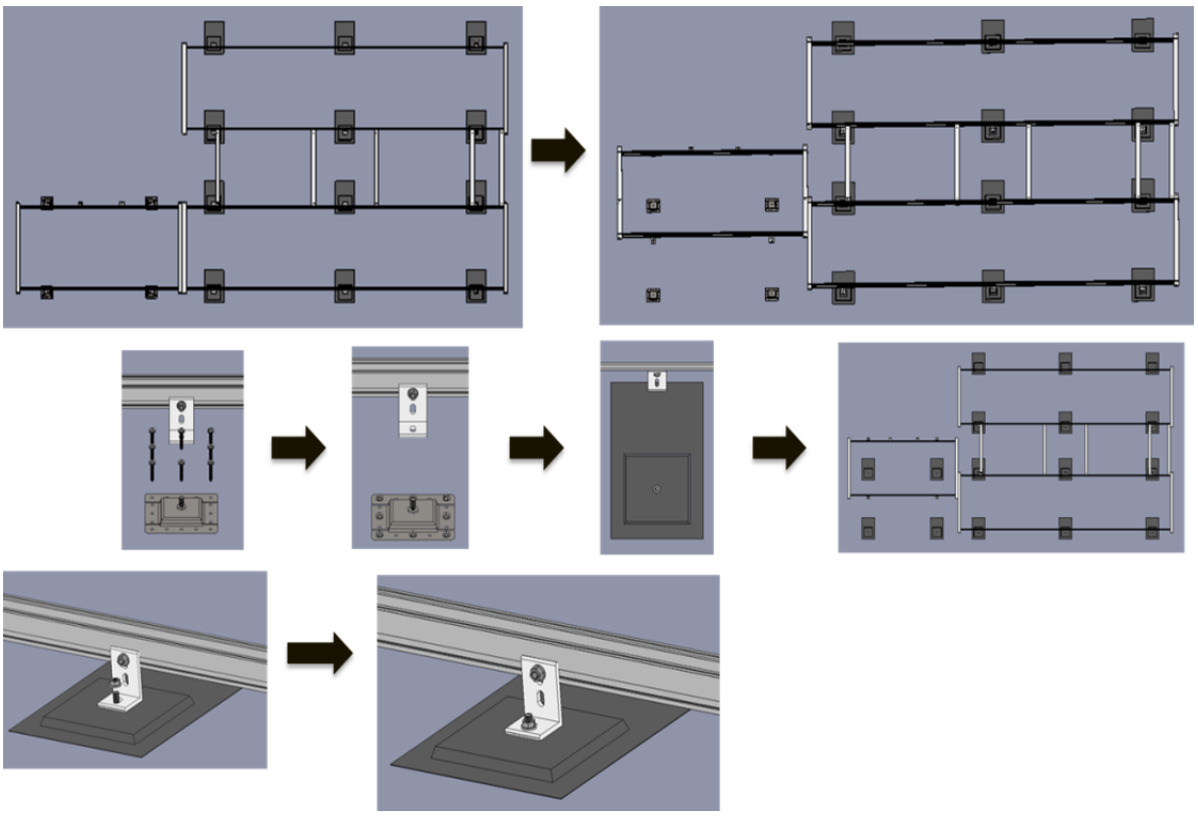


Figure 7.22: Installation procedure step 20.

Step 21: Lineup the rectangle formed by the third and fourth rail to be adjacent to the one formed by the first and second rails (*Fig. 7.23*).

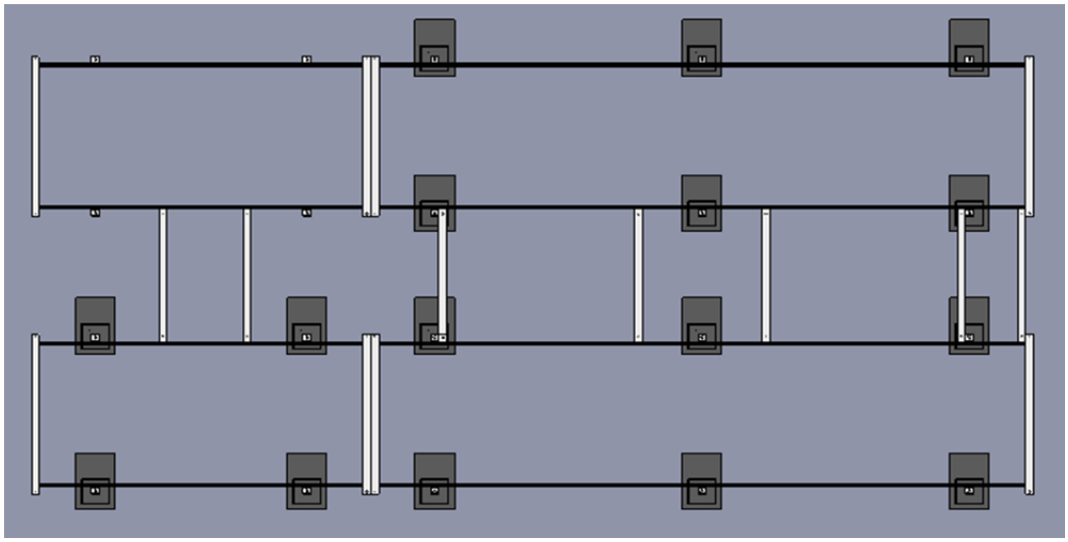


Figure 7.23: Installation procedure step 21.

<u>Step 22:</u> Position the 2 spacers for the power electronics' enclosure (*Fig. 7.24*).

22.1 To fit properly (approximately 90 degree angle) between rail 3 and rail 4.

22.2 Do not yet tighten the said spacers but make sure that it is aligned properly prior to performing the following step.

22.3 Tighten 4th L and 6th L on the third rail.

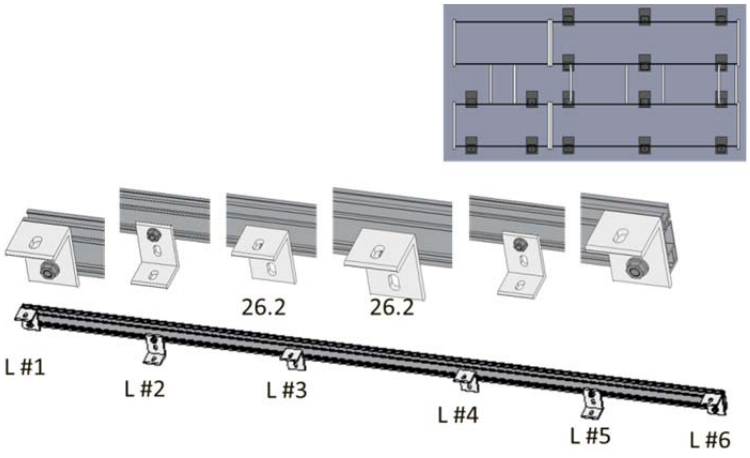


Figure 7.24: Installation procedure step 22.

Step 23: Install the bottom part of the left flashing of the third rail, installing only 2 screws in each (*Fig. 7.25*).

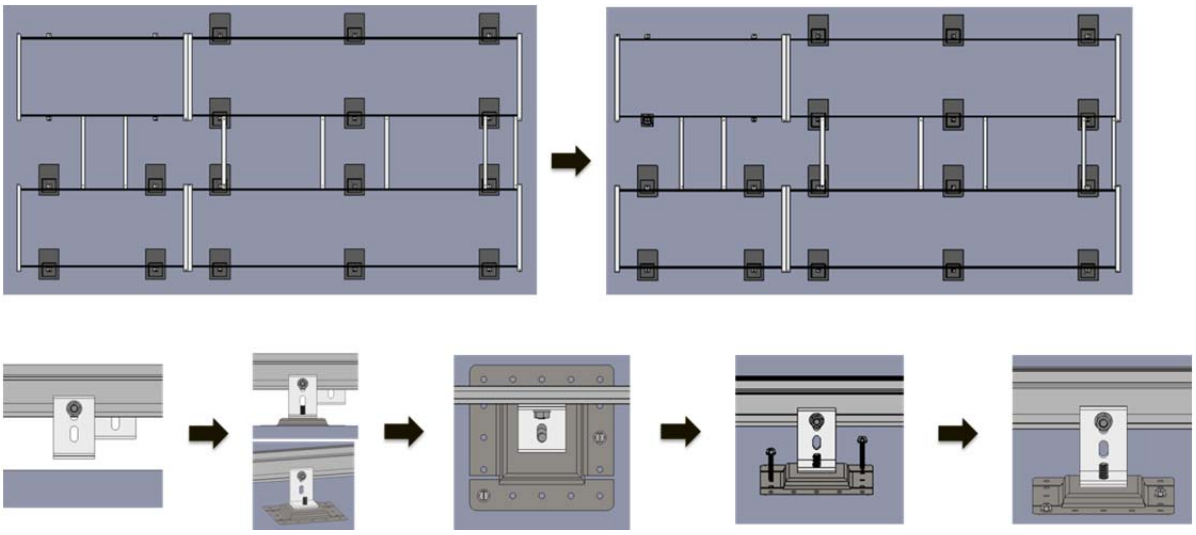


Figure 7.25: Installation procedure step 23.

Step 24: Double check that the 2 spacers used for the power electronics enclosure are still lined up properly. Then tighten all the remaining Ls (*Fig. 7.26*).

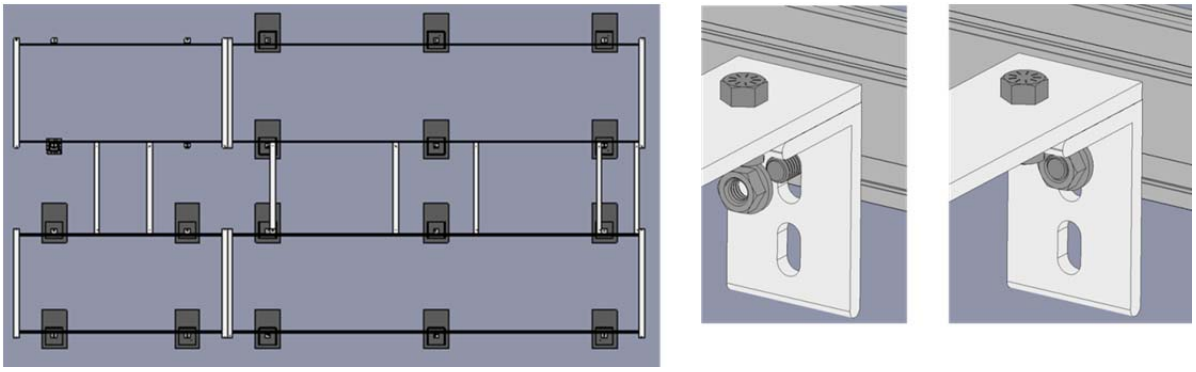


Figure 7.26: Installation procedure step 24.

Step 25: Install the bottom part of the right flashing of the third rail, installing only 2 screws in each (*Fig. 7.27*).

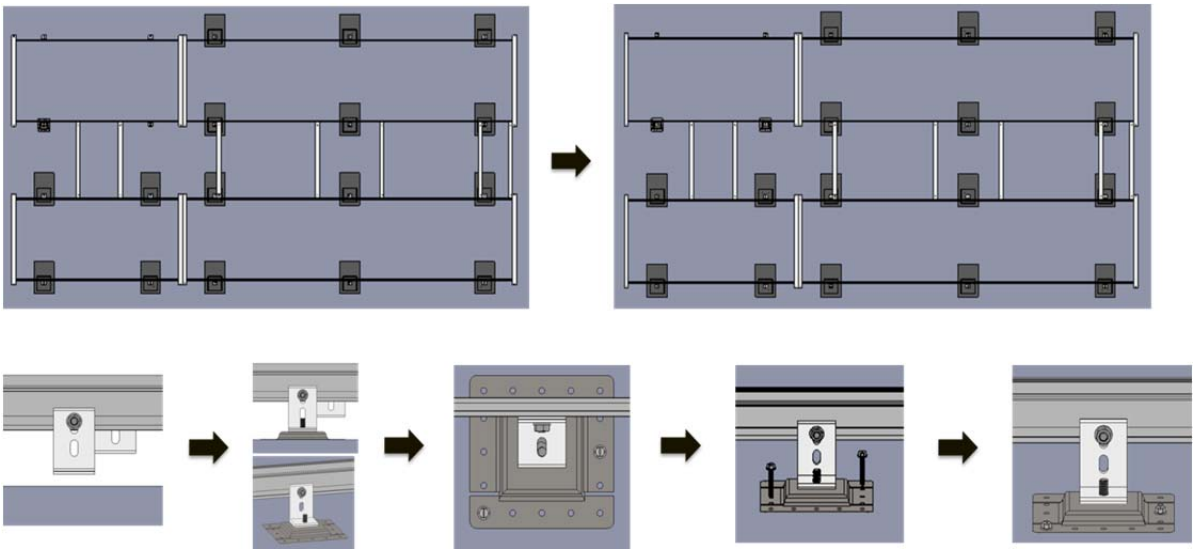


Figure 7.27: Installation procedure step 25.

Step 26: Continue installing the flashings on the third and fourth rails in a similar way performed for the first and second rail (*Fig. 7.28*).

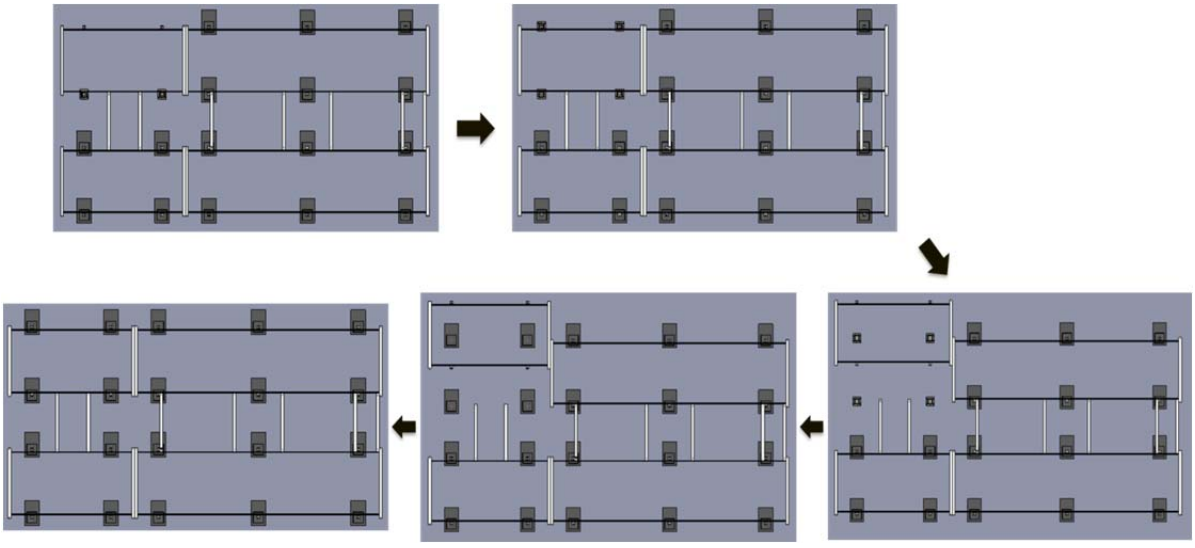


Figure 7.28: Installation procedure step 26.

Step 27: Tighten all remaining related spacers.

Step 28: Install the 1kW and 2kW power electronics' enclosures (*Fig. 7.29*).

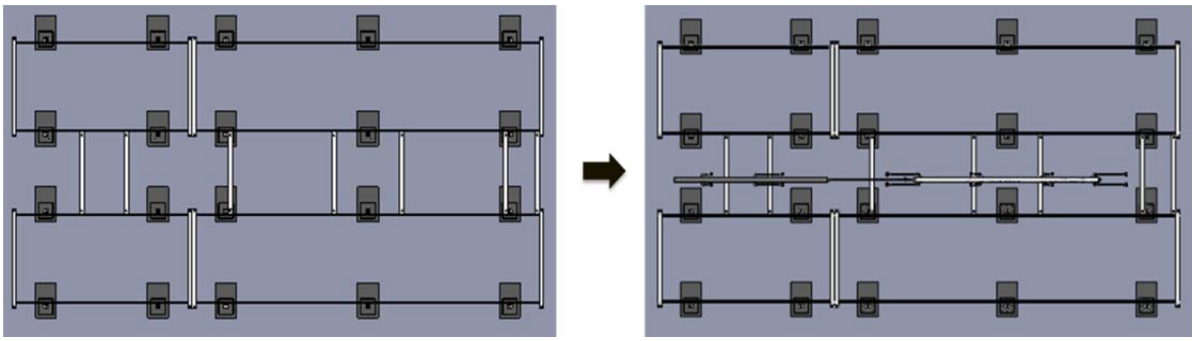


Figure 7.29: Installation procedure step 28.

Step 29: Connect the 1kW to the 2kW power electronics' integrated enclosures (*Fig. 7.30*).

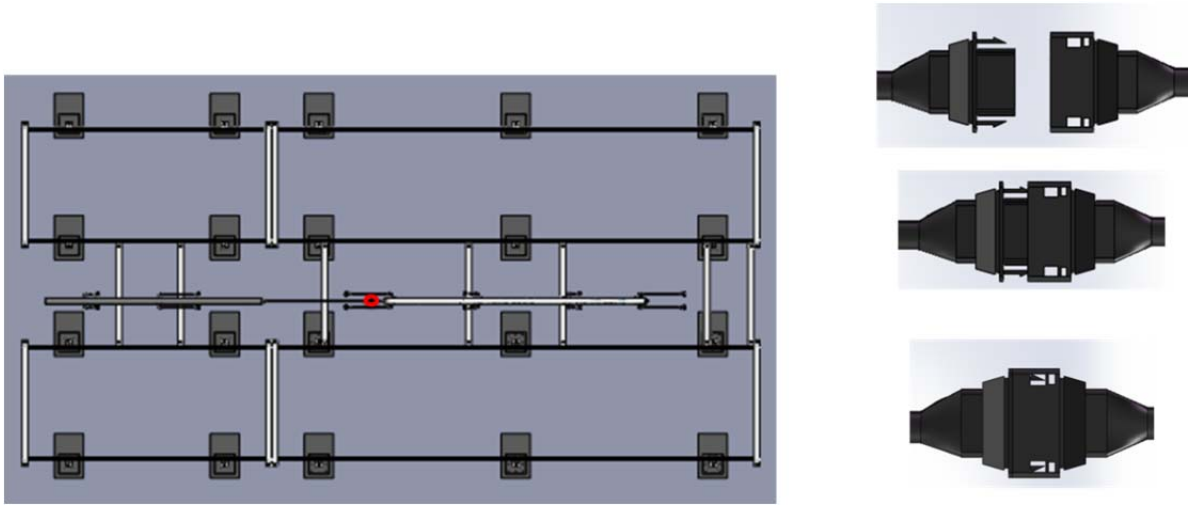


Figure 7.30: Installation procedure step 29.

Step 30: Install the PV panels and connect each at the time of installation (*Fig. 7.31*).

30.1 Panel installation should either be clockwise or counterclockwise. Connect each panel once installed.

Or,

30.2 Install top and bottom (right to left or left to right) and connect each panel once installed.

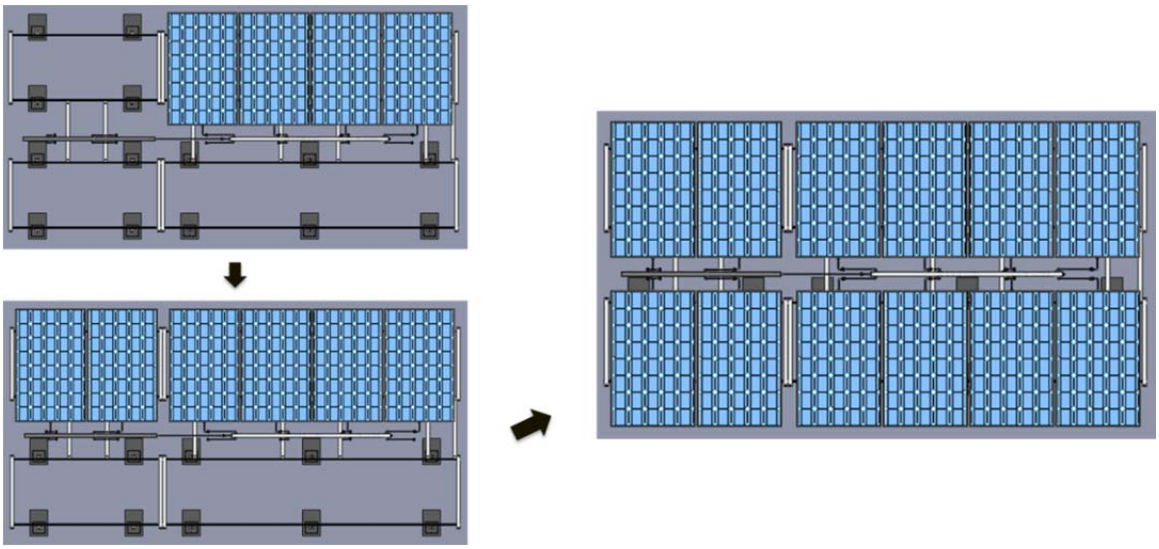


Figure 7.31: Installation procedure step 30.

Step 31: Slide the one foot PVC pipe through the cable coming out of the last power electronics enclosure as shown. The said PVC is for cable management in order to prevent the cable from touching the roof (*Fig. 7.32*).

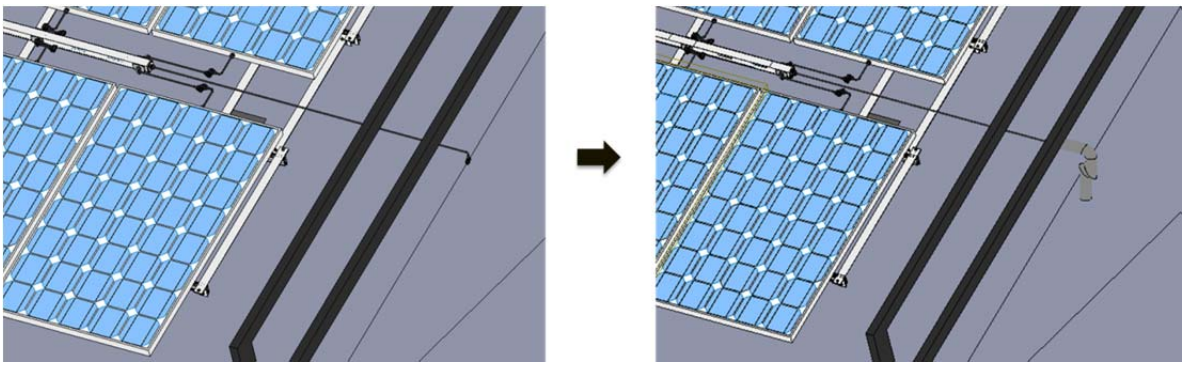


Figure 7.32: Installation procedure step 31.

Step 32: Make the connection to the top of the Cable Junction & Reeling Box (*Fig. 7.33*).

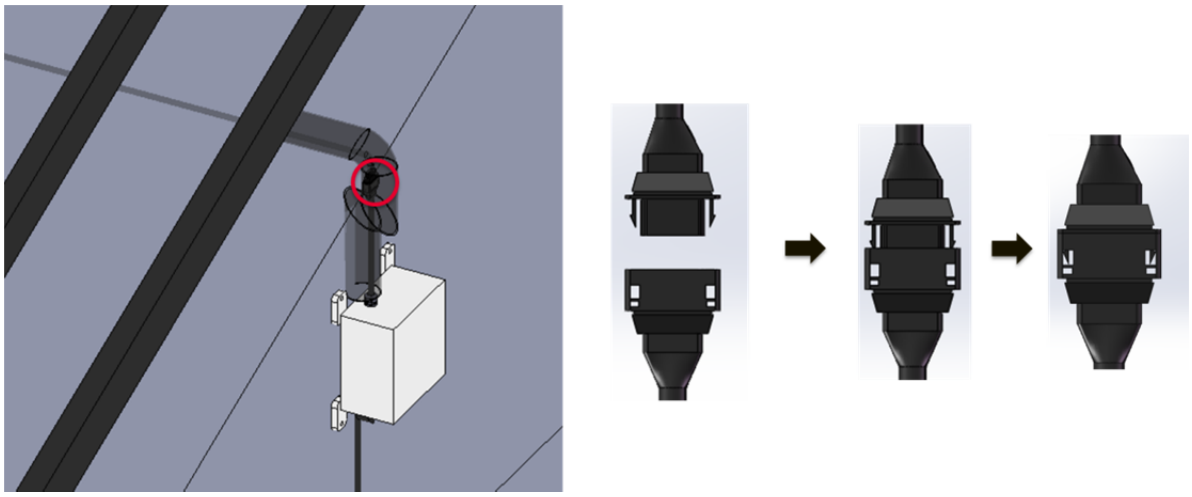


Figure 7.33: Installation procedure step 32.

Step 33: Slide back the PVC and install 2 clamps to firmly attach to the dwelling vertical wall (*Fig. 7.34*).

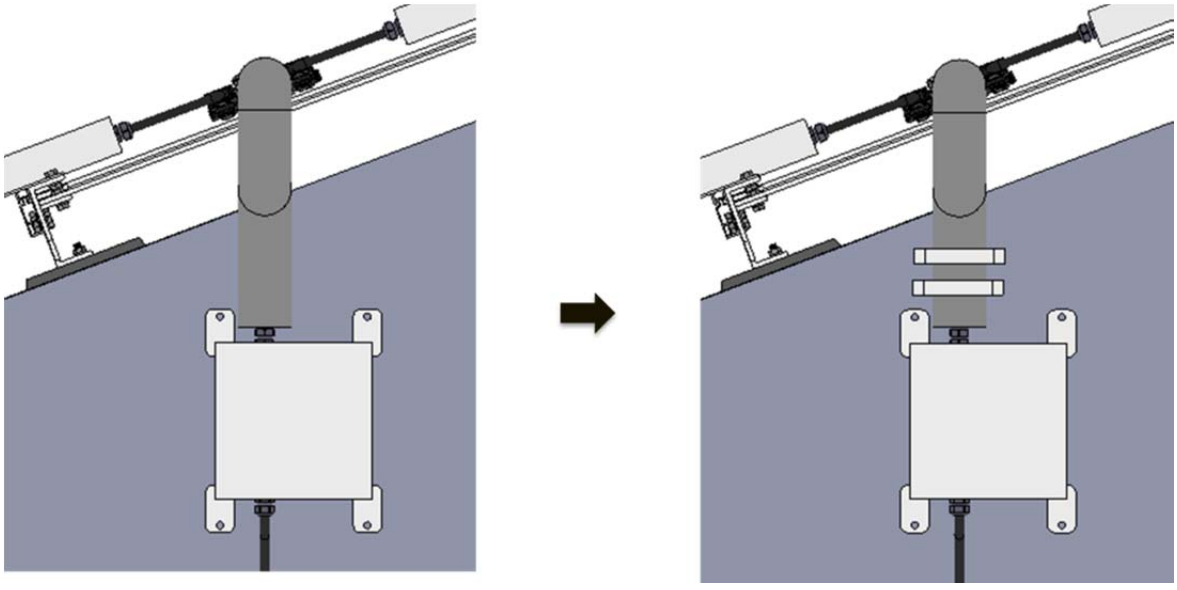


Figure 7.34: Installation procedure step 33.

Step 34: Pull and position the Reeling Box down for the cable assembly to be tight at the roof (*Fig. 7.35*).

The Cable Reeling & Junction Box is proposed to be available in 3 part numbers, with different cable length each, for residential applications. One of the said part numbers would be offered for a single story dwelling; a second part number for a 2-story dwelling, and third part number for 3-story dwelling applications.

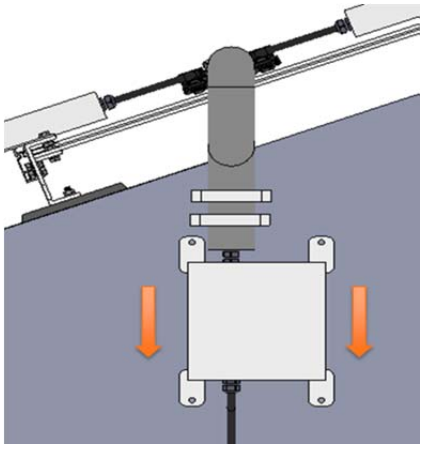


Figure 7.35: Installation procedure step 34.

Step 35: Install the Reeling Box on the vertical wall of the dwelling at the position determined in prior step (*Fig. 7.36*).

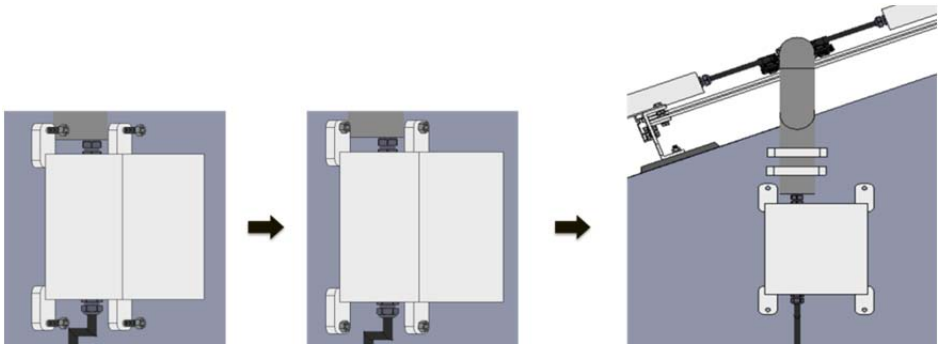


Figure 7.36: Installation procedure step 35.

Step 36: Pull the cable that is reeled inside the Reeling Box to the length needed to connect with PUI (*Fig. 7.37*).

Pull the cable (which has a connector at its end) that is reeled inside the Reeling Box to the length needed to connect to the installed PUI cable (which is in a conduit designed to be 10' from the ground as per the NEC code) that has an already installed connector (where the end of the conduit is waterproofed using heat shrink slice of rubber or the desired material used in production).

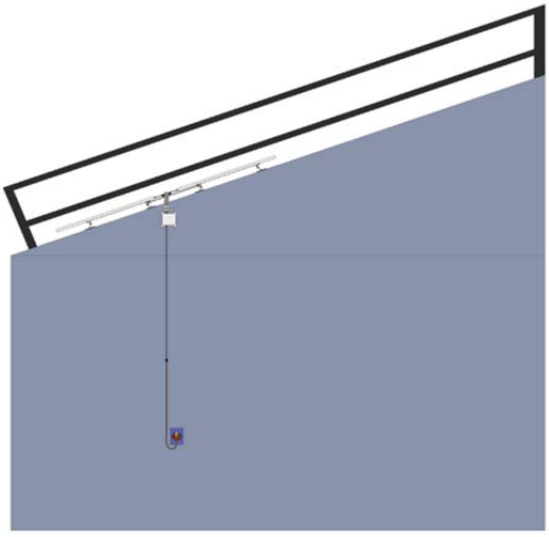


Figure 7.37: Installation procedure step 36.

Step 37: Clamp (or strap) the cable to the vertical wall as per the NEC requirement.

Per *NEC* 334.30, type USE conductors "shall be supported and secured by staples, cable ties, straps, hangers, or similar fittings designed and installed so as not to damage the cable, at intervals not exceeding 1.4 m (4.6 feet) and within 300 mm (12 inches) of every outlet box.

Step 38: Tighten the gland of the bottom of the Reeling Box (*Fig. 7.38*).

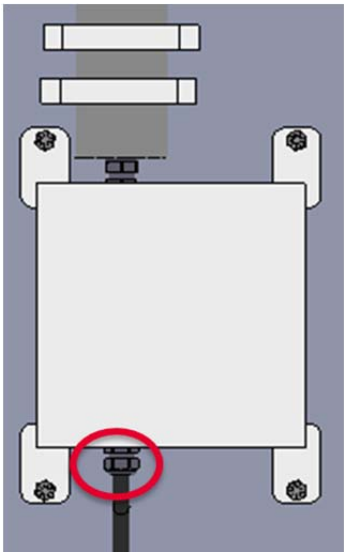


Figure 7.38: Installation procedure step 38.

With step 38, the proposed system integration is accomplished. Fig. 7.39 illustrates a drawing of the installed 3 kW residential PnP solar system.

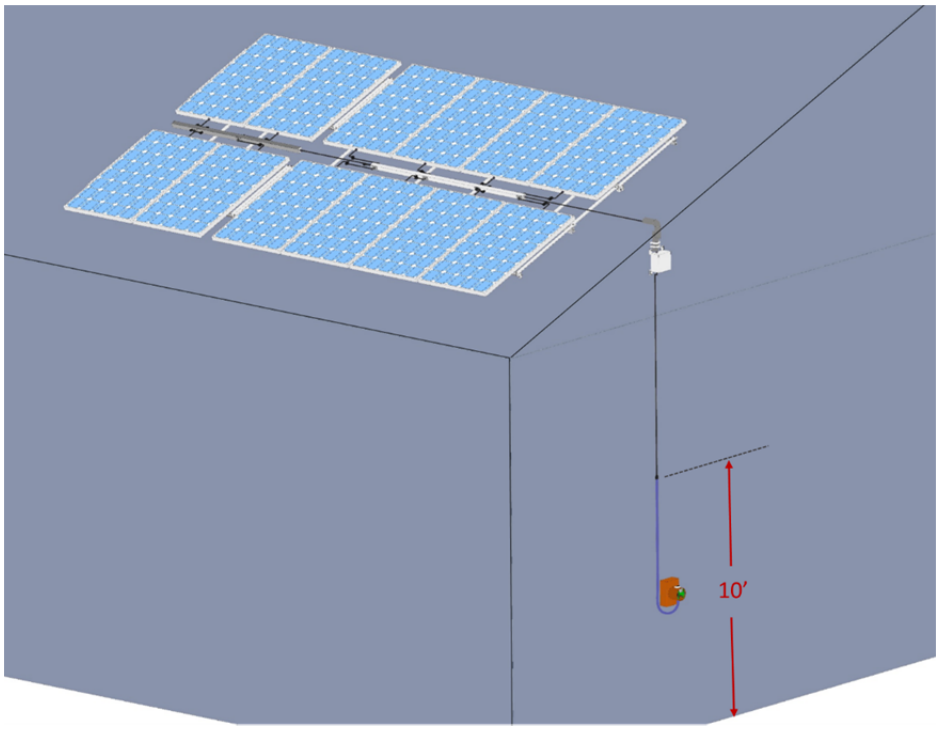


Figure 7.39: 3 kW residential PnP solar system installation designed according to the proposed approach.

7-5 Innovative PnP System Experimental Results

Fig. 7.40 illustrates the modification to the PV panel connectors, where two of the pins are used for the panel power connections and the third pin is tied to the PV panel frame in order to attach it to the system ground. Once the said 3-pin connector is connected to the power electronics' enclosure, the connectors' ground pin makes contact, where the system ground is already delivered to the said enclosure via the cable coming from the PUI.

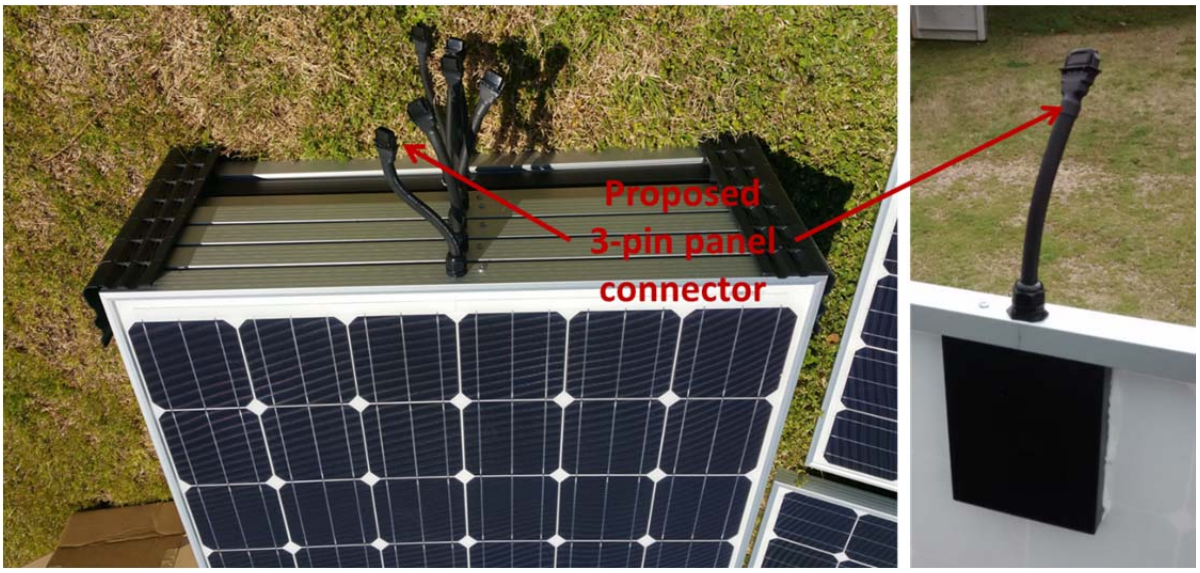


Figure 7.40: Proposed 3-pin panel connector to replace the MC4 panel connectors.

Fig. 7.41 presents a photo of the proposed cable reeling & junction box as well as the PUI described earlier in this chapter. The top side of the box has an approximately 12" cable that is terminated by one of the proposed 3-pin connector, which connects to the most right power electronics enclosure's output connector. On the bottom of the box, an adjustable length cable, with a connector at the end, is designed to connect to the cable in conduit coming out of the PV utility interface (PUI). Inside the box, an approximately 10' cable in

embedded, which serves as to allow the bottom cable coming out of the cable reeling & junction box to be adjustable.

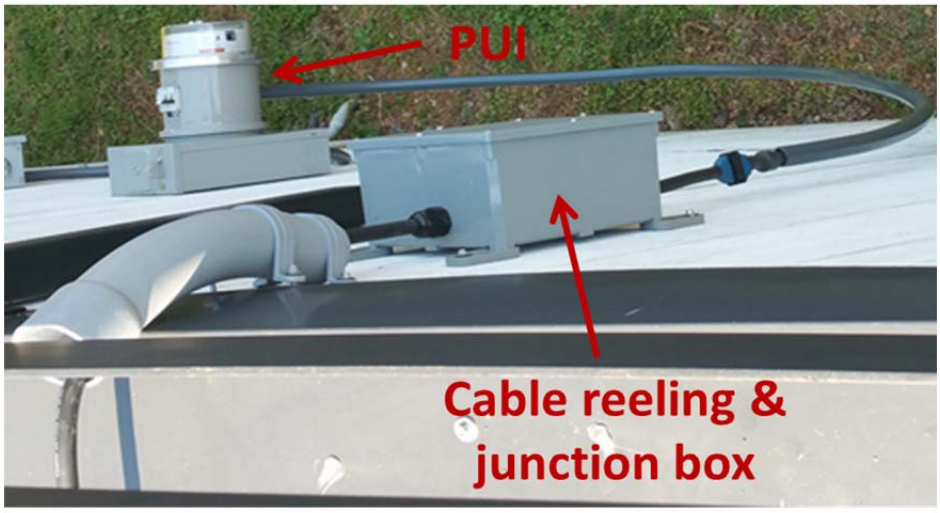


Figure 7.41: Proposed cable reeling & junction box and system connection method.

Fig. 7.42 shows a photo of the installed 3kW residential PV solar system using the proposed low cost system integration method.

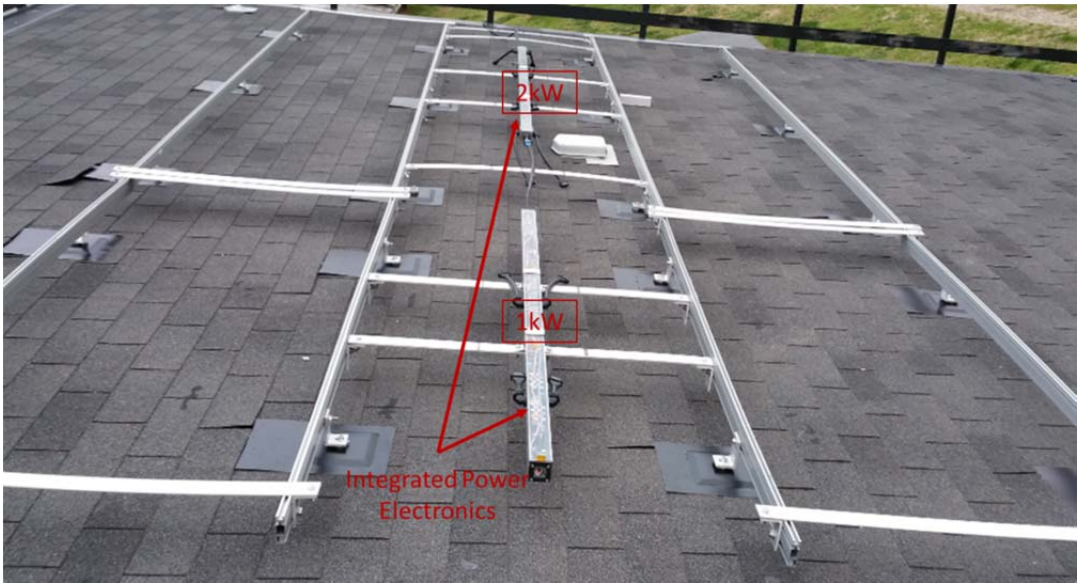


Figure 7.42: Installed integrated racking system performed according to the proposed method.

Fig. 7.43 shows a photo of the installed 3kW residential PV solar system using the proposed low cost system integration method.

Figure 7.43: Installed integrated 3kW system performed according to the proposed method.

7-6 Comparison with Current Integration and Installation Methods

The aforementioned innovative integrated installation method presents significant advantages over current related practices. According to the "Benchmarking Non-Hardware Balance-of-System (Soft) Costs for U.S. Photovoltaic Systems, Using a Bottom-Up Approach and Installer Survey – Second Edition," published by the National Renewable Energy Laboratory's (NREL) [38], the overall weighted average of approximately 21 hours or $0.13/W was obtained for residential solar PV installations. Furthermore, based on Complete Solar [39], the installation time is given as 2 to 3 days.

Moreover, based on Energy Informative [40], "The total installation time for a standard 3-kilowatt solar system of about 20 solar panels is usually somewhere between 1 and 3 days. Average labor time is 75 man-hours, which can be further broken down into electrician installation labor (49 man-hours) and non-electrician installation labor (26 man-hours)." *Table 7.2* illustrates a comparison summary of the residential solar PV system installation time.

Table 7.2: Residential solar installation time comparison.

Residential Installation time			
Source	**Time to Install**	**Quote**	**Ref.**
NREL	23 hours	"…weighted average of **23 hours** per installation."	[38]
CompleteSolar	2-3 days		[39]
Energy Informative	1-3 days	"The total installation time for a standard 3-kilowatt solar system of about 20 solar panels is usually somewhere between 1 and 3 days. **Average labor time is 75 man-hours**, which can be further broken down into electrician installation labor (49 man-hours) and non-electrician installation labor (26 man-hours)."	[40]
Accomplished Innovative Installation Method – **FREEDM Systems Center @ NCSU**	**1 hr. and 21 minutes**	Two untrained individuals needed only **one hour and 21 minutes** to install the 3kW system	

Based on the data provided in *Table 7.2*, the offered Innovative Plug and Play Residential PV System presents significant installation time advantage over current practices. Furthermore, based on [38], the installer (roofer) costs $40.49 per hour. Hence, based on

[40], it would cost $1054.52 for skilled installers to complete a 3kW residential solar system. Moreover, also based on [40], it would require 49 man-hours for an electrician's installation labor. Additionally, based on [41], electricians do charge $50 to $100 per hour, depending on where they are located in the U.S. [42] stated that "... an electrician may charge $70 just to walk in the door, that money might cover the first hour of work. ..." On the other hand, based on the United States Department of Labor, Bureau of Labor Statistics [43], the mean hourly wage for an electrician is $26.21. *Table 7.3* illustrates the proposed innovative residential solar system integration method installation cost advantage method over current practices.

Table 7.3: Residential solar installation (3kW) cost advantage of the proposed PnP installation method over current practices.

3 kW Residential Installation Cost				
Installation Method	**Electrician Cost (USD) [43]**	**Installer (Roofer) Cost (USD) [38]**	**Total Installation (Electrician + Roofer) (USD)**	**Savings due to the Proposed Innovative PnP Integration Method**
Current Practice [40]	49 X 26.21 = 1,284.29	26 X 40.49 = 1,052.74	**2337.03**	**$2,227.71**
Proposed System Integration Method	0	2 X 1.35 X 40.49 = 109.32	**109.32**	

7-7 Conclusion

In this chapter, a PnP PV residential solar system integration method was proposed. The scheme includes innovative racking integration to include the power electronics, which is proposed to be embedded in one mechanical enclosure per up to 2kW per sub-system.

Furthermore, the proposed improved racking installation technique, aiming to speed up installation while providing easy to implement system grounding is detailed. Moreover, a comprehensive installation procedure was as well experimental results are thoroughly presented. The said architecture is scalable and cost effective for implementations in residential as well as other solar applications. Two untrained individuals needed only one hour and 21 minutes to install the 3kW system illustrated in *Fig. 7.43* [47]. The method allows for PnP residential installation to be realizable at low cost.

Chapter 8: Conclusion

8-1 Conclusion

In this document, major PV solar system architectures that are currently utilized in residential and commercial applications were presented, where the advantages and disadvantages of each were introduced. Furthermore, a low cost DC/DC parallel system configuration was proposed in chapter 1. Moreover, a novel low cost simplified analog interleaving implementation technique for PV converters suitable for wide range applications was detailed in chapter 2. The scheme is based on a master/slave methodology resulting into an efficient soft-switched interleaved variable frequency flybacks operating at the boundary conduction mode (BCM).

The presented innovative control method is suitable for real-world applications while it is simple and low cost. It does not require an auxiliary startup supply nor does it utilize a PWM or driver chips. In addition to featuring reduced drive circuit losses, the scheme allows for the use of lower voltage rating switching devices. Configuration, operation principle, design equations and considerations were thoroughly covered.

In chapter 3, a BCM design model was detailed. This included a step by step component selection and transformer design optimization technique, which was detailed in chapter 4, for the DC/DC interleaved variable frequency flyback PV converter, operating in the boundary conduction mode (BCM). The calculation of the BCM flyback transformer losses as well as ferrite material selection and design implementation were presented. Several related equations were offered to include a newly derived experimentally verified equation

for calculating the minimum and maximum operating frequency. The method was utilized to for the design of the 250W converter prototype.

In chapter 5, innovative startup, turn ON, turn OFF, and control circuits were introduced. Each of the said circuits uses very low cost and efficient discrete components, resulting in a very low cost and efficient converter. With the aforementioned circuits, the converter operates without the need for clock, PWM or driver chips.

Experimental results of the converter prototypes were detailed in chapter 6. The efficient design, following the design model and optimization introduced in chapters 3 and 4, resulted in the use of 80V voltage rated MOSFETs for both the master and slave interleaved flybacks presented in chapter 2. The measured peak drain voltage was approximately 67V at full load. Furthermore, from testing the updated prototype, the converter achieved a California Energy Commission (CEC) Weighted Efficiency of 96.42%.

On the other hand, a novel PV plug and play system integration method was presented in chapter 7. The technique includes the integration of the power electronics in one mechanical enclosure per up to 2kW per sub-system. Furthermore, an innovative racking installation method, aimed to speed up installation while providing easy to implement system grounding, was included. A new electrical system configuration to reduce the number of used connectors, while eliminating the need for a licensed electrician in order to perform the system wiring, is an additional benefit of the proposed methodology. The said architecture is scalable and cost effective for residential and other solar applications. Two untrained individuals needed only one hour and 21 minutes to install the 3kW system illustrated in chapter 7. The method allows for PnP residential installation to be realizable at low cost.

8-2 Future Work

Integrating the startup, control, and other circuits illustrated in chapter 5, into one chip, may provide additional cost and performance advantages to the convertor. Furthermore, standardizing the 3-pin PV panel connector, illustrated in *Fig. 7.40*, is beneficial to grounding, reducing installation time, cost, and possibly the reliability of the PV solar system. Moreover, while the presented innovative plug and play (PnP) integrated solar system could work with any commercially available racking products, developing a more customized racking system may result into further reducing the installation time and system cost.

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