ABSTRACT

TRIPATHI, AWNEESH KUMAR. Enabling MVDC Grids with Bidirectional DC-DC Isolator Based on Three-phase DAB Converter with 15kV SiC Power devices. (Under the direction of Subhashish Bhattacharya.)

The Dual Active Bridge (DAB) converter is a ZVS soft switched high power-density bidirectional isolated dc-dc converter used for high power conversion. Due to higher switching-frequency and higher efficiency enabled by the newly developed state of the art high-voltage (HV) 10-15kV SiC devices, the MV DAB is getting popular as an equivalent compact dc-dc counterpart of the conventional bulky ac transformer for voltage conversion and isolation. The MV DAB has thus emerged as the key enabler of dc micro-grids which are getting popular for navy-ship power systems, data-centers and offshore renewable energy integration. The MV DAB is also popularly used as the intermediate dc-dc stage of a compact and intelligent alternative of three-phase conventional transformer - a power-electronic ac-ac transformer or Transformer-less Intelligent Power Substation (TIPS). The TIPS is suitable for renewable energy integration as it offers different frequency and voltage three-phase ac or dc type interface with controlled power-flows. It can also be employed at critical grid locations as an active filter and power factor correction.

This dissertation is focused on the development and demonstration of a non-cascaded topology medium-voltage high-frequency (MV-HF) DAB converter with simple power control enabled by 15kV/40A SiC IGBT modules on high-voltage side and 1200V SiC MOSFETs on low-voltage (LV) side. The major challenges for this work are optimum specification and characterization of the MV-HF transformer and inductors, optimum operation and controls for higher efficiency and reduced EMI using ZVS enforcement techniques, common-mode mitigation and TIPS integration.

This dissertation can be roughly divided into three parts. The first part starts with selection of a three-phase DAB topology for TIPS project that offers advantages of higher power-density, higher efficiency, smoother transformer current, smaller stress on the MV devices and optimum controls. A composite three-phase topology and its d-q control are proposed in this regard and they are evaluated using simulation and also on a LV hardware prototype. This evaluation of different three-phase topologies based on efficiency, operation and controls help specify the optimum topology and transformer arrangement for medium-voltage hardware. The preliminary magnetics design and HV SiC switching data are used for extensive DAB simulation to predict problems at the MV level. The complete TIPS simulations with sensitivity analysis help to reach a final specification of the magnetics for the given device characteristics and operating conditions. The MV-HF transformer is developed by external agency based on the detailed specification. This follows with extensive characterization of the MV-HF transformer using

measurements and spice simulations to synthesize an equivalent circuit which is useful to emulate the actual MV operation in simulation and also scaled to the LV prototype for verification of smooth operation and controls. The simulation predicts ringing and EMI problem in the MV operation and thus the control objective is modified. A DAB model consisting of parasitic parameters of the transformer is also studied to predict any effect on the control and ZVS operation. The MV side external filters are designed and built to minimize the parasitic ringing in the topology. The DAB control hardware is developed for the proposed algorithm and tested with and without parasitic emulation.

The second part of the dissertation focuses on the MV converter hardware development, testing and analysis of ZVS using simulations and supporting converter experiments. The ZVS range is affected by parasitics caused current ringing, duty-ratio reduction of the three-level MV converter, the converter dead time and DAB reactive power. The 15 kV/40 A SiC IGBT gate-resistance has been optimized in prior work to limit its dv/dt compatible for the gate-driver components resulting in specification of the converter dead-time. The experimental results are presented to verify the relation between ZVS condition and high dv/dt that causes EMI and added switching-loss. The DAB MV converter ZVS being a prime objective, optimum control and flexible operation of the proposed topology are proposed with experimental results. TIPS integration and grounding simulations that are used initially for specification of the MV-HF transformer, are presented with specification of the common-mode chokes used. The DAB control block-diagram is used to model DAB impedances for TIPS integration mode control tuning.

The last part of this dissertation proposes a novel series-compensation technique for ZVS in HV SiC based DAB and implements it on a simple single-phase MV DAB setup. The experimental validation is also provided. This is followed by series-injection enabled snubbered operation of the 15 kV SiC IGBT in the simple DAB converter. The turn-on losses are zero by maintaining ZVS and the turn-off losses are also reduced using the snubber as validated by experimental heat-run tests. The snubbers also limit the turn-off dv/dt resulting in smaller EMI. An intelligent gate-driver for the HV SiC devices has been proposed that can transfer critical data from the switching devices of the converter for ZVS detection and data-logging purposes. These additional operating data help the main controls to operate the DAB system in optimum condition. In the last, a comparison of 15 kV SiC IGBT with 15 kV SiC MOSFET is presented for the same target DAB application. The experimental MV NPC converter pole test results help understand the differences between the two devices from ZVS, EMI and efficiency perspective. Practically, the higher switching frequency and MV-HF transformer compactness have conflicting requirements from parasitics perspective as the ZVS range of the MV DAB becomes smaller for higher device capacitance as in case of MOSFET. This makes a clear winner difficult to predict but the thermal considerations, for higher temperature, higher power and compact packaging applications, might make SiC IGBT a better choice.

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Enabling MVDC Grids with Bidirectional DC-DC Isolator Based on Three-phase DAB Converter with 15kV SiC Power devices

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DEDICATION

I am thankful to my parents Indoo and Laxmikant, brothers Manish, Rajnish, sister in-law Menka and other family members for always backing me to pursue and complete the doctoral degree and so I dedicate this dissertation to them. I also dedicate this dissertation to all my four grandparents Baba Ramanuj and Nana Ramashankar, and finally nephews, Shivam and Saksham. I also dedicate my dissertation to my undergrad friends who predicted me doing PhD from my attitude.

BIOGRAPHY

The author, Awneesh K. Tripathi was born in a small Indian town in Gorakhpur, Uttar Pradesh in 1985. He earned B.Tech in Electrical Engineering from Harcourt Butler Technological Institute Kanpur in 2006. He secured 9th rank in Graduate Aptitude Test in Engineering 2005. He earned Master of Engineering degree in Electrical Engineering from Indian Institute of Science Bangalore in 2008. He worked at custom power supply manufacturer S.M. Creative Electronics Ltd. Gurgaon from 2008-2009 as Design Engineer in Power Technology Group. He also taught briefly at Institute of Technology and Management Gurgaon prior to joining North Carolina State University in spring 2011 as PhD graduate student. Currently he is working towards PhD in Electrical Engineering at FREEDM system center Lab in NCSU Raleigh. His research interests are high power dc-dc converter topologies, SiC based power-electronics converter development, power-electronic controller development, electrical drives, power electronic grid interface for renewable energy sources and power quality.

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LIST OF SYMBOLS

dv/dt	Switching voltage steepness
P/Q	Active to reactive power ratio
V_{an}	DAB a-phase to ac neutral voltage
V_{ao}	DAB a-phase to dc mid-point voltage
V_{Ya}	DAB secondary star a-phase to neutral voltage
$V_{\Delta a}$	DAB secondary delta a-phase to c-phase voltage
i_a	DAB primary MV side a-phase current
C_{ps}	DAB MV-HF transformer inter-winding capacitance
i_{Ya}	DAB LV star a-phase current
$i_{\Delta a}$	DAB LV delta a-phase current
V_{s1}	MV a-phase NPC converter pole top device voltage
E_a	MV a-phase transformer terminal voltage
i_{s1}	MV a-phase NPC converter pole top device current
V_{sY}	LV star a-phase converter top device voltage
i_{sY}	LV star a-phase converter top device current
π	The number pi
V_{dc1}	DAB input dc bus voltage
V_{dc2}	DAB output dc bus voltage
C_{dc2}	DAB output capacitance
V_{dc}	DAB input dc bus voltage
L_{f1}	DAB input MV side filter
$V_{n^{an}}$	DAB a-phase to ac neutral voltage n^{th} harmonic voltage
γ	DAB a-phase pole voltage per quarter cycle zero clamping angle
ω	DAB frequency
D	NPC converter duty-ratio
Z_{tie}	DAB series impedance
θ	DAB series impedance angle
ϕ_0	DAB nominal phase-angle
v_s	DAB sender end voltage
v_r	DAB receiver end voltage
L_{df1}	DAB HV side external filter inductor
R_{df1}	DAB HV side parallel damping resistor

Chapter 1

Introduction

1.1 Background

The electrical grid powered by mostly conventional energy sources is under transformation to accommodate more renewable energy sources. The coal and natural gas thermal plants are getting costlier and also cause pollution to the environment. In recent year, the world has seen more abrupt changes in the weather pattern possibly caused by what is known as green-house effect. The advances in renewable energy technology such as wind, solar has lowered the cost per unit of electricity and made them more competitive to centralized thermal plants. Therefore these are getting more into applications in the distributed as well as centralized energy-generation. The smart grid concept for optimum operation of electric grid with higher penetration of renewable generation, has accelerated the research in the area of grid-scale power electronic conversion.

1.1.1 Solid State Transformer (SST)

These converters such as Solid State Transformer (SST) provide not only suitable conversion but also quick control and flexible operation for smart grid. The renewable sources generate electricity in different forms (ac or dc) and it may often be intermittent and unreliable. For example, wind-speed might be random and therefore the turbine speed changes frequently. There is a need of suitable grid interface with variable frequency (ac-dc-ac) and also a battery storage for increasing the equivalent inertia of the distributed generator for stability. Another example is the solar PV generating low-voltage dc. There is conversion and control challenge to inter-connect the renewable energy sources to local loads and to the grid for improving the reliability at the demand side. The requirements for a suitable power interface between grid and load/grid can be listed as-

- Compatible voltage type at the inter-connections (ac, dc, frequency)
- Harmonic-free current injection to the grid

- Bi-directional power-transfer capability
- Smooth and reliable control
- Galvanic isolation for safety and protection
- Compact size, efficient and economical
- Reliable and simple maintenance

The concept of such a power-electronics based transformer, in varying motivation and target application, is well known with different names by different contributors [1, 2, 3, 4, 5, 6, 7, 8, 9]. A conventional approach is to employ a bi-directional PWM converter for grid-dc bus conversion and then use a dc-dc (isolation) and dc-ac converter to interconnect the sources/loads to the common dc bus [7]. At the ac-side, better sinusoidal waveform can be produced from dc either by increasing switching frequency or number of voltage levels. Increasing switching frequency causes increased device switching-losses and so there is an upper limit. Increasing converter switching voltage level, helps in reducing device voltage rating required for an application along-with better waveforms. However, the number of the output voltage levels is practically limited due to complexity and imbalance of the dc link capacitor voltages.

The recent popularity of solid state transformer (SST) [10], Transformer-less Intelligent Power Substation (TIPS) [11] and dc micro-grid for integrating renewable energy generation [12], has triggered research in the medium-voltage (MV) high-power isolated dc-dc converters [13]. With increase in the depth of non-linear power electronic loads in household, there might be a need of active filtering at the distribution level. A conventional method to compensate reactive power using switched capacitors may be costly and bulky. The above power converter can also play role for voltage and power-factor correction. The conventional 60 Hz transformer is simple and reliable but bulky and can not interconnect two asynchronous networks or dc type source. The SST or TIPS is an alternative to the conventional line-frequency bulky distribution transformer [14, 10]. Thus the SST or TIPS may get application for the conventional transformer at critical locations providing benefit of multi-dimension controls like reactive-power compensation, active filtering along-with active power flow controls [10, 14, 15, 16, 17]. With advancement in power-electronics device technology, it has been now possible to avail HV SiC devices capable of fast switching (5-20 kHz) at 10-15 kV medium-voltage levels. As a result, single switch non-cascaded converter based high-frequency (HF) transformers can be used for isolation instead of the cascaded converter due to simplicity and compactness. SST or TIPS is a three-stage converter consisting of a HF dc-dc link as the intermediate stage. The HF transformer is light and compact compared to its conventional counterpart. SST/TIPS is suitable for renewable energy interfacing as it can vary the end converter frequencies and voltage so that it can operate at maximum power point tracking (MPPT). It can also be employed at critical grid locations as active filter and reactive compensator.

Figure 1.1: UNIFLEX project photograph

1.1.2 Dual Active Bridge (DAB)

The new developments in wide band gap device technology has resulted in single chip HV blocking and high-frequency (HF) switching devices. The dual active bridge (DAB) is a zero voltage switching (ZVS) soft-switched, high power-density, isolated, bidirectional dc-dc converter first proposed in [18, 19, 20] for high-power grid-scale applications. It is used as an intermediate HF dc-dc isolation and voltage conversion stage of a SST [21] for applications like PV-grid, wind-grid or grid-grid interfaces and dc transformer for dc micro-grids [12]. Fig. 1.1 shows an application of the DAB topology for high-power medium-frequency conversion in UNIFLEX project [22].

1.1.3 DAB as DC Transformer

The DAB is often used as a dc transformer for the dc micro-grid for different loads/sources and intermediate dc-dc isolation stage of a TIPS [23]. The TIPS is an alternative for the conventional distribution transformer. It consists of ac-dc Active Front-End Converter (AFEC), isolated dc-dc DAB and dc-ac inverter stages. The DAB is employed at the output stage of a recently popular MV dc interface [24]. A typical MV dc micro-grid is shown in Fig. 1.2. It can support a mixture of loads/sources and feed power back to the dc micro-grid when a renewable source like photovoltaic generates power during day.

1.2 Research Motivation

1.2.1 15kV SiC IGBT based DAB Topology

A typical Modular Multi-level Converter (MMC) topology schematic, using lower voltage devices for MV applications, is shown in Fig. 1.3. The MMC topology suffers from light load poor efficiency,

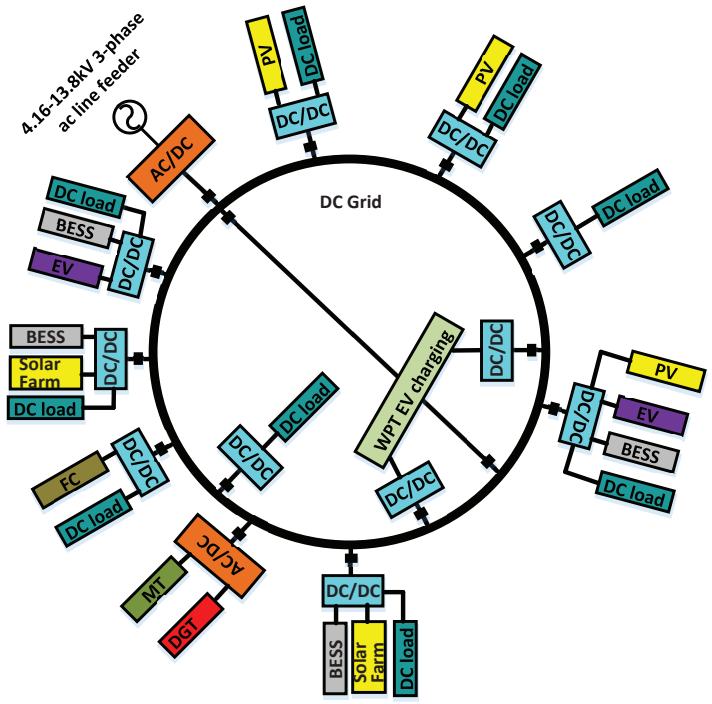


Figure 1.2: A typical ring type dc micro-grid for navy ship

higher conduction-loss and complexity in terms of topology and controls. The higher blocking voltage capability has resulted in use of simpler topology over the cascaded H-bridge (CHB) which becomes complex with number of cells and requires complex balancing control [25]. The HV SiC devices are very promising as an alternative to MMC or MMC LV cells [26]. They are also promising for dc micro-grids that are potential candidates for navy ships, data-centers and under sea offshore dc micro-grid application [16]. Prior to the development of HV SiC devices, the 6.5kV Si IGBT is the maximum rated device used in PWM converters in terms of voltage and switching frequency [27]. The range of switching frequency is still 0.5-2 kHz. Thus a converter would require large passive components. A popular MV distribution grid standard suitable for dc micro-grid interface in US is 4.16 kV/60Hz three-phase system [13]. This grid interface needs a dc bus of at-least 7kV. A non-cascaded 8 kV H-bridge topology which has the advantages of simpler control and lesser number of devices, requires at least 4-level topology for using 6.5kV IGBTs. Cree Inc. has developed SiC technology IGBTs rated for 15 kV for TIPS project. Fig. 1.4 shows the photograph of its packaging. It has a 15 kV, 20 A IGBT chip with $2x10$ kV, 10 A diodes. The 15 kV SiC MOSFET have also been recently developed in a research program. Such HV SiC devices have enabled non-cascaded MV converter topologies. The high-frequency (HF) dc-dc Dual Active Bridge (DAB) based on simpler MV side converter is getting popular for dc micro-grid applications. It has higher efficiency, power-density and mean-time-between-failure (MTBF) over

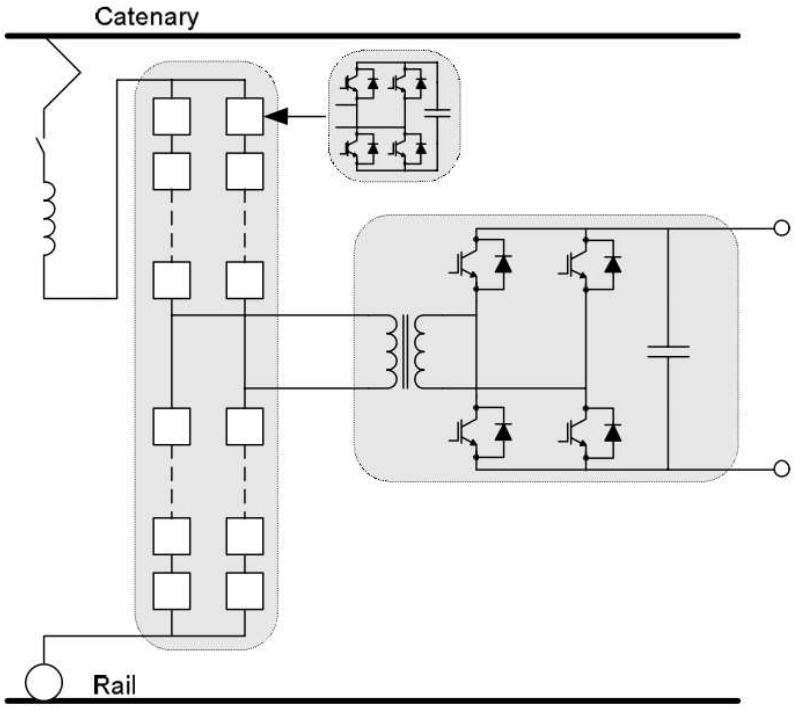


Figure 1.3: PET MMC topology

the cascaded DAB topology. The control of such a compact medium-voltage high-frequency (MV-HF) DAB is simple. A MV 3-level neutral-point clamped (NPC) pole has been developed using 15 kV SiC IGBTs [28]. These poles can be used in MV grid interface TIPS topology [11]. This MV topology offers simple control. The switching capability is in the high-frequency (HF) 3-10 kHz range for these devices. This reduces the filter & series-inductor size on the ac-dc AFEC and the MV-HF transformer size of the DAB dc-dc stage. But these devices have high dv/dt switching which combined with the magnetic component's parasitics and the required dead-time, causes EMI and control challenges for the AFEC [29] and non-ZVS operation in the DAB at light load [30].

1.2.2 Transformer-less Intelligent Power Substation (TIPS)

The TIPS is a three-phase (3-ph) three-stage ac-dc-dc-ac SST system based on a non-cascaded structure [11]. It interfaces medium-voltage (MV) 13.8 kV distribution grid with low-voltage (LV) 480 V grid. The MV side converters use 15 kV SiC IGBTs which are characterized in [31]. The first stage of the TIPS is an AFEC which converts the 3-ph ac voltage to 22 kV dc [29]. A dc-dc Dual Active Bridge (DAB) converter steps down it to 800 V dc. The DAB is based on a compact high-frequency (HF) transformer for conversion and galvanic isolation. The TIPS MV-HF transformers are presented in [32]. TIPS is a HF link three-stage ac-dc-dc-ac converter based three-phase solid-state alternative for a

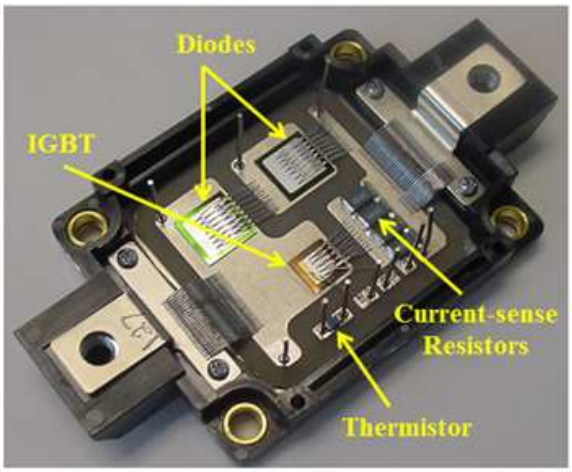


Figure 1.4: 15 kV SiC IGBT co-pack module open photo photograph, built by Cree packaged by Powerex

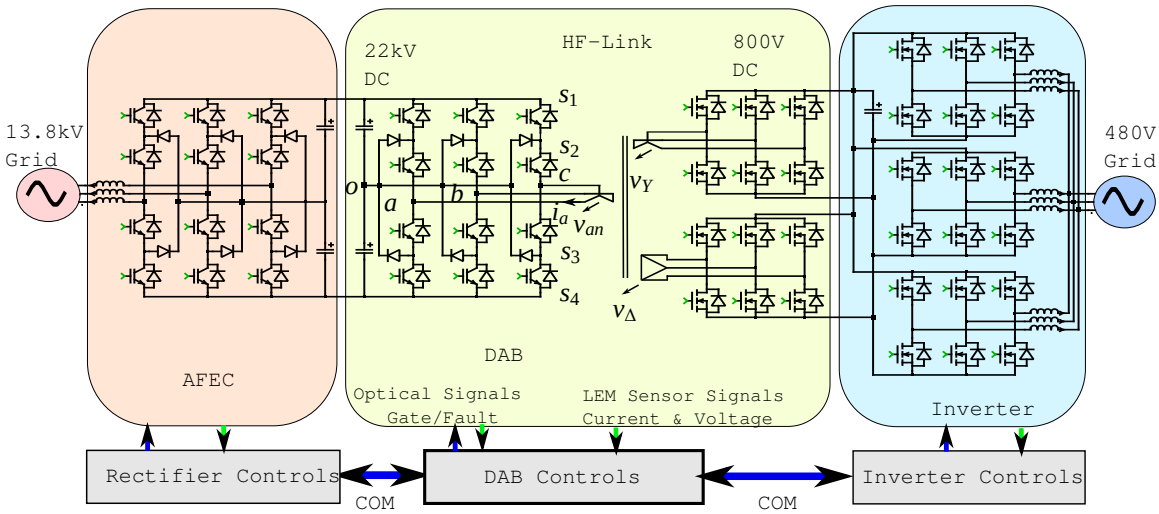


Figure 1.5: TIPS topology schematic

conventional distribution-transformer connecting a 13.8 kV and 480 V grids and ensuring bi-directional power flow [11]. It has three stages of power-conversion namely Rectifier, DAB dc-dc converter and Inverter as shown in Fig. 1.5. The Rectifier Module converts 13.8 kV three-phase ac supply to 22 kV dc voltage. The 22 kV dc voltage is stepped down to 800 V dc by the DAB converter at the link-frequency of 10 kHz. The 800 V dc is converted to 480 V ac for grid connection using the Inverter Module. High-voltage (HV) DAB converter is a soft switched high power conversion topology suitable for SST/TIPS application. Three-phase DAB topology offers advantage of high power density, smoother transformer current, smaller HV device stress. The TIPS is a MV Grid interface [11, 33] based on 15 kV SiC IGBTs (from CREE Inc.). It is rated to interface 13.8 kV MV Grid to 480 V low voltage (LV) Grid. It utilizes a three-phase DAB in the intermediate dc-dc stage, switching at 10 kHz to step down a front-end converter regulated 22 kV dc bus to 800 V dc for LV side conversion. The three-phase DAB offers advantages of a relatively smaller dc capacitor and higher magnetic utilization as compared to a single-phase DAB of the same rating [34]. The bidirectional galvanically-isolated DAB dc-dc converter was initially proposed in [19, 20] is widely used for high-power, HF dc-dc conversion. It has advantages of high power-density, isolation, bidirectional capability, modular and simple structure [35]. The DAB is often utilized as the intermediate dc-dc isolation stage of a grid interface SST. The SST uses ac-dc, isolated dc-dc and dc-ac stages for interfacing the grids. A complex Y:Y/Δ three-phase DAB has been proposed for 22 kV dc to 800 V dc at 100 kW application earlier in [36] and shown in Fig. 2.5. The main reason for using this topology is to share the 100 kW rated load between two secondary converters for reliability and higher efficiency [37]. The reason for Y/Δ connection is to improve the primary-converter current THD for d-q current control. The d-q control is useful to provide an internal current control protection and also to improve the system dynamics by decoupling the second order system poles [38]. The DAB is a high power density isolated dc-dc converter suited as an important component for MV renewable energy integration system [19, 20]. It is turn-on ZVS soft switched converter providing dc voltage transformation and isolation. The control simplicity and higher MTBF reliability requirements make a single phase Dual Active Half Bridge (DAHB) popular over other DAB topologies as it requires fewer switches [39]. However it has the disadvantages of relatively higher ripple voltage and lower power density compared to a three-phase DAB [34]. The DAB may lose the ZVS at light loads due to small freewheeling current during complementary switch turn-off. The 15 kV SiC IGBT has considerable parasitic capacitance especially below punch-through and also its dv/dt is made relatively lower (30 kV/μs) with higher gate resistance to avoid EMI problems in this region [40]. Therefore a dead-time in the range of 3.8 μs is kept. The DAB has to be operated in zero voltage switching (ZVS) to help improve the HV device efficiency and EMI issue. The DAB topology offers ZVS for the switching devices. The switching losses are low also due to partial soft-switching turn-off contributed by device parasitic capacitances.

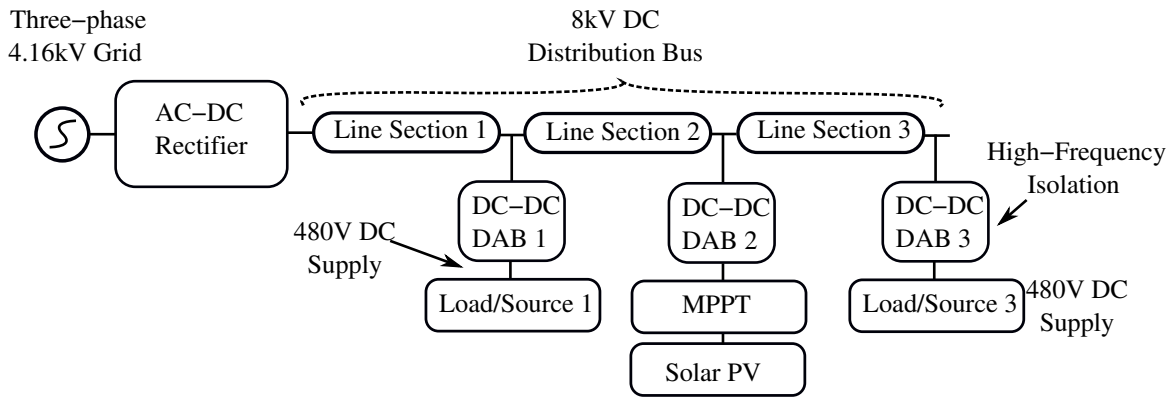


Figure 1.6: Implemented dc micro-grid

1.2.3 DC micro-grid

The medium-voltage (MV) dc micro-grid has been getting very popular for data-centers, offshore wind and navy ship applications. The advantage of dc micro-grids are mainly elimination of bulky lower-frequency ac-ac transformers and simple integration of renewable sources such as PV system [24]. This migration is partially enabled by the recent development of wide band gap semiconductor devices switching at higher speed, higher voltage and temperature. This grid level is also compatible for MV drives in applications such as steel mills etc. This grid interface needs a dc bus in the range of 7-8kV. Therefore the experimental setup developed as part of TIPS project can be used as a testbed for MV dc micro-grid as shown in Fig. 1.6. As the isolation is often required in power system transformer applications for protection and fault detection. This is accomplished by compact HF transformer of the DAB.

1.3 Research Contribution

The contribution of this dissertation is the experimental validation of HV SiC devices in simpler non-cascaded topology for MV dc-dc power conversion application using DAB. The main advantage of HV SiC devices is the higher chip and converter power-density. These SiC devices have increased the individual modular voltage. These modules can result in MMC with fewer cells downsizing the complexity. The 15kV SiC IGBT developed by CREE Inc. has enabled non-cascaded MV DAB for higher power levels. The MV blocking on a single chip is enabled by punch-through (PT) technology however, the dv/dt above PT voltage level can be as high as 110kV/µs [41]. This high dv/dt interacts with module parasitics and MV transformer parasitics causing spikes in current that in turn results in increased switching losses [42, 43] and EMI related problems like control malfunctioning [44]. This can even result in spurious gate-driver tripping of the MV converters. Slowing down dv/dt using higher gate-

resistance may not be optimum from efficiency perspective. Additionally for the SiC IGBT, the dv/dt can be loosely controlled above PT level [40]. This requires for the MV side of the DAB to always operate in ZVS since the dv/dt appearing due to natural commutation through anti-parallel diode is much lower [45]. This reduces switching losses as well as the EMI [42].

However the device parasitics combined with transformer parasitics might cause non-ZVS operation in DAB due to duty control, dead-time, ringing and dv/dt current spike. A practical 100 kW DAB HF transformer has significant parasitics which generate ringing in the MV device currents. This may trigger false shoot through protection and may generate EMI issue. The non-ZVS operation causes poor efficiency and EMI. Therefore transformer must be respecified from these two inputs and common-mode (CM) filters must be used as transformer cap can not be reduced entirely. The three-phase Y:Y/Δ DAB offers advantage of reduced device-stress, lower step-voltage at transformer, high power-density and smaller dc capacitor. It draws dominantly sinusoidal current at the transformer primary without multi-pulse PWM or resonant components [46], suitable for d-q current control. It also transfers three times power with one extra leg in contrast to single-phase DAB. The d-q control is also possible due to sinusoidal nature of DAB HF current offering better control. Other solutions are ZVS ensuring d-q controls and negative current measurement with IMGD, HV filter design, series compensation, series injection with snubbering. The last two solutions are studied with a simple DAB topology.

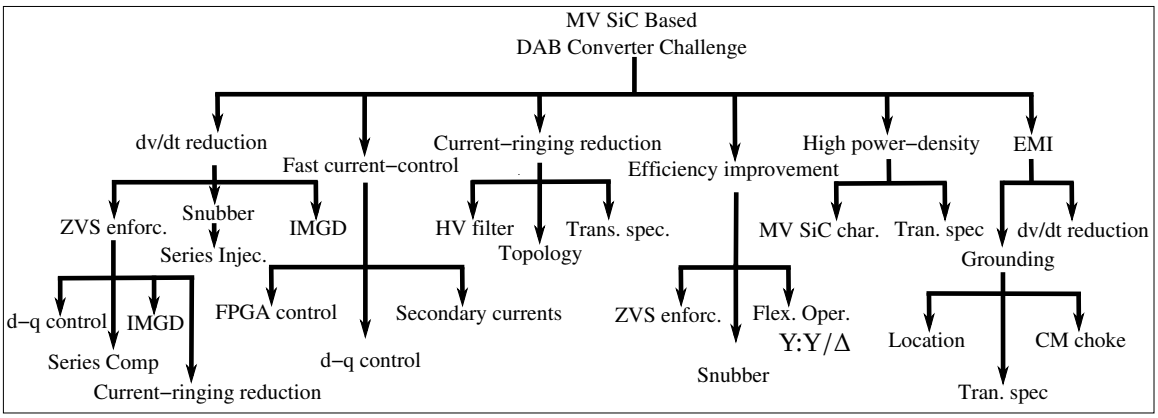


Figure 1.7: HV SiC based DAB problem chart

During the design and development of this HV SiC based DAB, some specific problems had to be solved as shown in Fig. 1.7. They are listed as follows. The challenges are 1. dv/dt reduction using a. ZVS enforcement using i. d-q control, ii. series compensation, iii. IMGD, iv. current-ringing reduction, b. snubber using i. series injection, c. IMGD, 2. fast current control using a. FPGA control, b. d-q, c. secondary currents, 3. current ringing reduction using a. HV side filter, b. topology selection with zero period, c. transformer specification, 4. efficiency improvement in wide load range using a. ZVS enforce-

ment, b. snubber, c. flexible Y:Y/Δ mode, 5. High power density achievement using a. HV SiC devices driven MV-HF transformer due to good thermal conduction and high operating temperature, b. compact transformer requiring smaller L_m and smaller number of turns, 6. EMI reduction using a. grounding using i. proper ground location, ii. transformer specification with smaller inter-winding capacitance, iii. CM current reduction using choke, b. dv/dt reduction. Finally it can be concluded in terms of topology selected, transformer specification, controls, additional controls helped solve different listed problems. Due to CM and dv/dt windings need more separation, so research needed in AFEC inductor and DAB transformer parasitics.

1.4 Dissertation Outline

The flow-chart describing the organization of the dissertation is shown in Fig. 1.8. It starts from study of different secondary side variant three-phase DAB topologies for TIPS application. It goes through transformer specification, its characterization, DAB modeling & control, MV hardware development, ZVS considerations, flexible operations and common-mode considerations. The all condition ZVS operation of the MV SiC converter is the most important requirement for optimum design and performance of the MV DAB. Apart from the methods used for the Y:Y/Δ topology, some other methods are proposed which have been studied on a simpler DAB topology but can be extended to the Y:Y/Δ as well. These methods are covered through series compensated DAB, series enabled snubber operation and intelligent gate-driver chapters. The dissertation concludes with a comparison between 15 kV SiC IGBT and 15 kV SiC MOSFET for the above application. This dissertation is organized using following chapters.

Chapter 2 evaluates different MV NPC based three-phase topologies and justifies the selection of the Y:Y/Δ DAB topology based on simulations [37]. The composite three-phase topology and d-q control [36] is selected to address some issues faced with a practical MV-HF transformer. It also evaluates the topology on a low-voltage experimental prototype setup for operation and control.

In chapter 3, the MV-HF transformer specification is generated based on the DAB simulations considering parasitics, LV setup results and simulations for minimum reactive power [47]. The HF transformer, after design optimization and matching with the intermediate simulations is built by external agency. Additional required inductors are also specified considering design parameters from the MV-HF transformer.

Chapter 4 presents MV-HF transformer measurement and spice simulations to synthesize an equivalent circuit [48] which is useful to emulate the actual HV operation in the simulation. The simulation predicts ringing and EMI problem in the HV operation and thus the control algorithm is modified [49]. A model consisting of parasitic parameters of the transformer is also studied to predict any effect on the control and ZVS operation. The HV side external filters are designed and built to minimize the parasitic ringing in the topology.

Chapter 5 covers the simplified modeling of the three-phase DAB and its control design study using

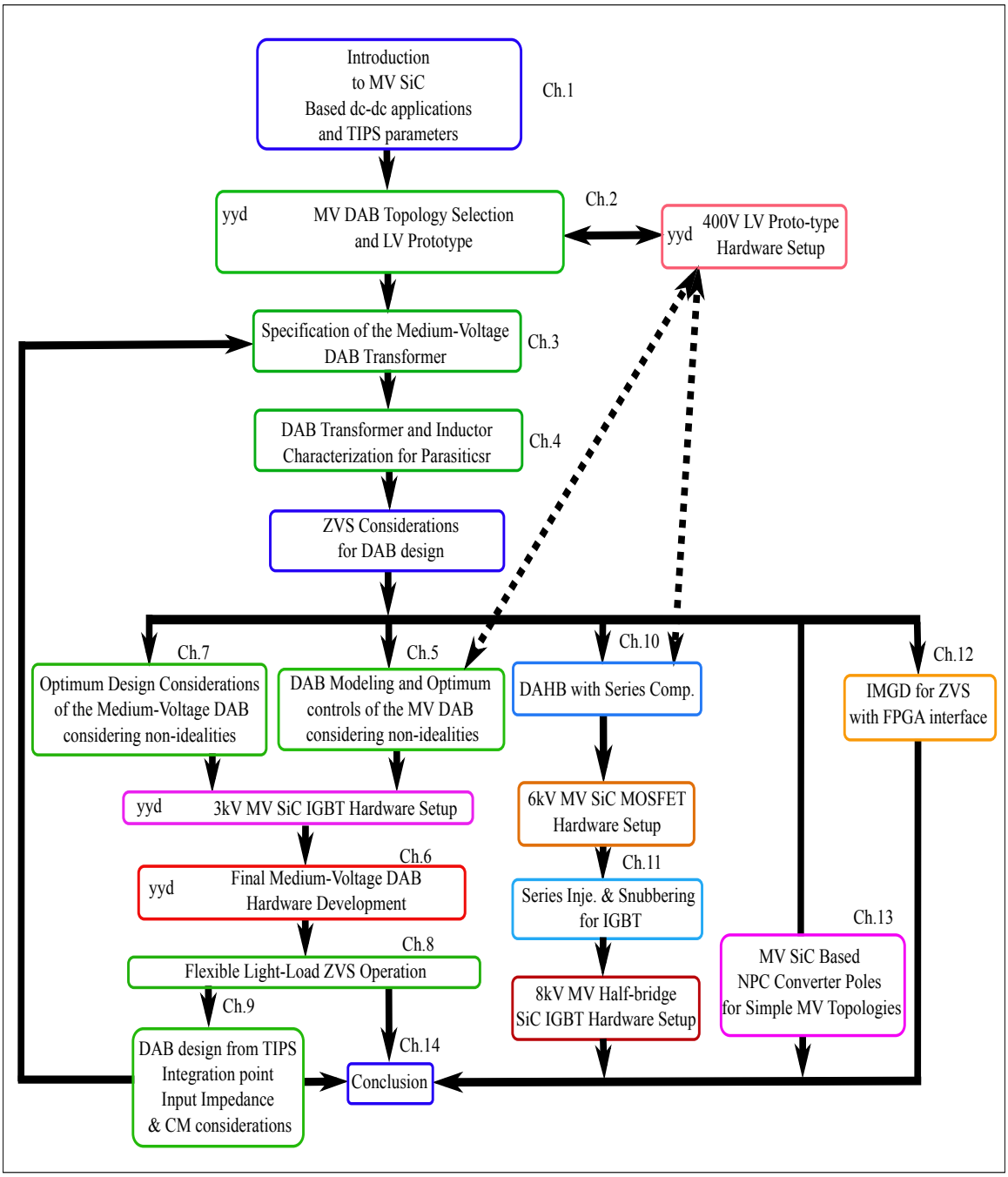


Figure 1.8: Dissertation outline

d-q transformation based DAB control for ZVS enforcement. The development of control hardware based on FPGA and ultra-fast ADCs is presented. The control is validated on a LV hardware prototype for testing the transients, implementation full d-q and effect of parasitics. The 3kV MV results are shown for steady-state with just voltage control.

Chapter 6 describes the medium-voltage hardware development for the demonstration of TIPS DAB section. It highlights important components such as gate-driver, NPC converter pole and their validation with experimental results. The MV DAB final setup is shown with explanation of wiring and transformer arrangements and their verification.

Chapter 7 presents the study of the optimum design of the MV DAB for ZVS considerations. The ZVS range is affected by parasitics, duty-ratio reduction for three level operation of HV converter, dead time of the switching devices. The SiC IGBT (HV device) used in the topology is under research and hence the device parameters such as gate resistance, dead time, blanking time are also actively under trial [41] according to the system parasitics. So the optimum operation of the converter is a challenging problem. The MV DAB extensive experimental results are provided for different conditions to validate the claim.

The Y:Y/Δ topology can also be operated flexibly as presented in chapter 8. For light-load where ZVS is difficult to maintain, one of the secondary converters can be turned-off. The efficiency is calculated based on Matlab-Plecs simulation using actual switching data of the devices. The effectiveness of maintaining ZVS is also highlighted. It has been validated with 3kV experimental results.

Chapter 9 presents the TIPS cascaded effect interaction between AFEC and DAB control systems using impedance comparison. It then presents common-mode (CM) passive filter design for TIPS system. As the HV oil insulation and high power-density requirement force the transformer to posses considerably high mutual capacitance. Combined with HV and high dv/dt, there can be large EMI currents flowing through the transformers, in case the output is grounded for safety similar to bearing currents in converter fed induction motor [50]. The TIPS schematics equivalent circuit is drawn similar to [51, 52] and simple network is solved and CM chokes are designed and developed such as to limit the CM currents to a acceptable small value. The TIPS integration, after implementing the impedance analysis directed control tuning and few grounding/shielding/EMI choke solutions, has been validated at 8kV dc bus and 4.16kV ac three-phase grid.

Chapter 10 presents a a simple modified single phase DAB topology based on same 15kV SiC IGBT and 1200V SiC MOSFET for the same voltage rating as TIPS which can be scaled to higher power rating that is the motivation behind using IGBTs as compared to MOSFETs. It also evaluates d-q control derived from the composite topology in chapter 3 to compare with the selected three-phase topology. It also presents a method to extend the ZVS towards light load and even with voltage ratio deviation in the DAB. For the simplified DAB topology, it only needs a fractional rating series transformer excited by fractional current rating low cost secondary switches. It has been validated with 6kV experimental results.

Chapter 11 presents an extension to the ZVS extension of the series injection mode and even accommodating snubber across the IGBTs which solves EMI issue without increasing losses and actually helping more soft-switching for loss-less operation. This has been implemented on the hardware at 3kV.

Chapter 12 presents IMGD for implementing ZVS with FPGA interface. For ensuring ZVS in the MV converter, given the current ringing and nonlinear device capacitance, it is needed to measure the device current lag angle as well as negative current-magnitude at the turn-on instant. This can be done using the IMGD which has onboard sensing, ADC and fast optical communication interfacing to the FPGA based main control board. This method can be extended to the MV high-power DAB for optimum and reliable operation. Only the IMGD functionality of optically sending the fast signal, has been validated with 5kV high side experimental results under EMI conditions.

Chapter 13 presents 15kV SiC MOSFET based NPC poles and their experimental validation for intended DAB switching as MV dc-dc converter. The DAB operates the converter in ZVS turn-on soft-switching mode, therefore MV device conduction loss is important comparison parameter. The two devices are briefly compared in this chapter for MV DAB suitability. The NPC pole has been validated with 10kV experimental results under different conditions for showing benefit of ZVS as compared to 15kV SiC IGBT.

Chapter 14 summarizes the dissertation. The contribution is in terms of topology selection, transformer specification using sensitivity analysis, transformer characterization, controls and hardware development, optimum-operation simulations and experiments, ZVS extension techniques, intelligent gate-driver development with fast optical data capability, grounding and common-mode filter design for TIPS and TIPS integration. There is a tread-off with the parasitics of transformer for smooth ZVS operation with cost & size. The controls and external HV side filters attenuate the current spike and ringing arising due to the parasitics.

Chapter 2

MV DAB Topology Selection and LV Prototype

2.1 Introduction

The dual active bridge (DAB) is a bidirectional isolated dc-dc converter. It has been proposed in [19, 18] as single and three phase topologies for high-power applications. The three-phase DAB utilizes reduced size output dc capacitor and offers higher power density as compared to the single-phase DAB for same ratings [19, 18]. This chapter proposes three different three-phase Dual Active Bridge (DAB) topologies employing 15 kV Si-IGBT based three-level converter at the high-voltage side and 1200 V SiC-MOSFET based converters in three different arrangements at the low-voltage side. A comparative evaluation of the topologies is presented in terms of switch VA rating, harmonics, P-δ curve, losses, reliability and magnetics[53] . The three topologies are Y:Y/Δ, Y:Y and Y:Open windings with three single-phase converters.

This chapter then describes the Y:Y/Δ three phase DAB topology selected for the TIPS application in detail. This topology introduced in [36], saves MV side device voltage rating as well as the current rating since the maximum step-voltage applied across transformer MV winding, responsible for current ringing is smaller, $V_{dc}/3$. It has three level converters connected at the MV side of the MF 10 kHz DAB transformer and paralleled two-level converters in Y/Δ at the secondary. They are switched in six step mode. The three-level converters connected at the high-voltage side in each topology are operated with 30° zero-period. The proposed arrangements at low-voltage side of the medium-frequency (MF) transformer help to reduce dominant harmonic currents. Thus harmonic-free currents in the high frequency link transformer are achieved without switching to multi-pulse PWM. The dominantly sinusoidal DAB transformer currents can be utilized for inner d-q current control. Other advantages might be higher magnetic utilization [18] and smaller magneto-striction problems as the flux is dominantly sinusoidal but its verification is beyond the scope of this dissertation. This chapter also presents a new d-q control

of DAB. This chapter also presents different transformer arrangements for implementation of the three-phase transformer based topology. The proposed topology and controls are validated with simulation results followed by LV prototype experimental results.

2.2 Why single-phase DAB topology is difficult for TIPS

With AFEC output dc at 22 kV, and even with three-level NPC converter at MV side of transformer, 11 kV step voltage will be applied across transformer with high dv/dt contributed by SiC devices, making switches to carry peaky currents at step transition. Three-phase three-level converter at MV side causes the step voltage of 7500 V. The Y/Δ connections at LV side combined with this MV side converter cause much smooth current through transformer close to sine-wave. This provides opportunity for d-q control rather than peak-current control. Single phase DAB has triangular flux shape while three phase DAB has smoother flux shape [34, 54].

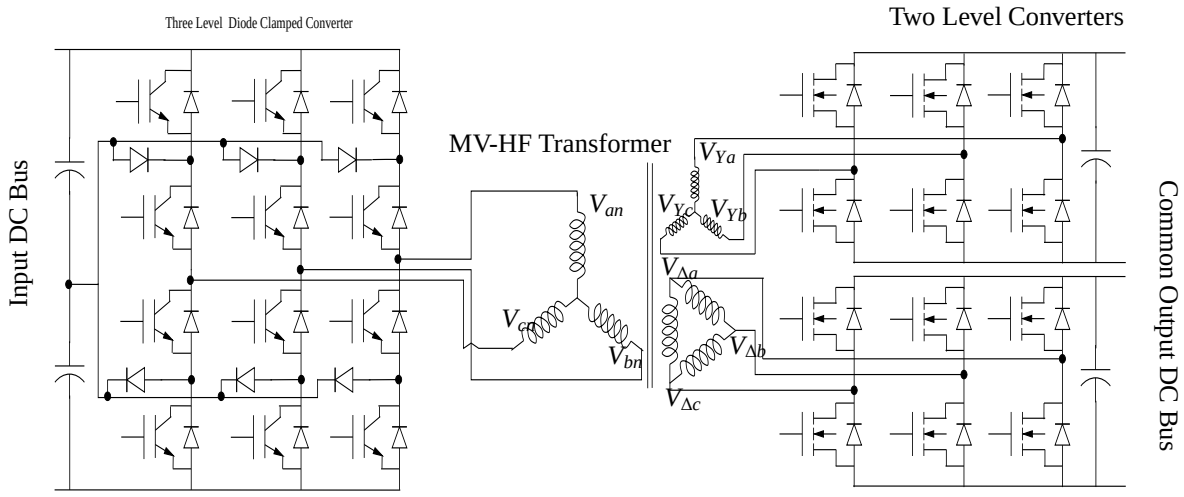
2.3 Description of Proposed DAB Power Topologies

2.3.1 Topology: 1. Y(3-level):Y/Δ(2-level)

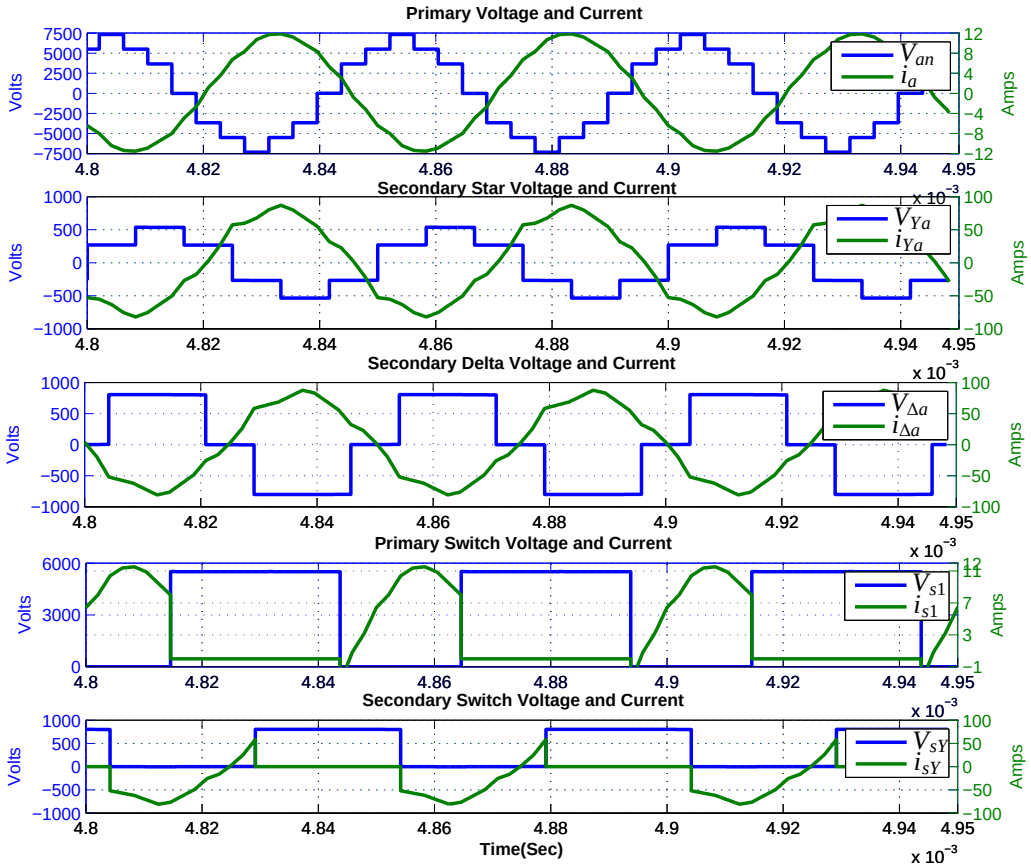
In this topology a three-level NPC converter is connected to primary star-winding and 2 two-level converters are connected to two secondary windings in star-delta manner as shown in Fig. 2.1(a). The two-level converters are in 30° phase-shift so that they produce synchronous fundamental flux. In this process higher order odd-harmonics are canceled-out due to 150° and 210° phase difference. The EMF produced due to two-level converters has small higher order odd-harmonics and interacts with three-level side star winding to generate a cleaner fundamental current between primary star and the converter system [36]. However the two-level sides have dominant $5th$, $7th$ and derivative harmonics in the circulating current between them. Fig. 2.1(b) shows the simulation result for this topology which consists of R-phase voltages and currents along with transformer-EMF. The circulating current between Y and Δ exists for all phase-angles with respect to primary and is limited by the leakage inductances of the two sides. Therefore the leakage inductances cannot be designed small, as is desired.

2.3.2 Topology: 2. Y(3-level):Y(3-level)

This topology uses a 2 three-phase star-windings connected to three-level NPC converters each side. There is no dominant high-order odd harmonic current in this case as both sides are fed from three-level NPC converters with 30° zero-enforcing. Though it also uses 24 power-devices as in Topology 1, the transformer is less complex and device voltage ratings are smaller for same dc bus voltage. Fig. 2.2(a) shows the schematic of diode-clamped three-level converters tied to three-phase transformer in star-connection. To compensate the volt-second lost due to smaller duty-cycle compared to two-level con-

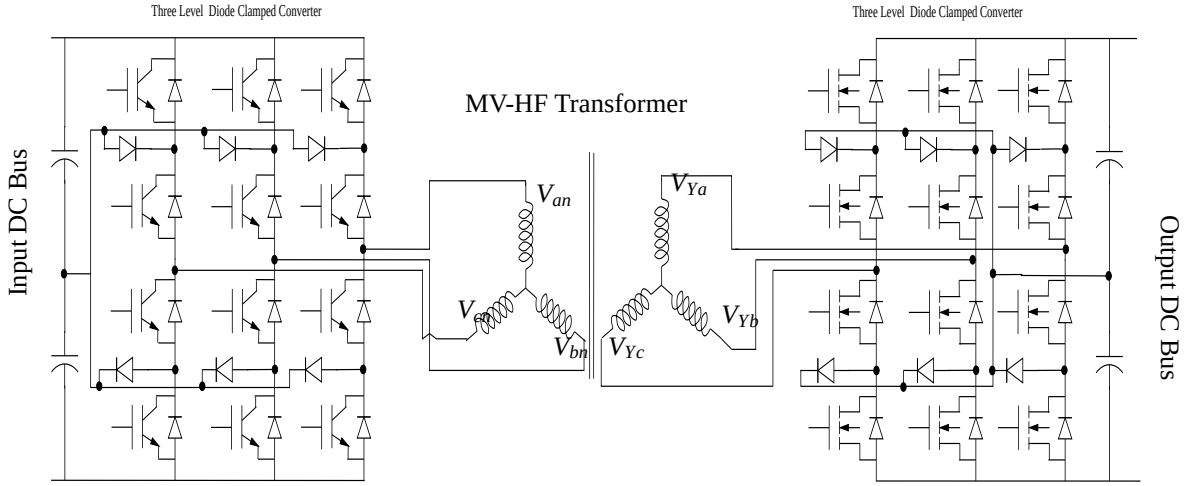


(a) Circuit diagram for Y:Y/Δ DAB

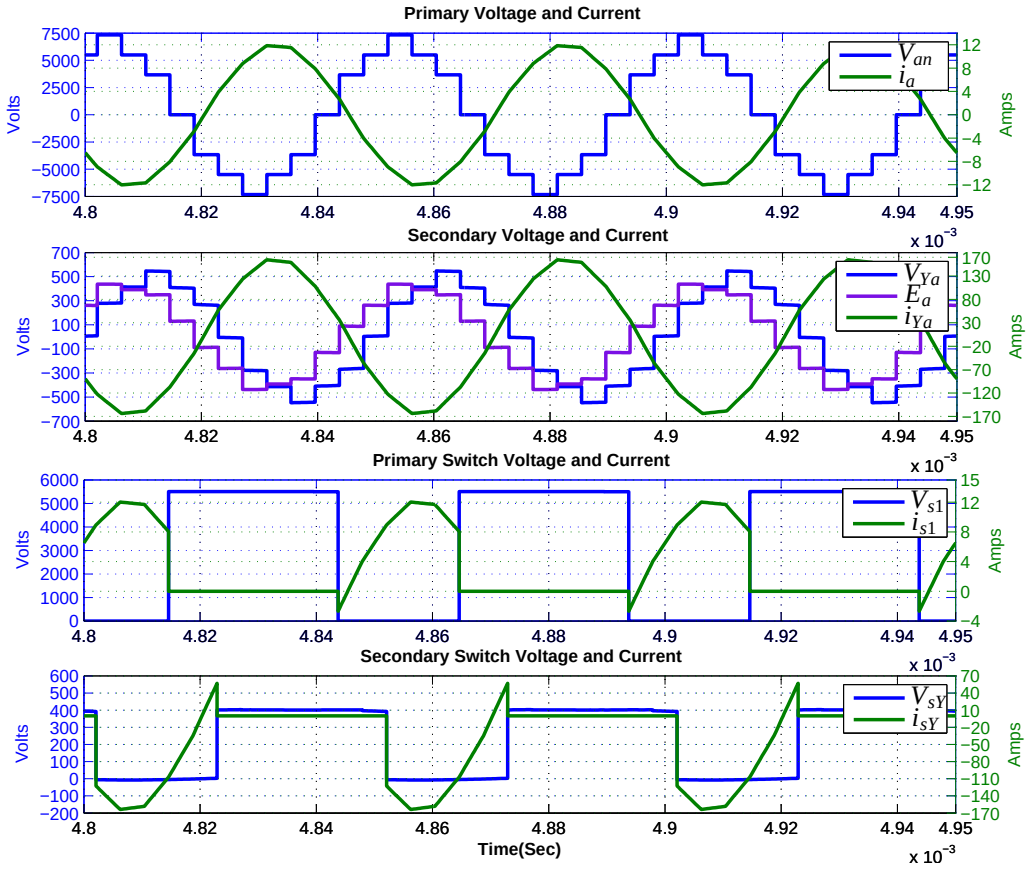


(b) Steady-state simulation topology-1

Figure 2.1: Y:Y/Δ three-level DAB



(a) Circuit diagram for Y:Y three-level DAB



(b) Steady-state simulation topology-2

Figure 2.2: Y:Y three-level DAB three-level DAB

verter, the dc bus voltage is increased to 841 V for all three-level converters equivalent to 800 V for two-level converters. When compared to the first topology leakage inductance of the secondary side has to be half in this and next topology to make them equivalent to two paralleled converters. Fig. 2.2(b) shows the simulation result at Full load of 100 kW for this topology. Transformer currents are same and have less harmonics due to identical three-level NPC converters on both sides.It also shows the top device voltage and current waveforms which are in ZVS confirmed by the negative current at turn ON.

2.3.3 Topology: 3. Y(3-level):Open windings with three single-phase converters

The primary-side remains same but secondary-side is open, 3 single-phase windings fed by single-phase full-bridges as shown in Fig. 2.3(a). Transformer is almost similar to topology-3 with only difference that secondary phase windings are not inter-connected here to form a neutral and switching device requirement is again same. As the transformer turn-ratio is kept 1:1, the secondary dc bus is kept at 400 V for the full-bridge. Fig. 2.3(b) shows the simulation result for this topology which consists of R-phase voltages and currents along with device voltage and current at single-phase bridge which again works in ZVS.

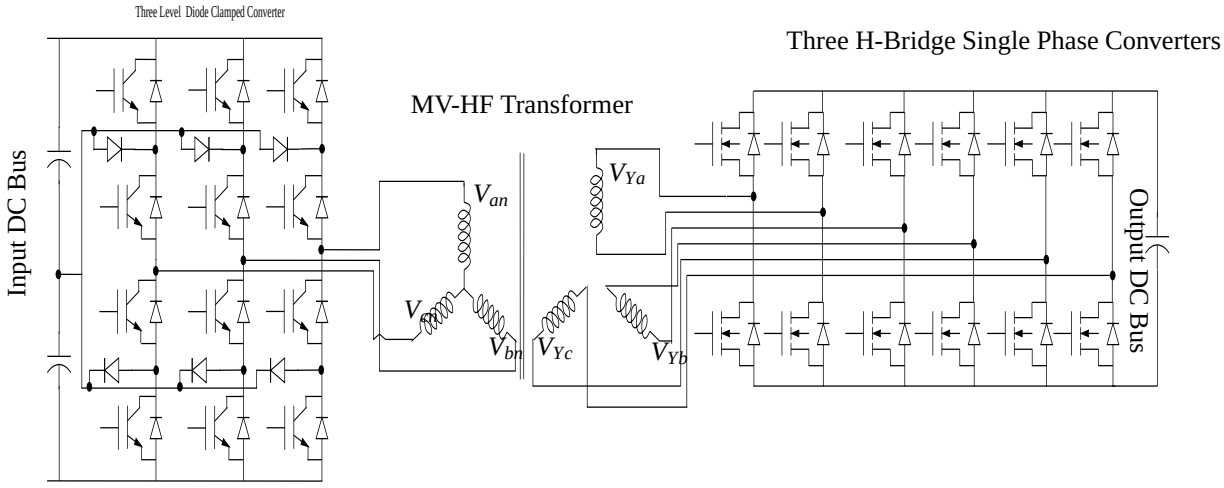
2.4 Comparison of Topologies

2.4.1 Simulation Performance

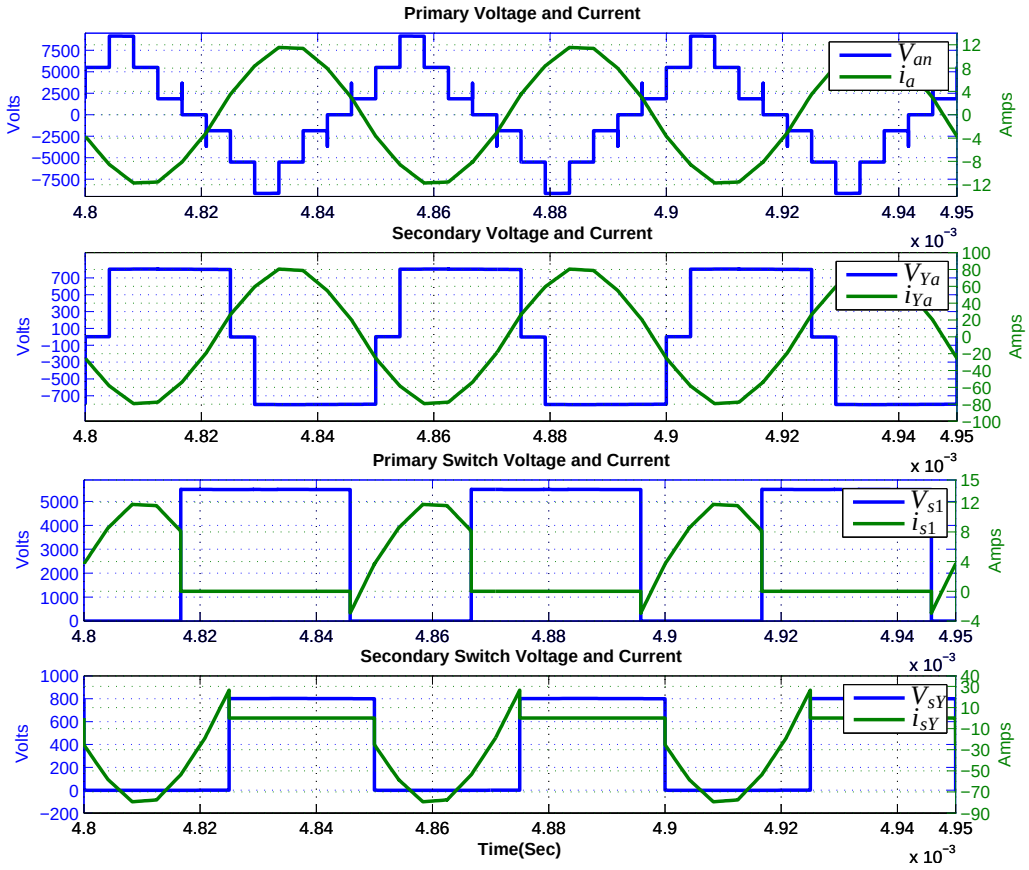
Fig. 2.4 shows the P-δ curve for the three topologies and compares them with a hypothetical sinusoidal curve. It confirms that three-phase DAB compared to single-phase DAB has nearly sinusoidal P-δ curve with small deviations at the peak power. As the curves resemble to that of a two-machine conventional power system, the sinusoidal nature will make the system under-damped oscillatory. The high-frequency transformer winding resistances will provide damping. Table 2.1 shows the comparison

Table 2.1: Topology comparison based on device loss data simulation for 11 kV-800 V, 100 kW MV-DAB Demonstration using 15 kV/20 A, 2 μm buffer SiC IGBTs on MV

Topology	Y-Y/Δ		$Y-Y$		Y:1ϕ	
	Primary	Secondary	Primary	Secondary	Primary	Secondary
Power Loss	*Cond.* = 217.8 W *Switch.* = 715.2 W	*Cond.* = 376.7 W *Switch.* = 236.4 W	*Cond.* = 232.4 W *Switch.* = 726 W	*Cond.* = 1161.4 W *Switch.* = 256.2 W	*Cond.* = 224 W *Switch.* = 740.4 W	*Cond.* = 515.4 W *Switch.* = 106.1 W
	Primary	Secondary	Primary	Secondary	Primary	Secondary
Device Rating	V_{pk} = 5500 V I_{pk} = 11.6 A V_{rms} = 4200 V I_{rms} = 5.71 A	V_{pk} = 800 V I_{pk} = 81 A V_{rms} = 566.6 V I_{rms} = 38.24 A	V_{pk} = 5500 V I_{pk} = 12 A V_{rms} = 4201 V I_{rms} = 5.99 A	V_{pk} = 400 V I_{pk} = 164 A V_{rms} = 306 V I_{rms} = 81.24 A	V_{pk} = 5500 V I_{pk} = 11.6 A V_{rms} = 4200 V I_{rms} = 5.81 A	V_{pk} = 800 V I_{pk} = 78.6 A V_{rms} = 566.6 V I_{rms} = 39.21 A
	Primary	Secondary	Primary	Secondary	Primary	Secondary
THD	V = 16.86% I = 2.15%	V = 30.96% I = 7.41%	V = 16.86% I = 1.65%	V = 16.48% I = 1.65%	V = 16.86% I = 1.6%	V = 31.83% I = 1.6%
Efficiency	98.5%		97.66%		98.41%	



(a) Circuit diagram for Y:open windings three-level DAB



(b) Steady-state simulation topology-3

Figure 2.3: Y:open windings three-level DAB

at 100 kW based on simulation. Converter secondary side losses are low because power is transferred from primary to secondary and the anti parallel SiC-diodes carry current in secondary side which offer small voltage drops in conduction. These results are based on the data sheet of 1200 V/100 A SiC MOSFET (package 4804, M.S.K.) used at secondary sides and 15 kV/20 A 2 µm buffer IGBTs at primary side of all topologies for the prototype. Topology 1 seems to give higher efficiency because secondary current is split in two paralleled converters and hence smaller conduction losses. Switching losses are small compared to conduction losses as the SiC devices are very fast [55, 41, 56]. In terms of harmonics, the second topology offers the best prospects compared to other two as the three-level NPC converters are configured to generate minimum voltage harmonics. This is desirable for d-q control, as the sinusoidal currents transform in to dc quantities which is easy to control by simple PI based compensator. Also the voltage-ratings are half for three-level converters but other practical challenges arise such as capacitor voltage imbalance and ripple at full load condition. The MV primary side of all three topologies is same both in structure and performance and also suitable from the view of practical limitation of device blocking voltage capability. At secondary side in topology 2 and 3, two MOSFETs conduct in series all the time for each phase, resulting increased conduction losses [57]. For 1200 V MOSFET, topology 1 gives balanced performance in terms of switching and conduction losses. Topology 1 has two secondary circuits independent of each other, so it is failure safe. In contrast, other two topologies will fail if any switch fails.

2.4.2 Magnetics Requirement

Transformer and Inductors are important component of the Dual Active Bridge. All the above three-phase topologies can be built using three single-phase transformers as three-phase high-frequency cores are not commercially available. Using single-phase transformer in topology 3, introduces triplen harmonics voltage at MV-phase to transformer-neutral voltage,but it doesn't distort the primary current as there is no connection between transformer neutral and converter neutral. Topology 2 and 3 have simpler structure in terms of number of windings, Topology 1 requires three winding transformer for Y and Δ sides. Core losses for three topologies are not too different from each-other and depend on the particular design. Topology 2 applies better waveforms on both sides of transformer and is expected to have slightly lower core-loss. Topology 1 applies triplen voltages in nearly opposite polarity at two secondary windings so there is circulating current only limited by leakage and external inductance. Topology 3 applies triplen voltage at secondary that also generates triplen magnetizing current and the triplen voltage is generated in primary as well. Inductor requirement is lower for topology 2 and 3 but more and larger value for topology 1 as there are circulating currents at secondary side. One 35 kVA single-phase transformer-design for topology 1 has been estimated to dissipate 108 W and 322 W for nano-crystalline and ferrite cores respectively at 10 kHz. Transformer losses further decrease the efficiency but they are nearly same for all three topologies.

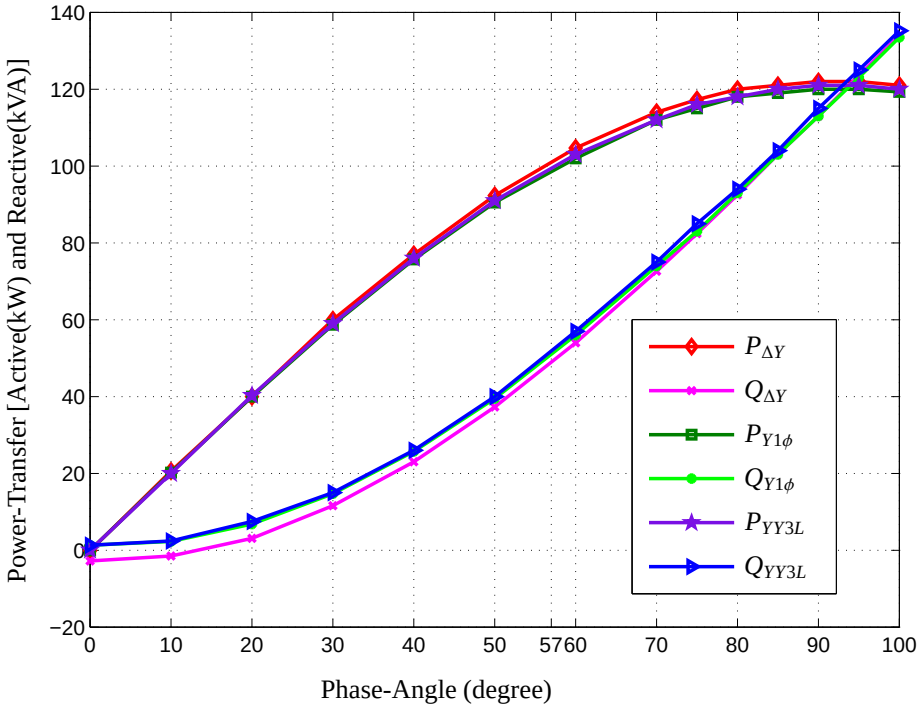


Figure 2.4: Power-angle curve for three topologies

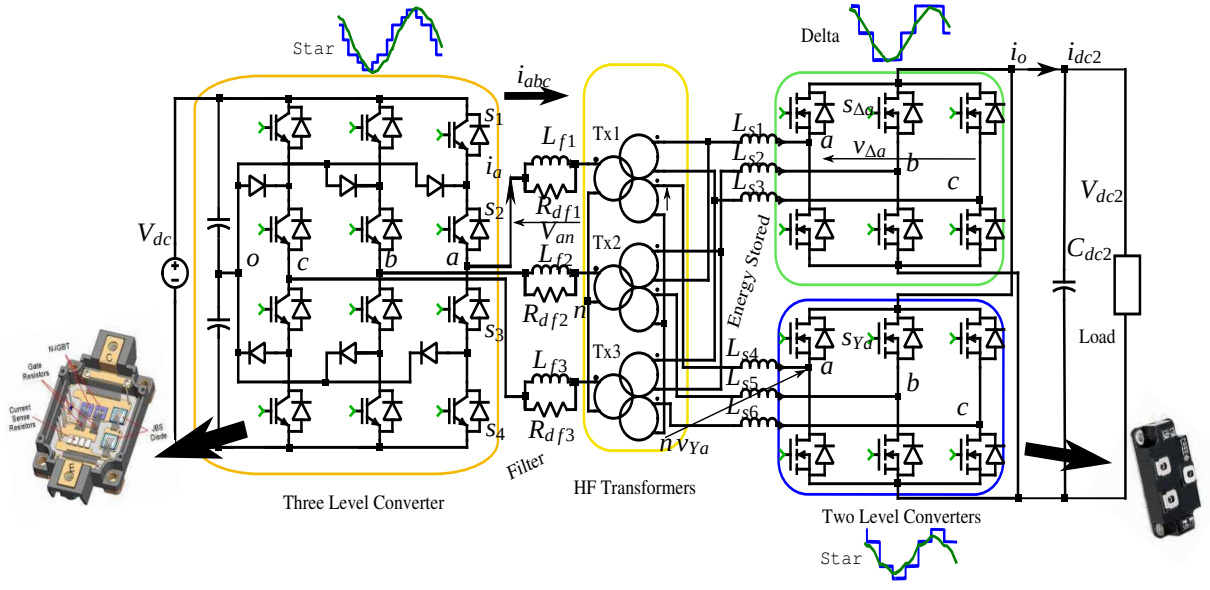


Figure 2.5: Schematic of the three-phase Y:Y/Δ DABC

2.4.3 Advantages of the Topology

Fig. 2.7 shows the *a* phase converter voltage and current of each side at 2 kW simulation. As expected primary current is predominantly sinusoidal. The secondary currents have dominant 5^{th}, 7^{th} and derivative harmonics circulating between them which exists for any DAB angle. The maximum step voltage applied on transformer primary is near $\frac{V_{dc1}}{3}$, which would be $\frac{V_{dc1}}{2}$ for single-phase DAB with three-level half bridge converter and $\frac{2V_{dc1}}{3}$ for two-level $Y : Y$ three-phase converter. This topology has been compared with derivative three-phase DAB topologies in [53]. The two converters at the secondary make this topology improve the reliability.

2.5 Detailed Description of the Y:Y/Δ

The proposed DAB power topology as shown in Fig. 2.5, consists of three phase three winding Y:Y/Δ MF link transformer connected to a three level converter at the MV star side and two phase shifted two-level converters at the LV Y/Δ sides. The dc bus of the three level converter and two-level converters are kept at 22 kV and 800 V respectively. The MV three level converter has been built with 15 kV SiC IGBTs (CREE). The low voltage two-level converters are be built with 1200 V/100 A SiC MOSFET (4804, M.S.Kennedy Corp.). The crux of the proposed DAB structure is to reduce dominant lower-order harmonics (5^{th} and 7^{th}) in the MF link transformer. The three level converter offers lower voltage stress to MV semiconductor devices and helps to synthesize a smoother waveform compared to a single two-level converter [58]. Therefore the three level converter is switched with 15° zero period in its pole voltages. It ensures significant reduction of $n = (6m \pm 1)$ harmonics from its pole voltage; where$m = 1, 3, 5, ..$ [59, 60]. The triplen harmonics in the line current are absent because of Y connection. The 18° zero period in pole voltages results in total cancellation of 5^{th} order harmonics and 13° zero period in pole voltages results in total cancellation of 7^{th} order harmonics, so a middle angle is preferred. This can be analyzed from Eq. 2.1. At steady-state both the two-level converters are switched simultaneously.

2.5.1 Current Shaping in the Y:Y/Δ Three-Phase DAB

The primary converter is operated in six-step with 41% duty-ratio of top switch to generate minimum of 5^{th} and 7^{th} harmonics. Eq. (2.1) shows the n^{th} harmonic primary phase voltage V_{an} with $\gamma = 15°$ zero-period which is equivalent to 41% duty-ratio. The two-level converters are in 30° phase-shift so that they produce synchronous fundamental-flux in the transformer. The DAB topology comprises of a three-level neutral-point clamped (NPC) converter on the MV side which feeds the star configured primary-windings of three single-phase MV-HF transformers. The star-connected three-level converter is operated in six-step with 41.7% duty ratio of outer switches to generate a minimum of 5^{th}, 7^{th} harmonics in the V_{ao}. As shown in (2.1), the n^{th} harmonic primary voltage V_{ao} is function of the zero-period (γ). Fig. 2.9 shows the total harmonic distortion (THD) of the V_{ao} with respect to γ. The γ is 15° which

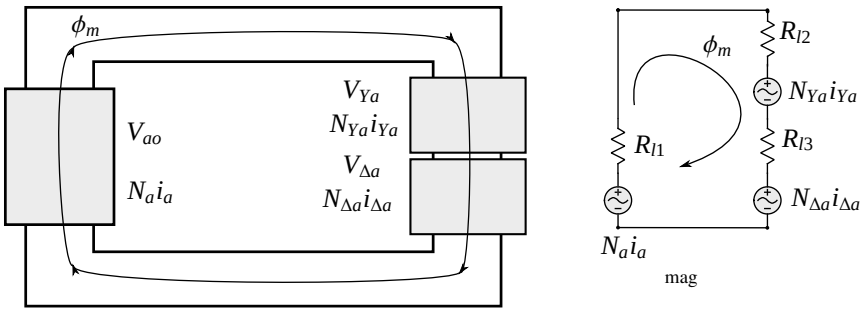


Figure 2.6: Cancellation of higher order harmonics

Table 2.2: Rated DAB parameters for TIPS application

Parameters	**Value[Units]**
Input dc Voltage	22 kV
Output dc Voltage	800 V
Input side Duty-Ratio	41% nominal
Primary External Inductors	440 μH
Secondary External Inductors	80 μH
Real Power Transfer	100 kW
Switching-frequency	10 kHz

is equivalent to 41.7% D. The THD is smallest for this γ value. Eq. 2.2 and 2.3 depict that 5^{th} and 7^{th} harmonics of Y and Δ sides will add in phase-opposition. As shown in Fig. 2.6, the MMF in the core, contributed by secondary higher order odd-harmonics ($6m \pm 1$) tend to be in opposite direction due to the opposite voltage phases ($30[6n \pm 1] \pm 30, \forall n = 1, 3, 5..$) [61]. They cannot cause any flux. Hence these harmonic voltages do not excite transformer EMF and there are harmonic currents flowing between secondary converters. The predominantly fundamental DAB primary and resultant transformer EMF interact to generate a cleaner current through the primary winding.

$$V_{n^{an}} = \frac{4V_{DC}}{2n\pi} \cos[n\gamma] \sin[n\omega t] \tag{2.1}$$

$$V_{n^{Ya}} = \frac{4V_{dc2}}{2n\pi} \sin[n\omega t] \tag{2.2}$$

$$V_{n^{\Delta a}} = \sqrt{3}\frac{4V_{dc2}}{2n\pi} \sin n[\omega t + \frac{\pi}{6}] \forall n = 1, 3, 5.. \tag{2.3}$$

Table 2.2 shows the rated TIPS parameters of the simulation study. Fig. 2.7 shows for a phase voltage and current simulation-waveforms at 100 kW real power transfer. V_{an} is the phase to neutral voltage waveform for a three-level converter with $\gamma = 15°$ zero period to eliminate most of 5^{th} and 7^{th} har-

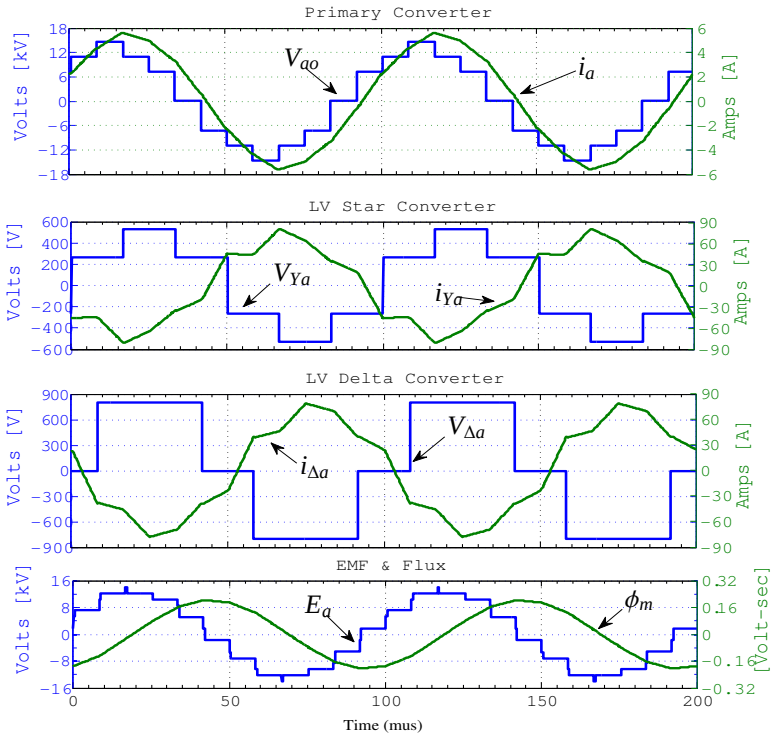


Figure 2.7: Three phase DAB 100 kW steady state simulation

monics. V_{Ya} and $V_{\Delta a}$ are secondary side phase to neutral and phase to phase voltages for Y and Δ sides respectively. They add up in the transformer core and produce resultant voltage in the secondary side. Ideally the series leakage inductance is assumed to be evenly distributed between primary and secondary sides. E_a is phase to neutral voltage waveform due to resultant flux created by the interaction of primary and secondary imposed voltage. It is measured after the leakage inductance on three level side in the model. It has 12 levels of discrete voltages contributed by $Y : Y/\Delta$ individual voltage waveforms. As expected primary current is predominantly sinusoidal while secondary currents have dominant 5^{th}, 7^{th} and derivative harmonics circulating between them which exists for all DAB angles. Maximum step voltage applied on transformer primary is near $\frac{V_{dc1}}{3}$, which would be $\frac{V_{dc1}}{2}$ for single phase DAB with three level half bridge converter and $\frac{2V_{dc1}}{3}$ for two-level Y:Y three phase converter. This topology has been compared with derivative three phase DAB topologies in [37] and is more efficient with the given SiC device loss data. Fig. 2.8 shows the frequency spectrum of the waveforms corresponding to Fig. 2.7. Fig. 2.9 shows a THD plot with zero state clamping angle of the NPC converter. The total harmonic distortion of the waveforms is shown in Table 2.3 which shows that 15° does better and relative harmonic content is provided in Table 2.4. It can be seen that 11^{th} and 13^{th} harmonics don't reduce, that is because for 30° phase shift they add in same phase. For this topology most of the power transfer is carried by fundamental current due to absence of dominant harmonic components. The phase shift between primary and

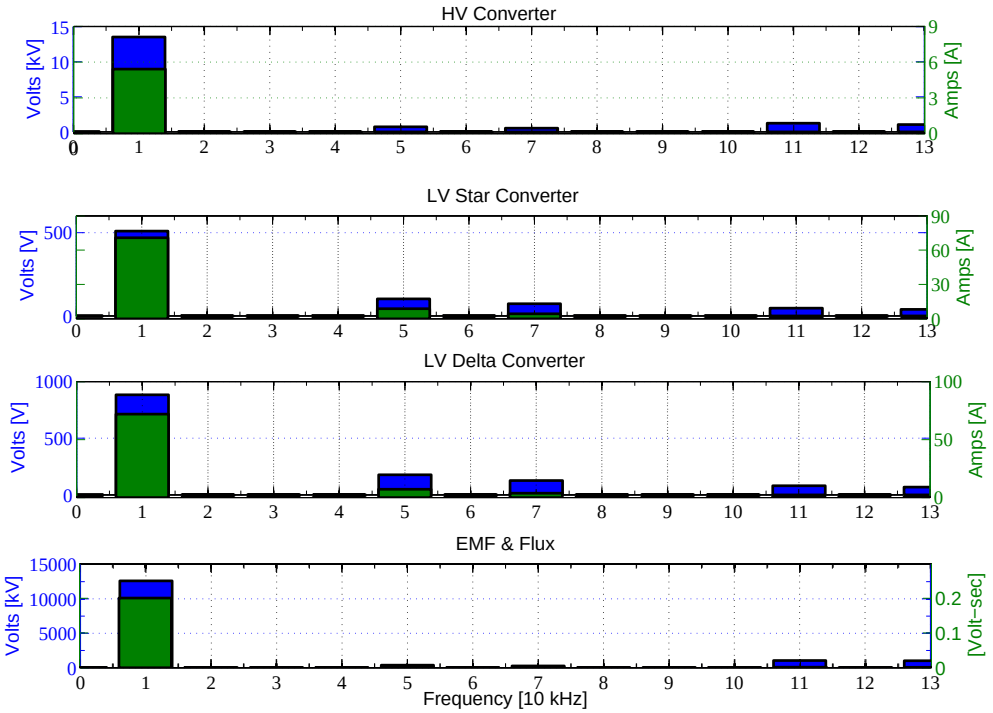


Figure 2.8: FFT of three phase DAB steady state simulation

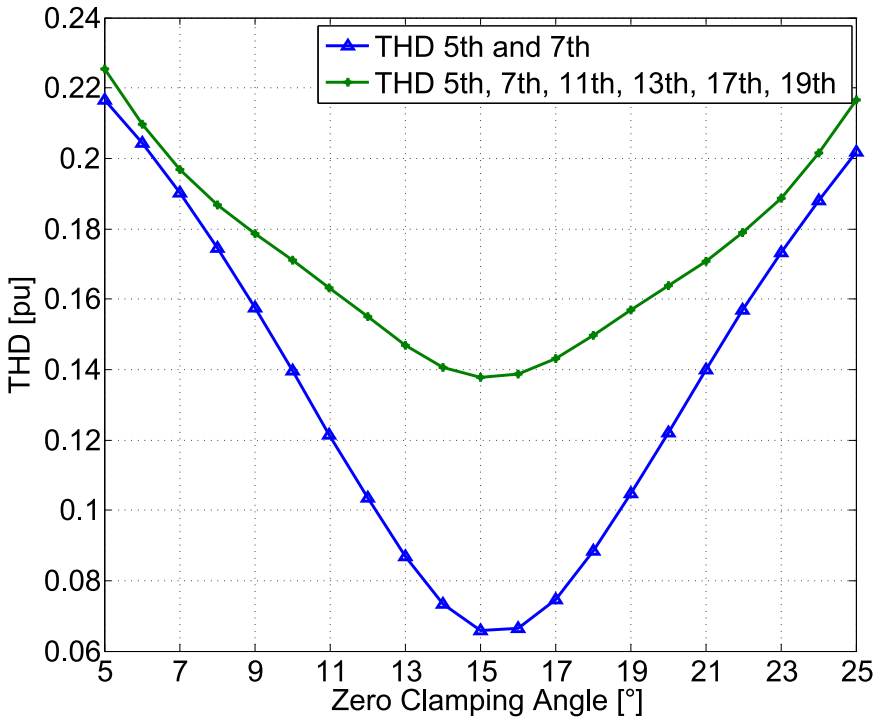


Figure 2.9: Three-level converter duty ratio selection (γ)

Table 2.3: Total harmonic distortion for the simulation result

Zero Period	V_{an}	V_{Ya}	$V_{\Delta a}$	E_a	i_a
THD 15°	17.24%	31.75%	30.15%	16.44%	1.97%
THD 18°	17.53%	31.75%	30.15%	14.28%	2.06%

Table 2.4: Relative harmonic content of the simulation result

Frequency	5^{th}	7^{th}	11^{th}	13^{th}	17^{th}	19^{th}
V_{an}	5.36%	3.83%	9.09%	7.69%	1.57%	1.41%
V_{Ya}	20.00%	14.29%	9.09%	7.69%	5.88%	5.26%
$V_{\Delta a}$	20.00%	14.29%	9.09%	7.69%	5.88%	5.26%
E_a	1.38%	0.94%	8.87%	8.04%	0.31%	0.42%
i_a	1.36%	0.69%	1.04%	0.44%	0.12%	0.09%

secondary side voltage set, transfers power as shown in Eq. 2.4. The operating conditions such as rated phase shift ϕ_0 and coupling inductance $L_s = |Z_{tie}|\cos(\theta)$ are designed to consider the reactive power flow characteristics of DAB in [47].

2.6 Operation of the Three-Phase Y:Y/Δ DAB

As shown in Fig. 2.5, there are two two-level MOSFET LV converters to share the current for 100 kW. If they are connected in Y and Δ manner then they can be operated in 30° phase-shift so that they produce synchronous fundamental-flux in the transformer. In this process, the higher order harmonics of the established transformer EMF are canceled. Fig. 2.7 shows the 100 kW ideal simulation for a phase converter voltages and currents for each of star MV, delta LV and star LV sides. It does not consider the parasitics or the t_d's. As expected, the MV side current is predominantly sinusoidal but the LV converters carry circulating current. The maximum step voltage on primary is around 7500 V ($V_{dc}/3$).

2.7 Description of Proposed d-q Control

For three-phase DAB, the controller generates pulses for reference converter and shifts the pulses of other side converter for power transfer, so it is easy to use the reference generated sine and cosine signal to convert the nearly sinusoidal currents into d-q currents and feedback to inner current-control loop. There will be an outer-voltage loop to control the dc bus voltage to the desired level. The three phase DAB currents are nearly sinusoidal in the discussed topology due to three level converter at the primary side and Y/Δ configuration at the secondary side. This fact can be utilized to transform three phase ac currents into synchronously rotating d-q frame with respect to secondary voltage vector which is produced as reference in the controller board. Fig. 2.10 shows the basic control block diagram for

operation of the DAB. The low voltage side two-level converters are operated with fixed six step gate pulses each and a 30° phase shift to match the two fundamental voltages after transformer connection. The three level converter is operated with phase shift modulator that shifts the phase angle of generated voltage with respect to the two-level side fundamental voltage. The q-axis current is the real component

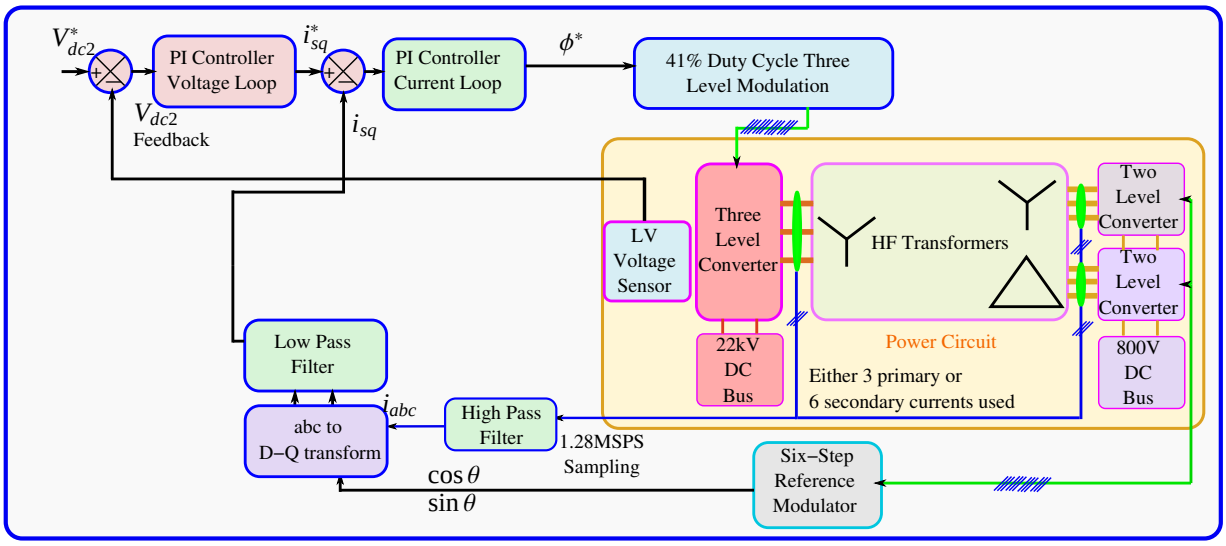


Figure 2.10: Control block diagram for Y:Y/Δ three-phase DAB

of current responsible for real power flow. So this can be used as inner current control feedback after smoothing it with a low pass filter. The d-axis current depends on phase angle between primary and secondary sides and it represents reactive component. It is assumed that the per unit fundamental voltage magnitudes of the two sides are same. The phase-shift between primary and secondary voltage, transfers real power as shown in (2.4). The operating-conditions such as rated phase-shift ϕ_0 and coupling inductance $L_s = |Z_{tie}|\cos(\theta)$ are designed to consider the reactive power-flow characteristics of DAB in [47].

$$P = \frac{v_s v_r}{|Z_{tie}|}\cos[\theta - \phi] - \frac{v_r^2}{|Z_{tie}|}\cos[\theta] \tag{2.4}$$

$$\frac{\partial P}{\partial \phi} = \frac{v_s v_r}{|Z_{tie}|}\sin[\theta - \phi_0] \tag{2.5}$$

$$Q = \frac{v_s v_r}{|Z_{tie}|}\sin[\phi - \theta] - \frac{v_r^2}{|Z_{tie}|}\sin[\theta] \tag{2.6}$$

(2.5) shows the linearized gain of the DAB system. (2.6) shows the reactive power. The basic DAB operation relation analogous to power system is shown in Eq. 2.4. This is basically non-linear equation but for a considerable value of angle, this can be linearized around a steady state operating point (ϕ_0)

in Eq. 2.5. The Y:Y/Δ DAB MV converter is analogous to a vector controlled AFEC tied to the grid. The two-level secondary converters are switched with fixed six step and hence can be considered as the grid. The three level converter can be switched with variable duty ratio and a phase relative to secondary hence can be considered as the AFEC. The MV-HF transformer leakage inductance and external inductors form the tie inductor. The in-phase component of inductor current transfers real power to the secondary output. For control simulation, low-voltage side has one resistive-load of 100 kW. A

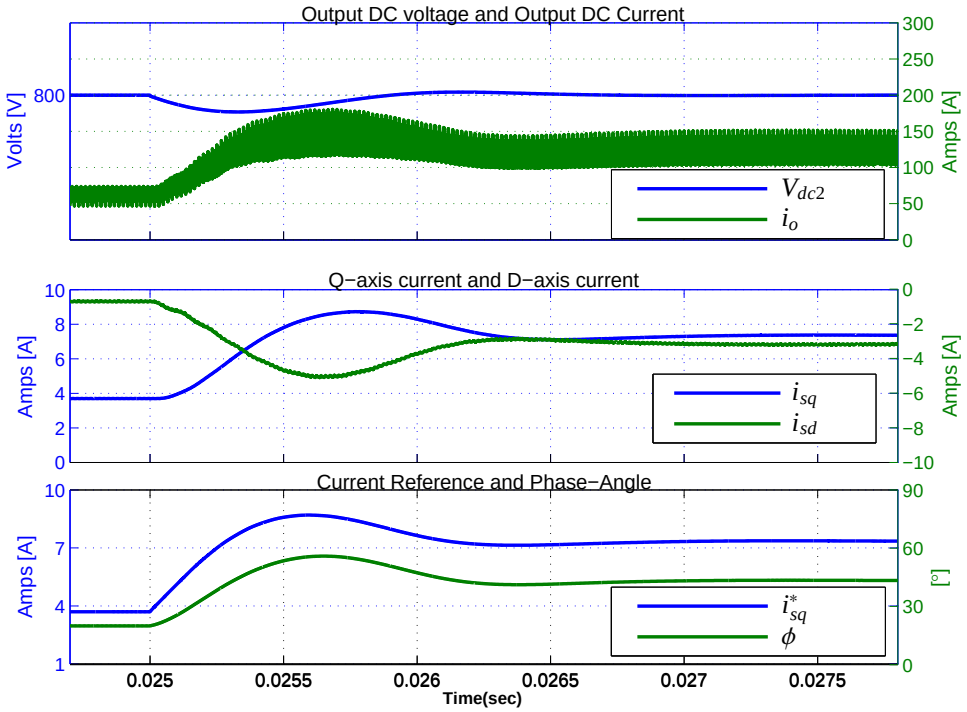
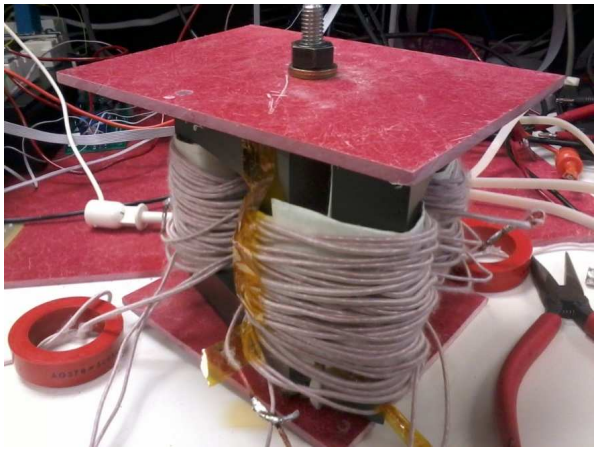


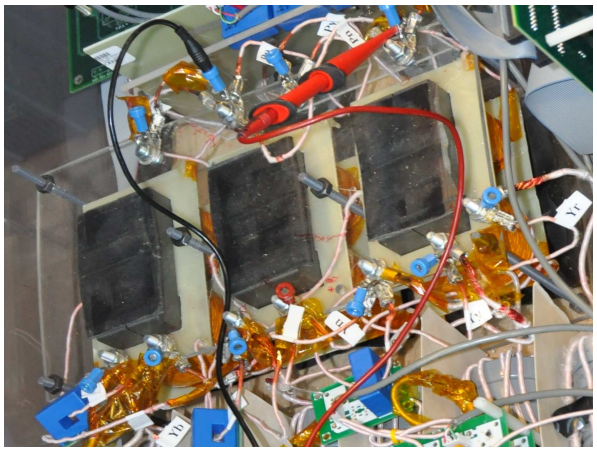
Figure 2.11: Transient response using d-q mode control

transient is simulated by turning-on the passive-load at instant 22 ms while keeping set-voltage level at 800 V. There is an internal-current control loop with d-current limit of 10 A as well as an outer-voltage loop with parameters based on DAB model. Fig. 2.11 shows the output voltage, DAB *a* phase current and phase angle control command for the above transient condition. It takes 8 ms for the system to come to next steady-state which also depends on the amount of disturbance. The secondary dc side has one switched resistive loads of 100 kW. A transient is created by turning on resistive load while keeping voltage reference at 800 V. There is an internal current control loop as well as a voltage loop.

(a) Three-Phase 10kHz, 200 V, 2 kW Transformer with E-cores



(b) Three-Phase 10kHz, 200 V, 2 kW Transformer with U-cores



(c) Three-Phase 10kHz, 400 V, 4 kW Transformer with three single-phase transformers

Figure 2.12: Different transformer arrangements for three-phase DAB

Table 2.5: Parameters of the LV experimental setup

Parameters	**Value[Units]**
Input dc Voltage	200 V
Output dc Voltage	200 V
Input side Duty Cycle	41%*nominal*
Effective Leakage Inductance	400 µH
Real Power Transfer	2 kW
Switching frequency	10 kHz

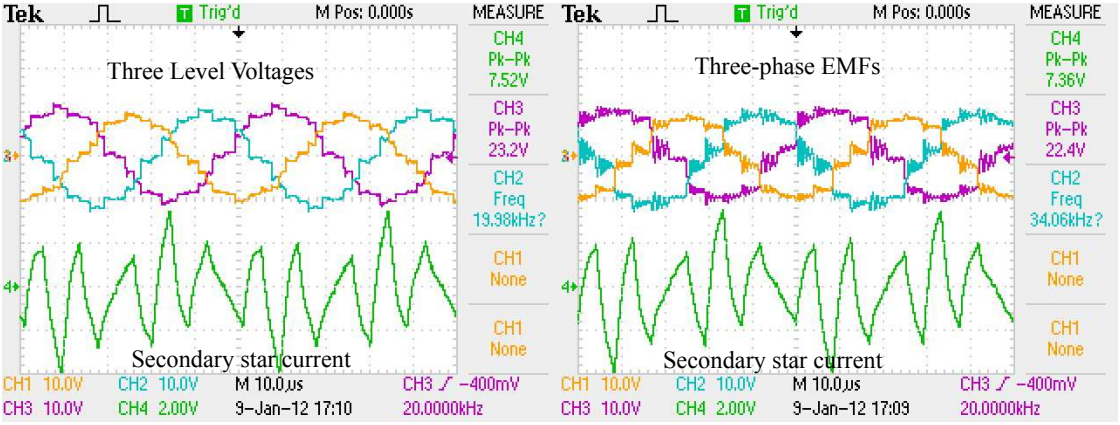


Figure 2.13: LV transformer excitation for Y:Y/Δ DAB topology

2.8 LV Prototype Transformer Arrangements

In the LV prototype setup different transformer arrangements have been tried out. A snap of the transformer is shown in Fig. 2.12. For the Y:Y/Δ topology, a three-phase, three-winding transformer operating at 10kHz is required. These prototype transformers have turn ratio of $1:1:\sqrt{3}$ rated for 200 V on primary and 2 kW power. Commercially, ferrite E-cores and U or C-cores are available for such prototype applications. The E-cores are suitable for single-phase shell type structure as there is mismatch in cross-section areas of the three legs. The central limb is twice thicker. It has been used here as shown in Fig. 2.12(a) as a single unit three-phase transformer. But since the reluctance seen by each phase is not symmetric and also all three-phase fluxes do not interact in a balanced symmetric way, the transformer does not work as intended. Fig. 2.12(b) shows a symmetric three-phase arrangement with U-cores that are used to construct a structure like axial transformer so that the legs are symmetric for all three phases. It makes a single package three-phase transformer. This transformer works as intended but the mechanical arrangement and isolation are difficult to pass for a medium-voltage scale-up design. This requires customized cores with symmetric three-limb structure and large window area to provide

enough space for insulating materials and windings. Most important issue is that common-mode excitation has no magnetic path, thus there is no back EMF for such voltage harmonics and the induced current is only limited by leakage/external inductors. Fig. 2.12(c) shows the final symmetric arrangement of three-phase three-winding with three single-phase transformers. It is suitable from isolation and symmetric operation perspective. The leakage inductance is found to be 20μH per side and magnetizing inductance to be 4mH. Therefore 400μH external inductors are added on the secondary side to limit 5^{th} and 7^{th} harmonic currents of Y and Δ sides. On each leg of the transformer an open single turn wire was put to measure the transformer EMF. At common DC bus voltage of 50V, the transformers are excited from primary and secondary converters one at a time. Fig. 2.13 shows the corresponding EMF which resembles to the waveform by three-level side excitation.

2.9 LV Prototype Experimental Results

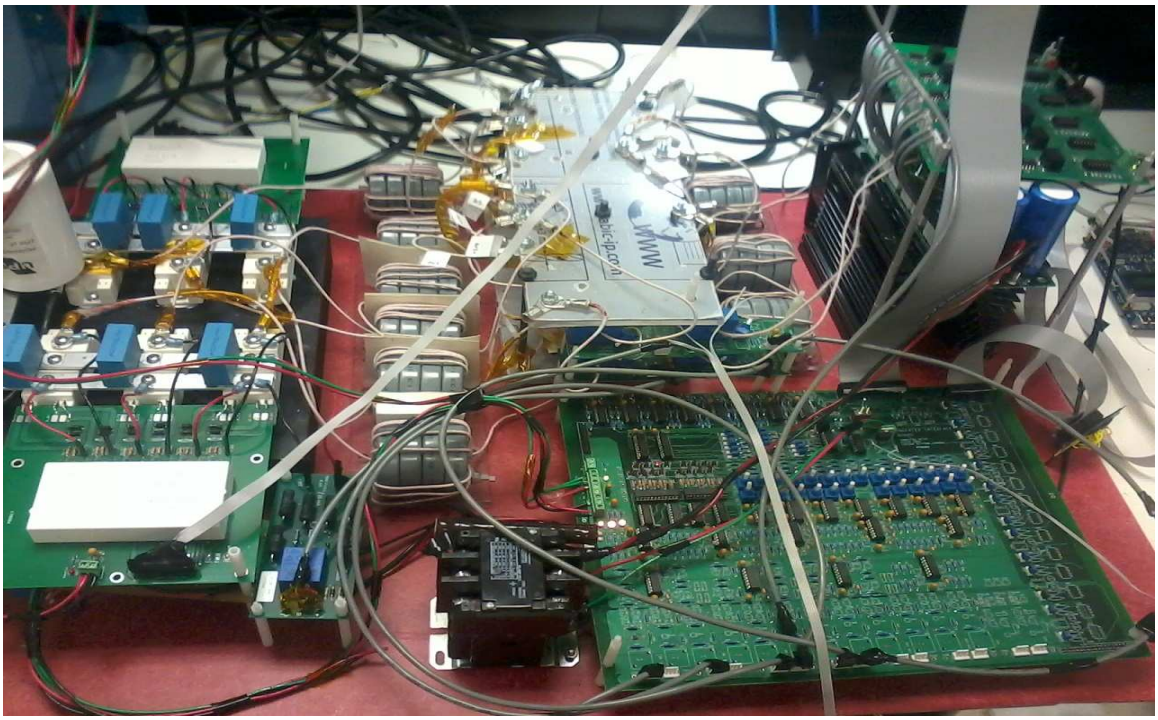


Figure 2.14: LV prototype hardware setup I for Y:Y/Δ DAB topology

Fig. 2.14 shows the LV setup for the experimental validation of the topology. It is important to verify all the control and operation issues that may arise in MV setup. The MV magnetics and converter must be designed after the understanding with LV setup. Table 2.5 shows the parameters of the hardware proto-

type setup study. DAB converter output to input voltage ratio is 1.0 and they can be connected together with same polarity for open loop testing and plotting $P-\phi$ curve. Fig. 2.15 shows the flux current

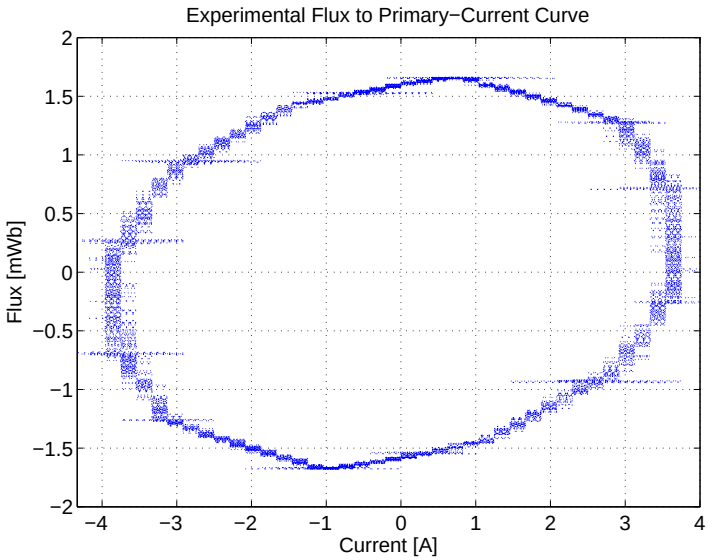


Figure 2.15: Experimental waveforms flux-primary current plot

plot for the experiment. The Y:Y/Δ configuration offers reduced harmonic distortion in the transformer current and offers. Figs. 2.16, 2.17, 2.18 and 2.19 show the steady state experimental waveforms of converter phase voltages and currents for different phase angles(ϕ). It resembles the simulation result and was performed in open loop control with input and output dc buses tied together just as Sumpner's test of transformer.

2.10 Conclusion

The Y-Y/Δ and Y:1ϕ topologies utilize two-level converters at low voltage side and three-level converters at 22 kV side. And the blocking-voltage rating requirement for three-level converter is half in ideal case so only three-level converters are feasible to implement at 22 kV side. For 800 V side two-level converters can be used if required to avoid problems of capacitor voltage imbalance and ripple. These topologies reduce the maximum step voltage subject to transformer minimizing any parasitics caused ringing. The sinusoidal nature of primary current and three-level duty-ratio control makes d-q control suitable ensuring good performance. The Y:Y topology offers the harmonic-less operation desired by control but at the 800 V side they need to carry large currents and if paralleled with another three-level converter,the number of device requirement will be double at the secondary-side. Y:1ϕ and $Y-Y$

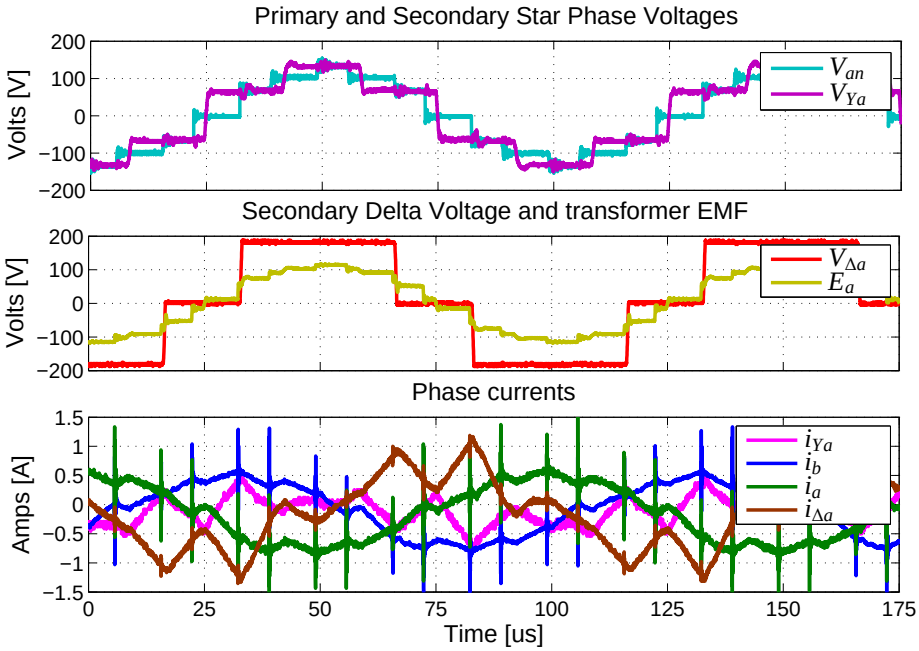


Figure 2.16: Experimental waveforms at 0° phase-angle

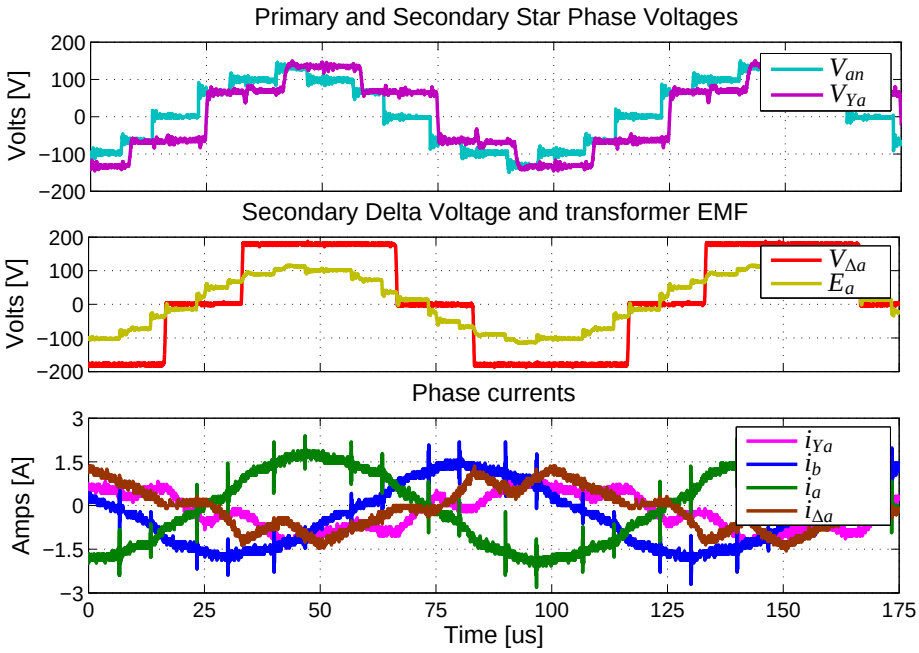


Figure 2.17: Experimental waveforms at 30° phase-angle

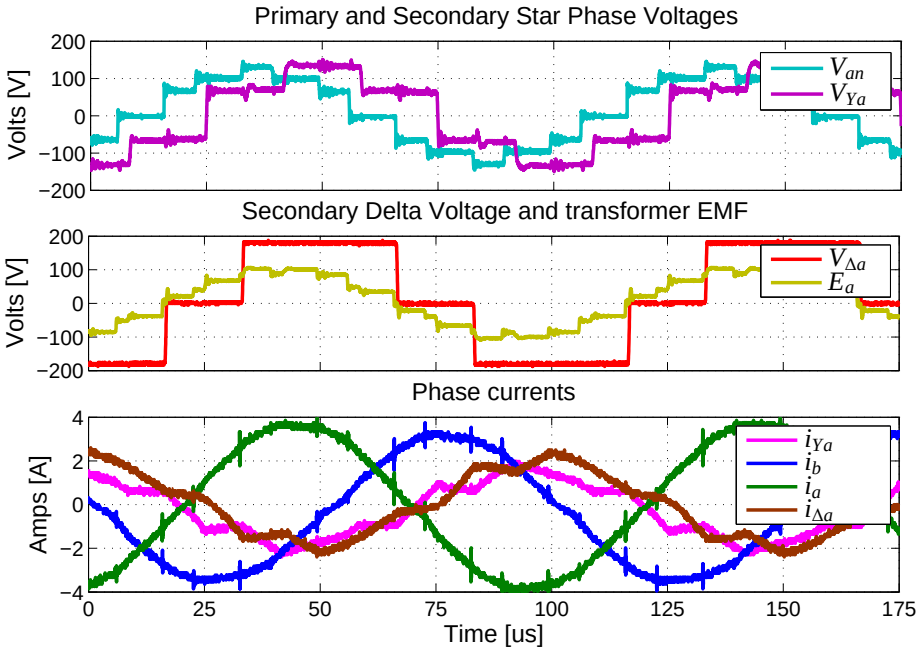


Figure 2.18: Experimental waveforms at 60° phase-angle

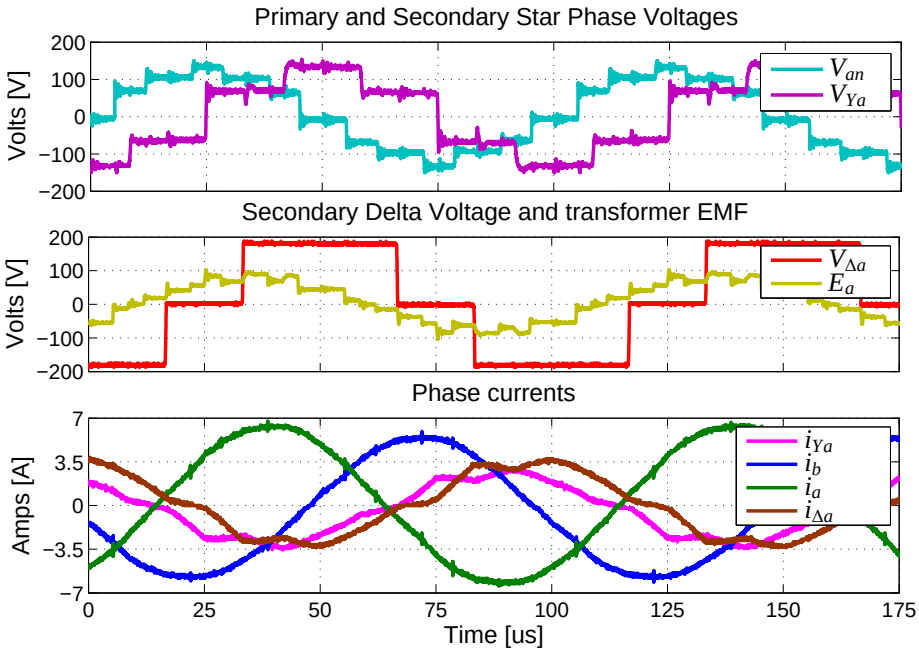


Figure 2.19: Experimental waveforms at 90° phase-angle

topologies have higher conduction losses at secondary as two switches conduct in series and current is higher for Y:Y topology. These topologies also need each switch on secondary side to function and Y:Y/Δ can still work with lower rating if one converter(Y or Δ) at output fails. The selected Y-Y/Δ topology is found to be more efficient with the given SiC device loss data. For the given rated voltage, the three single-phase transformer proves to be a better choice from isolation and also operation perspective. The simulations presented, validate the proposed d-q controls. The open-loop LV hardware results verify the steady-state operation of the proposed DAB.

Chapter 3

Specification of the Medium-Voltage DAB Transformer

3.1 Introduction

The MV DAB design must consider the non-ideal parameters on the top of the basic DAB design [20]. This chapter presents MV-HF transformer's specification. The MV-HF transformer used in the DAB is the compact power-electronic alternative to bulky transformers to provide the isolation between high and low voltage dc link voltages in DAB converters. The design of MV-HF transformer used in DAB stage of such application is very challenging considering the required isolation, size and cost [47].

This chapter first presents an analysis of switching and conduction losses using actual device switching data based simulations on different operating points of three-phase Y:Y/Δ DAB converter leading to an optimum transformer specification. The transformer turn-ratio deviation from nominal, shifts the sharing of reactive power by primary and secondary sides. Equal sharing of reactive power results in lower conduction losses for DAB. But in practice, the device switching and conduction characteristics might shift the optimum efficiency turn-ratio and duty-ratio points considerably. For lab demonstration, the transformer needs to be designed for full TIPS rating of 100 kW but dual voltage modes 11 kV and 22 kV dc DAB operation. Therefore the DAB design considerations and efficiency optimization are presented using simulation study based on the 15 kV SiC IGBT/1200 V SiC MOSFET device actual switching loss data (8 kV, 10 A) for 100 kW, 11 kV-800 V dc DAB operation. A design consideration for three-phase DAB based on reactive power flow has been presented in [47, 62] which compares two combination of primary to secondary turn-ratio for smaller reactive power and concludes that for symmetric DAB system, losses are small if operated at nominal turn-ratio, when Q is minimum for given Power P. In this chapter simulation study has been carried out using Matlab-PLECS tool for two operating power level of 50 kW and 100 kW keeping same transformer leakage inductance at different turn-ratio and duty-ratio.

The main challenges for the design of this transformer are high-voltage isolation, high magnetizing inductance, minimal parasitics (inter and intra winding capacitances), optimum size and cooling arrangement. The design and analysis of high voltage MV-HF transformer has been discussed earlier in [63, 64, 65, 66]. However, these transformers are for voltage much less than 11 kV. Here each single-phase transformer has two sets of secondary windings which can be configured in star delta connection [32]. Such an arrangement has the advantage of having the harmonic currents circulating in the secondary windings only. Based on the specification transformer cores and winding arrangements are selected [67]. The MV-HF transformer preliminary design is based on ideal DAB simulation. The preliminary estimated MV-HF transformer leakage and magnetizing inductances are small and parasitic capacitances are high, therefore sensitivity analysis is presented to reach an optimization. Also external inductors are required to support DAB transfer impedance. The six additional LV inductors can be put for Y and Δ coupling, since they help to reduce 5^{th} and 7^{th} harmonic-currents circulating between star and delta windings in this topology. More inter-turn spacing and mutual winding separation are required to minimize the parasitic capacitance resulting in increased transformer size. Thus the parasitics cannot be kept very low as there is an upper limit on the size since the main motivation of HF operation is to reduce the magnetic size. Therefore as a solution to reduce the current ringing, HV side filter inductors are also specified in this chapter through sensitivity analysis simulations.

3.2 Reactive Power Flow

Fig. 3.1 shows the DAB P, Q-δ plot for the basic magnetics design. The full load DAB ϕ is selected 45° where ideal P/Q is 1.2, keeping in view that a large reactive power results in inflated conduction losses [47]. Also a smaller full-load DAB angle makes the phase control resolution small [68] and results in more distortion in the currents. Thus small full-load DAB angle makes the controllability difficult. Keeping in view the THD of primary current and losses, the phase angle around 25° can be optimum which corresponds to 50 kW for the above converter. The rated parameters for the simulation-study are shown in Table 2.2.

A simulation study has been done with parameters given in Table 3.1 to evaluate the effect of change in primary/secondary turn-ratio of the transformer on efficiency of the practical system. Fig. 3.2 shows reactive power flow from primary and secondary sides to the transformer with different taps while maintaining real power transfer to 100 kW and 50 kW respectively by suitable changing voltage phase angle by converter control. Sum of the reactive power from three converters, is consumed by the leakage inductance and it is lowest for case of 9 kV tap. We can also see that as the primary tap increases, primary current to transformer decreases and secondary currents increase. We can also see that maximum efficiency occurs at 11 kV tap and does not coincide with lowest reactive power flow. For 50 kW simulation, reactive power can go negative as well that is due to fact that voltage phase angle is around 25° and current vector can pass the voltage vectors now after tap change. The turn-ratio effect can also be emu-

Table 3.1: Parameters of the simulation

Quantity	Value[Units]
Input dc Voltage	11 kV
Output dc Voltage	800 V
Input side Duty Cycle	41%*nominal*, (36% − 50%)
Effective Leakage Inductance	42 μH
Real Power Transfer	CaseI: 100 kW, CaseII: 50 kW
Switching frequency	10 kHz

lated by dynamically changing primary side three level duty-ratio, but it can be 50% at maximum and it deteriorates the THD of the primary side current from 2% to 8% and also results in lower efficiency when away from nominal duty-ratio [69].

3.3 DAB Converter Losses

Near nominal turn-ratio DAB converters operate in Zero Voltage Switching (ZVS) at full load. Fig. 3.3 shows the primary and secondary side conduction losses at 10 kHz for two power levels. When tap is changed, DAB current vector moves towards one of the voltage vector and it draws less current from that voltage vector. We can notice a change in associated converter losses as well, for example primary switching losses decrease sharply from left to right while secondary conduction losses increase. Total converter loss which depends not only on reactive power flow but also on used device characteristics, become smallest for around nominal turn-ratio. We know that for MOSFET turn on loss is high and for IGBT turn off loss is high. Fig. 3.4 shows that combined switching loss becomes smallest at 14 kV as the largest part is contributed by top IGBT turn off, but over compensation results in leading current for HV converter and hence turn on loss as well. The middle switch of the three level converter marked as *energy*2 can be made to have zero switching losses that happen when we operate at smaller phase angle and near unity power factor for HV side converter. As switching and conduction losses in this application have opposite requirement for minimum value turn-ratio, total loss still finds nominal point most efficient for 10 kHz. But at 20 kHz, switching loss will double and becomes more dominant and forces the optimum turn-ratio toward minimum switching energy turn-ratio. Fig. 3.5 shows the efficiency of the DAB with different turn-ratio operation. Fig 3.6 shows the switching loss and power as a function of the HV converter duty-cycle. The middle switch of the three-level converter marked as *energy*2 can be made to have zero switching losses that happen when we operate at smaller phase-angle and near unity power-factor for HV side converter. As switching and conduction losses in this application have opposite requirement for minimum value turn-ratio, total loss still finds nominal point most efficient for

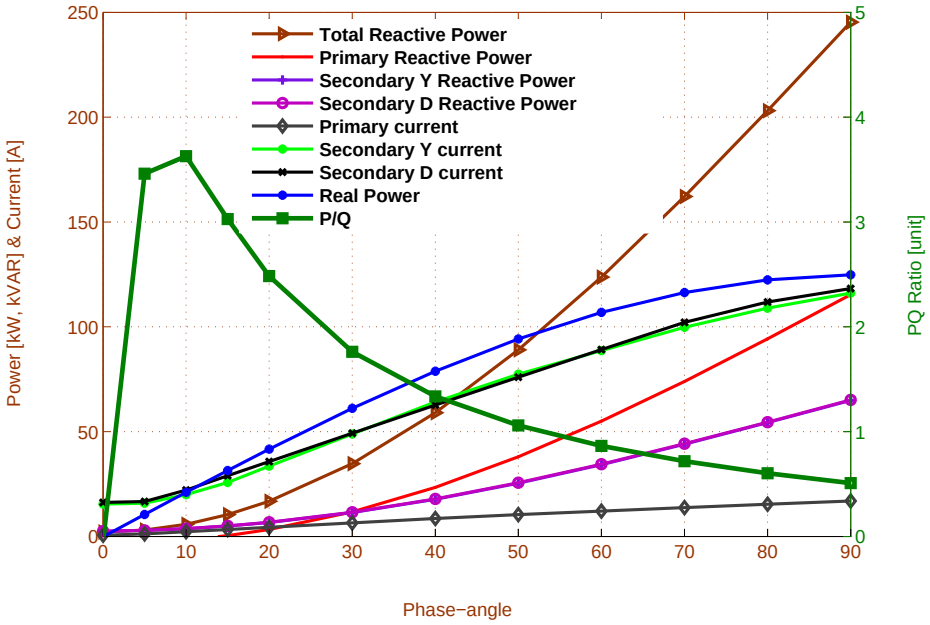


Figure 3.1: *P, Q-δ* curve for Y:Y/Δ

10 kHz. Total converter loss which depends not only on reactive power-flow but also on used device characteristics, become smallest for around nominal turn-ratio.

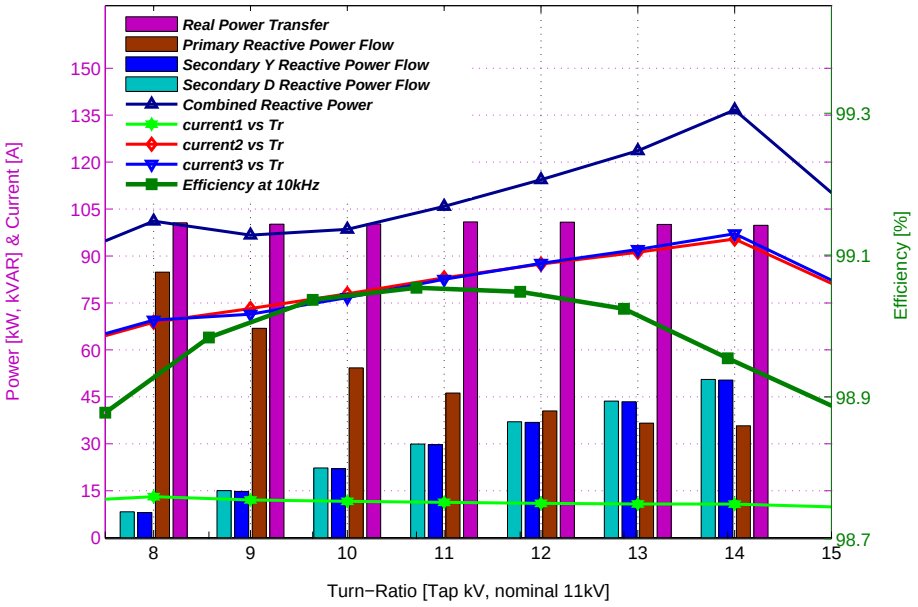
3.4 Transformer Specifications

The MV-HF transformer is used in DAB for voltage conversion and galvanic isolation between the LV output to MV input. Its specification is dependent upon power, voltage and tie inductance [70]. Due to the reasons given in previous chapter and for simple structure, three single phase transformers configured externally for Y:Y/Δ connections are used as a three-phase MV-HF transformer. Fig. 3.7 shows the flow-chart used in the design of the transformer. It starts from specification and goes through basic design to the detailed design. For a given power and voltage rating, a transformer can be designed with different combination of windings and core volume. Optimum design for over all weight of the transformer depends on balancing of the two on the basis of flux density and current density limits [70, 71, 72].

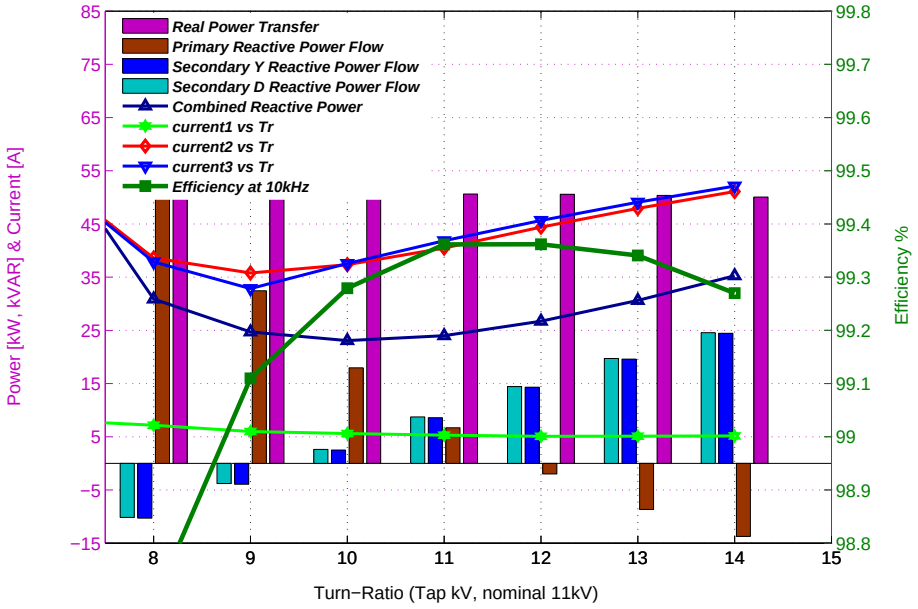
$$P = \frac{V_{s1} V_{r1}}{\omega L_{coupling}} \sin(\phi) \tag{3.1}$$

$$V_1 = 4.44 f B_m A_c N_1 \tag{3.2}$$

$$V_1 I_1 = 4.44 f B_m A_c N_1 \delta_m a_w \tag{3.3}$$

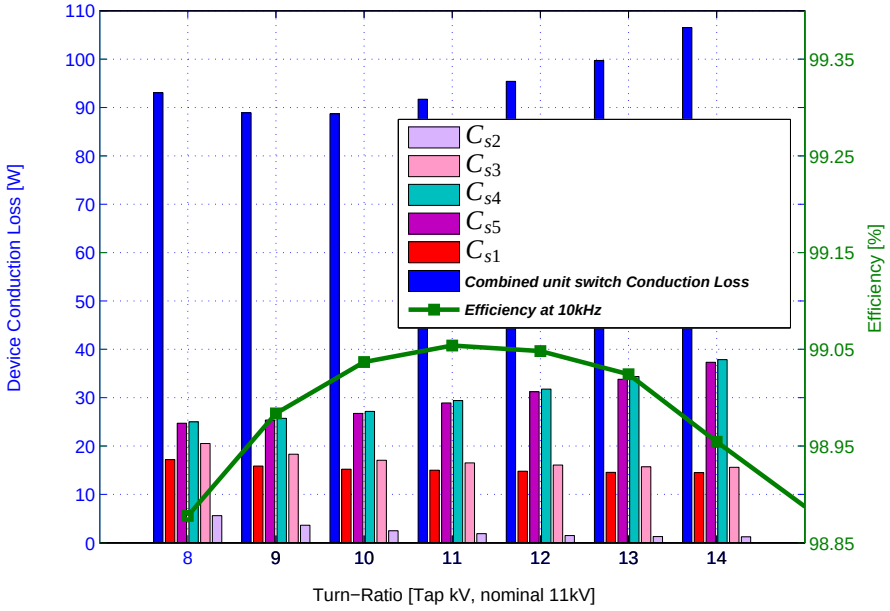


(a) 100 kW

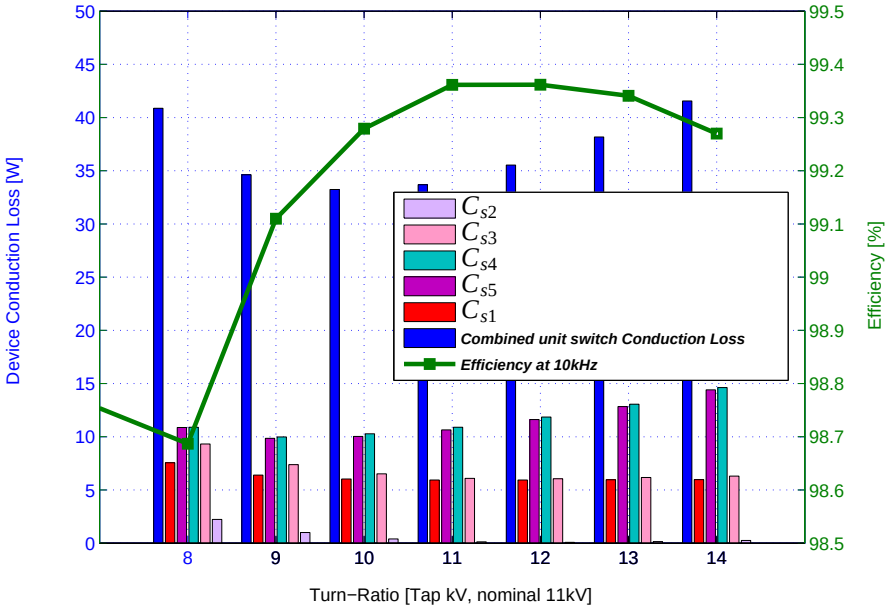


(b) 50 kW

Figure 3.2: Reactive power and current with turn-ratio

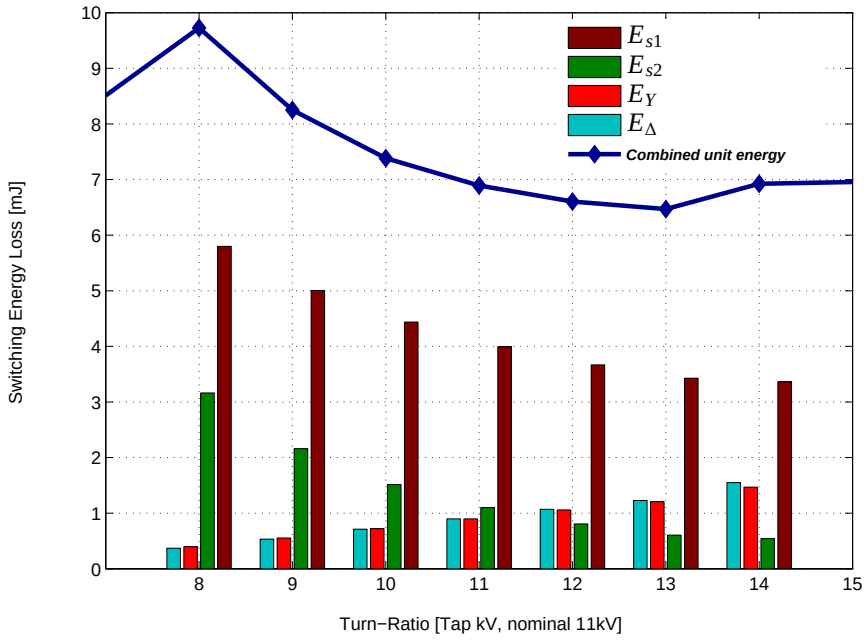


(a) 100 kW

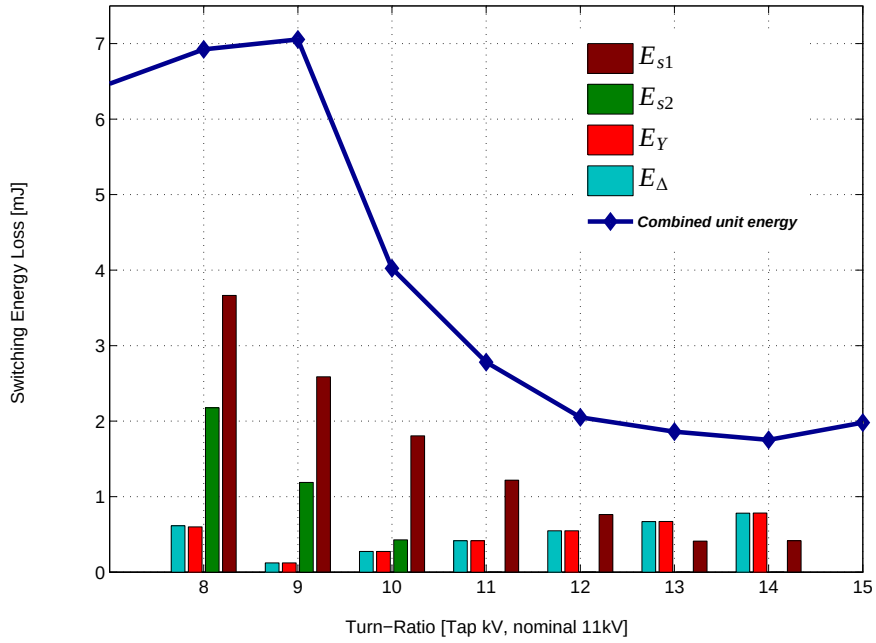


(b) 50 kW

Figure 3.3: Conduction losses with turn-ratio



(a) 100 kW



(b) 50 kW

Figure 3.4: Switching energy losses with turn-ratio

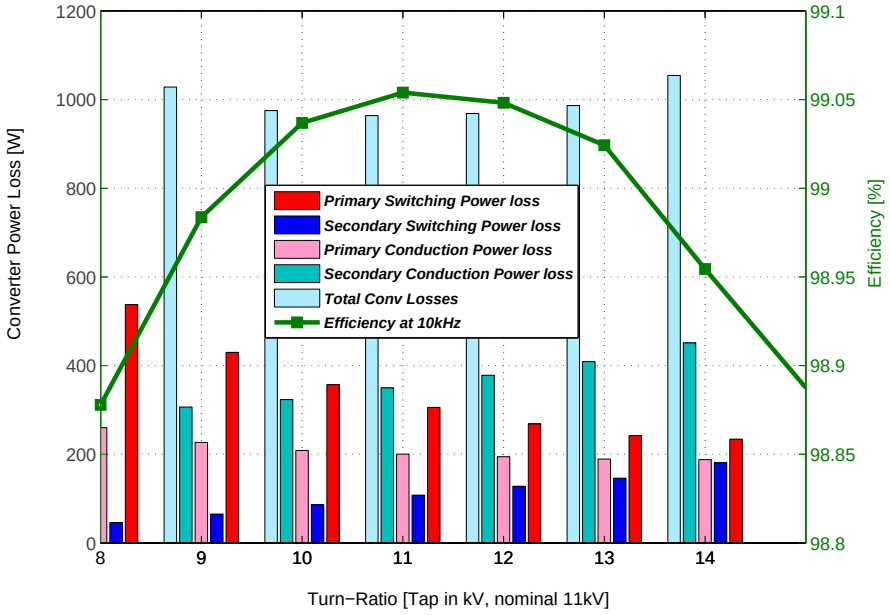


Figure 3.5: Efficiency with turn-ratio at 100 kW

$$P_c = K f^{\alpha} B_m^{\beta} \tag{3.4}$$

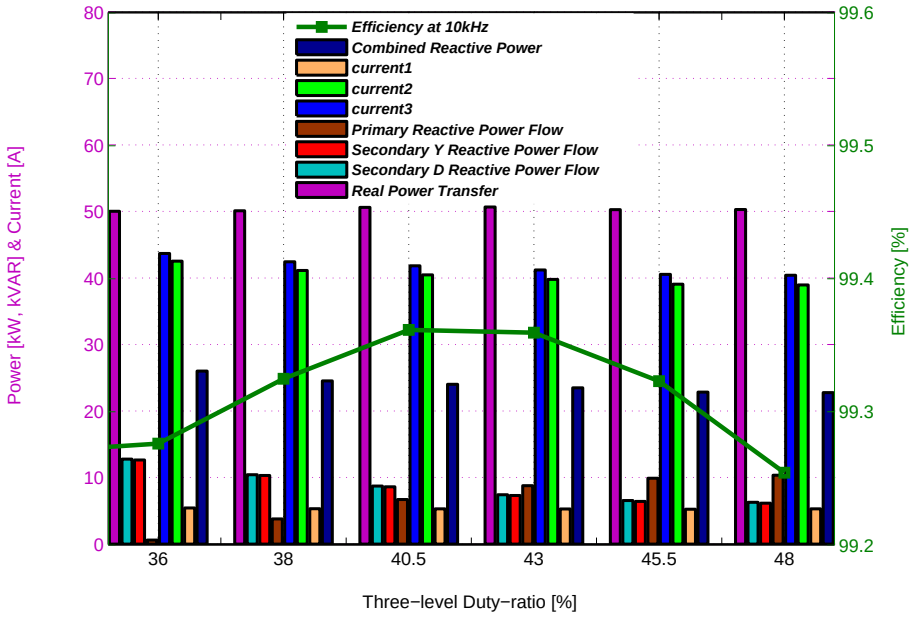
$$L_m = A_L N_1^2 \tag{3.5}$$

3.4.1 Switching frequency Specifications

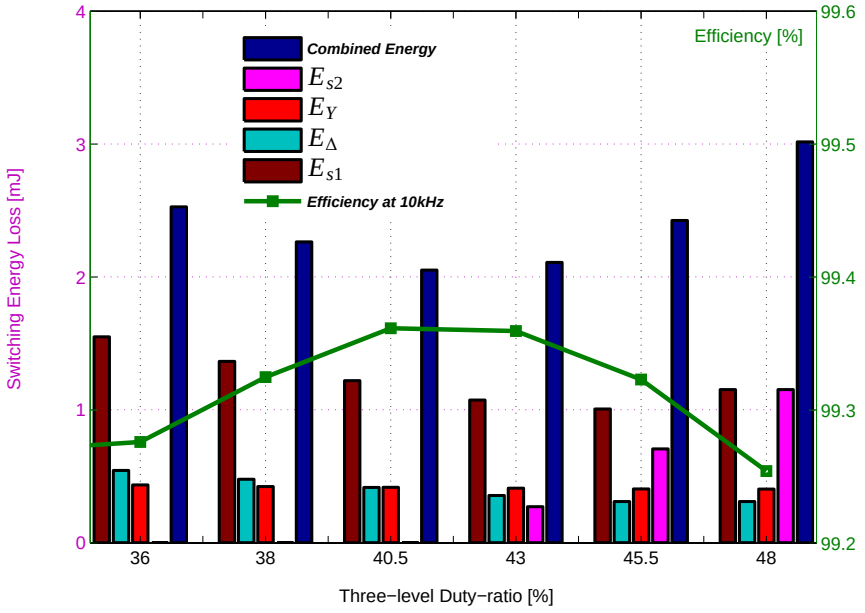
Ideally higher switching frequency reduces the size and weight of the power-electronics converter magnetics but increases switching losses. With real device switching-data, the DAB has following expected losses and efficiency as shown in Table 3.2. The DAB 10kHz switching-frequency for TIPS project has been selected mainly based on the MV converter losses. Other major factor for this selection is the MV converter dead-time used based on the intended maximum dv/dt switching. This is more than thrice the AFEC switching-frequency due to possibility of ZVS soft-switching. This affects both the core material selection and size of the transformer.

3.4.2 Transformer turns ratio Specifications

The transformer turn-ratio has significant impact on DAB performance. For optimum DAB performance from zero voltage switching (ZVS) and smaller conduction loss perspective, the turns ratio has to be equal to input and output fundamental voltage-ratios. DAB operates at minimum reactive power in this condition. For 22 kV-800 V dc-dc operation and rated primary three-level nominal duty as 41%, the



(a) Power



(b) Switching loss

Figure 3.6: Duty-cycle effect on power and switching loss at nominal turn-ratio at 50 kW

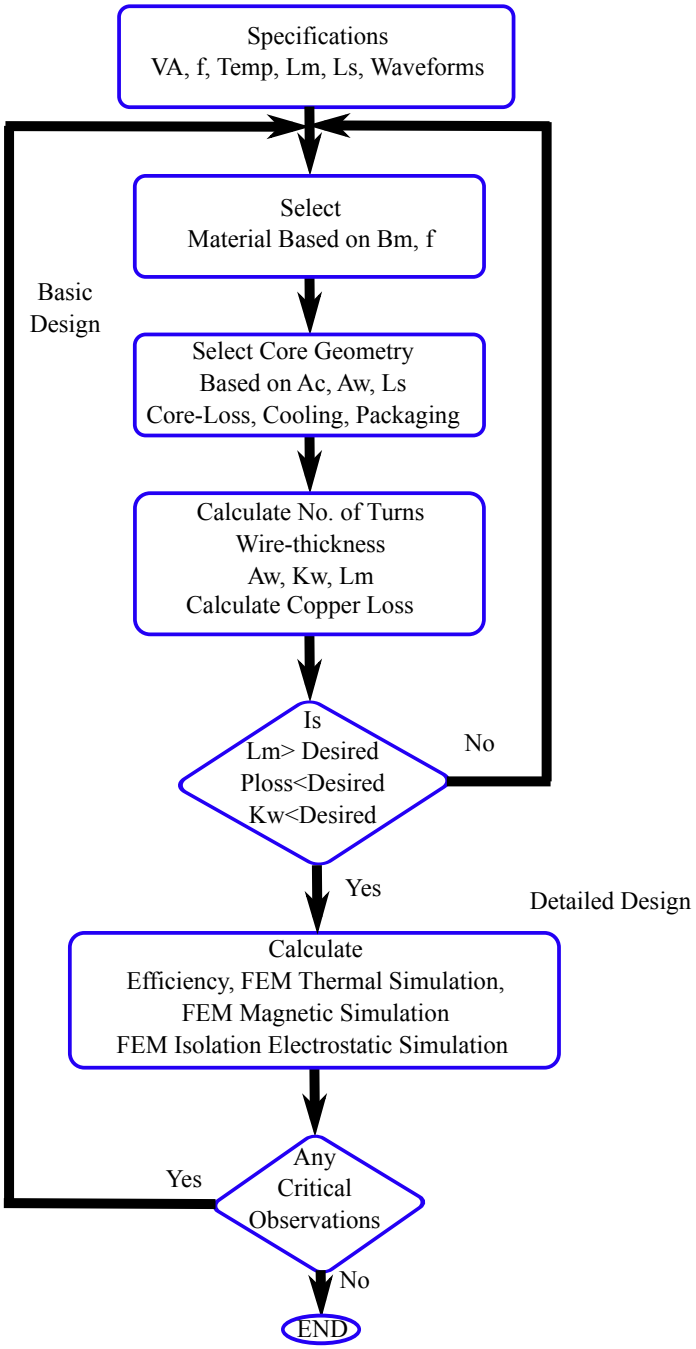


Figure 3.7: MV-HF transformer design block diagram

Table 3.2: 100 kW DAB expected efficiency with practical considerations

Parameters	Value
Primary Switching Loss	601.8[W]
Secondary Switching Loss	86.4[W]
Primary Conduction Loss	84.1[W]
Secondary Conduction Loss	511.0[W]
Total Converter Loss	1283.3[W]
Transformer Coil losses	50[W]
Transformer Core losses	80[W]
Total Losses	1413.3[W]
Efficiency	98.47[%]

turns for star LV winding is $27:1$ and $15.6:1$ for Δ winding. For 11 kV-800 V dc-dc operation, another set of secondary LV windings are desired. They are connected in series for 11 kV demonstration and extra set is left open for 22 kV. This results in 5 winding three single-phase transformers with turn-ratio $27:1:\sqrt{3}:1:\sqrt{3}$.

3.4.3 Leakage inductance Specifications

The DAB requires leakage inductances analogous to the coupling inductors in a front end converter. Equation 3.1 shows the simplified power transfer relation for DAB assuming sinusoidal approximation. To maintain ZVS, less reactive power and wider control range a full load phase angle of 40° between the two bridges has been selected. For rated conditions and 40° phase at full load of 100 kW, 40 µH equivalent coupling inductance is required for DAB referred to the LV side based on the power equation 2.4. Star and Delta two level converters share the fundamental current equally, thus leakage inductance required for each path on the LV side is 80 µH. For ZVS, less reactive power and better control a phase of 40°. 29.16mH referred on primary.

3.4.4 Voltage and Current ratings Specifications

Voltage ratings of the primary and secondary are directly related to the DC bus voltage levels intended. The MV converter being a half-bridge, applies lower voltage on the transformer. The voltage and current ratings are estimated from the ideal DAB simulations for rated power. Table 3.3 shows the required capability of each single phase-transformer for 11 kV DC bus. Table 3.4 shows the required capability of each single phase-transformer for 22 kV DC bus. Three-level topology and Y/Δ configuration makes transformer EMF close to sinusoidal. The peak currents are smaller compared to single phase DAB. Assuming sinusoidal approximation, the relation between transformer EMF and power rating to the pa-

Table 3.3: Transformer Specification for 11 kV-800 V, 100 kW Demonstration

	V_a **[V]**	i_a **[A]**	$V_{\Delta a1}$ **[V]**	$i_{\Delta a1}$ **[A]**	$V_{\Delta a2}$ **[V]**	$i_{\Delta a2}$ **[A]**	V_{Ya1} **[V]**	i_{Ya1} **[A]**	V_{Ya2} **[V]**	i_{Ya2} **[A]**
Peak	7334	11	402	44	402	44	268	82	268	82
RMS	4783	7.8	313	31	313	31	181	52	181	52

rameters are shown in Eq. 3.2 and 3.3 respectively. The galvanic isolation level of more than 35 kV RMS is desirable as voltage doubling may happen due switching transient. No grounding of the transformer tank is desired as it increases parasitic capacitance seen by MV converter. The 95 kV BIL desired for a equivalent line frequency transformer is automatically taken care off as it is not seen by the DAB transformer and has to be dealt on the AFEC converter.

Table 3.4: Transformer Specification for 22 kV-800 V, 100 kW Demonstration

	V_a **[kV]**	i_a **[A]**	$V_{\Delta a1}$ **[V]**	$i_{\Delta a1}$ **[A]**	$V_{\Delta a2}$ **[V]**	$i_{\Delta a2}$ **[A]**	V_{Ya1} **[V]**	i_{Ya1} **[A]**	V_{Ya2} **[V]**	i_{Ya2} **[A]**
Peak	14.67	5.6	805	46	*NA*	*NA*	536	83	*NA*	*NA*
RMS	9.6	4	626	31	*NA*	*NA*	362	52	*NA*	*NA*

3.4.5 Magnetizing Inductance Specifications

The selection of magnetizing inductance depends on the magnetizing current at rated voltage and frequency. It is calculated as in Eq. 3.5 from AL (inductance per turn) value of a core selected. Ideally, a relatively high magnetizing inductance is desirable for DAB application compared to an equivalent resonant converter. But there is a trade off between the magnetizing current and size of the transformer. Table 3.5 shows the sensitivity analysis of the magnetizing current and inductance. The magnetizing current is selected as 15% of full load current as it does not result in too much conduction loss and still helps in ZVS at light load as studied in simulation. One high voltage winding and four LV windings with turns-ratio $27:1:\sqrt{3}:1:\sqrt{3}$ are used and the magnetizing inductance referred to MV winding is 280mH corresponding to the 15% I_m current.

3.4.6 Parasitic Capacitance Specification

The transformer parameters such as parasitic capacitance and leakage inductance are estimated through calculations and FEM simulations after the design goes through first iteration. Simulation for sensitivity analysis on the baseline equivalent circuit with the estimated parameters are carried out both in standalone DAB and also in integrated TIPS mode with grounding. The inter-winding capacitance (C_{ps}) also contributes to the differential capacitance as well as common-mode (CM) capacitance. The inter-turn capacitance only contributes to differential capacitance. The differential capacitance is mainly respon-

Table 3.5: Magnetizing Inductance Sensitivity

I_m [%]	I_m [A]	L_m^{HV} [H]	L_m^{LV} [mH]
2%	0.08	1.9099	2.5254
10%	0.4	0.38197	0.505
20%	0.8	0.19099	0.25254
30%	1.2	0.1272	0.168
40%	1.6	0.095	0.126
50%	2	0.076	0.101

sible for ringing in the MV converter currents. The preliminary design showed a large inter-winding capacitance of 5000pF due to a compact design and the oil, used for insulation and cooling, acting as dielectric. Therefore a comprehensive simulation of entire TIPS with necessary grounding and CM choke is carried out for varying C_{ps} value but rated TIPS conditions. The MV device current and its ringing are monitored. The baseline common-mode TIPS simulation considers 400μH differential HV inductors at DAB HV and 500mH CM choke at the output inverter load terminals by default in all cases unless mentioned. The comparison table for different transformer-inductor parameters are shown in Table 3.6. After one more transformer design iteration by relaxing the size constraint, C_{ps} of 1200pF is selected with oil considered. Without oil, the C_{ps} is around 700[pF].

Table 3.6: Sensitivity analysis for transformer parasitics

C_{ps} [pF]	L_{f1} [μH]	i_a^{peak} [A]	i_a^{rms} [A]	$i_{\Delta a}^{peak}$ [A]	$i_{\Delta a}^{rms}$ [A]	i_{Ya}^{peak} [A]	i_{Ya}^{rms} [A]	f_r [kHz]	V_{CM} [kV]
5000	400	56.6	29.8	47	28.1	81.8	49.6	130 > 110 > 10	4.6
4000	400	39	14.6	51	31.63	84	54.5	130 > 110 > 10	4.4
3000	400	34	16.75	45	29.26	77	49.6	130 > 110 > 10	4.4
2000	400	12.6	6.3	42	28.6	75	50.1	130 > 10 > 110	6
1000	400	11	4.78	39	28.7	78	51	10 > 130 > 110	5.5
500	400	13.38	5.53	49.8	28.6	81.7	48.4	10 > 130 > 110	5
1000	800	11.25	5.34	51.1	30.5	79.1	50.2	10 > 130 > 110	35
1000	400,L_{cm1}	11.36	4.87	39.9	27.96	77.2	48.6	10 > 130 > 110	2.4

3.4.7 Core Material

Transformer core geometry is designed based on magnetizing inductance, voltage and current rating, frequency of operation and availability of the required core. Core geometry design also takes inputs from core loss and copper loss balancing at the rated conditions, commercial availability of core geometry and star-delta turns ratio constraint (near to $1:\sqrt{3}$). Eq. 3.4 shows the standard specific core loss equation. This can be used with core volume to calculate core-loss of the transformer. Design process is shown in

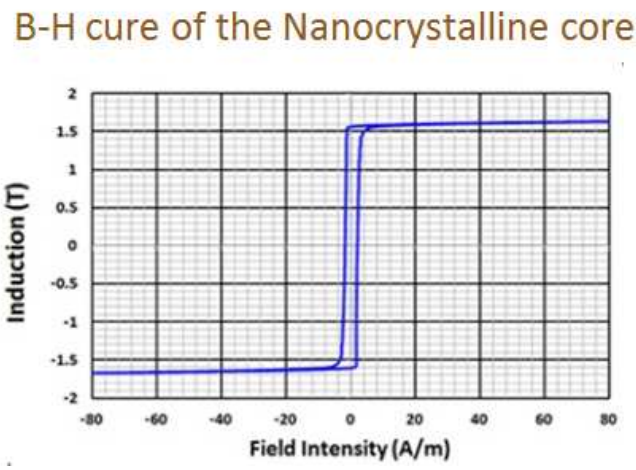


Figure 3.8: MV-HF transformer Core

the flowchart in Fig. 3.7. Magnetic material selection is very critical. Fig. 3.8 shows the B-H curve of the nanocrystalline core used. It has lower core loss and higher flux density. The transformer enclosure is oil filled for insulation and thermal management. The magnetic core area and window area are related to the core geometry. The core area can be calculated for a given number of turns, maximum flux and current density and conductor cross section area. The important constraint is the window area available for a commercially available core. This limitation can be solved by putting more cores in parallel. It is concluded from Eq. 3.5 here that magnetizing inductance which depends dominantly on number of turns cannot be kept too high for optimum size. Also, the transformer can not provide enough leakage inductance required for the power transfer; therefore external inductors are to be used at LV side. As per simulation result of the DAB converter in Fig 2.7 under ideal conditions, the specification parameters for the transformer are presented as in Table 3.7. The basic specifications for the transformer are based on simulation for 11 kV, 100 kW and 22 kV, 100 kW dc operation. The larger ratings from both table are taken as the final specification in Table 3.7.

3.5 DAB LV External Inductor Specification

External Inductors are required in case transformer does not provide required leakage inductance. From initial design calculations, transformer only provides 5 – 10μH leakage only referred from LV side, thus 80μH 6 nos. external inductors are needed. These external inductors are used in series to the MV-HF transformer leakage inductances. These inductors are connected after single-phase transformers are connected together in star-delta fashion at the low voltage side before inverters. Three inductors are required for star and three for delta windings. Fig 3.9 shows voltage and current waveforms of these inductors for ideal rated DAB conditions. The peak and RMS values are tabulated in Table 3.8. After

Table 3.7: Design specification parameters of the MV TIPS transformer

Parameters	**Value[Units]**
Power	35 kVA
Primary Voltage	9.6 kV rms, 16.6 kV peak
Secondary Voltage Y winding 1&2	360 Vrms, 605 V peak
Secondary Voltage Delta winding 1&2	625 Vrms, 1050 V peak
Primary current	8 A rms, 12 A peak
Secondary current Y winding 1&2	52 A rms, 83 A peak
Secondary current Delta winding 1 &2	31 A rms, 46 A peak
Frequency	10 kHz ±1%
Magnetization inductance (from primary)	280 mH, ±10%
Parasitic capacitance (inter-turn C_p)	< 500 pF
Parasitic capacitance (inter-winding C_{ps})	1000 pF
Isolation primary to secondary	20 kV rms
Efficiency	> 99%

considering the parasitics, the simulation of the DAB for this LV inductor is shown in Fig 3.10. It does not change the RMS values much, but as expected, it increases the peak value a little.

Table 3.8: LV External Inductor Specification for 22 kV-800 V, 100 kW Demonstration

	$V_{\Delta La}$ **[V]**	$i_{\Delta La}$ **[A]**	V_{YLa} **[V]**	i_{YLa} **[A]**
Peak	650	81	590	83
RMS	267.29	53.17	267.29	53.17

3.6 DAB HV External Inductor Specification

A practical compact MV-HF transformer has significant parasitics that cause spike and ringing in the DAB MV converter currents. Thus they play negative role for ZVS operation and also cause EMI as explained in later chapters. The spike is caused by hard-switching mode dv/dt of the HV SiC device and parasitic capacitance seen by the converter output pole. The current ringing is caused by large step-voltage on the transformer and the interaction of MV side leakage inductance and MV-HF transformer parasitics. This problem can be minimized by using external non-capacitive inductors at the HV side as the MV-HF transformer parasitics can not be reduced further due to size and cost constraint. A parallel resistor can be used together with each HV inductor as a complete filter to damp the ringing. Fig. 3.11

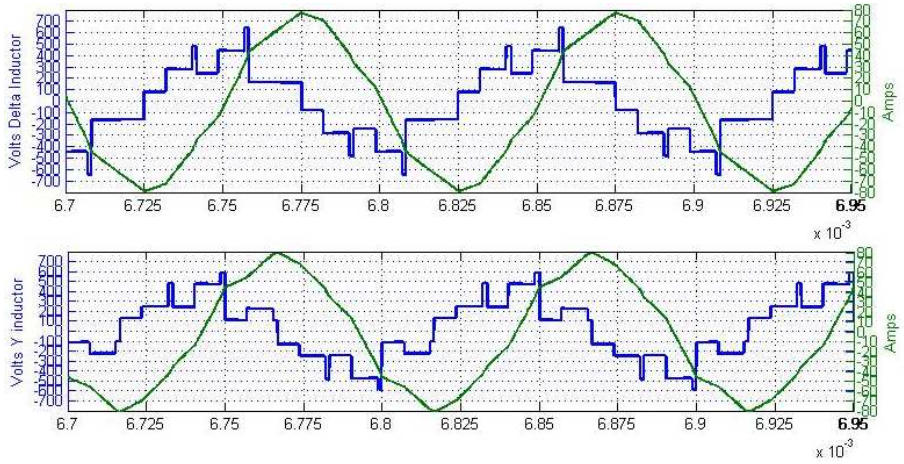


Figure 3.9: LV Inductor 100 kW steady state simulation with parasitics

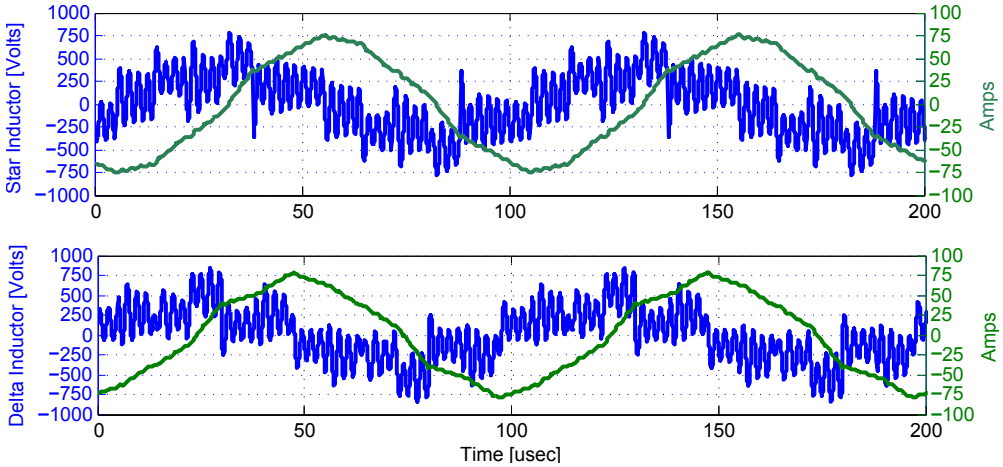


Figure 3.10: LV Inductor 100 kW steady state simulation with parasitics

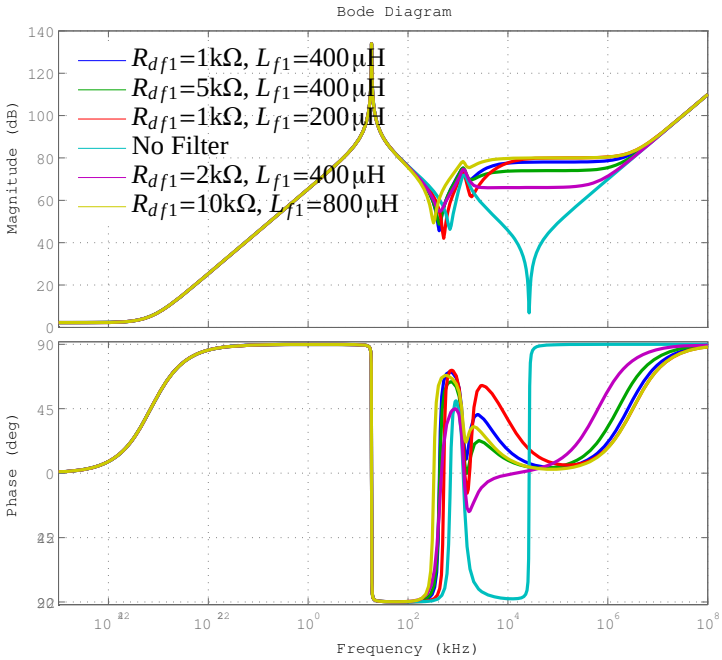


Figure 3.11: dv/dt filter design

shows the frequency sweep plot of the input impedance seen by MV converter for different values of the filter components. The high frequency region valley points are important from ringing point of view. A high R_{df} results in higher second frequency valley but lower first frequency valley point. The pole voltage will have dominant quasi-square harmonic frequencies, so the valley points should not be near to them. At rated condition, V_{ao} has $6m \pm 1$ harmonics, where $m > 1$. In addition keeping in view the R_{df} losses from time domain simulations, R_{df1}=5kΩ, L_{f1}=400μH is selected. Again the parasitics of this filter must be minimum, here it is around 50pF. Fig. 3.12 shows voltage and current waveforms of these inductors for selected transformer parasitics and rated DAB conditions. The peak and RMS values appearing for the HV inductors are tabulated in Table 3.9. The parasitics of the external inductors must

Table 3.9: HV External Inductor Specification for 22/11kV-800V, 100kW Demonstration

	V_{La} **[V]**	i_{La} **[A]**
Peak	7000	12
RMS	1350	8

be very small specially for this HV side location. This is achieved by separating the winding turns from one another and also from the core surface as maximum possible. For this a mechanical frame with holes

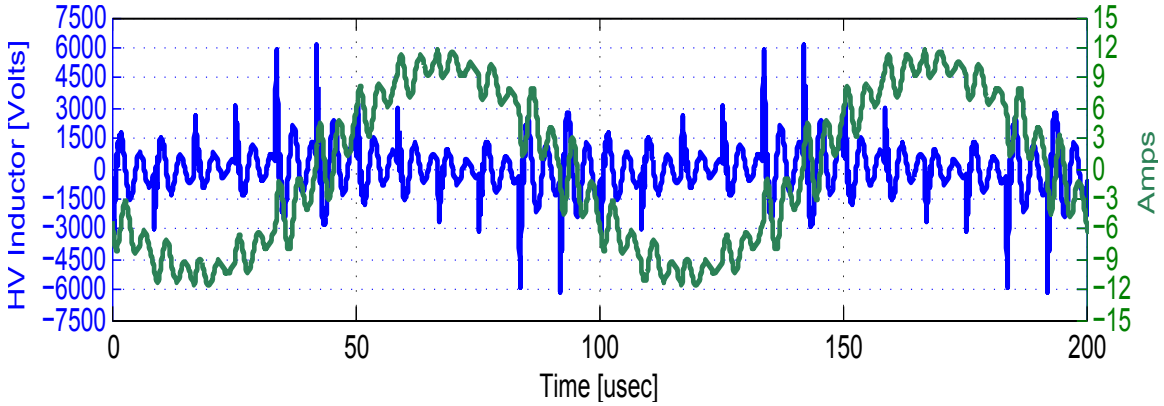


Figure 3.12: HV Inductor 100 kW steady state simulation with parasitics

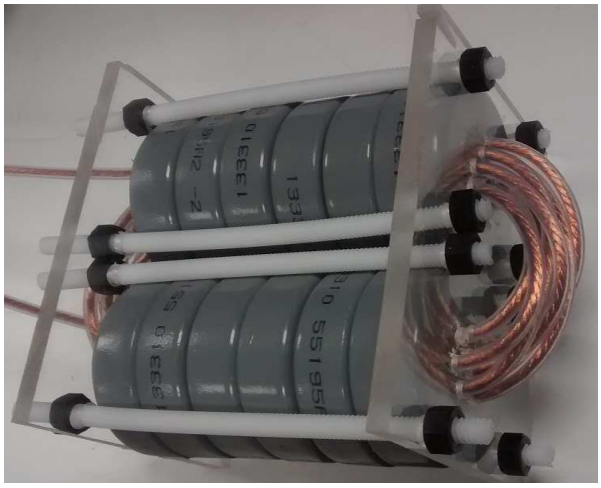


Figure 3.13: Low parasitic inductor

can be used to spread the turns in equidistantial space as shown for the inductor design in Fig. 3.13. It uses powder iron toroid cores with AL value selected based on its design objective in terms of saturation current and inductance value.

3.7 Conclusion

The MV-HF transformer for three-phase composite topology DAB specification has been generated from DAB simulation. In a DAB design, for the optimum performance, the transformer turn-ratio is kept in the ratio of fundamental voltages applied on primary and secondary. This ensures minimum reactive power-flow and also the maximum efficiency. The DAB inductance design for a given power-level can be optimized by selecting a lower full load DAB angle with high P/Q ratio but still holding enough precision in the control. Transformer turn-ratio and leakage inductance for a given power transfer can be designed optimum for high P/Q ratio and maximum efficiency. Hence the MV HF DAB design must take the parasitics of devices and magnetics into consideration on top of the conventional DAB design.

Chapter 4

DAB Transformer and Inductor Characterization for Parasitics

4.1 Introduction

This chapter presents the characterization of developed single-phase MV-HF transformer and external inductors, which are used for the three phase DAB applications [73]. A practical MV-HF transformer design consists considerable parasitics in the transformer [74, 75, 76]. These parasitics might not be favorable for DAB operation as presented is later chapters. In this chapter, the equivalent circuit model of the transformer is also presented. The challenges due to the parasitics are presented with simulation using the model of this transformer. Experimental switching tests are also provided to validate the transformer specifications and its proposed model. The switching tests using the actual 15 kV SiC IGBT based NPC converter are also presented to show the effectiveness of the HV side filter inductor against parasitics.

4.2 DAB MV-HF Transformer and Inductors

Fig. 4.1 and Fig. 4.2 show photographs of the developed DAB external inductors from specifications in previous chapter. Fig. 4.3 shows the photograph of the MV-HF transformer designed and built for TIPS application and from the specification in previous chapter. It is rated at 35kVA, 10 kHz, 9600 V to 625V/625V/360 V/360 V, and 65kg when dry, 95kg when oil filled. Before they are used in the MV DAB demonstration setup, it is important to characterize them for parasitics. The DAB simulation incorporating the associated parasitics helps understand the EMI and ZVS issues. This also helps to study the effect on controls.

Figure 4.1: DAB HV inductor

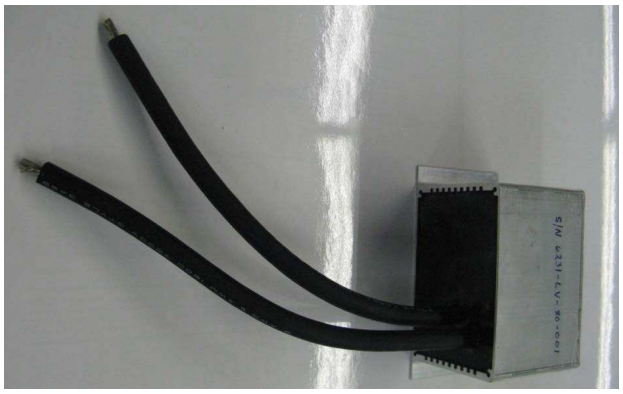


Figure 4.2: DAB LV inductor

Figure 4.3: Photograph of the MV-HF transformer with winding arrangement

4.3 Transformer Characterization

The transformer characteristics are measured with *HP*4294A impedance analyzer. The magnitude and phase of the impedance are measured from 100Hz to 100MHz from primary terminals for two cases of secondary open and shorted. Open and short circuit tests are used to calculate the equivalent circuit parameters of the MV-HF transformer. Fig. 4.4 and Fig. 4.5 show the impedance-angle plot with

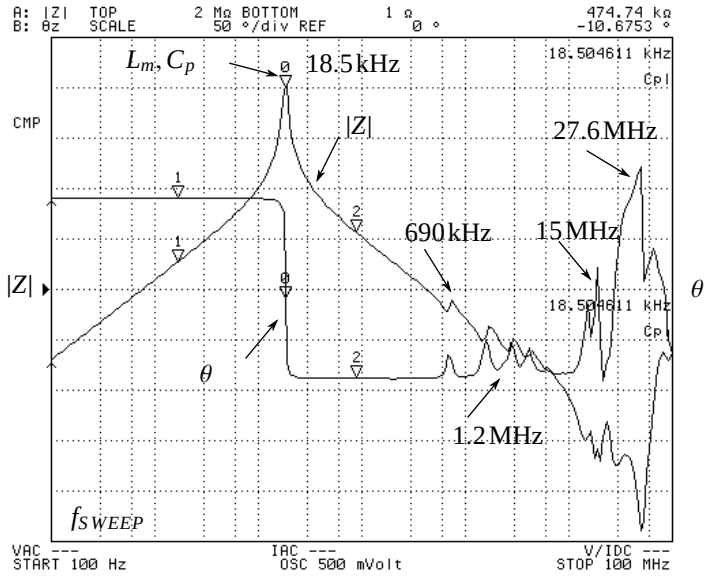


Figure 4.4: MV-HF transformer impedance plot secondary open-circuit

respect to frequency in log scale from primary winding respectively for open and short circuit cases. The initial 20dB positive slope in open circuit test represents L_m. The resonance at 18.5kHz indicates the total transformer capacitance to L_m resonance. This capacitance C_m comes to be 250pF from the resonance frequency and L_m calculations. Short circuit test mainly represents series parameters of the transformer i.e. leakage inductance. As it is a five winding transformer, there are different short circuit test combinations. This can be used to distribute the leakage inductance to each winding. The resonance at 500kHz can be considered due to total differential capacitance pair with leakage inductance. The series capacitance which is in parallel with leakage produces resonance at 1.2MHz in both tests. As the winding resistance increase exponentially with frequency, higher frequency resonances are over damped. The highest resonance frequency in this range occurs at 27MHz and the circuit turns inductive from capacitive at this point. This can be modeled with a small inductance in series with the overall

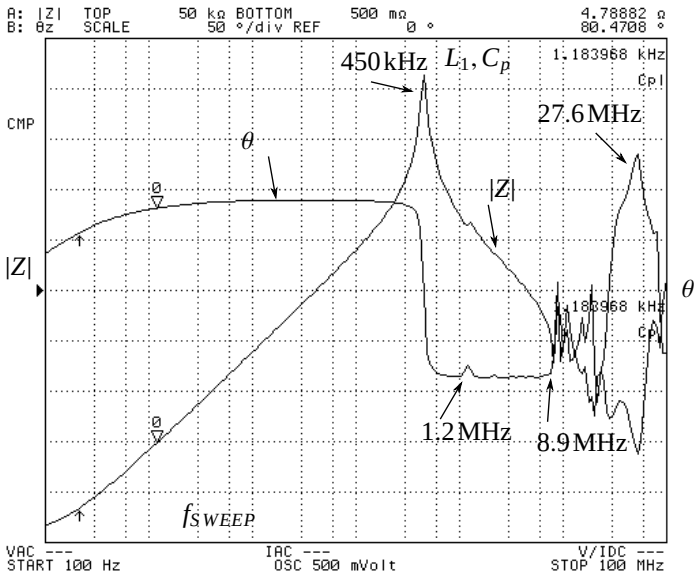


Figure 4.5: MV-HF transformer impedance plot secondary short-circuit

circuit at primary side. Hi Pot tests, voltage transfer ratio tests and heat run tests are also done to complete the characterization. The core loss and coil losses are estimated to be 50 W and 80 W respectively from the heat runs; the estimated efficiency of the transformer is 99.6%. Hi pot tests showed transformer withstood 25 kV. The voltage transfer ratio tests showed the primary to secondary ratios to be 26.7 and 15 for Y and Δ respectively.

4.4 External Inductor Characterization

Fig. 4.6 show the impedance-angle plot with respect to frequency in log scale from LV side external inductor. The initial 20 dB positive slope represents L_{s1}. The resonance at 2.22 MHz indicates parasitic capacitance (C_{s1}) to L_{s1} resonance. This capacitance C_{s1} comes to be 65 pF from the resonance frequency and L_{s1} = 80 µH calculations. Fig. 4.7 show the impedance-angle plot with respect to frequency in log scale from HV side external inductor. The initial 20 dB positive slope represents L_{f1}. The resonance at 1.5 MHz indicates the parasitic capacitance (C_{f1}) to L_{f1} resonance. This capacitance C_{f1} comes to be 28 pF from the resonance frequency and L_{f1} = 400 µH calculations.

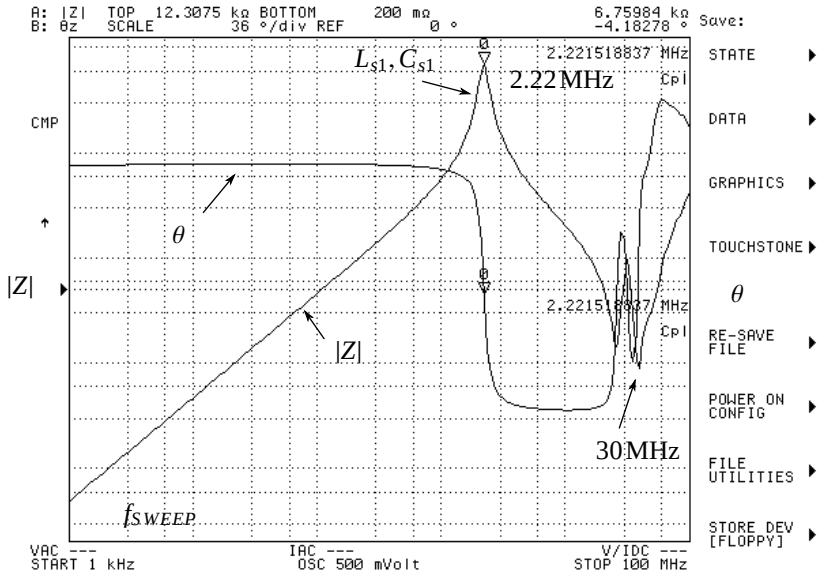


Figure 4.6: LV inductor impedance frequency plot

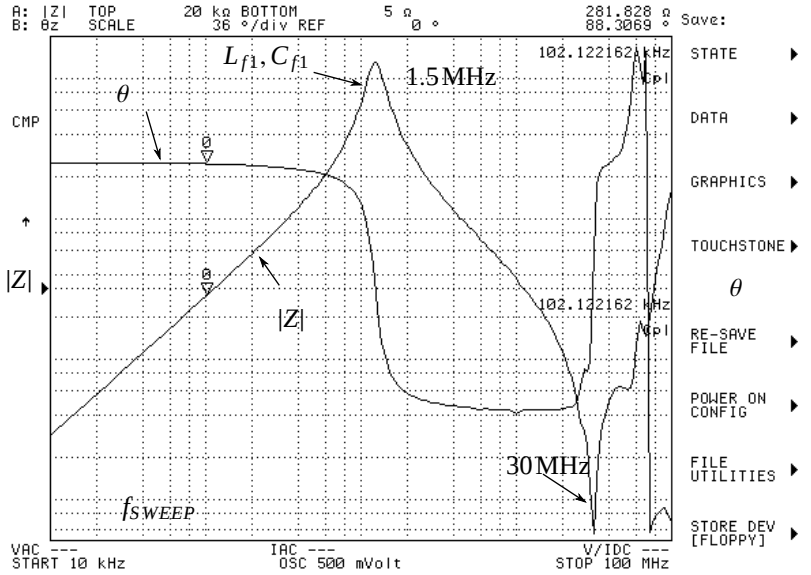


Figure 4.7: HV inductor impedance frequency plot

4.5 Transformer Equivalent Circuit Modeling

Equivalent circuit model of the MV-HF transformer is useful in the simulation of the DAB converter to predict converter performance. Fig. 4.8 shows the open/short circuit frequency sweep of the MV-HF transformer [32]. Based on this plot an equivalent circuit is synthesized for simulations as shown in Fig. 4.9 similar to [74, 77] based on the impedance measurement. The measured parameters are shown in the Table 4.1 [32]. The MV-HF transformer measurements data can be used to synthesize an equivalent circuit. Circuit simulation is done in Spice to build the equivalent circuit model. An equivalent circuit model is built to match impedance frequency sweep characteristics of the MV-HF transformer [48]. The simulation and measurement plots are compared and the parameters are tuned. The skin effect can be modeled using a high resistance in parallel with leakage inductance. The mutual capacitance is difficult to model. A simple equivalent circuit considering major frequencies is shown in Fig. 4.9. Mutual ca-

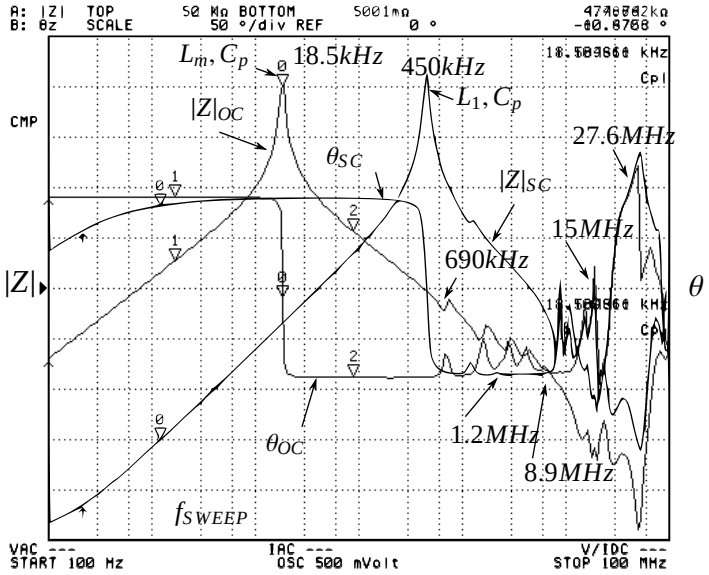


Figure 4.8: MV-HF transformer impedance plot

pacitances affect the L_m-C_p resonance dominantly and out of 250 pF only a small portion comes from actual inter turn capacitance. This is justified because 18.5 kHz frequency does not match if 250 pF is considered in addition to the mutual capacitance. The equivalent circuit synthesis helps in addressing any control issue which may arise due to the transformer parasitics. The transformer design, analysis and characterization have been validated by using one transformer in single phase DAB experimental mea-

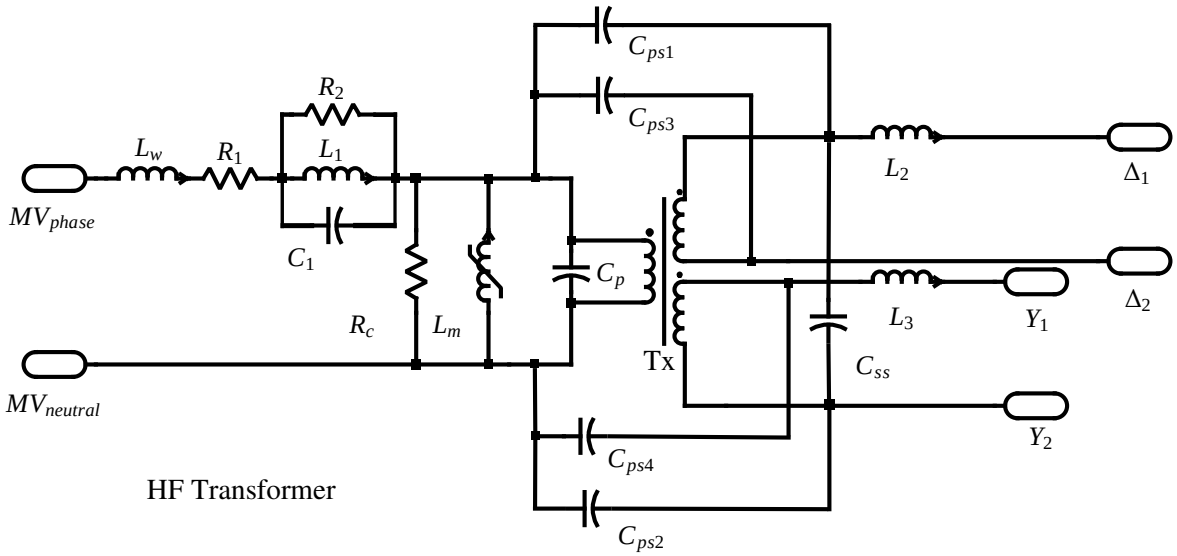


Figure 4.9: MV-HF transformer equivalent circuit

Table 4.1: Measured parameters of the MV MV-HF transformer

Parameters	Absolute	p.u.	Parameters	Absolute	p.u.
L_1	150 µH	0.0052	$C_{ps'i}$	180 pF	(0.02)
R_1	1.3 Ω	0.0007	N	$26.7:1:\sqrt{3}$	
R_2	4000 Ω	2.2	R_{df1}	5000 Ω	2.7
C_1	100 pF	0.05	C_{ss}	4000 pF	0.0005
L_m	293 mH	10.14	L_2	4 µH	0.05
L_w	500 nH	10^{-5}	L_3	7 µH	0.05
C_p	50 pF	0.0057	R_c	5 MΩ	2700
L_{f1}	400 µH	0.0152	L_{s1}	80 µH	2.09

surements. The corresponding measured parameters of the transformer are summarized in Table 4.1. Fig. 4.10 and Fig. 4.11 show the impedance-frequency for spice simulation of the equivalent circuit from primary winding for open and short circuit cases respectively. Fig. 4.12 shows the exact per phase equivalent circuit of DABC system with transformer and inductor equivalent parameters. It is very useful for designing the filter parameters and also for modeling and control design of the DABC [32]. Since the MV-HF transformer parasitic capacitance can not be minimized beyond certain value due to size and cost constraints, a dv/dt non-capacitive inductor based filter on the MV side is employed.

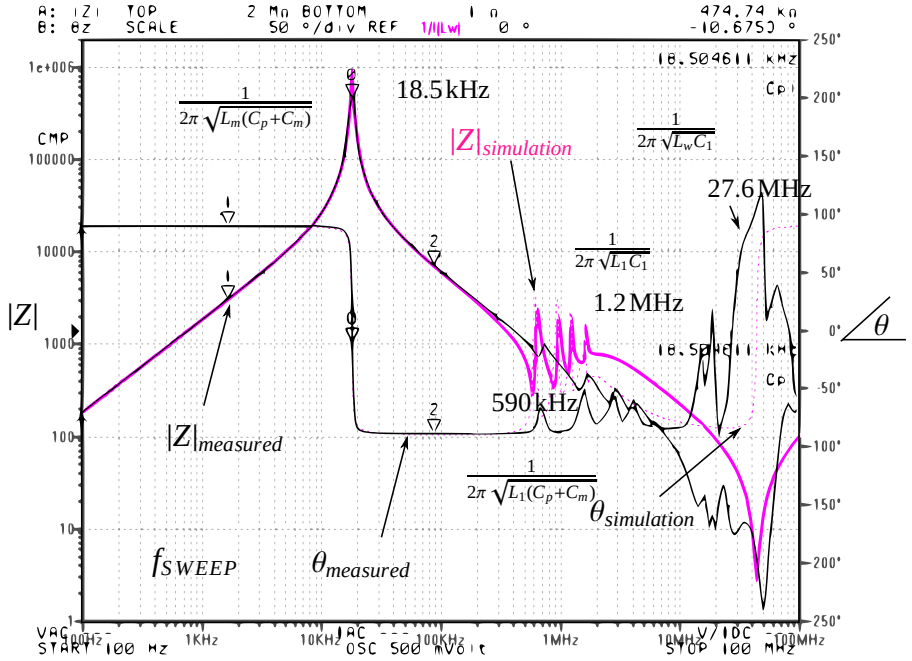


Figure 4.10: MV-HF transformer spice-simulation secondary open-circuit

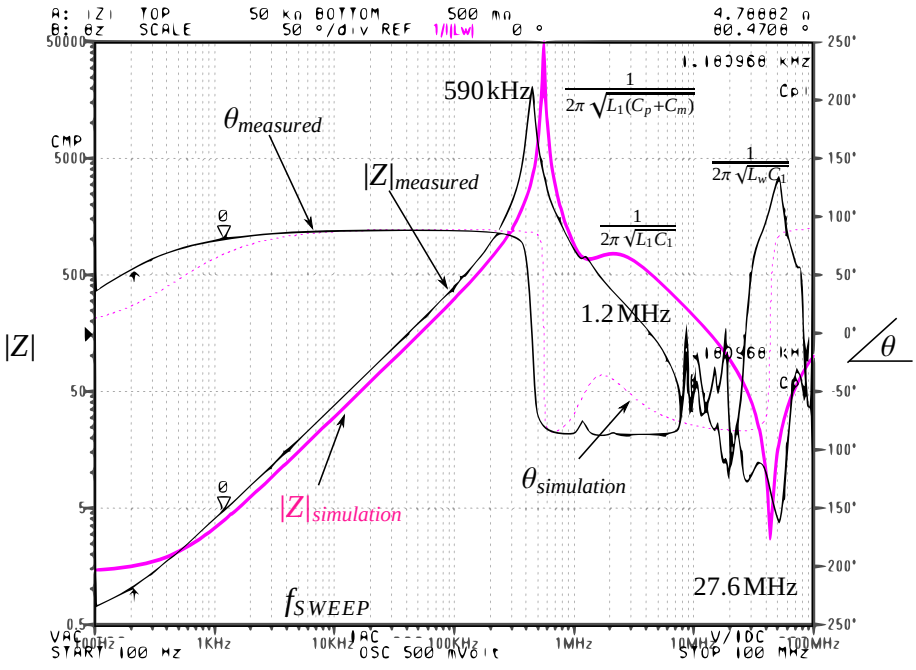


Figure 4.11: MV-HF transformer spice-simulation secondary short-circuit

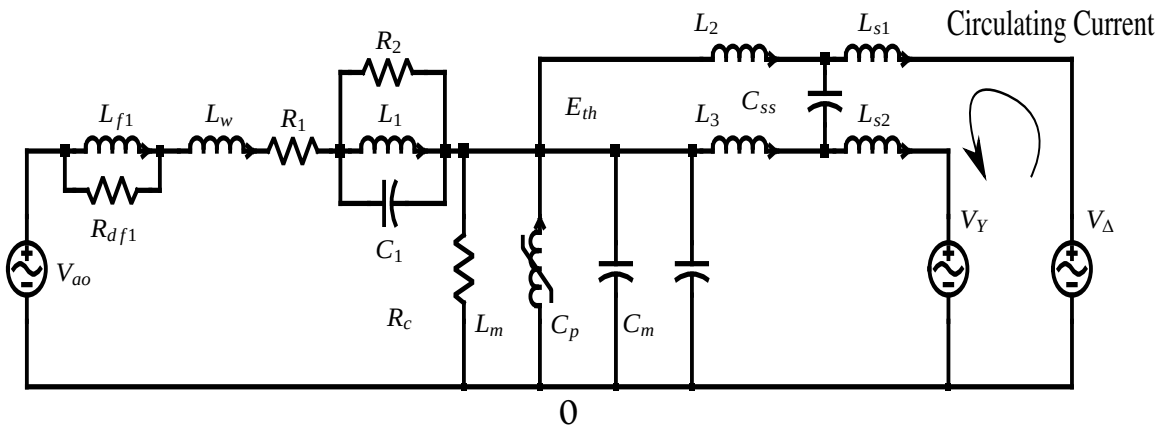


Figure 4.12: Single-phase equivalent circuit of Y:Y/Δ DABC

4.5.1 MV-HF Transformer Mutual Capacitance

Although the MV-HF transformer is used for isolation between the input and output stages of the TIPS, the C_{ps} is always present which propagates the CM noise to the output. Fig. 4.13 shows the electrostatic FEM simulation of a simple equivalent specification transformer of the actual MV-HF transformer. The transformer core outer geometry is 30cmX26cmX40cm, made with U-cores. The total C_{ps} = 1200 pF is calculated from the FEM simulation and it matches with the MV-HF transformer measured value. This indicates that for smaller C_{ps}, the transformer size has to be increased.

4.6 MV-HF Transformer Testing

4.6.1 Test at IAP Lab

The MV-HF Transformer is electrically tested both at manufacturer and in the lab. Tests performed at the manufacturer are mainly impedance measurements, hi-pot, heat-run with open secondary, heat-run with shorted secondary and heat-run with 10 kHz square wave. Fig. 4.14 shows the test setup photograph. The characteristics magnetization inductance comes as 400 mH, leakage inductance as 600 µH and primary to secondary capacitance as 1200 pF. The hi-pot test is performed from primary to secondary up to 12kV dc for 1min without any issue. Fig. 4.15 shows the voltage-ratio measurement result for star LV winding. A fixed voltage square wave up to 800 V is applied on the MV terminals with LV terminals kept open and the desired winding voltages are captured. Fig. 4.16 shows the voltage-ratio measurement result for delta LV winding. The voltage-ratio of primary to delta secondary comes as 15 and from primary to star secondary as 26.7 from these results. Fig. 4.17 shows the MV-HF transformer shorted secondary switching test result where the excitation is done with a 10 kHz square wave voltage from primary MV side and all the secondaries are short-circuited. This is kept running for 350 min as shown in Fig. 4.18.

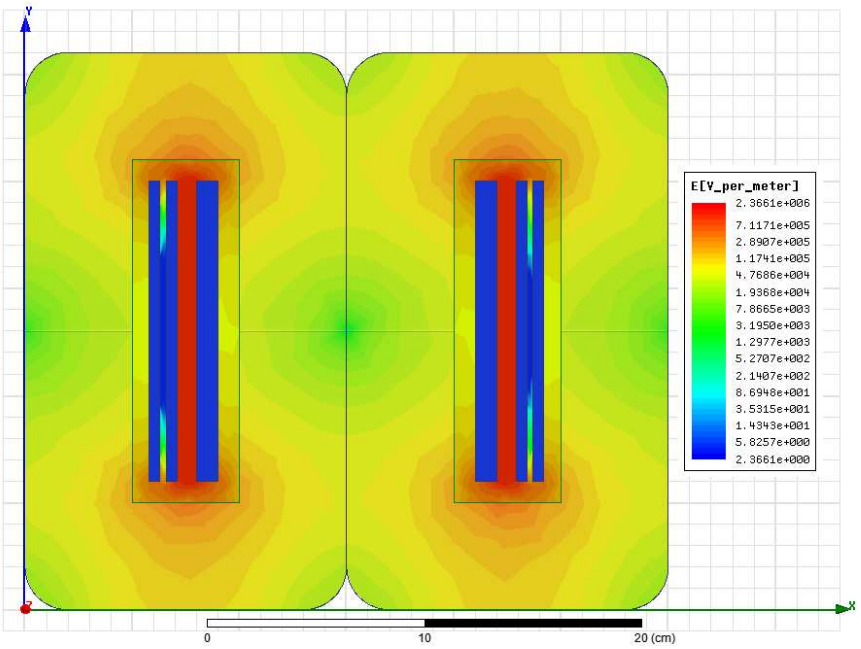


Figure 4.13: Electrostatic FEM simulation for C_{ps} of MV-HF transformer equivalent

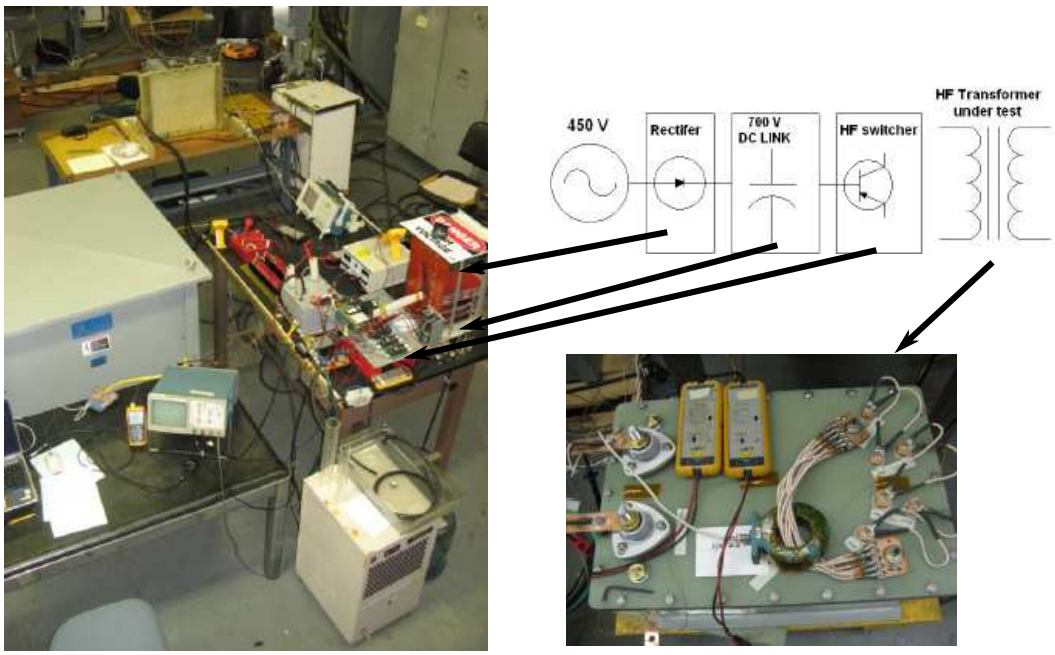


Figure 4.14: MV-HF transformer IAP test setup

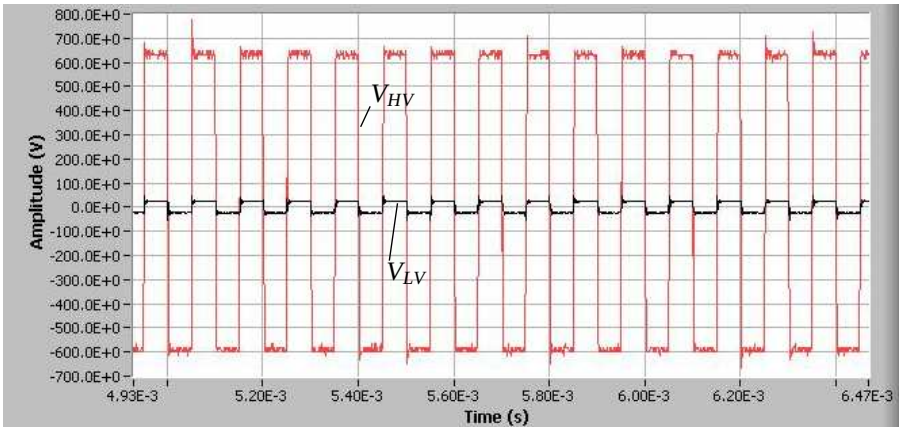


Figure 4.15: Switching test on MV-HF transformer for star LV voltage ratio measurement

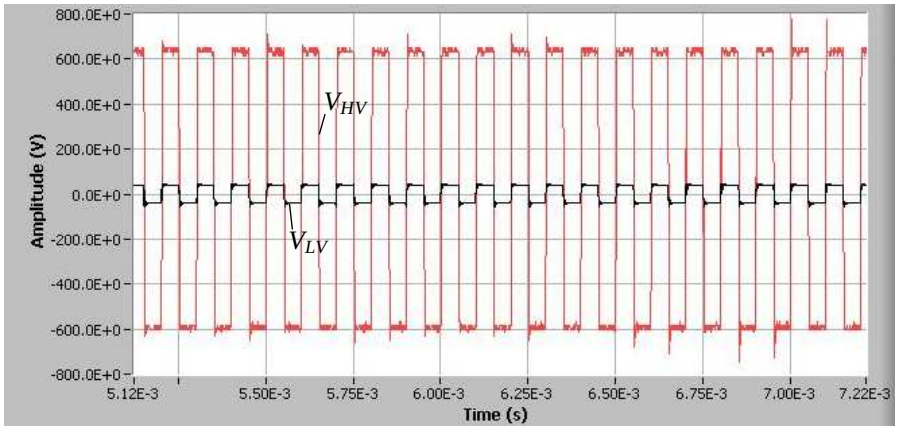


Figure 4.16: Switching test on MV-HF transformer for delta LV voltage ratio measurement

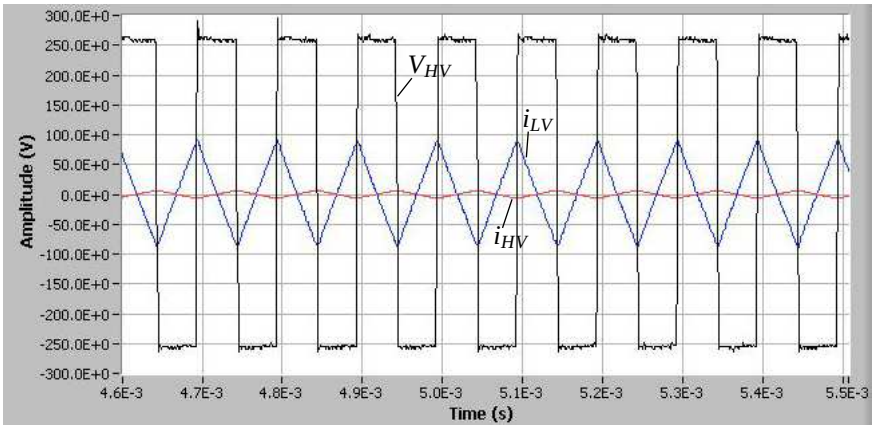


Figure 4.17: Switching test on MV-HF transformer losses measurements

Since it is not a rated voltage condition it mainly gives rated conduction losses. It gives coil conduction loss as 50 W. The core losses are estimated using FEM simulation which gives 80 W. Therefore the total losses are 130 W and the MV-HF transformer efficiency comes about 99.6%. The heat-run temperatures are monitored at different locations. The oil temperature sensor is dipped in to the oil after stopping the electrical excitation for safety, therefore it shows a sharp rise that is misleading. The secondary end top sensor gives highest reading for the arrangement. Overall the temperature stabilizes in about 5hours.

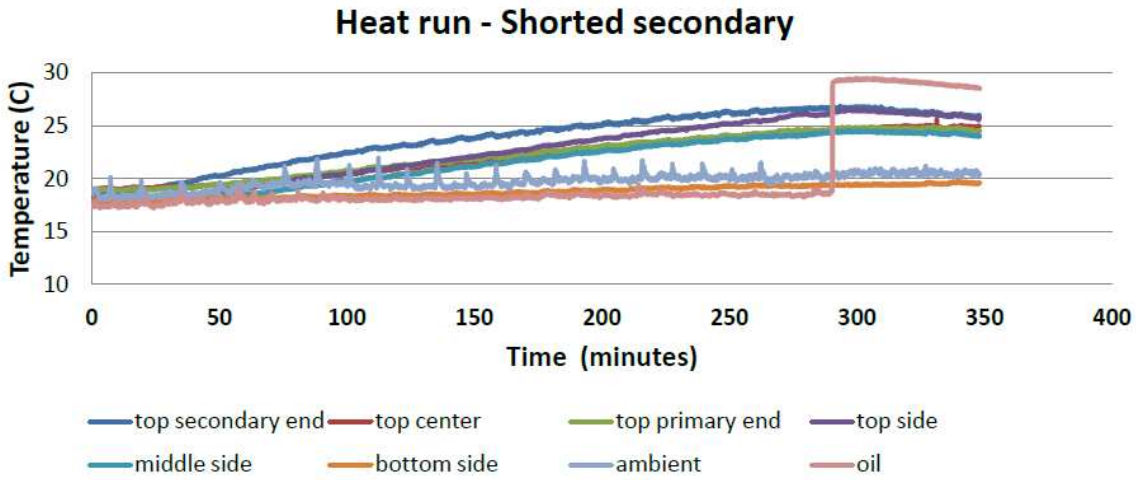


Figure 4.18: Heat-run test on MV-HF transformer with short circuit test

4.6.2 Test at FREEDM Lab

The 15kV, 20A, 2μm buffer SiC IGBT based SiC JBS diode-clamped NPC converter with 200Ω gate-resistance, hardware discussed later, is used to apply higher voltage and higher dv/dt quasi-square voltage waveform on the MV side of the transformer with secondaries under different loadings. The schematic of the test setup is shown in Fig. 4.19. All the secondaries are connected in series together. This test validates the transformer model and also highlights the importance of DAB ZVS on the waveforms which are discussed later. Fig. 4.20 shows the test setup photograph, mainly the transformer connections with HV and LV side external inductors. These tests also highlight the importance of these inductors. Fig. 4.21 shows the test results at 1kV on transformer primary MV and resistive load of 800Ω on the secondary LV but without the HV filter inductor on the MV side. A large spike with high-frequency ringing can be observed as expected. Fig. 4.22 shows the expanded view of the same test result. The frequency of ringing can be observed to be 3MHz which is closer to the applied dv/dt rate (frequency). Therefore the converter applied dv/dt or the transformer capacitance has to be carefully

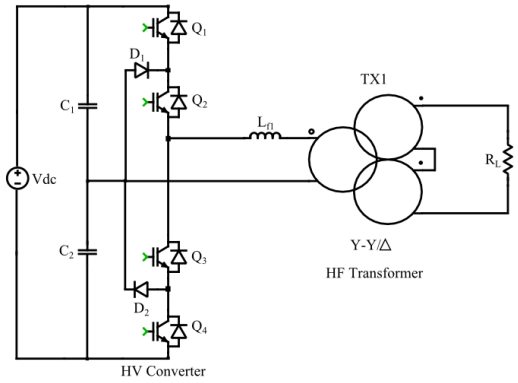


Figure 4.19: Switching test on MV-HF transformer testing arrangement

Figure 4.20: MV-HF transformer NCSU test setup

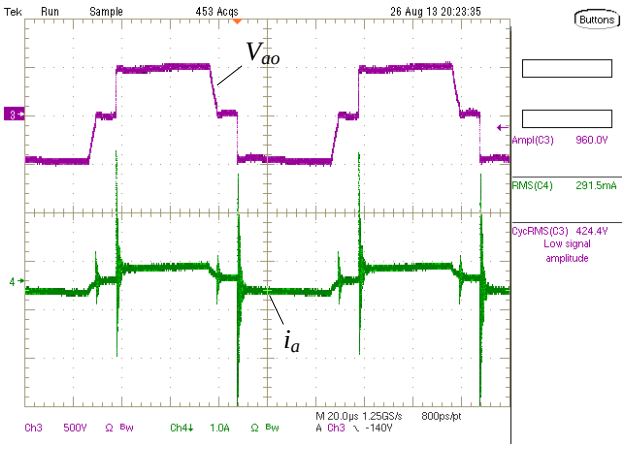


Figure 4.21: Test at 1kV with resistive load 800 Ω on secondary but without filter inductor

selected unless a HV filter is planned. Fig. 4.23 shows the test results at 2kV with resistive load of 800Ω on secondary but with the HV filter inductor of 400μH. The current spike has reduced from 2.5A at 1kV to 1.5A at 2kV but the ringing has reduced to a large extent (magnitude from 4A to 0.6A p-p) and its frequency has come down to 350kHz. The smaller reduction in spike current compared to the ringing can be attributed to the parasitic capacitance of the HV inductor itself. Therefore non-capacitive HV side inductors are desired. Fig. 4.24 shows the test results at 3kV with resistive load of 800Ω on

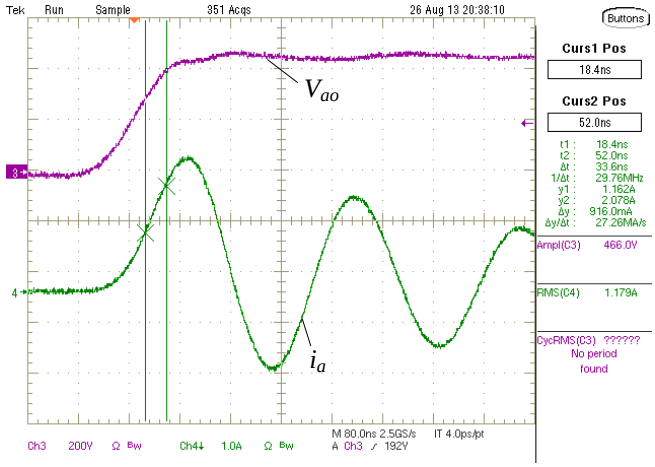


Figure 4.22: Expanded test at 1kV with resistive load 800Ω on secondary but without filter inductor

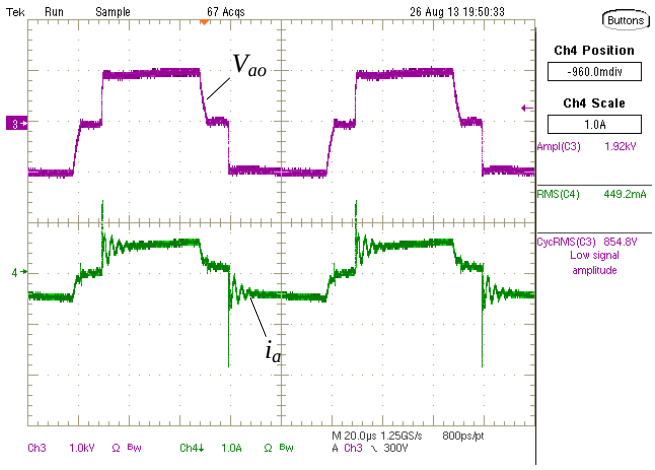


Figure 4.23: Test at 2kV with filter inductor of 400μH and resistive load 800Ω on secondary

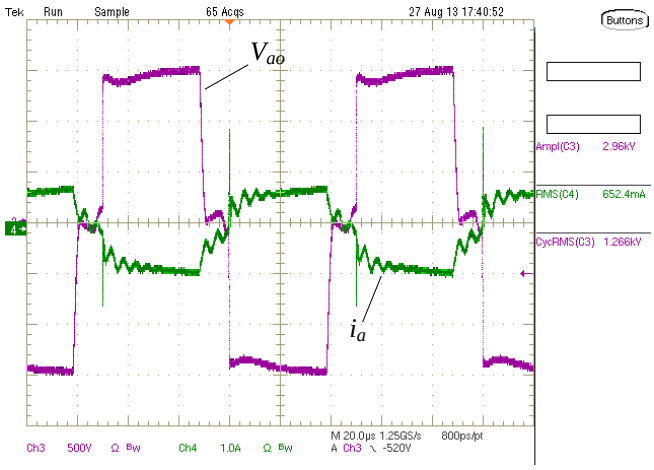


Figure 4.24: Test at 3kV with three filter inductors each of 1200µH and resistive load 800Ω

secondary but with increased HV filter inductor of 1200µH. The spike current is 1.8A, the ringing frequency is around 200kHz and magnitude is 0.3A p-p. Fig. 4.22 shows the expanded view of the same test result. Fig. 4.25 shows the expanded view of the same test result. It can be observed that spike current duration is same as the converter voltage dv/dt transition period. This verifies that combined parasitic capacitance on the converter pole is interacting with the dv/dt. Fig. 4.26 shows the test results at 3kV with HV filter inductor of 1200µH but R-L load of 6Ω and 80µH on the secondary side. Now the MV converter supplies lagging current and ZVS occurs. This is the intended mode in a DAB operation. Fig. 4.27 shows the expanded view of the same test result. It can be seen that the converter dv/dt has reduced to 1kV/µs and corresponding spike current is down to 0.3A. This mode is explained in later chapters. These experiments validate the model used in next chapters.

4.7 Effect of MV-HF Transformer Parasitic on the DAB Operation and Improvement

Fig. 4.9 shows a simplified parasitic equivalent circuit of the MV-HF transformer similar to [74] based on measurements. The parameters are shown in the Table 4.1. The estimated and measured leakage inductance is too low for DAB operation and so external inductors are required. These inductors are easy to design and install at secondary LV sides as the inductance value will be smaller because of turns ratio, though current capacity will be higher. Though six additional inductors are required for Y and Δ coupling, they help to reduce 5^{th} and 7^{th} harmonic currents circulating between star and delta windings. The primary parasitic capacitance is dominant over secondary capacitances in per unit terms due to high turns ratio. The primary current gets distorted at the switching instants though the secondary currents are still in smooth shape. This is because secondary converters are separated by large coupling

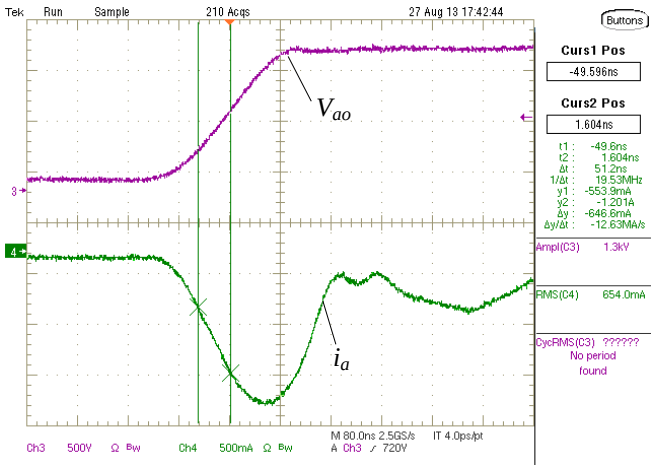


Figure 4.25: Expanded Test at 3kV with three filter inductors each of 1200μH and resistive load 800Ω

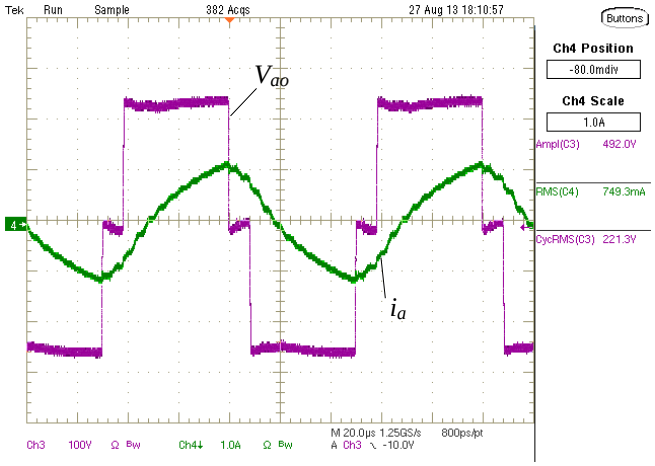


Figure 4.26: Test at 3kV with three filter inductors each of 1200μH and lagging load (R=6Ω and L=80μH)

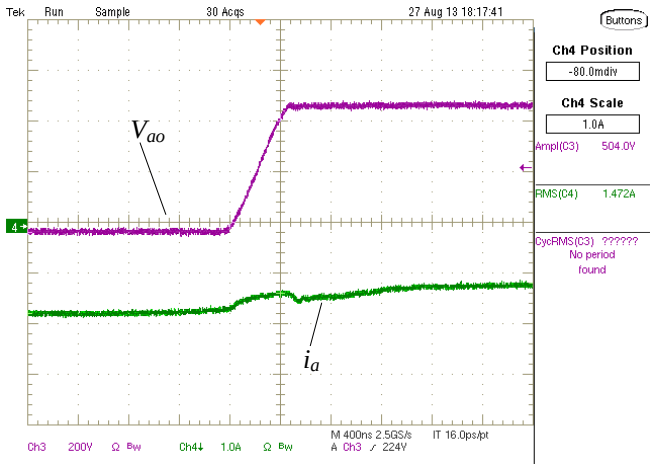


Figure 4.27: Expanded Test at 3kV with three filter inductors each of 1200μH and lagging load (R=6Ω and =80μH)

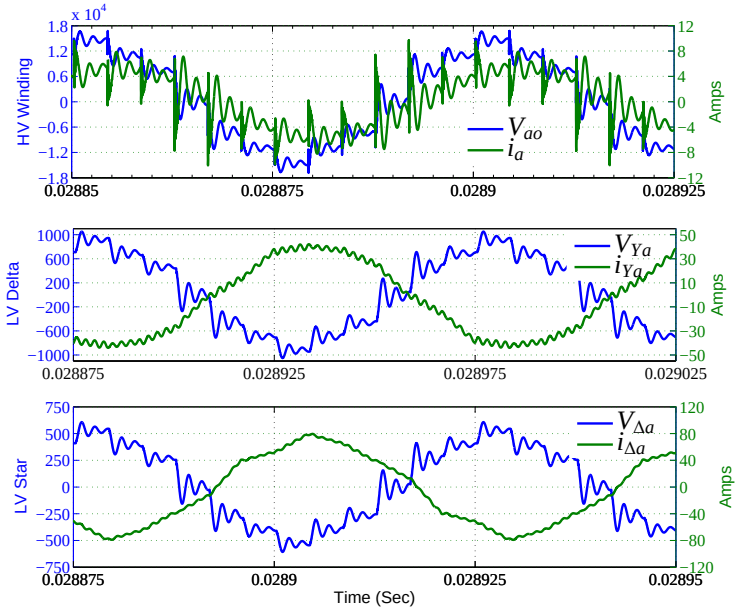


Figure 4.28: Transformer voltage and currents with parasitic for 100 kW

inductors (p.u. magnitude) from transformer. Analyzing the single phase equivalent DAB circuit shown in Fig. 4.12 and relating with Table 4.1, it can be seen that primary leakage inductance and transformer differential equivalent capacitance form a resonance pair. The primary current shoots up at the maximum step voltage application instant. To limit the device peak current, non capacitive external inductors are required at the HV primary side as well, whose value depends on the peak current to be allowed through the SiC device.

$$Z_p = \frac{1}{\frac{1}{sL_{f1}} + \frac{1}{R_{df1}}} + sL_w + R_1 + \frac{1}{\frac{1}{sL_1} + \frac{1}{R_2} + sC_1} + \frac{1}{\frac{1}{R_c} + \frac{1}{sL_m} + s[C_p + C_m]} \tag{4.1}$$

$$Z_p(\omega_p) = \sqrt{\frac{L_{f1} + L_1}{C_p + C_m}} \tag{4.2}$$

$$\omega_p = \sqrt{\frac{1}{[L_{f1} + L_1][C_p + C_m]}} \tag{4.3}$$

Eq. 4.1 shows the impedance of input section of the equivalent circuit in Laplace domain. Peak current is given by the ratio of maximum step voltage to Z_p at the natural frequency. Eq. 4.2 shows the simplified impedance value at the resonance frequency calculated from Eq. 4.3. C_m is the equivalent shunt capacitance contributed by mutual capacitances. The ringing currents do not result in turn on loss for NPC converter IGBTs, if the DAB current lags the pole voltage by a margin. The margin depends on the magnitude of final parasitic current flowing in primary. Due to the distortion in primary currents, the d-q currents get distorted and may deteriorate control performance. The L_m makes DAB current to lag even at light load and thus helps primary to achieve ZVS but reduces ZVS range for secondary. Star connection at the NPC converter reduces the maximum step voltage applied to transformer winding and limits the 15 kV IGBT peak current. The simulation waveforms for transformer winding voltage and currents considering parasitic are shown in Fig. 4.28. The primary current has ringing at the switching instants while secondary currents are still smooth. Transformer voltage also has significant ringing. The total effective differential capacitance measured from the MV side is 250 pF. It also includes the reflected secondary and inter-winding capacitances [32]. The primary-current would be high at the maximum step-voltage application instant. To limit the peak-noise current, non-capacitive external inductors are also required at the MV-primary side, whose value depends on the peak-current to be allowed through the devices and the ringing-frequency [49]. The star-connection at the primary three-level converter side reduces the maximum step-voltage applied to the individual transformer and makes it feasible for 15 kV-20 A IGBTs to supply the peak current.

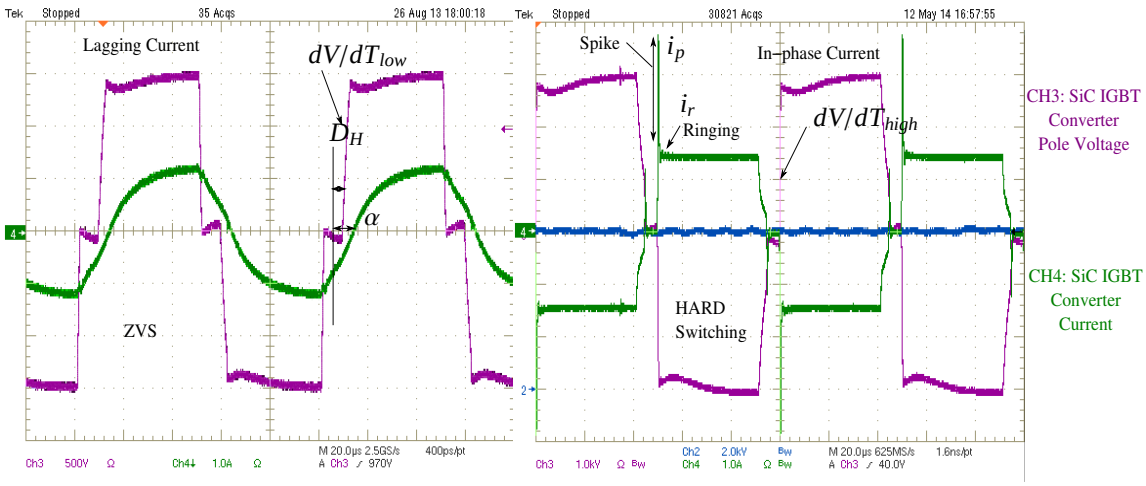


Figure 4.29: Experimental results showing ZVS effect on dv/dt slope of three-level pole

$$i_r(\omega_p) = \frac{V_{step}}{Z_p(\omega_p)} \tag{4.4}$$

$$i_p = C_{pole}\frac{dV_{ao}}{dt} \tag{4.5}$$

The parasitic MV side input impedance of the equivalent-circuit is shown in (4.1). The simplified impedance is shown in (4.2), at the resonance frequency (150 kHz-450 kHz) calculated from (4.3). The ringing current amplitude is shown in (4.4) at the natural frequency. Another component of spike current comes from dv/dt as in (4.5). The pole capacitance (C_{pole}) consists of device, inductor and transformer parasitics. Though C_{pole} is dynamic, an average assumption of 300 pF with 30 kV/µs slope gives an i_p of 9A. The ringing frequency of this component is in couple of MHz range as it is an impulse with dv/dt transition only. Fig 4.29 shows the hardware results for soft-switching effect on current ringing and dv/dt slope. Fig. 4.29 shows the effect of soft-switching on the dv/dt slope of V_{ao}. The lagging current causes free-wheeling action of the anti-parallel diodes which in turn applies slower dv/dt due to the natural commutation. The hard switching dv/dt is much higher which depends on the gate resistance below punch-through level. It generates spike and ringing in the device currents. It also narrows down the ZVS range. The control design is not affected by the parasitics as the resonant frequencies are much higher than the control bandwidth.

4.8 Conclusion

The transformer model spice simulation results match the frequency-sweep impedance measurements in both open and short circuit conditions. The FEM simulation of a similar practical design, also gives a matching realistic inter-winding capacitance. The Y:Y/Δ DAB utilizes three-level NPC converter at

22 kV side using 15 kV SiC-IGBT. This applies reduced step-voltage on the MV-HF transformers causing smaller ringing as concluded from simulations. The parasitics play major role in deciding soft-switching operation of the converter. The switching, hi-pot isolation and heat-run test results validate the transformer design. The presented experimental results with 15 kV SiC IGBT based NPC converter show the bad effect of parasitics in terms of current spike and ringing. They result in increased EMI and switching losses. The 3 kV test results after inserting the HV filter suppresses the current spike and ringing as expected. The simple mathematical terms derived for the spike and ringing in terms of pole capacitance, dv/dt and step-voltage, approximately explain the reason behind them.

Chapter 5

DAB Modeling and Optimum controls of the MV DAB considering non-idealities

5.1 Introduction

A three-phase DAB in Y:Y/Δ configuration for medium-voltage high power dc-dc application, operates with dominantly sinusoidal ac currents. A simple model is presented for the controller design. This model should also consider the transformer parasitics effect on the system as they are important for control in standalone and integrated TIPS operation of the DAB. Conventionally the DAB output voltage is controlled by adjusting the relative phase of primary and secondary converter switching with a PI controller based feedback loop. The DAB current is generally not controlled directly. However, for medium-voltage (MV) high-power DAB application based on 15kV SiC-IGBT devices, there is a need to limit the device peak current during transients as required by device safe operating area. These HV SiC devices do not have any overloading capability and do not have sufficient desat protection [41, 44]. This is partly attributed to the fact that SiC devices have resulted in higher chip power-density with higher blocking voltage and thermal conductivity. Another reason for current control is fast flux balancing [78]. The conventional current control approach is to sense the output dc current prior to the dc capacitor. But the current after capacitor is not appropriate signal for instantaneous power transfer as it is slower signal [38, 79]. The d-q signals in a synchronous frame aligned with the secondary voltage vector, represent the active and reactive components of the DAB high-frequency (HF) ac currents accurately [80, 49]. Compared to the DAB output current prior to the dc capacitor, the q-axis current has smaller ripple that avoids filtering. Also this current ripple magnitude depends on the DAB dc voltages and inductor value. The inner current control also helps to attenuate the dc offset problem during transients [38]. The d-q components completely describe the DAB operating condition and this information can be used to maintain zero voltage switching (ZVS). The phase-angle and the duty-ratio control of three-level neutral point clamped (NPC) converter at high voltage (HV) side (two plant-

inputs), make it possible for d-q based control to set the current-vector at an optimum angle of voltage-vectors ensuring ZVS and minimum reactive power-flow [81].

This chapter presents a simple d-q model for the DAB based on sinusoidal-approximation (SA) and the significance of d-q currents. A detailed control block-diagram for d-q based control implementation is also presented. It also presents the control strategy to ensure optimum-operation of the DAB enabled by d-q feedback. The three-level dc-bus mid-point can also be actively balanced by adjusting top and bottom duty-ratios independently [82]. The current sensing is challenging due to high speed continuous fetching for d-q calculations. The ADC speed is the only limitation for updating speed of the phase-angle. This is important when the closed loop bandwidth has to be high [83]. This chapter presents the minimum specifications of the controller for the present DAB topology with d-q current control. The FPGA and DSP are briefly compared for the given application. The important components of the board are also explained. It also presents the programming of the algorithm for the DAB application. The auxiliary boards used for safety and protection during MV operation are also described. It presents the experimental results of the control implementation in a low voltage prototype of the original DAB of the TIPS. The parasitics are scaled and added as lumped elements to emulate MV-HF transformer in the low rating prototype setup with objective to test the control with parasitics. It also presents the experimental results on a MV hardware setup with just voltage feedback but using the proposed control hardware and protections.

5.2 D-Q Frame Modeling of Three-Phase DAB

The three-phase Y:Y/Δ DAB topology was previously introduced in [80]. Compared to two-level $Y:Y$ DAB topology, it draws dominantly sinusoidal transformer currents without multiple-pulse PWM or resonant components[46]. In DAB, the relative phase-angle between primary and secondary converters is the primary control input. DAB is analogous to a vector-controlled active front end converter (AFEC) tied to a grid. The two-level secondary converters are switched with fixed phase six-step modulation and hence can be considered as the grid. The three level converter can be switched with variable duty-ratio and phase relative to the secondary and thus can be considered as the PWM converter. The MV-HF Transformer leakage inductance and external inductors make the tie inductor of the AFEC. The in-phase component of inductor current transfers real power to the secondary side output. The phase of this current can be controlled by adjusting the primary converter duty cycle [68, 84, 85].

5.2.1 Sinusoidal Approximation (SA) Model of DAB

For this topology, most of the power-transfer is carried by fundamental components. Hence the converter voltages can be assumed to be sinusoidal for simplicity.

$$i_{sq} = \frac{v_s}{|Z_{tie}|}\cos[\theta - \phi] - \frac{v_r}{|Z_{tie}|}\cos[\theta] \tag{5.1}$$

$$i_{sd} = \frac{v_s}{|Z_{tie}|}\sin[\phi - \theta] - \frac{v_r}{|Z_{tie}|}\sin[\theta] \tag{5.2}$$

Eqs. (5.1) and (5.2) show that for d-q components have different sensitivity with ϕ as the DAB impedance angle is near 90°. Fig. 5.1 shows a simple model of DAB system as current source. The magnitude is proportional to i_{sq} which has v_s and ϕ as the main dependent variables. The i_{sd} has v_r as the main dependent variable and is less dependent on ϕ in the operating range.

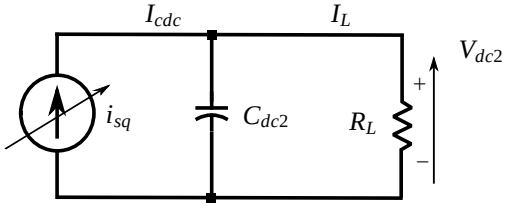


Figure 5.1: Simple equivalent circuit of DAB

5.2.2 D-Q Transformation

The DAB transformer current depends on primary, secondary voltages and the phase. It consists of real and reactive components. If the magnitude of the converter voltages is matched in the turns ratio of the transformer, the reactive component remains minimum and generally the current control is not done. In some cases it is required to eliminate the dc offset problem. With sudden change in the phase-angle, the flux in transformer needs to setup. The DAB currents capture a dc offset which decays with L_s/R_s time constant. Fig. 5.2 shows the space-vector phasor-diagram for the DAB. ZVS range shrinks for three-level converter ($< 50\%D$) and light-loading of the DAB. d-q control ensures ZVS operation of DAB, as it can maintain i_{sd} independent of i_{sq} by adjusting duty-ratio of primary converter and hence controlling primary voltage magnitude [86]. To calculate the optimum current-lag angle for DAB current, device switching characteristics are taken in to consideration along with reactive-power. SiC IGBT turn-off losses can be high, hence the current lag angle should be limited. For minimum ZVS lag angle, a margin for parasitic currents and dead-time are added to the converter zero-state angle.

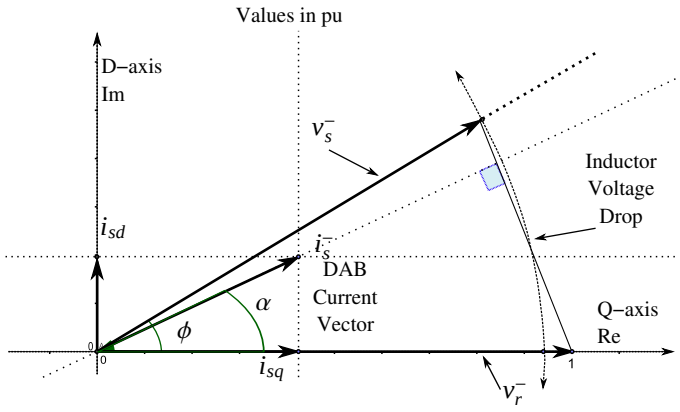


Figure 5.2: Vector diagram for DAB control

5.2.3 Significance of D-Q Current

The dominantly sinusoidal shape of current makes the Y:Y/Δ topology suitable for d-q current transformation. The i_{sq} component represents the actual DAB output current and has smaller ripple independent of the dc voltages or the inductor value. This avoids use of filtering and enabled faster current control bandwidth. The reactive component is not readily available from other methods. Fig. 5.3 shows the comparative simulation of d-q currents with conventional currents available for DAB current control. The transformation is with respect to rotating frame synchronized with secondary converter. The output dc bus is kept near zero. I_{cdc} has large ripple compared to the i_{sq} though both have same average value. Both quantities increase with the input voltage magnitude. They respond to the phase with higher sensitivity for ϕ near zero. In the contrary, i_{sq} is sensitive at ϕ near 90° to the input voltage. The i_{sq} depends only on the DAB phase-angle and input converter voltage. When the transformation is done with frame synchronized with primary converter, the i_{sq} matches the average input DAB current. But the input current has high ripple content. The ripple is dependent on the voltage drop across series inductance and its value. Fig. 5.4 shows the simulation with resistive load at output dc and zero initial voltage at the capacitor. The capacitor charges with rate proportional to $i_{sq} - I_L$ confirming the model in Fig. 5.1. Eq. (5.3) shows the simple model equation.

$$i_{sq} = C_{dc2}\frac{dV_{dc2}}{dt} + \frac{V_{dc2}}{R_L} \tag{5.3}$$

Output voltage affects the i_{sd} but not the i_{sq}. There is no current similar to the i_{sd} certainly not the $|I_{ac}|$ that captures peak current. Since there is no signal available which confirms that reactive component is minimum. Hence a current feedback is required in addition to the dc voltages, PWM and phase information. Hence the d-q currents represent the real and reactive components in accurate and fast manner.

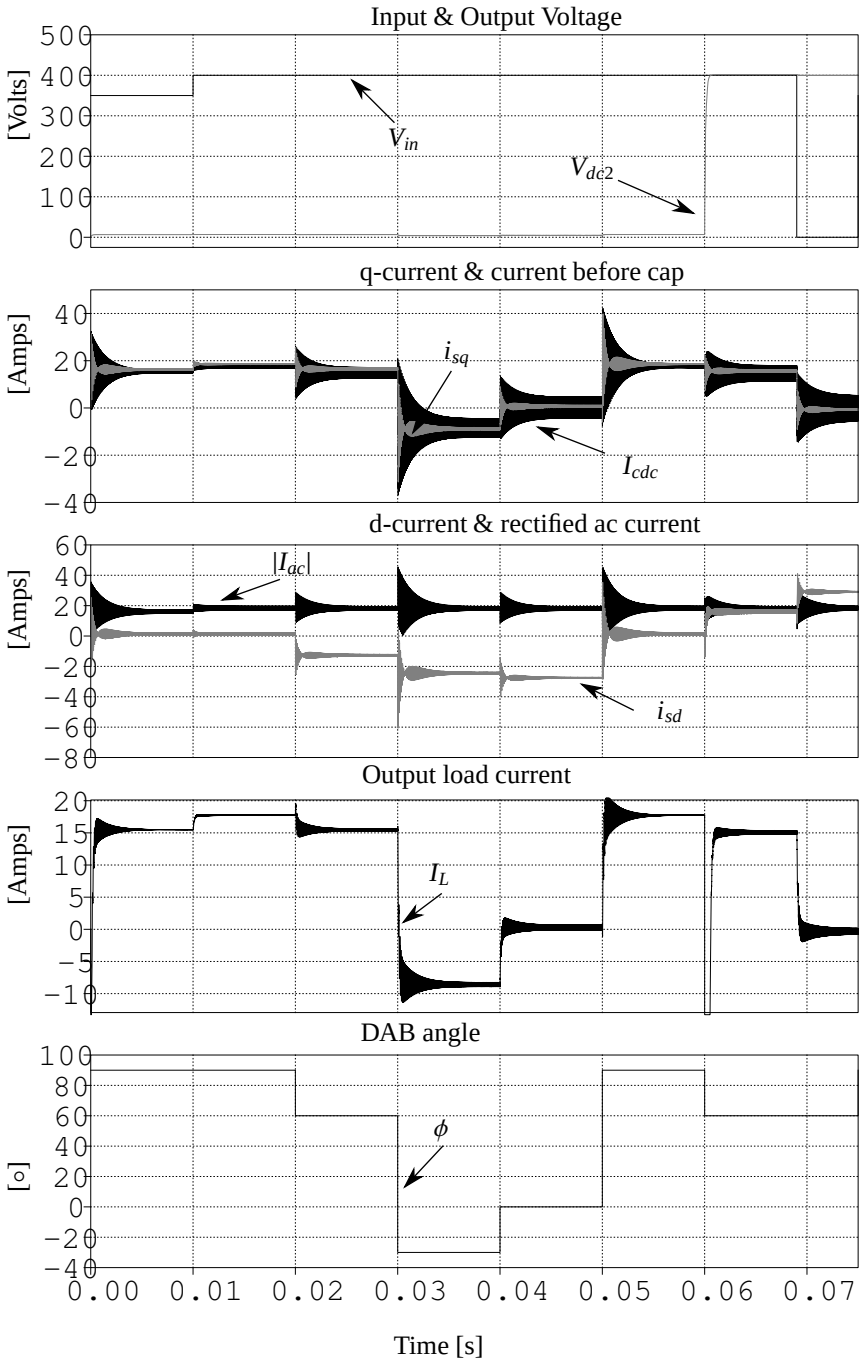


Figure 5.3: Simulation of the d-q transformation at near zero output voltage

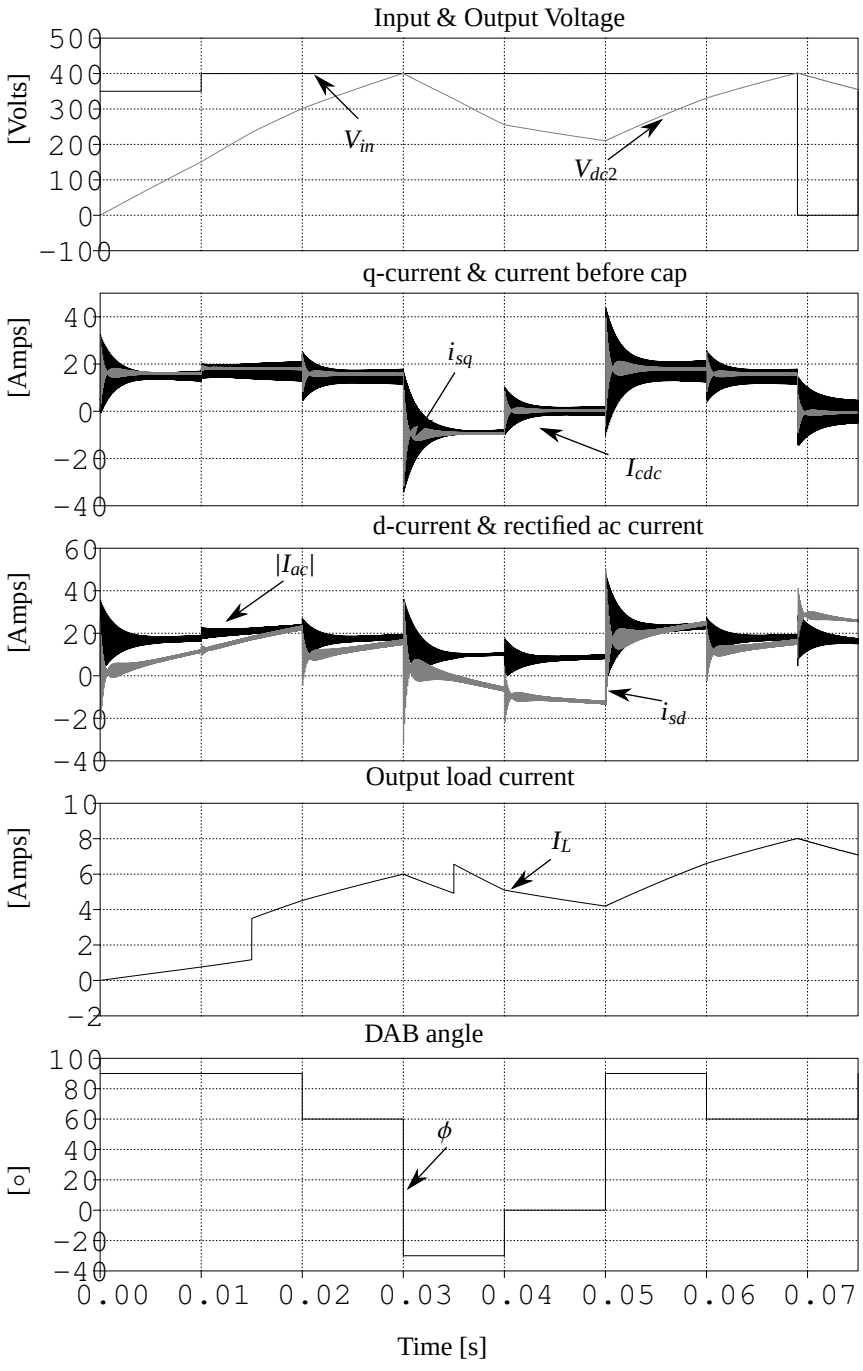


Figure 5.4: Simulation of the d-q transformation for resistive load at output

5.2.4 Vector Control Model of DAB

The Y:Y/Δ three phase DAB contains predominantly sinusoidal current can be modeled similar to the AFEC. The DAB AC current can be transformed using Park's transformation.

$$\underline{i}_s(t) = i_{s\alpha}(t) + j i_{s\beta}(t) \tag{5.4}$$

$$\underline{v}_s(t) = v_{s\alpha}(t) + j v_{s\beta}(t) \tag{5.5}$$

$$\underline{v}_r(t) = v_{r\alpha}(t) + j v_{r\beta}(t) \tag{5.6}$$

$$\underline{v}_s(t) = R_s \underline{i}_s(t) + L_s \frac{d\underline{i}_s(t)}{dt} + \underline{v}_r(t) \tag{5.7}$$

Space-vector variables are resultant of $\alpha - \beta$ phase quantities are shown in Eqs. 5.4, 5.5 and 5.6. Eq. 5.7 shows the simplified space-vector DAB dynamic relation.

$$\underline{i}_s(t) = [i_{sq}(t) + j i_{sd}(t)] e^{j\omega_s(t)} \tag{5.8}$$

$$i_{sq}(t) = i_{s\alpha}(t)\cos[\omega_s t] + i_{s\beta}(t)\sin[\omega_s t] \tag{5.9}$$

$$i_{sd}(t) = i_{s\beta}(t)\cos[\omega_s t] - i_{s\alpha}(t)\sin[\omega_s t] \tag{5.10}$$

In synchronously rotating frame with frequency ω_s aligned to the secondary converter voltage vector, the DAB current can be transformed into two components real (i_{sq}) and reactive (i_{sd}) in Eqs. 5.8, 5.9 and 5.10. In the d-q frame, the DAB voltage equation can be written as in Eqs. 5.11 and 5.12. There are cross coupling terms which can be canceled using feed forward terms.

$$v_{sq}(t) = R_s \underline{i}_{sq}(t) + L_s \frac{d\underline{i}_{sq}(t)}{dt} - L_s i_{sd} \omega_s + v_{rq} \tag{5.11}$$

$$v_{sd}(t) = R_s \underline{i}_{sd}(t) + L_s \frac{d\underline{i}_{sd}(t)}{dt} + L_s i_{sq} \omega_s \tag{5.12}$$

For the purpose of the control, the d-axis and q-axis currents must be controlled independently. The presence of the terms containing i_{sq} in v_{sd} equation and i_{sd} in v_{sq} equation indicates cross coupling. Hence we need to add the decoupling terms shown in Eq. 5.13 and 5.14 to the output of PI controllers in feed-forward.

$$v_{sqx} = \frac{V_{rq}}{G} - \frac{L_s \omega i_{sd}(t)}{G} \tag{5.13}$$

$$v_{sdx} = \frac{L_s \omega i_{sq}(t)}{G} \tag{5.14}$$

where G is the gain of the converter.

After adding the above feed-forward components in the control circuit, the currents i_{sd} and i_{sq}, are

completely decoupled and entirely depend upon the voltages v_{sd} and v_{sq} respectively.

5.3 D-Q Mode Control

Fig. 5.5 shows the improved block diagram for the d-q vector control of three phase DAB [80, 49]. The predominantly sinusoidal nature of the DAB currents for this topology, makes it possible to extract real component (dc in nature) and use it for feedback. Other methods to find the real component from DAB currents, for example, DAB output current preceding to dc capacitor or the rectified signal from DAB currents, have dominant 6^{th} and 12^{th} harmonics [68]. The controller generates the gate-pulses for two-level converters as reference-vector and phase-shifts the gate-pulses of primary-side converter for DAB operation. Hence it is simple to use the reference-vector generated sine and cosine signals readily available in the controller, to transform the DAB currents in d-q frame. One outer voltage loop is used to regulate the V_{dc2} at V^*_{dc2} setting. The PI current-controllers might generate step-change in phase-angle of the DAB during transients resulting in exponentially decaying dc error in DAB currents. One such study is on instantaneous current control proposed in [38]. This dc component causes oscillation in dc output current and also d-q currents. But it is possible to use a high-pass filter after sensed DAB currents and then transform them into d-q frame to remove oscillations. An internal d-q current loop enables fast response and provides another safety level for the over-currents. The d-q control ensures that the switch currents do not exceed the limit in transient-conditions. The controller generates the three-level side gate-pulses by comparing v^*_{abc} with duty-ratio information v^*_{comp}. Fig. 5.6 shows the PWM generation in the controller for three level and secondary two level devices by comparing sinusoidal references with a dc level representing duty ratio. The controller generates fixed phase pulses for reference two-level converters and shifts the pulses of primary-side converter for power-transfer. The reference generated sine and cosine signals are used to transform the DAB-currents into d-q currents for feedback. For NPC three level leg, s_1, s_3 and s_2, s_4 gate pairs are complementary. The v^*_{comp} of NPC converter comes from the reference voltage v^*_{abc} magnitude fed to a linearizing look up table (LUT) shown in Fig. 5.7 similar to [87]. The simulation for this topology which consists of a-phase converter voltages and currents for each of $Y-HV, \Delta-LV \& Y-L$V sides respectively has been shown in Fig. 2.7.

$$v_{comp} = \frac{2}{3} v_{dq} \sqrt{1 - (\pi \frac{v_{fund}}{4})^2} \tag{5.15}$$

$$v_{abc} = \frac{2}{3} v_{dq} = \pi \frac{v_{fund}}{4} \tag{5.16}$$

Eqs. 5.15 and 5.16 give the relation of comparator voltage level, the d-q reference magnitude and fundamental content of the pole output voltage. It is used to prepare the table. The LUT block is tested for linearity of input and fundamental output.

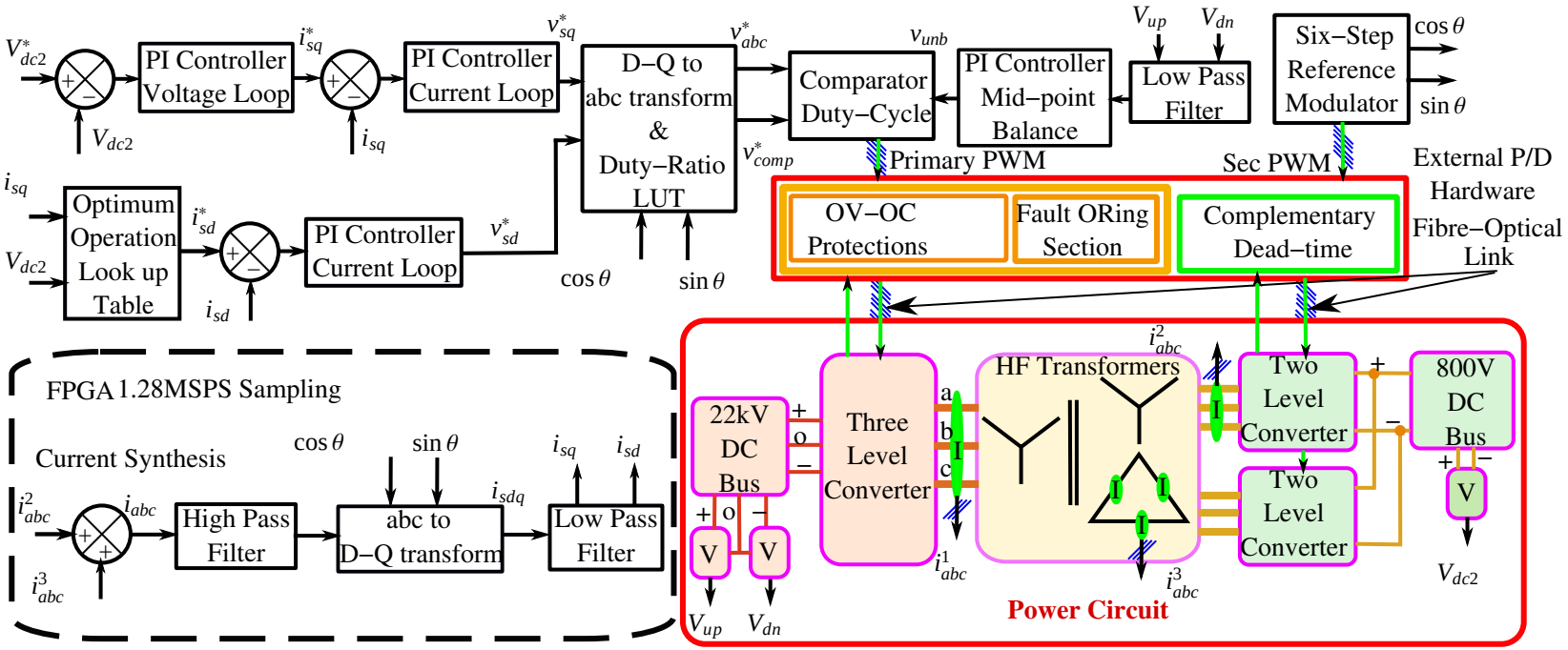


Figure 5.5: Control block diagram for d-q control of DAB

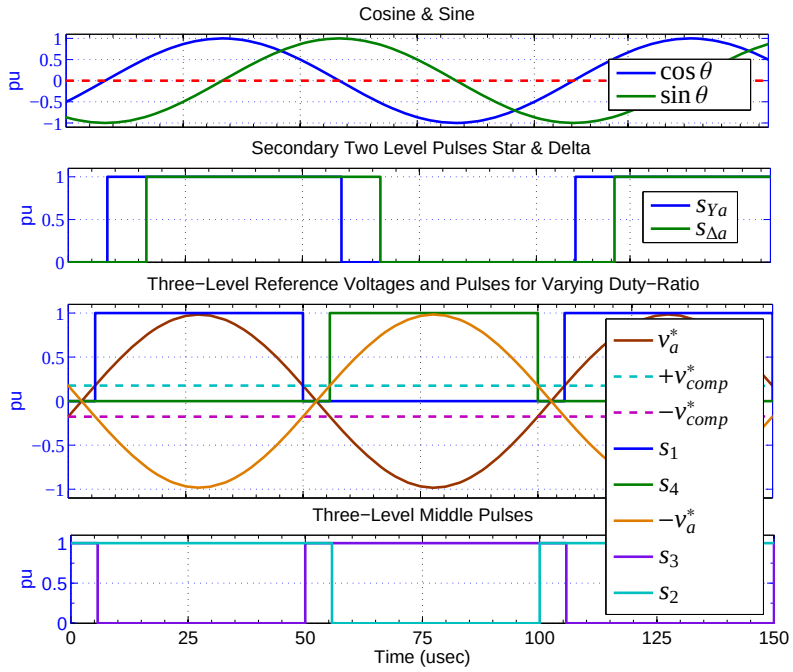


Figure 5.6: Modulation scheme of three phase DAB

The ΔV_{dc2} error is fed to a PI controller which generates i_{sq}^*. The i_{sd}^* is generated from a look up table which is a function of i_{sq}^* and V_{dc2} for optimum operation trajectory calculated analytically [88, 81, 89]. The optimum operation is the one that ensures ZVS condition keeping minimum reactive power flow in the DAB magnetics. This matches to the highest efficiency as well. The Δi_{sq} and Δi_{sq} errors are fed to inner PI controllers which generate the v_{sq}^* and v_{sd}^*. The primary current ringing due to parasitics may affect the control loop. With the distorted primary currents in presence of transformer parasitic components, there are two methods to get rid of ringing without filtering the signal,

1. Harmonic current extraction based on approximate model of transformer input section
2. Sensing star delta currents at the secondary and adding them to emulate the MV current with secondary currents and estimated magnetizing current.

Second method is simple to implement since it is not much dependent on input parasitics. Though it does not contain magnetizing current (i_m) and hence there is an error in the actual d-q current flowing from the primary side. The i_m is easier to estimate with a simple model and can be added to the sensed currents to solve this issue. Fig. 5.2 shows the space vector phasor diagram for the DAB. The ZVS range shrinks for three level converter ($< 50\% D$), smaller magnetizing inductance, dead time of converters, ringing currents and light loading of the DAB. d-q control ensures ZVS operation of DAB, as it can maintain i_{sd} independent of i_{sq} by adjusting duty ratio of primary converter and hence controlling primary voltage

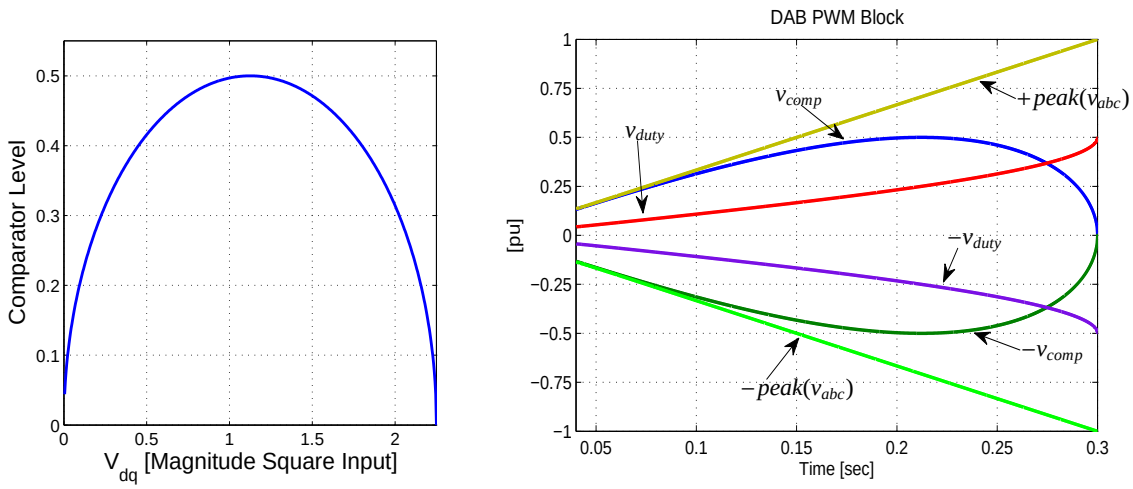


Figure 5.7: Modulation scheme of three phase DAB

magnitude [86, 90]. To calculate the optimum current lag angle for DAB current, device switching characteristics are taken in to consideration along with reactive power. SiC IGBT turn off losses can be high, hence the current lag angle should be limited. For minimum ZVS lag angle, a margin for parasitic currents and dead time are added to the converter zero state angle [82]. Hence the controller specifications can be summarized as below,

1. 12 Digital/PWM Output with external complementary board implementing dead-time
2. Converting 3 10 kHz current signals at 2 MSPS
3. Converting 2 MV sensor signal and 1 ouput LV sensor voltage signal
4. Additional 2 digital input and 2 output for fault and on/off signals
5. 2 PI controller for current and 1 for voltage
6. Cosine and Sine generation with look up table (LUT)
7. d-q transformation block to generate i_{sq} & i_{sd} currents
8. Inverse d-q transformation block to generate v^*_{abc}
9. 3 High pass filter for currents and 3 low pass filters for voltages

In a control program, a DSP sequentially processes commands with infinite loop [91]. The above control blocks add up to a large delay. Thus the reference commands can not be updated quickly, which limits the bandwidth of current controllers which are desirable in order of 5krad/sec. This needs loop T_s around 2µs for accurate discrete representation. The DSPs also have limited PWM control registers

which is another limitation [91]. Therefore an FPGA is better suited for this complex DAB application. However an interface board with fast ADCs and Diff-amps is required [92, 93]. A DE2 prototyping board from ALTERA based on cyclone II FPGA with on-board 50 MHz/27 MHz clocks for timing (counter) has been used for control implementation [92]. It has two 40 pin expansion headers, toggle switches and LED indications [94]. A parallel ADC ADS7865 is able to fetch the converted digital result at 2 MSPS [95]. The available general purpose input output (GPIO) are 72 in used FPGA kit, and two set of 12 bit parallel bus has been used to interface 4 ADCs using chip select pin.

5.4 DAB Transfer-Function Modeling with Transformer Parasitics

The DAB input voltage is 22 kV dc and output dc bus is regulated with feedback at 800 V rated for 100 kW of power. The real component of d-q transformed high-frequency current (i_{sq}) is used as inner current loop along-with outer voltage loop. Fig. 4.12 shows the exact equivalent circuit of DAB system with transformer parasitics parameters. Table 4.1 shows the measured values of transformer and inductor parameters in relation to Fig. 4.12. It is used to calculate the transfer function for i_{sq} current to phase-angle control. This circuit can be simplified by ignoring secondary capacitance and representing secondary with one equivalent source and equivalent inductance. The simplified schematic is shown in

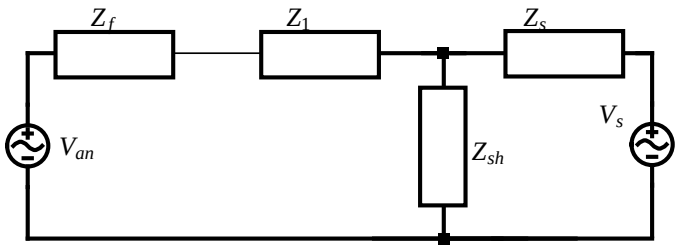


Figure 5.8: Simplified single-phase equivalent circuit of Y:Y/Δ DAB

Fig. 5.8. The inductance L_s is half the total inductance of star and delta paths separately. Here L_w can be ignored as it is relatively small value. It is followed by further simplified step by step to calculate the series equivalent impedance (Z_{tie}) of DAB for power-transfer in frequency domain. Voltage error caused by phase-angle between primary and secondary will drop across this impedance and generate DAB current. Real power transferred to secondary is given by Eq. 2.4. Here (Z_{tie}) has impedance angle θ and control-angle is ϕ.

$$\frac{\partial i_{sq}}{\partial \phi} = \frac{v_s}{|Z_{tie}|} \sin(\theta - \phi_0) \tag{5.17}$$

Eq. 5.17 shows the plant gain (real component of current to control angle) at steady state operating point angle (ϕ_0). As the transfer function depends on the nominal operating phase-angle, it can be

calculated for 50% load. Eq. 5.18 shows the total shunt impedance of the equivalent circuit in Fig. 4.12. Eq. 5.19 shows the filter impedance and Eq. 5.20 shows the transformer primary series impedance. Eq. 5.21 shows the Thevenin's impedance of primary circuit coupling to the secondary. Eq. 5.22 shows the Thevenin's voltage where v_s is the voltage error at angle ϕ_0 and Eq. 5.24 the DAB total series tie impedance. Transfer function of the real current to control phase-change is the multiplication of terms in Eq. 5.22 to the inverse of Eq. 5.25 for a given steady state control angle (ϕ_0).

$$Z_{sh} = \frac{1}{\frac{1}{sL_m} + s(C_p + C_m) + \frac{1}{R_c}} \tag{5.18}$$

$$Z_f = \frac{1}{\frac{1}{sL_{f1}} + \frac{1}{R_{df1}}} \tag{5.19}$$

$$Z_1 = \frac{1}{\frac{1}{sL_1} + sC_1 + \frac{1}{R_2}} \tag{5.20}$$

$$Z_{th} = \frac{1}{\frac{1}{Zsh} + \frac{1}{Z_f + Z_1}} \tag{5.21}$$

$$v_s = v_s^* \frac{Z_{sh}}{Z_{sh} + Z_f + Z_1} \tag{5.22}$$

$$Z_s = N^2[sL_2 + R_2] \tag{5.23}$$

$$Z_{tie} = Z_{th} + Z_s \tag{5.24}$$

$$F_z = \frac{1}{Z_{tie}} \tag{5.25}$$

Fig. 5.9 shows the Laplace domain transfer function ($\frac{\partial i_{sq}}{\partial \phi}(s)$) considering the DAB equivalent circuit with parasitics. It is obtained by simplifying the input side into a Thevenin's circuit (E_{th}, Z_{th}), which interacts with the Z_{tie} behind v_r. It is clear that parasitics are affecting the plot after 1 Mrad/sec frequency while the DAB current control bandwidth is less than 10 krad/sec. Hence there is no considerable direct effect of parasitics on the controller design. The parameter values are taken from the real measurement values of transformer and inductors at the rated conditions. The prime objective is to visualize any effect of transformer parasitics on the control. The parasitic frequency due to transformer L_m and C_p is 18.5 kHz but it is in shunt connection and does not contribute in control transfer function as seen in the impedance plots separately. Other parasitic frequencies are much higher (> 2 Mrad/sec) than DAB switching frequency, do not play any significant role in controls and are ignored for current control design. The only major parasitic frequency is that caused by tie inductance and resistance which occurs at lower frequency (5 krad/sec). DAB current control bandwidth (4.8 krad/sec or 800 Hz) must be much smaller than half of 10 kHz (switching frequency). And voltage control bandwidth is chosen 798 rad/sec or 110 Hz much slower than inner current-loop. Fig. 5.10 shows the control design block-diagram

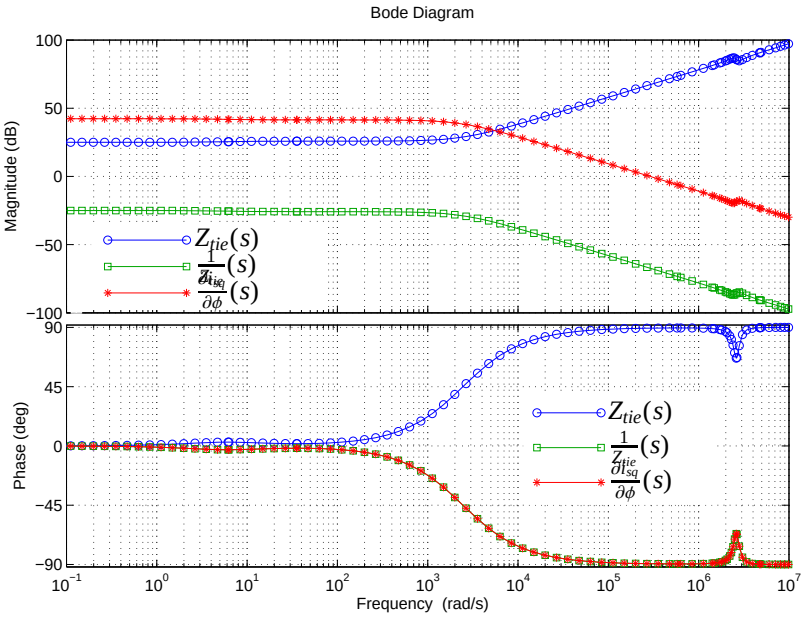


Figure 5.9: DAB transfer function with parasitics at rated condition

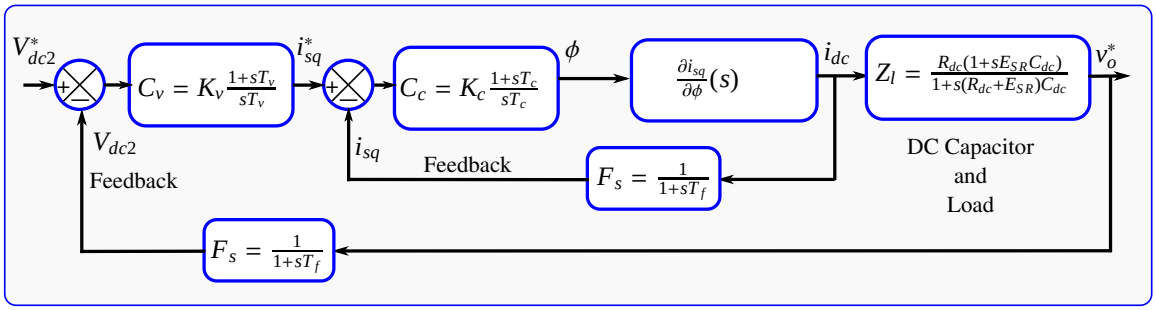


Figure 5.10: Block diagram for impedance transfer function calculation

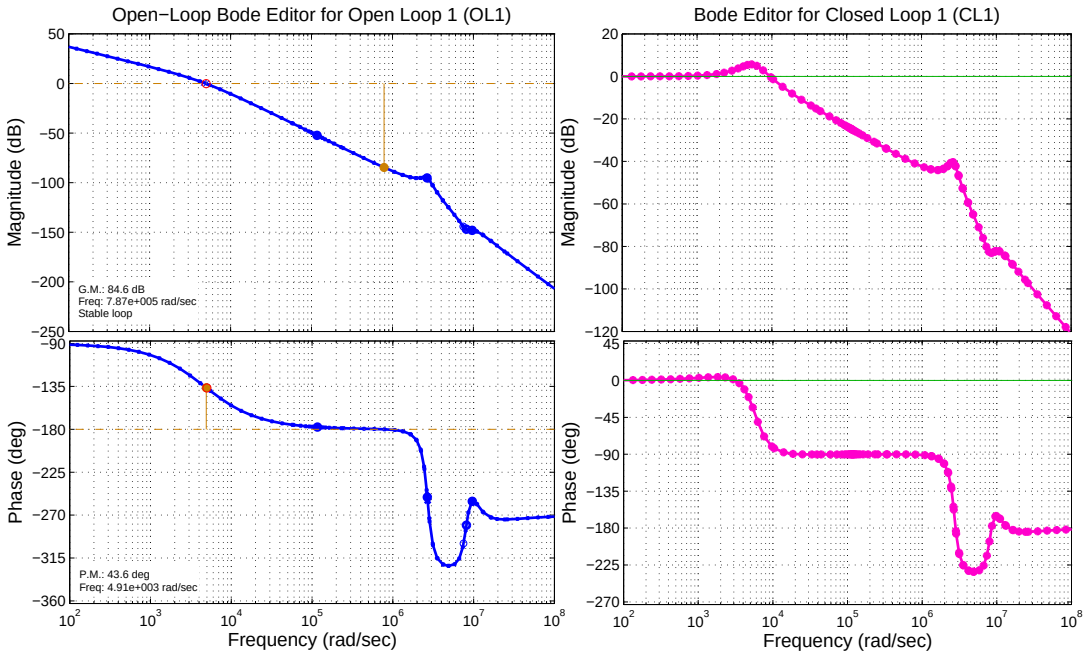


Figure 5.11: Current control design of the dual active bridge

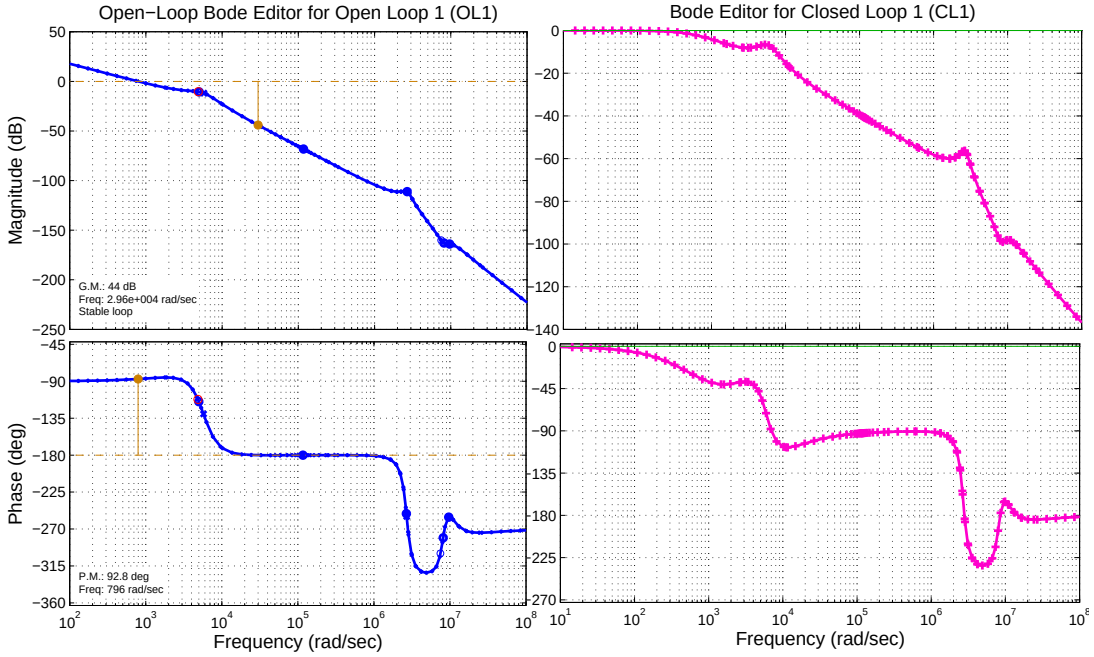


Figure 5.12: Voltage control design of the dual active bridge

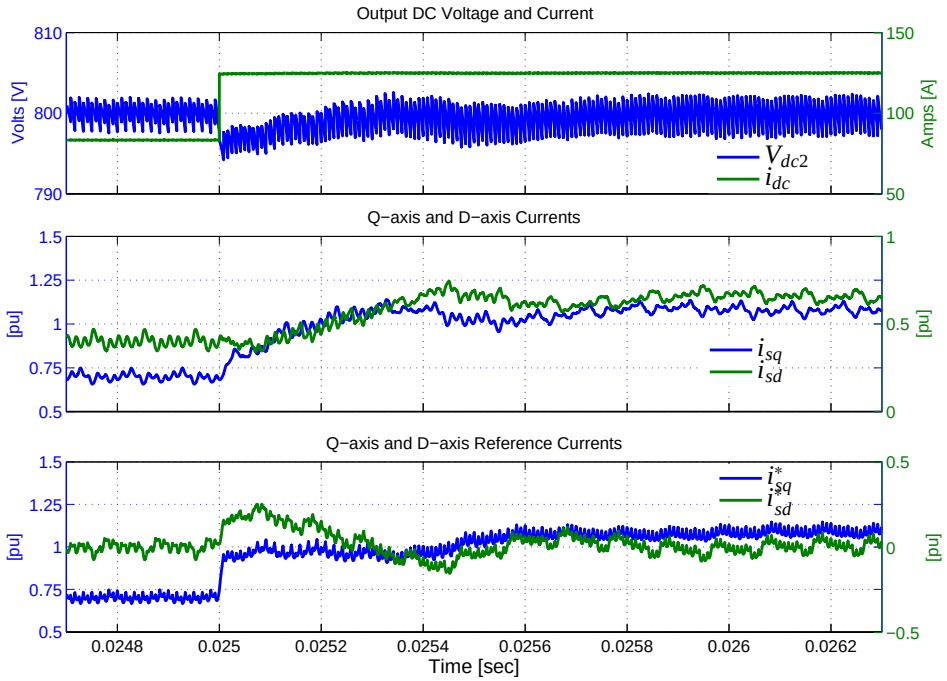


Figure 5.13: Transient results for DAB considering transformer parasitics

with current and output dc voltage feedback. Here (v_{in}) and (i_o) inputs are only used to compute DAB impedances reflected to cascaded converters and not for control design. Fig. 5.11 shows the open loop and closed loop transfer functions with current controller including transformer parasitics. It is evident that gain-margin and phase-margin do not depend on parasitics at higher frequencies as controller bandwidth and switching frequencies are much smaller and so they do not dictate the controller design. Fig. 5.12 shows the voltage controller design plots. The internal current loop is faster than the outer loop. The closed loop current control transfer function is considered as a plant transfer function in the design of the voltage control loop. The dc capacitor and 10% load resistance are the major parameters for this block. The bandwidth is kept 800 rad/sec which offers good gain and phase margins. Fig. 5.13 and Fig. 5.14 show the dc and ac simulation-waveforms for this control under load transient from 50 kW to 100 kW with parasitic of transformers considered. The i_{sq} has smaller ripple than the i_o and settles faster as discussed earlier. Secondary currents are cleaner than primary currents.

5.5 Interface Board Design

In addition to 6 high speed analog inputs, more sensing channels might be required for additional features such as flux balancing, temperature etc. ADS7865 can be configured for either 2 high speed channels or 4 half speed channels. With 72 GPIOs available on DE2 board and for sake of less complexity

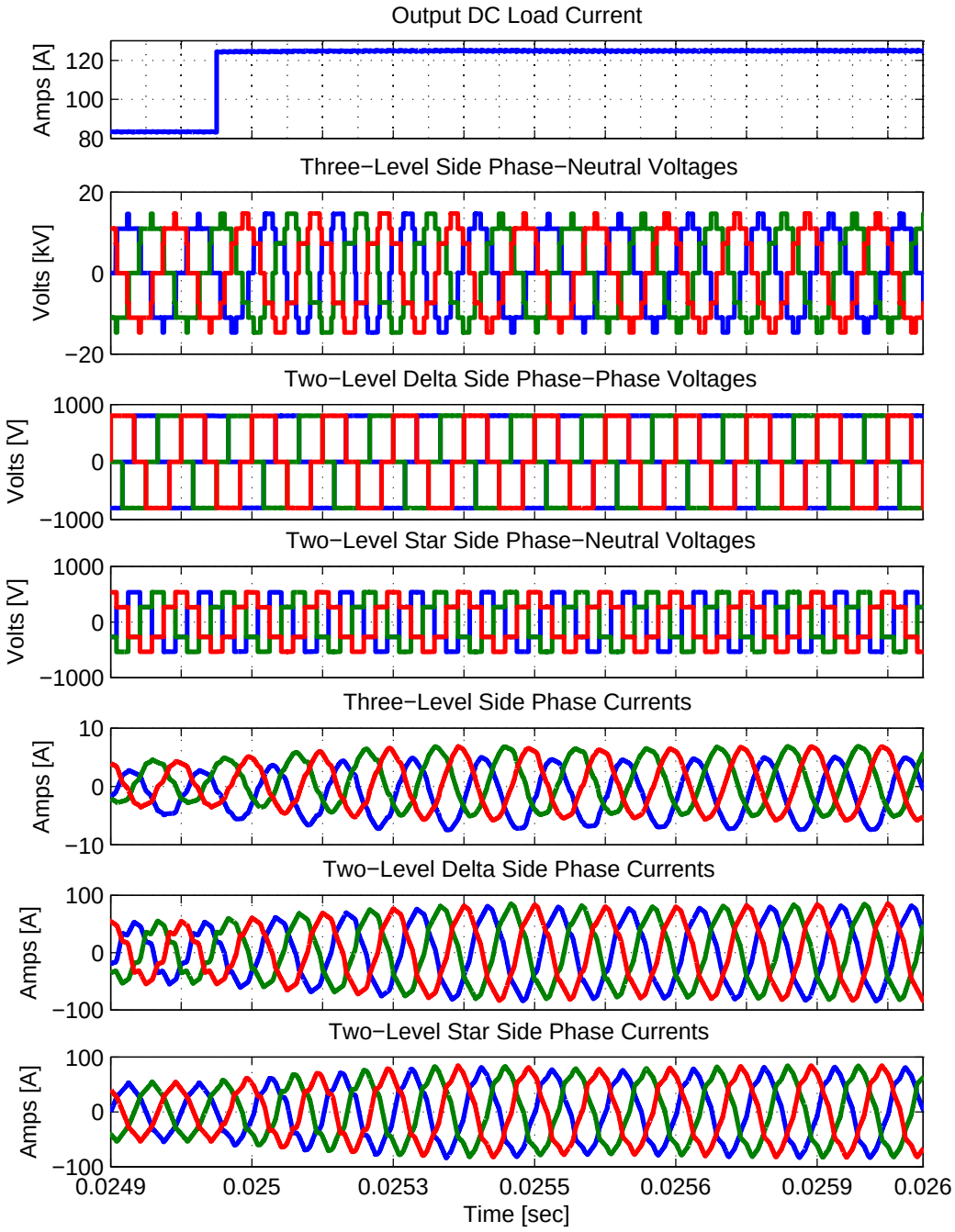


Figure 5.14: Transient results for DAB considering transformer parasitics

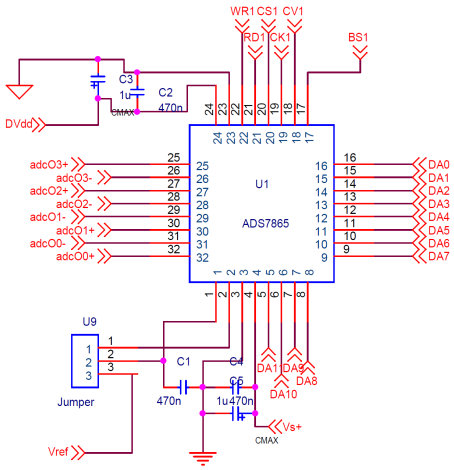


Figure 5.15: ADS7865 Schematic for the Interface Board

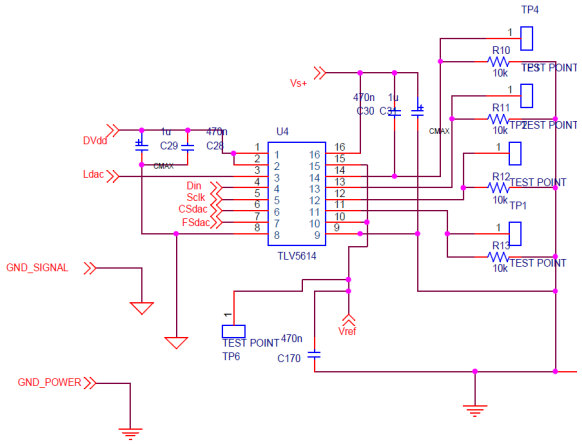


Figure 5.16: TLV5614 Schematic on Interface Board

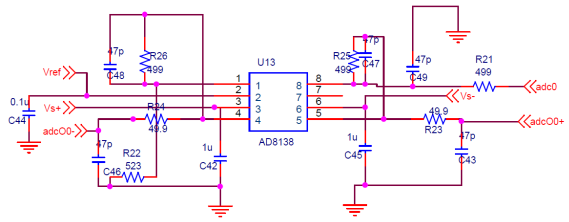


Figure 5.17: AD8138 Schematic on Interface Board

only 4 ADC ICs are used with 2 sets of parallel data bus for analog signals. Each ADC IC is fed with a clock signal CK, chip select CS, conversion start CV, write WR, read RD and a busy BS. One ADC pair is connected to the 12 bit data bus (DAs, DBs). Since the GPIOs in the FPGA can be used for PWM as well as peripheral interfacing, the DE2 board is sufficient to output all 24 gate signals for the DAB. Each ADC can fetch 2 conversion signals at 2 MSPS or 4 signals at 1 MSPS. Fig. 5.15 shows the schematic of the ADS7865 IC used in the interface board configured for differential input [95]. The reference voltage (2.5 V) for conversion can be given from external circuit. The analog section requires 5 V and the digital requires 3.3 V for operation. The analog inputs can be used as single-ended or differential depending on requirement. Fig. 5.16 shows the schematic of the DAC TLV5614 used in the interface board to probe 4 internal digital variables at a time with 330 kHz sampling [96]. It is used to debug and verify the implementation. It can be operated by a multiplexer with selection lines driven by constant which can be modified online with keyboard. It also requires analog and digital supply and reference voltage. The data is transferred serially from the FPGA board. The data-line required is just one but the speed gets limited. It can update 4 output channels one by one based on the selection data. Fig. 5.17 shows the differential op-amp AD8138 schematic used to nullify the CM noise [97]. The gain is kept unity. Since the analog signal comes from protection/dead-time (P/D) card, the op-amp input is used as single-ended. But the output driving the ADC is differential. Hence it cancels any CM noise generated by power converter.

5.6 Auxiliary Boards for Protection

Fig. 5.18 shows the P/D and ORing boards used for the MV DAB setup. The P/D board receives gate signals from the FPGA interface board and transfers back sensor signals received from individual sensors of the power circuit for A/D conversion. All the voltage and current sensors are from LEM. The current sensors LA 100-P has $< 1\,\mu s$ response time and voltage sensor LV 25-P has $40\,\mu s$ response time. The voltage sensors therefore limit the voltage loop bandwidth. The P/D board generates complementary gate pulses with defined dead time using RC pair and AND logic. It can also be generated directly from the controller. But the analog hardware based dead time and inversion is preferred due to reliability as the digital pins might go in unknown state when hung creating a shoot-through in the converter leg. The ORing board combines individual fault signals received from gate drivers of the MV converter switches and shuts down all three phase gate signals together in case of individual switch fault trips. Without this board there might be unbalanced three phase DAB operation which is not desirable.

5.7 FPGA Board Programming

Fig. 5.19 shows the fabricated interface circuit board. It has 16 diff-amp units, 1 DAC and 4 ADCs with required connectors. The timing information of the ADS7865 is shown in Fig. 5.20 taken from TI datasheet [96]. A low triggered conversion start (CV) signal starts the operation. After busy signal is off after

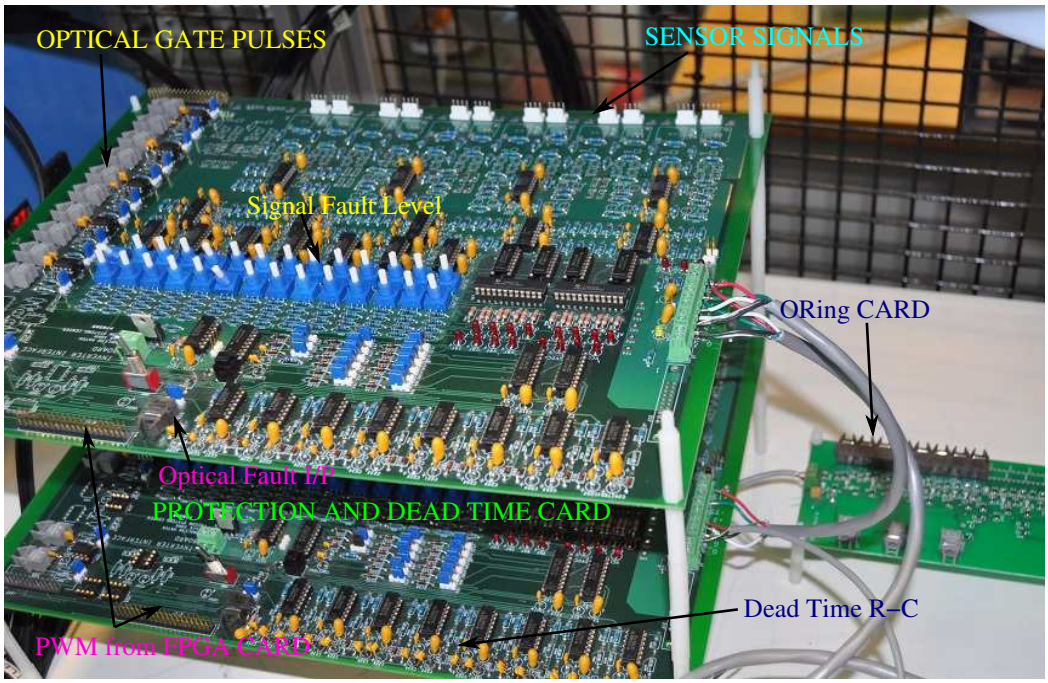


Figure 5.18: Final control hardware setup for Y:Y/Δ DAB

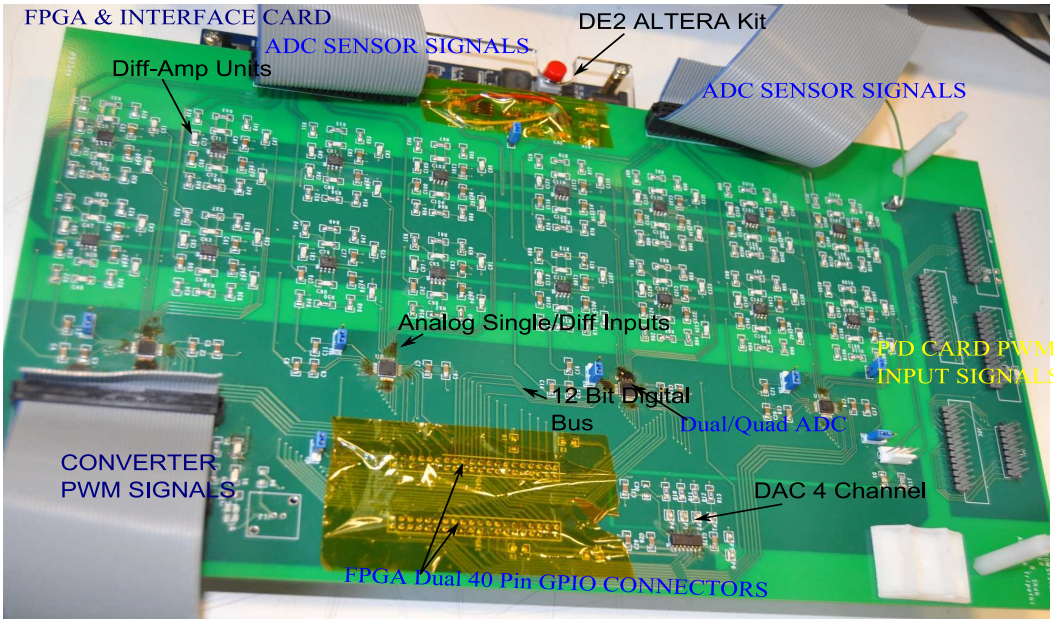


Figure 5.19: Fabricated Interface Board Photograph

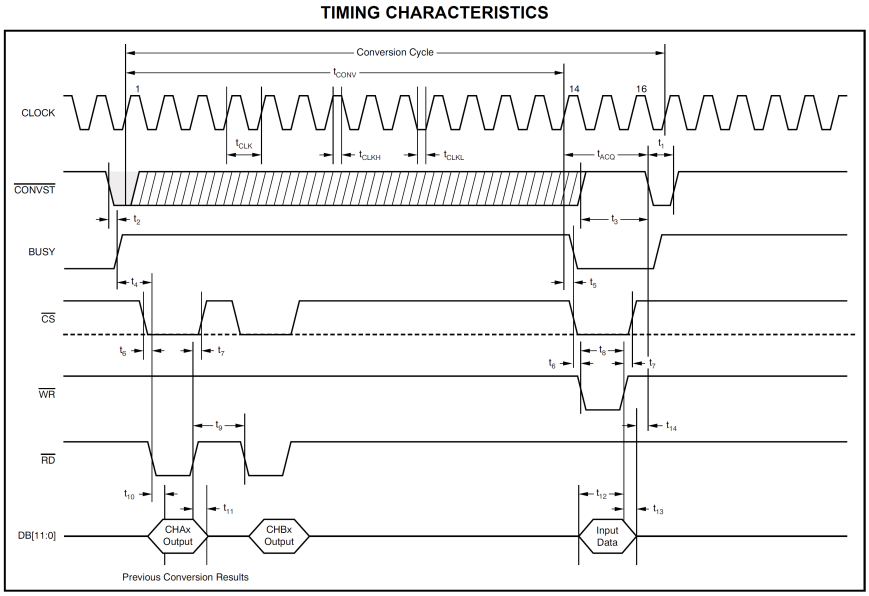


Figure 5.20: ADS7865 Timing Diagram (**Reproduced from datasheet)**

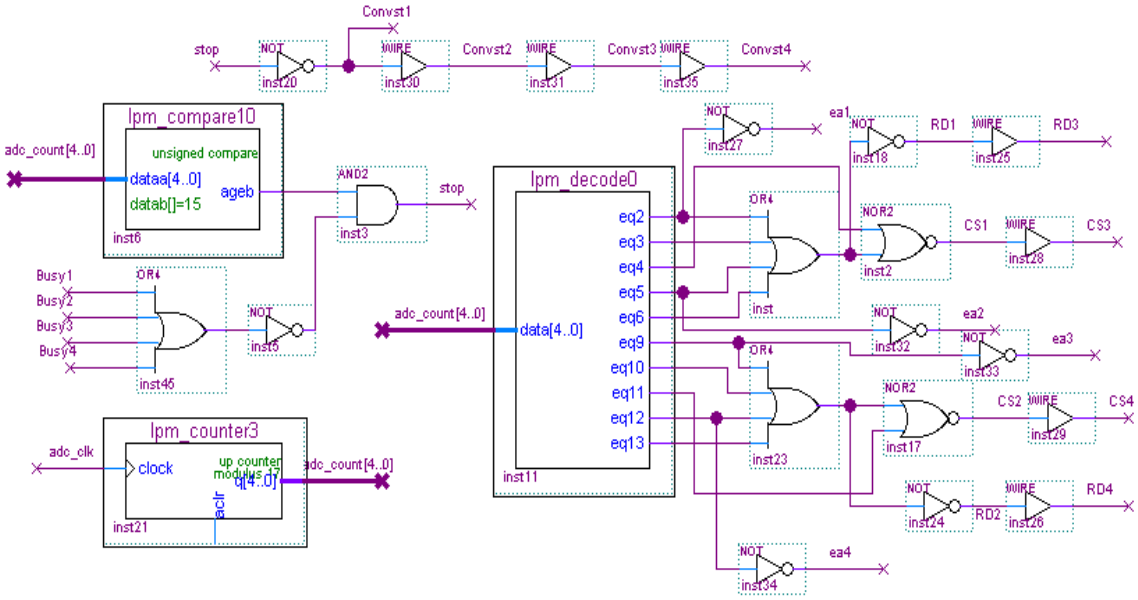


Figure 5.21: ADC Interfacing Program for the FPGA

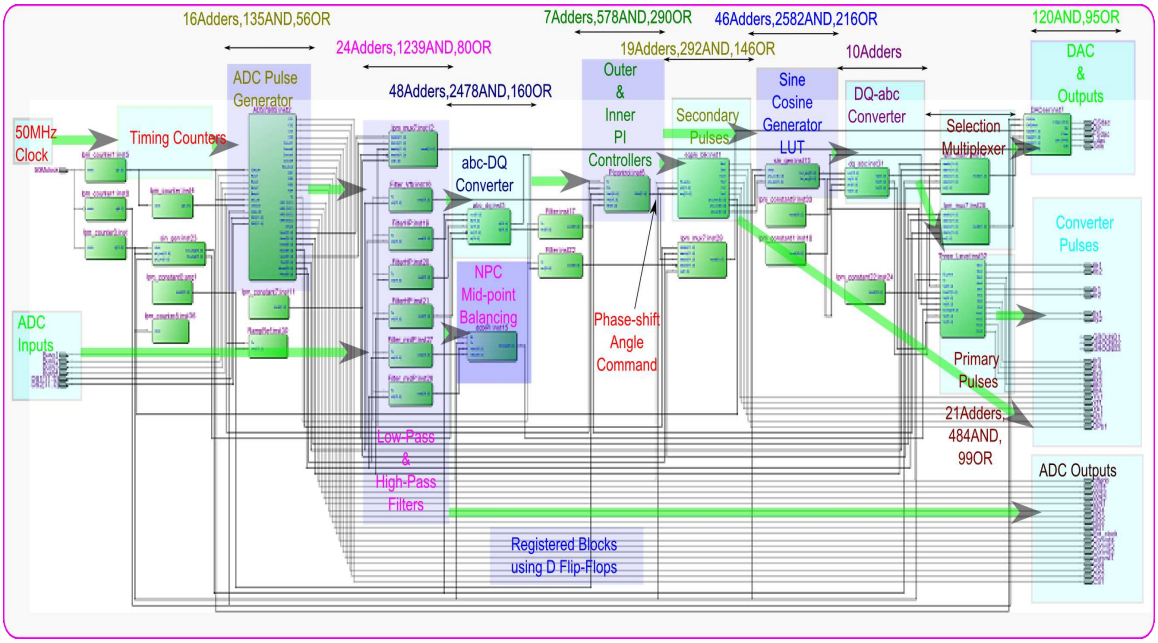


Figure 5.22: Quartus II FPGA Implementation RTL View of the Program

certain counts of the clock, the chip is selected (CS low) and data is read (RD low). First read fetches the first ADC result, the second read command fetches the second ADC result for the chip selected IC. This timing is generated using a counter, decoder and combinational logic as shown in Fig. 5.21. A modulus 17 up-counter repeats itself with 25 MHz clock. The CV is pulled down for last two counts which starts conversion operation for the next sampling. The present sampling data are read by generating CS and dual RD signals using the decoder. Inside the FPGA program, latch enable EAs are used to route the dual data to appropriate variables. The PI controllers are implemented with modified Euler equation for differentiation. The sampling time T_s and control time constant T_c selection along with proportional constant K_c are important for control bandwidth requirement. If the sampling speed which is same as the ADC sampling speed is not sufficiently small, a wider bandwidth can not be achieved due to too small integration constant value. (5.26) shows the time domain differential equation converted into discrete domain by first order Euler method. (5.27) represents the expression for digital integration derived from (5.26). (5.28) shows the PI controller expression in Laplace domain. (5.29) shows the integration part derived from (5.27). (5.30) shows the PI implementation for the FPGA.

$$\frac{dx_t}{dt} = y_t = \frac{x_{k+1} - x_k}{T_s} = y_k \tag{5.26}$$

$$x_{k+1} = x_k + T_s y_k \tag{5.27}$$

$$K_c[X_s + \frac{1}{sT_c}X_s] = K_c X_s + I_s = Y_s \tag{5.28}$$

Table 5.1: Quartus II Device Utilization

Parameters	Value[Units]
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	4,019 / 33,216 (12 %)
Total combinational functions	3,947 / 33,216 (12 %)
Dedicated logic registers	730 / 33,216 (2 %)
Total registers	730
Total pins	73 / 475 (15 %)
Total virtual pins	0
Total memory bits	40,960 / 483,840 (8 %)
Embedded Multiplier	
9-bit elements	36 / 70 (51 %)
Total PLLs	0 / 4 (0 %)

$$i_{k+1} = i_k + \frac{T_s K_c}{T_c} x_k \tag{5.29}$$

$$y_k = K_c x_k + i_k \tag{5.30}$$

Table 5.1 shows the compilation report with quartus II tool [98]. It summarizes the device utilization of the cyclone II FPGA. Even after implementation of all the discussed algorithm blocks mentioned earlier, the resource utilization is low. Fig. 5.22 shows RTL implementation of the program in terms of operators. Timing analysis of the implementation does not indicate any setup time or hold time violations which occur when a combinational circuit between two synchronous registers is too slow or too fast respectively. It would take 150 MHz DSP TMS320F28335, more than 26 µs to process the equivalent combinational functions, thus limiting the sampling time. Pipe-lining increases the throughput but it does not remove the delay in updating of the command for the sensed feedback.

5.8 Scaling of the MV-HF parasitics to LV prototype

The above discussed control is first verified in LV prototype before it is applied to actual MV-DAB. It is important to emulate the effect of the parasitics in LV prototype. The parasitics are scaled to LV TIPS prototype by per-unit and calculated lumped capacitances are added at winding ends similar to equivalent circuit. The LV 400 V-400 V, 4 kW prototype Y:Y/Δ DAB setup II shown in Fig. 5.23, has been used to verify controls under parasitic emulation of the MV-HF transformer. The ratings of the low voltage hardware are shown in Table 5.2. Scaling of design-parameters is important for estimation of

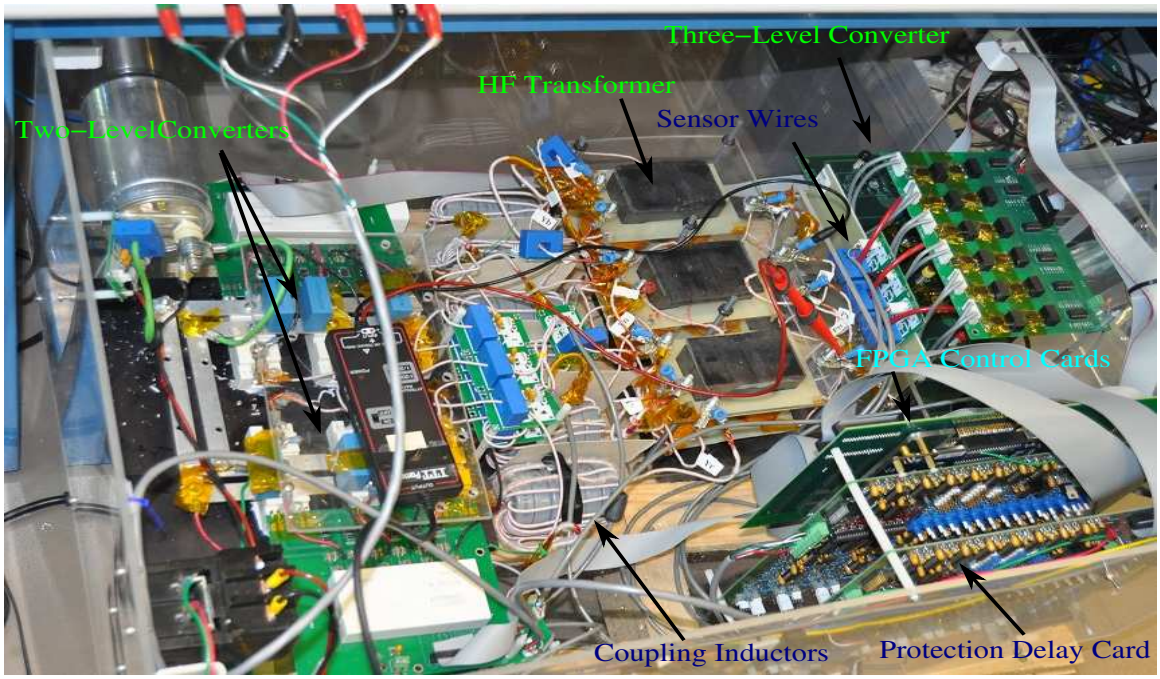


Figure 5.23: LV prototype hardware setup II for Y:Y/Δ DAB topology

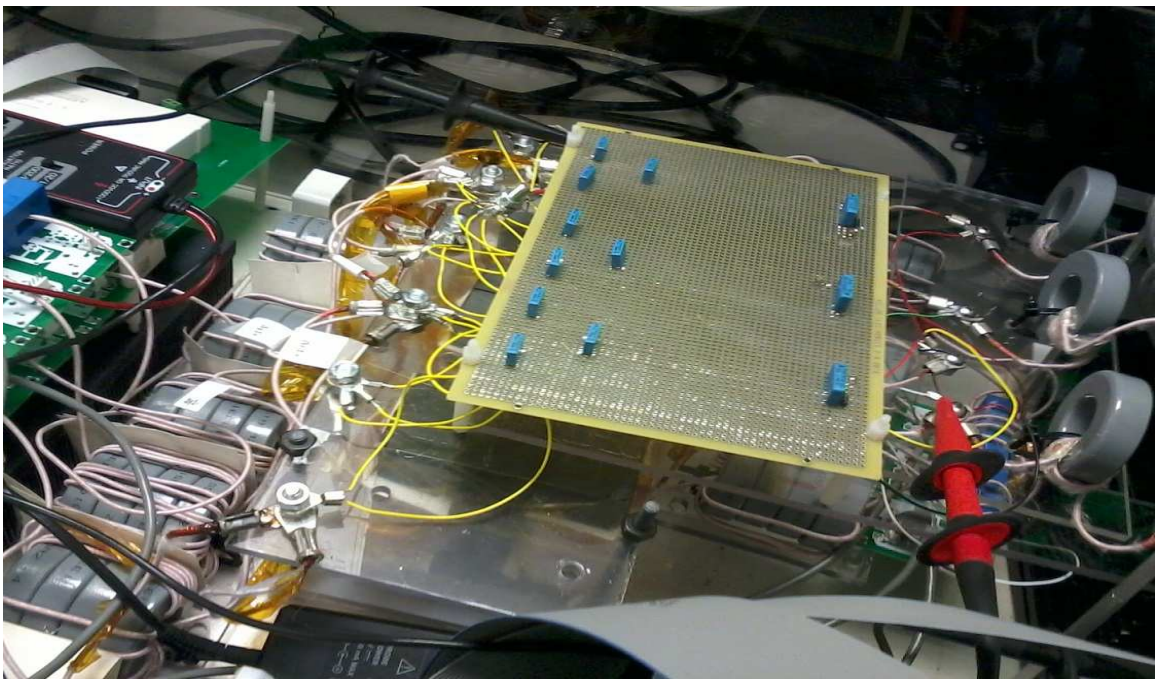


Figure 5.24: Photograph of MV-HF transformer parasitic emulation in LV prototype hardware setup II

Table 5.2: Parameters of the LV and MV experimental setup

Parameters	**LV Setup Value[Units]**	**HV Setup Value[Units]**
Input dc Voltage	400 V	3 kV
Output dc Voltage	400 V	200 V
Input side Duty-Ratio	41% *nominal*	41% *nominal*
DAB Inductance	400 μH	80 μH
Real Power Transfer	4 kW	5 kW
Switching-frequency	10 kHz	10 kHz

cost or feasibility issue for standardized three phase DAB. It also helps to emulate the parasitics of a MV-HF high power transformer of the DAB in a LV low power prototype lab setup and test the worst case performance and controls issues. The per unit method of scaling is widely used in power system design which also ensures that energy stored in parasitics to base power ratio remains same and has been verified in this chapter. It is scaled to a LV three phase DAB setup rated at 400 V-400 V dc, 4 kW and the scaled parameters are shown in Table 5.3. The rated power is selected as the base power. The rated

Table 5.3: Scaling of the parasitics to 400 V-400 V, 4 kW setup

Quantity	Value[Units]
Turn-ratio	$1 : \sqrt{3} : 1$
Primary inter-turn cap C_{p1}	4.7 nF
Secondary inter-turn cap C_{s1}	500 pF
Mutual between any two winding total C_{ps}	16.9 nF
Magnetization inductance (from primary)	3.11 mH, +/ − 10%
Core-loss equivalent resistance	53129 Ω
Total Leakage Inductance	1.59 μH, 0.013 Ω
External HV Inductance	4.67 μH, 0.005 Ω
External HV Damping Resistor	53.1 Ω
External LV Inductance	642 μH, 1.6 Ω
Input CM choke	3.18 mH
Output CM choke	0.74 mH
Input dc capacitor	49.7 μF

voltage for primary side and secondary side of transformer according to turn ratio are selected as base voltages for each side. Standard impedance equations are used to calculate base impedance which are

later used to divide the actual impedance values to get corresponding pu values. The per unit values for scaled system remains same for referencing to either side. It has to be multiplied with the base values to calculate the actual values. Eq. 5.31, 5.32 and 5.33 show the base parameter relations for one side that can also applied for other side. The scaled parasitic capacitance are higher than actual transformer parasitics of the LV setup hence external components are put at transformer as shown in Fig. 5.24.

$$Z_{b1} = \frac{V_{b1}^2}{P_1} \tag{5.31}$$

$$L_{b1} = \frac{Z_{b1}}{2\pi f_n} \tag{5.32}$$

$$C_{b1} = \frac{1}{2\pi f_n Z_{b1}} \tag{5.33}$$

5.9 Experimental Results

The LV setup is operated in closed loop control first without parasitic emulation and then after inserting the scaled components in the setup. Fig. 5.25 and Fig. 5.26 show the steady-state experimental waveforms without and with the parasitics. Fig. 5.27 and Fig. 5.28 show the experimental sudden load

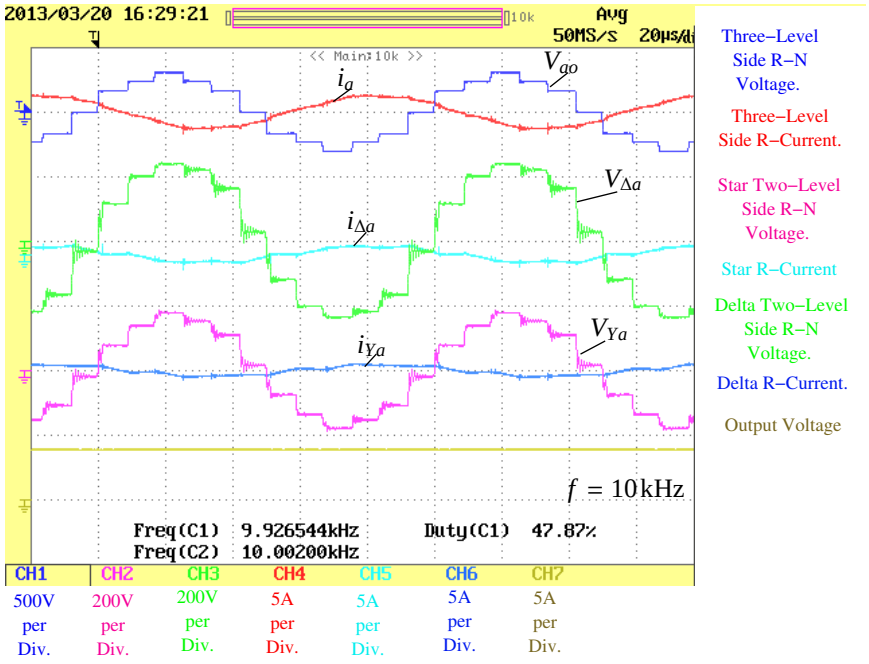


Figure 5.25: 400 V-400 V dc, 4 kW experiment results- steady state without parasitic

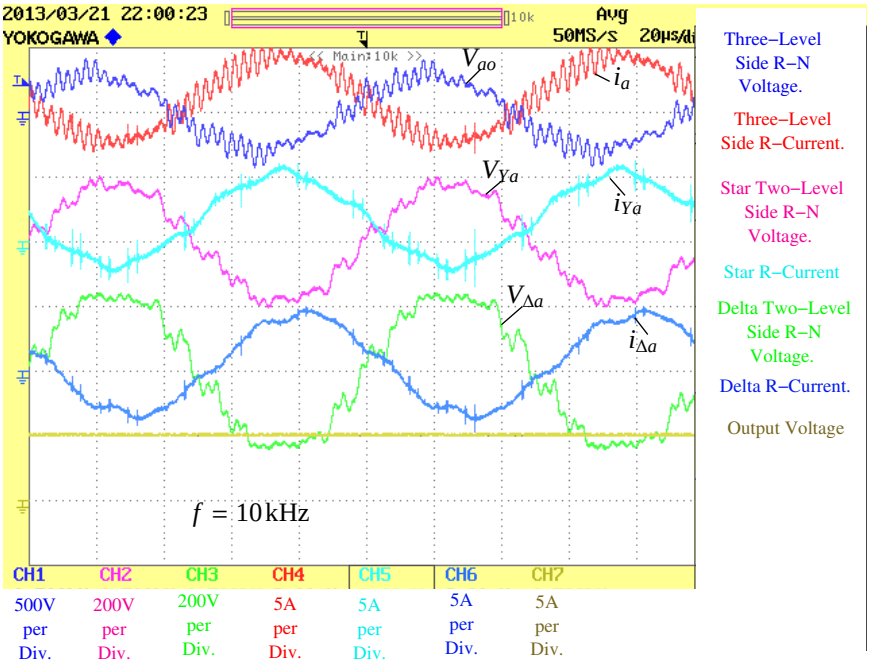


Figure 5.26: 400 V-400 V dc, 4 kW experiment results-steady state with parasitic

transient waveforms of transformer EMF, current and dc input-output voltages for the Y:Y/Δ setup at 250 V dc bus and full-load condition for without and with parasitic. The primary current gets distorted but control works well as can be seen from waveforms. The device parameter and dead-time mismatch may cause mid-point of three-level converter to unbalance, which is corrected by actively adjusting top and bottom device duty-ratios [99]. Fig. 5.29 shows the d-q currents for 400 V-400 V, 4 kW DAB operation. The fundamental frequency of current is 10 kHz which has to be sampled around 1.28 MSPS to calculate d-q current correctly. This has been implemented on a FPGA based controller board using ultra-fast ADCs as shown in Fig. 5.19. Primary converter pole voltage waveform is shown and found to be balanced with an active-balancing control loop [100]. Fig. 5.30 shows the MV-DAB setup-I using 15 kV/20 A, 2 µm buffer SiC IGBTs on MV, for rating shown in Table 5.2. Figs. 5.31 and 5.32 show converter result in different scales at 3kV-220V dc, 5 kW three-phase DAB operation with only a voltage control loop. The primary duty-ratio control for optimum current vector setting is not suitable for the 15 kV SiC-IGBT due to deterioration of current THD and reduction of ZVS range as presented later. Thus it is desirable to fix the duty-ratio of the three-level converter at primary at high-voltage to ensure ZVS and minimum THD in the transformer currents. After the duty-ratio of primary converter is fixed, phase-angle is the only control variable and it cannot control i_{sd}. The DAB currents have ringing as expected from simulation and emulation in the lower rating prototype. Fig. 5.33 shows the frequency spectra of the converter result. It shows 280 kHz ringing on the MV side and an additional 150 kHz

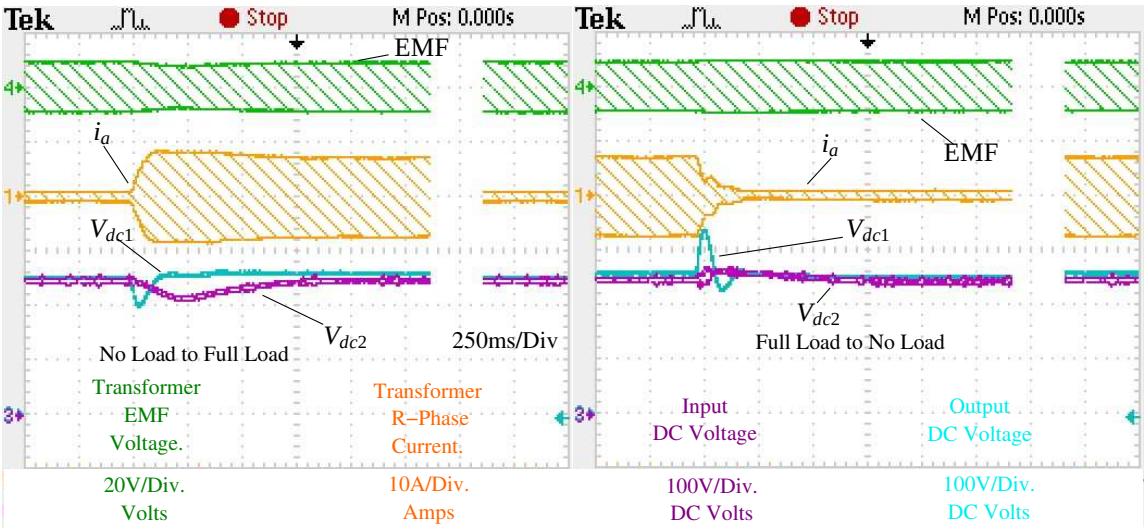


Figure 5.27: 250 V-250 V dc, 2 kW experiment results-transient without parasitic

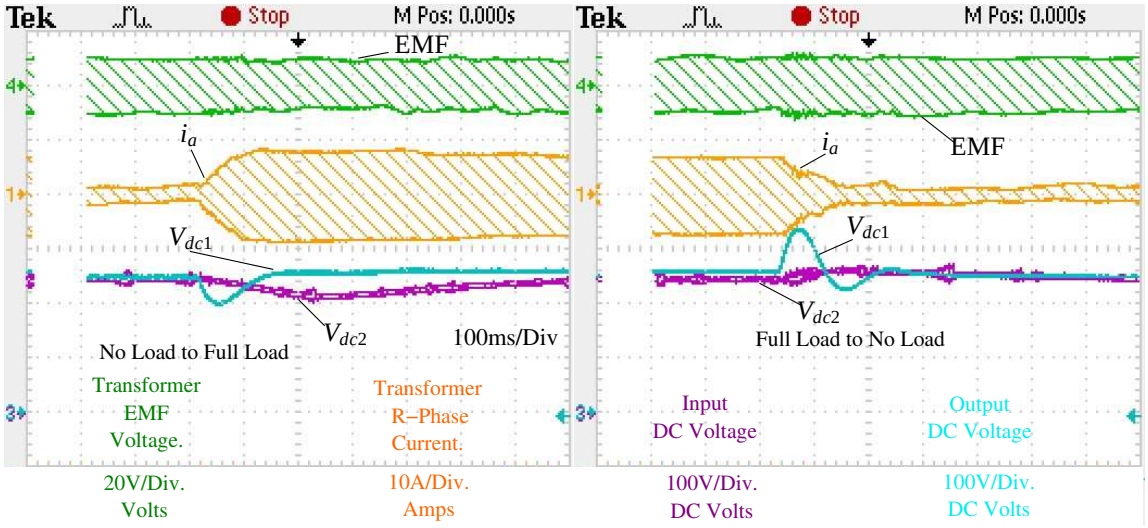


Figure 5.28: 250 V-250 V dc, 2 kW experiment results-transient with parasitic

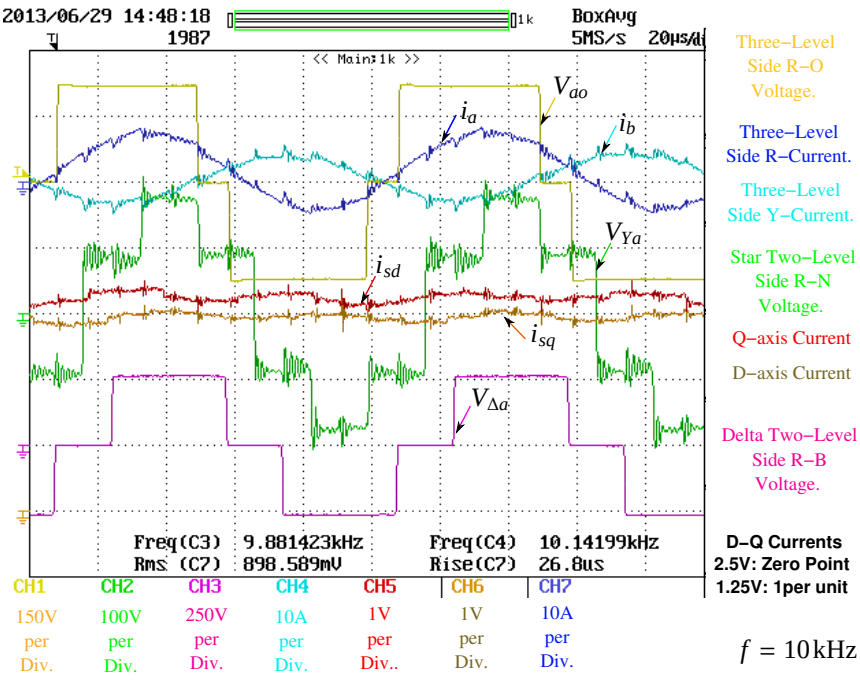


Figure 5.29: DAB d-q currents calculated from sensed currents

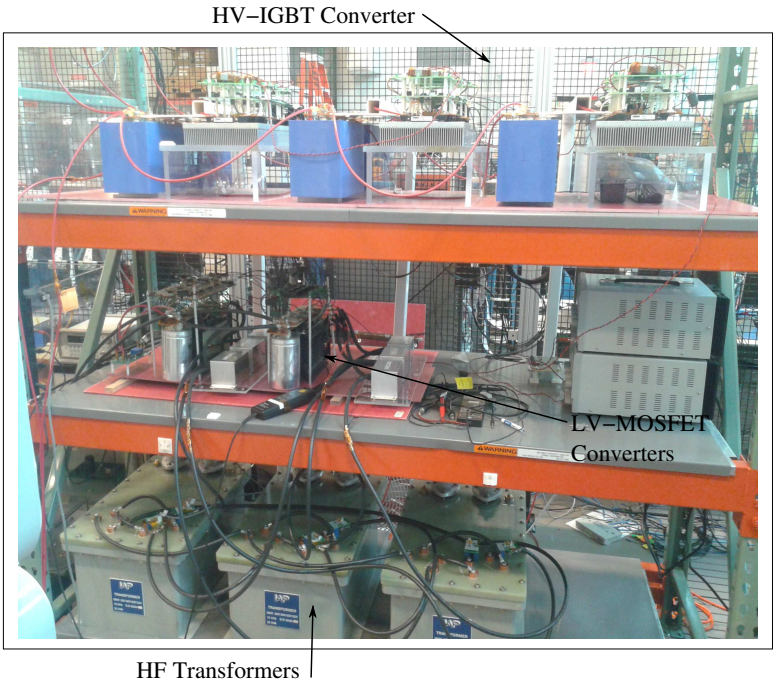


Figure 5.30: MV hardware set-up I for 100 kW Y:Y/Δ DAB topology

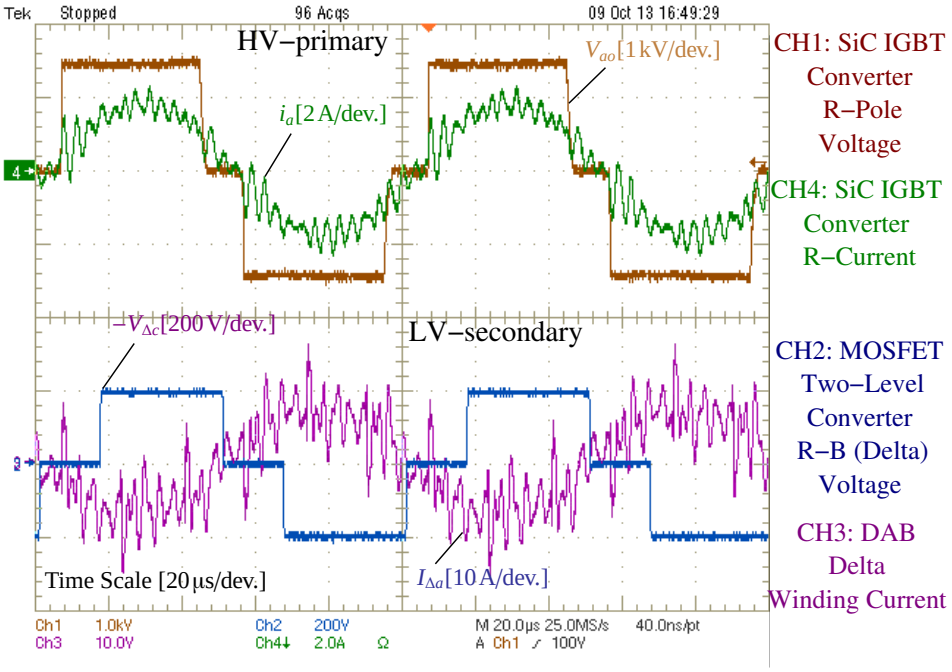


Figure 5.31: Y:Y/Δ DAB converter result at 3 kV-220 V dc, 5 kW

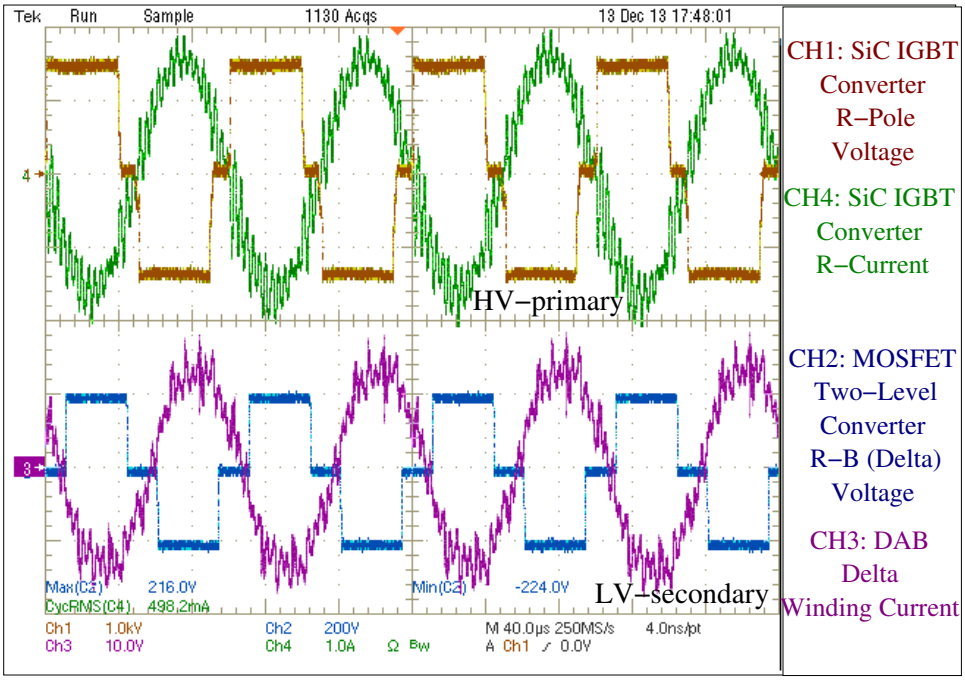


Figure 5.32: Y:Y/Δ DAB converter result at 3 kV-220 V dc, 5 kW

component on the LV side currents.

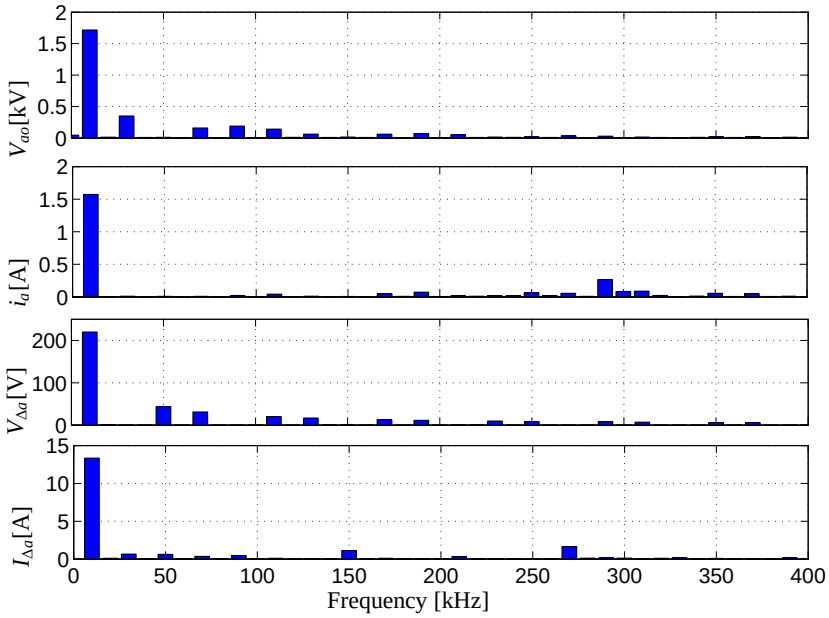


Figure 5.33: Y:Y/Δ DAB FFT of the waveforms at 3 kV-220 V dc, 5 kW

5.10 Conclusion

Parasitics do not directly affect the control performance as verified by the DAB model and controller designs. The sinusoidal DAB current and three-level duty-ratio control make d-q control suitable for 15 kV SiC-IGBT based MV DAB ensuring optimum performance. To ensure ZVS, i_{sd} reference is generated from i_{sq} such that i_s vector aligns with optimum trajectory. This FPGA based d-q control operating with 1.28 MSPS loop sampling combined with 12 pulse primary control helps achieve faster response time. This method is comparable to some of the fastest DAB current control methods. The energy stored in the reactive elements to base power ratio depends only on frequency which is constant. So this is conserved in the scaling study and proves to be reasonable. The parasitic emulation in LV setup produces experimental steady and transient results same as the HV simulation results. The device parasitics combined with transformer parasitic cause voltage imbalance in the NPC converter mid-point which has been solved and validated with experimental result using feed-forward duty control. The d-q currents has some low-frequency component due to unbalanced current measurements that can be improved with sensor correction. The 3 kV results, with only voltage feedback, are similar to that expected from simulation for ringing, steady-state and ZVS.

Chapter 6

Final Medium-Voltage DAB Hardware Development

6.1 Introduction

The 15kV SiC IGBT based three-level topology enables a non-cascaded MV DAB as discussed earlier. The NPC three-level pole is used to support 22kV MV dc bus rating. This chapter presents the final hardware development of the medium voltage (MV) DAB converter system for lab demonstration rated up to 14kV. This chapter shows the used device 15kV SiC IGBT and 1200V SiC MOSFET switching characteristics earlier presented in [41, 101]. The MV gate-driver is also shown for comparison later with intelligent MV gate-driver. The neutral-point diode clamping (NPC) three-level converter pole built using these devices are presented with experimental results up to 10kV. The LV MOSFET converters are qualified in earlier work [101]. The main motivation of using HF transformer is to reduce the magnetic size. The non-ZVS NPC pole switching loss analysis is also presented. The DAB main setup arrangement, wiring, transformer connections, load-bank and HV sensor are also explained with their associated test results.

6.2 15kV SiC IGBT Switching Characteristics

The MV gate-driver as shown in Fig. 6.1 with isolation cap of 4pF is designed and presented in [44]. The challenges for a 15kV SiC IGBT gate-driver (GD) design are the high-voltage isolation and high dv/dt (30kV/µs) EMI immunity [41, 40]. A suitable such basic MV GD with < 4pF isolation capacitance power-supply is presented previously in [44]. The driving and desat function is supported by a 2.5Amp AVAGO driver with integrated (Vce) desat detection and fault status feedback [44].

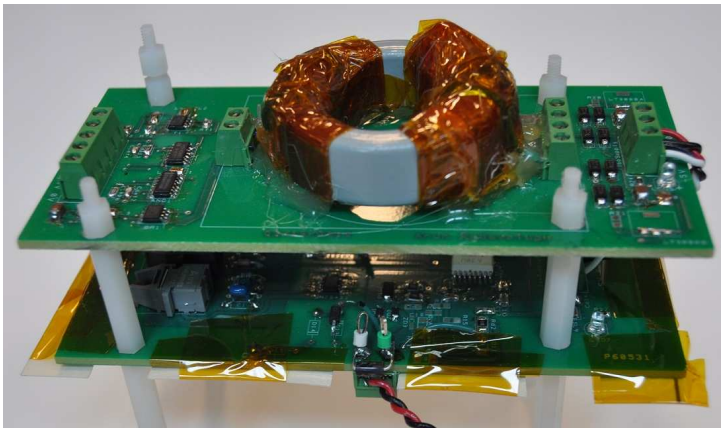


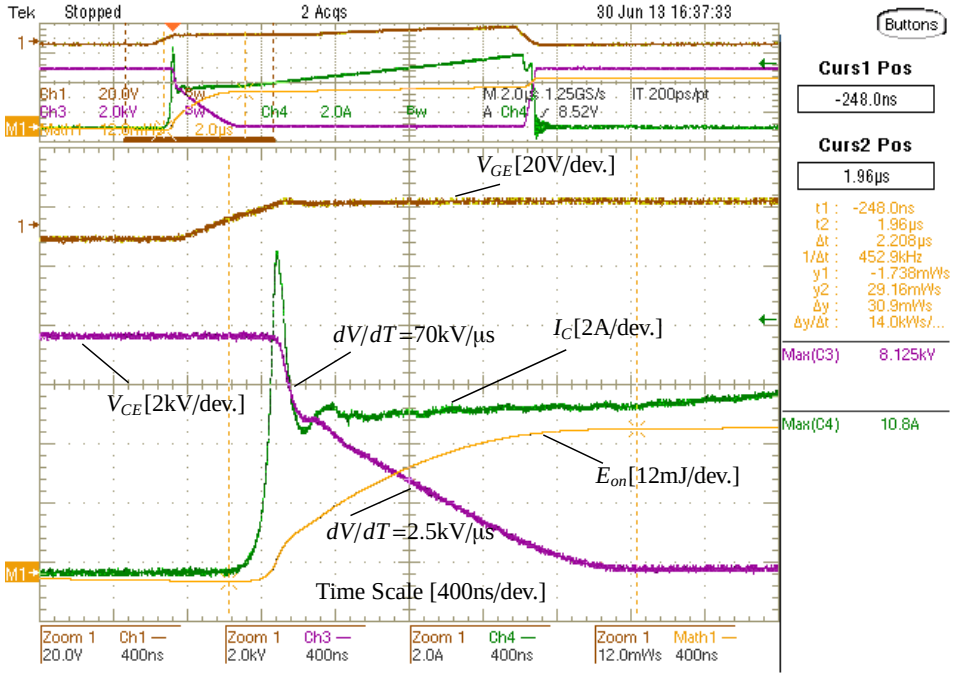
Figure 6.1: Photograph of the TIPS MV gate-driver

6.2.1 15kV/20A, 2μm buffer SiC IGBT

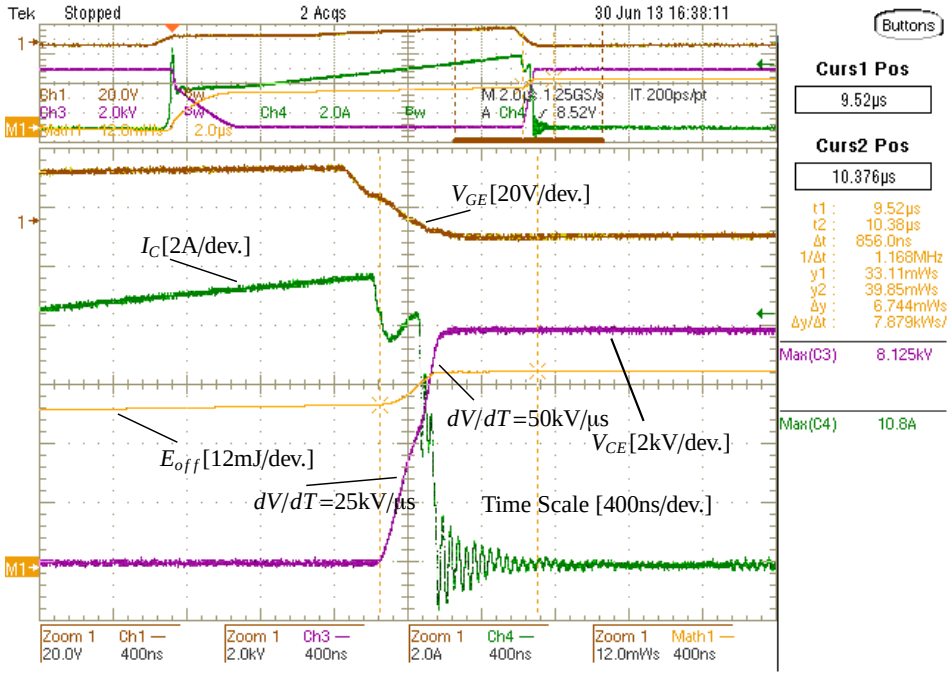
A double-pulse (DP) test hardware setup is used for characterization of the given HV SiC devices presented in [41]. The 15kV, 20A, 2μm buffer SiC IGBT based SiC JBS diode-clamped NPC converter with 200Ω gate-resistance, hardware. Fig. 6.2(a) and Fig. 6.2(b) show the double-pulse (DP) test results on the 15kV/20A SiC IGBT co-pack module during turn-on and turn-off respectively at 8kV/10A/175°C. The gate resistances are selected such that the above punch-through dv/dt is limited to 30-100kV/μs for EMI consideration [40].

6.2.2 15kV/40A, 5μm buffer SiC IGBT

The hard-switching DP test results of the 15kV/40A SiC IGBT module, which has two 20A chips in parallel, are shown in Fig. 6.3 at 5kV, 5A and 175°C hot-plate temperature. The detailed characterization is provided in [102]. These devices cannot be switched at a very high dv/dt due to the EMI issues leading to malfunctioning of the gate driver [44] and other electronics. Such high dv/dt generate EMI even for the control and protection electronics and also results in high switching loss. Also the high current ringing is generated corresponding to the slope which cumulatively limits ZVS range. It can be noticed there are two slopes for below and above PT level as mentioned earlier. The turn-on gate resistance is 33Ω for this maximum turn-on dv/dt of 30kV/μs while the turn-off gate-resistance is 10Ω resulting in maximum turn-off dv/dt of 12.5kV/μs. It also results in 9.4mJ and 19mJ energy-loss respectively for turn-on and turn-off. These gate-resistance's are selected to limit the maximum dv/dt from experimental setup point, given the particular gate-driver design [44]. The dead-time is selected as 3.4μs considering the switching delay and the ZVS criteria that dead-time has to be greater than module parasitic discharge time during freewheeling through its anti-parallel diode [42]. Fig. 6.4 shows the look-up-table (LUT) of switching losses for this devices under different hard-switching voltages



(a) IGBT turn-on hard-switching



(b) IGBT turn-off hard-switching

Figure 6.2: 2 µm buffer 15 kV/20 A SiC IGBT switching characteristics at 8 kV/10 A/175°C

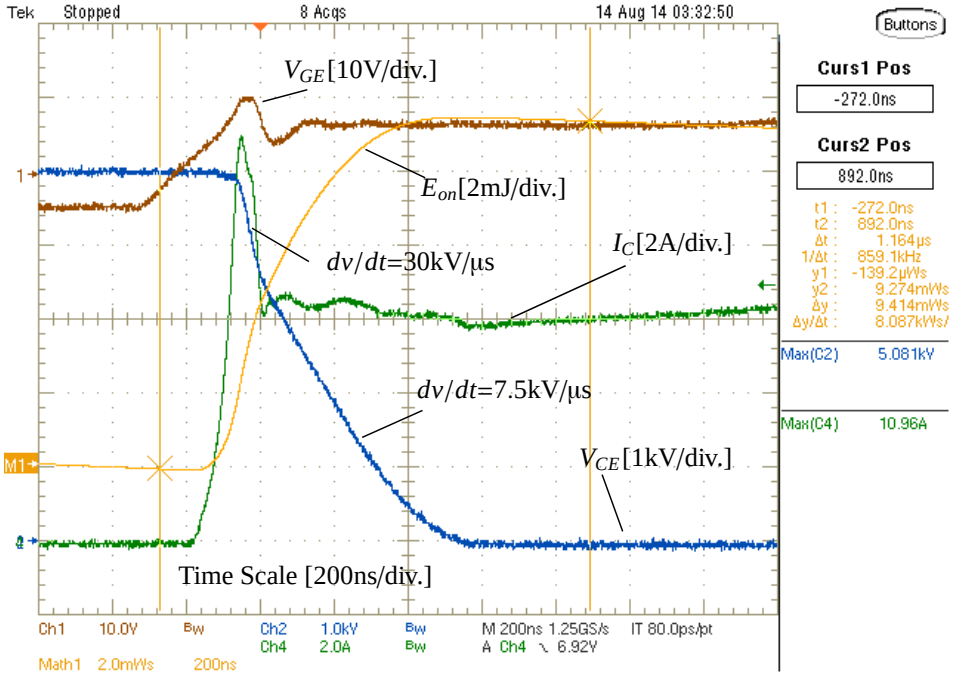
and currents up to 6kV/10A. Three temperatures are considered 25°C/150°C/175°C. This is fed to the Matlab-Plecs simulation block for worst case loss calculations for a DAB, as it does not consider any parasitic capacitance of the device that may help in reducing actual turn-off losses. For switching loss at unknown points, the simulation interpolates. Similarly when thermal model is entered and temperature rises, the simulation interpolates to predict losses for intermediate temperatures. This loss calculation method has been followed throughout in this dissertation.

6.3 NPC Converter Pole

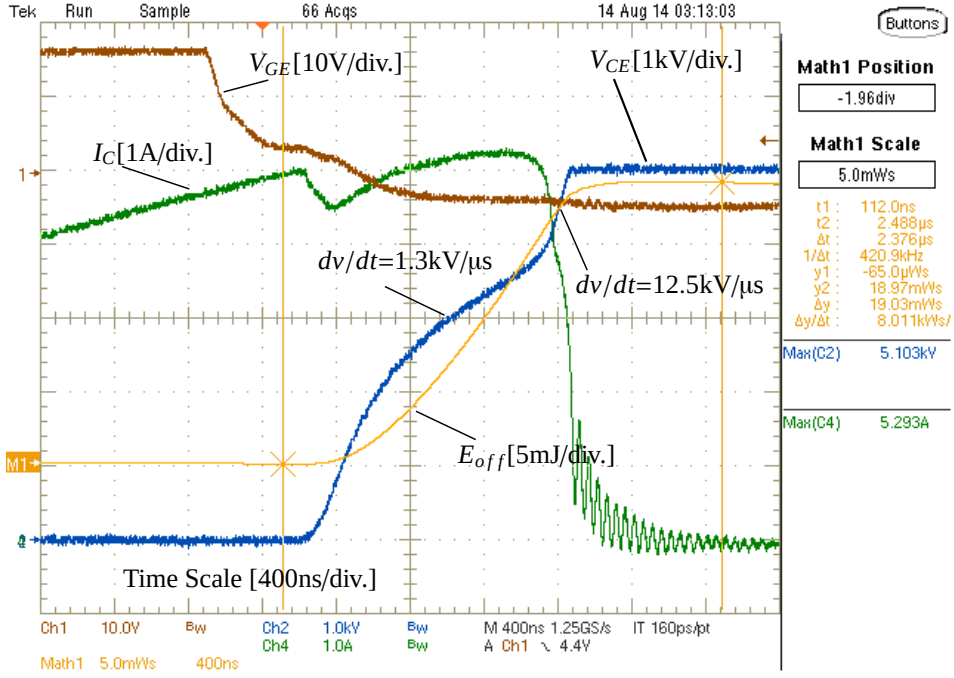
Multilevel converters are used in high-power high-voltage applications due to their advantage of lower voltage-stress on the devices and modular structure. Cascaded H-bridge and diode-clamped NPC converters have been very popular for medium-frequency high-power applications. The cascaded converter requires either multiple isolated dc supplies or a multi-winding primary side transformer in case of single dc source. The NPC converter requires multiple capacitors at the dc source for voltage division. Both face the problem of dc voltage imbalance and need active correction. TIPS system rectifier generates 22kV dc and the MV switching device can maximum go up to 15kV, so the multilevel converter must be used and it can be a NPC converter and to reduce the complexity and number of switches, it has to be three-level. The capacitor voltage imbalance has to be actively balanced by the control. The 15kV SiC IGBT has considerable parasitic capacitance especially below punch-through and also its dv/dt is made relatively lower (30kV/µs) with higher gate resistance to avoid EMI problems in this region [40]. Therefore a dead-time in the range of 3.8µs is selected. To maintain turn-on ZVS at light loads there should be sufficient current to discharge the parasitics before the dead-time ends. Three-phase DAB with smoother current near zero-crossings is more difficult to maintain ZVS compared to a single phase DAB with trapezoidal current [42]. Above punch-through the parasitic cap reduces in 15kV SiC IGBT, this results in EMI and increased turn-off losses even if the turn-on ZVS is maintained [31]. With DAB switching frequency at 10kHz and given dv/dt, the 3.8µs dead-time is suitable [30]. The 3L NPC pole built using these devices is shown in Fig. 6.5.

6.3.1 NPC Pole Assembly

All gate voltage levels in 4 gate-drivers are matched to ±2% by adjusting turns. The three-level poles using 4, 40A/5µm SiC IGBTs and 2, SiC JBS diodes (2-series), are built for both the AFEC and DAB converters. There are three identical poles for each of DAB and AFEC. Each pole has three-level dc bus built with series connected 3.5kV film capacitors. The bleeder resistances are used to balance series connected capacitors. For this setup two capacitors are connected in series for each half of the dc bus making the setup ready for 14kV maximum voltage test. All the devices used in these poles have been qualified on 30min boost converter heat-run test. The modified gate drivers having the transobs and zener

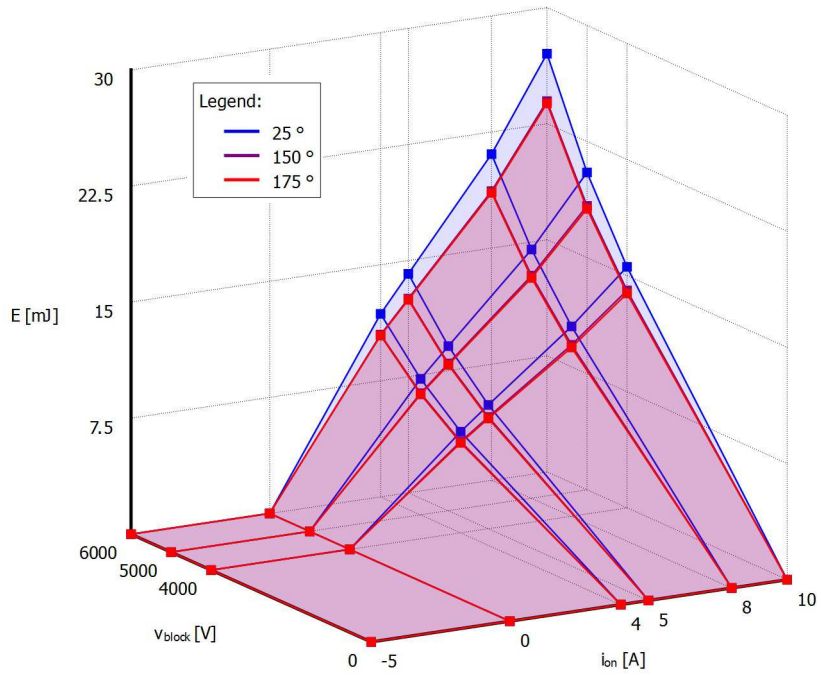


(a) Hard turn-on at 5 kV/5 A

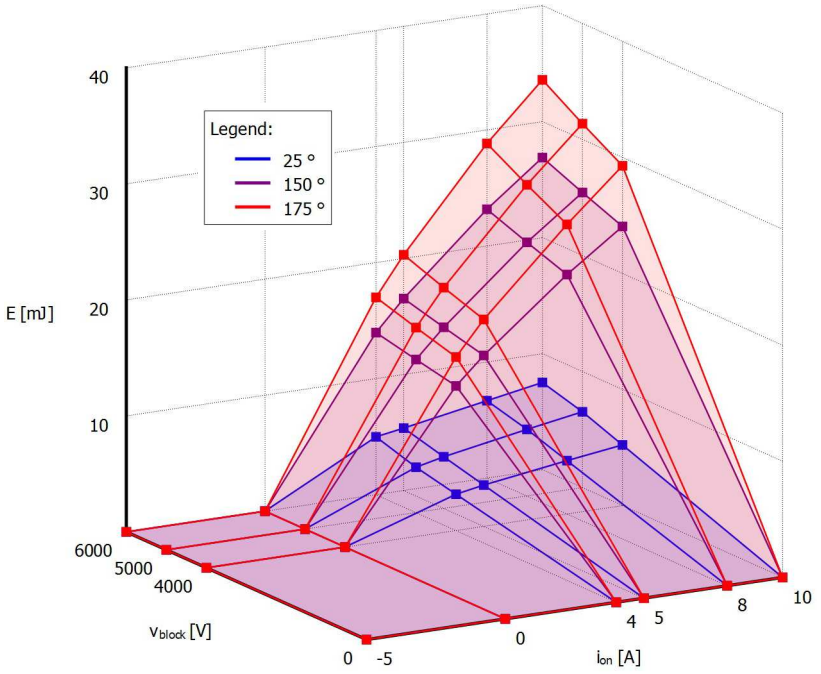


(b) Hard turn-off at 5 kV/5 A

Figure 6.3: 5 µm buffer 15 kV/40 A SiC IGBT switching characteristics at 5 kV/5 A/175°C



(a) IGBT turn-on hard-switching



(b) IGBT turn-off hard-switching

Figure 6.4: LUT of 15 kV/40 A SiC IGBT switching losses

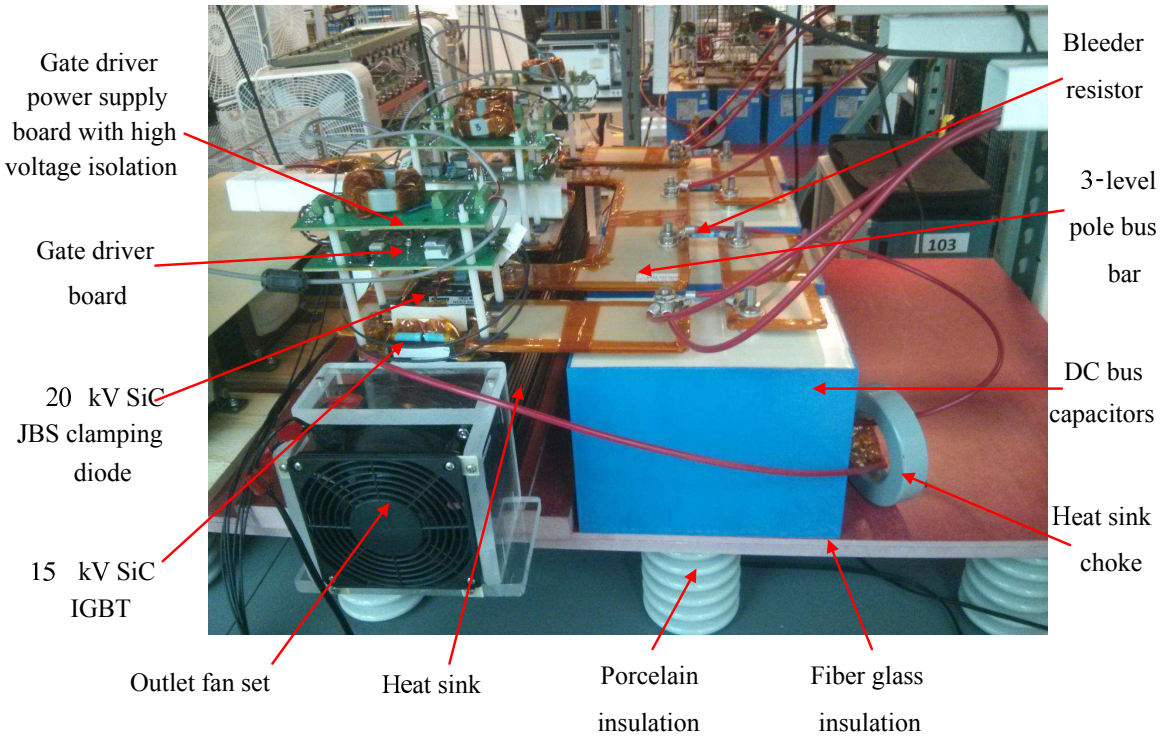


Figure 6.5: Photograph of the MV NPC pole

diode protections are used in these pole tests. In the MV hardware set-up II of the AFEC and DAB, all devices are changed to 5μm buffer from earlier 2μm buffer devices with same module package. All diodes are replaced with 2-series diodes (16kV/10A) compared to earlier 1-series diodes (20kV/10A) due to later's non-availability. All the gate drivers in different poles are also made uniform in terms of the turn-on and turn-off gate voltages. The transorbs for suppressing any transient over-voltage spike are installed in all the gate drivers as device gate protection. Since the device anti-parallel section and clamping diode modules use two SiC JBS diodes in series to block higher voltage, leakage balancing non-capacitive bleeder resistors are connected in parallel across each series diodes to balance their blocking voltage. Also in a three-level pole during positive cycle, the bottom two devices are in off state and their blocking voltage depends on the device leakage value, the bleeder resistors are used across the devices to again balance their blocking voltage because they have slightly different level of leakage even after a matching pair is selected. Two inlet fans and two outlets fans are mounted across the heatsink conduit for each pole for increasing the CFM. The complete thermal design for this converter for this hardware setup is presented in [102]. Few layers of kapton tape and nomex paper are used for insulating all the exposed terminals, edges and metal contacts. This is very important because with the given device package, its pin outlet and busbar design, it is challenging to maintain a safe creepage distance between high voltage (often high-frequency) and ground. Each NPC pole heatsink is grounded to converter dc

neutral with a choke as shown in Fig. 6.5. Without this mid-point grounding, EMI related false fault-trips in the gate-drivers are encountered at lower voltage itself. Solid grounding without the choke caused large current spikes in this grounding wire. A more detailed discussion is presented in [28].

6.3.2 NPC Pole Heat-run Test

Prior to putting these poles in TIPS setup, they have been heat-run tested individually at 10kV dc bus both with 5kHz square and 5kHz SPWM switching. They also are tested at 6kV dc bus with 10kHz square PWM in the actual TIPS-DAB mode. In the actual DAB, ZVS will happen and the thermal run done here with resistive load gives worst case losses due to hard-switching, therefore the poles have not been run at 10kV dc bus with 10kHz square PWM as the thermal management is not designed for worst case. A boost converter using the same device, is used to generate 10kV dc source for testing these poles from a lab Magna power source of 3kV dc, 50kW. The components qualified in this test are busbar, gate-drivers, PWM with dead-times and heat-sink thermals. The DAB poles work with

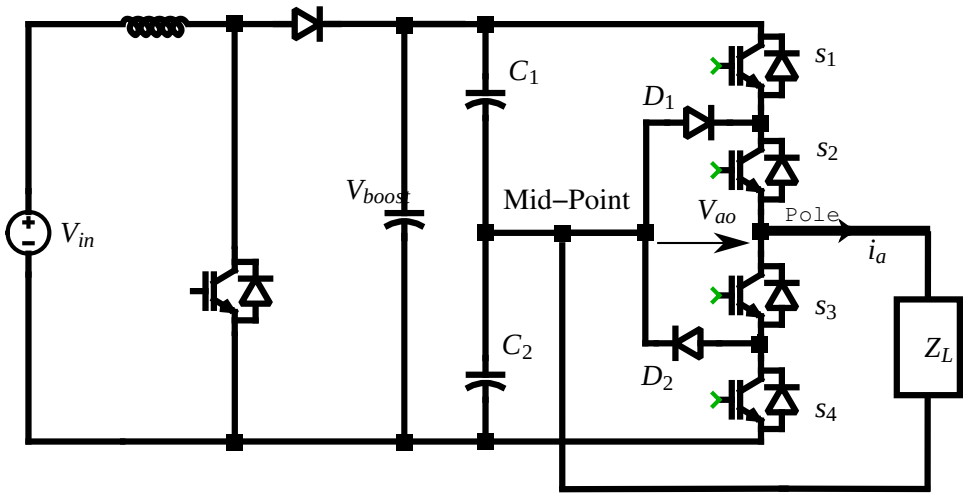


Figure 6.6: Schematic of the 10kV qualification test with R and RL load

square-wave modulation while the AFEC poles work with SPWM in actual application. But to test the thermal stability of each pole on same standard, all the poles are first tested at 10kV dc, 7.2kW power and 5kHz square-wave PWM for 30mins. In this test, the NPC poles are switched in quasi-square mode with 41.6% duty-ratio to generate minimum THD for MV DAB application [23]. Three levels of voltage are produced at the pole, just like the proposed DAB operation, i.e. 0, $+Vdc/2$ & $-Vdc/2$ and the duty of $+Vdc/2$ & $-Vdc/2$ are kept 41.6% each, the rest 0 is equally distributed and sandwiched between them. Fig. 6.6 shows the schematic of the qualification test. The device numbers represent the specific

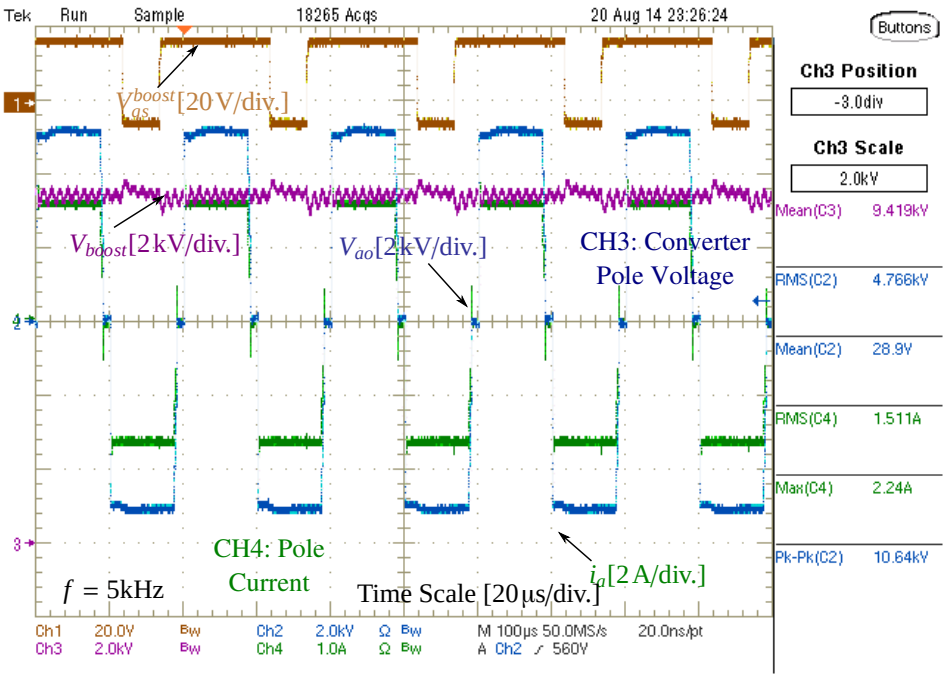


Figure 6.7: 15 kV SiC IGBT based 10 kV NPC three poles 7.2kW, run for 30 mins with 3 kΩ R load at 5 kHz switching

Figure 6.8: Thermal run for 30 min at 10 kV with R load at 5 kHz

SiC-IGBT and JBS-diode locations in the pole. They have been matched after the individual boost test for their leakage and thermal stability. Fig 6.7 shows the scope waveforms from the test measurements with resistive load. It shows the boost supply output in pink which is the DC supply for pole testing. The blue waveform represents the pole to DC neutral voltage under square wave modulation as mentioned earlier. The green waveform is the pole current with resistive load. The brown waveform is the gate pulse for the boost converter which is also 5kHz. The scales for each channel are given below. For heat-run test, the poles are switched with 3kΩ resistive load. As expected it generates turn-on spikes due to hard-switching as shown in Fig 6.7. The power output corresponds to 7.5kW for the 10kV dc bus. The boost converter supply also switches at 5kHz. The ringing in the boost supply voltage is attributed to interaction of Magna power source to boost inductor parasitics. Fig 6.8 shows the thermal image at the end of the 30 min heat-run test. Since in the NPC square wave test, the switching losses (turn-on and

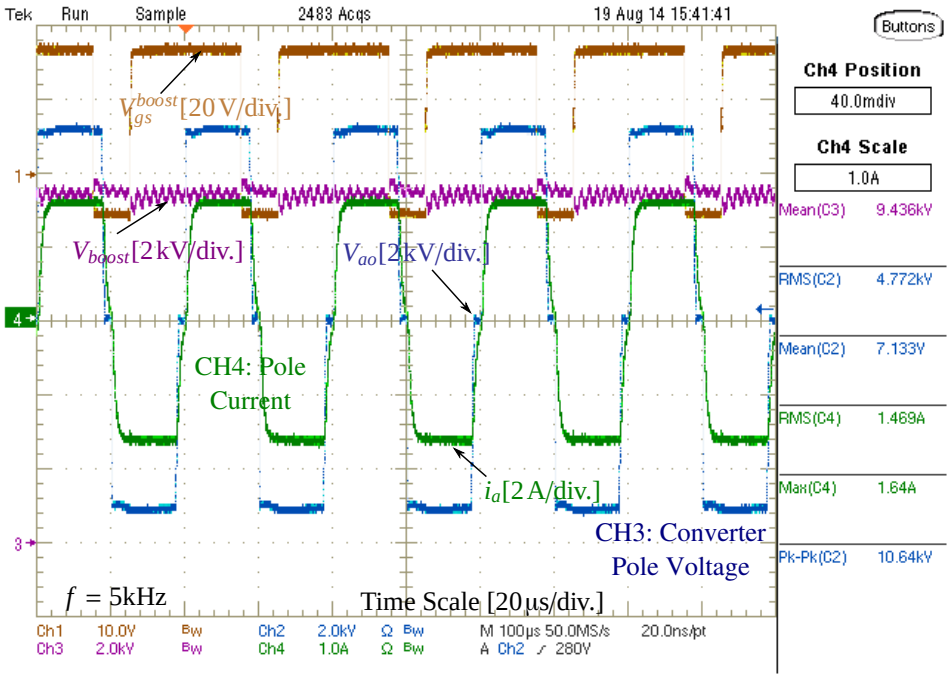


Figure 6.9: 15kV SiC IGBT based 10kV NPC pole 4kW with 3kΩ-14mH RL load at 5kHz

turn-off) are higher for outer ($s1$, $s4$) devices than the middle devices and the switching loss at 5kHz is dominant over conduction losses, therefore outer device locations below the base plates are the hot-spots. There are two fans mounted at either side of the heat-sink to setup airflow path. One fan injects air and the other side fan exhausts the warm air. The injection side heat-sink area is found to be cooler than the other side. It has nothing to do with devices but the thermal physics. The thermal picture is taken from T420 FLIR camera which avails three pointers to focus on hot-spots. The third points is the

average heat sink temperature. The measurement spot, pointer sp1 is near the inlet fan, sp2 indicates the mean heat-sink temp and sp3 is near the outlet fan. Also it is to note that sp1 is near base plate of bottom IGBT, sp2 in the middle of the heat-sink and sp3 is near base plate of the top IGBT. Fig. 6.9 shows the scope waveforms from the test measurements with lagging load (resistor 3kΩ, inductor 14mH). This test was done to observe the effect of lagging load on the NPC converter performance under the same square wave modulation. The results are thermally just a little lower than the resistive load tests hence the next tests are continued under resistive load only for rest of poles. But the current spike is certainly reduced. This phenomena can be justified since the turn-off loss is 19mJ against turn-on loss of 9.4mJ for the 15kV SiC IGBT as in the DP test result. Other factor is that inductance is relatively smaller for 5kHz and full ZVS is not occurring. Full ZVS removes the turn-on loss completely but turn-off loss remains but is lower than the hard turn-off value since there is always some parasitics capacitance across the device.

6.3.3 Analysis of the Current Spike in the NPC Pole Testing

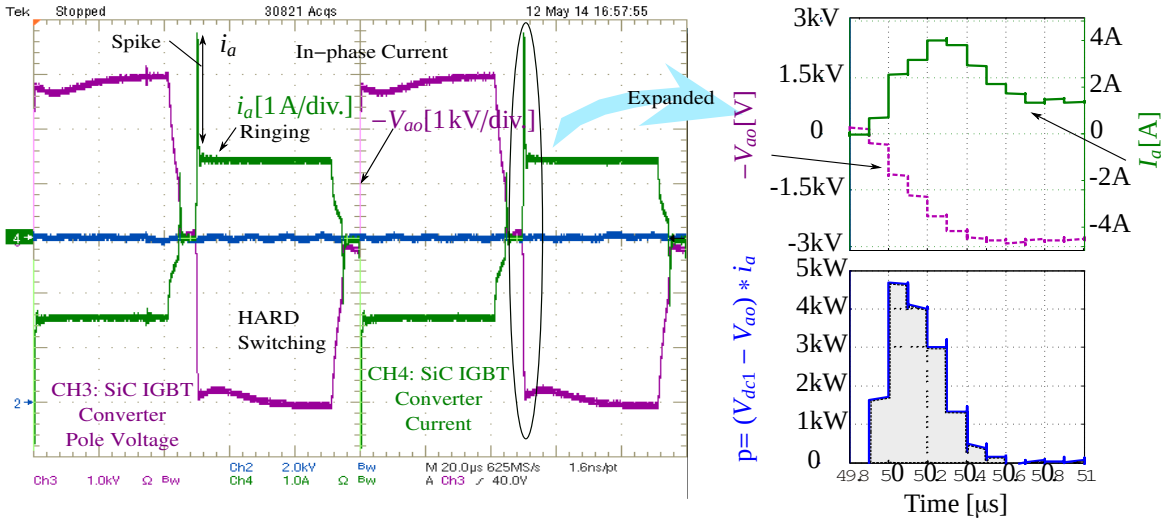


Figure 6.10: 15kV SiC IGBT based 6kV NPC pole 4kW non-ZVS

When the NPC pole is tested in DAB mode switching supplying a 3kΩ resistive load. The dc voltage supply is 6kV and power output is around 4kW. As shown in Fig. 6.10, it generates turn-on spikes in current. As shown in the expanded turn-on duration, it results in inflated real switching loss. It is of about 1.6mJ value after integrating the power loss-time area. It is higher than what would have been in absence of the module parasitics. It occurs due to module capacitance and load capacitance charging, since at this dv/dt, the parasitics are significant. Therefore, higher dv/dt will lead to higher energy-loss

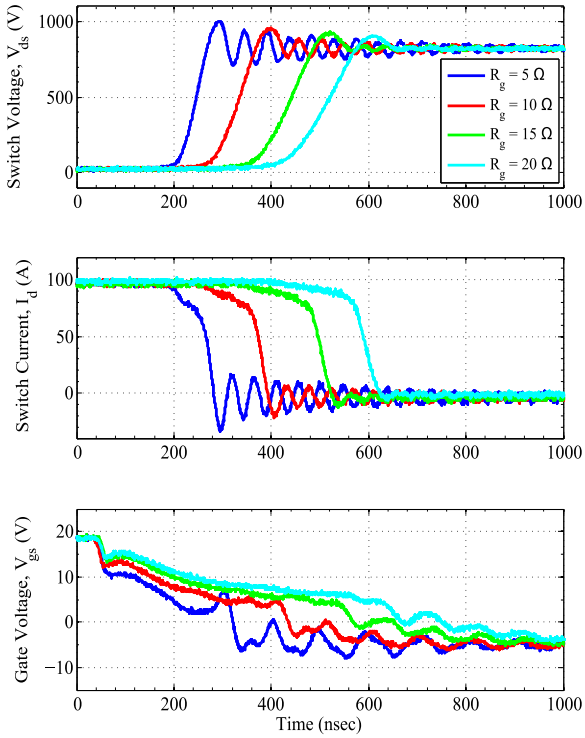
Table 6.1: MV DAB setup parameters

Parameters	Value[Units]
Input dc Voltage	8kV
Output dc Voltage	480V
Switching Frequency	10kHz
Rated Load	50kW
Mag. Inductance, L_m	293mH
Transformer Turns-ratio	13.4/1/1.7 nominal
Equi. Diff. Capacitance, C_p	250pF
Total Leakage from HV side, L_1	643μH
Total Mutual Capacitance	1200pF
Input side Duty-Ratio	41% nominal
External Inductor, L_{s1}	80μH/100A
External Inductor, L_{f1}	400μH/10A
Filter Damper, R_{df1}	5kΩ/4kV
Input Half dc Capacitor	180μF/6kV
Output dc Capacitor	10000μF/1200V

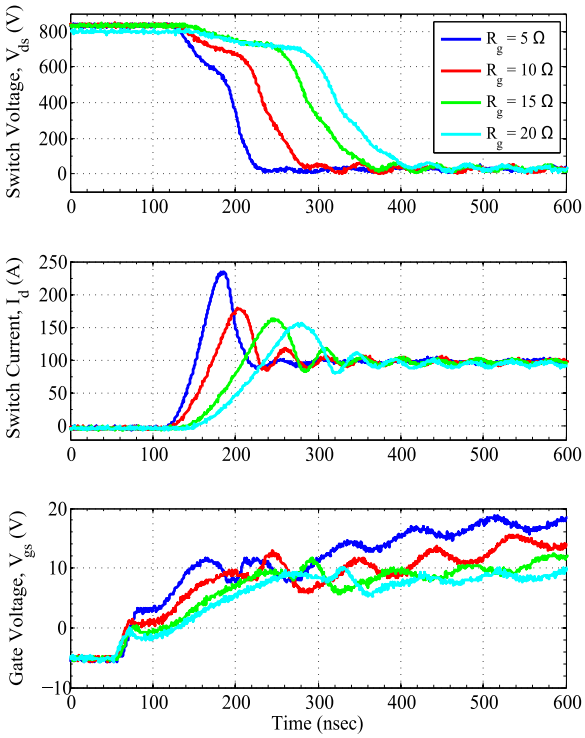
and EMI due to the current spike. There is sampling limitation in the measurement so the energy-loss is approximate. This result supports the claim that DAB MV converter should operate in ZVS for better efficiency and less EMI generation [42].

6.4 1200V SiC MOSFET Switching Characteristics

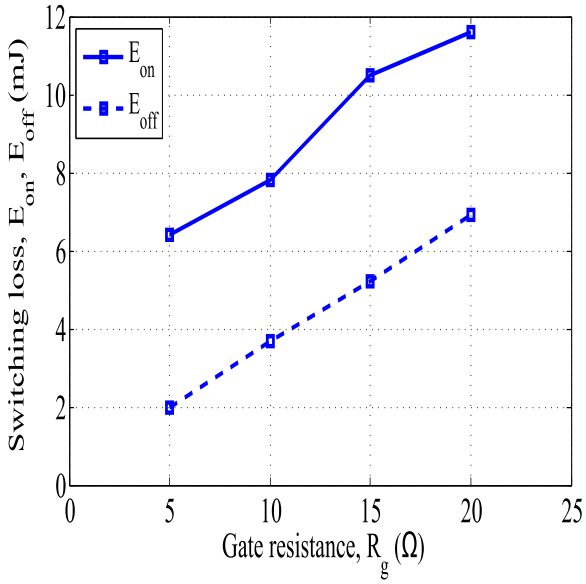
Figs. 6.11(a) and 6.11(b) show the SiC MOSFET hard-switching characteristics for turn off and turn on. The detailed characterization has been presented in [101]. The gate resistance of 10Ω is found to be optimum since it does not cause much current or voltage overshoot. It offers a medium dv/dt (8-12kV/μs) without resulting in high switching loss as shown in Fig. 6.11(c). The LV side external inductors have high per unit (p.u.) value and hence the effect of MOSFET dv/dt is expected to be limited since they have small parasitics in per unit value. In practice the device needs to be slowed down with moderate switching losses. The LV three-phase converters based on these modules are tested at 35kVA each in [101]. Two of them are used in DAB LV side star & delta and three of them are used in the output inverter stage.



(a) MOSFET turn-off hard-switching



(b) MOSFET turn-on hard-switching



(c) Effect of gate resistance on MOSFET switching

Figure 6.11: 1200 V/100 A SiC MOSFET switching characteristics

6.5 Y:Y/Δ DAB Hardware Setup

The schematic of the topology is shown in Fig. 2.5. It has one MV converter on star configured primary and two LV converters on star-delta configured secondaries. The DAB rating and parameters are given in Table 6.1. The Y:Y/Δ three-phase MV-HF transformer is formed by three single-phase three-winding transformers. The primary is fed with three-level NPC poles shown in Fig. 6.5. They generate quasi-square wave pulses with 41.6% duty-ratio to generate minimum THD at full load. Fig. 6.12 and Fig. 6.13 show the hardware setup of the MV three-phase DAB converter rated for up to 100 kW TIPS rating. The converter has robust arrangement, enough isolation clearance, shielding of feedback signal cables, transorb and zener included in gate drives. The AFEC and DAB are 3-ph converters and consist of 3 modular NPC poles each, built with 15 kV SiC IGBTs and 20 kV SiC JBS clamping diodes.

6.5.1 Rack Arrangement and Wiring

These poles and HV inductors, which are at high potential, are isolated from the rack frame using porcelain standoffs. The AFEC and DAB differential inductors are designed in the previous works [29, 32, 30, 103]. The transformers have already good isolation with its cabinet. But still the LV converters, LV inductors and transformers are based upon fibreglass isolation sheets. Each NPC pole has local dc capacitor bank. These local dc buses are connected together for the DAB resulting in one three-level dc bus. Two HV voltage sensors are connected to measure these dc buses and active balance using controls. The controller generated gate signals are optically routed to the GDs. A LV voltage sensor is used to measure LV dc bus or output of the DAB. The sensor cables are shielded and referenced at the control ground to avoid any noise pick-up. Good EMI quality power supplies are used, one for all MV gate-drivers, one for LV gate-drivers and one for P/D & control boards outside HV testing cage. Also all the power supplies have a CM choke at their ac chords. All the power cables are routed using guides as shown in Fig. 6.12. All the control power supplies and even fans are powered from two separate UPS back-ups so that the system is in known state and can safely shutdown if lab power fails or trips.

6.5.2 Transformer Connections

A photograph of the three single-phase MV-HF transformer's star-delta connections in three-phase is shown in Fig. 6.14. For connections, suitable current and isolation rating cables are used. The HV cables are rated for 40 kV isolation, 10 A and LV cables for 1700 V, 100 A. For transformer Δ winding current measurement, a pearson wide band current probe is placed as shown in Fig. 6.14 over two cables entering the Δ+. Floating neutral connections are made as in the schematic shown in Fig. 2.5 for Y sides. Before the DAB system is tested in closed-loop, the transformer connections with the phase-sequence are verified by powering only the LV converters of the DAB with a small voltage while primary HV windings are kept open. Only LV delta converter is turned on (LV gate-driver has a pulse off switch) and

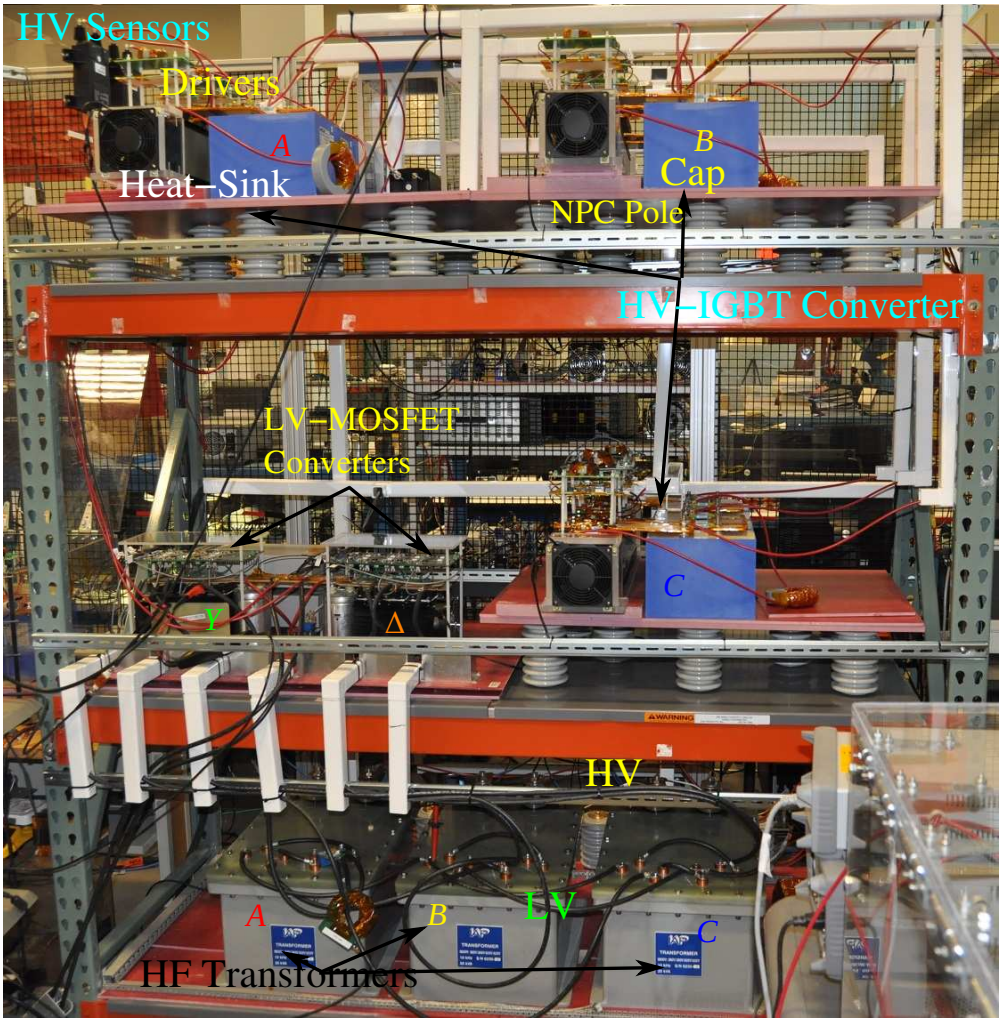


Figure 6.12: Hardware-setup II for MV three-phase Y:Y/Δ DAB

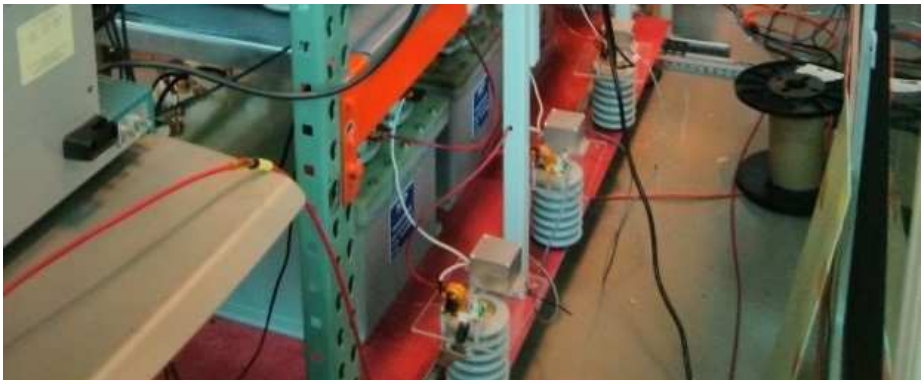


Figure 6.13: Rear view of the hardware-setup II

Figure 6.14: Photograph of the DAB transformers in three-phase

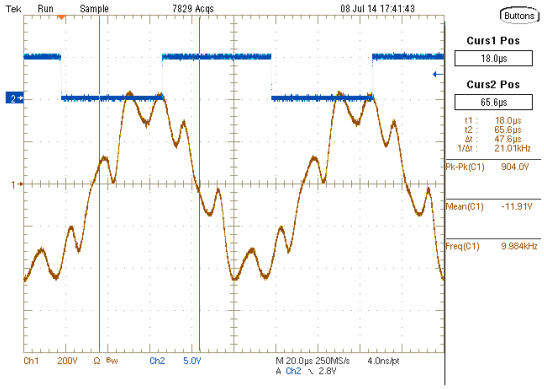


Figure 6.15: Test from secondary excitation while star is off

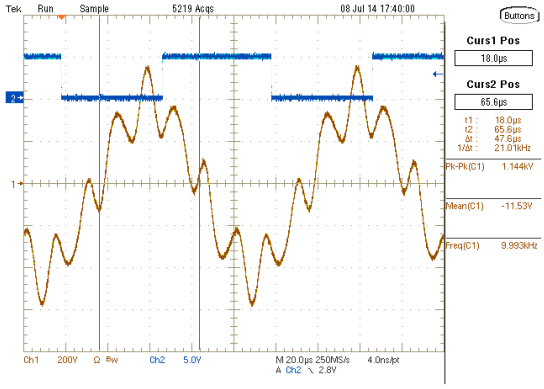


Figure 6.16: Test from secondary excitation while delta is off

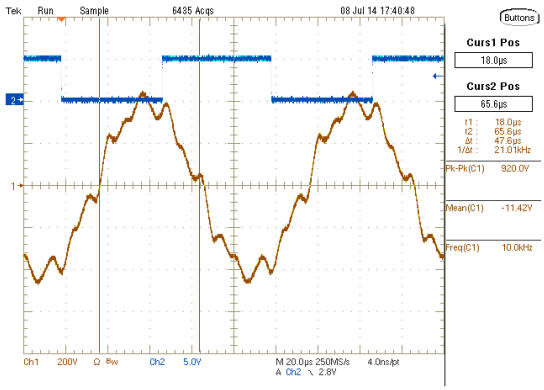


Figure 6.17: Test from secondary excitation while both LV are on

waveforms are captured on primary a-phase HV winding as shown in Fig. 6.15. This is a typical three-phase neutral connection waveform for six step switching. Now only the LV star converter is turned on and the waveforms are captured on primary a-phase HV winding as shown in Fig. 6.16. The waveforms are again expected for six step switching three-phase neutral connection. Now both the LV star and delta converters are turned on and the waveforms are captured on primary a-phase HV winding as shown in Fig. 6.17. The waveforms as seen is very smooth without any change in its fundamental phase relative to a reference PWM as expected. It seems that 5^{th} and 7^{th} harmonic currents of Y and Δ sides have canceled each other. The circulating current between the two is also small as expected due to LV inductors.

6.5.3 Load bank development

Fig. 6.18 shows the load bank developed for the TIPS project DAB LV side loading. Each resistor is 10Ω, 10A and 1kW rated. Fifty such resistors are assembled in the rack. These resistors can be configured in different series and parallel combinations to load the connected converter at different power levels. It can be loaded up to 50kW peak power. Four standard fans mounted as shown in the figure, provide the forced air cooling to the load resistors. The resistors are organized as parallel bank of 4 resistors, total 12 groups of 2.5Ω and 40A. They are now connected in series to make total 30Ω, 1200V and 48kW rated.

6.5.4 MV Voltage Sensor Testing

As shown earlier in Fig. 5.18, the P/D board has sensor interface with a burden resistance to convert current source measurement signals into voltage source for protection comparators and A/D conversion in the FPGA interface board for controls. For MV three-level dc bus measurement, two 4.2kV LEM voltage sensors are used. Before closed loop test, they are tested for linearity and performance. Fig. 6.19 shows the plot of measurements with voltage. The measured signal are DAC output of the ADC con-

Figure 6.18: Photograph of the DAB low voltage load bank

verted dc bus voltage signals for top and bottom dc buses. The ADC can measure from 0 to 5V with 2.5V as reference (zero signal) level. The DAC also has 2.5V as reference and is setup to output negative of the digital value. Therefore for voltage increase the measurements drop linearly as expected. The 50Ω burden resistance is good for 4.2kV measurement. From sense signal point of view, 25Ω burden resistance doubles the limit but decreases the resolution. This setup is powered with 50Ω burden setting and it can lead to DAB operation up to 8kV. One important point to note is that this voltage sensor DV 4200 has 50μs response time which affects the voltage control bandwidth and therefore is accounted for in the control design. To go above 8kV DAB operation, either two of the sensors are connected in series power connections and parallel-sense (current source) terminations, or a series power resistance is used to divide the voltage. As seen in the figure, the later gives linear signal, but in real high voltage condition, this does not work as planned, since the sensor response time changes and the resistors get hot and their resistance changes. This is one of the reason for voltage limit of the demonstration. The control design of integrated TIPS system is challenging as presented in following integration chapter.

6.6 Conclusion

In this chapter, the step by step qualification and setup development is discussed with different demonstration limiting factors. The NPC poles qualification is limited to 10kV and 10kW and this makes the

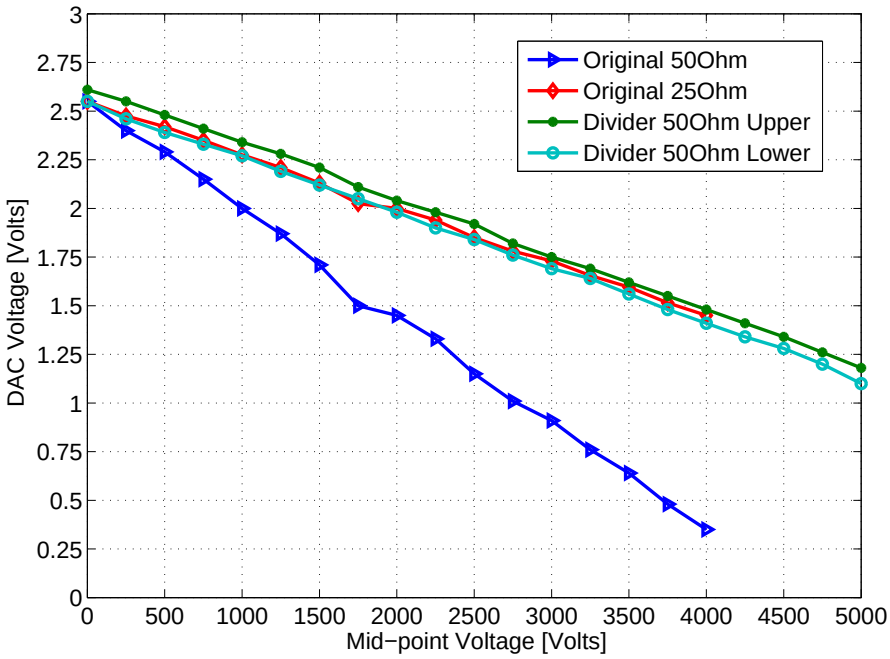


Figure 6.19: TIPS MV voltage sensor test

poles ready for DAB demonstration till maximum 30kW. From 30min thermal results, it is clear that the cooling system is stable for this power but for 5kHz load with not much advantage from ZVS due to high turn-off loss of the IGBT. Therefore MV DAB is not been tested for 30kW. It is also evident from the non-ZVS switching analysis that in order to optimally operate the MV DAB at rated voltage, ZVS operation needs to be ensured. The boost power supply using the same IGBT, has been a major limitation for 10kW power limit as the Magna power can go maximum till 3kV. Most of the components in the DAB setup are rated for full TIPS rating. The busbars can be rearranged to accommodate more film capacitors in series for more than 14kV tests. The wiring, shielding, grounding and pole arrangements are important from EMI perspective. The transformer booting up results verify the phase-sequence and basic working of the topology. The load can be used demonstration till maximum 50kW. The MV sensor linearity has been tested up to 4kV and its limitations are presented for going up in voltage.

Chapter 7

Optimum Design Considerations of the Medium-Voltage DAB considering non-idealities

7.1 Introduction

The 15kV SiC IGBT based three-level topology enables a non-cascaded DAB. It is simple to control compared to a series cascaded structure using voltage and power balancing control. But it poses additional challenges at the MV level as the converter needs to be optimized for parasitics, dv/dt and dead-time (t_d). These parameters affect the ZVS range of the DAB as presented in this chapter. This chapter presents these ZVS challenges in the design of a medium voltage (MV) DAB converter system using extensive non-ideal Matlab-Plecs simulations. This chapter presents the effects of MV-HF transformer's parasitic, t_d and D on ZVS range using a vector diagram. This chapter also presents an optimum design for the DAB while considering the device and transformer characteristics. The two control variables, the DAB phase-angle (ϕ) and the three-level converter D make it possible to set current-vector at an optimum angle of voltage-vectors ensuring ZVS and minimum reactive power-flow [49]. This chapter presents criteria for an optimally designed DAB that can be operated at the highest efficiency with low EMI. The critical design factors are highlighted for the developed MV DAB. The experimental results of MV Y:Y/Δ DAB operation for different power, voltage & voltage-ratio and frequency has been presented. The experimental results are presented, leading up to 8kV, successfully obtained after implementing the methods discussed.

7.2 ZVS Criteria for the Y:Y/Δ DAB

The MV-HF transformer has considerable parasitics which are generally ignored for a LV DAB [38]. But the high dv/dt's of the SiC IGBT/MOSFET switches, which have been characterized in [41, 44, 101], cause undesirable spike and ringing in the currents on hard-switching at such voltage level. The MV three-level converter causes smaller current ringing due to parasitics compared to an MV two-level converter. The slowing down of devices attenuates the ringing but causes more switching losses. Also, it requires larger t_d of the converters which affects the DAB ZVS operation. Before generating the specification of the HF transformer, simulations with non-ideal conditions is done. The dv/dt, V_{dc1} and parasitics define the magnitude of current ringing. This ringing needs the current to lag from pole-voltage (V_{ao}) by an extra phase (θ_p) for ZVS operation otherwise the switch voltage will be non-zero at the end of t_d. The dv/dt also defines the needed t_d. Which then defines an additional phase d_H required for ZVS. If the converter is operated with less than 50% duty-ratio (D), this adds another D_H required for ZVS. All the three types of α's add up and limit the DAB ZVS range. The starting parameter for these limitations are the parasitic capacitances of device, transformer and inductor. Therefore they need to be reduced if the ZVS range is highly limited. In other words, to operate the MV DAB in ZVS mode either parasitics need to be reduced or the frequency needs to be constrained. ZVS mode for DAB is active as long as the DAB current-vector is between primary and secondary voltage-vectors. To meet ZVS for IGBTs of three-level converter at a given operating point, the DAB α can be increased by either reducing output dc voltage setting of the DAB or increasing the D of the three-level converter. The shift in primary D from 41.7%, results in distorted current. The ZVS range is limited by DAB-angle. Lagging the current without increasing DAB-angle causes ZVS to lose for the secondary converters. Increasing the DAB frequency for given magnetic design, results in increased DAB-angle for a given load. Fig. 7.1 shows the MV side three-level pole and absolute ZVS condition inequality.

7.2.1 Effect of MV Device Parasitic Capacitance

The device capacitance helps minimize turn-off loss similar to a snubber. But it is very critical for selection of t_d and ZVS operation. Since the current is low for MV side device, during free-wheeling transition, this capacitance needs to be charged/discharged by the pole current for the next turn-on [104]. If there is not enough t_d, the zero voltage will not happen on the turning-on device. This causes partial ZVS. This charge time is $t_c = C_{pole}V_{ao}/I_o$ approximately. With average assumption of 300pF, t_c for $V_{ao} = 11$kV and $I_o = 1$A is 3.3 μs. The t_d must be larger than this. The current lag time t_l must be further larger as shown in Fig. 7.1.

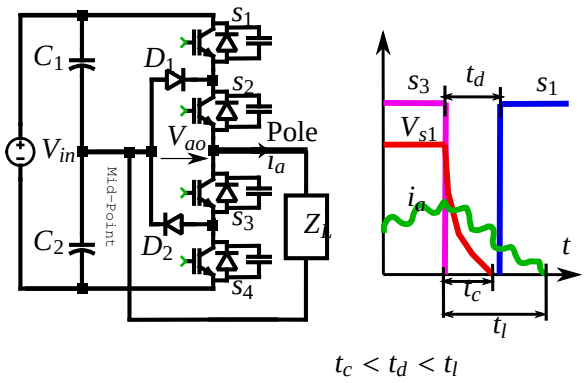


Figure 7.1: Three-level pole and ZVS operation

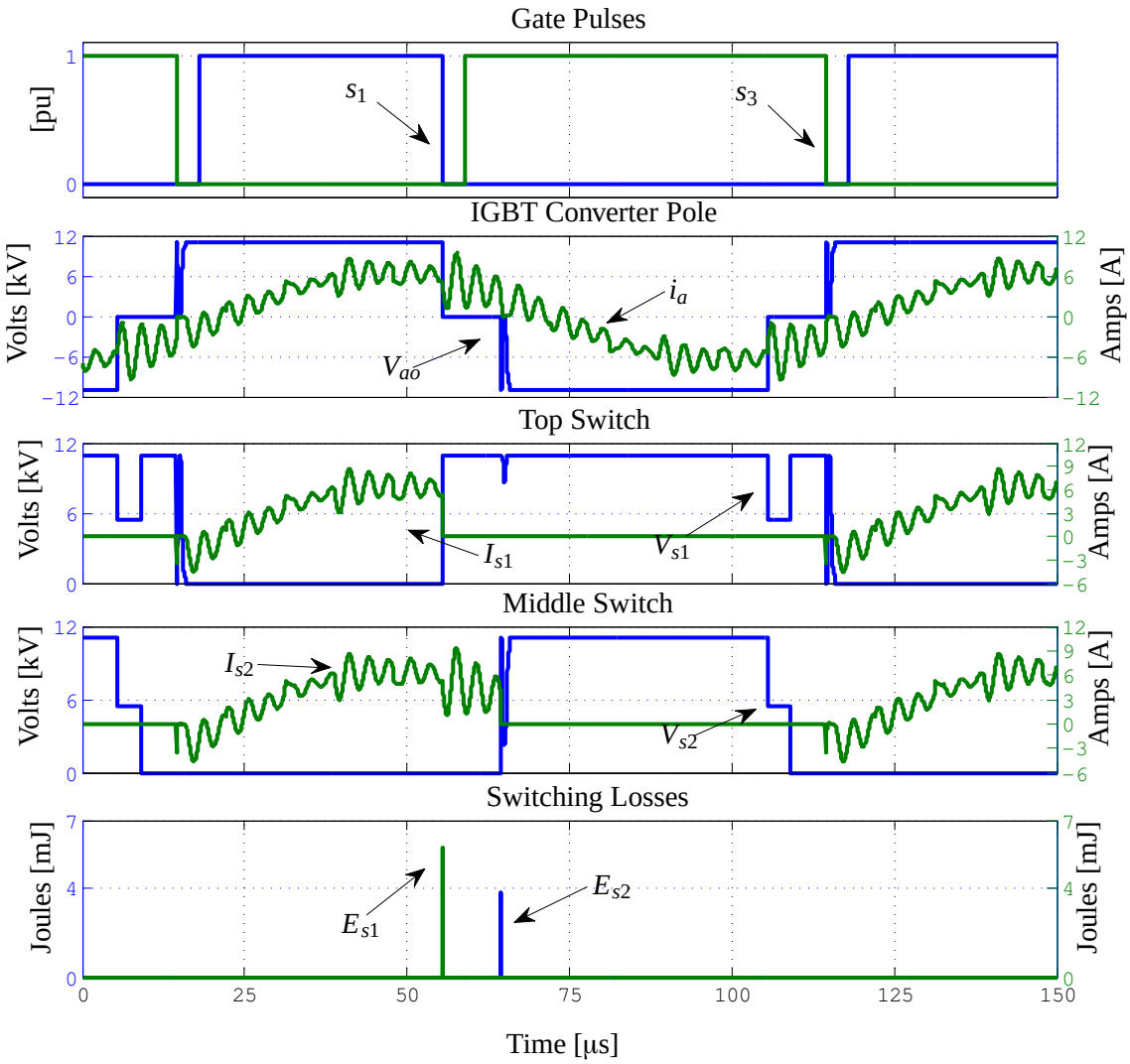


Figure 7.2: IGBT three-level simulation considering dead-time and parasitics

7.2.2 Effect of MV Converter Duty Cycle

Using rated 41.7% D helps cancel harmonics and also provide a PWM control around this D. Transformer turn-ratio is selected considering this rated duty ratio so that reactive power is minimum. The PWM control can actively position the current vector at an optimum phase [86]. For ZVS of the MV side IGBT converter, the minimum α can be calculated from waveforms for six-step shown in Fig. 7.2. With reduced D (41.7%) gate signals for three-level converter, the fundamental voltage vector lags the turn-off instant of bottom-middle device and leads the turn-on instant of top device by 15°. The DAB current must lag the voltage-vector by this minimum angle D_H (same as *gamma*). Lagging the current vector for ZVS causes turn-off to occur at higher currents, now generating more turn-off loss. Thus, it is an optimization problem in light of the experimental behavior of the devices. The outer IGBTs of the three-level pole shown in Fig. 7.1, have narrow ZVS range compared to the inner ones. Lagging the current too much causes more reactive power-flow and hence more current for the same power level. The ZVS of MOSFETs is at boundary for higher α's or even violated.

7.2.3 Effect of MV Converter Dead Time

Fig. 6.2(a) and 6.2(b) show the SiC IGBT hard-switching characteristics at 8kV and 10A. The detailed characterization is provided in [41]. These devices cannot be switched at a very high dv/dt due to the EMI issues leading to malfunction of the gate driver [44] and other electronics. The limited dv/dt also helps to reduce the device spike currents due to parasitics. Considering a safety margin for the switching transition, a t_d of 3.4μs has been selected for the MV converter. This t_d is significant for 10kHz DAB since with this the time period is 100μs. The t_d occurs in both positive and negative half cycles. If DAB-current does not lag sufficiently, the t_d can reduce considerable portion of V_{ao} (7% for 10kHz). This results in mismatch of DAB HF voltages and it increases reactive power, results in non-ZVS operation and reduces maximum power-transfer capability significantly. A slight mismatch in the t_d's of top two and bottom two switches, can result in dc mid-point mismatch.

When the three-level converter current is lagging as desired for ZVS, converter voltage has same D_H as desired by controls and there is no t_d effect. This is because of free-wheeling action by anti-parallel diodes. As in Fig. 7.2, the V_{ao} for $D_H = 41.7\%$ is exactly same as it rises to the $+Vdc/2$ when bottom-middle switch turns-off (path through top diode in free-wheeling mode). The V_{ao} falls to $-Vdc/2$ when top device is turned-off. Importantly IGBT turn-off transient applies slower dv/dt compared to turn-on, hence this helps to reduce the DAB peak current ringing and does not cause false shoot-through trip in the gate-drivers. An additional phase $d_H = 12.6°$ needs to be added for t_d.

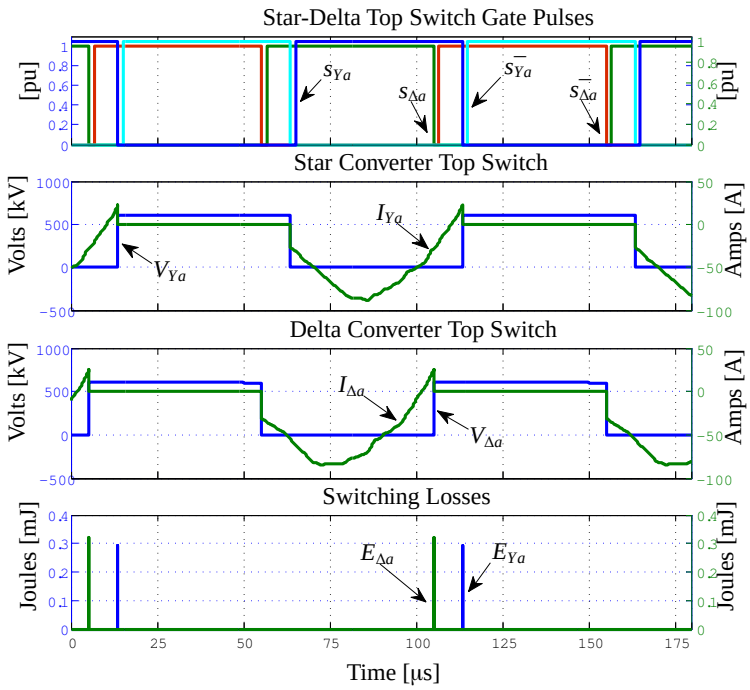


Figure 7.3: DAB secondary (MOSFET) simulation with dead time and parasitics

7.2.4 Effect of LV Converter Dead Time

Fig. 7.3 shows the MOSFET switch waveforms of the LV converters in the DAB. Since the DAB is operating at 100kW in ZVS, the anti-parallel diodes freewheel and V_{ao} changes polarity as soon the outgoing device turns off. There is a small gap between full hard and full soft switching, equivalent to the t_d where the ZVS is partial. A t_d of 1.5µs is selected for the MOSFET converters after optimization between switching loss and EMI. For ZVS condition, minimum secondary lead angle β consists of d_L, a margin equivalent to t_d. With practical device data, the DAB has following expected losses and efficiency as shown in Table 3.2.

7.2.5 Effect of HF Transformer Magnetizing-Inductance and Parasitic Capacitance

Smaller magnetizing-inductance (L_m) makes DAB currents to lag behind and helps DAB converters for ZVS. As shown in Fig. 7.4, the magnetizing current comes from both primary and secondary sides. The individual component add to the respective converter currents. This results in more virtual α and β with factors θ_{mp} and θ_{ms} respectively. The magnetizing current of MV-HF transformer comes is shared according to DAB voltage-ratio and external inductor location. For TIPS all the external inductance is towards LV side to draw most current from MV side for ZVS. The ringing current due to parasitics, does not result in turn-on loss if the DAB current still lags the converter V_{ao} by a margin θ_p. This

margin depends on the magnitude of final parasitic current flowing in primary. As transformer current has parasitic current-ripple, which occurs when bottom-middle switch is turned off and ZVS switching happens after the t_d period passes. To ensure that due to ripple, turn-on instant current does not turn positive, two things can be done. Firstly, ringing frequency can be adjusted with input filter inductor design such that at turn-on instant, it is in negative phase. But practically it is difficult to estimate it correctly.

$$i_r^{pk} < i_a^{pk} \sin\theta_p \tag{7.1}$$

$$i_{m1}^{pk} < i_a^{pk} \sin\theta_{mp} \tag{7.2}$$

Secondly, a margin equivalent to ringing as shown in (7.1), can be added to the α angle. The margin equivalent to magnetizing current from MV side is as shown in (7.2). With rated ϕ 45° for 100 kW, 22 kV-800 V, it is 5° here. The ZVS can be ensured near full load as α of over 32° is required. For secondary side β needs to include a similar ringing margin θ_s. The parasitics adversely affect the ZVS from fundamental harmonic aspect as well [20]. It is important to maintain ZVS for the MV side

Table 7.1: Variables of the ZVS limitation

Symbol	Description
α	MV converter current phase-lag
β	LV converter current phase-lead
i_{s1}^{-}	MV converter current with magnetizing
i_{s2}^{-}	LV converter current with magnetizing
i_r^{pk}	MV converter current ringing peak
i_a^{pk}	MV converter current peak
i_{m1}^{pk}	MV magnetizing current peak
D_H	MV converter duty ratio
d_H	MV converter dead time
d_L	LV converter dead time
θ_{mp}	Margin for MV magnetizing current
θ_{ms}	Margin for LV magnetizing current
θ_s	LV margin for current ringing
θ_p	MV margin for current ringing

converter in all conditions for the DAB to avoid EMI and switching loss. The ZVS range constraint is shown with vector diagram in Fig. 7.4 with notations in Table 7.1. The dead-time (d_H), smaller duty-ratio (D_H) and parasitic ringing (θ_p) shrink available ZVS range while magnetizing current helps it [30]. The d_H is needed for the switching delay protection but it asks for a minimum lagging current

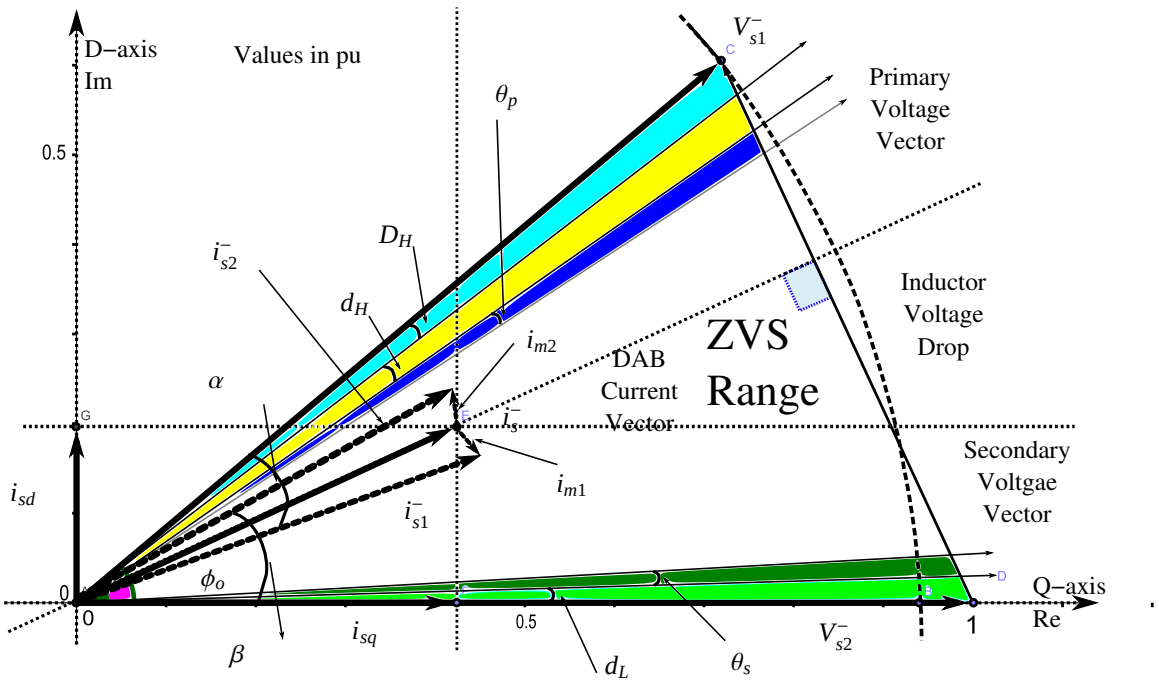


Figure 7.4: Phasor diagram showing DAB ZVS constraints

so that anti-parallel diode could freewheel and discharge the device parasitics to zero. The D_H causes narrower on time for outer NPC devices but wider on time for inner devices. To avoid non-negative current during turn-on of outer devices, an equivalent phase lag for current is needed. The parasitics call for an equivalent lag θ_p ZVS since they make the zero-crossings uncertain [30]. These factors are also counted for the secondary side but the LV side factors are relatively small here. Smaller L_m makes DAB currents to lag behind for primary (i_{s1}^-) and lead for secondary (i_{s2}^-). Thus it helps DAB converters for ZVS. As shown in Fig. 7.4, the magnetizing current comes from both primary and secondary sides. The individual components add to the respective converter currents.

7.3 Optimum Design

The above analysis suggests that with practical considerations of the devices for t_d and parasitics, the ZVS range is limited. There is a large operating area where the V_{ao} shape and magnitude can vary as it is defined by parasitics, device dv/dt and loading. The V_{ao} can be defined only when the ZVS occurs. The maximum duty-mismatch for voltage-balancing control is limited, therefore the mid-point voltage can be unbalanced in hard switching modes. Though it does not saturate the transformer, it appears as a common mode voltage for the star connected transformers.

Fig. 7.4 shows the space-vector phasor-diagram for the DAB. ZVS range shrinks for three-level

converter smaller D (< 50%), smaller magnetizing-inductance, dead-time of converters, current ringing and light-loading of the DAB. Here D_H is region due to Duty ratio, d_H the HV converter dead time, θ_p the angle due to parasitics and d_L the dead time at LV converters. Table 7.1 shows the factors for ZVS consideration. The d-q control can ensure ZVS operation of the DAB, as it can maintain d-axis current independent of q-axis current by adjusting D of primary converter and hence controlling primary voltage magnitude [81]. To calculate the optimum power-factor angle for DAB current, device switching-characteristics are taken in to consideration along with reactive power-flow. SiC IGBT turn-off losses are high and so current cannot be let to lag by large angle from converter V_{ao}. For minimum ZVS condition α, a margin for parasitic current (θ_p), duty-ratio (D_H), magnetizing current (θ_{mp}) and dead-time (d_H) are added to the converter zero-state angle as shown in (7.3). Similarly for secondary, the β is given in (7.4) without duty-ratio control.

$$\alpha = \theta_p + d_H + D_H - \theta_{mp} \tag{7.3}$$

$$\beta = \theta_s + d_L - \theta_{ms} \tag{7.4}$$

For TIPS-DAB parameters, the $d_H = 12.6^\circ$ and $D_H = \gamma = 15^\circ$ are fixed on MV NPC converter. The θ_p and θ_{mp} vary with the DAB load and are 5° and 8.62° respectively at full-load. Both margins increase towards light loading. Considering these factors α is around 24° at full-load and around 15.4° at 50% load. Similarly for LV converter ZVS d_L is fixed at 12.6° and θ_s is 5° at full-load. Fig. 3.6(b) shows the switching loss as a function of the MV converter duty cycle. The middle switch of the three-level converter marked as *energy*2 can be made to have zero switching losses that happens when the MV side converter operates at smaller ϕ and near unity power-factor. As the switching and conduction losses in this application have opposite requirement for minimum value turn-ratio, total loss still finds nominal point most efficient for 10 kHz. Total converter loss which depends not only on reactive power-flow but also on used device characteristics, become smallest for around nominal turn-ratio. The D-current reference is generated from look-up table which is a function of q-axis current for optimum-operation trajectory calculated analytically [88]. The optimum-operation ensures ZVS condition keeping minimum reactive power-flow in DAB magnetic components. Fig. 7.5 shows the power transfer as a function of duty ratio and phase angle. For one power level there can be various (D, ϕ) operating points. d-q control ensures ZVS operation of DAB, as it can maintain d-axis current independent of q-axis current by adjusting duty-cycle of primary converter and hence controlling primary voltage magnitude [86]. To calculate the optimum power-factor angle for DAB current, device switching-characteristics are taken in to consideration along with reactive power-flow. SiC IGBT turn-off losses are high and so current can not be let to lag by large angle from converter pole voltage. For minimum ZVS lag-angle, a margin for parasitic currents and dead-time are added to the converter zero-state angle. D-current reference is generated from look-up table which is a function of q-axis current for optimum-operation trajectory calculated analytically [81]. The optimum-operation is the one that ensures ZVS condition keeping min-

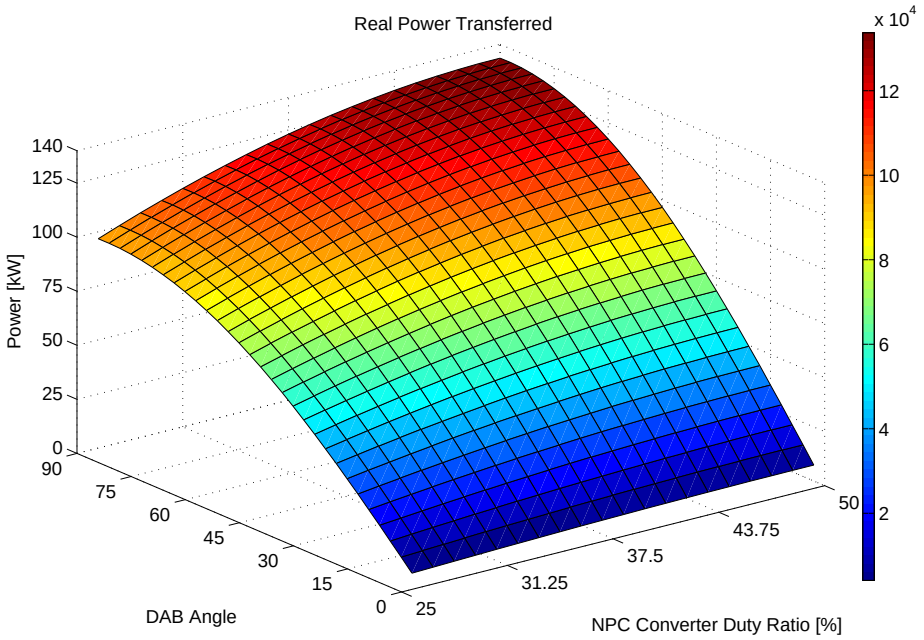


Figure 7.5: Y:Y/Δ DAB power-flow plot with duty and phase angle

imum reactive power-flow in DAB magnetics. Fig 4.29 shows the hardware results for soft-switching effect on current ringing and dv/dt slope.

7.4 Experimental Results

The hardware setup of MV DAB is shown in Fig. 6.12. It shows three NPC poles built using 15 kV SiC IGBTs, dc caps, bus-bar, heat-sink and gate-drivers with optical isolation. The FEC and DAB are 3ϕ converters and consist of 3 modular NPC poles each, built with 15 kV SiC IGBTs and 20 kV SiC JBS clamping diodes as described in previous chapter. This setup has been tested in standalone mode at 6 kV dc bus for 7.4 kW power transfer with the boost power supply explained in previous chapter. Above 6 kV, the TIPS AFEC is used as power supply and they have been integrated up to 8 kV maximum. The DAB currents show the expected ringing in the currents due to the transformers parasitics as expected in transformer characterization chapter. The DAB was pushed in steps in voltage to operate up to 6 kV and results captured for different conditions validating the ZVS understanding in this chapter. The CRC voltage probe with gain of 10000:1 are used to measure differential high-frequency high-voltage. The load resistor's are configured for fixed with 9 series connected banks of 4 parallel connected resistors, making it total rated 22.5 Ω and 40 A or maximum 36 kW rated. The DAB output reference voltage was increased in slow ramp in step proportional to boost output voltage, therefore load changes with output

voltage value for following experiments.

7.4.1 Different Power Comparison

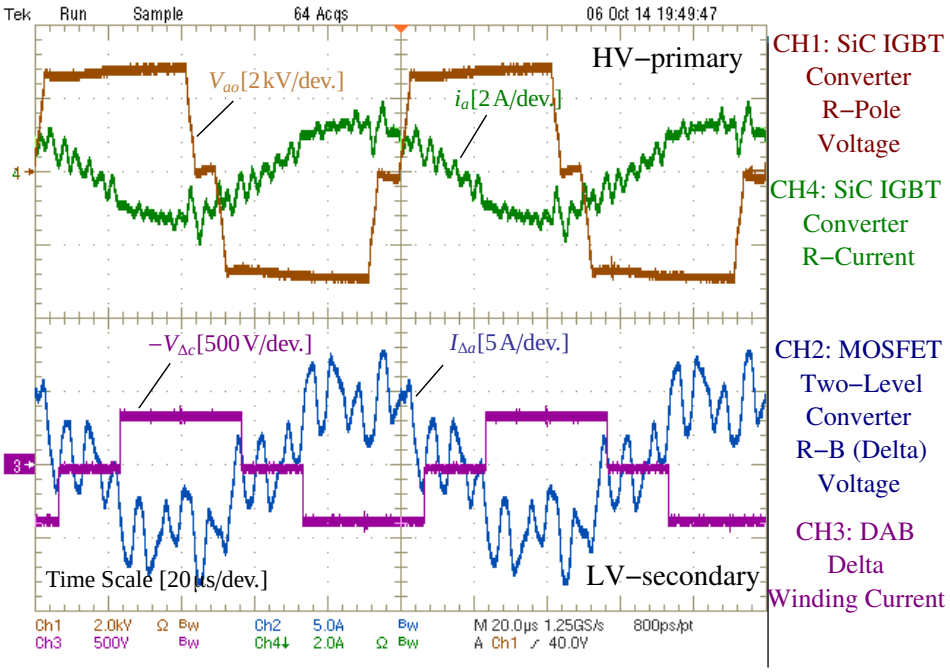


Figure 7.6: Y:Y/Δ DAB converter result at 6 kV-360 V dc, 4 kW, 10 kHz

Fig. 7.6 shows the DAB converter primary and delta secondary waveforms at 6 kV and 4 kW. The three-level pole works in ZVS mode here and the dv/dt is decided by the natural commutation in which the load current charges/discharges the device capacitances while the t_d is still active. Before the t_d ends the zero voltage must be reached for ZVS. To reach this condition the time required is too large at this high voltage and relatively small current level. Hence the 10 kHz frequency of DAB at this rating seems high for these devices. As expected, the DAB currents have ringing due to parasitics. The frequency of the ringing is same as calculated with net series inductance and the transformer shunt capacitance. Fig. 7.7 shows the frequency spectra of the converter result. It shows 300 kHz ringing on the MV side and an additional 150 kHz component on the LV side currents. Fig. 7.8 shows the converter result with 8-channel scope at a higher power rating of 6 kV-400 V dc, 7.4 kW three-phase DAB 10 kHz operation. This has been previously reported in [30]. In addition to primary and delta secondary waveforms, it shows the b phase MV voltage, star secondary line voltage and current. It can be seen from the V_{ao} shape and I_a that full ZVS is not occurring. The parasitic capacitances of devices are not discharged

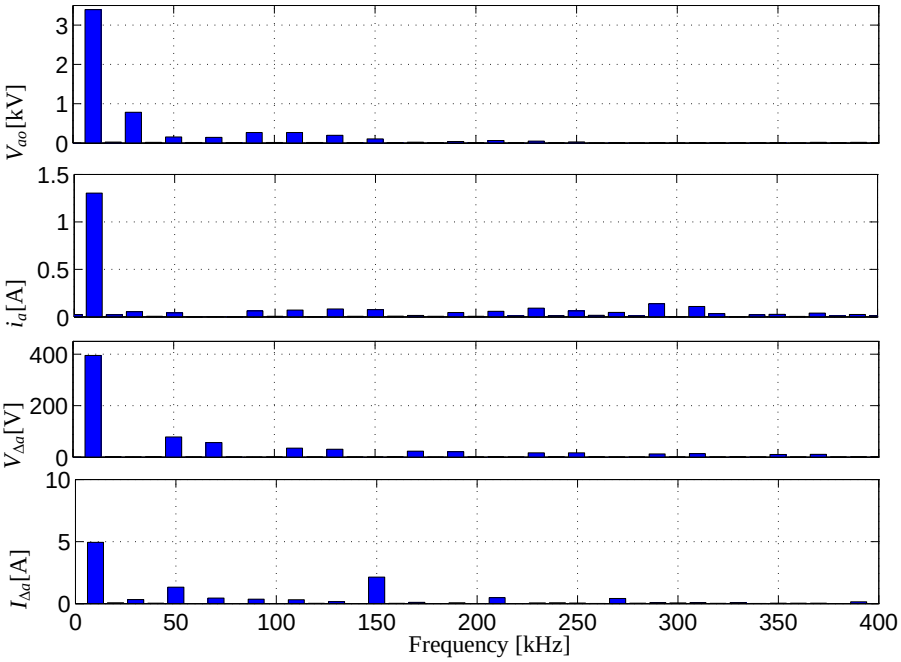


Figure 7.7: Y:Y/Δ DAB FFT of the waveforms at 6 kV-360 V dc, 4 kW

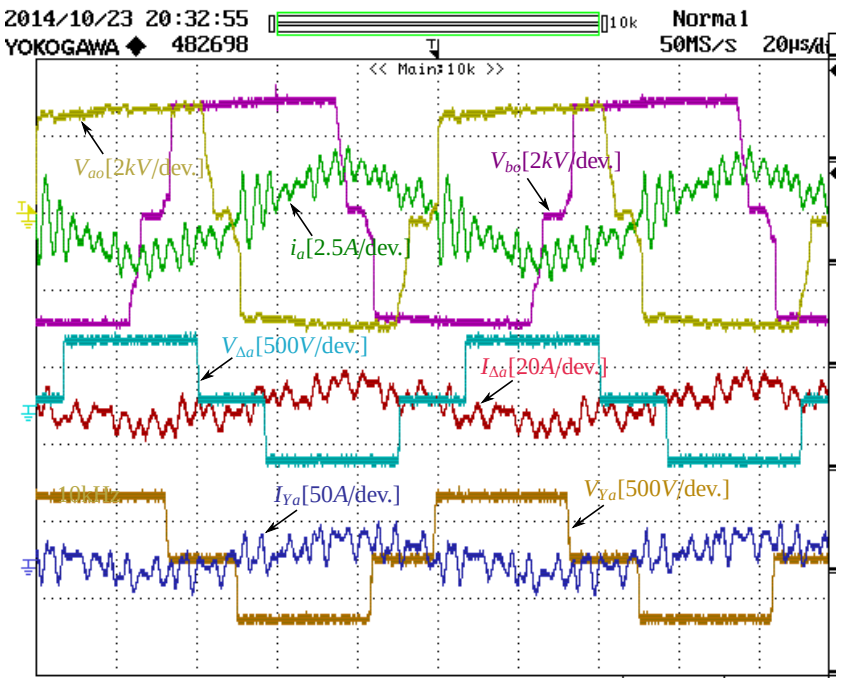


Figure 7.8: Y:Y/Δ DAB converter results at 6 kV-400 V dc, 7.4 kW, 10 kHz

fully to zero before the dead-time ends. Therefore two dv/dt slopes are occurring. The hard turn-on gives 30kV/µs. In comparison to Fig. 7.6, here the output dc voltage is 400 V instead of 360 V. Hence the ZVS is nearly lost and the V_{ao} dv/dt is 30kV/µs. V_{ao} and $V_{\Delta a}$ relative phase is the DAB ϕ. It is only 10°. The rated power is 25 kW at 6 kV and 40° phase.

7.4.2 Different Voltage and Voltage-ratio with Same Load Resistor

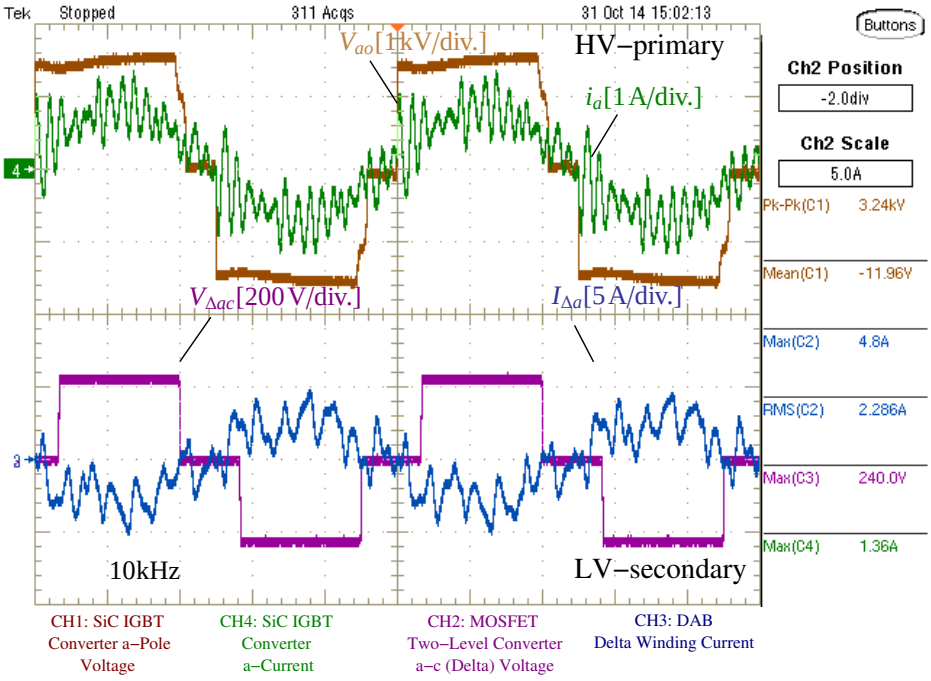


Figure 7.9: $Y:Y/\Delta$ DAB Converter Results at 3.24 kV-220 V dc, 2.15 kW

Fig. 7.9 shows the DAB results for 3.24 kV-220 V dc, Fig. 7.10 for 4 kV-240 V dc, Fig. 7.11 for 5.12 kV-300 V dc, Fig. 7.12 for 5 kV-340 V dc, Fig. 7.13 for 5.3 kV-350 V dc, Fig. 7.14 for 6.5 kV-400 V dc, Fig. 7.15 for 7 kV-400 V dc dc and Fig. 7.16 for 7 kV-420 V dc output. It is clear from these results that whenever the output to input voltage ratio is below or equal to 60 V per 1 kV-dc, full ZVS occurs and the dv/dt slopes are smoother otherwise partial ZVS or hard-switching occurs. Therefore to go up in voltage output was kept below according to this ratio for less EMI generation. Fig. 7.17 shows the maximum voltage DAB results at 8 kV-480 V dc, 10 kHz and 9.6 kW power. It shows primary and delta secondary side voltage & current. The figure does not show the star LV converter waveform due to limited channels on the remotely controlled oscilloscope for this voltage. The converter does not show any considerable heating and the losses seem to be similar to the expected calculation using the actual

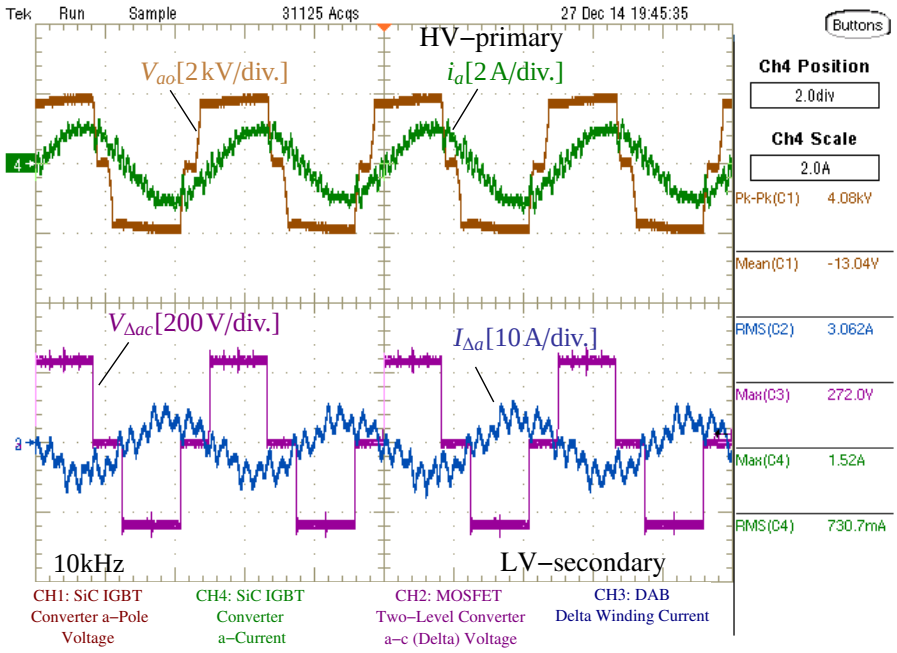


Figure 7.10: $Y:Y/\Delta$ DAB Converter Results at 4 kV-240 V dc, 2.56 kW

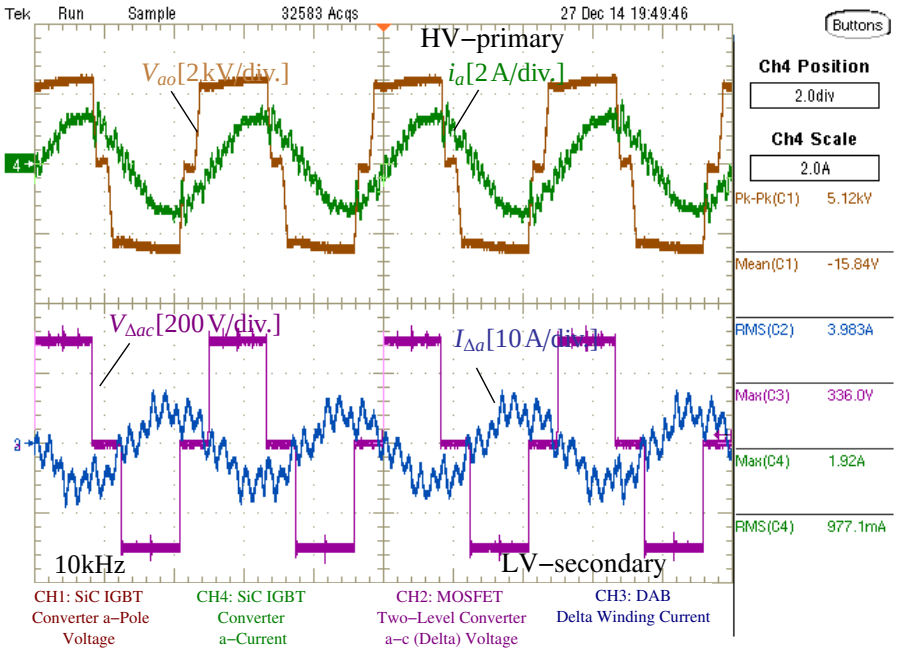


Figure 7.11: $Y:Y/\Delta$ DAB Converter Results at 5.12 kV-300 V dc, 4 kW

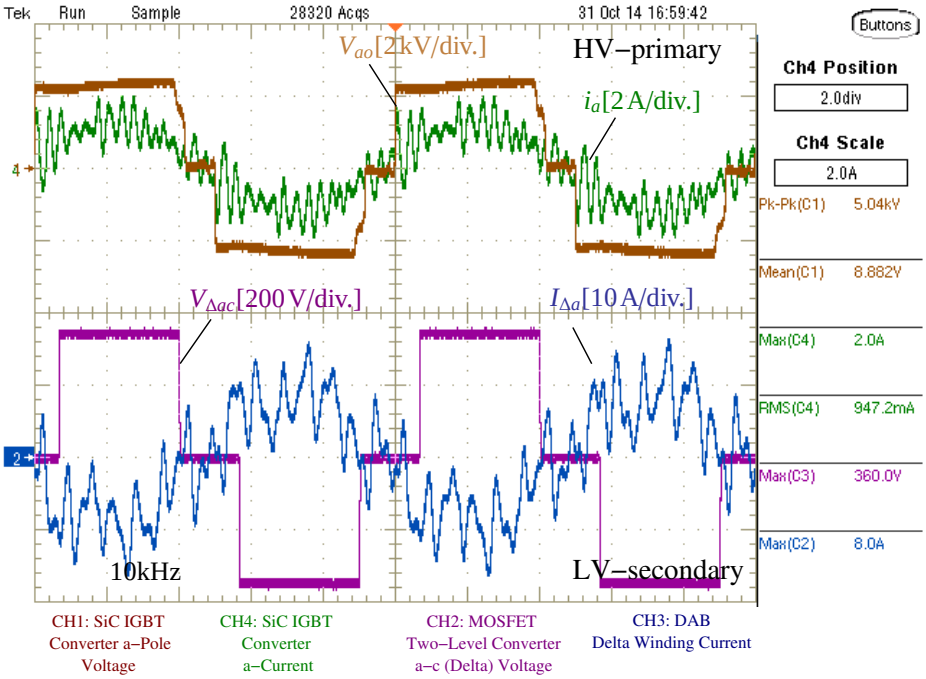


Figure 7.12: $Y:Y/\Delta$ DAB Converter Results at 5 kV-340 V dc, 5 kW

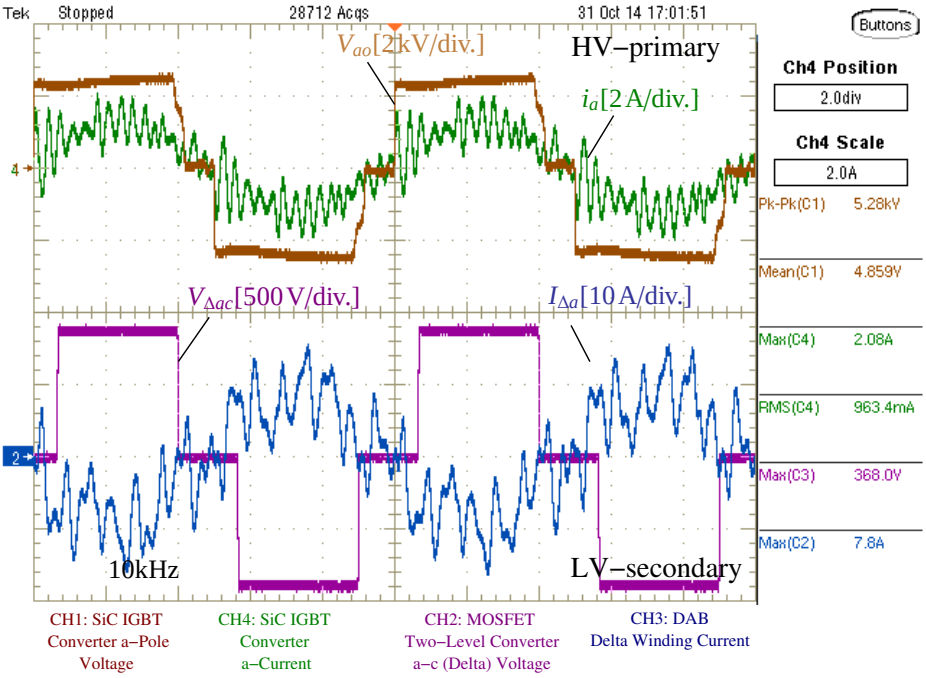


Figure 7.13: $Y:Y/\Delta$ DAB Converter Results at 5.3 kV-350 V dc, 5.5 kW

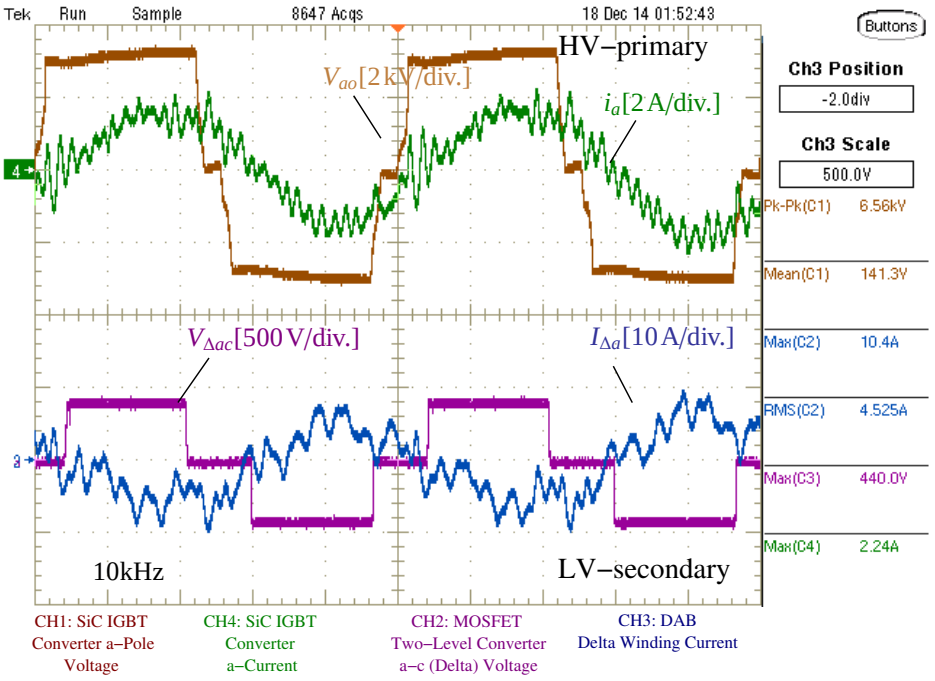


Figure 7.14: $Y:Y/\Delta$ DAB Converter Results at 6.5 kV-400 V dc, 7.11 kW

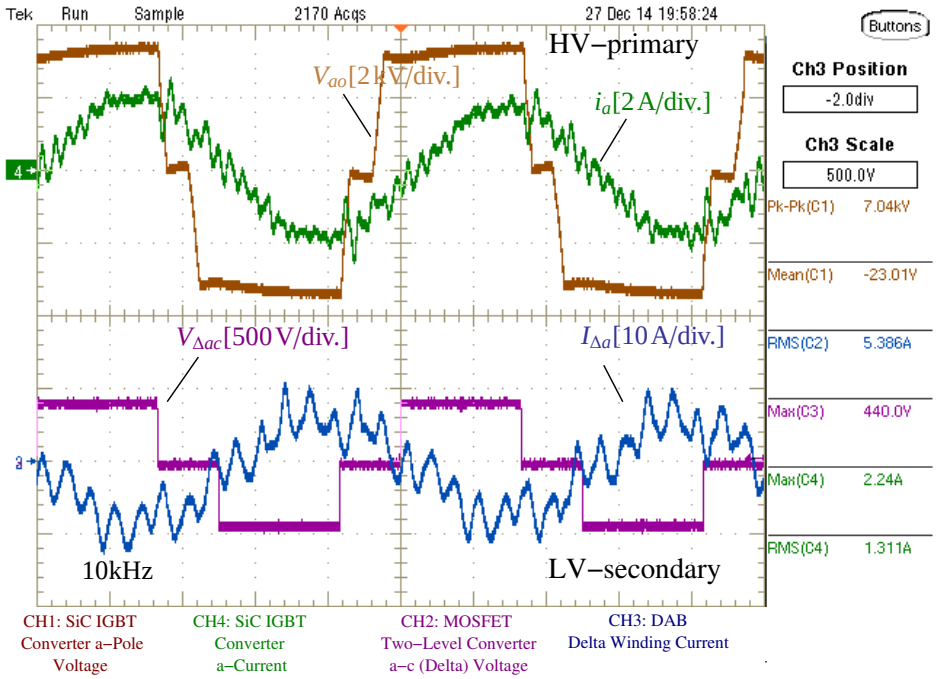


Figure 7.15: $Y:Y/\Delta$ DAB Converter Results at 7 kV-400 V dc, 7.11 kW

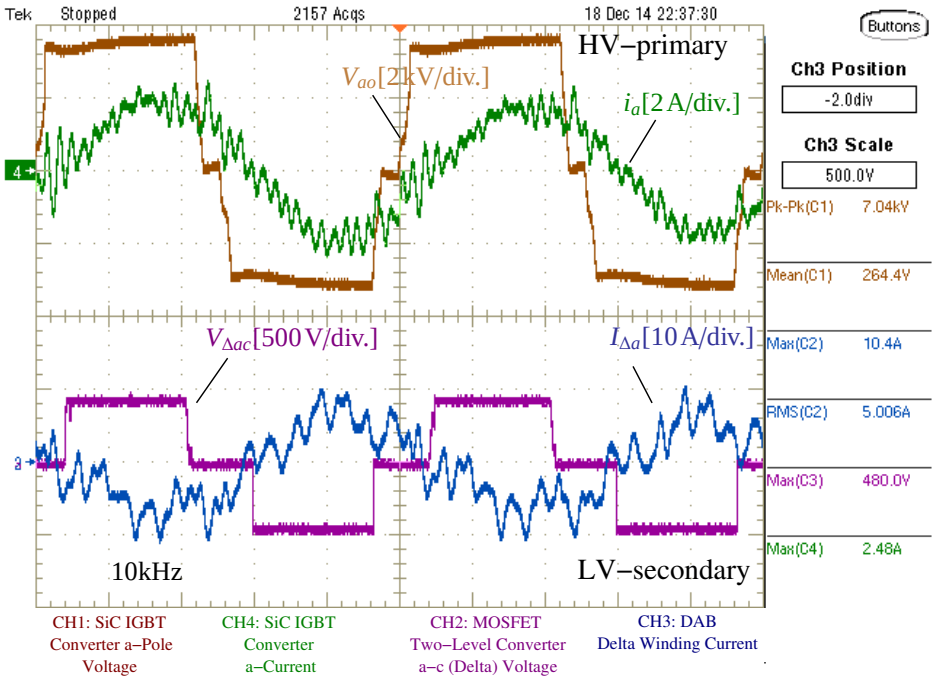


Figure 7.16: $Y:Y/\Delta$ DAB Converter Results at 7 kV-420 V dc, 7.84 kW

device hard-switching data and measurement of the circuit elements. In comparison to Fig. 7.8, here the output dc voltage is lower than that by turn-ratio (580 V). Hence the ZVS occurs for MV side and the dv/dt of V_{ao} is 2.5kV/µs. The V_{ao} and $V_{\Delta a}$ relative phase is the DAB ϕ. It is only 10°. The rated power is 50 kW at 8 kV and 40° DAB angle.

7.4.3 Different Frequency Comparison

Fig. 7.18 and Fig. 7.19 respectively show 3 kV-200 V dc, 4.5 kW results at 10 kHz and 5 kHz with the star line to neutral voltage. Due to parasitics the neutral has large oscillations and the line to neutral voltage is distorted for 10 kHz. It is smoother for the 5 kHz because the parasitic frequency matches and resonates with the 15^{th} harmonic of 10 kHz voltage. The 5 kHz operation reduces the DAB angle to half. It can be noticed that full ZVS is occurring compared to 10 kHz. There are two reasons for this, one is the reduction of DAB angle which increases the sensitivity of reactive power on the voltage ratio. This ratio is little less than 1.0 here and therefore it causes lagging primary current. Other reason is that reduction in ringing lowers the phase margin needed for ZVS. This result emphasizes the importance of parasitics when working at this high frequency at high voltage level and also validates the discussion in this chapter.

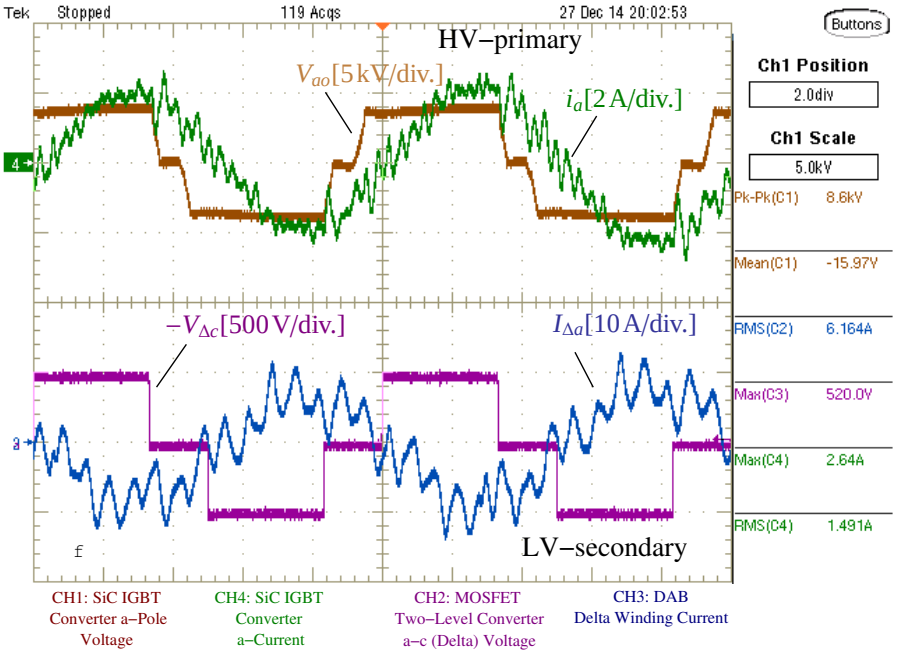


Figure 7.17: 8 kV-480 V dc, 9.6 kW, 10 kHz experiment of three-phase Y:Y/Δ DAB

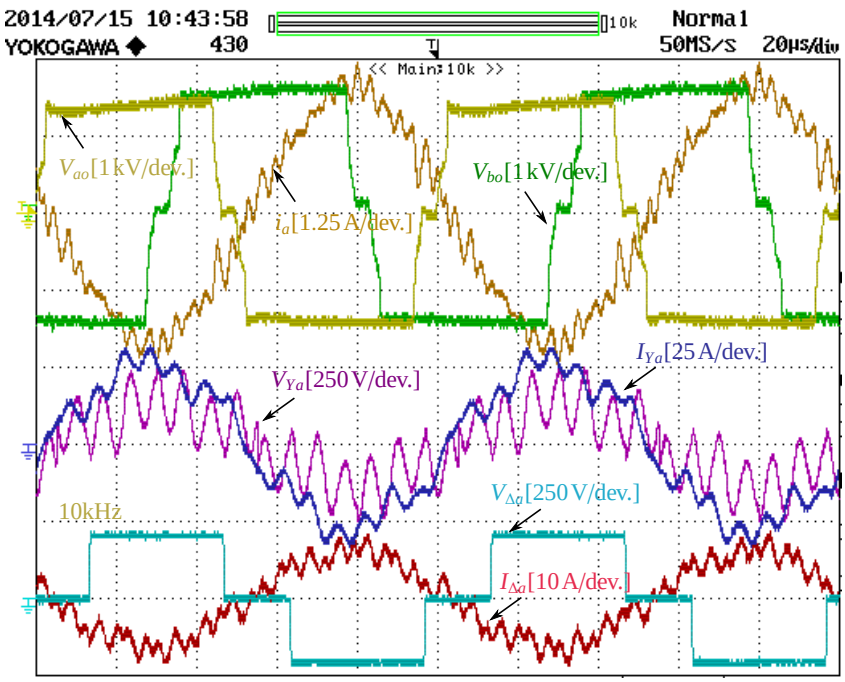


Figure 7.18: Y:Y/Δ DAB converter result at 3 kV-200 V dc, 4.5 kW, 10 kHz

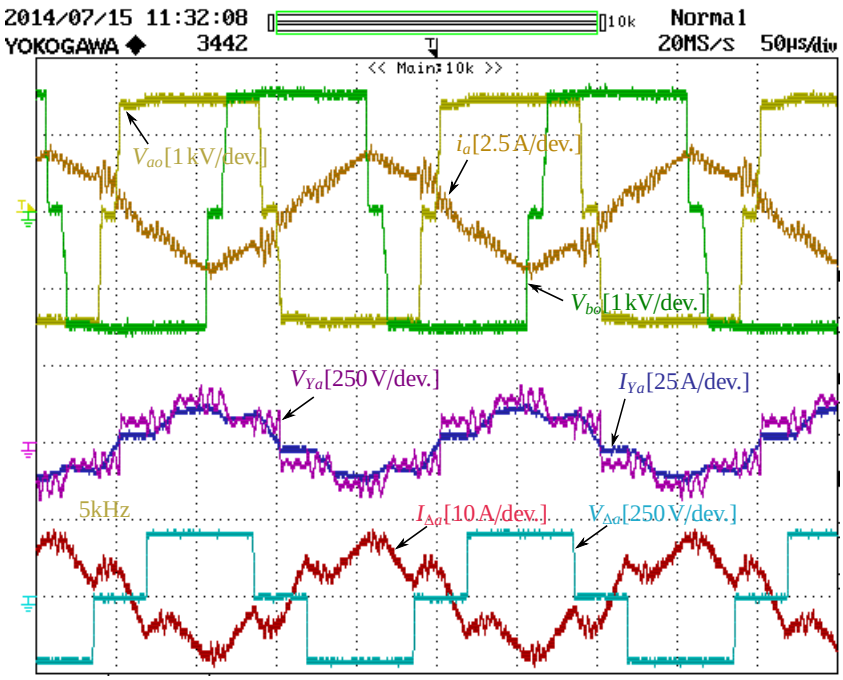


Figure 7.19: Y:Y/Δ DAB converter result at 3 kV-200 V dc, 4.5 kW, 5 kHz

7.5 Conclusion

Device characteristics are important in determination of optimum efficiency turn-ratio of the transformer and duty cycle in three-phase DAB along with minimum Q point which ensures minimum winding conduction loss for the DAB. The device dv/dt characteristic depends on the gate resistance up to punch-through voltage level after that it becomes high. A high dv/dt results in ringing in the device currents caused by parasitics, which effectively reduces the ZVS range. A low hard-switching dv/dt causes more switching losses and longer transition time which needs more dead-time (t_d). The pole capacitance also cannot be very high otherwise for ZVS, the t_d must be increased. The ratio of t_d to DAB period should not be high otherwise it reduces the ZVS range, reduce the pole-voltage, increase reactive power and deviate the DAB from its optimum efficiency point. The LV MOSFET converters have smaller dv/dt and t_d. Also the p.u. pole capacitance is low so it does not cause EMI or ringing problem also verified in the experimental results. Therefore the MV converter is more important to maintain ZVS since the hard-switching generates high dv/dt which causes EMI again verified in the different condition test results. The transformer turn-ratio can be selected such that the current vector lags the MV converter by a minimum magnitude as defined by ringing and t_d. This may result in non-ZVS mode operation for LV converters at light loads. The D control provides a little flexibility for optimum operation as it may result in non-ZVS mode and also deteriorate the current shape which is important for d-q control. It limits ZVS range and draws higher reactive power due to mismatch in volts/turn on primary and

secondary of transformer. So only voltage control has been implemented in the MV-DAB hardware with 41.6% MV duty-ratio and analysis have been validated with final 8kV results. This dc voltage is sufficient for 4.16kV MV grid AFEC interface application. The 5kHz operation result validates the presented ringing and ZVS reasoning.

Chapter 8

Flexible Operation of the MV Y:Y/Δ Dual Active Bridge

8.1 Introduction

The light load Y:Y/Δ DAB operation remains a concern due to the inter-dependence of pole voltage, dv/dt and ZVS condition, on the parasitics and dead-time [30]. The compact size MV-HF DAB transformer has significant parasitic capacitances for such voltage. The high dv/dt hard-switching characteristics of the developed IGBTs added to the parasitics, cause EMI issues and increased switching loss especially at light load due to the loss of ZVS. For MV side ZVS, the current needs to lag behind primary-voltage by a certain phase-angle defined by the non-ideal parameters. But for the secondary side ZVS, the DAB angle needs to be extended. To temporarily solve this problem, the output dc voltage is kept lower than the rated value in the presented experiment. This causes a lagging current to meet the ZVS for MV converter at the cost of losing ZVS for the secondary. This is acceptable considering high dv/dt generation at MV during hard-switching [40, 41]. Some relevant methods for flexible light load DAB operation are presented in [77, 105, 106]. Any additional component for the already complex topology is not desired. The concept of operating the three-phase as single-phase DAB is highly applicable for this MV DAB topology [77]. The concept of using dual leakage transformer DAB with variable frequency may be partially suitable as the operating frequency of the 15 kV SiC IGBT is selected as 10 kHz based on its switching characteristics, but one of the secondary converters which make two parallel independent DABs, can be switched or hold based on the requirement [105]. The burst mode light load operation may not be suitable for this MV DAB as it causes multiple switching [106]. The PWM control of one side converter in buck/boost mode to match the transformer applied voltages is very applicable but due to half-bridge 2-level at the secondary it can be only applied at 3-level primary here in buck mode [107].

This chapter demonstrates 15 kV/40 A SiC IGBT based DAB is at 8 kV test results. This enables a

4.16kV MV grid interface together with the AFEC reported in [29]. This chapter addresses the wide range loading efficiency and EMI issues by utilizing the dual secondary converters as Single Active Bridge (SAB) or hybrid mode. A lagging current is required for the ZVS and lower dv/dt on the MV side converter. For this the output side voltage can be reduced but this forces secondary converters out of ZVS and also drive higher reactive power causing conduction losses. By switching-off one of the secondary converters, the DAB is transformed into a hybrid of SAB and DAB. Theoretically the DAB angle can be doubled as the series inductance is concentrated mainly on secondary side converters. This can be helpful to maintain ZVS in wide range loading. Also the switched off converter offers zero switching loss. The chapter presents extended ZVS mode by utilizing the complex topology. It also presents simulations considering all parameters to bring out the advantages and the approximate efficiency. It also presents experimental results for extended ZVS mode.

8.2 Extended ZVS Mode of Operation

There are a couple of motivations to use this composite topology: 1. Reduction of harmonics in the primary current for d-q control, 2. Utilizing 1200V/100A MOSFET device based three-phase converters to transfer 100kW shared by the two secondary converters [101].

8.2.1 DAB ZVS Constraints

One simple method for MV ZVS is to simply keep the DAB output voltage low so that it operates in buck mode. This makes the DAB current always lagging with respect to MV pole voltage resulting in ZVS. This is also effective in reverse power-flow mode as well. Yet this is not an optimized way as it results in higher conduction loss at higher load and once the system design is fixed, any deviation in operating Voltage-Ratio (VR) reproduces non-ZVS mode. So a practical method needs to be employed. Since the experiments are done in buck mode for ZVS on MV side, the advantages of hybrid mode is seen at rated VR in simulations. So LV voltage is kept 580V for 8kV MV dc.

Fig. 8.1 shows MV side switch waveforms the DAB simulation for 15% load in normal mode. It can be seen that ZVS is lost for top switches. This generates EMI problem as well as turn-on losses. Though these MatLab-PLECS simulations are not able to show the effect of natural soft turn-off occurring due to device parasitic capacitance, the actual turn-off switching losses are expected to be much smaller. This further increases the advantage of maintaining ZVS for MV side. Fig. 8.2 shows the LV switch waveforms in the same condition. The MV duty-ratio is 45%.

8.2.2 Duty-ratio Droop Control

A simple light load ZVS technique is the MV converter duty-ratio incremental droop control where it is increased towards light load all the way to 50%. But at zero load it disables the advantage of three-level

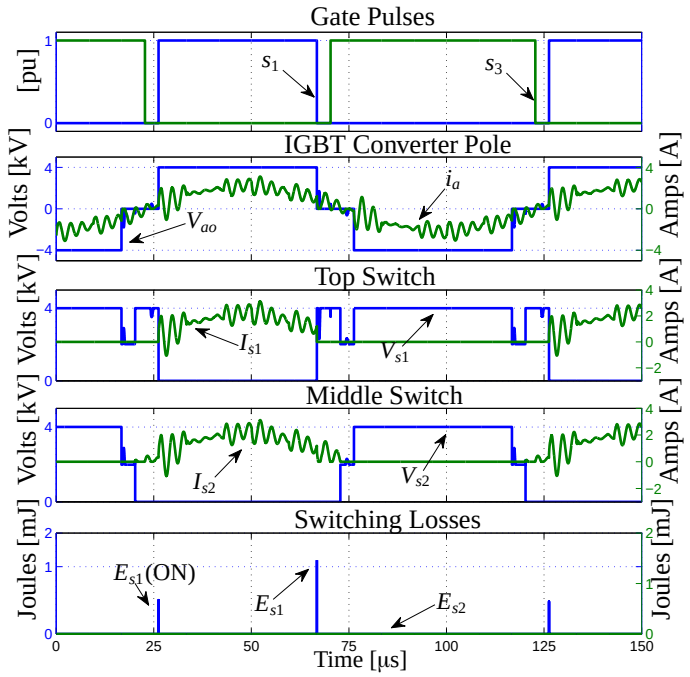


Figure 8.1: DAB simulation in normal mode at 15% load: primary switches

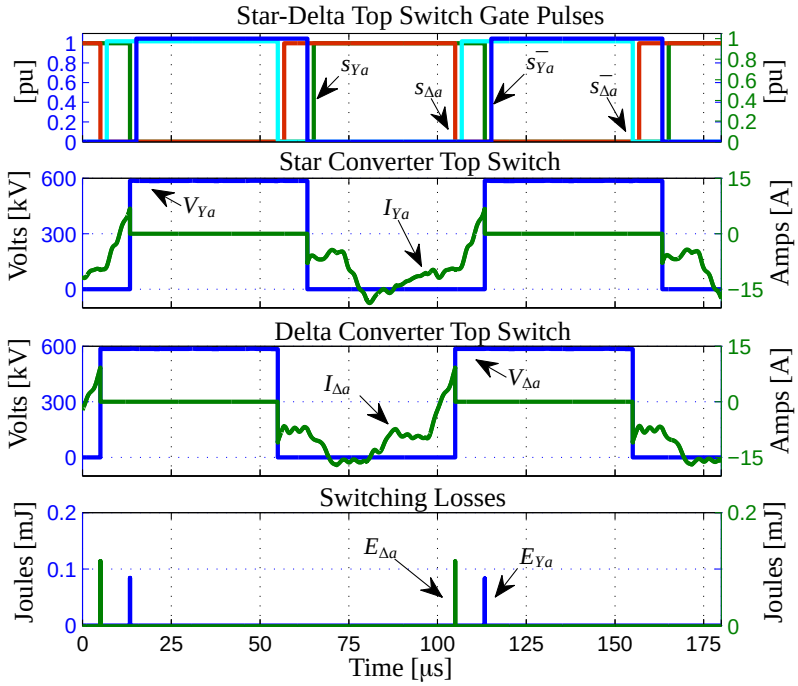


Figure 8.2: DAB simulation in normal mode at 15% load: secondary switches

smoother voltage transition.

8.2.3 Hybrid Mode

With Y:Y/Δ topology consisting of dual secondary windings, it is possible to switch off one of them at light load (< 35%). Since the DAB inductance is mainly concentrated on secondary side in the form of external inductors. The two secondaries are nearly decoupled from each other. Therefore this increases the voltage angle for the switching converter pair and their available ZVS range nearly doubles. But the switched off secondary converter still has its anti-parallel diodes in circuit. They conduct in buck mode of operation as a SAB converter. But the current flowing is dependent on VR and is smaller with loading due to drop in the inductors compared to the DAB current. The DAB action applies 1 pu voltage at 60° phase, which generates current in same magnitude as the SAB supplying secondary short circuited. Also the current phase generated by DAB action is at 30° with respect to voltage vectors while for SAB it is lagging nearly 90° of the active bridge voltage vector. Fig. 8.3 shows the DAB simulation

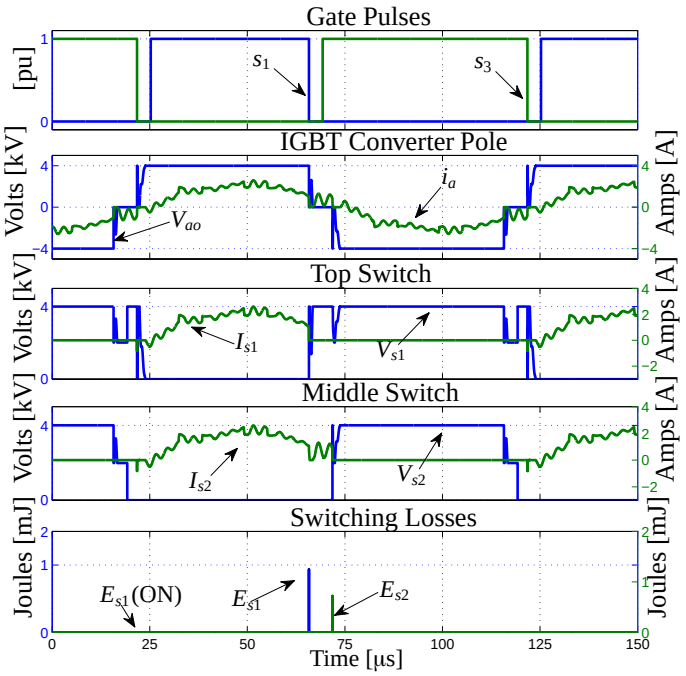


Figure 8.3: DAB simulation in hybrid mode at 15% load: primary switches

at 15% load with the delta LV converter off (diode mode). The converter works in ZVS mode now as the SAB operation draws smaller than 50% current from the MV converter. Effectively the DAB angle is increased which causes more lagging current drawn from MV converter. This causes ZVS as shown

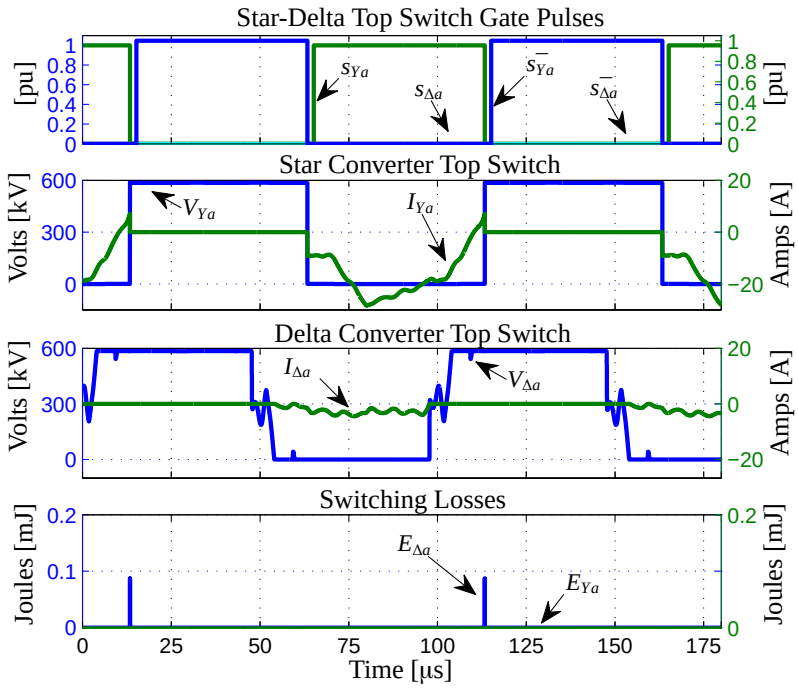


Figure 8.4: DAB simulation in hybrid mode at 15% load: secondary switches

in Fig. 8.3. Fig. 8.4 shows the LV switch waveforms in the same condition. The Δ converter no longer switches and its current depends on voltage-ratio mismatch. Thus the hybrid DAB and SAB operation at light load boosts the DAB efficiency due to reduction in switching losses as shown in Table 8.1. This reduction is not only contributed by switching off one of the secondary converters but also due to reduction in switching loss of MV converter. This also improves the DAB performance in light of the interaction of parasitic capacitances and the dead time. As there is more lagging current for the primary MV converter causing its pole voltage to be smooth. But this advantage is moderated by the increased conduction losses occurring in now just one current path. For given MV DAB setup, the R_{ac} of the series inductors are quite high and that is further moderating the advantages. As explained earlier these simulation based predictions give worst case loss data for turn-off. The advantage of hybrid mode is expected to be more visible in practice and for high-power MV DAB. The main advantage of maintaining ZVS is EMI reduction for the MV DAB [30]. But in these simulations a slight increase in current lag causes more tun-off losses. A drawback is that secondary dc voltage ripple magnitude doubles and frequency becomes half. But the limitation of this method is that in buck mode VR, there is an uncontrolled power flow from SAB and the DAB has to operate in reverse mode to keep the net power same. This only generates more conduction loss. The solution is to control MV duty-ratio such that ac voltage-ratio is matched. But limiting the MV duty-ratio makes it hard-switched as explained earlier. Hence this scheme might only be suitable till mid power range. For extreme light load, the DAB

Table 8.1: DAB expected losses and efficiency at 8kV-580V

Parameters Mode	Full Load	15% Load	Δ OFF	Y OFF
MV Switching	344.8[W]	95.94[W]	88.65[W]	99.26[W]
LV Switching	34.6[W]	11.87[W]	7.23[W]	5.21[W]
MV Conduction	108.6[W]	28.08[W]	29.4[W]	27.1[W]
LV Conduction	206.3[W]	47.7[W]	51.8[W]	50.0[W]
Total Conv. Loss	694.4[W]	183.6[W]	177.1[W]	181.6[W]
Total Copper Loss	757.2[W]	79.4[W]	100.2[W]	107.3[W]
Core Loss	31.7[W]	31.7[W]	31.7[W]	31.7[W]
Total DAB Losses	1483.4[W]	294.8[W]	309.1[W]	320.6[W]
Output Power	48.97[kW]	15.72[kW]	16.15[kW]	15.47[kW]
Converter Efficiency	98.60[%]	98.84[%]	98.91[%]	98.84[%]
Aggregate Efficiency	97.06[%]	98.16[%]	98.12[%]	97.97[%]

should be operated near 50% MV duty-ratio and let the LV side hard-switch. There is no advantage of using flexible operation of dual windings in higher load (> 40%) as it only causes more MV turn-off and DAB conduction losses.

8.3 Experimental Results

Fig. 8.5 and Fig. 8.6 respectively show 3kV-200V dc, 1.8kW results at 10kHz, for normal and hybrid mode (Δ pulse off). The hybrid operation increases the DAB active vector angle to nearly double. The turned-off Δ converter is in SAB diode rectifier mode and the current is governed by VR. The experiments are done at buck mode so the SAB current is higher and the DAB pair has to flow power in reverse direction as visible in polarity of Y current. This is not optimum from conduction loss point of view but it maintains ZVS. Fig. 8.7 shows the expanded view of the MV pole waveforms in above results for comparison. It can be noticed from smoother dv/dt slopes in V_{ao} that full ZVS is occurring compared to the normal operation where partial ZVS is occurring with steeper dv/dt. There are two reasons for this, one is the increase of DAB angle for same power but only one DAB path active. Other reason is that VR is near turn-ratio, so there is no forced lagging current in the MV converter. The steeper dv/dt comes on condition that dead-time period gets over before the anti-parallel diode could discharge the combined parasitics to zero volts.

8.4 Conclusion

The proposed light load ZVS range extension for a composite MV-HF DAB using its hybrid operation has been validated through simulations and MV side 3kV dc experiments. The expected efficiency improvement is verified from the MatLab-Plecs loss analysis using actual switching data, but it is worst

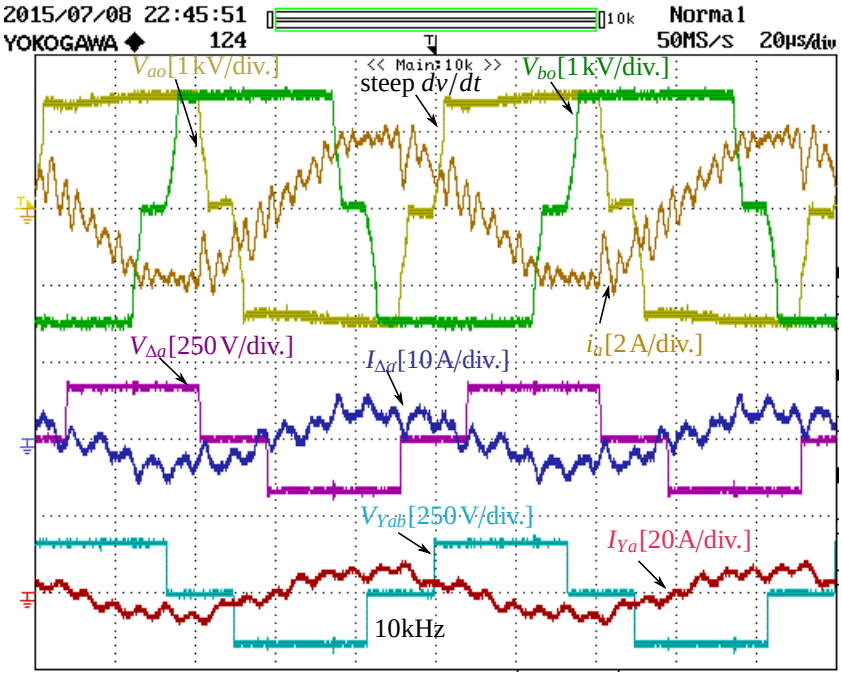


Figure 8.5: Normal mode with partial ZVS at 3 kV-200 V dc, 1.8 kW, 10 kHz

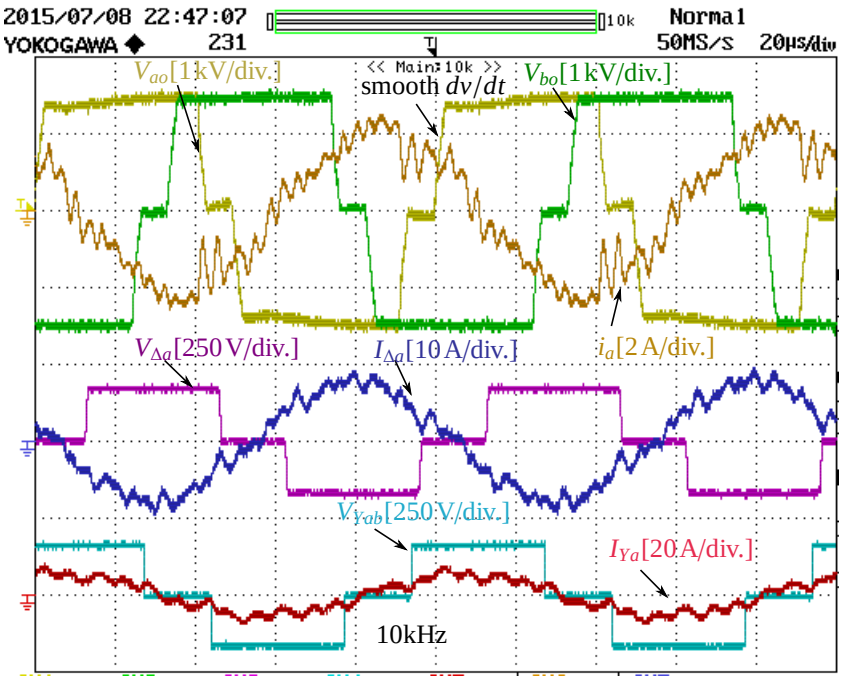


Figure 8.6: Hybrid mode with full ZVS at 3 kV-200 V dc, 1.8 kW, 10 kHz

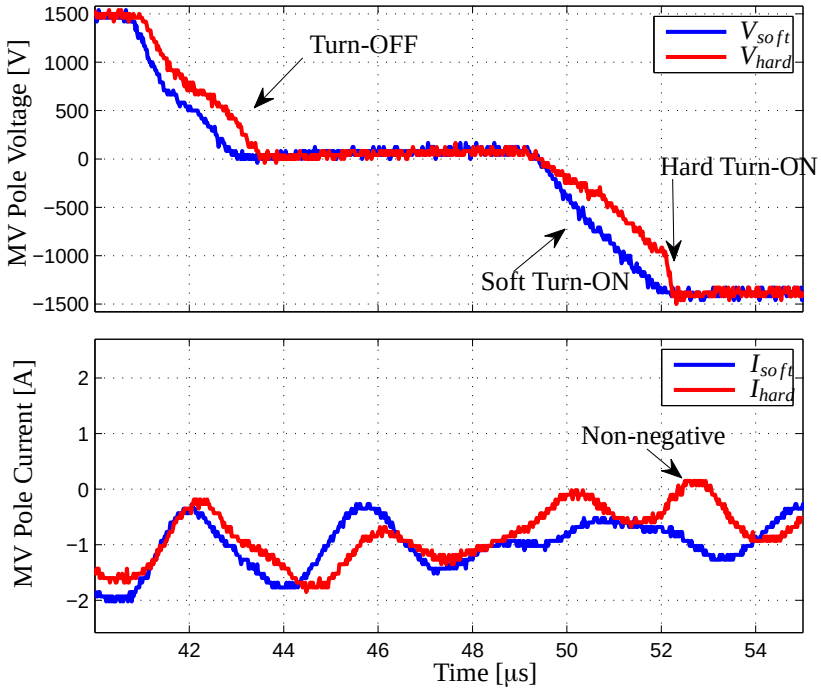


Figure 8.7: Comparison between partial and full ZVS switching

case as it ignores the soft-switching effect of device parasitic capacitance. The ZVS improvement is clearly verified from the test results of both cases at the light load. The topology has been demonstrated in the normal mode at 8 kV dc bus that makes it eligible for direct grid connected AFEC integration. The dual output converters provide flexibility for ZVS and also increase the reliability of the system, as the failure of one secondary switch does not necessitate to the shutdown of the system.

Chapter 9

Integration and Grid Connected CM Noise Considerations of Transformer-less Intelligent Power Substation (TIPS) System

9.1 Introduction

An important challenge for the TIPS/SST technology is the common-mode (CM) switching noise, which might not only limit it from operating at its rated high voltage but also might interfere with other systems near the coupling points. The high-frequency (HF) EMI can also affect the control electronics. The SiC based converters operating at the MV level generate high magnitude and high dv/dt CM voltage which makes TIPS system parasitics significant. The dv/dt of 15 kV SiC IGBTs, responsible for HF EMI noise, can be as high as 110 kV/µs above its 6 kV punch-through level [40]. The propagated CM noise depends on the operating voltage, dv/dt and path's impedance in the system. The major parasitic capacitances are formed in MV-HF transformer inter-winding capacitance (C_{ps}) [30], device to heat-sink [40], heat-sink to ground and other live surfaces including load to the ground as shown in Fig. 9.1. Since the grounding is required to define the potential of floating surfaces and the output of the TIPS for uninterrupted operation and safety, there would be circulating CM currents determined by the MV-HF transformer C_{ps} [108]. These currents would fail the SST/TIPS system for EMI qualification if not attenuated. The shielding and grounding of the MV winding for a MF transformer was presented in [109] to minimize the C_{ps}. But the shielding that needs to be grounded, increases the lumped capacitance to ground (C'_p). The transformer shielding if grounded for TIPS system, would generate triplen harmonic currents in the DAB MV side. This is not allowable due to control requirements and resonant oscillations caused by inductor

and transformer parasitics. Also the shielding complicates isolation design. Thus shielding solution for CM reduction can not be used in TIPS. For a typical low power SMPS, the MV-HF transformer has a weak C_{ps} CM path which is generally ignored when the output is grounded. In MV SST, the cost and size constraints in the transformer design, introduce significant C_{ps} in the MV-HF transformer. The problem of CM currents in ac-dc converters and inverter fed drive systems has been well known and addressed in literature [50, 110, 111]. However, there is a dearth of study on the CM and grounding issues for the SST systems.

This chapter proposes aptly designed non-capacitive grid coupling CM chokes and passive components for grounding at suitable locations in TIPS system to limit CM noise propagation [23]. The MV converter heat-sinks are connected to their dc mid-points to suppress the spurious converter tripping in TIPS by defining a known voltage to it [28]. The MV dc bus also needs to be grounded using passive components to locally bypass its CM noise. Other paths such as through the controls, gate-drivers (GD) and power-supplies are taken care of EMI with CM chokes and very small ($< 4\,\text{pF}$) gate-driver isolation capacitances [40]. The current-sensors (CS) and voltage-sensors (VS) cables are shielded and grounded to the lab-ground using EMI chokes towards the control termination as shown in Fig. 9.1. The shielding is always grounded to source ground. In this chapter, each converter stage is represented by its CM voltage and impedance similar to [52, 51]. Table 9.2 shows important component parameters of the TIPS system for CM study. A passive filter specification is generated based on this simple model in frequency domain. This chapter first presents the DAB transfer functions interacting with cascaded AFEC transfer functions to make stable TIPS integration. It then describes the TIPS topology and its control operation. The contributions of different stages on the CM generation are also discussed. The importance of grounding TIPS and the need of CM filters are also explained. A CM equivalent circuit is developed based on the major parasitic paths identified in the actual setup for filter calculations. A passive filter specification based on the simple calculation for FCC standard is also presented. The time domain simulations verifying the effectiveness of the CM filter in rated TIPS considering measured parasitics are presented. The characteristics of developed chokes are also presented. The MV TIPS integration lab demo results for $4.16\,\text{kV}$ grid connected operation after implementing some of the grounding considerations, are presented after that. Lastly the LV prototype TIPS grounding experiments implementing complete grounding solution, are presented.

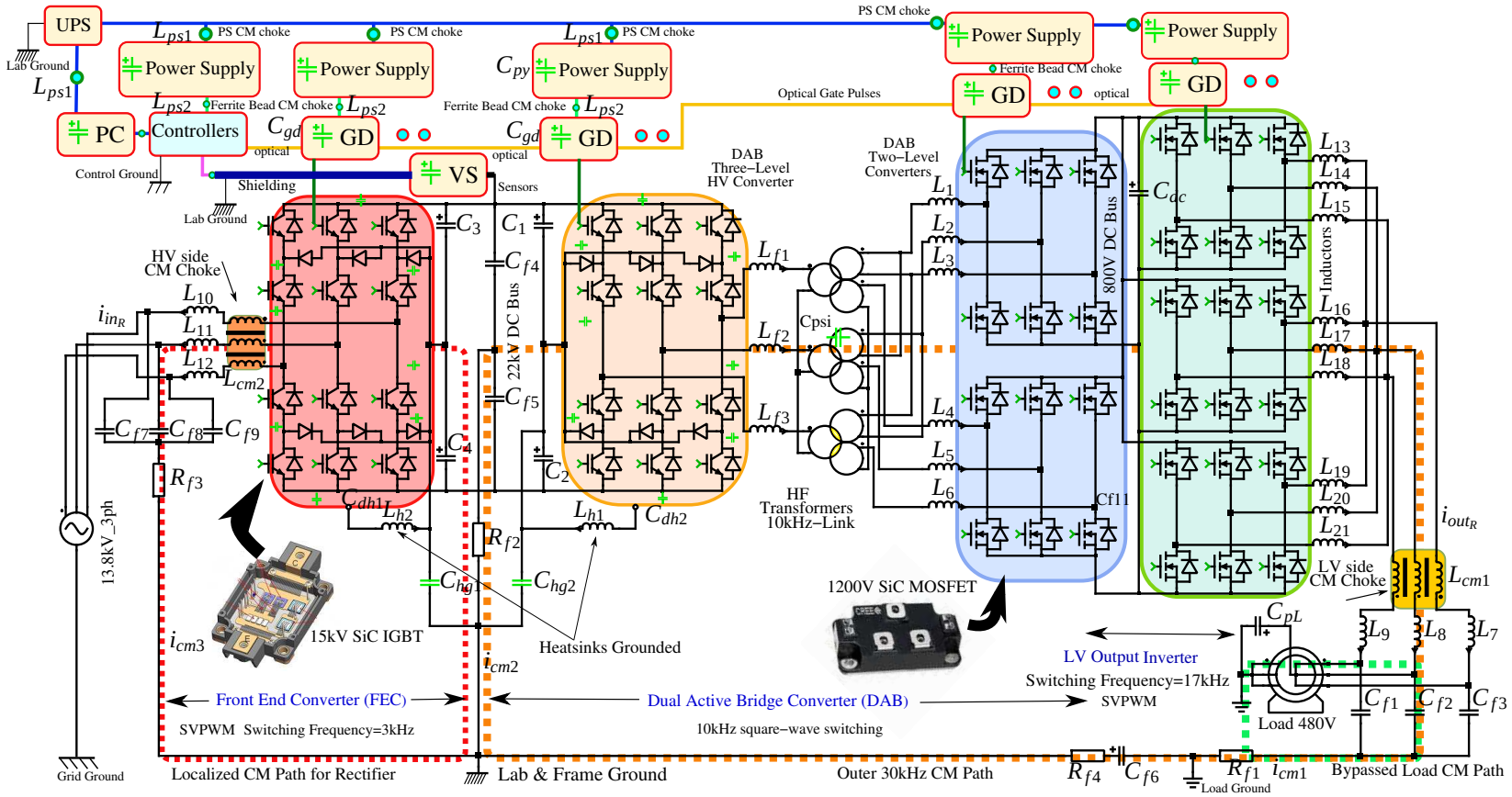


Figure 9.1: Schematic of the TIPS system with proposed CM filter solution for grounding

Table 9.1: MV TIPS parameters

Parameters	**Value[Units]**
Grid line-line voltage	13.8kV
AFEC switching-frequency	3kHz
MV dc voltage	22kV
DAB switching-frequency	10kHz
LV dc voltage	800V
Inverter switching-frequency	17kHz
Real power transfer	100kW

Table 9.2: TIPS rated passive components and parasitics

Parameters	**Value[Units]**	**Parameters**	**Value[Units]**
L_{h1} to L_{h2}	1.8mH	L_{ps1}	2mH
$Z(L_{ps2})$	50Ω@10MHz	C_{gd}	4pF
C_{dh1} to C_{dh2}	500pF	C_{py}	20pF
L_1 to L_6	80μH	C_{ps1} to C_{ps4}	300pF
L_{f1} to L_{f3}	400μH	L_7 to L_9	0.5mH
L_{10} to L_{12}	280mH	L_{13} to L_{21}	0.5mH
C_{10} to C_{12}	3nF	C_{13} to C_{21}	1nF
C_{f4} to C_{f5}	0.080μF	C_{f6}	1000nF
C_{f7} to C_{f9}	0.080μF	C_{hg1} to C_{hg2}	200pF
R_{f1}	100Ω	C_{pL}	500pF
R_{f2}	50Ω	C_p	50pF
R_{f3}	50Ω	C_{VS}	50pF
C_{f1} to C_{f3}	1μF	R_{f4}	50Ω

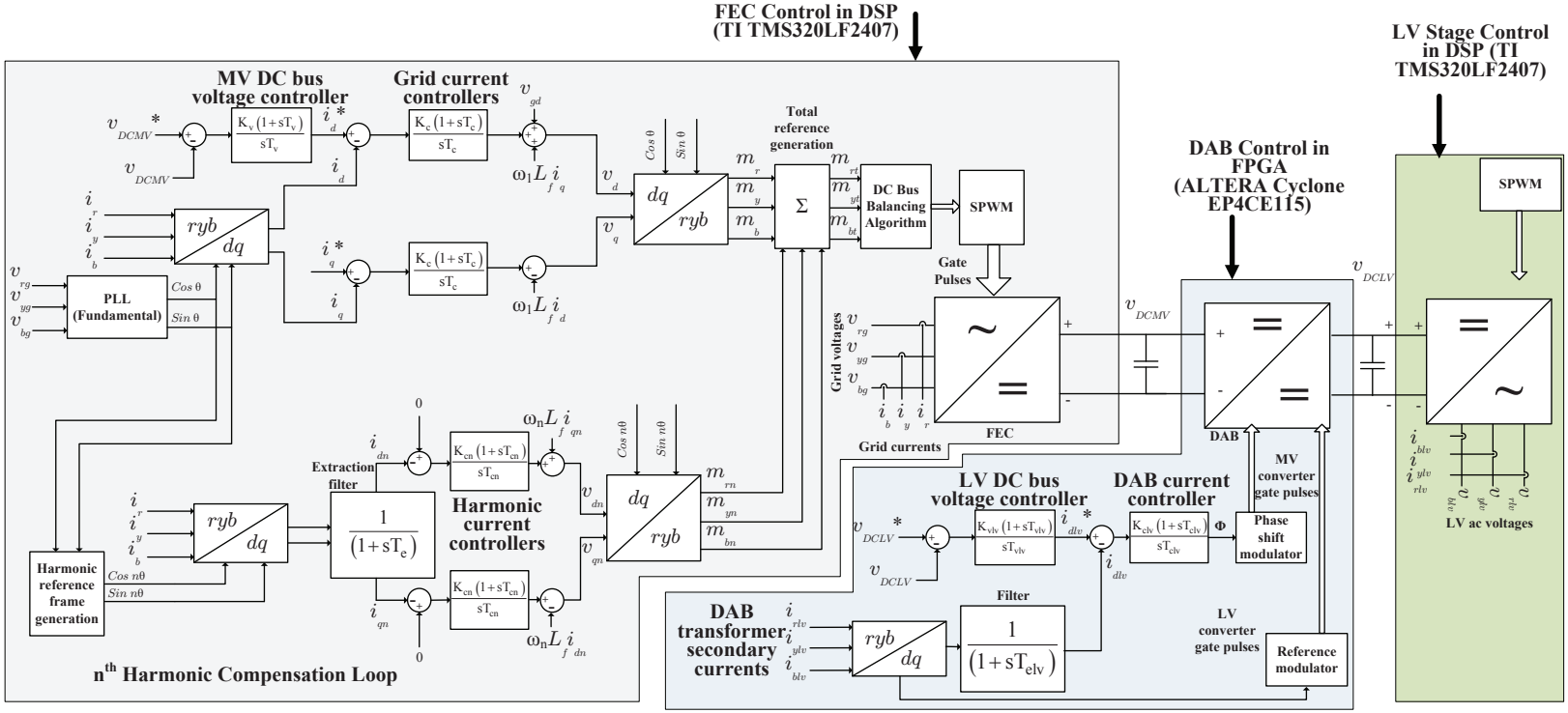


Figure 9.2: TIPS system complete control block diagram

9.2 TIPS Operation

TIPS DAB inductors are designed with differential noise considerations for the device characteristics and transformer parasitics [30]. Similarly the TIPS AFEC inductors with lower parasitics are specified and selected such that the given dv/dt does not produce high differential noise [29]. The 800 V dc is converted to three-phase 480 V ac using the LV inverter module. The complete schematic of TIPS with grounding is shown in Fig. 9.1. Table 9.1 shows rated parameters of the TIPS system. As shown in Fig. 9.1, the 15 kV SiC IGBTs based three-level neutral-point-clamped (NPC) converters are used on the AFEC stage and MV side of the DAB stage. The 1200 V SiC MOSFET based two-Level (2L) converters are used on the LV side of the DAB and the LV output inverter. Fig. 9.2 shows the control block-diagram for entire TIPS system. It has three independent controllers for three stages of the TIPS system. The AFEC regulates its MV dc bus at 22 kV using vector-control based on 3 kHz space-vector PWM switching [29]. It is capable of independently controlling reactive and real power flow that makes this stage useful also as a reactive power compensator for some applications. The harmonic control loop takes care of dead-time and grid induced harmonic currents. As shown in Fig. 9.2, the DAB draws power from 22 kV dc bus and regulates the LV dc bus at 800 V using phase-shift control of square-wave switching at 10 kHz. As shown in Fig. 9.1, the DAB MV NPC converter is connected to the primary star-configured windings of three single-phase MV-HF transformers. The DAB MV poles are switched in quasi-square with 41% duty-ratio and 120° mutual phase-shift to construct a 3-ph space-vector [30]. A pair of LV 2L converters are connected to the dual secondary-windings configured in star-delta manner. The 3-ph pairs are balanced with 120° phase-shift and the star-delta 3-ph pairs operate in 30° mutual phase-shift such that they produce synchronous fundamental flux in the transformer to construct the corresponding secondary side space-vector. This arrangement establishes near sinusoidal ac current on the primary star winding of the MV-HF transformer [30]. The DAB controls generates phase and duty functions to operate it in ZVS over wide load range. The 17 kHz, 120° interleaved PWM switching LV inverter stage as shown in Fig. 9.1, draws power from 800 V dc bus and maintains its 3-ph ac rms voltage in closed-loop for feeding the load/grid. The interleaved operation of converters reduces the differential filter size because the effective switching-frequency is 51 kHz but the CM filter size does not reduce. This topology as proposed in [11] is chosen based on the TIPS rating, efficiency promised, ZVS switching criteria and the available 15 kV SiC IGBTs and 1200 V SiC MOSFETs SOAs [45].

9.3 TIPS Impedance Analysis for System Integration

After the closed loop control system is designed for the DAB taking transformer parasitics into consideration, it is important to evaluate the input impedance, output impedance and noise voltage gain of the DAB for open and closed loop. This is due to the fact that two stable cascaded converters might still make an unstable system together [112]. Similarly AFEC system impedances are modeled for integra-

tion stability study. For this their individual control blocks are added with perturbation inputs to model the input and output impedances. Fig. 9.3 shows the DAB control block-diagram with internal current

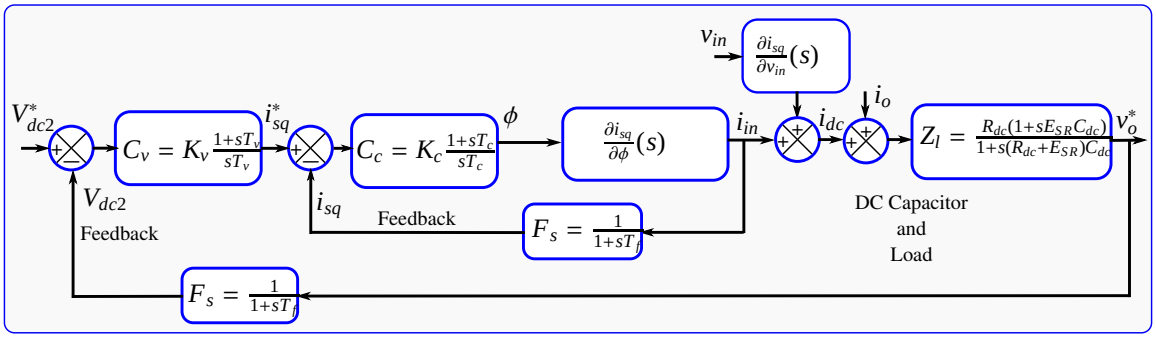


Figure 9.3: Block diagram for impedance transfer function calculation

and outer dc voltage feedback with perturbation signals for impedance modeling.

$$C_c = K_c \frac{1 + sT_c}{sT_c} \tag{9.1}$$

$$C_v = K_v \frac{1 + sT_v}{sT_v} \tag{9.2}$$

$$F_s = \frac{1}{1 + sT_f} \tag{9.3}$$

$$Z_l = \frac{R_{dc}(1 + sE_{SR}C_{dc})}{1 + s(R_{dc} + E_{SR})C_{dc}} \tag{9.4}$$

$$F_b = F_s(C_v Z_l + 1)C_c \frac{\partial i_{sq}}{\partial V_{in}}^{op} \tag{9.5}$$

$$\frac{\partial i_{sq}}{\partial V_{in}}^{op} = \frac{\sin(\phi)}{|Z_{tie}|} \tag{9.6}$$

$$\frac{\partial i_{sq}}{\partial V_{in}} = \frac{\frac{\partial i_{sq}}{\partial V_{in}}^{op}}{1 + F_b} - \frac{\partial i_{sq}}{\partial V_{in}}^{op} \tag{9.7}$$

$$G_v, \frac{\partial V_o}{\partial V_{in}} = Z_l \frac{\frac{\partial i_{sq}}{\partial V_{in}}^{op}}{1 + F_b} \tag{9.8}$$

$$C_c^{loop} = \frac{C_c \frac{\partial i_{sq}}{\partial \phi}}{1 + F_s C_c \frac{\partial i_{sq}}{\partial \phi}} \tag{9.9}$$

$$Z_{in}^{op} = \frac{1}{\frac{\partial i_{sq}}{\partial V_{in}}^{op}} \tag{9.10}$$

$$Z_{in} = \frac{1}{\frac{\partial i_{sq}}{\partial V_{in}}} \tag{9.11}$$

$$Z_o^{op} = Z_l \tag{9.12}$$

$$Z_o = \frac{Z_l}{1 + F_s C_v C_c^{loop} Z_l} \tag{9.13}$$

Eqs. 9.1, 9.2 and 9.3 show the current, voltage loop PI controller and filter transfer-functions respectively. Eq. 9.4 shows the DAB passive load model. Eq. 9.5 shows the feedback loop gain term. Eqs. 9.6 and 9.7 show the open and closed loop terms for $\frac{\partial i_{sq}}{\partial V_{in}}$. Eq. 9.8 shows the input DC noise voltage attenuation term. Eq. 9.9 shows the current closed loop gain. Eqs. 9.10 and 9.11 show the input impedance for open and closed loop. Eqs. 9.12and 9.13 show the output impedance for open and closed loop.

$$Z_{out_rect}(s) = -\left(\frac{\omega_i}{C_{dc}}\right)\left(\frac{s\left(1 + \frac{s}{\omega_i}\right)}{s^3 + \omega_i s^2 + K's + \frac{K'}{T_v}}\right) \tag{9.14}$$

$$K' = \frac{mK_v\omega_i}{C_{dc}} \tag{9.15}$$

Fig. 9.4 shows the AFEC control block-diagram with internal current and outer dc voltage feedback with perturbation signals for impedance modeling developed in [113]. The AFEC expressions for output impedance are given in Eqs. 9.14 and 9.15 derived from the block reduction of AFEC in [113]. Fig. 9.5 shows the bode gain-phase plots for the discussed transfer functions. Input impedance and output impedance improve with closed-loop feedback compared to their open-loop plots. Input impedance has a constant value at low frequency for both open and closed-loop, but there is negative sign attributed to the one with closed-loop. This can be understood by the fact that output of DAB with voltage regulation and resistive load is constant power load. An increase in the input voltage will result in decrease in input current due to control. So the input impedance is negative and constant at low frequency. In open-loop it was primarily the output load resistance referred to primary. The output impedance is zero at low frequency with closed loop while it is constant in open loop. This is understandable that if a small current is injected at output dc bus the voltage feedback tries to maintain the voltage by reducing the DAB output current into the bus. Input impedance in the bode-plot has a zero coinciding with current control bandwidth and output impedance has a double pole coinciding with voltage control bandwidth. For stable integration input impedance of DAB that is negative in sign must be higher than rectifier output impedance at the voltage loop bandwidth. This gives an impression that inner current control helps improve the input impedance from integration point of view. Fig. 9.6 shows the bode gain-phase plots for the TIPS stability functions on the same graph earlier presented in [113]. As shown, the AFEC

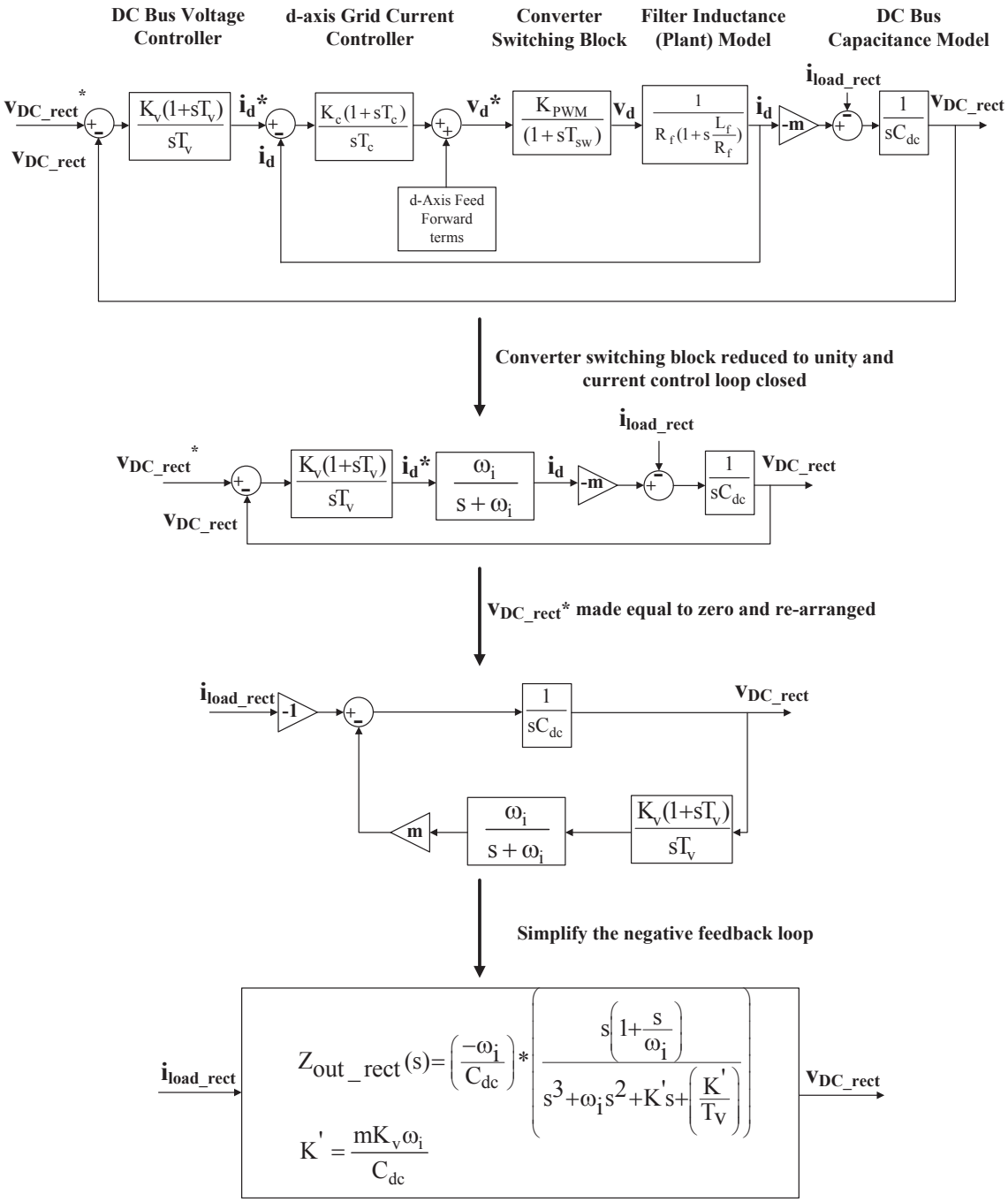


Figure 9.4: AFEC input impedance block reduction

output impedance is zero at low frequency with closed loop. The higher frequency region magnitude depends on combined AFEC and DAB MV dc capacitor size. The AFEC bandwidth and the modulation index affect lower frequency region magnitude. For stable integration input impedance of the DAB that is negative in sign must be higher than the AFEC output impedance in all frequencies. Also in the HV experiments, the DAB was made slower (smaller bandwidth) by trial and error, compared to its standalone controls. This might be due to its output impedance resonant valley point violating the criteria.

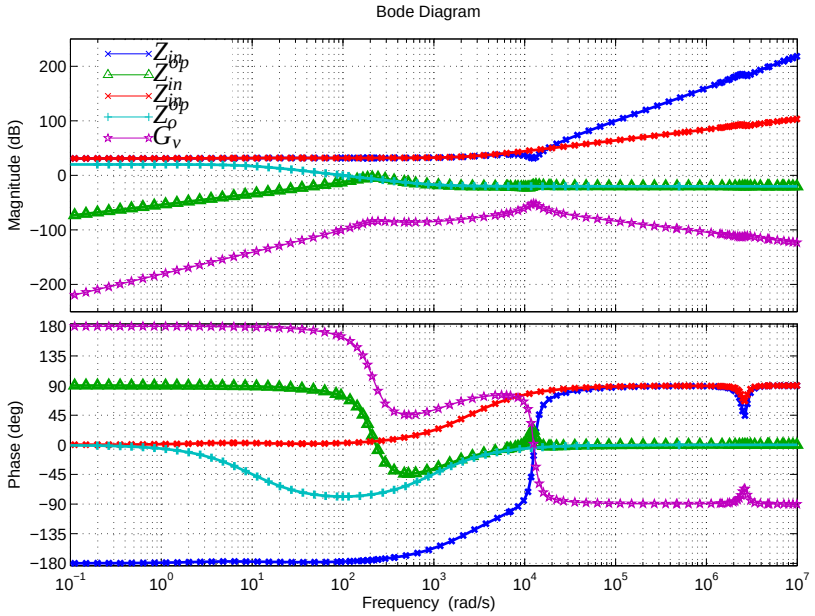


Figure 9.5: Impedance transfer function of the dual active bridge

9.4 TIPS Grounding, CM and EMI considerations

9.4.1 The CM noise Sources of TIPS

Figs. 9.7 and 9.8 show the four converter CM voltages between dc mid-point and respective ac-neutrals and also the spectra of these CM voltages. The DAB converters operating in six-step mode; generate 30 kHz and derivative noise which are triplens of the fundamental switching-frequency. The PWM converters generate switching-frequency noise and their derivative (3 kHz by MV AFEC and 17 kHz by LV inverter). The peak CM voltages and the dominant frequencies are summarized in Table 9.3. The CM

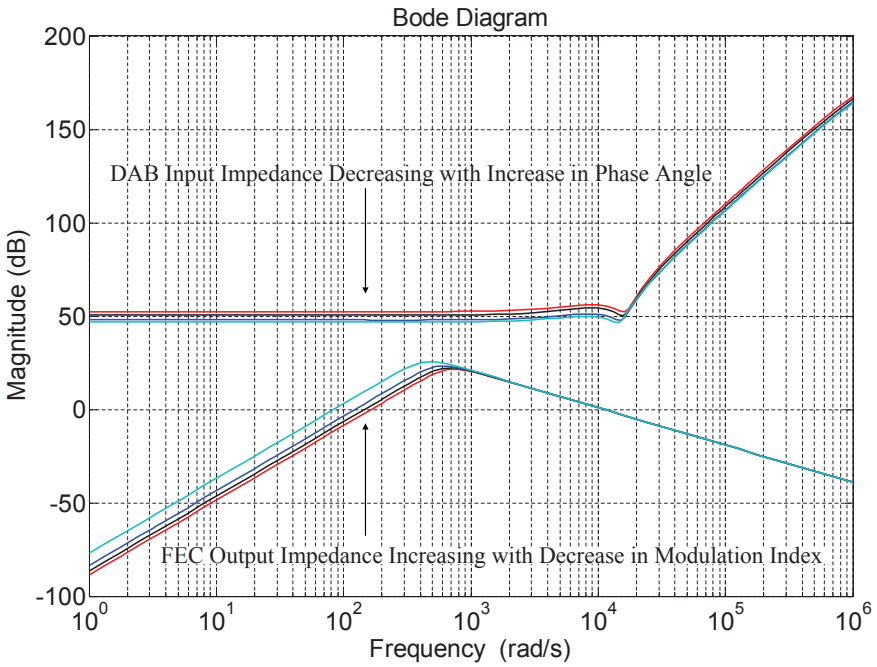


Figure 9.6: DAB input impedance vs AFEC output impedance

voltage level compared to a LV SMPS is very large and therefore the parasitics are very important for grid-tie EMI considerations. Fig. 9.8 shows the effect of dv/dt switching steepness on the CM voltage for the MV side of DAB converter. The dv/dt is approximately emulated with a ramp shape in the simulation and therefore the actual switching shape is between the ideal switching and the ramp switching. The ramp switching lowers the CM voltage magnitude significantly beyond 1MHz. The peak reduction can be seen to be around 25dB for 110kV/µs and 30dB for 30kV/µs near 30MHz. This shows that the dv/dt is more important for the HF CM noise or the EMI and it may generate more of a radiated noise. Therefore an optimization is required between the permissible EMI and the switching loss of the SiC devices.

9.4.2 Importance of Grounding TIPS

This study considers the TIPS system to be connected to a 4-wire MV grid at the input side and the output to be connected to a 3-ph motor load at the output. The MV transformer provides considerable isolation capacitance path for HF CM currents. Due to this the CM voltages are present in the floating output terminals. Also there is CM current flowing in to the grid. These two effects pose safety and operational issues and often lead to failures of the system connected to them. The TIPS output load has its own parasitics C_{pL} to the ground and the TIPS CM generators can result in high floating voltages if the output is left ungrounded. Providing a low-impedance CM path (Y-caps in parallel with the output

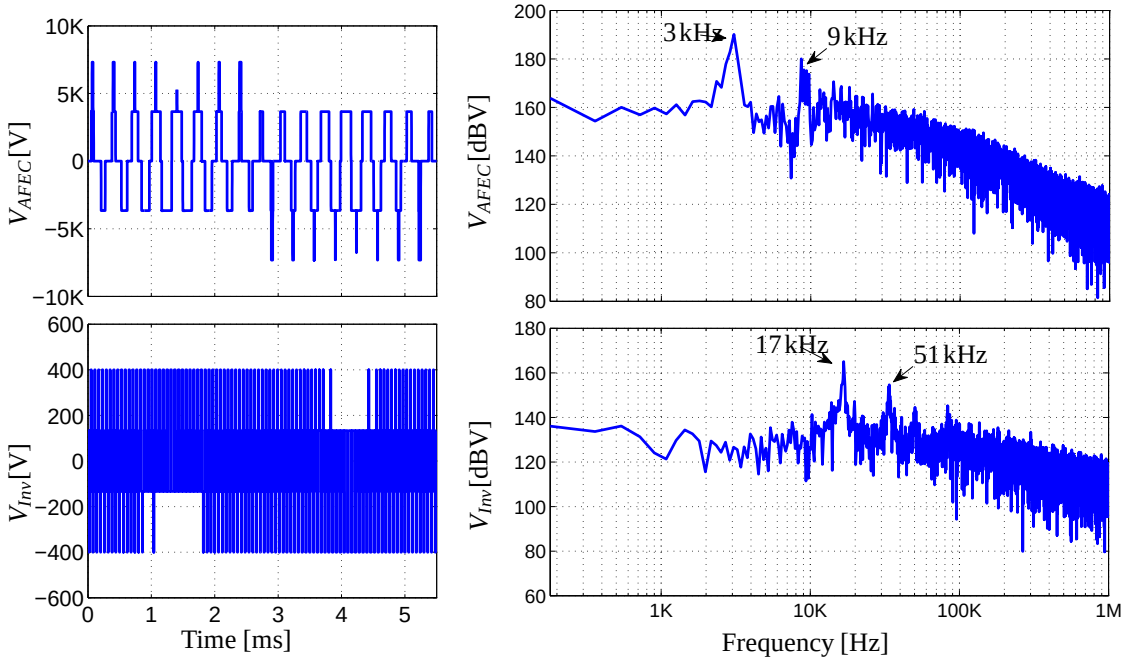


Figure 9.7: CM noise simulation and its spectra of the AFEC and LV inverters

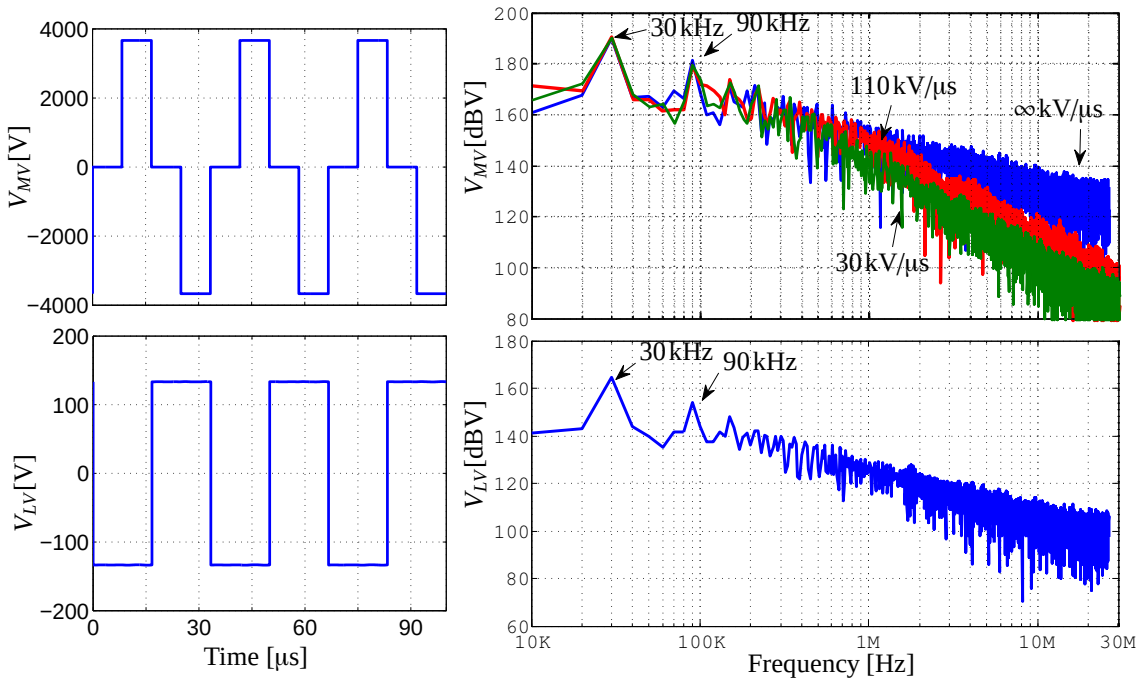


Figure 9.8: CM noise simulation and its spectra of DAB converters

Table 9.3: TIPS common-mode source contributions

Converter	Parameter	Value[Units]
Front-End MV (3L-PWM)	Peak CM voltage	$\frac{22}{3}$ kV Grid
	Dominant frequency	3 kHz
Primary DAB (3L-Six-step)	Peak CM voltage	$\frac{22}{6}$ kV Grid
	Dominant frequency	30 kHz
Secondary DAB (2L-Six-step)	Peak CM voltage	$\frac{800}{6}$ V Grid
	Dominant frequency	30 kHz
LV Inverter (2L-PWM)	Peak CM voltage	$\frac{800}{2}$ V Grid
	Dominant frequency	17 kHz

load, C_{f1} to C_{f3}) to the ground, diverts the CM current which would otherwise flow through the load. This is the standard solution for bearing current mitigation in the inverter fed motor drives [52].

9.4.3 Need of the EMI Filters

As shown in Fig. 9.1 there are CM/EMI paths through GD, VS and CS. The GD is designed such that the coupling parasitics C_{gd} is in the order of 4pF [31]. The VS and CS are selected based on the rating and availability. In the TIPS integration, there has been EMI related false trips in the GD and control units. Since it is difficult to guess the EMI path for these false trips beforehand, the trial and error method of shielding, grounding and CM-EMI choke insertion in certain components near the converters, has been used to solve this and go up in the system voltage in the running system. In the process, ferrite beads and EMI chokes are inserted in the locations shown in Fig. 9.1. The L_{ps1} is the EMI choke and L_{ps2} is the ferrite bead used for the EMI mitigation. The VS and CS sensor cables are shielded and grounded with the lab-ground as the TIPS frame is already grounded. The inserted L_{ps2} blocks EMI from entering the control ground and it is diverted back to source. The power supplies are chosen with lowest coupling capacitance and of high quality. The 15 kV SiC IGBT modules have significant capacitance between the junction to base plate. If the heat-sink is floating, it is seen that above certain voltage and dv/dt, the GD circuit malfunctions and trips. Therefore it is important to tie the heat-sink to a known voltage in the NPC leg. The dc mid-point seems a suitable point as it is symmetric for the devices. But there are locally circulating currents upon this connection and to limit that, a differential EMI choke L_{h1} is used [28].

9.4.4 Need of the Power terminal CM Filters

The CM current propagating through the LV inverter power terminal is decided by the transformer C_{ps} which offers low impedance path for the HF CM noise. This CM current is high in magnitude and can

not be solved alone by the EMI filters. To minimize this, CM filters for the grounding of TIPS system are necessary. The CM choke, which makes the overall power circuit path inductive at the CM frequency, located at the output of the TIPS system can be used to attenuate noise injected. The output grounding still does not affect the TIPS isolation as the two grounds can be separated by a grounding capacitor which allows bypassing of the CM current but does not provide any low frequency or dc current path.

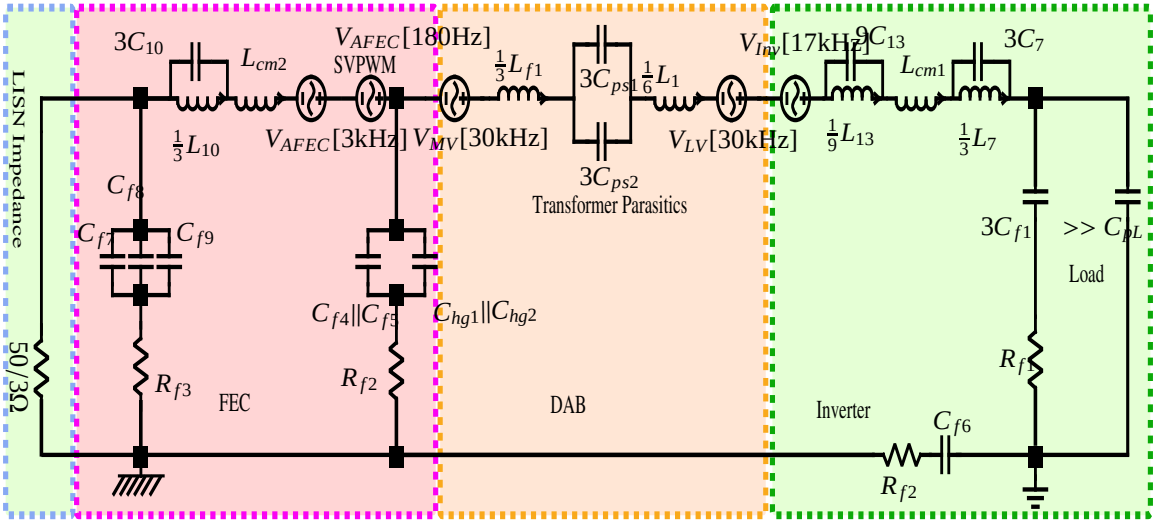


Figure 9.9: CM equivalent circuit of the TIPS considering CM filters

9.5 Specification of Passive CM Filter

The CM voltage sources and path impedances involved need to be recognized for the passive CM filter design. The highest voltage magnitude and the lowest frequency CM source is the AFEC rectifier as shown in Table 9.3. Thus this is the most critical CM source for passive filter design. The second critical CM source is the DAB MV side converter because of the magnitude and dv/dt. Fig. 9.9 shows the power circuit CM equivalent circuit of the complete TIPS systems shown earlier in Fig. 9.1, similar to [111, 52]. Other CM paths are negligible and ignored for the design of the power circuit CM chokes. Each TIPS component is represented by its single-line equivalent CM voltage and CM impedance. The transformer turn-ratio does not scale-down the CM impedances or the CM voltages. The passive CM filter consists of the grounding capacitances (C_{f1} to C_{f9}), damping resistors (R_{f1} to R_{f4}) and the CM chokes (L_{cm1} and L_{cm2}). If the load has very small parasitics (C_{pL}), then such complex filter and grounding solution may not be required. This study assumes that there is a highly parasitic ground-coupling load (motor), connected to the TIPS. Thus the outer CM loop always exists.

9.5.1 Input CM Filter

For a single CM choke solution, the CM path contains 3kHz, 30kHz and 51kHz CM sources. A single CM choke can be used at the output of LV inverters to block the CM voltage and bypass an acceptable limited current to the ground. In that case, part of lower frequency CM noise (3kHz) drops at the transformer C_{ps}, though 30kHz noise drops predominantly across CM inductor. Since the 3kHz CM current is low frequency for the 10kHz MV-HF transformer, it cannot be allowed to conduct through as it affects the DAB operation. The transformer can be designed such as to minimize the C_{ps} to attenuate the propagating CM current. But this dilutes the size advantage of the TIPS system over a 60Hz transformer. Therefore this 3kHz AFEC noise needs to be locally bypassed using an input CM choke and grounding the MV dc bus with C_{f4}, C_{f5} and R_{f2}. The heat-sink to ground porcelain standoff capacitances (C_{hg1} to C_{hg2}) are also considered, but C_{f4} to C_{f5} are chosen high enough to bypass them. The grid can be connected to this ground using Y-caps C_{f7} to C_{f9} and damping resistance R_{f3} as shown in Fig. 9.1. A L-C-L filter design for TIPS AFEC rated operation has been presented in [114]. So the same capacitor bank design can be utilized as C_{f7} to C_{f9} as they give a higher value which is better for CM noise bypassing. The value used for that design are 0.42μF. The CM current is limited primarily by an input CM choke L_{cm2}. To meet the common EMI standard, the lower EMI limit 150kHz drop must be below 66dBμV average (FCC standard) across LISN 50Ω stabilized impedance per phase as shown in Fig 9.9. Equation (1) gives the 150kHz CM current permissible with L-C-L Y-caps for TIPS. This approximately results in maximum i_{cm}(150kHz) as 2.5mA for impedance $Z_{inG}(f)$ offered by the above L-C-L caps. With dominantly inductive CM filter the allowed AFEC side CM current at 3kHz is 125mA.

$$i_{cm}^{max}(f) = \frac{2 * 10^{-3}}{50/3 \| Z_{inG}(f)} \tag{9.16}$$

9.5.2 Output CM Filter

The DAB MV CM current cannot be bypassed locally using MV-HF transformer neutral grounding since it generates triplen currents undesired for DAB operation and control. So the 30kHz CM current takes a longer loop and is limited by a CM choke L_{cm1} either at MV dc input to DAB or at the output inverter stage. The inductance value remains same but the winding, voltage and current ratings are decided by the differential ratings of the two locations. For first location on MV dc bus, both differential and CM voltage ratings are high but the current-rating is low and also only two windings are needed. The second location is selected for this chapter so that differential isolation voltage rating between two phases are small though it carries higher current. The major impedance is formed by transformer C_{ps} and L_{cm1}. The overall CM path is made inductive at the CM frequency (30kHz). The TIPS output is grounded using Y-capacitors C_{f1}, C_{f2}, C_{f3} and damping resistance R_{f1}. The value of Y-capacitors is selected such that they do not draw significant differential-current from the converter but their impedance is much smaller

at the 30kHz. They bypass most of the CM current which would otherwise flow through the load.

$$i_{cm}(f) = \frac{V_{cm}(f)}{Z_{eff}(f)} \tag{9.17}$$

$$R_{fi} = 0.5\sqrt{\frac{L_i}{C_i}} \tag{9.18}$$

Eqs. (9.16)-(9.18) are used for the CM filter selection [111, 52]. The CM inductors are selected such

Table 9.4: CM choke specifications

Input Choke L_{cm2}		**Output Choke** L_{cm1}	
Parameters	**Value[Units]**	**Parameters**	**Value[Units]**
L_{self}	200mH	L_{self}	50mH
L_{leak}	$< 400\mu$H	L_{leak}	$< 100\mu$H
L_{mut}	200mH	L_{mut}	50mH
V_{diff}	22kV	V_{diff}	800V
V_{core}	22kV	V_{core}	22kV
i_{inR}	4A	i_{outR}	200A
f	3kHz	f	30kHz
V_{cm}	22/3kV	V_{cm}	22/6kV

that the effective loop impedance (Z_{eff}) limits 30kHz internally circulating CM current to 100mA peak and the 3kHz internally circulating CM current to 200mA peak spike, using (1, 2) as discussed earlier. Thus the design for the dominant CM noise also works for the 150kHz FCC standard. The individual damping resistor (R_{fi}) is selected using (3) for given loop impedances. The input and output grounds are connected with a capacitor (C_{f6}) and damping resistor (R_{f4}), which offers sufficiently low impedance for the CM current. The designed CM filter parameters are summarized in Table 9.4. As discussed, the output choke can be specified for DAB input dc location also. The advantages for that location are two windings and smaller currents but the inter-winding isolation and isolation to the core, both need to be 22kV rated. The inverter side location is chosen for study to avoid higher isolation requirements.

9.6 Simulation Results: HV and LV CM Choke Specification

The TIPS shown in Fig. 9.1, is simulated using the measured values of the designed components and associated parasitics as shown in Table 9.2. Only the main parasitics are considered. The TIPS transfers 100kW in forward power-flow direction. The AFEC regulates 22kV dc and the DAB regulates 800V

dc and the inverter drives a resistive load. The output inductive filters are part of TIPS. The voltage & current of the CM chokes and the damping resistor currents are plotted. The simulation is run for 4-5 cycles of 60Hz in 1μs step-time considering the 10kHz DAB operation. Fig. 9.10 and Fig. 9.11 show

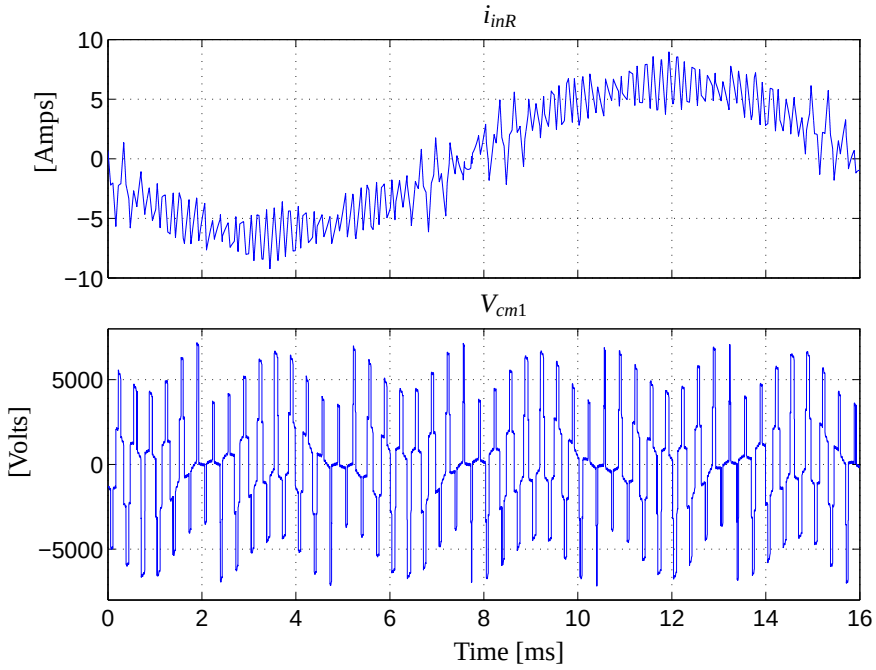


Figure 9.10: Common Mode (HV) Inductor-I 100 kW steady state simulation with parasitics

Table 9.5: Common Mode (HV) Inductor-I Specifications

Parameter	**Value**
Winding Voltage	2.5kV rms, 7.5kV peak
Winding Current	5A rms, 9A peak
Inductance	200mH
No of windings	3, wound on common core (All +ve)
Frequency	Blocks 3kHz voltage noise

the current and voltage simulation of the complete TIPS system for the common mode chokes. The HV side choke is connected at input and the LV choke at the output inverter. This simulation is also used to specify the MV-HF transformer C_{ps} value, it should be smaller than 2000pF from device current perspective at rated condition. Any capacitance in this range is suitable with below CM inductors. Table 9.5

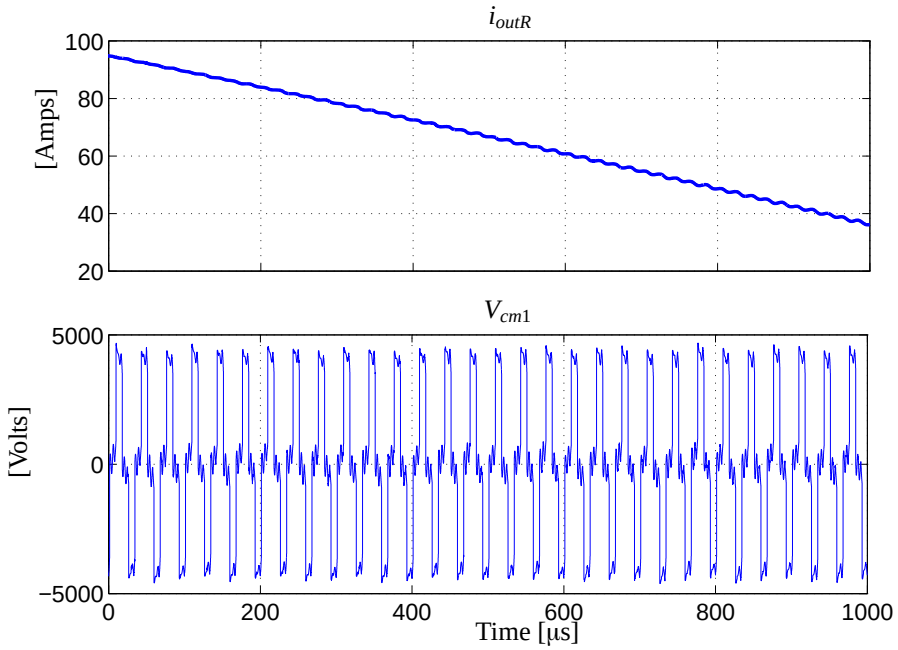


Figure 9.11: Common Mode (LV) Inductor-II 100 kW steady state simulation with parasitics

Table 9.6: Common Mode (LV) Inductor-II Specifications

Parameter	**Value**
Winding Voltage	2.6kV rms, 5kV peak
Winding Current	117A rms, 165A peak
Inductance	50mH
No of windings	3, wound on common core (All +ve)
Frequency	Blocks 30kHz voltage noise

and Table 9.6 present the choke specification for HV and LV side respectively from time-domain simulation. Fig. 9.12 and 9.13 show the rated condition frequency spectra of phase currents and blocked voltages of the input and output CM chokes respectively. It can be seen that they block the desired CM voltages and conduct only the differential fundamental currents. There is only CM voltage drop across CM chokes and they do not cause any line-frequency voltage drop since the leakage inductance is negligible. The CM current is within the desired limit. The input choke blocks mainly 3 kHz CM voltage and the output choke blocks the 30 kHz CM voltage. Fig. 9.15 shows the built TIPS CM chokes based on the specification generated in the simulation study. The parasitics associated with these chokes must be small for them to be effective. But the CM choke size and cost constraints place a lower limit for the parasitics and the final design needs optimization. Fig. 9.16 shows the impedance sweep of the chokes on one CM winding with other two windings open. It can be noticed that the resonance frequency is in

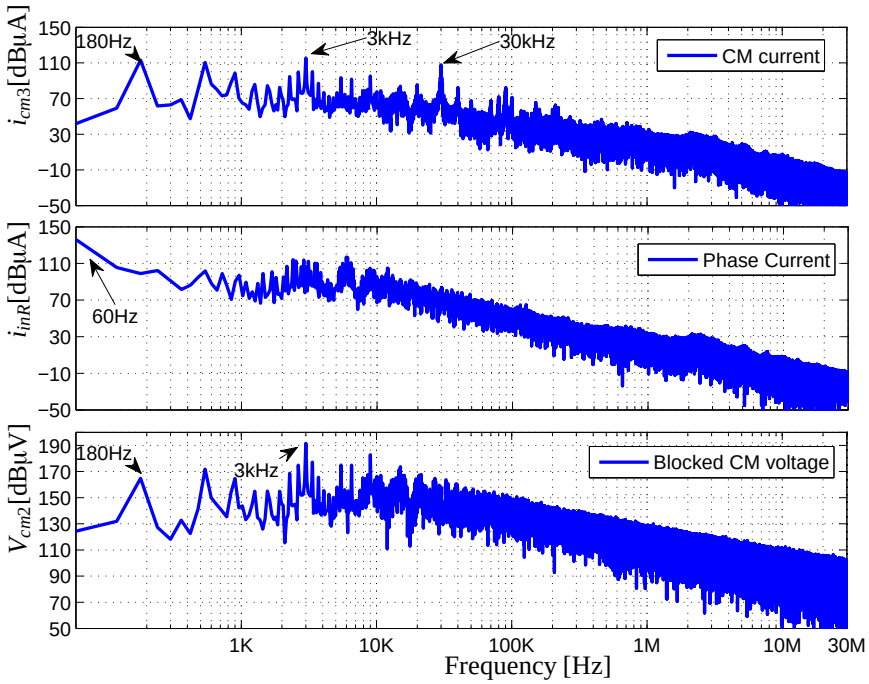


Figure 9.12: Input CM choke simulation spectra: current and blocked voltage

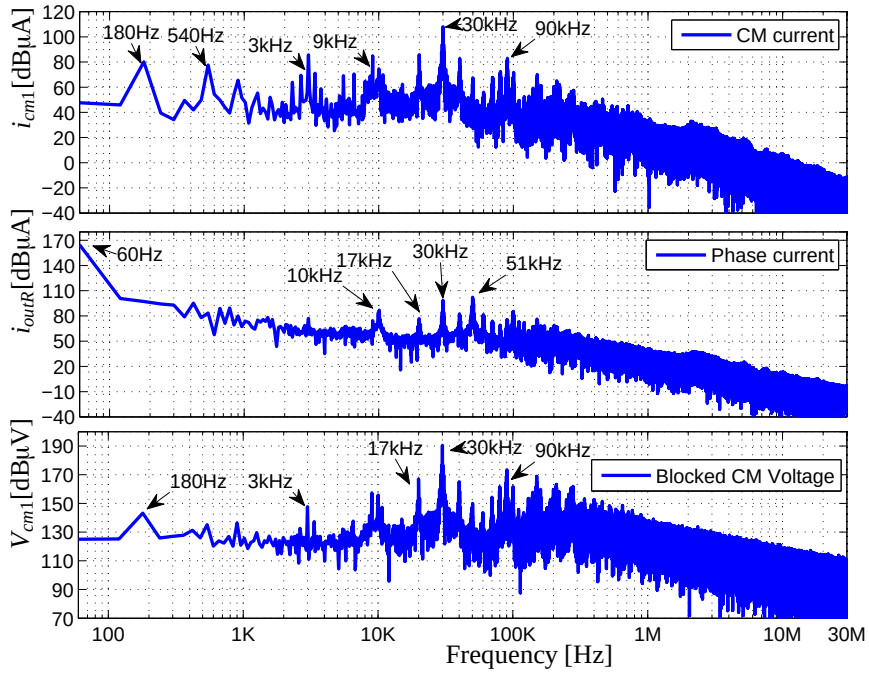
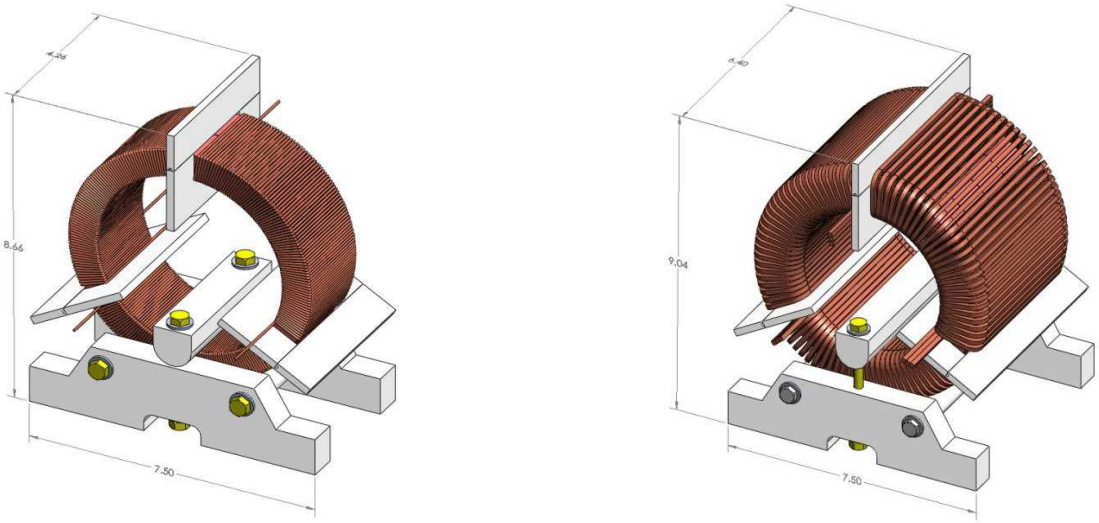
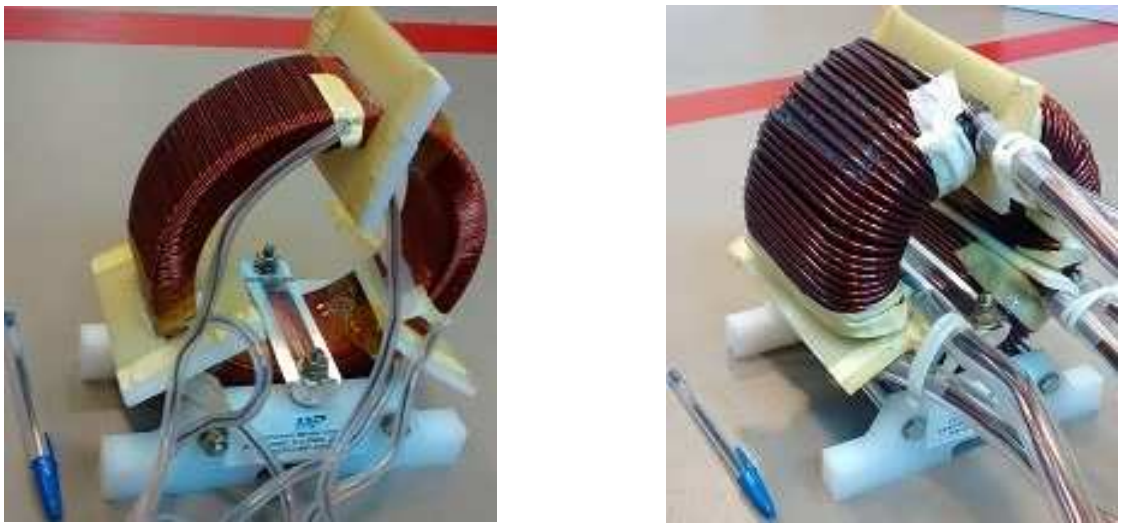


Figure 9.13: Output CM choke simulation spectra: current and blocked voltage



(a) Input choke L_{cm2} **(b)** Output choke L_{cm1}

Figure 9.14: CAD view of the TIPS CM chokes



(a) Input choke L_{cm2} **(b)** Output choke L_{cm1}

Figure 9.15: Photograph of the Developed TIPS CM chokes

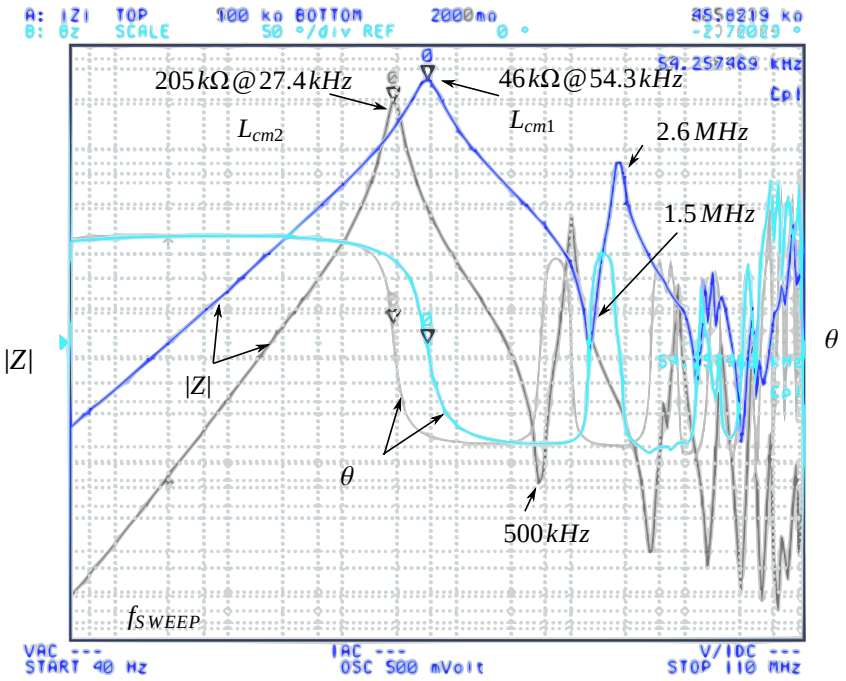


Figure 9.16: Frequency sweep impedance measurement of the CM chokes

the order of the CM frequency and it turns capacitive thereafter. Thus additional EMI filters might be required for higher frequencies and this CM choke is good for the low frequency CM noise mitigation.

9.7 High Voltage TIPS Setup

Fig. 9.17 shows the lab demo plan for the MV TIPS. As the 4.16kV MV grid is generated with a variac and a isolated step-up 75kVA $\Delta - \Delta$ transformer in the lab, there is no need to employ all the CM filter components. Only half of the AFEC inductors - 140mH as simple L filter are used for up to 8kV. As these IGBTs are research devices, the grid and load are left ungrounded and only the MV dc bus grounding is implemented with C_{f4}, C_{f5} and R_{f2}. Fig. 9.18 shows the AFEC and DAB setup for the 100kW TIPS. The AFEC and DAB are 3-ph converters and consist of 3 modular NPC poles each, built with 15kV SiC IGBTs and 20kV SiC JBS clamping diodes. These poles are isolated from the frame using porcelain standoffs. Each pole has local dc capacitor bank built with series connected 3.5kV film capacitors. The AFEC and DAB differential inductors are designed in the previous works [29, 32, 30, 103]. The controller generated gate signals are optically routed to the GDs. The sensor cables are shielded and referenced at the control ground to avoid any noise pick-up. Also all the control power supplies have a CM choke at their ac chords. This setup has been integrated up to 8kV dc bus for 9.6kW power transfer.

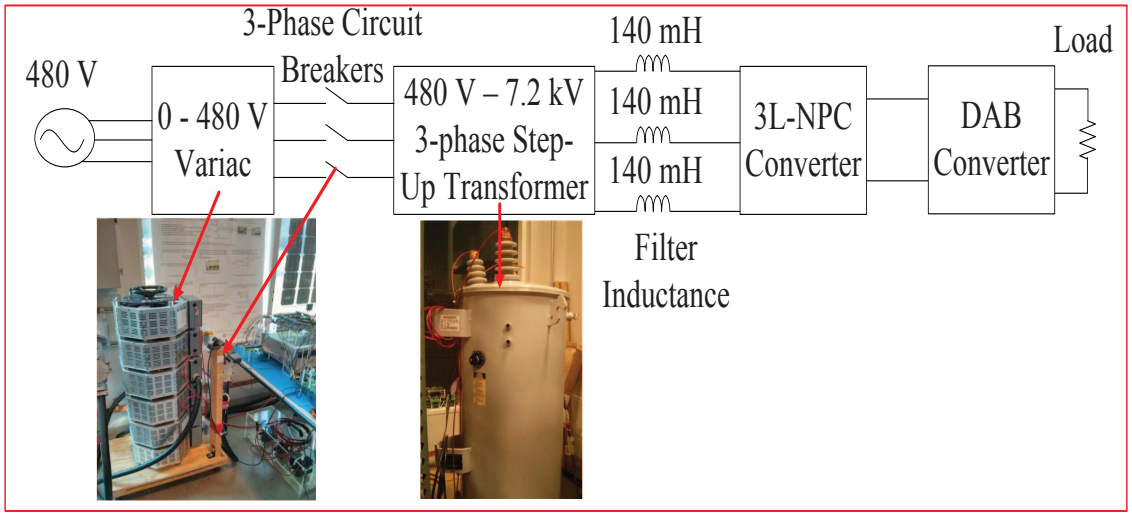


Figure 9.17: TIPS lab demo test diagram

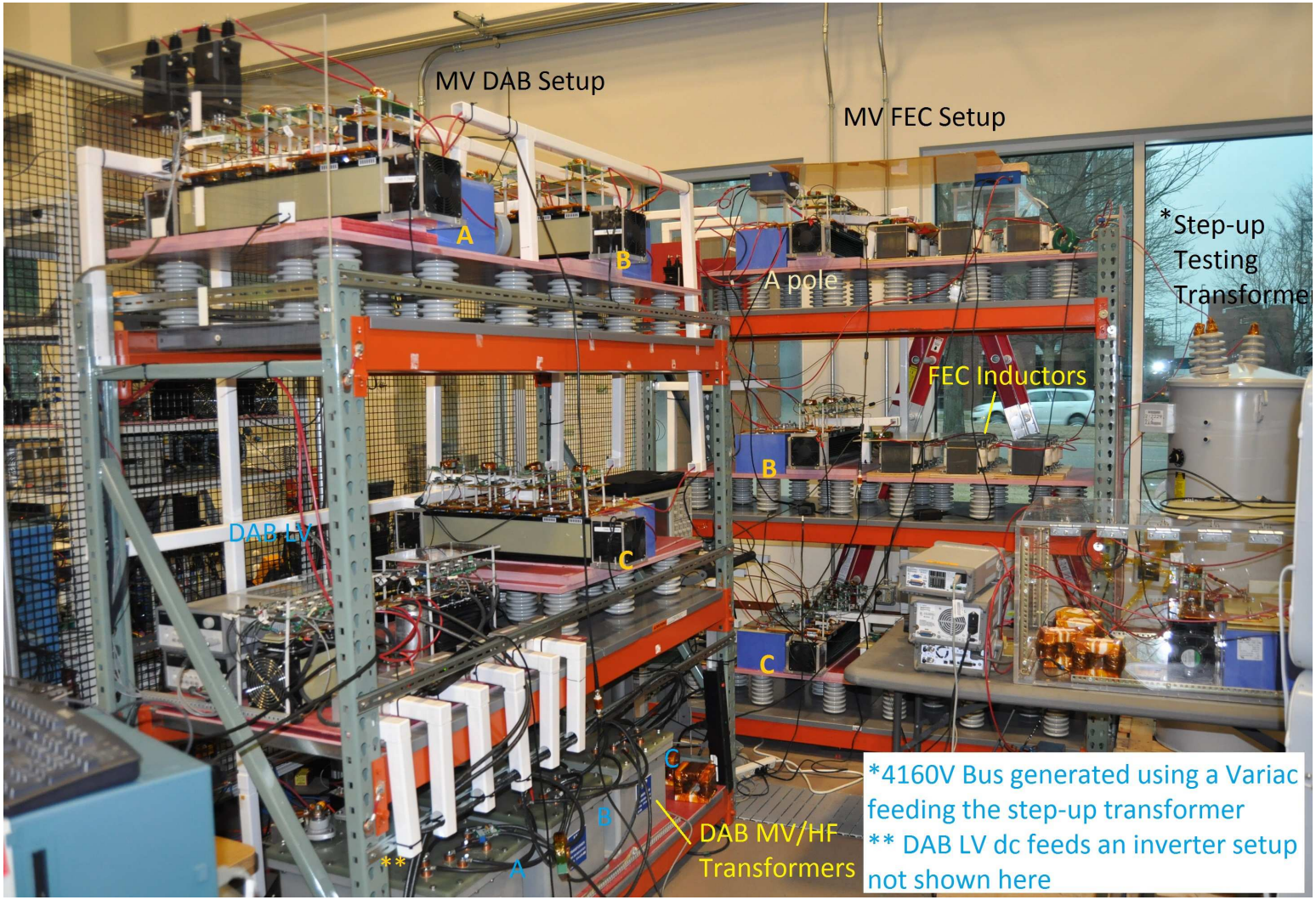
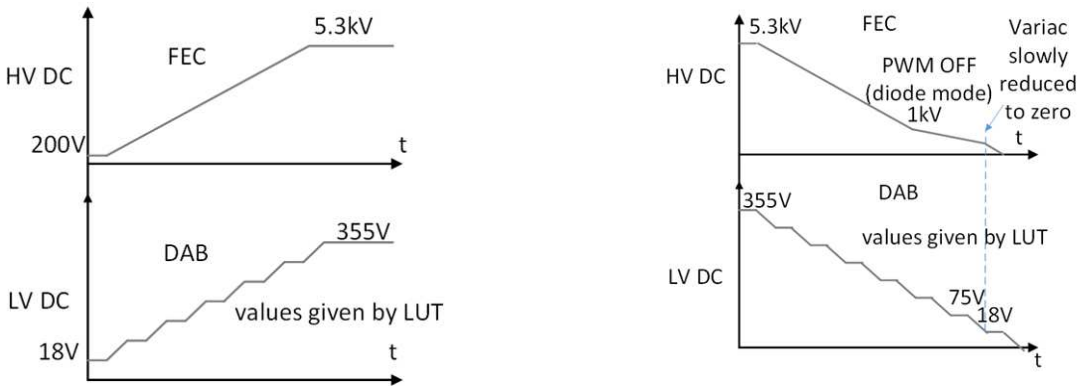


Figure 9.18: 100 kW TIPS system setup

9.8 TIPS Integration Test Procedure

A TIPS start up and shutdown scheme is developed for testing TIPS in integration mode in the lab. The testing procedure for shut-down is as follows as shown in Fig. 9.19(a). First the MV dc bus is pre-charged through AFEC with in diode mode (PWM off) using the variac to 200V dc, The DAB control operates in closed loop with output voltage set to 18V. Then the AFEC closed loop control PWM are turned on with a ramp increase in reference dc link voltage of the AFEC. Then the the fault communication between the AFEC, the DAB input MV converter and the DAB output LV converter P/D boards are turned on. This is because a fault loop is created between the three P/D boards and with AFEC PWM off, it would trip all boards in cascaded effect. The variac voltage setting is adjusted such that the input line current should not exceed 6A peak or in other words the AFEC modulation index should remain is a range decided by trial error with all system settings in place. Based on MV dc link voltage the DAB ouput voltage is increased in steps with a look-up table (LUT) based approach constructed based on trial and error such that DAB voltage ratio is maintained about 60 V per 1 kV-dc. This maintains full ZVS turn-on and the dv/dt slopes are in EMI limit as explained in earlier chapter. The testing procedure



(a) Start-up **(b)** Shut-down

Figure 9.19: TIPS Testing Procedure

for shut-down is as follows as shown in Fig. 9.19(b). The AFEC reduces the reference for MV dc link voltage in a slow ramp. The DAB always flows its reference LUT and automatically reduces its LV dc voltage linearly in discrete steps. After reaching about 1kV, the AFEC PWM are turned off and it goes into diode rectifier mode. The DAB continues to reduce its LV dc following the LUT till 75V. Finally DAB with a manual switch reduces its LV dc discarding the LUT after-wards and reduces to 18V. The AFEC variac is reduced to zero setting.

9.9 High Voltage Experimental Results

Before AFEC and DAB are integrated, they have been individually tested up to 6kV. Fig. 9.20 shows the experimental results for AFEC at 6kV dc voltage in controlled rectifier mode supplying a resistor load of 7kW. The AFEC is switched at 5kHz for the demo due to control bandwidth requirements [29]. The frequency spectra is also shown. It can be seen that the AFEC currents have considerable 5kHz switching differential noise. The differential noise is real and attributed to the AFEC coupling inductor and its parasitics interacting with the high dv/dt. There are even harmonics also explained previously in [29]. Fig. 9.21 shows the experimental results for DAB switching of the MV NPC pole considering a

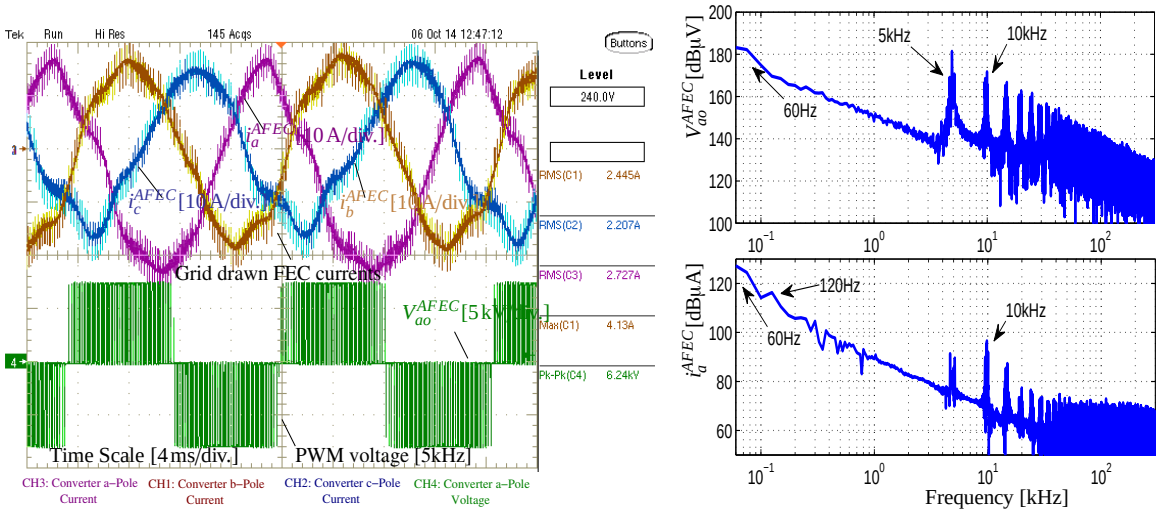


Figure 9.20: Standalone AFEC converter 6kV result and its spectra

resistive load as well as the actual DAB load with ZVS operation for same power level. It shows the effect of soft-switching on the dv/dt slope of V_{ao}. The lagging current causes free-wheeling action of the anti-parallel diodes which in turn applies slower dv/dt due to the natural commutation. The hard switching dv/dt is much higher which depends on the gate resistance below punch-through level. It generates spike and ringing in the device currents. It also narrows down the ZVS range. The control design is not affected by the parasitics as the resonant frequencies are much higher than the control bandwidth. The spectra for both conditions are plotted as shown. It can be seen that ZVS operation minimizes the EMI noise as compared to hard-switching in 1MHz to 10MHz range. Fig. 9.22 and Fig. 9.23 show the TIPS DAB and LV inverter integration results at 4.2kV dc voltage and 2.3kW power [131]. This has been completed on setup with 15kV/20A, 2μm buffer SiC IGBT devices. The AFEC results are captured in separate scope presented in [131]. The voltage in this setup could not be increased further due to

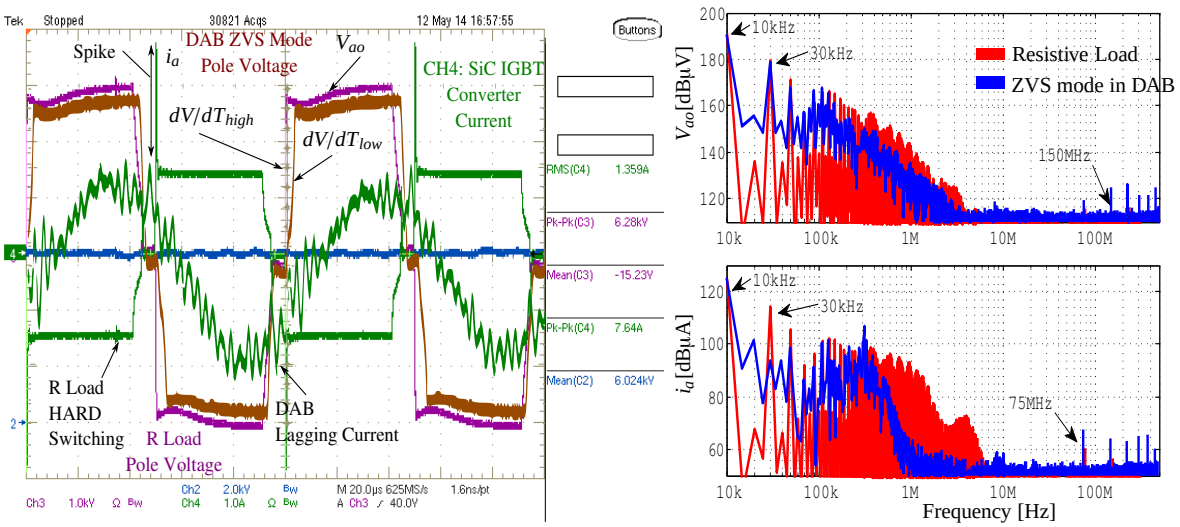


Figure 9.21: Standalone DAB NPC pole 6 kV results showing ZVS effect on dv/dt and spectra

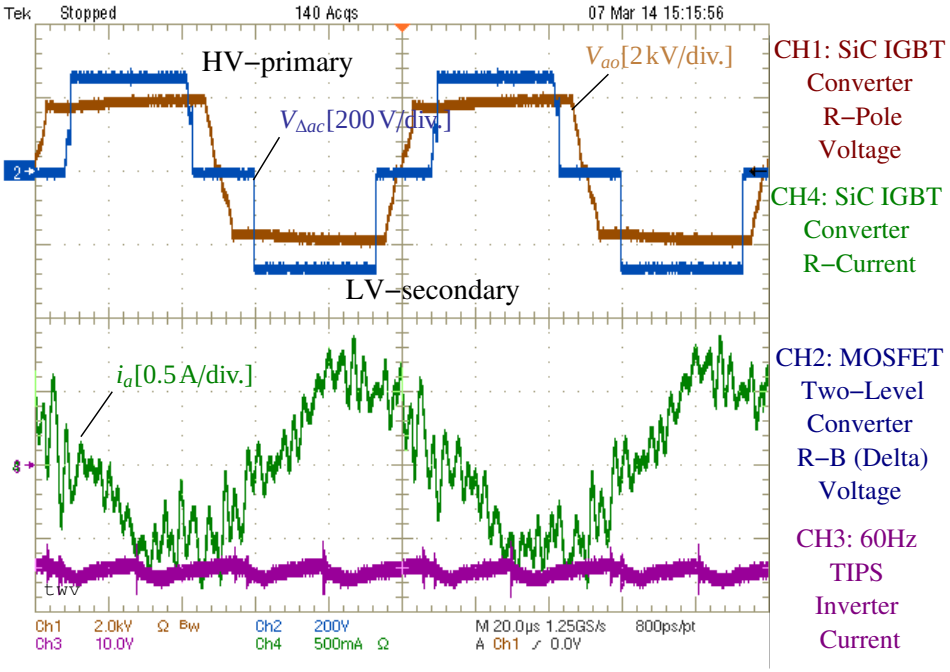


Figure 9.22: Integration mode Y:Y/Δ DAB converter results at 4.2 kV-260 V dc, 2.3 kW power

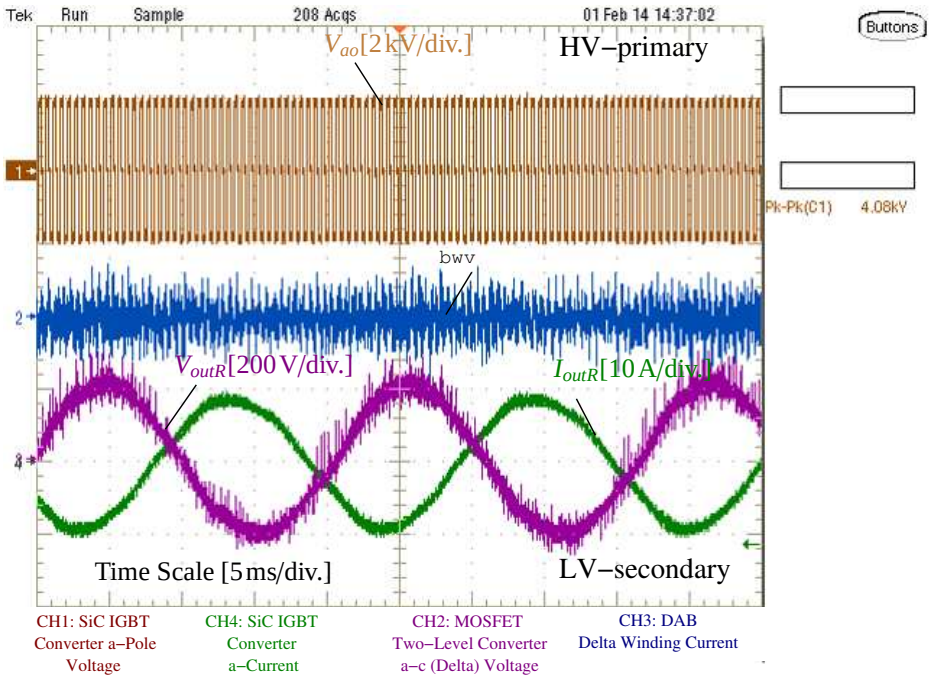


Figure 9.23: Integration mode LV three-phase output inverter results at 260 V dc, 2.3 kW power

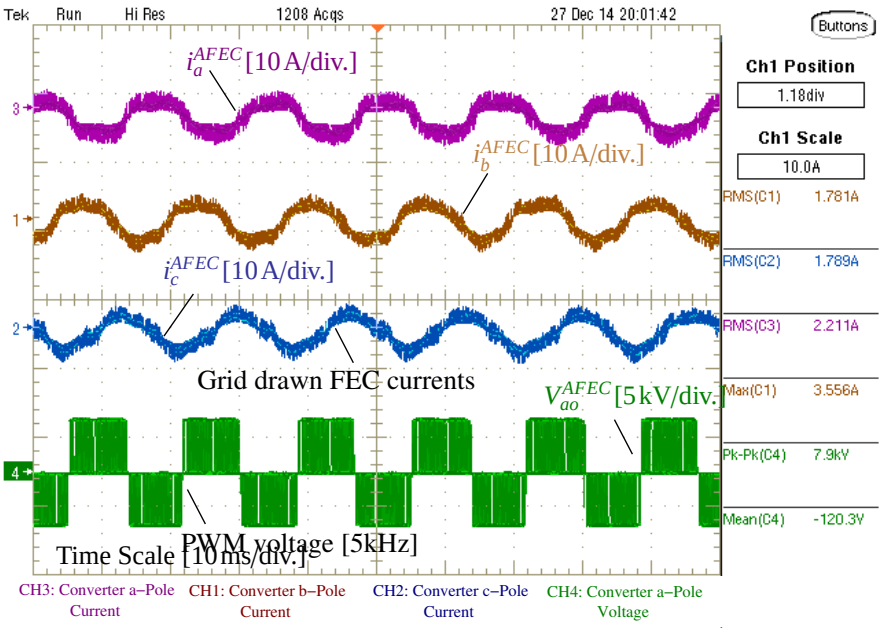


Figure 9.24: Integration mode AFEC converter results at 8 kV, 9.6 kW, 5 kHz

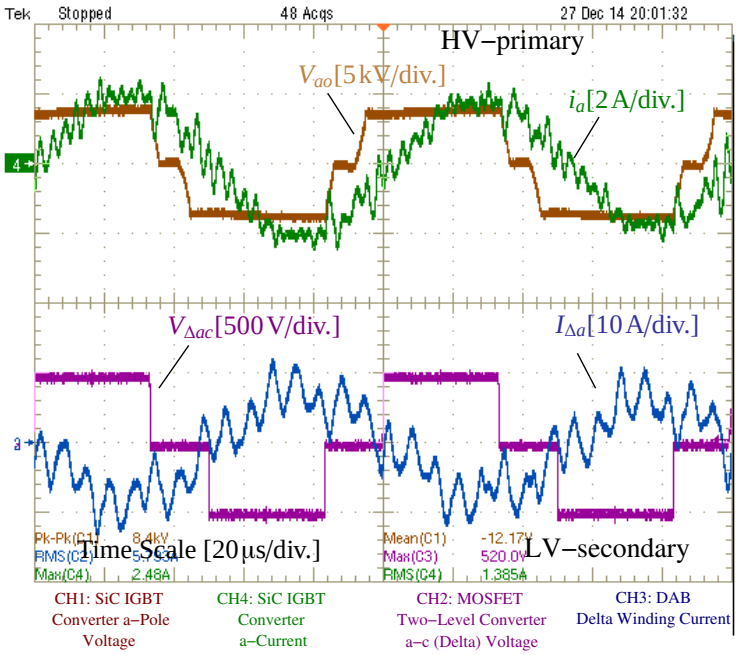


Figure 9.25: Integration mode Y:Y/Δ DAB converter results at 8 kV-480 V dc, 9.6 kW

EMI tripping problem coming with the switching of these devices. After new setups are developed with 40 A/ 5 µm IGBTs and grounding & shielding on control wiring are followed, the integration voltage is increased further. Fig. 9.24 and Fig. 9.25 show the TIPS integration results for AFEC and DAB respectively at 8 kV dc voltage and 4.16 kV MV grid [45, 103]. Compared to previous AFEC result, grid drawn currents for the higher power are less harmonic. There is no significant CM current in absence of the grounding. For the grid side grounding, the CM choke must be put in as the AFEC generates high CM voltage with high dv/dt due to hard-switching and the $\Delta - \Delta$ transformer can not block these HF CM voltage. Therefore up to the 8 kV demo tests, grid side is not grounded. As shown in Fig. 9.25 result, the DAB MV pole dv/dt is ZVS mode dependent. On losing the ZVS, it generates high dv/dt. The HF current has considerable differential noise due to the transformer inter-turn C_p and the mutual C_{ps}. The primary current has 350 kHz ringing and the secondary has 150 kHz dominant ringing. In presence of the output grounding, it is expected to conduct 30 kHz CM current as well but its magnitude will be limited by the output CM choke. A dc resistor load is used for TIPS integration, therefore the output grounding is not implemented for the MV tests.

9.10 Low Voltage Prototype Experimental Results

All the grounding and common mode components planned for the MV TIPS for grounding have been scaled down to LV TIPS rating since the CM filter solution is first implemented in the LV prototype. All the solutions have not been completely implemented on the MV TIPS setup. Table 9.7 shows the parameters of the scaled LV TIPS prototype which is built with rating of 208 V 3-ph to 208 V 3-ph 60Hz and 4 kW power. The MV TIPS system parasitics and important parameters are scaled down by per-unit method. The scaled-down parasitics turn out to be very high compared to the actual parasitics of the LV TIPS system. Therefore equivalent external capacitors are inserted in the DAB MF transformer similar to its equivalent circuit to emulate the real MV conditions [49]. Fig. 9.26 shows the photograph of the parasitic emulated converter setups and filtering components. The rated dc voltages of the DAB are 400 V, operating at 10 kHz frequency. The LV AFEC operates at 5 kHz and the output inverter at 20 kHz PWM switching. The LV experimental testing of the grounding has been done at 150V, 500W

Table 9.7: Selected LV TIPS CM components based on scaled-down MV parameters

Parameters	Value[Units]	Parameters	Value[Units]
L_{cm1}	4 mH	L_{cm2}	1 mH
L_1 to L_6	600 µH	C_{ps1} to C_{ps3}	18 nF
L_{f1} to L_{f3}	8 µH	L_7 to L_9	10 mH
L_{10} to L_{12}	10 mH	C_p	4.7 nF
C_{f4} to C_{f5}	2 µF	C_{f6}	2 µF
C_{f7} to C_{f9}	2 µF	C_{f1} to C_{f3}	20 µF
R_{f1}	5Ω	R_{f2}	5Ω
R_{f3}	10Ω	R_{f4}	5Ω

power rating only, to verify the grounding concept. Three single-phase transformers with 1:1 turn-ratio, have been used to emulate the $\Delta - \Delta$ transformer used in the MV-TIPS system. Fig. 9.27 shows the LV setup test arrangement highlighting the grounding reactor, CM choke, Y-cap banks, AFEC with its controls and the LV $\Delta - \Delta$ transformers. This transformer floats the AFEC converter with respect to the lab ground. Various options of grounding are tested in this setup. The AFEC is operated in closed loop generating 150V dc on output. The AFEC is connected to the ac grid here with a variac for smooth start-up. A low voltage variac is connected to 208V line to line three-phase grid. In MV-TIPS experiment, a 460V Variac is used with another 460V grid available in the lab. Fig. 9.28 shows the AFEC side input CM choke results for grounded TIPS prototype at 150 V dc and 500 W. The component variables are labeled as shown in Fig. 9.1. As expected, when the dc is grounded with the grid side ac neutral, all the

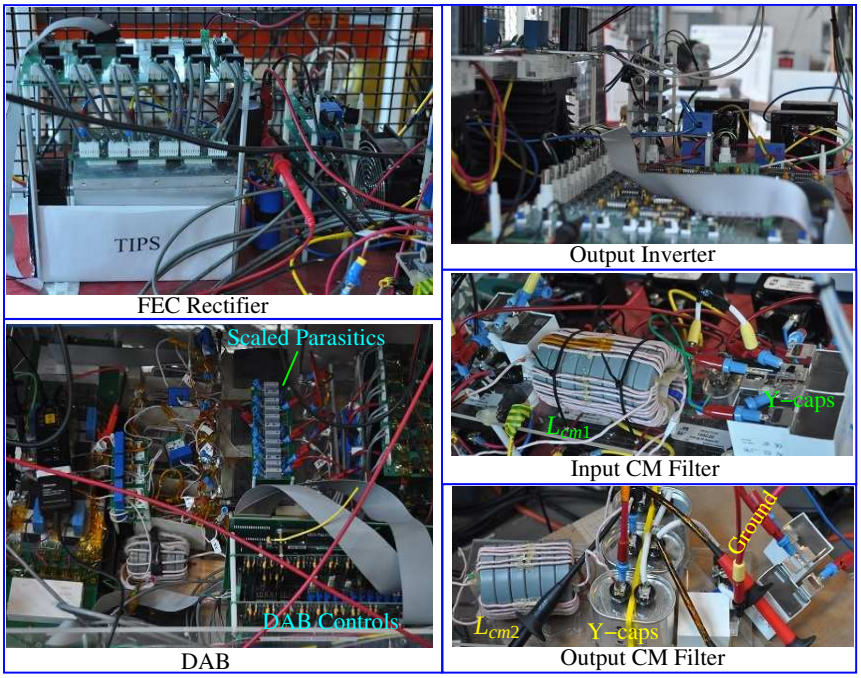


Figure 9.26: Photograph of the LV TIPS setup for CM filtering and grounding

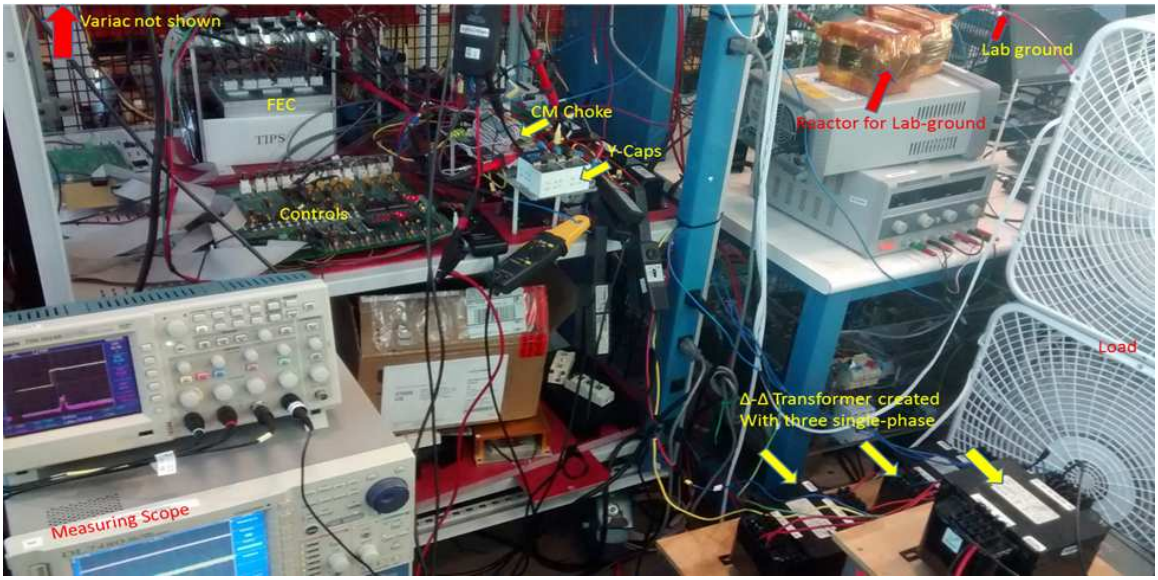


Figure 9.27: Photograph of the LV TIPS setup for CM filtering and grounding

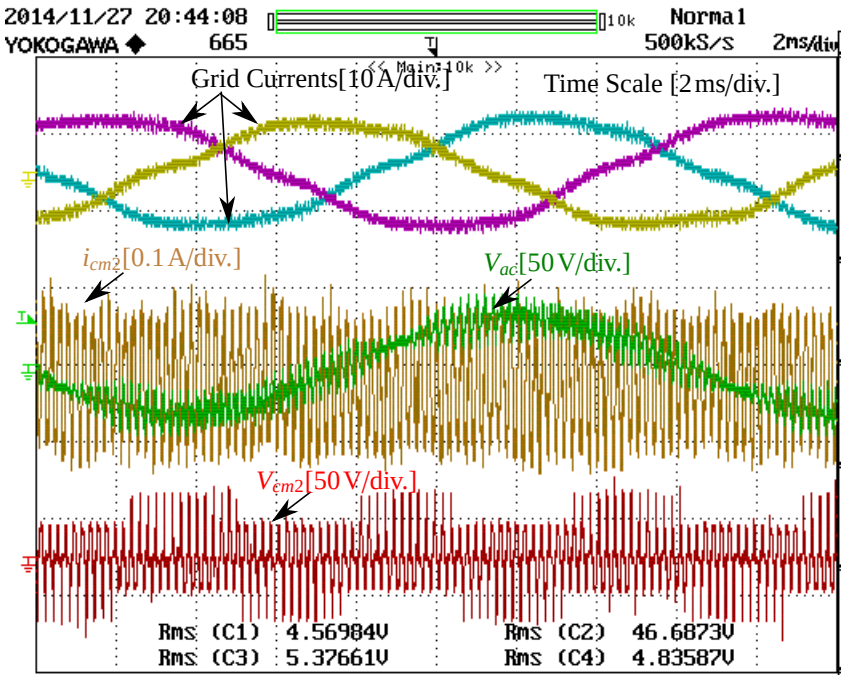


Figure 9.28: AFEC side integration results with CM choke at 150 V dc output

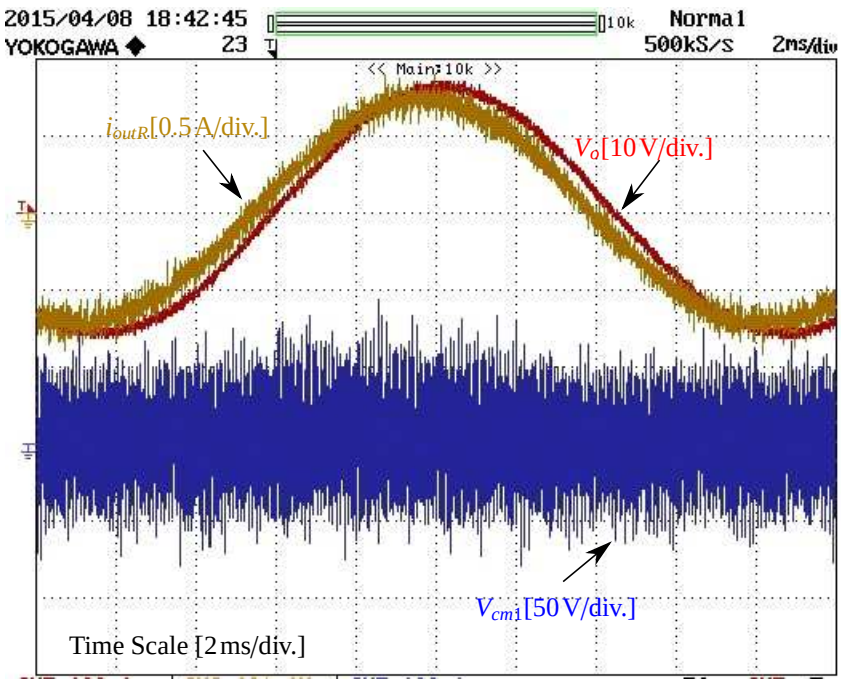


Figure 9.29: Inverter side integration results with CM choke at 27 V dc

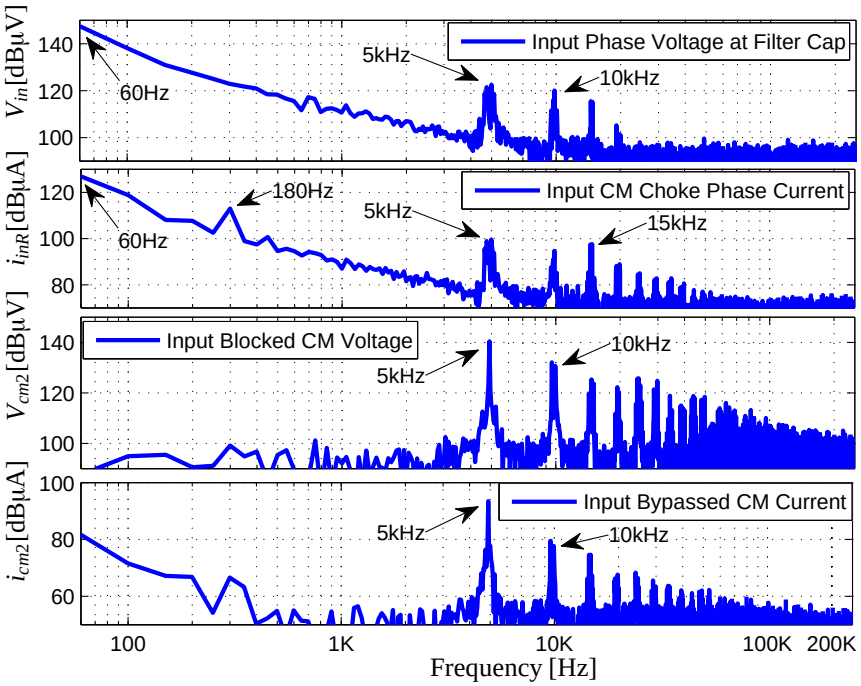


Figure 9.30: Spectra of AFEC side CM choke at 150 V dc

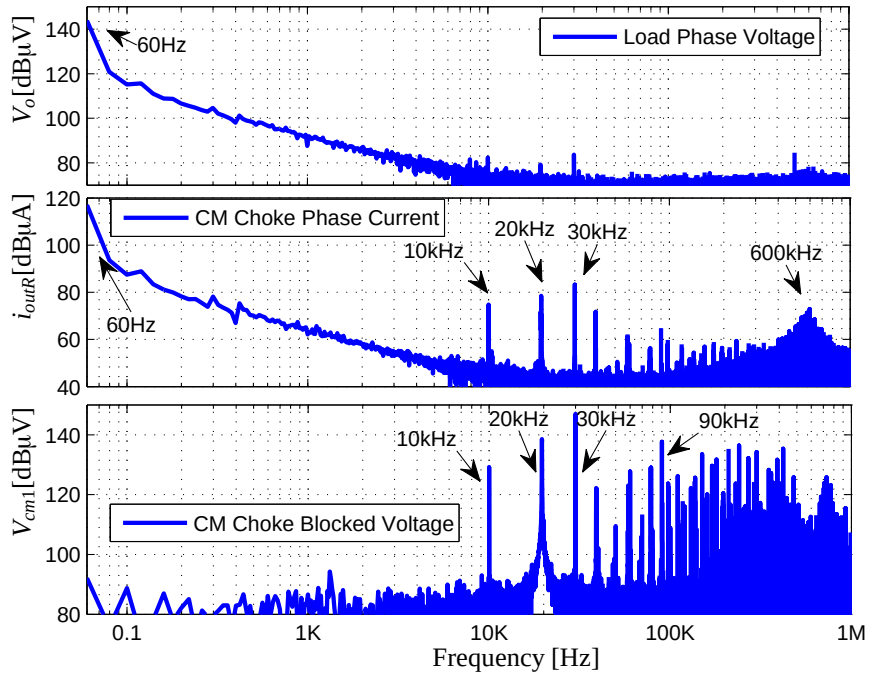


Figure 9.31: Spectra of inverter side CM choke at 27 V dc

local AFEC CM voltage is blocked by the CM choke. Thus it prevents AFEC CM noise from moving to the DAB output circuit. The LV TIPS setup has 1:1 turn-ratio of the DAB MF transformer. For a CM circuit, the transformer turn-ratio does not affect the CM source magnitude or the CM impedances. Therefore the real magnitude of the CM voltages has to be considered. The rated condition LV TIPS experiment can not replicate the MV TIPS CM behavior and therefore the DAB output voltage is kept low to 27V. This makes the DAB primary converter CM voltage dominant and that appears across the CM choke at the LV inverter output. Fig. 9.29 shows the output choke results in grounding condition. There is only CM voltage drop across the CM chokes as can be seen from the respective spectra in Fig. 9.30 and Fig. 9.31. There are few conclusions from this LV experiment as below.

- When AFEC output dc neutral is grounded, the AFEC CM voltage drops across input choke as shown in Fig. 9.30.
- When the MF transformer emulation mutual capacitor C_{ps} is disconnected, there is no CM voltage or noise propagation to the output inverter.
- When the output Y-caps neutral is disconnected from ground but keeping the C_{ps}, a larger than expected HF CM voltage appears across the output choke as well as between load neutral and ground. This may be due to resonance between L_{cm2} and load parasitics. This shows that grounding is needed when a compact MV-HF transformer has significant C_{ps}.
- When the output Y-caps neutral is grounded, the expected CM voltage appears across the output choke as shown in Fig. 9.31. But the output neutral is at a defined ground potential.
- The CM currents in 150kHz range are small and even the dominant CM components are in limit after using the CM chokes.

9.11 Conclusion

The TIPS active unit's impedance transfer-functions clearly describe their dependence on control bandwidth, dc capacitor and loading level. The selection of bandwidths has been aptly made by plotting the AFEC output impedance and DAB input impedance on the same graph, which made the TIPS system stable. This chapter attempts to demonstrate the importance of grid-tie CM considerations for a realistic TIPS/SST. The TIPS/SST grounding and CM filtering is required for safety, uninterrupted operation and meeting the EMI standards. The compact transformer parasitics combined with high voltage and high dv/dt of the HV SiC devices, cause propagation of CM currents. This chapter presents another factor to compact HF transformer mutual capacitance specification used in the earlier chapter. Thus they play a role in optimization of cost, size and power-density of the SST/TIPS. This chapter formulates this optimization problem in context of TIPS topology & parameters and also identifies important design

factors. The combined TIPS simulation results considering parasitics and CM filters show the efficacy of the proposed passive CM filters. For the 4.16kV grid connected lab demo, the extra step-up isolation transformer allowed the MV side dc neutral to be grounded without installing the CM filters up to 8kV. The heat-sink to dc midpoint grounding, shielding of certain PCB & sensors and insertion of CM chokes in all power-supplies helped in reaching the final TIPS integration 8kV voltage level. The FFT spectrum of the experimental waveforms validate the EMI peaks and their relation with ZVS and filter (CM, DM) parasitics. The complete CM filter design is verified on the TIPS LV prototype setup with MV transformer parasitic scaling and emulation. These experiments resemble the simulations. This study highlights the importance of grounding and CM filters in the TIPS/SST system. This is the very first time operation of non-cascaded grid-tie HF isolated converter that has been reported at this voltage level.

Chapter 10

Novel ZVS range Extension of MV DAB using Series Compensation

10.1 Introduction

The motivation for the ZVS in MV converter of the MV DAB is presented in this chapter along with generalized ZVS criteria. This chapter proposes a novel ZVS extension technique for DAB. For simplicity, this technique has been implemented for a simple dual active half bridge (DAHB) topology but it can be extended to the original TIPS topology as well. It can enforce ZVS even in presence of significant limitations discussed earlier for a HV SiC based converter driven MV-HF transformer. This chapter also applies d-q current control for single-phase DAB converter for ZVS control. This topology is tested at 1.5kV using 15kV IGBT based MV converter and d-q transformation is verified. First, the structure and operation of the proposed LV side series compensated DAB is presented with simulation. It also presents a sinusoidal approximated simple model of the series addition and its numerical expression for Match-PF optimum utilization. A general specification for the series components is also presented.

With the detailed loss data for different v-i available for the 15kV IGBTs using the double-pulse (DP) test, a LUT of turn-on and turn-off losses is constructed. This is used for Matlab/Plecs simulation to predict converter switching and conduction losses quantitatively at 6kV. This chapter presents the efficiency curves for different series-compensation control modes. The simulation is an approximation but it helps to understand the series-compensation effects on the system efficiency. For this the MV DAB hardware parameters are considered in the simulation. This chapter proposes an optimum look-up-table (LUT) of series-compensation angle (θ_c) and duty (d_c) based on optimum curve. In the last, this chapter presents the MV experimental validation of the series-compensation technique at 6kV-270V DAB operation using 15kV IGBT and then 10kV MOSFET on MV side and 1200V MOSFET on LV sides. The switching transitions are compared.

10.2 ZVS Considerations of a MV DAB

The DAB ZVS condition holds as long as the DAB current zero-crossing (ZC) lags the MV voltage ZC but leads the secondary voltage ZC. Fig. 10.1 shows the general DAB ZVS condition with normalized secondary voltage. For a DAB, if there is a deviation in normalized dc voltage-ratio (N_v/N_t) beyond $\cos(\phi)$ or $1/\cos(\phi)$ p.u. from the nominal turns-ratio (1 p.u.), the ZVS is lost for load angles smaller than ϕ [20]. For boost-mode when p.u. output voltage is higher, primary converter loses ZVS and vice versa. The DAB ϕ reduces towards lighter loads. This also reduces the DAB ZVS range [20]. For deviated N_v conditions, DAB PWM control helps to maintain ZVS until certain light-load by adjusting primary and secondary converter duty-ratios in relation to the N_v [81]. But the reduced D's themselves limit ZVS range since the current ZC must lag by a margin defined by D from primary switch turn-on instant [42]. There is also current-ringing in MV converter caused by applied step-voltage's interaction with MV transformer parasitics characterized in [32]. The current-ringing also reduces ZVS range [42]. The quasi-square MV pole voltage moderates the current ringing in a single-phase DAB [42]. Thus the factor's limiting ZVS are N_v/N_t deviation, light-load, smaller D, dead-time and current-ringing. A small rated-

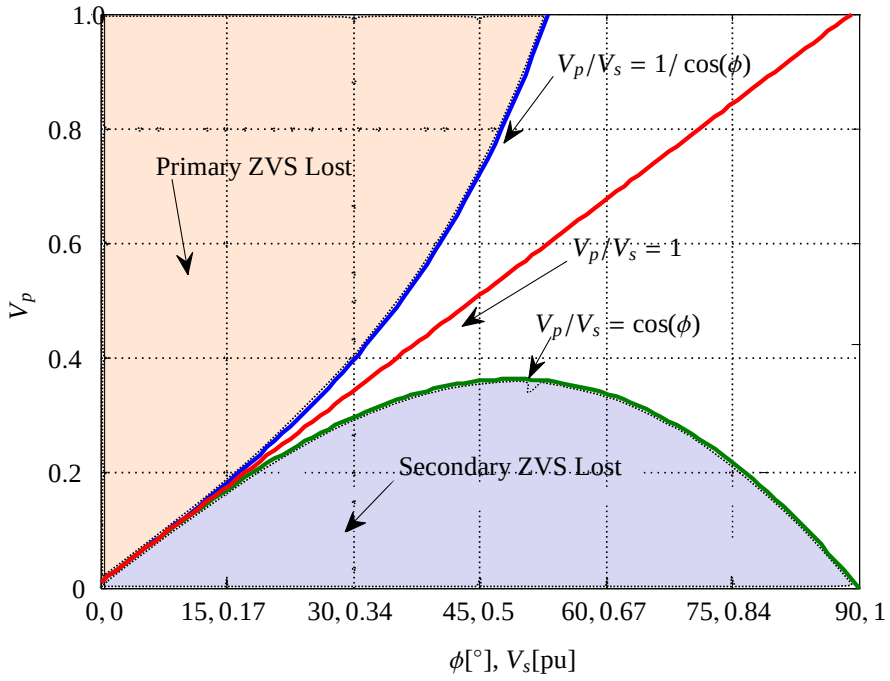


Figure 10.1: DAB converter ZVS with DAB angle in terms of voltage-ratio

load L_{DAB} or smaller ϕ DAB design suffers not only of poor controllability but narrow ZVS range. The opposite design suffers from lower P/Q ratio or higher DAB reactive power which is responsible

for higher current and conduction losses [42]. For optimum MV DAB, it is desirable to maintain a sufficiently small positive virtual DAB-angle ϕ' using series-compensation for expected load and N_v/N_t variation. This is equivalent to manipulating L_{DAB}.

10.3 Proposed Novel ZVS Technique

In literature, there are two approaches to ensure ZVS at light-load, either by change in switching pattern [115], or by change in DAB reactance. The first method does not need additional hardware and relieves device stress by cutting down reactive-power caused by any dc voltage-ratio (N_v) deviation. But it reduces the maximum power capability in buck-mode. Moreover it introduces multiple device-switching in the converter half-cycle which is not desirable for MV high-power DAB. In second approach, DAB reactance can be changed either by controlling switching-frequency (f_{sw}) with load [116, 117] or by employing a variable inductor. Increasing DAB f_{sw}, does not help much as the switching losses increase proportionally and it is ineffective against the N_v deviation. The variable inductance can be in form of a saturable inductor [46] or can be changed in discreet steps. The former method shapes current near zero-crossing (ZC) using a saturable reactor. The DAB inductance is non-linear and it becomes effectively higher near ZC. This effectively increases light-load angle. In discreet method such as a DAB employing a complex transformer with dual leakage design [105], transformer leakage inductance is increased at light load so that DAB-angle (ϕ) increases. This approach has little flexibility in controls and requires additional relays and complex over-rated transformer. Another method of N_v compensation can be a DAB transformer with taps which are adjusted based on input to output N_v. But tap changing control is discontinuous with limited number of taps and it also needs other accessories. The proposed method virtually changes the tap setting besides injecting desired Q_c into DAB coupling [118]. The topology is shown in Fig. 10.2. The hardware addition for series compensation is a fractional rating series-transformer fed with an additional half/full bridge based on fractional current-rating switches at low-voltage (LV). The previous approaches look simpler since additional magnetics can be integrated in the main transformer (T_{r1}) design. However on a MV converter, parasitics caused ringing, dead-time and any D less than 50%, need certain lagging current for ZVS [42, 49]. Thus they narrow down ZVS range available even if the N_v/N_t is 1.0. Thus series-compensation is useful as it can control power-factor (PF) and ac voltage-ratio of the main converters independently. The series-compensation adds two-dimensional (2-D) series voltage components which provide more flexibility than a tap-changing DAB. The first component can maintain converter ac voltage-ratio even with a deviated dc N_v. The second component can widen/narrow-down effective virtual-ϕ (ϕ') as per requirement. It can maintain ZVS even with significant error in sensing dc N_v and with significant dead-time at light-load. The two components can be set such that the current vector is placed in the middle of main converter voltages even under N_v deviation. This setting is termed as matched-power-factor (Match-PF) mode. It ascertains ZVS throughout but not necessarily results in optimum efficiency. The light-load DAB operation at de-

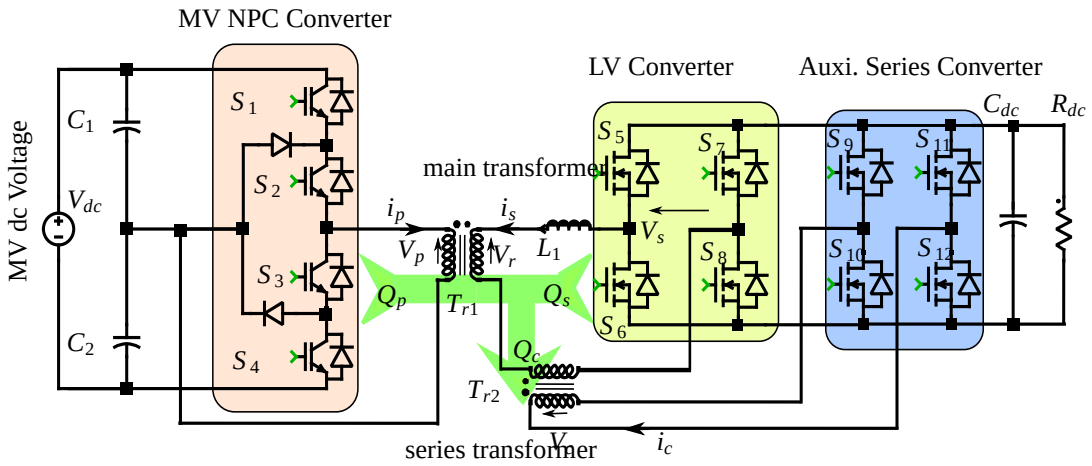


Figure 10.2: DAB schematic with secondary side series-compensation

viated N_v, causes poor efficiency. The main converter PF can be reduced for ZVS by injecting series Q_c. Optimum series-compensation can help restore light-load efficiency. It can reduce DAB current (rms, peak) towards higher loads and deviated N_v. Thus it does not only maintain ZVS but also reduces the turn-off switching and conduction loss. The series transformer (T_{r2}) adds core-loss when turned on, but the overall loss is still smaller for a typical high-power MV DAB.

10.4 DAHB Power Topology as Test-setup for ZVS technique

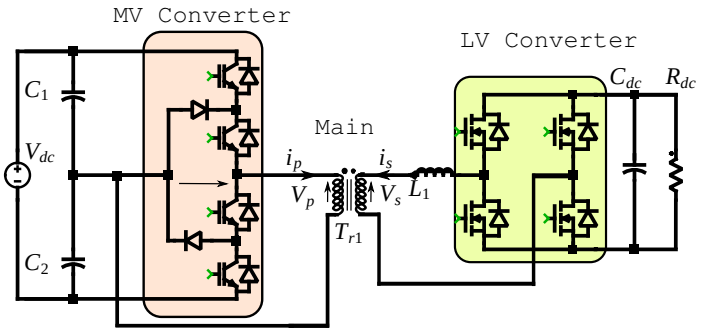


Figure 10.3: Single-phase DAHB topology

The DAHB has a two winding MV-HF transformer connected to the converters as shown in Fig. 10.3. The low-voltage side of the DAHB is connected to two-level H bridge converter similar to [119]. A three-level NPC half bridge converter is connected on the high voltage side. This topology can generate

a quasi square three-level waveform while saving device voltage rating at the HV side. The DAB can be operated in 60° zero clamping mode to eliminate 3^{rd} harmonic voltage across transformer windings in addition to reduction in applied step voltage. As the frequency of converters is fixed at 10 kHz, one quarter cycle delay on the sensed transformer current, can be used to generate imaginary second phase current [120]. The two phase $\alpha - \beta$ currents can then be transformed to standard d-q frame. The real component of the d-q current can be used for inner current control loop. This d-q based control also works for the square wave operation and other single-phase DAB topologies. A d-q based inner current and outer voltage control algorithm of the DAB is presented in this chapter. The proposed d-q control technique for single-phase DAB ensures fast dynamic performance. The full d-q control can regulate the current phase by adjusting primary and secondary duty-cycles dynamically. Hence it can provide a simple controller implementation ensuring ZVS and high efficiency.

The DAHB converter topology and d-q control is motivated from [36] for a simpler possible converter topology with 15 kV SiC IGBTs HV devices and LV 1200 V SiC MOSFET. The three-level converter on HV, offers half dc voltage stress to the semiconductor devices. A practical MV-HF transformer has significant inter turn parasitic capacitance [49]. The 35 kVA, 10 kHz TIPS MV-HF transformer parameters are adapted for simulation as shown in Table 10.1. Table 10.2 shows DAB simulation param-

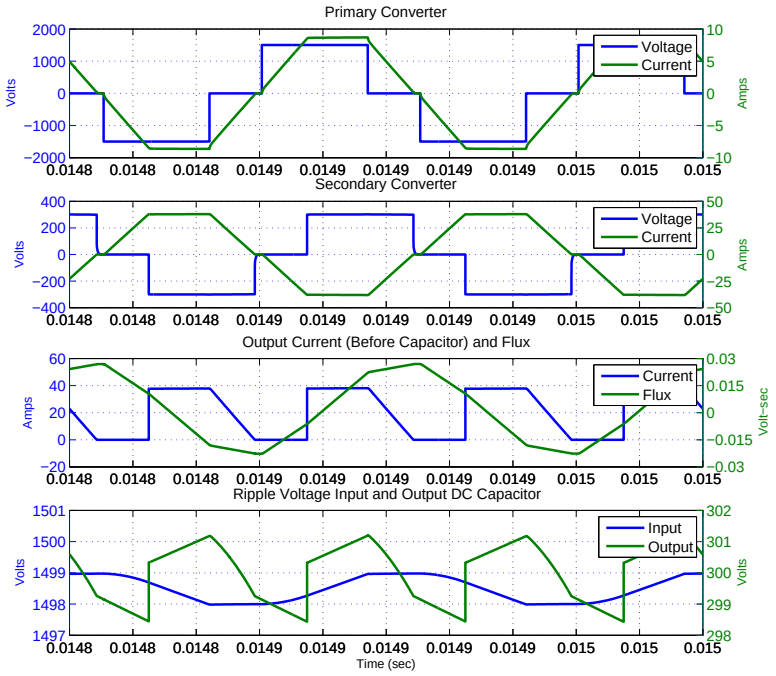


Figure 10.4: Simulation results with 60° mode

eters. Fig. 10.4 shows the DAB waveforms for 60° operation. The frequency spectra for corresponding

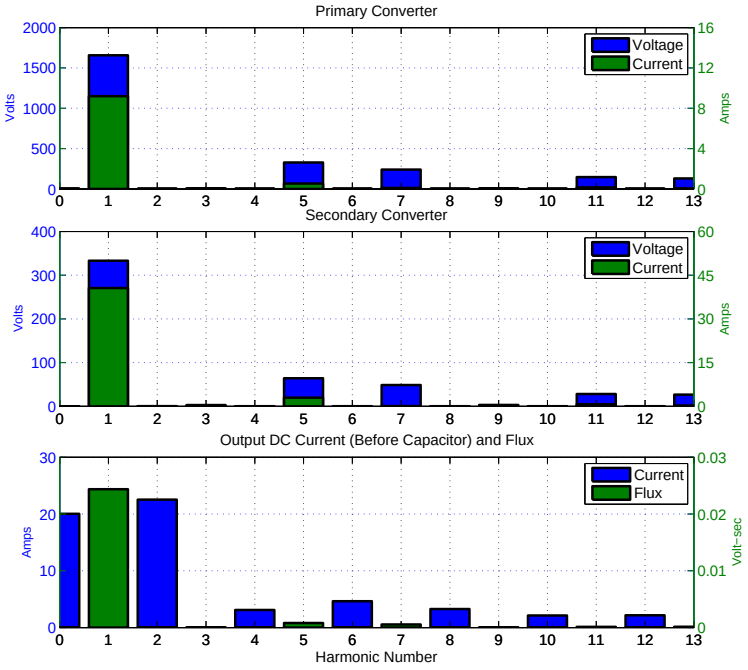


Figure 10.5: FFT of simulation with 60° mode

waveforms are shown in Fig. 10.5. The three-level converter with 60° zero period control (< 50% Duty) moderates the maximum step voltage applied on the HV side of transformer. This helps to reduce the peak inrush current through the HV devices. The low-voltage two-level H bridge converter is also operated in 60° zero period phase transition mode similar to the HV side. Fig. 10.6 shows waveforms for square wave operation. The frequency spectra for corresponding waveforms are shown in Fig. 10.7. It can be observed that dc current ripple goes from negative to peak positive. Hence the DAB with discussed control requires dc capacitor size with smaller RMS current rating and generates smaller voltage ripple for same DAB angle. The smoother current shape makes transformer and inductor utilization factors higher. The 60° mode reduces the peak flux to RMS flux ratio similar to three-phase DAB [121]. The DAHB topology also produces half ac voltage as compared to full bridge, reducing the transformer turn-ratio to half for the high transformation ratio application. Both these facts are useful in optimization of the transformer design for high power density. Fig. 10.8 and 10.9 show the DAB instantaneous $p-q$ power simulation for the two modes. It is calculated by using imaginary β axis voltage and current in addition to the real value. It can be seen that p_{ac} has higher magnitude for the square-wave mode as an indication of reciprocating energy between input and output. Though 60° zero control eliminates the 3^{rd} harmonic voltage, it also reduces the fundamental voltage and the maximum power capability at a dc voltage and inductor value. Hence inductor value has to be calculated for the reduced voltage. Another limitation of 60° mode is that ZVS range of the outer devices reduces with the duty-cycle and DAB

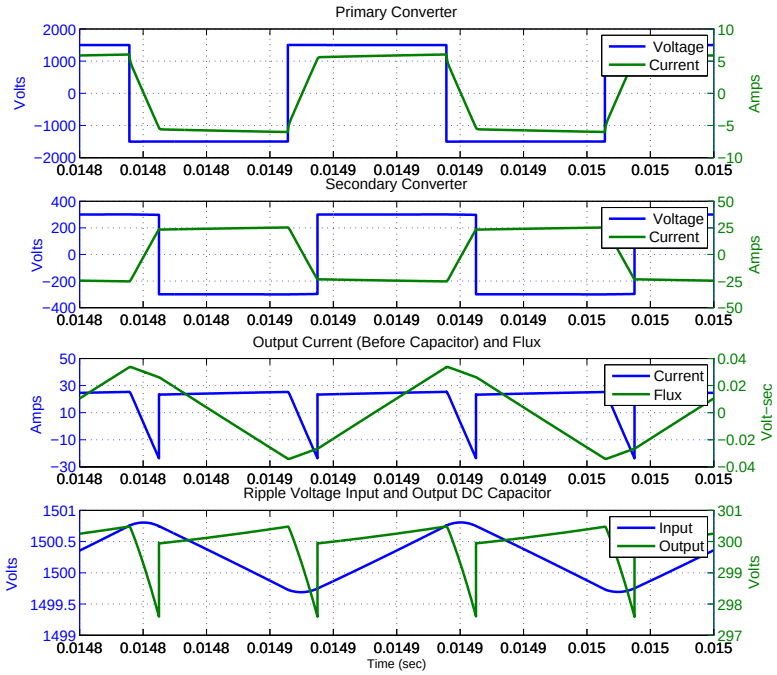


Figure 10.6: Simulation results with square wave mode

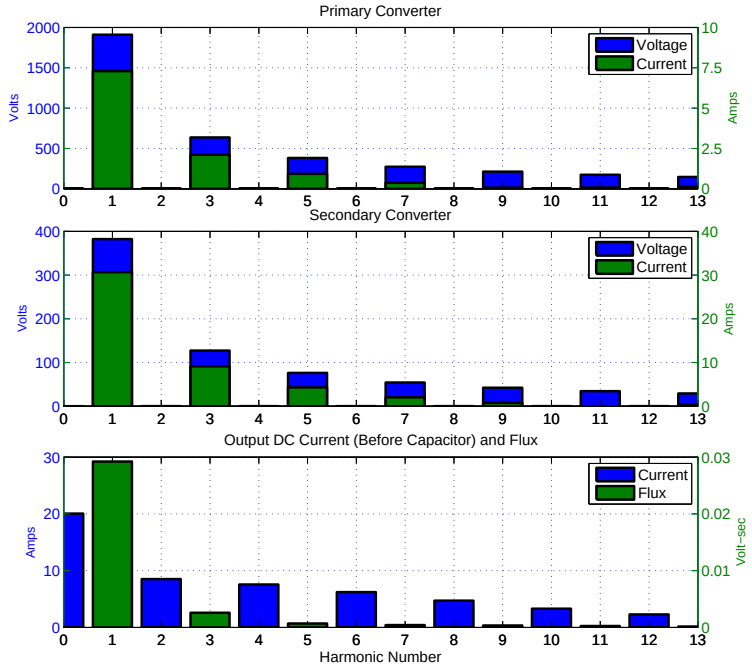


Figure 10.7: FFT simulation with square wave mode

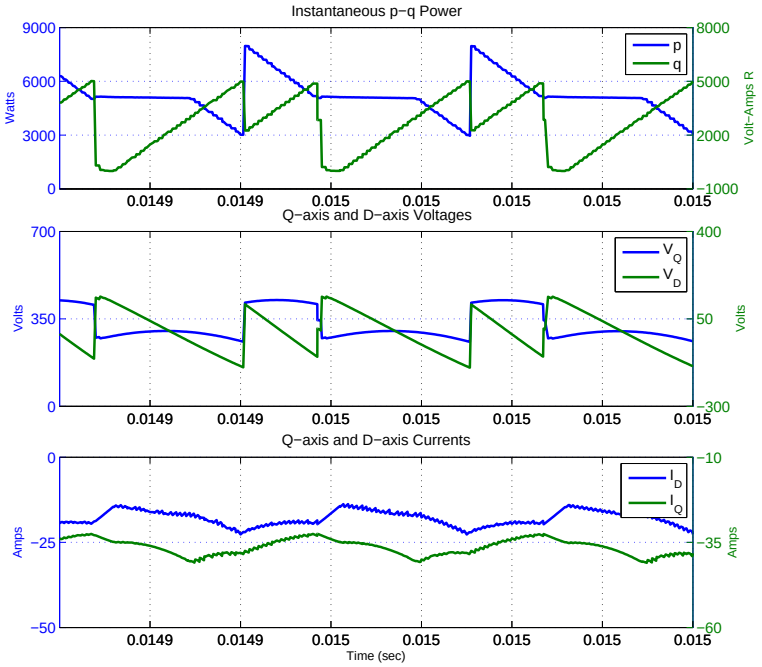


Figure 10.8: Instantaneous $p - q$ plot with 60° mode

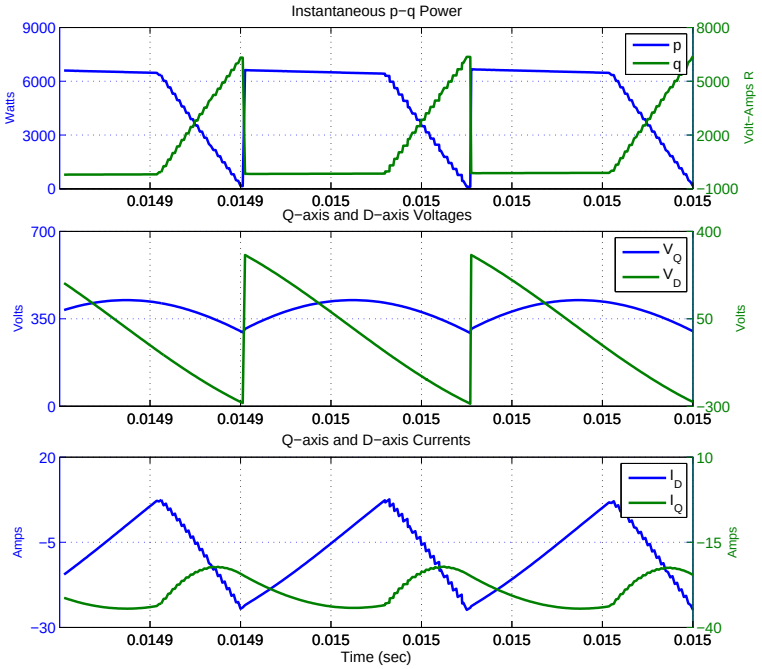


Figure 10.9: Instantaneous $p - q$ plot with square wave mode

Table 10.1: MV-HF transformer parameters

Parameters	**Value[Units]**
Mag. Inductance, L_m	293 mH
Total Equi. Diff. Capacitance, C_p	250 pF
Total Leakage from HV side, L_1	643 μH
DAB Inductance	80 μH
Total Mutual Capacitance	1200 pF
Switching frequency	10 kHz

Table 10.2: Simulation parameters

Parameters	**Value[Units]**
Input dc Voltage	3 kV
Output dc Voltage	300 V
DAB Inductance	80 μH
Real Power Transfer	5 kW
Switching frequency	10 kHz

current needs to lag behind the turn-on instant by half the zero period. Three-phase DAB eliminates 3^{rd} harmonic voltage without reducing the fundamental voltage or the narrowing the ZVS range, thus it has an advantage. It offers smaller dc ripple than the single-phase topologies.

10.5 DAHB Control

Secondary H bridge converter operates with a reference phase-transition modulator. The three-level converter is operated with phase shift modulator that changes the phase angle of generated voltage with respect to two-level side voltage. The transformer ac current is transformed into synchronously rotating d-q reference frame aligned with secondary voltage vector which is produced as a reference in the controller board. The block diagram of the above control algorithm is presented in Fig. 10.10. Sudden load (50%) is applied for two cases, 60° and square modes. The 60° mode reduces maximum power transfer capability. This is important to note that, for both cases the output power is kept same, hence 60° mode requires higher fundamental current and its benefit of smaller ripple voltage, ripple current and peak current may seem moderated in the simulations. Fig. 10.11 and 10.12 show the transient simulation waveforms for the two cases. The i_{sq} has smaller noise for 3^{rd} harmonic elimination case than the i_{sd} and it is smoother compared to the DAB output current. The DAB output current has 20 kHz frequency and requires filtering for current control. The rectified ac current is not an optimum signal

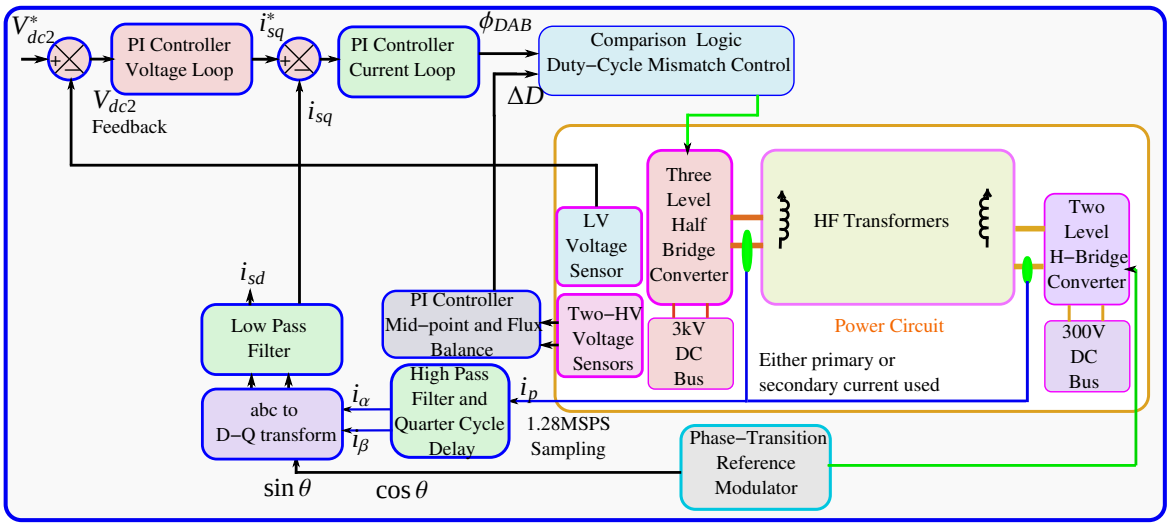


Figure 10.10: Single-phase DAHB control in d-q mode

to be used for current control as it has only magnitude information and not the angle information. The d-q currents have smaller magnitude and 40kHz ripple and so offer fast current control loop. Three level converter can also be used in varying pulse mode together with secondary converter for optimum operation [122]. This is simpler to implement with d-q based control which already has decoupled reactive and active current information. The three-level converter also has mid point voltage correction loop implemented. The dc volt-sec applied across transformer is measured with R-C filter and compensated by adjusting three-level duty cycle.

Table 10.3: Parameters of the SiC MOSFET and IGBT experimental setup

Parameters	**LV Setup Value[Units]**	**HV Setup Value[Units]**
Input dc Voltage	800V	1.5kV
Output dc Voltage	70V	107V
DAB Inductance	80μH	80μH
Real Power Transfer	1kW	5kW
Switching-frequency	10kHz	10kHz

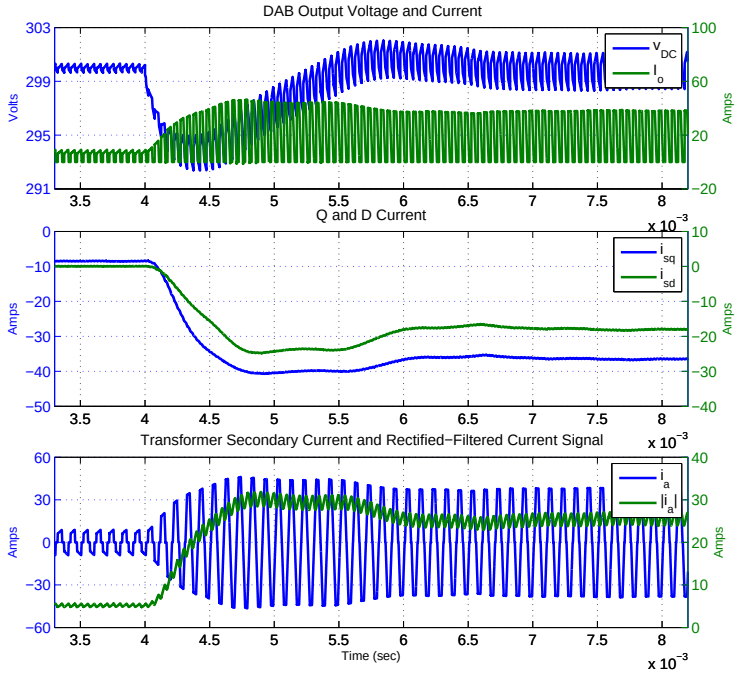


Figure 10.11: Transient simulation with 60° zero control

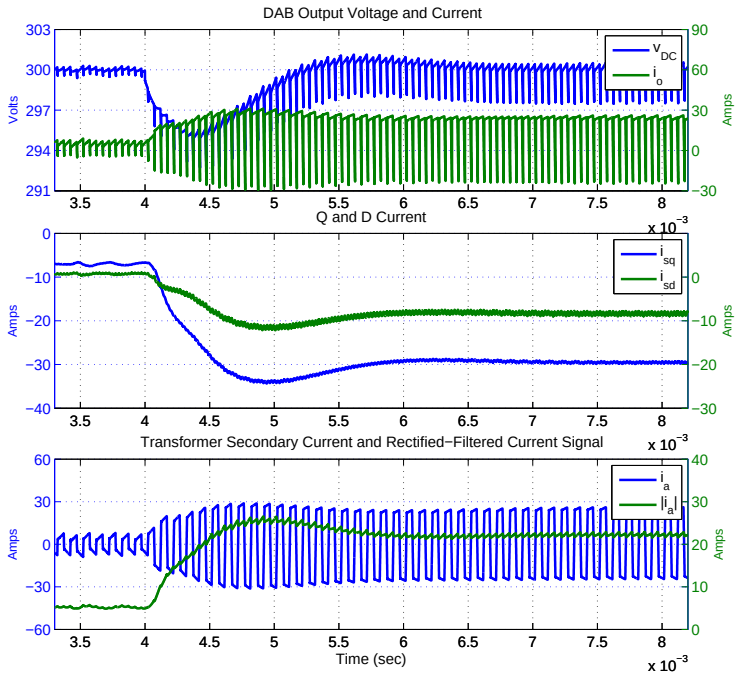


Figure 10.12: Transient simulation with square wave mode

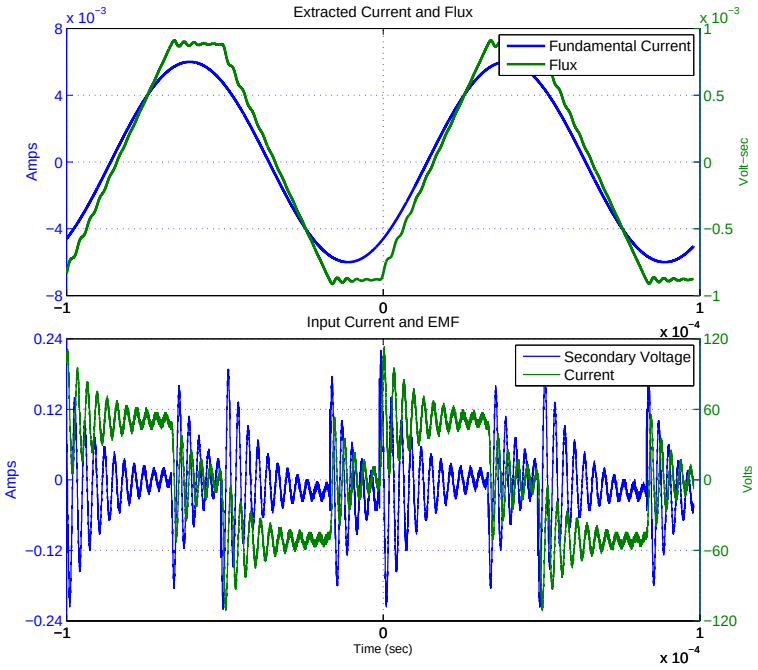


Figure 10.13: Experimental flux plot of hf transformer with 60° mode

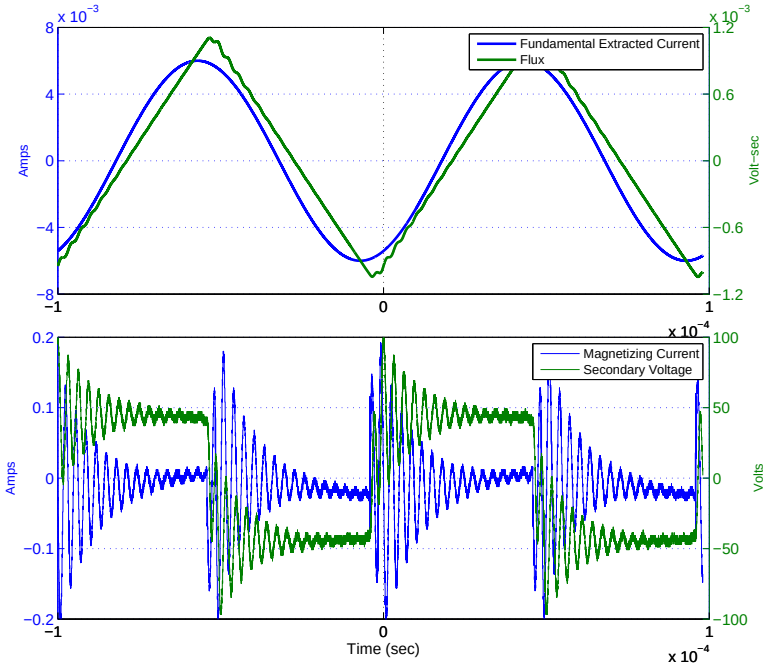


Figure 10.14: Experimental flux plot of hf transformer with square wave mode

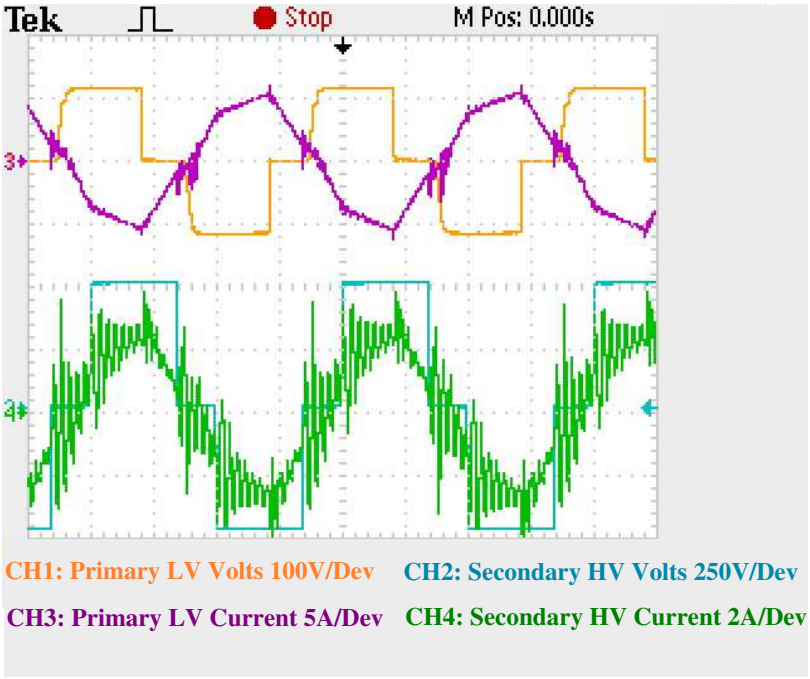


Figure 10.15: Experimental results with only MOSFETs and 60° mode

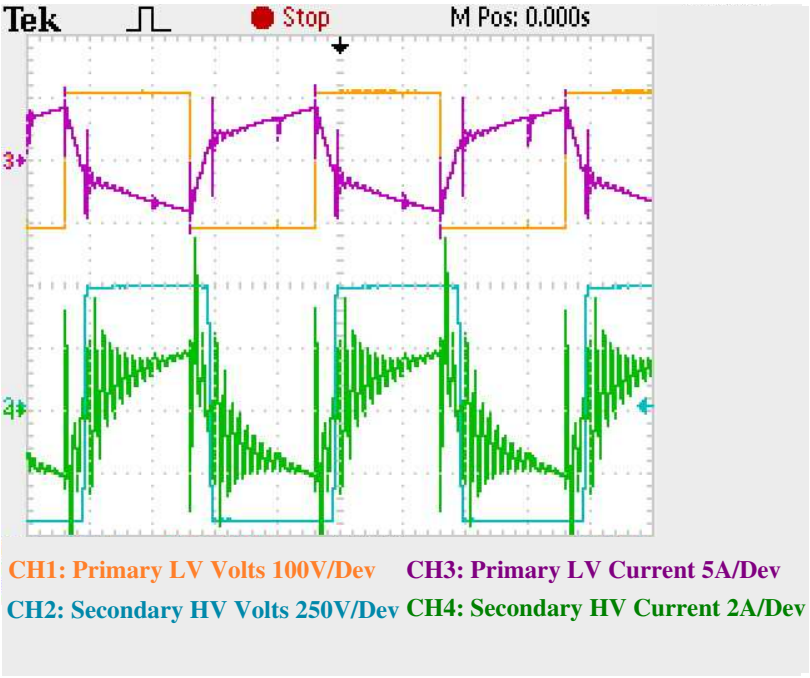


Figure 10.16: Experimental results with only MOSFETs and square wave mode

10.6 Experimental Results

Fig. 10.13 and 10.14 show the DAB experimental flux waveform for the two types of excitation from the HV side with LV open. The dc Bus at HV is 800 V for excitation test. Since the 60° mode reduces fundamental voltage, the dc bus voltage is reduced for square mode to fairly compare the peak flux for same fundamental voltage. The extracted fundamental current has same magnitude. It can be seen that peak flux is higher for the square mode due to triangular shape. This also depends on DAB angle but weakly, due to higher per-unit inductance at the secondary for TIPS setup. Thus 60° mode under-utilizes switch ratings but may optimize the magnetics. The ringing in the current, due to parasitics, makes it difficult to plot the B-H curve. Table 10.3 shows two sets of experimental setup parameters. First experiment is done with SiC MOSFET based H bridge converter at the 800 V side as well on the secondary side. Fig. 10.15 and 10.16 show the experimental waveforms for this case. As expected, the HV side current caused by transformer parasitics, has smaller ringing at switching instants for 60° mode compared to the square mode. Second experiment is with 15 kV SiC IGBT three-level half bridge at the HV side and secondary remains same. Fig. 10.17 shows the experimental setup for HV TIPS application configured for this case. Fig. 10.18 and 10.19 show the experimental waveforms for second experiment

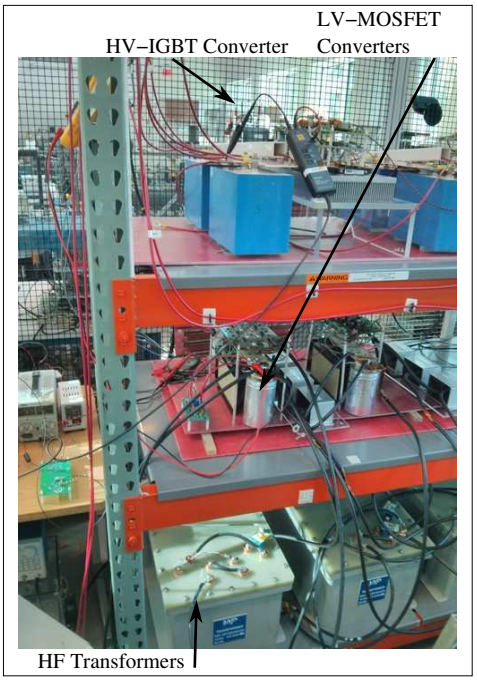


Figure 10.17: Single-phase dab setup (originally three-phase setup)

at 1.5 kV. Now, the HV side current caused by transformer parasitic, has smaller peak currents for both

cases. This can be attributed to the fact that 15kV SiC IGBT applies slower dv/dt at transformer whereas ideal dv/dt was applied for the SiC MOSFET. At further higher voltage (> 6kV), the primary current

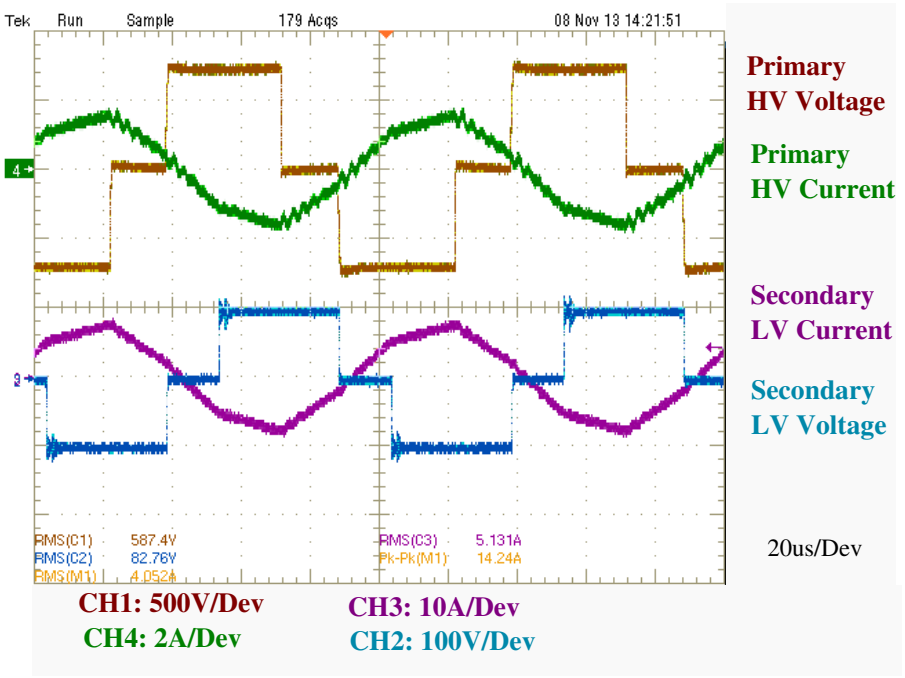


Figure 10.18: Experimental results with 60° zero control

will pick-up ringing as the dv/dt will rise due to punch through [41]. And this topology will look more advantageous from current ringing point of view as the HV device has limited current capability. Fig. 10.20 shows the experimental waveforms for d-q current calculation using FPGA controller and fast ADC board. The D and Q signals are as expected from simulation.

10.7 Series Compensated DAB Topology

10.7.1 Structure

The single-phase DAB is popular over three-phase DAB due to its simplicity of the power-topology and control. However, it has the disadvantages of relatively higher dc capacitor size, higher peak current and flux in the transformer [19, 34]. From device reliability perspective of a MV dc-dc system, simpler topology like dual active half bridge (DAHB) with fewer switches while still providing flexible operation should be selected [39]. Fig. 10.2 shows the DAHB topology in which a three-level (3-L) half-bridge leg based on 15kV SiC IGBT, is connected to the MV side of a 10 kHz main transformer. A two-

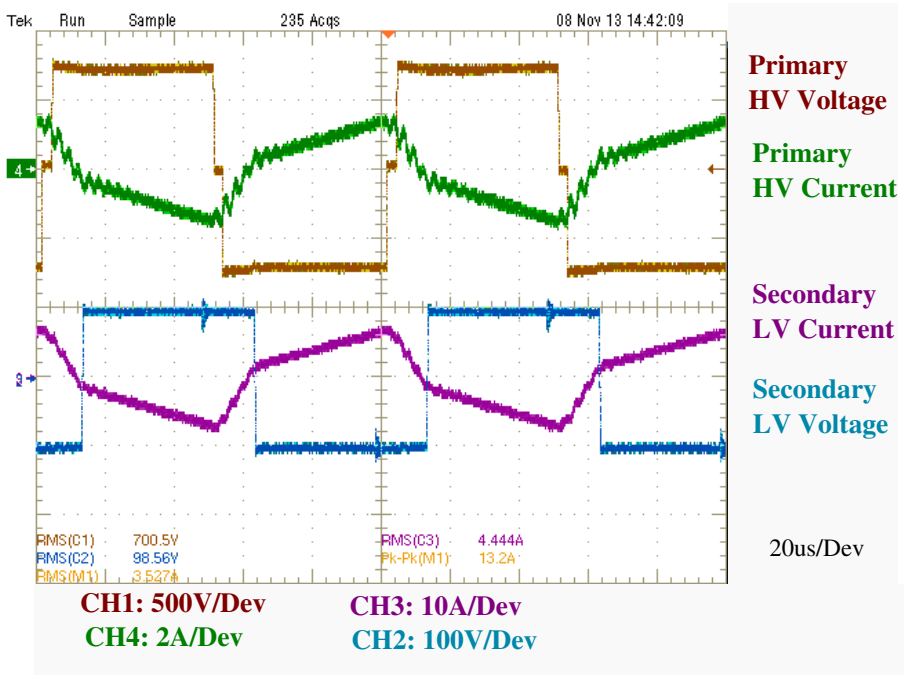


Figure 10.19: Experimental results with square wave mode

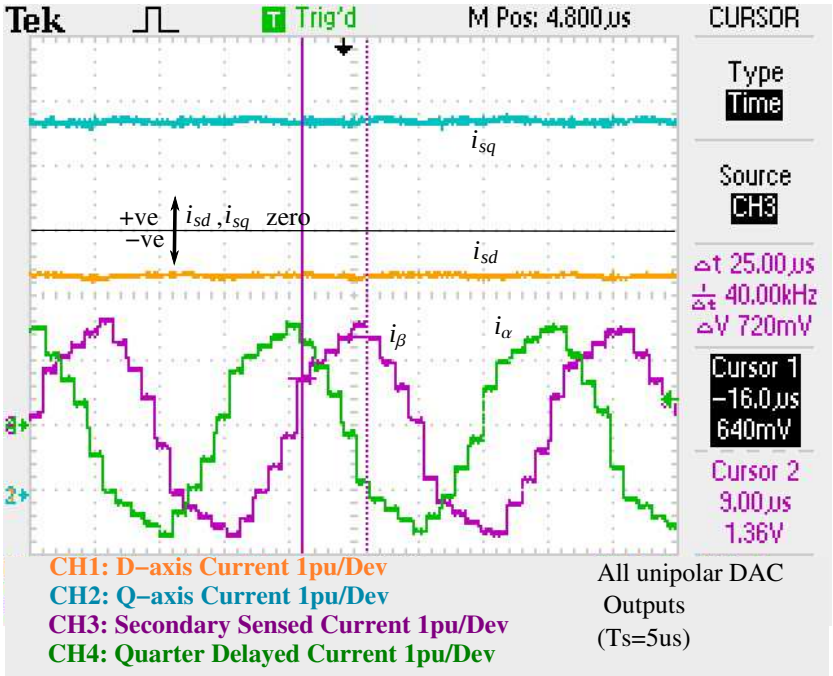
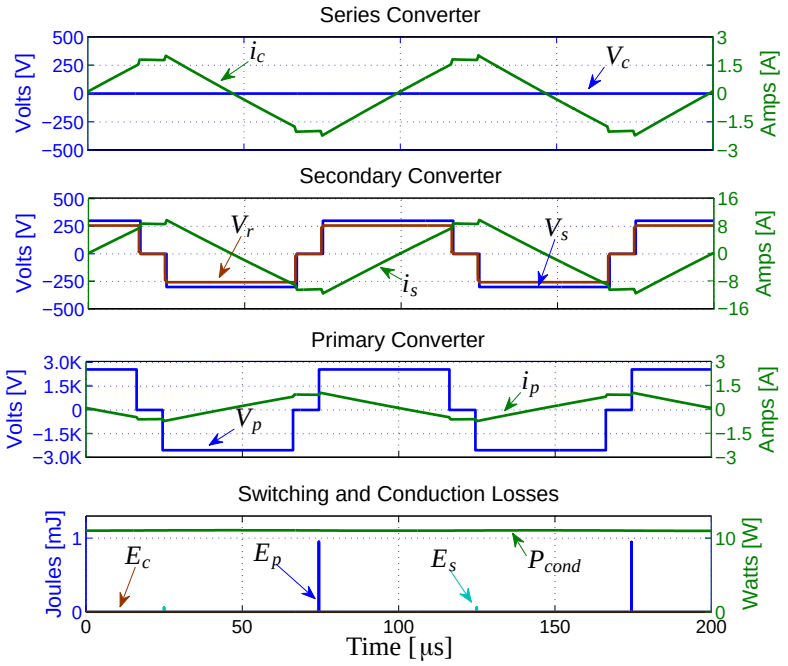


Figure 10.20: Experimental results d-q current calculation

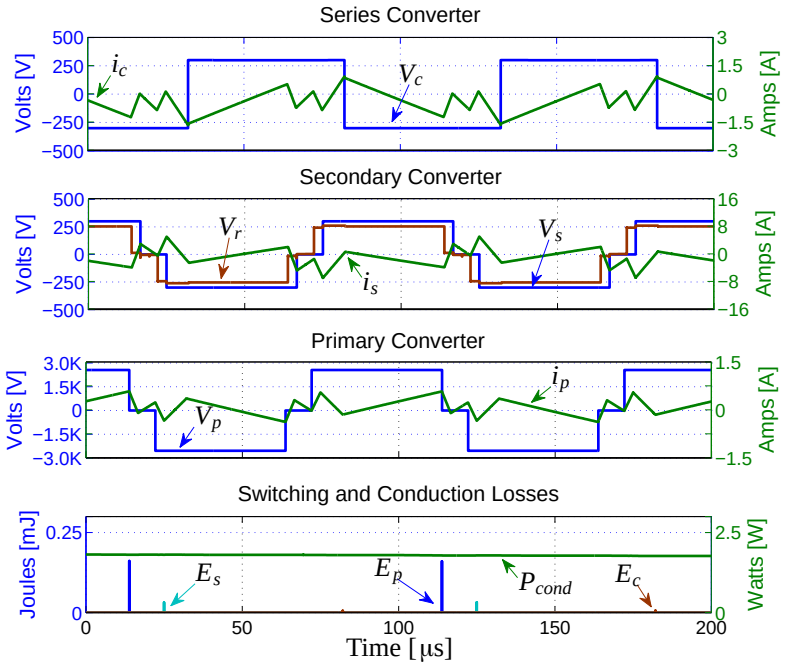
Table 10.4: Parameters of MV simulation and experiment

Parameters	**MV Hardware & Simulation Value[Units]**
Input dc Voltage[V_{dc}]	6 kV
Output dc Voltage[V_o]	300 V
External Inductance[L_1]	80 μH, 0.2 Ω
T_{r1} Leakage Inductance (LV side)	8 μH, 13 mΩ
T_{r1} Turns-ratio	10 : 1
T_{r2} Leakage Inductance (LV side)	6 μH, 8 mΩ
T_{r2} Turns-ratio	1 : 5
C_{dc}	10000 μF
Rated R_{dc}	20 Ω
C_1, C_2	120 μF
Real Power Transfer	5 kW
T_{r1} Core Loss	50 W
T_{r2} Core Loss	20 W
Switching-frequency	10 kHz

level (2-L) H-bridge based on 1200 V SiC-MOSFET characterized in [101], is connected to LV side. The MV series-compensation DAB simulation and hardware parameters are shown in Table 10.4. This makes single-phase DAB current resemble to that of three-phase DAB waveforms but at the cost of reduced maximum power capability. Compared to square-waveforms it offers smaller peak flux for same fundamental voltage. Thus it saves transformer size for a given real-power but at the cost of reduction of ZVS range for outer MV devices (S_1, S_4) in DAHB and non-utilization of switching devices to the full capacity. The two inner devices (S_2, S_3) at MV operate in fully soft-switched mode as ZVS range expands for inner switches. This is due to the fact that inner devices have complementary gate signals respective to the outer devices (S_4, S_1) [42]. As shown in Fig. 10.2, for the series circuit, an additional LV H-bridge feeds primary of an auxiliary series transformer. The secondaries of the main and series transformers are connected in series. The series-compensation can be added to all DAB topologies including the most popular DAB based on H-bridges. The series transformer is excited from LV to avoid extra MV devices. The secondary of the series transformer can be connected in series of either primary or secondary of the main transformer. If connected on primary, MV isolation is also required on series transformer, so it is preferred to be connected on secondary. Simulations show that both cases result in similar performance.



(a) Without series-compensation



(b) Optimum lead series-compensation

Figure 10.21: Boost mode with 15% smaller input voltage at 5% load

10.7.2 Operating Principle

In MV DAB simulation/hardware, the main converters are operated with 41% D and the series converter operates with square-wave or 50% D. The series voltage (V_c) phase is controlled with respect to the LV converter voltage as in Fig. 10.2. The two loading conditions are simulated without and with series-compensation for optimum leading and lagging phase-angles respectively. These angles are taken from the optimum efficiency curve explained later.

Light Load Operation

Fig. 10.21(a) shows light-load simulation without series-compensation under 15% smaller input voltage. It can be noticed that MV converter ZVS is lost, resulting in increased switching loss. There is also additional conduction loss due to increased reactive-power. Fig. 10.21(b) shows the simulation with optimum lead series-compensation which maintains ZVS. It also brings down conduction loss but adds series transformer core-loss. It has nearly 90° leading phase of V_c. For lead series-compensation, the resultant secondary voltage V_r leads secondary converter V_s. Since V_r phase with primary vector V_p remains approximately same at the given unchanged load, ϕ' is widened. This shows that DAB converters now operate in ZVS, even at a small operating ϕ at light-load with deviated N_v.

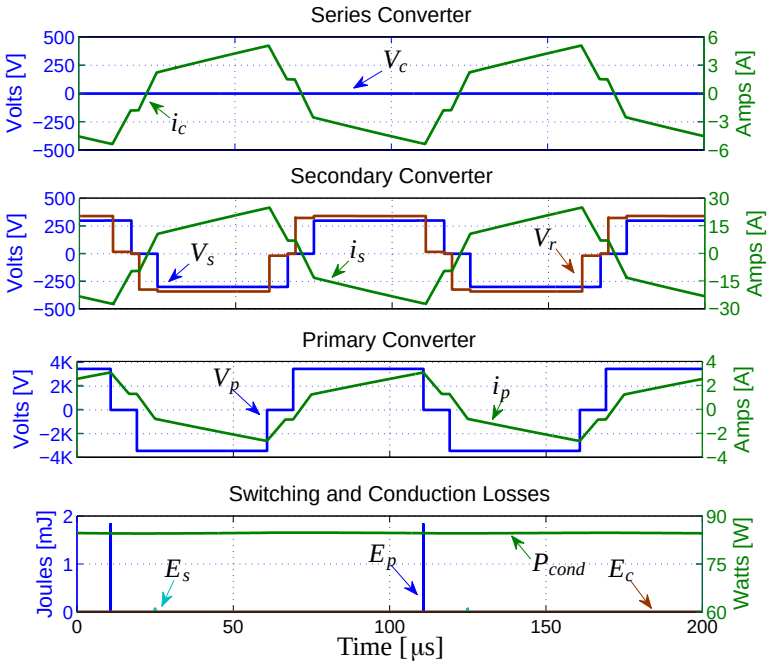
Full Load Operation

Fig. 10.22(a) shows full load simulation without series-compensation under 15% larger input voltage. It yields more conduction loss due to higher reactive-power and larger turn-off IGBT switching losses. Fig. 10.22(b) shows the simulation with optimum lag series-compensation. It improves the current shape, reduces the magnitude and also reduces reactive-power flow. Thus it helps to reduce the turn-off and conduction losses. It has nearly 90° lagging phase of V_c. For lag series-compensation, V_r lags V_s. Since V_r phase with respect to V_p remains approximately same at the given unchanged load, DAB converters can operate at a relatively smaller virtual ϕ' even at full load, resulting in smaller turn-off losses. It also decreases reactive-power and conduction losses in the DAB. If series-compensation is controlled with the loading of DAB such that MV converter maintains a small lagging PF, the ZVS can be ensured throughout.

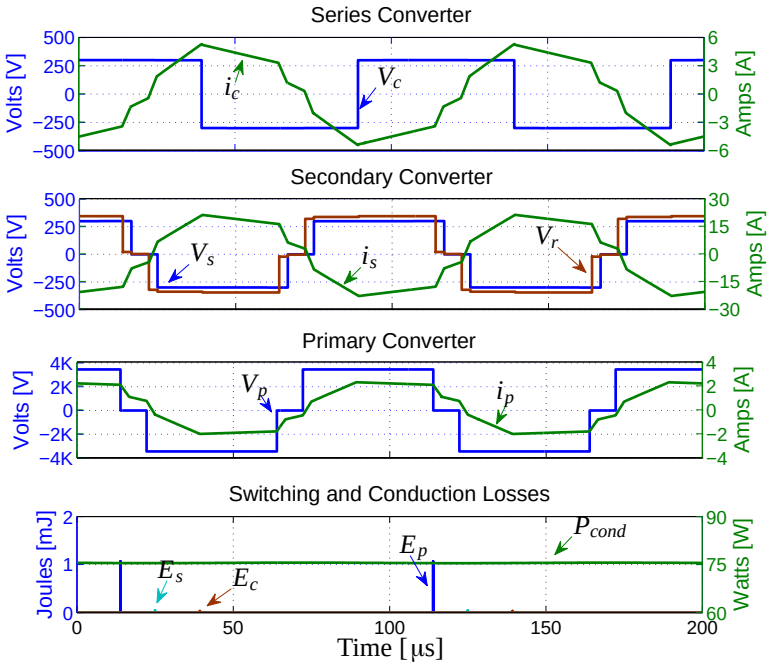
10.8 Series Compensated DAB Control

10.8.1 Modeling of DAB with Auxiliary Series Winding

The DAB operates with square/quasi-square voltages which can be approximated as sinusoidal for a simple series-compensation model. The aim of this simple mathematical model is to calculate the ZC or the fundamental vector-angles in presence of series-compensation. This helps in ZVS determination and



(a) Without series-compensation



(b) With optimum Lag series-compensation

Figure 10.22: Buck mode with 15% larger input voltage at full load

thus the simplification is reasonable. Fig. 10.23 shows sinusoidal approximation vector-diagram of the DAB with series-compensation. Table 10.5 shows the symbol notations used. The series-compensation

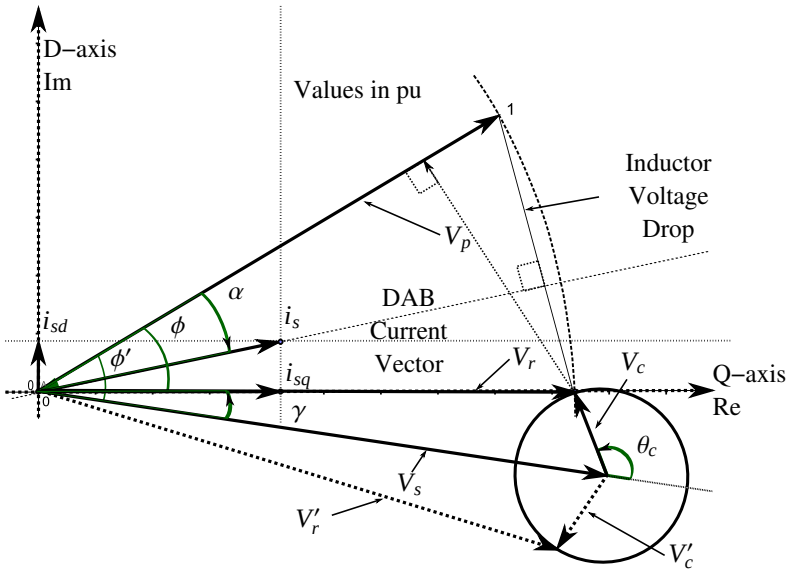


Figure 10.23: Fundamental vector diagram for series compensation

phase θ_c can vary from 0° to 360°. The N_c is defined as depth of compensation and it is ratio of V_c magnitude to the original V_s magnitude. For a given fixed load, V_r remains at approximately constant ϕ with V_p, if N_c is a small fraction. Expression (10.1) shows V_r magnitude of the DAB. The ϕ of V_r for a given fixed load, real-power is given in (10.2). The primary PF angle (α) assuming purely reactive DAB series-inductance, is given in (10.3). The phase (γ) of V_s with respect to V_r is shown in (10.4). The angle between V_s and V_p, (ϕ') is shown in (10.5). From this last relation, the series-compensation in quadrature phase ($\theta_c = 90°$) is equivalent to manipulating the virtual DAB reactance.

$$V_r = \sqrt{(V_s^2 + V_c^2 + 2V_s V_c \cos(\theta_c))} \tag{10.1}$$

$$\phi = \sin^{-1} \frac{PX}{V_r V_p} \tag{10.2}$$

$$\alpha = \tan^{-1} \frac{V_p - V_r \cos(\phi)}{V_r \sin(\phi)} \tag{10.3}$$

$$\gamma = \sin^{-1} \frac{V_c \sin(\theta_c)}{V_r} \tag{10.4}$$

$$\phi' = \phi + \gamma \tag{10.5}$$

Table 10.5: Vector diagram symbols (per unit)

N_t	DAB transformer turn-ratio	N_v	DAB dc voltage-ratio
L_{DAB}	DAB series inductance	N_v/N_t	normalized dc voltage-ratio
N_c	Depth of compensation (V_c/V_s)	θ_c	Series phase angle
ϕ	DAB phase angle V_p to V_r	γ	Compensation angle V_r to V_s
α	Current vector angle V_p to i_p	ϕ'	Virtual DAB angle V_p to V_s
Q_c	Series reactive-power	PF	Power-factor
D	Main converters duty-ratio	d_c	Series duty-ratio
V_r	Resultant voltage	V_p	MV converter voltage
i_p	MV converter current	V_s	LV converter voltage
dv/dt	Switching voltage steepness	f_{sw}	Switching-frequency
MV	Medium-voltage	di/dt	Switching current steepness
i_s	LV converter current	P	DAB real power
X	DAB reactance	V_c	Series converter voltage
LUT	Look-up-table	Match-PF	Matched-power-factor
PT	Punch-through	MF	Medium-frequency
ZC	Zero-crossing	MF	Medium-frequency

10.8.2 Specification of Series Components for the DAB

The main transformer turn-ratio is selected in the ratio of rated V_p and V_s voltages. The series transformer turn-ratio is selected according to the N_c required. Higher N_c may result in better ZVS range but increases size, weight and cost of the system. An optimization between series component's rating, cost, efficiency and performance is needed. The N_c is selected based on the minimum ϕ' that needs to be maintained for near zero load or the maximum N_v deviation expected. A 20% N_c is selected for implementation as it can create virtual $\phi' = \tan^{-1} 1/5 = 11.3°$ at zero load. This ϕ' is sufficient to account for the ZVS margins needed for both main converters. The rated load DAB ϕ is 40° selected based reactive power considerations [42]. The series transformer secondary carries same current as the main transformer secondary but has lower voltage rating. The series transformer primary has same voltage rating as the main transformer secondary but lower current rating as determined by the N_c. The series transformer real-power rating is also a N_c-factor of main transformer rating. The LV series transformer switches have LV voltage rating but a N_c-factor current rating. The series transformer core loss should not be high. The series transformer series winding should not have high resistance. For a high-power MV DAB this fractional rating series transformer can recover the cost in a short time given the flexibility it provides.

10.8.3 Matched-power-factor (Match-PF) LUT Function

The LV converter feeding the series transformer, draws a small portion of DAB current and the switches have either small turn-on or turn-off losses only. The DAB ZVS can be maintained with this extra circuit without deregulating the output voltage in proportion to the input voltage. Additionally the input to output N_v can be sensed and used to calculate optimum series-compensation angle for maintaining ZVS dynamically. The series converter can be operated with different d_c and θ_c under different loading conditions. It can also be short-circuited to emulate original DAB circuit or to cut-off core-losses when the series-compensation is undesirable. The controlled d_c helps to inject controlled V_c required for particular loading condition. The d_c and θ_c for a given load are selected from a LUT. The LUT is designed based on below criteria-

- The higher load PF is minimum for both main converters while keeping a defined minimum lagging current phase from primary with controlled lag series-compensation.
- The MV converter based on SiC IGBT/MOSFET, has higher turn-on losses and EMI issues, thus asks for a minimum lagging current phase.
- The defined minimum lagging phase current is maintained at lighter load with lead series-compensation since the ϕ' needs to be expanded for both main converters to be in ZVS.

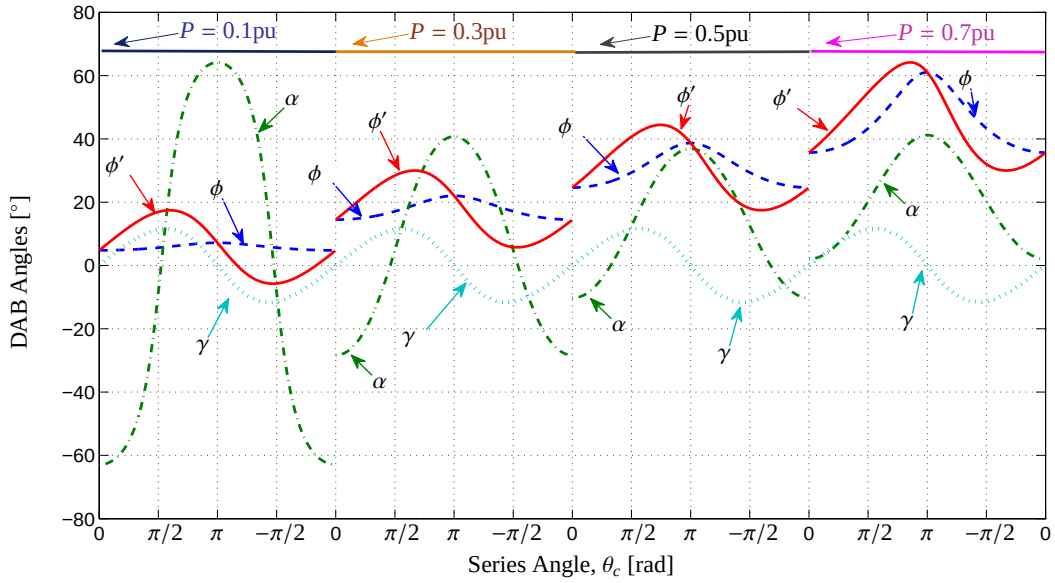


Figure 10.24: Series angle θ_c [rad] effect on vector diagram under different loads

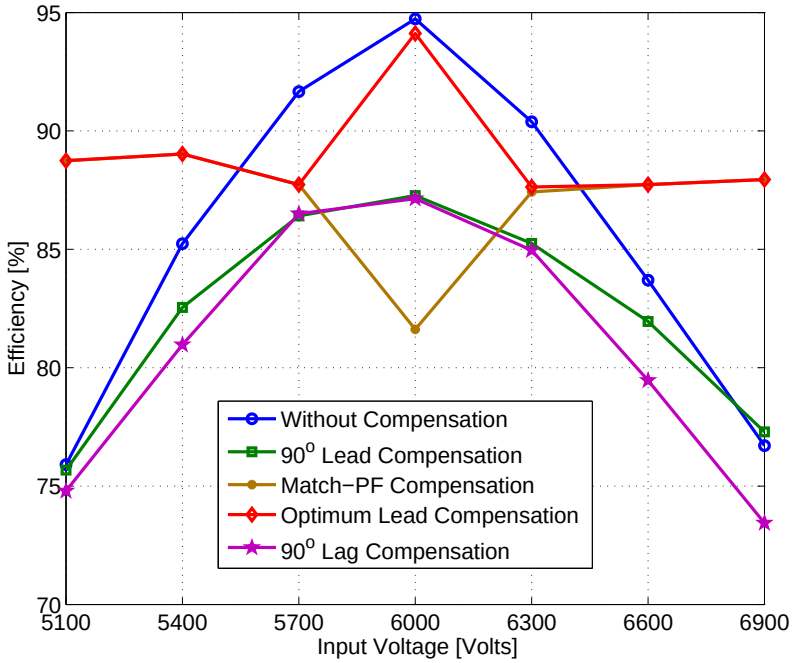
Fig. 10.24 shows plot of vector-diagram angles with the series-compensation angle θ_c under different loads. The current phase α is highly sensitive to the θ_c at lighter loads. The generalized ideal condition for ZVS is that current-vector should be in the middle of main converter voltage-vectors as in (10.6).

$$\alpha = \phi'/2 \tag{10.6}$$

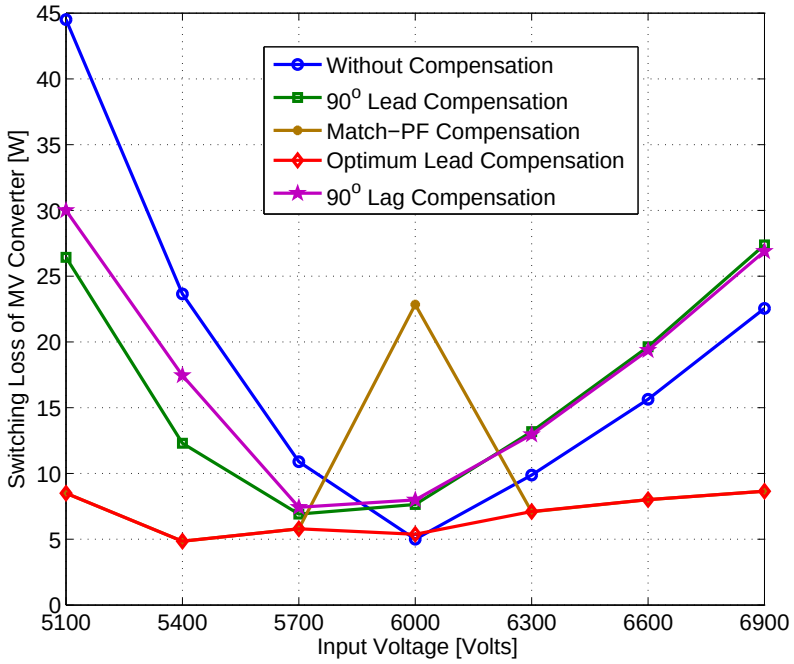
To meet this condition, a LUT of θ_c and d_c as function of loading, can be constructed known as Match-PF LUT. As shown in Fig. 10.24, there are two opposite polarity solutions for θ_c under all loading conditions of which one is suitable. The 20% N_c is roughly equivalent to ±30% of DAB angle 40° with the ϕ' it can create. The full-load can not be considered immediately at 30% load as the negative Q_c would make $\phi' = 0°$. Therefor light-load is considered below 40%. For less than 40% load, leading polarity is taken. And for more than 40% loading, lagging polarity is taken since it minimizes the reactive-power flow. The light-load DAB series-compensation requirement is reduced near nominal N_v. This is because the component required for voltage equalizing, is zero and the maximum ϕ' created is more than sufficient. Thus V_c can be reduced using series d_c control to cut-off additional series transformer core-loss. Since N_v affects the DAB ZVS behavior, N_v is taken into calculation of the optimum LUT which becomes two dimensional. The d_c of series-compensation voltage (V_c) can be varied to achieve different N_c as function of loading and N_v of the DAB. It helps not to add conduction and series transformer core loss in the DAB at light-load and nominal N_v.

10.9 Optimum Series Compensation of MV DAB

For a typical series-compensation added MV DAB system, Match-PF is a generalized optimum condition from ZVS perspective. But the optimum efficiency curve is dependent on specific module characteristics and parameters. For this calculation, a simulation study is presented with the real switching data of 15 kV SiC IGBT [41] and 1200 V SiC MOSFET [101] modules used in Transformer-less Intelligent Power Substation (TIPS) project [11]. The simulation parameters are earlier shown in Table 10.4. The DAB is simulated with mentioned parameters for following series-compensation control modes - (i) without compensation, (ii) 90° lead, (iii) Match-PF, (iv) optimum and (v) 90° lag compensation over ±10% dc N_v deviation. Fig. 10.25 shows light-load comparison curves of efficiency and corresponding total switching loss in the MV converter on different N_v. It can be seen that series-compensation is not efficient near nominal N_v ($N_v/N_t = 1$). The light-load efficiency drops due to additional series transformer core-loss. Also the increased conduction losses due to injected Q_c pulls it further down. Below certain lower input dc, ZVS is lost which results in EMI and higher magnitude turn-on loss in IGBTs. The Match-PF proves very effective in this mode. For certain higher input dc also, Match-PF is optimum. Fig. 10.26 shows full-load comparison curves of efficiency and corresponding total switching loss in the MV converter on different N_v. For lower input dc case, the Match-PF method tries to reduce V_r. In

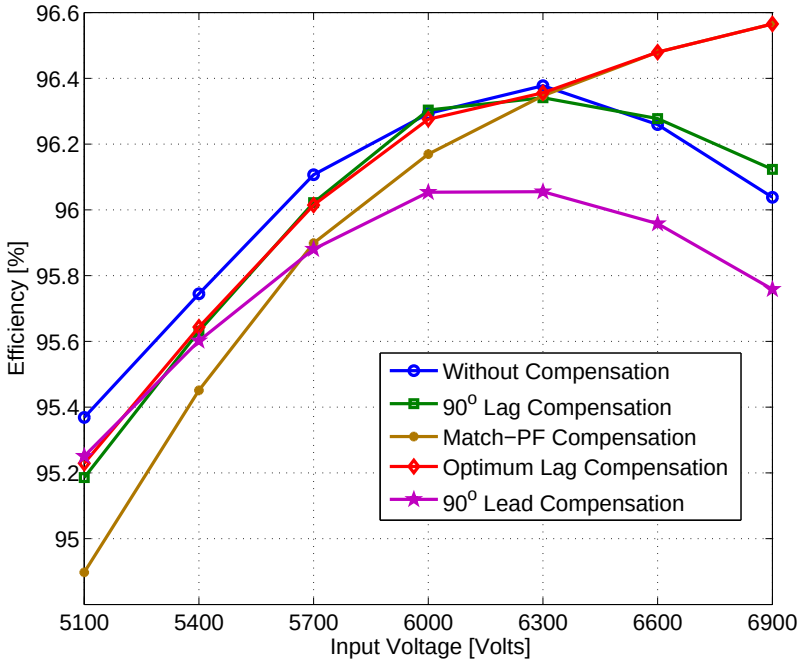


(a) Efficiency comparison on N_v variations

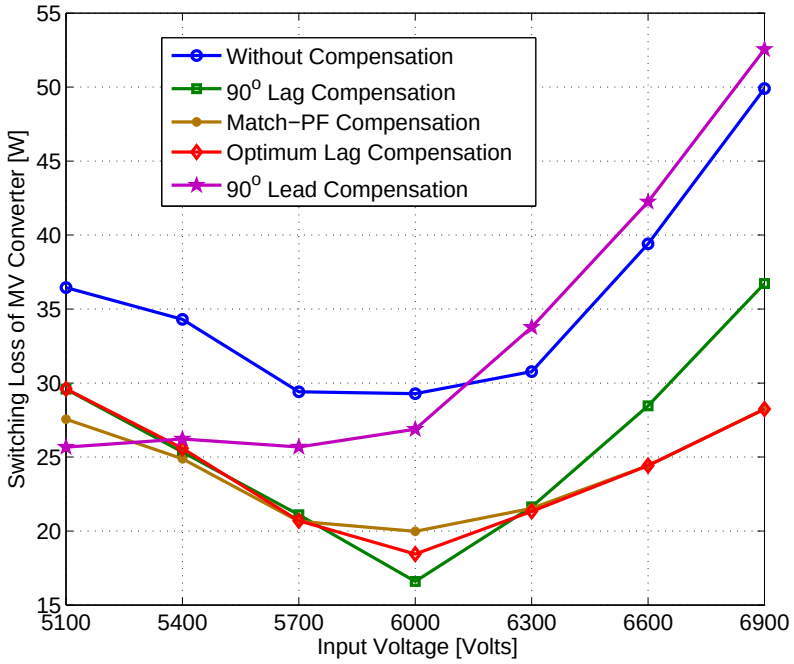


(b) Total switching loss of MV comparison on N_v variations

Figure 10.25: Comparison of DAB performance for different series-compensation under light-load

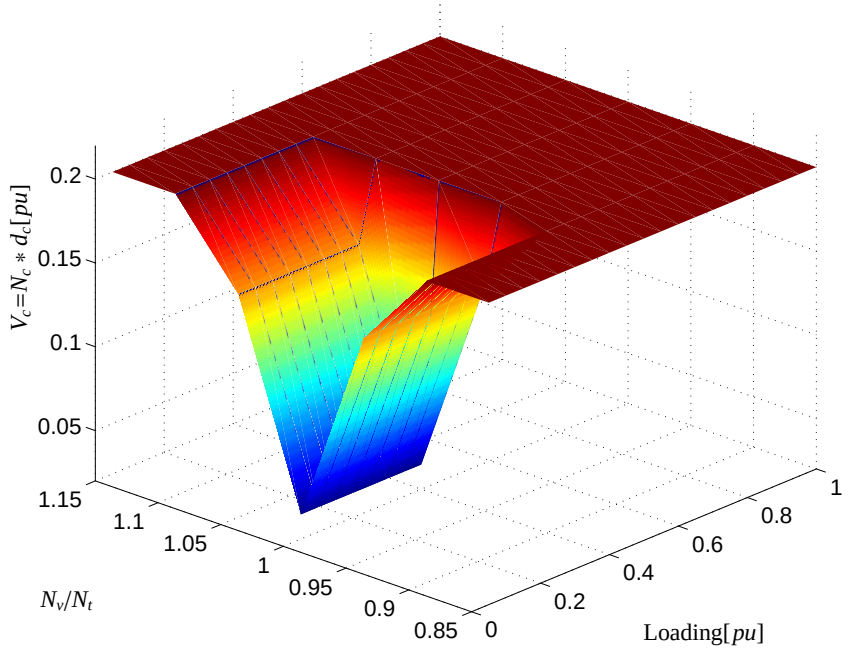


(a) Efficiency comparison on N_v variations

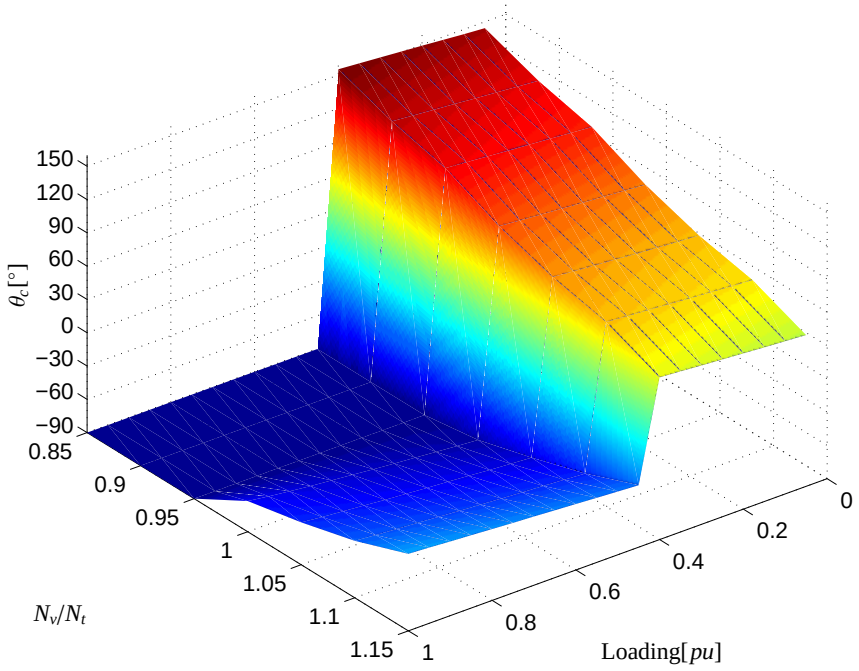


(b) Total switching loss of MV comparison on N_v variations

Figure 10.26: Comparison of DAB performance for different series-compensation under full load



(a) Desired series V_c using duty-ratio



(b) Desired series angle

Figure 10.27: Optimum 2-D look-up-table (LUT) as function of loading and N_v/N_t

this process, it increases the DAB ϕ' and reactive-power to support the same real-power. Thus, it results in lower efficiency in this range. As shown in Fig. 10.26(b), the fixed 90° lag phase series-compensation results in relatively lower total switching loss in the MV converter in this N_v region. This is because, it does not reduce V_r but still reduces ϕ'. The fixed 90° lead phase series-compensation results in more switching loss as Q_c injection is undesired at higher load. For higher input dc, the Match-PF is effective due to the reduction in reactive-power, conduction loss and turn-off loss.

The optimum LUT has been derived based on simulation trajectories for efficiency under different modes as previously shown in Fig. 10.25 and Fig. 10.26. Fig. 12.3 shows the d_c variation and the corresponding optimum θ_c as function of loading and N_v/N_t. The V_c must be used to the maximum when correcting PF at higher load. While it should be limited by d_c control near nominal N_v towards light-load. This produces smaller distortion in the DAB current and smaller conduction losses. The d_c reduction also limits the series transformer core-loss. Thus it depends on the N_v/N_t as well as the loading. As shown in Fig. 10.27(a), the V_c is 10% and 20% respectively at N_v deviation of 5% and 10% using d_c in light load region. The Match-PF is followed below 40% loading but using V_c also as a variable. Above 40% loading the θ_c is kept at 90° lag for N_v/N_t less than 1.0. This is because matching PF reduces V_r and decreases the maximum power capability. The current vector need not be in the middle of voltage vectors at wider ϕ'. For N_v/N_t more than 1.0, Match-PF is followed. Fig. 10.27(b) gives the recommended θ_c for using the series converter as function of d_c, loading and N_v/N_t. It results in series-compensation vector addition such that ZVS occurs with maximum efficiency for the DAB converter. It follows the optimum curves in Fig. 10.25 and Fig. 10.26.

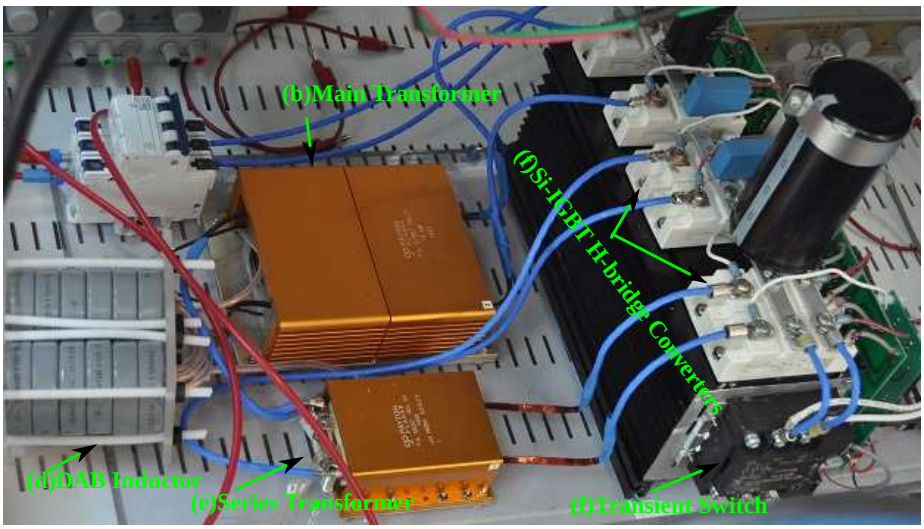


Figure 10.28: Photographs of 400 V series-compensation DAB setup

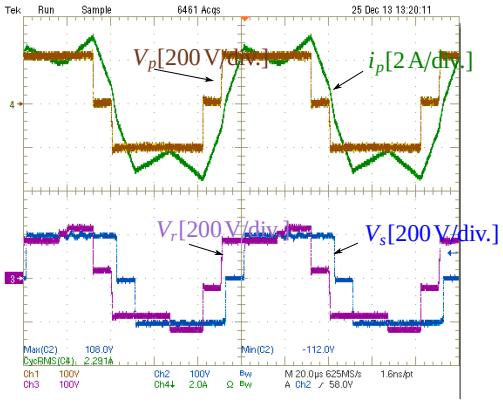


Figure 10.29: Experimental Results with 90° Lag Compensation

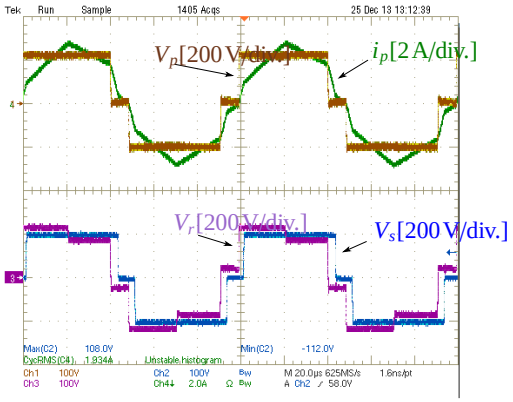


Figure 10.30: Experimental Results with 90° Lead Compensation

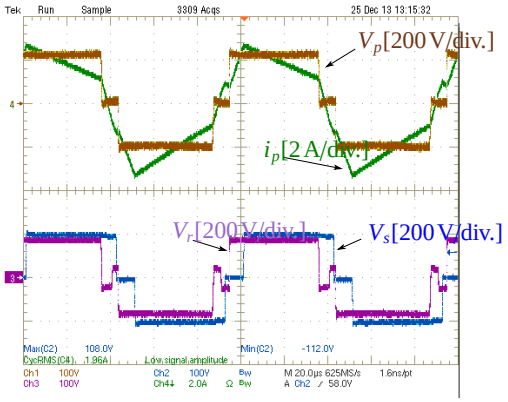


Figure 10.31: Experimental Result with 180° Phase Compensation

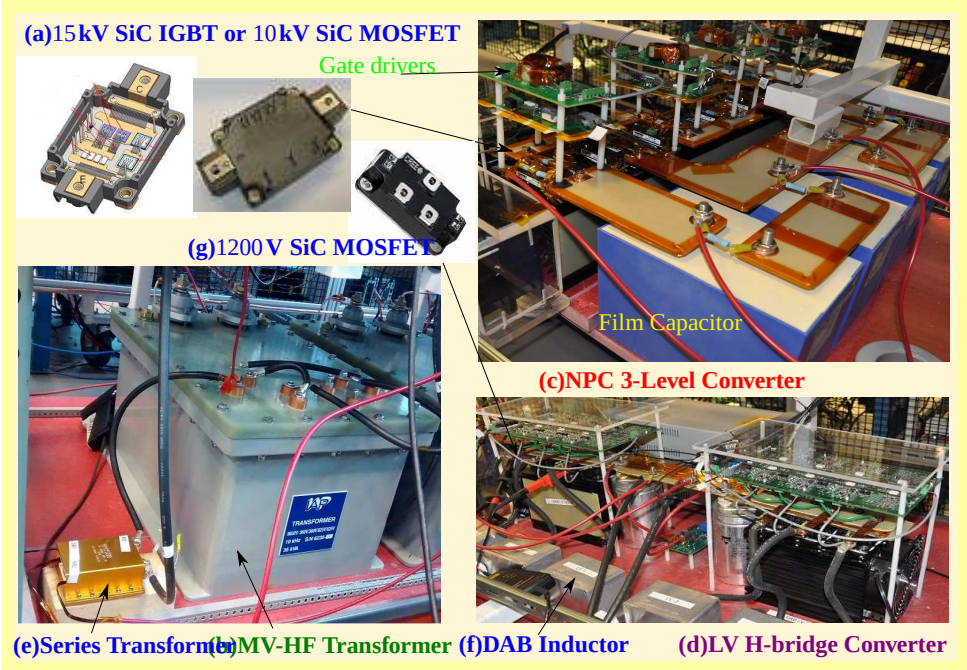


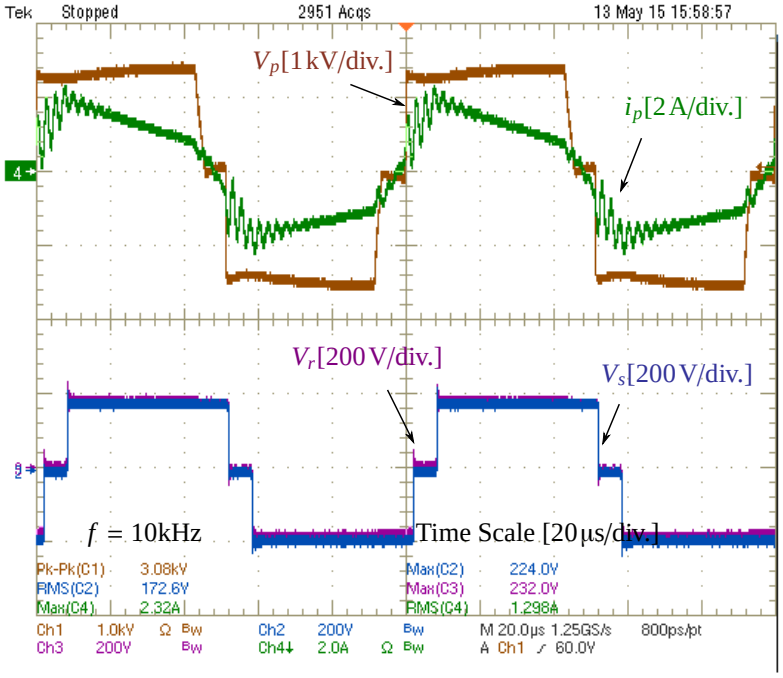
Figure 10.32: Photographs of 6kV series-compensation DAB setup

10.10 Experimental Validation

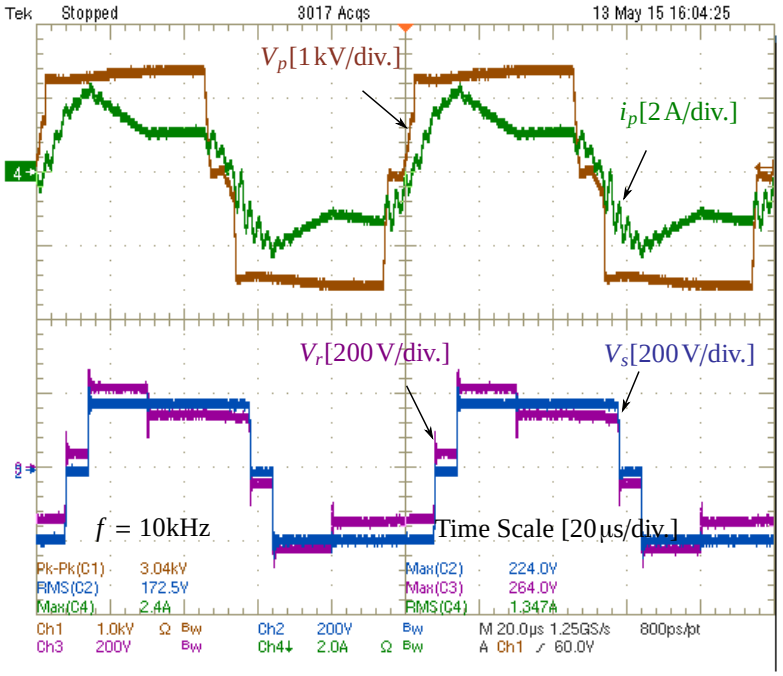
Prior to implementation in the MV setup a LV setup shown in Fig. 10.28, has been tested for series compensation technique. The results match to the simulation and has been presented in [118]. It shows Payton 1:1 10kW main transformer, series 5:1 2kW transformer, low parasitic inductor and h-bridge converters supplying the DAB as in the schematic shown in Fig. 10.2. Fig. 10.29 and Fig. 10.30 show the LV experimental waveforms for 90° lag and lead compensation respectively at 200V-100V, 400W DAHB operation. Fig. 10.31 shows the LV experimental waveforms for 180° compensation. As expected the primary converter voltage angle can be controlled without affecting the power flow which depends on the resultant vector phase. Hence the ZVS mode can be extended towards light load as well. The series transformer primary carries the same current flowing in the primary of the main transformer. But the voltage rating is 20% taken here. Hence the series transformer is rated at 20% power rating of the main transformer. The series transformer carries reactive power mainly when in ±90° compensation mode. The secondary of the series transformer is rated for same voltage as the secondary of the main transformer, but it carries smaller current.

The MV converter hardware are initially built using 15kV SiC IGBTs as MV devices for 3kV-150V, 10kHz DAB tests. Since the same copack module package with 20kV SiC JBS anti-parallel diode, open and closed photographs as shown in Fig. 10.32(a), is used to house both type MV devices, these modules are replaced with 10kV SiC MOSFETs for 6kV DAB tests. Fig. 10.32 shows the 6kV-270V, 10kHz

MV DAB hardware setup for series-compensation test with parameters shown in Table 10.4. It uses the TIPS MV-HF transformer shown in Fig. 10.32(b) rated at 35 kW [32]. A 4 kW rated series transformer shown in Fig. 10.32(e) is used for the compensation. The TIPS external inductor shown in Fig. 10.32(f) is also included in the setup as the leakage-inductance of the combined transformers is still small. The main transformer primary is fed with 3-L pole shown in Fig. 10.32(c) and main transformer secondary is fed with 2-L H-bridges as shown in Fig. 10.32(d). The series transformer is fed by another 2-L H-bridge connected on the same LV dc bus. This experiment validates the basic working of series-compensation for DAB at a load of 4 kW. A voltage feedback control maintains the output LV dc at 270 V, which feeds a fixed 22 Ω load resistance. The series converter phase θ_c is varied using an open-loop command. The V_p, V_r, V_s & I_p signals are probed under different series-compensation θ_c. Fig. 10.33 shows the experimental results without and with 110° lead series-compensation respectively. The without-series-compensation mode is equivalent to the conventional DAB operation. As in Fig. 10.33(a), the DAB seems to operate in buck mode and the loading is not enough that ZVS could happen. Also due to step voltage, dv/dt and parasitics interaction, there is ringing in the current. Both conditions cumulatively cause non-ZVS operation and higher dv/dt appears. In Fig. 10.33(b), the series-compensation is at 110° lead and the DAB is in ZVS. The dv/dt during switching is low. This effect is created by the two components of the series-compensation voltage vector. Fig. 10.34 shows 6 kV-270 V, 10 kHz DAB test using 10 kV SiC MOSFETs as MV device. The experimental results are shown for without and with 90° lead series-compensation respectively. The purpose of DAB test is to verify the series operation and effect on ZVS, so the device type is not important for this experiment. The DAB N_v is near nominal in Fig. 10.34(a) but due to ringing in the current, there is non-ZVS operation. As a result, the dv/dt during turn-on is high and the DAB is less efficient. With series-compensation at 90° lead as in Fig. 10.34(b), there is an improvement in the dv/dt but not sufficient to create full ZVS. This is attributed to the D less than 50% and the ringing. Fig. 10.35 shows the 0° and 180° phase addition that is equivalent to tap-change. As implied from Fig. 10.35(a), 0° series-compensation pulls N_v down and the MV converter is out of ZVS. It is reflected in the dv/dt and current ringing. In Fig. 10.35(b), the 180° phase causes opposite tap-change and pushes N_v up such that MV converter is in ZVS but LV converter nearly loses ZVS. But due to p.u. distribution of the series inductance and dv/dt, only the hard-switching MV converter generates ringing in transformer current and EMI. Thus the MV converter ZVS must be met but without over-increasing conduction losses. Fig. 10.36 shows the result for 90° lag series-compensation. As expected the MV converter is more into non-ZVS. This mode has to be applied at higher load and D near 50%. This mode reduces reactive-power and the conduction losses. Also the DAB current becomes smooth. But it is not desirable at light load. Fig. 10.37 shows the expanded view of the MV pole waveforms from 6 kV results for comparison. It can be noticed from positive current during bottom switch (S_4) turn-on and corresponding lower maximum dv/dt of 6 kV/μs in V_p for 180° series-compensation that full ZVS occurs compared to the other modes where partial or non-ZVS occurs with steeper dv/dt of 30 kV/μs. If lagging pole current is able to discharge the turning-on device parasitics through anti-parallel diode

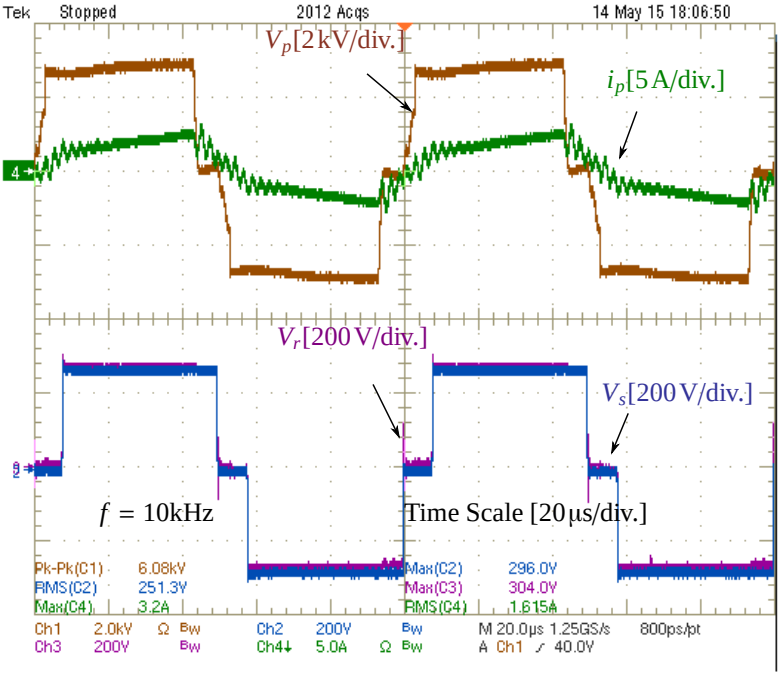


(a) No series-compensation

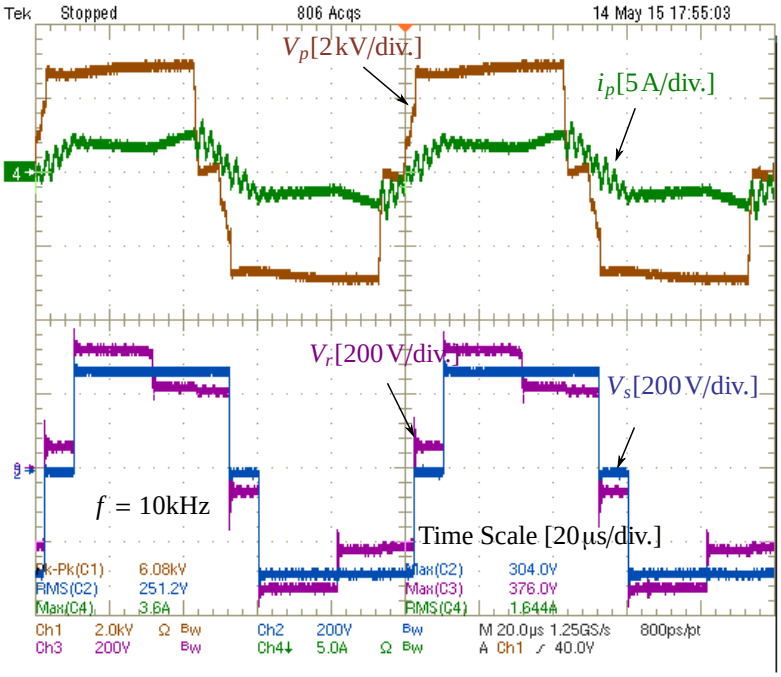


(b) 110° lead series-compensation

Figure 10.33: 15 kV IGBT based 3 kV-150 V, 10 kHz, 2 kW DAB results

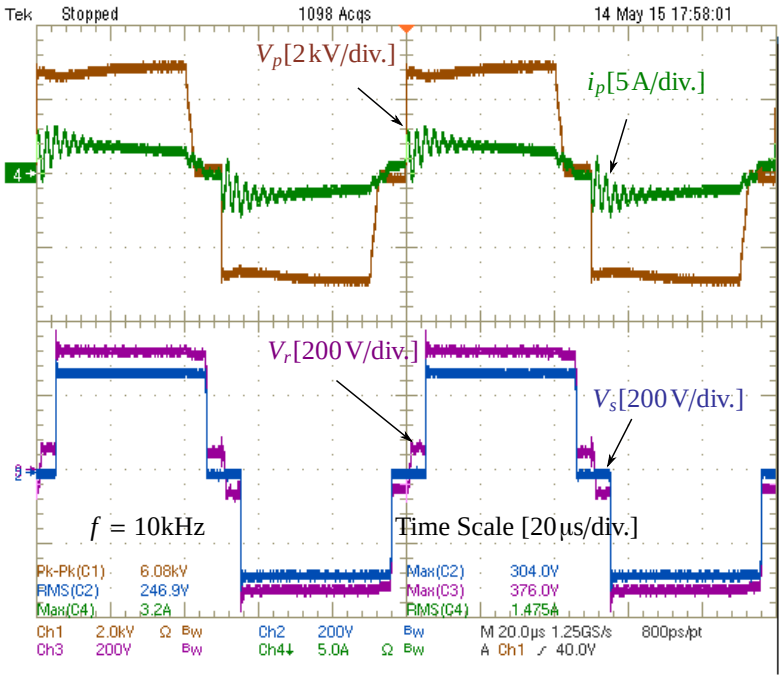


(a) Without series-compensation

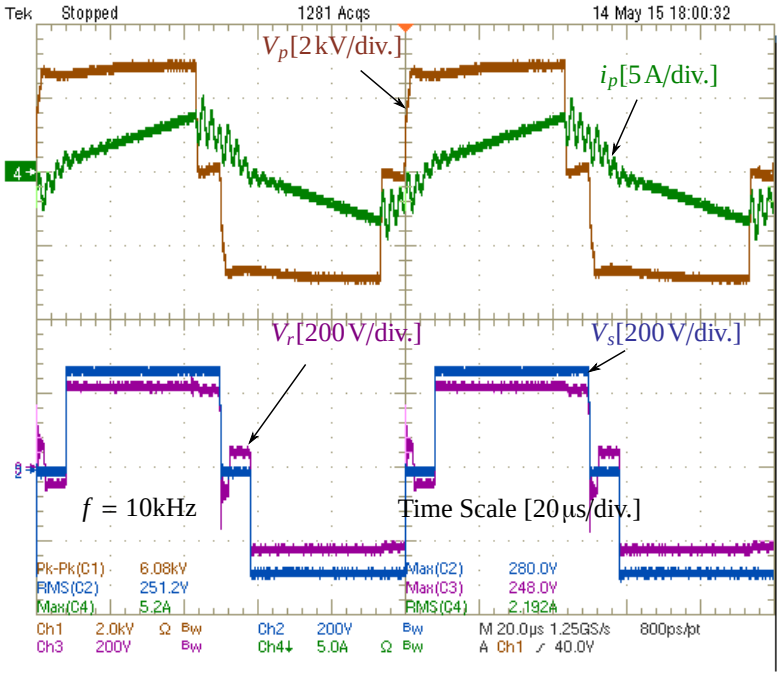


(b) 90° lead series-compensation

Figure 10.34: 10 kV MOSFET based 6 kV-270 V, 10 kHz,4 kW DAB results



(a) 0° series-compensation



(b) 180° series-compensation

Figure 10.35: 10 kV MOSFET based 6 kV-270 V, 10 kHz DAB results

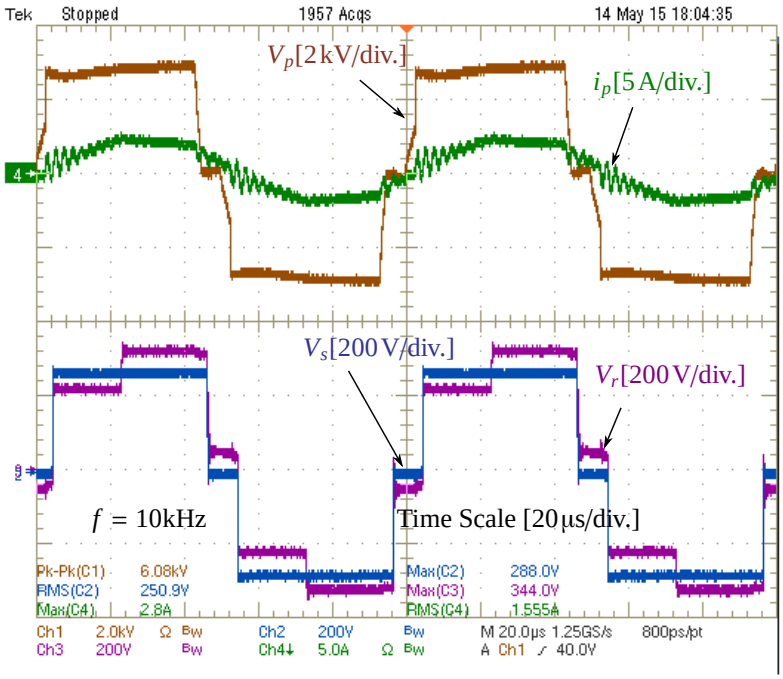


Figure 10.36: 10 kV MOSFET based 6 kV-270 V DAB results for 90° lag series-compensation

Table 10.6: Comparison between different modes

Parameter	**No Comp**	90° **lag**	180° **Comp**	0° **Comp**	90° **lead**
Power from MV converter (kW)	3.5854	3.5950	3.7712	3.5045	3.6012
Efficiency	92.42%	92.17%	87.87%	94.55%	92.01%
Maximum turn-on dv/dt **(kV/µs)**	30	30	6	30	30
Maximum turn-off dv/dt **(kV/µs)**	4.5	2.5	6	1.5	4

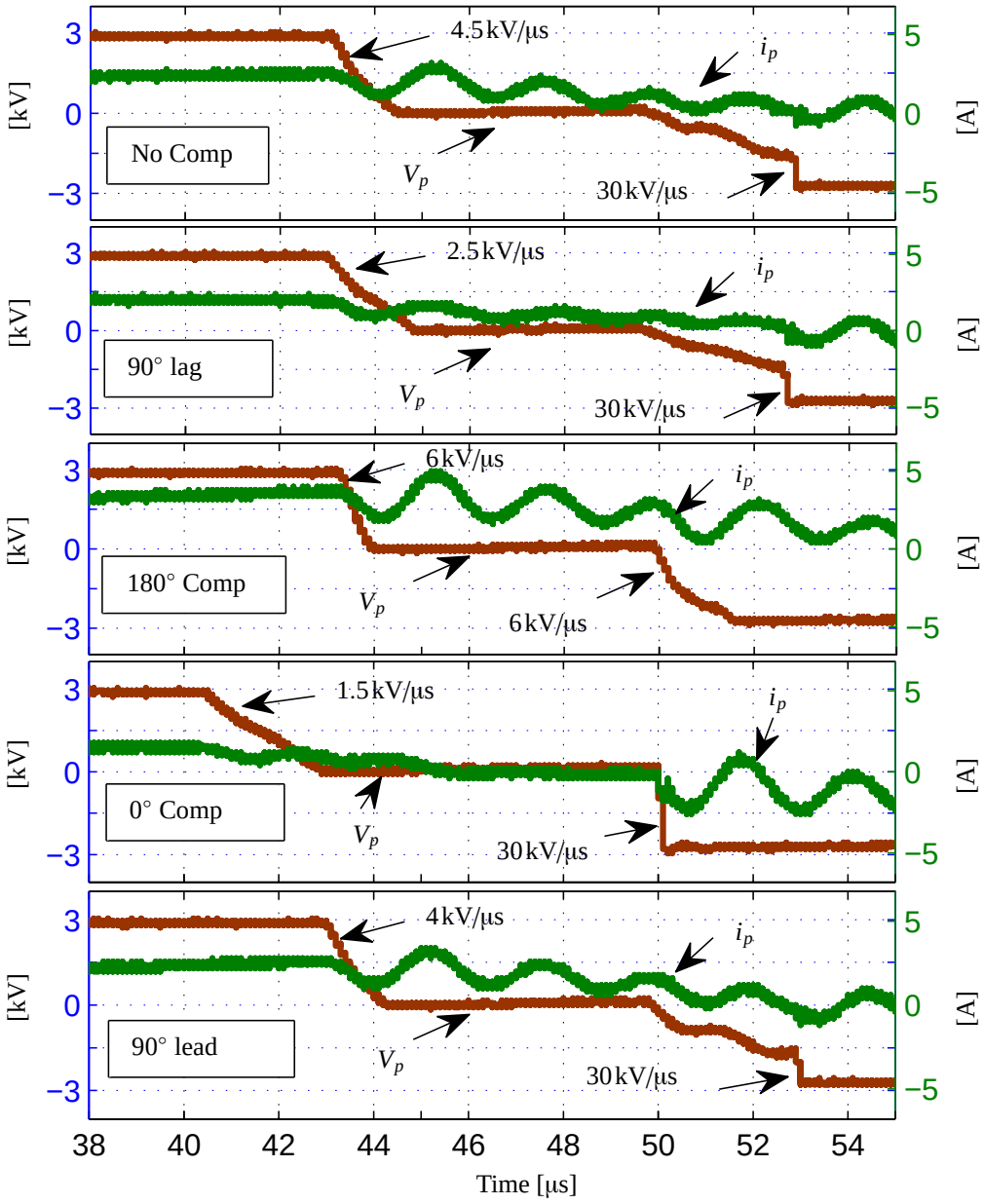


Figure 10.37: MV converter output, expanded near switching transitions under different modes from the experiments

before the dead-time ends, the turn-on is soft or ZVS. Compared to the hard-switching cases as in Fig. 6.10 resulting in positive energy-loss during turn-on, the switch $v - i$ energy is negative for 180° series-compensation. This implies that energy is not lost but stored in the parasitics coming out of the DAB series inductance and regenerated in next switching. If the turn-off current is high, the off dv/dt slope also becomes as high as 6 kV/μs but still much lower than the hard turn-on 30 kV/μs. Ideally the DAB three-level MV pole device on/off current should be such that both dv/dt slopes are low and the dead-time is designed accordingly. Table 10.6 shows the calculated power coming out of MV converters in the presented DAB results. It also shows efficiency for rest of the DAB system and MV pole dv/dt during turn-on and off. The MV DAB input dc current being very small at this high-voltage, it was difficult to measure the total DAB input power and MV converter associated power-loss. Estimating the MV converter losses using exact simulation is also beyond scope of this chapter. As discussed earlier, the load remains same as 3.31 kW for all cases. As expected, voltage-ratio correction with 0° Comp, results in highest efficiency at this load even with additional series component associated losses due to reduction of reactive power flow. The 180° Comp ensures MV ZVS but draws extra reactive power and therefore results in poor efficiency calculated without MV converter losses. It can also be noticed from Fig. 6.10, that 90° lead mode increases soft-switching parasitic discharging level towards zero without decreasing efficiency much compared to No Comp and 90° lag modes. At higher voltage and higher main converter duty-ratios, the benefits of this mode can be expected to be more visible. With series-compensation, DAB main converter voltage angle can be controlled without affecting real-power. These experiments support the claim that ZVS mode can be extended towards light-load under unregulated N_v.

10.11 Conclusion

The 15 kV SiC IGBT or same rating SiC MOSFET based MV converter powered DAB needs to maintain ZVS, since the hard-switching causes high dv/dt transitions at the converter output. This draws large surge current from devices at the turn-on instant and thus causes EMI & energy-loss as validated in DAHB experiments and earlier chapters. The quasi-square three-level NPC operation applies smoother step voltage on MV-HF transformer for good. The d-q transformation generates smoother and fast feed-back current as validated by experiments. The series addition of a phase controlled voltage to one of the main converters of a DAB, controls DAB current angle without change in the DAB dc voltages or the power level. This series-compensation can be used to maintain a small lagging PF on MV converter over wide load and voltage-ratio range. Thus by injecting additional controlled reactive power, it maintains ZVS even at light load and minimizes reactive power-flow at higher load against any voltage-ratio change. For saving isolation rating of the series transformer, this addition is done on the LV. The series transformer is fed from LV secondary to avoid extra MV switches. The series-compensation provides extra 10° virtual DAB-angle, therefore Match-PF is followed up to 16° (40% loading). It is possible to optimize series-compensation at higher loading also but only for buck-mode (high input) so that the

maximum power does not reduce. The series-duty is reduced when dc voltages are matched and the load angle is smaller than 15°. This saves the undesirable series transformer core-loss at the rated light-load condition and thus improves efficiency. As validated in the extensive simulations, for higher power DAB using HV SiC devices, this technique proves very effective without much addition to size, weight or cost. The experiments under different series modes shows that under ZVS enabled by one mode makes the dv/dt moderate. Also the power drawn from MV under different modes varies for the same output load. The MV converter switching loss being too small for the presented experiments, it is difficult to measure improvements, therefore it is only estimated using Matlab-Plecs simulation.

Chapter 11

Snubbered Light Load Full ZVS of a 15kV SiC IGBT Based DAB using Series Injection

11.1 Introduction

To maintain turn-on ZVS at light loads there should be sufficient current to discharge the parasitic before the dead-time ends. Three-phase DAB with smoother current near zero-crossings is more difficult to maintain ZVS compared to a single phase DAB with trapezoidal current [42]. There are good number of solutions proposed to solve light load DAB ZVS problem [105, 46, 81]. The general light load solutions may not be suitable for this MV DAB. A 15kV SiC IGBT being a research device has still challenges posed that need to be specifically solved due to the voltage magnitude and its characteristics. Above punch-through the parasitic capacitor reduces in 15kV SiC IGBT, this results in EMI and increased turn-off losses even if the turn-on ZVS is maintained [31]. If a snubber capacitor is used in parallel with IGBT for solution, the turn-on ZVS is more difficult to achieve as the light load current needed during turn-off of the complementary switch to discharge the added capacitor within dead-time, is high [42]. This problem discourages snubber solution for 15kV SiC IGBT based DAB since non-ZVS turn-on will abruptly short circuit the snubber capacitor and damage the devices. A series compensated DAB for optimum ZVS control in wide load and voltage range is proposed in [118]. The control approach in that chapter is to keep DAB current fundamental vector in middle of voltage vectors. The objective is to maintain ZVS at light load even in presence of significant voltage deviation. This chapter uses the same topology to solve above mentioned problem for a snubbered 15kV SiC IGBT based MV topology but presents a different objective and control approach. Also the series transformer turn-ratio is different here as higher depth of compensation is required to be able to induce a high current with small series duty-ratio. Since a high turn-off current is required in DAB MV pole such as to freewheel and discharge

the turning on device & snubber capacitor, the series circuit only adds a suitable polarity triangular current independent of loading. It is not used voltage-ratio correction here as presented in the previous chapter.

This chapter presents the series injection enabled snubbered 15 kV SiC IGBT MV converter powered full ZVS DAHB converter topology and operation. The Matlab-Plecs simulations are also presented at rated condition. A simple parameter selection for series circuit based on simulations is presented. The series injection ensures the ZVS turn-on in all loading conditions by generating sufficient negative freewheeling current as required by the added device capacitance, independent of DAB voltage-ratio and loading. The snubber capacitor makes the IGBT turn-off soft without slowing the device using gate-resistance. The energy stored in the capacitor during turn-off is regenerated into DAB during next turn-on [123]. Thus this topology is fully soft-switched especially for MV side under all conditions. The 15 kV SiC IGBT based MV half bridge experimental results and thermal measurements highlighting the effect of snubber, are presented. The 3 kV-160 V experimental results for series compensated 15 kV SiC IGBT based DAHB to enable the snubbered operation are presented in this chapter.

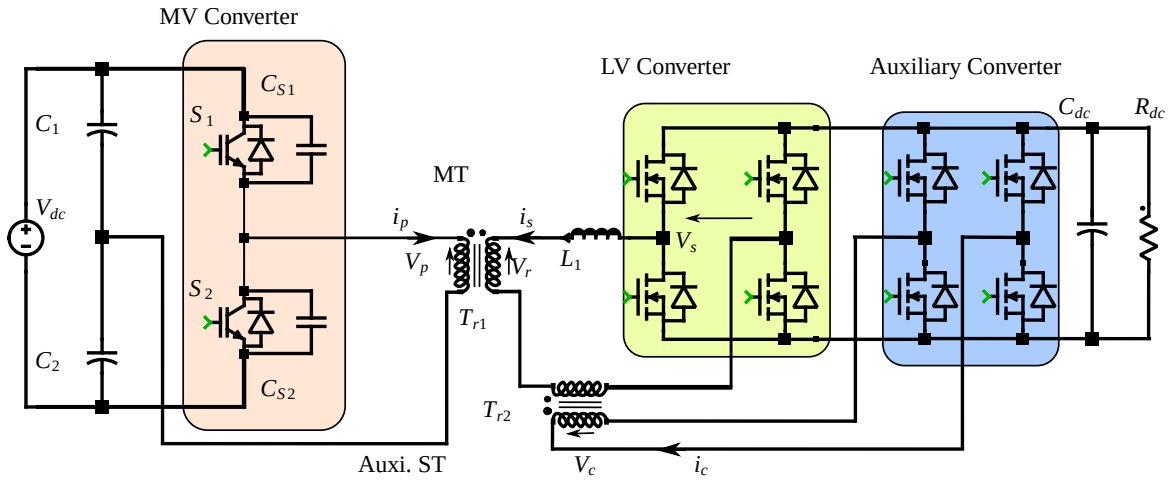


Figure 11.1: Schematic of series enabled full ZVS DAB

11.2 Series Enabled Full ZVS DAHB Topology

As shown in Fig. 11.1, a two-level half-bridge based on 15 kV/40A SiC-IGBT, is connected to the MV side of a medium-frequency (MF) DAB transformer operating at 10 kHz [118]. A 1200 V SiC-MOSFET based two-level H-bridge is connected to the low voltage (LV) side of the transformer. A series transformer rated for lower secondary voltage and power, injects a controlled voltage pulse in

Table 11.1: Rated parameters of MV simulation and MV DABC setup

Parameters	**MV Hardware & Simulation Value[Units]**
Input dc Voltage[V_{dc}]	6 kV
Output dc Voltage[V_o]	300 V
External Inductance[L_1]	80 μH, 0.2 Ω
Snubbers C_{s1}, C_{s2}	0.55 nF
T_{r1} Turns-ratio	10 : 1
T_{r1} Leakage Inductance (LV side)	8 μH, 13 mΩ
T_{r1} Mutual Inductance (MV side)	293 mH
T_{r1} Shunt Cap (MV side)	250 pF
T_{r2} Turns-ratio	1 : 1
T_{r2} Leakage Inductance	23 μH, 8 mΩ
T_{r2} Mutual Inductance	22 mH
C_{dc}	10000 μF
Rated R_{dc}	20 Ω
C_1, C_2	120 μF
Real Power Transfer	5 kW
T_{r1} Core Loss	50 W
T_{r2} Core Loss	20 W
Switching-frequency	10 kHz

series of the secondary DAB circuit as shown in Fig. 11.1. This series transformer is excited by an additional LV H-bridge composed of low current rating devices. Fig. 6.2(a) and Fig. 6.2(b) show the

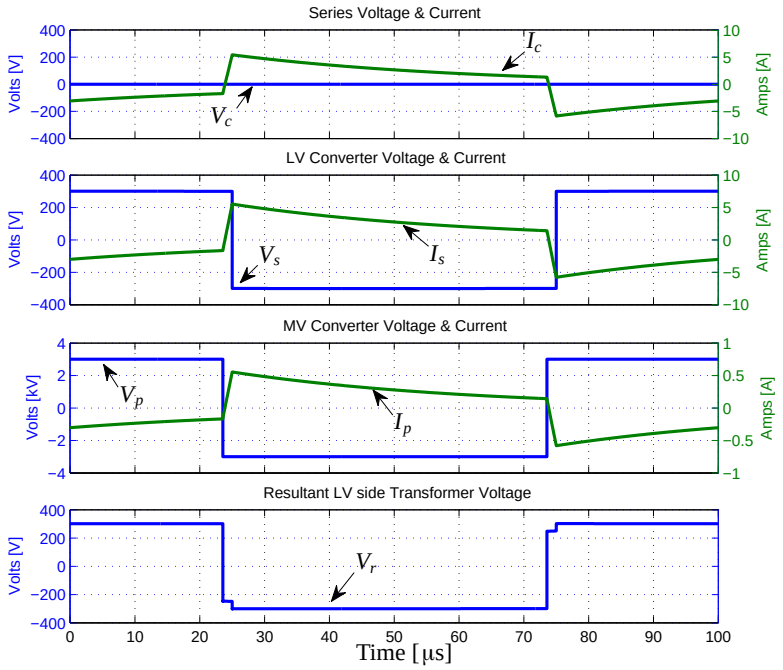


Figure 11.2: Simulation at light load without series injection or snubber

Double Pulse (DP) test results on the 15kV/40A SiC IGBT co-pack module during turn-on and turn-off respectively. The gate resistances are selected such that the below punch-through dv/dt is limited to a practical value for EMI consideration. The snubber slows dv/dt throughout without active gating and without resulting in increased losses [123]. With DAB switching frequency at 10kHz and given dv/dt, the dead-time is selected as 3.8μs. The parameters of this presented MV topology and its hardware are shown in Table 11.1 [42]. Fig. 11.2 shows the ideal DAHB simulation for light load. The phase lead of primary MV converter voltage w.r.t secondary voltage causes power flow to maintain LV dc bus. Fig. 11.3 shows the DAHB simulation considering converter dead-times for light load. This is approximate MATLAB/PLECS simulation without considering device parasitics. But a realistic notch in MV voltage can be seen that occurs as there is not enough lagging current for freewheeling and maintaining zero voltage across the turning on device. The series voltage pulse with certain duty-ratio when added near zero phase of the primary, generates a triangular freewheeling current as shown in the simulation result in Fig. 11.4. Since the turn-on ZVS is now enforced, a snubber capacitor is used in this simulation resulting in slower dv/dt loss-less transitions. There is no considerable loss associated with the series circuit as it only conducts for small duration. It is excited from LV side with either a half

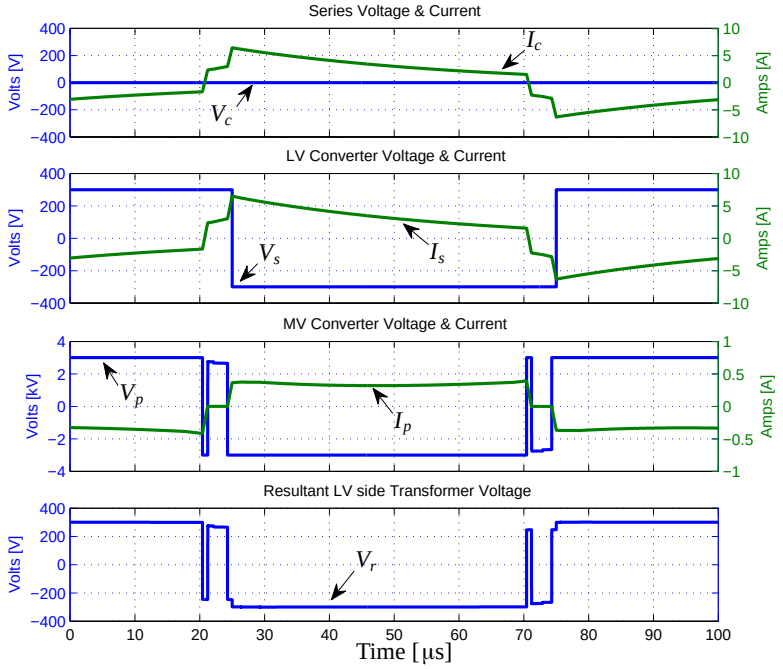


Figure 11.3: Simulation at light load without series injection or snubber but with dead-time

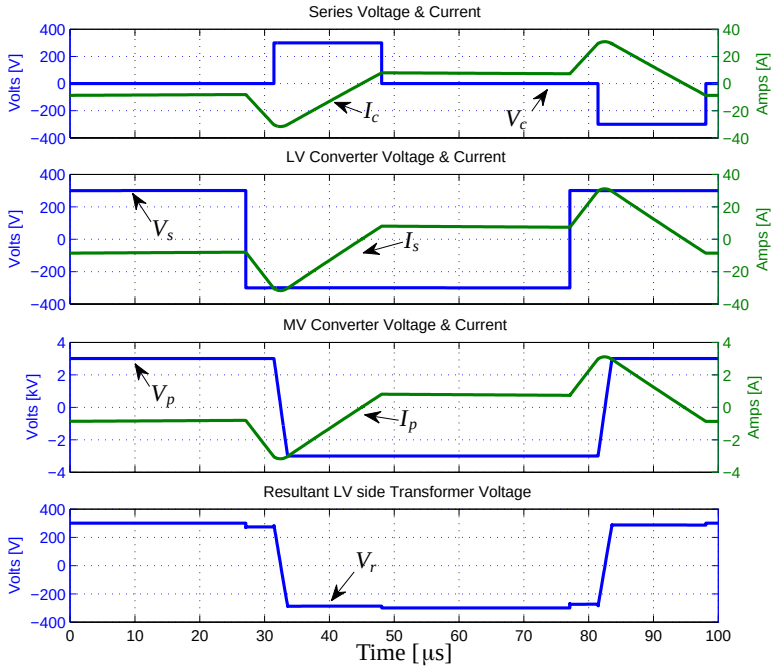


Figure 11.4: Simulation at light load with full ZVS

bridge or full fridge depending on output dc capacitor configurations and series size-weight constraints. The DAB LV converter might lose ZVS due to the injection but it is acceptable as it does not result in considerable loss addition or EMI. Since the DAB inductors are rated for full load current, there is no problem posed by the triangular current peak in the original design.

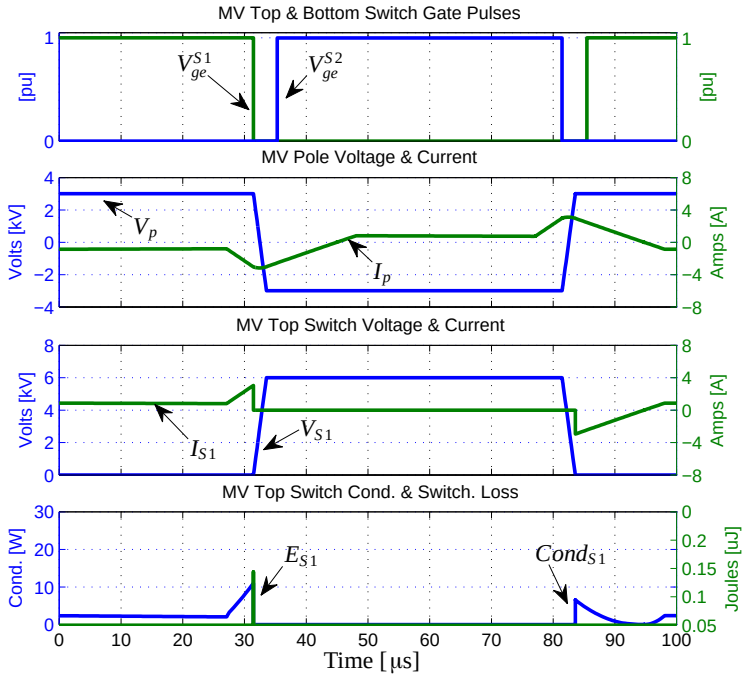


Figure 11.5: MV side simulation at light load with full ZVS compensation

11.3 Design Parameters

To design the series transformer turn-ratio and pulse duty-ratio, the snubber capacitor, maximum discharge time, maximum current and DAB inductance parameters are taken into account. As shown in (11.1), there is a minimum peak current requirement for a given snubber capacitor value across the MV switches for ZVS and loss-less operation. Also in (11.2), dependence of this current achieved through this method on the series duty-ratio is shown. The symbols are described in Table 11.2. The peak current during turn-off instant is dependent on the DAB loading and a series induced value. This induced value is effective more at light load when DAB contributed current is small.

$$t_d > C_s^* V_{dc} / I_p \tag{11.1}$$

Table 11.2: Symbols used

Parameters	Symbol
Ser. Tra. Turns	N_s
Peak MV Current	I_p
MV dc bus	V_{dc}
Series duty	D_s
DAB Inductance	L_d
Dead-time	t_d
Tot. Snubber Cap.	C_s^*

$$I_p = I_d + D_s V_{lv}/[L_d N_s f_s] \tag{11.2}$$

Fig. 11.5 shows the simulation of MV switch waveforms considering the snubber for the 15kV/40A SiC IGBT co-pack at light load with series injection. Fig. 11.6 shows the waveforms without series injection and without any snubber. In practice there is always some parasitic capacitor that may not discharge in regenerative manner, resulting in loss during turn on at light load. Fig. 11.7 shows the DAB LV switch waveforms for light load and with full ZVS topology. It can be seen that ZVS is lost but as mentioned earlier it has no considerable disadvantage. For just MV side ZVS the LV dc bus could have been decreased at light load, but this results in reactive current in the DAB generating conduction losses. The overall efficiency of this full ZVS topology is expected to be highest.

11.4 Experimental Results

Fig. 11.8 shows the MV experimental setup for the MV topology with parameters shown in Table 11.1. It shows the topology components such as series transformer, main transformer, MV half-bridge & LV converters and the DAB external inductor. For showing the benefit of snubber in terms of turn-off loss and dv/dt reduction for these IGBTs, the half-bridge is run with stand-alone inductive load to create high current for turn-on ZVS [123]. Fig. 11.9 shows the experimental result for an inductively loaded 15kV SiC IGBT based half-bridge at 7kV dc operation without snubber capacitor [123]. Fig. 11.10 shows the expanded view of the same result in same condition. It can be seen that dv/dt is 14.6kV/µs after the punch-through [123]. Fig. 11.11 shows the result in same condition but with snubber of 1.1nF [123]. The dv/dt is 2.7kV/µs as desired. Also the temperature recorded after 20 min heat run test is found to be lower on the same heat-sink point as shown in thermal photograph in Fig. 11.12 [123]. This indicates that losses due to turn-off switching have reduced. Here the turn-on ZVS was created for both tests by inductive load to achieve the required peak-current during turn-off instant. Thus the loss in snubber case is contributed mainly by conduction and the final turn-off loss is very small. For a non-compensated

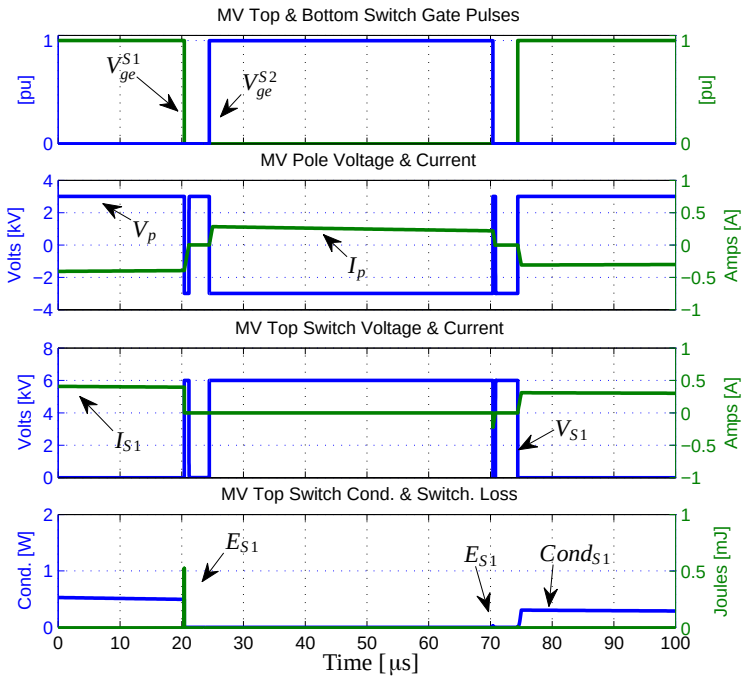


Figure 11.6: MV side simulation at light load without snubber or series compensation

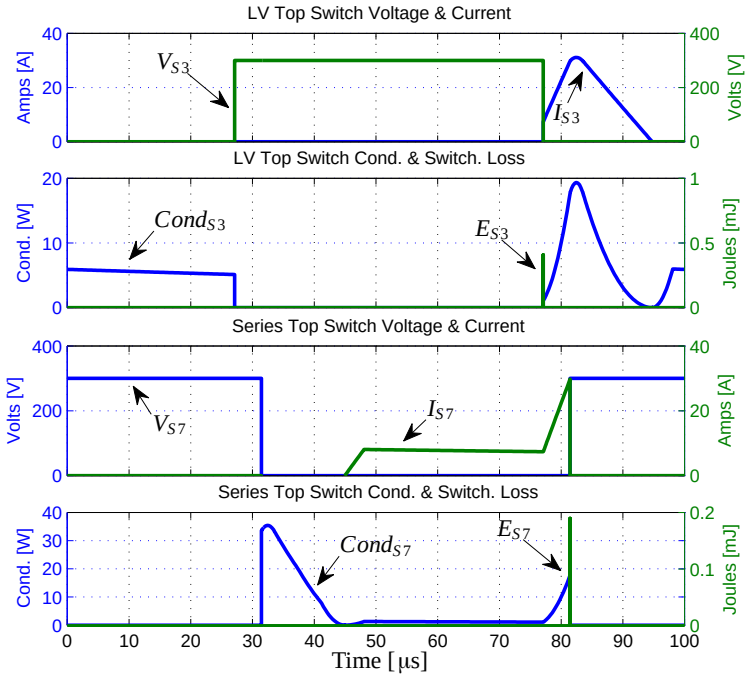


Figure 11.7: LV side simulation at light load with full zvs compensation circuit

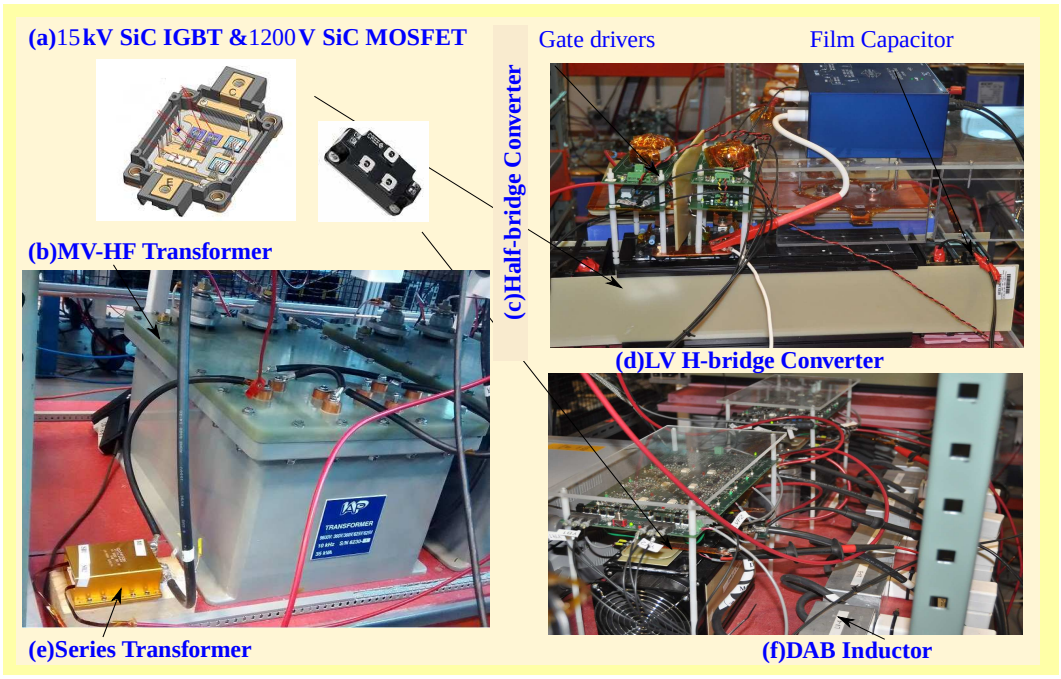


Figure 11.8: Photograph of 6kV MV DAHB setup for the ZVS test

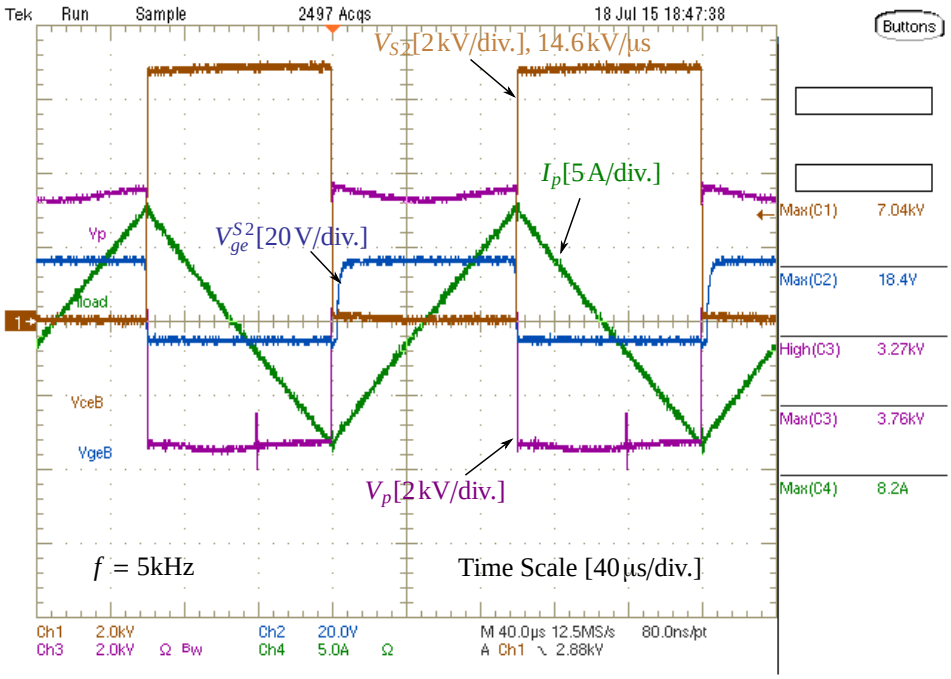


Figure 11.9: 15kV SiC IGBT 7kV half-bridge without snubber

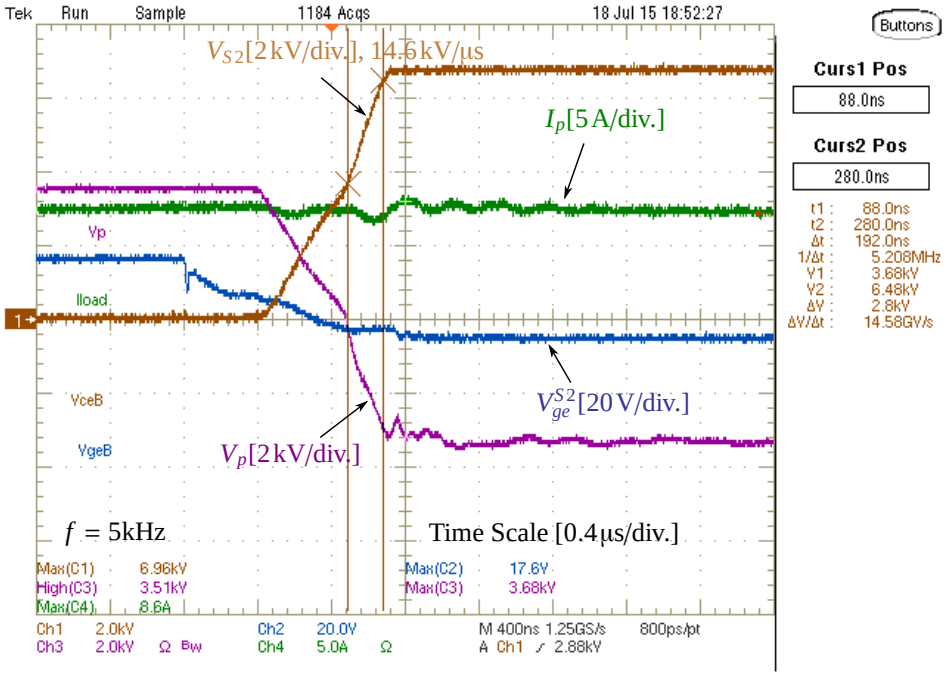


Figure 11.10: Expanded 7 kV half-bridge result without snubber

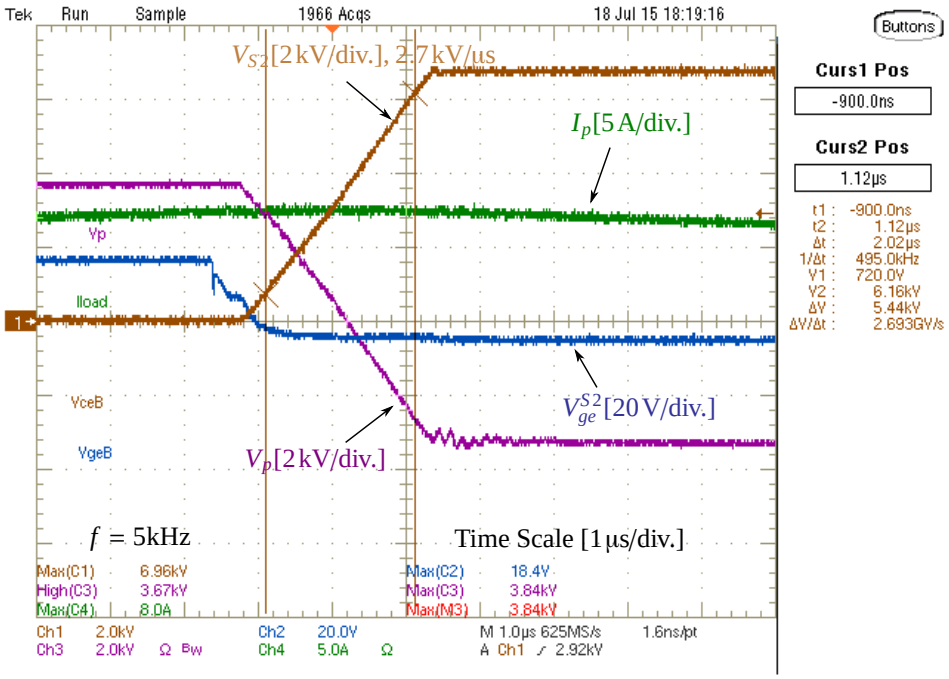
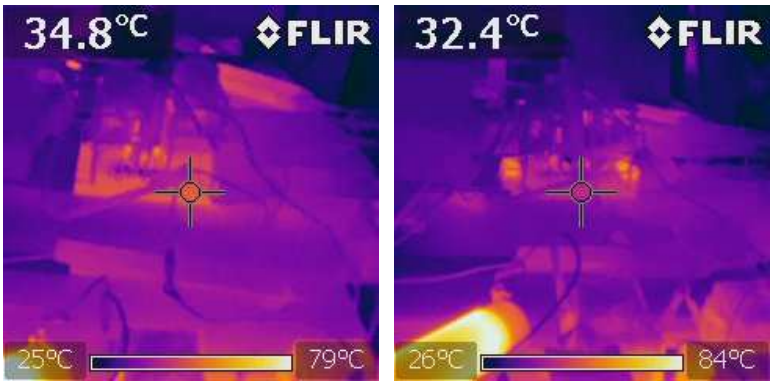


Figure 11.11: Expanded 7 kV half-bridge result with 1.1 nF snubber



a) No snubber b) With snubber

Figure 11.12: 20min thermal runs without & with full ZVS

MV DAB, there might be turn-on loss as well due to loss of ZVS at light load since there is always significant device capacitance to discharge. For implementing snubber in the DAHB, the inductive load is replaced by the DAHB transformer connected with secondary and series converter. Fig. 11.13 shows the 3kV DAHB experimental result without snubber or series compensation. Fig. 11.14 shows the the same result without snubber but with series compensation using $5:1$ N_s series transformer and 16.7% duty. Fig. 11.15 shows the the same result but with series compensation using $1:1$ N_s series transformer. Now the series duty is kept 8.3% compared to the simulations as this provides sufficient peak triangular current. Fig. 11.16 shows the the same result with 150pF snubber and series compensation using $1:1$ N_s series transformer. It can be seen there is dv/dt reduction in the pole voltage but the turning-on device voltage reduces to zero before the dead-time ends. This mode of operation also corresponds to maximum efficiency. But the overall loss is not measured in this chapter to verify it. Fig. 11.17 shows the comparison of dv/dt for half-bridge voltage and current for Fig. 11.15 and Fig. 11.16 cases. It can be seen that there are slower dv/dt near zero pole voltage in middle of higher dv/dt transitions. After using the snubber, the difference between two dv/dt's is brought down but the total discharge time increases. This implies that it may be happening due to non-linear device capacitance. The energy stored in snubber is regenerated in the next discharge cycle. Thus the snubber decreases EMI together with the turn-off losses.

11.5 Conclusion

15kV SiC IGBT based simple DAB topology is very promising for high power and medium-voltage application. The snubber capacitor addition improves the EMI and turn-off losses of the MV device above punch-through level. The half-bridge inductive loading experiments show drop in MV converter heatsink temperature after inserting snubbers across 15kV SiC IGBT. The problem of turn-on ZVS loss

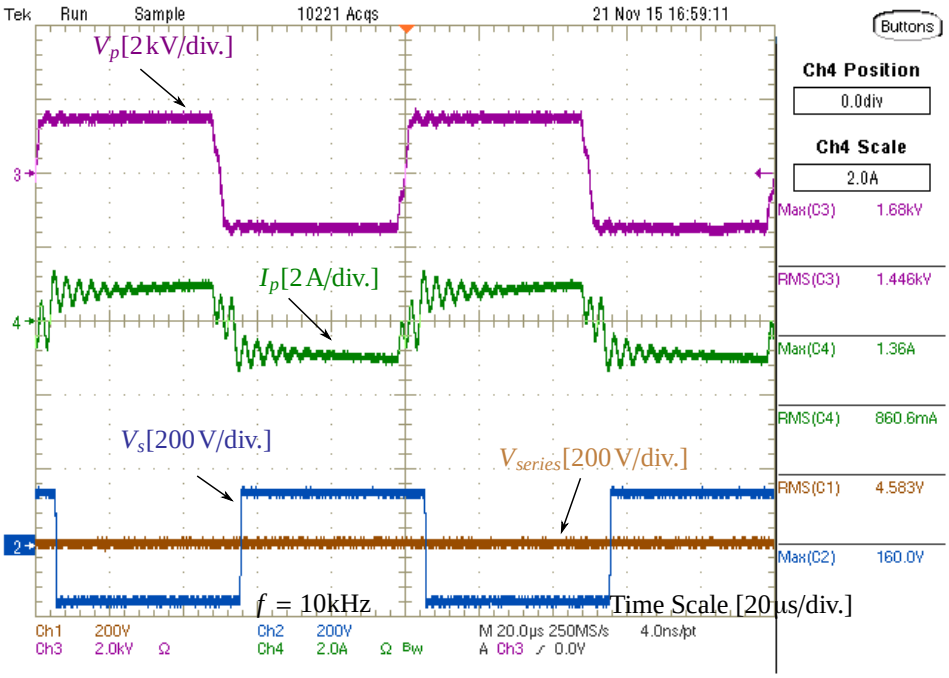


Figure 11.13: 3 kV DAHB operation without series addition or snubber

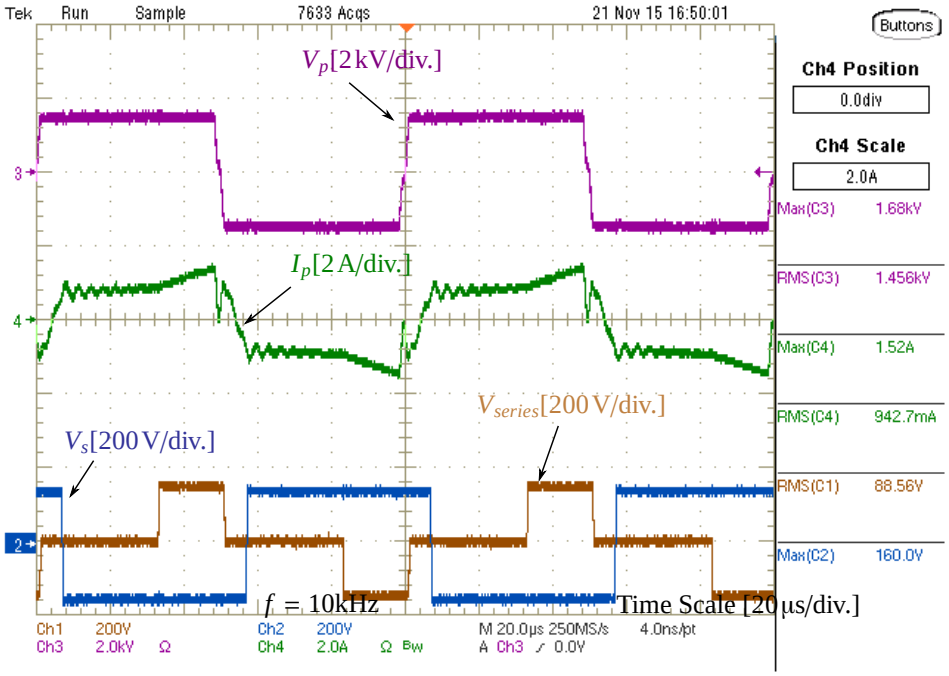


Figure 11.14: 3 kV DAHB operation without snubber with 5 : 1 N_s

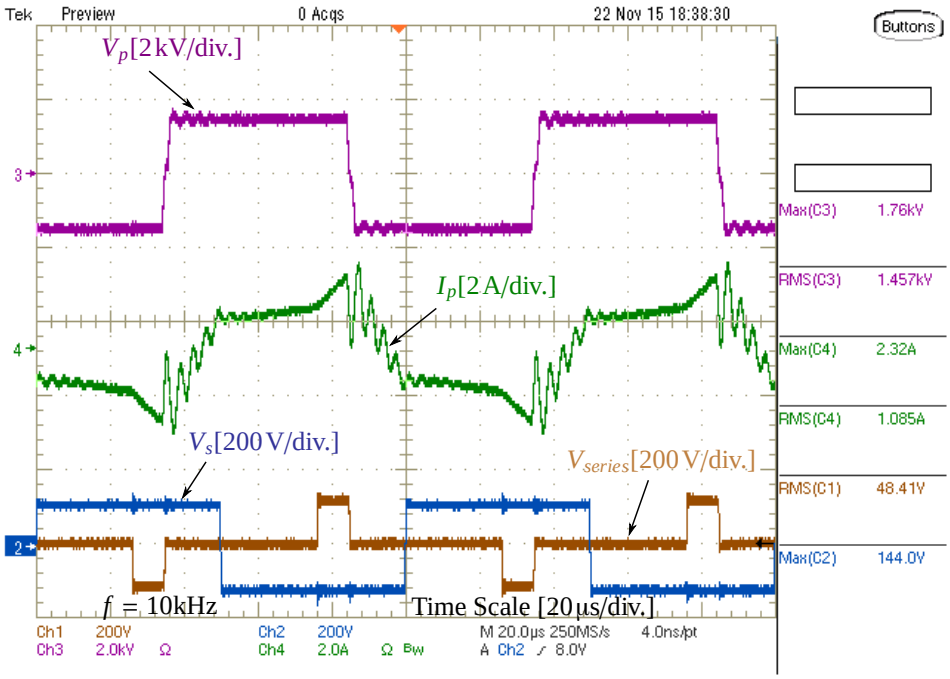


Figure 11.15: 3 kV DAHB operation without snubber with 1 : 1 N_s

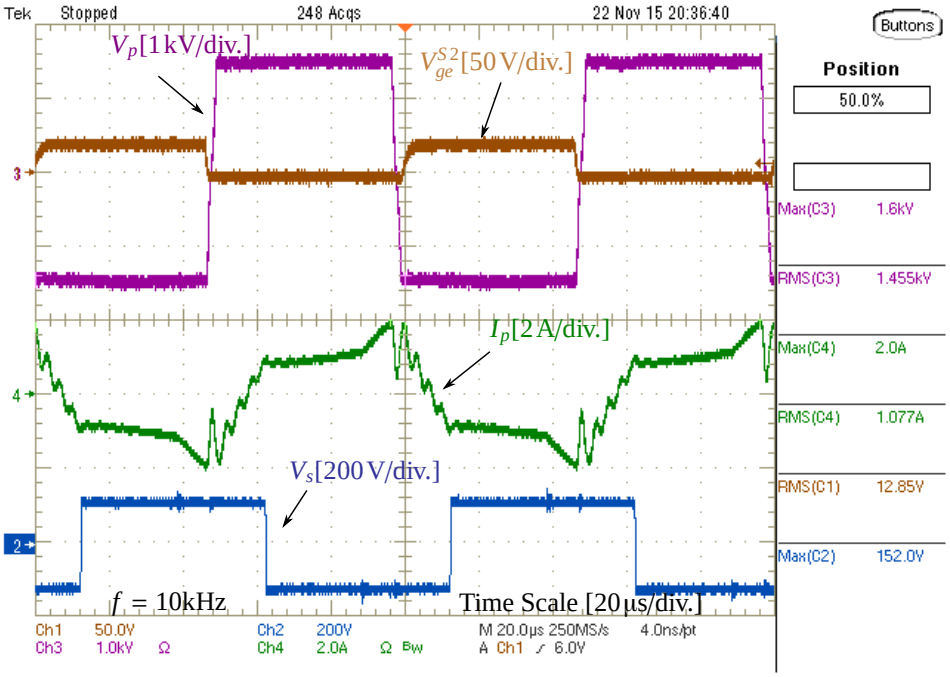


Figure 11.16: 3 kV DAHB operation with 150 pF snubber and 1 : 1 N_s

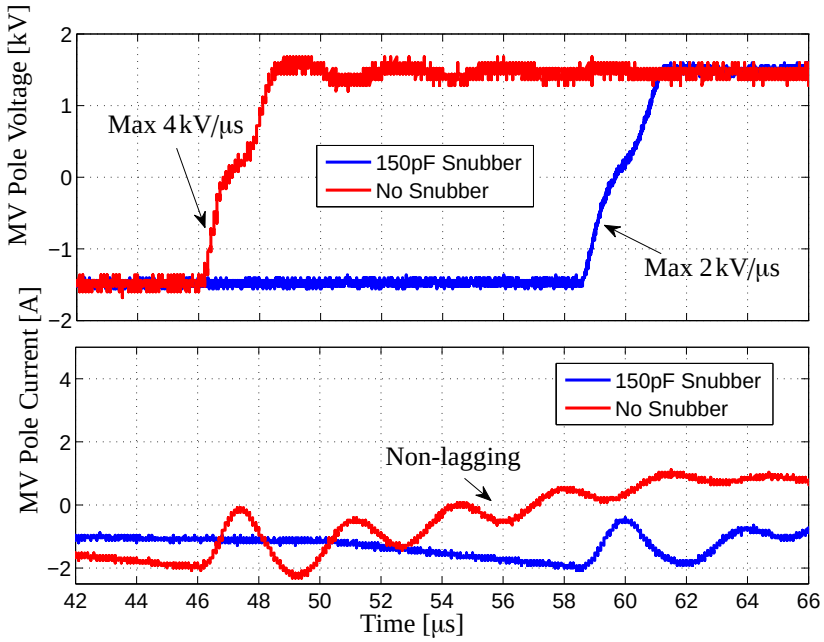


Figure 11.17: Experimental dv/dt comparison between with and without snubber

due to added device capacitance, especially at light load, is solved by the presented series injection as validated by presented simulations. A simple lower power series circuit consisting of a fractional rating LV transformer and low current LV switches, is utilized to shape the current near zero-crossing to meet the turn-on ZVS criteria. As presented in the 3kV-160V experimental results, the injection makes this DAB topology fully soft-switched generating low EMI and switching losses.

Chapter 12

A MV Intelligent Gate Driver for ZVS Enforcement and Advanced Protections

12.1 Introduction

This chapter first presents the basic block diagram highlighting the intelligent gate-driving features. The purpose of the intelligence addition is generally optimization in terms of the switching loss and the EMI by active-gating. These parameters for a DAB are dependent on ZVS operation unlike the AFEC hard-switching converter. The ZVS in the MV DAB can be ensured by optically transmitting the value of negative switch current at the turn-off instant and also the phase information of the current to main DAB controller. The main controller then utilizes one of the ZVS enforcement methods discussed earlier in the dissertation to calibrate the operating point accordingly to ensure ZVS, maximum efficiency and lower EMI emission. It also helps for matched series/parallel operation of the devices for scalability [124, 125]. This chapter presents high side intelligent MV gate-driver (IMGD) qualification results with sensing of I_d, $V_{ds}(on)$ and T_{mod} device conditions. The digital implementation and programming are also presented. Due to criticality of application and high stress on the device, it is important to acquire operating data from the device under test for diagnosis or predicting failure beforehand. Some of these functions have been previously implemented for low-voltage Si devices [126, 127, 128]. However this EMI hardened Intelligent MV Gate Driver (IMGD), based on a CPLD digital logic, provides optically isolated data-logging under given high dv/dt and isolation voltage. Even in the harsh environment, it measures near-chip module temperature (T_{mod}), drain on-voltage ($V_{ds}(on)$) & device current (I_d). The fault signal and measured data are optically sent to the control side FPGA based IMGD interface board for decoding, data-logging and diagnosis [124, 125].

In this chapter, an active saturation control of SiC device is attempted. An over-current triggered device saturation is controlled using gate-voltage magnitude using a shunt connected BJT. This helps reduce blanking time and increasing SCWT. Active gate-driving is implemented for 15kV SiC IGBT

Table 12.1: Intelligent MV gate driver functions

Parameters/Functions	Value[Units]
Isolation Voltage	20 kV
Isolation Capacitance	$< 1.5\,p$F
Drive Voltages	$+20/-5$ V
Optical Communication	$V_{ds(on)}, I_{ds}, T$
Shoot-through Protection	V_{gs} Controlled
Protections	Local OT, OC, ST
Active Gating	Clock Timed

using CPLD controlled switching circuit to moderate the above punch-through dv/dt without slowing the device with gate-resistance. The CPLD provides flexibility in configuring the signals and protections based on custom application. Together with a local clock, it helps in timing the events such as advanced gating and protections. It interfaces ADCs with the optical signals. It has recommended nominal blanking time of 2.8 µs and extra 2 µs fall time [129]. The typical protection time provided by this driver is 5 µs. The mentioned devices are still in research and development stage and costly. The short-circuit (SC) protection of these devices has currently not been implemented as it is very challenging due to their characteristics [44]. Higher blocking capability for same buffer thickness and better thermal conductivity of these wide band-gap SiC devices have enabled high power density of the chip. But the reduction in chip size has also reduced short-circuit withstand time (SCWT). These devices with small SCWT, cannot be protected by above AVAGO driver. A proper matching has to be done between protection time and SCWT. Reducing blanking time results in spurious trips. The functionality of the proposed IMGD is shown in Table 12.1. This IMGD provides sensing, advance gate-driving, protection and communication functions on top of the basic gate-driving. Advanced gate-driving using the CPLD has to be applied for improving SC protection. The 10 kV SiC MOSFET and the 15 kV SiC IGBT do not have sharp saturation curve for SC protection [130, 44].

12.2 Block Diagram

Fig. 12.1 shows the block diagram of IMGD. It mainly consists of the sensing & measurements, comparators, ADCs, communication, active-gating and the driver stages. A 44 pin ALTERA CPLD EPM3032A is used as the local brain. The simple 6 pin, 40 MHz serial 8 bit, 3 MSPS ADCs are used to convert the critical measurements. The PWM and fault signals are routed through CPLD. The local Over-Temperature (OT) and Over-Current (OC) fault signals are generated using ultra-fast comparators. This board has two optical receivers and four optical transmitters which are configured by CPLD as PWM,

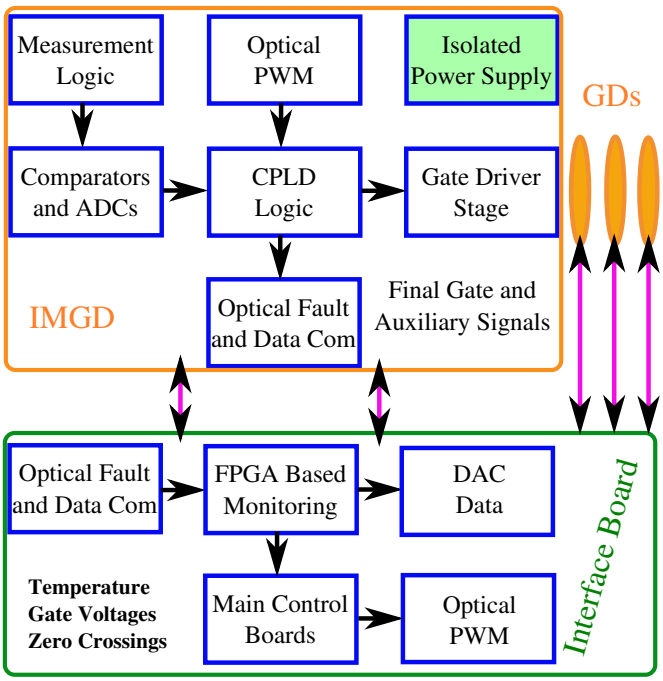


Figure 12.1: Block diagram of intelligent MV gate driver

clock, fault and serial ADC signals. These IMGDs communicate with an interface board which can do the data-logging and independent abnormal condition controls. The FPGA at the interface board can implement the communication decoding and other digital functions such as status display. The main control boards based on DSP or FPGA, implement the actual control algorithm for the converter systems such as Grid-tie Front End Converter [131] and dc-dc Dual Active Bridge [42]. They also have separate provisions for over-voltage and OC protections of the converters. They need feedback sensors such as voltage and current sensors for closed-loop control. The PWM cables are optical. The feedback sensors must have very small coupling capacitance and good isolation level for EMI resistant functioning.

12.3 Active Gating and Shoot-Through Protection Circuits

12.3.1 Active Gate Driving

As shown in Fig. 12.2, a pair of resistance paths are switched between S and GD ground SC1 to create a dynamically changing effective gate resistance during device switching. The sequence and delay of these switching is digitally controlled by the CPLD in steps of local 100 MHz clock. The advantage is mostly for SiC IGBTs above punch-through voltage switching [40]. The steeper dv/dt can now be controlled without increasing the gate-resistance and the losses. This feature can also be used with MOSFET/IGBT to reduce the spike current during turn-on so that desat blanking time could be reduced

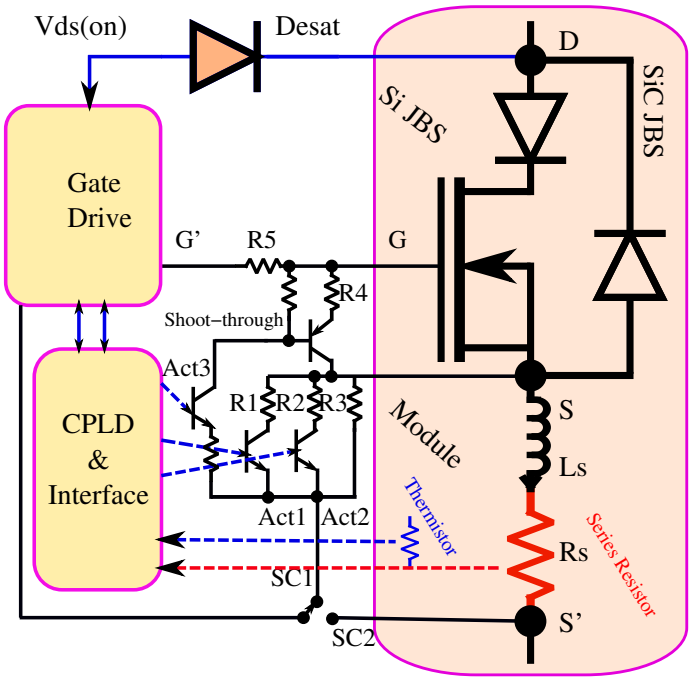
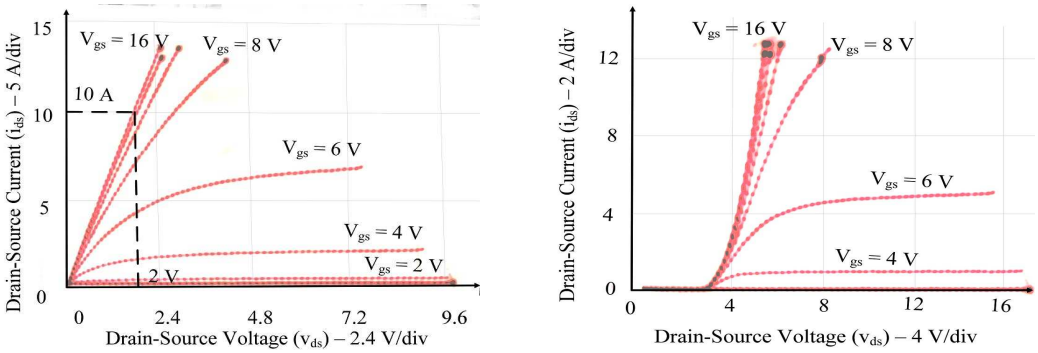


Figure 12.2: Active gating & protection circuit



(a) 10 kV SiC MOSFET **(b)** 15 kV SiC IGBT

Figure 12.3: Forward characteristics of the HV SiC devices

by avoiding spurious fault detections. Since the AVAGO driver has 300 ns delay between input PWM and output pulse, the active BJTs timings are relative to the output pulse by feeding it back to the CPLD [129].

12.3.2 Shoot-through or SC protection by controlled saturation

The present AVAGO driver is retained on this IMGD for driving stage similar to the previous 15 kV SiC IGBT GD [44]. Fig. 12.3(a) and Fig. 12.3(b) show the SiC MOSFET and IGBT forward characteristics.

It can be seen that both devices have limited saturation current for V_{gs} in range of 6 to 8 Volts. Fig. 12.4 shows the timing diagram of AVAGO driver [129]. After the fault is detected, it takes $t_{desat}(90\%V_{gs})$ = 300ns to start dropping the V_{gs}. The $t_{desat}(10\%V_{gs})$ depends on R_g and C_{gs}, and can be typically in order of 2µs. A blanking time of t_{blank}=2.8µs is recommended to avoid dv/dt noise. So the minimum protection time is $t_{desat}(10\%V_{gs})$ + t_{blank} which is typically 5µs. The shoot-through solution for SiC

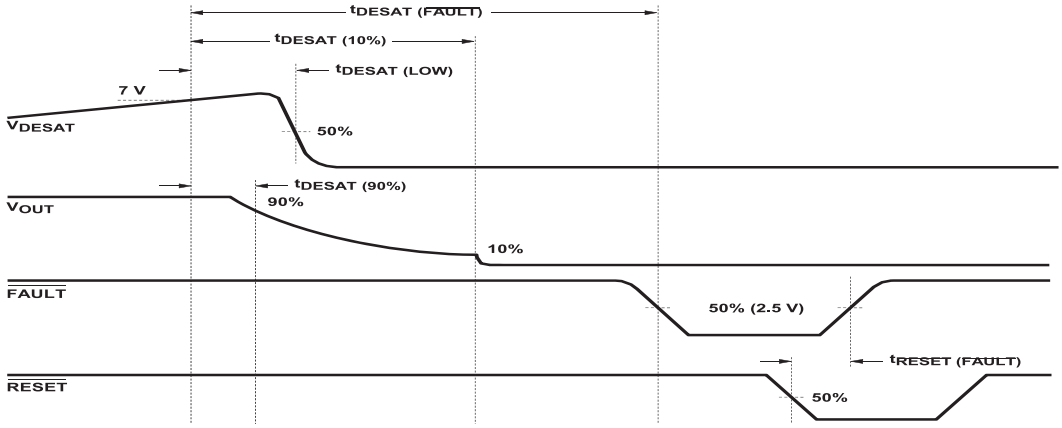


Figure 12.4: AVAGO driver protection timing diagram

10kV MOSFET and 15kV IGBT is difficult as it does not allow this magnitude time duration before it fails. Therefore this typical time has to be shortened: 1. By turning device quickly off during desat=7V detection using very low off gate-resistance in order of 1 or 2Ω, 2. Minimizing t_{blank} but at the cost of increased noise pick-up. The second active pulse terminal can be used to reduce gate resistance during desat trigger but it is internal signal and its difficult to change gate-resistance externally without this trigger information. Fig. 12.2, a gate-voltage level reduction using a shunt switch circuit during short/overload is used to protect the device by forcefully saturating it. A regulator cannot achieve this as it cannot discharge 20V quickly, so a switching topology is used to change voltage quickly [125]. The OC level for triggering the shunt circuit is kept 2-3 times peak nominal current and is enabled using a digital blanking time to avoid spurious trigger which would result in abnormal gate-driving. At the start of the gate-pulse, the comparator is disabled for specific time duration and then used to latch this OC fault. With reduced gate-voltage during OC the MOSFET is more likely to saturate [130]. This enlarges the SCWT of the device and also makes the desat detection fast together with the soft turn-on using active gating described above. The AVAGO driver can now generate a desat fault signal in case of the real SC equivalent to smaller blanking time. Another provision for SC protection is to dynamically use device S and S terminals with overlapping switches such that during SC, gate voltage is naturally lowered by sense resistor to protect the device. Both of these methods are tried in this GD board as

marked in Fig. 12.2.

12.4 Circuit Implementations

The SiC MOSFET and IGBT modules are supposed to have inbuilt shunt resistor and a thermistor temperature sensor as shown in Fig. 12.2. They provide foundation for the IMGD main functions. Fig. 12.1 block diagram components are explained in following points.

- A thermistor signal amplifier is on board for signal conditioning. The INA330 is used for this purpose and the resistor values are designed using (1) and configured for temperature measurement up to 80°C currently [132].

$$R_m^{Min/Max} = \frac{R_G}{\frac{R_G}{R_1} \pm 1.65} \tag{12.1}$$

- Two current sense differential amplifiers are placed for device and gate current signals. They are based on fixed gain (G=20) current sense amplifier ADM4073 [133].
- Differential amplifier for on-state drain voltage measurement is also included.
- Ultra-fast high temperature EMI hardened comparators & analog to digital converters (ADC) convert the measured signals into digital domain for outside optical communication. The used comparator LMV7219 has 7 ns delay with internal hysteresis [134]. The used ADC AD7278 has high speed serial interface with 3 MSPS throughput [135]. Fig. 12.5 shows the timing diagram for

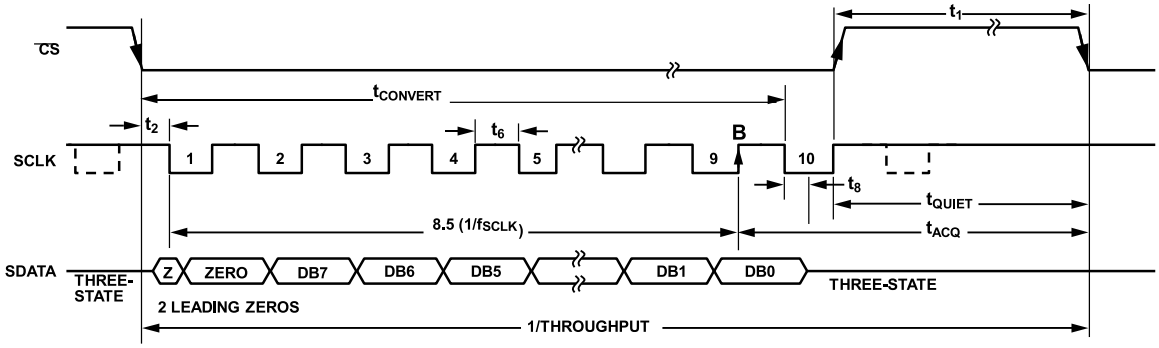


Figure 12.5: ADC timing diagram

ADC interfacing [135]. The clock-speed for nominal throughput is 36 MHz. Due to limitation of optical bandwidth of 10 MHz, a lower word data rate of 250 kSPS is implemented. The spike data such as gate-current does not need to be converted to 8 bit, rather it can be sensed with comparators for few selected di/dt slopes.

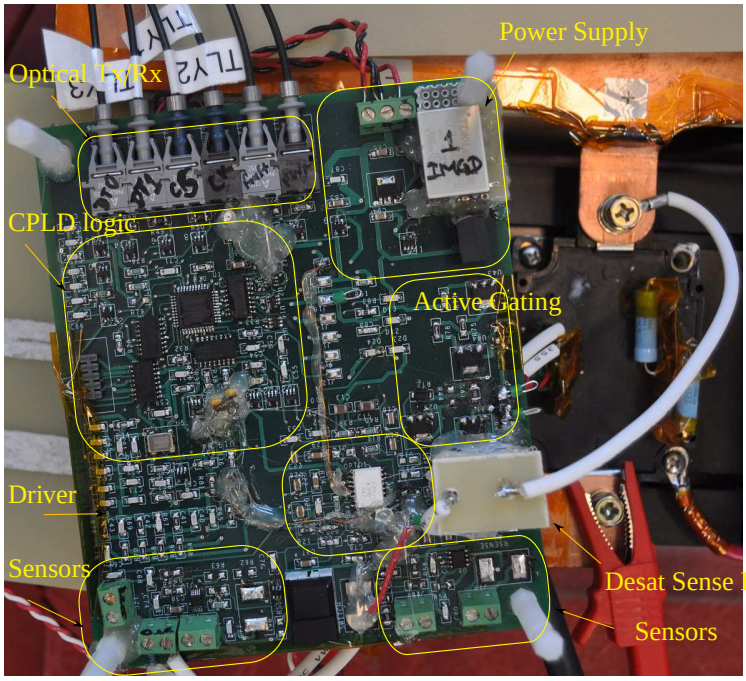


Figure 12.6: Intelligent gate driver circuit board

- Optical Links: Individual IMGDs of a converter need to send fault signals to main control board. All the IMGDs to interface communication including PWM and fault signal, is via optical fiber cables to provide necessary isolation. Important ADC and comparator information also needs to be sent as digital signal using simple protocols. The optical cable uses Avago HFBR-1528 transmitter and HFBR-2528 receiver with 10 MBd signaling rate. This signaling rate is sufficient for sending important information to the interface board.

12.5 IMGD and Interface Boards

Fig. 12.6 shows the populated IMGD board with all mentioned functions. This is the first version board with extra components than the requirement. In the final version this will be optimized. It has different analog and digital functional sections which are separated from one another for better EMI performance. Fig. 12.7 shows the populated interface board which communicates with the IMGDs of a MV converter. It has on-board DACs and FPGA board for implementing monitoring and data-logging function. Each IMGD has 4 Tx and 2 Rx used respectively as Fault, DT0, DT1, CS, CK and PWM. The interface has the opposite type optical Tx/Rx for all signals and 12 IMGDs. The interface FPGA transmits a common clock for IMGD ADC operation and communication. The IMGD generates CS signal for framing of serial data and each bit is read synchronous to the transmitted clock of interface. The critical

measurements can be converted by DACs for display and data-logging. Based on any abnormality or any fault signal from any particular IMGD, all the IMGDs can be turned off together for safety.

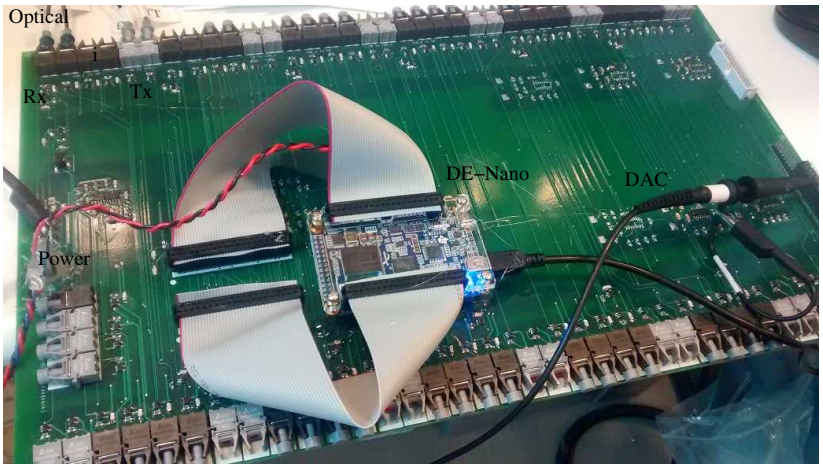


Figure 12.7: IMGD interface circuit board

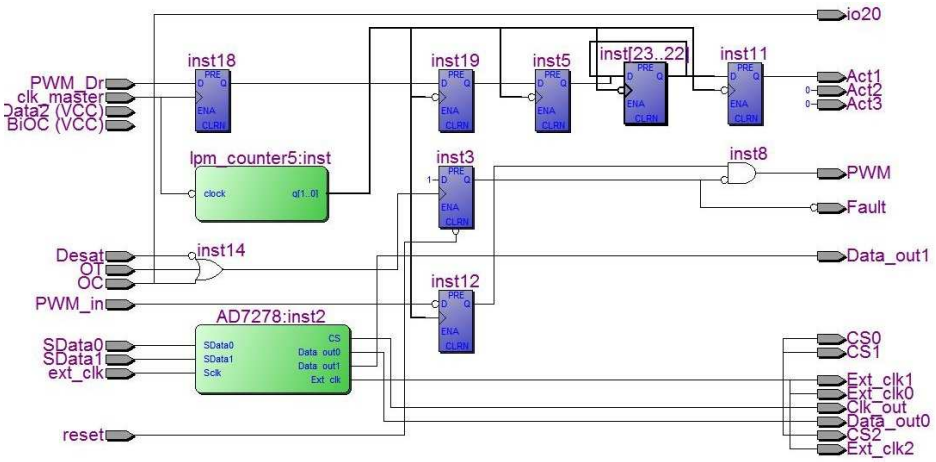


Figure 12.8: Altera Quartus II RTL view of the CPLD implementation on IMGD

Table 12.2: IMGD CPLD utilization

Parameters	Value[Units]
Family	MAX3000A
Device	EPM3032ATI44-10
Timing Models	Final
Total macrocells	27/32(84%)
Total pins	30/34(88%)

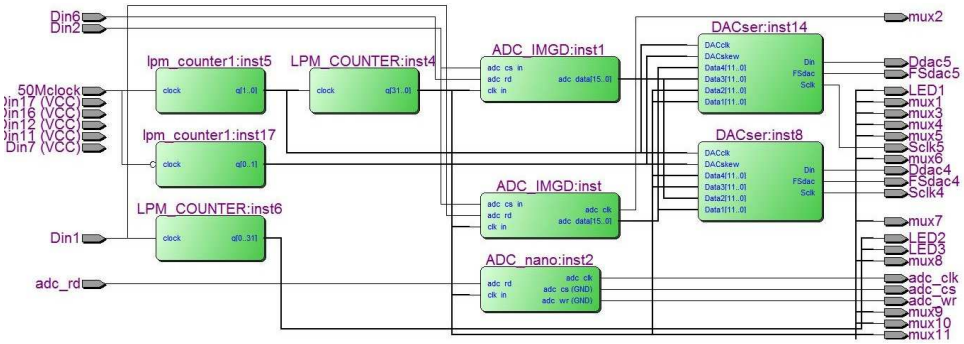


Figure 12.9: Altera Quartus II RTL view of the interface implementation

12.6 Digital Implementations

The motivation for using CPLD is that it is digital and the in-circuit programmable chip once programmed, works as a hard wired custom logic. There is no loading time delay as in case of a FPGA with an EEPROM. The digital processing is more noise resistant compared to the analog processing for active gate-drive, smart protection and optical-communication functions. Considering the harsh EMI environment for the GD, a CPLD EPM3032A with 34 I/O, 5 ns pin to pin delay, 32 macro-cells and 600 gates size is selected to implement the required digital functions. There is individual on-board clock 100 MHz for timing the active-gating and desat protection signals. This allows 10 ns resolution in the timing. For the active-gating, the driver output PWM is synchronized with the local clock using a register and other cascaded registers are fed with appropriate divided clocks to generate delay. The interface generated optically received clock is used for ADC operation and communication as there is no need for synchronization and more than 10 MBd speed. The CPLD implements five main functions a.) ADC protocol, b.) Oring and latching the local protections b.) Optical comm. to interface board, c.) Active gate-drive by switching transistors with series resistance, d.) Smart protection by shunt transistor-series resistance switching in case of over-current. Fig. 12.8 shows the RTL view of the simple implementation of latched fault protected PWM gate-driving with active-gating, data-logging and OT, OC protections. It takes sen-

sor digital inputs, optical PWM, local & external data clocks, desat, driver output and generates digital data, serial data-frame CS, common-fault and PWM for desired purpose. Table 12.2 shows the device utilization for the CPLD with mentioned implementation. The selected CPLD is optimum in terms of complexity and resources. Fig. 12.9 shows the RTL view of the simple implementation of FPGA based interface board. It is configured for this basic test to read two data lines of an IMGD and direct it to on-board two DACs for logging. It provides PWM and communication clock to this IMGD as well.

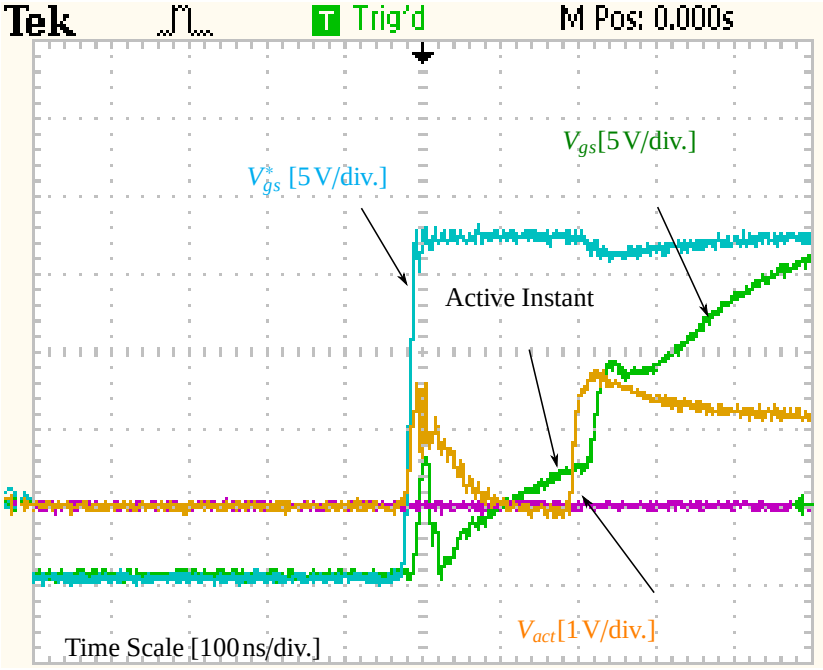


Figure 12.10: Active pulse generation test

12.7 Experimental Results

The designed gate-driver is tested on a 10 kV SiC MOSFET and 15 kV SiC IGBT. The gate voltage control, temperature measurement, active gate resistance and current sensing features are tested. The digitally controlled active gating pulse w.r.t. the Driver output PWM is shown in Fig. 12.10. The waveform shown is BJT base voltage w.r.t. control ground. The V_{gs} is the gate-voltage measured at the IMGD output pins. The connecting wire inductance causes a positive spike during turn-on transition but it does not appear on the device termination pins. Fig. 12.11 shows DP switching test of 10 kV SiC MOSFET at 6 kV and 10 A with 10 Ω R_g. A turn-on spike can be seen shooting to 30 A. Fig. 12.12 shows the result under same conditions for testing the active-gating functionality. The starting R_g is 50 Ω. It can be seen

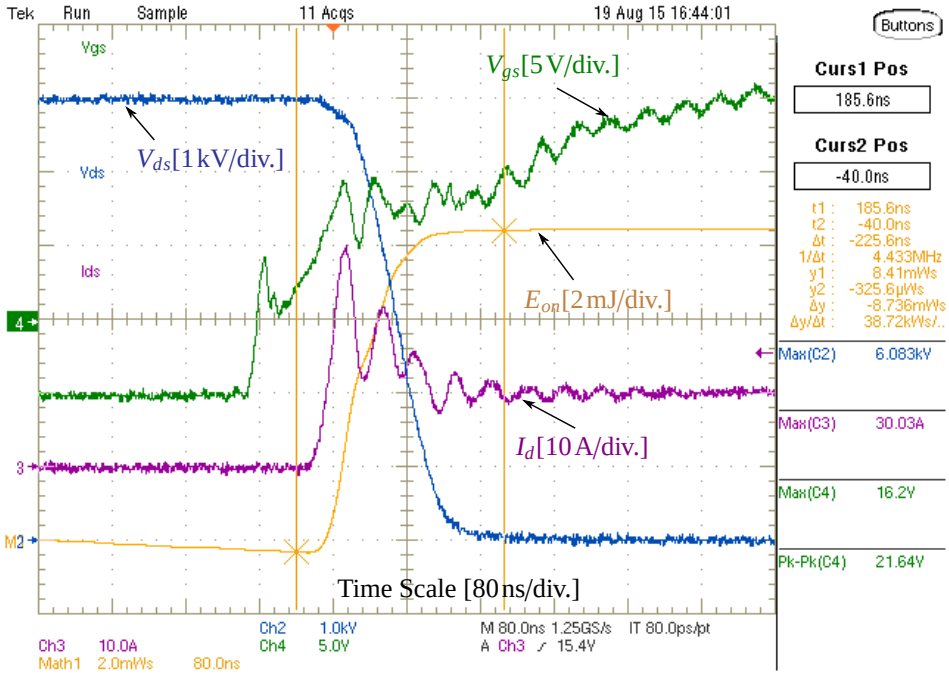


Figure 12.11: Passive gating double-pulse test

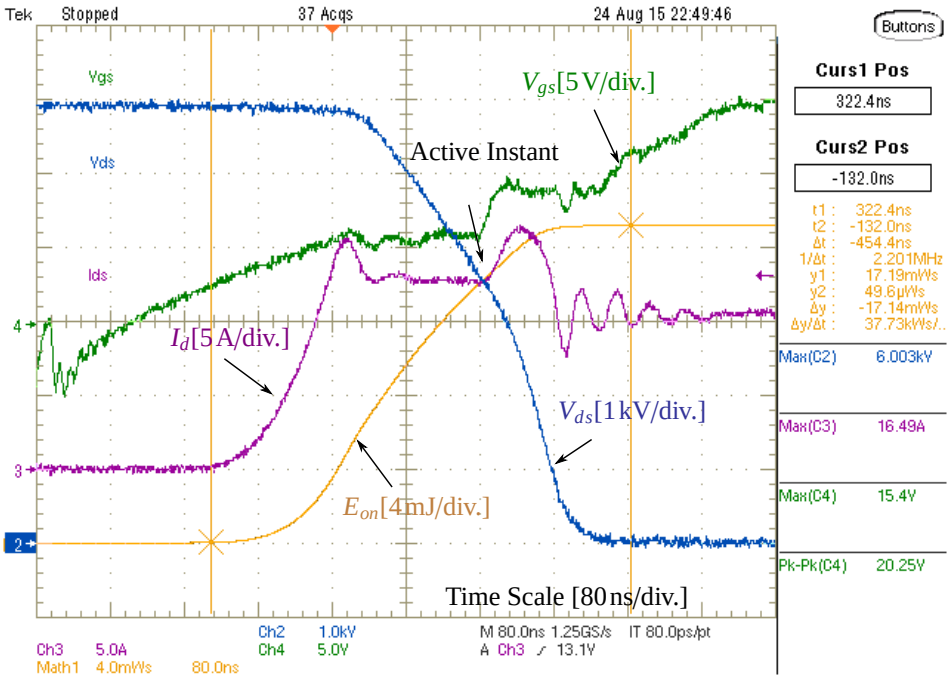


Figure 12.12: Active gating double-pulse test

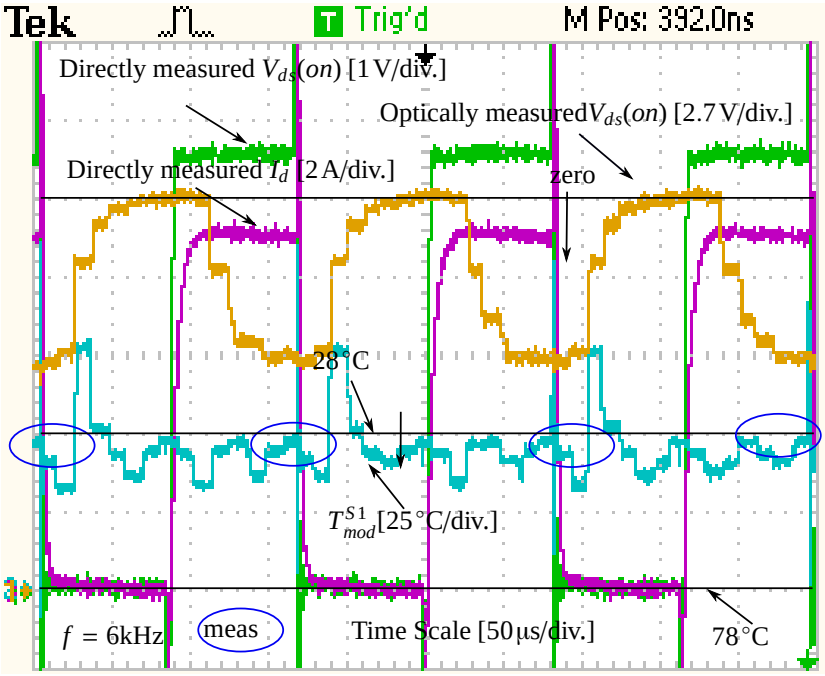


Figure 12.13: Monitoring test with IMGD using genesic desat diode at 60V

that the active circuit with 4.7Ω R_g is switched on after certain delay. This delay can be tuned such as to reshape the V_{ds}. This will be helpful in soft turn-on and also in moderating 15kV SiC IGBT dv/dt as discussed earlier.

Fig. 12.13 shows the LV test for verifying optical measurements from the IMGD and the desat function using Genesic 8kV desat diode. This is a 50% duty test on a resistor load in series with the IGBT. This desat setting allows upto 9A current for this IGBT. The desat-sensing, $V_{ds}(on)$, T_{mod} and I_d measurements are verified in this setup. The $V_{ds}(on)$ signal is shown in negative polarity for current DAC setting but it can be scaled as per requirement. Fig. 12.14 shows the boost-buck hardware setup photograph for validating the IMGD with its basic functionality. 15kV SiC IGBT is selected for this test as it applies harsher dv/dt on the IMGD above punch-through level. A H-bridge bus-bar arrangement has been used with SiC JBS diodes on position 1 and 4 in free-wheeling polarity. The IGBTs are in position 2 and 3. The IMGD drives the top side IGBT for HV validation. Fig. 12.15 shows the results for 5kV, 3.75kW operation for the IMGD at MV potential. The boost input is 1.25kV and output is 5kV. The boost duty is 25%. The buck converter IGBT switch is now at higher potential so that its IMGD gets 5kV pulsating stress. The buck duty is 50% feeding a resistive load for simplicity. The IMGD input power supply is at ground reference and the output which powers the IMGD, is at 5kV stress. Fig. 12.17 shows the optically transmitted $V_{ds}(on)$ and T_{mod}^{S1} measurements coming from the IMGD out of high voltage setup. The T_{mod}^{S1} signal gets distorted near device voltage transition due to change in the

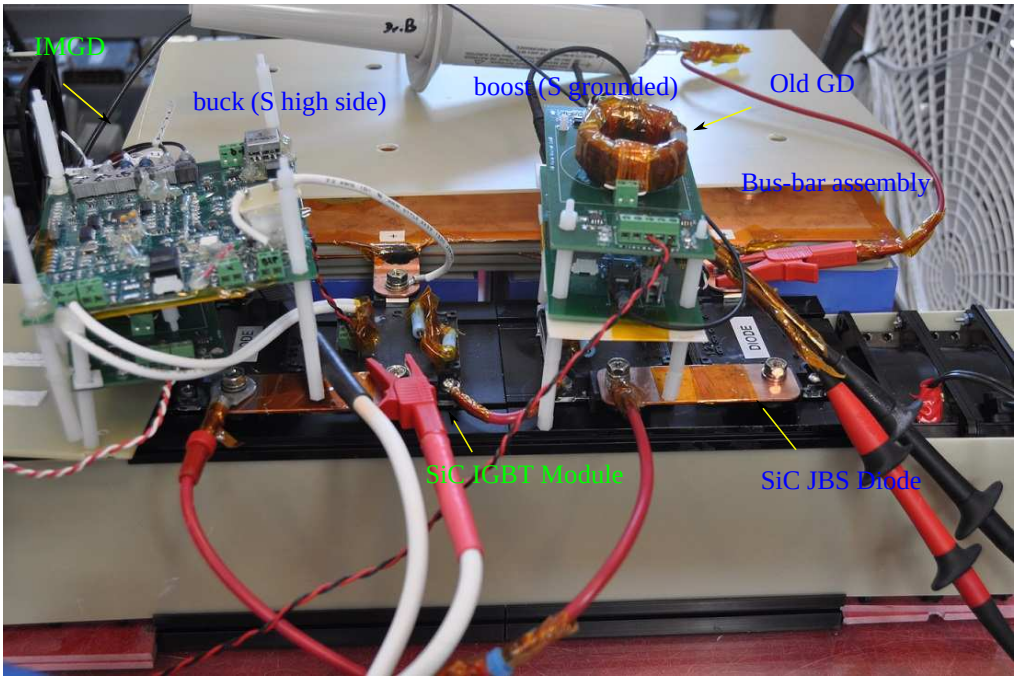


Figure 12.14: Boost-buck setup

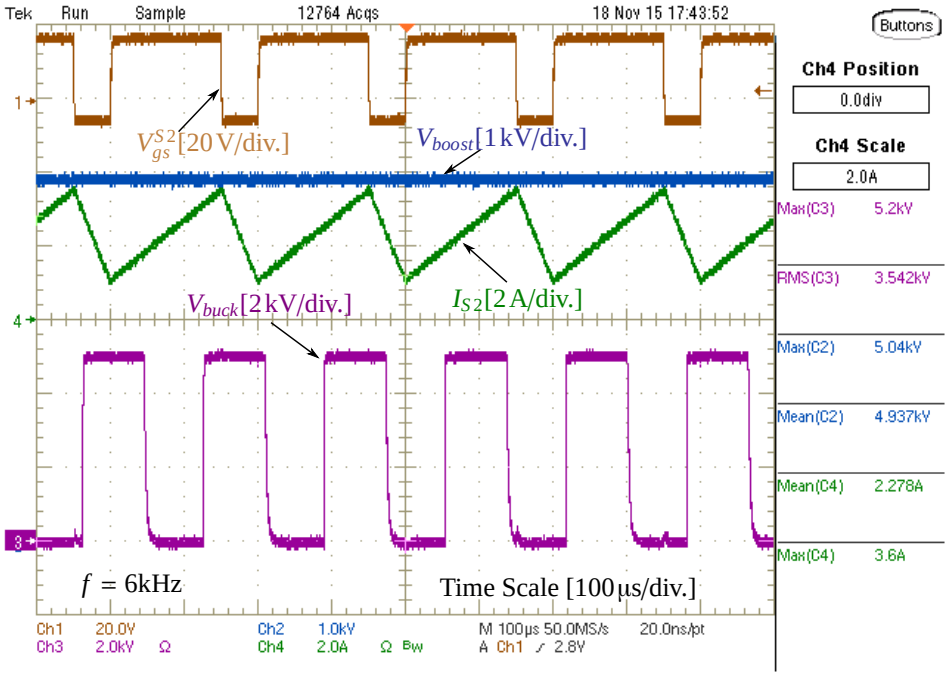


Figure 12.15: 5 kV, 3.75 kW boost-buck GD qualification results

Figure 12.16: Boost-buck test thermal photograph

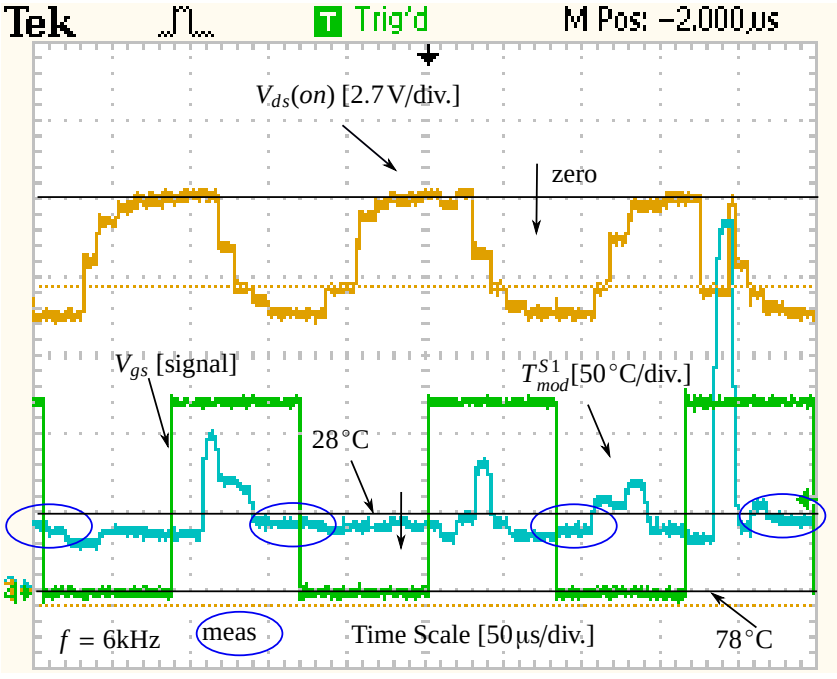


Figure 12.17: 5 kV boost-buck GD qualification interface side results

ground level and EMI. Normally it is not required to be logged so fast, therefore it can be measured only in the encircled zone and averaged for logging. Fig. 12.16 shows the thermal photograph of the setup in Fig. 12.14 after 30 min thermal run at 5kV and 3kW power in boost-buck operation.

12.8 Conclusion

A MV intelligent gate-driver from block diagram till implementation, has been presented in this chapter which is not only capable of active gate driving and extended shoot-through protection for HV SiC devices, 10kV,15kV MOSFET and 15kV IGBT but also able to optically fetch real-time operating switch data to the outside main control for ZVS enforcement and data-logging purposes. The $V_{ds}(on)$ and temperature are very useful to determine stability of the non-cascaded MV SiC converter using HV SiC devices. The operating data of this gate-driver such as temperature, current, $V_{ds}(on)$ sense in high side of boost-buck converter at 5kV have been optically received on main control board and presented in this chapter. The active gating for demonstration has been verified in the 6kV double-pulse results. The shoot-through test with advance protection for the HV SiC devices, has not been completed.

Chapter 13

10kV SiC MOSFET Based NPC Poles for MV DAB Application

13.1 Introduction

The recent developments in HV SiC MOSFET and SiC IGBT device technology have paved way for simple non-series & non-cascaded medium-voltage (MV) converter topologies [14, 11]. These devices can operate at higher voltages and can switch at higher frequencies compared to their Si counterparts [31]. These characteristics enable applications such as high-speed MV drives, MV dc micro-grids and compact grid-connected converters for renewable energy [131, 42]. The DAB being a ZVS turn-on soft-switching topology, the two HV SiC devices can be compared for turn-off and conduction losses. This chapter compares the two devices for a previously presented MV DAB application with supporting results. The high dV/dT occurring in these devices in conjunction with the parasitics, causes EMI and increased switching loss towards the light load where loss of ZVS is possible. These two HV SiC devices have different switching characteristics. The suitability of each device depends on the switching frequency, power level, operating temperature and converter power density requirements. The qualification results of MV NPC converter poles for DAB application based on 15kV SiC IGBT device are presented at 10kV dc bus in previous chapter. This chapter presents the same condition test results for 15kV SiC MOSFET under 5-20kHz switching frequencies and compared for performance. The 8kV-480V experimental validation of the MV DAB based on 15kV SiC IGBTs switching at 10kHz is presented in previous chapter. This chapter utilizes the same8kV-480V dc MV DAB hardware as the target application to compare the HV SiC devices for performance. The expected efficiency for this application based on the two devices is estimated from simulation using real switching data. The MV DAB operation at light load is a critical region for the design due to inter-dependence of switching dv/dt on ZVS, device & load parasitics and dead-time. For the DAB MV converter ZVS must be maintained in all conditions for which the DAB current needs to lag behind primary-voltage by a certain phase-angle

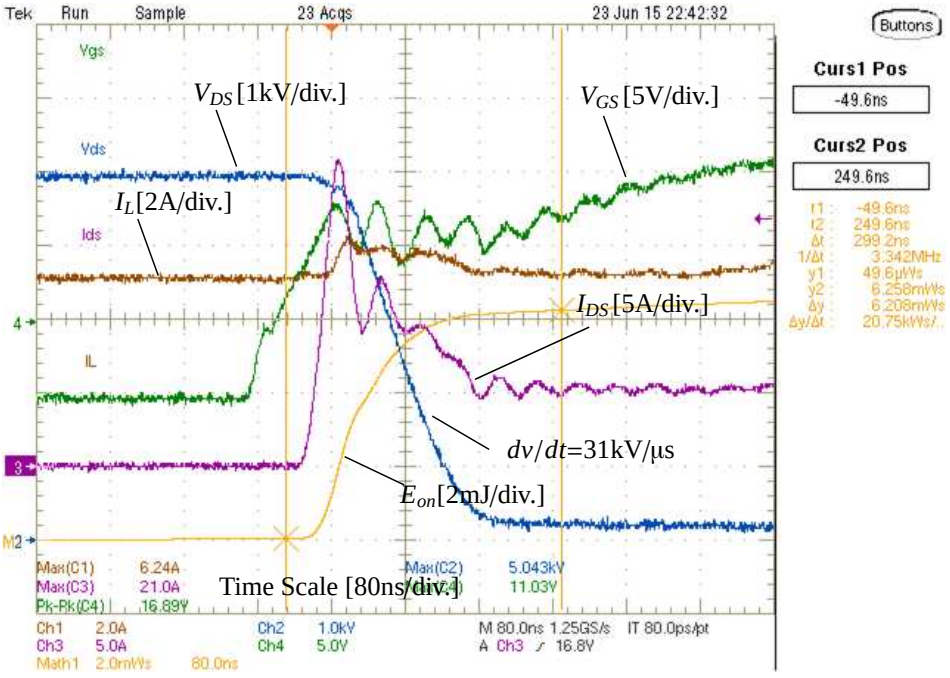
defined by the non-idealities. For light load ZVS in the present context, some methods have been studied in [105]- [107]. This chapter is organized as follows. First the comparison of real switching test of the two devices in similar conditions is presented. The NPC three-level converter poles built using these devices are presented with experimental results. The effect of ZVS and different switching frequency on the DAB mode switching for the two devices are clearly shown. This chapter then presents an estimation of efficiency with the two devices for the target TIPS-DAB topology. The last section discusses the suitability of the two devices for different conditions based on the earlier discussed sections.

13.2 15kV SiC IGBT and 15kV SiC MOSFET Application

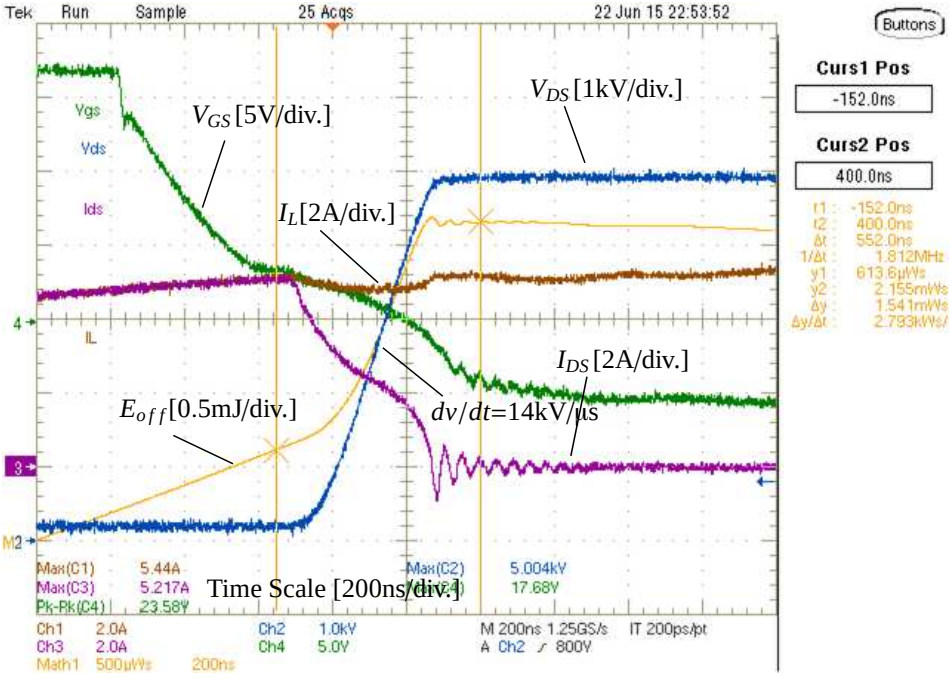
The HV SiC devices have enabled the use of a simpler 3-level neutral-point clamped (NPC) topology [23]. The switching capabilities for the 15kV SiC IGBT ranges from 3-10kHz while 5-20kHz for 15kV SiC MOSFETs [58, 136, 130, 137]. The higher switching frequency theoretically reduces the filter size on the AFEC and the MV-HF transformer size of the DAB stage. But these devices have high dV/dT switching steepness and considerable parasitic capacitance which needs to be tuned with MV-HF transformer parasitics and the needed dead-time to ensure ZVS operation at light load [23]. The compactness of the MV DAB transformer often works against the low parasitic capacitances requirements. The developed 15kV SiC IGBT uses punch-through (PT) technology for faster switching. But it results in double dv/dt slope for voltage above and below PT level. To reduce the EMI level for a specific MV DAB design, the maximum dv/dt needs to be limited. The 15kV SiC MOSFET being a unipolar carrier device has single dv/dt slope which is variable with the gate-resistance. But for the 15kV SiC IGBT, the above PT slope is difficult to control with gate-resistance without poorly slowing the second slope and increasing the losses. An active-gating solution for dv/dt management has been evaluated in [40]. A snubber solution has been validated in this regard in [123]. Other way to look the devices from circuit perspective is that 15kV SiC IGBT has very small parasitic capacitance above PT compared to the 15kV SiC MOSFET. Therefore the MOSFET does not require snubber at all. Broadly it is more suited for relatively lower power but higher switching frequency. A three-phase Y-Y/Δ DAB was selected for 22kV dc to 800V dc at 100kW application earlier in [23]. This topology was selected to utilize the 15kV/20A SiC IGBTs and 1200V/100A SiC MOSFET modules in one DAB unit supplying 100kW rated load under rated conditions for simple control. The secondary side Y/Δ connection improved the current THD suitable for internal D-Q current control.

13.3 15kV SiC MOSFET Switching Test Comparison

The 15kV/20A SiC MOSFET hard-switching characteristics at 5kV/5A/175°C are shown in Fig. 13.1 and presented in [137]. Again it should not be switched at a very high dv/dt due to EMI issues Limited dv/dt helps transformer spike currents to be limited. The hard-switching test results of the 15kV/40A



(a) Hard turn-on at 5 kV/5 A



(b) Hard turn-off at 5 kV/5 A

Figure 13.1: 15 kV/20 A SiC MOSFET switching characteristics at 5 kV/5 A/175°C

Table 13.1: Comparison of Approximate Co-pack Module Pole Capacitance

Device	2μm/20**A IGBT**	5μm/40**A IGBT**	20**A MOSFET single**	20**A MOSFET leg**
Gate on-resistance (Ω)	200	33	14.7	33
Current overshoot	5.5	5	15	15
Maximum turn-on dv/dt **(kV/μs)**	70	30	45	31
Pole cap. C_{ce} **(pF)**	80	165	330	500

SiC IGBT module are presented for same condition in chapter 6. A clamped inductive double pulse test (DPT) setup is used to characterize hard-switching of the devices. The conduction characterization with temperature is carried on forward test using hot-plate. The gate resistances of 33Ω and 10Ω, are used for turn-on and turn-off switching respectively, both in the IGBT and MOSFET tests. The switching waveforms are captured during the transition for 15kV/20A SiC MOSFET. The maximum dv/dt of both type devices are similar in this condition [137]. The i-v area during transitions are integrated for measuring losses. The IGBT turn-on and turn-off losses are 9.4 mJ and 19 mJ respectively. These are found to be 6.2 mJ and 1.5 mJ respectively for MOSFET. This makes MOSFET suitable for higher switching frequency application as expected due to its unipolar characteristics. From the forward test, the on-state voltage drop is 4.31 V for the IGBT at 150°C, 20 V on-gate voltage and 5 A current. The specific on-resistance of the MOSFET varies from 0.64Ω at 25°C to 1.65Ω at 150°C. This makes its voltage drop 8.25 V at 5 A current at 150°C. From total loss perspective and for a hard-switching converter application, IGBT can be a better choice for higher power level and lower frequency. On the other hand for lower power and higher frequency application, MOSFET is suitable. This SiC device selection criteria is similar to its Si counterpart. However from the SiC IGBT DPT test results, a turn-on spike can be seen shooting up to 30 A. Also two slopes can be noticed for below and above PT level. To keep higher dv/dt limited for EMI performance, IGBT is dissipating more energy. With various i-v conditions loss data available for the two devices using the DPT test, a LUT of turn-on and turn-off losses is constructed for system level loss calculation. An approximation of an equivalent co-pack module pole capacitances, based on turn-on DPT test current-spike region results, is presented in Table 13.1. These parasitics from circuit point, might be equivalent to a total pole capacitance (snubber) and can be used for comparison purpose between devices for ZVS consideration. It can be seen that IGBT has smaller device capacitance. The device capacitance is favorable for reduced turn-off losses and EMI, but it needs more negative lagging current for ZVS soft turn-on in a NPC or half-bridge based DAB converter.

13.4 MV NPC Pole Test Comparison

The 3-L NPC pole built using these devices is shown in Fig. 6.5 with all accessories labeled. Prior to putting these poles in MV DAB setup, they have been heat-run tested individually at a dc bus supplied from a boost source. A more detailed discussion regarding MV SiC converter setup is presented in [28].

These NPC poles are switched in quasi-square mode with 41.6% duty-ratio to generate minimum THD for MV DAB application [23]. When switched with 3kΩ resistive load, both devices generate turn-on spikes due to hard-switching as shown in Fig. 6.10 and Fig 13.2. The power output corresponds to 7.2kW for 10kV dc bus and 4 kW for 6 kV dc. When expanded it shows turn-on switching loss of 1.6 mJ for Fig. 6.10 [23]. It happens due to device capacitance and load capacitance charging, since at this dv/dt, the parasitics are significant. Therefore higher dv/dt results in increased energy-loss and EMI. For full ZVS in the DAB, the device parasitic capacitances must be fully discharged to zero before the dead-time ends. The dead-time is 3.4µs for mentioned gate drive setting. The ZVS condition is emulated here by adding a 14 mH series inductance with the load. Fig 13.3, Fig 13.4, Fig 13.5 and Fig 13.6 show various

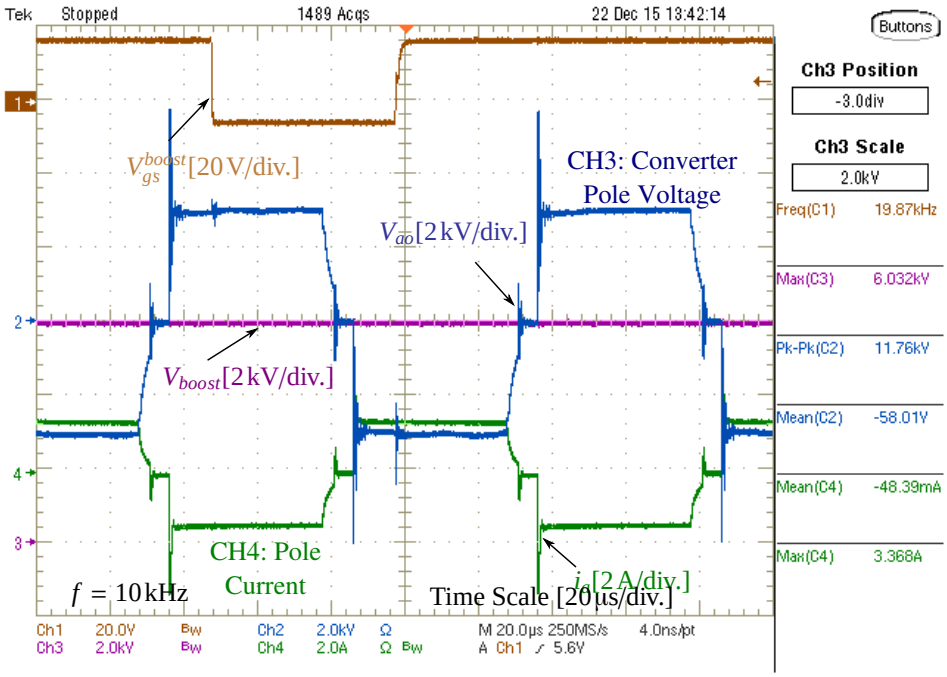


Figure 13.2: 15kV SiC MOSFET based 6kV NPC pole 4kW with R load at 10kHz

results with partial or full ZVS conditions. It can be seen that more lagging current is required by the MOSFET for full ZVS that certainly happens in Fig 13.6. With higher frequency and same inductor, the current became more lagging which caused the ZVS. The corresponding ringing and spike are smaller in the voltage as device voltage becomes zero before dead-time ends. The real power changes with the frequency. Fig 13.7 shows the thermal images for these tests after 20 min heat-run test each. It can be seen that for ZVS condition, MOSFET has less loss even at higher switching frequency as expected. This happens because it has higher parasitic capacitance compared to IGBT for same condition which makes turn-off transition regenerative and the stored energy is reclaimed in next turn-on switching instant.

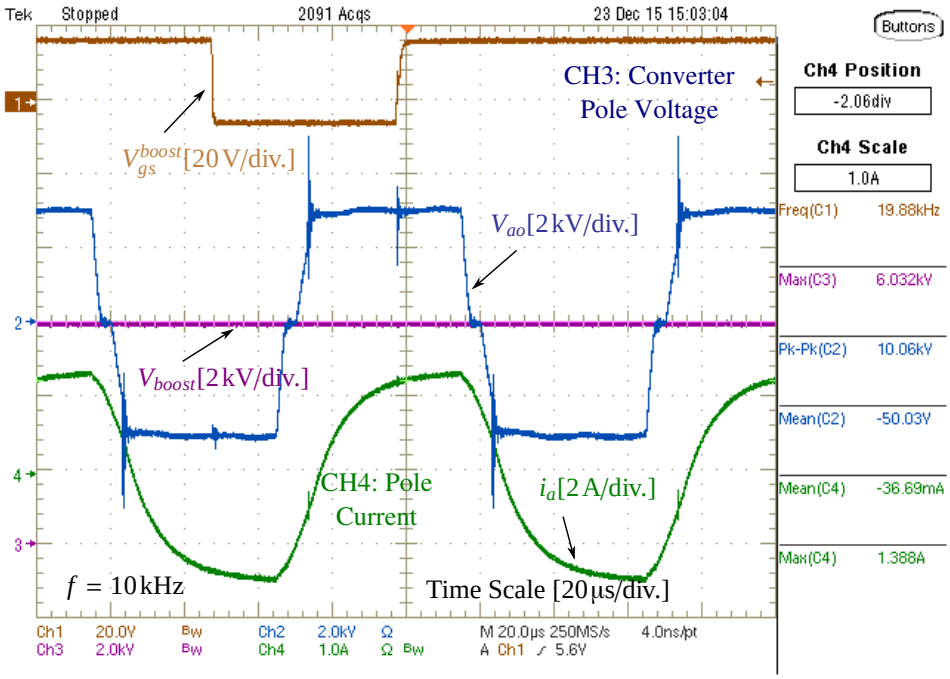


Figure 13.3: 15 kV SiC MOSFET based 6 kV NPC pole 4 kW with RL load at 10 kHz

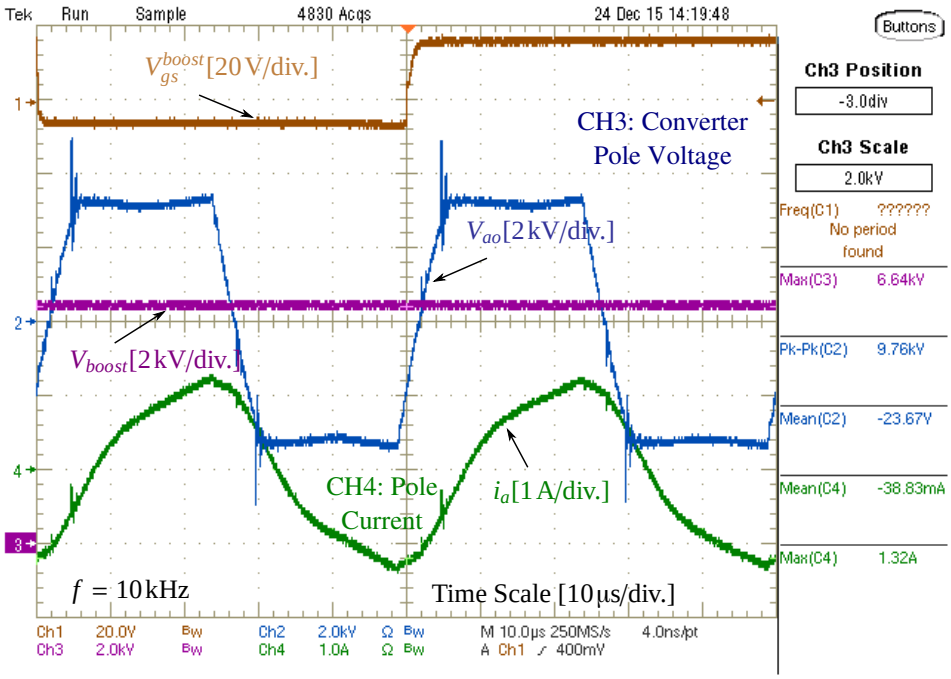


Figure 13.4: 15 kV SiC MOSFET based 6 kV NPC pole 4 kW with RL load at 20 kHz

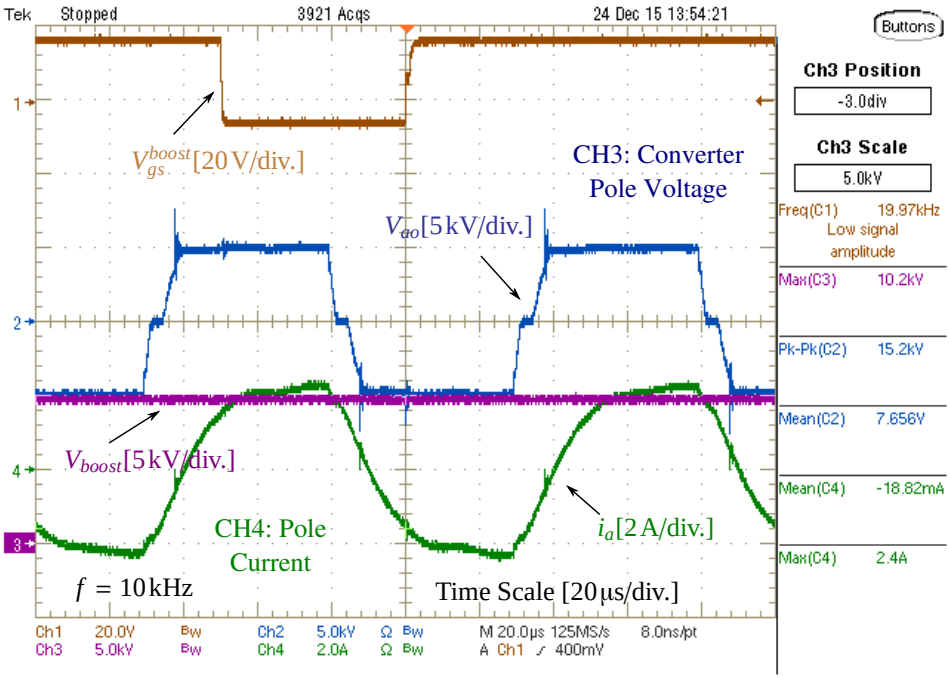


Figure 13.5: 15 kV SiC MOSFET based 10 kV NPC pole 7.2 kW with RL load at 10 kHz

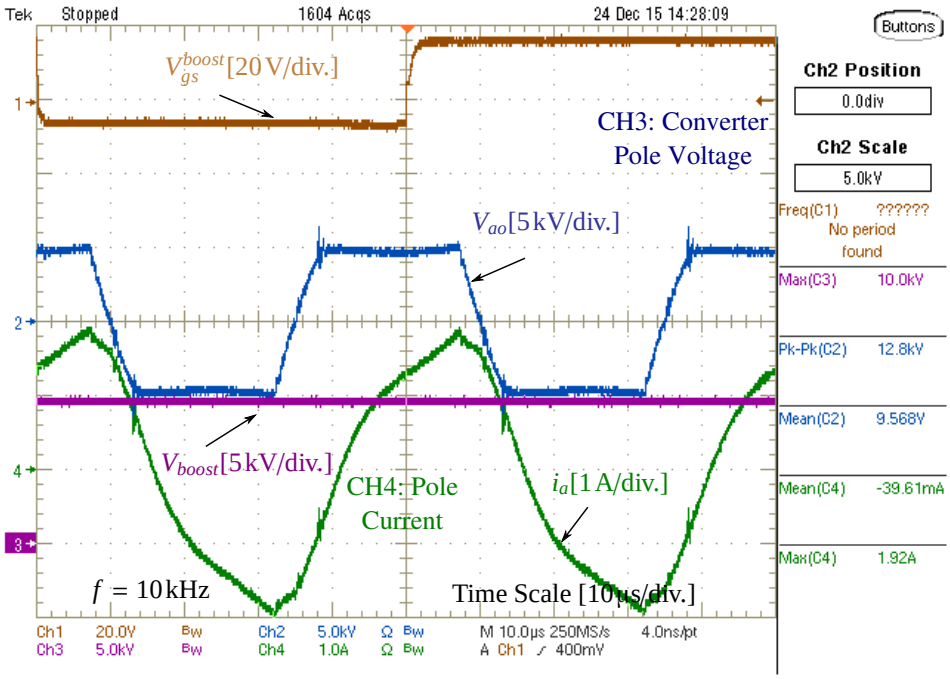


Figure 13.6: 15 kV SiC MOSFET based 10 kV NPC pole 7.2 kW with RL load at 20 kHz

(a) 6 kV thermals R load at 10 kHz

(b) 10 kV thermals RL load at 20 kHz

Figure 13.7: 10 kV thermals RL load at 20 kHz

Table 13.2: DAB Expected Losses and Efficiency 8 kV-480 V

Load[kW]	50	50	50	10	10
Device	**IGBT**	**MOSFET**	**MOSFET**	**IGBT**	**MOSFET**
Frequency[kHz]	10	10	20	10	10
MV Switching[W]	875	52.8	91.9	305	43
LV Switching[W]	33.5	32.6	36.3	56.4	50
MV Conduction[W]	143	164.4	169.5	30.6	18.6
LV Conduction[W]	279	276	257	52.3	59.4
Total Conv. Loss[W]	1331	525	554	445	171
Output Power[kW]	54.76	54.32	50.39	11.07	11.74
Efficiency[%]	97.63%	99.04%	98.91%	96.14%	98.56%

13.5 MV DAB ZVS Challenge and Efficiency Projection

The schematic of the MV DAB testbed is shown in Fig. 2.5. The rated parameters are shown in Table 6.1. ZVS must be maintained in the MV side converter in all conditions for the DAB to avoid switching loss and EMI. This can be achieved in the DAB by simply keeping output voltage low so that it draws lagging current from the NPC pole for the demo. Since it is intended to show higher voltage switching in real grid-tie system consisting of AFEC tied to 4.16 kV, the power out of each NPC pole is very low and there is no considerable heating of the converters. Therefore losses can only be estimated using the actual device hard-switching data and are found to be really close to actual thermals. The turn-on ZVS happens in the simulation and so it does not contribute to the losses. Table 13.2 shows the loss estimation for the DAB for both type MV devices. For 20 kHz simulation DAB inductance is halved for fair comparison. It can be noticed that MOSFET proves to be more efficient both at light and full load. But if the converter heat sink design is optimized for size and higher operating temperature, this trend might reverse.

13.6 Conclusions

Both the HV SiC devices are tested for hard-switching (double-pulse) as well as in a real converter situation (NPC pole). The ZVS turn-on soft-switching that happens in optimum DAB operation is emulated with inductive load pole testing. The switching losses for this mode is very low as expected from simulation and also from the NPC pole heat-run test where temperature drops from 31.8°C at 6kV, 10kHz to 25.9°C at 10kV, 20kHz. The demo dc voltage of 8kV is sufficient for 4.16kV MV grid interface application and dc micro-grid. But the MOSFET capacitance being higher than IGBT, it requires more negative DAB switch current for free-wheeling action and is therefore challenging. At the test condition in this chapter, it is difficult to prefer one device but the EMI, turn-off loss issues with the IGBT make it less attractive for this power. Howeve a snubber with the 15kV IGBT might make it equivalent to 15kV MOSFET without temperature sensitive $R_{ds}(on)$ problem. Therefore, at higher power for optimized heat sink and temperature design where the conduction losses increase manifold, would shift the focus back to IGBTs.

Chapter 14

Conclusion and Future Tasks

This chapter presents the conclusions of this dissertation, highlights the major contributions and suggests possible future tasks in the area of this dissertation.

14.1 Conclusion of the Dissertation

In-depth design considerations and challenges of a non-cascaded medium-voltage (MV) medium-frequency (MF) DAB converter application using MV devices such as 15 kV SiC IGBTs and MOSFETs have been presented in this dissertation. It helps to understand the limitations of the higher switching speed of the HV SiC devices from high-frequency isolated converter's perspective and its perceived benefit of inversely proportional smaller transformer size. A composite three-phase Y:Y/Δ DAB topology has been selected based on efficiency, reliability, smaller stress on the MV device & transformer and flexible control features. Extensive simulations considering ideal and parasitic model have been completed with important parameter's sensitivity analysis to come to the specifications of an optimum MV-HF transformer and the required DAB inductors. The optimum design helps to reach a feasible development of the transformer and inductor by the external agency. The development of FPGA based ultra-fast ADC interface board has been completed and the proposed d-q control of DAB has been implemented for flexible and fast current control keeping in view the 15 kV SiC IGBT based DAB requirements. For voltage imbalance in the NPC converter mid-point due to mismatched parasitics, there is a corrective control implemented to actively balance it. The implemented control has been successfully tested on a 400 V low-voltage (LV) setup both with voltage & inner current control and on the final MV DAB setup up to 8 kV final dc voltage with just voltage control due to interaction with other TIPS cascaded closed loop systems.

The transformer high-frequency sweep impedance measurement and spice simulations help to synthesize an equivalent circuit model of the MV-HF transformer. This model has been verified with trans-

former converter excitation tests and matches with simulations. It is used in extensive system level simulations to predict ZVS limitations and TIPS system common-mode considerations. The modeling of the DAB as a plant considering the transformer parasitic model has been completed. It has been observed based on the frequency plot of the transfer-function model that parasitics do not directly affect the control performance but there is indirect effect on ZVS performance of the HV SiC based converter. The parasitic emulation in the LV DAB setup has resulted in experimental transformer-waveforms same as the MV simulation waveforms, when all the parasitic capacitances are connected similar to the MV-HF equivalent circuit model. The inter-winding common-mode (CM) capacitance has also been scaled and emulated in LV TIPS setup with all three converters to understand grounding and EMI problems. The CM chokes block their expected CM voltage and pass only the fundamental currents.

The neutral-point-clamped (NPC) three-level converter pole test at the MV with and without lagging current highlight the importance of ZVS operation. The non-ZVS causes inflated turn-on losses and EMI generation confirmed with gate-driver trips in case of non-ZVS mode. From DAB experiments at MV, it is verified that device parasitics limit ZVS range as they need higher negative MV converter current before turn-on instant of the top switch to discharge its capacitance during dead-time even at light load. Transformer parasitics cause MV converter current ringing that makes the negative MV current uncertain by a margin proportional to p-p ringing magnitude, this also limits ZVS range. The larger dead-time and narrower NPC converter duty-ratio also limit ZVS range as the negative current should be extended to this extra duration to keep turning-on device voltage firmly zero, otherwise there is uncertainty for floating case. To ensure ZVS in the proposed MV DAB its full d-q control and flexible control of parallel secondary dual converter are utilized. In the first part the i_{sd} reference is generated from i_{sq} look-up table such that i_s vector aligns with an optimum trajectory defined by the ZVS minimum lag angle for the MV converter. This is not implemented in the MV DAB since only voltage control is implemented due to TIPS integration bandwidth requirements. The CM and grounding experiments at the LV TIPS with emulation of transformer parasitics and other CM parameters after scaling are completed and the results are as expected by the simulations. The grounding solution is partially applied for the MV TIPS with only MV dc mid-point grounding using a resistor. This is limited by the experimental facility and use of a variac-transformer for grid generation.

In the later part of the dissertation novel ZVS enforcement techniques are proposed and they are implemented on a simple MV DAHB topology using either 15 kV SiC IGBTs or 10 kV SiC MOSFETs. The series compensation technique experimental results for different series operating modes are compared. As expected from the simulations, the appropriate mode solved the ZVS issue resulting in moderate dv/dt. The MV converter efficiency could only be worst case estimated with simulations. But the advantage of series compensation is visible in the experimental efficiency of rest of the DAB in deviated voltage ratio conditions. Also the d-q control of the DAB has been extended to the DAHB converter as

well to optimize the performance. The benefit of using snubber across the 15kV SiC IGBTs has been extended to the DAHB converter by using a novel series voltage-pulse injection technique using the earlier proposed hardware. The experimental results presented using the implementation validate the technique. The negative current, before turn-on instant of the top device in the hardware experiment, increases due to the applied voltage pulse as expected in simulation. This results in ZVS turn-on even with the added snubber. The turn-off dv/dt decreases in the DAB results for the snubbered 15kV SiC IGBT while still maintaining turn-on ZVS. The switching loss also decrease as noticed from thermal photographs of the 15kV SiC IGBT heatsink in a previously done inductive mode half-bridge converter test.

In the later part of the dissertation, an intelligent gate-driver has been developed that can correct the 15kV SiC IGBT dv/dt since it has a CPLD and local clock to time the dynamic gate resistors as needed. It has been tested on a 10kV SiC MOSFET in a 6kV double-pulse test just for the demonstration purpose. This active gate-driving feature is another way for reducing losses and EMI without complicating the turn-on ZVS in the DAB. This gate-driver has been tested on 5kV high side switching while optically sending critical measurements such as $V_{ds}(on)$ and module temperature to the interface board for ZVS estimation and data-logging. The data have been monitored in the scope outside the HV setup. The optically received 8bit parallel 250kSPS device current measurement is enough to determine safe ZVS margin and it can be used by the main controller for ZVS enforcement but is beyond the scope of this work.

Finally the dissertation compares the 15kV SiC IGBT and 15kV SiC MOSFET based on double-pulse and converter tests for the presented DAB application. The similar NPC converter pole is built and tested in square mode switching up to 10kV dc bus at 10-20kHz. The thermal results and dv/dt seen in the captured results make MOSFET a better choice since it has higher output capacitance from turn-off perspective. But the turn-on ZVS becomes little harder to achieve specially at higher switching frequency as it requires more lagging current as the dv/dt slopes become too flatter as observed from the results. These results highlight the importance of ZVS just like the case with IGBTs. However high dependence of $R_{ds}(on)$ on temperature for MOSFET might make IGBT a better choice for high-operating temperature compact high-power designs. Device capacitance needs to be optimum. The higher value (MOSFET) results in narrow ZVS (turn-on) range and too low (IGBT) results in higher turn-off dv/dt and switching loss. The 15kV IGBT with a small snubber, is a good switch for higher-voltage, higher-power, higher-temperature design converter application. The 5-10kHz range may be optimum. The 15kV MOSFET not necessarily results in higher switching frequency DAB application as reducing dead-time is a challenge given the device capacitance. The 20kHz may be an optimum frequency from the presented experimental results.

14.2 Major Contributions

The major contributions of this dissertation are listed below.

- The main contribution is 8kV-480V dc experimental validation of 15kV SiC IGBT & 1200V SiC MOSFET based medium-voltage DAB switching at 10kHz in TIPS integrated mode with 4.16kV grid-tied AFEC.
- The major contribution is HV SiC devices based simpler non-cascaded 14kV DAB hardware development with all wiring, insulation, sensing and thermal requirements for isolated MV dc-dc high power conversion application. It has been run up to 6kV (v_{dc2} feedback) in standalone mode using boost as power-supply.
- Another major contribution is HV SiC devices based NPC converter pole development, experimental testing and ZVS problem analysis from loss and EMI perspective.
- Another unique contribution is detailed specification of DAB MV-HF Transformer from parasitics perspective.
- The DAB MV-HF transformer characterization and equivalent circuit synthesis are presented with emulation in simulation and low-voltage prototype with parasitics scaling as a major contribution.
- Y:Y/Δ DAB extensive simulations with ideal, practical parameters and parasitics are presented. Alternative HV three phase DABs and transformer arrangement are compared for best solution.
- The L-C ringing of the transformer (300kHz here), causes irregular slower freewheeling and thus limits ZVS in DAB. High L/C ratio using proposed HV filter results in lower magnitude of the current spike and ringing.
- The study of DAB-ZVS range considering dead-time, current ringing, transformer and converter pole parasitic capacitance,duty-ratio and magnetizing current is unique and major contribution.
- Device parasitics combined with transformer parasitics cause voltage imbalance in NPC converter mid-point and there is a corrective control logic implemented for it.
- DAB experimental results are verified both in 400V LV setup both with v_{dc2} and i_{sq} control.
- Modeling of DAB as a plant with parasitics is presented for sinusoidal approximation. It is observed from frequency plot of model that parasitics do not directly affect controls but there may be indirect effect on ZVS.
- Parasitic emulation in LV setup produces experimental results same as HV-simulation results when all parasitic capacitances are lumped at HV side in differential.

- Extensive TIPS simulation with CM chokes and grounding is presented. Parameters are scaled and emulated in LV TIPS setup and integrated after proposed grounding implementation as a unique contribution.
- ZVS extension using a proposed series-compensation on a simple MV DAHB converter is studied with existing transformer and converters to weigh performance.
- Proposed series-injection technique to accommodate snubber across the IGBTs which solves turn-off dv/dt EMI and loss issue.
- IMGD is developed with fast optical data-link feature for implementing ZVS sense with FPGA interface and active/advance gate-driving.
- Comparison of 15kV SiC MOSFET and IGBT for intended DAB application from ZVS, switching-frequency and thermal perspective

14.3 Future Tasks

Below are some possible points for future work in the area of this dissertation. It consists of some modeling and more experimental work

- Device capacitance changing with voltage is difficult to simulate for a converter. Device parasitic capacitance measurement and model in a converter simulation for exact loss and dv/dt emulation
- Mathematical modeling of the ZVS condition with load, device and transformer parasitics
- Model for optimum switching-frequency and dead-time selection for the HV SiC devices
- Increasing the load on the DAB medium-voltage experiment by using a higher power supply
- Series connection of HV sensors for more than 8kV dc bus
- Replacing DAB inductors with higher Q value and smaller parasitics
- Common-mode and EMI implementation

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