ABSTRACT

RAMACHANDRAN, RAMYA. Investigation of Surface States in Gallium Nitride Devices using a New High Frequency Measurement Technique. (Under the direction of Dr. Douglas W. Barlage).

Surface states place a limitation on the high-frequency behavior of Gallium Nitride devices by causing RF dispersion. They are also a source of undesirable $1/f$ noise.

This thesis specifically aims to explore techniques to address known experimental observations of dispersion phenomena of unknown origin in the 1-30 GHz frequency range. A new method to investigate these at high frequencies is proposed. It involves the measurement of $S$-parameters between the drain and source of a GaN $n$-$i$-$n$ structure in the GHz frequency range. The basis of the proposed technique is the assumption that the behavior of surface states and other dispersion phenomena can be isolated by subtracting the behavior of the device from the measured $Y$-parameters.
Investigation of Surface States in Gallium Nitride Devices using a New High Frequency Measurement Technique

by

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A thesis submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

Raleigh

2006

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ACKNOWLEDGMENTS

I would like to firstly thank Dr. Barlage for all the support, advice and good cheer he has afforded me over the past two and a half years. My thanks also to Dr. Johnson and Dr. Kolbas for taking the time to be a part of my committee. I am also grateful to Dr. Maysam Ghovanloo and Dr. Christal Gordon.

Everyone in the research group that I was a part of - Krishnanshu Dandu, Yawei Jin, Lei Ma, Yoganand Saripalli and Chang Zeng - has helped me immensely at some point or the other and taught me a lot along the way. Thanks so much!
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Chapter 1

Introduction

Devices based on wide band gap semiconductor materials are gaining popularity because of the fundamental limitations being faced by highly scaled silicon devices. Gallium nitride and silicon carbide have facilitated the manufacturing of high power microwave transistors which can operate at least till 100 GHz and the X-band respectively.

Some of the basic material properties of GaN that make it a competitive material for microwave transistors are its large energy gap (3.4eV), low dielectric constant (9.5), high thermal conductivity (1.23 W/K-cm) and high breakdown field (2MV/cm) \[1\]. The low dielectric constant of wide band gap materials allows devices made from them to have larger areas for a certain impedance, and hence carry larger RF currents and provide larger power. The high thermal conductivity permits power from the device to be removed easily. Due to the large breakdown field, the device can sustain larger voltages which is required if it must supply high power. Another important feature that motivates the use of these materials for microwave power devices is their ability to operate at high temperatures \[2\].

The two important phenomena that limit the output power performance of nitride-based FETs are:

1. RF Dispersion: The device output power at high frequencies (GHz range) is much lower than that predicted by DC characteristics.

2. Current Collapse: The reduction in DC drain current that occurs when a large
drain to source voltage is applied to the device.

It has been stated that charge on the surface is the most significant contributor to RF dispersion [3]-[4], while current collapse is due to trapping of carriers in deep defects within the device. Moreover, for a device to be viable for microwave systems, an important parameter is the level of low-frequency noise [5] and many GaN-based devices in the past have shown very high levels of $1/f$ noise. This has been attributed to surface or interface traps. Theoretical and electrical experimental studies have determined the presence of at least two traps located near the surface in GaN [6]. However, no technique has been fully developed to explore the electrical interface and surface behavior at GHz frequency range of GaN or any other semiconductor. This work addresses this need to develop techniques of isolating material behavior at this range. A novel method to study surface states using the $S$-parameters of the channel region of an $n-i-n$ structure between 1 and 10 GHz is proposed.

### 1.1 Overview of the Method

The basis of the proposed technique is that the behavior of traps can be isolated by subtracting the behavior of the intrinsic device from the measured parameters. To this end, the method involves measuring the $S$-parameters of the device between the drain and the source. The $S$-parameters are measured between 1 and 10 GHz using a network analyzer. A 3-element model for the device is derived by fitting within the 1-3 GHz frequency range. The difference between the measured $Y$-parameters and the $Y$-parameters of the 3-element model then gives the $Y$-parameters of the traps. The trap $Y$-parameters can then be used in subsequent studies to experimentally explore the nature of the defects.

Measurements are conducted between the drain and source so that the entire channel region can be observed. Further, since the overall capacitance seen in this direction is smaller, more traps per capacitance can be observed. However, this also requires that smaller capacitance (in the fF range) need to be measured. This idea is explained in
further detail in Chapter 3.

The methodology put forward in this thesis uses high frequencies for mainly two reasons: (i) high frequency traps are expected in GaN and these have not been measured so far using MHz-range measurements and (ii) high frequencies are required to measure the capacitances in the fF range. To be able to use lumped models to extract a capacitance from an impedance measurement, it is necessary that $\omega RC \ll 1$ \cite{7}. Fig. 1.1 shows the range of capacitances that can be extracted given that this condition needs to be satisfied, assuming $R$ remains constant.

![Figure 1.1: Log-log plot of the capacitance that can be measured at a particular frequency](image)

This method differs from other methods firstly, in that the 1-10GHz frequency range used to study traps is much higher than what has been reported in literature. Studying traps at this frequency allows for the observation of traps with a shorter lifetime. Literature so far has limited the study of traps to the MHz range. Further, the specific model used to isolate trap behavior from measured parameters is also different, though a similar method has been proposed earlier \cite{8}.
1.2 Organization of this Document

Chapter 2 presents a literature review of surface states and the various experimental methods used to characterize them. The relationship between flicker noise and surface states is also explored.

Chapter 3 describes, in detail, the experimental method proposed and used in this work, along with the analysis of the data from the measurements. Design rules and experimental limitations are also discussed here.

In Chapter 4, the results of the analysis applied on one sample is presented.

Appendix A contains some introductory background information regarding $S$-parameters and high-frequency measurements using a network analyzer.

The results of the analysis on four other devices is included in Appendix B.
Chapter 2

Surface States and their Characterization

The electrical characteristics of a semiconductor device are affected by the quality of the surface and the physical interfaces between the different materials it is manufactured from. The dependence becomes more pronounced for power devices at high frequencies. It is therefore imperative to study the surface properties of materials with regard to their electrical behavior.

This chapter starts by introducing the concept of surface states. It then describes the different methods used to characterize them, as reported in literature. This is followed by a look at flicker noise in circuits and how they are impacted by surface states.

2.1 Surface States - Introduction

Traps, by definition, are energy states within the energy gap where, once a carrier has been captured, the next most probable event is the re-excitation of the carrier to its original state, as opposed to recombination with the opposite carrier. Those states where the next probable event is recombination are called recombination centers.

Surface states are allowed energy states for electrons or holes which exist only at the surface of the semiconductor material, and not within the bulk. They can arise due to two main reasons. Firstly, since the atoms on the surface are spatially bound only from one side, the characteristic energies of electrons would be different from those in the bulk. These states are called Shockley or Tamm states. The other source is the
presence of crystal defects or foreign atoms on the surface, which produces energy levels throughout the bandgap depending on the nature of the bonding [10]. Similarly, at the interface between two materials, there is an interruption of the periodicity of the lattice and this forms interface states.

2.1.1 Classification of Surface States

Surface and interface traps can be classified based on different criteria. Traps that are physically located close to the bulk and can therefore attain equilibrium with it quickly are called ‘fast’, while those that are further away and take longer to reach equilibrium are referred to as ‘slow’.

States that are neutral when occupied by an electron and positively charged when not occupied are called ‘donor’ states. ‘Acceptor’ states are those that are negative when occupied by an electron and neutral when unoccupied.

Yet another classification distinguishes traps as ‘hole traps’ and ‘electron traps’ [11]. Hole traps are those that tend to be filled with electrons from the conduction band and release to the valence band. They have a propensity to capture holes. Similarly electron traps have a propensity to capture electrons. If $e_1$ and $e_2$ are the emission rates for electrons and holes respectively, then the equilibrium electron occupation for a state is given by

$$n_1 = \frac{e_2}{e_1 + e_2} N$$

(2.1)

where $N$ is the concentration of the trap. Therefore, for a hole trap, $e_2 \gg e_1$.

2.2 Surface and Interface Traps in GaN devices

Trapping effects place a direct limitation on the power performance in wide band gap microwave FETs [12]. The traps limit the output current of a device by changing the equilibrium charge distribution in the channel, and hence have a direct impact on the output power. They cause a difference in the drain current response between DC and RF inputs. In this section, we look at the important trapping effects in GaN power
devices and what experiments can be conducted to measure them. We also try and understand the location of the traps and the methods that may be used to minimize them.

2.2.1 Location of Traps

The possible spatial locations of traps in GaN devices are (i) the surface, (ii) the AlGaN barrier layer, (iii) the 2-D electron gas interface and (iv) the GaN buffer layer. Of these, the traps that affect the microwave power performance most are the ones at the surface and the buffer layers. A direct correlation between the other two with performance has not been established yet. Further, active trapping centers exist near dislocations in the material. However, even though the dislocation density in nitrides is very high, no direct link with specific traps has been proven [12].

Since GaN has a hexagonal crystal structure, it is more susceptible to surface effects because the polarity effects cause coupling of surface traps to the 2-D electron gas.

2.2.2 Effects of Trapping Phenomena

Transconductance frequency dispersion, current collapse, gate and drain lag transients and limited microwave power delivery are some of the important effects of trapping.

Current Collapse

Current collapse is defined as “the persistent, yet recoverable, reduction of DC drain current as a result of the application of high drain bias” [12]. It happens because high drain-source ($V_{ds}$) voltage causes hot carriers to get injected into the regions in the channel close to the drain where they get trapped. This reduces the number of carriers available for current delivery and hence the output power [13]. Negative gate bias can also cause current collapse [14].

Similar effects are seen in Si MOSFETs. The traps responsible for current collapse
have been found to exist in the GaN buffer layer, and in HEMTs at the AlGaN-GaN interface, in the AlGaN layer or at the surface [15].

Current collapse in a HEMT has been envisioned to be a result of the charging up of a reverse biased ‘virtual gate’ located in the gate-drain access region as in Fig. 2.1 [3]. Since passivation of the surface of the device using SiN$_4$ decreased the collapse, it was concluded that the traps responsible for this are located on the surface. Passivation helps by preventing the positive charge sheet at the surface from getting compensated.

![Figure 2.1: Model of a HEMT showing the location of the virtual gate and schematic representation [3]](image)

Light illumination has been found to help in the recovery from current collapse. Also, thermal emission from deep traps have been observed. Both these have been found to have a time dependence. The wavelength dependence of the recovery using photoionization spectrum suggests the presence of two distinct traps – Trap 1 at 1.8eV below the conduction band and Trap 2 at 2.85eV [16]. Trap 1 is related to structural defects such as dislocations and grain boundaries and Trap 2 is related to carbon concentration [12].

In contrast to these observations, [14] suggests the presence of traps below 1eV. Recovery from current collapse with illumination has been confirmed even with the use of light with energy smaller than the bandgap. This is due to release of electrons from surface states which leads to an increase in the density of the 2DEG in the HEMT. Further studies performed by the authors included focusing light on specific regions of the device. This showed that most traps were located in the gate-drain region as compared to the gate-source region, since more recovery was observed in the former
Gate and Drain Lag Transients

Gate and drain lag transients refer to the response of drain current to gate and drain voltage pulses. They lead to pulse narrowing and inaccurate switching. Gate lag is caused by surface traps near the edges of the gate while drain lag is caused by substrate traps in buffer layer [12].

Gate lag measurements are conducted after doing surface treatment. Annealing of unpassivated devices reduces gate lag and transconductance dispersion. SiN$_4$ passivation decreases gate lag by creating an optimal interface between the dielectric and the semiconductor which is relatively free from surface defects, dangling bonds, adsorbed ions and charged residuals. Gate lag measurements at high frequencies show that drain current compression is due to traps in the AlGaN barrier or the surface, and not the buffer layer.

Drain current transient measurements are often used to study trapping effects because unlike capacitance measurements which provide information about the region under the gate, these are sensitive to the whole length of the channel. Drain lag measurements can be used to find time dependence of recovery from current collapse by thermal emission. $V_{ds}$ is pulsed from 0–15 V or 20–0 V while $V_{gs}$ is maintained at 0 V. The high $V_{ds}$ causes current collapse and the time to recover from it (which is of the order of minutes) is measured.

Like current collapse, drain lag also has been found to be related to the conductivity of buffer. Three traps with different time constants were identified by [17] – intermediate time (~10s), fast (~1s) and slow (> 100s).

Transconductance and Output Conductance Dispersion

Transconductance ($g_m$) dispersion has been attributed to trapping at/near the surface, while output conductance (or equivalently, $R_o$) dispersion is caused by trapping below the active channel [18].
Two energy levels located in GaN channel were identified to be responsible for these two phenomena. One is a Si donor in AlGaN, and the other is either the surface states near drain or at AlGaN/GaN interface [8].

**Power Drift and Power Slump**

Power drift is defined as a recoverable reduction in power output over time. On the other hand, power slump is a permanent reduction in output power. They have been found to be related to the degree of gate lag. Both are believed to be caused by electron trapping in the SiN$_4$ passivation layer or by the creation of interface traps due to hot-electron effects [19].

### 2.2.3 Optimal Power Performance

The following steps may help in obtaining optimal power performance in GaN microwave devices:

1. Surface passivation
2. Reduction of peak fields in the channel (near the drain) to minimize hot electron effects
3. Improvement in the quality of epitaxial materials
4. Optimization of epitaxial and gate recess structures
5. Change in channel doping and geometry. For instance, use of moderate to high doping near gate edge can reduce gate lag

The technique presented in this work is meant to be a way to accurately quantify progress in limiting the deleterious effects of these traps by using these methods.

### 2.2.4 Other Performance-Limiting Factors

One of the important factors which limits the performance of a GaN device at high frequencies is the modulation of the source region which causes the source resistance to
change with RF drive and current [1]. The source resistance is highest when the voltage is high and current is low. This forces the resistance of the device to increase and its dynamic load line tends towards the horizontal as the frequency increases. This degrades the RF swing of the device at higher frequencies.

As mentioned earlier, one of the most attractive features of wide bandgap materials is their high breakdown voltage. However, it has been observed in AlGaAs/GaAs HEMTs as well as GaN MESFETs that RF breakdown is significantly lower than DC breakdown [1]. The result of this breakdown would be a distortion in the dynamic load line and RF performance.

2.3 Characterization of Traps

In order to completely characterize a trap, it is necessary to quantify the concentration, the energy levels, the cross-sections for capture of carriers and the thermal emission rates [20]. This section details the various techniques reported in literature to characterize some or all of the above features of surface states in GaN and GaAs-based devices. These techniques may be broadly classified as time-domain (or transient) techniques and frequency-domain techniques.

2.3.1 Time-domain Techniques

The most important time-domain technique to characterize traps is Deep-Level Transient Spectroscopy or DLTS. There have been many variants and modifications of DLTS that have been developed since DLTS was first introduced [11]. These include techniques to characterize states in MOS capacitors [21], semiconductor alloys [22] and devices using novel materials including GaN [23]. Since DLTS is wide-spread in its use, this section starts with a look at DLTS, followed by other time-domain techniques.
Overview of DLTS

Deep-Level Transient Spectroscopy is a basic, yet powerful high-frequency transient measurement technique which can be used to observe and quantify various properties of traps in semiconductors [11]. It is a capacitance thermal scanning method and can indicate the location and concentration of a trap, in addition to facilitating the measurement of activation energy, concentration profile and carrier capture cross-sections for each trap.

The basis of DLTS is capacitance transient measurements. In such measurements, the characteristics of the capacitance transient associated with returning to thermal equilibrium after a pulse is studied. A bias pulse introduces carriers and changes the occupation of a trap by carriers from the steady-state value and thereby causes a change in capacitance. When the bias is removed, the carriers return to their steady state and the capacitance also returns as an exponential function of time. The sign of the capacitance change indicates whether the occupation of a trap by electrons has been increased or decreased by the pulse. Therefore, the pulse itself can be classified as an injection (minority-carrier) pulse which introduces minority carriers into the system, or a majority-carrier pulse which introduces majority carriers. The time constant of the transient as a function of temperature is related to the activation energy of the trap. The capacitance change corresponding to completely filling a trap with an injection pulse gives the concentration of a trap. For instance, for an $n^+p$ junction,

$$N = 2\frac{\Delta C}{C}(N_A - N_D) \quad (2.2)$$

where $N$ is the trap concentration, $\Delta C$ is the change in capacitance at the instant that the pulse is applied, $C$ is the capacitance under steady-state conditions and $N_A - N_D$ is the net acceptor concentration on the $p$ side of the junction.

DLTS sets an emission rate window so that the system only responds when a transient with a rate within this window is applied. This emission rate window for low-field carriers is related to temperature by the following equation and can be set by varying
the temperature of the sample.

\[ e_1 = \frac{\sigma_1 v_1 N_{D1}}{g_1} e^{-\Delta E/kT} \]  

(2.3)

where \( \sigma_1 \) is the minority carrier cross section, \( v_1 \) is the mean thermal velocity of the carriers, \( N_{D1} \) is the effective density of states in the minority-carrier band, \( g_1 \) is the degeneracy of the trap level and \( \Delta E \) is the energy difference between the trap level and the minority-carrier band. \( k \) is the Boltzmann constant and \( T \) is the temperature. A similar equation can be written for the majority carriers. The slope of the straight line plot of \( \log(e_1) \) or \( \log(e_2) \) versus \( 1/T \) gives the activation energy of the trap.

Another method is possible to determine the activation energy. The instantaneous value of the capacitance transient at two times \( t_1 \) and \( t_2 \) as the temperature is varied is recorded. The difference between these capacitances (i.e., \( C(t_2) - C(t_1) \)) is plotted as a function of temperature. This curve goes through a maximum for a particular trap at time \( \tau_{max} \) given by

\[ \tau_{max} = \frac{t_1 - t_2}{\ln(t_1/t_2)} \]  

(2.4)

Thus, at the maximum of the \( C(t_2) - C(t_1) \) curve, the temperature can be recorded and \( \tau_{max} \) calculated to get a point on the \( \log(e_1) \) versus \( 1/T \) curve. Other values of \( t_1 \) and \( t_2 \) can be used to obtain other points on the curve, thus establishing the activation energy. Eq. (2.2) gives the trap concentration.

Concentration profiles and capture rates are other parameters that can be extracted from DLTS measurements.

**Other time-domain Techniques**

The effect of light and temperature on traps using time-domain techniques is described in [24]. The GaN MESFETs in the study are subject to pulse and static measurements. For static measurements, the \( V_{gs} \) is varied in steps of 2V between \(-9V\) and \(1V\) and the drain current is measured with respect to \( V_{ds} \). For the pulsed measurements, \( V_{ds} \) is varied from \(0\) to \(18V\) at a frequency of \(100kHz\). The difference in the drain current
between the static and the pulsed measurements is attributed to the presence of traps in the GaN material or on the surface. This is because the trapped electrons do not have enough time to respond to the 100kHz pulse. Further, a difference in the magnitude of the drain current is observed when the static and pulsed measurements are carried out in the absence of light as compared to when it is conducted in the presence of light. The increased current in the presence of light indicates that the carriers are detrapped by the light. Similarly, higher temperatures (150°C) also caused the carriers to be freed, thereby increasing the current.

The authors also present an equation for the threshold voltage $V_t$ of the device

$$V_t = V_{bi} - q(N_d + N_t)a^2/2\epsilon$$

where $V_{bi}$ is the built-in voltage, $q$ is the electronic charge, $N_d$ is the bulk doping, $N_t$ is the trap density, $\epsilon$ is the dielectric constant and $a$ is the active layer thickness. It is argued that traps which are in the material or the buffer would increase $N_t$ under pulsed conditions in comparison with static conditions, thereby decreasing $V_t$. However, since $V_t$ did not change, it is argued that the traps are located at the surface.

### 2.3.2 Frequency-domain Techniques

**Measurement of Output Impedance**

The output impedance of FETs determines their performance in microwave circuits such as mixers, ADCs, oscillators and amplifier. The variation of output (drain-source) impedance with frequency, bias or temperature affects the performance of devices and must be accounted for during design and incorporated into device models. The frequency dispersion of output impedance is chiefly observed in saturated devices at frequencies below 10MHz and they are brought about by deep-level interface traps [25].

The variation of the output impedance of AlGaAs/InGaAs/GaAs PHEMTs with frequency is studied in [26]. The dispersion of the output impedance with frequency increases with temperature. The reactance first exhibits a minimum (capacitive nature)
and then a maximum (inductive nature) as the frequency is increased. These frequencies are also seen to increase with temperature. These observations indicate that there are two trapping mechanisms exhibited by these devices.

\[
\tau = \frac{1}{2\pi f_m} = \frac{1}{T^2} e^{E_a/kT}
\]

(2.6)

where \( \tau \) is the time constant, \( f_m \) is either the frequency at which the minimum or maximum reactance occurs and \( E_a \) is the activation energy of the corresponding trap. Using this equation, \( \tau T^2 \) is plotted against \( 1000/T \) and \( E_a \) of the two traps was determined to be 0.61eV and 0.82eV. Up to 1MHz, the trapping of hot electrons in these two traps is thought to be responsible for the output impedance dispersion.

Trapping phenomena in AlGaN/GaN MODFETs has been studied over a frequency range of 20Hz to 1MHz and a temperature range of 77 to 150K [8]. \( V_{ds} \) was maintained at 2.5 or 5V, and \( V_{gs} \) at −1 or 0V (the threshold voltage of the devices at room temperature was found to be approximately −2V). Low temperature measurements are conducted since they are more sensitive to shallow traps that affect device reliability and microwave performance.

A simplified empirical circuit model for output admittance dispersion is presented as in Fig. 2.2.

![Empirical model for output impedance dispersion](image)

**Figure 2.2:** Empirical model for output impedance dispersion

The output admittance \( Y_o(\omega) \) of the FET as a function of frequency is then given
by
\[ Y_\omega(\omega) = \left[ g_o + \frac{\omega^2 C_T/\omega_c}{1 + (\omega/\omega_c)^2} \right] + j \left[ \omega C_o + \frac{\omega C_T}{1 + (\omega/\omega_c)^2} \right] \] (2.7)

where \( g_o, C_o \) and \( C_T \) are the conductance and capacitances from the model. \( g_o \) represents the drain-source leakage and channel modulation effects, \( C_o \) represents the gate-drain and gate-source capacitance, and \( R_T C_T \) represents a single trapping center with time constant \( \tau = R_T C_T \). The characteristic frequency \( f_c \) is the frequency at which the susceptance reaches a local maximum, or can be found as a best fit to the measured conductance and susceptance curves at a particular temperature. It is given by \( f_c = 1/\tau \). Upon finding \( f_c \) by this method, the activation energy \( E_a \) and apparent capture cross-section \( \sigma \) can be found by knowing that \( f_c \) is related to the emission rate of the charge-trapping center and therefore follows the Arrhenius dependence.

\[ f_c = \sigma v_{th} N_c e^{-E_a/kT} = A T^2 e^{-E_a/kT} \] (2.8)

where \( v_{th} \) is the mean thermal velocity and \( N_c \) is the effective density of states in the conduction band. This equation is used to obtain an Arrhenius plot of \( \ln(f_c/T^2) \) versus \( 1/kT \).

Similar experiments can be performed at higher temperatures and information about deeper traps can be extracted.

**Measurement of Transconductance**

The transconductance \( g_m \) is the rate of change of drain current with respect to the gate voltage. The resistance of the source-gate and source-drain areas of a FET depends on the depth of the depletion region here. This is, in turn, dependent on the occupied surface state density. Therefore, if the surface state density is dependent on frequency, so is \( g_m \) [27].

The dispersion of transconductance has been used to identify traps in the gate-drain region of AlGaAs/GaAs HEMTs [28]. Dispersion of \( g_m \) at low frequencies is attributed to electron trapping, but at high frequencies, \( g_m \) drops because the electron emission
from the traps is too slow to follow the gate voltage. The authors report results from reliability testing at high $V_{ds}$. Drain current is seen to decrease and the drain parasitic resistance is seen to increase rapidly during these tests. Eq. (2.8) is used to calculate the activation energy and apparent cross-section of the traps.

In conclusion, it is important to note that at frequencies that are small compared to the characteristic frequency, the surface traps are able to follow the applied voltage signal. But at higher frequencies, since they are unable to respond instantaneously to the voltage, the charge in the surface states appears to be static. However, even though these traps cannot respond to signals at microwave frequencies, they affect the behavior of devices at high frequencies because the equivalent circuit of the device is determined by the position and size of its overall depletion layer at a given bias condition [27].

2.3.3 Capacitance Measurements in MOS devices

In the MOS domain, a different technique is used to model the devices. Lonnum and Johannessen describe a new measurement technique to quantify carrier density in very leaky Schottky-barrier devices [29]. The conventional C/V profiling is not useful in these cases because of the presence of parasitic series and parallel resistances. A small-signal equivalent circuit model which accounts for these parasitics is presented as in Fig. 2.3 - $R_s$ and $R_p$ are the series and parallel parasitic resistances, while $C$ is the frequency-independent capacitance.

![3-element model](image)

**Figure 2.3:** 3-element model
In order to find the values of all three components, it is necessary to measure the impedance $Z$, as opposed to just the capacitance at two frequencies. It is important to note that $R_s$, $R_p$ and $C$ are bias-dependent. From the equivalent circuit, the impedance can be calculated as

$$Z = |Z|e^{j\phi} = \frac{\omega R_p^2 C}{1 + \omega^2 R_p^2 C^2}(\cot \phi - j) = K(\omega)(\cot \phi - j)$$

(2.9)

where

$$\cot \phi = \frac{R_s + R_p + \omega^2 R_s R_p^2 C^2}{\omega^2 R_p^2 C}$$

(2.10)

Now, the magnitude of the imaginary component of $Z$ can be expressed as

$$|\text{im}(Z)| = |Z|\sin \phi = \frac{\omega R_p^2 C}{1 + \omega^2 R_p^2 C^2} = K(\omega)$$

(2.11)

Therefore, by measuring $Z$ and $\phi$ at two different frequencies $\omega_1$ and $\omega_2$, $K(\omega_1)$ and $K(\omega_2)$ are obtained as $|Z_1|\sin(\phi_1)$ and $|Z_2|\sin(\phi_2)$ respectively. From this, the three parameters are derived as

$$C = \frac{\omega_2 |Z_2|\sin \phi_2 - \omega_1 |Z_1|\sin \phi_1}{\omega_2^2 - \omega_1^2}$$

(2.12)

$$R_p = \frac{1}{\omega C} \cdot \left| \frac{|Z|\sin \phi}{1 - \omega C|Z|\sin \phi} \right|^{1/2}$$

(2.13)

$$R_s = |Z|\cos \phi - \frac{R_p}{1 + \omega^2 R_p^2 C^2}$$

(2.14)

The experiments were conducted at 1MHz and 2MHz on GaAs MMIC prototypes and carrier density and depletion depth were calculated from these measurements.

This same method has been used to characterize a MOS capacitor with a leaky gate oxide [30]. Here, $R_p$ is the effective device resistance due to tunneling through the oxide and $R_s$ is the series resistance of the substrate and gate. This measurement method
eliminates the frequency dependence of the measured capacitance.

The impedance can be measured assuming a parallel RC model as in Fig. 2.4.

\[ Z = \frac{D' - j}{\omega C'(1 + D'^2)} \]  

(2.15)

where \( R' \) is the measured resistance, \( C' \) is the measured capacitance and \( D' = \frac{1}{\omega R'C} \) is the dissipation.

However, using the three-element model as shown earlier in Fig. 2.3, the ‘true’ impedance is given by:

\[ Z = R_s + \frac{R_p(1 - j\omega CR_p)}{1 + \omega^2 C^2 R_p^2} \]  

(2.16)

Equating the imaginary part of Eq. (2.15) and Eq. (2.16) gives:

\[ \frac{1 + \omega^2 C^2 R_p^2}{C R_p^2} = \omega^2 C'(1 + D'^2) \]  

(2.17)

Measuring \( C' \) and \( D' \) at two frequencies (at the same bias) and substituting in Eq. (2.17) gives the frequency-independent capacitance \( C \) as:

\[ C = \frac{f_1^2 C'_1(1 + D'_1^2) - f_2^2 C'_2(1 + D'_2^2)}{f_1^2 - f_2^2} \]  

(2.18)
Similarly, working with the real part of the equation gives $R_s$ and $R_p$:

$$R_p = \frac{1}{\omega^2 C' C (1 + D')^2 - \omega^2 C^2}^{1/2}$$  \hspace{1cm} (2.19)

$$R_s = \frac{D'}{\omega C'' (1 + D')^2} - \frac{R_p}{1 + \omega^2 C^2 R_p^2}$$  \hspace{1cm} (2.20)

### 2.3.4 Use of Conductance and Capacitance Measurements

Characterization of traps using equivalent circuit models is a common technique and has been used on MOS capacitors and GaAs devices [31].

The trapping-detrapping process leads to a loss of free energy which manifests itself as a change in conductance and the change in charge storage of the states causes a change in capacitance. Trap studies have also been conducted by measuring the conductance and capacitance between the drain and gate of an AlGaN/GaN HFET [7]. These measurements were conducted with respect to frequency and gate bias, and the approximate time constant and density of traps was established.

The experimental procedure for such methods essentially involves measuring the impedance between the two terminals at different frequencies and values of bias. The measured impedance is then modeled by a simplified equivalent circuit depending on the device being characterized. The HFET is modeled as shown in Fig. 2.5.

![Figure 2.5: Measurement circuit, actual equivalent circuit and simplified equivalent circuit to extract trap parameters](image)
In the actual model, $C_s$ is the capacitance of the spacer layer and $C_{it}$ and $R_{it}$ are the capacitance and resistive loss terms associated with the traps. In the simplified model, the barrier capacitance $C_b$ and the series resistance of the drain contact $R_s$ are separately measured. The values of $C_p$ and $G_p$ are then obtained from $C_b$ and $R_s$, and the measured conductance and capacitance $C_m$ and $G_m$ by comparing the two circuits. The interface trap density $D_{it}$ and time constant $\tau$ can be calculated by plotting $C_p$ and $G_p$ as functions of frequency and fitting them to the AC response of the actual equivalent circuit.

For traps at a single level, $C_p$ and $G_p/\omega$ are given by

$$C_p = C_s + \frac{C_{it}}{1 + \left(\frac{\omega \tau}{2}\right)^2}$$

$$G_p = q \frac{\omega \tau D_{it}}{1 + \left(\frac{\omega \tau}{2}\right)^2}$$

(2.21)

For traps at a continuum of level, the expressions are

$$C_p = C_s + \frac{C_{it}}{\omega \tau \tan(\omega \tau)}$$

$$G_p = \frac{q D_{it}}{2 \omega \tau} \ln \left[1 + \left(\frac{\omega \tau}{2}\right)^2\right]$$

(2.22)

### 2.4 Flicker Noise

Low-frequency noise is an important parameter in microwave systems and flicker noise which manifests itself at low frequencies is an important figure of merit. It limits the phase noise factor for all transistors, and hence needs to be taken into account in circuits, especially phase-noise amplifiers [32].

Studies have shown that the main sources of flicker noise are material defects and certain localized states which act as trapping and detrapping centers. Changes in the occupancy of surface states due to trapping and detrapping of carriers is an important contributor to flicker noise [33].
2.4.1 Definition

Flicker noise or $1/f$ noise has the property that its spectral density increases without limit as frequency decreases. The noise power follows a $1/f^\alpha$ characteristic with $\alpha$ varying from 0.8 to 1.3, with the most common value being 1. Integrating over the range of frequencies of interest, the noise power is given by

$$N_f = K f \int \frac{df}{f} = K f \ln \frac{f_h}{f_l}$$

(2.23)

where $f_h$ and $f_l$ are the upper and lower frequencies of interest and $K$ is a constant.

It must be noted that all low-frequency noise is not flicker noise. Generation-recombination noise or $G$-$R$ noise is also an important contributing factor. $G$-$R$ noise is different from $1/f$ noise in that it arises from discrete trap energy states. $1/f$ noise arises from excitation of carriers from traps at a broad distribution of energy levels. The $G$-$R$ noise causes multiple bumps in the noise energy spectrum. However, if the $G$-$R$ traps are sufficiently close in energy, they resemble a $1/f$ spectrum.

2.4.2 Modeling of Flicker Noise

Flicker Noise in a Diode

SPICE uses diodes to generate flicker noise and it calculates the noise current in a diode as

$$I_d^2 = K F \left( I_{dc}^{AF} \right) \frac{f}{f} + 2qI_{dc}$$

(2.24)

where $KF$ is the flicker noise coefficient, $AF$ is the flicker noise exponent and $I_{dc}$ is the DC bias current through the diode.

Flicker Noise in BJTs

In bipolar junction transistors (BJTs), the two important sources of flicker noise are 
(a) defects and contamination in the semiconductor material and (b) recombination of carriers in the base-emitter junction of bipolar transistors. The spectral noise density of
flicker noise in BJTs $I_{nf}^2$ is given by

$$I_{nf}^2 = \frac{2qI_{dc}f_c^mB}{f} \quad (2.25)$$

where $I_{dc}$ is the DC current, $f_c$ is the corner frequency, $B$ is the bandwidth and the exponent $m$ has a value between 1 and 2.

**Flicker Noise in FETs**

The important noise sources in Field Effect Transistors (FETs) are gate leakage current, contact noise, bulk noise, surface noise and the fluctuations of the Schottky barrier region [36].

In Junction-FETs, the trapping centers are in the depletion region.

In MOSFETs, $1/f$ noise is generated by the trapping of carriers in energy states in the oxide interface and gate region. The spectral density is given by

$$I_{nf}^2 = K_FI_{DQ}^2A_FfC_{ox}L^2 \quad (2.26)$$

where $I_{DQ}$ is the quiescent drain current and $L$ is the effective channel length.

**Flicker Noise in a GaAs devices**

GaAs devices are generally observed to be less noisy than Si devices at high frequencies, but more noisy at lower frequencies (below 1MHz). Further, since GaAs devices so far have been optimized only for digital and RF applications where $1/f$ noise is not a major concern, they remain poor in this aspect. However, smaller device sizes have made $1/f$ noise levels higher. It can also be noted that none of the different GaAs FET structures have striking advantages over the others as far as $1/f$ noise is concerned [33].
2.4.3 Relationship between Flicker Noise and Surface States

Experimental evidence relating the $1/f$ noise spectrum and interface state density in MOSFETs was first presented by Sah and Hielscher [37]. A one-to-one proportional relationship was observed between the density of surface states at the Si-SiO$_2$ interface and the $1/f$ noise power referred to the gate. A correlation was also observed between the noise and the real part of the gate impedance. The surface state density as well as the noise power were found to be heavily dependent on the fabrication process and quality of the interface.

The relationship of $1/f$ noise to surface state density has also been studied by measuring channel conductance of a MOSFET under strong inversion as a function of gate charge [38]. The proportionality between surface state density at the Fermi level and $1/f$ noise is confirmed and this density is established as a unique parameter in quantifying $1/f$ noise.

The spectral density of the noise arising from surface defects has been modeled as

$$
\frac{S_{ld}}{I_d^2} = \frac{S_{Rds}}{R_{ds}^2} \frac{R_{ds}^2}{(R_{ds} + R_{ch})^2} \tag{2.27}
$$

where $R_{ch}$ is the channel resistance which varies with the gate-source voltage, $R_{ds} = R_d + R_s$ is the resistance of the gate-source and drain-source regions, and $S_{Rds}$ is the spectral noise density [36].

$1/f$ noise has only an indirect relationship with temperature – the surface-state density, and thus $1/f$ noise, is affected by temperature. The noise is found to decrease with increasing temperature. As long as the transistor is in strong inversion, the noise remains constant at a given frequency since the surface potential does not change much with gate bias [38].

The Hooge parameter $\alpha$ is often used to characterize the noise level in different materials and structures. It is given by

$$
\alpha = \frac{S_f}{I^2} f N \tag{2.28}
$$
where $N$ is the total number of conduction electrons and $S_1/I^2$ is the relative spectral density of the noise. Desirable values of $\alpha$ for commercial applications is $10^{-4} - 10^{-5}$ [5].
Chapter 3

Experiment and Analysis Methodology

Surface states and existing methods to characterize them have been described in detail in Chapter 2. This chapter now explains the new method proposed by this work to measure surface states. It starts with a description of the fabrication and expected electrical properties of the device under test. The measurement methodology and the analysis of the data obtained from measurements is then described. This is followed by a look at the advantages and limitations of this technique.

3.1 Fabrication and Structure of the Devices

The experiments were conducted on GaN $n$-$i$-$n$ structures. This structure is a critical part of a fully depleted MOSFET and is often used to evaluate the quality of the regrown region.

3.1.1 Process Flow

The cross-sectional view of the device is shown in Fig. 3.1. The process flow is as follows:

1. Channel formation: $i$-GaN, $p$-GaN and $n$-GaN are grown on C-oriented sapphire substrates using Metal-Organic Chemical Vapor Deposition (MOCVD). An AlN buffer layer is first grown at low temperatures to promote two-dimensional nucleation, and a channel is grown on top of this buffer layer.
2. Mesa formation using metal mask/Photolithography Level 1: In this first post-growth step to isolate the channel, mesa mask is used. Prior to photolithography, the sample is cleaned and baked. 5nm chromium and 200nm nickel is deposited and then lifted off in acetone.

3. Identification of the mesa: Ni and Cr are used to identify the mesa. The GaN is etched using Plasmatherm Reactive Ion Etching (RIE) using boron trichloride.

4. Removal of metal: Ni and Cr are removed in remover solution. Ni etch contains nitric acid, and Cr etch contains perchloric acid and ceric ammonium nitrate.

5. Photolithography Level 2: The ohmic contact region is identified. Then, 165nm of ohmic metal Ti-Al-Mo-Au is deposited in e-beam and lifted off in acetone. This is followed by Rapid Thermal Annealing (RTA) at 850°C for 60s.

6. Photolithography Level 3: A gate mask is used to put down 1.4µm length gate metal - 200nm of Ni. This is done using e-beam and then lifted off in acetone.

7. Photolithography Level 4: An interconnect metal pad is put down for measurement.

**Figure 3.1:** Cross-sectional view of the fabricated n-i-n structure
purposes using an interconnect mask. 5-15nm of Ni and 200-500nm gold are put down using e-beam and then lifted off in acetone.

3.1.2 Structure of the Device

Figs. 3.2 [39], 3.3 and 3.4 [40] are the SEM images of the $n$-$i$-$n$ structure which were used for measurements. Note that the gate is not formed on these devices.

![Figure 3.2](image_url)

**Figure 3.2**: SEM micro-graph showing the layout of the $n$-$i$-$n$ structure

As described in the next section, during measurement, the Ground-Source-Ground (G-S-G) probe used grounds the source contacts and measures the signal at the drain.

3.1.3 Electrical Characteristics

$n$-$i$-$n$ structures exhibit space-charge-limited transport and the I-V characteristics are given by the Mott-Gurney limit which indicates a direct square-law relationship between current and voltage.

\[
J = \frac{9\varepsilon_s \mu_n V_d \sqrt{\frac{2}{3L^3}}} \]

(3.1)
Figure 3.3: SEM image of the \textit{n-i-n} structure - top view

Figure 3.4: SEM image of the \textit{n-i-n} structure - tilted view
The measured I-V characteristic of a typical \( n-i-n \) structure in the presence and absence of illumination is shown in Fig. 3.5.

![Figure 3.5: Measured DC characteristics of a typical \( n-i-n \) structure](image)

**Figure 3.5:** Measured DC characteristics of a typical \( n-i-n \) structure

### 3.2 Experiment Method

The Scattering or \( S \)-parameters of the devices were measured using the Network Analyzer HP8510. G-S-G probes from Picoprobe were used to make contact with the drain and source. The set-up was calibrated before use every time in order to remove systematic errors (see Appendix A). DC bias was provided from the Source Measure Unit (SMU) HP4142B connected to the probes using bias tees.

A LabVIEW (National Instruments) program was used to control the SMU and Network Analyzer from a PC. The bias to each of the ports can be controlled independently and the \( S \)-parameters recorded for any desired value of bias. The \( S \)-parameters were saved in Touchstone format. These are read into Agilent Advanced Design System (ADS) using the Data File Tool and can be plotted as Smith chart, logmag, phase and other formats.
The Touchstone format used saves the 2-port $S$-parameter data as a tab-delimited text file with the real and imaginary parts of each of the four $S$-parameters with respect to frequency. This allows easy export into Excel where further analysis of the data was conducted.

For $n$-$i$-$n$ structures with no gate, the $S$-parameters were measured only at the drain. Only data from Port 2 ($S_{22}$, the reflection coefficient from the drain to the source) is used in the analysis, over various values of drain bias $V_d$. Fig. 3.6 shows the position of the probes with respect to the device at the time that the measurements were taken.

![Figure 3.6: Location of the probes during measurement](image)

The frequency range of measurement was 45MHz to 10GHz. $V_d$ was varied from $-15$V to 15V in steps of 5V. These measurements were conducted both in the presence and absence of light. The light source was the light from the microscope bulb. It is surmised that in the presence of light, the carriers are detrapped to the conduction band, while they remain trapped in the absence of light. As can be seen in Fig. 3.5, in the presence of light, the drain current of the device is slightly more than that in the absence of light. This is an indication of trapping - in the absence of light, there are fewer carriers available to participate in current conduction.
3.3 Analysis of the Data

A parallel two-element model and a three-element model were derived for each device for each bias condition, in the presence and absence of light. This section describes the derivation of these models.

Verification of data

Before modeling of the device is described in detail, a quick verification of the data obtained from the Network Analyzer is in order. To ensure that there is little drift in the measurements over time, the S-parameters of known resistances are measured. Fig. 3.7 shows the resistance measured by the Network Analyzer on a standard 50Ω and 100Ω on the calibration substrate at different times, 30 minutes apart, within the same calibration. These measurements were also conducted between 45MHz and 10GHz.

![Figure 3.7: Measured resistance of a standard 50Ω and 100Ω at times t1 and t2](image)

Figure 3.7: Measured resistance of a standard 50Ω and 100Ω at times t1 and t2

From this, we can note that there is likely to be a maximum of 4% error in the measurement. This is because the Network Analyzer is most prone to error around 50Ω. Further away from the center of the Smith Chart, it becomes less sensitive, and shows
less error. The variation over frequency is similar for the two measurements at the same
time. This indicates that though the overall values of the measurement can be trusted,
at this point, the slight variations over frequency may only be remnants of measurement.

### 3.3.1 Two-element Model

S-parameters are related to the reflection and transmission coefficients. $S_{11}$ and $S_{22}$
are the reflection coefficients $\Gamma$ for ports 1 and 2 are related to the load impedance $Z_L$
at that port as

\[
S_{11} = \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}
\]  

(3.2)

where $Z_0$ is the characteristic impedance of the system, in this case, 50Ω. Rewriting
this, we get,

\[
Z_L = Z_0 \left( \frac{1 + S_{11}}{1 - S_{11}} \right)
\]

(3.3)

The load impedance $Z_L$ can be considered as a parallel or series combination of a
resistance and an inductor or capacitor. In our measurements, net capacitive behavior is
observed. Since the electrical length of the structure at these frequencies is less than 15°,
it is acceptable to ignore the inductance of this structure. Therefore, the load impedance
may be envisioned as one of the structures in Fig. 3.8.

\[\text{Figure 3.8: Two-element series and parallel model of the measured load impedance}\]

Since $S$-parameters are complex quantities, we can express $S_{11}$ in the form $S_{11} = a + jb$, where $a$ and $b$ are the real and imaginary parts of $S_{11}$. If we consider the series
model, we can write,

\[ Z_L = R_s + \frac{j}{\omega C_s} = 50 \left( \frac{1 + a + jb}{1 - (a + jb)} \right) \]  \hspace{1cm} (3.4)

Solving for \( R_s \) and \( C_s \), we get

\[ R_s = 50 \left( \frac{1 - a^2 - b^2}{1 - 2a + a^2 + b^2} \right) \]

\[ C_s = -\frac{1}{2\pi f} \left( \frac{1 - 2a + a^2 + b^2}{100b} \right) \]  \hspace{1cm} (3.5)

Similarly, if we consider the parallel mode, we can write \( \Gamma \) in terms of load admittance \( Y_L \) and \( Y_\theta = 1/Z_\theta \) as

\[ S_{11} = \Gamma = \frac{Y_\theta - Y_L}{Y_\theta + Y_L} \]  \hspace{1cm} (3.6)

This gives

\[ Y_L = Y_\theta \left( \frac{1 - S_{11}}{1 + S_{11}} \right) \]  \hspace{1cm} (3.7)

From the parallel model in Fig. 3.8,

\[ Y_L = \frac{1}{R_p} + j\omega C_p = \frac{1}{50} \left( \frac{1 - (a + jb)}{1 + a + jb} \right) \]  \hspace{1cm} (3.8)

Solving for \( R_p \) and \( C_p \), we get

\[ R_p = 50 \left( \frac{1 + 2a + a^2 + b^2}{1 - a^2 - b^2} \right) \]

\[ C_p = -\frac{1}{50\pi f} \left( \frac{b}{1 + 2a + a^2 + b^2} \right) \]  \hspace{1cm} (3.9)

The parallel resistance \( R_p \) can be represented as a conductance \( G_p \) for better interpretation.

\[ G_p = \frac{1}{R_p} \]  \hspace{1cm} (3.10)

In this manner, the values of \( G_p \) and \( C_p \) can be plotted with respect to frequency at a given drain bias, or with respect to drain bias at a particular frequency.
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3.3.2 Three-element Model

A three-element model, however, is a more complete and accurate representation of the device. This three-element model consists of a series resistance $R_s$, a resistance $R_p$ which is in parallel with a capacitance $C_p$. This is similar to the three-element model shown in Fig. 2.3.

As shown in Fig. 3.9, the series resistance $R_s$ represents the resistance of the probe contacts and in the metal, the parallel resistance $R_p$ represents the leakage current through the device and $C_p$ corresponds to the depletion layer capacitance between the source and drain.

![Figure 3.9: Significance of each component of the three-element model](image)

Deriving the three-element model

Data fitting is used to derive the three-element model. Agilent ADS was used to conduct the data fitting. The schematic used for this purpose is shown in Fig. 3.10.

Each set of measured $S$-parameter data from the Network Analyzer stored in 2-port Touchstone (.s2p) format is first read into ADS Dataset (.ds) format. The dataset file is read into the simulation using the DataAccessComponent DAC1. The S2P_Eqn block S2P1 assigns the data from the DataAccessComponent to variables. In this schematic, the measured $S_{11}$, $S_{12}$, $S_{21}$ and $S_{22}$ are read as the $S$-parameters related to ports 1 and 2 assuming a 50Ω system. In the dataset shown, the drain was at Port 2. The three-element model is constructed using $R_s$, $R_p$ and $C_p$. The name associated with this
Figure 3.10: ADS schematic used to derive the three-element model
model is Port 3. Again, a 50Ω system is assumed. The S-Param block SP1 calculates the
S-parameters for each of the three specified ports from 1 to 10 GHz, in steps of 100 MHz.
In order to find the best fit values for the elements in the model, two goals are specified
- OptimGoal1 attempts to minimize the absolute difference between the magnitude of
the measured $S_{22}$ and the modeled $S_{33}$, while OptimGoal2 attempts to minimize the
absolute difference between the phase of the measured $S_{22}$ and the modeled $S_{33}$. The
optimization type in Optim1 is set to Random.

It is intuitive to believe that the series resistance $R_s$ remains constant for each device
for all conditions. It is also observed that for a given condition of illumination, the
capacitance $C_p$ remains more or less constant. This can be understood by noting that
the device is a fully depleted region between two heavily doped regions. Therefore,
the depleted region does not change with bias, keeping the capacitance constant for
given condition of illumination. This implies that the variation in device behavior under
different bias conditions can be captured merely by the resistance $R_p$.

It is observed that the phase is controlled by the values of $R_s$ and $C_p$. Their con-
tribution to variation in the magnitude of the S-parameter is negligible. On the other
hand, $R_p$ controls the magnitude and has little contribution to the phase behavior. Fur-
ther, the optimization works best when each goal is specified independent of the other.
Therefore, to extract the best-fit model, the values of $R_s$ and $C_p$ were first ascertained
for each condition of illumination using OptimGoal2. Then OptimGoal1 was used to
find the best value of $R_p$ for each value of drain bias.

The three-element model was derived for all samples using the data between 1 and
3 GHz. Fig. 3.11 shows the plots in ADS where the fitting was done for one of the
samples. This frequency range was specifically chosen because below 1GHz, the Network
Analyzer used does not give reliable readings. Up to 3GHz, it was possible to obtain a
three-element fit with less than 0.3% error.

The value of $G_p$ and $C_p$ for four different devices with no drain bias is shown in Table
3.1. The conductance is seen to be higher and the capacitance lower in the presence of
illumination for all cases.
Figure 3.11: Plots showing the fitting of the three-element model in ADS

This is consistently seen across all samples and can be explained by noting that in the presence of light, more carriers are released for conduction, thereby increasing the current and reducing the resistance. In the absence of light, the carriers are trapped and this causes the capacitance to increase. What is interesting to determine, however, is the difference between what is a bulk effect and what is a surface effect. The light introduces a significant amount of enhanced conduction from the electron hole pairs created. This is not a trapping or surface effect. What is needed is a method to determine the residue

Table 3.1: Gp and Cp of different devices derived using the three-element model

<table>
<thead>
<tr>
<th>Device ID</th>
<th>$G_p$ - Light (mS)</th>
<th>$G_p$ - Dark (mS)</th>
<th>$C_p$ - Light (fF)</th>
<th>$C_p$ - Dark (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device 1</td>
<td>0.0826</td>
<td>0.0606</td>
<td>39.7</td>
<td>40.2</td>
</tr>
<tr>
<td>Device 2</td>
<td>0.139</td>
<td>0.0987</td>
<td>63.6</td>
<td>64.0</td>
</tr>
<tr>
<td>Device 3</td>
<td>0.0516</td>
<td>0.0444</td>
<td>35.9</td>
<td>37.2</td>
</tr>
<tr>
<td>Device 4</td>
<td>0.0431</td>
<td>0.0337</td>
<td>42.4</td>
<td>44.6</td>
</tr>
</tbody>
</table>
or the amount of electrical behavior that is not explained by bulk or non-trapping properties.

Calculating the Residue

The four 2-port $S$-parameters are related to the Admittance or $Y$-parameters as

$$
Y_{11} = Y_0 \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}
$$

$$
Y_{12} = Y_0 \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}
$$

$$
Y_{21} = Y_0 \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}
$$

$$
Y_{22} = Y_0 \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}
$$

(3.11)

where $Y_0 = 1/Z_0$ is the characteristic admittance of the system.

The measured $S$-parameters can be then be examined as $Y$-parameters and thought of as a combination of device behavior and trap behavior, as shown in Fig. 3.12.

![Figure 3.12](image)

**Figure 3.12:** Separating the measured $Y$-parameters into device and trap $Y$-parameters

As described earlier, $Y_{3el}$ (or equivalently $S_{33}$ of Fig. 3.10) is obtained by deriving a unique three-element model for each condition of drain bias and illumination for each device in the lower range of frequencies. The residue $Y$-parameters, $Y_T$, is then found from the measured $Y$-parameters (equivalent to $S_{22}$ in Fig. 3.10) as
Chapter 3

Experiment and Analysis Methodology

Figure 3.13: Plots showing the calculation of the residue in ADS

\[ real(Y_T) = \text{abs}(real(Y_{meas}) - real(Y_{3el})) \]

\[ \text{imag}(Y_T) = \text{abs}(\text{imag}(Y_{meas}) - \text{imag}(Y_{3el})) \]  

(3.12)

This residue in the higher frequency range then indicates the equivalent model for the traps since we have effectively subtracted the ideal behavior of the device from the measured behavior. This is shown in Fig. 3.13.

3.4 Preliminary Analysis and Discussion

The reasons for using the method described above to characterize surface states was briefly mentioned in Chapter 1. Here, we look at these in a little more detail. But before that, some preliminary calculations to verify the data are in order.
3.4.1 Calculation of Capacitance for the $n$-$i$-$n$ Structure

The $n$-$i$-$n$ structure can be approximated as a coplanar waveguide with dimensions as indicated in Fig. 3.14(a). The dopant density of the source and drain regions is low and introduces additional loss. But, a numerical analysis indicates that this contribution does not alter the expected capacitance value significantly. The measurement pads (as shown in Fig 3.14(b)) are also a significant fraction of the measured capacitance in this configuration and should be included for accuracy. The sum of the two theoretical capacitances is what is to be expected, as in Fig. 3.14(c).

To calculate the capacitance of this structure, the transmission line properties are found using the ADS LineCalc utility. For given dimensions and material properties, this software package solves appropriate electromagnetic relations to produce an impedance and electrical line length. It should be noted that in lossless lines, there is no frequency dependence on the parameters of interest. However, when there is series resistive and parallel conductive loss, this condition should be re-evaluated. For the purposes of a check for accuracy and consistency of results though, this can be neglected.

To find the effective capacitance that is presented by the coplanar waveguide structure, its physical length is related to the impedance and electrical line length. The characteristic impedance is given by the standard relation

$$Z_o = \sqrt{\frac{L}{C}}$$

(3.13)

where $L$ and $C$ are the inductance and capacitance per unit length. The electrical line length $\theta$ is given by

$$\theta = \frac{2\pi l_g}{v_g} f = \frac{2\pi l_g}{1/\sqrt{LC}} f = 2\pi f l_g \sqrt{LC}$$

(3.14)

where $f$ is the frequency at which the measurement is taken. The total capacitance $C_o = l_g C$ of the $n$-$i$-$n$ structure can be evaluated by solving in terms of the electrical line as

$$C_o = \frac{\theta}{2\pi f Z_o}$$

(3.15)
Figure 3.14: Theoretical calculation of capacitance of an n-i-n structure using LineCalc
This relation is used in conjunction with LineCalc to produce the plot in Fig. 3.15.

Figure 3.15: Projected capacitance with respect to dimensions

A sweep of dimensions is shown. This has been calculated for electrical line lengths < 15°. The effective capacitance is plotted for varying gap space and line length. For typical dimensions used in this study, the center conductor width is found to be inconsequential. Using a similar method, the expected pad capacitance $C_p$ is approximately 20fF for the devices in this study. Further, for the dimensions indicated by SEM of the typical structure (55µm × 0.7µm), the expected capacitance is approximately 20fF. It is therefore concluded that a capacitance of at least 40fF should be observed in the measurements.

3.4.2 Comparison of ‘Signal-to-Noise Ratio’

The number of traps exposed during testing is directly related to the surface area involved in the measurement. In this method, the $S$-parameters are measured between the drain and source terminals of the $n$-$i$-$n$ structure as shown in Fig. 3.10(b). Let us compare this to the measurement between the gate and drain as in Fig. 3.10(a) - the
method traditionally used [7]. The total capacitance seen in the other method is of much larger magnitude than ours since the large gate capacitance is also seen there. Moreover, the drain-source direction allows observation of the entire channel length, as opposed to the gate-drain direction where only a portion of the channel can be observed.

Figure 3.16: Measuring impedance between (a) gate and drain terminals, and (b) drain and source terminals

From both these observations, we see that the ratio of the residue to the measured capacitance is larger in our methodology. The residue represents the surface traps which we want to observe (‘signal’) and the inherent capacitance is that part of the measurement which we want to subtract out (‘noise’). Hence, the ‘signal-to-noise’ ratio here is larger.

A chart to compare the horizontal and the more traditional vertical configuration with different dielectric thicknesses is shown in Fig. 3.17. Here, the thickness of SiO$_2$ is varied as 10Å, 100Å and 1000Å.

It is clear then that there is no advantage to using the $n$-$i$-$n$ structure for this measurement when the dielectric thickness is large. However, at small dielectric thicknesses,
the signal-to-noise ratio is of significant advantage to the traditional measurement technique. This makes this experiment more accurate and dependable in this regime.

3.4.3 Suitability for Frequency of Application

To explore the frequency suitability of a particular structure, consider the three-element model. The imaginary conductance due the capacitance of interest must be significantly larger than any conductance due to any leakage current, including the Mott-Gurney current that might be present. In addition the series resistance must be significantly smaller than the impedance due to the capacitance of interest. These requirements create two design rules that will dictate the frequency bounds where successful measurements of capacitance can occur. This is a fundamental limitation and exists for all measurements. It is this interaction that ultimately creates difficulties in measuring and isolating non-classically predicted effects in capacitance of semiconductor behavior.

Figure 3.17: Normalized signal-to-noise ratio vs. gap dimension
3.4.4 Limitations due to the Instrument

A limitation of this method is that since the capacitance being measured is small, obtaining correct readings was found to be impossible for some of the devices with smaller dimensions. A lower limit on the frequency range of measurement exists while using the particular Network Analyzer that was used in these experiments - reliable readings are not obtained for frequencies below 1GHz. Also, accurate three-element model fitting was not obtained for all measurements due to sensitivity to calibration.

Figure 3.18: Dependence of measurability of capacitance on frequency
Chapter 4

Results and Conclusions

In this chapter, the measurements and results of the analysis proposed in Chapter 3 is presented. The results from the two-element model are followed by those from the three-element model and the residue. All results presented in this chapter are from one particular two-finger device, ‘Device 1’, whose length and width are approximately 0.7µm and 55µm respectively. Similar results from three other devices are presented in Appendix B.

4.1 Two-element Model

Figs. 4.1 and 4.2 show the plot of \( G_p \) and \( C_p \) of the two-element model as a function of the drain voltage \( V_d \), as measured at different frequencies.

Figs. 4.3 and 4.4 compare \( G_p \) and \( C_p \) with respect to frequency in the presence and absence of light, while \( V_d \) is maintained at 0V.

4.2 Three-element Model

For this particular device, the three-element model parameters obtained by fitting to the measured values are as follows -

Presence of light: \( R_s = 44.2\,\Omega, \ C_p = 39.7\,\text{fF} \)

Absence of light: \( R_s = 44.2\,\Omega, \ C_p = 40.2\,\text{fF} \)
Figure 4.1: Two-element Model - Plot of $G_p$ with respect to $V_d$ at different frequencies

Figure 4.2: Two-element Model - Plot of $C_p$ with respect to $V_d$ at different frequencies
Figure 4.3: Two-element Model - Comparison of Gp in the presence and absence of light. Vd=0

Figure 4.4: Two-element Model - Comparison of Cp in the presence and absence of light. Vd=0
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Results and Conclusions

The variation of $G_p$ with bias, in the presence and absence of light is shown in Fig. 4.3.

![Figure 4.5: Three-element Model - Comparison of Gp in the presence and absence of light. Vd=0](image)

**Figure 4.5:** Three-element Model - Comparison of Gp in the presence and absence of light. Vd=0

### 4.3 Residue

Figs. [4.6] and [4.7] show the variation of residue with frequency in the presence and absence of light, while the drain bias is held at 0V. The real part corresponds to the admittance, and the imaginary part divided by the angular frequency gives the capacitance of the residue.

The variation of the residual conductance and capacitance with drain bias was also studied. This is shown in Figs. [4.8] and [4.9]. It can be seen that there is not much change of residue with bias. This is expected since the three-element model accounts for the bias dependence of the device.

Attempts were made to quantify the surface states using the information obtained from calculating the residue. One method that was considered was combining the ideas
Chapter 4  

Results and Conclusions

Figure 4.6: Residue of Y - conductance. Vd=0

Figure 4.7: Residue of Y - capacitance. Vd=0
Figure 4.8: Residue of Y - conductance for different values of Vd

Figure 4.9: Residue of Y - capacitance for different values of Vd
presented in [8] and [7]. This would suggest that since the behavior of the device has been subtracted from the measured parameters, the residue is a property of the trapping effects. Therefore, if a parallel \( RC \) model is used to represent the traps, Eq. (2.21) or Eq (2.22) could be used to determine the density of surface traps \( D_{it} \), assuming the time constant \( \tau \) is known or can be determined.

Here, a value of \( \tau \) had to be assumed since there was no straightforward way to estimate that from these experiments. A really small value of \( \tau \) was assumed because we are interested in knowing high-frequency effects. Curves generated using both equations (for discrete as well as a continuum of traps) are shown in Fig. 4.10. In both equations, \( \tau = 10 \text{ps} \) and \( D_{it} = 1.5 \times 10^{10} / \text{cm}^2 \).

![Figure 4.10: Fitting of equations for trap parameters on the residue](image)

Both \( \tau \) and \( D_{it} \) were varied so as to try and fit to the data as best as possible. For the devices on which this method was applied, \( D_{it} \) values that gave the best possible fit were of the order of \( 10^{10} / \text{cm}^2 \). However, this did not appear to be a reasonable method, firstly, since the derivation of the original equations did not appear convincing. Also, the fit was bad and since there was no way to determine \( \tau \), the fitting seemed arbitrary.
Another thought was to characterize the traps using the difference between the residue in the presence and in the absence of light. However, this is not credible since the residue is obtained after subtracting out a three-element model and the difference could depend on the difference in accuracy of the fit between both cases.

A more reasonable thinking would be to find the difference between the capacitance and/or conductance obtained by the two-element model in the presence and absence of light. This was attempted, but did not give consistent results across all samples.

### 4.4 Conclusions and Future Work

This thesis has taken a first step towards trying to understand the traps that affect GaN devices using a new method. Fig. 4.11 lists the chief steps of this technique.

The novelty of the technique lies, most importantly, in the frequency range used to investigate the traps. Given the dimensions of the devices under test, it becomes necessary to measure the impedance at high frequencies to be able to reliably estimate the capacitance and hence, the effects of the surface states.

The fact that it is the drain-source impedance of an $n$-$i$-$n$ structure that is being measured, as opposed to the gate-drain or gate-source impedance of a FET, is also noteworthy. As mentioned earlier, this facilitates the examination of the entire channel length, and not just a part of it. Moreover, the ratio of the capacitance of interest to the measured capacitance is definitely larger in the drain-source direction. This ensures that the method used to characterize the traps from these measurements will yield more accurate numbers.

The three-element models used to account for the frequency-dependent behavior of just the device was found to be consistent and as expected with respect to the state of illumination. The residue obtained on subtracting the expected behavior of the device clearly evinces the presence of some spurious effects. Though it was not possible to distinctly distinguish the exact source of these effects, the method used to isolate them is sound.
Using the network analyzer, measure S-parameters of the device at the drain between 1GHz and 10GHz, both in the presence and absence of light.

Arrive at 3-element model for device behavior by fitting to data between 1 - 3GHz. Rs remains constant for a device, Cp remains constant for one condition of illumination. Variation in Gp captures change device behavior with bias.

Subtract Y-parameters of the 3-element model from the measured Y-parameters to obtain the 'residue' - Y-parameters of the traps.

Analyze the residue to obtain information about the traps.

Figure 4.11: Flowchart describing the method proposed by this thesis
Future work would consist of finding a method to quantify surface states using the technique described in this work. For this to be possible, it would be necessary to take readings on more samples and also verify them on another instrument.

Measurement of the output impedance over temperature at these high frequencies is also likely to provide more insight into the behavior of traps.

From the discussion in Chapter 3, it also becomes apparent that specialized test structures will need to be fabricated. To this end, an array of $n$-$i$-$n$ structures with channel lengths of 1, 2, 5 and 10$\mu$m and widths of 50, 100, 200 and 400$\mu$m is suggested. This would help to find a broad frequency range with maximum ability to measure capacitance.
List of References


APPENDICES
Appendix A

S-parameters and the Network Analyzer

This appendix offers a quick introduction to S-parameters, the Smith Chart and calibrating the network analyzer - essential tools to understanding any RF measurement.

A.1 S-parameters

At very high frequencies, it is impossible to accurately measure voltages and currents since it is required to take into consideration the direction and phase of the traveling signals or standing waves. Hence, S-parameters, which are small-signal parameters relating the incident and reflected voltage waves at each port, are used [41]. They are fixed properties of a linear circuit which describe how energy couples between each pair of ports in a general N-port network.

The S-parameter matrix \([S]\) is defined for an N-port network as

\[
\begin{pmatrix}
V_1^- \\
V_2^- \\
\vdots \\
V_N^-
\end{pmatrix} =
\begin{pmatrix}
S_{11} & S_{12} & \cdots & S_{1N} \\
S_{21} & S_{22} & \cdots & \vdots \\
\vdots & \vdots & \ddots & \vdots \\
S_{N1} & S_{N2} & \cdots & S_{NN}
\end{pmatrix}
\begin{pmatrix}
V_1^+ \\
V_2^+ \\
\vdots \\
V_N^+
\end{pmatrix}
\]

or

\[
[V^-] = [S][V^+]
\]  
(A.1)
where \( V_n^+ \) and \( V_n^- \) are the amplitudes of the voltage waves incident on and reflected from port \( n \) respectively. \( S_{ij} \) is therefore defined as the ratio of the voltage wave amplitude coming out of port \( i \) to the incident voltage at port \( j \) when the incident waves at all ports, other than \( j \), are set to zero. Therefore, when all other ports are terminated with matched loads, \( S_{ii} \) is the reflection coefficient \( \Gamma \) looking into port \( i \), and \( S_{ij} \) is the transmission coefficient \( T \) from port \( j \) to \( i \). For a two-port network, we can visualize this as in Fig. A.1.

![Figure A.1: 2-port S-parameters](image)

\[
\begin{pmatrix}
|b_1|^2 \\
|b_2|^2
\end{pmatrix}
= \begin{pmatrix}
|S_{11}|^2 & |S_{12}|^2 \\
|S_{21}|^2 & |S_{22}|^2
\end{pmatrix}
\begin{pmatrix}
|a_1|^2 \\
|a_2|^2
\end{pmatrix}
\]

where \( |a_i|^2 \) and \( |b_i|^2 \) are respectively the powers of the waves traveling towards and away from port \( i \).

The main advantages of using \( S \)-parameters are that they are easy to obtain at high frequencies and also that their measurement does not require open or shorts. Further, they are related to familiar RF terms like reflection coefficient, gain, etc. and algebraically related to \( H \), \( Z \) and \( Y \) parameters. It is also possible to cascade \( S \)-parameters from different devices to obtain the overall system performance.
A.2 Smith Chart

The Smith chart is essentially a polar plot of the reflection coefficient $\Gamma$, on which is superimposed the positive half of the impedance plane as shown in Fig. A.2 [42]. The normalized impedance $z_L = Z_L/Z_0$ can be related to $\Gamma$ as [41]

$$\Gamma = \frac{z_L - 1}{z_L + 1} = |\Gamma|e^{j\theta} \quad (A.2)$$

The Smith chart is therefore useful a tool to not only to convert from reflection coefficient to impedance and vice-versa, but also to visualize the impedance or admittance.

A.3 Network Analyzer Calibration

Calibration of the network analyzer is important to remove the sources of systematic errors in the measurement. There are 6 sources of systematic errors that need to be calibrated out in order to make a good measurement. As shown in Fig. A.3 [43], these are (a) Signal leakage: Directivity, Crosstalk (b) Signal reflections: Source mismatch, Load mismatch and (c) Frequency response of receiver: Reflection, Transmission tracking.
There are 6 terms in each of the two directions. Therefore, a 12-term error correction method is used. The idea is to characterize systematic error terms by measuring known calibration standards and then removing these errors from subsequent measurements.

A one-port calibration removes 3 error terms - directivity, source match, reflection tracking. A two-port calibration removes all 12 error terms. The standards defined in a cal-kit definition file in the network analyzer.

Two-port calibration is conducted by presenting each of the ports with Short, Open, (50Ω) Load and Thru as shown in Fig. A.4. Re-measuring each standard after calibration is a good practice to check the quality of the calibration.
Appendix B

Results from More Samples

This appendix contains results from four devices other than that presented in Chapter 4. All have the same structure as Device 1. Devices 2 and 3 have the same dimensions as Device 1, i.e., their width is approximately $55\mu m$ and length is $0.7\mu m$. Devices 4 is larger - its width and length are approximately $75\mu m$ and $0.7\mu m$ respectively.

For these devices, the three-element model parameters obtained by fitting to the measured values are as follows -

Device 2:

Presence of light: $R_s = 50.0\Omega$, $C_p = 63.6fF$

Absence of light: $R_s = 50.0\Omega$, $C_p = 64.0fF$

Device 3:

Presence of light: $R_s = 44.9\Omega$, $C_p = 35.9fF$

Absence of light: $R_s = 44.9\Omega$, $C_p = 37.2fF$

Device 4:

Presence of light: $R_s = 49.9\Omega$, $C_p = 42.4fF$

Absence of light: $R_s = 49.9\Omega$, $C_p = 44.6fF$
B.1 Device 2

Figure B.1: 2-element Model - Comparison of Gp in the presence and absence of light

Figure B.2: 3-element Model - Comparison of Gp in the presence and absence of light
Figure B.3: Residue of Y - Conductance. Vd=0

Figure B.4: Residue of Y - Capacitance. Vd=0
Appendix B

B.2 Device 3

Figure B.5: 2-element Model - Comparison of Gp in the presence and absence of light

Figure B.6: 3-element Model - Comparison of Gp in the presence and absence of light
Figure B.7: Residue of Y - Conductance. Vd=0

Figure B.8: Residue of Y - Capacitance. Vd=0
B.3 Device 4

Figure B.9: 2-element Model - Comparison of Gp in the presence and absence of light

Figure B.10: 3-element Model - Comparison of Gp in the presence and absence of light
Appendix B

Figure B.11: Residue of Y - Conductance. Vd=0

Figure B.12: Residue of Y - Capacitance. Vd=0