ABSTRACT

QIN, JIFENG. A Low Noise, High Efficiency Envelope Modulator Structure for EDGE Polar Modulation. (Under the direction of Dr. Alex Q. Huang).

Dynamic supply of power amplifiers in wireless transmitters can overcome the linearity-efficiency tradeoff issue in power amplifiers design, and envelope modulator is the key block in the dynamic supply system, low noise and high efficiency implementations are of many people's interests.

Power management issues in envelope modulators for polar modulation are becoming increasingly complex and challenging. Both voltage step up and step down functions are required based on the input and output voltage ranges, the envelope modulator should have enough bandwidth to pass the modulated fast changing signal without distortion, and the output spectrum of the envelope modulator should meet stringent wireless standard specifications. High efficiency, high bandwidth and low noise requirements make envelope modulator design very challenging, and traditional switch mode power supplies like buck-boost converters cannot provide good spectrum results because of their high noise boost region.

Comparing with switching mode power supplies, charge pumps have several advantages in terms of low noise and high efficiency, in this thesis, a novel two stage envelope modulator structure is proposed by using a voltage doubler followed with a 10MHz buck converter, this modulator achieves high efficiency, and the switching noise is reduced by 50dB compared to 4 switch buck boost converter (4SBBC) solution, and the spectrum simulation results meet the EDGE wireless standard.

A Low Noise, High Efficiency Envelope Modulator Structure for EDGE Polar Modulation

by
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Chair of Advisory Committee

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DEDICATION

To my parents,
Gang Qin and Yiling Liao

And my fiancée,
Xiaolan Xu

BIOGRAPHY

Jifeng Qin was born in Guiyang, Guizhou province, China on October, 8, 1983. He spent four years in Chu Kochen Honors College at Zhejiang University, China, and received his Bachelor degree (with honors) in Electrical Engineering in 2006. After that, he joined Semiconductor Power Electronics Center at North Carolina State University, USA, and working as a research assistant there. His research interests include power management integrated circuits design and power electronics for portable applications.

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Chapter 1 Introduction

Nowadays, wireless communication and mobile systems play an important role in our daily life. Cellular telephones, personal digital assistants (PDAs), satellite television, global positioning systems (GPS), and other wireless networking devices have changed our way of living tremendously. As predicted by Moore's law [Moore'65], the transistor count in a single chip will double every eighteen months and the performance of integrated circuits (ICs) will increase while the cost will go down, which in turn makes it possible to integrate more functions in a single mobile device. However, the main drawback in device shrinking is increased power consumption. For wireless handheld devices and other portable applications, minimizing power consumption is especially crucial to prolong the battery life. This issue is partly solved by the development of semiconductor processing and battery technology, however there is still much room for innovation in wireless transmitter architecture and integrated circuits design.

1.1 Wireless Communication Standard

1.1.1 The evolution of 2G and 3G standard

Table 1.1 summarizes the specifications of different wireless standards. Thanks to the agreement that led to the development of the Global System for Mobile Communications (GSM) standard twenty years ago, the mobile telephony market has been growing rapidly ever since. Today, the GSM family makes up 85% of the global mobile services market and serves more than 2.5 billion people in 218 countries all over the world [GSM'07].

Table 1.1 Summary of various wireless communication standards [McCune'05]

System	Bandwidth (MHz)	Modulation	Peak to Average Power Ratio (dB)	Peak to Minimum Power Ratio (dB)	Antenna Power (dBm)	Duplex	Power Control Dynamic Range (dB)	TX Duty Cycle	Spectral Quality (dB)
1G (AMPS)	0.03	FM	0	0	28	full	25	100%	–26 (1)
ANSI-136	0.03	$\pi/4$-DQPSK	3.5	19	28	half	35	33%	–26 (1)
GSM	0.2	GMSK	0	0	33	half	30	13%	–60 (3)
GPRS	0.2	GMSK	0	0	33	half	30	13–50%	–60 (3)
EDGE	0.2	$3\pi/8$-8PSK	3.2	17	27	half	30	13–50%	–54 (3)
UMTS	3.84	HPSK	3.5–7	infinite	24	full	80	100%	–33 (1)
IS-95B	1.23	OQPSK	5.5–12	26–infinite	24	full	73	100%	–42 (2)
cdma2000	1.23	HPSK	4–9	infinite	24	full	80	100%	–42 (2)
TETRA	.025	$\pi/4$-DQPSK	3.5	19	36	half	45	25%	–60 (1)
Bluetooth	1	GFSK	0	0	20	half	–	variable	–20 (4)
802.11b	11	QPSK	3	infinite	20	half	–	variable	–30 (5)
802.11a/g	18	OFDM	6–17	infinite	20	half	–	variable	–20 (5)

Spectral Quality Notes:
1–Adjacent channel power, equal bandwidth to the main channel.
2–Nearby (885-kHz offset) channel power, measured in 30kHz bandwidth.
3–Transmitter signal mask at 400-kHz offset.
4–Transmitter signal mask at 500-kHz offset.
5–Transmitter signal mask at 11-MHz offset.

As shown in Table 1.1, the third generation (3G) wireless systems such as CDMA2000 and Wideband CDMA offer a significant increase in channel capacity and are suited for broadband data access [Steer'07]. However a higher data transmit rate requires more signal bandwidth and a higher power control dynamic range. The high data rate means larger amplitude modulation of the signal in order to increase the number of bits per transmitted symbol, which in turn results in a larger peak to average ratio (PAR) of the modulated signal. Thus the efficiency of the power amplifier (PA) will decrease due to increased power back-off [Lee'04]. Additionally, more signal bandwidth means the change of the symbols happens at a faster rate, which results in more stringent design specifications for the wireless transmitter.

1.1.2 Enhanced Data rate for GSM Evolution (EDGE) Standard

EDGE standard is known as a transition from 2G to 3G network and it is compatible with the GSM standard. Fig. 1.1 illustrates the comparison of the EDGE standard and other wireless standards in terms of transmit range and bit rate. The development of the EDGE standard stems from the urgent need for increasing the system data transmit capacity within the same 200 kHz GSM bandwidth, so it is necessary to use an efficient modulation technique that can provide a higher throughput/occupied bandwidth ratio.

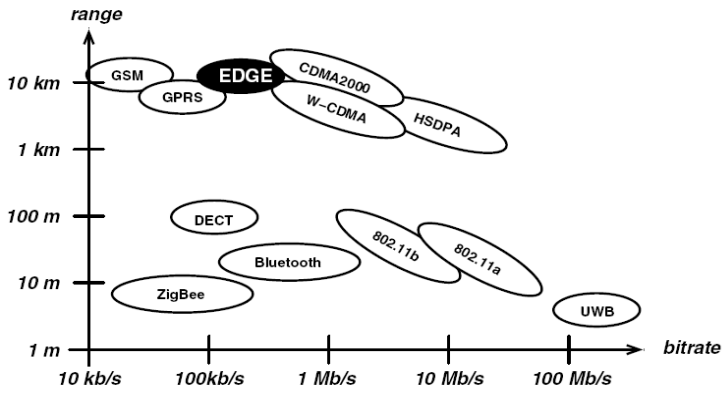


Figure 1.1 Position of the EDGE system between other wireless standards [Reynaert'06]

The time and frequency domain EDGE signals are shown in Fig. 1.2. The modulation scheme for EDGE is $3\pi/8$ offset 8-phase-shift-keying (8PSK). Since one symbol now contains 3 bits of information, the data rate is 812.5 kbps, 3 times faster than that of the GSM standard, which uses Gaussian-minimal-shift-keying (GMSK). The main difference between these two modulation methods is that GMSK has constant envelope signal, while both the envelope and the phase signal are changing for $3\pi/8$ offset 8PSK modulation [Mashhour'99]. This affects the RF transmitter design as will be discussed in chapter 2.

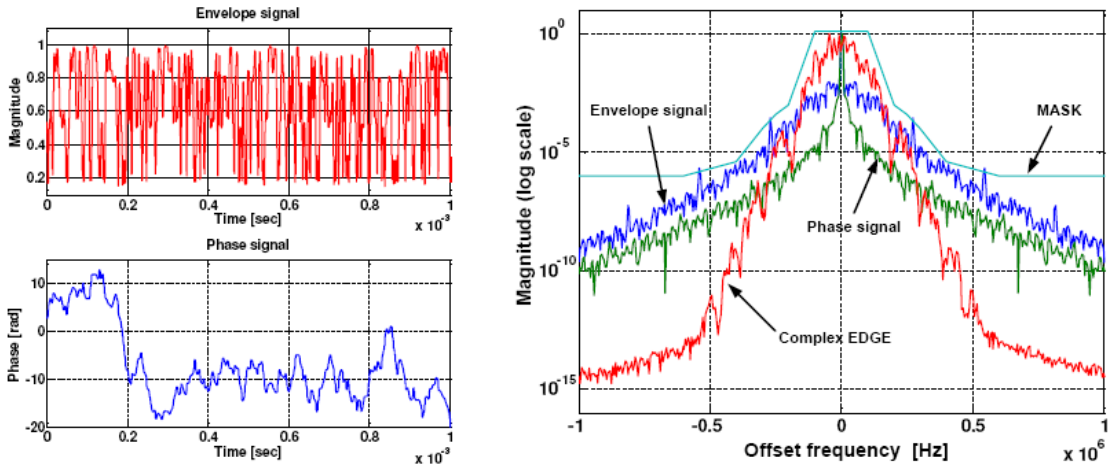


Figure 1.2 EDGE signals in time and frequency domains

1.2 Power Amplifiers (PAs) in Wireless Transmitter

Wireless portable devices require a radio frequency (RF) transmitter to send the information signal to the nearest base station. Fig. 1.3 shows a simple block diagram for a direct-conversion transmitter.

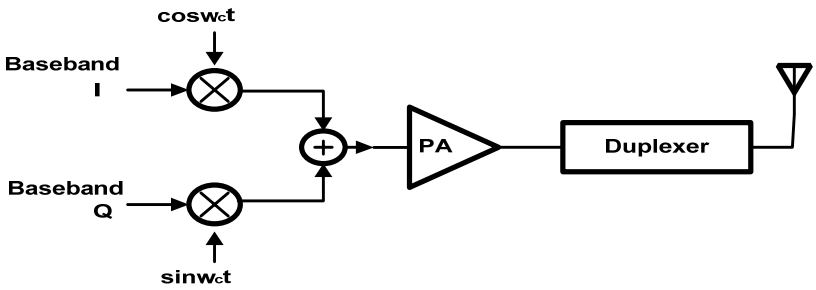


Figure 1.3 Block diagram of a direct-conversion transmitter

As shown in Fig 1.3, the PA is the last stage of the transmitter and serves as the interface between the baseband modulated signal and the antenna. The goal of the PA is to provide enough power to drive the antenna so that the electromagnetic signal it transmits can reach the base station with sufficient strength. The transmitted signal should have minimal

distortion in order to prevent spectrum regrowth both inside and outside its bandwidth (i.e. interfering with other channels), which means the PA should have very high linearity. On the other hand, as the PA is the most power consuming block in the transmitter, high efficiency is highly desirable for prolonging the battery life.

Besides linearity and efficiency, other keywords used to define the performance of the PA are output power and gain. Generally speaking, output power and linearity are set by the wireless standard, and if they are not met the PA is considered useless. Efficiency and gain are both related to the battery lifetime, a high efficiency and high gain PA consumes less battery power [Reynaert'06]. These four parameters are related to each other and it is difficult to optimize all of them simultaneously. The most common issue is the PA linearity and efficiency tradeoff, which will be illustrated in the rest of this section.

1.2.1 PA Linearity

Linearity of the PA is measured both in-band and out-of-band, and the specifications related to the measurement are discussed as follows:

(a) Adjacent Channel Power Ratio (ACPR):

ACPR is the performance metric that measures how much of the signal is spreading into the adjacent channel as the result of the nonlinearities of the PA. In Fig. 1.4, ACPR is defined as the power contained in a defined bandwidth (BW2) at a defined offset (f_O) from the channel center frequency (f_C), divided by the power in a defined bandwidth (BW1) placed around the channel center frequency [Kenington'00].

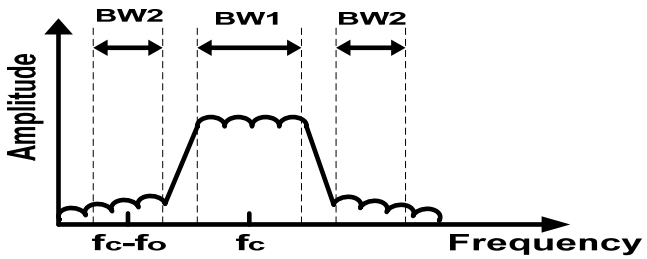


Figure 1.4 Adjacent channel power ratio

(b) Error Vector Magnitude (EVM):

In digital communications, the digital bits signal is modulated onto an analog carrier by changing its magnitude and phase, and they can be mapped as the specific locations on in phase (I) and quadrature-phase (Q) planes, which commonly known as the constellation diagram. The EVM is defined as the scalar distance between the end points of measured signals and reference signals, as shown in Fig. 1.5.

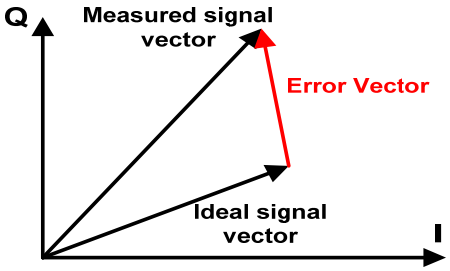


Figure 1.5 Illustration of error vector in the I/Q plane

The error vector is a complex parameter which contains both magnitude and phase information, EVM is measured as the root mean square (RMS) value of the error vector and typical values are between 5% and 15% [Kenington'00]

1.2.2 PA Efficiency

The efficiency of the PA is defined in different ways, the most straightforward definition of which is drain efficiency:

$$\eta_{Drain} = \frac{P_{out}}{P_{DC}} \qquad (1.1)$$

where P_{out} is the output power and P_{DC} is the power drawn from the DC supply.

Another definition is power added efficiency (PAE), which includes the losses due to the input power and is defined as:

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \qquad (1.2)$$

PAE takes the gain of the PA into consideration and therefore describes the performance of the PA more accurately than drain efficiency. PAE can be rewrite as:

$$\eta_{PAE} = \frac{P_{out}(1-1/(P_{out}/P_{in}))}{P_{DC}} \qquad (1.3)$$

PAE approaches drain efficiency as the power gain P_{out}/P_{in} goes to infinity.

Drain efficiency and PAE represent the performance of the PA only when it works at the peak output power. In EDGE and other wireless communication standards, the PA operates at its peak power only for a little fraction of time, while most of the time the PA operates at 20dB to 30dB power backoff. The average efficiency of the PA, which takes the output power's probability density function (PDF) in to consideration, is the most important measure in determining the battery life for the transmitter [Sevic'97]. The average efficiency is defined as:

$$\overline{\eta}_{avg} = \frac{\int_{-\infty}^{\infty} P_L\, g(P_L)\, dP_L}{\int_{-\infty}^{\infty} P_{SUPPLY}\, g(P_L)\, dP_L} \qquad (1.4)$$

where P_L is the instant power delivered to the load, P_{SUPPLY} is the instant power drawn from the DC supply, and $g(P_L)$ is the probability density function of wireless standard. $\bar{\eta}_{avg}$ shows to what extent the PA converts battery power to transmitted power.

1.2.3 PA Classification

Power amplifiers are traditionally divided in several classes based on the different driving schemes and the harmonic content of the drain voltage. In wireless communication systems, the most important classification is linear class PA such as class A, B and AB, and nonlinear class PA which contains class C, D, E and F [Lee-1'04].

(a) Linear Classes:

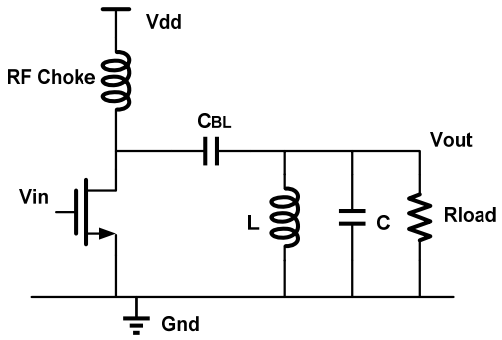


Figure 1.6 Linear PA structure

Linear class PAs are usually differentiated by the conduction angle of the transistors. Fig. 1.6 represents the typical structure of all the linear PAs. The RF choke inductor feeds DC power to the drain. The drain is connected to a tank circuit through the DC block capacitor to prevent any DC dissipation to the load.

Fig. 1.7 shows the DC bias points for different linear PAs. The straightforward method to increase the efficiency is to reduce the time when the current and voltage are both

nonzero, which means reducing the conduction angle. A class B PA is typically biased at the threshold of the transistor so the conduction angle is 180 degree, and the maximum efficiency is increased to 78%, with the sacrifice of linearity. The conduction angle and efficiency of a class AB PA sits between those of class A and class B.

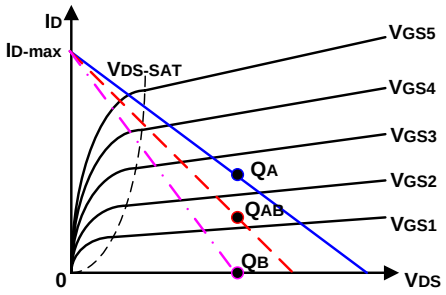


Figure 1.7 Bias points for linear PAs

(b) Nonlinear Classes:

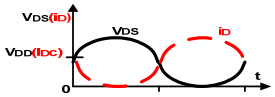
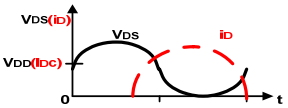
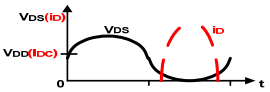
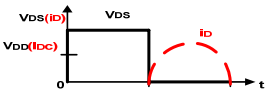
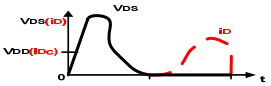
The nonlinear PAs use different schemes to maximize the efficiency. The structure of a class C PA is the same as its linear counterparts but it is biased at a conduction angle of less than 180 degrees, which results in deterioration of amplitude linearity but improvement of efficiency. The maximum efficiency of class C PA approaches 100% as the conduction angle approaches zero degree.

Class D and class E PAs are known as switching PAs. They are different from linear PAs in that the transistors are driven hard enough to make them act like switches, and therefore theoretically there will be no time that the current and the voltage are both nonzero, ideally resulting in 100% efficiency. A class D PA usually uses two active elements to create a square wave and then it is filtered by a high Q tank structure, while a class E PA uses a high-order reactive network that provides enough freedom to shape the switch voltage to have both zero value and zero slope when the transistor turns on, reducing its switching loss.

A class F PA increases its frequency by using a quarter wavelength of transmission line or resonant band-stop filter. By cleverly arranging for the square-wave voltage to see no load at all frequencies above the fundamental, the switch current is ideally zero both at switch turn on and turn off times, leading to 100% maximum efficiency.

The summary of the different PAs are listed at Table 1.2.

Table1.2 Performance summaries of different PAs

Class	***I-V Waveform***	***Efficiency***	η_{MAX} **%**	**Conduction Angle** ϕ
A		$\eta = \frac{V_{OUT}^2}{2V_{DD}^2}$	50%	360^0
B		$\eta = \frac{\pi V_{OUT}}{4V_{DD}}$	78.5%	180^0
AB		$\eta = \frac{V_{OUT}}{V_{DD}} \frac{\phi - \sin\phi}{4(\sin\frac{\phi}{2} - \frac{\phi}{2}\cos\frac{\phi}{2})}$	50%-78.5%	180^0-360^0
C		$\eta = \frac{V_{OUT}}{V_{DD}} \frac{\phi - \sin\phi}{4(\sin\frac{\phi}{2} - \frac{\phi}{2}\cos\frac{\phi}{2})}$	100%	$<180^0$
D		/	100%	$<180^0$
E		/	100%	$<180^0$
F		/	100%	$<180^0$

1.2.4 Linearity and Efficiency Tradeoff

The most important factor to increase the battery lifetime in portable devices, such as mobile phones for EDGE communication, is to minimize the power drawn from the battery to the power-hungry PA, and meet the wireless communication standard linearity specification at the same time. However, the linearity and efficiency tradeoff discussed in the preceding chapter makes it difficult to realize a high linearity and energy-efficiency PA for portable application. Linear class PAs have high linearity but the efficiency is low. Nonlinear class PAs can ideally achieve 100% efficiency, but may result in severe signal distortion between the input signal and output signal. Nowadays numerous PA linearization and efficiency boosting techniques are used in order to solve this problem. The scheme for designing an efficient, high linearity PA can be divided into two categories: (a) improve the linearity of a non-linear PA and (b) improve the efficiency of a linear PA. Both methods will be discussed in the following section.

1.3 PA Linearization Techniques

Linearization techniques basically refer to the methods used to improve the linearity of the PA with additional circuits. The most straightforward and simplest way is to use negative feedback which is commonly used in low frequency analog circuits design. However, directly feeding back the output signal from the PA is not practical within the RF and microwave frequency range due to stability and time causality conflicts [Cripps'99]. Therefore, most of the time indirect feedback schemes are used, such as envelope feedback,

polar loop feedback and Cartesian loop feedback. Detailed discussions of each scheme can be found in [Sahu'04] and [Kenington'00].

Different from feedback methods, open loop methods are relatively simple and there are no bandwidth reduction or stability issues. Several methods such as feedforward, pre-distortion and linear amplification with non-linear components (LINC) are based on the open loop operation, but they are seldom used today due to various drawbacks [Lee-1'04].

Today a popular scheme for PA linearization is polar modulation. The idea originates from the envelope elimination and restoration (EER) technique first proposed by Kahn in 1952 [Kahn'52].

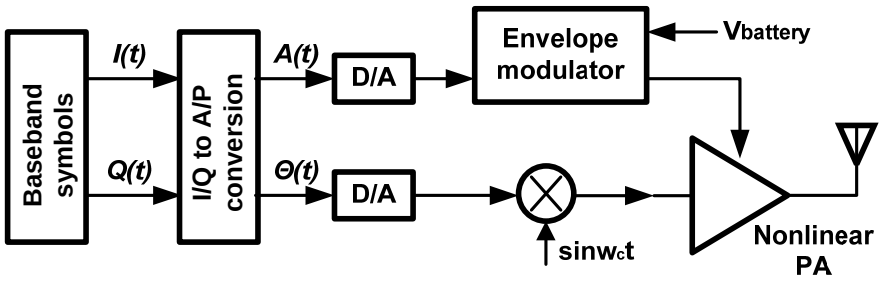


Figure 1.8 Schematic of polar modulation for a nonlinear RF PA

Fig. 1.8 illustrates the schematic of polar modulation. The baseband generator, which is often realized by digital signal processing (DSP) circuits, generates the in-phase signal $I(t)$ and quadrature-phase signal $Q(t)$. The relation between the baseband signals and the RF signal is give by:

$$v_{RF}(t) = I(t)\cos(\omega t) + Q(t)\sin(\omega t) \qquad (1.5)$$

This Cartesian form RF signal is then transferred to polar form, represented by an envelope signal and a phase signal:

$$v_{RF}(t) = A(t)\cos(\omega t + \theta(t)) \quad (1.6)$$

Now the PA is only processing the constant phase modulated signal, so a high efficiency PA can be used. The time varying envelope signal is then recombined with the phase signal by dynamically change the supply voltage of the PA through the envelope modulator, which often realized by a dc-dc converter. The major benefit of the polar modulation is to shift the linearity requirement from RF to the baseband envelope branch. Many well known techniques such as feedback can be directly applied at this low baseband frequency to improve the linearity of the envelope modulator. Moreover, the envelope modulator can be realized by a high efficiency switch mode power supply. Thus, an efficient high linearity PA can be achieved by using polar modulation.

The bandwidth of the RF signal depends on the wireless standard. For EDGE standard, the bandwidth is 200kHz, however, the envelope bandwidth is larger than 200kHz. In order for the envelope signal to pass through the envelope modulator, a large bandwidth and a high switching frequency are necessary, if the envelope modulator is realized by a switch mode power supply. This, in turn, degrades its light load efficiency. Moreover, delay mismatch of the phase and envelope branch should be compensated to avoid distortion [Reynaert'06].

1.4 PA Efficiency Boosting Techniques

Linear PA's efficiency is improved by adjusting the quiescent power consumption according to the output power, which is achieved by dynamically changing the supply voltage of the PA, thereby varying the PA's bias point. This method is called envelope

tracking. As shown in Fig. 1.9, in order to adjust the power supply efficiently and rapidly, a fast switching mode power supply is necessary.

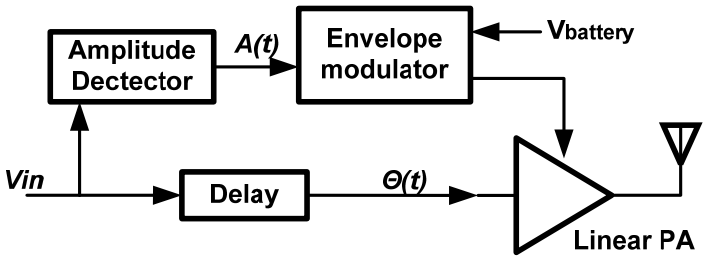


Figure 1.9 Schematic of envelope tracking method

Envelope tracking follows the PA's instantaneous output power, and therefore it can achieve high peak power efficiency. However in a wireless transmission system, because the PA works at power backoff most of the time, the average efficiency is of more concern than the peak power efficiency. Average power tracking method takes this into consideration, and it is similar to envelop tracking except that the power supply tracks the average transmitted power. It provides increased average efficiency for systems with large power control ranges and low peak to average power ratios.

1.5 Object and Thesis Outline

The objective of this work is to design an envelope modulator for EDGE polar modulation. The envelope modulator serves as the dynamic power supply for a class E nonlinear PA, therefore the efficiency should be maximized while the linearity should meet the EDGE spectral specification.

The thesis is composed of six chapters and is organized as follows: Chapter 1 is the introduction and presents the background. The need for prolonging the battery life in wireless

systems is stressed. The PA's linearity-efficiency tradeoff is discussed and some solutions are provided.

In chapter 2, several existing envelope modulator structures are reviewed in terms of their performance based on efficiency, noise and cost. The two stage solution is proposed based on the input and output voltage requirement of EDGE standard.

In chapter 3, the first stage high efficiency voltage doubler design is introduced and analyzed.

Chapter 4 introduces the implementation of the second stage 10MHz current mode buck converter. Efficiency optimization and system simulation results are demonstrated.

Chapter 5 discusses the comparison of different two stage structures. Finally the summary of this thesis and future research plans are presented in chapter 6.

Chapter 2 Literature Review of Dynamic Power Supply Techniques and Proposed Two Stage Modulator Structure

As discussed in the chapter 1, dynamic power supply techniques can improve the efficiency of the linear PA and the linearity of the nonlinear PA. A summary of state-of-the-art dynamic power supply techniques highlighting their key advantages and disadvantages is presented in Table2.1.

Table2.1 Comparison of different dynamic power supply methods

Method	Advantages	Disadvantages
Envelope Tracking	High peak power efficiency	High switching frequency for DC/DC converter. Requirement for delay mismatch
Average Envelope Tracking	Increase average efficiency	Low peak power efficiency
Polar Modulation /EER	High peak power efficiency	High switching frequency for DC/DC converter. Requirement for delay mismatch

Numerous publications have addressed dynamic power supply techniques in recent years. Section 2.1 serves as the literature review of current dynamic power supply methods. Different switch mode power supply structures are compared in terms of efficiency, complexity and spectral performance in section 2.2. The proposed two stage structure suited for EDGE polar modulation is introduced at the end of this chapter.

2.1 Literature Review of Previous Work

Table 2.2 highlights publications that are representative of previous research in the field of dynamic power supply of PAs, comparing the envelope modulators for various

applications in terms of structures, switching frequencies and efficiencies. It is important to note the difference between the maximum efficiency and the average efficiency, the former parameter is only specified at maximum output power and therefore may not directly related to the battery life, as discussed by Sevic [Sevic'97]. It is the average energy efficiency, which takes the PDF of transmitted signal into consideration, determines the battery performance in the RF transmitter.

Table2.2 Summary of previous researches on dynamic supply of PAs

*** PA and envelope modulator**
**** Envelope modulator only**

Method	Author	Modulator Type	Application	Envelope Bandwidth	Switching Frequency	Max Efficiency	Average Efficiency	Reference
Envelope Tracking	Midya,etc (Motorola)	Buck	QPSK	160kHz	800kHz	90%**		[Midya'01]
	Schlumpf,etc (EPFL)	Buck	IS95-CDMA	1.5MHz	16MHz	85%**@95mA		[Schlumpf'04]
	Wang, etc (UCSD)	Hybrid Buck	OFDM	20MHz	100MHz	30%*@0.1W		[Wang-1'05]
	Hanington,etc (UCSD)	Boost	IS95-CDMA	1.22MHz	10MHz	65%**@0.2W 74%**@1W	6.38%*	[Hanington'99]
Average Envelope Tracking	Staudinger,etc (Motorola)	Buck	IS95B-CDMA	500kHz	5MHz	90%**	11.4%*	[Staudinger'00]
	Sahu, etc (Georgia Tech)	Buck-Boost	IS95-CDMA	1.5MHz	500kHz	10%**@LL 65%**@HL	6.78%*	[Sahu'04]
Polar Modulation/EER	Su, etc (Hewlett-Packard Lab)	Delta	NADC			49%*@1W		[Su'98]
	Nagle, etc (M/A-COM Eurotec)	Interleaving Delta		800kHz		80%**		[Nagle'05]
	Wang, etc (UC Boulder)	Buck		12kHz	200kHz	60%* 96%**		[Wang-2'04]
	Jiang, etc (UC Boulder)	Buck	EDGE	1MHz	4.3MHz			[Jiang'06]
	Jinseok, etc (SPEC)	Buck-Boost	EDGE	1MHz	10MHz		82%**	[Jinseok'08]

2.1.1 Envelope Tracking

As discussed in section 1.3, the supply voltage of the PA is dynamically changed according to the output power level in an envelope tracking system. As a result, the PA operates at high efficiency even in the power backoff range.

Midya from Motorola described a buck envelope modulator used for a 25 kHz QPSK signal [Midya'01]. Sensorless current mode control is used and the buck converter can achieve a maximum efficiency of 90% at the switching frequency of 800 kHz. The efficiency of the whole transmitter is about 50% at 20W peak RF power. This is twice as efficient as using a constant power supply class AB PA.

Schlumpf proposed a buck converter used for CDMA application [Schlumpf'04]. Its switching frequency is 16MHz, which makes it capable of tracking the 1.5MHz envelope bandwidth, and the efficiency of the modulator is 85% at an output voltage of 1.25V and a load current of 95mA. Simple hysteretic control is used.

In [Hanington'99], a boost dc-dc converter with an operating frequency of 10MHz was demonstrated using a GaAs HBT, which can boost the power supply of PA to between 3V and 10V when the output power is larger than 18dBm. The efficiency of the converter is in the range of 65%-74% for output powers in the range of 0.2-1W. The overall average efficiency of the transmitter was reported as 6.38% for dynamic power supply, compared to 3.89% for a 10V power supply PA.

Wang proposed a hybrid buck converter for an envelope tracking PA used for a WLAN802.11g application [Wang-1'05]. With the combination of a linear regulator and a switching regulator, the converter can adjust the supply voltage at a frequency of over

20MHz. The overall system peak drain efficiency was reported as 30% at the output power of 0.1W.

2.1.2 Average Envelope Tracking

An average envelope tracking method increases the average efficiency by tracking the RMS value of the output power level. Staudinger from Motorola introduced a buck converter that serves as an envelope modulator for a CDMA application [Staudinger'00]. Working at a 5MHz switching frequency, the converter can achieve 90% peak efficiency. The system average efficiency is increased from 2.2% to 11% by changing the PA's supply voltage.

Sahu from Georgia Institute of Technology proposed a buck-boost average envelope tracking modulator for a CDMA application [Sahu'04]. The switching frequency of the converter is 500 kHz with an efficiency of 10%-65% over 0.4V-4V output. The overall system average efficiency is improved to 6.78%, which is 4 times better than the fixed supply efficiency.

2.1.3 Polar Modulation/EER

Polar modulation/EER can be done by amplitude modulating the supply voltage of a nonlinear PA through an envelope modulator. In [Su'98] and [Nagle'05], the envelope modulator uses delta modulation. The paper written by Su claimed the maximum efficiency of the transmitter is 30% at the output power of 1W. Nagle proposed the interleaving delta modulation method and enables the envelope modulator to achieve a maximum efficiency of 80%.

Wang from the University of Colorado at Boulder demonstrated the design of a 10 GHz drain modulated class E PA using a buck converter as the envelope modulator [Wang-2'04]. The switching frequency of the buck converter is only 200 kHz and 96% peak efficiency can be achieved, the peak efficiency of the whole system is reported as 60%.

In 2006, Jiang proposed a buck envelope tracker for a Polar EDGE transmitter [Jiang'06], which switches at 4.33 MHz with the capability of tracking 1.3 MHz of envelope bandwidth. The controller design for the buck converter produces an overall Bessel type low-pass transfer function, which gives a constant time delay for the envelope modulator. However, the efficiency of the converter is not reported.

An envelope tracker for EDGE polar modulation is also addressed in Jinseok's paper [Jinseok'08], A 10MHz 4 switch buck boost converter (4SBBC) is used, which uses current mode control. The average efficiency for the converter is 82% when the input battery voltage is 3.3V and the output voltage changes from 0.7V to 5V based on the EDGE standard.

2.2 Switch Mode Power Supply Circuits Structure

The envelope modulator realized by the dc-dc converter is the most important block of the RF transmitter, which transforms a fixed battery supply into different voltage levels for dynamic supply of a PA. Different envelope modulator structures are discussed in the preceding section. For battery powered systems and wireless application, the important specifications for the dc-dc converters are high efficiency, low cost and low spurious noise. Switch mode dc-dc converters can be divided into three categories: linear regulator, switching regulator and switching capacitor structure. Each structure is discussed briefly.

(a) Linear Regulator

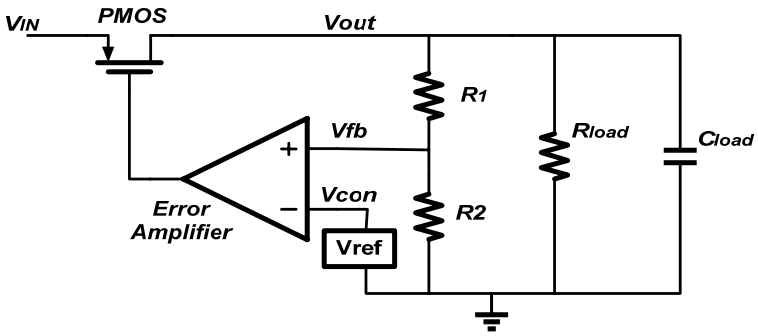


Figure 2.1 Schematic of a linear regulator

Fig. 2.1 illustrates the schematic diagram of linear regulator. The passive transistor (PMOS in the graph) operates in the saturation region and connects between the input and the output. An error amplifier is used in the negative feedback loop to ensure that the output voltage is equal to the control voltage, which in turn is usually generated by bandgap reference circuits. By controlling the voltage drop across the passive transistor, the output voltage can be regulated regardless of change in the input voltage or load current. When the output voltage is regulated to a voltage very close to the input voltage, the regulator is said to work in dropout mode and the transistor is forced to work in the linear region.

The power loss of the linear regulator depends on the load condition and voltage ratio. Specifically, the efficiency can be calculated as:

$$\eta\% = \frac{V_{OUT} I_{LOAD}}{(V_{IN} - V_{OUT}) I_{LOAD} + V_{OUT} I_{LOAD}} \doteq \frac{V_{OUT}}{V_{IN}} \qquad (2.1)$$

[Rincon-Mora'02]. So a linear regulator can only achieve high efficiency in the region where the input and output voltage are close, which is not well suited for a dynamic power supply where the output voltage not only always changes, but also always below the input voltage.

Although linear regulator is easy to design, the abovementioned drawbacks limit its application.

(b) Switching Regulator

A switching regulator is the most commonly used structure in dc-dc converter design. Its merit lies in the fact that for a fixed input voltage, both efficient step-up (boost) and step-down (buck) voltage conversion can be achieved. Fig. 2.2 shows the synchronous buck converter for lowering the input voltage. The gate voltages of the transistors are controlled so that they are “on” and “off” respectively, and as the result, the input voltage is chopped at the summing node. An inductor and a capacitor form a low pass filter. The output voltage is the average of the chopped voltage, which is fed back to an error amplifier and control circuits to generate the correct pulse width to control the transistor. This is called pulse width modulation (PWM) and the feedback scheme is used to ensure the regulation of the output voltage [Ericsson’02].

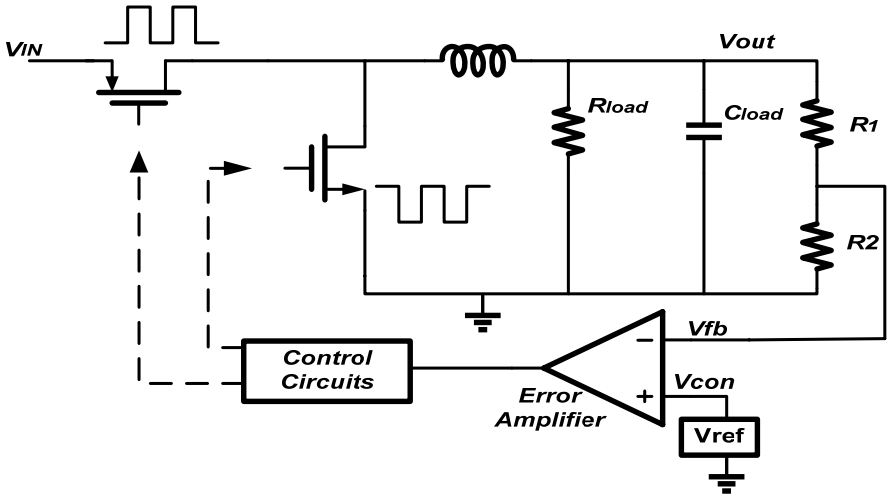


Figure 2.2 Schematic of a step down switching regulator

Theoretically the efficiency of the switching regulator is 100% because the inductor and capacitor do not consume power, and the voltage and current do not both cross the transistor at the same time. However, there will be a short V-I overlap in reality which will dissipate power. Also the inductor and capacitor's parasitic resistances will consume some power. Even taking all the parasitics into consideration, the switching regulator can still achieve very good efficiency. The output voltage is not constant and there will be a switching ripple at the output, which in turn generates some noise in the spectrum domain, for a switching regulator used in a dynamic power supply system, methods should be taken to ensure that the output ripple noise does not exceed the spectrum mask for the required specifications.

(c)Switching Capacitor Circuits

Switching capacitor circuits, also known as charge pumps, are well suited for battery-powered applications since there are no inductors in the structure, only external capacitor are required for voltage conversion, and therefore they are compact and low cost, they also have spectral performance superior to that of the switching regulators [Maxim].

Fig. 2.3 shows the schematic of a simple voltage doubler. The switches are controlled in such a way that S1 and S2 first turn on half of the period. The flying capacitor connects in parallel with the input and it is charged to a voltage equal to the input voltage. Then S3 and S4 turn on while S1 and S2 turn off for the rest of the period. Since the voltage drop across the flying capacitor cannot change instantly, it connects in series with the input so that twice the input voltage can be generated at the output.

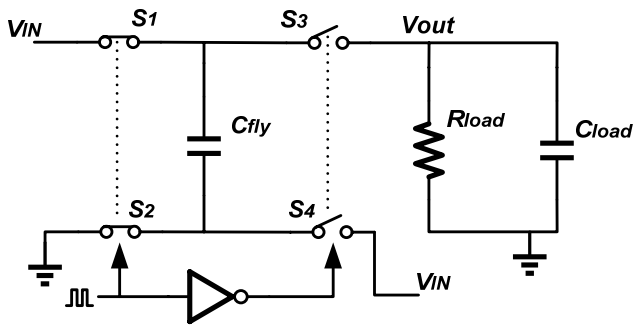


Figure 2.3 Schematic of a voltage doubler

The efficiency of a charge pump is ideally 100%. However, when charging and discharging the capacitor C, there will be energy loss in each switching cycle as:

$$E_{LOSS} = (1/2)C\Delta V^2 \qquad (2.2)$$

The conduction loss due to the equivalent resistors of the switches will also decrease the overall efficiency.

From the above analysis, switching regulators and the charge pumps are the suitable candidates for dynamic power supply of PAs.

2.3 Proposed Low Noise, High Efficiency Envelope Modulator Structure for EDGE Polar Modulation

The PA serves as the load for a dc-dc converter envelope modulator. A class E PA can be modeled as a constant resistor [Sokal'75]. Based on the EDGE output power requirement and the specification of a 17dB PAR [3GPP'05], the output voltage of the envelope modulator changes from 0.7V to 5V. The input voltage of the envelope modulator is connected to the battery. A lithium-ion battery is typically used, as it has a higher energy density than its Ni-Cs/Ni-MH counterparts. The battery voltage is about 4.2V when fully

charged and 2.7V when fully discharged, with a nominal operating voltage of 3.3V [NSC]. Due to the input and output voltage requirements of the envelope modulator, both step-down and step-up voltage conversions are needed.

Another feature of the EDGE signal can be revealed by its frequency domain information. As shown in Fig. 1.1, the complex EDGE signal has the most energy within the bandwidth of 200 KHz. However, the bandwidth of the envelope has a wider spectrum. The bandwidth needed for the envelope modulator is 1-2MHz [Jinseok'08], which means the switching frequency should be much higher.

In recent years, numerous papers address dynamic power supply design for EDGE polar modulation. Many of the polar transmitters still use low dropout (LDO) linear regulators to realize the modulators for simplicity, resulting in low average energy efficiency. Others use switching regulators but have other drawbacks. In [Jiang'06], the battery voltage is fixed at 3.6V, and therefore the envelope modulator cannot make full use of the battery voltage range. Jinseok takes the characteristics of the battery into consideration and proposes a 4SBBC structure for realizing the envelope modulator. As shown in Fig. 2.4 [Jinseok'08], four switches are controlled to give the step down or step up functions based on the requirement.

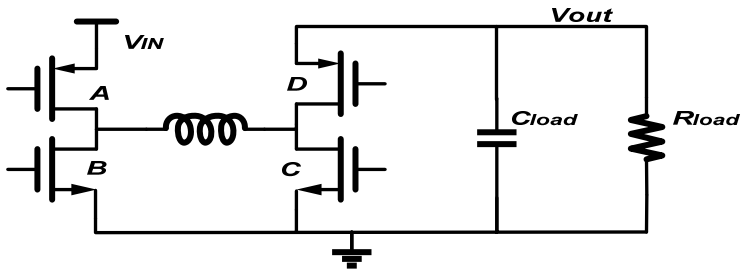


Figure 2.4 Schematic of 4SBBC

Fig. 2.5 illustrates the spectrum simulation results of the 4SBBC structure. Although the average efficiency is good and the in band spectrum meets the EDGE standard, the out-of-band spurious noise exceeds the EDGE spectrum mask at the switching frequency of 10MHz and its harmonics.

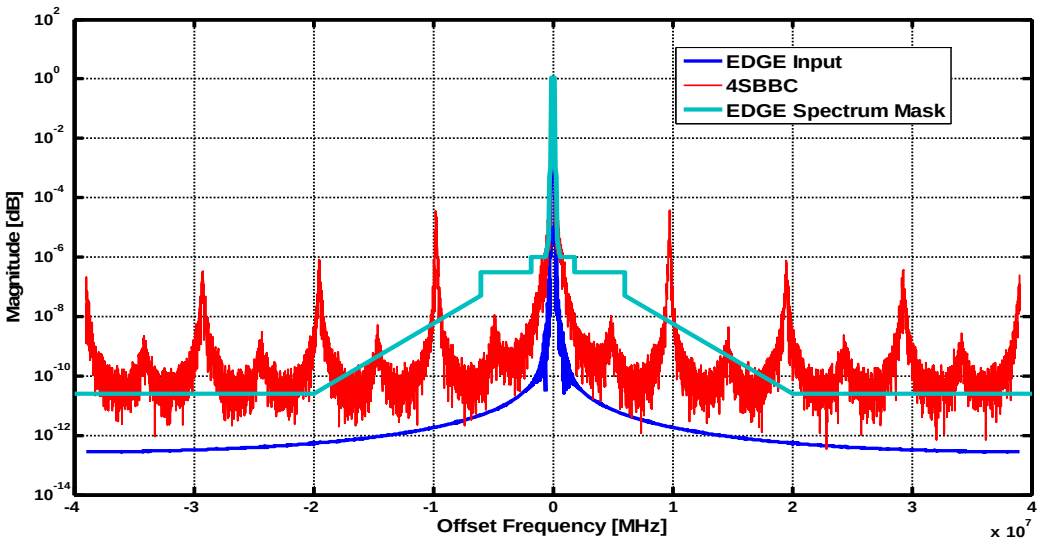


Figure 2.5 Spectrum simulation results for 4SBBC (Courtesy of Jinseok Park)

Most of the switching spurious noise is generated when the 4SBBC works in the step-up (boost) region. Here the inductor is connected to the input and all the current flows to the output to charge the output capacitor, which in turn generates large ripple voltage at the output, resulting in spectral performance deterioration. The same problem does not occur when 4SBBC works in the step-down (buck) region, where the inductor is connected to the output and only inductor ripple current follows to the output capacitor. The noise performance in this case is much better than the boost case.

From the above analysis, if we can get rid of the high noise boost region of the 4SBBC and only use the buck converter, the output switching spurious noise will be reduced

and the EDGE specifications can be met. The proposed two stage structure is based on this idea. Fig. 2.6 shows the proposed envelope modulator structure for EDGE polar modulation. Instead of using 4SBBC, a high efficiency charge pump is used as the first stage to boost up the battery voltage, and then a buck converter is used as the second stage to step down the voltage based on the EDGE output specification.

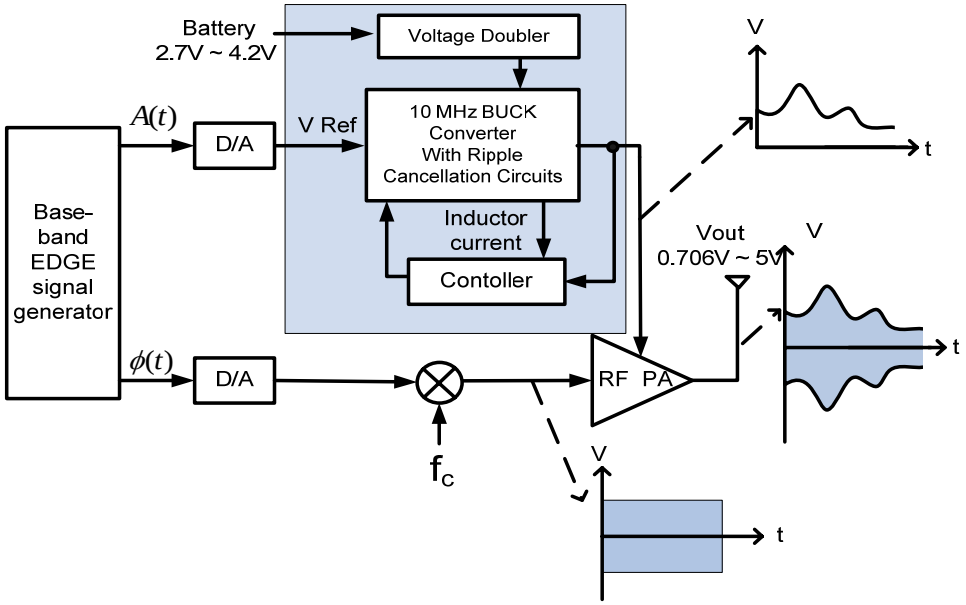


Figure 2.6 Proposed two stage envelope modulator structure

Compared to a linear regulator, a buck converter is more energy efficient for the dynamic output voltage applications, and high overall efficiency is achieved if a high efficiency charge pump is used as the first stage to boost the voltage. On the other hand, a buck converter has better spectrum performance than the buck-boost counterpart. In order to further reduce the noise, ripple cancellation circuits are added to the buck converter. The detailed design of the proposed two stage envelope modulator will be discussed in the following two chapters. Chapter 3 addresses the design of a high efficient charge pump as the

first stage, and chapter 4 discusses the implementation of the buck converter, as well as the system simulation results when the two stages are connected together.

Chapter 3 First Stage High Efficiency Charge Pump Design

As discussed in the preceding chapters, the input voltage for envelope modulator is set by the Li-ion battery as from 2.7V to 4.2V, and the output voltage is changing between 0.7V to 5V determined by the EDGE standard. Although buck-boost converter seems to be a good candidate for this application, the output spectrum cannot meet the EDGE requirement [Jinseok'08], and therefore charge pump circuits followed by a buck converter is proposed. In this two stage envelope modulator design, the role of the charge pump circuits is to boosting the battery voltage to higher level so that only step down conversion is necessary in the second stage. For the worst case condition, the 2.7V input voltage should be boosted to above the maximum output voltage 5V so as to make full use of the battery, as the result, voltage doubler is a possible solution for this condition. High efficiency is crucial for charge pump design, and since the output of the charge pump is connected to the input of the buck converter, the ripple generated by charge pump will propagate to the second buck stage, therefore low ripple voltage at the output is preferred.

The voltage doubler structure and its working principle will be discussed in section 3.1, followed by the loss and efficiency calculation, parameter selection and efficiency optimization. Simulation results will be demonstrated at the end of this chapter.

3.1 Switching Capacitor Voltage Doubler Structure

In recent years, voltage doublers are widely used in battery-powered portable applications, such as provide a higher supply voltage for driving the light emitting diodes (LEDs) and the I/O circuitries. Among different voltage doubler structures, the cross-coupled

voltage doubler is the most commonly used topology. Fig. 3.1 shows the schematics of the cross-coupled voltage doubler [Favrat'98].

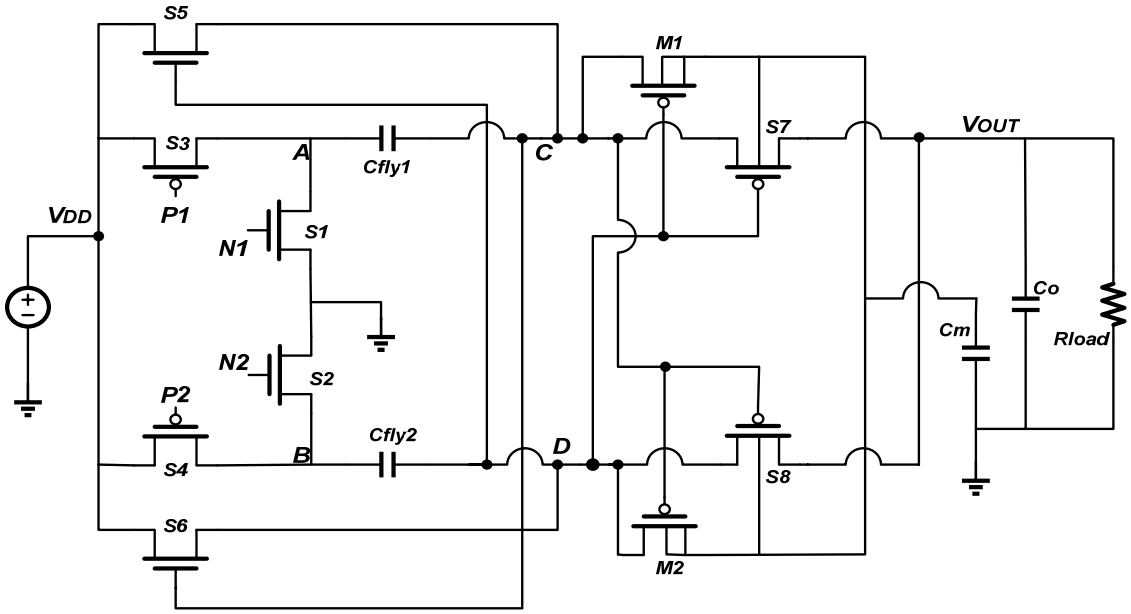


Figure 3.1 Voltage doubler structure

3.1.1 Operating Principle

As shown in Fig. 3.1, the voltage doubler can be considered as two identical branches, one branch consists of switch S1, S3, S5 and S7, auxiliary switch M1 and flying capacitor C_{FLY1}, the rest of the switches and C_{FLY2} are belong to another branch. Both branches share the same input voltage from the Li-ion battery, and the same output capacitor and load. The gate of switch S5 and S6, S7 and S8 are cross-coupled, which eliminates the need for separate bootstrap gate drivers.

The operation of the voltage doubler can be illustrated as follows: P1 and N1, P2 and N2 are connected to clock drive signals changing from 0 to V_{DD} with the duty cycle of 50%, respectively. When the voltage at P1 and N1 is V_{DD} while at P2 and N2 is 0, switch S4 is on

so that the voltage at node B is V_{DD}, since C_{FLY2} was charged to V_{DD} in the previous half cycle and the voltage across the capacitor cannot change abruptly, the voltage at node D will be pumped to $2V_{DD}$. On the other hand, S1 is on and node A is approximately at zero voltage, since the gate of S5 is connected to node D which is $2V_{DD}$, S5 will also on and the capacitor C_{FLY1} will be charged to V_{DD} through S5 and S1. On the other hand, the voltage at node C and node D is V_{DD} and $2V_{DD}$, respectively, switch S8 turns on and the output capacitance is charged to $2V_{DD}$ through switch S4 and S8. In another half cycle, the voltage at node C and node D will be opposite and the output capacitance will also be charged to $2V_{DD}$ through S3 and S7.

The auxiliary switches M1 and M2 are important in this structure because they can prevent the bulk of S7 and S8 from switching. For standard n-well CMOS technology, the cross-section of PMOS in a p-substrate is shown in Fig. 3.2 with its equivalent schematics [Favrat'98], there are two vertical and one lateral parasitic bipolar transistors exist in this structure, which results in difficulty for accurately modeling the switches, and if these parasitic transistors are triggered on, leakage current will flow from drain and source to ground, which in turn increase the power loss.

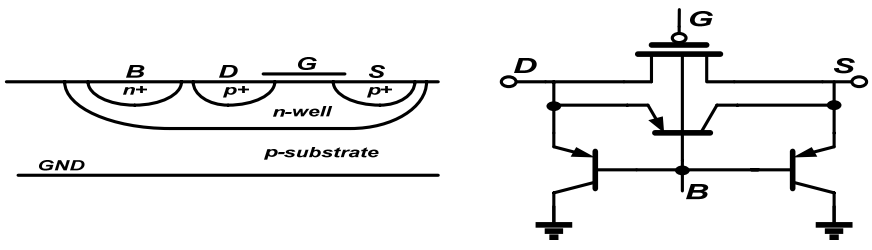


Figure 3.2 Cross section and equivalent schematic of the PMOS in n-well process

The only possible solution to get rid of the parasitic transistors is to tie the bulk terminal at the highest voltage between source and drain, and that is exactly why the auxiliary switch M1 and M2 are used, they are controlled in such a way so that the bulk of the main switches S7 and S8 always stay at highest voltage between there sources and drains, and therefore bulk switching is prevented.

3.1.2 Non-Overlapping Clock Design

For voltage doubler structure shown in Fig.3.1, P1 and N1, P2 and N2 should not be turned on at the same time, otherwise the short-circuit current will flow from the battery to ground and increase the power loss. On the other hand, we should also make non-overlapping drive signals at P1 and P2, N1 and N2 to prevent the discharging current to the ground. Therefore drive circuits should be carefully designed and non-overlapping clock should be generated.

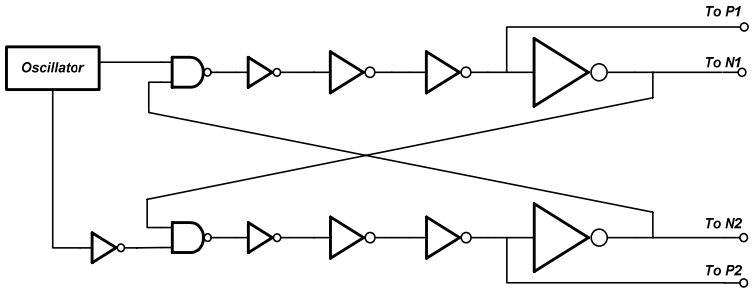
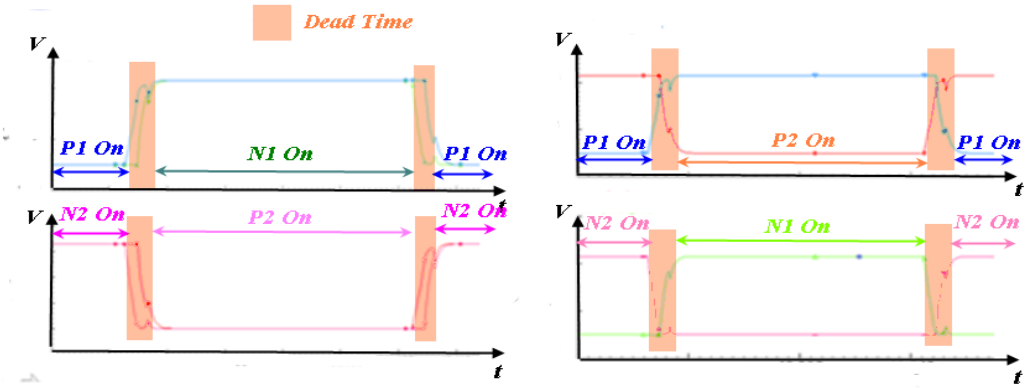


Figure 3.3 Non-overlapping clock generator

The schematic of the non-overlapping clock generator is shown on Fig. 3.3. Cross-coupled NAND gates are used to generate the non-overlapping signal, inverter chains are

inserted to adjust the dead time and increase the drive capability. The cadence simulation results in shown in Fig. 3.4 and illustrated its functionality.



(a) Waveforms at P1 and N1, P2 and N2 **(b) Waveforms at P1 and P2, N1 and N2**

Figure 3.4 Simulation waveforms of the driver signals

3.2 Efficiency Calculation

Unlike the switching regulators, the charge pump circuits usually works at open loop and fixed frequency [Wang-3'97]. The power loss of the voltage doubler consists of two parts: resistive power loss which depends on the load currents, ESR of the flying capacitors, on-resistances of the switches, and dynamic power loss which relates to the switch size, output voltage and switching frequency. The modeling of voltage doubler and efficiency calculation method will be discussed in the following section.

3.2.1 Conduction Power Loss

At steady state, the switches are operating in the linear region, if we ignore the channel length modulation effects, the on-resistance R_S of the switch is:

$$R_S = \frac{L}{\mu C_{ox} W (V_{GS} - V_T)} \qquad (3.1)$$

Where μ is mobility, C_{ox} is the capacitance per unit area of the gate oxide, W and L represents the switch width and length, V_{GS} is the gate to source voltage, and V_T is the transistor threshold voltage.

The equivalent resistance R_C and ESR of the flying capacitors should also be taken into consideration, the equation to calculate R_C can be written as:

$$R_C = \frac{1}{2 f_S C_{FLY}} \qquad (3.2)$$

The factor 2 comes from the two flying capacitors which act at each phase of the clock cycle [Favrat'98]. So the total on-resistance R_{CON} for each half clock cycle is:

$$R_{CON} = R_C + 2R_S + R_{ESRC} = \frac{1}{2 f_S C_{FLY}} + \frac{L_n}{\mu_n C_{ox} W_n (V_{GSn} - V_{Tn})} + \frac{L_p}{\mu_p C_{ox} W_p (V_{GSp} - V_{Tp})} + R_{ESRC} \quad (3.3)$$

To simplify the design, the on-resistances of all the switches except the two auxiliary switches are assumed to be the same and voltage drop across each switch is ignored.

The voltage doubler then can be modeled as the voltage source $2V_{DD}$ and series connection of the on-resistance R_{CON} and the load resistance R_{LOAD}, Fig. 3.5 illustrates the equivalent modeling of the voltage doubler.

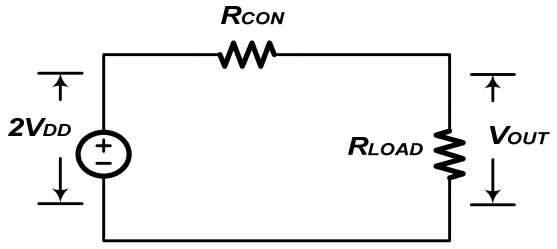


Figure 3.5 Equivalent modeling of voltage doubler

The output voltage V_{OUT} and output voltage drop ΔV_{OUT} due to R_{CON} can be calculated as:

$$V_{OUT} = 2V_{DD}\frac{R_{LOAD}}{R_{LOAD}+R_{CON}} \qquad (3.4)$$

$$\Delta V_{OUT} = 2V_{DD}\frac{R_{CON}}{R_{LOAD}+R_{CON}} \qquad (3.5)$$

3.2.2 Dynamic Power Loss

Dynamic power loss results from charging and discharging the capacitors. For the charging process, consider a simple circuit in Fig. 3.6, capacitor C is charged by the voltage source V_{DD} through a PMOS transistor. The energy drawn from the voltage source can be derived by integrating the instantaneous power over the charging period:

$$E_{VDD} = \int_0^\infty i(t)V_{DD}dt = V_{DD}\int_0^\infty C_L\frac{dV_{OUT}}{dt}dt = V_{DD}\int_0^{V_{DD}} dV_{OUT} = C_L V_{DD}^2 \qquad (3.6)$$

The energy stored by the capacitor is:

$$E_C = \int_0^\infty i(t)V_{OUT}dt = \int_0^\infty C_L\frac{dV_{OUT}}{dt}V_{OUT}dt = \int_0^{V_{DD}} V_{OUT}dV_{OUT} = \frac{1}{2}C_L V_{DD}^2 \qquad (3.7)$$

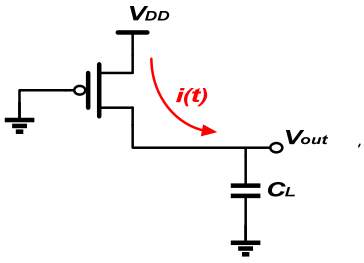


Figure 3.6 Charging a capacitor through a PMOS transistor

From (3.6) and (3.7), we can see half of the energy ($\frac{1}{2}C_L V_{DD}^2$) is lost in the charging process, during the discharging phase, the stored $\frac{1}{2}C_L V_{DD}^2$ energy will be removed from the capacitor,

so each switching cycle the dynamic loss is $C_L V_{DD}^2$, here V_{DD} is the voltage change across the capacitor.

The dynamic power loss for the voltage doubler can be calculated in the same way and all the capacitances should be taken into consideration. Apart from the two flying capacitors, there are parasitic capacitances at the gate, drain and source of the each switch, assume the total gate capacitance for each branch is C_g, and the capacitance at node A and C are C_A and C_C, respectively. The voltage at these nodes will swing between V_{DD} and $2V_{DD}$, so the voltage change across these parasitic capacitances is equal to V_{DD}. We can define the total parasitic capacitances C_P for each branch as:

$$C_P = C_A + C_C + C_g \qquad (3.8)$$

C_P is proportional to the gate width W and gate length L. The total dynamic energy loss can be calculated as:

$$E_S = 2C_P V_{DD}^2 + 2C\Delta V_{OUT}^2 \qquad (3.9)$$

The power efficiency is calculated by the following equation:

$$\eta\% = \frac{E_{LOAD}}{E_{LOAD} + E_S} \qquad (3.10)$$

E_{LOAD} is the energy delivered from the voltage source to the load and is calculated as:

$$E_{LOAD} = \frac{V_{OUT}^2}{f_S R_{LOAD}} \qquad (3.11)$$

By substitute (3.4), (3.5), (3.9) and (3.11) into (3.10), the result is:

$$\eta\% = \frac{1}{1 + C_P f_S \frac{(R_{LOAD} + R_{CON})^2}{2R_{LOAD}} + 2C_{FLY} f_S \frac{R_{CON}^2}{R_{LOAD}}} \qquad (3.12)$$

R_{CON} is given by $R_{CON} = \frac{1}{2 f_S C_{FLY}} + \frac{L_n}{\mu_n C_{ox} W_n (V_{GS\,n} - V_{T\,n})} + \frac{L_p}{\mu_p C_{ox} W_p (V_{GS\,p} - V_{T\,p})} + R_{ESRC}$ (3.3).

From (3.3) and (3.12), the efficiency of the voltage doubler is affected by many factors, such as switching frequency, output voltage, gate size, load condition and flying capacitance. There are tradeoffs in selecting these parameters, for example, if the switch length L is fixed, increase the switch width W will decrease its on-resistance, and in turn decrease the conduction loss, but the switching loss will increase due to larger parasitic capacitance.

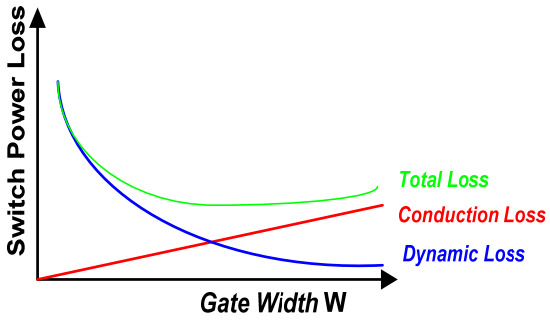


Figure 3.7 Switch power losses versus gate width

Fig. 3.7 shows the conduction and dynamic loss as the function of the switch width [Stauth'06], as indicated in the graph, there exist an optimal width of the switch so that the total loss is at the minimum. Next section will discuss how to select the abovementioned parameters in order to get high efficiency, and the general design flow will be summarized.

3.3 Design Flow

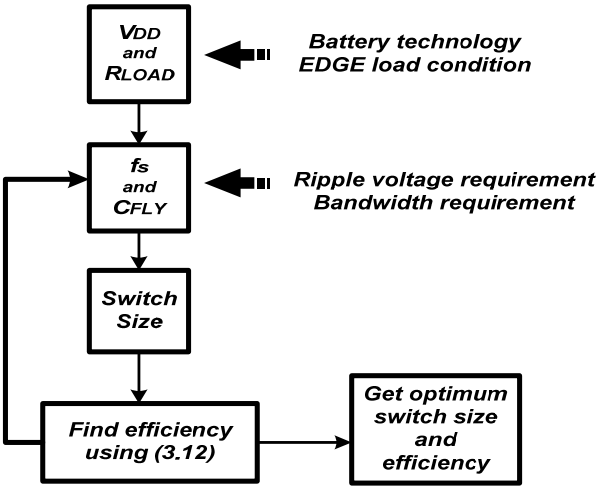


Figure 3.8 Design flow of voltage doubler

The voltage doubler design process is based on the specification of EDGE system and semiconductor process information, the goal is to achieve optimum efficiency by using (3.12) derived in the previous section. Fig. 3.8 illustrates the design flow of the voltage doubler.

The input voltage of the doubler comes from the Li-ion battery and it will decrease gradually as time goes by, on the other hand, the load condition is also changing based on the EDGE standard time domain information, which makes it complicate and time consuming to select the design parameters, many iterations are necessary in order to find the optimum efficiency. For simplicity, the design and optimization procedure of the voltage doubler is at the nominal battery voltage and most frequently occurred load condition, and then check and iterate the design process for the entire load range if necessary. This design procedure will save lots of time and still get the sub-optimum results.

First of all, input voltage is chosen based on the battery technology, and then we should define the load condition for the doubler, since the output voltage is followed by the

buck converter and the output of buck converter is fast changing EDGE signal, the input current of the buck converter (also the output load current for voltage doubler) will vary based on the time domain EDGE information. For simplify the design procedure, we will find the optimum efficiency at one load condition which occurs most on the PDF of EDGE standard, then maximize the efficiency for the whole load range.

Secondly, switching frequency and flying capacitor is chosen based on the ripple voltage requirement, different switch size is selected and equation (3.12) is used to calculate the efficiency, since there is a tradeoff between the conduction loss and dynamic loss, an optimum point should be found, and several iteration may be needed to get the optimum size and efficiency. The detailed parameter selection procedure will be illustrated in the next section.

3.4 Parameter Selection and Efficiency Optimization

(a) Input voltage and load condition selection

Li-ion battery is used as the input power source for its high power density, the nominal input voltage is 3.3V [NSC], and therefore the input voltage is picked up as this voltage.

The output of the voltage doubler is connected to the input of the buck converter, which is then connected to PA. According to the voltage probability statistic chart of EDGE standard shown in Fig 3.9, the voltage of EDGE signal is more likely to be located between 2.3 and 4.7V. PA serves as the load of the buck converter and can be modeled as a 5Ω resistor [Sokal'75], which determines the output power range of the buck converter as

between 1.1W and 4.5W. The doubler should provide the second stage buck converter with such variable power, as the result, the load current of doubler is changing between 0 and 1A. In the efficiency optimization procedure, we select the load for the doubler in this range.

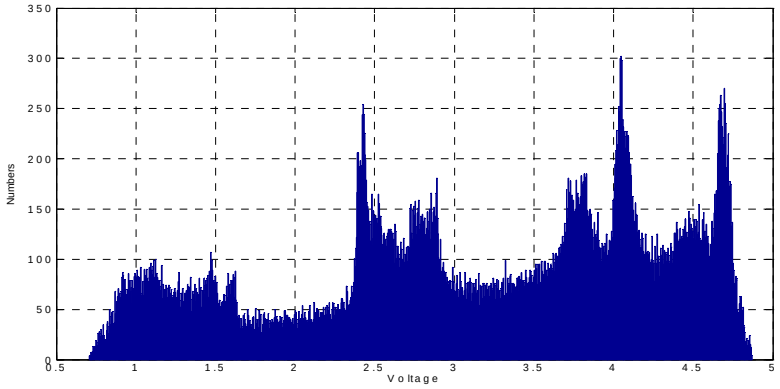


Figure 3.9: Time domain voltage probability statistic chart of EDGE signal

(b) Switching frequency and capacitor selection

Next step is to select the switching frequency. For this parallel, opposite-phase driven voltage doubler structure, the effective ripple frequency at the output is twice the driver frequency of the flying capacitors. This voltage ripple will be connected to the input of the buck converter, in order to reduce the input ripple effects at the output of the buck converter, the ripple frequency should be selected within the bandwidth of the buck converter, under this condition the input ripple will be suppressed based on the close-loop transfer function of the buck converter [Ericsson'01]. The typical bandwidth requirement for envelope modulator used for EDGE polar modulation is around 1-2MHz [Jinseok'08], and therefore we pick up 1MHz ripple frequency as the starting point, which in turn requires the switching frequency of the voltage doubler as 500kHz.

The output capacitor is then selected based on the ripple voltage requirement. The ripple voltage at the output can be calculated as:

$$V_{ripple} = \frac{I_{LOAD}}{2 f_S C_{LOAD}} \qquad (3.13)$$

In order for the ripple voltage stay within 100mV range in the worst load condition, the output capacitor is chosen to be $6.8\mu F$.

The doubler consists of two anti-phase charge pumps. As we know, the flying capacitor in the charge pump is used as the voltage source. The dynamic loss on the capacitor is $C\Delta V^2$ in one cycle. If the capacitor is too small, then the charging and discharging process is fast, which results in a large voltage fluctuation ΔV on capacitor and increase the switching loss. As the result, parameter sweeping is used to determine the flying capacitor value in order to minimize the dynamic loss and in turn maximize the efficiency. Fig 3.10 shows the simulation results for the efficiency versus flying capacitance at $f_S = 500kHz$ and load current of 0.8A, which is the most occurred situation for EDGE signal, the ideal switches are used.

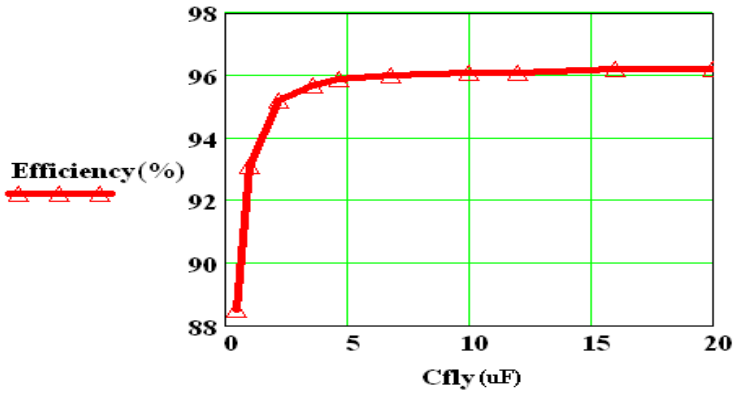


Figure 3.10 Efficiency versus flying capacitance value

From the simulation results, the flying capacitance C_{FLY} is chosen as $4.7\mu F$.

(c) Switch size selection

The length of all the switches is chosen to be the minimal channel length 0.6 μm based on the process so as to minimize the parasitic capacitance, and both the width of the NMOS and PMOS are swept to find the optimum efficiency.

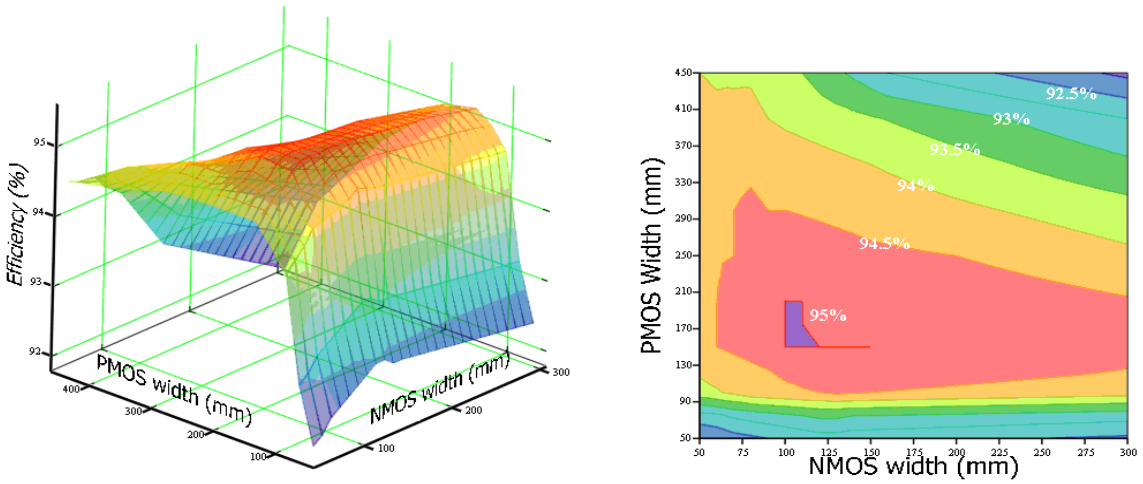


Figure 3.11: Contour graph of efficiency versus switch width

The simulation result shown in Fig.3.11 illustrates the relation between the efficiency and the switch width. As shown on the contour graph, the optimum PMOS width is 150mm, and the width for NMOS is 100mm.

For auxiliary switches M1 and M2, since they do not need to pass the high load current, small width of 1mm is chosen for their width and the length is the minimal length.

Finally, a summary of different parameters are shown on Table 3.1:

Table 3.1 Summary of the voltage doubler parameters

Technology	JAZZ 0.6um
Input Voltage Range	2.7~4.2V
Switching Frequency	500 kHz
Output Voltage	Vo=6.45V@Vdd=3.3V
Output Ripple	60mV@Vdd=3.3V, Iload=0.5A
NMOS Switch Size	W=100mm,L=600nm
PMOS Switch Size	W=150mm,L=600nm
Load Capacitor	6.8uF
Flying Capacitor	4.7uF

3.5 Simulation Results and Summary

As illustrated in last section, the parameter selection and efficiency optimization is based on the most frequently occurred load condition, in the real fact the load is changing based on the EDGE standard, and therefore the different load condition should be checked to ensure the high efficiency.

The comparison between the efficiency simulation results and calculated results based on equation (3.13) are shown in Fig.3.12 for different load conditions, the simulation results matches well with the calculated results. The voltage doubler can achieve around 95% efficiency under most of the load conditions.

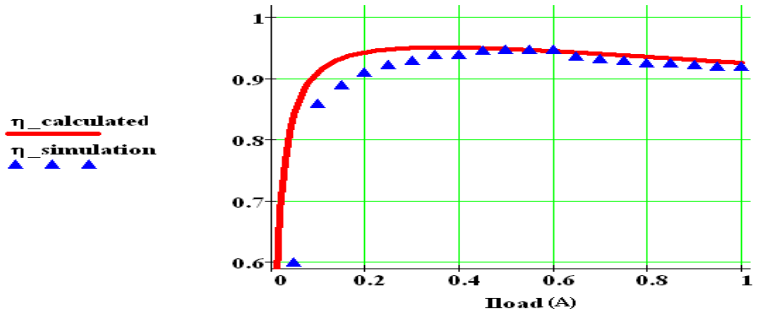


Figure 3.12 Efficiency versus load current

The output of the voltage doubler will be connected to the input of the second stage buck converter, which is used to step down the boosted voltage to the desired level determined by the EDGE standard, as the result, the characteristics of the voltage doubler, such as efficiency, output voltage, output ripple…etc, will all affect the second stage buck converter design, some parameters of the voltage doubler may be tuned later. In the chapter 4, how to design the second stage buck converter will be addressed and system simulation results will be shown.

Chapter 4 Second Stage Adaptive Buck Converter Design and System Simulation Results

The dynamic supply voltage for driving the PA in EDGE transmitter is always lower than the boosted voltage from the output of the voltage doubler, as the result, a step down dc-dc converter is required to sit in between so as to reduce the boosted voltage to the required level. The bandwidth of the converter should be large enough in order to pass the bandwidth limited envelope signal, and the output should follow the fast changing EDGE signal. On the other hand, high efficiency is always preferred to save the energy and prolong the battery life eventually.

Step down switch mode power supply is superior to the LDO counterpart because LDO suffers from low efficiency when the output voltage is low. Also, the output spectrum should meet the stringent EDGE mask, which means low noise is another important requirement, since the inductor is connected to the output and only ripple current flows to charge the output capacitor, so the output ripple is smaller compared to the buck-boost converter works in the boost region, where all the inductor current flows to the output capacitor and in turn cause large ripple noise [Jinseok'08]. In a word, high frequency buck converter is a good candidate for this application, considering its high efficiency, fast response, low noise and suitability for IC implementation.

In this chapter, the circuit topology of the adaptive buck converter and its design procedure is discussed in detail. In order to meet the stringent EDGE spectrum at the output, ripple cancellation circuits are added in order to further reduce the output voltage ripple noise,

which will be analyzed in the following section. Finally, power losses analysis, energy efficiency calculation and optimization are performed.

4.1 Circuits Topology and Operation Principle

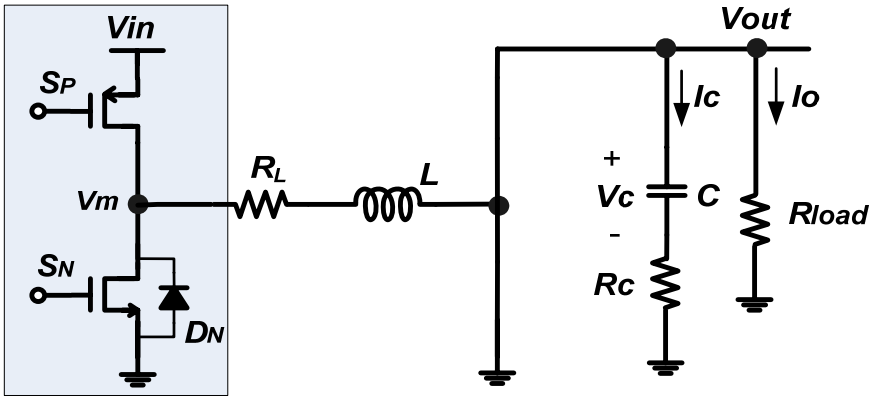


Figure 4.1 Schematic of synchronous buck converter

The schematic of the step down buck converter is shown in Fig 4.1, the synchronous NMOS switch is used to instead of the bottom rectifier diode, so there will be less voltage drop on the switch when it conducts, which in turn improves the efficiency of the converter. V_{IN} is the input voltage which connected to the output of the voltage doubler, V_{OUT} stands for the output dynamic voltage. PA is modeled as a constant load resistance R_{LOAD} for the buck converter. R_L and R_C are equivalent series resistance (ESR) of the inductor and output capacitor, respectively.

Two switches S_N and S_P are switching on and off alternately, so the voltage at node V_m acts like the chopped input voltage which is changing between V_{IN} and ground, then the inductor and capacitor acts like the low-pass filter and the average of the chopped voltage is

passed to output. Specifically speaking, during the T_{ON} time when the top PMOS switch is on and bottom NMOS is off, there will be positive voltage across the inductor, which provides the current to the load and charge the output capacitor, while during the T_{OFF} time when the NMOS switch is on, inductor voltage becomes negative, the output capacitor is discharged to provide the load current, the duty cycle D is defined as:

$$D = \frac{T_{ON}}{T_{OFF} + T_{ON}} = \frac{T_{ON}}{T} \qquad (4.1)$$

There is a short time delay known as dead time between the turn off of the PMOS and turn on of the NMOS, which is necessary to prevent the losses due to the shoot through current in the switch, since both switches are off during the dead time, the current will go though the body diode D_N of the bottom switch. The conventional steady state waveform of the buck converter is shown on Fig 4.2.

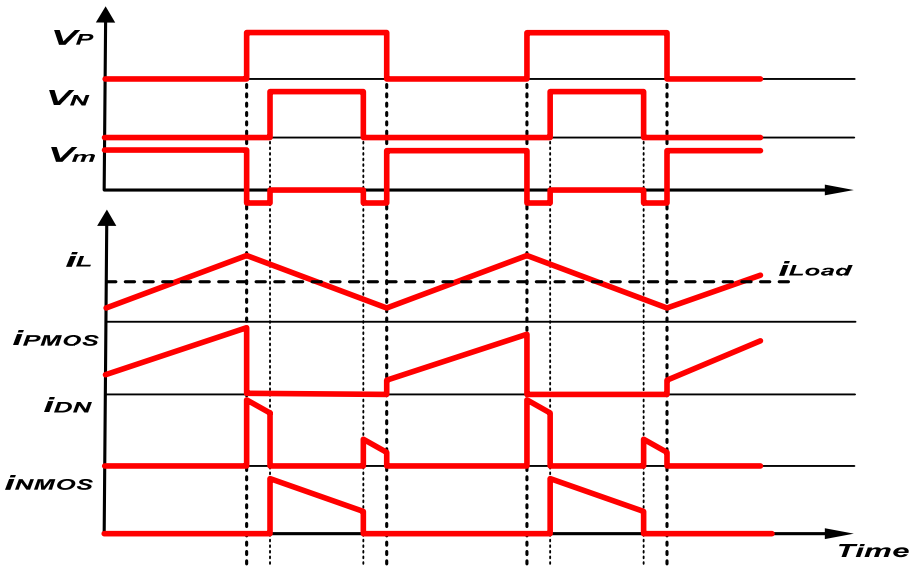


Figure 4.2 Steady state waveforms of buck converter

From Fig. 4.2 we can see only ripple current flow through the output capacitor in the steady state, as a result, the output ripple voltage is much smaller than the boost converter, where all the inductor current will flow through the output capacitor.

4.2 Power Stage Design

The bandwidth limited EDGE envelope signals should pass the adaptive buck converter with minimal distortion, therefore the bandwidth of the buck converter should be larger than t he bandwidth of the envelope signals, which is around 1-2MHz, so 10MHz switching frequency is chosen in order to achieve the desired bandwidth.

After chose the switching frequency, the corner frequency of the power stage can be decided, and the value of power inductor and output capacitor can be chosen accordingly. The schematic of the power stage, including all the parasitic, is shown in Fig 4.3:

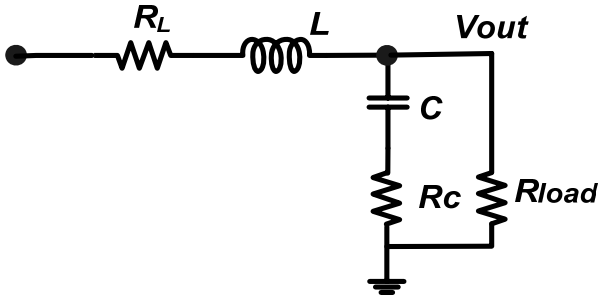


Figure 4.3 Schematic of Power Stage

In the reality, the ESR of the output capacitor R_C is usually very small, if we neglect the effect of the R_C in the transfer function, the power stage transfer function is:

$$H(s) = \frac{R_{LOAD}/(R_L + R_{LOAD})}{1 + (\frac{L}{R_{LOAD} + R_L} + \frac{CR_{LOAD}R_L}{R_{LOAD} + R_L})s + LC\frac{R_{LOAD}}{R_{LOAD} + R_L}s^2} \qquad (4.2)$$

It contains double-poles at corner frequency f_C, which can be written as:

$$f_C = \frac{1}{2\pi\sqrt{LC\frac{R_{LOAD}+R_L}{R_{LOAD}}}} \approx \frac{1}{2\pi\sqrt{LC}} \qquad (4.3)$$

The corner frequency should be chosen based on the bandwidth requirement and ripple suppression effects. First of all, power stage servers as the last stage of the envelope modulator and it must be able to pass the desired EDGE envelope signal, so the corner frequency should be chosen near the envelope bandwidth which is around 1MHz. On the other hand, if the corner frequency is set as 1/6 to 1/10 of the switching frequency, the worst case supply ripple will be around only 2% of the supply voltage, given the -40dB/decade attenuation of the power stage [Stauth'06]. Based on the abovementioned requirement, the corner frequency f_C is chosen to be approximately 1MHz.

The next step is to set the inductor and capacitor values, in the buck converter, the average inductor current is equal to the load current, which is given by:

$$I_{L(AVG)} = I_{LOAD} = \frac{V_{OUT}}{R_{LOAD}} \qquad (4.4)$$

The value of peak to peak inductor current ripple is selected such that the converter works in the continuous current mode (CCM) under worst case condition, which occurs when the load current is changing to its minimal value. So we can select the inductor L as:

$$L > \frac{(1-D_{MIN})V_{OUT(MIN)}}{2f_s\Delta I_L} \qquad (4.5)$$

$L = 280nH$ is chosen to ensure the CCM condition, and based on equation (4.3), the output capacitance is chosen to be 100nF in order to achieve the desired corner frequency.

The quality factor of the power stage is:

$$Q \approx \frac{R_{LOAD}}{2\pi f_C L} \qquad (4.6)$$

For quality factor less than ½, the poles are real and the effective -3dB bandwidth is less than the corner frequency in this case, so it is reasonable to choose quality factor larger than ½, so the double-poles become imaginary, which is the case for this design. The bode plot of the designed power stage is shown in Fig 4.4.

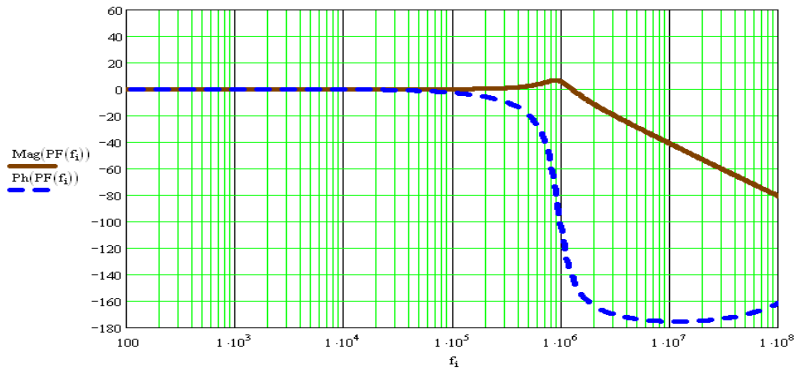


Figure 4.4 The bode plot of the power stage

4.3 Controller Design

Voltage mode and current mode control are the most widely used control schemes used in DC/DC converters. Different from the voltage mode control, there are two control loops in current mode controller. The inner loop inductor current information is sensed and feedback to make a comparison with the outer loop control voltage, as the result, the power inductor acts like a current source and does not involved in the total transfer function, which makes it easier to design the controller. In a word, current mode control scheme can give faster response and easier design of the compensator compared to voltage mode control, which is suitable to process the fast EDGE envelope signal with high stability.

The schematic of the designed current mode buck controller is shown in Fig 4.5. In the outer voltage loop, the difference of the output voltage and the reference EDGE signal is amplified by the error amplifier (EA) to generate the control voltage V_C , compensation circuits are added to shape the loop gain in order to make the system stable under all of the load conditions. On the other hand, the inner loop inductor current information is sensed by current sensor and transferred to voltage information, artificial voltage ramp generated from the oscillator should be added in order to solved the instability problem when duty cycle is larger than 0.5 [Ericsson'01]. Then the combined voltage is compared to the previous mentioned control voltage V_C to provide the duty cycle information, which is then feed into the driver circuits and dead time control circuits to generate the control signal for the main switches.

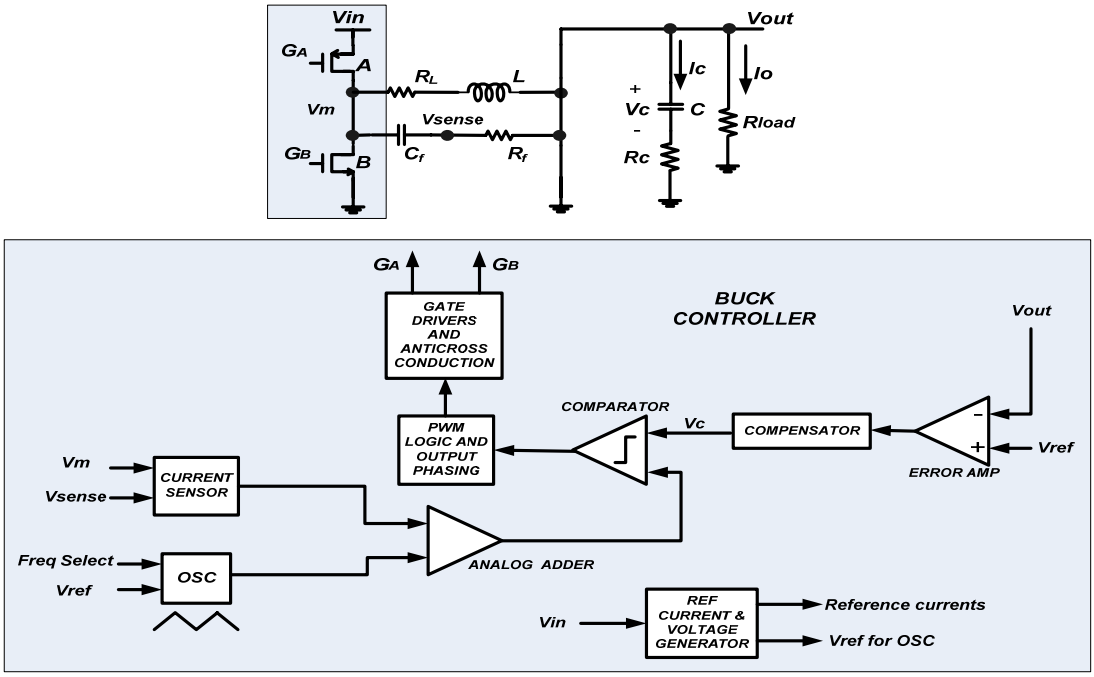


Figure 4.5 The block diagrams of the current mode buck controller

Current sensing circuits and compensator are the most difficult blocks for implementation, and the performance of which are very crucial for the system, the design and the implementation of the current sensing circuits and compensator circuits will be discussed in detail in the following sections.

4.3.1 Current Sensor and Analog Adder

"Filter-Sense the Inductor" method is used for sensing the continuous inductor current information [Forghani-zadeh'02]. This technique uses a RC network to filter the voltage across the inductor and sense the current though the inductor ESR, as shown in Fig 4.5, the voltage across the inductor is:

$$v_L = (R_L + sL)I_L \qquad (4.7)$$

The voltage across the capacitor is:

$$v_C = \frac{v_L}{1+sR_fC_f} = R_L I_L \left(\frac{1+s(L/R_L)}{1+sR_fC_f}\right) \qquad (4.8)$$

If we choose R_f and C_f such that:

$$R_fC_f = L/R_L \qquad (4.9)$$

The inductor current information can be related to capacitor voltage as: $v_C = R_L I_L$ (4.10).

There are two major design issues by using this current sensing technique. In buck converter, the switch S_A and S_B in Fig 4.5 are on and off alternatively, as the result, there will be wide voltage swing at sensing node V_m and V_{sense}, which are changing from ground to V_{DD} and vice versa. So rail to rail input common mode range is necessary at the input of the

current sensor for detecting the deferential voltage across C_f , which can be achieved by using both PMOS and NMOS together at the input stage.

On the other hand, the inductor current frequency is the same as the 10MHz switch frequency, to accurate sense such high frequency current information without distortion, the current sensor should have very fast response, active feedback amplifier (AFA) architecture is chosen for the mercy of the high speed [Brunner'94], [Pearson'03].

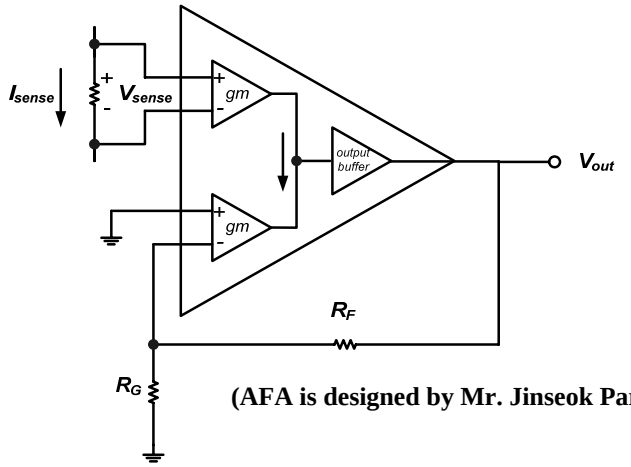


Figure 4.6 The block diagram of AFA

As shown in Fig 4.6, because of the infinite input impedance of output buffer in AFA, all the current generate from the top G_m block will flow to the bottom G_m block, if the transconductance of both G_m blocks are the same, the voltage at the input of the bottom G_m block will copy the sensed voltage with the opposite polarity, good separation between the signal input and the feedback network is achieved in this way. The copied voltage is then applied on R_G and amplified to the output by the following equation:

$$V_{OUT} = (1 + \frac{R_F}{R_G})V_{sense} \qquad (4.11)$$

The high speed analog adder in Fig 4.5 can be implemented by using the same AFA structure. As shown in Fig 4.7, the differential input voltage of two transconductance blocks should be the same but with opposite polarity, therefore we can get:

$$V_{sense} - 0 = -(V_{ramp} - V_{OUT})$$

$$V_{OUT} = V_{sense} + V_{ramp} \qquad (4.12)$$

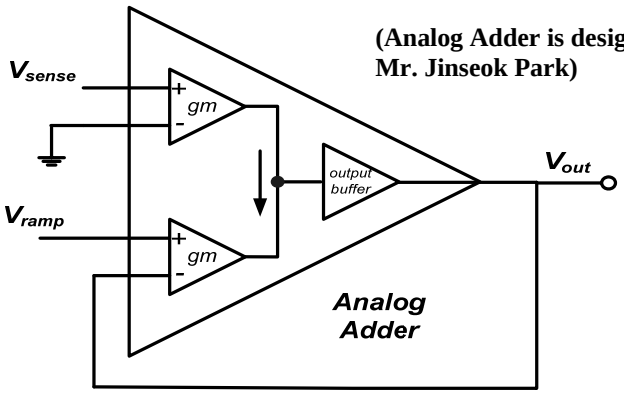


Figure 4.7 Schematic of Analog Adder Using AFA Structure.

4.3.2 Compensator Design

Since the inductor will not be involved in the overall transfer function, the compensator design is easier than voltage mode control. The control block diagram from the EDGE input to the output of the converter is shown in Fig. 4.8:

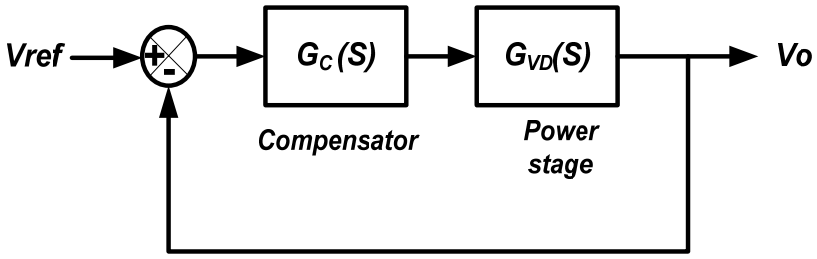


Figure 4.8 control diagram from the EDGE reference input to output

From Fig 4.8 we can get the loop gain T can be expressed as:

$$T(s) = G_C(s) \cdot G_{VD}(s) \qquad (4.13)$$

And the close loop relationship is:

$$\frac{V_{OUT}}{V_{ref}} = \frac{T}{1+T} \approx 1 \quad when\ T >> 1 \qquad (4.14)$$

Our design goal is to make the above equation valid up to the bandwidth of the EDGE reference signal, and the close loop crossover frequency should be around 1MHz.

As shown in Fig.4.9, one zero, two pole G_m structure is used for implementing the compensator, it has the faster response compared to the conventional Op-amplifier design.

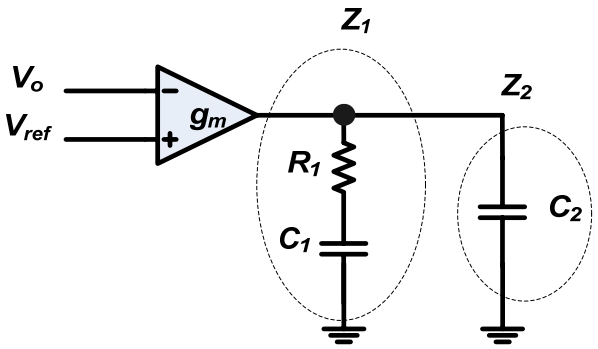


Figure 4.9 One zero two pole compensator

The transfer function of the compensator can be expressed as:

$$G_C(s) = -g_m(s)\left(Z_1 // Z_2\right) = \frac{g_m}{s\left(C_1 + C_2\right)} \frac{1 + sR_1C_1}{1 + sR_1 \dfrac{C_1C_2}{C_1 + C_2}} \qquad (4.15)$$

From (4.15), one pole is set at the origin so as to increase the gain at low frequency, the zero is chosen at the corner frequency of the power stage to cancel the effect of the pole, and the second pole is located at the higher frequency to suppress the high frequency noise. The bode plot of the compensator is shown in Fig. 4.10.

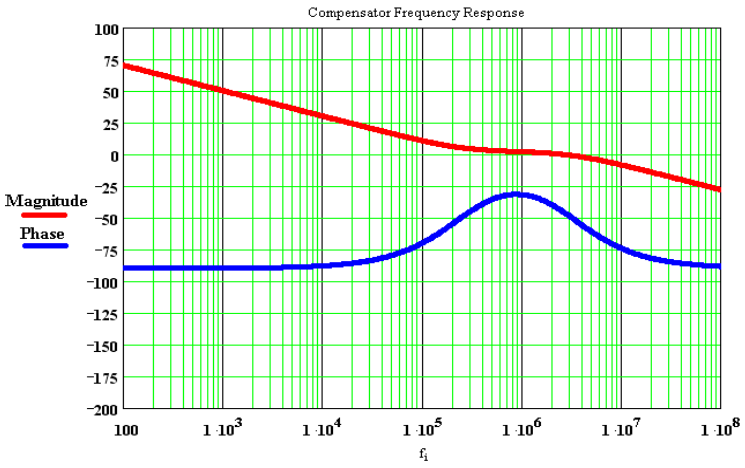


Figure 4.10 The bode plot of the compensator

The bode plot of the total open loop gain $T(s)_{OL}$ and the closed loop transfer function $T(s)_{CL}$ is shown in Fig. 4.11.

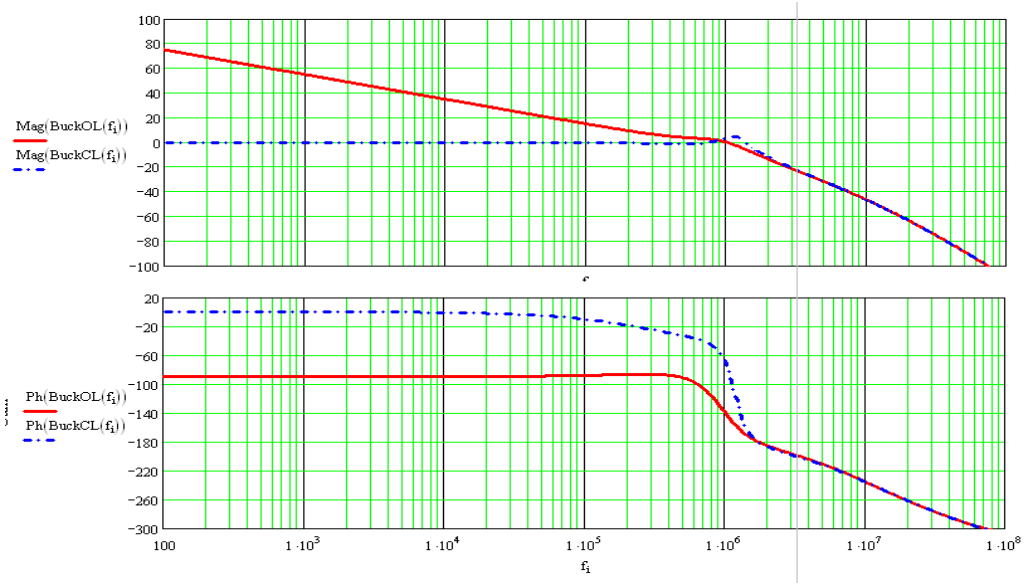


Figure 4.11 The bode plot of the open loop and close loop transfer function

As shown on the graph, the closed loop control bandwidth is around 1.5MHz, which is suitable to pass the EDGE envelope signal.

4.4 Ripple Cancellation Circuits Design

For envelope modulator used in EDGE polar modulation, one important specification is that the output voltage spectrum should meet the stringent EDGE standard, and the output voltage ripple appears as the undesired noise and deteriorate the modulator performance in frequency domain, for buck converter, the output ripple can be expressed as:

$$\Delta v_{OUT}(t) = i_C(t)R_C + \frac{1}{C}\int_0^t i_C(t)dt \qquad (4.16)$$

As we can see, it is the current flowing into the output capacitor and its ESR that generate the ripple voltage at the output, therefore if we can find a way to cancel out this current, the output voltage ripple will be greatly reduced and the spectrum performance will be increased accordingly. Ripple cancellation circuits shown in the Fig.4.12 is based on this principle [Sato'05].

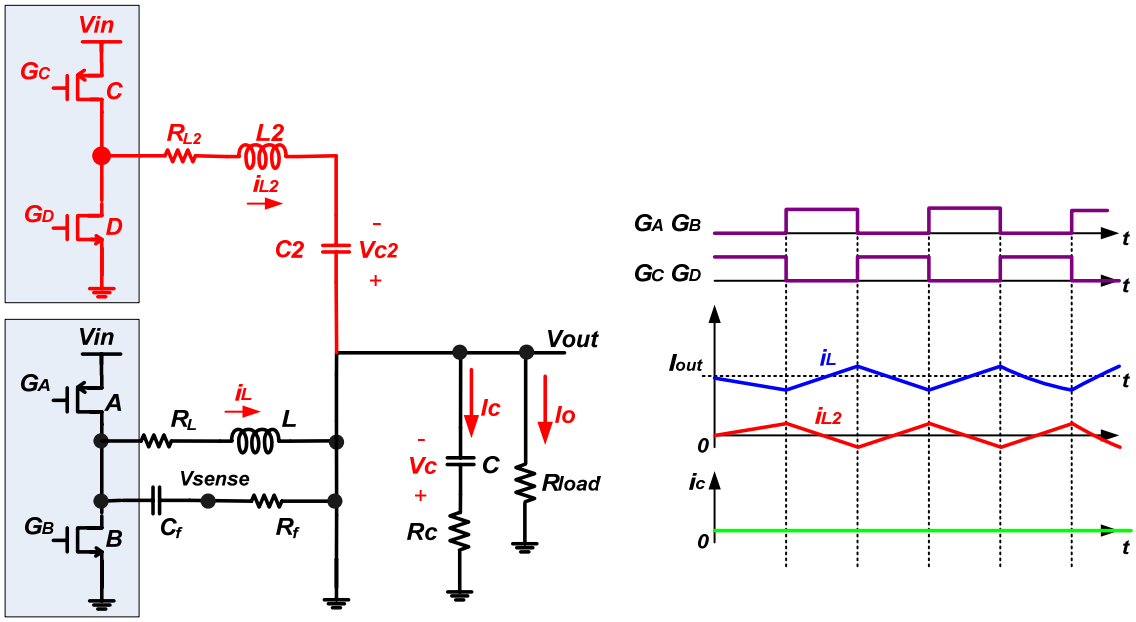


Figure 4.12 Ripple cancellation circuits and key waveforms

As indicated in Fig. 4.12, an auxiliary branch is added in parallel with the original buck converter, and the driving signals for auxiliary switches are anti-phase with the main switches. If we ignore the ESR of the inductor for the moment, by using the voltage-second balance on the inductors in both branches, we can get the following equation at steady state:

$$\begin{cases} V_C = DV_{IN} \\ V_{C2} = (1-2D)V_{IN} \end{cases} \qquad (4.17)$$

D is the duty cycle of the main switches. When switch *A* and switch *D* are on, the current following into the inductors can be expressed as:

$$\begin{cases} i_L = \dfrac{V_{IN} - V_C}{L} t + I_{L0} = \dfrac{1-D}{L} V_{IN} t + I_{L0} \\ i_{L2} = -\dfrac{V_{C2} + V_C}{L_2} t + I_{L20} = -\dfrac{1-D}{L_2} V_{IN} t + I_{L20} \end{cases} \qquad (4.18)$$

Where I_{L0} and I_{L20} are the initial values of the inductor current i_L and i_{L2}, respectively. From the equation (4.18) we can see that if we choose *L2 = L*, we can easy get that the current following into the output capacitance is

$$i_C = i_L + i_{L2} = I_{L0} + I_{L20} \qquad (4.19)$$

So only the DC inductor current exists and the entire ripple current is following through L2 and the output voltage ripple is greatly reduced.

By using the same method described in [Sato'05-2], the transfer function from the control to the output become the fourth order system, after the compensation the closed loop gain is reduced to around 800kHz. Fig. 4.13 shows the simulation results of the output ripple voltage versus output voltage when ripple cancellation circuits are added, the maximum ripple voltage is 8mV, which is greatly reduced compare to the original buck converter as

around 100mV, the small existing ripple voltage comes from the driver mismatch and the effects of the inductor ESR.

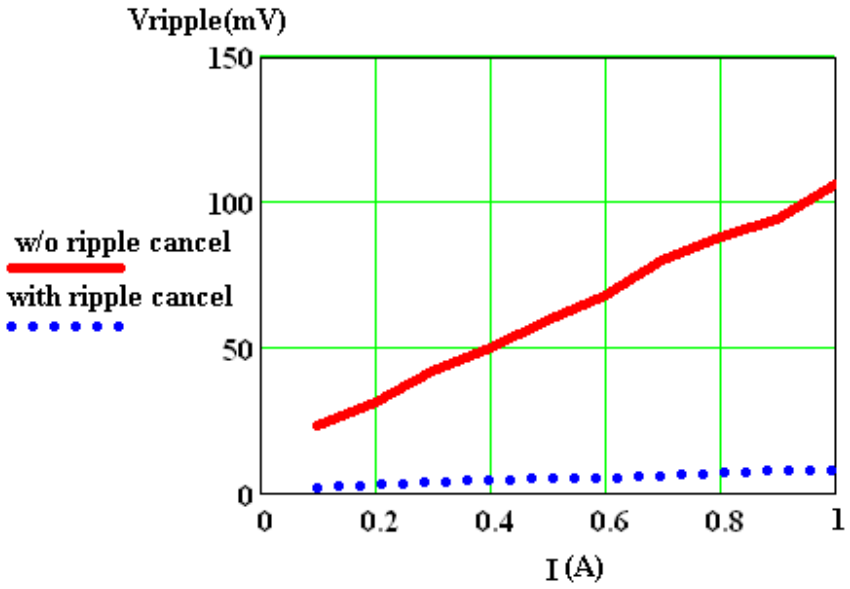


Figure 4.13 Buck converter ripple voltage versus load current

4.5 Losses Calculation and Efficiency Optimization

Theoretical estimation of power losses in the buck converter is crucial to estimate and optimize the efficiency performance, for the adaptive buck converter, the output voltage is changing with time, which means the instant power losses are also changing with time, therefore instant power losses should be integrated over the specified time frame to calculate the overall energy efficiency, and efficiency optimization is concentrated on how to reduce the total energy loss, which in turn prolongs the battery life time.

Power losses in the switching mode power supply are usually classified into two categories: switching losses and conduction losses. Switching losses are mainly caused by

charging and discharging the parasitic capacitances in the circuits, and the voltage-current overlap on the switching devices when changing their states. On the other hand, the conduction losses usually result from the current flow through the non-ideal power devices, filter elements and interconnect. Dead-time control circuits are usually adopted in synchronous converters in order to avoid shoot-through current, and the current will flow through the body diode of the switches during the dead-time, which will generate large conduction loss since the voltage drop on the diode is large (usually around 0.7V). Mathematical calculation of the loss components can be found in [Ericsson'01], for the designed adaptive buck converter with ripple cancellation circuits, the summary of the power losses are presented in Table 4.1.

Table 4.1 Summary of power losses in the adaptive buck converter

Mechanism	Expression
Resistor Loss for Two Main Switches	$\frac{R_{DSP}}{W_P}\cdot(I_L+\frac{\Delta I_L^2}{12})\cdot D+\frac{R_{DSN}}{W_N}\cdot(I_L+\frac{\Delta I_L^2}{12})\cdot(1-D-\frac{2t_{deadtime}}{T})$
Resistor Loss for Two Ripple Cancellation Switches	$\frac{R_{DSP}}{W_{P2}}\cdot\frac{\Delta I_L^2}{12}\cdot(1-D)+\frac{R_{DSN}}{W_{N2}}\cdot\frac{\Delta I_L^2}{12}\cdot(D-\frac{2t_{deadtime}}{T})$
Diode Conduction Loss	$(\frac{2t_{deadtime}}{T})I_{L(avg)}V_{DIODE}$
V-I Overlap for Top Switch Turn on and turn off	$0.5I_L(V_{IN}-V_{OUT})(t_{on}+t_{off})f_s$
Gate Charging Loss	$f\cdot C_{Parasitics}(W_P+W_N+W_{P2}+W_{N2})\cdot V_{IN}^2$
Inductor ESR Loss	$ESR_L\cdot(I_L^2+\frac{\Delta I_L^2}{12})+ESR_L\cdot\frac{\Delta I_L^2}{12}$
Capacitor ESR Loss	$ESR_C\cdot I_{RMSC}^2$
Other Loss	$I_{BIAS(TOTAL)}V_{IN}$

Various notations used in the table are as follows: $t_{deadtime}$ stands for the dead time, t_{on} and t_{off} stands for the voltage-current overlapping time when top switch is turned on and turned off, respectively. V_{DIODE} is the diode voltage, R_{DSN} and R_{DSP} are the on-resistances for the NMOS and PMOS normalized to 1mm. $C_{Parastics}$ is the input capacitance per mini meter of the switch, W_N and W_P are the widths of the main NMOS and PMOS transistors, W_{N2} and W_{P2} are the widths of the ripple cancellation NMOS and PMOS transistors. I_L and ΔI_L are average and peak-to-peak ripple inductor current, respectively.

The power efficiency can be expressed as:

$$\eta = \frac{P_{OUT}}{\sum P_{LOSS} + P_{OUT}} = \frac{V_O^2 / R}{(V_O^2 / R) + \sum P_{LOSS}} \qquad (4.20)$$

From the expression we can see that the power efficiency is related to the output voltage, Fig. 4.14 shows the relationship between the power efficiency and the output voltage when input voltage of buck converter is 6.4V.

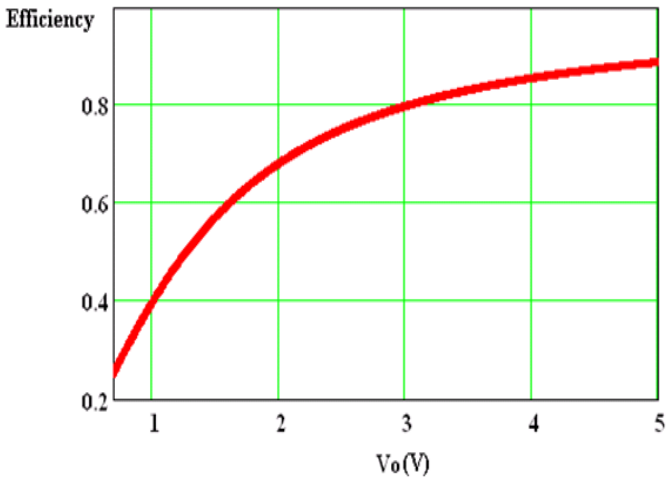
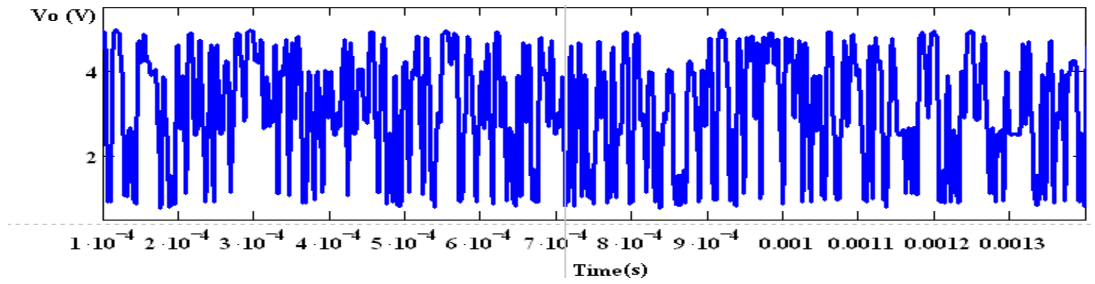
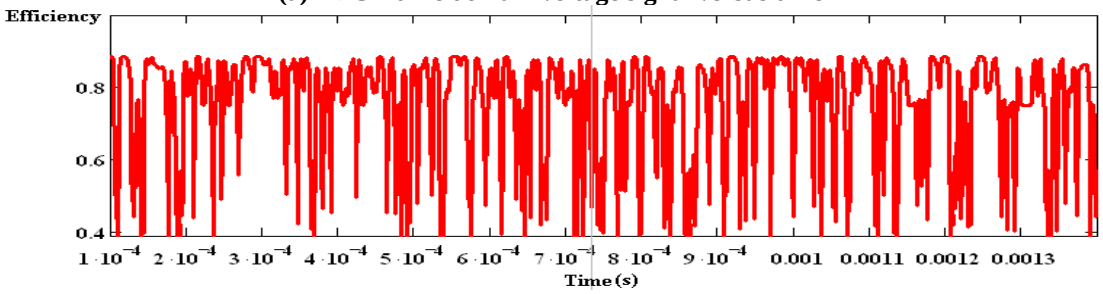


Figure 4.14 Power efficiency versus output voltage

Since the output voltage is changing as time goes by based on the EDGE standard, based on the relationship given in Fig. 4.14, the instant power efficiency will also change as the function of time. Fig. 4.15 shows the instant output voltage profile and the related instant efficiency with time, 1.4ms long time domain EDGE profile is used for simulation.



(a) EDGE time domain voltage signal versus time



(b) Instant power efficiency versus time

Figure 4.15 Simulation results of efficiency versus time

Eventually, it is the energy efficiency that determines the battery life time, so integration of the instant power efficiency is needed to find the energy efficiency, which can be expressed as follows:

$$Eff\,\% = \frac{\int_0^{\sigma} \frac{V_o(t)^2}{R_{LOAD}} dt}{\int_0^{\sigma} \frac{V_o(t)^2}{R_{LOAD}\eta(V_o(t))} dt} \qquad (4.21)$$

Where σ is the end time of the output EDGE profile, switch size can be optimized based on equation (4.21) to improve the efficiency. There are four switches in the buck converter, for the main branch, the width of the PMOS switch is chosen to be three times of the NMOS switch in order to get the same on-resistance. For the other two switches in the ripple cancellation branch, switch width can be smaller since they only deal with the ripple power.

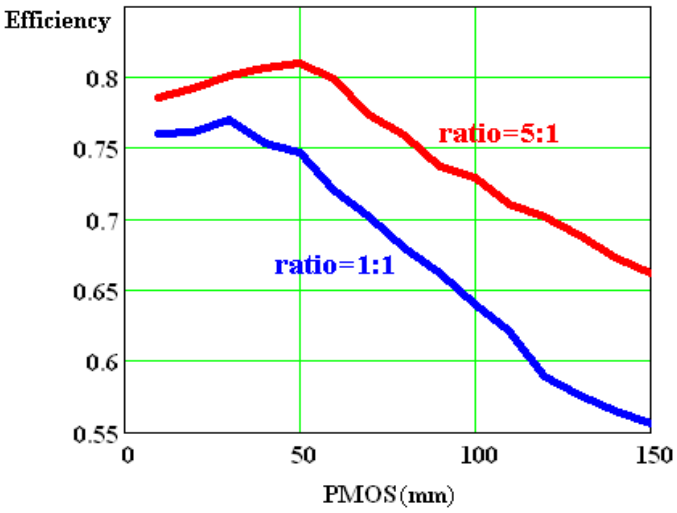


Figure 4.16 Energy efficiency versus main switch PMOS width

Fig. 4.16 shows the calculation results of the energy efficiency versus main switch PMOS width, two cases are compared, and one case is that the widths of the switches in ripple cancellation branch are chosen to be the same as the switches in main branch, for another case, main switches size are five times larger. As shown in the figure, reduce the size of the ripple cancellation switches will reduce the switching loss, with in turn increase the energy efficiency, the PMOS width of the main switch are chosen to be 50mm based on the calculation results and size ratio of 5:1 is chosen between main branch and ripple cancellation branch.

4.6 System Simulation Results and Summary

Table 4.2 summarized the design parameters of the adaptive buck converter, and the simulated energy efficiency is 76% when input voltage is 6.4V.

Table 4.2 Design Parameters of Buck converter

Input voltage range(Output of doubler)	V_{in}	5.2V – 8.2V
Output voltage range	V_{out}	1V – 5V
Switching frequency	f_{sw}	10MHz
Output capacitor	C	100nF
Output inductor	L	280nH
Load resistance	R	5Ω
Output filter resonant frequency	$\frac{1}{2\pi\sqrt{RC}}$	951kHz
Worst case loop gain cutoff frequency	f_c	428kHz
Worst case phase margin	degree	42
Worst case close loop control bandwidth		1.1MHz
Energy efficiency (Vin=6.4V)		76%

10MHz buck converter is connected to the output of the high efficiency voltage doubler to test the overall system performance, the time domain simulation results are shown in Fig. 4.16, the tracking signal at the output of the buck converter follows EDGE reference signal very well.

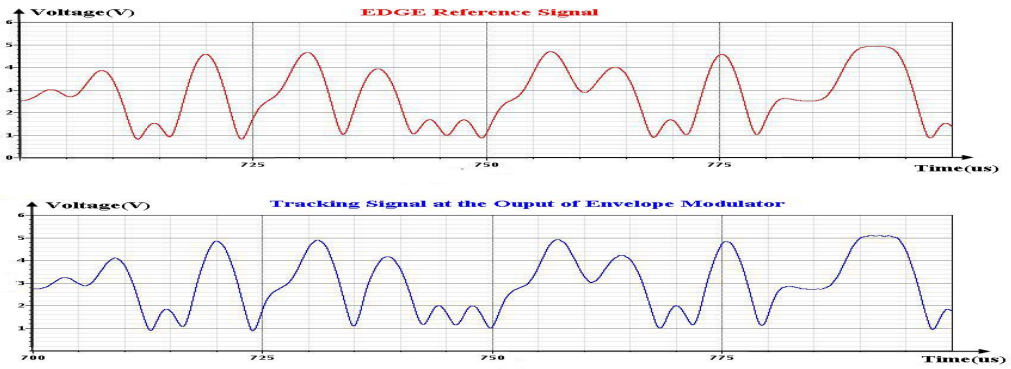


Figure 4.17 Time domain simulation results

For testing the spectral performance, the test bench is set up in MATLAB and the schematics are shown in Fig. 4.18.

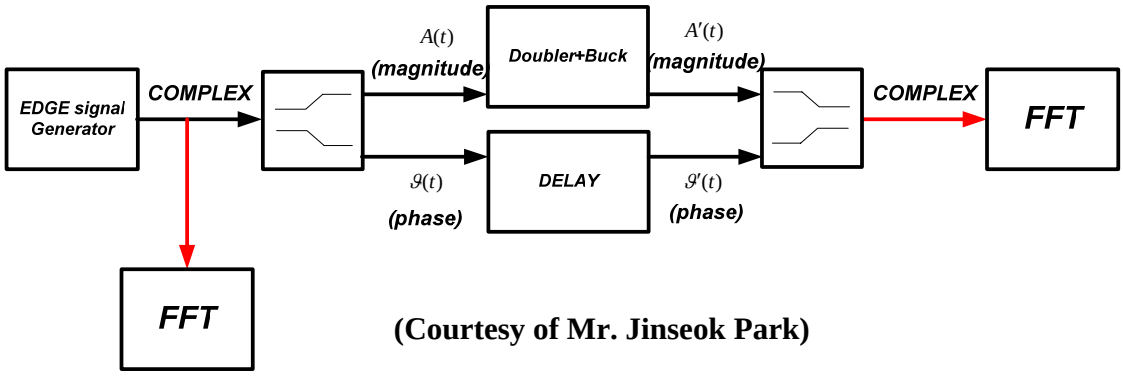
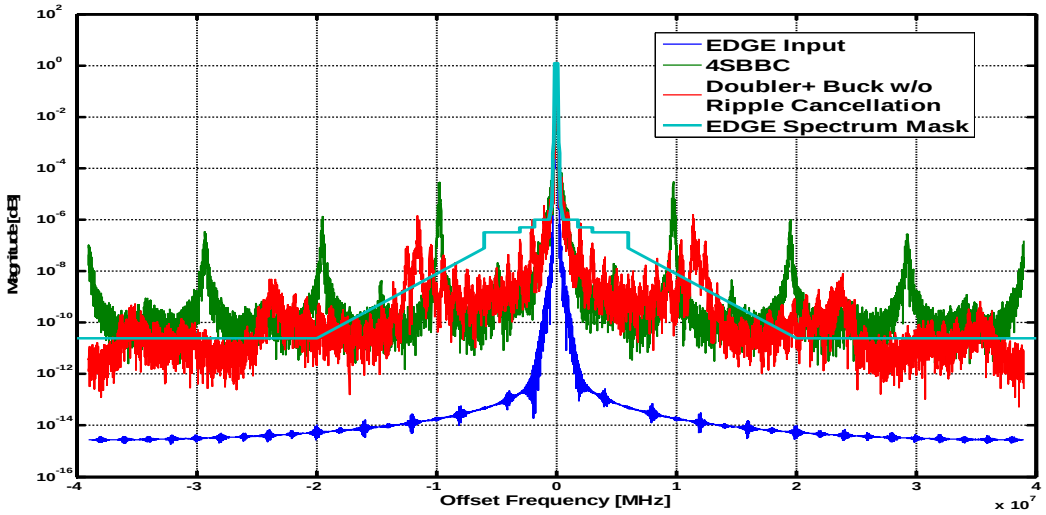


Figure 4.18 Test bench for simulating the spectral performance

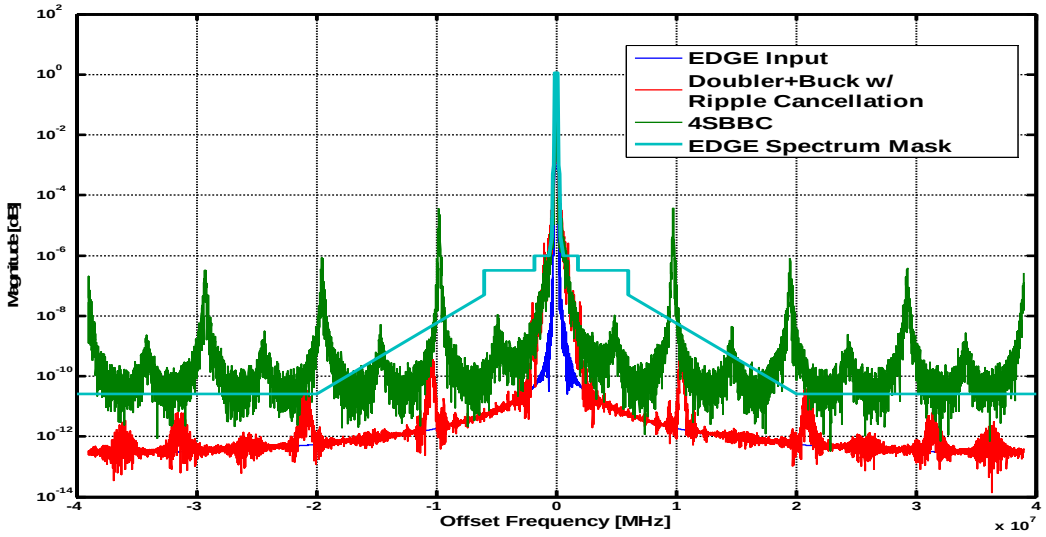
The EDGE signal generator generates the complex EDGE signal and split into magnitude and phase branch, the envelope of the complex signal *A(t)* goes through the designed doubler followed by buck envelope structure. The main causes of linearity degradation in polar modulation are the differential delay between envelope and phase branch [Reynaert'06], therefore, delay block should be inserted to the phase block to balance the delay in both branches. The delayed phase signal is then recombined with the output signal of the envelope modulator to drive the PA. Fast Fourier Transformation (FFT) is measured to test the spectrum performance.

Fig. 4.19 is the spectrum simulation results of the designed envelope modulator, Fig. 4.19(a) shows the spectrum performance by using doubler followed with buck converter and do not include the ripple cancellation circuits, at 10MHz fundamental switching frequency, the switching noise is reduced from 44.2dBc to 57dBc, i.e. 13dB noise reduction, but still does not satisfy the 80dBc requirement from the EDGE standard [3GPP'05]. When ripple

cancellation circuits is added, as shown in Fig. 4.19(b) this spurious components at 10MHz is reduced to 95.3dBc and meet the EDGE spectrum mask requirement, the noise performance is improved by 51dB compared to 4SBBC counterpart.



(a): Spectrum of voltage doubler + buck w/o ripple cancellation circuits



(b): Spectrum of voltage doubler + buck w/ ripple cancellation circuits
Figure 4.19 Spectrum simulation results of the proposed two stage structure

As discussed before, the delay mismatch between the envelope and the phase branch will cause the spectrum regrowth, so delay compensation should be added to the phase branch. Fig. 4.20 shows the spectrum regrowth effects caused by delay mismatch.

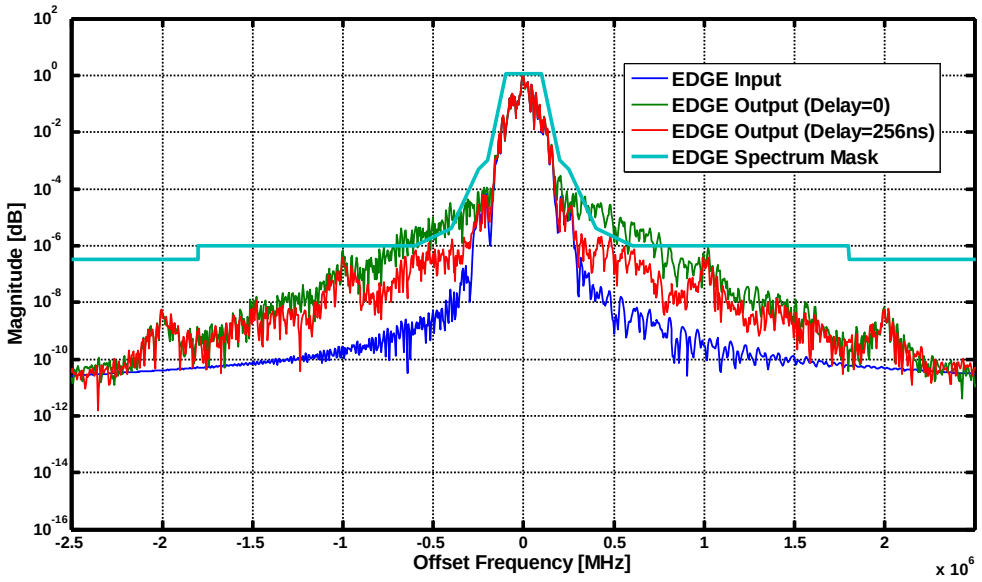


Figure 4.20 Effects of delay mismatch in spectral performance

The designed voltage doubler plus buck converter with ripple cancellation circuits structure is used for this simulation. The green line represents the output EDGE spectrum when no delay compensation is added in the phase branch, as we can see the spectrum does not meet the EDGE spectrum mask from 400 kHz to 600 kHz, and this frequency range is the most stringent requirement over all the frequency range. However, when 256ns delay is added to phase branch, the spectrum meet the EDGE standard. The spectrum peaks at 1MHz and its harmonics come from the voltage doubler, which are successfully suppressed by the following buck converter.

The performance comparison are summarized in Table 4.3

Table 4.3 Summary of spectral performance for different structures

Offset	EDGE Spectrum Requirement	4SBBC with 256ns Delay	Voltage Doubler + Buck		
			No Ripple Cancel	With Ripple Cancel	
			No Delay Compensation		256ns Delay
400kHz	< -54dBc	-55dBc	-48dBc	-50dBc	-58dBc
600kHz	< -60dBc	-62dBc	-52dBc	-55dBc	-63dBc
10MHz	< -80dBc	-44.2dBc	-57dBc	-95dBc	-95.1dBc

In this chapter, the design of the adaptive high frequency buck converter is discussed, which serves as the second stage of the proposed envelope modulator structure, ripple cancellation circuits are added in order to further reduce the ripple noise. Loss calculation and energy efficiency optimization procedure of the buck converter are proposed, which can be extended to any structures using dynamic power supply.

The text bench is built in MATLAB and the delay compensation is added to phase branch so as to cancel the mismatch effects. The CADENCE simulation results show that compared to the 4SBBC structure, the proposed envelope modulator structure has much better spectrum performance, which meets the EDGE spectrum requirement in all the frequency range, the spurious components at 10MHz switching frequency is reduced by 51dB, the proposed structure also has good energy efficiency as well.

The abovementioned mentioned voltage doubler followed by buck converter two stage schemes can be generalized and other schematics might be used, for example, instead of using switch capacitor voltage doubler, boost converter can also boost the voltage, buck converter can also be taken place by LDO. Different two stage solutions are compared in terms of efficiency, spectrum performance and complexity in the next chapter.

Chapter 5 Alternative Two Stage Solutions

As discussed in the preceding chapters, the input and output requirement of the EDGE envelope modulator makes it necessary to use two stage solutions. For the proposed structure, when the Li-ion battery is fully charged to 4.2V, the output voltage of the first stage voltage doubler will be around 8V, which will constrain its use in low voltage integrated circuits. There are several alternatives to the proposed topology with lower voltage ratings. Regulated charge pump and boost switch mode power supply can replace the voltage doubler at the first stage, on the other hand, instead of using buck converter as second stage, linear regulator can be used for the sake of its low noise characteristic.

In this chapter, apart from using switch capacitor voltage doubler as the first stage, regulated charge pump and boost converter structures are discussed and the advantages and disadvantages are compared when followed by the buck converter. For the second stage, linear regulator and buck converter structures are compared.

5.1 Regulated Voltage Doubler Followed by Buck Converter

The output of the voltage doubler can be regulated when it is larger than a specific voltage threshold for decreasing the voltage rating on the circuits. Lee's Pseudo-Continuous regulation method is based on the voltage doubler structure [Lee'07], three-stage switchable Opamp is required and the system becomes more complex when combined with buck converter. For simplicity, a hysterics comparator is used to compare the voltage doubler output voltage with a reference threshold voltage, when the output voltage is larger than the reference voltage, the comparator will generate a signal to shut down the clock. The output

voltage will be regulated in this way. The schematic of the regulated charge pump is shown in Fig. 5.1.

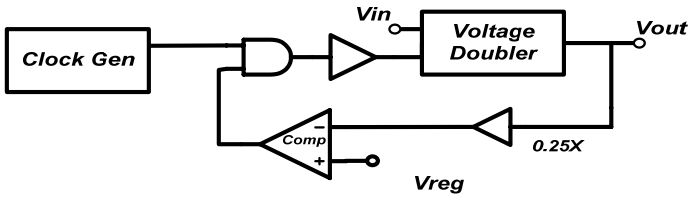


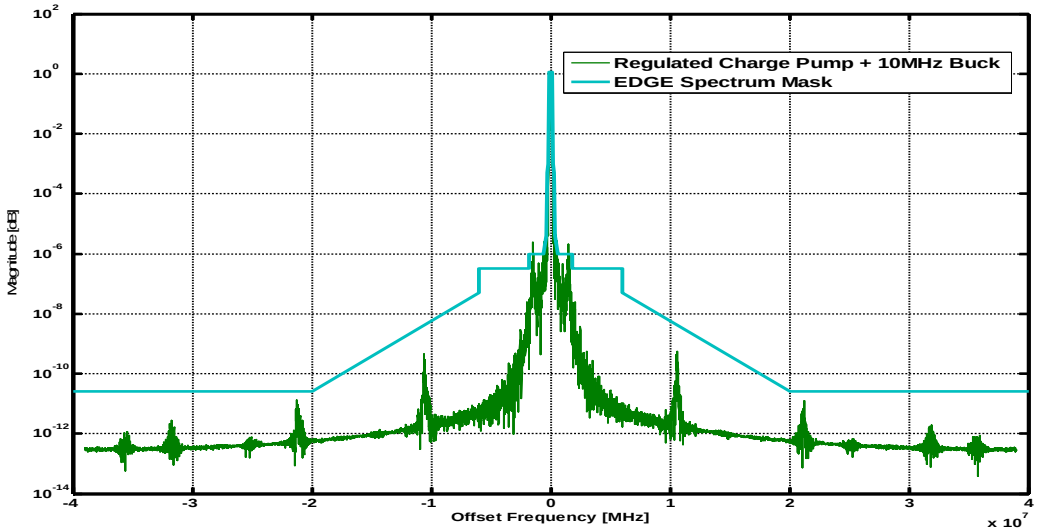
Figure 5.1 Schematic of the regulated charge pump

The output voltage ripple on the charge pump is related to the hysteric characteristics of the comparator as well as the load current, which is worse than the non-regulated voltage doubler. Fig.5.2 shows the spectrum simulation results and the spurious noise are mostly come from the low frequency range.

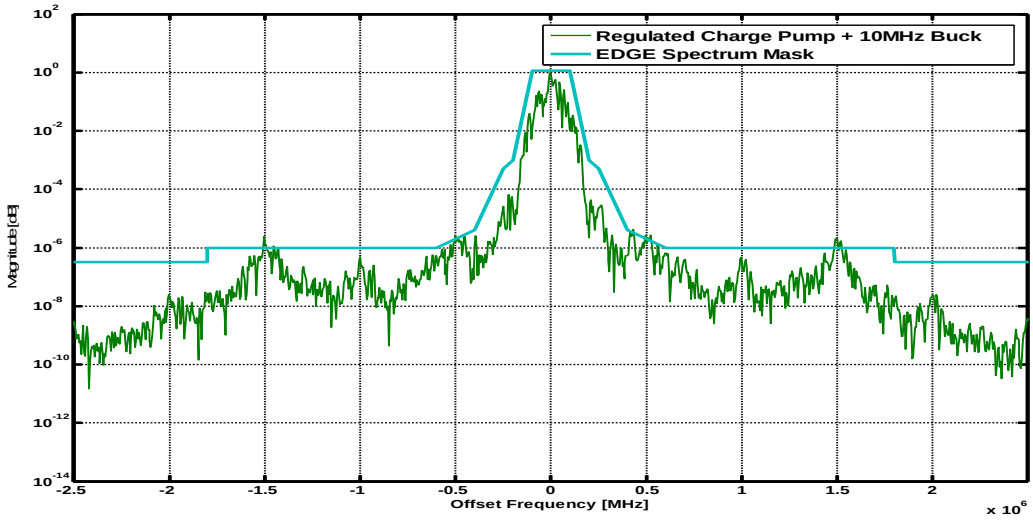
The drawback of the regulated structure comes from its low efficiency. For any charge pump circuits, the theoretical maximum efficiency is only related to the output and input voltage [Zhu'96] as:

$$\eta\% = \frac{V_{OUT}}{nV_{IN}} \qquad (5.1)$$

Here *n* is the number of the flying capacitors for each charge phase. So if regulated charge pump structure is used, efficiency will decrease when increase the input voltage. The average efficiency of the regulated charge pump linear regulator can be used to when input voltage is 4V and output voltage is regulated to 6.5V is only 75%, and the overall efficiency is only around 50% when combined with the buck stage.



(a) 40MHz Offset Frequency



(b) 250KHz Offset Frequency

Figure 5.2 Spectrum simulation results of regulated charge pump

5.2 Regulated Voltage Doubler Followed by Linear Regulator

Linear regulator can be used to replace the buck converter for the second stage, in that case, we can get rid of the spurious noise at fundamental switching frequency and its harmonics of buck converter, since linear regulator does not require the switching clock. The

structure of the linear regulator has been discussed in section 2.2, although it has good spectral performance, it also suffers from the low efficiency problem, the loss for the linear regulator is approximately the difference between the input and output voltage times the load current, since the input voltage is relatively high and the output voltage is the fast changing EDGE signal, the efficiency is quite low when the output voltage is low. When the voltage at the input of the linear regulator is regulated to 6.5V, the average efficiency is only 60%, and the overall system efficiency is 43% when combined with the regulated charge pump.

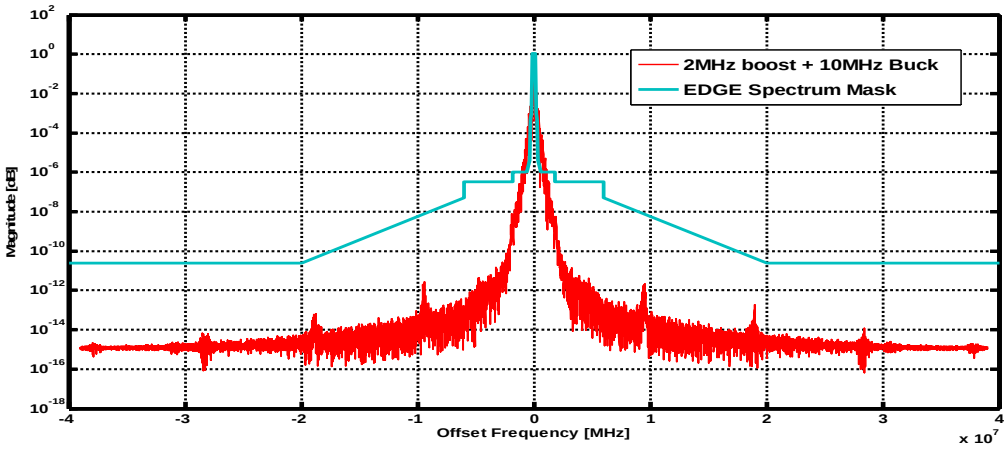
5.3 Boost Converter Followed by Buck Converter.

Boost switching mode power supply can step up the battery voltage and regulated to any desired value with high efficiency, so it may replace the charge pump in the first stage, the conventional voltage mode controlled 2MHz boost converter is designed, and the value of the inductor and the capacitor are chosen to be 1uH and 6.8uF, based on the trade-off of the output ripple voltage and the size of the passive components.

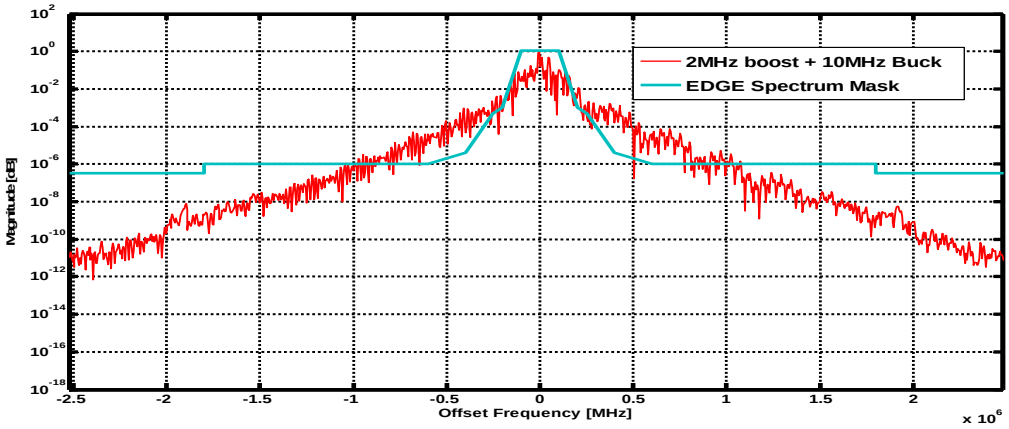
Combined with the original buck converter, the overall system spectrum simulation results and efficiency are tested when the boost converter steps up the battery voltage to 5.5V. The first stage boost converter can achieve 92% average efficiency and the overall efficiency is 65%, which is comparable to the proposed structure discussed in chapter 3. However, the problem for using boost converter lies in its poor spectrum performance. There exists a right-half-plane zero (RHZ) in the loop transfer function which makes the compensation more difficult to design and constrained the overall transient performance [Ericsson'01]. The location of the RHZ can be expressed as:

$$f_{RHZ} = \frac{(1-D)^2 V_{OUT}}{I_{LOAD} L} \qquad (5.2)$$

D stands for the duty cycle at the steady state. Under the worst case condition the boost converter should step up 2.7V battery voltage to 5.5V, and the load current under this condition is around 1A, which gives the RHZ located at around 200 kHz. As a rule of thumb, the crossover frequency should be chosen much less than RHZ frequency, which in turn gives poor transient performance.



(a) 40MHz Offset Frequency



(b) 250KHz Offset Frequency

Figure 5.3 Spectrum simulation results of boost followed by buck

As shown in Fig. 5.3, when connected with the adaptive buck converter, the boost switch mode power supply cannot handle the fast changing EDGE load condition, much spurious noise are generated in the low frequency range.

5.4 Structure Comparison

The summary of the different two stage solutions are listed in Table 5.1, the proposed voltage doubler followed by buck converter envelope modulator structure has best performance in terms of the efficiency and spectrum noise reduction, although the voltage rating might be high, it still a possible solution for EDGE polar modulation.

Table 5.1 Summary of various two stage solutions

Structure	**1st Stage**	Voltage Doubler	Regulated Charge Pump		Boost
	2nd Stage	Buck		Linear Regulator	Buck
Energy Efficiency		73%	50%	43%	65%
Spectrum Noise	**400kHz**	-58dBc	-55dBc	-56dBc	-30dBc
	600kHz	-63dBc	-60dBc	-62dBc	-42dBc
	10MHz	-95.1dBc	-92dBc	-100dBc	-110dBc
Complexity		Medium	Medium	Simple	Complex
Voltage Rating		8V	6.5V	6.5V	5.5V

Chapter 6 Summary and Future Work

6.1 Summary

The main contribution of this work is the proposed design methodology of an envelope modulator for EDGE polar modulation. The proposed structure has good spectra performance as well as high efficiency. The switching spurious noise is reduced by about 50dB compared to a 4SBBC structure [Jinseok'08] and the spectra meet the stringent EDGE specifications.

A two stage solution is proposed since the input and output voltages are both changing. The design of a high efficiency voltage doubler as the first stage is discussed and guidelines on how to select the design parameter are introduced.

Due to the high bandwidth requirement to pass the envelope EDGE signal, a 10MHz current mode control buck converter is proposed as the second stage. Ripple cancellation circuits are added to the converter for further reducing the spurious noise, greatly improving the spectra performance. A general approach to optimizing the overall energy efficiency to prolong the battery life time is also given.

Lastly, it is seen that the proposed scheme has the best efficiency and spectra performance in a comparison of two stage solutions, and might be a good candidate for EDGE polar modulation.

6.2 Limitations

There are several limitations in this research project and how to solve them are the future research directions. First of all, as discussed in chapter 5, the maximum voltage rating

of the proposed structure is about 8V, which may lead to the potential breakdown issue on the transistors. The mechanism is discussed as follows.

There exists a maximum allowed voltage across transistor terminals for any CMOS process, which is often limited by the device characteristics. The cross section of CMOS process is shown in Fig. 6.1. For reliable device operation, the maximum electric field across a device gate oxide should be limited, otherwise gate oxide breakdown will happen, resulting in resistive connections between the gate and the channel which is destructive to the transistor. This maximum allowed electric field determines the maximum gate-to-source (V_{GS}) and gate-to-drain (V_{GD}) voltage. Transistors with a thicker gate oxide offer higher voltage toleration, but the switching losses will increase due to larger gate capacitance.

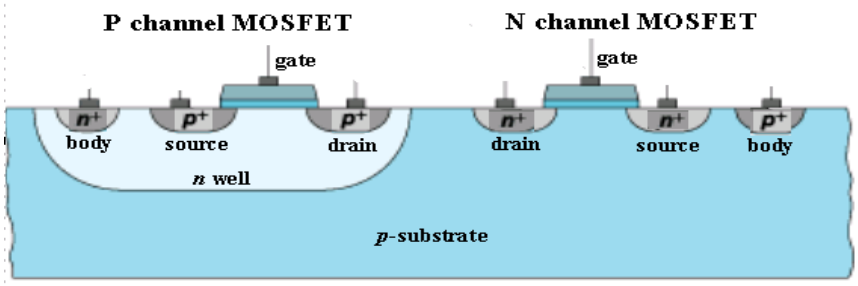


Figure 6.1 Cross section of CMOS process

For short channel device, increase the drain-to-source (V_{DS}) voltage will cause the drain touches the depletion region around the source. This phenomenon is called punch through and it will result in more gradual increase of the drain current. Punch through can be prevented by increasing the channel length of the transistors.

As shown in Fig. 6.1, there are parasitic p-n junctions between p-type substrate and n+-type source and drain, as the source-to-body (V_{SB}) and drain-to-body (V_{DB}) voltage increased, the electric field in the depletion region of the p-n junctions increases and the

mobile carriers are accelerated to higher velocities, which have sufficient kinetic energy that their collisions with the atoms in the lattice can excite electrons from the valence band to the conduction band (i.e. impact-ionization). Eventually, avalanche breakdown occurs when the impact ionization process attains an infinite rate. The breakdown voltage for the abrupt junction can be obtained by using the following formula [Baliga'96]:

$$BV = 5.34 \times 10^{13} N_A^{-3/4} \qquad (6.1)$$

Where N_A is the acceptor concentration on the homogeneously doped P region, since the substrate is relatively lightly doped, the voltage limit on drain and source diodes is often as three times large as the maximum tolerable voltage of the gate oxide [Hazucha'07], so the maximum tolerable voltage of a CMOS process is often limited by the maximum voltage across the gate oxide (i.e. V_{GS} and V_{GD}),

For the proposed two stage solution, the input of the envelope modulator is connected to Li-ion battery, which sets the input voltage range as between 2.7V to 4.2V, under a certain operation voltage range such as 4V, the boosted voltage at the output of the first stage voltage doubler will be 8V. We can recall the voltage doubler structure in Fig. 6.2.

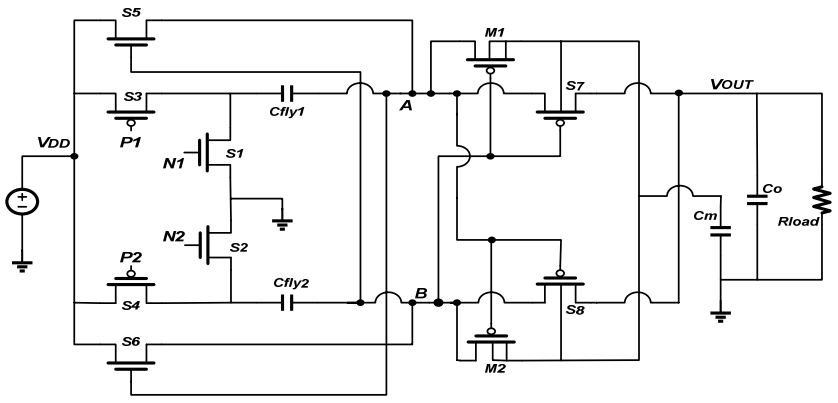


Figure 6.2 Voltage doubler structure

The maximum sustained V_{GS}, V_{GD}, V_{SB} and V_{DB} for each main transistor shown in Fig 6.2 are summarized in Table 6.1. Since cross-coupled structures are used in the first stage voltage doubler, the V_{GS} and V_{GD} for all the switching transistors will only see half of the output voltage, so there will be no voltage stress issue on the voltage doubler. However, the output of the voltage doubler is connected to the input and the gate driver of the buck converter, so the maximum gate oxide voltage will be the same as the output voltage of the doubler, constraining the usefulness of the proposed structure in low voltage processes. How to reduce the voltage stress on the transistors in second stage buck converter should be further investigated.

Table 6.1 Maximum voltage stress on each transistor of the voltage doubler

	Maximum Voltage			
Switch	**|VGS|**	**|VGD|**	**|VSB|**	**|VDB|**
S1	*VDD*	*VDD*	*0*	*VDD*
S2	*VDD*	*VDD*	*0*	*VDD*
S3	*VDD*	*VDD*	*VDD*	*VDD*
S4	*VDD*	*VDD*	*VDD*	*VDD*
S5	*VDD*	*VDD*	*VDD*	*VDD*
S6	*VDD*	*VDD*	*VDD*	*VDD*
S7	*VDD*	*VDD*	*VDD*	*0*
S8	*VDD*	*VDD*	*VDD*	*0*
M1	*VDD*	*VDD*	*VDD*	*0*
M2	*VDD*	*VDD*	*VDD*	*0*

Secondly, for the second stage buck converter, the switching losses are large under the 10MHz switching frequency, reducing the efficiency, especially in light load condition.

6.3 Future Work

Envelope modulator design for dynamic power supply of PAs is a quite attractive research topic nowadays and there are still many things to investigate in this area.

First of all, methods for reducing the voltage rating of the second stage buck converter are very worth investigating. One option to reduce the voltage stress across the gate oxide was proposed by Intel in 2007 [Hazucha'07], as shown in Fig. 6.3, by connecting two bridge transistors in series and by stacking the drivers, the high-side driver works between supplies V_{IN} and $V_{IN}/2$, and the low-side driver works between supplies $V_{IN}/2$ and ground, as a result, V_{GS} and V_{GD} of the main transistors are limited $V_{IN}/2$, and therefore allowing input voltage to be increased to twice the maximum process voltage.

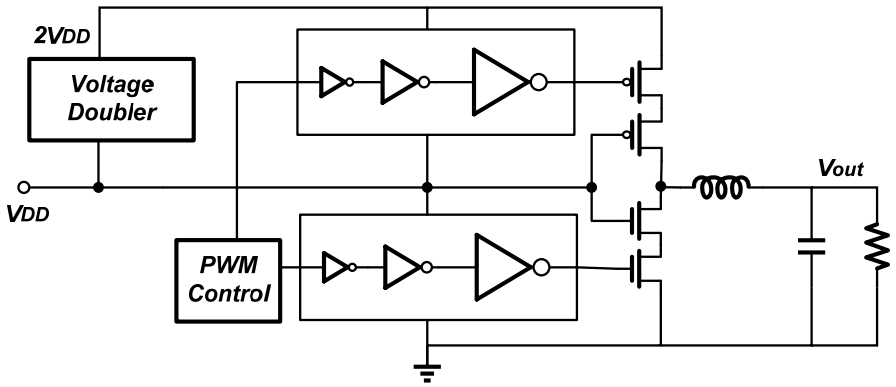


Figure 6.3 Reduce the buck converter voltage stress by using stacked transistors

Secondly, a switching regulator has good efficiency while linear regulator has low noise and easier to design. It might be possible to combine the features of both linear and switching regulators to increase both spectral performance and efficiency, as indicated in [Midya'00] and [Kwak'07].

Last but not the least, apart from current mode control, other control methods can be used in order to increase the efficiency of the buck converter, especially in light load condition. Pulse Frequency Control (PFM), which has been successfully used in [Sahu'04], maybe suitable for this application and could be worth investigating.

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