ABSTRACT

CASTRO, SUSANA PATRICIA. Characterization of the Boron Doping Process Using Boron Nitride Solid Source Diffusion

The purpose of this research has been to develop an optimum process for the boron doping of implants and polysilicon gates of metal-oxide-semiconductor (MOS) devices. An experimental design was constructed to determine the effects of diffusion temperature, time, and ambient on characteristics of the doping process. A temperature range of 800 to 1000 degrees Celsius was studied with a diffusion time between 10 and 60 minutes. Two diffusion ambients were used for doping processes, a pure nitrogen ambient and a nitrogen-oxygen gaseous mixture. Device wafers were fabricated, and the testing of MOS capacitors and van der Pauw test structures was performed to determine the effect of diffusion conditions on flatband voltage and poly gate doping. Materials characterization techniques were used on monitor wafers for each diffusion process to determine the wafer structure formed for each process and evaluate the effectiveness of the deglaze etch. The processes that resulted in the best device characteristics without suffering from significant poly depletion effects and flatband voltage shifts were wafers doped at 800 degrees Celsius in a pure nitrogen atmosphere for 20 minutes and 45 minutes. The presence of oxygen in the atmosphere caused the depletion of boron from the Si wafer surface. The formation of the Si-B phase only occurred on devices processed at 1000 degrees Celsius. The deglaze process used in this experiment did not fully remove this layer, and thus all devices doped at this temperature were seriously degraded.

CHARACTERIZATION OF THE BORON DOPING PROCESS USING BORON NITRIDE SOLID SOURCE DIFFUSION

by

SUSANA PATRICIA CASTRO

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APPROVED BY:

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Chair of Advisory Committee

PERSONAL BIOGRAPHY

SUSANA P. CASTRO

Susana P. Castro was born in the capital city of Honduras, Tegucigalpa. Because of her father's occupation at the United States Agency for International Development (USAID), she lived her childhood and adolescent years in several countries, including the United States of America, the Dominican Republic, and Guatemala. She spent more than half of her life in northern Virginia, where she completed her high school education. She graduated from Virginia Polytechnic Institute and State University in May of 1997 with a B.S. in Materials Science and Engineering. Her most treasured experiences in the field of engineering took place throughout her undergraduate education during her summer internships. Her internship in the summer of 1996 with the Research Experience for Undergraduates (REU) Program at North Carolina State University, sponsored by the National Science Foundation (NSF) Engineering Research Center (ERC) for Advanced Electronic Materials Processing (AEMP), introduced her to the field of microelectronics. Her internship in Chicago, Illinois, the following summer with the Center for the Advancement of Hispanics in Science and Engineering Education (CAHSEE) gave her the opportunity to teach a college-level engineering course to a group of young talented Hispanic high school students. Here, she gained a tremendous respect for the teaching profession. Her wonderful experience at the REU program in 1996 encouraged her to pursue her Master of Science Degree in Materials Science and Engineering, with an emphasis in the microelectronics field, at North Carolina State University.

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CHAPTER I

Introduction

1.1 Methods of Doping for P-Type Implants

The introduction of dopants into a substrate for the purpose of fabricating microelectronic device implants has long been performed by diffusion. Although the future trend for smaller size devices calls for a greater control of critical dimensions that is more easily achieved through ion implantation, diffusion remains to be a widely used method of doping. A large thermal budget for diffusion processes is a disadvantage, but the ability to process wafer lots at a time with this doping method is one of the reasons for its wide continued use. In addition, the degenerate doping of polysilicon gates for metal-oxide-semiconductor (MOS) devices is easily achieved through diffusion. In the Microelectronics Laboratory at North Carolina State University (NCSU), boron and phosphorus diffusion furnaces are used by many students for the formation of p- and n-type implants and for the degenerate doping of poly gates on device wafers.

Of all group IV elements in the periodic table, boron has been the most widely used element for the purpose of doping silicon p-type. Boron can be introduced into the silicon substrate by deposited films or by exposure to a vapor containing the dopant source. Diffusion processes carried out in furnace tubes are very reproducible, resulting in excellent across the wafer and wafer-to-wafer uniformity. The work of this thesis focuses on the use of boron nitride planar diffusion sources as

the dopant source for boron diffusion in silicon. This boron diffusion system will be described in detail in the next chapter.

1.2 The Issue of Silicon-Boron Phase Formation

The quality of diffusion processes carried out in furnace tube systems are affected by a number of factors, including gas flow, temperature, time of diffusion, ambient, substrate material, and dopant source. Literature on boron diffusion systems shows the formation of a silicon-boron phase during diffusion at the silicon substrate and borosilicate glass (BSG) interface. This phase is believed to form in situations of high boron concentrations at the silicon surface. Regardless of the expected formation of the Si-B phase outlined in various published works, results from previous boron diffusion runs at the NCSU Microelectronics Laboratory using the boron nitride planar diffusion source system show no evidence of this phase. This unexpected result has motivated the need for an overall characterization of the BN solid source diffusion system.

The Si-B phase has been reported to consist of the SiB_4 or SiB_6 compounds depending on diffusion conditions. Ellipsometric studies of the material indicate the compound has an index of refraction between 1.6 and 1.7. It is insoluble in hydrofluoric acidic solutions generally used in the deglaze process, which is the reason for the required oxidation step in the deglaze. Oxidizing the processed wafer after an initial HF etch will allow the Si-B phase to react with oxygen and form a boron-silicon oxide, also known as borosilicate glass. The BSG formed can then be

removed with a final HF etch, removing all undesired diffusion byproducts from the Si surface by the end of the deglaze process.

The presence of the phase can visibly be detected by the presence of a hydrophilic silicon surface after an HF etch and/or a brownish yellow silicon surface. A previous in-depth study on the growth of the Si-B phase showed that the formation of this phase, depending on the dopant source used, decreases with the oxygen content in the diffusion ambient at low diffusion temperatures. The oxygen is believed to increase the growth rate of SiO_2 on the Si wafer during diffusion, thereby reducing the chances of accumulating a high boron concentration at the Si-SiO_2 (or Si-BSG) interface.

1.3 Outline of Thesis Work

The goal of this work was to determine an optimum process for the doping of poly gates and device implants. In order to achieve this goal, an overall characterization of the doping process is needed, including the determination of poly gate doping and any defects induced by the boron diffusion process which have an effect on device electrical characteristics. The quality of the diffusion process may also be affected by the formation of the Si-B phase, so efforts to determine the conditions that form this phase is be made. The factors under study in this thesis include the effects of diffusion temperature, time, and ambient on the diffusion of boron in silicon. These goals were achieved by designing an experiment that would explore various levels of these three parameters. A blank wafer for each diffusion condition in the experiment would be processed and later used for materials

characterization purposes. Device wafers were also fabricated at each diffusion condition using the four-level ECE 539 class mask set for the spring of 1998. The electrical testing of capacitors and test structures fabricated with this mask set would allow the extraction of parameters of interest such as sheet resistance, poly doping level, and flatband voltage.

In Chapter II of this thesis, the boron nitride solid source diffusion system under evaluation in this experiment will be described. Chapter III will explain the experimental procedure followed along with the characterization methods used to achieve the experimental objectives. Results from these methods will be discussed in Chapter IV, and a summary of the results and conclusions obtained will be given in Chapter V.

CHAPTER II

Boron Nitride Planar Diffusion Source System

2.1 Boron Nitride Solid Source Diffusion Process

In a horizontal furnace, boron nitride planar diffusion source wafers and silicon wafers are loaded perpendicular to the furnace tube axis onto a silica boat as shown in the diagram below. Silicon wafers are placed adjacent to source wafers so that only the front surface (device side) of the wafer is doped. During diffusion, a gas flow, usually consisting of an inert gas such as nitrogen, is used to prevent the entering of air contaminants into the tube. The flow of gas also creates a boundary layer around the wafers, allowing the dopant vapor to be transported from the source wafer to the silicon wafer by concentration gradient diffusion. Although nitrogen is typically used for this purpose, gaseous mixtures of nitrogen, oxygen, and hydrogen have also been used.

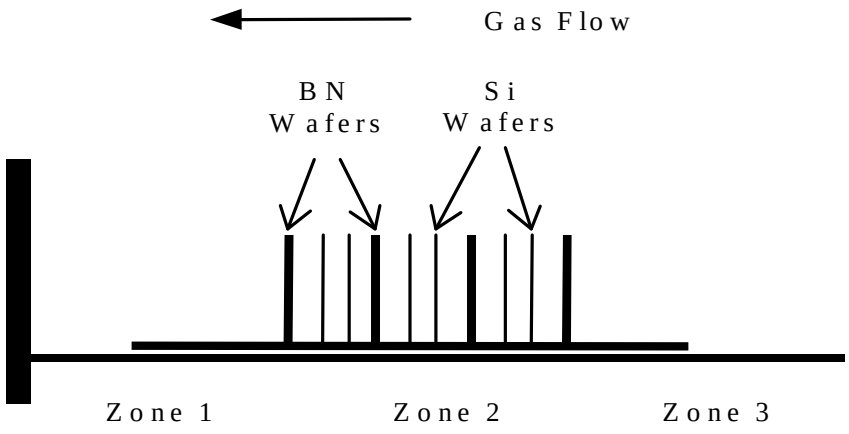

Figure 2.1 – Wafer arrangement in furnace for boron nitride solid source diffusion

Table 2.1 – Boron nitride planar diffusion source activation procedure

Step	Gas Flow	Temperature	Time
Ramp Up	N_2, 4 slpm	storage temp → 925°C	35 min.
Oxidation	O_2, 4 slpm	925°C	20 min.
Anneal	N_2, 4 slpm	925°C	20 min.
Ramp Down	N_2, 4 slpm	925°C → storage or boat-out temp	45 min.

The boron nitride source wafers used for this experiment were of a BN-975 grade designed by the Carborundum Corporation for use at temperatures between 800° and 1000°C. The source wafers are composed of boron nitride platelets held together by a B_2O_3 binder. New boron nitride wafers undergo an activation procedure as described in Table 2.1. The oxidation step forms a thin layer of B_2O_3 glass on the surface of the source wafer by the chemical reaction below:

$$4BN + 3O_2 \rightarrow 2B_2O_3 + 2N_2 \qquad \textit{Eq. 2.1}$$

The purpose for the anneal step is to stop the oxidation reaction above and stabilize the rate of dopant volatilization. When not in use, the boron nitride source wafers are stored in the furnace at 400°C with a N_2 flow rate of 1500 sccm.

The general steps followed for a boron diffusion run are outlined in Table 2.2. Note that the diffusion ambient gases, temperatures, and times are varied in the experimental work for this thesis. The information given for these variables in the table is the standard used at the Microelectronics Laboratory. During the diffusion step, the B_2O_3 layer previously formed on the BN wafer during activation vaporizes

Table 2.2 – General boron diffusion procedure

Step	Gas Flow	Temperature	Time
Boat In	N_2, 4 slpm	750°C	10 min.
Stabilize	N_2, 4 slpm	750°C	5 min.
Ramp Up	N_2, 4 slpm	750°C → 900°C	25 min.
Diffusion	N_2, 4 slpm	900°C	30 min.
Ramp Down	N_2, 4 slpm	900°C → 750°C	45 min.
Boat Out	N_2, 4 slpm	750°C	10 min.

and is transferred to the adjacent silicon wafer. A layer of B_2O_3 then forms on the Si wafer surface and acts as the boron dopant source during diffusion. The following interface reaction occurs:

$$2B_2O_3 + 3Si \Leftrightarrow 4B + 3SiO_2 \qquad \textit{Eq. 2.2}$$

Depending on diffusion conditions, the following reactions may also occur:

$$Si + B \Leftrightarrow Si\text{-}B \text{ phase} \qquad \textit{Eq. 2.3}$$

$$Si\text{-}B \text{ phase} + O_2 \Leftrightarrow B\text{-}Si\text{-}O \text{ glass} \qquad \textit{Eq. 2.4}$$

$$Si + O_2 \Leftrightarrow SiO_2 \qquad \textit{Eq. 2.5}$$

Figure 2.2 is a schematic of the structure that is expected to form during diffusion. The Si-B phase may or may not be present depending on diffusion conditions.

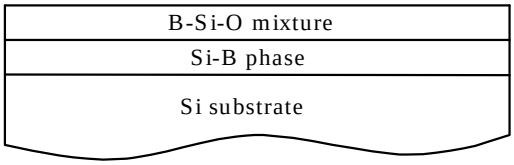

Figure 2.2 – Schematic of structure formed on Si wafer during boron diffusion

2.2 Deglaze Process

The deglaze is the process followed for the removal of diffusion byproducts. The standard deglaze process used at the Microelectronics Laboratory is shown in Table 2.3. Steps 1 and 3 involve the immersion of processed wafers in a hydrofluoric acid solution for the etching of BSG. For the wafers processed in this thesis study, a 15:1 H_2O:HF solution was used for this purpose. Solutions of varying HF concentrations, and even buffered oxide etch (BOE) solutions, have been used in the past for deglaze. At Carborundum, a 10:1 HF solution is used for the BSG etch step. A more dilute solution was used in this experiment to obtain a slower etch rate and prevent the etching of field and gate oxides on device wafers.

Table 2.3 – Standard deglaze process

Step 1	15:1 H_2O:HF etch for 30 seconds at room temperature
Step 2	Chemical oxidation in 90°C HNO_3 solution for 30 minutes
Step 3	15:1 H_2O:HF etch for 30 seconds at room temperature

Step 2 of the deglaze process involves the immersion of wafers in a hot nitric acid solution. Nitric acid, a very strong oxidizing agent, is brought to a temperature of 90°C (slightly above its boiling point) using a hot plate. This nitric acid step acts as a form of oxidation and is needed to oxidize the Si-B layer that may have formed during diffusion. The Si-B layer reacts with oxygen, producing a boron silicon glass mixture (BSG), which can then be etched away by the HF solution used in step 3 of the deglaze.

The use of nitric acid for the oxidation of the Si-B layer has been used effectively in the past. However, a low-temperature thermal oxidation is the preferred method of oxidizing this layer and is used at Carborundum. The disadvantages to a thermal oxidation process include a further drive-in of the junction and a possible depletion of boron dopants at the silicon surface. This boron depletion can occur because boron has an affinity to oxide, which results in an accumulation of boron in the oxide and therefore a depletion of boron in the silicon substrate at the Si-SiO_2 interface. However, this boron depletion effect may not be significant at low temperatures. The results of the experimental work for this thesis will help evaluate the effectiveness of the Microelectronics Laboratory standard deglaze process for the boron nitride solid source diffusion system.

CHAPTER III

Experimental Approach

3.1 Experimental Design

The main approach used to achieve the experimental objectives in this thesis was to examine the effects of the diffusion conditions explored in this experiment on the formation of the silicon-boron phase and on device characteristics. The results of this study will allow the determination of an optimum process for the doping of poly gates and implants. The variables in the experiment include diffusion ambient, temperature, and time. Points were chosen in a modified central composite design as shown below to achieve the experimental goals with the least number of wafers.

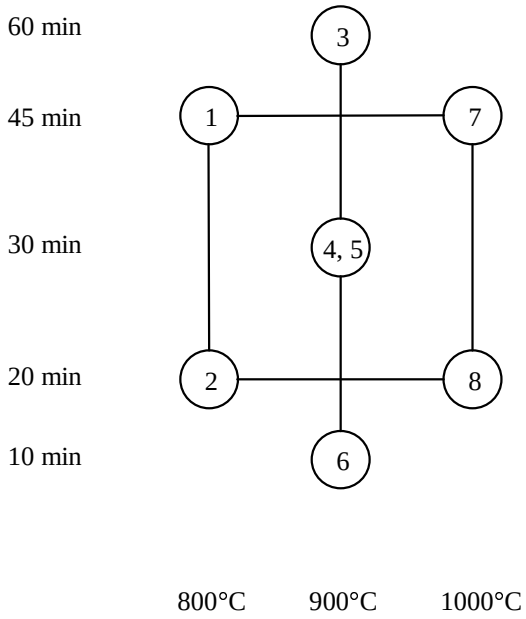

Figure 3.1 – Schematic of the chosen experimental points in the design

The experimental design shown in Figure 2.1 determined the diffusion temperatures and times that would be carried out in the experiment. The temperature range explored was 800°C to 1000°C, since the BN-975 grade planar diffusion sources used in the experiment were designed for use in this range. Times of diffusion up to 60 minutes were used, since a diffusion time of greater than one hour would require too high of a thermal budget for practical use. This design for temperature and time was carried out for two different diffusion ambients: 1) a pure nitrogen atmosphere and 2) a nitrogen-oxygen gaseous mixture. Note that although only 7 points were explored in each ambient, the center point of the design was repeated to address the issue of repeatability, resulting in 8 different diffusion temperatures and times per ambient. The complete experimental design resulted in a total of 16 diffusion runs.

In order to prevent the over-oxidation of the boron nitride solid source wafers, the diffusion runs carried out in a nitrogen-oxygen gas ambient were broken down into two steps. For the first half of the diffusion time, the doping process was performed in a N_2O_2 environment. The second half of the diffusion time was carried out in a pure nitrogen ambient. During diffusion processes, a presence of oxygen in the atmosphere will oxidize the BN wafers as discussed in Chapter II. As in the activation procedure followed for new BN wafers, an anneal in nitrogen is needed to stop the oxidation process and stabilize the rate of dopant volatilization. For this reason, a diffusion run in an oxidizing atmosphere should be followed by an anneal in nitrogen at the diffusion run temperature. In order to preserve the structure for our design of experiments, the diffusion runs in an oxidizing atmosphere were broken

down into the two step N_2O_2/N_2 process, within the diffusion time originally designated.

For each of the 16 diffusion conditions in the experiment, one wafer would undergo an entire device fabrication sequence. Devices would be fabricated on only half of this wafer while the other half would be left blank for the purpose of obtaining four-point probe measurements. The testing of capacitors and test structures would allow the extraction of important electrical characteristics. An additional blank wafer (monitor wafer) for each diffusion run would be processed that would be used for materials characterization purposes such as transmission electron microscopy (TEM) and spreading resistance analysis (SRA). Note that two wafers were processed for each of the 16 diffusion runs – one monitor wafer and one device wafer.

3.2 Wafer Processing

Devices were fabricated using the ECE 539 class mask set for the spring of 1998. The device fabrication process for this mask set is a four mask level process: active, poly, contact, and metal. A detailed description of the process sequence is given in Appendix A. Table 3.1 is a general outline of the major steps in the device process flow. As explained in the previous section, devices were fabricated on only half of the wafer so that four-point probe measurements could be obtained from the blank half of the wafer.

Table 3.1 – Outline of process sequence

Step 1	Initial clean (JT Baker)
Step 2	Field oxide growth
Step 3	Active mask photolithography and field oxide etch
Step 4	Pre-gate clean, gate oxide growth, and polysilicon deposition
Step 5	Poly mask photolithography, polysilicon etch, and gate oxide etch
Step 6	Implant and poly gate doping with BN solid source and deglaze
Step 7	Low temperature oxide deposition
Step 8	Contact mask photolithography and oxide etch
Step 9	Front-side metal deposition
Step 10	Metal mask photolithography and metal etch
Step 11	Back-side metal deposition and forming gas anneal

Blank wafers used for materials characterization techniques went through a BN solid source diffusion run using the standard process explained in Chapter II. One monitor wafer was used for each diffusion run. Table 3.2 is a list of all 16 diffusion runs performed in this experiment. These blank wafers were cleaved in half, and a modified deglaze etch was performed on one half of the wafer. This modified deglaze simply included a 1 second dip in water followed by a 30 second etch in a 15:1 HF solution. This modified deglaze would be compared to the standard deglaze by means of four-point probe and optical measurements as will be discussed in the following sections. The dip in water was done for the purpose of removing B_2O_3

Table 3.2 – List of 16 diffusion runs performed in experiment

Wafer Identification	Temperature	Time	Ambient
A1	800°C	45 min.	N_2
A2	800°C	20 min./25min.	N_2O_2/N_2
A3	800°C	20 min.	N_2
A4	800°C	10 min./10 min.	N_2O_2/N_2
B1	900°C	60 min.	N_2
B2	900°C	30 min./30 min.	N_2O_2/N_2
B3	900°C	30 min.	N_2
B4	900°C	15 min./15 min.	N_2O_2/N_2
B5	900°C	30 min.	N_2
B6	900°C	15 min./15 min.	N_2O_2/N_2
B7	900°C	10 min.	N_2
B8	900°C	5 min./5 min.	N_2O_2/N_2
C1	1000°C	45 min.	N_2
C2	1000°C	20 min./25min.	N_2O_2/N_2
C3	1000°C	20 min.	N_2
C4	1000°C	10 min./10 min.	N_2O_2/N_2

Note: The diffusion runs were not necessarily performed in this order. Runs were completed in a random fashion to reduce experimental biases. The Wafer Identification column gives the labels scribed onto the wafer backside prior to wafer processing. These wafer labels may be referred to in the following sections of this thesis. Remember that two wafers were processed at each diffusion condition, one monitor wafer and one device wafer.

from the wafer surface before obtaining optical measurements of the BSG layer. After diffusion, a hazy surface appeared on processed wafers which was caused by the hydration of unreacted B_2O_3 on the Si wafer surface. The removal of this hazy layer, which could be achieved by dipping the wafers in water, was needed to obtain accurate optical measurements.

In the following sections, a brief description of the materials and electrical characterization methods used in this experiment to obtain the desired data is given. Testing procedures and conditions are given for each method.

3.3 Characterization Methods Used on Monitor Wafers

The blank wafers processed for each diffusion run were cleaved in half, as previously explained. The half of the wafer that underwent the modified deglaze process was used mainly for sheet resistance and BSG film thickness measurements. The procedure and instruments used for these measurements will be described in detail in the following appropriate sections. The half of the wafer that did not go through a deglaze provided samples for transmission electron microscopy (TEM) work, spreading resistance analysis (SRA), and x-ray diffraction (XRD) analysis.

3.3.1 Transmission Electron Microscopy

TEM was used in this experiment to obtain an image of the structure formed on the silicon wafer by the BN solid source diffusion process. Low magnification images provided by TEM would be able to verify the BSG/Si-B/Si sample structure originally expected for doped Si samples by the BN system. The imaging

of an amorphous surface layer on the Si substrate would correspond to the BSG layer. At high magnifications, the lattice structure of the single crystal Si substrate could easily be imaged and any crystal defects at the Si surface caused by the doping process could be detected. The presence of the Si-B phase would be indicated by a crystalline layer sandwiched between the BSG film and the Si substrate.

Although the presence of the Si-B phase can be verified by a hydrophilic Si surface after the initial HF etch in the deglaze, methods of characterizing this layer have not been well established. An exact index of refraction is not known for the Si-B phase, and hence any optical methods used for measuring the thickness of this layer will not give accurate results. Therefore, TEM was the chosen method to extract Si-B layer thickness. In addition, because Carborundum has reported Si-B layer thicknesses of 100 Å or less, the high resolution attainable by TEM methods was essential in order to characterize the Si-B layer.

Since TEM is a very time consuming and expensive characterization technique, images were not obtained from all samples. The wafers processed in a N_2 ambient were chosen to determine a general relationship between the Si-B layer thickness and the diffusion temperature and time. From these wafers, the 3 that were doped at 900ºC (not including the 30 min. replicate run) were imaged. These 3 points would allow the determination of a general model for the relationship between Si-B phase formation and diffusion time. This model would enable the prediction of the Si-B layer thickness at any diffusion time. A temperature effect on the Si-B layer thickness could then be determined at a constant diffusion time.

A Si-B thickness for a wafer doped at 900ºC for 45 minutes could be extrapolated from the diffusion time model, and this thickness could then plotted with the thicknesses obtained from the two wafers doped for 45 minutes at 800ºC and 1000ºC. A general model of the effect of diffusion temperature on Si-B phase formation could then be determined.

To verify that the temperature and time models extracted from the N_2 data were consistent in a mixed nitrogen-oxygen ambient, several wafers that were processed in the N_2O_2 ambient were randomly chosen and imaged by TEM. The samples imaged will be given in Chapter IV along with a discussion of the results obtained from these images.

3.3.2 Optical Measurements

Optical measurements were performed on the half-wafer samples that underwent the modified deglaze process as previously described in Section 3.2. A Nanospec/AFT Nanometrics microscope was used for these measurements. This instrument scans across an incident light wavelength from 480 to 790 nm, which is reflected by the film, producing a pattern of interference fringes. The amplitude and frequency of the sinusoidal pattern depends on the substrate and film thickness being measured. A number of algorithms have been programmed for the measurement of certain film thicknesses with the Nanometrics. The program used to make all optical measurements on the half-wafer samples was an “oxide on Si” program for the measurement of SiO_2 film thickness on a Si substrate.

Measurements were made before and after the samples underwent the modified deglaze. It was assumed that the Nanometrics program used was sufficient for the measuring of BSG thicknesses using an index of refraction of 1.46. The optical properties of BSG are very similar to that of SiO_2 since this glass is simply an amorphous silicon oxide with a high boron content. The presence of boron will have a slight effect on the index of refraction of SiO_2, but the use of this algorithm for BSG thickness measurements will give reasonably good estimates. The measurements obtained from these measurements are compared to extracted BSG film thicknesses from TEM images in Chapter IV.

Optical measurements of each half-wafer sample were performed twice, once after the water dip and once after the HF etch. This was done to determine the effect of the initial HF dip on boron diffusion byproducts. A remaining film on the Si wafer after this initial HF etch would indicate the presence of the Si-B phase.

3.3.3 Four-Point Probe Measurements

Sheet resistance measurements were also done for the half-wafer samples that underwent the modified deglaze process using a four-point probe instrument. The assumption was made that by using a half-blank wafer for sheet resistance measurements with the four-point probe, correction factors for sample geometry would not need to be taken into account.

The Si-B phase that may form during boron diffusion is known to be a conductive layer. Therefore, the presence of a Si-B phase on the Si surface can be detected through four-point probe measurements. The sheet resistance for a

sample with a Si-B layer would be lower than that for an identically doped sample without a Si-B surface layer. The four-point probe is measuring the lower resistivity of the Si-B layer in parallel with the junction layer, thus resulting in an overall lower resistivity. By comparing the sheet resistance of the half-wafer samples that undergo the modified deglaze process to the sheet resistance of the device wafers that undergo the standard deglaze, we are able to evaluate the effectiveness of the nitric acid oxidation step in removing the Si-B phase.

3.3.4 X-Ray Diffraction

Small samples were cleaved from the half wafer that did not go through a deglaze. An x-ray diffractometer with a CuK_α x-ray source was used to detect the presence of the Si-B phase. The samples were first dipped in concentrated HF to remove BSG so that the signal intensity of the Si-B phase would not be diminished. X-ray scans of diffraction angles (2θ) between 20° and 70° were first performed. However, because of Si-B layers of 100 Å or less were expected, smaller scans between 30° and 35° were done at a slower scan rate to increase signal intensity. The most intense peaks of the Si-B phases lay in this 2θ range.

3.3.5 Spreading Resistance Analysis

Samples were sent to Solecon Laboratories, Inc., for spreading resistance analysis for the purpose of obtaining resistivity and dopant profiles. Because this technique is expensive, certain samples were selected for this analysis method. To obtain a temperature and time relationship to junction depth, dose, and surface

carrier concentration, the three samples doped at 900°C and the two doped at 800° and 1000° for 45 minutes for each diffusion ambient were selected for analysis. This was done for the same reasoning previously described in Section 3.3.1 when choosing samples that would be imaged by TEM

.

3.4 Characterization Methods Used on Device Wafers

One half of each device wafer was left blank for four-point probe measurements. Optical measurements were also performed on this blank half of the wafer for reasons that will be given in the appropriate following sections. The devices tested for electrical characteristics include metal-oxide-semiconductor (MOS) capacitors and van der Pauw test structures.

3.4.1 Capacitance-Voltage Measurements

The MOS capacitors fabricated were tested for capacitance-voltage (CV) characteristics. The definition of capacitance is

$$C = \frac{dQ}{dV} \qquad \textit{Eq. 3.1}$$

where dQ is the change in charge due to a change in voltage, dV. During CV measurements, a small amplitude ac voltage superimposed on a dc bias is applied to the gate metal contact. The ac voltage creates a change in charge and thus, a capacitance is measured. The dc bias determines the region of device behavior, e.g., accumulation, depletion, or inversion. Since the bias is applied to the gate, the following relationship applies:

$$C = \frac{dQ_G}{dV_G} \qquad \textit{Eq. 3.2}$$

where Q_G is the gate charge and V_G is the gate voltage. In a MOS structure, charge neutrality requires that the gate charge be compensated for by an equal and opposite charge in the remaining areas of the structure (the oxide, the semiconductor, and the oxide-semiconductor interface):

$$Q_G = -\left(Q_s + Q_{ox} + Q_{it}\right) \qquad \textit{Eq. 3.3}$$

where Q_s is the charge in the semiconductor, Q_{ox} is the charge in the oxide, and Q_{it} represents interface trapped charges that are present at the Si-SiO_2 interface due to defects and impurities. In an ideal situation, there are no oxide charges present, and therefore $Q_{ox} = 0$. Assuming this ideal case, the gate voltage becomes $-(Q_s + Q_{it})$.

By Kirkhoff's law, the following relationship must apply:

$$V_G = V_{ox} + V_s \qquad \textit{Eq. 3.4}$$

where V_{ox} is the voltage drop across the oxide and V_s is the voltage drop across the semiconductor. With the above expressions for Q_G and V_G, the measured capacitance for the CV measurements can be written as:

$$C = -\frac{dQ_S + dQ_{it}}{dV_{OX} + dV_S} \qquad \textit{Eq. 3.5}$$

which can also be written as

$$C = -\frac{1}{\frac{dV_{ox}}{dQ_s + dQ_{it}} + \frac{dV_s}{dQ_s + dQ_{it}}} \qquad \textit{Eq. 3.6}$$

The charge in the semiconductor, in general, is due to hole charge Q_P, space-charge region bulk charge Q_B, and electron charge Q_N. Therefore, the capacitance can be rewritten further as:

$$C = -\frac{1}{\frac{dV_{OX}}{dQ_S + dQ_{it}} + \frac{dV_S}{dQ_P + dQ_N + dQ_B + dQ_{it}}} \qquad \textit{Eq. 3.7}$$

Using the general definition for capacitance, the above equation becomes

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_P + C_B + C_N + C_{it}}} \qquad \textit{Eq. 3.8}$$

Our MOS devices were fabricated on a n-type substrate. Therefore, for positive gate voltages, the semiconductor surface is heavily accumulated with electrons and Q_N dominates, resulting in a very large value for C_N. The total capacitance measured is then approximately equal to C_{ox}. For small negative gate voltages, the surface is depleted and the charge due to the space-charge region charge, Q_B, dominates. The trapped interface charge capacitance also contributes to the measured capacitance. The total capacitance is the combination of C_{ox} in series with C_B in parallel with C_{it}. When C_P begins to appear in weak inversion, the total capacitance becomes:

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_B + C_N + C_{it}}} \qquad \textit{Eq. 3.9}$$

In strong inversion, which occurs at negative gate voltages for n-type substrates, Q_P dominates and C_P becomes very large. The low-frequency (LF) CV curve results if the inversion charge Q_P is able to follow the applied ac voltage. In this case, the total capacitance once again becomes C_{ox} as in the accumulation region. When Q_P is unable to follow the high frequency of the applied ac voltage, the measured capacitance is the combination of C_{ox} in series with C_B resulting in

the high-frequency (HF) CV curve. If the voltage ramp rate is so high that no inversion charge can form, a deep depletion CV curve is produced.

Using the Keithley CV tester, low frequency and high frequency CV curves were obtained for the following MOS capacitors sizes: 100 μm x100 μm, 200 μm x 200 μm, 300 μm x 300 μm, and 500 μm x 500 μm. Five capacitors for each size were measured and an average CV curve was calculated. The average high frequency CV curves for the 500 μm x 500 μm devices were later inputted into a computer program developed by Dr. John Hauser, a professor in the Electrical Engineering Department at NCSU, that is able to extract flatband voltage from the inputted data and calculate poly depletion effects. For the capacitance measurements, the bias was ramped from +3 V to –3 V (from accumulation to inversion) with a 20 mV voltage step and a time delay of 0.07 seconds, resulting in an approximate ramp rate of 0.286 V/sec.

The capacitance of a material is

$$C = \frac{\varepsilon A}{d} \qquad \textit{Eq. 3.10}$$

where ε is the permittivity of the material, A is the cross-sectional area, and d is the material layer thickness. The theoretical value for the oxide capacitance for the device wafers used in this experiment can therefore be calculated, assuming an oxide permittivity of $\varepsilon_{ox} = 3.9 \times \varepsilon_o$, where ε_o is the permittivity of vacuum (8.85×10^{-14} F/cm). Solving for the oxide capacitance using the average oxide thickness measured on the gate monitor wafer (150 Å), we obtain the values listed in Table 3.3 for each size capacitor measured. Plots of C_{ox} vs. the capacitor area should be

linear and have a slope approximately equal to ε_{ox}/t_{ox}, where t_{ox} is the gate oxide thickness. These plots were constructed for each device wafer to characterize the quality of each doping process.

The theoretical flatband voltage for our MOS devices is simply equal to the metal-semiconductor work function, assuming no oxide charges. To calculate the metal-semiconductor work function, a further assumption that the polysilicon is degenerately doped (ϕ_p=0.56V) is assumed. According to the wafer manufacturer of the silicon wafers used to fabricate the device wafers, the doping level of the substrate is approximately 1 x 10^{16} cm^{-3}. Therefore using the equation

$$\phi_s = \frac{kT}{q} \ln \frac{n_i}{N_D} \qquad \textit{Eq. 3.11}$$

a value of -0.348 V for the substrate potential, ϕ_s, is calculated, where N_D is the substrate doping level, n_i is the intrinsic carrier concentration (1.45 x 10^{10} cm^{-3}),

Table 3.3 – Theoretical oxide capacitance values for tested capacitors

Capacitor Area	Theoretical Oxide Capacitance (pF)
100 μm x100 μm	23
200 μm x 200 μm	92
300 μm x 300 μm	207
500 μm x 500 μm	575

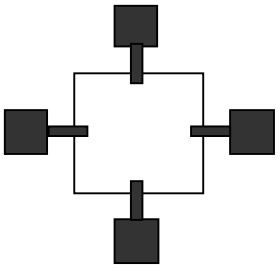

Figure 3.2 – Schematic of the van der Pauw structure
tested for sheet resistance data

and kT/q is 0.0259 V. This gives a metal-semiconductor work function ϕ_{ms} of:

$$\phi_{ms} = 0.56 - (-0.348) = 0.908V \qquad \textit{Eq. 3.12}$$

Any deviations of experimentally extracted flatband voltages from this theoretical value may be attributed to gate oxide charges.

3.4.2 Van Der Pauw Measurements

A schematic of the van der Pauw structure tested on all wafers is shown in Figure 3.2. The poly van der Pauw structures were tested, from which we obtained sheet resistance, ρ_s, for the doped poly. A current, I, was applied across two adjacent contacts and the voltage, V, was then measured across the two remaining contacts. Since the structure is symmetrical, the sheet resistance can be calculated from the following relationship:

$$\rho_s = \frac{\rho}{t} = \left(\frac{\pi}{\ln(2)}\right) \times \left(\frac{V}{I}\right) \qquad \textit{Eq. 3.13}$$

By using the resistivity vs. doping concentration plot given in *Semiconductor Material and Device Characterization* by D. K. Schroder, developed for boron-doped Si, an estimation of poly doping can be obtained with the use of the van der Pauw sheet resistance values.

3.4.3 Four-Point Probe Measurements

At the end of the device fabrication sequence, sheet resistance measurements with the four-point probe were obtained on the blank half of the device wafers. In Chapter IV, these measurements are compared to sheet resistance measurements from etched half-wafer samples using the modified deglaze process.

3.4.4 Optical Measurements

Optical measurements of the blank side of the device wafer were acquired using the "oxide on Si" program at the end of the device fabrication sequence. This was done to verify the absence of all diffusion byproducts from the wafer surface. As will be discussed in Chapter IV, some wafers did not dewet after the deglaze. This hydrophilic surface was assumed to indicate the presence of the Si-B phase, which could be verified by optical measurements.

CHAPTER IV

Experimental Results and Discussion

4.1 Transmission Electron Microscopy Results

The TEM work completed as was described in Chapter III showed the presence of a thick amorphous layer (BSG) on the Si substrate for all samples. Not all samples imaged, however, showed the presence of a Si-B crystalline layer sandwiched between the BSG and Si substrate. The only sample showing this layer (of the nitrogen ambient processed samples imaged) was the sample doped at 1000°C for 45 minutes. This result confirms that the hydrophilic surface of this wafer after the deglaze was due to the presence of Si-B. Images show that this layer was very non-uniform and caused a rough surface on the Si. Because of this severe non-uniformity, an exact thickness could not be extracted for the Si-B layer. An image of a sample doped in the nitrogen-oxygen ambient at 1000°C for 45 minutes showed a similar structure to the 1000°C/45 min./N_2 sample and is shown in Figure 4.1. From these two images, the Si-B layer thickness seemed to be on the order of 50 Å.

Images for two additional samples doped in the nitrogen-oxygen ambient were obtained (800°C/45 min. and 900°C/30 min.) These images confirmed the non-presence of a Si-B layer for samples doped under 1000°C. An additional observation for the 900°C/60 min./N_2 and 900°C/30 min./N_2O_2 samples is significant distortion at the Si-SiO_2 interface, which may allow for the formation of defect levels in devices. All TEM images are included in Appendix B.

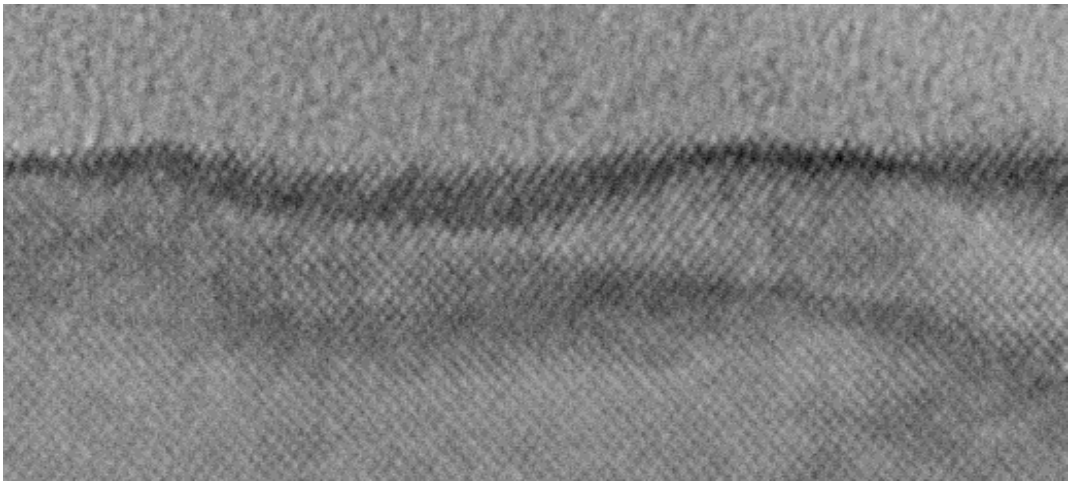

Figure 4.1 – Cross-sectional TEM image of a sample doped at 1000°C/45 min/N_2O_2

BSG layer thicknesses were extracted from TEM images. Although the method of extraction was very susceptible to errors, the measurements were expected to give reasonable estimations of the actual BSG layer thickness. In the following section, these measurements will be compared to the optical measurements of the BSG layer.

4.2 Optical Measurements

The BSG thickness measured for each sample is given in Table 4.1. For samples C1 and C3, a measurement could not be obtained with the "oxide on Si" program. The presence of Si-B is partly the reason for this result. An additional reason may be the rough Si surface due to the non-uniformity of the Si-B phase. A possible reason as to why this same effect was not encountered for the C2 and C4 samples is that the oxygen content in the atmosphere had some kind of effect on the uniformity of the Si-B layer. Thus, the Si wafer surface did not have the amount of roughness encountered in the wafers doped in nitrogen only. A qualitative comparison of the TEM images for C1 and C2 seem to support this idea (see Appendix B for TEM images).

As is expected, Table 4.1 shows that, in general, BSG thickness increases with temperature and time. At the higher diffusion temperatures, the presence of oxygen in the atmosphere resulted in a thicker BSG layer because of the additional oxide formed from the reaction between oxygen and the Si substrate. This effect was not noticed at 800°C due to the lower diffusion temperature. A lower temperature leads to a lower boron diffusion coefficient, and therefore, to slower reaction rates. The

Table 4.1 – BSG thickness measurements

Sample	Optical	TEM
A1 (800°C/45 min./N_2)	536	521
A2 (800°C/45 min./N_2O_2)	452	--
A3 (800°C/20 min./N_2)	482	--
A4 (800°C/20 min./N_2O_2)	473	417
B1 (900°C/60 min./N_2)	1166	885
B2 (900°C/60 min./N_2O_2)	1391	--
B3 (900°C/30 min./N_2)	1284	--
B4 (900°C/30 min./N_2O_2)	1357	1133
B5 (900°C/30 min./N_2)	1329	1029
B6 (900°C/30 min./N_2O_2)	1104	--
B7 (900°C/10 min./N_2)	942	841
B8 (900°C/10 min./N_2O_2)	1065	--
C1 (1000°C/45 min./N_2)	--	2537
C2 (1000°C/45 min./N_2O_2)	3773	--
C3 (1000°C/20 min./N_2)	--	--
C4 (1000°C/20 min./N_2O_2)	2561	--

oxidation of the Si substrate may increase the BSG thickness at first, but as time of diffusion increases, the slow diffusion of boron through the oxide layer greatly reduces the amount of boron reaching the Si surface, and therefore results in less formation of BSG.

Optical measurements made on the blank side of device wafers verified the removal of diffusion byproducts for all wafers except the 1000°C/45 min./N_2 doped wafer. A thickness was returned when using the "SiO_2 on Si" program. Although the actual value of this returned thickness is not any kind of accurate measurement of the layers present on the Si surface, they reveal the presence of the Si-B phase on the surface that should have been removed by the deglaze. This was also the only wafer that remained a brownish yellow color after the deglaze. Therefore, we can conclude that at this diffusion condition, the standard deglaze process is not effective. Table 4.2 is a comparison of the optical measurements obtained from the device wafers and from the half-wafer samples that underwent the modified deglaze etch. Only the samples for which a thickness value was returned after the deglaze etch are reported.

Table 4.2 – Optical measurements on deglaze etched samples

Diffusion Condition	Device Wafer	Half-Wafer Blank
1000°C/45 min./N_2	551 Å	610 Å
1000°C/45 min./N_2O_2	<100 Å	282 Å
1000°C/20 min./N_2	<100 Å	384 Å
1000°C/20 min./N_2O_2	<100 Å	143 Å

For all other samples, a "less than 100 Å" measurement was returned since this is the resolution limitation for the "Si on SiO_2" program. From this data, we can conclude that all wafers doped at 1000°C were the only wafers that formed the Si-B phase during diffusion. However, even though no film thickness was returned for the last 3 device wafers listed in Table 4.2, a hydrophilic surface indicates that the Si-B phase is still present on these wafers after the deglaze. Therefore we can conclude that the nitric acid oxidation is not effective in removing this layer.

4.3 Four-Point Probe Measurements

Sheet resistance values obtained from the four-point probe for both the device wafers and the half-wafer samples are compared in Figure 4.3. No significant difference between the wafers that underwent the standard deglaze and those that underwent the modified deglaze etch is seen. For those wafers doped at 1000°C, a successful removal of the Si-B phase would be indicated by a higher sheet resistance than that obtained from the samples simply etched in HF. This is not the case, and thus further proves that the nitric acid step in the deglaze process may not be effective in removing the Si-B layer from the Si wafer surface. For all samples, no significant difference is seen between sheet resistance of monitor wafers and that of device wafers.

Plots of log sheet resistance vs. log diffusion time for samples doped at 900°C were constructed to establish a sheet resistance and time relationship. A linear fit to this data by linear regression would give this relationship:

$$\log \rho_s = n \log t \Rightarrow \rho_s \alpha t^n \qquad \textit{Eq. 4.1}$$

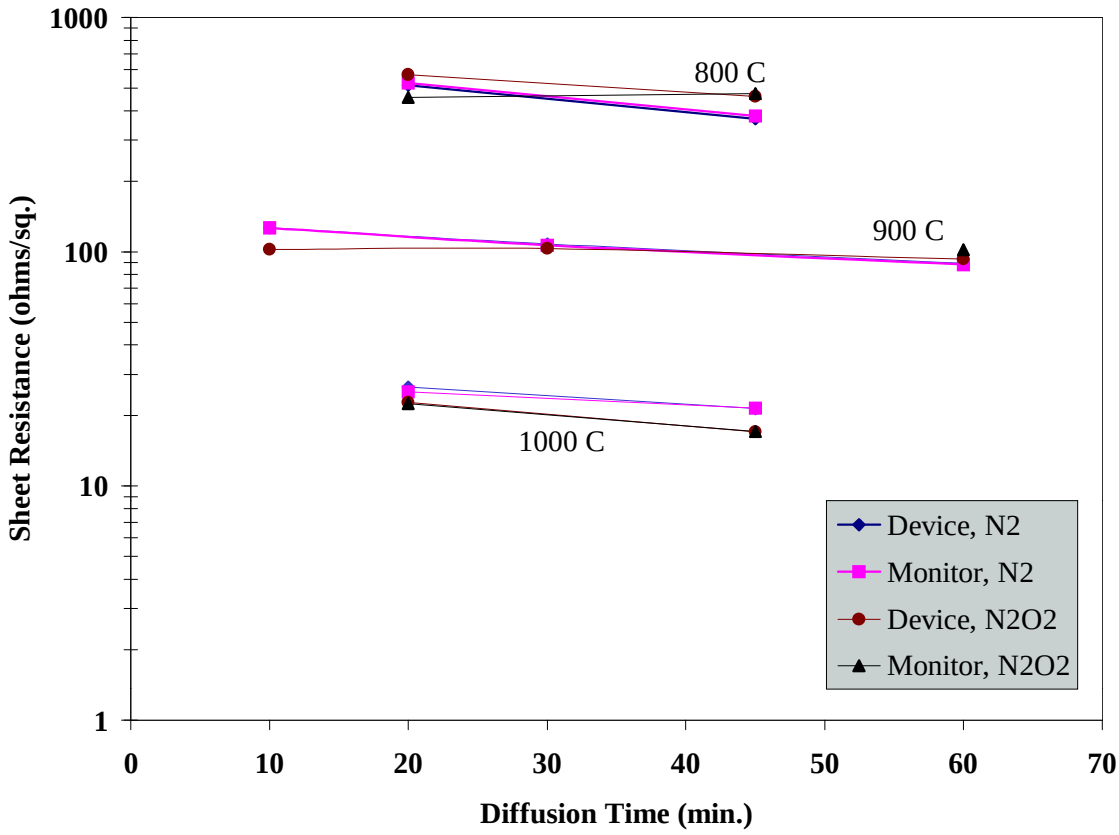

Figure 4.2 – Plot of four-point probe sheet resistance
vs. diffusion time for all diffusion runs

where n is a constant and t is the diffusion time in minutes. A high R^2 value for this linear fit would indicate a good model for the sheet resistance and diffusion time relationship. Only those samples doped in a nitrogen atmosphere reported a high R^2 value of 0.96 as shown in Figure 4.4. Therefore only for these samples could we establish a relationship between sheet resistance and diffusion time. The slope of the fitted line reveals that $\rho_s \alpha t^{1/5}$. According to the R^2 value, this model accounts for 96% of the variability in the data. Using this model, a value for a doped sample at 900°C for 45 minutes was extrapolated and used to construct a plot of log sheet resistance vs. 1/kT for samples of a 45 minute diffusion time. This plot shown in Figure 4.5 also reveals a good linear fit, meaning that sheet resistance is proportional to $e^{1/kT}$.

Reasons for not being able to establish a temperature and time relationship for samples doped in a nitrogen-oxygen ambient may include boron depletion from the Si surface, thus affecting sheet resistance. Spreading resistance analysis results will confirm this effect.

4.4 X-Ray Diffraction Results

For the x-ray diffraction scans performed on all samples, no Si-B diffraction peaks were detected. We cannot conclude, however, that the reason for this result is that there was no Si-B phase formed. Because all samples doped at 1000°C did not dewet after a long HF etch, it was expected that these samples would definitely show Si-B peaks, but this was not the case. Since TEM images show a definite crystalline Si-B phase, the only reasonable explanation for the absence of Si-B peaks in x-ray

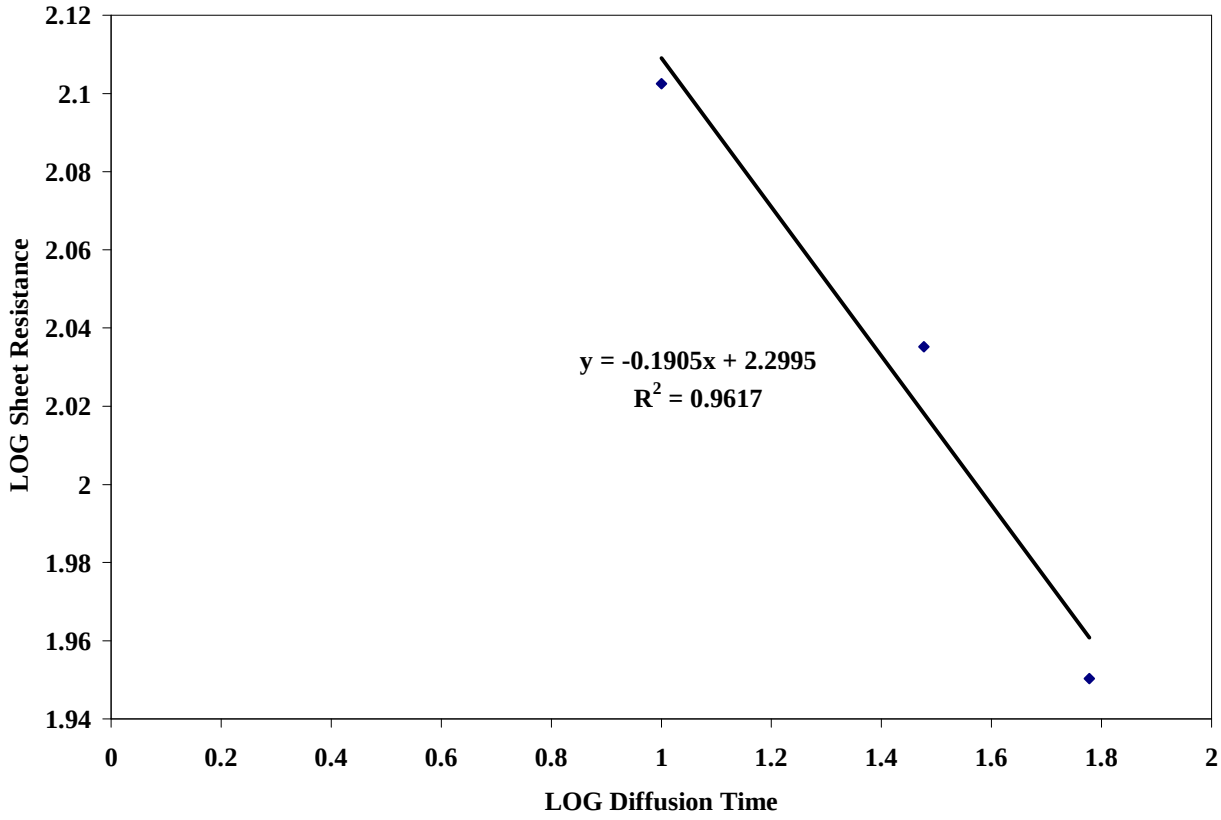

Figure 4.3 – Plot of log sheet resistance vs. log diffusion time
for a constant diffusion temperature of 900°C

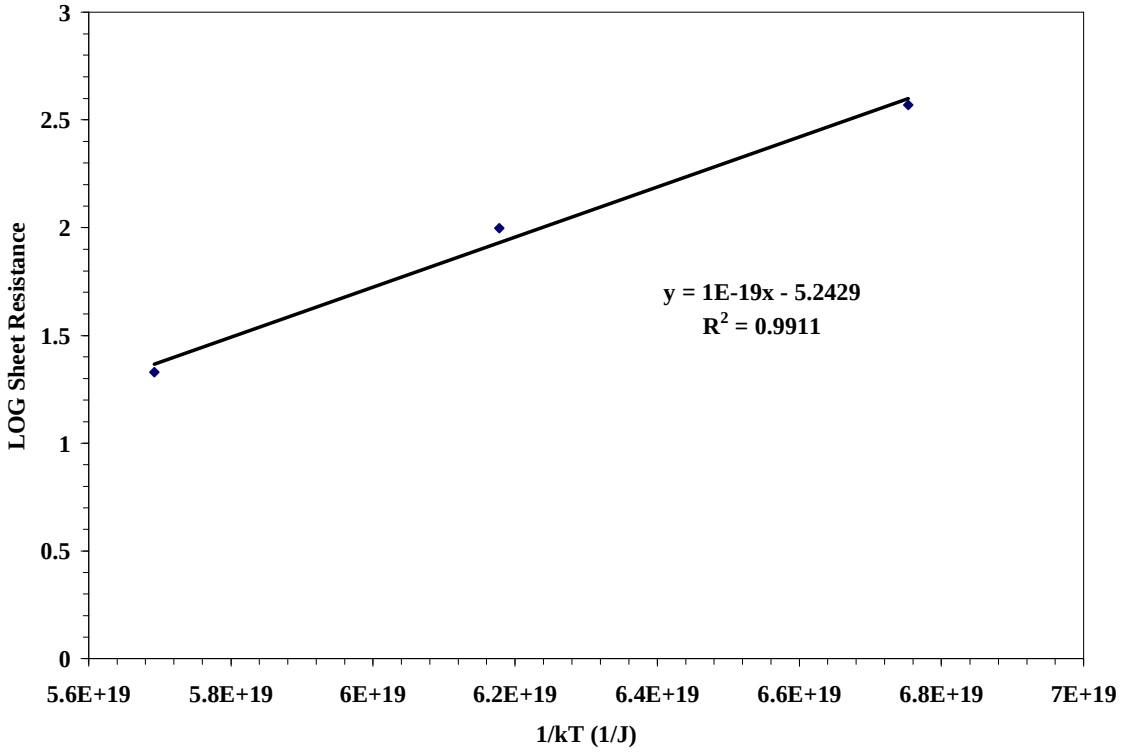

Figure 4.4 - Plot of log sheet resistance vs. 1/kT
for a constant diffusion time of 45 minutes

diffraction measurements is that the layer was too thin to produce x-ray signals of a large enough intensity. This problem may be solved by using larger diffraction and/or scattering slits. These slits control the size of the irradiated area and thus the signal intensity. An additional solution would be to do scans at a slower rate than used in this experiment.

4.5 Spreading Resistance Analysis Results

A total of ten samples were analyzed using SRA as described in Chapter III. Relationships between the dose and diffusion time could not be established because of the low R^2 value returned for the plot of log dose versus log diffusion time. A log junction depth vs. log diffusion time plot, however, did show a significant relationship and is shown in Figure 4.6. Slopes of approximately 0.2 indicate that x_j is proportional to $t^{1/5}$. A subsequent plot of log junction depth vs. 1/kT also revealed a significant R^2 value and is therefore a good model (Figure 4.7).

Dopant profiles obtained from the samples, shown in Appendix C, show an increase in boron depletion at the Si wafer surface with diffusion time. In general, the nitrogen-oxygen atmosphere seemed to enhance this depletion. This is most likely due to the larger BSG thicknesses formed in an oxidizing atmosphere. In addition, the diffusion of boron in silicon is enhanced in an oxidizing atmosphere, and therefore accounts for the larger junction depths achieved for samples doped in the nitrogen-oxygen atmosphere.

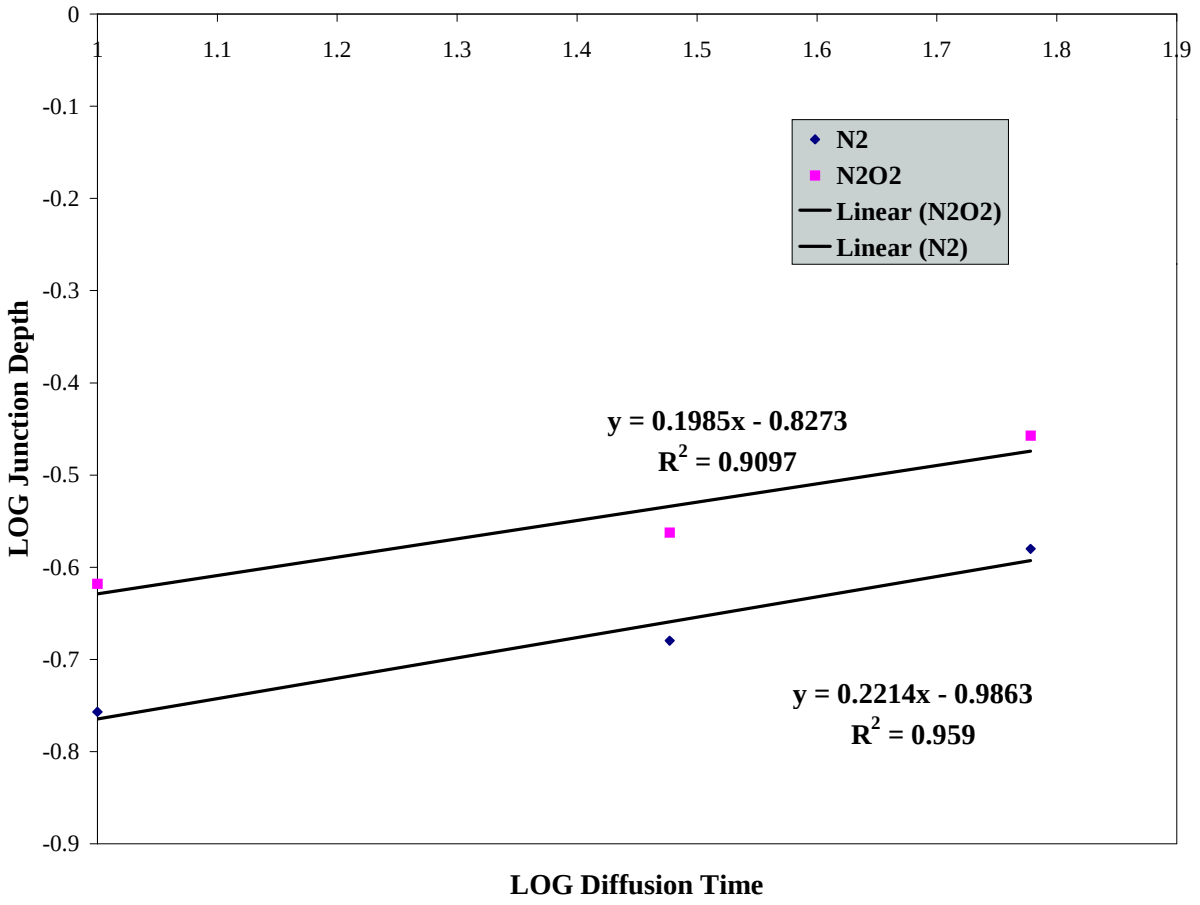

Figure 4.5 – Plot of log junction depth vs. log diffusion time
for a 900°C diffusion temperature

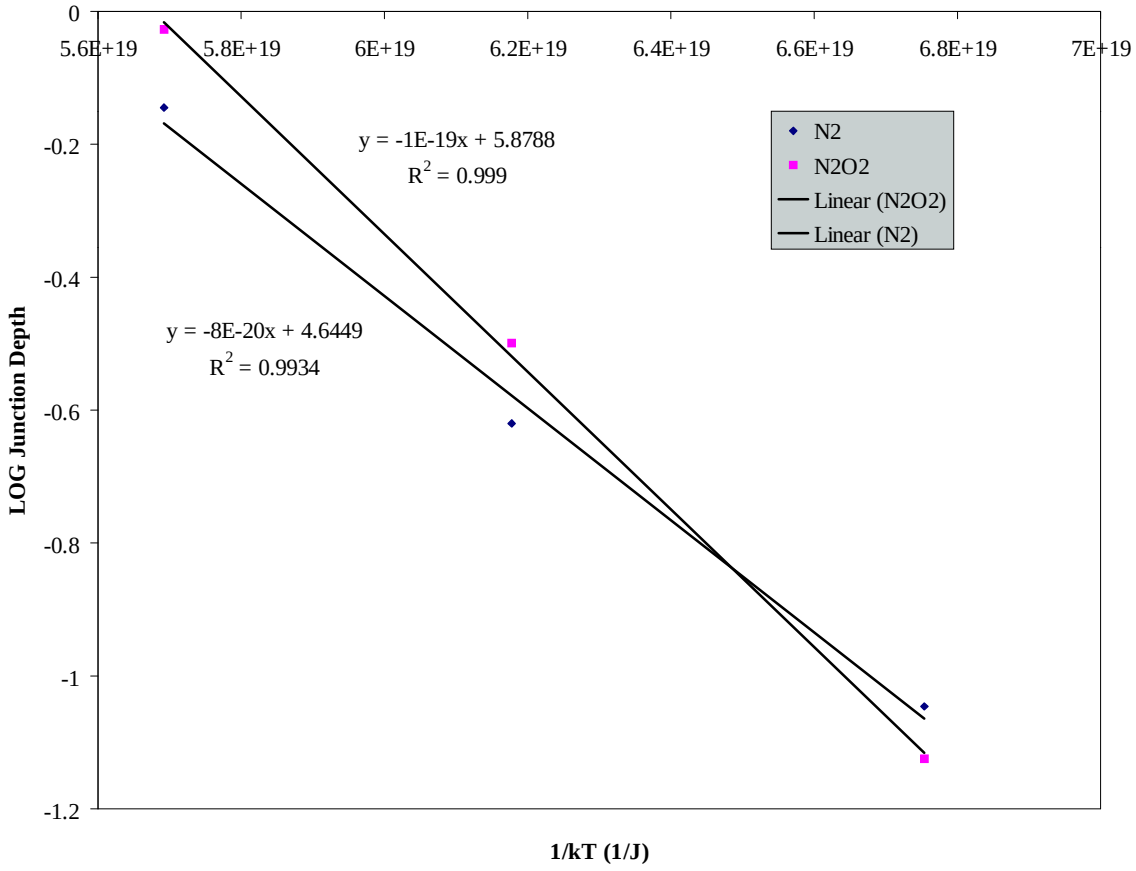

Figure 4.6 – Plot of log junction depth vs. 1/kT
for a constant diffusion time of 45 minutes

4.6 Capacitance-Voltage Measurements

Average high frequency CV curves for the 500 μm x 500 μm capacitors were obtained as explained in Chapter III. Figure 4.8 shows a typical HF curve obtained from most device wafers. The actual measured CV curve and the CV curve after correcting for polysilicon depletion effects are not significantly different. The most significant differences in these curves was observed for the 900°C/60 min. diffusion runs in both gaseous ambients. HF CV curves for all samples are located in Appendix D. Note that no data was obtained for wafers doped at 1000°C because no coherent data could be obtained from these devices. The device degradation may be attributed to the presence of the Si-B phase.

In order to evaluate each doping process qualitatively, plots of C_{ox} versus the capacitor area were plotted. Note that the C_{ox} values plotted are averages from five measurements per capacitor area. A linear fit to the plotted points shows very high R^2 values for all devices. In addition, similar slopes of this plot were achieved ranging from 2.26 x 10^{-7} F/cm^2 to 2.36 x 10^{-7} F/cm^2, resulting in t_{ox} values between 146 Å and 153 Å. This is very close to the average gate oxide thickness measured on the gate monitor during the process flow (150 Å). See Appendix E for a C_{ox} vs. area plot for each device wafer.

Flatband voltages extracted from the 500 μm x 500 μm capacitor CV data are plotted in Figure 4.9 versus thermal budget. Using our theoretical calculation of a flatband voltage of 0.908 V as a basis for determining an optimum process, the wafer doped at 800ºC/20 min./N_2O_2 showed the best process, with the 800°C

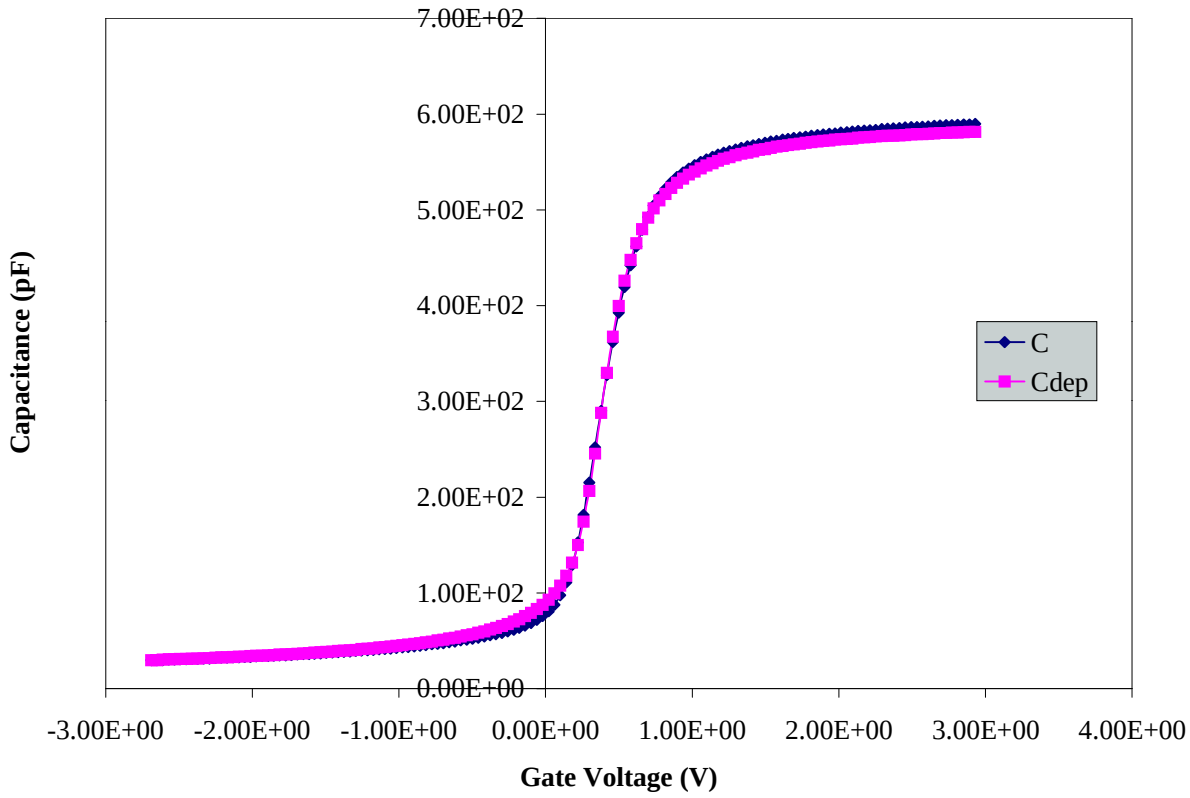

Figure 4.7 – High frequency CV curve for 900°C/30 min./N_2 doped wafer

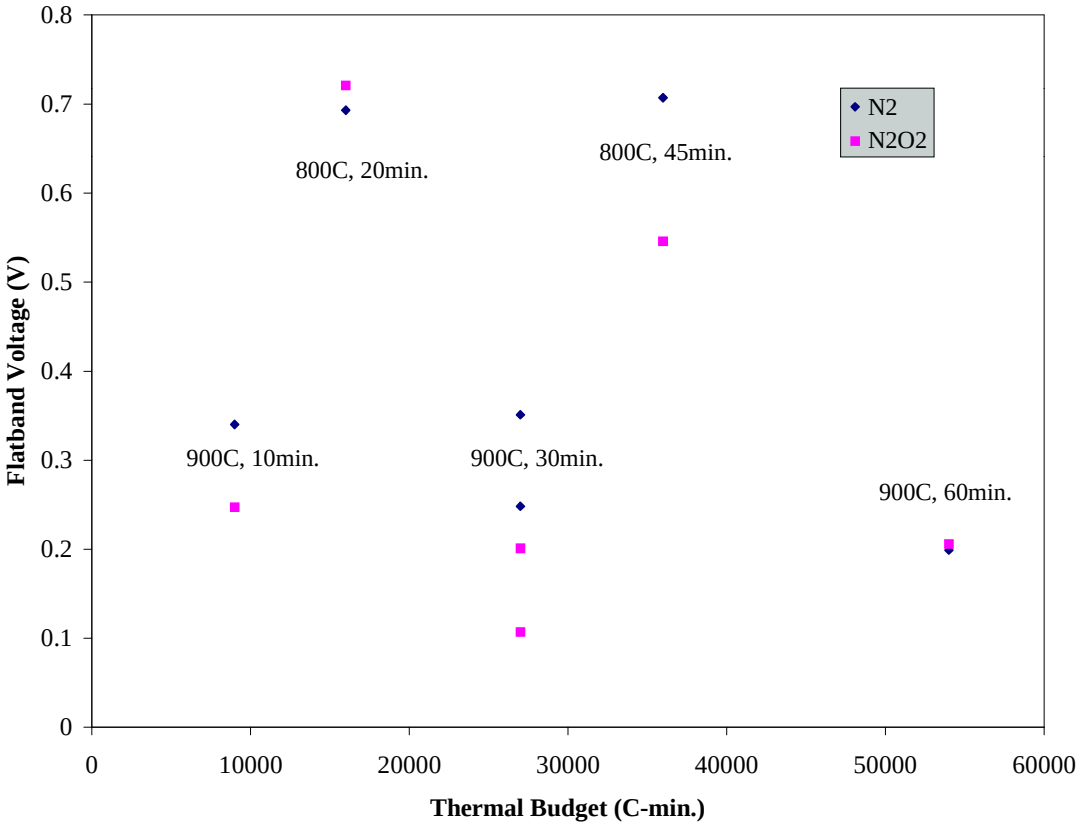

Figure 4.8 – Plot of flatband voltage vs. thermal budget

diffusion runs in N_2 at a close second. Generally, flatband voltage shifts are attributed to charges in the oxide. Significant shifts in the flatband due to positive oxide charges occurred with the devices fabricated at 900°C. We can assume that boron penetration in the gate oxide is the reason for this large shift in the flatband. Boron penetration may be occurring at the optimum 800ºC diffusion conditions as well, but the effects are less significant in this case.

Low frequency CV curves were also obtained for each device wafer, but were not analyzed because of unexplained anomalies in the curves. In inversion, the measured capacitance did not become the oxide capacitance as it should have. It is possible that the voltage ramp rate used to test the capacitors was too fast and did not allow enough time for the device to reach equilibrium. Therefore, further testing of the capacitors at a slower ramp rate should be completed to obtain low frequency CV curves.

4.7 Van Der Pauw Measurements

Sheet resistance values for polysilicon were extracted from van der Pauw measurements. The average polysilicon thickness measured on the poly monitor was 1398 Å. This thickness was used to obtain polysilicon resistivity from the sheet resistance measurements:

$$\rho = \rho_s \times t \qquad \textit{Eq. 4.2}$$

A reference plot of resistivity vs. doping concentration for boron doped silicon was then used to obtain a poly doping level from the calculated resisitivity values. Results show that the polysilicon was degenerately doped for all devices (i.e., above

$3 \times 10^{19} cm^{-3}$). A graph of poly doping versus the thermal budget (diffusion temperature x time) is shown in Figure 4.10. Note that wafers doped at 1000°C did not produce functioning devices, and therefore, poly doping level could not be extracted for these wafers. In general, higher values of poly doping were obtained with the nitrogen diffusion ambient for wafers with equivalent thermal budgets.

The highest doping level of poly was achieved with the 900°C/60 min./N_2 diffusion condition, but at the cost of a high thermal budget. Almost equivalent levels of poly doping can be achieved at the 900°C/30 min/N_2 and 900°C/10 min/N_2 conditions. Since the poly doping at these conditions is in the 9×10^{19} cm^{-3} to 1×10^{20} cm^{-3} range, these are the optimum processing conditions for the doping of poly. The 800°C diffusion runs showed only slightly lower levels of poly doping, but were still degenerately doped, with the runs in the nitrogen ambient showing the highest levels.

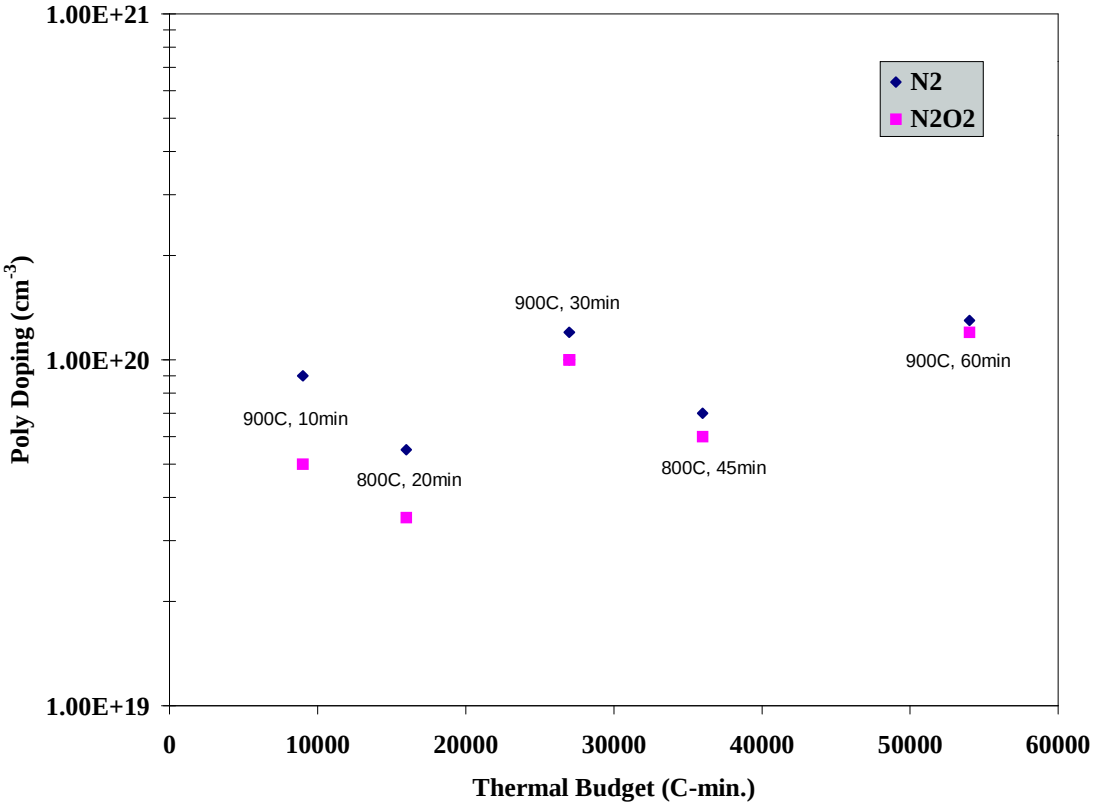

Figure 4.9 – Plot of poly doping level vs. thermal budget

CHAPTER V

Summary and Conclusions

5.1 Summary

The main objective of this thesis was to determine an optimum process for the boron doping of p-type implants and polysilicon gates of MOS devices using boron nitride solid source diffusion. To achieve this goal, a design of experiments was constructed that studied a wide range of diffusion conditions in which temperature, time, and diffusion ambient were varied. MOS devices were fabricated at the 14 different diffusion conditions determined by the experimental design. A replicate run was done at the center points of the design to address process repeatability, for a total of 16 different runs. Monitor wafers were also doped at these 16 conditions.

Polysilicon van der Pauw test structures and MOS capacitors were tested on all device wafers for the extraction of poly doping and flatband voltage. Information could not be extracted from devices processed at 1000°C because they showed severe degradation, most likely due to the presence of the Si-B phase. Consistent linear plots of C_{ox} vs. capacitance area showed an overall good quality process for the device wafers. Severe shifts in flatband voltage were found for wafers doped at 900°C. Because shifts in flatband are due to oxide charges, the shift may be partially due to boron penetration in the gate oxide. Van der Pauw measurements gave poly doping levels in the 10^{19} cm^{-3} and 10^{20} cm^{-3} range.

Materials characterization methods, such as TEM, were used on monitor wafers to characterize the structure formed during diffusion. Spreading resistance

analysis gave dopant profiles for certain processing conditions. From SRA, models for the relationship between junction depth and diffusion time and temperature were established. A relationship between sheet resistance and diffusion time and temperature was only established for the nitrogen gas ambient process. Four-point probe and optical measurements were used to determine the presence of the Si-B phase and evaluate the nitric acid oxidation step in the standard deglaze process. An attempt was made to use x-ray diffraction to detect the Si-B phase layer but was unsuccessful.

5.2 Conclusions

The optimal conditions for the doping of poly according to calculations from van der Pauw measurements, occurred at the 900°C/60 min./N_2 diffusion run. However, all diffusion conditions resulted in degenerately doped poly. Close to theoretical flatband voltages were obtained from the runs performed at 800°C in a N_2 ambient and at 800°C/20 min./N_2O_2. Taking all of these results into account, any diffusion process performed at 800°C in a nitrogen ambient can be expected to give good overall device characteristics. The lowest thermal budget would be achieved with the 800°C/20 min./N_2 diffusion process. Furthermore, the standard deglaze process used for this experiment should be modified since the nitric acid step did not fully oxidize the Si-B phase.

5.2 Future Work

The use of a statistical package to determine temperature and time models for sheet resistance and dose should be explored. Further testing should be done of MOS capacitors in an effort to verify the poly doping levels calculated through van der Pauw measurements. This can be accomplished by obtaining low frequency CV curves using a higher ramp rate than the one used in this experiment to ensure device equilibrium during the test.

Modification of the deglaze etch should be carried out. A thermal oxidation can replace the nitric acid step for the removal of the Si-B phase. The question should be addressed as to whether an oxidation step is needed at all if the Si-B phase is not formed. This may easily be done by fabricating devices that undergo an oxidation step in the deglaze and comparing device characteristics, such as flatband voltage, to devices that only undergo an HF etch for the deglaze.

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APPENDIX A

Device Process Sequence

1. Wafer Marking and Initial Characterization
    - Hand scribe wafer identification marks onto backside of all wafers using a diamond tip pencil
    - Four-point probe measurements to verify wafer resistivity

2. Initial Clean (JT Baker)
    - Clean wafers in JT Baker (a 5:1:1 solution of deionized (DI) water, NH_4OH, and H_2O_2) for 5 min.
    - Rinse wafers in DI water for 5 min.
    - Spin dry wafers in N_2

3. Field Oxide Growth (1000°C, 40 min., 2% HCl, dry/wet/dry oxidation, 3000 Å target)
    - Boat out silica boat
    - Load wafers in silica boat wafer flat up
    - Boat in silica boat at 750°C in 7200 sccm N_2 and 70 sccm O_2 (10 min.)
    - Ramp up furnace temperature to 1000°C (31 min.)
    - Dry pre-oxidation in 1000 sccm O_2 and 2% HCl (10 min.)
    - Wet oxidation in 1000 sccm O_2, 2000 sccm H_2, and 2% HCl (40 min.)
    - Dry post-oxidation in 1000 sccm O_2 and 2% HCl (10 min.)
    - Cool down furnace to 750°C in 7200 sccm N_2 (45 min.)
    - Boat out wafers (10 min.)

4. Active Mask Lithography

    - Spin HMDS Primer onto wafer at 4500 rpm for 40 sec.
    - Spin positive photoresist (JSR 10cp) onto wafer at 4500 rpm for 40 sec.
    - Pre-exposure bake on hot plate at 90°C for 1 min.
    - Expose 1998 ECE 539 Active Mask for 8 sec.
    - Post-exposure bake on hot plate at 115°C for 1 min.
    - Develop for 1 min.
    - Rinse wafers in DI water for 5 min.
    - Spin dry in N_2
    - Post-develop bake on hot plate at 115°C for 5 min.

5. Descum

    - Standard descum plasma etch using the March Instruments Asher (80 sccm O_2, 600 mT pressure) for 3 min.

6. Field Oxide Etch

    - Etch in 10:1 buffered oxide etch (BOE) solution for 330 sec.
    - Rinse in DI water for 5 min.
    - Spin dry in N_2

7. Photoresist Removal

- 10 min. in Nanostrip bath #1
- 5 min. in Nanostrip bath #2
- 5 min. rinse
- Spin dry in N_2

8. Surface Clean (JT Baker)
    - 5 min. in JT Baker clean
    - Rinse in DI water for 5 min.
    - Spin dry in N_2

9. Gate Oxide Growth (950°C, 10 min., with HCl, 150 Å target)
    - Boat out silica boat
    - Load wafers in silica boat wafer flat up
    - Boat in silica boat at 750°C in 7200 sccm N_2 and 200 sccm O_2 (10 min.)
    - Ramp up furnace temperature to 950°C (31 min.)
    - Dry oxidation in 2860 sccm O_2 and 135 sccm HCl (10 min.)
    - Cool down furnace to 750°C in 7200 sccm N_2 (45 min.)
    - Boat out wafers (10 min.)

10. Polysilicon Deposition (1500 Å target)

- Load wafers in silica boat wafer flat up in low pressure chemical vapor deposition (LPCVD) furnace
- Deposit amorphous silicon (540°C, 100 mT pressure, 100% Si_2H_6) for 46.8 min.

11. Poly Gate Lithography

- Spin HMDS Primer onto wafer at 4500 rpm for 40 sec.
- Spin positive photoresist (JSR 10cp) onto wafer at 4500 rpm for 40 sec.
- Pre-exposure bake on hot plate at 90°C for 1 min.
- Expose 1998 ECE 539 Poly Mask for 8 sec.
- Post-exposure bake on hot plate at 115°C for 1 min.
- Develop for 1 min.
- Rinse wafers in DI water for 5 min.
- Spin dry in N_2
- Post-develop bake on hot plate at 115°C for 5 min.

12. Polysilicon Etch

- Etch in poly etch solution (wafers visually monitored during etch to determine etch endpoint)
- Rinse in DI water for 5 min.
- Spin dry in N_2

13. Photoresist Removal

- 10 min. in Nanostrip bath #1
- 5 min. in Nanostrip bath #2
- 5 min. rinse
- Spin dry in N_2

14. Surface Clean (JT Baker)
    - JT Baker clean for 5 min.
    - Rinse in DI water for 5 min.
    - Spin dry in N_2

15. Gate Oxide Etch
    - Etch in 10:1 BOE solution for 20 sec.
    - Rinse in DI water for 5 min.
    - Spin dry in N_2

16. Boron Diffusion
    - Boron diffusion details are covered in text

17. Deglaze
    - Deglaze steps are covered in text
    - Rinse wafers in DI water for 5 min.
    - Spin dry in N_2

18. Low Temperature Oxide (LTO) Deposition (2000 Å target)

- Load wafers in LPCVD furnace wafer flat up
- Deposit LTO (410°C, 750 mT pressure, 200 sccm O_2, 100 sccm LTO) for 34 min.

19. Contact Hole Lithography

- Spin HMDS Primer onto wafer at 4500 rpm for 40 sec.
- Spin positive photoresist (JSR 10cp) onto wafer at 4500 rpm for 40 sec.
- Pre-exposure bake on hot plate at 90°C for 1 min.
- Expose 1998 ECE 539 Contact Mask for 8 sec.
- Post-exposure bake on hot plate at 115°C for 1 min.
- Develop for 1 min.
- Rinse wafers in DI water for 5 min.
- Spin dry in N_2
- Post-develop bake on hot plate at 115°C for 5 min.

20. Descum

- Standard descum plasma etch using the March Instruments Asher (80 sccm O_2, 600 mT pressure) for 3 min.

21. Contact Hole Etch

- Etch in 10:1 BOE solution for 58 sec. (until backside of wafer dewets)
- Rinse in DI water for 5 min.
- Spin dry in N_2

22. Photoresist Removal

- 10 min. in Nanostrip bath #1
- 5 min. in Nanostrip bath #2
- 5 min. rinse
- Spin dry in N_2

23. Back Door Etch

- Etch in dilute BOE solution for 5 min.
- Rinse in DI water for 5 min.
- Spin dry in N_2

24. Frontside Metal Deposition

- 500 Å titanium evaporation
- 2000 Å aluminum evaporation

25. Metal Mask Lithography

- Spin HMDS Primer onto wafer at 4500 rpm for 40 sec.
- Spin positive photoresist (JSR 10cp) onto wafer at 4500 rpm for 40 sec.
- Pre-exposure bake on hot plate at 90°C for 1 min.
- Expose 1998 ECE 539 Metal Mask for 8 sec.
- Post-exposure bake on hot plate at 115°C for 1 min.
- Develop for 1 min.
- Rinse wafers in DI water for 5 min.
- Spin dry in N_2
- Post-develop bake on hot plate at 115°C for 5 min.

26. Metal Etch

- Etch in heated bath of aluminum etch solution (wafers visually monitored during etch to determine etch endpoint)
- Rinse in DI water for 5 min.
- Spin dry in N_2
- Etch in titanium etch solution (wafers visually monitored during etch to determine etch endpoint)
- Rinse in DI water for 5 min.
- Spin dry in N_2

27. Photoresist Removal

- 5 min. in Accustrip bath #1
- 5 min. in Accustrip bath #2
- Rinse wafers in DI water for 10 min.
- Spin dry wafers in N_2

28. Backside Metal Deposition

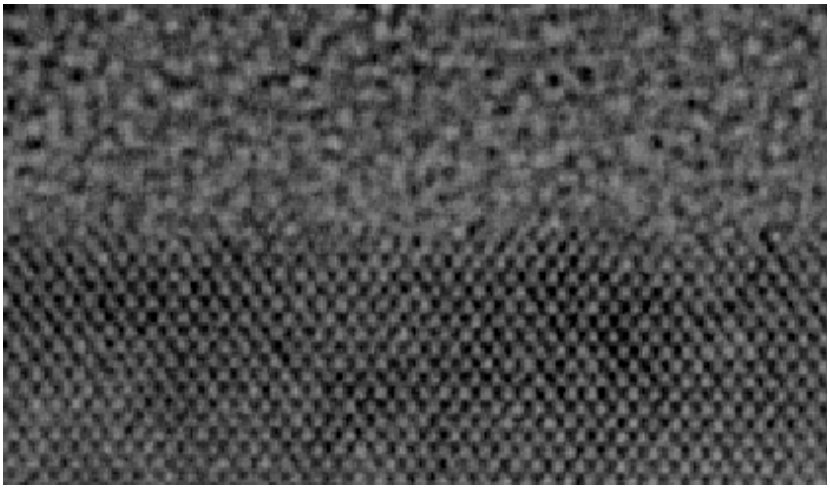
- 2000 Å aluminum evaporation

29. Forming Gas Anneal

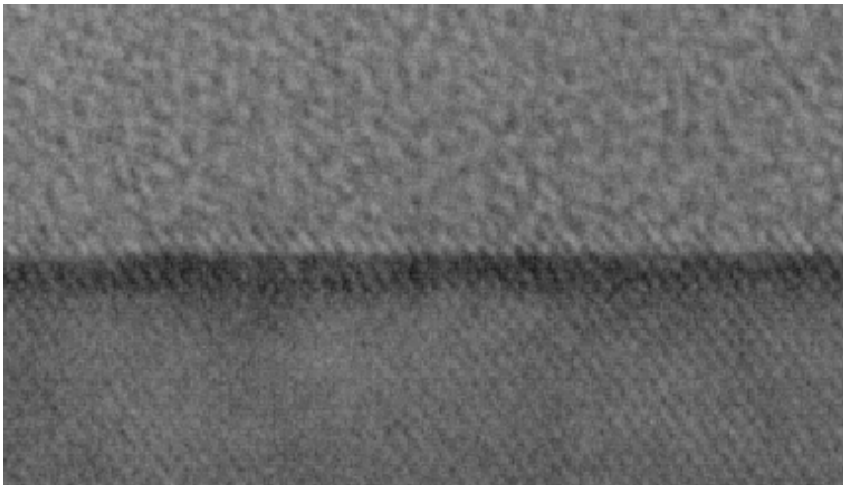
- Boat out silica boat
- Load wafers in silica boat
- Boat in silica boat in 7200 sccm N_2 (10 min.)
- Ramp up furnace temperature to 400°C (20 min.)
- Anneal in 10:1 N_2/H_2 (30 min.)
- Cool down furnace in 7200 sccm N_2 (10 min.)
- Boat out wafers (10 min.)

APPENDIX B

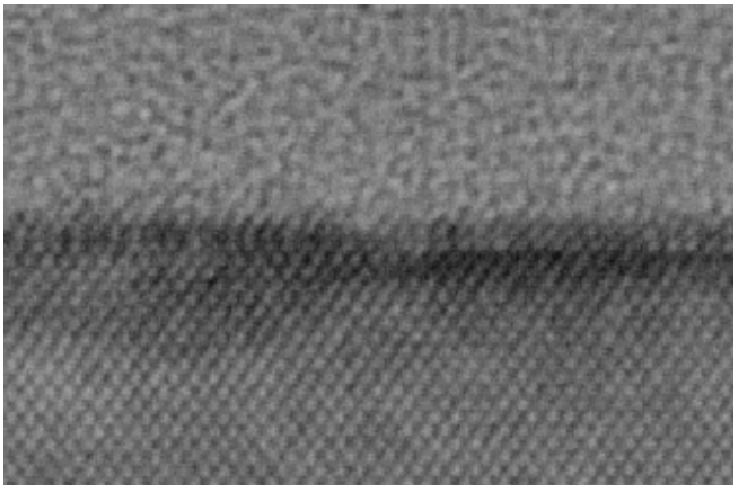
TEM Images



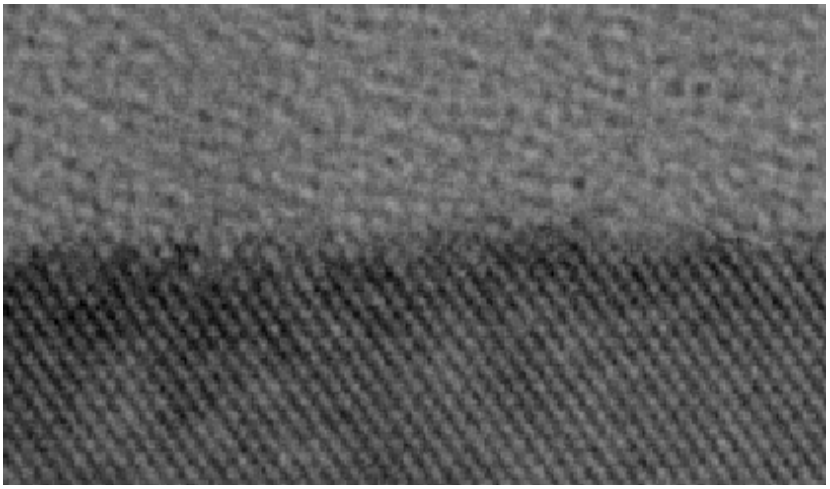
Cross-Sectional TEM Image for Sample A1 (800°C/45 min./N_2)



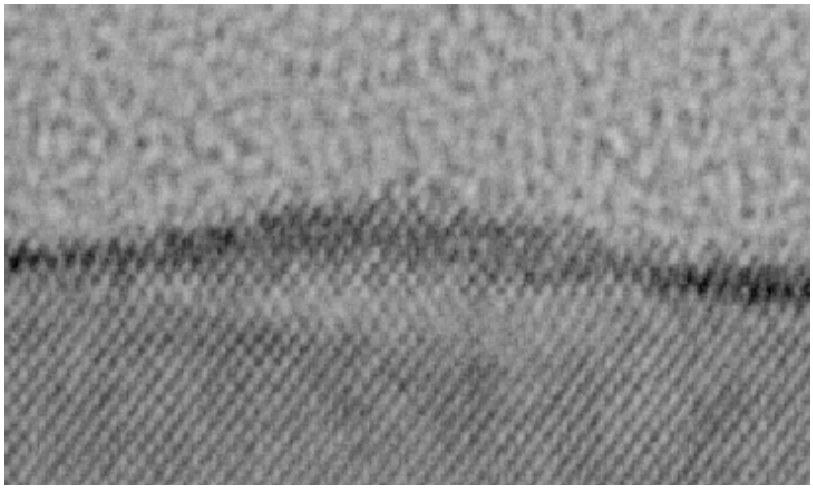
Cross-Sectional TEM Image for Sample A2 (800°C/45 min./N_2O_2)



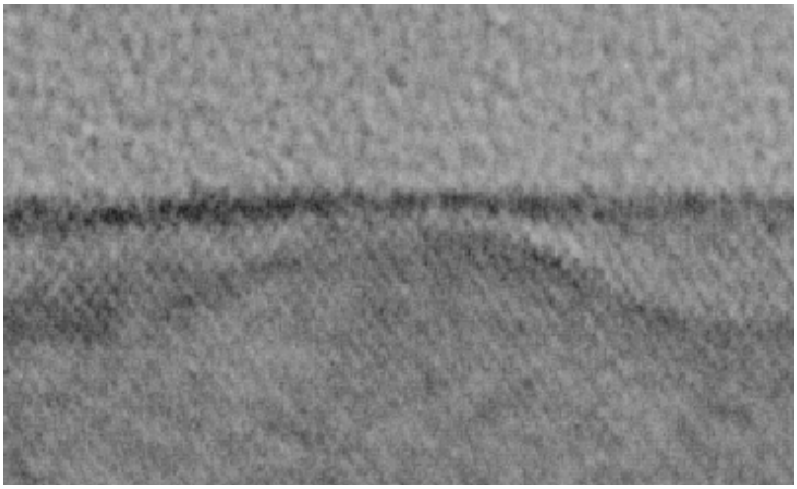
Cross-Sectional TEM Image for Sample B7 (900°C/10 min./N_2)



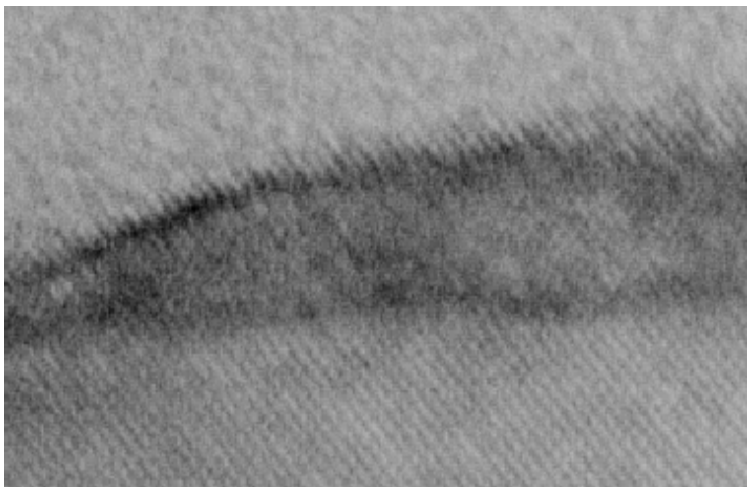
Cross-Sectional TEM Image for Sample B5 (900°C/30 min./N_2)



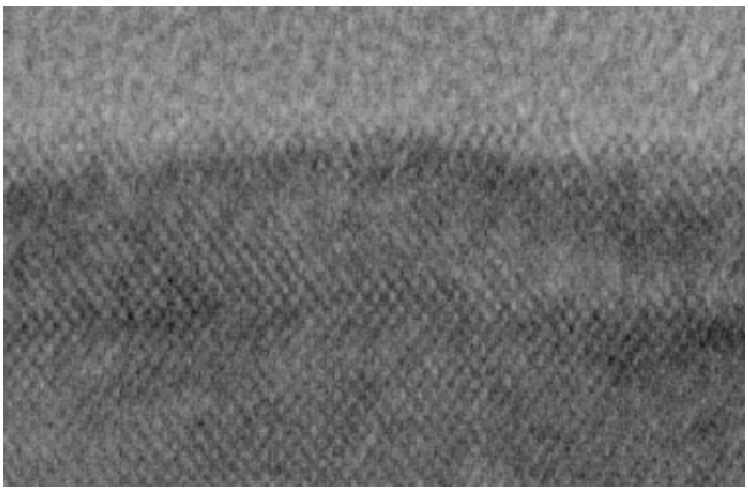
Cross-Sectional TEM Image for Sample B1 (900°C/60 min./N_2)



Cross-Sectional TEM Image for Sample B4 (900°C/30 min./N_2O_2)



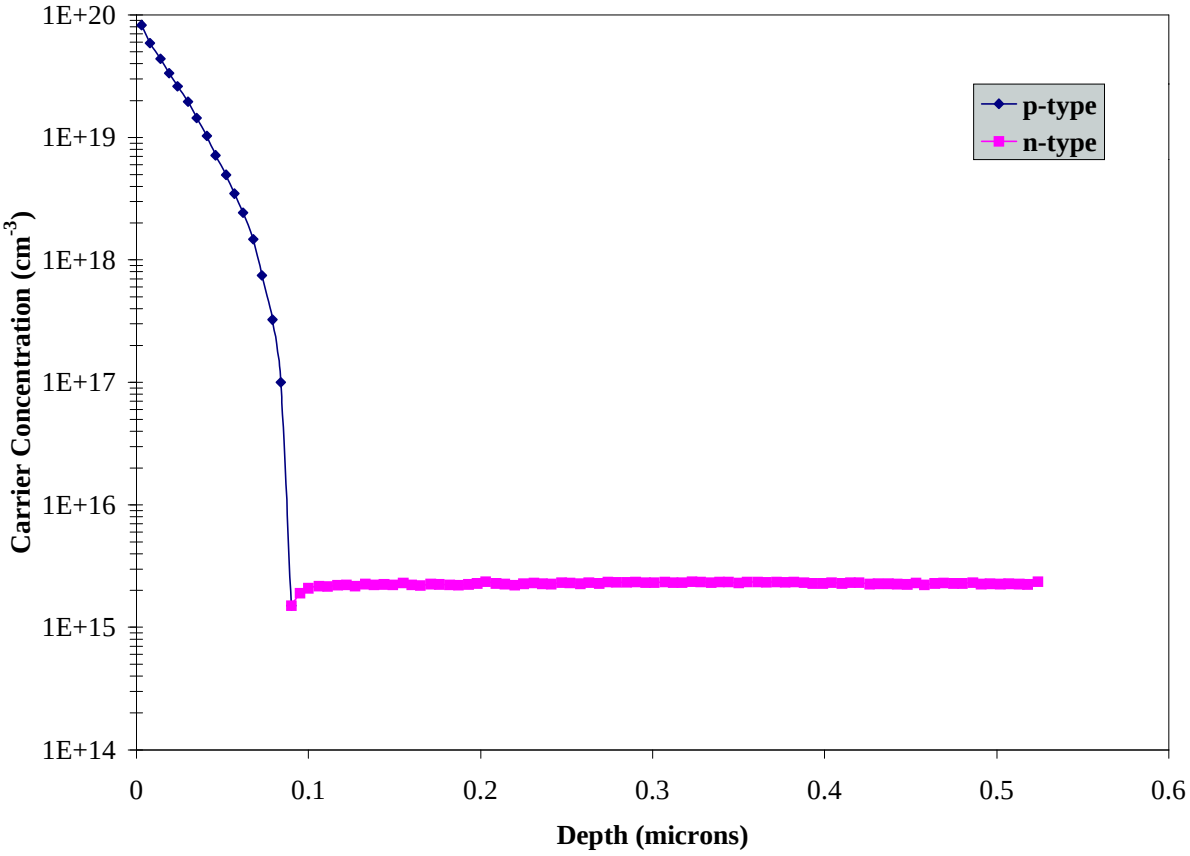
Cross-Sectional TEM Image for Sample C1 (1000°C/45 min./N_2)



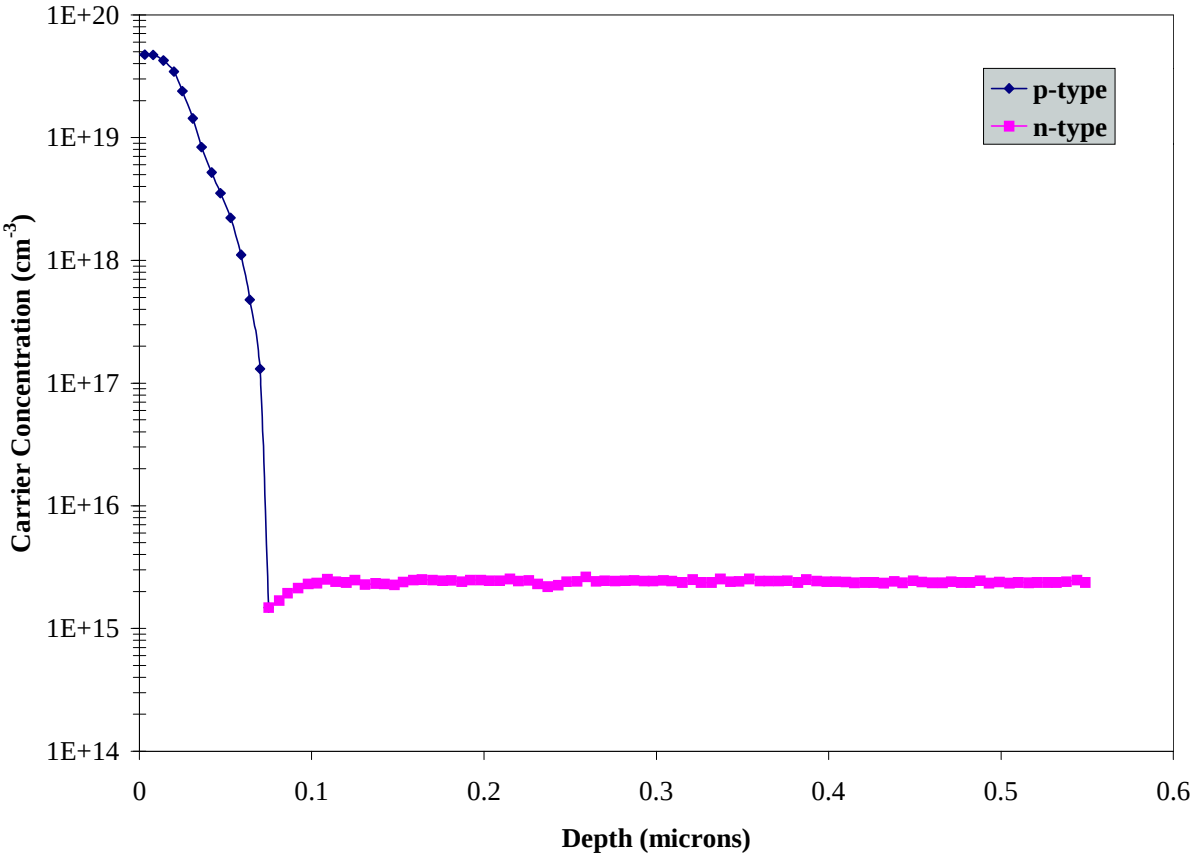
Cross-Sectional TEM Image for Sample C2 (1000°C/45 min./N_2O_2)

APPENDIX C

Spreading Resistance Profiles



SRA Profile for Wafer A1 (800°C/45 min./N_2)



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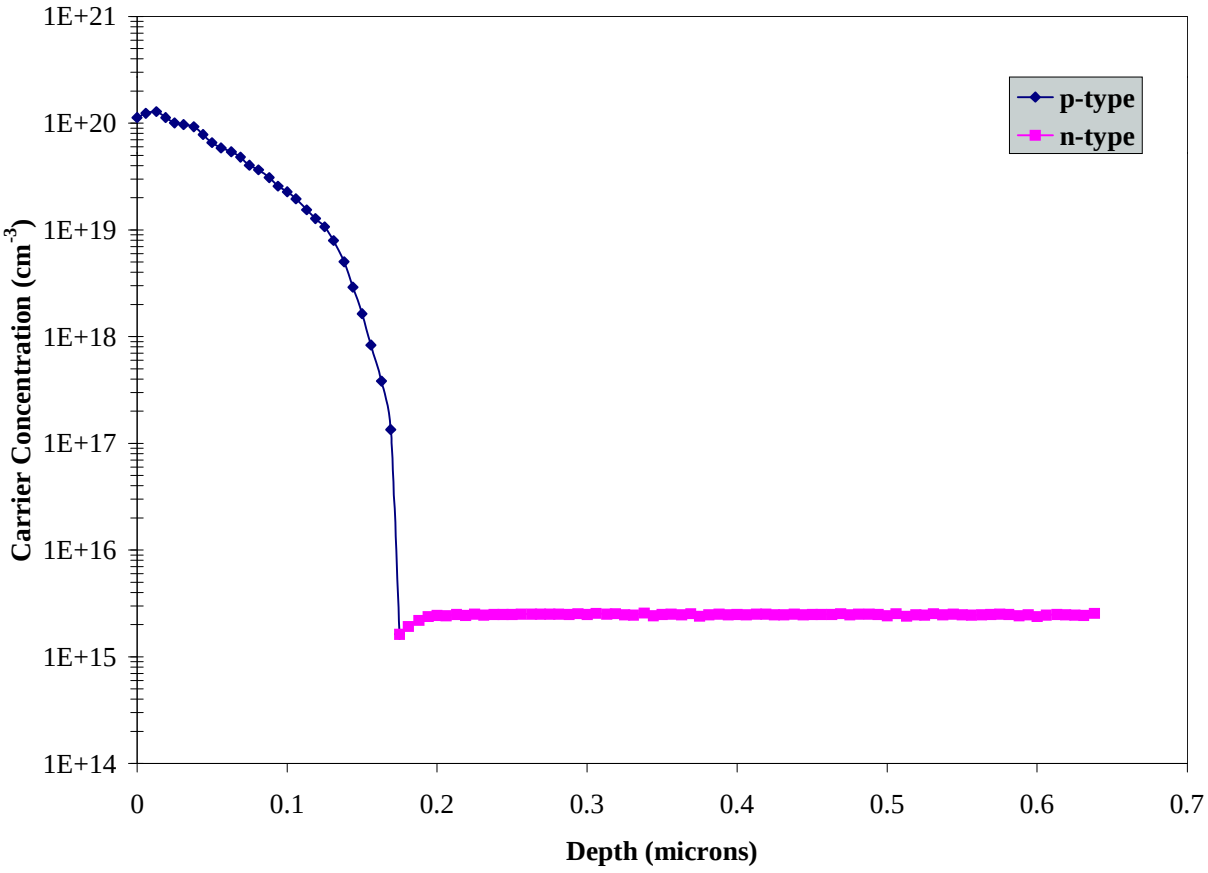
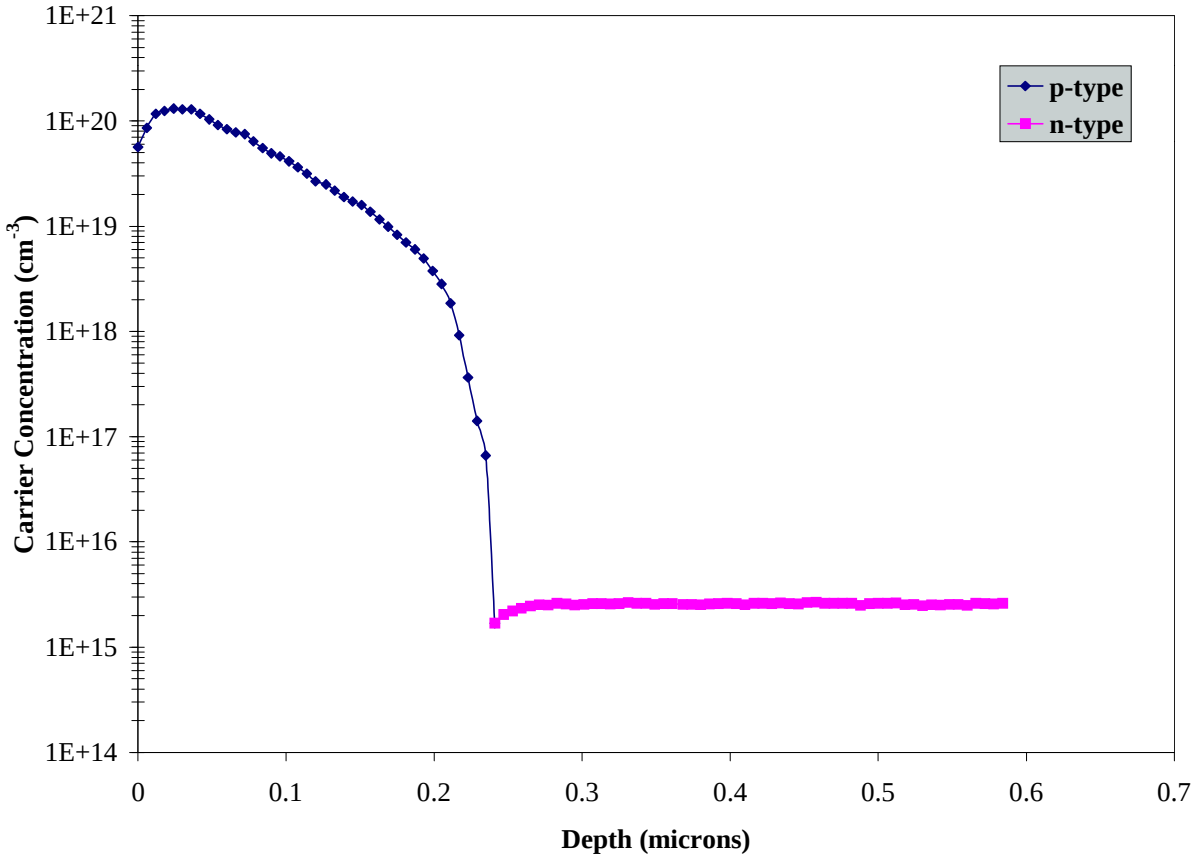
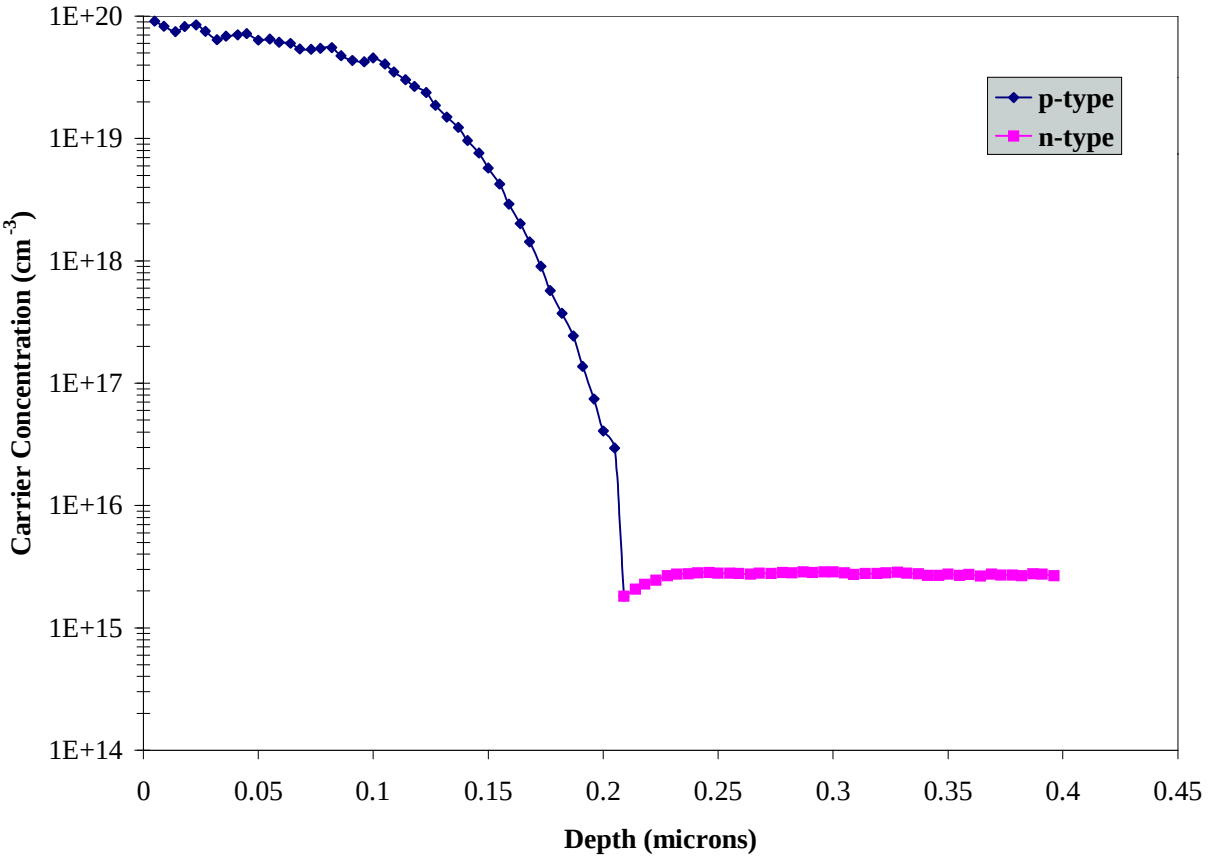


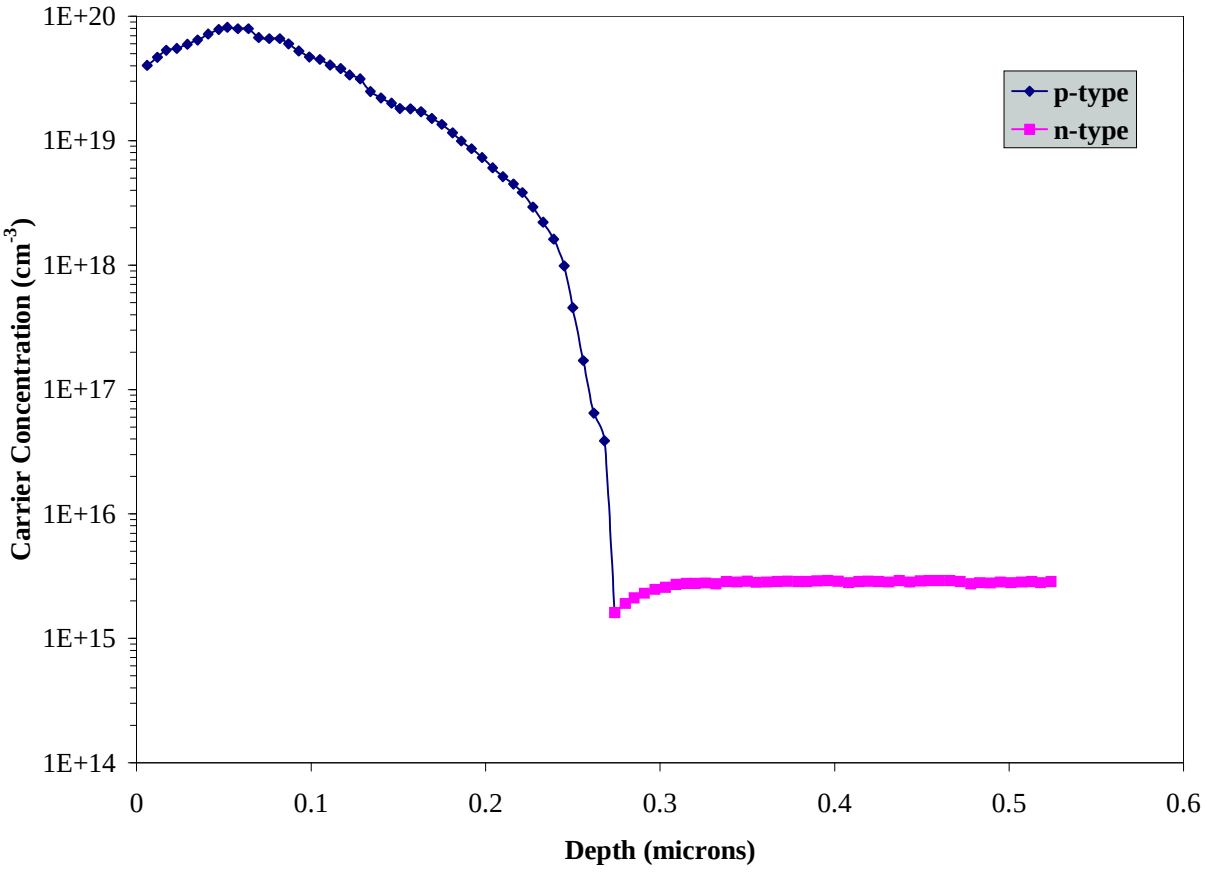
SRA Profile for Wafer B7 (900°C/10 min./N_2)



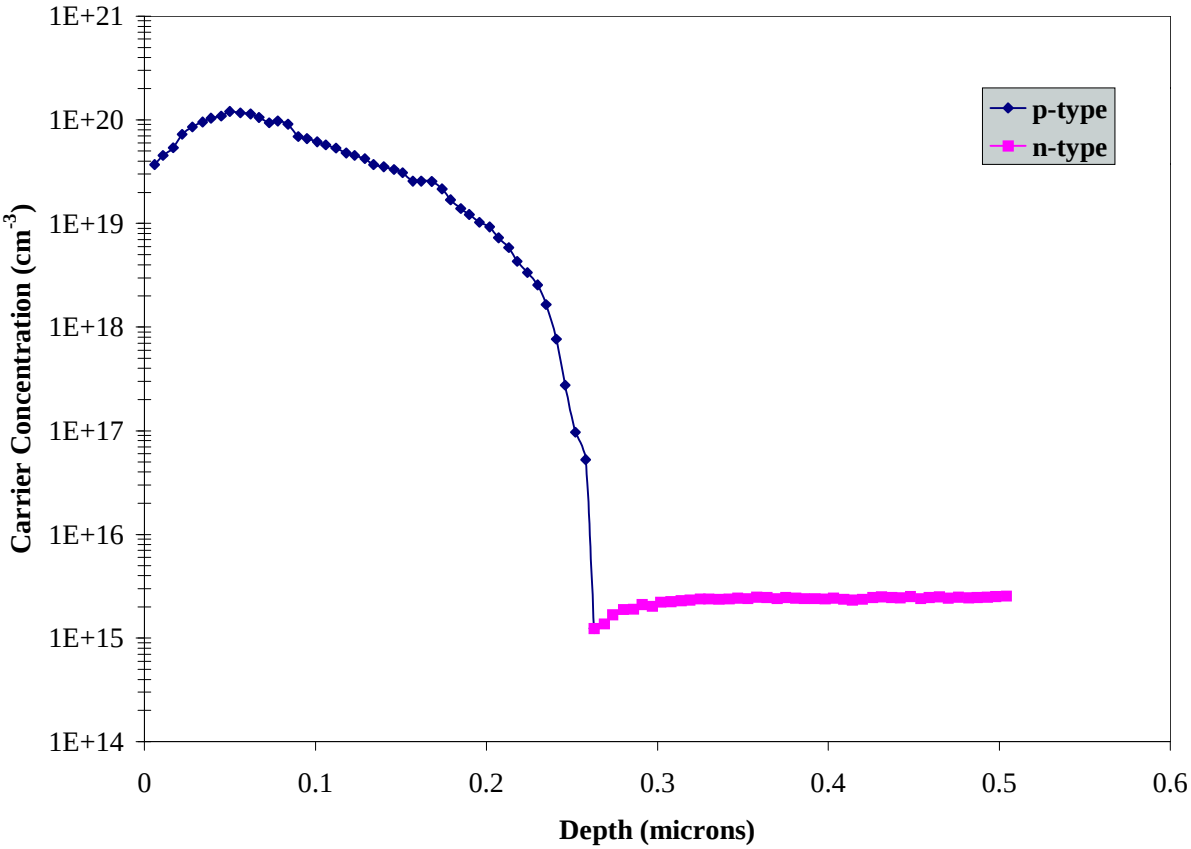
SRA Profile for Wafer B8 (900°C/10 min./N_2O_2)



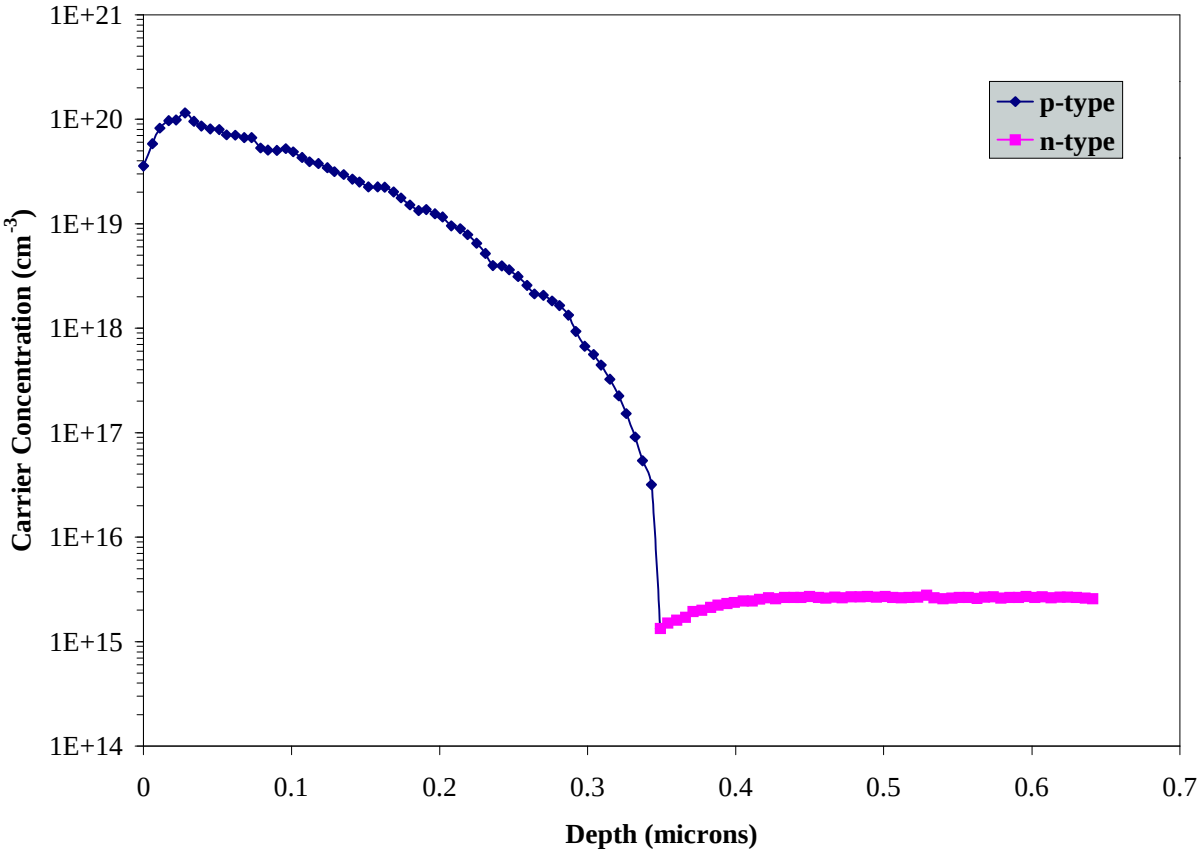
SRA Profile for Wafer B5 (900°C/30 min./N_2)



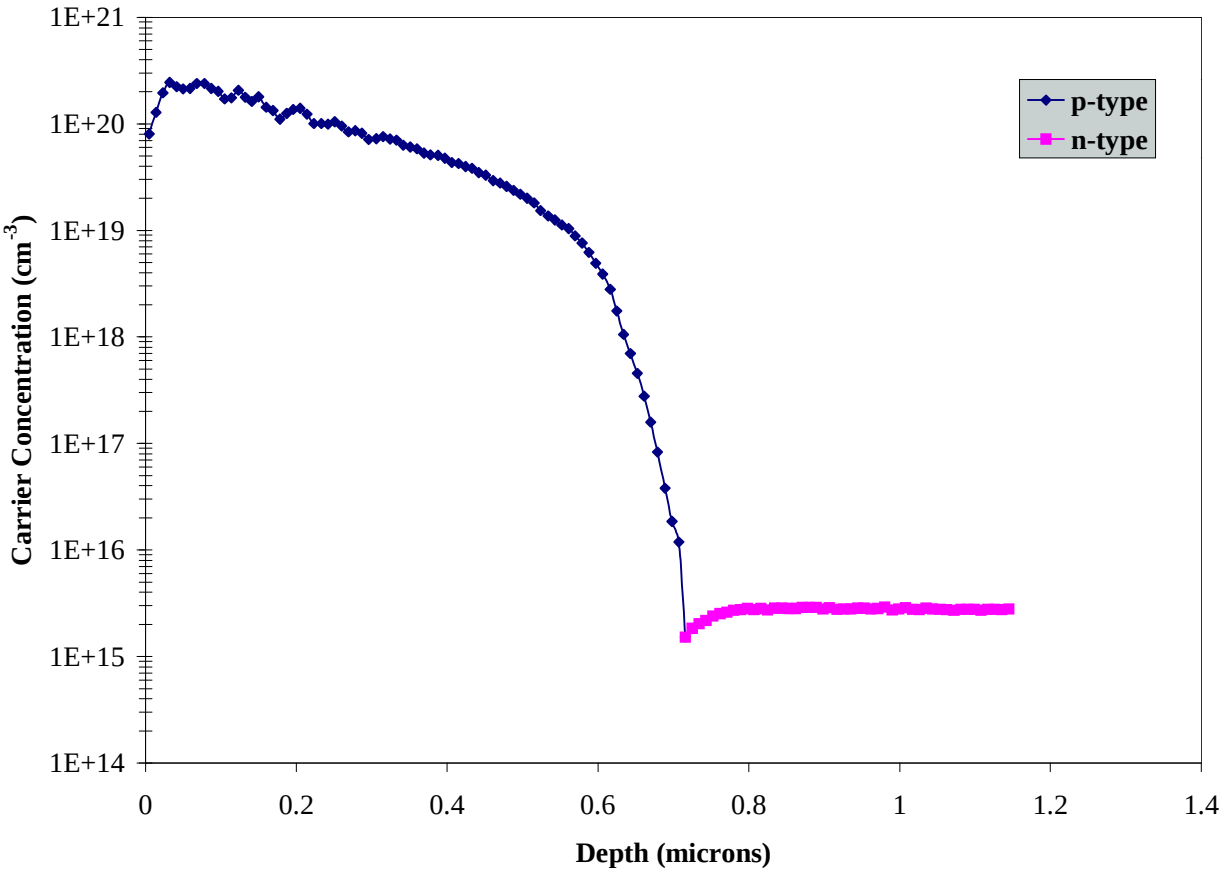
SRA Profile for Wafer B4 (900°C/30 min/N_2O_2)



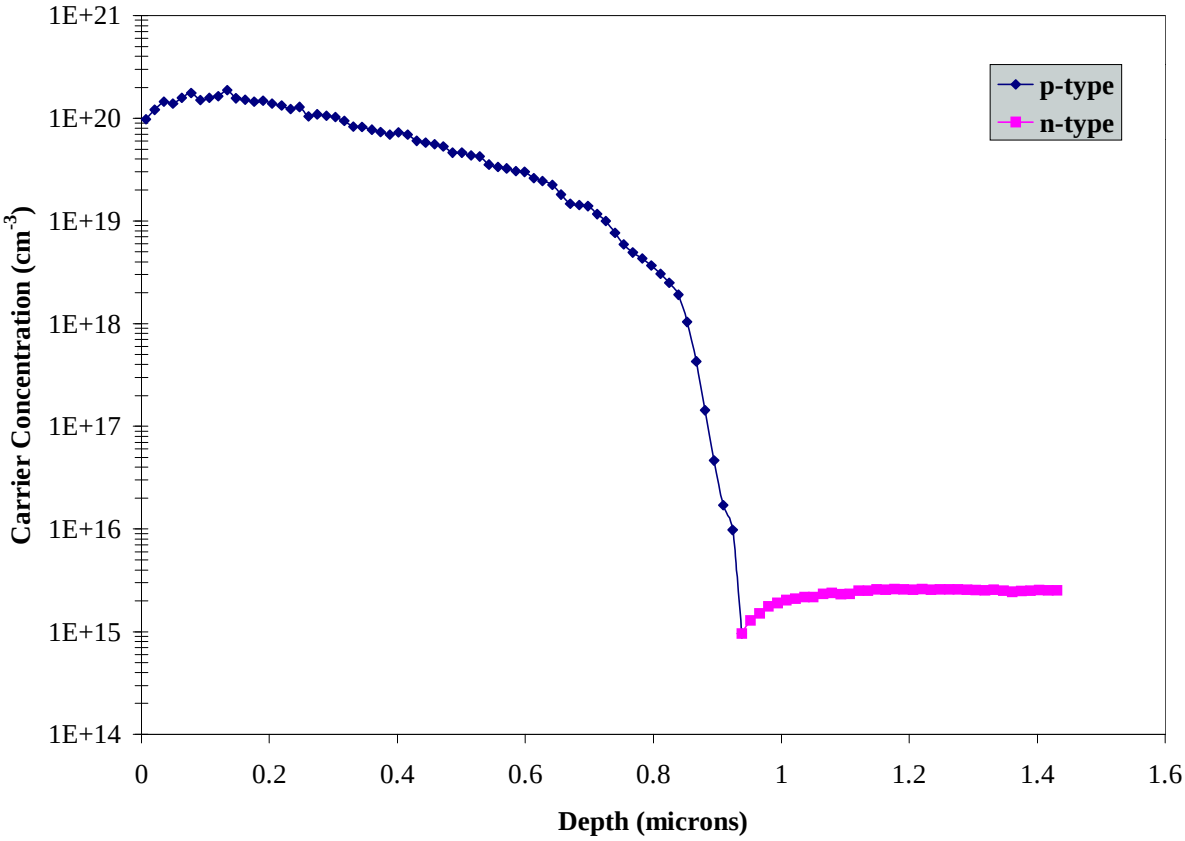
SRA Profile for Wafer B1 (900°C/60 min./N_2)



SRA Profile for Wafer B2 (900°C/60 min./N_2O_2)



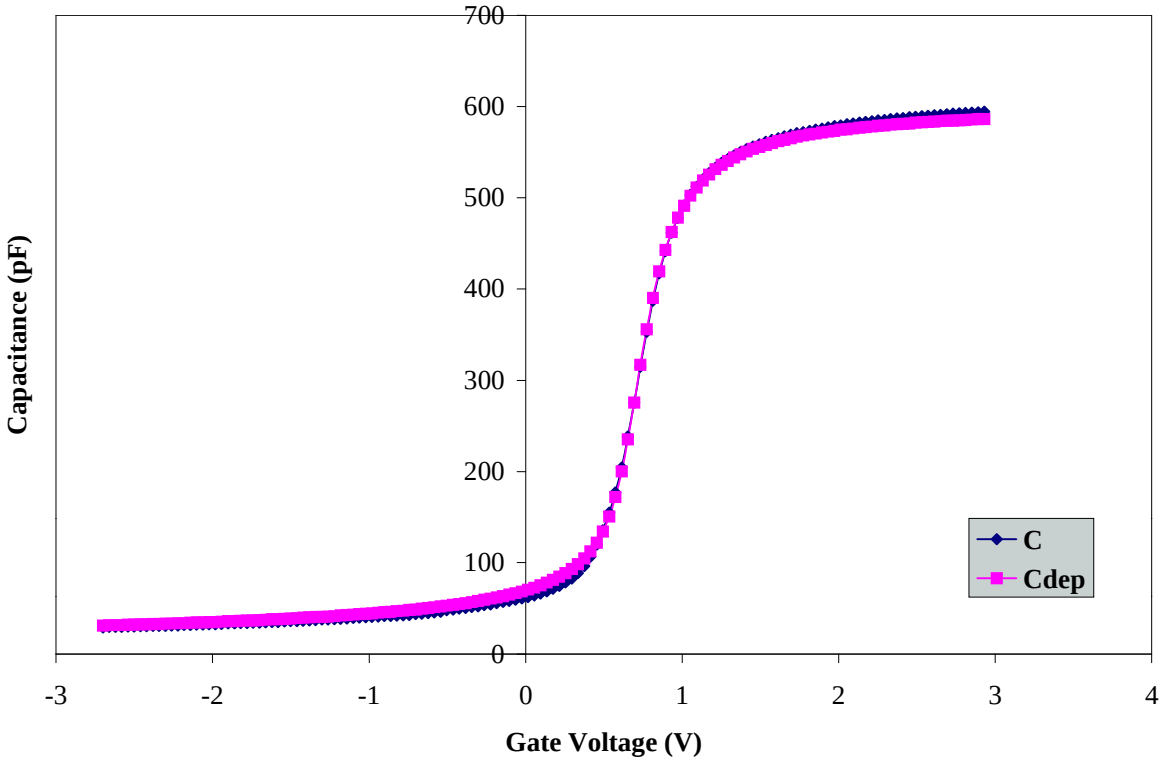
SRA Profile for Wafer C1 (1000°C/45 min./N_2)



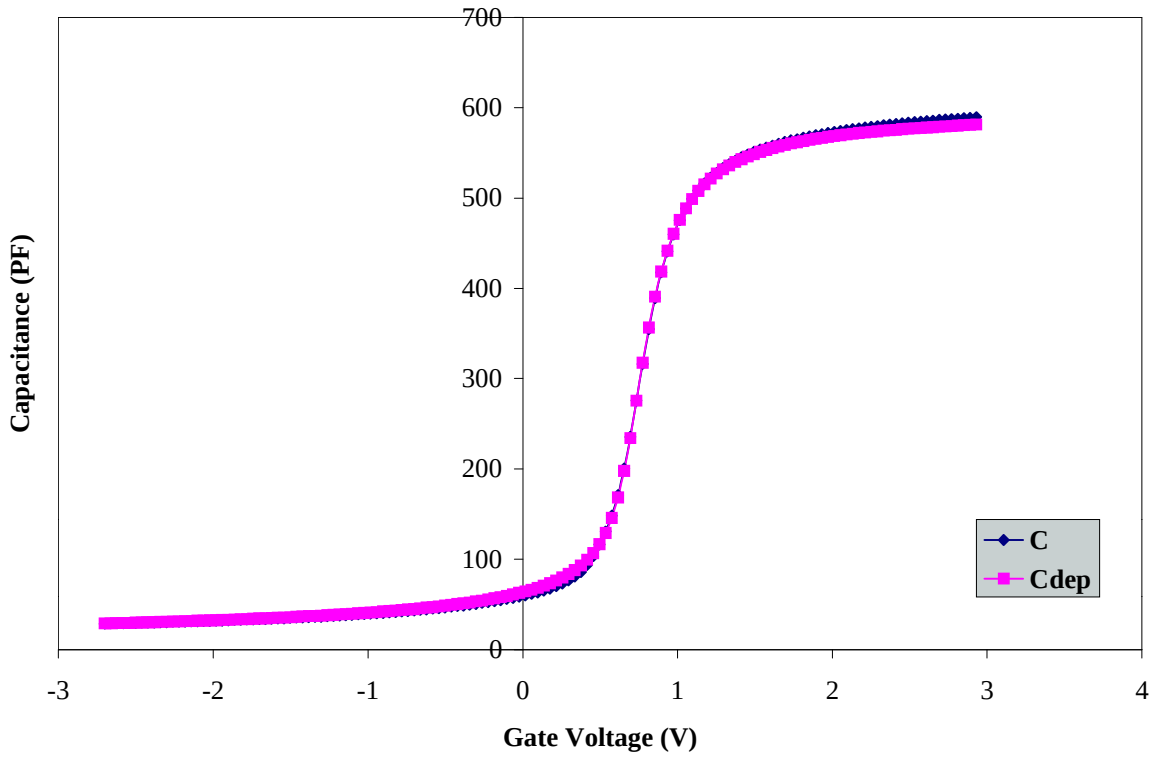
SRA Profile for Wafer C2 (1000°C/45 min./N_2O_2)

APPENDIX D

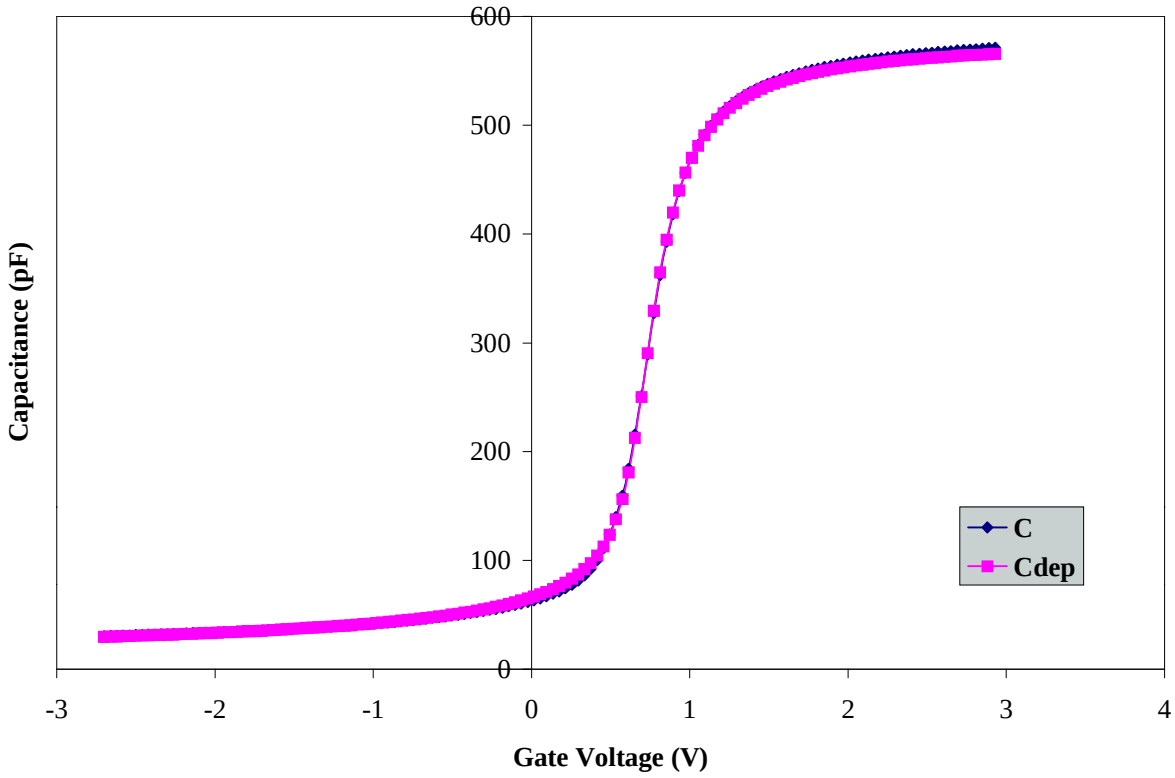
Capacitance-Voltage Curves



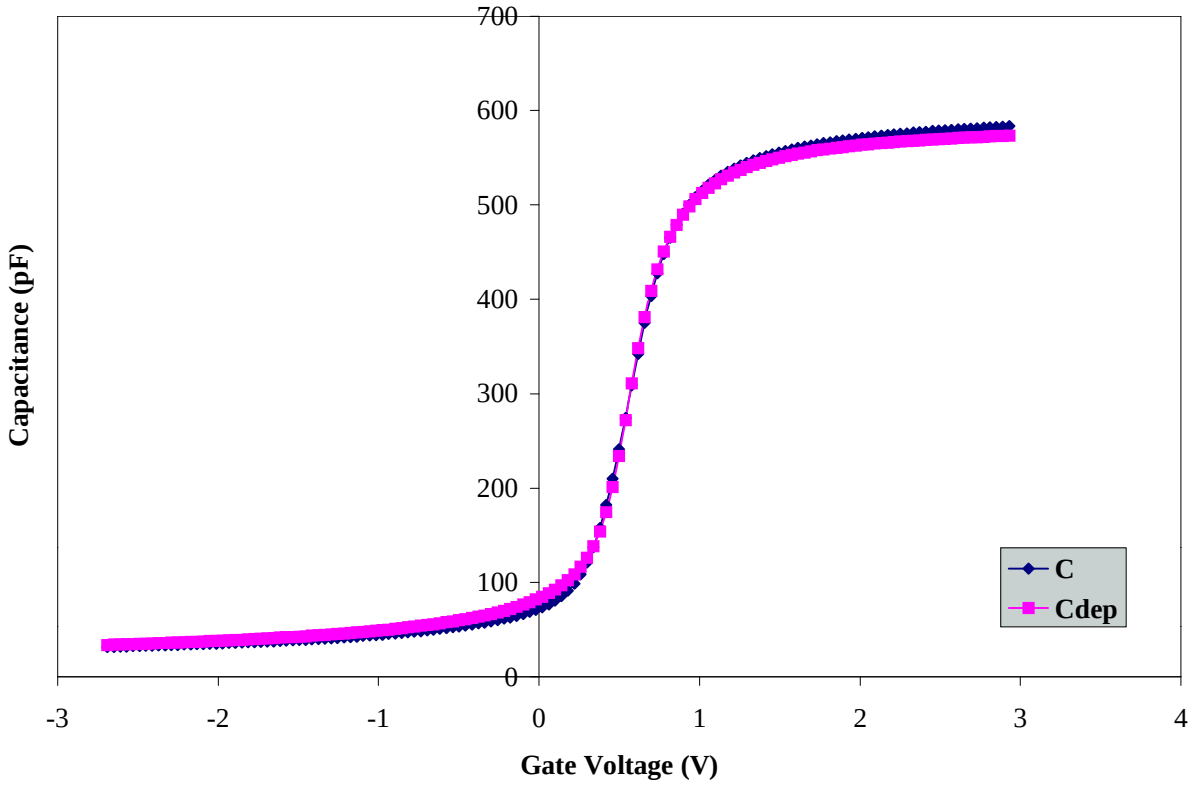
High Frequency CV Curve for Wafer A3 (800°C/20 min./N_2)



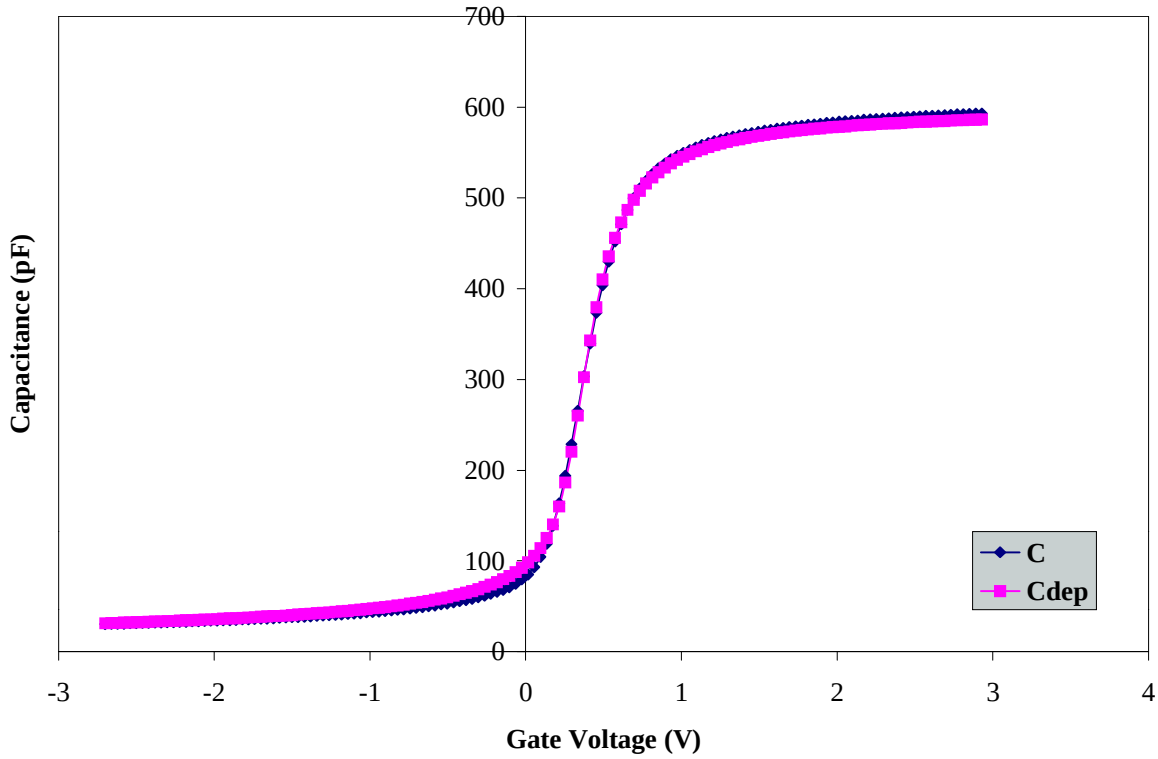
High Frequency CV Curve for Wafer A4 (800°C/20 min./N_2O_2)



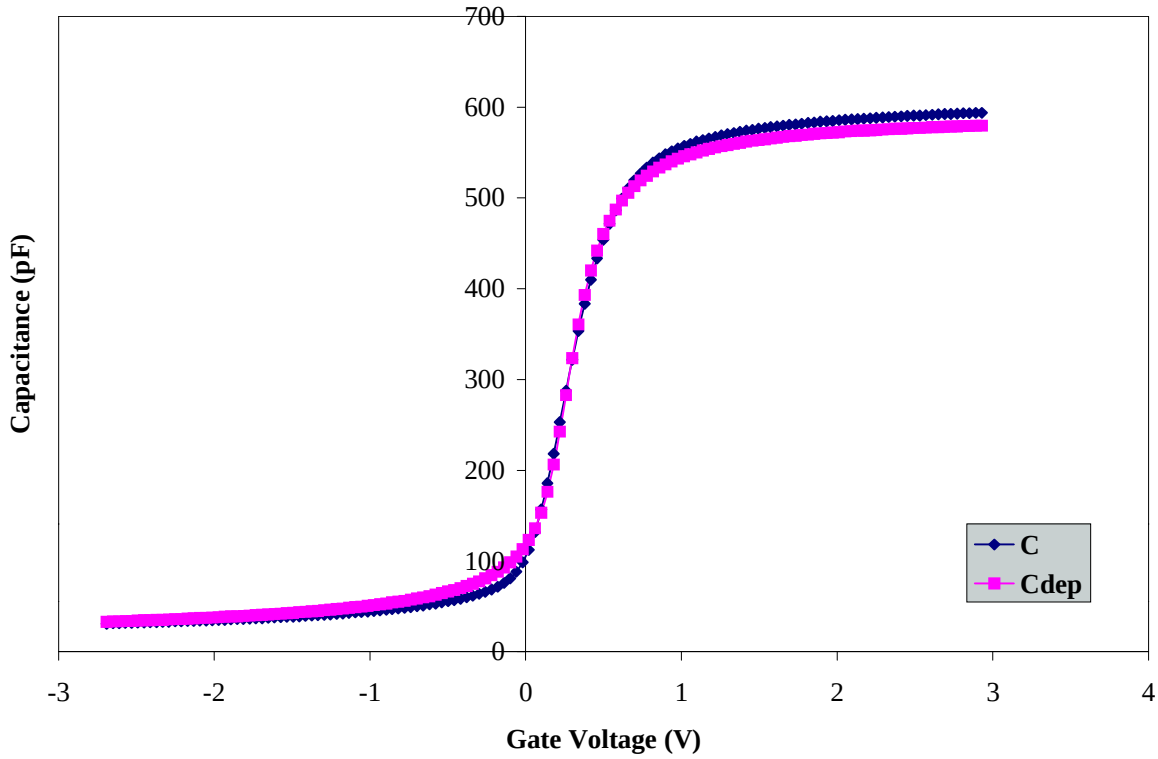
High Frequency CV Curve for Wafer A1 (800°C/45 min./N_2)



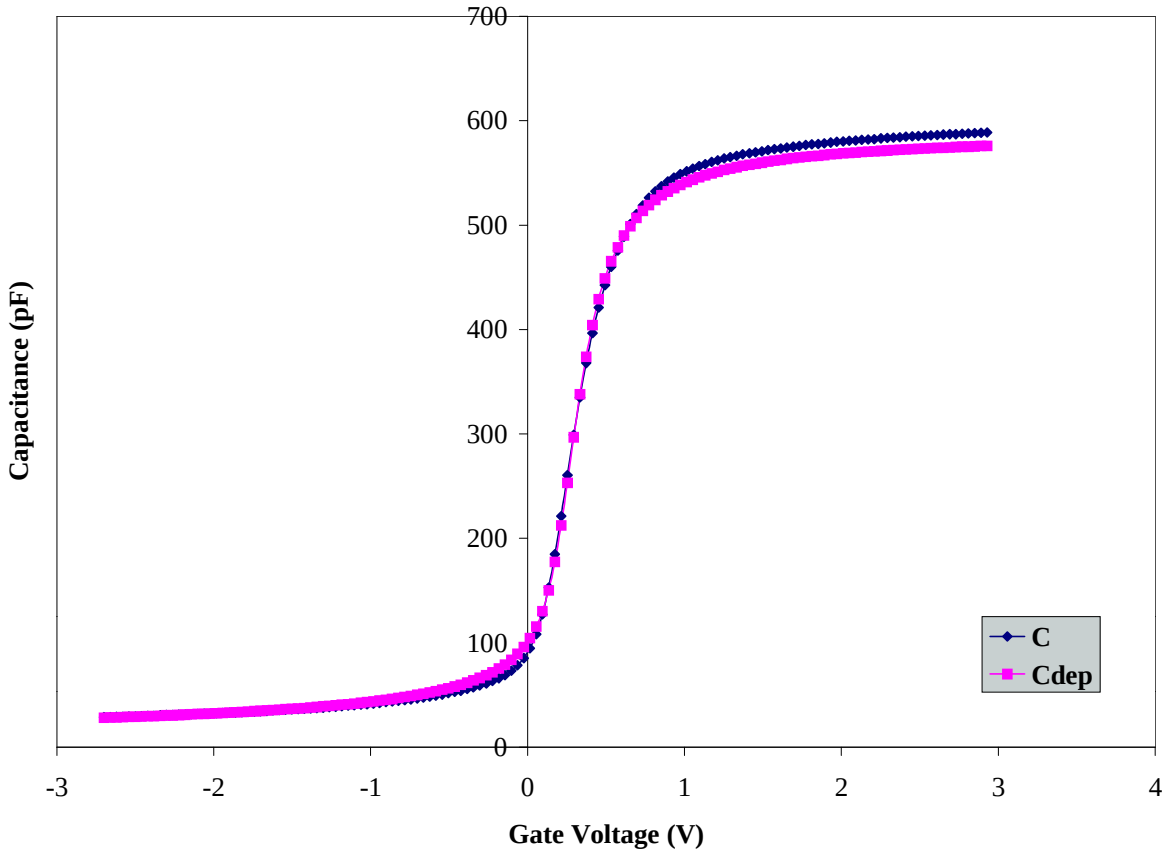
High Frequency CV Curve for Wafer A2 (800°C/45 min./N_2O_2)



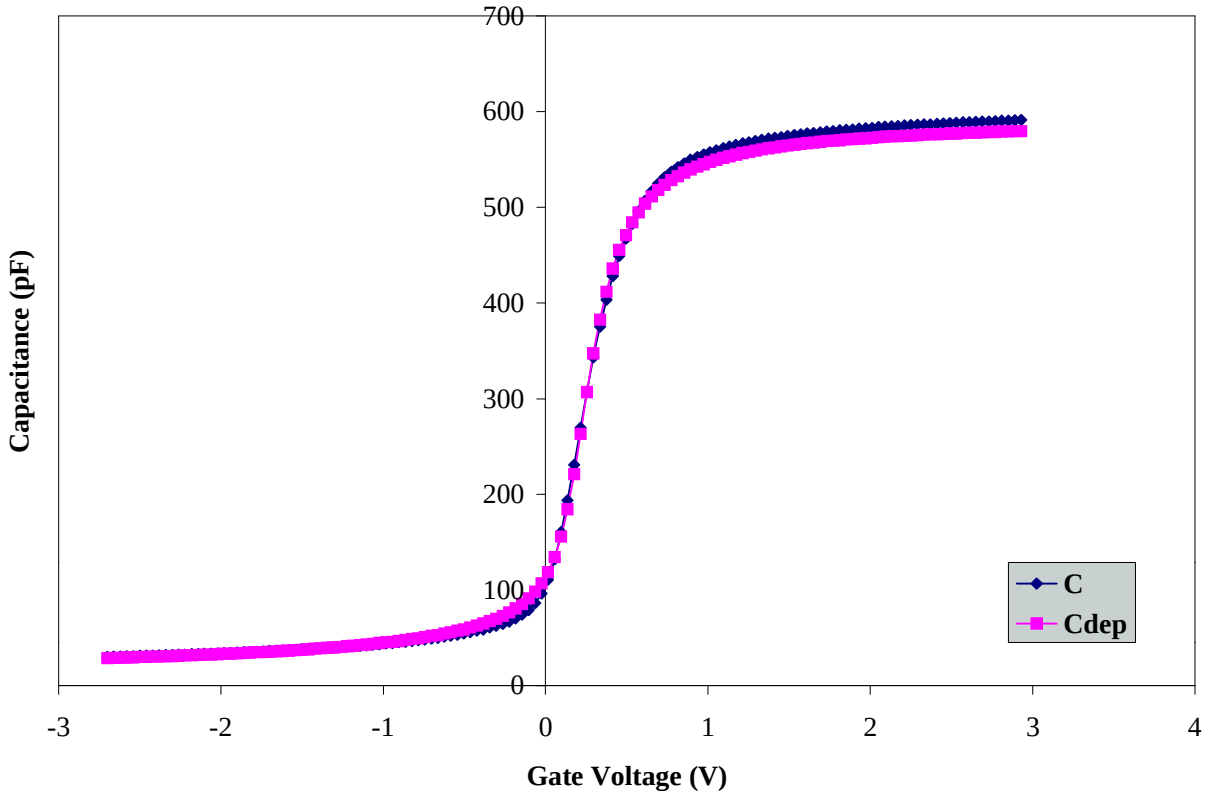
High Frequency CV Curve for Wafer B7 (900°C/10 min./N_2)



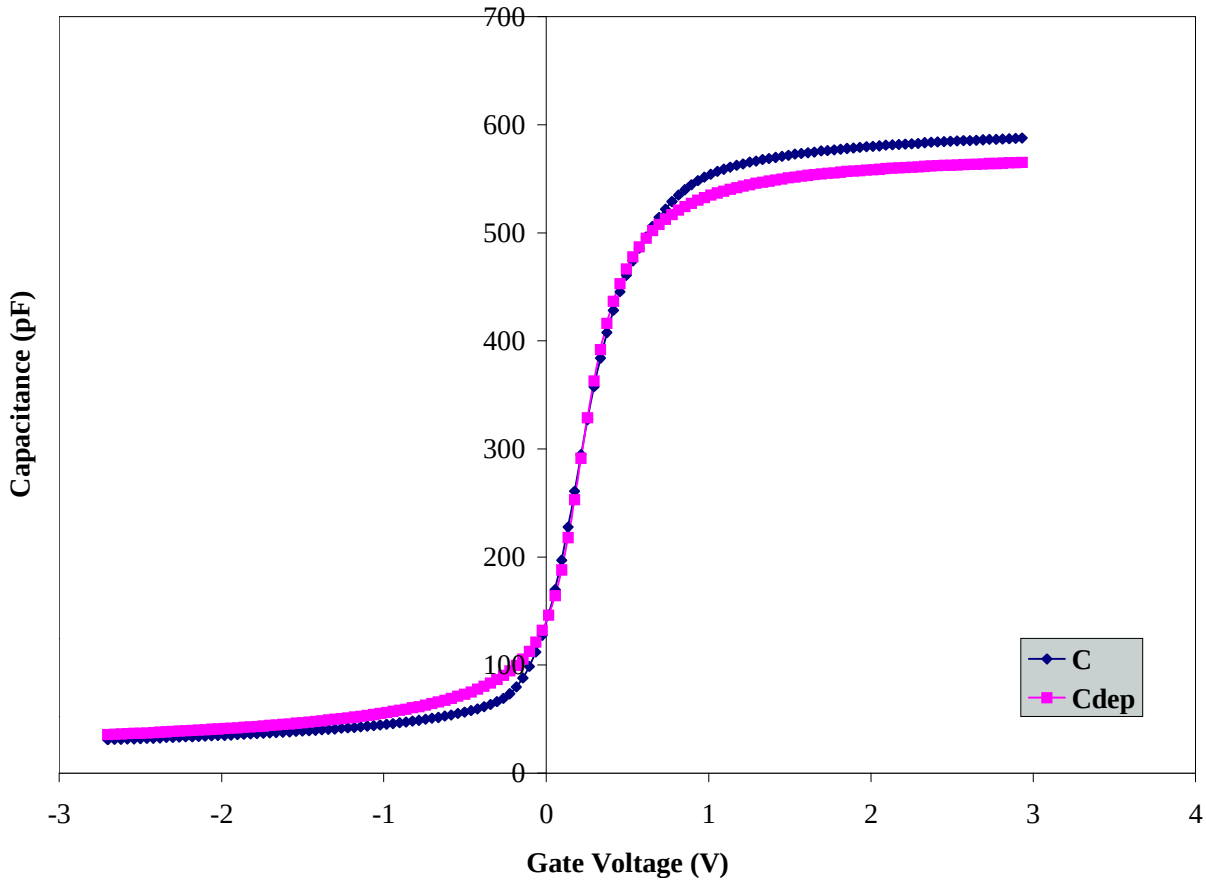
High Frequency CV Curve for Wafer B8 (900°C/10 min./N_2O_2)



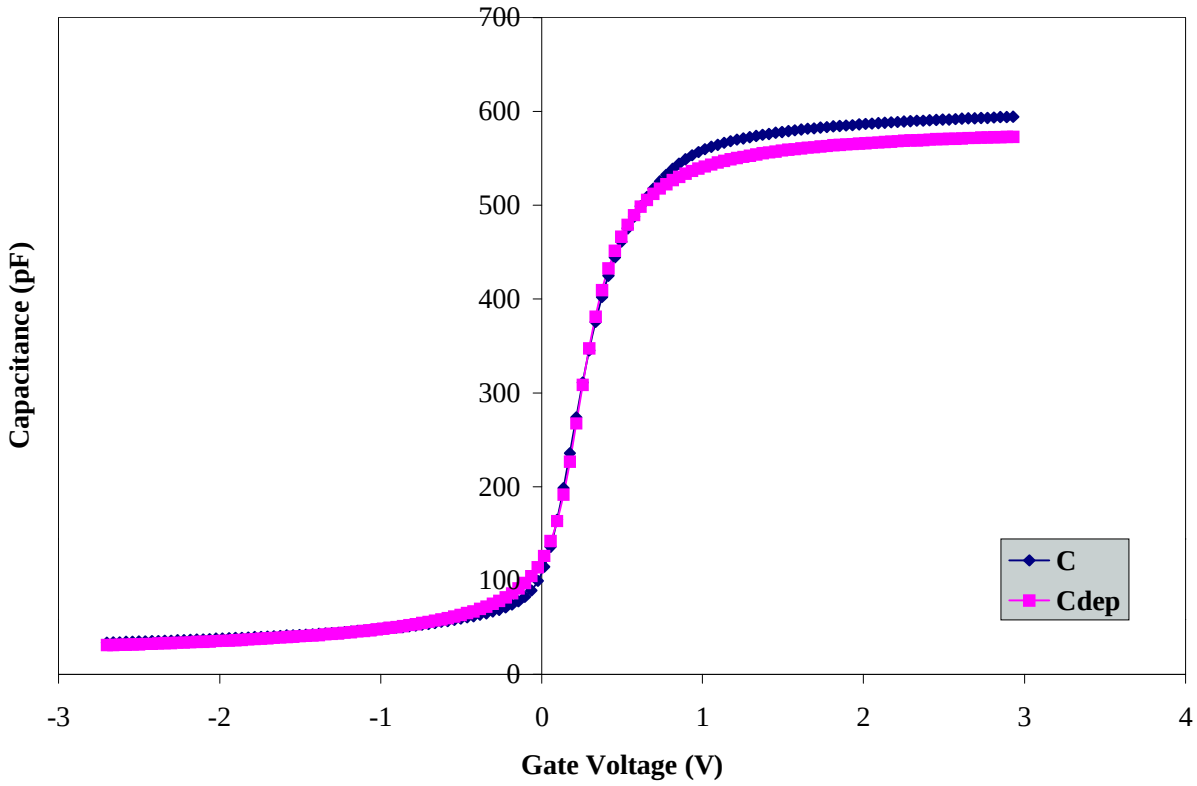
High Frequency CV Curve for Wafer B5 (900°C/30 min./N_2)



High Frequency CV Curve for Wafer B4 (900°C/30 min/N_2O_2)



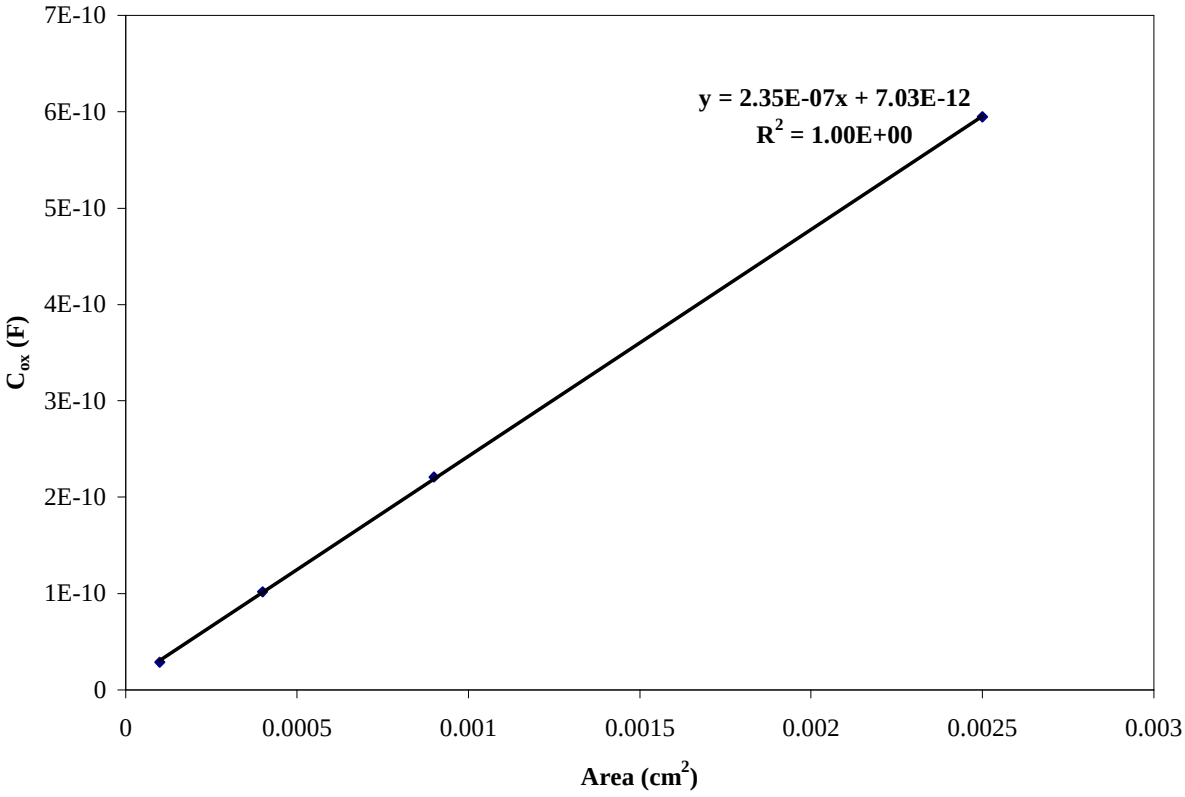
High Frequency CV Curve for Wafer B1 (900°C/60 min./N_2)



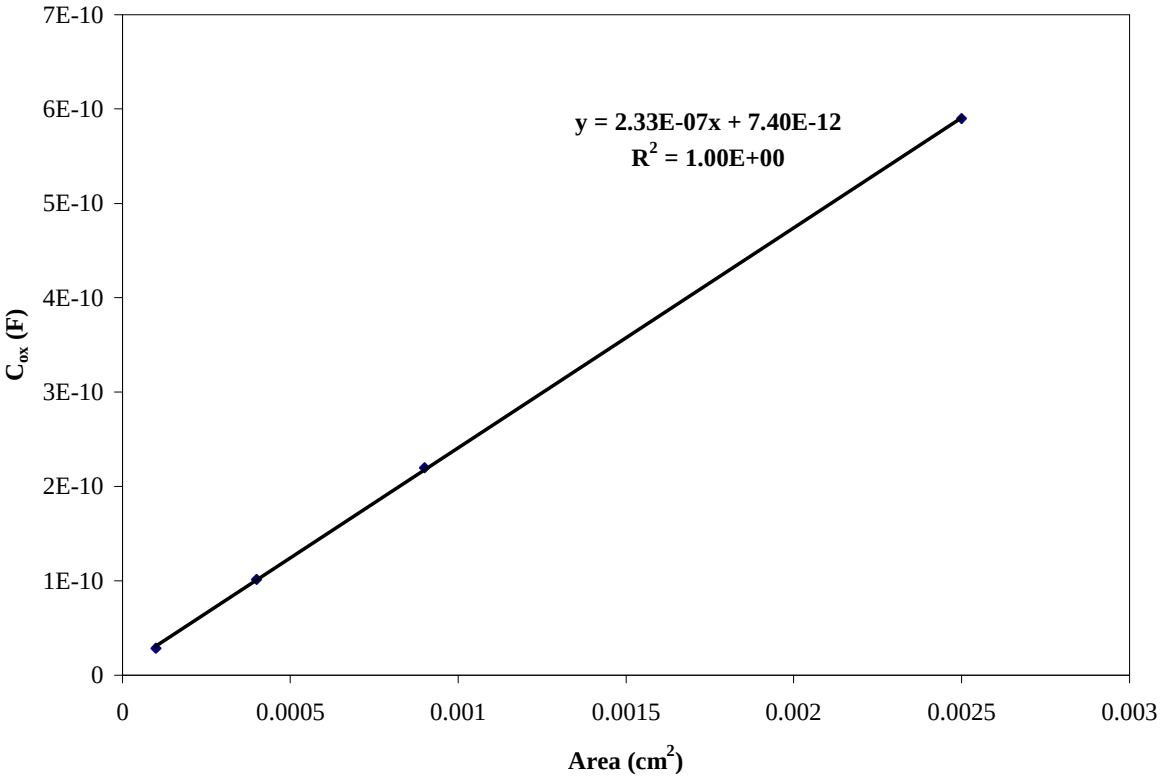
High Frequency CV Curve for Wafer B2 (900°C/60 min./N_2O_2)

APPENDIX E

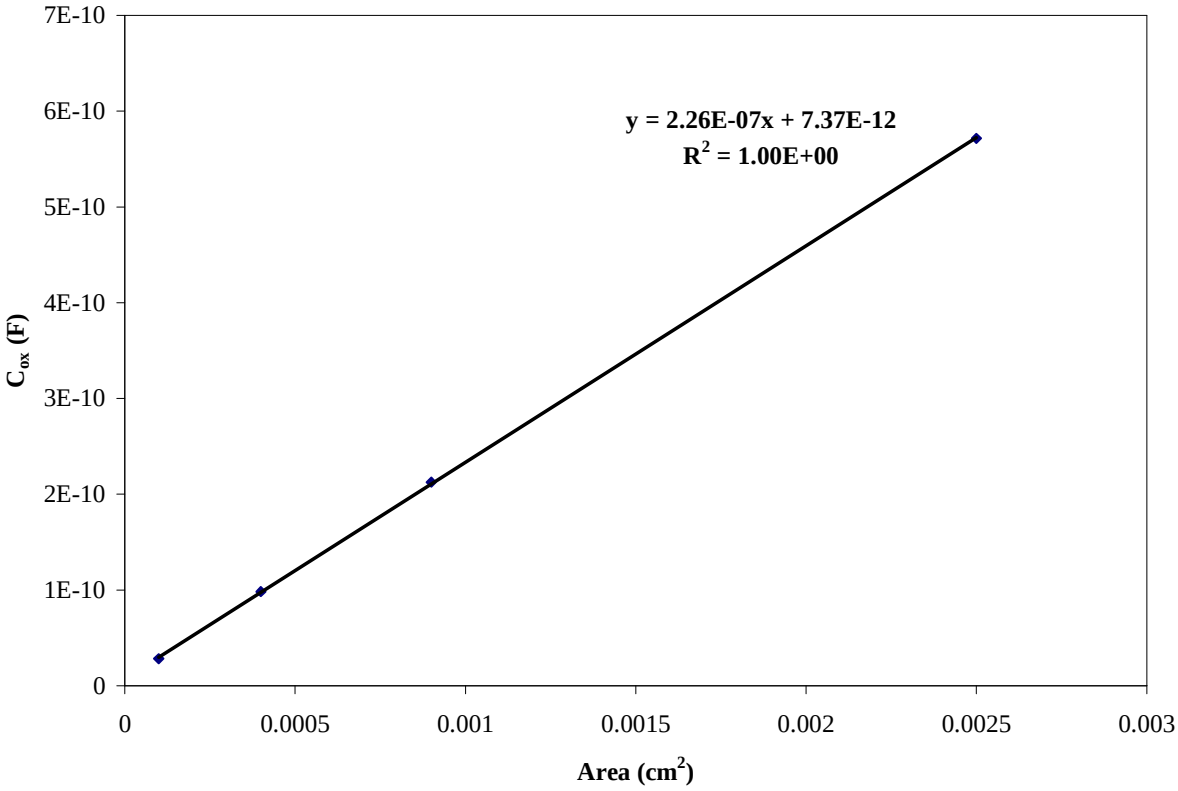
Oxide Capacitance vs. Capacitor Area Plots



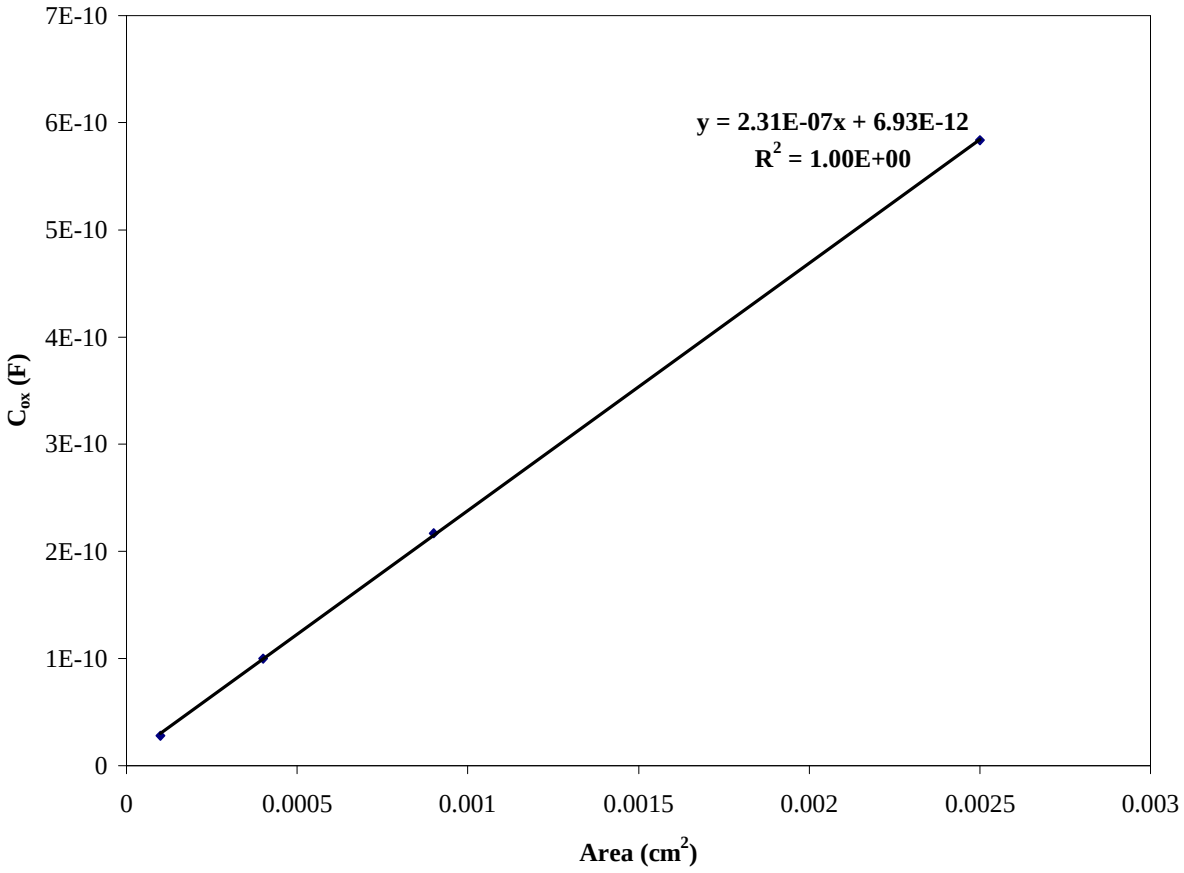
C_{ox} vs. Capacitor Area Plot for Wafer A3 (800°C/20 min./N_2)



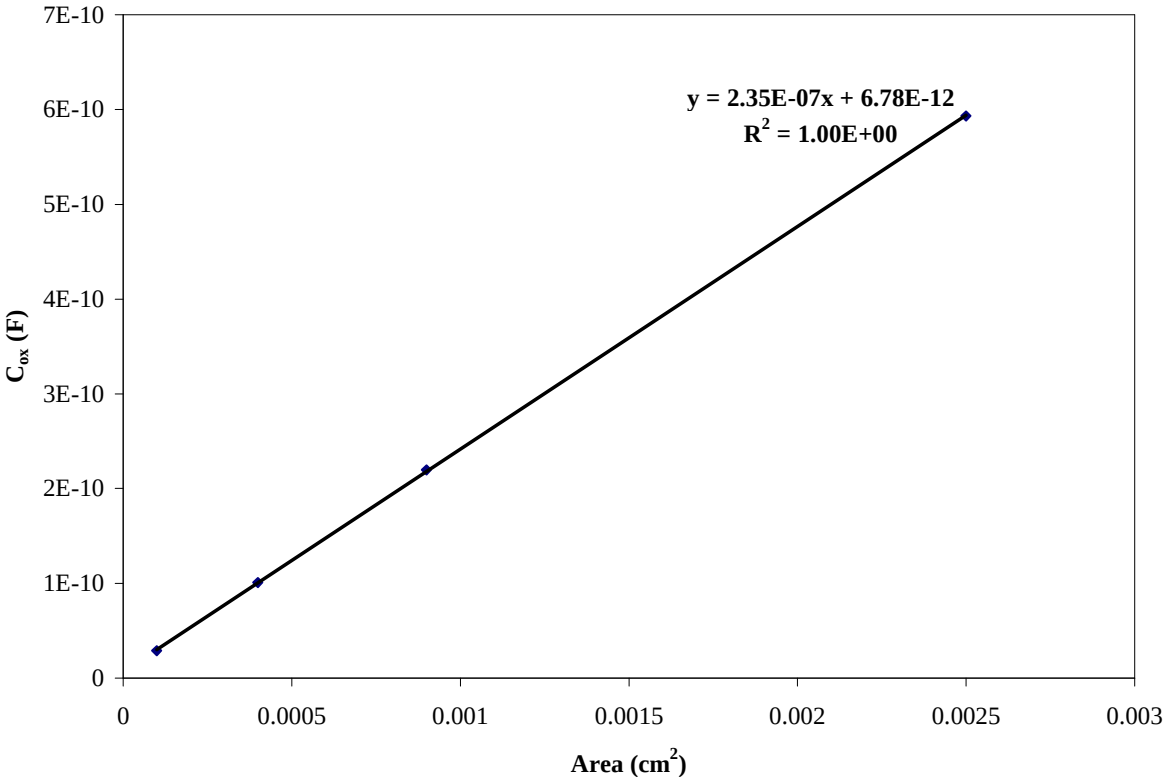
C_{ox} vs. Capacitor Area Plot for Wafer A4 (800°C/20 min./N_2O_2)



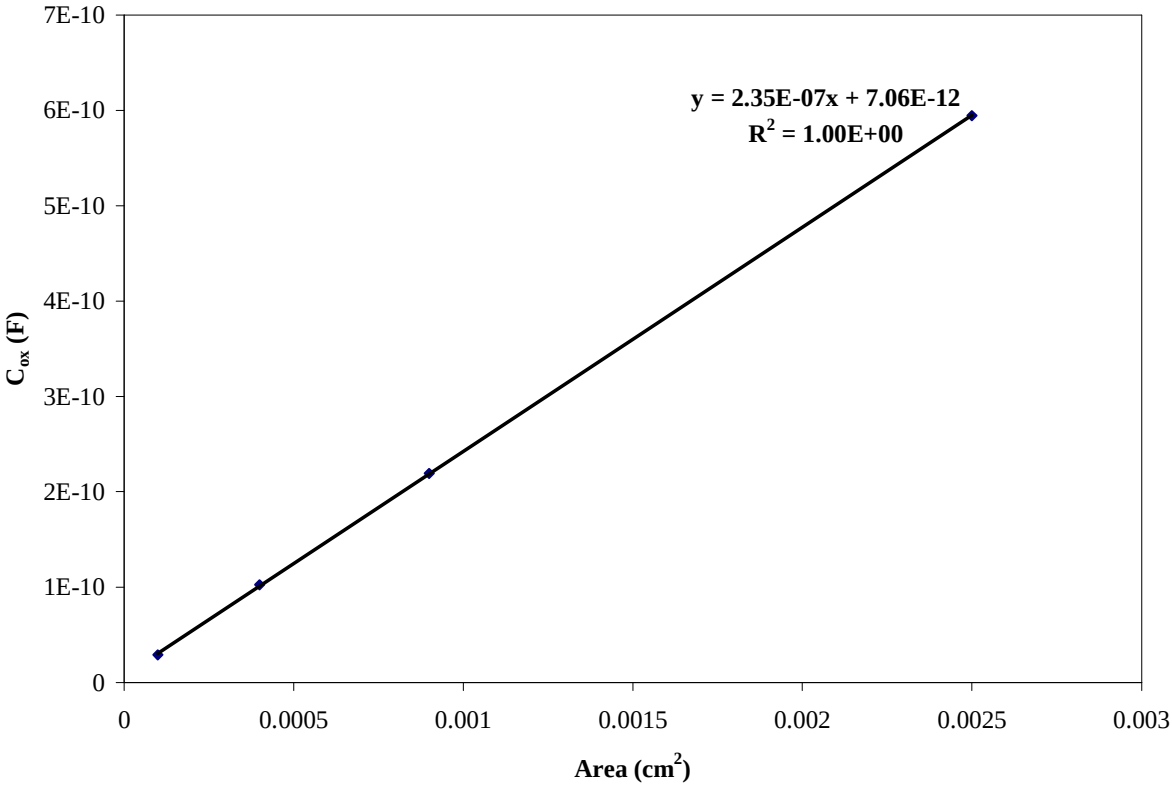
C_{ox} vs. Capacitor Area Plot for Wafer A1 (800°C/45 min./N_2)



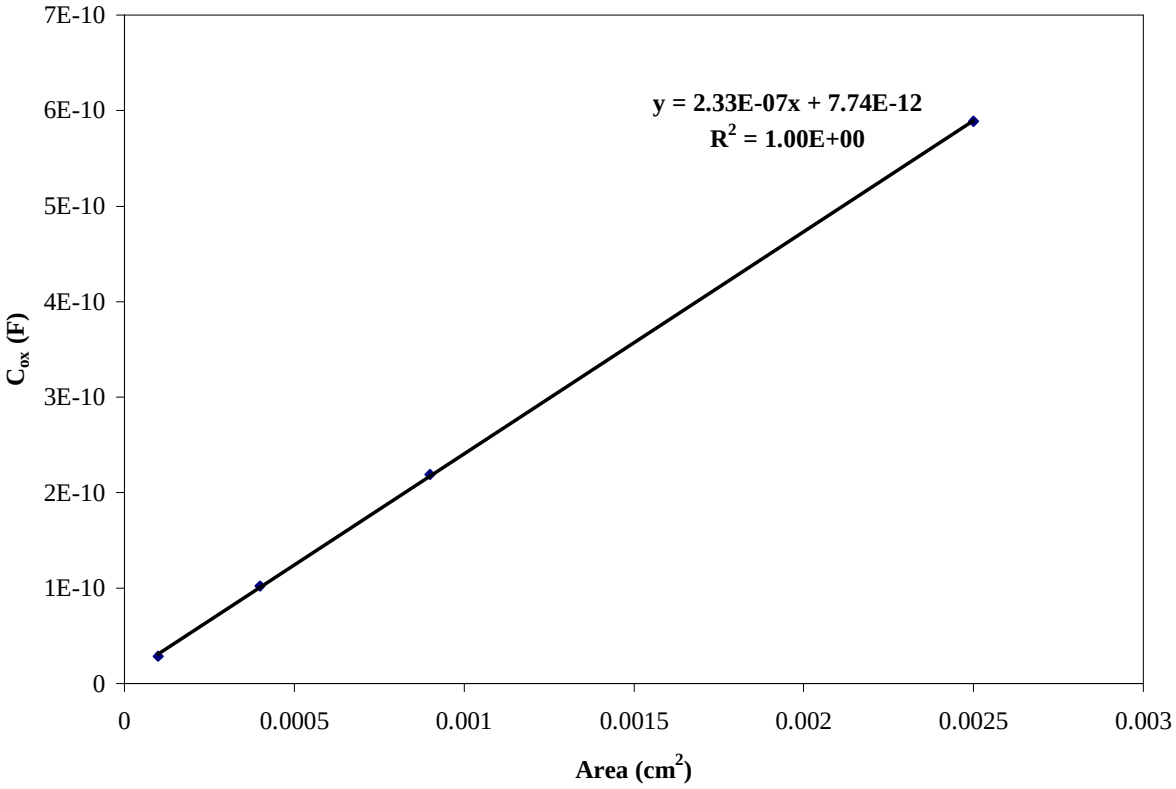
C_{ox} vs. Capacitor Area Plot for Wafer A2 (800°C/45 min./N_2O_2)



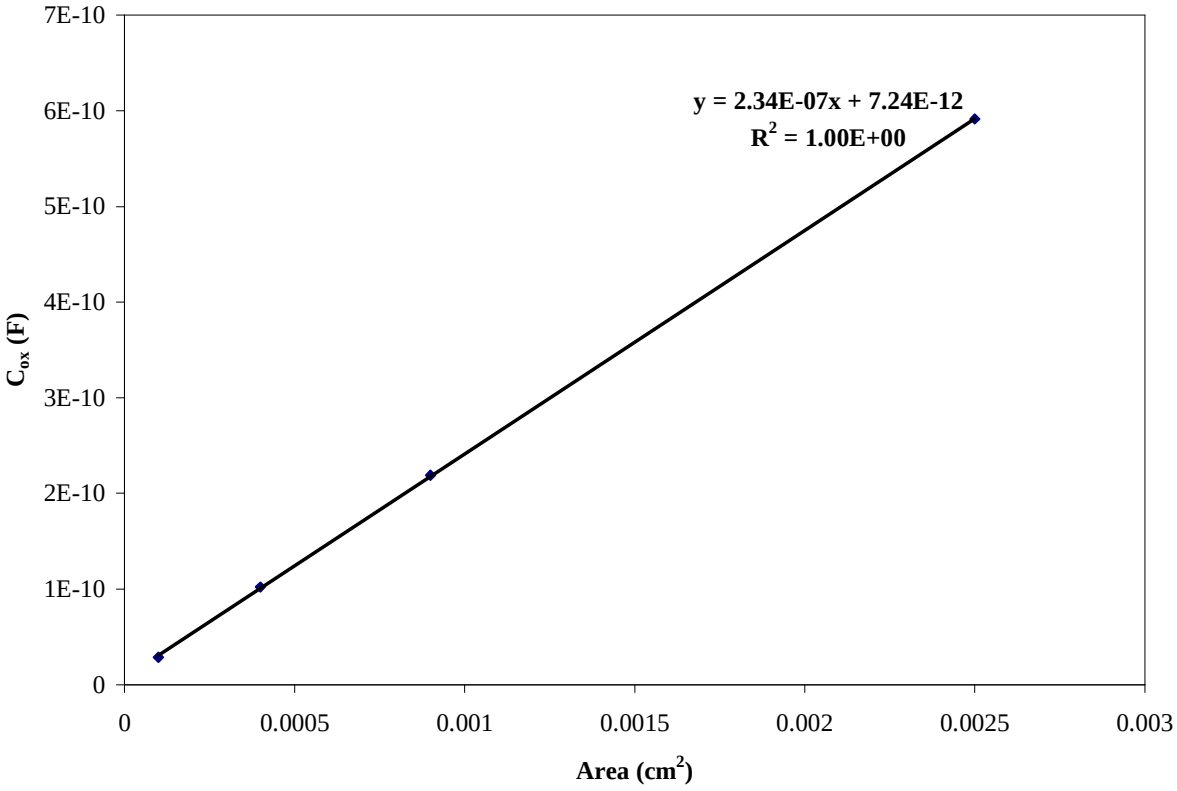
C_{ox} vs. Capacitor Area Plot for Wafer B7 (900°C/10 min./N_2)



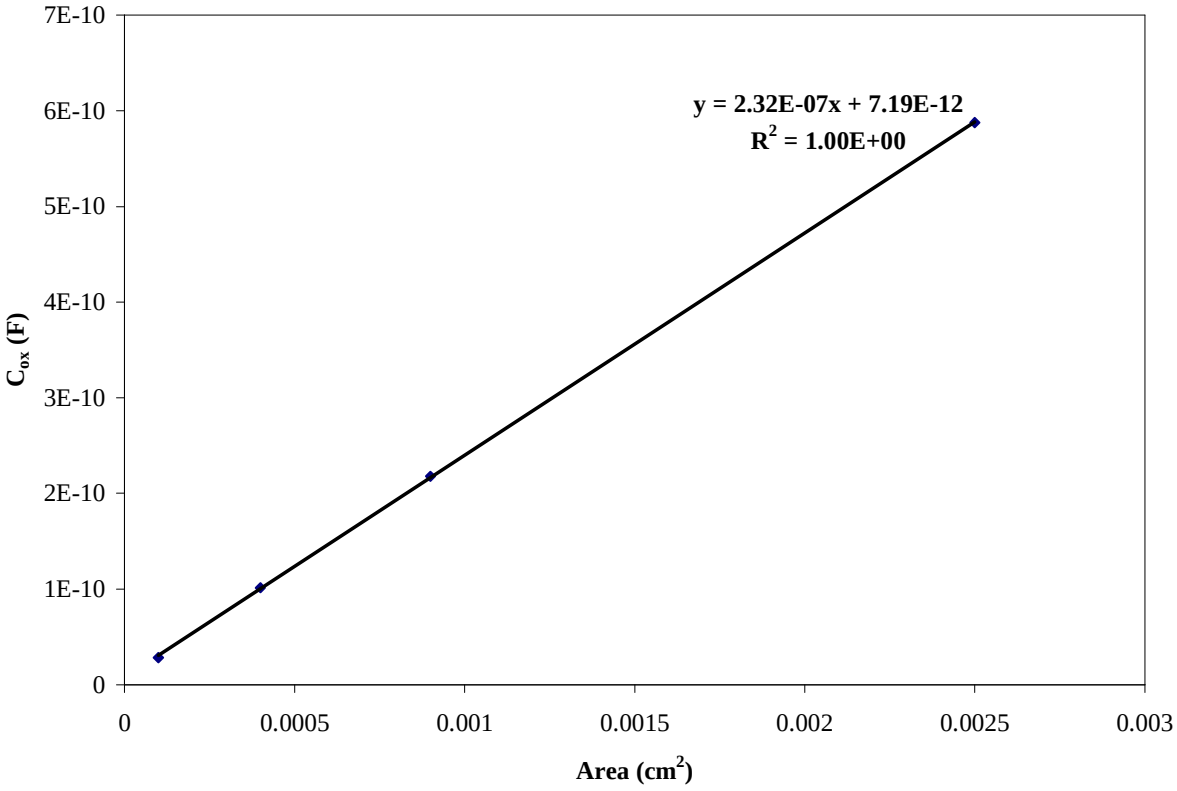
C_{ox} vs. Capacitor Area Plot for Wafer B8 (900°C/10 min./N_2O_2)



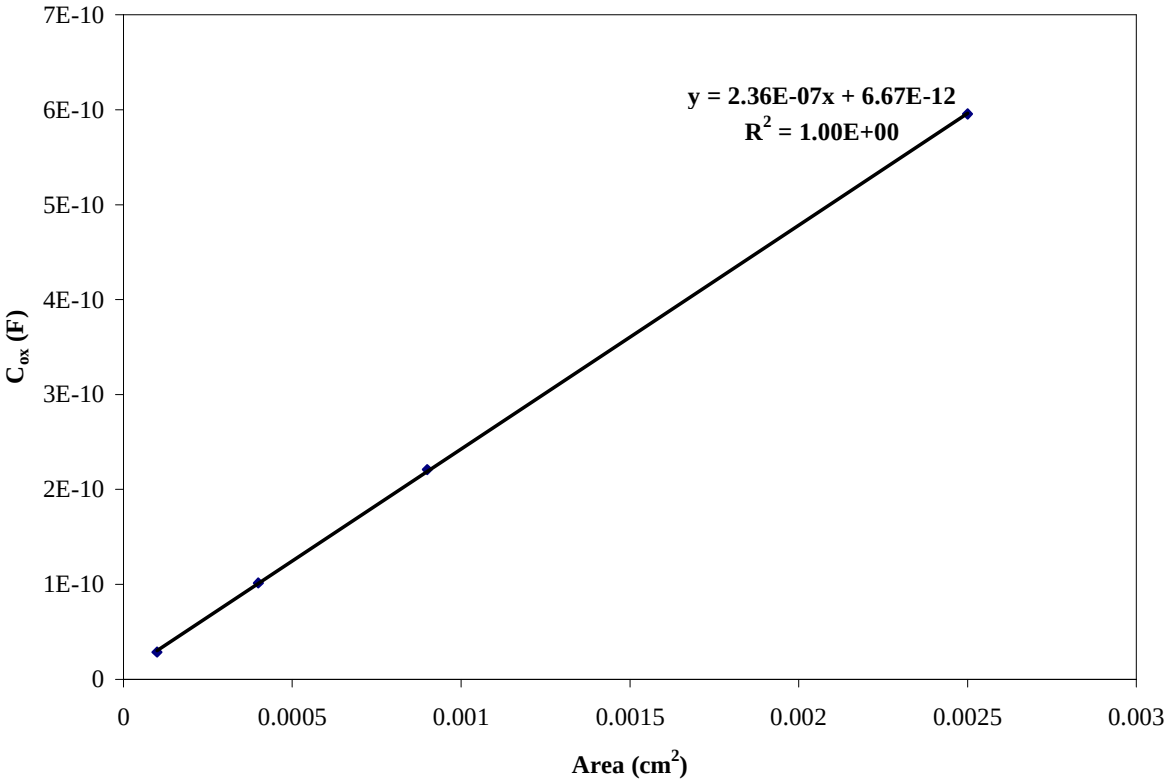
C_{ox} vs. Capacitor Area Plot for Wafer B5 (900°C/30 min./N_2)



C_{ox} vs. Capacitor Area Plot for Wafer B4 (900°C/30 min/N_2O_2)



C_{ox} vs. Capacitor Area Plot for Wafer B1 (900°C/60 min./N_2)



C_{ox} vs. Capacitor Area Plot for Wafer B2 (900°C/60 min./N_2O_2)