ABSTRACT

BAWA, GAURAV. A Switched Capacitor based Micro-stimulator for Deep Brain Stimulation. (Under the direction of Dr. Maysam Ghovanloo and Dr. Leda Lunardi.)

This thesis presents a novel technique for the development of an implantable stimulator for Deep Brain Stimulation. The key idea is to harvest energy from an inductive link using an efficient switching mechanism at the secondary side. To validate the concept, extensive characterization was performed by simulating explicit differential equations in MATLAB in addition to a prototype implementation in standard CMOS technology. In principle, a zero current switching methodology at the secondary coil has proved to be extremely energy efficient due to no extra wastage of power in the parallel resonant circuits.

A high efficiency full-wave rectifier has been implemented in standard CMOS technology, which ensures a measured efficiency of ~ 85 % while delivering ~ 19 mW of power to the load at 500 KHz input frequency. The underlying principle is that of synchronous rectification, minimization of MOS switch resistance through biasing in deep triode and blockage of reverse currents from the load to source using a lossless capacitive voltage divider technique.

Dual-mode backtelemetry has been incorporated in a full-wave active rectifier with minimal area overhead and an increased data rate and reading range in measurement results, when the rectifier loading varies over time.
DEDICATION

To

My Parents
BIOGRAPHY

Gaurav Bawa was born on 11th October, 1981, in Punjab, India. He received the B. Tech. in Electrical Engineering from the Indian Institute of Technology, Delhi, India in 2003. In Fall 2006, he started his graduate studies in the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh, North Carolina, USA.

In the summer of 2002, he was an intern in the Microelectronics Group at Università di Udine, Italy and in Fall 2003, at National Instruments, India, in the Motion Control Group. From 2003-2006, he worked as a Design Engineer at ST Microelectronics, India. During this period, he was involved in the design and validation of Flash Memory Test Vehicles in submicron NVM Technology, and subsequently in the design of analog-to-digital converters for the product division. His research interests include low-power RF, analog and digital circuit design.

He is a member of Phi Kappa Phi, Tau Beta Pi, and a student member of the Institute of Electrical and Electronics Engineers (IEEE).
ACKNOWLEDGEMENTS

First and foremost, I thank my parents for allowing me the freedom to choose the path less trodden and standing by me through thick and thin. To me, they are and will always be the epitomes of love, strength and integrity.

I thank Dr. Maysam Ghovanloo for providing me an opportunity to conduct research under his guidance. He is a great source of enthusiasm which is reflected in his research and teaching style. I am indebted to him for imbibing in me the mantra that “all research is quantitative”.

I would like to express my gratitude towards Dr. Leda Lunardi, for agreeing to serve as the co-chair of my committee. My sincere appreciation goes out to my very helpful and approachable committee members, Dr. Lianne Cartee and Dr. Kevin Gard. This thesis would not have been possible without the knowledge I gained in their courses. I also thank Dr. Subhashish Bhattacharya for selflessly taking out time for some intriguing technical discussions. I am grateful to Elaine Hardin for ensuring a smooth defense and graduation.

I thank Uei-Ming Jow, Ming Yin and Jia Wang, members of the NC-Bionics Lab, for helping me at various stages and providing a nice work environment. I thank Sandeep Navada for all the good and bad times that we shared, and in the present context, for helping remove some of the clutter in the development of Chapter 5 of the thesis. I also thank Abhik Sarkar, Suresh Thummalapenta and Sridevi Seshabhattar for treating me like a brother and Paula D’onofrio, for treating me like a son.
TABLE OF CONTENTS

List of Figures ........................................................................................................................................ v
List of Tables ......................................................................................................................................... xi

Chapter 1 ........................................................................................................................................ 1
  1. Introduction ................................................................................................................................. 1
    1.1 Background and Motivation ................................................................................................. 1
    1.2 Thesis Organization ............................................................................................................ 4
    1.3 References ............................................................................................................................ 5

Chapter 2 ........................................................................................................................................ 6
  2. System Architecture ................................................................................................................... 6
    2.1 Introduction ............................................................................................................................ 6
    2.2 System Overview ................................................................................................................ 6
    2.3 Detailed Description .......................................................................................................... 8
      2.3.1 Neuron Model ........................................................................................................ 8
      2.3.2 Stimulator Back-End .......................................................................................... 10
      2.3.3 Charge Metering and Failure Safety Block ................................................... 11
      2.3.4 Power Conditioning Block ............................................................................ 13
      2.3.5 Data Transmitter and Receiver Block ............................................................ 14
      2.3.6 Digital Controller Block ................................................................................ 14
    2.4 References ............................................................................................................................ 15

Chapter 3 ........................................................................................................................................ 17
  3. A High Efficiency Full-wave Rectifier in Standard CMOS Technology ............................... 17
    3.1 Introduction ............................................................................................................................ 17
    3.2 Circuit Description .............................................................................................................. 18
      3.2.1 Comparators ........................................................................................................ 20
      3.2.2 Output Voltage Monitor .................................................................................... 23
    3.3 Measurement Results ......................................................................................................... 23
    3.4 Power Dissemination in the Rectifier .............................................................................. 30
    3.5 Limits to Rectifier Dropout Voltage .............................................................................. 31
    3.6 Limits to Rectifier Efficiency ............................................................................................ 32
    3.7 Effects of Phase-Lead Control ............................................................................................ 33
    3.8 References ............................................................................................................................ 35

Chapter 4 ........................................................................................................................................ 37
  4. An Active Rectifier with built-in dual-mode Backtelemetry in Standard CMOS Technology .... 37
    4.1 Introduction ............................................................................................................................ 37
    4.2 Circuit Description .............................................................................................................. 39
    4.3 Measurement Results ......................................................................................................... 41
    4.4 Variations in loaded Q² in different modes of operation ............................................. 46
    4.5 Reflected Impedance in Backtelemetry .......................................................................... 51
    4.6 References ............................................................................................................................ 54
LIST OF FIGURES

Fig. 1.1 An implantable cardiac pacemaker device .................................................................1
Fig. 1.2 Examples of highly size constrained IMDs (a) Intraocular Epi-retinal Prostheses and (b) Cochlear Implant .................................................................2
Fig. 1.3 A state-of-the-art implanted deep brain stimulator ..................................................3
Fig. 2.1 Simplified Architecture of a contemporary wirelessly-powered Implantable Stimulator System .........................................................................................7
Fig. 2.2 (a) Neuron Model (b) Response of neuron to a stimulus ...........................................9
Fig. 2.3 A typical charge-balanced biphasic current stimulus pulse .....................................12
Fig. 3.1 Complete rectifier schematic including the inductive-link used for telemetry power transmission .........................................................................................18
Fig. 3.2 Comparator schematic representing the gray dashed box in Fig. 3.1 .......................20
Fig. 3.3 Simulation results showing the coil voltages \( V_{C1} \) and \( V_{C2} \), gate and bulk voltages for \( P_1 \) \( V_{GC1} \) and \( V_{BC1} \), respectively), and the output voltage \( V_{OUT} \) ...........................................................................21
Fig. 3.4 (a) Schematic diagram of the output voltage monitor. (b) Post-layout transient simulation of the rectifier waveforms at startup ..............................................24
Fig. 3.5 Die Photo of the rectifier in AMI 0.5 \( \mu \)m CMOS process .........................................25
Fig. 3.6 Measured rectifier input and output waveforms when \( V_{C1,2} = 5 \text{ V} \), \( R_L = 1 \text{ k}\Omega \) and \( C_L = 1 \text{ } \mu\text{F} \) ...........................................................................................................25
Fig. 3.7 Measured rectifier PCE and output DC voltage when \( V_{C1,2} = 5 \text{ V} \) and \( C_L = 1 \text{ } \mu\text{F} \) as a function of input carrier frequency \( f \) with output loading \( (R_L) \) of 1 k\( \Omega \) ...........................................................................................27
Fig. 3.8 Measured output DC voltage when \( V_{C1,2} = 5 \text{ V} \) and \( C_L = 1 \text{ } \mu\text{F} \) as a function of \( R_L \) with \( f = 0.5 \text{ MHz} \) ..............................................................................................................27
Fig. 3.9 Waveforms of a rectifier during the half-wave with time stamps indicated ...............29
Fig. 3.10 Pie-chart showing the simulation results of the distribution of input power in the Rectifier at maximum efficiency (90.4%) and nominal loading of \( R_L = 1 \text{ k}\Omega \), \( V_2 = 5 \text{ V} \), \( f = 0.5 \text{ MHz} \), and \( C_L = 1 \text{ } \mu\text{F} \) ..................................................................................31
Fig. 3.11 Simulated rectifier PCE and output DC voltage vs. \( R_L \) when ideal comparators \( (A_{1,2}) \) are used in the rectifier of Fig. 2 (compare with Fig. 5b). Operating conditions: \( V_{C1,2} = 5 \text{ V} \), \( f = 0.5 \text{ MHz} \), \( C_L = 1 \text{ } \mu\text{F} \) ..........32
Fig. 3.12 PCE variation vs. comparator delay, \( T_d \), at 1 MHz with and without phase-lead compensation using a capacitive divider with the voltage division ratio shown on the left vertical axis. The capacitive divider is added to the input of the comparator to control the reverse current ......................................................34
Fig. 3.13 PCE variations vs. phase-lead division ratio, \( \sigma = C_{POLY}/(C_{PAR} + C_{POLY}) \), for a fixed comparator delay of \( T_d = 10 \text{ ns} \) when \( V_{IN} = 5 \text{ V} \) at 1MHz .........................35
Fig. 4.1 Block diagram of a generic system for wireless power and data transmission across an inductive link. .......................................................................................38
Fig. 4.2 Complete active back-telemetry rectifier (ABTR) schematic for forward power and reverse data transmission over an inductive link .......................40
Fig. 4.3 Die photo of the active back telemetry rectifier chip fabricated in AMI 0.5-µm standard CMOS process (0.45 × 0.9 mm²) ..................................................42
Fig. 4.4 Measured ABTR waveforms showing consecutive OC, Rectifier, and SC modes of operation at f = 1 MHz, C_L = 144 nF and R_L = 1 kΩ .........................43
Fig. 4.5 Waveforms showing (from top) the original and Manchester-encoded data bit streams, primary sensed current, carrier envelope, and recovered back telemetry data, which was sent through the ABTR OC input at 200 kHz with f = 1 MHz, R_L = 1 kΩ and d = 20 mm ..................................................44
Fig. 4.6 Simplified and linearized equivalent circuit description for the inductive wireless link shown in Fig. 4.2 ........................................................................47
Fig. 4.7 Imaginary, real, and magnitude of the transponder impedance, Z_L, and its loaded quality factor, Q_{2L}, vs. the linearized resistance seen through ABTR input port R_{L,eq} in Fig. 4.6..........................................................52
Fig. 4.8 The reflected impedance (Z_R) at the primary shown in the complex plane as a function of equivalent loading at the secondary (R_{L,eq}), with R_{L,eq} ascending from left to right in the range 1 Ω – 1 kΩ ..................................................53
Fig. 5.1 Equivalent Circuit model of a half-wave rectifier ......................................58
Fig. 5.2 Triangular approximation of the V_{OUT} steady state ripple waveform during charging and discharging phases of C_L when the rectifier switch closes and opens with duty cycle, D, in every carrier cycle, T_S = 1/f. The same model applies to full-wave rectifiers if V_{IN} is commutated and T_S = 1/2f ..................59
Fig. 5.3 Half-wave rectifier waveforms generated in MATLAB based on more realistic differential equations setup in section 5.3 to find the relationship between switching duty cycle, D, and other circuit parameters in Fig. 5.1. V_{IN} = 5 V, f = 1 MHz, R_S = 5 Ω, R_L = 1 kΩ, and C_L = 1 nF .........................62
Fig. 5.4 Plot of f(D), defined in section 5.3, with zero crossing at D = 0.21 for V_{IN} = 5 V, f = 1 MHz, R_S = 5 Ω, R_L = 1 kΩ, and C_L = 1 nF in Fig. 5.1 ......................64
Fig. 5.5 Comparing closed form approximation, numerical differential equations, and SPICE simulation methods for evaluating the rectifier PCE vs. R_L. Nominal values are C_L = 1 µF, R_L = 1 kΩ, and R_S = 5 Ω ........................................65
Fig. 5.6 Comparing closed form approximation, numerical differential equations, and SPICE simulation methods for evaluating the rectifier PCE vs. C_L. Nominal values are C_L = 1 µF, R_L = 1 kΩ, and R_S = 5 Ω ........................................66
Fig. 5.7 Comparing closed form approximation, numerical differential equations, and SPICE simulation methods for evaluating the rectifier PCE vs. R_S. Nominal values are C_L = 1 µF, R_L = 1 kΩ, and R_S = 5 Ω ........................................67
Fig. 5.8 Plot showing the variation of the total switch resistance, R_S, with the choice of the width of the PMOS transistor, for a given area constraint of A = 2500 µm² in AMI-0.5 µm standard CMOS technology (Table 5.1) .......................72
Fig. 5.9 SPICE simulation results showing the variation of PCE and V_{OUT} vs. the PMOS switch size (W_P) for a given silicon area, A = 5000 µm², in a full-wave IC-rectifier with ideal comparators in 0.5-µm CMOS technology ..............73
Fig. 5.10 SPICE simulation results showing the variation of PCE and vs. the PMOS switch size \( W_P \) at an operating frequency of 13.56 MHz, in a full-wave IC-rectifier with ideal comparators in 0.5-µm CMOS technology. The NMOS switches are driven dynamically in this case ........................................74
Fig. 5.11 Schematic of a full-wave rectifier core operating at ISM Band frequency ..75
Fig. 5.12 A high speed asynchronous comparator driving the NMOS switch in a full-wave rectifier operating at \( f = 13.56 \) MHz ..............................................................76
Fig. 6.1 Circuit Description and step response of charging a capacitor with (a) Constant Voltage Source (b) Constant Current Source ...........................................81
Fig. 6.2 Circuit Schematic showing the concept of a half-wave Parallel SCS .............83
Fig. 6.3 MATLAB simulation of a half-wave Parallel SCS, when \( f = 1 \) MHz, \( L_2 = 7.77 \) µH, \( R_2 = 4.975 \) Ω, \( C_2 = 3.26 \) nF, \( C_LP = 1 \) µF, \( T_{SW} = 50 \) ns, \( V_{IND} = 0.35 \) V 86
Fig. 6.4 Efficiency and Energy Profile in MATLAB of a half-wave Parallel SCS, when \( f = 1 \) MHz, \( L_2 = 7.77 \) µH, \( R_2 = 4.975 \) Ω, \( C_2 = 3.26 \) nF, \( C_LP = 1 \) µF, \( T_{SW} = 50 \) ns .................................................................88
Fig. 6.5 Circuit Schematic showing the concept of a full-wave Series SCS. The control circuitry is not shown .................................................................97
Fig. 6.6 MATLAB simulation showing the voltage profile during switching of a full-wave Series SCS, when \( f = 1 \) MHz, \( L_2 = 3.05 \) µH, \( R_2 = 0.53 \) Ω, \( C_2 = 8.3 \) nF, \( C_{LP,N} = 1 \) µF, \( V_{IND} = 5 \) V .................................................................98
Fig. 6.7 MATLAB simulation of a full-wave Series SCS, when \( f = 1 \) MHz, \( L_2 = 3.05 \) µH, \( R_2 = 0.53 \) Ω, \( C_2 = 8.3 \) nF, \( C_{LP,N} = 1 \) µF, \( V_{IND} = 5 \) V. (a) Input and output voltages (b) Input inductor current ...........................................99
Fig. 6.8 MATLAB simulation results showing the dependence of efficiency and output DC voltage on \( R_2 \) in a full-wave Series SCS, when \( f = 1 \) MHz, \( L_2 = 3.05 \) µH, \( C_2 = 8.3 \) nF, \( C_{LP,N} = 1 \) µF, \( V_{IND} = 5 \) V .........................................................100
Fig. 6.9 MATLAB simulation of a full-wave Series SCS, when \( f = 1 \) MHz, \( L_2 = 3.05 \) µH, \( R_2 = 0.53 \) Ω, \( C_2 = 4 \) nF, \( C_{LP,N} = 1 \) µF, \( V_{IND} = 5 \) V. (a) Input and output voltages (b) Input inductor current .........................................................101
Fig. 6.10 MATLAB simulation results showing the dependence of efficiency and output DC voltage on \( R_2 \) in a full-wave Series SCS, when \( f = 1 \) MHz, \( L_2 = 3.05 \) µH, \( C_2 = 4 \) nF, \( C_{LP,N} = 1 \) µF, \( V_{IND} = 5 \) V .........................................................102
Fig. 6.11 MATLAB simulation results showing the dependence of (a) efficiency and output DC voltage (b) charging time, on \( C_2 \) in a full-wave Series SCS, when \( f = 1 \) MHz, \( L_2 = 3.05 \) µH, \( R_2 = 0.53 \) Ω, \( C_{LP,N} = 1 \) µF, \( V_{IND} = 5 \) V .................................103
Fig. 6.12 MATLAB simulation results showing the dependence of efficiency and output DC voltage on \( f \) in a full-wave Series SCS, when \( L_2 = 3.05 \) µH, \( C_2 = 4 \) nF, \( R_2 = 0.53 \) Ω, \( C_{LP,N} = 1 \) µF, \( V_{IND} = 5 \) V .........................................................104
Fig. 6.13 MATLAB simulation results showing the dependence of (a) charging time and (b) output DC voltage on \( C_2 \) and \( C_{LP,N} \) in a full-wave Series SCS, when \( f = 1 \) MHz, \( L_2 = 3.05 \) µH, \( R_2 = 0.53 \) Ω, \( V_{IND} = 5 \) V .........................................................105
Fig. 6.14 MATLAB simulation results showing the dependence of efficiency on $C_2$ and $C_{LP,N}$ in a full-wave Series SCS, when $f = 1$ MHz, $L_2 = 3.05$ $\mu$H, $R_2 = 0.53$ $\Omega$, $V_{IND} = 5$ V ................................................................................................106
Fig. 6.15 Schematic of PMOS based switch for implementing the switch for (a) $C_{LP}$ (b) $C_{LN}$ .............................................................................................................................................109
Fig. 6.16 Schematic of NMOS based switch for implementing the switch for (a) $C_{LP}$ (b) $C_{LN}$ .............................................................................................................................................110
Fig. 6.17 Complete Circuit Schematic of the Series SCS .........................................................................................111
Fig. 6.18 CMOS Schematic of (a) Preamplifier (b) Comparator_P,N .........................................................112
LIST OF TABLES

Table 4.1 Active Back Telemetry Rectifier Modes of Operation..............................41
Table 4.2 Q_{2L} and R_{LEQ} Variations in various modes of rectifier operation ..........51
Table 5.1 Typical model parameters for AMI 0.5 µm process at room temperature .71
Table 6.1 P1 (Fig. 6.15a) conditions during two phases of the coil voltage ..........108
Table 6.2 P2 (Fig. 6.15b) conditions during two phases of the coil voltage ..........108
Table 6.3 N2 (Fig. 6.16b) conditions during two phases of the coil voltage ..........108
Chapter 1

1. Introduction

1.1 Background and Motivation

With the advent of integrated circuit technology, the miniaturization of complex computing systems such as microprocessors occurred as a natural consequence which revolutionized the way the common man perceived these large processing machines. Towards the later part of the 20th century, the miniaturization due to the silicon technology and its biocompatibility resulted in advancement of medical electronics. This occurred simultaneously with the advancement in neurophysiology. In late 1950s, the development of integrated cardiac pacemakers took place, whose basic purpose is to

![An implantable cardiac pacemaker device](image)

Fig. 1.1. An implantable cardiac pacemaker device [1].
ensure that heart beats at the correct rate and rhythm. Thus, in such a device, the circuitry for both the recording/processing and generation of the cardiac action potentials is necessary. Fig. 1.1 shows the example of a state-of-the-art pacemaker device, in which a battery is present to supply DC power to the on-chip circuitry, which has a lifetime of 10 ~ 12 years, made possible through ultra-low-power design techniques [1].

In the last few decades, researchers have been working towards more ambitious goals like cochlear implants and retinal prostheses for aiding the deaf and blind respectively (see Fig. 1.2). Due to size constraint in these applications, it is not possible to have a small enough battery present with the implant, which can ensure a lifetime similar to that in the case of pacemakers. In such scenarios, the power transmission needs to be done wirelessly since the implant needs to be minimally invasive. This is accomplished through an inductive link, in which the primary coil is powered by a

Fig. 1.2. Examples of highly size constrained IMDs (a) Intraocular Epi-retinal Prostheses [2] and (b) Cochlear Implant [3].
battery while the secondary coil converts the variations in magnetic flux to electrical signals and is made available to a rectifier which performs AC-DC conversion to power the stimulator or recording circuitry. The complete system needs to be extremely energy-efficient to maximize the life and minimize the size of the external battery, and to minimize the internal power dissipation which can raise the temperature of the implant. The exact value depends on the location of the implant inside the body, but as a thumb-rule, it should not result in an increase of temperature of the surrounding tissue by more than 1 °C [4].

Deep brain stimulation is a commercially available effective therapy for patients suffering from movement disorders like Parkinson’s disease, Tremor and Dystonia. These devices being inspired by the pacemaker technology are currently
implanted in the chest area of the patient, as shown in Fig. 1.3. The wires connecting the stimulator device to the implanted electrodes run through the back of neck and result in mechanical failures due to strain developed over a period of time. This is the case since these stimulators are not efficient enough to result in a smaller battery, which consumes half the area of the total implanted device. The ultimate goal of this research is to provide energy-efficient solutions in wireless power transmission to take the battery out of the system, leading to considerable size reduction. Hence, it would be possible to fit the device outside the skull, under the scalp leading to minimal invasiveness, reduced patient discomfort and an enhanced robustness.

In addition to the power transmission, there is a need for data transmission from the implant. This is important for the doctor to be able to adjust the stimulation parameters, to set up a feedback loop or to know the status of the implanted device. The same principle is applicable in passive Radio-Frequency-Identification (RFID) systems, in which the reader wirelessly powers the transponder through an alternating carrier and performs identification by sending data back and forth on the same carrier signal [6]. More recently, researchers are looking at efficient means of energy harvesting in micro-power applications for use in wireless sensor nodes [7].

1.2 Thesis Organization

The thesis has been organized as follows: Chapter 2 describes the complete system architecture of a wirelessly powered implantable device for stimulation. Chapter 3 describes a high-efficiency Rectifier in standard CMOS technology. Chapter 4
describes the theory and implementation of complementary Backtelemetry features in an active rectifier leading to an enhanced reading range. Chapter 5 provides the analysis and design guidelines for an active full-wave rectifier in standard CMOS technology. Chapter 6 describes the theory and proof-of-concept for an energy-efficient switched capacitor based microstimulator. Finally, Chapter 7 contains the conclusions of the thesis with scope for future work.

1.3 References


Chapter 2

2. System Architecture

2.1 Introduction

In this chapter, we describe a system level architecture for size-constrained implantable microelectronic devices (IMD) that do not have a built-in battery, and are hence wirelessly powered. As discussed in Chapter 1, this is indeed true for applications like bionic ears and epi-retinal prosthesis. Since the larger objective of this research is to eliminate a battery in a conventional Deep Brain Stimulation implant by employing efficient energy harvesting techniques from an inductive link, the resultant stimulator architecture will also be applicable to DBS.

2.2 System Overview

With the battery absent from the implanted system, the power requirements need to be met by wireless power transmission through a pair of magnetically coupled coils, which must be placed close to each other at a distance of a few centimeters, depending on the nature of application. This is done in order to increase the coefficient of coupling ($k$) between the coils and hence maximize the efficiency of the link.

A generic architecture of such a system is shown in Fig. 2.1. The complete system consists of components that are either external to the body or implanted inside the body. The latter can either be implemented on an integrated circuit (IC) or be present off-chip as a discrete component. This choice is mainly based on area-cost
Fig. 2.1: Simplified Architecture of a contemporary wirelessly-powered Implantable Stimulator System.
tradeoff. While an integrated circuit helps in reduction of size, it comes with a cost overhead. Hence, the components which do not show appreciable reduction in size on migration to an IC should preferably be implemented as a discrete component.

2.3 Detailed Description

In this section, we will have a closer look at the components and their specifications. The sub-division has been done based on the functionality and deliberately done with a bottom-top approach to understand the system conception. To begin with, a generic neuron electrical model is presented to understand the target load driven by the system.

2.3.1 Neuron Model

Fig. 2.2 (a) shows the Hodgkin-Huxley model for a cell membrane based on the observations from the voltage-clamp experiments conducted on a squid axon [1]. 

\[ C_{MEM} \] is the capacitance of the membrane which physically exists due to the separation of two conducting mediums with different concentrations. The ionic contributions of Sodium (Na\(^+\)), Potassium (K\(^+\)) and Chlorine (Cl\(^-\)) diffusion currents is modeled by the conductance \( g_{NA}, g_K \) and \( g_{CL} \) in series with their respective Nernst Potentials [2]. When the membrane is at equilibrium and no current flows through \( C_{MEM} \), the membrane rest potential is given by,

\[
V_{MEM, \text{REST}} = \frac{g_{NA}E_{NA} + g_KE_K + g_{CL}E_{CL}}{g_{NA} + g_K + g_{CL}} \quad (2.3.1.1)
\]
Fig. 2.2. (a) Neuron Model (b) Response of neuron to a stimulus [3]
The Nernst Potentials for potassium and chlorine are negative while that of sodium is positive. The resulting rest potential of the membrane is typically ~ -70 mV.

Fig. 2.2 (b) shows the response of a neuron to a stimulus. If the magnitude of the stimulus is so small that it is unable to depolarize the cell membrane a threshold voltage above its resting potential, then no action potential will occur. In this case, the response resembles that of a parallel $RC$ charging and discharging profile. Once the threshold is exceeded, the sodium activation channels begin to open leading to a greater influx of Na$^+$ ions from extracellular to intracellular medium, leading to cell membrane depolarization. At the peak of the curve, the sodium inactivation channels close leading to a period of refractoriness. At this point, K$^+$ ions begin to leave the cell due to the activation of their gating channels which leads to a decrease in the membrane potential. This eventually results in a period of hyperpolarisation before the cell membrane reaches its resting potential [2]. This variation in the ionic conductance over time is represented by a variable resistance in the electrical model in Fig. 2.2 (a), resulting in a non-linear load for the stimulator.

2.3.2 **Stimulator Back-End**

Neural stimulation refers to the process of injecting charge into the neural tissue to evoke an action potential. Generally, the method of stimulation is extracellular in which the extracellular medium is made more negative which is same as driving the intracellular potential to a positive potential, hence leading to membrane depolarization.
There can be multiple sites present in a given stimulator depending on the type of application, and the number of the sites active at any given time is generally programmable. In addition, the stimulation can either be Monopolar or Bipolar. In Monopolar stimulation, the charge is injected in the extracellular medium using a given working electrode while the charge is returned to a distant ground reference, which can be made as the body of the stimulator. In this case, the stimulating site can be modeled as a point source generating spherical equipotential surfaces around it, making it non-directional. In Bipolar stimulation, the working and the counter electrode are placed in close proximity, such that the current passing through one is returned through the other electrode. This ensures a greater degree of selectivity in stimulation since the electric field distribution is concentrated. In Fig. 2.1, the example shown is that of bipolar stimulation, with the electrodes modeled by their equivalent double layer capacitance, $C_{DL}$ [4]. In addition, these electrodes are shown to be integrated since they can be fabricated on silicon substrates along-with the CMOS circuitry, also known as micro-machined electrodes [5]. This ensures complete integration of the entire system resulting in an extremely compact footprint.

2.3.3 Charge Metering and Failure Safety Block

During stimulation, the net charge stored in the tissue should ideally be zero at the end of the stimulus pulse since it can lead to irreversible non-Faradaic reactions at the electrode-electrolyte interface. This can lead to changes in the pH of the electrolyte or the corrosion of the electrode. In order to prevent this, symmetric biphasic
Fig. 2.3. A typical charge-balanced biphasic current stimulus pulse [4].

Pulses are used for stimulation for charge balancing. This means that an anodic phase always follows a cathodic phase or vice-versa (Fig. 2.3). There exist safety limits based upon the amount of charge injected into the tissue per stimulus phase ($Q_{PM}$) and charge density of the microelectrode ($Q_D$) [6]. Thus, a biocompatible electrode with high charge carrying capability should be the choice for this application. Typically, Iridium Oxide or Tantalum electrodes since they display the aforementioned characteristics [7].

Typically, the stimulators used are either voltage-controlled (VCS) or current-controlled (CCS). In VCS, the amount of charge injected into the tissue is not controlled and hence there is a need for charge metering. One method is to measure the charge injected by integrating the current flowing into the electrode over time. This analog information can be converted to digital domain by the use of a precision low-power Analog-to-Digital Converter (ADC). The binary data bits thus obtained can be used to communicate to the central control system and be stored on-chip for data-logging. Even in the case of CCS, to ensure that the net charge injected is zero is practically not possible. This is because, the
current injected in the cathodic and anodic phases is limited by the mismatch between the transistors and hence a technology dependent parameter which of the order of \( \sim 1 - 2 \% \). One simple way to achieve this is by shorting the electrode after stimulation, the accuracy of which is constrained by the switch resistance, the double layer capacitance and the frequency of stimulation. For stimulators requiring higher matching, especial circuit techniques need to be utilized [8].

**Failure safety** is an important feature of an implantable stimulator. This is because, if a device failure takes place, it must be ensured that an uncontrollable amount of charge is not injected into the tissue. This can be heuristically ensured by evaluating faults such as junction and oxide breakdowns and generating appropriate status signals on the chip [9].

### 2.3.4 Power Conditioning Block

The most important block in the complete system is the one ensuring the power transfer since power efficiency is one of the most important factors in biomedical implants. In a typical wirelessly powered system as shown in Fig. 2.1, the battery is present external to the human body providing stable DC supply to a switch-mode class-E power amplifier (PA). It is desirable to maximize the efficiency to maximize the battery life and reduce its size, and most importantly to minimize the power dissipated in the tissue. The PA powers the primary inductor \( L_1 \) which is loosely coupled to a secondary coil \( L_2 \), implanted inside the body. Since the size of \( L_2 \) cannot be made very large, the coupling between the coils \( k \) becomes an important bottleneck in the power
transmission efficiency. The AC power received at the secondary is converted to DC by an integrated voltage rectifier, which is generally followed by a low-dropout voltage regulator (LDO) to provide high frequency switching noise free stable supply, $V_{\text{SUPPLY}}$. As can be seen from Fig. 2.1, this supply is made available to rest of the on-chip circuitry. A power-on-reset circuit present after the voltage regulator detects a stable value of $V_{\text{SUPPLY}}$, and resets the state machine in the digital control logic.

It must be understood that the bottleneck in power transmission efficiency in mainly the coupling of the inductors, the voltage rectifier and finally the stimulator block. The focus of this work is mainly on the rectifier and stimulator blocks as will be covered in later chapters.

### 2.3.5 Data Transmitter and Receiver Block

There is a need for forward data transmission from the external world to the implanted system. This is mainly to allow the programmability of the stimulation parameters, since the doctor needs to adjust them for a certain individual. The forward data is generally produced by modulating the carrier at the transmitter and the receiver implemented on-chip for demodulating the data and clock extraction from the same.

In addition, there can be a need to transmit data back to the external world which could include status of the implant temperature (sensors not shown in Fig. 2.1), a failure status or send back the data logged during stimulation. This is generally achieved by a low data rate backtelemetry which can be incorporated in the voltage rectifier, as will be discussed in Chapter 4.
2.3.6 **Digital Controller Block**

The digital controller module forms the brain of the implant, making sure that the system works in a proper order both in terms of handshaking between the various on-chip components and that with the external world. It is fairly inexpensive in terms of power requirements since there is no need for a very high speed operation in such an application. The implementation should preferably be custom ASIC design as against a reconfigurable logic in order to optimize the design for area and power. In addition, several low-power digital design techniques can also be used, if the frequency of operation is not high [10].

2.4 **References**


[3] [http://media.wiley.com/assets/7/95/0-7645-5422-0_0704.jpg](http://media.wiley.com/assets/7/95/0-7645-5422-0_0704.jpg)


Chapter 3

3. A High Efficiency Full-wave Rectifier in Standard CMOS Technology

3.1 Introduction

Wireless transmission of power in applications where batteries cannot be used due to size, lifetime, or cost constraints usually takes place by inducing an AC power carrier signal through a pair of inductively coupled coils that constitute a transformer. A rectifier follows the receiver LC-tank circuit to convert the AC carrier to a DC voltage, which supplies the rest of the system. The small coupling coefficient between the two coils is the bottleneck in wireless power transmission. Therefore, the received power is considered precious and should be preserved in the AC-DC conversion. Radio frequency identification (RFID) [1], [2] implantable microelectronic devices (IMD) [3], and wireless sensors [4] are some of the size constrained applications in which an integrated rectifier plays a significant role. Including the cost in this equation leads ASIC designers towards implementing the entire system, including the rectifier, on a chip (SoC) in standard CMOS technology. However, up until now CMOS rectifiers have generally suffered from low power conversion efficiency (PCE) mainly due to the large dropout voltage across the diode-connected MOSFETs. Other factors that can degrade the PCE include the reverse current from the load back to the LC-tank circuit and the leakage current into the substrate. In this chapter we explain a new full-wave CMOS rectifier with minimized dropout voltage through biasing the main conducting MOSFETs in deep
triode region as well as decreasing the reverse and substrate leakage currents. We also ensure the rectifier safe startup by employing a supporting parallel path.

### 3.2 Circuit Description

A generic inductive link for power transmission including a simplified schematic of the proposed rectifier is shown in Fig. 3.1. Instead of diode-connecting the main rectifying PMOS transistors ($P_1$, $P_2$) as in our prior work [5], a pair of comparators is used to sense the difference between the input coil voltages ($V_{C1}$, $V_{C2}$) and the rectified output ($V_{OUT}$) across each rectifying PMOS. The comparator outputs switch $P_1$ and $P_2$ On
or Off depending on whether \( V_{C1,2} \) are greater or lesser than \( V_{OUT} \), respectively. When the comparator outputs are low, \( V_{SG1,2} \approx V_{C1,2} > (V_{SD1,2} + |V_{TP}|) \), where \( V_{TP} \) is the PMOS threshold voltage. As long as \( V_{OUT} > |V_{TP}| \), \( P_1 \) and \( P_2 \) are pushed into deep triode region where they are On and produce a much smaller dropout along the main current path to the load, \( R_L \), compared to when they are in saturation. Similarly, \( N_1 \) and \( N_2 \) experience a large \( V_{GS1,2} = V_{C1,2} > V_{TN} \) when they are On and, therefore, show a small dropout in the current return path from \( R_L \) back to the LC-tank. \( P_{1-5} \) have been implemented in separate n-well regions and their bulk voltages are dynamically controlled using auxiliary PMOS devices \((P_{IA}, P_{IB})\) to eliminate body-effect and substrate leakage. While the former prevents the threshold voltage of the rectifying transistors from increasing, hence reducing the dropout voltage, the latter reduces the risk of latch-up [5]. Both of these effects also help improving the rectifier PCE.

One of the challenges in this design was to provide a stable operating voltage for the comparators at rectifier startup when the \( V_{OUT} \) has not yet been stabilized. This could potentially be fatal for the rectifier operation as it can result in the rectifier never waking up because of \( P_{1,2} \) being continually Off due to the lack of proper gate drive. Our solution was to utilize a diode-connected dummy rectifier \((P_3, P_4)\) in parallel with the main rectifier to quickly charge a relatively small capacitor, \( C_{DUM} = 1 \) nF, and provide an early operating supply, \( V_{DUM} \), just for the comparators in Fig. 3.1. It should be noted that \( N_{1,2} \) can provide the return current path for both the dummy and main rectifiers. Once \( V_{OUT} \) rises above \( V_{DUM} \) (due to smaller dropout), transistor \( P_5 \), controlled by a threshold monitoring circuit, connects \( V_{OUT} \) to \( V_{DUM} \) and automatically turns the
dummy rectifier $Off$. In the rest of this section we describe the details of the rectifier operation, some of the design issues, and post-layout simulation waveforms.

### 3.2.1 Comparators

In this topology (Fig. 3.1), the most important block that determines the rectifier performance is the comparator. Two-stage hysteresis comparators were designed (Fig. 3.2) using partial positive feedback [6] with an input common-mode range (ICMR) that extends beyond the supply level by utilizing an NMOS folded cascode differential pair. An output stage is also added to provide rail-to-rail output swing as well as high

![Fig. 3.2. Phase Lead Comparator schematic representing the gray dashed box in Fig. 3.1.](image-url)
speed drive capability of the large P\textsubscript{1,2} capacitive gate terminals (W/L = 2.5mm/0.6µm).

Hysteresis is important for this application to reject noise and interference at the input of the comparators and to reject the dip in the input coil voltage when P\textsubscript{1,2} are activated. This dip is due to the fact that when current passes through P\textsubscript{1}, the return current through N\textsubscript{2} causes C\textsubscript{2} to become slightly negative and consequently decreases C\textsubscript{1}. This effect is illustrated in the simulation in Fig. 3.3.

A supply-independent bias for the comparator is provided by a beta multiplier, which is designed to provide a current of 2 µA at 2.5 V supply. Both the bias generator and the comparator are connected to $V_{DUM}$ to quickly start up and initiate the rectification process. There exists a possibility of back current propagation from the ripple-rejection capacitor, $C_L$, back to the coil when $V_{C1,2} < V_{OUT}$ and the comparator
tends to switch \( P_{1,2} \) \textit{Off}. This current, which can reduce the rectifier PCE by stealing the stored charge from \( C_L \), results mainly from the finite delay associated with the comparators. Increasing the comparators speed would be helpful only up to a certain level at the cost of increased power consumption, which also harms the PCE. Our remedy was to create a phase-lead and initiate an early comparison by utilizing lossless capacitive voltage dividers at the negative input terminal of each comparator, as illustrated in Fig. 3.2. The small phase-lead will compensate for the comparator delay both at the onset of \( P_{1,2} \) turn-on and at turn-off. Capacitive dividers have an insignificant effect on the LC-tank resonance frequency, which can be accounted for by adjusting \( C_P \) value.

The capacitive division is achieved by using a poly-poly capacitor, \( C_{POLY} \), and the input gate capacitance of the folded cascode NMOS, \( C_{PAR} \), as shown in Fig. 3.2. Even though \( C_{PAR} \) is highly nonlinear, since the \( P_{1,2} \) switching mainly takes place when the coil voltages are high, we can expect \( C_{PAR} \) to show a constant gate capacitance in the strong inversion region. Care must be taken to ensure that the bottom plate of \( C_{POLY} \) is connected to the input coil nodes and not to the floating input node of the comparator. In this design, the comparator delay and hysteresis, and the capacitive divider work in synergy to prevent any reverse current from propagating back to the coil. Disruptions in this balance can lead to decreased PCE. Therefore, a tuning mechanism would be desirable. For example, PCE would be lowered by an increased comparator hysteresis that delays \( P_{1,2} \) firing. The effect of capacitive voltage divider is more complicated. An increased ratio would mean that \( P_{1,2} \) turns \textit{On} early and \textit{Off} late. This will lead to reverse currents before and after \( V_{P1,2} \) peaks and lower the PCE. The simulation
waveforms in Fig. 3.3 show the comparator action with $V_{OUT}$ and $V_{CID}$ being the comparator inputs and $V_{GC1}$ as its output.

### 3.2.2 Output Voltage Monitor

The comparators are initially powered by the dummy rectifier path (P$_{3,4}$) to quickly become functional and start the main rectifier. However, once the main rectifier starts up, $V_{OUT}$ surpasses $V_{DUM}$ due to its smaller dropout voltage and it would be necessary to supply the comparators from $V_{OUT}$ to extend their input dynamic range. A simple circuit, shown in Fig. 3.4 (a), which has no static power consumption [7], monitors $V_{OUT}$ and once it surpasses a certain threshold ($2V_{TP}$), activates a one-shot circuit to turn P$_5$ *On* after a certain delay ($R_mC_m$). Note that the last inverter in the chain must be supplied by $V_{DUM}$ since during the time when $V_{OUT}$ is not yet stable, P$_5$ needs to be kept *Off* by the only stable voltage present on chip, which is $V_{DUM}$. The rectifier startup is simulated in Fig. 3.4 (b). It can be seen that $V_{DUM}$ rises rapidly up to ~3.5 V. However, $V_{OUT}$ catches up in about 20 µs and the output monitor turns P$_5$ *On*, shorting $V_{DUM}$ to $V_{OUT}$. This automatically turns the dummy rectifier (P$_{3,4}$) *Off*.

### 3.3 Measurement Results

A prototype rectifier was designed and fabricated in the AMI 0.5-µm n-well 5 V standard CMOS process through MOSIS. Fig. 3.5 shows the rectifier die microphotograph in which we have maximized the separation between high current...
Fig. 3.4. (a) Schematic diagram of the output voltage monitor. (b) Post-layout transient simulation of the rectifier waveforms at startup.
Fig. 3.5. Die Photo of the rectifier in AMI 0.5 μm CMOS process.

Fig. 3.6. Measured rectifier input and output waveforms when $V_{C1,2}(peak) = 5$ V, $R_L = 1$ kΩ and $C_L = 1$ μF.
carrying P\textsubscript{1,2} and N\textsubscript{1,2} transistors and equipped them with guard rings to reduce the risk of latch-up and substrate leakage [5]. The rectifier occupies \( \sim 0.4 \text{ mm}^2 \) in this process.

To test the rectifier, we setup an inductive wireless link similar to Fig. 3.1 using a pair of planar spiral coils with primary and secondary inductances of 24.3 and 14.8 \( \mu \text{H} \), respectively. The relative distance between the coils was 10 mm, about the average thickness of the skin, and their geometries were optimized for operation at 1 MHz as described in [9]. The coupling coefficient between the coils when they were aligned was measured \( k \approx 0.25 \) using a network analyzer (Agilent E5071B). \( L_1 \) was driven by an HP 8111A function generator, and measurements on \( L_2 \) were done using a multichannel digital oscilloscope (Tektronix DPO-4034). Fig. 3.6 shows the measured rectifier waveforms when \( V_{C1,2}(\text{peak}) = 5 \text{ V}, f = 0.5 \text{ MHz} \), and the rectifier is loaded with \( R_L \parallel C_L = 1 \text{ k\Omega} \parallel 1 \mu\text{F} \).

The measured rectifier performance is shown in Fig. 3.7 in terms of the PCE and \( V_{\text{OUT}} \) vs. \( f \) and \( R_L \) when \( V_{C1,2}(\text{peak}) = 5 \text{ V} \). In the present prototype, we obtained maximum PCE = 84.8\% and \( V_{\text{OUT}} = 4.36 \text{ V} \) around \( f = 0.5 \text{ MHz} \), while PCE was measured above 80\% in the frequency range of 0.125 – 1 MHz. Fig. 3.8 illustrates the effects of \( R_L \) on the PCE and \( V_{\text{OUT}} \) for the present architecture, which also depend on the size of the rectifying elements (\( P_{1,2} \) and \( N_{1,2} \)). For heavy loads, \( R_L < 1 \text{ k\Omega} \), PCE decreases due to the increased voltage drop across \( P_{1,2} \) and \( N_{1,2} \), while the switching duty cycle also increases. For light loads, \( R_L > 1 \text{k\Omega} \), the output power becomes comparable to the rectifier’s internal losses,
Fig. 3.7. Measured rectifier PCE and output DC voltage when $V_{C1,2}(peak) = 5$ V and $C_L = 1 \mu F$ as a function of input carrier frequency ($f$) with output loading ($R_L$) of 1 kΩ.

Fig. 3.8. Measured rectifier output DC voltage when $V_{C1,2}(peak) = 5$ V and $C_L = 1 \mu F$ as a function of input carrier frequency ($f$) with output loading ($R_L$) of 1 kΩ.
hence decreasing the PCE.

To understand Fig. 3.7 in more detail we have performed the following simple analysis, see Fig. 3.9.

\(V_{OUT} = \text{Output DC Voltage (V)}\)

\(T_D = \text{Regeneration Time constant of the comparator (sec)}\)

\(V_H = \text{Hysteresis Window of the comparator (V)}\)

\(\omega_0 = \text{Input sinusoidal frequency (rad/sec)}\)

\(V_i = \text{Input Voltage Amplitude (V)}\)

\(K = \text{Input Voltage Capacitive Division factor}\)

\(T_2 = \text{Time instant when } V_{OUT} \text{ becomes equal to the input voltage (sec)}\)

\(T_1 = \text{Time instant when } V_{OUT} \text{ becomes equal to the divided input voltage (sec)}\)

\(T_3 = \text{Time instant when } (V_{OUT} - V_H/2) \text{ becomes equal to the divided input voltage and the comparator enters into the regenerative mode (sec)}\)

From the above definitions, we can write:

\[T_D = T_2 - T_3 \quad (3.3.1)\]

\[T_1 = \frac{1}{\omega_0} \times \sin^{-1} \left( \frac{V_{OUT}}{KV_i} \right) \quad (3.3.2)\]

\[T_2 = \frac{1}{\omega_0} \times \sin^{-1} \left( \frac{V_{OUT}}{V_i} \right) \quad (3.3.3)\]

\[T_3 = \frac{1}{\omega_0} \times \sin^{-1} \left( \frac{V_{OUT} - V_H/2}{KV_i} \right) \quad (3.3.4)\]

Substituting (4) and (2) in (1), we get,
Fig. 3.9: Waveforms of a rectifier during the half-wave with time stamps indicated.

\[ T_D = \frac{1}{\omega_0} \left[ \sin^{-1} \left( \frac{V_{OUT}}{V_i} \right) - \sin^{-1} \left( \frac{V_{OUT} - \frac{V_H}{2}}{KV_i} \right) \right] \]  \hspace{1cm} (3.3.5)

Eq. (3.3.5) is a relation between the comparator delay, hysteresis, capacitive division, input voltage frequency and amplitude as well as the output DC voltage. \( V_{OUT} \), however, is still a dependant parameter, while the others can be chosen by design. Thus, each one of them affects \( V_{OUT} \) and consequently the PCE in a non-linear fashion. This also makes the design optimization of the comparator extremely complex and needs to be done empirically through simulations.
3.4 Power Dissemination in the Rectifier

A post-layout simulation of the ABTR circuit in Fig. 3.2 was performed to analyze the power distribution in various power dissipating elements in the Rectifier mode when it provides the maximum PCE based on the measurements \(V_2 = 5\, \text{V}, f = 0.5\, \text{MHz}, C_L = 1\, \mu\text{F}, \text{and } R_L = 1\, \text{k}\Omega\). Fig. 3.10 shows the result of this simulation in a pie-chart. The rectifier PCE, obtained by dividing the power delivered to the load by the total input power, was 90.4\%, which is 5.6\% higher than the measured value in Fig. 3.7. We believe that this discrepancy was resulted from the additional parasitic components, which were not included in the rectifier model, especially those from interconnects and measurement instrumentation. In a real application, such as in Interstim-2B [2], since the rectifier block is going to be part of a system-on-a-chip (SoC), its efficiency is likely to be closer to the higher simulated value.

The static dissipation \(P_{\text{STATIC}} = 1.17\%\) in \(P_{1,2}\) driver circuitry \((A_{1,2}\) comparators) and bias generator is the quiescent current supplied from \(V_{\text{OUT}}\). The dynamic power dissipation \(P_{\text{DYNAMIC}} = 1.02\%\) in the rectifier is calculated by subtracting the static power from the total dissipation in the driver circuitry when operating the rectifier. This is consumed mainly in the buffers employed after the comparator blocks to drive large \(P_{1,2}\) switches (see Fig. 3.1). The dissipation in the main rectifying elements \(P_{1,2}\) and \(N_{1,2}\) On-resistance \(P_{\text{SWITCHES}}\) is 7.4\%, i.e. the bottleneck to a highest achievable PCE. This is despite operating these switches in deep triode region. Even though it is possible to reduce \(P_{\text{SWITCHES}}\) by increasing the size of the rectifying elements, it comes at the expense of silicon area and increased parasitic
capacitance of these switches. Hence, there needs to be a compromise between the rectifier size, comparator drive capability, and carrier frequency, which is out of the scope of this paper. A detailed theoretical analysis and optimization of the active integrated CMOS rectifiers can be found in Chapter 5 of the thesis.

3.5 Limits to Rectifier Dropout Voltage

As mentioned in section II, we have introduced a phase-lead when $P_{1,2}$ is being switched $Off$ to account for the comparator delay and eliminate reverse currents [14], [18]. On the other hand, the loss-less capacitive divider also introduces a phase-lag when $P_{1,2}$ is being switched $On$. The comparator delay also adds to this lag and results in a notable reduction in the switching duty cycle. In the present design, for example, the input capacitive divider has a ratio of 0.93, which corresponds to a 350 mV dropout

Fig. 3.10: Pie-chart showing the simulation results of the distribution of input power in the Rectifier at maximum efficiency (90.4%) and nominal loading of $R_L = 1 \, \text{k}\Omega, V_2 = 5 \, \text{V}, f = 0.5 \, \text{MHz}$, and $C_L = 1 \, \mu\text{F}$. 

Power Dissipation Breakup

- P_LOAD
- P_SWITCHES
- P_STATIC
- P_DYNAMIC
- P_MISC
voltage at 5 V input. Thus, a lower dropout can be achieved in this architecture by employing a faster comparator and reducing the phase-lead accordingly.

### 3.6 **Limits to Rectifier Efficiency**

In active rectifiers the comparator characteristics such as delay, power consumption, and output drive capability have a significant effect on the maximum achievable efficiency. To observe the effect of comparator delay on efficiency, we ran simulations on the ABTR post-layout extraction in the same conditions as in section IV.C, while replacing $A_{1,2}$ with ideal comparators that had zero delay, unlimited drive capability, and no power dissipation. $R_L$ was swept in Fig. 3.11 from 10 Ω to 100 kΩ.
similar to the measured results described in Fig. 3.8. The same trend can be observed with the PCE reaching 96.2% for \( R_L = 1 \sim 10 \text{k}\Omega \). This shows that there is only 3.8% power dissipation in the rectifying elements, which is almost half of the amount shown in Fig. 3.7 with realistic comparators that have 33 ns delay.

The reduced power dissipation in the rectifying elements can be attributed to the increased rectifier switching duty cycle, \( D\% \), as a result of eliminating the phase-lead capacitive voltage divider (\( C_{POLY} \) and \( C_{PAR} \) in Fig. 3.2). This in turn reduces the average current passing through \( P_{1,2} \) and \( N_{1,2} \) to replenish the charge in \( C_L \) that is delivered to \( R_L \) in every carrier cycle. \( D\% \) also depends on the \( \tau = R_L C_L \) and affects the \( V_{OUT} \) ripple. Hence, the RC load can also affect the amount of power that is dissipated in the switching elements as can be seen in Fig. 3.11.

### 3.7 Effects of Phase-Lead Control

In this section, we take a closer look at the effects of the phase-lead capacitive divider in the control of back currents from \( C_L \) to the \( L_2C_P \) tank. For this purpose, we built a rectifier model in SPICE using an ideal comparator with adjustable delay, \( T_d \), for both rising and falling edges. Fig. 3.12 compares the PCE for compensated and uncompensated rectifiers vs. \( T_d \). It can be seen that the capacitive phase-lead, described in section 3.2, is quite effective in maintaining a high PCE especially for slower comparators or when the carrier frequency is high and \( T_d \) is comparable to \( T_S \). Fig. 3.13 also shows the required ratio, \( \sigma = C_{POLY}/(C_{PAR} + C_{POLY}) \), that would maximize the PCE for each delay. It should also be noted that increased \( T_d \) results in a slight
As mentioned earlier, the rectifier PCE is quite sensitive to the phase-lead capacitive divider ratio. Fig. 3.13 shows how PCE changes vs. $\sigma$ for a constant delay of $T_d = 10$ ns, and peaks at $\sigma = 0.99$. In practice, process variations and various mismatches can affect $\sigma$. In addition, the comparator rising and falling delays are not necessarily equal. For the latter case, $\sigma$ should be indicated based on the comparator delay at the time of the switch being opened. Further, the comparator being a voltage/current sense-and-amplification device, its delay would always be a function of the input voltage amplitude.

Degradation in the PCE despite phase-lead compensation because of the steady reduction in the switching duty cycle, $D$. 

Fig. 3.12: PCE variation vs. comparator delay, $T_d$, at 1 MHz with and without phase-lead compensation using a capacitive divider with the voltage division ratio shown on the left vertical axis. The capacitive divider is added to the input of the comparator to control the reverse current.
and frequency, as well as the corresponding output voltage level [10]. These effects along with the comparator offset, hysteresis, and dynamic non-idealities can complicate evaluation of the right value for $\sigma$. Therefore, $\sigma$ may need to be empirically adjusted for the chosen comparator topology, and a certain degree of programmability or control via a closed-loop feedback would be desirable.

### 3.8 References


Chapter 4

4. An Active Rectifier with built-in dual-mode Backtelemetry in Standard CMOS Technology

4.1 Introduction

Size-constrained high power implantable microelectronic devices (IMD) such as retinal and cochlear implants, low-cost passive Radio Frequency Identification (RFID) tags, and many wireless sensors cannot accommodate any internal energy sources in the form of batteries due to their low energy density, high cost, and limited lifetime [1]-[6]. There is also a need for data to be transferred from such systems to the outside world which may include the status of the implant, a feedback loop, or other stored or collected information [4], [6]-[12]. In applications where high data rates are not necessary, wireless power and bidirectional data transmission can occur by modulating a single carrier at $f = 1$~$20$ MHz and using load-shift keying (LSK) through an inductive link, as shown in Fig. 4.1. LSK requires either a good coupling between the transponder and reader coils or large variations in the impedance seen across the transponder coil [6], [12].

With the size of the transponder being limited, the small coupling, $M$, between the coils forms a bottleneck in power and data transmission. On the power front, it is imperative for the rectifier to be extremely efficient to convert the small received AC power to DC and present it to the load with minimum dissipation. A more efficient rectifier can deliver a given amount of power for a lesser voltage induced across the secondary coil. Thus it requires a smaller coupling coefficient, $k$, and allows for a greater...
relative distance between the coils. Active rectifiers have been proven to be more efficient compared to their diode-connected passive counterparts in several prior designs [13]-[16]. They also generate less heat for the same amount of power being delivered to the load, keeping the IMD and its surrounding tissue cooler [17].

On the data front, it is important to maximize the changes in transponder impedance variations to compensate for the small coupling coefficient and overcome noise and interference on the reader [6]. Most traditional LSK methods rely on the nominal loading of the transponder to induce the impedance change. If the loading varies over time, which is the case especially in more complex systems, the reading range will be adversely affected because one should always consider the worst-case loading in designing the back telemetry link.
We hereby present a high power conversion efficiency (PCE) active back telemetry rectifier (ABTR), which has built-in dual-mode LSK capability, both open- and short-circuit, enabling transfer of data back to the reader at higher rates or over further distances, while accommodating varying load conditions. This is an improvement over an earlier diode-connected version of this rectifier described in [18].

4.2 Circuit Description

The complete circuit schematic of the ABTR is shown in Fig. 4.2. The rectifier has three modes of operation namely, Rectifier, Short-Coil (SC), and Open-Coil (OC), which are summarized in Table 4.1. When the two ABTR logic inputs are low (OC, SC = 0, 0), the circuit operates as a full-wave rectifier providing an unregulated DC supply to the load. The basic architecture of the rectifier is similar to [18], wherein the main rectifying elements are the pMOS pair, $P_{1,2}$, while the nMOS pair, $N_{1,2}$ provide the current path back to the coil. The bulk potential of $P_{1,2}$ is given by $V_{BC1,2}$, which is dynamically controlled to be connected to the higher of $V_{C1,2}$ and $V_{OUT}$, at all times. This helps minimizing latch-up, body effect, and substrate leakage problems as explained in [19]. However, instead of diode-connecting $P_{1,2}$ for rectification, as we did in [18], leading to dropout voltages across each pMOS above the threshold voltage, $|V_{Tp}|$, here we actively drive the gates of $P_{1,2}$ via a pair of high speed comparators, $A_{1,2}$, to bias $P_{1,2}$ in the deep triode region during conduction. This would result in a significant reduction in the MOS channel resistance and consequently the rectifier dropout voltage [20], [21]. The reader is referred to Chapter 2 of the thesis for a detailed discussion of the rectifier mode.
of operation with measurement results.

In the Short-Coil mode of operation \((OC, SC = 0,1)\), the secondary \(L_2C_2\) tank is shorted by pulling the gates of \(N_{1,2}\) up to the highest on-chip voltage, \(V_{BC1,2}\). This is accomplished through a pair of on-chip level-shifting multiplexers, \(MUX_{5,6}\) (box-3, Fig. 4.2), which can convert any on-chip logic level to \(V_{Body-Ground}\). The small resistance presented across \(L_2C_2\) reduces its quality factor, \(Q_2\), thereby decreasing the voltage across \(L_2\) and the current through it. Since \(V_{C1,2} < V_{OUT}\) in this mode, \(A_{1,2}\) pull the
gates of $P_{1,2}$ high and keep them off. This would eliminate $C_L$ from being discharged through $N_{1,2}$.

In the Open-Coil mode of operation ($OC, SC = 1,0$), $L_2C_2$ is opened by connecting the gates of $P_{1,2,3,4}$ in the main and startup rectifiers to their respective bulk potentials using $MUX_{1,2,3,4}$. This would increase $Q_2$ of $L_2C_2$ tank, increasing the voltage across $L_2C_2$ and the current through $L_2$. Drastic changes in $Q_2$ during $SC$ and $OC$ modes with respect to its nominal value in the rectifier mode, which is dependant on $R_L$, result in similar changes in $L_2$ and $L_1$ currents due to their mutual inductance, $M$ [6]. These changes when captured by a small resistor or a current-sense transformer on the primary side, as shown in Fig. 4.1, can be used to demodulate the power carrier amplitude variations and recover the back telemetry data. Dual-mode back telemetry feature of the proposed rectifier can, therefore, provide more variations in $Q_2$ and enhance the reading range especially in complex systems where $R_L$ is variable.

4.3 Measurement Results
We have developed a prototype chip for the proposed ABTR architecture in the AMI 0.5-µm 3M/2P n-well 5 V standard CMOS process. The die photo is shown in Fig. 4.3, which active area, excluding the pad frame, is ~0.4 mm\(^2\). The rectifier was powered by an HP-8111A function generator through a pair of planar spiral coils fabricated on PCB [22].

The values for the primary and secondary coils were measured \(L_1, R_1 = 24.3 \, \mu H, 2.24 \, \Omega\); and \(L_2, R_2 = 14.4 \, \mu H, 1.56 \, \Omega\), using a high precision LCR meter (Instek-LCR819). \(C_1\) and \(C_2\) were adjusted to resonate at each desired carrier frequency in \(f = 0.1 \sim 2 \, MHz\) range, while the rectifier was loaded with \(R_L = 1 \, k\Omega\) and \(C_L = 1 \, \mu F\). The current flowing into the rectifier was differentially measured across a 10 \(\Omega\) resistor.

![Fig. 4.3: Die photo of the active back telemetry rectifier chip fabricated in AMI 0.5-µm standard CMOS process (0.45 × 0.9 mm\(^2\)).](image-url)
connected in series between $L_2C_2$ and the ABTR input. The connection between $L_1$ and Ground was passed through a current sense transformer ($L_{SEN} = 365 \, \mu H$, $R_{SEN} = 24.8 \, \Omega$), as shown in Fig. 4.1, and the transformer isolated output voltage, called $I_{SEN}$, was directly connected to one of the oscilloscope channels to monitor the changes in $L_1$ current.

Fig. 4.4 shows the measured transient waveforms when the ABTR is operated at $f = 1 \, MHz$ and switched between $OC$, Rectification, and $SC$ modes, consecutively, by changing its digital inputs at 33 kHz. Even though the $SC$ input is not shown, the effect of each rectifier operating mode and changes in $Q_2$ are quite obvious on
Fig. 4.5. Waveforms showing (from top) the original and Manchester-encoded data bit streams, primary sensed current, carrier envelope, and recovered back telemetry data, which was sent through the ABTR OC input at 200 kHz with $f = 1 \text{ MHz}$, $R_L = 1 \text{k}\Omega$ and $d = 20 \text{ mm}$.

$V_{C2}$ and $I_{SEN}$. It can also be seen, from $V_{OUT}$ that $C_L$ exponentially discharges in $R_L$ during OC and SC, and recharges during the normal rectifier operation.

Another observation was that the changes in $V_{C2}$ and $I_{SEN}$ during OC were smaller than those during SC. This was because of the presence of electrostatic discharge protection circuitry, $ESD_{1,2}$ shown in box-1 of Fig. 4.2, as part of the pad-frame structure. These circuits are off during SC mode and normal rectifier operation. However during OC mode, when $Q_2$ increases and $V_{C1,2}$ go beyond the supply rail, $ESD_{1,2}$ turn on and form a leakage path across the rectifier to the $V_{OUT}$ rail and eventually to the load, $R_L$. This
leakage path clamps $V_{CL,2}$ at a diode-drop above $V_{OUT}$ and does not allow $Q_2$ to increase as much as it should.

In order to demonstrate the ABTR back telemetry operation through $SC$ and $OC$ inputs, and evaluate the effect of dual-mode operation on the reading range and bit error rate (BER), we generated a 200 kb/s Manchester-encoded serial data bit stream using a digital I/O card. A sample segment of the original data stream at 100 kb/s and its Manchester-encoded version are shown on traces 1 and 2 of Fig. 4.5, respectively. In this experiment, the nominal coils separation, loading, and carrier frequency were $d = 20$ mm, $R_L = 1$ k$\Omega$, and $f = 1$ MHz, respectively. Data recovery on the primary side involved digitization of $I_{SEN}$ (trace-3 in Fig. 4.5) at 250 MHz using a digital oscilloscope (Tektronix DPO4034) and processing it offline in MATLAB. Zero crossings of $I_{SEN}$ were detected to indicate the carrier signal period and reconstruct the received carrier envelope.

There were two types of amplitude variations at the primary; one at high frequency (200 kb/s) due to the rectifier LSK, and the other at low frequency due to fluctuations in the power amplifier output voltage, coils separation, and other sources of interference. The undesirable low frequency interference was eliminated by running a moving average on $I_{SEN}$, and subtracting it from the carrier envelope information. Thereafter, binarization was performed by checking the peaks of $I_{SEN}$ that were above or below the moving threshold. Comparing the resulting waveform, which is shown on trace-4 of Fig. 4.5, with trace-2 demonstrates the accuracy of the demodulated serial data.
bits. Finally, the original symbols were recovered by Manchester decoding trace-4 via edge detection and retrieval of pulse width information (trace 5).

With this setup in place, the BER was measured by comparing the back scattered and received data bit streams for a total of 2048 bits (256-bit frames in 8 trials). However, no errors were detected. Considering the facts that a dedicated reader was not utilized and the coil dimensions were not optimized, we simply defined the maximum coil separation, $d_{\text{max}}$, that could maintain BER $< 5 \times 10^{-4}$ as the reading range in our test setup. For $R_L = 1 \, \text{k}\Omega$, $d_{\text{max}}$ was 28 and 25 mm for SC and OC modes, respectively. When we reduced $R_L$ to 300 $\Omega$, $d_{\text{max}}$ for SC was reduced to 23 mm, while $d_{\text{max}}$ for OC was increased to 26 mm, despite its subdued operation due to the ESD circuitry. This result was expected because as mentioned in section 4.1, maximizing the transponder impedance variations can improve the reading range in inductively powered devices. Thus, we could conclude that when $R_L$ was variable, a combination of SC and OC modes increased the reading range in our experimental setup by 12% compared to using only one of these modes similar to the traditional LSK scheme.

4.4 Variations in loaded $Q_2$ in different modes of operation

We talked about variations in the secondary Q-factor when the ABTR changes the $L_2C_2$ tank loading in its 3 modes of operation. Here we would like to understand how $Q_{2L}$ (loaded $Q_2$) changes and in what range. This in turn depends on the linearized equivalent resistance, $R_{Leq}$, seen through the rectifier input port. Direct measurement of $Q_{2L}$ and $R_{Leq}$ during ABTR operation is not feasible. Therefore, we
calculated them indirectly from other measurable parameters in the setup shown in Figs. 4.1 and 4.2. A straightforward set of measurable values could be the voltages across $L_1$ and $L_2$, which are named $V_1$ and $V_2$, respectively, when other variable parameters such as $f$, $M$, and $R_L$ are held constant. Obviously, $V_2 = V_{C1} - V_{C2}$ needs to be measured differentially in order not to disturb the transponder isolation from the reader.

To find the relationship between $(V_1, V_2)$ and $(Q_{2L}, R_{Leq})$, we have further simplified the schematic diagram of Fig. 4.2 to the equivalent circuit model in Fig. 4.6. Here is how $Q_{2L}$ is defined,

\begin{align}
Q_L &= \omega C_2 R_{L,eq} \tag{4.4.1} \\
Q_2 &= \frac{\omega L_2}{R_2} \tag{4.4.2} \\
Q_{2L} &= Q_2 \parallel Q_L = \frac{Q_2 Q_L}{Q_2 + Q_L} \tag{4.4.3}
\end{align}
where, $Q_L$ is the load Q-factor and $Q_2$ is the unloaded Q-factor of $L_2$. It is also possible to find the voltage transfer function across the inductive link, $F_V = |V_2(j \omega)/V_1(j \omega)|$, which derivation is given in the appendix, assuming $Q_L^2 >> 1$ [23].

We can write the KVL equations for the currents in $L_1$ and $L_2$, shown as $I_1$ and $I_2$, respectively.

$$I_2(j \omega) = \frac{-j \omega M I_1(j \omega)}{R_2 + j \omega L_2 + Z_{L, eq}(j \omega)} \quad (4.4.4)$$

$$I_1(j \omega) = \frac{V_1(j \omega)}{R_1 + j \omega L_1 + \frac{1}{j \omega C_1} + Z_{R}(j \omega)} \quad (4.4.5)$$

where $Z_R$ is the reflected impedance on to the primary [23],

$$Z_R(j \omega) = \frac{j \omega M I_2(j \omega)}{I_1(j \omega)} \quad (4.4.6)$$

$$\Rightarrow Z_R(j \omega) = \frac{(\omega M)^2}{R_2 + j \omega L_2 + Z_{L, eq}(j \omega)} \quad (4.4.7)$$

The secondary coil voltage is related to its current by,

$$V_2(j \omega) = -I_2(j \omega) \times Z_{L, eq}(j \omega) \quad (4.4.8)$$

Assuming $Q_L^2 >> 1$ and that the primary and secondary tanks are often tuned at the carrier frequency, we can substitute (8) in (14) and reach at,

$$Z_R(j \omega) = \frac{(\omega M)^2}{R_2 + \frac{Z_{L, eq}(j \omega)^2}{R_{L, eq}}} \quad (4.4.9)$$

Using this in (10) and (11) leads to,
\[ I_2(j \omega) = \frac{-j \omega M I_1(j \omega)}{R_2 + \frac{|Z_{L, eq}(j \omega)|^2}{R_{L, eq}}} \] 

(4.4.10)

\[ \Rightarrow I_1(j \omega) = \frac{V_1(j \omega)}{R_1 + \frac{|Z_{L, eq}(j \omega)|^2}{R_{L, eq}}} \] 

(4.4.11)

Using (14)-(17), we can write the voltage transfer function as,

\[ \frac{V_2(j \omega)}{V_1(j \omega)} = \frac{j \omega M \times Z_{L, eq}(j \omega)}{R_1 \left( R_2 + \frac{|Z_{L, eq}(j \omega)|^2}{R_{L, eq}} \right) + (\omega M)^2} \] 

(4.4.12)

\[ \frac{V_2(j \omega)}{V_1(j \omega)} = \frac{j \omega M \times R_{L, eq} \times Z_{L, eq}(j \omega)}{(R_1 R_2 + (\omega M)^2) \times R_{L, eq} + R_1 \times |Z_{L, eq}(j \omega)|^2} \] 

(4.4.13)

Taking the magnitude of the above equation,

\[ \left| \frac{V_2(j \omega)}{V_1(j \omega)} \right| = \frac{(\omega M) \times R_{L, eq} \times |Z_{L, eq}(j \omega)|}{(R_1 R_2 + (\omega M)^2) \times R_{L, eq} + R_1 \times |Z_{L, eq}(j \omega)|^2} \] 

(4.4.14)

Substituting (8) and rearranging (20),

\[ \left| \frac{V_2(j \omega)}{V_1(j \omega)} \right| = \frac{(\omega M) \times R_{L, eq} \times \sqrt{1 + (\omega C_2 R_{L, eq})^2}}{(R_1 R_2 + (\omega M)^2) \times (1 + (\omega C_2 R_{L, eq})^2) + R_1 R_{L, eq}} \] 

(4.4.15)

Since \( Q_L^2 \gg 1 \), (21) can be simplified further to give,

\[ \left| \frac{V_2(j \omega)}{V_1(j \omega)} \right| = \frac{(\omega M) \times R_{L, eq} \times \omega C_2}{(R_1 R_2 + (\omega M)^2) \times R_{L, eq} \times (\omega C_2)^2 + R_1} \] 

(4.4.16)
Hence, we can now write the final expression for the voltage transfer function from the primary to the secondary.

\[
F_V = \frac{V_2(j\omega)}{V_1(j\omega)} = \frac{\omega^2 M C_2 R_{L,eq}}{R_{L,eq}(R_1 R_2 + (\omega M)^2)(\omega C_2)^2 + R_1}.
\]  

(4.4.17)

If we calculate \( F_V \) from measured or simulated \((V_1, V_2)\), then the above equation can be solved for \( R_{L,eq} \) to give,

\[
R_{L,eq} = \frac{R_1}{\sqrt{\frac{\omega^2 M C_2}{F_V} - \left\{ (R_1 R_2 + (\omega M)^2 \times (\omega C_2)^2 \right\}}}.
\]  

(4.4.18)

We combined the realistic off-chip component and parasitic values from the test setup described in section 4.3 with post-layout extracted ABTR model in SPICE to simulate \( F_V \) at \( k = 0.1 \) and \( f = 1 \) MHz. Table 4.2 summarizes the \( Q_{2L} \) and \( R_{Leq} \) variations in different modes of ABTR operation.

It can be seen that \( Q_{2L} \) changes in a wide range and \( Q_L^2 >> 1 \) assumption holds true with \( R_L = 1 \) k\(\Omega\) in the Rectifier and OC modes, where (4) and (5) will be valid, but not the SC mode. With this setup, we have also simulated \( Q_{2L} \) and \( R_{Leq} \) when the ESD protection circuits are not present and there are no undesired leakage currents to \( R_L \) in the OC mode (in a high voltage process for example). It can be seen that \( Q_{2L} \) in this case is increased and extended \( \Delta Q_{2L} \) with respect to the Rectifier mode even further. This would results in easier back telemetry data demodulation and extended reading range. It should also be noted that with heavier loading, i.e. lower \( R_L \), \( Q_{2L} \) tends to decrease in the Rectifier mode, while it stays the same in the OC mode, thereby increasing \( \Delta Q_{2L} \).
$Q_{2L}$ for the SC or the Rectifier modes with small $R_L$ cannot be computed using (4) and (5) since $Q_L \leq 1$. In this case Fig. 4.6 should be analyzed or simulated without the simplifications discussed in the appendix. According to the simulations using the typical model in the AMI 0.5-μm CMOS process, the effective resistance of $N_{i,2}$ across $L_2$ is ~3 Ω for a gate voltage of 3 V. Hence, the resulting $Q_{2L}$ is 0.03 for this mode of operation, which results in a larger $\Delta Q_{2L}$ if $R_L = 1 \text{kΩ}$ compared to the OC mode.

### 4.5 Reflected Impedance in Backtelemetry

The reflected impedance on to the primary side, $Z_R$, is the key parameter in back telemetry and a function of the impedance at the secondary, $Z_2$ in Fig. 4.6. It is given by:

$$Z_R(j\omega) = \frac{(\omega M)^2}{Z_2(j\omega)} \quad (4.5.1)$$

$$Z_2(j\omega) = R_2 + j\omega L_2 + Z_{L, eq}(j\omega) \quad (4.5.2)$$

$$Z_{L, eq}(j\omega) = \frac{R_{L, eq}}{j\omega C_2 R_{L, eq} + 1} \quad (4.5.3)$$

Using (3.4.1), $Z_2$ in (3.4.2) can be converted to a more useful form,
Fig. 4.7 shows how the imaginary and real parts of the transponder impedance, $Z_2$, and its loaded quality factor, $Q_{2L}$, vs. the linearized resistance seen through ABTR input port $R_{L(eq)}$ in Fig. 4.6.

$$Z_2(j\omega) = \left( R_2 + \frac{R_{L(eq)}}{Q_c^2 + 1} \right) + j \left( \omega L_2 - \frac{1}{\omega C_2} \left( \frac{Q_c^2}{Q_c^2 + 1} \right) \right).$$

(4.5.4)

Fig. 4.7 shows how the imaginary and real parts of $Z_2$ change as $R_{L(eq)}$ varies from short to 1 kΩ in our setup at $f = 1$ MHz. Fig. 4.7 also shows how $|Z_2|$ and $Q_{2L}$ change with $R_{L(eq)}$. It can be observed that when $Q_{2L}^2 > 10$ ($Q_{2L} > 3.2$), which corresponds to $R_{L(eq)} > 313$ Ω, the imaginary part of $Z_2$ will be negligible at resonance. In this region, which includes the
Rectifier and OC modes of operation according to Table 4.2, an increase in $R_{L,eq}$ (e.g. when switching from Rectifier to OC) results in a reduction in $Z_2$, an increase in $Z_R$, and a reduction in $I_1$. This is evident in Fig. 4.4 waveforms. On the other hand, when $Q_{2L} < 1$ (e.g. switching from Rectifier to SC), $Z_2$ is highly inductive and largely contributed by the inductance of $L_2$. Similarly, $Z_R$ will be highly reactive and therefore, results in both amplitude and phase modulation on the primary side.

It can also be inferred from Fig. 4.7 that for very small values of $R_{L,eq}$ there is a complete dominance of $L_2$ and any changes in $R_{L,eq}$ would produce little change in $Z_2$. The real part of $Z_2$ peaks at $R_{L,eq} = \omega L_2$, which corresponds to $Q_{2L} = 1$. Therefore,
for heavily loaded transponders that result in $R_{L,eq} < \omega L$, the existence of the OC mode in the proposed ABTR seems to be an effective way in extending the reading range. It is also instructive to look at the locus curve of the reflected impedance in different ABTR modes of operation, which are shown in Fig. 4.8 for our experimental setup. Reducing $R_{L,eq}$ reduces the resistive component of $Z_R$ (moving from right to left), resulting in load modulation [6].

4.6 References


Chapter 5

5. Analysis and Design of an Active Rectifier in Standard CMOS Technology

5.1 Introduction

In Chapter 3, a high efficiency rectifier was presented in standard CMOS technology for AC-DC conversion in applications like Radio frequency identification (RFID), Implantable Microelectronic Devices (IMD), and wireless sensors. However, it was observed that the rectifier was limited in terms of its maximum operation frequency which was measured to be $\sim 2$ MHz. A few research groups have proposed different methods to address these issues in their IC-rectifier designs [1] - [4]. However there is still a lack of detailed analysis and deep understanding about how these IC-rectifiers work and what parameters affect their performance the most. This knowledge is necessary in design and development of new SoC ASICs for the aforementioned applications. To the best of the author’s knowledge, there has been a lack of analytical discussion of such a system in standard textbooks.

In this chapter we explain the analysis, design, and implementation of a synchronous full-wave CMOS rectifier with minimized dropout voltage through active biasing of the main conducting MOSFETs in the deep triode region, eliminating the body effect, and decreasing the reverse and substrate leakage currents. A detailed discussion of how to model and optimize various rectifier design parameters is provided. In addition, we have considered the effects when moving to higher frequencies of operation in the ISM band $\sim 13.56$ MHz. A higher frequency of operation has two
benefits. Firstly, the efficiency of an inductive link increases with increase in quality factor of primary and secondary inductors as a linear proportionality, which is critical for biomedical implants [5]. Secondly, it increases the bandwidth of the Backtelemetry data transfer. However, it will be later learnt that a higher frequency of operation constrains the active rectifier design in a momentous way.

5.2 Triangular Waveform Approximation

A simplified equivalent circuit of a rectifier can be represented by a switch connecting a sinusoidal voltage source to an RC load whenever $V_{IN} > V_{OUT}$ as shown in Fig. 5.1. A series resistor, $R_s$, represents the switch parasitic resistance during conduction. The switch off resistance is considered infinite in this simple model. If we ignore the switching delay and assume that the output peak-to-peak ripple, $\Delta V$, is small compared to $V_{OUT}$, the charging and discharging of $C_L$, which are sine and exponential functions, respectively, can be approximated with linear functions and represented by the triangular
The charge acquired by $C_L$ when the switch is closed is given by,

$$Q_{CH} = C_L \cdot \Delta V = (I_{RS} - I_{RL}) \cdot D \cdot T_S$$  \hspace{1cm} (5.2.1)

where $I_{RS}$ is the average current flowing through the switch, $I_{RL} = V_{OUT}/R_L$ is the average current flowing through $R_L$, $D$ is the rectifier switching duty cycle, and $T_S$ is 100% or 50% of the period of the input sinusoid ($1/f$) in half- or full-wave rectifiers, respectively.

Similarly, the charge lost by $C_L$ when the switch is open is given by,

$$Q_{DISCH} = C_L \cdot \Delta V = I_{RL} \cdot (1 - D) \cdot T_S$$  \hspace{1cm} (5.2.2)

At steady state, the amount of charge gained and lost by $C_L$ are equal, and by equating (5.1) and (5.2),
\[ I_{RS} = \frac{V_{OUT}}{D \cdot R_L} \]  

(5.2.3)

Using this simple model, we can approximate the average output power and the power dissipated in \( R_s \),

\[ P_{OUT} = I_{RL}^2 \cdot R_L, \]  

(5.2.4)

\[ P_{DISS} = I_{RS}^2 \cdot R_S \cdot D. \]  

(5.2.5)

Hence, the rectifier PCE is given by

\[ \eta = \frac{P_{OUT}}{P_{DISS} + P_{OUT}} = \frac{I_{RL}^2 \cdot R_L}{I_{RS}^2 \cdot R_S \cdot D + I_{RL}^2 \cdot R_L}. \]  

(5.2.6)

Substituting \( I_{RL} \) and \( I_{RS} \) in (5.6),

\[ \eta = \frac{1}{1 + \frac{R_S}{D \cdot R_L}}. \]  

(5.2.7)

An obvious conclusion from (5.2.7) is that the PCE increases by reducing the switch parasitic resistance, \( R_s \). In our prototype implementation, we have tried to achieve this by biasing the switching MOSFETs in deep triode region, where they show the lowest resistance. A less intuitive insight from this simple model is that the PCE is also a function of \( R_L \) and the rectifier duty cycle, \( D \), which in turn depends on the ripple rejection filter, \( C_L \), and other circuit parameters. An increase in \( D \) tends to increase the PCE, which explains why a full-wave rectifier is preferred over a half-wave one. In the next section, we find the relationship between the rectifier duty cycle, \( D \), and other rectifier circuit parameters.
5.3 Rectifier Differential Equations

The IC-rectifier PCE can be modeled using the 1st order differential equations that describe the simple equivalent circuit in Fig. 5.1 when the switch is open or closed. In Fig. 5.3, a more realistic charging and discharging sequence for \( C_L \) has been depicted with the time reference, \( t = 0 \), set at a zero-crossing of the input sine wave. At \( t = t_0 \), the switch closes and \( C_L \) charges till \( t = t_0 + DT_S \). From this time onward, the switch opens and \( C_L \) exponentially discharges till \( t = t_0 + T_S \). At steady state,

\[
V_{OUT}(t_0) = V_{OUT}(t_0 + T_S) \tag{5.3.1}
\]

\[
V_{OUT}(t_0 + T_S) = V_{OUT}(t_0 + DT_S) \cdot \exp\left(-\frac{(1-D)T_S}{R_C C_L}\right) \tag{5.3.2}
\]

Therefore,

\[
V_{OUT}(t_0 + DT_S) = V_{OUT}(t_0) \cdot \exp\left(\frac{(1-D)T_S}{R_C C_L}\right). \tag{5.3.3}
\]

This is a relation between the initial and final \( V_{OUT} \) during \( C_L \) charging phase. For this phase, we can write the following differential equation using KCL at the output node,

\[
\frac{V_{IN}(t) - V_{OUT}(t)}{R_S} = \frac{V_{OUT}(t)}{R_L} + C_L \frac{dV_{OUT}(t)}{dt} \tag{5.3.4}
\]

where \( V_{IN} \) is the AC input sine wave given by,

\[
V_{IN}(t) = V_{C1}(t) - V_{C2}(t) = V_i \sin(\omega t). \tag{5.3.5}
\]

Solving this equation for \( V_{OUT} \) gives,

\[
V_{OUT}(t) = A_i \sin(\omega t - \theta) + K \times e^{\xi(t - t_0)} \tag{5.3.6}
\]
where,

\[ \omega_0 = \frac{2\pi}{T_s}, \quad \theta = \tan^{-1} \left( \frac{\omega_0 R_{SW} C_L}{1 + R_{SW}/R_L} \right), \quad \xi = \frac{-1}{C_L \times (R_{SW} \parallel R_L)} \]

\[ A_i = \frac{V_i}{\sqrt{\left(1 + \frac{R_{SW}}{R_L}\right)^2 + \left(\omega_0 R_{SW} C_L\right)^2}} \]

\[ K = V_{OUT}(t_0) - A_i \sin(\omega_0 t_0 - \theta) \]
The comparator firing angle, \( t_0 \), is another dependent parameter, which can be found with the assumptions that the comparator has negligible delay, offset, and hysteresis. Thus, as soon as \( V_{IN} \) crosses \( V_{OUT} \), the switch changes its position,

\[
V_{OUT}(t_0) = V_i \sin(\omega_0 t_0) \tag{5.3.7}
\]

\[
V_{OUT}(t_0 + DT_s) = V_i \sin(\omega_0 t_0 + DT_s) \tag{5.3.8}
\]

Making use of (5.3.2)-(5.3.8), we can arrive at two equations that relate \( t_0 \) and \( D \), to other circuit parameters,

\[
\cot(\omega_0 t_0) = \frac{(1-D)T_s}{e^{\frac{R_s C_L}{V_i}} - \cos(\omega_0 DT_s)} \sin(\omega_0 DT_s) \tag{5.3.9}
\]

\[
\cot(\omega_0 t_0) = \frac{\frac{V_i}{A_i} \left( \frac{(1-D)T_s}{e^{\frac{R_s C_L}{V_i}} - e^{\bar{\xi} DT_s}} - e^{\bar{\xi} DT_s} \cos(\theta) - \cos(\omega_0 DT_s - \theta) \right) - e^{\bar{\xi} DT_s} \cos(\theta)}{\sin(\omega_0 DT_s - \theta) - \sin(\theta) e^{\bar{\xi} DT_s}} \tag{5.3.10}
\]

It is also possible to eliminating \( t_0 \) from the above equations by simply subtracting them to find \( D \),

\[
f(D) = 0. \tag{5.3.11}
\]

\( f(D) \) is a nonlinear function and difficult to solve in a closed form. However, it can be solved numerically as shown in Fig. 5.4 where \( f(D) \) is evaluated in the range, \( 0 < D < 0.5 \), for a half-wave rectifier with \( R_L = 1 \, k\Omega \), \( R_S = 5 \, \Omega \), and \( C_L = 1 \, \text{nF} \). Fig. 5.4 shows that the solution to (5.3.11) in this condition is \( D = 0.21 \), which is also verified in SPICE
simulations. Once having $D$ and $t_0$, finding PCE would be straight forward.

5.4 A comparison between methods

We described an approximate closed-form expression for PCE in section 5.2 and a numerical platform for the rectifier waveforms based on differential equations in section 5.3. Here we call the PCE resulted from these methods $PCE-\text{Aprx}$ and $PCE-\text{Num}$, respectively, and compare them with the PCE resulted from circuit simulation in SPICE, $PCE-\text{Sim}$. Our purpose is to validate and compare the accuracy of our PCE calculation models using the simulator as the gold standard.
We simulated the half-wave rectifier of Fig. 5.1 with $V_i = 5 \text{ V}$ at 1 MHz and an ideal comparator of negligible delay (< 1 ns) controlling the switch that has $R_S = 5 \Omega$. For $PCE$-$Aprx$, $D$ is obtained from SPICE simulations first, and then fed into (5.2.7).

Fig. 5.5 shows $PCE$ and $D$ when $C_L = 1 \mu\text{F}$ and $R_L$ is swept from 10 Ω to 100 kΩ, Fig. 5.6 shows the same when $R_L = 1 \text{kΩ}$ and $C_L$ is swept from 100 pF to 100 µF, and in Fig. 5.7, $R_L = 1 \text{kΩ}$, $C_L = 1 \mu\text{F}$, and $R_S$ is swept from 1 Ω to 100 Ω. It can be seen that despite some minor differences, both approximation and numerical methods give accurate results in the practical range of interest. It can also be observed that $PCE$-$Aprx$ often gives an
optimistic estimate of the PCE.

5.5 NMOS and PMOS Switch-Size Optimization

Once given the nominal RC load and $V_{IN}$, one can design an IC-rectifier based on two different scenarios. Firstly, a IC-rectifier with minimum possible silicon area that can provide a desired PCE. Secondly, a IC-rectifier with optimized switch-sizes for a given area on silicon that achieves the highest possible PCE. Considering 5.2.7 and Fig. 5.7, it is obvious that $R_s$ needs to be minimized in both cases. In the full-wave IC-rectifier of Fig. 3.1, the PMOS and the NMOS transistors $P_1$-$N_2$ and $P_2$-$N_1$ connect in

![Diagram showing Power Conversion Efficiency vs. Duty Cycle for different CL values.]

Fig. 5.6. Comparing closed form approximation, numerical differential equations, and SPICE simulation methods for evaluating the rectifier PCE vs. $C_L$. Nominal values are $C_L = 1 \, \mu F$, $R_L = 1 \, k\Omega$, and $R_s = 5 \, \Omega$. 

series in the main current path during each half-wave conduction cycle. Thus $R_s$ would be the sum of their resistances while they operate in the triode region.

Two constraints for area and switch resistance can be given by the following equations:

$$A = L \cdot (W_P + W_N), \quad (5.5.1)$$

$$R_s = L \cdot \left[ \frac{1}{K_P \cdot W_P \cdot (V_{OUT} - V_{THP})} + \frac{1}{K_N \cdot W_N \cdot (V_{OUT} - V_{THN})} \right] \quad (5.5.2)$$

where,

$A$ = Area of the half-wave structure (mm$^2$)

$K_P = \mu_P C_{ox}$, $K_N = \mu_N C_{ox}$ (A/V$^2$)

$W_P$, $W_N$ = Width of the PMOS and NMOS switches (mm)
$L =$ Length of the MOSFET switches (mm)

$V_{THP}, V_{THN} =$ Threshold voltages of PMOS and NMOS (V)

Our assumptions are; the NMOS and PMOS gate drives are close to $V_{OUT} > |V_{THP}|$ and $V_{THN}$ during conduction such that they are biased in deep triode region, and all MOSFET switches have the same length ($L$), which can be the minimum length allowed by the fabrication technology as long as their breakdown voltage is not a concern

5.5.1 Minimizing Area for a given Switch Resistance

In this case, we attempt to minimize (5.5.1) with $W_P$ and $W_N$ as variables keeping other parameters constant. $W_N$ can be evaluated from (5.5.2) and substituted in (5.5.1),

$$A = L \cdot W_P + \frac{L^2}{K_N \cdot (V_{OUT} - V_{THN}) \cdot \left[ R_S \cdot \frac{L}{K_P \cdot W_P \cdot (V_{OUT} - |V_{THP}|)} \right]}$$

(5.5.3)

This expression can be written in a simpler form,

$$A = L \cdot \left( W_P + 1 \left[ K_1 - \frac{K_2}{W_P} \right] \right),$$

(5.5.4)

by defining,

$$K_1 = \frac{R_S \cdot K_N \cdot (V_{OUT} - V_{THN})}{L},$$

(5.5.5)

$$K_2 = \frac{K_N}{K_P} \left( \frac{V_{OUT} - V_{THN}}{V_{OUT} - |V_{THP}|} \right),$$

(5.5.6)

(5.5.4) gives the area as a function of the independent parameter $W_P$, and hence can be differentiated w.r.t. $W_P$ to find the minima for the function.
\[
\frac{\delta A}{\delta W_P} = L - L \times \left[ K_1 \frac{K_2}{W_P} \right]^{-2} \times \left( \frac{K_2}{W_P^2} \right) = 0
\]  
(5.5.7)

The choice of \( W_P \) must ensure that the resistance of the PMOS switch is smaller than the total switch resistance, \( R_S \). Thus,

\[
\left[ K_1 - \frac{K_2}{W_P} \right] > 0
\]  
(5.5.8)

With (5.5.8) being true for all values of \( W_P \) in the desired range, it is easy to show the root of (5.5.7) is the local minima by the second derivative test. We can now calculate \( W_P \) from (5.5.7) to be,

\[
\left[ K_1 - \frac{K_2}{W_P} \right]^{-2} = \left( \frac{W_P^2}{K_2} \right)
\]  
(5.5.9)

We can take the square root and retain only the positive terms since neither LHS nor RHS can be negative (from (5.5.8)). Thus,

\[
W_P = \left( \frac{K_2 + \sqrt{K_2}}{K_1} \right).
\]  
(5.5.10)

Substituting (5.5.5) and (5.5.6) in (5.5.7) we get,

\[
W_P = \frac{L}{K_P \cdot R_S \cdot (V_{OUT} - V_{THP})} + \frac{L}{R_S \sqrt{(K_P \cdot (V_{OUT} - V_{THN}) \cdot (K_P \cdot (V_{OUT} - V_{THP}))}}
\]  
(5.5.11)

Rearranging (5.5.8) and substituting (5.5.6), we get,

\[
R_S = \frac{L}{K_P \cdot W_P \cdot (V_{OUT} - V_{THP})} + \frac{L}{W_N \cdot K_N \cdot (V_{OUT} - V_{THN}) \cdot \left( \frac{W_P}{W_N} \right) \cdot \frac{1}{\sqrt{K_2}}}
\]  
(5.5.12)

Comparing (5.5.9) with (5.5.2) readily gives,
(5.5.13) provides a useful guideline on how to choose the size of the PMOS and NMOS switches in an IC-rectifier to achieve the minimum area for a given \( R_s \).

5.5.2 Minimizing Switch Resistance for a given Area

In this case, we attempt to minimize (5.5.2) with \( W_P \) and \( W_N \) as variables keeping other parameters constant. For this, we can evaluate \( W_N \) from (5.5.1),

\[
W_N = \left( \frac{A}{L} - W_P \right) > 0
\]  

(5.5.14)

Substituting in (5.5.2) we get,

\[
R_s = L \times \left[ \frac{1}{(K_P \times W_P \times (V_{OUT} - V_{THP}))} + \frac{1}{(K_N \times (V_{OUT} - V_{THN})) \times \left( \frac{A}{L} - W_P \right)} \right]
\]  

(5.5.15)

We can thus calculate the stationary point for the function given by (5.5.15) by taking the first derivative.

\[
\frac{\partial R_s}{\partial W_P} = L \times \left[ -\frac{1}{(K_P \times W_P^2 \times (V_{OUT} - V_{THP}))} + \frac{1}{(K_N \times (V_{OUT} - V_{THN})) \times \left( \frac{A}{L} - W_P \right)^2} \right] = 0
\]  

(5.5.16)

The second derivative can easily be seen to be positive for all values of \( W_P \), hence proving the solution of (5.5.16) to be minima. Solving (5.5.16) we get,
\[ AR_{\text{opt}} = \left( \frac{W_P}{W_N} \right)_{\text{opt}} = \frac{W_P}{\left( \frac{A}{L} - W_P \right)} = \sqrt{\frac{K_N \times (V_{\text{OUT}} - V_{\text{THN}})}{K_P \times (V_{\text{OUT}} - V_{\text{THP}})}} \]  \hspace{1cm} (5.5.17)

It can be seen that (5.5.17) is the same as (5.5.13), proving that both the cases have the same condition for optimality. Interestingly, the resulting optimal \( W_P \) for minimizing \( R_S \) when the area is given results in the same \( (W_P/W_N)_{\text{opt}} \) ratio as in (5.5.10), confirming that in fact the same conditions apply to both aforementioned design scenarios. Hence, we can conclude that choosing \( (W_P/W_N)_{\text{opt}} \) based on (5.5.10) results in minimum rectifier area and switch resistance.

As an example, we designed a rectifier based on the specifications listed in Table 5.1 from the AMI-0.5 \( \mu \)m standard CMOS process. The optimal ratio, \( (W_P/W_N)_{\text{opt}} \) from (5.5.10) with \( A = 2500 \ \mu \text{m}^2 \) for the half-wave structure came out to be 1.78. Fig. 5.8 shows \( R_S \) plotted using (5.5.12) for \( W_P \) in 0.5 to 4 mm range. It can be seen that \( R_{S_{\text{min}}} = 2.33 \ \Omega \) occurs at \( W_P \approx 2700 \ \mu \text{m} \) and \( W_N \approx 1500 \ \mu \text{m} \). It is also observed that for 1.6 mm < \( W_P < 3.5 \ \text{mm}, R_S < 3 \ \Omega \) and outside this range it increases rapidly.

### Table 5.1

Typical model parameters for AMI-0.5 \( \mu \)m process at room temperature

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum feature length</td>
<td>( L_{P,N} )</td>
<td>0.6 ( \mu )m</td>
</tr>
<tr>
<td>PMOS transconductance parameter</td>
<td>( K_P = \mu_P C_{\text{ox}} )</td>
<td>36.8 ( \mu \text{A/V}^2 )</td>
</tr>
<tr>
<td>NMOS transconductance parameter</td>
<td>( K_N = \mu_N C_{\text{ox}} )</td>
<td>109.6 ( \mu \text{A/V}^2 )</td>
</tr>
<tr>
<td>NMOS threshold voltage</td>
<td>( V_{\text{THN}} )</td>
<td>0.67 V</td>
</tr>
<tr>
<td>PMOS threshold voltage</td>
<td>(</td>
<td>V_{\text{THP}}</td>
</tr>
</tbody>
</table>
In order to find the best possible PCE when only the losses in the rectifier switches are considered, we set up a SPICE model for the full-wave rectifier in Fig. 3.1 using ideal comparators \((A_{1,2})\) to drive the gates of \(P_{1,2}\) with no delay (<1 ns), hysteresis, offset, or power dissipation. It can be seen in Fig. 5.9, where \(W_P\) is swept from 0.5 to 3.5 mm and \(W_N\) is obtained from the area constraint (5.5.11), that \(V_{OUT}\) peaks at \(W_P \approx 2700 \, \mu m\), which agrees with the results shown in Fig. 5.8. The PCE, however, peaks slightly higher at \(W_P \approx 3000 \, \mu m\). We can attribute this change to the effect of a slightly higher switching duty cycle with higher \(W_P\), which can improve the rectifier PCE according to (5.1.7).

![Figure 5.8](image.png)

**Fig. 5.8:** Plot showing the variation of the total switch resistance, \(R_S\), with the choice of the width of the PMOS transistor, for a given area constraint of \(A = 2500 \, \mu m^2\) in AMI-0.5 \(\mu m\) standard CMOS technology (Table 5.1).
Another observation that is important in design and optimization of IC-rectifiers is that $R_S$ is a function of $V_{OUT}$, which is not known \textit{a priori}. Therefore, assuming that the switching transistors’ gate-drive is equal to $V_{C1,2(peak)}$ results in an optimistic estimate for $R_S$, $V_{OUT}$, and PCE. However, since the dropout voltage is small compared to $V_{OUT}$ in this architecture, $V_{OUT} = V_{C1,2(peak)} = V_i$ would be an acceptable estimate in the first design step. Once $V_{OUT}$ is found in simulations, as in Fig. 5.9, it can be used in successive iterations to obtain better $(W_p/W_n)_{opt}$, $R_S$, and PCE estimates.

5.6 A High Frequency Rectifier in Standard CMOS Technology

In section 5.5 we described an approximate analytical expression for the rectifier efficiency assuming that the main source of loss in the rectifier exists in the
MOS switch resistance. This has been verified in the post layout simulation results of the active rectifier in section 3.4, where the switch loss accounted for ~ 80% of total power loss in the full-wave rectifier structure. The dynamic losses were ~ 10% when $f_{IN} = 0.5$ MHz. It can be said that if everything else were to remain the same, the dynamic losses would increase in direct proportionality to the switching frequency ($f \times C \times V^2$). Hence, the efficiency expression must include these losses and the efficiency is given by,

$$\eta = \frac{1}{1 + \frac{R_S}{R_L D} + f_{IN} C_G R_L} \quad (5.6.1)$$

where, $C_G$ is the gate oxide capacitance given by,
One important conclusion from this is that the NMOS should be used for switching since it has a smaller width in an optimized structure. The resulting rectifier core is shown in Fig. 5.11. Thus, the rectifier architecture will remain the same as that described in Fig. 3.1, but now the NMOS switches will be actively driven by the comparators and the PMOS gates will be driven by the complementary coil voltages. Hence, the gate of $P_1$ is driven by $V_{C2}$ and that of $P_2$ by $V_{C1}$. Secondly, the optimal switch size will depend on the frequency of operation. Fig. 5.8 shows the dependence of PCE on the width of PMOS

$$C_G = C_{ox} \times L \times W$$
(W_P) at the ISM band frequency (13.56 MHz), when the NMOS is chosen from the optimal ratio as described in (5.5.17). In our design, we have chosen W_P = 1.5 mm since it can be seen the peak of the efficiency occurs in the range 1 mm – 1.5 mm. Choosing a larger MOSFET results in a lower dropout without significant increase in the area. The corresponding NMOS size would thus be ~ 830 µm.

Another important consideration is the comparator design. It has been observed in the ideal comparator simulations that the switching duty cycle at nominal load would be ~ 5 – 10 ns. Thus, it can be seen that the comparator described in Chapter

Fig. 5.12: A high speed asynchronous comparator driving the NMOS switch in a full-wave rectifier operating at f = 13.56 MHz.
3 would be too slow at such a high frequency. We use the comparator described in [2] for this purpose, with the final schematic as shown in Fig. 5.12. The comparator switches the NMOS N2 On when $V_{C1} > V_{OUT}$ or $V_{C2} < Ground$. The static current in the left branch is controlled by the resistance of $M_5$, which is kept in deep triode region of operation by connecting the gate to $Ground$. In addition, back currents protection is performed by sinking current from the node $VBP$. The switch $S_{BC}$ is activated once $GC_{N2}$ goes high to switch $N_2$ ‘On’. Thus, a voltage offset is created at the input of the comparator and makes the comparator trip before $V_{C1}$ becomes less than the output DC voltage, $V_{OUT}$. The value of $I_B$ is empirically determined and comes out to be equal to ~ 100 $\mu$A for $f = 13.56$ MHz.

It must also be observed that since $V_{C1}$ swings between 0 V and 5 V for a 5 V input, only one of the comparators consumes static power in one half cycle, making the topology extremely energy efficient. With this structure consuming ~ 20 $\mu$A average current and the switch sizes as described, the output DC voltage is ~ 4.65 V for a 5 V input sinusoid at 13.56 MHz. The simulated efficiency for the rectifier is ~ 86 %.

5.7 References


Chapter 6

6. Design of a Switched Capacitor Based Microstimulator

6.1 Motivation

Conventional micro stimulators can be broadly categorized into voltage controlled or current controlled. In voltage controlled stimulation (VCS), a fixed voltage is applied across the electrode and the tissue while in the current controlled stimulation (CCS), a fixed current is made to pass through the stimulating electrode. The VCS is a simplistic mode of stimulation and has high power efficiency when the stimulation voltage is close to the supply voltage. However, it suffers from safety limitations because the amount of charge injected is dependent of the tissue impedance which can vary over time. In CCS, since the amount of current (and hence charge depending on pulse-width) injected is a constant, the safety is ensured. However, the drawback is in terms of power efficiency since a lot of power is wasted across the saturated MOSFET used for stimulation.

In this work, we present the theory and possible implementations of a switched-capacitor based stimulator (SCS) that is capable of combining the safety benefits of the CCS and has energy efficiency comparable to VCS. The underlying idea is to charge a bank of capacitors by harvesting energy directly from the wireless link and use them for providing a fixed amount of stored charge to the tissue. Thus, as a consequence we also propose to eliminate the battery used in current DBS implants, thereby leading to a considerable reduction in the implant size.
6.2 System Specifications

In a typical DBS implant, the frequency of stimulation is set in the range of 130 – 200 Hz to get the desired therapeutic benefits. With typically 4 sites for biphasic stimulation, this means that two complementary capacitors need to be charged in 1.25 ms. The minimum charge per phase requirement in DBS is 1.8 µC. This is considering a 0.06 cm² electrode having a charge density limit ~ 30 µC/cm². The voltage compliance is in the range 2 – 4 V, and it has been observed that voltage above 3.6 V can lead to activation of voltage doubler/tripler circuits within neurotransmitters which can drain unnecessary power from the source [6].

6.3 Fundamental Theory of Operation

In the SCS architecture, the bottleneck in ensuring high energy efficiency would lie with the problem of charging a bank of large capacitors being used for stimulation. If a capacitor were to be charged by switching with an ideal voltage source (Fig. 6.1a), it corresponds to charging in minimum possible time with an exponential settling response [2]. In general, when the switch resistance $R$ is finite, it accounts for the all the power dissipation in the circuit. However, even in the limiting case when $R \rightarrow 0$, the dissipated energy is in the form of electromagnetic radiations (EMR) [3]. In general, the efficiency for this case is,

$$\eta = 1 - e^{-\frac{T}{\tau}} \cdot \frac{1}{2}. \quad (6.3.1)$$
where, $T$ is total charging time and $\tau$ is the RC time constant. It can be seen that with this configuration in place, the efficiency would never exceed 50%.

Charging a capacitor efficiently is considered to be a non-linear optimization problem, with the solution that the voltage profile of the input voltage source be a ramp [2]. This equivalently corresponds to charging with an ideal current source (Fig. 6.1b). The efficiency for this case is given by,
\[
\eta = \frac{1}{1 + \frac{E_{\text{Diss}}}{E_{\text{Out}}}} = \frac{1}{1 + \frac{I_{\text{IN}}^2 RT}{CV_{\text{OUT}}^2}} = \frac{1}{1 + \frac{I_{\text{IN}}^2 RT}{\frac{I_{\text{IN}}^2 T^2}{2C}}}
\]

\[
\Rightarrow \eta = \frac{1}{1 + 2 \frac{T}{\tau}}.
\]

(6.3.2)

It can be easily seen that to achieve 90% efficiency, \( T = 18 \times \tau \). In the limiting case, when \( T \to \infty \), the efficiency approaches 100%. Thus, it means that charging a capacitor to a given voltage with an infinitesimally small current will result in no power loss. This is also known as the **adiabatic charging principle**.

It must now be understood that a MOS based current source has limited voltage compliance. We hereby exploit the properties of an inductor as a voltage independent constant current source, which is also done in most commercial DC-DC converters. The main difference of an magnetically coupled inductor with respect to a DC-DC converter arises from the fact that while the inductor current in the latter is a DC signal (with small ripple), it is a time varying AC signal in the former with the frequency same as the input signal frequency defined by the Power Amplifier (Fig. 2.1).

### 6.4 Charging via Parallel RLC Tank

Fig. 6.2 shows a parallel RLC tank at the secondary, similar to the one used for the rectifier in Chapter 3. In this case, the induced voltage \( V_{\text{IND}} \) is amplified to \( V_2 \), when \( L_2 \) and \( C_2 \) are at resonance, by the quality factor of the secondary coil, \( Q_2 \). This means that to ensure voltage input of \( \sim 5 \text{ V} \), and \( Q_2 \sim 10 \), the induced voltage would only
need to be 500 mV, which is desirable for loosely coupled coils. As discussed in Chapter 4, this would be true only when there is no load connected across the secondary coil. With the introduction of load, or equivalently a means of stealing charge from the tank the voltage $V_2$ will tend to decrease and hence the induced power magnitude would need to be adjusted accordingly. With this concept in mind, we can now describe the complete circuit in Fig. 6.2, which is the half-wave implementation of the Parallel SCS.

Fig. 6.2. Circuit Schematic showing the concept of a half-wave Parallel SCS.
The underlying principle for Parallel SCS is same as that of the voltage rectifier in
Chapter 3, wherein the switch $S_P$ must be turned On when $V_2 > V_{OUTP}$, which is also the
zero voltage switching (ZVS) principle. However, as compared to the previous case,
where the comparator implemented an open loop control led to a steady state output DC
voltage, here the switch is closed for a fixed duration implemented by a one-shot or
monostable multivibrator. This means that only a controlled amount of charge is
transferred from the coil to the output load capacitor. This is done to prevent $V_2$ from
decreasing drastically if the load capacitor becomes a part of the circuit for a long
duration. Hence, it would result in $C_{LP}$ not getting charged to the peak of the input
voltage. An alternate consequence of this would be that in order to charge $C_{LP}$ to ~ 5 V,
the voltage $V_2$ would need to be made much greater than 5 V when no switching is taking
place. This is unacceptable since this voltage should not exceed the maximum $V_{DS}$ or $V_{GS}$
requirements for a given technology (5 V for 2P/3M AMI 0.5 µm CMOS). In our design,
we have ensured that the switching duty cycle is small ~ $T_s/100$ – $T_s/10$. In this case, the
original amplitude on $V_2$ can be restored by adjusting either the input frequency or the
value of $C_2$. In such a scenario, the load capacitor is charged with quantum current
packets in each charging cycle, and when integrated over time tend to mimic a constant
current source charging profile.

6.4.1 Simulation Results

It is possible to simulate the circuit in Fig. 6.2 using explicit differential
equations in MATLAB. When the switch is open, the system is 2$^{nd}$ order while 3$^{rd}$ order
when the switch is closed. We can simplify this by a starting assumption that the switch has zero resistance, in which case the order doesn’t change in the two configurations. Thus, we can define a dummy capacitor $C_T$ which is equal to $C_2$ when the switch is open and equal to $(C_2 + C_{LP})$ when the switch closes when the voltage difference between $C_2$ and $C_{LP}$ is zero. The differential equations can be written considering the KVL around the loop in Fig. 6.2:

$$V_{IND}(t) = L_2 \frac{dI_2(t)}{dt} + I_2(t)R_2 + V_2(t) \quad (6.3.1.1)$$

$$I_2(t) = C_T \frac{dV_2(t)}{dt} \quad (6.3.1.2)$$

Hence,

$$V_{IND}(t) = L_2 C_T \frac{d^2V_2(t)}{dt^2} + R_2 C_T \frac{dV_2(t)}{dt} + V_2(t) \quad (6.3.1.3)$$

The natural response to the above differential equation can either be over-damped (OD), under-damped (UD) or critically damped (CD), based on the values of circuit parameters [4]. These conditions can be mathematically described by evaluating the determinant of the RHS of (6.3.1.3),

$$Det = R_2^2 - 4 \frac{L_2}{C_T} \quad (6.3.1.4)$$

It has been observed that for the practical design of coils fabricated on a PCB, the response is under-damped [5]. This is the case when $Det < 0$. Hence, here we shall describe the equations for an under-damped response. It is left as an exercise to the reader.
to evaluate the response for other cases. The complete response is a superposition of the forced and natural response and is given in the equations that follow.

The voltage across the capacitor in the network \((V_{CT} = V_2)\):

\[
V_{CT}(t) = A \sin(\omega t - \theta) + e^{\delta t} \times \left[K_1 \sin(\omega t) + K_2 \cos(\omega t)\right]
\] (6.3.1.5)

where,
\[ V_{BD}(t) = V_i \sin(\omega_0 t), \quad A_i = \frac{V_i}{\sqrt{(1 - \omega_0^2 L_2 C_T)^2 + (\omega_0 R_2 C_T)^2}}, \quad \theta = \tan^{-1}\left(\frac{\omega_0 R_2 C_T}{1 - \omega_0^2 L_2 C_T}\right) \]

\[ \omega_0 = \frac{2\pi}{T}, \quad \xi_0 = -\frac{R_2}{2L_2}, \quad \omega_n = \sqrt{\frac{1}{L_2 C_T} - \xi_0^2} \]

\( K_1 \) and \( K_2 \) are natural response parameters that depend on initial conditions of inductor current \( (I_{CT} = I_{L2}) \) and capacitor voltage. These can be evaluated as,

\[
K_1 = f(V_{CT_0}) \frac{e^{-\xi_0 \omega_0}}{\omega_0} \left[ \omega_0 \sin(\omega_0 t_0) - \xi_0 \cos(\omega_0 t_0) + \frac{e^{-\xi_0 \omega_0}}{\omega_0} g(I_{L2_0}) \cos(\omega_0 t_0) \right] (6.3.1.6)
\]

\[
K_2 = f(V_{CT_0}) \frac{e^{-\xi_0 \omega_0}}{\omega_0} \left[ \xi_0 \sin(\omega_0 t_0) + \omega_0 \cos(\omega_0 t_0) - \frac{e^{-\xi_0 \omega_0}}{\omega_0} g(I_{L2_0}) \sin(\omega_0 t_0) \right] (6.3.1.7)
\]

where \( t_0 \) is the time instant of switching. \( f \) and \( g \) are overdrive coefficients for voltage and current respectively, that drive the natural response (NR). This is to say that if the initial condition becomes equal to the forcing function at time \( t_0 \) the NR will cease to exist and a steady state condition would be achieved.

\[ f(V_{CT_0}) = V_{CT_0} - A \sin(\omega_0 t_0 - \theta) \quad (6.3.1.8) \]

\[ g(I_{CT_0}) = I_{CT_0} \frac{\omega_0}{C_T} - A \omega_0 \cos(\omega_0 t_0 - \theta) \quad (6.3.1.9) \]

We can now evaluate the complete expression for the voltage across the capacitor:

\[
V_{CT}(t) = A \sin(\omega_0 t - \theta) + f(V_{CT_0}) \frac{e^{-\xi_0 \omega_0}}{\omega_0} \left[ -\xi_0 \sin(\omega_0 \Delta t) + \omega_0 \cos(\omega_0 \Delta t) \right] + \frac{e^{-\xi_0 \omega_0}}{\omega_0} g(I_{L2_0}) \sin(\omega_0 \Delta t) \quad (6.3.1.10)
\]

The current through the inductor (or the equivalent capacitor in the network, \( C_T \)):
The simulation results are shown in Fig. 6.3 wherein the switch gets activated as soon as the output voltage becomes equal to the input voltage for a time $T_{SW}$. The energy profile

$$\frac{I_{CT}(t)}{C_T} = A \omega_0 \cos(\omega_0 t - \theta) + g(I_{CT0}) e^{i \omega_T t} \left[ \xi_0 \sin(\omega_0 \Delta t) + \omega_0 \cos(\omega_0 \Delta t) \right] - \frac{(\xi^2 + \omega^2) e^{i \omega_T t}}{\omega_0} f(V_{CT0}) \sin(\omega_0 \Delta t)$$

(6.3.1.11)

where, $\Delta t = t - t_0$.

The simulation results are shown in Fig. 6.3 wherein the switch gets activated as soon as the output voltage becomes equal to the input voltage for a time $T_{SW}$. The energy profile

Fig. 6.4. Efficiency and Energy Profile in MATLAB of a half-wave Parallel SCS, when $f = 1$ MHz, $L_2 = 7.77 \mu$H, $R_2 = 4.975$ Ω, $C_2 = 3.26$ nF, $C_{LP} = 1$ µF, $T_{SW} = 50$ ns.
is shown in Fig. 6.4 for the case when $f = 1$ MHz, $L_2 = 7.77 \mu$H, $R_2 = 4.975 \Omega$, $C_2 = 3.26$ nF, $C_{LP} = 1 \mu$F, $T_{SW} = 50$ ns. The efficiency of charging to $\sim 1.9$ V is $\sim 24.8\%$. We have conducted many such experiments but the results have been far from encouraging.

**Key Observations:**

1. Efficiency increases with increase in $T_{SW}$ and the use of a full-wave structure. Hence, charging the capacitor as quickly as possible helps compensate for the large dissipation in $R_2$.

2. The time required for charging is in the milliseconds range and may not be able to meet the design specifications as laid down in Section (6.3).

3. The secondary voltage ($V_2$) assumes a concave envelope which implies that the frequency response of the circuit has a non-linear dependence on the output voltage/input current.

4. As the output capacitor charges, the switch activation time instant moves up the input voltage sinusoidal profile but down the input current profile. Thus, a stage is reached when there exist reverse currents from the load capacitor back to the coil. In such a case, $T_{SW}$ needs to be decreased adaptively such that the switch doesn’t remain active when the current reverses its direction. This can lead to a more complicated control for the system based on input current sensing.

**6.4.2 Theoretical Analysis of Efficiency**

The efficiency can be analytically calculated from the explicit solutions to the differential equations derived in the previous section. It must be understood that the
every charging cycle would be different in this case in terms of initial conditions, unlike a rectifier operating at steady state, as described in Chapter 5. Hence, to evaluate an accurate expression, each cycle must be evaluated separately, which can be an extremely tedious task, providing little insight.

We can do a more simplistic analysis based on the peak current in the inductor, assuming that the voltage envelope doesn’t change too much over the entire charging cycle, which can be assumed to take ‘N’ cycles with respect to the input time period. The energy dissipated in resistor $R_2$ is given as,

$$E_{DISS} = \int_0^{NT_o} I_{L2, RMS}^2 \times R_2 \times dt = I_{L2, PK}^2 \times R_2 \times NT_o = \frac{I_{L2, PK}^2}{2} \times R_2 \times NT_o \quad (6.4.2.1)$$

The output energy is equal to the energy stored in the load capacitor,

$$E_{out} = \frac{C_{LP} V_{OUT}^2}{2} \quad (6.4.2.2)$$

In addition, the $L_2C_2$ tank is tuned and hence the peak magnetic energy stored in inductor $L_2$ equals the peak electrical energy stored in capacitor $C_2$.

$$\frac{1}{2} C_2 V_{2, PK}^2 = \frac{1}{2} I_{L2, PK}^2 L_2$$

$$\Rightarrow \frac{V_{2, PK}^2}{I_{L2, PK}^2} = \frac{L_2}{C_2} \quad (6.4.2.3)$$

The efficiency can now be described as follows using (6.4.2.1), (6.4.2.2) and (6.4.2.3),

$$\eta = \frac{E_{out}}{E_{out} + E_{DISS}} = \frac{C_{LP} V_{OUT}^2}{\frac{2}{2} + \frac{I_{L2, PK}^2}{2} \times R_2 \times NT_o}$$
\[ \Rightarrow \eta = \frac{1}{1 + \frac{R_2 C_2}{L_2 K^2} \times \frac{N T_0}{C_{LP}}} \tag{6.4.2.4} \]

where, \( K = \frac{V_{out}}{V_{2,PK}} \)

Equation (6.4.2.4) provides valuable insight into the analysis of the efficiency of Parallel SCS. It essentially describes the efficiency using only the circuit parameters. Firstly, it can be observed that the efficiency for a given \( C_{LP} \) will decrease for increasing duration of charging, \( N T_0 \). In the limiting case \( N T_0 \rightarrow \infty \), the efficiency will approach 0 %. This theory tends to refute the theory of adiabatic charging of capacitors, as described in Section (6.3). Intuitively, this can be explained by the fact that if the output energy to the capacitor is a constant, the power dissipation in the resistor \( R_2 \) (due to the large current flowing in the \( R_2 L_2 C_2 \) tank) increases linearly with increase in charging duration. Secondly, it can be seen that the efficiency has a square dependence on the output voltage achieved with respect to the peak input voltage of the resonant tank. This phenomenon is described in greater detail in the next sub-section. These deductions are in good argument with some of the key observations in Section (6.4.1).

6.4.3 Comparison with a Parallel RLC Rectifier

It can be seen that foregoing analysis of Parallel SCS efficiency is a product of the secondary link efficiency and that of the rectification strategy. In [6], a system based on parallel RLC rectifier has been reported in which this efficiency \( \sim 81 \% \). Using the same secondary link and operating frequency, the full-wave parallel SCS gives

91
efficiency ~ 58 %, even when the switch resistance is negligible (100 % rectification efficiency). We hereby propose to analytically compare the efficiency of a rectifier with that of an SCS. Clearly, both the systems are identical in terms of switch control mechanism, with the only difference that the load is a parallel RC in the case of a rectifier. The basic premise is that the energy dissipation in secondary resistor $R_2$ is the same in both the cases. The reader is referred to the half-wave structure in Fig. 6.2 for the discussion that follows.

**Case I – Rectifier**

The efficiency of the secondary link can be given as:

$$\eta_{\text{RECT}} = \frac{E_{\text{OUT}}}{E_{\text{OUT}} + E_{\text{DISS}}} \quad (6.4.3.1)$$

Now, the dissipation in the circuit is given by the expression:

$$E_{\text{DISS}} = \int_0^{NT_o} I_L^2 \times R_2 \times dt \quad (6.4.3.2)$$

where, $NT_o$ is the total time under observation.

As discussed in section (6.4.2), this dissipation can be assumed to be the same in both the systems if the voltage amplitude remains the same. Hence, in principle, the efficiency depends on the output energy that is available in both the cases. We assume a single charging cycle since the conditions over $N$ cycles remain the same for a rectifier. The output energy calculations can be done as follows:

$Q_{ph} = \text{Charge gained by the } R_L \parallel C_L \text{ network during the time } (T_{SW}) \text{ when the switch is ‘On’}$

$V_{pk} = \text{Peak voltage at the output of the rectifier}$

$V_R = \text{Ripple in the output of the rectifier}$
The above two voltages are related by the following relation, assuming that the time
starts when the charging pulse finishes. Hence, 0 to (T_o – T_{sw}) is the discharging time and
(T_o – T_{sw}) to T_o is the charging time.

\[ V_R = \int_{0}^{T_o-T_{sw}} V_{pk} \times e^{-t} \times R_{CL} \times dt \]

\[ V_R = V_{pk} \left( 1 - e^{-\frac{(T_o-T_{sw})}{R_{CL}}} \right) \]  \hspace{1cm} (6.4.3.3)

And the charge is related by the equation:

\[ Q_{PH} = \int_{0}^{T_o-T_{sw}} \frac{V_{pk}}{R_L} \times e^{-t} \times R_{CL} \times dt = C_L V_{pk} \left( 1 - e^{-\frac{(T_o-T_{sw})}{R_{CL}}} \right) \]  \hspace{1cm} (6.4.3.4)

Now, we can calculate the output energy for 1 cycle, separating the charging and
discharging terms.

\[ E_{OUT} = \int_{0}^{T_o} V_{out} \times I_{RL} \times dt = \int_{0}^{T_o-T_{sw}} V_{out} \times I_{RL} \times dt + \int_{T_o-T_{sw}}^{T_o} V_{out} \times I_{RL} \times dt \]

The charging term is difficult to approximate since it is based on the circuit conditions
and parameters, and the resulting expression becomes very verbose. Let us make an
approximation that voltage is almost the average of the final and initial values. This is a
reasonable assumption if T_{SW} and V_R are small.

\[ E_{OUT} = \int_{0}^{T_o-T_{sw}} \frac{V_{pk}^2}{2} \times e^{-2t} \times R_{CL} \times dt + \int_{T_o-T_{sw}}^{T_o} \frac{(V_{pk} - 0.5V_R)^2}{R_L} \times dt \]

\[ \Rightarrow E_{OUT} = \frac{C_L V_{pk}^2}{2} \left( 1 - e^{-\frac{2(T_o-T_{sw})}{R_{CL}}} \right) + \frac{(V_{pk} - 0.5V_R)^2}{R_L} \times T_{sw} \]  \hspace{1cm} (6.4.3.5)

The peak and ripple voltages are related by the expression,
\[ V_{PK} - 0.5V_R = \frac{V_{PK}}{2} \left( 1 + e^{-\frac{(T_o - T_{sw})}{R_L C_L}} \right) \]

Hence,

\[ E_{OUT} = \frac{C_L V_{pk}^2}{2} \left( 1 - e^{-\frac{2(T_o - T_{sw})}{R_L C_L}} \right) + \frac{V_{PK}^2}{4R_L} \left( 1 + e^{-\frac{(T_o - T_{sw})}{R_L C_L}} \right)^2 T_{sw} \]

\[ \Rightarrow E_{OUT} = \frac{C_L V_{pk}^2}{2} \left( 1 - e^{-\frac{2(T_o - T_{sw})}{R_L C_L}} \right) + \frac{V_{PK}^2}{4R_L} \left( 1 + e^{-\frac{(T_o - T_{sw})}{R_L C_L}} + 2e^{-\frac{(T_o - T_{sw})}{R_L C_L}} \right) T_{sw} \]

At this point, we need to combine these terms and express in terms of \( Q_{ph} \) and \( V_{pk} \), which indeed are the parameters used for defining the efficiency. We can make a first order approximation for the exponential based on the fact that \( R_L C_L \gg T_o \).

\[ e^x \approx 1 + x \]

We can approximate the charge per phase.

\[ Q_{PH} = C_L V_{pk} \left( 1 - e^{-\frac{(T_o - T_{sw})}{R_L C_L}} \right) = C_L V_{pk} \left( 1 - 1 + \frac{T_o - T_{sw}}{R_L C_L} \right) = C_L V_{pk} \left( \frac{T_o - T_{sw}}{R_L C_L} \right) \]

We can also approximate the equation for energy the same way.

\[ E_{OUT} = \frac{2C_L V_{pk}^2}{2} \left( \frac{T_o - T_{sw}}{R_L C_L} \right) + \frac{V_{PK}^2 T_{sw}}{4R_L} \left( 1 + 1 - \frac{2(T_o - T_{sw})}{R_L C_L} + 2 - \frac{2(T_o - T_{sw})}{R_L C_L} \right) \]

\[ \Rightarrow E_{OUT} = C_L V_{pk} \frac{T_{o - T_{sw}}}{R_L C_L} + \frac{V_{PK}^2 T_{sw}}{R_L} - \frac{V_{PK}^2 T_{sw}}{R_L} \times \frac{(T_o - T_{sw})}{R_L C_L} \]

\[ (6.4.3.6) \]

We can now substitute \( Q_{ph} \) into the above equation,

\[ E_{OUT} = Q_{PH} \times V_{pk} + V_{PK} \times Q_{PH} \times \frac{T_{sw}}{(T_o - T_{sw})} - V_{PK} \times Q_{PH} \times \frac{T_{sw}}{R_L C_L} \]
\[ E_{OUT} = Q_{PH} \times V_{pk} \times \left( \frac{T_o}{T_o - T_{sw}} - \frac{T_{sw}}{R_t C_L} \right) \]  

(6.4.3.7)

Hence, we have finally got a relation based on \( Q_{ph} \) and \( V_{pk} \). It should be easy to see that in the above relation, the first term in the bracket is slightly greater than 1, while the second is almost negligible in comparison.

The total energy for ‘N’ cycles would be given by,

\[ E_{OUT,T | RECT} = N \times Q_{PH} \times V_{pk} \times \left( \frac{T_o}{T_o - T_{sw}} - \frac{T_{sw}}{R_t C_L} \right) \]  

(6.4.3.8)

**Case II – SCS**

In SCS, since \( Q_{ph} \) is fixed, the voltage increment per cycle is fixed.

\[ \Rightarrow \Delta V = \frac{Q_{PH}}{C_L} \]  

(6.4.3.9)

\[ V_{pk} = \frac{N \times Q_{PH}}{C_L} \]  

(6.4.3.10)

Now, we shall look at the total equation for efficiency for SCS.

\[ \eta_{|SCS} = \frac{E_{OUT}}{E_{OUT} + E_{DISS}} \]  

(6.4.3.11)

As discussed before, the dissipation in the two cases can be assumed to be the same over ‘N’ cycles. Thus we can do a detailed analysis of the output energy.

\[ E_{OUT,T} = \int_{0}^{N T_o} I_{CL} \times V_{CL} \times dt \]

The above expression is non-zero only for the time when the switch is ‘On’, hence it can be piecewise divided into \( N \) expressions for the switchings. Here, \( T_{sw,i} \) is a variable.
\[ E_{OUT,T} = \sum_{i=1}^{N} E_{OUT,i} = \sum_{i=1}^{N} T_{SW,i} \int I_{CL} \times V_{CL} \times dt \]

\[ E_{OUT,i} = \int_{0}^{T_{SW,i}} I_{CL} \times V_{CL} \times dt = C_{L} \times \Delta V \times V_{avg,i} = Q_{PH} \times V_{avg,i} \quad (6.4.3.12) \]

Here, \( V_{avg,i} \) will have the following values:

\[ V_{avg,1} = \frac{\Delta V}{2}, V_{avg,2} = \frac{3\Delta V}{2}, V_{avg,3} = \frac{5\Delta V}{2}, \ldots \]

\[ V_{avg,i} = \frac{\Delta V}{2}(2i-1) \quad (6.4.3.11) \]

\[ E_{OUT,i} = Q_{PH} \times V_{avg,i} = Q_{PH} \times \frac{\Delta V}{2}(2i-1) = Q_{PH} \times \frac{V_{pk}}{2N}(2i-1) \]

Indeed we can compare this to the expression for output energy in the case of a rectifier. It can be seen that the maxima is at \( i = N \), at which this energy would be almost equal to that of a rectifier in each cycle. Now, intuitively we can say that the whole being equal to the sum of the parts is not going to be greater than the energy output of a rectifier in \( N \) cycles, thus proving that a rectifier operating at steady state is more efficient than an SCS with the same configuration.

\[ E_{OUT,T} = Q_{PH} \times \frac{V_{pk}}{2N} \times \sum_{i=1}^{N} (2i-1) = Q_{PH} \times \frac{V_{pk}}{2N} \times \left[ \frac{2N(N+1)}{2} - N \right] \]

\[ E_{OUT,T} = Q_{PH} \times \frac{V_{pk}}{2N} \times \left[ N^2 \right] = Q_{PH} \times \frac{V_{pk}}{2} \times N \]

\[ E_{OUT,T \mid SCS} = N \times Q_{PH} \times \frac{V_{pk}}{2} \]

It can be seen that the above expression for \( E_{OUT} \) would result in the same efficiency for Parallel SCS as is derived in section (6.4.2).
The foregoing discussion assumes that the process of rectification is 100% efficient with zero switch resistance and the dissipation only occurs in the inductor parasitic. However, even if the switch resistance were finite, the rectifier would still be more efficient compared to the SCS. This is because in SCS, the switch activation instant moves down the current sinusoid (and up the voltage sinusoid) from the crest down to the trough, while the rectifier operates mainly around the trough. This essentially means that the average switch current is higher in SCS compared to the rectifier leading to higher dissipation.

6.5 Charging via Series RLC Tank

It was learnt in the previous section that Parallel SCS results in a poor efficiency mainly due to the large currents flowing through the inductor parasitic.
resistance ($R_2$), through the resonant tank even when no output energy is being supplied.

In Fig. 6.5, an alternative to this problem is suggested as a Series SCS in which the current flowing through the $R_2$ is made equal to that flowing through the switches and hence the load. This can be made possible with the principle of current-mode rectification, in which switches $S_P$ and $S_N$ are enabled based on the polarity of the input inductor current. Thus, when $I_{L2} > 0$, $S_P$ is switched ‘On’ and when $I_{L2} < 0$, $S_N$ is switched ‘On’, resulting in zero current switching (ZCS). As a result, $C_{LP}$ charges to positive voltage while $C_{LN}$ charges to a negative voltage. It must be understood that this structure

Fig. 6.6. MATLAB simulation showing the voltage profile during switching of a full-wave Series SCS, when $f = 1$ MHz, $L_2 = 3.05$ µH, $R_2 = 0.53$ Ω, $C_2 = 8.3$ nF, $C_{LP,N} = 1$ µF, $V_{IND} = 5$ V.
Fig. 6.7. MATLAB simulation of a full-wave Series SCS, when $f = 1$ MHz, $L_2 = 3.05$ $\mu$H, $R_2 = 0.53$ $\Omega$, $C_2 = 8.3$ nF, $C_{LP,N} = 1$ $\mu$F, $V_{IND} = 5$ V. (a) Input and output voltages (b) Input inductor current.
can only operate in full-wave. This is because passing current through $C_2$ in one direction turns it into a battery with a given polarity and prohibits subsequent switchings from taking place. Hence, current must be reversed from $C_2$ so that no net charge remains at the end of a single charging cycle. In this topology, since there is no amplification of the induced voltage to $V_2$, the induced voltage needs to be similar in magnitude to the final desired output voltage. This necessitates the requirement of a power amplifier at the primary link.

6.5.1 Simulation Results
Fig. 6.9. MATLAB simulation of a full-wave Series SCS, when $f = 1 \text{ MHz}$, $L_2 = 3.05 \mu\text{H}$, $R_2 = 0.53 \Omega$, $C_2 = 4 \text{ nF}$, $C_{LP,N} = 1 \mu\text{F}$, $V_{IND} = 5 \text{ V}$. (a) Input and output voltages (b) Input inductor current.
It is possible to simulate the circuit in Fig. 6.5 in MATLAB using the differential equations (DE) described in section (6.4.1). As in the previous case, the DE will be 2\textsuperscript{nd} order if the switch resistance is considered to be negligible. However, in contrast to the previous case, the loss in the switch resistance can equivalently be modeled as a part of $R_2$ since the current flowing through both of them is the same. Fig. 6.6 shows the voltage profile when $C_2$ is tuned to $L_2$ at the input frequency. In this, the secondary voltage $V_2$ is being switched between positive and negative output capacitor voltages, depending on the current polarity. It can also be seen that when one capacitor charges, the other’s voltage stays constant and vice-versa. Thus, it results in a duty cycle of $T_0/2$. For the case under discussion, the current and energy profile is shown in Fig.6.7b. It can be seen that from the time of the onset of switching at about 0.5 $\mu$s, the total charging time of two 1
μF capacitors to ±6.22 V is ~ 12 μs. This corresponds to a very fast charging profile and it can be seen that the peak current ~ 2.5 A. The efficiency for this case is ~ 79.8 %. However, it can be seen from Fig. 6.8 that the efficiency and output DC voltage falls
rapidly with increasing $R_2$. This is unacceptable since the switch resistance will tend to have a finite value, generally of the order of a few ohms.

If the discussion in section (6.3) were to be considered, the efficiency could possibly be improved by trying to “slow down” the capacitor charging process. This can be achieved by reducing the current, which translates to an increase in the network impedance. However, with $L_2C_2$ at resonance, the network impedance is mainly a function of the resistance $R_2$. This is because, $C_{LP,N}$ are almost an order of magnitude greater than $C_2$ and don’t affect the characteristics of the network. Hence, the only way increase this impedance and decrease the current would be by detuning the secondary out of their resonance. The results are shown in Fig. 6.9, for the case when $C_2$ is decreased to 4 nF, almost half of its tuning value. Comparing Fig. 6.9a with Fig. 6.7, it can be seen

Fig. 6.12. MATLAB simulation results showing the dependence of efficiency and output DC voltage on $f$ in a full-wave Series SCS, when $L_2 = 3.05 \ \mu\text{H}, \ C_2 = 4 \ \text{nF}, \ R_2 = 0.53 \ \Omega, \ C_{LP,N} = 1 \ \mu\text{F}, \ V_{IND} = 5 \ \text{V}.$
Fig. 6.13. MATLAB simulation results showing the dependence of (a) charging time and (b) output DC voltage on $C_2$ and $C_{LP,N}$ in a full-wave Series SCS, when $f = 1$ MHz, $L_2 = 3.05$ $\mu$H, $R_2 = 0.53$ $\Omega$, $V_{IND} = 5$ V.
that the charging current peak has decreased by an order of magnitude and the current profile elongates itself over time. This is indeed the desired scenario for our case. As can be seen from Fig. 6.9b, the efficiency for this case is \( \sim 95\% \). As a consequence of the aforementioned change, the dependence of efficiency and output DC voltage on \( R_2 \) decreases, as can be seen from the simulation results in Fig. 6.10.

We have also characterized the Series SCS to gain insights into the dependence of efficiency, output DC voltage and charging time as the three most important parameters, on various circuit parameters and input frequency. As can be seen
in Fig. 6.11a, $V_{OUT}$ has maxima while efficiency has minima at the case when the secondary is tuned to the input frequency. A bell shaped curve for the efficiency is obtained, which resembles the impedance characteristics of a series RLC network. It can be seen that the charging time increases monotonically above and below the $C_2$ tuning range (8.3 nF in this case). Also interesting to note is the dependence of efficiency on input frequency ($f$), when $C_2$ is held constant. It can be seen from Fig. 6.12 that it is exactly the case of changing $C_2$ at a given frequency, with the efficiency minima occurring at 1 MHz.

With this knowledge, we have attempted to see the dependence of $V_{OUT}$, $\eta$ and $NT$ on $C_2$ and $C_L$ by plotting 3D curves from data obtained from simulations. Uptil now, the information available was only for 1 $\mu$F. As can be seen from Fig. 6.13 and 6.14, (the discontinuities in the graphs are due to incomplete set of simulations and should be ignored) even in the worst case when $NT \sim 750$ $\mu$s for $C_L = 10$ $\mu$F, the output voltage achieved is in the range 3.5 – 4 V. In addition this is true for $C_2$ in the range 5 – 2 nF and ensures an efficiency $\sim 95\%$. Thus, the Series SCS topology is able to comfortably meet all the design requirements as stated in Section (6.2). In the following sections, we take a look at some of the practical implementation issues.

**6.6 Proof of Concept**

In this section, we describe some of the details on the implementation of Series SCS in a standard CMOS based technology. For AMI 0.5 $\mu$m CMOS, the allowable junction voltage is 5 V. Thus, we can afford to charge $C_{LP}$ and $C_{LN}$ to $\pm 2.5$ V in
the prototype implementation. To drive the on-chip switching circuitry, a positive supply, $V_{DD} = +2.5$ V, and a negative supply, $V_{SS} = -2.5$ V needs to be made available. This can be done be an optimized low dropout voltage rectifier as discussed in Chapter 5. The two capacitors charge with respect to the secondary ground voltage as shown in Fig. 6.5. At this point, we firstly consider the design of the MOS switches implementation of $S_P$ and $S_N$ in Fig. 6.5. Fig. 6.16 shows a PMOS based implementation for both $S_P$ and $S_N$ while Fig. 6.17 depicts an NMOS based implementation. The two cases need to be evaluated

### Table 6.1

**P1 (Fig. 6.15A) Conditions During Two Phases Of The Coil Voltage**

<table>
<thead>
<tr>
<th>$V_2$</th>
<th>$P1$</th>
<th>$V_{GC1}$</th>
<th>$V_{BC1}$</th>
<th>$V_{OUT_MIN}$</th>
<th>$D_{SW}$</th>
<th>$D_{DW}$</th>
<th>$D_{WB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 0</td>
<td>ON</td>
<td>$V_{SS}$</td>
<td>$V_2$</td>
<td>$V_{SS} +</td>
<td>V_{THP}</td>
<td>$</td>
<td>Short</td>
</tr>
<tr>
<td>&lt; 0</td>
<td>OFF</td>
<td>$V_{DD}$</td>
<td>$V_{OUTP}$</td>
<td>Boosted</td>
<td>RBD*</td>
<td>Short</td>
<td>RBD*</td>
</tr>
</tbody>
</table>

*RBD = Reverse Biased Diode

### Table 6.2

**P2 (Fig. 6.15B) Conditions During Two Phases Of The Coil Voltage**

<table>
<thead>
<tr>
<th>$V_2$</th>
<th>$P2$</th>
<th>$V_{GC2}$</th>
<th>$V_{BC2}$</th>
<th>$V_{OUT_MIN}$</th>
<th>$D_{SW}$</th>
<th>$D_{DW}$</th>
<th>$D_{WB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 0</td>
<td>OFF</td>
<td>$V_{DD}$</td>
<td>$V_2$</td>
<td>Boosted</td>
<td>Short</td>
<td>RBD*</td>
<td>RBD*</td>
</tr>
<tr>
<td>&lt; 0</td>
<td>ON</td>
<td>$V_{SS}$</td>
<td>$V_{SS}$</td>
<td>$V_{SS} +</td>
<td>V_{THP}</td>
<td>$</td>
<td>RBD*</td>
</tr>
</tbody>
</table>

*RBD = Reverse Biased Diode

### Table 6.3

**N2 (Fig. 6.16B) Conditions During Two Phases Of The Coil Voltage**

<table>
<thead>
<tr>
<th>$V_2$</th>
<th>$N2$</th>
<th>$V_{GC1}$</th>
<th>$V_{BC1}$</th>
<th>$V_{OUT_MAX}$</th>
<th>$D_{DB}$</th>
<th>$D_{SB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 0</td>
<td>OFF</td>
<td>$V_{SS}$</td>
<td>$V_{SS}$</td>
<td>$- V_{THP}$</td>
<td>RBD*</td>
<td>RBD* if $</td>
</tr>
<tr>
<td>&lt; 0</td>
<td>ON</td>
<td>$V_{DD}$</td>
<td>$V_{SS}$</td>
<td>$V_{DD} - V_{THP}$</td>
<td>RBD* if $</td>
<td>V_{OUTP}</td>
</tr>
</tbody>
</table>

*RBD = Reverse Biased Diode
Fig. 6.15: Schematic of PMOS based switch for implementing the switch for
(a) $C_{LP}$ (b) $C_{LN}$
Fig. 6.16: Schematic of NMOS based switch for implementing the switch for (a) $C_{LP}$ (b) $C_{LN}$
Fig. 6.17. Complete Circuit Schematic of the Series SCS.
Fig. 6.18: CMOS Schematic of (a) Preamplifier (b) Comparator_P,N
carefully. PMOS bulk will be dynamically controlled to reduce body effect and latch-up. It can be seen that $P1$ operates in safe conditions in both cases when the voltage $V_2$ swings between positive and negative values. In the problem is that the minimum negative voltage to which $CLN$ can be charged is about $\sim -1.6$ V. This is because PMOS cannot conduct low voltages. Similarly, NMOS cannot conduct high voltages. Hence, we need to reject $P2$ and $N1$. For $N2$ implementation shown in Fig. 6.16b, we can write the conditions in Table 6.3. The NMOS bulk has been connected to the most negative voltage on the chip, $V_{SS}$.

The final schematic is shown in Fig. 6.17. A small resistance $R_{SEN}$ has been inserted in series in the main current path to sense the current polarity. The comparators check the zero crossings of $V_{SEN}$ and switch $C_{LP}$ or $C_{LN}$ based on this information. It must be seen that the phases of $GC_P$ and $GC_N$ need to be completely non-overlapping else it can lead to charge sharing between $C_{LP}$ and $C_{LN}$, and hence loss of energy. Dummy diodes have been added in parallel to the main switching MOSFETs for two reasons. Firstly, it helps to startup the charger when the amplitude of the current is small, which depends on the value of $C_{PAR}$. Secondly, it helps relax the delay requirements of the comparator by providing a parallel lossy path as long as the comparator has not switched. The -3DB bandwidth of the preamplifier needs to be made large to ensure a wideband current sensor.

The preamp shown in Fig. 6.18a consumes 40 $\mu$A and has a DC gain of $\sim 25$ for $R_{SEN} = 0.5$ $\Omega$. The high gain relaxes the power requirements of the following comparators, while the high power dissipation ensures 3DB bandwidth of $\sim 1.5$ MHz,
which is sufficient to amplify an input signal of 1 MHz. In addition, it also helps attenuate the high frequency transients, thereby preventing any spurious switch activations. The comparator shown in Fig. 6.18b, and has asymmetrical rise and fall times, due to different slewing for pull-up and pull-down. In the current design this automatically ensures that the switch opening is faster than the complementary switch closure, thereby making the two phases completely non-overlapping. Each comparator consumes 5 µA of static power. The preamplifier and the comparator each introduce a delay of ~ 20 ns.

In a prototype implementation in AMI 0.5 µm CMOS, \( W_{PL} = 3 \text{ mm}, \ W_{NI} = 1 \text{ mm}, \ W_{PL,D} = 600 \mu\text{m}, \ W_{NI,D} = 200 \mu\text{m}, \) and the length is kept to a minimum at 0.6 µm. With the system just described in place, and \( f = 1 \text{ MHz}, \ L_2 = 3.05 \mu\text{H}, \ R_2 = 0.53 \Omega, \ C_2 = 2.5 \text{ nF}, \ C_{LP,N} = 1 \mu\text{F}, \ V_{IND} = 2.5 \text{ V}, \) the output capacitors charge to ±1.9 V in 120 µs with an efficiency of 78 %.

6.7 References


Chapter 7

7. Conclusions and Future Work

7.1 Conclusions

In this thesis, we have focused on the efficient transmission of power wirelessly via an inductive link. An AC-DC converter was proposed which performs synchronous rectification of the induced power at the secondary end of the coil. By pushing the switching MOSFET into deep triode, the rectifier dropout voltage decreases and the efficiency increases at the same time. In addition, we adopted a lossless capacitive division to control the reverse currents and prevent the degradation of efficiency. A prototype rectifier was designed and fabricated in the AMI-0.5 μm standard CMOS process occupying an active area of ~0.4 mm$^2$. An output voltage of 4.36 V was reached at 0.5 MHz with an input voltage of 5 V$_{\text{Peak}}$ and loading of 1 kΩ in parallel with 1 μF for ripple rejection. The measured efficiency of the prototype rectifier was 85 %. In addition, we performed theoretical analysis of factors affecting the rectifier and were able to optimize the switch size based on area and resistance constraints. A rectifier operating at ISM band frequency of 13.56 MHz was also designed and optimized to provide 86 % efficiency in simulations.

We have successfully incorporated dual-mode backtelemetry in an active rectifier ensuring high efficiency and hence an enhanced reading range in measured results. We have theoretically proved that the use of complementary backtelemetry feature will become increasingly important when considering complex systems with high frequency wireless power transmission and variable power requirements.
We have performed extensive theoretical analysis for understanding the efficiency constraints in the development of a switched capacitor based micro-stimulator, with special emphasis on the specifications for Deep Brain Stimulation. It was deduced through simulations in SPICE and that of differential equations in MATLAB, that a series RLC tank can be more efficient than a parallel RLC based structure and an extremely viable option for DBS. In addition, a circuit prototype was built to charge a single capacitor bank. Even with various circuit parameters not completely optimized, the efficiency while considering the secondary link was ~ 78 %, while the state-of-the-art optimized links report an efficiency of ~ 81 %.

7.2 Future Work

The current SCS implementation needs to be further optimized based on the simulation data obtained in Chapter 6. Finally, the complete system as discussed in the Chapter 2 of the thesis needs to be developed and tested. This would mainly involve development of control logic for the switching between various capacitors, the reduction of reverse charging currents to increase the charging efficiency. In addition, the efficiency analysis needs to be performed while considering the losses in the power amplifier, the primary coil and the magnetic coupling.

In addition, since an SCS produces unconventional exponential decaying current profiles, its efficacy needs to be tested on living tissue through in vivo experiments.