Abstract

PUNDI, BHARATRAM SATYANARAYANAN. Class-E Power Amplifier Design and Back-Telemetry Communication for Retinal Prosthesis. (Under the direction of Wentai Liu.)

This thesis discusses the power link in the retinal prosthesis project that aims to provide vision to the profoundly blind. Clinical experiments have confirmed that electrical stimulation can be used to duplicate the action of photoreceptors in the retina to provide vision to blind patients suffering from RP/AMD. The retinal prosthesis system consists of an intraocular unit implanted inside the eye and a separate extraocular unit. The micro-stimulator involved in retinal prosthesis consists of multiple electrodes arranged in two-dimensional array and is a part of the intraocular unit. The micro-stimulator needs data and power to be transferred wirelessly from the extraocular unit.

The power link consists of a highly efficient Class-E driver that transfers power inductively to the intraocular unit. A Class-E power driver is developed to suit the requirements and has been analyzed. The effect of the loaded Q variations on the Class-E circuit has been studied.

Back-telemetry from the intraocular unit is necessary and is achieved through load modulation in the intraocular unit. A novel variation of PWM encoding has been conceived and employed to combine data and clock. The data detection unit consisting of

an envelope detector and a PWM decoder has been developed. The data received is processed in the extraocular unit to adjust the power transfer and achieve power regulation. The format for data transmission has been proposed to arrange data into continuous packets, which includes error detection capabilities.

CLASS-E POWER AMPLIFIER DESIGN AND BACK-TELEMETRY COMMUNICATION FOR RETINAL PROSTHESIS

by

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Biography

Bharatram S. Pundi was born on September 7, 1977 in Chennai, India. He graduated from Indian Institute of Technology – Madras with his Bachelor's degree in Electrical Engineering in 2000. He subsequently joined the ECE department at North Carolina State University. He worked as a student intern at IBM in Research Triangle Park in the summer of 2001 as an ASIC verification engineer. He joined Dr. Wentai Liu's group at NCSU to work on the power link for the retinal prosthesis in Fall-2001. He completed his MS in Computer Engineering from North Carolina State University in December 2002. His fields of interest include analog, digital and mixed-signal VLSI design, ASIC design and verification. He also has active interest in applications like micro-architecture, DSP and communications.

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Chapter 1

Introduction

The retinal prosthesis project focuses on the development of an implantable rehabilitative device that can replace the functionality of deceptive photoreceptors in patients suffering from retinitis pigmentosa (RP) and age-related macular degeneration (AMD). Currently, no treatment is available for either disease that destroys the light sensing photoreceptor (rods/cones) cells. The photoreceptor cells in a healthy retina initiate the neural response to the incidence of light energy on the retina. The bi-polar and the ganglion cells of the inner retina then process the neural signal prior to higher processing. Though the retinal photoreceptors are defective for patients suffering from RP/AMD, the bi-polar and the ganglion cells to which the photoreceptors synapse survive at a higher rate [1].

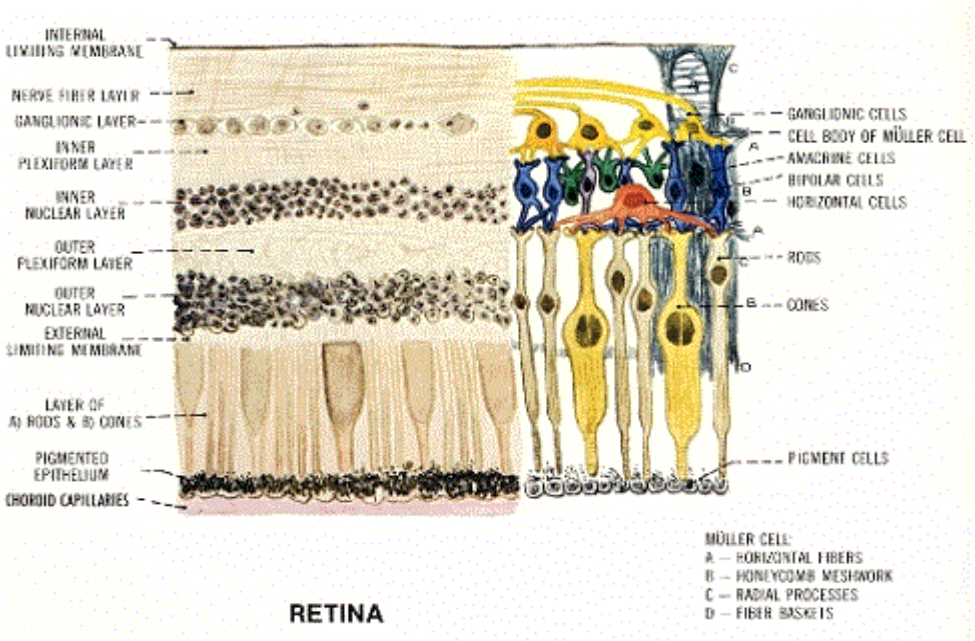


Figure 1.1: Retina

1.1 Retinal micro-stimulator

The bi-polar and the ganglion cells can respond to artificial electrical stimulation provided by an implanted chip. Previous clinical studies [2] have shown that the controlled electrical signals applied to a small area in the retina using a microelectrode can be used to stimulate neural response in the remaining retinal cells. Blind patients on whom the tests were conducted perceived the neural response as a spot of light. When multiple electrodes were activated in a two dimensional array [2], a number of spots of light were visible to the patients which when viewed resembled the pattern represented by the active electrodes. When controlled pattern stimulation of retinal neurons is coupled with an external image acquisition and transmission system, it is possible for the sight-impaired to regain form vision.

The implantable stimulator [3] has been provided with thousand electrodes in order to perceive complex images, which means that there is considerable amount of power required by the micro-stimulator. There is also a need for high wireless data rate throughput from the extraocular unit to the intraocular unit. The data will be used to provide information from the external image acquisition unit to drive the electrodes inside the eye.

1.2 Power and Data link

The thousand electrode used in the micro-stimulator needs to maintain an image rate of 60 frames/sec or more to obtain a non-flickering image when stimulating remaining retinal neurons for the blind. This means that, apart from power transmission, a high data

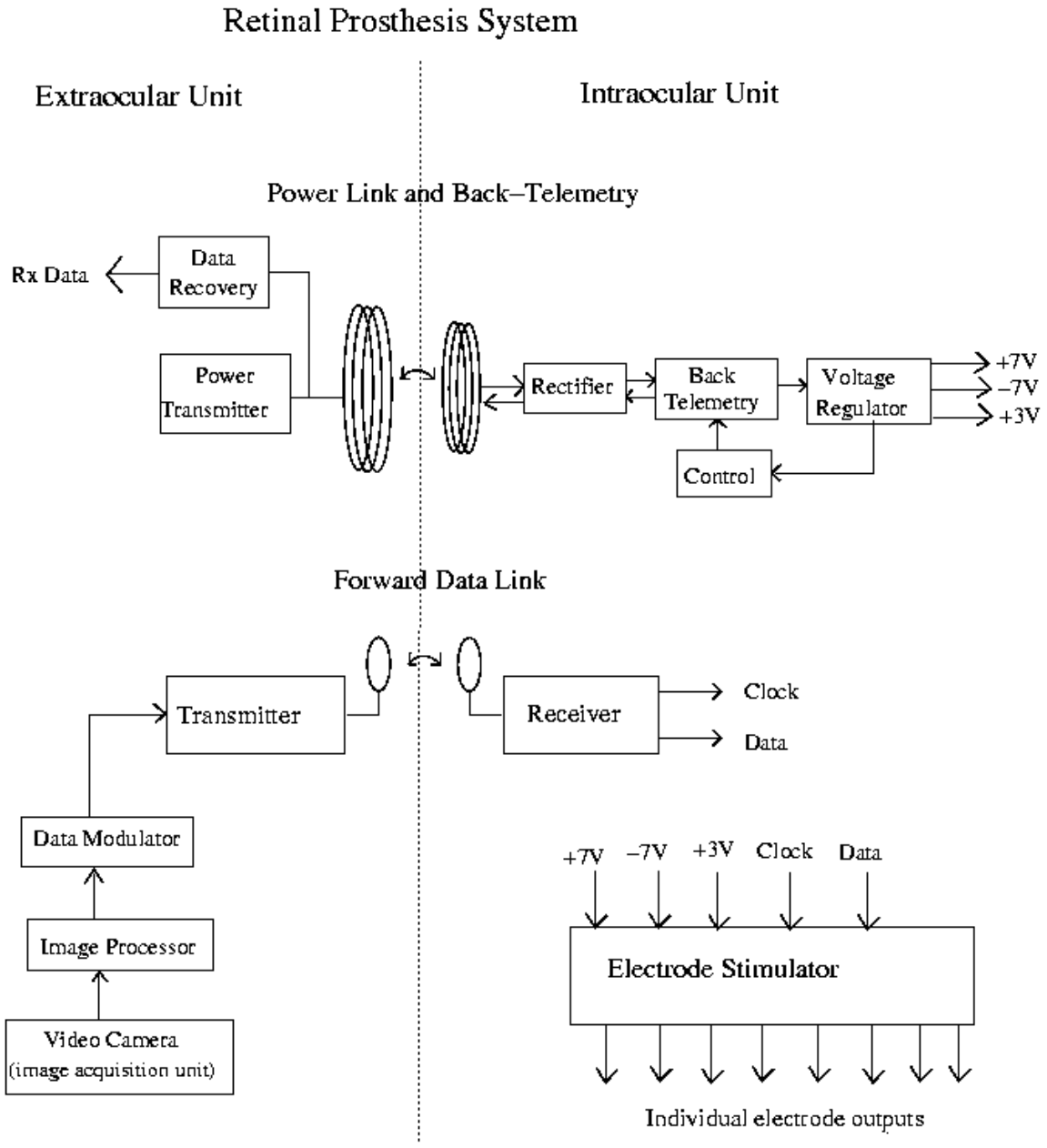


Figure 1.2: Retinal Prosthesis System

rate is required for non-flickering images. Since we cannot pass a wire through the eye, both data and power has to be delivered wirelessly. The human body is penetrable to magnetic fields at low frequencies, which is ideal for inductively transmitting power from the extraocular to the intraocular units. However, due to narrow bandwidths at low frequencies, the possible data rate of transmission is much lower than the required rate of data transmission. Improved data rates will be obtained by separating the power carrier from the data carrier.

Both data and power transfer is accomplished using coil couplings at different frequencies as shown above in fig 1.2. The coils are aligned in such a way as to minimize cross coupling between the two. Binary differentially encoded PSK data is transmitted at a higher frequency through one of the coils. The powering and back-telemetry is achieved through coil coupling at a lower frequency of 1Mhz. Thus a mixed low-high frequency system is employed in the retinal prosthesis project. Separating the power link from the data link permits optimization of the inductive power link to minimize the electromagnetic and thermal absorption of the retina.

1.3 Back-telemetry communication

The passive back-telemeter is used to periodically update the external unit about critical information related to the intraocular unit. The power level on the secondary side is monitored and the information is communicated back to the primary side where this information is processed and any required changes in the power transferred will be carried out. The main reason for the power regulation is that the coupling coefficient

between the primary and the secondary is not a constant. Any change in coil orientation or distance between coils leads to changes in the coupling coefficient and a resultant change in induced voltage. This means that the primary circuit has to adjust to ensure that the induced voltage is maintained at the required value. Apart from power related information, it is also important to communicate information like electrode impedance levels, ph content, and temperature inside eye from the intraocular unit. Back-telemetry is achieved through load modulation on the secondary side.

1.4 Components of power link

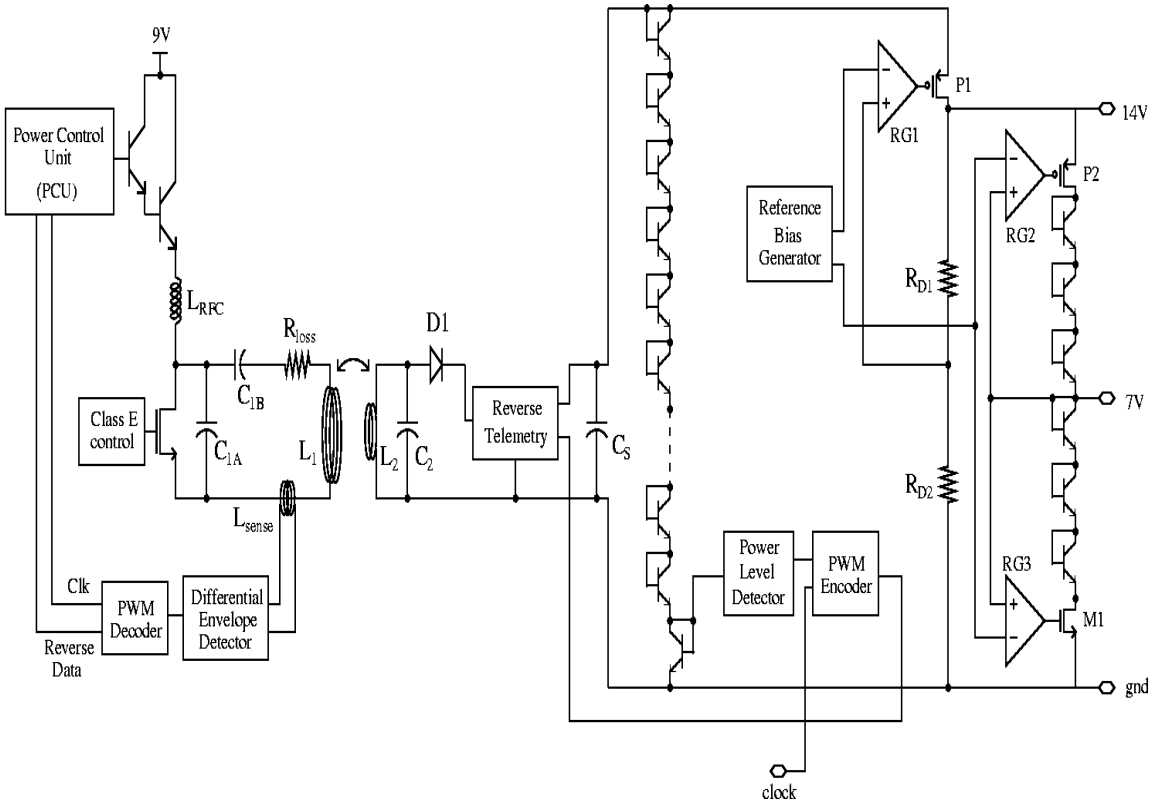


Figure 1.3: Power Link Overview

The focus of this document is on the lower frequency power link and the back-telemetry unit, the details of which have been shown above. The technology employed is AMI-1.6.

The power transmitter uses a powerful Class-E amplifier driver that is very efficient. Details of Class-E amplifier design have been discussed in chapter-2.

Rectification is achieved using a single-phase rectification diode and a capacitor, generating a dual rail supply of +7/-7 and a 3V supply for digital logic. An initial shunt type regulator provides current regulation and coarse voltage regulation. A series type regulator to provide the necessary fine voltage regulation follows the initial regulation. The details about regulation have been explained in detail in [4].

Back-telemetry operates using the principle of load modulation [4,5]. The primary coil voltage is affected by load modulation, and these disturbances are detected by using a coil loosely coupled to the primary inductance. A differential envelope detector is used to detect the disturbances. Pulse width modulation scheme is employed in reverse telemetry so that clock and data are combined into a single digital waveform. Further details about reverse telemetry communication have been discussed in chapter-3.

Chapter-4 offers summary and conclusions for the thesis and also discusses the broad direction of the ongoing work related to retinal prosthesis.

Chapter 2

Class-E Power Amplifier Design

It is medically infeasible for permanent wired connections pass through the eyeball wall. Hence the power and data transmission to the implanted unit is achieved through a wireless link. Power is transferred to the implant by using a power amplifier circuit, which converts DC to AC power. The implanted unit uses rectifiers on the receiver side to convert AC waveforms back to DC to act as the supply voltage. The inductive link used has very low coupling coefficients and hence highly efficient Class-E power amplifiers capable of producing the required coil currents have been used for the purpose.

2.1 Types of Power Amplifiers

Fundamentally, there are two types of tuned power amplifier topologies. The conventional Class-A/AB/B/C power amplifiers have the active device transistor acting as a current source. The parallel-tuned output circuit maintains sinusoidal collector voltages. On the other hand, Class-E power amplifiers are a switched mode power amplifier, where the active device acts as a switch.

Use of active device as switch instead of a high-impedance current source improves efficiency. When a power amplifier uses the active device as a high impedance current source, the output current is determined primarily by the input drive and is almost independent of the output voltage. If the active device saturates, then basic design

assumptions become invalid. Also, a practical active-device current source requires at least a certain minimum permissible voltage across itself, while an active-device switch may be operated at a much smaller 'on' voltage. In a switching-mode device, the 'on' state ac impedance is low compared to the ac impedances in the surrounding circuit. In a current-source device, ac impedance is high compared to the surrounding circuit.

2.2 Fundamentals of Class-E power amplifiers

Nathan Sokal and Alan Sokal [6] first proposed the Class-E power amplifier architecture. Class-E is a tuned power amplifier topology composed of a single pole switch and a load network. The load network studied below consists of a resonant circuit in series with the load, and a capacitor that shunts the switch. The collector voltage waveform is determined by the switch when it is 'on', and by the transient response when the switch is 'off'.

Minimizing power dissipation while providing a desired output power maximizes efficiency. In most RF and microwave power amplifiers, the largest power dissipation is in the power transistor. This is given by the product of transistor voltage and current integrated and averaged over time. Although the transistor must sustain high voltage during part of the RF period and conduct high current during part of the RF period, the Class-E circuit is so arranged such that the high voltage and high current do not overlap and hence avoid high power dissipation.

The figure below from [6] shows the ideal Class-E voltage and current waveforms that meet the high efficiency requirement.

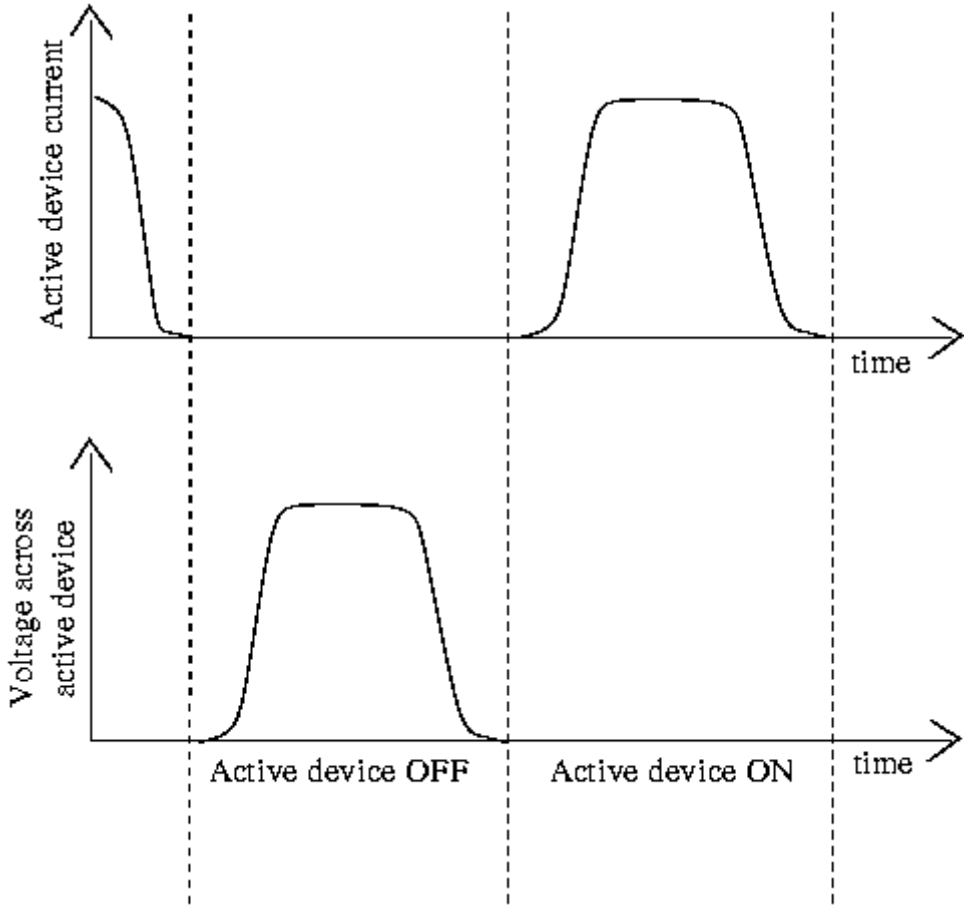


Figure 2.1 Target waveforms

The transistor is operated as a switch. One of the most important factors that have to be accommodated is the transistors practical limitation for RF and microwave applications. The transistor switching times are usually an appreciable fraction of the RF period. To avoid a high v-i product during switching transitions, a suitable load network is employed which help meet certain timing requirements.

The voltage-current product is made low [6,7] throughout the RF period by ensuring the following conditions on the v-i waveforms for the active device.

1. During the ON state, the voltage across the active device is nearly zero when high current is flowing through the device. The transistor is acting like a low resistance switch when switched on.
2. When there is high voltage across the device, the current through it is made zero as the transistor behaves like an open switch.
3. To take the switching time into account, the rise of the transistor voltage is delayed until after the current has reduced to zero.
4. The transistor voltage returns to zero before the current begins to rise. A suitable load network fulfills the timing requirements of conditions 3 and 4.
5. The transistor voltage at turn-on time is nominally zero. Then the turning-on transistor does not discharge a charged shunt capacitance in the load network. This avoids dissipation of stored capacitor energy($C*V^2/2$) f times per second.
6. The slope of the transistor voltage waveform is nominally zero at turn-on time. Then, the current injected into the turning-on transistor by the load network rises smoothly from zero at a controlled moderate rate, resulting in low i^2R dissipation.

The above conditions keeps down the power dissipation across the active device and helps to increase the efficiency.

2.3 Load Networks for Class-E circuits

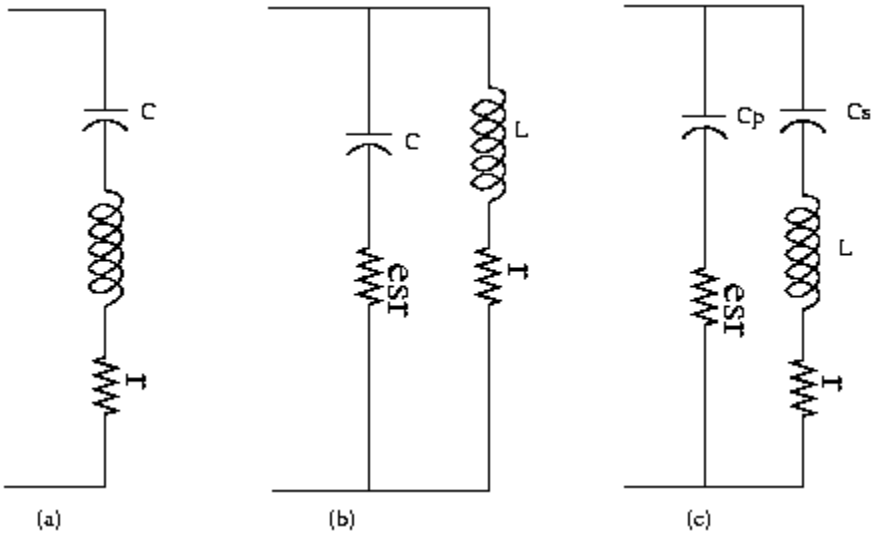


Figure 2.2: Load network

Different topologies can be applied for the Class-E load network to satisfy the conditions for Class-E action as explained in [8].

The first load network shown in (a) places a capacitor in series with the coil and the pair is driven at their resonant frequency. At resonance, the effective impedance is the series resistance as the coil reactance cancels that of the capacitor at resonance. This reduces the voltage that the active device must handle but increases the coil current. The large current value might lead to excessive power dissipation in the active device.

The second load network shown in (b) is a parallel resonance circuit that lowers the current that the active device must carry. In this configuration, an inductor and capacitor are placed in parallel. The equivalent series resistance at resonance is high and hence large coil currents will lead to high voltages across active device. This is also a

disadvantage because we require high-voltage active device having large capacitances, which limit the operating frequency.

The third network (c) is a multi-frequency series-parallel resonant circuit that combines both the above networks. The network provides a means to drive a large current through the coil while keeping the current and voltage across the active device to acceptable levels. It also helps to satisfy the conditions required for Class-E operation.

2.4 Structure of Class-E circuits

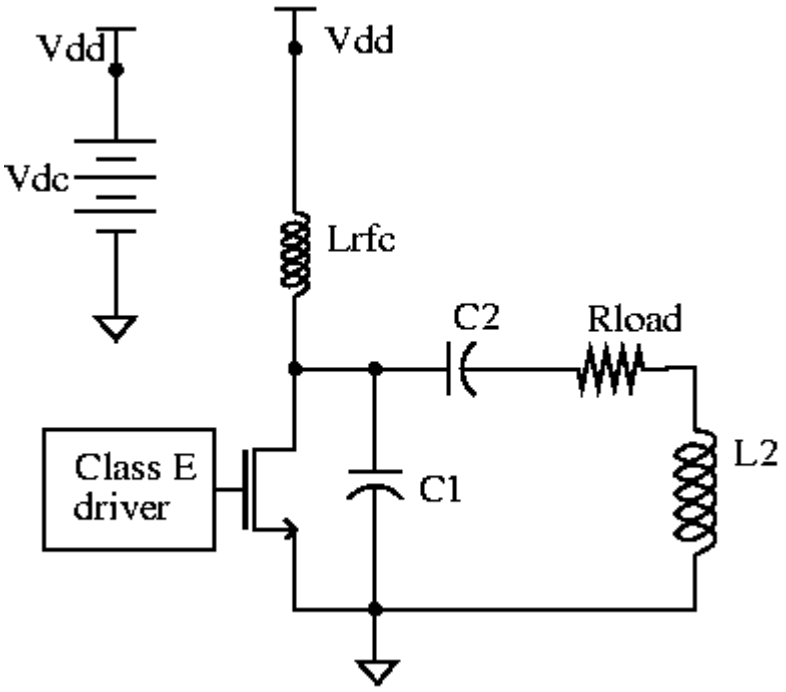


Figure 2.3: Class-E configuration

A simple Class-E driver is a voltage pulse source with a specific frequency and duty-cycle. Lrfc is a high reactance choke. Rload can be the actual load or is the input port resistance of the effective load. The active device voltage drops to a minimum when the device is turned on with the voltage pulse source. Proper choice of L2, C2, C1 values

with an appropriate voltage driver to the active device results in a high-efficiency power amplifier [6,7,8,9]. One of the biggest advantages of Class-E circuits is that it is possible to produce high coil voltages without a high supply voltage.

2.5 Idealized Class-E circuit behavior

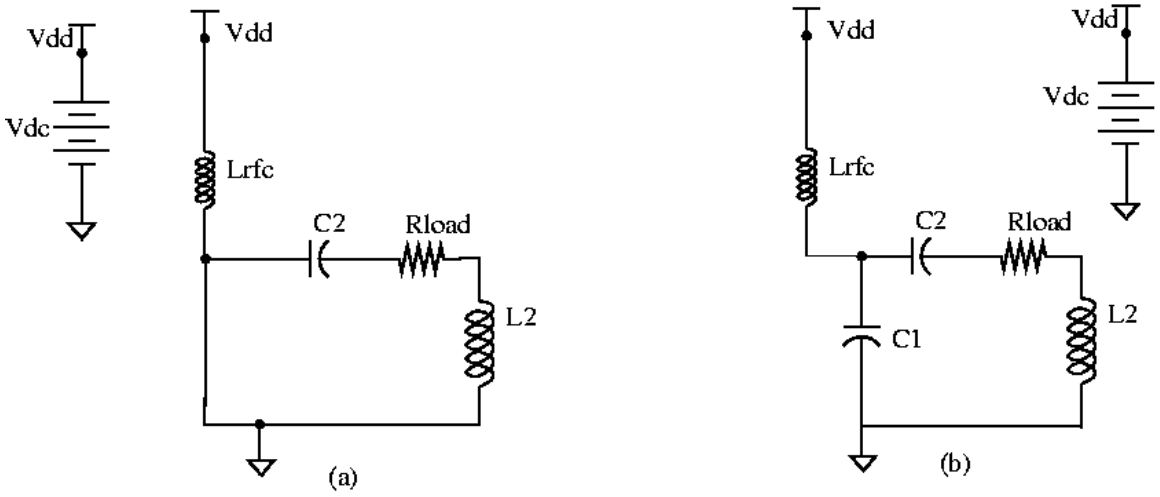


Figure 2.4: Idealized equivalent circuit

The operation of Class-E circuits has been exhaustively discussed in the literature [6,7,8,9,10]. The Class-E driver uses a multi-frequency load network. When the active device is 'on' as shown in (a), the load is L2, C2 and Rload. When the device is 'off' as shown in (b), the load consists of L2, C1, C2 and Rload in series. C1 ensures that when the active device is turned off, there is a delay in the voltage rise across the device.

Thus we have different circuits that resonate at two different frequencies. When the circuit is operated between the series and parallel peaks, there is a particular frequency where the power losses in the driver are minimized. This Class-E point achieves the objectives of Class-E operation by avoiding the co-existence of high voltage and high

current. For a sufficiently high Q load, it can be assumed that the current in the L2-C2 branch is nearly sinusoidal with a frequency equal to that of the switch drive. While the switch is closed, L2 and C2 supply current back to the switch, and no current flows through C1. When the switch opens, L2 and C2 continue supplying current, which now flows through C1 and makes the voltage across C1 (and the switch) positive. When the current in the L2-C2 branch reverses direction, the current is provided by C1 and the voltage across the switch reduces. When the voltage across the switch reduces to zero, the switch is closed and the cycle is repeated. The RFC choke acts as a constant current supply. For high-Q systems, switch voltage and L2 current are close to 90 degree out of phase and the voltage across the switch has a value of zero with zero slope at the time the switch closes. The Class-E driver is immune to the problem of switch capacitance limiting the frequency range. The switch capacitance can be compensated by modifying the value of parallel capacitance.

2.6 Class-E circuits at different values of Q_L

Different kinds [11] of transient voltage responses are possible for different values of the network loaded Q (Q_L). For a given driver pulse voltage source frequency and duty cycle and R_{load}, it is important to select the correct component values of C1, C2 and L2 for Class-E operation. As illustrated in [11], incorrect values can lead to power loss. The formula for the network loaded Q_L is given by:

$$Q_L = (\omega L_2 / R_{load}) \qquad (2.1)$$

2.6.1 Over-damped Q_L (low)

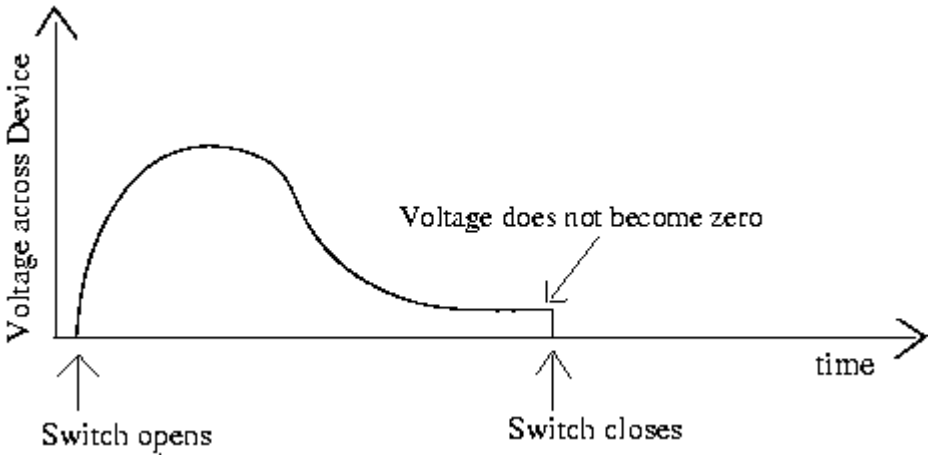


Figure 2.5: Over damped sub-optimum behavior

When Q_L is low, there is too much damping due to the resistance. After the active device is off, the voltage across C1 does not return to zero at the next turn-on instant as the RC time is high. This means that there will be a voltage discharge in C1 from a non-zero value to a very low voltage, leading to wastage of power.

2.6.2 Under-damped Q_L (high)

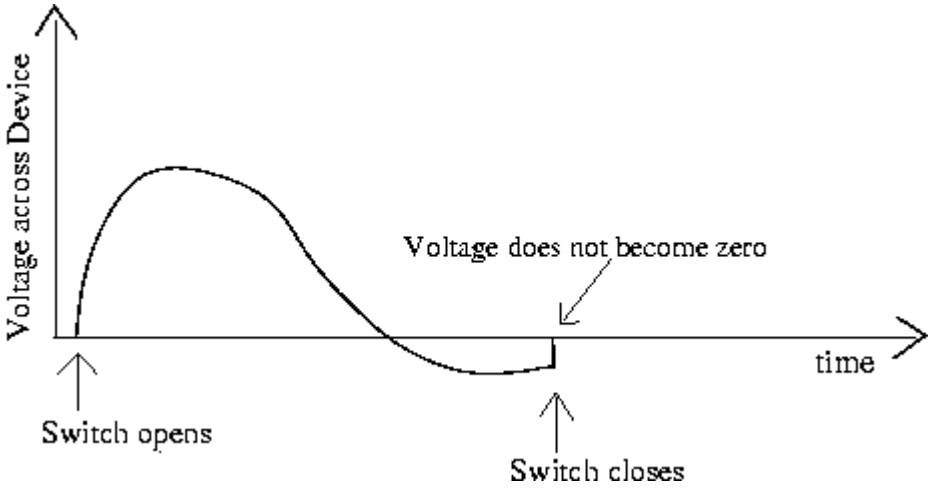


Figure 2.6: Under-damped sub-optimum behavior

When Q_L is too high, there is not enough damping in the system to prevent ringing and voltage shoots past the zero value and is negative when the switch closes. Another possibility for high Q_L, which is shown below, is that the voltage derivative at the time the switch closes is not zero although the voltage itself is zero.

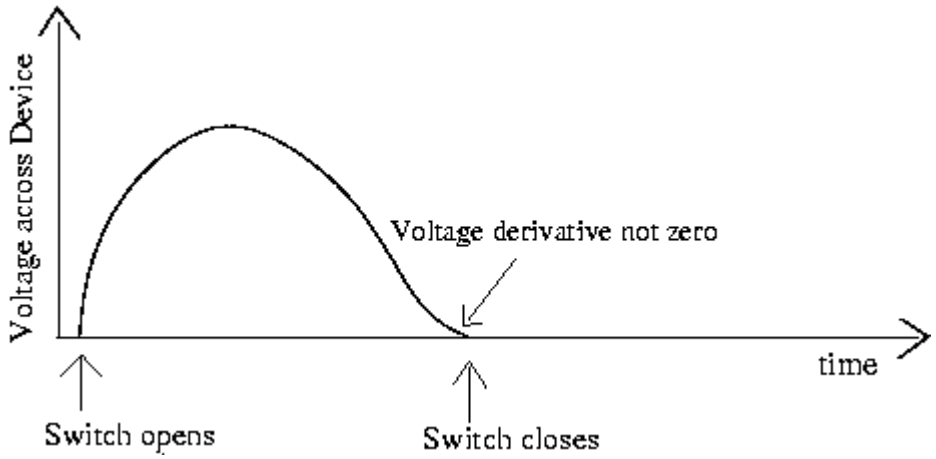


Figure 2.7: Another sub-optimum case

2.6.3 Optimum Q_L

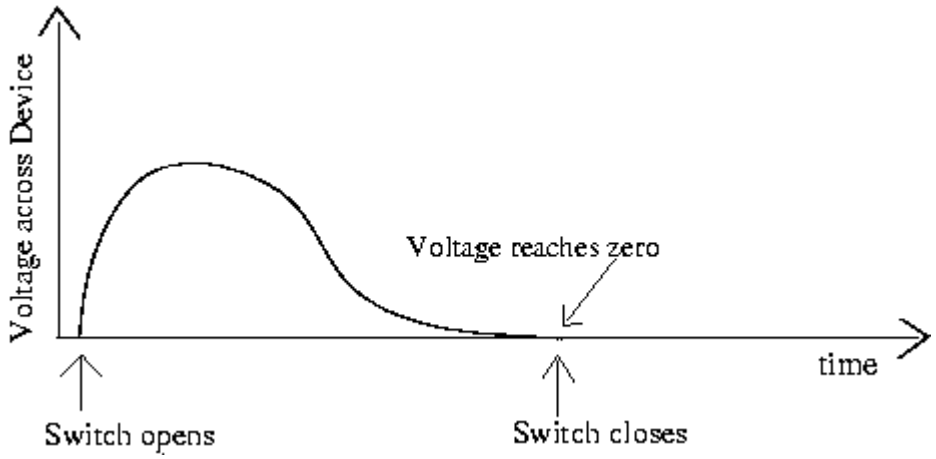


Figure 2.8: Optimal waveforms

When the correct value of Q_L is achieved, proper Class-E operation can be ensured. As shown above, the voltage value and its time derivative are zero when the switch closes.

2.7 Determination of component values

As illustrated in the previous section, given a load and power requirement, it is important to decide the correct component values to achieve the Class-E point. Otherwise, there will be un-necessary power loss that defeats the main purpose of Class-E amplifier, namely efficiency.

Depending on whether the active device is 'on' or 'off', the Class-E circuit behaves as two different circuits, as explained earlier. Hence for the two positions of the switch, we have two separate differential equations determining the behavior of voltage and current waveforms. These differential equations have been explained in detail in [10].

A lot of research work described in the literature about Class-E amplifiers does not describe the details of Class-E amplifier design and the choice of component values. The approach for determining the component values is to either solve the exact differential equation or make some approximations that will help simplify the equations and make the solution easy to arrive at.

Sokal [6,7] and Kazimierczuk [9] have taken the first approach. In [6,7], Sokal has provided explicit design equations that yield the low-order lumped-element Class-E circuit where the pulse driver for the active device has a 50% duty-cycle. Kazimierczuk [9] has provided tables that can be used for specific values of Q_L but for different pulse source duty-cycles. Troyk [8] has taken the second approach and has made an additional assumption of a high Q_L and recommended low duty-cycle source. This simplifies the

differential equations to a closed-form solution. Troyk's approach is not usable in our circuit that involves a low Q_L value. However, it can be useful in the closed loop approach to Class-E design [12].

2.7.1 Design and tuning steps for Class-E circuits

Sokal [7] has provided explicit equations for C1 and C2, once the values of L2 and Rload and the operating frequency are known.

$$C1 = [1/(2\pi fR)\,(\pi^2/4 + 1)\,(\pi/2)]\,[0.99866 + 0.91424/Q_L - 1.03175/Q_L^2] + [0.6/(2\pi f)^2 L_1] \quad (2.2)$$

$$= [1/34.2219\,fR]\,[0.99866 + 0.91424/Q_L - 1.03175/Q_L^2] + 0.6/(2\pi f)^2 L_1] \quad (2.3)$$

$$C2 = [1/(2\pi fR)]\,[1/(Q_L - 0.104823)]\,[1.00121 + 1.01468/(Q_L - 1.7879)] - [0.2/(2\pi f)^2 L_1] \quad (2.4)$$

The above equations assume ideal conditions like zero turn-on resistance and perfect choke inductance that acts as an ideal current source. However, these two assumptions don't hold and hence the values need to be adjusted. A tuning method for bringing the Class-E from an off-nominal condition back to the nominal condition has been described in [7]. The procedure can also be used to tune Class-E circuits that are not on the nominal point due to the additional reactance provided by the load-impedance-transforming network. The duty-cycle employed for the input drive is 50%. The active device has to be chosen appropriate to the load network and the power delivered to it.

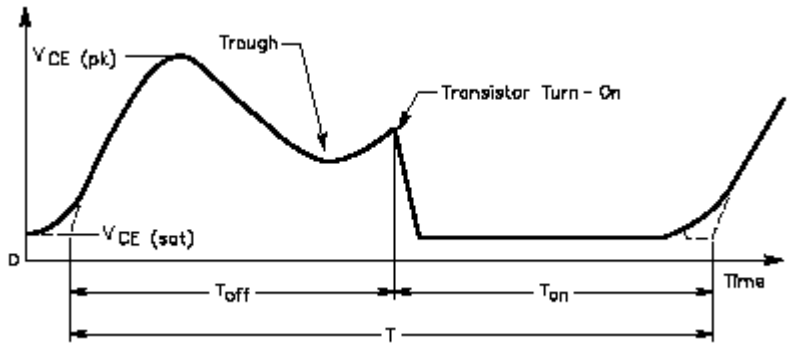


Figure 2.9: Typical mistuned Vce waveform during transistor turn-on and turn-off

Fig 2.9 shows a *V*CE waveform for an amplifier with off-nominal tuning. This off-nominal behavior can be suppressed by tuning the load component values [7].

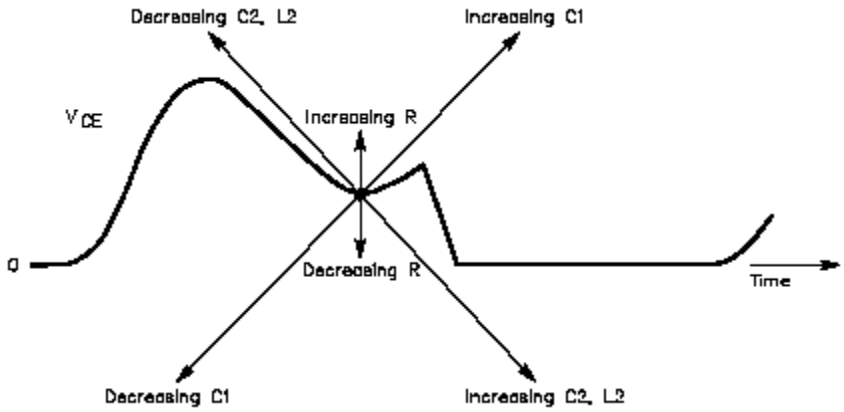


Figure 2.10: Effect of adjusting load network components

Figure 2.10 shows how the load network components affect the *V*CE waveform. It is possible to tune the load network to fulfill the desired conditions for ideal Class-E.

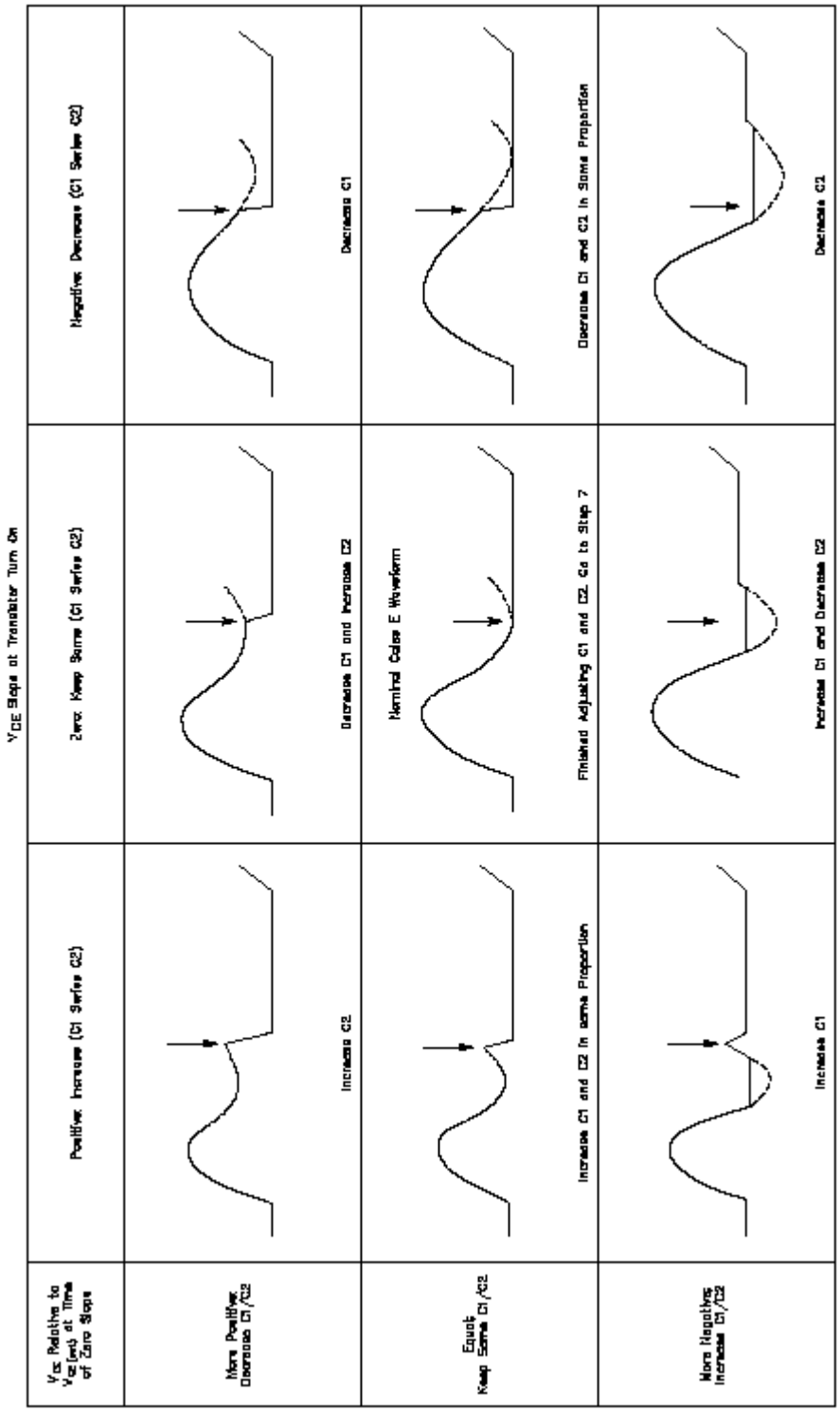


Figure 2.11: C1 and C2 adjustment procedure

Fig 2.11 shows the adjustment procedure involving C1 and C2. As mentioned earlier, the values of Rload and L2 and the operating frequency are fixed initially. Now, any off-nominal behavior is suppressed by adjusting C1 and C2 from Figure 2.11. This procedure can be used to finalize C1 and C2 [7].

2.8 Class-E design for the power link

The inductive power link between the intraocular and extraocular units is designed to deliver power to the micro-stimulator that acts as the secondary load. The power link can be modeled as shown below in Figure 2.12. The rectifier can be modeled as a diode and a charging capacitor, and the load (micro-stimulator) can be modeled as a resistive load. The secondary side located in the intraocular unit consists of a resonating LC pair apart from the rectifier and the load.

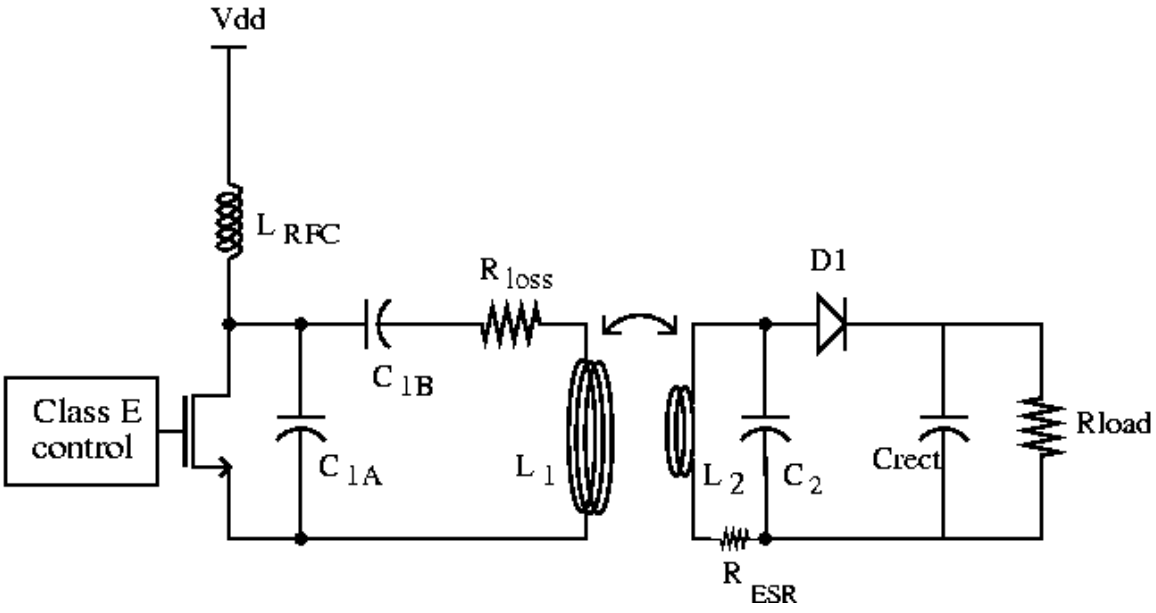


Figure 2.12: Power link simplified model

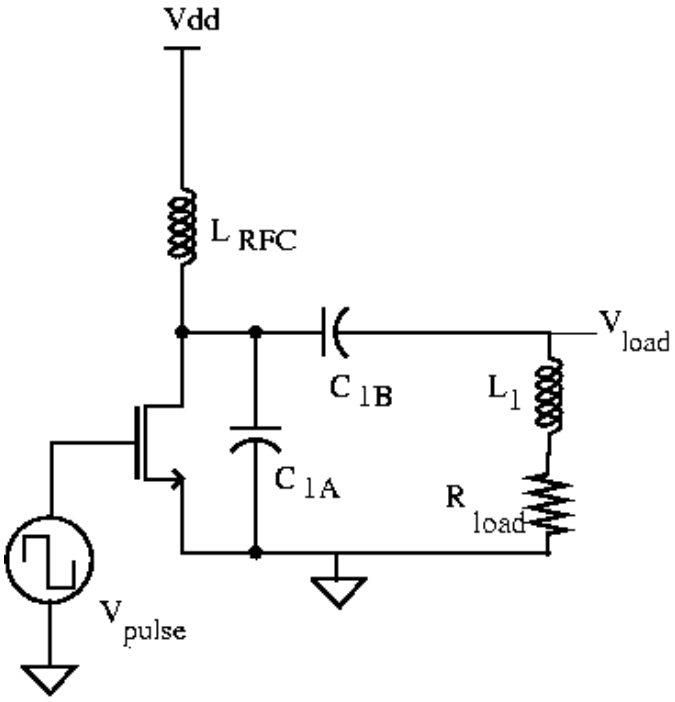
A target power of 250mW is consumed by the micro-stimulator load and has to be delivered while minimizing both the power dissipated in the secondary resonant tank and the total H-field radiated by primary and secondary coils. The induced voltage on the secondary side should not be less than 15V even when there are variations in the coupling coefficient between the two coils. The variations in the coil-coupling coefficient occur because the center-to-center distance between coils varies between 2mm to 15mm.

Given the above constraints, L2=60μH, L1=66μH and C2=300pF were chosen and the equivalent value of R_{LOAD} as seen from the primary side was calculated to be 37.7Ω, as explained in [12]. From these values, Q_L can be calculated.

$$Q_L = L1\omega / R_{LOAD} = 11 \qquad (2.5)$$

The design equations in [6,7] assume ideal switch behavior and also that L_{RFC} acts as an ideal current source at steady state. As explained earlier, they need to be tuned further [7]. It is also very important to choose the proper active power device. MOSFETS are better than BJT as they consume lesser base currents. The active device used in simulations is an AMI-1.6 technology NMOS device with an aspect ratio of 15mm/1.6μm. Using Sokal's equations and tuning procedure, values C_{1A}= 873pF and C_{1B}= 427pF were calculated for Q_L= 11.

2.9 Simulation results



V_{PULSE} is a pulse source of 4V with a duty cycle of 50%. C_{1A}= 873pF, C_{1B}= 427pF, L1=66μH, R_{LOAD}= 37.7Ω. L_{RFC}= 1mH. Vdd=5V.

Figure 2.13: Class-E circuit for simulation

Figure 2.14 below illustrates the non-overlapping current and voltage waveforms. Figure-2.15 illustrates a current of 68mA from the 5V voltage source. Notice that the current waveform in Figure 2.15 has a ripple. The presence of ripples is one of the non-idealities involved in Class-E circuits arising due to inductance not being too big. The load current is a sinusoid with amplitude of 131.7mA.

Input power = 5*0.068 = 0.34 W

Output power = $.1317^2$*Rload/2 = 0.327 W

Efficiency = 96.2%

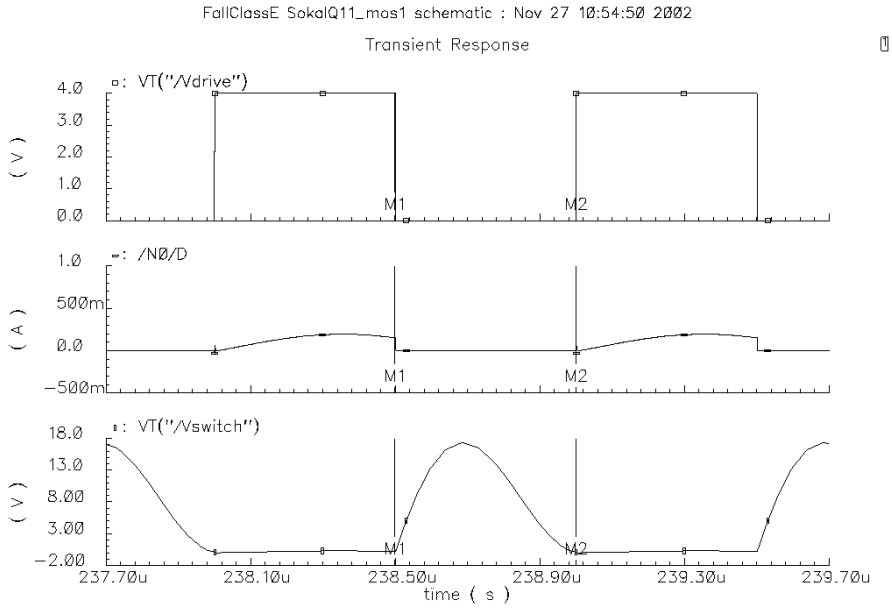


Figure 2.14: Class-E active device voltage and current

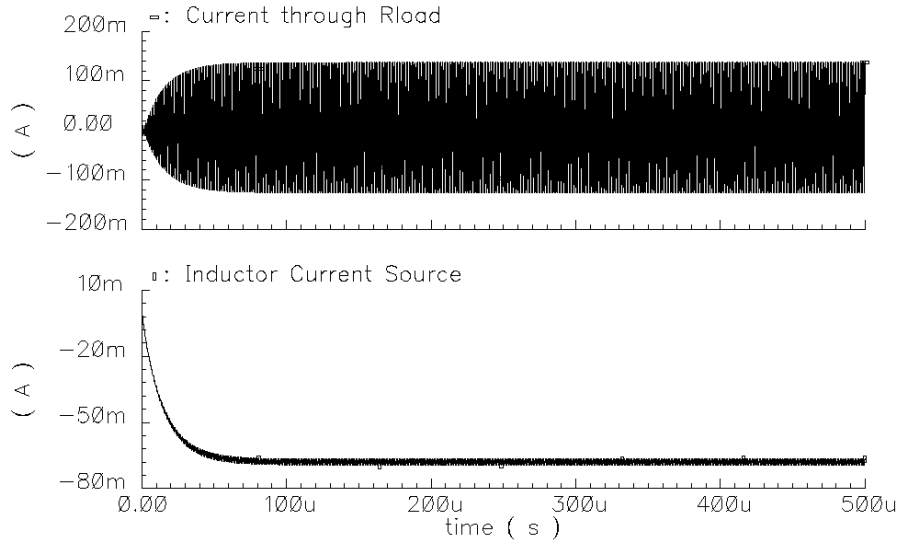


Figure 2.15: Load current and RFC inductor current containing ripples

2.9.1 Output power variation with Voltage supply

Vsupply	Load Current	Load power	Input power	Efficiency
3	0.07762	0.1136	0.1188	95.62
4	0.1042	0.2047	0.2148	95.3
5	0.1317	0.327	0.34	96.17
6	0.1585	0.4738	0.4929	96.12
7	0.1852	0.647	0.6745	95.93

Table 2.1: Load power versus Supply voltage table

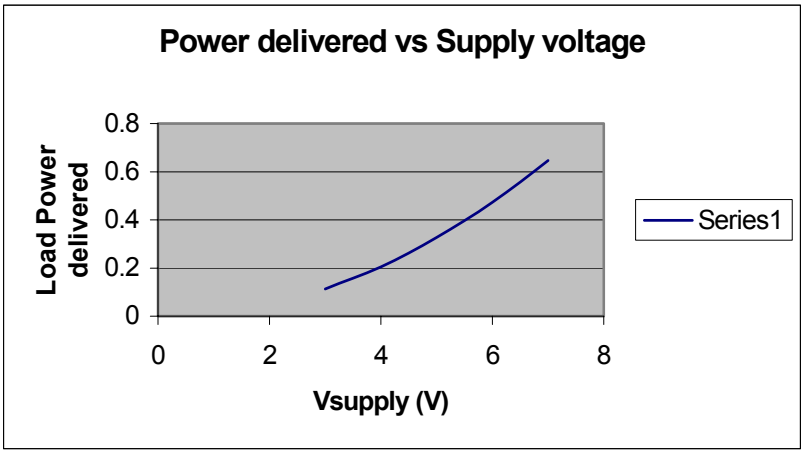


Figure 2.16: Load power versus supply voltage plot

The load power has a linear relation with respect to the supply voltage, as shown in Figure 2.16.

Chapter 3

Back-telemetry Communication

3.1 Secondary side circuit details

The power transmitter for the inductive link uses a high efficiency Class-E power amplifier to drive the transmitter coil. The coil is inductively linked to implanted unit and the induced waveform on the secondary side is rectified to provide the +7V/-7V DC supply for electrode stimulation and DC logic.

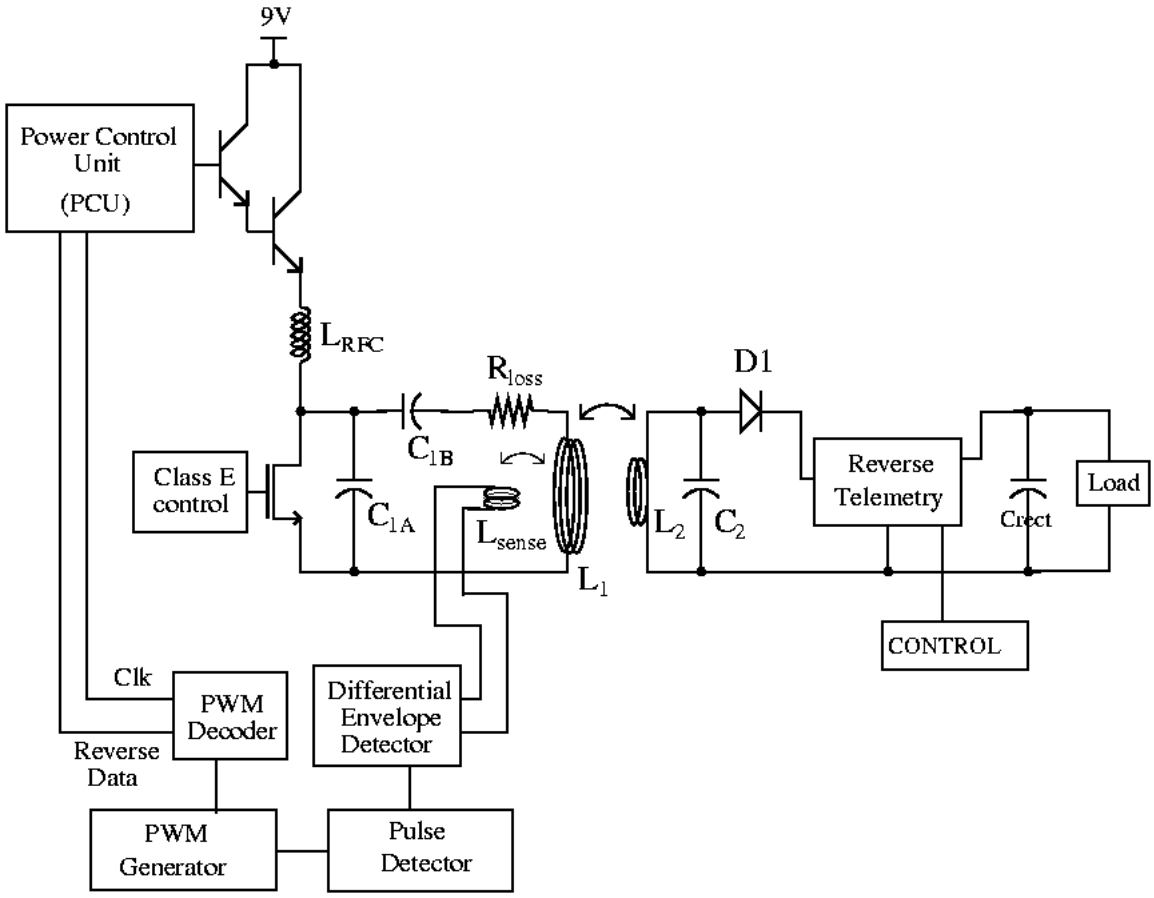


Figure 3.1: Power link block diagram

In the implanted unit, rectification is achieved via a single-phase rectifier and an off-chip charge storage capacitor (Cs). The voltage regulators generate the dual rail supply on the secondary side. An initial shunt type regulator provides current regulation and coarse voltage regulation. A series-type regulator provides the necessary fine voltage regulation required for subsequent stages [4,13].

3.2 Need for back-telemetry communication

The coupling coefficient between the primary and secondary coils is susceptible to changes as the shape of the coils and the distance between them might change with time. This changes the mutual inductance and hence changes the reflected impedance on the primary side. This changes the coil voltage on the primary side and the induced voltage on the secondary side. Hence the rectified voltage available across the secondary might change from the required value of 14V. This is not tolerable and must immediately be fixed. Hence there is a need for a feedback of information from the secondary unit to the external unit. This back-telemetry communication is accomplished using load modulation. Along with the voltage information to improve power regulation efficiency related to induced voltage, it is necessary to transmit information like electrode impedance and chip temperature. Once the external unit receives this information, it is processed and the appropriate adjustments are made to the system. For example, a power control unit has been designed to use the back-telemetry data to control power delivered to the secondary side. A low data rate of 5kbps has been used for back-telemetry communication.

3.3 Back-telemetry load modulation

One common way of achieving ASK through an inductive couple consisting of a pair of RF coils is to modulate the resonant capacitance or coil inductance of the power receiving secondary circuit. The resultant shifts in the resonant frequency are reflected back upon the external coil as changes in the voltage amplitude across it. However the RF power link efficiency is reduced. An alternate more efficient technique called Load Shift Keying (LSK) or reflectance modulation [5], allows simultaneous powering and data transmission through the same RF inductive couple. LSK utilizes the property of an inductive couple in which a change of the secondary load is reflected onto the primary coil as a varying reflected impedance.

Consider the circuit shown below:

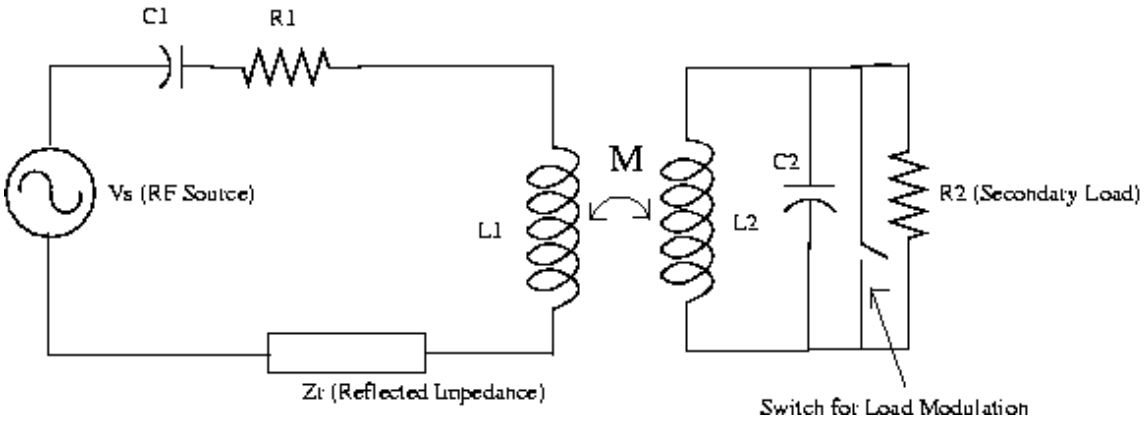


Figure 3.2: Load modulation circuit

In the above circuit, Zr is the reflected impedance that becomes a part of the total impedance on the primary side.

The above circuit has different values of Zr when the switch is open and when the switch is closed. But this traditional way of performing LSK is not applicable in the power link as the micro-stimulator cannot be short-circuited. To avoid this, a different configuration is used to create load modulation as shown below [4]. Here, the load is disconnected for a short duration and a charging capacitor (Cs) is employed to hold the voltage across the load during that period.

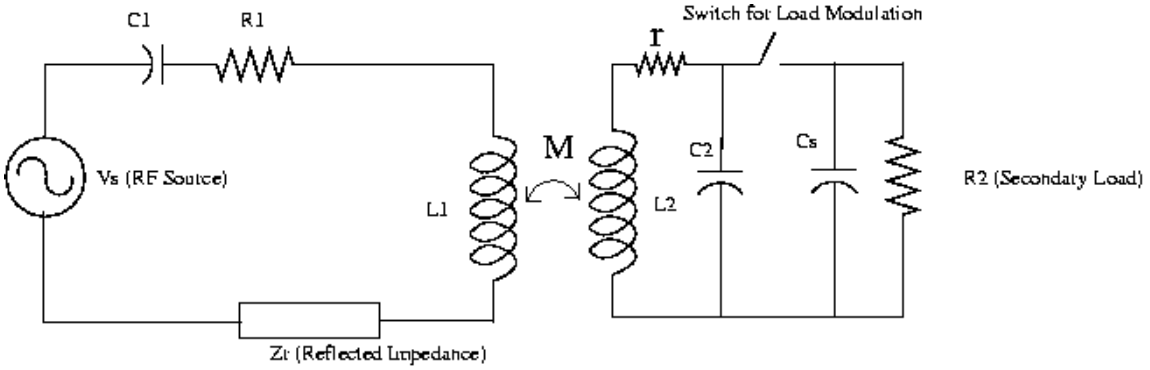


Figure 3.3: Alternate load modulation configuration

Equations related to reflected impedance:

Let Z2 be the impedance on the secondary side; When the switch is closed on the secondary side, the secondary impedance is given by:

$$Z_2 = j\omega L_2 + \left(\frac{1}{R_2} + j\omega C_2\right)^{-1} \quad (3.1)$$

When the switch is open, the secondary impedance is given by the equation:

$$Z_2 = j\omega L_2 + \left(j\omega C_2\right)^{-1} + r \quad (3.2)$$

Under the condition of resonance in the secondary side and when the switch is open, the impedance becomes:

$$Z_2 = r \quad (3.3)$$

The reflected impedance is given by the equation:

$$Zr = \frac{(\omega M)^2}{Z_2} \quad (3.4)$$

The reflected impedance changes with the position of the switch and this changes the Q-value of the system. It should be remembered that the load is not constant and draws varying amounts of current. The micro-stimulator load consists of several current drivers and depending on the data received from the forward data link, the electrodes draw different amounts of current. However, for simplicity of modeling, the micro-stimulator load is approximated to a constant resistance load.

3.4 Transient waveforms for data transmission

The reflected impedance value is different when the switch is open and when it is closed. This change in the reflected impedance causes the current and voltage values to change. During the period when the position of the switch changes, there is a transient voltage disturbance across the coils because of the change in the reflected impedance. This transient waveform has been used in a simple but novel data transmission scheme.

As explained earlier, the Q-value of the system changes with the position of the switch. However, the Class-E circuit has been designed to have optimum efficiency for only one of the Q values. Originally, an ASK modulation scheme for the transmission of data was planned. This will mean that the switch is operated at the transmission frequency and is switched ‘on’ or ‘off’ depending on the bit to be transmitted. However, there are different constraints. The power transmission efficiency gets lowered because of the constant

changes in the system Q value. Also, since the open position of the switch means that the charging capacitor (Cs) provides power to the load. Hence, Pulses with very low 'off' duty cycle is used to represent the data.

The voltage pulse connected to the switch is used to disconnect the load for a short duration and then connect it back. Using short pulses ensures that the load is disconnected from the source only for a short duration. As explained earlier, when the position of the switch changes the load, a transient rising voltage waveform is generated across the coil. The primary inductor voltage is sensed with a loosely coupled coil (i.e K=0.03) and transient waveforms are detected with a differential envelope detector for increased noise immunity.

3.5 Encoding and data rate for reverse telemetry communication

Traditional PWM encoding cannot be employed for data transmission, as the duty-cycle needs to be low. Hence, novel variation of PWM encoding is employed for reverse telemetry communication, as shown in figure-3.4 below. Two pulses are involved in the transmission of every single bit.

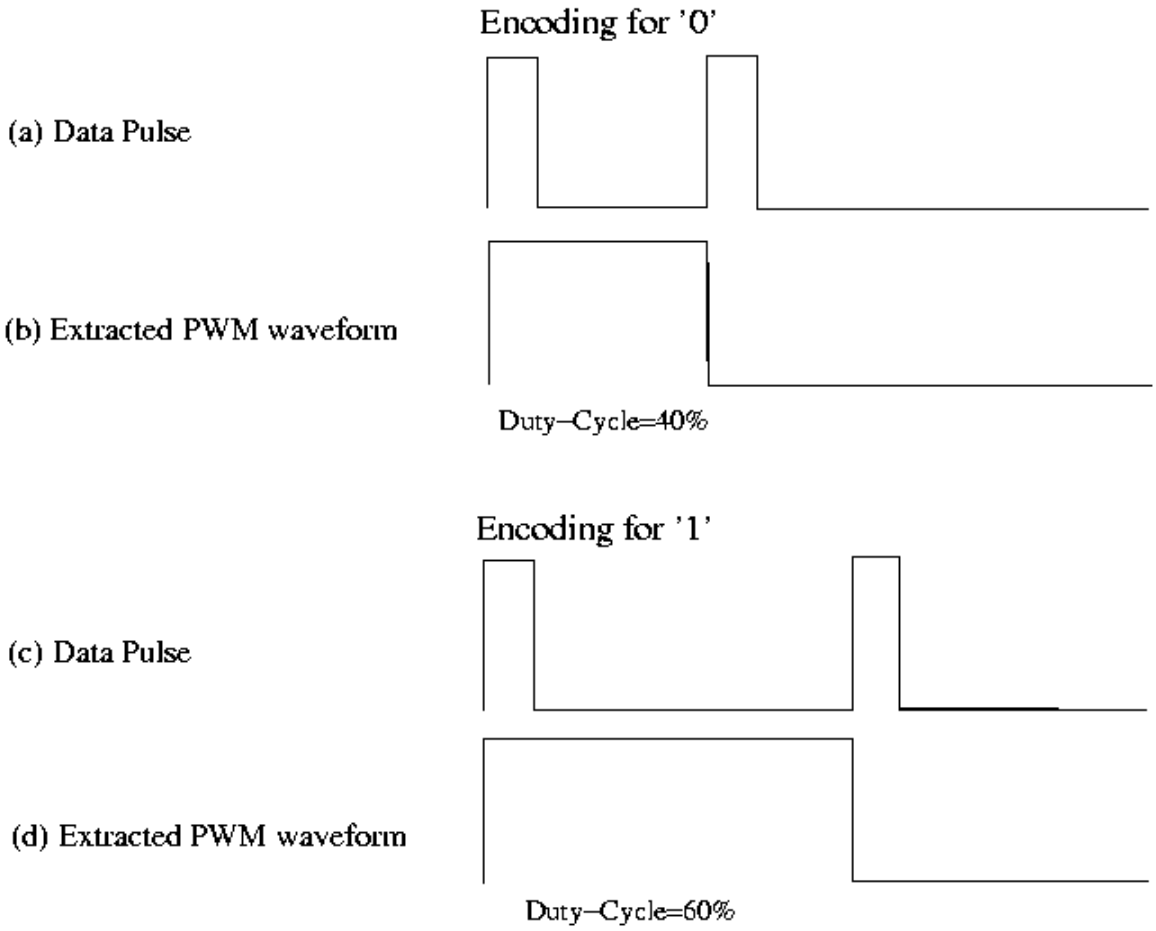


Figure 3.4: Novel variation of PWM encoding

The data pulses are timed as illustrated above, so that a PWM waveform can be extracted. A duty cycle of 40% had been chosen to encode '0', and 60% has been chosen to encode '1'. Each time this data pulse is applied on the secondary side, the transient waveform explained in the previous section is triggered. Care should be taken to make sure that the transients die down before the next data pulse is exerted. This imposes the limitation on the data rate, as there is a minimum time gap required between two successive pulses. Through simulations spanning the range [12] of acceptable k values, it was found that a data rate of more than 6Kbps does not yield reliable data communication. A data rate of

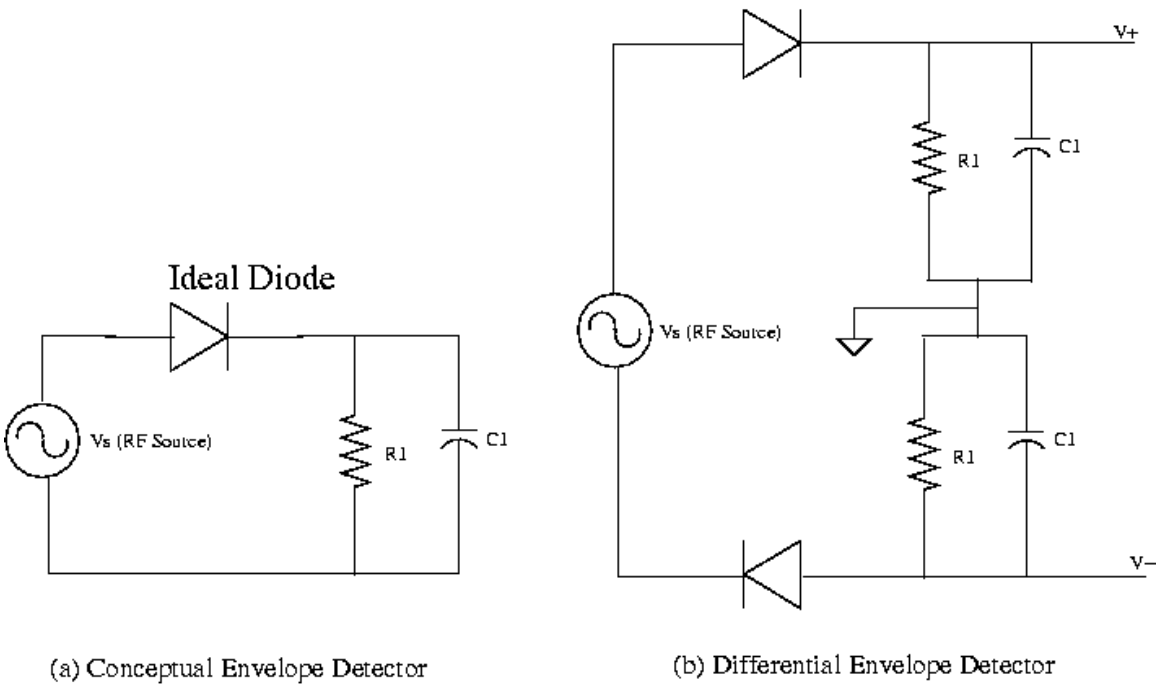
5Kbps has been chosen for reverse telemetry communication. This is still subject to change, depending on the control system analysis of the entire power control system [13].

3.6 Components for back-telemetry data detection

The power level on the secondary level is sensed and the data is transmitted back to the primary by controlling the secondary load with the reverse telemetry switch. The data detection unit on the primary side consists of an envelope detector, PWM generator and a PWM decoder. A variation of PWM encoding has been used so that PWM reverse-telemetry data can be recovered on the extraocular unit. The PWM decoder provides the decoded data and the clock to the power control unit that changes the supply voltage for the Class-E amplifier, thus regulating power. PWM encoding has been used to combine data and clock into a single bit-stream. Each unit's function and design has been discussed in detail below.

3.6.1 Envelope Detector

The conventional envelope detector shown below in Figure 3.5(a) consists of a parallel RC network. The diode works as a rectifier and passes current in a single direction and blocks negative voltage values from the RC network. The RC network acts as a low-pass filter that removes high-frequency components so that only the smooth envelope remains. Roughly the operation of this circuit is as follows. When the input voltage is greater than the voltage across the capacitance, the output voltage tracks the input. When the input voltage falls below the output voltage, the output voltage decays exponentially with time constant 1/RC.



(a) Conceptual Envelope Detector

(b) Differential Envelope Detector

Figure 3.5: Envelope Detector

The differential envelope detector, shown in Figure 3.5(b), has been used to detect both the positive and the negative envelopes. The DC levels of these two envelopes are adjusted and then passed through a comparator. These two envelopes are now passed through a comparator to detect the transient disturbance in the coil voltage. This is used to detect the data. Differential envelope detector provides for increased noise immunity as it uses both envelopes.

3.6.2 Pulse Detection Unit

The voltage on the primary coil is sensed with a loosely coupled coil and passed through a differential envelope detector. The positive and negative envelopes are compared to produce the detected pulse. However, there are several problems that need to be solved for successful pulse detection.

3.6.2.1 Issues in pulse detection

The voltage envelopes consist of a series of spikes during load modulation, with slowly varying waveform in-between the spikes. The variations in-between the spikes depend on the changes in the induced voltage brought about by the power control unit. Back-telemetry data is used to achieve power control. For successful pulse detection, the spikes in the envelopes need to intersect while the slowly varying portions do not intersect. This will ensure that the envelopes can be fed to a comparator to output the detected pulse.

To achieve the above objective, the following tasks need to be performed:

(a) Amplify the spikes in the envelopes.

(b) Suppress the slow variations in the envelope in between the spikes.

(c) Manipulate the DC levels of the detected envelopes.

The implementations of these tasks interfere with one another, and the correct balance has to be achieved during circuit design to accomplish proper pulse detection. The different scenarios in pulse detection are explained below.

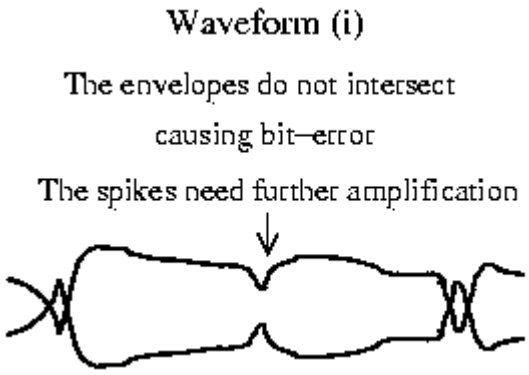


Figure 3.6: Non-intersection of spikes in envelope

Figure 3.6 illustrates the case where some of the spikes do not intersect. The spikes need to intersect for pulse detection. Hence the spikes need to be amplified.

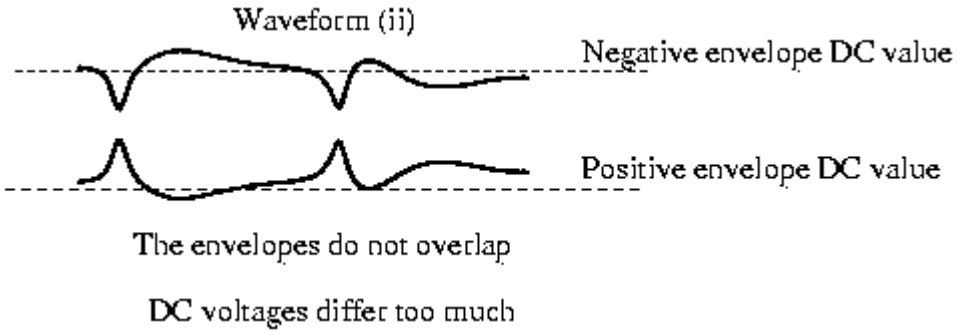


Figure 3.7: Widely separated envelopes

The DC levels of the two envelopes can be separately adjusted to give the two envelopes proper separation, so that they overlap in the required manner. In Figure 3.7, the two envelopes are separated too much and do not overlap anywhere. The difference in their DC levels needs to be reduced.

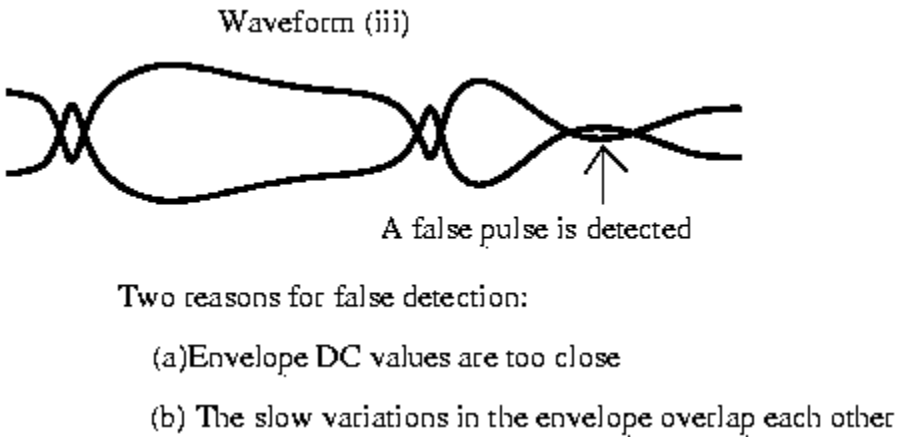


Figure 3.8: Detection of a false pulse

Figure 3.8 illustrates the possibility of the detection of a false pulse. It might happen if the envelopes are too close, in which case their average DC value should be adjusted to separate them. Also, the slow variations in between spikes should be suppressed to avoid the above situation.

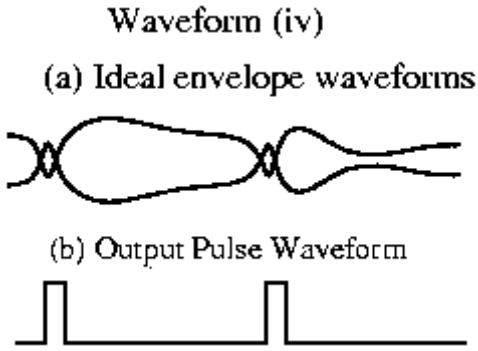


Figure 3.9: Ideal envelope waveforms

Figure 3.9 shows the ideal envelope waveforms for pulse detection. The output pulses have been also been illustrated. The envelopes at the output of the envelope detector circuit do not satisfy the requirements for proper pulse detection. They need to be processed through additional circuitry to meet the conditions.

3.6.2.2 Pulse Detection Circuit

DC block capacitors are cascaded to the output of the differential envelope detector. The envelope is then passed through dual amplifier system followed by a comparator and a differential to single level converter as shown in Figure 3.10.

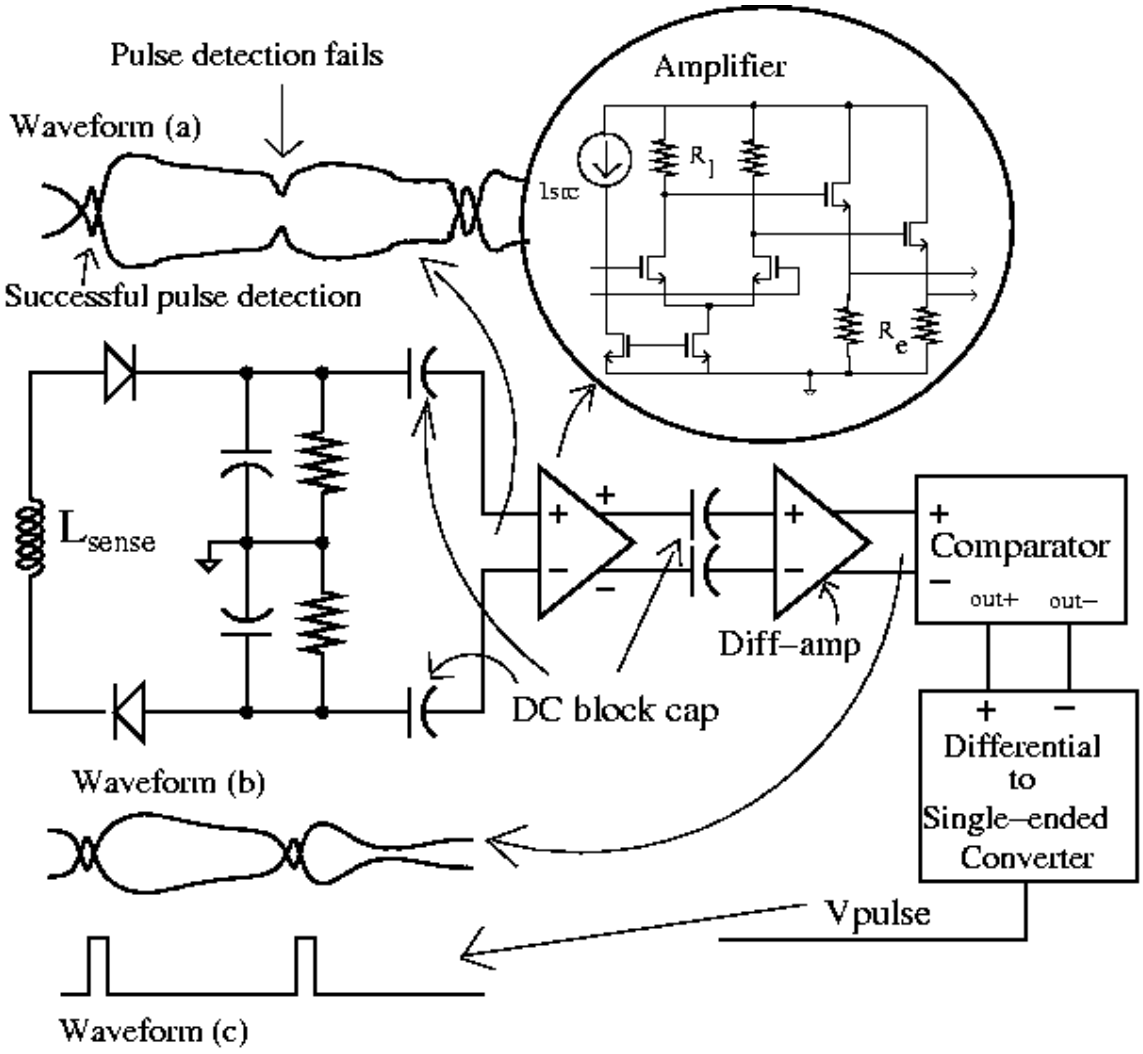


Figure 3.10: Pulse Detection Unit

The first amplifier used consists of a simple open-loop differential amplifier cascaded with a source-follower. The components used in the differential amplifier are: Isrc=400μA; R_l=10KΩ. The differential amplifier DC-gain is 8.3 (18.4db). The differential amplifier input gates are biased at 2.5V. The source follower is used as a

buffer to the next stage. Source followers are used as they offer a high input resistance and low output resistance. The source follower has a gain of 0.68 (-3.35db). The overall gain of this amplifier is 5.7 (15.05db).

This amplifier is followed up by DC block capacitors (C=1nF) to filter out the variations in between the spikes. A second differential amplifier, with a DC-gain of 2 (6.02 db) is used after the DC capacitor, to further amplify the spikes before they are fed to the comparator. The DC bias value of this amplifier is adjusted so that the envelopes have optimum separation between them at the input of the comparator. This manipulation of the DC bias values helps to achieve increased noise immunity, as the positive and negative overlaps are well separated except during the occurrence of the spikes when they overlap. The input DC bias values of the second differential amplifier are 3.33V and 3.7V. The output DC bias voltages are 3.02V and 4.92V.

Two separate amplifier stages have been employed instead of a single amplifier with a larger gain. This distributed amplifier system results in a higher bandwidth compared to a single amplifier, which is important considering the high frequency spikes that need to be amplified. Also, employing a second differential amplifier provides greater flexibility to adjust its DC bias values, and thus manipulate the vertical separation of the two envelopes. Replacement of the double amplifier system with a single amplifier can be a topic for further investigation. The overall design and the component values of the amplifiers were modified and finalized after several simulation runs of back-telemetry

communication system to ensure that the spikes overlap for all possible values of coupling coefficient between the intraocular and extraocular coils.

At the output of this double amplifier circuit, the two differential envelope waveforms are ready for comparison. A comparator with hysterisis is employed to ensure that the comparator is not sensitive to small changes in the input. A differential to single ended conversion circuit is employed to output the detected pulse.

3.6.3 PWM Generator

The advantage of PWM encoding is that the clock is contained in the data itself and hence extra circuitry like PLL is not needed to extract clock from data. As explained earlier, it is not possible to use PWM waveforms directly on the secondary side, as the load cannot be disconnected for a long period. Hence, narrow pulses are employed on the secondary side for load modulation. The pulses on the secondary transmission side are timed such that when they are passed through a toggle flip-flop, they generate the PWM waveform. The pulses are recovered by the pulse detection unit on the primary side and used to generate PWM waveforms.

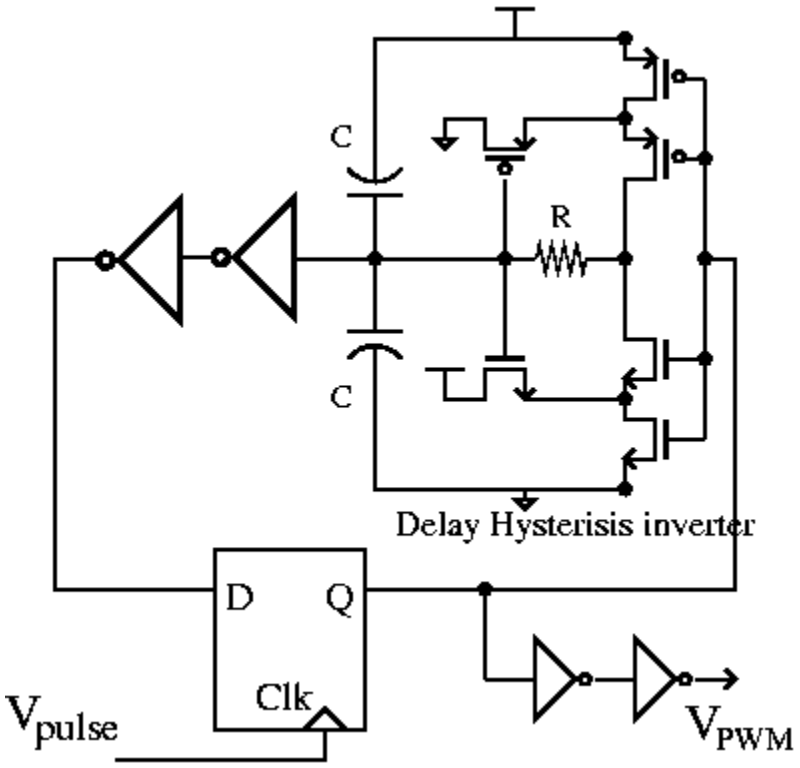


Figure 3.11: PWM Generator

As shown in Figure-3.11, the toggle flip-flop used consists of a D-FF with Q and D pins connected by three inverters, one of which has a delay hysterisis. The detected pulse acts as the clock to the D-FF as shown above. The additional delay hysterisis inverter guarantees that the output toggles to the first incoming edge and remains insensitive to any input change for approximately 6μs. This feature is necessary so that the PWM waveform generated is not disturbed by any random variations in the transient disturbance for the duration of the telemetry burst, which is set to 4.7us. Despite using comparator with hysterisis in the pulse detection stage, it is still possible that the detected pulse is fast changing instead of one single pulse. The delay hysterisis inverter takes care

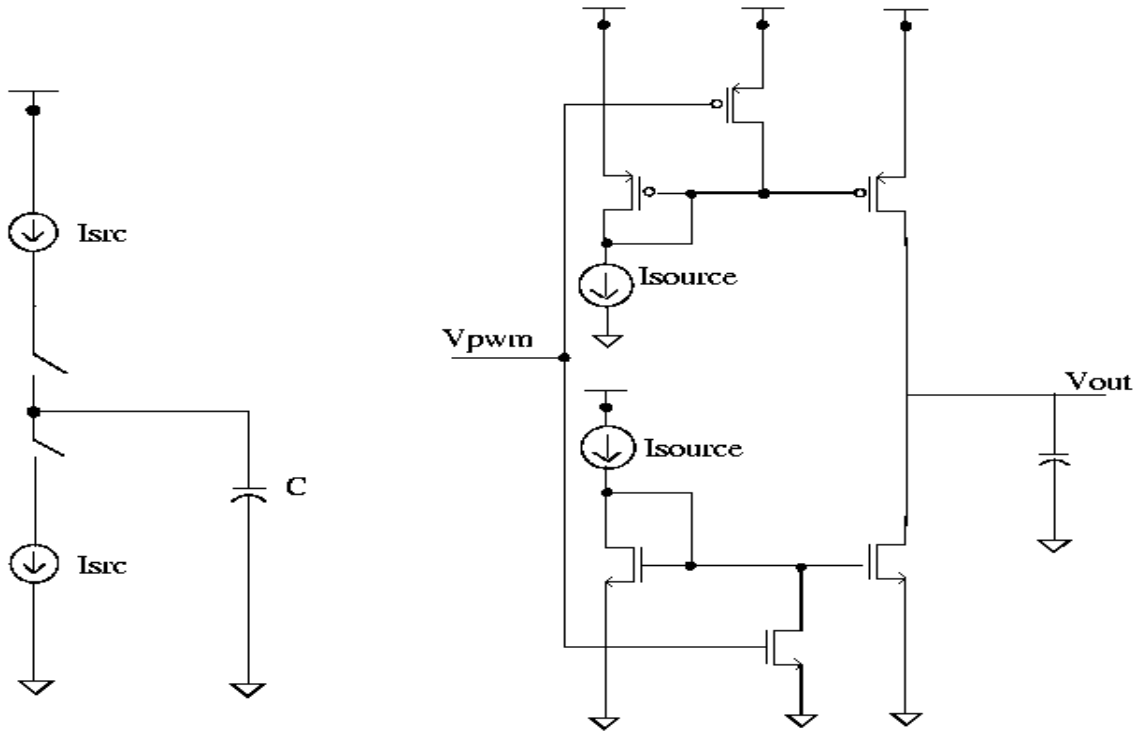
of this event by providing a delay of approximately 6μs, which depends on the product RC of the resistor and the capacitor used. The components for the delay hysterisis is resistor R=10KΩ, and capacitor C=200pF. These values were decided by simulating the delay hysterisis inverter, and then adjusting resistor and capacitor values to obtain the required delay between input and output waveforms.

3.6.4 PWM Decoder

PWM Decoder consists of a charge-pump integrator and a comparator. The PWM waveforms employed in reverse telemetry communication consists of pulses with two different duty cycles for the digital high and low states. The PWM decoder has to differentiate between the duty cycles. This can be done using a charge-pump integrator and a comparator. The charge pump integrates the PWM waveform and the comparator is set to output the NRZ data.

3.6.4.1 Charge Pump Integrator

Charge-pump integrator is used to help differentiate between the two different duty-cycles used in the PWM waveforms.



(a) Conceptual Charge Pump (b) Actual Charge Pump

Figure 3.12: Charge Pump

Equations defining charge pump capacitor voltage is given by the following equations.

$$Q = CV = \int Idt \tag{3.5}$$

$$\Delta V = (I / C) \int dt \tag{3.6}$$

$$\Delta V = (I / C) \Delta t \tag{3.7}$$

The voltage across the capacitor in the charge pump is directly proportional to the 'on' duration of the PWM waveform, which in-turn is decided by the duty cycle. This voltage is fed to the comparator whose other input is set to an appropriate threshold value. The value of the current source and the capacitance is related to the duty cycle and the frequency of the PWM waveform. The component values used for the charge pump are explained in the later section.

3.6.4.2 Comparator

Voltage comparator compares the instantaneous values of two analog voltages and generates a digital 1 or 0 indicating the polarity of that difference. The dominant application of comparators is in A/D converters.

There are different kinds of comparators: comparators with latch and without latch. Comparators without latch have a high-gain amplifier and a single ended large swing output that is compatible with driving digital logic circuits. Comparators with latch have an additional strobe input. If the strobe input is high, the input stage is disabled and the digital output is stored in a latch until the strobe signal is made low. Latch comparators can be implemented as a combination of a high gain amplifier and a simple digital latch or as a low gain amplifier and high-sensitivity latch.

The latch comparator used here was proposed by Yukawa [14] and consists of discharge transistors, an n-channel flip-flop with a pair of n-channel transfer gates for strobing, p-channel flip-flop, and p-channel pre-charge transistors.

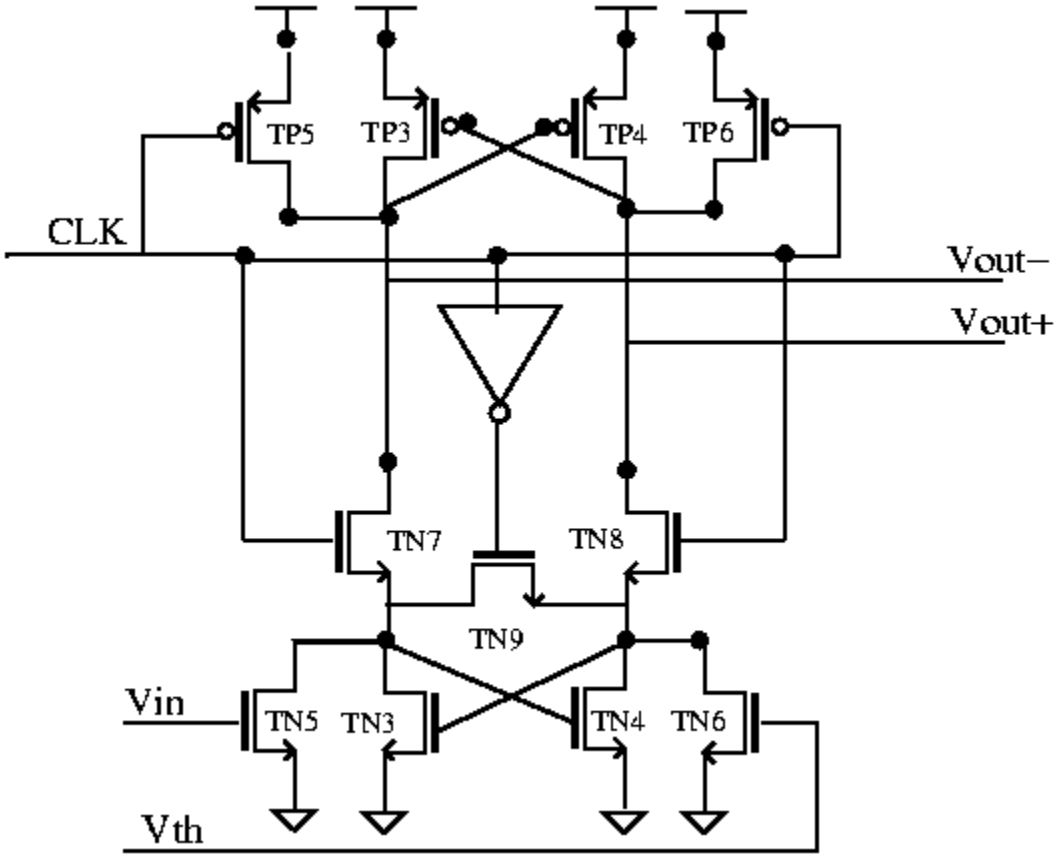


Figure 3.13: Latch Comparator

The dynamic operation of this circuit is divided into the reset interval and the comparison interval. At the reset interval, Clock is low, transfer gates TN7 and TN8 are off and p-channel pre-charge transistors TP5 and TP6 are on. Therefore, both the p-channel flip-flop nodes, formed by TP3 and TP4, are charged up to power supply voltage level. The n-channel flip-flop nodes, formed by TN3 and TN4, are discharged to ground level through n-channel discharge transistors. When the Clock goes high, charging current starts to flow from the p-channel side to the n-channel flip-flop. A part of the current is discharged through discharge transistors TN5 and TN6 whose gates are controlled by the inputs. Since current values differ between two discharge transistors, a large voltage difference is obtained when the n-channel drain voltages exceed the threshold voltage.

Voltage gain is amplified quickly after the flip-flop reaches more than unity gain. The amplified difference is transferred through the transfer gates and amplified to a voltage swing nearly equal to the power supply voltages.

One of the main constraints in the comparator design is the common mode input voltage range. In Yukawa's original proposal, a differential amplifier is used before the comparator stage. In our case, the two input voltages are directly fed to the comparator. One of the inputs to the comparator is an externally set DC voltage source that acts as a comparator threshold voltage. If this value is too high, then the corresponding n-channel gate will be on all the time and hence the comparator functionality is affected. If this value is lower than the threshold voltage, the comparator cannot function properly. Hence it is important to choose a proper value for the externally set threshold voltage as also the aspect ratios of the devices.

The aspect ratio for TN5 and TN6, whose gates are connected to the inputs, is 36μm/1.6μm, made bigger compared to the other devices. The aspect ratio for TN3 and TN4 that form a flip-flop is 12μm/1.6μm. The aspect ratio for TN5, TN6 and TN7 is 12μm/1.6μm. The p-channel flip-flop nodes formed by TP3 and TP4 also have the aspect ratio 24μm/1.6μm. The pre-charge transistors TP5 and TP6 have the aspect ratio 24μm/1.6μm. These values were finalized after repeated simulations.

3.6.4.3 Functioning of the PWM decoder

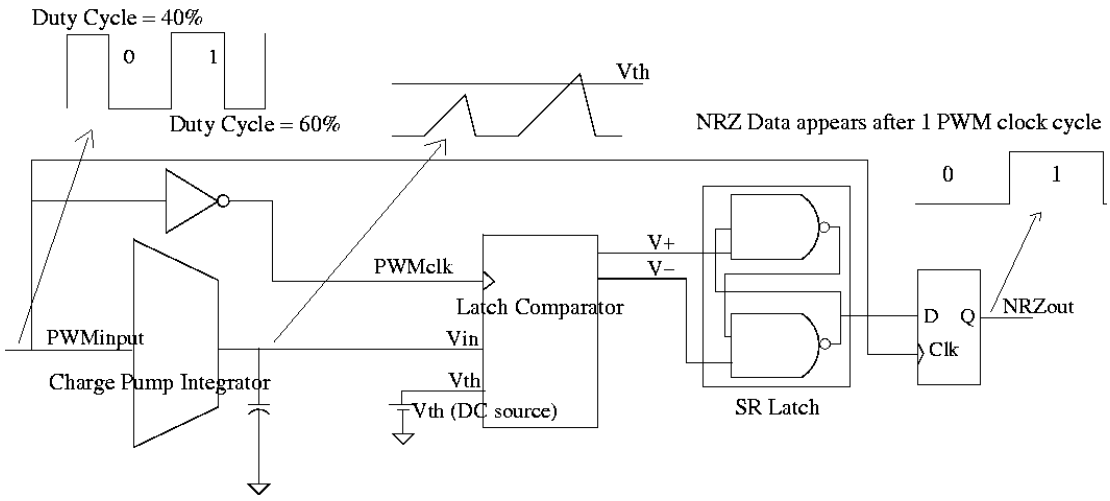


Figure 3.14: PWM Decoder

The PWM waveform from the PWM generator unit is input to the charge-pump integrator. During the ‘on’ or ‘high’ time of the PWM waveform, the output voltage of the charge-pump is linearly increasing with time. During the ‘off’ time, the output voltage is decreasing linearly with time. This gives the output waveform a triangle shape. The peak of the triangle occurs when the input transitions from ‘on’ to ‘off’, and the voltage value depends on the duty-cycle of the input pulse. The PWM waveform is inverted to act as the clock (CLK) input to the latch comparator. This makes the evaluation phase of the comparator compare the peak value of the triangle waveform with an externally set threshold value. The voltage threshold value is set to differentiate between the two different peak values. The latch comparator is sensitive and can differentiate between small variations in the duty cycle. The duty cycles representing ‘1’ and ‘0’ are chosen such that they are complementary to each other. That is they are symmetric around the 50% duty cycle. This is important so that if a pulse is missed

during data detection, the detected NRZ waveform will be complementary to that of the transmitted NRZ pulse.

The latch comparator is semi-dynamic. When the PWMclk is ‘low’, both V+ and V- are pulled up to Vdd. When the PWMclk input is ‘high’, evaluation phase begins. V+ and V- are fed to an SR latch. When both S and R inputs are high, the output of SR latch is unchanged. This property is used here to produce the NRZ waveform. A D-FF is used in the end for synchronization with the PWM waveform. The NRZ waveform is available at the output with a latency of one clock cycle.

3.6.4.4 Component values for charge-pump

The data rate for reverse telemetry communication is 5kbps. The values for the charge-pump and the two duty-cycles for data ‘1’ and ‘0’ have to be considered during the design of the PWM block. The duty-cycles have to be symmetric about 0.5. This is because, it is important that the inverted PWM waveform is also easily decoded. The reason for this is explained later in section 3.8.1.

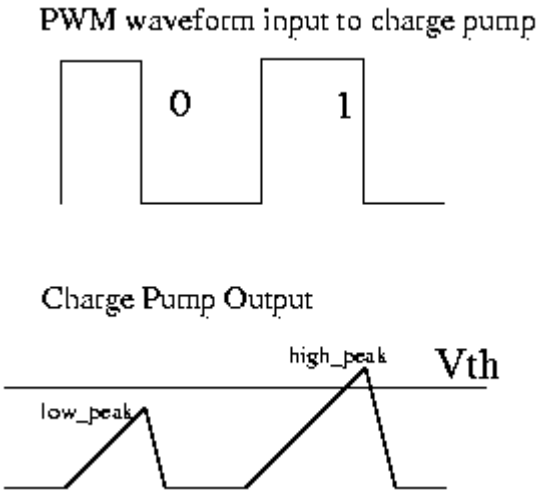


Figure 3.15: Charge pump input and output

The latch comparator employed in the PWM decoder has a range of acceptable values for Vth. The lower limit is set by the threshold potential of the MOS device used, which is 0.7V. It is undesirable to have a high value for Vth as it leads to high drain current to the device. The charge pump current source and capacitor values are related to the value of Vth. The value of the threshold value used is 1.28V. The current source used is 10μA and the capacitance is 200pF. The two duty-cycles chosen are 40% and 60%. Both duty-cycles are kept as close to 50% as possible, as the inverted waveform also has to be decoded without error. These values were chosen after multiple simulations.

3.6.5 Power Control Block

The power control block [15] performs the task of controlling the power transmitted through the inductive link. It uses the property of the Class-E power amplifier that the current drawn by the power amplifier remains a constant. Hence increasing the DC voltage source leads to more power being delivered across the inductive link. The Power Control Block processes the NRZ data that is recovered by the data detection unit. The

DC source for the power amplifier is increased if the data recovered is '1' and decreased if '0' is recovered. Hence power can be increased or decreased to the required extent through a series of steps. The recovered PWM waveform is used as the clock for the digital circuit involved and hence power control operates at the data rate.

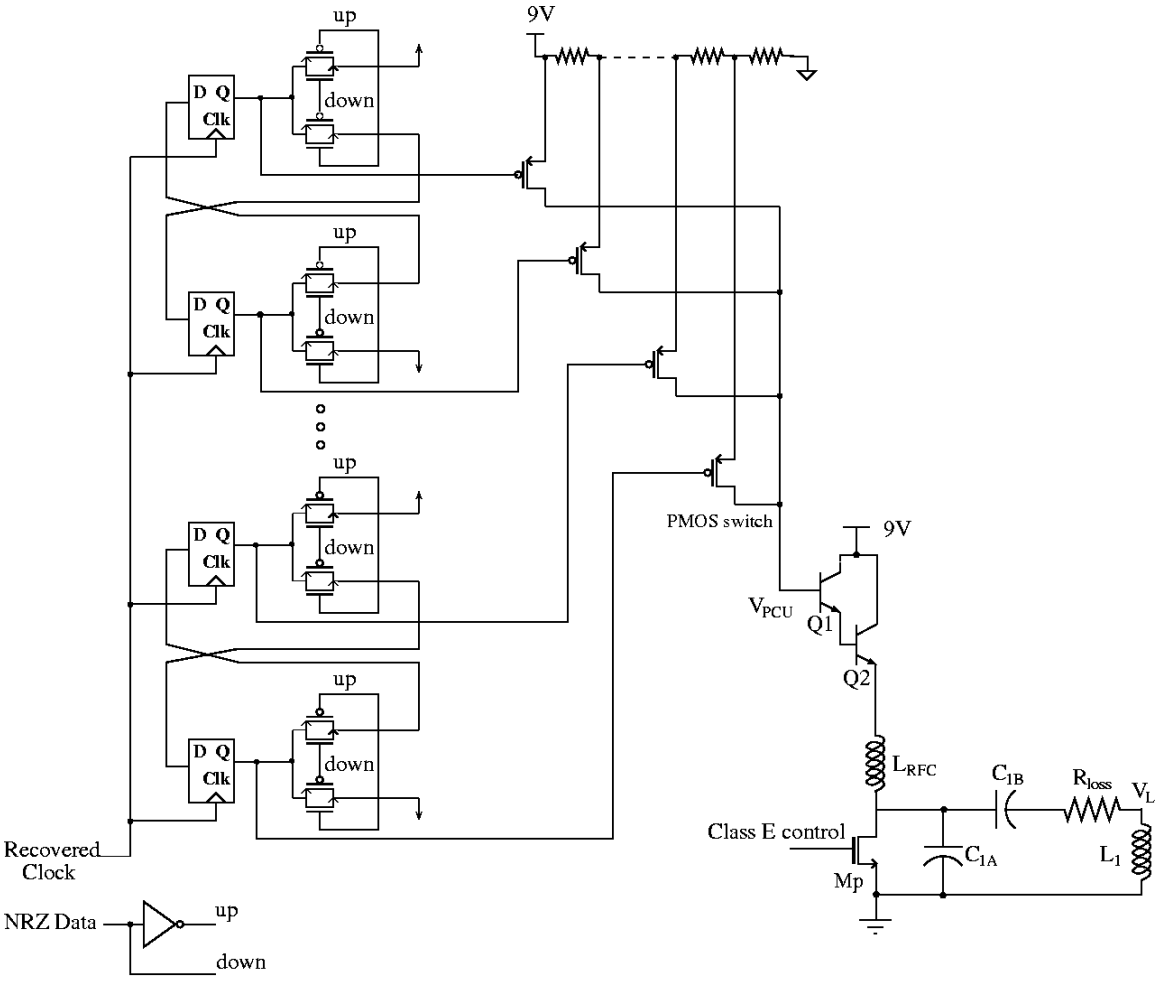


Figure 3.16: Power Control Block

Varying the DC voltage source for the power amplifier is achieved by tapping different voltage levels from a resistive potential divider. A shift register consisting of D-flip-flops and transmission gates is used to drive PMOS switches used to tap different voltage

levels from the divider. Only one of the DFF's will be high to drive the corresponding PMOS switch. The voltage can be stepped up or down by shifting the '1' in either direction in the shift register. The circuit provides sixteen power levels from 5V to 9V. A Darlington pair is used to minimize loading on the potential divider.

3.6.6 Reverse telemetry switch circuitry

The details of the reverse telemetry switch [13] are explained below. An off-chip capacitor Cs is used to supply power to the chip while P3 is off. A weak P4 transistor stays on at all times to provide initial charge to Cs during start-up and does not affect the back-telemeter operation.

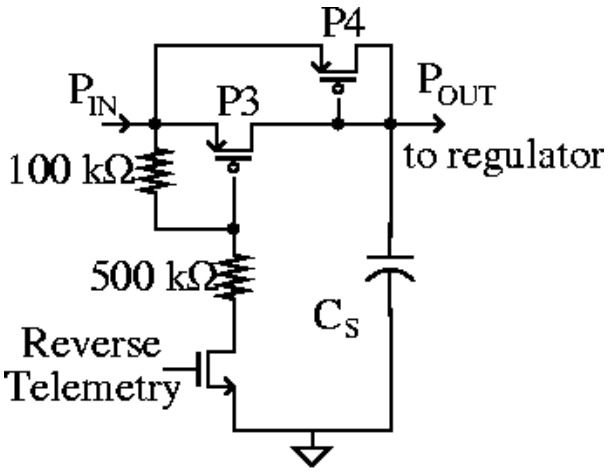


Figure 3.17: Back-telemetry switch arrangement

The aspect ratio of P3 (500μm/1.6μm) is made considerably larger than for P4 (20μm/4μm). This makes sure that the 'on' resistance of the device P3 is much smaller than that of P4. These values were finalized during simulations, and can be further investigated.

3.7 Power link simulation results

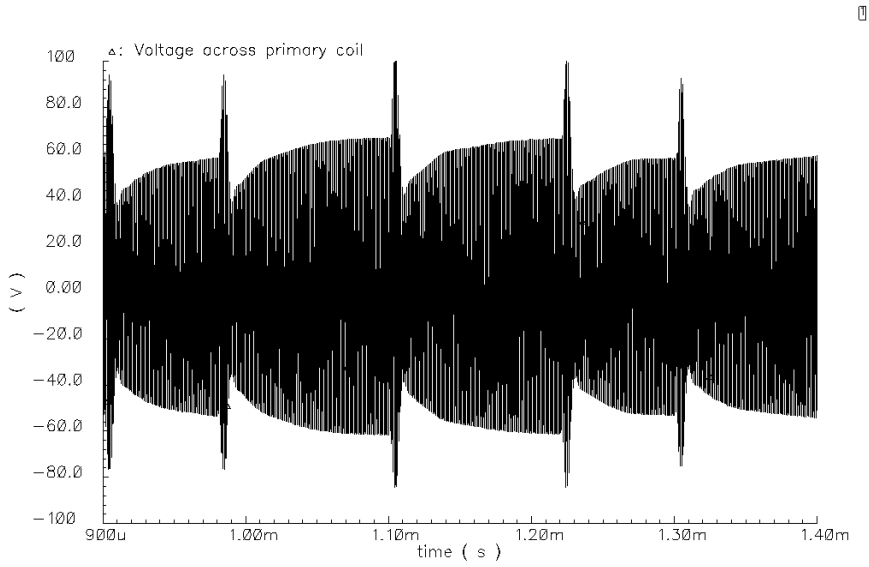


Figure 3.18: Primary coil voltage disturbance due to load modulation

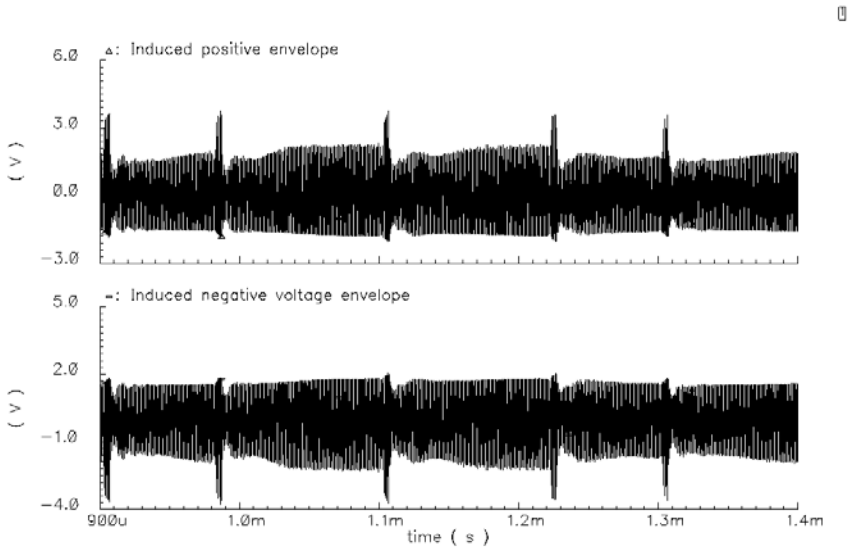


Figure3.19: Positive and negative terminals of primary envelope sense inductance

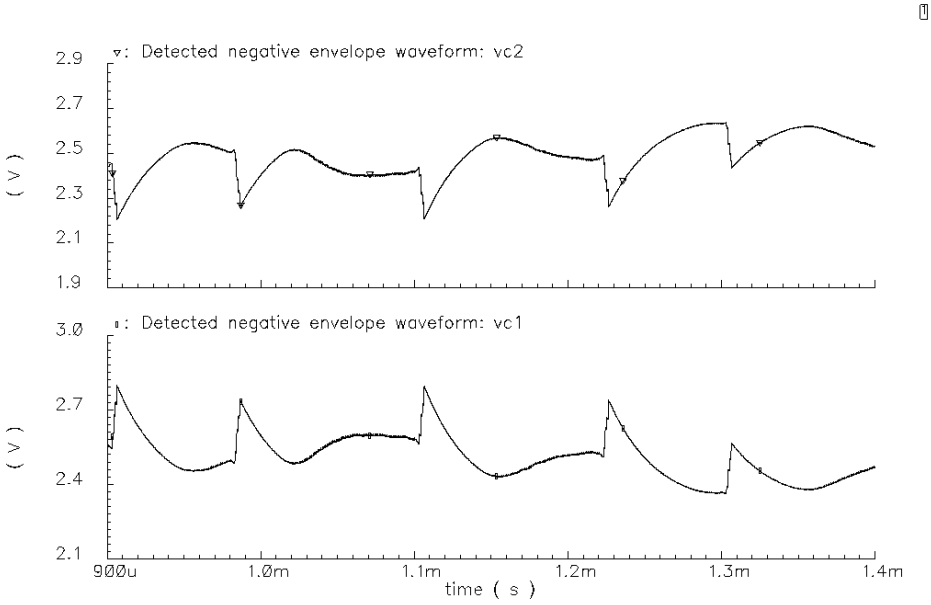


Figure 3.20: The positive and negative envelopes

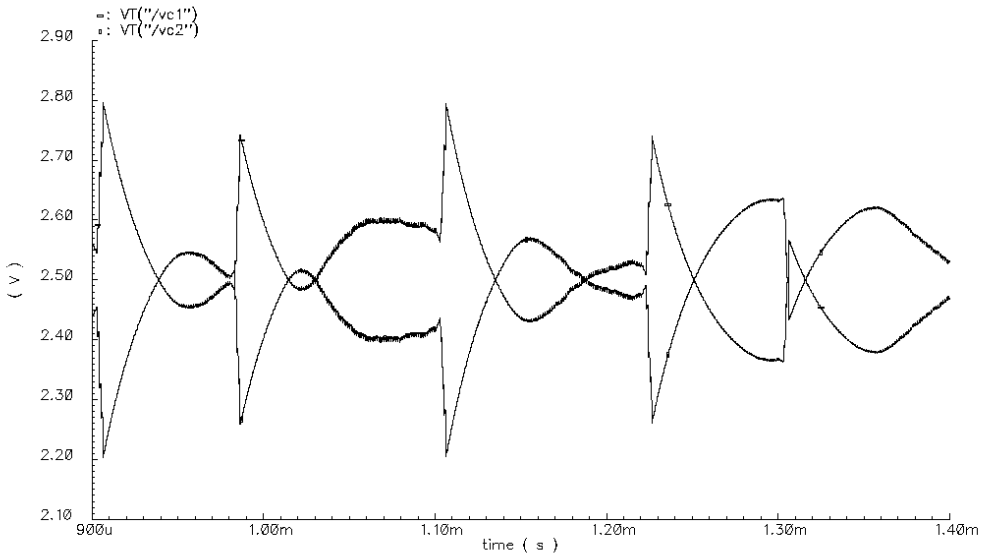


Figure 3.21: The overlapping envelopes input to Pulse Detection Block

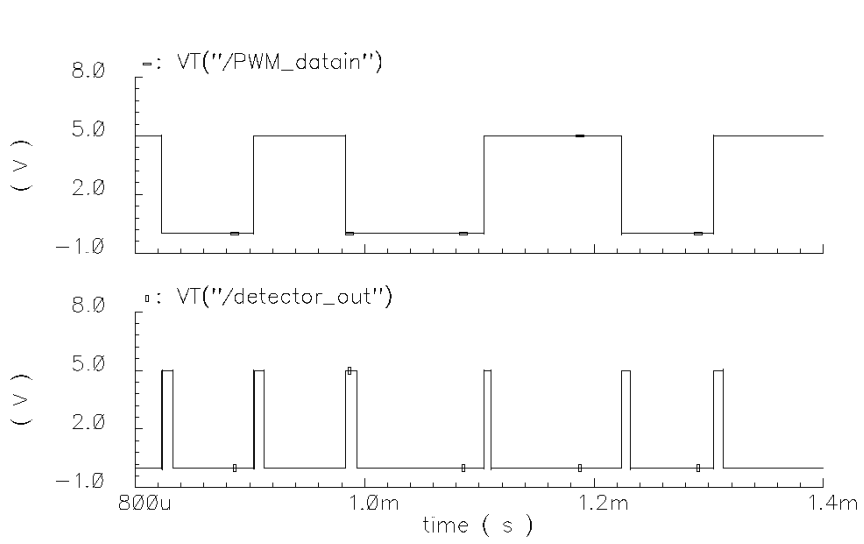


Figure 3.22: PWM Generator input and output

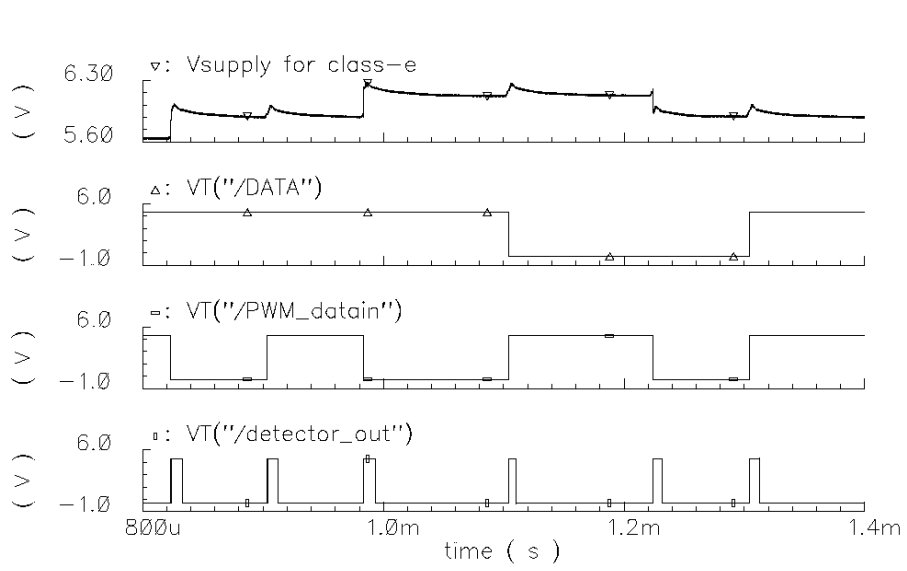


Figure 3.23: NRZ data from PWM waveform & Supply Voltage for power amplifier

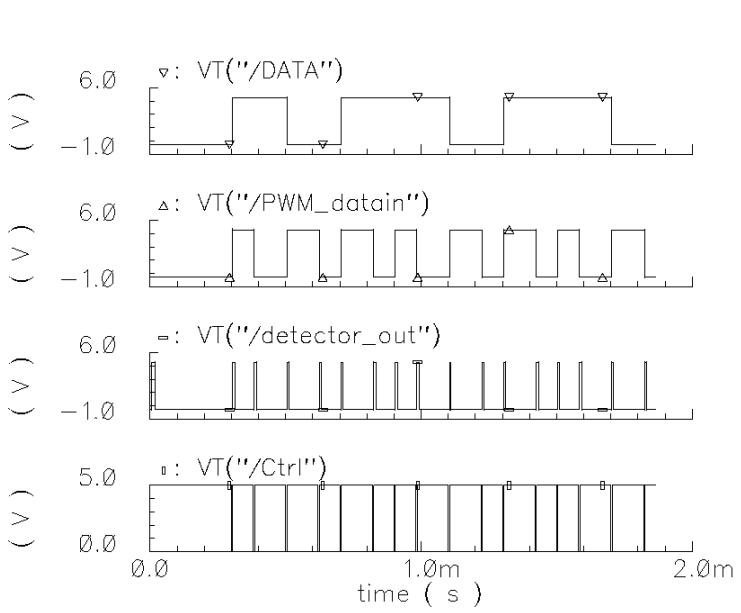


Figure 3.24: Decoded Data for 2ms duration

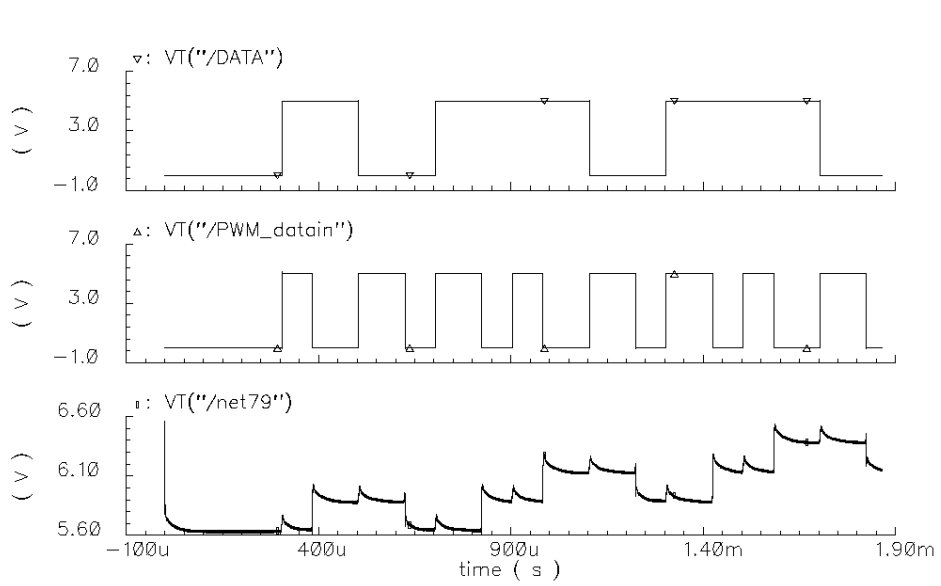


Figure 3.25: Waveform (net79) driving the Darlington pair, and the decoded data

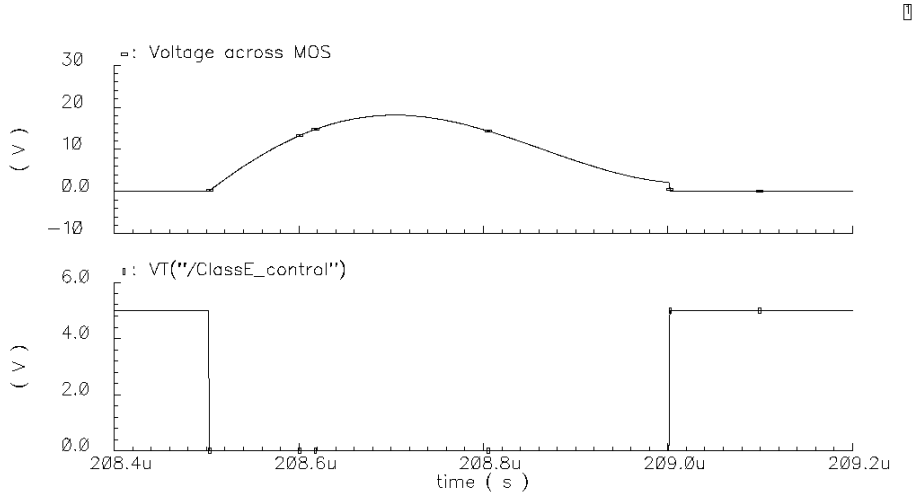


Figure 3.26: Class-E device voltage

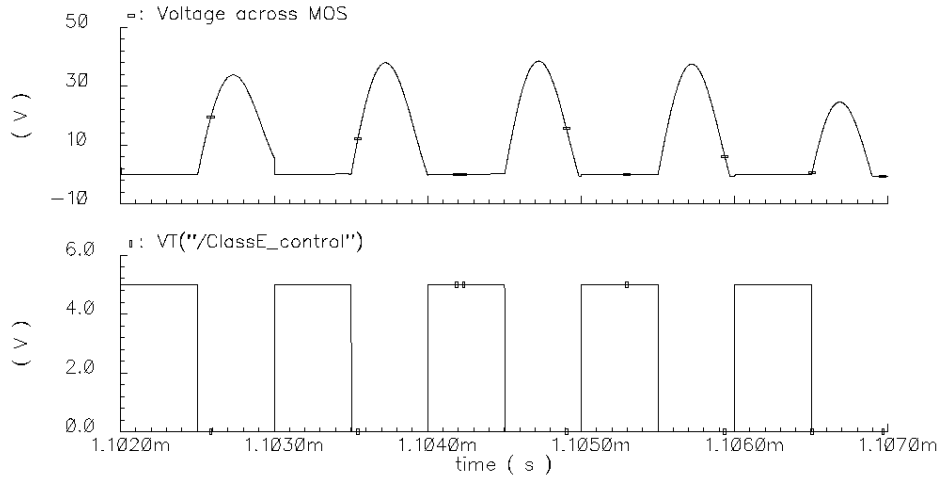


Figure 3.27: Class-E device voltage during transient disturbance

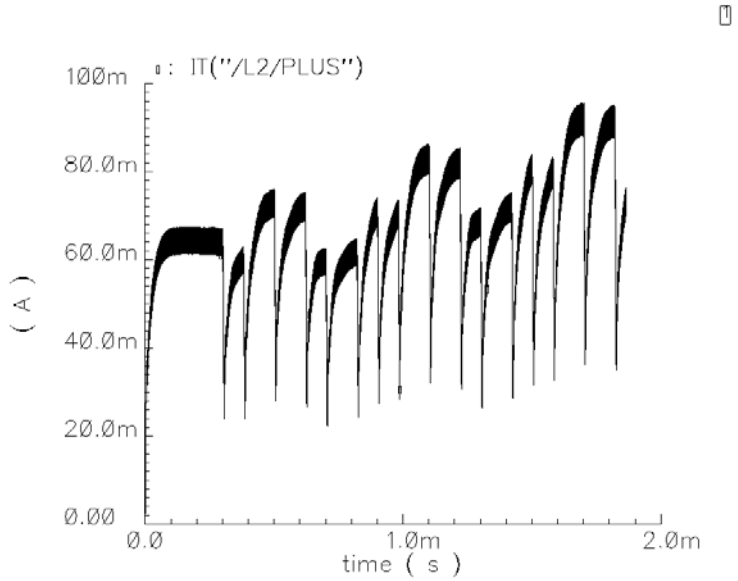


Figure 3.28: Input supply current source

Figure 3.25 indicates the recovered data on the primary side. There is a 1 clock-cycle delay between the transmitted data bit and the decoded NRZ data bit. The power control unit uses this data to change the supply voltage and hence the power delivered is regulated.

3.8 Proposed back-telemetry data packaging scheme

3.8.1 Differential encoding for back-telemetry data

Differential encoding is used to ensure that even if the recovered bit stream at the receiver is an inverted version of the transmitted bit stream, the original bit stream has been recovered. This is very important in our data detection scheme because, if a pulse is not detected, then the subsequent PWM waveform is inverted. Differential encoding

ensured that loss of a pulse means only one bit might be in error during data recovery. However loss of two successive pulses leads to the loss of a data bit. In other words, a data bit is dropped. It is very important that we have a mechanism to find out if the entire correct data is received. Hence it is necessary to follow a format that includes some error recognition aspects.

3.8.2 Proposed format for data packets

Each data packet will be 24 bits long. The first four bits will constitute the sync bit. Then every three bits will have 1 parity bit immediately following it, making a total of 15 data bits and five parity bits.

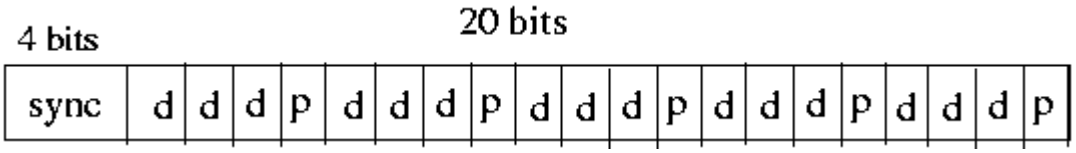


Figure 3.29: 24-bit data packet format

The sync bits, chosen to be 1111, are used to identify the beginning of the packet. Even parity is used so that the sync bits will not occur inside the packet.

Chapter 4

Conclusion

Several issues related to the design of the power link of retinal prosthesis have been discussed. A novel dual frequency approach has been adopted to deliver power and data to the intraocular unit using two separate coils.

Class-E power amplifier design methods have been studied. A Class-E power amplifier circuit has been designed to deliver power to the micro-stimulator in the intraocular unit, and has been optimized for reduced power consumption. The Class-E power amplifier can accept feedback information from the secondary side and increase the power delivered by raising its supply voltage. This ensures power supply regulation even as the distance between the coils vary within a range.

Reverse telemetry data detection and clock recovery is achieved via a differential envelope detector for increased noise immunity in the presence of a slow varying power carrier. Data communication is achieved by transmitting short pulses that are detected on the primary side. These detected pulses, when passed through a toggle latch, generate a PWM waveform that can be converted to NRZ data. Thus a novel variation of PWM encoding of data has been conceived and implemented. Simulation results, using AMI-1.6 process, showing the reverse telemetry data detection with a data rate of 5Kbps have been presented. The protocol to be followed in data communication has also been proposed.

The scope for future work includes a closed-loop self-driving Class-E driver that achieves optimized power transfer. Presently, the Class-E power amplifier is driven by an external voltage pulse source. If there are variations or inaccuracies in the component values, the fixed frequency and duty cycle of the external pulse will not enable the amplifier to function efficiently. Apart from the closed-loop Class-E implementation, there is also focus on the development of an efficient DC/DC converter that cuts down losses in the power control unit.

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