ABSTRACT

GADFORT, PETER. Low Power Interconnect Circuits using Silicon Carriers. (Under the direction of Professor P. D. Franzon).

Due to the ever-increasing complexity of the tasks that modern electronic devices are expected to carry out, many devices incorporate multiple chips linked via input/output pins and transmission lines on a single board in multi-chip modules. The interconnects between these chips are a large source of power drain due to the parasitic capacitance loading of the input/output pads on the chip and the transmission lines.

By moving multiple chips onto the same substrate to form a "virtual" chip, the I/O pins and transmission lines used to connect the chips can be replaced with a silicon carrier and micro-bumps. By creating these "virtual" chips, incompatible technologies such as GaAs and silicon substrate can be merged into a single package. Using silicon carriers also allows for the use of fine-pitch interconnects down to 2 $\mu$m - built into the silicon carrier - which is a large improvement over current organic or ceramic packaging technologies.

This work investigates a current mode circuit proposed by Zhang [1] to achieve a significant power advantage over current signaling techniques and packaging technologies. This will be achieved by utilizing silicon carrier technology for the interconnects between integrated circuits. The interconnects can span the carrier from a few millimeters up to several centimeters depending on the interconnect structure. By trading the bandwidth of the silicon carrier for length of the interconnect, various lengths can be chosen for the desired data throughput. Also, by trading noise margin for reduced power in the I/O circuits a significant power reduction in the circuits can be achieved.

This work will show that a power reduction of 75%, for the power metric of power per gigabit per second, is possible over current organic packaging technologies and a standard driver, by using the improved driver and the silicon carrier interconnects. These circuits were designed in a predictive 45 nm process and the achieved bit error rates were on the order of $10^{-15}$ errors/bit while operating at 4 Gbps.
Low Power Interconnect Circuits using Silicon Carriers

by

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DEDICATION

Dedicated to my friends and family without whose support and guidance this thesis would not have been possible.
BIOGRAPHY

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Chapter 1

Introduction

1.1 Motivation

As electronic systems increase in complexity, the ability to integrate all the functionality of the system onto a single chip may not be possible. Manufacturing process integration may not permit a solution on a single chip; however, heterogeneous semiconductor technologies might be required to overcome this challenge as noted by Knickerbocker [8] and Tummala and Madisetti [9]. In these cases, System on Package offers many benefits to overcome these challenges and gain additional benefits. System on Package allows different technologies to be included in a single package to form the whole system, as it would on a System on Chip implementation, but without many of the process integration concerns.

Current System on Package and other multichip module technologies are trending towards obsolescence as the data throughput and power limitations increase as reported by the International Technology Roadmap for Semiconductors [10]. Therefore, new System on Package technologies are required to help alleviate some of these concerns related to throughput and power.

Silicon based packages, such as silicon carriers, have been proposed to replace current multichip modules by creating “virtual” silicon chips with multiple chips
bonded to the carriers as reported by Knickerbocker [8]. Two cross sections of this “virtual” chip concept are shown in figure 1.1, where the silicon carrier is used to provide interconnects between the chips and to connections external to the package. These systems have the added advantage that active devices can be included on the carrier, which is not possible with printed circuit boards, to allow buffers to be added to help with the longer interconnects. Silicon carriers also address the issue of wiring density while having a much smaller wiring pitch than with current organic packaging technologies. The same is true for the I/O site density, with controlled collapse chip connection (C4) bonds offering a factor of 10 improvement in density over wirebonding technologies, because the C4 micro-bumps allow for the whole surface area of the chip to be used for I/O sited, whereas with wirebonding only the perimeter of the chip can be used.

This work will focus on utilizing silicon carrier interconnects and on-chip signaling techniques to gain a power advantage over traditional FR-4 interconnects for off-chip signaling. On-chip signaling for global interconnects is similar to silicon carrier interconnects and have equivalent issues with power consumption, throughput, noise, and overall length of the interconnects. Therefore on-chip signaling techniques can
be applied for off-chip communications purposes.

1.2 Goal of This Work

This work will demonstrate the use of silicon carrier interconnects as efficient chip-to-chip structures for low power high speed communications. By characterizing the interconnects in Ansoft’s HFSS, the S-parameters were extracted and used in HSPICE simulations to fully describe the silicon carrier interconnects and any frequency dependent loss that is associated with them. Two drivers will be designed, one driver to serve as a base and one to show the improved power advantage of the improved driver for the silicon carrier interconnects.

1.3 Thesis Overview

In chapter 2, topics discussed include the various challenges facing System on Package systems related chip-to-chip communications caused by input and output pads on the chips, the usable wiring pitches, and required signaling speeds. Techniques related to microstrip structures, such as coplanar waveguides and differential signaling pairs, are reviewed to alleviate some of these the noise issues. Also, various driver circuits will be discussed for lowering the power requirements of these circuits.

Chapter 3 discusses silicon carriers for System on Package applications. The benefits of silicon carriers include the increase in wiring density and use of C4 micro-bumps to gain an advantage in I/O density over current packaging technologies. Other benefits - and some drawbacks - of using silicon carriers are also discussed. The discussion concludes with an overview of two proposed interconnect structures, the coplanar waveguide and differential signaling pair, and how they were simulated in Ansoft’s HFSS [11] to extract models for use in HSPICE simulations with the drivers from chapter 4 and the interconnects performed in the silicon carriers for chip-to-chip communications.
In chapter 4, two differential current mode drivers are developed and discussed. The first driver serves as a reference to compare the power and speed performance metrics of the two drivers. This reference driver is designed to operate over a differential pair for an organic substrate (FR-4). The second driver is designed to operate on the differential pair discussed in chapter 3 for the silicon carrier. This driver will emphasize the higher frequency content of the transmitted signal due to the fact that the silicon carrier interconnects are lossy compared to the FR-4 interconnect. Both drivers were designed in a predictive 45 nm process [12] and were operating at 4 Gbps.

Chapter 5 concludes this thesis and will propose possible future avenues of work to be explored.
Chapter 2

System on Package

2.1 Introduction

System on Package (SOP), also called System in Package (SIP), is a package in which multiple integrated circuits are included to form an entire system within the package. Packaging has always been an important part of electronics; however, in the past its primary function was structural. However, with increasing demands on systems the packaging is starting to play a more important role in providing required functionality and performance as reported by Tummala [9]. It is these increased functionality and performance demands that have lead to growing interest in SOP as a method to achieve these goals.

This chapter will discuss some of the advantages of System on Package designs, the challenges of chip-to-chip communications, and various signaling structures and drivers.

2.2 Advantages of System on Package

System on Package has many advantages over System on Chip (SOC) configurations, where the system is implemented completely on a single integrated circuit [9].
An illustration of each of these systems is shown in figure 2.1 with the System on Chip in 2.1(a) and the System on Package in 2.1(b). The SOP allows for increased noise isolation as it provides a simple solution to isolate digital/analog/RF circuits from each other by having them implemented on separate chips, whereas in SOC the isolation would only be the substrate between the devices. Along with noise isolation, the SOP also improves system integration by building the various integrated circuits in the appropriate process. This means that, while an RF circuit would be built onto a GaAs substrate and the digital and analog circuits would be manufactured onto silicon substrates, the entire system could be formed inside a package containing all the integrated circuits. Another important advantage of SOP over SOC is not related to the electrical performance of the systems, but it relates to how quickly the systems can be designed and manufactured. The time-to-market for a SOP is much less than that of a SOC. The reduction is in part due to the use of known good dies, that is dies that can be tested before being implemented in the system. This kind of testing would not be possible until the end of the processing of the entire system for the SOC, which could reduce the overall yield.

System on Package can also be used to design 3D packages as reported by Kim [3]. Here the integrated circuits are stacked on top of each other to reduce the system footprint as shown in figure 2.2. In this figure, the system on the left is a 3D stacked circuit where the various chips are connected directly together through tall vias, and on the right the system is a 3D package with several levels of chips and packages in between them to create the 3D package. The advantages of using 3D packages over 3D circuit are similar to those of SOP versus SOC. Again, the use of different integrated
circuit processes allow for analog/digital/RF circuits to be bonded together to form the 3D packages, which is not possible with 3D circuits. However, the 3D circuits will have a much smaller component size, down to the nanoscale, whereas the 3D packages will be on the order of microns instead.

2.3 Challenges of Chip-to-Chip Interconnects

The current challenges with chip-to-chip communication center around the desired signaling rates, the widths of the data buses, and power related to the interconnects and drivers of the interconnects. The challenge for the designers is to leverage the design trade-offs shown in figure 2.3 to achieve the best interconnect for the intended application. The goals of high speed interconnects for chip-to-chip communication has several issues that will be discussed in the following sections about the I/O pads, wiring pitches, and signaling speed.

Input/Output Pads

The input and output pads of the integrated circuits perform some important tasks including providing the electrostatic discharge (ESD) protection for the input gates and rebuffering of the input or output signals to be driven to another chip. However, these pads have a very large capacitance associated with them, which limits the achievable signaling speeds and has a negative effect on the power of the system.
Another issue with the pads are their relative location on the dies. The pads can only be located on the periphery of the chips, which limits the number of I/O sites for the integrated circuit. This means a low density of I/O on the chip, since only the periphery of the chip is usable, which translates to only about 4K I/O pins/cm² as reported by Knickerbocker [8].

Some of these issues can be alleviated by utilizing micro-bumps to connect the chips to the next level of interconnects. By using micro-bumps and flip-chip bonding the chip to the next level of interconnects, the entire surface of the chip can be utilized for I/O placement, which yields I/O densities of 40K I/O sites/cm² as reported by Knickerbocker [8]. This has the added advantage of reducing the series inductance of the connect levels when comparing the flip-chip connection to a wire-bonded connection as mentioned by Hall, Hall, and McCall [13]. This can be seen in figure 2.4, where the chip on the left is wire bonded to the package and has a larger induction loop, and the micro-bump flip-chip bonded chip on the right has a much smaller induction loop.
Wiring Pitch

The wiring pitch of the packaging can also be a limiting factor in the overall communication data rate and size of the interconnect buses. The wiring pitch makes a design trade-off of signaling rates versus number of interconnects needed. This means that if a system needs a throughput of 64 Gb/s, the system could be comprised of 64 1 Gb/s wires or 16 4 Gb/s wires. Each of these designs would have the desired throughput, but the one with 64 wires would consume a much larger area than the one with only 16 wires. Therefore a small wiring pitch will be desirable for a System on Package applications as there will be more interconnects to place due to the use of micro-bumps for the I/O sites instead of wire-bonding.

However, the smallest wiring pitch may not be the most desirable, as it could cause excess crosstalk noise on the neighboring channels. Methods of mitigating this type of noise will be discussed in section 2.4.1.

Signaling Speeds

As mentioned in the previous section, the signaling speed is determined by the needed throughput and the available number of wires for the signaling. Furthermore, as the core frequency increases, the bus speed will have to scale accordingly in order to keep up with the data demands of the systems as reported by Hall, Hall, and McCall [13].

The signaling speed is determined by the driver design and the interconnect characteristics. For very lossy interconnects, such as those on-chip, the power of the driver
would increase substantially in order to operate at high signaling rates for that driver. For less lossy interconnect, such as those in FR-4, the drivers would consume much less power while operating at the same signaling rate.

The signaling rate also effects the area of the driver itself. If the area of the driver is much larger then that of the I/O site, then the effective I/O density would be decreased for the system. All of these trade-offs are shown in figure 2.3.

2.4 Off-chip Signaling

Off-chip signaling is comprised of two parts: the structures with which the signals are carried from one chip to another and the drivers that produce the signals that travel down the interconnects.

2.4.1 Structures

There are many different types of structures that can make up the interconnects between two integrated circuits. In this section three basic structures will be discussed: a single ended coplanar waveguide, a differential signaling pair, and a twisted differential signaling pair.

Single Ended

The single ended interconnect only has one wire (or trace) to carry the signal to the end of the interconnect. One such structure is the coplanar waveguide, which was developed in 1969 by C. P. Wen [14]. The coplanar waveguide has become very popular with RF designers for use at frequencies exceeding 10 GHz as mentioned by Steer [15] because of its good suppression of radiation. Yet this structure does have some drawbacks including the increased area needed to place the two reference planes next to the signal trace. The coplanar waveguide structure is shown in figure 2.5 with the ground-signal-ground configuration.
Since the coplanar waveguide is a single ended structure, it does not offer the same level of noise immunity from surrounding traces as a differential pair would.

IBM has proposed using coplanar waveguides for its silicon carriers as a possible interconnect for chip-to-chip communication as reported by Knickerbocker [8] [2]. These waveguides will be discussed in section 3.5.1.

**Differential Pair**

The differential signaling pair has two signaling wires (or traces) which carry equal but opposite information to the end of the interconnect where the data is reconstructed using the difference of the two interconnects. The differential pair is very popular with analog designers because of its relatively high suppression of common mode noise, which results in a much cleaner signal as reported by Zhang, George, and Rabaey [5]. For this same reason, differential traces and drivers have become popular as well with high speed digital designers where the greater noise immunity allows an added speed advantage. The differential signaling traces are shown in figure 2.6.

The structure has one obvious drawback, which is the need for two signal traces which need to be routed together to ensure the proper noise immunity. However, the differential pair still suffers from some crosstalk effects, but these can be reduced by either limiting the lengths parallel interconnects or using a twisted differential pair as will be discussed in the next section.

In addition to coplanar waveguides, IBM has also proposed using grounded dif-
Differential pairs for its silicon carriers as a possible interconnect for chip-to-chip communication as reported by Knickerbocker [8] [16]. This type of signal trace will be discussed in section 3.5.2.

**Twisted Differential Pairs**

For the highest level of noise immunity, a twisted differential signaling pair would be needed. In this structure, multiple metal layers are used for routing to mimic the twisted part of the differential line. By twisting the differential lines, crosstalk can be mitigated or canceled by allowing alternating sections to be exposed to the same noise events as reported by Zhang [1] and by Kam [17]. This reduction in crosstalk has been shown by Kam [17], where the far end crosstalk was reduced by a factor of 7.75 over a coupled microstrip line. It has also been shown that the wiring delay of the twisted differential pair is much less than that of the differential pair by Hatirmaz [4], an improvement of about a factor of 2 to 4 reduction for a 2 mm segment. In figure 2.7, the proposed twisted differential signaling pair is shown with the relative propagating edges shown.

The reduction in crosstalk and increased propagation velocity of the signals would make the twisted differential pair highly suitable for high speed signaling in SOP applications, but in some cases when additional metal layers are not available, this would not be possible.
2.4.2 Circuits

The second part of off-chip signaling is the driver designs to accomplish the desired throughput, delay, and power. The drivers are designed to cope with the various parasitic effects of the interconnects they are transmitting signals across. In the following sections, circuits, which have been demonstrated for on-chip signaling, will be discussed as they could also be useful for SOP applications, especially those of the silicon carriers which will be discussed in chapter 3.

Low-swing Signaling Techniques

A simple and effective way to reduce power on the communications interconnects is to reduce the signal swing. The equation for dynamic power as a function of the voltage swing on the interconnect expressed in equation 2.1 from Rabaey [18].

\[
P_{\text{dyn}} = \alpha f C_L V_{\text{swing}}^2
\]  

(2.1)

Where \( \alpha \) is the switching activity on the interconnect; \( f \) is the clock frequency; \( C_L \) is the capacitive load including the buffer and interconnect capacitance; and \( V_{\text{swing}} \) is the
voltage swing on the interconnect. From this equation, it is evident that a reduction in the voltage swing produces a squared reduction in the dynamic power. As shown in figure 2.8, the driver launches a reduced swing signal down the interconnect and the signal is amplified back to a full swing signal at the receiver. However, the signal swing cannot continue to be reduced because the swing is limited by noise sources like receiver offset and sensitivity, cross talk from other data lines, reflections from previous bits due to poor termination, and coupled supply noise as mentioned by Poulton [19] and therefore power efficient circuits are also needed to reduce power.

Several low swing drivers have been proposed by Zhang, George, and Rabaey [5] and [20]. The simplest of these drivers is shown in figure 2.9. In this circuit, the signal is buffered to a reduced $VDD_L$ in order to produce the smaller signal swing, which
is launched onto the interconnect. At the receiver, the signal is latched in the cross-coupled inverters and buffered back to a full swing signal. This circuit demonstrated a reduction in energy by a factor of approximately 3 as reported by Rabaey [5]. The circuit is very simple to design, but it requires an additional voltage source to supply $V_{DD_L}$.

When utilizing low swing signaling techniques, an amplifying circuit will be needed at the receiver to generate the full swing output signal, and this will have some additional power associated with the amplifying circuit. However, the power savings from the reduced swing on the interconnect will far outweigh the power required for the amplifier as noted by Zhang [1]. Additionally, the low swing signals will have longer delays than their full swing counter parts, as demonstrated by Rabaey [5] and [20].

Since the signals have a reduced swing, they will be more prone to crosstalk issues. Therefore greater care is needed to isolate the signal traces from noise sources. To alleviate some of this problem, differential signaling can be used and will be discussed in the next section.

**Low-swing Differential Signaling Techniques**

In order to improve the noise immunity of the low swing interconnects, differential signaling can be utilized. One such circuit was proposed by Rabaey [5], where it was demonstrated to achieve a energy reduction by a factor of approximately 4 when compared to a simple inverter driver. This was achieved using a further reduced signal swing, more than that of the single ended low swing interconnect. This reduction was acceptable because of the common mode rejection of the differential interconnect and receiving latch. This interconnect is shown in figure 2.10. In this circuit, the reduced swing signals are generated at the two buffers, which uses NMOS transistors for both pull-up and pull-down. By doing this, the swing will be further reduced from $REF$ to $REF - V_t$. The signals then travel down the differential interconnects and are amplified and latched at the receiver. The main drawbacks of using this circuit will
be the need for additional reference voltages to supply $REF$ as well as low $V_t$ devices for use in the driver circuits, as well as doubling the number of wires needed for the interconnects.

### Low-swing Twisted Differential Signaling Techniques

As mentioned in section 2.4.1, the twisted differential signaling pairs will offer greater immunity to noise and crosstalk of the three structures discussed. One signaling technique was proposed by Hatirnaz [6] for twisted differential pairs. As shown in figure 2.11(a), the driver consists of a self level converter (SLC) driver which produces a swing from $GND + V_{tp}$ to $V_{DD} - V_{tn}$ and results in a desired reduced swing of the driver. The transistors $M_{P3}$ and $M_{N3}$ are diode connected and sized to control the output swing within the desired range. The same is true for the complementary path consisting of $M_{P3}$, $M_{N3}$, $M_{P4}$, and $M_{N4}$. In figure 2.11(b), the receiver consists of a modified asymmetric source driver level converter (MASDLC), which amplifies the difference between the signals $V_{DIFF1}$ and $V_{DIFF2}$. The interconnects are laid out as tightly-coupled twisted differential pairs in order to provide the highest noise immunity and decrease the effects of inductance.

This circuit showed large time delay improvement over voltage mode signaling with
Figure 2.11: Twisted differential pair driver and receiver circuits. After Narasimhan et al. [6], copyright IEEE 2005.
optimal repeater insertion for interconnects shorter than 1.2 cm as shown by Hatirnaz [6]. Also, the power of the MASDLC receiver demonstrated a power reduction of a factor of almost 3.

The main drawbacks of using such a configuration include the need for multiple metal layers to create the twisted differential lines and the design overhead of driver and receiver.

Multilevel Current Mode Techniques

Multilevel signaling is another way to help reduce power and the number of interconnects needed. One such system was proposed by Joshi and Sharma [7]. In this system, two bits are encoded into four current levels which are then sent down the interconnect and decoded using a receiver circuit and a simple decoder circuit. By encoding two bits into a single signal, the number of required interconnects is reduced by half, which reduces the area allocated to interconnects. This system can be seen in figure 2.12. In figure 2.12(a), the driver of the system is shown. This driver will
produce currents of 0, $I$, 2$I$, and 3$I$ on $I_{int}$. The current level is determined by the state of Bit0 and Bit1. The driver circuit is relatively simple to design, and most of the effort will be focused on generating the appropriate $I_{gen}$, since this will determine the static power of the circuit. The receiver is shown in 2.12(b), which requires some additional effort for the design to get the correct $I_{ref}$, in order ensure the proper operation of this circuit for detecting the four current levels. Additionally, the receiver can be designed to match the impedance of the interconnect as shown in equation 2.2, which will help with the signal quality by reducing ringing on the interconnect.

$$R_{in} = \frac{1 - \frac{g_{n2}}{g_{n1}}}{\frac{g_{m2}}{g_{m1}}}$$

(2.2)

where $g_x$ is the transconductance of the transistor $x$ in figure 2.12(b).

### 2.5 Summary

In this chapter, System on Packages were introduced and several of the benefits were discussed as well as the enabling structures and circuits to perform chip-to-chip signaling.

The signaling performance metrics of delay, power, throughput, noise, and area are some of challenges System on Package applications are facing with regard to the interconnects and supporting circuits. Designers must make a trade-off among these metrics for the desired application in order to produce the most effective system.

The structures that will be further discussed in chapter 3 are the coplanar waveguide and differential signaling pair for the specific application of silicon carriers. The twisted differential pair was also discussed in this chapter and showed great noise immunity, but it will require multiple metal layers to implement in MCMs.

Several low swing drivers discussed in this chapter are all showing large reduction in power over a full swing interconnect, but the low swing also implies the signals are more prone to crosstalk and other noise issues, which limits the swing amplitude. The energy metrics for these circuits have been tabulated in table 2.1. From this table,
Table 2.1: Summary of previous signaling techniques.

<table>
<thead>
<tr>
<th>Signaling techniques</th>
<th>Energy per bit (pJ/bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-swing</td>
<td>4.4</td>
</tr>
<tr>
<td>Low-swing differential</td>
<td>3.0</td>
</tr>
<tr>
<td>Low-swing twisted differential</td>
<td>3.4</td>
</tr>
</tbody>
</table>

The differential signaling techniques are showing the best performance for single level signaling, and the multilevel current mode signaling techniques has the best energy per bit. This shows that multilevel signaling would be desirable, but it does not offer the same noise margins as single level signaling can, therefore single level differential signaling will be chosen for the drivers in chapter 4.
Chapter 3

Silicon Carrier Interconnects

3.1 Introduction

Silicon carriers are a technology proposed as a possible System on Package implementation as mentioned by the International Technology Roadmap for Semiconductors [10] as a substitute for organic laminate packaging, which is reaching its usable limits. The silicon carrier consists of a blank silicon wafer where the back end of line processing (BEOL) has been performed to implement the desired structures, such as metal interconnects. Although the silicon carrier wafer is blank, active devices could be added to the substrate to add buffers or other circuits. The chips are then flip-chip bonded onto the silicon carrier using C4 micro-bumps, which will be discussed in section 3.4, to form the System on Package. This configuration can be seen in figure 3.1, where two chips have been placed on the silicon carrier, and the carrier provides the interconnect structures between the two chips with two metal layers. In the figure, the two chips are shown in green, the silicon carrier in red, and the C4 micro-bumps and copper interconnects in gray. The figure also shows a through silicon via for connections outside the module. The C4 micro-bumps are 25 µm in diameter and are spaced 25 µm apart as shown in the figure, also the micro-bumps are 8 µm tall, which they are reduced to after the dies are bonded to the carrier.
Using silicon carriers allows for smaller System on Package footprints and can be used for alternate purposes, such as thermal relief for chips or holders for opto-electronic communication transceivers. Thermal relief solutions include building fluidic paths in the carriers and pumping fluids through them to provide the needed cooling for the chips on the silicon carriers as reported by Aibin [21]. The opto-electronic transceivers are placed into cavities, which are etched during processing, in the carrier and then connected to optical waveguides and integrated circuits to control the system as demonstrated by Knickerbocker [2] [8] [16]. The carriers also allow incompatible technologies to be merged into a single package, such as GaAs substrates or any other compound substrate and bonded to the carrier for smaller system footprints.

This chapter will cover some of the benefits and drawbacks of using silicon carriers for chip-to-chip interconnects and the characterization of two types of interconnects.

### 3.2 Benefits of Silicon Carrier Interconnects

The benefits of using silicon carriers for chip-to-chip interconnects include the achievable wiring pitch, I/O bump density, and full custom design of interconnects.

Possibly one of the biggest benefits of using silicon carriers for chip-to-chip interconnects would be the use of current BEOL technologies, to build up to the interconnects and flip-chip bond the chips to the carrier technologies that are currently
widely available at foundries can be utilized. This implies that foundries would not need to retool or upgrade to begin processing silicon carrier wafers but only modify their process flow. The silicon carrier wafer would only have to go through the metalization of the wafer processing at the foundry to have the interconnects built onto the wafer.

The wiring pitch of the silicon carrier is $2 \, \mu m$, which is a great improvement over ceramic packaging which has a wiring pitch of about $150 \, \mu m$ as reported by Knickerbocker [2] [8]. However, while this small wiring pitch might not currently be realistic as the micro-bumps cannot be that dense, but as the micro-bump technology improves to allow smaller and tighter micro-bumps, this wiring pitch will become more relevant.

The micro-bumps provide the I/O sites from which the chip will be both connected to and communicating with the silicon carrier. The density of the micro-bumps can be as high as $40K \, (I/O)/cm^2$ with a pitch of $50 \, \mu m$, which is quite large compared to organic or ceramic packaging that only reaches about $4K \, (I/O)/cm^2$ as reported by Knickerbocker [8] [2]. The increase in density is largely due to utilization of the entire chip surface, as opposed to only the outer edge of the chip when the interconnects are connected using wire bonds.

Finally, the silicon carrier allows for a full custom design of the interconnects for chip-to-chip communication. Based on the application and other factors, designers can choose to use differential signaling pairs, coplanar waveguides, or any other signaling structure which they desire. Since the silicon carriers provide such a dense I/O, utilizing differential signaling schemes would not consume the same amount of area and crucial pads as it would with organic packaging.

An additional benefit includes the thermal compatibility of the silicon carrier to silicon chips. The expansion of the silicon carrier will be similar to the thermal expansion of the silicon based integrated circuits soldered onto it, because the expansion coefficient of the silicon carrier is the same that of the silicon integrated circuits as noted by Knickerbocker [8]. This allows for less stress to build up in the interface
between the integrated circuits and the carrier, providing a much higher reliability for the package.

3.3 Drawbacks of Silicon Carrier Interconnects

The drawbacks of using silicon carriers interconnects would be the cost associated with the additional foundry processing required to implement the carrier and to attach the chip to the carrier itself. These costs would include the BEOL processing and additional design time required for the silicon carrier.

As will be discussed in section 3.5, the interconnects also have some limitations with respect to the length and cut-off frequency. The length of the interconnect is inversely related to the cut-off frequency of the interconnect; therefore for very short interconnects, high data rates would be possible, whereas for long interconnects this would not be possible.

3.4 C4 Micro-bumps

The silicon carriers and chips will be bonded together using a flip-chip bonding technique with controlled collapse chip connections (C4) as reported by Knickerbocker [8] [22]. As mentioned in section 3.2, these connections allow the chips to be structurally attached to the silicon carrier while also providing the electrical connection from the chip to the silicon carrier interconnect. The micro-bumps are built onto the chip, which will be soldered onto the carrier using the micro-bumps, using electroplating to deposit the solder onto the chip. Then the chip and carrier are aligned and fused together using the micro-bumps as structural support to hold the two components together. This final structure can be seen in figure 3.1, where two chips, C4 micro-bump, metal interconnects, and silicon carrier are shown.
3.5 Interconnects

IBM has investigated several interconnect structures for silicon carriers including coplanar waveguides and differential signaling pairs as reported by Knickerbocker [8], which will be discussed and simulated in this section. These interconnects will provide the chip-to-chip communication for the System on Package applications they will be applied towards. The simulations will be performed using Ansof's High Frequency Structure Simulator (HFSS) [11], which will provide the S-parameters needed to implement the interconnects in HSPICE [23] simulations for the driver circuits in chapter 4.

3.5.1 Coplanar Waveguide

The coplanar waveguide transmission line consists of a single signal trace and two reference traces as shown in figure 3.2 as reported by Knickerbocker [8]. In the figure, the silicon substrate is shown at the bottom of the structure with the silicon dioxide (SiO₂) on top in which the metal traces are placed. On top of that is a thin silicon nitride layer for wafer passivation. The metal traces shown are the two reference traces in green, and the signaling trace in red and are implemented using copper for the metal as noted by Knickerbocker [2] [8].

The coplanar waveguide is ideal for dense interconnects because it terminates its
field lines on the reference places, allowing for a more dense placement of coplanar waveguides or any other structure which would be effected by stray fields. This can be seen in figure 3.3, where the blue area indicates no electric fields and red area indicates the fields with the largest magnitude. However, because the field lines extend farther up and down, this makes the coplanar waveguide more difficult to design for multi-level metal layers without providing additional shielding.

This coplanar waveguide was simulated in HFSS with the dimensions shown in figure 3.2. This results in an interconnect with a characteristic impedance, $Z_0$, of almost 49 $\Omega$ measured at 10 GHz.

IBM recommends using the coplanar waveguide for low to mid-range data rates as noted by Knickerbocker [8] (speeds less than 10 Gbps). From HSPICE simulations using the S-parameters extracted from HFSS, the coplanar waveguides are unsuited for high speed signaling as the frequency response of the waveguides indicate a very low cut-off frequency, which can be seen in figure 3.4. In this figure, three different lengths of coplanar waveguides were analyzed in the frequency domain and show the low cut-off frequency. Therefore, for long lines from chip-to-chip, these would not be able to keep up with the required signaling rates. The reason for the poor performance is due to dispersion effects, which will be discussed in the next section. The figure
Figure 3.4: Coplanar waveguide frequency response for lengths of 5 mm (blue), 10 mm (red), and 50 mm (green).
shows that, for interconnects that are 5 mm long, the 3 dB frequency is 2.38 GHz; for lengths of 10 mm, the cut-off frequency is 3.21 GHz; and for lengths of 50 mm, the cut-off frequency is 842 MHz.

**Dispersion Effects**

The dispersion effects coplanar waveguides are subjected to are caused by the fact that half of the field lines are in air and the other half in the SiO\(_2\). To investigate this (and potentially alleviate the problem), the surrounding SiO\(_2\) was increased in thickness to allow more of the field lines to be contained within the dielectric itself and not in the air. By increasing the distance from the metal traces to the silicon nitride layer from 0.4 \(\mu\)m to 5 \(\mu\)m, the cut-off frequency increases from the original 842 MHz to 4.683 GHz; however, by changing this distance, the characteristic impedance is changing as well from almost 49 \(\Omega\) to 45 \(\Omega\).

The frequency response for three different distances from the metal traces to the nitride layer for a 1 cm coplanar waveguide can be seen in figure 3.5, where it is evident that, as the distance increases, the frequency response improves. The figure shows that the interconnects cut-off frequency for the thickness of the SiO\(_2\) between the copper and nitride layer of 0.4 \(\mu\)m is 842 MHz, as the thickness increases to 1 \(\mu\)m the cut-off frequency increases to 1.30 GHz, and as the thickness increases to 5 \(\mu\)m the frequency increases up to 4.68 GHz.

### 3.5.2 Differential Signaling Pair

The differential signaling pair consists of two signaling traces and a ground plane as shown in figure 3.6. Just as with the coplanar waveguide in section 3.5.1, the silicon substrate is at the bottom with the silicon dioxide, SiO\(_2\), on top of the substrate and finally a thin passivation layer of silicon nitride. The metal traces are the two signaling traces in red and the green plane is the reference plane, all of this is implemented in copper for the metal as noted by Knickerbocker [8] [16].
Figure 3.5: Coplanar waveguide frequency response with increasing SiO\(_2\) thickness from metal traces to nitride layer of 0.4 \(\mu\)m (blue), 1 \(\mu\)m (green), and 5 \(\mu\)m (red).

Figure 3.6: Differential pair cross section.
This differential signaling pair was simulated in HFSS with the dimensions shown in figure 3.6. This results in an interconnect with a differential characteristic impedance, $Z_{\text{diff}}$, of almost 95 Ω measured at 10 GHz and a common mode impedance, $Z_c$, of almost 27 Ω.

IBM recommends using the differential micro strips for high data rates above 10 Gbps as reported by Knickerbocker [8]. From HSPICE simulations using the S-parameters extracted from HFSS, the differential signaling pairs have a higher cut-off frequency than the coplanar waveguides. This makes the differential pairs better suited for high speed signaling for the long interconnects required for chip-to-chip communication. But, again, as the length of the interconnects increase the cut-off frequency decreases, just as with the coplanar waveguides, though not nearly as dramatic as shown in figure 3.7. The differential signaling pair does not suffer from the same dispersion effects as the coplanar waveguide because the fields are grounded to the reference plane, which makes them more suited for the high speed signaling. The figure shows that, for interconnects that are 5 mm long, the 3 dB frequency is 40.84 GHz; for lengths of 10 mm, the cut-off frequency drops to 16.24 GHz; and for lengths of 50 mm, the cut-off frequency drops to 1.42 GHz. From the figure it is evident that for lengths less than 5 cm, high speed signaling would be easily feasible, as the cut-off frequency is high enough to provide the needed bandwidth; yet for lengths greater than 5 cm this would become increasingly more difficult as the cut-off frequency would fall below 1 GHz.

The differential pair is also better suited for multi-layer interconnects, as the field lines do no extend nearly as far as the coplanar waveguides and the field terminates on the reference plane as shown in figure 3.8, where the blue area indicates no electric fields and red area indicates the fields with the largest magnitude.

Using HSPICE simulations and the HFSS S-parameters, the differential pair was compared to the results by IBM [8] and demonstrated that the simulations differ by less than 10% from IBM’s results. These results have been compiled in table 3.1, where the time delay was simulated in a transient HSPICE simulation and measured
Figure 3.7: Differential pair transmission line frequency response for lengths of 5 mm (blue), 10mm (red), and 50 mm (green).

Figure 3.8: Differential pair electric field distribution.
Table 3.1: HFSS/HSPICE vs IBM for 5 mm differential pair interconnect.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>HFSS/SPICE result</th>
<th>IBM result [8]</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_d$</td>
<td>34.79 ps</td>
<td>37.2 ps</td>
<td>-6.48%</td>
</tr>
<tr>
<td>$Z_{diff}$ at 10 GHz</td>
<td>95Ω</td>
<td>105Ω</td>
<td>-9.52%</td>
</tr>
</tbody>
</table>

at the 50% voltage of a rising edge.

3.6 Summary

In this chapter, the benefits and drawbacks of using silicon carriers for SOP applications were discussed, as well as two different signaling structures were investigated: a coplanar waveguide and a differential signaling pair.

The primary benefits of the silicon carriers come from the I/O densities that can be achieved using current BEOL technologies and C4 micro-bumps. Additionally, the silicon carriers provide benefits outside the electrical performance of the interconnects with thermal reliefs in the form of fluidic channels to help cool the chips.

The interconnects structures were simulated in HFSS as if they were implemented on a silicon carrier as described by IBM. The performance of the two interconnects varied greatly.

The coplanar waveguide was shown to be best suited for low data rates, due to the dispersion of the field lines into air. Therefore, if the coplanar waveguide was redesigned to be embedded completely in the SiO$_2$, the performance of the transmission line will improve allowing for slightly higher data rates over longer lines.

The differential signaling pair was shown to be most efficient for lengths less than 5 cm as the loss in lengths greater than this would result in cut-off frequencies below 1 GHz making it increasingly more difficult to accommodate high data rates; however, for short interconnects, very high speed data rates would possible as the cut-off frequency is over 40 GHz for a 5 mm long signaling pair.

Because of the performance advantages, the differential signaling pair will be used for the improved driver in chapter 4 as it allows for higher data rates for the same
lengths of interconnects when compared to the coplanar waveguides.
Chapter 4

Driver Circuits

4.1 Introduction

In this chapter, the design of two drivers will be discussed as well as the signaling techniques which the drivers will use. A brief discussion of the estimation of the performance measures will also be provided.

The drivers discussed in this chapter will be implemented using MOSFET models from the FreePDK45 [12] developed by North Carolina State University. This is a predictive process design kit used to model the transistors for both drivers. The kit is modeling a generic 45 nm process based on published papers, predictive technology models, and rule scaling.

4.2 Current Mode Signaling

The signaling scheme that will be utilized for the drivers in this chapter will be current mode signaling. This type of signaling launches a current down an interconnect instead of a voltage, allowing for a simpler design process by only requiring knowledge of the magnitude of the current required to produce the desired voltage swing at the receiver. Figure 4.1 shows the path that the current will take in a single-
ended interconnect. The voltage swing is produced at the termination, $R_{term}$, on the receiver side of the interconnect. The interconnect is represented by $R_{int}$.

### 4.2.1 Differential Signaling

For additional immunity against noise events, differential signaling can be utilized as was discussed in section 2.4.1. Differential signaling uses two interconnects, which are routed in a similar fashion, to allow noise events like glitches and other crosstalk events from unrelated interconnects to be canceled out. Figure 4.2(a) shows an example of the driver and interconnect, where the interconnect is set up as a differential pair. This could also represent the noisy received signals of a single ended transmission. In figure 4.2(b) the received signals are shown with noise, and the differential signal at the bottom as computed by $V_P - V_N = V_{diff}$. The received signals show a significant amount of noise that is common to both signals, therefore the received differential signal is still clean, whereas the single-ended received signal is still very noisy.
Figure 4.2: Differential current mode signaling.
4.3 Bit Error Rate Estimation

In order to estimate the bit error rate of a system, the eye diagram at the receiver will be utilized. The noise on the interconnect is then modeled as Gaussian noise, and from this the bit error rate can be computed. As seen in figure 4.3, the eye diagram has been translated into two Gaussian curves, one for the high logical level and one for the low logical level. The area in the shaded regions of the Gaussians indicate the bit error rate for that logical level. Using equation 4.1, the Q-factor for the logical level can be estimated, and the bit error rate is estimated by subsequently using the complementary error function. In the equation $\mu_x$ is the average voltage for the logic level being estimated, $NM_x$ is the noise margin for the logic level as determined by the receiving circuit, and $\sigma_x$ is the standard deviation of the voltage level, that would be the one sigma noise.

$$Q_x = \frac{\mu_x - NM_x}{\sigma_x}$$  \hspace{1cm} (4.1)

For the two logical levels, equation 4.2 is used to combine the Q-factors for the high and low logical levels to estimate the overall bit error rate for the system. In
this equation, $P_1$ and $P_0$ are the probabilities that a logical one or zero were sent, respectively. Assuming $P_1 = P_0 = \frac{1}{2}$ gives rise to equation 4.3.

$$BER = P_1 \ast \text{erfc}(Q_1) + P_0 \ast \text{erfc}(Q_0)$$  \hspace{1cm} (4.2)

$$BER = \frac{\text{erfc}(Q_1) + \text{erfc}(Q_0)}{2}$$  \hspace{1cm} (4.3)

4.3.1 Other Performance Measures

In order to measure some additional performance metrics of the received signals, two additional metrics will be extracted from the eye diagrams.

The first measure will be the signal-to-noise ratio. This measure will measure how much of the received signal is noise and how much is signal. It will be computed using equation 4.4.

$$SNR = \frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}$$  \hspace{1cm} (4.4)

The second measure will be the eye opening factor. This measure will test how open the eye diagram is during the sampling interval. The closer to 1 the eye opening factor is, the more open the eye will be. It will be computed using expression 4.5.

$$\frac{(\mu_1 - \sigma_1) - (\mu_0 + \sigma_0)}{\mu_1 - \mu_0}$$  \hspace{1cm} (4.5)

4.4 Reference Driver

The reference driver will be used to compare the performance of the improved driver, which will be discussed in section 4.5. For a reference, the reference driver will operate over a normal FR-4 interconnect that is 5 cm long with a data rate of 4 Gbps and with capacitors to the ground reference to model the input and output capacitances of the I/O pads of the chips.
Figure 4.4: Reference driver.
4.4.1 Design

The design of this circuit is relatively simple, as it consists of a basic differential amplifier with $M_1$ and $M_2$ as the input transistors and the two resistors, $R$ and the interconnect, as the load on the amplifier. In this circuit $M_1$ and $M_2$ are sized to be identical to provide the same drive strength at the output of the driver and are sized to be able to drive the entire current of $I_{tail}$. For this reason $M_1$ and $M_2$ must be sized quite large to allow all of $I_{tail}$ to flow through them. Because the two drive transistors are so large, two buffers are used to buffer the input signal to the drive transistors to provide sharp-edged signals to the driver itself.

For the circuit to operate at 4 Gbps, the RC constant of the driver must allow the signals through without significant attenuation. Therefore the two resistors cannot be too large as this would increase the RC constant of the driver. Also, the resistors have to be sized to appropriately terminate the interconnect, therefore $R \approx Z_0$ where $Z_0$ is the characteristic impedance of the interconnect. The capacitance that dominates the output of the driver is the pad capacitance of the I/O pads on the chip.

4.4.2 Operation

This circuit has only two modes of operation: one for transmitting a logical ‘one’ and one for transmitting a logical ‘zero.’

Transmitting a ‘one’

For transmitting a logical ‘one’ bit, $M_1$ till turn on allowing current to flow through it, while $M_2$ will turn off preventing any current from flowing in that branch of the circuit. This allows $D_{out}$ to rise to near $Vdd$ and $\overline{D_{out}}$ to fall to form the differential signal transmitted down the interconnect.
Transmitting a ‘zero’

For transmitting a logical ‘zero’ bit, the transistors will reverse roles from the previous operation. Therefore $M_2$ will turn on, allowing current to flow through it, while $M_1$ will turn off, preventing any current from flowing in that branch of the circuit. In this case, $D_{out}$ will fall while $\overline{D_{out}}$ will rise up to $V_{dd}$ to form the differential signal transmitted down the interconnect to the receiver again.

4.4.3 Demonstration

The circuit was simulated in HSPICE using a pseudo random bit stream as the input to the driver. Measuring the output of the 5 cm long FR-4 differential interconnect at the input to the receiver, an eye diagram was constructed as shown in figure 4.5. In this figure, some noise can be seen. This is primarily reflections from
Table 4.1: Reference driver performance for a 5 cm FR-4 differential interconnect.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>‘one’ voltage level ($\mu_1$)</td>
<td>178 mV</td>
</tr>
<tr>
<td>‘one’ noise ($\sigma_1$)</td>
<td>22.9 mV</td>
</tr>
<tr>
<td>$NM_H$</td>
<td>128 mV</td>
</tr>
<tr>
<td>‘zero’ voltage level ($\mu_0$)</td>
<td>-179 mV</td>
</tr>
<tr>
<td>‘zero’ noise ($\sigma_0$)</td>
<td>22.8 mV</td>
</tr>
<tr>
<td>$NM_L$</td>
<td>129 mV</td>
</tr>
<tr>
<td>Bit error rate</td>
<td>$2.08 \times 10^{-15}$ errors/bit</td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>17.85 dB</td>
</tr>
<tr>
<td>Eye opening factor</td>
<td>0.87</td>
</tr>
</tbody>
</table>

The performance of this driver and interconnect is shown in Table 4.1, where the bit error rate, signal-to-noise ratio, and eye opening factors have been compiled. The bit error rate was computed using equation 4.3, the signal-to-noise ratio was computed using 4.4, and the eye opening factor was computed using equation 4.5. During the operation of this circuit, the measured power was 13.57 mW; this value is also reported in Table 4.3. The full schematic and transistor sizing for this driver is provided in Appendix A.

### 4.5 Improved Driver

This driver was proposed for on-chip signaling by Zhang [1], but because the silicon carrier interconnects behave similar to long on-chip interconnects, this driver will still work for chip-to-chip communication applications. This driver will be designed to operate over the interconnect described in Section 3.5.2, which will be 5 cm long. As with the reference driver, this driver will operate at 4 Gbps with a similar bit error rate as reported in Table 4.1. The data rate of 4 Gbps was chosen because it is only slightly higher than the cut-off frequency in of a 5 cm long silicon carrier interconnect.
as demonstrated in section 3.5.2, therefore it would still be possible to operate at this speed with some channel equalization to overcome the loss in the channel at the higher frequencies.

4.5.1 Design

The design of this circuit will involve more effort than with the reference driver, as this driver consists of many more parts. The various parts have been broken down into 3 sub-parts: the main data path, the equalization data path, and the delay cell as shown in figure 4.6. The design of each part will be described in the following three sections.

Main Data Path

The main data path of the driver is shown in the bottom box in figure 4.6. It consists of two buffers, bufA and bufB, and transistors $M5 - 8$. The transistors are sized to provide the necessary current to be sent down the interconnect to produce the voltage swing at the receiver. The current required to produce this effect is determined by equation 4.6, where $R_{\text{term}}$ is the termination resistor at the receiver and $V_{\text{swing}}$ is the required swing at the receiver. Because this driver is a differential driver, only half the static current, $I_{\text{static}}$, is required, and consequently the voltage swing is doubled.

$$2 \times I_{\text{static}} \times R_{\text{term}} = V_{\text{swing}} \quad (4.6)$$

The buffers in this data path serve two purposes: to buffer the incoming signals to allow for sharp edges at the output transistors $M5 - 8$ and to add a delay to the signals. The delay is set to be approximately identically to the delay in the logic for the equalization logic. By adding this delay, the control signals for all the output transistors will be presented to the transistor gates at nearly the same time in both the main data path and the equalization data path, which allows the transistors to work together to send the required amount of current down the interconnects.
Figure 4.6: Improved driver.
Equalization Data Path

The equalization data path of the driver is shown in the top box in figure 4.6. It consists of the delay cell, which will be discussed in the next section, and two tri-state buffers. The delay cell and the logic in the tri-state buffers detect ‘0’ to ‘1’ and ‘1’ to ‘0’ transitions of $D_{in}$ and $\overline{D_{in}}$. During these transitions the tri-state buffers will turn on to provide the necessary pre-emphasis to the signal to improve the quality of the received signal. During steady state, i.e. non transitioning input bits, the equalization output will be in a high impedance mode and not contribute to the operation of the driver.

The output transistors $M1-4$ are sized to compensate for the attenuation effects of the interconnect. This means that, for various lengths of the interconnects, only this part of the driver would need to be redesigned. Therefore, for very short interconnects this part of the driver may not be needed.

Delay Cell

The delay cell for this driver is not a flip-flop; instead it is made up of inverters as shown in figure 4.7. The inverters are comprised of long channel transistors, $M2$ and...
$M3$, which add an additional delay when compared to minimum channel transistors. Consequently, less transistors are needed to create a one clock period delay.

Because the transistors used to make up the inverters have some mismatch in the transconductance parameters between the PMOS, $K_p$, and NMOS, $K_n$, the delay for a ‘1’ is different from the delay of a ‘0.’ Therefore, restoring inverters, $M0$, $M1$, $M4$, and $M5$ are used between each long channel inverter pair to compensate for this mismatch and to progressively size the inverters to drive larger loads.

By utilizing inverters, there is no load on the clock to create the delay in the previous bit as there would be when utilizing a flip-flop to store the previous bit. Also, as reported by Zhang [1], the inverters provide some compensation for process corner variations. The delay will be increased on slow process corners to provide the additional pre-emphasis time for the reduced performance of the output transistors, and the delay will be decreased over fast process corners to remove the unneeded pre-emphasis time.

4.5.2 Operation

This circuit has two modes of operation: one mode is for transitioning bits, i.e. during ‘1’ to ‘0’ and ‘0’ to ‘1’ transitions, and the other for steady state operation, where the incoming bits are not transitioning.

Bit Transitions

During bit transitions, both the equalization data path and main data path are operating and supplying current to the interconnect.

During a ‘0’ to ‘1’ transition the transistors $M1$ and $M7$ in figure 4.6 will be on, pulling up $Dout$ and transistors $M4$ and $M6$ will be pulling down $\overline{Dout}$. This will send an emphasized ‘1’ bit down the interconnect. In this case $M1$ and $M7$ will be in parallel allowing for the pull up of $Dout$ to be faster than if only one transistor is on. The same is true to $M4$ and $M6$ and pulling down $\overline{Dout}$. 
During a ‘1’ to ‘0’ transition the transistors $M_2$ and $M_8$ in figure 4.6 will be on pulling down $Dout$, and transistors $M_3$ and $M_5$ will be pulling up $\overline{Dout}$. This will send an emphasized ‘0’ bit down the interconnect. Just as in the previous case, the paired transistors will be in parallel offering the pre-emphasis.

**Steady State**

During a steady state operation, the pre-emphasis is not needed. Therefore this portion of the output will be off, only utilizing the main data path for the output of the driver. This saves power on the driver by only sending a small static current down the interconnect as the swing requirements would already have been met with the pre-emphasis from the bit transition from the previous section.

While transmitting continuous ‘1’ bits, only transistors $M_6$ and $M_7$ in figure 4.6, will be on allowing a path for the current to flow to the interconnect. Whereas when transmitting continuous ‘0’ bits, the only transistors that will assist will be $M_5$ and $M_8$.

**4.5.3 Demonstration**

The circuit was simulated in HSPICE using a pseudo random bit stream as the input to the driver, the same bit stream as used with the reference driver. By measuring the output of the 5 cm long silicon carrier differential interconnect, with the same parameters from section 3.5.2, at the input to the receiver, an eye diagram was constructed as shown in figure 4.8. In this figure, some noise is evident throughout the whole signal, this is primarily due to the lossy effects of the silicon carrier interconnects and inter symbol interference. Also, the rise and fall times of the received signal is limited by the frequency response of the interconnect. This can be alleviated by means of a shorter interconnect length as mentioned in section 3.5.2. From the figure, the ‘one’ and ‘zero’ levels can be estimated to be approximately $\pm 130$ mV. The performance of this driver and interconnect is shown in table 4.2, where the bit
error rate, signal-to-noise ratio, and eye opening factors have been compiled. The bit error rate was computed using equation 4.3, the signal-to-noise ratio was computed using 4.4, and the eye opening factor was computed using equation 4.5. During the operation of this circuit, the measured power was 3.32 mW; this value is also reported in table 4.3. The full schematic and transistor sizing for this driver is provided in appendix B.

4.6 Summary

In this chapter, the design of two drivers for both a normal FR-4 and a silicon carrier interconnect operating at 4 Gbps were discussed. Both drivers achieved a similar bit error rate on the order of $10^{-15}$ errors/bit but with a significant power reduction for the improved driver over the reference driver. This reduction is in part
Table 4.2: Improved driver performance for a 5 cm silicon carrier differential interconnect.

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<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>‘one’ voltage level ($\mu_1$)</td>
<td>134 mV</td>
</tr>
<tr>
<td>‘one’ noise ($\sigma_1$)</td>
<td>15.1 mV</td>
</tr>
<tr>
<td>$\text{NM}_H$</td>
<td>84 mV</td>
</tr>
<tr>
<td>‘zero’ voltage level ($\mu_0$)</td>
<td>-127 mV</td>
</tr>
<tr>
<td>‘zero’ noise ($\sigma_0$)</td>
<td>13.8 mV</td>
</tr>
<tr>
<td>$\text{NM}_L$</td>
<td>77 mV</td>
</tr>
<tr>
<td>Bit error rate</td>
<td>$3.39 \times 10^{-15}$ errors/bit</td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>19.12 dB</td>
</tr>
<tr>
<td>Eye opening factor</td>
<td>0.89</td>
</tr>
</tbody>
</table>

due to a reduced voltage swing at the receiver for the improved driver but is primarily
due to the reduction in the static current of the drivers.

The areas of the two drivers can be approximated by summing up the widths of
all the gates in the circuit itself. For the reference driver, the area is approximated
to be 260 $\mu$m, while for the improved driver the area is almost 134 $\mu$m, which is
a 49% reduction in size of the circuits. However, because the improved driver uses
many more transistors, the layout design rules might reduce this reduction margin
somewhat.

The power supply currents for both drivers can be seen in figure 4.9. This current
is for the operation of the drivers while transmitting the bit stream ‘1011.’ In the
figure, the reference driver is on top in blue and the improved driver on the bottom
in red. It is clearly evident that there is a large reduction in the current being drawn
from the power rail for each driver. The static current is reduced by nearly 89% and
the peak currents by 69%. With the large reduction in peak currents, local effects
of power rail fluctuations and ground bouncing should be mitigated for the improved
driver when compared to the reference driver.

For comparison, the performance metrics have been compiled for both drivers in
table 4.3. From this table it is evident that both drivers have similar performance
metrics, but the power for the improved driver is reduced by nearly 75%, making it
a better choice for the short high speed interconnects like the silicon carriers. One
Figure 4.9: Vdd current usage.

Table 4.3: Driver performance at 4 Gbps.

<table>
<thead>
<tr>
<th></th>
<th>Reference driver</th>
<th>Improved driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit error rate</td>
<td>$2.083 \times 10^{-15}$</td>
<td>$3.390 \times 10^{-15}$</td>
</tr>
<tr>
<td>Signal to noise ratio</td>
<td>17.85 dB</td>
<td>19.12 dB</td>
</tr>
<tr>
<td>Eye opening factor</td>
<td>0.872</td>
<td>0.889</td>
</tr>
<tr>
<td>Power</td>
<td>13.57 mW</td>
<td>3.32 mW</td>
</tr>
<tr>
<td>Area (by gate widths)</td>
<td>260 $\mu$m</td>
<td>133.52 $\mu$m</td>
</tr>
</tbody>
</table>
of the power metrics of interest is the power-per-gigabit-per-second (W/Gbps). This metric allows drivers to be compared on a normalized scale so they can be compared more effectively. The reference driver achieved a power of 3.39 mW/Gbps, where as the improved driver achieved 0.83 mW/Gbps. With these metrics it is clear that the improved driver is much closer to making on-chip drivers capable of transferring data at 1 Tbps off the chip or at higher speeds [24].
Chapter 5

Conclusions

5.1 Summary

This work dealt with utilizing silicon carriers for System on Package applications, such as chip-to-chip communications. The benefits and drawbacks of silicon carriers over current packaging technologies were discussed as it pertains to chip-to-chip signaling. Several design trade-offs were discussed including power consumption, data throughput, and noise margins.

In essence, power savings is achieved by reducing the swing on the interconnect, trading it for a reduced noise margin, and then amplifying the signal again at the receiver. Since the power savings for the interconnect is greater than the power required for the amplifier at the receiver, this makes for a good trade-off. To help with the noise concerns for the reduced swing, differential signaling was used instead of a single ended signaling techniques that would have required additional shielding for crosstalk protection.

Through the utilization of silicon carriers, the power is further reduced and data throughput is increased because the input and output pads on the chips were no longer needed, instead micro-bumps provided the physical and electrical connection from the chip to the silicon carrier. However, the silicon carrier did show there was
an upper limit for interconnect lengths for high speed signaling applications, as the cut-off frequency noticeably decreased with the length.

The demonstrated results showed that the silicon carrier driver operating at the same speed offered about a 75% reduction in power over the reference driver for the FR-4 interconnect. Since the silicon carrier driver offered a better control over the current path, there was a substantial decrease in the peak current from the reference driver, which would also help with simultaneous switching noise. If the silicon carrier interconnect had been shorter, the pre-emphasis might not have been needed and would have further reduced the power consumption of the system.

5.2 Future Work

Off-chip signaling will continue to be an important area of research, especially as systems grow in complexity and size. Consequently, there are additional avenues of research to investigate the trade-offs of data throughput, power consumption, noise, delay, and area for silicon carriers.

Performance measures for additional signaling structures, such as the twisted differential signaling pair, should be investigated and would offer designers additional choices when designing the various interconnects. Similarly, additional signaling schemes should be investigated, including voltage mode and hybrid mode signaling.

As the systems increase in complexity, utilization of computer aided design (CAD) tools will become more important for achieving the best results when balancing noise, power, and throughput in large complex systems. Development of CAD tools to be integrated into the design flow will help automate the design of silicon carrier interconnects and driver placement on the chips.
Bibliography


Appendices
A

Reference Driver Transistor Sizing

The full transistor schematic for the reference driver is shown in figure A.1, where $R = 42 \, \Omega$ and the transistors are sized according to table A.1. In the table, the transistors in bold indicate the transistors that are connected to the interconnect.
Figure A.1: Full schematic for reference driver.

Table A.1: Full transistor sizing for reference driver.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0 (L = 270 nm)</td>
<td>10</td>
</tr>
<tr>
<td>M1 (L = 180 nm)</td>
<td>5</td>
</tr>
<tr>
<td>M2 (L = 180 nm)</td>
<td>65</td>
</tr>
<tr>
<td>M3</td>
<td>45</td>
</tr>
<tr>
<td>M4</td>
<td>45</td>
</tr>
<tr>
<td>M5</td>
<td>10</td>
</tr>
<tr>
<td>M6</td>
<td>5</td>
</tr>
<tr>
<td>M7</td>
<td>20</td>
</tr>
<tr>
<td>M8</td>
<td>10</td>
</tr>
<tr>
<td>M9</td>
<td>10</td>
</tr>
<tr>
<td>M10</td>
<td>5</td>
</tr>
<tr>
<td>M11</td>
<td>20</td>
</tr>
<tr>
<td>M12</td>
<td>10</td>
</tr>
<tr>
<td>All other transistors (L = 50 nm)</td>
<td></td>
</tr>
</tbody>
</table>
B

Improved Driver Transistor Sizing

The full transistor schematic for the improved driver is shown in figure B.1. In the figure, $D_{in}[n-1]$ and $D_{in}[n-1]$ are supplied from the delay cell in section B.1 and are the delayed versions of $D_{in}[n]$ and $D_{in}[n]$, respectively. The transistors are sized according to table B.1. In the table, the transistors in bold indicate the transistors that are connected to the interconnect.

B.1 Delay Cell

The full transistor schematic for the delay cell is shown in figure B.2. The transistors are sized according to table B.2.
Figure B.1: Full schematic for improved driver.
Table B.1: Full transistor sizing for improved driver.

<table>
<thead>
<tr>
<th>Data path transistor</th>
<th>W (µm)</th>
<th>Equalization path transistor</th>
<th>W (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M20</td>
<td>0.18</td>
<td>M0</td>
<td>17.5</td>
</tr>
<tr>
<td>M21</td>
<td>0.09</td>
<td>M1</td>
<td>7.5</td>
</tr>
<tr>
<td>M22</td>
<td>0.54</td>
<td>M2</td>
<td>17.5</td>
</tr>
<tr>
<td>M23</td>
<td>0.27</td>
<td>M3</td>
<td>7.5</td>
</tr>
<tr>
<td>M24</td>
<td>1.64</td>
<td>M8</td>
<td>5</td>
</tr>
<tr>
<td>M25</td>
<td>0.82</td>
<td>M9</td>
<td>5</td>
</tr>
<tr>
<td>M26</td>
<td>0.18</td>
<td>M10</td>
<td>2.5</td>
</tr>
<tr>
<td>M27</td>
<td>0.09</td>
<td>M11</td>
<td>5</td>
</tr>
<tr>
<td>M28</td>
<td>0.54</td>
<td>M12</td>
<td>5</td>
</tr>
<tr>
<td>M29</td>
<td>0.27</td>
<td>M13</td>
<td>5</td>
</tr>
<tr>
<td>M30</td>
<td>1.64</td>
<td>M14</td>
<td>2.5</td>
</tr>
<tr>
<td>M31</td>
<td>0.82</td>
<td>M15</td>
<td>5</td>
</tr>
<tr>
<td>M4</td>
<td>6</td>
<td>M16</td>
<td>2.5</td>
</tr>
<tr>
<td>M5</td>
<td>3</td>
<td>M17</td>
<td>1.25</td>
</tr>
<tr>
<td>M6</td>
<td>7</td>
<td>M18</td>
<td>2.5</td>
</tr>
<tr>
<td>M7</td>
<td>3</td>
<td>M19</td>
<td>1.25</td>
</tr>
</tbody>
</table>

All transistors (L = 50 nm)
Figure B.2: Full schematic for delay cell.
Table B.2: Full transistor sizing for delay cell.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>0.18</td>
</tr>
<tr>
<td>M1</td>
<td>0.09</td>
</tr>
<tr>
<td>M2*</td>
<td>0.18</td>
</tr>
<tr>
<td>M3*</td>
<td>0.09</td>
</tr>
<tr>
<td>M4</td>
<td>0.18</td>
</tr>
<tr>
<td>M5</td>
<td>0.09</td>
</tr>
<tr>
<td>M6</td>
<td>0.36</td>
</tr>
<tr>
<td>M7</td>
<td>0.18</td>
</tr>
<tr>
<td>M8*</td>
<td>0.36</td>
</tr>
<tr>
<td>M9*</td>
<td>0.18</td>
</tr>
<tr>
<td>M10</td>
<td>0.36</td>
</tr>
<tr>
<td>M11</td>
<td>0.18</td>
</tr>
<tr>
<td>M12</td>
<td>0.72</td>
</tr>
<tr>
<td>M13</td>
<td>0.36</td>
</tr>
<tr>
<td>M14*</td>
<td>0.72</td>
</tr>
<tr>
<td>M15*</td>
<td>0.36</td>
</tr>
<tr>
<td>M16</td>
<td>0.72</td>
</tr>
<tr>
<td>M17</td>
<td>0.36</td>
</tr>
<tr>
<td>M18</td>
<td>1.2</td>
</tr>
<tr>
<td>M19</td>
<td>0.6</td>
</tr>
</tbody>
</table>

* Long channel transistor (L = 90 nm)
All other transistors (L = 50 nm)