Abstract

Terry, David B. Ultra High Vacuum Physical Vapor Deposition of Yttrium Aluminate and Hafnium Aluminate High-\(k\) dielectrics on Silicon. (Under the direction of Gregory N. Parsons.)

Ultra high vacuum physical vapor deposition is used to deposit thin films of varying yttrium:aluminum and hafnium:aluminum concentrations on H-terminated silicon(100) and oxidized \textit{ex-situ} at several temperatures. X-ray Photoelectron Spectroscopy is used to analyze the surface composition of the films and electrical properties were evaluated using capacitance-voltages measurements with aluminum electrodes. The diffusion of silicon into the dielectric films is decreased with high concentrations (>78\%) of aluminum. However, at high concentrations of aluminum a relatively thick interfacial oxide layer is formed. The flatband voltage shifted from \(-0.18\)V to \(-0.78\)V for the hafnium oxide films and \(-1.22\)V to \(-1.18\)V for yttrium oxide films. The flatband voltage shifted from \(-0.55\)V to \(-0.61\)V for 70\% Hf:Al mixture and \(-0.78\)V to \(-0.76\)V for 42\%Y:Al mixture. These flatband voltage shifts indicate that hafnium based mixtures are more sensitive to thermal treatments than yttrium based mixtures. Also, capacitance-voltage measurements show the ability to tune the flatband voltage and possibly vary the rate of silicon oxidation (tune equivalent oxide thickness) by aluminum alloying.
Ultra High Vacuum Physical Vapor Deposition of Yttrium Aluminate and Hafnium Aluminate High-k Dielectrics on Silicon

by

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A thesis submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the Degree of Master of Science

CHEMICAL ENGINEERING

Raleigh, North Carolina

2004

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1. Chapter 1: Introduction

Aggressive progress in complementary metal-oxide-semiconductor (CMOS) integrated circuit technology has allowed device performance and speed to meet market demand. One such attempt to meet this demand is the continual reduction of the dimensions in a metal-oxide-semiconductor field effect transistor (MOSFET) termed “scaling” to increase the density of transistors per chip. Figure 1.1 is a cross section of a typical MOS device drawn to scale in the vertical and horizontal dimensions for the 350 or 250 nm technologies.[1]

In the case of improving the performance associated with scaling, we will consider a simplified, source referenced, strong-inversion model for the drive current of MOSFET devices written as:

\[
I_{DSN} = \frac{W}{L} \mu C_{inv} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]
\]  

(1)

where \(W\) is the width of the transistor channel, \(L\) is the channel length, \(\mu\) is the channel carrier mobility, \(C_{inv}\) is the gate dielectric capacitance density when the underlying channel is in the inverted state, \(V_{GS}\) and \(V_{DS}\) are the voltages applied to the gate and drain, respectively, and \(V_T\) is the threshold voltage. A plot of \(I_{DSN}\) will initially increase linearly with \(V_{DS}\) and reach a maximum when \(V_{DS,\text{sat}} = V_{GS} - V_T\). The corresponding value of the drive current is found by using \(V_{DS} = V_{DS,\text{sat}}\) from Eq. (1):

\[
I'_{DSN} = \frac{W}{L} \mu C_{inv} \left[ \frac{(V_{GS} - V_T)^2}{2} \right].
\]  

(2)

The range for the term \((V_{GS} - V_T)\) is limited by reliability and room temperature operation constraints since temperature <100°C typically cause statistical fluctuations in thermal
energy.[2] Therefore, increasing drive current, $I_{DSN}$, by decreasing the channel length or an increase in gate dielectric capacitance would improve device performance.

To increase the gate dielectric capacitance we will consider a parallel plate capacitor. It must be noted that quantum mechanical effects and depletion effects from the Si substrate and gate electrode will be ignored for the discussion of gate capacitance. The capacitance can be expressed as follows:

$$C = \frac{\kappa \varepsilon_0 A}{t}$$

(3)

where $\kappa$ is the dielectric constant (also referred to as the relative permittivity), $\varepsilon_0$ is the permittivity of free space, $A$ is the area of the gate electrode, and $t$ is the thickness of the gate dielectric. It can be seen that decreasing the dielectric thickness would increase the gate capacitance and ultimately improve the device performance. However, device performance does not actually scale with dielectric thickness due to Fowler-Nordheim (FN) tunneling (quantum mechanical electron tunneling through a triangular potential), direct tunneling of carriers or by trap-assisted components (after being stressed), which increase leakage current with decreasing dielectric thickness and ultimately degrade device performance.

Rearranging Eq. (3), we can express device performance in terms of equivalent dielectric thickness

$$\frac{t_{eq}}{\kappa_{SiO_2}} = \frac{t_{high-k}}{\kappa_{high-k}}$$

(4)

or

$$t_{high-k} = \left( \frac{\kappa_{high-k}}{\kappa_{SiO_2} = 3.9} \right) \bullet t_{eq}$$

(5)
where $\kappa_{\text{SiO}_2}$ is the dielectric constant for SiO$_2$, $\kappa_{\text{high-k}}$ is the dielectric constant for an alternative dielectric with $\kappa_{\text{high-k}} > \kappa_{\text{SiO}_2}$, and $t_{\text{eq}}$ is the theoretical thickness of SiO$_2$. In order to achieve the desired device performance a physically thicker film is allowed with an alternative high-k material.

As shown in table 1, International Technology Roadmap for Semiconductors (ITRS) 2003 predicts the following device dimensions by the year of 2018 and beyond [3]:

<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Actual Trend Numbers (nm)</td>
<td>101</td>
<td>90</td>
<td>71.4</td>
<td>63.6</td>
<td>58.5</td>
<td>45</td>
<td>35.7</td>
<td>31.8</td>
<td>25.3</td>
<td>22.5</td>
<td>17.9</td>
</tr>
<tr>
<td>ITRS Rounded Node Numbers (nm)</td>
<td>100</td>
<td>90</td>
<td>70</td>
<td>65</td>
<td>50</td>
<td>45</td>
<td>35</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
</tr>
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The minimum feature size in the above table is defined as the minimum size line that can be patterned and transformed to wafers which is associated with the channel length. It is limited by lithography techniques.

The following sections will focus on the issues associated with the scaling of the channel gate capacitance. In fact, the gate stack including the oxide-silicon interface, the gate insulator and the gate electrode is believed to be among the most critical challenges for a MOS device since the gate oxide is quickly approaching its atomic (and absolute) limit. Figure 1.2 is another version of the projected dimensions for gate insulator with years in linear scale. The figure indicates that the equivalent oxide thickness, $t_{\text{ox}}$, should be no more than 1 nm at the 50 nm generation, which is only a few atomic layers thick for SiO$_2$.

As the SiO$_2$ layer shrinks below 3 nm, quantum mechanical (QM) tunneling through the gate oxide starts playing a significant role (Figure 1.3). Additionally, experimental gate oxide tunneling currents for oxide thickness from 3.5 nm to 2.9 nm [4] and calculated curves between 3.5nm and 1.4nm are illustrated in Figure 1.4. This clearly indicates the domination
of direct tunneling over the voltage range under study. An upper limit of gate current was suggested to be 1 A/cm² (see figure 1.4). However, Hauser et al. argued that 30 A/cm² of gate current may be tolerable and a 1.5 nm SiO₂ layer may work.[1] Good device performance has been experimentally obtained with 1.5 nm oxides at gate lengths of around 100 nm.[5] QM effects also influence the carrier distribution perpendicular to the oxide surface. A peak in carrier distribution exists 1–3 nm in the silicon away from the oxide-silicon interface, which adds an “effective oxide thickness” of several angstroms to the real oxide thickness. For 50 nm and beyond generations, these QM effects will begin to dominate and significantly increase equivalent oxide thickness (EOT). Therefore, the study of alternative high-k gate dielectrics with reduced gate leakage currents appears critical.

Some of the effective replacement materials for silicon dioxide that are currently being investigated to replace silicon dioxide (k ~ 3.9) include Al₂O₃ (k ~ 8-11.5), HfO₂ (k ~ 26-30), ZrO₂ (k ~ 22.5-28), Y₂O₃ (k ~ 14-17) and various mixtures. Again, the basic idea for using high-k materials is increasing the film thickness to reduce the tunneling leakage current and improve the reliability while scaling the equivalent oxide thickness below the direct tunneling limit of SiO₂. The materials were deposited by various methods and show leakage current suppression by several orders of magnitude. Although these results are very promising, many challenges are still present. A detailed research investigation will be discussed in the literature review section.
Figure 1.1: A cross-section view of a typical MOS device.
Figure 1.2: Projected device dimensions for future technology generations.
Figure 1.3: Projected device dimensions for future technology generations
Figure 1.4: Experimental tunneling currents for thin SiO$_2$ dielectric.
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2. Chapter 2: Literature Review

2.1 Ideal High-k Materials

An argument proposed repeatedly is that as silicon oxide approaches its physical limits a material with a higher dielectric constant and thermodynamically stable in contact with silicon while remaining amorphous in subsequent processing conditions may allow the use of physically thicker films while providing the same equivalent oxide thickness, \( t_{eq} \). Therefore, the following is a discussion of basic properties, dielectric processing and the performance requirements for alternative high-k materials.

First, the basic properties provide the initial criteria for selecting an alternative high-k material. The dielectric constant should lie in the range 10-30 and must be an insulator so it should have a band gap above \( \sim 5.0 \) eV. Figure 2.1 illustrates basic properties of current high-k candidates. Also, the alternative high-k material should be thermodynamically stable on Si upon high temperature anneals (needed for dopant activation for polysilicon gates). Unstable dielectric materials will form interfacial layers (see Figure 2.2), which are in series with the dielectric. The effect of reduced capacitance can be seen when the structure contains several dielectrics in series, the lowest capacitor (silicates and \( \text{SiO}_x \)-like interfacial layers) will dominate the overall capacitance, \( C_{tot} \),

\[
\frac{1}{C_{tot}} = \frac{1}{C_{\text{low-k}}} + \frac{1}{C_{\text{high-k}}} \tag{6}
\]

where \( C_{\text{low-k}} \) and \( C_{\text{high-k}} \) are the capacitance of the low-k dielectric and the high-k dielectric, respectively. Referring back to Eq. (5), an interfacial layer with low capacitance will ultimately compromise the minimum achievable \( t_{eq} \) value.

Second, the dielectric processing conditions will determine whether the microstructure is amorphous, polycrystalline, or epitaxial. Generally, the dielectric should be
non-reactive (thermodynamically stable) with the Si substrate or with the gate electrode at any processing condition and the interfaces should remain largely stress-free. Consequently, large interface constraints will force defect creation (dislocation, point defects) or new phases such as crystalline oxides, which lead to non-optimal properties. An amorphous dielectric must remain amorphous at processing conditions and during its operating life. Additionally, the dielectric must have low diffusivities to ionic transport to prevent gate materials from contaminating the transistor channel. A smooth surface is also critical to obtain a high quality dielectric-silicon interface.

Most importantly, the dielectric must behave as an insulator with low leakage currents. The leakage current will include contributions ranging from tunneling to defect-related channels involving dislocation, grain boundaries, and point defects. There should be a low effective fixed charge to reduce electron scattering in the Si in which large amounts of fixed charge ultimately lead to poor mobility. The densities of surface states, interface fixed charge, and bulk fixed charge should be as low as possible.

The requirement of low bulk defect density would be ideally fulfilled in crystalline materials [1]. However, to obtain a perfect interface, the high-k material should exactly match with silicon and therefore be grown epitaxially on the substrate. Even so, bond dipoles, even in a perfect lattice-matched interface, can lead to charge scattering and poor device performance. Also, grain boundaries inside crystalline materials act as fast diffusion paths and sites for preferential adsorption of impurities, which may contribute to a dramatic increase in leakage current. Amorphous materials are covalently bonded and exhibit considerable flexibility in their structure. Therefore, they should be able to provide a low defect density interface as far as they are thermodynamically stable in contact with silicon. A
major concern about amorphous high-k materials is whether they could be compatible with the subsequent processes of MOSFET fabrication and remains in their amorphous state.

2.2 Recent Studies on High-k Gate Dielectrics

2.2.2 Review on Aluminum Oxide

Initially, Al₂O₃ attracted much attention because it has a large band gap (9 eV), large conduction-band offset with silicon (2.8 eV), remains amorphous at T > 900°C, and exhibits a very low oxygen diffusion rate. Consequently, due to the large band-gap and band-offset, aluminum oxide has a very low leakage current density.

Amorphous Al₂O₃ films have been deposited by physical vapor deposition (PVD)[2], thermal chemical vapor deposition (CVD)[3-7] & plasma-enhanced chemical vapor deposition (PECVD) at low temperatures[8-10], and atomic layer deposition (ALD)[11-18] with triethyldialuminum tri-sec-butoxide (TEDA-TSB)[3-10] and trimethylaluminum (TMA)[11-18] precursors most widely used in literature. High-resolution transmission electron microscopy (HRTEM) was employed to explore the microstructural aspects of the ALD films (Figure 2.3)[12]. A continuously uniform film is observed and the deposited film is amorphous. The Al₂O₃/SiOₓNx/Si sample resulted in a ~2.0±0.3nm Al₂O₃ layer on ~0.5±0.3nm bottom oxynitride layer. For the H-passivated sample, the results showed ~2.4±0.3nm Al₂O₃ layer without an interfacial oxide. However, thin Al₂O₃ films deposited by CVD[3], found evidence of an aluminum silicate interface with Si (Figure 2.4). The silicate formation is most likely due to non-equilibrium conditions of excess oxygen during deposition and since the layer is thicker than expected may suggest additional oxidation mechanisms are present.
On the other hand, crystalline Si can be formed on Al₂O₃ without significant reaction between Si and Al₂O₃ [19]. The silicon/Al₂O₃ interface is abrupt to the resolution limit of TEM (a point resolution of 2.5 Å) and the silicon is locally fault-free. Ultimately, the ability to form an abrupt interface makes Al₂O₃ unique since most other high-k dielectric studied form a lower-k layer (SiO₂ or silicate) during deposition on Si substrates.

Most studies for aluminum oxide on Si show a measured flatband voltage shift in the positive direction compared to that expected by the electrode and substrate types used indicating the present of negative fixed charge. Although this shift could arise from damage associated with gate electrode deposition or other forms of processing treatments, it is typically interpreted as negative fixed charge within the oxide film. This result is unique since other alternative high-k replacement candidates typically show a negative shift indicating positive fixed charge. However, aluminum oxide is a short-term solution because of its relatively smaller dielectric constant than other high-k materials and therefore may be a deterrence to qualify it as an alternative to SiO₂.

2.2.3 Review on Group IIIB (Y₂O₃ & La₂O₃)

Yttrium oxide (Y₂O₃) is an attractive material as an alternative gate dielectric in CMOS application due to its wide energy band gap (~5.5 eV) [20], high dielectric constant (14–17) [21] and good thermal stability (stable up to 2325°C) [22, 23]. Another attractive property of Y₂O₃ is the lattice constant of crystalline Y₂O₃ which matches well with silicon: a(Y₂O₃)=10.06 Å, a(Si)×2=10.86 Å [24]. Lanthanum oxide (La₂O₃) largely stands out with its relatively large dielectric constant of 18-30 [25] with a comparable energy band gap of 5.4 eV [26].
Different deposition techniques have been used to grow Y₂O₃ and La₂O₃ on Si(100): electron beam deposition[23, 24, 27-32], thermal oxidation[21, 33], r.f. sputtering[34-39], and chemical vapor deposition[16, 40-42]. In all cases, group IIIB metal oxides have demonstrated interfacial layer formation that result from unwanted reaction with silicon or SiO₂. Additionally, yttria and lanthana have intrinsically large positive fixed charge that imposes electrical challenges (i.e. reduced mobility) and high oxygen affinities, which makes them susceptible to OH (water) absorption during exposure to the ambient.

2.2.5 Review on Group IVB (HfO₂ & ZrO₂)

A substantial amount of investigation has gone into group IVB metal oxides, specifically HfO₂ and ZrO₂ by different deposition techniques such as: e-beam evaporation[32, 43-46], physical vapor deposition[47-58], chemical solution deposition[59], chemical vapor deposition[7, 60-90] and atomic layer deposition[16-18, 91-97]. The HfO₂ and ZrO₂ dielectrics are attractive since they are thermodynamically stable in contact with Si[22, 90]. HfO₂, especially, has many desirable properties such as high dielectric constant (~30), high heat of formation (~271 kcal/mol)[98] and relatively large band gap (~5.68 eV).[99] While these materials are thermodynamically stable under equilibrium conditions, processing often leads to an unintentional SiOₓ-like interfacial layer that reduces the overall dielectric constant. Furthermore, HfO₂ and ZrO₂ systems demonstrate the ability to achieve low tₑq values with lower leakage currents than would be achieved using comparable SiO₂ films but tend to crystallize at relatively low temperatures (~500°C), leading to polycrystalline films, with apparent enhanced leakage current paths along grain boundaries.
2.2.6 Review of Pseudobinary Alloys

Oxide alloying is an attempt to combine and complement the desirable properties from several materials, and thereby overcome the deficiencies associated with the individual materials. These materials are predominantly non-stoichiometric mixtures, and are therefore termed pseudobinary.

Aluminates (and silicates) have the underlying principle of mixing a high-k (crystalline) metal oxide with an amorphous, stable, low-k material (\(\text{Al}_2\text{O}_3\) or \(\text{SiO}_2\)) to obtain a desirable morphology with suitable properties for CMOS gate dielectrics. The effect of adding \(\text{Al}_2\text{O}_3\) or \(\text{SiO}_2\) to metal oxides is to produce an amorphous film that is thermodynamically stable on Si. The overall permittivity of the pseudobinary alloy is inevitably lower than the pure metal oxide, but this tradeoff can be very adequate for the improved stability.

There has been less information reported on aluminates than other pseudobinary alloys such as silicates. Several techniques were used to develop the aluminate films such as: flame-fusion method[100], e-beam evaporation[101], reactive sintering from powders[102, 103], physical vapor deposition[104-106], chemical vapor deposition[107-112], and atomic layer deposition[113-120].

Some intriguing published results[112] show a significantly larger positive flatband voltage shift than the end member oxides with significant hysteresis (Figure 2.5) where the energy of localized electron traps (Figure 2.6) of 0.2-0.3 and 1.4eV above the Si conduction band edge were associated with \(\text{AlO}^1\text{\_{terminal}}\) bonding groups rupturing of the network and anitbonding Hf atom \(d\) states, respectively. Structural characteristics of \(\text{HfO}_2\)-\(\text{Al}_2\text{O}_3\) nanolaminates using high-resolution transmission electron microscopy (HRTEM) (Figure
2.7) composed of HfO₂ and Al₂O₃ layers show an amorphous structure up to the annealing temperature of 870°C where the boundary layers are flat and the nanolaminate structure is maintained. At temperatures above 920°C, the laminate structure is drastically broken and accompanied by a structural transition from amorphous to a crystalline state. A dielectric constant of ~10 from the accumulation capacitance of the as-grown film gradually increased to ~17 as the annealing temperature increased.[113]
Chapter Two Figures

Figure 2.1: Comparison of relevant properties for high-k candidates with conduction band offset, $\Delta E_C$, and valence band offset, $\Delta E_V$. Dielectric constant values are in parenthesis.
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Figure 2.7: HRTEM data for Al₂O₃-HfO₂ nanolaminate film of (a) as-grown film and (b) annealed at 920°C.
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3. Chapter 3: Research Tools and Approaches

This chapter will examine how dielectric films are deposited as part of the fabrication of integrated circuits. Important issues in film deposition include the physical and chemical properties of the film. Also, chemical vapor deposition (CVD) and physical vapor deposition (PVD) processes will be discussed, along with the various analytical tools necessary to study the deposited films.

3.1 CVD System

3.1.1 Remote PECVD System

CVD processes are based on chemical reactions to deposit materials using a metal precursor source in the gas phase. A low sticking coefficient and isotropic arrival angle distribution lead to good step coverage (allowing deposition into smaller and deeper holes and spaces), and CVD processes, used mostly for dielectrics, in general have these attributes. This is partly due to the source gas filling the whole chamber and having a short mean free path. However, CVD process may have contamination problems (mostly carbon impurities from precursors).

Remote PECVD (RPECVD) has several advantages over conventional direct PECVD [1]. In a direct PECVD process, the substrate is placed in the plasma excitation region and the process gases are subjected to the direct plasma excitation, which can contribute to the gas phase generation of a significant number of deposition precursors allowing many parallel reactions to occur and may lead to the formation of undesirable bonding groups. RPECVD can control the reaction pathways more easily than conventional PECVD since only part of the process gases are subjected to the direct plasma excitation. RPECVD can also minimize
the damage from the plasma ions by placing the substrate outside the plasma generation region.

Our remote PECVD system (Figure 3.1) has a copper coil with an inner diameter > 32 cm wrapped around a 32-cm quartz tube. By applying a RF power, a capacitive plasma can be generated. Two gas dispersal rings with small holes is used to flow metalorganic, silane and inert gases. The outer ring has a diameter of 3.75”, while the diameter of the inner ring is 2.5”.

3.1.2 UHV-PVD system

In PVD, the processes are physically, rather than chemically, based and are generally more versatile than CVD methods, allowing for the deposition of almost any material. The depositing material comes from a remotely located area source or target and often arrives at the wafers in a more directed manner. For sputter PVD, the sticking coefficient is usually higher than CVD processes depending on system geometry (e.g., target size, target-to-wafer distance, rotation of substrate), operating condition (e.g., pressure), and the depositing material. In general, physical processes dominate and sputtered atoms attach to the substrate surface and mostly remain attached without desorbing. No surface reaction occurs other than simple condensation. As a result, thickness uniformity, shadowing by surface topography, and step coverage can be very important issues in PVD deposition.

The PVD system used for our studies (Figure 3.2) uses a RF magnetron sputtering system with 2-inch sputter targets. It can simultaneously reactive sputter three targets using Ar, O₂, N₂, and Xe inert gases onto a rotating and heating 8” wafer sample holder.
3.2 Physical and Chemical Characterization Techniques

3.2.1 Surface Profilometry

A Tencor Alpha-Step 500 surface profilometer is used to physically measure film thickness. An apparatus with a diamond needle stylus mechanically moves across the sample and traces the topography of the film so that the profilometer can measure surface roughness or the height of a step (> 80 Å). The step is made by placing a cover slide on the silicon sample before deposition, the cover serves as a shadow mask. For deposition conditions that involve the precursors with low sticking coefficient or high surface mobility, a step created by the cover slide can be difficult to achieve because the precursors or reactants may diffuse underneath the slide. In this situation, lithographic techniques can be used to create the step. Photoresist will be applied to cover half the film, and then dipped into a buffered HF oxide etch (BOE) solution till the solution droplets bead up on the uncovered silicon surface indicating the oxide has been etched away since a bare silicon surface is hydrophobic and the oxide is hydrophilic. In fact, the etch rate is also a parameter of interest since BOE cannot etch some silicates. Then the photoresist is removed by trichloroethylene or acetone, and the dielectric step remaining is used to determine the thickness.

3.2.2 Ellipsometry

Ellipsometry can also be used to determine the thickness of films as well as optical constants. Spectroscopic ellipsometry (SE), like single wave ellipsometry but using multiple wavelengths, is a true contactless, noninvasive technique measuring the change in polarization state of light reflected from the surface of a sample. A VASE SE system (J. A. Woollam Co., Inc.) with combination of variable angle of incidence is used to measure the aluminate films. However some difficulties may be encountered when measuring thin films

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(<100Å). This may be due to the limitations of ellipsometry on accuracy and uncertainty of the calculated film parameters which stem from 1) the choice of starting assumptions during data analysis, i.e., there are different dispersion relations or dielectric functions for the dielectric film, none of which is taken to be the standard; and 2) the inevitable correlation of variables when extracting multiple variables in the very thin film regime [2]. This may also be from the uncertain composition of the aluminate films, and the presence of a silicate layer at the silicon and high-k interface. Since very thin films (20-50 Å) of high-k dielectrics are important to the CMOS industry, the ellipsometry must be combined with other methods for thickness measurement, such as transmission electron microscopy (TEM).

3.2.3 Fourier Transform Infrared Spectroscopy

Chemical bonds having a dipole moment absorb light in the infrared range of the spectrum. Fourier transform infrared spectroscopy (FTIR) measures the vibrational modes of various bonds. Hence IR absorption analysis is an excellent tool to observe water adsorption (OH groups) and CO₂ reactions leading to carbonates (C-O groups) on high-k dielectric films when exposed to atmospheric conditions. The instrument used is a Nicolet Model 750 and has a wavenumber range of 400-4000 cm⁻¹. Chemically bonded groups in the dielectric films have vibrational frequencies in this range and each group will absorb light at a specific range of wavenumber values.

3.2.4 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface analysis technique where an incident X-ray beam results in the emission of photoelectrons from the surface (and near surface region) of the material. The binding energy of these photoelectrons is used to identify different elements and bonding environments near the surface region. Collecting the
electrons that emerge at small angles to the surface plane increases the surface sensitivity of
photoelectron spectroscopy. These electrons must travel a longer distance in the solid, and
therefore they are more likely to be absorbed unless they are generated at the surface or near
the surface region. The electron kinetic energy is related to the incident X-ray energy as:

$$E_{\text{kin}} \approx h\nu - E_B$$

where $E_B$ is the binding energy of the electron and is characteristic of the atom from which it
was emitted. These values are well tabulated in literature.[3] The shift in the binding energy
corresponds to different oxidation states of the atom. Hence XPS can be used to establish
what elements are present and the bonding environment on the surface.

3.2.5 Auger Electron Spectroscopy

Auger electron spectroscopy (AES) uses a focused electron beam of 3-5 keV to excite
Auger electrons out of outer shells of the atoms in the film. The energy of Auger electrons is
measured to determine the elements present in the sample. Since Auger electrons are readily
absorbed in all solids, the Auger technique samples a depth of typically 5 to 50 Å. The most
frequent use for AES is a depth information method by obtaining a spectrum from the
surface, then to remove a fixed number of atomic layers by ion bombardment and to repeat
the analysis until the desired depth has been reached [4]. In this way, the variation in
composition with depth can be determined.

3.2.6 Rutherford Backscattering Spectroscopy

Rutherford backscattering spectroscopy (RBS), also known as high-energy ion
(back)-scattering spectrometry (HEIS), is based on bombarding a sample with energetic ions
(typically He ions of 1 to 3 MeV energy) and measuring the energy of the backscattered He
ions [5]. It is quantitative without recourse to calibrated standards. It can determine the
masses of the elements in the film, their depth profile over distances from 100Å to several microns from the surface, and the crystalline structure in a nondestructive way. The depth resolution is on the order of 100 Å. RBS is particularly suitable for heavy elements on light substrates. Its major weakness is the difficulty of measuring light elements on a heavy substrate.

3.2.7 Transmission Electron Microscopy

Transmission electron microscopy (TEM) provides extremely high special resolution imaging, approaching 1.5 Å. Since the incident electron beam must pass entirely through the section, which needs to be prepared only ten to hundreds of nanometers thick, the sample preparation is a significant challenge [6]. The three primary imaging modes are bright-field, dark-field and high-resolution microscopy. In particular, high resolution TEM (HRTEM) gives structural information on the atomic size level and has become very important for interface analysis. Physical thickness, presence of interface layers or smoothness of an interface and crystallinity of a film can be obtained from TEM. However, small crystallites may amorphize from ion beam bombardment in sample preparation.

Electron energy loss spectroscopy (EELS) is the analysis of the distribution of electron energies for electrons transmitted through the film [5]. EELS is very sensitive to low-Z (Z=atomic number) elements (Z ≤ 10). It is mainly used to obtain microanalytical and structural information approaching the very high resolution of the electron beam.

3.3 Electrical Characterization

3.3.1 Electrical Measurements on MOS Capacitors

Capacitance-Voltage Measurements
High- and low frequency capacitance-voltage (C-V) measurements can be performed on MOS capacitors (MOSCAPs). The parameters that can be extracted include flat band voltage ($V_{fb}$), threshold voltage ($V_{th}$), doping concentration of the substrate, fixed charge ($Q_f$), interface traps density ($D_{it}$), and oxide thickness ($t_{ox}$). The dielectric constant is obtained by the equation $\varepsilon = \frac{C_{t_{ox}}/A}{\varepsilon_0}$, where $C$ is the capacitance, $A$ is the electrode area, $\varepsilon_0$ is the vacuum permittivity. The fixed oxide charge is deduced by the shift in the measured $V_{fb}$ from the ideal case where $V_{fb} = \Phi_{ms}$, the work function difference of the semiconductor and metal. As the gate dielectric thickness is less than 2.5 nm, a universal model by Hauser for high-frequency C-V data can be used to extract parameters of interest.[7]

MOSCAPs with field oxide isolation and contact pad are better than those made from shadow masks and the use of mercury probe. The devices made from shadow masks suffer various problems including large corner electrical field, humidity effect, charging from the environment and processing damage. Very small devices cannot be used ($<2.5 \times 10^{-5} \text{ cm}^2$) due to the difficulties in probing small dots.

**Current-Voltage Measurements**

Current-voltage (I-V) measurements can also be performed on MOSCAPs. Leakage current and mechanism (Fowler-Nordheim tunneling or direct tunneling) may be extracted.

3.3.2 Electrical Measurements on MOSFETs

The electrical measurements must be done on both PMOS and NMOS devices since the gate dielectrics may not work on both of the structures. In addition to the C-V and I-V measurements done on MOSCAPs devices, other measurements can also be done on MOSFETs. Measurements of $I_d-V_d$ as a function of $V_g$ can be used to extract transconductance and the surface mobility in the channel, where $I_d$ is the drain current, $V_d$ is
the drain voltage and $V_g$ is the gate voltage. Threshold voltage and sub-threshold swing can be extracted from $I_d$-$V_g$ measurements. Other parameters such as $I_{dss}$ (drain saturation current), $I_{off}$ (off state drain (leakage) current at $V_g = 0$) and series resistance of the MOSFETs in the ‘on’ condition may be determined.
Chapter Three Figures

Figure 3.1: Remote PECVD system
Figure 3.2: ultra high vacuum-PVD system
References


4. Chapter 4: Experimental Results of Aluminate Dielectrics

Chapter 4 is a draft manuscript being prepared for publication.
Thermal Stability of $(\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ and $(\text{Y}_2\text{O}_3)_x(\text{Al}_2\text{O}_3)_{1-x}$ formed by oxidation of $\text{Hf}_x:\text{Al}_{1-x}$ and $\text{Y}_x:\text{Al}_{1-x}$ mixtures on Si

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Abstract

Yttrium:Aluminum & Hafnium:Aluminum oxide mixtures were investigated as a possible replacement for SiO$_2$ gate dielectric. Capacitance versus voltage analysis indicates that addition of Al to Hf and Y oxides results in a positive shift in flatband voltage with increasing Al concentration for both set of mixtures. XPS investigation of Y(or Hf) and Al chemical states of the alloy films indicate the films are a homogenous mixture of HfO$_2$ (or Y$_2$O$_3$) and Al$_2$O$_3$. 
Introduction

The 2003 International Technology Roadmap for Semiconductors (ITRS) suggests a gate dielectric thickness below 1.0nm for the 65nm generation by 2007 if industry continues to use silicon oxynitride[1]. Because of the aggressive scaling of complementary metal oxide semiconductor (CMOS) devices, SiO$_2$ gate dielectrics are approaching their physical limits due to direct charge tunneling as dielectric thickness decreases. In order to achieve the desired device performance by reducing leakage currents, a physically thicker film is allowed with an alternative high-k material. Therefore, the study of alternative high-k gate dielectrics with reduced gate leakage currents appears critical.

Currently there is intense effort in the search for a high-k dielectric replacement for SiO$_2$, with Y$_2$O$_3$, Al$_2$O$_3$, HfO$_2$, ZrO$_2$, and their silicate and aluminate forms as the leading candidates for an alternative high-k dielectric[2-4], and studies of TiO$_2$ and Ta$_2$O$_5$ have received some attention.[5, 6]. The hope is that materials with a higher dielectric constant than SiO$_2$ will reduce tunneling. Theoretically, these oxides are stable on Si surface at equilibrium, however, since metal deposition processes are under non-equilibrium conditions all high-k dielectrics (with the important exception of Al) have a significant tendency to form large interfacial layers upon high temperature post deposition anneals. Thus meeting appreciable equivalent oxide thickness have proven to be very difficult since any lower-k interfacial layer will ultimately decrease the overall capacitance of the dielectric. Additionally, most high-k materials will become crystalline or poly-crystalline during post deposition anneals. Grain boundaries provide current pathways and degrade the gate oxide’s ability to electrically separate the gate electrode from the channel.
Recently, transition metal aluminates have become attractive as a possible replacement for SiO₂, such as \((\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}\) [7-17], \((\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}\) [18-22], and \((\text{La}_2\text{O}_3)_x(\text{Al}_2\text{O}_3)_{1-x}\) [23, 24]. The theory of pseudobinary alloys is to mix a high-k crystalline material with a low-k amorphous material to create a more thermodynamically stable dielectric on silicon. Additionally, Al₂O₃ has uniquely demonstrated an abrupt interface with silicon. Therefore, alloying aluminum with high-k transition metal oxides may provide a more abrupt interface. However, the permittivity for the pseudobinary alloy is lower than the transition metal oxide (high-k material), but this tradeoff may be warranted for improved device performance. Previous studies have shown that intrinsic negative fixed charge is present in Al₂O₃/Si interfaces and intrinsic positive fixed charge in Y₂O₃(or HfO₂)/Si interfaces. Therefore alloying transition metal oxides with aluminum oxide is a possible way to achieve charge neutrality at the high-k/Si interface. Such charge compensation may promote electrical tuning such as flatband voltage, \(V_{FB}\).

Charge compensation (chemical modification) of transition metal oxide films by means of aluminum alloying to form transition metal aluminates, specifically YaAlOₓ (LaAlOₓ) and HfAlOₓ, may improve the stability and electronic performance of the dielectric/silicon interface in electronic devices. Charge compensation is based on the idea of combining a dielectric with positive fixed charge, \(+Q_f\) (oxides of yttrium, lanthanum, and hafnium) and a dielectric with negative fixed charge, \(-Q_f\) (aluminum oxide) to create a charge balanced dielectric. It is instructive to consider the energy-band diagram for ideal MIS structures (Figure 4.1) using (a) n-type and (b) p-type substrates. For these ideal structures, at \(V=0\) applied voltage on the metal gate, the work function difference between the metal and the substrate, \(\Phi_{MS}\), is zero.
\[ \Phi_{MS} = \Phi_M - \left( \chi + \frac{E_g}{2q} - \Psi_B \right) = 0 \; \text{for } n\text{-type} \]  

(7)  

\[ \Phi_{MS} = \Phi_M - \left( \chi + \frac{E_g}{2q} + \Psi_B \right) = 0 \; \text{for } p\text{-type} \]  

(8)  

where \( \Phi_M \) is the metal work function, \( \chi \) is the semiconductor electron affinity, \( E_g \) is the semiconductor band gap, \( \Phi_B \) is the potential barrier between the metal and dielectric, and \( \Psi_B \) is the potential difference between the Fermi level and the intrinsic Fermi level. Under these conditions, the energy bands are flat (shown in Figure 4.1) and the \( V = V_{FB} = 0 \). However, due to fixed charge in dielectric, the measured \( V_{FB} \) can be expressed as:

\[ V_{FB} = \Phi_{MS} \pm \left( \frac{Q_f}{C_{acc}} \right) \]  

(9)  

where \( C_{acc} \) is the measured capacitance in accumulation. We will study mixing a positive fixed charge dielectric with a negative fixed charge dielectric where the total fixed charge, \( Q_{tot} \), will be equal and opposite to \( \Phi_{MS} \) (\( Q_{tot} = -\Phi_{MS} \)) which will allow us to operate at \( V_{FB} = 0 \).

The primary focus in this project is to achieve a better understanding of the fundamental issues concerning the constitutive and electrical behavior of transition metal aluminate dielectrics. Therefore, we will concentrate on obtaining fundamental chemical and electrical data pertaining to the bond formation and bond arrangement at the interfaces of a metal gate/M:Al/Si substrate structure with M=Y, La, or Hf using remote PECVD and PVD with post deposition anneals as possible routes to optimal interface formation.
Experimental Approach

Thin films of transition metal oxides (\(\text{Y}_2\text{O}_3\) and \(\text{HfO}_2\)) and films with varying concentration of Y(or HF):Al metal mixtures were formed by oxidation of metal mixtures. Metal mixtures were deposited using ultra high vacuum physical vapor deposition, and oxidation was performed by \textit{ex-situ} furnace oxidation in the presence of dry air. The Si(100) substrates were prepared by J.T. Baker clean for 5 min, deionized water (DI) rinse for 5min, and buffer oxide etch (BOE) for 1 min. They were blown dry with nitrogen and placed in the PVD loadlock.

The Y, Hf, and Al targets were purchased from Target Materials with a 99.99%, 99.5%, and 99.999% purity, respectively. Variations in homogeneous mixtures of the deposited metal films were accomplished by varying the r.f. power and sputtering for a fixed amount of time based on measured single metal deposition rates. Metal oxide semiconductor capacitors were formed with 2000Å Al electrodes by shadow mask Al metal evaporation.

Film characterization was performed using X-ray Photoelectron Spectroscopy (XPS) and capacitance-voltage (C-V) analysis. XPS was conducted on a Riber LAS3000 instrument equipped with a single-pass, cylindrical mirror (MAC2) analyzer. An Mg K\(\alpha\) (\(h\nu=1253.6\) eV), non-monochromatic X-ray source at a 90° take-off angle was used for all measurements. Step sizes of 1.0eV and 0.1eV were used to obtain survey and detailed XPS spectra, respectively. C-V measurements were conducted on an HP4284 LCR with a 1 MHz sweeping frequency from –3 to 1 Volt. Capacitor areas were measured using a Nikon Eclipse Optical Microscope equipped with a digital camera. Small electrode areas, \(~1\times10^{-5}\) cm\(^2\), were measured to avoid instrumental errors associated with large areas. Equivalent
oxide thickness (EOT) and flatband voltage were extracted from C-V data using the NCSU CV program.[25]
Results and Discussion

Y:Al & Hf:Al films with thickness ~25Å were deposited on H terminated Si(100) substrates and oxidized ex-situ at 400 to 700°C in dry air at atmospheric pressure for 2 minutes. XPS was then used to analyze the surface composition of the films and spectral regions are displayed in Figures 4.2 and 4.3 for Y:Al and Hf:Al mixtures, respectively. The films were sufficiently thin enough to detect the 99.3eV Si substrate peak in the Si 2p spectra (except for the 100% Hf film). Consider first the Y:Al films in Figure 4.2. For the Si 2p spectra in Figure 4.2a the feature at 99.3eV is from the Si substrate. The intensity of the substrate peak decreases with increasing Al fraction consistent with increasing film thickness with increasing Al content. The feature near 103eV is due to oxidized silicon either at the dielectric/silicon interface and/or oxidized Si in the dielectric film bulk. The relative size of the Si-O feature increases with increasing Al content. The position of the Si-O peak near 103eV shifts to lower binding energy as Y content increases from 0 to 78%, then it shifts to higher binding energy as Y content increases further. This is likely due to a relatively large amount of silicon in the film bulk (ie, y-silicate) for low Al content, and a relatively thick interfacial oxide layer for high Al content. This is also consistent with the position of the O1s peak for these films, shown in Figure 4.2b.

For the Hf case, shown in Figure 4.3a-b, the Si-O peak intensity decreases with increasing Hf content and peak position stays nearly fixed at 103.0eV. The O1s peak shifts smoothly from 533.0eV to 531.5eV with increasing Hf content. This data is consistent with silicate at the dielectric/silicon interface, but with lower silicon content as compared to the Y samples.
The electrical properties of Y:Al and Hf:Al mixtures were evaluated by C-V measurements with Al electrodes (without a forming gas anneal being performed). The effects of temperature on flatband voltage for end member Y$_2$O$_3$ and HfO$_2$ films as shown in Figure 4.4. The measurements were made with voltage sweeps from depletion to accumulation at 1 MHz. With increasing temperature, the flatband voltage increases positively for Y$_2$O$_3$ and negatively for HfO$_2$ films. The flatband voltage for HfO$_2$ films were more sensitive to temperature than the Y$_2$O$_3$ films because the magnitude of negative shift for HfO$_2$ is greater than the positive shift for Y$_2$O$_3$ which can be seen in Figure 4.4 by the steepness of the slopes. The flatband voltage shifted from $-0.18$V to $-0.78$V for the hafnium films and $-1.22$V to $-1.18$V for the yttrium films over the temperature range. However, both series show a negative flatband shift indicating positive fixed charge. No attempt was made to distinguish oxide trapped and interface trapped charge in this work.

A continuing investigation on the effects of temperature can be seen in Figure 4.5 on 42% Y:Al and 70% Hf:Al mixtures. Similar effects were observed for the mixtures. Hafnium based mixtures were more sensitive to temperature than yttrium based mixtures. The flatband voltage shifted from $-0.55$V to $-0.61$V for the hafnium based films and $-0.78$V to $-0.76$V for the yttrium based films over the temperature range. So far, all films continue to show negative flatband voltage indicating positive fixed charge. Figures 4.6 & 4.7 illustrate the hysteresis of 70mV for 42% Y and 210mV for 70% Hf films, respectively.

The ability to tune flatband voltage with Al alloying was also investigated. Figure 4.8 shows the effects of Al alloying on Yttrium and Hafnium oxide films. The films were annealed at 700°C in air for 2 min (except 500°C for 100% Al). A positive shift in flatband voltage was observed for both series with increasing Al composition with yttrium films.
showing a larger sensitivity to Al alloying. A zero flatband voltage was never achieved in any of the films possibly due to dangling bonds at the silicon interface. Dangling bonds are usually associated with lattice mismatch between high-k dielectric films in contact with Si substrate, which is consistent with negative voltages shown in Figures 4.4c. It may be possible to recover the flatband condition via H₂ forming gas anneal to passivate the observed dangling bonds.

The effects of Al alloying on equivalent oxide thickness (EOT) was also investigated. There was an increase in EOT with increasing temperature, in most cases, for YAlOₓ and HfAlOₓ films seen in figures 4.9 and 4.10, respectively. This is likely because at higher temperatures, oxygen can diffuse with relative ease through both deposited metal mixture series and react with the silicon surface forming an interfacial silicate layer. This is consistent with the binding energy peak shifts in the XPS data. Also for several films, we observed a systematic increase in EOT with decreasing aluminum composition possibly due to the higher reactivity of Y (or Hf) metals to OH groups than the Al metals.
Conclusions

Yttrium:Aluminum & Hafnium:Aluminum mixtures were grown on H-passivated Si(100) substrates by PVD and *ex-situ* furnace oxidation in dry air. XPS analysis revealed that silicon consumption was evident regardless of Al composition. The ability to distinguish if a single silicate type layer or a stack of silicate and aluminate layers is uncertain. However, C-V measurements show the ability to tune the flatband voltage and possibly vary the rate of silicon oxidation (tune EOT) by aluminum alloying. Without a forming gas anneal, dangling bonds still exist at the high-k/silicon interface and therefore a zero flatband voltage was not achieved for this experiment. Under optimal conditions, we believe a transition metal:aluminum film composition with a zero flatband voltage and minimal substrate consumption will be achieved in future experiments.
Chapter Four Figures

Figure 4.1: Energy-band diagrams and associated high-frequency C-V curves for ideal MIS diodes for (a) n-type and (b) p-type semiconductor substrates. For these ideal diodes, V=0 corresponds to a flatband condition. For dielectrics with positive (+Qf) or negative (-Qf) fixed charge, an applied voltage (V_{FB}) is required to obtain a flatband condition and the corresponding C-V curve shifts in proportion to the fixed charge.
Figure 4.2: XPS of PVD Y and Al metals.
Figure 4.3: XPS of PVD Hf and Al metals.
Figure 4.4  effects of temperature on flatband voltage for end member Y$_2$O$_3$ and HfO$_2$ films
Figure 4.5: Effects of temperature on flatband voltage for 42% Y$_2$O$_3$ and 70% HfO$_2$ films
Figure 4.6: Hysteresis for 42% YAlO$_x$ film with flatband voltage, $V_{FB}$. 

$V_{FB} = -0.72 \text{V}$
Figure 4.7: Hysteresis for 70% HfAlO$_x$ film with flatband voltage, $V_{FB}$. 
Figure 4.8: Effects of Al alloying on Yttrium and Hafnium films.
Figure 4.9: The effect of aluminum alloying on equivalent oxide thickness (EOT) for YAlO_x films.
Figure 4.10: The effect of aluminum alloying on equivalent oxide thickness (EOT) for HfAlO_x films.
References

5. Chapter 5: Future Work

In view of the stringent specifications discussed previously, the quality and characteristics of the interfaces between the silicon substrate/high-k/gate electrode are key issues towards a successful integration of transition metal aluminum alloys into advanced technologies. For high-performance applications where very low EOT values are targeted, interfacial SiO$_2$-type layer must be kept to a minimum. The high-k layer should be thermally stable and have a low number of electrically active defects. In order to achieve good bulk properties and minimal SiO$_x$ interfacial layer formation it is essential to establish well-controlled processing conditions and post-deposition anneals. The optimization of the full gate stack requires the understanding of various interactions that are occurring. The overall thermal stability of the high-k layer must be investigated, including the effect of the silicon substrate (lower interface) and gate electrode (upper interface) interactions with the high-k dielectric (refer to Figure 2.2) and other chemical changes (i.e. crystallization or phase separation) that may occur during various process steps. However, there are additional factors, such as polysilicon depletion effects (which degrades the total capacitance of gate dielectrics by adding a few angstroms of EOT) and boron diffusion into the channel region (which causes significant, undesired shifts in $V_{FB}$ and $V_T$ values), associated with using polysilicon gate electrodes. As a result, there is immense interest in using a metal gate electrode. Metal gate not only eliminates the gate depletion and boron penetration problems but also greatly reduces the gate sheet resistance. Also, it reduces the thermal budget since the high thermal anneals needed for dopant activation is eliminated. Therefore, the feasibility of using gate metal electrodes for low EOT and their interactions with transition
metal aluminate dielectrics should be investigated. Specifically, dual metal gate using two separate metals (one with a high work function of around 5 eV and the other with a low work function of around 4 eV) should be investigated in order to achieve the desirable threshold voltages for both p-MOSFET and n-MOSFET bulk CMOS devices. Figure 5.1 illustrates the energy diagrams for NMOS and PMOS FET devices using metal gate electrodes.

The primary focus of this future work is to achieve a better understanding of the fundamental issues concerning the constitutive and electrical behavior of transition metal aluminate dielectrics. Therefore, we will concentrate on obtaining fundamental chemical and electrical data pertaining to the bond formation and bond arrangement at the interfaces of a metal gate/M:Al/Si substrate structure with M=Y, La, or Hf using remote PECVD and PVD with post deposition anneals as possible routes to optimal interface formation. Also, we will study the effects of various processing conditions on interface stability and electrical behavior for 50nm node MOSFET technology. Additionally, this work will concentrate on characterizing the thermophysical properties of transition metal aluminate alloys and the development of new optimally designed dielectric alloys.

In the light of limited availability of literature dealing with transition metal aluminates under actual MOSCAP and MOSFET operating condition, the following objectives are proposed:

1. Demonstrate novel modifications of bulk Y$_2$O$_3$ and HfO$_2$ dielectrics with Al alloying. This will include showing qualitatively that aluminum alloying can be used to controllably modify constitutive properties and electrical behavior.

2. Establish a fundamental understanding of chemical routes for bulk and interface modifications. This will involve determining the extent of interfacial layer formation.
at the Y (or Hf):Al/Si interface and possibly bulk phase separation during varying process conditions. Also this study will evaluate electronic performance of new YAlOₓ & HfAlOₓ dielectrics established from 1 above and the effects of nitridation barriers on silicate formation.

3. Study interfacial properties of transition metal aluminate dielectrics (established from 1&2) against dual metal gates. This will involve studying chemical states at the dielectric/gate electrode interface and possibly identify interface charge formation. Also, we will investigate a performance evaluation of *in-situ* MOSCAP fabrication.

**Sample preparation and deposition**

Two clean substrate samples will be prepared prior to each YAlOₓ, LaAlOₓ & HfAlOₓ film deposition run. One is from a blank wafer for chemical and physical characterization; the other is from a patterned wafer for electrical measurements. The patterned wafer is fabricated in the following way: J. T. Baker clean, growth of field oxide and definition of the active region. The blank and patterned samples will be cleaned with J. T. Baker solution and dipped in a diluted 10:1 HF solution to remove the native oxide right before the deposition. Then, the YAlOₓ, LaAlOₓ & HfAlOₓ films will be deposited using Triethyl(tri-sec-butoxy)dialuminum [TEDA], Tris(2,2,6,6-tetramethyl-3,5-heptanedionato) yttrium [Y(TMHD)], Tris(2,2,6,6-tetramethyl-3,5-heptanedionato) lanthanum [La(TMHD)] and Hafnium t-butoxide [Hf(t-but)] in the PECVD reactor (Figure 3.1) or co-sputtered 2” metal targets in an ultra high vacuum PVD reactor (Figure 3.2). O₂, N₂O and water can be used as oxygen sources. The temperatures vary from 200 to 400°C and the pressure is in the range between 0.2 and 1 Torr.
4.1 **Study Novel Alloying of high-k dielectrics.**

The initial experiments will focus on observing phenomological trends with M:Al mixtures with M=Y, La, Hf. We have experience with plasma enhanced chemical vapor deposition of yttrium oxide, aluminum oxide, and their silicates,[1-5] and with physical vapor deposition of yttrium, hafnium, lanthanum, zirconium, and their silicates.[6-10] We will use a similar technique in our PECVD reactor and an ultra high vacuum PVD reactor on HF last silicon substrates.

This study will focus on observing the shift in $V_{FB}$ with aluminum alloying of Y and Hf films in PVD and Y, La, Hf films in PECVD processes (see Figure 5.2). We speculate that charge compensation by varying the aluminum composition in yttrium oxide and hafnium oxide films will yield a dielectric films with $V_{FB}=0$. Other trends to be studied will be the effect of process conditions (temperature, Al composition) on equivalent oxide thickness (EOT). Studying the modulation of $V_{FB}$ and EOT values can give a qualitative approximation to the extent of silicate formation.

We will characterize these films using surface and electrical characterization tools available to us, including XPS, FT-IR, and C-V. FT-IR will be used to identify OH adsorption and CO$_2$ reactions and its effect on EOT values. XPS data will be used to measure the peaks for Y 3d, Hf 4f, Al 2p, Si 2p, and then calculate the composition of the films by integrating the peaks areas. This will identify the films’ composition at $V_{FB}=0$ to obtain a charge neutral film. Additionally, XPS peak binding energy shifts will be used to determine if phase separation will occur for thin films by observing local Al$_2$O$_3$, Y$_2$O$_3$, La$_2$O$_3$ and HfO$_2$ environments. To obtain $V_{FB}$ values, we will measure the capacitance versus gate voltage (C-V) for the films and use the NCSU CV program.[11]
4.2 Study of $\text{SiO}_x$ layer formation at dielectric/substrate interface.

The enhanced oxidation of silicon is believed to be present in remote PECVD of metal precursors or during the subsequent oxidation anneal. We will therefore test for an interfacial $\text{SiO}_x$ layer formation when our precursors are PECVD deposited directly on silicon or during the rapid thermal anneals for PECVD & PVD films. It will be beneficial to compare the two processes since silicon substrate oxidation can be highly process dependent.

Oxygen, $\text{N}_2\text{O}$, and $\text{N}_2$ plasma with possibly He or $\text{H}_2$ dilution will be used for PECVD films and Ar plasmas for PVD films. The influences of the operation parameters including oxidation temperatures, pressures, RF powers, and flow rates of plasma & precursor gases need to be studied to have the best control of the interface layer formation.

For each run, we will measure dielectric samples using XPS and compare the Si 2p, Al 2p, Y3d, and Hf 4f peak binding energy shifts to determine the extent of interface formation. Other XPS features will also be analyzed such as silicide formation (also using the appropriate peak binding energy shift) by PVD since the metal deposits directly on the substrate and may form silicides (which are conductive and therefore degrade dielectric functionality) and impurity incorporation. Other techniques such as AES and RBS combined with FTIR can be used to characterize the chemical compositions, chemical oxidation states of the constituents, and depth profiling of the films. We will also use TEM and EELS, if available, to look for evidence of an interfacial layer formation during PECVD and PVD processes. Besides the thickness, TEM can provide the information about the crystallinity (amorphous, polycrystalline or crystalline) and the microstructure (single- or multi-layer) of the deposited films. Based on these results, we will develop another experiment set to determine the extent of oxidation/nitridation needed to inhibit silicate formation.
Controlling the structure and composition of the interface layer can lead to good electronic quality of metal silicate/silicon interfaces. The stoichiometry of yttrium (lanthanum or hafnium) aluminate films can be adjusted by controlling the ratio of the precursor partial pressures; composition will be obtained from XPS peak measurements. This study will focus on the influences of operation parameters (substrate temperature, pressure, ratio of the flow rates for the yttrium and aluminum precursors, RF power, flow rate of oxidizing species, etc.) on the electrical properties of the films. Effects of post-deposition anneals on interfacial layer formation will also be studied.

After the deposition of aluminate films, various annealing techniques can be studied to improve the electrical properties by minimizing the interface traps and fixed charge densities. Forming gas anneal, rapid thermal anneal (RTA), conventional anneal in inert gases and oxidizing gases (O₂, N₂O, etc.) will be considered. After post deposition anneal, Al evaporated gates (~2000Å) will complete the gate stack and the electrical properties such as threshold voltage (V_{th}), doping concentration of the substrate, fixed charge (Q_{f}), interface traps density (D_{it}), and oxide thickness (t_{ox}) from C-V curves and transconductance and the surface mobility in the channel from I-V curves, will be correlated to the chemical compositions and physical structures. Thus, monitoring electrical properties while varying processing parameters will be used to determine the optimal deposition conditions.

A quantitative evaluation of the activation energies for a SiOₓ-like interface layer may be employed to gauge the extent and rate of its formation. The activation energy for interface layer formation will be determined by an Arrhenius plot using XPS data. Plotting the ratio of [SiO]/[Si] versus inverse temperature will yield the energy of activation for silicate formation.[8, 12]
4.3 Study interlayer formation at the dielectric/electrode interface.

Because of the deleterious effects associated with scaling polysilicon gate electrodes (i.e. high gate resistance, polysilicon depletion, and boron penetration into the channel), this study will investigate transition metal aluminate dielectrics stability in contact with dual metal gate electrode. Current studies with dual metal gates include titanium[13], molybdenum[13], tantalum[14], and ruthenium[15]. Since, Zhong et al. [16] have demonstrated Ru and RuO₂ gate electrodes to have good thermal stability on ZrO₂, ZrSiO₄, and Y-silicate dielectric, we propose that Ru based dual gate electrodes in contact with hafnium (having very similar properties to zirconium) & yttrium alloy mixtures may show similar promising results. In the course of our research, this study will be performed in the second, and possibly the third year of our research. Therefore, within this time frame, if a new candidate metal electrode shows promising results in thermal stability with hafnium or yttrium based dielectrics we will consider studying the interface stability of our transition metal aluminates with such a new gate metal electrode.

This study will focus on processing conditions and post deposition anneals on YAlox & HfAlox reactions with Ru based gate electrodes. For each run, we will measure XPS and compare the Y 3d, Hf 4f, Al 2p, Si 2p, and Ru 4f peak binding energy shifts to determine the extent of upper interface layer formation. Other XPS features will also be analyzed such as silicide formation and impurity incorporation. Other techniques such as AES and RBS combined can be used to characterize the chemical compositions, chemical oxidation states of the constituents, and depth profiling of the films. We will also use TEM and EELS, if available, to look for evidence of an upper interface layer for PECVD and PVD processes. Besides the thickness, TEM can provide the information about the crystallinity (amorphous,
polycrystalline or crystalline) and the microstructure (single- or multi-layer) of the deposited film. Based on these results, we will develop another experiment set to determine the extent of oxidation/nitridation needed to inhibit interface layer formation.

Electrical measurements will be performed on the patterned samples. C-V and I-V measurements will be done on MOS capacitors. Referring to Eq. 9, we will now use this equation to help determine the metal work function since we are using a new metal gate. After the deposition of aluminates films, various annealing techniques can be studied to improve the electrical properties by minimizing the interface traps and fixed charge densities. Forming gas anneal, rapid thermal anneal (RTA), conventional anneal in inert gases and oxidizing gases (O₂, N₂O, etc.) will be considered. The electrical properties should be correlated to the chemical compositions and physical structures. Thus, the electrical properties can be improved by optimizing the deposition process.

Also, in-situ MOSCAP fabrication will be performed since OH and CO₂ groups from ambient exposure has been shown to have significant reactivity with yttrium[4], hafnium[17], zirconium[17], and lanthanum[10] based dielectrics. Therefore the in-situ deposition of dual metal electrode will act as a capping barrier to OH groups reacting with the underlying dielectric during ex-situ anneals. Figure 5.3 illustrates a similar process for in-situ device fabrication using field oxide isolation. However, dual metal deposition will follow a process similar to studies by Zhong[16] using lift-off lithography.
Figure 5.1: Energy diagram of threshold voltages for NMOS and PMOS FET devices using (a) midgap metal gates and (b) dual metal gates. \( E_c \) is the conductance band, \( E_v \) is the valence band, \( \Phi_M \) is the work function of the metal indicated and \( V_T \) is the threshold voltage.
Figure 5.2: Energy-band diagrams and associated high-frequency C-V curves for ideal MIS diodes for (a) n-type and (b) p-type semiconductor substrates. For these ideal diodes, $V=0$ corresponds to a flatband condition. For dielectrics with positive (+$Q_f$) or negative (-$Q_f$) fixed charge, an applied voltage ($V_{FB}$) is required to obtain a flatband condition and the corresponding C-V curve shifts in proportion to the fixed charge.
Figure 5.3: schematic process for *in-situ* MOSCAP fabrication. a) photoresist deposited and patterned, b) isolation regions defined and photoresist removed, c) sequentially, dielectric deposited, vacuum anneal, and dual metal deposited, d) gate contacts defined and etched.
References


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