ABSTRACT

LIU, FUDE. Interfaces in Novel Electronic Materials. (Under the direction of Dr. Gerd Duscher.)

Si-based devices have been scaling down over a forty year time span, following Moore’s law. However, materials are now an important constraint. One of the most serious problems is now the field effect transistor (FET) gate dielectric. The thickness of the gate SiO$_2$ layer presently is becoming so thin that gate current leakage becomes a problem due to the tunneling effect. So it is desirable to find high-K dielectrics to replace SiO$_2$ so that a physically thicker gate dielectric can be used and then the tunneling effect can be reduced or avoided. Very recently, more interest has been shown in the La-based material system. In this study, a main part of effort was put on amorphous LaScO$_3$ and La$_2$O$_3$/SiO$_2$ alloys grown on Si (001) substrate, using a lot of TEM techniques. We have demonstrated that amorphous LaScO$_3$ ($\leq$3.5 nm) can be deposited directly on Si substrate as a gate dielectric for CMOS devices. However, oxygen diffusion through the thin LaScO$_{3+x}$ film and reaction with Si substrate increased the EOT and the interface roughness at 1000 °C. So possible oxygen sources at 1000 °C need to be eliminated. As to the high-K La-silicate layer on Si, we also studied the interface structure and the chemical composition in detail. It was shown that the high-K La-silicate capped with UHV-W is a good choice for the next generation gate dielectric. Excess oxygen caused the TaN grain growth and then the rough interface between the high-K layer and the TaN layer, and gave rise to the SiO$_x$ layer between the high-K layer and the Si substrate. The chemical changes across the high-K layer were well determined. All these results give us a deep understanding about the promising La-based oxides as the next generation gate dielectric.
Compared to the mature Si industry, III-nitrides had been long regarded as a scientific curiosity. They have now earned a most respected place in modern electronic and optoelectronic devices. Unlike silicon and other traditional materials such as GaAs, III-nitrides are particularly suitable for high-frequency, high-power and high-temperature applications. Unfortunately, the choice of appropriate substrate materials for III-nitrides is still one of the biggest issues to be solved. Sapphire offers a compromise as the most widely used substrate material to date. And much remains to be known about the interface structures and GaN inversion domain boundaries (IDBs). In this study, we tried to determine these interface structures and GaN-IDBs. To the GaN films on c-sapphire with a low temperature AlN (LT-AlN) nucleation layer, the 7.5:8.5 theory about misfit edge dislocations of LT-AlN on c-sapphire was confirmed. The theoretical threading dislocation density in AlN was derived to be $8.48 \times 10^{13}/cm^2$. The direct polarity determination of GaN was successfully realized for the first time. The interface atomic structure of LT-AlN on c-sapphire was determined. For the first time, we experimentally explained why LT-AlN layers can invert the polarity of GaN. The exact 3-D geometry of AlN pits was determined for the first time. The GaN IDBs were also studied in detail. A transition region with mixed polarities was found with the convergent beam electron diffraction (CBED) method. The transition region was related to the not well defined edge of the LT-AlN. As to the interface of GaN on c-sapphire, the 7.2:6.2 theory was confirmed. The dislocation loops were observed experimentally. The chemical reaction between GaN and sapphire at high temperature was identified. The interface structure of GaN on sapphire was determined for the first time. Also for the first time, we experimentally explained the N-face polarity of GaN directly grown on sapphire. Finally, a more accurate GaN IDB was proposed.
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by

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DEDICATION

To Lei Ji, our families, and our friends
FUDE LIU was born in FuYang, AnHui, China. He went to primary school when he was 7 years old. Being a wild child had made his childhood full of a lot of fun. He stayed there until he finished his high school at HongQi Middle School and was admitted with the highest scores in FuYang by South China University of Technology (GuangZhou, China) in 1993. He stayed there until he received his Master degree in Materials Science in 2000. After graduation, he worked for Johnson Electric (HongKong) on Micro-Motors for a while before he went to Rutgers University where he got his Master degree in Ceramics Engineering. In 2004, he transferred to NC State University to continue his PhD study.
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1. INTRODUCTION

1.1 Amorphous High-K Gate Dielectrics for Si-based Field Effect Transistors

The devices have been scaling down over a forty year time span, following Moore’s law. However, the scaling can not go forever. The limits are often believed to be in lithography and the availability of sufficiently small light wavelength to pattern the minimum feature size. It turns out that materials are now also an important constraint. The materials issues include interconnect conducting materials, gate metals, low-K dielectrics as the inter-circuit passivants, high-K gate dielectrics. One of the most serious problems in logic circuits is now the field effect transistor (FET) gate dielectric.\(^1\)

The thickness of the gate SiO\(_2\) layer presently is becoming so thin (<1.6nm) that gate current leakage becomes a problem due to the tunneling effect. Mainly due to this reason, it is desirable to find high-K dielectrics to replace SiO\(_2\) so that a physically thicker gate dielectric can be used and then the tunneling effect can be reduced or avoided. Therefore, the objective is to develop high-K dielectrics which allow scaling to continue to ever lower values of ‘equivalent oxide thickness’ (EOT).

The choice of a high-K dielectric needs to meet a few requirements\(^1\), i.e., a high enough K, band offsets with Si of over 1 eV, thermodynamically and kinetically stable with Si, good interface with Si, few bulk electrically active defects. Based on these criteria, many candidate materials have been found. Most of them are oxides. In about 2001, the choice of oxides was narrowed down to Hf-based materials. However, the focus has been shifted to La-based oxide or its alloys recently after it was found that there are a lot of problems with Hf-
based materials. However, not much is known about this La-based material system. In this study, a main part of efforts was put on LaScO$_3$ and La$_2$O$_3$/SiO$_2$ alloys grown on Si (001) substrate. It needs to be pointed out that we just studied amorphous oxide films which are the lowest cost solution. Obviously, polycrystalline oxide is not a choice due to the grain boundary related problems. Epitaxial oxide films are thought to be the long term solution, but there are still a lot of issues needed to be solved about epitaxial oxide films on Si.

1.2 The Rise of GaN-based Devices

III-nitrides commonly refer to AlN, GaN, InN and their alloys. Long regarded as a scientific curiosity, they have now earned a most respected place in modern electronic and optoelectronic devices. Unlike the conventional semiconductors such as Si and GaAs with a diamond or zinc-blende structure, III-nitrides have a thermodynamically stable structure, wurtzite. The large difference in electronegativity between the group III elements (Al=1.18, Ga=1.13, In=0.99) and nitrogen (N=3.0) leads to very strong chemical bonds in III-nitride material system; also III-nitrides have a wide range of direct energy gaps ($E_g$(AlN)=6.2 eV, $E_g$(GaN)=3.44 eV, $E_g$(InN)=0.7 eV). These are the origin of many interesting properties of III-nitrides.

The direct bandgap of III-nitrides is one of their most beneficial features for optoelectronic device applications such as light-emitting diodes (LEDs), laser diodes (LDs), and photo-detectors. Most importantly, AlInGaN compounds exhibit a direct bandgap energy that can be continuously tailored between 0.7 eV (or wavelength, 1780 nm) and 6.2 eV (or wavelength, 200 nm) and thus covers the near infrared to near UV spectral bands. It is also
known that III-nitrides are very robust materials with high melting points, mechanical strength, high thermal conductivity, high saturated electron drift velocities, and the ability to resist radiation damage. All of these make III-nitrides a material system suitable for high-frequency, high-power and high-temperature applications such as transistors for RF transmission applications. Plus, GaN-based spintronics is one of the newest GaN-related research topics\(^7\), which aims to make use of electron spin besides electron charge for device applications. Moreover, III-nitrides are polar crystals as they do not have a center of symmetry. The crystal polarity of GaN can be inverted from N-face polar to Ga-face polar by the low temperature AlN (LT-AlN) nucleation layer, which provides a new degree of freedom for the investigation of III-nitrides and their devices\(^8\).

Unfortunately, the choice of appropriate substrate materials for III-nitrides is still one of the biggest issues to be solved. Compared to Si and SiC, sapphire offers a compromise as the most widely used substrate material to date. And much remains to be known about the interface structures of LT-AlN on c-sapphire and GaN on c-sapphire, and GaN inversion domain boundaries (IDBs). In this study, we tried to determine these interface structures aimed for GaN-based transistors and GaN-IDBs aimed for some potential novel devices.

References


(2005).


2 LITERATURE REVIEW

2.1 Amorphous High-K Dielectrics on Si (001)

The thickness of the SiO$_2$ layer presently used as the gate dielectric for the complementary metal oxide semiconductor (CMOS) devices is about 1 nm. At this thickness, the gate leakage current due to the tunneling effect is becoming a serious issue. For the device scaling to continue, this material constraint has to be encountered. In this section, we introduce the important role played by high-K dielectrics in Si-based transistors, then why more efforts are putting on the study of La-based high-K dielectrics, and finally, the materials issues related to this new material system.

2.1.1 High-K Dielectrics and Si-based Transistors

One important property of a dielectric material is its permittivity. Permittivity ($\varepsilon$) is a measure of the ability of a material to be polarized by an electric field. The dielectric constant (K) of a material is the ratio of its permittivity $\varepsilon$ to the permittivity of vacuum $\varepsilon_0$, so $K = \varepsilon / \varepsilon_0$. The dielectric constant is therefore also known as the relative permittivity of the material. The dielectric constant (K), consequently, defines the capacitance ($C = \varepsilon_0$ KA/d) of any capacitor comprising of a layer of dielectric sandwiched between two metal plates (Fig.1). Capacitance is a measure of the ability of a material to hold charge if a voltage is applied across it ($Q = CV$). All other parameters equal, K would determine capacitance of the structure shown in Fig. 1, or in other words, it would define the extent of capacitive coupling between two conducting plates. So with a high-K dielectric such coupling would be strong, and with a low-K dielectric being obviously weak. The K value
of SiO$_2$ is 3.9. Dielectrics featuring K>3.9 are referred to as high-K dielectrics while dielectric featuring K<3.9 are defined as low-K dielectrics.

Fig. 1 A capacitor comprising of a layer of dielectric sandwiched between two metal plates and its capacitance $C$ defined by the dielectric constant $K$ of the dielectric layer$^1$.

In cutting edge silicon electronics, high-K dielectrics are needed to implement fully functional very high-density integrated circuit. High-K dielectrics are needed in MOS gate stacks to maintain sufficiently high capacitance of the metal (gate)-dielectric-Si structure in MOS/CMOS transistors (Fig. 2). Due to the continued scaling of the channel length (L), and hence reduced gate area A, the need to maintain sufficient capacitance of the MOS gate stack was met by gradual decrease of the thickness of SiO$_2$ gate oxide (see the equation shown in Fig. 1). Obviously, such scaling cannot continue indefinitely as at certain point gate oxide will become so thin (<1.6 nm for SiO$_2$) that, due to excessive tunneling current, it would stop playing role of an insulator (Fig. 3 (a)). Hence, high-K dielectric, assuring same capacitive coupling but at the larger physical thickness of the film (Fig. 3 (b)), must be used instead of SiO$_2$ as a gate dielectric in advanced MOS/CMOS integrated circuits. These are to be discussed in detail below.
Fig. 2 Simplified cross-section of a high-k gate dielectric stack with accompanying physical gate length (Lg) and junction structures\textsuperscript{2}.

Fig. 3 (a) Leakage current vs. voltage for various thickness of SiO\textsubscript{2} layers\textsuperscript{3}, and (b) Schematic of direct tunneling through a SiO\textsubscript{2} layer and the more difficult tunneling through a thicker layer of high K oxide\textsuperscript{4}.
For device design, all FET dimensions scale proportionately and the precise material does not affect electrical designs (i.e. keep threshold voltage $V_T$ constant and then $C$ constant, assuming all other parameters equivalent), so it is convenient to define an ‘electrical thickness’ of the new gate oxide in terms of its equivalent silicon dioxide thickness or ‘equivalent oxide thickness’ (EOT) $^5$, which is to be discussed in detail below. The threshold voltage is,

$$V_T = V_{FB} + V_{T\text{ideal}}$$

where, $V_{FB}$ is the flat band voltage

$\Phi_{ms}$ is the work function difference

$\phi_F$ measures the position of the Fermi level below the intrinsic level $E_i$ for the semiconductor

$Q_i$ is the effective positive charge at the interface

$Q_d$ is the depletion region charge

$C_i$ is the capacitance of the insulator

To keep threshold voltage $V_T$ constant, we need to keep $C$ constant, assuming all other parameters equivalent. Since the devices are scaling down, which means $A$ going down, the thickness of SiO$_2$ $t_{\text{SiO}_2}$ should go down in order to keep the same $C$. If a high-K material is used to replace SiO$_2$, the corresponding thickness $t_{\text{SiO}_2}$ is called ‘equivalent oxide thickness’ (EOT). From the equation shown below, due to the larger value of $K$, a thicker high-K film
can be applied under the condition of same value of EOT. So the tunneling effect can be reduced or avoided.

\[
C_{\text{SiO}_2} = \frac{3.9 \text{A}}{t_{\text{SiO}_2}} \quad C_{\text{oxide}} = \frac{K \text{A}}{t_{\text{oxide}}}
\]

\[
t_{\text{SiO}_2} = \frac{EOT}{K / 3.9}
\]

EOT is a very important scaling parameter (Fig. 4). It is projected that high-K gate dielectric will be required by 2008 to control the gate leakage, according to the 2005 roadmap. As can be seen from the equation shown above, the EOT scaling can be achieved by simply decreasing \(t_{\text{oxide}}\) or increasing \(K\). However, \(t_{\text{oxide}}\) can not be decreased indefinitely due to the quantum tunneling effect as mentioned previously. Plus, \(K\) can not be increased unlimitedly; there is a trade off between \(K\) and the bandgap \(E_g\). All these issues are to be discussed in the next section.
2.1.2 La-based Oxides: LaScO$_3$ and La$_2$O$_3$/SiO$_2$ Alloy

Basically, there are 5 conditions that need to be met by a new high-K oxide (Table 1).
Table 1 Criteria for choices of high-K dielectrics

(Modified from the reference\textsuperscript{4})

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>High enough dielectric constant K</td>
</tr>
<tr>
<td>2</td>
<td>Band offsets (&gt; 1 eV)---wide band gap</td>
</tr>
<tr>
<td>3</td>
<td>Thermodynamic stability---no reaction with Si: Oxides with high heat of formation</td>
</tr>
<tr>
<td>4</td>
<td>Kinetic stability---stable up to 1000 °C for 10 sec.</td>
</tr>
<tr>
<td>5</td>
<td>Good interface quality---smooth interface and few defects</td>
</tr>
<tr>
<td>6</td>
<td>Few bulk electrically active defects</td>
</tr>
</tbody>
</table>

As pointed out previously, we expect to have a K value as high as possible in order to obtain a smaller EOT. However, the high-K thin layer also acts as an insulator. This requires that the band offsets between the high-K oxide and the Si substrate should be over 1 eV (Fig. 5). This limits the choice of oxide to those with band gaps over 5 eV, considering that the band alignment between high-K oxide and Si is usually asymmetric. In fact, there is a trade off between K values and bandgaps (Fig. 6). So the K values are in the range of 20-30. It is interesting to notice that the over 5 eV requirement is consistent with the criterion 3 about thermodynamic stability. This is reasonable because a high heat of formation for an oxide, which means thermodynamically stable with the Si substrate, correlates with a wide band gap, in ionic compounds. The first three criteria listed in Table 1 limit the choices to HfO\textsubscript{2}, La\textsubscript{2}O\textsubscript{3}, and LaAlO\textsubscript{3} (Table 2).
Fig. 5 Schematic of band offsets determining carrier injection into oxide band states.

Fig. 6 Static dielectric constant vs. band gap for candidate gate oxides$^6$
Table 2 Candidate gate dielectrics on Si

<table>
<thead>
<tr>
<th></th>
<th>K</th>
<th>Gap (eV)</th>
<th>CB offset (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiO₂</td>
<td>3.9</td>
<td>9</td>
<td>3.2</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>7</td>
<td>5.3</td>
<td>2.4</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>9</td>
<td>8.8</td>
<td>2.8 (not ALD)</td>
</tr>
<tr>
<td>Ta₂O₅</td>
<td>22</td>
<td>4.4</td>
<td>0.35</td>
</tr>
<tr>
<td>TiO₂</td>
<td>80</td>
<td>3.5</td>
<td>0</td>
</tr>
<tr>
<td>SrTiO₃</td>
<td>2000</td>
<td>3.2</td>
<td>0</td>
</tr>
<tr>
<td>ZrO₂</td>
<td>25</td>
<td>5.8</td>
<td>1.5</td>
</tr>
<tr>
<td>HfO₂</td>
<td>25</td>
<td>5.8</td>
<td>1.4</td>
</tr>
<tr>
<td>HfSiO₄</td>
<td>11</td>
<td>6.5</td>
<td>1.8</td>
</tr>
<tr>
<td>La₂O₃</td>
<td>30</td>
<td>6</td>
<td>2.3</td>
</tr>
<tr>
<td>Y₂O₃</td>
<td>15</td>
<td>6</td>
<td>2.3</td>
</tr>
<tr>
<td>α-La₂O₃</td>
<td>30</td>
<td>5.6</td>
<td>1.8</td>
</tr>
</tbody>
</table>

With modern film growth methods, it is easy to get structurally straight interface. However, the interface defect is an important issue. It is believed that there are basically two ways to ensure a high quality interface, either by using an amorphous oxide or using an epitaxial oxide on the Si. Polycrystalline oxides generally are not considered mainly due to the problems associated with grain boundaries. Although their dielectric constants and bandgaps are found to be slightly lower than their corresponding single crystalline phases, amorphous oxide films are the lowest cost solution. Epitaxial oxide films are thought to be the long term solution. However, current research indicates that there are still a lot of issues
to be solved about epitaxial oxide films on Si\textsuperscript{7-9}. So in this study, we just considered the case of amorphous films on Si (001).

As pointed out before, the high-K oxides are now narrowed down to HfO\textsubscript{2}, La\textsubscript{2}O\textsubscript{3}, and LaAlO\textsubscript{3}. However, the problems of making HfO\textsubscript{2} into a successful electronic materials appeared extremely high\textsuperscript{4}. As far as kinetic stability is concerned, unfortunately, all the high-K candidates crystallise well below 1000 °C. This problem can be circumvented by “alloying” with other oxides such as Al\textsubscript{2}O\textsubscript{3}, SiO\textsubscript{2}, and Sc\textsubscript{2}O\textsubscript{3}, as shown below.

\[
\begin{align*}
\text{La}_2\text{O}_3 + \text{Al}_2\text{O}_3 &\rightarrow \text{LaAlO}_3 \\
\text{La}_2\text{O}_3 + \text{SiO}_2 &\rightarrow \text{La}_{4-4x/3}\text{Si}_x\text{O}_6 \\
\text{La}_2\text{O}_3 + \text{Sc}_2\text{O}_3 &\rightarrow \text{LaScO}_3 (K=30, E_g=6.0)
\end{align*}
\]

So essentially, all the high-K dielectrics are La\textsubscript{2}O\textsubscript{3}-based so far. In fact, La-based high-K gate oxides are attracting more and more attention due to their potential possibility as good gate dielectrics\textsuperscript{10}. In this study, we just considered amorphous La\textsubscript{2}O\textsubscript{3}/SiO\textsubscript{2} alloy and LaScO\textsubscript{3} on Si substrates. It needs to point out that the La\textsubscript{2}O\textsubscript{3}/SiO\textsubscript{2} alloy film was grown in a different way from that of LaScO\textsubscript{3} film, although the molecular beam deposition (MBD) method was used for both cases. This will be discussed specifically in the late section. LaAlO\textsubscript{3} was not considered, mainly because the sample was found to have a SiO\textsubscript{2} interfacial layer with the Si substrate, which greatly increases the equivalent oxide thickness (EOT).
The electrically active defects in the oxide film give rise to electronic states in the bandgap of the oxide, which degrade the device performance. This and other issues are to be introduced in detail in the next section.

2.1.3 Materials Science Issues with High-K oxides

There are many challenges reported in literature in replacing SiO$_2$ with a high-K dielectric for high-performance CMOS (Table 3), especially when poly-Si is applied.

**Table 3** Problems with High K oxides

(Modified from the reference$^4$)

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>How to reach EOT &lt;1 nm---An interfacial layer (K&lt;9) often formed</td>
</tr>
<tr>
<td>2.</td>
<td>Threshold voltage $V_T$ shifts---Flat band voltages shifted from CMOS standards</td>
</tr>
<tr>
<td>3.</td>
<td>Carrier Mobility below expectation---Below Universal mobility model</td>
</tr>
<tr>
<td>4.</td>
<td>Oxide has too many charge traps---Not glassy like SiO$_2$</td>
</tr>
</tbody>
</table>

An interfacial layer of SiO$_2$ often exists between the high-K oxide layer and the Si substrate. There are advantages and disadvantages for this, as long as its presence and thickness can be controlled. Obviously, the interfacial layer adds to the overall EOT. However, the electrical quality of the Si-oxide interface can be improved because the Si-SiO$_2$ interface is of high-quality, although the interfacial layer may not have the same quality as SiO$_2$ produced by thermal oxidation of Si$^{11,12}$.  

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As seen from the threshold voltage $V_T$ equation in section 2.1.1, $V_T$ is a function of the interface charge $Q_i$. High-K oxides have a large defect density, which causes the $V_T$ shift. However, some tests\textsuperscript{13} suggest that the origin could be the interaction of the poly-Si gate and the high-K gate oxide.

The mobilities in devices with high-K gate dielectrics presently lie well below the universe mobility curve\textsuperscript{14-16}. The causes are not well understood. There are two likely causes, the charge scattering due to the oxide trapped charge and interface states\textsuperscript{17}, and the remote scattering due to the low-lying polar lattice vibration modes of high-K oxides\textsuperscript{18}.

High-K oxides usually possess a larger bulk density of defects and trapped charge than SiO$_2$\textsuperscript{19}. The bulk defects and trapped charge can cause $V_T$ shift, device unreliability, and the mobility reduction.

According to the International Technology Roadmap for Semiconductors (ITRS) 2005, it is projected that high-K gate dielectric will be required by 2008 to control the gate leakage and the solutions for EOT below 1.0 nm are not understood. So we tried to study the interface structures of high-K dielectrics on Si (001) substrates with many TEM/STEM techniques, so that we can have a deeper understanding about these new high-K dielectrics.

### 2.2 GaN-based Systems

#### 2.2.1 Historical Development of III-nitride Semiconductors

Here we give a brief historical development of III-nitrides to show clearly why these so important materials had not been used to make useful devices until the early 1990s. The development can be grouped into four phases\textsuperscript{20}.
In phase I (1900-1960s), no significant progress were made, although AlN, GaN, and InN were synthesized as early as 1907, 1910, and 1932, respectively, much earlier than conventional GaAs and Si. The main reason is the difficulty to synthesize these materials.

Phase II (1960-1970s) is mainly about the epitaxial growth of GaN (or AlN) thin film with hydride phase epitaxy (HVPE), metalorganic chemical vapor deposition (MOCVD) and then molecular beam epitaxy (MBE). However, the quality of GaN films on non-native substrates was very poor.

During phase III (1980s), there were two fundamental breakthroughs, the concept of a low temperature (LT) nucleation layer which allows the growth of smooth GaN thin films on a non-native substrate\(^2\), and the demonstration of p-type GaN films through low-energy electron beam irradiation (LEEBI)\(^2\) or thermal annealing\(^3\).

Phase IV (1990-today) has seen the most dramatic and spectacular research and development work such as the commercialized GaN-based blue LEDs, long life GaN-based laser diodes\(^4\), AlGaN/GaN high-electron mobility transistors (HEMTs)\(^5\), UV photodetectors\(^6\), and “Blu-ray Disc”. It should be noticed that one important film growth method called “Lateral Epitaxial Overgrowth” was developed in this phase, which can reduce dislocation density in heteroepitaxial grown GaN\(^7\). In this study, we used the concept of LT-AlN nucleation layer, together with the “Lateral Epitaxial Overgrowth” technique to grow GaN films on sapphires.
2.2.2 Figures of Merit of GaN

As mentioned before, GaN has a wurtzite structure (Fig. 7). This structure makes GaN have different properties from other semiconductor materials such as Si, SiC, and GaAs (Table 4).

Fig. 7 GaN: new symmetry, new properties (shown are diamond structure [111], zinc blende structure [111], and wurtzite structure [0001])..

Table 4 Properties of commonly used semiconductor materials

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Si</th>
<th>GaAs</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Gap (eV)</td>
<td>1.11</td>
<td>1.43</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Breakdown E-Field (V/cm)</td>
<td>6.0\times10^9</td>
<td>6.5\times10^9</td>
<td>3.5\times10^8</td>
<td>3.5\times10^8</td>
</tr>
<tr>
<td>Saturation Velocity (cm/s)</td>
<td>1.0\times10^7</td>
<td>2.0\times10^7</td>
<td>2.0\times10^7</td>
<td>2.5\times10^7</td>
</tr>
<tr>
<td>Electron Mobility (cm²/V-s)</td>
<td>1350</td>
<td>6000</td>
<td>800</td>
<td>1500</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cmK)</td>
<td>1.5</td>
<td>0.46</td>
<td>3.5</td>
<td>1.7</td>
</tr>
<tr>
<td>Heterostructures</td>
<td>SiGe/Si</td>
<td>AlGaAs/GaAs</td>
<td>None</td>
<td>AlGaN/GaN</td>
</tr>
<tr>
<td></td>
<td>InGaP/GaAs</td>
<td>AlGaAs/InGaAs</td>
<td>AlGaN/GaN</td>
<td></td>
</tr>
</tbody>
</table>

* Typical two-dimensional electron gas mobility for AlGaN/GaN heterostructures.

Ricardo Borges, nitronex
Two figures of merit are generally used to characterize materials for electronic devices. The first one is the Johnson figure of merit (JFM),

$$\text{JFM} = \left( \frac{E_m V_s}{2\pi} \right)^2$$

where, $E_m$ is the breakdown voltage and $V_s$ is the saturation velocity.

The second one is the Keyes figure of merit (KFM),

$$\text{KFM} = \sigma_T \left( \frac{c V_s}{2\pi \varepsilon} \right)^{1/2}$$

where, $\sigma_T$ is the thermal conductivity, $c$ is the light speed, and $\varepsilon$ is the dielectric constant.

The values of the JFM and KFM for different materials are listed in Table 29, confirming that GaN-based semiconductors are very promising for high-temperature, high-power, and high-frequency electronic devices.

**Table 5** Values of JFM and KFM for different materials

(Normalized to Si)

<table>
<thead>
<tr>
<th>Materials</th>
<th>Si</th>
<th>GaAs</th>
<th>GaN</th>
<th>6H-SiC</th>
<th>3C-SiC</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFM</td>
<td>1</td>
<td>7.1</td>
<td><strong>2029</strong></td>
<td>712</td>
<td>712</td>
<td>8117</td>
</tr>
<tr>
<td>KFM</td>
<td>1</td>
<td>0.45</td>
<td><strong>1.6</strong></td>
<td>5.2</td>
<td>5.2</td>
<td>32.1</td>
</tr>
</tbody>
</table>
In summary, gallium nitride’s great boom is that it combines the high breakdown field of silicon carbide with the high-frequency characteristics of gallium arsenide, silicon-germanium, or indium phosphide.

2.2.3 GaN-Based Transistors and GaN Inversion Domain Boundary (IDB)-Based Devices

As mentioned before, GaN and its alloys are very promising in make high quality optoelectronic and electronic devices. Here we just focus on the GaN-based transistors, which make it easier to see the differences when compared with conventional Si-based transistors. Also studied are the potential GaN-IDB-based devices which make use of the polarity of GaN.

2.2.3.1 GaN-based Transistors

The electron mobility in GaN is lower than that in GaAs, but the saturation velocity, $V_s$ ($\sim 1.3 \times 10^7$ cm/s), is equivalent and should reach $2 \times 10^7$ cm/s in the next few years. There is an unusual phenomenon of GaN when AlGaN is grown on top of a GaN layer. An electrically charged region is formed in the immediate vicinity of the heterojunction due to spontaneous electrical polarization within the crystal and piezoelectric polarization caused by lattice mismatch. This will be discussed further when GaN IDB is introduced. These combined polarizations, in turn, induce an excess of free-moving electrons in the GaN. So a 2DEG spontaneously forms near the polarization region, hard against the AlGaN but without straying into it because the material’s higher bandgap acts as a barrier. This phenomenon is a major contributor to gallium nitride’s outstanding high-frequency characteristics. Based on this phenomenon, GaN-FETs can be fabricated (Fig. 8), even without doping.
The GaN-based transistors are capable of handling frequencies and power levels well beyond those possible with Si, GaAs, or SiC (see Table 6). And frequency and power-handling capabilities of GaN transistors could make all the difference in the amplifiers, modulators, and other key components of the advanced communications networks. Nor does heat bother gallium nitride much. Researchers at Astralux tested a GaN transistor at a temperature of 300 °C and found that it amplified very well. In contrast, silicon transistors stop working at about 140 °C. The result bodes well for the use of GaN electronics in engines, satellites, and other hot environments. GaN’s success in LEDs and laser in recent years helped direct attention to work on high-power, high-frequency GaN transistors. Broadband wireless networks, ubiquitous hybrid electric vehicles, sophisticated controllers for electric grids, and compact, rugged radars have made plenty of promises in recent years.
Table 6 The power-and frequency-handling capabilities of different transistors

(Modified from reference\textsuperscript{30})

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Power (W/mm)</th>
<th>Frequency (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN-based</td>
<td>&gt;10</td>
<td>10</td>
</tr>
<tr>
<td>Si-based</td>
<td>--</td>
<td>&lt;2-3</td>
</tr>
<tr>
<td>SiC-based</td>
<td>7.2</td>
<td>&lt;3.5</td>
</tr>
<tr>
<td>GaAs-based</td>
<td>&lt;1</td>
<td>10</td>
</tr>
<tr>
<td>SiGe-based</td>
<td>&lt;1</td>
<td>10 (or higher)</td>
</tr>
</tbody>
</table>

2.2.3.2 GaN Inversion Domain Boundary (IDB)-Based Devices

III-nitrides are essentially ionic solids with a strong charge transfer between N atoms and III-atoms due to the different electronegativity. This gives rise to a macroscopic spontaneous polarization $P$ opposite to the c-direction of the wurtzite crystal lattice (Fig. 9). The $P$ values of AlN, GaN, and InN, are 0.09, 0.034, and 0.042 C/m\textsuperscript{2}, respectively. In other words, the corresponding fixed surface charge is in the order of $10^{13}$-$10^{14}$ e/cm\textsuperscript{2}. This large $P$ value gives rise to the large internal electric field $E$, in the order of $10^6$-$10^7$ V/cm. In practice, the macroscopic polarization also includes piezoelectric polarization mainly due to the lattice mismatch. For the Ga-face side, the polarization-induced fixed lattice charges are negative at the surface and positive at the substrate interface, the crystallographic c-axis and the internal electric field point away from the substrate towards the surface whereas the polarization has
the opposite direction, and the compensating surface charge is positive. For the N-face side, the opposite is true.

Fig. 9 Directions of c-axis, \( P \), and \( E \). Also shown are the polarization-induced terminating fixed charges, the compensating surface charges due to adsorbed ions, and the inversion domain boundary (IDB) \(^{31}\).

Also seen is the inversion domain boundary (IDB) separating adjacent domains of different polarity\(^ {32}\). In this study, we tried to invert the polarity by using a LT-AlN nucleation layer (Fig. 10). The different polarity between the right side and left side comes from the different chemical strengths of the III-N versus the III-O bonds (Ga-N > Ga-O, Al-N < Al-O). Here is just a simplified view of the structure of this specific case. In practice, not much is known about the real structure. This is one main part of this study.
With the new degree of freedom from polarity, a lot of novel optical or electronic devices have been tried or proposed based on the simple lateral polarity heterostructures (LPHs) (Fig. 11). In the ideal case of defect free IDBs and no surface charge compensation, the lateral band alignment is expected to be the one shown in Fig. 11. For the N-face material, the positive polarization-induced fixed charges give rise to an electron accumulation layer at the free surface, fixing the Fermi level close to the conduction band edge. The opposite is true to the Ga-face material. So basically, the structure is like a p-n junction. In practice, however, the situation is more complex. Even so, many interesting electronic and optical properties have been observed from devices based on LPHs, including the rectifying behavior of IDBs\textsuperscript{31}, the strong recombination at the IDBs\textsuperscript{33}, and the lateral tunnel diode\textsuperscript{31}.

**Fig. 10** Simplified schematic view of the III-nitride/sapphire interface and the GaN IDB\textsuperscript{31}.
2.2.4 Materials Science Issues on GaN-based Devices

Even with so many advantages, GaN transistors are not ubiquitous. This is because, fundamentally, no inexpensive substrate material for gallium nitride exists. Ideally, the substrate and the lower layers of the device are made of the same material to avoid lattice mismatch problem, which can seriously degrade device performance. Unfortunately, no gallium nitride wafers are available until now. So today GaN devices are fabricated on substrates of sapphire, silicon carbide, or even silicon\textsuperscript{27,34}.

Silicon carbide is a fairly good match for gallium nitride—the crystal lattices of the two compounds are mismatched by only 3.3 % (the figure for sapphire and gallium nitride is...
13.29 %; the mismatch is worse for silicon and gallium nitride, 16.96 %) (Table 7). Also, silicon carbide is an even better conductor of heat than gallium nitride (Table 8). However, SiC wafer is still very expensive. Si remains a desirable choice because it is the most widely used electronic materials and is widely available in large areas at much lower price. However, it does not have a crystal structure and physical properties similar to GaN, and the lattice mismatch is large. Sapphire offers a compromise between these two extremes as high-quality sapphire wafer are widely available and are cheaper than SiC, and sapphire has a similar hexagonal crystal structure as GaN. So today sapphire is the most commonly used one as the GaN substrate.
Table 7 Lattice parameters and energy gaps of potential substrate materials for GaN

<table>
<thead>
<tr>
<th>Materials</th>
<th>Lattice parameters (Å)</th>
<th>Plane with nearest match with GaN (0001)</th>
<th>Effective a lattice constant (Å)</th>
<th>Lattice mismatch with GaN (%) ((a_{GaN}-a_{sub})/a_{sub})</th>
<th>Energy gap (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN (hexagonal)</td>
<td>(a=3.1891) (c=5.1855)</td>
<td>(0001)</td>
<td>3.1891</td>
<td>0</td>
<td>3.44</td>
</tr>
<tr>
<td>AlN (hexagonal)</td>
<td>(a=3.112) (c=4.982)</td>
<td>(0001)</td>
<td>3.112</td>
<td>2.47</td>
<td>6.2</td>
</tr>
<tr>
<td>(\text{Al}_2\text{O}_3) (trigonal)</td>
<td>(a=4.758) (c=12.991)</td>
<td>(0001) rotated 30°</td>
<td>2.747</td>
<td>13.29</td>
<td>&gt;8.5</td>
</tr>
<tr>
<td>4H-SiC (hexagonal)</td>
<td>(a=3.073) (c=10.053)</td>
<td>(0001)</td>
<td>3.073</td>
<td>3.77</td>
<td>3.20</td>
</tr>
<tr>
<td>6H-SiC (hexagonal)</td>
<td>(a=3.081) (c=15.117)</td>
<td>(0001)</td>
<td>3.081</td>
<td>3.51</td>
<td>2.86</td>
</tr>
<tr>
<td>Si (cubic)</td>
<td>(a=5.431)</td>
<td>(111)</td>
<td>3.840</td>
<td>-16.96</td>
<td>1.12</td>
</tr>
</tbody>
</table>
Table 8 Thermal properties of potential substrate materials for GaN

<table>
<thead>
<tr>
<th>Materials</th>
<th>Thermal expansion coefficient or TEC $\alpha$ $(10^{-6} \text{K}^{-1})$</th>
<th>Mismatch with GaN by cooling 1000°C (%) $(\text{TEC}<em>{\text{GaN}}-\text{TEC}</em>{\text{sub}}) \times (-1000K)$</th>
<th>Thermal conductivity (W/cm.K)</th>
<th>Melting point ($^\circ$C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN</td>
<td>5.6 (0-600°C)</td>
<td>0</td>
<td>1.7-1.8</td>
<td>&gt;1700</td>
</tr>
<tr>
<td>AlN</td>
<td>5.7</td>
<td>0.01</td>
<td>2.0</td>
<td>3000</td>
</tr>
<tr>
<td>$\text{Al}_2\text{O}_3$</td>
<td>8.6</td>
<td>0.30</td>
<td>0.3</td>
<td>2015</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>4.46</td>
<td>-0.11</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>4.44</td>
<td>-0.12</td>
<td>4.9</td>
<td>--</td>
</tr>
<tr>
<td>Si</td>
<td>3.90</td>
<td>-0.17</td>
<td>1.3</td>
<td>1412</td>
</tr>
</tbody>
</table>

Due to the large lattice and thermal mismatches between GaN epitaxial layer and the sapphire substrate, it is not easy to get crack-free GaN film grown directly on sapphire substrate (dislocation density $> 10^{11} \text{cm}^{-2}$). Moreover, the high residual electron concentration ($>10^{19} \text{cm}^{-3}$) in GaN and the high activation energy of Mg dopants made it quite difficult to achieve p-type conduction and to control the conductivity of n-type GaN. These problems were greatly solved by applying the concept of LT-ALN nucleation layer\textsuperscript{35} and annealing. However, the GaN grown on a sapphire substrate with the LT-ALN nucleation layer still contains dislocations, as many as $10^{8}$-$10^{10} \text{ cm}^{-2}$. Even these dislocations do not introduce impurity states in the bandgap, they are considered to be a major cause of the degradation of device performance. By applying the concept of epitaxial lateral overgrowth (ELO)\textsuperscript{36}, the dislocation density can be reduced to the order of $10^{7} \text{cm}^{-2}$. 

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To further solve the dislocation and other defect related problems with GaN films, it is very important to know what happens at the interface between GaN (or LT-AlN) and c-sapphire. In this study, we aim to determine these interface structures and GaN IDBs.

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3. EXPERIMENTAL METHODS

3.1 Film Growth Methods

Modern solid state devices require high quality film growth methods. Molecular beam epitaxy (MBE) (or called molecular beam deposition (MBD) when applied to grow amorphous films), and metal organic chemical vapor deposition (MOCVD) (or called metalorganic vapor phase epitaxy (MOVPE) when applied specifically to grow epitaxy films) meet this requirement. Both methods can give high quality films at low growth rate, atomically sharp interfaces, and can grow far from equilibrium systems reliably, although they are “expensive” growth techniques which require great care. In this study, MBD is applied for growing amorphous high-K dielectrics on Si (001) substrates, and MOVPE for GaN epitaxy on sapphire substrate with/without low temperature (LT) AlN nucleation layer. Here we briefly introduce both film growth methods.

3.1.1 Molecular Beam Deposition (MBD)

Molecular beam epitaxy (MBE) film growth system (see Fig. 1) can also be used to grow amorphous film on substrates at low temperature. Here comes the name of molecular beam deposition (MBD). MBD is a high vacuum (up to $10^{-11}$ torr) system. Due to the low background pressure, the reflection high energy electron diffraction (RHEED) technique is applied to monitor the growing films. The chamber walls are usually liquid-N$_2$ cooled to ensure high vacuum and to prevent dirt to come off from the chamber wall. When a crucible is heated, atoms or molecules are evaporated from single element in the crucible and then...
impinge on the heated substrate. The shutters allow one to change the composition of the growing film. The film growth rate is ~1.0 monolayer per second.

**Fig. 1** Schematic diagram of the MBD system (modified from reference\(^1\)).

3.1.2 **Metal Organic Vapor Epitaxy (MOVPE)**

MOVPE is an important growth technique widely used for heteroepitaxy. A typical MOVPE system is shown in Fig. 2. Chemical reaction occurs on the heated substrate and mass flow controllers control the species deposited.
Fig. 2 schematic diagram of the MOCVD system (modified from reference1).

In Table 1, we compare the differences of these two film growth methods. However, it is possible to have hybrid epitaxial techniques called MOMBD (metal organic MBD) or MOMBE (metal organic MBE), combining the best of MBD and MOVPE.
Table 1 Differences between MBD and MOVPE

<table>
<thead>
<tr>
<th></th>
<th>MBD</th>
<th>MOVPE</th>
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<tbody>
<tr>
<td>Vacuum</td>
<td>UHV</td>
<td>Atmospheric or low pressure</td>
</tr>
<tr>
<td>Precursors</td>
<td>Elements</td>
<td>Complex molecules</td>
</tr>
<tr>
<td>Chemical reaction</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Local area growth</td>
<td>Hard</td>
<td>Easy</td>
</tr>
<tr>
<td>Safe issue</td>
<td>Non-toxic</td>
<td>Toxic</td>
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3.2 Atomic-scale Characterization Techniques

As device sizes shrinking, atomic-scale characterization techniques are required. A modern TEM/STEM meets this requirement. Different experimental characterization techniques are discussed in this section. All the experimental data were acquired from the TEM/STEM JEOL2010F (NCSU) and the aberration-corrected STEM VG-501HUX (ORNL). Also, to exactly determine the atomic structures of interfaces, \textit{ab initio} calculations need to be done. Density functional theory (DFT) based \textit{ab initio} calculation is playing an important role in materials science. The computer package VASP is used for running the calculations with the help of Materials Studio to construct the initial atomic models.

3.2.1 High Resolution Transmission Electron Microscopy (HRTEM) Imaging

The features seen in a TEM image can come from scattering contrast (also called mass-thickness contrast, important for amorphous specimens), diffraction contrast (important for crystalline specimens), or phase contrast (for all specimens). Here we just focus on the later
case. The phase contrast originates from the interference between electron waves that have passed through different regions of the specimen, due to the phase difference of the electron waves. Such electrons can be imaged by defocusing the objective lens. Unlike the case of diffraction-contrast images, no objective aperture (or a large one) is used to enable several diffracted beams to contribute to the image. The Fresnel fringe inside a circular hole is sometimes used as a guide to adjust the objective-lens stigmator. Often times, the fast Fourier transform (FFT) is applied to do this correction when imaging an amorphous region. This can be easily realized, for example, on the JEOL2010F with a GIF system.

When a crystalline specimen is tilted on its zone axes and irradiated by a parallel electron beam, the phase contrast in high magnification (>250kx) images allows the lattice of atoms to be seen directly. The electron-wave explanation is that the electrons traveling down the center of an atom column have their phase retarded relative to those that travel in between atom columns, which causes the phase difference and then phase contrast. However, the basic effect can be also be understood by treating the electrons as particles (see Fig. 3).
The nuclei of the atoms elastically scatter the electrons through angles that depend inversely on the impact parameter of each electron. The impact parameter is defined as the distance of closest approach to the nuclei. The parallel beam provides a continuous range of impact parameter. Due to the scattering, the electron current density appears non-uniform at planes above and below the atom plane. If the objective lens is focused on the atom plane, the uniform illumination will ensure no image contrast. If we overfocus slightly the objective lens, the TEM will image a plane below the specimen, where the electrons are more numerous at the positions vertically below the atom positions (see Fig. 3). So the atoms appear bright relative to their surroundings in the final image. The opposite is true when the objective image is underfocused. The optimum amount of defocus ($\Delta z$) is about 20nm for a typical TEM. For the interpretation of phase-contrast images, it requires that one knows the spherical-aberration coefficient of the objective lens and the amount of defocus ($\Delta z$).
practice, this is done by recording a through-focus series of HRTEM images with positive and negative $\Delta z$ and carrying out image simulation. HRTEM images are particularly valuable for examining the interface atomic structure within a solid (see Fig. 4).

Fig. 4 HRTEM image of amorphous LaAlO$_3$ on Si (001)

3.2.2 Z-contrast Imaging and Electron Energy Loss Spectroscopy (EELS)

Most scanning transmission electron microscopy (STEM) images are recorded in dark-field mode, using an annular dark-field (ADF) detector located close to the specimen. The detector is similar to a Robinson or solid-state backscattered electron (BSE) detector used in the scanning electron microscope (SEM), but it collects electrons that are transmitted through the specimen and scattered within a certain angular range ($\theta_{\text{min}}$ and $\theta_{\text{max}}$) (Fig. 5). By making
\( \theta_{\text{min}} \) large, the so-called \( Z \)-contrast images can be formed. Simultaneously, by fitting an energy-loss spectrometer, an EELS spectrum can be formed from electrons (with scattering angle up to \( \theta_{\text{min}} \)) that pass through the central hole of the annular detector.

**Fig. 5** Simplified \( Z \)-contrast imaging and EELS setup. Courtesy of Gerd Duscher, NCSU.

### 3.2.2.1 \( Z \)-Contrast Imaging

When \( \theta_{\text{min}} \) is large enough, only large-angle (mainly elastic) scattering is collected. Its intensity is approximately proportional to \( Z^2 \) (\( Z \)=atomic number). There comes the so-called \( Z \)-contrast imaging. Therefore, the \( Z \)-contrast image contains strong atomic-number contrast and not much diffraction contrast (most of the diffracted electrons have a scattering angle...
less than $\theta_{\text{min}}$ and pass through the central hole of the annular detector). So it is seen that the region with higher atomic number appears brighter in a Z-contrast image.

To a dedicated STEM with a field-emission source and a strongly excited objective lens (low coefficient of spherical aberration, $C_s$), the probe size can be less than 1 Å. In fact, it can form a Z-contrast image with resolution of $\sim$0.6 Å$^2$. Unlike the phase-contrast HRTEM imaging, the annular detector provides an amplitude (scattering-contrast) signal that is relatively insensitive to the objective-lens focus; there are no contrast reversals and the image is more directly interpretable in terms of atomic coordinates$^3$. So direct sub-angstrom imaging of a crystal lattice is possible now.

3.2.2.2 Electron Energy Loss Spectroscopy (EELS)

Electron energy-loss spectroscopy (EELS) $^4$ is to perform spectroscopy on the primary electrons that have passed through a thin TEM specimen. To accurately measure the energy loss, a magnetic prism is applied to disperse (and focus) the electron beam, according to the simple physical relation,

$$e v B = \frac{m v^2}{R}$$

where $e$ is the electron charge, $B$ is the magnetic field, $v$ is the electron speed, $m$ is the electron relativistic mass, and $R$ is the radius of the circle arc that an electron moves along.

The schematic structure of a parallel-recording EELS (PEELS) spectrometer is shown in Fig. 6. The QX, QY, SX, and SY lenses are used for EELS alignment. The drift tube,
together with energy shift, is adjusted for energy dispersion calibration. The dispersion is magnified by lenses Q1-Q4. The thin YAG scintillator converts the electron-intensity distribution to a photon-intensity distribution which is imaged through a fiber-optic window onto a photodiode or CCD camera cooled to ~20°C. The recorded images can then be converted to EELS spectra.

**Fig. 6** Parallel-recording EELS (PEELS) spectrometer mounted below the viewing screen of a TEM/STEM. Courtesy of Ondrej Krivanek and Gatan Inc.

A typical EELS spectrum (Fig. 7) contains 3 parts. The zero-loss (ZL) peak represents electrons that were scattered elastically or remained unscattered while passing through the specimen. The plasmon peak(s) represents inelastic scattering by outer-shell (valence or
conduction) electrons in the specimen. In the low-loss region (<50 eV), the intensity of the plasmon peak relative to the zero-loss peak can be used to measure the local thickness, since the amount of inelastic scattering is proportional to the specimen thickness in a single-scattering approximation. The core loss part contains the ionization edge(s) which is due to the inelastic excitation of inner-shell electrons at an energy loss equal to an inner-shell ionization energy. So the energy of each ionization edge indicates which elements are present within the specimen. Also, the energy-loss intensity can be integrated over a region of about 50-100 eV after background subtraction to give a signal $I_A$ that is proportional to the concentration of the element A that gives rise to the ionization edge. The atomic ratio of two different elements (A, B) can calculated with the equation,

$$\frac{n_A}{n_B} = \frac{I_A \sigma_B}{I_B \sigma_A}$$

where $\sigma$ is the ionization cross section that can be calculated as a function of the atomic number, type of shell, and the integration range used for each element.

In this study, instead of using the above equation directly, we use a modified quantification approach developed by Gerd Duscher with a spreadsheet solver and macros. Instead of integrating for $I_A$ or $I_B$, a fit function (as function of the background, a polynomial, and the cross sections) is applied to least-square fit the EELS spectrum. Also, from the fine structure in the low loss region and the ionization edges, detailed information about the atomic arrangement and chemical bonding can be inferred. For example, the intensities of the
two sharp peaks (also called white lines) at the onset of the transition-metal (for example, La and Sc) edges can be used to determine the oxidation state (valency) of the atoms.

**Fig. 7** EELS spectrum with the different parts indicated (adapted from MSE 791C class notes by Gerd Duscher, NCSU, spring, 2006).

In this study, we studied the EELS core losses to determine the chemical composition and chemical bonding information about the amorphous high-K materials on silicon.
3.2.3 Convergent Beam Electron Diffraction (CBED)

Unlike conventional selected area electron diffraction (SAED) technique which uses a parallel beam and relies on elastic scattering, convergent beam electron diffraction (CBED) uses a convergent beam of electrons to the relatively thick area of the specimen which contributes to the diffraction pattern and contains inelastic scattering information also (Fig. 8).

Fig. 8 Schematic of a CBED pattern formation (modified from 1999 MATTER, The University of Liverpool)
In thick area, inelastically scattered electrons travel in all directions although their distribution peaks in a forward direction. Because the electrons are inelastically scattered in all directions, the diffracted electrons will form a cone when Bragg diffraction condition is met. Hence we observe Kikuchi lines. Fig. 8 shows how a pair of Kikuchi lines are formed, one excess line and one deficit line. So each disc containing variations in intensity can usually be seen. In fact, due to dynamic effect, such patterns contain a wealth of information about the symmetry and thickness of the crystal and are widely used in TEM. In this study, we use CBED to study the polarity change of the GaN film on c-sapphire. Also simulated CBED patterns are compared with experimental ones so that both the polarity and thickness information can be determined locally (see Fig. 9).
Fig. 9 Experimental and simulated CBED patterns. Clearly shown is the opposite polarity at two different regions.

3.2.4 Density Functional Theory (DFT) Based *ab initio* Calculation

In principle, to calculate properties of the solid state, one must solve the Schrödinger (or Dirac) equation for an enormous number of interacting particles. Since it is not possible to solve this equation analytically for a many-body system, one has to find numerical schemes. However, even modern numerical techniques for solving such differential equations
are impossible. Therefore, one has to find some approximation methods. The Born-Oppenheimer approximation is the one often applied, where the nuclei are thought to have fixed positions since the mass of the atomic nuclei is at least three orders of magnitude larger than the mass of the electrons. So the problem is now simplified to solve the electron problem.

So far the most successful and most often used technique to solve the many electron problems is based on the density-functional theory (DFT), which is mainly developed by Hohenberg, Kohn, Sham, and other contributors. The first main idea of DFT is to describe an interacting system of electrons via its electron density \( n(r) \) and not via its many-body wave function; all ground-state properties are functions of the ground-state electron density \( n(r) \). For \( N \) electrons in a solid, which obey the Pauli principle and repulse each other via the Coulomb potential, this means that the basic variable of the system depends only on three -- the spatial coordinates \( x, y, \) and \( z \) -- rather than \( 3^N \) degrees of freedom. This greatly simplifies the problem. The second main idea of DFT says that the ground-state total energy function is minimal for the correct ground-state density with respect to all densities leading to the correct number of electrons. This principle allows the ground state density to be determined as long as the ground-state total energy function is known. However, the exact expression for the total energy function is unknown to a complicated many-body problem. So many approximation methods have been developed for the total energy function, especially for the exchange-correlation energy. Nowadays, the most widely used approximation is the local density approximation (LDA) or its spin-dependent version, the local spin density approximation (LSDA). In this approximation the exchange-correlation energy is chosen to
be at every point $\vec{r}$ the exchange-correlation potential of a free electron-gas with a uniform density of $n(\vec{r})$. The exchange-correlation energy is then no longer a functional of the density but just a function. The approximation also performs reasonably well for a slowly varying density $n(\vec{r})$. However, experience has shown that this approximation works well even for systems which have very inhomogeneous electron densities.

In practice, the computer simulation package VASP is widely used for running calculations. It is a complex package for performing *ab-initio* quantum-mechanical molecular dynamic (MD) calculations using pseudopotentials and a plane wave set$^{10}$. The approach implemented in VASP is based on the LDA with the free energy as the variational quantity and an exact evaluation of the instantaneous electron ground state at each MD-step using efficient matrix diagonalization schemes and an efficient Pulay$^{11}$ charge density mixing. The interaction between ions and electrons is described using ultrasoft Vanderbilt pseudopotentials (US-PP) or the projector augmented wave method (PAW). Both techniques allow a considerable reduction of the necessary number of plane-waves per atom for transition metals and first row elements. Generally not more than 100 plane waves per atom are required to describe bulk materials. In this study, VASP is applied to simulate the interface structure of AlN on sapphire. Different models of the interface structure were set up and compared with the Z-contrast images got from the interface so that the right interface structure was determined.
References


4. RESULTS AND DISCUSSIONS

4.1 LaScO$_3$ on Si (001)

(This part was adapted from a paper to be submitted to Journal of Applied Physics)

The Interface Structure of LaScO$_3$ on Si (001)

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ABSTRACT

Further CMOS device scaling requires a high dielectric constant material to replace SiO$_2$ as a gate dielectric. Amorphous or single-crystalline materials with perovskite-like structure are promising candidates. In this study, the amorphous LaScO$_3$ film was directly deposited on Si (001) by molecular beam deposition (MBD) at ~100 °C with an amorphous Al$_2$O$_3$
capping layer. The as-grown samples were then annealed at 700, 800, and 1000 °C, respectively, under nitrogen ambient for 10 seconds. Various TEM techniques were applied to study the interface structure at atomic resolution, including Z-contrast imaging, electron energy-loss spectroscopy (EELS), and high-resolution transmission electron microscopy (HRTEM). The bulk LaScO$_3$ film kept amorphous at least up to 700 °C and became polycrystalline at 800 °C. All samples showed an interfacial layer thickness of about 3.5 nm except the 1000 °C-annealed one where oxygen diffused to the interface and reacted with Si substrate, leading to a thicker interfacial layer. The interfacial layer kept amorphous up to 1000 °C, which meets the industrial requirement for processing. While the chemical composition of the bulk LaScO$_3$ is stoichiometric, whether the interfacial layer is oxygen rich or poor will depend on the film growth, oxygen sources, and post-annealing conditions. Even though the dielectric constant of this interfacial layer may be lower than bulk LaScO$_3$, we expect this thermally stable interfacial layer itself can be used as an alternative gate dielectric. However, how to control oxygen content will be an important issue.

I. INTRODUCTION

Due to the problems with high gate current-leakage, the complementary metal oxide semiconductor (CMOS) devices cannot be scaled down further without replacing SiO$_2$ with a high-K oxide as a gate dielectric. Such a replacement will allow a lower ‘equivalent oxide thickness’ (EOT). LaScO$_3$ is a promising candidate for the following reasons. Single crystalline LaScO$_3$ exits in an orthorhombic perovskite structure (Pnma, a=5.784 Å, b=8.108 Å, c=5.688 Å)$^{1,2}$. Ab initio calculations$^3$ found that the band gap is 3.98–4.61 eV. Because
these simulations used the local density approximation (LDA), this bandgap is underestimated. Optical measurements resulted in an optical gap of 6 eV for polycrystalline LaScO$_3$. Amorphous LaScO$_3$ thin films on silicon have a dielectric constant $\kappa$ of 22–24 and a band gap $E_g$ of 5.7 eV (which compare favorably to the values of SiO$_2$: $\kappa_{SiO_2} = 3.9$, $E_g = 9$ eV). The band offsets between amorphous LaScO$_3$ and silicon were measured to be 2.0 eV and 2.5 eV for the conduction and valence bands, respectively. All these parameters meet the requirements of a new gate oxide.

Besides the electronic requirements there are other requirements that have to be met by a replacement material for SiO$_2$. Such a material has to be thermodynamically and kinetically stable in the presence of silicon, and the interface has to have a low trap state density. Additionally the interface between the dielectric and silicon substrate has to be atomically sharp to minimize scattering of charge carriers, which reduces mobility. To study these requirements, it is necessary to investigate the atomic structure of these materials and their interfaces before and after heat treatment. It is believed that there are basically two ways to ensure a high quality interface, either by using an amorphous oxide or using an epitaxial oxide on the Si. Polycrystalline oxides generally are not considered mainly due to the problems associated with grain boundaries. Amorphous oxide films do not have this disadvantage, but their dielectric constants and bandgaps are found to be slightly lower than their corresponding single crystalline phases. Epitaxial oxide films are thought to be the long term solution. Current research indicates that there are still a lot of issues needed to be solved about epitaxial oxide films on Si$^{8-11}$. 

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In this paper, various TEM techniques, including Z-contrast imaging, electron energy-loss spectroscopy (EELS), high-resolution transmission electron microscopy (HRTEM) were applied to study the interface structure at atomic resolution. We demonstrate that it is possible to grow a stoichiometric LaScO$_3$ film on Si substrate with an amorphous substoichiometric LaScO$_{3-x}$ interfacial layer under specific growth conditions and post-annealing treatment. This interfacial layer remains amorphous up to 1000 °C. We indicated that this thermally stable interfacial layer itself can be used as an alternative dielectric, although oxygen diffusion to the interface at 1000 °C becomes an important issue.

II. EXPERIMENT

Here, we present the interface structure of LaScO$_3$ on Si (001) directly deposited by molecular beam deposition (MBD). 100 nm-thick films were grown using elemental sources in an EPI 930 MBE chamber modified for the growth of oxides. The Si substrates were boron doped ($>4\times10^{19}$ B/cm$^3$) with one side polished. The native SiO$_2$ on the silicon wafer was thermally desorbed in ultrahigh vacuum at a substrate temperature of 900 °C, as measured with a pyrometer. Lanthanum, Scandium, and molecular oxygen (99.994% purity) at a background pressure of $5\times10^{-8}$ Torr, were co-deposited with the substrate temperature of ~100 °C as measured with a thermocouple. The lanthanum and scandium fluxes were each $2\times10^{13}$ atoms/cm$^2$ s. The film composition was evaluated using Rutherford backscattering spectrometry (RBS), giving a La:Sc concentration ratio close to 1:1. 10 nm-thick amorphous Al$_2$O$_3$ films were deposited as capping layers to prevent formation of interfacial SiO$_2$ in air. To investigate the kinetic stability of this new gate oxide material, the as-grown samples
were annealed by rapid thermal annealing (RTA) at 700, 800, and 1000 °C, respectively, under the nitrogen ambient for 10 seconds. All the samples were grown and annealed at Penn State and then shipped in air to NCSU and ORNL for atomic structure characterization. All the cross-sectional TEM specimens were prepared by standard mechanical grinding and ion milling\textsuperscript{13}, except the one which was prepared with the cleavage method\textsuperscript{14} as specified. HRTEM images were acquired at NCSU using a 200 kV TEM (JEOL 2010F); Z-contrast images and EELS spectra were simultaneously obtained at ORNL with a VG HB501UX STEM (equipped with a Nion aberration corrector, providing a electron probe size close to 1 Å) operated at 100 kV. An improved method was applied to quantify all the EELS spectra\textsuperscript{15}.

III. RESULTS AND DISCUSSIONS

Fig. 1 shows the Z-contrast image of the as-grown sample with an amorphous LaScO\textsubscript{3} film. In the Z-contrast imaging technique, the image intensity is approximately proportional to the average atomic number square (Z\textsuperscript{2}). So LaScO\textsubscript{3} will appear brighter than Si and silicon oxide darker than Si in a Z-contrast image. From the image intensity profile in Fig. 1, the interfacial layer thickness was determined to be about 3.5 nm, which is not observable in HRTEM images. Also shown is the atomically sharp interface, which is desirable for device applications. As shown in Fig. 2 (a), the interfacial layer close to the substrate is easily damaged by the electron beam. This enhanced electron beam sensitivity suggests that there are a lot of defects in the material. Since no dark area is visible at the interface between the interfacial layer and Si substrate (see Fig. 2 (b)), no silicon oxide was found. To verify this result and to exclude artifacts introduced by specimen preparation, one specimen was
prepared with the cleavage method. There was still no silicon oxide detectable. So the interface is not only structurally sharp, but also chemically sharp, which was further confirmed by EELS results.

![Graph showing interfacial layer thickness](image)

**Fig. 1** Z-contrast image of as-grown sample. The image intensity profile across the interface is shown on the top. The interfacial layer thickness is about 3.5 nm.
Fig. 2 Z-contrast images of as-grown sample. (a) The region damaged by electron beam is close to the interface; (b) No dark area visible at the interface for the TEM specimen prepared with cleavage method in order to minimize the artifacts introduced by specimen preparation.

EELS spectra were acquired from four different positions across the interface of the as-grown sample. Spectra with the Si-L\textsubscript{23} and La-N\textsubscript{45} edges are shown in Fig. 3. Although the energy onsets of these two edges are almost the same (~99 eV), we can still distinguish them.
by their shapes (i.e., energy-loss near-edge structure: ELNES). EELS spectrum 1 just shows the Si-L\textsubscript{23} edge of the substrate and EELS spectra 3-4 show the pure La-N\textsubscript{45} edge of the oxide, while spectrum 2 is approximately a linear combination of spectrum 1 and 3. Any reaction at the interface would result in a change of the Si-L\textsubscript{2,3} or the La-N\textsubscript{4,5} edge, but since a linear combination can account for spectrum 2, we can exclude such an reaction layer. So these results indicate that there is no observable La diffusion to the Si side and no observable Si diffusion to the LaScO\textsubscript{3} side within the detection sensitivity of EELS technique. The Sc-L\textsubscript{23} (407 and 402 eV, respectively) and O-K (532 eV) edges are shown in Fig. 4. None of these edges can be detected in spectrum 1, which was acquired in the bulk Si close to the interface. This means, that there was no observable Sc and O diffusion to the bulk Si side neither. Therefore, we conclude on a chemically sharp interface.
Fig. 3 EELSs acquired from four different positions across the interface of as-grown sample (the same labels applied for other EELSs). Shown are the Si-L$_{23}$ and La-N$_{45}$ edges.
Fig. 4 EELSs acquired from four different positions across the interface of as-grown sample. Shown are the Sc-L$_{23}$ (407 and 402 eV, respectively) and O-K (532 eV) edges. The insets are the Sc/O ratios and the normalized Sc white line intensities.

To get the atomic ratios and oxidation states of Sc and La, an improved method was applied to quantify all the EELS spectra. Hydrogenic cross-sections and Hartree-Slater cross-sections were used for atomic ratio calculation and oxidation state calculation, respectively. The oxidation states for transition metal or rare earth elements are usually derived from their while-lines. The free-electron gas like part 50 eV in width, beginning 50 eV past the white line onset, was chosen as the normalization window. The higher normalized white line intensities mean higher oxidation states. It should be noted that all the
atomic ratios in this study are calibrated with the ones from crystalline LaScO$_3$ (i.e. the 800 °C-annealed sample where the LaScO$_3$ film crystallized) where Sc/O (and La/O also) ratio is 1:3 (=0.33).

![EELS spectrum](image)

**Fig. 5** EELs acquired from four different positions across the interface of as-grown sample. Shown are the La-M$_{45}$ edges (849 and 832 eV, respectively). The insets are the La/O ratios and the normalized La white line intensities.

The atomic ratios and normalized white line intensities for Sc and La are shown in Fig. 4 and Fig. 5. At the bulk film (position 4), the Sc/O and La/O ratios are both 0.31, which are within the error bars of the stoichiometric value of 0.33. The ratios are higher at the
interfacial layer (position 3) and lower at the interface (position 1). It is reasonable to expect a higher oxygen content at the interface since the interfacial layer is expected to be oxygen terminated towards the Si substrate. In all these positions, the Sc/La ratio is close to 1, which is consistent with the evaluation from RBS that the La/Sc ratio of deposited film is close to 1:1. Moreover, the Sc/O and La/O ratios are consistent with the oxidation states of Sc and La. From the normalized white line intensities, Sc and La have higher oxidation states in the bulk film than in the interfacial layer. La is also in high oxidation state at the interface, which means that the interfacial layer is likely La-O terminated. So the film is within our error bars stoichiometric, except that the interface is oxygen rich and the interfacial layer is oxygen poor compared to bulk stoichiometric LaScO$_3$. However, the high Sc/O and La/O ratio (usually, higher average atomic number is expected) in the interfacial layer does not mean that the interfacial layer will appear brighter than the bulk film in the Z-contrast images. As can be seen in Fig. 1 and Fig.2, the interfacial layer is darker than the bulk film. The interfacial layer may not be as dense as the bulk film due to low temperature film growth and lattice mismatch problems, which will decrease the average atomic number. As mentioned before, there are a lot of defects in the interfacial layer, which leads to easy electron beam damage. This will be further discussed later in terms of image intensity slopes in Z-contrast images.

The 700 °C-annealed sample was characterized in the same way. The Z-contrast image is shown in Fig. 6. No changes were observed, which means the amorphous oxide film is stable at least up to 700 °C.
When annealed at 800 °C, the film became polycrystalline with grain size >30nm (see Fig.7). However, the interfacial layer is still amorphous with the same thickness of 3.5 nm (see Fig.7 and Fig. 8). HRTEM image (Fig. 9 (a)) also shows the same structure as in Fig. 7. The interface is still atomically sharp. The crystal orientation relation between crystalline
LaScO$_3$ and Si substrate turned out to be close to LaScO$_3$ (101) //Si(001) and LaScO$_3$ [010] //Si[110], although there was an interfacial layer between them and the bulk film is polycrystalline. This orientation is similar to that of the epitaxial LaScO$_3$ thin films on silicon (001) using buffer layers of alkaline earth oxides. Fig. 9 (b) shows that the crystalline LaScO$_3$ become amorphous more easily than Si under ion milling at <5 keV.

![Fig. 7 Z-contrast images of 800 °C-annealed sample. The LaScO$_3$ film became polycrystalline with large grains (>30nm). The interfacial layer is still amorphous and keeps the same uniform thickness of 3.5 nm.](image)
Fig. 8 Z-contrast image of 800 °C-annealed sample. The image intensity profile across the interface is shown on the top. Again, the interfacial layer thickness is about 3.5 nm and no dark area (silicon oxide) is visible at the interface.
Fig. 9 HRTEM images of 800 °C-annealed sample. (a) shows the same results as Fig. 7. The inset is the Inverse FFT of LaScO₃ image region with Gatan® DigitalMicrograph. (b) shows that the crystalline LaScO₃ is easier to become amorphous than Si under ion milling at <5 keV.

The interface is chemically sharp also, as shown in Figs 10-12. In the same way, the Sc/O ratios and the La oxidation states at the different positions across the interface were derived. Similar to the as-grown sample, the Sc/La is close to 1 and the interfacial layer is likely La-O terminated to Si substate. However, there was observable oxygen diffusion to the interfacial layer, as indicated by the lower Sc/O and La/O ratios. Again, this can be further confirmed.
by the oxidation states of Sc and La. The same (or even higher) Sc (and La) oxidation states exist at the interfacial layer, compared to the bulk film region. As mentioned before, the bulk film of the as-grown sample is oxygen rich. So it is not surprising that oxygen diffused from the bulk film to the interfacial layer at 800 °C, but still no oxygen-silicon reaction was observed. Moreover, the composition of the interfacial layer is more uniform and dense than that of the as-grown sample and the 700 °C-annealed sample, as can be seen from their image intensity profile slopes.
**Fig. 10** EELSs acquired from four different positions across the interface of 800 °C-annealed sample (the same labels applied for other EELSs). Shown are the Si-L$_{23}$ and La-N$_{45}$ edges.

**Fig. 11** EELSs acquired from four different positions across the interface of 800 °C-annealed sample. Shown are the Sc-L$_{23}$ (407 and 402 eV, respectively) and O-K (532 eV) edges. The insets are the Sc/O ratios and the normalized Sc white line intensities (the mark ‘?’ means the EELS is too noisy to get the reliable value of normalized white line intensity).
**Fig. 12** EELSs acquired from four different positions across the interface of 800 °C-annealed sample. Shown are the La-M\(_{45}\) edges (849 and 832 eV, respectively). The insets are the La/O ratios and the normalized La white line intensities.

Finally, the 1000 °C-annealed sample was characterized with HRTEM and Z-contrast imaging (Fig. 13). The interfacial layer thickness increased dramatically from ~3.5 nm to ~7.5 nm. The interface is not as sharp as before due to the oxygen reaction with Si substrate. The roughness could be one main reason for the reduced charge carrier mobility encountered when replacing SiO\(_2\) with a high-K oxide. The image intensity profiles across the interface are shown on the left side for both images. To the Z-contrast image, the image intensity profile has a prominent peak close to the crystalline LaScO\(_3\) side. The peak was either caused
by strain effect or by oxygen denude (causing average atomic number increase). It turned out to be the former case since similar peak was observed just out of the anneal region where no oxygen reaction with Si happened. The peak width in this profile is \(-3\) nm, which is close to the interfacial layer thickness for the previous samples (\(-3.5\) nm). The image intensity at the interface region is lower than at the silicon side, which means there is silicon oxide formation. Besides, the image intensity changes gradually in the reaction region. So at 1000 \(^\circ\)C, more oxygen diffused through the interfacial layer from the bulk film and reacted with Si substrate. Therefore, how to eliminate oxygen source at 1000 \(^\circ\)C is very important to avoid oxygen-silicon reaction.
Fig. 13 HRTEM image and Z-contrast image of 1000 °C-annealed sample. Image intensity profiles are shown on the right side.
Table 1 Summary of experimental results

<table>
<thead>
<tr>
<th>Sample</th>
<th>Interfacial thickness (nm)</th>
<th>Sc/O ratio</th>
<th>Sc oxidation states: (L₃+L₄)/free e⁻</th>
<th>La/O</th>
<th>La oxidation states: (M₅+M₄)/free e⁻</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-grown at 100 °C</td>
<td>3.5</td>
<td>1. ---</td>
<td>1. ---</td>
<td>1. ---</td>
<td>1. ---</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. 0.13</td>
<td>2. 0.39</td>
<td>2. 0.13</td>
<td>2. 1.60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. 0.43</td>
<td>3. 0.49</td>
<td>3. 0.45</td>
<td>3. 1.09</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. 0.31</td>
<td>4. 0.72</td>
<td>4. 0.31</td>
<td>4. 1.70</td>
</tr>
<tr>
<td>Annealed at 700 °C for 10 sec.</td>
<td>3.5</td>
<td>----</td>
<td>----</td>
<td>----</td>
<td>----</td>
</tr>
<tr>
<td>Annealed at 800 °C for 10 sec.</td>
<td>3.5</td>
<td>1. ---</td>
<td>1. ---</td>
<td>1. ---</td>
<td>1. ---</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. 0.20</td>
<td>2. (?)</td>
<td>2. 0.09</td>
<td>2. 0.23</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. 0.20</td>
<td>3. 0.24</td>
<td>3. 0.27</td>
<td>3. 0.19</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. 0.33</td>
<td>4. 0.17</td>
<td>4. 0.33</td>
<td>4. 0.17</td>
</tr>
<tr>
<td>Annealed at 1000 °C for 10 sec.</td>
<td>7.5</td>
<td>----</td>
<td>----</td>
<td>----</td>
<td>----</td>
</tr>
</tbody>
</table>

IV. CONCLUSIONS

To conclude (see TABLE 1), we have demonstrated that amorphous LaScO₃ film can be grown on Si at low temperature 100 °C with a 3.5 nm thick interfacial layer. The bulk film for as-grown sample is close to be stoichiometric and became polycrystalline at 800 °C. The interfacial layer is oxygen rich after post-annealing, depending on the annealing temperature and oxygen sources. The 3.5 nm thick interfacial layer remains amorphous up to 1000 °C. So amorphous LaScO₃ (≤3.5 nm) can be deposited directly on Si substrate as gate dielectric for CMOS devices. However, oxygen diffusion through the thin LaScO₃ₓ film and reaction with Si substrate can increase the EOT and the interface roughness at 1000 °C. So possible oxygen sources at 1000 °C need to be eliminated, for example, by choosing right metal gate or
capping layer materials.

ACKNOWLEDGMENTS

F. D. Liu wants to thank Dr. Steve Pennycook and his group at ORNL for helping with microscope operation and specimen preparation. L. F. Edge gratefully acknowledges and AMD/SRC fellowship. The financial support of the Semiconductor Research Corporation (SRC) is highly appreciated here.

References


4.2 La-Silicate on Si (001)

(This part was adapted from two papers in preparation)

Chemical Composition Changes across the High-K La-silicate Layers on Silicon (001)

Substrates

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La-based high-K oxides are attracting more and more attention due to their potential possibility as good gate dielectrics for CMOS devices\textsuperscript{1,2}. La\textsubscript{2}O\textsubscript{3} has a dielectric constant K in the range of 25-30 and a bandgap ~6.0 eV\textsuperscript{3}, which make it ideal as the next generation high-K gate dielectric. To ensure a high quality Si-oxide interface, we can either use an amorphous oxide on the Si substrate, or use a high-K oxide epitaxy. Obviously, using an amorphous oxide is the lowest-cost and easiest solution. Ideally, an epitaxy should be used. However, it has been very challenging to have an epitaxial oxide film on the Si substrate\textsuperscript{4-6}. In this study, we just considered the former case.
Like most other currently studied oxides, La$_2$O$_3$ crystallizes well below 1000 °C. Alloying the desired oxide with a glass former – SiO$_2$ or Al$_2$O$_3$ – can solve this problem$^7$$^8$. In this study, SiO$_2$ is preferred, since aluminates usually have a higher defect concentration than silicates. Another advantage of alloying with SiO$_2$ is that the oxygen diffusion rate in the oxide is greatly reduced so that the action of oxygen and the Si substrate can be avoided$^9$. It is well known that the SiO$_2$-Si interface is of very good electrical quality. So including a SiO$_2$ interfacial layer to separate the high-K oxide away from the channel could make sure the good electrical interface quality with the Si substrate.

![Fig. 1 Schematic of film growth processing for as-deposited samples.](image)

<table>
<thead>
<tr>
<th>Specimen</th>
<th>Annealing temperature (10 sec.)</th>
<th>Tungsten used</th>
<th>Tungsten thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>As-deposited</td>
<td>UHV-W</td>
<td>~500</td>
</tr>
<tr>
<td>2</td>
<td>1000 °C</td>
<td>UHV-W</td>
<td>~500</td>
</tr>
<tr>
<td>3</td>
<td>1000 °C</td>
<td>DC-W</td>
<td>~1000</td>
</tr>
</tbody>
</table>

To take the advantages mentioned above, we designed the experiments as shown in Fig. 1. First, thin SiO$_2$ layer and La$_2$O$_3$ layers were grown on Si (001) substrates. Then a 400 °C
in situ anneal was carried out to condense and alloy the two thin films. After that, gate metals were grown on top. TaN was used instead of Ta due to its more stability. W blocks oxygen and hydrogen (forming gas anneal) from anneal. Two kinds of tungsten layers were investigated in order to determine what caused the EOT increase after RTA annealing at 1000 °C for 10 sec in N₂ environment. Therefore, we have three samples (Table 1). From XRD results, we already know that DC-W has a β-W (or W₃O) structure. However, it also has been confirmed by XRD¹⁰ that there is a phase transformation at high temperature as shown below,

\[
\beta - W \ (or \ W_3O) \rightarrow \alpha - W
\]

We will show later that the phase transformation is the main reason for the EOT increase due to the fact that oxygen is released during the phase transformation and then the oxygen diffuses to the interface with the Si substrate and reacts with silicon.

First, let us get the general information about the high-K La-silicate layer from conventional HRTEM images and Z-contrast images (see Figs. 2-4). It should be noted that in order to minimize the artifacts caused by specimen preparation, cleavage method was used to prepare TEM specimens.
Fig. 2 (a) HRTEM image, and (b) Z-contrast image of as-deposited sample with UHV-W. At the top of each image is the corresponding image intensity profile.
Fig. 3 (a) HRTEM image, and (b) Z-contrast image of annealed sample with UHV-W. At the top of each image is the corresponding image intensity profile.
Fig. 4 (a) HRTEM image, and (b) Z-contrast image of annealed sample with DC-W. At the top of each image is the corresponding image intensity profile.
From the images shown above, the thickness of the high-K La-silicate layer just increased slightly (2.0 nm→2.2 nm) after annealing for the sample with UHV-W. There was a significant thickness increase (2.0 nm→4.0 nm) for the sample with DC-W, however. It was already confirmed from XRD that the W layer has a $\beta$-W (or W$_3$O) phase. So we just need to check if there was a phase transformation ($\beta$-W→$\alpha$-W) after annealing. The phase transformation was confirmed from the HRTEM image processed with Fast Fourier Transformation (FFT) (Fig. 5). It was found that the big W-grain was on the axis [113] of $\alpha$-W.
**Fig. 5** (a) HRTEM image, and (b) its FFT from a W grain which is fitted well by a simulated SAED pattern by the computer software Java-EMS.
Also noted from Figs 2-4 is the interface roughness with the TaN layer for the annealed sample with DC-W. This sample also has big TaN grains at the interface. To the other two samples, the La-silicate layers have sharp interfaces both the silicon substrate and the TaN layer, and the TaN grains are the interfaces are small, as seen from Figs 2-4.

From the Z-contrast image intensity profiles, we can also tell roughly the chemical composition change of the high-K La-silicate layers. To the as-deposited sample, the deposited La$_2$O$_3$ layer and SiO$_2$ layer were not mixed well, as indicated by the two slopes of the Z-contrast image intensity profile. To the annealed sample with UHV-W, there is basically one slope, indicating the well-mixed condition. To the annealed sample with DC-W, there is an ‘extended tail’ on the Z-contrast image intensity profile, indicating possible oxygen reaction with the Si substrate. However, to exactly determine the chemical composition change across the high-K La-silicate layers, EELS analysis was done.
**Fig. 6** Schematic view of rectangular scan done for the as-deposited sample. The arrow indicates the scanning direction.

Fig. 6 schematically shows the rectangular scan done for the as-deposited sample. The arrow indicates the scanning direction. The scanning rectangular window on the sample is 2.2 nm x 1.5 nm, as determined from Z-contrast images and EELS spectra. Different edges are shown in Fig. 7.
(a) Si-L edge (~99 eV) and La-N edge (~99 eV)

(b) C-K edge (284 eV) and N-K edge (401 eV)
(c) O-K edge (532 eV)
Fig. 7 Different edges obtained from the as-deposited sample. The spectra numbers are the same as those positions numbers shown in Fig. 6.

From the EELS spectra, the chemical composition changes across the high-K layer were obtained (Fig. 8).
Fig. 8 Chemical composition changes across the high-K layer of the as-deposited sample.

A few results need to be paid more attention. First, as shown in Fig. 8 (a), there was some La diffused to the SiO$_x$ layer and the La-O super atomic layer structure which to be discussed in more detail later. The observations about the oxidation state changes of La (Fig. 8 (a)) and the Si/La ratios are consistent with these results. Fig. 7 (b) shows no N edge, indicating the chemical sharp interface between La-O layer and the TaN layer, which was consistent with the results obtained from Fig. 8.

Now let us look at the annealed sample with UHV-W. The point scan EELS spectra are shown in Fig. 9.
(a) Z-contrast image indicating the point scan positions

(b) Si-L edge (≈99 eV) and La-N edge (≈99 eV)
(c) C-K edge (284 eV) and N-K edge (401 eV)

(d) O-K edge (532 eV)
Compared to the as-deposited sample, this annealed sample with UHV-W did not show chemically sharp interface with TaN, although it has a smooth interface. As indicated from Fig. 9 (c), there as some N diffused to the La-O layer. However, the reaction between La-O layer and the TaN is expected to be slight based on the observation of the no obvious EOT increase and the EELS results shown below which was got from the rectangular scan across the high-K layer on this sample (Fig. 10).
Two things should be noted. One is that the super La-O atomic layer was partially destroyed due to the reaction/mixing with the Si-O layer and the TaN layer. The other is the more complete alloying between La-O layer and the Si-O layer. This confirmed the result got from Z-contrast image intensity profiles.

Finally, we studied the annealed sample with DC-W. Similarly, the EELS spectra from rectangular scan are shown in Fig. 11 and the chemical changes across the high-K layer are shown in Fig. 12.

**Fig. 10** Chemical changes across the high-K layer got from rectangular scan.
(a) Si-L edge (~99 eV) and La-N edge (~99 eV)
(b) C-K edge (284 eV) and N-K edge (401 eV)
(c) O-K edge (532 eV)
(d) La-M edge (832 eV)

Fig. 11 EELS spectra acquired from the annealed sample with DC-W. See Fig. 12 about the rectangular scan area.
Fig. 12 Chemical changes across the high-K layer got from rectangular scan.
Compared the annealed sample with UHV-W, this sample showed a more obvious reaction between the TaN layer and the La-O layer as indicated by the N-K edges in Fig. 11 (b). Also, as noted before, the big TaN grains at the interface makes it worse for EOT increase and possible long-distance charge scattering. Another important observation is that there is a SiOx layer between the La-silicate layer and the Si substrate. This could be the main cause of the EOT increase. So oxygen is the EOT killer and it also causes the rough interface with the TaN layer.

To sum it up, the high-K layer thickness was determined. The high-K layers kept amorphous even after annealing. The thickness decreased only slightly for the annealed sample with UHV-W. Also this sample showed good interfaces with both the Si substrate and the TaN layer, although it was observed that there was slight reaction between the high-K layer and the TaN layer. The La-O layer and the Si-O layer was shown to be alloyed well at high temperature anneal. All of these make the sample with UHV-W a good choice for the next generation gate dielectric. To the annealed sample with DC-W, the oxygen initially contained in the DC-W caused the rough interface between the high-K layer and the TaN layer, and gave rise to the SiOx layer between the high-K layer and the Si substrate. The chemical changes across the high-K layer were well determined. All these results give us a deep understanding about the promising La-silicates as the next generation gate dielectrics.
References


4.3 LT-AlN Nucleation Layer on c-sapphire

(This part was adapted from two papers in preparation)

Interface structures of LT-AlN nucleation layer on c-sapphire

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\textsuperscript{2}Condensed Matter Division, Oak Ridge National Lab, Oak, Ridge, TN 37831

Wide bandgap III-nitrides have seen enormous success in modern electronic and optoelectronic devices. However, the choice of appropriate substrate materials for III-nitrides is still an issue. Compared to Si and SiC, sapphire offers a compromise as the most widely used substrate materials to date. High-quality GaN on sapphire has been achieved by applying both the LT (low temperature)-AlN nucleation layer technique and the ELO (epitaxial lateral overgrowth) technique\textsuperscript{1}. Moreover, the crystal polarity of GaN can be inverted from N-face polar to Ga-face polar by the LT-AlN nucleation layer, which provides a new degree of freedom for the investigation of III-nitrides and their devices\textsuperscript{2}. So LT-AlN
plays an important role in III-nitrides and their devices. However, much remains to be known about the interface structures of LT-AlN on c-sapphire.

In this study, we aim to study the interface structures of LT-AlN on c-sapphire, including the one between AlN and GaN. The sample was grown by a "two-step" MOVPE (metalorganic vapor phase epitaxy) process with a prior nitridation of the sapphire substrate and a LT-AlN nucleation layer (15 nm) grown at 600 °C and a V/III ratio of 24500 due to the inefficient kinetics of the NH₃ decomposition. The GaN film (1 μm) was subsequently grown on the annealed LT-AlN layer at a higher temperature of 1030 °C and a V/III ratio around 100. The TEM specimen was prepared by the standard mechanical grinding and ion milling method. Z-contrast imaging and density functional theory (DFT) based ab initio calculation were applied to study the interface structures.

Before proceeding to the experimental results, let us re-check the lattice parameters, lattice mismatch, and crystal orientation relation between GaN, AlN, and sapphire (see Table 1). The lattice mismatch between GaN and AlN is 2.48%, which makes AlN a good choice as a LT nucleation layer on the sapphire substrate. Even with a lot of efforts, the dislocation density in the high-quality GaN film grown on LT-AlN is still in the order of 10⁵ cm⁻², which is much higher than those found in more traditional III/V semiconductor systems such as the arsenides and phosphides. In order to have high performance III-nitride based devices, the dislocation issues have to be solved, which in turn to large extent depends on the proper understanding about the interface structures.
Table 1 Lattice parameters and lattice mismatch with sapphire

<table>
<thead>
<tr>
<th>Material</th>
<th>Lattice constant (Å)</th>
<th>Plane with nearest match to GaN(0001)</th>
<th>Effective lattice constant $a_{\text{eff}}$ (Å)</th>
<th>Lattice mismatch with sapphire (%) $(\frac{a_{\text{eff}}^{\text{GaN or AlN}} - a_{\text{eff}}^{\text{sapphire}}}{a_{\text{eff}}^{\text{sapphire}}})*100$</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN</td>
<td>$a=3.189$ $c=5.186$</td>
<td>(0001)</td>
<td>3.189</td>
<td>16.09</td>
</tr>
<tr>
<td>AlN</td>
<td>$a=3.112$ $c=4.982$</td>
<td>(0001)</td>
<td>3.112</td>
<td>13.29</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>$a=4.758$ $c=12.991$</td>
<td>(0001) rotated $30^\circ$ ($=4.758 / \sqrt{3}$)</td>
<td>2.747</td>
<td>0</td>
</tr>
</tbody>
</table>

Fig.1 shows two Z-contrast images of the sample. In a Z-contrast image, only large-angle elastic scattered electrons are collected and then its image intensity is approximately proportional to $Z^2$. Compared to phase-contrast HRTEM imaging, Z-contrast imaging is relatively insensitive to focusing conditions and specimen thickness, and its image is more directly interpretable in terms of atomic coordinates$^4$. So AlN appears darker than GaN and sapphire in a Z-contrast image. The threading dislocations can also be seen clearly in a Z-contrast image. The threading dislocation density is estimated to be in the order of $10^9$/cm$^2$. Also shown are the AlN pits, which are to be discussed in detail later.
Fig. 1 Z-contrast images.
From the Z-contrast images, the 8.5:7.5 relationship of the edge dislocations was observed (Fig. 2). On the [-2110] projection of AlN, the Al-Al distance in the [01-10] direction is

$$\frac{\sqrt{3}}{2} a_{\text{AlN}} = 2.695 \text{ Å}$$

and on the [-1100] projection of sapphire, the Al-Al distance in the [11-20] direction is

$$\frac{1}{2} a_{\text{sapphire}} = 2.379 \text{ Å}$$

So this Al-Al distance difference gives rise to about every 8.5 (\(\frac{2.695}{2.695 - 2.379} = 8.5\)) Al-Al atomic distances in AlN corresponding to about 7.5 (\(\frac{2.379}{2.695 - 2.379} = 7.5\)) Al-Al atomic distances in sapphire (see Fig. 2). Experimental results are 8.7 and 7.7, respectively, which are pretty close to the theoretical values, 8.5 and 7.5.
The above approach is different from the one mentioned in the reference\textsuperscript{1}, but it gives the same results and we think, is more straightforward. The lattice mismatch is expected to be the same for other directions in the c-plane due to the lattice symmetry (hexagonal).

Actually, we can take a step further. Because of the hexagonal structure of AlN, there are 6 equivalent $<-2110>$ directions: [-2110], [2-1-10], [1-210], [-12-10], [11-20], and [-1-120]. So we can assume that there is a threading dislocation at each point that the misfit dislocations

\textbf{Fig. 2} 8.5:7.5 lattice misfit edge dislocations.
meet (Fig. 3). Therefore, we can get the theoretical threading dislocation density, 8.48 \times 10^{13}/cm^2 (1.18 \times 10^{14}/cm^2 for GaN on sapphire). The threading dislocations are caused by the stress concentration due to the arrangement of the misfit edge dislocations. This is not a serious problem for more traditional cubic III/V semiconductor systems such as the arsenides and phosphides, because usually there are 2 (rather than 3) edge dislocation lines cross each other. This explains why the threading dislocation density is much lower in cubic III/V materials. Shuji Nakamura from UCSB believes non-polar GaN could also play an important role in reducing the threading dislocation density. It is interesting to note that non-polar planes such as the (01-1-1) plane usually do not have hexagonal structure.

![Fig. 3 Relationship between misfit edge dislocations and threading dislocations. Each black line represents a misfit edge dislocation line and each green spot a threading dislocation perpendicular to the misfit edge dislocation plane.](image)
Before determining the interface atomic structure, it is important to know the polarization direction of GaN or AlN. So far, three methods have been used to identify the polarity of hexagonal III-nitrides, i.e., chemical etching, convergent electron beam diffraction (CBED), and high resolution Z-contrast imaging\(^5\). In this study, all these three methods were used. In the following, only the direct polarity determination of GaN and AlN are shown. The CBED method is to be discussed in the next part when the GaN inversion domain boundaries (IDBs) are encountered.

For a wurtzite-structure crystal, the [0001] direction (or \(c\) axis) is usually defined along the Ga-face lattice polarity and [000-1] direction along the N-face lattice polarity (Fig. 4).

![Fig. 4 GaN (or AlN) [0001] direction definition.](image)

Fig. 5 shows the direct lattice polarity determination of both GaN and AlN from Z-contrast images. Only very recently was the direct polarity determination of AlN realized\(^5\). 

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Although the much stronger Ga scattering than N scattering makes it difficult to separate Ga atom column from N atom column, we succeeded in directly determining the GaN local lattice polarity for the first time.

(a) Ga-face GaN

(b) Al-face AlN

**Fig. 5** Direct lattice polarity determination of local lattice in GaN and AlN from Z-contrast images. To GaN, two opposite polar lattice structures are used to fit the same Z-contrast image.
The lattice structure of sapphire has been well known for a long time. However, the direct lattice structure determination was impossible until recently with the aberration-corrected STEM-Z contrast imaging. The direct lattice structure determination is very important in determining the interface atomic structures. The Z-contrast image of sapphire is shown in Fig. 6. The O and Al atom columns can be seen clearly.

![Fig. 6 Direct lattice structure determination of sapphire.](image)

Now we have determined the lattice structures of GaN, AlN, and sapphire. With this information at hand, it is easier to determine the interface structure. The interface structure is shown in Fig. 7. There are a few important points on which more attention should be paid. The lattice misfit edge dislocation was observed, as expected before. However, the dislocation plane is not the interface plane. It is one Al-N monolayer above the interface. This monolayer acts as a transition layer to tolerate the lattice mismatch between AlN and sapphire. Sapphire lattice is very stiff compared to AlN. So it is reasonable to have this
transition layer of AlN. Another extremely important point is that such an interface structure is the first experimental explanation as to why AlN can invert the polarity of GaN. It has been well known that the direct grown GaN film on sapphire has an N-face polarity, while it has a Ga-face polarity when a LT-AlN nucleation layer is put between them\(^8\). Usually, “epi-ready” sapphire substrates are O-terminated. Actually, it should not matter whether the substrate is oxygen-terminated or Al-terminated. As seen from the Z-contrast image, it clearly shows that the top Al monolayer on sapphire belongs to the substrate. This is reasonable, since Al-O bonds are stronger than Al-N bonds. So we have the first experimental explanation about the polarity change of GaN by LT-AlN.

**Fig. 7** Z-contrast image of AlN/sapphire interface. Arrows represent how the lattice was distorted due to the misfit edge dislocation.

Based on the Z-contrast image shown above, the interface structure can be roughly determined like this (Fig. 8),
To make things easier, we have considered only the region without misfit edge dislocations. From the Z-contrast image, the only thing unknown about the interface structure is that how many N atoms and Al atoms are at the interface. To determine this, a few models were set up and then DFT-based *ab initio* calculations were run to see which one has the lowest energy.

Now, let us just consider the Al-N layer and the Al-O layer at the interface (Fig. 9 (a)). Because the structure is hexagonal on the c-plane both for AlN and sapphire (Fig. 9 (b)) and the results already indicated that the N atoms of the Al-N layer lies just above the Al atoms.
of the Al-O layer as seen in the projection direction (Fig. 7), the N atoms must lie exactly on
the Al atoms of the Al-O layer and therefore the Al-N hexagon (3 Al atoms + 3 N atoms)
exactly sits on the Al-O hexagon (2 Al atoms + 3 O atoms). The observation narrows things
down to a few cases. In the following, we just consider 4 most likely models.

In model 1, both the Al-N layer and the Al-O layer follow their corresponding bulk
structure. In model 2, 1/3 of Al atoms are added in the Al-O layer so that the Al-N layer and
the Al-O layer are structurally similar, if all the atoms are considered as hard balls. In model
3, 1/3 N atoms are taken away in the Al-N layer. In model 4, 1/3 of Al atoms are added in the
Al-O layer and 1/3 N atoms are taken away in the Al-N layer. \textit{ab initio} calculations indicated
that model 1 has the lowest energy among these 4 models.
Fig. 9 (a) Cross-sectional view of the Al-N layer and the Al-O layer at the interface, (b) top-down view of the Al-N layer with different Al/N ratios (only 4x4 unit cells are shown), and top down view of the Al-O layer with different Al/O ratios (only 2x2 unit cells are shown). 4 most likely models are proposed.
After relaxation, the calculated model 1 interface structure is shown in Fig. 10. This structure will be applied when discussing GaN inversion domain boundaries (IDBs) in the next part. Further calculations need to be done about the structure with the dislocations. However, current results are good enough for this study.

![Model 1 interface structure after relaxation by DFT based ab initio calculations.](image)

**Fig. 10** Model 1 interface structure after relaxation by DFT based *ab initio* calculations.

The interface atomic structure between AlN and GaN is much simple and straightforward. However, the pits could make things complicated. In fact, AN (or GaN) pits
are usually observed in AlN (or GaN) films grown on sapphire substrates\textsuperscript{9} \textsuperscript{10}. A lot of 2-D information has been obtained about the pits shape\textsuperscript{11}. However, the exact 3-D geometry has not been determined.

The pits shape has been thought to be like the one in Fig. 11 (a). Almost all the methods used to determine the pits geometry only give 2-D information. In order to derive back to the 3-D information from 2-D information, first of all, we need to know the relationship between them. For a TEM specimen, if we cut through the pits at different positions, different cutting cross sections will be got (Fig. 11 (b) and (c)). Between positions 2 and 3, the angle $\alpha$ is constant, which can be used to identify the pits planes. Between positions 1 and 2, the angle $\beta$ can vary in the range of $\alpha$ and $180^\circ$. 
Fig. 11 (a) 3-D view, (b) top-down view, and (c) cutting cross sections at two different positions.
The cross sections determine what we see about the pits shape in a Z-contrast image (Fig. 12). The measured pits tip angles are shown in Table 2. It indicates that the angle \( \alpha \) is about 56.8°, which is exactly the tip angle value of the pits with planes \{01-1-1\}. This is further confirmed if we blow up the region circled in Fig. 12. This is shown in Fig. 13, where the pits plane was identified to be plane (01-1-1).

![AlN pits shown in a Z-contrast image.](image)

**Fig. 12** AlN pits shown in a Z-contrast image.

<table>
<thead>
<tr>
<th>Plaines</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
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<tbody>
<tr>
<td>Pits tip angle(( \alpha ) or ( \beta ))</td>
<td>85.48°</td>
<td>56.82°</td>
<td>74.60</td>
<td>59.72</td>
<td>57.04</td>
<td>57.4</td>
<td>60.68</td>
</tr>
</tbody>
</table>

**Table 2** Pits tip angles
Based on the results obtained above, we can take one step further to determine the exact 3-D geometry of a pits. As mentioned before, the image intensity is approximately proportional to the atomic number $Z^2$. So, a $Z$-contrast image can actually give us 3-D information about the pits. In fact, the geometry of one pits (the one labeled number 6 in Fig. 12) was exactly determined (Fig. 14). The experimentally measured geometry values are the same as those derived from pure geometry calculations. So for the first time, we determined the exact 3-D geometry of AlN pits.
In summary, the 7.5:8.5 theory about misfit edge dislocations of LT-AlN on c-sapphire was confirmed. The theoretical threading dislocation density in AlN was derived to be $8.48 \times 10^{13}/\text{cm}^2$. The direct polarity determination of GaN was successfully realized for the first time. The interface atomic structure was determined. It was observed that the misfit edge dislocation plane was one Al-N monolayer above the interface plane. For the first time, we experimentally explained why LT-AlN layers can invert the polarity of GaN. Finally, the exact 3-D geometry of AlN pits was determined for the first time.

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References


4.4 GaN Inversion Domain Boundaries

(This part was adapted from two papers in preparation)

GaN Inversion Domain Boundaries on c-sapphire

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The crystal polarity of III-nitrides provides a new degree of freedom for the investigation of III-nitrides and their devices\textsuperscript{1}. The GaN inversion domain boundaries have a lot of unique properties, which can be used to fabricate many novel electronic and optoelectronic devices\textsuperscript{2,3}. However, not much is known about their real structural and electronic properties.

In this study, we aim to determine the interface structures of GaN on c-sapphire and GaN inversion domain boundaries (IDBs). The sample was grown by a MOVPE (metalorganic vapor phase epitaxy) process. A LT-AlN nucleation layer (18 nm) was first patterned on c-sapphire by the photolithography method and then a GaN layer was grown on the whole surface (Fig. 1). The TEM specimen was prepared by the standard mechanical
grinding and ion milling method. Z-contrast imaging, conventional bright field imaging, convergent electron beam diffraction (CBED), and density functional theory (DFT) based *ab initio* calculations were applied to study the interface structures.

**Fig. 1** Schematic view of the sample structure, top-down view (top) and cross-sectional view (bottom).

Fig. 2 shows the structure at the inversion domain boundary region. The LT-AlN layer thickness was measured to be about 18 nm. The LT-AlN layer did not end up sharply, which caused the IDBs not well defined. This will be discussed in more detail later.
Fig. 2 Z-contrast image of the cross-sectional specimen. The crystal orientation is the sample as that shown in Fig. 1.

Although Z-contrast imaging can directly determine the polarity of GaN, this information is too local. CBED can give a better global view about the IDBs. So we chose CBED to study the IDBs. In order to determine the polarity of GaN, we need to choose the right zone axis. Zone axis [0-110] was usually chosen because the features are not so good on the zone axis [-2110] (Fig. 3). However, it is easier to determine the atomic structure from a Z-contrast image on the zone axis [-2110], as will be shown later.
Simulated 100nm thick $[0\ 1\ 10]$
Fig. 3 Polarity scan across the IDB region. (a) Traditional bright field image, (b) simulated CBED patterns on two different zone axes, and (c) experimental CBED patterns. The software program Java-EMS was used to do the simulation.
The polarity scan was done across the IDB region (Fig. 3). There are a few IDBs, which we call transition region. The similar observation was found in the literature\textsuperscript{5}, except that the film was grown with plasma induced molecular beam epitaxy (PIMBE) and the transition region was shifted to the Ga-face side. In this study, the transition region was shift to the N-face side. This could be caused by the nitridation step. By comparing with the simulated CBED patterns, the GaN zone axis was determined to be [0-110] and the specimen thickness was about 100 nm at the positions scanned. Some experimental CBED patterns are not so clean. This is thought to be caused by defects, especially dislocations, in the GaN film. In order to see why there are a few IDBs instead of one, we took a closer look at the edge of the LT-AlN layer (Fig. 4 (a)). Clearly, the LT-AlN layer did not end up sharply. There were some GaN islands and AlN islands also. It was noticed also from optical microscopy observations that the edges of LT-AlN were not well aligned in the [-2110] and [0-110] directions. The Z-contrast image of the plane view specimen indicated a wavy boundary caused by the photolithography patterning (Fig. 4 (b)). The contrast about the boundary between N-face region and Ga-face region is thought to come from the thickness contrast. It was noticed that the Ga-face side is thicker than the N-face side due the LT-AlN layer, and also, the N-face side is easier to ion mill away. All of these could cause the formation of the transition layer.
Fig. 4 Z-contrast images, (a) Cross-sectional view (GaN zone axis [0-110]), and (b) plane view.

The real situation near the edge of the LT-AlN is really complicated due to the reasons mentioned above. Since we already know the interface structure between LT-AlN and sapphire, it is easier to get the idea what the IDBs should be like if we know the interface structure between GaN and sapphire. So we studied the region far away from the LT-AlN edge. Also as pointed out earlier, it is easier to determine the atomic structure from a Z-
contrast image on the GaN zone axis [-2110]. So one more TEM specimen was prepared, as
cut in a way shown below (Fig. 5),

![Diagram of sample structure](image)

**Fig. 5** Schematic view of the sample structure, top-down view (top) and cross-sectional view (bottom).

Fig. 6 shows the Z-contrast image of the cross-sectional specimen. The dislocation
density is estimated to be in the order of $10^{10}/\text{cm}^2$, which, as expected, is lower than the
theoretical threading dislocation density, $1.18 \times 10^{14}/\text{cm}^2$. Again, we studied the lattice misfit
edge dislocations at the interface of GaN/sapphire (Fig. 7). The experimental results
indicated a 7.4:6.4 lattice misfit, which are pretty close to the theoretical value, 7.2:6.2. Also clearly shown is the rough interface, which to be discussed later.

Fig. 6 Z-contrast image of the cross-sectional specimen.
Before proceeding to the interface atomic structure, it is worth checking our theory about the relation between lattice misfit edge dislocations and threading dislocations (Fig. 8 (a)). As pointed out before, around each threading dislocation, there is stress concentration.
Due the arrangement of the threading dislocations, we expect to see roughly circular dislocations loops around each threading dislocations. Since threading dislocation densities decrease as moving away from the interface, of course, we should see big loops in a TEM plane-view specimen which was cut a few hand nanometer away from the interface. A TEM specimen is thin so that the stress can be relaxed by forming dislocations. In fact, this is what was observed from Fig. 8 (b). So our theory was supported by experimental observations, even though the real situation is more complicated.
Fig. 8 Relation between misfit edge dislocations and threading dislocations. (a) Theoretical model (close to the interface). Each black line represents a misfit edge dislocation line and each green spot a threading dislocation perpendicular to the misfit edge dislocation plane. (b) Plan-view experimental results from the N-face side. The specimen plane was cut a few hundred nanometer away from the interface.
Unlike the sharp interface of LT-AlN on sapphire, this interface is pretty atomically rough (~2 nm). Similar observation was found in the literature. There was a clear interfacial reaction between GaN and sapphire for annealing temperatures higher than 1000 °C as indicated by Raman scattering\textsuperscript{6}. The chemical composition of the interfacial layer could be Al\textsubscript{x}Ga\textsubscript{1-x}N, which has been reported in the literature\textsuperscript{7}. However, no direct determination of the interface structure has been done. Understanding the interface structure is essential because the interface determines the quality and polarity of subsequently grown films.

The Z-contrast image is shown in Fig. 9 (a). The sapphire lattice structure is clearly shown. So it is easy to determine its structure. It is little difficult to determine the Ga-N layer lying just on the Al-O layer. Due to the higher lattice mismatch near the interface and the stronger scattering of Ga atoms, no direct lattice information about GaN can be got near the interface. Direct lattice determination can be done far away from the interface and the lattice structure near the interface can be derived. However, this could be misleading due to the stacking faults in the [0001] direction. Since it is always known the GaN film is N-face, we tried two possible cases, i.e., using Ga-N layer a and Ga-N layer b to fit the underlying Al-O layer (Fig. 9 (b)). Compared with the experimental results, it was found that the Ga-N layer b (not layer a) is the right one lying exactly on the Al-O layer, which means Ga atoms stay at the Al positions. The same thing happened at other regions with rough interface. This indicates that the reactions mentioned above are possible. Based on these observations, the atomic model was proposed to fit the experimental results (Fig. 9 (a)). Just as the case of LT-AlN on sapphire, there are a few import points on which more attention should be paid on.
The lattice misfit edge dislocation was observed, and the dislocation plane is one Ga-N monolayer above the interface. This monolayer acts as a transition layer to tolerate the lattice mismatch between GaN and sapphire. As seen from the Z-contrast image, it clearly shows that the first Ga monolayer at the interface belongs to the GaN film, since Ga-N bonds are stronger than Ga-O bonds. So we have the first experimental explanation about the N-face polarity of GaN directly grown on sapphire.
Fig. 9 (a) Z-contrast image of the interface and its atomic fitting model, and (b) Ga-N layer a and Ga-N layer b tried to fit the underlying Al-O layer. Ga-N layer b was determined to be the right one on the Al-O layer.
So far, we have determined the interface structure of GaN on sapphire except how many O and Ga atoms at the interface that needs to be determined by DFT based *ab initio* calculations. However, this does not matter to the whole picture about the interface structure of GaN on sapphire. Together with the known interface structure of AlN on sapphire, it is now ready to construct the GaN IDBs (Fig. 10 (a)). Compared with the early proposed GaN IDB model (Fig. 10 (b)), our model contains more information especially about the misfit edge dislocations and the atomic configurations at the interface. So our new model gives more insights about real GaN IDB structures.
Fig. 10 (a) new GaN IDB model based experimental results, and (b) proposed GaN IDB model.
In summary, the GaN IDBs were studied in detail. A transition region with mixed polarities was found with the CBED method. The transition region was related to the not well defined edge of the LT-AL. The 7.2:6.2 theory about misfit edge dislocations of GaN on c-sapphire was confirmed. The dislocation loops were observed experimentally, indicating the stress concentration around thread dislocations. The chemical reaction between GaN and sapphire at high temperature were identified. The reaction mechanism was proposed. The interface structure of GaN on sapphire was determined for the first time. Like AlN on sapphire, the misfit edge dislocation plane was one Ga-N monolayer above the interface plane. For the first time, we also experimentally explained the N-face polarity of GaN directly grown on sapphire. Finally, a more accurate GaN IDB was proposed, which gives new insights for future work.

References


5. Conclusions

In this study, we investigated the interface structures of novel electronic materials for both traditional Si-based devices and rapidly growing GaN-based high temperature, high frequency, and high power devices. The conclusions were then split in two parts, one for high-K dielectrics, and the other for GaN-based systems.

5.1 High-K Dielectrics

We have demonstrated that amorphous LaScO$_3$ film can be grown on Si at low temperature 100 °C with a 3.5 nm thick interfacial layer. The bulk film for as-grown sample was close to be stoichiometric and became polycrystalline at 800 °C. The interfacial layer was oxygen rich after post-annealing, depending on the annealing temperature and oxygen sources. The 3.5 nm thick interfacial layer remained amorphous up to 1000 °C. So amorphous LaScO$_3$ (≤3.5 nm) can be deposited directly on Si substrate as gate dielectric for CMOS devices. However, oxygen diffusion through the thin LaScO$_{3+x}$ film and reaction with Si substrate increased the EOT and the interface roughness at 1000 °C. So possible oxygen sources at 1000 °C need to be eliminated, for example, by choosing right metal gate or capping layer materials.

As to the high-K La-silicate layer on Si, we also studied the interface structure and the chemical composition in detail. The high-K layers kept amorphous even after annealing. The thickness creased only slightly for the annealed sample with UHV-W. Also this sample showed good interfaces with both the Si substrate and the TaN layer, although it was observed that there was slight reaction between the high-K layer and the TaN layer. The La-
O layer and the Si-O layer was shown to be alloyed well at high temperature anneal. All of these make the sample with UHV-W a good choice for the next generation gate dielectric. To the annealed sample with DC-W, the oxygen initially contained in the DC-W caused the rough interface between the high-K layer and the TaN layer, and gave rise to the SiOx layer between the high-K layer and the Si substrate. The chemical changes across the high-K layer were well determined. All these results give us a deep understanding about the promising La-based oxides as the next generation gate dielectrics.

5.2 GaN-based Systems

To the GaN films on c-sapphire with a LT-AlN nucleation layer, the 7.5:8.5 theory about misfit edge dislocations of LT-AlN on c-sapphire was confirmed. The theoretical threading dislocation density in AlN was derived to be $8.48 \times 10^{13}/\text{cm}^2$. The direct polarity determination of GaN was successfully realized for the first time. The interface atomic structure of LT-AlN on c-sapphire was determined. It was observed that the misfit edge dislocation plane was one Al-N monolayer above the interface plane. For the first time, we experimentally explained why LT-AlN layers can invert the polarity of GaN. Finally, the exact 3-D geometry of AlN pits was determined for the first time.

The GaN IDBs were also studied in detail. A transition region with mixed polarities was found with the CBED method. The transition region was related to the not well defined edge of the LT-AL. The 7.2:6.2 theory about misfit edge dislocations of GaN on c-sapphire was confirmed. The dislocation loops were observed experimentally, indicating the tress concentration around thread dislocations. The chemical reaction between GaN and sapphire at high temperature were identified. The reaction mechanism was proposed. The interface
structure of GaN on c-sapphire was determined for the first time. Like AlN on sapphire, the misfit edge dislocation plane was one Ga-N monolayer above the interface plane. For the first time, we also experimentally explained the N-face polarity of GaN directly grown on sapphire. Finally, a more accurate GaN IDB was proposed, which gives new insights for future work.