ABSTRACT

ZHANG, RENHUA. Electronic Defect Characterization of Strained-Si/SiGe/Si Heterostructure. (Under the direction of George A. Rozgonyi.)

A strained-Si layer grown on a SiGe buffer layer is a promising candidate to replace bulk Si for CMOS devices, because of the mobility enhancement for both electrons and holes, independent of geometric scaling. Despite intensive research efforts, there is still a lack of understanding of electrically-active defects within the top strained-Si layer, or at the strained-Si/SiGe interface, which are critical to CMOS device performance. This lack of understanding is mainly due to the very small thickness (tens of nm) of top strained-Si layer, rendering the conventional electrical junction based characterization tools ineffective.

In this thesis, a combination of electrical (*C*-*V*, DLTS, MCTS, and EBIC) and structural characterization techniques (preferential etching, and Nomarski optical microscopy) was employed to study strained-Si/SiGe/Si heterostructures with varying thickness of strained-Si layer, and to identify deep levels related to threading or misfit dislocations. Electrical characterizations were mainly performed using Schottky diodes of *p*-type heterostructures. To introduce strain relaxation and generate misfit dislocations at the strained-Si/SiGe interface, a 73.5-nm-thick metastable strained-Si layer (with a thickness larger than the critical value) was thermally annealed at 800 ºC in oxidizing atmosphere to grow a 10 nm thick oxide. This work consists of three parts. The first part of the study focused on defects within the graded SiGe layer, and identified dopant compensation and

temperature-dependent *C-V* characteristics, due to a high density of hole traps. The second part compared the electrical properties of as-grown and thermally-annealed 73.5-nm-thick strained-Si/$Si_{0.8}Ge_{0.2}$/Si heterostructures using *C-V*, DLTS and EBIC methods. Changes of charge carrier depth profiles and EBIC contrast after thermal annealing were attributed to the removal of dislocation-trail related defects within the SiGe layers by 800 ºC thermal annealing. In addition to the dislocation-trail defects, DLTS measurements identified a near-surface (less than 150 nm deep) extended defect formed after annealing, and related it to the formation and motion of misfit dislocations during the strain relaxation of top Si layer. The advantages of optically-excited MCTS technique for characterizing minority carrier (electron) trap levels located within the depletion region of a Schottky diode was demonstrated in the last part. One electron trap was observed for different as-grown samples, and the volume density of the electron trap scales linearly with areal threading dislocation densities measured by preferential etching/optical microscope. Thus, this electron trap is related to threading dislocation. The MCTS spectra of thermally-annealed 73.5-nm-thick strained-Si sample were analyzed and compared to the well-know electron traps of plastically deformed *n*-type Si. And the hole trap *H5* detected by DLTS was compared with the electron traps by MCTS, and related to the electron trap *D* of plastically deformed *n*-type Si, which becomes a hole trap due to the decrease of band gap from Si to $Si_{0.8}Ge_{0.2}$.

ELECTRONIC DEFECT CHARACTERIZATION OF STRAINED-Si/SiGe/Si HETEROSTRUCTURES

By

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To my parents and my wife

BIOGRAPHY

Renhua Zhang was born on January 8, 1979 in the Zhejiang province of P. R. China. He received his bachelor degree from Materials Science and Engineering Department of Tsinghua University, Beijing, P. R. China in June 2000. After graduation, he joined Dr. George A. Rozgonyi's Microelectronic Materials group at North Carolina State University. During the first three years of graduate school, he worked on the electrical and structural characterization of polycrystalline sheet silicon for photovoltaic applications, in collaboration with GE energy, formerly known as AstroPower. Afterwards, he focused on the electrical defect characterization of strained-Si/SiGe/Si heterostructures, and based his thesis on the application of various electrical characterization techniques for studying the top strained-Si layers.

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INTRODUCTION

During the last 40 years, the amazing performance improvements in CMOS integrated circuits are primarily driven by a continuous geometric scaling of individual MOSFET transistors. As the device dimensions approach <100 nm, geometric scaling becomes increasingly difficult. New materials that can improve the device performance are of great interest. Strained-Si grown on a relaxed $Si_{1-x}Ge_x$ buffer layer is becoming a promising candidate to replace traditional bulk Si in high-performance CMOS, because of the enhanced charge carrier mobilities for electrons and holes, as well as good compatibility to CMOS fabrication technology.

Nevertheless, there are still many materials issues to be addressed, which are essential to the successful application of the strained-Si CMOS technology. Although a metastable strained-Si layer can be epitaxially grown at relatively low temperatures to a thickness larger than the critical value predicted by Matthews-Blakeslee model, this metastable strained-Si layer can relax by the formation of misfit dislocations at the strained-Si/SiGe interface, and the rate of misfit dislocation formation increases exponentially with temperature. However, the CMOS fabrication process includes standard steps (e.g., activation of ion-implanted dopant species, and gate oxidation) requiring temperatures as high as 1000 ºC. Thus, it is critical to be able to measure the changes of tensile strain and misfit dislocations density during a high-temperature process.

Although various structural characterization methods (e.g., preferential etching, TEM, x-ray diffraction, Raman spectroscopy, etc.) have been successfully applied for studying the

strain relaxation and dislocation generation, there are limited efforts to study the electrical properties of the extended defects generated at the strained-Si/SiGe interface, particularly dislocation-related deep levels. It is obvious that the capability to detect dislocation-related deep levels is critical to studying or even controlling the introduction of threading and misfit dislocations, which can degrade the CMOS performance by increasing leakage current and reducing the carrier mobility. The lack of electrical characterization results is mainly due to the very small thickness (tens of nm) of top strained-Si layer, rendering the conventional electrical junction based characterization techniques ineffective. Therefore, an in-depth study of the electrically active defects within the strained-Si/SiGe/Si heterostructure, especially, the strained-Si/SiGe interface, is carried out using conventional techniques (*C*-*V*, DLTS, and EBIC), as well as the unusual one like MCTS. The thesis is organized as following:

Chapter 1 of "Literature Review" discusses the conventional growth process of strained-Si/SiGe/Si heterostructure and the reasons for carrier mobility enhancement. The recent structural and electrical characterization results of defects of the strained-Si/SiGe/Si heterostructure are included, and dislocation-related deep levels of plastically deformed *n*-type Si are reviewed.

Chapter 2 of "Research Methodology" briefly describes the electrical characterization techniques used in this study (*C*-*V*, DLTS, MCTS, and EBIC), and the basic concept of Schottky diodes for electrical testing. DLTS and MCTS are two powerful complementary tools for studying deep levels located in the upper and lower halves of the band gap of a semiconductor. EBIC with an e-beam of different energy can be used to study defects located at different depths from the surface.

Chapter 3 of "Carrier Depletion by Defects in the Graded SiGe Layer of

Strained-Si/SiGe/Si Heterostructure" focuses on the temperature-dependent *C-V* characteristics of Schottky diodes of strained-Si/SiGe/Si heterostructure, and identifies significant carrier depletion within the graded SiGe layer, which can be modeled as a capacitance C_R in parallel with resistance R. The agreement between the activation energy of resistance R and that of a hole trap level detected by DLTS indicates that the carrier depletion is caused by this defect level.

Chapter 4 of "Effects of Thermal Annealing on Deep-level Defects in Strained-Si/SiGe/Si Heterostructure" studies the effects of thermal annealing at 800 ºC in oxidizing atmosphere on the electrical properties of 73.5-nm-thick strained-Si/SiGe heterostructure using *C-V*, DLTS and EBIC methods. DLTS technique identified a deep level located within 150 nm from the surface, introduced by the strain relaxation of top Si layer during thermal annealing. The nature of this deep level is determined to be *localized* extended defect, i.e., point-defect clouds surrounding 60º dislocations from the dependence of DLTS signal on electrical filling pulse duration.

Chapter 5 of "Minority Carrier Transient Spectroscopy Study of Strained-Si/SiGe/Si Heterostructure" explores the applicability of MCTS technique for detecting defect levels located within the strained-Si layer, or at the strained-Si/SiGe interface, using a laser pulse to generate minority carriers within the depletion region of a Schottky diode. The observed minority carrier (electron) defect levels of as-grown and annealed samples are then compared with the well-known electron traps of plastically deformed *n*-type Si. One electron trap of as-grown sample is related to threading dislocations, and the high density electron traps of thermally-annealed metastable sample are attributed to point-defects located at or close to dislocations.

CHAPTER 1: LITERATURE REVIEW

1. 1. Strained-Silicon for Future CMOS

Strained-Si is a promising candidate to replace traditional bulk Si in deep submicron complementary metal-oxide-semiconductor (CMOS) technology, due to the higher carrier mobility. Also this outstanding material has very good compatibility to modern CMOS fabrication processes. Essentially, it is now well established that without changing the channel material, significant enhancements in device performance are possible using strained-silicon [1,2,3]. Thus, the strained-Si wafer shows great promise and rapidly approaches its practicality as an attractive candidate for fabricating high speed and low power CMOS devices.

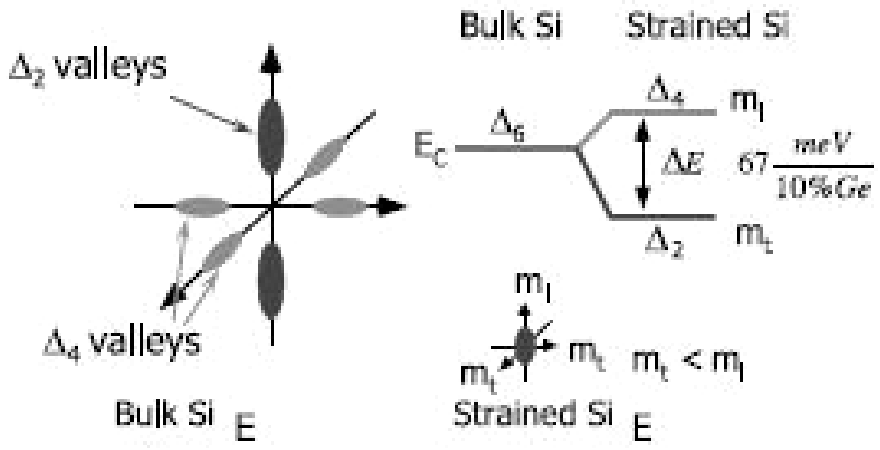

Figure 1-1. Schematic representation of the strain induced conduction band splitting in strained-Si [2].

Theoretically, the reasons for carrier mobility enhancement in strained-Si have been studied extensively [4,5,6,7]. The most commonly accepted explanation is that biaxial tensile

strain splits the six-fold degeneracy of the conduction band, and lowers the two-fold degenerate perpendicular Δ-valleys with respect to the four-fold in-plane Δ-valleys in energy space (see Figure 1-1 (a)). Such energy splitting suppresses inter-valley carrier scattering between the two-fold and four-fold degenerate valleys, and causes preferential occupation of the two-fold valleys, where the in-plane conduction mass is lower. These two effects lead to increased electron mobility.

In unstrained Si, the valence band maximum is composed of three bands: the degenerate heavy-hole (HH) and light-hole (LH) bands at k=0, and the split-off (SO) band which is slightly lower in energy (see Figure 1-2 (a)). Similarly, the biaxial strain splits the valence band degeneracy at the Γ-point and shifts the split-off band, and application of stress also changes the shape of the bands, as shown in Figure 1-2 (b) [8]. Therefore, due to the band deformation, the in-plane transport mass becomes smaller and the inter-band scattering is also suppressed. Thus the in-plane hole mobility is improved.

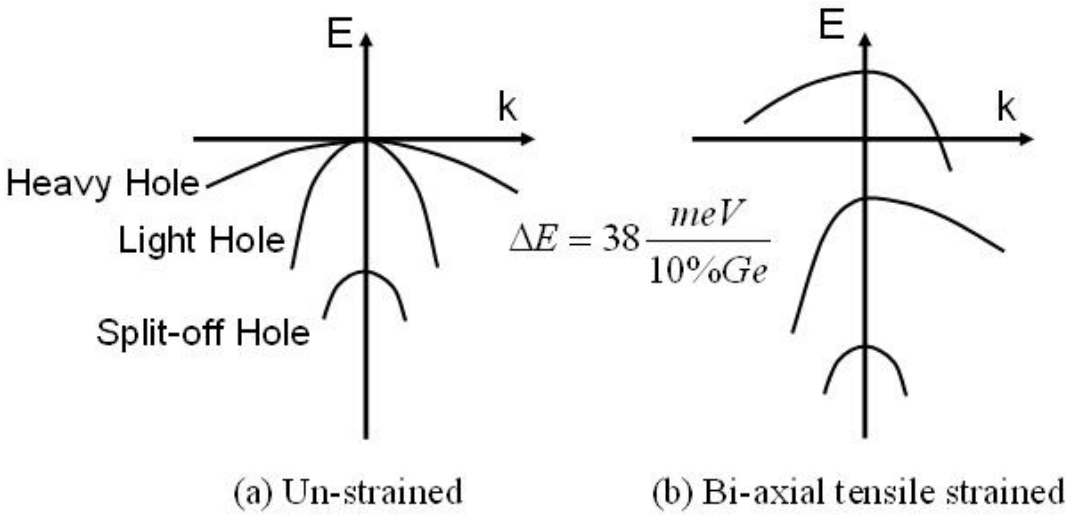

Figure 1-2. Simplified schematic of hole valence band structure for (a) unstrained and (b) bi-axial tensile strained-Si [9].

1. 2. Strained-Si Channel

Strain in Si channel can be introduced in various ways. The two main techniques to induce strain in a CMOS channel are global strain and local strain. Global strain requires a virtual substrate upon which a strained layer is epitaxially grown. On the other hand, local strain can be accomplished either by selectively growing pseudomorphic SiGe epitaxially in recessed source-drain regions surrounding the channel, or by depositing highly-stressed dielectric liners over the gate.

The focus of this thesis is on the electrical and structural properties of Si layer with global strain, i.e., biaxial strain.

1.2.1. Growth of Strained-Si/SiGe/Si-substrate Heterostructure

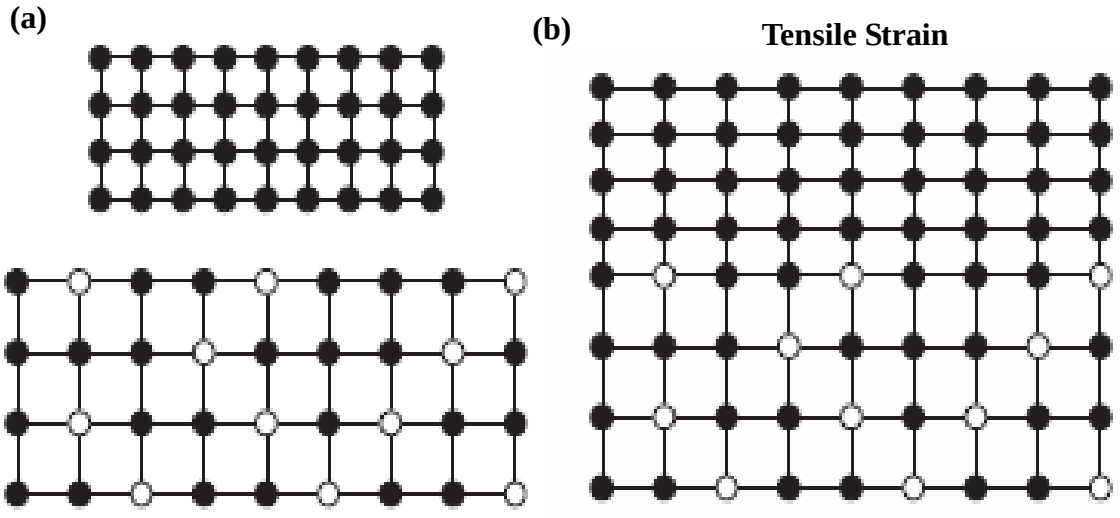

Figure 1-3. A schematic diagram of the bulk lattice constants of a bulk-Si film to be grown on top of a bulk-$Si_{1-x}Ge_x$ film (a), and one of the two films placed together with the top film being tensile strained (b).

The most commonly used method to induce global strain is to deposit a thin Si epitaxial

layer on top of a thick relaxed SiGe buffer layer [2]. Silicon and germanium, both of the diamond lattice structure, can form a continuous series of $Si_{1-x}Ge_x$ alloy with x ranging from 0 to 1. The lattice constants are 0.5431 nm for Si and 0.5657 nm for Ge. And the lattice constant a_{SiGe} for relaxed $Si_{1-x}Ge_x$ alloy could be calculated according to the Vegard's law:

$$a_{Si_{1-x}Ge_x} = a_{Si} \cdot (1-x) + a_{Ge} \cdot x \qquad \textbf{(Eq. 1. 1)}$$

Relaxed SiGe with 26% Ge has a crystal lattice parameter ~1% larger than that of Si. Therefore, when a thin layer of Si is pseudomorphically grown on a thick, relaxed SiGe layer, the lattice constant of the Si film conforms to that of the SiGe layer, and the lattice mismatch between Si and SiGe leads to ~1% biaxial tensile strain in the Si layer, as shown in Figure 1-3. The magnitude of the strain in the Si can be varied by changing the Ge content in the SiGe template.

1. 3. Performance Enhancement of Strained-Si CMOS Devices

Strained-Si metal-oxide-semiconductor field-effect-transistor (MOSFETs) are device structures that take advantage of strain-induced enhancement of carrier transport in silicon, and the typical structures of strained-Si/relaxed SiGe bulk MOSFETs are shown in Figure 1-4. Recent work has provided encouraging experimental data showing the mobility enhancement with different devices structures, including both *n*-channel and *p*-channel devices. The *n*-channel MOSFET mobility measured on large area, long channel devices are shown in Figure 1-5, showing that the mobility of the strained-Si device is ~70% higher than the universal MOSFET mobility or the mobility of the control Si device [10]. Fabrication processes such as source/drain extensions and halos, channel ion implantation, and associated

high temperature activation anneals are shown to have no adverse impact on device characteristics, suggesting that a conventional CMOS process flow can be adopted while still achieving the mobility and current drive enhancement.

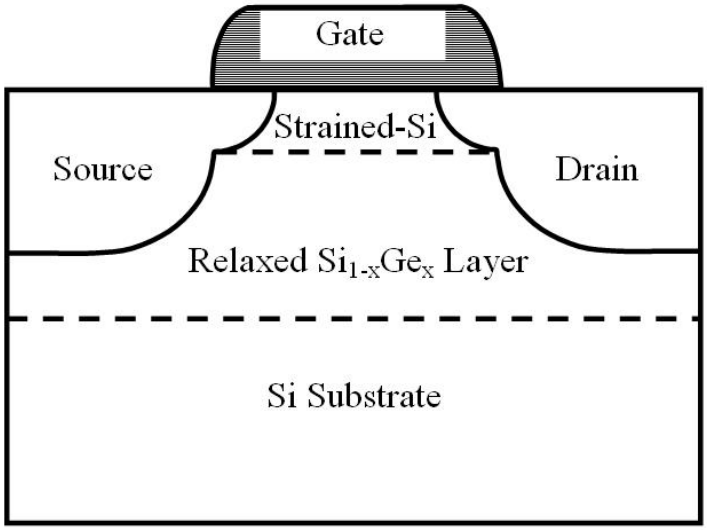

Figure 1-4. Typical structures of strained-Si/relaxed SiGe bulk MOSFETs [9].

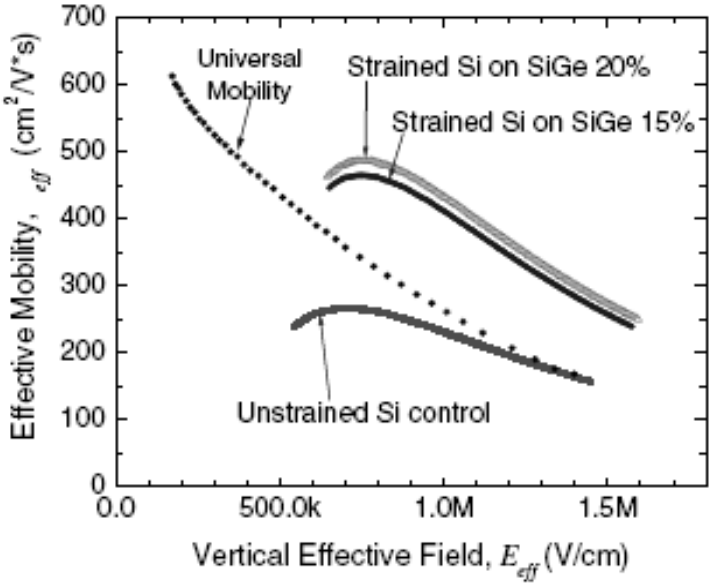

Figure 1-5. Effective electron mobility of strained-Si MOSFETs [10].

1. 4. Structural Characterization of Defects of Strained-Si/SiGe/Si Heterostructure

When producing strained layers for CMOS technology, constraints are imposed on the thickness, lateral dimensions and crystalline quality of the channel layer. The foremost critical challenge in the strained-Si/SiGe CMOS technology is the control of extended defects in the epitaxial layers: dislocations. The defects present in the SiGe buffer layer also grow into the strained-Si overgrown layer, and additional defects may be created in the strained-Si layer if the thickness of the layer exceeds the critical thickness value. Thermal processing during CMOS fabrication steps can cause relaxation of the strain in the Si layer, or out-diffusion of Ge, and should be monitored accordingly.

1. 4. 1. Defects Structure of SiGe Buffer Layer

The primary function of the relaxed SiGe layer is to serve as a "virtual substrate" for tensile-straining the top Si epilayer. In order to produce a relaxed SiGe epilayer with low threading dislocation densities on a Si substrate, the conventional method is to grow thick (a few μm) compositionally-graded buffer layers and a following layer of uniform SiGe. Mismatch strain is gradually relaxed by a modified Frank–Reed (MFR) mechanism [11,12], and the majority of 60° misfit dislocations (MDs) formed during the relaxation process are trapped within the SiGe graded layer, as shown in Figure 1-6. These buried dislocations should not greatly degrade MOSFET device performance at the strained-Si surface.

Some of these MDs, with a density of 10^5–10^6 cm^{-2}, may thread to the MOSFET device region at the surface, and thus these threading dislocations (TDs) must be controlled.

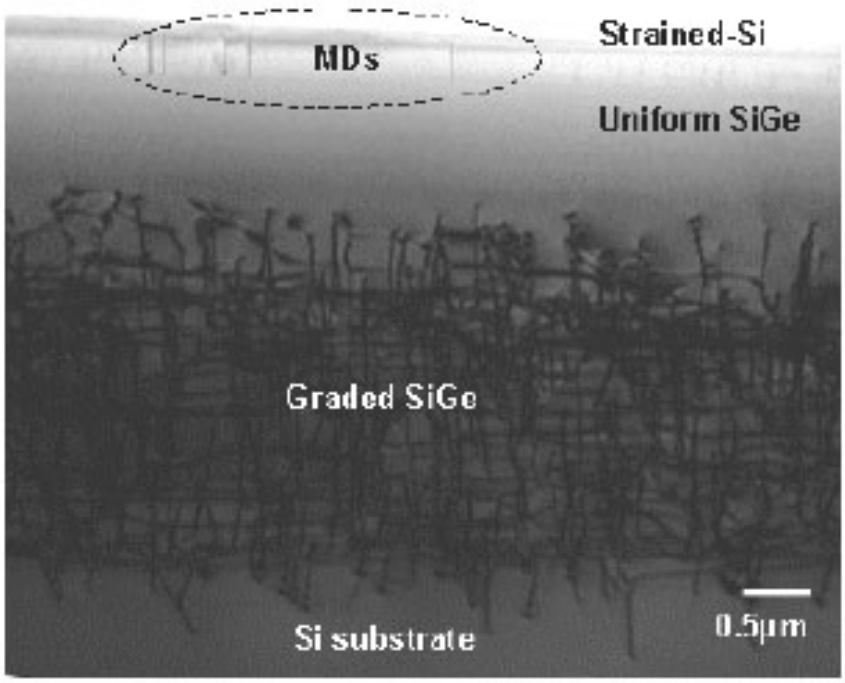

Figure 1-6. Cross-sectional TEM image of a strained-Si/SiGe heterostructure [13]. Most of the dislocations are confined within the SiGe graded layer, while some misfit dislocations are generated at the interface of strained-Si and uniform SiGe layers.

1. 4. 2. Defects Structure of Strained-Si Top Layer

The choice of channel thickness in strained-Si MOSFETs is an important one. For the strained-Si layer with a thickness in the thinnest regime of ~5 nm, carrier confinement will decrease with decreasing thickness due to quantum effects. This poor confinement in the Si channel leads to carrier conduction through the low-mobility relaxed SiGe buffer layer, and degrades the overall device mobility [14]. In addition, thinner strained-Si layers are more susceptible to Ge diffusion at high temperatures. For practical purposes, it is desirable to have a strained-Si thickness of >15 nm, because 8-10 nm of the initial Si is typically consumed during various CMOS fabrication steps (e.g., surface cleans, Ge diffusion, and gate oxidation).

1.4.2.1.Critical Thickness of Strained-Si Layer

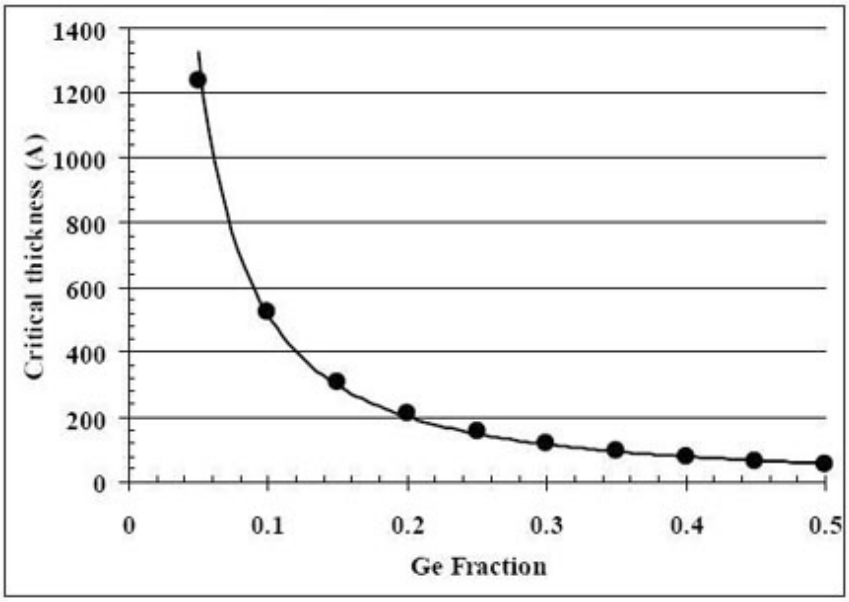

Figure 1-7. Critical thickness h_c of a silicon layer grown on a fully-relaxed $Si_{1-x}Ge_x$ layer as a function of the germanium content x [22].

The lattice mismatch between Si and relaxed $Si_{1-x}Ge_x$ is ~4.2% x, where x is the Ge content in the $Si_{1-x}Ge_x$ layer. Since the lattice mismatch is sufficiently small, the deposited first several atomic layers of Si will be strained to match the SiGe substrate and a coherent interface will be formed. The strained-Si/SiGe heterostructure stores a high amount of elastic strain energy, since the inter-atomic bond lengths in the epilayer are stretched or compressed compared to their equilibrium values. At some thickness of an epilayer, generally called the critical thickness h_c, it becomes energetically favorable to relieve the elastic strain energy by introducing misfit dislocations and allowing the epilayer to relax towards its bulk lattice constant. This critical thickness has been calculated by several groups based on different models [15,16,17,18,19,20,21]. Figure 1-7 shows the calculated critical thickness of strained-Si layer grown on a fully relaxed SiGe as a function of Ge content, displaying an

exponentially decreasing value of the critical thickness with increasing strain, i.e., Ge content [22].

As mentioned in Section *1.4.2*, strained-Si thickness needs to be larger than 15 nm for practical purposes. Meanwhile, charge carrier mobilities of strained-Si grown on $Si_{1-x}Ge_x$ virtual substrates are theoretically predicted and experimentally demonstrated to increase with higher Ge content because of a larger tensile strain, and saturate upon reaching a Ge content of 25% for electrons [23,24,25], or 40% for holes [26,27,28,29], as shown in Table 1-1. Thus there is a strong motivation to increase Ge content to the value of 40% to achieve maximum carrier mobility enhancement of CMOS devices comprising of both *n*- and *p*-MOSFETs. Since the combination of desired strained-Si layer thickness and Ge content exceeds the theoretical curve of the critical thickness h_c as a function of Ge content x, the critical thickness value becomes a restriction to the design of Si layer thickness and Ge content for strained-Si/SiGe/Si MOSFETs. And the study of possible strain relaxation and dislocation formation of a metastable strained-Si layer with a thickness exceeding h_c becomes necessary to fully benefit from the strained-Si/SiGe/Si MOSFET architecture.

Table 1-1. Theoretical predicted values of low-field electron [23] and hole [26] mobility enhancements of strained-Si layer grown on relaxed $Si_{1-x}Ge_x$ layer, relative to the mobility values of un-strained bulk-Si.

x	0.1	0.2	0.3	0.4	0.5
electron	1.46	1.68	1.70	1.70	1.70
hole	1.25	1.68	2.35	2.53	2.55

1.4.2 2. Strain Relaxation and Defect Formation for Strained-Si Layer

Many groups have studied the strain relaxation and the associated defect formation using

structural analysis techniques, e.g., preferential chemical etching, atomic force microscopy, and transmission electron microscopy. It was generally accepted that TDs will glide as soon as the thickness of the overgrown strained-Si exceeds the critical thickness h_c, and result in the formation of MDs at the strained-Si/SiGe interface, according to the Matthews and Blakeslee model [16,19]. Recent studies observed that dislocations may form in the strained-Si layers even when the layer thickness is less than the predicted h_c, via the nucleation of dislocation half-loops, in addition to the gliding of pre-existing threading dislocations [21]. The threading dislocations connected to the misfit dislocations at the upper interface may extend into the upper part of the constant SiGe layer, as shown Figure 1-6. Furthermore, stacking faults were identified for the supercritical strained-Si layer, and related to the gliding of partial dislocations [30,31]. Selective strain relaxation of strained-Si layer was also verified by studying the strain fluctuation in the strained-Si/relaxed-SiGe heterostructure using micro-Raman spectroscopy [32].

1. 5. Electrical Characterization of Defects of Strained-Si/SiGe/Si Heterostructure

1. 5. 1. Electrical Properties of Dislocated Si/SiGe/Si Layered Structures

The detrimental effects of dislocations on the electrical performance of devices fabricated using Si/SiGe/Si heterostructures have been studied extensively. A correlation between junction leakage current density and threading dislocation density (TDD) has been established for both *p*-*i*-*n* diodes of $Si_{0.75}Ge_{0.25}$ graded buffer layers [33] and n^+/p-junctions of strained-silicon/relaxed $Si_{0.8}Ge_{0.2}$ [34]. The leakage was demonstrated to scale linearly with the TDD, and can be modeled by deep-level assisted generation processes.

In addition, the effects of MDs on the characteristics of electronic devices were

studied by measuring the leakage current of a metastable SiGe/Si *p-n* junction during heating while monitoring the dislocation densities with *in-situ* TEM [35], or by comparing the off-state leakage currents of strained-Si MOSFETs with various strained silicon thicknesses (above or below the critical thickness) [36]. Thus, the increase of leakage current due to the higher misfit dislocation density has also been established, and the leakage mechanism between source/drain contacts of strained-Si MOSFET was further studied using photon emission microscopy, and shown to be the enhanced dopant diffusion near misfit dislocations, as shown in Figure 1-8 [36].

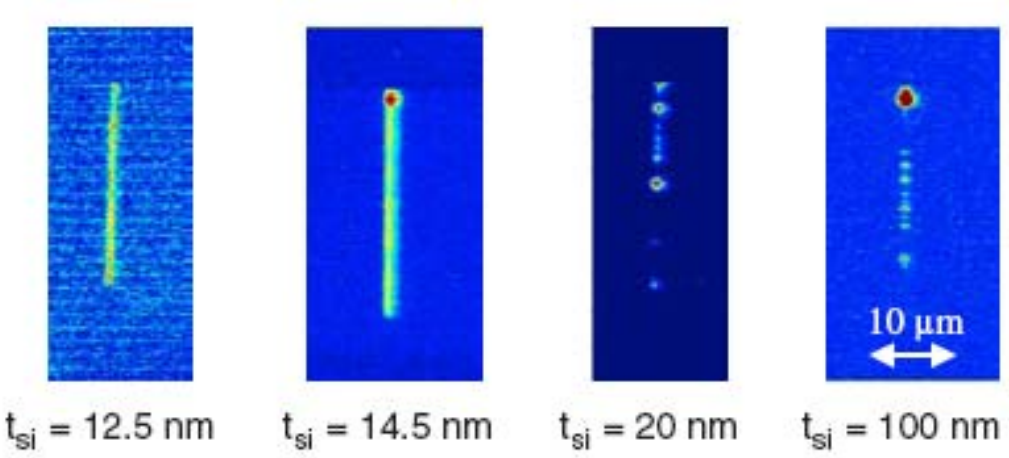

Figure 1-8. Photon emission microscopy images of light emission from strained-silicon MOSFETs with varying strained-Si layer thickness. The differences between light emission for different strained-Si thickness supports the hypothesis that misfit dislocation diffusion pipes cause source/drain shorts [36].

Furthermore, the introduction of misfit dislocations at the strained-Si/SiGe interface will substantially degrade the expected mobility enhancement of strained-Si layer. In addition to the mobilities reduction due to the loss of tensile strain, misfit dislocations also induce a strong scattering potential close to the carriers in the strained-Si, and disadvantageously affect the carrier mobilities [37].

In short, the introduction of dislocations (TDs or MDs) within, or even close to the strained-Si top layer would be detrimental to the final strained-Si MOSFETs device performance, by lowering the charge carrier mobility, as well as increasing the off-state leakage currents. Hence, it is essential to perform both structural and electrical characterizations of dislocations at the strained-Si/SiGe interface, and especially desirable to be able to non-destructively detect the strain-relaxation of metastable strained-Si layer during the CMOS fabrication process.

The device performance enhancement due to higher carrier mobilities, and the possible degradations because of extended defects have also been mentioned in the most recent 2004 *International Technology Roadmap for Semiconductors* (ITRS) published by the Semiconductor Industry Association (SIA), as shown in Table 1-2 of the information related to strained-Si MOSFETs [38].

Table 1-2. The information related to strained-Si MOSFETs in 2004 *International Technology Roadmap for Semiconductors* (ITRS) [38].

Transport-enhanced MOSFETs	Advantages	Potential Weakness
Strained Si, Ge, SiGe, SiGeC or other semiconductor; on bulk or SOI	High mobility without change in device architecture	Material defects and diode leakage; Process compatibility and thermal budget.

1. 5. 2. Electrical Defect Characterization of Dislocations in Strained-Si Top Layer

So far, several studies have been done concerning the defect states within the strained-Si top layer employing electrical characterization tools [39,40].Yuan *et al.* have demonstrated that electron-beam-induced current (EBIC) technique can be used to investigate MDs at the strained-Si/SiGe interface of 100-nm-thick strained-Si/$Si_{0.8}Ge_{0.2}$/Si with a Schottky

contact [39]. Misfit dislocations were intentionally introduced to the top strained-Si layer by growing the strained-Si layer to a thickness larger than the critical thickness. Misfit dislocations located at different depths (at the strained-Si/SiGe interface, or within the graded SiGe layer) can be differentiated by using e-beam of different energy for EBIC measurements. For an e-beam of 4 keV (or 20 keV), the electron range R_e is calculated to be 320 nm (or 3.5 μm), meaning that the volume of generated electron hole pairs contains either only strained-Si and constant SiGe layers for 4 keV, or strained-Si constant and graded SiGe layers for 20 keV. Figure 1-9 illustrates typical EBIC micrographs taken with an e-beam of 4 keV at 300 K (a) and 65 K (b), or with an e-beam of 20 keV at 300 K (c) and 65 K (d), respectively. Low-temperature EBIC micrograph of strained-Si and constant SiGe layers (Figure 1-9(b)) shows two orthogonal sets of dark lines oriented along ⟨110⟩ directions and some dark dots, originating from the misfit and threading dislocations at the strained-Si/SiGe interface; while low-temperature EBIC micrograph of the graded SiGe layer (Figure 1-9(d)) shows a dense orthogonal dark line pattern of the dense dislocation network.

Since little or no EBIC contrast is observed on the same sample region at 300 K (see Figure 1-9(a) and (c)), the energy level of observed dislocations could be estimated to be shallow levels according to the Shockley–Read–Hall recombination model [41,42].

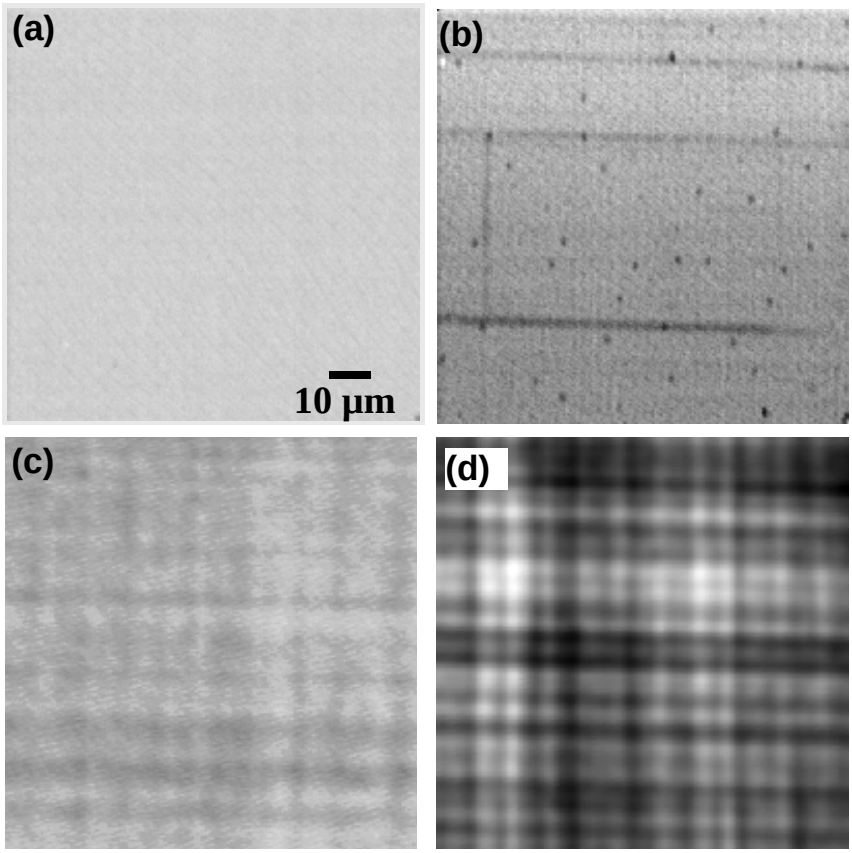

Figure 1-9. EBIC micrographs of 100-nm-thick strained-Si/$Si_{0.8}Ge_{0.2}$/Si heterostructure: (a) 4 keV at 300 K; (b) 4 keV at 65 K; (c) 20 keV at 300 K; (d) 20 keV at 65 K [39].

Wang *et al.* used DLTS and metal-oxide-semiconductor (MOS) transient capacitance methods to evaluate the interface states density of both oxide/strained-Si and strained-Si/SiGe interfaces and minority carrier generation lifetime of a MOS structure, respectively [43]. It was found that interface state density is independent on the thickness of strained-Si, and strongly increases with higher Ge content of SiGe layer. On the other hand, minority carrier generation lifetime shows an obvious dependence on both strained-Si thickness and Ge content.

1. 5. 3. Dislocation-related Deep Levels

Despite the obvious importance of studying dislocation-related deep levels within the strained-Si/SiGe/Si heterostructure, there is still a lack of understanding of the electrically-active defects located within the top strained-Si layer, or at the strained-Si/SiGe interface, critical to the optimum performance of final MOSFETs. This situation is mainly due to the very small thickness (tens of nm) of top strained-Si layer, rendering the conventional electrical junction based characterization tools ineffective. For this reason, this thesis focuses on the electronic defect characterization of strained-Si/SiGe/Si heterostructure, employing a combination of electrical (*C-V*, DLTS, MCTS, and EBIC), and structural (preferential etching/Nomarski optical microscopy) characterization techniques.

Although no direct results on the defect states within the strained-Si layer are available in the literature, there are extensive works on plastically deformed Si and SiGe/Si heterostructure, producing a large body of results about dislocation-related deep levels in Si or SiGe. Since both strain-relaxation of metastable strained-Si layer and plastic deformation of bulk Si involve the generation of dislocations, the previous extensive work on plastically deformed Si will be used as references for the discussion of defects detected in the strained-Si/SiGe/Si heterostructure. In the following, the deep levels of plastically deformed Si will be briefly mentioned.

1.5.3.1 Defect states in plastically deformed silicon

DLTS has been extensively applied to plastically deformed silicon to study the electronic properties of a complex spectrum of extended defects by several groups [44,45,46,47,48]. Typically, a Si sample bar is plastically deformed by creep (four-point bending)

along the [112] direction in a forming gas atmosphere (92% N2 and 8% H2) using a quartz and graphite deformation apparatus. The resulting plastic strain ranges from 1% to 1.5%. In addition to dislocations, a large amount of point defects and point-defect clusters are introduced through the dislocation motion or interaction, during the plastic deformation process. Consequently, both donor and acceptor states are generated within the band gap, due to these electrically active lattice imperfections. The complex defect spectrum of plastically deformed *n*-type Si has been identified as four traps, labeled *A*, *B*, *C*, and *D*, mainly based on the extensive work on the formation and annealing behaviors of different defects [45, 48], as shown in Figure 1-10, and their characteristic parameters are reported in Table 1-3.

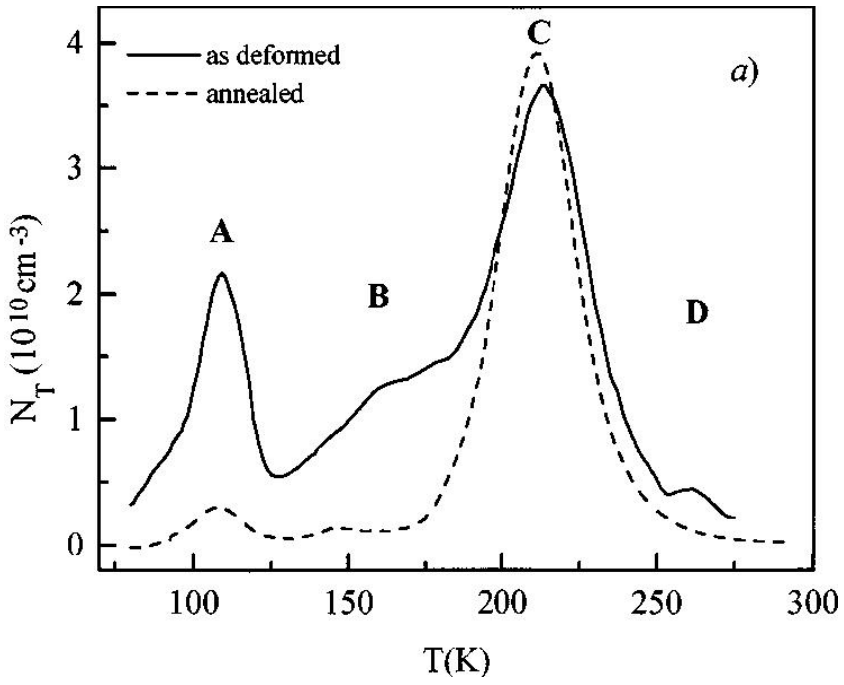

Figure 1-10. DLTS spectra of a plastically deformed *n*-type Si with a dislocation density of 10^4 cm^{-2}, before (solid line) and after (dashed line) thermal annealing at 850 ºC for 1 h [48].

Table 1-3. Electrical parameters of electron traps in plastically deformed *n*-type silicon, including trap energy level within the energy band gap, and capture cross section [45,48].

Trap	E_a (eV)	σ_n (cm^2)
A	0.19	
B	0.29	1.5×10^{-16}
C	0.40	8.9×10^{-16}
D	0.56	

Moreover, several unique properties of dislocation-related defect states have been identified using DLTS technique, and will be briefly mentioned in the following:

(1) Dislocations are spatially extended defects, and consequently they can change their charge state within wide limits by capturing or emitting many electrons.

(2) Due to the strain field associated with dislocations, the capacitance transients are often non-exponential, resulting in broadened DLTS peaks.

(3) Coulomb interaction among charges confined at the dislocation results in a time-dependent Coulomb barrier $\Phi(t)$, which builds up during the capture process of charge carriers. The presence of the Coulomb barrier around the dislocation causes the ‘‘logarithmic filling time dependence’’ of extended defects, and the local band bending may also induce a shift of the dislocation level with respect to the Fermi level, during filling and emptying of the traps.

After extensive studies on the formation and annealing behaviors of different defects, as well as computer simulations, the general conclusion about the origin of the deep levels of plastically-deformed *n*-type Si detected by DLTS technique is that the electrical properties are mainly due to point defect effects, not the dislocation core structure. And more specifically, trap *A* was identified with point-defect clusters related in some way to dislocation motion.

Trap *B* and *D* are thermally unstable deformation-induced point defects not necessarily localized at dislocations. Trap *C* could be related to point-defect clouds, with a radius of ~ 1 nm, surrounding 60º dislocations [47].

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CHAPTER 2: RESEARCH METHODOLOGY

2. 1. Introduction

In this thesis, various structural and electrical characterization methods were employed to study different aspects of the strained-Si/SiGe/Si heterostructures, with focuses on the top strained-Si layer. Threading and misfit dislocations were delineated using preferential etching, and observed by a Nomarski optical microscope. Plan-view and/or cross-sectional transmission electron microscopy (TEM) were used to study the distribution of dislocations within the heterostructures.

The focus of this study is the electronic defect characterization of trap levels related to the top strained-Si layer. For the graded-SiGe layer, temperature- and frequency-dependent capacitance-voltage (*C*-*V*) measurements were employed to study the effects of high density of dislocations on the capacitance values of Schottky diodes fabricated using strained-Si/SiGe/Si heterostructures. Deep-level transient spectroscopy (DLTS) and minority carrier transient spectroscopy (MCTS) are two powerful complementary tools for studying deep levels located in the upper and lower halves of the band gap of a semiconductor. MCTS technique uses laser pulse to excite minority carriers within the depletion region of a Schottky diode to fill trap levels, and then monitor the emission of minority carriers from the trap levels when the laser is turned off. Thus MCTS is well suited for studying near-surface defects (e.g., the strained-Si/SiGe interface). Electron-beam induced current (EBIC) using an e-beam of different energy can be used to detect defects located at different depths from the surface, and can be used to separate the defect levels related to the top strained-Si layers and deeper graded SiGe layer. This chapter briefly describes the electrical characterization techniques and

experimental procedures employed in this study.

2. 2. Schottky Barrier Diodes

When a metal and a semiconductor are brought into intimate contact with each other, a rectifying contact (Schottky barrier diode) can be formed. An energy barrier (Schottky barrier) arises due to the difference in the work functions of the metal and semiconductor. Though the details of Schottky barrier formation are not yet fully understood, it was pointed out that imperfections at the semiconductor surface (surface states) play an important role in determining the barrier height, which is relatively independent of the work function of the metal [1]. As a result of the equilibration of Fermi levels in both materials, a semiconductor region depleted of free carriers forms near the contact, and this depletion region or space charge region (SCR) is accompanied by a band bending due to the ionized dopant impurities.

Using the thermionic emission theory and neglecting series and shunt resistance, the Schottky barrier current-voltage characteristics are described by

$$I = I_S\left(\exp\left(\frac{qV}{n_I kT}\right) - 1\right), \qquad \textbf{(Eq. 2. 1)}$$

where I_S, the dark saturation current, is given by

$$I_S = AA^*T^2 \exp\left(-\frac{q\Phi_B}{kT}\right). \qquad \textbf{(Eq. 2. 2)}$$

Here, q is the charge of an electron, A is the diode area, A^* is the effective Richardson's constant, n_I represents the ideality factor and Φ_B is the Schottky barrier height.

By applying the depletion approximation as a boundary condition to the Poisson

equation, the following equations relating to the depletion width and free carrier concentration can be derived:

$$\frac{d\left(1/C^2\right)}{dV} = -\frac{2}{q\varepsilon_s\varepsilon_0 A^2 N_B}, \qquad \textbf{(Eq. 2. 3)}$$

$$W = \frac{\varepsilon_s\varepsilon_0 A}{C}, \qquad \textbf{(Eq. 2. 4)}$$

where ε_s is the dielectric constant of the semiconductor, ε_0 is the permittivity of free space, C is the capacitance, N_B (=N_A or N_D, depending on doping type) is the free carrier concentration and W is the depletion width.

The above two equations are only applicable to semiconductors in which the deep level trap concentrations are relatively low in comparison to the dopant concentration. If there are traps present in sufficiently high concentrations, the measured free carrier profiles are no longer representative of the dopant concentration since the deep levels are able to contribute to the measured capacitance.

2. 3. Capacitance-Voltage (*C*-*V*) Measurement

The capacitance-voltage measurement is a fundamental but very important technique to assess the electrical properties of a dielectric film or a device. Capacitance can be defined as the change in the charge amount, dQ, due to a change in the voltage, dV:

$$C = \frac{dQ}{dV}. \qquad \textbf{(Eq. 2. 5)}$$

This method is known as differential or small signal capacitance. Most capacitance measurements are made with capacitance meters or capacitance bridges, by

superimposing a small-amplitude ac voltage v on the dc voltage V, as a change of voltage. Capacitance meters assume the device under test (DUT) to be represented by either the parallel equivalent circuit in Figure 2-1 (a) or the series equivalent circuit in Figure 2-1 (b).

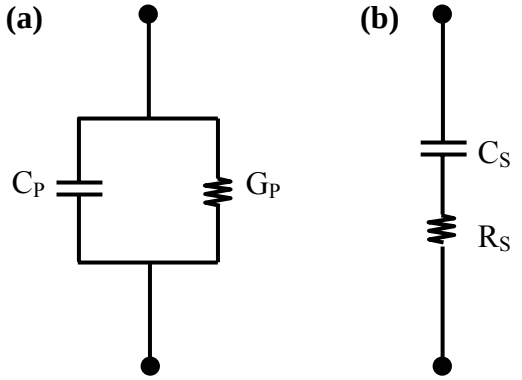

Figure 2-1. (a) Parallel equivalent circuit, and (b) series equivalent circuit of a device under test (DUT) for the measurement using capacitance meters.

For the DUT represented by a parallel equivalent circuit (see Figure 2-2), an ac signal v_i is applied to the DUT and the device impedance Z is calculated from the ratio of v_i to the sample current i_i. In the vector voltage-current method, the ac voltage typically varies at frequencies of 10 kHz to 1MHz with amplitude of 10 to 20 mV. Since the high input impedance of a high-gain operational amplifier allows no current through ($i_i \approx i_o$), the amplifier with a feedback resistor R_F operates as a current-to-voltage converter: $i_o = -v_o/R_F$. Since $i_i = v_i/Z$, the device impedance can be derived from v_o and v_i as

$$Z = -\frac{R_F v_i}{v_o}. \qquad \textbf{(Eq. 2. 6)}$$

For the parallel equivalent circuit in Figure 2-2, the device impedance of the is given by

$$Z = \frac{G}{G^2 + (\omega c)^2} - \frac{j\omega C}{G^2 + (\omega C)^2}, \qquad \textbf{(Eq. 2. 7)}$$

where C is the equivalent parallel capacitance, G is the equivalent parallel conductance, and the testing angular frequency $\omega = 2\pi f$. The device impedance consists of a conductance and a susceptance, respectively. Furthermore, the voltages v_o and v_i are fed to a phase detector and the conductance and susceptance of the sample are obtained by using the 0º and 90º phase angles of v_o referenced to v_i. The 0º phase angle gives the conductance G while the 90º phase angle gives the susceptance or the capacitance C.

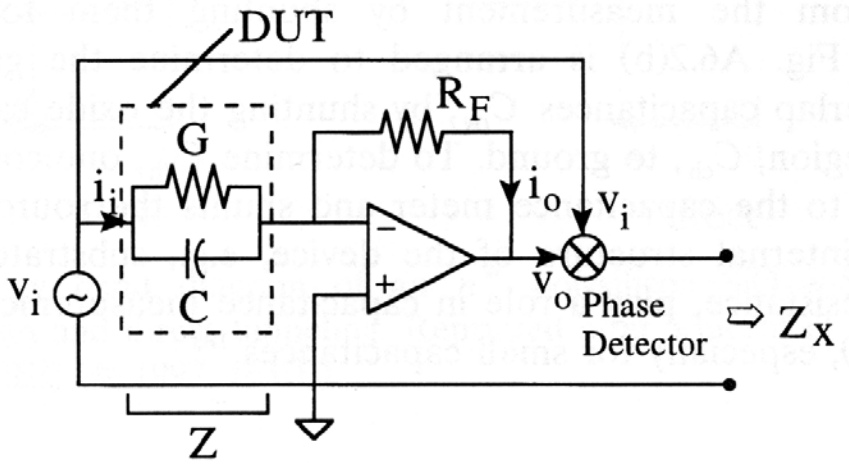

Figure 2-2. Schematic circuit diagram of a capacitance-conductance meter [2].

2. 4. Deep-Level Transient Spectroscopy (DLTS)

For an ideal Schottky barrier diode of *p*-type silicon under the depletion approximation, there is no possibility of carrier capture. Thus only the emission process can be observed, which can only happen through the forced introduction of carriers, by applying a voltage bias pulse. When carriers leave the filled deep states due to an external influence, a capacitance transient can be observed. In this section, only one-sided junctions or Schottky barrier

structures will be considered.

2. 4. 1. Capacitance Transient

Let us consider a deep level hole trap situated at an energy E_T within the semiconductor band gap with a concentration of N_T states per unit volume. Figure 2-3 (a)-(c) illustrate the capture and emission processes of majority carriers (holes are symbolized by open circles) by this deep level, when the voltage bias of the Schottky diode is pulsed. Initially, the device is under reverse bias V_R. In this condition, no mobile carriers are present in the SCR of width W. The deep level states within the band gap in that region are therefore empty (or filled with electrons) as symbolized by the filled circles.

Immediately after an injection pulse towards zero bias, the SCR decreases and majority carriers are then available for capture. The filled majority carrier traps are represented by the open circles.

Once the injection pulse is switched off and the device returned to its initial state, the junction capacitance is reduced due to the trapped majority carriers compensating the immobile charged states in the SCR. These carriers can be excited into the valence band E_V, and swept away from the SCR by the applied voltage potential, provided there is sufficient excitation energy to stimulate such transitions. This excitation energy can either be in the form of thermal or optical energy. The emission rate e_p of a hole from a deep level at a temperature T is described by

$$e_p = \sigma_p T^2 K \exp\left(-\frac{E_T - E_V}{kT}\right). \qquad \textbf{(Eq. 2. 8)}$$

Here σ_p is the hole capture cross-section, k is the Boltzmann constant, and K is a material coefficient which is dependent on both doping types and semiconductor materials.

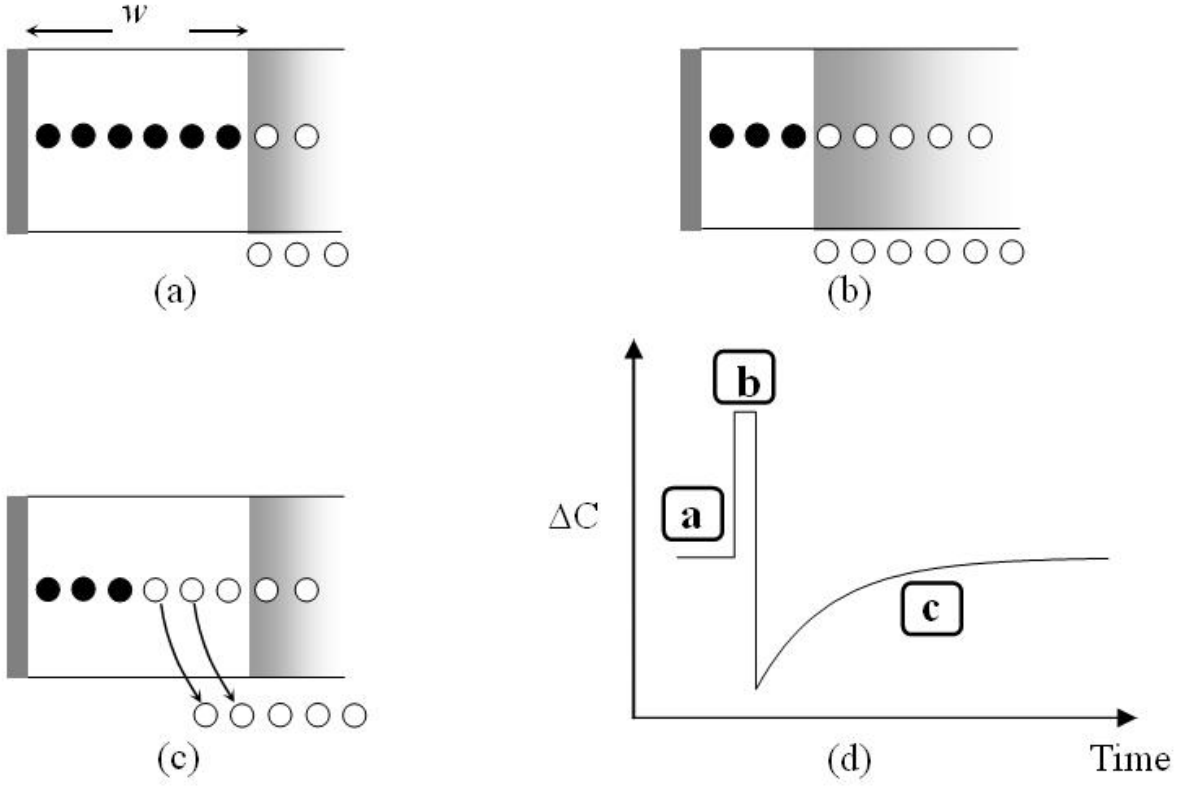

Figure 2-3. Capacitance transient of a majority carrier trap (hole trap in this case) in a *p*-type Schottky barrier diode. The diode (a) is under reverse bias V_R, (b) injected with a filling pulse V_P, and (c) is again at V_R where the carriers are emitted by the majority carrier trap [3].

The resulting junction capacitance can then be expressed by an exponential time-varying function as

$$C(t) = C(0)\exp\left(-\frac{t}{\tau}\right) = C(0)\exp\left(-t \cdot e_p\right), \qquad \textbf{(Eq. 2. 9)}$$

where τ is the emission time constant and is equal to the inverse of the emission rate e_p, and

$C(0)$ is the capacitance at $t = 0$, the instant the forward pulse is switched off and the capacitance transient begins.

The capacitance transient forms the basis of the DLTS technique, and can be used to extract the electronic properties of deep levels.

2. 4. 2. DLTS Signal Using a Rate Window

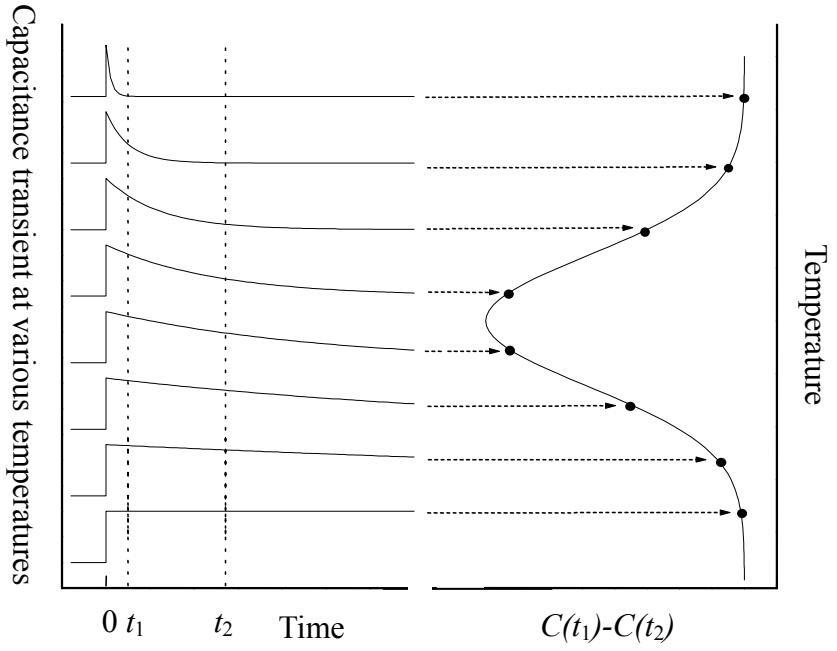

Figure 2-4. Illustration of how a double boxcar integrator is used to define the emission rate window. The output is the average difference of the capacitance amplitudes at the sampling times t_1 and t_2. The right-hand part of the figure is the so-called DLTS spectrum [4].

The main feature of the DLTS technique is the employment of an instrument to set an emission rate window such that the instrument produces a maximum signal output proportional to the defect concentration when the emission rate of carriers from the trap falls within the set rate window. To produce what is commonly known as a DLTS spectrum, the

diode is set at a reverse bias V_R on top of which is superimposed a continuous train of positive filling pulses V_P, while the temperature T is ramped. When the carriers have enough thermal energy, emission from the trap will take place. Figure 2-4 illustrates how the original rate window, using a double boxcar, was implemented [4]. The boxcar samples the capacitance at two fixed times t_1 and t_2 after the start of the capacitance transient, and determines the corresponding change in the capacitance ΔC. The emission rate time constant τ of the carriers from the defect is varied by changing the temperature.

A maximum appears in the ΔC output at a certain temperature T_{max}, when τ is related to t_1 and t_2 through the formula

$$\tau = \frac{t_2 - t_1}{\ln(t_2 / t_1)}. \qquad \textbf{(Eq. 2. 10)}$$

T_{max} is unique for each trap at a given τ. By performing further temperature scans using different rate windows, a set of T_{max} corresponding to each τ for the same trap can be generated.

By rearranging Eq. 2.8, one obtains

$$\ln\left(\frac{T_{\max}^2}{e}\right) = \ln\left(T_{\max}^2 \cdot \tau\right) = \frac{E_a}{kT_{\max}} - \ln(K\sigma_p), \qquad \textbf{(Eq. 2. 11)}$$

where E_a and σ_p represents the apparent activation energy and apparent capture cross-section, respectively. Thus, an Arrhenius plot can then be produced from this set of values, to extract the values of apparent activation energy and capture cross-section of a deep level, as the "signature" of the defect.

2. 4. 3. Determination of Concentration of Trap Level

The concentration of a specific trap can be directly determined by observing the change in capacitance as a function of the region being sampled. If the doping profile N_A and trap level concentration N_T are spatially uniform for *p*-type material, and N_T is much lower than N_A, then the defect concentration N_T is given by the following approximation

$$N_T = 2N_A \frac{\Delta C}{C} \frac{W_R^2}{(W_R - \lambda)^2 - (W_P - \lambda)^2}, \qquad \textbf{(Eq. 2. 12)}$$

where ΔC is the capacitance transient amplitude (given by the height of a DLTS peak), and C is the capacitance under the applied reverse bias voltage V_R. W_R and W_P are the depletion region widths for the reverse bias (V_R) and the filling pulse (V_P) voltages, respectively. λ is the length of the transition region in the depletion region where the deep level lies above the Fermi level.

To a first approximation, if we can further assume that $\Delta C << C$, and $\lambda << W_P$ (all traps are completely filled during the filling pulse), then the defect concentration N_T is given by

$$N_T \approx \frac{\Delta C}{C} \times 2N_A. \qquad \textbf{(Eq. 2. 13)}$$

This equation typically underestimates the true trap density since the pulse used to fill the traps does not encompass the entire depletion region.

2. 5. Minority Carrier Transient Spectroscopy (MCTS)

DLTS technique employing electrical pulsing is limited to the characterization of defect states in only one half of the band gap. To study the defect states throughout the whole band gap, minority carrier transient spectroscopy (MCTS) was originally developed by Brunwin *et*

al. [5]. Laser pulse with photon energy greater than the band gap ($hv > E_g$) is directed to a semitransparent Schottky barrier diode to generate electron-hole pairs within the semiconductor. Figure 2-5(a) shows the band diagram of a semi-transparent Schottky barrier diode on a *p*-type semiconductor with a reverse bias of V_R.

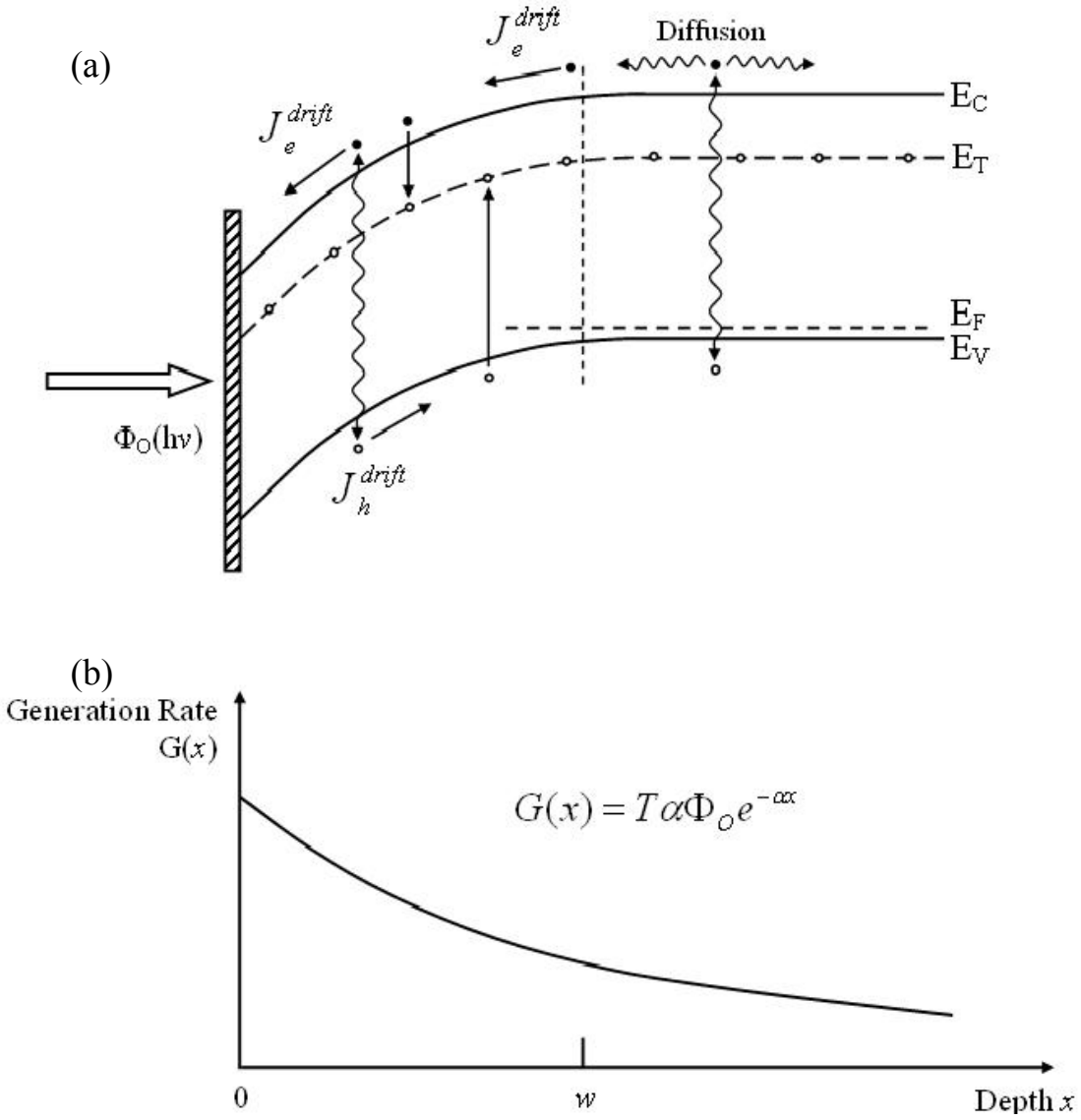

Figure 2-5. (a)Band diagram of a *p*-type semiconductor with a transparent Schottky barrier contact, which contains a minority carrier trap (E_T); (b)Illumination through the barrier with a flux Φ_O of photons ($hv > E_g$) generates electron-hole pairs at a rate G(x) [6]. These generated charge carriers result in a drift current of holes, and drift and diffusion currents of electrons

within the depletion region W. The higher density of electrons provides minority carriers for capture at the trap.

Illumination through the barrier with a flux Φ_O of photons ($hv > E_g$) generates electron-hole pairs, as illustrate in Figure 2-5(b). Electrons (or holes) are generated at a local rate per unit volume G(x)

$$G(x) = T_C \alpha \Phi_O e^{-\alpha x}, \qquad \textbf{(Eq. 2. 14)}$$

where T_C is the transparency of the contact, α is the absorption coefficient at the particular photon energy.

Within the depletion region W, the electric field E acts on both electrons and holes to produce a drift current: holes drift in a positive x direction into the semiconductor, and electrons in a negative x direction toward the metal, as shown in Figure 2-5(a). Furthermore, the electric field prevents holes generated beyond W from entering the depletion region, whereas draws electrons into the depletion region. Within the depletion region, the electron current is made up of drift and diffusion components, whereas the hole current is due to drift alone. Thus, the steady state electron concentration exceeds the hole concentrations, and the ratio of minority carrier to majority carrier within the depletion region can be further improved by increasing the electron diffusion current using a semiconductor with a long diffusion length.

Consequently, within the depletion region W, only minority carriers are available for capture at traps during the optical pulse. When the laser pulse is turned off, the subsequent thermally-stimulated electron emission transient from the trap level is measured and processed in the same way as DLTS, and the amplitude of the capacitance transient is given by

$$\frac{\Delta C_O}{C} = \frac{1}{2}\left(\frac{W-\lambda}{W}\right)^2 \frac{N_T}{N_A}\left(\frac{c_p}{e_p + c_p}\right), \qquad \textbf{(Eq. 2. 15)}$$

where ΔC_O is the change in capacitance after optical pulse, C the capacitance under the reverse bias V_R, λ the transition length, c_p and e_p are the capture and emission rate of electrons by the deep level.

It is essential to note the important attribute of MCTS technique, which can effectively fill and empty the defect levels located within the W-λ layer using optical pulses. This enables the detection of near-surface deep levels located within the depletion region.

Due to the lack of a homogeneous minority carrier density within the depletion region, the exact interpretation of the MCTS spectrum requires solving the continuity equation within the depletion region under illumination, and fitting of the experimental spectrum with numerical simulation. This procedure is too complex to be accomplished in this study, instead, we will refer to the recent calculation by Davidson *et al.* on the *n*-type Si using optical pulse with the same wavelength (850 nm, hv = 1.46 eV) as the experimental setup used in this study [7].

Figure 2-6 shows the electron and hole concentrations in a reverse biased Schottky diode of *n*-type Si for two cases: in the dark, or under illumination, within a depletion region of width 1.0 μm. This calculation demonstrated that the minority carrier (hole) concentration under illumination exceeds the majority carrier (electron) concentration in the depletion region by more than two orders of magnitude for *n*-type Si. The finding of the significantly higher concentration of minority carrier within the depletion region is also applicable for *p*-type Si/SiGe/Si heterostructure of similar doping concentration using optical pulse of the same wavelength.

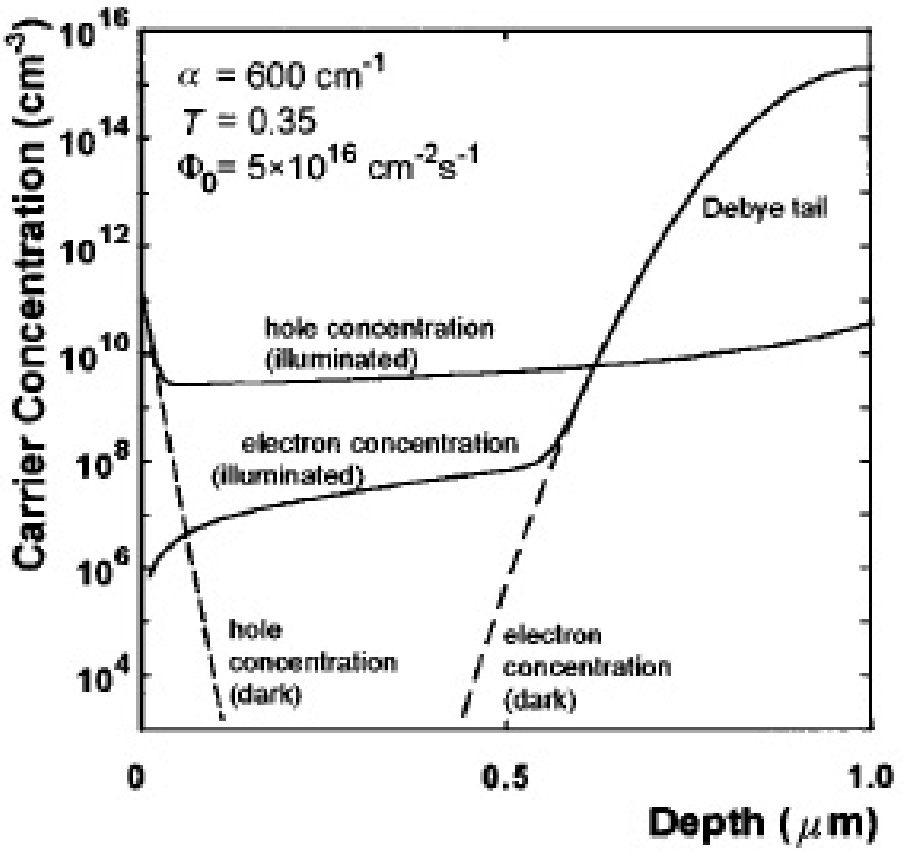

Figure 2-6. Electron and hole concentrations in a reverse biased Schottky diode obtained from solutions of the continuity equation: (----) semiconductor in the dark; (—) semiconductor illuminated. Inset: values of absorption coefficient α, lifetime τ_R, and incident optical power density Φ_0 used in the calculation [8].

2. 6. Electron-Beam-Induced Current (EBIC)

The EBIC mode of scanning electron microscopy (SEM) is a unique nondestructive electrical measurement technique to study the defect distribution and their electrical activities in semiconductors [9,10]. Usually, an electron beam (e-beam) of energy E and beam current I_b is raster-scanned across an electrical junction (p-n junction, Schottky barrier diode, MOSFET, or MOS capacitor), as shown in Figure 2-7 for the case of a Schottky diode of *p*-type Si. Electron-hole pairs (ehp) are generated in the semiconductor by absorbing the e-beam energy,

and some of the charge carriers diffuse to the electrical junction, where they are separated by the internal electrical field and be collected by the external circuit as the electron-beam-induced current I_{EBIC}.

If an electrically active defect is located near the ehp generation volume, some of the ehp may recombine at the defect, resulting in a local reduction of the collected current. Therefore, to map the defect distribution and their electrical activities, an e-beam is scanned over the surface of the electrical junction, and the generated current I_{EBIC} is measured at each point along the scan, and displayed as a brightness map. Areas of low defect density result in a higher EBIC current and appear brighter, while areas of higher defect density produce a smaller EBIC current and appear darker in the EBIC image.

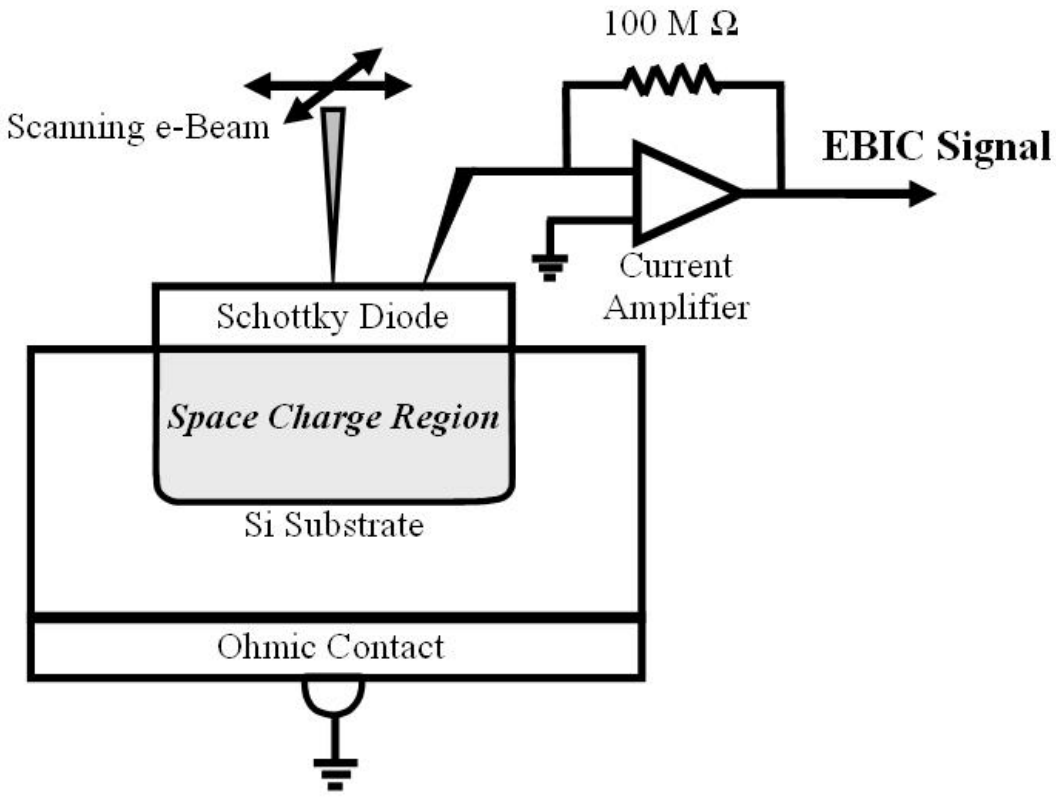

Figure 2-7. Schematic of EBIC measurement on a Schottky barrier diode of *p*-type Si.

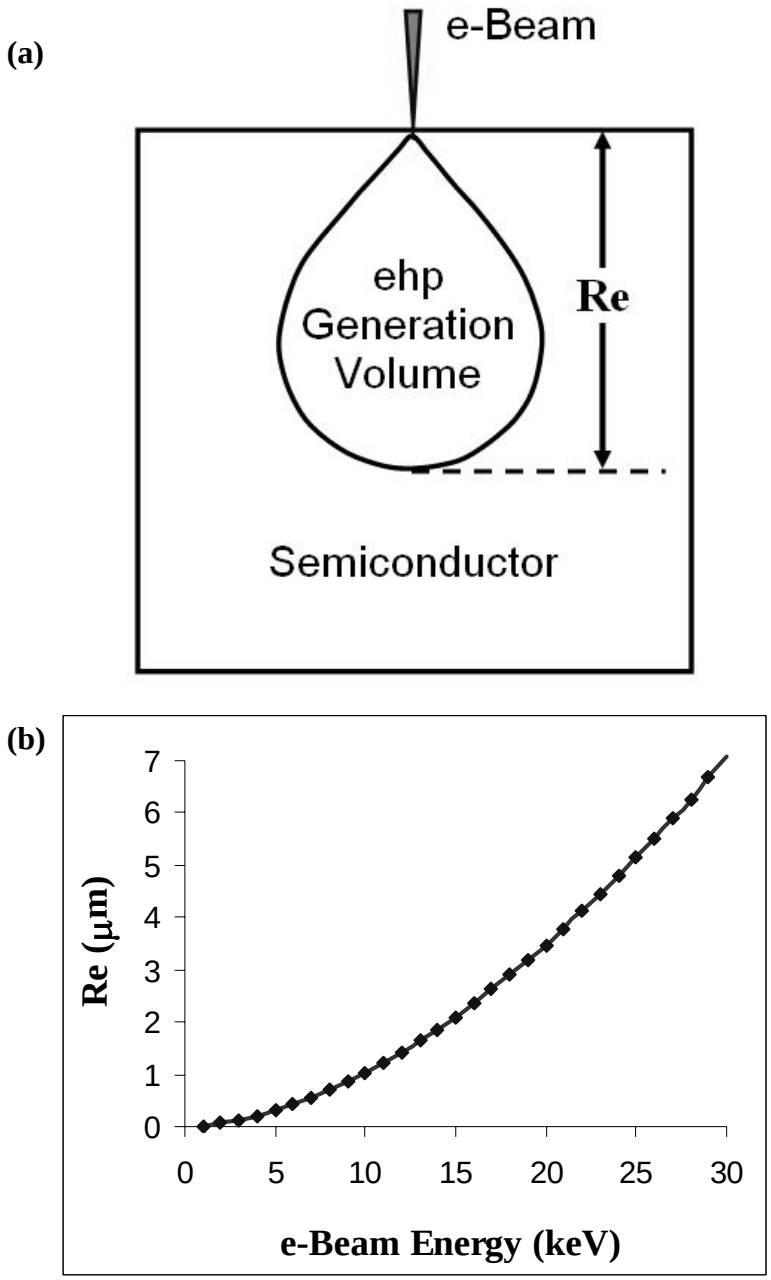

Figure 2-8. (a) Schematic of the interaction between e-beam and bulk semiconductor. The characteristic parameter of electron ranges R_e is shown as the diameter of electron-hole pairs generation volume; (b) R_e as a function of the e-Beam energy.

In addition to spatially mapping the defect distribution in semiconductors, EBIC

provides the possibility of detecting defects located at some depth by varying e-beam energy E. Electron-beam with different energies corresponds to different electron ranges R_e, which is approximately the diameter of ehp generation volume, as shown in Figure 2-8(a) and (b) [11,12]. Thus EBIC micrographs measured with different e-beam energies can be related to electrically active defects located at different depths, which is very useful for studying semiconductors with depth-dependent defect distribution, e.g., strained-Si/SiGe/Si-substrate heterostructures [13]. Higher energy e-beam can be used to observe the high density misfit dislocations at deeper region of graded SiGe layer, while lower energy e-beam can be used to examine threading dislocations located within constant SiGe layer [14,15], or even the misfit dislocations at the interface of partially-relaxed strained-Si/SiGe layers [13].

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CHAPTER 3. CARRIER DEPLETION BY DEFECTS IN GRADED SiGe LAYERS OF Strained-Si/SiGe/Si HETEROSTRUCTURES

3. 1. Introduction

Strained-Si grown on relaxed SiGe "virtual substrate" is of strong interest due to the higher carrier mobility, and the ability to essentially improve the MOSFET device performance without the aggressive geometric scaling. Furthermore, a tensile-strained Si layer for the channel of MOSFET device is compatible with the modern bulk-Si CMOS technology.

However, there is a strong concern with strained-Si electrical devices, because of the presence of dislocations within the strained-Si/SiGe/Si heterostructures. Since the strain-relaxed SiGe layer is formed via the introduction of strain-relieving misfit dislocations, dislocations are inherent defects of the strained-Si/SiGe/Si heterostructures. There are misfit dislocations confined within the graded SiGe layer or at the interface of SiGe/Si-substrate, as well as the threading dislocations originating from the SiGe layer and penetrating up to the top surface. For the supercritical strained-Si with a thickness exceeding the critical thickness, misfit dislocations may form at the strained-Si/SiGe interface [1,2]. And the possible depth distribution of dislocations for a supercritical strained-Si/SiGe/Si-substrate heterostructure is schematically shown in Figure 3-1.

The presence of threading or misfit dislocations at the strained-Si/SiGe interface is most detrimental to the MOSFET device performance by reducing carrier mobility and/or increasing leakage current [3,4,5,6], and require a systematic structural and electrical characterization, which will be discussed in Chapters 4 and 5. On the other hand, the dense misfit dislocations confined within the graded SiGe layer are further away from the top Si

layer where the MOSFETs operate, and consequently less harmful to the final device performance. Nevertheless, it is necessary to study the defects related to the misfit dislocations within the graded SiGe layer, and the effects of these trap levels on the device characteristics.

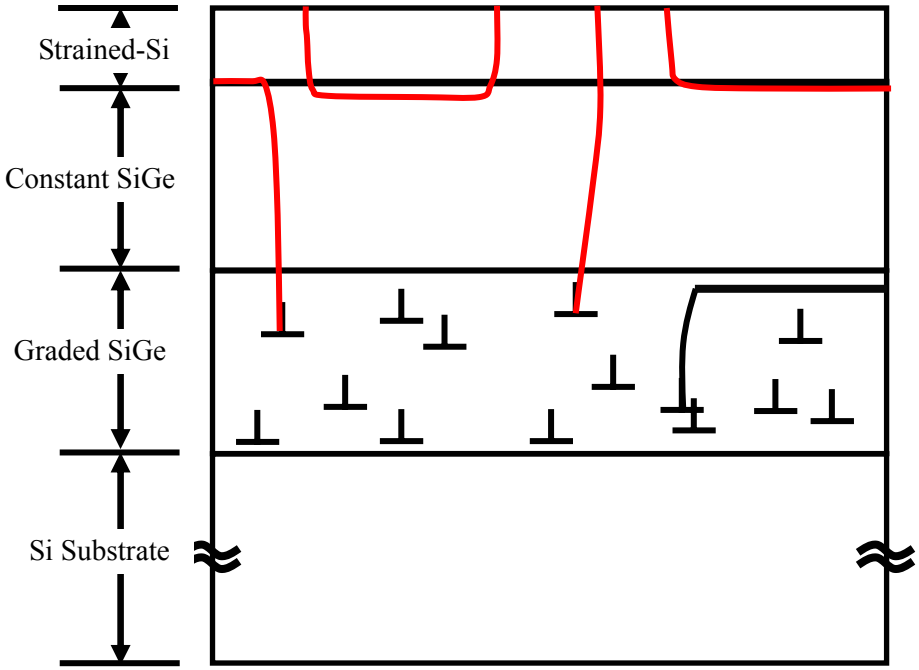


Figure 3-1. Schematic of a strained-Si/SiGe/Si heterostructure, with most of the dislocations confined within the SiGe graded layer, and some misfit dislocations generated at the strained-Si/SiGe interface. Note that some of the dislocations originate from the SiGe layer and penetrate up to the top Si layer.

The electrically active deep levels related to the dislocations within graded SiGe layer have been studied extensively through a combination of deep-level transient spectroscopy (DLTS), and electron-beam-induced current (EBIC), and photoluminescence (PL) measurements [7,8,9,10]. These previous electrical characterization results revealed the presence of defect states within the band gap, which may resulting in electrical

conductivity-type conversion for *n*-type SiGe layer, and compensation of *p*-type SiGe layer [10], similar to plastically-deformed bulk Si [11].

However, there are limited works concerning the effects of the high-density acceptor-like dislocation-related defects on the capacitance-voltage (*C-V*) characteristics of electrical devices of the strained-Si/SiGe/Si heterostructures, especially at lower temperatures. A systematic study and a quantitative understanding of the *C-V* characteristics are central to accurately determine the spatial depth of electrically-active defects employing capacitance-transient-based techniques (e.g., DLTS). Thus, in this chapter, we will first discuss the temperature-dependent *C-V* characteristics of Schottky barrier diodes of the heterostructures, and identify the carrier depletion within the graded SiGe layer. Then, the temperature-dependence of *C-V* characteristics will be explained considering the Fermi level pinning by local deep levels, which allows the determination of the activation energy of the defect level. Finally, this activation energy of the defect level will be compared with the results of DLTS measurements.

3. 2. Experimental Details

The strained-Si/SiGe/Si-substrate heterostructure discussed in this chapter was grown by chemical vapor deposition on a *p*-type Si substrate. On the Si substrate, a 3000 nm thick graded $Si_{1-x}Ge_x$ layer (x is increased from 0% to 20%) was grown, which is followed by a 2000 nm thick uniform $Si_{1-x}Ge_x$ layer (x = 20%). Finally, a strained-Si layer with a thickness of 115 nm was grown on the relaxed uniform SiGe layer.

Schottky barrier diodes and ohmic contacts were prepared by evaporating Aluminum on the strained-Si layer surface, and by rubbing Ga–In eutectic on the back side, respectively.

C-V and DLTS measurements were carried out using a BioRad DL8000 digital DLTS system at the frequency of 1 MHz in the temperature range from 50 K to 300 K.

3. 3. Results and Discussion

3. 3. 1. Temperature-dependent Capacitance-Voltage Characteristics

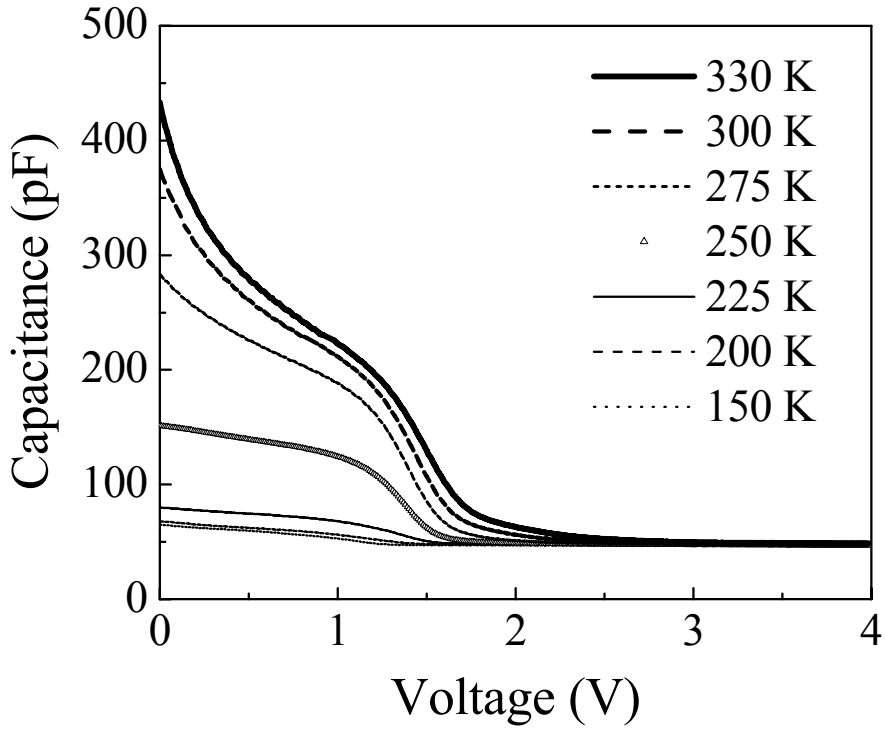


Figure 3-2. *C-V* characteristics of the Schottky barrier diodes measured in the temperatures ranging from 330 to 150 K.

C-V characteristics of the Schottky barrier diode of this as-grown strained-Si/SiGe/Si heterostructure have been measured in the temperature range from 330 to 150 K, and are displayed in Figure 3-2. Note that the *C-V* characteristics are strongly temperature dependent,

with the capacitance values essentially decreasing with lower temperatures. This trend is especially prominent for bias voltages smaller than 2 V, in the temperature range between 225 and 275 K. The value of zero bias capacitance is reduced from 426 pF at 330 K to 64 pF at 150 K. It is seen that even though the capacitance values are greatly reduced with decreasing temperatures, the inflexion points of the temperature-dependent *C-V* characteristics are still maintained.

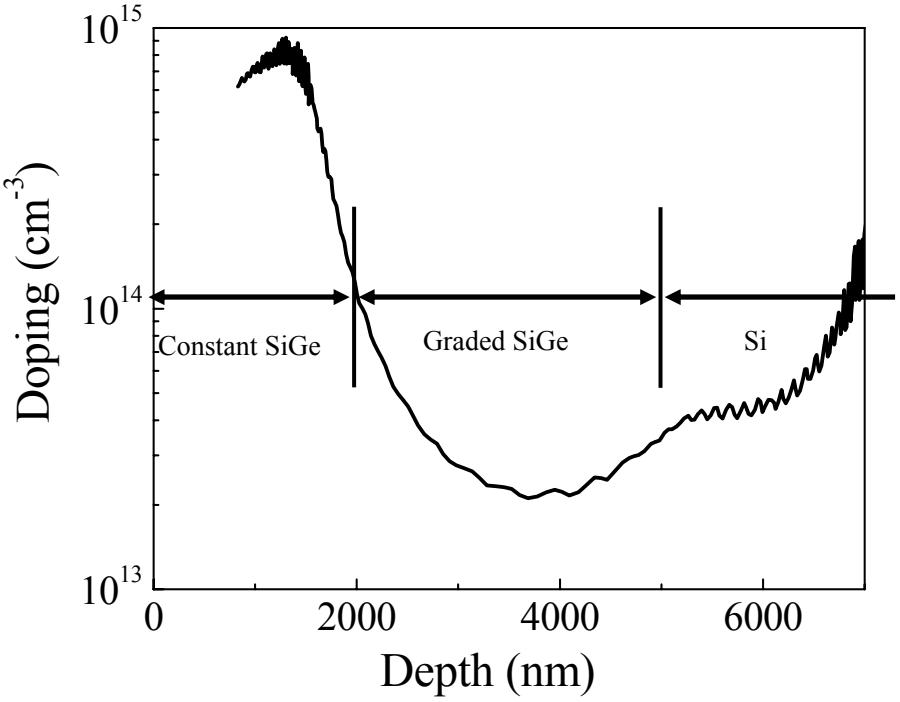


Figure 3-3. The depth profile of apparent carrier concentration of strained-Si/SiGe/Si heterostructure, calculated from the *C-V* characteristics measured at 330K.

The depth profile of apparent carrier concentration is calculated from the *C-V* characteristics measured at 330K (see Figure 3-2), and shown in Figure 3-3. Drastic carrier depletion seems to occur within the graded SiGe layer, and spreads to constant SiGe

layer and Si substrate on both sides. Local carrier depletion within the graded SiGe layer coincides with a dense misfit dislocation network introduced to relive the lattice-mismatch strain between SiGe layer and Si substrate, as confirmed by cross-sectional TEM study. Consequently, a layer with a high resistivity results from this carrier depletion, and may affect *C*-*V* and DLTS measurements.

It is likely that a high concentration of donor-like trap levels exist in the graded SiGe layer due to the formation of strain-relieving misfit dislocations, and may captures free charge carriers (holes), resulting in a local carrier depletion. If the local concentration of this donor level is higher than that of the incorporated B dopant, Fermi level is locally pinned to the donor-like defect level. The schematic of the band diagram of a strained-Si/SiGe/Si heterostructure with local high-concentration trap levels is displayed in Figure 3-4(a). Within the graded SiGe layer, a potential barrier forms due to the pinning of local Fermi level to the high density defect level, and the height of this potential barrier (E_b) is approximately equal to the difference between the energy level of defect state (E_T) and Fermi level (E_F), as specified by

$$E_b = E_T - E_F. \qquad \textbf{(Eq. 3. 1)}$$

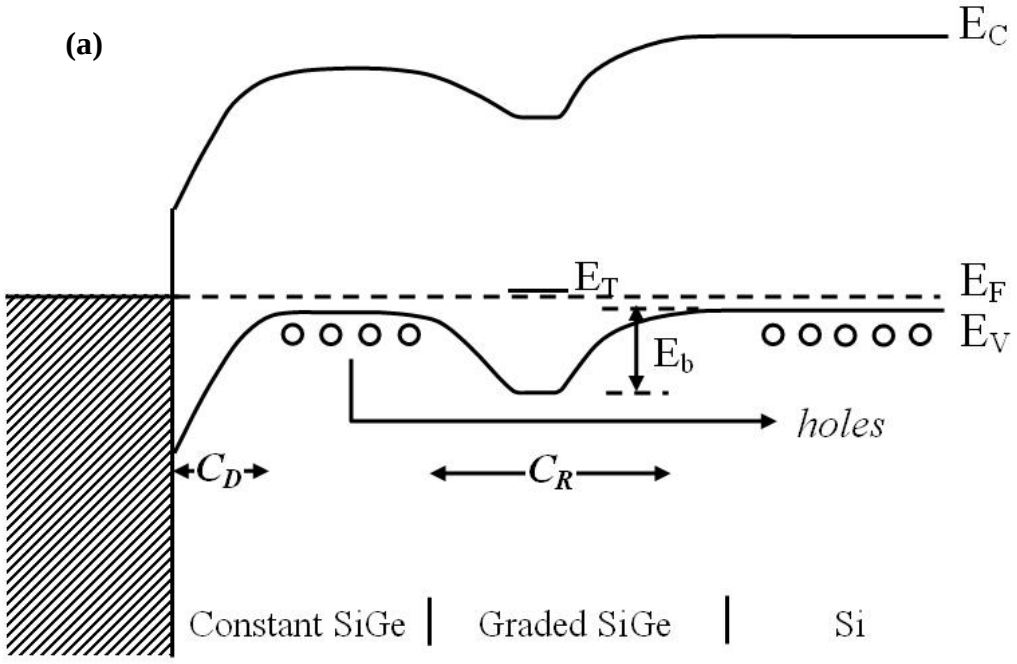
The corresponding equivalent circuit of a small ac signal for this band structure is represented by Figure 3-4(b), where C_D is the depletion capacitance of the Schottky barrier diode, C_R is the equivalent capacitance of the potential barrier within the graded SiGe layer, and the associated parallel resistance term of R is the inverse of the ac conductance G of the barrier. According to the formulation based on thermionic current [12], R per area is given by

$$G = \frac{1}{R} = \frac{q^2 v_{th} N_v}{2kT} e^{-\frac{E_b}{kT}} = \frac{q^2 (\frac{3kT}{m^*})^{\frac{1}{2}} 2(\frac{2\pi kTm^*}{h^2})^{\frac{3}{2}}}{2kT} e^{-\frac{E_b}{kT}} = AkTe^{-\frac{E_b}{kT}} \quad \textbf{(Eq. 3. 2)}$$

$$R = \frac{1}{AkT} e^{\frac{E_b}{kT}} \quad \textbf{(Eq. 3. 3)}$$

Here, q is the elemental charge, v_{th} is the thermal velocity, N_v is the effective density-of-states of the valence band, k is the Boltzmann constant, T is temperature, and A is a constant value independent of temperature.

Note that the Schottky barrier capacitance C_D can be varied by applying different bias voltage, while the equivalent capacitance of the potential barrier C_R is a fixed value determined by the width of the resistive layer, and R is dependent on the temperature.



(b)

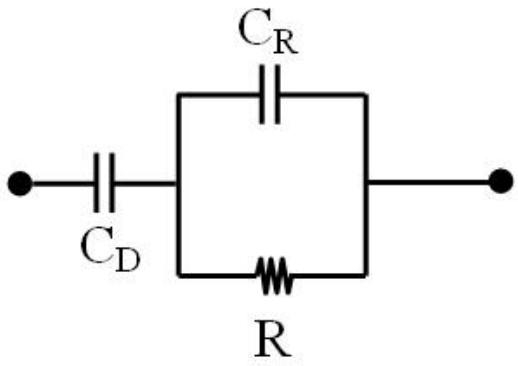


Figure 3-4. (a) The schematic of the band diagram of a strained-Si/SiGe/Si heterostructure with local high-concentration defects. This band diagram contains a Schottky barrier diode with a depletion capacitance C_D, and a resistive graded SiGe layer represented by a capacitance C_R in parallel with a resistance R. (b) The equivalent circuit for this band structure.

In the real *C*-*V* measurement, the capacitance of the equivalent circuit of Figure 3-4(b) is represented by the total capacitance C in parallel with the conductance G_P, and could be described as:

$$C = \frac{C_D + \omega^2 R^2 C_D C_R (C_D + C_R)}{1 + \omega^2 R^2 (C_D + C_R)^2}, \qquad \textbf{(Eq. 3. 4)}$$

where the testing angular frequency $\omega = 2\pi f$, and f is 1 MHz.

Hence, the strong temperature-dependence of *C*-*V* characteristics shown in Figure 3-2 could be qualitatively explained using the equivalent circuit of Figure 3-4(b). At high temperatures (e.g., 330 K), the resistance R of the resistive graded SiGe layer is a small value, and the related capacitance C_R is practically shunted by this small resistance, and the total capacitance C measured at 330 K is basically the value of depletion capacitance C_D of the Schottky barrier diode. As a result, the depth profile of apparent carrier concentration can be

calculated from the high temperature *C-V* characteristics according to Eq. 2.3 and 2.4 discussed in Chapter 2, without the interference of the underlying resistive graded SiGe layer.

The equivalent resistance *R* increases exponentially with the inverse of temperature (see Eq. 3.3) because of the potential barrier E_b, and C_R starts to affect the value of measured capacitance *C* when the value of $\omega R(C_D + C_R)$ is increased towards 1 with decreasing temperature, as suggested by Eq. 3.4. At low temperatures (e.g., 100 K), due to the large values of *R*, the measured capacitance *C* becomes the series combination of C_D and C_R, given by

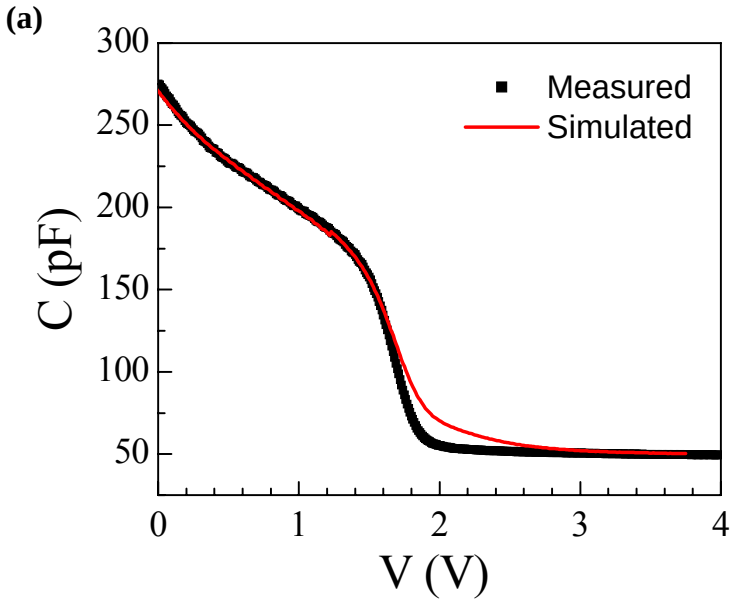
$$C = \frac{C_D C_R}{C_D + C_R}. \qquad \textbf{(Eq. 3. 5)}$$

Then the equivalent capacitance C_R of the resistive layer could be calculated as ~75 pF, which corresponds to a thickness of 4.7 μm, slightly larger than the thickness of the graded SiGe layer of 3 μm. As a result, the resistive layer may include both graded SiGe layer, and a part of the Si-substrate, consistent with the depth profile of carrier concentration shown in Figure 3-3.

The validity of this proposed model is quantitatively verified by comparing the measured *C-V* characteristics with those simulated according to the equivalent circuit of Figure 3-4(b). Note that the *C-V* curve measured at 330 K were used as $C_D(V)$, since the effective *R* is lowest at this temperature and can be neglected. Figure 3-5(a) and (b) show both the measured (black lines) and simulated (red lines) *C-V* characteristics for temperatures of 275 and 225 K, respectively. It is seen that the simulated *C-V* curves are almost identical with those measured ones for bias voltage less than 1.5 V. For bias voltage larger than 1.5 V, the depletion region of the Schottky diode extends into the graded SiGe layer, i.e., the resistive layer, and the equivalent circuit becomes invalid due to the overlapping of the two

depletion regions.

The values of capacitance C_R and resistance R were determined from the fitting of the C-V characteristics of each measured temperature. It is noted that the calculated values of C_R are practically independent of temperature, indicating a constant thickness of the resistive layer, while the values of resistance R varies significantly with different temperatures. Further analysis revealed an exponential dependence of the resistance R on (1/T), as shown in Figure 3-6, consistent with the proposed carrier depletion model and the effective pinning of Fermi level to a defect level (see Figure 3-4(a)). The effective barrier height E_b of 0.28 eV was determined from the Arrhenius plot of Figure 3-6.



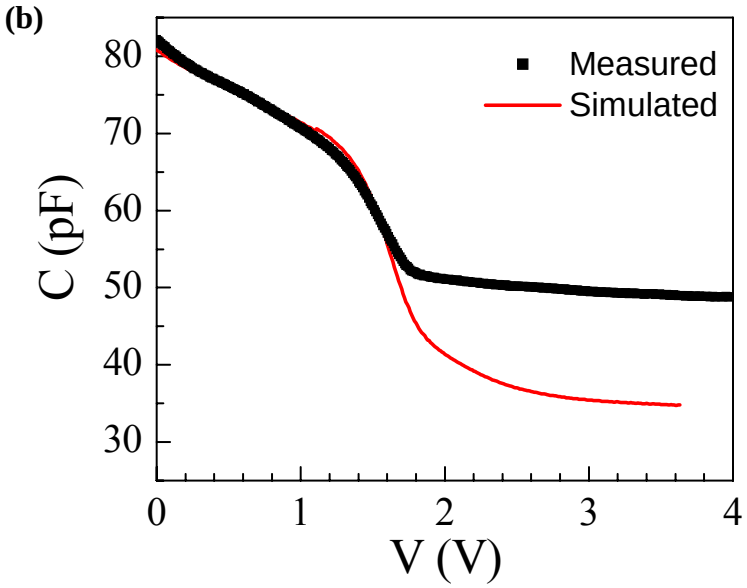


Figure 3-5. The comparison of simulated (red lines) and measured (black lines) *C-V* characteristics at 275 (a) and 225 K (b), respectively.

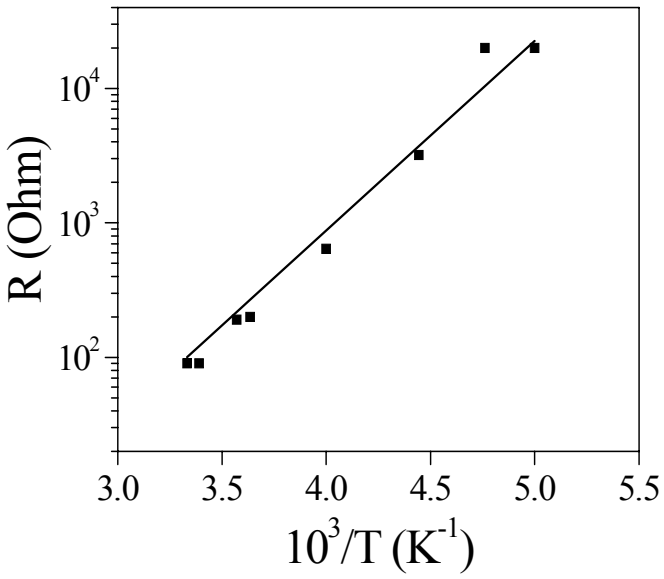


Figure 3-6. An Arrhenius plot of resistance *R* as a function of (1000/*T*).

3. 3. 2. DLTS Results

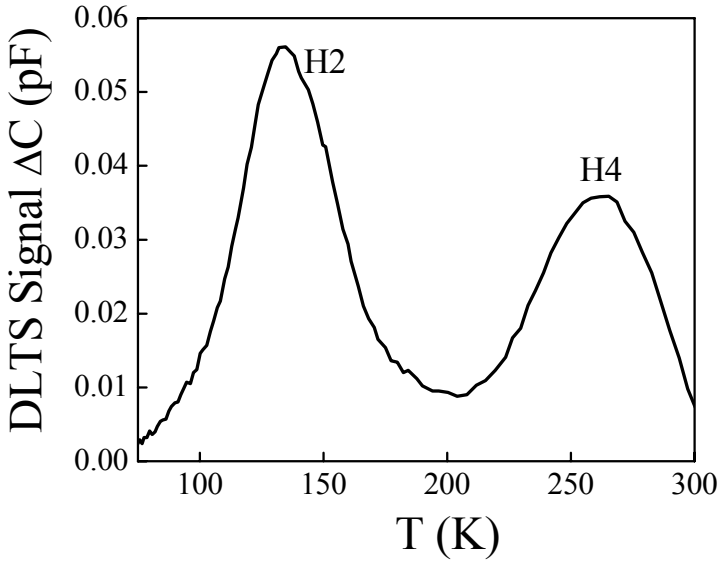


Figure 3-7. DLTS spectrum of the strained-Si/SiGe/Si heterostructure measured with reverse and pulse voltages of 2 and 1 V, and a pulse duration of 1 ms. The time window is 20 ms.

Table 3-1. Electrical properties including trap energy level within the energy band gap E_a, capture cross section σ, and trap concentration N_T of defect levels detected by the DLTS spectrum (as shown in Figure 3-7).

Trap Level	T (K)	E_a	σ	N_T
H2	135	0.26 eV	4.9×10^{-14} cm^2	2.2×10^{13} cm^{-3}
H4	260	0.46 eV	1.3×10^{-15} cm^2	1.1×10^{13} cm^{-3}

Figure 3-7 shows the typical DLTS spectrum measured for the strained-Si/SiGe/Si heterostructure with reverse and pulse voltages of 2 and 1 V, and a pulse duration of 1 ms. According to the *C-V* characteristics, this combination of reverse and pulse voltages employed for DLTS measurements enables the electrical defect study of only the graded SiGe layer. Two DLTS peaks were observed at temperatures around 135 and 260 K, respectively, and related to

majority carrier (hole) traps. Electrical properties of the observed hole traps including energy levels within the energy band gap, capture cross sections, and trap concentrations have been calculated from the corresponding Arrhenius plots, and presented in Table 3-1. Since these two trap levels are only observed in the relaxed graded SiGe layer, the hole traps are probably electrically-active defects generated during the strain relaxation of the graded SiGe layer, and associated with the dense misfit dislocations. The origin and nature of these two defects will be discussed in more details in the following chapter, and the labeling of the two hole traps are in accordance with that of Chapter 4.

Nevertheless, we can further corroborate the proposed model of Fermi level pinning by a donor level (see Figure 3-4(a)) by comparing the results of temperature-dependent *C-V* and DLTS measurements. According to Eq. 3.1, the Fermi level can be calculated form the measured defect energy level of 0.46 eV and potential barrier height of 0.28 eV as 0.18 eV. This value of Fermi level would translate to a doping concentration of ~10^{15} cm^{-3} at the DLTS peak temperature of 260 K, consistent with the measured carrier concentration of Figure 3-3. Also, the defect concentration of hole trap *H4* (~10^{13} cm^{-3}) is comparable to the free hole concentration of the graded SiGe layer (~3×10^{13} cm^{-3}), and able to capture most of free charge carriers, resulting in a significant carrier depletion.

3. 4. Conclusions

In summary, a strong temperature-dependence of *C-V* characteristics of Schottky diodes of strained-Si/SiGe/Si heterostructure are identified and related to a significant carrier depletion within the graded SiGe layer. A model of Fermi-level pinning by a donor level is proposed, which results in a potential barrier within graded SiGe layer. An equivalent

circuit can be established, taking into account of the Schottky barrier capacitance C_D, as well as a capacitance C_R in parallel with resistance R due to the presence of a potential barrier. The value of the potential barrier height E_b is determined from the temperature dependence of R, and found to be consistent with the energy level of a hole trap detected by DLTS measurement.

The temperature dependence of *C-V* characteristics is generally observed for Schottky barrier diodes of different strained-Si/SiGe/Si heterostructures, though in various extents. The study of this strained-Si/SiGe/Si heterostructure with a relatively low doping concentration proves that the variation of measured zero-bias capacitance with decreasing temperature is not due to the change of depletion region, rather due to the defects within the underlying graded SiGe layer. This finding is important for the accurate determination of the spatial depth of observed deep levels in the following chapters using DLTS or MCTS techniques.

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CHAPTER 4. EFFECTS OF THERMAL ANNEALING ON DEEP-LEVEL DEFECTS IN Strained-Si/SiGe/Si HETEROSTRUCTURE

(To be submitted)

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ABSTRACT

The effects of thermal annealing at 800 ºC in oxidizing atmosphere on the electrical properties of strained-Si/SiGe heterostructure were investigated using capacitance-voltage (*C-V*), deep-level transient spectroscopy (DLTS), and electron-beam-induced current (EBIC) techniques. Changes of apparent carrier concentration profile and EBIC contrast after thermal annealing were attributed to the annealing of dislocation-trail related defects. DLTS measurements identified a near-surface (less than 150 nm deep) extended defect only present in the annealed heterostructure, and related it to the formation and motion of misfit dislocations during the strain relaxation of metastable strained-Si layer.

4. 1. Introduction

Strained-Si is a promising candidate to replace traditional bulk Si in high-speed complementary metal-oxide-semiconductor (CMOS) technology, due to the higher electron and hole mobilities in the strained-Si channel layer [1,2].However, if the thickness of a lattice-mismatched epilayer is close to or exceeds the critical thickness it becomes energetically favorable to relieve the mismatch strain through the introduction of misfit dislocations [3,4].If the strained-Si layers were grown at low temperatures with a thickness exceeding the critical one, the resulting films are metastable to dislocation formation, and a partial strain relaxation could occur during subsequent thermal processings (e.g., gate oxidation, implanted dopant activation, etc.) for fabricating CMOS devices. The stress relaxation could essentially change the properties of strained-Si layer both by the reduction of stress and by the introduction of misfit and threading dislocations together with deformation-induced defects, resulting in reduced mobility enhancement and increased leakage current for the final devices [5,6,7,8].

So far, several studies have been done concerning the strained-Si top layer using structural and electrical characterization [9,10,11].Yuan *et al.* have demonstrated that Electron-Beam-Induced Current (EBIC) can be employed to investigate MDs at the interface of strained-Si/$Si_{0.8}Ge_{0.2}$, located within the depletion region of a Schottky contact [9,10]. Wang *et al.* used Deep-level transient spectroscopy (DLTS) and metal-oxide-semiconductor (MOS) transient capacitance methods to evaluate the interface states density of both oxide/strained-Si and strained-Si/SiGe interfaces and minority carrier generation lifetime of a MOS structure, respectively [11]. However, there has been no report on the defect levels generated at the strained-Si/SiGe interface after strain relaxation. The properties of both

dislocations and deformation-induced defects depend on deformation conditions, contamination level etc., and were not totally understood even in single-crystalline Si. In the strained-Si/SiGe heterostructures their behaviour could be even more complex. Therefore, the investigations of defects in such structures and of their transformation under annealing have fundamental and practical importance.

In this paper, the metastable as-grown strained-Si/SiGe heterostructure and that annealed at 800˚C are studied by the capacitance-voltage (*C-V*), DLTS and EBIC techniques. The *C-V* measurements show that annealing leads to the disappearance of some defects in the graded SiGe probably induced by the motion of threading dislocations. The DLTS spectrum similar to that ascribed to the dislocation trails in plastically-deformed Si is observed in graded SiGe layer (of both as-grown and annealed heterostructures). One additional prominent DLTS peak is observed only on the annealed one, and attributed to a near-surface dislocation-related trap level. This indicates that thermal annealing creates deformation-induced defects in the strained-Si layer.

4. 2. Experimental Details

The strained-Si/SiGe/Si-substrate heterostructure was synthesized by chemical vapor deposition on a *p*-type 200 mm Si wafer using either SiH_4 (for strained-Si layer) or SiH_2Cl_2 and GeH_4 (for SiGe layer) as source gases. The structure consists of four epilayers deposited on a highly doped *p*-Si substrate with a boron concentration of about $10^{19}cm^{-3}$. On the Si wafer, a 2500 nm thick Si epilayer of $10^{16}cm^{-3}$ boron doping was grown, which is followed by a 670 nm thick graded $Si_{1-x}Ge_x$ layer (x is increased from 0% to 20%), and a 1000 nm thick uniform $Si_{1-x}Ge_x$ (x = 20%). Finally, a strained-Si layer with a thickness of 73.5 nm

was grown on the relaxed uniform SiGe layer. As-grown strained-Si/SiGe heterostructure was divided into two parts, and one of them was annealed at 800˚C in oxidizing atmosphere to grow a 10 nm thick oxide to represent the conventional gate oxide growth process. Since the 73.5 nm strained-Si layer is larger than the calculated critical thickness (~20 nm) [3,4]for strained-Si grown on relaxed $Si_{0.8}Ge_{0.2}$, the as-grown top Si layer was metastable, and it could undergo some relaxation during thermal annealing.

C-V and DLTS measurements were carried out using a BioRad DL8000 digital DLTS system in the temperature range from 50 K to 300 K. EBIC studies were performed using a JSM-840A (JEOL) SEM operating in the EBIC mode on the same Schottky diodes at electron-beam (e-beam) energy E_b varying from 8 to 30 keV and at temperatures of 90 K and 300 K. Besides, a HP 4275A multi-frequency LCR meter was used to measure the *C-V* and conductance-voltage characteristics at frequencies from 10 KHz to 2 MHz, to identify and correct the effects of series resistance on the capacitance values. For the electrical analyses, the Schottky and ohmic contacts were prepared by evaporating Aluminum on the strained-Si layer surface, and by rubbing Ga–In on the back side, respectively. Note that thermally-grown oxide of the annealed sample was removed using a diluted HF solution before preparing the Schottky contacts.

4. 3. Results and Discussion

4. 3. 1. *C-V* Measurements

The *C-V* curves measured on the as-grown and annealed heterostructures are presented in Figure 4-1. Note that the capacitance values of the Schottky diodes for both heterostructures weakly depend on the temperature in the temperature range from

300 K to 100 K. And the capacitance values of the annealed sample are higher than those of the as-grown one in the total temperature range. The apparent charge carrier concentration profiles (see Figure 4-2) reconstructed from the corresponding *C-V* curves shows that thermal annealing leaded to an increase in the carrier concentration at a depth larger than 0.6 μm. The results of frequency-dependent capacitance and conductance measurement indicate that some effective resistance and capacitance associated with the large density of misfit dislocations within the graded SiGe layer exist. However, the total series resistance including both Ohmic contact resistance and dislocation-related effective resistance does not exceed 100 Ohm at room temperature and increases slightly with cooling as indicated by the weak temperature dependence of capacitance values. In the annealed sample the series resistance is found to be lower than that in as-grown one, which is consistent with an increase in the carrier concentration after annealing, as revealed in Figure 4-2. This allows us to conclude that in spite of rather high misfit dislocation density in the graded SiGe layer the resistance of this layer still remains rather low.

Observation of rather unusual carrier concentration increase in the constant and graded SiGe layers after thermal annealing could be due to annealing of some defects introduced by the dislocation motion during the strain relaxation of SiGe layers. In principle, these defects could be associated with the dislocation trails [12].In this case an essential increase in carrier concentration after annealing could means that the defect concentration in the dislocation trails could be rather high.

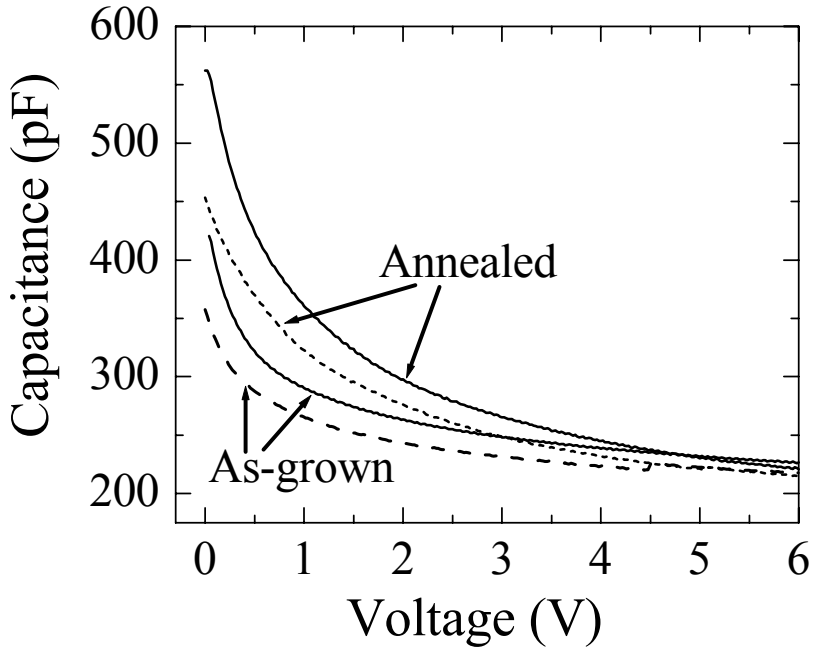

Figure 4-1. *C-V* curves measured on as-grown and annealed samples at 300 K (solid lines) and 100 K (dashed lines).

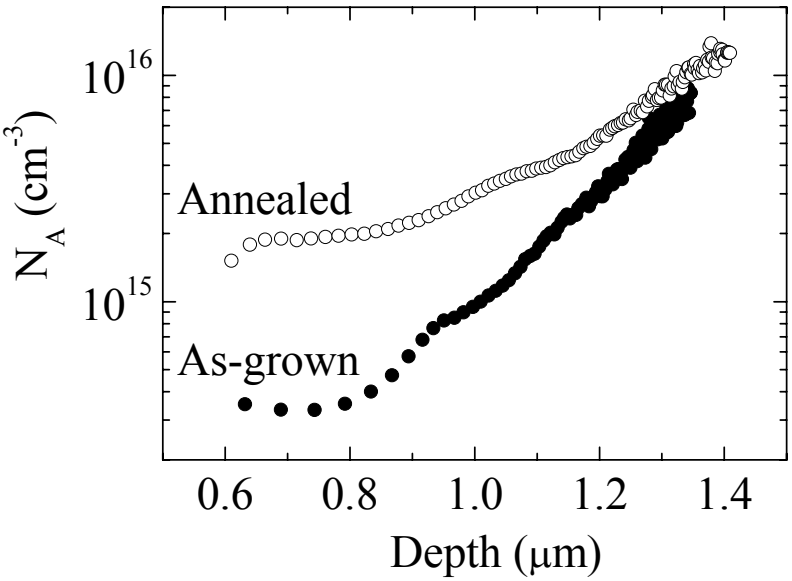

Figure 4-2. Apparent charge carrier concentration profiles of as-grown (solid circles) and

annealed (open circles) heterostructures.

4. 3. 2. DLTS Measurements

Figure 4-3 shows the typical DLTS spectra obtained on the as-grown strained-Si/SiGe heterostructure with a time window of 20 ms employing different reverse voltages V_R and pulse voltages V_P, which correspond to different depth regions within the multilayer structures. To assign the measured defect to a certain depth, the depletion region width W for corresponding reverse and pulse voltages was calculated from the C–V curves with a correction for the series resistance and λ-layer [13] using the following expressions:

$$W = \frac{\varepsilon_s \varepsilon_0 A}{C}, \qquad \textbf{(Eq. 4. 1)}$$

$$\lambda = \sqrt{\frac{2\varepsilon_s \varepsilon_0}{q^2 N_B}(E_F - E_T)}, \quad . \qquad \textbf{(Eq. 4. 2)}$$

where ε_s is the relative dielectric constant of the semiconductor, ε_0 the Permittivity of vacuum, A the Schottky contact area, C the measured sample capacitance at voltage V, q the electronic charge, N_B(=N_A or N_D, depending on doping type) the free carrier concentration, E_F the Fermi energy level, and E_T the trap energy level within the energy band gap [14,15].

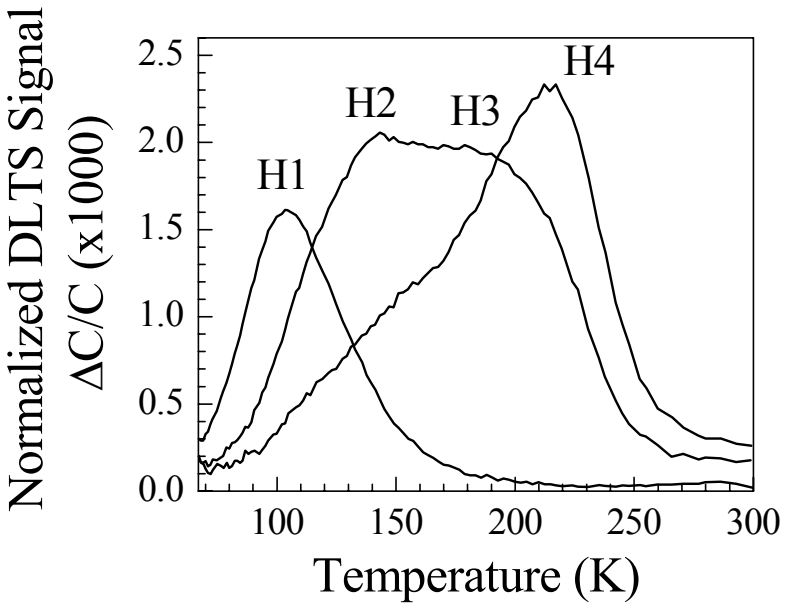

Figure 4-3. Normalized DLTS spectra ($\Delta C/C$) measured in the as-grown heterostructure at different depths. The biasing conditions are: V_R = 0.5 V & V_P = 0 V, V_R = 1.0 V & V_P = 0.5 V, V_R = 2.0 V & V_P = 1.0 V, respectively. t_P=1.0 ms.

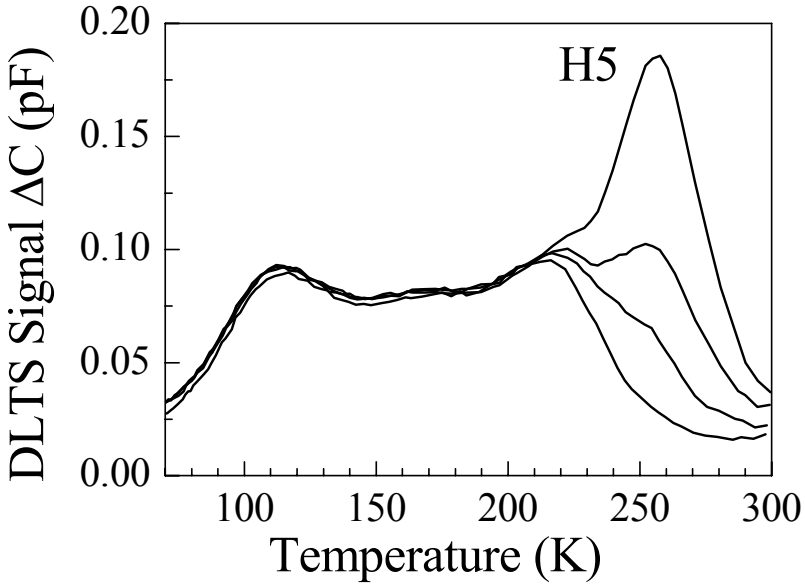

Figure 4-4. DLTS spectra measured in the annealed heterostructure using different

pulse durations t_P (t_P = 0.01, 0.03, 0.1 and 0.3 ms, respectively). Reverse voltage V_R = 3.0 V, and pulse voltage V_P = -0.3 V.

It is noted that the DLTS spectrum changes with depth, and four majority carrier (hole) defect levels *H1*, *H2*, *H3* and *H4* have been identified for different depths, as marked in Figure 4-3. DLTS peak *H1* is the only defect that could be observed at the depth smaller than 500 nm, the defects *H2* and *H3* could be revealed at a depth of about 600-700 nm, and at a depth larger than 700 nm the defect *H4* prevails.

In the annealed heterostructure, the DLTS spectrum at a depth larger than 500 nm was essentially the same as that observed on the as-grown one. But by employing small pulse voltages, an additional prominent deep level defect *H5* at smaller depths is revealed, as shown in Figure 4-4. This *H5* peak is shifted about 10-15 K to higher temperature in comparison with *H4* peak. The fact that the peak height of defect *H5* essentially decreases with increasing reverse bias voltages allows to associate the defect *H5* with near surface layers.

Electrical properties of the observed DLTS defect levels including energy level within the energy band gap, capture cross section, and trap concentration have been calculated from the corresponding Arrhenius plots, and presented in Table 4-1. Although the activation energy values obtained from the Arrhenius plots vary slightly depending on reverse bias and pulse voltages, the variations of DLTS peak temperature are rather small. Rather small temperature dependence of peaks measured at the same rate window allows to ascribe them to some energy levels probably dependent on Ge content.

Table 4-1. Electrical properties including trap energy level within the energy band gap, capture cross section, and trap concentration of defect levels of both samples, calculated from the corresponding Arrhenius plots.

	As-grown		Annealed	
H1	102K	0.20eV, 3.9×10^{-14}cm^2, 2.4×10^{13}cm^{-3}	90K	0.18eV, 1.2×10^{-13}cm^2, 3.7×10^{12}cm^{-3}
H2	115K	0.25eV, 2.4×10^{-13}cm^2, 2.6×10^{13}cm^{-3}	113K	0.19eV, 2.9×10^{-15}cm^2, 3.6×10^{13}cm^{-3}
H3	N/A	N/A	168K	0.31eV, 6.2×10^{-15}cm^2, 2.8×10^{13}cm^{-3}
H4	215K	0.43eV, 1.9×10^{-14}cm^2, 2.5×10^{13}cm^{-3}	213K	0.43eV, 1.6×10^{-14}cm^2, 2.9×10^{13}cm^{-3}
H5	N/A	N/A	255K	0.43eV, 2.4×10^{-16}cm^2, 3.1×10^{14}cm^{-3}

For the biasing conditions under which *H5* was detected, the corresponding depletion region *W* and λ-layer widths were calculated to be 650 nm and 500 nm, respectively, using the measured values of capacitance, carrier concentration, and trap energy level of *H5*. Consequently, the depth of the defect responsible for DLTS peak *H5* was estimated to be smaller than 150 nm.

To identify the origins and types of DLTS defects observed, we investigated the kinetics of the charge carriers capture process by these defects. Defect levels associated with point defects, *localized* extended defects or *band-like* extended defects can be distinguished from each other by monitoring the DLTS signal dependence on filling pulse duration t_P.[16,17] The carrier capture by both localized and band-like extended defect states is usually modeled by a time-dependent Coulomb barrier $\Phi(t)$ which builds up during the capture process of charge carriers, and can be described by a logarithmic time dependence of DLTS peak height; while

for point defects, the carrier capture kinetics has an exponential time dependence. Furthermore, the two types of extended defect states can be distinguished on the grounds of the dependence of their DLTS-line shape on the filling pulse duration. Band-like extended defects, e.g., dislocation core states, show an asymmetric DLTS peak broadening on the low-temperature side with increasing filling pulse duration, while the DLTS-line maximum stays constant with varying filling pulse duration for localized extended defects (e.g., 60º dislocations in plastically deformed Si).

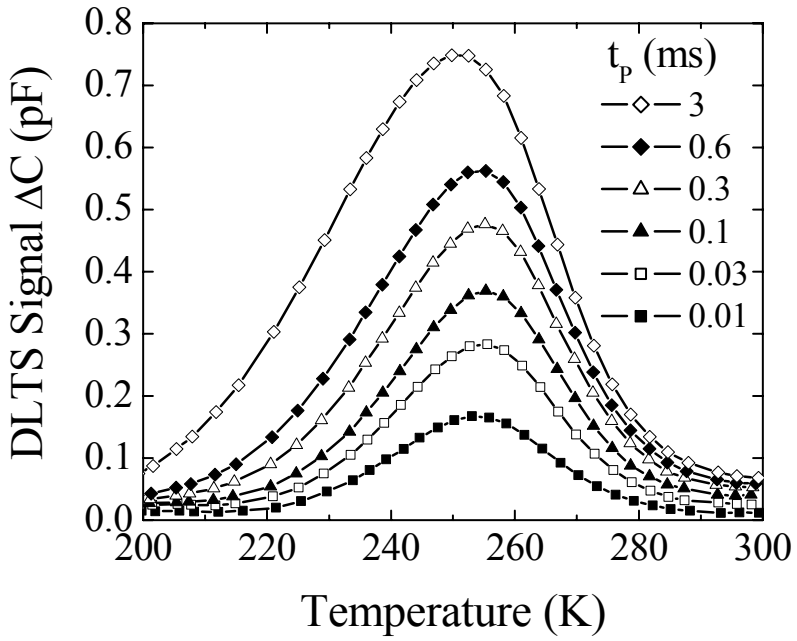

Figure 4-5. DLTS peak height dependence on the pulse duration t_P for defect *H5* in the annealed heterostructure. t_P = 0.01, 0.03, 0.1, 0.3, 0.6 and 3 ms, respectively. Reverse voltage V_R = 1.0 V, and pulse voltage V_P = -0.3 V.

The results of the capture kinetics study are displayed in Figure 4-4, showing that peaks *H1-H3* are saturated at a rather small pulse duration (e.g., 0.01 ms) while the amplitude of

peak *H5* slowly increases with increasing pulse duration. A more detailed study of peak *H5* (see Figure 4-5) demonstrates that the peak height of defect *H5* scales with the logarithm of the filling pulse duration with a symmetric peak shape. These observations strongly suggest that defect level *H5* is associated with extended defects, the charge buildup of which governs the capture rate.

Since the thickness of strained-Si layer (73.5 nm) of this strained-Si/SiGe heterostructure exceeds the equilibrium critical thickness (about 20 nm) predicted by the Matthews-Blakeslee theory, the top Si layer is metastable to dislocation formation, and some strain relaxation could occur during thermal annealing, resulting in the formation of misfit and threading dislocations. Yuan *et al.* revealed that individual 60° misfit dislocations exist at the interface of strained-Si/$Si_{0.8}Ge_{0.2}$ for a 100 nm thick strained-Si layer, in a Cross-sectional TEM image [9]. Furthermore, after the partial strain relaxation, some of the 60° misfit dislocations extended up to 250 nm downward into the constant SiGe layer. Thus, for the oxidized 75 nm thick strained-Si layer, similar process of misfit dislocation formation and motion could occur, and the depth region with 60° dislocations could be of the order of 200 nm, which is pretty close the depth location of *H5* (150 nm) calculated from the voltage dependence of DLTS peak height. Based on the knowledge of the isolated extended defects nature and the near surface location, the DLTS peak *H5* observed after annealing could be attributed to dislocations or to some deformation induced defects created during dislocation motion.

A comparison between the DLTS results of strained-Si/SiGe heterostructure and plastically-deformed *p*-Si deformed in the clean conditions allows to infer that these defects are associated not with dislocations themselves but with the dislocation trails.

Indeed, the *H5* peak is very similar to the spectrum observed in plastically-deformed Si [12], where it was associated with the defects formed in the dislocation trails. In the crystals deformed in the clean conditions, when the dislocation electrical activity was suppressed, these defects are the major electrically active defects introduced during plastic deformation.

In principal, the same defects could be introduced also in the SiGe layers during the threading dislocation motion. It should be noted that defect *H4* revealed at a large depth are similar to *H5* and also demonstrates a similar dependence on filling pulse duration. Such similarity supports the idea that both *H4* and *H5* defects are associated with the same deformation-induced defects. The small difference in the activation energy between the defects *H4* and *H5* could be determined by the difference in their location, since defect *H5* is probably located in the top Si or constant SiGe layer while *H4* in graded SiGe layer.

The nature of *H1-H3* defects located in the uniform SiGe layer is not clear yet but it seems that they could be associated with some point-like defects stable up to 800ºC. And it is well known that point defects can be formed during the dislocation motion and interaction, e.g., jogs, kinks [18].

4. 3. 3. EBIC Measurements

As revealed by the aforementioned DLTS results, some dislocation-related defects were introduced in the top layers of this strained-Si/SiGe heterostructure during thermal annealing at 800ºC. The EBIC measurements were performed employing varying e-beam energies to distinguish EBIC contrasts due to dislocations located at different depths, and to identify the lateral distribution and recombination activity of the extended defects, especially those at the strained-Si/SiGe interface.

Since no additional misfit dislocations are generated in the constant SiGe layer, where the graded SiGe layer reaches its final Ge content and relaxes to its original lattice constant, this 1000 nm constant SiGe layer separates the overgrown strained-Si layer from the graded SiGe layer with high density of dislocations. To detect the extended defects at the strained-Si/SiGe interface, a low-energy e-beam should be used to avoid the influence of the dislocations in the deeper graded SiGe layer. The electron range R_e for an e-beam with energy of 10 keV is calculated to be around 1000 nm [19,20], which means that the volume of carrier generation contains only the strained-Si layer and the constant SiGe layer, not the graded SiGe layer.

At beam energies larger than 10 keV, two-dimensional cross-hatch pattern consisting of dark and bright bands (5-10 μm wide) can be revealed in the EBIC mode in both as-grown and annealed heterostructures, as illustrated in Figure 4-6(a) of EBIC micrograph of as-grown sample obtained at 90 K using 20 keV beam energy. It should be noted that the EBIC micrographs obtained using beam energies ranging from 15 to 35 keV are qualitatively similar for both samples, demonstrating the usual cross-hatch pattern. As seen in Figure 4-6(b), although the contrast of cross-hatch pattern at 10 keV is essentially smaller in comparison with that obtained at 20 keV, the structure of dark lines on the both images obtained in the same place is similar. That means that in spite of rather different electron range (3.7 and 1.0 μm) the same defects are revealed. At low temperatures, the maximum EBIC contrast was observed at 15-20 keV and it reaches a value of about 2-4% for the as-grown samples and of 1-2% for annealed ones, suggesting that the EBIC contrast noticeably decreases after annealing. With temperature increase the cross-hatching EBIC contrast decreases and at 300 K it was 2-3 times smaller than that at 90 K.

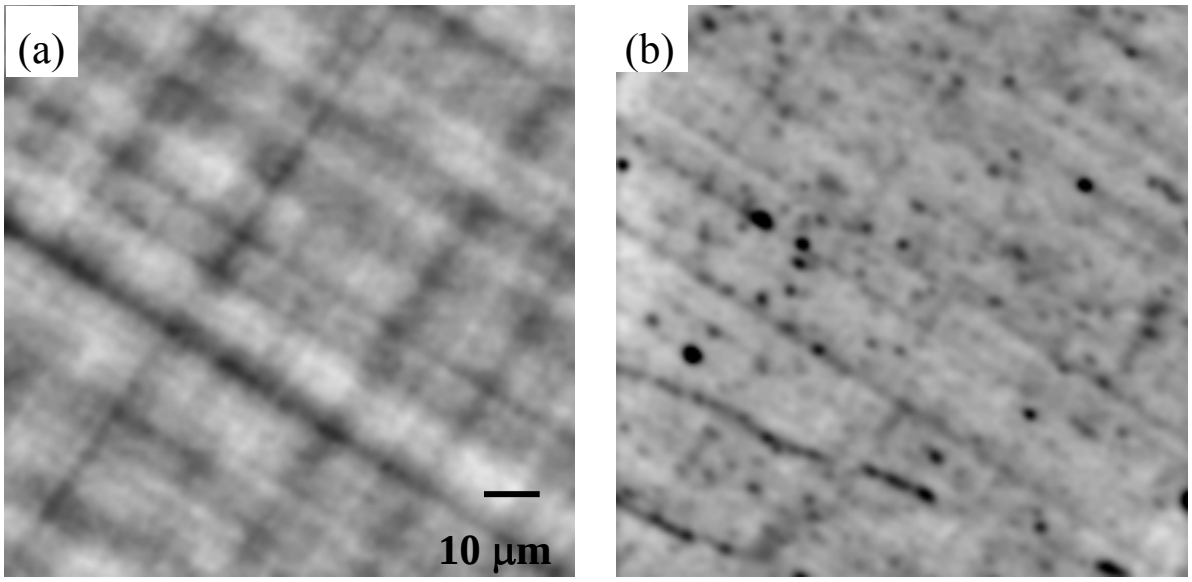

Figure 4-6. EBIC micrographs of as-grown sample obtained at 20 keV (a) and 10 keV (b), respectively. Image size is 100 × 100 μm^2. Note that EBIC micrographs were obtained on the same sample location.

Our calculations using the Donolato model [21] have shown that the contrast associated with defects in the graded SiGe layer should monotonically decrease while reducing E_b, and practically disappears at ~12 keV [22]. Moreover, the image should change with beam energy because misfit dislocations are distributed inside the rather thick layer. Contrary, the images obtained at different energies are very similar, and the cross-hatch pattern is still observable at 10 keV and the contrast reached the maximum at 15-20 keV. If the defects revealed are associated with the dislocation trails formed behind threading dislocations all these results could be easy explained. Indeed, the quasi two-dimensional defects formed behind moving dislocations are known to produce the essential EBIC contrast even in rather clean samples [23,24], while the EBIC contrast from the clean dislocations was very small even at low temperatures. The dislocation trails could extend through all layers and their contrast

disappears when the electron range will be smaller than the effective depletion region width, therefore, this assumption allows to explain the similarity of images obtained at different beam energies. The temperature dependence of EBIC contrast from dislocation trails in *p*-Si [24] was similar to that observed in this study for the cross-hatch EBIC contrast. And at last, such assumption allows also to explain the decrease of EBIC contrast after at 800ºC annealing because, as it was shown in Ref. 23 that the EBIC contrast associated with dislocation trails annealed at 800-850ºC.

Some dark points could be revealed in Figure 4-6(a), which were well seen at 10 keV. In principal, these points could be associated with threading dislocations. However, as indicated by our *C-V* and DLTS measurements, the electrical activity of misfit dislocations is rather low due to the low contamination level in the samples studied. For this reason the electrical activity of threading dislocations should also be low. As investigations of clean dislocations in plastically deformed Si have shown, they could not be revealed in the EBIC mode even at low temperature [23].For this reason to clarify the nature of black points revealed in the EBIC mode at low beam energies additional investigations should be carried out.

4. 4. Conclusion

In summary, the effects of thermal annealing at 800 ºC in oxidizing atmosphere on the electrical properties of strained-Si/SiGe heterostructure were investigated using *C-V*, DLTS, and EBIC techniques. Changes of apparent carrier concentration profile after thermal annealing were identified by *C-V* characteristics, and attributed to the annealing of dislocation-trail related defects within the constant and graded SiGe layers.

By comparing the defect spectrum of as-grown and annealed heterostructures, an

additional DLTS peak was identified for the annealed sample, and this DLTS peak was determined to be of *localized* extended defect nature, and located within 150 nm from the surface from its peak height dependence on reverse and pulse voltages, and filling pulse durations, respectively. The attribution of the DLTS peak to the motion of misfit dislocation during the relaxation of the strained-Si layer suggests that 800˚C oxidation process may be strong enough to relax the metastable strained-Si layer, and result in undesirable dislocations within the MOSFET device regions.

The EBIC measurements employing different temperatures and varying e-beam energies separated the EBIC contrast due to the recombination centers located at different depths. The commonly observed EBIC cross-hatch pattern are attributed to the dislocation trails within constant SiGe layer, due to its contrast dependence on the e-beam energy, temperature, and thermal annealing.

Acknowledgements

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CHAPTER 5: MINORITY CARRIER TRANSIENT SPECTROSCOPY STUDY OF Strained-Si/SiGe/Si HETEROSTRUCTURES

ABSTRACT

Optically excited minority carrier transient spectroscopy (MCTS) is used for the characterization of strained-Si/SiGe/Si heterostructures, focusing on the top strained-Si layer and the strained-Si/SiGe interface. The excitation of minority carriers using optical pulses allows the study of the recombination activities of dislocations located within the depletion region, which are otherwise unable to be filled by traditional deep-level transient spectroscopy (DLTS) using electrical pulses. The minority carrier peaks associated with extended defects, similar to the well-known electron traps of plastically deformed *n*-type Si, are revealed. The characteristics of corresponding level and its depth distribution are analyzed by varying the optical pulse duration and reverse bias voltage. And these observed MCTS peaks are attributed to threading and/or misfit dislocations in the strained-Si and/or uniform SiGe layers.

5. 1. Introduction

Due to the higher electron and hole mobilities in the strained-Si layer than those of bulk Si and very good compatibility to modern complementary metal-oxide-semiconductor (CMOS) technology, strained-Si is becoming a promising candidate to replace traditional bulk Si in high-performance CMOS fabrication process [1,2]. A general strategy for fabricating the strained-Si channels is to grow a graded SiGe layer on top of standard Si substrate followed by a uniform SiGe buffer layer, and finally overgrow a thin strained-Si layer. A tensile strain in the top thin Si layer is introduced due to the lattice-mismatch between strained-Si and relaxed SiGe layers.

During the growth of strain-relaxed graded SiGe layer, mismatch strain is gradually relaxed by a modified Frank–Reed (MFR) mechanism [3,4], and the majority of 60° misfit dislocations (MDs) formed during the relaxation process are trapped within the SiGe graded layer. However, some of these dislocations may thread to the surface of strained-Si device layer, and degrade the final MOSFET device performance at the strained-Si surface by increasing the leakage current [5,6,7]. Accordingly, the threading dislocations (TDs) with a typical density of 10^4–10^6 cm^{-2} must be characterized and controlled. Furthermore, if the thickness of the tensile-strained Si epilayer exceeds the predicted critical thickness, it becomes energetically favorable to relieve the mismatch strain through the introduction of MDs at the strained-Si/SiGe interface [8,9], which may induce a strong scattering potential for the charge carriers in the strained-Si, and disadvantageously affect the carrier mobilities [10].

Thus, for successful practical application of strained-Si, it is essential to be able to determine the concentration and electrical properties of dislocations within the strained-Si layer, and near the strained-Si/SiGe interface. So far, preferential etching/Nomarski optical

microscopy, and transmission electron microscopy (TEM) have been extensively applied to study the defect structures of strained-Si top layer [11,12,13]. However, there are limited reports on the electrical characterization of the performance-degrading extended defects [14] of the strained-Si/SiGe heterostructures. Recently, we identified a near-surface (less than 150 nm deep) extended defect in the thermally annealed metastable strained-Si/SiGe/Si heterostructure using deep-level transient spectroscopy (DLTS) technique, and related it to the formation and motion of misfit dislocations at the strained-Si/SiGe interface [15].

However, the main obstacle to the electrical characterization of the deep levels of threading and/or misfit dislocations is the very thin layer of top strained-Si. For a semiconductor containing deep levels, there is a transition region, situated within the depletion region, where the conducting conduction/valence band is empty of free charge carriers, but the traps are still filled. Thus the filling and emptying of deep levels using electrical pulses is prohibited for depths smaller than W-λ (W is the width of depletion region, and λ is the length of the transition region), and the DLTS technique carried out on Schottky barrier diodes is unable to detect deep levels located inside of the transition region [16]. The values of the depletion region width W and the transition length λ can be calculated using the following expressions:

$$W = \frac{\varepsilon\varepsilon_0 A}{C}, \qquad \textbf{(Eq. 5. 1)}$$

$$\lambda = \sqrt{\frac{2\varepsilon\varepsilon_0}{q^2 N_A}(E_F - E_T)}, \quad . \qquad \textbf{(Eq. 5. 2)}$$

where ε_s is the relative dielectric constant of the semiconductor, ε_0 the Permittivity of vacuum,

A the Schottky contact area, C the measured sample capacitance at voltage V, q the electronic charge, N_A the free carrier concentration of p-type semiconductor, E_F the Fermi energy level, and E_T the trap energy level within the energy band gap. Thus, the direct measurement of extended defects of the strained-Si layer using conventional DLTS technique is still limited, due to the thin layer thickness and its low doping concentration.

To overcome the limited applicability of the conventional DLTS for near-surface defects, we present in this paper a detailed analysis of the dislocation-related defect levels for strained-Si top layers using minority carrier transient spectroscopy (MCTS) method. Unlike DLTS which fills deep levels using electrical pulses, MCTS injects minority carriers by directing a light pulse of above-band-gap energy on a semitransparent Schottky diode to excite both majority and minority carriers. The majority carrier generated in the neutral material is prevented from entering the depletion region by the electric field, whereas minority carriers generated in the neutral material within a diffusion length are extracted by the depletion field, resulting in a higher concentration of minority carriers within the depletion region. Thus, MCTS can effectively fill and empty the defect levels located within the W-λ layer, enabling the detection of deep levels located within strained-Si layer, and/or constant SiGe layer.

It is important to note that the information of minority carrier defects at the strained-Si/SiGe interface, and their capture and emission kinetics is essential for the optimum performance of strained-Si MOSFETs, which functions by transporting minority carriers along the strained-Si inversion channel region. The investigation of electron traps on the upper half of the band-gap using MCTS technique provides the opportunity to compare the observed electron traps with those in the extensive literature of plastically deformed n-type Si

[17,18,19,20], and SiGe/Si heterostructures [21,22,23].

5. 2. Experimental Details

Strained-Si/SiGe/Si heterostructures of different strained-Si layer thicknesses were used in this study. The *p*-type strained-Si/SiGe/Si-substrate heterostructure was synthesized by chemical vapor deposition using either SiH_4 (for strained-Si layer) or SiH_2Cl_2 and GeH_4 (for SiGe layer) as source gases. A fully relaxed constant $Si_{0.8}Ge_{0.2}$ layer was grown a compositionally-graded SiGe layer on a *p*-type Si (001) substrate. Subsequently, a strained-Si layer was grown on top of the constant $Si_{0.8}Ge_{0.2}$ layer to a thickness smaller or larger than the critical thickness (about 20 nm) [8] to represent a fully-strained Si layer with only threading dislocations, or a metastable one which may have misfit dislocations at the strained-Si/SiGe interface. The thicknesses of strained-Si, uniform SiGe and graded SiGe layers are 15, 2500, and 2000 nm for the fully-strained sample, and 73.5, 1000, and 670 nm for the metastable one, respectively.

To study the thermal stability of metastable strained-Si layer, the as-grown 73.5-nm-thick strained-Si/SiGe/Si heterostructure was divided into two parts, and one of them was annealed at 800˚C in oxidizing atmosphere to grow a 10 nm thick oxide to represent the conventional gate oxide growth process.

For an estimation of the dislocation density and the degree of strain relaxation, samples were etched with a Schimmel etchant (1 part 0.15 M $K_2Cr_2O_7$: 2 parts 49% HF) for different time, and etch pit densities were evaluated from Nomarski optical micrographs.

Semitransparent Schottky diodes were prepared by evaporation of a thin Aluminum layer on top of the strained-Si layer. Current-voltage (*I-V*) characteristics were

measured in the dark or under illumination to ensure low leakage current and optical transparency necessary for MCTS measurements. Note that thermally-grown oxide of the annealed sample was removed using a diluted HF solution before preparing the Schottky contacts. The back ohmic contacts were prepared by rubbing Ga–In eutectic on the back side.

Capacitance-voltage (*C-V*) and MCTS measurements were carried out using a BioRad DL8000 digital DLTS system in the temperature range from 50 K to 300 K at a frequency of 1 MHz. The optical injection for MCTS measurement was realized by a GaAs/GaAlAs double heterostructure laser with a wavelength of 850 nm. Laser pulse duration (t_P) can be varied from 0.005 to 10 ms. The apparent charge carrier depth profile of as-grown 15-nm-thick strained-Si/SiGe/Si heterostructure was measured using spreading resistance profiling (SRP) technique.

5. 3. Results

5. 3. 1. As-grown Strained-Si/SiGe/Si Heterostructures

To better reveal etch pits due to threading dislocations, dark-field Nomarski optical micrographs of chemical etched as-grown 15-nm-thick and 73.5-nm-thick samples were taken, and shown in Figure 5-1(a) and (b), respectively. The densities of TD (white spots) in Figure 5-1 are estimated to be about 1.4×10^5 cm^{-2} and 1.6×10^4 cm^{-2}, respectively. It is important to note that the etch pit density did not change with increasing etching time, and no line features due to MDs were detected, indicating that both of the as-grown samples are fully strained.

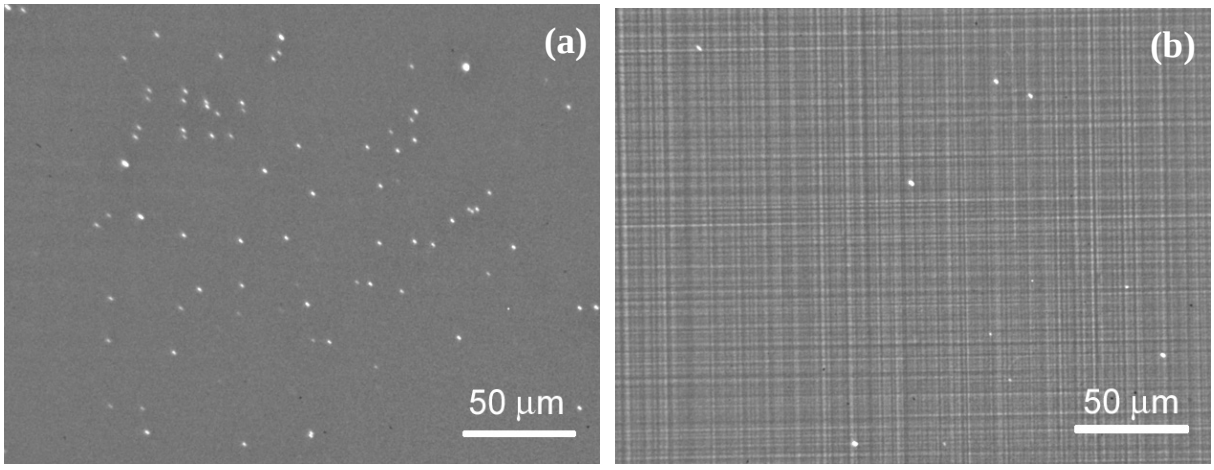

Figure 5-1. Dark-field Nomarski optical micrographs of etch pits delineated using preferential etching for 15-nm-thick (a), and 73.5-nm-thick (b) strained-Si/SiGe/Si heterostructures.

For MCTS measurements, modest values of reverse bias voltage V_R were used, to ensure that the probing region of MCTS, i.e., the depth of W-λ, were kept within the strained-Si and constant SiGe layers, to avoid the complication caused by the graded SiGe layer with dense dislocations, and to increase the sensitivity of MCTS.

Figure 5-2 shows typical MCTS spectra of as-grown 15-nm-thick strained-Si/$Si_{0.8}Ge_{0.2}$/Si heterostructure using different reverse bias voltages V_R. An electron trap was observed at a temperature of ~175 K. Note that the peak heights of MCTS spectra remain relatively constant, with increasing V_R, indicating a uniform depth distribution of this electron trap within the strained-Si and constant SiGe layers (the value of W-λ is calculated to be about 430 nm for 0 V, and 1400 nm for 3V from the corresponding C-V characteristics). The depth profiling of defects using MCTS will be discussed in more details later.

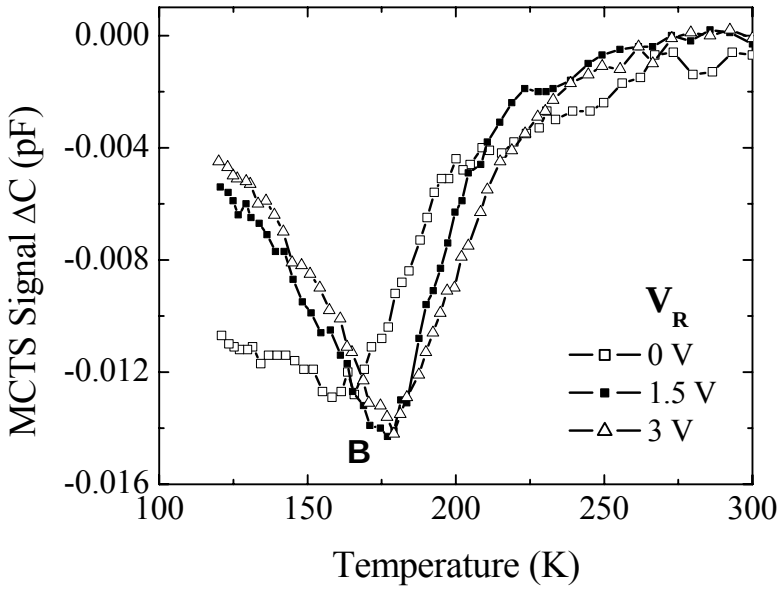

Figure 5-2. MCTS spectra of as-grown 15-nm-thick strained-Si/SiGe/Si heterostructure samples using an optical pulse of 1 ms for different reverse bias voltages V_R. t_W = 20 ms.

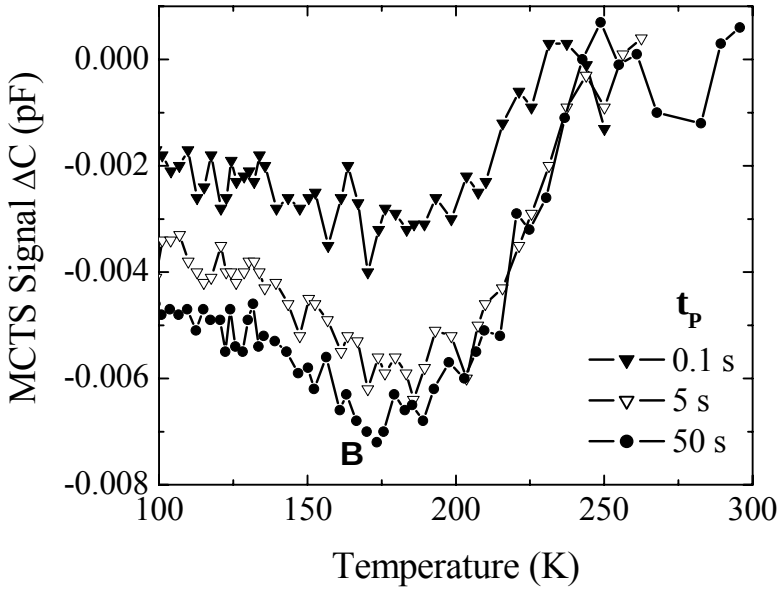

Figure 5-3. MCTS spectra of as-grown 73.5-nm-thick strained-Si/SiGe heterostructure samples for optical filling pulse durations t_P of 0.1 s, 5 s, and 50 s. The reverse bias V_R was kept at 0 V. t_W = 20 ms.

An electron trap with the same peak temperature was observed for the as-grown 73.5-nm-thick strained-Si/$Si_{0.8}Ge_{0.2}$/Si heterostructure using MCTS measurement, as shown in Figure 5-3. Note that the peak height for the 73.5-nm-thick sample is only half of that for 15-nm-thick sample.

It has been established that DLTS technique can distinguish point defects and extended defects based on their different capture kinetics of majority charge carriers [24], and the validity of this criterion was extended to the case of minority carrier by Grillot *et al.* [25]. The filling of an extended defect by charge carriers is usually modeled by a time-dependent Coulomb barrier $\Phi(t)$ which builds up during the capture process of charge carriers, and the resulting logarithmic time dependence of DLTS peak height can be described by the following expression:

$$n_T(t_P) \propto \ln(t_P), \qquad \textbf{(Eq. 5. 3)}$$

where n_T is the density of filled traps, and t_P the filling pulse duration. While the charge carrier capture kinetics is different for point defects, with an exponential time dependence:

$$n_T(t_P) = N_T[1 - \exp(-\langle v_{th} \rangle \sigma n t_P)]. \qquad \textbf{(Eq. 5. 4)}$$

Here, N_T is the total trap density, $\langle v_{th} \rangle$ the mean electron thermal velocity, σ the electron capture cross section, n the electron density.

Thus, the nature of this electron trap can be further clarified by measuring the MCTS signal dependence on optical filling pulse duration t_P, see Figure 5-3. Albeit the noise in the MCTS spectra because of low trap density, a clear logarithmic dependence of MCTS peak height on pulse duration is observed, indicating that the electron trap observed for as-grown

strained-Si heterostructure is related to extended defects, rather than homogeneously distributed point defects.

Since both of the as-grown samples were identified as fully-strained from the preferential etch/optical microscopy study (see Figure 5-1), only threading dislocations are expected to be present within the strained-Si and constant SiGe layers, which were defined by the values of V_R used for MCTS measurements. Thus, the extended defect-related electron trap is attributed to threading dislocations, and labeled as the *B* line, according to the classification of deep levels in plastically deformed Si by Omling *et al.* [17].

Due to the inhomogeneous doping profile, the direct calculation of electron trap concentration for as-grown 73.5-nm-thick sample is difficult to perform. Only the trap density of as-grown 15-nm-thick sample with a relatively-uniform doping profile can be estimated from the MCTS signal following the same equation as the conventional DLTS:

$$N_T = 2\frac{\Delta C}{C}\left(\frac{w}{w-\lambda}\right)^2 N_A, \qquad \textbf{(Eq. 5. 5)}$$

where N_T is the trap density, N_A the apparent acceptor concentration, ΔC the height of MCTS peak, and C the capacitance at reverse bias V_R. The value of electron trap density for the as-grown 15-nm-thick samples is estimated to be around 3.8×10^{11} cm^{-3}. From the comparison of electron trap (volume) density and etch pit (area) density, the number of traps per length of dislocation can also be calculated to be 2.7×10^{6} cm^{-1}, which is consistent with the predicted value by Kveder *et al.* [26], thus confirming the assignment of MCTS peak at 175 K to threading dislocations.

The assignment of this electron trap to threading dislocations is also in agreement with the observation of a majority carrier (electron in this case) trap at ~175 K for *n*-type

$Si/Si_{1-x}Ge_x/Si$ heterostructures using conventional DLTS technique [22,23]. It was proved that the electron trap in the *n*-type Si/SiGe/Si heterostructure also has a rather uniform depth distribution [23], and the trap concentration is proportional to the threading dislocation density [22]. Note that Si cap layers in the *n*-type Si/SiGe/Si heterostructures are several micrometers thick, different from the strained-Si layer with a thickness of tens of nm.

5. 3. 2. Thermally-Annealed Metastable Strained-Si/SiGe/Si Heterostructure

After preferential etching, a strong increase of etch pit density was observed for the thermally-annealed 73.5-nm-thick sample than the as-grown one. This dramatic increase of threading dislocation density after thermal annealing indicates that the mismatch strain of top Si layer relaxes through the formation of dislocation half-loops, consistent with the meta-stability of the 73.5-nm-thick strained-Si top layer.

Accordingly, a drastic increase in the electron trap concentration was observed for the 73.5-nm-thick sample after thermal annealing at 800˚C (Figure 5-4), as compared to that of as-grown sample (Figure 5-3). The electrical properties of three MCTS electron traps have been calculated from the corresponding Arrhenius plots of the thermal emission rates e_n versus the inverse temperature, and their characteristic parameters including energy level within the energy band gap, capture cross section, and trap concentration are reported in Table 5-1. Although the data scatter, it is clear that these electron traps detected by MCTS for annealed metastable strained-Si are the same group of deep levels for plastic deformed *n*-type Si, will be labeled as the *A*, *B*, and *C* lines, following the notation of Omling *et al.* [17]. Note that the B line is also observed for the as-grown strained-Si sample with a much lower concentration, and attribute to threading dislocations.

Since the strain-relaxation process of top Si layer is similar to the plastic deformation of bulk Si, the observation of the same set of deep levels in *n*-type Si created by plastic deformation is not un-expected. It is interesting to note that the metastable strained-Si relaxes during the thermal annealing at 800 ºC, which is comparable to the annealing temperature of plastically-deformed Si to remove the thermally unstable states [17,18,19]. As a result, the generation and annealing of dislocation-related defects are simultaneously occurring during the thermal processing of metastable strained-Si layer.

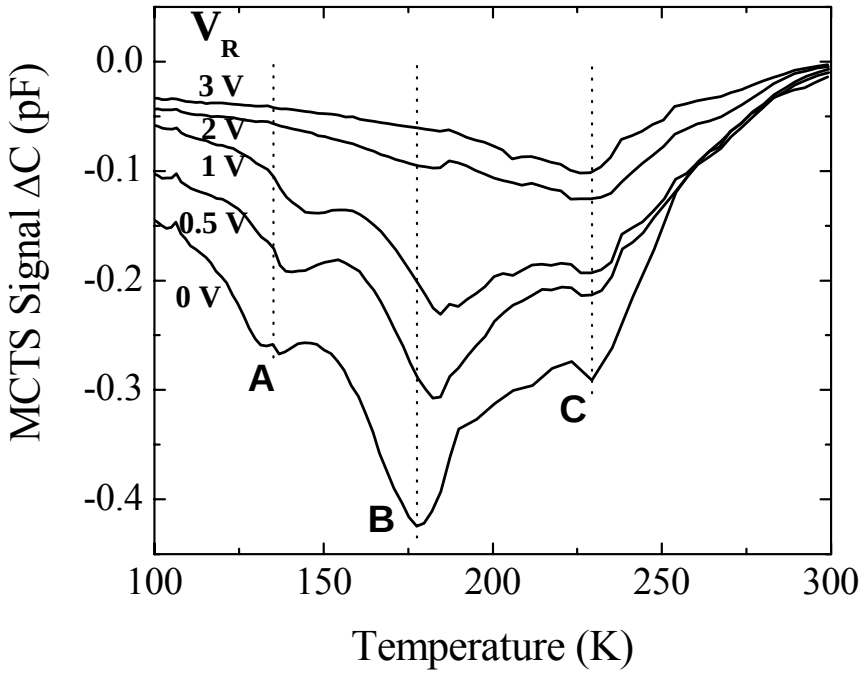

Figure 5-4. MCTS spectra measured on thermally-annealed sample, for different reverse bias V_R, while optical pulse duration t_P = 0.1 ms, and emission rate e = 50 s^{-1}.

Table 5-1. Electrical properties of MCTS peaks of thermally-annealed 73.5-nm-thick strained-Si/SiGe/Si heterostructure, including trap energy level within the energy band gap, and trap concentration.

Trap	E_a (eV)	N_T (cm^{-3})
A	0.19	4×10^{13}
B	0.26	6.5×10^{13}
C	N/A	5×10^{13}

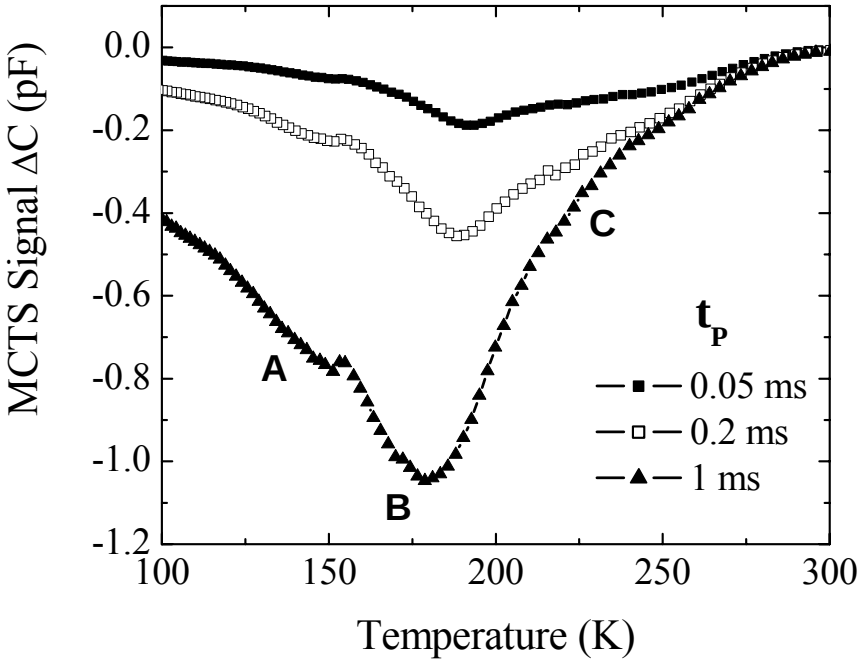

Figure 5-5. MCTS spectra measured on thermally-annealed sample. Dependence on the optical filling pulse duration t_P. The fixed parameters are the reverse bias V_R = 1.0 V and emission rate e = 50 s^{-1}.

In order to prove that electron traps *A*, *B*, and *C* are actually related to dislocations (or extended defects), we studied the capture kinetics of MCTS signals by varying the optical filling pulse duration, and the results are shown in Figure 5-5. Despite of the overlapping of neighboring MCTS peaks, we still can see that the MCTS peak heights of the *A* and *B* lines scale with the logarithm of the filling pulse duration t_P. This logarithmic dependence

also appears to be true of the *C* line, but this less certain since the MCTS peak *C* becomes a shoulder of peak *B* when the filling duration is increased further to 1 ms.

As shown in Figure 5-5, the position of the dominant *B* line peak shifts towards lower temperature with an increasing filling pulse duration t_P for thermally-annealed 73.5-nm-thick sample, indicating a band-like nature of defects consisting of a distribution of deep levels [24]. And the formation of band-like deep levels was proposed to be caused the fluctuations of point defect densities around dislocations due to inhomogeneous plastic deformation [19].

The determination of the distribution of deep levels within the band gap for lines *A* and *C* was influenced by the overlapping of the dominant *B* line, especially for longer filling pulse durations. To avoid the uncertainty introduced by neighboring peaks, we performed a set of MCTS measurements by varying the reverse bias voltage V_R, while employing a moderate value of filling pulse duration of 0.1 ms. Knobloch *et al.* proposed that for the dislocations located at a certain depth, e.g., at the interface of Si and SiGe layers, the band bending can be increased by applying a larger reverse bias V_R, to enable the emission of electrons from the deeper dislocation-related states [23]. Thus, the broadness of the energy distribution of dislocation-related defects can be measured from the extent of MCTS peak position shift towards higher temperatures with increasing V_R.

As shown in Figure 5-4, the peak position of the *C* line remained fixed at the same temperature of 229 K, when reverse bias V_R is varied from 0 V to 3 V. Accordingly, the C line is due to a narrow energy distribution of dislocation-related states. As for the B line, there is a small shift of the MCTS peak from 177 K at V_R = 0 V to 185 K at 2V, while the most drastic shift of peak temperature is observed for the *A* line from 135 K at 0 V to 148 K at 1 V. Consequently, the width of energy distribution ΔE of the dislocation-related defects A and B

are determined to be 25, and 15 meV, respectively, according to the measured MCTS peak temperature shifts.

5. 3. 3. Depth Distribution of Electron Traps in Strained-Si/SiGe/Si Heterostructures

Although the exact determination of electron trap density of the strained-Si/SiGe/Si heterostructures was difficult due to the inhomogeneous doping profile, as well as the non-uniform distribution of minority carriers injected by optical laser within the depletion region [27]. Still, the observed MCTS peak height dependence on reverse bias voltages V_R can be qualitatively modeled, since the doping profiles of the samples are largely constant in the constant SiGe layer, according to the C-V characteristics. Note that the as-grown 15-nm-thick sample has an almost uniform doping concentration of 1.3×10^{15} with about 15% fluctuation, according to the SRP results. Thus, to simplify, we will use the 15-nm-thick sample as an ideal sample with a uniform doping of 1.3×10^{15} cm^{-3}.

For the case of a deep level with uniform concentration of N_T, according to the Eq. 5.5, the measured MCTS signal ΔC for a saturating filling pulse can be expressed as

$$\Delta C = \frac{1}{2} C \left(\frac{w-\lambda}{w} \right)^2 \frac{N_T}{N_A} = \frac{1}{2} \frac{(w-\lambda)^2}{w^3} \frac{N_T}{N_A} \varepsilon_s \varepsilon_0 A = cons\tan t \times \frac{(w-\lambda)^2}{w^3}. \quad \textbf{(Eq. 5. 6)}$$

On the other hand, for the case of a deep level located only within the top strained-Si layer, i.e., within the W-λ layer for the bias voltage of 0 V, the measured MCTS signal ΔC can be calculated to have the following dependence on W or C

$$\Delta C = \frac{1}{2} \frac{(W_0-\lambda_0)^2}{W^3} \frac{N_T}{N_A} \varepsilon_s \varepsilon_0 A = cons\tan t \times \frac{1}{W^3} = cons\tan t \times C^3. \quad \textbf{(Eq. 5. 7)}$$

The measured values of MCTS peak heights as a function of reverse bias voltage

V_R are plotted in Figure 5-6, together with the theoretical curves for the two cases of uniform defect concentration throughout the whole heterostructure, or only at the top Si layer. From the comparison of experimental results and the two ideal cases, it is evident that the *B* lines of two as-grown samples have a uniform defect concentration throughout the whole constant SiGe layer, while the defects of thermally-annealed 73.5-nm-thick sample are mainly located within the *W*-λ layer for V_R of 0 V (i.e., 150 nm), the upper part of the constant SiGe layer. So, the experimentally-determined depth distributions of electron traps are consistent with the previous assignment of electron traps to threading dislocations, or misfit dislocations.

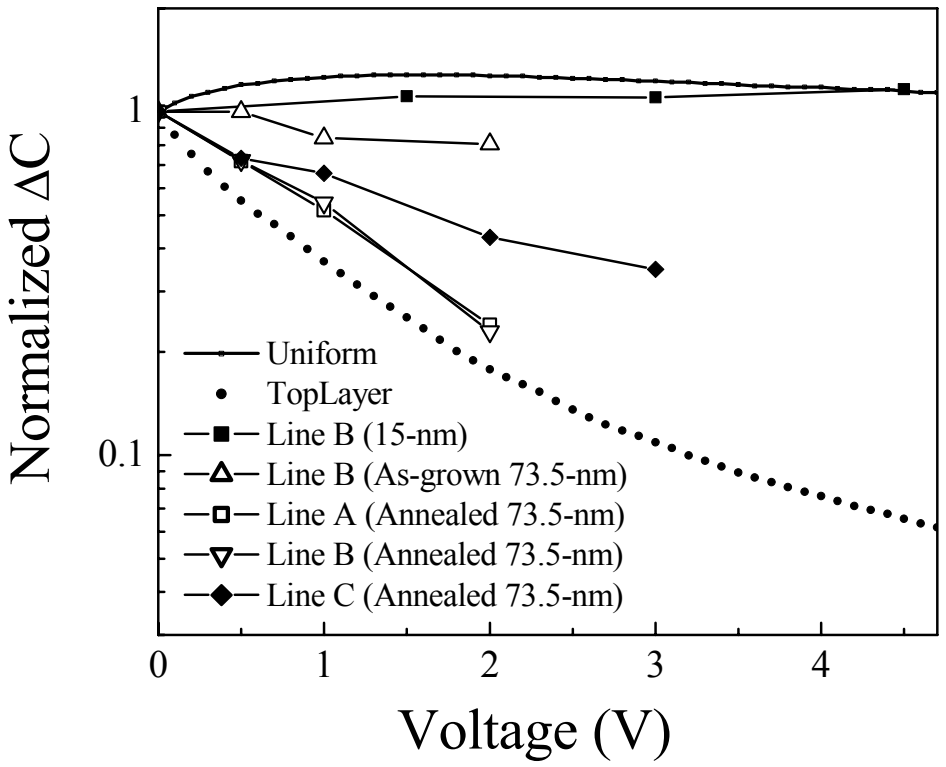

Figure 5-6. Dependence of normalized MCTS peak heights on the reverse bias voltage V_R for electron traps of different samples: the *B* lines of as-grown 15-nm-thick, and 73.5-nm-thick samples, the *A*, *B*, *C* lines of thermally-annealed 73.5-nm-thick sample. The theoretical curves for two ideal cases of uniform defect concentration, or defect located within the

W-λ layer for V_R of 0 V are also included for comparison.

5. 4. Discussion

From the extensive work on plastically deformed *n*-type Si, it was concluded that electron traps *A*, *B*, and *D* are mainly due to point defects generated during the plastic deformation, which are not necessarily localized at dislocations [17,18,20]; while trap *C* was attributed to a narrow point defect cloud surrounding 60º dislocations with a radius of ~ 1 nm from computer simulations [24]. The MCTS results of broad energy distributions for electron traps *A* and *B*, and a narrow distribution for trap *C* of *p*-type annealed heterostructure is consistent with the prior identification of point defects located close to, or at dislocation core, respectively.

The MCTS results of the thermally-annealed 73.5-nm-thick strained-Si/SiGe/Si heterostructure will be compared to the previous DLTS results on the same sample [15], to yield information of recombination centers at both upper and lower half of the band gap. Indeed, a prominent new hole trap level was detected using DLTS technique for the metastable strained-Si/SiGe/Si heterostructure only after thermal annealing 800 ºC. The hole trap, labeled as *H5*, is located less than 150 nm from the surface from the DLTS peak height dependence on reverse bias voltage V_R, and exhibited an identical capture kinetics of holes as that of electrons for the *C* line in *n*-type Si [24]. Therefore, it is likely that the majority carrier trap *H5* generated during the strain relaxation of the metastable strained-Si layer has the same microscopic structure as that proposed for the *C* line [24]: point-defect clouds surrounding 60º dislocations.

Since the activation energy of the hole trap *H5* was determined to be 0.43 eV from the

corresponding Arrhenius plot, and the activation energy of the missing electron trap *D* is 0.56 eV from the previous extensive work [18,20], the sum thermal activation energies for both trap is close to the SiGe band gap (≈1.0 eV). Thus we propose that the hole trap *H5* is actually the missing electron trap *C*. This would suggest that this trap level interacts with the conduction and the valence band as we should expect from a neutral recombination center, capable of capturing both majority and minority carriers as a recombination center.

5. 5. Conclusion

Thus, optically excited MCTS has been successfully applied for studying the electron traps of as-grown or thermally-annealed strained-Si/SiGe/Si heterostructures, and identified the electron traps related to threading or misfit dislocations. The excitation of minority carriers using optical laser pulse allows the study of the recombination activities of dislocations located within the depletion region (the Si top layer and the strained-Si/SiGe interface), which are otherwise unable to be filled by conventional DLTS electrical pulsing.

One minority carrier trap was identified for as-grown strained-Si/SiGe/Si heterostructure, and attributed to threading dislocations because of its charge capture kinetics, the correlation of trap concentration and etch pit density, and the MCTS peak height dependence on V_R.

High densities of electron traps were observed for the annealed 73.5-nm-thick sample, and were associated with the well-known electron traps of plastically deformed *n*-type Si. The capture kinetics and depth distribution of these electron traps were studied by varying filling pulse duration t_P, and reverse bias V_R. Also, the electron traps observed by MCTS were compared with the hole trap previously detected using DLTS, and related to a depth of less than 150 nm, which is consistent with the proposed formation mechanism through the

strain-relaxation of top metastable strained-Si layer.

Acknowledgements

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SUMMARY

The detrimental effects of threading and misfit dislocations at the interface of strained-Si/SiGe layers on electrical device performance have been well established, and these extended defects can be studied using various structural characterization methods. However, there is limited understanding of deep levels related to dislocations, mainly due to the very small thickness (tens of nm) of top strained-Si layer.

A set of strained-Si/$Si_{0.8}Ge_{0.2}$/Si heterostructures with different strained-Si layer thicknesses and thermal processings was used in this study to represent fully-strained Si layer with only low density of threading dislocations, and partially-relaxed one with high density of misfit dislocations. These extended defects were characterized using a combination of electrical techniques (*C*-*V*, DLTS, MCTS, and EBIC), and preferential etching/Nomarski optical microscopy.

A temperature dependence of *C*-*V* curves was identified for the Schottky diodes, and attribute to hole traps in the graded SiGe layer with dense misfit dislocations. This observation serves as a basis for the depth profiling of defects using capacitance-based DLTS and MCTS techniques. DLTS has been successfully applied to monitor the dislocation formation of a metastable strained-Si layer after 800 ˚C thermal processing, and identified a near-surface (less than 150 nm deep) extended defect, likely a result of the dislocation motion in the upper part of constant SiGe layer.

The advantages of optically-excited MCTS for detecting minority carrier trap levels within the depletion region of Schottky diode has demonstrated for both fully-strained and

partially-relaxed Si top layers. For as-grown samples with different threading dislocation densities, one electron trap was observed, and its volume density increases linearly with threading dislocation density. This observation allows the attribution of the electron trap to threading dislocations. The MCTS spectra of partially-relaxed sample were analyzed, and a good agreement was found between the electron traps of strained-Si/SiGe/Si heterostructure with those of plastically deformed *n*-type Si.