Abstract

CHANDRASEKAR, KARTHIK. Inductively Coupled Connectors. (Under the direction of Dr. Paul Franzon).

AC coupled interconnects show promise to enable multi-gigabit/second data rates between high pin count IC’s within a multi-chip module, while achieving significant power savings as well [3]. AC Coupling can be realized with planar inductive or capacitive elements. Inductive coupling offers many degrees of freedom for system design by varying geometric parameters to tune parasitic elements in the model, such as: the crossover capacitance between the spirals, the magnetic coupling coefficient, winding resistance, inductance ratio and impedance terminations. So far, inductively coupled interconnects have mainly shown potential for multi-Gbps signaling only in level 1 interconnections, i.e. direct chip to chip communication and 3D IC’s. Multi-Gbps pulse signaling is demonstrated with inductively coupled interconnects across packaging interfaces in this dissertation. This shows feasibility of realizing sub-mm pitch, true Zero Insertion Force (ZIF) surface mount connectors and sockets (i.e. level 2 and level 3 interconnections). Inductors are fabricated on two opposing surfaces, e.g. the faces of a connector or socket. When mated, they form a transformer, which is used to carry signals through the mated interface. The main advantage of building a separable connection this way, is that it is possible to achieve a high density with a simple mechanical structure. This in turn, offers potential for cost reduction and support for true three dimensional packaging. Being a true zero-insertion force interface, very high pin counts could be easily supported. ZIF sub-mm pitch surface mount inductive connector technology also
addresses some of the signal integrity problems inherent in pressfit style connectors. It is difficult to use capacitive coupling for this application, because the structure is placed in the transmission line, not at one end. Thus both the driving impedance and load being driven is 50 ohms. The high, frequency-dependent impedance of a series capacitor would lead to reflection noise (i.e. return loss). Unless large capacitors or lossy codes guaranteeing only high frequency content are used, the transmitted swing would be too small (i.e. excessive insertion loss). In contrast, inductively coupled connectors can achieve broad band matching impedance and give acceptable values to return and insertion losses. Methods to optimize signal integrity are discussed in detail for inductively coupled systems in this dissertation. The signaling data rate achieved in this system is from 1 Gbps to 8.5 Gbps, which depends on the 3 dB coupling frequency of the composite channel consisting of the inductive interconnections and the transmission lines.
Inductively Coupled Connectors

by
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Biography

Karthik Chandrasekar was born in Chennai, India in October 1978. He finished his Bachelor’s degree in Electrical and Electronics Engineering at Sri Venkateswara College of Engineering (SVCE), Chennai in May 2000. He received his MS degree in Computer Engineering at North Carolina State University (NCSU) in August 2002. He started the PhD program at NCSU in August 2002 and is expecting to finish by November 2008. His PhD research topic involves investigating inductive coupling for connector and socket applications. He investigated several research topics including on-chip inductance issues for multi-metal layer VLSI layouts and deembedding procedures for on-chip interconnects before arriving at his PhD topic. He spent summer of 2005 interning with nVidia, Santa Clara in the Substrate design group. In the long term he is interested in a career in areas spanning signal integrity, package layout and modeling, RF IC design and custom circuit design for high speed serial links.
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1 Introduction

1.1 Problem Statement

The demands for high density, high bandwidth interconnections are ever increasing with the growing complexity of today’s high performance designs. Number of signal pins and the operating frequency in chip applications are on the upsurge and the product doubles every 28 months based on Intel’s data [91]. As the number of signal pins and operating frequency on chip rises, the demand for off-chip bandwidth also rises for effective system level integration. IC packages are mounted on daughter boards which in turn are mounted on larger motherboards. AC coupled interconnects show promise to enable multi-gigabit/second data rates between high pin count IC’s within a multi-chip module, while achieving significant power savings as well [3]. AC Coupling can be realized with planar inductive or capacitive elements. Inductive coupling offers many degrees of freedom for system design by varying geometric parameters to tune various elements in the model, such as: the crossover capacitance between the spirals, the magnetic coupling coefficient, inductance ratio, winding resistance and impedance terminations. Inductively coupled interconnects have shown potential for multi-Gbps signaling in chip to chip communication and 3D IC’s [3, 14, 97]. This has application in level 2 (package to board) and level 3 (board to board) interconnections as well. Traditionally, the backplane and IC socket industries have relied on press-fit style designs which are easy to mass assemble reliably. However, these structures
require plated through hole vias, for mating with pins, which present impedance discontinuities that cause reflections and disrupt the return path. This increases return path inductance and crosstalk, particularly at >= 1 Gbps data rates [2]. Mechanically mated connectors and sockets are also subject to wear and tear due to insertion force and repeated use. Surface mount backplane connectors offer electrical advantages over conventional press-fit style designs, but they suffer from coplanarity issues and offer less mechanical robustness and reliability [2]. To have an application in real world commercial designs, inductive connectors or sockets need to be able to achieve Gbps signaling at a sub-1.3 mm pitch to compete with other connectors and sockets available commercially [46, 47, 84]. The central objective of this dissertation is to determine if a surface mount, zero-insertion-force inductive connector can achieve Gbps signaling with pitches of 1.3 mm or less and to establish the design rules and tradeoffs. Figure 1.1 shows a high level view of the inductively coupled interface.

Figure 1.1: Inductively coupled interface
1.2 Dissertation Overview

Chapter 2 reviews previous work by other researchers in key areas related to this work. Chapter 3 discusses theory, design methodology and tradeoffs for inductively coupled connectors. Chapter 4 establishes basic proof of concept for inductive connectors through experimental work and analysis. Chapter 5 establishes the potential and limitations of fine pitch connectors for multi-Gbps pulse signaling through experimental work, modeling and analysis. Chapter 6 discusses design procedure for inductively coupled connectors and shows a design example to illustrate the procedure. Chapter 7 discusses conclusions and future work.

1.3 Contributions

1. Inductively coupled interconnects are evaluated for sub-1.3mm pitch backplane connector and socket applications at Gbps signaling data rates. Inductive coupling has not been studied or applied previously for this application. This work establishes viability of a true zero insertion force (ZIF) surface mount connector technology which can address some of the inherent signal integrity problems with press fit connector technology. Future potential and limitations of this technology are established.
2. Tradeoffs involved in optimizing transformer performance by varying inductance values, coupling coefficient, winding phase, crossover capacitance and series terminations have been documented in the context of the application. Methods to control reflections and signal integrity have been established. Transformers have been used typically in RF/Microwave applications and more recently in point to point high speed digital signaling systems. Using transformers in distributed backplane systems brings additional challenges. Correlation between frequency domain and time domain performance metrics has been well understood and applied in the context of this application.

3. Basic feasibility for a contactless inductive connector was established through RF and digital measurement and analysis of coarse pitch experiments on low cost printed circuit boards. 400 Mbps~3.3 Gbps signaling was demonstrated with 2.5 mm ~10 mm outer diameter transformers.

4. Feasibility for fine pitch inductive connectors for Gbps signaling was established through RF and digital measurement/ analysis of experiments on a 3-layer substrate process with buried bumps. 1.25~8.5 Gbps signaling was demonstrated with 100 µm outer diameter transformers.

5. Simple modeling approach is presented for inductive interconnections in the context of socket and connector applications. Models have been validated with measurement. Design procedure, engineering tradeoffs and guidelines are established for inductive connector design.

6. Transformer geometries spanning a wide range from 100 µm outer diameter to 10 mm outer diameter have been characterized, modeled and understood. This represents a large
database of readily available measurement data. A designer can plug in actual measured results to evaluate feasibility of particular inductive connector geometry in a specific application without relying on extensive modeling.

1.4 Publications during PhD

1.4.1 First Author Publications


1.4.2 Other Publications


2 Literature Review

2.1 Overview

The sections below discuss previous work by other researchers in conceptual areas which are relevant in the context of designing a high density, high bandwidth AC coupled system. Several researchers have investigated AC coupling for a wide variety of applications and the sections below review some of the key contributions which are relevant in the context of designing a high density, high bandwidth AC coupled connector system. Section 2.2 reviews previous work on AC coupling which has been applied in a wide variety of analog circuit designs, chip to chip communication in MCM’s, Level 1 packaging and 3D IC’s. However it is yet to be applied in Level 3 and Level 2 interconnections which are the focus of this work.

This work is based on using inductive coupling to transmit information in printed circuit boards and packaging interfaces at GHz range frequencies. Accurate models for spiral inductors and stacked transformers are critical to achieve desired performance. There is a huge body of literature associated with modeling these elements at GHz frequencies on silicon substrates; probably more compared to other substrates and packages. Section 2.3 discusses issues with spiral inductor and transformer modeling on silicon substrates, packages, and organic substrates. Section 2.4 discusses some of the advances in integrating magnetics with inductors. Integrating magnetics on board is cheaper compared to silicon and this could potentially be useful in the long term to boost inductance values and magnetic
coupling. Section 2.5 provides an overview of some of the advances in Level 3 and Level 2 interconnection technologies. Section 2.5 also reviews advances in realizing fine trace and via feature sizes on printed circuit boards and packages. This is important to be able to realize fine pitch inductive connectors or sockets in the future. The section concludes with a brief discussion of advances in integrating resistors on packages and printed circuit boards. Inductive interconnections require series resistance for low frequency impedance matching and the ability to integrate resistors with low parasitics is useful. Section 2.6 discusses some of the signaling standards and specifications in the context of board to board high speed serial links.

2.2 AC Coupling

The basic idea of AC Coupling is that capacitive or inductive elements can be used to block DC voltage and transmit AC information in a signal. Coupling capacitors are commonly used in analog circuit design applications to isolate the dc biases between subsequent stages and to provide frequency compensation in opamps [57, 66]. Gabara et.al used an on-chip coupling capacitor directly underneath the bondpad to block the DC levels of input signals [57]. Capacitively coupled signals suffer from the zero wander effect which causes the dc level of the output signal to be dependent on the input data transitions. They used a quantized feedback technique to reestablish local DC level at receiver hence enabling error free transmission for a $2^{31}-1$ pseudorandom data sequence at 800 Mbps. On-chip inductive coupling has found application in RF circuits such as LNAs, Baluns and Mixers [71, 72, 73].
The idea of AC coupling can be used to transmit information across an interface with no direct physical connection. This idea can be exploited in on chip and off chip communication applications. This is of specific interest in the context of this work and sections 2.1.1 and 2.1.2 below discuss applications of AC coupling in communication across different interfaces.

2.2.1 AC Coupling - Capacitive Coupling

Salzman et.al proposed using capacitive coupling instead of conductive junctions in flipped chip MCM designs [31]. Here signaling is done with pulses instead of square waves. Hayden [62] showed through simulations that pulse signaling could enable high speed and noise tolerant communications. A buried solder bump structure was proposed for AC coupling by Mick et.al and this is shown in Figure 2.1 [3]. Mick et.al demonstrated chip to chip capacitive coupling at a 4 Gbps NRZ signaling data rate in this work. The main idea behind the ACI scheme proposed in this work is that the DC component of a digital signal carries no information and that non-contacting AC connections can be built a lot denser and simpler than DC connections. Buried solder bumps provide the DC path while the coupling capacitors provide the AC path from chip to substrate.
Kuhn et.al use capacitive coupling for vertical digital signal transmission between adjacent chip layers in a 3D IC application [30]. Measured results show operation at 15 MHz and 25 MHz using 20 µm by 20 µm capacitor plates with a coupling capacitance of 5 fF in a 0.5 µm, 3.3 Volt technology. Kanda et.al demonstrate a wireless super connect with a similar physical structure [67]. They report a data rate of 1.27 Gbps/pin with a power consumption of 3 mW/pin using 20 µm by 20 µm coupling capacitors.

Drost et.al applied capacitive coupling in proximity communications [20]. Proximity communication is based on exploiting the fact that faster low cost communication is possible over shorter distances. The main difference between the physical structure in comparison to 3D IC’s is that here the chips are overlapped only partially, which in turn provides access to rest of the chip’s surface area for dc connections and area ball bonded I/O. They use built-in vernier position measuring circuits on their chips for accurate alignment. IBM’s Collective Intelligent Brick systems use circular connectors which act as capacitive elements to enable
communication between bricks without the need for cumbersome cable links [63]. Lei Luo demonstrates potential for passive equalization with coupling capacitors in chip to chip communication [102].

2.2.2 AC Coupling - Inductive Coupling

Inductive coupling has also been used for communicating between ICs in various low frequency applications. Bouvier et.al used inductive coupling to communicate between a smart card and its receiver using an inductive element with a footprint of less than 4 mm\(^2\) [74]. Recently Mizoguchi et.al demonstrated a wireless super connect based on Inductive coupling at GHz frequencies [14]. Here inductive coupling is used to communicate between two chips stacked face up through a distance of 300 µm at a data rate of 1.2 Gbps/pin. The inductor footprint in this work is 100 µm by 100 µm. In addition, inductive coupling has also been used for signal transmission in low frequency biomedical applications [87]. Jian Xu et.al demonstrates 2.8 Gbps data rates with inductively coupled structures in 3D IC applications [97].

2.3 Integrated passive components – Spiral Inductors and Transformers

2.3.1 Inductors on silicon

Planar spiral inductors are widely used in RF circuit communication blocks such as LNAs, Mixers and VCOs. Square spirals are commonly used due to their ease of layout. Silicon
substrate is often preferred for a wide variety of RFIC designs at lower GHz frequencies due to its lower cost compared to GaAs ICs and also because of ease of integration with baseband circuits. Inductance extraction of spiral inductors is a fairly difficult task. Some of the primary obstacles in obtaining accurate results with commercial tools include the 1:1 aspect ratio of the width to thickness of the wires that necessitates the proper modeling of field distribution inside the conductor volume, substrate loss in silicon, high frequency phenomena such as eddy current in the interconnect and the complexity of the shielding metal plate used to screen the spirals from the semiconductor substrate. Some of the early work on modeling on chip spiral inductors was based on numerical techniques, curve fitting and empirical equations. The shortcomings with these approaches are that they are process dependent and also not scalable with physical dimensions. Figure 2.2 shows a simple model for on chip spiral inductors proposed by Yue et.al [61, 77]. Here $L_s$, $R_s$ denote the series inductance and resistance of the coil respectively. $C_s$ is the capacitance between the coil winding layer and its underpass layer. $C_{ox}$ is the oxide capacitance between the spiral coil and the silicon substrate. $R_{si}$ and $C_{si}$ are used to model the substrate. The model is fairly simple as it models skin effect only to a first order and also ignores distributed effects at high frequencies. However in on chip applications where metal thickness lies between 1 µm to 2 µm, skin effect can typically be ignored at lower GHz frequencies.
Figure 2.2: Model for a spiral inductor on silicon substrate [61, 77]

This model is similar conceptually to models proposed by other authors [17, 76, 78] with variations primarily in choice of model elements used to capture substrate effects. For example other researchers have used variations of the model shown in Figure 2.2 without the element $C_{si}$.

Niknejad et.al reported a method to extract parameter values for the inductor model from measured data [17]. They used Y-parameters to extract various elements in the pi-model for an inductor. They cautioned however that the value of inductance computed using this technique includes the effect of capacitive coupling. They also commented that the extraction technique reported in [61] was probably better at addressing this problem. The approach outlined in [61] consists of the following sequence of steps – de-embedding the pad parasitics from the measured S-parameters, S matrix to Transmission Matrix conversion; determine propagation constant and characteristic impedance and finally determining model parameters.
from propagation constant and characteristic impedance. The pad parasitics are deembedded by subtracting the Y-parameters of the open circuit pad structure from the Y-parameters of the spiral coil. This technique is fairly common and is used in [17, 61, 76]. Niknejad et.al noted however that this de-embedding technique could introduce errors because of parasitic coupling between the spiral coil and the pads. They recommended placing the pads reasonably far apart from the device under test [17].

Niknejad et.al also developed a tool called ASITIC which enables efficient computer aided design and optimization for a wide variety of spiral inductors, transformers on silicon. ASITIC can be used to generate narrowband models for spiral inductors fairly quickly which eases the design process. Niknejad et.al also suggested using polygonal spirals instead of square spirals to reduce loss and improve Q-factor. The main argument in favor of polygonal spirals is that they have a higher Q in a given area compared to their square spiral counterparts. Hexagonal and octagonal spirals are quite commonly used by various other researchers. However square spirals yield the highest inductance in a given area compared to other alternatives.

Mohan et.al report the development of simple analytical expressions to compute DC inductance of square, hexagonal, octagonal and circular spiral inductors [64]. While several authors have reported lumped models based on fitting to measured data accurate analytical equations which predict inductance values accurately to within 3 to 5% error have been lacking and Mohan et.al address these issues [64].
The properties of the silicon substrate have a great impact on setting performance limits on inductors built in these processes. Several authors have studied the tradeoffs involved and suggested techniques to improve performance of inductors on silicon. Yue et.al studied the effect of ground shields on the performance of the inductors and demonstrated the improvements that can be gained by using a Patterned Ground shield [8]. The effect of the Patterned Ground shield proposed in [8] is to eliminate image currents in the substrate which contribute to inductance reduction of the spiral coil. Park et.al studied the dependence of substrate resistivity on inductor Q-factor [79]. As substrate resistivity increases the substrate resistance increases and the conducting losses in the substrate reduces. As a result the inductor Q-factor increases with increasing substrate resistivity. However, high values of substrate resistivity are not convenient to realize in fabrication facilities.

Long et.al showed that metallization losses dominated inductor Q at low frequencies and that this can addressed by using thicker metal layers. They report an increase in Q-factor from 5 to 10 when aluminum metal thickness changes from 1 µm to 3 µm [27]. Burghartz et.al illustrated improvements in inductor Q-factor by reducing inductor resistance by shunting several metal layers through via arrays [80].

Liu et.al demonstrated a toroidal inductor as a means of obtaining better flux linkage compared to spiral inductors in MMIC applications. This was fabricated through micro-machining techniques on low resistivity silicon [37].
2.3.2 Inductors in packages and organic substrates

Liu et al. investigated the dependence of inductance on geometric factors for inductors fabricated on FR4 [81]. Inductors fabricated on Printed wiring board (PWB) have higher tolerances and lower cost compared to inductors fabricated on chip. Liu et al. also developed a normalizing procedure to relate inductance, inductance tolerance and inductor geometry to fabrication process precision. Dalmia et al. report high Q inductors at GHz frequencies in a low temperature organic laminate build up process [82]. This paper discusses some of the tradeoffs in choice of return path and line width/space for inductor design. Dalmia et al. discussed implementation of high Q inductors in MCM-L technology. It reports a maximum Q of 99 by using cascaded loop inductors for an 11 nH inductor at 2.2 GHz with a resonant frequency of 3.6 GHz. Typically most high Q package inductors use LTCC technology which has advantages in terms of loss characteristics. But LTCC technology is rather expensive. Feasibility of using PWB as a base substrate for building high Q inductors has been established using a low cost process technology [69, 81, 82]. Dalmia et al. also discussed a method for modeling inductors using multi-line parameters. The multi-line method uses a distributed model for the coupled line segments. Arnold et al. reported characterization of thin film integrated spiral inductors in an MCM-D silicon substrate technology [83]. Horng et al. reported a modified T-model for modeling embedded inductors in LTCC technology over a large bandwidth [19].
2.3.3 Transformer modeling

Transformers are harder to model than spiral inductors using CAD tools since it has more metallization layers and complex 3D geometry. There are different types of integrated transformers with associated models. Stacked transformers are most relevant in the context of AC Coupling. Mohan et.al presented a lumped circuit model for on chip transformers with analytical design equations to determine the values of the model parameters [5]. Verma et.al derived an ABCD network model from Mohan’s lumped model and also broke down the parameter extraction problem separately with model approximations at low frequency and high frequency [4]. In a transformer the Magnetic coupling between the spiral inductors is modeled by using a coupling coefficient term (K) and capacitive coupling between the spiral inductors is modeled using a crossover capacitance term (C_c). A basic transformer model based on [4, 5] is conceptually similar to the one shown in Figure 2.3.

Figure 2.3: Coupled inductor model
Zhou et.al use monolithic transformers which provide better performance than inductors in a fully differential LNA circuit [71]. Here the on chip transformers serve the purpose of input/output tuning and no off chip components are needed. Wong et.al exploit the inherent crossover capacitance in an on chip transformer to build an integrated capacitive coupled transformer [12]. This is useful in RF circuits where low voltage supply is required. This structure also has a wide bandwidth due to its distributed nature which gives flexibility in modifying the operation frequency of the device without making any changes to the transformer geometry. Razavi et.al discuss modeling and optimization issues for stacked transformers in CMOS technology [13]. They discuss limits on achievable voltage gain placed by crossover capacitance and layout techniques to reduce crossover capacitance. The performance of a transformer is also sensitive to the winding phase. Mick discusses some of the tradeoffs involved in choice of winding phase through simulation studies [38].
2.4 Magnetic films in integrated inductors and transformers

V. Koreniviski concluded in his paper [49] that an efficient magnetic film inductor with appreciable inductance boost is yet to be developed for GHz applications. However he suggested that a magnetically sandwiched strip inductor holds promise in the future for GHz applications. Ahn proposed integrating magnetic core materials to build toroidal inductor structures using post-processing techniques on CMOS [28]. This achieves inductance boost at lower MHz frequencies. Kuribara et.al developed an equivalent circuit model for a RF integrated magnetic film inductor which is shown in Figure 2.4 [33]. The relationship between permeability of the magnetic material and inductance of the coil is analyzed in this work. $L_m$ and $R_m$ are the inductance and resistance contributions arising from the magnetic film. $L_s$ and $R_s$ are inductance and resistance of the spiral coil. $R_1$, $C_{21}$, $R_2$, $C_{22}$ are the parasitics at the inner and outer ports of the spiral coil. $C_{m1}$ and $C_{m2}$ account for the capacitance between the magnetic film and the coil and between magnetic film and the ground plane.

![Figure 2.4: Equivalent circuit for a magnetic film inductor ([33])](image)
2.5 Level 2 and Level 3 Interconnections

2.5.1 Level 2 Interconnections

Level 2 interconnections represent connections between an IC package and a printed circuit board. IC sockets represent Level 2 interconnections. Some major categories of sockets include single in-line package sockets, dual in-line package sockets, zigzag in-line package sockets, pin grid array sockets, ball grid array sockets, land grid array sockets and spring sockets. Figure 2.5 below shows some typical categories of Level 2 interconnections.

![Image of DIP, PGA, BGA package sockets](Source: [84], [85], [104] Intel)

Figure 2.5: DIP, PGA, BGA package sockets (Source: [84], [85], [104] Intel)

Early in the evolution stage of microprocessor packaging, I/O connections were peripheral and hence DIP (dual in-line) and SIP (single in-line) type sockets were typically used. Later as area array packaging was found to be more attractive in achieving denser I/O connections PGA and BGA sockets were used. Later LGA sockets were found to be more attractive particularly for mid and high end systems. LGA sockets offer comparable or higher density to BGA and PGA sockets with the added benefits of simplicity in rework in the event of manufacturing defects. For example, LGA designs with 1mm contact pitch can achieve 1681
connections within a 42.5 mm² module while PGA designs which typically employ 2.5 mm contact pitch can achieve only 289 connections within same area [93, 94]. Typical numbers for pitch in LGA socket designs range from 1 mm to 1.27 mm. In LGA technologies interconnection between the module side and the printed circuit board is provided through a conductive interposer. Available interposer technologies include compressible conductive spring designs, metal-elastomer composites and many others. A widely used LGA contact technology which is of direct interest to us is the fuzz button [93]. This design is a small column of kinked molybdenum wire contained in a cylindrical shaped housing. This column of wire can be compressed elastically over large axial displacements and the force encountered is well controlled. Such an interface could help in defining a small vertical distance between the mating boards which in turn would make it possible to integrate inductive elements for contactless connections.
2.5.2 Level 3 Interconnections

Based on an article in Electronic News in April 2000 [22], board to board connectors represent nearly 74% of all the demand for high speed connectors and were predicted to accelerate at a rate of 18.5 CGR (compound growth rate) and reach 2.4 billion dollars by the year 2004. There are two classes of board to board connectors –

1) Backplane to daughter card connectors which are used to provide high density right angle interfaces with printed circuit boards.

2) Mezzanine connectors which are high density connectors for parallel connection of printed circuit boards. Mezzanine connectors help to relocate high pin count devices onto mezzanine or module cards to simplify routing on the motherboard.

![Figure 2.6: Level 3 interconnections (Source: [9])](image)
Mechanically mated connectors are subject to wear and tear in the long run primarily due to the insertion force per contact (1 to 1.5 oz/contact being the current standard [23]) and this could limit scalability to higher pin counts. Also traditional mechanically mated connectors (for example Pressfit Backplane connectors) require a plated through hole via field which could disrupt the return path hence increasing loop inductance and crosstalk. Plated through hole (PTH) vias also have higher capacitive parasitics compared to microvias and create unused stubs in high density board layouts which could lead to reflections at higher frequencies. However certain connector technologies are emerging in the market – for example, surface mount/fit and compression mount/fit that show performance enhancement in lab environments [2]. A connector using surface mount termination makes contact to a pad on the surface of the PCB. Blind microvia arrays can be used for escape routing for signal pins on the PCB. This leads to improved signal integrity due to lower parasitics associated with blind microvias and elimination of stubs. The tradeoff is higher cost for these via technologies. Some concerns against surface mount connector technologies include mechanical durability and suitable mass assembly techniques. The biggest impediment to successful commercial deployment of these technologies is regarding the ability of the surface mount solder joint to withstand large mechanical stresses common in a backplane environment. As of today, the commercial deployment of surface mount connector technologies is sparse and happens only when performance advantages clearly outweigh cost and risk concerns. Research thrust/progress in this direction towards obtaining better mechanical durability is potentially the biggest threat to inductive surface mount connector technology from a competitive perspective. There is also a growing need for connectors with
lower profile in board stacking applications and it is of great importance in fine pitch
connectors used in portable devices as well [24]. J.S Corbin et.al also suggest LGA
technology as an application for board to board connectors [93]. The low profile that can be
achieved with LGA helps with minimal offset between the mating boards. Table 2.1 below
summarizes density, speed, % crosstalk and signaling mode for some of the popular
backplane connectors used today in the industry.

**Table 2.1: Density, Gbps per pin, signaling mode and % crosstalk for some popular
connectors**

<table>
<thead>
<tr>
<th>Connector Make</th>
<th>Signaling Mode</th>
<th>Data Rate (Gb/sec)</th>
<th>% Crosstalk</th>
<th>Density</th>
<th>Insertion force per pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Teradyne’s VHDM-HSD 8 row</td>
<td>Differential</td>
<td>5</td>
<td>2%</td>
<td>38 differential pairs per linear inch</td>
<td>40 grams per signal</td>
</tr>
<tr>
<td>Teradyne’s VHDM 8 row</td>
<td>Single Ended</td>
<td>2.5</td>
<td>Less than 5%</td>
<td>101 signals per linear inch</td>
<td>40 grams per signal</td>
</tr>
<tr>
<td>Tyco - SpeedPac</td>
<td>Differential</td>
<td>2.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Molex’s GbX</td>
<td>Differential</td>
<td>6 to 10</td>
<td>Less than 5%</td>
<td>69 differential pairs per linear inch</td>
<td></td>
</tr>
</tbody>
</table>
Molex’s Gbx connector achieves 6 Gbps to 10 Gbps signaling speeds with a density of 69 differential pairs per linear inch. The Gbx connector is compatible with existing and future generations of 10 Gigabit XAUI and Infiniband systems.

2.5.3 Processing advances in Packages and Printed Circuit Boards

Line widths of 20~25 µm and microvias with landing pads as small as 80 µm are available in next generation organic chip packaging technologies [6]. These technologies help in integration of high density chips effectively in Level 1 packaging applications. The ability to realize these fine feature sizes means we can realize desired inductance values in smaller footprints by using minimum trace width and intern-turn spacing. Sockets are package to board interconnections. The limiting factor to achieving ultra high density footprints for an inductive socket technology could be the advances in mainstream board level technology. IC packaging carriers tend to advance faster with successive generations in processing capabilities compared to board level processing. For example the minimum trace width in substrate level processes is 18-25 µm while the minimum trace width even in high end PCB processes is still only 50 µm. Endicott Interconnect technologies and Sanmina SCI are leaders in advanced board level manufacturing. Their current mainstream capabilities include 2mil trace width/space and 6 mil via hole PTH with 10 mil landing pads [105]. Endicott interconnect technology is also investigating integration of a fine pitch redistribution layer on printed circuit boards for their high end products. However there is significant need for high density traces and there is a significant research thrust in this direction [106]. In the future we
can expect to see 25–50 µm trace widths and 50–75 µm microvias even on printed circuit boards [92, 107, 108]. Surface mount discrete resistors have high frequency parasitics and also occupy significant real estate on printed circuit boards. Integrated buried resistors are being developed to address these needs [89]. These resistors have minimal parasitics at high frequencies. Achievable gap spacing in package to board and board to board interconnections also depends on surface roughness of FR4. In [40] it is reported that surface roughness of FR4 ranges typically from 1 µm to 10 µm.

### 2.6 Board to Board Serial Links

Backplanes are typically used to connect boards including telecom switches, routers, digital cross connects and multiprocessor systems. Communication and computing systems share some common backplane requirements and typically communication is desired over 20 to 40 inches of backplane interconnect with two connectors. FR4 material is preferred for the backplane for nominal cost.

**Figure 2.7:** High level view of a board to board Serial Link
Table 2.2 below summarizes some of the commonly used electrical signaling standards in high speed board to board serial links [75, 109, 110, 111, 112].

<table>
<thead>
<tr>
<th>Specification</th>
<th>Data Rate per link</th>
<th>Application</th>
<th>Other Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express</td>
<td>2.5 Gb/sec</td>
<td>Networking</td>
<td></td>
</tr>
<tr>
<td>RapidIO</td>
<td>3.125 Gb/sec</td>
<td>DSP, Wireless</td>
<td></td>
</tr>
<tr>
<td>Infiniband</td>
<td>3.125 Gb/sec</td>
<td>Computer Clusters,</td>
<td>Blade Servers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data communication</td>
<td></td>
</tr>
<tr>
<td>XAUI</td>
<td>3.125 Gb/sec</td>
<td>Data communication</td>
<td></td>
</tr>
<tr>
<td>Star Fabric</td>
<td>2.5 Gb/sec</td>
<td>Embedded, test</td>
<td>equipment</td>
</tr>
<tr>
<td>Ethernet</td>
<td>10 Gb/sec</td>
<td>Networking</td>
<td></td>
</tr>
</tbody>
</table>

The performance requirements are different for backplane communication and backplane computing applications. Telecom applications typically need a BER of 10e-15 while Ethernet typically needs a BER of 10e-12. These in turn place varying constraints on the backplane link.
3 Inductively Coupled Connectors – Theory, Design Tradeoffs and Analysis

3.1 Overview

Inductively coupled interfaces can be used in both level 3 interconnections (board-board connectors) and level 2 interconnections (package-board interconnections). Figure 3.1 shows the channel for an inductively coupled backplane connector system and Figure 3.2 shows the channel for an inductively coupled socket system. In the long-term such a structure can potentially be implemented by using low profile land grid array (LGA) style interconnections. Insertion force and mechanical stress is a problem in high pin count interconnections and this can be addressed by using contactless inductively coupled elements for high speed signal connections while using fuzz buttons [86] for power, ground connections and to provide a rigid mechanical interface.
Figure 3.1: Backplane connector system with inductive connectors (board to board interconnections)

Figure 3.2: Socket system with inductive interconnections (Package to Board interconnections)

PTH via stubs are assumed at the input and output interface of the socket and connector systems in Figure 3.1 and Figure 3.2. Stubs are not included at the inductive interface since a
surface mount inductive connector or socket would remove the need for PTH vias. To design inductive connectors or sockets we must be able to model them reliably and optimize/design based on the application. The following sections discuss transformer design, modeling and tradeoffs in context of the socket and backplane connector application.

### 3.2 NRZ or Pulse signaling

An ideal transformer is a high pass filter and the value of inductance sets the 3 dB high pass coupling frequency for the filter. Shrivastava et.al [18] established performance metrics for package level interconnects. For X Gbps non return to zero (NRZ) signaling they recommend $S_{21}$ values better than – 4 dB upto X GHz for the value segment products. They recommend $S_{11}$ values better than -10 dB upto 0.7*X GHz and values better than -6 dB between 0.7*X to X GHz. A transformer realized with large inductances can be used to meet these specifications and accomplish NRZ signaling. Figure 3.3 shows frequency response for a transformer realized with 50 nH inductances. The 3 dB high pass coupling frequency for this transformer in a 50 ohm system is $25 / 2 * \pi * L = 79.6$ MHz. As long as the input data stream is band-limited so that the lowest frequency content is ~80 MHz this can be used for transferring NRZ data with reasonable fidelity.
However it is hard to realize ~50 nH inductances in small footprints with available feature sizes in package and board processes. For example the maximum inductance realizable in a process with 25 µm trace width/space and 75 µm microvias in a 775 µm outer diameter is 22 nH. Trace width/spacing of ~15 µm would be required to achieve 50 nH inductance in a coil with 775 µm outer diameter. Realizing 50 nH inductance values in a package or board level process will also lead to long electrical lengths leading to distributed behavior. This would introduce issues both from a signal integrity perspective as well as increased complexity in modeling. For high fidelity NRZ signal transfer the value of inductance in practice would need to be much larger than even 50 nH to prevent droop in DC levels. For example Figure 3.4 shows output of a transformer system with 50 nH and 500 nH inductances in response to an input step.

**Figure 3.3:** Frequency response for an ideal transformer with 50 nH inductances
Figure 3.4: Step response for ideal transformers with 50 nH and 500 nH inductances

A transformer realized with 500 nH inductances would have its 3 dB high pass coupling frequency 10 times lower compared to a transformer realized with 50 nH inductances. This in turn implies that the transformer with 500 nH inductances has lower attenuation in its frequency response at low frequencies close to DC compared to the transformer with 50nH inductances. This leads to a more faithful reproduction of the NRZ signal with less droop in DC levels.

Pulse signaling offers advantages in terms of potential for higher speed and lower power. In pulse signaling only information in the edge is transmitted. Transformers can be used in theory for non return to zero (NRZ) or pulse signaling. Step response is illustrated for the two cases in Figure 3.5. The input signal in our system is broadband digital NRZ data; output waveform from the transformer can be faithfully reproduced NRZ or pulses depending on the value of inductances. An ideal transformer is a high pass filter and the value of inductance sets the 3 dB high pass coupling frequency for the filter. NRZ signaling with a transformer in
a 50 ohm system needs fairly large values of inductances to be able to couple data across a wide band of frequencies from close to DC to the knee frequency corresponding to the digital edge.

**Figure 3.5:** NRZ and pulse signaling across a transformer

**Figure 3.6:** Frequency response for an ideal transformer with 5 nH inductances
More realistic option for sub-mm pitch inductive connector system is pulse signaling. All the information in a digital signal is in the high frequency content of the edge. This information can be used to detect a 1 to 0 and 0 to 1 transition. A transformer realized with small inductance values ranging from 1 nH~5 nH can be used to read high frequency information in the edge while attenuating low frequency components. This can be used to convert input step to pulses as shown in Figure 3.5. Filtering of low frequency components leads to the pulse waveform in this case. These pulse waveforms can then be recovered back to NRZ through circuit techniques [41, 97].

Figure 3.6 shows frequency response for an ideal transformer realized with 5nH inductors. An ideal transformer realized with 5 nH inductances has a 3 dB high pass coupling frequency at 1 GHz and impedance matching is only possible from this frequency upwards. In pulse signaling, the performance of the interconnect needs to be evaluated as a function of edge rate. The rise time of the edge determines the highest frequency content of the input data. Various references suggest methods for estimating knee frequency using approximations such as $0.5/t_r$. Figure 3.7 shows the voltage spectra FFT obtained from Hspice for a simple NRZ waveform with 50 ps rise and fall times. In digital applications the highest frequency we care about is the knee frequency ($0.5/t_r$) which is 10 GHz in this case. In analog applications signals of smaller amplitude levels with up to -30 dB attenuation are often useful. Hence higher order harmonics have to be analyzed as well.
Figure 3.7: FFT Analysis plot for a NRZ waveform with 50 ps edge rate

The frequency response of an inductive system for pulse signaling needs to be optimized up to the knee frequency corresponding to the digital edge (i.e. 10 GHz in this case).
3.3 Transformer modeling and optimization for pulse signaling

3.3.1 Transformer modeling

There is a large volume of body in the literature relating to transformer modeling. High fidelity models are important to predict performance before building them. The elements in the model depend on the geometry of the inductor coils, the substrate they are realized on and return paths. Figure 3.8 shows the baseline transformer lumped model for analysis in this work.

![Coupled inductor model](image)

(a) In-phase wound  (b) Out of phase wound

**Figure 3.8:** Coupled inductor model (in phase and out of phase)

Here L represents the inductance of the primary and secondary coils assuming they are equal. K represents the magnetic coupling coefficient between the coils. $C_c$ is the crossover
capacitance arising due to the overlap area of the two coils. \(C_p\) is the parasitic capacitance to ground for the coils. \(R\) is the winding resistance for the coils. This work focuses on inductors realized on laminate and packaging substrates as opposed to conductive silicon. Hence some of the complexity associated with modeling parasitics associated with a conductive substrate is eliminated leading to a simplified model in Figure 3.8. The model can be expanded to distributed structures by cascading multiple sections of the lumped model. EM tools like Sonnet or HFSS can be used for modeling distributed structures. The choice of whether to use a lumped model or a distributed model must be made based on the electrical length of the structure. For example the edge rate in typical high speed digital applications is ~70 ps. This sets the knee frequency at 7 GHz. If the electrical length of a structure is less than or equal to one tenth of operating wavelength at 7 GHz then a lumped model would suffice, else distributed or EM modeling is needed. The model in Figure 3.8 ignores skin effect. Skin effect should be modeled for thicker metallization while it can be ignored for thinner metallization. A ladder network similar to the one proposed in [11] can be used to include skin effect.

The value of inductance and magnetic coupling coefficient corresponding to the coupled inductor model can be determined with reasonable accuracy with tools such as ASITIC and OEA. The accuracy of these tools was validated by comparing predicted value of \(L\) and \(K\) from ASITIC/OEA with values obtained from model fits with measured data. Benchmark on chip transformers designed by Stephen Mick on silicon wafers in a TSMC 0.25 µm and a TSMC 0.35 µm process was available for this exercise. Figure 3.9 shows the die photo of one
of the benchmark structures. Table 3.1 shows the comparison of extracted L and K from ASITIC with extracted values from model fits to measured data for the structure shown in Figure 3.9

![Die photo for benchmark on chip transformer](image)

**Figure 3.9:** Die photo for benchmark on chip transformer

This structure was fabricated in a TSMC 0.25 µm, five metal layer process. A patterned polysilicon ground shield (PGS) was placed between the bottom spiral inductor and the substrate to reduce eddy currents and eliminate difficulties associated with modeling the substrate. The structure has 50 µm external diameter; nine turns on primary and secondary, 1.2 µm Metal width and 1.2 µm spacing between the turns.

**Table 3.1: Comparison of extracted L and K from ASITIC and circuit model fits to measured data**

<table>
<thead>
<tr>
<th>Benchmark Structure</th>
<th>K (from circuit model fit with measured data)</th>
<th>K (from ASITIC)</th>
<th>L (from circuit model fit with measured data)</th>
<th>L (from ASITIC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 µm diameter transformer</td>
<td>0.5</td>
<td>0.55</td>
<td>2.8 nH</td>
<td>2.4 nH</td>
</tr>
</tbody>
</table>
The inductance value in ASITIC is marginally smaller than the value extracted from model fits to measured data on account of the patterned polysilicon ground shield. ASITIC simulations do not include the effect of the patterned poly-silicon ground shield (PGS). In the absence of the PGS image currents flowing through the silicon substrate can lead to reduction in inductance values.

### 3.3.2 Optimizing transformer model parameters for Pulse signaling

#### 3.3.2.1 Inductance Values

Figure 3.10 shows the step response of three different parasitic free coupled inductors with a coupling coefficient of 0.9. The settling times for equal value coupled inductors with inductance values of 5 nH, 15 nH, and 25 nH, are 900 ps, 2.2 ns, and 4 ns, respectively when the load impedance is 50 ohms. An inductor has an associated decay time, which sets a limit on the signaling data rate. For example a transformer realized with 5 nH inductors has a step response which settles to 10% of its peak amplitude in 900 ps if no equalization is used in the system to filter the tail. A signal to noise ratio of 10 (i.e. 20 dB) is a typically acceptable number for digital applications. This sets the maximum data rate achievable for this system at 1/900 ps = 1.1 Gbps. Since we are interested in Gbps pulse signaling this sets the upper limit on the value of inductance in our application.
The settling time of the step response for the inductive elements can be reduced by using high impedance terminations on the secondary inductor coil. High impedance terminations on the secondary coil increases the 3 dB high pass coupling frequency which filters low frequency components further and increases the 3 dB bandwidth as well. This in turn leads to faster settling times and enables signaling at faster data rates. Figure 3.11 shows the step response of three different parasitic free coupled inductors with a coupling coefficient of 0.9 when the system reference impedance is 500 ohms. The settling times for equal value coupled inductors with inductance values of 5 nH, 15 nH, and 25 nH, are 600 ps, 1.4 ns, and 2 ns, respectively when the load impedance is 500 ohms. The amplitude of the received signal is also higher when the load impedance is 500 ohms.
Figure 3.11: Step response of 3 different parasitic free coupled inductors with a coupling coefficient of 0.9

However the output of inductive connectors or sockets is typically loaded by a 50 ohm transmission line on package or FR4. The choice of 50 ohms characteristic impedance for the traces is driven by routing density and optimum performance characteristics on FR4/package. Hence it is hard to impact system performance beneficially by varying load terminations. If differential signaling were employed in the connector with two identical 50 ohm lines the differential impedance looking in is 100 ohms. The decay rate for the coupled inductors would be faster for coupled inductors in a 100 ohm system compared to a 50 ohm system. This could have some application in achieving faster speeds with differential connectors as opposed to single ended connectors.

The lower limit on the value of inductance is set by the signal swing required in the end application for the connector or socket structure when it is plugged in a real system. For a given area, trace width, and inter-turn spacing, the magnetic coupling increases with
inductance. Hence it is hard to achieve good magnetic coupling when the inductance values are extremely low.

### 3.3.2.2 Choice of Inductor Shape:

Though there are various alternatives available for inductor shape design a square shape is the most appropriate for our application. Our goal is to achieve as small a pitch as possible with available trace width and space to realize 1 ~ 5 nH inductances. It is hard to realize sufficient inductance values in small footprints. In a given area a square inductor has the highest inductance compared to other alternatives like hexagonal or octagonal inductors. In on chip RF applications hexagonal or octagonal inductor shapes are used as opposed to simple square shapes since they have a better Q factor due to smaller winding resistance. However in package and laminate processes the minimum trace width is 1~2 mils, which in turn contributes towards much smaller winding resistance compared to chip processes. Also in our application some winding resistance could actually be beneficial for tuning the return loss and achieving broader bandwidth. Table 3.2 shows comparison of inductance, DC resistance and magnetic coupling coefficient for square, hexagonal and octagonal shapes. Magnetic coupling coefficient is extracted by simulating vertically stacked square, hexagonal and octagonal inductors. A 500 µm diameter transformer with 25 µm trace width/space and 3 turns is chosen as the test case. Simulations were performed using ASITIC. 5 µm gap spacing is assumed between the vertically stacked 500 µm diameter inductors for extracting coupling coefficient (K). The difference between K for the 3 cases is marginal.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Square Inductors</th>
<th>Hexagonal Inductors</th>
<th>Octagonal Inductors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>5.13 nH</td>
<td>4.31 nH</td>
<td>4.32 nH</td>
</tr>
<tr>
<td>DC Resistance</td>
<td>4.475 ohms</td>
<td>3.76 ohms</td>
<td>3.68 ohms</td>
</tr>
<tr>
<td>K (with gap spacing of 5 µm)</td>
<td>0.921</td>
<td>0.922</td>
<td>0.922</td>
</tr>
</tbody>
</table>

Another alternative to boost inductance values in small footprints is to use multiple winding layer structures to build the primary and secondary inductors constituting the transformer. Figure 3.12 shows two dual layer inductors coupling across a gap spacing d. In most package and laminate processes the inter-layer spacing between the winding layers forming the dual layer inductor is of the order of 5~10 mils. The gap spacing (d) between the two physical interfaces is typically around 1~2 mils.
This implies that in Figure 3.12 inductors $L_1$ and $L_3$ are tightly coupled magnetically while inductors $L_2$ and $L_4$ are weakly coupled. The weakly coupled inductors which are generally comparable in inductance values to the tightly coupled inductors act as leakage inductances in the transformer electrically. This leads to high frequency roll off in the forward transfer function and impedance mismatches as discussed in section 3.3.2.3. Hence dual layer inductors are not a viable alternative to obtain performance benefits unless the inter-layer spacing for the dual layer coil is comparable or much less than the gap spacing (d). Other alternative geometries include center-tapped symmetric structures [72] for differential signaling. However realizing this structure needs significant number of via transitions. The size of microvias in package processes ranges between 2 to 3 mils. This significantly limits realization of high density inductor footprints to achieve sufficient inductance values over a
range of operating frequencies. Based on these discussions a simple single layer square inductor is a good choice for this application.

3.3.2.3 Magnetic coupling coefficient (K)

High magnetic coupling coefficient values are desirable in inductively coupled connectors for improving insertion loss and return loss, and increasing bandwidth. Figure 3.13 shows the T circuit model for a transformer with $K < 1$. As the $K$ reduces the value of the leakage inductances in the model $L_1 - M$ & $L_2 - M$ grow which in turn contribute to high frequency roll off in forward transfer function, more loss and impedance mismatches, leading to reflections.
Figure 3.13: T-model for a transformer with leakage flux (M = K * SQRT(L₁ * L₂))

Figure 3.14 shows a simple transformer model assumed for the discussion in this section.

Figure 3.14: Transformer model to analyze variation of K
Figure 3.15 shows how $S_{21}$ changes as the leakage inductance increases when $K$ drops from 1 to 0.6.

![Graph showing $S_{21}$ for increasing leakage inductance (assuming $L_1 = L_2 = 5$ nH)](image)

**Figure 3.15:** $S_{21}$ for increasing leakage inductance (assuming $L_1 = L_2 = 5$ nH)

As $K$ drops the 3 dB bandwidth of the system reduces and the loss through the system also increases. For example when $K$ changes from 0.8 to 0.6 the 3 dB bandwidth of the system reduces from 8.9 GHz to 4.9 GHz. Figure 3.16 shows $S_{11}$ for increasing leakage inductance. Authors at Intel [18] established that atleast -10 dB of return loss is required for acceptable performance in package interconnects.
When $K = 1$ the $S_{11}$ is better than -10 dB from 2 GHz upwards. A deviation of $K$ to 0.8 or below degrades the return loss below -5 dB which is unacceptable. The magnetic coupling coefficient between two vertically stacked planar spiral inductors is a function of many factors, including gap spacing, inductance and effective area. In a level 2 or level 3 interconnect application using organic laminates, the achievable gap spacing between the coupling elements is limited by the surface roughness of FR4, and the thickness of the interlayer dielectric used to isolate the coupling elements. The surface roughness of FR4 can range from 1 µm to 10 µm [40], which produces a large and unpredictable variation in the gap spacing. Figure 3.17 shows $K$ vs gap spacing(d) extracted using ASITIC for a sample transformer structure. The transformer chosen is 500 µm in outer diameter with 25 µm trace
width/space and 3 turns. The extracted value of inductance is 5.13 nH. The metalization is 2 µm thick copper.

![Graph](image)

**Figure 3.17**: K vs Gap spacing(d) extracted using ASITIC for a 500 µm diameter transformer

The value of K is 0.91 when the gap spacing is 5 µm. The value of K is 0.5 when the gap spacing is 50 µm. An empirical design rule observed through iterative simulations in ASITIC is that the transformer outer diameter needs to be 10 times the gap spacing to achieve a K of 0.5. Depending on how the physical interface is realized in sockets or connectors the gap spacing can be as high as 25 µm. The value of K is 0.67 when gap spacing is 25 µm. Table 3.3 shows how K changes when the trace width changes for a certain transformer with all other factors remaining the same. As the trace width changes from 5 µm to 45 µm the K changes from 0.562 to 0.714. As the trace width increases the inductance actually reduces.
The increase in K is attributed to the increase in Mutual inductance(M) due to the increased effective surface area of the transformer which is the product of electrical length and trace width. For example in table 3.3, K increases from 0.562 to 0.714 when effective area of the inductor coils increase by a factor of 7.11 (with fixed gap spacing, outer diameter and inter-turn spacing).

Table 3.3: K extracted from ASITIC for varying trace widths

<table>
<thead>
<tr>
<th>500 µm Outer diameter transformer with 3 turns (Gap spacing = 25 µm)</th>
<th>K (Extracted from ASITIC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/S = 5 µm/25 µm</td>
<td>0.562</td>
</tr>
<tr>
<td>W/S = 15 µm/25 µm</td>
<td>0.638</td>
</tr>
<tr>
<td>W/S = 25 µm/25 µm</td>
<td>0.677</td>
</tr>
<tr>
<td>W/S = 35 µm/25 µm</td>
<td>0.700</td>
</tr>
<tr>
<td>W/S = 45 µm/25 µm</td>
<td>0.714</td>
</tr>
</tbody>
</table>

Process limitations also constrain choice of trace width, trace spacing and realizable inductance values in a given area. These process constraints limit the maximum value of the magnetic coupling coefficient between the inductors. For a given area, trace width(W), and inter-turn spacing(S), the magnetic coupling increases with inductance. Therefore, adding more turns, within the constraints of area, would provide a boost in K, which is one way to improve the bandwidth of the coupled inductors. Table 3.4 shows extracted K from ASITIC
when no. of turns increases for a transformer leading to increasing inductance with all other geometrical parameters remaining the same.

However, for high-speed applications, short decay times are required, which will affect the choice of inductance values for a particular design. The tradeoffs between desired signal amplitude, bandwidth and signaling speed have to be balanced carefully in the context of system level application requirements. This is explained in more detail in the case study chapter through a design example.

### Table 3.4: K extracted from ASITIC for increasing Inductance

<table>
<thead>
<tr>
<th>500 µm Outer diameter transformer (W = S = 25 µm)</th>
<th>K (Extracted from ASITIC)</th>
<th>Inductance (extracted from ASITIC)</th>
</tr>
</thead>
<tbody>
<tr>
<td># of turns = 1</td>
<td>0.58</td>
<td>1.37 nH</td>
</tr>
<tr>
<td># of turns = 2</td>
<td>0.65</td>
<td>3.38 nH</td>
</tr>
<tr>
<td># of turns = 3</td>
<td>0.67</td>
<td>5.13 nH</td>
</tr>
<tr>
<td># of turns = 4</td>
<td>0.68</td>
<td>6.2 nH</td>
</tr>
</tbody>
</table>
3.3.2.4 Parasitic capacitance

On packages and printed circuit boards the main contributor to shunt parasitic capacitance ($C_p$) is the proximity of the inductors to the ground planes. Figures 3.18(a) and 3.18(b) show representative transformer geometry and equivalent circuit model. Excessive shunt parasitic capacitance ($C_p$) can create issues by causing high frequency roll-off in the forward transfer function ($S_{21}$), cause ringing in the time domain response and introduce impedance matching issues.

![Transformer geometry – Inductor (L) coils and GND Planes](image)

**Figure 3.18(a):** Transformer geometry – Inductor (L) coils and GND Planes

![Equivalent circuit model](image)

**Figure 3.18(b):** Equivalent circuit model

**Figure 3.18:** Transformer Geometry and Circuit Model
Figure 3.19 shows $S_{21}$ curves when $C_p$ in the model shown in Figure 3.18(b) varies from 100 fF to 1 pF. As $C_p$ increases from 100 fF to 500 fF the 3 dB bandwidth of the system drops from 19 GHz to 6 GHz. This would limit operation at multi-Gbps speeds. Parasitic capacitance can be controlled through careful layout of the spiral inductor coils and their return paths. For example in test-structures fabricated in this research the spacing between the spiral inductor and its neighboring ground plane was $1/4^{th}$ of the outer diameter of the coil. The ground plane was on a layer below the inductor coil. For this configuration, capacitive parasitics extracted in circuit models was minimal (and usually <50 fF). This ground plane spacing rule was determined through a process of trial and error on test-structures built in iterative fabrication runs. When the spacing of the coil to the ground plane is much smaller than this...
the shunt parasitic capacitance to ground increases which in turn degrades high frequency impedance matching. When the spacing of the coil to the ground plane is too large the loop inductance of the return path increases which in turn increases the effective inductance of the coil to a value different from desired design. The ground plane was removed in the area directly underneath the spiral inductor to reduce eddy currents. This reduces parasitic capacitance as well since parallel plate capacitance between the spiral inductor coil and its ground plane is minimized.

3.3.2.5 Winding resistance

In most applications low loss is desired to maximize signal transfer through the transformer. Winding resistance of a spiral inductor can be minimized by widening the metal traces, increasing the thickness of the metallization used to build the inductor and minimizing the electrical length of the inductor. However while widening the traces decreases the winding resistance it also increases the crossover capacitance \((C_c)\) between the coils. This increased crossover capacitance can cause roll off in the forward transfer function \((S_{21})\) by resonating with the inductive element in the equivalent circuit model shown in Figure 3.18. This effect is along similar lines as the curves in Figure 3.19. This in turn degrades system performance. Also increased trace widths can increase shunt capacitive parasitics due to larger conductor area. These factors must be considered while optimizing the inductor geometry to minimize ohmic loss. In this work a combination of frequency domain and time domain EM simulations, extracted circuit models and simulations with spiral inductor simulation tools
such as ASITIC/OEA were used to determine optimal trace width/space to tradeoff between winding resistance and capacitive parasitics.

### 3.3.2.6 Winding Phase, Cross over capacitance and Series termination

In practice the value of magnetic coupling coefficient in a transformer is always less than 1. In on chip transformers where the inter-layer dielectric spacing is of the order of 2 µm the value of $K$ is typically $> 0.9$. However as gap spacing increases the value of $K$ drops and in our application it is closer to 0.7. Also in case of vertically stacked transformers there is always a crossover capacitance due to the overlap area of the coils. These non-ideal effects contribute to some differences in performance of the transformer depending on the winding sense. In the absence of crossover capacitance the performance of in-phase and out of phase wound transformers are identical. However the presence of the crossover capacitance introduces differences in the frequency response for the two cases. Stephen Mick in his dissertation discusses this from a pole-zero perspective. Here a simple intuitive explanation is presented to add to the understanding and these ideas are verified by measurements shown in chapter 4. A transformer can be represented by its T-equivalent circuit or pi-equivalent circuit. Figure 3.20 shows pi-equivalent circuits for a transformer with no shunt capacitive parasitics or winding resistance to study the impact of crossover capacitance on winding sense. The shunt capacitive terms and winding resistance terms are not required in the model to understand the impact of crossover capacitance on winding sense. We use a pi equivalent
circuit in this discussion as opposed to a T-circuit as it is easier to decompose a pi model into series-parallel combinations as opposed to a T-model.
In the pi model for in phase wound coils we have an inductance term in parallel with the crossover capacitance. This is a classical tank circuit. Larger values of crossover capacitance tend to shift the resonance point in the forward transfer function to lower frequencies. This in turn introduces impedance discontinuities and reduces the 3 dB bandwidth. In the pi Model for out of phase wound coils we have a negative inductance term in parallel with the crossover capacitance. A negative inductance is equivalent to a capacitor whose value changes with frequency. Hence the effective combination of $C_c$ and the negative inductance looks like two capacitors in parallel which in turn equates to a larger capacitance. This in turn shifts the resonance point to much higher frequencies since this is no longer a tank circuit. Figure 3.21 shows a simple lumped transformer model to see the difference between in phase and out of phase wound coils.
Figures 3.22, 3.23 show $S_{21}$ and $S_{11}$ curves for in-phase transformer with different values of magnetic coupling coefficient and crossover capacitance.

**Figure 3.21:** Lumped model for in phase vs out of phase Study

**Figure 3.22:** $S_{21}$ for in phase transformer with varying K and $C_c$
Crossover capacitance introduces pronounced notches in the frequency response for in phase wound coils while it can be used more beneficially for out of phase wound coils. Figures 3.24 and 3.25 show $S_{21}$ and $S_{11}$ curves for an out of phase transformer with different values of magnetic coupling coefficient and crossover capacitance. There is a significant roll-off at high frequencies when $K$ is 0.7 and this roll-off would be more pronounced for higher inductance values. Addition of crossover capacitance ($C_c$) value of 200 fF compensates for the high frequency roll-off in the frequency response in Figure 3.24. Since PCB & package trace widths are relatively larger compared to on chip features we can exploit the cross-over capacitance beneficially to obtain desired frequency response as the crossover capacitor acts as a high pass filter. An inductor has a rising impedance profile with frequency while a capacitor has a falling impedance profile with frequency.
Iterative simulations with simple lumped transformer models can be used to determine values of crossover capacitance which achieve best case values of $S_{21}$ and $S_{11}$. 

**Figure 3.24:** $S_{21}$ for out of phase transformer with different $K$ and $C_c$

**Figure 3.25:** $S_{11}$ for out of phase transformer with different $K$ and $C_c$
The impact of $C_c$ on performance can be analyzed independently of the winding resistance and shunt parasitic capacitance. Figure 3.26 shows a simplified transformer T-circuit model without winding resistance and shunt parasitic capacitance. This simplification is to help in deriving manageable closed form expressions for S parameters and transfer functions. The transformer model in figure 3.26 can be viewed as a parallel combination of the transformer T-circuit model and crossover capacitance assuming both these elements share a common ground return path. Equivalent ABCD network can be determined for this network and then converted to S parameters as in [19]. S parameter equations derived from first principles using ABCD chain parameter computations for transformer models are unwieldy. This makes it hard for the designer to gain an intuitive understanding of channel optimization. In this respect the voltage transfer function is more useful. Nevertheless S parameters are a valuable source of guidance early on in the design process to help the designer identify potential sources of discontinuity and problem spots in the frequency domain. Once this is accomplished it is more informative to look at transfer functions and step response. Figure
3.27 shows the input impedance plot obtained using Agilent Design System (ADS) as a function of $C_c$ with fixed values of $L_1$, $L_2$ and $K$ in the circuit model in Figure 3.26. When the value of $C_c$ is 10 fF impedance profile is rising (inductive) and this would lead to $S_{11}$ degradation. When the value of $C_c$ is 400 fF impedance ranges from 40 to 56 ohms over a narrower bandwidth of 2.2 GHz to 4.2 GHz. When the value of $C_c$ is 200 fF impedance ranges from 40 to 60 ohms between 3 GHz to 9 GHz and $S_{21}/ S_{11}$ can be optimized in this bandwidth. For this transformer, a nominal value for $C_c$ of 200 fF is a good choice.

For this transformer, a nominal value for $C_c$ of 200 fF is a good choice.

![Figure 3.27: Input impedance vs. frequency for model in Figure 8 ($L_1 = L_2 = 2$ nH; $K = 0.7$; $C_c$ varies from 10 fF to 400 fF)](image)

When the value of $C_c$ changes to 240 fF (a 20% variation over a nominal value of 200 fF), the input impedance shows variation of 1 to 9 ohms between 4.5 to 10 GHz. Process variations is another issue to be mindful of when designing inductive connectors for real world applications and impedance variations should be within +/-10%. Equation 1 shows the
voltage transfer function for a simplified transformer model without shunt parasitic capacitance and winding resistance shown in Figure 3.26. The term \((L_1 L_2-M^2)\) is proportional to leakage in the transformer system and the product of this term with \(C_c\) in the numerator of equation 1 impacts the zeros of the transfer function,

\[
s = \sqrt{\frac{M}{(L_1 L_2 - M^2) C_c}}.
\]

When the leakage inductance is very small, \(C_c\) has no impact upon the system zero but it still impacts the system poles. This implies that \(C_c\) has almost no effect on controlling reflection noise in the system. As the leakage inductance grows \(C_c\) has more control over reflection noise in the system.

\[
H_{21}(s) = \frac{((L_1 L_2 - M^2) C_c s^2 - M) R_L s}{A C_c s^3 + (L_1 L_2 - M^2 + B C_c) s^2 + (R_s L_2 + R_L L_1) s + R_s R_L}
\]

\[
A = (L_1 L_2 - M^2) (R_s + R_L); \quad B = (L_1 + L_2 + 2M) R_s R_L
\]

**Equation 1: Voltage transfer function to capture the effect of \(C_c\)**

(Source Resistance – \(R_s\), Load termination - \(R_L\))

From S parameter or Input impedance plots a range of useful values of \(C_c\) can be identified to tune the system response. However, a point to note is that excess crossover capacitance can negatively impact transformer step response due to overshoots and oscillations. Hence the value of crossover capacitance used to tune the frequency response should be as small as possible without introducing overshoots or oscillations in the step response. Pole zero plots
derived from the transfer function in equation 1 can also be used to determine values of $C_c$ which make system response underdamped or unstable which introduces overshoots or oscillations in the system transient response. The transfer function in equation 1 is a $3^{rd}$ order system and hence the system response can be more complex than a $2^{nd}$ order system depending on dominant poles and their relative proximity to each other as well. An over-damped system has no overshoots in its transient response. From this analysis an upper bound can be established on values of $C_c$ that can be used to tune the system.

The poles of the transfer function convey information about the nature of the response. When $C_c = 10$ fF the system poles are real and distinct as shown in Figure 3.28(a) and the system is over-damped. When $C_c = 200$ fF the system has real and complex conjugate poles as shown in Figure 3.28(b). In this case, system response depends on the dominant poles. The dominant poles are the ones located closer to the origin. Since the real pole is located closer to the origin in this case it is expected that this system will have an over-damped response. When $C_c = 400$ fF the system has real and complex conjugate poles but in this case the complex poles are located closer to the origin as shown in Figure 3.29. Hence it is expected that this system will have an underdamped response with one or two overshoots before settling to steady state value. This in turn reduces the signal to noise ratio of the system and introduces sources of error in the interconnect channel. From these pole zero plots the designer can ensure that the choice of values of $C_c$ used to tune input impedance or frequency responses don’t cause the system response to be underdamped.
(a): Pole zero plots obtained from equation 1 ($L_1 = L_2 = 2 \text{nH}; K = 0.7; C_c = 10 \text{fF}; 50 \text{ ohm system}$)

(b) Pole zero plots obtained from equation 1 ($L_1 = L_2 = 2 \text{nH}; K = 0.7; C_c = 200 \text{fF}; 50 \text{ ohm system}$)

**Figure 3.28:** Pole zero plots from equation 1
Figure 3.29: Pole zero plots obtained from equation 1 ($L_1 = L_2 = 2 \text{nH}$; $K = 0.7$; $C_c = 400 \text{fF}$; 50 ohm system)

Figure 3.30 shows step response derived from equation 1 in a 50 ohm system with $C_c$ varying from 100 fF to 400 fF.
Figure 3.30: Step response derived from equation 1 for a 70 ps edge: $L_1 = L_2 = 2 \text{nH}; K = 0.7; C\text{c varies from 100 fF to 400 fF}$

In Figure 3.30 the magnitude of the overshoot approaches $1/10^{th}$ of the signal swing when the crossover capacitance is 400 fF. This is the region where the system response is underdamped as observed in the pole zero plots. Optimizing crossover capacitance helps in high frequency impedance matching. Controlling the low frequency return loss needs lossy elements like a series resistance since electrically a transformer circuit is a short at DC. Figure 3.32 shows that broadband $S_{11} >= -10 \text{dB}$ for a baseline transformer circuit model shown in Figure 3.31 can be achieved through a combination of 25 $\Omega$ series termination and 200 fF series crossover capacitance. Operating at multi-Gbps speeds needs fast settling times for the inductors and based on table 1 the inductance value should be intermediate between 1 to 5 nH. Inductance values of 2 nH and magnetic coupling coefficient values of $K = 0.7$ are reasonable assumptions for an inductive connector system built in packaging interfaces to operate at Multi-Gbps speeds. The threshold on the acceptable value of $K$ varies on a case by case basis and is specific to the attenuation budget of the system (i.e. single connector system
or 2 connector system etc.) and the reflection noise tolerance of the system (i.e. the extent of
degradation introduced by series leakage inductance). An approximate rule of thumb is to
keep leakage inductance term in the transformer T-circuit model < 1 nH, the faster the edge
rate this requirement becomes more stringent. \( C_c \) value of 200 fF is nominal for impedance
matching in the 3 GHz to 9 GHz band and also the transient response is overdamped with
this choice of \( C_c \).

\[ \text{Figure 3.31: Transformer model (with series termination and } C_c) \]
Series termination optimization is an engineering tradeoff between signal amplitude attenuation and reflection noise control. Too low a value of series termination provides no benefits for impedance matching while too high a value attenuates the signal transmitted to unacceptable levels. Hence an intermediate value of $25 \ \Omega$ is used in this simulation. The transfer function in equation 1 can also be used to gain insights on series termination optimization by varying $R_s$ and $R_L$. While this is not a direct one to one analysis variation of these terminations can be used to draw analogies and make inferences on impact of series terminations on system response. For example the transfer function clearly reveals that the load termination has impact on system zeroes while the source termination only impacts the system poles as it shows up only in the denominator of the transfer function. This provides insights as to how to optimize series termination placement to control reflections in a backplane connector channel. The transformer (i.e. connector) sees an effective load impedance $R_{\text{load}}$ for the forward travelling wave and an effective load impedance given by
the combination of series termination, Transmission line and driver impedance for the backward travelling wave. Sometimes system constraints dictate the value of load impedance and it is useful to have more degrees of freedom in controlling reflections by adjusting source and load terminations for forward and backward travelling waves. Series termination and load termination act interchangeably as reflection control mechanisms depending on the direction of wave propagation. The transformer model parameters shown in Figure 3.31 can be realized in small electrical winding lengths and can thus be represented with a lumped model. The nominal transformer geometry that corresponds to \( L_1 = L_2 = 2 \text{ nH}, K = 0.7, \) and \( C_c = 200 \text{ fF} \) is shown in Table 3.5. The transformer geometry shown in table 3.5 can be realized in an aggressive laminate technology with 25 \( \mu \text{m} \) minimum trace width and 50 \( \mu \text{m} \) microvias [22, 23]. Here the gap spacing is assumed to be 25 \( \mu \text{m} \) and dielectric constant of the material in the gap is assumed to be 4.0. A gap spacing of 25 \( \mu \text{m} \) is a realistic estimate for spacing between two printed circuit boards with a surface roughness ranging from 1 \( \mu \text{m} \) to 5 \( \mu \text{m} \) with a thin coat of polyimide acting as a spacer. Based on empirical trends observed in ASITIC simulations, a transformer outer diameter at least 10 times the gap spacing is needed to achieve a \( K \) of 0.5 across this gap spacing. Polynomial curve fits obtained from ASITIC plots of \( K \) vs gap spacing can be used to understand relationship between these parameters for different transformer geometries. These relationships can be used by the designer as rules of thumb. Magnetic coupling is a complex function of several geometrical parameters and 3D EM simulations should be used for higher accuracy. A generic choice of transformer geometry with 370 \( \mu \text{m} \) outer diameter with 25 \( \mu \text{m} \) trace width/spacing fails to achieve a \( K \) of 0.7 and also falls short of achieving a 200 fF crossover capacitance. This geometry is
documented in table 3.5 for purpose of comparison with the nominal geometry. In order to boost the crossover capacitance, the trace width was increased to 47 µm. Increasing the trace width means a reduction in inductance and hence a higher loop area is required to realize a 2 nH inductance with wider traces. The additional loop area is also needed to increase K from 0.6 to 0.7. Several references in the literature capture closed form expressions for transformer circuit model elements and these equations can be used to obtain quick first pass estimates while designing transformer geometries [18, 19, 20, 21].

Table 3.5: Transformer geometry to achieve $L_1 = L_2 = 2$ nH; $C_c = 200$ fF; $K = 0.7$ across a 25 µm dielectric spacing with a dielectric constant of 4.0; 25 µm minimum trace width; 50 µm microvias

<table>
<thead>
<tr>
<th>Outer Diameter (D in µm)</th>
<th>W/S (in µm)</th>
<th># of Turns</th>
<th>K</th>
<th>$C_c$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>370</td>
<td>25/25</td>
<td>2</td>
<td>0.60</td>
<td>88.85 fF</td>
</tr>
<tr>
<td>460</td>
<td>47/25</td>
<td>2</td>
<td>0.70</td>
<td>200.3 fF</td>
</tr>
</tbody>
</table>

Integrating a series resistance of 25 ohms is hard through geometrical optimizations for a spiral inductor on PCB due to minimum trace widths of the order of 25 µm. Options include using an embedded resistor or building inductor coils with thin metallization to increase series resistance on organic substrates. These results show that broadband impedance matching can be achieved for an inductive connector through $C_c$ and series termination.
optimization and table 3.5 also documents geometrical details of a nominal structure to build this in a 1 mil laminate technology. Since an inductive channel is frequency dependent, numerical optimization of model parameters requires extensive simulation on a case by case basis specific to the edge rate and signaling data rate of the system. The transfer function in equation 1 can be plugged in a TDR simulation setup to determine precise numerical values of $C_c$ and series termination to minimize reflection noise. Signal to noise ratio values can be tabulated and analyzed for different cases.

### 3.3.2.7 In phase or out of phase

The difference in performance of an in-phase and out of phase transformer arises due to the crossover capacitance. If the value of crossover capacitance is too small to impact the transformer model then the choice of winding sense doesn’t matter. The choice of edge rate in a digital application sets the upper limit on the highest frequency content in a Pseudo random (PRBS) bit sequence. If the bandwidth extension effect of out of phase coils helps only with frequencies higher than the highest spectral content in the PRBS data then the choice of winding sense doesn’t matter, else it does.

### 3.4 EM Modeling for transformers

As discussed in the section on transformer modeling, if the electrical length of the transformer is less than or equal to $\lambda/10$ at the highest frequency of interest lumped models
are sufficient. Else distributed circuit models or EM modeling is necessary. The complexity of return path structures, PTH vias and electrically large transformers could make EM modeling necessary in some inductive connector designs.

![Figure 3.33: Simulation setup in Sonnet](image)

This section shows some simulation results obtained using Sonnet to validate the tradeoffs we observed with circuit model analysis. Let’s consider a 500 µm outer diameter transformer with 25 µm trace width/space and 3 turns which has an inductance of 5.1 nH. Figure 3.33 shows the simulation setup in Sonnet to extract the S parameter data files for this structure. Figure 3.34 shows $S_{21}$ for a 500 µm out of phase transformer across a gap spacing of 5 µm. Here crossover capacitance between the coils is varied by changing the dielectric constant of the material occupying the space between the coils. The value of $S_{21}$ remains similar up to 3 GHz and thereafter the roll-off in $S_{21}$ is influenced by the value of crossover capacitance. Also when the gap spacing is as small as 5 µm the K is fairly high and in this case the value of crossover capacitance needed to optimize $S_{21}$ is relatively small. In fact excess crossover
capacitance is detrimental in this case. The optimum value of crossover capacitance desired can be determined from pole/zero analysis of the voltage transfer function.

Figure 3.34: $S_{21}$ for varying crossover capacitance when gap spacing = 5 µm
Figure 3.35: $S_{11}$ for varying crossover capacitance when gap spacing = 5 µm

Figure 3.35 shows $S_{11}$ for varying crossover capacitance values. The value of crossover capacitance should be optimized to deal with reflections in the operating bandwidth. Series termination is needed to deal with low frequency reflections. How beneficial series termination is in a certain scenario depends on the value of series terminations, load terminations and whether the system is a single connector or two connector system. Analysis along the lines of the discussion in section 6.2.6 should be used to determine desired series resistance.
Figure 3.36: $S_{21}$ for varying crossover capacitance when gap spacing = 15 µm.

Figure 3.36 shows $S_{21}$ for varying crossover capacitance when gap spacing = 15 µm. When gap spacing between the inductor coils increases to 15 µm the K drops and in this case a higher crossover capacitance is needed to boost the forward transfer function ($S_{21}$).
Also when the $K$ is lower a higher value of crossover capacitance is needed to tune the return loss as shown in Figure 3.37. However a point to remember is that the optimum crossover capacitance determination should be made after analyzing the step response as well as discussed earlier. Figure 3.38 shows the difference in performance of $S_{21}$ between in phase and out of phase wound transformer. As expected the out of phase transformer has a higher bandwidth compared to the in phase transformer due to the beneficial effect of crossover capacitance. The 3 dB bandwidth for the out of phase structure is 3.5 GHz while the 3 dB bandwidth for the in phase structure is 2.5 GHz.

Figure 3.37: $S_{11}$ for varying crossover capacitance when gap spacing = 15 $\mu$m
Figure 3.38: $S_{21}$ for in phase and out of phase transformer

Figure 3.39: $S_{11}$ for in phase and out of phase transformer
Figure 3.39 shows improved return loss for the out of phase transformer compared to the in phase structure. For example the return loss values are better than -10 dB for the out of phase transformer between 1.5 GHz to 3 GHz. Return loss values are unacceptable for the in phase transformer and less than -5 dB in the 1.5 GHz to 3 GHz range. The improved return loss performance of the out of phase structure was earlier explained through lumped circuit models and this is validated here by the EM simulations as well.

3.5 Inductive Socket System

Impedance matching constraints are different depending on the application of the inductive interconnect structure in a system. For example an inductive socket system such as the one shown in Figure 3.2 has only one inductive interconnection in it’s transmission path and it can be terminated on both ends by 50 ohm matched driver and receivers. Adding an additional series termination to the transformer interconnect structure adds more loss without discernible benefits in mitigating reflections. The main problem here is introduced by PTH via stubs which introduce reflections at high frequencies depending on its length. The effect of PTH via stubs is reduced typically by careful layout and the more expensive option of back drilling to minimize stub lengths. Figure 3.40 shows block diagram for an inductive socket system.
Let's consider the system in Figure 3.40 without the stubs for simplifying analysis in order to build more understanding. In this system all reflections are then negated at the matched driver/receiver 50 ohm interface at least on 2\textsuperscript{nd} incidence. However the magnitude of the backward traveling wave at interfaces between transmission line and transformer can reduce signal to noise ratio, induce some crosstalk with adjacent neighboring lines and hence the amplitude of this backward traveling wave must be as small as possible. Analyzing reflections in a complex system with multiple components is challenging. TDR is a valuable tool for this analysis. For example a good way to optimize an inductive socket system would be to have a transformer interconnect driven by an ideal transmission line to study reflections using TDR. An ideal transmission line is more intuitive for analysis since reflections are not dampened by losses on line in this case and it is a way to gauge intrinsic impedance matching ability of the interconnect structure. TDR simulations are a good way to determine the types of discontinuities in the system and the time at which they occur. ADS has built in tools which extract TDR impedance and reflection coefficient profiles. The extraction can be done
from the S-parameter data or from the step response. Figure 3.41 shows the simulation setup for TDR. The DUT in this case is a short and the purpose of the Z profile plot is a “sanity check” before we proceed to discuss Z profile plots for inductive connectors. The ideal transmission line in the simulation has a ~10 ns delay and the TDR Z profile plots should be observed after 20 ns in the simulation which is the time for round-trip delay. The plot was started at a short instant of time before 20 ns to avoid some errors generated in the internal algorithm used by ADS for TDR data generation.

![Figure 3.41: S-parameter simulation setup with 50 ohm reference port impedances for TDR extraction. DUT is a short circuit](image)

Figure 3.41 shows the TDR Z profile plot versus time when the DUT is a short. As expected the impedance profile quickly decays down to 0.
**Figure 3.42:** TDR Z profile plot for a short circuit

Figure 3.43 shows the simulation setup with inductive and capacitive discontinuities added to the DUT. Figure 3.44 shows the extracted Z profile. A series inductor looks like an open for a short instant of time (i.e. at high-f) and produces a positive spike in the impedance profile and a shunt capacitor looks like a short at high frequencies and produces a negative spike in the impedance profile. In fact this is probably a fairly simplistic model for a real world connector – A connector pin has series inductance and via stubs could produce shunt capacitive parasitics.

**Figure 3.43:** Simulation setup for TDR extraction. DUT is a 1 nH series inductor followed by 500 fF shunt capacitor
Let’s move to understanding TDR for a transformer. Remember a perfectly coupled transformer with no leakage and parasitics can be represented be just a single shunt inductor in its equivalent T-model. Figure 3.45 shows the equivalent TDR simulation setup for a transformer with 5nH inductors coupled perfectly with no parasitics. An ideal transformer with 5 nH inductors with $K = 1$ can be represented by a 5 nH shunt inductor electrically.

**Figure 3.44:** Simulated TDR Z profile plot for the DUT consisting of series inductance and shunt capacitance

**Figure 3.45:** TDR simulation set up for an ideal transformer with 5 nH inductors
Figure 3.46 shows the TDR Z profile plot for the ideal transformer (“inductive connector”). At high frequencies the inductor looks like an open. The TDR input sampler sees an open circuit in shunt with a 50 ohm load termination at high frequencies. The parallel combination of a 50 ohm shunt resistor with a high impedance load looks like ~50 ohms effectively and for a short instant of time the shunt inductor looks like a 50 ohm interconnect structure. Thereafter over time at lower frequencies the inductor looks like a short and the impedance quickly decays to zero.

**Figure 3.46:** Simulated TDR Z profile for an ideal inductive connector (5 nH inductors, K = 1)

The inductive connector looks like a matched impedance only for short instants of time (i.e. high f). While 50 ohms impedance is desirable from a connector over the f-band we have to note that -10 dB of return loss is acceptable for most digital applications and this implies that about 20ohms of deviation from 50 ohms might be acceptable. A perfectly coupled transformer realized with 5 nH inductors has return loss better than -10 dB only at
frequencies over 2.5 GHz. For an inductive connector TDR should be used to evaluate impedance profiles only over shorter periods of time corresponding to the frequencies at which the system is matched. It can be used to gauge impedance discontinuities created by leakage inductance which grows as $K$ reduces from the T-circuit model shown in Figure 3.13. These series leakage inductances would produce positive spikes in the impedance profile representing an inductive discontinuity as indicated in Figure 3.44. Most commercial connector manufacturers use their mechanical connectors for NRZ signaling. So they plot their Z profiles over longer periods of time to check if the component looks like 50 ohms over the entire frequency band. In our case if the inductive connector was realized with large 1250 nH inductors with perfect coupling just for sake of argument then it would look like a matched connection over the entire band of frequencies and we can do a one to one comparison with Z profile plots generated by connector makers. Figure 3.47 shows Z profile plot for a large transformer built with 1250 nH inductors which are perfectly coupled.

**Figure 3.47:** Simulated TDR profile for an ideal inductive connector with large inductors (1250 nH)
A 50 ohm series termination can be added to help the analysis and deviation of impedance from 50 ohms can be used to gauge discontinuity from an inductive connector. Figure 3.48 shows the frequency (f) domain simulation setup when a 50 ohm series termination is added to a perfectly coupled inductive connector realized with 5 nH inductors.

![Diagram of a 5 nH transformer with series termination](image)

**Figure 3.48:** f-domain model for a 5 nH transformer, $K = 1$ with 50 ohm series termination

Figure 3.49 shows the frequency response for this model. Return loss is better than or equal to -10 dB from DC to high frequency.

![Frequency response graph](image)

**Figure 3.49:** Frequency response for the model shown in figure 3.40 (impact of adding series termination on the frequency response)
This system will look like a matched system to the TDR simulations over longer instants of time and can be used for comparison with Z profile plots of other commercial connectors. Figure 3.50 shows the simulated TDR z profile showing the impact of adding the series termination for the simulation setup in Figure 3.48. Addition of a series termination solves the low frequency impedance matching problem by achieving a 50 ohm match. At higher frequencies the inductive impedance of the transformer system causes a deviation in impedance profile to 75 ohms. This also brings up the point that a lower value of series termination<50 ohms can be used to strike a balance between high frequency and low frequency impedance matching.

![Figure 3.50: Simulated TDR Z profile showing impact of adding the series termination](image)

Figures 3.51, 3.52 show the TDR simulation setup and Z profile plot when K < 1. Due to the leakage inductance, the TDR Z profile exhibits a much higher deviation from 50 ohms compared to the case when K = 1.
Figure 3.51: Circuit model for transformer with $K = 0.7$

The series leakage inductance contributes to a rising impedance profile with frequency. Crossover capacitance tuning can be used to mitigate this effect since a series capacitor has a falling impedance profile with frequency. TDR simulations can be used to determine what values of magnetic coupling coefficient are acceptable in transformer design for high speed digital applications. A reasonable goal based on [53] is to keep series leakage inductance $< 1$ nH.
Figure 3.52: TDR Z profile plot for simulation setup in Figure 3.43 (impedance in ohms versus time in nsec)

TDR scopes and simulation algorithms typically use 35 ps rise times to resolve discontinuities well. But quite often most real applications have only 70-100 ps edge rates. So TDR plots obtained with 35 ps rise times might tend to over amplify the impedance mismatch problem because a 35 ps edge has a higher knee frequency than a 70-100 ps edge and the transformer does not need to be well matched at such high frequencies. In these cases some post processing techniques or rise time filters must be used to evaluate performance as a function of edge rate [114].

Based on the discussion on TDR, the goal is to reduce leakage inductance and parasitics to minimize impedance mismatches. Capacitive tuning can also be used beneficially as discussed in previous sections to aid impedance matching for inductive connectors. The goal of the inductive interconnect design in a socket system is to maximize signal transfer at X Gbps by optimizing transformer model parameters and minimize backward traveling
reflected waves using TDR as an aid. Stubs which are part of most real socket channels introduce resonances in frequency response and they have to be dealt with through careful layout and backdrilling to minimize stub lengths to shift resonances to higher frequencies. The best way to minimize leakage in a practical transformer design is to build transformers with small inductance values 1~2 nH with K \geq 0.7 and compensate to the extent possible with capacitive tuning. Series terminations can be used to achieve low frequency impedance matching while capacitive tuning can be used to achieve high frequency impedance matching. Voltage transfer function analysis in conjunction with TDR must be used to optimize \( C_c \) and series termination on a case by case basis in different applications.

### 3.6 Inductive backplane connector system

#### 3.6.1 Double pulse effect in Backplane connector channels

An application for inductive interconnect structures is in communicating between two daughter cards through a 30 cm to 1 m long backplane as shown in Figure 3.1. An ideal transformer can be represented by just a shunt inductor using its T-equivalent circuit as shown in Figure 3.53 where \( M = K \times \sqrt{L_1 \times L_2} \).
Figure 3.53: T-Model for an ideal transformer with $K = 1$

Figure 3.54 shows simulation setup to study step response of the channel shown. A series resistor followed by a shunt inductor is a differentiator with transfer function $\left(\frac{j\omega L}{R+j\omega L}\right)$. The first transformer in Figure 3.54 is driven by a 50 ohm resistor which leads to first differentiating effect and the 2nd differentiation occurs at the 2nd transformer which is driven by the complex impedance of the preceding stages. Hence a digital step input passing through a channel with 2 transformers shown in Figure 3.54 encounters double differentiation and this produces a double pulse as shown in Figure 3.55.

Figure 3.54: Simulation setup in ADS for 2 ideal transformers communicating over a lossless 50 ohm line
Figure 3.55: Step response at output of 2\textsuperscript{nd} transformer in Figure 3.46

The delay of the lossless 50 ohm transmission line in Figure 3.54 is set to 2.5 ns so that the reflections don’t superimpose over the double pulse. If the 2\textsuperscript{nd} transformer had a large inductance value of the order of 25–50 nH the double pulse can be suppressed. This happens because the 3 dB coupling frequency of the channel moves to frequencies close to DC and hence 2\textsuperscript{nd} differentiation effect is suppressed. This is analogous to making the transfer function closer to unity instead of high pass at the 2\textsuperscript{nd} transformer. However large inductances are hard to realize in practice in laminate processes in sub-mm pitch.

Alternatively the receiving side coupling element can be any passive component with a wide passband. This concept is illustrated with a simple simulation setup. A complete AC coupled system including coupled inductors on the transmitting side, a series coupling capacitor on the receiving side, with 1cm stubs representative of daughter cards, was simulated in Hspice over a 1m long 50 ohm transmission line on FR4. The W model was used to capture the behavior of the transmission line in Hspice. Figure 3.56 shows the system level view of the
simulation setup. Figure 3.57 shows the circuit model for a transformer on the transmitting side obtained using commercial CAD tools. In simulation the transmitter is an ideal voltage source while a high impedance receiver is modeled with a simple 200 ohm resistor. A 50 ohm parallel termination was also used on the transmission line to suppress reflections. Due to low frequency content in the NRZ random data stream, the receiving side needs a coupling element with a wide passband in the frequency domain, therefore, a 2 pF series capacitor was used. Alternatively a transformer using high inductance values of about 25 nH can be used on the receiving side to obtain similar performance. However, long winding lengths, leading to distributed behavior, are needed to realize high inductance values in PCB processes. This increases complexity from a modeling perspective and a valid model needs to be employed to obtain a realistic simulation result. Figure 3.58 shows the simulated “AC Coupled” eye diagram obtained at 2 Gbs for 4000 bits of random data, with a maximum run length of 7 bits. While there is some noisy information in the eye indicated by the vertically bunched lines at the center, it is below 50 mV. The receiver can be designed so that information below this threshold is rejected.
Figure 3.56: Simulation setup

Figure 3.57: Transformer model
Another alternative to using wide passband receiving side components to suppress double pulse is to drive the first transformer with a low impedance driver. The first transformer in Figure 3.54 is a differentiator with transfer function \((j\omega L/R + j\omega L)\) and the transfer function goes to unity when \(R \ll j\omega L\). But this is hard in practice too as there is a short 50 ohm transmission line in a connector or socket system in reality between the driver and the inductive interface as shown in Figures 3.1, 3.2. This would place constraints on the output impedance of the driver. The most viable alternative is to use transmit side waveshaping to subtract out the double pulse.
3.6.2 Reflections in a Backplane Connector Channel

The transmission line in Figure 3.54 for a two transformer system sees the input and output 50 ohm driver/receiver load through the transformer which is a short circuit at DC. Here impedance matching is more critical compared to a single transformer system since there is no impedance matching through the driver/receiver impedance. The transmission line is assumed to be lossless to simplify the analysis and gain better understanding of the fundamental factors which affect performance. Here a 50 ohm series termination is needed to provide impedance matching. Adding a series termination adds attenuation and it makes sense to use the series termination just to suppress the reflections at 2nd incidence rather than using series terminations on both sides of the transmission line. Figure 3.59 shows a system simulation setup in ADS to study step response of the channel to understand reflections.

**Figure 3.59:** System simulation setup in ADS with no series terminations
**Figure 3.60:** Step response at the Node OUT in Figure 3.51

The step response in Figure 3.60 shows both double pulse and reflections in the system. The reflections in the system are observed after 8 ns (after 3x delay of the transmission line). The signal swing is 220 mV and the worst case magnitude of the reflected bump is 40 mV. Ignoring the double pulse this leads to a signal to noise ratio of 14.8

**Figure 3.61:** System simulation setup with Low Z driver and 50 ohm series

Figure 3.62 shows step response when series terminations are added in the channel as shown in Figure 3.61 and a low Z driver is employed. The low Z driver negates the double pulse
while the series terminations suppress the reflections occurring on the channel after 8 ns. A transmission line with round trip delays as long as 8 ns was used in the simulation in order to isolate the double pulse and reflection effects that arise in a 2 transformer system.

**Figure 3.62:** Step response at Channel output with 2 series terminations

**Figure 3.63:** Channel with series termination only at 2\textsuperscript{nd} incidence
Figure 3.64: Step response with one series termination at 2\textsuperscript{nd} incidence

Figure 3.64 shows step response with series termination on one end of the transmission line to suppress reflections occurring at 2\textsuperscript{nd} incidence with termination placement as shown in Figure 3.63. This is equally effective in dealing with reflections with higher signal swing compared to the case with 2 series terminations on either end of the transmission line. Figure 3.65 shows the same channel in Figure 3.61 with a 50 ohm driver instead of a low Z driver. This would imply that double pulses will persist in the system and there would be some reflections due to the double pulse as well. In this case the reflections would be worse compared to the case in Figure 3.61. However we need to compare primarily to the case with no series terminations in the channel as shown in Figure 3.59. Figure 3.66 shows the step response.
Figure 3.65: Channel with series termination only at 2\textsuperscript{nd} incidence and 50 ohm driver

The worst case magnitude of the negative reflected bump in Figure 3.66 is 24 mV and the peak signal swing is 182 mV. This leads to a signal to noise ratio of 17.96 dB. This calculation doesn’t take the double pulse into account. This is better than a computed signal noise of 14.8 dB for the step response in Figure 3.60. We can increase the signal to noise ratio closer to desired values of >= 20 dB by employing a low Z driver in Figure 3.65.
optimal scenario is the case shown in Figure 3.63 with a low Z driver and a 50 ohm termination placed after the first connector at the input side of the transmission line.

The transfer function in equation 1 in section 3.3.2.6 reveals that load termination has more impact on the zeros (i.e. reflections) than the source termination. Hence the series termination placed in the 2 connector channel is more effective after the forward travelling wave gets reflected once and traverses back on the channel backwards as now the 2nd transformer sees the series termination as a load. The analysis for a backplane connector has been done without including the effect of the stub at the driver-transformer interface. This is primarily to keep the analysis easy to follow and break up the problem easier. To summarize the goal of inductive interconnect design in a 2 transformer system is to maximize signal transfer at X Gbps with good signal to noise ratio. Dealing with double pulses would most likely require transmit side waveshaping. In addition to methods discussed for reflection control thus far, using losses on FR4 might also be beneficial in dampening reflections in a 2 transformer system.

### 3.7 Process Variations for Inductively coupled Systems

When an inductive structure is used in a socket or connector application there could be some variation in gap spacing between the stacked inductors. Also there could be some misalignment between the two inductors stacked on top of each other. These variations could arise in assembly. To analyze these issues EM simulations were performed using Sonnet for
a sample transformer structure with 500 µm outer diameter. The inductors were built with 25
µm trace width/space with a 75 µm diameter circular via used for connections between metal
layers. The simulation-setup is shown in Figure 3.67. Both the inductors stacked on top of
each other have 3 turns each with a 5 nH inductance. An air gap is assumed between the two
inductor coils.

**Figure 3.67:** Simulation setup in Sonnet for a 500 µm diameter transformer

Figure 3.68 shows that peak $S_{21}$ varies by 3-4 dB when air gap spacing between the inductors
changes from 5 µm to 25 µm. Variation in $S_{11}$ is more pronounced when gap spacing
changes from 5 µm to 25 µm and this is due to the 5x variation in crossover capacitance
between the inductors. The impedance of a capacitor is inversely proportional to the distance
between the plates and this contributes to pronounced variation in $S_{11}$. 


Figure 3.68: Simulated $S_{21}$ when gap (AG) varies from 5 µm to 25 µm

Figure 3.69: Simulated $S_{11}$ when gap (AG) varies from 5 µm to 25 µm
Figure 3.70: Simulated $S_{21}$ for misalignment (m.a) in X-direction

Figure 3.71: Simulated $S_{21}$ for misalignment (m.a) in X-direction
Magnetic coupling coefficient rolls off less rapidly as explained in sec.3.8 and hence variation in $S_{21}$ is only 3-4 dB even with 5x variations in gap spacing. To keep variation in $S_{11}$ within 3-4 dB the variation in gap spacing from desired value should be within 5-10%. As discussed in section 3.3.2.6 the key goal is to ensure that variations in $C_c$ produce impedance variations in $Z_{in}$ less than or equal to +/-10%. $Z_{in}$ is a better metric to gauge impact of process variations in AC coupled system than % change in gap spacing though they are all interrelated. Figure 3.70 and Figure 3.71 show variation in $S_{21}$ and $S_{11}$ when two stacked inductors are misaligned by 10 µm and 20 µm respectively. The variation in $S_{21}$ is less than 0.5 dB when misalignment is 10 µm and about 2~3 dB when misalignment is 20 µm. The variation in $S_{11}$ is more pronounced with 20 µm misalignment since the overlap area of the inductors changes hence changing the crossover capacitance.

**Figure 3.72:** Pi model for a transformer with no resistive loss and no shunt capacitive parasitics
When vertically stacked inductors are misaligned in X-direction the magnetic coupling coefficient (K) drops. The crossover capacitance between the two inductors also drops as a result of misalignment since the overlap area of the inductors is reduced. However when K drops the term \((L_1 \ast L_2 - M^2)/(-M)\) in the pi model shown for an out of phase transformer in Figure 3.72 increases. A negative inductor can be thought of as capacitor and hence this implies a rise in capacitance from this term. This increase in capacitance fights the reduction in crossover capacitance. Hence the tolerance to misalignment depends on the factor by which the term \((L_1 \ast L_2 - M^2)/(-M)\) rises in proportion to the drop in crossover capacitance.

Even for an in phase transformer the inductive term \((L_1 \ast L_2 - M^2)/M\) would increase while the crossover capacitance reduces which also fight each other. This discussion also brings up the point that the sensitivity of transformers to process variations is geometry specific since \(M\) and \(C_c\) are both functions of transformer geometry. However the general trend is that \(S_{21}\) is more tolerant to process variations compared to \(S_{11}\). This is due to \(S_{11}\) being sensitive to capacitive tuning. Based on discussion in this section, variation in gap spacing should be less than 5-10% and misalignment should be less than or equal to 10 µm to minimize variation in \(S_{11}\) to within 3-4 dB. Higher misalignment can be tolerated if the transformer geometry is realized with traces of larger width. In this case a similar numerical misalignment contributes to less variation in crossover capacitance compared to transformers realized with narrower traces. In chapter 5 we see in experimental results that a 500 µm diameter transformer with 50 µm trace widths tolerates misalignment of 25 µm.
3.8 Capacitive vs. Inductive coupling

This section briefly touches on some of the tradeoffs between capacitive coupling and inductive coupling for completeness. The main thrust of this dissertation is inductive coupling. Capacitors are easier to model compared to coupled spiral inductors. In capacitive systems high impedance shunt terminations can be used more beneficially to tune the return loss at low frequencies while this is more difficult in the case of an inductive system because an inductor is low impedance at low frequencies. However, the problems associated with this impedance mismatch at low frequencies can be offset by using inductive coupling when signaling across long serial links so that the reflections are attenuated sufficiently over the round trip delay of the link and also by using series terminations. In addition, the use of pulsed signaling schemes where low frequency energy is minimized helps in reducing the reflected energy in the interconnect. Also the input impedance of the coupled capacitors is more sensitive to the gap spacing compared to coupled inductors. This is due to the inverse relationship of capacitance with gap spacing, while for inductors the magnetic coupling coefficient decreases less rapidly. For example, let’s assume we need an impedance match corresponding to 3 to 5 GHz range (and) let’s consider 250 µm pitch capacitor plates separated by a 10 µm gap in a dielectric of $\varepsilon_r = 4$. This produces a capacitance of 221 fF and this produces an impedance of 50 ohms at a fairly high frequency of 14.3 GHz. Reducing the gap spacing by a factor of 3 to 4 would address the issue but quite often there is not considerable freedom with this as gap spacing could be set by manufacturing tolerances and in a board to board system it could be set by surface roughness of the laminates. If the gap
spacing were 20 µm instead of 10 µm it would reduce capacitance by a factor of two and in the example above the 50 ohm match would be obtained at only 28.6 GHz. In essence the value of Capacitance is inversely proportional to Gap spacing “d” (i.e. \( C \propto \frac{1}{d} \)) which causes a faster roll-off in impedance. On the other hand coupling coefficient (K) between two coupled inductors does not drop as rapidly. Two inductors of 250 µm outer diameter with 5 turns each and metal width/spacing of 12.5 microns were simulated using ASITIC to obtain the data shown in Figure. 3.73. The data in Figure 3.73 fits to a fifth order polynomial given by

\[
K = -0.713 \times 10^{-9} d^5 + 0.156 \times 10^{-6} d^4 - 0.000143 d^3 + 0.000793 d^2 - 0.0332 d + 0.9994.
\]

**Figure 3.73:** K (vs) gap spacing for a 250 µm pitch transformer
3.9 Design flow and Summary

Figure 3.74 shows suggested design tool flow for optimizing inductive connectors and sockets before building them.

![Diagram of design flow](image)

**Figure 3.74:** Tool flow for inductive connector/socket design

Designing an inductive channel is application specific and is constraint driven. For example, the target signaling data rate sets the value of inductance. The choice of transformer area and geometry to realize this inductance is influenced by process constraints such as minimum trace width/space and via feature size. The goal is to synthesize transformer geometry with this inductance value in the given process with highest possible K, and optimum crossover capacitance to help $S_{11}$ at higher frequencies. The crossover capacitance chosen should not impact step response negatively by introducing oscillations. Embedded series terminations realized in package and board processes can be used for low frequency impedance matching. Impedance matching constraints are different for single transformer and 2 transformer
systems due to differences in the transmission path and the effect of double pulse needs to be addressed in 2 transformer systems with transmit side waveshaping. The tradeoffs and design methodologies to design an inductively coupled connector have been established in this chapter. A step by step design procedure is illustrated in the final chapter of this dissertation through a design example.
4 Inductively coupled connectors – Proof of concept

4.1 Overview

Building sub-1.3 mm pitch transformers with fine via technologies and assembling them in packaging and PCB interfaces is not feasible in readily accessible commercial processes. As part of the research progression we prototyped experiments first on low cost printed circuit boards with coarser dimensions. The objective was to demonstrate the basic feasibility of inductive connects/sockets through measurements and validate theory.

4.2 Optimizing frequency response of board to board transformers

High magnetic coupling coefficient values are desirable in inductively coupled connectors for improving insertion loss and return loss, and increasing bandwidth. The magnetic coupling coefficient between two vertically stacked planar spiral inductors is a function of many factors, such as: gap spacing, inductance and effective loop area. In a board-to-board application, the achievable gap spacing between the coupling elements is limited by the surface roughness of FR4, and the thickness of the interlayer dielectric used to isolate the coupling elements. The surface roughness of FR4 can range from 1µm to 10 µm [40], which produces a large and unpredictable variation in the gap spacing. Process limitations also constrain choice of trace width, trace spacing and realizable inductance values in a given area. These process variations limit the maximum value of the magnetic coupling coefficient.
between the inductors. Meanwhile, for high-speed applications, short decay times are required, which will affect the choice of inductance values for a particular design. Hence, the trade-offs among these factors will need to be balanced carefully.

**Figure 4.1:** Coupling coefficient (K) versus gap spacing (D) for a 10 mm outer diameter symmetrical transformer with inductance value of 27 nH

Figure 4.1 shows a plot of extracted value of coupling coefficient (K) versus gap spacing obtained using ASITIC for two 10 mm outer diameter inductors with 1 turn each having an inductance of 27 nH. Considering the surface roughness values of FR4 and the thickness values of readily available interlayer dielectric spacers (such as paper), the achievable gap spacing varies anywhere between 50 µm to 200 µm. When the gap spacing is 50 µm, K is 0.92 and when the gap spacing is 200 µm, K drops to 0.76 which limits the achievable bandwidth. There is a significant roll-off at high frequencies when K is 0.7 and this roll-off would be more pronounced for higher inductance values. Addition of an optimum value of
crossover capacitance ($C_c$) compensates for the high frequency roll-off in the frequency response. Since PCB trace widths are relatively larger compared to on chip features we can exploit the inherent cross-over capacitance beneficially to obtain desired frequency response as the crossover capacitor acts as a high pass filter. High K dielectric spacers might be useful to achieve desired values of crossover capacitance with transformers of smaller outer diameter with fine feature trace width/space. The value of crossover capacitance to obtain an input impedance match can be determined using $Z$ and $ABCD$ parameter computation from lumped circuit model approximations for transformers. This value of crossover capacitance can be realized in a transformer by adjusting the trace width and loop area. The value of crossover capacitance in a transformer can be estimated to a first order using a parallel plate estimate over the physical length of the transformer.

### 4.3 Design and Layout of Test Vehicle

Board-to-board inductively coupled connectors with outer dimensions ranging from 2.5 mm to 10 mm were built in an inexpensive two layer PCB process with minimum feature size of 7 mils (~0.175 mm) for traces and 20 mils (0.500 mm) for via holes. The FR4 substrate is 62 mils (~1.550 mm) thick with a dielectric constant ranging from 4.2 to 5.0. Transformers with outer dimensions as large as 10 mm were chosen to achieve sufficiently high magnetic coupling over gap spacing which could be as large as 50~200 µm in a board to board interface. The test structures built have an inductance ranging from 5 nH to 50 nH. For the purpose of focused discussion, transformer structures with outer diameters larger than or
equal to 5 mm with inductance values greater than 20 nH are referred to as electrically large structures in the sections that follow. Transformer structures with outer diameter less than 5 mm and inductance values less than 10 nH are referred to as electrically small structures at these frequencies. The loop area and trace width/spacing were chosen for optimal \( K \) and crossover capacitance using commercial tools, such as OEA and ASITIC. Figure 4.2 shows a picture of the test boards fabricated from Express PCB and Figure 4.3 shows the test-setup for measuring one of these transformers. A sheet of paper, approximately 90 \( \mu \)m thick, was used as an interlayer dielectric between the two inductors. Screw holes and alignment traces were used on the boards to align the coils during measurement.

*Figure 4.2:* Photo of the test circuits fabricated on PCB

*Figure 4.3:* Photo of test-setup of the transformer with SMA connectors and alignment traces/screw holes for alignment and control of the gap spacing
4.4 Measurement Results and Analysis

4.4.1 Measurement Results for Electrically large transformers on PCB

Figure 4.4 shows measured data for a 10 mm outer diameter symmetric transformer with one turn each on primary and secondary, trace width of 20 mils (~0.5 mm) and an inter-turn spacing of 10 mils (~0.25 mm). The extracted inductance from ASITIC for this structure was 27 nH. Measurements were made using a HP8510C network analyzer. TRL calibration was used to de-embed the measurements between 400 MHz to 2.5 GHz. Figure 4.5 shows the TRL standards fabricated on the PCB. An open was used as the reflect standard. The thru is the symmetric coax-microstrip transitions feeding in to the transformer at port 1 and port 2. A transmission line 6.26 cm long was used to cover the operating frequency between 400 MHz to 2.5 GHz. The transformers designed were expected to have good frequency response up to 2.5 GHz. Since these are large structures on a printed circuit board, data rates are slower and not over 1~2 Gbps in most cases. Hence TRL was designed for measurement in this band of frequencies. Copper foil ground shields and tapers were used to minimize impedance mismatch at transitions. In the measurement shown in Figure 4.4 return loss is better than or equal to -10 dB from 500 MHz to 2.5 GHz, and insertion loss is better than or equal to -3.7 dB from 400 MHz to 2.5 GHz. These performance metrics meet the performance specifications outlined for package level interconnects over at least half a decade of bandwidth [18].
Figure 4.4: Measured data for 10 mm outer diameter transformer with TRL de-embedding

![Figure showing S21 and S11](image)

Figure 4.5: TRL calibration standards

Figure 4.6 shows measured step response, for the 10mm transformer, to a 250 mV step input from a Tektronix 11801A oscilloscope. The output signal has amplitude of 160 mV. From Figure 4.6 we note that the output signal level of the transformer decays to 10% of its peak amplitude in 2.5ns which implies a maximum signaling data rate of 400 Mbps.

Figure 4.7 shows the measured “AC coupled eye diagram” at 400 Mbps for a $2^{23}-1$ random NRZ data stream. A transformer acts as a differentiator and converts the input NRZ data into pulses. A pulse receiver can be used to recover NRZ data from the pulse output.
Figure 4.6: Measured step response of the 10 mm outer diameter transformer for a 250 mV step input (160 mV output voltage amplitude; Units: 500 ps per division on X axis and 20 mV per division on Y axis)

Figure 4.7: Measured eye diagram for 10 mm diameter transformer – 400 Mbps random NRZ data (800 mV peak to peak output voltage amplitude; Units: 500 ps per division on X axis and 200 mV per division on Y axis)
**Figure 4.8:** TDR measurement for 10 mm outer diameter transformer (Units: 200 mp per division on Y axis and 2 ns per division on X axis)

Figure 4.8 shows TDR measurements for the 10mm outer diameter transformer. The TDR in this case is a plot of reflection coefficient versus time. The first small spike corresponds to a small inductive discontinuity from the SMA since it occurs earlier in time. The 2nd spike is due to the impedance mismatch at the transformer interface. The deviation in reflection coefficient in this case corresponds to an impedance value of 67.64 ohms. It must be noted that though ISI limits the performance of this test-structure at data rates beyond 400Mbps there are numerous high frequency signaling rates, when using coded data, at which board-to-board transformers produces an acceptable eye opening. Figure 4.9 shows eye diagram for
the 10 mm outer diameter transformer for 3.3 Gbps coded data with the maximum run length being four.

Figure 4.9: Eye diagram for the 10 mm outer diameter transformer for 3.3 Gbps coded data (Units: 200 mV per division on Y axis, 100 ps per division on X axis)

However the BER is poor as visible in the timing and voltage jitter in the eye. In this case, the signaling rate is high enough and the maximum run length is limited, so that more traditional signaling methods (non pulse) may be used. Here since the decay rate of the transformer is slow the next bit arrives before the high transition falls sufficiently in voltage and this is in some sense similar to NRZ signaling with droop in DC levels. To validate this behavior other transformer samples were measured to see if a similar effect was observed. Figure 4.10 shows frequency response for another transformer sample with 5mm outer diameter which had optimum $S_{21}/S_{11}$ in the band of measurement shown.
Figure 4.10: Frequency response for a 5 mm outer diameter transformer

Figure 4.11 shows eye opening at 3.3 Gbps for the 5 mm outer diameter transformer which is limited, by ISI, to operation at 500 Mbps, for pulse signaling.
Figure 4.11: Measured eye diagram for 5 mm diameter transformer - 3.3 Gbps coded $2^5-1$ NRZ data (400 mV peak to peak output voltage amplitude) (Units: 100 ps per division on X axis and 200 mV per division on Y axis)

4.4.2 Measurement Results and Analysis for Electrically Smaller transformers

Scaling to smaller transformers with smaller inductance values could potentially enable pulse signaling at higher data rates due to their faster decay times. Figure 4.12 shows the step response for a 2.5 mm outer diameter transformer with one turn each on primary and secondary. In this case, the decay time is 1 ns. The value of extracted inductance from ASITIC for this structure was 6 nH. The output signal has amplitude of 60mV for an input
voltage of 250 mV which is approximately 2.5x smaller when compared to the output signal level for the 10 mm transformer discussed in the previous section. However, with a larger input signal the output signal level would increase to an acceptable value (e.g. 1 V input = 240 mV output). Figure 4.13 shows the measured AC coupled eye diagram for a 2.5 mm outer diameter transformer with one turn each on primary and secondary for random NRZ data at 1.45 Gbps.

![Figure 4.12: Measured step response for a 2.5 mm outer diameter transformer for a 250 mV step input (60 mV output voltage amplitude)](image_url)
Figure 4.13: Measured eye diagram at 1.45 Gbps (Units: 200 ps per division on X axis and 200 mV per division on Y axis)

The ringing in the waveforms in Figure 4.13 relative to the ideal step response observed in Figure 4.12 are due to some noise from the HP8133 source.
Figure 4.14: Measured eye diagram for a cable from HP8133 to oscilloscope (Cable is Non-ideal) (Units: 500 ps per division on X axis and 100 mV per division on Y axis)

Figure 4.14 shows measured eye diagram for just a low loss cable connected between HP8133 signal generator and the oscilloscope. There is noise in the eye even in this measurement. Some of the ringing could also be due to transmitting high bandwidth information over a band limited structure. For example the distributed nature of the transformer with the L, C elements in combination with leakage inductance could degrade the 3 dB bandwidth and this in turn could lead to the effects shown in Figure 4.13. One way to address this issue is to limit the edge rate so that excessive high frequency information is not being transmitted. Figure 4.15 shows frequency response in a band between 4.1 GHz to 9 GHz for the 2.5 mm outer diameter transformer corresponding to the region where optimum $S_{11}$ was observed. A point to be noted is that TRL calibration was designed to de-embed only
until 2.5 GHz since most of the transformers designed work at only ~1 Gbps data rates in the time domain. Hence this measurement was made with just OSLT calibration on the HP8510 network analyzer. The objective of this frequency domain experiment was just to confirm that $S_{11}$ is narrowband for a transformer with small inductance values since the 3 dB coupling frequency is higher compared to transformers with larger inductances. The effect of de-embedding would be to remove 1~2 dB loss from $S_{21}$ and improve the return loss by a few dB.

![Plot of $S_{21}$ and $S_{11}$](image)

**Figure 4.15:** Measured f-domain data for 2.5 mm outer diameter transformer

In this case capacitive tuning dose not help in tuning $S_{11}$ in the band of interest corresponding to 1.45 Gbps digital NRZ data with 200 ps edge rates. The inter-layer dielectric between the inductors is a sheet of paper 90 µm thick. As we scale from 10 mm outer diameter to 2.5 mm outer diameter the achievable K drops for the same gap spacing. Unless the gap spacing scales down it is hard to achieve $S_{11}/S_{21}$ optimization for transformers with smaller outer
diameter and lesser inductance. Figure 4.16 shows layout for designs fabricated on a 2\textsuperscript{nd} iteration in a 4 layer PCB process with 14mil thick substrates. The objective was to scale down in size and also to build embedded transformers on PCB for better characterization. With an embedded transformer the gap spacing between the inductors is fixed and hence it makes characterization/analysis easier.

![Photo of PCB Layout](image.png)

**Figure 4.16: Photo of PCB Layout**

Table 4.1 summarizes step response measurements on transformers with varying outer diameters, inductances with varying gap spacing and dielectrics. The table shows output voltage in response to a 250 mV step input and time taken for transformer step response to decay to zero. As expected the decay times are faster for transformers with smaller inductances while the signal swing is higher for transformers with large inductances. Transformer design for pulse signaling is a tradeoff between signal swing and inter symbol interference (ISI).
The term assembly in the table refers to the uncertainty in board to board gap spacing introduced due to warpage on FR4. In Table 4.1 there is one transformer measurement for a 3.3 mm diameter embedded transformer on a multi-layer PCB. Here the gap spacing between the inductors is known to be 64 µm based on dielectric stackup. We see from table 4.1 that the 3.3 mm embedded transformer with 64 µm gap spacing produces a similar output voltage within 5mV of the 2.1 mm board to board transformer. The gap spacing for the 2.1 mm board to board transformer is 25 µm (thickness of polyimide film) + assembly (i.e. warpage). The
3.3 mm diameter embedded transformer has larger loop area and inductance compared to the 2.1 mm diameter transformer. Hence it is expected to produce larger output voltage compared to the 2.1 mm diameter transformer for the same gap spacing. Since the magnitude of output voltages are comparable for the 2.1 mm diameter transformer and the 3.3 mm embedded transformer the gap spacing for the 2.1 mm diameter transformer is definitely less than 64 µm. Hence the uncertainty introduced in gap spacing during assembly is less than 39 µm. From the results discussed, smaller inductance values with acceptable K, well controlled gap interfaces, optimal crossover capacitance, and coded data streams may be required to enable high density AC coupled connections to signal at Gbps+ data rates as we scale PCB processes with advanced manufacturing capabilities.

### 4.4.3 Measurement Results – In phase vs Out of Phase

Chapter 3 discusses difference in performance of in-phase and out of phase transformers in the presence of crossover capacitance. Measurements were performed to validate the theory presented in chapter 3 and the results are shown below in Figure 4.17.
Figure 4.17: Measurements with in phase and out of phase winding for a 3 mm diameter transformer with one turn on primary and secondary

Return Loss Bandwidth is about 2.2 GHz for the out of phase structure. Insertion Loss bandwidth is extended for the out of phase structure. These results are consistent with the theory presented in chapter 3 where a bandwidth extension effect is observed.

4.4.4 Measurement - Impact of Series termination

In chapter 3 we suggested using series termination to deal with low frequency reflections. We validate this with measurement. In this case the series termination is a discrete surface mount component. In the long term embedded resistors on PCB can be used to minimize high frequency parasitics. Figure 4.18 shows experimental data for a 3.3 mm outer diameter embedded transformer with 6 nH inductances built on a multi-layer printed circuit board. The gap spacing between the two vertically stacked inductors is 64 µm. An embedded transformer is used as the validation experiment since there is uncertainty with predicting the
gap spacing in transformer coupling across laminate interfaces due to surface roughness, warpage of printed circuit boards which in turn makes analysis harder. Figures 4.18(a) and 4.18(b) show the frequency response for the transformer without series termination and with a 47.5 ohm surface mount series termination mounted on the PCB.

(a): Frequency response for a 3.3 mm outer diameter embedded transformer on a multi-layer PCB with no series termination

(b): Frequency response for a 3.3 mm outer diameter embedded transformer on a Multi-layer PCB with 47.5 ohm series termination

Figure 4.18: Frequency response of embedded transformer
This measurement data shows that you can use the series termination to improve the return loss at low frequencies without significantly affecting high frequency return loss until 3 GHz. The attenuation ($S_{21}$) is higher with the series termination at lower frequencies. It contributes beneficially to system bandwidth at frequencies over 2 GHz in combination with the crossover capacitance. Figure 4.19 shows TDR measurement for the embedded transformer with a 47.5 ohm series termination added.

![Figure 4.19: TDR measurement for the embedded transformer with 47.5 ohm series termination](image)

This TDR shows reflection coefficient versus time. There is a significant deviation of impedance to 95 ohms corresponding to the spike in reflection coefficient. But remember a
TDR measurement uses 35 ps edge rates. A 35 ps edge corresponds to a knee frequency of 14
GHz. The impedance deviation that we see is clearly over-amplified. Figures 4.20, 4.21 show
measured eye diagram at 1.25 Gbps and 2.4 Gbps respectively for the embedded transformer
with series termination.

**Figure 4.20:** Eye diagram at 1.25 Gbps for embedded transformer with series termination
(Units: 50 mV per division on Y axis and 100 ps per division on X axis)
4.4.5 Measured results – System

Figure 4.22 shows test setup and measured data for a system consisting of two transformers communicating across a 7.5 cm microstrip line on FR4. This is similar to the backplane connector channel discussed in chapter 3. Reflections and double pulses are dominant issues in this system unless a combination of series termination, longer lines and waveshaping are used to mitigate these effects.
The transformers used in the system are of 10 mm diameters which have wideband $S_{11}$ from 500 MHz to 2.5 GHz. However since the inductance values are as high as 27 nH the decay time is of the order of 2.5 ns and operation is only possible up to 400 Mbps. Here measurement is shown at 200 Mbps. The transformers are not impedance matched at low frequencies. The eyes show the presence of both reflections and double pulse. Low frequency reflections can be dealt with by using series terminations to achieve a 50 ohm match and by using longer traces on FR4 to dampen out the reflected waves. The double pulse is harder to deal with. Though in theory the double pulse can be eliminated by using wider passband components on the receiver side or low impedance drivers it is hard to realize in practice as discussed in chapter 3. A more realistic way of dealing with double pulses is by using waveshaping and equalization at the transmitter side to subtract out the double pulse.
4.4.6 Measurement Results - Density

Figures 4.23 and 4.24 show the test setup and measured isolation for two 3 mm outer diameter inductors of one turn each with an inductance of 7.8 nH. The results indicate that isolation is better than or equal to -20 dB up to 4 GHz even when the spacing between the inductors is 20% of the outer diameter. This indicates potential for dense AC coupled connections as we scale to high density PCB processes with 1 mil (~0.025 mm) feature size for the traces with 50 μm blind via capability.

![Test-setup for measuring crosstalk](image)

**Figure 4.23:** Test-setup for measuring crosstalk
4.5 Modeling Board to Board Transformers

The 1:1 aspect ratio of the width to thickness of the wires, multiple layers of metallization, complexity of ground shield structures and the three dimensional nature of the problem quite often make transformer modeling quite time consuming and unwieldy. Quite often measured data from test-structures is used to serve as a guide in the design process. Commercial CAD tools such as ASITIC and OEA can be used to predict inductance and magnetic coupling coefficient. Winding resistance and parasitic capacitance to ground can be estimated from process parameters. Crossover capacitance can be estimated using a parallel plate estimate over the overlap area of the inductors. On a PCB, long winding lengths are needed to realize reasonable inductance values, which in turn lead to distributed behavior. Hence, multiple $\pi$ sections are needed to obtain a valid electrical circuit model for board to board transformers.

**Figure 4.24:** Crosstalk between two 3 mm outer diameter inductors spaced 0.65mm apart
Figure 4.25 shows a distributed circuit model for board to board transformers. This was used to model the measured data for the 10 mm outer diameter discussed in section 4.4.1. The estimated inductance value from ASITIC was 27 nH and the extracted value of K was 0.86.

![Circuit model diagram](image)

**Figure 4.25:** Circuit model \( (L_1 = 9 \text{ nH}; L_2 = 9 \text{ nH}; R = 1 \text{ ohm}; K = 0.9; C_c = 1 \text{ pF}; C_p = 100 \text{ fF}) \)

Figure 4.26 and Figure 4.27 show comparison of measured versus simulated eye diagrams.
Time domain simulations are used instead of frequency domain results. While the correlation with $S_{21}$ is reasonably good for the distributed model it is hard to numerically match $S_{11}$ partly because return loss is more sensitive to the precise values of the capacitive parasitics in
the model. However, the bandwidth of the simulated $S_{11}$ follows the $S_{11}$ bandwidth of the measured data. The bandwidth of $S_{11}$ is defined in this work as the region where $S_{11}$ is better than or equal to -10 dB. While frequency domain data is very useful, precise model fitting is often cumbersome. Quite often in a digital application it is more informative to look at time domain data. Countless hours were spent on EM modeling with both SONNET and HFSS for electrically large transformers on PCB in addition to distributed circuit models. While the trends observed in EM simulation matched measured data conceptually, numerical matching was hard. The real world measurement environment is lossy and a low Q environment while EM simulations are typically high Q in nature. For example this distinction led to some resonances being observed in EM simulations at certain frequencies which were pronounced. In measurements, resonances were observed at the same frequencies but the notch in frequency response was far less pronounced and mitigated quickly due to the nature of the lossy environment. A low Q environment has more loss and broader bandwidth while a high Q environment has less loss and narrow bandwidth. Other potential problems with EM simulations for electrically large structures include meshing. The transformer diameter is of the order of 10 mm. But the gap spacing between the coils is of the order of 50 µm to 100 µm which contributes to a large aspect ratio which makes accurate meshing harder in the EM tools. Figure 4.28(a) shows simulation results from HFSS for the 10 mm outer diameter transformer discussed earlier in Section 4.4.1. Measured S parameters for the 10 mm outer diameter transformer are also shown in Figure 4.28(b) for comparison. The measurements include the effect of the feedlines (i.e no TRL calibration) to match the HFSS simulation setup.
4.28 (a) HFSS simulation for a 10 mm outer diameter transformer

4.28 (b) Measurement for 10 mm diameter transformer simulated in Figure 4.28(a)

Figure 4.28: Measurement and simulation for 10mm diameter transformer
While the measurement shows a tiny resonant notch in $S_{21}$ at 600 MHz this is more pronounced in HFSS simulation due to reasons discussed earlier. The resonance at 3.2 GHz in the measurement is also observed in the HFSS simulation. The bandwidth of the simulated $S_{21}/S_{11}$ follows the trend of measured data though precise numerical matching is hard due to reasons discussed. In the measurement setup the gap spacing is also influenced by warpage, which is hard to model in the simulation setup in HFSS. Figure 4.29 shows the 3D model setup in HFSS simulation.

Figure 4.29: 3D model for the 10 mm outer diameter transformer in HFSS

The objective of this work is to realize electrically small connectors with as fine pitch geometries as feasible. As we move towards this end goal, complexity of modeling reduces and lumped modeling would be sufficient in most cases while EM modeling could be
required for some structures with moderate complexity. The goal of the PCB experiments was to validate theory with experimental results, analyze/understand results obtained to move further on the learning curve towards the end goal.
5 Fine pitch inductively coupled connectors for Multi-Gbps Pulse Signaling

5.1 Overview

In chapter 4, a basic proof of feasibility was established through measurement of coarse pitch transformers on low cost printed circuit boards. To have an application that competes quantitatively with other connectors we need to be able to demonstrate multi-Gbps signaling with sub-1.3 mm pitch transformers. The following sections discuss experimental work, simulation and analysis related to characterization of inductive interconnections for socket and backplane connector channels.

5.2 Experimental work for characterizing transformers:

5.2.1 Experiment design, layout and Test Frame

We fabricated inductive test-structures through RTI in a 3 metal layer substrate process with similar physical structure, assembly and layout to the one reported in [88]. Figure 5.1 shows the substrate stackup. Figure 5.2 shows the layout for the mask that was designed and sent to fabrication. The mask includes test-structures built by various people within the group. The inductive experiments on the mask were built by John Wilson and me. The top metal layer
was used for the Inductive I/O structures while routing was done through 50 ohm striplines on the inner metal layer.

**Figure 5.1:** 3 layer substrate process with buried bumps (2 µm thick copper metallization & BCB dielectric with \( \varepsilon_r = 2.65 \))

**Figure 5.2:** Mask sent to RTI for fabrication
The inductors fabricated on the complete mask had outer diameters ranging from 100 µm to 500 µm and had trace width/spacing of 5 µm/5 µm to 50 µm/50 µm. The experiment list included transformer experiments with single layer inductors, dual layer inductors, differential inductors, socket and backplane connector type channels including transmission lines and crosstalk experiments. Open test frames were included for de-embedding. There were yield problems with solder bumps on several substrates and only two sub-diced substrate samples with corresponding mating set of flipped samples arrived back from fabrication. Problems in fabrication included solder bump release, residual dielectric left on solder bumps leading to open circuits and winding shorts on inductor coils. The experiments on substrates SB1 and SB2 which arrived back from fabrication and yielded had trace width/spacing of 5 µm/5 µm. Figures 5.3, 5.4 show the substrate samples SB1, SB2 and corresponding flip-chip samples FC1 and FC2. On these there were winding shorts on some coils and solder bump yield issues on some signal paths which led to open circuits. A total of 4 transformer experiments and 6 capacitor experiments yielded totally out of 84 experiments in all on the two substrates. Of the 4 transformer experiments there were winding shorts on 2 transformer experiments. But these shorts led to a reduced inductance value on these experiments due to wider traces that were formed with adjacent turns shorting together. These structures still performed acceptably at Gbps data rates.
Figure 5.3: Substrates SB1 and SB2 with inductive test-structures

14 rows of inductor experiments: 1..14 (AND) 3 columns: a..c
(2 sub-diced substrates labeled SB1 and SB2)
Figure 5.4: Flip-chip samples to mate with SB1, SB2

One of the substrates was flipped onto its corresponding mating sample with buried bumps to create the test interface for characterizing inductive coupling. Figure 5.5(a) shows a cross sectional view of the test-setup and Figure 5.5(b) shows a sample photo of an inductor on the bottom substrate.
5.2.2 Characterizing Gap Spacing

Determining the gap spacing between the inductor coils accurately is important for high fidelity modeling and characterization. The air gap spacing between the inductors on the substrates is estimated to be 4~7.5 µm based on best case and worst case capacitor measurements across the interface shown in Figure 5.5. Data from the manufacturer indicated a gap spacing of 7.5 µm. Frequency domain measurements were made from 50 MHz to 18 GHz with a HP8510 network analyzer with 100 µm pitch GS probes. Figure 5.6 shows $S_{21}$ for three identical 200 µm diameter capacitor structures labeled SB2_14a, SB2_14b and SB2_14c at different locations on the substrate. The difference in $S_{21}$ values for the same structure repeated at different locations in the substrate implies a deviation in gap spacing with some warpage in the substrate-substrate interface.
Figure 5.6: Measured data for Capacitors 14a, 14b and 14c on substrate SB2

Figure 5.7 shows the electrical models used to match the measured data for the best case and worst case capacitor measurements SB2_14a and SB2_14c. Figures 5.8, 5.9 show the measured vs simulated curves for SB2_14a and SB2_14c. The model correlates well within 1~2 dB deviation between 50 MHz to 18 GHz.
5.7(a) Model for SB2_14a

5.7(b) Model for SB2_14c

Figure 5.7: Electrical models for capacitors SB2_14a and SB2_14c
The electrical model in Figure 5.7 shows 50 fF of through capacitance for structure SB2_14a and 95 fF of through capacitance for structure SB2_14c. Based on these values the air gap spacing is estimated to be 4~7 µm. Figure 5.10 shows eye diagram measurements for
capacitor structure SB2_14c. Time domain measurements were made with an N4901b serial BERT and a Tek11801A oscilloscope.
Results indicate 275 mV pp eye opening at high speeds. Capacitive structures perform well at higher frequencies as expected. As you go higher in frequency the impedance of a through capacitor reduces and becomes closer to a short circuit. However remember that the impedance of a capacitor approaches 50 ohms at only very high frequencies as discussed in chapter 3. It is hard to achieve impedance matching and also sensitivity to gap spacing is high for capacitive structures.
5.2.3 Transformer Characterization

Figure 5.11 shows $S_{21}$ and $S_{11}$ measurements for a 100 µm diameter transformer SB1_11a.

![Graph showing S11 and S21 measurements](image)

**Figure 5.11:** Measured data for a 100 µm diameter transformer (SB1_11a) (with 1.22 nH inductors realized with 5 µm trace width/space) across a gap spacing of 4~7.5 µm.

Figures 5.12(a) and 5.12(b) shows the measured eye diagram for transformer SB1_11a for $2^7$-1 PBRS data at 4.25 Gb/sec and 8.5 Gb/sec with 25 ps edge rates. Time domain measurements were made with an Agilent N4901b serial BERT and a Tek11801A oscilloscope.
(a) Measured data for a 100 µm diameter transformer (SB1_11a) (with 1.22 nH inductors realized with 5 µm trace width/space) across a gap spacing of 4~7.5 µm. (Eye diagram at 4.25 Gb/sec)

(b) Measured data for a 100 µm diameter transformer (SB1_11a) (with 1.22 nH inductors realized with 5 µm trace width/space) across a gap spacing of 4~7.5 µm. (Eye diagram at 8.5 Gb/sec)

Figure 5.12: Measured Eye diagrams
Figure 5.13(a) shows the electrical model for the transformer SB1_11a. Values of magnetic coupling coefficient (K) and inductance in the model were extracted using ASITIC. Shunt capacitive parasitics are very small and make minimal impact on the model since the inductor is on a low loss substrate as opposed to conductive silicon. Also the ground plane is removed in the area immediately surrounding the inductor to reduce shunt capacitive parasitics and to prevent eddy currents. The DC Resistance at port 1 was measured to be 7.5 ohms which correlates closely with 7.6 ohms used in the model. Figure 5.13(b) shows the measured vs. simulated $S_{21}$ and $S_{11}$. Figure 5.14 shows the measured vs. simulated phase. Lossless transmission line models from ADS were used to include the effect of the 50 ohm feedlines from the probe pad to the inductor. The lengths of the feedlines are asymmetric since there are multiple columns of inductor experiments which need to be routed to corresponding probe pads. Note that a simple circuit model provides a broadband match from 50 MHz to 18 GHz for both phase and magnitude information due to the lumped nature of the transformer. The electrical length of this structure is 1.1 mm and approaches $1/10^{th}$ of the operating wavelength at only 17 GHz and hence lumped models would be valid over decades of bandwidth. This would save a lot of simulation time which is needed for full wave EM simulations in commercial connectors.
(a) Lumped circuit model

(b) Measured vs. simulated results for 100 µm diameter transformer (SB1_11a)

Figure 5.13: Measurement and simulation results for transformer SB1_11a
Figure 5.14: Measured vs. simulated $S_{21}$ for SB1_11a (Phase)

Figure 5.15 shows the measured frequency domain data for transformer SB1_11b. Figure 5.16 depicts the measured eye diagram at 1.25 Gbps and 2.5 Gbps respectively.

Figure 5.15: Measured frequency domain data for 100 $\mu$m diameter transformer SB1_11b (with 4.1 nH inductance coils with 5 $\mu$m/5 $\mu$m trace width/space)
(a) Eye diagram at 1.25 Gbps  

(b) Eye diagram at 2.5 Gbps

**Figure 5.16:** Measured Eye diagrams for an 100 µm diameter transformer SB1_11b

Figure 5.17 shows the electrical model for transformer SB1_11b which matched frequency domain data from 50 MHz to 18 GHz. The methodology is similar to the discussion for SB1_11a. The inductors in this transformer are double layer inductors with the inter-layer spacing being ~5 µm. The winding resistance for this structure is larger compared to SB1_11a due to longer electrical length.
Figure 5.17: Electrical model for transformer SB1_11b

Figures 5.18(a), 5.18(b) shows the measured vs. simulated curves from model for SB1_11b.
Figure 5.18: Measured and simulation results for transformer SB1_11b

5.18(a): Measured vs. simulated results for transformer SB1_11b

5.18(b): Measured vs. simulated results for transformer SB1_11b
The return loss characteristics for structures SB1_11a and SB1_11b are poor from measurement because the crossover capacitance between the two inductor coils in this measurement is very small. For example the crossover capacitance is estimated to be 9~15 fF for structure SB1_11a from simple parallel plate formulae. Since the gap spacing is fixed by the solder bump height it is hard to vary the crossover capacitance in measurement. Improving the high frequency return loss for this structure requires a boost in the cross-over capacitance through increasing trace width, reducing gap spacing or increasing dielectric constant without degrading step response of the transformer. Low frequency return loss can be improved through a 50 ohm integrated series terminator on board. The tradeoff in achieving the improved return loss with the 50 ohm discrete termination is more attenuation. In a system application an inductive connector would be used to communicate over 10 cm to 1 m long lines on FR4 and in this case the losses in the line can be used to dampen out the reflections as well. Table 5.1 summarizes measurements on experiments SB1_11a and SB1_11b. We are able to achieve 8.5 Gb/sec signaling with a 100 µm diameter transformer which is built with 1.2 nH inductances and 2.5 Gb/sec signaling with a 100 µm diameter transformer built with 4 nH inductances. The 3 dB bandwidth is fairly high for these structures and this could help in scaling to higher data rates in the future. The goal of these substrate assembly experiments were to determine best case signaling data rate and pitch for transformer interconnect structures in a process accessible to us
Table 5.1: Summary of transformer measurements SB1_11a, SB1_11b

<table>
<thead>
<tr>
<th>Transformer Sample # (100 µm Outer diameter)</th>
<th>Inductance (from ASITIC)</th>
<th>3 dB high pass coupling frequency</th>
<th>3 dB bandwidth</th>
<th>AC coupled eye opening</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB1_11a</td>
<td>1.22 nH</td>
<td>3.6 GHz</td>
<td>15.2 GHz</td>
<td>400 mV pp @ 4.25 Gb/sec</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>200 mV pp @ 8.5 Gb/sec</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>450 mV pp @ 2.5 Gb/sec</td>
</tr>
<tr>
<td>SB1_11b</td>
<td>4.12 nH</td>
<td>947 MHz</td>
<td>8.6 GHz</td>
<td>550 mV pp @ 1.25 Gb/sec</td>
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</table>

Table 5.2 summarizes measurements for all the 4 transformer experiments including the ones which had winding failure. Transformers SB2_7b and SB2_10b were determined to have winding shorts. Visual inspection was not possible after assembly to determine this. The inductance prediction from ASITIC and the inductance extracted from the 3 dB coupling frequency are several orders of magnitude different. In the presence of winding shorts, the adjacent turns merging could effectively look like a larger effective trace width leading to a much smaller inductance. Also the measured DC resistance for transformers SB2_7b and SB2_10b are expected to be 2x~3x times the values for transformers SB1_11a and SB1_11b based on longer winding lengths in the geometry. However, the DC resistance values from the table for SB2_7b, SB2_10b are comparable: (1~1.2 X) relative to SB1_11a, SB1_11b. This indicates winding shorts for these structures.
Table 5.2: Summary of all transformer measurements on SB1 and SB2

<table>
<thead>
<tr>
<th>Transformer Sample</th>
<th>Outer Diameter</th>
<th># of Turns (5 µm W/S)</th>
<th>Inductance (from ASITIC)</th>
<th>f-3 dB (High pass coupling frequency)</th>
<th>Inductance (from f-3 dB)</th>
<th>R_{dc} (DC resistance)</th>
<th>Voltage swing for the “AC coupled Eye” at X Gb/sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB1_11a</td>
<td>100 µm</td>
<td>4</td>
<td>1.22 nH</td>
<td>3.6 GHz</td>
<td>1.1 nH</td>
<td>7.5 Ω</td>
<td>400 mV pp @ 4.25 Gb/sec ; 200 mV pp @ 8.5 Gb/sec</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>SB1_11b</td>
<td>100 µm</td>
<td>4 per layer (2 layers)</td>
<td>4.12 nH</td>
<td>947 MHz</td>
<td>4.2 nH</td>
<td>12.3 Ω</td>
<td>550 mV pp @ 1.25 Gb/sec ; 450 mV pp @ 2.5 Gb/sec</td>
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<tr>
<td>SB2_7b</td>
<td>160 µm</td>
<td>7 per layer (2 layers)</td>
<td>17.05 nH</td>
<td>4.6 GHz</td>
<td>0.86 nH</td>
<td>10.2 Ω</td>
<td>350 mV pp @ 4.25 Gb/sec ; 120 mV pp @ 8.5 Gb/sec</td>
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</tr>
<tr>
<td>SB2_10b</td>
<td>200 µm</td>
<td>9 per layer (2 layers)</td>
<td>32.4 nH</td>
<td>3.14 GHz</td>
<td>1.26 nH</td>
<td>11.9 Ω</td>
<td>450 mV pp @ 4.25 Gb/sec ; 400 mV pp @ 6 Gb/sec</td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>275 mV pp @ 8.5 Gb/sec</td>
</tr>
</tbody>
</table>
5.3 Inductive Socket - System level analysis

This section discusses simulation and analysis for an inductively coupled socket channel similar to Figure 3.2. The modeled S parameters of transformer SB1_11a is used as the transformer model in the simulation. This model was validated with measurement as discussed earlier in the chapter. The feedlines were removed from the model to de-embed the effect of these lines. Impedance matching constraints are different depending on the application of the inductive interconnect structure in a system. For example an inductive socket system such as the one shown in figure 3.2 has only one inductive interconnection in it’s transmission path and it can be terminated on both ends by 50 ohm matched driver and receivers. The main problem here is introduced by PTH via stubs which introduce reflections at high frequencies depending on its length. Figure 5.19 shows block diagram of the simulation setup for the inductive socket system.

Figure 5.19: Block diagram for inductive socket system simulation
The 50 ohm driver and receiver in the simulation are modeled as 50 ohm resistors. The 50 ohm transmission line models are based on physical stackup for an 8.5 mil wide microstrip line on a 5 mil thick FR4 dielectric. The stub models are based on a simple equivalent circuit discussed in Figure 1 [90]. The model is simplistic in the sense that it doesn’t include return current behavior but it is fairly accurate until 10 GHz. Figures 5.20, 5.21 and 5.22 show eye diagrams at the input of the receiver in Figure 5.19 when the stub length varies from 10 mils to 100 mils. The input data is 1000 bits of 5 Gbps PRBS. We assume 50 ps edge rates in our data input stream and this sets the knee frequency of the system at 10 GHz.

![Eye diagram at input of receiver (PTH Via stub length = 10 mils; Eye opening = 350 mV pp)](image_url)

**Figure 5.20:** Eye diagram at input of receiver (PTH Via stub length = 10 mils; Eye opening = 350 mV pp)
Figure 5.21: Eye diagram at input of receiver (PTH Via stub length = 50 mils, Eye opening = 260 mV pp)

Figure 5.22: Eye diagram at input of receiver (PTH Via stub length = 100 mils, Eye opening = 150 mV pp)

When via stub length is 100 mils, eye opening reduces to 150 mV pp as shown in Figure 5.22. At least 200 mV pp eye opening is required for a pulse receiver to recover NRZ data from the pulses. Via stub lengths of 10 mils and 50 mils lead to acceptable eye openings >200 mV pp in Figures 5.20, 5.21. When via stub length is 50 mils, noise floor at center of
eye is ~20 mV and the signal to noise ratio is 16.2 dB. Signal to Noise ratios of 20 dB are desired in typical backplane systems. Via stub length of 10 mils leads to acceptable signal to noise ratio of 24.8 dB. Problems created by long stub lengths are primarily dealt with by routing to minimize stub lengths and by using back drilling to remove the stubs. In an inductive socket system, a 50 ohm series termination is not needed for matching low frequency components since the 50 ohm termination is provided by the driver and receiver. Crossover capacitive tuning by itself helps only in narrow band high frequency impedance matching which may or may not be useful depending on the frequency spectrum of the input data. However we can use some crossover capacitance to boost the signal swing while ensuring overshoot is less than 10% of signal swing. For example a 100 fF crossover capacitance can be added to the transformer model for SB1_11a without degrading step response. Figure 5.23 shows the modified block diagram.

**Figure 5.23:** Modified block diagram with 100 fF crossover capacitance added to transformer model
Figure 5.24 shows the eye diagram at the input of the receiver for the setup in Figure 5.23 with stub length of 10 mils. The addition of the 100 fF crossover capacitance boosts peak to peak signal swing from 360 mV in Figure 5.19 to 400 mV pp in Figure 5.23.

![Eye diagram at input of receiver](image)

**Figure 5.24:** Eye diagram at input of receiver (PTH Via stub length = 10 mils; Eye opening = 400 mV pp)

In an inductive socket system the main goal of transformer design is to achieve multi-Gbps pulse signaling with output signal swing >= 200 mVpp with fine pitch transformers. This can be recovered into NRZ by a pulse CMOS receiver. High frequency impedance matching issues are dealt with primarily by reducing PTH via stub lengths through layout and back drilling. In this section we have shown 5 Gbps signaling through a 100 µm diameter transformer interface when it is plugged in a channel similar to a socket application. Another point to be noted is that while low frequency impedance matching is provided by driver and receiver 50 ohm impedances, it is still important to minimize the magnitude of the backward
traveling reflections in socket channels before they die down at 2\textsuperscript{nd} incidence. A TDR analysis as discussed in chapter 3 should be used to optimize leakage inductance and impedance mismatch at transitions between transmission lines and inductive interconnections.

5.4 Inductive backplane connector – System level analysis

A backplane connector system with 2 transformers communicating across a 30 cm 50 ohm line on FR4 has a lot more attenuation compared to a single transformer socket system. From Table 5.1 in section 5.2, transformer SB1_11b has a higher signal swing at 1x~2x times its 3 dB coupling frequency compared to transformer SB1_11a. The crossover capacitance is very small for this transformer which in turn leads to a poor return loss. The transmission line for a two transformer system sees the input and output 50 ohm driver/receiver load through the transformer which is a short circuit at DC. Here impedance matching is more critical compared to a single transformer system since there is no direct matching through the driver/receiver. Here a 50 ohm series termination is needed to provide impedance matching for the low frequency components. Adding a series termination adds attenuation and it makes sense to use the series termination just to suppress the reflections at 2\textsuperscript{nd} incidence rather than using series terminations on both sides of the transmission line. Improving the return loss over a broad range and compensating for high frequency roll off in insertion loss for structure SB1_11b needs a 50 ohm series termination and a crossover capacitance of ~200 fF. Figure
5.25 shows the insertion and return loss for transformer SB1_11b with an added crossover capacitance of 200 fF and a 50 ohm series termination.

\( \text{(a) Modified transformer model for SB1_11b} \quad \text{(b) } S_{21} \text{ and } S_{11} \text{ in dB} \)

**Figure 5.25:** Frequency response of T2 with 50 ohm series termination and 200 fF crossover capacitance

Figure 5.26 shows block diagram of the simulation setup in ADS for an inductive connector system. The S parameters from validated model for transformer SB1_11b with an added crossover capacitance is used as the transformer model in the simulation. The tradeoff is reduced signaling data rate since the transformer SB1_11b realized with 4.12 nH inductances has a slower decay time. The 50 ohm driver and receiver in the simulation are modeled as 50 ohm resistors. The 50 ohm transmission line models are based on physical stackup for an 8.5 mil wide microstrip line on a 5 mil thick FR4 dielectric. The stub models are based on a simple equivalent circuit discussed in Figure 1 in [90].
Figure 5.26: Block diagram of an inductive connector system in ADS

Figure 5.27 shows the eye diagram at the input of the receiver for the setup in Figure 5.26. The peak to peak signal swing is 200 mV which is sufficient for recovery to NRZ data by a pulse CMOS receiver. The peak magnitude of the double pulse in the AC coupled eye is about 40 mV. The double pulse needs to be dealt with through transmit side wave shaping. However if the magnitude of the double pulse is under a threshold of say ~50 mV which is below sensitivity of most CMOS receivers it could probably be rejected through careful receiver design. Also receiver circuits have been designed to sense similar waveforms before recovering to NRZ.

![Eye diagram with no stubs](image1.png) ![Eye diagram with 50 mil stub](image2.png)

**Figure 5.27:** Eye diagram at 2 Gbps at input of receiver
Figure 5.28 shows the eye diagram at the input of the receiver for the setup shown in Figure 5.26 with no 50 ohm termination and no 200 fF crossover capacitance across the transformer. This eye has 30 mV additional voltage jitter, 30 ps additional timing jitter and 20 mV of additional noise floor at the center of the eye compared to the eye diagram in Figure 5.27(a).

![Eye Diagram](image)

**Figure 5.28:** Eye diagram at 2 Gbps at input of receiver with no stubs (no 50 ohm termination and no $C_c$)

### 5.5 Scaling

This work has shown feasibility for multi-Gbps pulse signaling in inductive connector and socket applications. We used measured data from a 100 µm diameter transformer SB1_11a built with 5 µm width and space across a 4 µm~7.5 µm air gap with 1.2 nH inductance as validation test-structure for the socket application. We performed the demonstration in a
process accessible to us. For a translation to implementation in a real application we should be able to replicate these results in laminate and package processes. In a high end laminate or package process with 25 µm trace width/space and 75 µm microvias a 1.2 nH inductance can be realized in a 275 µm diameter structure with electrical length approaching 1/10\textsuperscript{th} of operating wavelength only over 5 GHz. Crosstalk constraints would drive the spacing between adjacent inductors to be 1/5\textsuperscript{th} of the outer diameter based on measurement in chapter 4. This implies that we can build 330 µm pitch inductive sockets and these can be single ended or even differential. Measured data from 100 µm diameter transformer SB1_11b built with 5 µm width and space with 4.12 nH inductance was used as the validation experiment for the backplane connector application. A 4.12 nH inductance can be realized in a 450 µm diameter structure with 25 µm trace width/space and 75 µm microvias with electrical length approaching 1/10\textsuperscript{th} of operating wavelength only over 5 GHz. Based on the crosstalk constraints we can build 540 µm pitch inductive backplane connectors and these can be single ended or even differential. A point to be noted is that gap spacing between inductive elements is hard to predict precisely as it is heavily dependent on the technology implementation. However it may be hard to achieve gap spacing of the order of 4 µm~7.5 µm in package and laminate processes. The gap spacing is more likely to be around 25 µm. Remember that magnetic coupling is a function of loop area as discussed in chapter 3. As we scale from 100 µm diameter transformers to 275/450 µm diameter transformers the increased magnetic coupling will help in compensating for higher values of gap spacing that might be encountered in real applications. Also remember that in package and laminate processes trace widths are of the order of 25 µm, metal thickness is of the order of 25 µm which implies
much lower ohmic loss compared to inductor structures realized on substrates fabricated by RTI.

Inductive mating experiments were fabricated on ceramic substrates to validate scaling. The experiments had outer diameter ranging from 400 µm to 800 µm. Experimental variations in geometry included winding phase, no. of turns and trace width. In the long term, a high end PCB process will be able to realize 25 µm trace widths and 75 µm microvias. These dimensions were realized in the short-term through test-structures on ceramic substrates. In order to realize 75 µm PTH vias, the substrate thickness of the ceramic samples needs to be as low as 125 µm due to aspect ratio dependence. This also led to some problems with yield. Designs were realized in a 2 metal layer process with gold metallization on ceramic substrates. These designs are fabricated top-down and not bottom-up. Hence yield problems were encountered depending on the size of the substrate and location of the samples on the substrate. One set of mating substrates with 4 transformer experiments and one capacitor experiment yielded and returned from fabrication out of a total of 8 mating samples with 5 experiments each. We discuss results for one sample structure.
Figure 5.29: Test-setup for characterizing 500 µm diameter transformers

Figure 5.29 shows the test frame used for characterization. The bottom substrate was designed to be larger than the top substrate for probing. Alignment marks were included on the substrates to align the inductor coils. A 3-4 µm thick polyimide dielectric layer deposited on top metallization was used as dielectric spacer between the inductor coils. Since the substrate had only 2 layers this made return path and routing line design difficult given the constraints of testing. Probing can only be done on top surface of the substrates. Different configuration of feedlines and ground paths - microstrip and striplines formed between the two assembled substrates were designed in layout based on SONNET simulations. However considering that only 5 designs yielded and returned back from fabrication, testing was done on the sample with only the stripline configuration. Analysis was done on the tested sample. Since the transmission line structures on the substrate did not yield, deembedding the pad, PTH via and feedlines was not possible. The length of the low loss feedlines to the inductor
 coils is ~1 mm. These feedlines would not impact measurements significantly in the frequency band of interest.

**Figure 5.30:** Mask sent to fabrication to ATP thin film products

Figure 5.30 shows the mask sent to fabrication. Another mask with wide set of test-structures was designed for 2\textsuperscript{nd} round of fabrication. However, considering the yield on the first run the 2\textsuperscript{nd} iteration was discarded. Figures 5.31, 5.32 show photos of designs on the ceramic substrates.
Figure 5.31: Photo of samples on ceramic substrates

Figure 5.32: Photo showing wire/epoxy used to hold test-setup and GS probes

Figure 5.33 shows the measured frequency domain data for a 500 μm outer diameter transformer with 2 turns, trace width = 50 μm and inter-turn spacing = 25 μm. The inductance extracted from ASITIC for this structure was 2.2 nH
Figure 5.33: Measured frequency domain data for 500 µm diameter transformer (Trace width/space = 50 µm/25 µm, 2 turns, L = 2.2 nH)

Based on 3 dB high pass coupling frequency of 3.5 GHz for this structure it was expected to work at 3.5~7 Gbps. The S parameter data files were exported into ADS to obtain the eye diagram. Figure 5.34 shows the eye diagram at 4 Gbps.
Figure 5.34: Eye diagram at 4 Gbps for 500 μm diameter transformer characterized on ceramics run

The input voltage in the simulation was 1 V and the edge rate was 50 ps. The peak to peak signal swing is 500 mV. This is promising for socket and backplane connector applications. The electrical length of this structure is fairly small and inductance value is ~2 nH. The results in this chapter demonstrate potential for building electrically small connectors in fine pitch footprints. Signal integrity can be optimized by using integrated series terminations, capacitive tuning and losses on FR4. Figure 5.35 shows comparison of measured frequency domain data in Figure 5.33 with EM simulation from SONNET. As discussed in chapter 4, EM simulation has lower loss compared to the measurement result. However, the EM simulation follows the measurement with similar trends as in chapter 4 though a numerical match was hard.
5.6 Process Variations

When an inductive structure is used in a socket or connector application there could be some variation in gap spacing between the stacked inductors. Also there could be some misalignment between the two inductors stacked on top of each other. These variations could arise in assembly. EM simulations were used to analyze this in chapter 3. This section shows some measured data from the ceramics run experiments. It is hard to vary the gap spacing in measurement since the gap spacing is fixed by the thickness of the polyimide dielectric spacer. Figures 5.36, 5.37 show measured data for a 500 µm diameter transformer when it is aligned well using alignment marks and when the misalignment is 25 µm with respect to the reference.

Figure 5.35: EM simulation in SONNET versus measured data
Figure 5.36: $S_{21}$ for aligned and misaligned experiments

Figure 5.37: $S_{11}$ for aligned and misaligned experiments
The variation in $S_{21}$ is less than or equal to a dB from 50 MHz to 15 GHz. Thereafter there is more variation. However in an application with 50 ps edge rates, the knee frequency is 10 GHz and the spectral content thereafter can be ignored. The variation in $S_{11}$ is less than or equal to a dB until 6 GHz. Thereafter the deviation is between 2~3 dB. These results observed for this transformer sample are very promising. The $S_{11}$ values are still close to -10 dB between 6 GHz to 10 GHz with 25 µm misalignment and a value of -6 dB is sufficient [18]. Simulation and experimental results in this dissertation point to a definite trend. $S_{11}$ is more sensitive than $S_{21}$ to process variations. 3-4 dB variation in $S_{11}$ is acceptable. A 500 µm transformer structure with 50 µm trace widths is representative of a connector realized in a high end laminate process. Tolerance to 25 µm misalignment enforces the point that we can build inductive connectors with acceptable process variations in real world applications.
6 Design Procedure for Inductively Coupled Connectors

6.1 Design Procedure

The objective of this chapter is to summarize a design procedure for inductively coupled connector systems based on experimental and simulation work in this dissertation. Inductive connectors are well suited for custom applications where the operating frequency range and geometrical constraints are well defined. Since design methodology is application specific with several engineering tradeoffs it is more useful to explain with an example rather than generic design guidelines. The design procedure is outlined below. There is some iteration and overlap between these 10 steps in real world design but the intent is to document a well defined sequence of easy to follow steps. Intensive numerical optimization is not the objective of this chapter; rather the goal is to demonstrate a formal design methodology. Section 6.2 shows a design example which uses these principles to design an optimal connector structure for a given application.

1. Define specifications for the application: X Gb/sec signaling, edge Rate, length of 50 ohm transmission line on FR4, gap spacing between inductor coils (and) minimum trace width/space / via size used to build the inductor.

2. Determine Inductance (L) value to achieve X Gb/sec based on simple time domain transformer circuit model simulations which plot output voltage amplitude and decay rates.
3. In practice it is hard to achieve values of $K \geq 0.9$ in fine pitch footprints. The goal is to determine if we can meet attenuation budget of the channel with chosen value of inductance and edge rate with a reasonable value of $K$ taking into account FR4 line losses?. If yes, determine the exact range of $K$ required for achieving acceptable $S_{21}$ or 200 mV pp voltage output. If not, we have to revise the target signaling speed or reduce the channel length we operate over.

4. Determine value of $K$ needed to keep reflection noise due to series leakage inductance under check. Signal to noise ratio of 20 dB is desirable. For example, a series leakage inductance $\leq 0.5$ nH is desired for 50 ps edge rates. Series inductance degrades high speed digital signals with fast edges and the goal is to keep the reflection noise under the threshold for the specified edge rate and signaling speed.

5. Use gap spacing and target pitch to determine range of transformer outer diameters you can use to achieve this value of $K$. For example, an empirical rule derived from simulation in chapter 3 is that a transformer diameter at least 10 times the gap spacing is needed to achieve $K$ of 0.5. Another empirical rule from simulations in chapter 3 is that a relative increase in transformer effective area by a factor of 7.11 provides a boost of 0.15 in $K$. This assumes fixed gap spacing, inter-turn spacing and transformer outer diameter. Transformer effective area is the product of electrical length and trace width.

6. Realize transformer as an electrically short structure with desired value of $L$, $K$. Iterative simulations can be used to optimize transformer geometrical parameters such as trace width, outer diameter precisely. Distributed transformers are not desirable for high speed digital signals with fast edges. Transmission lines are structures with well defined return path with
controlled impedance and hence can be used as interconnects for high speed digital signals. Distributed transformers are not exactly transmission lines with homogeneous return paths and it is hard to tune L-C sections precisely in practice to achieve controlled impedances and predict their values accurately. Since we want fine pitch transformers for high speed digital signaling we should build lumped electrically short structures. Edge rate is used to determine the frequency up to which the structure should look electrically short.

7. One caveat is a designer should be aware if he can actually realize a certain value of K, L in an electrically short structure with a certain value of trace width/space/via size. Otherwise there are iterations involved and assumptions for specifications in step 1 (trace width/space/via size etc.) might need readjusting.

8. Tune the transformer electrical length and trace width to achieve desired value of $C_c$ to compensate for leakage. Overshoots/oscillations places a clear upper bound on how high a $C_c$ we can use (and) edge rate/signaling speed helps in defining the frequency range we want to tune using $C_c$. Simulations with simple lumped circuit models can be used to determine desired value of $C_c$. Use out–of-phase wound transformers along with $C_c$ tuning for optimizing high frequency S parameters.

9. An inductor is electrically a short circuit at DC. Use 20-50 ohms embedded series termination for low frequency impedance matching.

10. In single connector socket systems attenuation budget isn’t much of an issue when the maximum channel length on FR4 is 15 cm. So we should use the smallest inductance in this application. For example, based on experimental work in this research we can use 1 nH.
inductances for 8.5 Gbps signaling in the best case. In two connector backplane systems channel length is of the order of 30 cm to 1 m. In this case we should make engineering tradeoffs to signal at slower data rates ranging from 1 Gbps to 4 Gbps with larger inductances of the order of 3 nH to 5 nH with larger relative pitches compared to the socket application.

### 6.2 Design example – Inductive socket system

Let’s assume that the goal is to achieve 6 Gbps signaling across a representative inductive socket system shown earlier in section 3.1. The edge rate is assumed to be 50 ps. Sub-mm pitch footprints are needed to have a real competitive application for inductive elements. The problem narrows down to building a fine pitch transformer in sub-mm pitch footprints to achieve good signal integrity at 6 Gbps within process constraints. The minimum feature sizes in a high end laminate process are 25 µm trace width/space and 50 µm microvias. The vertical gap spacing between the coils is assumed to be 25 µm in this application.

#### 6.2.1 Determine inductance values

![Figure 6.1: Simulation setup to choose inductance values](image)
Table 6.1: Inductance values (vs.) decay rates: 1V input step voltage

<table>
<thead>
<tr>
<th>L₁ = L₂ = L (nH)</th>
<th>Settling time to 10% of peak voltage (nsec)</th>
<th>Peak Voltage (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.151</td>
<td>290</td>
</tr>
<tr>
<td>2</td>
<td>0.250</td>
<td>367</td>
</tr>
<tr>
<td>3</td>
<td>0.346</td>
<td>410</td>
</tr>
<tr>
<td>4</td>
<td>0.440</td>
<td>431</td>
</tr>
</tbody>
</table>

The first step is to determine the inductance values we can use for 6 Gbps signaling. From the table 6.1 above, the decay time with 1 nH inductance values is 0.150 nsec which sets the maximum signaling data rate at 6.6 Gbs (i.e 1/0.15 = 6.6 Gbs). Hence they can be used for 6 Gbps signaling. Inductance values over 1 nH in table 6.1 have a longer decay time and hence wouldn’t be suitable for 6 Gbps signaling. Output voltage amplitude of at least 200 mV peak to peak or 100 mV single ended is needed at the receiver input in an inductive socket system. We have sufficient margin here with output voltage amplitude of 290 mV to deal with transmission line losses on FR4 in socket applications. We are assuming K of 1 here but even with K of 0.5 we would have sufficient voltage margin. Typical transmission line lengths in inductive socket systems are 4 to 6 inches and conductor loss is about 0.15 dB per inch at 1 GHz on fine line substrates [150]. In this example we are assuming a 15 cm lossy line on FR4 with conductor loss of 0.1 dB per cm at 2 GHz. The transmission line configuration is 8.5 mil wide microstrip on 5 mil thick FR4 substrate.
Equation 2 captures transfer function for a circuit model consisting of ideal coupled inductors in Figure 6.2.

\[ H_{21}(s) = \frac{\sqrt{L_1 L_2} R_L s}{(R_S L_2 + R_L L_1)s + R_S R_L} \]

**Figure 6.2:** Perfectly coupled inductors (T-model; \( L_1\cdot M = L_2\cdot M = 0 \), \( M = K \sqrt{L_1 L_2} \))

**Equation 2: Voltage transfer function for the model in Figure 6.2**

To a first order the transfer function in equation 2 can be used to plot step response and gain insights on filtering behaviour and decay rates. For example, the transfer function in equation 2 indicates a pole at \( s = -\frac{R_S R_L}{R_S L_2 + R_L L_1} \). As the value of inductance increases the pole frequency reduces which indicates a lower 3 dB coupling frequency, more low frequency content and hence a longer settling time for step response. When the value of inductance is very small the pole frequency is higher which indicates a higher 3 dB coupling frequency, less low frequency content and hence a smaller settling time for step response.
6.2.2 Determine acceptable range of magnetic coupling coefficient (K)

Achieving high $S_{21}$ bandwidth and return loss values better than -10 dB needs values of magnetic coupling coefficient as close to 1 as possible. But achieving high values of $K$ (>=0.9) requires transformers of larger outer diameter which conflicts with the goal of building fine pitch footprints. The goal hence is to determine values of $K$ which would meet acceptable requirements for $S_{21}$ without degrading $S_{11}$ significantly due to leakage inductance.

The model is shown in Figure 6.3. A simulation of this model in Figure 6.4 shows that with a $K$ of 0.5 we can achieve sufficient output voltage amplitude of 105 mV (i.e 210 mVpp) in an inductive socket system to communicate across a 15 cm lossy line on FR4. The objective is to obtain 200 mV peak to peak amplitude; for recovery to NRZ data by a pulse receiver. It is also important to keep noise levels low and achieve a signal to noise ratio of at least 20 dB. The transmission line model is based on an 8.5 mil wide microstrip line on a 5 mil thick FR4 substrate. In laminates with thick copper metallization, DC resistance values are typically small and were of the order of a few ohms for structures characterized in this work. Hence DC resistance is assumed to be 1 ohm in Figure 6.3.
Figure 6.3: A simplified inductive socket system (without stubs)

Figure 6.4: Output voltage at node “out” in Figure 6.2

$S_{11}$ optimization needs series resistance, crossover capacitance tuning and leakage inductance control.
From the T-circuit model shown in Figure 6.5, series leakage inductance in a transformer is $L_{1-M}$. Series inductance degrades impedance matching and the goal of transformer design is to minimize series inductance which leads to degradation of high speed digital signals with fast edge rates. Figure 6.6 and Figure 6.7 show simulation set up and step response with reflections superimposed to study effect of series inductance on a 50 ps rising edge.
Figure 6.7: Reflection due to series inductance at node “in1” in Figure 6.5

Figure 6.7 shows that reflected waveform amplitude superimposed on the 0.5 V step increases from 29 mV to 150 mV as series inductance changes from 0.25 nH to 2 nH. Table 6.2 shows peak reflection noise as a function of edge rate and leakage inductance. To keep reflected noise within 10% of the 0.5 V output step voltage, series inductance should be less than or equal to 0.5 nH at 50 ps edge rate and less than or equal to 1 nH at 100 ps edge rates. At slower edge rates high frequency content is lower and hence the requirements on leakage inductance control to mitigate reflection noise are lower compared to faster edge rates. In the design example shown in this chapter edge rate is 50 ps and hence the goal is to control leakage inductance to less than or equal to 0.5 nH.
### Table 6.2: Reflection noise vs leakage inductance vs edge rate

<table>
<thead>
<tr>
<th>Edge rate (ps)</th>
<th>Leakage inductance(nH)</th>
<th>Peak reflection noise (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 ps</td>
<td>0.25 nH</td>
<td>25 mV</td>
</tr>
<tr>
<td>50 ps</td>
<td>0.5 nH</td>
<td>50 mV</td>
</tr>
<tr>
<td>50 ps</td>
<td>0.75 nH</td>
<td>74 mV</td>
</tr>
<tr>
<td>50 ps</td>
<td>1 nH</td>
<td>99.3 mV</td>
</tr>
<tr>
<td>50 ps</td>
<td>1.5 nH</td>
<td>143.5 mV</td>
</tr>
<tr>
<td>50 ps</td>
<td>2 nH</td>
<td>180 mV</td>
</tr>
<tr>
<td>100 ps</td>
<td>0.25 nH</td>
<td>12.3 mV</td>
</tr>
<tr>
<td>100 ps</td>
<td>0.5 nH</td>
<td>25 mV</td>
</tr>
<tr>
<td>100 ps</td>
<td>0.75 nH</td>
<td>37.3 mV</td>
</tr>
<tr>
<td>100 ps</td>
<td>1 nH</td>
<td>49.9 mV</td>
</tr>
<tr>
<td>100 ps</td>
<td>1.5 nH</td>
<td>74.8 mV</td>
</tr>
<tr>
<td>100 ps</td>
<td>2 nH</td>
<td>99.3 mV</td>
</tr>
</tbody>
</table>

A transformer model has both series and shunt inductances in a T-configuration as shown in Figure 6.5 and the effective equivalent series inductance is different from $L_1-M$. However it is
the series inductance in the T model which is the primary contributor to high frequency discontinuities in a transformer. The shunt inductance is used to achieve 50 ohm impedance at high frequencies in an ideal transformer. As a first pass rule of thumb we can choose values of L,K which keep the series inductance element in the T-Model $\leq 0.5 \text{nH}$. With 1 nH inductances, K should be $\geq 0.5$ to keep series leakage inductance in the T model $\leq 0.5 \text{nH}$. Figure 6.9 shows TDR Z plot obtained using ADS simulation for a circuit model with 1 nH inductors, K=0.5 as shown in Figure 6.8. The positive spike in Figure 6.9 corresponding to a series inductance element contributes to a variation of 4 ohms in the Z profile. The reflection coefficient in this case can be computed using $\tau = \frac{Z_L - Z_0}{Z_L + Z_0}$. Assuming $Z_L$ of 54 ohms and $Z_0$ of 50 ohms the reflection coefficient is 0.038 which results in a return loss of $-20\log(\varsigma) = -28.2 \text{ dB}$ which is acceptable in this application as discussed in chapter 3.

Figure 6.8: Circuit model with 1 nH inductors; $K = 0.5$, $R_{dc} = 1 \text{ ohms}$
We have established in this section that a $K \geq 0.5$ is desired in this system to achieve acceptable $S_{21}$ while keeping leakage inductance under control.

Table 6.2 shows how leakage inductance changes with $K$ and $L$ for a 500 µm outer diameter transformer simulated with ASITIC. Trace width and inter turn spacing was set to 25 µm in all cases and the number of turns were varied. There is a basic tradeoff here. Structures with larger inductance (and thus lower operating frequency) have better coupling coefficients. But they also have higher series leakage inductance when realized in a similar geometry compared to smaller inductance structures which in turn leads to increased reflections. This is a strong reason to use smallest inductance possible for an application with a certain target signaling speed. Leakage inductance can be controlled through a combination of the right choice of inductance and $K$. 

![Figure 6.9: Z profile plot for model in Figure 6.7](image-url)
Table 6.3: Sample calculations (500 µm diameter transformer with fixed gap spacing between the coils)

<table>
<thead>
<tr>
<th># of Turns</th>
<th>K (from ASITIC)</th>
<th>Inductance(from ASITIC)</th>
<th>Leakage inductance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.58</td>
<td>1.37 nH</td>
<td>0.58 nH</td>
</tr>
<tr>
<td>2</td>
<td>0.65</td>
<td>3.38 nH</td>
<td>1.19 nH</td>
</tr>
<tr>
<td>3</td>
<td>0.67</td>
<td>5.13 nH</td>
<td>1.7 nH</td>
</tr>
<tr>
<td>4</td>
<td>0.68</td>
<td>6.2 nH</td>
<td>1.99 nH</td>
</tr>
</tbody>
</table>

Equation 3 shows transfer function for a transformer model with leakage shown in Figure 6.5. This can be used as a first order method to determine acceptable values of K by plotting transient response.

\[
H_{21}(s) = \frac{MR_L s}{(L_1 L_2 - M^2)s^2 + (R_S L_2 + R_L L_1)s + R_S R_L}
\]

**Equation 3: Voltage transfer function for transformer model in Figure 6.5**

Finite leakage introduces an additional pole in the response proportional to the term \((L_1 L_2 - M^2)\). This is a measure of leakage inductance in the transformer. The band pass nature of the frequency response arises due to this leakage inductance factor in the denominator of the transfer function. This effect shows up in step response as smaller peak amplitude and
filtering of the sharp rising edges in the pulse waveform. This simplified voltage transfer function (which doesn’t include the capacitance effects) provides insights on optimizing the amplitude and band pass frequency response of the transformer but doesn’t provide obvious clues on reflection control. The insertion loss in the transformer introduced by imperfect coupling produces a low Q wide bandwidth network. Since $S_{21}$ reduces, return loss degrades to satisfy power conservation laws. This is under the assumption that there are no radiation effects into free space because of the inductor acting as an antenna. Radiation effects exist for electrically large inductors on printed circuit boards and are not a concern for electrically short designs discussed in this chapter. This transfer function in equation 3 should be plugged in a TDR simulation setup to analyze magnitude of backward travelling reflected waves. The end objective is to determine a value of $K$ which produces 200 mV peak to peak output voltage in the system and achieves reflection noise less than or equal to $1/10^{th}$ of the signal amplitude.

6.2.3 Transformer geometry implementation – $K$, $L$, outer diameter, trace width

Distributed transformer structures introduce complexity from impedance matching perspective for broadband digital signals and are hard to model accurately. The transformer structure used as a connector should be a lumped element. With a 50 ps edge there is frequency content until 10 GHz. If the electrical length of the structure is within $1/7^{th}$ to $1/10^{th}$ of the operating wavelength we can build a connector which looks electrically short until at least 10 GHz. This sets the electrical length range between 1.5 mm to 2.1 mm for the
transformer structures. The goal is to synthesize lumped transformer geometry with maximum K possible across a 25 µm air gap with <= 1 mm pitch. The minimum acceptable K is 0.5 and inductance value required is 1 nH. Based on simulations with ASITIC in chapter 3, a transformer outer diameter latest 10 times the gap spacing is needed to achieve a K of 0.5. The minimum usable transformer diameter is 250 µm in this example since the gap spacing assumption in this application is 25 µm. Crosstalk rules limit spacing between 2 inductor coils to one fifth of the coil outer diameter. So the largest possible transformer we can use is of 833 µm outer diameter to stay within 1 mm pitch target. Table 6.3 lists various transformer geometrical implementations to realize 1nH inductance values with K>=0.5 across a 25 µm gap spacing

Table 6.4: Transformers with 1 nH inductance to achieve K >= 0.5; 25 µm gap spacing

<table>
<thead>
<tr>
<th>Outer diameter (D in µm)</th>
<th>W, S (µm)</th>
<th># of turns</th>
<th>K</th>
<th>Electrical length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>260</td>
<td>25,25</td>
<td>2</td>
<td>0.54</td>
<td>1580</td>
</tr>
<tr>
<td>490</td>
<td>50,25</td>
<td>1</td>
<td>0.66</td>
<td>1885</td>
</tr>
<tr>
<td>700</td>
<td>125,25</td>
<td>1</td>
<td>0.79</td>
<td>2650</td>
</tr>
<tr>
<td>830</td>
<td>185,25</td>
<td>1</td>
<td>0.83</td>
<td>3110</td>
</tr>
</tbody>
</table>

Larger transformer outer diameters contribute to higher K, so the goal is to pick the largest transformer we can use for the application while staying within pitch targets and 2.1 mm
electrical length. From table 6.3 above the 490 µm diameter transformer meets this constraint. Realizing a 1 nH inductance in a transformer outer diameter of 490 µm needs trace widths ~50 µm assuming the inter-turn spacing is held constant at 25 µm in all cases. Wider trace widths help in boosting K as shown through simulations in chapter 3 and is optimized through iterative simulations with ASITIC. An empirical rule from chapter 3 that can be used as guideline is that K increases by 0.15 when relative effective area of the inductor coils increases by a factor of 7.11. This assumes fixed gap spacing, outer diameter and inter-turn spacing.

6.2.4 Transformer geometry – Cc tuning

We can achieve a K of 0.66 with 490 µm diameter transformers as shown in table 6.3. Figure 6.10 shows a simple circuit model with 1 nH inductors and K =0.66 to determine desired value of Cc for tuning frequency response. The winding phase is assumed to be out of phase since it is has been established to offer bandwidth extension benefits.
Figure 6.10: Circuit model to study $C_c$ tuning

From design principles in chapter 3, opposite winding phase, $C_c$ tuning and series termination is needed to optimize $S_{21}/S_{11}$. We have to determine value of $C_c$ needed to compensate for leakage and tune $S_{21}/S_{11}$. First step is to determine the upper limit on the value of $C_c$ we can use for tuning frequency response. High $C_c$ values lead to overshoots/oscillations in the step response due to the system response becoming underdamped. From Figure 6.11 below with $C_c = 200$ fF the ringing is at a value of 25 mV which is $1/10^{th}$ of the voltage swing. This is the tolerable upper limit for noise. With $C_c = 200$ fF, the signal to noise ratio is 20 dB. Hence we should build a transformer with $C_c \leq 200$ fF. The 2$^{nd}$ step is to determine what is the best value of $C_c$ to use in the range $0 < C_c \leq 200$ fF for tuning return loss.
Figure 6.11: Step response to determine effect of $C_c$

Figure 6.12: $S_{11}$ for different values of $C_c$

Figure 6.12 shows with $C_c = 100$ fF $S_{11}$ is better than -10 dB from 12 GHz onwards. With 6 Gbps signaling speeds and 50 ps edge rates impedance matching is desired from DC to 10
GHz. $C_c = 100 \, \text{fF}$ doesn’t help with impedance matching until 12 GHz, hence we need a higher crossover capacitance value. With $C_c = 150 \, \text{fF}$, $S_{11} \geq -10 \, \text{dB}$ is achieved from 7 GHz to 20 GHz. However the spectral content is very low at frequencies above 10 GHz with a 50 ps edge as discussed in chapter 3. We care only about impedance matching until 10 GHz and it is more desirable to obtain better $S_{11}$ at frequencies less than 7 GHz as well since a 6 Gbps signal has a fundamental at 3 GHz. With $C_c = 200 \, \text{fF}$, $S_{11} \geq -10 \, \text{dB}$ is obtained from 6 GHz to 10 GHz and is optimal from an impedance matching perspective. Equation 4 shows voltage transfer function for a simple transformer model to capture effect of $C_c$. This was discussed in detail in section 3.3.2.6 and is briefly summarized here. Pole/zero plots from this transfer function can be used to optimize $C_c$ for desired frequency response and time domain response. This analysis can be used by the designer to tune crossover capacitance for the system.

$$H_{21}(s) = \frac{((L_1 L_2 - M^2) C_c s^2 - M)R_L s}{A C_c s^3 + (L_1 L_2 - M^2 + BC_c) s^2 + (R_s L_2 + R_L L_I) s + R_s R_L}$$

$$A = (L_1 L_2 - M^2) (R_s + R_L); \quad B = (L_1 + L_2 + 2M)R_s R_L$$

**Equation 4: Voltage transfer function to capture the effect of $C_c$ (Source Resistance – $R_s$, Load termination - $R_L$.)**

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Table 6.4 shows the transformer geometry implementation derived from the structure in table 6.1 to achieve $C_c = 200 \text{ fF}$. An increase in trace width from 50 µm to 67 µm and increase in transformer outer diameter from 490 µm to 550 µm is needed here to achieve a $C_c$ of 200 fF. The crossover capacitance can be adjusted to 200 fF using the expression for parallel plate capacitance: $[C_c = (\text{Electrical length}) \ast (\text{Trace width}) \ast \epsilon_0 \ast \epsilon_r / \text{(Gap spacing)}]$. The electrical length and trace width are varied to achieve the desired value. We have to ensure staying within an electrical length of 2.1 mm to keep the structure lumped and achieving an inductance of 1 nH with the chosen trace width/electrical length.

Table 6.5: Transformer geometry with 1 nH inductance, $K \geq 0.5$, $C_c$ varied from 133 fF to 200 fF (ASITIC simulation)

<table>
<thead>
<tr>
<th>Outer Dia (D in µm)</th>
<th>W/S (in µm)</th>
<th>L(nH)</th>
<th>Electrical length (µm)</th>
<th>$C_c$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>490</td>
<td>50/25µm</td>
<td>1.01nH</td>
<td>1885</td>
<td>133fF</td>
</tr>
<tr>
<td>550</td>
<td>67/25</td>
<td>1.04nH</td>
<td>2110</td>
<td>200.1fF</td>
</tr>
</tbody>
</table>

In table 6.5 the structure with 550 µm outer diameter with 67 µm trace width achieves $C$ of 200 fF. Since the outer diameter is larger than 490 µm it also contributes to a boost in $K$ from 0.66 to 0.71 (not shown in table above). In summary the transformer geometry can be determined from knowledge of: gap spacing, dielectric constant ($\epsilon_r$), target pitch for the application, electrical length requirements to keep the structure lumped, minimum
acceptable K for the system, desired inductance value and desired value of $C_c$ to tune system performance.

### 6.2.6 Series termination Optimization

The intent of this section is to provide a guideline on choice of series terminations rather than a numerical result. Optimization of series termination requires intensive numerical simulation on a case by case basis and transfer function analysis as well. $C_c$ optimization address the high frequency impedance matching problem while matching from DC to 6 GHz can be achieved with series terminations in the range of 10 to 50 ohms. The choice of value of series termination is an engineering tradeoff between signal amplitude attenuation due to series resistance and reflected noise control. Figure 6.13 shows simulation setup to plot step response to a 50 ps edge to study tradeoffs in choice of series termination. An ideal transmission line was used in this setup to understand reflection noise improvements obtained using the series resistance without line losses decaying the reflections. At the driver end a source resistance of 30 ohms was assumed to introduce a deliberate source of back and forth reflections.
Table 6.6 captures voltage at node “out” and signal to noise ratio at the node “out” when the series termination $R$ in Figure 6.12 is varied from 12.5 ohms to 50 ohms. The input voltage is 1 V in this simulation setup.
Table 6.6: Series termination sweep ($V_{out}$ – Forward voltage transfer; Edge rate = 50 ps)

<table>
<thead>
<tr>
<th>$R_{series}$ (ohms)</th>
<th>$V_{out}$ (mV)</th>
<th>Peak Reflection Noise (+ve or –ve) (mV)</th>
<th>SNR ratio at output (in dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.5 ohms</td>
<td>300.9 mV</td>
<td>31.39 mV</td>
<td>19.63 dB</td>
</tr>
<tr>
<td>25 ohms</td>
<td>263.6 mV</td>
<td>17.6 mV</td>
<td>23.5 dB</td>
</tr>
<tr>
<td>37.5 ohms</td>
<td>233.3 mV</td>
<td>16.99 mV</td>
<td>22.75 dB</td>
</tr>
<tr>
<td>50 ohms</td>
<td>208.4 mV</td>
<td>17.67 mV</td>
<td>21.43 dB</td>
</tr>
</tbody>
</table>

When the series termination is at a mid range value of 25 ohms the signal to noise ratio is better than at other end range values of series resistance and equal to 23.5 dB. While the optimal value of series termination is dependent on the specific passive channel, the essence of this discussion is that the best choice is intermediate between 0 ohms to 50 ohms to achieve desired signal swing with minimal reflections.

Equation 4 can be used to gain insightful understanding of impact of source and load terminations on transformer frequency response and step response. For example as discussed
in chapter 3, the transfer function in equation 4 indicates that source terminations impact only system poles while load terminations impact system poles and zeros. Hence reflection control needs optimization of load terminations. However, system constraints in a backplane system such as receiver design limit the freedom in tuning the load termination as desired. An important point to remember is that in a backplane channel series termination acts as load for backward traveling waves after 1\textsuperscript{st} incidence and this value can be optimized to suppress reflections at 2\textsuperscript{nd} incidence. For first incidence the series resistor still helps by making the system a lossy wide bandwidth low Q network which is desired in digital systems.

![Series terminations acting as load in an inductive socket system](image)

**Figure 6.14:** Series terminations acting as load in an inductive socket system

Figure 6.14 shows series termination in an inductive socket system. The series termination and load terminations act interchangeably as source and load terminations depending on the direction of wave propagation. The transformer (i.e. connector) sees an effective load impedance R-load for the forward travelling wave and an effective load impedance given by the combination of series termination, transmission line and driver impedance for the backward travelling wave. Sometimes system constraints dictate the value of load impedance
and it is useful to have more degrees of freedom in controlling reflections by adjusting source and load terminations for forward and backward travelling waves. Another key point is that in a single connector system, the driver impedance is already close to 50 ohms and the series termination only provides marginal help for reflection control in a 50 ohm system and it doesn’t help much in compensating for non-idealities created by capacitive parasitics at the driver end. On the other hand in two transformer systems discussed in this dissertation the 2\textsuperscript{nd} transformer at the driver end is a short circuit at low frequencies and hence the effective impedance looking into the driver is a short circuit. In this case series termination helps significantly in impedance matching and reflection control for the low frequency components. The precise value of series termination desired can be determined by using the transfer function in equation 4 in a system level simulation and capturing signal to noise ratio for different cases.

### 6.2.7 Optimal transformer geometry for this example

![Equivalent circuit model](image)

**Figure 6.15:** Equivalent circuit model
Figure 6.15 shows the transformer equivalent circuit model for the transformer geometry to achieve 6 Gbps signaling across a 6” inductive socket system. These model parameters can be achieved with a transformer of 550 µm outer diameter, 67 µm trace width, 25 µm inter-turn spacing and 1 turn as outlined in table 6.4. Resistance of the inductor coil is ignored in the model here since it is order of 1-2 ohms in laminates with thick copper metallization. A 25 ohm embedded series resistor can be used or in the long term this value of resistance can be integrated in the inductor coil with advanced processing feature sizes on laminates. Shunt Capacitive parasitics can be controlled to values <50 fF through return path spacing as outlined in chapter 3 and are hence ignored in this model. Figure 6.16 shows S parameters for the model in Figure 6.15.

Figure 6.16: S parameters for the optimal model in Figure 6.12

A transformer used as a connector should be an electrically short device used as a high speed signal transfer mechanism. Inductance values should be sufficient to achieve X Gb/sec signaling. K should be optimized to keep leakage inductance as small as possible for high
speed signaling applications and $C_c$ should be used to compensate for effects of leakage at high frequencies. The winding phase should be out of phase. Series resistance is used to achieve low frequency impedance matching.
7 Conclusions and Future Work

7.1 Conclusions

Inductively coupled interconnect structures have been evaluated for level 2 and level 3 interconnections. A transformer used as a connector should be an electrically short device used as a high speed signal transfer mechanism. Distributed transformers are not desirable for high speed digital signals with fast edges. Transmission lines are structures with well defined return path with controlled impedance and hence can be used as interconnects for high speed digital signals. Distributed Transformers are not exactly transmission lines with homogeneous return paths and it is hard to tune L-C sections precisely in practice to achieve controlled impedances and predict their values accurately. Since we want fine pitch transformers for high speed digital signaling we should build lumped electrically short structures. Edge rate is used to determine the frequency up to which the structure should look electrically short. For example, with a 50 ps edge there is frequency content until 10 GHz. If the electrical length of the structure is within 1/7\textsuperscript{th} to 1/10\textsuperscript{th} of the operating wavelength at this frequency we can build a connector which looks electrically short until at least 10 GHz. This sets the electrical length range between 1.5 mm to 2.1 mm for the transformer structures at this edge rate. The key point here is that essentially the design space for the designer is now narrowed down to a finite sample space. The goal is to find the best transformer geometry within this window to meet performance specifications for an application
Once the desired electrical length is determined for the transformer the goal is to first determine the ideal electrical model parameters desired for this physical transformer. The first step is to compute value of inductance required for X Gb/sec signaling. As discussed in the design procedure chapter it is important to remember that value of inductance chosen should be as small as possible to keep leakage inductance under control. The upper threshold on tolerable leakage inductance in a system can be determined from simple time domain simulations as a function of edge rate as discussed in chapter 6. Leakage inductance contributes directly to reflection noise in an inductive connector system and the goal of transformer design in the connector application fundamentally is to negate the impact of leakage inductance on system performance. Leakage inductance depends on magnetic coupling coefficient and inductance and both of them have to be optimized to keep leakage inductance under a certain threshold for a given edge rate. Acceptable value of magnetic coupling coefficient is also constrained by attenuation budget of the system. Once a range is identified for acceptable magnetic coupling coefficient (K), transformer geometry within a certain desired electrical length can be synthesized to achieve desired inductance and magnetic coupling coefficient. Empirical rules summarized in this dissertation from simple ASITIC simulations and measured data can be used to synthesize a appropriate transformer geometry to achieve a desired K. K depends predominantly on the transformer outer diameter and gap spacing and empirical observations can used for a quick first pass choice of transformer geometry with more optimization thereafter with CAD tools.
There are fundamental limits on achievable magnetic coupling coefficient (K) because of finite gap spacing and fine pitch constraints on transformer geometry. Crossover capacitance inherent in the physical implementation of a stacked transformer can be used to compensate for imperfect magnetic coupling and optimize reflection noise at high frequencies. The trace width in the transformer geometry implementation should be adjusted in combination with transformer outer diameter to achieve desired value of crossover capacitance. Simple parallel plate equations can be used to compute crossover capacitance. It is also important to use out of phase wound transformers to capitalize on the benefits of crossover capacitance as discussed in chapter 3. Since an inductor is a short at low frequencies, embedded series termination is essential for low frequency impedance matching in inductive connector systems. Exact numerical value and placement of series terminations in the channel also impacts how beneficial it is as discussed in chapter 6. For example, series termination is more beneficial for reflection noise control for the backward traveling wave in a backplane connector system. Hence, it has more impact on reflection noise control in an inductive 2 connector system which has significant low frequency discontinuities at both ends compared to a single connector inductive system which is more likely to have to better low frequency impedance match at the driver end.

Voltage transfer functions presented in chapter 3 and chapter 6 should be used by the designer to optimize the various transformer model parameters: inductance (L), magnetic coupling coefficient (K), crossover capacitance (C_c) and series termination. As discussed in chapter 3, return path proximity in layout can be used to control parasitic capacitance to
negligible values in the inductive connector application. S parameter equations derived from first principles using ABCD chain parameter computations for transformer models are unwieldy. This makes it hard for the designer to gain an intuitive understanding of channel optimization. In this respect the voltage transfer function is more useful. Nevertheless S parameters are a valuable source of guidance early on in the design process to help the designer identify potential sources of discontinuity and problem spots in the frequency domain. Once this is accomplished it is more informative to look at transfer functions and step response. The key objective in inductive connector system design is to optimize the Signal to Noise ratio. A typical requirement for a pulse receiver circuit is 200 mV peak to peak input signal with SNR ratio better than 20 dB for recovery to NRZ. There are different sources of noise in a system but the main goal is to use the voltage transfer functions to optimize magnitude of forward signal transmitted in the system and minimize reflection noise to achieve SNR ratio >= 20 dB. From transfer function analysis, using step response and pole zero plots the transformer circuit model parameters can be optimized to achieve desired performance corresponding to a certain signaling data rate, edge rate within process constraints for a certain application. A design procedure has been outlined in this dissertation for the designer to employ to achieve best case results in inductive connector design for the desired application.

Multi Gbps pulse signaling is demonstrated with sub-mm pitch inductive connector prototypes. All design concepts have been validated with measurement data. A simplified modeling method is presented for fine pitch inductive structures and has been validated with
measurement. One of the biggest impediments to successful realization of a technology is lack of model to hardware correlation and lack of wide sample space of experimental data to cover a wide variety of possibilities. This dissertation addresses this with a huge volume of measurement data and analysis in chapter 4 and chapter 5. This empowers the designer to translate a high performance predictable inductive connector design from concept to realization in quick time.

Single transformer socket systems can operate at higher speeds up to 8.5 Gbps while the attenuation in two transformer backplane connector system leads to lower signaling data rates of the order of 1 to 4 Gbps. Two transformer systems need novel equalization schemes while single transformer systems can work with little or no equalization. Novel Pulse receiver circuits have to be used to recover 200 mV pp pulse at the receiver input to NRZ data. The connector demos in this dissertation have been accomplished with realistic process constraints encountered in laminate applications. We have hence demonstrated that ZIF sub-mm pitch surface mount inductive connector technology can be a viable option in the near future. This technology can address some of the inherent problems with signal integrity in press fit connector technology. Inductive connectors are better suited in custom applications where the air gap spacing, process feature sizes, and operating frequency range are well known. Process variations is an important issue to be mindful of when designing inductive connectors for real world applications and impedance variations should be within +/-10% of the target specification. $S_{11}$ is found to be more sensitive to process variations compared to $S_{21}$, but the variations in $S_{11}$ can be controlled to within 3-4 dB variation as observed in
measurements. Hence we can build inductive connectors with good performance repeatability in a real world manufacturing process.

7.2 Future work

As the inductor dimensions required for high density AC coupled interconnect application keeps scaling downwards, emphasis moves away from microwave design more to the circuits and signaling aspect of things. Some areas to investigate on the transformer design include integrating the 50 ohm series resistance as part of the inductor coil using thin metallization copper on laminates or other materials. Using ferromagnetics to boost magnetic coupling at GHz range frequencies is promising, but needs further research thrust. On the signaling side novel equalization techniques for 2 transformer systems is a topic worth investigating. The double pulse effect can be negated through transmit side waveshaping. Building novel circuitry to achieve this with optimized area and power dissipation is useful. Also narrowband signaling schemes like raised cosine signaling could be useful in addressing reflections in inductively coupled systems. Raised cosine signals have spectral content in a much narrower band compared to a broadband NRZ digital signal. Driver circuits which can implement such signaling schemes would be promising.
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