ABSTRACT

LIU, YU. Advanced Modulation, Control and Application for Multilevel Inverters. (Under the direction of Alex Huang.)

The purpose of the research has been to develop advanced modulation, control and application for multilevel inverters. A new series of modulations has been proposed to achieve minimal THD (Total Harmonic Distortion) for multilevel inverters. The first minimal THD modulation is a real-time algorithm used to calculate optimal values of switching angles for given DC voltages and a modulation index. The second one is an algorithm used to calculate optimal values of DC voltages and switching angles for a given modulation index. The third one used an algorithm to calculate optimal values of DC voltages, switching angles and a modulation index. Another new optimal combination modulation strategy has been proposed for the 10 MVA 5-level cascade multilevel inverter based STATCOM (Static Synchronous Compensator) system. In this thesis, I also proposed several advanced controls for cascade multilevel inverters to be used in STATCOM applications. A new feedback control strategy for balancing individual DC capacitor voltages is proposed. The key part of the control strategy is a compensator used to cancel the variable parts in the model. I have also proposed the solutions for enhancing ride-through capability of the STATCOM during faults conditions.

Advanced Modulation, Control and Application for Multilevel Inverters

by
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DEDICATION

To My Wife Xiaoxue

and

My Parents Shixian & Delian

BIOGRAPHY

Yu Liu was born in Anhui, China. He received the B.E. degree and the M.E. degree in electrical engineering from Zhejiang University, China, in 1998 and 2002, respectively. He is completing the Ph.D. degree in North Carolina State University, Raleigh, North Carolina.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1. Introduction

1.1 Inverters in power electronics

Power electronics is very important in modern technology and is now used in a great variety of products [1, 2], including heat controls, light controls, motor controls, power supplies, vehicle propulsion systems, Flexible AC Transmission Systems (FACTS) and High-Voltage DC (HVDC) systems. The power electronics circuits can be classified into six categories: (i) diode rectifiers; (ii) AC-DC converters (controlled rectifiers); (iii) AC-AC converters (AC voltage controllers); (iv) DC-DC converters (DC choppers); (v) DC-AC converters (inverters) and (vi) static converters [2].

A DC-AC converter is also known as an inverter. The function of an inverter is to produce an AC voltage /current, with controlled magnitude and frequency. Figure 1.1 is a conceptual block diagram of a DC/AC inverter. The DC voltage source of the inverter can be either a controlled/uncontrolled rectifier or batteries. A typical three-phase inverter is shown in Figure 1.2.

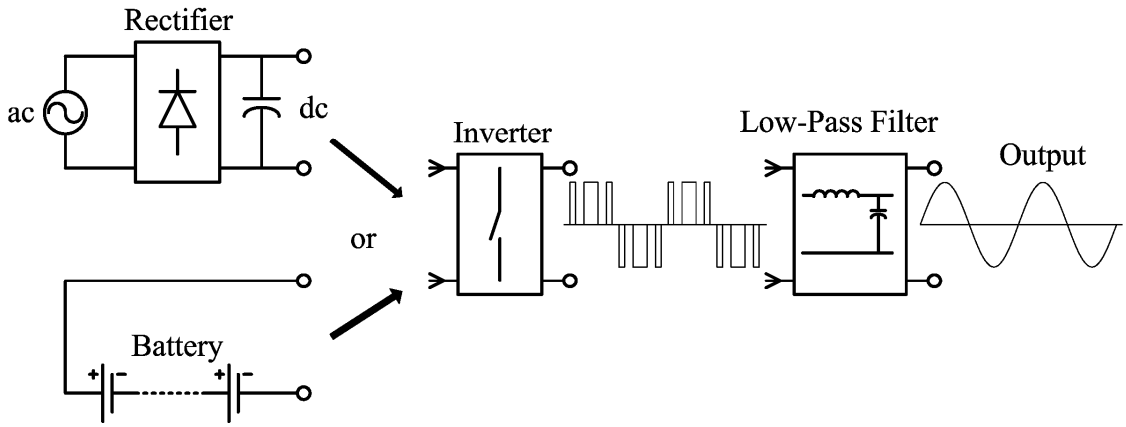


Figure 1.1. Block diagram of a DC/AC inverter

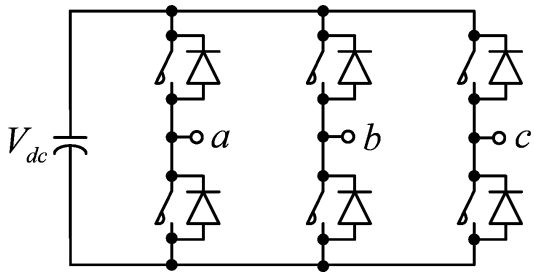


Figure 1.2. Three-phase inverter

1.2 Introduction to multilevel inverters

Multilevel inverters contain several power semiconductors and capacitor voltage sources. Output voltages of multilevel inverters include the additions of the capacitor voltages due to the commutation of the switches. Figure 1.3 shows a schematic diagram of one phase leg of inverters with several numbers of levels. The action of power semiconductors is represented by an ideal switch with several actions. A two-

level inverter, as shown in Figure 1.3 (a), generates an output voltage of two levels with respect to the negative terminal of the capacitor, while the three-level inverter shown in Figure 1.3 (b) generates three voltages, and so on. Thus, the output voltages of multilevel inverters have several levels. Moreover, they can reach high voltage, while the power semiconductors must withstand only reduced voltages.

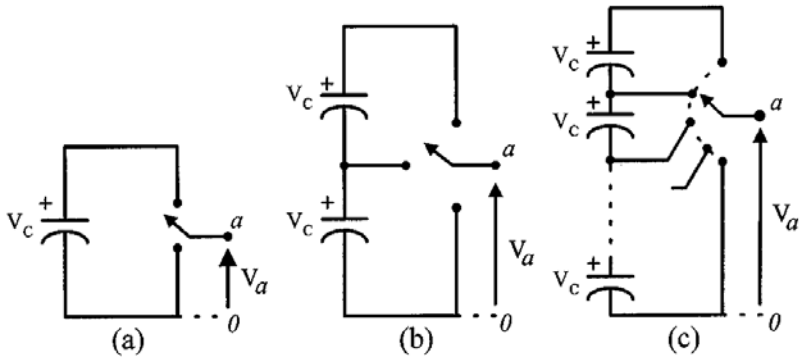


Figure 1.3. One phase leg of an inverter
(a) Two levels, (b) Three levels, and (c) *n* levels

Multilevel inverters have been receiving increasing attention in recent years [3], because they have many attractive features. The features are: 1) The output voltage distortion is very low due to multiple levels in the output voltages. 2) The *dv/dt* of switches is low since the switches endure reduced voltage. 3) The switches can operate at a lower switching frequency. 4) In the applications of motor drives, the input currents have low distortions and the common-mode voltages are reduced. 5) The common-mode voltages can be eliminated using sophisticated modulation methods [4, 5].

Various kinds of multilevel inverters have been proposed, tested and installed. They are diode-clamped (neutral-clamped) multilevel inverters [6]; capacitors-clamped (flying capacitors) multilevel inverters [3, 7], cascade multilevel inverters with separate DC sources [3, 8, 9], hybrid multilevel inverters [10-15], generalized multilevel inverters [16], mixed-level multilevel inverters [17], , multilevel inverters by the connection of three-phase two-level inverters [9], and soft-switched multilevel inverters [18-25].

The family of multilevel inverters has emerged as the solution for high power applications. This is because it is difficult to be implemented via a single power semiconductor switch directly in a medium-voltage network [3, 26, 27]. Multilevel inverters have been applied to different high power applications, such as large motor drives [13, 17, 27-34], railway traction applications [28-31, 35], HVDC transmissions [36], Unified Power Flow Controllers (UPFC) [37-40], Static Var Compensators (SVC) and STATCOM [36, 41-51]. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased. The transformers can be eliminated due to the reduced voltage that the switch sustains. Moreover, as cost effective solutions, the applications of multilevel inverters are also extended to medium and low power applications, such as electrical

vehicle propulsion systems [27, 34], active power filters (APF) [52-55], voltage sag compensations [56], photovoltaic systems [57-59] and distributed power systems [26].

Multilevel inverter circuits have been around for about 30 years. The cascade multilevel inverter was first proposed in 1975 [60]. Separate DC-sourced full-bridge cells are placed in series to synthesize a staircase AC output voltage. The diode-clamped inverter, also called the Neutral-Point Clamped (NPC) inverter, was presented in 1980 [61]. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, this circuit topology prevailed in 1980s. The capacitor-clamped multilevel inverter emerged in the 1990s [62, 63]. Although the cascade multilevel inverter was invented earlier, its application did not prevail until the mid 1990s. The advantages of cascade multilevel inverters were prominent for motor drives and utility applications. The cascade inverter has drawn great interest due to the great demand of medium-voltage high-power inverters. The cascade inverter is also used in regenerative-type motor drive applications [64, 65]. Recently, some new topologies of multilevel inverters have emerged. This included generalized multilevel inverters [16], mixed multilevel inverters [17], hybrid multilevel inverters [10, 14] and soft-switched multilevel inverters [18-22]. Today, multilevel inverters are used extensively in high-power applications with medium voltage levels, such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. Moreover, as a cost-effective solution, the application of multilevel inverters has also extended to low

power application, such as photovoltaic systems [58], hybrid electrical vehicles [34] and voltage sag compensation [56], in which the effort of output filter components can be decreased substantially due to low harmonics distortion of output voltages of the multilevel inverters.

1.3 Topologies of multilevel inverters

1.3.1 Diode-clamped inverter

A three-level diode-clamped inverter is shown in Figure 1.4 (a). In this circuit, the DC-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors, *n*, can be defined as the neutral point. The output voltage v_{an} has three states: *E*, 0 and -*E*. For voltage level *E*, switches S_1 and S_2 need to be turned on; for -*E*, switches $S_{1'}$ and $S_{2'}$ need to be turned on; and for the 0 level, S_2 and $S_{2'}$ need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and $D_{1'}$. These two diodes clamp the switch voltage to half the level of the DC-bus voltage. When both S_1 and S_2 are turned on, the voltage across *a* and 0 is 2*E*, i.e., $v_{a0} = 2E$. In this case, $D_{1'}$ balances out the voltage sharing between $S_{1'}$ and $S_{2'}$ with $S_{1'}$ blocking the voltage across C_1 and $S_{2'}$ blocking the voltage across C_2. Notice that the output voltage v_{an} is AC, and v_{a0} is DC. The difference between v_{an} and v_{a0} is

the voltage across C_2, which is E. If the output is removed between a and 0, then the circuit becomes a DC/DC converter, which has three output voltage levels: E, 0 and -E.

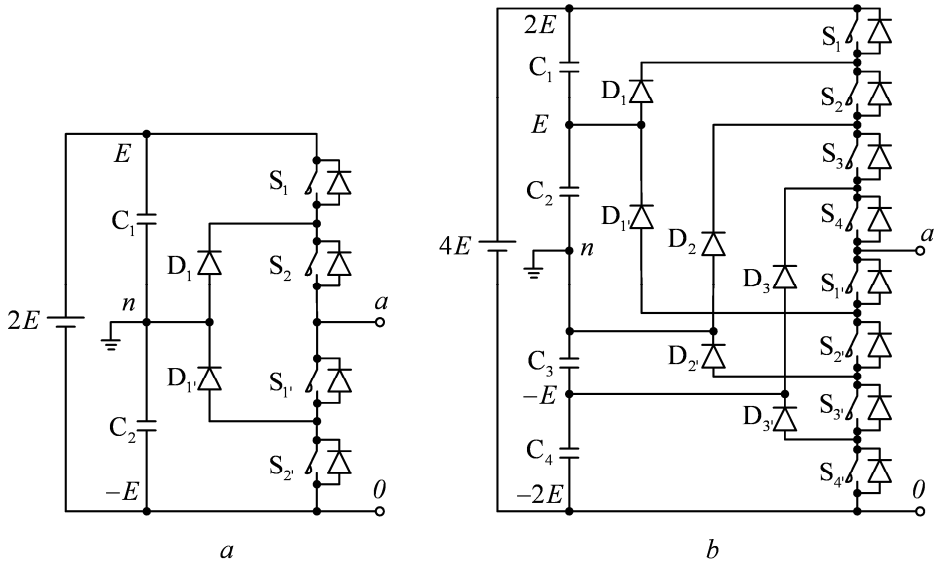


Figure 1.4. Diode-clamped multilevel inverter circuit topologies
(a) Three-level (b) Five-level

Figure 1.4 (b) shows a five-level diode-clamped converter in which the DC bus consists of four capacitors, C_1, C_2, C_3 and C_4. For DC bus voltage 4E, the voltage across each capacitor is E, and each device voltage stress will be limited to one capacitor voltage level E through clamping diodes.

In explaining how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are five switch combinations used to synthesize the five level voltage across a and n.

- For voltage level van = 2E, turn on all upper switches S1 ~ S4.

- For voltage level van = E, turn on three upper switches S2 ~ S4 and one lower switch S1'.
- For voltage level van = 0, turn on two upper switches S3 and S4 and two lower switches S1' and S2'.
- For voltage level van = -E, turn on one upper switch S4 and three lower switches S1' ~ S3'.
- For voltage level van = -2E, turn on all lower switches S1' ~ S4'.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1, $S_{1'}$), (S_2, $S_{2'}$), (S_3, $S_{3'}$), and (S_4, $S_{4'}$).

Although each active switching device is only required to block a voltage level of *E*, the clamping diodes must have different voltage ratings for reverse voltage blocking. Using $D_{1'}$ of Figure 1.4 (b) as an example, when lower devices $S_{2'}$ ~ $S_{4'}$ are turned on, $D_{1'}$ needs to block three capacitor voltages, or 3*E*. Similarly, D_2 and $D_{2'}$ need to block 2*E*, and D_1 needs to block 3*E*.

1.3.2 Capacitor-clamped inverter

Figure 1.5 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter with dependent capacitors clamping the device voltage to one capacitor voltage level. The

inverter in Figure 1.5 (a) provides a three-level output across *a* and *n*, i.e. $v_{an} = E$, 0, or -*E*. For the voltage level *E*, switches S_1 and S_2 need to be turned on; for -*E*, switches $S_{1'}$ and $S_{2'}$ need to be turned on; and for the 0 level, either pair (S_1, $S_{1'}$) or (S_2, $S_{2'}$) needs to be turned on. Clamping capacitor C_1 is charged when S_1 and $S_{1'}$ are turned on, and is discharged when S_2 and $S_{2'}$ are turned on. The charge of C_1 can be balanced by a proper selection of the 0-level switch combinations.

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Figure 1.5 (b) as an example, the voltage of the five-level phase-leg *a* output with respect to the neutral point *n*, v_{an}, can be synthesized by the following switching combinations.

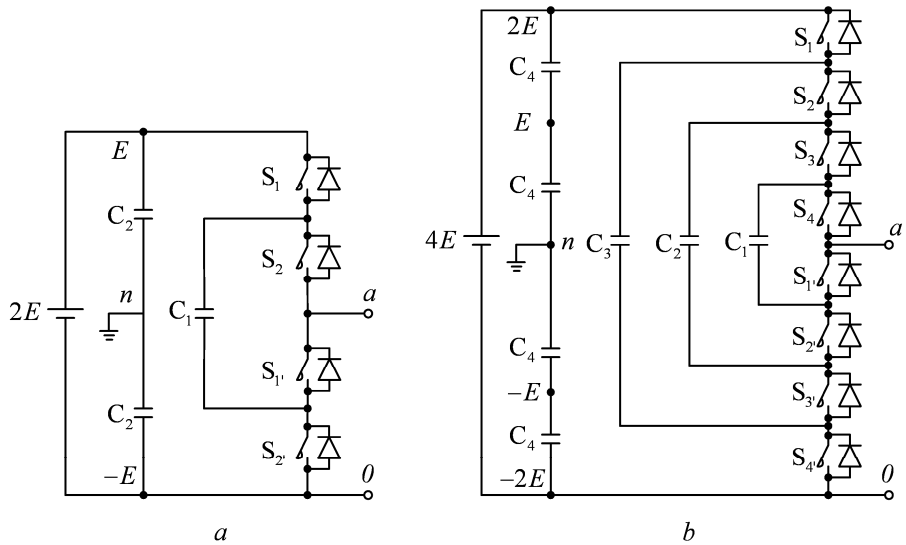


Figure 1.5. Capacitor-clamped multilevel inverter circuit topologies
(a) Three-level (b) Five-level

- For voltage level $v_{an} = 2E$, turn on all upper switches $S_1 \sim S_4$.
- For voltage level $v_{an} = E$, there are three combinations:
  - S_1, S_2, S_3, $S_{1'}$: $v_{an} = 2E$ (upper C_4) - E (C_1);
  - S_2, S_3, S_4, $S_{4'}$: $v_{an} = 3E$ (C_3) - $2E$ (lower C_4); and
  - S_1, S_3, S_4, $S_{3'}$: $v_{an} = 2E$ (upper C_4) - $3E$ (C_3) + $2E$ (C_2).
- For voltage level v_{an} =0, there are six combinations:
  - S_1, S_2, $S_{1'}$, $S_{4'}$: $v_{an} = 2E$ (upper C_4) - $2E$ (C_2);
  - S_3, S_4, $S_{3'}$, $S_{4'}$: $v_{an} = 2E$ (C_2) - $2E$ (lower C_4);
  - S_1, S_3, $S_{1'}$, $S_{3'}$: $v_{an} = 2E$ (upper C_4) - $3E$ (C_3) + $2E$ (C_2) - E (C_1);
  - S_1, S_4, $S_{2'}$, $S_{3'}$: $v_{an} = 2E$ (upper C_4) - $3E$ (C_3) + E (C_1);
  - S_2, S_4, $S_{2'}$, $S_{4'}$: $v_{an} = 3E$ (C_3) - $2E$ (C_2) + E (C_1) - $2E$ (lower C_4); and
  - S_2, S_3, $S_{1'}$, $S_{4'}$: $v_{an} = 3E$ (C_3) - E (C_1) - $2E$ (lower C_4).
- For voltage level $V_{an} = -E$, there are three combinations:
  - S_1, $S_{1'}$, $S_{2'}$, $S_{3'}$: $v_{an} = 2E$ (upper C_4) - $3E$ (C_3);
  - S_4, $S_{2'}$, $S_{3'}$, $S_{4'}$: $v_{an} = E$ (C_1) - $2E$ (lower C_4); and
  - S_3, $S_{1'}$, $S_{3'}$, $S_{4'}$: $v_{an} = 2E$ (C_2) - E (C_1) - $2E$ (lower C_4).
- For voltage level $v_{an} = -2E$, turn on all lower switches, $S_{1'} \sim S_{4'}$.

In the preceding description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode. By proper selection of capacitor combinations, it is possible to balance the capacitor charge.

1.3.3 Cascade multilevel inverter (CMI)

The basic structure is based on the connection of H-Bridges (HBs). Figure 1.6 shows the power circuit for one phase leg of a multilevel inverter with three HBs (HB_1, HB_2 and HB_3) in each phase. Each HB is supplied by a separate DC source. The resulting phase voltage is synthesized by the addition of the voltages generated by the different HBs. If the DC link voltages of HBs are identical, the multilevel inverter is called the cascade multilevel inverter. However, it is possible to have different values among the DC link voltages of HBs, and the circuit can be called the hybrid multilevel inverter.

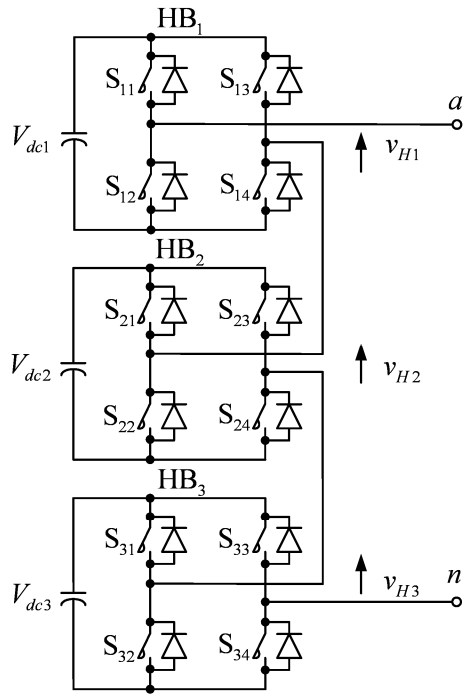


Figure 1.6. Multilevel inverter based on the connection of HBs

In cascade multilevel inverter, the DC link voltages of HBs are identical, etc. in Figure 1.6,

$$V_{dc1} = V_{dc2} = V_{dc3} = E \tag{1.1}$$

where E is unit voltage. Each HB generates three voltages at the output: +E, 0, and -E. This is made possible by connecting the capacitors sequentially to the AC side via the three power switches. The resulting output AC voltage swings from -3E to 3E with seven levels as shown in Figure 1.7.

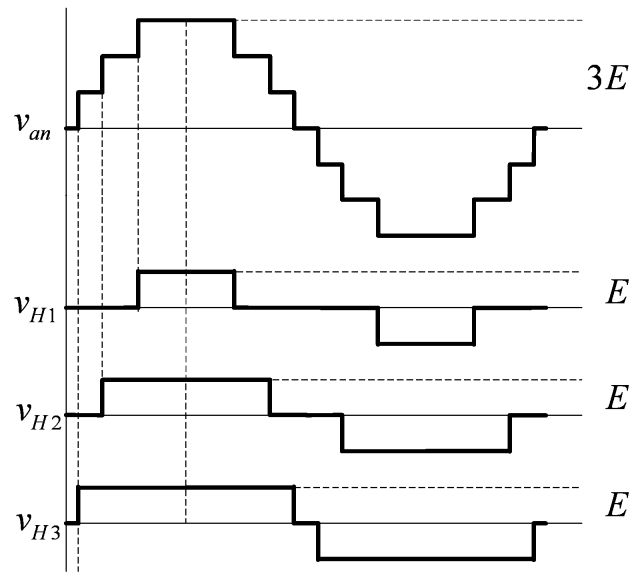


Figure 1.7. Waveforms of cascade multilevel inverter

1.3.4 Binary hybrid multilevel inverter (BHMI)

In binary hybrid multilevel inverters, the DC link voltages of HB_i (the ith HB), V_{dci}, is $2^{i-1}E$. In a 3-HB one phase leg,

$$V_{dc1} = E \quad V_{dc2} = 2E \quad V_{dc3} = 4E \tag{1.2}$$

As shown in Figure 1.8, the output waveform, v_{an}, has 15 levels. One of the advantages is that the HB with a higher DC link voltage has a lower number of commutation and thereby reduces the associated switching losses. Manjrekar, et. al [14] illustrates a seven-level inverter using this hybrid topology. The HB with higher DC link voltage consists of lower switching frequency component, e.g. IGCT. The higher switching

frequency components, e.g. IGBT, are used to construct the HB with a lower DC link voltage.

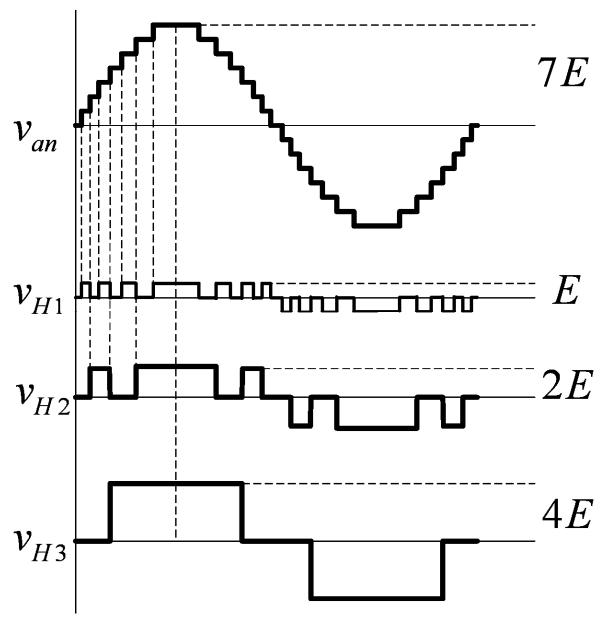


Figure 1.8. Waveforms of binary hybrid multilevel inverter

1.3.5 Quasi-linear multilevel inverter (QLMI)

In quasi-linear multilevel inverter, the DC link voltages of HB$_i$, V_{dci} can be expressed as

$$V_{dci} = \begin{cases} E & i = 1 \\ 2 \times 3^{i-2} E & i \geq 2 \end{cases} \tag{1.3}$$

In a 3-HB one phase leg,

$$V_{dc1} = E \quad V_{dc2} = 2E \quad V_{dc3} = 6E \tag{1.4}$$

As shown in Figure 1.9, the output waveform, v_{an}, has 19 levels.

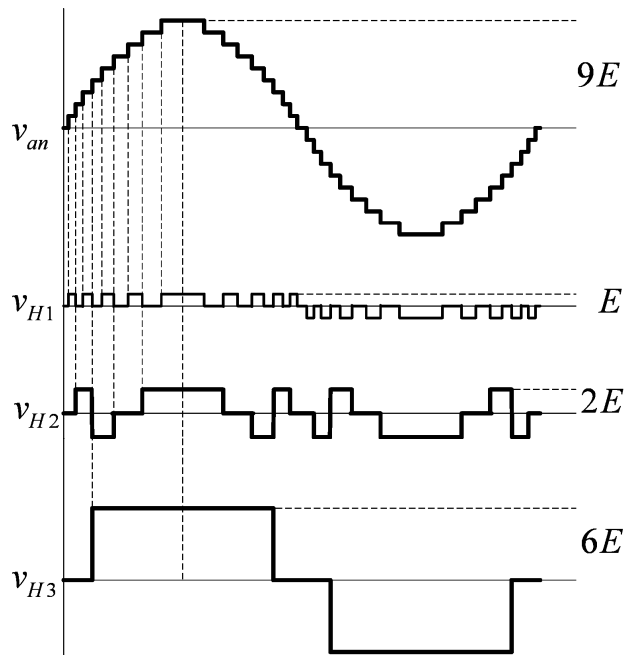


Figure 1.9. Waveforms of quasi-linear multilevel inverter

1.3.6 Trinary hybrid multilevel inverter (THMI)

In a trinary hybrid multilevel inverter, the DC link voltages of HB_i, V_{dci}, is $3^{i-1}E$. In a three-HB one phase leg,

$$V_{dc1} = E \quad V_{dc2} = 3E \quad V_{dc3} = 9E \tag{1.5}$$

As shown in Figure 1.10, the output waveform, v_{an}, has 27 levels. To the best of the author's knowledge, this circuit has the greatest level number for a given number of HBs among existing multilevel inverters.

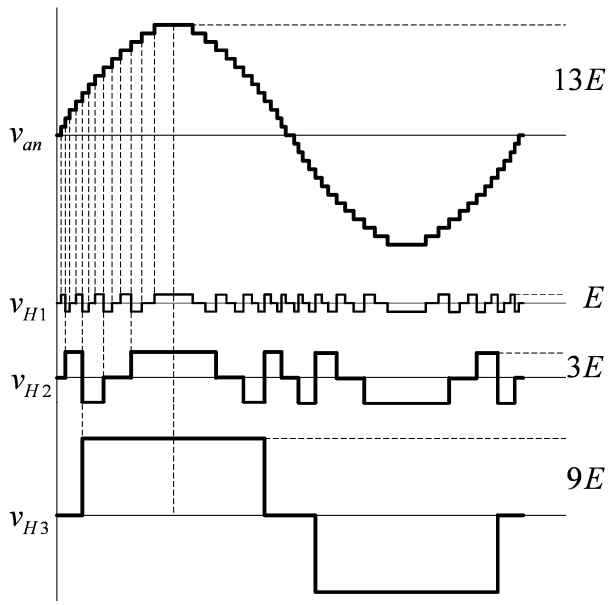


Figure 1.10. Waveforms of trinary hybrid multilevel inverter

1.3.7 Other kinds of multilevel inverters

1.3.7.1 Generalized multilevel inverters (GMI)

A generalized multilevel inverter topology has previously been presented in [16]. The existing multilevel inverters, such as diode-clamped and capacitor-clamped multilevel inverters, can be derived from this generalized inverter topology. Moreover, the generalized multilevel inverter topology can balance each voltage level by itself regardless of load characteristics. Therefore, the generalized multilevel inverter topology provides a true multilevel structure that can balance each DC voltage level automatically at any number of levels, regardless of active or reactive power

conversion, and without any assistance from other circuits. Thus, in principle, it provides a complete multilevel topology that embraces the existing multilevel inverters.

As shown in Figure 1.11, the basic cell is a two-level phase leg, so this generalized multilevel inverter is called a P2 multilevel inverter. Each switching device, diode, or capacitor's voltage is E, i.e., $1/(m\text{-}1)$ of the DC-link voltage. Any inverter with any number of levels, including the conventional two-level inverter can be obtained using this generalized topology.

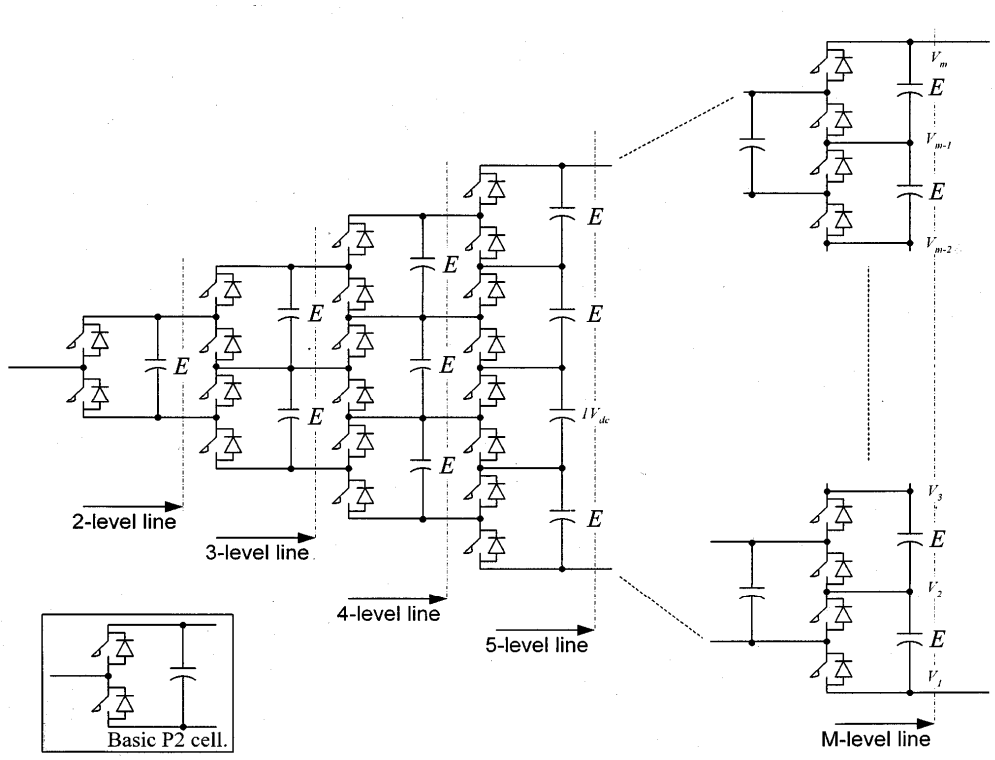


Figure 1.11. Generalized P2 multilevel inverter structure

1.3.7.2 Mixed-level multilevel inverter topologies

For high-voltage high-power applications, it is possible to adopt multilevel diode-clamped or capacitor-clamped inverters to replace the full-bridge cell in a cascade multilevel inverter [17]. The reason for doing so is to reduce the amount of separate DC sources. The nine-level cascade inverter requires four separate DC sources for one phase leg and twelve for a three-phase inverter. If a three-level inverter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-phase inverter. The configuration can be considered as having mixed-level multilevel cells because it embeds multilevel cells as the building block of the cascade multilevel inverter.

1.3.7.3 Multilevel inverters by the connection of three-phase two-level inverters

Standard three-phase two-level inverters are connected by transformers as shown in Figure 1.12 [9]. In order for the inverter output voltages to be added up, the inverter outputs of the three modules need to be synchronized with a separation of 120° between each phase. For example, obtaining a three-level voltage between outputs a and b, the voltage is synthesized by $V_{ab} = V_{a1\text{-}b1} + V_{a1\text{-}b1} + V_{a1\text{-}b1}$. The phase between b_1 and a_2 is provided by a_3 and b_3 through an isolated transformer. With three inverters synchronized, the voltages $V_{a1\text{-}b1}$, $V_{a1\text{-}b1}$, $V_{a1\text{-}b1}$ are all in phase; thus, the output level is simply tripled.

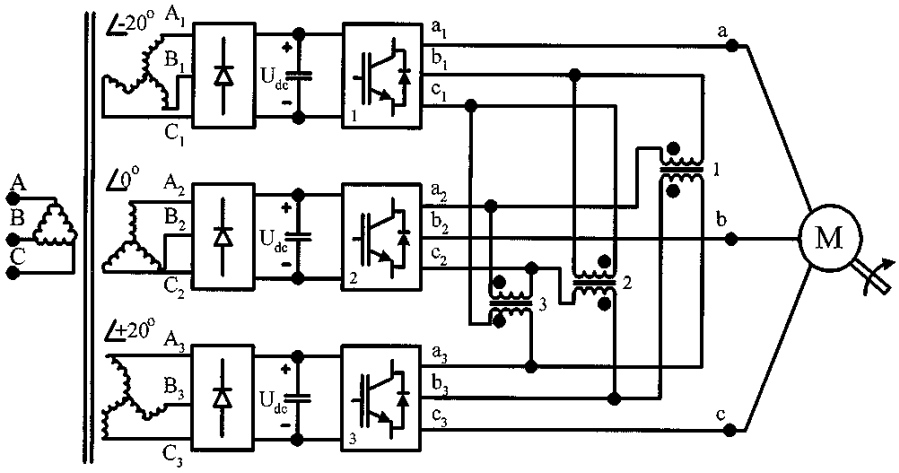


Figure 1.12. Cascade inverter with three-phase cells

1.3.7.4 Soft-switched multilevel inverters

There are numerous ways of implementing soft-switching methods, such as Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). This reduces the switching losses and increases efficiency for different multilevel inverters. For the cascade multilevel inverter, because each inverter cell is a two-level circuit, the implementation of soft switching is not at all different from that of conventional two-level inverters. For capacitor- or diode-clamped inverters, however, the choice of a soft-switching circuit can be found with different circuit combinations [18, 21, 23-25]. Although ZVS is possible [66], most literature proposes ZVS types including Auxiliary Resonant Commutated Pole (ARCP), coupled inductors with Zero-Voltage Transition (ZVT), and their combinations.

1.4 Applications of multilevel inverters

1.4.1 High power applications

In a medium-voltage network, it is difficult to connect a single power semiconductor switch directly to medium-voltage grids (2.3, 3.3, 4.16, or 6.9 kV). Multilevel inverters are presented as the solutions for working with higher voltage levels.

1.4.1.1 Large motor drives with non-regenerative front ends.

Diode-clamped three-level multilevel inverters are now widely applied in medium-voltage (2.3, 3.3, 4.16, and even 6 kV) applications, using an IGBT with forced-air cooling. These applications cover a wide range of high-power loads including fans, pumps, blowers, compressors, and conveyors. A three-level capacitor-clamped multilevel inverter is also used as a motor drive [67]. A seven -level cascade multilevel inverter is used in non-regenerative drives in 2.3 kV network [8]. The input part of each HB has a three-phase diode rectifier, which does not allow the regeneration of power. Tolbert, et. al [68] presents a transformerless multilevel inverter as an application for High-power Electric Vehicle (HEV) motor drives. Multilevel inverters have almost no electromagnetic interference or common-mode voltage; and make a HEV more accessible and safer. And open wiring is possible for most of an HEV

power system. A hybrid seven-level inverter is applied in the 4.16 kV systems. The top HB uses IGBT and the low one uses GTO [14].

1.4.1.2 Large motor drives with regenerative front ends

The use of a three-level Active Front End (AFE) at the input side of a three-level diode-clamped inverter has become a very popular solution for high-power regenerative loads [69, 70]. Especially in [70], two three-level AFEs that are used in a so-called tandem configuration. Rodriguez, et. al [71] presents a multilevel converter with regeneration capacity. Each cell in the converter contains a single-phase inverter at the output side and a PWM rectifier at the input side. The output side inverters of the cells are connected in series, while the input side rectifiers are connected in parallel through the input transformer. A single-phase AFE, instead of a three-phase one, has been considered at the input side of each cell to achieve lower power semiconductors and simpler control.

1.4.1.3 Applications in power systems

The first Unified Power Flow Controller (UPFC) in the world was based on a diode-clamped three-level inverter [38]. The UPFC is comprised of the back-to-back connection of two identical GTO thyristor-based three-level converters, each rated at 160 MVA. It was commissioned in mid 1998 at the Inez Station of American Electric Power (AEP) in Kentucky for voltage support and power-flow control. On the other

hand, the cascade multilevel inverter is best suited for harmonic/reactive compensation and other utility applications [48, 72, 73]. Each HB inverter unit can balance its DC voltage without requiring additional isolated power sources. GEC Alsthom T&D has commercialized the cascade multilevel inverter for reactive power compensation/generation (STATCOM).

1.4.2 Medium and low power application

The AC output terminal voltage that multilevel inverters synthesize has low harmonic distortion. Thus, the filter requirement is reduced. Moreover, with the topologies of multilevel inverters, the transformers can be eliminated. In recent years, the volume and price of active components (semiconductor switches) has decreased significantly, while the passive components, such as inductors, capacitors or transformers have remained about the same. Therefore, in medium and low applications, the systems with the configuration of multilevel inverters can be compacter and cheaper.

1.4.2.1 Photovoltaic systems

Various topologies of multilevel inverters have been investigated for the application of a photovoltaic system in [57]. Amongst the topologies without transformers, the diode clamped multilevel inverters and the cascade multilevel inverters have been identified as the most promising topologies. The design and control

issues associated with the development of a 1.8 kW prototype single-phase grid-connected photovoltaic system incorporating a cascade multilevel inverter is discussed in [59].

1.4.2.2 Voltage sag compensation

A cascade multilevel inverter was studied as a cost-effective way of series sag compensation, because it eliminates the bulky injection transformers and other large filter components used in series active filters [74]. Batteries and high-current automotive MOSFETs proved to be interesting options in terms of energy storage and switching components for this design.

1.4.2.3 Distributed energy application

Distributed energy systems, mostly those using alternative energies such as fuel cells or photovoltaic panels, can be easily configured with a separate source connected through the power conversion circuits used as an energy module or building blocks to provide individual output. A cascade multilevel inverter can then be configured with multiple modules. Such a system does not need a transformer to provide isolation. This system can be constructed in a cost effective manner [26].

1.5 Modulations of multilevel inverters

The function of a modulation strategy is to force the inverter voltages/currents to follow the reference voltages/currents. The modulation strategies for inverters can be

divided into two categories: The voltage modulation strategies and the current modulation strategies. These are corresponding to the voltage-mode control and the current-mode control, respectively.

The voltage-mode control system for an inverter will generate reference voltages. The output voltages of the inverter will follow the reference voltages. The current-mode control system will generate reference currents instead of reference voltages. The inverter currents will follow the reference currents.

In the applications of multilevel inverters, the voltage-mode control systems are much more popular than the current-mode control systems. The reason is that the current-mode control systems usually require very high switching frequencies for smoothing currents. Most multilevel inverters are used in high-voltage and high-power application where the power semiconductor switches cannot switch at very high frequencies. With the voltage-mode control, contrarily, the inverter can switch at lower frequencies, even line-frequency for the cases of multilevel inverters.

Thus, only the modulation strategies for the voltage-mode control will be investigated. Figure 1.13 illustrates the function of the modulation strategies in the whole system for inverters. The voltage-mode control system generates reference voltages that are generally sinusoidal waveforms. The blocks implementing modulation strategies will generate firing pulse based on reference voltages. The inverters receive these firing signals, and then generate output voltages of the inverters.

There are two basic requirements for a modulation strategy. The first one is that the reference voltages must be in phase with output voltages of the inverter. The second one is that the amplitudes of fundamental components of reference voltages and inverter voltages must be identical.

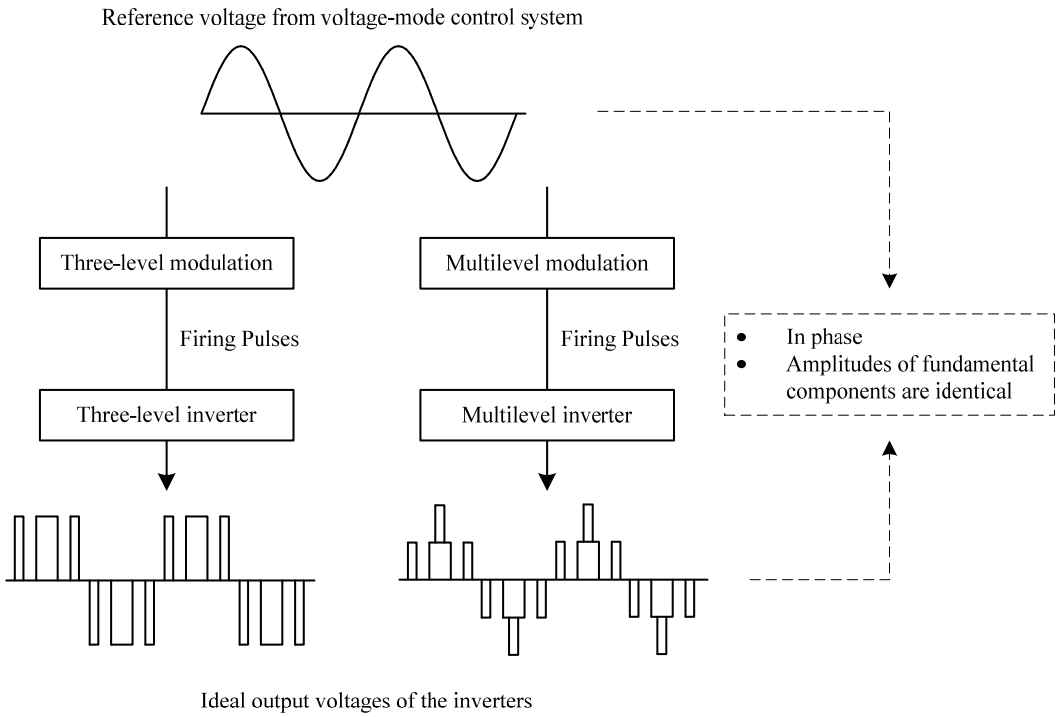


Figure 1.13. Modulation strategy for the voltage-mode control system

An additional requirement for modulation strategies is about voltage harmonics. The specific requirements change according to different applications. Roughly, the total harmonic distortion is expected to be small. Meanwhile, in most applications,

lower order harmonics are expected to be small. This will be described in detail later in this chapter.

Various modulation strategies for multilevel inverters with voltage-mode control have been developed for multilevel inverters. The authors in [26] classified these modulation strategies used in multilevel inverters according to switching frequencies. I classified these modulation strategies here according to the mechanism of the modulation strategies instead of switching frequencies. There are four categories. They are: multilevel SPWM, space vector modulation, space vector control, and optimal modulation. I will introduce the first three briefly and specify the last one in detail.

1.5.1 Multilevel SPWM

The multilevel Sinusoidal Pulse Width Modulation (SPWM) is based on the classical SPWM with triangular carriers. One method uses phase shifting of multiple carrier signals [75, 76]. Figure 1.14 shows this method in a seven-level cascade multilevel inverter [77]. For an m-level inverter, the number of carriers is (m-1). The phase shift is 360° / (m-1). Another method uses voltage shifting of multiple carrier signals [32, 75, 76]. Figure 1.15 shows this method in a seven-level inverter. For an m-level inverter, the number of carriers is (m-1).

With the above two multilevel SPWM, the dominant lower order harmonics are pushed to around $(m\text{-}1)f_{sw}$, where f_{sw} is the switching frequency of power

semiconductor devices. In other words, equivalent switching frequency of the inverter is $(m\text{-}1)f_{sw}$.

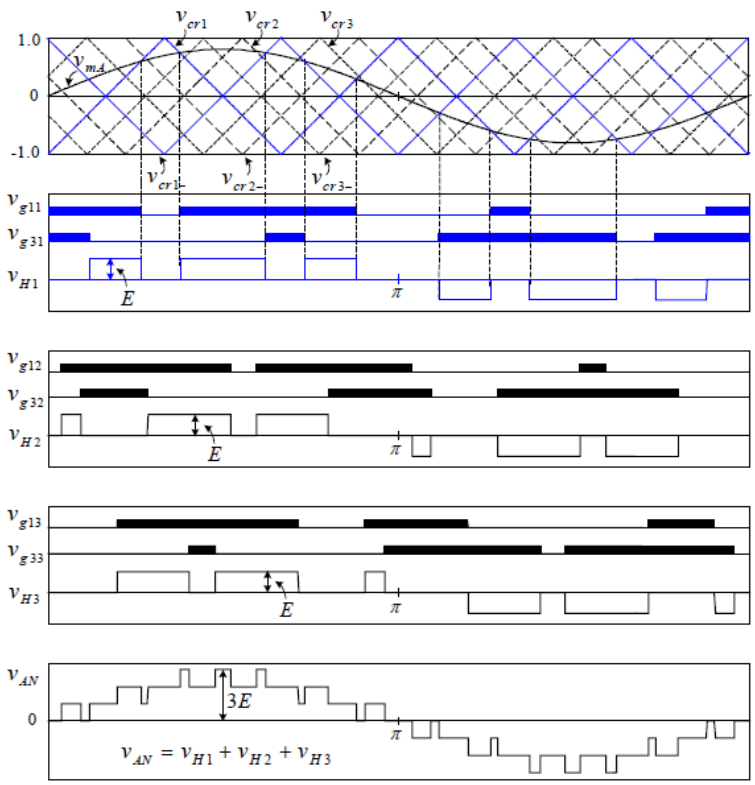


Figure 1.14. Multilevel SPWM using phase shifting of multiple carrier signals in a seven-level inverter

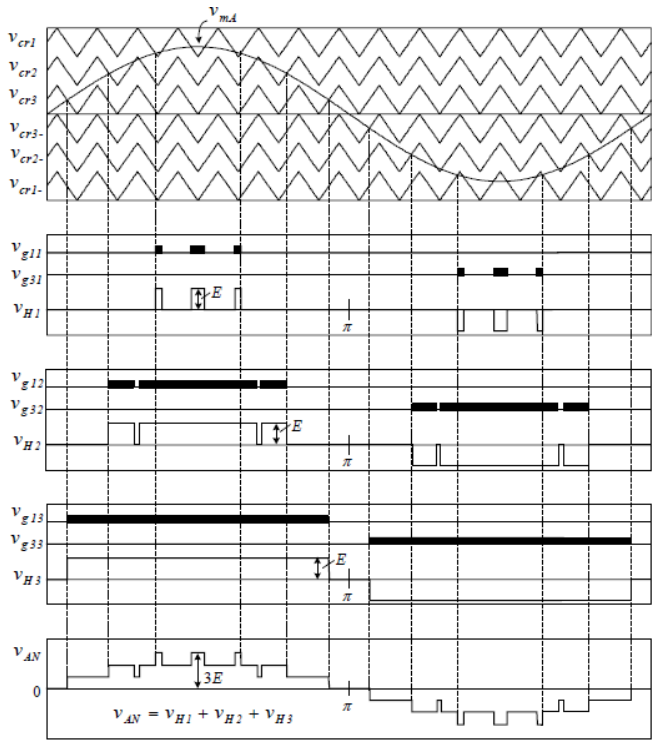


Figure 1.15. Multilevel SPWM using voltage shifting of multiple carrier signals in a seven-level inverter

1.5.2 Space vector modulation

The space vector modulation used in two-level or three-level inverters can be easily extended to all multilevel inverters [78, 79]. Figure 1.16 shows space vectors for the traditional two-, three- and five-level inverters. The adjacent three vectors can synthesize a desired voltage vector by computing the duty cycle (T_j, T_{j+1}, and T_{j+2}) for each vector as shown in (1.6). The harmonic performance of the space vector modulation is similar to that of multilevel SPWM.

$$V^* = \frac{(T_j V_j + T_{j+1} V_{j+1} + T_{j+2} V_{j+2})}{T} \tag{1.6}$$

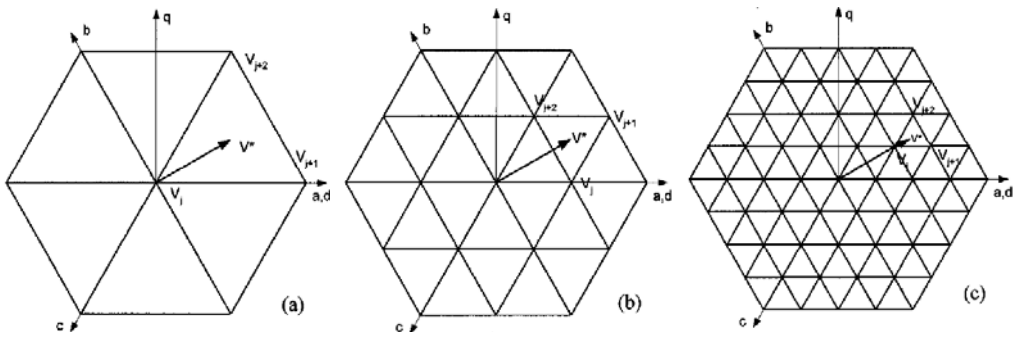


Figure 1.16. Space-vector diagram: (a) two-level, (b) three-level, and (c) five-level

1.5.3 Space vector control

Space vector control [4, 80, 81] is also based on the space vector theory, but it is conceptually different than the space vector modulation. This strategy works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as is the principle of the space vector modulation. The main idea is to deliver to the load a voltage vector that minimizes the space error or distance to the reference vector. This strategy is suitable for the inverter with many levels. The high density of vectors produced by the inverter with many levels will generate only small errors in relation to the reference vector. Figure 1.17 shows the voltage generated by one cell in an 11-level inverter. The load voltage of the inverter is shown in Figure 1.17 (b).

As shown in Figure 1.17 (b), the inverter voltage generated by the space vector control is similar to that generated by the staircase modulation. The space vector modulation doesn't optimize the waveform for certain aims, like harmonic elimination or minimization.

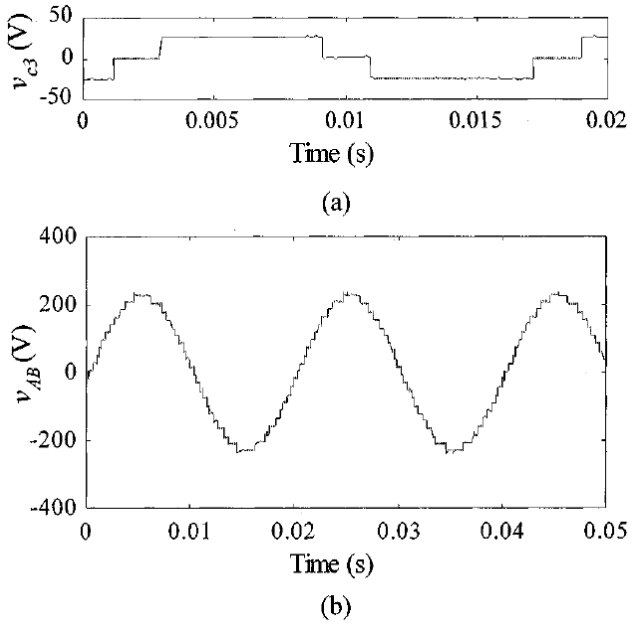


Figure 1.17. Voltage generated by an 11-level inverter with space vector control. (a) One-cell voltage. (b) Resulting load voltage.

1.5.4 Optimal Modulation

Optimal modulations are fundamentally different with above modulation methods. Firstly, the inputs of modulation blocks are different as shown in Figure 1.18. For modulation strategies aforementioned, the input of the modulation block is the

instantaneous value of reference voltage. For optimal modulation strategies, the inputs are modulation index representing amplitude and phase representing phase information. Secondly, for modulation strategies aforementioned, the characteristics of voltage spectrums are determined by the mechanism of the modulation strategies. For optimal modulation, different optimal modulations result in different voltage spectrums, which are determined by pre-defined different optimal aims.

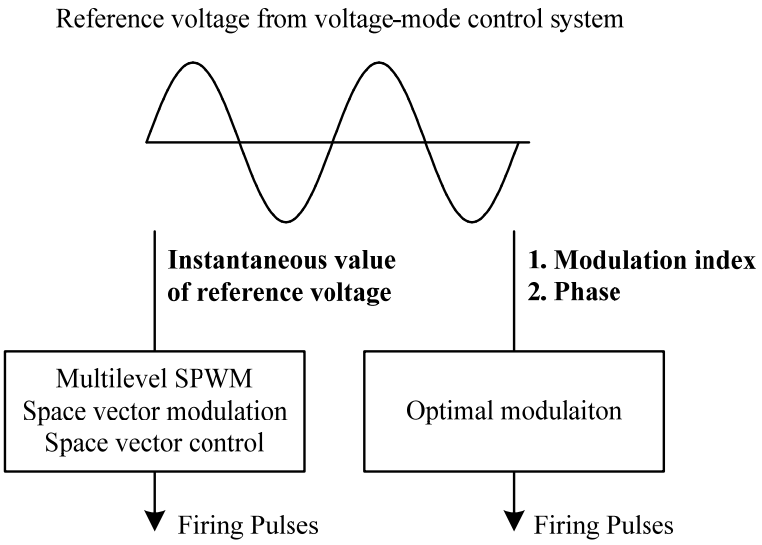


Figure 1.18. Comparison between optimal modulation and other modulation

Several optimal modulation strategies have been proposed, which are introduced as follows with the example multilevel inverter as shown in Figure 1.19.

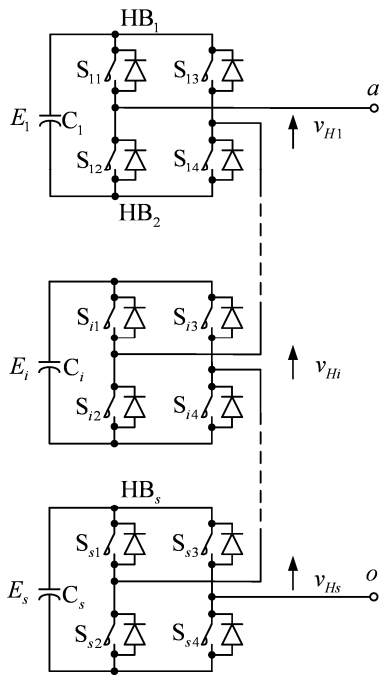


Figure 1.19. A phase leg of cascade multilevel inverter

1.5.4.1 Staircase modulation with elimination of lower order harmonics

The phase voltage of the inverter with the staircase modulation is shown in Figure 1.20. The switching angles, θ_1, θ_2 … θ_s, determine the waveform shape. In the first quarter cycle, the voltage increases a level after reaching a new switching angle. This is the basic principle of the staircase modulation.

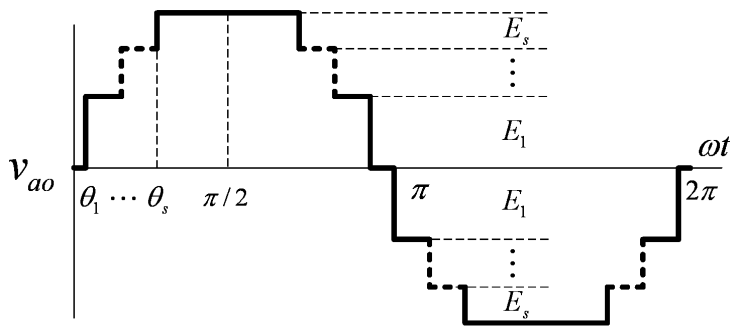


Figure 1.20. Phase voltage of a multilevel inverter with the staircase modulation

For the waveform shown in Figure 1.20, by applying Fourier series analysis, the amplitude of any odd *n*th harmonic can be expressed as

$$V_n = \frac{4}{n\pi}\sum_{k=1}^{s}[E_k \cos(n\theta_k)] \tag{1.7}$$

where n is an odd harmonic order and θ_k is the kth switching angle. The amplitudes of all even harmonics are zero. The modulation index, m, is defined as

$$m = \frac{\pi}{4}\frac{V_1}{\sum_{i=1}^{s} E_i} \tag{1.8}$$

The voltage THD is defined as:

$$\text{THD} = \sqrt{\frac{\sum_{n=3,5,7\ldots} V_n^2}{V_1^2}} \tag{1.9}$$

Elimination of lower order harmonics is the optimal goal for the staircase modulation. Most previous literatures refers to the equal voltage steps show in the Figure 1.20. Thus, we assume E_1 to E_s are equal to E. For an inverter with ($2s$+1) levels,

the maximum number of eliminated lower order harmonics is (s-1). Take the example of a seven-level inverter, the third and fifth harmonics can be eliminated as shown in

$$\begin{aligned} &\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)=3\cdot m \\ &\cos(3\theta_1)+\cos(3\theta_2)+\cos(3\theta_3)=0 \\ &\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)=0 \end{aligned} \tag{1.10}$$

In the three-phase system, triple order harmonics can be automatically eliminated by proper connection of a three-phase system. In other words, it is not necessary to eliminate tripe order harmonics by the modulation. For a seven-level case, the fifth and seventh harmonics will be eliminated as shown in

$$\begin{aligned} &\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)=3\cdot m \\ &\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)=0 \\ &\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)=0 \end{aligned} \tag{1.11}$$

The equation sets shown in (1.10) and (1.11) are non-linear and transcendental. Several methods, such as the Newton-Raphson iteration method with multiple variables [27], the methods based on the theory of symmetric polynomials and resultants [82], and the methods based on genetic algorithms [83, 84], have been proposed to solve the non-linear transcendental equation set. Calculations based on all above methods are very time-consuming.

1.5.4.2 Staircase modulation with equal voltage-second area

Several people tried to develop algorithms using switching angles that can be calculated in real-time for the staircase modulation. In [85], a simple method has been

proposed. It makes use of the voltage-second areas of the divided reference voltage according to the output voltage levels of the inverter. This method avoids solving a set of nonlinear transcendental equations, but calculates several trigonometric functions. Thus, the calculation based on this method can be done in real-time. However, this method cannot guarantee that the THD of the voltage is minimized or the lower order that harmonic components of the voltage are eliminated.

1.5.4.3 Selective harmonic elimination PWM with equal voltage steps

In the staircase modulation, the output voltage levels of the multilevel inverter limit the amount of eliminated lower order harmonics. The selective harmonic elimination PWM [82-84, 86, 87] increases the amount of eliminated lower order harmonics without increasing the number of output voltage levels. The selective harmonic elimination PWM was first introduced in 1973 for two-level high-power inverters. As shown in Figure 1.21, more notches have been added to increase the number of switching angles. This is different with the staircase modulation, where the voltage might increase or decrease a level after reaching a new switching angle in the first quarter cycle. Thus, the amount of eliminated lower order harmonics is determined by the number of switching angles instead of voltage levels. The equation sets for solving these switching angles are also non-linear and transcendental. The methods proposed in [27, 82-84, 86] may be used to solve the equation sets. Calculations based on all above methods are still very time-consuming. The selective harmonic

elimination PWM might eliminate more lower-order harmonics, but increase the amplitudes of higher-order harmonics. Moreover, the equation sets might have no solution if more notches are added.

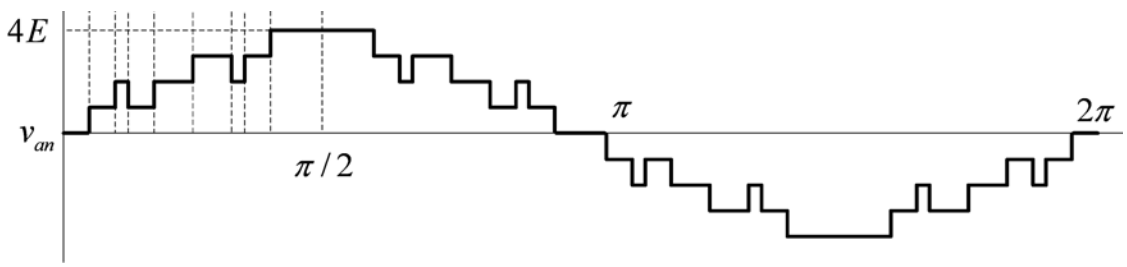


Figure 1.21. Waveform using the selective harmonics elimination PWM

1.5.4.4 Selective harmonic elimination PWM with unequal voltage steps

Voltage steps in multilevel inverters might not be the same. Available DC sources of the cascade multilevel inverters are batteries, photovoltaic arrays, fuel cells, rectifies … etc [88]. In cascade multilevel inverter based photovoltaic systems [89, 90], the operating DC voltages of standard photovoltaic cells range from 15V to 35 V [91]. In the cascade multilevel inverter based energy storage system with batteries [92], the voltages of batteries also change due to their states of charge. The varying voltages of DC sources result in varying voltage steps in the multilevel output waveform. The varying voltage steps (varying DC source voltages) bring challenges to the algorithms in determining switching angles for the staircase modulation. Not only switching angles, but also the variations of voltage steps, will determine the harmonic distortion

of output voltages [88]. The algorithms proposed in [93, 94] address the situations with unequal or varying voltage steps. The optimization aim is the elimination of lower order harmonics and the calculation is still very time-consuming.

1.5.4.5 Selective harmonic mitigation modulation

Recently, a new selective harmonic mitigation modulation has been proposed in [95]. By using this method, all harmonics and THD (instead of only certain harmonics) is considered as a global problem in conjunction with one specific actual grid code. In this way, the elimination of some harmonics is avoided, but high-quality output signals are obtained. This method reformulates the applied grid code and the switching pattern as a nonlinear optimization problem over a continuous space. Solving these nonlinear equations is still very time-consuming. One of the attractive points of this modulation is that it can be customized based on the grid code.

1.6 Control of multilevel inverters

The control strategies for inverters can basically be divided into two categories: voltage-mode control and current-mode control. The voltage-mode control system for an inverter will generate reference voltages. The output voltages of the inverter will follow the reference voltages. The current-mode control system will generate reference currents instead of reference voltages. The inverter currents will follow the reference currents. In the applications of multilevel inverters, the voltage-mode control systems

are much more popular than the current-mode control systems. The reason is that the current-mode control systems usually require very high switching frequencies for smoothing currents. Most multilevel inverters are used in high-voltage and high-power application where the power semiconductors cannot switch at very high frequencies. With the voltage-mode control, contrarily, the inverter can switch at lower frequencies, even line-frequency, in the cases of multilevel inverters.

Various voltage-mode control strategies for multilevel inverters have been proposed, presented and developed for different applications, such as motor drives and FACTS devices. I focus on the control of the multilevel inverter for an important FACTS device, the STATCOM. This is connected as a shunt to the power system, and is used for generating or absorbing reactive power [42]. A STATCOM works in the capacitive mode if it injects reactive power to the power system. It works in the inductive mode if it absorbs reactive power from the system. If there is no reactive power exchange between a STATCOM and the system, the STATCOM works in the standby mode. The STATCOM can be utilized to regulate voltage, control power factor and stabilize power flow [109]. Compared with conventional Static VAr Compensator (SVC), the STATCOM has advantages such as fast speed, compact footprint and small harmonics [42, 110].

Increased attention has been paid to multilevel inverters for the STATCOM in a medium-voltage network because it is difficult to use a single power semiconductor

switch directly in medium-voltage networks [11, 26, 48, 49, 92, 111, 112]. Cascade multilevel inverters that are based on the connection of several H-bridges are very popular among the existing topologies of multilevel inverters due to their modularization and extensibility [3, 113, 114]. The control of a cascade multilevel inverter for the STATCOM has been studied and presented in [48, 49, 73, 88, 111, 112, 115-119].

1.7 Objective

1.7.1 Advanced modulation for multilevel inverters

With the same switching frequency, generally speaking, the voltage quality generated by the optimal modulation is better than that by the popular SPWM or the space vector PWM. I focus on the optimal modulation in the thesis. The brief comparison of the previous optimal modulations aforementioned is shown in Table 1.1.

Table 1.1. Summary of previous optimal modulation strategies

Optimal modulation	Optimization aim	Real time calculation	For varying voltage steps
Staircase modulation with elimination of lower order harmonics	Elimination of lower order harmonics	No	No
Staircase modulation with equal voltage-second area	Voltage-second balance	Yes	No
Selective harmonic elimination PWM with equal voltage steps	Elimination of lower order harmonics	No	No
Selective harmonic elimination PWM with unequal voltage steps	Elimination of lower order harmonics	No	Yes
Selective harmonic mitigation modulation	Meet specific grid codes	No	No

The characteristics of the optimal modulations are summarized as follows.

A) Various optimization aims. The proposed optimal modulation strategies have various optimization aims. Essentially, the optimization aim is determined by specification of harmonic limitation provided by customers or utilities and additional filters. The specifications of harmonic limitations are different for different products and different installations. Some specifications only give the limitation of voltage THD. Some specify the limitation of current THD. Some even specify the limitations of each harmonic component. Passive or active filters that suppress some specific harmonics also affect the optimization goal. The optimization goal should be expressed in terms of designing optimal modulations to meet harmonic specification with minimum switching frequencies, or minimum voltage levels, or minimum additional filters. Due to various harmonics and system specifications, researchers found out that it is different to develop a universal optimal modulation strategy to meet all applications. Most researchers simplify the problems and focus on the optimal modulations that eliminate lower order harmonics. This is because 1) lower order harmonics are difficult to be suppressed by filters; 2) traditional multilevel SPWM and space vector modulation also eliminate lower order harmonics; 3) it is straightforward to eliminate lower order harmonics by the optimal modulations, like (1.10) or (1.11). Recently, researchers realized that the optimization goal should be based on harmonic specification. In [95], an optimal modulation has been proposed to meet specific grid

codes that specify the limitation of individual harmonics. In the future, the customized optimal modulation for the specific harmonic requirement is promising.

B) Low switching frequencies. To achieve the same harmonic performance, the switching frequencies with the optimal modulations are much lower than those with popular multilevel SPWM or space vector modulations. Using an example of a seven-level cascade multilevel inverter, to eliminate third – 17th harmonics, the switching frequencies with optimal modulations are 120 Hz, while those with multilevel SPWM are more than 180 Hz.

C) Rely on look-up tables. The implementation of most optimal modulations relies heavily on a large look-up table. For most optimal modulations, the switching angles corresponding to a modulation index can be obtained by solving a non-linear and transcendental equation set. Solving the equation set is very time-consuming. It cannot be done by a microprocessor or a DSP in real-time. It can only be done by an offline computer offline. Switching angles obtained offline have to be stored in a look-up table in a microprocessor or a DSP. The data of switching angles stored in the look-up table increases if the required resolution of the fundamental component of the voltage increases.

D) Problems for the inverters with variable voltage steps. Most optimal modulations are only suitable for the inverter with variable voltage steps. Few modulations [93, 94] have been proposed for the inverters with variable voltage steps.

Implementation of the proposed algorithm encounters serious problems due to the huge size of look-up tables. Calculation for obtaining the switching angles is very time-consuming. It can only be done by an offline computer. The solved switching angles have to be stored in a look-up table. Each combination of different voltage steps and modulation indexes will correspond to a set of switching angles in the look-up tables. Thus, the size of the look-up tables will be huge and it is practically impossible to implement it using normal microprocessors or DSPs. Therefore, the inverters with variable voltage steps require optimal modulations in which the switching angles can be calculated in real-time.

E) Worse voltage qualities during the fault situation. In optimal modulations aforementioned for multilevel inverters, the switching angles are optimized for certain objectives under an important assumption. The number of voltage levels is fixed. However, when one or more power modules in the multilevel levels fail, the multilevel inverter may continue to function but with the loss of some voltage levels. The voltage quality will become much worse because of reduced voltage levels. For example, switching angles are calculated to eliminate lower order harmonics for a multilevel inverter. If the multilevel inverter loses two voltage levels, the lower order harmonics will increase substantially. One solution is to calculate more switching angles for reducing voltage levels. But this will increase the size of look-up tables dramatically.

In this thesis, two new optimal modulations will be proposed. They are *minimal THD modulation* and *optimal combination modulation*.

1.7.1.1 Minimal THD modulation

The optimization aim for optimal modulations should be expressed in terms of designing optimal modulations to meet specific harmonic specifications with minimum switching frequencies, or minimum voltage levels, or minimum additional filters. Some harmonic specifications only give the limitation of voltage THD. Some specify the limitation of current THD. Some even specify each harmonics limitations. Elimination of lower order harmonics that most researchers focus on actually don't hit above harmonic specifications. The selective harmonic mitigation modulation proposed in [95] deals with the harmonic specification in which each harmonic limitation is specified. Now, however, no optimal modulation has been proposed for the harmonic specification that only gives the limitation of voltage THD. The minimal THD modulation will deal with the former. The optimization goal of the minimal THD modulation is the minimization of voltage THD.

One crucial drawbacks of the previous optimal modulations is that the optimal switching angles could not be calculated in real-time and one had to rely on look-up tables with the pre-calculated angles. In the minimal THD modulation, the switching angles can be calculated in real-time. Therefore, the implementation does not rely on the look-up table.

Another crucial drawback of previous optimal modulations is that they are not suitable for the multilevel inverters with unequal or variable voltage steps. Here, the minimal THD modulation is not only suitable for the multilevel inverter with equal voltage steps, but also for the multilevel inverter with unequal and variable voltage steps.

In short, the minimal THD modulation has three advantages. They are minimization of voltage THD, real-time calculation, and compatibility using the inverter with unequal or variable voltage steps.

1.7.1.2 Optimal combination modulation

The other new optimal modulation, the optimal combination modulation, is also presented for a 10 MVA STATCOM application. It is kind of a customized optimal modulation based on grid codes (IEEE 519 standard). The switching frequencies have been determined by the thermal capability of converters. Moreover, the inverter is required to continue functioning even if it loses some voltage levels. With the optimal combination modulation, the voltage quality will not decrease much due to reduced voltage levels.

1.7.2 Advanced control of multilevel inverter

In this thesis, I am focusing on the control of the cascade multilevel inverter for the STATCOM. [3, 113, 114]. Various controls of cascade multilevel inverter for the

STATCOM have been studied and presented in [48, 49, 73, 88, 111, 112, 115-119]. However, there are still two challenges remaining. They are DC capacitor voltage balancing and ride through capability.

1.7.2.1 DC capacitor voltage balancing

One challenging problem of the cascade multilevel inverter based STATCOM is the imbalance of the DC capacitor voltages [120, 121]. The imbalance is caused by:

1) Different switching patterns for different H-bridges [116, 122];

2) Parameter variations of active and passive components inside H-bridges;

3) Control resolution [123].

To achieve higher voltage quality, the switching patterns are usually different for different H-bridges in a phase. The differences of switching patterns mean that H-bridges cannot equally share the exchanged power with the power system [116]. This causes uneven charging of DC capacitors [92]. The parameter variations of components inherently cause different power losses of H-bridges.

The imbalance of DC capacitor voltages will degrade the quality of the voltage output. In severe cases, this could lead to the complete collapse of the power-conversion system [92]. Moreover, it will cause excessive voltages across the devices and an imbalance of switching losses [123].

An adequate control strategy for avoiding the imbalance of DC capacitor voltages must meet four requirements.

1) It can balance voltages when the STATCOM works in the capacitive mode, the inductive mode and the standby mode;

2) The impact on voltage quality should be as small as possible;

3) It can balance voltages when components of H-bridges have parameter variations;

4) It can balance voltages when H-bridges switch with different switching patterns.

The methods presented in [110, 124] balance the voltages by swapping switching patterns. Due to no feedback control, they may not meet the third requirement. The feedback control strategies presented in [11, 48, 119, 123, 125] reshape the output voltages of H-bridges based on the feedback signals of the DC capacitor voltages. Thus, they meet the third and fourth requirement. However, the papers [11, 48, 119, 123, 125] do not show if the control strategies work in different operating modes. Also, the impact on voltage qualities was not analyzed.

The modeling of the multilevel converter benefits the design of control systems [115, 126]. I propose a new feedback control strategy for balancing individual DC capacitor voltages based on the detailed small-signal model. The small-signal model leads us to find out an efficient way for reshaping the voltage to achieve the control goal. The transfer function for an individual DC capacitor voltage derived from the small-signal model shows that the gain of the transfer function keeps changing. By introducing a compensator into the control loop to cancel the variation of gain, the

controller works well in the whole operating region. This includes the capacitive mode, the inductive mode and the standby mode.

1.7.2.2 Ride through capability

For the control of the cascade multilevel inverter for STATCOM, besides DC capacitor voltage balancing, there is another important issue to consider. This is the fault ride through capability of the multilevel inverter. The fault ride through is regarded as one of the main challenges in the design of control and protection of the wind turbines in wind farms [134-139]. Although the definition of fault ride-through varies, the German Transmission and Distribution (E.ON) regulation is likely to set the standard [140], which stipulates that a wind turbine in a wind farm should remain stable and connected during certain fault conditions [141]. The standard stated in the German Transmission and Distribution Utility (E.ON) regulation stipulates that a wind turbine should remain stable and connected during the fault while voltage at the coupling point drops to 15% of nominal value (i.e., a drop of 85%) for a period of 150 ms. Only when the grid voltage drops below the curve is the turbine allowed to disconnect from the grid.

Serving the wind farm, the multilevel inverter based STATCOM is not allowed to trip before the wind turbine is disconnected. If the STATCOM trips before the wind turbines trip, the bus voltage will drop more due to the absence of the STATCOM, which in turn might trip the wind turbines.

In the reference [138], the authors state that the LVRT (Low Voltage Ride Through) capability of wind turbines can be enhanced by the use of a STATCOM. However, we think the assumption is that the STATCOM itself has enough ride-through capability. Therefore, one objective is to develop advanced controls to enhance the ride-through capability of the cascade multilevel inverter based STATCOM

1.8 Major contributions

The major contributions are

- Develop a new series of minimal THD modulation for multilevel inverters, including 1) Optimal values of switching angles for given DC voltages and modulation index, 2) Optimal values of DC voltages and switching angles for a given modulation index, and 3) Optimal values of DC voltages, switching angles and modulation index. The first one can be implemented in real-time.
- Propose a new optimal combination modulation based on grid codes (IEEE 519 standard).
- Develop a new feedback control strategy for balancing individual DC capacitor voltages in the cascade multilevel inverter based STATCOM, based on the detailed small signal model. The controller can work well in all operating regions that include: the capacitive mode, the inductive mode and the standby

mode. The impact of the individual DC voltage controller on the voltage quality is small.

- Propose solutions for enhancing ride-through capability of the cascade multilevel inverter based STATCOM during faults conditions.

Chapter 2. Minimal THD modulation

The minimal THD modulation is designed for the staircase modulation as shown in Figure 1.20. Actually, only the staircase modulation will result in the minimal THD. More notches in the waveforms will deteriorate the THD. Note the proposed minimal THD modulation is also for the multilevel inverter with unequal or variable voltage steps.

2.1 Optimal values of switching angles for given DC voltages and modulation index

The algorithm presented in this section is applied in most cases. DC voltages might be stable or keep changing. DC voltages could be equal or not. The modulation block will monitor DC voltages and the updated modulation index, and then figure out a set of switching angles based on the presented algorithm. Note that these calculations are rapid. Therefore the switching angles can be figured out in real-time. No look-up tables are needed.

2.1.1 Problem

We begin by recalling some notions. Figure 1.20 shows the output voltage of a ($2s + 1$) level multilevel inverter with the staircase modulation. There are s positive voltage

steps, s negative voltage steps and a zero voltage level. $E_1 \ldots E_s$ indicates the voltage steps as shown in Figure 1.20. Note that $E_1 \ldots E_s$ may not be equal and may vary. The quantities $\theta_1 \ldots \theta_s$ are the switching angles that indicate the on or off instant of switches inside the inverter.

For the waveform shown in Figure 1.20, by applying Fourier series analysis, the amplitude of any odd nth harmonic can be expressed as (1.7). The modulation index, m, is defined as (1.8). The voltage THD is defined as (1.9).

Now we are ready to state the problem: Devise a real-time algorithm for

Input : $E_1 \ldots E_s$, and m

Output : $\theta_1 \ldots \theta_s$ such that THD is minimum.

Remarks: The inputs $E_1 \ldots E_s$ come from DC capacitor voltages or the additions and subtractions of DC capacitor voltages in the inverter [11, 26, 96]. The DC capacitor voltages are measured by voltage sensors. The input m is the determined by a controller in a practical multilevel inverter system. The outputs $\theta_1 \ldots \theta_s$ are used by the inverter to control the switches.

Remarks: It is important to note that minimizing voltage THD is desirable in some applications, but not a panacea for all applications. However, the minimum voltage THD is desired for certain other applications [89, 90, 97-101]. Therefore we believe that the problem of minimizing voltage THD is, though not a panacea for all the applications, still an important one to address.

2.1.2 Algorithm

Our proposed algorithm for the problem:

Input : $E_1 \ldots E_s$, and m

Output : $\theta_1 \ldots \theta_s$ such that THD is minimum.

The algorithm consists of the following two steps:

Step 1. Determine ρ by solving the equation

$$\sum_{k=1}^{s} e_k \sqrt{1-(\mu_k \cdot \rho)^2} = m \tag{2.1}$$

where

$$e_k = \frac{E_k}{\sum_{i=1}^{s} E_l} \tag{2.2}$$

$$\mu_k = \frac{\sum_{i=1}^{k} E_i - E_k / 2}{\sum_{i=1}^{s} E_i - E_s / 2} \tag{2.3}$$

Step 2. Determine switching angles by evaluating

$$\theta_k = \arcsin(\mu_k \rho) \quad k = 1, 2, \ldots, s \tag{2.4}$$

2.1.3 Proof

In this section, we will first prove mathematically that the proposed algorithm outputs the switching angles that minimizes the voltage THD. Then the computational complexity is analyzed to prove that the algorithm can be done in *real-time* by normal microprocessors or DSPs.

A) Proof of minimality of the voltage THD

We will prove that the proposed algorithm outputs the switching angles that minimize the voltage THD. The proof technique is substantially different from (in fact better than) the one used in [102] in that it uses a much better/simpler expression for THD.

Without losing generality, assume that $E_1 + E_2 + \cdots + E_s = 1$. The output voltage of the inverter as shown in Figure 1.20 can be expressed as

$$v = \sum_{k=1}^{s} E_k (u_{\theta_k} - u_{\pi-\theta_k} - u_{\pi+\theta_k} + u_{2\pi-\theta_k}) \tag{2.5}$$

where u is a unit step function. By Fourier series expansion, we obtain that

$$v = \sum_{n=1,3,5,\ldots} V_n \sin n\theta \tag{2.6}$$

where

$$V_n = \frac{4}{\pi n} \sum_{l=1}^{s} E_l \cos n\theta_l \tag{2.7}$$

The modulation index, m, is defined by

$$m = \frac{\pi}{4} V_1 = \sum_{l=1}^{s} E_l \cos \theta_l \tag{2.8}$$

The THD is expressed as d

$$d = \sqrt{\frac{\sum_{n=3,5,\ldots} V_n^2}{V_1^2}} \tag{2.9}$$

The next lemma provides a simpler/better expression for THD.

Lemma 1 The THD is given by

$$d = \sqrt{\frac{\pi}{4m^2}\sum_{l=0}^{s}(E_1+\cdots+E_l)^2(\theta_{l+1}-\theta_l)-1} \tag{2.10}$$

where $\theta_0 = 0$ and $\theta_{s+1} = \pi/2$.

Proof. Observe

$$\int_0^{\frac{\pi}{2}} v^2 d\theta = \int_0^{\frac{\pi}{2}} (\sum_{n=1,3,5,\ldots} V_n \sin n\theta)^2 d\theta = \frac{\pi}{4}\sum_{n=1,3,5,\ldots} V_n^{\,2} \tag{2.11}$$

$$\int_0^{\frac{\pi}{2}} v^2 d\theta = \sum_{l=0}^{s}\int_{\theta_l}^{\theta_{l+1}} (E_1+\cdots+E_l)^2 d\theta = \sum_{l=0}^{s}(E_1+\cdots+E_l)^2(\theta_{l+1}-\theta_l) \tag{2.12}$$

Hence

$$\begin{aligned} d &= \sqrt{\frac{\frac{4}{\pi}\sum_{l=0}^{s}(E_1+\cdots+E_l)^2(\theta_{l+1}-\theta_l)-V_1^2}{V_1^2}} \\ &= \sqrt{\frac{4}{\pi V_1^2}\sum_{l=0}^{s}(E_1+\cdots+E_l)^2(\theta_{l+1}-\theta_l)-1} \end{aligned} \tag{2.13}$$

Further simplifying, we get

$$\begin{aligned} d &= \sqrt{\frac{4}{\pi(\frac{4}{\pi}m)^2}\sum_{l=0}^{s}(E_1+\cdots+E_l)^2(\theta_{l+1}-\theta_l)-1} \\ &= \sqrt{\frac{\pi}{4m^2}\sum_{l=0}^{s}(E_1+\cdots+E_l)^2(\theta_{l+1}-\theta_l)-1} \end{aligned} \tag{2.14}$$

The proof of the lemma is completed.

Under the constraint as shown in (2.8), we will minimize d^2 (instead of d since it is equivalent and simpler). From the Lagrange multiplier method, we obtain the following system of equation:

$$\frac{\partial}{\partial \theta_k} d^2 = \lambda \frac{\partial}{\partial \theta_k}\left(\frac{\pi}{4} V_1 - m\right) \tag{2.15}$$

The nth harmonic, V_n, is shown as (2.7). Note that

$$\text{RHS} = \lambda \frac{\partial}{\partial \theta_k} \frac{\pi}{4} V_1 = \lambda \frac{\partial}{\partial \theta_k} (\textstyle\sum_{i=1}^{s} E_i \cos\theta_i) = -\lambda E_k \sin\theta_k \tag{2.16}$$

Note also that

$$\begin{aligned} \text{LHS} &= \frac{\partial}{\partial \theta_k} \left(\frac{\pi}{4m^2} \sum_{l=0}^{s} (E_1 + \cdots E_l)^2 (\theta_{l+1} - \theta_l) - 1\right) \\ &= \frac{\pi}{4m^2} \left((\sum_{l=1}^{k-1} E_l)^2 - (\sum_{l=1}^{k} E_l)^2\right) = \frac{-2\pi}{4m^2} E_k \left(\sum_{l=1}^{k} E_l - \frac{E_k}{2}\right) \end{aligned} \tag{2.17}$$

By equating LHS and RHS, we have

$$\begin{aligned} &\frac{-2\pi}{4m^2} E_k \left(\sum_{l=1}^{k} E_l - \frac{E_k}{2}\right) = -\lambda E_k \sin\theta_k \\ &\sin\theta_k = \frac{\pi\left(\sum_{l=1}^{k} E_l - \frac{E_k}{2}\right)}{2\lambda m^2} = \frac{\sum_{l=1}^{k} E_l - \frac{E_k}{2}}{\sum_{l=1}^{s} E_l - \frac{E_s}{2}} \frac{\pi\left(\sum_{l=1}^{s} E_l - \frac{E_s}{2}\right)}{2\lambda m^2} \end{aligned} \tag{2.18}$$

$$\sin\theta_k = \frac{\sum_{l=1}^{k} E_l - \frac{E_k}{2}}{\sum_{l=1}^{s} E_l - \frac{E_s}{2}} \rho \tag{2.19}$$

where

$$\rho = \frac{\pi(\sum_{l=1}^{s} E_l - \frac{E_s}{2})}{2\lambda m^2} \tag{2.20}$$

The above derivation is based on the assumption $E_1 + E_2 + \cdots + E_s = 1$. When $E_1 + E_2 + \cdots + E_s \neq 1$, the equation (2.19) is still true, but ρ is expressed as

$$\rho = \frac{\pi(\sum_{l=1}^{s} E_l - \frac{E_s}{2})}{2\lambda m^2 \sum_{l=1}^{s} E_l} \tag{2.21}$$

From (1.7), (1.8) and (2.19), we can derive equation (2.1) by which the value of ρ can be determined.

B) Proof of real-time

We will illustrate that the proposed algorithm outputs the optimal switching angles in real-time. The Newton-Raphson method is used to solve (2.1). From (2.1), we can derive that

$$f(\rho) = \sum_{k=1}^{s} (e_k \sqrt{1-(\mu_k \cdot \rho)^2}) - m \tag{2.22}$$

$$f'(\rho) = \sum_{k=1}^{s} \frac{-e_k \mu_k{}^2 \rho}{\sqrt{1-(\mu_k \cdot \rho)^2}} \tag{2.23}$$

The value of ρ after jth iteration, ρ_j, can be expressed as

$$\rho_j = \rho_{j-1} - f(\rho_{j-1}) / f'(\rho_{j-1}) \tag{2.24}$$

The flow chart of the algorithm is shown in Figure 2.1. The input signals are E_k (the amplitudes of voltage steps), m (modulation index) and ρ_0 (initial value of ρ). In Figure 2.1, m_c is a calculated modulation index during the iteration. If the difference between m_c and m is small enough, the iteration will end and the resulting switching angles are precise enough.

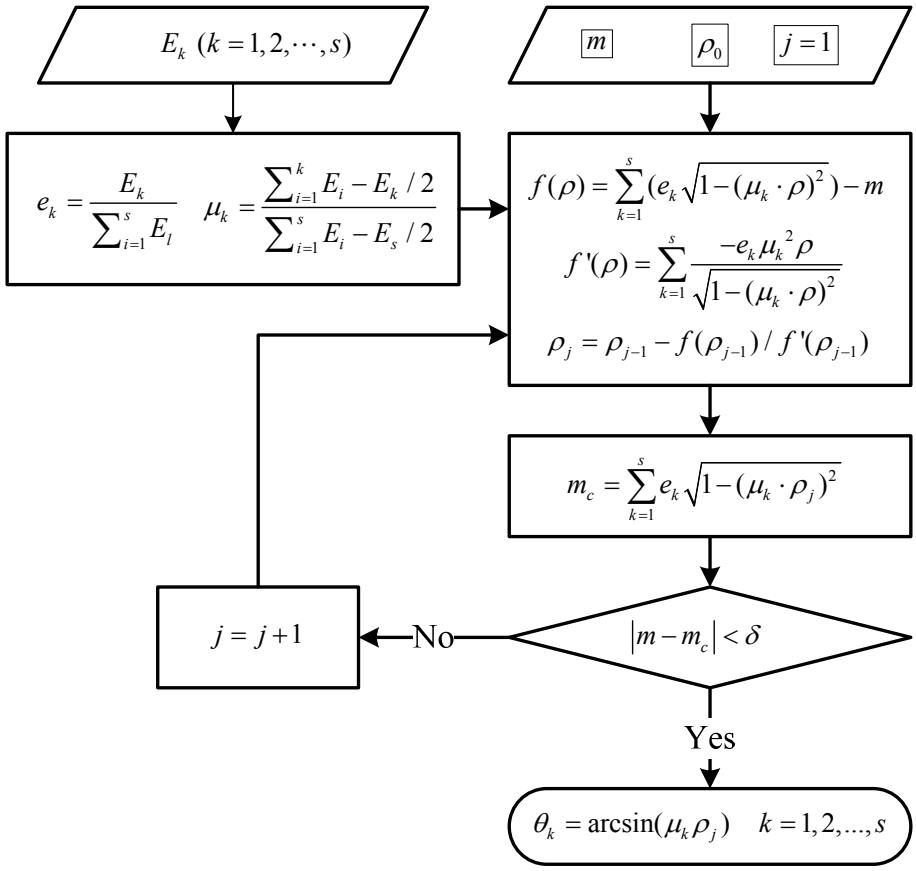


Figure 2.1. Flow chart of the algorithm

The first analysis is based on the assumption that the modulation index or the voltage steps change randomly. The ρ_0 in Figure 2.1 is set as 0.9. In the case of the seven-level inverter, the errors of m, $|m\text{-}m_c|$, are less than 0.0005 after four iterations for all combinations of different modulation indexes and the voltage steps.

The second analysis is for practical applications. In most of practical applications, the modulation index, m, changes gradually. The voltage steps change slowly due to the limitation of charging or discharging currents for DC capacitors.

Use the example of a seven-level inverter. The voltage steps are E_1, E_2 and E_3. Suppose, in T_{tr}, m changes from 0.64 to 0.93, E_2 changes from 1 pu to 0.95 pu, E_3 changes from 1 pu to 0.9 pu, linearly. E_1 is kept to be 1 pu. The sampling frequency is 10 kHz. Take the example that T_{tr} is 5.8 ms. Thus, m increases around 0.005 at the next calculation during the next sampling period. The first calculation is for the case where m is 0.64. At this calculation, the initial value of ρ for iteration is 0.9. Four time iterations are used to solve ρ for the m of 0.64. The next calculation is for the m of 0.645. The initial value of ρ for the iteration is set as the solved ρ in the case where m is 0.64. Note that only one time of iteration is used to solve ρ in the case where m is 0.645. Then, in the case where m is 0.65, the initial value of ρ for iteration is set as the solved ρ in the case where m is 0.645 and one time of iteration is applied to gain ρ in the case where m is 0.65. By this way, all values of ρ corresponding to 0.645, 0.65, 0.655, … , 0.93 are calculated. In short, the initial value of ρ is set as the calculated ρ by the

calculation in the last sampling period and one time of iteration is enough to get the precise value of ρ. The error of m, $|m\text{-}m_c|$, is used to measure the precision of calculation. The waveforms of m, E_1, E_2, E_3 and the error of m, during the 5.8 ms, are shown in Figure 2.2. The maximum error of m is 0.00022 as shown in Figure 2.3.

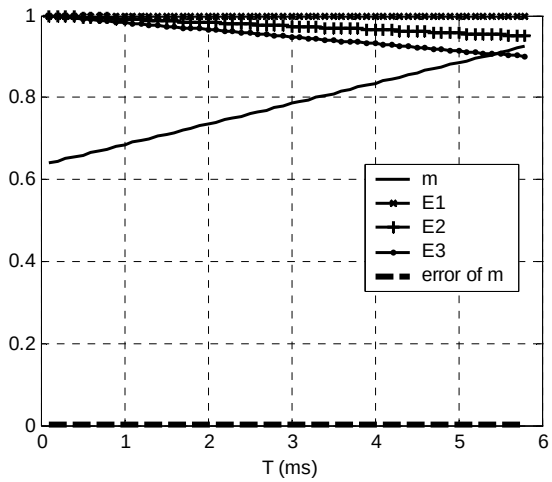


Figure 2.2. Waveforms of m, voltage steps and the error of m during 5.8 ms

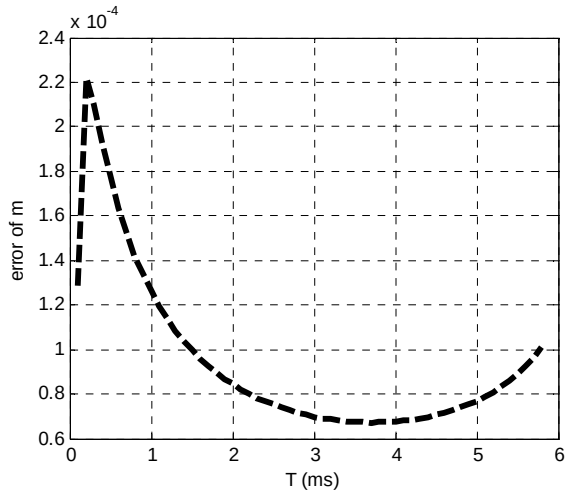


Figure 2.3. Detail of the error of *m* during 5.8 ms

Figure 2.4 shows the relationship between T_{tr} and the maximum errors of *m* for three cases. Case 1: in T_{tr}, *m* changes from 0.64 to 0.93, E_2 changes from 1 pu to 0.95 pu, E_3 changes from 1 pu to 0.9 pu, linearly, and E_1 is 1 pu. Case 2: in T_{tr}, *m* changes from 0.64 to 0.93, E_2 changes from 1 pu to 0.8 pu, E_3 changes from 1 pu to 0.6 pu, linearly, and E_1 is 1 pu. Case 3: In T_{tr}, *m* changes from 0.64 to 0.93, E_2 changes from 1 pu to 0.6 pu, E_3 changes from 1 pu to 0 pu, linearly, and E_1 is 1 pu. The sampling frequency is 10 kHz. As shown in Figure 2.4, if T_{tr} is large than 2.7 ms, the maximum errors of *m* are less than 0.001, which means the calculated results are precise enough.

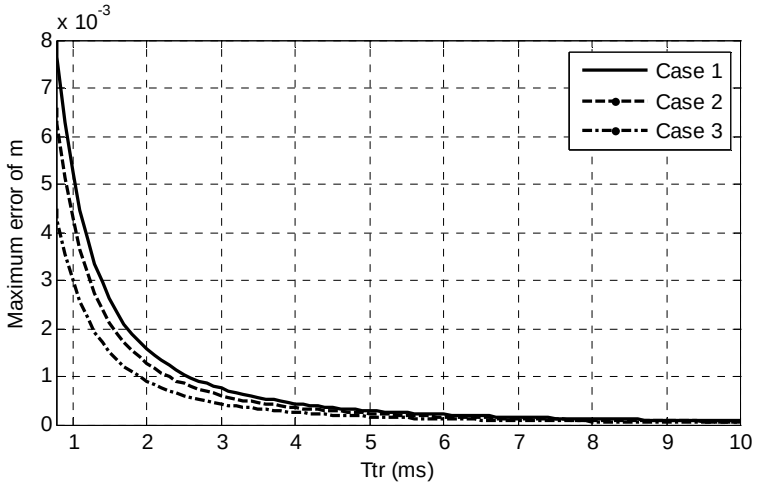


Figure 2.4. Relationship between T_{tr} and the maximum errors of m

The above analysis is for the seven-level inverter. The calculating accuracy and converging speed for the inverter with more levels is almost the same as those for the seven-level inverter. The implementation of the algorithm that is summarized here is based on the 10 kHz sampling frequency. Application I: the changing rate of the modulation index is less than 0.1/ms and the changing rates of voltage steps are less than 0.37 pu/ms. In application I, one iteration can result in precise results. In application II: the changing rates of the modulation index and voltage steps are larger than those in application I. In application II, when the larger changing rates are detected, iterations up to four times are needed to get precise results.

Most of practical applications belong to the application I. Therefore, computing complexity is analyzed based on one time of iteration. Only multiplication, division, square root and arcsin operations are considered since they require most of the

computing time. Based on (2.2), (2.3), (2.22), (2.23) and (2.24), the time needed for one iteration is expressed as

$$T_{iteration} = (3s+2)\cdot T_{multiplication} + T_{rootsquare} + (s+5)T_{divison} \tag{2.25}$$

where $T_{multiplicaton}$, $T_{rootsquare}$, $T_{division}$ are time costs of multiplication, root square and division operations, respectively.

Thus, for a (2s + 1) level multilevel inverter, the total computational complexity of the algorithm is just

$$T_{solve} = (4s+2)\cdot T_{multiplication} + T_{rootsquare} + (s+5)T_{divison} + s\cdot T_{\arcsin} \tag{2.26}$$

where T_{arcsin} is time cost of arcsin operation. In a case of a seven-level inverter, s is three. The computing complexity is just 14 multiplications, 8 divisions, a root square and 3 arc-sin operations. Such computing complexity can be easily handled by common microprocessors or DSPs in real-time. The experimental results for a seven-level multilevel inverter show that the time cost for the calculation is only 24 μs by using a DSP with a clock frequency of 225 MHz.

2.1.4 Discussions

A) Comparison with other optimal modulations

Table 2.1 shows the comparison between the minimal THD modulation and other optimal modulations.

Table 2.1. Comparison between the minimal THD modulation and other optimal modulations

Modulation	Optimization aim	Real time calculation	For varying voltage steps
Minimal THD modulation	Minimization of voltage THD	Yes	Yes
Staircase modulation with elimination of lower order harmonics	Elimination of lower order harmonics	No	No
Staircase modulation with equal voltage-second area	Voltage-second balance	Yes	No
Selective harmonic elimination PWM with equal voltage steps	Elimination of lower order harmonics	No	No
Selective harmonic elimination PWM with unequal voltage steps	Elimination of lower order harmonics	No	Yes
Selective harmonic mitigation modulation	Meet specific grid codes	No	No

The first item compared here is voltage THD. Because most previous optimal modulations are for equal voltage steps, the comparison of voltage THD here is under the assumption of equal voltage steps. In the case of the seven-level multilevel inverter with the step modulation, four voltage THDs gained by different methods are compared. The switching angles solved by the proposed algorithm are shown in Figure 2.5. The first THD is gained by the proposed method. The method [27, 82] by which the second THD is gained is to eliminate fifth and seventh order harmonics. The method by which the third THD is gained is to eliminate third and fifth order harmonics. The fourth THD is gained by the method proposed by Kang in [85]. Figure 2.6 and Figure 2.7 show the comparison results. Large values of the second and third THD suggest that the elimination of lower order harmonics cannot lead to the minimization of the THD. The Kang's method based on the theory of voltage second

balance [85] can achieve a small THD that is , however, still larger than the THD by the proposed method as shown in Figure 2.6 and Figure 2.7. Actually, the THD gained by the proposed method has been proven minimal by mathematical derivation aforementioned. Therefore, from the point of view of the voltage THD and the real-time implementation, the proposed algorithm is better than previous methods. As shown in Figure 2.6, the THD is the least when the modulation index is around 0.84, which indicates the modulation index in normal operation may be designed at 0.84.

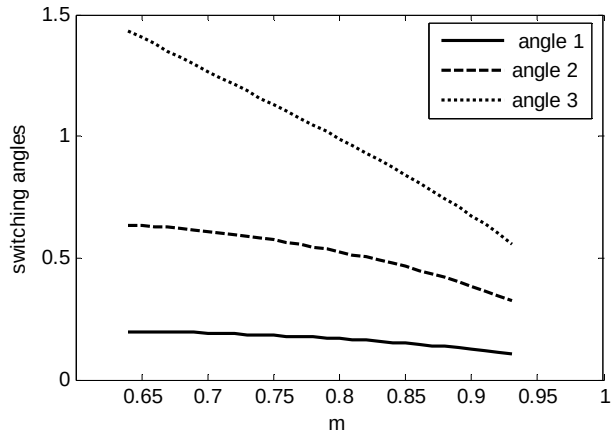


Figure 2.5. Switching angles with respect to modulation indexes

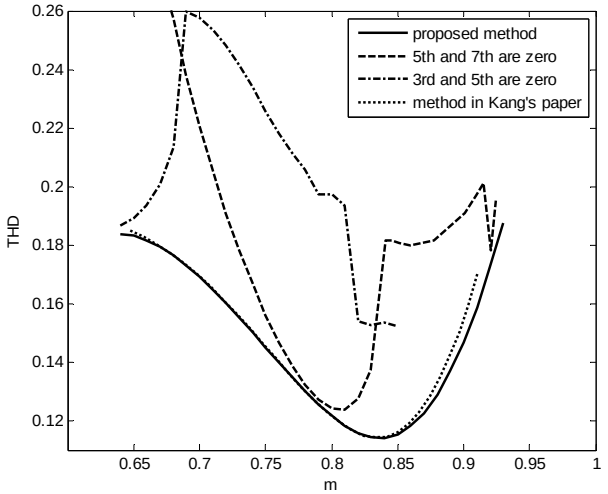


Figure 2.6. Comparison of THD between the proposed method and previous methods

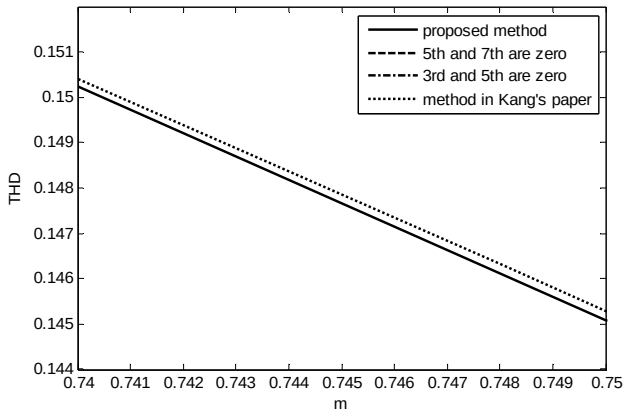


Figure 2.7. Detail of comparison of THD between the proposed method and the previous method

The second item discussed here is the ability of real-time calculation. The computational complexity of the algorithm in [85, 88, 102] and the proposed algorithm here is small enough that normal microprocessors and DSPs can finish the calculation

in real-time. It means that we don't rely on look-up tables. This is very important for unequal or varying voltage steps. If the look-up tables are used for the multilevel inverters with varying voltage steps, each combination of different voltage steps and modulation indexes will correspond to a set of switching angles in the look-up table. Thus, the size of the look-up table will be huge and it is impossible to implement it practically using normal microprocessors or DSPs.

The algorithms presented in [88, 93, 94] and the proposed algorithm here address the situations with unequal or varying voltage steps. The varying voltages of DC sources result in the varying voltage steps. In the inverter proposed in [96], the voltage steps are intrinsically unequal and varying. The real-time calculating ability of the proposed algorithm leads to the elimination of huge look-up tables. Therefore, the algorithm is very promising for this application with unequal or varying voltage steps.

B) Improved voltage THD by the proposed algorithm for multilevel inverter with unequal voltage steps

The algorithm presented in [102] and the proposed algorithm focus on obtaining the minimal voltage THD. The algorithm in [102] is for multilevel inverters with identical voltage steps. The algorithm here is an extension of the algorithm in [102]. It uses the information of measured voltage steps to regulate switching angles to get the minimal voltage THD. This is for a multilevel inverter with unequal or varying voltage steps. So, the comparison between the algorithm in [102] and the proposed algorithm

here is presented to show the improvement of the voltage THD with the proposed algorithm for a multilevel inverter with unequal voltage steps.

The comparisons are carried out for the following three cases in a seven-level multilevel inverter: 1) E_2 and E_3 drop to 0.7 pu and 0.5 pu, respectively; 2) E_2 and $E3$ drop to 0.8 pu and 0.6 pu, respectively; and 3) E_2 and $E3$ drop to 0.9 pu and 0.8 pu, respectively. E_1 is 1 pu in above three cases.

Figure 2.8, Figure 2.9 and Figure 2.10 show the THD comparison results between the previous algorithm in [102] and the proposed algorithm here for the above three cases respectively. The voltage THD obtained by the proposed algorithm is smaller than that by the algorithm in [102], especially in the range of low modulation index. We can also find out that the THD improvement is prominent when the voltage steps have large differences.

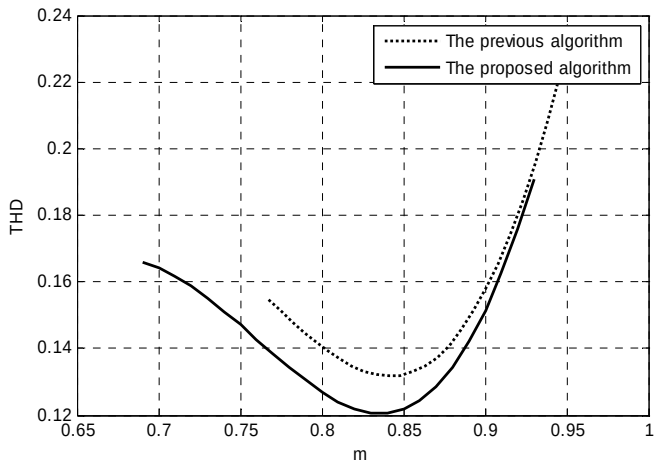


Figure 2.8. Comparison of THDs when E_1, E_2 and E_3 are 1 pu, 0.7 pu and 0.5 pu, respectively.

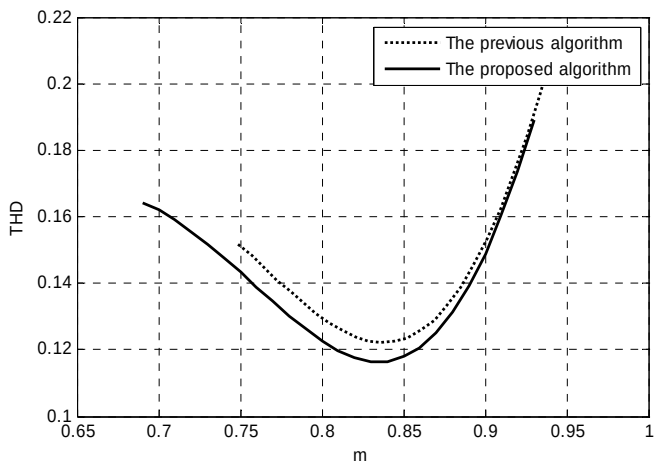


Figure 2.9. Comparison of THDs when E_1, E_2 and E_3 are 1 pu, 0.8 pu and 0.6 pu, respectively.

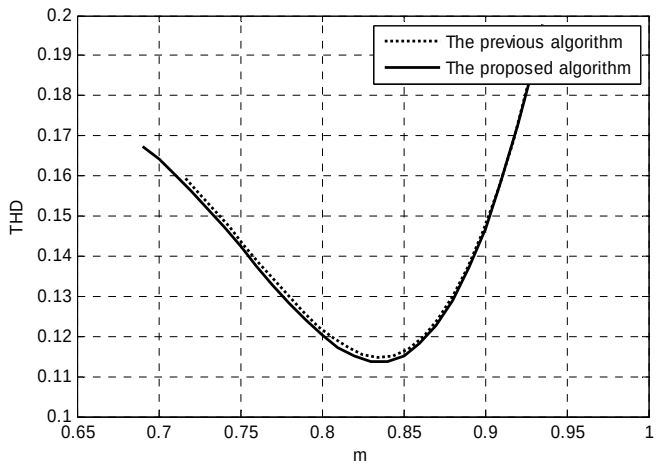


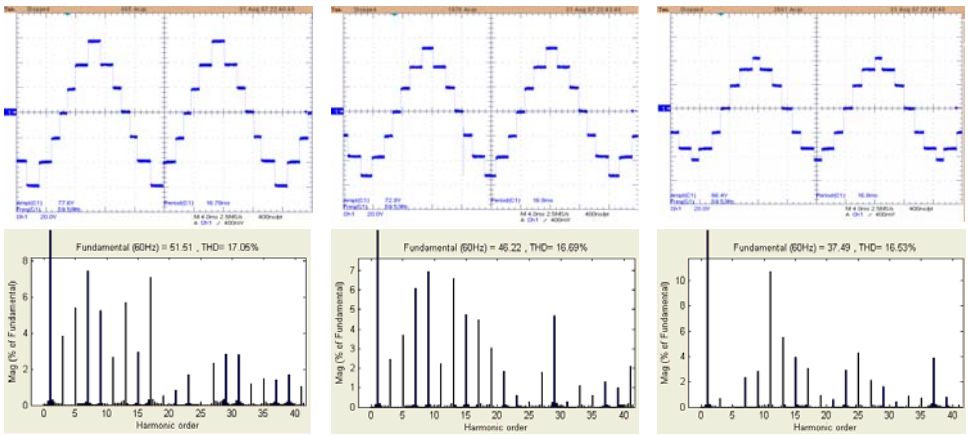
Figure 2.10. Comparison of THDs when E_1, E_2 and E_3 are 1 pu, 0.9 pu and 0.8 pu, respectively.

2.1.5 Experimental results

To verify the performance of the proposed method, a cascade multilevel inverter was developed in the laboratory. Three IGBT H-bridges are used to form a single-phase seven-level multilevel inverter. The model of IGBT module is PM50RAS120. The DC sources of the H-bridge are DC power supplies with output voltages ranging from 0 V to 30 V. The load is a 10 Ω resistor and a 7.5 mH inductor. A local controller controls an IGBT module through a drive board and optical fibers. The central controller is connected to three local controllers. The central controller includes a TMS320C6701 DSP board, an AED 106 FPGA daughter board and two PCI boards mounted with Altera FLEX 10k30A FPGA. A DSP calculates the switching angles

based on DC source voltages sampled by voltage sensors and the given modulation index with the 10 kHz sampling frequency.

The voltage THD generated by the proposed algorithm is minimal. This has been proven by a rigorous mathematic derivation. The experimental results in Figure 2.1, Figure 2.2 and Figure 2.3 show stable output voltage waveforms and their spectrums in the condition of no load. The measured THD as shown in Figure 2.1, Figure 2.2 and Figure 2.3 verify the calculated THD as shown in Figure 2.8, Figure 2.9 and Figure 2.10. Since the optimization aim is the minimization of THD, the lower order harmonics are not eliminated.

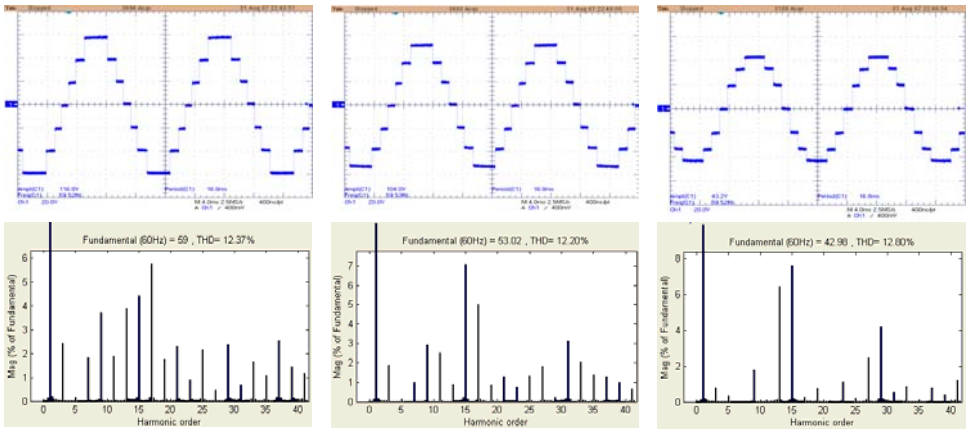


Ratio of DC voltages: 1:1:1
Angles: 0.19, 0.61, 1.27

Ratio of DC voltages: 1:0.9:0.8
Angles: 0.21, 0.66, 1.32

Ratio of DC voltages: 1:0.7:0.5
Angles: 0.26, 0.76, 1.44

Figure 2.11. The output voltages of the multilevel inverter (modulation index is 0.7)

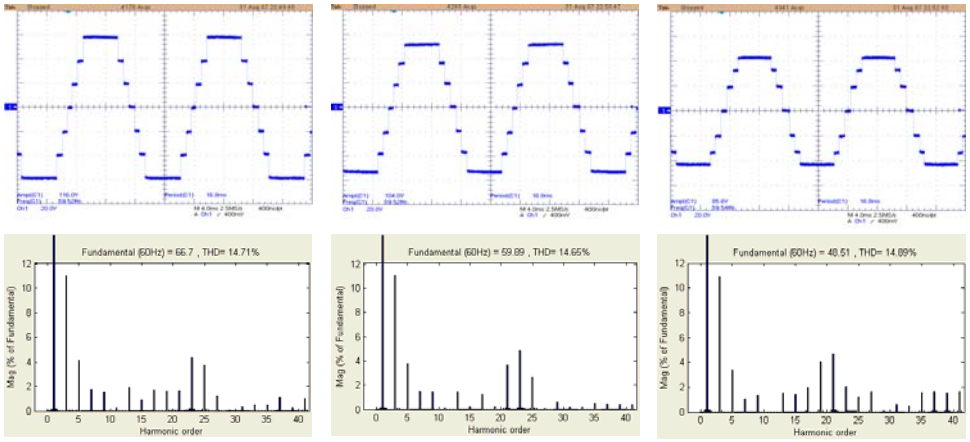


Ratio of DC voltages: 1:1:1
Angles: 0.17, 0.53, 0.99

Ratio of DC voltages: 1:0.9:0.8
Angles: 0.19, 0.57, 1.02

Ratio of DC voltages: 1:0.7:0.5
Angles: 0.23, 0.66, 1.09

Figure 2.12. The output voltage of the multilevel inverter (modulation index is 0.8)



Ratio of DC voltages: 1:1:1
Angles: 0.13, 0.38, 0.67

Ratio of DC voltages: 1:0.9:0.8
Angles: 0.14, 0.41, 0.69

Ratio of DC voltages: 1:0.7:0.5
Angles: 0.17, 0.48, 0.73

Figure 2.13. The output voltage of the multilevel inverter (modulation index is 0.9)

Figure 2.14, Figure 2.15, Figure 2.16 and Figure 2.17 show the dynamic performances when the modulation index and the frequency change. Figure 2.14 and Figure 2.15 show the output voltages and currents when the modulation index and the

frequency change slowly. As shown in Figure 2.14, the waveforms between two cursors are the output voltages and currents when the modulation index changes from 0.64 to 0.93 linearly and the frequency changes from 60 Hz to 87 Hz linearly in 58 ms. Figure 2.15 shows the case where the modulation index changes from 0.93 to 0.64 linearly and the frequency changes from 87 Hz to 60 Hz linearly in 58 ms. Figure 2.16 and Figure 2.17 show the cases while the modulation index and the frequency change quickly. Figure 2.16 shows the case where the modulation index changes from 0.64 to 0.93 linearly and the frequency changes from 60 Hz to 87 Hz linearly in 5.8 ms. Figure 2.17 shows the case where the modulation index changes from 0.93 to 0.64 linearly and the frequency changes from 87 Hz to 60 Hz linearly in 5.8 ms.

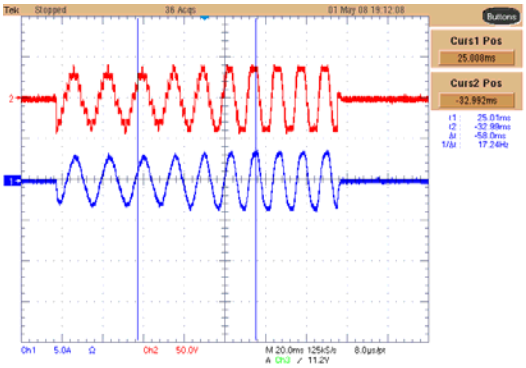


Figure 2.14. Output voltage and current of the inverter when modulation index changes from 0.64 to 0.93 and frequency changes from 60 Hz to 87 Hz in 58 ms
(CH1: current, CH2: output voltage)

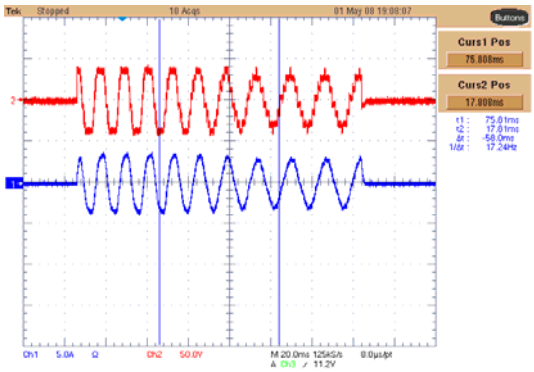


Figure 2.15. Output voltage and current of the inverter when modulation index changes from 0.93 to 0.64 and frequency changes from 87 Hz to 60 Hz in 58 ms
(CH1: current, CH2: output voltage)

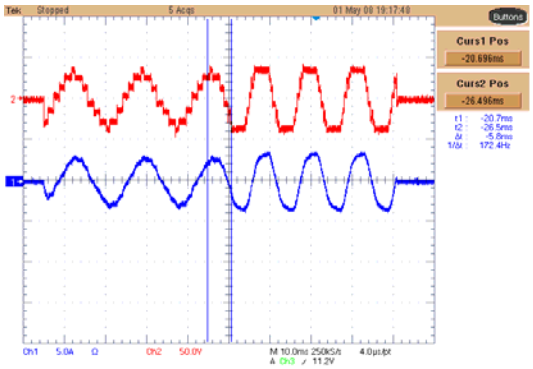


Figure 2.16. Output voltage and current of the inverter when modulation index changes from 0.64 to 0.93 and frequency changes from 60 Hz to 87 Hz in 5.8 ms
(CH1: current, CH2: output voltage)

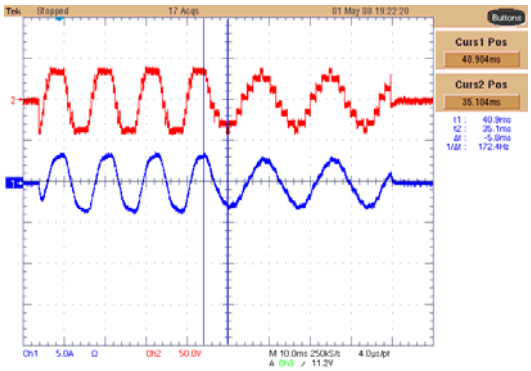


Figure 2.17. Output voltage and current of the inverter when modulation index changes from 0.93 to 0.64 and frequency changes from 87 Hz to 60 Hz in 5.8 ms
(CH1: current, CH2: output voltage)

Figure 2.18 and Figure 2.19 show the dynamic performances when a DC source voltage changes. Figure 2.18 shows the output voltage, the current and the changing voltage of the DC source when the DC source voltage changes from 0 V to 26 V. Figure 2.19 shows the case when the DC source voltage changes from 26 V to 0 V.

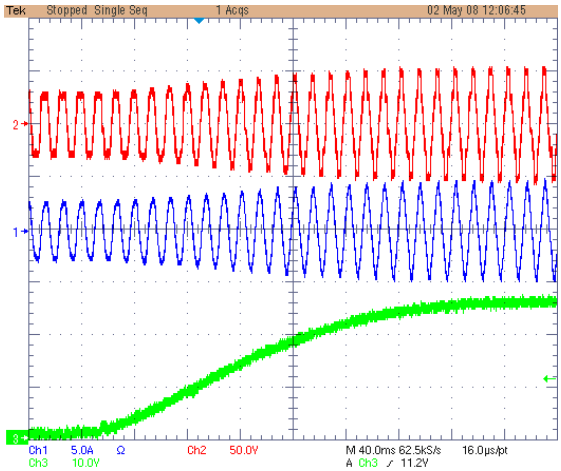


Figure 2.18. Output voltage and current of the inverter when one DC source voltage increase from 0V to 26 V
(CH1: current, CH2: output voltage, CH3: DC source voltage)

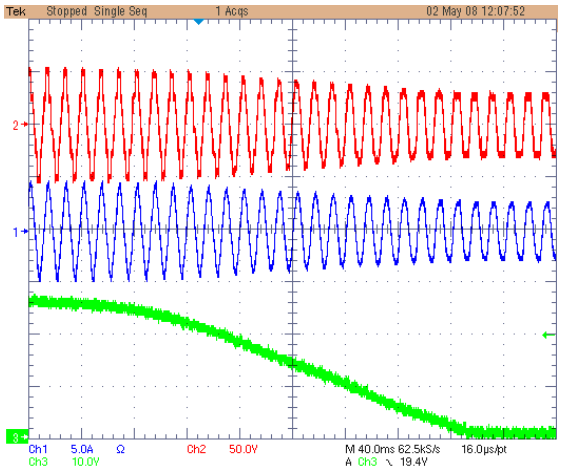


Figure 2.19. Output voltage and current of the inverter when one DC source voltage decrease from 26 V to 0V
(CH1: current, CH2: output voltage, CH3: DC source voltage)

The final item tested by the experiments is how long the calculations take when using the DSP. In experiments as shown in from Figure 2.14 to Figure 2.19, the

changing rate of the modulation index is less than 0.1 ms and the changing rates of voltage steps are much less than 0.37 pu/ms. Thus, one iteration is enough to get precise results. The DSP used in the experiment is TMS320C6713 with a clock frequency of 225 MHz. Based on testing results, around 5423 clocks are needed to finish the calculation. In other words, the calculation takes only 24 μs. Currently, the functions of ar-sin and square root used in the experiment are from libraries provided by DSP software. Within the total 5423 clocks, three times of arc-sin operations takes 2424 clocks and three times of square root operations takes 1152 clocks. In the future, the calculation time of the proposed algorithm could be decreased greatly by using a specialized algorithm for ar-sin and square root operations.

2.1.6 Summary

This section proposes an algorithm by which the switching angles are calculated in real-time for multilevel inverters with unequal or varying voltage steps under the staircase modulation. With the proposed algorithm, the voltage THD is minimized. This is proven by a rigorous mathematical derivation. A new expression of THD is presented to simplify the derivation significantly. The computational complexity is analyzed to show that the computing time is small enough that common microprocessor or DSP can handle it easily in real-time. Thus, the minimization of the voltage THD and the real-time calculating ability make the proposed algorithm

attractive in multilevel inverters with unequal or varying voltage steps. Experimental results verify the performance of the algorithm.

2.2 Optimal values of DC voltages and switching angles for a given modulation index

In last section, I presented an algorithm for calculating the switching angles with given values of DC voltages and a modulation index. The DC voltages are determined passively by environmental conditions, such as sunshine in a solar application. The modulation index is determined by the control system for a close-loop control.

In some advanced multilevel inverter configurations, the DC voltages can be controlled or fixed in advance. One case is that additional DC-DC converters are inserted into DC links to control DC link voltages in real time [99, 103]. The other case is that of a cascade multilevel inverter based SATCOM [104], in which DC link voltages can also be controlled.

Once we have the freedom of DC voltages, we can achieve less THD. This section will present the algorithm which, with a given modulation index, figures out the values of DC voltages and switching angles, such that THD is minimum. The calculated values of DC voltages are set as reference values of DC voltages in DC voltage control systems. The switching angles determine switching instants of power semiconductors.

2.2.1 Problem

For multilevel voltage with (2s+1) levels, devise an algorithm for

Input: m

Output: $E_1, \ldots E_s, \theta_1, \ldots$ and θ_s, such that THD is minimum.

2.2.2 Algorithm

Get $E_1, \ldots E_s, \theta_1, \ldots$ and θ_s by solving the following equations

$$\begin{aligned} p_k &= \frac{\cos\theta_k - \cos\theta_{k+1}}{\theta_{k+1} - \theta_k} \qquad (k = 1 \ldots s-1) \\ p_s &= \frac{q_1 \cos\theta_1 + \cdots + q_s \cos\theta_s}{m} \\ E_k &= \frac{q_k}{p_s} \qquad (k = 1 \ldots s) \end{aligned} \tag{2.27}$$

Where

$$\begin{aligned} q_k &= 2(p_k - \sin\theta_k) \\ p_k &= 2(\sin\theta_k - \sin\theta_{k-1} + \sin\theta_{k-2} - \cdots) \\ \theta_j &= 0 \quad (j \le 0) \end{aligned} \tag{2.28}$$

There are (4s) equations, and there are (4s) variables.

2.2.3 Proof

In order to simplify the presentation of the proof, we consider the case when s = 3. The generalization to arbitrary s is obvious. We will minimize $f = (4m^2/\pi)(d^2+1)$ under the constraints that $g = h = 0$ where

$$
\begin{aligned}
f &= E_1^2(\theta_2-\theta_1)+(E_1+E_2)^2(\theta_3-\theta_2)+(E_1+E_2+E_3)^2(\pi/2-\theta_3)\\
g &= E_1\cos\theta_1+E_2\cos\theta_2+E_3\cos\theta_3-m\\
h &= E_1+E_2+E_3-1
\end{aligned}
\tag{2.29}
$$

From Lagrange multiplier method, we obtain the following system of eight equations

$$
\begin{aligned}
\frac{\partial f}{\partial\theta_1} &= \lambda\frac{\partial g}{\partial\theta_1}+\mu\frac{\partial h}{\partial\theta_1}\\
\frac{\partial f}{\partial\theta_2} &= \lambda\frac{\partial g}{\partial\theta_2}+\mu\frac{\partial h}{\partial\theta_2}\\
\frac{\partial f}{\partial\theta_3} &= \lambda\frac{\partial g}{\partial\theta_3}+\mu\frac{\partial h}{\partial\theta_3}\\
\frac{\partial f}{\partial E_1} &= \lambda\frac{\partial g}{\partial E_1}+\mu\frac{\partial h}{\partial E_1}\\
\frac{\partial f}{\partial E_2} &= \lambda\frac{\partial g}{\partial E_2}+\mu\frac{\partial h}{\partial E_2}\\
\frac{\partial f}{\partial E_3} &= \lambda\frac{\partial g}{\partial E_3}+\mu\frac{\partial h}{\partial E_3}\\
g &= 0\\
h &= 0
\end{aligned}
\tag{2.30}
$$

There are eight unknown θ_1, θ_2, θ_3, E_1, E_2, E_3, λ and μ. By inserting f, g and h into the equations above, we obtain the following system of seven equations.

$$
\begin{aligned}
0.5E_1 &= 0.5\lambda\sin\theta_1\\
E_1+0.5E_2 &= 0.5\lambda\sin\theta_2\\
E_1+E_2+0.5E_3 &= 0.5\lambda\sin\theta_2\\
E_1(\theta_2-\theta_1) &= 0.5\lambda(\cos\theta_1-\cos\theta_2)\\
(E_1+E_2)(\theta_3-\theta_2) &= 0.5\lambda(\cos\theta_2-\cos\theta_3)\\
E_1\cos\theta_1+E_2\cos\theta_2+E_3\cos\theta_3 &= m\\
E_1+E_2+E_3 &= 1
\end{aligned}
\tag{2.31}
$$

Note that we have eliminated μ. From the first three equations, we obtain:

$$\begin{aligned} E_1 &= \lambda \sin\theta_1 \\ E_2 &= \lambda(\sin\theta_2 - 2\sin\theta_1) \\ E_3 &= \lambda(\sin\theta_3 - 2\sin\theta_2 + 2\sin\theta_1) \end{aligned} \tag{2.32}$$

By putting these into the remaining equations and simplifying, we obtain:

$$\begin{aligned} &2\sin\theta_1 = \frac{\cos\theta_1 - \cos\theta_2}{\theta_2 - \theta_1} \\ &2(\sin\theta_2 - \sin\theta_1) = \frac{\cos\theta_2 - \cos\theta_3}{\theta_3 - \theta_2} \\ &(\sin\theta_1)\cos\theta_1 + (\sin\theta_2 - 2\sin\theta_1)\cos\theta_2 + (\sin\theta_3 - 2\sin\theta_2 + 2\sin\theta_1)\cos\theta_3 = \frac{m}{\lambda} \\ &\sin\theta_3 - \sin\theta_2 + \sin\theta_1 = \frac{1}{\lambda} \end{aligned} \tag{2.33}$$

This motivates the following short-hand notations:

$$\begin{aligned} p_k &= 2(\sin\theta_k - \sin\theta_{k-1} + \sin\theta_{k-2} - \cdots) \\ q_k &= 2(\sin\theta_k - 2\sin\theta_{k-1} + 2\sin\theta_{k-2} - \cdots) = 2(p_k - \sin\theta_k) \\ \theta_j &= 0 \quad (j \le 0) \end{aligned} \tag{2.34}$$

Using these notations, we have

$$\begin{aligned} p_k &= \frac{\cos\theta_k - \cos\theta_{k+1}}{\theta_{k+1} - \theta_k} \qquad (k = 1, 2) \\ p_s &= \frac{q_1\cos\theta_1 + q_2\cos\theta_2 + q_3\cos\theta_3}{m} \\ E_k &= \frac{q_k}{p_s} \qquad (k = 1, 2, 3) \end{aligned} \tag{2.35}$$

The algorithm for arbitrary s as shown in (2.27) is generalized from (2.35).

2.2.4 Discussions

The case of a seven-level cascade multilevel inverter is studied here. The number of H-bridges, s, is three. For given modulation indexes from 0.7 to 0.9, we utilized the proposed algorithm to determine E_1, E_2, and E_3 (as show in Figure 2.20) and the corresponding switching angles (as shown in Figure 2.21). The assumption is that the summation of DC voltages is always 1. Note the calculations here have been done off-line, not real-time calculation.

As shown in Figure 2.20, the optimal DC voltages are not equal for all modulation indexes. This implies that *the previous design guideline in which the step voltages are identical are not appropriate from the point of view of voltage quality*. In practical design, the identical voltage steps may be preferred from the point of view of modular design. Therefore, there is a tradeoff between the optimal voltage quality and modular design.

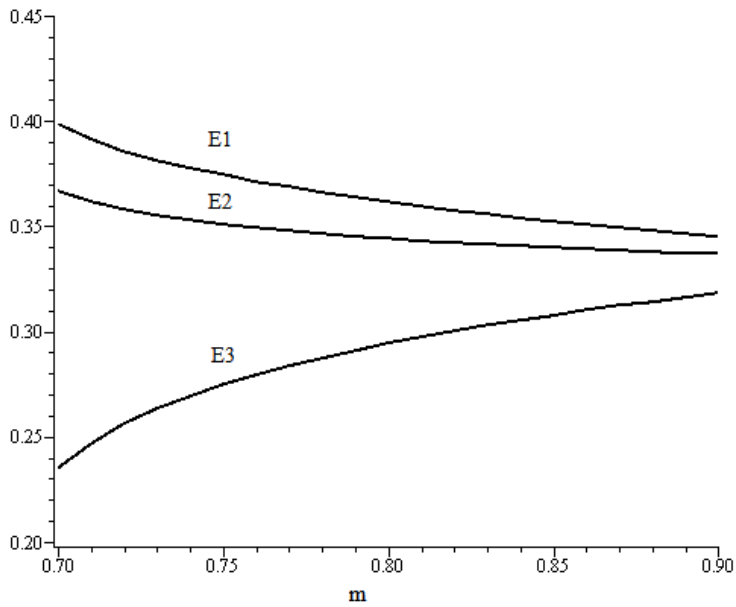


Figure 2.20. E_1, E_2, and E_3 (Assumption $E_1+E_2+E_3 = 1$)

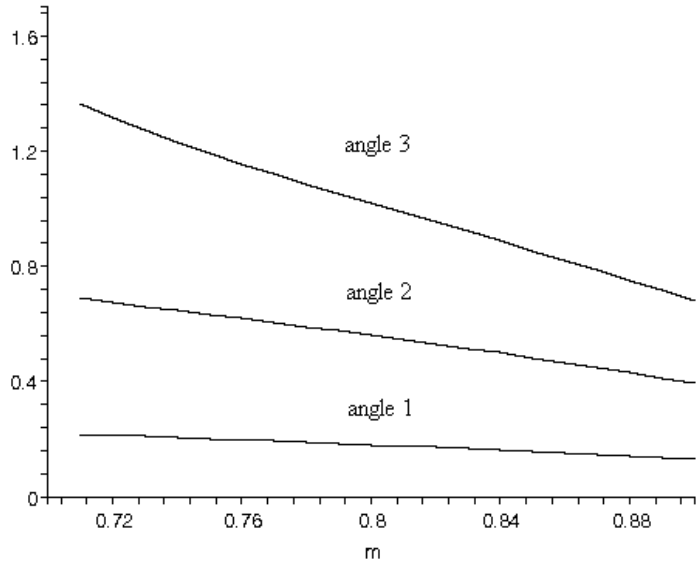


Figure 2.21. Switching angles

The corresponding minimum THD of the output voltage of the inverter is shown in Figure 2.22. The minimum THD gained in the inverter with equal step voltages is calculated by the algorithm proposed in [105]. This is also shown in Figure 2.22. The THD with the optimal step voltages proposed here is less than the minimum THD with equal step voltages, especially for smaller modulation indexes.

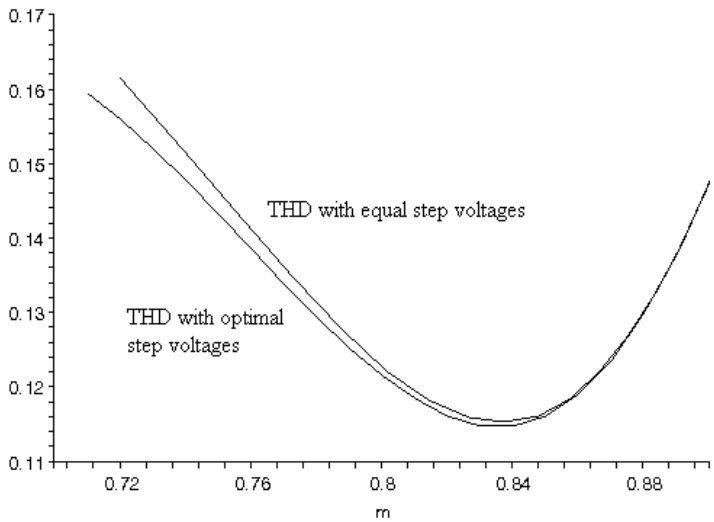


Figure 2.22. Comparison of THD between the inverters with equal step voltages and optimal step voltages

When we implement the algorithm, the modulation index is determined by utilizing a feed-back control loop. The ratios of DC voltages keep changing with respect to the change of the modulation index. Note that the summation of all DC voltages is fixed in this scenario.

One limitation here is that the algorithm fixes DC voltage ratios and H-bridge output voltage shapes for a certain modulation index. Thus, the power flow ratios for H-bridges are fixed for the modulation index if phase shifts between H-bridge output voltages and the current are the same. If we want to change these power flow ratios, the only freedom we could use is the change of the phase shifts. However, different phase shifts will inevitably cause the voltage quality of the multilevel inverter to deteriorate. Therefore, to push the voltage quality to the optimized peak, we have a trade-off between the voltage quality and the control of the power flow distribution among H-bridges.

2.3 Optimal values of DC voltages, switching angles and modulation index

In the last section, the amplitude of the multilevel inverter output voltage is regulated by the modulation index. In applications where the amplitude is fixed, we can just fix the modulation index to simplify the control. At the same time, we could determine an optimized modulation index to minimize THD. If the multilevel inverter output voltage amplitude changes slowly, we could still make the modulation index constant. But we can change the summation of DC voltages.

In this section, I have proposed an algorithm that determines a modulation index, a set of switching angles and appropriate DC voltages ratios to minimize THD for a

certain level inverter. Consequently, there is only one optimized design for a multilevel inverter with the certain levels.

2.3.1 Problem

Devise an algorithm for

Input: s

Output: $E_1, \ldots E_s, \theta_1, \ldots$ and θ_s, m, such that THD is minimum.

2.3.2 Algorithm

Our proposed algorithm for the problem:

Input: s

Output: $E_1, \ldots E_s, \theta_1, \ldots$ and θ_s, m, such that THD is minimum.

Get $E_1, \ldots E_s, \theta_1, \ldots, \theta_s$ and m by solving the following equation

$$\begin{aligned} & p_k = \frac{\cos\theta_k - \cos\theta_{k+1}}{\theta_{k+1} - \theta_k} \qquad (k = 1 \ldots s-1) \\ & p_1^2(\theta_2 - \theta_1) + \cdots + p_s^2(\theta_{s+1} - \theta_s) = q_1 \cos\theta_1 + \cdots + q_s \cos\theta_s \\ & E_k = \frac{q_k}{p_s} \qquad (k = 1 \ldots s) \end{aligned} \tag{2.36}$$

Where

$$\begin{aligned} & q_k = 2(p_k - \sin\theta_k) \\ & p_k = 2(\sin\theta_k - \sin\theta_{k-1} + \sin\theta_{k-2} - \cdots) \\ & \theta_j = 0 \quad (j \le 0) \end{aligned} \tag{2.37}$$

There are (4*s*) equations, and there are (4*s*) variables.

2.3.3 Proof

In order to simplify the presentation of the proof, we consider the case when $s = 3$. The generalization to arbitrary s is obvious. We will minimize $f = (4m^2/\pi)(d^2+1)$ under the constraints that $g = h = 0$ where

$$\begin{aligned} f &= E_1^2(\theta_2-\theta_1)+(E_1+E_2)^2(\theta_3-\theta_2)+(E_1+E_2+E_3)^2(\pi/2-\theta_3) \\ g &= E_1\cos\theta_1+E_2\cos\theta_2+E_3\cos\theta_3-m \\ h &= E_1+E_2+E_3-1 \end{aligned} \tag{2.38}$$

where $\theta_4 = \pi/2$. From Lagrange multiplier method, we obtain the following system of eight equations.

$$
\begin{aligned}
&\frac{\partial f}{\partial \theta_1} = \lambda \frac{\partial g}{\partial \theta_1} + \mu \frac{\partial h}{\partial \theta_1} \\
&\frac{\partial f}{\partial \theta_2} = \lambda \frac{\partial g}{\partial \theta_2} + \mu \frac{\partial h}{\partial \theta_2} \\
&\frac{\partial f}{\partial \theta_3} = \lambda \frac{\partial g}{\partial \theta_3} + \mu \frac{\partial h}{\partial \theta_3} \\
&\frac{\partial f}{\partial E_1} = \lambda \frac{\partial g}{\partial E_1} + \mu \frac{\partial h}{\partial E_1} \\
&\frac{\partial f}{\partial E_2} = \lambda \frac{\partial g}{\partial E_2} + \mu \frac{\partial h}{\partial E_2} \\
&\frac{\partial f}{\partial E_3} = \lambda \frac{\partial g}{\partial E_3} + \mu \frac{\partial h}{\partial E_3} \\
&\frac{\partial f}{\partial m} = \lambda \frac{\partial g}{\partial m} + \mu \frac{\partial h}{\partial m} \\
&g = 0 \\
&h = 0
\end{aligned}
\tag{2.39}
$$

There are nine unknown θ_1, θ_2, θ_3, E_1, E_2, E_3, λ, μ and m. By inserting f, g and h into the equations above, we obtain the following system of eight equations.

$$
\begin{aligned}
&-E_1^2 = -m^2 \lambda E_1 \sin\theta_1 \\
&E_1^2 - (E_1 + E_2)^2 = -m^2 \lambda E_2 \sin\theta_2 \\
&(E_1 + E_2)^2 - (E_1 + E_2 + E_3)^2 = -m^2 \lambda E_3 \sin\theta_3 \\
&2E_1(\theta_2 - \theta_1) + 2(E_1 + E_2)(\theta_3 - \theta_2) + 2(E_1 + E_2 + E_3)(\theta_4 - \theta_3) = m^2(\lambda \cos\theta_1 + \mu) \\
&2(E_1 + E_2)(\theta_3 - \theta_2) + 2(E_1 + E_2 + E_3)(\theta_4 - \theta_3) = m^2(\lambda \cos\theta_2 + \mu) \\
&2(E_1 + E_2 + E_3)(\theta_4 - \theta_3) = m^2(\lambda \cos\theta_3 + \mu) \\
&2{E_1}^2(\theta_2 - \theta_1) + 2(E_1 + E_2)^2(\theta_3 - \theta_2) + 2(E_1 + E_2 + E_3)^2(\theta_4 - \theta_3) = m^3 \lambda \\
&E_1 \cos\theta_1 + E_2 \cos\theta_2 + E_3 \cos\theta_3 = m \\
&E_1 + E_2 + E_3 = 1
\end{aligned}
\tag{2.40}
$$

By factoring and simplifying the left hand side of the first three equations and by carrying out successive "row" operations on the next three equations, we obtain the following system of eight equations in eight unknowns.

$$\begin{aligned}
&E_1^2 = m^2\lambda E_1 \sin\theta_1 \\
&2E_1 + E_2 = m^2\lambda E_2 \sin\theta_2 \\
&2E_1 + 2E_2 + E_3 = m^2\lambda E_3 \sin\theta_3 \\
&2E_1(\theta_2 - \theta_1) = m^2\lambda(\cos\theta_1 - \cos\theta_2) \\
&2(E_1 + E_2)(\theta_2 - \theta_1) = m^2\lambda(\cos\theta_2 - \cos\theta_3) \\
&E_1{}^2(\theta_2 - \theta_1) + (E_1 + E_2)^2(\theta_3 - \theta_2) + (E_1 + E_2 + E_3)^2(\theta_4 - \theta_3) = m^3\lambda / 2 \\
&E_1 \cos\theta_1 + E_2 \cos\theta_2 + E_3 \cos\theta_3 = m \\
&E_1 + E_2 + E_3 = 1
\end{aligned} \tag{2.41}$$

Note that we have eliminated μ. From the first three equations, we obtain:

$$\begin{aligned}
&E_1 = \lambda \sin\theta_1 \\
&E_2 = \lambda(\sin\theta_2 - 2\sin\theta_1) \\
&E_3 = \lambda(\sin\theta_3 - 2\sin\theta_2 + 2\sin\theta_1)
\end{aligned} \tag{2.42}$$

By putting these into the remaining equations and simplifying, we obtain:

$$
\begin{aligned}
&2\sin\theta_1 = \frac{\cos\theta_1 - \cos\theta_2}{\theta_2 - \theta_1} \\
&2(\sin\theta_2 - \sin\theta_1) = \frac{\cos\theta_2 - \cos\theta_3}{\theta_3 - \theta_2} \\
&(\sin\theta_1)^2(\theta_2 - \theta_1) + (\sin\theta_2 - \sin\theta_1)^2(\theta_3 - \theta_2) + (\sin\theta_3 - \sin\theta_2 + \sin\theta_1)^2(\theta_4 - \theta_3) = \frac{1}{2m\lambda} \\
&(\sin\theta_1)\cos\theta_1 + (\sin\theta_2 - 2\sin\theta_1)\cos\theta_2 + (\sin\theta_3 - 2\sin\theta_2 + 2\sin\theta_1)\cos\theta_3 = \frac{1}{m\lambda} \\
&\sin\theta_3 - \sin\theta_2 + \sin\theta_1 = \frac{1}{m^2\lambda}
\end{aligned}
$$

(2.43)

This motivates the following short-hand notations:

$$
\begin{aligned}
&p_k = 2(\sin\theta_k - \sin\theta_{k-1} + \sin\theta_{k-2} - \cdots) \\
&q_k = 2(\sin\theta_k - 2\sin\theta_{k-1} + 2\sin\theta_{k-2} - \cdots) = 2(p_k - \sin\theta_k) \\
&\theta_j = 0 \quad (j \le 0)
\end{aligned}
\tag{2.44}
$$

Using these notations, we have

$$
\begin{aligned}
&p_k = \frac{\cos\theta_k - \cos\theta_{k+1}}{\theta_{k+1} - \theta_k} \qquad (k = 1, 2) \\
&(\frac{p_1}{2})^2(\theta_2 - \theta_1) + (\frac{p_2}{2})^2(\theta_3 - \theta_2) + (\frac{p_3}{2})^2(\theta_4 - \theta_3) = \frac{1}{2m\lambda} \\
&\frac{q_1}{2}\cos\theta_1 + \frac{q_2}{2}\cos\theta_2 + \frac{q_3}{2}\cos\theta_3 = \frac{1}{m\lambda} \\
&\frac{p_3}{2} = \frac{1}{m^2\lambda} \\
&E_k = m^2\lambda\frac{q_k}{2} \qquad (k = 1, 2, 3)
\end{aligned}
\tag{2.45}
$$

By eliminating λ and m, we have

$$p_k = \frac{\cos\theta_k - \cos\theta_{k+1}}{\theta_{k+1} - \theta_k} \qquad (k = 1, 2)$$

$$p_1^2(\theta_2 - \theta_1) + p_2^2(\theta_3 - \theta_2) + p_3^2(\theta_4 - \theta_3) = q_1 \cos\theta_1 + q_2 \cos\theta_2 + q_3 \cos\theta_3 \qquad (2.46)$$

$$E_k = \frac{q_k}{p_s} \qquad (k = 1, 2, 3)$$

It is can be obviously generalized to arbitrary s, as shown in (2.36).

2.3.4 Discussions

For a different value of *s*, the optimal values of modulation index, DC voltages and switching angles are shown in Table 2.2. (Assumption: the summation of DC voltages is 1.) This is instructive information for engineers in selecting appropriate DC voltages and modulation index to achieve better voltage quality.

Table 2.2. Optimal values of modulation index, DC voltages and switching angles for different voltage levels

s	***m***	**THD**	**Ratio/Angles**						
2	0.859	0.163	0.52/0.23	0.48/0.74					
3	0.835	0.114	0.35/0.16	0.34/0.51	0.31/0.91				
4	0.822	0.088	0.27/0.13	0.26/0.39	0.25/0.67	0.22/1.00			
5	0.815	0.072	0.22/0.10	0.21/0.31	0.21/0.54	0.19/0.78	0.17/1.07		
6	0.810	0.061	0.18/0.09	0.18/0.26	0.18/0.44	0.17/0.64	0.15/0.86	0.14/1.12	
7	0.806	0.052	0.16/0.08	0.15/0.23	0.15/0.39	0.15/0.55	0.14/0.72	0.13/0.92	0.12/1.16

The limitation of this algorithm is similar to what I proposed in the last section. The power flow ratios are fixed. These ratios are pre-determined. Therefore, we can design H-bridges based on these ratios to meet the current rating and thermal performance.

2.4 Applications of Minimal THD modulation

The series of minimal THD modulation was initially proposed for a voltage source multilevel inverter. Voltage THD of the inverter is minimized. This is preferable in many applications, as mentioned in previous sections.

Actually, the series of minimal THD modulation is suitable for current source multilevel inverters [106, 107]. The current source multilevel inverters are generally applied in large motor drives, where the current THD is of main concern. The less current THD means less power losses caused by harmonics. The minimal THD modulations for current source multilevel inverters guarantee minimal current THD. This results in minimal power losses caused by harmonics.

Chapter 3. Optimal combination modulation

3.1 Motivation of the optimal modulation

The optimal combination modulation method is a customized optimal modulation. It was developed for the 10 MVA STATCOM project. The modulation strategy used in the 10 MVA STATCOM project must meet the flowing criteria.

1. The topology of multilevel inverter is the five-level cascade multilevel inverter.
2. The switching frequency has been designed to be 300 Hz, since the removal capability of the heat pipe is about 4 kW and then nominal output current is as high as 1.39 kA (RMS value).
3. The current harmonics distortion must meet IEEE 519 standards [108].
4. The STATCOM should maintain its functionality even if some cells are bypassed due to faults. This means that the number of voltage levels decreases in three phases. The proposed modulation must guarantee that the voltage quality will have small deterioration due to reduced voltage levels.

Several previous modulation strategies have been studied for the 10 MVA STATCOM. With the staircase modulation [11, 48], the inverter switches at a lower frequency, but the current harmonic distortions are higher than the limits stated in the standard. The multilevel SPWM [32, 75] can result in lower current harmonic

distortions, but the switching frequency should be higher than 300 Hz. Moreover, for general optimal modulations, the voltage quality will deteriorate substantially under the condition of reduced voltage levels. This is because the pre-calculated angles are optimized for nominal voltage levels.

3.2 Algorithm to calculate switching angles

The five-level cascade multilevel inverter is shown in Figure 3.1. v_{dc} is the voltage of a DC capacitor in an H-bridge. Here, we assume that all DC capacitor voltages are E. The amplitude of a voltage step is also E. Figure 3.2 shows the A phase voltage waveforms generated by the proposed optimal combination modulation. $v_{H,a1}$ and $v_{H,a2}$ are output voltages of two H-bridges in the A phase.

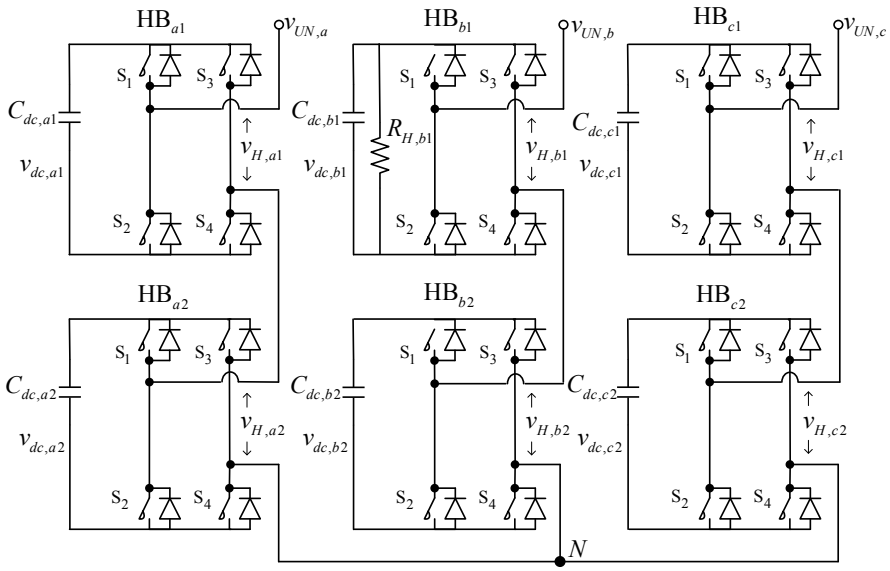


Figure 3.1. Five-level cascade multilevel inverter

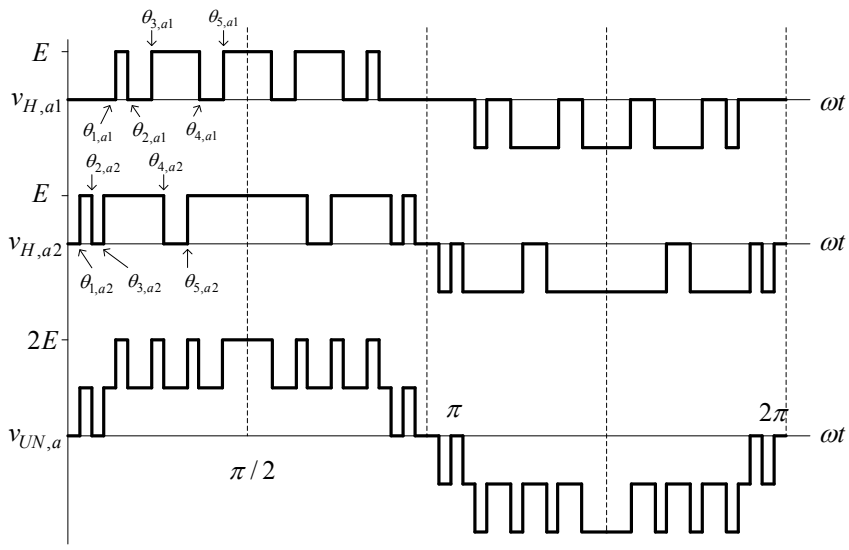


Figure 3.2. Optimal combination modulation for five-level inverter

As shown in Figure 3.2, the output voltage of an H-bridge has five switching angles in the period from 0 to $\pi/2$. So the phase voltage of the inverter can achieve ten switching angles in the period from 0 to $\pi/2$. Based on Fourier series transformation, the harmonics of $v_{H,a1}$ can be expressed as:

$$V_{H,a1(n)} = \frac{4E}{n\pi}[\cos(n\theta_{1,a1}) - \cos(n\theta_{2,a1}) + \cos(n\theta_{3,a1}) - \cos(n\theta_{4,a1}) + \cos(n\theta_{5,a1})] \quad (3.1)$$

Ideally, given a desired amplitude of the fundamental component of $v_{H,a1}$, $V_{H,a1(1)}$, one wants to determine the switching angles to make specific harmonics be zero. For a three-phase application, the triple-order harmonics in each phase does not need be canceled as they automatically cancel in the line-to-line voltages. Here, the 5th, 7th,

11th and 13th order harmonics are chosen to be eliminated. The switching angles of the first H-bridge in the A phase must satisfy the following equations:

$$\begin{aligned}
&V_{H,a1(1)} = \frac{4E}{\pi}[\cos(\theta_{1,a1}) - \cos(\theta_{2,a1}) + \cos(\theta_{3,a1}) - \cos(\theta_{4,a1}) + \cos(\theta_{5,a1})] \\
&0 = \cos(5\theta_{1,a1}) - \cos(5\theta_{2,a1}) + \cos(5\theta_{3,a1}) - \cos(5\theta_{4,a1}) + \cos(5\theta_{5,a1}) \\
&0 = \cos(7\theta_{1,a1}) - \cos(7\theta_{2,a1}) + \cos(7\theta_{3,a1}) - \cos(7\theta_{4,a1}) + \cos(7\theta_{5,a1}) \\
&0 = \cos(11\theta_{1,a1}) - \cos(11\theta_{2,a1}) + \cos(11\theta_{3,a1}) - \cos(11\theta_{4,a1}) + \cos(11\theta_{5,a1}) \\
&0 = \cos(13\theta_{1,a1}) - \cos(13\theta_{2,a1}) + \cos(13\theta_{3,a1}) - \cos(13\theta_{4,a1}) + \cos(13\theta_{5,a1})
\end{aligned} \tag{3.2}$$

We can define the modulation index of the A phase first H-bridge as:

$$m_{a1} = \frac{\pi}{4}\frac{V_{H,a1(1)}}{E} \tag{3.3}$$

The resultant method is used here to find the solutions[82]. The solutions exist in a range of the modulation indices from 0 to 0.9. Some modulation indices have no solutions, but some have up to three solutions.

In the A phase, the five-level cascade multilevel inverter can be viewed as two H-bridges connected in series, and these H-bridges can be controlled independently. This control method inherently eliminate lower order harmonics (5th, 7th, 11th and 13th) since each H-bridge does not generate them. The modulation index for the A phase is defined as:

$$m_a = \frac{\pi}{4}\frac{V_{a(1)}}{2E} \tag{3.4}$$

where $V_{a(1)}$ is the amplitude of fundamental component of A phase voltage. If output voltages of three phases of the inverter are symmetric, m_a, m_b and m_c will be the same.

The modulation index for the A phase is expressed.

$$m_a = \frac{1}{2}\sum_{i=1}^{2} c_{ai} m_{ai} \tag{3.5}$$

c_{ai} is polar index and can be 1, 0 or -1. This represents the output voltage of the ith H-bridge is positive, zero or negative with respect to the output voltage of the phase leg voltage.

The available values of m_{a1} and m_{a2} are from 0 to 0.9 and the resolutions are set as 0.01. The algorithm for calculating the switching angles for the A-phase is as follows.

Step 1. We can get $90^2 \times 3^2 = 72900$ combinations of [m_{a1}, m_{a2}, c_{a1}, c_{a2}] with respect to an m_a, and then pick up the combinations that satisfy (3.5).

Step 2. For each m_{ai}, there are up to three sets of solutions of switching angles. For each resulting combination gotten from step 1, we can get up to $3^2 = 9$ combinations of [$\theta_{1,a1}$, $\theta_{2,a1}$, $\theta_{3,a1}$, $\theta_{4,a1}$, $\theta_{5,a1}$, c_{a1}, $\theta_{1,a2}$, $\theta_{2,a2}$, $\theta_{3,a2}$, $\theta_{4,a2}$, $\theta_{5,a2}$, c_{a2}].

Step 3. For a combination, [$\theta_{1,a1}$, $\theta_{2,a1}$, $\theta_{3,a1}$, $\theta_{4,a1}$, $\theta_{5,a1}$, c_{a1}, $\theta_{1,a2}$, $\theta_{2,a2}$, $\theta_{3,a2}$, $\theta_{4,a2}$, $\theta_{5,a2}$, c_{a2}], the nth harmonic of A phase leg voltages can be expressed as

$$V_{a,(n)} = \sum_{i=1}^{2} \frac{4Ec_{ai}}{n\pi}[\cos(n\theta_{1,ai}) - \cos(n\theta_{2,ai}) + \cos(n\theta_{3,ai}) - \cos(n\theta_{4,ai}) + \cos(n\theta_{5,ai})] \tag{3.6}$$

If it is a three-phase balancing system, the THD for the line-to-line voltage is defined as:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_{a(n)}^2}}{V_{a(1)}} \qquad (n = 5, 7, 11, 13, 17, ...) \tag{3.7}$$

The current harmonics injected to the system are also calculated based on parameters of the STATCOM and the power system. The total demand distortion (TDD) is defined as

$$\text{TDD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_{a(n)}^2}}{I_{\text{nominal}}} \qquad (n = 5, 7, 11, 13, 17, ...) \tag{3.8}$$

where $I_{a(n)}$ is the current harmonic injected into the bus and I_{nominal} is the nominal current flowing through the bus. IEEE 519 standard specifies the limits of current harmonics and TDD. Only the combinations that meet all requirements stated in the IEEE 519 standard are chosen.

Step 4. For each combination, [$\theta_{1,a1}$, $\theta_{2,a1}$, $\theta_{3,a1}$, $\theta_{4,a1}$, $\theta_{5,a1}$, c_{a1}, $\theta_{1,a2}$, $\theta_{2,a2}$, $\theta_{3,a2}$, $\theta_{4,a2}$, $\theta_{5,a2}$, c_{a2}], chosen from step 3, we can derive two different combinations, [A_1, A_2] and [A_2, A_1], where A_i is ($\theta_{1,ai}$, $\theta_{2,ai}$, $\theta_{3,ai}$, $\theta_{4,ai}$, $\theta_{5,ai}$, c_{ai}).

Step 5. For each modulation index, we find out all combinations that satisfy all conditions described from step 1 to step 4. From these combinations, we choose a combination whose switching angles are the closet to the switching angles with respect to the adjacent modulation index. The result of this method can produce the variations of switching angles being much smoother.

3.3 Case study: five-level inverter based STATCOM

The case studied is a five-level cascade inverter based 10 MVAr STATCOM system connected to a transmission line of 64 MW. The inductance of the coupling inductor is 0.6886 mH. IEEE 519 standard states that the percentage of 5th, 7th, 11th and 13th harmonics of transmission line current caused by the STATCOM must be less than 2%, the percentage of the 17th and 19th harmonics of that must be less than 1.5%, the percentage of 23rd, 25th, 29th and 31st harmonics of that must be less than 0.6%, the percentage of 35th and higher harmonics of that must be less than 0.3%. Note that the base current is the nominal current flowing through the bus. IEEE 519 standard also states the limitation of TDD as 5%.

Based on the proposed optimal PWM modulation strategy and the IEEE 519 requirement, the switching angles, c_{a1} and c_{a2} are shown in Figure 3.3, Figure 3.5, Figure 3.4 and Figure 3.6, respectively.

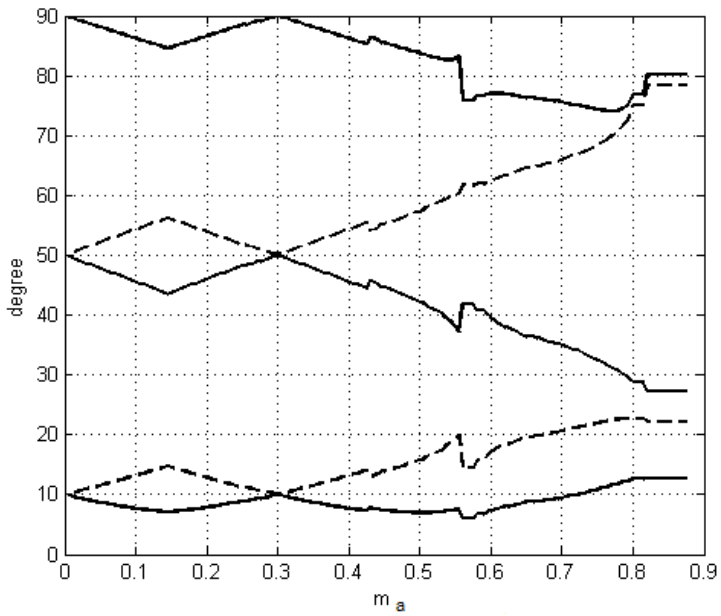


Figure 3.3. The first set of switching angles

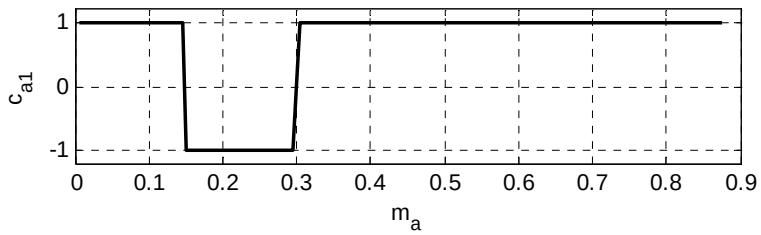


Figure 3.4. The value of c_{a1}

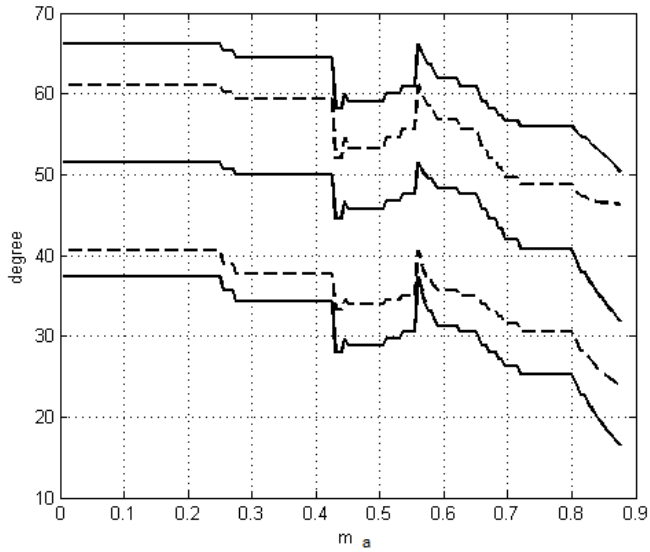


Figure 3.5. The second set of switching angles

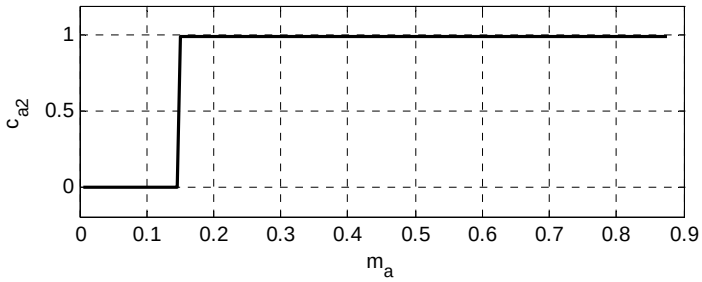


Figure 3.6. The value of c_{a2}

We assume it is a three-phase balancing system. The m_a, m_b and m_c are m. Current harmonic components that are injected into the transmission line are also calculated and are shown in Figure 3.7, Figure 3.8, Figure 3.9 and Figure 3.10. The percentages of 5th, 7th, 11th and 13th harmonics of transmission line current caused by the

STATCOM are less than 2%. The percentages of the 17th and 19th harmonics of transmission line current caused by the STATCOM are less than 1.5%. The percentages of 23rd, 25th, 29th and 31st harmonics of transmission line current caused by the STATCOM are less than 0.6%. The percentages of higher order harmonics of transmission line current caused by the STATCOM are less than 0.3%. TDD of transmission line current caused by the STATCOM is shown in Figure 3.11. It is less than 5%. Therefore, the percentages of current harmonics and the TDD meet IEEE 519 standard.

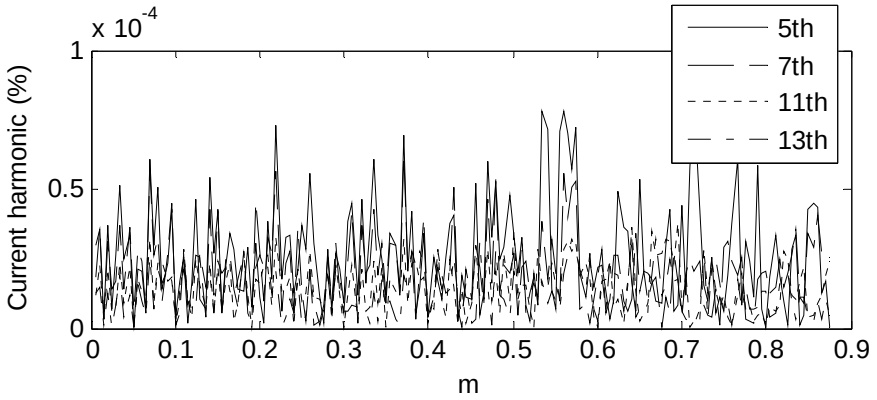


Figure 3.7. Percentage of 5th 7th, 11th and 13th harmonics

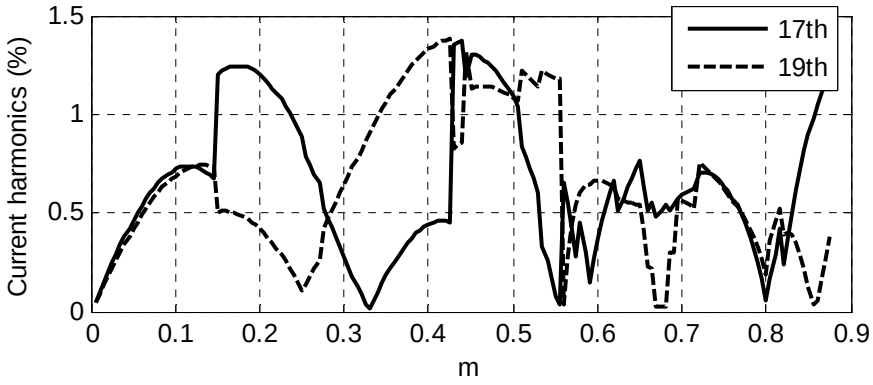


Figure 3.8. Percentage of 17th and 19th harmonics

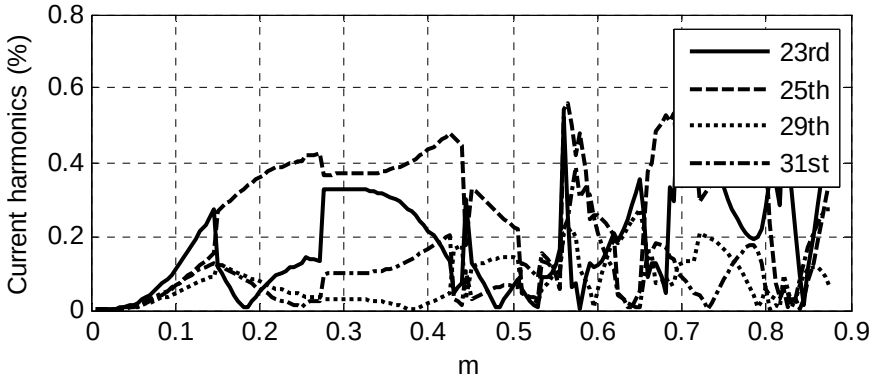


Figure 3.9. Percentage of 23rd, 25th, 29th and 31st harmonics

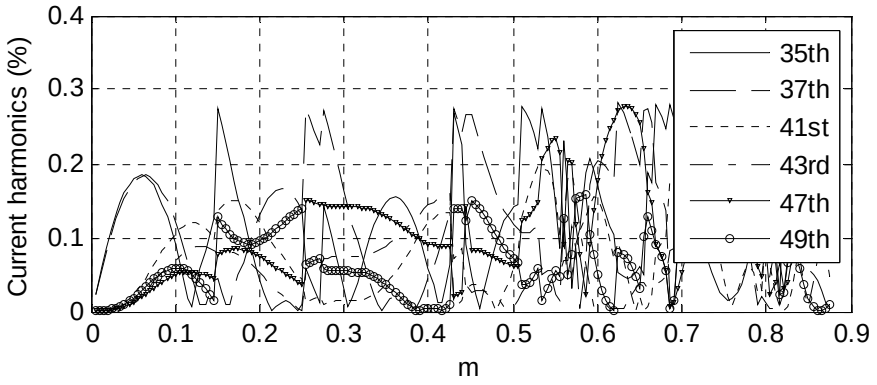


Figure 3.10. Percentage of 35th and higher order harmonics

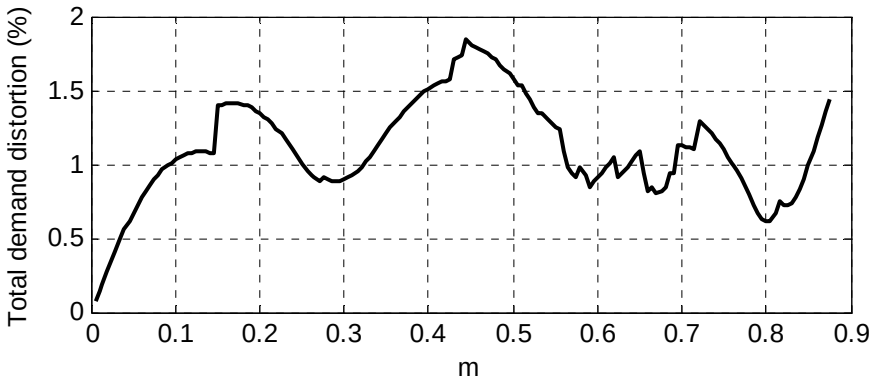


Figure 3.11. TDD of transmission current caused by the STATCOM

In a more practical simulation that includes control delay, the simulated current harmonics under full load condition are shown in Figure 3.12. The blue line is the limitation of current harmonics stated in IEEE 519 standard. The red line shows percentages of current harmonics injected into the bus when the STATCOM works in capacitive mode with full-rating. The yellow line shows them when the STATCOM works in the inductive mode with full-rating. These two cases are the worst cases. As

shown in Figure 3.12, each order current harmonic is less than the limitation stated in the standard.

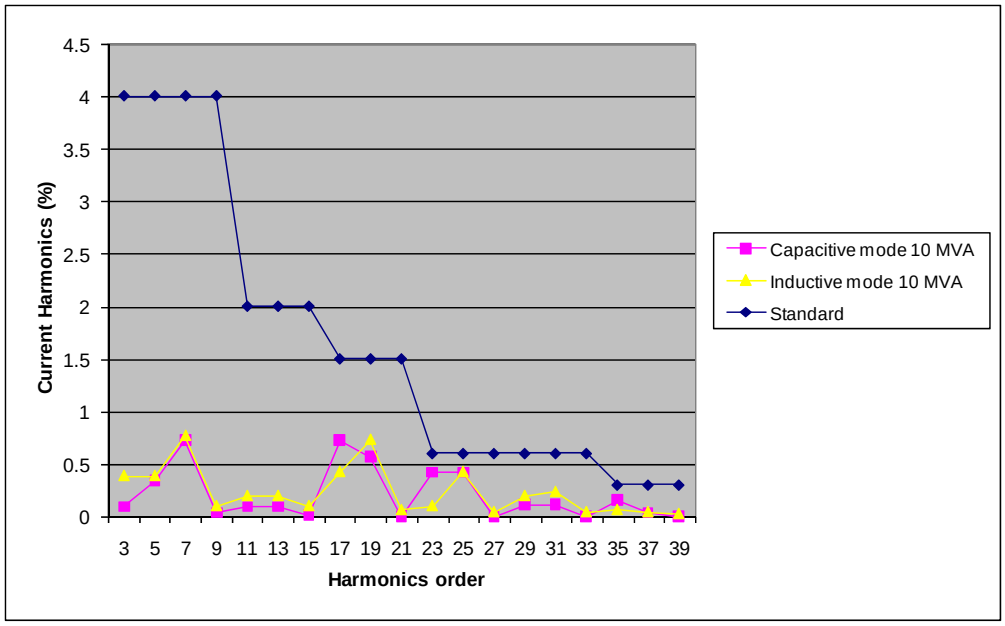


Figure 3.12. The difference between the simulated harmonics and IEEE 519 standard

3.4 Summary

A new optimal combination modulation strategy is proposed for the 10 MVAr STATCOM systems. There are two optimizations in this strategy. The first one is the optimization of switching angles for each H-bridge to eliminate the 5th, 7th, 11th, and 13th harmonics. Even when a cell is bypassed due to faults, lower order harmonics still don't exist. The second one is the optimization of combination of switching angles of two H-bridges for reducing the higher order harmonics to meet IEEE 519 standard for a

specified application. The calculation results and simulation results show, with the proposed optimal combination modulation, that the current harmonics and TDD can meet IEEE 519 standard when the five-level cascade multilevel inverter based 10 MVAr STATCOM is connected to a 64 MW system.

Chapter 4. Control of cascade multilevel inverter for STATCOM

4.1 Introduction

In this chapter, I am presenting a new control for balancing DC capacitor voltages. An adequate control strategy for avoiding the imbalance of DC capacitor voltages must meet the following four requirements.

1) It can balance voltages when the STATCOM works in the capacitive mode, the inductive mode and the standby mode;

2) Its impact on voltage quality is as small as possible;

3) It can balance voltages when components of H-bridges have parameter variations;

4) It can balance voltages when H-bridges switch with different switching patterns.

The methods presented in [110, 124] balance the voltages by swapping switching patterns. Due to no feedback control, they may not meet the third requirement. The feedback control strategies presented in [11, 48, 119, 123, 125] reshape the output voltages of H-bridges based on the feedback signals of the DC capacitor voltages. Thus, they meet the third and fourth requirement. However, the papers [11, 48, 119, 123, 125]

did not show if the control strategies work in different operating modes. Also, the impacts on voltage qualities were not analyzed.

The modeling of the multilevel converter benefits the design of control systems [115, 126]. This chapter proposes a new feedback control strategy for balancing individual DC capacitor voltages based on the detailed small-signal model. The small-signal model leads us to find out an efficient way for reshaping the voltage to achieve the control goal. The transfer function for an individual DC capacitor voltage derived from the small-signal model shows that the gain of the transfer function keeps changing. By introducing a compensator into the control loop to cancel the variation of gain, the controller works well in the whole operating region of: the capacitive mode, the inductive mode and the standby mode.

Note: that although the focus of this chapter is the DC capacitor voltage balancing control, this chapter also covers the conventional current loop control and average DC voltage loop control.

4.2 Problem

Find a better method for controlling individual DC capacitor voltages in cascade multilevel inverter based STATCOM.

Constraint: The methods should balance capacitor voltages when the STATCOM works in capacitive mode, inductive mode and standby mode.

Optimization goal: Less impact on original H-bridge voltage. The original H-bridge voltages are regulated slightly for controlling the DC capacitor voltages. A better method will cause less change on the original H-bridge voltage.

4.3 Proposed control method

Figure 4.1 shows the three-phase five-level cascade multilevel inverter based STATCOM. Two H-bridges are connected in series in a phase. The inverter is connected to the power system through interface inductors (L_S, R_S). The resistor connected in parallel with the DC capacitor implies the power losses of the H-bridge.

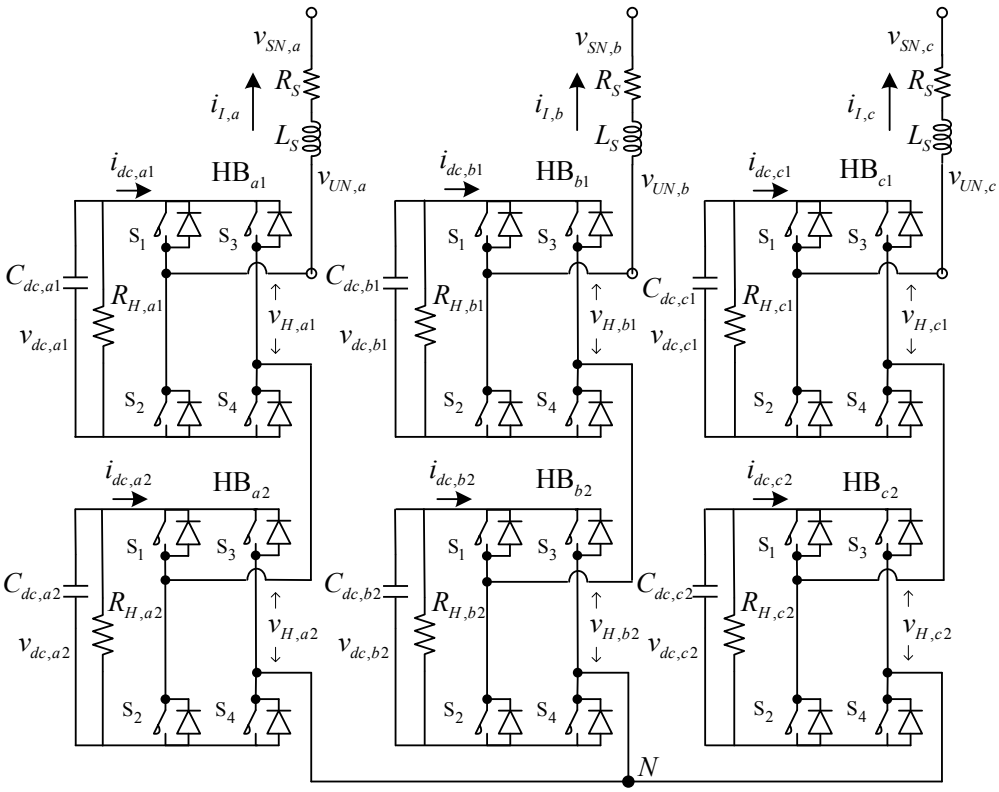


Figure 4.1. Five-level cascade multilevel inverter based STATCOM

The optimal combination modulation presented in Chapter 3 is used for the five-level inverter based STATCOM. The output voltage of the first H-bridge, $v_{H,a1}$, is determined by switching angles, $\theta_{1,a1}$, $\theta_{2,a1}$, $\theta_{3,a1}$, $\theta_{4,a1}$ and $\theta_{5,a1}$. That of the second H-bridge is determined by $\theta_{1,a2}$, $\theta_{2,a2}$, $\theta_{3,a2}$, $\theta_{4,a2}$ and $\theta_{5,a2}$. The DC link voltages in H-bridges are assumed as E. Switching angles are determined by the modulation index of the inverter, m. In a three-phase balancing system, the amplitudes of fundamental components $v_{UN,a}$, $v_{UN,b}$ and $v_{UN,c}$ are the same and expressed as V_{UN}. The m is defined as:

$$m = \frac{\pi}{4} \cdot \frac{V_{UN}}{2E} \tag{4.1}$$

The relationships between the m and switching angles are shown in Figure 3.3 and Figure 3.5, respectively.

Figure 4.2 shows the control loop for an individual DC capacitor voltage in the A-phase. A DC capacitor voltage, $v_{dc,ak}$, is compared with reference voltage, E. H_{ind} is a PI controller. G_D represents the digital delay. $G_{f,RC}$ represents the filter. The model of the circuit, $G_{vdc\theta,ak}$, will be explained later. $H_{\lambda,ak}$, the key part of the controller, is the calculation resulting from many variables in the system. The ωt is the output of the phase lock loop. The $i_{I,d}$, $i_{I,q}$ and $i_{I,0}$ are the currents in dq0 coordinate. The d_q and d_d are the duty cycles in dq0 coordinate. The $\theta_{1,a\mathrm{k}}$, $\theta_{2,a\mathrm{k}}$, $\theta_{3,a\mathrm{k}}$, $\theta_{4,a\mathrm{k}}$ and $\theta_{5,a\mathrm{k}}$ represent original switching angles. Thus, the $H_{\lambda,ak}$ is determined by multiple system states and time. Figure 4.3 and Figure 4.4 show those in the B-phase and C-phase, respectively.

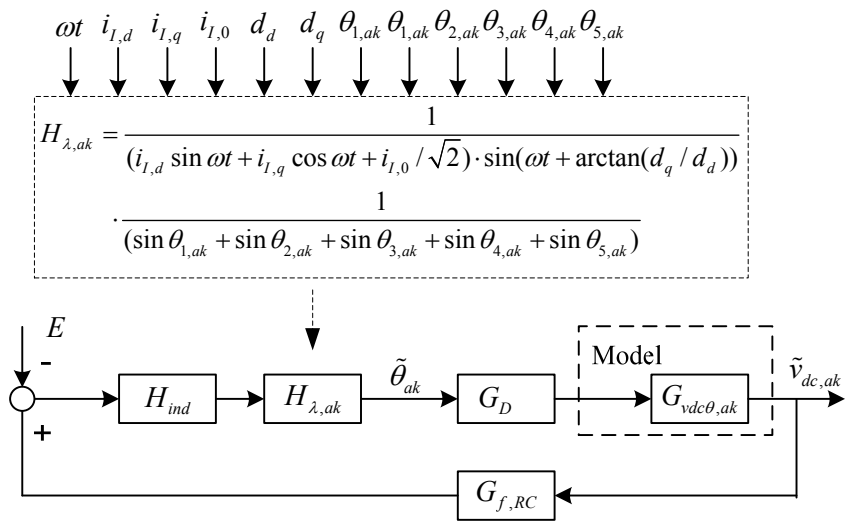


Figure 4.2. Control loop for DC capacitor voltages in the A-phase

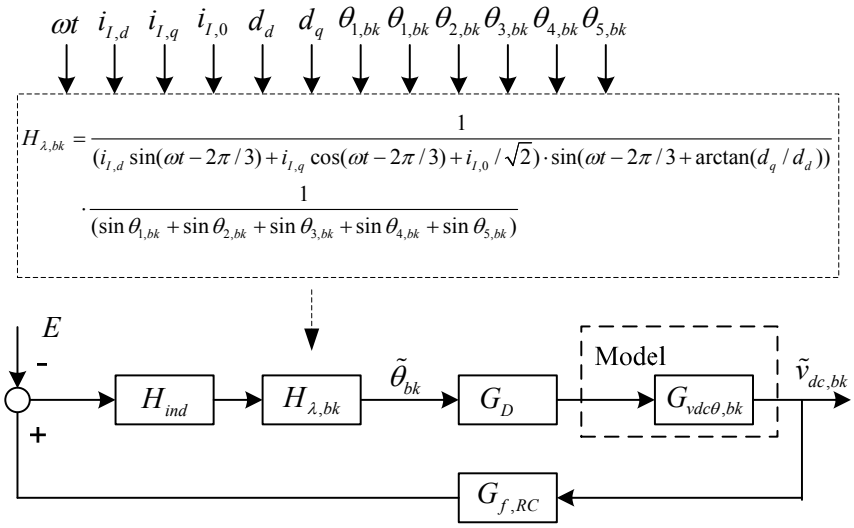


Figure 4.3. Control loop for DC capacitor voltages in the B-phase

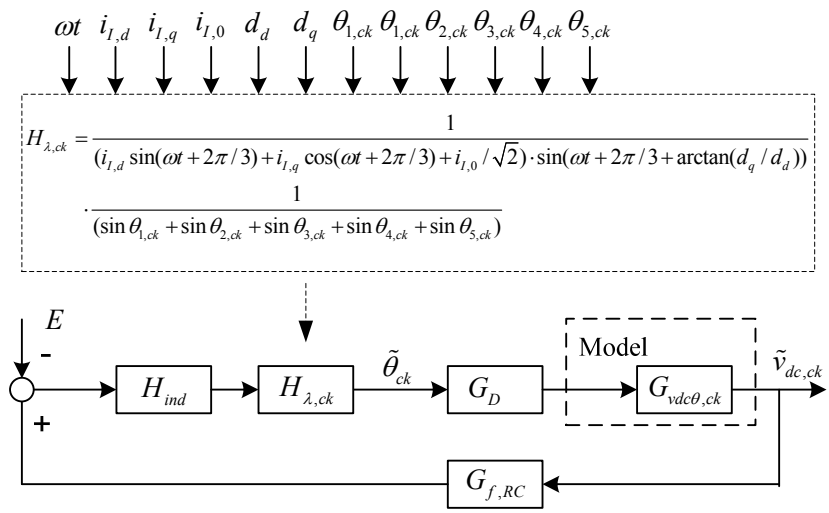


Figure 4.4. Control loop for DC capacitor voltages in the C-phase

The $\tilde{\theta}_{ak}$ is used to regulate the output voltage of inverter slightly as shown in Figure 4.5. Initially, the switching angles are determined by the modulation index. Here, the switching angles are changed slightly based on $\tilde{\theta}_{ak}$. Then, DC capacitor voltages can be controlled. The solid line is the original voltage and the dashed line is the changed voltage. In the figure, the amplitude of the fundamental component of changed voltage is larger than that that of the original voltage.

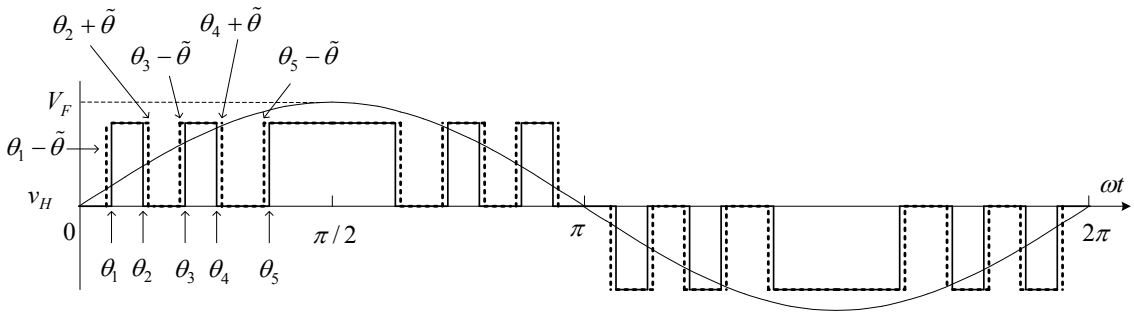


Figure 4.5. H-bridge output voltages before and after shifting a small angle

4.4 Proof

The analyses of the proposed method and other existing methods [11, 48, 110, 119, 123-125] show that the proposed method is a better method, under the constraint that this method should balance DC capacitor voltages in all operating modes.

Method A: the proposed method.

Method B: the method presented in [110, 124].

Method C: the method presented in [123, 125].

Method D: the method presented in [11, 48].

Method E: the method presented in [119].

4.4.1 Constraint

The constraint is that this method should balance DC capacitor voltages when the STATCOM works in all operating modes: the capacitive mode, the inductive mode and the standby mode.

Method B tries to balance the DC capacitor voltages by swapping switching patterns. Due to no feedback control, the method B cannot balance voltages when the H-bridges have parameter variations. This is illustrated by simulation results in Figure 4.10.

Methods D and the method E may balance DC capacitor voltages in one operation mode, but they cannot balance voltages in all operating modes. Only methods A and C can balance voltages in all operating modes. The following analysis provides proof.

A DC capacitor voltage is determined by the active power flowing into the H-bridge. The active power is determined by the fundamental components of the H-bridge output voltage and the current flowing into the H-bridge, if the effect of harmonics is ignored. Methods A, C, D and E regulate the DC capacitor voltages by slightly reshaping the fundamental components of the H-bridge output voltages.

Take the example of the first H-bridge in A-phase. Suppose the STATCOM runs in the capacitive mode. In the sub-figure I of Figure 4.6, $v_{SN,a}$ is the A-phase grid voltage, which is in phase with ωt.

$$v_{SN,a} = V_{SN,a} \sin(\omega t) \tag{4.2}$$

The fundamental component of the H-bridge output voltage, $v_{F,a1}$, is expressed as

$$v_{F,a1} = V_{F,a1}\sin(\omega t - \varphi) \qquad \varphi = -\arctan(d_q / d_d) \tag{4.3}$$

The phase difference between $v_{F,a1}$ and A-phase current, $i_{I,a}$, is ($\pi/2+\gamma$), where γ is a small positive angle.

$$i_{I,a} = I_{I,a}\sin(\omega t - \varphi - \frac{\pi}{2} - \gamma) \tag{4.4}$$

Thus, the output power of the H-bridge is expressed as

$$P = -\frac{1}{2}V_{F,a1}I_{I,a}\sin\gamma \tag{4.5}$$

Here the output power is negative. This means that the H-bridge absorbs the active power for compensating the power losses inside the H-bridge.

The absorbed active power is regulated to balance the DC capacitor voltage by reshaping the $v_{F,a1}$ slightly. The sub-figures II, III, IV and V of Figure 4.6 show the reshaped voltages by method A, C, D and E, respectively, which are denoted as $v'_{F,a1}$ and shown as bold lines in Figure 4.6. For comparison, we assume that all control strategies try to inject more power into H-bridges to increase DC capacitor voltages.

The $v'_{F,a1}$ in the sub-figure II is generated by the method A here. The amplitude of $v_{F,a1}$, $V_{F,a1}$, increases $\Delta V_{F,a1}$ when ($v_{F,a1}\times i_{I,a}$) is negative. The $V_{F,a1}$ decreases $\Delta V_{F,a1}$ when ($v_{F,a1}\times i_{I,a}$) is positive. The additional active power generated by reshaping $v_{F,a1}$ is expressed as

$$\Delta P \approx -\Delta V_{F,a1} \cdot I_{I,a} \cdot \frac{\cos\gamma}{\pi} \tag{4.6}$$

The $v'_{F,a1}$ in the sub-figure III is generated by the method C, which always increases $V_{F,a1}$. The additional active power is

$$\Delta P \approx -\Delta V_{F,a1} \cdot I_{I,a} \cdot \frac{\sin\gamma}{2} \tag{4.7}$$

The $v'_{F,a1}$ in the sub-figure IV is generated by the method D, which shifts $v_{F,a1}$ with $\Delta\gamma$. The additional active power is

$$\Delta P \approx -V_{F,a1} \cdot I_{I,a} \cdot \frac{\Delta\gamma}{2} \tag{4.8}$$

The $v'_{F,a1}$ in the sub-figure V is generated by the method E. $V_{F,a1}$ increases $\Delta V_{F,a1}$ when ωt is in [0, π/2] or [3π/2, 2π]. $V_{F,a1}$ decreases $\Delta V_{F,a1}$ when ωt is in [π/2, 3π/2]. The additional active power generated by this method is

$$\Delta P \approx -\Delta V_{F,a1} \cdot I_{I,a} \cdot \frac{\cos(2\varphi+\gamma)}{\pi} \tag{4.9}$$

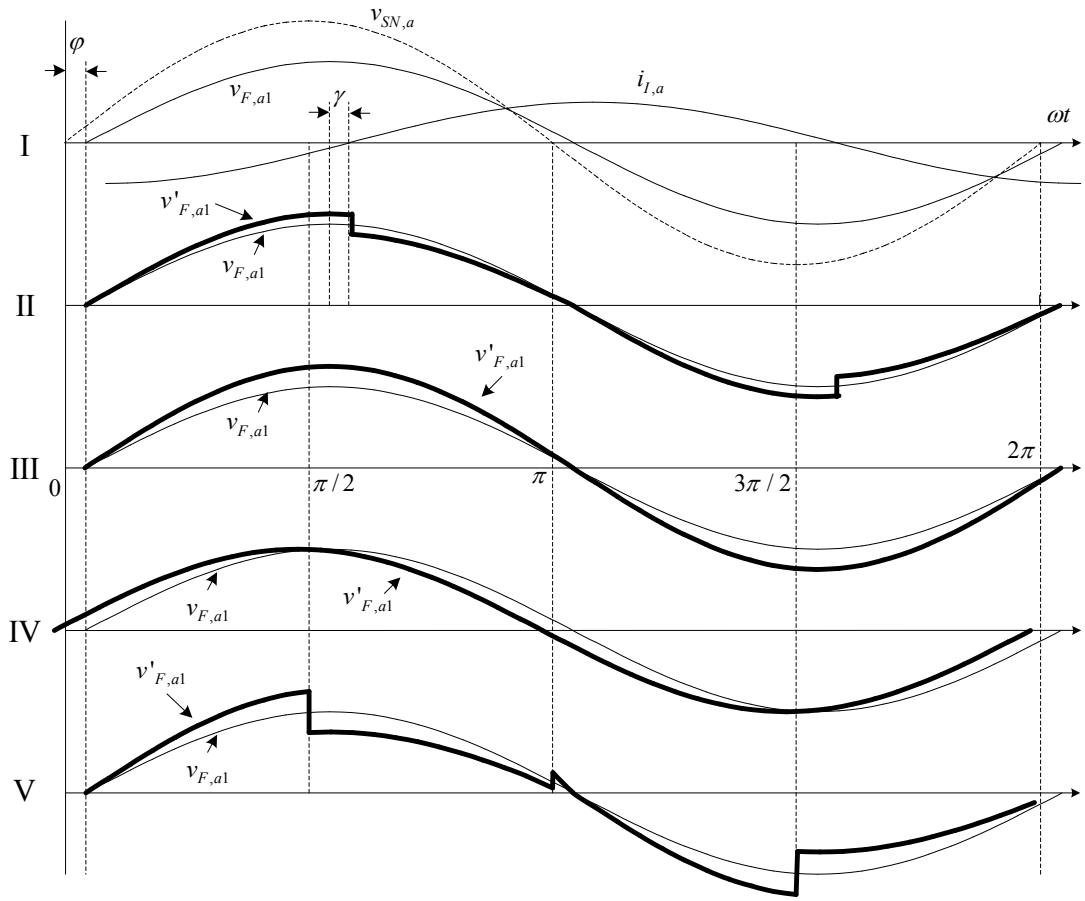


Figure 4.6. Waveforms in the capacitive mode

An adequate control strategy must regulate individual DC capacitor voltages when the STATCOM works in different operating modes (the capacitive mode, the inductive mode and the standby mode). However, the differences of control strategies for different operating modes have not been mentioned for the methods C, D and E.

Suppose the STATCOM moves to the inductive mode. For comparison, we still assume that all control strategies try to inject more active power into H-bridges to

increase DC capacitor voltages. Figure 4.7 shows the waveforms for the inductive mode. In sub-figure I, the phase shift between $v_{F,a1}$ and $i_{I,a}$ is $(-\pi/2-\gamma)$, where γ is a small positive angle. In sub-figure II for the method A, the $v'_{F,a1}$ is generated by the proposed method. Note that $V_{F,a1}$ increases smartly when $(v_{F,a1}\times i_{I,a})$ is positive, and decreases when $(v_{F,a1}\times i_{I,a})$ is negative. Compared with the control strategy in the capacitive mode, you will find that the changing direction in the inductive mode is different from that in the capacitive mode, which is determined by λ_{a1} in (4.47). Other $v'_{F,a1}$ in sub-figure III, IV and V of Figure 4.7 for methods C, D and E are the same as those of Figure 4.6, since no differences of control strategies have been pointed out in different operating modes in [11, 48, 119, 123, 125]. The additional active power generated by the $v'_{F,a1}$ in sub-figure II and III is still expressed as (4.6) and (4.7). This means that the more active power is injected into the H-bridge. However, the additional power generated by the $v'_{F,a1}$ in sub-figure IV and V is expressed as (4.10) and (4.11), which is different from (4.8) and (4.9). It means that less active power is injected into the H-bridge. Therefore, only methods A and C can work well for different operating modes, while methods D and E may not.

$$\Delta P \approx V_{F,a1} \cdot I_{I,a} \cdot \frac{\Delta\gamma}{2} \tag{4.10}$$

$$\Delta P \approx \Delta V_{F,a1} \cdot I_{I,a} \cdot \frac{\cos(-2\varphi+\gamma)}{\pi} \tag{4.11}$$

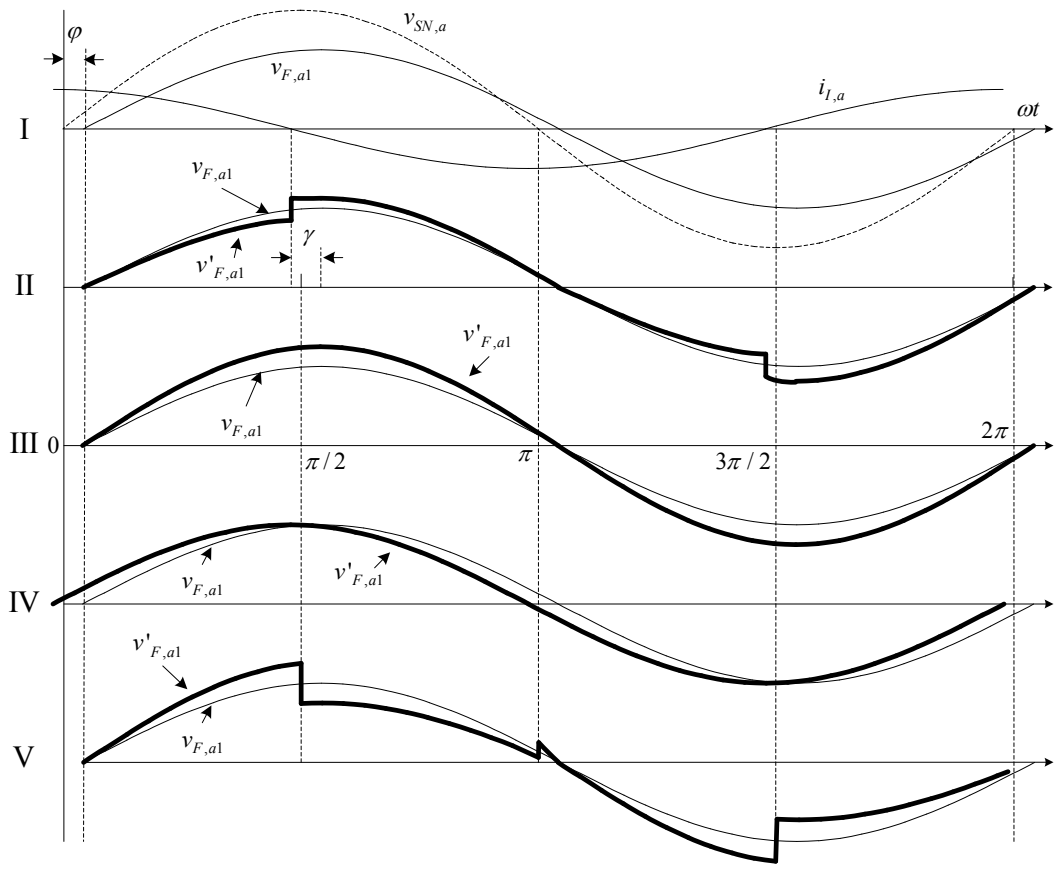


Figure 4.7. Waveforms in the inductive mode

4.4.2 Impact on voltage quality

Only methods A and C can balance DC capacitor voltages when the STATCOM works in all operating modes. Therefore, only methods A and C meet the constraint.

Here, the optimization goal is to have the less impact on original H-bridge voltage. The original H-bridge voltages are regulated slightly for controlling the DC capacitor voltages. A better method will cause less change on the original H-bridge voltage.

Let us compare methods A and C. In both the capacitive mode and the inductive mode, the additional active power by methods A and C are expressed as (4.6) and (4.7), respectively, in which γ and φ are very small. Therefore, to achieve the same ΔP, $\Delta V_{F,a1}$ in (4.6) is much smaller than that in (4.7). Therefore, to generate the same additional active power, the additional amplitude change added on the STATCOM output voltage by method A is much smaller than that by method C. Therefore, we think that the proposed method A is better.

4.5 Derivation of the proposed method

4.5.1 Modeling of STATCOM

In the following derivation,

$$j = a, b, c \qquad k = 1, 2 \tag{4.12}$$

<u>Switching model</u>

Based on the circuit as shown in Figure 4.1, we get

$$\begin{aligned} v_{H,jk} &= S_{jk} v_{dc,jk} \qquad\qquad i_{dc,jk} = S_{jk} i_{I,j} \\ v_{UN,j} &= v_{H,j1} + v_{H,j2} = S_{j1} v_{dc,j1} + S_{j2} v_{dc,j2} \end{aligned} \tag{4.13}$$

S_{jk} and $v_{dc,jk}$ are the switching functions [115] and the DC link voltages, respectively. The value of the switching function is 1 when S_1 and S_4 are turned on, and is -1 when S_2 and S_3 are turned on, and is 0 when S_1 and S_3 are turned on or when S_2 and S_4 are turned on.

Average model

The value of S_{jk} is averaged to be d_{jk}.

$$d_{jk} = \overline{S}_{jk} \tag{4.14}$$

Thus, the (4.13) is rewritten as

$$\begin{aligned} \overline{v}_{H,jk} &= d_{jk} v_{dc,jk} \qquad\qquad \overline{i}_{dc,jk} = d_{jk} i_{I,j} \\ \overline{v}_{UN,j} &= \overline{v}_{H,j1} + \overline{v}_{H,j2} = d_{j1} v_{dc,j1} + d_{j2} v_{dc,j2} \end{aligned} \tag{4.15}$$

Note:

$$d_j = d_{j1} + d_{j2} \tag{4.16}$$

4.5.2 Control loops for currents

In the derivations of control loops for currents, all DC capacitor voltages are assumed as E. Based on the circuit in Figure 4.1, we get

$$\frac{d}{dt}\begin{bmatrix} i_{I,a} \\ i_{I,b} \\ i_{I,c} \end{bmatrix} = \frac{1}{L_S}\begin{bmatrix} d_a E \\ d_b E \\ d_c E \end{bmatrix} - \frac{1}{L_S}\begin{bmatrix} v_{SN,a} \\ v_{SN,b} \\ v_{SN,c} \end{bmatrix} - \frac{R_S}{L_S}\begin{bmatrix} i_{I,a} \\ i_{I,b} \\ i_{I,c} \end{bmatrix} \tag{4.17}$$

The transformation matrix from *abc* coordinate to *dq* coordinate is

$$T = \sqrt{\frac{2}{3}}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{4.18}$$

The ωt is the output of the phase lock loop. Remark: The $v_{SN,a}$ is in phase with $\sin(\omega t)$. The small signal model in the *dq* coordinate is shown as

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{I,d}\\ \tilde{i}_{I,q}\\ \tilde{i}_{I,0}\end{bmatrix}=\frac{E}{L_S}\begin{bmatrix}\tilde{d}_d\\ \tilde{d}_q\\ \tilde{d}_0\end{bmatrix}-\frac{1}{L_S}\begin{bmatrix}v_{SN,d}\\ v_{SN,q}\\ v_{SN,0}\end{bmatrix}-\frac{R_S}{L_S}\begin{bmatrix}\tilde{i}_{I,d}\\ \tilde{i}_{I,q}\\ \tilde{i}_{I,0}\end{bmatrix}+\begin{bmatrix}\omega\tilde{i}_{I,q}\\ -\omega\tilde{i}_{I,d}\\ 0\end{bmatrix} \tag{4.19}$$

Transfer function for current loops

$$G_{id}=\frac{\tilde{i}_{I,d}}{(\tilde{d}_d+\tilde{i}_{I,q}\omega L/E)}=\frac{E/L_S}{s+R_S/L_S} \tag{4.20}$$

$$G_{iq}=\frac{\tilde{i}_{I,q}}{(\tilde{d}_q-\tilde{i}_{I,d}\omega L/E)}=\frac{E/L_S}{s+R_S/L_S} \tag{4.21}$$

$$G_{i0,d0}=\frac{\tilde{i}_{I,0}}{\tilde{d}_0}=\frac{E/L_S}{s+R_S/L_S} \tag{4.22}$$

Current loops are shown in Figure 4.8. The decoupled controller cancels the coupling parts in the model. In the loops, we consider the effects of sensor filters and digital delay. The high-frequency RC filter before the sensor is modeled as

$$G_{f,RC}=\frac{1}{1+s/p_{f,RC}} \tag{4.23}$$

The digital delay in digital controller is T_D and is modeled as

$$G_D=\frac{1-sT_D/2}{1+sT_D/2} \tag{4.24}$$

The loop gains for d and q current channel are expressed as (4.25) and (4.26). The H_{id} and H_{iq} are PI compensators.

$$T_{I,id}=H_{id}G_DG_{id}G_{f,RC} \tag{4.25}$$

$$T_{I,iq} = H_{iq} G_D G_{iq} G_{f,RC} \tag{4.26}$$

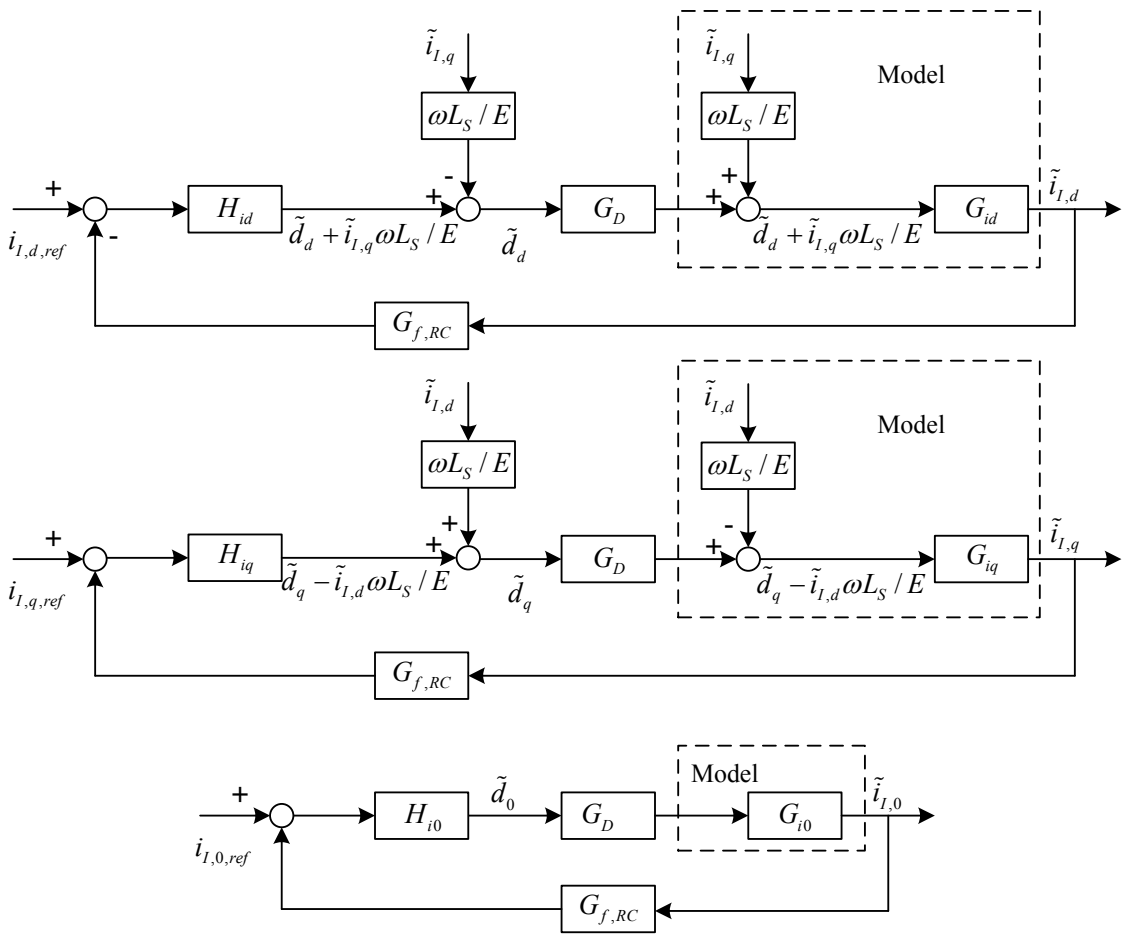


Figure 4.8. Control loops for inverter currents

4.5.3 Control loop for the summation of DC capacitor voltages

Based on the circuit in Figure 4.1, we get

$$\frac{d}{dt} v_{dc,jk} = -\frac{v_{dc,jk} + \overline{i}_{dc,jk} R_{H,jk}}{R_{H,jk} C_{dc,jk}} = -\frac{v_{dc,jk} + d_{jk} i_{I,j} R_{H,jk}}{R_{H,jk} C_{dc,jk}} \tag{4.27}$$

In the derivation of the control loop for the summation of DC capacitor voltages, $R_{H,jk}$ is assumed as R_H and $C_{dc,jk}$ is assumed as C_{dc}. Note:

$$\begin{aligned} v_{dc,j} &= v_{dc,j1} + v_{dc,j2} \\ v_{dc} &= v_{dc,a} + v_{dc,b} + v_{dc,c} \end{aligned} \tag{4.28}$$

From (4.27), (4.28) and (4.16), we get

$$\begin{aligned} \frac{d}{dt} v_{dc} &= -\frac{1}{R_H C_{dc}} v_{dc} - \frac{1}{C_{dc}} (d_a i_{I,a} + d_c i_{I,b} + d_c i_{I,c}) \\ &= -\frac{1}{R_H C_{dc}} v_{dc} - \frac{1}{C_{dc}} (d_d i_{I,d} + d_q i_{I,q} + d_0 i_{I,0}) \end{aligned} \tag{4.29}$$

The small signal model for the summation of DC capacitor voltages is

$$\frac{d}{dt} \tilde{v}_{dc} = -\frac{1}{R_H C_{dc}} \tilde{v}_{dc} - \frac{1}{C_{dc}} (\tilde{d}_d i_{I,d} + \tilde{d}_q i_{I,q} + \tilde{d}_0 i_{I,0} + d_d \tilde{i}_{I,d} + d_q \tilde{i}_{I,q} + d_0 \tilde{i}_{I,0}) \tag{4.30}$$

Transfer functions for $\tilde{d}_d$ and $\tilde{i}_{I,d}$ are expressed as (4.31) and (4.32). Transfer functions for other signals are not listed because they are not involved in the control loop.

$$G_{v,dd} = \frac{\tilde{v}_{dc}}{\tilde{d}_d} = -\frac{i_{I,d} / C_{dc}}{s + 1/(R_H C_{dc})} \tag{4.31}$$

$$G_{v,id} = \frac{\tilde{v}_{dc}}{\tilde{i}_{I,d}} = -\frac{d_d / C_{dc}}{s + 1/(R_H C_{dc})} \tag{4.32}$$

The control loop for the summation of all DC capacitor voltages is shown in Figure 4.9. The loop gain is expressed as (4.33) and the H_{dc} is a PI compensator.

$$T_{vdc} = H_{dc} \frac{H_{id} G_D G_{id}}{1 + G_f H_{id} G_D G_{id}} G_f \left(\frac{G_{v,dd}}{G_{id}} + G_{v,id} \right) \tag{4.33}$$

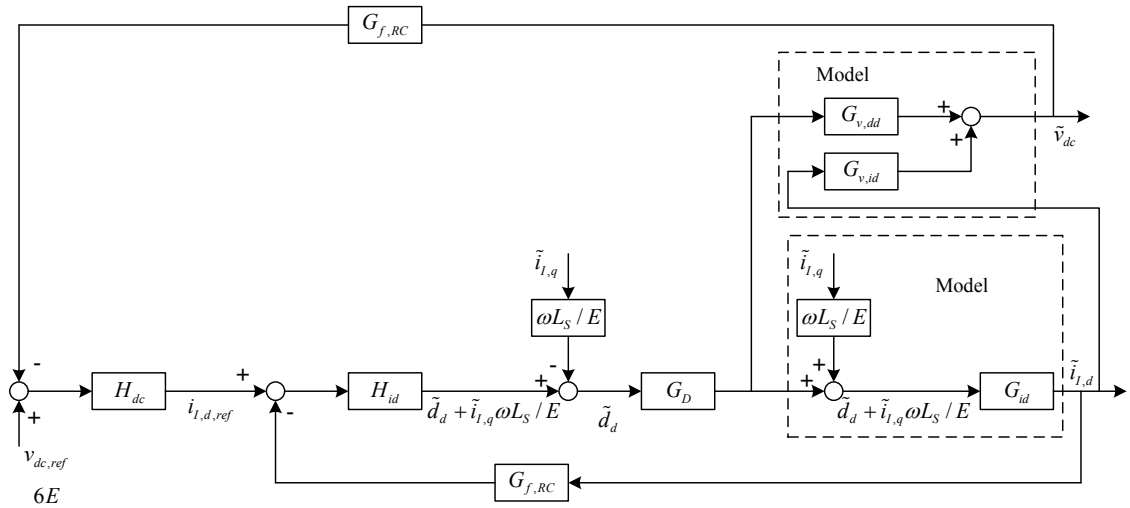


Figure 4.9. Control loop for the summation of all DC capacitor voltages

4.5.4 Control Loops for Individual DC Capacitor Voltages

Based on the circuit in Figure 4.1, for each H-bridge, we get differential functions for the DC capacitor voltage:

$$\frac{d}{dt}\begin{bmatrix} v_{dc,ak} \\ v_{dc,bk} \\ v_{dc,ck} \end{bmatrix} = -\begin{bmatrix} v_{dc,ak} / (R_{H,ak} C_{dc,ak}) \\ v_{dc,bk} / (R_{H,bk} C_{dc,bk}) \\ v_{dc,ck} / (R_{H,ck} C_{dc,ck}) \end{bmatrix} - \begin{bmatrix} d_{ak} i_{I,a} / C_{dc,ak} \\ d_{bk} i_{I,b} / C_{dc,bk} \\ d_{ck} i_{I,c} / C_{dc,ck} \end{bmatrix} \tag{4.34}$$

The transpose of T, T^{tr}, is also the inverse matrix of T. Thus, $T^{tr}T$ is a unit matrix. From (4.34) and the characteristic of T, we get

$$\frac{d}{dt}\begin{bmatrix} v_{dc,ak} \\ v_{dc,bk} \\ v_{dc,ck} \end{bmatrix} = -\begin{bmatrix} \dfrac{v_{dc,ak}}{R_{H,ak}C_{dc,ak}} \\ \dfrac{v_{dc,bk}}{R_{H,bk}C_{dc,bk}} \\ \dfrac{v_{dc,ck}}{R_{H,ck}C_{dc,ck}} \end{bmatrix} - \begin{bmatrix} \dfrac{d_{ak}}{C_{dc,ak}} & 0 & 0 \\ 0 & \dfrac{d_{bk}}{C_{dc,bk}} & 0 \\ 0 & 0 & \dfrac{d_{ck}}{C_{dc,ck}} \end{bmatrix} T^{tr} T \begin{bmatrix} i_{I,a} \\ i_{I,b} \\ i_{I,c} \end{bmatrix} \tag{4.35}$$

From the *abc* coordinate to the *dq* coordinate, we get

$$\begin{bmatrix} i_{I,d} \\ i_{I,q} \\ i_{I,0} \end{bmatrix} = T \begin{bmatrix} i_{I,a} \\ i_{I,b} \\ i_{I,c} \end{bmatrix} \tag{4.36}$$

From (4.35) and (4.36), we get the small signal model as shown in

$$\frac{d}{dt}\begin{bmatrix} \tilde{v}_{dc,ak} \\ \tilde{v}_{dc,bk} \\ \tilde{v}_{dc,ck} \end{bmatrix} = -\begin{bmatrix} \dfrac{\tilde{v}_{dc,ak}}{R_{H,ak}C_{dc,ak}} \\ \dfrac{\tilde{v}_{dc,bk}}{R_{H,bk}C_{dc,bk}} \\ \dfrac{\tilde{v}_{dc,ck}}{R_{H,ck}C_{dc,ck}} \end{bmatrix} - \sqrt{\frac{2}{3}} \begin{bmatrix} \dfrac{\tilde{d}_{ak}}{C_{dc,ak}}(i_{I,d}\sin\omega t + i_{I,q}\cos\omega t + \dfrac{i_{I,0}}{\sqrt{2}}) \\ \dfrac{\tilde{d}_{bk}}{C_{dc,bk}}(i_{I,d}\sin(\omega t - \dfrac{2\pi}{3}) + i_{I,q}\cos(\omega t - \dfrac{2\pi}{3}) + \dfrac{i_{I,0}}{\sqrt{2}}) \\ \dfrac{\tilde{d}_{ck}}{C_{dc,ck}}(i_{I,d}\sin(\omega t + \dfrac{2\pi}{3}) + i_{I,q}\cos(\omega t + \dfrac{2\pi}{3}) + \dfrac{i_{I,0}}{\sqrt{2}}) \end{bmatrix}$$

(4.37)

Thus, in the A-phase, a transfer function from an H-bridge duty cycle to the corresponding DC capacitor voltage is

$$G_{vdcd,ak} = \frac{\tilde{v}_{dc,ak}}{\tilde{d}_{ak}} = -\frac{\dfrac{1}{C_{dc,ak}}\sqrt{\dfrac{2}{3}}(i_{I,d}\sin\omega t + i_{I,q}\cos\omega t + \dfrac{i_{I,0}}{\sqrt{2}})}{s + 1/(R_{H,ak}C_{dc,ak})} \tag{4.38}$$

In the B-phase, it is

$$G_{vdcd,bk} = \frac{\tilde{v}_{dc,bk}}{\tilde{d}_{bk}} = -\frac{\frac{1}{C_{dc,bk}}\sqrt{\frac{2}{3}}(i_{I,d}\sin(\omega t - \frac{2\pi}{3}) + i_{I,q}\cos(\omega t - \frac{2\pi}{3}) + \frac{i_{I,0}}{\sqrt{2}})}{s + 1/(R_{H,bk}C_{dc,bk})} \quad (4.39)$$

In the C-phase, it is

$$G_{vdcd,ck} = \frac{\tilde{v}_{dc,ck}}{\tilde{d}_{ck}} = -\frac{\frac{1}{C_{dc,ck}}\sqrt{\frac{2}{3}}(i_{I,d}\sin(\omega t + \frac{2\pi}{3}) + i_{I,q}\cos(\omega t + \frac{2\pi}{3}) + \frac{i_{I,0}}{\sqrt{2}})}{s + 1/(R_{H,ck}C_{dc,ck})} \quad (4.40)$$

Remark: Based on the above three transfer functions, the control strategy for balancing DC capacitor voltages can be designed for the multilevel inverter working with multilevel SPWM, which is not coved here. I have only focused on the control strategy for a multilevel inverter working with the optimal combination modulation.

Consider an H-bridge in the A-phase. The output voltage is shown in Figure 4.5. The fundamental component of the H-bridge output voltage can be expressed as

$$v_{F,ak} = V_{F,ak}\sin(\omega t + \arctan(d_q / d_d)) \quad (4.41)$$

Note that the $v_{SN,a}$ is in phase with $\sin(\omega t)$. The $V_{F,ak}$ is the amplitude of the $v_{F,ak}$. Approximately, the duty cycle for the H-bridge can be express as

$$d_{ak} = v_{F,ak} / E \quad (4.42)$$

The amplitude, $V_{F,ak}$, is calculated by the switching angles.

$$V_{F,ak} = \frac{4E}{\pi}(\cos\theta_{1,ak} - \cos\theta_{2,ak} + \cos\theta_{3,ak} - \cos\theta_{4,ak} + \cos\theta_{5,ak}) \quad (4.43)$$

From (4.41), (4.42) and (4.43), we get

$$d_{ak} = (4/\pi)\cdot\sin(\omega t + \arctan(d_q / d_d)) \\ \cdot(\cos\theta_{1,ak} - \cos\theta_{2,ak} + \cos\theta_{3,ak} - \cos\theta_{4,ak} + \cos\theta_{5,ak}) \tag{4.44}$$

In Figure 4.5, the dotted waveform is the voltage after a small angle shift for switching angles. All five switching angles have the same angle shift, $\tilde{\theta}_{ak}$. Please note the shifting directions of angles as shown in Figure 4.5. Thus, the small signal function for (4.44) is expressed as (4.45).

$$\tilde{d}_{ak} = \tilde{\theta}_{ak}\cdot(4/\pi)\cdot\sin(\omega t + \arctan(d_q / d_d)) \\ \cdot(\sin\theta_{1,ak} + \sin\theta_{2,ak} + \sin\theta_{3,ak} + \sin\theta_{4,ak} + \sin\theta_{5,ak}) \tag{4.45}$$

Remark: If the inverter functions with other optimal modulation [11, 27, 86, 110, 127, 128], the equation (4.45) needs to have a slight modifications.

From (4.38) and (4.45), we get the transfer function from an angle shift to the corresponding DC capacitor voltage in the A-phase.

$$G_{vdc\theta,ak} = \frac{\tilde{v}_{dc,ak}}{\tilde{\theta}_{ak}} = -\frac{\sqrt{\frac{2}{3}}\frac{4}{\pi C_{dc,ak}}}{s + 1/(R_{H,ak}C_{dc,ak})}\lambda_{ak} \tag{4.46}$$

$$\lambda_{ak} = (i_{I,d}\sin\omega t + i_{I,q}\cos\omega t + i_{I,0}/\sqrt{2}) \\ \cdot\sin(\omega t + \arctan(d_q / d_d)) \\ \cdot(\sin\theta_{1,ak} + \sin\theta_{2,ak} + \sin\theta_{3,ak} + \sin\theta_{4,ak} + \sin\theta_{5,ak}) \tag{4.47}$$

The transfer function for the B-phase is

$$G_{vdc\theta,bk} = \frac{\tilde{v}_{dc,bk}}{\tilde{\theta}_{bk}} = -\frac{\sqrt{\frac{2}{3}}\frac{4}{\pi C_{dc,bk}}}{s+1/(R_{H,bk}C_{dc,bk})}\lambda_{bk} \tag{4.48}$$

$$\begin{aligned}\lambda_{bk} = &(i_{I,d}\sin(\omega t - 2\pi/3) + i_{I,q}\cos(\omega t - 2\pi/3) + i_{I,0}/\sqrt{2}) \\ &\cdot \sin(\omega t - 2\pi/3 + \arctan(d_q/d_d)) \\ &\cdot (\sin\theta_{1,bk} + \sin\theta_{2,bk} + \sin\theta_{3,bk} + \sin\theta_{4,bk} + \sin\theta_{5,bk})\end{aligned} \tag{4.49}$$

The transfer function for the C-phase is

$$G_{vdc\theta,ck} = \frac{\tilde{v}_{dc,ck}}{\tilde{\theta}_{ck}} = -\frac{\sqrt{\frac{2}{3}}\frac{4}{\pi C_{dc,ck}}}{s+1/(R_{H,ck}C_{dc,ck})}\lambda_{ck} \tag{4.50}$$

$$\begin{aligned}\lambda_{ck} = &(i_{I,d}\sin(\omega t + 2\pi/3) + i_{I,q}\cos(\omega t + 2\pi/3) + i_{I,0}/\sqrt{2}) \\ &\cdot \sin(\omega t + 2\pi/3 + \arctan(d_q/d_d)) \\ &\cdot (\sin\theta_{1,ck} + \sin\theta_{2,ck} + \sin\theta_{3,ck} + \sin\theta_{4,ck} + \sin\theta_{5,ck})\end{aligned} \tag{4.51}$$

The index λ_{jk} is very important. The value of λ_{jk} keeps changing. It can be positive, negative or zero. Figure 4.2 shows the control loop for an individual DC capacitor voltage in the A-phase. Figure 4.3 and Figure 4.4 show those in the B-phase and C-phase, respectively. In the control loops, we have a compensator, $H_{\lambda,jk}$, to cancel the effect of λ_{jk}. This is the key part of the proposed control strategy.

$$H_{\lambda,jk} = 1/\lambda_{jk} \tag{4.52}$$

The loop gain for control loops is expressed as (4.53). $H_{ind,jk}$ is a PI compensator.

$$T_{ind,jk} = \frac{4}{\pi C_{dc,jk}}\sqrt{\frac{2}{3}}\frac{G_D G_f H_{ind,jk}}{s+1/(R_{H,jk}C_{dc,jk})} \tag{4.53}$$

4.6 Verifications

4.6.1 Simulation for the prototype system

The performance of the proposed control strategy has been verified by simulations and experiments. The simulation investigations were performed by MATLAB Simulink and the hardware prototype has been built in the laboratory.

The parameters of the STATCOM for both the simulation and the experimental prototype are the same. The rating is 500 VAr due to limitation of the power source in the experimental prototype. The VPCC are 56 V (line-to-line, RMS). The current rating is 5.15 A. The inductance of interface inductors is 2.5 mH. The Equivalent Series Resistance (ESR) of interface inductors is 0.22 Ω. The DC capacitor voltages are 29.2 V. The capacitance of DC capacitors is 2700 μF. The ESR of DC capacitors is 11 mΩ. The switching devices are the IGBT modules (PM50RSA120).

The parameters of the controllers for both the simulation and the experimental prototype are the same. The loop gains for *d* channel and *q* channel currents are expressed as (4.25) and (4.26). I have designed the same loop gain for *d* channel current and *q* channel current. The parameters of the PI controllers are (P = 0.056, I = 14.4). The bandwidth is 69 Hz and the phase margin is 62°. The loop gain for the summation of DC capacitor voltages is expressed as (4.33). The parameters of the PI controller are (P = 0.36, I = 0.46). The bandwidth is 44 Hz and the phase margin is

56.7°. The loop gain for the individual DC capacitor voltages is expressed as (4.53). The parameters of the PI controllers are (P = 70, I = 3.7). The bandwidth is 8.1 Hz and the phase margin is 89.5°.

Figure 4.10 to Figure 4.15 are simulation results. Figure 4.10 shows that the controller can balance DC capacitor voltages when H-bridges have different parameters. Figure 4.11 shows that the controller works well when H-bridges always switch with different switching patterns. Figure 4.12, Figure 4.13 and Figure 4.14 show the performance of the controller when the STATCOM works in the capacitive mode, the inductive mode and the standby mode, respectively. Figure 4.15 shows the performance during the step changes between different references of reactive power.

In the simulation shown in Figure 4.10, the STATCOM functions in the capacitive mode (reference reactive power is 400 VAr). The switching patterns are swapped around every six cycle between two H-bridges in a phase. The different ripples of DC capacitor voltages imply the different switching patterns. To get imbalanced parameters of H-bridges, an extra 220 Ω resistor is connected in parallel to the DC capacitor in the first H-bridge of A-phase. At the same time, another 220 Ω resistor is connected to the DC capacitor in the second H-bridge of B-phase. The controllers for individual DC capacitor voltages stop working between 0.6 S and 1.2 S. Thus, the angle shifts and outputs of the controller are zero during this period. As shown in Figure 4.10, after the controllers stop working at 0.6 S, $v_{dc,a1}$ and $v_{dc,b2}$ start decreasing

due to more power losses caused by the 220 Ω resistors. This means that the DC capacitor voltages cannot be balanced by only swapping switching patterns if there are parameter imbalances. After 1.2 S, the proposed controller functions, then the DC capacitor voltages are balanced. In addition, the angle shifts are less than 0.5^{o} in steady state. These small angle shifts will not deteriorate the voltage quality.

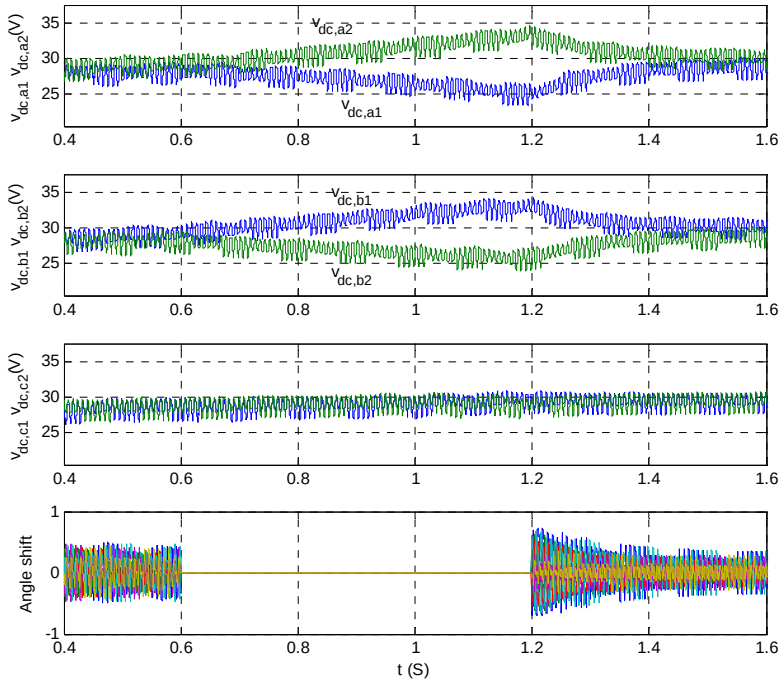


Figure 4.10. Simulation waveforms when H-bridges have different parameters

The simulation shows in Figure 4.11 that H-bridges have the same parameters, but switching patterns are not swapped. In one phase, two different ripples of DC capacitor voltages indicate the two H-bridges always switch with different switching patterns. The controllers for individual DC capacitor voltages stop functioning between 0.6 S

and 1.2 S. The DC capacitor voltages become imbalanced after 0.6 S. This means that different switching patterns cause imbalance of DC capacitor voltages. After 1.2 S, the proposed controller functions, then the DC capacitor voltages are balanced.

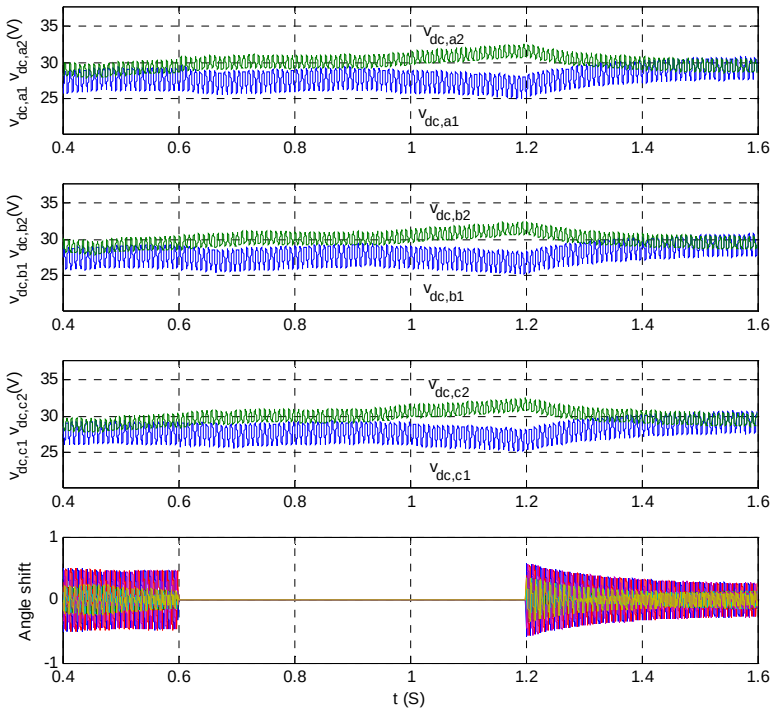


Figure 4.11. Simulation waveforms when H-bridges switch with different switching patterns

The simulations shown in Figure 4.12, Figure 4.13, Figure 4.14 and Figure 4.15, H-bridges have different parameters, like the case shown in Figure 4.10. Also, H-bridges always switch with different switching patterns, like the case in Figure 4.15.

Figure 4.12 shows the case where the STATCOM is in the capacitive mode. Before 0.4 S, the references for $v_{dc,c1}$ and $v_{dc,c2}$ in the controller are set as 25 V and 33

V, respectively. After 0.4 S, all references are set as 29.2 V. Figure 4.12 shows the two DC capacitor voltages, output voltage of the inverter and the current in the C-phase. After all references of individual DC capacitor voltages are set as the same value, the DC capacitor voltages are balanced. Figure 4.13 and Figure 4.14 show the cases when the STATCOM is in the inductive mode and the standby mode, respectively.

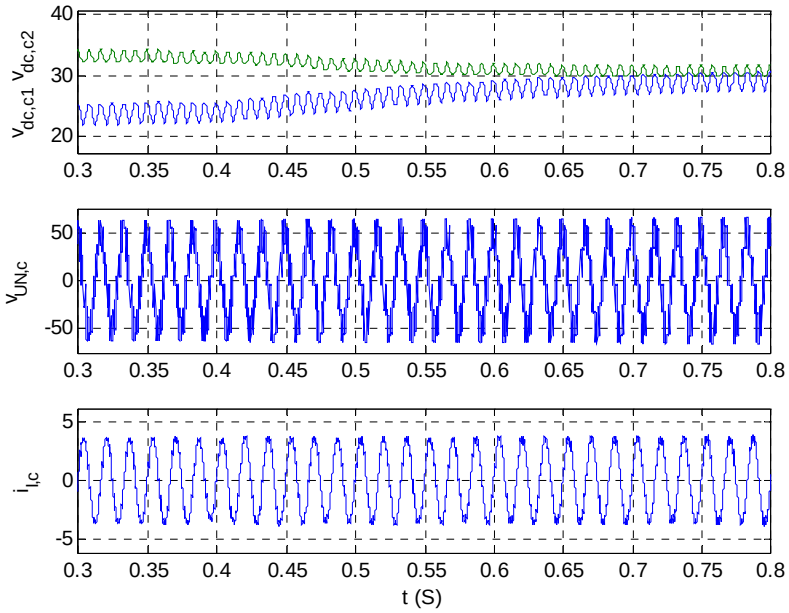


Figure 4.12. Simulation waveforms in the capacitive mode

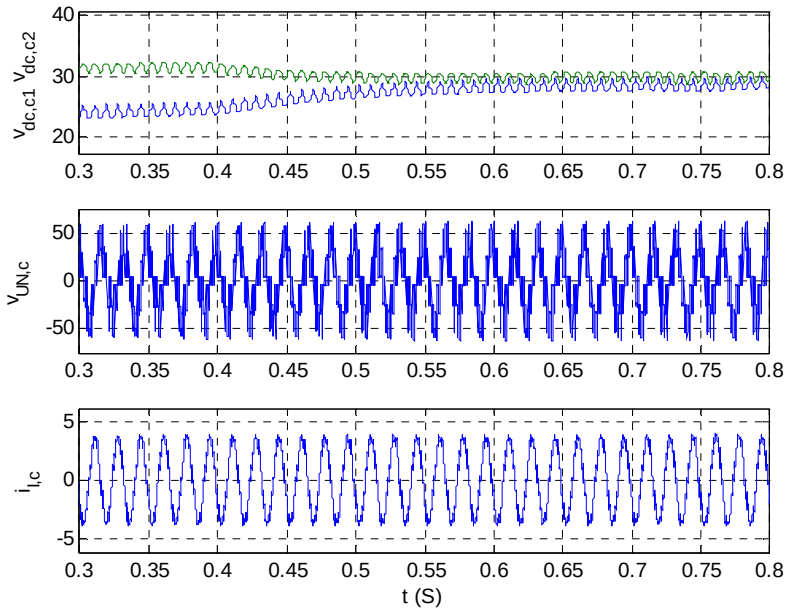


Figure 4.13. Simulation waveforms in the inductive mode

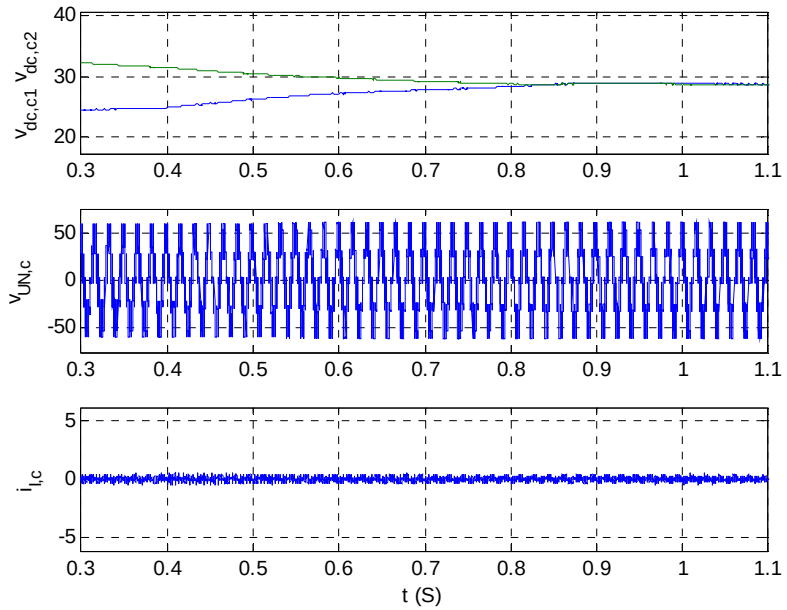


Figure 4.14. Simulation results in the standby mode

Figure 4.15 shows the simulation waveforms when the reference value of reactive power has step changes. The reference has the step changes from -400 VAr to 50 VAr at 1 S, from 50 VAr to 400 VAr at 1.4 S, and from 400 VAr to -50 VAr at 1.8 S. The negative reference of reactive power indicates the STATCOM is in the capacitive mode, while the positive one indicates the inductive mode. In this case, all references of individual DC capacitor voltages are set as the same value. As shown in Figure 4.15, DC capacitor voltages are balanced during step changes.

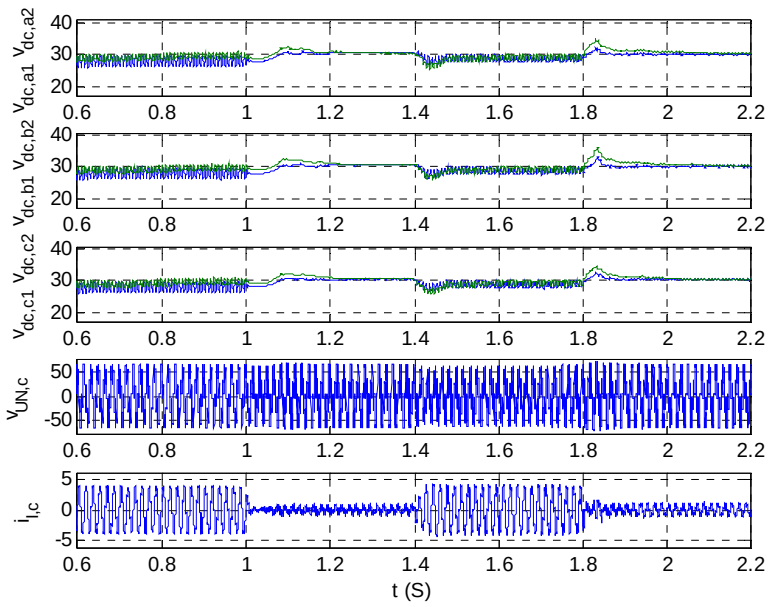


Figure 4.15. Simulation waveforms during the step changes between different references of reactive power

4.6.2 Experiment for the prototype system

To verify the performance the proposed control strategies, a hardware prototype has been built in the laboratory as shown in Figure 4.16. Six IGBT modules are built as six H-bridges.

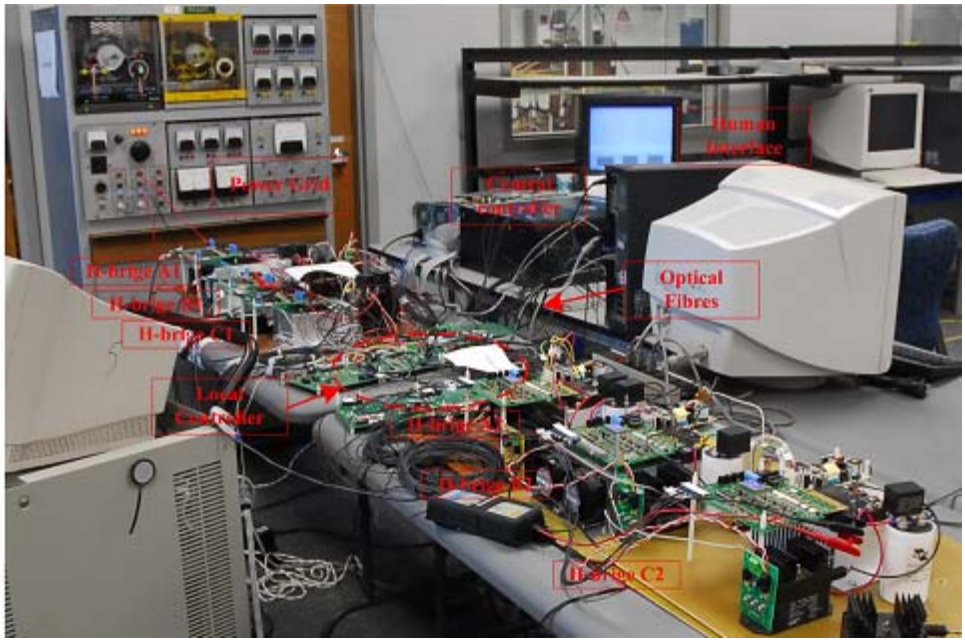


Figure 4.16. Hardware prototype setup

The architecture of the controller hardware is shown in Figure 4.17. It consists of six local controllers, one for each ETO H-bridge converter, and one central controller. The central controller includes a TMS320C6701 DSP board, an AED 106 FPGA daughter board and two PCI boards mounted with Altera FLEX 10k30A FPGA. What makes this control system unique is the fact that the local controller is a part of the

power converter itself. It forms the optical interface of the power converter, thus making it a black box that converts light-signals to high-power electric-signals. In addition to the above, the local controller provides local protection, monitors the health of the converter, and sends status feedback and telemetry signals to the central-controller. The central controller runs control algorithms, high-level protection, and communication with the Human Interface and SCADA systems.

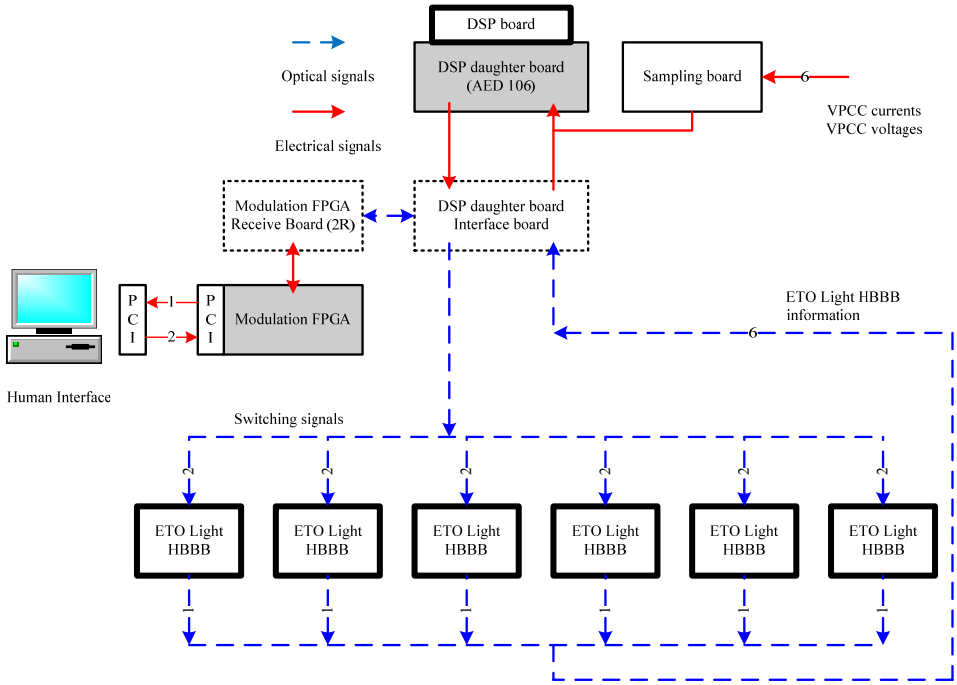


Figure 4.17. Architecture of the distributed controller

In experiments, H-bridges have different parameters, like the simulation case in Figure 4.10. Also, the H-bridges always switch with different switching patterns, like the simulation case in Figure 4.11.

Figure 4.18 shows the experimental waveforms when the STATCOM functions in the steady state. In Figure 4.18, channels 1 and 2 are the output voltages of two H-bridges in the C-phase. Channels 3 and 4 are the five-level output voltages of the inverter and the phase current in the C-phase.

In Figure 4.19, Figure 4.20, Figure 4.21 and Figure 4.22, the channels 1 and 2 are two DC capacitor voltages in the C-phase. Channels 3 and the channel 4 are the five-level output voltage of the inverter and the phase current in the C-phase.

Figure 4.19 shows the experimental waveforms when the STATCOM runs in the capacitive mode. Initially, the references of two DC capacitor voltages are 25V and 33V. Figure 4.19 shows the transition after both references are set as 29.2 V. Figure 4.20 shows the case in the inductive mode. From Figure 4.19 and Figure 4.20, we can find that the ripples of DC capacitor voltages are different. This implies H-bridges switch with different switching patterns. Figure 4.21 shows the case in the standby mode. The experimental results shown in Figure 4.19, Figure 4.20 and Figure 4.21 verify the simulation results shown in Figure 4.12, Figure 4.13 and Figure 4.14, respectively.

Figure 4.22 shows the experimental waveforms when the STATCOM functions in different operating modes. First, the reference of reactive power decreases from 0 to -450 VAr gradually in 400 ms. Then the reference increases from -450 VAr to 450 VAr

in 800 ms. Finally, the reference decreases from 450 VAr to 0 in 400 ms. As shown in Figure 4.22, the DC capacitor voltages are balanced in the whole operating regions.

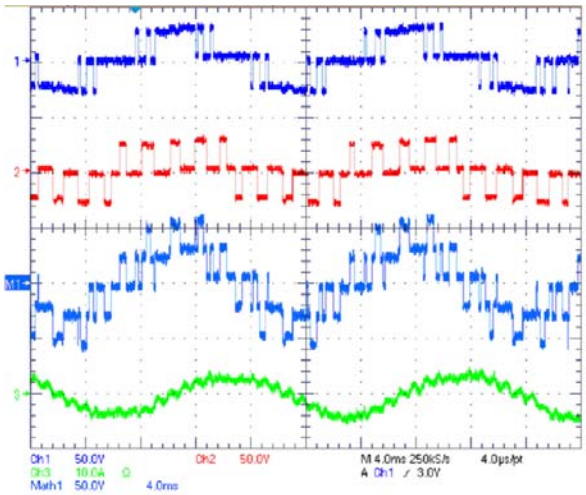


Figure 4.18. The detailed H-bridge output voltages and current

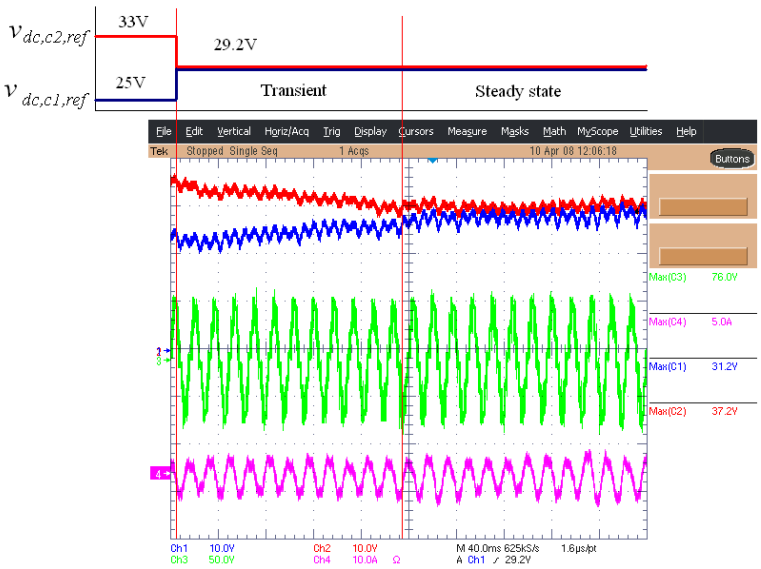


Figure 4.19. Experimental waveforms in the capacitive mode

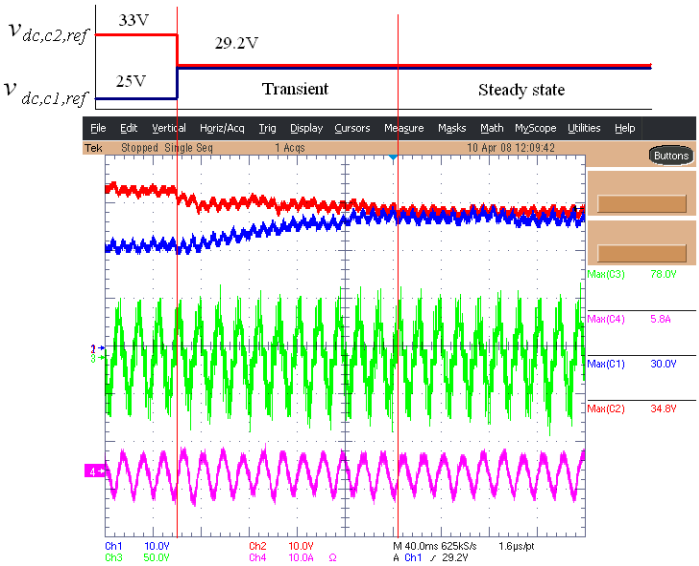


Figure 4.20. Experimental waveforms in the inductive mode

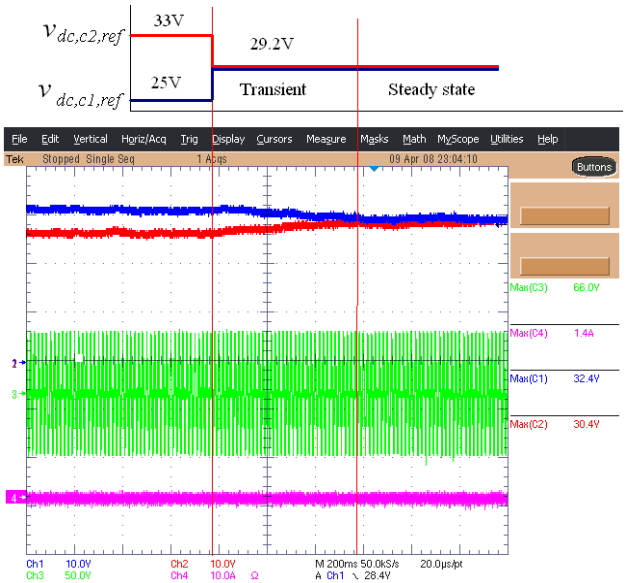


Figure 4.21. Experimental waveforms in the standby mode

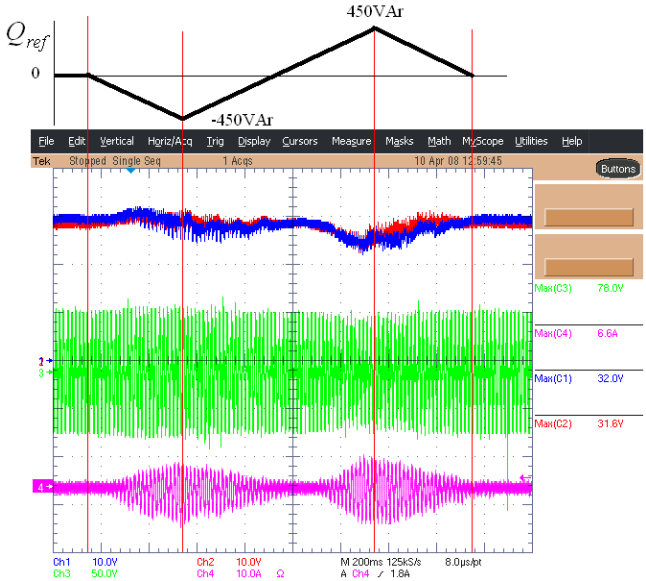


Figure 4.22. Experimental waveforms during different operating modes

4.6.3 Simulation for 10 MVA STATCOM

The designed control strategy is for a 10 MVAr STATCOM that will mitigate voltage fluctuations caused by a wind farm. The topology of the STATCOM is shown in Figure 4.1 and the parameters are shown in Table 4.1. The base voltage is 4.16 kV. The base current is 2.4 kA. The base power is 17.3 MVA. The base impedance is 1 Ω. The design of controller parameters is based on p. u. values. The loop gains for *d* channel and *q* channel currents are expressed as (4.25) and(4.26). Here, we design the same loop gain for *d* channel current and *q* channel current. The parameters of the PI controller are (P=0.29, I=73.46). The bandwidth is 69 Hz and the phase margin is 62°. The loop gain for the summation of DC capacitor voltages is expressed as (4.33). The parameters of the PI controller are (P=2.3, I=2.9). The bandwidth is 44 Hz and the phase margin is 56.7^{o}. The loop gain for the individual DC capacitor voltages is expressed as (4.53). The parameters of the PI controller are (P=1.8, I=0.095). The bandwidth is 14.5 Hz and the phase margin is 89.5^{o}.

The performance of the proposed control strategy for the five-level cascade multilevel inverter based STATCOM has been verified by simulations. The simulation investigations were performed by MATLAB Simulink. The parameters used in the simulation are p. u. values. We add small changes to the parameters of components in H-bridges to generate parameter variations for different H-bridges.

Table 4.1. Parameters of the 10 MVAr STATCOM

Parameters	**Nominal Value**	**p. u.**
Power rating	10MVAr	0.578
Line-line voltage	4.16 kV	1
Phase current	1.39 kA	0.578
Transmission Line voltage	69 kV	16.59
Transformer	69kV/4.16kV	16.59/1
Dc capacitor voltage	2170 kV	0.52
Dc capacitors	12 mF	0.012
Resistance of DC capacitor	2.3 mΩ	0.0023
Interface inductors	0.69 mH	0.0007
Interface resistor	26 mΩ	0.026
Device: Emitter turn-off thyristor [129]		
Device Ron	1 mΩ	0.001
Device forward voltage	3.3 V	0.0008
Diode forward voltage	3.1 V	0.0007
Fall time	1 µs	1 µs
Tail time	3 µs	3 µs
Snubber resistance	100 kΩ	100k
Snubber capacitance	inf	Inf
Filter R	4 Ω	4
Filter C	1 nF	1 n
Digital delay	100 µs	100 µs

Figure 4.23 shows the simulation waveforms in the capacitive mode. The reference of Iq is -1, which means that the rms value of phase current should be 1/sqrt(3) = 0.578 p. u. that is the nominal current rating of the STATCOM as shown in Table 4.1. The amplitude of the nominal current is 0.82 p. u. The first three figures show the DC capacitor voltages in the A-phase, B-phase and C-phase, respectively. The fourth figure is the output voltage of the inverter in the A-phase. The fourth figure shows the inverter currents. The fifth figure show six angle shifts for balancing six individual DC

capacitor voltages. The shapes of 120 Hz ripples of the two DC capacitor voltages in a phase are different. This implies that the two H-bridges in a phase run with different switching patterns. Without additional individual DC capacitor voltage control, the different switching patterns will cause different active power flowing into H-bridges. This causes DC capacitor voltage imbalance. In the simulation as shown in Figure 4.23, before 0.4s, the references are for $v_{dc,a1}$, $v_{dc,a2}$, $v_{dc,b1}$, $v_{dc,b2}$, $v_{dc,c1}$, $v_{dc,c2}$ are 0.44, 0.6, 0.6, 0.44, 0.52 and 0.52, respectively. After 0.4s, all references are 0.52. From simulation results as shown in Figure 4.23, we find that all DC capacitor voltages are controlled to be 0.52 after 0.4s. This verifies the controller performance when H-bridges have different switching patterns and parameter variations. From Figure 4.23, we also find that maximum angle shifts are less than 0.7^{o} when the system is stable. These small angle shifts will not deteriorate the voltage quality.

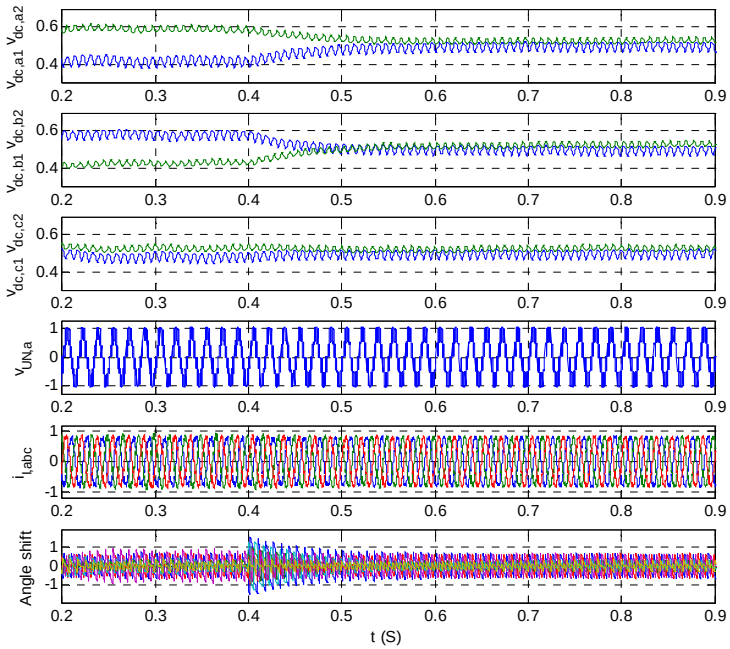


Figure 4.23. Simulation waveforms in the capacitive mode

Figure 4.24 shows a case in the inductive mode. The Iq reference is 1. Different shapes of DC capacitor voltage ripples indicate that H-bridges run with different switching patterns. Reference settings of DC capacitor voltages are the same as the simulation in Figure 4.23. After 0.4s, DC capacitor voltages are controlled to be equal. This verifies the controller performance in the inductive mode. We also find that the angle shifts are small.

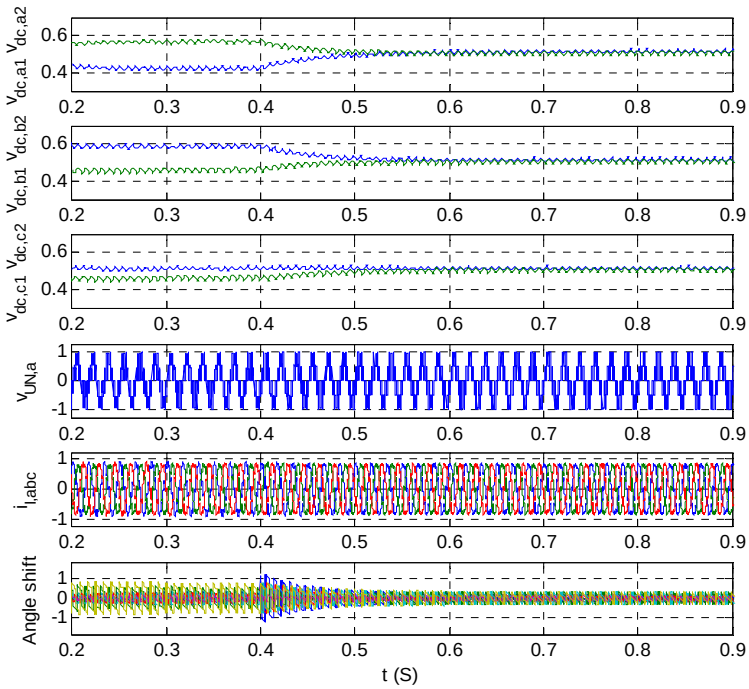


Figure 4.24. Simulation waveforms in the inductive mode

Figure 4.25 shows the case in the standby mode. The Iq reference is 0. Small inverter currents are only for compensating the inverter power losses. Reference settings of DC capacitor voltages are the same as the simulation in Figure 4.23 and Figure 4.24. After 0.4 s, the DC capacitor voltages are controlled to be equal. This verifies the controller performance in the standby mode. When the system is stable, no ripples are on the DC capacitor voltages and the angle shifts are small.

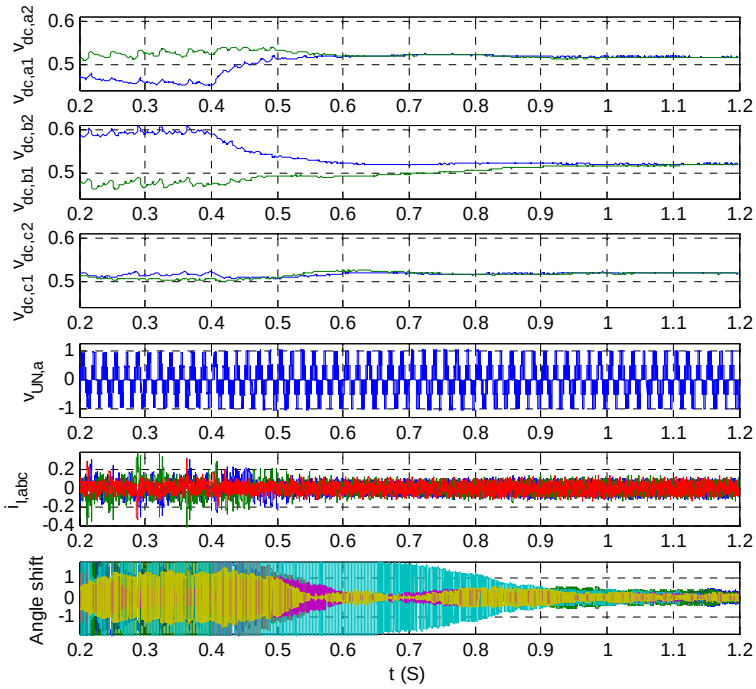


Figure 4.25. Simulation results in the standby mode

Figure 4.26 shows the simulation waves when the Iq reference has step changes. The reference has step changes from -0.8 to 0.1 at 0.5s, from 0.1 to 0.8 at 0.8s and from 0.8 to -0.1 at 1.1s. As shown in Figure 4.26, DC capacitor voltages are balanced during step changes between different references of reactive power.

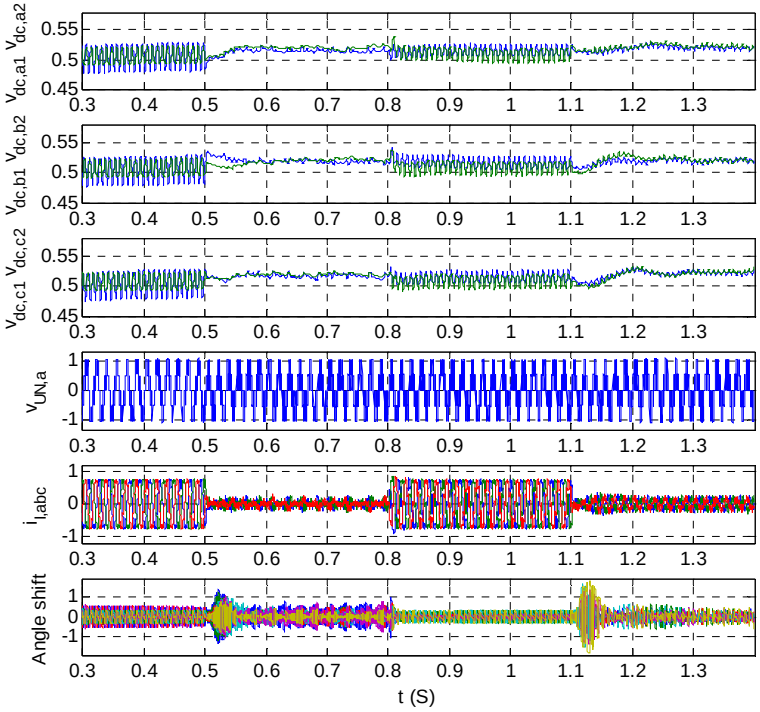


Figure 4.26. Simulation waveforms during the step changes between different references of reactive power

4.6.4 Controller hardware in-the-loop test results for 10MVA STATCOM

Advanced modulation strategy and control strategies have been developed for the five-level inverter based STATCOM. Also, the distributed controller hardware configurations show the merits of modularization and extendibility. The traditional process of developing a controller (including hardware and software) for high power electronic applications such as a STATCOM is:

1) Design the controller and verify performance by simulation;

2) Develop controller hardware and implement control algorithm in the controller hardware;

3) Test the controller with low power laboratory prototype system;

4) Validate the controller with the system by field test.

Recently, a Controller Hardware-In Loop (CHIL) test has been proposed to validate and predict controller performance under different system conditions before field test. For the CHIL test, the 10 MVA cascade multilevel converter STATCOM system and associated utility networks are modeled in a Real-Time Digital Simulator (RTDS). The controller hardware is connected to the RTDS through interface boards. The controller hardware communicates with RTDS to perform the real-time tests.

The CHIL test can help us identify problems that cannot be observed in the experiments of the laboratory prototype. Since complete models of power electronic systems and utility systems are involved in the test, the testing results can show the impact of power electronic system on utility system and help us tune both controller parameters and protection settings.

The deployment of the STATCOM is for the 50 MW Condon wind farm in Oregon in Bonneville Power Administration (BPA) network, as shown in Figure 4.27. As the Condon wind farm utilizes fixed-speed induction machines connected to a relatively weak portion of the 69kV BPA system, this site exhibits high sensitivity of voltage to reactive power injections. Based on the size of the local substation capacitor

bank (C_1 – C_8 in Figure 4.27), a 10 MVA STATCOM has been proposed initially to solve severe short term (seconds to minutes) voltage fluctuation occurring in the system [130]. In the meantime, the root cause of theses fluctuations has been traced down to intermittent malfunctioning of the substation capacitor bank controls caused by lack of a backup power for the controls. Nevertheless, this wind farm application was still considered a good site to field test the 10 MVA STATCOM.

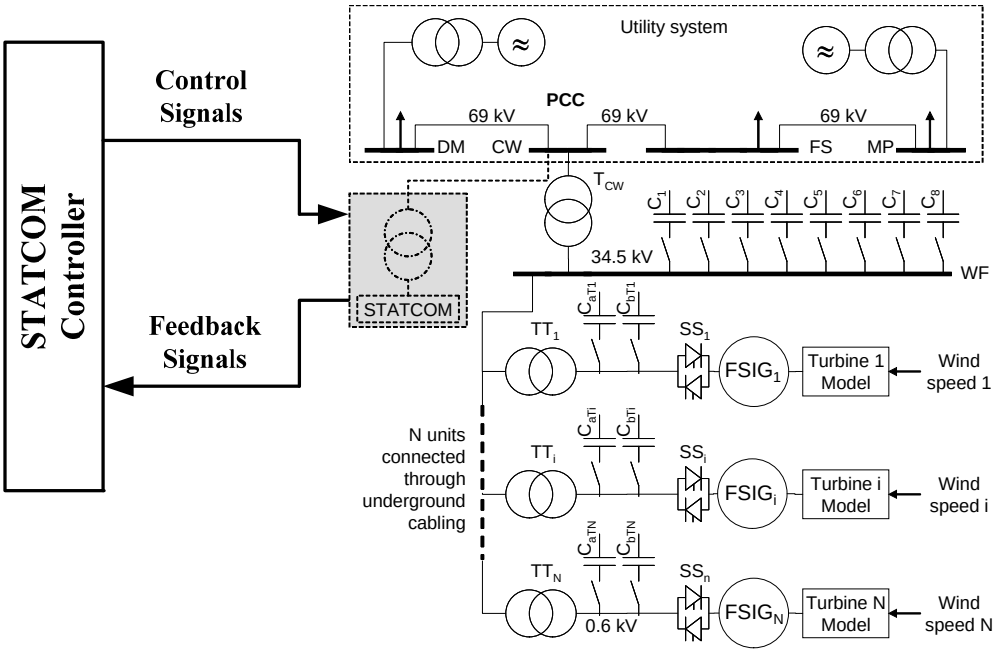


Figure 4.27. Controller and 10 MVA STATCOM for the Condon wind farm in Oregon

The CHIL testing of the controller is done with a detailed scaled model of the 50 MW wind farm and 69kV utility system. Figure 4.28 shows the configuration for the CHIL test and Figure 4.29 shows the photo of the test setup. The STATCOM, the wind

farm, and the relevant portion of the BPA system were modeled on a RTDS. The 50 MW wind farm consists of 83 fixed-speed induction generators (FSIG). With the available 14-rack RTDS system up to 72 individual wind turbine models of this type could be implemented on 12 racks leaving one rack for the surrounding utility system and one rack for the 5-level STATCOM model. However, in the absence of a native dual speed induction motor model in RTDS two machine models were used to represent one turbine. Hence, the model consists of 36 turbines representing the 83 actually existing on site. A detailed description of the implementation and validation of this model in RTDS can be found in [131, 132]. The implementation of the five-level STATCOM model on the real time simulator, described in detail in [133], utilizes a full switching model, simulated with a 2 μs time-step size. The above model is implemented in the commercial RTDS, which utilizes the Dommel algorithm for electromagnetic transient simulations. The STATCOM controller hardware and control algorithm has been described in Section II.

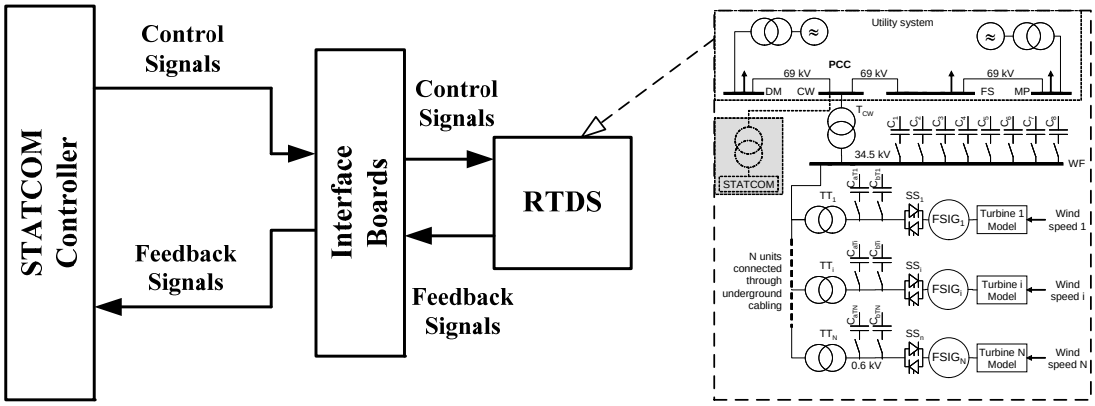


Figure 4.28. Configuration of STATCOM controller hardware-in-the-loop test

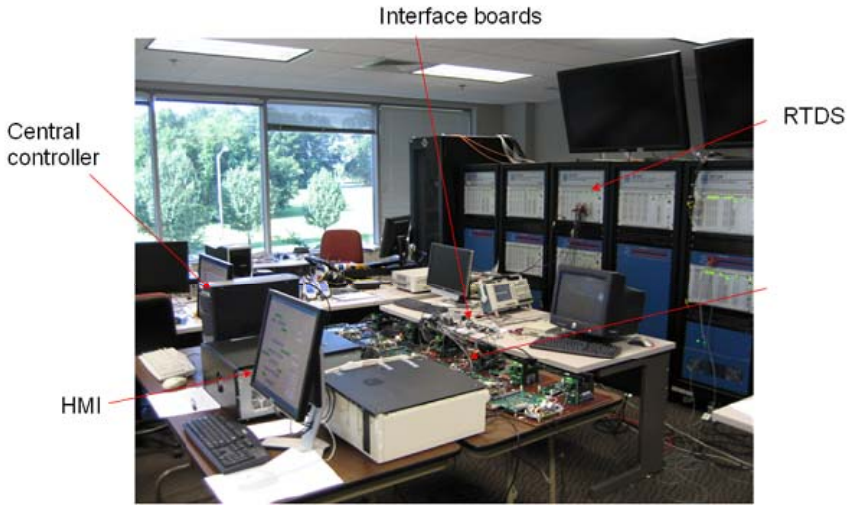


Figure 4.29. Photo of test setup for STATCOM controller hardware-in-the-loop

Additionally, as shown in Figure 4.28, interface boards are required and have been developed between the STATCOM controller and the RTDS. The control signals are 24 firing pulses to 24 ETOs emulated inside the RTDS, two switch command signals for pre-charging the DC capacitors, one protection signal, six signals for six capacitor

banks and one signal for the circuit breakers. The feedback signals are three VPCC signals, three currents, six DC capacitor voltages and one protection signal. The interface boards and signal channels are shown in Figure 4.30 and Figure 4.31.

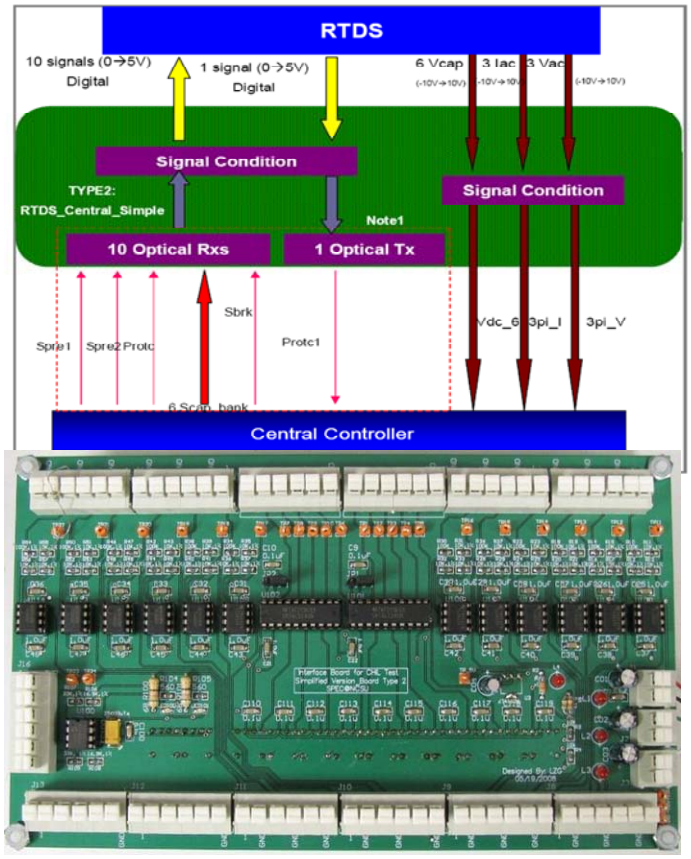


Figure 4.30. Signal paths and interface board for STATCOM central controller

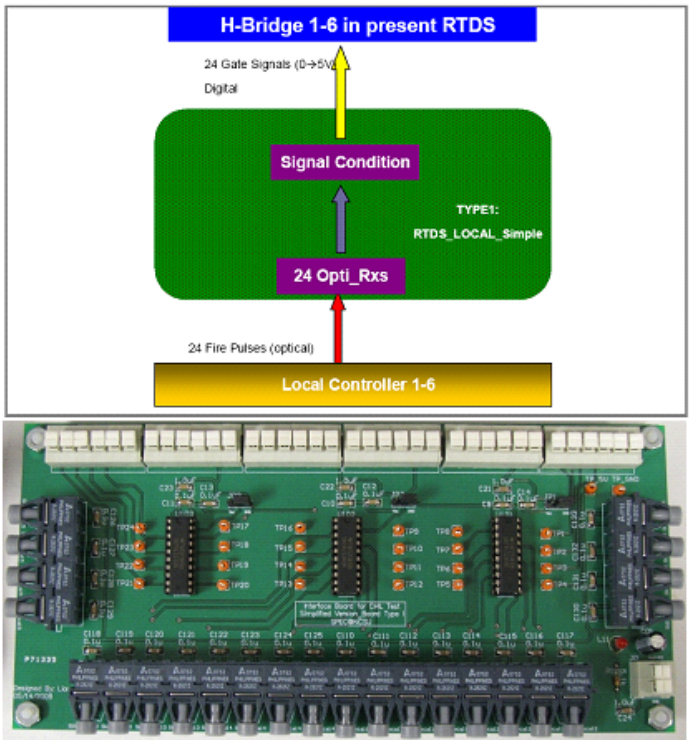


Figure 4.31. Signal paths and interface board for STATCOM local controllers

Figure 4.32 and Figure 4.33 show the CHIL test waveforms when the STATCOM is under the steady state and in capacitive mode (-0.8 pu Iq) and inductive mode (0.8 pu Iq), respectively. The VPCC phase voltage, the three-phase output voltages of the cascade multilevel inverter, output current and individual DC bus voltages are shown in Figure 4.32 and Figure 4.33. The base voltage is 4.16 kV. The base current is 2.4 kA. The spikes on the inverter voltages comes from the inverter model in the RTDS [133]. The six DC capacitor voltages are well balanced. This verifies the new proposed

control for balancing individual DC capacitor voltages. The nominal DC voltage is 2.17 kV.

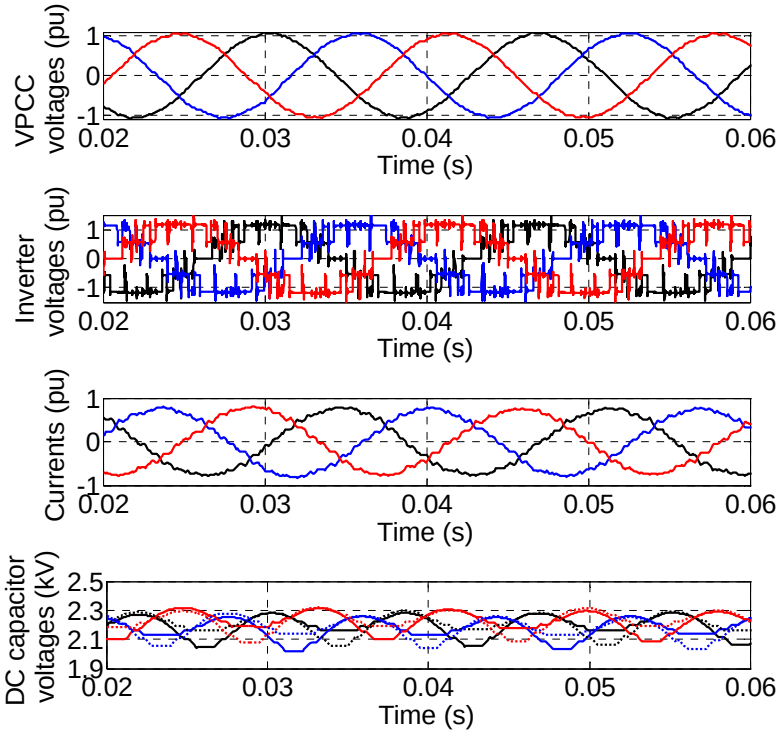


Figure 4.32. Steady state STATCOM waveforms in capacitive mode

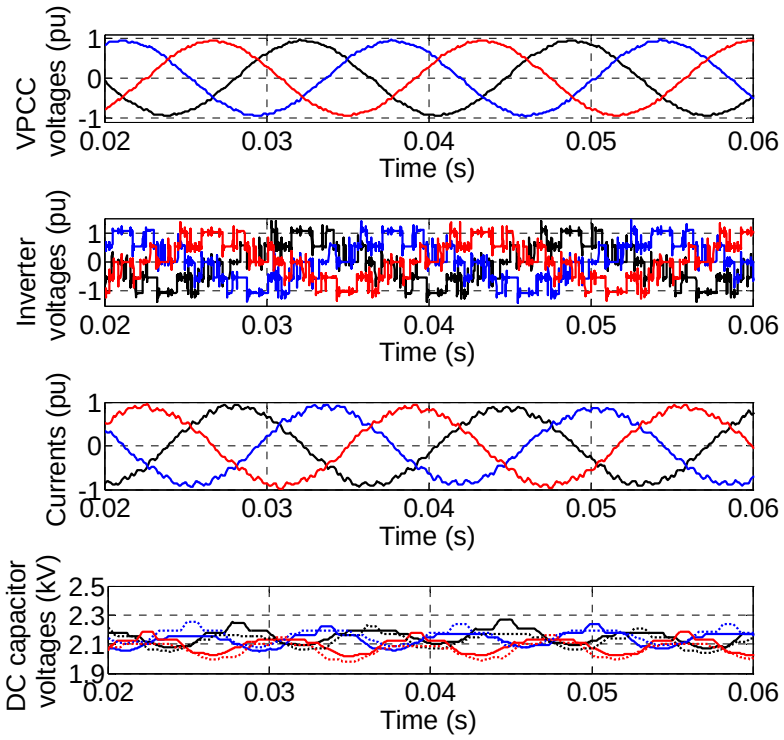


Figure 4.33. Steady state STATCOM waveforms in inductive mode

Figure 4.34 shows the waveforms when the STATCOM responds to a step change of Iq reference from 0.8 pu (inductive mode) to –0.8 pu (capacitive mode). Figure 4.35 shows the waveforms when the STATCOM responds to a ramp change where the Iq reference changes from 0.8 pu (inductive mode) to -0.8 pu (capacitive mode) gradually in 50 ms. Figure 4.36 and Figure 4.37 shows the cases where Iq reference changes from -0.8 pu (capacitive mode) to 0.8 pu (inductive mode). For the cases in Figure 4.34 and Figure 4.35, the VPCC increases 6%, whereas for Figure 4.36 and Figure 4.37, the VPCC reduces 6%. The DC bus voltage over-shoots are within the design limits and are adjusted by a controller parameter tuning. The over-shoots of the currents and the

DC capacitor voltages in the above two tests give the references for the protection settings of the controller.

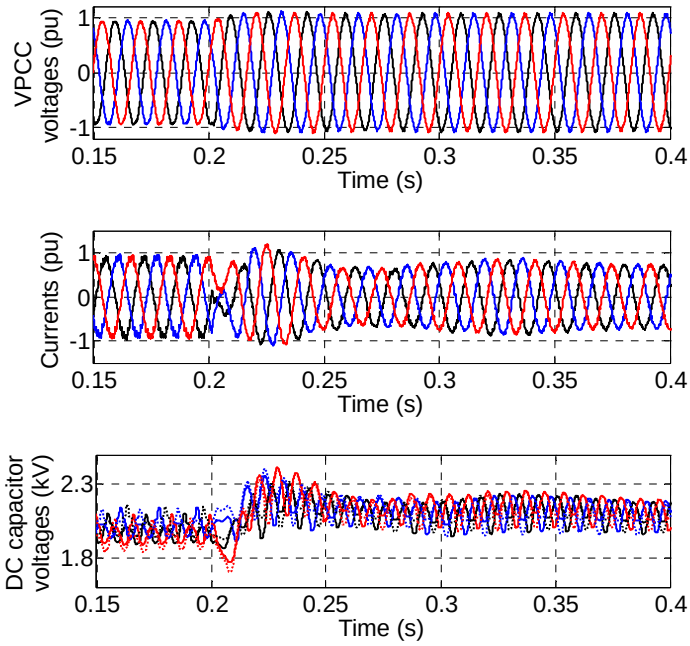


Figure 4.34. STATCOM response to step change in reactive power from 0.8 pu (inductive mode) to -0.8 pu (capacitive mode)

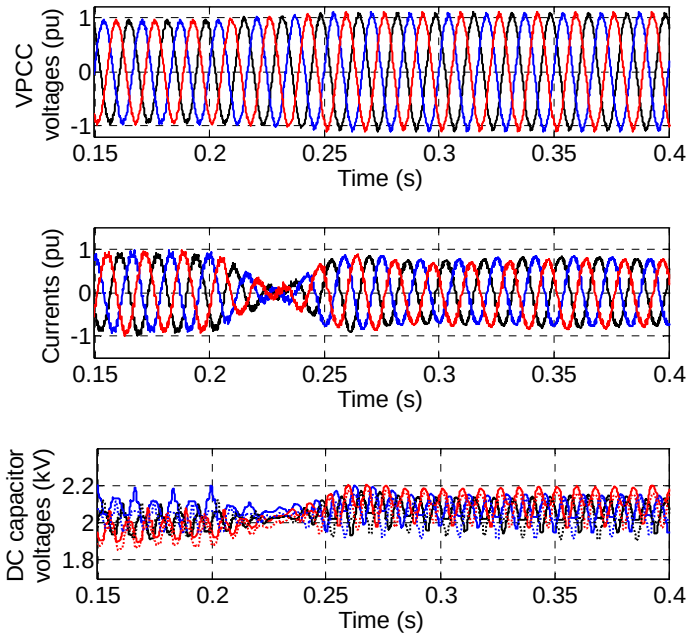


Figure 4.35. STATCOM response to ramp change in reactive power from 0.8 pu (inductive mode) to -0.8 pu (capacitive mode)

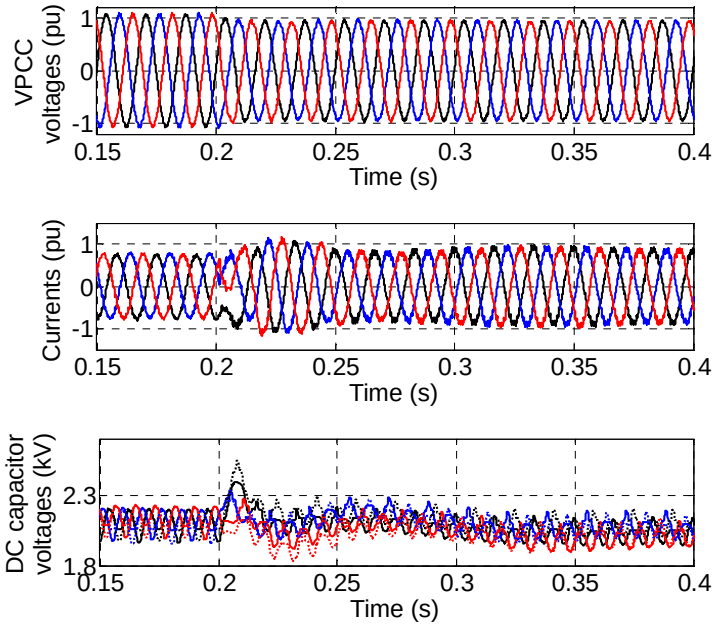


Figure 4.36. STATCOM response to step change in reactive power from -0.8 pu (capacitive mode) to 0.8 pu (inductive mode)

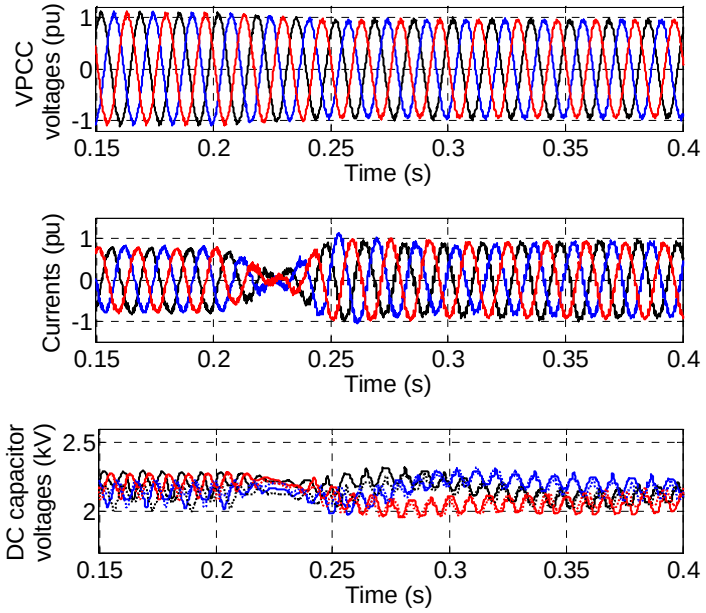


Figure 4.37. STATCOM responses to ramp change in reactive power from -0.8 pu (capacitive mode) to 0.8 pu (inductive mode)

4.7 Summary

A new feedback control strategy for balancing individual DC capacitor voltages is proposed. The design methodology is based on the detailed small-signal model of the STATCOM and the cascade multilevel inverter. The key element of the control strategy is a compensator used to cancel the variation parts in the model. The controller can balance individual DC capacitor voltages when the H-bridges switch with different switching patterns and have parameter variations. The controller works well in all operating regions: the capacitive mode, the inductive mode and the standby mode. The impact of the individual DC voltage controller on the voltage quality is small. The

control strategy has no restriction on the cascade number. Simulation results, experimental results and CHIL test results verify the performance of the controller.

Chapter 5. Enhance ride-through capability of a cascade multilevel inverter for STATCOM

5.1 Introduction

5.1.1 Ride-through capability of the STATCOM

The fault ride through is regarded as one of the main challenges to the design of control and protection of the wind turbines in wind farms [134-139]. Although the definition of fault ride-through varies, the German Transmission and Distribution (E.ON) regulation is likely to set the standard [140]. This stipulates that a wind turbine in a wind farm should remain stable and connected during certain fault conditions [141]. The standard stated in the German Transmission and Distribution Utility (E.ON) regulation is shown in Figure 5.1. This stipulates that a wind turbine should remain stable and connected during the fault while voltage at the coupling point drops to 15% of nominal value (i.e., a drop of 85%) for a period of 150 ms. Only when the grid voltage drops below the curve, is the turbine allowed to disconnect from the grid.

In serving the wind farm, the STATCOM is not allowed to trip before the wind turbine is disconnected. If the STATCOM trips before the wind turbines trip, the bus voltage will drop more due to the absence of the STATCOM, which in turn might trip

the wind turbines. Thus, the STATCOM should follow the same regulation as shown in Figure 5.1.

In the reference [138], the authors state that the Low Voltage Ride Through (LVRT) capability of the wind turbines can be enhanced by the use of a STATCOM. Each voltage dip remaining above solid line must not result in disconnection of the generator. Within the grey area, extra reactive power is demanded from wind power generator to deliver voltage support. However, we think the assumption is that the STATCOM itself has enough ride-through capability first. In this chapter, I have proposed several solutions to enhance the STATCOM's ride through capability for various fault conditions.

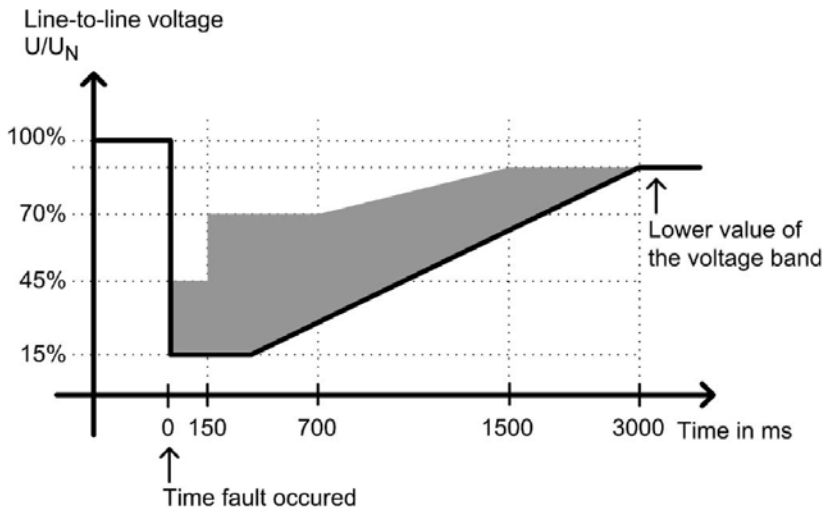


Figure 5.1. E.ON Netz requirements for fault ride-through capability of wind turbines connected to the grid

5.1.2 Effects of power transmission line faults on STATCOM

Power systems have lots of different faults. Here we only consider line faults, which will affect STATCOM directly. Line faults include single-line to ground faults, line-line faults and three-phase faults.

From the perspective of the STATCOM, its performance depends heavily on VPCC. The effect of the line faults on VPCC can be divided into two categories.

The first one is VPCC dip. It is caused by all three kinds of faults.

The second one is VPCC imbalance. It is caused by single-line to ground faults or line-line faults. Strictly speaking, there are two definitions for imbalance based on the symmetrical components. They are: (a) negative sequence voltage imbalance factor V2/V1 and (b) zero sequence voltage imbalance factor = V0/V1 (where V1, V2 and V0 are positive, negative and zero sequence voltages respectively). However, as zero sequence currents cannot flow in three wire systems the zero sequence voltage imbalances are of little practical value. Thus, in this chapter, we only study the VPCC imbalance caused by negative sequence voltage.

5.1.3 Protections of the STATCOM

The protections that might trip the STATCOM include over current protections, over DC capacitor voltage protections, temperature protections, PLL protections, etc.

In this chapter, we focus on two protections that might trip the STATCOM during the faults in most of cases.

The first is over current protection. In the case of the STATCOM for the wind farm, the nominal current is 1.39 kA (rms value). The amplitude of the nominal current is 1.966 kA. The base current is 2.4 kA. So amplitude of the nominal current is 0.82 p. u. The protection setting inside the ETO is 3000A. Thus, the threshold value for the over current protection is 1.25 p. u.

The second is over DC capacitor voltage protection. The DC capacitors in the high-power STATCOM system are very expensive. The cost of DC capacitors is around 30% of total cost. To decrease the investment, the protection margin for the voltage protection is designed to be quite small. The nominal voltage is 2170 V that is 0.52 p. u. The threshold voltage is 2630 V that is 0.63 p. u. Compared with STATCOMs with two-level inverters, three-level inverters and diode-clamped multilevel inverters, the STATCOM with cascade multilevel inverters are easier to be tripped by the over DC capacitor voltage protection. This is because the cascade multilevel inverters have multiple DC capacitors and imbalances of DC capacitor voltages occur without careful control.

5.1.4 Operation mode of STATCOM during the faults

During the faults, the VPCC will drop in balanced faults or imbalanced faults. The STATCOM should function in the capacitive mode to inject as much as possible

reactive power for boosting bus voltages. Therefore, in this chapter, we only study the performance of the STATCOM in the capacitive mode during faults.

5.1.5 Mild faults and severe faults

In this chapter, a mild fault means that the VPCC has fewer dips or fewer imbalance conditions (fewer negative components). The severe faults mean that the VPCC has severe dips or imbalances. I am proposing the solutions for enhancing ride-through capabilities of the STATCOM for both mild faults and severe faults. The solutions for mild faults and severe faults are slightly different as explained below. This is the reason why we distinguish the mild faults and severe faults. The criterion for partitioning of mild faults and severe faults are not covered in this chapter. This criterion depends heavily on specific applications and deployments.

5.2 Solutions for mild faults

5.2.1 Mild VPCC dip

Mild VPCC dip without imbalance is mainly caused by mild three-phase faults. The simulation in Figure 5.2 shows the performance of the STATCOM. The first sub figure is VPCC (line-line voltages). The second sub figure is STATCOM currents (phase currents). The third one is the A-phase inverter output voltage (five-level waveform). The fourth one is the two DC capacitor voltages in the A phase. The fifth

and sixth sub diagrams are DC capacitors voltages in the B phase and C phase, respectively.

The STATCOM runs in a nominal rating (Iq reference is -1 p. u., capacitive mode). From 0.4 S to 0.6 S, VPCC drops to 70% of the nominal value. As shown in the simulation, the maximum amplitude of the current is less than 1.25 p. u. and the maximum DC capacitor voltage is less than 0.63 p. u. Thus, the STATCOM can ride through this mild VPCC dip.

A feed-forward loop has been added into the d-channel current loop, as shown in Figure 5.3. This is to suppress the over-shoot currents and over-shoot DC capacitor voltages during the transient time. This is the common method in the STATCOM control.

Summary: the STATCOM can ride through mild VPCC dip without additional control.

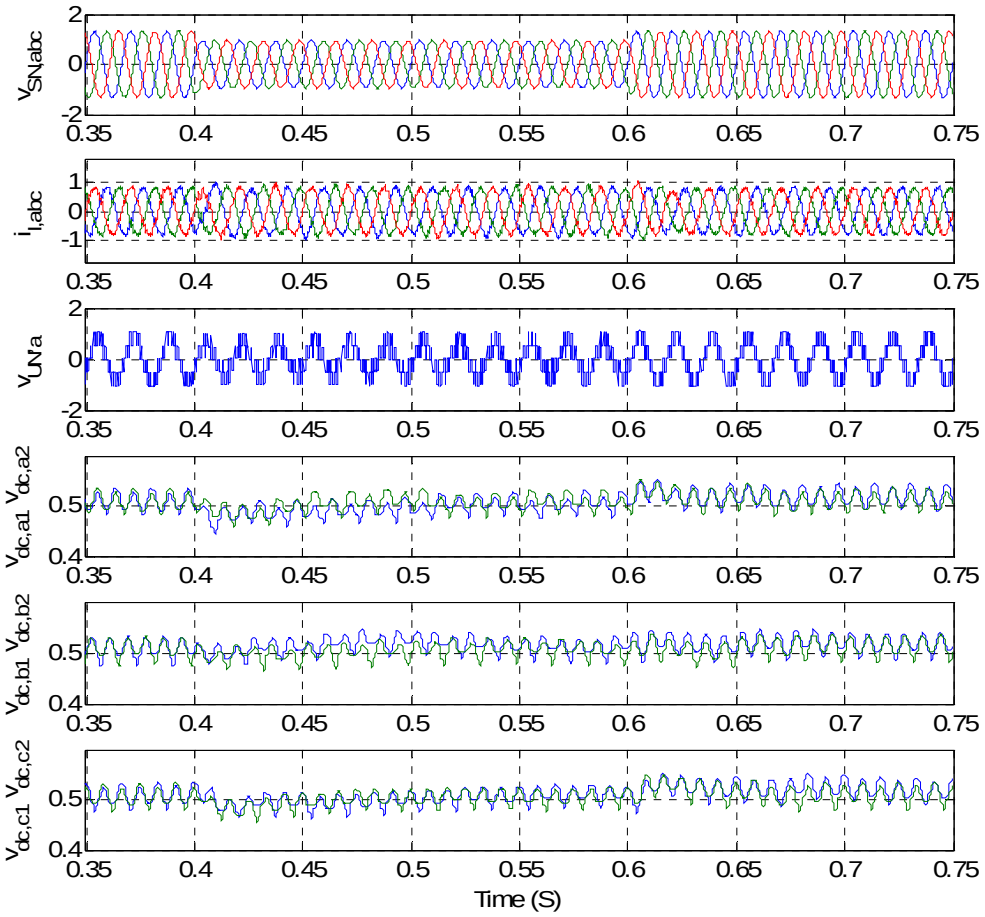


Figure 5.2. Simulation results when VPCC drops to 70% of nominal value

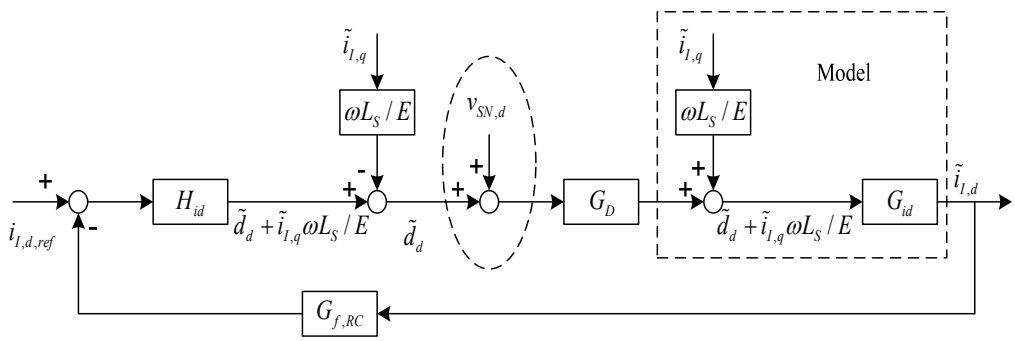


Figure 5.3. D-channel current loop with feed-forward loop

5.2.2 Mild VPCC imbalance

5.2.2.1 Definition of VPCC imbalance

VPCC imbalance comes mainly from system faults and load imbalance [11, 142-144]. When the STATCOM is deployed near the wind farm, we only focus on the VPCC imbalance caused by system faults (which are asymmetric) such as single phase line to ground faults or line-to-line faults.

In a balanced sinusoidal supply system the three line-neutral voltages are equal in magnitude and are phase displaced from each other by 120 degrees. Any differences that exist in the three voltage magnitude and/or a shift in the phase separation from 120 degrees is said to give rise to an imbalanced voltage.

The definition of voltage imbalance originates from the theory of Symmetrical Components which mathematically breaks down an imbalanced system into three balanced systems. These are called positive sequence, negative sequence and zero

sequence systems. For a perfectly balanced system both negative and zero sequence systems would be absent.

Strictly speaking, there are two definitions for imbalance based on the symmetrical components. They are: (a) negative sequence voltage imbalance factor = V_2/V_1 and (b) zero sequence voltage imbalance factor = V_0/V_1 (where V_1, V_2 and V_0 are positive, negative and zero sequence voltages respectively). However, as zero sequence currents cannot flow in three wire systems the zero sequence voltage imbalance is of little practical value.

5.2.2.2 Problems caused by VPCC imbalance

We found out the problems of the STATCOM during VPCC's imbalance in terms of the CHIL test results. One outcome was current imbalance, and the other was the imbalance of DC capacitor voltages. A simulation has also been done to verify these findings. Figure 5.4 from the CHIL test results clearly shows the imbalance issues of currents and DC capacitor voltages due to VPCC imbalance. The "current imbalance" and "VPCC imbalance" mean the value of their negative sequence components (p. u. value), respectively. The "DC voltage imbalance" means the difference of the maximum DC capacitor voltage and the minimum DC capacitor voltage (p. u. value).

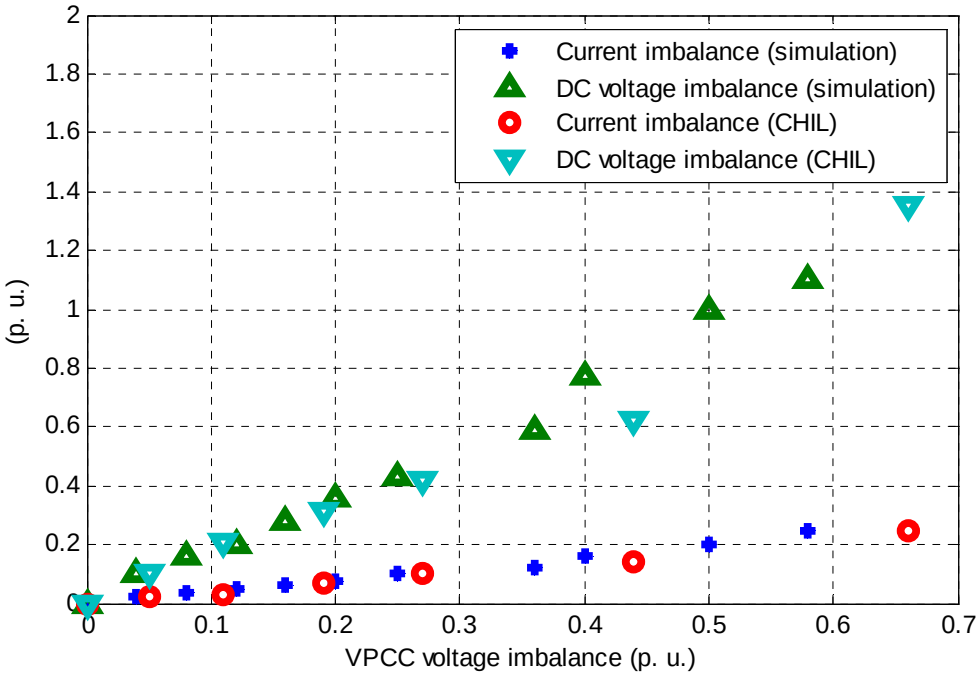


Figure 5.4. Behavior of the STATCOM during conditions of voltage imbalance

One interesting phenomena has been observed from both the CHIL tests and the off-line simulations. The imbalance of currents are much less severe than that we expected when the VPCC has large imbalances. We assumed that the output voltages of the inverter are balanced. Therefore, no negative sequence components exist in the output voltages of the inverter. The negative sequence voltages across the interface inductors are equal to the negative sequence components of VPCC. So, we expected that the small imbalance voltages of VPCC will cause large unblanced currents.

However, the assumption that the output voltages of the inverter are balance is not true. Figure 5.7 shows the simulation waveforms when VPCC has 20% negative

sequence component when Iq reference is -1 p. u. (capacitive mode, full rating). From 0.4 S to 0.6 S, the VPCC is imbalanced. As shown in sub-figure 1, the amplitude of A-phase VPCC (blue) is largest. Also, the amplitude of A-phase current is not dramatically different than other currents. The reason is that the A-phase DC capacitor voltages also increases automatically, as shown in sub-figure 4. Thus, the A-phase inverter output voltage also increases along with the increase of A-phase VPCC. Note that two DC capacitor voltages in the A-phase are always equal due to the control loops for individual DC capacitor voltages. However, the DC capacitor voltages in different phases are imbalanced as shown in sub-figure 4, 5 and 6.

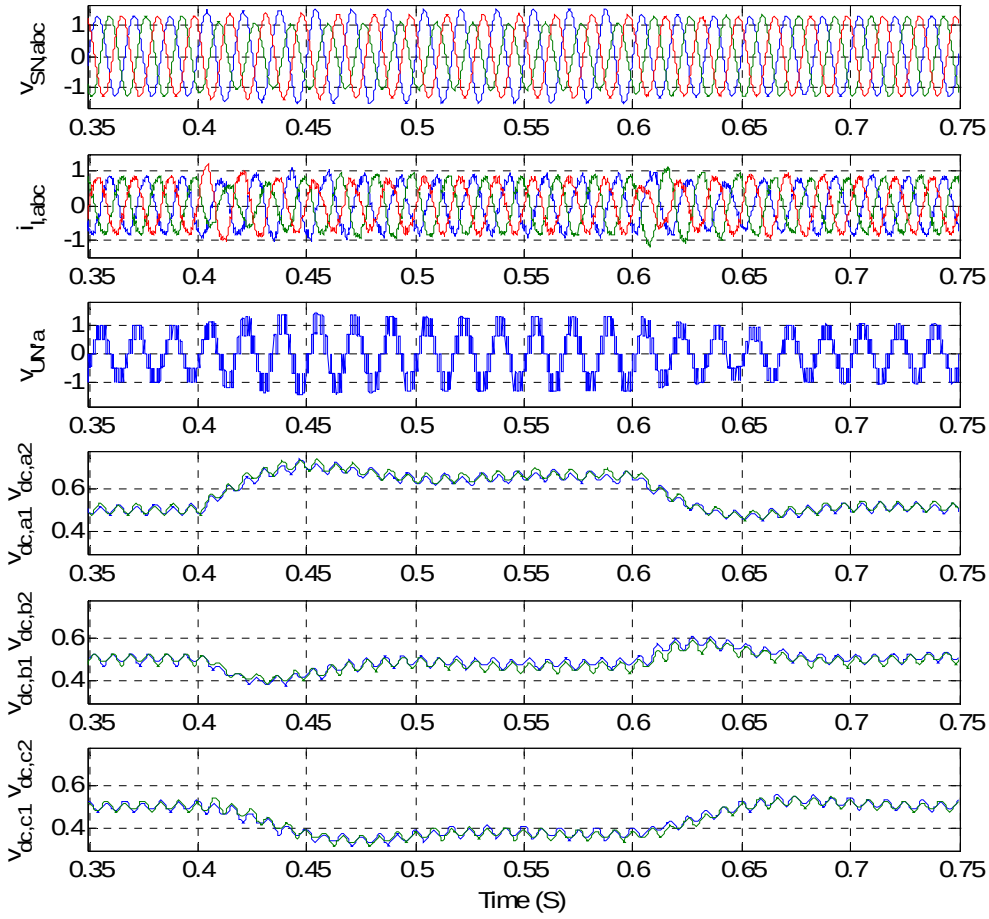


Figure 5.5. Simulation results when VPCC has 20% negative components

The main problem identified here is that the maximum DC capacitor voltage is larger than 0.63 p. u., which will trip over DC voltage protections.

5.2.2.3 Previous methods addressed VPCC imbalance

Most previous methods [11, 142-147] for addressing the VPCC imbalance focus on using large imbalanced AC currents to reduce the negative components of VPCC. In

other words, the STATCOM tried to eliminate the VPCC imbalance. However, the assumption here is that the STATCOM has enough over current margin. This is because the required currents for completely or partially eliminating the VPCC imbalance might be as high as two or three time larger than nominal currents. If the faults last for a long time, the STATCOM must run with the huge currents for a long time.

In our design of the STATCOM for the wind farm, the over current margin is very small. The maximum instantaneous current is 3000 A (1.25 p. u.). The maximum current is such that the STATCOM can run for a little bit longer time (such as 1 second). This is around 1688 A, 120% of nominal current, due to thermal limitation. Thus, the over current margin is pretty small. Therefore, the control goal cannot be expected to eliminate the VPCC imbalance during faults.

In the case of a cascade multilevel inverter based STATCOM, if we try to use the STATCOM to inject large imbalance currents to balance VPCC, the DC capacitor voltages will become extremely imbalanced and the maximum DC capacitor voltage will be much larger than nominal values. However, in our design of the STATCOM, the over DC voltage margin is very small (21%).

In terms of small over current margins and over DC voltage margins, the STATCOM cannot eliminate the VPCC imbalance during faults. The control goal here

is, under VPCC imbalance, that the STATCOM will keep running and inject reactive currents as much as possible.

5.2.2.4 Solution for VPCC imbalance

In the control presented in last chapter, the output voltages of the inverter are balanced. In other words, the inverter output voltages only have positive sequence components.

The solution for VPCC imbalance is that the inverter output voltages have both positive sequence components and negative sequence components. The positive sequence components are still used to generate reactive current. The negative sequence components of inverter output voltage will be the same as that of VPCC. Thus, theoretically, the negative sequence currents will be zero, which will help to reduce both steady maximum currents and transient currents. Another advantage is that the DC capacitor voltages in three phases are still balanced in this solution.

The positive sequence reference voltage of the inverter output is (V_+, θ_{a+}). This comes from the feedback control block. The negative sequence reference voltage of the inverter output is (V_-, θ_{a-}), which comes from measured VPCC.

$$\begin{aligned} v_{a+} &= V_+ \sin(\omega t + \theta_{a+}) & v_{a-} &= V_+ \sin(\omega t + \theta_{a-}) \\ v_{b+} &= V_+ \sin(\omega t + \theta_{a+} - 2\pi/3) & v_{b-} &= V_+ \sin(\omega t + \theta_{a-} + 2\pi/3) \\ v_{c+} &= V_+ \sin(\omega t + \theta_{a+} + 2\pi/3) & v_{c-} &= V_+ \sin(\omega t + \theta_{a-} - 2\pi/3) \end{aligned} \quad (5.1)$$

For A-phase inverter output voltage with the positive and negative components shown above, the real and imaginative parts are expressed as

$$\begin{aligned} \mathrm{Re}_a &= V_+ \cos\theta_{a+} + V_- \cos\theta_{a-} \\ \mathrm{Im}_a &= V_+ \sin\theta_{a+} + V_- \sin\theta_{a-} \end{aligned} \tag{5.2}$$

The B-phase and C-phase inverter voltage with the positive and negative components are shown as

$$\begin{aligned} \mathrm{Re}_b &= V_+ \cos(\theta_{a+} - 2\pi/3) + V_- \cos(\theta_{a-} + 2\pi/3) \\ \mathrm{Im}_b &= V_+ \sin(\theta_{a+} - 2\pi/3) + V_- \sin(\theta_{a-} + 2\pi/3) \end{aligned} \tag{5.3}$$

$$\begin{aligned} \mathrm{Re}_c &= V_+ \cos(\theta_{a+} + 2\pi/3) + V_- \cos(\theta_{a-} - 2\pi/3) \\ \mathrm{Im}_c &= V_+ \sin(\theta_{a+} + 2\pi/3) + V_- \sin(\theta_{a-} - 2\pi/3) \end{aligned} \tag{5.4}$$

In Figure 5.6, the positive sequence reference voltage is obtained from the control loop. The negative sequence reference voltage is the same as the negative sequence component of VPCC. The modulation indexes (*m*) and angle shifts (*Ang*) are different for different phases.

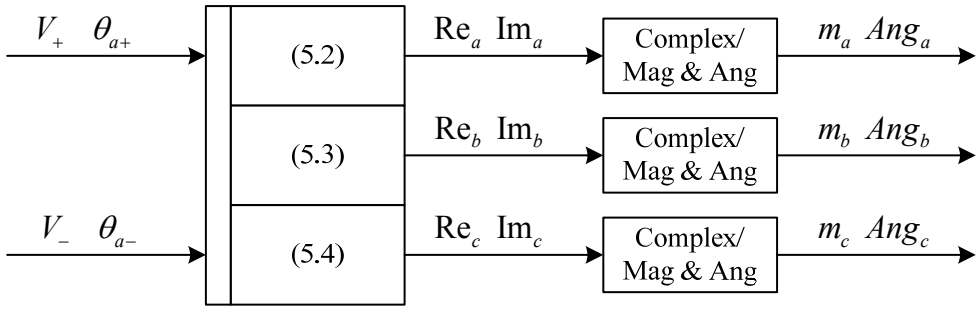


Figure 5.6. Control block with the negative components

Figure 5.7 shows the simulation results with the proposed methods. The STATCOM runs in full rating of the capacitive mode. From 0.4 to 0.6 S, the VPCC has 20% negative sequence components. With the proposed method, the controller has forced the inverter to generate additional negative sequence voltages that are equal to the negative component of the VPCC. As shown in Figure 5.7, the deviation of DC capacitor voltages is much less than that in Figure 5.5. The maximum DC capacitor voltage in Figure 5.7 is 0.6 p. u., while that in Figure 5.5 is 0.76 p. u. The difference between maximum DC voltage and minimum DC voltage in Figure 5.7 is 0.14 p. u., while that in Figure 5.5 is 0.45 p. u. Therefore, the proposed method reduces imbalance of DC capacitor voltages and reduces the maximum DC capacitor voltage.

Small imbalance of DC capacitor voltage cause limited imbalanced currents, as shown in Figure 5.7. The maximum current is less than 1.25 p. u., thus it will not trip over-current protection.

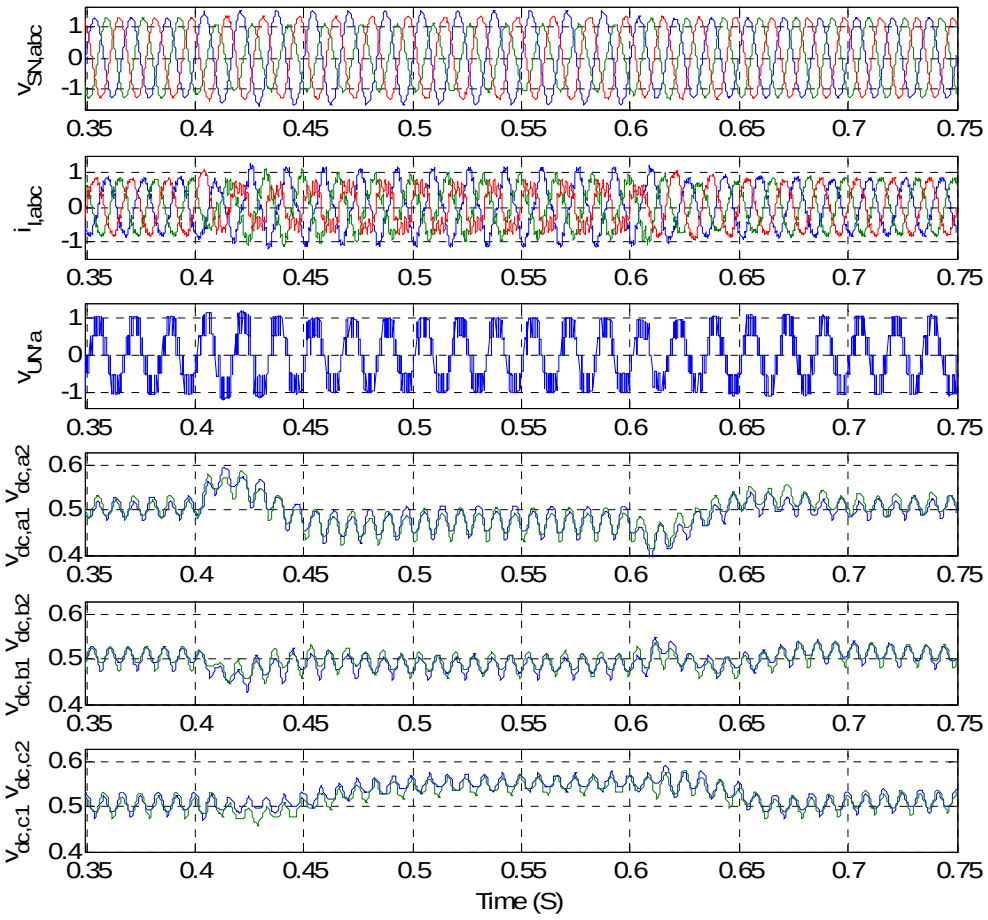


Figure 5.7. Simulation results with the proposed solution when VPCC has 20% negative components

5.2.3 Mild VPCC imbalance and dip

In practice, most VPCC imbalance comes with voltage dip. This is caused by asymmetric faults. If the faults are not severe or the locations of faults are far away from VPCC location, the VPCC dip and imbalance is mild. Here, we use simulation to

verify that the above proposed method can enhance the STATCOM's ride-through capability when the VPCC has mild voltage dip and imbalance.

In simulation as shown in Figure 5.8 and Figure 5.9, the VPCC drops 30% and has 20% negative sequence components from 0.4 S to 0.6 S. The STATCOM runs in full rating of the capacitive mode.

In simulation as shown in Figure 5.8, we don't apply the proposed method. The maximum DC capacitor voltage is as high as 0.79 p. u., which will trip the over DC voltage protection. The difference between maximum DC voltage and minimum DC voltage is 0.46 p. u.

In the simulation as shown in Figure 5.9, we apply the proposed method. The maximum DC capacitor voltage is 0.55 p. u. The difference between maximum DC voltage and minimum DC voltage is only 0.12 p. u. Also, the maximum current is less than 1.25 p. u.

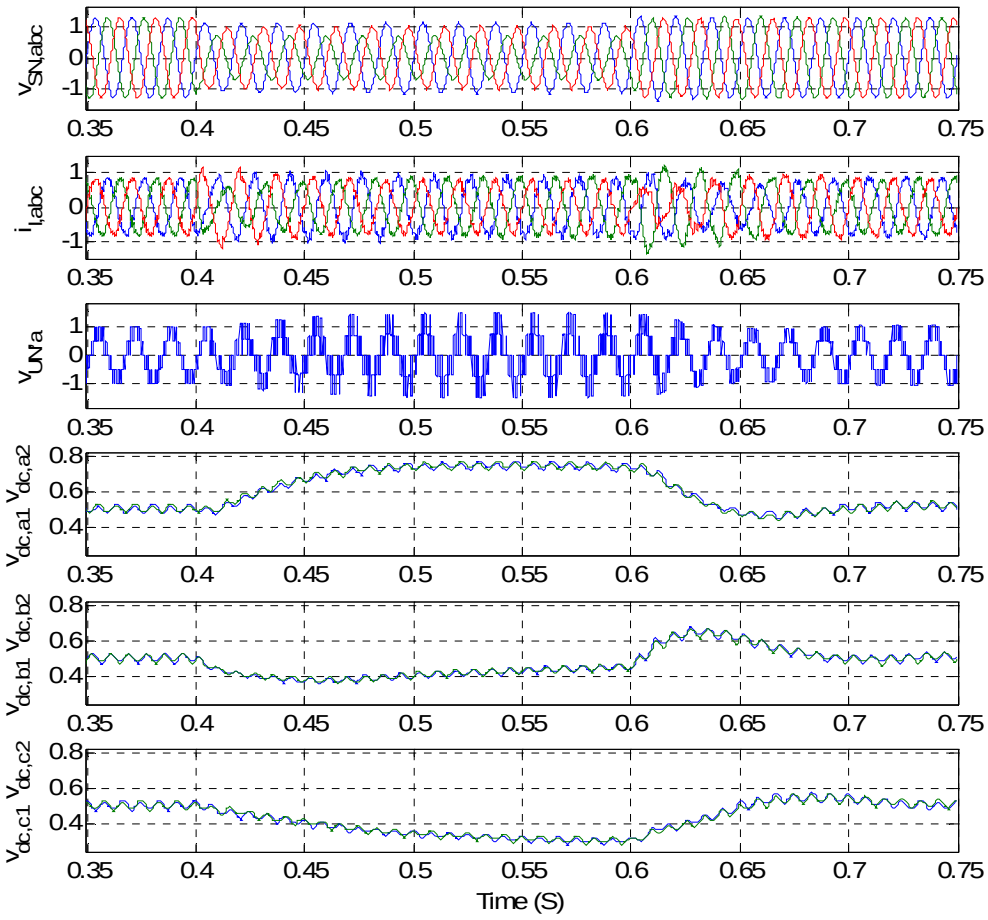


Figure 5.8. Simulation results without the proposed solution when VPCC drops 30% and has 20% negative sequence

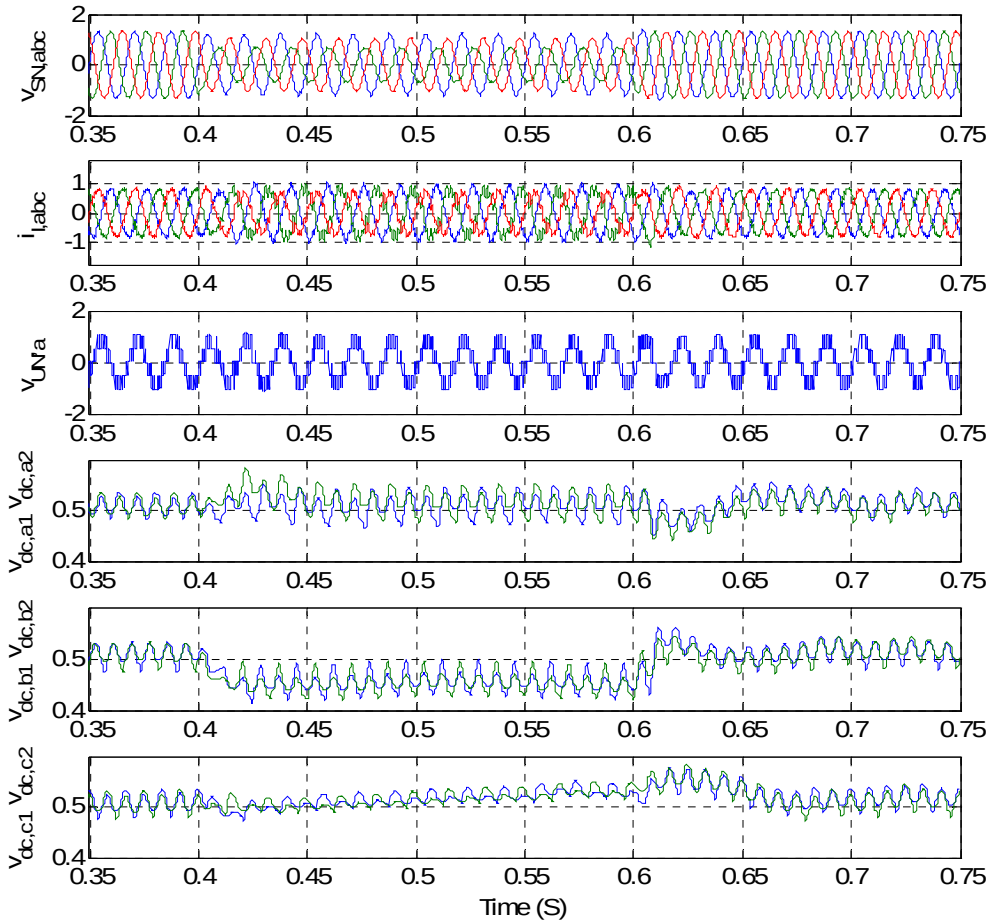


Figure 5.9. Simulation results with the proposed solution when VPCC drops 30% and has 20% negative sequence components

5.2.4 Summary for mild faults

Mild faults here mean that faults are mild or that the location of faults is far away from VPCC point. Therefore, the VPCC has a small dip or/and a little imbalance.

Based on control strategies presented in previous chapters, the STATCOM can ride through mild VPCC dips.

However, to ride through mild VPCC imbalance, the STATCOM control strategy needs be improved. Previously in this section, a new control strategy was presented. The inverter will generate voltages with negative sequence components that are equal to the negative sequence components of the VPCC. The simulation has verified that the STATCOM can ride through mild VPCC imbalance with the proposed solution. Moreover, the simulation has also verified that the STATCOM can ride through mild VPCC dips and imbalance with the proposed solution.

5.3 Solutions for severe faults

A severe fault means that the fault is severe and the fault location is close to the STATCOM. For symmetric faults (three-phase faults), the three-phase VPCC could drop 85%. For asymmetric faults, a phase voltage might drop 85% and at the same time the three-phase voltages could have severe imbalance.

The ride-through capability for severe VPCC dips or/and imbalance is a challenge for the design of the STATCOM controller. The control strategies proposed above for mild faults are not enough to help the STATCOM ride through severe VPCC dips or/and imbalance.

Additional control strategies will be presented to make sure the STATCOM can ride through severe VPCC dips or/and imbalance.

5.3.1 Severe VPCC dip

In simulation as shown in Figure 5.10, VPCC drops 85% from 0.4 S to 0.6 S. This is a severe VPCC dip. Two problems have been identified in Figure 5.10. 1) The currents exceed 1.25 p. u. during transients. 2) The maximum DC capacitor voltage exceeds 0.63 p. u. These two conditions will trip over current protections and over voltage protections.

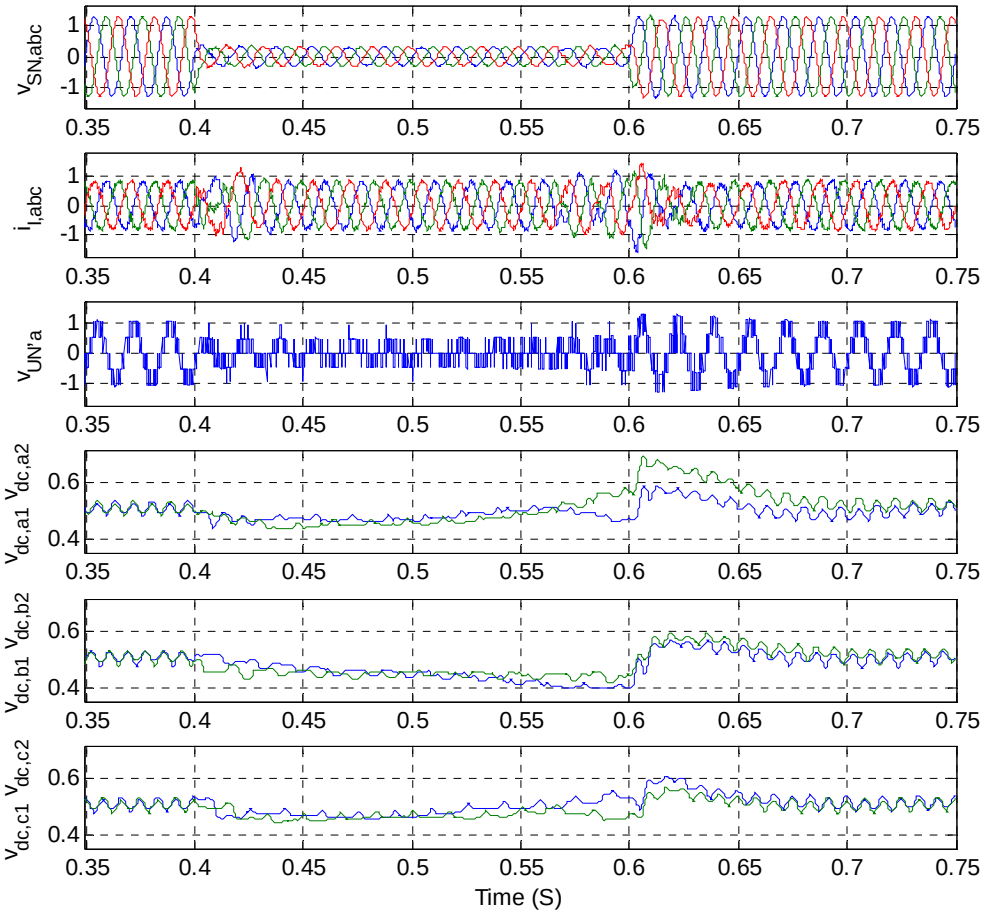


Figure 5.10. Simulation results when VPCC drops 85%

A good solution for ride through severe voltage dips is described below.

- Limit Iq reference as shown in Figure 4.8 to a smaller value during the severe dips. In other words, degrade the STATCOM currents. The purpose is to decrease maximum current to avoid tripping over-current protections.
- Decrease the reference of DC capacitor voltages as shown in Figure 4.9 during the severe dips. The purpose is to decrease maximum DC capacitor voltage to avoid tripping over-voltage protections.

In simulation as shown in Figure 5.12, VPCC drop 85% from 0.4 S to 0.6 S. The STATCOM runs in full rating of the capacitive mode. The STATCOM can ride through this severe dip by decreasing references of Iq and DC capacitor voltage. Suppose detection of faults need a cycle time. Then, the Iq reference changes from 1 p. u. to 0.3 p. u. at 0.416 S, and it changes from 0.3 p. u. to 1 p. u. at 0.616 S. The reference of DC capacitor voltage changes from 0.52 p. u. to 0.36 p. u. at 0.416 S, and then it changes from 0.36 p. u. to 0.52 p. u. at 0.616 S.

With the proposed solution (as shown in Figure 5.12), the maximum DC capacitor voltage is less than 0.55 p. u., and the maximum current is less than 1.02 p. u. Therefore, the STATCOM can ride through this severe voltage dip with this solution.

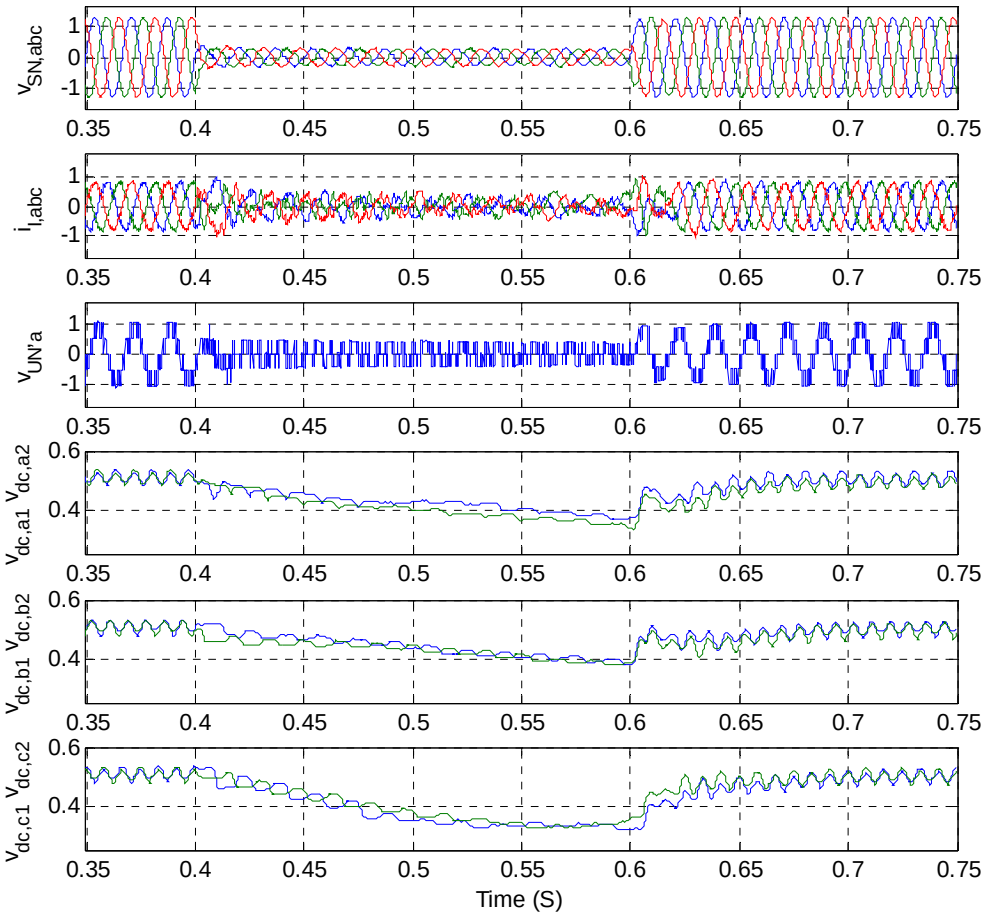


Figure 5.11. Simulation results with improved solution when VPCC drops 85%.

5.3.2 Severe VPCC imbalance and dip

Severe VPCC imbalances are generally caused by severe single line to ground faults or line-to-line faults near the STATCOM. Thus, VPCC severe imbalance always comes together with VPCC dips.

In the simulation in Figure 5.12, the VPCC drops 40% and has 40% negative sequence components from 0.4 S to 0.6 S. The STATCOM runs at full rating of capacitive mode. As shown in Figure 5.12, VPCC C-phase voltage (green line) almost drops 80%, while A-phase (blue line) voltage has no dip. In simulation (shown in Figure 5.12), we don't add additional negative sequence voltage on the inverter output voltage and we don't reduce the references of Iq and DC capacitor voltage. It can be seen that the DC capacitor voltages are extremely imbalanced and the maximum current exceed 1.25 p. u., the threshold current of the over-current protection.

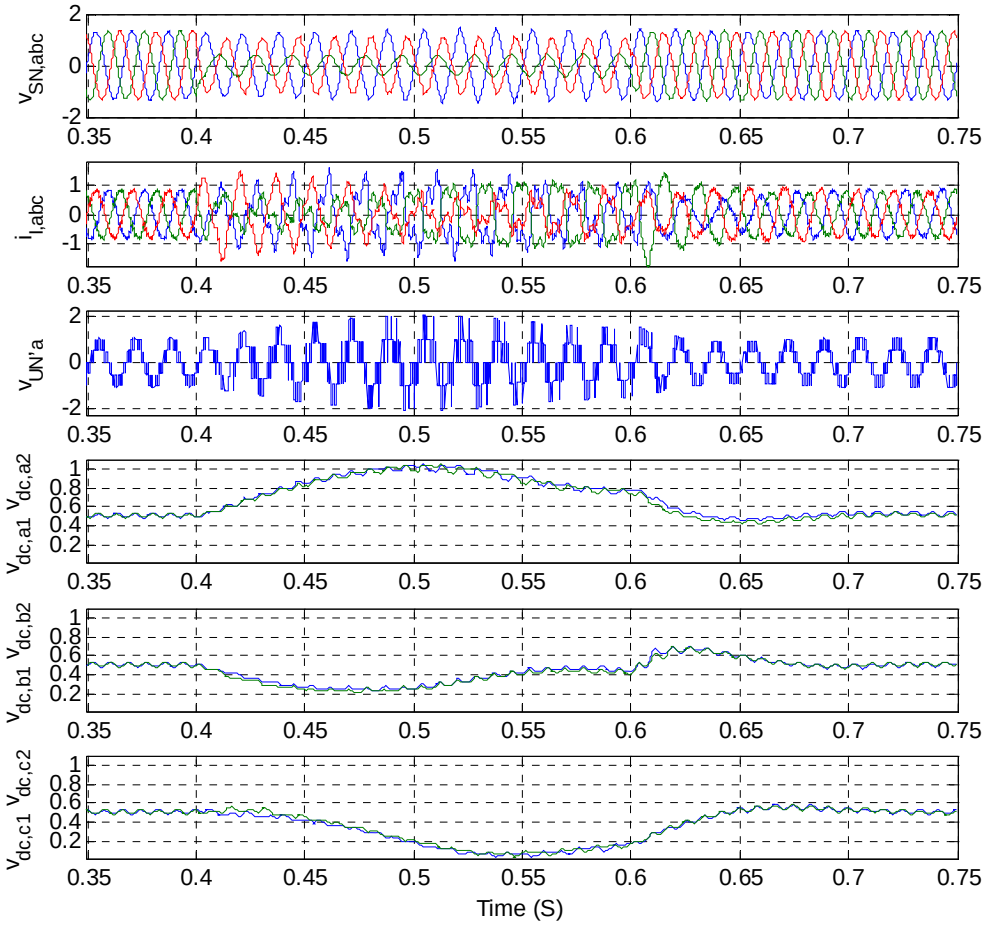


Figure 5.12. Simulation results when VPCC drop 40% and has 40% negative sequence components

The case in the simulation shown in Figure 5.13 is almost the same as that in Figure 5.12. The only difference is that we use the method proposed in the last section when the inverter generates additional negative sequence voltage that is equal to the VPCC negative sequence component. The maximum DC capacitor voltage reduces

significantly and is less than 0.59 p. u. This will not trip over DC protections. However, the maximum current still exceed 1.25 p. u., which will still trip over-current protection.

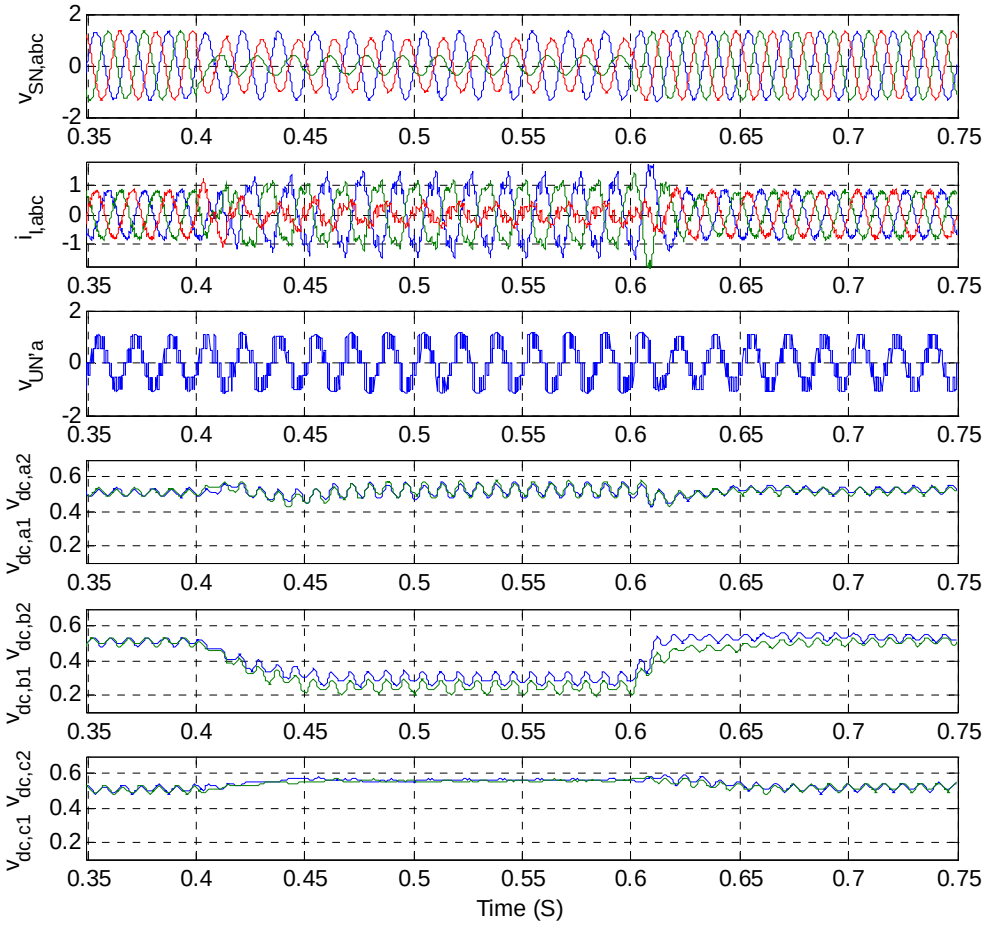


Figure 5.13. Simulation results with the method of adding negative sequence components on the inverter voltage when VPCC drop 40% and has 40% negative sequence components

The case in simulation (shown in Figure 5.14) is the almost same as that in Figure 5.13. The difference is that we do not use only the method proposed in the last section

when the inverter will generate additional negative sequence voltage and reduce the references of Iq and DC capacitor voltages. The Iq reference changes from 1 p. u. to 0.3 p. u. at 0.416 S, and then it changes from 0.3 p. u. to 1 p. u. at 0.616 S. The reference of the DC capacitor voltage changes from 0.52 p. u. to 0.36 p. u. at 0.416 S, and then it changes from 0.36 p. u. to 0.52 p. u. at 0.616 S.

The maximum DC capacitor voltage is less than 0.57 p. u. This will not trip over the DC protections. The maximum current is less than 1.05 p. u., and it will not trip over-current protection. Thus, the STATCOM can ride through this severe VPCC imbalance.

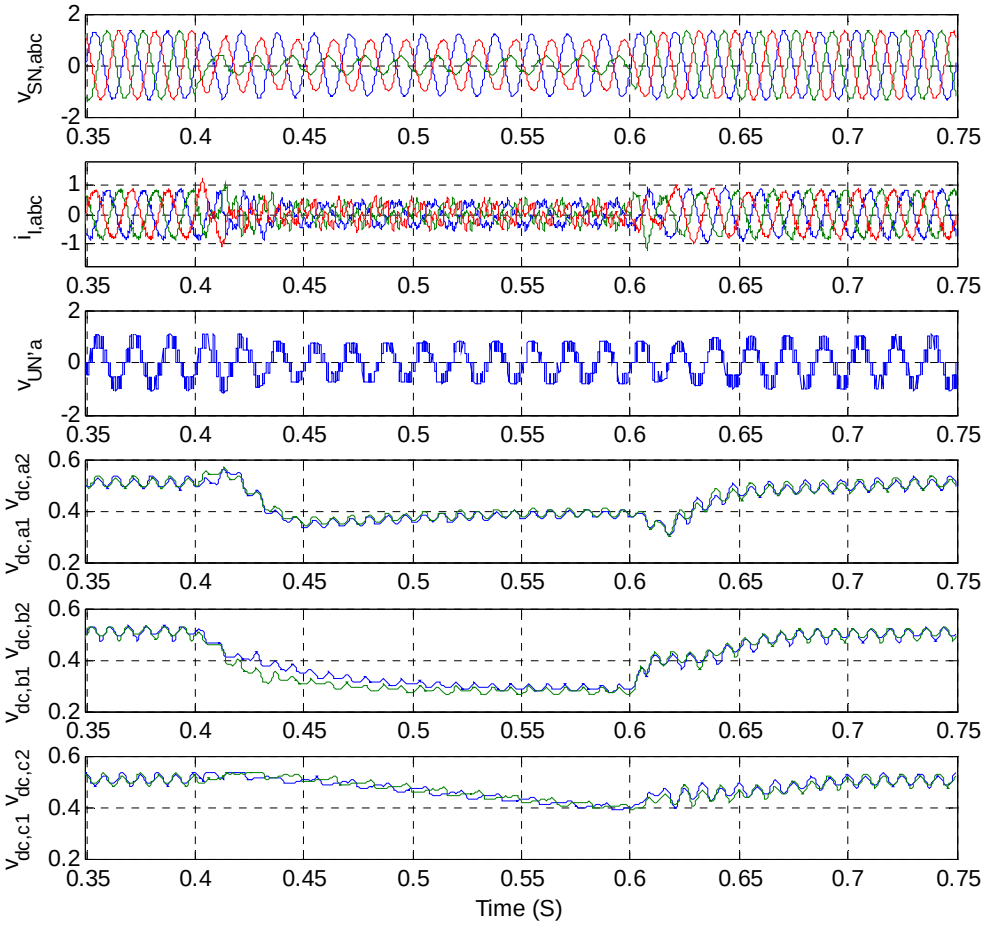


Figure 5.14. Simulation results with the proposed solution when VPCC drop 40% and has 40% negative sequence components

5.4 Summary

In this chapter, solutions for enhancing ride-through capability of the STATCOM during faults conditions have been proposed. The mild faults occur when the VPCC has a smaller dip or less imbalance (less negative components), while the severe faults

occur when the VPCC has severe dip or imbalance. The solutions for these VPCC situations are shown in Table 5.1. If the VPCC has imbalance, the inverter may generate additional negative sequence voltage that is equal to VPCC negative sequence voltage. This limits DC capacitor voltages. If VPCC has severe dips and/or imbalance, the reference of Iq and DC capacitor voltages needs to be reduced in order to limit over-shoot current and maximum DC capacitor voltages. Simulation results show that the STATCOM can ride through faults with the proposed solution as shown in Table 5.1. The criterion for partition of mild dip/imbalance and severe dip/imbalance faults are not covered in this chapter. Actually, this criterion depends heavily on specific applications and deployments of the STATCOM.

Table 5.1. Summary of proposed solutions to enhance ride through capability during different faults

VPCC	**Controller in last chapter**	**Inverter generates additional negative sequence voltage**	**Reduce references of Iq and DC capacitor voltage**
Mild dip	*		
Mild imbalance	*	*	
Mild imbalance + dip	*	*	
Severe dip	*		*
Severe imbalance + dip	*	*	*

Chapter 6. Conclusion

New series of minimal THD modulation for multilevel inverter have been presented. The first minimal THD modulation is the real-time algorithm to calculate optimal values of switching angles for given DC voltages and modulation index. It is suitable for a case where the DC voltages cannot be controlled and might have fluctuations. With the proposed algorithm, the voltage THD is minimized, which is proven by the rigorous mathematical derivation. A new expression of THD is presented to simplify the derivation significantly. The computational complexity is analyzed to show that the computing time is small enough that common microprocessors or a DSP can handle it easily in real-time. Thus, the minimization of the voltage THD and the real-time calculating ability make the proposed algorithm attractive in multilevel inverters with unequal or varying voltage steps. Experimental results verify the performance of the algorithm.

The second minimal THD modulation is the algorithm to calculate optimal values of DC voltages and switching angles for a given modulation index. It is suitable in the case where DC voltages can be controlled. Compared with the first one, we can get even lower THD with the second modulation by controlling the DC voltages and switching angles. The THD with the optimal DC voltages is less than the minimum THD with equal step voltages, especially for smaller modulation indexes.

The third minimal THD modulation is the algorithm to calculate optimal values of DC voltages, switching angles and modulation index. This gives an optimal design in terms of THD minimization for a multilevel inverter with certain levels. A table has been presented that shows optimal values of modulation index, DC voltages and switching angles for multilevel inverter s with different voltage levels. This provides instructive information for engineers in selecting appropriate DC voltages and a modulation index to achieve better voltage quality.

Another new optimal combination modulation strategy is proposed for the 10 MVA 5-leve cascade multilevel inverter based STATCOM system. There are two optimizations in this strategy. The first one is the optimization of switching angles for each H-bridge to eliminate the 5th, 7th, 11th, and 13th harmonics. Even when a cell is bypassed due to faults, lower order harmonics still don't exist. The second one is the optimization of the combination of switching angles of two H-bridges for reducing the higher order harmonics to meet the IEEE 519 standard for a specified application. The calculation results and simulation results show (with proposed optimal combination modulation) that the current harmonics and TDD can meet the IEEE 519 standard when the five-level cascade multilevel inverter based 10 MVAr STATCOM is connected to a 64 MW system.

A new feedback control strategy for balancing individual DC capacitor voltages is proposed. The design methodology is based on the detailed small-signal model of the

STATCOM and the cascade multilevel inverter. The key part of the control strategy is a compensator to cancel the variable parts in the model. The controller can balance individual DC capacitor voltages when H-bridges switch with different switching patterns and have parameter variations. The controller works well in all operating regions (the capacitive mode, the inductive mode and the standby mode). The impact of the individual DC voltage controller on the voltage quality is small. The control strategy has no restriction on the cascade number. Simulation results, experimental results and CHIL test results verify the performance of the controller.

The solutions for enhancing ride-through capability of the STATCOM during fault conditions have been presented. The mild faults occur when the VPCC has a smaller dip or a less imbalance (less negative components), while the severe faults occur when the VPCC has a severe dip or/and imbalance. If the VPCC has imbalance, the inverter may generate additional negative sequence voltage that is equal to VPCC negative sequence component, in order to limit DC capacitor voltages. If the VPCC has a severe dip and/or imbalance, the reference of Iq and DC capacitor voltages need to be reduced, in order to limit over-shoot current and maximum DC capacitor voltages. Simulation results show that the STATCOM can ride through faults with the proposed solutions.

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