Abstract

Vichienchom, Kasin A Multi-Gigabit CMOS Transceiver with 2x Oversampling Linear Phase Detector (Under the direction of Professor Wentai Liu).

This dissertation presents the design of a high-speed CMOS transceiver for serial digital data. The design is based on a parallel architecture data recovery circuit. It uses multiple clock phases from a multi-phase phase-locked loop (MPLL) operating at low frequency to sample high frequency input data in a time-interleaved manner. This results in the reduction of the speed requirement for the transceiver. The new technique of time-interleaved sampling is realized by placing the analog and digital samplers alternately to sample the input data at a sampling rate of two times the data rate (2x). This hybrid parallel sampling scheme provides the input phase error to the multi-phase PLL and simultaneously recovers and deserializes the input data. The data phase detection generates the loop error signal that is proportional to the input phase error, therefore allowing the PLL to have a proportional loop control. This results in improvement of the loop stability, the output jitter, and the bit error rate over the conventional all-digital 2x oversampling, referred to as the bang-bang type phase detection. In addition, to investigate its operation closely, the model and analysis of the multi-phase PLL based on the discrete-time linear system has been developed. This model takes into account the sampling nature of the loop, which provides greater insight into the system behavior and an understanding of system constraints. The analysis shows that when the PLL loop bandwidth is much smaller than the input frequency, the system response can be approximated by the conventional continuous-time model and thus the number of phase detectors employed can be reduced. The model predicts the stability limit of the multi-phase PLL as a function of input frequency, loop bandwidth, and the number of phase detectors. In addition, the phase noise due to the bang-bang type phase detector in PLL-based clock recovery circuits has been analyzed using this model.

The design was implemented in TSMC 0.35μm CMOS. The prototype was tested with the input data rate between 1Gbps to 3.3Gbps. The introduction of numerous parasitic components in the packaging of the prototype complicated the measurement and validation
of the proposed technique experimentally. The failure analysis identifies the causes as a severe noise condition in the supply rails and a resonance phenomenon of the power distribution network. The severe noise condition is due to the large parasitic inductance of the package and insufficient on-chip decoupling capacitance. Additionally, the condition was exacerbated by a change of the substrate type in the fabrication from a non-epitaxial to an epitaxial wafer. This not only defeated the noise preventive design strategy but also introduced more noise into the circuit. The large packaging parasitic inductance and the large on-chip capacitance have formed a resonance circuit that resonates with the input clock frequency. The analysis concludes that this capacitance possibly originates from either the loop filter capacitor or the capacitance between the bulk and the package cavity. Despite these manufacturing complications, transistor level simulations indicate not only the viability of this technique but also shows that the proposed implementation can work up to 3.2Gbps.
A Multi-gigabit CMOS Transceiver with 2x Oversampling Linear Phase Detector

by

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Biography

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Chapter 1

Introduction

1.1 Background and Motivation

As the world enters the age of information, there are increasing demands in communication technology. The advancements in computation technology result in high performance processors that require a high speed link to communicate between units and their peripherals. The communication networks such as Ethernet, SONET/SDH, ATM require higher bandwidth and greater efficiency to support its growing traffic. These propel the pursuit of a transceiver in the gigabit range.

CMOS technology has a primary advantage over traditional technologies such as GaAs, Si bipolar in its lower cost and higher integration. Despite its reduced maximum operation frequency of its devices, CMOS technology exhibits a faster speed improvement compared to other process technologies. These promising properties prompt an exploration of CMOS technology as an alternative to provide the low power and cost efficiency for a digital data transceiver.

1.2 Research Objective

The first objective of this research is to demonstrate the capability of CMOS technology. It is possible to develop a CMOS transceiver that can operate at a frequency beyond the limitation of its circuit bandwidth. This research does not pursue the maximum absolute speed, but rather attempts to prove that this speed limitation can be overcome. This develops into the realization and application of parallel architecture to this research. The second objective is to closely investigate the operation of the multi-phase phase locked-loop (MPLL). The PLL
alone is a very interesting topic in engineering, which is nontrivial and challenging to design and implement as an integrated circuit. The multi-phase PLL has been used for several applications including clock recovery circuits. Despite its sampling nature, in design and analysis it is often regarded as a continuous-time system. A thorough investigation of its operation can provide insight into the system behavior. As a result, an optimal design of the MPLL can be achieved.

1.3 Thesis Overview

This dissertation is organized as follows. Chapter 2 introduces the concept of clock and data recovery circuits. It presents the extensive review of previous work, particularly in CMOS design. Chapter 3 describes 2x oversampling linear phase detection. It includes the system modeling of the multi-phase PLL as well as the analysis of phase noise due to the bang-bang phase detector. The circuit design of the transceiver and its simulation results are explained. In chapter 4, the prototype implementation and measurements are described with accompanying analysis provided. The conclusion of this research appears in Chapter 5. In addition, the complete analysis of the multi-phase PLL is presented in Appendix A.
Chapter 2

Literature Review

2.1 Introduction

Transceiver is an important building block in digital communication systems. Its applications cover a wide range of digital systems that require serial links between units such as chip-to-chip, peripheral I/O, processor-to-processor communication. Additionally, it is also used in networks of digital systems including crossbar switches for Asynchronous Transfer Mode (ATM), optical receivers in Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET). As a result of the advances in process technology, the operating frequency of the digital systems continue to increase and so the speed required transferring data between the systems. In response to growing demand for higher bandwidth per link, many transceivers have been developed over the past decade. They continue to improve their performance in both speed and power consumption. This is due to not only the permission of the advanced process but also the improvement in both circuit techniques and architectures.

![Figure 2.1 A digital transceiver](image-url)
In general a digital transceiver is composed of the transmitter unit, the communication channel, and the receiver as illustrated in Figure 2.1. The transmitter sends the data with the timing controlled by the clock through the channel. The main components of the transmitter are the output driver and in many case the pre-emphasis equalizer. The equalizer shapes the transmitted signal to compensate for the channel response. The output driver sends out the data serially to the channel. The channel can be the copper trace on PCB and backplane, the cable, and the fiber optic. The receiver recovers the timing (or the embedded clock) from the stream of incoming signal and uses this information to retime the data. The main component of the receiver that performs this task is the clock and data recovery circuits (CDRs). Because it has to recover the distorted signal as it went through the bandwidth limited channel, the receiver is usually more complex than the transmitter.

This chapter we review the design techniques for monolithic CDRs appeared in literatures. It intends to cover comprehensively in both circuit techniques and system architectures. A performance comparison among the designs is also included at the last section.

2.2 Clock and Data Recovery Circuits

The basic function of CDR is to recover timing and data from a received data stream. Format of the data commonly used is non-return to zero (NRZ). In NRZ coding, binary 1 and 0 are represented by two distinct voltage (or current) levels as shown in Figure 2.2. Each bit has time duration $T_b$ called *bit-time*. The reciprocal of bit-time: $1/T_b$ is called *bit-rate* or *data rate*: $R$ and measured in bit per second (bps). The advantages of using NRZ are ease of generation and a relatively low bandwidth required. One method to generate NRZ, for example, is simply using binary data to turn on or turn off switch synchronously with a clock. Thus timing of the data is referenced to this clock which we will call it *data clock*. Frequency of the data clock is equal to the data rate.
As shown in Figure 2.2 the power spectrum density of NRZ at data rate $R$ bps has most of its energy within $R$ Hz. However there are two drawbacks of NRZ. First, there is no spectrum component at $R$ Hz and at integer multiple of $R$. Therefore the waveform of received data has no frequency component at data rate and integer multiple of data rate. This makes it difficult to recover. Secondly, timing information can only be obtained from transitions of data between 1 and 0. In case that NRZ has long sequences of consecutive 1 or 0, transitions are absent and so is the timing information. Furthermore, although data is transmitted as digital waveform, the received data usually suffers from noises and distortions while it propagates through a communication channel. In addition, most of high speed, cost-efficient links do not send the data clock separately. Consequently, the receiver circuit must have ability to extract timing information (the data clock) from the received data. The extraction of this implicit signal is called clock recovery. This timing information is then used in the process of retiming or regenerating data, the data recovery. Simplified block diagram of a digital receiver with CDR is illustrated in Figure 2.3.
There are several techniques and architectures to implement CDRs. They are varied depending on their applications. However, they can be classified into two groups regarding to the phase relationship between the data clock and a local clock at the receiver, the receiver clock.

### 2.2.1 CDR with Phase Synchronization

CDRs in this category are used techniques that require the receiver clock to maintain a constant phase relationship with the data clock. In order to do that, the receiver oscillator must adjust its frequency following any frequency change of the received data. Practically, both clocks only have the same average frequency. Therefore the phase difference between them $\Delta \phi(t)$ may be not truly constant but is bounded within a small range [1].

$$\Delta \phi(t) < \Delta \phi_{\text{max}}$$  \hspace{1cm} (1)

A phase-locked loop (PLL) is commonly used to keep the phase difference within the limit. This technique is sometime called *tracking clock recovery*. 

![Figure 2.3 Digital receiver with CDR](image)
2.2.2 CDR without Phase Synchronization

In this technique, data clock and receiver clock are derived from independent oscillators that have their average frequencies nominally the same. The local oscillator does not try to adjust itself following any frequency change of the data clock. Therefore the phase difference between receiver clock and received data varies with time. There is no phase locked between those signals. Data is recovered by using free running local clock to sample received data at a high rate, several samples per bit-time. These samples are then processed digitally to determine individual bit value. The data can be recovered correctly as long as the frequency mismatch does not exceed a certain limit. This technique is also called *oversampling clock recovery*.

2.2.3 Performance Metrics

In addition to speed (bit rate) and power consumption, a performance of a CDR is commonly evaluated in term of the following quantities.

**Jitter Performance**

Timing jitter from the transmitter and noises from communication channel contribute to the jitter of received data. This is the input jitter to the system. Ideally, the CDR reduces the input jitter through its low-pass behavior of its jitter transfer function and provides less-jitter clock and data. How well the CDR perform this task is measured from the amount of jitter in the recovered clock, the *output jitter*. The quantity is usually specified in time more than in phase. The unit in time can be second or in *unit interval* (UI), which is equal to one bit-time. Jitter can be observed as a horizontal spread of an eye diagram displayed on oscilloscope. It is specified in both rms and peak-to-peak value.
**Bit-Error Rate (BER)**

The number indicating the probability of a bit sent is received incorrectly. Theoretically, it can be calculated from signal-to-noise ratio (SNR) of the received data providing known signal conditions and noise distributions. In practice, this probability is measured via a bit error ratio test (BERT), performed using an error performance analyzer. Bit error ratio is defined as follow:

\[
\text{bit error ratio} = \frac{\text{number of bits received in error}}{\text{number of bits transferred}} = \frac{\text{error count in measurement period}}{(\text{bit rate}) \times (\text{measurement period})}
\]

**Run Length**: The maximum number of bits in consecutive one or zero that the CDR can recover correctly.

### 2.3 Phase Synchronization CDRs

The standard scheme of the phase synchronization CDR is shown in Figure 2.4. It uses PLL to lock its local oscillator (VCO) to received data (NRZ). It operates as following. The phase difference between the received data and the VCO clock generates the control signal driving the loop to the lock condition where the VCO frequency is equal to data rate and phase different is equal to zero. Once the loop is locked, one edge of the VCO clock aligns with bit boundary and the other edge samples at the center of the data bit as shown in Figure 2.5. The VCO clock is now representing the recovered clock. The sampled data is regenerated and synchronized with the recovered clock.
Noting that the scheme not only recovers timing and data, it also regenerates data clock and serial data, the feature required for repeaters in optical networks.

Although this CDR scheme looks similar to a simple conventional PLL, several of its features are different. First, the input signal to the loop is NRZ. As a result it requires a phase detector (PD) that can handle the non-periodic waveform. Secondly, the PLL of the CDR must be optimized to operate with a high frequency, distorted input signal. The loop must have a good input jitter rejection. This characteristic is achieved by using PLL with a narrow loop bandwidth. However PLL with a narrow loop bandwidth has a small capture range and
unreliable acquisition - features that are not desired. Therefore the simple scheme cannot provide both features simultaneously. Consequently, this CDR has been developed further in both circuits and loop architectures to have a good jitter performance and reliable acquisition as well as support very high data rate. We reviews these modifications starting with a key building block that has the most influence to the change, the phase detector. Then several loop architectures are described. Finally we will cover some aspects of other loop components such as VCO and loop integrator.

2.3.1 Phase Detectors

Because input data is NRZ, transition does not occur every clock cycle. It cannot use phase detectors that commonly used with periodic signal like multiplier, XOR, and 3-state phase frequency detector (PFD). It has to be a data activating phase detector. This type of circuit generates an error signal only when data transition occurs. There are two kinds of this circuit based on its output signal, the analog-output and the digital-output.

**Analog-Output PD**

This kind of PD generates the error signal linearly proportional to the input phase difference. Therefore a PLL using this PD will correct itself proportionally to the error. As a result, it can be approximated as a linear system. In sequence, it is easier to design and optimize loop. The most widely used one is Hogge’s PD [2] as shown in Figure 2.6.
It consists of two identical D flip-flops (DFFs) and xor gates. The waveforms show a scenario in which NRZ is leading VCO clock (clk). The PLL tries to line up rising edges of clk to transitions of NRZ. XOR1 creates UP pulse that its width is defined by a transition of NRZ and a falling edge of clk. XOR2 creates DN pulse. The width of DN pulse is equal to the time that clk is low. If clk has a 50 percent duty cycle, the difference between UP and DN is the phase error.

The PD produces output pulses only when a transition occurs. In the locked condition falling edge of clk is sampling at the center of each data bit and Q1 is the retimed data. Therefore, this circuit performs both phase detecting and data retiming in one unit.
Hogge’s PD works well with data rate up to several hundreds Mbps. However, there are limitations that can be problems at very high data rate (Gbps). First, the propagation delay of DFF1 \(t_{ctq1}\) is included in the UP pulse as designated by the shade areas while the propagation delay of DFF2 \(t_{ctq2}\) is not added on DN pulse since it is cancelled out with the delay of D2. At very high data rate \(t_{ctq1}\) can be a significant fraction of a bit time. To alleviate this effect a delay matched with \(t_{ctq1}\) was added between Q2 and the input of XOR2 as reported in [3]. Secondly, it requires clk to have 50 percent duty cycle, otherwise it will cause static phase error.

In addition to those limitations, Hogge’s PD is sensitive to data transition density. This is because at the lock condition the present of data transition creates UP pulse and then followed by DN pulse. Although UP and DN are perfectly matched so the net charge to the loop is zero, the fact that they do not occur in the same time results in the triangular pulse on the output of the loop integrator. Since each triangular pulse has positive net area, the present or absent of such a pulse affects the average output of the loop integrator causing data dependent jitter. To reduce this effect Hogge’s PD was modified to create one UP pulse following by two DN pulses then ending with another UP pulse. As a result, both net charge and net area of the triangular pulse are zero. Therefore the data dependent jitter is greatly reduced. Modified versions of Hogge’s PD were reported in [4,5,6]. In [6] the circuit using both clk rising and falling edges was employed in order to reduce clock speed by half.

Another PD operating with clock at half of the data rate is reported in [7]. As shown in Figure 2.7 it consists of two master-slave DFFs and two XOR gates. Its operation can be described as following. NRZ data is applied to both DFFs. The top DFF is clocked by the falling edge while the bottom one is clocked by the rising edge. The PD generates two signals at the XOR gates, Reference and Error. Reference is a high pulse, one bit-time long created when there is a transition in NRZ regardless of the phase error between clock and data. Error is also a high pulse and created when there is a transition in NRZ but its width varies according to the phase error. It will be a half of a bit-time if clock edge is lined up with
the center of each data bit. It will be smaller if clock leads NRZ and wider if clock lags NRZ. Because clock speed is a half of data rate, output Y1 and Y2 are the demultiplexed output of NRZ. They are valid alternately for two bit-times. Instead of using Error directly, the PD output is generated from the difference of Reference and Error after scaling up amplitude by a factor of two. As a result, the data dependence in Error and Reference are cancelled each other out.

This PD however to operate as described at high data rate requires a very stringent circuit design. First the circuit must be able to produce output pulse as small as half of the bit time. Secondly, the amplitude scaling up of Error must be precise otherwise it will introduce additional phase error. Finally, similar to Hogge’s PD it requires clock to have 50 percent duty cycle.

The last phase detector worth to mention is the sample and hold phase detector [8]. Its idea is using the rising edge of NRZ data to sample VCO signal and store its analog voltage. The phase error signal is then obtained from the voltage level.

The idea is feasible since at frequency range of GHz the VCO clock appears as an analog signal. Its voltage level changes over its period. Considering a VCO signal in Figure 2.8, if we use the voltage level at the middle of its transition as a reference for phase zero then voltage levels will changes proportionally from the highest at phase equal to -π/2 to the lowest at phase equal to π/2. Consequently, the phase error signal of PD can be generated from these voltages.
Figure 2.7 Savoj’s PD and its operation
One interesting point we can observe from this PD is that we can use VCO clock to sample voltage level of NRZ and derive phase error as well. It is actually better in several aspects such as faster edge rate of VCO is more suitable for sampling than that of NRZ, both rising edge and falling edge voltage of NRZ can be sampled thus increasing update rate of PLL. However, PD that takes this approach must have ability to mask out samples when there is no transition in NRZ and respond accordingly, such a PD is reported in [9,10].

**Binary-Output PD**

This type of circuit generates output signal that do not proportional to the input phase difference. The outputs simply carry information as lead/lag, fast/slow. This information is used to create a constant correcting signal that has a polarity according to input error. Thus the transfer characteristic of the PD is non-linear. An example of the circuit is shown in Figure 2.9 [11].
As shown in Figure 2.9 clk and clk_b is used to sample input NRZ. Therefore samples at A, T, and B are separated by a half clock period. Ideally, in locked condition A and B are at the center of data eye and T is at bit boundary. The samples are used to determine the phase relationship of NRZ and clk as described in the table. A modified version that works with a clock frequency half of a data rate was reported in [12]. This type of PD has an advantage in speed. However, there are two problems inherent with this phase detection scheme. First, the loop forces the sampler to sample at a time that might create a meta-stable state in a normal digital circuit. Secondly, because of “bang-bang” operation of PD, it results in non-linear control loop that is less stable and produces data pattern jitter.

Recently, an improved bang-bang PD was reported [13]. It adds two more sampler in the middle between A and T, and T and B. Therefore each sample is separated by one forth of clock period. The detection resolution is now $\pi/2$ and the correcting signal has two different...
levels as shown in Figure 2.10. This gives the response that is more proportional to phase error with the expense additional hardware.

![Avg Charge Pump Output over 1 cycle](image)

**Figure 2.10 Improved bang-bang PD**

### 2.3.2 Loop Architectures

The standard scheme as in Figure 2.4 has a good tracking ability but has a slow and unreliable frequency acquisition process. Because of large initial frequency offset between data clock and VCO, an acquisition aid is necessary. Generally, it is an auxiliary circuit operating in such a way that reduces the frequency offset to the PLL capture range. Different kind of auxiliary circuits yield different loop architectures. Some auxiliary circuits are quite complicated. Therefore it is not unusual to find them constituting more than half of the total CDRs. In this section we have classified those loop architectures into three groups; the frequency-locked loop/phase-locked loop, the delay-locked loop/phase-locked loop and the data loop/reference loop architecture. We then explore these three different architectures.
Frequency-Locked Loop /Phase-Locked Loop (FLL/PLL)

The main idea of these architectures is using the frequency loop to assist the frequency acquisition at the initial state while the phase loop are responsible for tracking the input data by maintaining the phase-locked condition.

As shown in Figure 2.11, it consists of FLL and PLL sharing a VCO (or sharing both an integrator and a VCO). First the frequency loop reduces the error in frequency between input data (NRZ) and VCO clock. Once frequency error is sufficiently small, the phase loop takes over and acquires the phase lock. Because control signals from frequency loop and phase loop are combined to control VCO, it is possible that their signals drive VCO in the opposite direction and lead to an unstable state. To prevent that situation, the frequency loop is often designed to have a constant loop gain while the loop gain of PLL increases as frequency difference reduces. Consequently, frequency loop is dominant at the beginning and its affect reduces as frequency difference gets smaller. During the final state of operation, the output of the frequency detector is identically zero, and no longer affects operation of the circuit.
Because the NRZ signal do not have frequency spectrum at the data rate, the non-linear technique is required in order to create that spectrum for frequency detection. The common technique is using edge detector circuits such as a differentiator followed by a rectifier, and a 2-input XOR with a small delay on one of its input.

There are two approaches of circuit implementation of this architecture, an analog approach and a digital approach. The analog implementation uses quadricorrelator technique [14,15,16,17] for frequency detection. An example is shown in Figure 2.12[17]. It uses quadrature outputs from VCO mixing with output of edge detector circuit and then low-pass filter to get $\sin(\omega_1-\omega_2)t$ and $\cos(\omega_1-\omega_2)t$. The $\sin(\omega_1-\omega_2)t$ signal is used as the control signal of phase loop. The $\cos(\omega_1-\omega_2)t$ signal is differentiated and mixed with $\sin(\omega_1-\omega_2)t$ resulting in $(\omega_1-\omega_2)\cos^2(\omega_1-\omega_2)t$. The average of this signal represents both polarity and magnitude of frequency difference. It is used as the control signal of the frequency loop. As frequency difference decreases, it approaches zero and the phase loop takes control, locking VCO output to the input data.

Figure 2.12 Quadricorrelation
Generally, if there is a frequency difference between any two signals, then their phase relationship will change with time at a rate proportional to the frequency difference. Following this fact, the digital approach of this architecture is designed. The key block of this approach is the digital frequency detectors, the rotational frequency detectors [3,18] and the phase frequency detector for NRZ data [19,20,21]. Both use input data to sample VCO clock and its quadrature. Then comparing the samples to determine their phase and frequency relationship through the beat note signal.

![Rotational Frequency Detector](image)

**Figure 2.13 Rotational frequency detector**

**Rotational Frequency Detector**

Shown in Figure 2.13 is the rotational frequency detector. It operates as following. Signal $\phi_1$ and $\phi_2$ are created from the in-phased (I) and the quadrature (Q) of VCO. They are sampled by transitions of input NRZ. The samples are shifted left every clock cycle by I. As seen
from the waveforms, if there is a frequency difference, the sampling position will move. Once the sampling point move across boundary BC, current samples stored in registers FF1 and FF2 are different from their previous samples stored in FF3 and FF4. Thus the frequency difference is detected. However, it can only determine whether VCO frequency is faster or slower than data rate.

Rotational frequency detector is quite simple and useful. However it can detect only frequency difference that is not greater than a half ($\pm 50\%$) of the data rate. To use in CMOS technology which VCO center frequency varies widely over process variations additional post-fabricated adjustment on VCO may be required. Furthermore, at very high speed the transition of received data is not sharp and strong enough to use for sampling. Thus it must be buffered. As a result, the data rate is limited by the circuit bandwidth of that buffer.

**Phase-Frequency Detector for NRZ**

Figure 2.14 shows the block diagram of the PFD for NRZ [19]. The principle of this technique is to create two beat notes (signals that has frequency equal to the different between NRZ and VCO frequency) using in-phase(I) and quadrature(Q) components of the VCO. By observing these two beat notes, frequency relationship between NRZ and VCO can be extracted. Its operation can be described as following. VCO output I and Q are sampled by every transition of input NRZ and their analog voltages are stored. Then the sampled signals are fed to a limiting output buffer. If the frequency of VCO and the data rate are not equal, the buffer outputs Q1 and Q2 will be beat note signals. Timing relationship between the beat notes provides information for detector circuits to generate signal Q3 indicating whether VCO is faster or slower than NRZ. As one can observe, during the time that Q2 is low, a transition of Q1 from low to high indicates $f_{\text{VCO}} > f_{\text{DATA}}$ and a transition of Q1 from high to low indicates $f_{\text{VCO}} < f_{\text{DATA}}$. In the same time the polarity of Q1 indicates the polarity of phase difference. Q1 is low (negative) meaning NRZ leading VCO and Q1 is high (positive)
meaning VCO leading NRZ. Q1 (phase status) and Q3 (frequency status) are used to drive loop into lock condition. Once both phase and frequency are locked, Q1 is the sample at zero crossing and its average will be zero.

The advantages of this PFD are speed and its simple circuit scheme. The front-end circuits that handle NRZ are the sample and hold which can operate at very high frequency. The other circuits after the limiter are driven by the beat notes, which are much slower than data.
rate. There are some drawbacks of this technique. First, since the NRZ is used to sample VCO, its rising edge and falling edge must be well defined. This requirement can be met in fiber optic but is difficult to meet in band-limited channels such as back plane and copper cable in which the data experience the severe ISI. Another disadvantage is its binary detection (fast/slow and lead/lag) of phase error contributing to output jitter.

The frequency range that the phase-frequency detector can detect covers $f_0/2 < f < 2f_0$ where $f_0$ is the center frequency of VCO. However because of the reducing of the DC component in the signal Q3 as the frequency difference increases the gain of the frequency detector decreases. This practically diminishes the effective range of the frequency detector. To increase the rage, an auxiliary circuit may be required. As in [22], a circuit that performs a digital search algorithm is added to the frequency detector. The circuit basically senses the DC level of the frequency detector output. If it is too small meaning the frequency difference is too large, the circuit will adjust the capacitor of its LC oscillator in such a way that bring the VCO frequency close to the data rate. Once the frequency difference reduces to the range that frequency detector can operate reliably the search algorithm stops and the frequency detector takes over.

**Delay Locked Loop / Phase Locked Loop (DLL/PLL)**

In FLL/PLL architecture, the CDR can have a good jitter rejection as a result of a narrow loop bandwidth of its PLL and in the same time, can have a fast acquisition property from its FLL. However, if the PLL used is a second order (or an approximate second order) system, its closed-loop frequency response i.e. the jitter transfer function will exhibits a jitter peaking, the condition that its gain exceeds unity over some rage of frequency. Thus over that range the input jitter is amplified. This is an undesirable feature particularly in systems that cascade several CDRs such as a string of repeaters since it contributes to the accumulation of jitter. The jitter peaking occurs because in the second order PLL the closed-
loop zero is always located at frequency lower than that of the closed-loop poles. Increasing the damping ratio, which effectively moves zero closer to poles, can reduce but eliminate the jitter peaking. However this often results in slow down the acquisition speed of the acquisition aid.

One solution that can eliminate jitter peaking and allow the PLL to maintain a small loop bandwidth without compromising acquisition speed is changing architecture of the CDR so that its PLL has no closed-loop zero. This is accomplished by modifying the loop filter to have only a capacitor and adding a voltage-controlled phase shifter or voltage-controlled delay line (VCDL) at the input path to the loop [5] as illustrated in Figure 2.15.

Assume that gain of the VCO, $K_{VCO}$, is greater than gain of the VCDL, $K_{VCDL}$. The linear system analysis shows that the sum of open-loop gains of the first order DLL and of the second order (without zero) PLL results in the loop transmission that inflects at the frequency equal to $K_{VCO}/K_{VCDL}$ rad. Thus the loop transmission behaves as if there is a stabilizing zero at that frequency. The loop crossover frequency is the same as the DLL crossover frequency, $K_D/K_{VCDL}$. The closed-loop transfer function is an all-pole second order with the similar poles as a standard PLL. Therefore it has the same stability. Because there is no zero, as long as the damping factor is greater than or equal to 0.707 it has no jitter peaking. In addition, the first pole locating at approximately $K_{VCO}/K_{VCDL}$ rad determines the loop bandwidth instead of the
second pole as in a standard PLL. Since the acquisition speed is determined by the loop crossover frequency $K_D \cdot K_{\text{VCDL}}$ and jitter filtering is determined by loop bandwidth $K_{\text{VCO}} / K_{\text{VCDL}}$, by using a high $K_{\text{VCDL}}$ a DLL/PLL can provide both narrow bandwidth (a good jitter rejection) and rapid acquisition simultaneously.

There are some issues need to be considered carefully. Firstly, the acquisition process of this architecture is combined effort of both the DLL and the PLL. It has to be ensured that it drives the loop in the same direction. Secondly, unlike the RC-realized zero of the standard PLL, this stabilizing zero disappears if the DLL is driven to the end of it delay range. As a result, the loop can be unstable. Because the DLL and the PLL share the same control voltage, the VCO tuning range then must not drive the DLL out of its range. Thus the VCO tuning range is a subset of the DLL tuning range. Therefore the range of the DLL defines the operation rage of this architecture. In term of control voltage it can be expressed as

$$\frac{\Delta \omega}{K_{\text{VCO}}} \leq \frac{\Delta \phi}{K_{\text{VCDL}}}$$

$$\frac{K_{\text{VCO}}}{K_{\text{VCDL}}} \geq \frac{\Delta \omega}{\Delta \phi} \tag{2}$$

where $\Delta \omega$ and $\Delta \phi$ are tuning ranges of VCO and VCDL. The equation (2) reveals that the lower limit of the loop bandwidth is not arbitrary but defined by the ratio of the VCO frequency range and the range of the VCDL.

**Data Loop / Reference Loop Architecture**

In preceding architectures, CDRs are capable to operate with a range of data rate as wide as its acquisition range allows. Usually, either a tuning range of the VCO or an operating range of its frequency detector limits the range. There are some applications however, required only to operate at one data rate. Therefore the task of acquisition aids reduces to only bring the VCO frequency to the specific data rate. This auxiliary circuit is often implemented as
another PLL locking to a local reference clock. The reference clock has a nominal frequency the same as data clock. This loop is referred as the reference loop. A simplified block diagram of this architecture is illustrated in Figure 2.16.

![Figure 2.16 Data loop/Reference loop](image)

Noting that the reference loop uses 3-state PFD resulting in an excellent acquisition. The other loop, the data loop uses phase detector and its input is NRZ data. Generally, reference loop first tunes VCO to the data rate then the data loop is activated and nullifies initial phase offset. Depending on its application, the reference loop may be disabled completely or may continue active after data loop is locking. An additional circuit such as a controller or frequency monitor is necessary to handle transitions between loops. Several schemes based on this architecture are described as following
Matched Gated Ring Oscillator Scheme

In some application such as burst mode transmission the instantaneous locking is required. This can be done by using matched gated ring oscillator scheme [23,24]. A gated ring oscillator is a ring oscillator whose output stage uses a NOR gate (or NAND gate) instead of a inverter. Therefore it allows an additional control signal (G) to start and stop the oscillation. A circuit diagram of the oscillator and a block diagram matched gated oscillator scheme are shown in Figure 2.17.

![Matched gated ring oscillator scheme](image)

The scheme uses three identical gated ring oscillators, VCO1, VCO2 and VCO3. The VCO1 has G connecting to GND so it always oscillates. It is a part of reference loop locking to reference frequency and providing a control voltage to VCO2 and VCO3. The G inputs of VCO2 and VCO3 are controlled by level of NRZ and its inverse respectively. Consequently, VCO2 and VCO3 are alternatively activated. Combined outputs of VCO2 and VCO3 are the recovered clock. The retimed data is the output of a DFF that clocked by the recovered clock.

This scheme has its advantages that it can lock on the first data transition and can handle low data transition density. However, because it is a broadband open loop system (no loop bandwidth), it has no jitter rejection.
Phase Selection Scheme

The block diagram of this scheme [25] is shown in Figure 2.18. It consists of a reference loop and a data loop that both are active all the time. The reference loop is a PLL multi-phase clock generator. A VCO of the reference loop provides a number of equally spaced clock phases at frequency of $N_{\text{ref}}$ (nominally equal to data rate). This loop can have a large tuning range since it is used a phase frequency detector. Clock recovery is performed by data loop. The data loop selects a clock phase from the reference loop that is best aligned with the incoming NRZ data. This clock phase is the recovered clock and it is used to retime data. Noting that the data loop uses digital filter instead of loop filter because the loop corrects itself by switching to a new clock phase not by tuning VCO frequency. If there is a frequency offset between $N_{\text{ref}}$ and data rate, an appropriate clock can still be generated by changing the control signal to select a different phase over time.
An advantage of this architecture is the independent selection of bandwidth in those two loops. The reference loop can be designed to have a wide bandwidth in order to suppress VCO jitter, for example, jitter induced by power-supply noise. At the same time, a narrow bandwidth can be used in the data loop to reduce jitter transferred.

A drawback of this scheme is the large cycle-to-cycle jitter that results from phases switching. Increasing the number of phase reduces phase spacing and the jitter. Having more delay stages in the VCO can generate more phases but this limits the speed. Other methods that enable large number of phases without degrading the VCO speed are using a phase interpolation [26] and a coupled oscillator [27] as will be explained in section 0.

![Figure 2.19 Feedback phase selection scheme](image)

Figure 2.19 Feedback phase selection scheme

An improved version of this technique that reduces the output jitter is the feedback phase selection scheme [28]. As shown in Figure 2.19, it moves the phase selection into the reference loop. Instead of selecting a clock phase for the phase detector of the data loop, the selected clock phase is fed to PFD of the reference loop. When data loop detects a misalignment of the NRZ and the VCO clock, the control signal from the digital filter is
changed to select a different phase of the feedback clock. This will cause a phase change in the divided clock feeding the PFD such that the charge pump will alter the VCO control voltage stored in the loop filter. Therefore, sudden phase steps generated by the clock recovery logic will be smoothed by the filter of reference loop, causing the VCO clock to slowly drift toward the correct phase with a rate of change determined by the bandwidth of the reference loop. As a result, more than a half of the output jitter is reduced. This scheme still has the advantage of the independence of selection of bandwidth in those loops.

**Multi-Phase Parallel Sampling Scheme**

All the CDRs that have been studied so far are using a serial sampling technique. The technique uses a VCO that has a frequency at the data rate to sample NRZ data serially. As a result, the incoming data is not only recovered, but it is regenerated as well. The regenerated data can be transmitted again to a next receiver at the same data rate. The ability to regenerate serial data is required for some digital communication links such as the repeater in optical networks. The serial CDRs however, requires its circuit blocks such as the phase detector, the VCO, and the sampler to operate at the same speed as the data rate. Consequently, for very high data rate applications (several Gbps) most of the serial CRCs are implemented in high $f_T$ process like Silicon bipolar, GaAs, and SiGe.

For a digital link of computer systems such as a chip-to-chip serial link, there is no need for the receiver to regenerate serial data, instead it needs to recover and deserialize data to a parallel format (word). Then the parallel data is synchronized to the receiver system clock. These can be achieved simultaneously by using a multi-phase parallel sampling scheme.

This technique uses slower speed VCO to recover faster input data. The reference loop tunes a N-stage differential VCO to the frequency that is equal to $1/N$-th of the data rate. Therefore the VCO clock period is equal to $N$-bit-time. If $2\cdot N$ equally spaced clock phases are tapped
from the VCO, the time resolution between any adjacent clock phases will be equal to one half of a bit-time. The parallel sampling is then accomplished by using all $2 \cdot N$ clock phases to sample incoming data. This results in an effective sampling rate two times of the data rate ($2x$) as shown in Figure 2.20.

![Figure 2.20 Multi-phase parallel sampling (shown only the data loop)](image)

To perform the phase detection, there are $N$ binary-output PDs (see section 0) in data loop. Each of them uses three successive clock phases to complete its “bang-bang” operation. Considering PD1 for example, it uses $\phi_1, \phi_2,$ and $\phi_3$ to sample the incoming data. Assuming a frequency difference is very small but there is some phase offset between data transitions and clock phases. Since the phase space is equal to a half of the bit-time, as $\phi_1$ and $\phi_3$ sample close to the center of two consecutive bits $\phi_2$ samples close to the boundary (or the transition) between those two bits. These three samples then are used to determine if the clock phases samples late or early. If there is a transition and the clock phases are late, the samples at $\phi_2,$
and \( \phi_3 \) will be the same and opposite to the sample at \( \phi_1 \). If the clock phases are early, the samples at \( \phi_1 \) and \( \phi_2 \) will be the same and opposite to the sample at \( \phi_3 \). Based on the late or early logic, PD1 then generates a constant error signal, UP1 or DN1 to a charge pump to change control voltage in such a way to reduce the phase error. Together all N phase detectors operate in time interleaved. The UPs and DNs signals generated from each PD that detects a data transition are combined to correct the loop. In the same time, the incoming data are demultiplexed at the phase detectors and they are re-aligned as a word with one of VCO clock phase by a data aligner (an array of latches).

The multi-phase parallel sampling has the speed advantage. Because data is sampling in parallel, each circuit blocks operate at the frequency 1/N-th of data rate. Therefore the circuit bandwidth requirement is relaxed. This allows the CMOS process, which has lower \( f_T \) but is highly integrated and cost-efficient to be used in very high-speed applications up to several Gbps [29,30,31,32].

Drawbacks of this technique are caused by the use of the binary-output PD. The data loop forces the sampler to sample at a time that might create a meta-stable state. The “bang-bang” loop control increases data dependent jitter and also limits the tracking range of the data loop. Additionally, the effective input capacitance of the receiver increases because the input capacitances of all samplers are parallel together. If the input capacitance is too large, it will adversely reduce bandwidth the receiver. There is a trade off between multiplexing ratio (N) and input capacitance to optimize speed.

2.3.3 Voltage Control Oscillator

The recovered clock is generated by VCO therefore the performance of VCO directly impacts the performance of the CDR. The jitter from VCO transfers to be output jitter of the recovered clock through the high-pass transfer function. Furthermore, the system analysis
shows that the –3 dB frequency of the high-pass function is the same as that of the low-pass jitter transfer function of its PLL. Thus the CDR employing a PLL with narrow bandwidth to reject input jitter will allow more VCO jitter contributing to its output jitter. Consequently, minimizing the VCO jitter is one of the most important issues in VCO design. The other important features are that the VCO should have are a wide tuning range and the linear frequency transfer characteristic with its control signal. The wider tuning range of VCO usually results in a wider the operation range of the CDR. The linearity characteristic of VCO with its control signal maintains a constant loop gain in the PLL over its lock range therefore improves the loop stability.

Most of VCO in CDRs are based on the ring oscillator. It has several advantages such as its ability to provide multi-phase clock required in some CDR architectures, its wide tuning range and its moderate area and power consumption required. However as the frequency operation increases, output jitter allowed as a percent of clock period (U.I) is very small and is difficult to achieve with the ring oscillator especially in CMOS technology. Therefore, recently CMOS CDRs have begun to implement their VCOs with the LC oscillator as it displays a lower output phase noise than the ring oscillator. In this section we review several topologies of both oscillators.

**Ring Oscillator**

There are several circuit design styles of delay cell in the ring oscillator. However the differential delay cell with a tail current source as show in Figure 2.21 are the most common. This is because its differential configuration results in good common noise rejection particularly to the supply noise. The tail current source providing high impedance to substrate reduces the effect of substrate noise coupling to the output node. Additionally, it provides both clk and clk_b usually needed for the fully differential implementation of the CDR. The output from this type of delay cell is a 50 percent duty cycle and small-swing signal. In case
that the full-swing clock signal needed, it requires an additional circuit to convert its output to the full swing signal. This circuit can introduce an error in duty cycle if it does not carefully design. Delay $\tau_d$ of the delay cell is proportional to $R_L C_L$, where $R_L$ is the resistive load and $C_L$ is the effective capacitive load, mainly the input capacitance of the next delay stage. To vary the oscillation frequency, the control signal is applied to either change the load $R_L$ or change the amount of charging current through the tail current source.

Figure 2.21 A differential ring oscillator and its delay cell

Figure 2.22 A delay stage and its control-biasing circuit
Figure 2.22 shows the a delay stage and its control circuit of the ring oscillator. In this design the frequency of oscillation is linearly proportional to the tail current controlled by \( V_{\text{con}} \). The design can be explained as following. The biasing circuit is a replica of the delay stage. The PMOS loads are biased in linear mode (triode region) and forced to have a constant voltage drop by the opamp feedback loop. As the \( V_{\text{con}} \) changes the tail current, the opamp changes PMOS bias voltage to maintain their constant voltage drop. Therefore

\[
\tau_d \propto R_L C_L = \frac{V_{\text{drop}}}{I_{\text{tail}}} C_L
\]

\[
\tau_d \propto \frac{1}{I_{\text{tail}}}
\]

\[
f_{\text{vco}} \propto \frac{1}{\tau_d} \propto I_{\text{tail}}
\]

Although this VCO gives a wide tuning range and a linear characteristic, it requires an opamp in biasing circuit. Furthermore, its response to the control signal is limited by the response of opamp feedback loop.

**Interpolative Ring Oscillator**

The tuning range of ring oscillator can be extended further with this topology. In this technique [17], each delay stage consists of two delay paths, a fast path and a slow path as shown in Figure 2.23 (a). The delay of each stage is adjust by decreasing gain of one path and increasing that of the other. As a result, the delay is the interpolation of the delays of the two paths. In the extreme cases, the slow path is completely off resulting in shortest delay, which define the maximum oscillation frequency. On the other hand, with the fast path off, it provides the largest delay defining the minimum frequency. The circuit implementation of this technique is shown in Figure 2.23 (b). In this design, it uses two control signals, \( V_{\text{fine}} \) from phase loop and \( V_{\text{coarse}} \) from frequency loop of FLL/PLL architecture and combined to generate differential control signal.
Because oscillation frequency of ring oscillator is proportional to the inverse of the total delay in the ring thus, the number of delay stage must be reduced to have higher oscillation frequency. This creates a problem since the criterion for the ring oscillator to oscillate are to have total ac phase shift 180° plus another 180° from dc phase shift (inverting output) and gain greater than 0 dB at oscillation frequency. Therefore for two-stage ring oscillator to oscillate, each delay stage must establish 90° ac phase shift within it unity-gain bandwidth, the condition that can not attain with the delay cell in Figure 2.21 since it has only one pole within its unity-gain bandwidth. There are two solutions for this problem one is using the double differential delay cell in ring oscillator [21] and the other is using inductive load instead of resistive load in the delay cell [8]. Both techniques are explained as following
Double Differential Delay Stage

The double differential delay stage is shown in Figure 2.24. It consists of two differential amplifiers with current mirror load connecting in parallel. Since the output of the cell is the combined of the single end output of each differential amplifier in opposite phase, therefore the dc gain is two-time of the differential delay cell of Figure 2.22 using the same transistors. Furthermore the frequency response analysis shows that the single-ended connecting of each current mirror load yields an additional pole-zero pair at the mid-band frequency increasing ac phase shift. As a result of increasing dc gain and ac phase shift simultaneously, this delay stage can fulfill oscillation requirement.

Delay Stage with Active Inductance Load

In this case the resistive load are replaced by a composite load consisting of R,C and a PMOS. This load with certain conditions will be inductive. As a result, it provides an extra phase shift within the unity gain-bandwidth to allow the oscillation. The small signal analysis
show that if \( C < C_L \), where \( C_L \) represents the capacitance at the output node, then this delay cell will provide \( 90^\circ \) phase shift within the unity-gain bandwidth.

![Delay cell with active inductance](image)

**Figure 2.25 Delay cell with active inductance**

Noting that the delay of this delay stage is adjusted by varying tail current changing the gain not the load of the cell. Therefore, amplitude of the output varies with its frequency. Although the load is inductive it does not form a resonance circuit as in LC oscillator.

**LC Oscillator**

The LC oscillator has its main advantage in lower output phase noise as a result of frequency filtering of its LC tune circuit. In addition, it is a self-limiting oscillator, meaning the amplitude of its output signal is controlled by its non-linearity of the active devices in the circuit. Thus no need for additional amplitude control. However, the LC oscillator has several drawbacks. First, for varactor-based tuning, its frequency tuning range is often limited by low supply voltage and maximum capacitance available to varactor. This is because at high frequency the parasitic capacitance can be a large portion of total effective capacitance. As a
result, the tuning range is typically less than 20 percent. Secondly, because of its on-chip inductance the LC oscillator usually occupies much larger chip area than the ring oscillator. Its power consumption is also greater than the ring oscillator.

The following LC oscillator shown in Figure 2.26 overcomes some of its drawbacks. It is a coupling oscillator [33, 22]. It consists of two identical negative-Gm oscillators M1-M2 and M3-M4. M5-M6 and M7-M8 are the transconductance stages coupling both oscillators. Because of the coupling configuration (similar to a two-stage ring oscillator), the oscillators are synchronized and providing the quadrature outputs. Instead of using varactor-based tuning, the frequency tuning is the combination of varying the coupling and varying the oscillator gain through their tail currents. In addition, the differential V-to-I permits the control signal to be differential thus improves the common noise mode rejection. As expected, CDRs with a LC oscillator shows a significant improvement in their output jitter [22, 51].

![Diagram of the coupling LC oscillator](image)

**Figure 2.26 The coupling LC oscillator**

### 2.4 CDR without Phase Synchronization

Alternatively, timing recovery of NRZ data can be done without phase locking. This technique is called oversampling clock recovery. It uses a local clock that does not has a
phase-locked to the NRZ sampling input NRZ at high rate, several samples per bit-time. These samples are then processed digitally to recover individual data value. It has an advantage of being primarily digital which is in contrast of the phase-locked clock recovery, less sensitive to process variation, operating condition and noises. To illustrate the concept of this technique, considering Figure 2.27, which presents the top view of a Nx oversampling data recovery circuit.

An array of $\frac{N \times M}{2}$ sampler circuits using $\frac{N \times M}{2}$ clock phases from a local clock generator usually a PLL clock generator continuously sample the M-bit long NRZ data. One bit of NRZ data is digitally sampled N times producing N-bit oversampling data. Hence, it is called Nx oversampling. A total of $N \times M$ oversampling data are fed to the Phase Detection block and a Delay/Store block. The Phase Detection block extracts phase information from the oversampling data. These phase information then used by the Processing/Decision block to select only one bit out of each N-bits oversampling data to represent each bit of NRZ. This is done by the Processing/Decision block provides the control signal to the N:1 selector. The
selector selects the appropriate M bits out of N\cdot M bits from the Store/Delay block to be the M-bit wide (parallel) recovered data.

The Figure 2.27(b) shows two examples of 5x oversampling. In both cases, the sampling resolution, which is the time between two adjacent sampling phases, is 1/5th of the bit-time. Since there is no phase-locked between the clock phases and the NRZ data, it is possible that the clock phase sample at the middle of the transition resulting in the meta-stable output. The top figure shows the best case where all samples are resolved correctly. The bottom one is one of the worst scenario where \( x \) are samples that can be both “1” or “0”.

2.4.1 Building Blocks

In this section, we describe the design of building blocks for this technique. There are three main circuits including the clock generator, the sampler circuit and the digital processing block. The clock generator and the sampler circuit are very related. Some sampling circuits are designed for a particular clock generator. The digital processing blocks are varied depending on their algorithms.

Clock Generators

The oversampling techniques require a number of uniformly spaced clock phases at a high frequency to sample input NRZ. For a simple clock generator, a PLL using a differential ring oscillator as a VCO can provide clock phases two times the number of delay stage in its ring by tapping the inverting and non-inverting outputs from each stage. Adding more delay stage increases the number of clock phase per period and so the sampling resolution. However, increasing number of delay stage in the ring oscillator decrease its oscillation frequency. Therefore this technique alone cannot provide a fine sampling resolution at high frequency.
For Nx oversampling, a sampling resolution is equal to $1/N$-th of the bit-time. At very high data rate, this time resolution can be smaller than the intrinsic gate delay of ring oscillator. Therefore a particular circuit to create such a fine resolution clock phase is required. There are three techniques to implement that kind of circuit. We describe briefly as following

**Phase Interpolation**

Phase interpolation technique [26,34] is shown in Figure 2.28. It takes two adjacent phases clk1 and clk2 (and their inverses) from the VCO to interpolate. Ideally, an interpolating output clk12 will appear halfway between delayed versions of its input phases, clk1d and clk2d. Consequently, time resolution between clk1d and clk12 as well as clk12 and clk2d will be a half of one delay stage.

The interpolator consists of two differential delay stages similar to those used in the VCO except that size of their tail current source transistor is reduced to be a half and they are sharing PMOS loads. The basic ideal is that a slew rate of a output clock phase of a delay stage is proportional to current drawn through its load. Reducing the tail current by a half, the slew rate will be reduced by a half as well. In the circuit, current $I_1$ is drawn as clk1 is active. Later, as clk2 is active, $I_1 + I_2$ is drawn. If $I_1$ and $I_2$ are equal a half of tail current used in VCO ($I_0$), clk12 will slew at half-rate for half of the time then slew at full-rate. and will appear halfway between clk1d and clk2d. However, because changing current also changes voltage swing, the output phase clk12 practically appears closer to clk2d instead of being the middle. As a result, a compensation is necessary to this techniques such as using $I_1 > I_2$ but sill keeping $I_1 + I_2 = I_0$ to have 50 percent interpolation.

This technique can generate one phase from two adjacent input phases. Thus one level of interpolation can double number of phase. For a high oversampling ratio it may need more
than one level. However, due to its tendency of error it is difficult to compensate a multi-level interpolation correctly.

**Figure 2.28 Phase interpolator**

**Array Oscillator**

An array oscillator is a structure based on a series of coupled ring oscillators as shown in Figure 2.29. The basic idea is to force several ring oscillators to oscillate at the same frequency and have uniformly offset in phase by a fraction of buffer delay. The offset between ring is created by vertically connecting top nodes ($T_i$) to bottom nodes ($B_j$) where $i \neq j$. Since the number of clock phase is equal to the number of delay stage, an NxM array oscillator can provide up to NxM clock phases. Drawbacks of this technique are large hardware and complex routing as well as N and M cannot be arbitrary. Additionally, each buffer delay requires an extra input for coupling with the adjacent ring. Because of a large number of delay stages, its tuning range is limited and its response to its control signal is slow. These can lead to an unstable PLL if it is not carefully designed.
Delay Vernier Technique

This technique is actually a delay generation technique. The main idea of this technique is the finer delay can be obtained using the difference between two coarse delays. The resolution is then limited by how well the coarse delays can be controlled. The technique can be easily explained through the design of matched delay sampler [35] as shown in Figure 2.30. The data and clock are propagated through separate delay chains, consisting of delay $D_d$ and $D_c$, respectively. Each latch samples the data sampling point at its clock’s rising edge. Adjacent latches thus sample the digital data at an effective interval of $\Delta t = |D_c - D_d|$. The advantages of this technique are its fine resolution and the simplicity of its circuit. However, it needs two DLLs to maintain nominal delay time on each delay line.
Digital Samplers

The received data often suffer from timing jitter, noises. In case of band limited channel, it can be heavily deteriorated as a result of inter-symbol interference (ISI). Therefore the sampler must have ability to detect a small difference of signal amplitude, amplify and resolve to the digital signal at high speed. Furthermore, it should be design to minimize possibility of meta-stability.

Sampler circuit is essentially a clock comparator. A typical architecture is shown in Figure 2.31. It consists of a preamplifier and a latch and has two mode of operation, tracking and latching. In the tracking mode, the preamplifier is enabled to amplify the input difference, therefore the output tracks the input, while the latch is disable. In the latch mode, the preamplifier is disabled and the latch is enabled so that the instantaneous output of the preamplifier is regeneratively amplified and logic levels are produced at Vout.
The resolve time of the sampler highly depends on time response of the latch stage. For the equivalent circuit of latch as in Figure 2.31(b), it can show that the time required for regeneration is \([36]\).

\[
T = \frac{\tau}{A-1} \ln \frac{V_{X_{Y1}}}{V_{X_{Y0}}}
\]  

(3)

where \(A\) and \(\tau\) are gain and time constant of latch, \(V_{X_{Y0}}\) and \(V_{X_{Y1}}\) are initial voltage difference and final voltage difference of latch.

Equation indicated that \(T\) is a function of gain and time constant as well as the initial voltage difference (output of the preamplifier). If \(V_{X_{Y0}}\) is very small, \(T\) will be very long and latch can enter meta-stable state. Because the sampler samples random data and the timing relationship between input data and clock is not completely defined, \(V_{X_{Y0}}\) is considered as a random variable and meta-stability is then described in term of probability. The possibility to have meta-stability can be lowered by increasing \(A\), decreasing \(\tau\), or pipelining the comparator output.
Three samplers are described here. The first sampler is shown in Figure 2.32. It is a current mode logic (CML) style [37]. It has been used as a sampler in high-speed digital interfacing circuits [38,39] and as a divider in frequency synthesizer [40,41]. There are some important characteristics about this circuit. First, it gives small swing output that is set by PMOS load. Because of the small swing, it can operate at very high speed. Secondly, the circuit steering a constant current drawn by its tail current source reduces switching noise in power rail. Finally, as operating speed increases gain of the preamplifier stage (M1 and M2) reduces. Therefore at very high speed it usually needs input difference several hundreds mV to operate correctly.

The second sampler [42] is shown in Figure 2.33 (a). It is a sense amplifier following by a static R-S latch. The bottom part serves as preamplifier stage while the top part is a precharged latch stage. The static latch is NAND-type hence it keeps the previous output when its input is precharged to high. It also reduces possibility of meta-stability. Using a precharged circuit speeds up the operation since no need for new output from preamplifier
stage to break previous store value (as in CML sampler). Transistor M1 and M2 are turned on at the end of tracking operation to reduce gain of the preamplifier stage as the regenerative process starts in the latch stage. This circuit has been modified further to improve speed and reduce an offset that arises from an imbalance in capacitance at nodes A and B by adding a digitally adjustable capacitor and a switch to precharge at each node as shown in Figure 2.33 (b) [43,44].

Figure 2.33 (a) Strong ARM sense amplifier (b) Modified version

The last sampler is shown in Figure 2.34 [45,46]. This circuit has a higher input sensitivity and a faster operating speed than previous two examples because not only its latch stage is a precharged circuit but its preamplifier stage is also a regenerative amplifier. It operates in three steps as following. While the preamplifier stage tracks new input with low gain because M1 is turned on, the latch stage is isolated and precharged. So the precharged time is hidden. Once new input is sampled, M1 is turned off so that the preamplifier has a high gain and gives its output to the latch stage to evaluate. The latch stage is then discharged and provides full swing output. Note that the sampler needs both clk and clk_b to control. One disadvantage of this sampler is its limited common mode range. The proper common mode level of its input is not at middle of the supply rail but rather close to GND.
Before leaving this section, the significance of the cross connecting transistors (M1, M2, M3 of Figure 2.33 and M1 of Figure 2.34) should be stressed. They basically alter gain of their circuits when necessary. Providing large gain during amplification state and small gain to break the latch.

**Digital Processing Block**

One set of oversampling data represent a snapshot of input data over a time window covered by the length of sampler. This length usually covered 2-3 bytes of input data. The digital processing block extracts timing information or phase information from these samples based on particular algorithm [46,47]. The most common method is to find the transitions by XOR adjacent sampled bits. Numbers of transition from several sets of oversampling data are tabulated and tallied to determine the bit boundary. Column positions that result in highest score indicate the bit boundary. Once the bit boundary is known, the sampled data at the middle between bit boundary can be select as the correct data.
Alternatively, the bit boundary can be determined from the similarity of the oversampling data. The oversampling data of the same input bit should be the same. 3x oversampling data, for example are grouped into 3-bits word by the phase alignment circuit. If phase aligns correctly, all the bits in each word will be the same. A detector circuit is designed to check this similarity and generate the output status. The decision to adjust phase alignment (by shifting left or shifting right) is based on majority vote of all output status. Once phase are properly adjusted the middle bit of each word is representing the input data.

Note that both methods averages phase information over a certain period of time by tally numbers of transition in the first method or using majority vote in the second method. This reduces chances of making wrong decisions i.e. pick wrong bits because of instantaneous phase error such as jitter and high frequency noises. The more phase information is collected the more reliable the decision is. However it comes with the expense of extra hardware. The hardware needed to implement processing block are essentially digital logic blocks such as registers, multiplexers, adders and accumulators. Additionally, digital processing can add latency to the system.

### 2.4.2 Characteristics

There are some important characteristics of oversampling clock recovery that are completely different from other techniques. First, it suffers from inherit phase quantization error. Considering the input data have a small phase shift resulting from timing jitter or frequency variation that is less than the time interval between the sampling clock (sampling resolution). The oversampling data will be the same. Therefore the system will not respond to any phase shift that is smaller than the sampling resolution. Importantly, in band-limited channel signal has a finite slew rate, signal amplitude is lower as it is farther from center of eye diagram. Therefore sampling with phase error reduces signal-noise-ratio. This can result in increasing bit error rate if the sampling resolution is a large portion of bit time. Increasing the
oversampling ratio reduces the quantization error but increases hardware, chip area and power.

Second significant feature is the ability to use non-causal algorithm to recover clock and data. The decision to select data bits out of a current set of oversampling can be based on phase information from sets of oversampling data before the current set as well as after the current set. This is the feature that PLL clock recovery does not have. Because of more information available, non-causal algorithms usually give better performance than causal algorithms.

The final feature is the timing recovery does not have to be a part of control loop as in PLL clock recovery. Therefore it does not have restrictions regarding to stability such as loop delay and loop bandwidth.

2.5 Conclusion

CDRs can be classified in to two groups; the phase synchronization or the PLL-based CDR and the oversampling data recovery. Within the groups, there are several architectures and implementation techniques which have their owns advantages and disadvantages. It is hard to make a fair comparison between each technique. Some techniques may be better for certain applications than other techniques depending on factors such as signal condition, type of links. Following are only comparatively summary in particular issues.

1. Data Recovery

PLL-based CDR responds to input data differently depending on the input jitter frequency. Data with low frequency jitter within the PLL bandwidth will be tracked accordingly. Thus it minimizes phase error and samples at the optimal point. With high frequency jitter outside the PLL bandwidth, it is not able to track. In contrast, oversampling recovery can respond to
both low-frequency jitter and high-frequency jitter but the amount of jitter must be greater than its quantization error. The PLL-based CDR is able to track frequency drift of received data, the capability that is not available in oversampling techniques. In oversampling if frequency continually drifts long enough, it will recover extra bits or miss some bits of data (overrun and underrun).

Both PLL-based CDR and oversampling can be subject to static phase error. Causes of this error in PLL come from a non-ideality of the circuit such as a finite set up time of PD and a mismatching in the charge pump current, which depends on how well the circuits are designed. In oversampling, it is a result of phase quantization error, which is inherent.

2. Speed

In phase synchronization CDRs, although speed (bit rate) is improved by using multi-phase parallel sampling, it does not increase linearly with number of phase. For example using 5:1 demultiplexing actually improves speed less than five times of the maximum speed achieved with serial recovery in the same process technology.

For oversampling as the data rate increases and bit time reduces, it requires a higher sampling resolution. A high frequency and fine multiphase clock generator and well-controlled sampling clock are the obstructions to overcome. However, this can be avoided by using the algorithm that allows the minimum oversampling ratio (3x) with the expense of a higher signal-to-noise ratio required and a maximum phase quantization error, one sixth of the bit-time.

3. Power Consumption and Chip Area

Typically a PLL-based CDR occupies less area and consumes less power than a oversampling CDR. Therefore, in applications that require only one link, it has this
advantage over the oversampling. However, in multi-link applications, several units of oversampling CDR can share common circuits such as a multiphase clock generator. As a result, it may have power and area advantage over PLL-based CDR for large number of links in one chip.

A following table summarizes works reported in recent years. It lists the works according to techniques used. Noting that measured BER and jitters should not be compared directly because of its difference in the testing setup. Additionally, in several works amount of power consumption reported are only for the core PLL excluding the buffer circuits and the off-chip drivers. Thus this table only provides a rough idea about performances numerically.
<table>
<thead>
<tr>
<th>Author</th>
<th>Technique</th>
<th>Technology</th>
<th>Speed</th>
<th>BER</th>
<th>Jitter</th>
<th>Power/Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rau [12]</td>
<td>PLL-CDR</td>
<td>CMOS</td>
<td>1 Gb/s</td>
<td>&lt;10⁻¹¹</td>
<td>N/A</td>
<td>911mW, 3.3 V, 0.38 mm²</td>
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<tr>
<td>Soda [48]</td>
<td>PLL-CDR</td>
<td>Si-bipolar</td>
<td>2.5Gb/s</td>
<td>N/A</td>
<td>N/A</td>
<td>450 mW, 3.3V, N/A</td>
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<td>Djahanshahi</td>
<td>PLL-CDR</td>
<td>0.35µ CMOS</td>
<td>622Mb/s</td>
<td>N/A</td>
<td>12.5ps rms (0.0117 UI)</td>
<td>200 mW, 0.84x0.7 mm²</td>
</tr>
<tr>
<td>Greshishchev</td>
<td>PLL-CDR</td>
<td>SiGe</td>
<td>10Gb/s</td>
<td>&lt;10⁻⁹</td>
<td>0.8ps rms</td>
<td>4.5W, -5 V, 4.5x4.5 mm²</td>
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<td>Ramezani [13]</td>
<td>PLL-CDR 4-level bang-bang</td>
<td>CMOS</td>
<td>5Gb/s</td>
<td>N/A</td>
<td>4.8ps rms</td>
<td>80mW, 1.8V, 0.64x0.67 mm²</td>
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<tr>
<td>Scheytt [20]</td>
<td>PLL-CDR</td>
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<td>0.155,0.622</td>
<td>N/A</td>
<td>3.8ps rms @ 2.488 G</td>
<td>680mW, -5V, N/A</td>
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<td>Iravani [38]</td>
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<td>0.35µ CMOS</td>
<td>1.25Gb/s</td>
<td>&lt;10⁻¹⁴</td>
<td>0.6 UI</td>
<td>150mW, 3-3.6V, N/A</td>
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<td>Farjad-Rad [10]</td>
<td>PLL-CDR</td>
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<td>8Gb/s 4-PAM</td>
<td>10⁻⁷</td>
<td>4ps rms, 28ps p-p</td>
<td>Tx and Rx, 1.1W, 3 V, 2x2 mm²</td>
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<td>Butala [8]</td>
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<td>2.5Gb/s</td>
<td>N/A</td>
<td>10.8ps rms</td>
<td>33.5mW, 3.3V, 0.8x0.4 mm²</td>
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<tr>
<td>Savoj [7]</td>
<td>PLL-CDR</td>
<td>0.18µ CMOS</td>
<td>10Gb/s</td>
<td>1.2x10⁻⁷</td>
<td>1ps rms</td>
<td>72mW, 2.5V, 1.1x0.9 mm²</td>
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<td>Butala [50]</td>
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<td>Savoj [51]</td>
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<td>10Gb/s</td>
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<td>Larsson [28]</td>
<td>PLL-CDR feedback phase selection</td>
<td>CMOS</td>
<td>0.002-1.6 Gb/s</td>
<td>N/A</td>
<td>8.5ps rms</td>
<td>18 mW @ 250 MHz, 0.9-2.5 V, 0.3x0.12 mm²</td>
</tr>
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Table 2.1 Summary of CDR performance reported in literatures
## Table 2.1 (continued)

<table>
<thead>
<tr>
<th>Author</th>
<th>Technique</th>
<th>Technology</th>
<th>Speed</th>
<th>BER</th>
<th>Jitter</th>
<th>Power/Area</th>
</tr>
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<tbody>
<tr>
<td>Lee [52]</td>
<td>4x</td>
<td>1.2μ CMOS</td>
<td>500Mb/s</td>
<td>&lt;10^-9</td>
<td>N/A</td>
<td>Rx and Tx 0.97W, 5V</td>
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<td>JSSC 95</td>
<td>Oversampling</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.06x3.06 mm²</td>
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<tr>
<td>Kim [53]</td>
<td>3x</td>
<td>0.6μ CMOS</td>
<td>800Mb/s</td>
<td>&lt;10^-12</td>
<td>N/A</td>
<td>750 mW N/A</td>
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<tr>
<td>CICC 95</td>
<td>Oversampling</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Kang [35]</td>
<td>16x</td>
<td>1.2μ CMOS</td>
<td>417Mb/s</td>
<td>N/A</td>
<td>120ps p-p</td>
<td>800 mW, 4.5 V 0.435x0.669 mm²</td>
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<tr>
<td>CICC 96</td>
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<td>625Mb/s</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Kim [54]</td>
<td>3x</td>
<td>0.6μ CMOS</td>
<td>960Mb/s</td>
<td>N/A</td>
<td>150ps p-p</td>
<td>700mW</td>
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<td>Symp 96</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Yang [34]</td>
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<td>2.5Gb/s</td>
<td>N/A</td>
<td>N/A</td>
<td>1W, 4.4 – 5.5 V 3x3 mm²</td>
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<td>Oversampling</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Yang [46]</td>
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<td>4Gb/s</td>
<td>&lt;10^-9</td>
<td>N/A</td>
<td>350mA 2.7-4 V N/A</td>
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<td></td>
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<td>622 Mb/s</td>
<td>N/A</td>
<td>46ps rms</td>
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</tr>
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<td>10:1</td>
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<td>Fiedler [31]</td>
<td>Parallel sampling</td>
<td>0.5μ CMOS</td>
<td>1.0625 Gb/s</td>
<td>&lt;10^-14</td>
<td>27ps rms</td>
<td>Rx and Tx 450mW,3.1-3.5V</td>
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<td>10:1</td>
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<td></td>
<td></td>
<td></td>
<td>4 mm²</td>
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<td>Chen [55]</td>
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<td>5:1</td>
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<td>Gu [32]</td>
<td>Parallel sampling</td>
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<td>0.5-3.5 Gb/s</td>
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<td>250mW (both Rx and Tx) 1 mm²</td>
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<td>10:1</td>
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</table>
2.6 References


Chapter 3

Proposed System

3.1 Introduction

Conventional serial clock and data recovery (CDR) circuits are implemented by using a phase-locked loop (PLL) to lock the local oscillator to the embedded clock of incoming non-return to zero (NRZ) data. This serial CDR technique can regenerate the data clock for applications where it is needed, but requires the phase detector, charge-pump, and oscillator to operate at frequencies as high as the data rate. Parallel data recovery techniques can reduce this speed requirement on the circuit building blocks while providing the data demultiplexing that is usually needed.

The parallel data recovery techniques use multi-phase clocks tapped from the local ring oscillator to sample several consecutive NRZ data bits in parallel. The parallel structure relaxes speed requirements on the circuits. There are two techniques based on this architecture, oversampling data recovery [1,2,3,4] and phase tracking data recovery [5,6,7,8].

Oversampling data recovery does not require the local oscillator to have phase synchronization with the data, and thus is susceptible to phase quantization error. In order to extract phase information, it must oversample the input at a minimum of three times the data rate (3x). A higher oversampling ratio reduces phase quantization error. As a result, it increases signal-to-noise ratio (SNR) [3]. However, the larger number of sampling circuits adversely increases the input capacitance and limits the data bandwidth. Also, the larger number of samples complicates processing and increases chip area and power consumption. In addition, because of lacking phase synchronization between input data and local oscillator, the local oscillator will not adjust its frequency to track the frequency of the input data.
Therefore in the occurrence of continuous input frequency drifting it results in either the extra bits or missing bits [9].

Phase tracking data recovery uses a multi-phase PLL to maintain phase relationship between the input data and the local oscillator. The phase detector in a multi-phase PLL is essentially an array of digital samplers. These samplers operate in time-interleave manner yielding the sampling rate two times the data rate (2x). For example, in the phase-locked condition if the phase detector consists of sixteen samplers, eight of them will align with the data transition and the others will sample at the center of the data eye alternately covering for eight bit-times. The phase error is determined from these samples by comparing the sample at data transition with its adjacent samples. Because all the samples are digital, the phase error signal only indicates that phase of the local clock is leading or lagging the data transition. As a result the PLL adjust itself by generating either positive or negative constant correcting signal to correct the error. There are two problems inherent with this 2x phase detection scheme. First, the PLL forces the sampler to sample at a time that might create a meta-stable state in a normal digital circuit. Secondly, because the loop-correcting signal is not linearly proportional to the amount of phase error, the PLL behave as a non-linear control system known as “bang-bang” loop control. This discontinuous non-linearity frequently causes undesirable behaviors such as an instability or limit cycle (oscillation) if its effect does not properly compensated for.

The PLL that can be modeled with a linear control loop is desirable not only to avoid the non-linearity effects but to gain benefits of using the familiar and powerful linear system analysis as well. In order to achieve that, the phase detector and charge pump of the PLL must generate the oscillator control signal that is linearly proportional to the amount of phase error. Standard charge pump circuits use switches to steer constant current sources. The amount of charge transferred to the loop filter is controlled by the duration that the switch is on. This duration or the on-time is controlled by the width of UP/DN pulses that is proportional to phase error. Since the pulse width varies following on the phase error, it
introduces additional frequency spectrum into the VCO control signal translated into spurious around VCO frequency spectrum. Moreover, as the data rate increases, the on-time of the same amount of phase error becomes smaller. As a result, the non-idealities of the circuits and the switches such as the non-zero settling time, the switch on/off delay make it more difficult in both creating the precise UP/DN pulses and controlling the switches.

In this proposal, we propose using a multi-phase PLL that can be modeled as a linear control system to overcome the drawbacks mentioned above. It maintains the advantages of phase tracking while reducing the speed requirements on the phase detector and charge-pump circuits. To avoid the discontinuous non-linearity, a new phase detection scheme is employed. The scheme incorporating a new data phase detector and a new charge-pump circuit results in a control loop that can be analyzed using the linear system analysis. The data phase detector uses both digital and analog samplers. While the digital samplers recover data bits in parallel, the analog samplers detect the level of input data at the transitions and generate the output voltage signals proportional to the phase error. These outputs then summed by the charge pump circuit, which is a transconductance amplifier. Instead of producing constant magnitude current pulse and varying its width, the charge pump produces a constant width current pulse with amplitude proportional to phase error. Because its width is constant, it can be defined long enough to alleviate the effect of the circuit non-idealities and relax the circuit speed requirement. Moreover, because the input data stream is immediately demultiplexed and recovered by the digital samplers, the scheme thus combines the timing recovery and data recovery within one unit so that area and power consumption is reduced.
3.2 Proposed System

3.2.1 A Multi-Phase PLL Data Recovery Circuit

The top-level structure of the proposed data recovery circuit is shown in Figure 3.1. It is a data loop / reference loop architecture. The reference loop is a standard PLL using a phase frequency detector (PFD) and a charge pump circuit (CP). The data loop is a multi-phase PLL using the phase detector and charge pump array. Both loops share a VCO and a loop filter (LPF). The VCO is an eight-stage differential ring oscillator providing sixteen uniformly spacing clock phases. One of the clock phases and a local clock (Ref) are the inputs of PFD of the reference loop. The local clock can be externally applied or derived from the system the CDR interfacing with. At the data loop the input NRZ data is applied to the phase detector array using the sampling clock generated from sixteen clock phases tapped from the VCO.

The objective of the reference loop is to bring the VCO from its free running frequency to the frequency close to one eighth of the data rate in a very short time. Then the data loop takes over to recover clock and data. Consequently, the operation of the circuit can be divided into two steps, the frequency acquisition and the phase acquisition. The first step is the frequency acquisition process. After the power on, only the frequency loop is active. Ref signal that has frequency approximately one eighth of the input NRZ is applied to the PFD. The reference loop thus tunes the VCO to lock to Ref. After it is locked, the controller deactivates the reference loop by turning off its charge pump circuit and simultaneously activates the data loop. Because the VCO frequency is now in the proximity of the one eighth of the data rate, its sixteen clock phases are separated by approximately a half of a bit-time. Once the data loop is active, the circuit enters the second step, the phase acquisition process. All sixteen clock phases are sampling the input data resulting in two samples per bit time, thus covering for eight bits long. Initially, there will be the phase offset between the clock phases and the
input data. The data loop therefore by using the data phase detection scheme that we will explain in the next section adjusts the VCO frequency until the phase locked is established. At the phase-locked state, the analog samplers sample at the data transition while the digital samplers sample at the center of the data bit. The time-interleaved outputs of the digital sample are then synchronized to be eight-bit wide recovered data ($d_0 - d_7$) by the data aligner.

Figure 3.1 The proposed system and the block diagram of the multi-phase PLL data recovery circuit
It is important to note that the on-chip operation frequency is the VCO frequency, which is much slower than the data rate due to its parallelism. In this design we use 8:1 demultiplexing ratio. The ratio or degree of parallelism is select based on trade-offs among following factors; (i) the circuit bandwidth supported by its process technology, (ii) the target data rate and (iii) the effective input capacitance of the circuit. The greater ratio can cover higher the data rate but in the same time it requires more number of stage in ring oscillator, which can slow down oscillation frequency. It also increases number of sampler in the PD array resulting in increasing the input capacitance of the circuit that can limit the maximum data rate.

### 3.2.2 Timing Recovery

![Data phase detector](image)

**Figure 3.2 Data phase detector**
The key building blocks are the data phase detector and the charge pump. As shown in Figure 3.2, eight digital samplers (D1-D8) and eight analog samplers (A1-A8) are placed alternately to form the phase detector. There are eight charge-pumps connected to the phase detector. Each sampler is controlled by each clock phase tapped from VCO so that eight bits of input data are sampled in parallel sixteen times (equivalent to 2x oversampling). When the phase is locked, the digital samplers latch the data at the center of the data eye and the analog samplers are timed to the data transitions determined by the crossing point of the differential inputs as shown in Figure 3.3.

Figure 3.3 Timing of data phase detector in the lock state

Figure 3.4 Phase detection technique
To understand how the data phase detector extract phase information considering a scenario in Figure 3.4 where the VCO is already tuned to one eighth of the data rate but has some phase offset, $\Delta \phi$, relative to the data transition. The digital samples ($d_1$, $d_1b$) and ($d_2$, $d_2b$) indicate that the input data change from low to high. The differential signal ($a_1-a_1b$) from the analog sampler is negative. Having negative analog sample while data changing from low to high means clk2 is sampling ahead of the crossing point. Thus the VCO is leading. As the phase error between data crossing point and clk2 increases, the magnitude $\Delta v = |a_1-a_1b|$ increases monotonically. Consequently, to a first order approximation, as long as the analog sampler sample during the transition (slope) of the input data the phase error is proportional to the magnitude of the analog sample. Conclusively, digital samples and polarity of analog samples tell if clk is leading or lagging while the magnitude $\Delta v$ reflects amount of phase error.

The differential voltage of analog samples and the transition information (low-to-high, high-to-low and no-transition) from the digital sampler are applied to the charge-pump circuits (CP1-CP8). Each charge-pump circuit, which is a transconductance amplifier or V-to-I circuit, then generates an output current where its amplitude is linearly proportional to the magnitude $\Delta v$, thereby proportional to phase error and its directions (pump-up/pump-down/no-pump) is accordant to the phase positions (lagging/leading/in-phase) to correct the loop. Since the correcting signal is linearly proportional to the error signal therefore, this phase detection technique allows the loop to be modeled and analyzed as a linear control system.

As it is described, the objective of this technique is to bring in the linearity to the timing recovery. However the assumption of linear control loop is valid under certain conditions. First, the proportionality of the magnitude $\Delta v$ to the phase error is valid only within the slope region. Thus it reduces the effective rage of the phase detector to be less than $(-\pi, \pi)$. How wide the effective range will be is depending on the signal condition of the NRZ data. Assuming the transition time at the high data rate can be any value between one third to one
half of the bit-time, hence the effective range will be \((-\pi/3, \pi/3)\) to \((-\pi, \pi)\). Therefore in system level design, it needs to take into account the variation of this range. Secondly, the differential voltage \(\Delta v\) must be within the linear operation range of the transconductance amplifier. This constrain can be accommodated by the proper circuit design.

Output currents from eight charge-pump circuits are summed and integrated by the loop filter. Moreover, because the eight charge-pumps operate in a time-interleaved manner, and the phase error is encoded in the current amplitudes rather than pulse widths, the operation of each charge pump can extend over more than one bit-time as shown in Figure 3.5. This characteristic significantly reduces the speed requirements on the charge pump circuits.

![Figure 3.5 Charge-pump current pulses](image)

**3.2.3 Data Recovery**

Data recovery is performed simultaneously with the timing recovery. The incoming data that are demultiplexed by the digital sampler D1-D8, are retimed by a data aligner circuit. As shown in Figure 3.6, the circuit is essentially a set of four-bit wide and eight-bit wide latches
clocked by two of clock phases separated by a half of a period to deskew the samples. The recovered data are eight-bit parallel (d0-d7) and synchronize with that clock.

![Data aligner](image)

**Figure 3.6 Data aligner**

### 3.2.4 Reference Loop

The function of the reference loop is to tune VCO frequency to the one eighth of the targeted data rate as fast as possible to reduce the acquisition time of the CDR. We propose to use a standard charge pump PLL with a PFD. This is because the PFD can detect both phase and frequency difference simultaneously. As a result, it has a fast acquisition and a wide capture range. Furthermore the circuit is fairly small and simple. Since the VCO frequency is rather slow, there is no need for a frequency divider in the feedback loop. The loop filter is shared with the data loop to save the chip area.

The reference loop is design to active only during the start-up and deactivates itself after the VCO frequency is locked for several reasons. Firstly, for most applications of serial link (backplane and cable) after links are established they are continuously maintained until the systems are powered down. In other applications such as optical channels, the idle pattern is sent when there is no data being transferred to keep the synchronization. Therefore, the acquisition process happens only one time at the beginning. Additionally, communication
channels are regulated by their standards that allow a certain frequency variation. This frequency variation can be compensated by tracking ability of the data loop. Thus, it is unlikely that the data loop will lose its lock. Secondly, since only one loop is active; it eliminates chance of interference between loops. Furthermore, the deactivated reference loop reduces some of its consumed power.

Noting that because of sharing the VCO and the loop filter with the data loop, the component values of the loop filter (R, Cs and Cp) are calculated based on the optimization of the data loop. The reference loop is then optimized through other loop parameters such as its charge-pump gain based on those component values.

3.2.5 Controller

The controller is responsible for providing signals to deactivate reference loop after it locked and activate the data loop. The simple way to implement is using RC timer that has a time constant longer than the acquisition time of the reference loop. Thus, the timer expires after reference loop is locked causing control signals to be generated and allows the data loop to take over. Although it is simple, the timer be too long than it supposes to be.

Alternatively, a lock detector can be implemented within the reference loop. The locked state of the reference loop can be observed through the VCO control signal (Vcon). During the acquisition state, Vcon displays the ripple or beat note with frequency equal to the frequency difference of Ref and VCO. As the loop approaches a locked state, the frequency difference becomes smaller, the ripple amplitude is reduced and Vcon becomes a DC like signal. Once this change is detected the lock signal can be generated. This approach however usually requires the complex analog circuits to monitor the frequency of the signal [10].
We propose a digital way for efficiency and simplicity. It uses a logic circuit that detects the lock condition of the reference loop by processing UP and DN signals of the charge pump. Once UP and DN are matched, it creates a signal to disable the charge-pump of the reference loop and enable the charge-pump of the data loop.

### 3.2.6 Adaptive Loop Bandwidth Capability

Because the propose architecture composes of multiple phase detectors and charge pumps that can be controlled individually, it allows us to experiment the loop operation with different number of active phase detector. The number of active phase detector and charge-pump is corresponding to the sampling rate of the PLL. When all the phase detectors are active, the PLL has its highest sampling rate. The higher sampling rate increases the phase detector gain and so the loop gain. As a result, it affects the loop bandwidth and noise performance of the PLL. Therefore multi-phase PLL gives an opportunity to study the effect of sampling rate to the system performance. We expect that by changing number of active phase detector, it is possible to alter loop parameters in order to optimize it performance for difference purposes.

### 3.3 Preliminary Work

To support the proposed ideal and verify its feasibility, we have been investigated and developed in both the theoretical and the technical works. We first develop the system model for the multi-phase PLL. Then based on that system model, the effect the non-linear operation of the bang-bang PD has been studied. The study reveals the trade-off for optimization the bang-bang type CDR and predicts its output phase noise contribution. Finally the circuit of the proposed system were designed and fabricated. The chip is now under testing.
3.3.1 System Modeling of Multi-Phase PLL

The system level modeling is necessary. It can be used to characterize and predict system behavior as well as verify with circuit level simulation. Since the reference loop has been well studied we will focus on modeling the data loop. Under the condition that the phase error is small so that the analog sampler is sampling on the slope of the bit boundary near the data crossing point, we can modeled the data loop with the linear control system and apply linear system analysis. Conventionally, PLLs are modeled in continuous-time system (s-domain). However, since the data loop is a time-interleaved sampling, it is more suitable to model in discrete-time system (z-domain). Moreover, z-domain has an advantage over s-domain in providing specific information about system stability condition. Nevertheless, we model the system in both s-domain and z-domain, and then compare the results if they are accordant. We first find the gain and the transfer characteristic of the phase detector/charge-pump then develop a linear model and represent it in term of a standard PLL parameters.

Continuous-time Model of Multi-Phase PLL

Considering the waveform at the input of one of eight analog samplings in Figure 3.7. The NRZ data has its bit-time equal to T, which is the period of its data clock. The VCO frequency is already one eighth of data rate but there is small phase offset existing. The loop tries to align one of its eight VCO phases, \( \phi_m \) at \( t_v \) to the data crossing point at \( t_r \). Similar to standard PLL analysis, we can use \( t_r \) as a reference position and consider the embedded data clock as a reference signal to which the loop tries to lock.
Figure 3.7 Phase detector gain calculation

Let $\omega_i = $ reference frequency $= 2\pi/T \text{ rad/sec}$

$\omega_o = $ VCO frequency $= \omega_i/N \text{ rad/sec}$, in this case $N = 8$

$\theta_i(t)$ = input phase: the accumulative phase of the data clock at time $t$

$\theta_o(t)$ = output phase: the accumulative phase of the VCO at time $t$

$\theta_e(t) = \theta_i(t) - \theta_o(t) = $ phase error

We can express the time difference $\Delta t = |t_v - t_r|$ in term of the phase that the data clock gains between $t_r$ and $t_v$:

$$\Delta t = \frac{|\Delta \theta_i|}{\omega_i} = \frac{\theta_i(t_v) - \theta_i(t_r)}{\omega_i}$$

Since we assume that the frequency is locked i.e. $\omega_i = N\omega_o$ we can express $\Delta t$ in term of the instantaneous phase difference between input phase and output phase at time $t_v$, hence
\[
\Delta t = \frac{\theta_1(t_v)}{\omega_i} - \frac{\theta_o(t_v)}{\omega_o}
\]
\[
= \frac{\theta_1(t_v)}{\omega_i} - \frac{N\theta_o(t_v)}{\omega_i}
\]
\[
= \frac{\theta_1(t_v) - N\theta_o(t_v)}{\omega_i}
\]
\[
= \frac{\theta_1(t_v) - N\theta_o(t_v)}{\omega_i}
\]

(1)

Because it references to the same frequency \(\omega_i\), \(\theta_1(t_v) - N\theta_o(t_v)\) is equivalent to \(\theta_c(t_v)\), the phase error at \(t_v\) in standard PLL analysis, therefore at any \(t\)

\[
\theta_c(t) = \theta_1(t) - N\theta_o(t)
\]

(2)

Assuming that rise time and fall time of NRZ are approximately linear and last for \(L\) second from the data crossing point until reaching its amplitude \(A\). Thus the differential voltage \(\Delta v\) is equal to \((A/L)\Delta t\). Let \(g_m\) is the transconductance of the charge-pump circuit. We can express the current pumped to the loop filter \(I_o\) from each charge-pump circuit as

\[
I_o = g_m \Delta v
\]
\[
= g_m \frac{A}{L} \Delta t
\]

Substituting (1) for \(\Delta t\).

\[
I_o = g_m \frac{A}{L} \left(\frac{\theta_1}{\omega_i} - \frac{N\theta_o}{\omega_i}\right)
\]
\[
= g_m \frac{A}{L} \frac{\theta_1 - N\theta_o}{2\pi} T
\]
\[
= g_m \frac{A}{2\pi L} (\theta_1 - N\theta_o)
\]
\[
= K_d \theta_c
\]

where \(K_d = g_m \frac{A}{2\pi L}\) is the phase detector/charge-pump gain. It relates the average loop correcting signal to the input error within a period of data clock. Noting that the gain is a
function of both amplitude and transition time of the input. The transfer characteristic is shown in Figure 3.8. Depending on the transition time, the proportional range can be less than $\pi$ radian.

Until now we have considered that all $N$ phase detectors are active and the input data has transition every clock period. To accounting for transition density, the phase detector gain will be multiply by an average transition density factor $\delta$, where $0<\delta<1$.

Before considering not all of phase detectors are active. We first need to relate the functional blocks of multi-phase PLL to that of standard PLL. Since its VCO runs at speed $N$ times slower than standard PLL, assuming the same range of control voltage, its VCO gain will be $K'_o = K_o/N$ where $K'_o$ is the VCO gain of standard PLL. When only $M$ of phase detector where $M \leq N$ are active, it is equivalent to multiply the phase detector by factor $M/N$. Therefore the block diagram of its continuous-time model can be drawn as in Figure 3.9. A $N$ block on the feedback path, in contrast with $\pm N$ usually seen in PLL frequency multiplier, corresponds to phase error expression in Eq.(2).
Figure 3.9 Continuous-time system block diagram

We obtain the following closed-loop transfer function:

\[
\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{M}{N} K_d F(s) \frac{K_o'}{s}}{1 + MK_d F(s) \frac{K_o'}{s}}
\]

Substituting \(F(s) = \frac{1}{sC}\) for a simple loop filter, results in a second order system

\[
\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{M}{N} K_d F(s) \frac{K_o}{Ns}}{1 + MK_d F(s) \frac{K_o}{Ns}}
\]

Comparing equation (2) to that of a standard PLL where \(M = N = 1\), we can conclude as following:

(i) Multi-phase PLL scales down the output phase by factor of \(1/N\)
(ii) $\zeta, \omega_n$ of multi-phase PLL are the $\zeta, \omega_n$ of regular PLL multiplied by factor of $\sqrt{M/N}$

(iii) Bandwidth of multi-phase PLL is also modified following the change of $\zeta$ and $\omega_n$

From this analysis, it shows that multi-phase PLL gives an option to change loop parameters through the number of active phase detectors, $M$, being used.

**Discrete-time Model of Multi-Phase PLL**

In this section we model the multi-phase PLL as a discrete-time system by applying impulse invariance transformation [11,12] to its continuous-time block diagram. However, the more accurate model and analysis using zero-order hold and including the delay due to the sampling and data processing is also given in the Appendix A. The data phase detector is modeled as a switch with a sampling period $T_s$ and a conversion gain $K_p$. $T_s$ is determined from the number of active phase detector $M$ and the transition density factor $\delta$. $T_s$ must be constant and $M$ cannot be arbitrary as in continuous time model. For $N = 8$, the possible $M$ that gives a constant $T_s$ are 1,2,4 and 8. Suppose there are $M$ phase detectors sampling in sequence in one VCO period $T$, therefore

$$T_s = \frac{T}{\delta M} = \frac{1}{\delta M f_0} = \frac{N}{\delta M f_i}$$

where $f_i$ and $f_o$ are input data frequency and VCO frequency in Hz respectively. $K_p$ is equal to $K_d/f_i$. The s-domain function of loop filter and VCO are transformed to $G(z)$ by mapping through $z = e^{ST_s}$. The block diagram is shown in Figure 3.10 and $G(z)$ is expressed as
Figure 3.10 Discrete-time block diagram

\[ G(z) = \frac{K_p' R z}{z - 1} + \frac{(K_p'/C)T_z z}{(z - 1)^2} \]

Hence the closed-loop transfer function is

\[ H_d(z) = \frac{K_p G(z)}{1 + K_p G(z)N} \]

\[ H_d(z) = \frac{Kz - (K\alpha)z}{(NK + 1)z^2 - (NK\alpha + 2)z + 1} \]  \( (5) \)

where \( K = K_p K_o' R \) and \( \alpha = 1 - \frac{T_s}{RC} \).

Eq.(5) can be used to characterize system in term of stability, transient and steady state response as well as frequency response. For the stability condition, the closed-loop poles must stay inside the unit circle. Using z-domain root locus, it reveals that the system will be stable if \( T_s \leq 2RC \). In practice, RC is a time constant of the loop filter which is much greater that \( T_s \).

The frequency response of s-domain and z-domain of a multi-phase PLL with different numbers of phase detector (1, 4 and 8) comparing to the standard PLL with the same loop components that has critical damp are shown in Figure 3.11. As expected, the loop
bandwidth decreases as the number of phase detector reduces. For the case of M = 8, the response is the same as standard PLL except the magnitude is scaled down by 1/8 because of the slower VCO.

The step response and ramp response representing the responses of the PLL to the input phase shifting and frequency shifting respectively are shown in Figure 3.12. In both case, for M = 8, its response are the same as the standard PLL which is designed to be critically damped. As the number of M reduces to 4 and 1, the open loop gain reduces and its response is more underdamped.

In summary, controlling the number of active phase detector provides another mean to control the loop dynamic of the PLL without changing the loop filter.

3.3.2 Analysis of Phase Noise Due to the Non-Linear Operation of the Bang-Bang PD

As mentioned earlier, the CDR with conventional 2x phase detection scheme suffers from the non-linearity due to its bang-bang operation. In this section the effect of this non-linearity to the noise performance of the CDR is analyzed.

The non-linearity originates from the operation of its phase detector. For simplicity of the analysis, we will consider the case of the single phase detector instead of multiple phase detector in parallel since the result is applicable for both cases. The transfer characteristic between input phase error and charge-pump is shown in Figure 3.13 for both types of phase detector. While the transfer characteristic of bang-bang PD is a step, the transfer characteristic of a linear type is a straight line with slope $K_d$.
Figure 3.11 Frequency response of multi-phase PLL (a) s-domain (b) z-domain
Figure 3.12 Unit step response and ramp response of z-domain
According to its operation, the bang-bang type PD behaves as a two level phase quantizer. In this scenario, input to the quantizer is the phase difference between the data crossing point and the clock edge in the range \((-\pi, \pi)\) and the outputs are positive and negative charge-pump currents, \(\pm I_o\). Thus the level spacing of the quantizer \(\Delta\) is \(2I_o\). We further characterize this quantizer by comparison its response to that of the linear PD. The difference between their charge-pump currents is the quantization error and it is defined as

\[
e_N = I_Q(\phi) - K_d(\phi)
\]

(4)

\[
e_N = I_Q(\phi) - K_d \cdot \phi
\]

(5)
where \( I_Q \) is charge-pump current of bang-bang PD

\[
I_Q = -I_o \quad \text{when} \quad -\pi < \phi < 0 \quad \text{and} \quad I_o \quad \text{when} \quad 0 < \phi < \pi
\]

\( I_L \) is charge-pump current of linear PD

The \( K_d \) is selected to be \( 2I_o/\pi \) in order to confine the quantization error \( e_N \) within \( \pm \Delta/2 \) or \([-I_o, I_o] \).

Following Eq.(7) we can model a bang-bang PD as a linear PD with an additive quantization error \( e_N \) as shown in Figure 3.14

**Figure 3.14 Linearized model of bang-bang type PD**

### 3.3.3 Approximation of the Quantization Error

Consider the operation of the PD. It samples the input phase difference and generates the input sequence to the loop. If we assume that the input phase difference changes randomly between sample to sample due to random nature of NRZ and random jitter from the communication channel, then the input sequence is a random sequence and the quantization error can be modeled as a random variable uniformly distributed within \( \pm \Delta/2 \) or \([-I_o, I_o] \). We further assume that it is uncorrelated with the input phase and its spectral density is white. However, once the PD placed inside the loop, its distribution depends on the response of the loop. Consider when the clock frequency is in the proximity of the data rate but there is some phase error. To minimize phase error the bang-bang operation causes the clock edge to move back and forth around the data transition. It usually takes several clock cycles for the phase
error to change from lead to lag and vices versa. Thus most of the time clock edge appears close to data transition resulting in small input phase error but large quantization error. As a result, distribution of $e_N$ is no longer uniform, indeed the probability of large $e_N$ is higher than that of small $e_N$. Therefore it is closer to model with a beta distribution in the interval $[-I_o, I_o]$ with $0<\alpha=\beta<1$ and zero mean as shown in In fact, uniform distribution is a special case of beta distribution with parameter $\alpha=\beta=1$.

![Beta Distribution](image)

**Figure 3.15 Random variable $e_N$ modeled with beta distribution**

**Discrete Time Model of CDR with a Bang-Bang PD**

Using the model developed in previous section, we can build the equivalent linear CDR of the bang-bang CDR and use linear system technique to analyze.

The functional block diagram of a CDR using bang-bang PD is shown in Figure 3.16. Although the phase error is sampled every clock cycle, it is available only when the transition occurs. Hence the effective sampling rate is $f_s=d\cdot f_{vco} = 1/T_s$, where $d$ is the transition density and $f_{vco}$ is VCO frequency. The loop integrator is a simple RC filter, thus $F(s) = R+1/sC$. $K_v$ is a VCO gain. Note that $e_N$ is present as an additive current noise to the integrator. Since we are interested only in the noise contributing from PD we omit noises from other noise sources. Because of its sampling operation, the loop is analyzed with discrete time model as
in previous section. As a result, PD gain is scaled down to be \( K_p = K_d / f_{vco} \) and the s-domain block is transformed to z-domain \( H(z) \) as in the following expression

\[
H(z) = R K_o \frac{z(z - \gamma)}{(z - 1)^2}
\]

where \( \gamma = 1 - (T_s/RC) \).

The PLL has two inputs, a input phase \( \phi_i(t) \) from NRZ and an additive current noise \( e_N \) from the PD. As we assume that they are uncorrelated, we can apply the linear system analysis. By setting \( e_N \) to zero, the transfer function from \( \phi_i \) to \( \phi_o \) can be computed as

\[
H_s(z) = \frac{\phi_o}{\phi_i} = \frac{K_p H(z)}{1 + K_p H(z)}
\]

Similarly, setting \( \phi_i \) to zero, we have the noise transfer function as

\[
H_n(z) = \frac{\phi_o}{E_n} = \frac{H(z)}{1 + K_p H(z)}
\]
Note that $H_n(z)$ has an unit of rad/A and $H_n(z) = H_d(z)/K_p$. This implies that, excluded the factor $K_p$, the PD noise spectrum will be shaped by the same characteristic low-pass transfer function of the linearized PLL when it appears at the output. Therefore, similar to input phase noise, it can reduced by designing PLL with a small loop bandwidth.

Since the response of loop to the input CDR is a well-known standard PLL response we will focus on analysis the response of the loop to the PD noise. The output spectral density of PD noise $S_{no}(f)$ can be calculated from

$$S_{no}(f) = S_n(f)|H_n(f)|^2$$

where $S_n(f)$ is its input spectral density and $H_n(f)$ is the $H_n(z)$ evaluated with $z = \exp(j2\pi f/f_s)$. The input spectrum is determined by the statistical properties of $e_N$. In our analysis however, we assume that the spectrum is white and all of its power is within $\pm f_s/2$. Consequently, its magnitude becomes its average power over the frequency, that is $\sigma_{ni}^2/f_s A^2/Hz$ and $\sigma_{ni}^2$ can be calculated from distribution of $e_N$.

$e_N$ has a beta distribution with $0<\alpha=\beta\leq1$ in which, from its definition, $\sigma_{ni}^2$ increases as with $\alpha, \beta$ decrease. Hence the smallest noise power occurs when $\alpha=\beta=1$ i.e. when $e_N$ has a uniform distribution. Consequently, the lower limit of input noise power is computed using the variance of uniform distribution.

$$\sigma_{ni,\min}^2 = \frac{\Delta^2}{12} = \frac{(2I_b)^2}{12}$$

$$S_{ni,\min}(f) = \frac{\Delta^2}{12 f_s}$$

Therefore,
\[ S_{no,\text{mi}}(f) = \frac{(2I_0)^2}{12} \frac{1}{f_s} |H_n(f)|^2 \]  
\[(12)\]

Substitute \( H_n(f) = \frac{H_s(f)}{K_p} \), we get the expression of output phase noise spectral density in term of power transfer function of the PLL.

\[ S_{no,\text{mi}}(f) = \frac{\Delta^2}{12} \frac{1}{f_s} \frac{1}{K_p^2} |H_s(f)|^2 \]  
\[(13)\]

If the input sequence \( \phi_i(k) \) is a stationary and ergodic random process, then the noise process \( e_N \) will also be stationary and ergodic. This means its statistical expectations and its time averages are equal. Thus, we can find variance of output phase noise from

\[ \sigma_{no}^2 = \theta_{no}^2 = \int_0^\infty S_{no}(f) df \]  
\[(14)\]

Substitute \( S_{\text{no,mi}}(f) \) from (10) into (11) results in

\[ \sigma_{no,\text{mi}}^2 = \frac{\Delta^2}{12} \frac{1}{f_s} \frac{1}{K_p^2} \int_0^{f_s} |H(f)|^2 df \]  
\[(15)\]

and the rms phase noise is simply \( \sqrt{\sigma_{\text{no,mi}}^2} \)

Evaluate (12) by substituting \( \Delta = 2I_o / f_{\text{vco}} \), \( K_p = 2I_o / \pi f_{\text{vco}} \) yields

\[ \sigma_{no,\text{mi}}^2 = \frac{\pi^2}{12} \frac{1}{f_s} \int_0^{f_s} |H_s(f)|^2 df \]  
\[(16)\]

There are two important points we can observe from (13) and (17). In (13), \( S_{\text{ni}}(f) \) is proportional to \( \Delta^2 \) meaning the large level spacing of the bang-bang PD resulting in large PD.
noise power. Since \( K_d \) is proportional to \( \Delta \), gain of equivalent linear PD will be large. As a result, its equivalent linearized PLL will have a large loop gain and \( H_s(f) \) will have a large bandwidth. While this may improve the acquisition and tracking ability of the CDR, it deteriorates ability to reject noises at the input of the CDR. In summary, a bang-bang PD with a large charge pump current will result not only increase its own input PD noise but also allow more noise to pass through the CDR input.

In (15) the variance of the output phase noise is expressed in term of the PD parameters and the jitter transfer function. After evaluated, the phase detector gain is cancelled out. Nevertheless, it effect to the output noise still exists through \( H_s(f) \). We can reduce output phase noise without changing \( K_d \) by modifying the PD to have multi-level output. For example, as illustrated in Figure 3.17, the modified PD has four levels. As a result, \( \Delta \) is reduced from \( I_L \) to be \( I_L/2 \) but \( K_d \) remains the same and is equal to \( I_L/\pi \). The output phase noise according to (15) is reduced by factor of four. This is analogous to a uniform multi-bit quantizer in A/D converter.
For CDR application, it is useful to refer to phase noise in terms of timing jitter $\sigma_t$. We can obtain variance of this quantity from the phase noise output spectrum using the following relationship [13]

$$\sigma_t^2 = \frac{2}{\omega_o} [R(0) - R(\tau)]$$

(17)

where $\sigma_t^2$ is the variance of timing jitter for measurement interval $\tau$.

$\omega_o$ is the recovered clock frequency

$R_\phi(\tau)$ is the autocorrelation of output phase noise, which is equal to inverse Fourier transform of $S_{no}(f)$

**Numerical Simulation**

CDRs using linear PD and bang-bang PD are modeled following the analysis in the last section. The models use $R=1500$ $\Omega$, $C=250$ pF, $K_d=80/\pi$ $\mu$A/rad, $K_o=300$ MHz/V and small $C_p=5p$ F. The numerical simulations are performed using Matlab. In simulation, the input phase noise with normal distribution is applied to emulate input jitter at the CDRs input. Current noises with the uniform and the beta distribution are used as an additive noise to the bang-bang PD. The rms of timing jitters as a function of measuring time calculated by (19) are plotted in Figure 3.18 for the case of $\alpha=\beta=0.5$ and 1. Noting that the timing jitter grows as the measuring time increases and is bounded as the $R_\phi(\tau)$ decreases. For the case of input phase noise is the only noise source (the lowest curve) timing jitter does not increase after measuring time larger than its loop time constant.
3.3.4 Circuit Design

To demonstrate the concept, the prototype CDR based on the proposed architecture has been designed using TSMC 0.35 μM CMOS process parameters. The design of each circuit block is explained as following.

Data Loop

Three main components of the data loop are the analog sample, the digital sampler and the charge-pump circuits.

Analog Sampler

The analog sampler is very important because it is a front-end of the phase error measurement. A good linearity and high sensitivity are desirable. Since input of the sampler is expected to be small swing signal in a rage of 100mV – 200mV and has frequency in GHz, it must be able to track that amplitude and hold for at least a half of VCO period (1 ns for 500
MHz). The sampler consists of a NMOS switch with a half-size dummy switch to cancel charge injection. It connects directly to the input stage of the low-gain differential amplifier. To maximize speed and efficiency, it uses the gate capacitance as the hold capacitor $C_H$. The effect from non-ideal switch of NMOS such as the RC low-pass filter formed by $R_{ON}$ of NMOS switch and $C_H$ and the aperture uncertainty from finite transition time of the clock are of concern. To minimize these effects, we use the low common mode level of the input (1 V) to increase an overdrive voltage of NMOS, which reduces $R_{ON}$ without having a large NMOS switch. Since the switch can be smaller, it reduces clock load and improves transition time as well as alleviates the effect of charge-injection that is not completely canceled. Further more the small NMOS switch results in small $C_{GD}$ thus reducing the clock feedthrough.

![Sampler circuits](image)

Figure 3.19 Sampler circuits (a) analog sampler (b) digital sampler. All sizes are in $\mu$m

The low-gain differential amplifier has gain approximately 1.5. It serves two purposes. First it provides a small amplification to compensate the attenuation due to low-pass effect of the analog sampler. Secondly, it provides additional the delay in signal path. This delay is necessary since at the high data rate the output of digital sampler may arrive to the charge-pump circuit at the time which analog sample is no longer valid (recall that the charge-pump circuit need both analog and digital samples to determine its output current) due to its long
resolve time comparing to the clock period. The circuit uses diode-connected load instead of resistive load since it is smaller and provides longer delay. Because both input and gain are small, the circuit operates in the linear range of its input-output characteristic.

**Digital Sampler**

The digital sampler is shown in Figure 3.19. It is a clocked comparator [14,15]. It uses a front-end sample-and-hold (S/H) circuit identical to the analog sampler in order to experience the same sampling errors. The comparator consists of a NMOS regenerative amplifier, a precharged-type PMOS latch and a static latch. It operates as follows. During tracking mode, M1 is on and M2, M3 are off. The latch stage is isolated from the amplifier stage and is precharged to high so the sampler output does not change. Because of the small $R_{on}$ of M1, the gain of the amplifier stage is reduced. Once it enters the hold mode, M1 is off, increasing the amplifier gain, and M2 and M3 turn on, allowing the precharged latch to evaluate the new data. The static latch at the last stage keeps the previous output while the PMOS latch is precharged high. Additionally, having two cascaded latches reduces the probability of the sampler producing a metastable output.

**Charge-Pump Circuit**

Conventionally, a charge-pump circuit uses switches to steer constant current sources. The amount of charge transferred to the loop filter is controlled by the duration that switch is on. This duration or the on-time is controlled by a timing pulse from the phase detector which is proportional to phase error. However, as the operating speed increases, it becomes more difficult to create the precise timing pulse to control the switches because of the speed limit of the circuit. Additionally, the switches have to turn on and off in a very short time aggravating its circuit non-idealities. In this design we take a difference approach. The phase error is measured through the amplitude of the analog sample. Charge-pump circuits then
encode this phase error into the current amplitude and create a constant pulse width. Eight charge pumps operate in time-interleaved manner, therefore the on-time of each current pulse can be longer than a bit-time. This eliminates the problem of creating narrow current pulses encountered in the standard approach.

The charge-pump circuit is a transconductance amplifier. The input stage is a differential amplifier connected to a PMOS wide-swing current mirror load through four NMOS switches. Each charge-pump has its own input stage, but the current mirror load, which functions as an analog summer, is shared. The circuit is shown in Figure 3.20.
The differential analog sample is applied to the input. The control signals select the appropriate connections to mirror the current into (source) or out of (sink) the loop filter proportional to the phase error. In case of no transition, the connections will result in the zero net current to the loop filter. The width of these signals defines the on time of the pump current, which is constant. These control signals are created from two digital samples, the samples right before and after the analog sample. They correspond to the transition status of the data according to the following table:

<table>
<thead>
<tr>
<th>Data Transition</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>Current Direction</th>
<th>( \Delta V = a - ab &gt; 0 )</th>
<th>( \Delta V = a - ab &lt; 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>High to Low</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>sink</td>
<td>source</td>
<td></td>
</tr>
<tr>
<td>Low to High</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>source</td>
<td>sink</td>
<td></td>
</tr>
<tr>
<td>High to High</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>net current = 0</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>Low to Low</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>N/A</td>
<td>net current = 0</td>
<td></td>
</tr>
</tbody>
</table>

A wide-swing cascode current mirror is used as the output stage of the circuit. It changes a differential input to a single end output current. In addition to allow a wide range of the control voltage, it provides high output impedance resulting in a good matching of PMOS and NMOS current sources.

The simulated input-output transfer characteristic of the low-gain amplifier cascaded with the charge-pump circuit is shown in Figure 3.21. The differential input is the output of the eight analog samplers sampling the 2-GHz sinusoidal signal with 150 mV amplitude and 1 V input common mode at 500 MHz. The output is the net current input to the loop filter. It shows a good linearity with a transconductance of 120 \( \mu A/V \).
Figure 3.21 Input-output transfer characteristic of V-to-I circuits

VCO Based Multi-Phase Clock Generator

Eight-stage differential ring oscillator and clock drivers are used for generating 16 sampling clock phases. The requirements of clock are full swing and have a fast transition in order to minimize sampling uncertainty. Its duty cycle should be as close to 50 percent as possible to have a uniform sampling space over the VCO tuning range. The tuning range should be wide enough to cover target data rate after taking process variation into account. Low noise and small power consumption are also desired. Two ring oscillator structures that can be a good candidate have been designed and compared.
The first VCO structure that has been tested is an eight-stage low-noise differential ring oscillator based on [12]. The attractive features of this structure are using dual-delay path to increase operation frequency and providing full-swing output. It produces less thermal noise because it allows devices in the delay cell to have full switching (completely turned off). The delay cell and the ring structure are shown in Figure 3.22a. Each cell is essentially the cascade voltage switch logic (CVSL) with two NMOSs to control the conductance of the cross-coupling connection. There are additional two PMOS devices for the inputs of auxiliary delay paths (Vina-, Vina+). Depending on how they are connected, these extra paths can either increase or decrease the delay. In Figure 3.22b, auxiliary inputs of the next stage share the same input signals with the main inputs of the current stage. As a result, the delay per stage is shorter compared to that without connecting the extra paths.

Simulation results show that the VCO gain is 74 MHz/V over the range of 200 MHz to 400 MHz. However, the duty cycle of this VCO varies significantly with operation frequency.
Thus, it requires the duty cycle correction unless it operates within frequency range about ±30 MHz from its center frequency. Although it provides the full-swing outputs, the variation in its duty cycle makes this VCO inappropriately for our application.

The second structure is based on the source coupling differential delay element. The main advantage of this delay element is good noise immunity from a high impedance node of the wide-swing tail current source. In addition, the delay element draws a constant current creating less switching noise. The oscillation frequency is controlled by changing the tail current while the output swing is kept constant by adjusting a bias voltage of PMOS load. This task is usually done by using a voltage to current converter combined with the control loop of an opamp and replica delay cell. However, to have a separated circuit to control tail current and use an opamp to control the swing is not efficient. Therefore, we introduce a new circuit that is simple and able to perform both tasks together. The circuit is illustrated in Figure 3.23. The circuit is developed based on circuits in [16] and [17].

The circuit works as following. M1, M2, M3 and Vref are formed a voltage-to-current converter. M2 and M3 are identical and in saturation mode. They have the same current flowing through and their gates are tied together. Therefore, $V_{GS2}$ is equal to $V_{GS3}$ and $V_{DS2}$ is equal to $V_{ref}$. $V_{ref}$ is chosen such that $V_{con-min} + |V_{tp1}| < V_{ref}$ to ensure linear operation of M2. As a result, the current of M2 reflected by wide-swing cascode to be the tail current of delay cells will change linearly to the $V_{con}$. The swing control is done by a loop of Vref, M3, M4, and M5. M3 and M4, which are in saturation force $V_{DS5}$ to be equal to Vref by adjusting the gate voltage of M5 through the change of $V_{D4}$. This gate voltage is connected to the P_bias for all PMOS loads in the delay cells. Since the PMOS loads carry the same current and have the same bias, their voltage drop will be equal to Vref. In this design Vref is created from two parasitic diodes (p+ on n-well) which results in output swing approximately 1.2 V.
Figure 3.23. Delay stage of VCO and its control circuit

Figure 3.24 Small-wing to full-swing buffer
Since the output is small swing, it needs a buffer to change to full swing. We have designed such a buffer as shown in Figure 3.24. The circuit operates as following. Without M2 and M3, M1 and M5 as well as M4 and M6 work like a normal inverter. Because the inputs are close to Vdd, M5 and M6 have never been completely turned off while M1 and M4 have never been completely turned on. As a result, the output levels are close to GND. By adding a cross coupling M2 and M3, it reduces the on-resistance of the pull-up network without increasing capacitive load to the inputs. With properly sizing, the output level is shifted to the middle of the supply rails and ready for the typical inverter.

This VCO has the gain of 300 MHz/V as shown in . Its duty cycle is about 50 percent within the frequency range of 320 MHz – 500 MHz without need of duty cycle correction.

![Figure 3.25 VCO control transfer characteristic](image)
**Reference Loop**

The reference loop composes of a three-stage phase frequency detector (PDF) and a charge-pump circuit. The dynamic-type PFD based on [18] is chosen because of its speed advantage and small area required. The charge pump circuit is implemented as simple current sources with UP and DN switches connecting to VDD and GND instead of the output node. This eliminates charge-sharing problem at the output node without need of a buffer amplifier. The phase detector and charge pump circuit are shown in Figure 3.26. In the simulations, the circuit shows small static phase error less than 18 ps at operation frequency 400 MHz. This is due to the mismatch between PMOS switch and NMOS switch. The error has no effect to the performance of the overall system.

![Figure 3.26 Dynamic phase detector and charge pump of the reference loop](image-url)

Figure 3.26 Dynamic phase detector and charge pump of the reference loop
**Controller**

The controller is essentially the lock detector circuit that generates the lock signal to disable the charge-pump of the reference loop and enable the charge-pump of the data loop. It consists of a XOR gate and a seven-bit resetable asynchronous counter as shown in Figure 3.27. The counter is clocked by the Ref and reseted by the XOR output. The XOR gate compares the UP and DN pulse from the output of PFD. At large phase difference of Ref and VCO, the XOR continuously produces pulses to reset the counter hence disable the lock signal. Once phase error between the Ref and VCO become so small that the XOR is unable to produce the reset signal, the counter continuously counts up to 128 Ref clock cycles then generates the lock signal allowing the data loop to take over.

![Figure 3.27 Controller circuit](image)

The smallest mismatch between UP and DN that the XOR can detect defines the number of bit needed for the counter to ensure that the reference loop is in locked state before switching to the data loop. In this design it can detect the mismatch as small as 150 ps. During the acquisition process of the reference loop there are two possible cases that the small mismatch can happen. The first case is when the Ref and VCO frequency are almost equal. At 500 MHz, 150 ps mismatch is equivalent to less than 0.08 percent of frequency error. This error is in the lock range of the reference loop and it can be eliminated before the counting ended. The other case, there is a large frequency difference outside the lock range but the phase
difference is momentarily small. In such a situation, the mismatch of UP and DN will eventually become larger again resulting in the counter being reseted before finishing the count.

**Loop Parameter Optimization**

Since data loop and reference share the VCO and the loop filter, they have to be designed together. The data loop is chosen to optimize first. The reference loop is then adjusted through its phase detector/charge-pump gain. The loop filter is a $RC_s$ with a small $C_p$ in parallel. The system is a third order, which has the first two poles at DC, a zero at $\omega_z = \frac{1}{RC_s}$ and the third pole at $\omega_p = \frac{C_s + C_p}{RC_s C_p}$. As $C_p << C_s$, it is an approximate second order system.

The following design procedure is applied.

1) Determine loop bandwidth of the PLL from the open-loop crossover frequency

$$\omega_{\text{cross}} = K = K_o K_d \frac{RC_s}{C_s + C_p}$$

2) Using $N = M$, damping factor: $\xi = \frac{1}{2} \sqrt{\frac{K}{\omega_z}}$

3) At $\omega_{\text{cross}}$, determine gain margin and phase margin for stability.

4) Additional stability condition from z-domain analysis $T_s \leq 2RC_s$ or data rate $> \frac{\omega_z}{2}$

The CDR is designed to have small loop bandwidth to reject input jitter. However, small loop bandwidth also allows more jitter from VCO and degrades tracking ability. Accounting for those factors and its ability to be integrated, the following components are used: $R=750 \ \Omega$, $Cs = 300 \ \text{pF}$, $Cp = 5 \ \text{pF}$. As a result, the loop bandwidth is approximately 11.25 MHz, $\xi = 0.8$, and phase margin = 70 degree. A matlab plot of the design is shown in Figure 3.28.
3.3.5 Simulation Results

The data recovery circuit is designed to recover NRZ data transmitted through a band-limited channel. In order to include the effect of the channel in simulation, we filter the input data with a first-order RC (50Ω and 2pF) low-pass filter with a –3 dB frequency of 1.6 GHz. A 3.2 Gbps 2^7-1 PRBS with amplitude 200 mV, transition time 150 ps is applied through the filter. After filtering the received data has an eye opening of 139 mV and 296 ps. The circuit is able to recover clock and data correctly. The simulated eye diagrams are shown in Figure 3.29. The top waveform is the input data. The bottom waveform overlays three of the 16 clock phases. CLK1 and CLK3 drive digital samplers to latch two consecutive data bits. CLK2 drives an analog sampler to measure the input at the transition between the two bits.

Figure 3.28 Matlab simulation of the data loop frequency response
Figure 3.29 Simulated eye-diagrams of the received data at 3.2 Gbps and the sampling clocks (internal signals) at 400 MHz

The recovered clock frequency is 1/8 of the data rate, or 400 MHz. As explained earlier, when the data loop is locked, the sampling clock edges (the falling edge of the recovered clock) of the analog samplers will align with data crossing points. However, in Figure 3.29 there is 60 ps delay between the data crossing point and the midpoint of clock falling edge (CLK2). This phase offset arises from three non-ideal effects in the analog sampling circuits. First, the RC delay formed by the finite $R_{on}$ of the NMOS switch and $C_{hold}$. Second, the finite transition time of the clock combined with the non-ideality of the switching threshold creates sampling uncertainty. In other words, the effective sampling time does not correspond exactly to the midpoint of the clock transition. Finally, the effective sampling time has a small dependence on the level of its input. The peak-to-peak jitter of the recovered clock at
the output pin with 5 pF load is 46 ps and shown in Figure 3.30. Summary of the design is in the table 2.

Figure 3.30 The peak-to-peak jitter of recovered clock at the output pin

Table 3.2 Summary of the design

<table>
<thead>
<tr>
<th>Data rate</th>
<th>Up to 3.2 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak-to-peak clock jitter</td>
<td>46 ps @ 3.2 Gbps</td>
</tr>
<tr>
<td>Process technology</td>
<td>TSMC 0.35μm CMOS technology</td>
</tr>
<tr>
<td>Chip area</td>
<td>0.98 mm²</td>
</tr>
<tr>
<td>Power consumption</td>
<td>145 mW for core CDR and 82 mW for output drivers @ 3.2 Gbps</td>
</tr>
</tbody>
</table>
3.4 Conclusion

In this chapter we have proposed the data recovery system based on the 2x oversampling linear phase detector technique. This technique uses a multi-phase PLL to generate 16 uniformly spaced clock phases. These clock phases are used in time-interleaved manner to sample the high-speed serial input data. They provide the effective sampling rate at two times of the data rate. The key to obtain the synchronization and to recover the data is to place eight analog samplers alternately with eight digital samplers. The sample voltages of the analog samplers and the bit values of the digital samplers are combined to provide the input phase error to the multi-phase PLL. Because of using analog sampler, the loop is corrected linearly toward the locking state. Once the PLL attains the lock state, the outputs from the digital samplers are the recovered data.

Because the multi-phase PLL uses the slow oscillator to recover the phase error from a high frequency input, its time-interleaved sampling behavior is neither be described nor predicted accurately with the conventional continuous-time PLL model. Therefore we have developed a new model based on discrete-time linear system. This model take into account the sampling nature of the loop, which provide greater insight into system behavior, and understanding the system constrains. We have used this model to analyze the phase noise due to non-linear operation of the all-digital 2x oversampling known as bang-bang type data recovery. The analysis shows that the multi-phase PLL that uses bang-bang type PD is inferior to the linear phase detector technique in terms of acquisition, output jitter and stability.
3.5 References


Chapter 4

Chip Implementation and Measurement

4.1 Introduction

In this chapter the physical design of the prototype is described. Several design techniques from the top level to the circuit level have been employed to cope with practical issues such as process variation and noise. The design of the test fixture, which is important to the measurement particularly at the high frequency, is discussed as well. The measurement results and its analysis are covered in great detail. Finally based on the test results, the design suggestions for further improvement are included at the end.

4.2 Physical Design

The prototype CDR was designed for the TSMC 0.35\(\mu\)m process, which has the \(f_T\) about 15 GHz\(^1\) and using 3.3 volts supply. The process offers one polysilicon and four metal layers. At the time the design was carried out, it was a non-epi process. However by the time it was submitted to fabricate the process had changed to be epi-process (using epitaxial wafer). The change of in the substrate directly affects the noise performance of the design. It will be discussed later in detail. Because the prototype CDR is composed of both digital and analog circuits, noises and interference are one of the great concerns. To minimize these effects, several preventive techniques in physical design had been implemented. Beginning from the top level, the floor planning of the chip was chosen to distance the digital parts and analog parts as much as possible. As shown in Figure 4.1, the top part of the chip is the digital circuits such as the control circuit, the retiming circuit and the output drivers. The analog circuits, which are more sensitive to noises, occupy the lower half of the chip. These include

\(^1\) Estimates from the National Roadmap for Semiconductors 1997 edition
the biasing circuits and the PLL. The high speed input signal and the parallel samplers are at the middle of the chip. The rest of the chip areas are the loop capacitance and the decoupling capacitance. Since it was expected to have the input NRZ data at the data rate up to 4 Gbps, which is too fast to go through the pin of the regular package (PGA). Therefore the input was provided directly to the chip using the microprobes and the probe pads with the on-chip polysilicon resistance terminators. The chip occupied total area of 2.2 mm x 0.6 mm.

![Figure 4.1 The floor plan of the prototype CDR and the die photograph](image)

In the circuit level, dummy devices and guard rings are used to surround some of the sensitive circuits. For the layout style, instead of having the centroid symmetry, the layout of the samplers and the VCO stages were carefully designed to maintain the compactness and the symmetry to their inputs, which are very important for the high-speed signal. The extra precaution was taken for the interconnect carrying the input NRZ data (metal4) by shielding and grounding with metal2 at the bottom and metal3 along the sidewall.
The passive components of the design are resistor and capacitor. Polysilicon was used for the resistor because of its small variation (approximately ±15). In this design a large value of capacitance is needed as the part of loop filter and the decoupling capacitance. It was realized from the accumulation-mode MOS capacitor because of its highest value per unit area (~ 4.5 fF/μm²) and its frequency independence. PMOS devices were used by connecting drain, source and body (well contact) together to be the negative terminal and gate to be the positive terminal of the capacitor. The arrays of a small unit-size capacitor of 1.6 pF were connected in parallel to have a large value capacitor and to have charge distributed evenly as well as to increase number of well contact.

The chip power distribution is the grid network formed by metal1 and metal2. It provides an easy access to the power rails and reduces the resistance. To reduce switching noises, the decoupling capacitors were distributed around the active area over the chip. However due to the limited chip area the total amount of decoupling capacitor is only 45 pF. To reduce the inductance from the wire bonding and the packaging, the multiple pins (total for 16 pins) are used for Vdd and GND. In addition, pins and routings for the Vdd and GND of the core CDR (VddA and GNDA) and of the output drivers (VddD and GNDD) are separated. However, GNDA and GNDD are still short together through the substrate.

4.3 Packaging

The prototype die is packaged in the ceramic PGA108M package provided by MOSIS. The electrical characteristic model of the package is shown in Figure 4.2. The resistance values of R1 and R2 are less than 0.5 Ω. The inductance values of L1 and L2 and the capacitance values of C1 and C2 are in the range of 4nH – 7nH and 0.1pF – 3pF respectively. When looking from the pin to the bond finger and including the input impedance of the circuit on the chip this parasitic network forms a low-pass filter that has the large gain peaking up to 40 dB at frequency around 1.6 GHz – 3 GHz. This network may not be the limit for the maximum frequency but it can cause the ringing in the signal that passes through it. This
ringing not only degrades the signal but in the worst-case it can as well cause the resonance if the signal frequency or its harmonic coincides with the ringing frequency.

![Figure 4.2 Model of the packaging parasitic [1]](image)

In addition to the parasitic inductance from the package the bonding wire, as a conductor above the ground plane, contributes the inductance approximately 1nH/mm. Depending on location of the pin and the die size, the length of bonding wire can be 3mm – 7 mm long. Therefore the total inductance in each pin from the packaging pin to the chip bonding pad are in the range of 7nH – 15nH. The large values of the parasitic inductance can significantly deteriorate the prototype performance, as we will discuss later in the measurement results.

### 4.4 Test Fixture Design

Test fixture is an important part of the testing. The main objective of the fixture is to facilitate the testing without introducing any artifact to the result. The fixture is fabricated from the two-layer print circuit board (PCB) with FR4 material. It was designed to have a large ground and Vdd plane to reduce impedance in power paths. The ground loop was avoided in order to minimize the electromagnetic interference from the surrounding sources. Total of approximately 50 μF on-board decoupling capacitances are added to minimize the effect of large switching noises. Because the on-board capacitor itself has the parasitic inductance it can effectively behave as a capacitor only in certain range of frequency.
Therefore one way to overcome this drawback is using different types of capacitor and combined with a variety of values in order to have different self-resonance frequency. The ceramic chip capacitor is preferred since it typically has the smallest parasitic inductance. The large number of small value decoupling capacitors is used in parallel to reduce it effective parasitic inductance. The capacitors were placed as close to the package pins as possible.

The input reference clock and the recovered output data are expected to have frequency up to 500 MHz. Therefore the connection between test fixture and the test equipments is using 50 Ω coaxial cable with the SMA connector. The on-board traces from the SMA connectors to the package pins are carefully designed to have 50 Ω impedance matching with the cable and was verified with the TDR measurement.

4.5 Measurement Setup

The measurement setup is shown in Figure 4.3 The HP8133 pulse generator provides \(2^{23}-1\) PRBS with the data rate up to 3.5 Gbps. The NRZ data is transmitted through the channel that composes of one meter long 50Ω coaxial cable (RG-142B/U) and the model-10 picoprobe™ set which together has the 3dB bandwidth more than 2 GHz. Therefore, to create the bandwidth limited channel, the 500ps low-pass risetime filter model-5910 from PicoSecond Pulse Labs is added into the channel limiting the bandwidth to 694 MHz. The filter is a 10th order filter with the insert loss approximately 25 dB for the first two octaves. The NRZ data are the differential signals with amplitude between 100mv – 200mv and common mode voltage in the range of 900mv to 1100mv. The full-swing reference clock at the frequency one eight of the data rate is provided by the HP8133 and fed directly to the test fixture. The outputs from the prototype are the full-swing eight-bit recovered data and the recovered clock. The outputs are sent to TekTLS216 logic scope to display the real-time digital signal. The recovered clock is also sent to the Tek11801A sampling scope to measure jitter and to display with the eye diagram of input NRZ data simultaneously.
4.6 Measurement Results

By the design, after the prototype is powered up, the reference clock and the input data are applied. The acquisition process will begin with the reference loop tuning the VCO to the frequency one-eighth of the input data rate. Once the VCO frequency is in the capture range of the data loop the reference loop is disabled. The data loop then takes over. The data will be recovered correctly after the data loop successfully acquires the phase locking with the stream of NRZ data. The entire process is expected to take within a few seconds.

The measurement was planned to conduct in a three-step experiment. The first experiment was to observe the self-oscillation of the VCO. Therefore the prototype was given only the power supply while the reference clock input and the data input were disabled. In the second step the reference clock was applied while the input data (in and inb) either floating or applied
with their common mode voltage. The final experiment was the full testing which both reference clock and the input data were applied.

In the first testing, when starting up the VCO oscillated at the frequency approximately 240 MHz to 260 MHz. This self-oscillation frequency varies from one chip to another chip and is significantly lower than the simulation result, which is around 400 MHz. The output VCO clock at the package pin with 5 pF load shows some distortions such as the ringing that results in a signal swing about ±500 mv larger than the power rails. It also displayed a variation of duty cycle from the 50 percent in the simulation to be between 55/45 to 60/40 percent. A large peak-to-peak jitter more than 300ps was observed. The supply and substrate noises are measured as following. At VddA pin, the supply of the core CDR circuit, noises amplitude is 450 mV peak-to-peak. At the VddD pin, the supply of the output drivers, noise amplitude is as large as 1.2 volt peak-to-peak. For the GND pin, the ground bouncing was approximately 800 mV peak-to-peak. Because the GND of the core circuits and the output drivers are actually shares through the same substrate therefore the ground bouncing is the collective results of both circuits. Once the output drivers were turned off the ground bouncing due to the core circuits alone was around 300 mV peak-to-peak. The results shows a severe noises condition.

The second test is to verify the operation of the reference loop. Since the reference loop is the PLL using PFD, its capture range is as wide as the range of the VCO. To facilitate the locking process, the 250 MHz reference clock which is close to self-oscillation, was first applied. The PLL did not lock. The VCO either continues the oscillation at its free running frequency or immediately stops the oscillation. In both cases, the VCO output signal shows the significant of the strong coupling of the reference clock as shown in the Figure 4.4. The coupling phenomenon is further examined by sweeping the frequency of reference from the very low frequency 10 MHz to 1 GHz. The result is interesting. As the frequency changed the amount of coupling either increased or decreased. At certain frequencies the amount of coupling was so large that the VCO stop the oscillation. The amplitudes of the coupling were measured at several locations both on the test fixture and inside the chip. On the average the
coupling amplitudes that appeared at the Vdd and the GND were in the range between 2 volts to 9 volts peak-to-peak. Their relative phase between the coupled Vdd and the coupled GND changed over the range of frequency. Apparently, such a large amplitude can prevent the circuits from proper functioning. The very high voltage several times greater than the supply rails is the indication of the resonance effect. In order to gain more understanding, the coupling amplitudes at Vdd and GND inside the chip are plotted versus the reference frequency as illustrated in Figure 4.5. The plot also compares the coupling when the reference clock was applied at the package finger and at the bonding pad. In both cases, the strong coupling occurs when reference clock frequency is in between 150 MHz – 250 MHz. Although the coupling amplitude at Vdd is larger than at GND, both show similar trend. The amplitudes are smaller when the clock is directly fed at the bonding pad.

Figure 4.4 The coupling between the VCO output and the input reference clock. On the left is the coupling on the Vdd and GND.
The fast edge rate (rise time and fall time) of the reference clock can also aggravate the coupling. The HP8133 pulse generator provides the signal with 80ps rise time and fall time. To alleviate its effect, the reference clock was passed through the risetime low-pass filters to reduce rise time to 200ps, 500ps and 1ns respectively. Although the coupling amplitude was reduced almost 30 percent when using 1ns filter, the reference loop was still not working correctly. Due to the problem of the reference loop, the data loop testing and full function experiment could not be conducted. This is because it requires the reference loop to lock first and then hand over the control to the data loop.

Figure 4.5 Plot of the coupling magnitude versus frequency of the input reference clock
4.7 Chip Modification and Measurement

From the result of the prototype testing, it can preliminarily conclude that there are at least two main problems contribute to the prototype failure. The first problem is the large supply noise and ground bouncing. The other problem is the coupling and the resonance in power distribution network caused by the input reference clock. In the experiment, turning off the output driver circuits can reduce the large supply noise and ground bouncing. Unfortunately, there is no other way to observe the output clock if its output driver is turned off. For the reference loop, because of the resonance, it cannot function correctly. Furthermore the coupling effect interferes and prevents other circuits to operation properly. In the design the reference loop serves only as an auxiliary circuit for the acquisition. Without reference loop the data loop is still capable to acquire the lock state within the small frequency range approximately 10 MHz from the VCO frequency if the preample input data is provided. Therefore the data loop, which performs the 2x oversampling, can still be tested. The procedure is to disable the reference loop and enable data loop using the external control signal while the VCO is oscillating at its free running frequency. Then apply the preamble at the data rate eight time of the VCO frequency. The data loop should be able to lock. Subsequently, the random data can be applied. To characterize the prototype performance, we can slowly change the data rate to find its operation range and tracking ability.

In order to achieve the procedure that we have described, the prototype need to be modified as shown conceptually in Figure 4.6.

1) The internal control signal from the controller that selects between reference loop and the data loop was cut allowing the external control signal to apply without damaging the chip.

2) The interconnect of the PLL control voltage was modified to allow external control signal to apply. These will give a mean to verify the operation of the VCO

3) The interconnect that routes the recovered clock to the output driver was modified to allow the access (probing) the clock signal without turning on the output driver.
The modification was done using Focused Ion Beam (FIB) technique to cut and patch metal layers.

The modified prototype testing was carried on as following. First the modified chip was powered with the output driver turning off. The supply and substrate noises were measured while the VCO oscillated at its free running frequency. The noise amplitude is reduced almost 50 percent. The free running oscillation clock was measured internally through the FIB spot. The frequency oscillation slightly changed to be around 260 MHz. The clock jitter is reduced to be less than 200 ps peak-to-peak. The measurement of the frequency spectrum showed that there was approximately 50 percent improvement in phase noise. The Table 2.1 summarizes the measurement results of the prototype before and after the modification. The
time domain waveform and the frequency spectrum are shown in Figure 4.7 and Figure 4.8 respectively.

Table 4.1 Summary of the measurement results of the free running oscillation

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Before Modification</th>
<th>After Modification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free Running Frequency</td>
<td>255 ± 5 MHz</td>
<td>260 ± 2 MHz</td>
</tr>
<tr>
<td>Supply Noise VddD</td>
<td>1.2 v</td>
<td>N/A</td>
</tr>
<tr>
<td>Supply Noise VddA</td>
<td>450 mv</td>
<td>450 mv</td>
</tr>
<tr>
<td>Substrate Noise GND</td>
<td>800 mv</td>
<td>300 mv</td>
</tr>
<tr>
<td>Jitter: peak-to-peak and rms</td>
<td>&gt; 300 ps, N/A</td>
<td>&lt; 200 ps, 25 ps</td>
</tr>
</tbody>
</table>

Figure 4.7 Waveform of the VCO clock after the modification. The falling edge (left) has 24ps rms jitter
Next, the VCO circuits which includes the ring oscillator, the biasing and voltage-to-current converter circuits were characterized. The external control voltage varied from 0 – 2 volts was applied through the FIB pad. The tail current of the ring oscillator was measured and plotted as a function of the control voltage and compared to the similar plotted from the simulation results using the process parameters from different runs. As shown in Figure 4.9, SYS, FAB and MAY are the simulation results. SYS uses the same process parameter used for design the chip. It is an only available parameter that includes the process variations (process corners). However it was 18 months old at the time it was used. FAB is the simulation using the parameter from the same run that the chip was fabricated (T16T_LO_EPI). MAY is the simulation result based on parameter on the May 2001 run (T13Q_1P4M) which is dated back two months prior the T16T_LO_EPI run. MEASURED is the plot of the data from the measurement results. These plots confirm that the simulation and the measurement of the dc characteristic of the circuits are almost the same. It also shows that for the dc testing the non-epi and the epi process parameter give the similar results. However the offset between SYS and the rest indicates that the parameter that used for the
designing prototype is out of date. By calculation, this offset translates into the lower of the VCO frequency by approximately 50 MHz.

Figure 4.9 Tail current of the differential VCO plot as a function of the control voltage.

Reference loop was tested again. The similar results i.e. the coupling and the resonance remains the same. This was expected since the modification did not alter the clock routing and the power distribution network.

The final test was the data loop testing. It was conducted as following. The external control signal disable the reference loop and enable the data loop. The VCO was left running at its free running oscillation (250 MHz – 260 MHz). The preamble input at the data rate eight times the free running oscillation (2.0 Gbps – 2.08 Gbps) was applied to the chip via the probe pads. The purpose is to use the PLL properties of the data loop to lock with the data. If
the different between data rate and the eight times of VCO frequency is in the pull-in range of the data loop, it will be lock. The pull-in range of the second order PLL is approximately proportional to the loop gain. The data loop was designed with a small loop gain to have a good input noise rejection. In this case, the pull-in range is around 10 MHz. The frequency of the VCO, however, is not stable. From the rms jitter measurement, it shows that the frequency varies with in ±0.75 MHz. Eight times of this values is ±6 MHz. It is still in the pull-in range. However if the peak-to-peak jitter is used in the calculation the frequency difference will be out of the range. One way to minimize the variation of VCO frequency is to bias the control voltage externally. However, because of the damage occurred during the test, it is no longer an option.

The test setup was mainly the same as in Figure 4.3. The eye diagram of the input data at 2 Gbps, 200mv amplitude with 1 volt offset from the pulse generator before and after passed through the risetime filter is shown in Figure 4.10. The signal after filtering shows the effect of bandwidth limited channel. The eye opening decreased approximately by one half. However, the signal measured at the input pads had a severe distortion such that the data eye was closed. Therefore the filter was removed and the input signals were directly fed through the one-meter long cable. Nevertheless, the signal measured at the input pad still had a strong distortion as shown in Figure 4.11 for the preamble and NRZ data respectively. The VCO frequency was monitored while applying the data. The frequency changed a few MHz from its free running but did not lock.
Figure 4.10 Eye Diagram of the Input Data at 2 Gbps before and after risetime filter and one meter long 50 \( \Omega \) cable (RG-142B/U)

Figure 4.11  Eye diagram of preamble and NRZ measured at the input pad without using the filter.
4.8 Failure Analysis

There are several factors contributing to the failure of the prototype. However the main sources are the supply and substrate noise, the resonance coupling and the processing related issue. The design technique both in the architecture level and the circuit level also has an effect either to alleviate or aggravate these the problems. In this analysis we will first look into each factor individually. These will later lead into understanding how their effects are combined to prevent the prototype from functioning correctly.

4.8.1 Supply and Substrate Noises

Although the architecture of the 2x oversampling is based on the time-interleaved sampling, which reduces the speed requirement of the on-chip clock frequency, the performance of the prototype is still depending on edge rate of the sampling clock. In this architecture the fast full swing clock edge was used to reduce of the sampling uncertainty and improve jitter and bit error rate in the recovered clock and data. In addition, for the testing purpose the prototype was designed to drive the full swing output signals through the pin to interface with peripheral circuits. As a result, the switching activity of the circuit draws a large amount of the current in a short period of time. This caused a large switching noise that results in supply and substrate bouncing. The moderate amount of supply and substrate noise can cause signal distortion and increasing gate delay by modulating the device threshold voltage. However a large mount of noise greater than a half of the device threshold voltage clearly can prevent the circuits from working correctly. Because of the concern in this potential problem, the prototype was designed using as many Vdd and GND pin as possible. The supply pins for the output drivers and the core circuits were separated. The decoupling capacitance was added around the switching circuits as much as possible. In addition, 200 mV clock was injected into the supply to create switching noise environment in the simulation. However because of a large parasitic inductance of the package and insufficient amount of decoupling capacitance the amplitude of the switching noise is still large enough
to forestall the prototype from working correctly. From the test results we can determine the amount of switching current actually occurs and the amount of decoupling capacitor needed to limit the noise amplitude within the acceptable level as following.

**Decoupling Capacitance Estimation**

After the modification the amount of noise are 450 mV in VddA and 300 mV in GNDA. For simplicity assume that both have peak-to-peak amplitude of noise 400 mV. The average packaging parasitic inductance in each pin is 10 nH. There are four pins in parallel for VddA and GNDA, thus reduced to 2.5 nH. Assume that the switching time is 500 ps. Therefore the switching current is estimate to be

\[
\Delta I = \frac{\Delta V \Delta T}{L} = \frac{(400 \text{mV})(500 \text{ps})}{2.5 \text{nH}} = 80 \text{mA}
\]

This is the maximum of switching current that supply pins provided to part of the circuits that switched during the rise time and fall time. Using this amount of switching current we can estimate the total effective capacitive load of the circuit that switches from rail-to-rail. First consider the simplified model of the prototype in Figure 4.12 [2].

---

**Figure 4.12 Simplified model for charge redistribution analysis**
In this model L is the parasitic inductance of the package and bonding wire. The on-chip parasitic inductance is small so it is neglected. The on-chip circuits are modeled as the switches and the capacitors [2]. The $C_n$ is represent the gate oxide capacitance of the nMOS devices and the capacitance of the interconnects above the substrate. Similarly, $C_p$ is represent the gate oxide capacitance of pMOS and the capacitance due to the interconnects above n-well. $C_d$ is the on-chip decoupling capacitance and other capacitance that coupling between Vdd and GND. In this model we also ignore the parasitic resistance in the power distribution and in the switches. During the clock rise time and fall time some of the capacitive loads $C_s$ are switching and draws an instantaneous large current. This current is supplied by the power supply pins as the current $I_L$ and by the charge transferred from $C_d$ as the current $I_D$. For example in Figure 4.12 as the clock slews from high to low, the switch $T_p$ is turning on and $T_n$ is turning off. The current $I_n$ charges $C_n$ to the Vdd while the $I_p$ discharges $C_p$. Therefore node A is raised to Vdd. In this case $C_s$ is equal to $C_n$. The instantaneous draw of $I_L$ results in the voltage drop across the inductance L causing the voltage $\Delta V$ dipping in Vdd and rising in GND node.

To estimate the $C_s$ of the prototype and the $C_d$ needed to contain supply and substrate bouncing within a given $\Delta V$, we apply the charge conservation law. Let $Q_L$ is the charge from the supply pins, $Q_{D1}$ and $Q_{D2}$ are the charge from decoupling capacitance before and after switching. $Q_{S1}$ is the charge needed to charge up $C_s$. Therefore

$$Q_L + Q_{D1} = Q_{S} + Q_{D2} \quad (1)$$

Roughly, $Q_L$ can be calculated from $\Delta Q_L = (\Delta V \Delta T/L) \Delta T$, where $\Delta T$ is the fall time and $\Delta V$ is the maximum drop in the supply. However this may overestimate since the drop in the supply is not constant over the length of the fall time. From the measurement the drop (or rising) in the supply can be approximated as a linear ramp function $V_n(t)$ which is 0 at $t = 0$ to $V_{max} = \Delta V$ at $t = t_f$ [3]. Therefore $I_L$ is
\[ I_L(t) = \frac{1}{L} \int V_n(\tau) d\tau \]

\[ = \frac{1}{L} \int_{0}^{t_f} V_{\max} \tau d\tau \]

\[ = \frac{V_{\max} t_f^2}{2Lt_f} \]

Consequently,

\[ Q_L = \int_{0}^{t_f} I_L(\tau) d\tau \]

\[ = \frac{V_{\max} t_f^2}{6L} \]

Note that the ramp approximation yields \( Q_L \) only \( 1/6 \) of \( \Delta Q_L \). Before the switching \( C_d \) has a charge of \( Q_{D1} = V_{dd}C_d \) and \( C_s \) has no charge. After switching, the total charge is \( Q_{D2} + Q_S = (C_d + C_s)(V_{dd} - 2\Delta V) \). Thus

\[ \frac{\Delta V t_f^2}{6L} + V_{dd}C_d = (V_{dd} - 2\Delta V)(C_d + C_s) \] (2)

\[ C_s = \left( \frac{V_{dd}C_d + \frac{\Delta V t_f^2}{6L}}{V_{dd} - 2\Delta V} \right) - C_d \]

Substituting \( t_f = 500 \) ps, \( \Delta V = 400 \) mV, \( L = 2.5 \) nH, \( V_{dd} = 3.3 \) and \( C_d = 50 \) pF yields \( C_s = 18.64 \) pF. This is the effective switching load of the prototype. In addition, \( C_s \) can be estimated from the power consumption, from

\[ P_{ave} = fC_s V_{dd}^2 \]

In measurement, \( f = 250 \) MHz, and average current is 30 mA. However, approximately 10 mA of 30 mA is the standing current. Thus the power average from the switching activity is around 20 mA which give \( C_s = 24 \) pF. Conclusively we can estimate that the effective
capacitive load of the prototype is around 20 pF. From the architecture level of the time-interleaved sampling, there is one eight of the circuits are switching or the activity factor $\alpha \approx 1.2$. Therefore we can estimate that the total capacitive load of the chip (exclude the PLL loop filter) is in between 160 pF to 200 pF.

In general the maximum noise amplitude $V_{\text{max}}$ should be kept below one half of the device threshold voltage, which is approximately 250 mV. Using equation (4.2), substitute $C_s = 18.64$ pF and $\Delta V = 250$ mV the minimum amount of on-chip decoupling capacitance $C_d$ required is 96 pF. Conservatively, we can assume that the decoupling capacitance should be able to provide all the charge for the $C_s$ without instantaneous draw current through the supply pins. In this case the required $C_d$ is calculated from the charge sharing between $C_s$ and $C_d$ by setting $Q_L = 0$ in (4.2). This results in $C_d = 104$ pF. This values is not overestimate as we consider the fact that if the decoupling capacitor is discharged significantly, it may take many cycle to charge it back up to Vdd. Therefore the conservatively high value should be used. In the prototype, due to the limited area, there is no decoupling capacitance for the output driver. The on-chip decoupling capacitance is for the core circuit. It is only 50 pF, which is clearly insufficient.

### 4.8.2 Resonance in Power Distribution Network

The large amount of coupling of the reference clock on the power distribution network is unusual. Typically the crosstalk between adjacent interconnect is in a few hundreds mV. It depends on state of the interconnects (Hi, Low or Float) and the parasitic network between them which can be both capacitive and inductive coupling. However, in our case, the coupling is not confined to the adjacent wires of the clock network but the coupling appears everywhere on the chip. This is because the coupling actually occurs on the power distribution network. Additionally, the magnitude of the coupling that is well above the supply rail and has a band-pass frequency response are the indication of the resonance. The
resonance circuit could be composed of the on-board power distribution and decoupling capacitance, the parasitic of the package, the on-chip power distribution network, the load capacitance of the circuit and the on-chip decoupling capacitance. The simplified model is shown in Figure 4.13 (a). In this model, $L_B$ and $C_{CB}$ are on-board inductance and capacitance. $L_F$, $C_F$ and $L_W$ are the packaging parasitic and bonding wire inductance. $C_{DC}$ is the on-chip decoupling capacitance. The active circuits are modeled as $C_p$, $C_n$ and $R_{on}$. Typically, the impedance of $R_{on}$ is much smaller than $C_n$ and $C_p$. The active circuits are the variable loads. They are depending on the activity ratio $\alpha$ that used in the power consumption estimations. Note that the parasitic resistance of the network is neglected since its value is very small.

This circuit can be simplified further [4] to the serial RLC resonance circuit as in Fig.4.12 (b). This resonance circuit has its natural frequency and damping factor as

\[
\omega = \sqrt{\frac{1}{2LC_T}}
\]

\[
\zeta = \frac{R_T}{2\sqrt{2L}}
\]

Figure 4.13 (a) Simplified models of the prototype power distribution (b) equivalent resonance circuit.
It can resonate if it is excited by another energy source that has the frequency spectrum or the harmonic within its frequency band.

Based on this model, the power distribution network has $L = 5 \text{ nH}$ and resonates between $150\text{MHz} - 250\text{ MHz}$. Thus the $C_T$ is equal to $80 \text{ pF} - 225 \text{ pF}$. This amount of capacitance much larger than the switched capacitive load from the active circuits combined with the on-chip decoupling capacitance. The only large capacitor on-chip is the loop filter capacitor of the PLL which is $280 \text{ pF}$. This capacitor is in series with small resistor about $1 \text{ k}\Omega$ and connected between the charge-pump output and $V_{ddA}$. If there is any low impedance path formed between the output of charge-pump circuit to GND at resonance frequency, this capacitor will be included into the equivalent network and can result in the resonance circuit. One possible scenario is shown in Figure 4.14.

Figure 4.14 The low impedance path from the charge-pump output to GND
The resonance can be prevented by increasing value of the $R_T$, which increases the damping factor of the circuit in Figure 4.13 (b). There are several ways to increase $R_T$ such as adding the resistance to the decoupling capacitor [5] or include some series resistance in the power distribution network as suggest in [6][7][8]. Based on these solutions, it may not be the best to minimize parasitic resistance in the power distribution network.

### 4.8.3 The Change of Substrate Type

The TSMC 0.35µm process has changed from non-epi process to the epi-process after the design was submitted. The main difference between these processes are that the non-epi process uses a uniform light doped substrate while the epi-process has a light doped epitaxial layer grown on a heavily doped bulk substrate[9]. The substrate of non-epi process can be modeled as a multiple nodes distributed resistive network [10]. Most of substrate current flows in the channel-stop diffusion near the die surface instead of high resistance bulk. Therefore the physical separation on the substrate has a large effect to the amount of substrate crosstalk. It was shown in [10] that the amount of substrate crosstalk reduces almost linearly to the distance from the noise source. Therefore the isolation between digital and analog circuits improves as the physical separation increases. Furthermore, the substrate noise coupling can be reduced almost an order of magnitude by using the guardring that interrupts channel stop and force substrate current to flow through the high resistance bulk.

In contrast, the heavily doped substrate of the epi-process can be regarded as a single node (equi-potential), any noise injected through the epitaxial layer into the heavily doped bulk will spread to the entire chip. As it was reported in [10] that the physical separation beyond four times thickness of the epitaxial layer will not significantly reduce substrate crosstalk. Using the guardring that connects to the on-chip substrate contact in this process can be destructively, since the large local substrate contact can couple to the noisy heavily doped bulk. Figure 4.15 shows the cross section of the analog circuit (nMOS) at “a” surrounded by
a guardring. R1, R2 and R3 represent the spreading resistance of the epitaxial layer. R1 can be made smaller than R2 if the guardring is placing as close to the analog circuit as possible. R3 can be small due to the large size of substrate contact. In (a) the guardring is connected to the on-chip substrate contact. As a result, it closely couples to the noisy heavily doped bulk. To implement guarding in this type of substrate it requires having the dedicated pin to connect the guardring to externally reference as in (b).

Figure 4.15 Model of the cross section of substrate used in epi-process and the gaurdring connection [10]. (a) connecting guard ring to the on-chip substrate contact and (b) connecting guard ring to the dedicate pin.

This difference in electrical characteristic of the substrate has the significant effect to the physical design strategy. The prototype design was based on non-epi process, utilizes its advantage of the physical separation to isolate digital and analog circuits. The guarding was implemented reference to local substrate contact. These techniques once implemented on the epi-process instead of reducing the coupling, it introduces more substrate coupling to the sensitive analog circuits.
Substrate Resonance in Epi-Process

The highly doped bulk used in epi-process, the non-conductive adhesive material and the cavity of the package can form the capacitor that coupling switching noise from the bulk to the cavity node. Depending on the bias voltage of the cavity node, this capacitive coupling can create a circuit that has a gain peaking i.e. exhibiting the resonance.

![Diagram of substrate resonance in epi-process](image)

Figure 4.16 A cross section of a circuit on the epi-process wafer showing the parasitic

Considering the Figure 4.16, \( C_C \) models the interconnect capacitances coupling switching noise sources such as the clock drivers to the substrate. \( C_S \) is the capacitance between bulk and cavity. \( R_S \) is the spreading resistance from the surface of the substrate contacts to the highly doped bulk node. \( L_S \) is the parasitic inductance of the substrate pin (Vss). If the cavity is biased at the same potential as Vss, \( C_S, R_S \) and \( L_S \) will be formed the impedance network \( Z_S \) between the bulk to the Vss. This network can effectively amplify and distribute the switching noise all over the die. Its equivalent circuit is shown in Figure 4.17 [10]
In Figure 4.17, the Vss and the cavity are biased to GND. The Vsw models the switching noise sources. The noise couples through $C_C$ to the substrate at $V_{bulk}$. The amount of noise at the substrate can be expressed in terms of $C_C$ and $Z_S$ as

$$V_{bulk} = \frac{C_C}{C_C + C_S} \left( \frac{S(S + \frac{R_S}{L_S})}{S^2 + \frac{R_S}{L_S} S + \frac{1}{L_S(C_C + C_S)}} \right) V_{sw}$$

This function has its maximum at frequency:

$$\omega = \sqrt{\frac{1}{L_S(C_C + C_S)} - \frac{R_S^2}{L_S}}$$

Therefore it can cause the resonance if the energy of the on-chip signal or its harmonic coincides with this frequency. To avoid the noise accumulation and possible resonance the value of $L_S$ should be kept as small as possible. Thus the resonance frequency will be much
higher than the chip operating frequency. In addition to minimize the inductive package, another simple solution is using the conductive adhesive material to glue the die to the cavity. As a result, V_{bulk} has the same potential as V_{ss} hence eliminating the substrate noise.

4.9 Possible Design Improvement

There are some possible improvements in the design of the prototype.

4.9.1 Circuit Styles

An alternative of circuit style for the digital part that minimizes the switching noise can be used. This type of circuits is known as the CMOS current mode logic (CML)[11], the folded source-coupled logic (FSCL)[12] and the current steering logic (CSL)[13]. The first two circuit styles are based on the building block similar to differential amplifier. It basically consists of has a tail current source, the differential input and output and the load which is can be either passive or active load. The last one, the CSL uses the single-end input and output. In its operation, the constant current is steered from supply to ground giving a small swing output based on functional results of the logic. Therefore it theoretically eliminates the switching noise. However there are several drawbacks of this type of circuit. First it requires both differential input and output, thus it need twice a number of interconnect. Secondly it is not as fast as full swing CMOS logic and has a limited ability to drive a big capacitive load. To gain the comparable speed it requires a large tail current hence increasing the static power consumption. This type of circuit style was considered as a possible candidate in the beginning. However because the design was aimed for low power consumption the digital part then was implement in the regular CMOS circuit. Considering the noise situation of the prototype, the large parasitic inductance of the package and the limited amount of the on-chip decoupling capacitor, these circuit styles can be an alternative solution.
4.9.2 Better Packaging

The chip performance can be significantly improved by using a package that has a small parasitic inductance. The prototype was designed with peripheral bonding pad. Therefore the package used has to support peripheral bonding. The current package is PGA108M. It has cavity size 0.350 x 0.350 in$^2$ which is equivalent to 8.8 x 8.8 mm$^2$. The prototype die size is only 2.2 x 2.2 mm$^2$. As a result, the length of bonding wire is unnecessary long, thus increasing parasitic inductance. Some commercial products for SONET/SDH use the package that has controlled impedance traces from the pins to the bonding pad. The impedance is controlled by using internal supply planes to eliminate the package inductance [14]. Alternative to commercial package is the chip-on-board (COB) solution. As reported in [15][16] a multi-layer PCB was designed to hold the microchip for testing purpose. The backside of the die is glued directly to the conducting plane on the testing board. The short bonding wires is connected directly to the conductor traces. This offered a controlled impedance and excellent ground plane for the chip.

Figure 4.18 Conventional package and chip-on-board (COB) solution
4.9.3 Design For Testability

The design can be more flexible and accessible in term of testability. More access points for the controllable and observable purpose can be included. This will be very useful to identify causes of the problems. The external loop capacitor can provide flexibility in experiment in term of PLL performance. However unless a particular circuit technique to reject external noise coupling through that component is employed, having an off-chip passive component of the PLL is not recommended.

4.10 Conclusion

In this chapter, we have described the implementation and the measurement of the design. The prototype was implemented in the TSMC 0.35 μm and was tested with the input data between 1 Gbps to 3.3 Gbps. However, the prototype fails to function correctly. The failure analysis identifies the causes as the severe noise condition in the supply rails and the resonance phenomenon of the power distribution network. The severe noise condition is due to di/dt voltage dropped across the large parasitic inductance of the package and insufficient on-chip decoupling capacitance. Additionally, the condition was exacerbated by the change of the substrate type in the fabrication from non-epitaxial to epitaxial wafer. This has not only defeated the noise preventive design strategy but also introduced more noise into the sensitive circuits. The resonance can occur naturally in any electronic systems that compose of capacitor and inductor. However, in the prototype, due to the large inductance and effective capacitive load the resonance frequency coincide with the operating frequency, thus prevented the circuit to function correctly. Finally we have suggested some solutions to alleviate these problems such as different types of circuit and packaging.
4.11 References


Chapter 5

Conclusions

5.1 Summary

The design of a multi-gigabit CMOS transceiver has been presented. Based on the parallel architecture and the multi-phase PLL, the design has shown that the gigabit range data rate can be achieved by using relatively low speed CMOS technology. The design utilizes the 2x oversampling linear phase detection that yields a low jitter recovered clock and improves loop stability. Because of its PLL-based design, it offers the tracking ability that can handle the frequency drift due to either the transmitter or the delay in the channel. The 2x oversampling requires the sampling rate only at two time of the data rate therefore reduces the hardware required such as the sampler and the clock phases. As a result, it reduces input capacitance of the system that limits the maximum bandwidth, consumes less area and power. The data recovery system uses on-chip clock at frequency 1/8th of the data rate. Due to its time-interleaved sampling and the parallel architecture, at its maximum data rate 3.2 Gbps the on-chip clock rate is only 400 MHz. The power consumption is 145 mW for the core receiver and 87 mW for the output drivers. The prototype was fabricated in TSMC 0.35μm. The tested chip however did not function correctly on account of the severe noise environment. The failure analysis reveals that there are three main causes. The first is the large switching noise (di/dt) due to large parasitic inductance of the package. The second is the resonance phenomena due to the resonance circuit formed by the packaging inductance and the on-chip capacitance either from the PLL loop capacitor or the substrate capacitance. The third is the change of the substrate type used in the fabrication process from non-epi wafer to epi wafer.

In addition to the design, the model and analysis of the multi-phase PLL has been developed. The model based on the discrete-time linear system is able to capture and accurately
describes the sampling nature of the multi-phase PLL in a familiar mathematic form. The analysis provides an insight into the system behavior and reveals system constrains.

### 5.2 Contributions

This research provides the contributions as following.

- The concept of the 2x oversampling linear phase detector [1].
- The analysis of phase noise due to the bang-bang phase detector in PLL-based clock and data recovery circuit [2].
- The model and analysis of the multi-phase PLL using discrete-time linear system [3].

### 5.3 Future Work

There are several related areas to be further investigated

- **De-emphasis Equalizer**

Inter-symbol interference is one of the main obstacles to overcome in the bandwidth limited channel. Most of the transceiver design implements a pre-emphasis type equalizer to compensate for the channel response on the transmitter side. This transmitter equalizer has an advantage of less complexity due to its availability of the timing control at the transmitter. However it usually consumes large power because it must shape output pulse against the channel attenuation. In contrast, the receiver equalizer is more complex because of the lack of timing but consume less power since the de-emphasis reshape the small amplitude of the received data prior the receiver.

The architecture of 2x oversampling facilitates the implementation of the receiver. The sampling clocks from the multi-phase PLL are available at a half bit-time resolution.
Therefore the half bit-time equalizer based on the decision feedback can be integrated into the receiver.

- **I/O Circuits**

High speed input output circuits are very important. Particularly as the signal frequency migrates into a multi-GHz range. In addition to speed, the high performance I/O must consume less power, occupies small area. Since it has to operate at the high speed and drive large load, it typically generates large switching noise. Therefore noise reduction techniques in I/O circuit such as an adjustable slew rate, and an adaptive impedance matching are very desirable. Furthermore bi-directional I/O circuits will play a significant role, as the I/O pin is increasingly precious.

### 5.4 References


Appendix A

Discrete-time Model and Analysis of Multi-Phase PLL

A.1 Introduction

Clock and data recovery circuit (CDR) is one of many applications of the phase-locked loop (PLL). There are two types of PLL-based CDR, the serial and the parallel CDR. The serial CDR is mainly the same as the conventional charge-pump PLL except that its phase detector is designed to function with the random data. Nevertheless, the operation of the phase detector is still based on the comparing edges of its input pulses and generating a pulse whose width carries the phase error [1-4]. Therefore the CDR can be analyzed directly with the existing models of the charge-pump PLL such as in [5,6]. In contrast, the parallel CDR [7-12] detects the phase error by using the multiple clock phases tapped from its oscillator to sample the input data in time-interleaved manner. The oscillator and the PLL circuit runs at frequency that is several times lower than the data rate. As a result, the parallel CDR can achieve a higher data rate than the serial CDR. Since it requires multiple clock phases this PLL is referred as the multi-phase PLL (MPLL). The MPLL can also be divided into the non-linear or bang-bang MPLL[7-10] and the linear MPLL [11,12] according to the relationship between the phase error and the loop correcting signal. The operation of both type of the MPLL is difference from the conventional charge-pump PLL in several aspects primarily due to its parallel structure and its sampling technique. Therefore, in design and analysis MPLL, the existing model of the charge-pump PLL cannot directly applied and in some cases, it is unable to predict the loop behavior accurately. Accordingly, the design is often not optimal.

In addition to a more comprehensive analysis to the section 3.3.1 in Chapter 3, the purpose of this appendix is to provide a means to perceive the MPLL so that its important features are
identified. Once its advantages and limitations become obvious, it can be exploited. It proceeds as following. In Section 2, the concept of the multi-phase PLL is reviewed. Then its simplified version, the linear sampling phase detection without the time-interleaved operation, is modeled in a discrete-time domain. Subsequently, this model is extended into the model of the MPLL in Section 3. In Section 4, we discuss the application of the model particularly in the CDR. Although the model and analysis in this appendix is derived for the linear CDR, its application to the non-linear type CDR is also proposed. We summarize the principle results in Section 5. Finally in section 6 we present the difference-equation analysis that uses in the examples of transient and frequency response simulations.

A.2 Concept of Multi-phase PLL

Multi-phase PLL (MPLL) is a PLL that use the multiple clock phases from its oscillator to lock to the input $Ref$ whose frequency is supposedly N (positive integer) time faster than its oscillator frequency. In order to achieve that, the PLL uses an array of N phase detectors to compare the input $Ref$ with N uniformly separated output clock phases from the oscillator. Outputs of all phase detectors and charge-pumped circuit are combined together to drive the loop. Once the PLL is locked each clock phase will be separated from one to another by the time equal to the period of the $Ref$. The conceptual diagram of multi-phase PLL is shown in Figure A.1.

The main advantage of the MPLL is that it uses a slower clock to lock to a faster input signal. This concept is very useful in CDR applications because it can relax the speed requirement of the circuits by incorporating with the parallel architecture. As a result, the CDR based on the MPLL is able to achieve the data rate several times higher than it possibly can if using the conventional serial clock recovery technique. The most important part of MPLL is its phase detection scheme. It is composed of the array of the phase detectors operating in time-interleaved manner to detect the phase error between two signals that their nominal frequencies are not the same. Therefore it must be insensitive to the frequency difference.
In addition, it must be able to handle the input signal that is random and has a long transition time as it passes through the bandwidth-limited channel. In consequence of these requirements, the technique to detect phase error of the MPLL is not based on the comparison of the rising (or falling) edges of its inputs (Ref and VCO). Instead, it uses a sampling technique to capture the analog level of the input Ref and extracts the phase error from that sample. We call this technique the linear sampling phase detection. This technique also leads to another type of charge-pump circuit that is compatible with the time-interleaved operation. In order to developing the model of the MPLL, we first need to understand and properly model the linear sampling phase detection along with its charge-pump circuit. However, to reduce the complexity, it is sensible to primarily model the linear sampling phase detection in a PLL without the time-interleaved operation. Subsequently, this model is modified to include the time-interleaved operation and extended into the model of the MPLL.
A.2.1 Linear Sampling Phase Detection

Model

The linear sampling phase detection is a technique of detecting phase error using the analog sampling. The main idea of the technique can be easily described with the waveforms in Figure A.2a. The top waveform, \( \text{Ref} \), is the input to the PLL. It presumably has a slow transition due to the bandwidth limited of the channel. At this moment, it is considered to be a periodic signal. \( \text{Clk} \) is the output of the VCO. Nominally in the locked state, both signals have the same frequency. The phase error between these signals is detected by using the falling edge of \( \text{Clk} \) samples the voltage level of \( \text{Ref} \) during its transition. On \( \text{Ref} \), if we use the middle of its rising edge (or the zero crossing for the bipolar signal) as a reference point for the zero phase error, then the increasing (decreasing) of the sampled voltage relative to the voltage at zero crossing point, \( \Delta v \), will imply the positive (negative) phase error. If we further assume that \( \text{Ref} \) changes linearly with time during its transition, then \( \Delta v \) will be proportional to \( \Delta t_i \), the time difference between the zero crossing and \( \text{Clk} \) falling edge as well. Since the magnitude of the phase error can be later derived from this \( \Delta t_i \), therefore both sign and magnitude of the phase error are encoded into this sampled voltage. The sampled voltage is held until the next sample is available i.e. one period of \( \text{Clk} \).

To incorporate this phase detection into a PLL, the sampled voltage is converted to current, which is eventually integrated by the loop filter to be the control voltage. The block diagram of the PLL is depicted in Figure A.2b. The sampling phase detector (SPD) represents the ideal phase detector based on this technique. Its inputs are \( \text{Ref} \) and \( \text{Clk} \) and the output is the sampled voltage \( V_{in} \). The transconductance amplifier with the gain of \( g_m \) functions as a charge-pump circuit converting \( V_{in} \) into \( I_o = g_m V_{in} \) to the loop filter.
Figure A.2 (a) Timing relationship in linear sampling phase detection

(b) PLL with sampling phase detector (SPD)

Let \( \text{Ref} \): the input signal with a period of \( T \), amplitude \( A \)

\( \theta_R(t) \): phase of \( \text{Ref} = \text{PLL input phase } \theta_i(t) \)

\( \theta_C(t) \): VCO output

\( \theta_V(t) \): phase of \( \text{Clk} = \text{PLL output phase } \theta_o(t) \):

\( \theta_e(t) \): phase error = \( \theta_R(t) - \theta_V(t) \)

\( t_k \): the time instant that rising edge of \( \text{Ref} \) reach its zero crossing, thus \( t_k - t_{k-1} = T \)

\( \Delta t_k \): time difference between zero crossing and falling edge of \( \text{Clk} \)

\( V_k \): the \( k \)th sample of the \( \text{Ref} \) at \( t = t_k + \Delta t_k \)
Refer to Figure A.2a, for small phase error

\[ \frac{\Delta t_k}{T} = \frac{\theta_e(k)}{2\pi} \]  

Therefore

\[ \Delta t_k = \frac{T}{2\pi} \theta_e(k) \]  

and if \( \text{Ref} \) lead \( \text{Clk} \), \( \theta_e(k) = \theta_R(k) - \theta_V(k) > 0 \), \( \Delta t_k > 0 \)

if \( \text{Clk} \) lead \( \text{Ref} \), \( \theta_e(k) = \theta_R(k) - \theta_V(k) < 0 \), \( \Delta t_k < 0 \)

Assuming \( \text{Ref} \) changes its voltage linearly during its transition with the slope \( M \) volt/sec, hence

\[ V_k = M\Delta t_k \]  

Consequently, we can express \( V_k \) in term of phase error as

\[ V_k = \frac{MT}{2\pi} \theta_e(k) \]  

\( V_k \) causes the transconductance amplifier to produce \( I_o \) to the loop filter

\[ I_o(k) = g_m \frac{MT}{2\pi} \theta_e(k) \]  

The quantities \( g_m \), \( M \), and \( T \) are assumed to be constant. Therefore equation (5) shows that the output current to the loop filter is proportional to the amount of phase error. For example, when \( \text{Ref} \) leads \( \text{Clk} \) \( \theta_e(k) > 0 \) the current flows into the loop filter. Similar to the continuous-time model of the charge-pump PLL we define this proportional factor as the phase detector gain \( K_d \). Thus
If the time delay due to the circuit operation of the SPD and the transconductance amplifier is insignificant compared to T, we can assume that I_o(k) occurs immediately at the sampling moment i.e. at t = t_k + Δt_k. As shown in Figure A.2a, the amplitude of I_o(k) changes from sample to sample according to (5) but it is constant over one VCO period.

To describe the PLL in Figure A.2(b) as a discrete-time system we first consider the system sampling rate. The PLL acquires its new input by sampling every VCO period then corrects itself by adjusting the VCO frequency. Therefore the sampling rate of the system is not uniform. In order to model the system analytically, we need to further approximate the sampling period of the system to be constant. From Figure A.2a, the VCO period T_v can be written as T + (Δt_k−Δt_k−1). As the PLL is close to lock state, the phase and the frequency error are small, i.e. (Δt_k−Δt_k−1) → 0. Therefore we can approximate the sampling period to be the period of Ref. T. The SPD now can be modeled using system block diagrams along with their signals as in Figure A.3. The sampling is modeled as an ideal impulse sampler with the sampling period T following by a zero-order hold block which keeps the current sample until new sample available and a constant gain block K_d

\[ K_d = g_m \frac{MT}{2\pi} \]  

(6)

![Figure A.3 Model of sampling phase detector (SPD)](image)
The linear model of the PLL with SPD is shown in Figure A.4. Note that the model is combined both discrete-time and continuous-time signals as denoted with kT and t. This type of system can be analyzed by both the discrete-time and the continuous-time method. However since the system contains an impulse sampler and we are interested in values of the signals only at the sampling event kT, it is greatly simplified and suitable to analyze with the discrete-time method. Two approaches of discrete-time analysis can be applied, the time domain and the frequency-domain. They both carry out the results that are interchangeable. The time-domain approach is to form a set of difference equations describing the system as we will explain in the section 6. The frequency-domain approach is to transform the system directly from s-domain to z-domain. To apply this approach there are certain conditions due to the sampling needed to be satisfied. To understand effects of the sampling that impose these conditions, consider a continuous-time system represented by $G(s)$ in Figure A.5. Its impulse response is $g(t) = L^{-1}\{G(s)\}$, where $L^{-1}$ denotes the Laplace transform. The system acquires its input $x(t)$ by impulse sampling operation with sampling frequency $f_s = 1/T$. The impulse sampled $x^*(t)$ is relate to the input by

\[
x^*(t) = \sum_{k=0}^{\infty} x(kT)\delta(k - kT)
\]  

(7)

It can be shown that the output of the system is

\[
y(t) = \sum_{k=0}^{\infty} x(kT)g(t - kT)
\]  

(8)
Therefore, the output at the sampling instant is

\[ y(nT) = \sum_{k=0}^{\infty} x(kT)g(nT - kT) \quad \text{where} \quad k \leq n \quad (9) \]

After taking z-transform of Eq (9) we find that

\[ Y(z) = G(z)X(z) \quad (10) \]

where \( Y(z) = \mathcal{Z}\{y(nT)\}, G(z) = \mathcal{Z}\{g(kT)\} \) and \( X(z) = \mathcal{Z}\{x(kT)\} \) are the z-transform of each signal respectively. This relationship is similar to \( Y(s) = G(s)X(s) \) of the same system without sampling. Consequently, we can analyze the continuous-time system with sampling by using its equivalent z-domain function. The condition required here is the sampling frequency \( f_s \) must high enough that \( x(kT) \) and \( g(kT) \) correctly represent \( x(t) \) and \( g(t) \) i.e. greater than twice of their signal bandwidths.

Another effect from impulsed sampling is the magnitude scaling of the system frequency response. Consider the Fourier transform of \( x^*(t) \) which is given by

\[ X^*(j\omega) = \frac{1}{T} \sum_{k=-\infty}^{\infty} X(j\omega - j\omega_s k) \quad \text{where} \quad \omega_s = 2\pi f_s \quad (11) \]

It is composed of the original frequency spectrum of \( x(t) \), \( X(j\omega) \), and an infinite number of that spectrum shifted in frequency from one to another by \( \omega_s \). All are attenuated by the factor \( 1/T \). The frequency spectrum of the output is
\[
Y(j\omega) = G(j\omega)X^*(j\omega) 
\]
(12)

\[
Y(j\omega) = G(j\omega)\sum_{k=-\infty}^{\infty} \frac{1}{T} X(j\omega + j\omega_k) 
\]
(13)

If the system has a low-pass response and the sampling frequency is greater than two times of the input signal bandwidth then

\[
Y(j\omega) = G(j\omega)\frac{1}{T} X(j\omega) 
\]
(14)

or

\[
\frac{Y(j\omega)}{X(j\omega)} = \frac{1}{T} G(j\omega) 
\]
(15)

Eq. (15) reveals that the frequency response of the sampling system is equal to that of the continuous-time system scaled by 1/T. Since the frequency response of the sampling system can be obtained from \( G(z) \) by evaluating Eq. (10) with \( z = e^{j\omega T} \) as well, we can conclude that

\[
G(z) \bigg|_{z=e^{j\omega T}} = \frac{1}{T} G(s) \bigg|_{s=j\omega} 
\]
(16)

Assume that the system in Figure A.4 satisfies the sampling condition and its response is low-pass. Thus we can apply the results from Eqs (10) and (16) to analyze the model. We first combine all the s-domain blocks in the forward path to be one single block \( G(s) \). Because there is no gain block in the feedback path, \( G(s) \) is also the open-loop gain of the system. We then derive its equivalent \( G(z) \).

The open-loop gain

\[
G(s) = \left(1 - e^{-ST}\right)K_d(F(s)) \frac{K_o}{s} 
\]

Consider a case of first order loop filter, which is a series connection of a resistor \( R \) and a capacitor \( C \). The \( F(s) \) is given by \( R+1/sC \). Hence
\[ G(s) = \left( \frac{1 - e^{-ST}}{s} \right) K_d \left( R + \frac{1}{sC} \right) K_o \]

The desired equivalent z-domain now can be derived from

\[ G(z) = Z \left\{ \mathcal{L}^{-1}\{G(s)\}_{t=kt} \right\} \]

\[ = Z \left\{ \left( \frac{1 - e^{-ST}}{s} \right) K_d \left( R + \frac{1}{sC} \right) K_o \right\}_{t=kt} \]

\[ = K_o K_d R (1 - z^{-1}) \left\{ \frac{T z^{-1}}{(1 - z^{-1})^2} + \frac{1}{2RC} \frac{T^2 z^{-1} (1 + z^{-1})}{(1 - z^{-1})^3} \right\} \]

To find the system transfer function \( H(z) \), substitute \( G(z) \) in \( H(z) = \frac{G(z)}{1 + G(z)} \) and rearrange terms,

\[ H(z) = \frac{\beta (z - 1) + \alpha}{(z - 1)^2 + \beta (z - 1) + \alpha} \quad (17) \]

where \( \beta = K_o K_d (RT + \frac{T^2}{2C}) \) and \( \alpha = K_o K_d \left( \frac{T^2}{C} \right) \)

As seen from Eq.(17), the system transfer function is second-order since the zero-order hold function does not give additional pole to the system. Noting that because of the feedback, \( H(z)|_{z=e^{j\omega T}} \neq \frac{1}{T} H(s)|_{s=j\omega} \). The Eq(17) in company with Figure A.4 is the discrete-time model of a PLL using the linear sampling phase detection (SPLL).
Stability

The Eq(17) completely describes the system. It can be used to characterize the system in terms of transient response, frequency response and stability. We first investigate the stability of the system. For the discrete-time closed-loop system, it becomes unstable if any of the closed-loop poles lies outside the unit circle and/or any multiple closed-loop poles lies on the unit circle in the z-plane.

The location of closed-loop poles can be examined by plotting the root of the system characteristic equation as a function of loop parameter. Let D(z) be the denominator of H(z) which is the characteristic equation of the system. After substituting $\alpha, \beta$ and rearrange

$$D(z) = 1 + K_o K_d R T (1 + \frac{T}{2RC}) \left( z - \frac{1 - T/2RC}{1 + T/2RC} \right)$$  \hspace{1cm} (18)

Similar to the analysis of the discrete-time charge-pump PLL (CPLL) in [5], the normalized loop gain is defined as $K_T = (K_o K_d R)(RC)$. The root locus of D(z) in Fig.6 shown that as $K_T$ increases from 0 to infinity, system poles move from $z = 1$, along the locus and end at the zeros of D(z) which are at $z = (1-T/2RC)/(1+T/2RC)$ and $z = -\infty$. Since $z = (1-T/2RC)/(1+T/2RC)$ is always inside the unit circle, hence the pole that moves toward $z = -\infty$ will move out of the unit circle when the gain is large enough. Therefore the stability limit of the system can be defined from the maximum $K_T$ that causes the pole move across the unit circle at $z = -1$ which is

$$K_T \leq \frac{1}{\pi \omega_c, T} = \frac{2RC}{T}$$ \hspace{1cm} (19)
Compare to the CPLL that has the same parameters, the stability limit is expressed as [5]

$$K \tau \leq \frac{1}{\frac{\pi}{\omega_1 \tau} \left( 1 + \frac{\pi}{\omega_1 \tau} \right)}$$  \hspace{1cm} (20)

Interestingly, the comparison of the Eq(19) and the Eq(20) shows that the SPLL can maintain its stability at the higher normalized loop gain than the CPLL. This is a result of the difference way of transferring charge into the loop filter. Referring to Figure A.7, the charge-pump circuit of CPLL has a constant current output but control amount of charge transferred by adjusting the time for the current to flow i.e. modulating the pulse width according to the phase error. In contrast, the SPLL uses the transconductance amplifier to provide the current. The current amplitude is varied according to the phase error but its turn-on time is constant and equal to a sampling period. Therefore with the same amount of phase error, the output current amplitude of the amplifier will always be smaller than that of the charge-pump circuit. As a result the SPLL can sustain larger $K \tau$ than charge-pump PLL. Furthermore the
smaller current amplitude alleviates the adverse effect of IR drop from the series resistor. The typical loop filters of a second order charge-pumped PLL are composed of a resistor and a capacitor connected in series. Because of the fixed amplitude of the charge-pumped current, it creates the instantaneous voltage jump of the loop filter output due to IR drop. This voltage jump causes the modulation in VCO frequency even if the phase error is very small, which is unacceptable in some applications. The most common solution is to include a small capacitor in parallel to the loop filter to filter out the ripple. Accordingly, the system is changed to be a third-order system thus impose more constrains in the stability. This however will not be an issue in SPLL, since the current amplitude is decreased as the phase error getting smaller.

For the designer it is useful to relate this limit to the system specification. The condition from Eq(19) can be expressed in term of input frequency \( \omega_i \) and the PLL loop bandwidth \( \omega_b \) which is equal to \( K \) as

\[
\frac{\omega_i}{\omega_b} = \frac{\omega_i}{K} \geq \pi
\]  

(21)
The plot of $K\tau$ versus $\omega_i\tau$ according to Eq(19) and Eq(20) are shown in Fig.8 for both SPLL and CPLL.

![Figure A.8 Stability limits of the second-order CPLL and SPLL](image)

From the Figure A.8, the solid line is the stability limit of the SPLL. It is a linear line with slop of $\pi$. The area beneath this line is the stable region of the SPLL. Similarly, the dashed line represents the stability limit and defines the stable region of the CPLL. Since in the locking state, $\omega_i$ is also the sampling rate hence, increasing the input Ref frequency also increase system sampling rate. On a vertical axis, increasing in $K\tau$ means the larger loop bandwidth. Because the dependency between input frequency and the system sampling rate, the information from the plot is should be read at a specific frequency. In both cases, for a given Ref frequency, the larger loop bandwidth is the less stable the PLLs are. It also shows that the SPLL can have a larger loop bandwidth than the CPLL, for example, at $\omega_i\tau = 5$ in order to be stable the CPLL must have $K\tau < 1$ or $\omega_i/K > 5$ while the SPLL requires $K\tau < 1.5$ or $\omega_i/K > 3.14$. The discrepancy of both curves however reduces as the sampling frequency increases i.e. both systems converge toward the continuous-time system.
**Steady-state Response**

Another property that is important to know is the steady state phase error of the PLL. The steady state phase error is defined as the \( \theta_d(k) \) as \( k \to \infty \). This can be calculated by applying the final-value theorem to the \( \theta_d(z) \) in response to the phase step \( \theta_i(t) = \Delta \theta \), or \( \theta_i(z) = \Delta \theta / (1 + z^{-1}) \) and the frequency step \( \theta_i(t) = \Delta \omega_i t \) or \( \theta_i(z) = \Delta \omega_i Tz^{-1} / (1 + z^{-1})^2 \). However the same results can be obtained by simply observing the number of pole of \( G(z) \) at \( z = 1 \). Since \( G(z) \) has double poles at \( z = 1 \), we can conclude that its steady-state phase error in response of phase step and frequency step is zero.

Up to this point we have developed and studied the discrete-time model and its system characteristic of the PLL based on the linear sampling phase detection. In the next section we will apply this knowledge to develop the discrete-time model of the MPLL.

**A.3 Model of Multi-Phase PLL**

Applying the result from previous section, the conceptual diagram in Figure A.1 can be redrawn as in Figure A.9. The array of PD and charge pump is replaced with an array of N SPDs and N transconductance amplifiers. The loop filter used here is only first-order. The VCO is an N-stage differential ring oscillator. The control signals \( \phi_i \phi_{i+1} \) at the amplifier define the active time for each amplifier. In this case the amplifier output (charge-pump current) of the present SPD lasts until the next SPD start to sample i.e. one sampling period, which is no longer the same as VCO period as in SPLL. The timing diagram is depicted in Figure A.9. The example of circuit implementation of an array SPD integrated with the amplifiers is shown in Fig.10.
Figure A.9 The multi-phase PLL using array of SPD and its timing diagram.
We can see from the timing diagram that falling edge of $\phi_1$ samples the rising edge of $Ref$ after the zero crossing by $\Delta t_1$ causes the current $I_{01}$ flowing into the loop filter. Later, the falling edge of $\phi_2$ samples the next rising edge $Ref$ and detects $\Delta t_2$ resulting in current $I_{02}$ flows into the loop filter while $\overline{\phi_1\phi_2}$ disables the amplifier1. The similar procedure continues for the next clock phases. Because nominally $\omega_1$ is equal to $N\omega_0$, therefore $Ref$ accumulates phase $N$ time faster than the VCO. Thus the phase error that reflects the timing error $\Delta t$ is not $\theta_R - \theta_V$ but $\theta_R - N\theta_V$. This can simply verify as following. Since there are $N$ clock phases, each phases represent the access point to the VCO output phase $\theta_V(t)$ at $n(2\pi/N)$ radius where $n = 0,1,2,\ldots N-1$. Suppose the PLL is in the lock condition, at $t = 0$, $\theta_R(0) = \theta_V(0) = 0$, so $\theta_0 = 0$ radius. After one period of the $Ref$, $t = T_R$, $\theta_R(T_R) = 2\pi$, the following phase of the VCO appears and it represents $\theta_R(T_R) = 2\pi/N$. Hence, $\theta_R(T_R) = \theta_R(T_R) - N\theta_V(T_R) = 2\pi - N(2\pi/N) = 0$ confirms that it actually in the lock condition. Therefore we can models this time-interleaved sampling as in Figure A.11.
As a result, the relationship from in Eq (1) now is modified to be, for small phase error

\[
\frac{\Delta t_k}{T} = \frac{\theta_e(k)}{2\pi} = \frac{\theta(t)_1 - N\theta_o(t)}{2\pi}
\]  

(22)

Assuming all SPDs and amplifiers are identical and have the gain \( g_m \). Similar to previous analysis, the output current from each sampling will be

\[
I_o(k) = g_m \frac{MT}{2\pi} \theta_e(k)
\]  

(23)

The array of phase detector collapses into the model of time-interleaved sampling with a zero-order hold and the gain \( K_d = g_m(MT/2\pi) \). The linear system model of the multi-phase PLL is drawn in Fig.12.

Figure A.12 The linear system model of multi-phase PLL
The same as SPLL, applying the linear discrete-time analysis yields

\[ H(z) = \frac{G(z)}{1 + NG(z)} \]  

(24)

where \( G(z) = K_o K_d R (1 - z^{-1}) \left\{ \frac{T z^{-1}}{(1 - z^{-1})^2} + \frac{1}{2RC} \left[ \frac{T^2 z^{-1} (1 + z^{-1})}{(1 - z^{-1})^3} \right] \right\} \)

Rearrange and express in term of \( \beta \) and \( \alpha \). The transfer function of MPLL is

\[ H(z) = \frac{\beta (z - 1) + \alpha}{(z - 1)^2 + N\beta (z - 1) + N\alpha} \]  

(25)

The result, as expected is a second-order system in the similar form as SPLL. However, now the PLL loop bandwidth \( \omega_b = NK \). The new characteristic equation is

\[ D(z) = 1 + NK_o K_d RT (1 + \frac{T}{2RC}) \left\{ \frac{z - \left( \frac{1 - T/2RC}{1 + T/2RC} \right)}{(z - 1)^2} \right\} \]  

(26)

which leads to the stability condition

\[ K \tau \leq \frac{1}{N} \frac{1}{\pi} = \frac{2RC}{NT} \quad \text{or} \quad \frac{\omega_i}{\omega_b} = \frac{\omega_i}{NK} \geq \pi \]  

(27)

At first glance, the Eq(19) and Eq(27) may indicate that SPLL is more stable than MPLL. In fact, both results cannot be compared directly, since the value of \( K \) are not the same due to the difference in their VCO gain. From a design perspective, however there is a particular case of comparison between multi-phase and single-phase design. If both are designed for the same \( Ref \), and use the same loop components, assuming the range of the control voltage of both designs are also the same, then the VCO gain of the MPLL \( K_{om} \) will be \( N \) time smaller.
than that of SPLL. This is one of the advantages of the multi-phase design since the VCO with smaller gain is generally less sensitive to noise than that with the larger gain. Evaluating Eq(25) by using $K_{om} = Ko/N$, the result is

$$H(z)|_{mpll} = 1/N H(z)|_{spll}$$  \hspace{0.2cm} (28)

This means that, in this case the MPLL will have the same characteristic as the SPLL i.e. the same frequency response, transient response, steady-state phase error and stability. However as indicated by its transfer function, its output is scaled down by 1/N reflecting the fact that the VCO accumulates phase at speed N times slower than the input.

### A.3.1 Sub-Sampling MPLL

Until now we assume that all N clock phases and phase detectors of the MPLL are used. However depending on its application and design specification, MPLL may not need all N phase detectors. We call this type of designs the sub-sampling MPLL. An example of such a design was reported in [7]. It uses only one phase detector instead of eight phase detectors in the design that the $Ref$ frequency is eight times faster than VCO frequency. The main purpose of sub-sampling design is to minimize the hardware. This however comes with the exchange of the system dynamic and stability. When the number of phase detector employed is less than N, the sampling period will be longer than $Ref$ period $T_R$. In this case the clock phases must be selected in such a way that results in the uniform sampling period. The number of phase detector and clock phases used must be the power of 2 i.e. 1, 2, 4, 8 and so on. For the discrete-time system reducing the sampling rate can affect system stability. From the stability condition in Eq (27), it can be rewritten using the sampling period $T_n = (N/n)T$ where $n = \text{number of phase detector}$, as
Thus, for a given value of loop gain $K$, reducing number of phase detector will make the system less stable. Note that changing the sampling period in this case does not change the loop gain $K$ because we assume that the zero-order hold maintains the present sample until next sample is available.

**A.3.2 Transient Response**

In design of MPLL it is interesting to know not only the stability limit of the system but also its response to instantaneous change of input such as phase step and frequency step. The response in time-domain can be found from the inverse $z$-transform of the $H(z)\theta_i(z)$ where $\theta_i(z)$ is the $z$-transform of the interested input. The result typically cannot be expressed in a closed-form and requires numerical computation. In this section we show some of the simulation results of the response to a phase step and a frequency step. The results are obtained from the numerical evaluation of the linear difference equations described in the section 6. We use the ideal second-order analog PLL (APLL) as a reference for comparison among the MPLLLs with different number of phase detector. The APLL is based on the continuous-time approximation of the charge-pump PLL [5] that is optimized for $\zeta=0.707$. Then its loop components $K_d$, $R$, and $C$ are used for design the MPLLLs. The MPLLLs use the VCO that eight time slower than that of the APLL hence their VCO gain $K_{om} = K_\omega/8$. The number of phase detector used is 1, 2, 4 and 8. The designs with three different loop bandwidths are compared. Figure A.13 (a) – (c) show the responses to the input phase step $\pm \pi/2$ radian from the small to large loop bandwidth respectively. The time axis is shown in $k$: the number of clock cycle of the Ref. In Figure A.13(a), the $\omega_i/\omega_b =100$, thus the sampling rate is high compared with the loop bandwidth. Consequently, the responses are very closed to the APLL even when using only one phase detector. In Figure A.13 (b) and (c) the loop bandwidth are increased so that the $\omega_i/\omega_b$ is 50 and 10 respectively. This is equivalent to

$$K\tau \leq \frac{1}{N} \frac{2RC}{(N/n)T} \text{ or } \frac{\omega_i}{\omega_b} = \frac{\omega_i}{NK} \geq \frac{N}{n\pi} \quad (29)$$
move to the left closer to the stability limit line in Figure 8. Eventually, in Figure A.13 (c) the MPLL with one and two phase detectors cannot maintain its stability. For the response to the input frequency step, since the designs have different loop bandwidths, they are applied with the different input frequency step $\Delta \omega_i$ while keep the same ratio of the frequency step to the loop bandwidth, $\Delta \omega_i/\omega_b = \pm 2$. The results are shown in Figure A.13 (d)-(f) for $\omega_i/\omega_b = 100, 50$ and 10 respectively. The similar trend is observed as in the case of input phase step. Note that in both cases the settling time decreases as the loop bandwidth increases. However the settling time does not change in each MPLL when uses different number of phase detectors since in this case the loop bandwidth does not change as the sampling period changes.

From these results we can conclude that although the MPLL is a discrete-time system, in the case of small loop bandwidth i.e. $\omega_i>>\omega_b$, its transient response can be approximated by the ideal analog PLL. Additionally, the number of phase detector employed can be reduced to minimize the hardware while the PLL response is still acceptable. As the loop bandwidth increase or the sampling rate reduces, it shows the characteristic of the sampling system that is well described by discrete-time model and subject to its stability limit. Therefore, in the design by using discrete-time model, we can predict its response more accurate.

(a) $\omega_i/\omega_b = 100$, $\theta_c = \pm \pi/2$

(b) $\omega_i/\omega_b = 50$, $\theta_c = \pm \pi/2$
Figure A.13 (a), (b), and (c) Transient responses to the input phase step (d), (e), and (f) Transient response to the input frequency step. $k = t/T$
A.3.3 PLL with Adaptive Loop Bandwidth

It has been known that the loop bandwidth is the indicator of the PLL performances in terms of the input noise rejection and the system dynamic. A PLL with larger loop bandwidth has a faster acquisition and better tracking ability. In contrast, to have a good input noise rejection the PLL loop bandwidth should be as small as possible. Therefore it is a trade-off between these abilities. MPLL offers an alternative for the PLL to have both properties without compromising each one of them. It allows the loop bandwidth to be changed according to its circumstance. For example, in the beginning of the acquisition process the MPLL can be set to have the largest loop bandwidth and once the phase locking is achieved, it changed to a smaller loop bandwidth to have a better input noise rejection. This can be accomplished by changing the loop gain of the MPLL since the loop bandwidth is proportional to the loop gain.

Consider the model of MPLL in Figure A.9, it is composed of N phase detectors and N transconductance amplifiers. Each of them is active for one sampling period defined by $\phi_i \phi_{i+1}$. In the last section, the sub-sampling MPLL is achieved by using the number of phase detector less than N. However this does not change the loop bandwidth because as the sampling period increases the duration that the transconductance amplifier is active also increases proportionally. As a result, the loop gain remains the same. But if we increase the sampling period without changing the duration that the amplifier is active, then we effectively decrease the loop gain and so the loop bandwidth. Practically, this is quite simple to implement in MPLL since the active time of the amplifier is already defined by the available clock phase when all N of phase detector are used. Typically, when locking, the active time is equal to the period of the Ref. Therefore we need only to deactivate some of the phase detector appropriately for example reducing from 8 to 4 and 4 to 2 respectively. Finally, we note here that although the method to adjust the loop bandwidth is in effect decreasing the sampling rate of the PLL, it affects the stability of the MPLL less than the
case of the sub-sampling MPLL due to the fact that the loop gain is also decrease simultaneously.

Fig. 14 shows the frequency response of a MPLL when the number of phase detector that is active changes between one, two, four and eight. The MPLL is designed with the VCO frequency eight time slower than the input frequency \( \omega_i \). Therefore it has eight phase detectors. When all eight phase detectors are active, it has the maximum loop bandwidth equal to \( \omega_i/100 \). The minimum loop bandwidth is \( \omega_i/800 \) when it uses only one phase detectors. The simulation is based on the Eq(A25) of the section 6. It shows that the loop bandwidth decreases proportionally as the number of phase detector reduces. Note that the pass-band gain is approximately –18 dB because the ratio of the output phase to the input phase is one-eighth.

One concern however about the consequence of changing the loop bandwidth by changing the loop gain is the altering of the jitter peaking. As seen in Figure A.14, when the bandwidth decreases, the jitter peaking increases. The higher the peaking is the more jitter is amplified. This occurs not only for the MPLL but also for the second-order charge-pump PLL in general. In the continuous-time PLL, the peak is inversely proportional to the normalized loop gain. As expected, the similar result is observed here. Therefore in design procedure, the maximum peak must be considered when the PLL has the smallest bandwidth.

When we adjust the loop bandwidth the sampling rate of the MPLL is also changed simultaneously. Therefore, it is interesting to see how it affects the transient response. Figure A.15 shows the response to the frequency step \( \omega i/100 \) rad/sec of the MPLL when their loop bandwidths reduced from \( \omega i/20 \) to \( \omega i/160 \) rad/sec. Once again, we compare the results with the continuous-time charge pump PLL since its loop bandwidth is independent from the sampling rate (the sampling rate is always = \( \infty \)). As the bandwidth reduces, it takes both PLLs longer to regain their locked state. Their settling times are virtually the same. The effect of decreasing sampling rate is noticeable at the maximum overshoot. The different
between the maximum overshoot of APLL and MPLL at the same loop bandwidth increases as the sampling rate decreases.

![Figure A.14 The frequency response of MPLL as the loop bandwidth is adjusted](image)

**Figure A.14** The frequency response of MPLL as the loop bandwidth is adjusted

![Figure A.15 The transient response of MPLL and APLL with different loop bandwidths](image)

**Figure A.15** The transient response of MPLL and APLL with different loop bandwidths

### A.4 Application of the Model to the CDRs

In this section we will apply the model of MPLL to the CDR. We will show that in practice the linear sampling phase detection, when encounters with the random data, needs the extra time to process before it can generate the loop correcting signal. This additional processing
time results in the delay in the PLL model and can adversely affect the system performance. In addition, the application of the model to multi-level clock recovery and other practical issues such as the effect of data density are discussed.

Consider a CDR that has the input NRZ data with the bit rate of \( R \) bps. Therefore bit-time \( T_R \) is equal to \( 1/R \) second. The MPLL uses a ring oscillator that composes of \( N \)-stage differential delay cell. The oscillator provides total \( 2N \) output clock phases. Therefore they are equally separated from one to another by \( \pi/N \) radian. If the oscillation period is \( T_v \), the delay between each phase will be \( T_v/2N \). In order to have the phase-lock with the input data and be able to sample at each data bit these clock phase must be separated by one half of the bit-time and aligned with the input data as illustrated in Figure A.16 for the case of \( N = 8 \). Therefore in the locking state \( T_v/N = T_R \) or the oscillation frequency must be \( 1/N \) of the data rate.

![Figure A.16 Timing Diagram of NRZ and multi-phase sampling](image)

Because the input is random, the sample at the data crossing point alone as in the case of the periodic input is insufficient to determine whether VCO clock is leading or lagging the data. It needs to know if the transition is taking place and if there is a transition, it is a high-to-low or low-to-high transition. This information is obtained from the samples before and after the data crossing point, for example, in Fig.16 to extract phase error at the falling edge of \( \phi_2 \), it
needs to know the values of $d_0$ and $d_1$. This means the phase detector could not provide the output immediately after the VCO clock samples at the transition as it was previously assumed. It has to wait until all three samples are available and processed by the decision-making logic to produce the appropriate control signal for the charge-pump circuit. The delay between the time that the transition is sampled and the charge-pump circuit (or the transconductance amplifier) receives its control signal, if comparable to the sampling period, needs to be included into the model. This delay is composed of one half of the bit-time delay for the third sample to be available and the gate delay of the decision-making logic. Assume that gate delay is small and less than one half of the bit-time, hence the control signal for the charge-pump circuit will be ready after the total delay of one bit-time (one sampling period). This means the phase detection scheme initiates the loop correcting signal one bit-time after it detects the phase error. Consequently, we modify the model of time interleave sampling in Figure A.11 by inserting one sampling period delay after the impulse sampling.

Another issue that needs an attention is the missing transition of the random data. In [6], it is reflected in the loop gain as the $K_d$ is multiplied by data density factor: $d$, where $0 < d \leq 1$ ($d = 1$ meaning there is a transition for every bit i.e. stream of ..10101..). In our analysis, however, the zero-order hold is included in the model, the absent of the transition results in the output of the zero-order hold equal to zero. Thus in the long-term average, it eventuates to both the decreasing of the loop gain and the increasing of sampling period simultaneously. Consequently, it is more accurate to model this effect by multiplying $K_d$ with $d$, and $T$ with $1/d$. The linear model of a CDR that uses MPLL and includes the effects of the delay and the data density is illustrated in Figure A.17 where $T_d = (1/d)T$ and $\bar{K}_d = dK_d$. 
The extra one bit-time delay is modeled with $z^{-1}$. Therefore, the open loop gain $G(z)$ has an additional pole at the origin on the $z$-plane. This results in adding a closed-loop pole on the positive real axis. The present of this pole degrades the transient response of the system as it increases the maximum overshoot and the settling time. To examine the system stability, we find the system characteristic equation, which is

$$D(z) = z^3 - 2z^2 + (N\beta + 1)z + N(\alpha - \beta)$$  \hspace{1cm} (30)$$

where $\beta$ and $\alpha$ has the same definition as in Eq(17) except replacing $T$ and $K_d$ with $T_d$ and $dK_d$. Using the root locus technique, one of possible root locus of Eq (30) is plotted in Figure A.18 for $d=1$. It shows that as the loop gain increases the pole due to the delay moves from the origin to the open loop zero while the other two poles at $z = 1$ migrate outside the unit circuit. The stability limit is found to be

$$K_T \leq \frac{1}{d} \frac{1}{N} \frac{\frac{1}{2} - \frac{3}{2} \left(\frac{\pi}{d\omega_i\tau}\right)}{\frac{n}{d\omega_i\tau} \left(1 - \frac{\pi}{d\omega_i\tau}\right)^2} = \frac{1}{d} \frac{1}{N} \frac{RC - \frac{3}{2}T_d}{T_d \left(1 - \frac{T_d}{2RC}\right)^2}$$  \hspace{1cm} (31)$$
As $\omega_i >> \pi/RC$, it can be simplified to $\frac{\omega_i}{NK} \geq \frac{1}{2} \frac{N}{n} \pi$. Thus, due to the delay its stability region is reduced approximately by half.

Figure A.18 Root locus plot of the CDR using multi-phase PLL

The product of $NK\tau$ is plotted as a function of $\omega_i\tau$ with $d = 1$ and 0.5 are shown in Figure A.19. In this plot we assume that all $N$ phase detectors are used. The solid line is the ideal case of MPLL where the input $Ref$ is periodic and the error signal is produced immediately after the sampling. The stability is degraded as the delay is taken into account as shown by the dashed lines. This can be understood by simply considering the fact that the PLL is a system with the negative feedback. Therefore, the delay of the correcting signal will result in the delay of the feedback signal that can possibly become the positive feedback. It also creates a constraint for the minimum frequency of the input $Ref$. By evaluating Eq(31) with condition $K\tau \geq 0$, it is found that $\omega_i \geq 3\pi/(2RC)$. The last curve combines the effect of both delay and data density. The effect from the data density causes the minimum frequency of $Ref$ to increase to be $3\pi/(d2RC)$.
Besides the two-level NRZ data, the linear sampling phase detection and its model can be applied to the CDR that uses the multi-level signal such as 4-PAM in [11] as well. However, because the input data has multiple amplitudes, only certain type of data transitions can be used to extract phase error. As a result, unless the data is encoded, the data density factor will be smaller than NRZ data.

**Non-linear Type MPLL-based CDR**

This type of CDR differs from the linear type in that it digitally samples the input at the data transition. Therefore it cannot extract the amount phase error but it can detect whether the phase error is positive or negative by comparing three successive samples. The loop then corrects itself by pumping either a positive or negative constant current pulse to the loop integrator. As a result of the fixed current pulse, the input-output characteristic of the phase detector is a step resembling a 1-bit quantizer. In other word the phase detector function as the 1-bit phase quantizer. Instead of pursuing the exact analysis of this non-linear system, which is complicated, we propose a possible alternative to analyze by using the model that we have developed. The technique is to linearize the non-linear phase detector to be the
linear sampling phase detector and the quantization noise source. Therefore the non-linear CDR can be modeled as the linear CDR in Figure A.17 with an additional input, the additive current noise source, placed between the $K_d$ and the LPF block. The analysis can be carried out depending upon the assumptions of the quantization noise in terms of its statistical distribution, its power spectrum and its correlation to the other input $\phi_d(t)$.

**A.5 Conclusion**

A multi-phase PLL achieves phase lock by utilizing the multiple clock phases to sample an input signal. Through use of the multiple phase sampling, a slow oscillator can be used to recover the phase error from a high frequency input. The operation of the multi-phase PLL is based on time-interleaved sampling. Its behavior can be neither described nor predicted accurately with the existing PLL models. Therefore, we have developed a new model, based on the discrete-time linear system. This model takes into account the sampling nature of the loop, which provides greater insight into the system behavior and an understanding of system constraints. The discrete-time analysis shows the conditions for the MP LL to be stable in terms of input frequency, loop bandwidth and the number of phase detectors. Ultimately this knowledge can be used to define the maximum allowable loop bandwidth of the MP LL. When the loop bandwidth is much smaller than the input frequency the system response can be approximated by the continuous-time model. The number of phase detector employed can be reduced to minimize the hardware. As the loop bandwidth increases the response differs from the response of the continuous-time PLL. Eventually, the system reaches its stability limit, which cannot be predicted by the continuous-time model. The model increases its accuracy when applied to the CDR by including the effect of the input data density and the delay inside the loop. It shows that the CDR system becomes the third-order, less stable and has additional constraint on the minimum input frequency.

Three configurations of MP LL are also described. The first configuration all the N phase detectors are used, thus in the locked condition the system sampling period will be equal to
the period of the input. It behaves as a regular PLL. The second configuration is the *sub-sampling* MPLL, which is designed to employ less than N phase detectors to reduce the hardware. In this case the sampling period is multiple of the input period and the charge-pump circuit provides the output current continuously over that sampling period. This causes the PLL bandwidth to remain constant. The last arrangement is the *adaptive loop bandwidth* configuration. In this case, the duration that the charge-pump is active is constant while the sampling period is adjusted in order to change the loop bandwidth by either decreasing or increasing the number of active phase detectors.

### A.6 The Difference-Equation Analysis of the Linear Sampling PLL

This section derives the linearized difference equations with constant coefficient of the second-order linear sampling PLL and multi-phase PLL. The analysis is based on the outline of the analysis of the charge-pump PLL in [5]. The purpose is to shown that with the same approximations the frequency domain transformation approach and the time-domain approach both conclude the same result. Additionally, the result of this analysis is used for calculation the example of the transient responses of the model.

#### Linear Sampling PLL

Let \( \theta_i(t) \): phase of Ref

\( \omega_i \): frequency of the Ref which is constant

\( \theta_o(t) \): phase of VCO

\( \theta_{\varepsilon}(t) \): phase error = \( \theta_i(t) - \theta_o(t) \)

\( \omega_c \): free running frequency of the VCO

\( v_c(t) \): loop filter output (Vcontrol)

\( v_x(t) \): voltage drop across loop capacitor

\( i_o(t) \): transconductant amplifier output
Figure A.20 The transconductance amplifier and the loop filter

Suppose the initial state start at \( t = 0 \). At \( t > 0 \) the input phase to the PLL is

\[
\theta_i(t) = \theta_i(0) + \omega_i \cdot t \tag{A1}
\]

and the output phase of PLL is

\[
\theta_o(t) = \theta_o(0) + \omega_o \cdot t + K_o \int_0^t v_i(\tau) d\tau \tag{A2}
\]

where \( K_o \) is the VCO gain. Refer to Figure A.20 the \( v_c(t) \) is found to be

\[
v_c(t) = i_o(t) R + \frac{1}{C} \int_0^t i_o(\lambda) d\lambda + v_i(0) \tag{A3}
\]

Substitute (A3) in (A2), we find

\[
\theta_o(t) = \theta_o(0) + \omega_o \cdot t + K_o \int_0^t i_o(t) R + \frac{1}{C} \int_0^t i_o(\lambda) d\lambda + v_i(0) \bigg) d\tau
\]

The amplifier output current is constant until the next sampling, hence \( i_o(t) = i_o \). As the current \( i_o \) flows to the loop filter, the voltage drop across the capacitor change to be
\[ v_x(t) = \frac{1}{C} i_o t + v_x(0) = \frac{1}{C} K_d \theta_x(0) t + v_x(0) \]  

(A4)

So the PLL output phase

\[ \theta_o(t) = \theta_o(0) + \sigma \varphi t + K_o \left( i_o R t + \frac{1}{C} i_o \frac{t^2}{2} + v_x(0) t \right) \]  

(A5)

Assume that at small phase error, \( \Delta t \equiv (T/2\pi) \theta_e(t) \) and the sampling interval \( T \pm \Delta t \equiv T \), the period of Ref. Thus for \( 0 < t < T \), substituting \( i_o = K_d \theta_e(0) \), where \( K_d = gm M(T/2\pi) \) as defined in (6). Therefore

\[ \theta_o(t) = \theta_o(0) + \sigma \varphi t + K_o \left( K_d \theta_e(0) R t + \frac{1}{C} K_d \theta_e(0) \frac{t^2}{2} + v_x(0) t \right) \]  

(A6)

Eq(A4) and Eq(A6) describe the system when \( 0 < t < T \) in term of its initial condition at \( t = 0 \). In this case only two state variables \( \theta_o \) and \( v_x \) are sufficient as it is a second-order system. Evaluating these equations at the end of sampling interval i.e. \( t = T \), the result will become the initial conditions for the next sampling interval i.e. \( T < t < 2T \). At \( t = T \), Eq(A5) and Eq(A6) become

\[ \theta_o(T) = \theta_o(0) + \sigma \varphi T + K_o K_d (RT + \frac{1}{C} \frac{T^2}{2}) \theta_e(0) + K_o v_x(0) T \]  

(A7)

\[ v_x(T) = \frac{1}{C} K_o \theta_e(0) T + v_x(0) \]  

(A8)

The phase error can be found from \( \theta_e(T) = \theta_i(T) - \theta_o(T) \). Since in one sampling period phase of Ref increases by \( 2\pi \), therefore \( \theta_e(T) = (\theta_i(0) + 2\pi) - \theta_o(T) \).

\[ \theta_e(T) = \theta_e(0) + 2\pi + \sigma \varphi T + K_o K_d (RT + \frac{1}{C} \frac{T^2}{2}) \theta_e(0) + K_o v_x(0) T \]  

A9
The Eq(A7), Eq(A8) and Eq(A9) are used for calculating the transient response.

Similarly, at \( t = 2T \),

\[
\theta_o(2T) = \theta_o(T) + \sigma_e T + K_o K_d (R T + \frac{1}{C} \frac{T^2}{2}) \theta_e(T) + K_o v_e(T) T
\]  
\[\text{(A10)}\]

\[
v_e(2T) = \frac{1}{C} K_d \theta_e(T) T + v_e(T)
\]
\[\text{(A11)}\]

Subtracting Eq(A10) by Eq(A7), we find

\[
\theta_o(2T) - \theta_o(T) = \theta_o(T) - \theta_o(0) + K_o K_d (R T + \frac{1}{C} \frac{T^2}{2}) [\theta_e(T) - \theta_e(0)] + K_o T [v_e(T) - v_e(0)]
\]
\[\text{(A12)}\]

The Eq(A11) and Eq(A12) can be written in term of \( kT \) where \( k = 0, 1, 2, \ldots \), For convenience \( T \) are omitted, thus we have

\[
v_e(k+1) = \frac{1}{C} K_d \theta_e(k) T + v_e(k)
\]
\[\text{(A13)}\]

and

\[
\theta_e(k+2) - \theta_e(k+1) = \theta_e(k+1) - \theta_e(k) + K_o K_d (R T + \frac{1}{C} \frac{T^2}{2}) [\theta_e(k+1) - \theta_e(k)] + K_o T [v_e(k+1) - v_e(k)]
\]
\[\text{(A14)}\]

Taking z-transform of Eq. (A13) and Eq.(A14) yield

\[
z v_e(z) = \frac{1}{C} K_d \theta_e(z) T + v_e(z)
\]
\[\text{(A15)}\]

\[
z^2 \theta_e(z) - z \theta_o(z) = z \theta_e(z) - \theta_o(z) + K_o K_d (R T + \frac{1}{C} \frac{T^2}{2}) [z \theta_e(z) - \theta_e(z)] + K_o T [z v_e(z) - v_e(z)]
\]
\[\text{(A16)}\]
Substituting \( \theta_s(z) = \theta_i(z) - \theta_o(z) \) in Eq.(A15) and Eq.(A16) and solving for the system transfer function results in
\[
\frac{\theta_s(z)}{\theta_i(z)} = \frac{K_o K_d (RT + \frac{T^2}{2C})(z-1) + K_o K_d \frac{T^2}{C}}{(z-1)^2 + K_o K_d (RT + \frac{T^2}{2C})(z-1) + K_o K_d \frac{T^2}{C}}
\] (A17)

Eq.(A17) is the same as Eq.(17) after defining \( \beta = K_o K_d (RT + \frac{T^2}{2C}) \) and \( \alpha = K_o K_d \frac{T^2}{C} \)

**Multi-phase PLL**

Multi-phase PLL is the time-interleaved operation of several linear sampling PLL. In multi-phase PLL there are three possible configurations. The first case, all the N phase detectors are used, thus in the locked condition the sampling period will be equal to the Ref period. The second case is the sub-sampling MPLL, which is the PLL is designed to have less than N phase detectors. As a result, the sampling period is multiple of Ref period. In this case, the charge-pump circuit provides the output current continuously over that sampling period. So the PLL bandwidth remains constant. The last setup is the adaptive loop bandwidth PLL. The duration that the charge-pump is active stays constant while the sampling period is adjusted in order to change the loop bandwidth by either decreasing or increasing the number of phase detector to be active. The analysis that cover all three cases are as following. In addition to the previously defined variable,

let \( \omega_o \): VCO frequency

\( N \): \( \omega_1 / \omega_o \)

\( \theta_o(t) \): phase error = \( \theta_i(t) - N \theta_o(t) \)

\( m \): number of phase detector used

\( T_V \): VCO period = \( 2 \pi / \omega_o \)

\( T_R \): Ref period = \( 2 \pi / \omega_1 \)
\[ T_p: \] length of time that charge-pump is active  
\[ T_m: \] sampling period \( T_m = \left(\frac{N}{m}\right) T_R \)

The current and voltage waveforms at the loop filter are drawn Figure A.21. In each sampling period \( T_m \) the amplifier output current is valid for \( T_p \). The VCO output phase and the voltage drop across the capacitor are found to be

For \( 0 \leq t \leq T_p \)

\[
\theta_o(t) = \theta_o(0) + \omega_c t + K_o \left( i_o R t + \frac{1}{C} i_o \frac{I^2}{2} + v_s(0) t \right)
\]

\[
v_s(t) = \frac{1}{C} i_o t + v_s(0)
\]

Therefore, at \( t = T_p \)

\[
\theta_o(T_p) = \theta_o(0) + \omega_c T_p + K_o \left( i_o R T_p + \frac{1}{C} i_o \frac{T_p^2}{2} + v_s(0) T_p \right) \quad (A18)
\]

\[
v_s(T_p) = \frac{1}{C} i_o T_p + v_s(0) \quad (A19)
\]

And for \( T_p < t \leq T_m \)

\[
\theta_o(t) = \theta_o(T_p) + \omega_c (t - T_p) + K_o v_s(T_p)(t - T_p) \quad (A20)
\]
\[ v_s(t) = v_s(T_p) = v_s(T_m) \]  \hspace{1cm} (A21)

Evaluation of the Eq(A20) at \( t = T_m \), the end of sampling period, by substituting \( \theta_o(T_p) \) and \( v_s(T_p) \) from Eq(A18) and Eq(A19) yields

\[
\theta_o(T_m) = \theta_o(0) + \sigma \omega_o T_p + K_o \left( i_o R T_p + \frac{1}{C} i_o T_p^2 \right) + \left( \omega_o + \frac{1}{C} i_o T_p + v_s(0) \right)(T_m - T_p) \hspace{1cm} (A22)
\]

Since \( i_o = K_d \theta_e(0) \), thus

\[
\theta_e(T_m) = \theta_e(0) + \sigma \omega_e T_p + K_e K_d \left( R T_p + \frac{1}{C} T_p^2 \right) \theta_e(0) + K_e v_e(0) T_p + \left( \omega_e + \frac{1}{C} K_e K_d \theta_e(0) + v_e(0) \right)(T_m - T_p) \hspace{1cm} (A23)
\]

Because the number of phased detector used is \( m \leq N \), the sampling period \( T_m \geq T_R \).

Therefore during time span of \( T_m \) the input phase advances for \( 2\pi N/m \) radian. From \( \theta_e(t) = \theta_i(t) - N \theta_o(t) \), evaluating at \( t = T_m \) gives \( \theta_o(T_m) = \theta_i(0) + 2\pi N/m - N \theta_o(T_m) \). Substitute \( \theta_o(T_m) \) from (A23) and rearrange. Finally we get

\[
\theta_o(T_m) = \theta_i(0) - N \left( \sigma \omega_i - \frac{2\pi}{m} + K_e K_d \left( R T_p + \frac{1}{C} T_p^2 \right) \theta_i(0) + K_e v_e(0) T_p + \left( \omega_e + \frac{1}{C} K_e K_d \theta_e(0) + v_e(0) \right)(T_m - T_p) \right) \hspace{1cm} (A24)
\]

The Eq(A21), Eq(A23) and Eq(A24) are used to determine the transient response of the multi-phase PLL at the sampling instant. To determine the system transfer function, write Eq(A21) and Eq(A23) in term of sampling index \( k \)

\[
v_s(k+1) = \frac{1}{C} i_o T_p + v_s(k) \]
\[
\theta_s(k+1) = \theta_s(k) + \theta_s T_p + \theta_s K_d \left( R T_p + \frac{1}{2} T_p^2 \right) \theta_s(k) + K_s v_s(k) T_p + \left( \alpha + \frac{1}{C} K_s K_d T_p \theta_s(k) + v_s(k) \right) (T_m - T_p)
\]

Taking z-transform and solving for the system transfer function yields

\[
\frac{\theta_s(z)}{\theta_i(z)} = \frac{\{K_s K_d (R T_p + \frac{T_p^2}{2 C}) + K_s K_d \frac{T_p (T_m - T_p)}{C}\} (z-1) + K_s K_d \frac{T_p (T_m - T_p)}{C} + K_s K_d \frac{T_p^2}{C}}{(z-1)^2 + N \{(K_s K_d (R T_p + \frac{T_p^2}{2 C}) + K_s K_d \frac{T_p (T_m - T_p)}{C}\} (z-1) + N \{K_s K_d \frac{T_p (T_m - T_p)}{C} + K_s K_d \frac{T_p^2}{C}\}}
\]

\((A25)\)

This is the system transfer function of multi-phase PLL that covers all three configurations. For example, in the first configuration all N phase detectors are used \( T_p = T_m = T_R \), thus the Eq(A25) is simplified to Eq(25). In sub-sampling PLL that used \( m \) phase detectors, \( T_p = T_m = (N/m)T_R \). Finally, in the adaptive loop bandwidth PLL, \( T_p \) is fixed, and usually chosen to be equal to \( T_R \). \( T_m \) is still equal to \((N/m)T_R\) but \( m \) is varied from 1 to \( N \).

A.7 References


