ABSTRACT

MICK, STEPHEN EDWARD. Analysis and Design Considerations for AC Coupled Interconnection Systems. (under the direction of Paul D. Franzon)

As the process technologies for microelectronic integrated circuits continue to improve, both the amount of integrated, on-chip functionality and the number of required off-chip interconnections (I/O) will continue to increase. These I/O will not only become more numerous but also will need to be packed densely and be capable of operating both with high bandwidth and low power. Packaging technology research is aimed at increasing I/O density and circuit research is underway to improve the bandwidth and power performance of I/Os. Advances are being made in each of these areas, but industrial roadmaps predict that these advances will not keep pace with the needed improvements. The research in this dissertation addresses this widening technological gap.

The central thesis in this work hinges on the recognition that arrays of densely packed, low-power, high-bandwidth I/Os can be created if the physical structure of each I/O is optimized for the type of information it must transmit. For example, the DC component of digital signals carries no information. Instead, digital signals contain information at frequencies well above DC (where the exact frequency spectrum of the information depends upon the edge rate of the data transitions). This can be exploited by recognizing that AC information can be transmitted across a boundary with non-contacting structures such as two plates of a capacitor or two coupled inductors. An I/O array can then be built with non-contacting structures for AC signals and direct contacts such as solder bumps

only where DC signal transfers are needed. In this way, AC signal paths are freed from the mechanical constraints of direct, contacting structures and both the compliance and rework problems encountered in other high density interconnect technologies can be alleviated.

Capacitive and Inductive AC Coupled Interconnections are extensively analyzed and measured in this work and presented as a means to provide an array of sub-100μm pitched, low-power, multi-gigabit per second per pin interconnections. A packaging structure that enables AC Coupled Interconnections is also presented.

ANALYSIS AND DESIGN CONSIDERATIONS FOR AC COUPLED INTERCONNECTION SYSTEMS

by
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DEDICATION

To Julie whose love and constant encouragement made this work possible.

BIOGRAPHY

Stephen Mick son of Dennis and Deborah Mick was born in August 1972 in Pasadena, Texas. In June of 1995, Stephen married Julie Miller and in December of that same year earned his B.S. in Electrical Engineering from the University of Houston. While completing his undergraduate degree, Stephen worked for three semesters at Texas Instruments as part of the cooperative education program. After graduation he continued working at Texas Instruments until he and his wife moved to North Carolina to continue their respective educations. Stephen earned his M.S. in Electrical Engineering from North Carolina State University in December 1998 and then investigated several possible Ph.D. research topics and interned for LSI Logic in 1999 before beginning his work in the area of AC Coupled Interconnections.

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Foremost I would like to thank God the Father for His grace, constant provision, answered prayer and redemption through the death and resurrection of the Lord Jesus Christ. Not only is faith in Christ eternally significant but also it has shaped my life and helped me to keep perspective when graduate school seemed overwhelming.

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Chapter 1 Introduction

1.1 Problem Statement

The demand is increasing rapidly for high density, high bandwidth off-chip I/O. Though the average densities implied by the ITRS roadmap are not too different from solder bump densities achievable today, the peak I/O densities in future products are expected to present a technological barrier to existing interconnection methodologies [1].

Many researchers are addressing the need for increased I/O density by trying to find methods to manufacture cost-effective, reliable solder bump interconnections with a pitch of 100μm or less. However, there are many known difficulties with achieving such pitches [2, 3, 4]. The compliance issues faced by small solder bumps are well known, and many attempts have been made to produce high aspect ratio solder bumps with some success but little impact due to manufacturing cost issues. A new process presented here uses buried solder bumps in conjunction with AC coupled interconnects to solve the problems introduced by continually shrinking the size and pitch of solder connections with current solder bump technologies.

In addition to increasing I/O density, a number of circuit design researchers are trying to develop methods to increase the bandwidth of each I/O by building new circuit topologies capable of multi-Gbps signaling. Approaches being explored include source-synchronous techniques to limit the effects of clock skew [5]; small-swing differential techniques to improve toggle rate and power-per-bit [6]; and equalization to compensate for the skin effect [6].

The structure presented in this dissertation recognizes that the goals of high density and high bandwidth can be achieved simultaneously by optimizing the interconnection structure for each type of signal that needs to be carried off-chip. That is, DC signals can be communicated by direct, mechanical connections and AC signals can be communicated off-chip by AC coupled connections. However, new transceiver circuits must be developed to exploit the properties of AC Coupled interconnections and a physical structure must be developed that provides an interface between chip and substrate compatible with the requirements of both DC and AC connections.

The structure developed in this dissertation will presently allow for 2533 I/O in a 310mm^2 chip area where 844 of the I/O are direct mechanical connections for DC signals and each of the remaining I/Os provide a fully differential, non-contacting AC signal path. This density exceeds the needs stated by the ITRS industry roadmap for several years into the future [1]. Moreover, the AC coupled structures presented here can support data rates of at least 6Gbps per I/O. Thus, this structure enables both high density and high bandwidth interconnections.

1.2 Motivation and Objectives

The research presented in this dissertation has been guided by several system-level goals. For example, it is a goal to develop a system that supports a high-density of interconnections (meeting the ITRS packaging roadmap) and that can communicate data at high bandwidths (≥ 3 Gbps) with low power (~40 mW per I/O). To this end, coupling elements suitable for implementation in both CCI and LCI system have been developed and characterized. A substrate fabrication process to support AC Coupled systems has been designed and transmission lines in this process have been characterized. Although development continues on this substrate process, the work in this dissertation will provide future researchers with design guidelines and experimental results necessary to develop a complete system.

1.3 Dissertation Overview

The ultimate goal of investigating AC Coupled systems is the development of high-speed, low-power, chip-to-chip communication systems with dense arrays of I/Os. The concepts of AC signal coupling, integrated coupling elements, and packaging are fundamental to the work presented in this dissertation and Chapter 2 reviews previous work in each of these areas.

Analysis of both capacitive and inductive ACCI systems is presented in Chapter 3 and measurements are presented in Chapter 4. System integration issues such as packaging, routing and coupling element density are presented in Chapter 5. The dissertation is concluded with suggestions for future work in Chapter 6.

1.4 Original Contributions

The original contributions of this research are subdivided into categories relating to specific aspects of this research.

1.4.1 AC Coupling

- Demonstration of 6Gbps NRZ data transmission through a series of two capacitively-coupled stages through an off-chip connection
- Analysis of coupled inductor model culminating in simulations showing feasibility of 5Gbs uncompensated signaling through inductively coupled channels.
- Performance comparison between capacitively and inductively coupled interconnections

1.4.2 Coupling Elements

- Development and validation through measurements of a model for coupled inductors

1.4.3 Packaging

- Design and prototype of buried solder bump package
- Co-development of a substrate fabrication process and transmission lines to support AC Coupled interconnections

1.5 Publications

To date, Mr. Mick's work has been published in a peer-reviewed journal, conference proceedings, and has been presented numerous times. A patent application has been filed on the work presented in this dissertation related to integrating AC Coupling with a new package structure.

1.5.1 Journals

Mick, S., Luo, L., Wilson, J., and Franzon, P., "Buried Bump and AC Coupled Interconnection Technology", *IEEE Transactions on Advanced Packaging*, 27(1), Feb 2004.

1.5.2 Conferences

Franzon, P., Kingon, A., Mick, S., Wilson, J., Luo, L., Chandrasekar, K., Bonafede, S., Statler, C., LaBennett, R., "High Frequency, High Density Interconnect Using AC Coupling", *MRS 2003 Symposium B: Materials, Integrations, and Packaging Issues for High-Frequency Devices*, Invited Paper, B6.1, Materials Research Society, Boston, Dec 1-5, 2003.

Franzon, P., Mick, S., Wilson, J., Luo, L., Chandrasekar, K., "AC Coupled Interconnect for High-Density High-Bandwidth Packaging", *2003 International Conference on Solid State Devices and Materials*, Tokyo, Japan, Sept. 16-19, 2003.

Mick, S., Wilson, J., Luo, L., Chandrasekar, K., Franzon, P., "AC Coupled Interconnect for Dense 3-D Systems", *IEEE Nuclear Science Symposium Medical Imaging Conference 13th International Workshop on Room-Temperature Semiconductor X- and Gamma Ray Detectors*, Session N7-3, IEEE, Portland, Oregon, Oct 19-25, 2003.

Mick, S.; Franzon, P.; “Design Guidelines for Inductive AC Coupled Interconnects”, *SRC Techcon 2003*, Semiconductor Research Corporation, Dallas, Texas, Aug 2003

Mick, S.; Luo, L.; Wilson, J.; Franzon, P.; “Buried Solder Bump Connections for High-Density Capacitive Coupling”, *Proceedings of the IEEE Electrical Performance of Electronic Packaging Conference*, IEEE, Monterey, California, Sept. 2002, pp 205-208.

Mick, S.; Franzon, P.; Huffman, A. “Packaging Technology for AC Coupled Interconnection”, *Flip-Chip Technology Workshop 2002, Proceedings of the International Microelectronics And Packaging Society*, IMAPS, Austin, Texas, June 2002.

Mick, S.; Wilson, J.; Franzon, P.; “4 Gbps high-density AC coupled interconnection”, *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference*, Invited Paper, IEEE, Orlando, Florida, May 2002, pp 133-140. Excerpts reprinted as Mick, S., Wilson, J., and Franzon, P., "AC scheme bumps I/O density," *EE Times*, 1218, CMP / United Business Media, May 13, 2002, pp 67,72.

Mick, S.; Franzon, P.; “AC Coupled Interconnect”, *SRC Techcon 2001*, Semiconductor Research Corporation, Dallas, Texas, Sept. 2001.

1.5.3 Presentations

This research has been presented on numerous occasions to industry partners and to funding agencies. Following is a list of presentations Mr. Mick has made:

“ACI for Space Electronics: Inductively-Coupled Circuit Issues”, US Air Force Program Review, September 2003, Raleigh

“AC Coupled Interconnect”, Tasks 1094.001 and 1094.002, SRC ICSS Program Review, September 2003, Seattle

“Design Considerations for Inductive AC Coupled Interconnect”, SRC Techcon, August 2003, Dallas

“AC Coupled Interconnect”, Task 722.001, SRC Back-end Packaging Program Review March 2003, Tucson

“AC Coupled Interconnect”, Task 722.001, SRC Back-end Packaging Program Review March 2002, Urbana-Champaign

“AC Coupled Interconnect”, Cisco, Nov 2000, RTP

1.5.4 Patent

Buried Solder Bumps for AC-Coupled Microelectronic Interconnects; SRC Patent ID: P0237; Inventors: Franzon, NC State; Mick, NC State; Wilson, NC State; File Date: 28-Nov-2001; Task 722.001

Chapter 2 Literature Review

2.1 Overview

The demand is increasing rapidly for high density, high bandwidth off-chip I/O. Though the average I/O densities implied by the ITRS roadmap are not too different from solder bump densities achievable today, the peak I/O densities in future products are expected to present a technological barrier to existing interconnection methodologies [1]. AC Coupled interconnects can provide a solution to this technological barrier. A complete AC Coupled system is composed of a transceiver, capacitive or inductive coupling elements and interconnections. Opposing metal plates on two ICs or on an IC and a substrate being brought into close and controlled proximity can create the capacitive coupling elements needed to implement an AC Coupled system. Similarly, opposing inductors on two ICs or on an IC and a substrate being brought into close and controlled proximity can form inductive coupling elements. The transceiver must be designed to compensate for the frequency response of the coupling elements and interconnections.

The ultimate goal of investigating AC Coupled interconnects is to support the development of a high-speed, low-power, chip-to-chip communication system with dense arrays of I/Os. Given the function and composition of such a system, the concepts of AC coupling of signals, integrated coupling elements (both capacitors and coupled inductors) and packaging are fundamental to the work presented in this thesis. A rich body of literature exists in each of these areas, and no single body of literature pulls together the information necessary to employ coupling elements and interconnections in the creation of a high-density, high bandwidth chip-chip communication system. Instead, innovations in each area must be reviewed to reveal the issues to be considered when designing an AC Coupled communication system.

2.2 AC Coupled Interconnection

The basic concept of AC coupling exploits the fact that capacitors placed in series or coupled inductors placed in parallel with an AC signal trace can block any DC voltage while passing the AC voltage. Both capacitive and inductive signal coupling can be used to transmit signals containing AC information across an interface where no direct physical connection exists. AC Coupling can be exploited in both on-chip and off-chip applications. Moreover, it can be used to transmit information across a chip-chip or chip-substrate boundary.

2.2.1 Capacitive Coupling

The simple process of capacitive AC coupling has found use in numerous applications. High power DC-DC converters can employ capacitive coupling to store and to commute energy [7]. Coupling capacitors can be used

to provide frequency compensation to op-amps [8]. Consecutive stages of multi-stage analog circuits exploit series coupling capacitors to keep the DC biases from the various stages isolated [9].

Gabara explored a quantized feedback receiver topology that used an integrated on-chip coupling capacitor with one side of the capacitor connected directly to an I/O pin and the other side connected to the input of the receiver [10]. Gabara's technique re-established a local DC level at the receiver thereby enabling non-encoded data to be recovered across a wide frequency range (2000Hz – 800MHz) [10].

Capacitive coupling does not have to be confined to capacitors that are completely on-chip. Instead, capacitive coupling can take advantage of the fact that two metal plates will form a capacitor when brought into close proximity of each other. Metal plates can be fabricated on either side of a physical interface and when the two surfaces are brought close enough to each other and the metal plates aligned, a capacitor is formed. AC coupling can be realized if this capacitor is connected as a series circuit element as illustrated in Figure 1. Capacitive coupling can be exploited in this way to transmit electrical signals from a rotating shaft to a stationary receiver [11]. It can also be used for IC boundary scan testing [12]; as a position sensor [13]; to directly couple signals in 3D packaging [14]; and to communicate information between multiple ICs [15, 16].

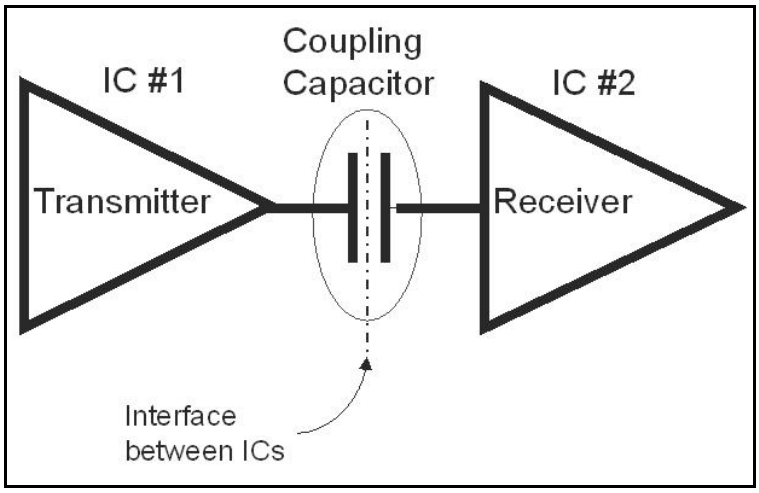


Figure 1: Illustration of AC Coupled Interconnection using series, trans-chip capacitive coupling elements

Knight proposed using capacitive coupling across a physical interface as a means to transmit signals between multiple ICs on a common MCM substrate [15]. In this implementation, Knight claimed that signals could be communicated between ICs along terminated transmission lines on a common substrate with low power (15mW per differential pair) and high data rates (1Gbps). Schaffer provided analysis of the signal-to-noise ratios (and hence the I/O density) that can be realized with direct chip-chip capacitive coupling [17]. Mick et al

demonstrated chip-chip capacitive coupling at data rates of 4Gbps NRZ [18]. Kanda continued with this idea and proposed an implementation of capacitive coupling in the context of 3D IC packaging [19].

Kuijk et al. reported using capacitive coupling to connect the output of a silicon, CMOS ring oscillator to a diode rectifier fabricated on a III-V substrate [16]. The researchers aligned metal plates on the top surfaces of each of the silicon and III-V substrates and brought the ICs into close proximity of each other. They suspended the two ICs from each other by creating a gap filled with a high permittivity, liquid dielectric to increase the coupling capacitance. The resulting structure was then sealed to prevent the dielectric from leaking out from between the two ICs.

Implementations of capacitive coupling across an interface are not restricted to point-to-point connections. Chang has proposed using capacitive coupling as a means to transmit multiple CDMA data signals between ICs along a single, common substrate transmission medium [20].

2.2.2 Inductive Coupling

Inductive coupling is often treated as a parasitic effect for on-chip wiring [21, 22, 23]. However, intentional (rather than parasitic) inductive coupling has found use in many applications. On-chip coupled inductors (i.e. transformers) find use in distributed power amplifiers [24], LNAs [25, 26], and mixers [27].

Wong et al. recognized that the capacitance between two on-chip, vertically-aligned, coupled inductors cannot be ignored. These researchers used the phrase "capacitively coupled transformer" to describe the on-chip capacitor / transformer hybrid that they designed and characterized for use in an LNA [26].

Like capacitive coupling, inductive coupling does not have to be confined to coupling elements that are completely on- or off-chip. Inductive coupling can take advantage of the fact that two inductors will form a transformer when brought into close proximity of each other. Individual inductors can be fabricated on either side of a physical interface and when the two surfaces are brought close enough to each other and the coupling elements aligned, a transformer is created. AC coupling can be realized if this transformer is connected as a circuit element as illustrated in Figure 2.

AC coupling between ICs with inductive elements has found many applications. For example, Chuah et al. reported a strain measurement system designed to be embedded in concrete that transferred both power and a signal across an inductively coupled-interface. [28]. Glaser reported work to transfer power and all I/O signals with inductive coupling and thereby eliminate the need for any physical interconnections [29]. In Glaser's work the on-chip inductor for power transmission was 30 turns, 24μH, 33mm^2 and operated at 980kHz. The on-chip inductor for bi-directional communication was 10 turns, 3μH, 26.8mm^2, and operated at 1MHz.

Inductive coupling between ICs has also been used in smart card applications to provide a non-contacting interface between smart cards and their receivers [30, 31]. The on-chip inductors used for this type of application are often large requiring an area of approximately $3mm^2$[30].

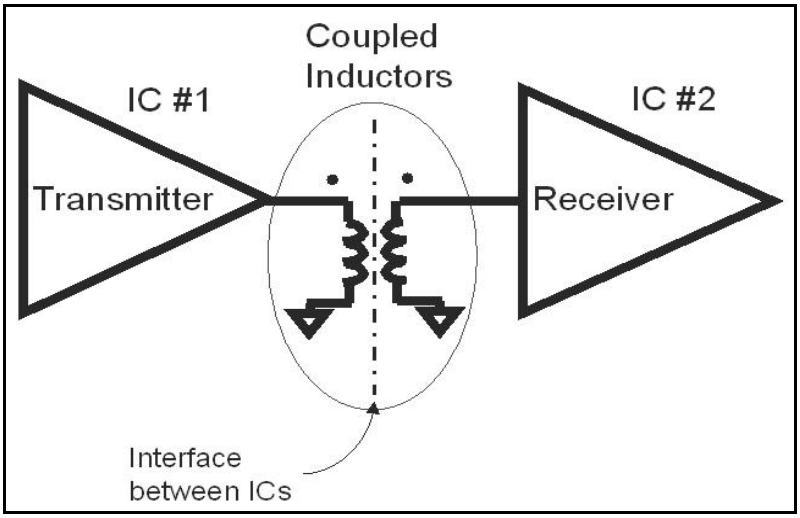


Figure 2: Illustration of AC Coupled Interconnection using shunt, trans-chip inductive coupling elements

Recently, Mizoguchi reported on the development of a transceiver in which inductive coupling is used to communicate information between two ICs stacked directly on top of each other [32]. The inductors used in this study are 300μm per side and the communication distance through the ICs is 300μm although only simulated waveforms are presented.

2.3 Integrated Passive Elements

AC Coupled systems implemented with inductive coupling rely upon integrated passive inductors and the performance of transformers built from these inductors. Numerous researchers have developed models of integrated inductors to aid in the design process and many performance results have been reported for on-chip inductors and transformers integrated into CMOS-based devices and substrates.

2.3.1 Inductor Modeling

Nguyen and Meyer proved the feasibility of integrating inductors onto silicon substrates for high-frequency applications [33]. Many researchers have since developed both methods for improving and models for predicting the performance of integrated inductors. A common 9-element lumped model for integrated CMOS

inductors on silicon is shown in Figure 3 [34, 35, 36, 37]. This model is used to create a frequency-independent representation of an inductor's electrical behavior.

The key to modeling is in understanding of the major mechanisms that must be modeled [37]. With reference to the model in Figure 3, the parameters of this model correspond to physical quantities [34, 37, 38]:

- L_S – series inductance
- R_S – winding resistance
- C_S – series feed-forward capacitance between the two inductor terminals
- C_{OX} – capacitance between inductor and substrate due to inter-level dielectric
- R_{SI} – resistance of substrate
- C_{SI} – capacitance across substrate

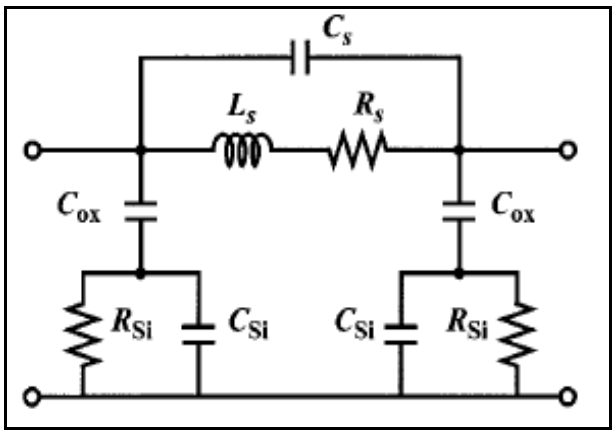


Figure 3: Common 9-element lumped inductor model
Variations of the model can be found in [34, 35, 36, 37]

Although it is not perfect, this model provides good correlation with measured results by capturing the behavior of crossover capacitance, substrate capacitance, substrate loss, and oxide capacitance [38]. The skin effect (which causes R_S to increase with increasing frequency) is not modeled directly. However, shortcomings with this model are not a surprise since the model simplifies a complex distributed system into nine lumped elements.

Many variations exist on the basic inductor model presented in Figure 3. For example, Niknejad has used four different variations of this model [39, 40, 41]. Crols used a model similar to this for inductors on a lowly doped silicon substrate but did not include C_{SI} and C_S [42]. Yue noted that if one terminal of the inductor were to be grounded, the 9-element lumped model could be simplified to a 5-element lumped model as shown in Figure 4 [38].

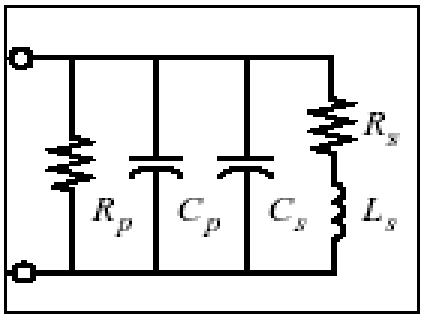


Figure 4: Lumped model for inductor with one grounded terminal

Yue reported a five-step method to extract the parameter values for a lumped inductor model from measured data [38]:

1. Measure S-Parameters of inductor
2. De-embed effects of measurement testbed
3. Convert S-Parameters to ABCD-Parameters
4. Solve for propagation constant and characteristic impedance from ABCD parameters
5. Solve for model values from propagation constant and characteristic impedance.

Ashby reported that de-embedding the measurement testbed could be accomplished by subtracting the Y-Parameters of the testbed from the Y-Parameters of the inductor [34]. However, Niknejad warned that parasitic coupling between the testbed and inductor complicates de-embedding the effects of the testbed from the inductor [41]. This coupling is present during inductor measurements but is not present during testbed-only measurements unless the testbed and the inductors are carefully isolated. Groves cautioned that the inductors should be measured across the desired operating temperature range since the Q of inductors over conductive silicon (15Ω-cm, P-type) decreases with increasing temperature [43].

Although it can be instructive to fit measured data to a model; it is also useful to develop a model that can be used to predict performance. Mohan et al developed analytic expressions to predict the values of the 9-element model parameters (from Figure 3) for square, hexagonal, octagonal, and circular inductor geometries [36]. With these formulas, inductors and circuits containing inductors could be designed and optimized without having to first fabricate, measure, and extract parameters of potential inductors. Hershensen developed a CAD tool for inductor design using a geometric programming technique to implement monomial expressions from Mohan's work [36, 44].

Niknejad developed a CAD tool named ASITIC (Analysis and Simulation of Inductors and Transformers for ICs) that enables design, optimization, and modeling of spiral inductors and transformers [41]. ASITIC is freely available (http://rfic.eecs.berkeley.edu/ ~niknejad/asitic.html) and models every segment of an inductor or transformer with a lumped model and uses electromagnetic techniques to compute inductance and capacitance matrices. This tool can be used to create lumped, narrowband models of inductors (Figure 5) using the built-in 'pix' command.

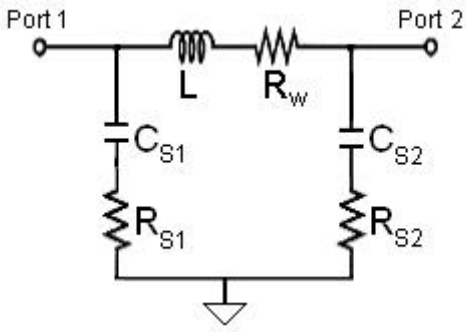


Figure 5: Narrowband model of inductors generated by ASITIC

Koutsoyannopoulos and Papananos developed a CAD tool named SISP (Spiral Inductor Simulation Program) to "accurately model polygonal (i.e. square, octagonal) spiral inductors, both planar and 3-D, transformers, and center-tapped spirals, splitters, and baluns" [45]. This CAD tool models every segment of a structure with a 2-port lumped model that is capacitively, inductively, and resistively coupled to all other segments. Its creators validated the performance of this tool by comparing simulated performance with the measured performance of inductors fabricated by several commercial foundries. This tool is now sold commercially (http://www.elab.ntua.gr/sisp/) but does not model stacked, coupled inductors.

2.3.2 Transformer Modeling

Mohan presented a number of topologies by which integrated transformers can be modeled and manufactured including tapered, interleaved and stacked [46]. Other researchers have also presented models and design equations for planar, coupled inductors [41, 45, 47, 48, 49, 50]. Of the topologies possible for coupled inductors, only stacked transformers are relevant to AC coupled interconnection systems. Mohan presented a lumped model of a stacked transformer where both primary and secondary are on the same integrated circuit. In his model, Mohan had an explicit connection between inductors with shared capacitance to ground. Mohan also provided design equations to predict the value of the model parameters from the transformer geometry [46].

Verma developed an ABCD-Parameter model from Mohan's lumped-element transformer model [51].Verma derived expressions for the 2-port S-parameters of a stacked transformer from his ABCD network model. Verma also developed a method to extract model parameters from measured S-parameter data by decomposing parameter extraction into two sub-problems: low-frequency and high-frequency parameter extraction.

ASITIC can be used to create lumped, narrowband models of transformers with the topology shown in Figure 6 using the built-in 'calctrans' command [52]. As shown in Figure 6, the ASITIC 'calctrans' command creates models for transformers that do not include the parasitic capacitances intrinsic to coupled inductors.

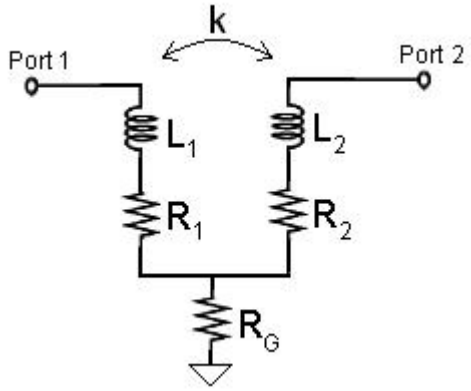


Figure 6: Narrowband model of transformer generated by ASITIC

Zolfaghari proposed a multi-metal topology for an integrated stacked transformer in which the primary coil was fabricated in a mid-level metal (of a multi-level metal process) and the secondary was fabricated on the remaining metal levels (both above and below the primary) [53]. Zolfaghari also proposed a subtle technique to improve transformer performance whereby the windings between stacked transformers were offset. This technique did not affect the mutual coupling between the primary and secondary but it reduced the parasitic capacitive coupling.

2.3.3 Inductor Performance in CMOS Technologies

Researchers have identified design techniques to overcome some of the inherent performance limitations with integrated inductors and transformers. For example, Niknejad advocated octagonal inductors instead of square spiral inductors as a means to increase Q [41]. Jorgensen stated that Q is maximized by maximizing the number of turns for a given inductor wire length; so he proposed using a circular inductor topology rather than a rectangular topology to maximize Q [54]. Jorgensen recognized that octagonal inductors could be used instead of circular inductors with minimal penalty.

Park investigated the effect of substrate resistivity and inductor geometry upon the inductor quality factor and found that Q increases with increasing substrate resistivity [55]. Park validated his findings by fabricating and measuring inductors with substrate resistivities of 4-6 Ω-cm, 30-50 Ω-cm, and 2 kΩ-cm. A process that relies upon highly resistive substrates is not widely transferable to commercial foundries since CMOS substrate resistivity is usually kept low to avoid latch-up.

Yue proposed the use of a patterned ground shield between the substrate and an inductor to reduce substrate coupling while improving the inductor quality factor [56]. Yue claimed that by using a patterned ground shield to eliminate substrate coupling, the design of on-chip inductors would be "simplified to a trade-off between the series resistance (R_S) and the oxide capacitance (C_{OX})" [37].

Long found that inductor Q is limited by the thin interconnect metallization available from commercial foundries; so he advocated thicker metal interconnections as a means to improve Q [57]. Long measured a 1.8nH inductor fabricated in a BiCMOS process and found that at 3GHz, increasing the conductor thickness from 1μm to 3μm can double the Q of the inductor from 5 to 10.

Burghartz proposed using inductors created from multiple metal levels and connected with via arrays to create inductors with an increased effective conductor thickness [58]. Burghartz fabricated inductors to test his theory in a process that supplied four AlCu metal levels where the top-level metal was 2μm thick and the lower-level metals were each 1μm thick. The process also used a 1.5μm thick dielectric between each metal layer and a 3μm thick dielectric between the substrate and the first metal layer. Burghartz found peak Q for inductors fabricated from a combination of all of the top-three metal layers supporting the claim that thicker conductors lead to higher Q.

Ashby proposed using an AT&T BiCMOS fabrication process with both highly resistive substrates and 5μm to 6μm gold metallization [34]. In this process, Ashby found that it was the DC resistance of the inductor spirals that limited peak Q to 12 across a frequency range from 3GHz to 4GHz.

2.3.4 Inductor Performance in non-CMOS Technologies

2.3.4.1 Post-processing

Rogers developed a method to post-process CMOS inductors with copper electroplating to increase the conductor thickness to 4μm [59]. Rogers was able to achieve a peak Q of 17 at 2GHz with a 250μm diameter inductor.

Ahn proposed the use of integrating magnetic core materials to create toroidal inductor structures through post-processing techniques on CMOS and bipolar integrated circuits [60]. The inductors in this process are large (on the mm scale) and achieve peak inductance in the low-MHz frequency range.

2.3.4.2 Multichip Modules

Inductor performance can be improved in a number of ways including increasing the resistivity of the substrate, using thick conductors, and creating a large gap between the inductor and the substrate. While these improvements prove taxing to CMOS integrated inductors, each improvement can be easily applied to inductors integrated onto packaging substrates such as MCMs [61, 62].

Arnold and Pedder reported the performance of thin-film spiral inductors in an MCM-D technology [63]. These researchers used silicon coated with silicon dioxide as a substrate and had a fabrication process that supplied four metal levels with polyimide as an inter-level dielectric. The wiring rules in this technology supported 25μm wire widths on 75μm pitch. Inductors with Q values ranging from 7 - 8 between 1GHz and 3GHz were demonstrated. Allen reported methods to fabricate inductors in MCM-L technologies [64].

Other researchers have been able to increase the Q of inductors in silicon-based MCM-D technologies by increasing substrate resistivity [65], increasing the thickness of the dielectric layers [66], and decreasing the minimum line width and spacing of metal traces [67]. Much of the current MCM-D research has been focused upon creating RF systems that rely upon integrated inductors rather than upon continued modeling of integrated inductors [68, 69, 70]. Researchers have also investigated integrating inductors into MCM-L and MCM-C substrates and making RF systems in these technologies [71, 72, 73, 74].

2.4 Packaging Technology

AC Coupled systems rely upon IC packaging technology to bring coupling elements into close proximity. Packaging has a long history including research in areas such as substrate processes, physical packages, and bonding methods. Each of these areas is relevant to AC Coupled Interconnection system design.

2.4.1 Background

Since the early days of integrated circuits, companies have been developing packaging technologies to build multi-component systems. Texas Instruments delivered to the U.S. Air Force the first computer built from integrated circuits in 1961. This computer was composed of 587 different integrated circuits that were each hermetically sealed, welded together and encapsulated into groups to form 47 modules [75]. Although it was an improvement over vacuum tube technology, early IC packaging was bulky and suffered from manufacturing

complexity. In 1964, IBM developed a method used in its IBM/360 computers to bond glass-encapsulated transistors, diodes and passive components into logic modules. This packaging technology was called SLT and was touted as offering "integrated circuits having close to maximum performance" due to its reduction of parasitic interactions between components, long lifetime without hermetically sealed devices, and manufacturing yields [76]. IBM documented the use of SLT with the creation of an AOI logic module. Solder was used to connect devices to the substrate. However in this technology, the solder from underneath the devices was free to wet the metal interconnections on the substrate. Rigid copper balls were used to prevent the devices from crashing into the substrate during solder reflow and causing short circuits between terminals.

In late 1968, IBM announced a method to bond flipped chips that did not rely upon rigid copper spheres or solid-state metallurgical interactions [77]. Miller recognized that if the solder-wettable surfaces on the substrate were controlled, then during reflow the surface tension of the solder could be used to suspend the devices above the substrate until the solder re-solidified. This technique would thereby prevent collapse-induced electrical shorts. Further, the use of "controlled collapse" allowed soft, ductile materials to be used for solder pads and eliminated the need for rigid contacts.

The advantages of controlled collapse over SLT and other rigid contact methods were numerous. The soft, ductile solder pads could withstand far more stress during thermal cycling and this led to reduced strain and fewer contact failures [77]. Moreover, the controlled collapse technique allowed for more tolerance in the planarity between bonding surfaces since solder could be deformed during reflow. The reduced need for planarity between bonding surfaces allowed "multi-pad devices of significant size and complexity" [77].

Miller discussed in detail several methods to restrict the areas to which solder could move during reflow including dots, dams, overlap, isolated lands and extra pads [77]. The dam method involved depositing a non-tinnable barrier material on top of tinnable landing pads to define regions where solder could form a joint. This new joining method proved to be very reliable. In pre-production studies, bond yields of 97% were observed [77]. Further studies investigated the thermal stability of controlled-collapse solder joints [78,79], optimization of landing pad geometry and solder volume [80], and optimization of solder composition [81].

Area array technologies have had a long and successful history of being employed in IC packages on advanced devices. However, for years, the cost associated with area array packaging has kept this technology from being applied in applications that were either too cost-sensitive or did not demand high I/O density. Instead, many packages were developed that relied upon all circuit I/Os being made available on the perimeter of the IC. Perimeter I/Os were wirebonded to pads within the package and then within the package routed to external pins.

2.4.2 Packaging Trends

Industry roadmaps make projections as to the number of signal, power and ground I/Os that future ICs will have to support [82]. Figure 7 shows the ITRS projection for package I/Os from 2001 to 2016. This roadmap makes projections for several classes of devices including low cost, cost-performance and high-performance devices (see Table 1) [83].

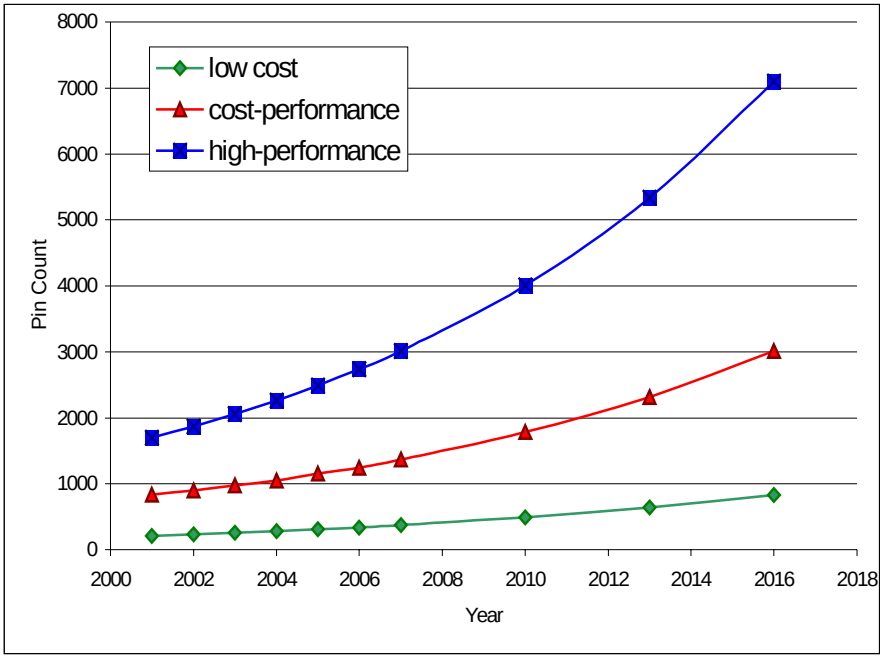


Figure 7: Packaging I/O Requirements 2001-2016 [82]

It is projected that the pin count for high-performance ICs will increase to 7100 I/Os by the year 2016 for a die size of 310mm^2 [82]. The roadmap indicates that technologies capable of supporting this high density have been identified although they are not yet proven to be transferable to industrial manufacturing. Further, no solution is known to exist that will achieve the required roadmap density while also meeting the roadmap cost-per-I/O targets [82].

Table 1 Device classifications in ITRS Roadmap [83]

Device Class	Description
Low-Cost	<$300 consumer products, microcontrollers, disk drives, displays
Hand-Held	<$1000 battery-powered products, mobile products, hand-held cellular telecommunications, other hand-held products
Cost-Performance	<$3000 notebooks, desktop personal computers, telecommunications
High-Performance	>$3000 high-end workstations, servers, avionics, supercomputers, most demanding requirements
Harsh	Automotive (under the hood) and other hostile environments
Memory	DRAMs, SRAMs

One effect of the demand for increased I/O density is to drive I/O pitch to ever-smaller levels. Wirebonding technology (fundamental for perimeter-style packages) has advanced to support the demanded I/O pitches using innovations such as multiple rows of bonding pads and ultra thin bonding wires. However, this technology is beginning to reach its limit since the I/O pitch continues to shrink [84,85]. Present day wirebonding systems can create rows of ultra-high pitched wirebonds on a pitch of 45 - 60μm [86,87]. Commercial wirebonding system manufacturers however have admitted that flip chip area array packaging will eventually be more cost effective for applications requiring high density since numerous manufacturing and cost issues exist in creating reliable, ultra high-pitch wirebond connections [84].

Another effect of the demand for higher I/O density is the development of smaller packages. There are currently four major classes of packages: through-hole, surface mount, area array, and 3-D – although there are hybrid through-hole / area array packages such as PGAs.

Through-hole packages are mounted to substrates by rigid leads that pass completely through the substrate. The density that these packages can support is limited due to difficulties in miniaturizing the package pins and through-substrate connection sites.

Surface mount packages are mounted to the surface of substrates by rigid leads that flare in or out at the bottom of the package. Surface mount devices can be made to have very small footprints. In this type of package ICs are connected to the internal package pads by bondwires. Thus, the pitch at which bondwires can be reliably manufactured will limit the I/O density that surface mount packages can support.

The solution to the problem of high-density interconnections must be addressed at many levels. Work is being done to improve interconnection density of substrate technology including array depopulation, microvias and thin-film technologies. The two techniques of microvias and thin-film substrates are recognized as being fundamental to enabling future PCBs to support the demands for increased I/O density [88]. Work is also being done to design substrates that will ensure signal integrity and manufacturing methods are being developed for creating fine-pitched arrays of solder bumps. Some researchers, however, propose schemes that represent a paradigm shift over present interconnection technology.

2.4.3 Substrate Technologies

A designer must consider the pin density that a particular substrate technology can support when designing an IC for area array, flip-chip packaging. In perimeter bonding technologies, the wirebond pitch translates directly into the substrate wiring pitch. However, for flip-chip applications, an array of coarsely spaced connections can require wiring rules more stringent than those required for fine-pitched perimeter-only connections. For example, consider the wiring rules for both a perimeter and an area array package with I/O on 60μm pitch. With perimeter packaging, all I/O could be routed if the wiring rules could support 30μm wide lines on a 60μm pitch. For the area array, however, the wiring rules would have to support 10μm wide lines on a 10μm pitch just to route two rows of the array with a single layer.

Wiring with 10μm wide lines would result in unacceptable resistive losses. For example, a 50Ω stripline fabricated from copper with a 5μm × 9μm cross-section would have a resistance per unit length of 4Ω/cm [89]. Rather than shrinking wire pitch and width to achieve all wiring on a single layer, more layers can be added to the substrate, but adding routing layers increases cost and manufacturing complexity.

For cost efficiency, some manufacturers develop infrastructure for a single base array bump size and pitch that is compatible with their existing low-cost substrates [90]. The area array bump size and pitch is designed to accommodate the most stringent I/O requirements that the manufacturer will support. Designs requiring fewer I/Os use the same bump sizes as the base array but allow for a larger bump pitch by not populating every site on the base array. This technique of depopulation has the effect of easing the substrate wiring rules for designs that do not require the highest I/O density [90]. For companies that employ depopulation, it is important that the base array bump size and pitch be carefully chosen since all other designs must use it.

Researchers are investigating techniques to create miniaturized vias (i.e. microvias) to mitigate the large via footprint typical on PCBs. For example, Hendriksen discussed a technique using an excimer laser to create microvias from 150μm to 50μm in diameter [91]. For testing purposes, the researchers used a conventional FR-4 PCB as a stable core and fabricated the microvias in organic dielectric layers added to the top and bottom of the

core. The researchers measured the effects of CTE mismatch between the organic materials and the FR-4, the thermal resistance of the organic materials, and the moisture sensitivity of the organic materials. The researchers concluded that their manufacturing technique could produce microvias down to 50µm on a 225µm pitch and was suitable for use with flip chip bonding. However, they admitted that manufacturing microvias smaller than 50µm in diameter would require more research due to problems with plating such small vias.

Depopulation and microvias do not deal with the pressing need to develop substrates that support ultra dense wiring. Accordingly, much ongoing research is aimed at developing substrate processes that can support finely pitched, narrow width conductors. Realistic wiring rules must be developed by balancing electrical performance with cost and fabrication complexity, and many issues must be considered when defining electrical performance including crosstalk, switching noise, insertion loss, dispersion and delay.

Ho et al reported a detailed study of the electrical performance tradeoffs for IBM's Thin-Film Module process [89]. This process consisted of two metal ground layers sandwiching two wiring layers and a topmost metal layer for fan-out. Copper was the preferred metal and polyimide (with $\varepsilon_r \approx 3.5$) was the preferred dielectric. To ensure acceptable electrical performance, constraints existed upon the fabrication process. It was noted that RIE must be used to etch both vias and wiring templates for electroplating. The process must also support metal lines and vias with large aspect ratios (metal height ÷ metal width). Finally, each layer must be fabricated with 10% planarity in order to control transmission line impedance.

With such a fabrication process, Ho et al found that thin-film lossy lines could be used to propagate high-speed pulses with low distortion over distances up to 20cm [89]. The researchers investigated crosstalk performance for thin-film lossy lines. They developed the structure shown in Figure 8 (with dimensions in µm) that maintained a 50Ω impedance, could support 1000 lines per inch over 20cm line lengths, and suffered less than 10% crosstalk. The transmission lines shown in Figure 8 were characterized by $\rho_{Cu} = 1.8\mu\Omega$-cm, $R_o = 4.1\Omega$/cm, $L_{max} = 2Z_o/R_o$ (at 20cm), and $Z_o = (L_{22}/C_{22})^{1/2} = 41\Omega$. Ho and his colleagues also reported a method to integrate capacitors into the substrate so as to mitigate the effects of inductance-related switching noise.

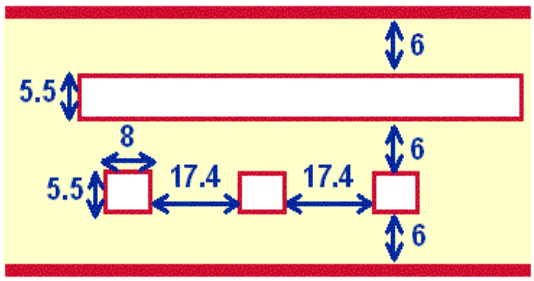


Figure 8: Triplate lines for IBM Thin-Film Module technology [89]

Haller and his colleagues reported electrical results of microstrip and stripline transmission lines fabricated with a GE high-density interconnect thin-film process [92]. The process employed four metal layers and three dielectric layers. From the bottom of the substrate to the top, the dielectrics were 50μm, 21μm, and ~15μm thick. All conductor layers were made of copper and were approximately 4μm thick.

In this fabrication process, TDR measurements confirmed that microstrip lines of 78μm on a 138μm pitch and striplines of 51μm, on a 111μm pitch maintained a 50Ω characteristic impedance [92]. VNA measurements were made of insertion and return losses. The researchers found a good correlation between theoretical and measured losses once the process details were taken into account. That is, once the conductors were fabricated, they had a trapezoidal rather than a rectangular cross-section. The researchers defined the "effective height" of the trapezoidal conductors such that the perimeter was identical to the idealized rectangular conductors assumed by their microstrip and stripline equations. The need to define an effective height is important since the effective geometry of thin film structures cannot be known until the details of the fabrication process have been determined. Thus, the wiring rules cannot be set until the tolerances of the fabrication process are known (or at least specified) [89, 92, 93, 94].

Another important finding was that for the given transmission line dimensions, insertion loss rather than crosstalk noise dominated interconnect performance for frequencies up to 9GHz [92]. The process must be modified to create lines that are not as lossy or transmitter and receiver circuits capable of communicating across lossy lines must be designed.

Substrates can be manufactured in more than one way but performance consistency across manufacturing methods is important. Thiel, et al. reported an effort to study the effects on high frequency signal transmission in thin film MCM-L substrates. The substrates that they studied adhered to the Motorola MRTV-2.2 / Interconnect Technology Research Institute specification ITRI-TV2.4A specification [95]. This substrate specification was developed to be compatible with current techniques for substrate fabrication. As an example, the substrate vias could be manufactured with photolithography, laser ablation, mechanical punching, or plasma etching. Although their data analysis was targeted toward MCM-L substrates and it was incomplete, they discussed several important aspects of substrate manufacturing that could impact performance consistency across different manufacturing techniques. The researchers noted that the electrical performance of interconnections on thin film substrates was a function of the substrate surface roughness, substrate dielectric thickness, dielectric constant, conductor cross-section, parasitics, and fabrication process tolerances. These findings underscore the fact that wiring rules can be established only after careful consideration of the thin-film substrate fabrication processes.

The electrical performance of the substrate becomes more important as the bandwidth to be sustained by each chip I/O increases. FR-4 has long been the predominant material used for printed circuit boards. It has been

found, for several reasons, that FR-4 is not a suitable substrate material for high-speed signal propagation [96]. The loss tangent of FR-4 is 0.025 and this leads to unacceptable signal loss over long connections (e.g. 10.8dB loss over 70cm at 2GHz). Materials with lower loss tangents are needed to support high-speed signal propagation.

Signal propagation delay for transmission lines on any particular material is a function of the dielectric constant of the material, and FR-4 has a relative dielectric constant of approximately 4.3. Power dissipation is also a function of a material's dielectric constant. Substrate materials with lower dielectric constants are being sought to reduce both signal propagation delay and power dissipation [96]. Moreover, cost, fabrication constraints, and moisture absorption (since moisture affects the stability of the dielectric constant) must all be considered when selecting a new substrate material [97].

Given the large number of variables that must be optimized, the absolute limits of substrate wiring are unclear. Pease and his colleagues make the argument that at room temperature, coplanar substrate interconnections on a line pitch of 35μm are feasible. The pitch can be shrunk to 6μm if the substrate is cooled to liquid nitrogen temperatures and to 2μm if superconducting interconnections are used [98].

Alternatives to the traditional use of substrate interconnections are being explored as methods to support an effective increase in I/O density. For example, if the frequency of data communication is high enough, the substrate traces interconnecting I/Os between ICs must be treated as transmission lines. In this situation, the transceiver circuits and interconnection can be specifically designed so that multiple bits of data can be in-flight simultaneously on the transmission line [99]. Per I/O data rates of up to 1Gbps have been achieved with this method.

2.4.4 Physical Packages

In addition to the substrates, much attention has been focused on the physical packaging for solder bump, area array technologies. Numerous packages based on these technologies and variations thereof are reported as evidenced by the articles on BGA [100, 101, 102, 103, 104], flip chip [101, 105, 106, 107], CSP & WLP [101, 108, 109, 110], and MCM [111, 112, 113, 114].

Organizations such as JEDEC help define standards for packages [115]. These standards set ranges for package features and are useful in maintaining consistency between packages implemented by different manufacturers. For example, JEDEC standard MO211-B defines the size, location and height tolerances for CSP packages [116]. This standard, like many others, does not define manufacturing methods. It is the responsibility of each manufacturer to qualify a reliable process for fabricating CSP packages that adhere to the standard [117]. Packages that are to be widely adopted will likely be manufacturable by a variety of processes.

Newly developed packages must be qualified by lifetime tests to ensure reliability in harsh environments [118]. For example, thermal cycling tests expose the major failure mechanism in BGA packages – solder joint cracking and delamination due to fatigue from thermal cycling [119]. It has been found that BGA reliability is dramatically improved by the use of underfill materials since these materials distribute across the entire package surface the stress induced by solder and package CTE mismatches [119].

There is an indistinct boundary between substrates and packaging for MCMs since MCMs act as both a substrate to interconnect multiple ICs and packaging to a PCB for these ICs. Like substrates, fabrication processes for MCMs must be carefully developed to ensure acceptable electrical performance for interconnections and manufacturing yield [120, 121,122, 123].

2.4.5 Bonding Processes

2.4.5.1 Solder Joining

The need for higher I/O densities drives continuing research in solder bump processes. Companies are involved in providing services for flip chip packaging and are working on many different techniques to create bumping processes capable of extremely high density. Current high-volume, production equipment for BGA packages is able to place 300µm diameter solder balls but machines with 200µm capability are in field trials [124]. Texas Instruments reports a WLP bump transfer process used to attach 127µm eutectic Sn / Pb solder bumps to an IC on a 356µm pitch although there are plans to study smaller pitches [125]. Motorola has developed a process to apply eutectic Sn / Pb solder to an IC by stencil printing and can achieve a 200µm solder bump pitch [126]. Using fine-line photolithography and solder electroplating, Unitive reports the ability to create 20µm solder bumps on a 50µm pitch [127]. However, the composition of the Unitive solder bumps is not disclosed.

The composition of solder bumps is important since it has a direct impact on cost and the reliability of the IC / substrate bonds. The selection of the materials of the solder bond pads (UBM) is equally important for cost and reliability [128]. Sn / Pb eutectic solder is well understood, is low-cost, has a low melting point, and allows for easy visual inspection of faulty connections [129]. Eutectic Sn / Pb solders with traditional Cr / Cu UBMs are not stable over many thermal cycles due to Sn / Cu interactions [130,131]. Phosphorous-doped nickel has been proposed as an additive for Cr / Cu UBMs to improve eutectic Sn / Pb reliability over thermal cycling [131]. The industry is moving away from lead-based solders for environmental, political and marketing reasons and working to develop an infrastructure for lead-free manufacturing [129, 132].

2.4.5.2 Sea of Polymer Pillars (SoPP)

Bakir et al have recently proposed the use of polymer pillars as a means to achieve an array of compliant electro-optical chip-substrate interconnections [133]. Polymer pillars are fabricated on the surface of a substrate and

after fabrication the pillar sidewalls are covered in metal. The researchers have reported 50% input coupling efficiency for polymer pillars 55μm wide and 100μm tall. An array of pillars 5μm wide and 13μm tall has been fabricated but results on this structure have not been reported. However, the claim is made that the SoPP technique can be used to achieve I/O densities in excess of $10^5/cm^2$.

2.4.5.3 Conductive Materials

Some researchers are investigating methods to replace arrays of solder bumps with conductive materials as a means either to connect ICs to a common substrate [134, 135] or directly to other ICs [136]. These materials are applied to coat the entire surface of the IC. They serve the dual purposes of bonding the IC to a substrate or other IC and acting as a conduction path for I/Os that are vertically aligned. Since the bonding material is conductive, the pad pitch and the conductivity of the material must be carefully selected so that crosstalk noise between adjacent I/O does not unduly hinder performance [136]. The bandwidth needed in the signal path must also be considered since the loss of conductive epoxies and pastes is generally a strong function of frequency [136].

2.4.5.4 3D Bonding

Wafer bonding, chip bonding and wiring in the third dimension is getting much attention [137, 138, 139, 140]. 3-D stacking and packaging of identical ICs has been used since the mid-1980s for memory modules but more recently is being applied to heterogeneous systems [139]. In order to achieve broad acceptance of 3D packaging, more research is needed on reliability; manufacturing methods must be developed to lower cost; and software design and test tools are needed [137-140].

2.4.5.5 Hybrid Bonding

Packaging techniques are being designed to tightly package devices fabricated in incompatible technologies. Giziewicz and colleagues reported a method to bond III-V VCSELs with standard CMOS devices [141]. The researchers fabricated VCELS that stood above their GaAs substrate surface like pillars and CMOS ICs with openings in the top passivation layer. They then flipped, aligned and bonded the VCSELS through the passivation openings on the CMOS IC [141].

Harsh et al. reported a flip-chip bonding process for MEMS devices that provided a small, reproducible gap across the chip / substrate interface [142]. The researchers found that the gap between the chip and substrate could be controlled to within ±0.1μm by precisely controlling the bonding force.

Chapter 3 AC Coupled Interconnect Analysis

3.1 Overview

The basic concept of AC coupling exploits the fact that capacitors placed in series or coupled inductors placed in parallel with an AC signal trace can block any DC voltage while passing the AC voltage. Both capacitive and inductive coupling are investigated as a means to transmit signals across a physical chip-chip or chip-substrate interface where no direct physical connection exists.

Capacitively coupled interconnection (CCI) systems can be designed to operate as either lumped (e.g. as in direct chip to chip applications) or as distributed systems (e.g. as in multichip modules). A coupling capacitance can be modeled by a simple pi-network of capacitors. A single instance of such a model can be used in the modeling of a lumped CCI system, but a distributed system – implying the presence of transmission line elements – is more appropriately described by two or more capacitor models separated by a transmission line. A description of the tradeoffs involved in CCI is presented.

Like CCI systems, inductively coupled interconnection (LCI) systems can be designed to operate as either lumped (e.g. as in 3D IC packaging) or as distributed systems (e.g. as in IC-substrate-IC applications). A pair of coupled inductors can be modeled by a schematic composed of R, L, and C components. A single instance of such a model can be used in the modeling of a lumped LCI system. Two or more coupled inductor models separated by a transmission line more appropriately describe a distributed system. Because of the complex behavior of a pair of coupled inductors, a model for coupled inductors is developed, its use for analysis is justified, and the values extracted for the components in the model are related to physical design parameters. After this, a detailed sensitivity analysis is performed both to show how electrical performance of the model changes as the component values of the model change and to expose issues that must be considered when designing a communication system using inductively coupled elements. This sensitivity analysis is performed in several parts starting with the case of ideal coupled inductors. Increasing levels of detail are added to the analysis until finally the complete model is analyzed.

The correlation of the coupled inductor model components to physical parameters and the sensitivity analysis are then applied to both lumped and distributed LCI systems. Guidelines are presented to show how to translate system specifications into constraints upon inductive coupling element design and placement, and input waveforms to maximize system response are discussed.

3.2 Capacitively Coupled Interconnects

Circuit schematics for lumped and distributed CCI systems are shown in Figure 9. In both systems, the AC coupling action performed by the capacitor C_C is deteriorated by the shunting parasitic capacitors C_P. In the case of a distributed system, a shunt termination resistor can be used to provide impedance matching.

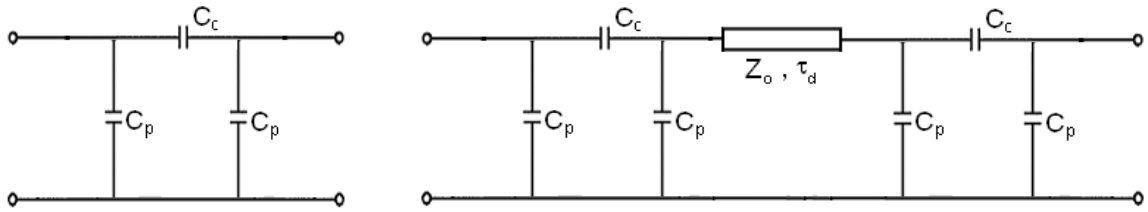


Figure 9 Circuit schematics for lumped and distributed CCI systems
Lumped (top), Distributed (bottom)

There are five key physical parameters impacting the electrical performance of the coupling and parasitic capacitors: the relative permittivity of the dielectric and the distance between capacitor plates, the lateral dimensions of the capacitor plates, and the distance from the bulk substrate to the capacitor plates. Figure 10 illustrates these geometrical parameters although the distance from the capacitor plates to the substrate is not explicitly labeled. The capacitor plates are shown in different colors to highlight the fact that the two plates that form the capacitor exist on physically different ICs (or IC and substrate).

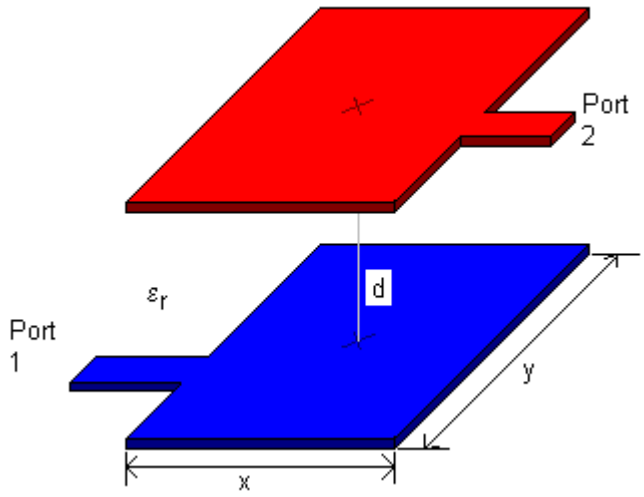


Figure 10 Geometrical parameters for coupling capacitor design

The value of C_C depends upon the plate separation, the dielectric between the plates and the physical size of the capacitor plates. The value of the parasitic capacitors C_P depends upon the distance from and the dielectric between the plate to the substrate and the size of the capacitor plate.

Control of these geometric parameters translates into three key metrics for each I/O of a CCI system: power, density and bandwidth. I/O bandwidth is determined by the value of the coupling capacitor, parasitics and the loss characteristics of any interconnections. The desired I/O density constrains the nearest-neighbor separation and the physical size of the capacitor plates. In addition to transceiver design, I/O power is determined by the value of the coupling capacitor, parasitics, system impedance and loss in the interconnection. Thus there are tradeoffs between each of the key performance metrics.

3.2.1 Lumped CCI System

In a lumped CCI system, the transmitter is connected to the receiver by a channel modeled as a Pi-network of capacitors (*see Figure 9*). The frequency response of this network can be described in a compact algebraic equation as shown in Equation 1. When the load resistance (R_L) is large, the channel is able to pass input voltages over a wide range of frequencies with the output scaled by the relative sizes of the coupling and parasitic capacitors.

$$\frac{V_{OUT}}{V_{IN}} = \frac{C_C R_L s}{1 + (C_C + C_{P2}) R_L s}$$

Equation 1 Frequency response of lumped CCI channel

Figure 11 and Figure 12 illustrate the impact of R_L and the ratio of C_C/C_P upon the frequency responses of several capacitive networks. Figure 11 shows the frequency response of a single capacitive network (C_C = 150fF, C_P = 50fF) for values of load resistance between 50Ω and 5MΩ. As R_L decreases, the bandpass network becomes increasingly narrow band.

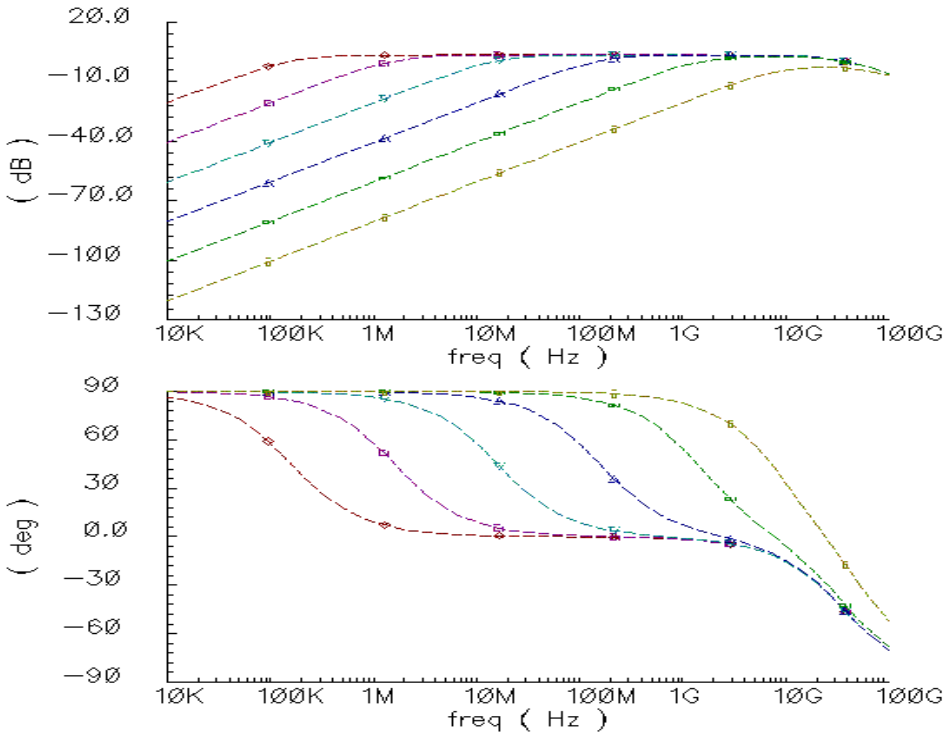


Figure 11 Frequency-domain responses demonstrating impact of R_L upon lumped CCI channel
Magnitude (top) and phase (bottom)
(gold) R_L = 50Ω, (green) R_L = 500Ω, (blue) R_L = 5000Ω,
(cyan) R_L = 50kΩ, (magenta) R_L = 500kΩ, (red) R_L = 5MΩ,
C_C = 150fF, C_P = 50fF;

Figure 12 shows both the frequency response and time-domain step response of three different capacitive networks (network 1: C_C = 150fF, C_P = 50fF; network 2: C_C = 1500fF, C_P = 500fF; network 3: C_C = 150fF, C_P = 500fF) for a fixed 1GΩ load impedance. The attenuation is equal through the passband for a fixed ratio of C_C/C_P; however, larger component values reduce the upper –3dB frequency. As the ratio of C_C/C_P decreases, the attenuation through the passband is increased, but the upper –3dB frequency moves slightly higher in frequency. Higher attenuation in the passband leads to smaller output voltages for time domain signals passed through the network, and lower –3dB frequencies lead to stronger low pass filtering of input signals. Although not shown explicitly in the figure, the channel response decays to 0V over the length of multiple bits so some manner of data encoding is required to prevent long streams of logic 0's and 1's from causing ISI.

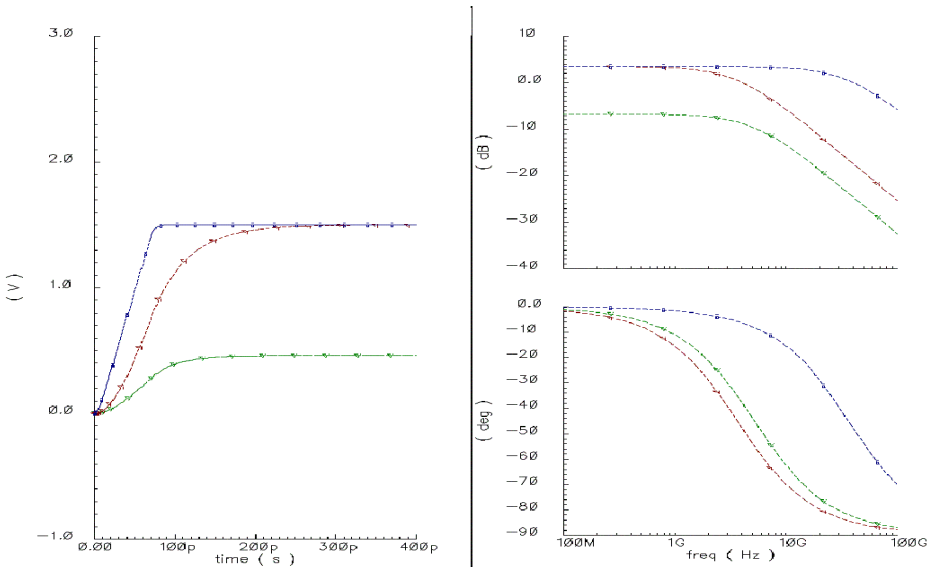


Figure 12 Time- and frequency-domain responses of lumped CCI channel to varying ratios of C_C / C_P with 1MΩ load
(left) Time-domain response
(right) Frequency-domain response with
(top, right) magnitude and (bottom, right) phase
(blue) C_C = 150fF, C_P = 50fF;
(red) C_C = 1500fF, C_P= 500fF;
(green) C_C = 150fF, C_P = 500fF

With a high impedance termination, it is the ratio of capacitance values between C_C and C_P and not the exact value of C_C that most impacts achievable bandwidth and channel attenuation for a lumped CCI system. As the ratio of C_C/C_P increases, the attenuation of the channel and therefore the power consumption of the transceiver is reduced. Therefore, large ratios of C_C/C_P are desirable to minimize power dissipation.

Extremely dense arrays of lumped, capacitively-coupled I/O channels can be created as long as the chip and substrate fabrication technologies can be used to create CCI channels with the correct ratio of C_C/C_P. Figure 13 shows the ratio of C_C/C_P as a function of the ratio of plate separation (D2) and the distance of the plates from the substrate (D1) and as a function of the ratio of the dielectric between each capacitor plate and its substrate (ε_{r1}) and the dielectric between capacitor plates (ε_{r2}). Examples of material combinations that would achieve the dielectric ratios are shown in the legend. Since CCI is intended for chip-chip systems, each plate will have shunt parasitic capacitance to its own substrate. The results reported in the figure assume that both plates are separated from their respective substrates by the same distance. The figure shows two trends to consider. First, for a fixed distance between the plates and the substrate (D1) as the gap between capacitor plates decreases (D2) the ratio of D1:D2 increases and therefore the coupling capacitance C_C grows larger relative to the shunting parasitic capacitor C_P. Secondly, for a fixed distance between the plates and the substrate (D1) and a fixed gap between

plates (D2), the capacitance ratio of C_C/C_P can be increased by using an underfill material between capacitor plates with a large relative permittivity.

The two trends revealed by Figure 13 can be used to understand the impact of the capacitance ratio upon packages designed to support capacitively coupled interconnections. For example, given capacitors formed on top of a substrate with oxide and a material with a dielectric constant of 2.65 (e.g. BCB) used between capacitor plates then the purple line in the graph indicates the tradeoff between D1/D2, $\varepsilon_{r2}/\varepsilon_{r1}$ and C_C/C_P. If C_C must be kept twice as large as C_P for correct circuit operation then the capacitor plates must be at least three times further from their respective substrates than from each other. If a fabrication technology allows a capacitor plate formed on the uppermost metal to be separated from the substrate by 9µm then the packaging technology must support a gap between a chip and substrate of at most 3µm. Thus, the specific capacitance ratio required for correct circuit operation impacts the gap that can be tolerated between capacitor plates and the minimum distance from the substrate.

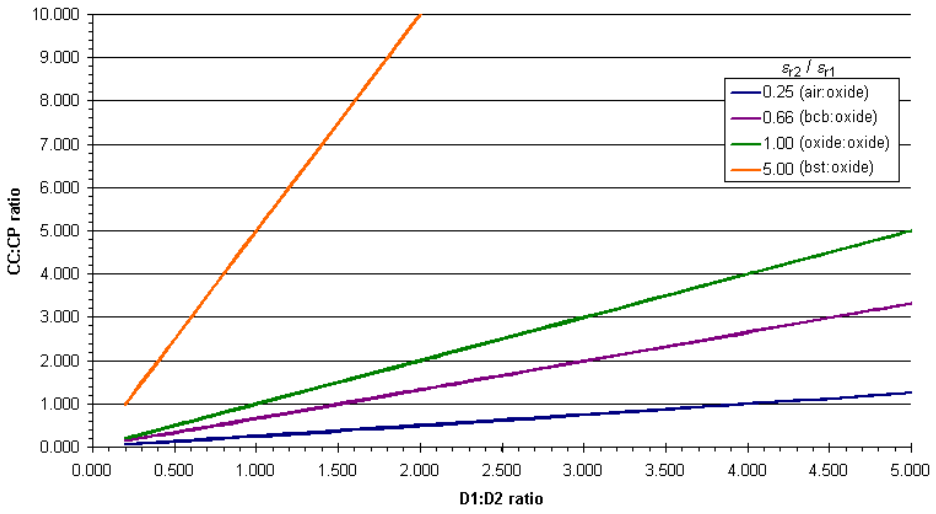


Figure 13 Ratio of C_P / C_C as a function of 1) the ratio of distance between capacitor plates and substrate, and 2) the ratio of relative permittivities of inter-capacitor dielectrics and substrate

D2 = distance between capacitor plates
D1 = distance from capacitor plates to the substrate
εr1 = relative permittivity of substrate dielectric
εr2 = relative permittivity of dielectric between capacitor plates

Practical considerations place limits upon how small C_C can be to achieve operational circuits since any real receiver circuit will present the capacitively-coupled channel with some input capacitance C_{RX}. In an actual circuit implementation, the capacitance ratio can be rewritten as C_C:(C_P + C_{RX}) to show the dependence upon the receiver input capacitance. With respect to Figure 13, the receiver input capacitance has the effect of requiring a smaller gap between capacitor plates or a larger plate-to-substrate standoff. For example, if a total capacitance

ratio of 2:1 is required for correct circuit operation but the receiver input capacitance is 20fF, then the system can be designed so that C_C is equal to 100fF and C_P is equal to 30fF to achieve this overall capacitance ratio. Thus with respect to Figure 13, a ratio of 10:3 would actually be required between the values of the coupling capacitor and its parasitic capacitance to ground. With these values, an oxide intra-chip dielectric and BCB inter-chip dielectric the ratio D1:D2 ratio increases from 3.0 to 5.0 because of the receiver parasitic capacitance.

3.2.2 Distributed CCI System

In a distributed CCI system, the transmitter is connected to the receiver by a channel modeled as a series connection of a Pi-network of capacitors, transmission line interconnection, and another Pi-network of capacitors (*see Figure 9*). The performance of the distributed CCI system is significantly different from that of the lumped system. Unlike the lumped CCI system, a low impedance transmission line terminates the first coupling stage of a distributed CCI system. This low impedance termination causes the coupling capacitors to have a bandpass response that differentiates signals passed through it. Moreover, the response is deteriorated by loss in the transmission line. Even still, a distributed CCI system must be designed to meet per-I/O bandwidth, density and power goals.

3.2.2.1 Capacitively-Coupled Network Terminated by Low Impedance

Looking at the impact upon I/O bandwidth for the first stage of a distributed CCI system in detail, the series coupling capacitance combined with the shunt parasitic capacitances and low impedance load resistance creates a channel from the driver to the receiver with a bandpass response. Like a lumped CCI system, the response is still described by Equation 1, but the load resistance in this case is small. The relative values of C_C and C_{P2} set the -3dB corner frequencies of the bandpass response. The capacitances encountered in CCI systems will be in the femtofarad range and the load impedance will depend upon the actual transmission line design but will typically be less than 100Ω. Using these values, the corner frequencies will typically be in the low- to mid-gigahertz. Data signals to be transmitted through a CCI channel should contain information in this frequency range since information outside of the channel passband will be filtered out and deteriorate performance.

In addition to the –3dB corner frequencies, Equation 1 indicates that, until the upper –3dB frequency attenuates the channel, the amplitude of signals is directly related to the size of the coupling capacitance C_C. Figure 14 illustrates both the bandpass nature of the channel and the impact of the value of C_C by showing the frequency responses of four systems with load impedance of 50Ω and capacitance values in the femtofarad range (i.e. C_C = 150fF & 250fF for C_P = 75fF & 125fF). Analysis of this figure shows the two curves corresponding to C_C = 250fF are roughly 5dB greater than the two curves for C_C = 150fF until the upper –3dB frequency of each channel begins to dominate performance. As compared to the low pass response resulting from a high

impedance termination as shown in Figure 12, this figure underscores the significant performance difference resulting fi

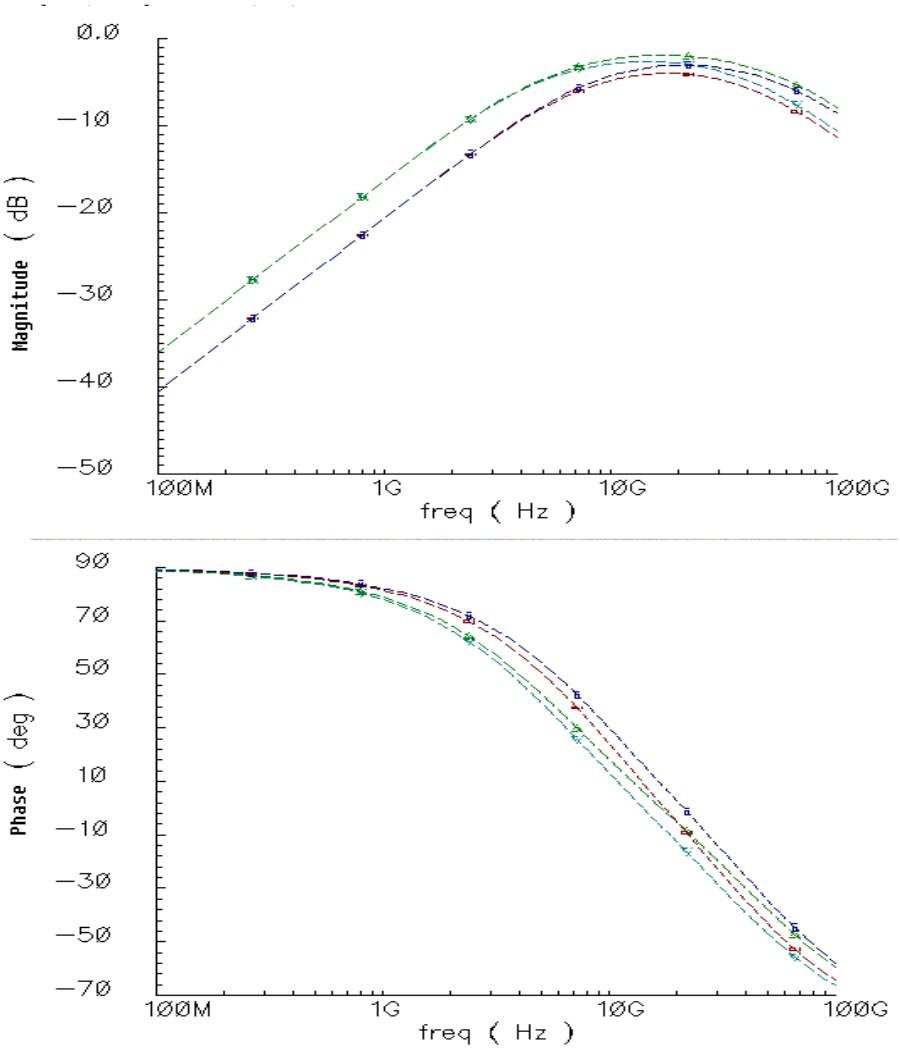


Figure 14 Magnitude and phase responses of lumped CCI channel
(dark blue) C_C *= 150fF,* C_P *= 75fF; (red)* C_C *= 150fF,* C_P *= 125fF*
(green) C_C *= 250fF,* C_P *= 75fF; (light blue)* C_C *= 250fF,* C_P *= 125fF*

In the time domain, this bandpass behavior can be interpreted as the channel performing edge detection (i.e. differentiation) upon the signals passed through it. This behavior is ideal for transmitting digital signals through a CCI system since these signals carry information in the *transitions* between binary states. Thus the edge rates of the data transitions effectively encode the data into a frequency band compatible with the capacitively coupled network. To use a CCI network with a low impedance load for digital data transmission, the coupling capacitance must be large enough to pass a detectable amplitude and the edge rates of the signals should be such to make the frequency content of the transitions fall within the channel passband. To illustrate these

requirements, Figure 15 shows how voltage steps of varying rise times are transmitted through two different CCI channels.

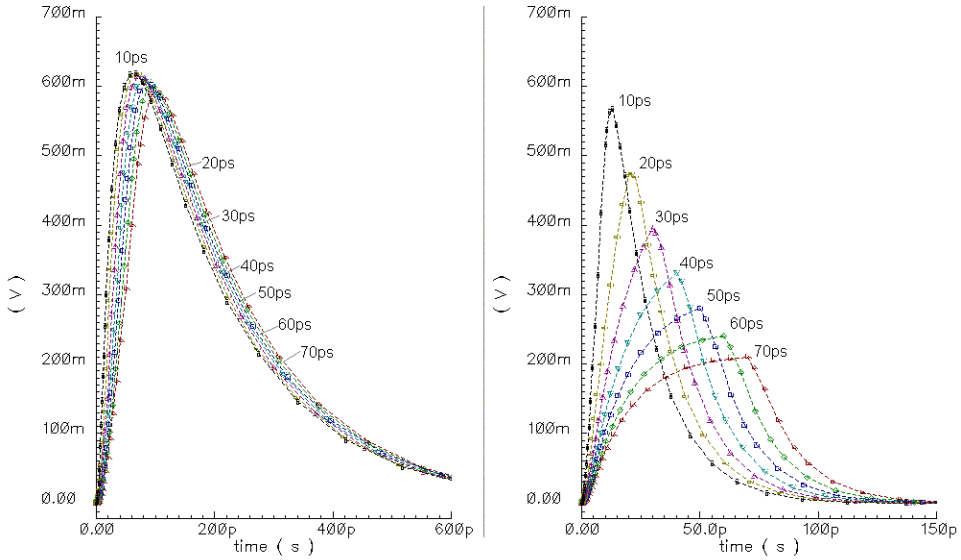


Figure 15 Time-domain response of a lumped CCI channel to input voltage steps with varying rise time
Input risetimes varied from 10ps to 70ps
(left) C_C = 1500fF, C_P = 500fF
(right) C_C = 150fF, C_P = 50fF

With respect to Figure 15, the passband for the channel with C_C = 150fF is centered at 25.1GHz with lower and upper –3dB frequencies at 7.3GHz and 79.9GHz, respectively. The passband for the channel with C_C = 1500fF is centered at 2.5GHz with lower and upper –3dB frequencies at 0.8GHz and 13.9GHz, respectively. Three important observations can be made about the response of these channels to voltage steps of varying rise time. First, maximum signaling through the channel occurs for the fastest edge rates independent of the value of coupling capacitance. The second observation is related to the settling time of the response. For large coupling capacitances (e.g. 1500fF), the channel response is not very sensitive to variations in edge rates in the picosecond range. However, as the coupling capacitance is decreased, the time domain response becomes significantly sensitive to changes in the signaling edge rate. For example, in the system where C_C = 150fF, the time required for the response to settle to 10% of its peak value is 55ps for 10ps rise times but 114ps for a 70ps rise time. Finally, even though the response is sensitive to edge rates, it is important to notice that for gigabit signaling, the response decays quickly over the length of a single bit time. Therefore, if edge rates can be made fast enough, coding is not needed on long streams of logic 1's and 0's to prevent ISI. Instead, since signaling is done only on data changes, the duration of the step response can be examined to decide the point in time when subsequent data bits should be transmitted. For example, if a given application could tolerate 10% ISI, then with respect to Figure 15, the capacitively coupled channel with C_C = 150fF could be used either to support an NRZ data rate of 18GHz

or 8.5GHz (i.e. the inverse of settle times) by using either 10ps or 70ps rise times, respectively. Of course, this quick calculation overestimates the *sustainable* data rates since clock skew and other sources of signal jitter have not been taken into account. For a given channel, if data rates are desired beyond that which can be supported by simply applying edges to the system after enough time has passed for the response to settle, then signal compensation / equalization techniques must be employed.

This coupling capacitance forms a voltage divider between itself and the parallel combination of its associated parasitic capacitance and the load impedance, and this voltage divider constrains the per-I/O power consumption. For example, if 0.9V is available for signaling from the output of the transmitter to a matched load but 100mV is required for the receiver to correctly detect a signal, then the total attenuation of the transmitted signal through the interconnection must be no more than 800mV. With a set edge rate, there is a minimum coupling capacitance needed to achieve signaling at a desired data rate. As discussed previously, the coupling capacitance and its parasitic capacitances are related to each other according to tradeoffs with the physical geometry and material set (*see Figure 13*) so channel attenuation (and thereby power consumption) cannot be set independently of I/O density goals.

The capacitance values needed to achieve specific system bandwidth goals constrain I/O density by impacting plate separation, the dielectric between the plates, and the physical sizes of the capacitor plates. Any specific capacitance value can be achieved by numerous plate sizes and separations as illustrated by Figure 16. This figure also reveals the maximum gap distance that can be tolerated for a given plate area and value of capacitance. For example, [143] reported capacitively coupled circuits for distributed CCI systems that operate with a capacitance of 150fF. Given this capacitance, Figure 16 shows that a gap between capacitor plates (i.e. parameter 'd' from Figure 10) of 21μm or less is needed to use capacitor plates on the order of 300μm per side but a gap of roughly 3μm or less is needed to use capacitor plates on the order of 110μm per side. The allowable gap between capacitor plates shrinks rapidly as the per-side dimension of the capacitor is reduced, but small per-side dimensions are desirable since smaller physical capacitors increase the number of I/O channels that can be fit into a given area. On balance, the physical packaging technology responsible for keeping two chips (or a chip and a substrate) in close and controlled proximity would better accommodate large capacitors that are tolerant to fluctuations in the gap.

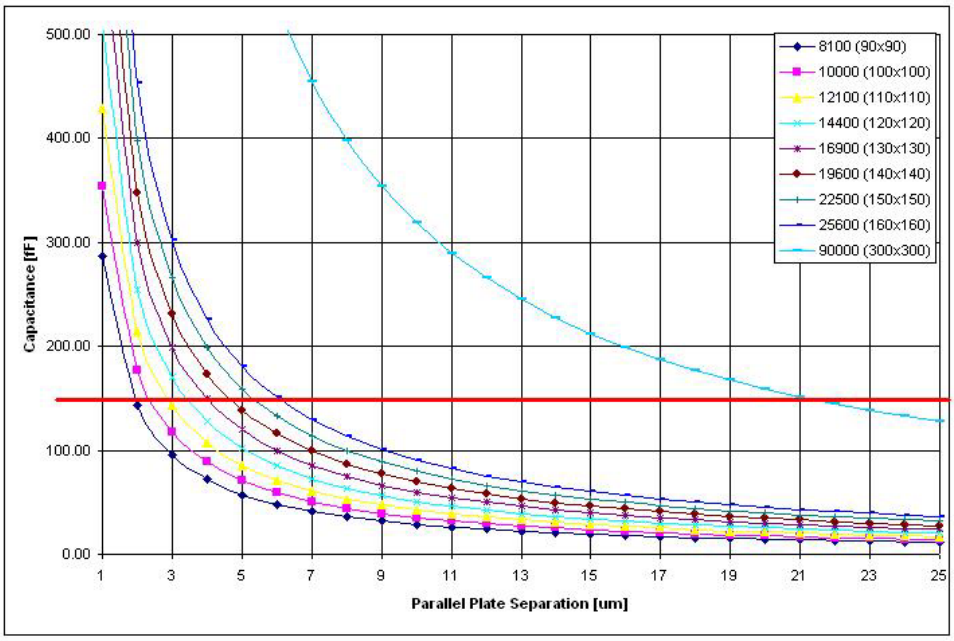


Figure 16 Capacitance between opposing plates versus plate area and separation
Results of 3D electromagnetic simulation assuming relative permittivity of dielectric = 4.0

3.2.2.2 Effect of Lossy Transmission Line on Distributed CCI System

It is the presence of a long interconnection modeled as a transmission line that causes a capacitively coupled system to be considered as distributed rather than lumped. Although ideal transmission lines will be lossless and have linear phase, practical transmission lines that can support routing of dense CCI systems will introduce attenuation and dispersion to signals transmitted through them and require impedance matching. The attenuation of the transmission line reduces the amount of signal that can be lost to the voltage divider formed by C_C, C_P and R_L in each coupling stage. The dispersion of the transmission line introduces ISI and reduces the signaling rate that could otherwise be achieved.

The transmission lines must be designed to present the system with known and controlled impedances so the design of these lines implies a geometry that is set by the thickness of the layers used to fabricate the substrate. The physical geometry of the transmission lines could reduce the achievable element density if not enough lines can be routed into an array of coupling elements. A discussion on the co-development of transmission lines and substrate process is presented in *Chapter 5*. The transmission lines also require that either transmitter- or receiver-side matching be used to avoid reflections due to impedance mismatch. Transmitter-side matching, for example, can be implemented by placing a terminating resistor in shunt with the transmission line input. Coupling and parasitic capacitor values in the femtofarad range will appear to be high impedances to the termination resistor, so the system can be matched up to the mid-gigahertz frequency range with a simple termination.

3.2.2.3 Performance of Complete Distributed CCI System

The final coupling stage of a distributed CCI system can be treated like the single coupling stage of a lumped CCI system. That is, the final stage is composed of similar values of capacitors and is terminated by a high impedance receiver. As mentioned, the combination of the transmission line, termination resistor and both transmitter and receiver coupling stages forms a voltage divider that reduces the signal reaching the receiver, and the loss in the transmission line further degrades the amount of signal appearing at the receiver. For digital signal transmission, the edge rates from the driver output should be made as sharp as possible to minimize attenuation through the channel. If signaling edge rates are made as sharp as possible from a given transmitter but the channel attenuation is still too great, then the value of C_C in the first coupling stage and the ratio of $C_C : C_P$ in the second coupling stage must be increased to compensate for the additional loss. However, changes to the capacitance values are directly realized by changes in the physical geometry of the coupling elements and the allowable gap between capacitor plates shrinks rapidly as the per-side dimension of the capacitor is reduced (*see Figure 16*). If the coupling and parasitic capacitor values are increased to compensate for the losses in the channel, then the achievable I/O density will suffer. Large values of C_C increase the area required to implement the coupling capacitor and / or require the physical package to support very small chip-chip gaps. The choice of coupling capacitor must be made to balance the tradeoff between capacitor dimensions, achievable driver edge rates, and tolerable loss through the channel.

3.3 Inductively Coupled Interconnects

Inductively-coupled interconnection (LCI) systems can operate over a wider range of chip-chip or chip-substrate gap distances than CCI systems and will provide an alternative to CCI systems in some situations. However, the design complexity of LCI systems is significantly greater than that of CCI systems. As such, a detailed analysis of a coupled inductor model will be presented. A discussion of the issues relevant to overall system performance will be given along side this model development.

3.3.1 Coupled Inductor Model

There are many ways to model a pair of coupled inductors. Choosing an appropriate model is fundamental to being able to understand how physical design parameters impact electrical performance.

One possibility for a coupled inductor model is shown in Figure 17. This model employs two instances of the inductor model used extensively in the literature [34, 35, 36] but adds the elements 'k' and 'C_C' to account for mutual coupling and parasitic capacitance between inductors. Recall that in the basic inductor model, L represents the inductance value, R_W models the series winding resistance, and the remaining parameters model parasitics.

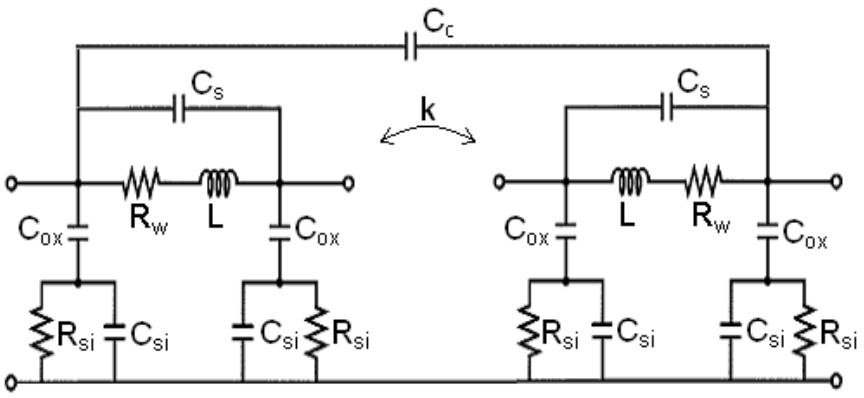


Figure 17 Lumped element model of coupled inductors

If the coupled inductors are driven such that one terminal of each inductor is at ground potential, then several of the elements in Figure 17 are shorted to ground and the model can be simplified significantly while still providing an effective means to model couple inductor performance. In this case the model reduces to the schematic shown in Figure 18.

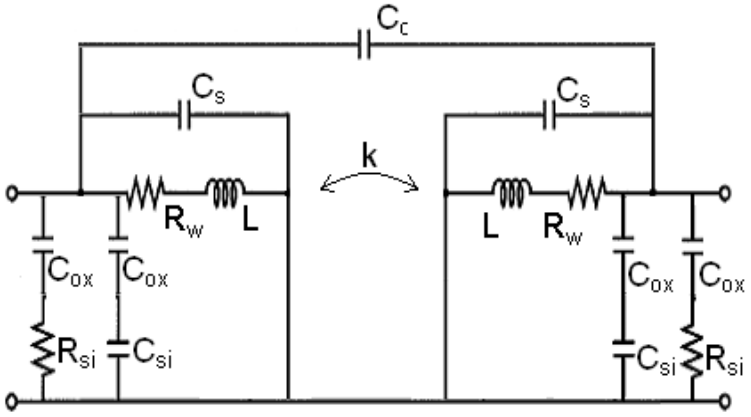


Figure 18 Lumped element model of single-ended coupled inductors

The model of Figure 18 can be further simplified by recognizing that for each inductor, C_S, is in parallel with the series combination of C_{OX} and C_{SI}. These three capacitors can be condensed into a single capacitor and represented as C_P. Moreover, R_{SI} and C_{OX} can be represented as a single resistor R_P with only a small impact on the ability of the model to capture the high-end frequency-dependence of the actual coupled inductors.

A coupled inductor model that embodies the above simplifications is shown in Figure 19 and will be used as the basis for the coupled inductor analysis to follow. This model is different from the stacked, coupled inductor

model presented by Mohan [36] and Niknejad [39] in two ways. First of all, both Mohan and Niknejad model parasitics related to a common path to the system ground between inductor terminals (although Mohan models the ground parasitics with a capacitor and Niknejad models the ground parasitics with a resistor). The model presented in Figure 19 does not include parasitics between the ports and system ground since the inductors for chip-chip AC coupling are fabricated on different integrated circuits and have different paths to ground. Secondly, this model includes the shunting parasitic term R_P to model the series combination of C_{OX} and R_{SI} although in practice this term is used as a parameter to fit the high-end frequency and phase response of the model to measurements.

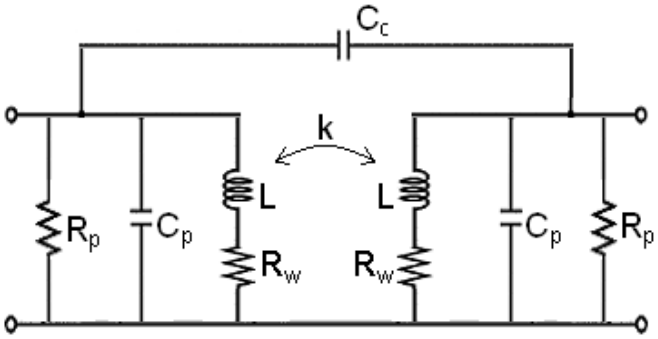


Figure 19 Simplified coupled inductor model (basis of analysis)

This model can be used to analyze the performance of inductive coupling stages in both lumped and distributed LCI systems. Lumped LCI systems can be defined as the class of systems that communicate over electrically short interconnection distances. Figure 20 shows a system-level schematic of a lumped LCI system. The performance of this type system can be predicted by using an appropriate circuit model for the transceiver along with the coupled inductor model of Figure 19. This type of system can be implemented in a number of contexts including 3D IC packaging and L0 or L1 packages.

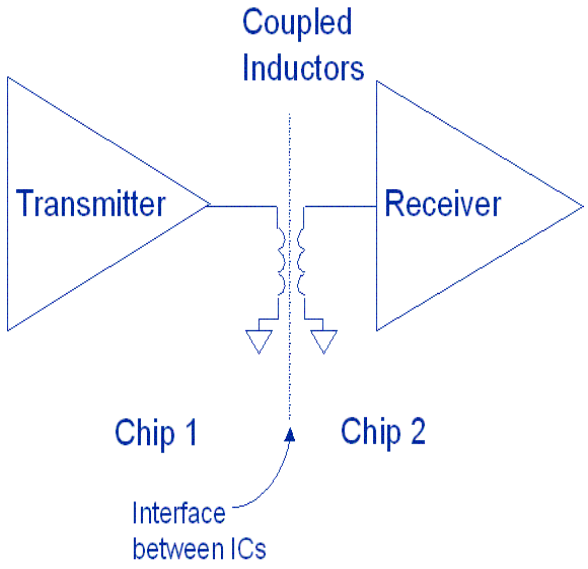


Figure 20 Schematic of a lumped LCI system

Distributed LCI systems can be defined as the class of systems that communicate over electrically long interconnection distances. Figure 21 shows a system-level schematic of a distributed LCI system. The performance of this type system can be predicted by using appropriate circuit-level models for the transceiver and routing along with two instances of the coupled inductor model of Figure 19. This type of system can be implemented in a number of contexts including board-level connectors and L1- or L2- packages.

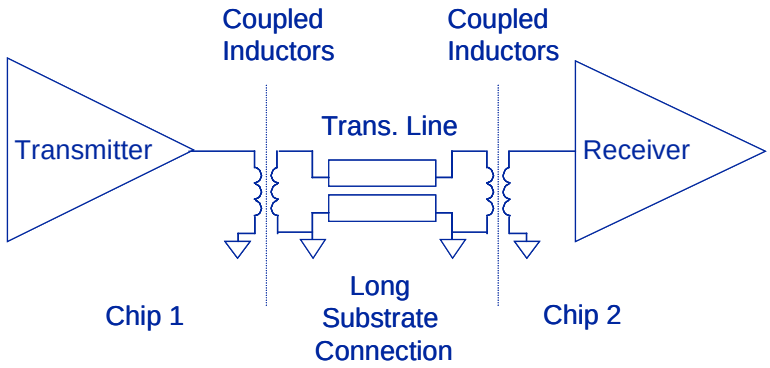


Figure 21 Schematic of a distributed LCI system

3.3.2 Correlation of Model to Physical Geometry

Although the exact values depend upon the specific fabrication process and geometric layout, each of the components in the model of Figure 19 can be related to one or more aspects of the physical geometry of the coupled inductors. Figure 22 presents the key geometrical parameters that impact the electrical performance of spiral, coupled inductors. With respect to the figure, 'W' denotes the width of the metal windings and 'T'

represents the thickness, 'S' indicates the space between metal windings, 'OD' is the outer diameter of the inductors, 'ID' refers to the inner diameter, the parameters 'X', 'Y', and 'Z' refer to the center-to-center offset between inductors in x-, y-, and z-directions, respectively, and 'N' (although not explicitly labeled in the figure) represents the number of turns in the inductors. Two comments are needed to clarify nomenclature that will be used in the following discussion. First of all, any of the previous electrical model or geometric parameters may be appended with the number '1' to indicate the parameter is being discussed with respect to the primary of the coupled inductors (i.e. the transformer input inductor) or with the number '2' to indicate the parameter is being discussed with respect to the secondary of the coupled inductors (i.e. the transformer output inductor). Secondly, the x- and y-offset are intended to represent lateral offset of the inductors and the z-offset represents the vertical distance between the faces of the coupled inductors.

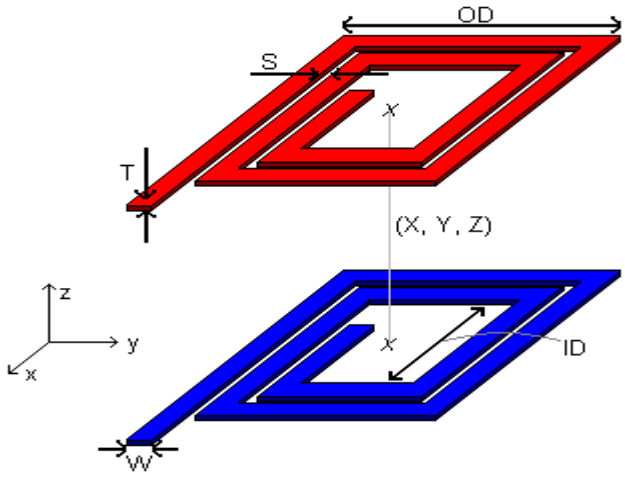


Figure 22 Geometrical parameters for coupled inductor design (isolated)

The value of inductance (L) and the mutual coupling (k) are of primary importance in the coupled inductor model. The inductances in the transformer are primarily impacted by the diameter and number of turns of the inductors [144].

Coupling between inductors is a result of the amount of magnetic flux from one inductor that penetrates a neighboring inductor. This coupling is dependent upon both the amount and strength of magnetic flux that an inductor generates and the distance between inductors. Thus, the coupling coefficient between stacked inductors is primarily influenced by the size of the x-, y- and z-offsets relative to the inductor diameters. Assuming two stacked, 3 turn inductors with diameters equal to 100µm, Figure 23 shows that k falls from roughly 0.8 with a z-offset of 2µm to roughly 0.6 at an offset of 4µm and to substantially less than 0.5 at an offset greater than 8µm. It

is important to note that the z-offset must be just a few percent of the inductor diameter to achieve coupling better than 0.8.

Also shown in Figure 23 is the impact that metal width and spacing have on the coupling coefficient on 3-turn square inductors with 100µm outer diameters. For constant metal width of 2µm, an inter-winding spacing of 1µm results in a coupling coefficient of 0.48 at a z-offset of 6µm. In order to increase k to 0.55, one of two design changes could be made: the z-offset could either be reduced to about 4µm (a 33% reduction in gap height) or the inter-winding spacing could be *increased* to 8µm while keeping the diameter constant. A similar trend is noticed if the data is analyzed from the viewpoint of constant spacing and variable winding width – for a fixed spacing, wider windings tend to improve mutual coupling. These effects upon mutual coupling become less noticeable as metal width and spacing continue to increase.

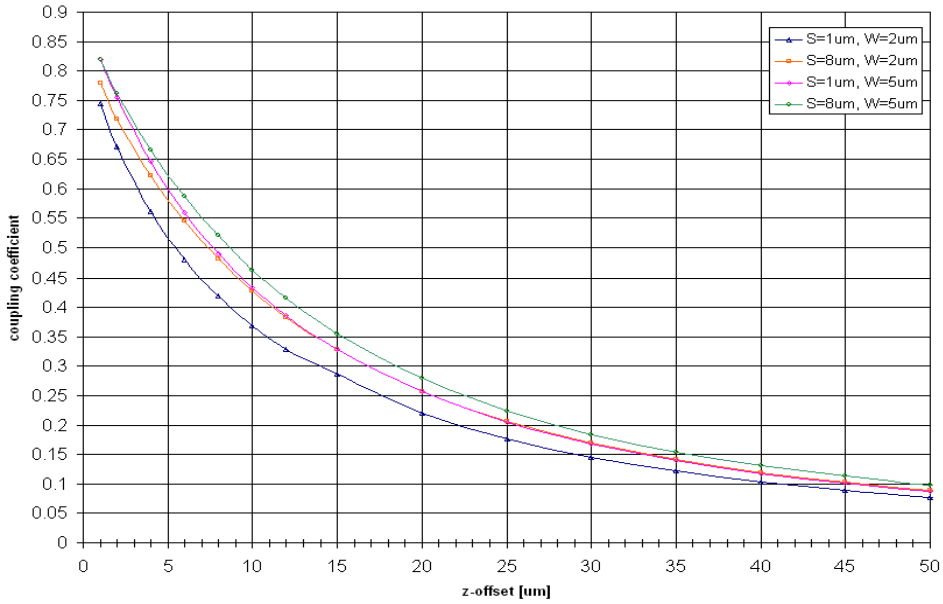


Figure 23 Coupling coefficient as a function of z-offset
100µm diameter inductors, 3 turns

The winding resistance (R_W) is mainly determined by the width, thickness and length of the inductor windings. For example, R_W increases linearly with the length of the inductor windings. A designer can control R_W by using fewer turns, wide inductor windings, and / or multiple metal levels strapped by vias to create effectively thicker windings.

The parasitic capacitances (C_C and C_P) and the shunt resistances (R_P) are determined by substrate resistivity, grounding structures near the inductors, and the x-. y-. and z-offsets between inductors. Modeling programs such

as Ansoft HFSS, OEA Spiral or ASITIC are recommended to estimate the values of these parasitics for a specific geometric and process configuration. As a general rule, R_P decreases as the number and / or quality of the grounding structures near the inductors increases since currents induced in the substrate encounter less resistance on their way to the system ground potential; C_C is maximized by zero lateral offset and a small vertical separation between inductors; and C_P is minimized by either shielding the inductors from the substrate [37, 56] or by increasing the distance between the substrate and the inductors.

A number of secondary effects complicate the process of picking a specific geometry to match a desired electrical performance. For instance, if a given inductor has a winding resistance that must be lowered, then several physical changes could be made to the coupled inductor layout to achieve this goal. If OD is kept constant and W is increased, then both R_W and L decrease. However, if ID is kept constant and W is increased, then R_W is decreased but L is increased. Moreover, there are any number of geometric configurations that can result in different coupling coefficients, winding resistances and parasitics for a fixed value of inductance. Figure 24 illustrates this point by showing the relationship between R_W and L for several combinations of W and S for designs considered for fabrication in a TSMC 0.35µm process. With reference to the figure, an inductance of 3nH could be achieved with a winding resistance anywhere in the range of 19Ω to 70Ω. Thus, the design space for inductors and transformers is vast but must be carefully explored to develop inductors suitable for a given application.

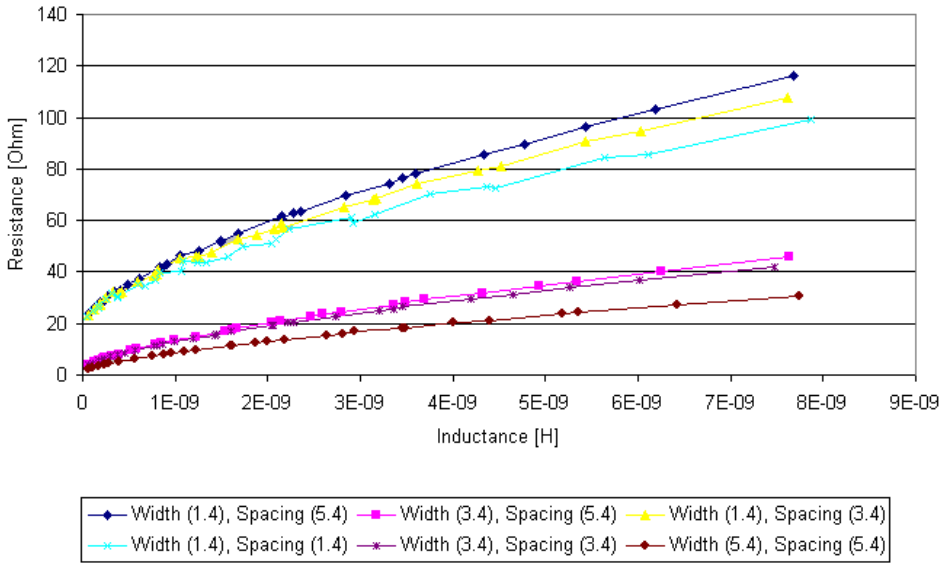


Figure 24 Inductor winding resistance as a function of inductance, winding width, and inter-winding spacing
Winding width and inter-winding spacing reported in µm

3.3.3 Model Development and Analysis

As the preceding discussion has shown, changes in a single variable of the physical design of coupled inductors can impact the values extracted for each of the elements in the coupled inductor model. The following sensitivity analysis shows how changes in component values impact the electrical performance of the coupled inductors. This analysis also exposes issues that must be considered in order to design a communication system with inductively coupled elements. This following analysis is decomposed into several parts starting with the case of ideal coupled inductors. Increasing levels of detail are added to the analysis until finally the complete model is analyzed.

3.3.3.1 Inductance

Ideal coupled inductors (i.e. transformers) can be represented schematically as shown in Figure 25. In this configuration, two inductors are perfectly coupled to each other (i.e. the coupling coefficient k = 1.0). This perfect coupling forms a circuit element with a high-pass frequency response as described by Equation 2.

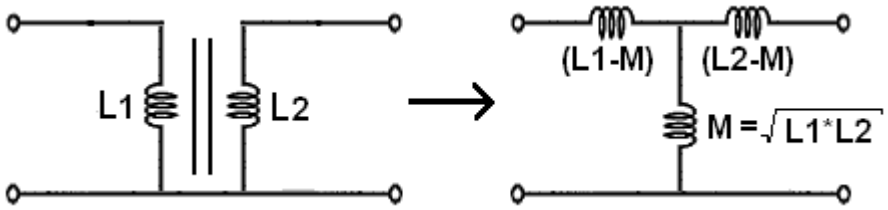


Figure 25 Equivalent models of perfectly coupled inductors

$$\frac{V_{LOAD}}{V_S} = \frac{\sqrt{L_1 L_2}\, R_L\, s}{\left(R_S L_2 + R_L L_1\right)s + R_S R_L}$$

Equation 2 Voltage transfer function for ideal coupled inductors

High-density LCI systems will be constrained to use inductances of at most a few tens of nanohenries (nH). This constraint will result in LCI systems having a 3dB frequency high enough that square wave pulses input into the primary will be converted / filtered into short voltage or current pulses at the output. Stated in another way, the coupled inductors differentiate the input signal and in effect perform edge detection. The -3dB frequency exists for ideal coupled inductors because the transformer appears as an impedance in parallel with the load. At low frequencies the transformer presents a small impedance to the load and effectively shorts the output voltage to ground. The impedance of the transformer increases with frequency so the short-circuiting effect is reduced with

increasing frequency. The 3dB frequency occurs when the transformer impedance is ¼ of the impedance it sees (for transformers with equal primary and secondary inductances). For frequencies much greater than the 3dB frequency, the impedance of the coupled inductors increases beyond that of its load and the network simply reflects the impedance seen at its primary to its secondary and vice versa.

To illustrate the behavior of a set of ideally coupled inductors, Figure 26 shows representative frequency responses (both magnitude and phase) of four different transformers in a 50Ω system (i.e. source and load impedances both equal 50Ω). In the case where $L_1 = L_2 = 50$nH the -3dB frequency occurs at about 80MHz, and for $L_1 = L_2 = 5$nH the -3dB frequency occurs at 800MHz. Increasing the inductance value lowers the -3dB frequency. The phase response for both transformers is indicative of a first-order system since the phase changes only 90° across frequency. In this system, the -3dB frequency occurs when the phase is equal to 45°.

Also shown in Figure 26 is the effect upon the magnitude and phase response for transformers where the primary and secondary inductances are of different values. In this case, a T-model (*see Figure 25*) can be used to understand the response. The model consists of three elements where the mutual inductance (i.e. the shunt element) has a value that is equal to the coupling coefficient multiplied by the geometric mean of the primary and secondary inductances. In the ideal case, the coupling coefficient equals unity so the mutual inductance is simply the geometric mean of the primary and secondary inductances. The two series elements have values equal to the primary (or secondary) minus the mutual inductance. The effect of non-equal primary and secondary inductances results in an inductor model that has "leakage" inductors in series with its ports. As shown in Figure 26, these inductors result in attenuation through the channel.

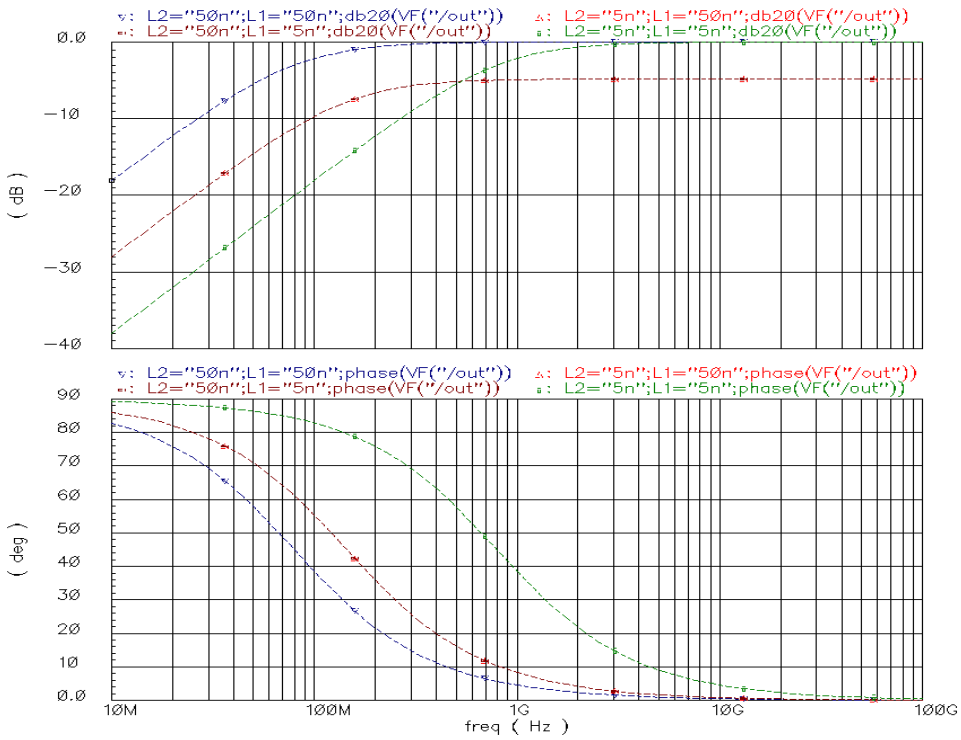


Figure 26 Magnitude and phase responses of four sets of ideal coupled inductor
$L_1 = L_2 = 50nH$ (blue), $L_1 = L_2 = 5nH$ (green),
$L_1 = 5nH$, $L_2 = 50nH$ (brown), $L_1 = 50nH$, $L_2 = 5nH$(red)
$R_S = R_L = 50\Omega$

The response of both transformers composed of equal inductances from Figure 26 to a positive-going, input voltage step with 70[ps] rise time is illustrated in Figure 27. The time-domain outputs demonstrate the filtering expected from the AC response – low frequency content is removed and a voltage pulse results on the transformer output. The step response for the transformer with L = 50nH retains more low frequency content from the input than does the transformer with L = 5nH. As a result, the response of the transformer with L=5nH settles to 10% of the peak value in about 460ps whereas the larger transformer requires 4.6ns to settle to 10% of the peak value. Although smaller inductances result in more heavily filtered pulses from the transformer, the duration of the step response is shorter. The response is similar in magnitude but opposite in polarity for a negative-edge, input voltage step.

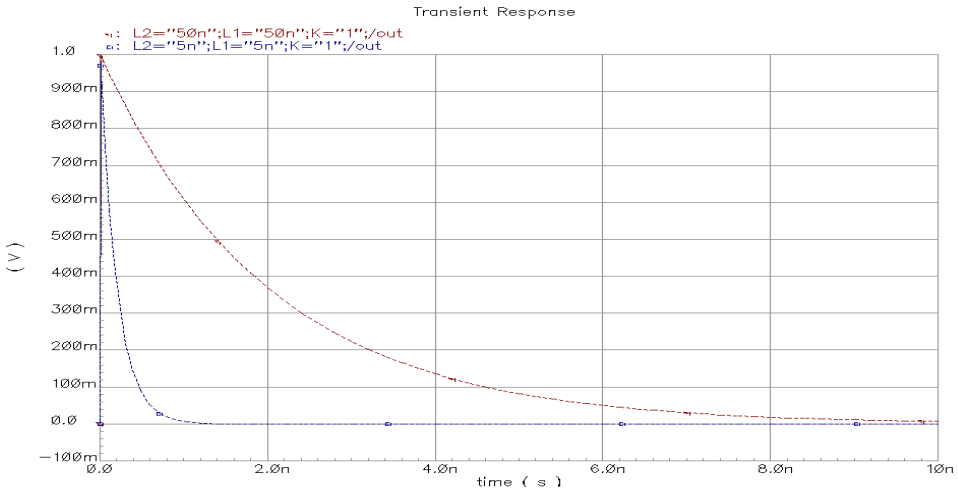


Figure 27 Step response for ideal coupled inductors
L1 = L2 = 5nH (blue) & 50nH (brown)

An important aspect of the filtering behavior for data transmission is the fact that this response decays quickly over the length of a single bit time. As a result, coding is not needed on long streams of logic 1's and 0's to prevent ISI. Instead, signaling can be done only on data changes, and the duration of the step response can be examined to decide the point in time when subsequent data bits should be transmitted. For example, if an application could tolerate 10% ISI, then with respect to Figure 27, the transformer composed of 5nH inductors could be used to support an NRZ data rate of 2.1GHz (i.e. the inverse of settle time).

As a rule of thumb, the highest frequency inputs can be transmitted via pulse signaling with low ISI through transformers composed of small and equal inductances. Slightly lower frequency inputs must be used to reduce ISI for transformers where the primary inductance is not equal to the secondary inductance.

3.3.3.2 Coupling Coefficient

Achieving high I/O densities in LCI systems will lead to inductor sizes on the order of 100µm in diameter. The inductor size combined with the fact that chip-substrate gaps will be on the order of a 1µm to 10µm will result in coupled inductors that cannot achieve perfect coupling. Imperfectly coupled inductors can be modeled with two inductors and a coupling coefficient k or with an equivalent T-model as shown in Figure 28.

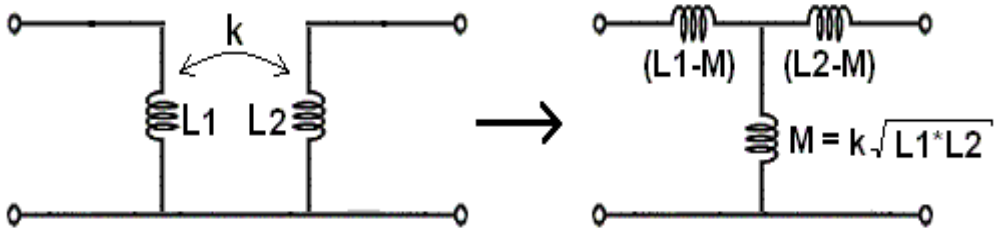


Figure 28 Equivalent models of coupled inductors with imperfect coupling

Imperfect coupling has a profound impact upon the coupled inductors, and this impact can be easily understood by considering the T-model of Figure 28. This model shows that imperfect coupling between inductors of value L is equivalent to three inductors: a mutual inductance and two leakage inductors. The mutual inductance has a value equal to the coupling coefficient multiplied by the geometric mean of the primary and secondary inductors and the leakage inductances have values of L1 or L2 less the mutual inductance.

The T-model for imperfectly coupled inductors looks almost identical to the model for perfectly coupled inductors with unequal primary and secondary inductances (*recall Figure 25*). However as shown in Equation 3, an expression for the voltage transferred across an imperfectly coupled transformer can be derived to reveal an important difference.

$$\frac{V_{LOAD}}{V_S} = \frac{M R_L s}{\left(L_1 L_2 - M^2\right)s^2 + \left(R_S L_2 + R_L L_1\right)s + R_S R_L}$$

Equation 3 Voltage transfer function for imperfectly coupled inductors

In Equation 3, R_S is the source impedance, R_L is the load impedance, s is the Laplace transform variable, and the remaining variables are taken as defined in Figure 28. Upon inspection of the denominator of Equation 3 it can be seen that, unlike the case with perfectly coupled inductors with unequal primary and secondary inductors, the leakage inductance caused by imperfect coupling introduces an additional pole into the AC response. This is true because the $(L_1L_2 - M^2)s^2$ term vanishes for perfect coupling but persists for imperfect coupling. The additional pole causes the response to become bandpass. Moreover, as the coupling coefficient decreases, the bandwidth of the transformer decreases and the loss through the transformer increases.

The impact of imperfect coupling upon the magnitude response is illustrated in Figure 29. For the figure, R_S and R_L are set to 50Ω, both primary and secondary inductances are set to 5nH and k is set to 0.6, 0.8 and 1.0. As

predicted from Equation 3, the frequency response exhibits bandpass behavior and the attenuation increases as k increasingly departs from unity.

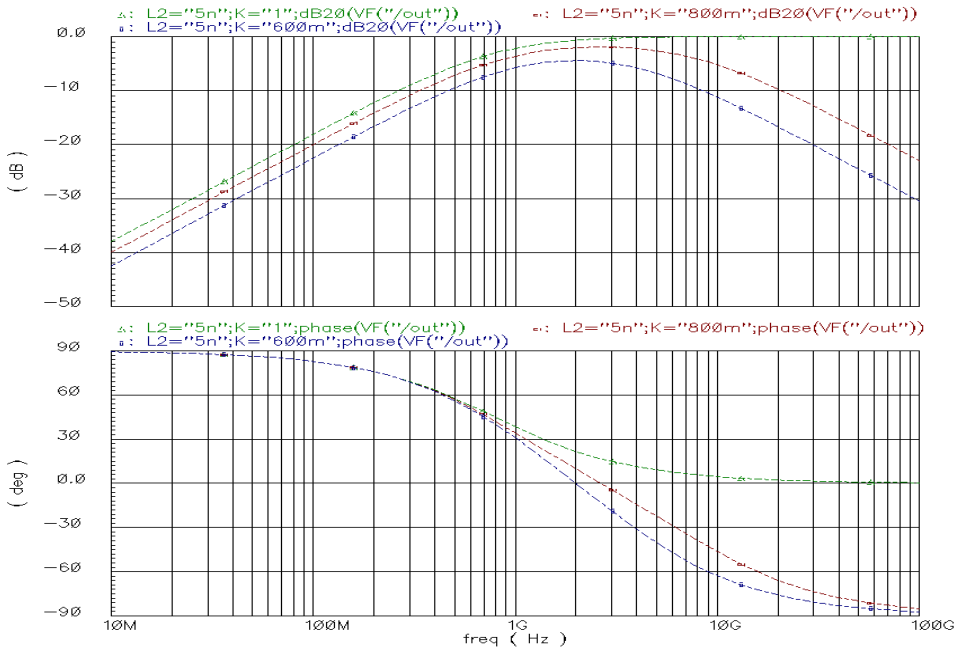


Figure 29 Magnitude and phase response of coupled inductors with varying coupling coefficient
k = 0.6 (blue), 0.8 (brown) and 1.0 (green)
$R_S = R_L = 50\Omega$

For example, when k=1.0, the transformer has a high pass response with a –3dB frequency at approximately 800MHz and no loss at high frequencies. When k is decreased to 0.8, the bandpass response is centered at 2.5GHz and has a lower 3dB frequency at ~750MHz and an upper 3dB frequency at 9.6GHz. The minimum loss through the transformer when k=0.8 is -1.9dB. The phase response also reveals the presence of the pole introduced by imperfect coupling due to the additional 90° phase shift across frequency.

However, the fact that the load impedance appears in the numerator of the voltage transfer function allows for a mechanism to partially compensate for imperfect coupling. Focusing on the frequency response from Figure 29 for k=0.8, Figure 30 shows that the bandwidth of the coupled inductors is extended significantly by increasing R_L from 50Ω to 50kΩ. For example, increasing R_L from 50Ω to 5kΩ changes the lower and upper 3dB points from approximately 750MHz and 9.6GHz to 1.6GHz and 445GHz, respectively. Thus, increasing R_L can significantly extend the bandwidth of the coupled inductors.

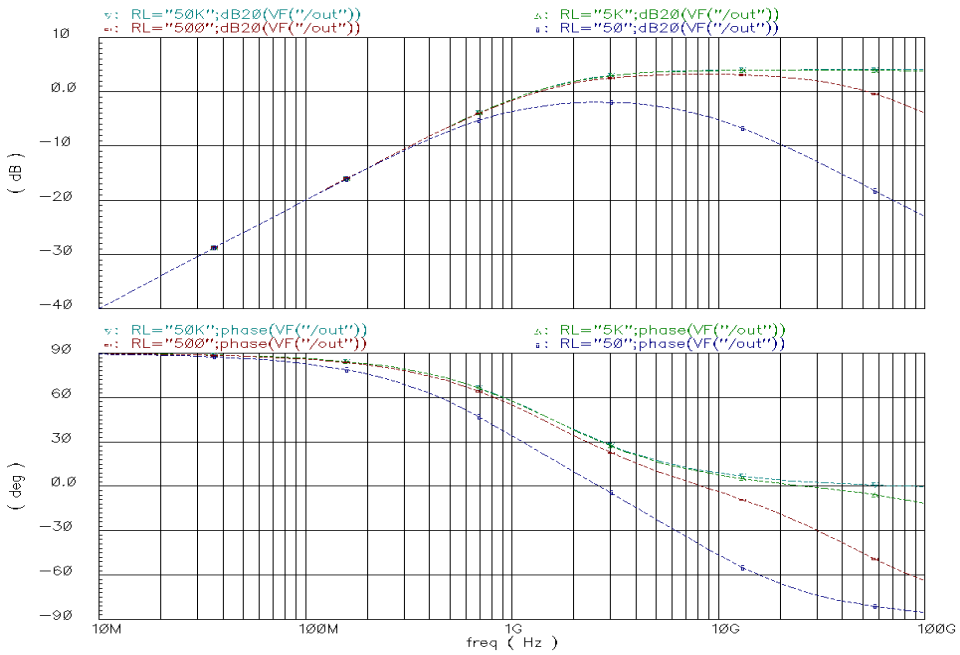


Figure 30 Magnitude and phase response of coupled inductors for different values of load impedance
R_L = 50Ω (blue), 500Ω (brown), 5kΩ (green) and 50kΩ (cyan)
R_S = 50Ω, k = 0.8

There is a limit to the amount of benefit that can be derived from large load impedances. For example, in distributed LCI systems, a low impedance transmission line will terminate the first stage so the behavior of inductive coupling networks must be understood for both high and low impedance loads.

Figure 31 shows the impact of imperfect coupling upon the step response for source and load impedances of 50Ω. As with the figure for the frequency response, the inductances are set to 5nH and k is taken as 0.6, 0.8 and 1.0. In addition, the step response assumes an input pulse with a rise time of 70ps. For values of k less than unity, the bandpass nature of the frequency response filters the leading edge of the time-domain response and results in a noticeable rise time to the peak voltage, and as k decreases, the attenuation through the transformer increases. With k equal to unity, the peak voltage through the transformer is 944mV and the time required for the output voltage to settle to 10% of the peak voltage is 530ps. When k drops to 0.6, the peak voltage through the transformer is only 458mV but the time required for the output voltage to settle to 10% of the peak voltage remains roughly 530ps.

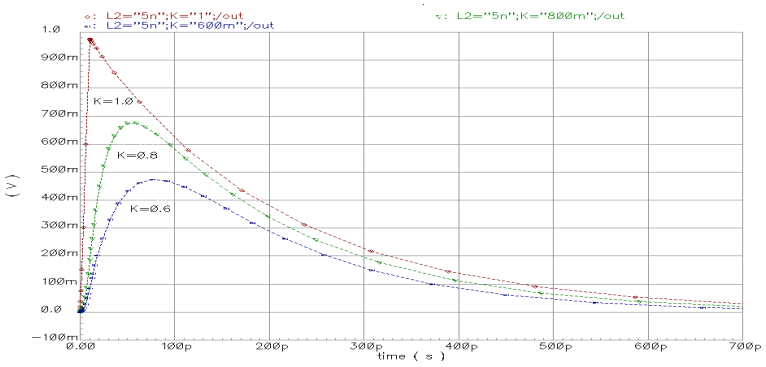


Figure 31 Step response of coupled inductors with varying coupling coefficient and low impedance termination
k = 0.6 (blue), 0.8 (brown) and 1.0 (green)
$R_S = 50\Omega$, $R_L = 50\Omega$

Figure 32 considers the time-domain response for high impedance loads. This figure shows the step response for a source impedance of 50Ω, load impedance varied from 50Ω to 5kΩ, inductances of 5nH and k of 0.8. Additionally, the step response assumes an input pulse with a rise time of 70ps. As with the response for a low impedance termination, the leading edge of the time-domain response is filtered and results in a noticeable risetime to the peak voltage. As R_L decreases, the attenuation through the transformer increases. The figure shows that the peak voltage increases from 641mV to 1.1V simply by increasing R_L from 50Ω to 500Ω. Equally important, increasing R_L from 50Ω to 500Ω reduces the time required for the response to settle to ten percent of the peak voltage from 530ps to 330ps (i.e. a 38% reduction in settling time).

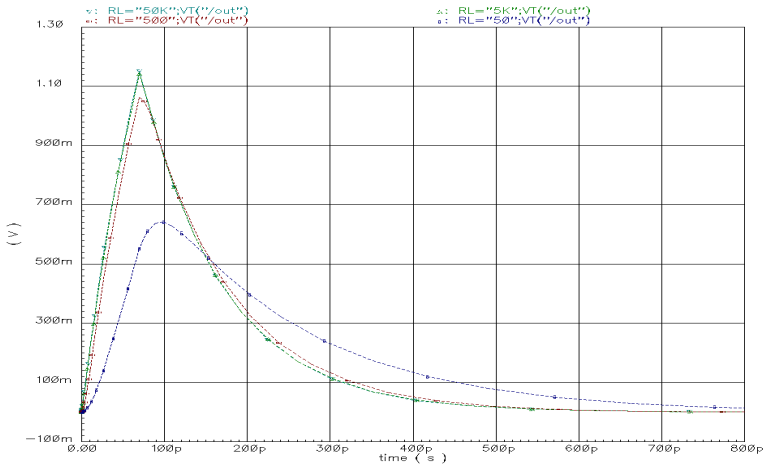


Figure 32 Step response of coupled inductors with varying coupling coefficient and high impedance termination
$R_L = 50\Omega$ (blue), 500Ω (brown), $5k\Omega$ (green) and $50k\Omega$ (cyan)
$R_S = 50\Omega$, k = 0.8

In terms of LCI system design, imperfect coupling between inductors can be compensated to some extent with increased load resistance. In distributed systems, a low impedance transmission line will terminate the first inductively coupled stage; so in these systems, the coupling coefficient must be large enough to limit the loss through the coupled inductors. However, near-unity coupling coefficients imply large diameter inductors in close proximity to each other and this presents a challenge toward achieving high I/O densities.

3.3.3.3 Winding Resistance

Coupled inductors in LCI systems will generally be designed to simultaneously minimize the area consumed but maximize the inductance values. This tradeoff can result in the use of inductors with narrow windings that suffer significantly from series winding resistance. A model of imperfectly coupled inductors with series winding resistance and an equivalent T-model are presented in Figure 33.

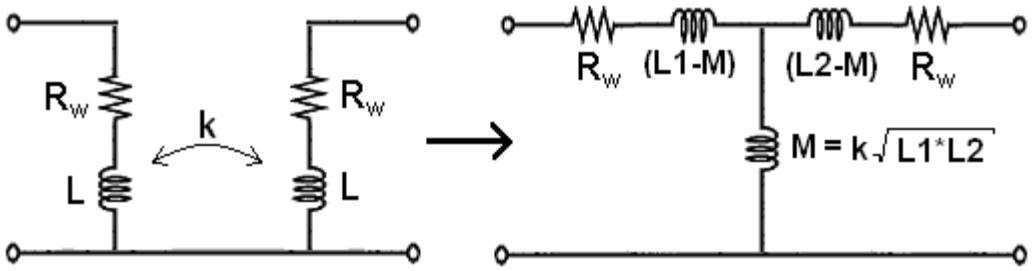


Figure 33 Equivalent models of coupled inductors with imperfect coupling and winding resistance

The equivalent T-model in Figure 33 closely resembles the model of coupled inductors without winding resistance, and the voltage transfer function as shown in Equation 4 verifies this similarity. By comparing Equation 4 to Equation 3 it can be seen that the presence of winding resistance increases the effective source and load impedances and has an impact upon the system poles. Since the winding resistance does not affect the system zero, large winding resistance cannot be used to offset the effect of imperfect inductor coupling upon system performance.

$$\frac{V_{LOAD}}{V_S} = \frac{M R_L s}{\left(L_1 L_2 - M^2\right)s^2 + \left(\left(R_S + R_{W1}\right)L_2 + \left(R_L + R_{W2}\right)L_1\right)s + \left(R_S + R_{W1}\right)\left(R_L + R_{W2}\right)}$$

Equation 4 Voltage transfer function for imperfectly coupled inductors with winding resistance

Analysis reveals that the winding resistance slightly increases the 3dB frequency of the magnitude response as compared to the system without winding resistance. The dual impacts of winding resistance and imperfect

coupling upon the magnitude response are shown in Figure 34 and Figure 35. For these figures, R_S and R_L are both set to 50Ω; the inductances are set to 5nH; R_W is taken as 0Ω, 10Ω, and 20Ω; and k is set to 1.0 (Figure 34) and 0.8 (Figure 35). Recall that perfect coupling results in a highpass frequency response and imperfect coupling results in a bandpass response. With this in mind, the figures show that winding resistance increases the attenuation in the passband. For example, with perfect coupling and no winding resistance, the coupled inductors can pass a 1V input with no attenuation. As the winding resistance is increased to 20Ω, the peak voltage through the passband drops to about 720mV – a 28% reduction.

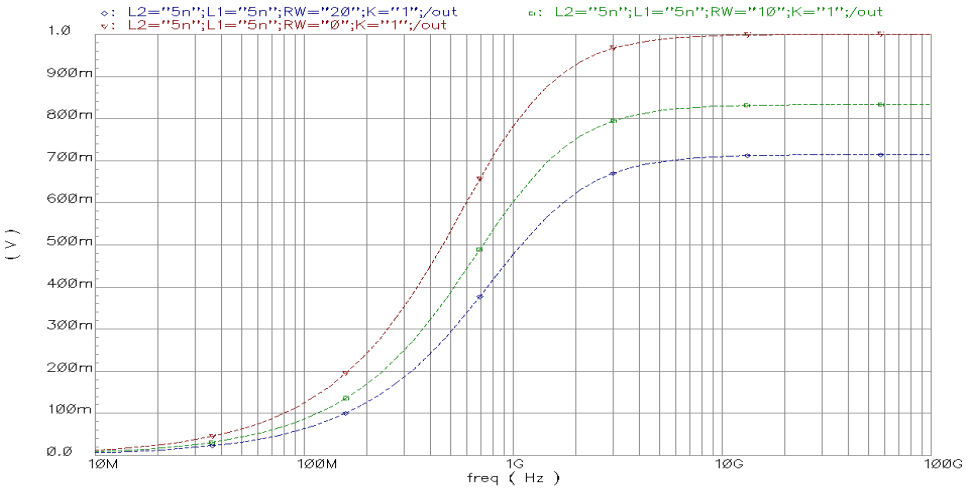


Figure 34 Impact of winding resistance upon magnitude response of perfectly coupled inductor for 50Ω termination
R_W = 0[Ω] (red), 10[Ω] (green), 20[Ω] (blue)
k = 1.0

With imperfect coupling, winding resistance has a similar impact. For example, with k = 0.8, the coupled inductors can pass 800mV of a 1V input signal. However, as the winding resistance is increased to 20Ω, the peak voltage through the passband drops to about 570mV – a 29% reduction

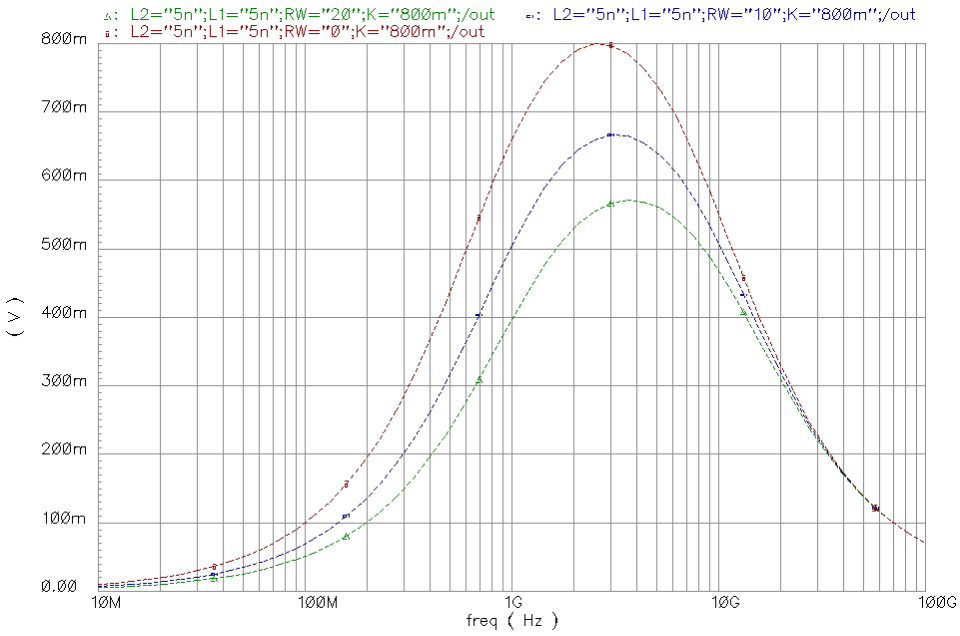


Figure 35 Impact of winding resistance upon magnitude response of imperfectly coupled inductor for 50Ω termination
R_W = 0[Ω] (red), 10[Ω] (blue), 20[Ω] (green)
k = 0.8

As is the case for imperfect coupling, the situation can be improved by increasing the load resistance since R_L appears in the numerator of the voltage transfer function. Figure 36 shows the frequency response when the load impedance is increased to 500Ω. In this figure, R_S is set to 50Ω; R_L is set to 500Ω (responses for R_L = 50Ω are shown in grayscale to highlight the impact of increased R_L); the inductances are set to 5nH; k is taken as 0.8; and R_W is taken as 1mΩ, 9Ω, and 18Ω. The simulation results in the figure show that increasing R_L from 50Ω to 500Ω can increase the response as much as 7dB – with the gains being more profound when the winding resistance is large.

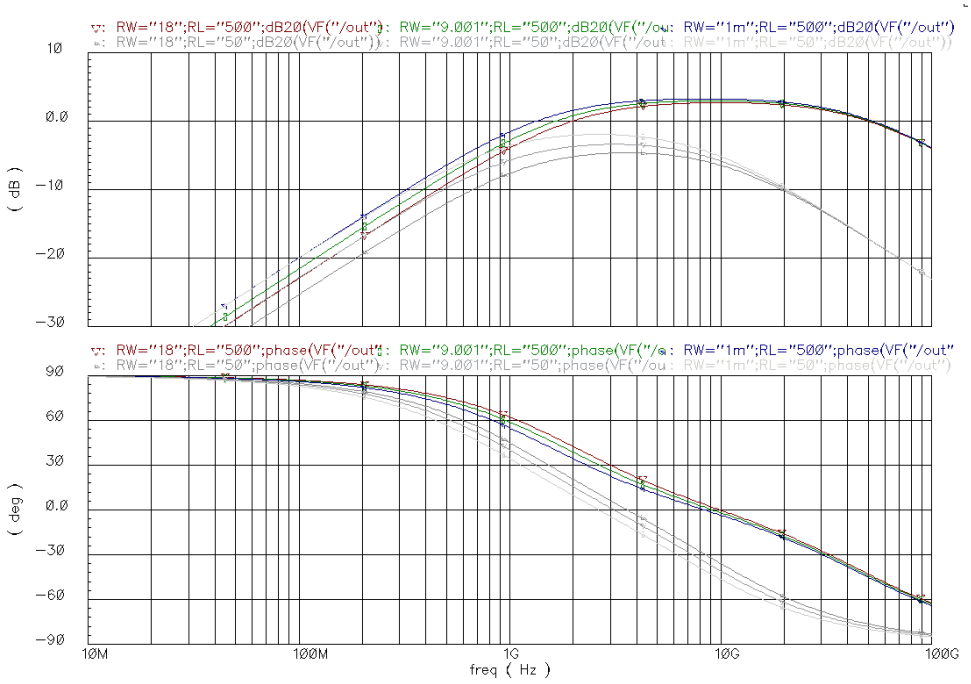


Figure 36 Impact of winding resistance upon magnitude response of imperfectly coupled inductor for 500Ω termination
R_W = 0[Ω] (red), 10[Ω] (green), 20[Ω] (blue)
k = 0.8

In the time-domain, winding resistance has the effect of adding attenuation but also slightly decreasing the settling time. Figure 37 illustrates this by showing the impact of winding resistance upon the step response for a system with k = 0.8 terminated in 50Ω. As before, the inductances are set to 5nH; R_W is taken as 0Ω, 10Ω, and 20Ω; and the step response assumes an input pulse with a rise time of 70ps. In the case where R_W = 0Ω, the peak voltage in the passband is 640mV and the time required to settle to 10% of the peak voltage is 532ps. However as R_W is increased to 20Ω, the peak voltage decreases to 454mV and the settle time is reduced to 404ps.

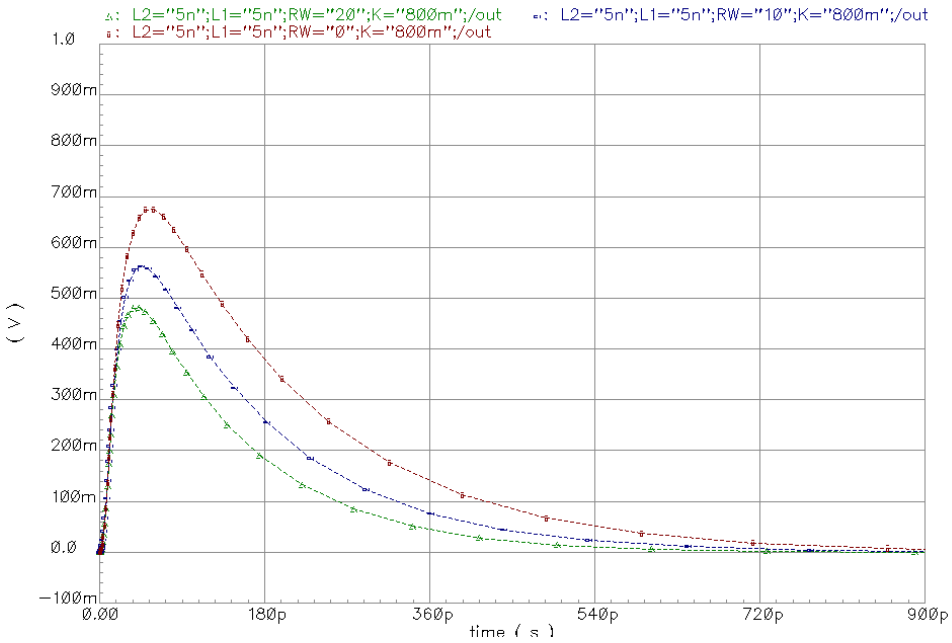


Figure 37 Impact of winding resistance upon step response for system terminated in 50Ω
R_W = 0[Ω] (red), 10[Ω] (green), 20[Ω] (blue)
k = 0.8

For higher impedance terminations, Figure 38 shows the impact of both winding resistance and imperfect coupling upon the step response for a system terminated in 500Ω. As before, the inductances are set to 5nH; k is set to 0.8; R_W is set to 1mΩ, 9Ω, and 18Ω; and the step response assumes an input pulse with a rise time of 70ps. The corresponding responses for R_L = 50Ω are shown in grayscale to underscore the impact of increasing the load impedance. The simulation results show with no winding resistance, increasing R_L from 50Ω to 500Ω increases the peak voltage from 640mV to 1062mV and decreases the 10% settling time from 532ps to 321ps. The impact is similar for large values of winding resistance. For example, when R_W is set to 20Ω, increasing R_L from 50Ω to 500Ω increases the peak voltage from 454mV to 918mV and decreases the 10% settling time from 404ps to 261ps.

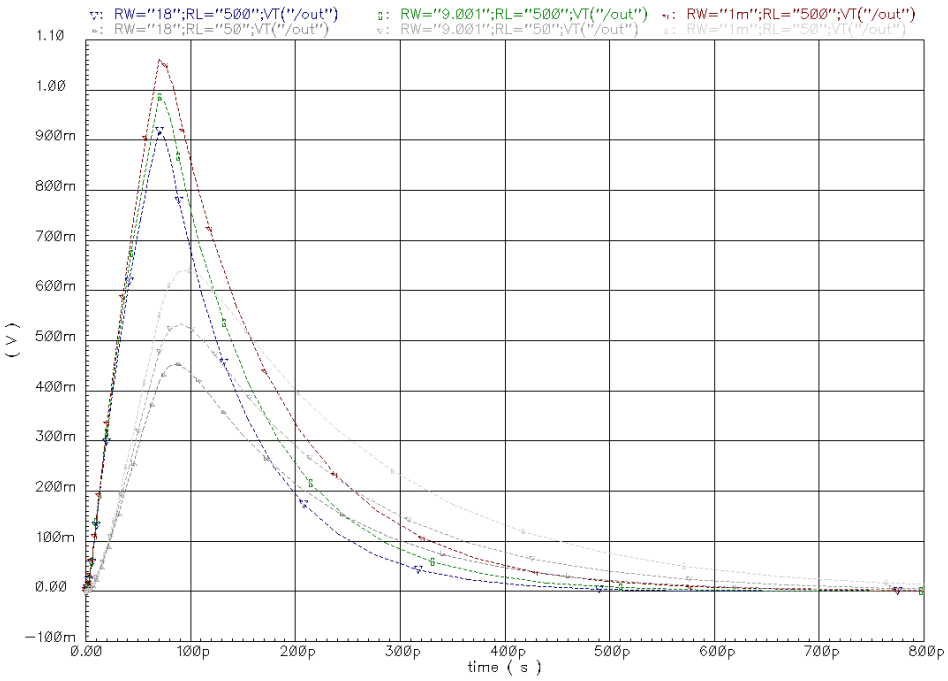


Figure 38 Impact of winding resistance upon step response for system terminated in 500Ω
R_W = 0[Ω] (red), 10[Ω] (green), 20[Ω] (blue)
k = 0.8

In terms of designing an LCI system, the effects introduced by winding resistance can be managed by careful design. Similar to the situation with imperfect coupling, winding resistance can be partially compensated with increased load resistance. However, since a low impedance transmission line will terminate the first inductively coupled stage of a distributed system, the winding resistance should be kept small in the first stage to minimize loss. Small winding resistance implies wide inductor windings and can increase inductor diameter if many turns are needed. For both lumped systems and the second coupling stage of distributed systems, higher winding resistance can be tolerated and this can lead to narrower windings, smaller diameter inductors and higher I/O densities.

3.3.3.4 Parasitic Capacitance

The presence of parasitic capacitance must also be taken into account since capacitance exists between both inductors and from each inductor to ground. Figure 39 shows a schematic of coupled inductors with parasitic capacitance, winding resistance and imperfect coupling.

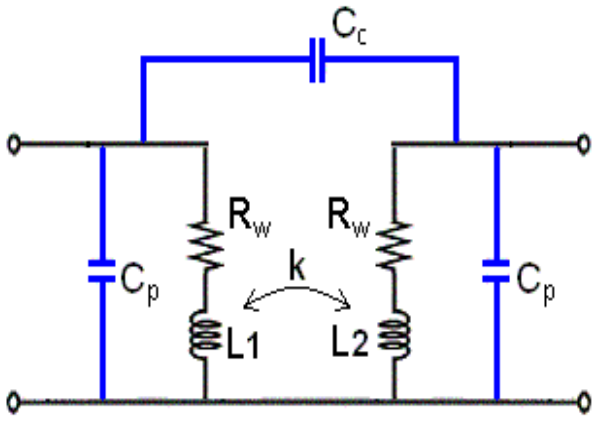
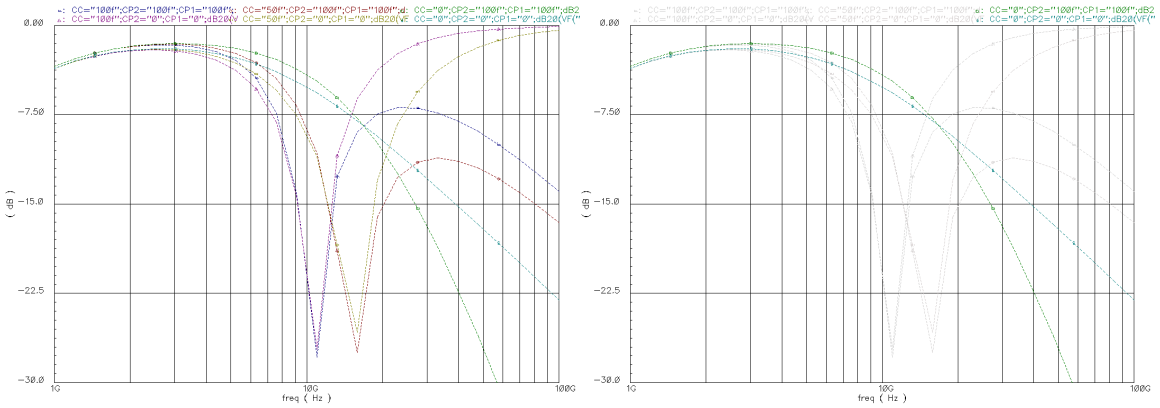


Figure 39 Equivalent model of coupled inductors with imperfect coupling, winding resistance, and parasitic capacitance
(left) Coupled inductors with imperfect coupling, winding resistance, and parasitic capacitance
(right) Capacitance associated with coupled inductors

As seen in Figure 39, the parasitic capacitances associated with coupled inductors are modeled by a Pi-network of capacitors and this looks much like a CCI channel. For LCI systems, parasitic capacitances in the femtofarad range are to be expected so these components will mainly impact the system response at high frequencies. The behavior associated with each of these capacitors is complex. The system becomes third order with respect to the Laplace variable s by adding the single coupling capacitor (C_C) to inductors coupled with a coefficient less than unity, but the system becomes fourth order by adding just the shunt capacitors (C_P) to inductors coupled with a coefficient less than unity.

A few generalities can be made about the effect of C_C and C_P upon the frequency domain performance of coupled inductors. To facilitate the discussion, Figure 40 shows the magnitude responses for the six coupled inductor permutations possible for C_P = 0 or 100fF and C_C = 0, 50fF or 100fF. The figure has been derived using $L_1 = L_2$ = 5nH, k = 0.8 and R_W = 10Ω. Figure 40 (a) shows all six of the responses. The three remaining sub-figures are for fixed values of C_C where each individual figure shows two colored curves corresponding to C_P equal to 0fF and 100fF. Considering Figure 40 (b), the blue curve shows the channel response when C_P = 0fF and the green curve shows the response for C_P = 100fF. As C_P is increased, the channel experiences slightly less attenuation through the passband but sharper rolloff for high frequencies. This trend is independent of the value of C_C as shown in Figure 40 (c) and (d) for C_C = 50fF and 100ffF, respectively. Also shown in Figure 40 (c) and (d) is the substantial impact that C_C has upon the frequency response. C_C disrupts the otherwise smooth bandpass behavior of the channel by introducing a notch in the response, and larger values of C_C result in this notch appearing at lower frequencies.



a) C_C = 0fF, 50fF 100fF; C_P = 0fF, 100fF

b) C_C = 0fF; C_P = 0fF, 100fF

c) C_C = 50fF; C_P = 0fF, 100fF

d) C_C = 100fF; C_P = 0fF, 100fF

Figure 40 Magnitude response of coupled inductors with parasitic capacitance
$L_1 = L_2$ = 5nH, k = 0.8, R_W = 10Ω

Reversing the winding sense of the inductors can mitigate the notch in the frequency response. That is, inductors can be physically oriented with respect to one another so that a current into one inductor will produce a current into or out of a specific terminal on the other inductor, and this orientation has a direct impact upon performance due to C_C. This physical orientation, although actually a geometric parameter, can be represented schematically by a dot convention. Simply stated, dots are placed at the terminals of each coupled inductor on a schematic in such a way that current flowing into the dot of one inductor induces a voltage with a positive reference polarity at the dot of the other inductor. Coupled inductor models that show the parasitic capacitances and that capture the winding sense are shown in Figure 41

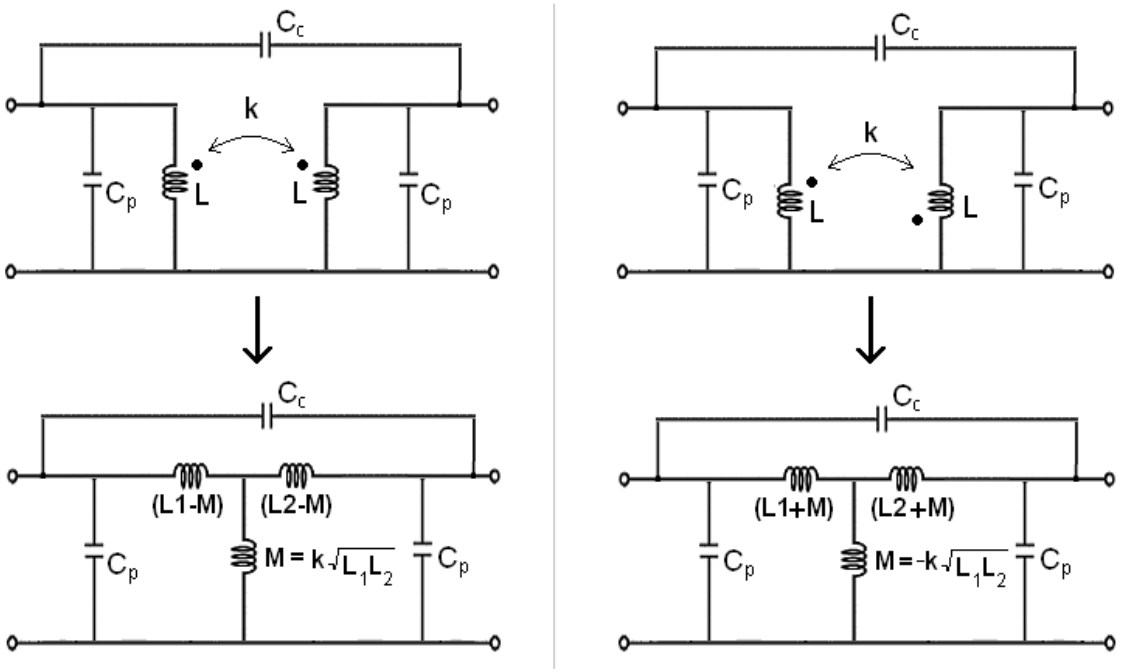


Figure 41 Equivalent models of coupled inductors with imperfect coupling, parasitic capacitance and winding sense
(left) in phase (or same) winding sense
(right) out of phase (or opposite) winding sense

Since the effects of C_C are seen independent of the presence of C_P, the behavior introduced by the coupling capacitance can be analyzed with a model that does not have the two C_P elements. The voltage transfer functions for coupled inductors with coupling capacitance are listed in Equation 5 and Equation 6 with the first equation valid for coupled inductors wound in phase and the second equation valid for coupled inductors with an opposite winding sense. These transfer functions are written to show explicitly the impact that C_C has upon the system. Comparing these equations, only one difference exists: the algebraic signs of both of the non-squared mutual inductance terms depend upon the winding sense. Although subtle, this difference has a profound effect upon system behavior.

$$\frac{V_{LOAD}}{V_S} = \frac{\left(\left(L_1L_2 - M^2\right)C_C s^2 + M\right)R_L s}{\alpha C_C s^3 + \left(L_1L_2 - M^2 + \beta_{in} C_C\right)s^2 + \left(R_S L_2 + R_L L_1\right)s + R_S R_L}$$

$$\alpha = \left(L_1L_2 - M^2\right)\left(R_S + R_L\right)$$

$$\beta_{in} = \left(L_1 + L_2 - 2M\right)R_S R_L$$

Equation 5 Voltage transfer function of coupled inductors capturing effect of same winding sense due to parasitic coupling capacitance

$$\frac{V_{LOAD}}{V_S} = \frac{\left(\left(L_1L_2 - M^2\right)C_C s^2 - M\right)R_L s}{\alpha C_C s^3 + \left(L_1L_2 - M^2 + \beta_{out} C_C\right)s^2 + \left(R_S L_2 + R_L L_1\right)s + R_S R_L}$$

$$\alpha = \left(L_1L_2 - M^2\right)\left(R_S + R_L\right)$$

$$\beta_{out} = \left(L_1 + L_2 + 2M\right)R_S R_L$$

Equation 6 Voltage transfer function of coupled inductors capturing effect of opposite winding sense due to parasitic coupling capacitance (C_C)

The impact of C_C upon coupled inductor performance and its dependence upon the winding sense can best be seen by graphing the trajectories of the poles and zeros of Equation 5 and Equation 6 in the complex plane as a function of C_C. These graphs can be created by substituting jω for s in the two voltage transfer functions, substituting values for each of the variables and then solving for and plotting the roots of both the numerators and denominators. Figure 42 shows the trajectories of the poles and zeros in the complex plane for coupled inductors as a function of C_C, R_L and winding sense. The graphs are derived for a system in which $L_1 = L_2 =$ 5nH, $R_W = 0$, $k = 0.8$ and $C_P = 0$. In the figure, the left side shows pole / zero trajectories for $R_L = 50\Omega$ and the right side shows trajectories for $R_L = 500\Omega$. Within each graph, C_C is varied from 1fF to 300fF. The trajectories of the poles of coupled inductors with the same winding sense are shown in red and the corresponding zeros are shown in magenta. The trajectories of the poles of coupled inductors with out of phase windings are shown in blue and the corresponding zeros are shown in green. For both graphs, the poles and zeros approach the origin for large values of C_C.

The stability of a system is related to the relative proximity of the poles and zeros to each other and to the jω axis. Pole / zero trajectory plots have value because they help to understand and even predict aspects of time

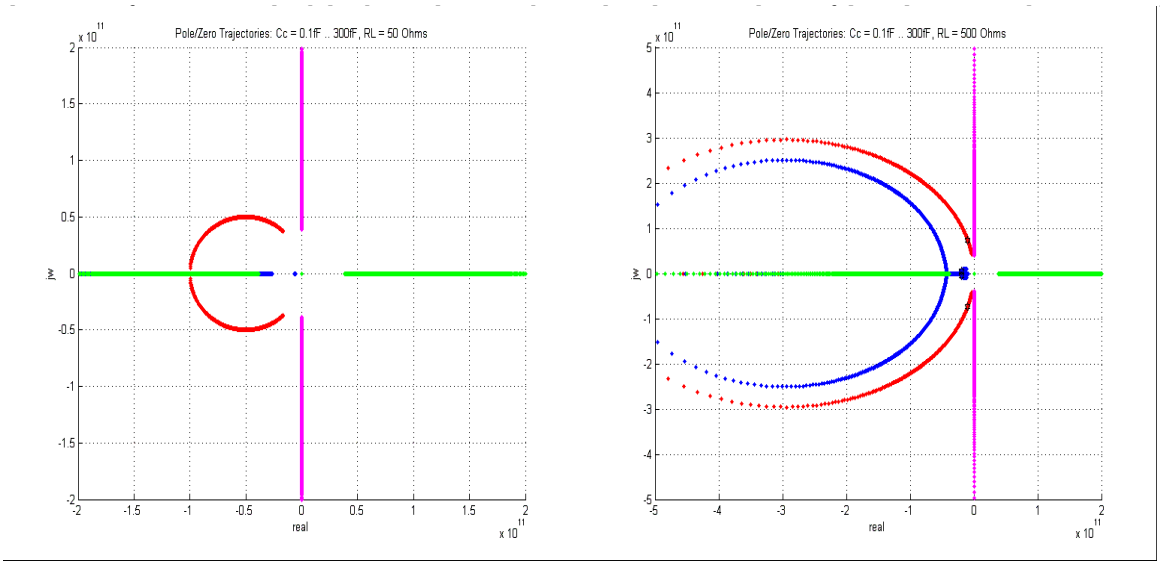


Figure 42 Trajectories of poles and zeros of coupled inductors with same phase and opposite phase windings as a function of coupling capacitance C_C

C_C is increasing as trajectories head toward origin of graph
(red) poles for inductors with same winding sense
(magenta) zeros for inductors with same winding sense
(blue) poles for inductors with opposite winding sense
(green) zeros for inductors with opposite winding sense
$R_S = 50\Omega$, $L_1 = 5nH$, $L_2 = 5nH$, $k = 0.8$, $C_C = 1fF \ldots 300fF$

The effect of the winding sense in Figure 42 is seen directly by comparing the trajectories of the zeros. The magenta curves (for in phase windings) always appear along the jω axis but the green curves (for out of phase windings) move along the real axis. In the case where $R_L = 50\Omega$, the poles of the system for oppositely wound coupled inductors remain on the real axis and do not approach the jω axis until very large values of C_C. It is expected then that this system will remain stable for large values of coupling capacitance and have a response like an overdamped system. However, in the other three scenarios (i.e. in phase winding for $R_L = 50\Omega$ or 500Ω and out of phase windings for $R_L = 500\Omega$) the poles depart from the real axis as they head toward the jω axis. In each of these scenarios, it is expected that a value for C_C will exist that will cause the system's transient response to experience oscillation. Moreover, for the case where $R_L = 500\Omega$, the poles of the coupled inductors wound in the same direction approach the jω axis more quickly than for coupled inductors with opposite winding sense. As such, it is expected that the system with an in phase winding sense will suffer from oscillation in the transient response for lower values of C_C than the system with opposite winding sense.

Several time domain responses are shown in Figure 43 to validate the qualitative predictions made from the pole / zero trajectories for C_C. The time domain responses are derived for a system in which $L_1 = L_2 = 5nH$, $R_W = 0$, $k = 0.8$ and $C_P = 0$. The time domain responses for inductors wound in phase are shown in the top half of each

graph and responses for coupled inductors with out of phase windings are shown in the bottom half. The left side of the figure shows the response for $R_L = 50\Omega$ and the right side of the figure shows the responses for $R_L = 500\Omega$. Within each figure, the value of C_C is varied from 0 to 500fF in 100fF increments.

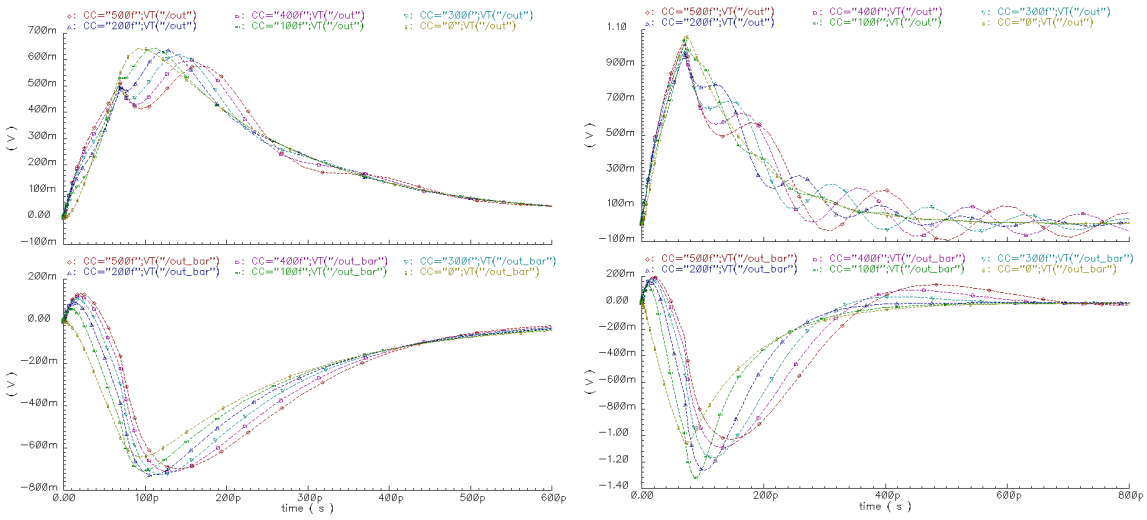


Figure 43 Time domain response of coupled inductors with coupling capacitance (C_C)
(left, top) $R_S = 50\Omega$, same winding sense, (left, bottom) $R_S = 50\Omega$, opposite winding sense
(right, top) $R_S = 500\Omega$, same winding sense, (right, bottom) $R_S = 500\Omega$, opposite winding sense
$L_1 = 5nH$, $L_2 = 5nH$, $k = 0.8$, $C_C = 0fF \ldots 500fF$

As predicted from the pole / zero plots, the system in which $R_L = 50\Omega$ and the coupled inductors are wound with an opposite sense is relatively insensitive to changes in C_C. However, the response of this system lingers in time. Also predicted by the pole / zero analysis, the transient response is highly sensitive to the winding sense. The response of the systems wound with the same winding sense exhibit oscillation in their transient responses, and the amplitude of the oscillations increase as C_C increases. The oscillations are distinct for this system with $R_L = 500\Omega$ with C_C as low as 100fF and become severe when C_C is increased to 200fF. The system with coupled inductors wound in an opposite sense and $R_L = 500\Omega$ has its poles off of the jω axis for small values of C_C – this system is less damped than the system with coupled inductors wound in an opposite sense but $R_L = 50\Omega$. As a result, the duration of the transient response decreases as C_C is increased. C_C can continue to be increased for this 500Ω system until the overshoot so severe that signal integrity is compromised. For example, this system can tolerate C_C as large as 400fF while keeping all oscillations after the initial response (e.g. overshoot and undershoot) below 10% of the peak voltage.

The behavior introduced by the parasitic shunting capacitances (C_P) can be analyzed with a similar methodology as that used to study the effect of C_C. A model slightly abridged from those shown in Figure 41 can be used since

the effect of C_P can be realized without other parasitics. The voltage transfer function for coupled inductors with parasitic shunting capacitance is listed in Equation 7. Although it is a higher order system than the voltage transfer functions related to C_C, this function only depends upon the inductor winding sense to establish the polarity of the output voltage (the numerator is taken as negative for coupled inductors with opposite winding sense and positive for in phase winding sense).

$$\frac{V_{LOAD}}{V_S} = \frac{\mp M R_L s}{\Phi R_S R_L C_{P1} C_{P2} s^4 + \Phi\left(C_{P1} R_S + C_{P2} R_L\right) s^3 + \left[\Phi + R_S R_L \left(C_{P1} L_1 + C_{P2} L_2\right)\right] s^2 + \left(R_S L_2 + R_L L_1\right) s + R_S R_L}$$

$$\Phi = \left(L_1 L_2 - M^2\right)$$

Equation 7 Voltage transfer function of coupled inductors due to parasitic shunt capacitance (C_P)
Minus sign in numerator to be used when inductors are wound with the opposite sense.

Figure 44 shows the trajectories of the poles and zeros of Equation 7 as a function of C_P and is derived for a system in which $L_1 = L_2 = 5nH$, $R_W = 0$, $k = 0.8$ and $C_C = 0$. In the figure, the left side shows pole / zero trajectories for $R_L = 50\Omega$ and the right side shows trajectories for $R_L = 500\Omega$. Within each graph, C_P is varied from 1fF to 1000fF. The trajectories of the poles of coupled inductors with in phase windings are shown in red and the corresponding zeros are shown in magenta. The trajectories of the poles of coupled inductors with out of phase windings are shown in blue and the corresponding zeros are shown in green. However, the zeros are difficult to see on the graph because one zero for each system is located at the origin and is independent of the value of C_P while the remaining zeros are located at $j\omega = \infty$.

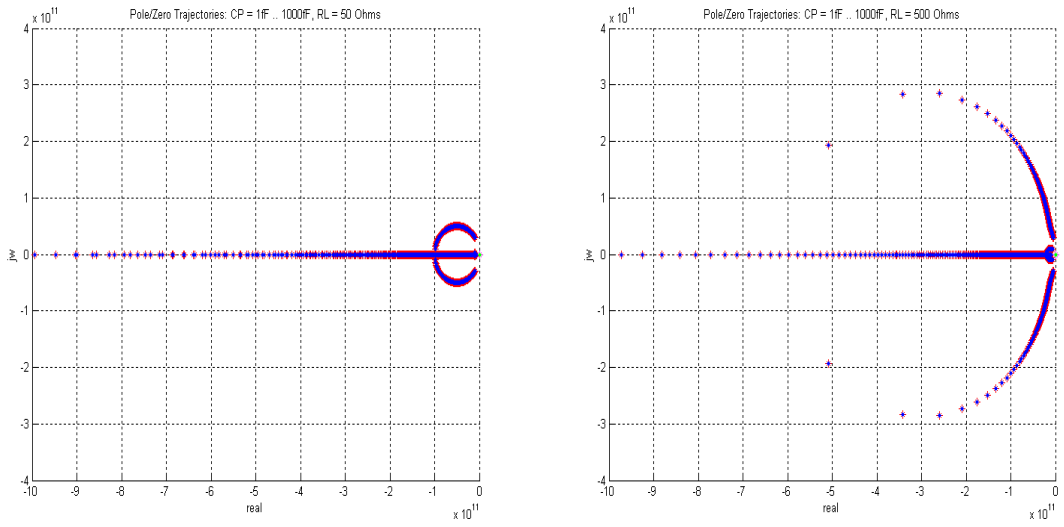


Figure 44 Trajectories of poles and zeros of coupled inductors with same phase and opposite phase windings as a function of parasitic shunting capacitance C_P
C_P is increasing as trajectories head toward origin of graph
(red) poles for inductors with same winding sense
(blue) poles for inductors with opposite winding sense
$R_S = 50\Omega$, $L_1 = 5nH$, $L_2 = 5nH$, $k = 0.8$, $C_P = 1fF \ldots 1000fF$

As can be seen clearly from both graphs, the pole trajectories are identical regardless of the winding sense of the inductors. However, since the polarity of the output voltage depends upon the winding sense, the time domain performance is expected to be symmetrical about the time axis. The systems for which $R_L = 50\Omega$ have their poles on the real axis for values of C_P up to 100fF at which point two poles become complex and the other two remain real. The systems for which $R_L = 500\Omega$ have their poles on the real axis for $C_P = 1fF$ but two of the poles become complex at $C_P = 2fF$. Comparing these two systems, the poles for the 500Ω system become complex for much lower values of C_P than for the 50Ω system. In addition, the complex poles for the 50Ω systems stay relatively close to the real axis compared to the 500Ω systems. Given these two observations, oscillations in the transient response of the 500Ω systems are expected for small values of C_P but the 50Ω systems are expected to be relatively insensitive to variations in C_P.

Figure 45 shows these trends in the transient response for a system in which $L_1 = L_2 = 5nH$, $k = 0.8$, $R_W = 0$ and $C_C = 0$. The top two graphs are for coupled inductors with the same winding sense and the lower two graphs are for coupled inductors with opposite winding sense. The graphs on the left of the figure show the response for $R_L = 50\Omega$ and the graphs on the right side of the figure show the response for $R_L = 500\Omega$. Within the graphs for $R_L = 50\Omega$, C_P is varied from 1fF to 1000fF, but for $R_L = 500\Omega$ the response is more sensitive to capacitance so C_P is only varied from 1fF to 250fF.

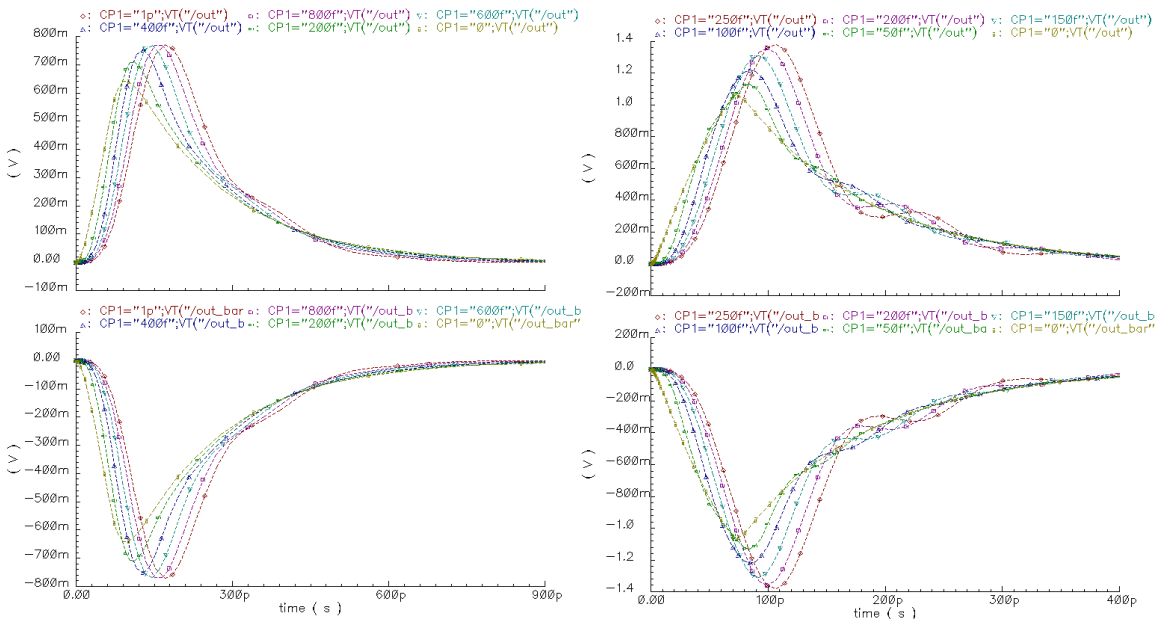


Figure 45 Time domain response of coupled inductors with shunting parasitic capacitance (C_P)

Increasing shunting capacitance tends to increase the amount of signal that passes through the coupled inductors at the expense of a longer time domain response. However, as the shunting capacitance continues to increase, eventually oscillations appear in the response. As expected, the systems for which R_L = 50Ω can tolerate very large parasitic capacitances without significant oscillation appearing in the transient response, but the 500Ω system is far more sensitive to variations in C_P. On the positive side, the response of the 500Ω systems couple more voltage across the transformer and the responses take less time to settle to 10% of the peak voltage as shown in Figure 46. The 50Ω system with C_P = 100fF has a peak voltage of 680mV and requires 518ps to settle to 68mV, but the 500Ω system with C_P = 100fF has a peak voltage of 1220mV yet requires only 301ps to settle to 121mV. In percentages, the peak voltage for the 500Ω system is 65% greater and the settle time 42% less than for the 50Ω system. Moreover, the peak observed in the frequency response of the system with R_L = 500Ω can be tuned by proper coupling element design so that low pass filtering introduced by the interconnect can be equalized.

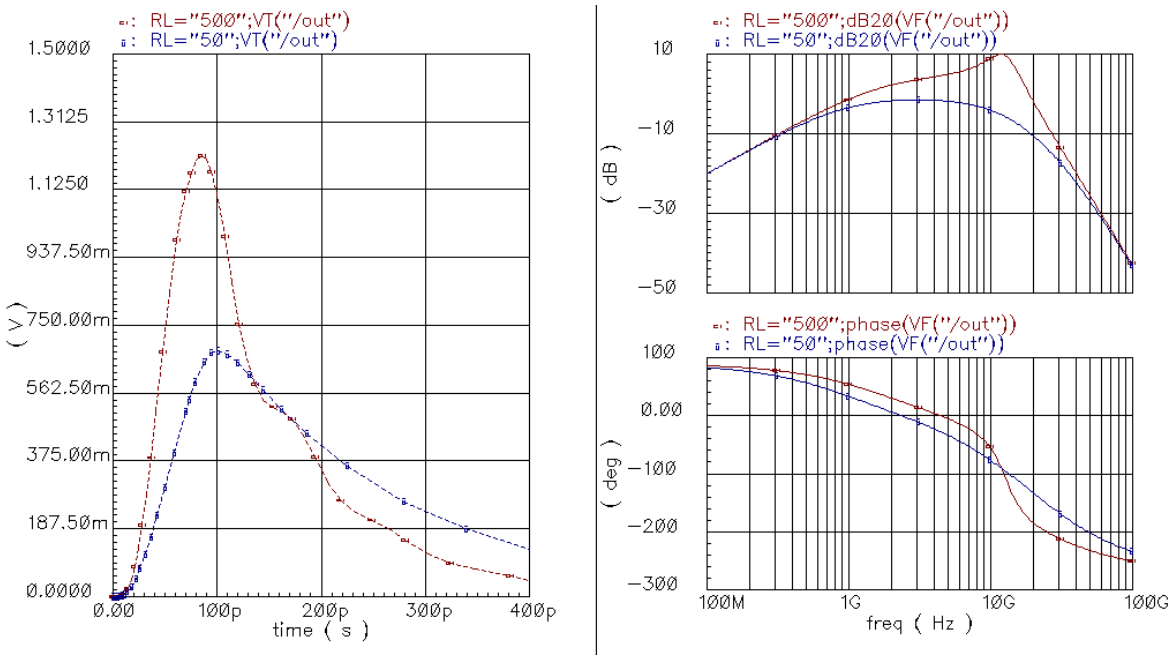


Figure 46 Time- and frequency domain plots demonstrating the impact of R_L upon coupled inductor response for a fixed value of C_p = 100fF
$L_1 = L_2 = 5nH$, $k = 0.8$, $R_W = 0$, $C_C = 0$

Parasitic capacitance cannot be avoided in a coupled inductor system. The effect of C_C is dependent upon the winding sense of the inductors – inductors wound in an opposite sense tend to have more stable performance than inductors wound in the same sense. The response due to C_P depends upon the winding sense only to establish the polarity of the output voltage. The performance of coupled inductors becomes more sensitive to both C_P and C_C as the load resistance is increased, and this sensitivity manifests itself as oscillations of increasing amplitude in the transient response as C_P and C_C are increased. A system with no capacitance is overdamped but both C_C and C_P can be increased to achieve optimal damping. In addition, through careful coupling element design, the frequency response can be tuned to realize some measure of channel equalization.

3.3.4 Discussion

The model of Figure 19 captures in a simple form many of the inherently complex behaviors of coupled inductors, but it should be used with knowledge of its assumptions, limitations and available alternatives. For example, the model contains a shunt resistor R_P at each port whose impact upon performance has not yet been examined in detail. As previously mentioned, this element appears in the coupled inductor model as a simplification of the physically relevant quantities R_{SI} and C_{OX}, but the model is fairly over a wide range of R_P values. Small values of R_P (i.e. large resistive substrate losses) attenuate the frequency response in the passband, but large values have little effect on the frequency performance. Figure 50 illustrates this behavior by showing

the frequency response of a transformer for R_P ranging from 100Ω to 1MΩ. In this figure, $L_1 = L_2 = 2.5$nH, k = 0.8, $R_{W1} = R_{W2} = 10\Omega$ and $C_{P1} = C_{P2} = C_C = 3$fF. The passband of this transformer is centered at 12.5GHz and extends from 2GHz to 105GHz. The response in the passband is attenuated for $R_P = 100\Omega$ but almost unchanged for values of R_P between 1kΩ and 1MΩ. R_P has little effect on the frequency response outside of the passband.

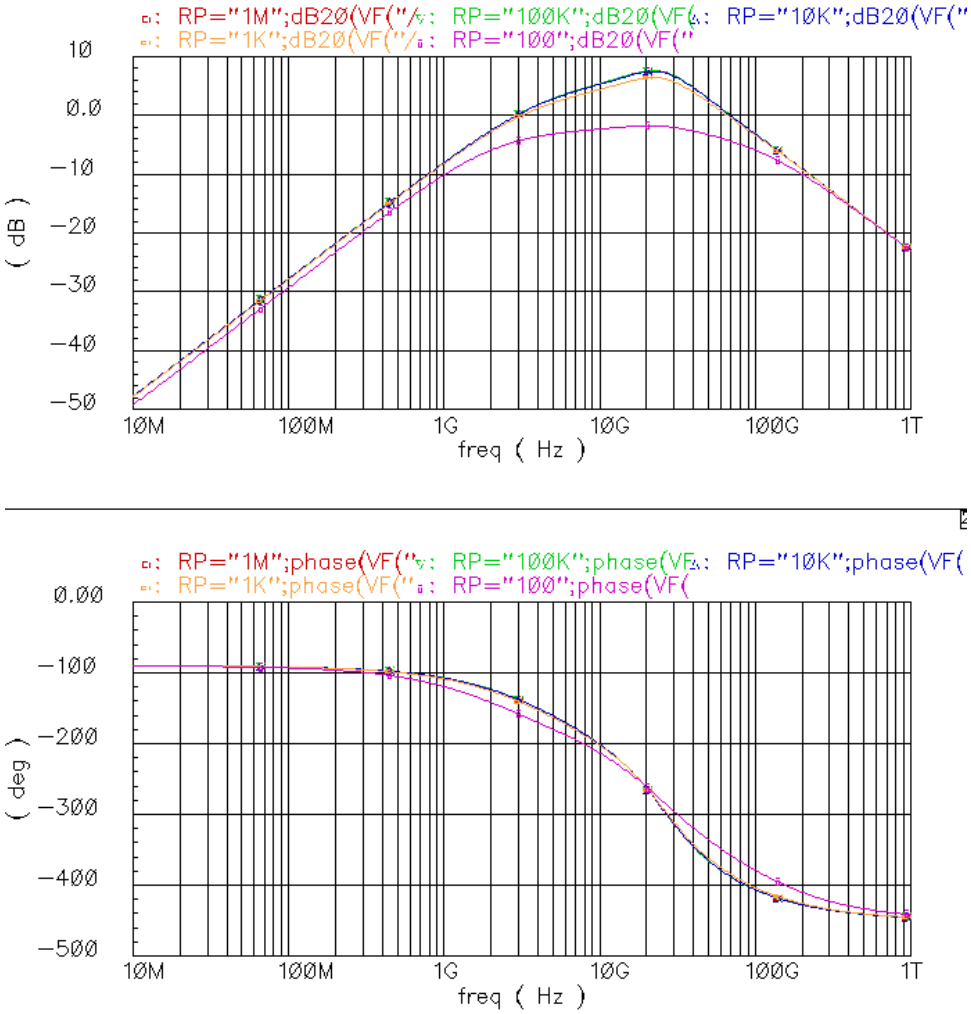


Figure 47 Impact upon frequency response due to variations in resistive substrate loss (R_P)

Comparing the performance of a complete coupled inductor model to measured data shows that it can accurately model coupled inductor performance from DC up to about 10GHz. Beyond 10GHz, the resistance of the inductors begins to change as a result of the skin effect. Rather than using R_P as a fitting parameter, the effect of skin resistance can be modeled by a network of parallel R-L elements in place of the single resistor R_W as shown

in Figure 48. The specific values of each component in the skin effect model can be chosen so that the overall frequency response of the model fits the measured data.

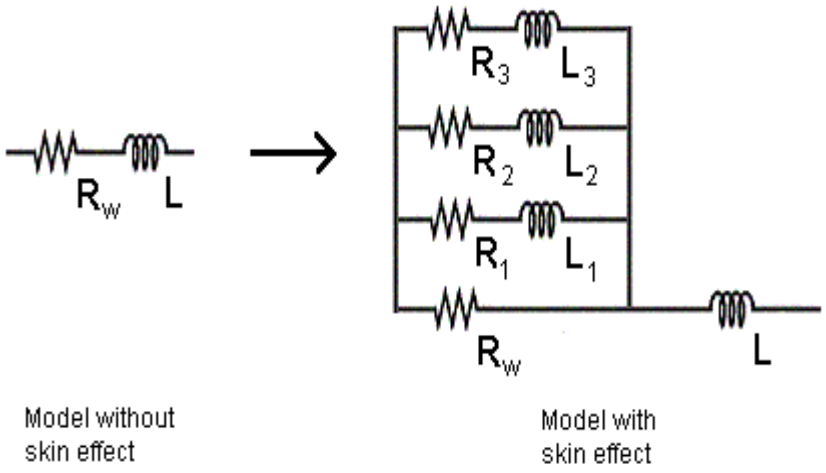


Figure 48 Ladder network replacement of R_W from coupled inductor model to capture skin effect resistance

In terms of time-domain performance, the complete model is not needed to achieve reasonable results. To illustrate this point, Figure 49 shows the relative impact on the time domain performance of increasingly realistic coupled inductor models. The values for the models are extracted from measurements of an 88μm diameter transformer fabricated in the TSMC 0.35μm process (i.e. L_1 = 2.2nH, L_2 = 2.5nH, k = 0.77, R_{W1} = 13.5Ω, R_{W2} = 30Ω, C_{P1} = 15fF, C_{P2} = 30fF, C_C = 21fF, R_{P1} = 1686Ω, R_{P2} = 610Ω, L_{LEAK} = 200pH). Each curve in the figure is labeled with the number of the corresponding schematic. The optimal performance is of course achieved with the curve labeled '1' when the inductors are perfectly coupled and have no associated parasitics. The two curves '2' and '3' have similar performance although the presence of the oscillation in the response of curve '3' makes it apparent that model contains parasitic capacitance. The remaining curves (i.e. '4' – '6') all have similar performance and show that the transient performance of coupled inductors can be modeled well with only the transformer primary and secondary, a coupling coefficient, winding resistance and parasitic capacitance. The R_P resistors modeling resistive substrate loss and leakage inductors do not substantially change the model behavior.

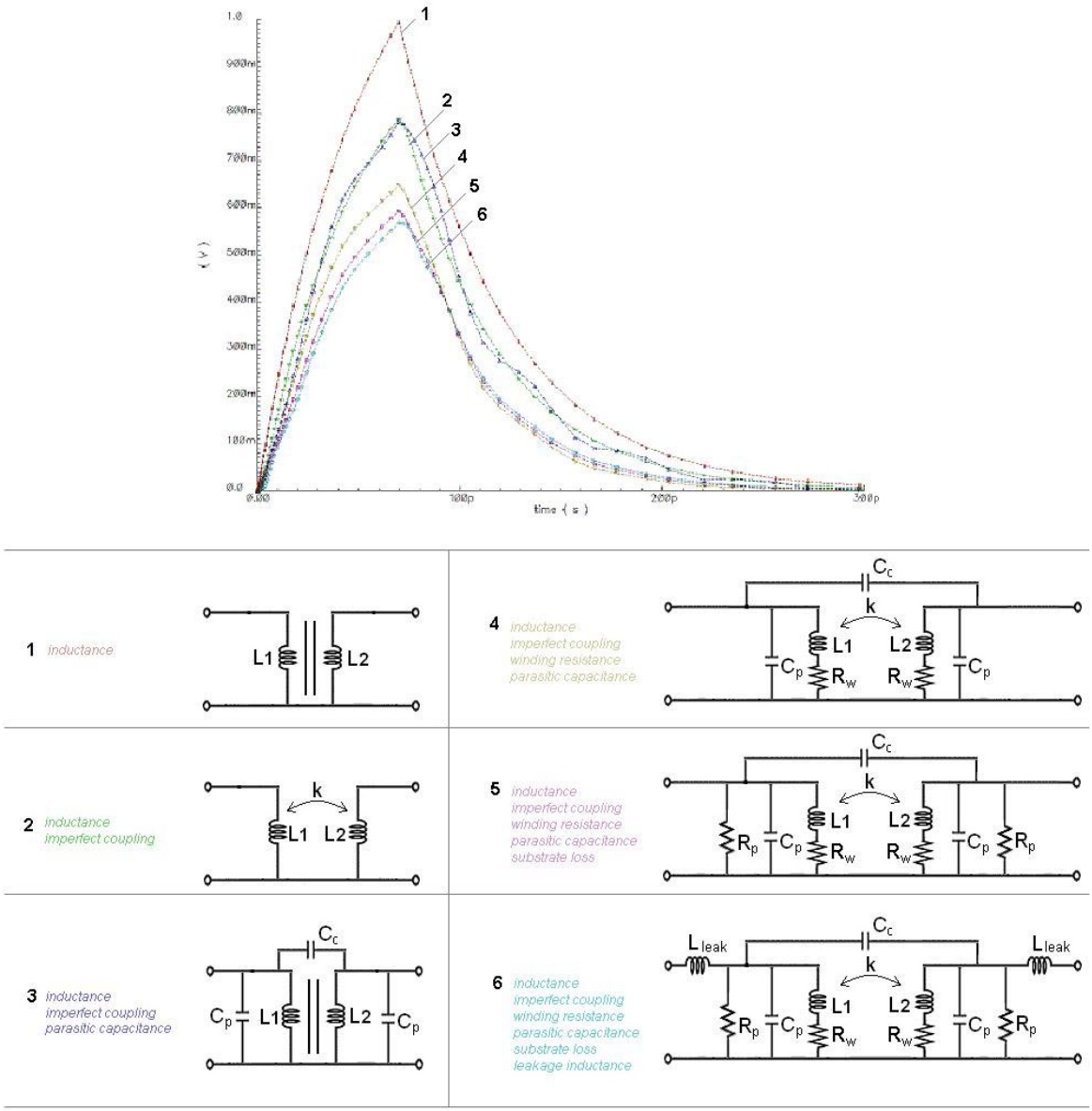


Figure 49 Comparison of LCI models with increasing levels of detail.
Input to all circuits is a 2V step input (1V available to a 50Ω load) with 70ps risetime

Control of the many geometric parameters and the frequency- and time-domain responses can be translated into three key performance metrics for each I/O of an LCI system: power, density and bandwidth. The relationships between these areas have been discussed in the analysis of the coupled inductor model, but the following discussion summarizes the important points for lumped and distributed systems.

3.3.4.1 Lumped LCI System

I/O bandwidth is determined by the value of the coupling inductors, parasitics and the loss characteristics of any interconnections. I/O density goals constrain the nearest-neighbor separation and the physical size of the inductors (thereby constraining the number of windings and range of possible inductances). In addition to transceiver design, I/O power is determined by the value of the coupling coefficient, parasitics, system impedance and loss in the interconnection. There are many tradeoffs between each of these performance metrics.

Unlike a lumped CCI system, an LCI system cannot be totally converted from a bandpass to a high or low pass characteristic by increasing the load impedance. Thus the load impedance should be chosen to optimize (and simplify if possible) the receiver design. To minimize system loss, a large coupling coefficient is desirable. Achieving a specific coupling coefficient is a tradeoff between inductor size and proximity. That is, improvements in inductor coupling are realized either by decreasing the gap between inductors through packaging innovations or by increasing the diameter of the inductors and thereby decreasing the achievable density.

Given a coupled inductor design and a specification for ISI, there exists a maximum *pulse frequency* that can be used to transmit information. However, it is possible to exceed these data rates by using signal equalization techniques to transmit a non-square wave pulse through the channel. Whether equalization techniques are employed, maximizing performance of a lumped LCI system with respect to I/O density, power and bandwidth, requires that a balance be achieved between the values and sizes of the inductances composing the transformer, mutual coupling, parasitics (both winding resistance and capacitance), desired data rate, and duration of the channel step response (e.g. the allowable ISI).

3.3.4.2 Distributed LCI System Performance

As with lumped LCI systems, the data rate that can be supported by a distributed LCI system will depend upon how long the step response of the channel lingers in time. For a distributed LCI system not only must the band-limiting effects and losses imposed by the coupled inductor parasitics be managed, but also the design must compensate for the potential performance decrease due to the transmission line and second set of coupled inductors.

The presence of the transmission line in the distributed LCI system requires that impedance matching be considered. Placing a shunt resistor to terminate the transmission line on the receiver side is one possible method of providing impedance matching. The terminating resistor in this arrangement is seen in parallel with R_P at the input to the second coupling stage and can be modeled as $R_P' = R_P \,//\, R_{TERMINATION}$. $R_{TERMINATION}$ will generally be close to the transmission line impedance so it will have the effect of reducing the value of R_P on the

transformer input. Figure 47 illustrates the impact that the terminating resistor has on the magnitude and phase of the transformer input impedance for terminating resistors ranging from 10Ω to 100Ω — the impact on systems with both opposite and in-phase winding senses is shown. The curves in the figure are derived for a system where $L_1 = L_2 = 2.5$nH, $k = 0.8$, $R_{W1} = R_{W2} = 10\Omega$ and $C_{P1} = C_{P2} = C_C = 30$fF. Also plotted in the figures is the magnitude and phase of the impedances of R_W, C_P and L as a function of frequency. Regardless of the winding sense, as the terminating resistor value is decreased the transformer impedance varies less over frequency, but since the termination resistor is in parallel with and reduces R_P this result is expected. That is, small values of R_P′ have the same effect as large substrate losses that tend to lower inductor Q. As inductor Q is lowered, less pronounced peaking of the frequency and impedance responses occurs. Another point to note is that large values of R_P′ have little effect on the impedance of coupled inductors with opposite winding sense but allow the impedance of inductors with the same winding sense to exhibit strong peaking. Finally, the low frequency impedance of the transformer approaches R_W // $R_{TERMINATION}$ and the high frequency impedance approaches the impedance of the coupling capacitance.

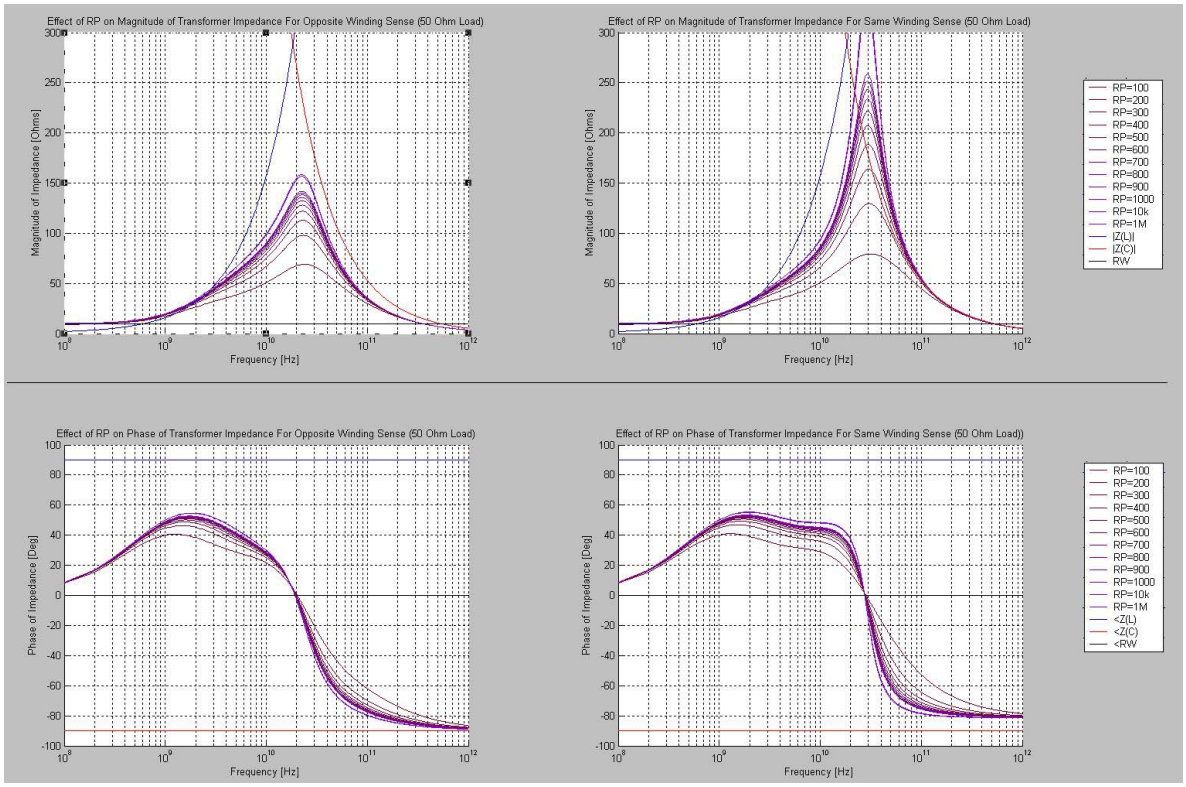


Figure 50 Transformer impedance (magnitude and phase) seen by load due to variations in resistive substrate loss (R_P)

The performance of an LCI system can be estimated by plotting the eye diagram resulting from the transmission of a random bit sequence. As an example of the performance that can be expected, Figure 51 shows a schematic of a distributed LCI system and Figure 52 shows the voltage waveforms at 4 points in the system (i.e. at the nodes labeled SOURCE, V_{IN}, V_{OUT1} and V_{OUT2}). Eye diagrams at V_{OUT1} and V_{OUT2} resulting from the transmission of the 5Gbps, 26-bit NRZ pattern 10_1100_1001_1101_0110_0100_1110 are also shown in the figure. Both coupling stages in the system use oppositely wound inductors and a 50Ω lossless transmission line is used. The component values for the system are: $L_1 = L_2 = 2nH$, $L_3 = L_4 = 5nH$, $M_{12} = 0.8 \times 2nH$, $M_{34} = 0.8 \times 5nH$, $R_1 = R_2 = R_3 = R_4 = 10\Omega$, $C_1 = C_2 = C_{12} = C_{34} = 25fF$, $C_3 = C_4 = 75fF$, $R_{P1} = R_{P2} = R_{P4} = R_L = 500\Omega$, $R_S = Z_O = R_{P3} = 50\Omega$,

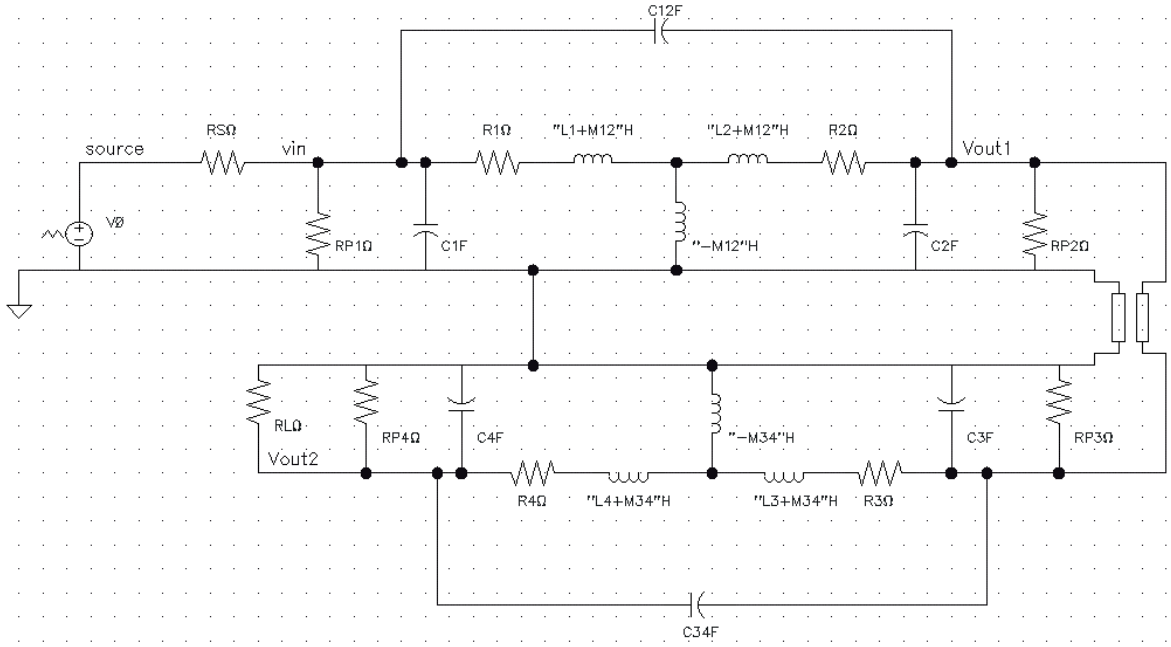


Figure 51 Schematic of distributed LCI system with complete coupled inductor models

The eye diagram opening changes as the values of the coupled inductor components change. But since the opening of the eye diagram (and hence ISI) depends upon how long the response to a step input lingers in time, the *pulse signaling* data rate that can be supported by an LCI system can be estimated from the unit step response. As the inductance increases, the response to a step lasts longer in time and ISI for a fixed frequency input increases. The parasitic capacitances associated with the coupled inductors can help tune the damping factor of the system and thereby reduce the settling time of the transient response, but too much capacitance results in oscillations in the response and hence larger ISI. Both increased R_L and R_W help to truncate the

duration of the time response leading to higher possible signaling rates. Decreasing R_P (or R_P') increases loss through the transformer and increasing R_L makes the response more sensitive to capacitance.

The eye diagram in Figure 52 is the result of using only the passive nature of the coupled inductors to create a channel that can communicate data at a 5 Gbps rate. However, the response due to pulse signaling can be improved beyond the maximum achievable with finite rise time, voltage steps, by using circuit techniques (e.g. active filters) to transmit a compensated or equalized waveform.

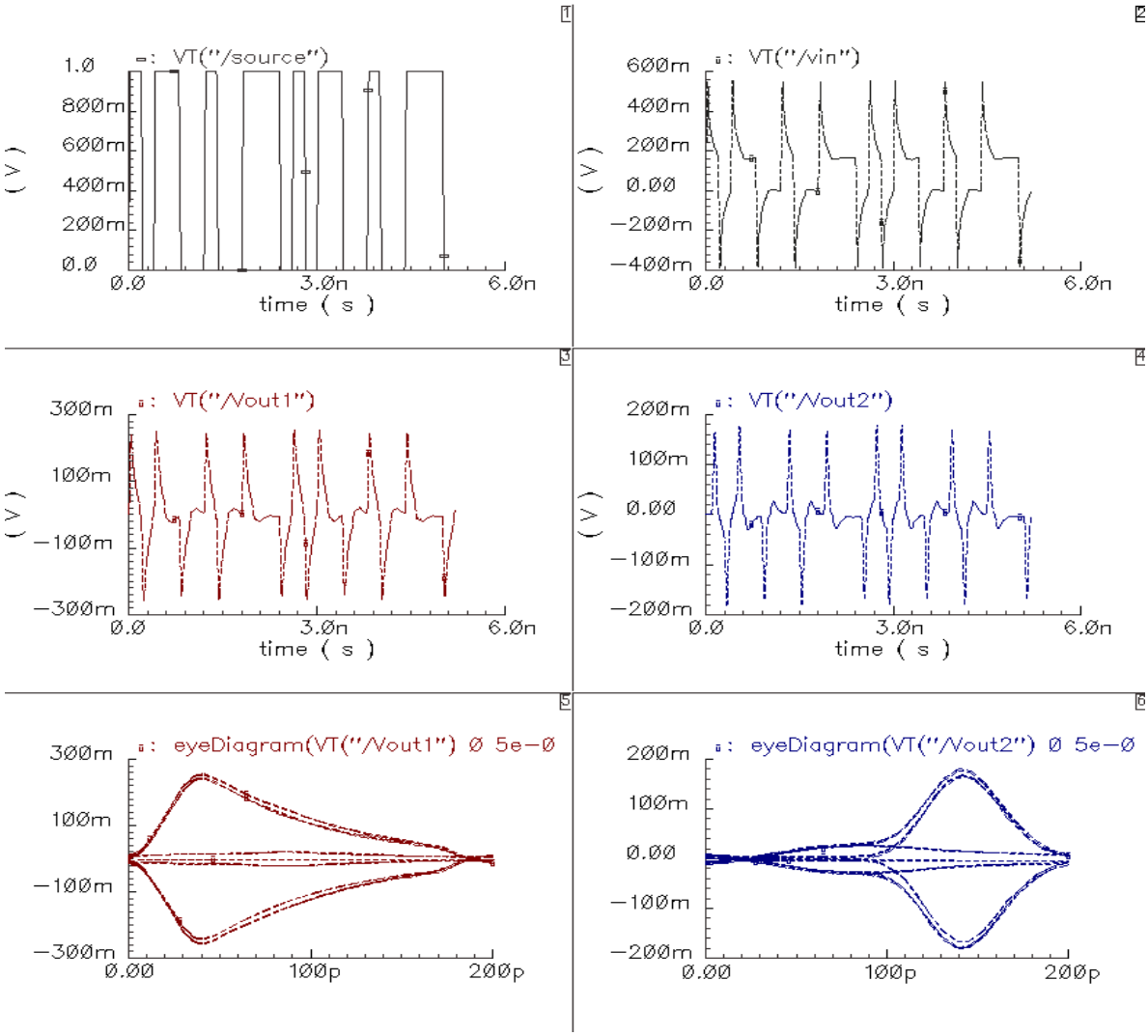


Figure 52 Voltage waveforms and eye diagrams of distributed LCI system transmitting 5Gbps NRZ data
Component values refer to Figure 51
$L1 = L2 = 2nH$, $L_3 = L_P = 5nH$, $M_{PP} = 0.8 \times 2nH$, $M_{3P} = 0.8 \times 5nH$, $R_P = R_P = R_3 = R_P = 10\Omega$, $C_P = C_P = C_{PP} = C_{3P}$ $=25fF$, $C_3 = C_P = 75fF$, $R_{PP} = R_{PP} = R_{PP} = R_P = 500\Omega$, $R_P = Z_P = R_{P3} = 50\ \Omega$,

To maximize the bandwidth, density and power performance of a distributed LCI system, a balance must be achieved between numerous design variables including the value of the inductances and other parameters composing the transformer, the desired data rate, the duration of the step response; and the length, impedance and loss of the interconnection.

3.3.4.3 Coupled Inductor Density

As discussed previously, much ongoing research is targeted at developing dense arrays of high-speed I/Os for packaged ICs. Applied to a communications system, each pair of coupled inductors creates an individual I/O. Therefore, densely packed coupled inductors could provide a method to achieve a high density of package I/O with each I/O capable of sustaining multi-Gbps data rates. However, it must be discovered how closely coupled inductors can be placed relative to each other and still function as I/Os with acceptable electrical performance. At present, a simulation model does not exist to predict the signal to noise tradeoffs associated with the placement of coupled inductors in a dense array. However, measured data presented in *Chapter 4* combined with 3D electromagnetic simulations should allow for the development of such a predictive model.

3.4 LCI versus CCI

Since the model for coupled inductors has a Pi-network of parasitic capacitors that is similar to the actual channel model of a CCI system, it is instructive to consider whether LCI offers any advantages over CCI. To make a comparison between these two types of AC Coupled systems, the potential bandwidth, attenuation and element size should be compared.

To compare potential bandwidth (i.e. by looking at relative settling times) and attenuation, Figure 53 shows time-domain responses at the output of a single coupling stage for each of these two systems under varying load resistance. Parameters for coupled inductors are taken directly from a model that fits measured data of a transformer fabricated in the TSMC 0.35μm process. The model parameters for this transformer are L_1 = 2.2nH, L_2 = 2.5nH, k = 0.77, R_{W1} = 13.5Ω, R_{W2} = 30Ω, C_{P1} = 15fF, C_{P2} = 30fF, C_C = 21fF, R_{P1} = 1686Ω and R_{P2} = 610Ω. The parameters for the CCI channel are chosen as $C_C = C_{P1} = C_{P2}$ = 150fF assuming an air gap between capacitor plate. This choice of C_C/C_P implies from Figure 13 that the capacitor plates must be at least 4× further from their respective substrates than from each other.

In the case where R_L = 50Ω, the LCI system transmits a peak voltage approximately 50% greater with a settling time (e.g. time to reach 10% of the peak voltage) almost twice the duration of the CCI coupling stage. As R_L is increased to 100Ω, the LCI stage still transmits more signal than the LCI stage but the difference in settling time is less drastic. When R_L is increased to 250Ω, the two systems have fairly equivalent performance although the

LCI system settling time is about 25% less than the CCI system. For larger values of R_L, the relative performance is reversed: the CCI system transmits greater peak voltage but requires more settling time.

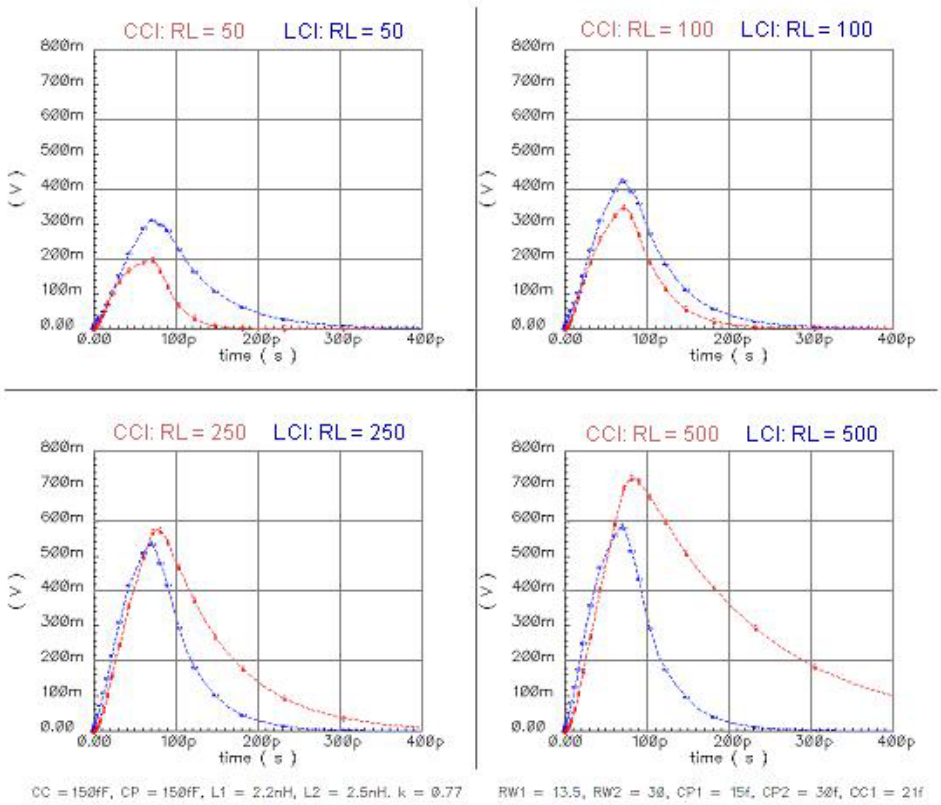


Figure 53 Time-domain performance of LCI versus CCI with air dielectric between plates

With the use of underfill materials in a CCI systems, it may be possible to increase the dielectric constant between opposing capacitor plates and improve the ratio of C_C/C_P beyond '1'. If the system can be constructed such that C_C = 150fF but $C_{P1} = C_{P2}$ = 50fF then CCI performance will improve. With respect to Figure 13, this choice of C_C/C_P implies two constraints upon the CCI system. First, the underfill between plates must have a dielectric constant at least equal to that of the inter-level dielectric used on each IC. Secondly, the capacitor plates must be at least the same distance from their respective substrates as from each other.

Figure 54 shows time-domain responses at the output of a single coupling stage for each of these two systems under varying load resistance with the improved ratio of C_C/C_P for the CCI stage. When R_L = 50Ω, the LCI system transmits a peak voltage approximately 50% greater with a settling time almost twice the duration of the CCI coupling stage. When R_L is increased to 100Ω, the two systems have fairly equivalent performance although

the LCI system settling time is about 25% greater than the CCI system. For larger values of R_L, the relative performance is reversed: the CCI system transmits greater peak voltage but requires more settling time.

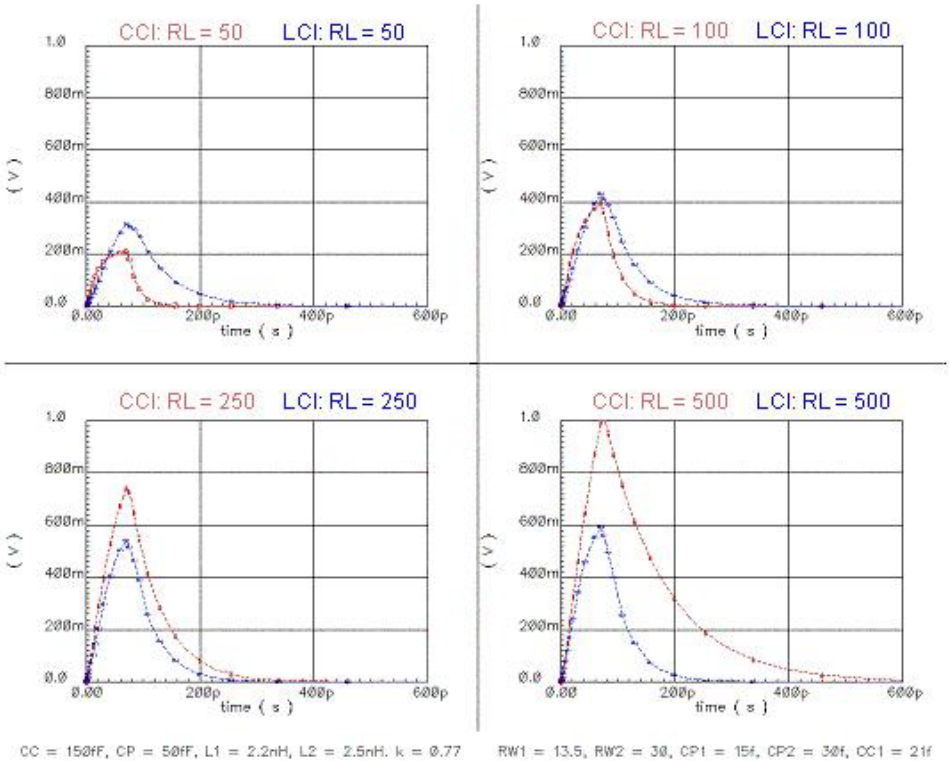


Figure 54 Time-domain performance of LCI versus CCI with non-air dielectric ($\varepsilon_r \approx 4$) between plates

In terms of element size, the transformer for the LCI coupling stage presented in all of the preceding simulations is 90µm in outer diameter. In the first CCI scenario (i.e. $C_C = C_P = 150$fF and the gap between capacitor plates is air) assuming the gap is 2µm, a 150fF coupling capacitor is approximately 184µm per side. In the second scenario (i.e. $C_C = 150$fF, $C_P = 50$fF and the gap between capacitor plates has $\varepsilon_r \approx 4$) assuming the gap is 2µm, a 150fF coupling capacitor is approximately 92µm per side.

Whether LCI or CCI is employed in a given system will depend upon the relative importance of the system specifications. If low attenuation is more important than high data rates, the termination resistance is small, and the packaging technology does not support large ratios of C_C/C_P, then LCI coupling stages are more appropriate than CCI. However, if very large ratios of C_C/C_P are possible and R_L is large, then CCI might be more appropriate than LCI. However, the decision of choosing between LCI and CCI is made more complicated by the relative importance of I/O density as a system specification. LCI can achieve higher I/O densities than CCI under

many situations. For example, if underfills with high relative dielectric constants are not available then the capacitor plates must be very large in order to achieve suitable values of capacitance and CCI I/O density will be lower than LCI I/O density. However, if advanced underfill materials are available, then the capacitor dimensions can be reduced and CCI I/O density could exceed LCI I/O density.

Chapter 4 CCI and LCI Measurements

4.1 Overview

Experiments have been designed, fabricated and measured on portions of both capacitive and inductive coupling channels to begin to verify the analyses of the previous chapter. Descriptions of the experiments and measured results are presented in this chapter.

4.2 Capacitive Coupling

The design and measurement results of experiments to prove the basic feasibility of capacitive coupling are presented.

4.2.1 Experimental Design

Experiments have been designed for time-domain measurements in the TSMC 0.35 μm process to prove the feasibility of capacitive coupling as an interconnection technology. A photograph of the fabricated chip is shown in Figure 55. The structures for the capacitive coupling experiments consist of four instances of a 3-stage inverting driver and four receivers. Instances of the transmitter and receiver designs are alternated along the left side of the die with large ground connections between each active structure. For these circuits, the coupling capacitors are fabricated entirely on-chip at the output of each driver and at the input of each receiver. However, the connection between transmitter and receiver coupling capacitors is achieved through an off-chip bondwire. Thus, in the actual measurements, square waves are passed through the sequence of: transmitter, capacitive coupling stage, off-chip bondwire, capacitive coupling stage and receiver.

Figure 55 shows three structures circled on the die and presents an equivalent schematic of these experiments. The transmitter that is circled is a 3-stage inverter chain with a 75mm x 75mm on-chip, series capacitor connected to its output. A second transmitter is also on the die consisting of the same 3-stage inverter chain but with a 150mm x 75mm on-chip capacitor connected to its output. The capacitance of these on-chip capacitors is calculated to be 0.80pF and 1.19pF, respectively. Two different receiver configurations are on-chip. The structure circled and presented in the schematic implements a modified capacitive coupling receiver first proposed by Kühn but only demonstrated at 25MHz in [14]. This receiver has a series, 75mm x 75mm on-chip capacitor connected to its input. The second receiver structure on the die implements the same receiver circuit but is connected to a series 150mm x 75mm on-chip capacitor. A schematic of this receiver is shown in Figure 56.

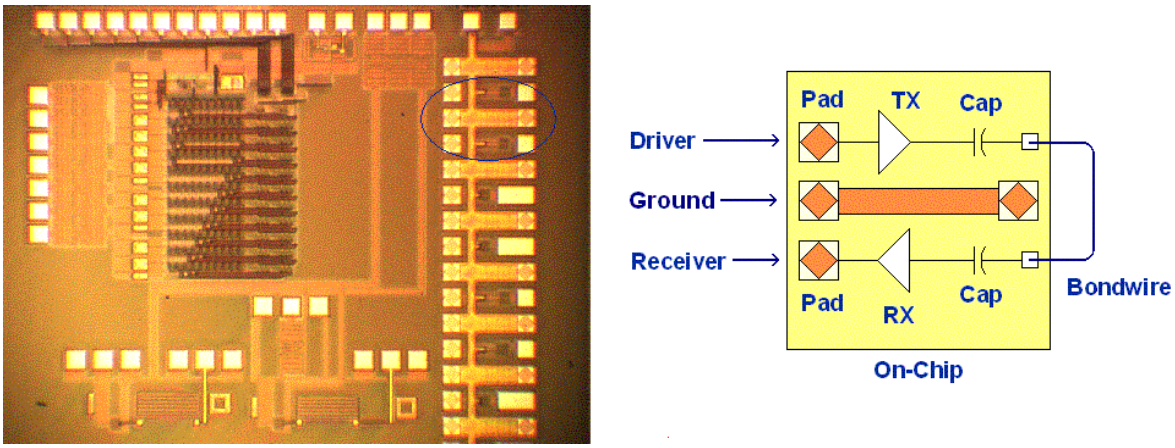


Figure 55 Die photo of capacitively-coupled driver and receiver experiments in the TSMC 0.35µm process
(left) die photo with three experiments highlighted: from top to bottom 1) transmitter, 2) large VDD/GND decoupling capacitor and 3) receiver.
(right) Schematic representation of measurement setup. Transmitter and receiver existed on a single integrated circuit but were connected through an off-chip bondwire.

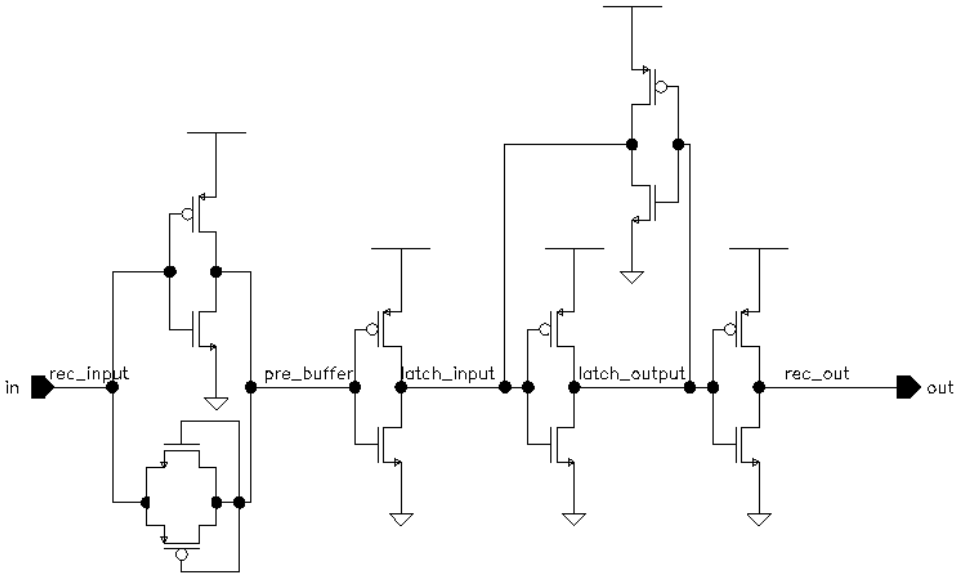


Figure 56 Schematic of receiver for capacitive coupling experiments

At the input of the receiver is an inverter that is self-biased to the peak gain region of its transfer characteristic. The feedback transistors are diode connected and these devices have dynamic input impedance. When the voltage across them is below their threshold voltage they have extremely high input impedance. This allows the

input impedance of the receiver to remain high for small input signals and as discussed in the previous chapter allows the performance advantages of a CCI system resulting from large values of R_L to be realized. The diode-connected devices also limit the maximum swing between the receiver input and the output of its first stage. As the output signal of the first stage transitions out of phase with its input signal the diodes eventually turn on and limit the voltage difference. This is important for detecting small pulses with fast edges in a system using minimum sized coupling capacitors. The next stage easily amplifies this signal to on chip digital levels. Following this buffer is a latch that stores the last transition of the input, making the receiver compliant

4.2.2 Measured Results

The die photographed in Figure 55 are 2mm x 2mm. Five chips have been mounted into a single 64-pin DIP package, and each chip is wirebonded to have its own package pins for power and ground supply voltages.

Characterization has been performed on several driver/coupling capacitor pairs for 3.3V peak to peak square wave inputs from 40MHz to 3GHz. It has been found that the delay through the 3-stage inverting driver and 75μm × 75μm series capacitor is 190ps at both 2.0GHz and 1.5GHz. The DC current drawn by the driver is 8mA at 2.4GHz, 5mA at 1.2GHz, 2mA at 600MHz, and less than 1mA at and below 75MHz. The edge rates at the output of the driver's series capacitor measured from –1.3V to +1.3V are found to be 132ps at 2.4GHz and 110ps at 1.2GHz. As confirmed with simulation, these edge rates at 2.4GHz will allow the on-chip capacitors to be reduced to 0.200pF (a 4× decrease in area) while maintaining sufficient current injection into the receivers for correct operation.

Figure 57 shows the measured results at the driver input, output of the driver series coupling capacitor and the output of the signal recovered by the receiver for a 3.3V, 2GHz square wave input. The measured waveforms are almost square-waves in shape although some limited bandwidth effects seem to be evident. For this configuration the total delay through the system (transmitter / coupling capacitors / bondwire / receiver) is measured to be 212ps. The small voltage scale in the figure is a result of a 101:1 voltage divider seen between the microprobe with a series 5000 Ω resistor used on the output and the 50Ω test equipment input. This voltage division is used to avoid damaging the test equipment. The input to the driver exhibits sharp ringing on both high-low and low-high transitions. This ringing occurs because of impedance mismatch between the test equipment and the driver. That is, the test equipment is configured for a 50Ω environment but effectively sees the high impedance of the transmitter input as an open circuit. Microprobes with a 50Ω termination at the probe tips can be used to present "clean" waveforms to the transmitter input. In spite of this mismatch, the receiver correctly recovers the input waveform. With an NRZ data-coding scheme, the transmitter/receiver system is capable of operating at 4Gbit/sec.

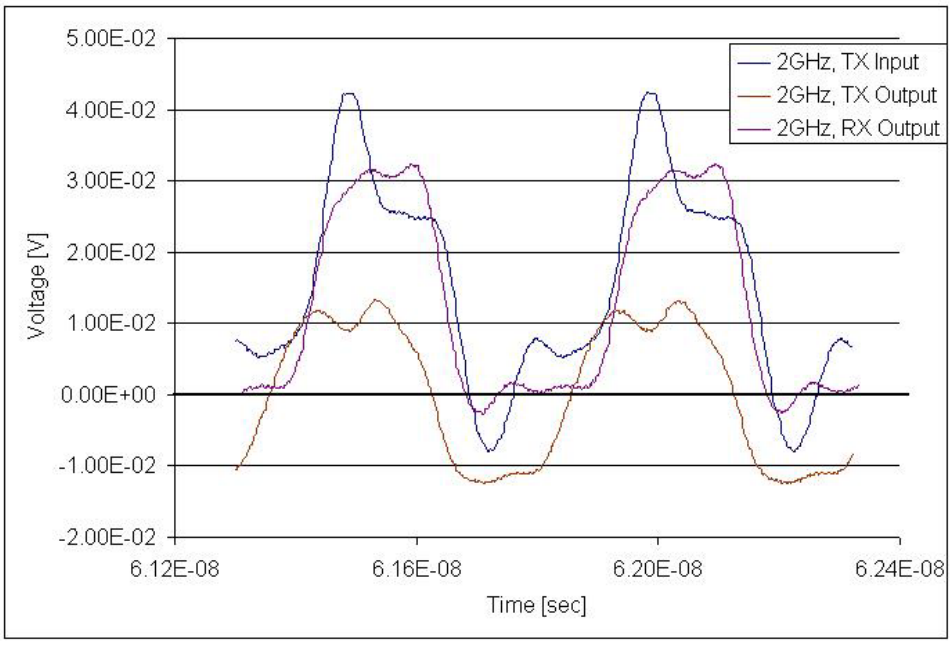


Figure 57 Performance of capacitively-coupled driver and receiver connected through an off-chip bondwire with 2GHz input square wave

Figure 58 shows the measured results at the output of the driver series coupling capacitor and the output of the signal recovered by the receiver for a 3.3V, 3GHz square wave input. The measured waveforms are sinusoidal in shape for two reasons. First, as supported by the simulations also shown in the figure, the transistors are beginning to approach their unity gain point so the harmonics that give a square wave its sharp edges are severely attenuated by the device performance. Additionally, the 3dB bandwidth of the probe used to measure the output is 7GHz. The effects of this bandwidth constraint also contribute to the sinusoidal shape of the measured signals. It is not possible to distinguish between the roll-off of the transistors and the roll-off of the measurement equipment so the total delay is not measured for this frequency. Even though the transistors are approaching their roll-off frequency, the receivers correctly recover the input signal.

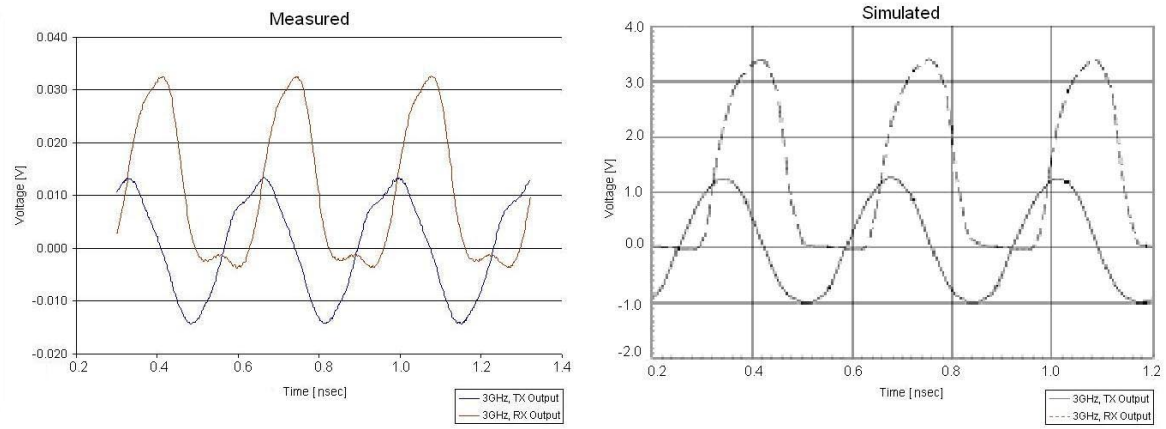


Figure 58 Performance of capacitively-coupled driver and receiver connected through an off-chip bondwire with 3GHz input square wave

With an NRZ data-coding scheme, a system with 0.35μm circuits is capable of operating at 6Gbit/sec! The prospects for CCI improve as transistor technology improves. The current that can be passed through a capacitor is proportional to the time rate of change of the voltage across the capacitor. Therefore, communication via capacitive coupling relies on fast edge rates to transfer data across series capacitors and edge rates achievable with a three-stage inverting driver will improve as the designs are fabricated in 0.18μm and 0.13μm technologies. Also, the unity gain frequency of transistors will continue to increase and thereby allow higher data rates to be achieved. As the operating frequency increases, smaller capacitance values can be used. The reduction in capacitance can either allow the physical dimensions of the capacitors to be reduced thereby allowing for an increase in I/O density. Or, the gap between capacitor plates can be increased thereby easing the constraints on the package and substrate fabrication technologies.

4.3 Inductive Coupling

Inductive coupling relies upon integrated on-chip inductors to act as either the primary or the secondary of a transformer. A set of experiments is presented to study the performance of integrated on-chip inductors so that the design space available for the individual coupling elements can be understood. However, since an LCI system must be designed so that on-chip inductors are coupled to off-chip inductors, three other sets of experiments have been designed to 1) validate the analysis of the coupled inductor model presented in the previous chapter, 2) understand the impact of lateral offset upon coupled inductor performance, and 3) determine the impact of crosstalk due to nearest neighbors and thereby understand the limits on I/O density.

4.3.1 Experimental Design

Experiments to quantify inductor performance are designed to understand the effects of geometric variations upon inductor performance. These experiments have been designed using a CAD tool by OEA named Spiral and are targeted for the TSMC 0.35µm CMOS process. Experiments have also been designed to validate the transformer model discussed in the previous chapter have been designed using a combination of CAD tools including Spiral and a freeware tool named ASITIC. These coupled inductor experiments are targeted to both the TSMC 0.25µm and the TSMC 0.35µm processes. Photographs of the two fabricated ICs from which results are measured are shown in Figure 59.

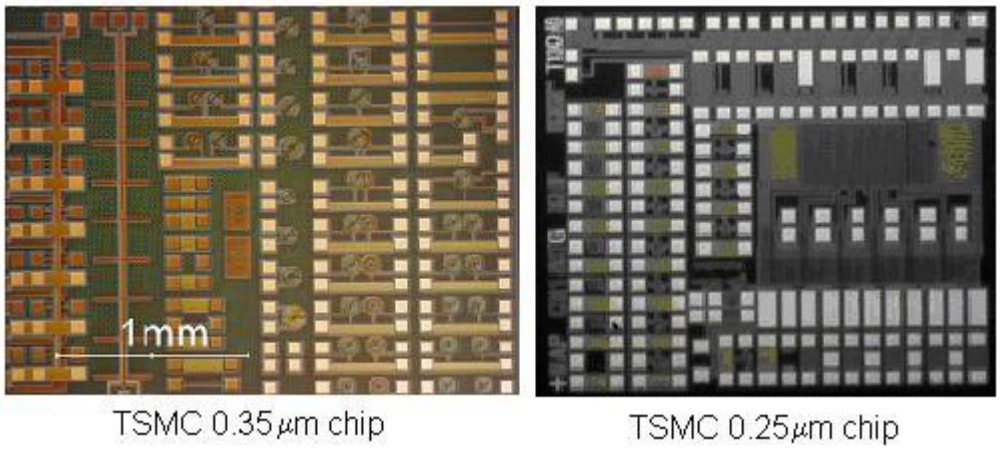


Figure 59 Photographs of inductor and transformer experiments fabricated in TSMC 0.35µm and TSMC 0.25µm processes

4.3.1.1 Inductor Geometric Variations

Several experiments have been designed with the goal of developing constraints on inductor layout to achieve desired frequency- and time-domain responses. The individual inductor experiments serve the additional goal of validating the ability of CAD tools to predict the performance of on-chip inductors.

'Spiral', a CAD tool available from OEA has been used to explore the design space and choose the specific inductors to be fabricated. The inductor experiments have been designed for the TSMC 0.35µm process, and Table 2 provides the geometric details of the test structures.

Table 2 Inductors designed to study electrical impact of geometric variations in the TSMC 0.35μm process

Design Name	Type	Metal Width / Spacing [μm]	Number of Turns	Inner Diameter (avg) [μm]	Outer Diameter (avg) [μm]
B1(top)	Asymmetric	3.4 / 1.4	5	43.7	91.3
B1 (bottom)	Asymmetric	3.4 / 1.4	5	36.6	83.9
B2	Asymmetric	3.4 / 1.4	5	23.6	71.3
B3	Asymmetric	3.4 / 1.4	5	43.7	91.3
B4	Asymmetric	3.4 / 1.4	5	63.5	111.3
B5	Symmetric	3.4 / 1.4	3	40	63.6
B6	Symmetric	3.4 / 1.4	4	40	73.2
B7	Symmetric	3.4 / 1.4	4	60	93.2
B8	Symmetric	3.4 / 1.4	6	40	115.4

All of the inductors have been designed with 8 sides. Except for 'B1' the experiments are fabricated on metal layer M4 and have in common diameter ≤ 120μm, $R_W \leq 30\Omega$ and L ≤ 3nH. Experiment 'B1' is an inductor composed of the series connection of windings on metal layers M2 and M4 and is expected to provide an inductance greater than 5nH. The inductor designs classified as 'asymmetric' are intended to be driven in a single-ended fashion as the inductor is wound from its input pad in a decreasing spiral into the center. Once the spiral is wound to the center, vias connect the spiral to an underpass that routes the center terminal to a ground pad. The 'symmetric' inductors start at both pad connections and spiral in toward the inductor center crossing over each other every half turn. In this way, the center point of the inductors could be grounded and the structure could be driven differentially. However, in these experiments the symmetric inductors are designed for single-ended drive. All of the inductors are designed with the same metal width and spacing, but the number of turns varies from 3 to 6, the inner diameter varies from 23.6μm to 63.5μm and the OD varies from 63.6μm to 115.4μm. Figure 60 shows photographs of the fabricated asymmetric inductor B3 and the symmetric inductor B6.

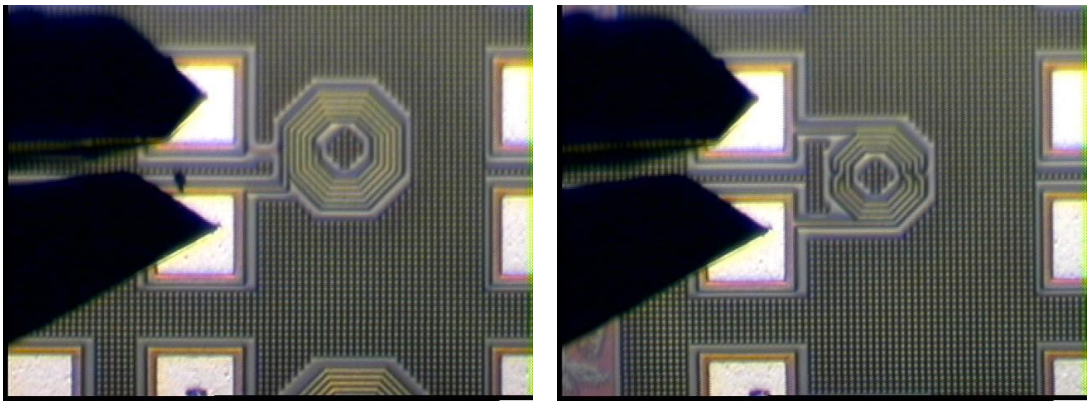


Figure 60 Photographs of two inductor experiments fabricated in the TSMC 0.35µm process
(left)design B3, (right) design B6

Spiral can generate a Spice-compatible model to predict the electrical performance of the inductors. Asymmetric inductors are fit to a 9-element model as shown in Figure 61 and symmetric inductors are fit to a more complex 19-element model as shown in Figure 62. Table 3 lists the values for the asymmetric model components and Table 4 lists the values for the symmetric model components. The value reported for B1 is expected to be too small because Spiral does not account for the mutual coupling between the two series-connected structures that comprise the inductor.

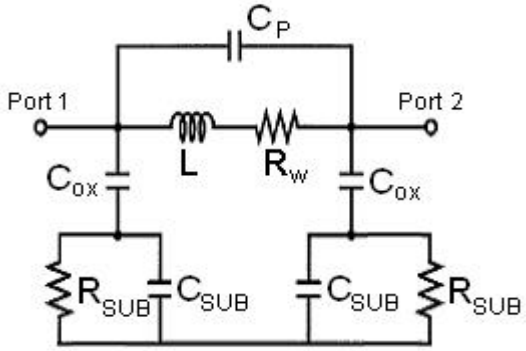


Figure 61 Lumped, asymmetric inductor model
generated by OEA Spiral

Table 3 Model values for asymmetric inductor designs generated by OEA Spiral
Component values refer to schematic in Figure 61

Design Name	L [nH]	R_W [Ω]	C_P [fF]	C_{OX} [fF]	C_{SUB} [fF]	R_{SUB} [Ω]
B1 (top)	2.0	22.0	124.2	6.1	11.4	43.0
B1 (bottom)	1.9	31.1	86.5	18.2	5.8	67.7
B2	1.1	17.9	71.7	8.9	6.3	75.9
B3	2.0	22.0	124.2	6.1	11.4	43.0
B4	2.8	28.3	126.4	9.4	12.3	45.2

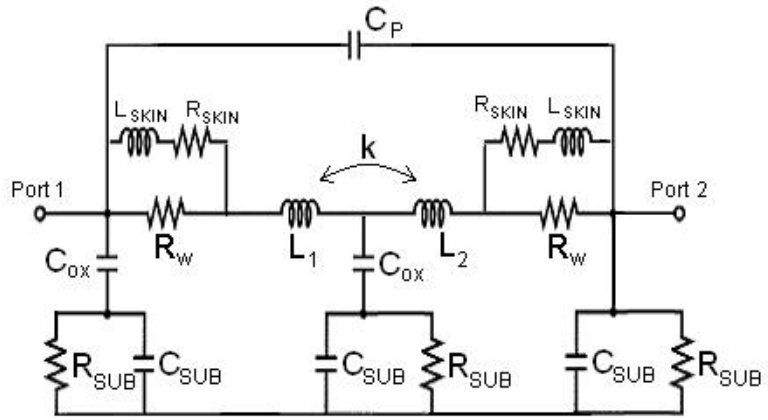


Figure 62 Lumped, symmetric inductor model generated by OEA Spiral

Table 4 Model values for symmetric inductor designs generated by OEA Spiral
Component values refer to schematic in Figure 62

Design Name	L1 [nH]	L2 [nH]	k	R_W [Ω]	C_P [fF]
B5	0.24	0.25	-0.44	13.1	21.4
B6	0.34	0.36	-0.63	18.8	14.6
B7	0.49	0.58	-0.66	17.5	23.5
B8	0.79	0.91	-0.70	18.7	59.8
Design Name	C_{OX} [fF]	C_{SUB} [fF]	R_{SUB} [Ω]	L_{SKIN} [pH]	R_{SKIN} [Ω]
B5	5.2	9.5	20.5	33.5	17.4
B6	6.7	21.0	16.6	92.7	25.8
B7	7.0	38.6	11.6	143.6	32.0
B8	15.7	61.1	8.1	224.9	14.0

When the symmetric inductors are driven as single-ended elements (i.e. with one terminal grounded), the total inductance seen from the ungrounded terminal will be approximately $L_1 + L_2 - 2M$ which is simply the equivalent inductance of series-connected coupled inductances. Since the inductors are measured as one-port devices, the effective inductances that should be measured are calculated from the preceding formula and reported in Table 5.

Table 5 Effective inductance for symmetric inductors driven as single-ended elements

Design Name	$L_{EFFECTIVE}$ [nH]
B5	0.7
B6	1.1
B7	1.8
B8	2.9

ASITIC can also be used to generate Spice-compatible models for predicting the electrical performance of inductors. ASITIC fits the parameters of all inductors to the simple model shown in Figure 63. ASITIC does its parameter fitting at a single frequency point, and for these experiments the frequency is chosen to be 1GHz. The model values for the inductor experiments predicted by ASITIC are listed in Table 6.

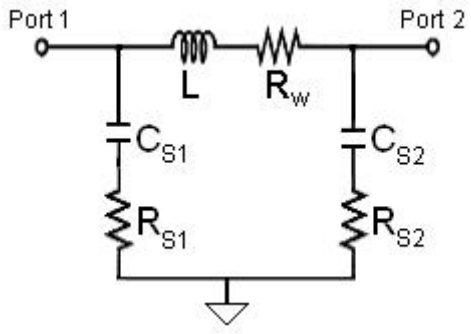


Figure 63 Lumped, narrow band inductor model generated by ASITIC

Table 6 Model values for inductor designs generated by ASITIC at 1GHz

Design Name	L [nH]	R_W [Ω]	C_{S1} [fF]	C_{S2} [fF]	R_{S1} [Ω]	R_{S2} [Ω]
B1	9.2	25	22	42	1260	682
B2	0.91	5.6	13	9.9	1090	1750
B3	1.7	8.4	18	15	880	1350
B4	2.5	11	23	20	760	1060
B5	0.62	4.4	10	10	1310	1270
B6	1.1	6.4	13	13	1180	1180
B7	1.7	8.5	18	18	960	960
B8	2.4	11	23	23	800	800

4.3.1.2 Transformer Geometric Variations

Several experiments have been designed with the goal of validating the ability of both CAD tools to predict the performance of on-chip transformers. The individual transformer experiments serve the two additional goals of 1) developing constraints on transformer layout to achieve desired frequency- and time-domain responses and 2) providing a baseline for subsequent coupling and crosstalk experiments.

A total of ten transformer structures with varying geometry have been designed for the TSMC0.35µm and TSMC 0.25µm fabrication processes. Table 7 provides the geometric details of the four transformer structures fabricated in the TSMC 0.35µm process and Figure 64 shows photographs of experiments B3 and B6 from the fabricated IC. Table 8 provides the details of the six transformer structures fabricated in the TSMC 0.25µm process and Figure 65 shows photographs of experiments 'L50wb' and 'L75wb' from the fabricated IC. Experiments A1 and C2 are composed of two overlapped instances of the inductor B6 – one instance on metal 2 and the other on metal 4 – to create a transformer. Experiments C1 and C3 are composed of two overlapped instances of the inductor B3 – one instance on metal 2 and the other on metal 4 – to create a transformer. Experiments C1 and C2 have polysilicon patterned ground shields below them to reduce the substrate parasitics [56].

Table 7 Geometric parameters of transformers designed for the TSMC 0.35µm process

Design Name	Type	Metal Width / Spacing [µm]	Number of Turns	Inner Diameter [µm]	Outer Diameter [µm]
A1	8-sided, Symmetric	3.4 / 1.4	4	40	73.2
C1	8-sided, Asymmetric, with PSG	3.4 / 1.4	5	43.7	91.3
C2	8-sided, Symmetric, with PSG	3.4 / 1.4	4	40	73.2
C3	8-sided, Asymmetric	3.4 / 1.4	5	43.7	91.3

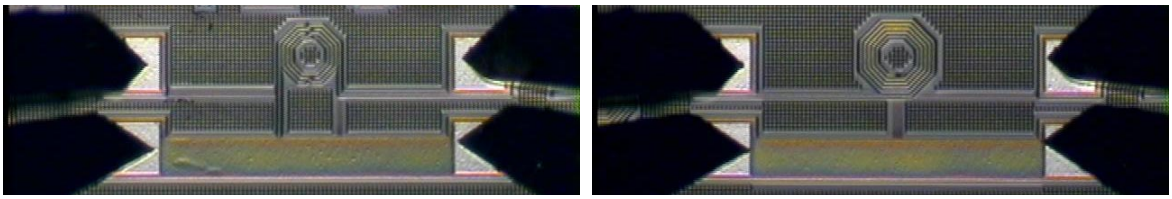


Figure 64 Photographs of two transformer experiments fabricated in the TSMC 0.35µm process
(left) design A1, (right) design C3

Table 8 Geometric parameters of transformers designed for the TSMC 0.25µm process

Design Name	Type	Metal Spacing [µm]	Number of Turns	Inner Diameter [µm]	Outer Diameter [µm]
L50	4-sided, Asymmetric with PSG	0.45 / 0.45	25	5.85	50.0
L50w	4-sided, Asymmetric with PSG	0.60 / 0.60	18	7.80	50.0
L50wb	4-sided, Asymmetric with PSG	1.20 / 1.20	9	8.40	50.0
L75	4-sided, Asymmetric with PSG	0.45 / 0.45	39	5.85	75.0
L75w	4-sided, Asymmetric with PSG	0.60 / 0.60	28	7.80	75.0
L75wb	4-sided, Asymmetric with PSG	1.20 / 1.20	14	8.40	75.0

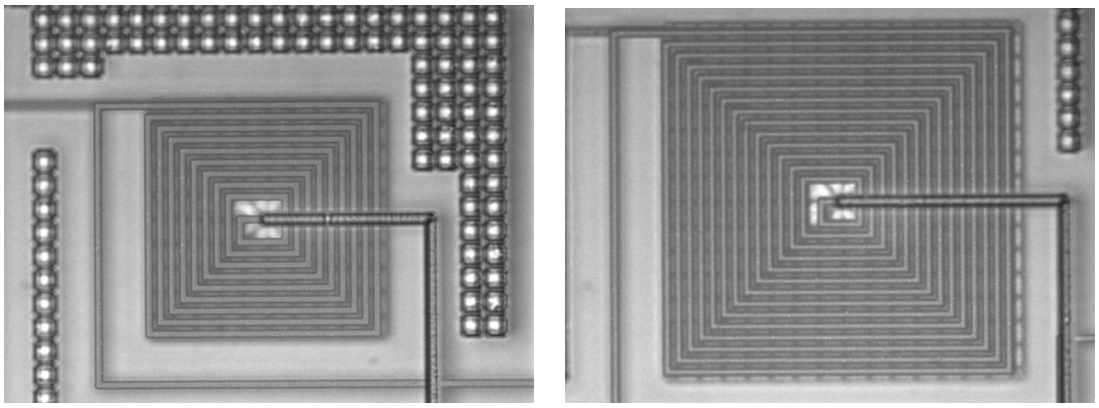


Figure 65 Photographs of two transformer experiments fabricated in the TSMC 0.25µm process
(left) design "L50wb", (right) design "L75wb"

ASITIC can be used to estimate the performance of on-chip transformers. However, the transformer models generated by this tool are narrowband and can lead to non-physical model values. ASITIC does not create transformer models that take user-defined grounding structures into account. As a result, the model values generated by ASITIC are the same for C2 and A1 and for C1 and C3 even though these pairs of designs are different by the presence or absence of a patterned ground shield. In addition, all of the TSMC 0.25µm designs have polysilicon patterned ground shields underneath them. The values of R_G reported by ASITIC for these experiments are expected to be pessimistic.

Figure 66 shows the lumped model ASITIC generates for transformers. Table 9 and Table 10 list the component values predicted by ASITIC for the TSMC 0.35µm and TSMC 0.25µm experiments, respectively.

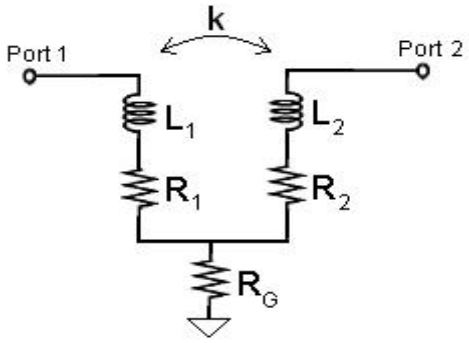


Figure 66 Lumped transformer model
generated by ASITIC

Table 9 Model values for TSMC 0.35µm transformer designs predicted by ASITIC

Design Name	L_1 [nH]	L_2 [nH]	k	R_1 [Ω]	R_2 [Ω]	R_G [Ω]
A1, C2	1.1	1.1	0.71	6.3	6.3	0.021
C1, C3	1.7	1.7	0.72	8.3	8.3	0.030

Table 10 Model values for TSMC 0.25µm transformer designs predicted by ASITIC

Design Name	L_1 [nH]	L_2 [nH]	k	R_1 [Ω]	R_2 [Ω]	R_G [Ω]
L50	19.8	19.8	0.53	230	254	N/A
L50w	9.1	9.0	0.54	106	124	0.15
L50wb	2.4	2.4	0.55	27	37	0.01
L75	67.4	67.3	0.64	520	557	N/A
L75w	30.8	29.7	0.66	236	270	3.6
L75wb	8.0	7.9	0.65	60	75	0.21

4.3.1.3 Alignment and Crosstalk

Twelve transformer structures of varying lateral offset have been designed for the TSMC0.35µm processes to determine how chip-chip (or chip-substrate) alignment will impact transformer coupling. Five other experiments have been designed to quantify the distance over which nearest neighbor inductors will interfere with each other with the goal of understanding the limits on I/O density in an LCI system

These experiments can be described in three sets (labeled A, C, and D). The A and C sets (comprising designs A1 – A4 and C3 – C10) are designed to study the effect of chip-chip alignment on transformer coupling. In these experiments, one inductor is fabricated on metal level 4 and the other inductor is fabricated on metal level 2. The amount of lateral offset is increased until a distance separates the two inductors slightly less than their diameter. The experiment set labeled D (comprised of designs D6 – D10) is designed to study coupling between neighboring inductors. In these experiments, both inductors are fabricated on metal level 4 and the amount of lateral offset is increased until a distance separates the two inductors slightly greater than their diameter.

All sets of experiments have been done with fixed designs for the inductors. Designs A1 – A4 use two instances of the individual inductor B6 and designs C3 – C10 and D6 – D10 use two instances of inductor B3. The physical specifications for the inductors in each experiment set are listed in Table 11. Table 12 lists both the edge-edge pitch of the two inductors in each experiment and in parentheses the amount of overlap is listed. When the pitch is less than the diameter of the inductors, the inductors are physically overlapped as indicated by

the positive overlap distance in the table. On the contrary, when the pitch is greater than the diameter of the inductors, the inductors are not physically overlapped, and the negative overlap distance in the table indicates this. Figure 67 shows photographs of experiments C6 and C7. These designs are representative of this type of alignment / crosstalk structure.

Table 11 Primary and secondary inductor geometries to study effect of lateral offset upon inductor coupling

TSMC 0.35μm 4 metal, 1 poly process

Design Set	Type	Metal Width / Spacing [μm]	Number of Turns	Inner Diameter [μm]	Outer Diameter [μm]	Metal Level / Port Number
A (primary)	Symmetric	3.4 / 1.4	3 5/8	40	73.2	M2
A (secondary)	Symmetric	3.4 / 1.4	3 5/8	40	73.2	M4
C (primary)	Asymmetric	3.4 / 1.4	5	43.7	91.3	M4
C (secondary)	Asymmetric	3.4 / 1.4	5	43.7	91.3	M2
D (input)	Asymmetric	3.4 / 1.4	5	43.7	91.3	M4
D (output)	Asymmetric	3.4 / 1.4	5	43.7	91.3	M4

Table 12 Lateral offsets for transformer alignment experiments

Design Name	x-pitch, (overlap) [μm]	Design Name	x-pitch, (overlap) [μm]	Design Name	x-pitch, (overlap) [μm]
A1	0.0, (75.6)	C5	46.0, (44.0)	D6	99.4, (-9.4)
A2	37.8 (37.8)	C6	68.0, (22.0)	D7	112.4, (-22.4)
A3	85.0 (-9.4)	C7	99.4, (-9.4)	D8	137.4, (-47.4)
A4	123.0 (-47.4)	C8	112.4, (-22.4)	D9	162.4, (-72.4)
C3	2.0, (88.0)	C9	137.4, (-47.4)	D10	187.4, (-97.4)
C4	24.0, (66.0)	C10	162.4, (-72.4)		

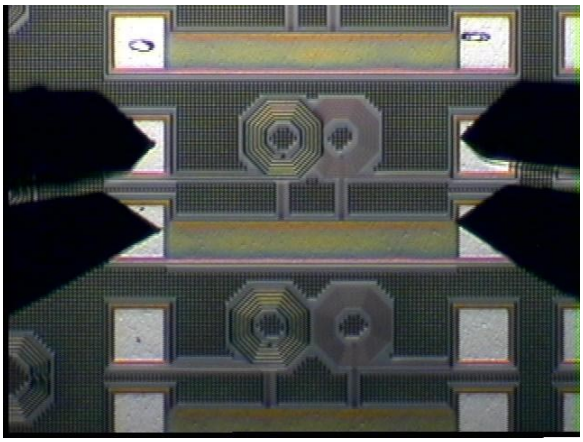


Figure 67 Photographs of transformer experiments derived from design C3 with increasing lateral offset and fabricated in the TSMC 0.35μm process
(top) design C6, (bottom) design C7

ASITIC can be used to estimate the coupling between inductors on different metal levels (i.e. for the transformer coupling experiments) and to estimate the coupling between inductors on the same metal level (i.e. for the nearest neighbor crosstalk experiments). Table 13 and Table 14 presents the transformer model values generated by ASITIC for the transformer alignment experiments, and Table 15 lists the model values for the inductor crosstalk experiments. ASITIC predicts the mutual coupling between neighboring inductors drops rapidly as a function of offset. This trend leads to two observations. First, chip-chip alignment must be controlled to assure good coupling between inductors intended to behave as transformers. Secondly, it should be possible to place inductors close to nearest neighbors and achieve high I/O densities without much crosstalk interference.

Table 13 Model values for TSMC 0.35μm transformer alignment experiments A1-A4 predicted by ASITIC

Design Name	L_1 [nH]	L_2 [nH]	k	R_1 [Ω]	R_2 [Ω]	R_G [mΩ]
A1	1.1	1.1	0.71	6.3	6.3	21
A2	1.1	1.1	0.054	6.3	6.3	2.0
A3	1.1	1.1	0.018	6.3	6.3	0.41
A4	1.1	1.1	0.0051	6.3	6.3	0.12

Table 14 Model values for TSMC 0.35µm transformer alignment experiments C3-C10 predicted by ASITIC

Design Name	L_1 [nH]	L_2 [nH]	k	R_1 [Ω]	R_2 [Ω]	R_G [Ω]
C3	1.7	1.7	0.72	8.3	8.3	30
C4	1.7	1.7	0.41	8.3	8.3	14
C5	1.7	1.7	0.021	8.3	8.3	1.9
C6	1.7	1.7	0.071	8.3	8.3	3.7
C7	1.7	1.7	0.017	8.3	8.3	0.63
C8	1.7	1.7	0.011	8.3	8.3	0.41
C9	1.7	1.7	0.0054	8.3	8.3	0.22
C10	1.7	1.7	0.0030	8.3	8.3	0.12

Table 15 Model values for TSMC 0.35µm inductor crosstalk experiments predicted by ASITIC

Design Name	L_1 [nH]	L_2 [nH]	k	R_1 [Ω]	R_2 [Ω]	R_G [Ω]
D6	1.7	1.7	0.017	8.3	8.3	0.60
D7	1.7	1.7	0.011	8.3	8.3	0.40
D8	1.7	1.7	0.0055	8.3	8.3	0.20
D9	1.7	1.7	0.0030	8.3	8.3	0.12
D10	1.7	1.7	0.0018	8.3	8.3	0.075

4.3.2 Measured Results

Both time- and frequency-domain measurements have been made on the various inductor, transformer and crosstalk experiments described in the previous section. Unless noted otherwise, time-domain reflectometry (TDR) and time-domain transmission (TDT) measurements have been performed with a Tektronix 11801 sampling oscilloscope with SD-24 and SD-26 sampling heads and HP 8133A signal generator; DC measurements have been performed on an Agilent 4155C parameter analyzer with Cascade Microtech DC probes; and high-frequency measurements (up to 20GHz) have been made on an HP 8510 vector network analyzer with either G-S or G-S-G model 40A probes by GGB Industries. Numerous software programs such as ADS, Maple, Matlab, Octave (a linux freeware tool similar to Matlab), Excel and customized GPIB programs have been used to acquire, analyze and graph the measured data.

4.3.2.1 Inductor Geometric Variations

Only the DC resistance of the individual inductors can be measured directly. The remaining parameters of the inductors (e.g. inductance, parasitic capacitance) are determined through a measurement and extraction procedure. That is, s-parameter data is measured from 200MHz to 20GHz and the effects of the measurement testbed are de-embedded from the data using Koolen's method [145]. The resulting data is then imported into ADS and component values for an inductor model are adjusted to minimize the error between the measured and modeled s-parameters. A schematic of the inductor model to which the data is fit is shown in Figure 68. This model captures the fact that the measured inductors have one terminal grounded are driven in a single-ended manner.

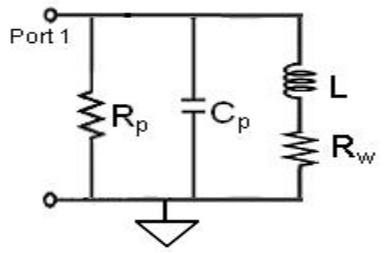


Figure 68 Model of inductor used to match measured data

Measured DC resistances for the individual inductors from the TSMC 0.35μm inductor experiments are reported in Table 16. The extracted values for inductance, winding resistance, shunt capacitance and substrate loss are also reported in the table. The extracted winding resistance is slightly lower than the measured winding resistance for two reasons. First, the measured resistance includes the 1Ω - 2Ω of probe resistance from the measurement equipment. Secondly, for the sake of model simplicity, the extracted winding resistance value is chosen to make the model s-parameters match the measured s-parameters over a broad frequency range (200MHz to 20GHz) rather than correspond exactly to a physical quantity.

Table 16 Measured and extracted values for TSMC 0.35µm inductors

Design Name	Inductance: extracted [nH]	*Winding Resistance: measured [Ω]*	Winding Resistance: extracted, [Ω]	Shunt Capacitance: extracted [fF]	Substrate Loss [Ω]
B1	7.4	*36.5*	34.0	40	1200
B2	1.3	*12.0*	10.0	20	1740
B3	2.2	*15.0*	13.5	15	1686
B4	3.3	*20.0*	17.0	15	1720
B5	0.9	*8.5*	6.0	5	400
B6	1.4	*11.0*	8.9	10	700
B7	2.0	*13.5*	11.5	18	825
B8	3.0	*15.0*	11.3	40	1000

Figure 69 shows a comparison of the S_{11} for the extracted model versus the measured S_{11} for inductor B3 and Figure 70 shows a comparison of S_{11} for the extracted model versus the measured S_{11} for inductor B6. The results from these inductors are presented because they form the basis for the TSMC 0.35µm transformer and crosstalk experiments; however, all of the extracted models match their respective measured data equally well. The extracted model for inductor B3 matches the measured data almost perfectly from 200MHz to about 8GHz. For frequencies beyond 8GHz the models are within 0.25dB of the measured data. The discrepancy between measured and modeled S_{11} occurs at high frequencies because the model does not capture the resistive loss due to the skin effect. The extracted model for the symmetric inductor B6 matches the measured data to within 0.5dB from 200MHz to 20GHz.

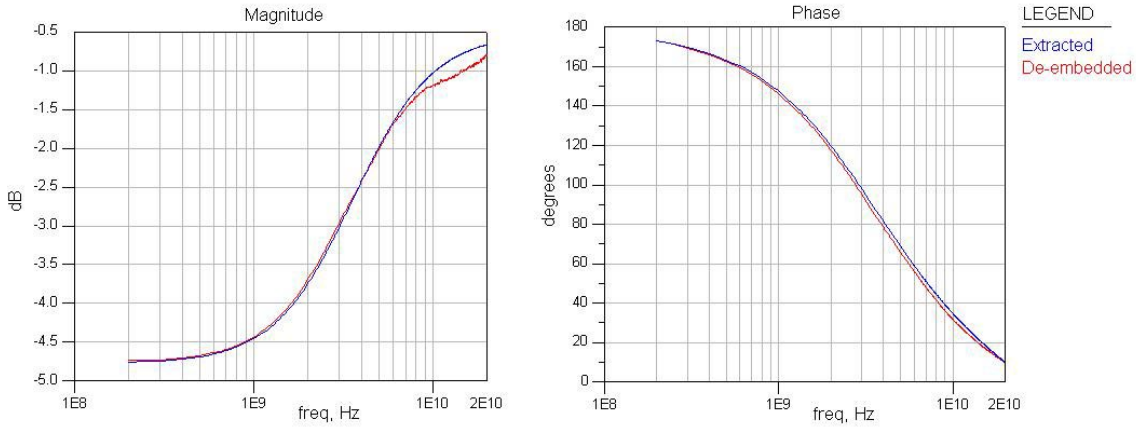


Figure 69 Measured (de-embedded) and extracted S_{11} magnitude / phase response of inductor B3
(red) Measured curve de-embedded from raw s-parameter data
(blue) Simulated from model fit to de-embedded data

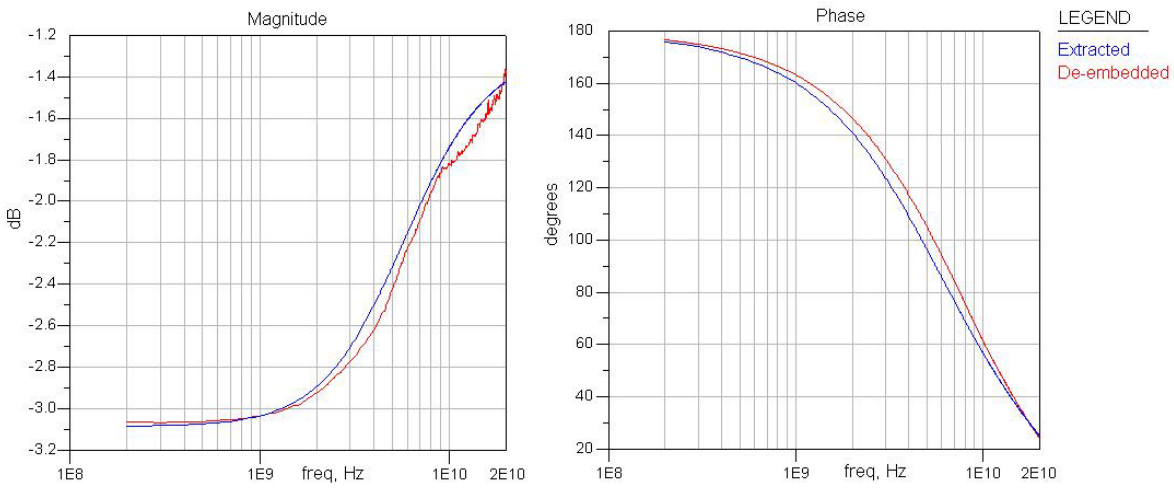


Figure 70 Measured (de-embedded) and extracted S_{11} magnitude / phase response of inductor B6
(red) Measured curve de-embedded from raw s-parameter data
(blue) Simulated from model fit to de-embedded data

The extracted values of inductance are compared to the inductance values predicted by Spiral and ASITIC in Table 17. As mentioned previously, Spiral does not account for the mutual inductance between the series-connected structures comprising inductor B1 so it is not surprising that the most significant percent error occurs for the inductance predicted by Spiral for this structure. For the remaining structures, both CAD tools tend to make pessimistic predictions for inductance but are generally within 25% of the extracted value.

Table 17 Comparison of extracted values for TSMC 0.35µm inductors and values predicted by Spiral and ASITIC
§ $L_{OEA\ SPIRAL}$ does not account for mutual coupling between the two series-connected inductors composing inductor B1

Design Name	$L_{EXTRACTED}$ [nH]	$L_{\backslash OEA\_SPIRAL}$ [nH]	L_{ASITIC} [nH]	% Error (extracted vs. Spiral)	% Error (extracted vs. ASITIC)
B1	7.4	3.9§	9.2	-47.3%	+24.0%
B2	1.3	1.1	0.91	-15.4%	-30.0%
B3	2.2	2.0	1.7	-9.1%	-22.7%
B4	3.3	2.8	2.5	-15.2%	-24.2%
B5	0.9	0.7	0.62	-22.2%	-31.1%
B6	1.4	1.1	1.1	-24.1%	-21.4%
B7	2.0	1.8	1.7	-10.0%	-15.0%
B8	3.0	2.9	2.4	-3.3%	-20.0%

Since the models generated by the CAD tools are different than the model to which measured data is fit, it is instructive to compare the predicted and measured electrical *performance* rather than predicted and extracted model *values*. Figure 71 shows the time- and frequency-domain performance of the extracted and predicted models for inductors B3 and B6. In these graphs, the time-domain response is to a 2V step input with 50ps rise time. Spiral predicts the rising-edge response and peak time domain voltage to within a few mV but over estimates the steady state time domain response. ASITIC also captures the rising edge behavior but slightly under estimates the peak voltage and steady state time domain response. In the frequency domain, ASITIC predicts the passband behavior of the inductor to within a few dB but the model used by Spiral under estimates the upper 3dB frequency.

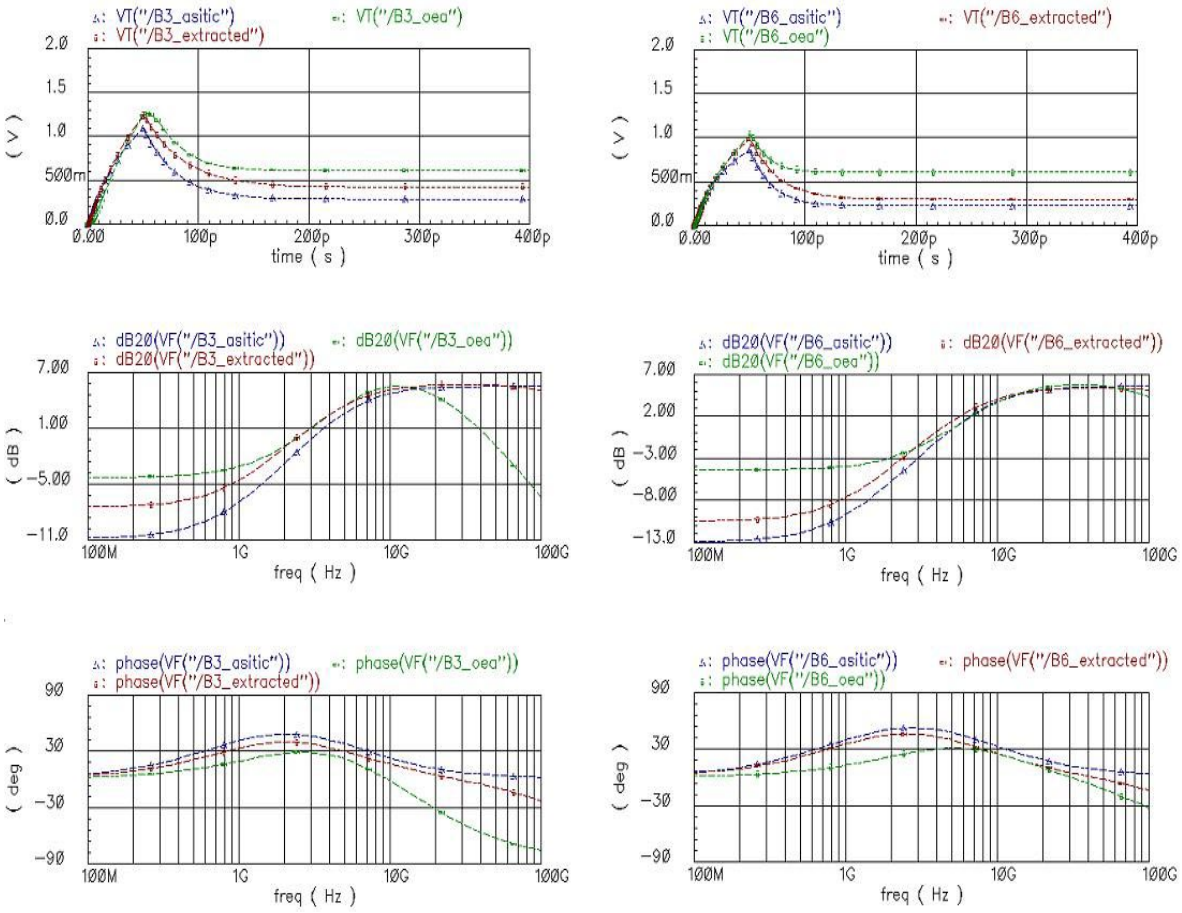


Figure 71 Time- and frequency-domain performance of extracted and predicted models for inductor B3 and B6
(left) inductor B3 step-, magnitude- and, phase response
(right) inductor B6 step-, magnitude- and, phase response
(red) Extracted model, (green) OEA Spiral model, (blue) ASITIC model

Both Spiral and ASITIC can be used to predict inductance and winding resistance with about 20% accuracy. Moreover, the model predicted by ASITIC is a good predictor of inductor behavior around the frequency where

the model is calculated. Therefore the goal of evaluating the utility of CAD tools for inductor has been accomplished. The other goal of understanding the tradeoffs between inductor layout and electrical performance can be achieved through exhaustive simulation with ASITIC. From the measured results presented here, a few trends are apparent. Larger diameter inductors tend to result in larger values of inductance. Also, symmetric inductors tend to result in less winding resistance per unit area than asymmetric inductors, but asymmetric inductors tend to result in slightly greater inductance per unit area than symmetric inductors. Therefore, inductance and winding resistance can be traded off through careful inductor design.

4.3.2.2 Transformer Geometric Variations

As with the inductors, only the DC resistance of the transformers can be measured directly. The remaining parameters (e.g. inductances, coupling coefficient, parasitic capacitance, etc) are determined through the measurement of the full two-port s-parameters and an extraction procedure similar to that employed for the inductor data. A schematic of the transformer model to which the data is fit is shown in Figure 72.

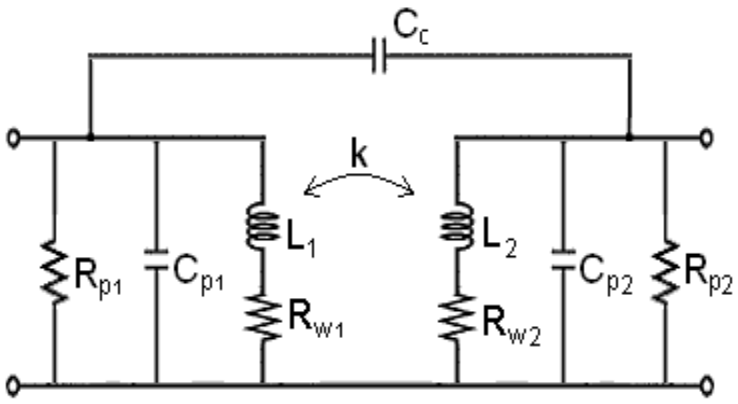


Figure 72 Model of transformer used for matching measured data

Each transformer in the TSMC 0.35μm experiments A1 – A4 and C2 is composed of two instances of inductor B6 and each transformer in experiments C1, C3 – C10 and D6 – D10 is composed of two instances of inductor B3. Thus the measured DC resistances of these experiments are the same as those already presented in Table 16 for the respective baseline inductor. The extracted values for inductance, winding resistance, coupling, capacitance and substrate loss are reported in Table 18.

Table 18 Extracted values for TSMC 0.35µm transformers

Design Name	L_1 [nH]	L_2 [nH]	R_{W1} [Ω]	R_{W2} [Ω]	k
A1	1.4	1.3	9	23	0.66
C1	2.2	2.7	14	33	0.71
C2	1.4	1.3	9	23	0.65
C3	2.2	2.6	14	30	0.77
Design Name	C_C [fF]	C_{P1} [fF]	C_{P2} [fF]	R_{P1} [Ω]	R_{P2} [Ω]
A1	16	10	29	4640	700
C1	30	15	25	1690	406
C2	17	10	26	3311	700
C3	35	15	21	1690	610

Figure 73 shows a comparison of the magnitude and phase of S_{11} and S_{22} for the extracted model versus the de-embedded measured s-parameters for transformer C3 and Figure 74 shows this comparison for S_{12} and S_{21}. These results are representative of the match that can be achieved in general between the de-embedded measured data and the transformer model. For all s-parameters, the extracted model matches the de-embedded phase within a few degrees from 200MHz to 20GHz. The extracted model also matches de-embedded magnitude across the entire measured frequency range within 2dB.

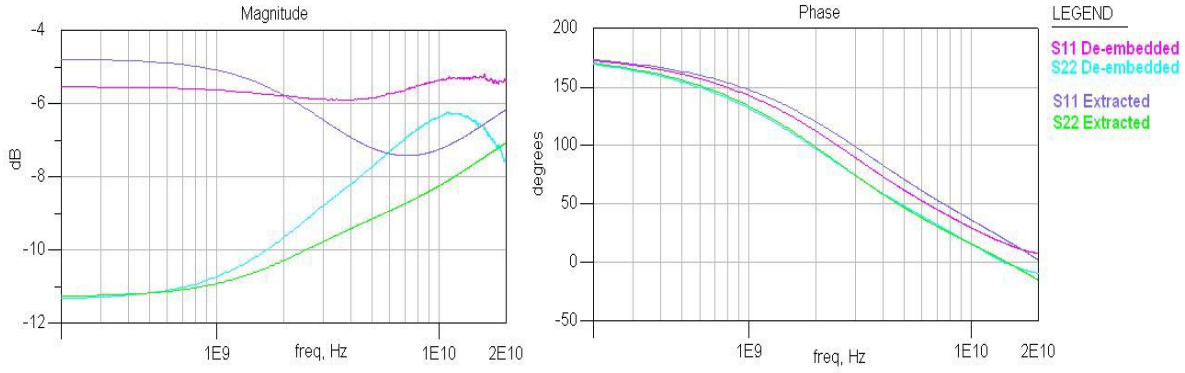


Figure 73 Measured (de-embedded) and extracted S_{11} and S_{22} magnitude / phase response of transformer C3

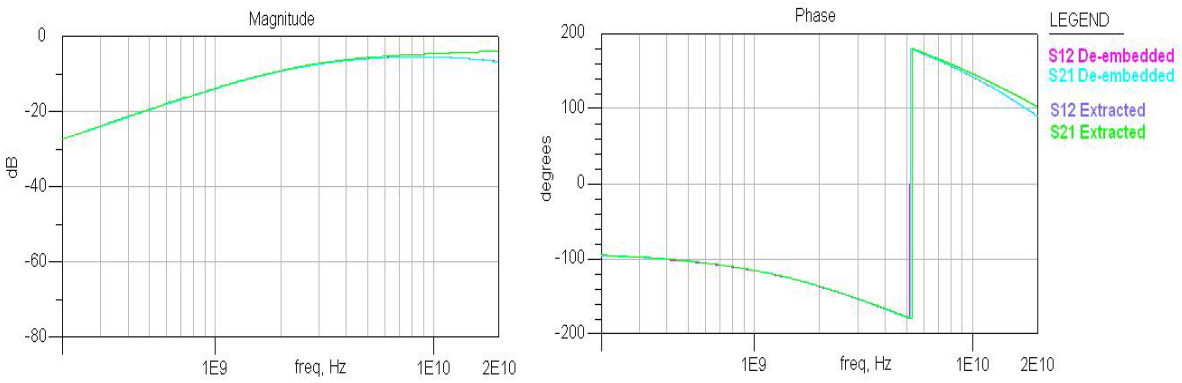


Figure 74 Measured (de-embedded) and extracted S_{12} and S_{21} magnitude / phase response of transformer C3

Comparing the values predicted by ASITIC and listed previously in Table 9 with the extracted model values in Table 18, it can be seen that for elements appearing in both models, the ASITIC predictions are within about 20% of the extracted parameters.

As with the inductors, comparing *electrical performance* rather than the *model values* is more meaningful since the transformer model generated by ASITIC does not have the same topology as the model used for parameter extraction. The time and frequency domain performance of the extracted models for transformers A1 and C3 are compared to the models predicted by ASITIC in Figure 75. The time domain responses are generated in simulation by applying at one terminal a 1V step with 50ps rise time and monitoring the output voltage at the other terminal. The frequency responses are simply the results of an AC sweep with a 1V AC input. The inductors comprising transformers A1 and C3 are wound in the same sense. Since the series loss of these structures is relatively small, the winding sense is evident from the notch in the passband of the magnitude responses of the transformers. As discussed in the previous chapter, this notch is sensitive to capacitance between inductors. ASITIC does not directly model this capacitance within a transformer so it is not surprising that its simple model does not capture this behavior. Except for this one shortcoming, the ASITIC model predicts the transformer behavior to within about 2dB of the extracted model and by extension within about 2dB of the measured data up to about 10GHz.

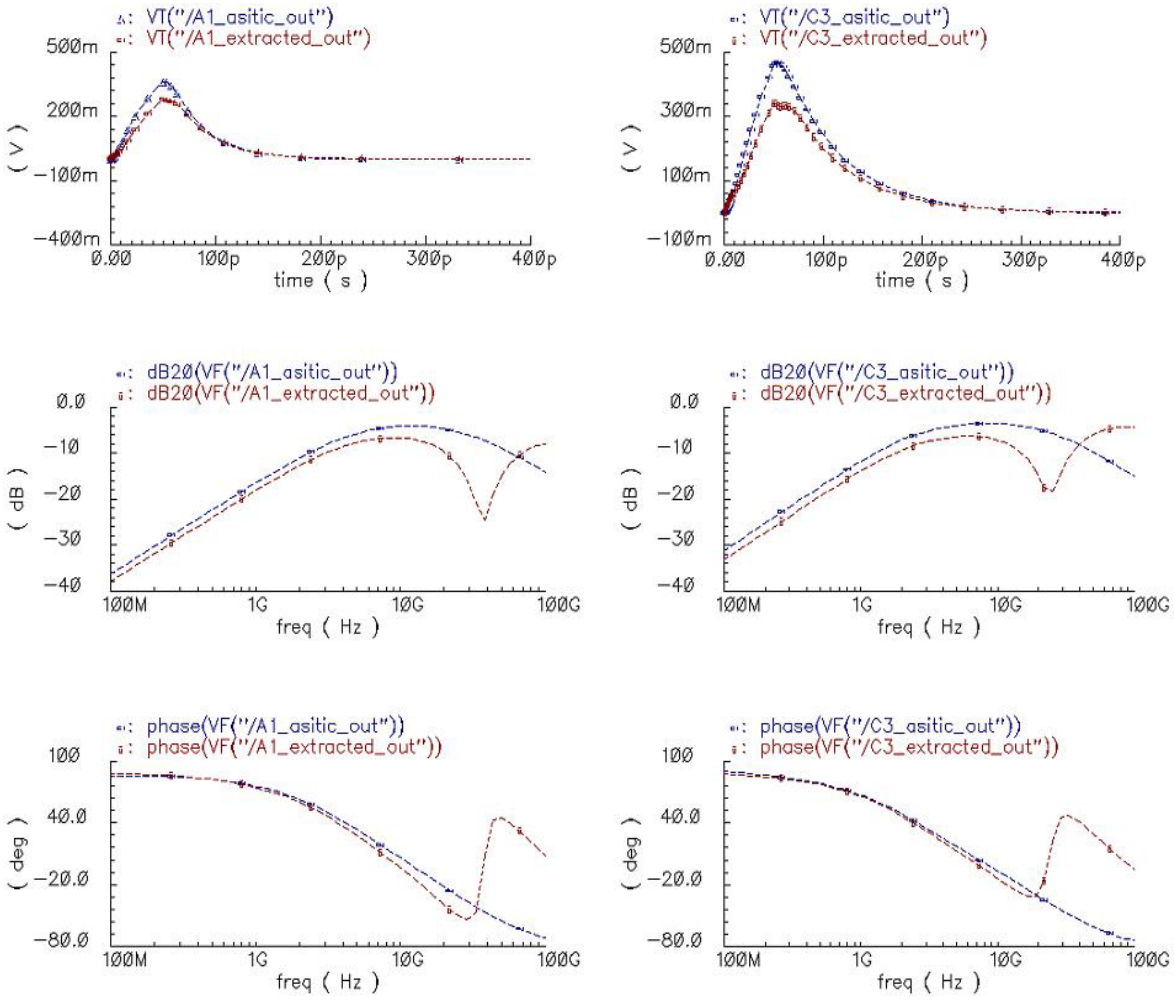


Figure 75 Time- and frequency-domain performance of extracted and predicted models for transformers A1 and C3
(left) transformer A1 step-, magnitude- and, phase response
(right) transformer C3 step-, magnitude- and, phase response
(red) Extracted model, (blue) ASITIC model

The TSMC 0.25µm experiments reveal similar trends. That is, the topology chosen for the extracted model can be used to create a circuit that fits the full two-port measured s-parameters data to within a few dB in magnitude and degrees in phase (*see Figure 76*). Also, the simple narrowband model predicted by ASITIC is somewhat optimistic when predicting the transient response of a transformer to a step input. Even still the ASITIC model captures the correct trend in the transient response and is within a few dB of the magnitude response up to 10GHz (*see Figure 77*).

The values extracted for inductance, winding resistance, mutual coupling, capacitance and substrate loss of the TSMC 0.25µm experiments are reported in Table 19. The values predicted for elements in the ASITIC

transformer model (*see Table 10*) are within about 20% of the value of corresponding elements in the extracted model only for the transformers that are composed of inductances under 10nH.

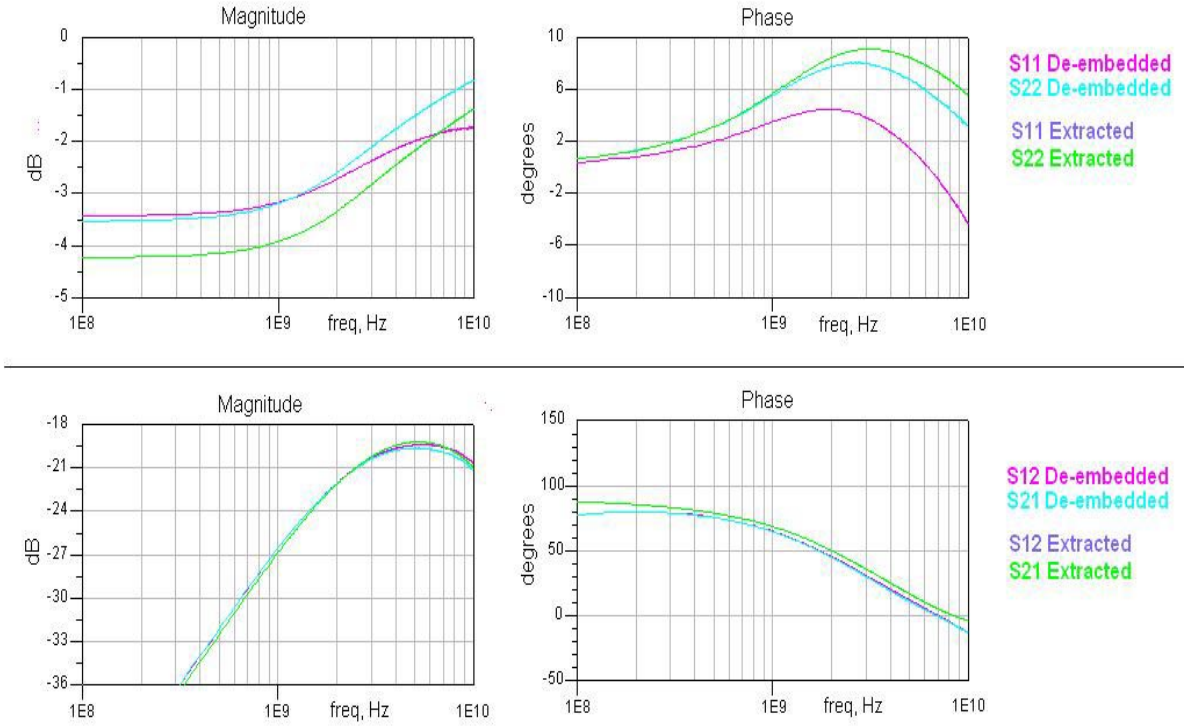


Figure 76 Measured (de-embedded) and extracted S_{11}, S_{22}, S_{21}, S_{12} magnitude and phase response of transformer L50w
(top) S11 and S22; (bottom) S21 and S12
(left) magnitude [dB], (right) phase [degrees]

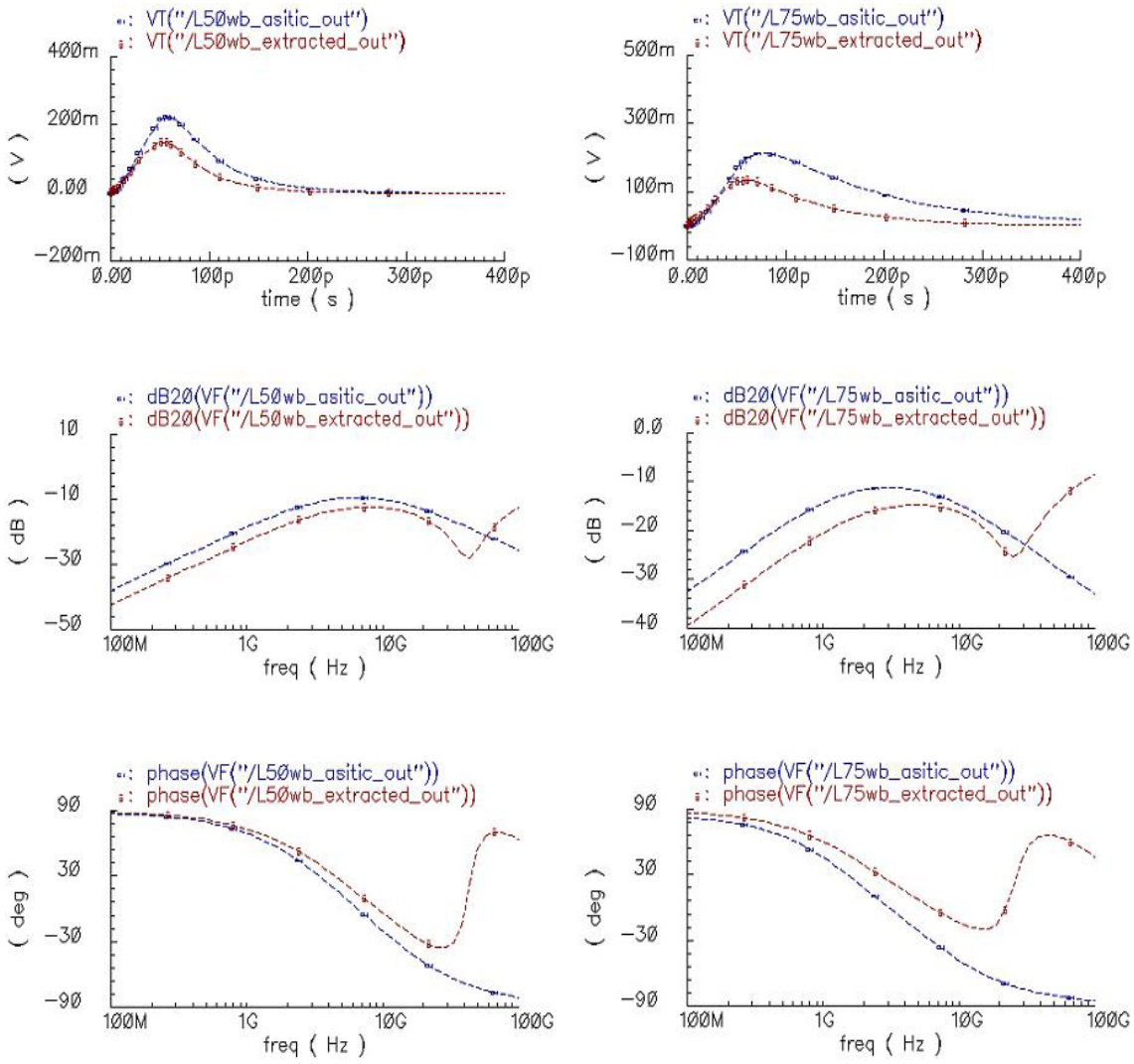


Figure 77 Time- and frequency-domain performance of extracted and predicted models for transformers L50wb and L75wb

Time domain response to 1V step with 50psec rise time
Frequency response generated by AC sweep with 1V source
(left) transformer L50wb step-, magnitude- and, phase response
(right) transformer L75wb step-, magnitude- and, phase response
(red) Extracted model, (blue) ASITIC model

Table 19 Extracted values for TSMC 0.25μm transformers

Design Name	L_1 [nH]	L_2 [nH]	R_{W1} [Ω]	R_{W2} [Ω]	K
L50	12	15	425	325	0.63
L50w	9	9	225	225	0.62
L50wb	3	4	74	74	0.63
L75	65	65	500	500	0.76
L75w	19	20	375	425	0.76
L75wb	9	10	150	155	0.76
Design Name	C_C [fF]	C_{P1} [fF]	C_{P2} [fF]	R_{P1} [kΩ]	R_{P2} [kΩ]
L50	5	4	4	4	5
L50w	7	4	4	3	3
L50wb	5	4	4	4	5
L75	8	8	5	3	3
L75w	8	7	5	4	5
L75wb	8	7	5	4	5

Given the number of structures available for measurement, several of the trends discussed in the previous chapter can be confirmed. Most importantly is the fact that the chosen model can be fit to within a few dB of measured data by using parameter values that correspond to predicted values. Since the predicted values of inductance, mutual coupling, and winding resistance are tied to the details of the physical structure and these values correspond to within ~20% of those in the extracted model it will be possible to relate model performance to physical transformer design. However, work remains to be done to estimate structure capacitance and substrate losses for coupled inductors in an LCI system prior to device fabrication.

In the discussion of geometric tradeoffs of transformer design, it is has been asserted that mutual coupling decreases as a function of the proportion of the vertical distance between inductors and the diameter of the inductors. Figure 78 shows the extracted coupling versus the ratio of vertical offset / inductor diameter for each of the transformer experiments. For a specific process the coupling does decrease as the ratio of offset / diameter increases. For example, the smaller 50μm transformers in the TSMC 0.25μm process have an extracted coupling coefficient of ~0.63 whereas the coupling of the large transformers fabricated on the same metal levels have an extracted coupling coefficient of ~0.76. However, the coupling coefficients of the 75μm transformers do not fit the trend otherwise present in the figure. These data points indicate that the coupling coefficient is a function of more than diameter and offset. In fact, Figure 23 shows ASITIC predicts that k depends upon inductor diameter, offset, winding width and winding spacing.

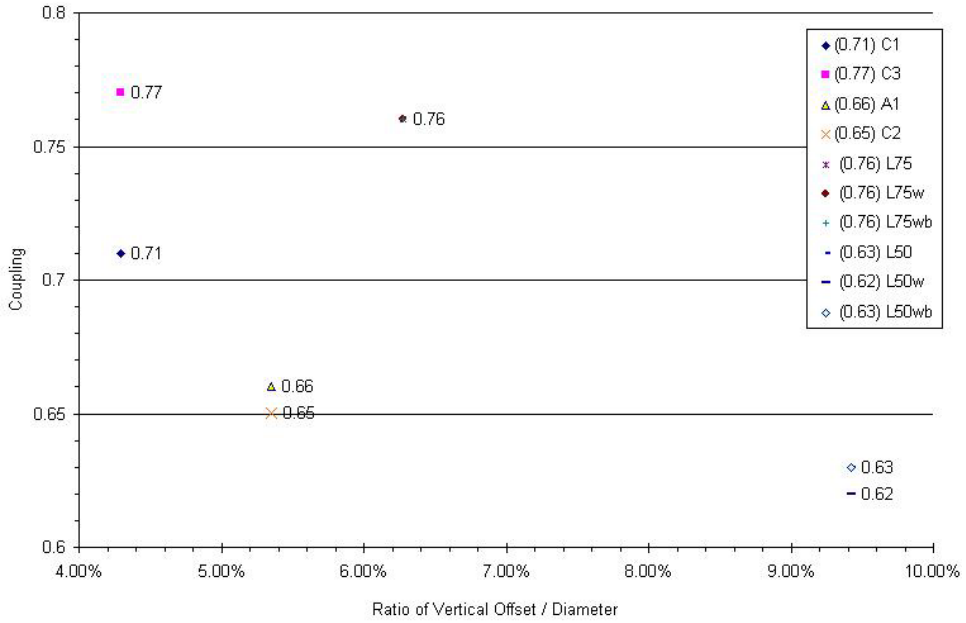


Figure 78 Extracted coupling coefficient versus ratio of vertical offset to transformer diameter for transformers fabricated in the TSMC 0.35µm and TSMC 0.25µm processes

In the analysis of the coupled inductor model it has been claimed that increasing winding resistance increases the attenuation through the transformer and the transformer passband is shifted to lower frequencies as the transformer inductances increase. These two effects can be observed together by comparing S_{21} of the 50µm and 75µm diameter inductors from the TSMC 0.25µm experiments as shown in Figure 79. The 50µm transformers increase in winding resistance and decrease in inductance in order of L50, L50w and L50wb. Likewise, the 75µm transformers increase in winding resistance and decrease in inductance in order of L75, L75w and L75wb. With respect to Figure 79, in each set of experiments, the least resistive transformers (e.g. L50wb and L75wb) suffer the least attenuation. Moreover, within each set of transformers, the center of the passband moves to lower frequencies as the inductance increases. For example, transformer L50w with $L_1 \approx L_2 \approx 9$nH has its peak response at approximately 5GHz but L50wb with $L_1 \approx L_2 \approx 3$nH has its peak response at approximately 7GHz.

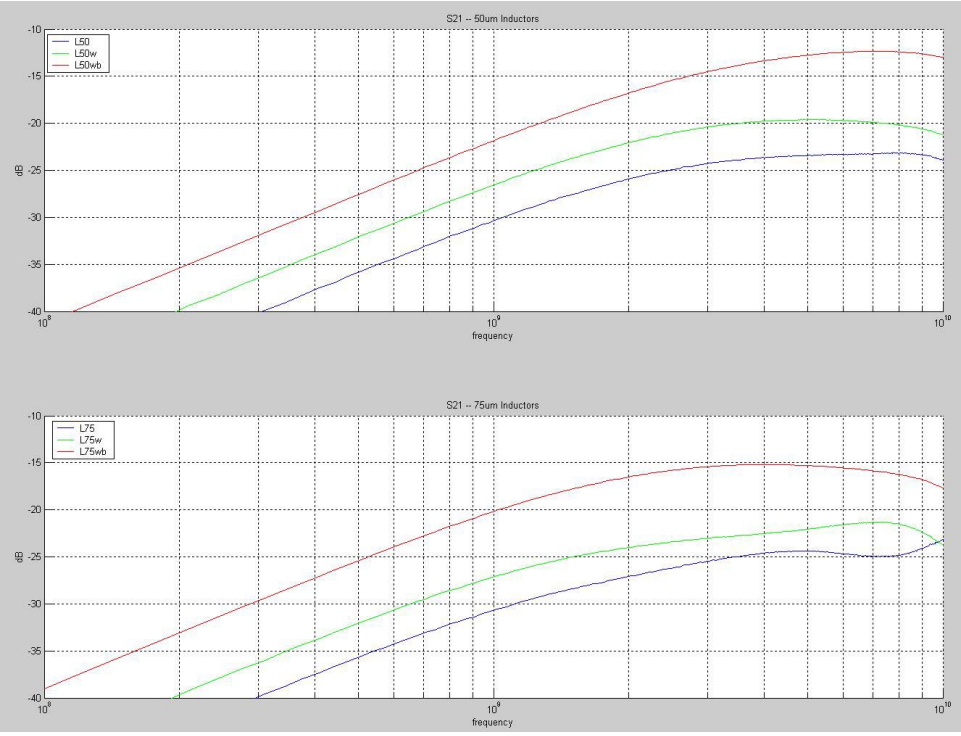


Figure 79 Comparison of measured S_{21} for TSMC 0.25µm transformers

When discussing the vast design space for coupled inductors, the claim is made that for any given value of inductance, there are numerous geometric configurations that can result in different coupling coefficients, winding resistances and parasitics. The claim can be substantiated in the measured data by comparing experiment L50w to L75wb. These two transformers have almost identical L1 and L2 of 9nH but the winding resistance of L50w is approximately 50% greater than that of L75wb. Further, the coupling coefficient of L75wb is 0.76 but the coupling coefficient of L50w is only 0.62. Therefore, when designing coupling elements for an LCI system, inductance, mutual coupling and winding resistance can be traded off through changes in transformer geometry.

Finally it has been claimed that the response of a transformer to a step input will decay within the duration of a single bit time and measured eye diagrams confirm this claim. Figure 80 presents eye diagrams measured for experiments A1 and C1-C3 with a 3.0Gbps NRZ pseudorandom bit sequence and Figure 81 presents eye diagrams measured for the same experiments but with a 1.0Gbps NRZ pseudorandom bit sequence. The measured data shows that for each transformer, the channel response reaches a peak voltage independent of data rate between 260mV for the symmetric transformers and 300mV for the asymmetric transformers in response to a 1V input. The eye openings are approximately 250mV for the symmetric transformers and 300mV for the asymmetric transformers. For example with the symmetric transformer A1 the eye diagram with a 3.0Gbps data

stream results in a peak voltage of 262mV and an eye opening of 238mV. The asymmetric transformer C3 under the same conditions provides a peak voltage of 306mV and an eye opening of 298mV. At the slower data of 1.0Gbps, transformer A1 has a peak voltage of 262mV and an eye opening of 254mV, and transformer C3 has a peak voltage of 322mV and an eye opening of 306mV, and

With respect to Figure 75, the peak, measured eye diagram voltages are the same as those predicted by the step response of the extracted transformer models. Once the peak voltage is reached, the transformer response decays to zero volts before a subsequent data transition. ISI must therefore be avoided either by waiting until the response has sufficiently dissipated before sending a subsequent bit or by using circuit techniques to send a compensated pattern for each bit.

The responses of experiments C1 and C3 are not noticeably different in amplitude or eye opening in spite of the patterned ground shield under transformer C1. Similarly, the response of transformer C2 with a PSG is not different in amplitude or eye opening than A1 without a PSG. The transformers built from symmetric inductors (e.g. A1 and C2) exhibit slightly more attenuation than the transformers built from asymmetric inductors (e.g. C3 and C1). The cause for the additional loss of the transformers built with symmetric inductors is simply due to the fact that the inductances comprising the transformer are not as large as those comprising the asymmetric transformers.

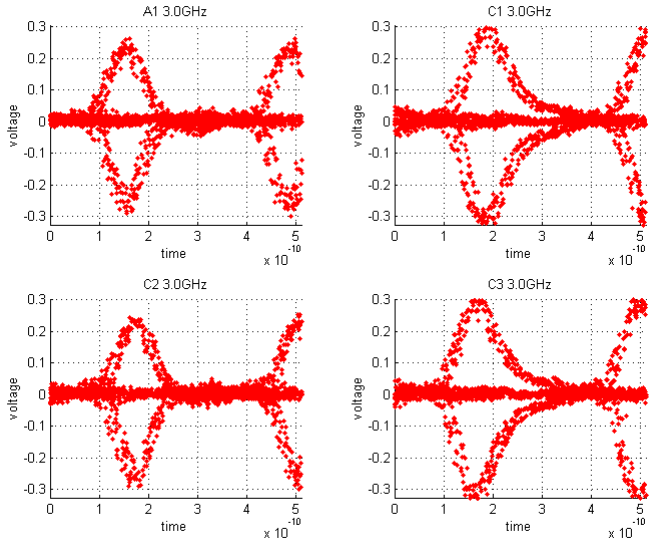


Figure 80 Measured eye diagrams for transformer experiments A1 and C1-C3 fabricated in the TSMC 0.35µm process subject to a 3.5Gbps NRZ, PRBS input signal

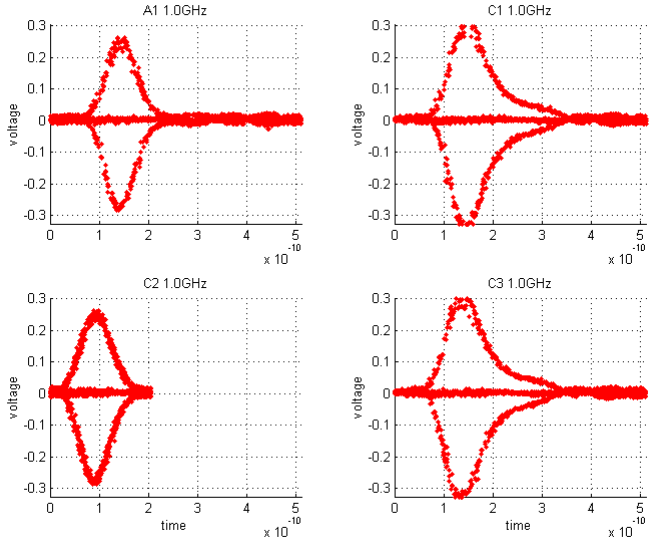


Figure 81 Measured eye diagrams for transformer experiments A1 and C1-C3 fabricated in the TSMC 0.35µm process subject to a 1.0Gbps NRZ, PRBS input signal

4.3.2.3 Alignment and Crosstalk

Several instantiations of transformers A1 and C3 have been fabricated with each instance having an increased lateral offset as reported in Table 12. Inductor B3 has also been instantiated numerous times to create neighboring inductors with increasing offset as reported in the same table. In both types of experiments, ASITIC predicts that coupling between inductors degrades quickly not just as a function of vertical offset as discussed in the previous section, but also as a function of lateral offset. Measured data confirms this prediction. Figure 82 shows the eye diagrams measured through experiments A1 – A4 by applying a 1V peak, 3.5Gbps NRZ pseudo random bit sequence to one terminal of the transformer and measuring the output voltage at the other terminal. Figure 83 shows the eye diagrams measured under the same experimental conditions for experiments C3 – C10 and Figure 84 shows the eye diagrams measured through experiments D6 – D10.

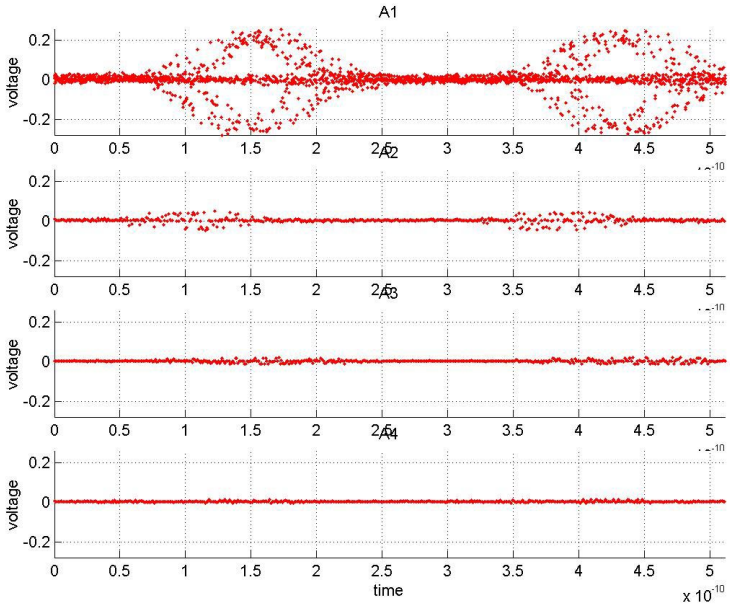


Figure 82 Measured eye diagrams for transformer alignment experiments A1 – A4 fabricated in the TSMC 0.35µm process subject to a 3.5Gbps NRZ, PRBS input signal

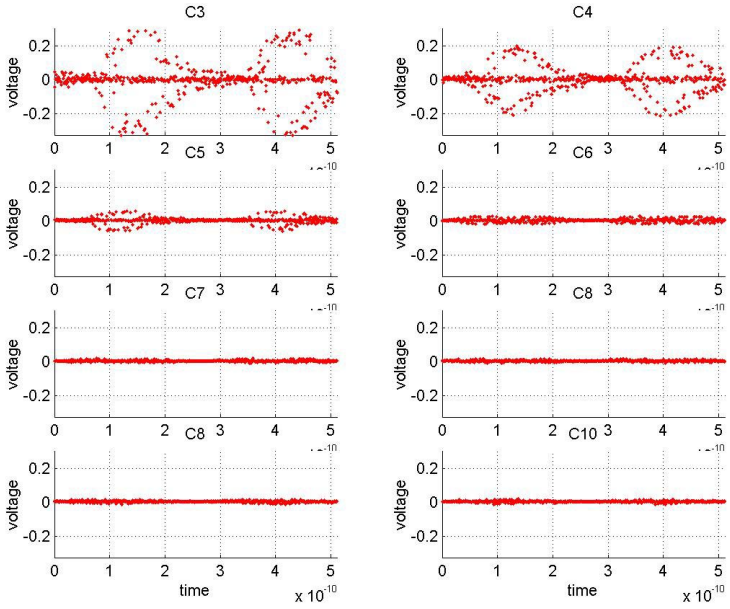


Figure 83 Measured eye diagrams for transformer alignment experiments C3 – C10 fabricated in the TSMC 0.35µm process subject to a 3.5Gbps NRZ, PRBS input signal

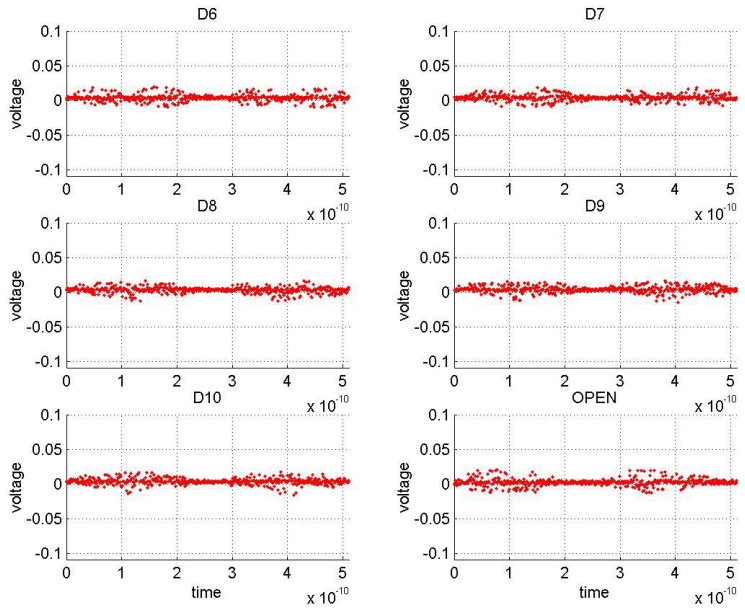


Figure 84 Measured eye diagrams for transformer crosstalk experiments D6 – D10 fabricated in the TSMC 0.35µm process subject to a 3.5Gbps NRZ, PRBS input signal

With zero lateral offset, the eye diagram from the symmetric transformer A1 with a 3.5Gbps pseudorandom, 1V input has a peak voltage ranging from 250mV to 258mV. The peak voltage degrades rapidly as lateral offset is introduced. For example, transformer A2 (which is the same as structure A1 except that the inductors are only overlapped by 50%), the peak voltage detected drops to 49mV with no detectable eye opening. Similarly, in structure A3 (with 9.4µm separating inductors and no overlap) the peak voltage drops to 20mV and in structure A4 (with 47.4µm separating inductors and no overlap) the peak voltage drops to 13mV.

The asymmetric transformer experiments C3-C10 offer finer granularity over offset than do A1-A4. Figure 85 shows the peak voltage as a function of offset for these 8 transformers. With almost zero overlap, the peak voltage coupled across the transformer is 302mV but this drops rapidly as the lateral offset is increased. By the time the transformer primary and secondary are separated by only 9.4µm (i.e. structure C7), the peak voltage is reduced to 18.2mV.

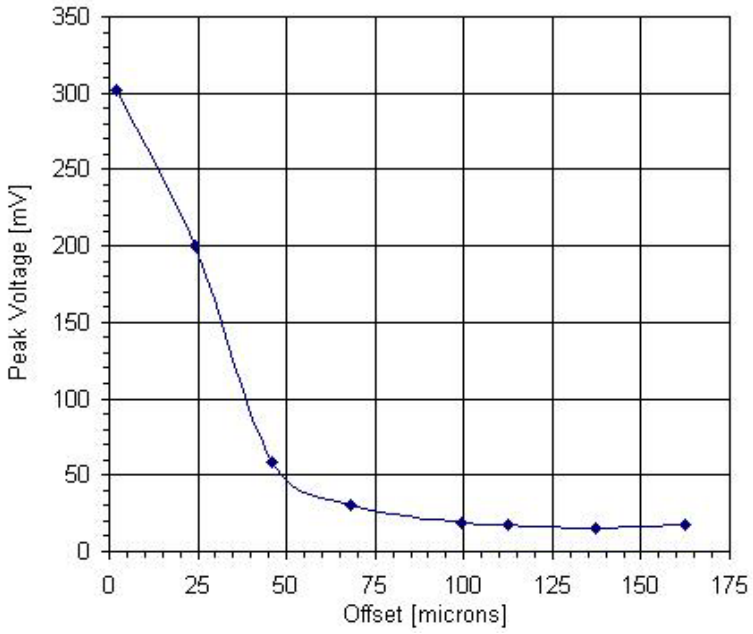


Figure 85 Measured peak voltage as a function of lateral offset for TSMC 0.35µm transformer alignment experiments C3 – C10

Similarly, neighboring inductors on the same metal level (i.e. D6 – D10) have little interference with each other even when the inductors are spaced as closely as 9.4µm as in design D6. The eye diagram for this experiment shows a peak, coupled voltage of 19.6mV. However, the graph in Figure 84 labeled 'OPEN' shows the response of the measurement system when no device is under test. Even in this case, the peak voltage measured is 20.7mV so the coupling between neighboring inductors is within the noise floor of the measurement system.

The coupled inductor model presented in the previous chapter does not yet take into account the effects of nearest neighbors. However, in an LCI system, coupled inductors must be placed such that interference from neighboring I/O does not cause unacceptable bit errors. The measurements presented here show that inductors separated by as little as 10% of their diameter have –24dB interference. The transformers and inductors in these experiments are in a nearly ideal environment with no underlying routing and no on-chip circuits injecting noise into the substrate. Work remains to be done to develop a predictive model for mutual coupling that takes these noise sources into account.

Chapter 5 Package Development

5.1 Overview

Dense chip-to-chip interconnections can be realized when capacitive or inductive AC coupled signaling is used with the physical interface presented in this chapter. A new packaging structure is needed because the requirements imposed by both DC and AC coupled connections cannot be met simultaneously by traditional packaging schemes. The packaging structure presented here accommodates the needs of each signaling methodology in order to create separate connection types for AC and DC signals across the same interface. DC connections require a direct, physical connection. Both capacitively-coupled and inductively-coupled AC signals require a small chip-substrate gap on the order of 1-10μm.

Two fabrication processes have been developed to demonstrate a physical technology to enable AC coupled interconnects. The development of and results from each process are presented. Finally, given the tolerances and physical parameters that can be realized, the implications upon the performance of AC coupled interconnections are discussed.

5.2 Packaging for AC Coupling

The proposed physical structure allows for both DC and AC coupled connections to exist across the same chip-substrate interface. DC connections are supported by means of solder bumps and AC coupled connections are supported as a direct result by which the solder bump connections are fabricated. That is, the solder bump connections are fabricated at the bottom of wells (or trenches) manufactured in the substrate. When an IC with solder bumps is mated to the substrate, the bumps are recessed below the surface of the substrate and the chip surface is brought into close proximity of the substrate. By nature of the controlled collapse of solder joining, the resulting gap is uniform and on the order of a few microns across the entire chip-substrate interface. This small but uniform gap allows two plates (e.g. one on the IC and a corresponding plate on the substrate) to form a coupling capacitor or two inductors (e.g. one on the IC and a corresponding plate on the substrate) to couple and form a transformer.

A top-down view of an IC and substrate before joining and a cross-section of a physical structure after joining are shown in Figure 86. Although only one IC is shown, the complete structure consists of multiple ICs and a common substrate. In practice an array of trenches is created in the substrate by using standard manufacturing processes. Solder bump landing pads are created at the base of each substrate trench. Routing layers allow DC voltages to be brought to the solder bumps and to allow interconnection between ICs via the AC coupling elements. A portion of each AC coupling element is fabricated on the uppermost metal level of the substrate

wherever AC interconnections to an IC are desired. VLSI chips can be created with any standard CMOS fabrication process. Pads for solder bumps should be fabricated on the top metal level of the chips where DC connections are desired between the chip and the substrate. The corresponding portion of each coupling element should be fabricated on the chip surface where AC coupled signals are needed. Overglass openings on the integrated circuits should be made only where solder bumps (i.e. DC connections) will be formed.

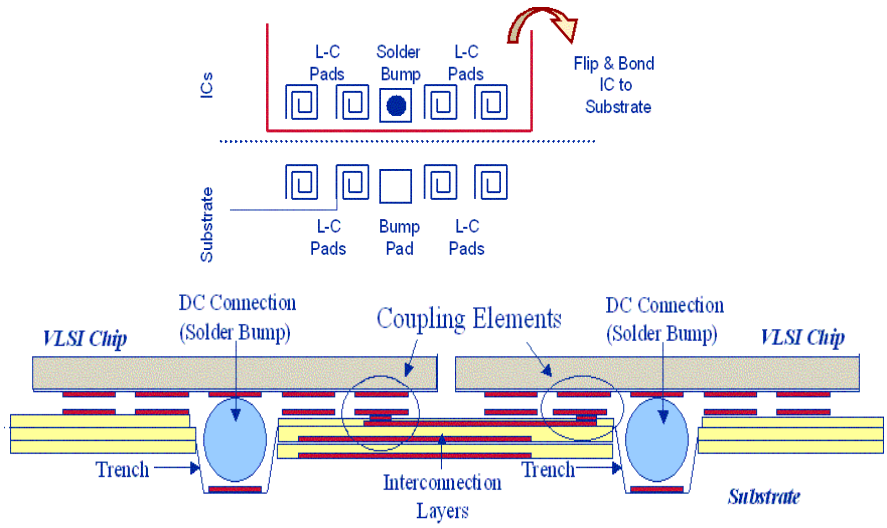


Figure 86: Top-down and side-view cross-sections of physical structure to support both buried solder bumps and AC coupled interconnections

Using this structure, a bumped chip can be positioned over the substrate so that the solder bumps will be recessed into the trenches and corresponding AC coupling elements aligned. As an advantage of this technique, the trench depth, solder ball size and pitch can be made as large as necessary to provide the required compliance. All the usual advantages of solder bump assembly, such as self-alignment, are still useful in this structure. Fabrication processes for the physical structure can be developed compatible with standard CMOS processing techniques and extendible to other package materials, including ceramics and plastics.

Packages present parasitics to on-chip and off-chip circuitry that should be taken into account during IC design and package selection [146]. However, packages can be designed specifically to enhance circuit performance by tailoring their parasitics [147]. Whether intentional or unintentional, IC designers should be aware of the impact upon electrical performance that can result from the choice of packaging.

The physical structure presented in Figure 86 can be viewed from the perspective of a circuit schematic as shown in Figure 87. For an LCI system, a transmitter circuit on one IC sends information into an on-chip inductor. This inductor is coupled to a second inductor on the substrate and this coupling causes the transmitted signal to

propagate along an interconnection on the substrate. The signal travels along the interconnection (possibly a transmission line) until it is coupled into a receiver circuit through a second chip-substrate transformer.

In a general AC coupled system, the package presents several benefits to the IC circuitry. The parasitic effects of bondwires and/or solder bumps of traditional packages are replaced on all AC signal paths by intentional coupling elements. Although the intentional insertion of coupling elements requires a new transceiver design to exploit the new package interface, the circuit topologies made possible by packaging for AC coupled interconnections promise to be low power and capable of supporting several thousand I/O per chip [18]. The proposed AC Coupled system also allows a dense array of power and ground connections to an IC, and this will help alleviate switching noise. Every AC signal will connect to the substrate at a point close to its origination. For buses of signals transferred off-chip, this will help manage skew by allowing all bus lines to be kept closely packed.

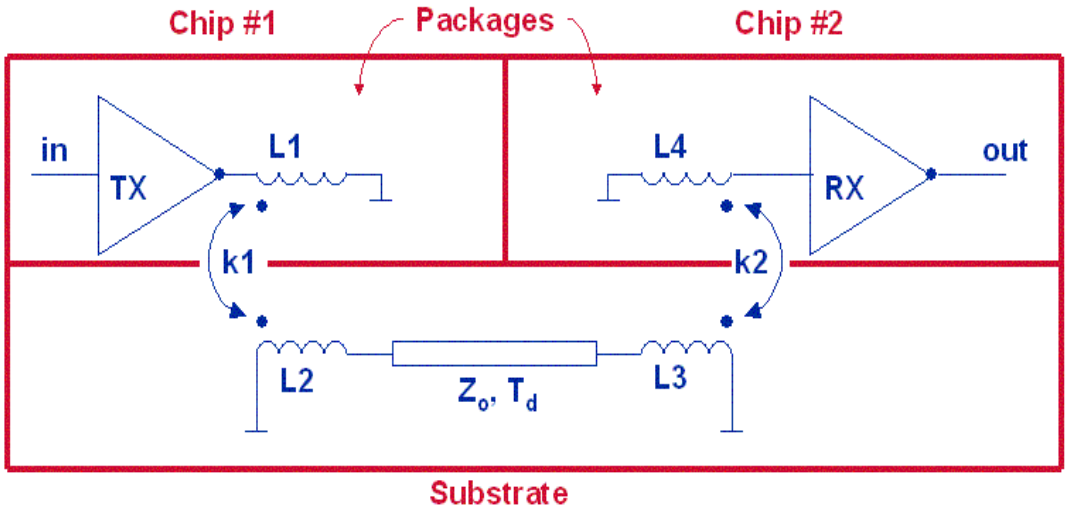


Figure 87 Circuit-level view of packaging structure

5.3 Fabrication Process Tradeoffs

In order to realize the benefits of AC coupling, several tradeoffs must be balanced to design a process for fabricating the physical system. Among the tradeoffs are the gap height uniformity across the IC / substrate interface and the trench design. Many parameters of the solder plating and reflow process must also be optimized. The fabrication process must be designed to enable the required element density and alignment and should be designed after careful consideration of the routing requirements for each DC and AC I/O. Also, the fabrication process must be developed in tandem with the design of the substrate transmission lines.

5.3.1 Gap Height Uniformity and Trench Design

The magnitude of the chip-substrate gap has a profound effect upon the performance of capacitive and inductive coupling elements. The performance of both capacitive and inductive coupling elements degrades quickly as gap height is increased. Numerically, capacitive coupling implementations require a gap height on the order of 1-2 μm that is uniform across the entire chip-substrate interface. Inductive coupling requires a gap height of less than about 5% of the inductor diameter.

Trenches for the solder bump connections can be fabricated in the substrate either as part of the substrate layer stackup or in a single etch process. The NCSU process (to be described shortly) provides an example of trench creation through a single etch step. In this process, silicon is used as a substrate material and trenches are created through bulk micromachining. However, for this process, the trench height becomes a function of a timed, wet etch so there can be significant trench depth variation between separate batches of substrates. The MCNC process (also to be described shortly) provides an example of trench creation as part of the substrate layer stack up. In this process, several layers are deposited and patterned as the substrate is fabricated, and patterning concentric vias of increasing diameter on each subsequent layer forms the trenches. With this type of process, both the thickness of each layer and the total height of all layers must be designed so that trenches of the correct depth can be fabricated.

In addition to the uniformity of the trench depth, the solder bumps must be of a consistent height. If either or both of these dimensions are not controlled then the chip-substrate gap after the ICs are joined to the substrate could be non-uniform. Gap height non-uniformity can degrade system performance. For example, the coupling between either capacitor plates or inductors is a strong function of the distance between corresponding elements. A non-uniform gap will cause variable coupling and therefore variable attenuation along the signal path.

5.3.2 Coupling Element Density

Multiple factors must be balanced to achieve a dense array of AC coupling elements. The constraints upon the fabrication process are more severe for inductive coupling than for capacitive coupling. The density of LC connections can be limited by the number of metal layers available in the fabrication process and by the design rule constraints imposed by the fabrication process.

Each inductive coupling element is composed of multiple turns so the minimum width and spacing supported by the fabrication process define the minimum space required to simply fabricate an inductor. For example, if a fabrication process can only support 10μm wide traces with 10μm spaces (i.e. 20μm pitch) then a 4-turn inductor will have an outer diameter of at least 150μm. In addition, LC connections require a via and a signal trace to

connect one terminal to ground and another via and signal trace is required to route the AC signal from the inductor output along the substrate to a second inductor. Large fabrication rules for vias (size and clearance) could cause the inductor inner diameter to increase simply to accommodate the space needed to connect to the inductor.

Coupling element density can be limited because of system electrical constraints or from an inability to fabricate and route signal lines to and from all of the coupling elements. For example, the performance specifications might require that physically large coupling elements be used in order to achieve to correct coupling capacitance or inductance in which case the area per coupling element will reduce I/O density. The density of both capacitively- and inductively-coupled arrays can be affected by the underlying routing from neighboring inductors and the number of available routing layers. For example, I/O density can be limited by routing problems if the substrate technology cannot support signal traces narrow enough to route all of the interconnections with the available routing layers. In such a case, either routing layers can be added to the substrate, the coupling element pitch could be increased to allow room between elements for routing, or the un-routable I/O can be eliminated.

5.3.3 Chip-Substrate Alignment

Achieving a prescribed I/O density can be complicated by the fact that the system performance and coupling element density are dependent both upon each other and the alignment tolerance between the substrate and chips. For example, inductive elements must be aligned with minimal offset in order to maximize coupling. Coupling through capacitive elements will also decrease due to misalignment since this type of coupling has a strong dependence upon the overlap area of the capacitor plates. Not only will chip-substrate misalignment increase attenuation through AC coupled channels, but also misalignment will bring neighboring elements closer to each other and thereby increase crosstalk between adjacent I/O. In both LCI and CCI systems, alignment can be controlled by appropriately sizing the trench (width and depth) and the solder bump landing pad.

5.3.4 Transmission Lines

The interconnections on the substrate must be designed to present the transmitter and receiver with a controlled-impedance while minimizing signal attenuation and dispersion. However, the electrical performance and physical dimensions of controlled impedance lines depends upon both the characteristics of the material from which the lines are made the surrounding environment. These relationships introduce a set of tradeoffs between I/O density, the substrate materials, and the substrate fabrication process. For example, once a set of substrate materials and the thickness of each layer are chosen, the geometry of the substrate transmission lines can be calculated to have the correct electrical characteristics. The geometry of the transmission lines must also be

chosen so that the specified I/O density can be achieved, but the transmission line dimensions cannot violate the design rules required by the process. However, the design rules of the substrate process cannot be chosen until the material set, thickness of each layer, and process flow is known.

5.4 NCSU Process

A fabrication processes using silicon substrates as a test vehicle has been developed in the NC State University cleanroom to prove the feasibility of joining a chip to a substrate with recessed solder bumps. The corresponding chips are fabricated by MCNC-RDI, a partnering research institute located in Research Triangle Park, NC.

5.4.1 Process Flow

The substrate fabrication process developed for the NCSU cleanroom consists of four photolithographic mask levels and Table 20 lists the sequence of fabrication steps. The solder bump trenches in this process are created in a single step by bulk etching the silicon substrate. Tetramethyl ammonium hydroxide TMAH is used as the etchant. Since TMAH is commonly used as a photoresist developer, a hard mask is needed to preserve the pattern of trench locations during the trench etch. The first process sequence is therefore the deposition and patterning of a thermal oxide film to define the locations of the solder bump trenches. The trenches are then formed through a bulk, anisotropic etch in TMAH at 85°C. This etch is preferential to the {111} planes resulting in a trench sidewall on <100> oriented silicon wafers of 54.7°.

Table 20 NCSU cleanroom substrate process flow

Process Step	Description
Hard mask deposition and patterning	Deposit 1300Å thermal oxide and pattern with darkfield mask to define locations of solder bump trenches
Solder bump trench creation	TMAH etch at 85° for 60min to form ~30μm deep trenches
Isolation oxide deposition	Deposit 5000Å thermal oxide to isolate adjacent trenches from substrate
Interconnect metal deposition and patterning	Deposit 2000Å aluminum and pattern interconnections
Inter-level dielectric deposition and patterning	Deposit and pattern 3000Å LTO to isolate interconnect metal and UBM
UBM deposition and patterning	Deposit and pattern 1000Å Ti, 7500Å Cu to form solder bump landing pads at the base of each trench

Since the bulk silicon substrate is conductive, a thermal oxide layer is deposited after the bulk etch to electrically isolate adjacent trenches from each other. This step is followed by the deposition of 2000Å of aluminum, and the aluminum is patterned to provide an interconnection layer within the various experiments on the substrate. The

interconnection layer is passivated with 3000Å of low-temperature oxide (LTO) and vias are formed in this dielectric where contacts will be made to the subsequent metal layer. Finally, the underbump metallurgy (1000Å Ti and 7500Å Cu) for the solder bumps is deposited and patterned in the base of each trench.

5.4.2 Experimental Design

The depth of the trenches in the prototype physical structure is designed to be 30μm, which is slightly less than the anticipated height of a reflowed solder bump. In this way the solder bumps pull the chip toward the substrate during the reflow process and define a fixed gap between the surfaces of the chip and substrate.

With the given trench creation process, the desired trench depth constrains the drawn width of the top of the trench and this sets the minimum pitch between adjacent trenches. That is, since the silicon crystalline planes fix the trench sidewalls at slope of 54.7° the width at the top of the trench must be at least 1.4× (i.e. $\sqrt{2}$ times) the depth of the trench. This factor of 1.4× is valid for a fully etched trench – i.e. a trench that is etched until it is completely bound by the silicon {111} planes as shown in Figure 88. In order to include room at the base of the trench for the solder bump landing pad, the drawn trench width must be increased.

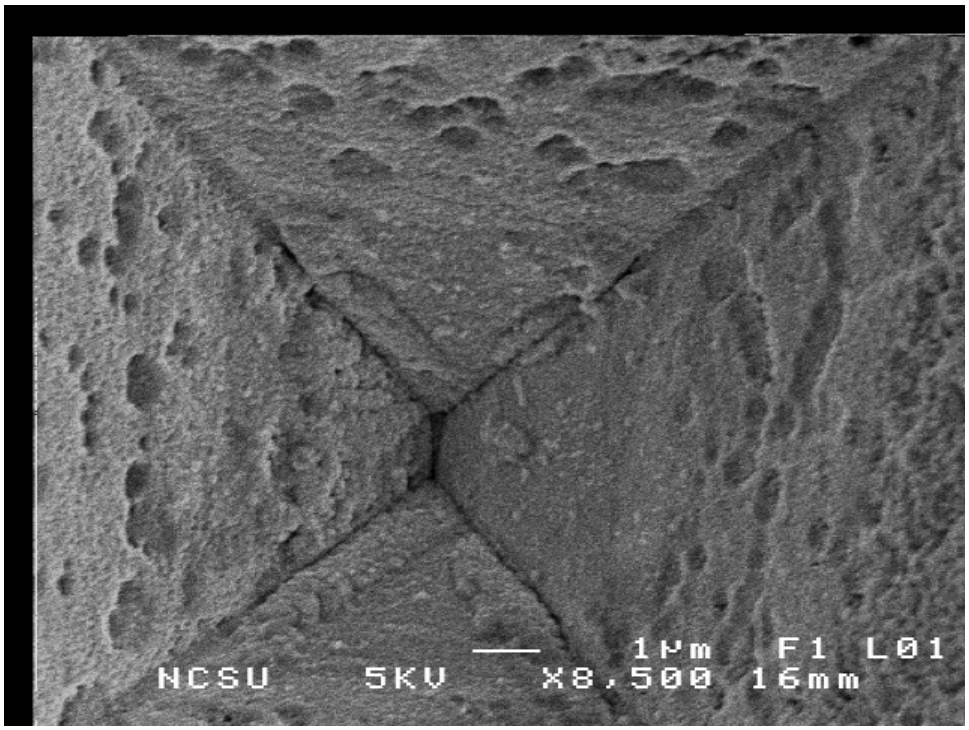


Figure 88 Fully etched trench in (100) silicon wafer

Several arrays of solder bump trenches have been designed where the pitch of trenches and the size of the solder bump landing pads at the trench base is varied between experiments. Specifically, the solder bump landing pad is designed as either 40µm or 80µm wide. The trench arrays with 40µm landing pads are designed with a pitch of either 116µm or 156µm. The trench arrays with 80µm landing pads are designed with a pitch of either 252µm or 316µm. Since the width of the landing pad directly impacts the achievable solder bump pitch, the trenches with a 40µm landing pads are designed for a higher pitch than the 80µm landing pad.

Figure 89 shows a layout of a daisy chain structure representative of the solder bump experiments. In this figure, the red squares are the footprints of the trenches at the surface of the substrate. The blue squares and connected lines are designed on the aluminum routing layer to provide connections between pairs of adjacent trenches. The smaller magenta squares within the routing layer at the trench bases are solder bump landing pads. The green lines represent the routing layer and solder pads on the ICs that will be joined with the substrate. Once joined, continuous connections are formed along columns of the structure and these columns are designed for electrical probing to ensure continuity of the alternating substrate-to-chip connections.

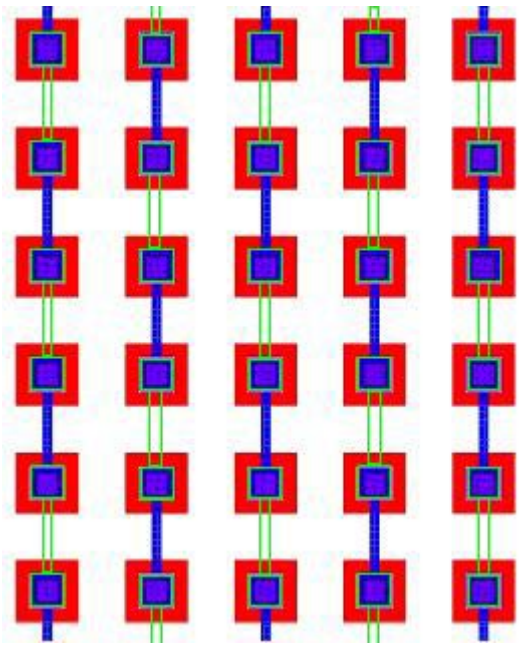


Figure 89 Snapshot of layout representative of test structures for NCSU substrate fabrication process

5.4.3 Results

The substrates fabricated in the NCSU cleanroom have a wide variation in final trench depth ranging from 22μm to 26μm. Of the six wafers processed, sample 'SEM3' provides the most consistent trench depth of approximately 26μm. SEM images have been taken of joined chip-substrate pairs. Figure 90 is an SEM image of a joined chip-substrate pair that has a 30 × 30 array of 26μm deep trenches, 80μm bump pads, and 31μm tall electroplated solder bumps. This image is taken from the center of the chip-substrate pair. The gap is observed to be uniform across the entire edge of the chip-substrate joint and is measured from the acquired image to be 7.25μm ± 0.07μm (where the margin of error is taken as the per-pixel resolution of the image).

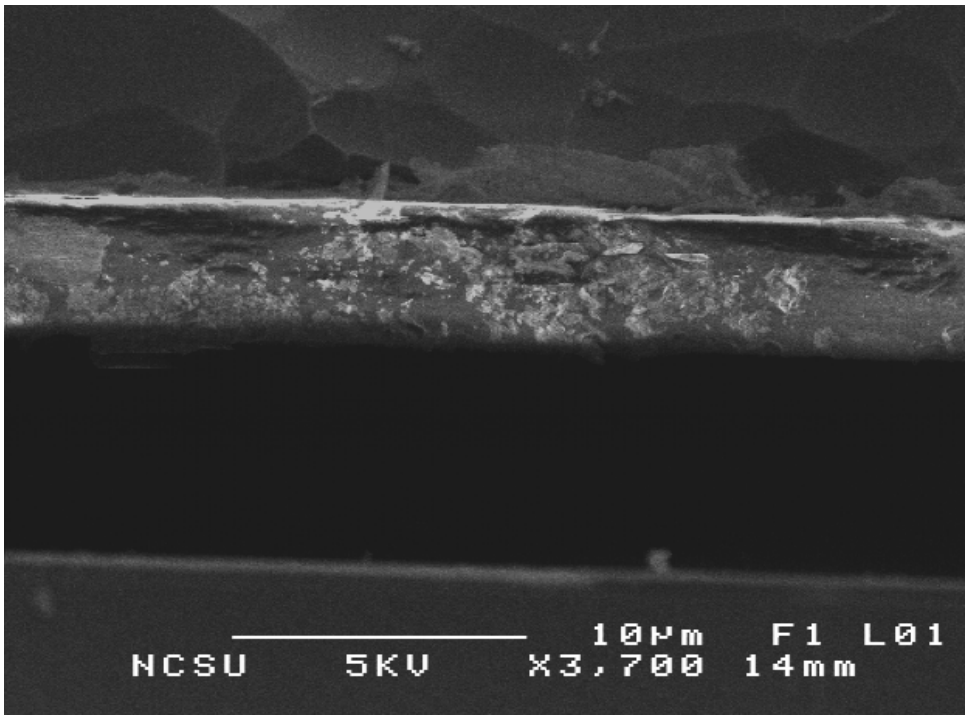


Figure 90 Side view of joined chip and substrate with uniform 7μm gap

Tensile pull tests have been performed on several joined chips and substrates and it is found that the joints can withstand a pull between 50 to 70 pounds before tearing apart. Figure 91 is an image of a section of a substrate after separation from a pull test. Although the complete array of solder bumps is not shown in the image, it is observed that all of the solder bumps across the substrate are successfully joined. It is also observed that the alignment of the chip and substrate is moved slightly off-center. This alignment can be improved by optimizing the trench size and both the solder bump and joining processes.

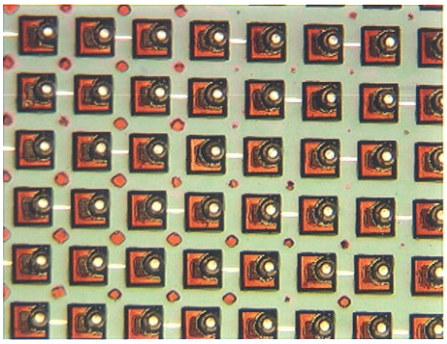


Figure 91 Top-down photograph of substrate after joining and separation demonstrating 100% solder bump yield

The fabrication of the silicon substrates suffers from processing problems that prevent exhaustive data from being collected. For example, the solder bump trenches are deep enough that photoresist coverage problems occur around the perimeters of the trenches during the photolithography process. The photoresist tends to pool near the bottoms of the trenches and thin along the upper edges. Although the photoresist at the top of the trenches is needed to protect the aluminum routing layer running from the substrate surface into the trench, the thinned photoresist is unable to withstand the subsequent processing and results in total yield loss of the routing layer over the edge of the trenches. This effect is best illustrated by the test structure shown in Figure 92. The test structure shown in this figure is designed to yield a single trench 350µm long and 150µm wide overlapped 50% by a metal plate of the same size. Instead, due to the thinned photoresist at the top of the trench, the metal plate is broken along the entire upper edge of the trench and remains only at the trench base and some distance beyond the trench edge.

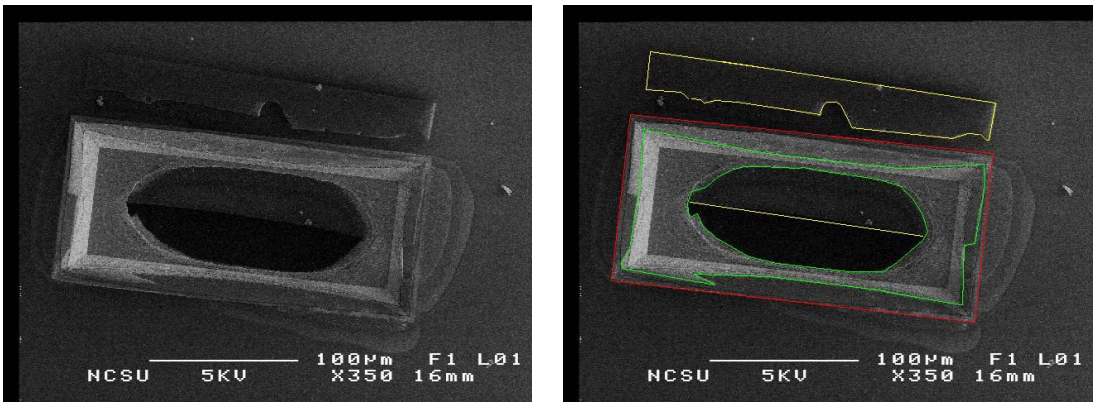


Figure 92 NCSU substrate test structure showing yield loss of metal routing layer over edge of trench feature
(left) unedited SEM image
(right) edited SEM image where trench feature is outlined in red, metal feature is outlined in yellow, and remnant of subsequent photoresist is outlined in green

The test structure shown in Figure 92 is not immune to subsequent processing since it exists on a wafer with experiments utilizing all process layers. The image shown here is taken after the entire 4-layer process is completed and as such, the effects of subsequent processing can be seen. The right side of the figure outlines the various layers comprising the image. The fabricated trench feature is outlined in red; the metal plate is outlined in yellow; and the remnant of photoresist from subsequent process steps is outlined in green. Focusing on the photoresist, the image clearly shows how after developing, the photoresist is absent around the entire perimeter of the trench yet is still pooled along the lower portion of the trench.

The impact of the trench depth upon the photoresist has resulted in 100% yield loss of the routing layer over the edges of the trenches. Since this routing layer is needed to connect solder bump landing pads to electrical probe pads no electrical data can be collected from these experiments. In order to mitigate this problem, a lift off process could be used to pattern features that must traverse the edge of the trench. Alternatively, the trenches can be built as part of the layer stackup so connections at the base of the trench are possible and the need to route metal along the sidewall of the trench is alleviated.

However, this set of experiments has shown that solder bumps can be bonded successfully into recessed trenches and that this bonding methodology can lead to controlled chip-substrate stand-offs.

5.5 MCNC Process

A second fabrication process using silicon substrates as a test vehicle is being developed in conjunction with MCNC. This process is being designed to overcome the challenges uncovered by its predecessor and will be used to create substrates for exhaustively testing ICs fabricated with active CCI and LCI transceivers. In the first round of process development, work is being done to understand tolerances on the chosen substrate process, to create models of the substrate routing and to understand the limits on interconnect density.

5.5.1 Modeling

Transmission line performance can be measured with several metrics such as characteristic impedance, delay and attenuation. Each of these parameters is dependent upon the physical geometry of the transmission line and the material in which the line is embedded. Figure 93 shows the geometric and material parameters that are important for designing transmission lines. In this figure, two adjacent lines are shown and ‘w’ is the width of the transmission line conductor, ‘s’ is the space between adjacent lines, ‘t’ is the thickness of the conductors, ‘ρ’ is the conductivity of the conductors, ‘ε_r’ is the relative dielectric constant of the material surrounding the transmission lines, and ‘h’ is the height of the conductors above a ground plane. The figure represents a ground

plane both above and below the two transmission lines by the thick, red lines at the top and bottom of the image. However, ground planes may not encapsulate embedded transmission lines so closely.

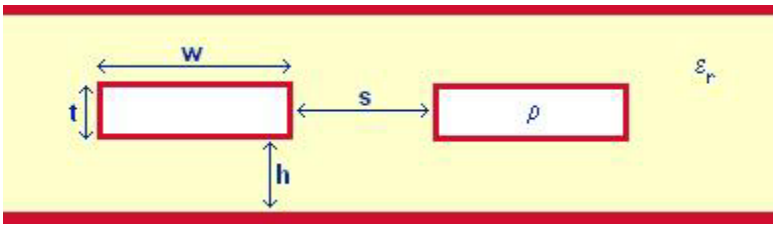


Figure 93 Critical parameters for design of embedded transmission lines

Given the numerous variables (e.g. w, s, h, t, ε_r, and ρ), there are many ways to physically build 50Ω, controlled impedance transmission lines, and Figure 94 shows cross-sections of three possible structures. The triplate structure developed by Ho, et al at IBM employs two routing layers encapsulated by two ground planes. These lines fabricated from copper and embedded in polyimide require large aspect ratios to achieve low loss and controlled impedance [89]. The coplanar waveguide and microstrip configurations shown in Figure 94 have been derived from 3D electromagnetic simulations with HFSS. In all cases, copper is the chosen interconnect metal since its advantages over aluminum are well known. The coplanar waveguide (CPW) structure can be routed independently of a dedicated ground plane, but to achieve a high interconnection pitch the ground conductors must be made narrow. Similarly, the triplate structure can achieve high line density but requires very thick and narrow metal conductors. Due to fabrication constraints, the microstrip structure has been chosen for implementation in the MCNC process over the CPW and triplate structures since its 15μm minimum feature size will allow for more relaxed photolithography tolerances than the other structures.

Looking at the analysis process in more detail, results from the HFSS simulations for isolated microstrip lines are shown in Figure 95. The simulations have been done for discrete configurations varying dielectric thickness, conductor width and dielectric constant between simulations. The graph shows that for a given conductor width, if the dielectric constant of the material surrounding the line is increased, then the line must be moved further from its ground plane to maintain a 50Ω impedance. Alternatively, for a fixed height above the ground plane, the line width must shrink as the dielectric constant of the material surrounding the line is increased.

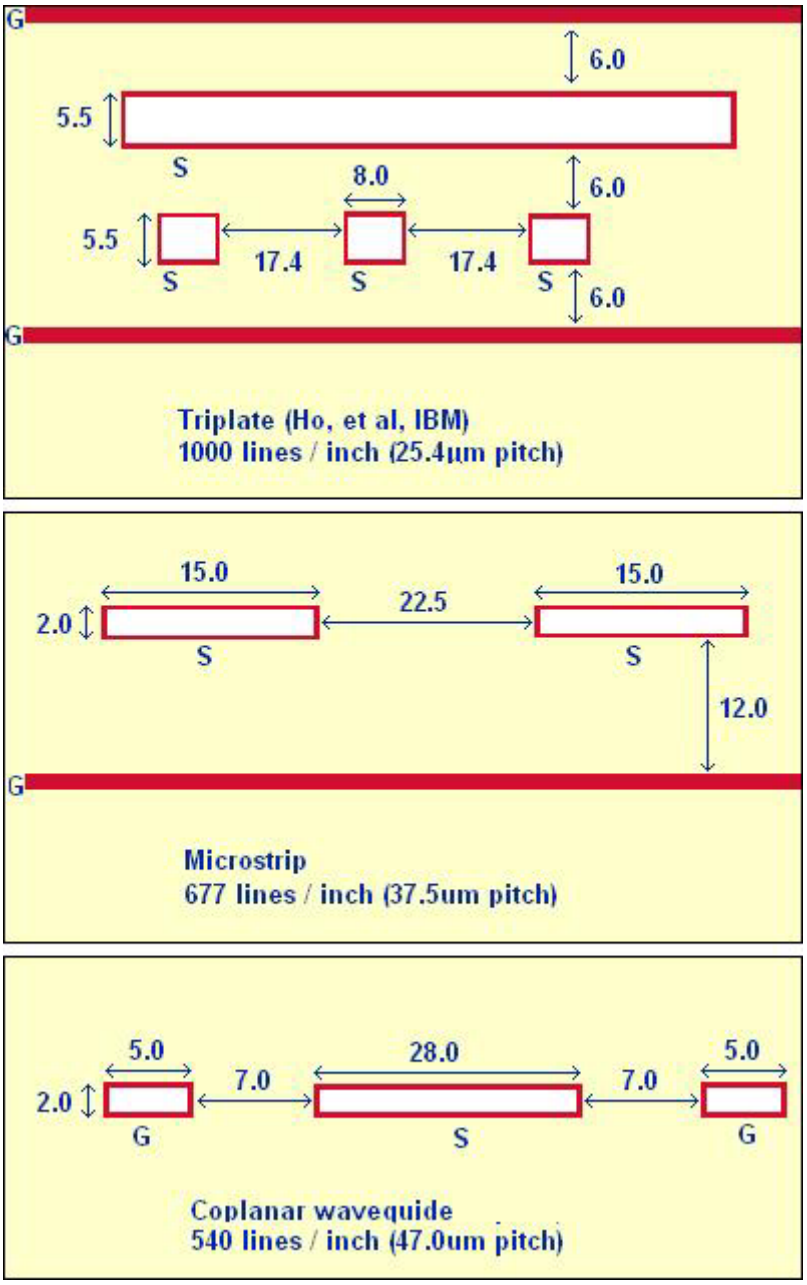


Figure 94 Possible configurations for transmission lines with a 50Ω characteristic impedance
(top)triplate structure requiring 4 metal levels
(middle) microstrip structure requiring 2 metal levels
(bottom) coplanar waveguide structure requiring 1 metal level

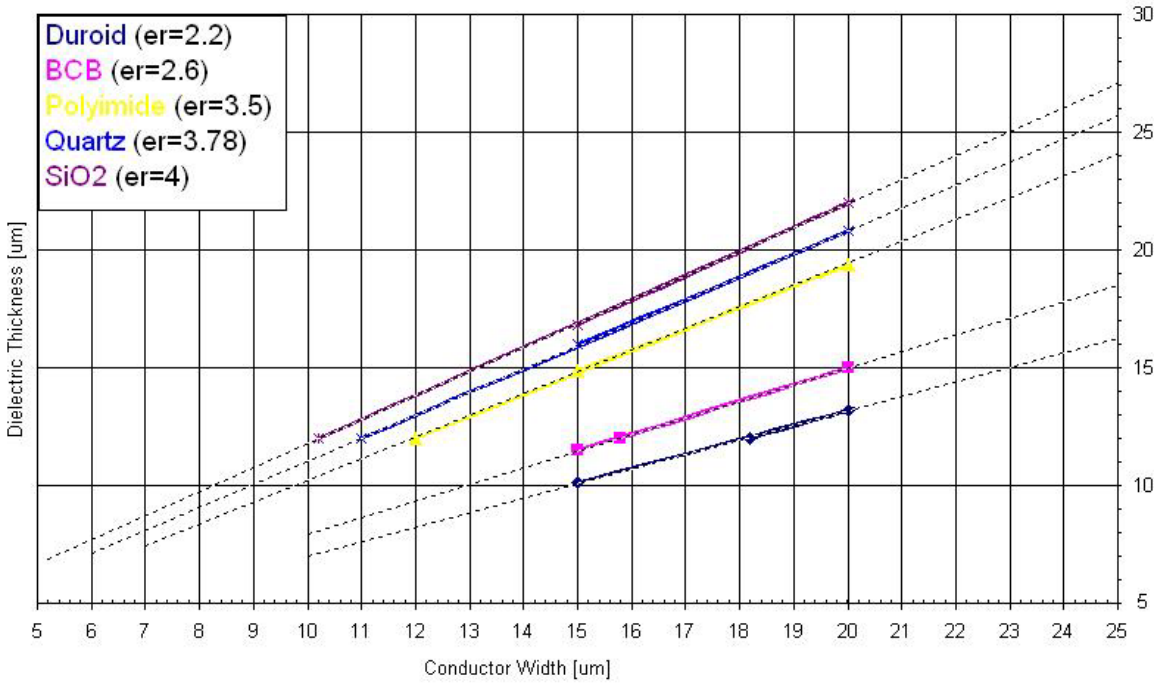


Figure 95 HFSS simulation results of dielectric thickness versus conductor width for 50Ω buried microstrip lines

A tradeoff therefore exists between dielectric thickness (i.e. which sets the distance between a microstrip line and its ground plane) and transmission line width. Materials with large dielectric constants allow for thin layers separating the line and the ground plane but require narrow lines to achieve 50Ω impedance. Narrow lines however suffer from large resistive losses. Thus, the choice between dielectric thickness and line width must be balanced with the expected attenuation over a prescribed length of line. For example, Figure 96 shows the attenuation in dB of four specific transmission line geometries as a function of frequency. Two of the transmission lines in the figure are embedded within polyimide and the other two are embedded in BCB. In polyimide, the width of the line must be approximately equal to the height of the line above the ground plane to achieve a 50Ω characteristic impedance. The two line configurations shown in the graph are for W=15μm / H=16μm and W=20μm / H=20μm. In the former case, Z_O is 51.9Ω and the attenuation is –9.12dB/10cm at 10.5GHz, and in the latter case, Zo is 50.8Ω and the attenuation is -7.44dB/10cm at 10.5GHz. In BCB, the transmission line can be moved closer to the ground plane compared to a line with the same width in polyimide. The two BCB line configurations shown in the graph are for W=15μm / H=12μm and W=20μm / H=16μm. In the former case, Z_O is 51.3Ω and the attenuation is –9.44dB/10cm at 10.5GHz, and in the latter case, Zo is 52.0Ω and the attenuation is -7.42dB/10cm at 10.5GHz. Thus for a given line width, thinner dielectric layers can be used with little to no impact upon signal attenuation if BCB is chosen as the dielectric material rather than polyimide.

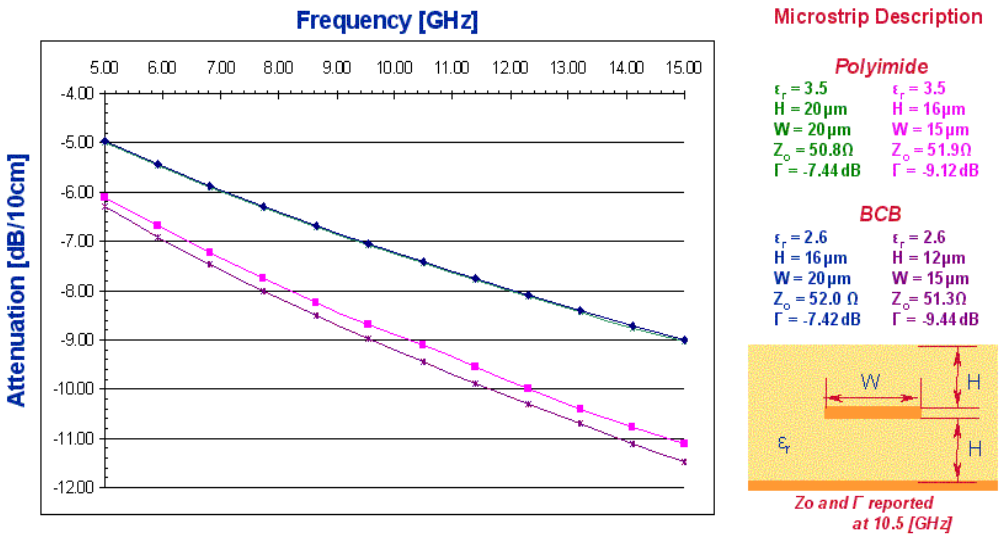


Figure 96 HFSS simulation results of attenuation for embedded microstrip lines versus dielectric and geometry

The choice between dielectric thickness and line width must also be balanced by fabrication constraints. For example, in the MCNC process the vias between layers will not be backfilled with metal and planarized as is common in commercial CMOS processes. Thicker dielectric layers will create processing challenges with respect to achieving continuity of metal lines in via features and therefore between metal levels. From a fabrication perspective thinner dielectric layers are preferable, but of course this will require narrower (and more lossy) transmission lines to maintain 50Ω impedance.

The preceding discussion has been with respect to isolated microstrip lines. However, to route all of the I/O in a densely packed array of AC Coupled interconnections, the transmission lines will have to be closely spaced. The characteristic impedance of a transmission line will drop as neighboring lines are brought closer. HFSS simulations show that the characteristic impedance of a 15µm wide microstrip line placed 12µm above its ground plane and embedded in BCB will remain 50Ω as long as the distance to its nearest neighbor is ≥ 22.5µm – which is the microstrip geometry shown in Figure 94.

5.5.2 Process Flow

The substrate fabrication process being developed at MCNC consists of five metal layers and four dielectric layers. A cross-section of the entire stackup is shown in Figure 97. The first two metal layers (M1 and M2) are intended to be used as the power and ground planes. These two layers will be inter-woven to form a dense mesh of power and ground connections and will also provide the landing pads for the recessed solder bumps. The third

and fourth metal layers (M3 and M4) are to be used for signal routing and the top layer metal (M5) will be used for coupling element fabrication. BCB is used for every dielectric layer (D1 – D4).

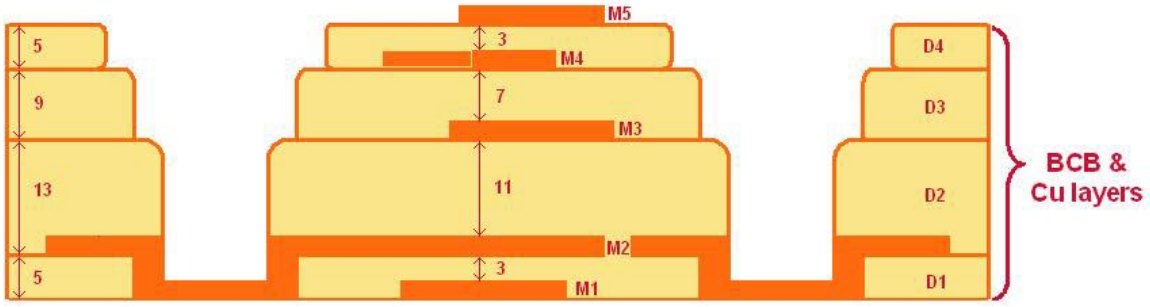


Figure 97 Cross-section of layer stackup for MCNC substrate process

Unlike the NCSU process in which the solder bump trenches are created by a single bulk etch, substrates fabricated with this process will have trenches created as a result of the layer stackup. That is, concentric vias of increasing diameter will be fabricated on subsequent layers so that the final structure will have a via from the top of the substrate to a solder bump landing pad on either metal level 1 or 2. The total distance from the top of the first metal layer to the top of the substrate will be 32µm, and the total distance from the top of the second metal layer to the top of the substrate will be 27µm. Solder bumps fabricated on ICs to be joined to these substrates can have a post-reflow height of 33-35µm if connecting to landing pads on metal 1. Or, the solder bumps can have a post-reflow height of 28-30µm if connecting to landing pads on metal 2. The precise tolerance in solder bump height depends upon the constraint placed upon the chip-substrate gap by the coupling method (capacitive or inductive) to be implemented between the chip and substrate.

5.5.3 Experimental Design

Isolated (single-ended) and coupled (differential) lines of varying length and width have been designed on both metal levels 3 and 4. The transmission lines on metal level 3 are designed with widths from 6µm to 24µm in steps of 3µm. The transmission lines on metal level 4 are designed with widths from 10µm to 46µm in steps of 6µm. All transmission lines are available in lengths of 49.866mm, 24.666mm, 16.232mm and 12.076mm.

Since the tolerances of the designed substrate fabrication are not yet known, the transmission line experiments are fabricated in a short-flow version of the process described in the previous section. This process consists of dielectric layers D2, D3 and D4; metal levels M2, M3 and M4; and the vias between each of these levels.

This first-pass at implementing the designed substrate process will accomplish two goals. First, the transmission line experiments will provide data to calibrate transmission line simulations against measured results. Secondly, test structures will allow the process limits on minimum feature sizes to be determined and from this estimates on the supportable I/O density can be made.

5.5.4 Transmission Line Results

The DC resistances of the isolated transmission lines on levels M3 and M4 are reported in Table 21. As expected, narrow lines are more resistive than wider lines and even with thick copper layers, the narrow lines have large DC resistance. The DC resistance measurements are shown graphically in Figure 98.

Table 21 DC Resistance of isolated microstrip transmission lines on metal levels 3 & 4
Measurement data from wafer #11

Metal 3			Metal 4		
Line Width [μm]	Resistance [Ω] (49.9mm length)	Resistance [Ω] (24.7mm length)	Line Width [μm]	Resistance [Ω] (49.9mm length)	Resistance [Ω] (24.7mm length)
6	30.6	60.9	10	18.7	36.7
9	21.2	41.7	16	12.3	23.6
12	16.5	31.9	22	9.4	17.6
15	13.5	25.9	28	7.5	14.1
18	11.4	22.0	34	6.4	11.8
21	10.0	19.0	40	5.7	10.2
24	8.8	17.7	46	5.1	9

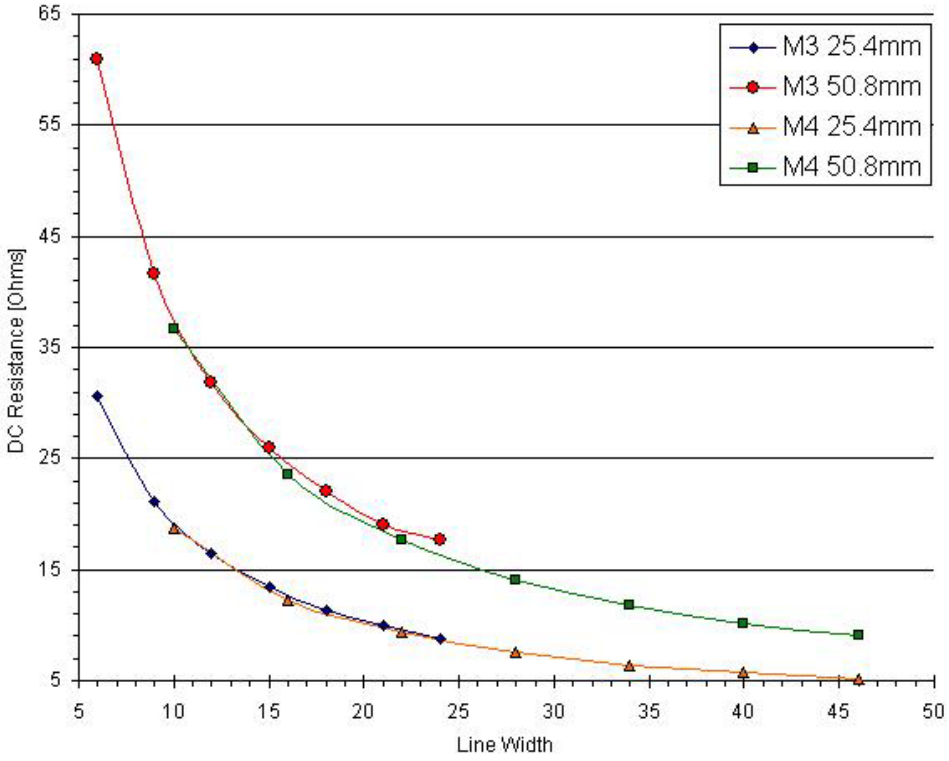


Figure 98 Plot of DC resistance measurements of isolated microstrip transmission lines on metal levels 3 & 4
Measurement data from wafer #11

TDR measurements on the transmission lines allow the characteristic impedance of the lines to be extracted. Figure 100 shows representative TDR data taken for varying lines widths of the 24.7mm long transmission lines on metal 3. The data in the graph have been converted from reflection coefficients to resistances with the identity shown in Equation 8 where Γ is the measured reflection coefficient and Z_O is the impedance of the measurement environment – which in this case is 50Ω. The step at approximately 0.14ns indicates the point at which the TDR pulse encounters the transmission line. The height of the initial step reveals the characteristic impedance of the line. The difference between the initial step and the peak value (which occurs at approximately 0.39ns for each line) corresponds to the DC resistance of the line. The TDR response eventually settles to the sum of the load impedance and DC resistance of the line.

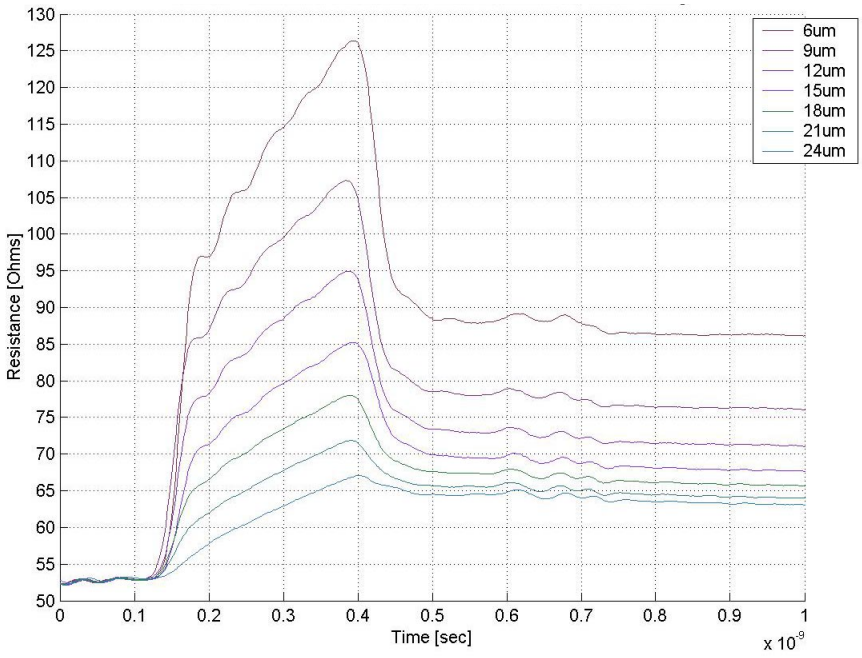


Figure 99 TDR measurements of MCNC wafer #15, metal 3 transmission lines
Transmission lines are 24.7mm long and the width is varied from 6μm to 21 μm in 3μm increments

$$R = Z_O\left(\frac{1+\Gamma}{1-\Gamma}\right)$$

Equation 8 Relationship between resistance and reflection coefficient measured by TDR

The characteristic impedance for the metal 3 transmission lines is extracted from the TDR measurements and plotted in Figure 100 as a function of line width. As expected, the data can be fit by a logarithmic equation [148]. The equation is plotted in the figure and listed explicitly in Equation 9.

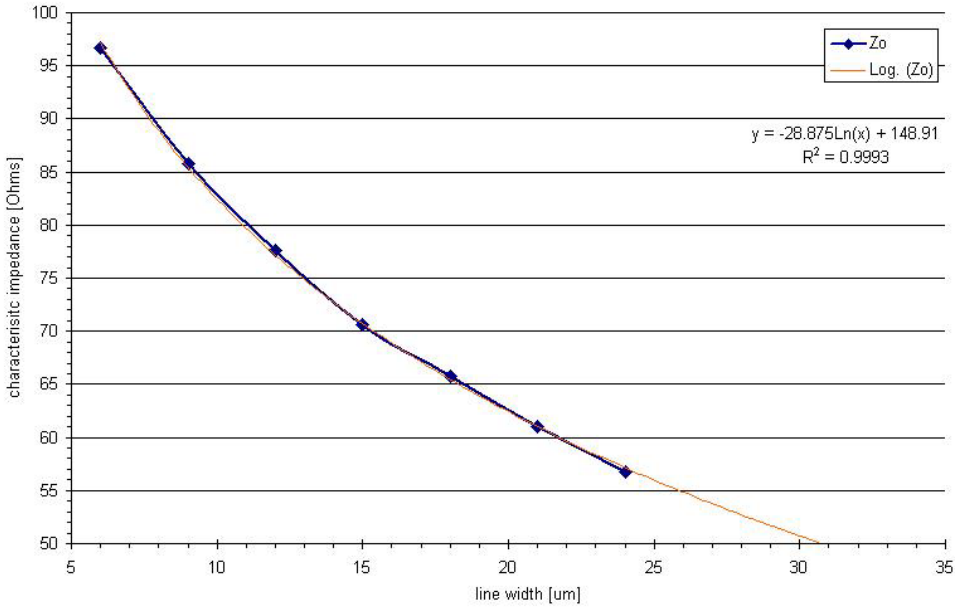


Figure 100 Metal 3 transmission line characteristic impedance versus line width

$$R = -28.875\ln(W) + 148.91$$

Equation 9 Equation fit to extracted characteristic impedance of M3 transmission lines on MCNC substrate #11

Comparing the extracted data against the HFSS simulations, the extracted characteristic impedance of the 15μm wide microstrip line embedded in 12μm BCB is much greater than that predicted by HFSS, but there are many possible causes for this variance. The most likely sources of the discrepancy are variations in the actual transmission line geometry and material parameters compared to the ideal simulated structure. For example, the simulated transmission lines are driven directly, but vias are present in the actual structure. The vias are small enough that they cannot be resolved within the sample time of the TDR instrument but their presence will change the capacitance of the line and hence its characteristic impedance. The measured impedance will also differ from the simulated impedance if the fabricated dimensions do not match the drawn dimensions or if the actual dielectric constant of the as-deposited BCB film does not match the assumed value of 2.65. For example, if the dielectric on the measured wafer is thicker than designed, then the measured characteristic impedance will be higher than intended. Also, if the transmission lines are narrower than drawn, the characteristic impedance will be higher than expected. It so happens that during processing, the BCB does not coat the substrates uniformly and the copper from which the transmission lines are patterned also does not cover the wafers uniformly. Instead thickness variations exist for both of these materials across the substrates. As a result, variations from the

designed transmission line characteristic impedance are to be expected. Dielectric and metal thickness variations of two substrates are detailed in Table 22.

Table 22 Variations of BCB and copper thickness across substrates
Measurement data from wafers #9 and #13, courtesy MCNC-RDI

Substrate	Measurement Location	BCB 2 (μm) (Level 1)	Metal 3 (μm) (Ti, Cu)	BCB 3 (μm) (Level 2)	Metal 4 (μm) (Ti, Cu)
Wafer #9	Center	13.4	2.5	6.9	2.0
	Middle	10.9	2.0	5.9	2.0
	Edge	9.3	2.2	5.3	1.8
Wafer #13	Center	12.5	2.3	8.5	2.8
	Middle	11.4	2.5	7.9	2.9
	Edge	10.1	2.6	6.6	2.6

HFSS simulations must not neglect the presence of vias because the impact of these features upon the transmission line impedance cannot be de-embedded from TDR measurements. However, a design equation has been fit almost perfectly to the measured data for transmission lines on the M3 routing layer. Future simulations and substrate designs can be compared against this design equation to ensure the characteristic impedance of the fabricated line more closely matches the intended value. In addition, effort must be made in the fabrication process to tightly control the thickness and uniformity of each layer so that the resulting structures yield the expected electrical characteristics.

5.5.5 Process Limits and Density

From the test structures available in the first round of substrates fabricated with the MCNC process, the minimum line size for future processes will be 5μm on a 10μm pitch. Figure 101 shows the inductance values that can be achieved for both 1- and 2-layer spiral inductors fabricated with these constraints. In the figure, the diameters of the inductors are 80μm, 90μm, or 100μm as indicated in the legend. The 1-layer spirals are wound on a single metal level and have a via connecting the center point to underlying routing. The 2-layer spirals have windings on two metal levels where the spiral is wound into the center on one level, transferred through a via to a second level and the wound back out from the center on the second level. As the figure demonstrates, a multi-level spiral inductor can achieve higher inductances in the same area than a single-layer inductor. Moreover, the figure shows that even with large metal width and spacing rules, inductances of almost 4nH can be realized and this is enough inductance to enable LC coupled interconnections.

The 2-layer inductor geometry is difficult to visualize so for clarity, example layout in 3-D perspective of a single-layer and a two-layer inductor is shown in Figure 102. The single-layer inductor corresponds to the data

point for 4 turns on the curve “D=100, 1 layer” in Figure 101. The two-layer inductor corresponds to the data point for 4 turns on the curve “D=100, 2 layers” in Figure 101. The yellow windings for both inductors are intended for fabrication on M5 of the MCNC process and the orange features are intended for fabrication on M4. The circular feature connecting M5 and M4 is a 10μm via, which is the minimum via size allowed to connect these two layers.

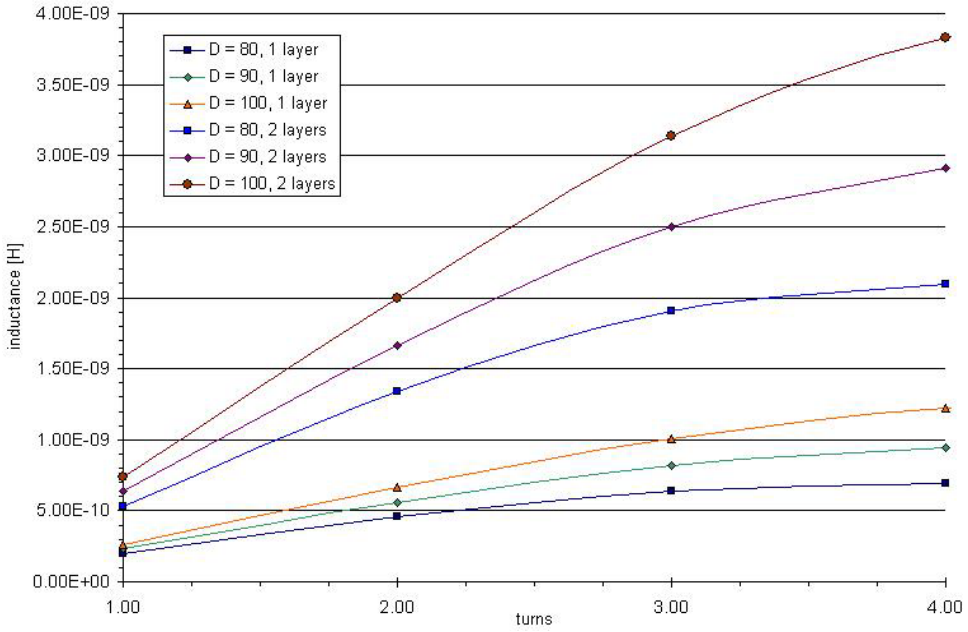


Figure 101 Inductance values achievable with MCNC substrate process as a function of inductor diameter and the number of metal levels containing spiral windings

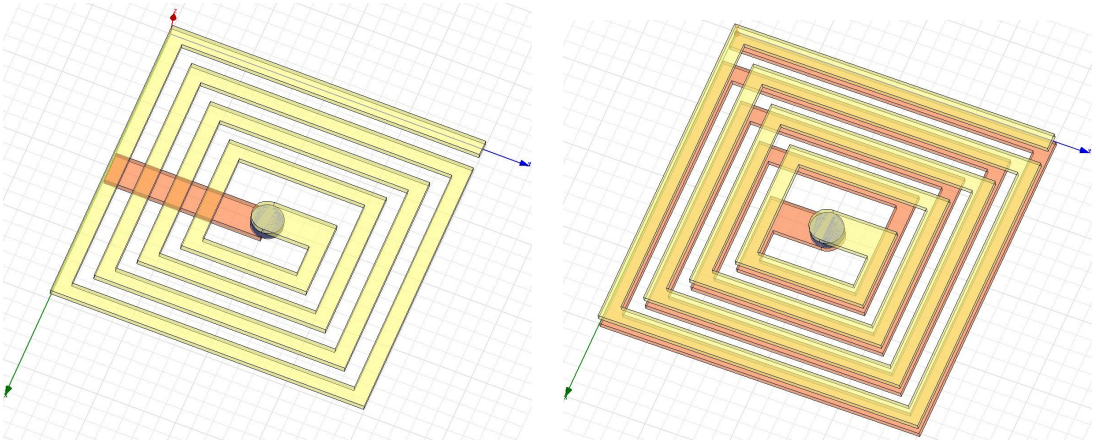


Figure 102 3-D perspectives of 4-turn, 100μm diameter single- and two-layer inductors with metal width and spacing equal to 5μm
(left) single-layer inductor with winding on M5 and connection to transmission line on M4
(right) two-layer inductor with windings on M5 and M4, M4 winding can connect directly to transmission line routing

In order to achieve a high density of interconnections, the AC coupled elements must be routed on the substrate. For substrates fabricated in the MCNC process, routing rather than inductor size will limit I/O density. To illustrate, Figure 103 shows a fully routed 32×32 array of AC connections and 16×32 array of DC connections. Each of the AC connections is a symmetric, center-tapped (i.e. differentially-driven) 100μm diameter inductor. Figure 104 shows a close up view of the coupling elements, vias, solder bumps, and routing. In the figure, the solder bumps are circled in red and the vias are circled in yellow.

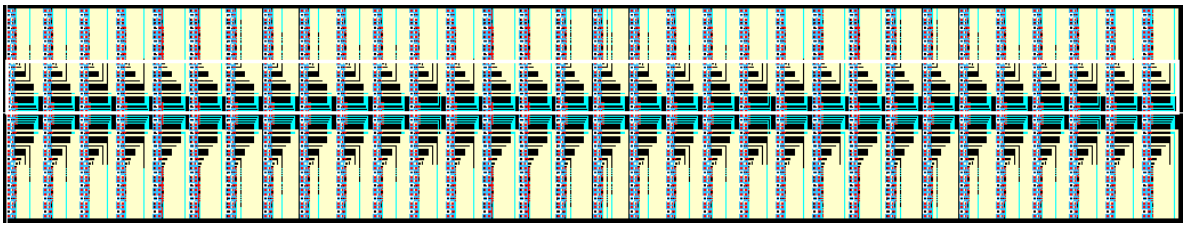


Figure 103 Layout snapshot of fully routed 32 x 32 array of differential AC connections and 16x32 array of DC connections in MCNC process

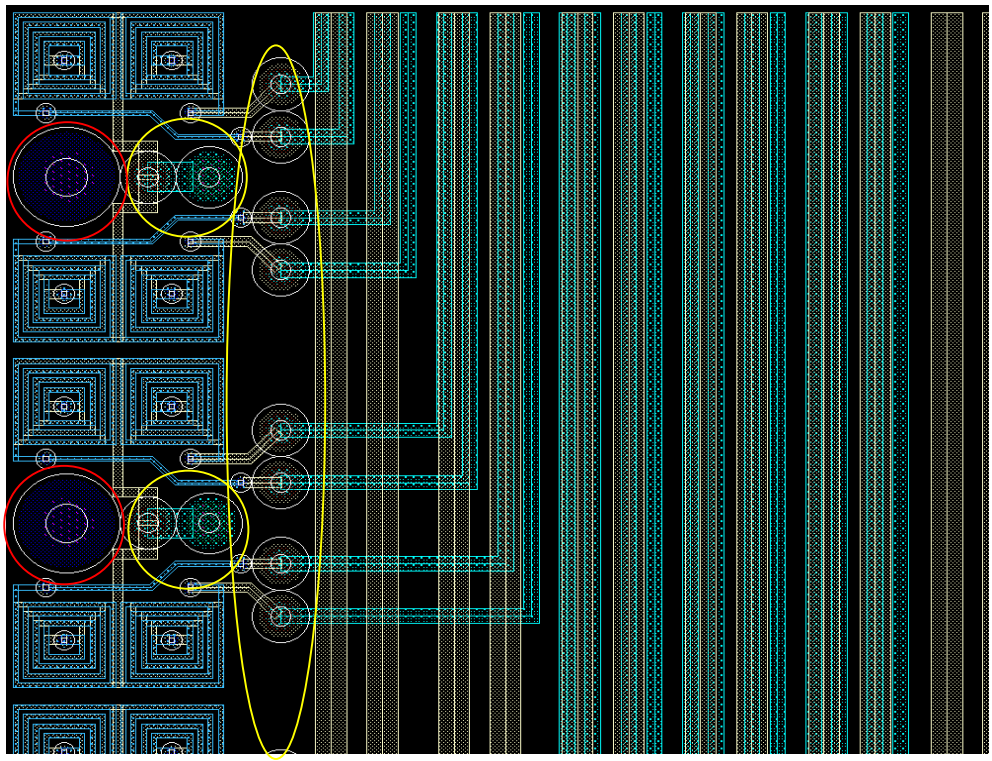


Figure 104 Zoomed-in view of fully routed design in MCNC process showing relative sizes of vias, solder bump sites, coupling elements, and routing.

As drawn, the array in Figure 103 consists of 1516 total I/Os in 188mm^2 – 512 DC connections and 1024 fully differential AC I/Os. All of the AC elements are routed with pairs of coupled microstrip lines designed both to have 50Ω impedance (i.e. metal3 routing: 15μm wide lines with 10μm gap and metal4 routing: 30μm wide lines with 15μm gap) and to be isolated from neighboring lines (i.e. metal3 routing: 20μm gap between neighboring pairs of lines and metal4 routing: 30μm gap between neighboring pairs of lines). In terms of area consumption of the drawn structure, the solder bumps and coupling elements consume 15% of the total area, the vias consume 13% of the total area, and the routing consumes 72% of the total area.

Extrapolated to an area of 310mm^2 as reported in the ITRS roadmap [1] the structure would provide 2533 total I/O while requiring only 844 direct, mechanical connections. It is important to note that the AC I/Os provide fully differential signal paths with a single I/O element. In order for a packaging technology that provides a contacting, mechanical connection for *every I/O* to replicate the density available with the AC Coupled approach shown in Figure 103 the technology would have to support 4221 total I/O in a 310mm^2 area. Thus AC Coupled Interconnects can greatly ease the requirements placed upon the mechanical interface.

Chapter 6 Future work

The research presented in this dissertation can be continued in several areas including coupling elements and transceivers. Development must also continue on the process technology for fabricating substrates amenable to AC Coupled Interconnections. Work can also be done on integrating design rules for AC Coupled systems into CAD tools to ease the burden on future designers of such systems. Specific innovations that can be achieved in each of these areas are presented in the following discussion.

6.1 Coupling Elements

A new model for coupled inductors has been presented but a methodology for accurately predicting parameter values prior to transformer fabrication needs to be developed. The development of such a methodology will require extensive 3D electromagnetic modeling of coupled inductors as well as actual device fabrication and measurement.

The performance of new topologies of inductors compatible with transceiver design should also be investigated. For example, a current steering transmitter circuit might benefit from driving a center-tapped inductor rather than the single-ended elements discussed in this work.

6.2 Transceiver Design

In order to demonstrate a complete, robust AC Coupled system, transceivers to maximize bandwidth and minimize power consumption must be demonstrated as capable of transmitting data over 10cm or longer substrate traces at 5Gbps in the presence of many nearest neighbors and other noise sources. Transmitter and receiver circuits in CCI systems can continue to be optimized, but for LCI systems, such transceivers need to be developed.

In order to achieve signaling rates beyond those that can be achieved by simple pulse signaling, transmitter-side equalization can be employed, but this will require transceivers that implement either continuous-time or discrete-time filtering. The design and optimization of such transceivers is a promising area of future research.

6.3 Substrate Fabrication

The gap that exists after joining chip to substrate plays a pivotal role in the quality of coupling that the passive L or C elements can achieve. Solder bump fabrication and joining processes must be developed and continually optimized to allow for tight control over this gap.

A substrate fabrication process needs to be developed to prevent the pitch of dense arrays of LCI and CCI elements from becoming routing-limited. This will require substrates supporting many routing layers and fabrication processes that maintain tight control over material parameters and fabricated line widths and via sizes.

CCI can benefit from the development and incorporation of high-k dielectric materials as underfills in the chip-substrate gap, and work is underway to develop such materials. Research should also be done to develop underfill materials that will enhance the performance of LCI systems.

6.4 CAD Tools

Successful design of AC Coupled systems relies upon the careful balancing of several complex tradeoffs. The knowledge required to design CCI and LCI systems should be distilled into a CAD tool capable of helping a designer visualize the impact of each design decision upon system specifications such as I/O density, power and bandwidth. Presently, a system designer would have to invoke several design tools and then rely upon educated guesses for final element geometries and placement. However, as predictive modeling for coupling element improves and transceivers are developed and characterized, criteria for meeting system specifications can be captured by a set of design rules and implemented in CAD tools.

Moreover, since AC Coupled systems promise to provide very high densities of I/O, CAD tool functionality should be extended to enable co-design of ICs and their corresponding substrates.

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