ABSTRACT

SACHIN, SONKUSALE. Planar Edge Defined Alternate Layer Process (PEDAL) - an unconventional technique for the fabrication of sub-25 nm nanowires and nanowire template. (Under the direction of Professor Paul. D. Franzon).

As defined by the US national science foundation, “nanofabrication is the process of making functional structures with arbitrary patterns having minimum dimensions less than 100 nm”. Nanofabrication, a key step in nanotechnology, has applications not only in conventional semiconductor devices but also in sensors, memory, nanofluidics, cross-bar logic architecture and nanoelectrical mechanical systems. In this research I have proposed and successfully demonstrated an unconventional lithographic technique called Planar Edge Defined Alternate Layer (PEDAL) to fabricate wafer scale sub 25 nm nanowire template. Good dimensional control and wafer scale uniformity of this process is shown by uniformity analysis of the width and spacing of an array of sixteen line-width structures with approximately 42 nm pitch and twenty four line-width structures with approximately 23 nm pitch. Results on routing capability of this process along with results of palladium nanowires obtained by PEDAL lift-off process done on the template with 42 nm pitch is also reported. In the case of template with array of sixteen lines, the average pitch of array across the 4 inch wafer was measured to be 40.83 nm with the standard deviation of 2.29 nm where as the average pitch of the lines in an array was found to be 41.5 nm with the standard deviation of 4.64 nm. After Pd lift-off the average pitch in nanowire array was measured to be 41.88 nm with standard deviation of 1.83 nm, close to the values obtained for the template. In the case of array of twenty four line-widths, average pitch of array across the 4 inch wafer was measured to be 21.1 nm with the standard deviation of 5 A where as the average pitch of the
line in an array was found to be 22.6 nm with the standard deviation of 9 Å. Other than experimental analysis, results from numerical simulations to find processing conditions to get good dimensional control in PEDAL process by taking process variations into account are also presented in this thesis.
Planar Edge Defined Alternate Layer Process (PEDAL) – an unconventional technique for the fabrication of sub-25 nm nanowires and nanowire template

by

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To my Father
Sachin Ramrao Sonkusale was born in Bhavnagar, Gujrat, India. He received his Bachelor of Technology degree in Electrical Engineering from Indian Institute of Technology, Kanpur, India, in 2000. He received his Masters of Science degree in Electrical Engineering from North Carolina State University, Raleigh, NC, in 2002. As a research assistant at Department of Electrical Engineering in Power Semiconductor Research Center, North Carolina State University, he worked on diodes, and accumulations and inversion channel field effect transistors on 4H-SiC substrate designed using Reduced Surface Electric Field (RESURF) concept with high reverse breakdown voltages and small on state resistance.

Since 2002, his primary area of research is nanofabrication of nanostructures and nanodevices. His current doctoral research focuses on one of the key challenges of nanofabrication which is lithography at sub-25 nm scale. His other contributions are novel processing approaches for sensor arrays for chemical and biological sensors, carbon nanotube vacuum encapsulation for active matrix displays, nanoelectromechanical structures for high frequency resonators, and unconventional lithography technique using resonant electromagnetic field assisted colloidal self assembly.
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CHAPTER 1

1. INTRODUCTION

Governments and companies around the world are spending billions of dollars on research related to nanotechnology as the expectations surrounding nanotechnology and nanofabrication are high. The U.S. government promoted an initiative announced in 2000 based on optimistic predictions that it would eventually lead to “materials with ten times the strength of steel and only a fraction of the weight, the ability to shrink the information housed in the Library of Congress into a volume the size of a sugar cube and the ability to detect dangerous cancerous tumors when they are only a few cells in size”. This initiative predicts nanotechnology will add a trillion dollars to the gross national product and add 2 million new jobs to the U.S. economy by 2013. Nanobusiness alliance says that nanotech companies are already generating millions of dollars and National science foundation predicts that Nanotech product and services will reach $1 trillion by year 2012. At present nanotechnology is at its early exploratory stage and it provides tremendous opportunity to do research which can lead to commercial production of cheap and high performance devices.

Nanoscience and nanotechnology cover many different areas, but one key set of methods for both is nanofabrication. The development of microelectronic circuits with <100-nm-scale features is proceeding rapidly by extensions of existing, conventional photolithographic techniques. Unconventional, low cost techniques and new materials will be required, for structures with dimensions below 20 nm, to change the cost structure of this very capital intensive industry. New products and technologies outside the field of microelectronics, but
still requiring nanoscale fabrication, are being developed in widely different areas such as biology, materials science, and optics. There will be many opportunities for the application of unconventional nanofabrication in these areas including (i) chemical and biological sensors (ii) Chemical catalysts (iii) High frequency filters and resonators (iv) data storing device; (v) printed, low-cost organic microelectronics; (vi) sub wavelength optics; (vii) tools for biology for investigating individual cells and cell-cell interactions; (viii) nanofluidics; (ix) nanoelectrical mechanical systems (NEMS).

As defined by the US national science foundation, "nanofabrication is the process of making functional structures with arbitrary patterns having minimum dimensions currently defined to be less than 100 nm. Speed and the performance of the microprocessors depend on the size of the individual transistors in the circuit, smaller the size, greater is the performance and speed. This is driving the electronics industry to shrink the feature size of semiconductor devices. According to Moores law the number of transistor in a given chip area doubles every eighteen months. Although the current achievement trails Moores law (figure 1.1), it is imperative that the feature size will keep shrinking and new lithography techniques needs to be explored to meet the high performance demands. At present the smallest gate length of the microprocessor currently in production is 37 nm [1] and current half-pitch or periodicity of manufactured dynamic random access memory (DRAM) is 90 nm. The International Technology Roadmap for semiconductors (ITRS), projects reaching the 45-nm node in 2010 (corresponding to transistor gate lengths down to 18 nm and DRAM spacing of 45 nm). To meet these stringent demands, researchers are developing alternative nanofabrication techniques which can evolve into new technology.
There are two ways the fabricating nanoscale features. One approach is to etch the patterns on the resist layer by serial writing techniques like scanning electron beam & focused ion beam or by parallel patterning techniques like photolithography. High operating costs and limited availability have restricted the use of these techniques to semiconductor IC industry. In photolithography beyond wavelength of 157 nm (figure 1.2) significant issues arise in terms of availability of light sources masks and need of new photoresist material. Other lithographic techniques using different forms of radiation including extreme UV, X-ray, electron beams, and ion-beams, are growing in importance.
In unconventional techniques, properties of molecules or colloidal particles to assemble into two dimensional or three dimensional structures are used to create patterns on substrate. These unconventional techniques like nanoimprinting [2-5], edge defined lithography [6-14], and self-assembly [15-18] use conventional techniques like photolithography for making initial template. The development in some unconventional lithographic tools, like molding [19, 20], dip pen [21-24] and nanoimprint has reached the level of commercial production. These techniques provide the high-yield low cost nanofabrication on non-planar surface and over large areas, an alternative to high-cost and low yield conventional lithographic
processes. The ability of any technique to replicate the nanostructures rapidly and inexpensively will be key factor in deciding which technique will prevail. In methods like molding and imprinting nanoscale patterns on masters are transferred to organic soft layer and these techniques have demonstrated their ability to make nano size features repeatedly on the large surface area and seems promising candidates of nanofabrication. The other method of nanofabrication uses scanning probe to write nanofeatures with nanoscale resolution using self assembly of organic material from tip onto a substrate. Although these unconventional lithography techniques are limited in terms of the patterns they can generate and/or by dependence on conventional lithography to generate initial patterns but they are very promising approaches towards low-cost fabrication of regular arrays of nanostructures like nanowires and nanodots to make high performance chemical and biological sensors, optical polarizers, data storing devices and chemical catalysts.

Low cost, high yield methods are needed to reduce the overall fabrication cost of the semiconductor chip. Even if these methods can generate simple patterns like array of wires, it will greatly reduce the fabrication cost as there are around fourteen layers of interconnect in todays chip, which includes one metal 1 layer, eight intermediate layer and five global layer (figure 1.3). As shown in table 1, currently a typical chip has total intermediate and metal 1 interconnect length of 907 m/cm² and by year 2018, the predicted total length will be 5035 m/cm².
Figure 1.3: Typical cross section of a chip (source – website of ITRS)

Table 1: ITRS semiconductor integrated circuit requirement (source ITRS website)

<table>
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<tr>
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<tbody>
<tr>
<td>Year of production</td>
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<td></td>
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<tr>
<td>Technology node</td>
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<td></td>
<td></td>
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<tr>
<td>DRAM ½ pitch (nm)</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>35</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
</tr>
<tr>
<td>MPU/ASIC ½ pitch (nm)</td>
<td>95</td>
<td>85</td>
<td>76</td>
<td>67</td>
<td>60</td>
<td>54</td>
<td>42</td>
<td>38</td>
<td>30</td>
<td>27</td>
<td>21</td>
</tr>
<tr>
<td>MPU printed gate length (nm)</td>
<td>45</td>
<td>40</td>
<td>35</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>20</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>MPU physical gate length (nm)</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
<td>9</td>
<td>7</td>
</tr>
<tr>
<td>Number of metal levels</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>13</td>
<td>14</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>Total interconnect length (exclude global layer (m/cm2))</td>
<td>907</td>
<td>1002</td>
<td>1117</td>
<td>1401</td>
<td>1559</td>
<td>1784</td>
<td>2214</td>
<td>2544</td>
<td>3544</td>
<td>4208</td>
<td>5035</td>
</tr>
<tr>
<td>Metal 1 wiring pitch (nm)</td>
<td>190</td>
<td>170</td>
<td>152</td>
<td>134</td>
<td>120</td>
<td>108</td>
<td>84</td>
<td>76</td>
<td>60</td>
<td>54</td>
<td>42</td>
</tr>
</tbody>
</table>
The metal1 layer covers more than 20% floor area of the wafer on DRAM chip and reducing the pitch of metal1 layer will provide more wafer area for IC component devices and hence increasing density the performance. Currently the pitch of metal1 layer is around 190 nm, and as suggested by ITRS it should shrink to 42 nm by year 2018. In the current research, I have proposed a reliable and cost-effective process for making wafer scale sub-25 nm nanowires. Currently, ebeam lithography [42-44], Nanoimprint lithography [95, 96], step and flash lithography [19, 88-92], immersion lithography [30-35] and interference lithography [40-41] seems to be the best candidate for making sub-25 nm nanowires. For low cost unconventional lithography technique to be successful, it is imperative that it fits in existing fabrication infrastructure; it should have an alignment capability, high yield and good critical dimension control. In the imprinting, embossing, scanning beam and other lithographic process which uses soft organic resist layer, the line-width structure has high width variation around the corners and along the length of their route. This limits their critical dimension control and the electrical properties of interconnects varies from die to die. Most of the techniques which have been developed for making nanometer size features are also limited by the technological challenges, as tabulated in Table 2, and more research is needed to find solutions to the existing problems.

Pattern transfer is another important step in nanofabrication following lithography. Most of the lithography techniques can only make patterns on the soft organic layer. To transfer the smaller patterns to the underlying substrates Reactive ion etching techniques like Deep Reactive Ion etching (DRIE) and Inductively Coupled Plasma Reactive Ion Etching (ICPRIE) is usually used.
<table>
<thead>
<tr>
<th>Pattern Formation using</th>
<th>Basis for intrinsic limitation</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Photons</strong>&lt;br&gt;UV, DUV, EUV, X-rays</td>
<td>Diffraction&lt;br&gt;Depth of Focus&lt;br&gt;Lenses and mask manufacturing&lt;br&gt;Resolution and depth of focus limited by wavelength and Numerical aperture</td>
<td>contact mode, near–field exposure, non-linear photoresist, optical proximity correction, Immersion technique, Interferometric lithography</td>
</tr>
<tr>
<td><strong>Electron and other Particles</strong>&lt;br&gt;electron and ions&lt;br&gt;neutral atom</td>
<td>Electrostatic interaction, serial writing, small field of writing, mask damage</td>
<td>Neutral atoms Projection particle beam lithography (SCALPEL) Arrays of sources</td>
</tr>
<tr>
<td><strong>Machining/Writing with Scanning probes</strong>&lt;br&gt;AFM, STM, NSOM, SECM and Dip pen</td>
<td>Serial writing, small field of writing, Surface diffusion of molecular ink, Low reproductibility because of changing tip dimension from use to use.</td>
<td>Array of probes, Harder material for making probes</td>
</tr>
<tr>
<td><strong>Physical contact</strong>&lt;br&gt;Printing, molding, Step and flash (SFIL), embossing</td>
<td>van der waals forces, speed of capillary filling, adhesion, mold damage</td>
<td>Low viscous solution, Surface modification.</td>
</tr>
<tr>
<td><strong>Self assembly</strong>&lt;br&gt;Block copolymer, proteins, DNA , colloids</td>
<td>Less control over domain size and shape, and defect density</td>
<td>Directed self-assembly using optical fields (holographic techniques) template or electric field</td>
</tr>
<tr>
<td><strong>Deposition</strong>&lt;br&gt;Cleaved edge overgrowth (SNAP)&lt;br&gt;Shadowed evaporation</td>
<td>Limited pattern shapes are possible, densely packed structure difficult to make,</td>
<td></td>
</tr>
<tr>
<td><strong>Size reduction</strong>&lt;br&gt;Compression of elastomeric molds</td>
<td>Uniform deformation with less than 100 nm controllability in dimension is difficult</td>
<td></td>
</tr>
<tr>
<td><strong>Edge based technologies</strong>&lt;br&gt;Near-field phase-shifting photolithography, Topographically directed photolithography, &amp; etching</td>
<td>Difficult mask preparation, low flexibility in pattern shapes</td>
<td></td>
</tr>
</tbody>
</table>
Reactive ion etching techniques are not successful in patterning all metals; hence the lift off technique is used to fabricate metal nanostructures. The lift-off technique produces the complimentary/negative of the pattern in the organic resist layer. In liftoff, the metal is deposited directionally on the patterned resist layer and then the underlying resist layer is etched off (figure 1.4(a), 1.4(b)). This leaves the metal only on the portion of the substrate where the organic resist layer was removed during lithography. The lift-off technique becomes increasingly difficult as the feature size decreases and the spacing between adjacent features decreases.

![Diagram of pattern transfer on metal layer using monolayer resist lift-off and bilayer resist lift-off]

**Figure 1.4: Pattern transfer on metal layer using monolayer resist lift-off and bilayer resist lift-off**

In soft lift-off the patterned organic resist layer is exposed to descum (i.e. residual resist removal by oxygen plasma) process step which alters the feature size. The cross-section of
the patterned resist layer are not exactly rectangular but tapered at the top as shown in the figure 1.4, due to the descuming step required to remove residual resist in the open areas. If the aspect ratio of the resist layer pattern is not high enough, the metal covers the entire step of the resist (figure 1.4(c)). The lift-off of the underlying resist layer becomes difficult once the metal covers the step edges as well. This problem is encountered basically in making dense array of nanowires with discontinuity observed along their length and more around the corners of their route. Some solutions like two layer resists have been demonstrated (figure 1.4(d) and 1.4(e)), but this technique has restrictions as the minimum spacing between nanowires depends on the undercut of the bottom resist layer.

![Figure 1.5: Pattern transfer by reflow of metal on hard template and lift-off](image)

Other intrinsic limitation of the lift-off technique is the reduced flow of the etchant in the spaces (i.e. the wet ability), as the feature size gets smaller, to etch the underlying resist
layer. A hard lift-off process followed after annealing can overcome the problem associated with soft lift-off. In hard lift-off instead of soft resist layer we have patterns on hard template, eliminating the possibility of size altering due to descum step. Also the reflow of the metal before lift-off at elevated temperatures by Rapid Thermal Annealing or by Pulsed Laser methods, can resolve the step coverage problem associated with the metal deposition on the nanowire templates (figure (1.5)). The elevated temperature annealing also improves the conductivity of the metal and reduces electromigration problem due to increase in grain size, although care has to be taken not to alter the composition of metal by interaction with underlying material during annealing.

In this research we have developed a new process called PEDAL (planar edge defined alternate process) process, which can be developed into more reliable technology to be used for wafer scale fabrication of sub-5 nm metal nanowires and nanowire template. Array of nanowires with with well defined length and route, aligned to the other layers with the accuracy of the initial lithographic technique used to define the step, can be fabricated. At present we have demonstrated the fabrication of array of sub-25 nm palladium nanowires on Silicon (110) wafer. The “PEDAL lift-off” has the ability to fabricate metal nanowires directly on the wafers without using nanoimprint techniques or without using organic resist layer as the lift-off layer. PEDAL process involves defining the path and location of nanowires by etching a trench directly in silicon wafer, or in the layer deposited on the silicon wafer. As shown in fig. 1.6(a), a trench is etched into silicon wafer by anisotropic etch. After defining the trench, a buffer layer of a-silicon is deposited on the trench {figure 1.6(b)} followed by conformal deposition of alternate layers of silicon nitride and amorphous
silicon (fig. 1.6(c)). Width of lines and spaces is decided by the thickness of the deposited thin films and number of depositions decides number of lines and spaces in an array. To planarize the topography of trench a thick layer of a-silicon is deposited for filling the trench followed by spin coating of a polymer (fig. 1.6 (d)). The stack of polymer, a-silicon and silicon nitride is planarized down to the required depth (figure 1.6(e)) using single etch process which is nonselective to silicon nitride, amorphous silicon and polymer or using combination of etch processes, involving a process which is nonselective to polymer and amorphous silicon to etch to level A and other etch process nonselective to silicon nitride and amorphous silicon to etch to level B (figure 1.6(d)). The lines and spaces are revealed by selectively etching a-silicon material (figure 1.6 (f)). This gives a template with silicon nitride lines which can be used for nano-imprinting. Nanowires can be directly patterned on the template by using the lift-off process. In this process lines and spaces are revealed by selectively etching silicon nitride (figure 1.6 (g)) followed by e-beam evaporation of metal on the wafer (figure 1.6 (h)) and lift-off of the metal by etching a-silicon (figure 1.6(i)). This gives us metal nanowires on insulting silicon nitride layer.
Figure 1.6: Schematic of PEDAL process and PEDAL lift-off process.
Various modifications of the PEDAL process discussed above are possible to give the desired end results; however, the basic method of defining lines and spaces remains the same. The process has the flexibility of routing the nanowires around the Logic and memory modules across the entire wafer in predetermined way. The fabrication facilities required for the process are readily available and this process provides the great alternative to existing slow and/or costly nanowire patterning techniques. PEDAL lift-off process when incorporated with Atomic Layer Deposition has the ability to make wafer-scale aligned sub-5 nm wide nanowires.

Some of the advantages of using PEDAL process for making array of sub-25 nm aligned nanowires are

1. It’s a wafer-scale process to define sub-25 nm array of aligned nanowires and nanowire template i.e. instead of writing one nanowire at a time (e-beam serial writing lithography) or making one die at a time (step an repeat photolithography), nanowires are fabricated all across the wafer simultaneously.

2. Minimum wire width and spacing is limited by thickness of the film deposited and is not limited by the wavelength of light, optics of lithography tools as in photolithography or scanning beam lithography.

3. Metal nanowires with well defined spacing, length and route can be fabricated with PEDAL unlike non-templated self-assembly process and superlattice nanowire transfer process.

4. There is little variation in the width and spacing of a wire along its total length and around corners. The hard template also gives resistance to feature size alteration
during descum and provides the alternative of high temperature metal reflow before lift-off. High temperature reflow can also reduce the surface roughness, increase the grain size and increase the mean time to failure of nanowires caused by electromigration.

5. Nanowires fabricated by PEDAL can be aligned to the other layers of the integrated circuit with the accuracy depending on the initial lithography step used to define the step edge.

6. This technique provides the feasible alternative to make not only wafer scale interconnects, but also low cost, high sensitivity chemical and biological sensors, high surface area chemical catalysts, optical polarizer, data storing devices, high frequency saw filters and cavity resonators.

7. PEDAL process has the potential to make sub-5 nm metal nanowires structures by using LPCVD process with low deposition rate or by integrating with Atomic layer deposition, which has the capability of conformally depositing monolayer of wide range of materials.

8. Fits in existing fabrication infrastructure and does not need costly lithographic tools like ebeam lithography or EUV lithography tools which are needed in most of the existing nanofabrication techniques to make initial masks, molds or templates.

Disadvantages of PEDAL process are

1. Nanowires form loop around edges of trenches which requires additional truncation step involving a photolithography and an etching step. If these templates are to be used for nanoimprinting then looping can be avoided, without the need of additional
photolithography and etching step, by modifying trench design and using the property of selective planarization as discussed in Appendix B.

2. Topography of lines and spaces greatly depends on sidewall angle of trenches, conformality of thin films and non-selectivity of RIE planarization process. In section 3, there is detailed analysis of effect of non-ideal processing conditions of each of these steps. Using numerical simulations, conditions to minimize the effect of the non-ideal processes on topography of template lines have also been derived.

3. Accuracy of alignment of features on wafer to on-template nanowires depends on the alignment accuracy of the lithography process used to define trenches. In nanoimprinting applications, alignment accuracy of imprinted lines will also depend on alignment accuracy of nanoimprinting tool.

4. Number of nanowires that can be fabricated in an array depends on the total time of thin film deposition process as well as the conformality of thin films. Conditions to minimize standard deviation of line widths in an array of large number of lines, resulting from non-conformality, has been derived in section 3.
CHAPTER 2

2. REVIEW

This chapter contains reviews of existing lithography techniques with demonstrated ability to make sub-100 nm nanowires. Some of these techniques are commercially available and are currently used in semiconductor industry. Other techniques are been demonstrated, though not yet completely developed for commercialization, but they seem to be promising candidate for making nanowires. Gates B.D, in his publication [29], divides lithography techniques into two categories, conventional as well as unconventional. This review is based on his publication and some techniques believed to be more successful than others are presented. As described in his publication, in conventional techniques he considers lithography technique using photons (UV, EUV, DUV, Xrays), electrons (e-beam), ion (focused ion Beam) and neutral particles. In unconventional techniques he included techniques like, embossing, molding, scanning probe tip, imprinting, edge defined lithography all of which were developed as a low cost alternative to costly conventional lithographic techniques. One of the main differences between conventional lithography technique and unconventional lithography technique is that conventional techniques are immensely researched and widely used in semiconductor industry where as unconventional techniques are relatively new. Other difference is that most of the unconventional techniques depend on conventional techniques for transferring or assembling patterns on substrate. In this section unconventional as well as conventional techniques are briefly discussed with some insight on their limitations.
2.1 Photolithography

In photolithography, properties of a photoresist are altered by exposing the resist to light. These photoresist materials are organic materials that cross-links and become more soluble in a basic solution upon exposure to light. The area where the photoresist is exposed to light is selected by the opening in the mask (figure 2.1(a)), usually obtained by etching chromium coating on glass/quartz plate. The region on the mask where chromium is present, shields photoresist from light. The patterned photoresist masks the substrate during subsequent process steps like etching (figure 2.1(c)), or it allows selective deposition of metal on substrate by lift-off technique. Widely used photolithography technique is step and scan projection lithography technique where a small area on the resist is exposed at a time and the whole wafer is scanned in number of steps. Scaling down dimensions in photolithography requires low wavelength light and complicated mask designs involving optical proximity correction and phase shifters to retain exposed resist feature profile and resolution. Need for new light source, optics of the system, resist and complicated mask design and material considerably increases the cost of lithography technique.

Another potential route to fabricate features with sub-50-nm resolution using 193-nm light is immersion lithography [30-35]. Imaging resolution of photolithography is improved in immersion lithography by altering the refractive index of medium between photoresist and imaging lens (figure 2.2). Increasing index of refraction of this medium by inserting fluid with refractive index higher than air (n=1) increases depth of focus and numerical aperture.
Switching medium from air ($n = 1$) to water ($n = 1.47$ at 193 nm) allows the lens systems to be designed with numerical apertures approaching 1.3, thus significantly improving ultimate achievable imaging resolution. This technique is still in exploratory stages as there are still issues related to contact of water with photoresist and mask. In order to use photolithography to pattern smaller features we need further advances, such as decreasing the wavelength to 157 nm [39,37] or to extreme ultraviolet (EUV) light which as discussed earlier will increase the cost of photolithography.
Figure 2.2: Immersion Lithography (a) Typical immersion lithography tool implemented using 193nm stepper (b) Immersion lithography principle (c) SEM of array of lines fabricated with immersion lithography with half pitch 65 nm (d) 50 nm and (e) 45 nm

To make simple patterns like nanowires and nanodots, use of masks can be eliminated by using interferometric lithography (40,41) which involves the constructive and destructive interference of multiple laser beams at the surface of a photoresist (figure 2.3). Interferometric lithography has demonstrated patterns as small as array of 40-nm wide parallel lines separated by 57 nm. The interference lithography technique is restricted to making array of symmetric structures and no routing of nanowires is possible.
Figure 2.3 (a) Schematic of interferometric lithography system. At a wavelength of 380nm, the two laser beams created by the splitter are recombined at the surface of the photoresist-coated substrate and form a standing wave which creates a grating image in the resist (b) top view of linear gratings (c) 515 nm hexagonal gratings (d) cross section of 515 nm line gratings.

2.2 Scanning Beam Lithography

Scanning beam lithography using electron beam [42-44] and ion beam [25-28] is a serial technique (figure 2.1(b)) with the capability to generate high-resolution features with arbitrary patterns. Scanning beam is slow technique as it involves writing one feature at a time and hence is used for the purpose of making photomasks. Patterning high resolution features with ebeam or ion beam depends on diameter of particle, acceleration of particle,
sensitivity of resists like Poly Methyl Metha Acrylate (PMMA) and developing condition of exposed resist.

![Diagram of E-beam direct write system](image)

**Figure 2.4: cross-section of typical E-beam direct write system (source- class notes ECE 738)**

A focused ion beam can write patterns into a photoresist or directly onto the substrate [74] by “milling” or selectively removing exposed material through ion bombardment. This lithography technique can pattern features in a semiconductor with resolution down to 20 nm and with the smallest lateral dimensions down to 5 nm. Contamination in FIB lithography is from implanted ions or material displaced from the substrate after milling. It can also create patterns in an additive process by ion deposition or a localized chemical vapor deposition.
2.3 MicroContact Printing

The transfer of ink from a relief structure to a target surface is a common process in classical printing techniques. In μCP [45] this principle is used to fabricate chemical patterns with micron-scale resolution on technological surfaces. The most famous application of μCP is to print alkanethiols on gold surfaces (figure 2.5). These molecules chemisorb on the gold and form self-assembled monolayers (SAMs). The metal is densely covered by the SAM, whereas the end group of the thiolates determines the chemistry, wetting, and transport properties of the surface. A SAM can effectively block ion transport to the underlying gold and can thus serve as a molecular resist in cyanide etch bath where the cyanide ions catalyze the dissolution of the gold in the uncovered regions. This process transfers the printed pattern into the substrate. The stamps for μCP are typically made from elastomeric materials like polydimethylsiloxane (PDMS). The precursors of the stamp material are polymerized on a master defined by optical or electron-beam lithography. After curing the stamp is released from the mold. The pattern of the stamp is impregnated with ink using an ink pad (left) or by applying some ink solution (right). During printing conformal contact between the relief pattern and the substrate allows the localized transfer of thiols and the formation of SAMs. The chemical pattern of SAMs can be transferred into the gold by a wet etch process. At submicron scales the diffusion of thiol molecules during printing can affect the contrast and broaden the printed features. The way of inking, and the duration of the print has been optimized to achieve ultimate resolution. With the method of contact inking we could reduce the effects of diffusion by a better control of the amount and the distribution of ink on the
Figure 2.5 (a) Diagram of process: A prepolymer (2) covering the master (1) is cured by heat or light, and demolded to form an elastomeric stamp (3). The stamp is inked by immersion (4) or contacted with an ink pad (5), and printed onto the substrate (6), forming a selfassembled monolayer (SAM). The ink pattern (7) is then transferred into the substrate by a selective etch (8). (b) Scanning electron microscopy (SEM) micrographs of the master, (c) image of the stamp, and (d) SEM micrograph of a printed and etched pattern.
Other form of micro-contact printing is electrical micro-contact printing in which flexible electrode mold is used to pattern a thin film of material which accepts and maintains electric potential by injecting and trapping charges [41,46-48]. Recent studies have used electric micro-contact printing in high density data storage [46] and electrostatic printing of particles such as graphitized carbon and iron oxide [48-50].

2.4 Scanning Probe tip lithography

As the name suggests this technique uses scanning probe tips for patterning features on the substrate. The scanning probe tip can be used to scrape layers from the surface as done in Nanoshaving [51-53] (figure 2.6) followed by self assembly of desired molecules in its place (nanografting). This method can be used to pattern or assemble multiple types of molecules on the surface. In this method defects in patterned material not only arise due to inherent defects in self assembly but also due to topographically dependent shaving efficiency using scanning probe tips.

In other method which is called Dip Pen Lithography [54-57], tip is dipped in an organic material which can self assemble on to substrate (figure 2.7). Dip-Pen Nanolithography (DPN) is a scanning probe nanopatterning technique in which an AFM tip is used to deliver molecules to a surface via a solvent meniscus, which naturally forms in the ambient atmosphere. This direct-write technique offers high-resolution patterning capabilities for a number of molecular and biomolecular 'inks' on a variety of substrates, such as metals, semiconductors, and monolayer functionalized surfaces. This process can fabricate features with lateral dimensions as small as 12 nm.
Figure 2.6: Procedure for nanografting. The schematic diagram provides an example of the fabrication of a $C_{18}S$ nanostructure inlaid in a $C_{10}S$ monolayer. The drawings are not to scale. (a) Well-ordered $C_{10}S$ on gold imaged via AFM with a low imaging force of 0.3 nN in a 2-butanol solution containing $C_{18}SH$. (b) At the image force of 5.2 nN (higher than the displacement force threshold of 5.1 nN), $C_{10}S$ molecules can be displaced during the scan, and $C_{18}SH$ molecules (0.1 mM) self-assemble on the exposed gold surface. (c) The resulting nanofeature of $C_{18}S$ can be imaged by AFM at a low imaging force, e.g. 0.3 nN. Under these conditions, the gold substrate is not deformed. The typical time to complete procedure (a-c) is 5 min.
Figure 2.7: Some of the potential applications of DPN. This technique allows one to create a large variety of systems with a single lithographic setup.

DPN allows one to precisely pattern multiple patterns with near-perfect registration. It's both a fabrication and imaging tool, as the patterned areas can be imaged with clean or ink-coated tips. The ability to achieve precise alignment of multiple patterns is an additional advantage earned by using an AFM tip to write, as well as read nanoscopic features on a surface. These attributes make DPN a valuable tool for studying fundamental issues in colloid chemistry, surface science, and nanotechnology. For instance, diffusion and capillarity on a surface at the nanometer level, organization and crystallization of particles onto chemical or biomolecular templates, monolayer etching resists for semiconductors, and nanometer-sized tethered polymer structures can be investigated using this technique.
Scanning probe lithography is also used to modify a surface chemically [58] like localized oxidation of a surface (metal, semiconductor, or SAM) in a pattern scanned by a conductive AFM or STM tip (Figure 2.8 (a)) [53, 58-63] in which a local electric field between the conductive tip and the surface induces oxidation of the surface. Typically, this method can generate 50-nm wide features. A carbon nanotube-modified AFM probe can, however, pattern 10-nm wide lines of silicon oxide on a silicon hydride surface (Figure 2.8 (b)) [64].

**Figure 2.8 (a)** Scanning electrochemical oxidation with a carbon nanotube-modified AFM tip can selectively oxidize a surface to pattern (b) 10-nm wide (2-nm tall) silicon oxide lines spaced by 100 nm.

For large volume, parallel production using the technique of writing features with scanning probe tips a system involving arrays of such tips called Millipede has been demonstrated [56, 57, 65, 66]. In this systems each scanning probe tips can be addressed independently and scanned in parallel giving higher sample throughput. Each probe in this array can be mechanically deflected in the vertical direction and resistively heated (fig 2.10). Writing features using scanning probe tips and molecular ink causes broadening of feature size due to
diffusion of ink (figure 2.9). The quality of written features depends on the interaction of tip and surface which greatly depends on surface material and topography.

Figure 2.9: (a) General layout of a DPN probe array. Each probe has 10 thermally actuated probes at one end (b) Unactuated probes are cold and sit on the surface where they modify the surface, actuated probes lift away from the surface where they do not deposit ink. (c) Ten different patterns written simultaneously by ten probes. Deposited ink shows dark in this LFM scans (d) close up of halo-free region from number (e) LFM image of line drawn from by small radius silicon probes under similar condition.

2.5 Self-Assembly for Nanofabrication

Self assembly is a process in which molecules or particles arrange by mutual physical bonding or chemical bonding. Self assembly creates patterns based on the molecule/particle size and surface interaction. As Shown in figure 2.10, self assembly give short range order in
a pattern like arrays of nanorods, arrays of nanodots or arrays of block copolymers. In order to use self assembly for controlled patterning, controlled self assembly processes are used in which self assembly is directed using electric or magnetic fields, surface topography or by external physical force.

Figure 2.10: (a) TEM micrograph of CdSe nanorods (A-C) nanocrystals with width of 3.2 nm and length 11, 20, and 40 nm respectively, (D-F) Nanocrystals with width of 4.2 nm and length of 11, 20, and 40 nm respectively (G) TEM micrograph of 3D assembly of 6 nm as synthesized Fe\textsubscript{50}Pt\textsubscript{50} particles (H) 3D assembly of 6 nm Fe\textsubscript{50}Pt\textsubscript{50} (I) HRSEM image of a ~ 180nm thick, 4 nm Fe\textsubscript{50}Pt\textsubscript{50} nanocrystal (J) High-resolution TEM image of 4-nm Fe\textsubscript{50}Pt\textsubscript{50} nanocrystals.

By directing self-assembly using templates it is possible to introduce an element of pattern into the self-assembled structure and sometimes increase the order of the self-assembled structure. Templated self-assembly [74-75] often uses top-down strategies to fabricate components that direct the bottom-up assembly of molecules, macromolecules, or colloidal
particles. Templated self-assembly is an alternative to nontemplated self-assembly for the controlled fabrication of patterned structures with nanometer-scale local order and for the generation of micrometer-size, or larger, domains of defect-free patterns. The combined use of a conventional lithography technique such as photolithography, and bottom-up self-assembly has been used to pattern block copolymers (Figure 2.11) [74-75].

![Figure 2.11: Templated self assembly of block-copolymer](image)

In this example, self assembled monolayer of PETS (poly ethylene terephthalate) was deposited on a silicon wafer (figure 2.11(a)). The SAM was patterned by EUV lithography by coating with resist layer (figure 2.11(b)) and masked exposure to EUV light (figure 2.11(c)) followed by exposure to soft X-ray in presence of oxygen (figure 2.11(d). This patterns PET chemically rather than physically. The resist was then removed and PS-b-
PMMA copolymer was spin coated onto the patterned SAM (figure 2.11(f)) and annealed (figure 2.11(g)). Chemically modified regions of the SAM present the polar groups containing oxygen and were preferentially wetted by PMMA block and unmodified regions exhibited neutral wetting behavior of block copolymer. Annealing a block copolymer film confined by physical boundaries can also direct the assembly of the copolymer into a regular structure [74-75]. These methods illustrate the use of templating to overcome the major disadvantages of nontemplated self-assembly like high level of defects and the inability to control.

Figure 2.12: Electrically aligned ZnO nanorods between 800-nm spaced, interdigitated gold electrodes on silicon oxide. The electrode fingers on the bottom and on the top were on the same potential. The applied electric field strength was $1.25 \times 10^7$ V/m, and the frequency was 1 kHz.
Figure 2.13: Schematic diagram of (a) a microscopic rod containing alternating sections of gold and nickel where the magnetic sections have an aspect ratio \((t/d)\) of \(_0.5\); (b) self-assembly of rods (the arrows on the nickel sections indicate the “easy” axis of polarization). (c) Scanning electron micrograph (SEM) of multiple bundles of rods. The light sections are gold, and the gray sections are nickel. The aspect ratio of the ferromagnetic sections is \(_0.5\). (b) SEM of a single bundle demonstrating the alignment of ferromagnetic sections.

Electric [76] (figure 2.12) and magnetic fields [77] (figure 2.13) as well as shear forces [78] and spatial constraints [79, 80] have been used to direct the assembly of nanoparticles and nanorods into different configurations. For example, template-assisted self-assembly has been used to direct the assembly of spherical and tetrapod-shaped nanoparticles where the capillary force exerted by the edge of a drop of evaporating solvent confines particles against an edge [82] in a narrow channel (figure 2.14) [83-86] or in a well [87].
In step and flash imprint lithography technique, a UV transparent mask is used to mold the photocurable polymer (19, 88-92). The mold is pressed on the polymer so till its surface is in contact with the surface of the substrate on which polymer is coated. After getting good contact with substrate, UV light is shine through the mold for curing photocurable polymer. When the mold is removed we obtain a patterned polymer on the substrate (figure 2.15). As with all contact lithography techniques, in SFIL also there can be problem of adhesion of polymer to the mold surface. This can be minimized by using release layers on the template which are non adhesive to polymers [19]. Incomplete displacement of polymer leaves a residual layer on the surface which is usually removed by descuming RIE etch step. This step...
creates broadening of the resist openings and thus can be limiting factor as dimensions are scaled down.

Figure 2.15: (A) Schematic illustration of the procedure for step-and-flash imprint lithography (SFIL). (B) SEM images of 40 nm lines (C) 20 nm wide lines patterned by SFIL.

The SFIL process patterns features down to at least 20 nm across a field size of 6.25 cm² per molding step [93]. Step-and-flash imprint lithography uses a rigid, transparent mold to print features at a constant temperature (22 °C) with low applied pressures (<1 lb/inch²). The low printing pressure allows imprinting on brittle substrates and reduces distortion caused by flexing of the mold or substrate. Use of transparent molds allows capability to align the imprinted layer to other layers in fabrication process sequence. The alignment accuracy in SFIL has been reported as high as (10 nm (3σ)) [94].
2.7 Nanoimprint Lithography (NIL)

Nanoimprinting lithography is similar to step and flash imprint lithography. The difference is that this technique uses the thermoplastic polymer instead of photocurable polymer and molds are not needed to be transparent [95, 96]. In this process the thermoplastic polymer coated on substrate is heated above glass transition temperature, and then the hard mold is pressed at high pressures till the mold is in complete contact with the substrate. After pressing the mold for predetermined time, substrate and the polymer is allowed to cool and then the mold is removed (figure 2.16).

Figure 2.16: Schematic illustration of nanoimprint lithography (NIL). The SEM images (B, C) show typical NIL experimental results. (B) Fresnel zone plates with a 125 nm minimum line width (C) metal dots with 10 nm diameter with 40 nm periodicity. (D) Dark-field optical image of 1 um gate length MOSFET fabricated by using NIL at all four lithographic levels (E) The SEM image of a 60 um channel-length MOSFET with overlay accuracy of 0.5 um in both X and Y

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Nanoimprint lithography can mold a variety of polymeric materials and pattern features as small as 5 nm \cite{97,98} and aspect ratios up to 20 (height-to-width) \cite{99} This process has been used to pattern components for a range of microelectronic, optical, and optoelectronic devices \cite{100, 101}. For example, gate lengths in a MOSFET have been defined by NIL with a minimum feature size as small as 60 nm \cite{102}. Heating and cooling cycles and high pressures (15-130 bar), applied during embossing, produce stress and wear on nanoimprint molds and lifetime of the mold is significant issue. This stress also presents a challenge for alignment during multilayer fabrication. In Nanoimprint lithography it’s been observed that the recipe for successful nanoimprinting depends on the pattern density as it directly affects the thermal distribution and resist reflow. There is also the problem of residual resist layer, sticking of resist to the mold, and incomplete contact of hard molds with the substrate.

### 2.8 Solvent-Assisted Micromolding (SAMIM)

SAMIM is another form of imprinting technique which does not use high temperature processes for transferring patterns from the mold onto a polymer. Instead this technique, as name suggests uses a solvent to dissolve the polymer which fills the gap of the mold and takes its shape \cite{103}. The solvent subsequently evaporates and the polymer retains the shape of the mold as it hardens (figure 2.17). The mild processing conditions of SAMIM are compatible with patterning polymer-based distributed feedback lasers \cite{104} and organic light-emitting diodes (OLEDs) \cite{105}. Since in SAMIM soft masks are used, the dimensional stability of this method is lower than that of the methods using hard mask. As with other imprinting techniques this technique also leaves residue between isolated features and requires descuming step. Solvent absorption can distort PDMS molds and number of repeats
is very limited using single mold. Line widths as small as 60 nm and aspect ratios of at least 1:1 have been patterned in a Novolac photoresist and poly (vinyl pyridine) by SAMIM [106].

Figure 2.17: (A) Schematic illustration SAMIM (B) AFM image of 60 nm wide lines patterned using SAMIM. (C) SEM image of square pyramidal structures showing a well-defined apex with 20 nm radius of curvature molded using SAMIM.

2.9 Crystalline Lattice step edge assisted lithography.

Material deposition at atomic step edges by electrodeposition gives nanowires on highly oriented graphite (HOPG) (Figure 2.18) [14,107] due to high surface reactivity at these edges facilitating the electrochemical reaction [108-110]. This approach can generate nanowires, as small as 15 nm, of metals (e.g., Ag, Pd, Cu, and Au), oxides (e.g., MoOx and Cu₂O), and semiconductors (e.g., MoS₂ and Bi₂Te₃) [14, 107, 111-115]. Due to surface dependent electrochemical reaction rate, the growth of nanowires by this process is random and uncontrolled. This can give wires with different diameters, surface roughness depending on
how fast or slow the reaction is at any particular step edge of crystalline lattice.

![Diagram of Palladium Mesowire Array (PMA)-based hydrogen sensor or switch]

Figure 2.18: (A) Schematic diagram of a Palladium Mesowire Array (PMA)-based hydrogen sensor or switch. (B) SEM image [400 um (h) by 600 um (w)] of the active area of a PMA-based hydrogen sensor. (C) PMAs were prepared by electrochemical step edge decoration at graphite surfaces and transferred to a cyanoacrylate film.

2.10 Lithography using Spacers

If the material is conformally deposited on the steps and directionally etched till material on the top of the steps is completely etched then we get the residual material on the sidewalls of the steps called spacers. This selective material on the sidewalls can also be obtained by the shadow evaporation of material like metals. Selective etching of the substrate generates narrow, vertical structures [116] which can be subsequently used to etch features into
underlying material. White et al. used this method to fabricate an array of 30-nm wide lines of silica with heights of 300 nm [117] (figure 2.19).

![Figure 2.19: (A) A schematic of the fabrication sequence for making high aspect ratio metal lines for wire grating optical polarizers (B) SEM of the SiO$_2$ structure fabricated with 30 nm width at 320 nm pitch.](image)

Depositing a low-temperature oxide uniformly over topographic features and etching the substrate by RIE can also pattern nanoscale features at the edge of each feature called spacers [118]. Somorjai et al. used this method to generate 10-nm wide vertical structures (Figure 2.20) [119]. This technique is often called size reduction lithography or alternatively a spacer technique.
Figure 2.20: (A) Schematic of size reduction lithography (B) Cross section of the 120 nm thick LTO deposited on the polysilicon step (C) Cross section view after the top LTO and poly-si layer have been etched away from the structure in part B (D) 20 nm metal nanowire made from size reduction lithography from C

Chou et al. demonstrated series of 10 nm fins by using the spacers formed along the side walls of the mesa and using this as the mask to etch the layer underneath it (figure 2.21). In this example the mesa is etched in the SiGe layer and 10nm high temperature oxide was conformally deposited on this structure. The HTO layer is etched selectively with respect to SiGe using RIE thus forming a spacer. The SiGe layer is then etched away forming 10 nm fin used as the hard mask to pattern the layer underneath it. Each of these techniques is limited in its ability to pattern arbitrary features by the features whose edges are being used and by the initial use of photolithography. Photolithography and electron-beam lithography can pattern
regular arrays of topographic features, and nanoscale structures generated at the step edge of these features are regularly spaced. Patterning intersecting (crossing) lines of metal using these methods is, however, not straightforward.

2.11 Lithography by controlled undercutting

In another edge defined technique, patterned arrays of nanostructured trenches can be fabricated by the controlled undercutting of the film by wet etch masked by photolithographically defined topographic features, followed by deposition of a thin film (Figure 2.22) [120] and lift-off the masking material. This method has patterned well-defined trenches with lateral dimensions as small as 50 nm. Controlled undercutting of photoresist has also patterned 50-nm wide islands of gold for growing ZnO nanowires [121].
Figure 2.22: (A) Schematic illustration of the use of controlled undercutting to pattern trenches with lateral dimensions as small as ~ 50 nm (E) SEM of cross-section of 75 nm wide trenches transferred into Si substrate

2.12 Phase-Shifting Edge Lithography

Near phase shifting photolithography is a technique in which the vertical edges of a transparent, topographically patterned substrate induce abrupt changes in the phase of incident, collimated light over short distances creating narrow regions of constructive and destructive interference to project “dark” or “bright” regions of incident light onto the surface of a photoresist (figure 2.23) [13, 122-127]. The smallest lateral dimensions are produced when the light has a phase shift of $\pi$ radians at the photoresist-mask interface (Figure 35A). Phase-shifting edge lithography is limited by the requirement that the mask must be transparent and situated as close as possible to the films of photoresist, ideally in contact. Instead of using the hard quartz mask which are expensive and tendency to be contaminated
when in contact, a much less elastomeric PDMS mask is used. A PDMS mask spontaneously and nondestructively achieves conformal contact with the photoresist and eliminates any gap between the mask and the resist. Near-field phase-shifting photolithography has been used to fabricate a number of simple patterns, such as rings and lines of photoresist and the smallest featured patterned is 30 nm wide. Phase-shifting lithography using a soft, conformal mask requires that the mask have vertical, straight sidewalls. Distortions in the mask broaden the features in the photoresist.

Figure 2.23 (A) Schematic illustration of Phase-shifting edge lithography using topographically patterned composite PDMS stamp (B) 30 nm wide rings and (C) 50 nm wide lines patterned using phase shifting edge lithography
2.13 Superlattice Nanowire Pattern Transfer

Alternating layers of films deposited on the flat wafer surface is used in SNAP process. These wafers are cleaved and one material is selectively etched. The edges of these cleaved wafers give line-width patterns, width of which depends on the film thickness. Multilayered structures grown by molecular beam epitaxy (MBE) are the most common substrates for this approach to nanofabrication. The grooves obtained along the edges are partially coated with a metal by selective angle deposition to generate parallel nanowires. Transfer of the metal wires to a silicon wafer is performed by contacting the metal-coated GaAs/AlGaAs superlattice to a heat-curable epoxy film 10 nm thick, supported on an oxidized silicon wafer; the epoxy served as an adhesion layer.

Figure 2.24 (A) Schematic illustration of a method to create nanowires by Superlattice Nanowire Transfer Process (B, C) SEM images showing the edge of the MBE-grown substrate with an array of deposited Pt nanowires (C) shows 10 nm diameter nanowire with pitch of 60 and 30 nm (D) nanowire cross-bar array
This process is called Super Lattice Nanowire transfer process (SNAP) [10]. Modifying the thickness of each layer of the substrate will change the spacing between the nanowires and the width of the nanowires. Free-standing Pt nanowires have been fabricated with diameters down to 8 nm at a pitch of 16 nm [19]. Parallel nanowires supported on adhesive substrates can be overlapped perpendicular to each other to create a cross-bar array (Figure 2.24D). An MBE-grown substrate consisting of alternating layers of AlGaAs and GaAs was also used to fabricate an array of field-effect transistors (FETs) with 20-nm gate lengths [128]. SNAP process, although has great scaling capability, it is restricted to making only linear nanowire array and wafer-scale routing is not possible.
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CHAPTER 3

3. THEORY AND DEVELOPMENT

As mentioned in previous section PEDAL process involves three critical steps. These are Trench etch, thin film deposition, and planarization. The profile of the template obtained depends on characteristics of each of these steps. This chapter discusses in detail requirements for each of the process steps as well as gives an insight on various processes involved in this research. In order to understand these processes various experiments have been carried out and the results are analyzed to design a successful process. These experiments were based on initial research presented in various publications, but due to difference in application, new experiments had to be designed to get the data that can be helpful in developing processes pertaining to PEDAL. Different conditions for these processes, ideal as well as non-ideal, have been analyzed to reach concrete conclusions on improving the quality of templates. Ideal cases of each of these processes i.e. perfectly vertical trench sidewalls, totally conformal atomically smooth film deposition and highly non-selective planarization recipe will yield a template which has line widths equal to thickness of thin films, sidewalls vertical and lines planar. In this chapter, tolerance of PEDAL process with respect to non-ideal conditions of each of these processes has been studied by numerical simulations. These non-ideal conditions include slope in trench sidewalls, totally non-conformal film deposition process and highly selective planarization processes. Design considerations to minimize or overcome the effect of non ideal processes on final template profile have also been suggested for each step.
3.1 Trench/Edge formation

Trench edge formation is the first key step of fabricating nanowire template using PEDAL process. In PEDAL process, initial route of the nanowires is defined by conventional optical lithography which in this research was i-line lithography tool. After patterning the photoresist, subsequent etch step to define trenches in the silicon wafer is one of the deciding factors of the final profile of the nanowire template and metal nanowires. In this section I have discussed various aspect of trench/ edge formation which will include the important requirements of this step, various experimental approaches of etching trenches and the effect of the non-ideal trench profiles.

3.1.1 Requirements of Trenches in PEDAL process

There are three important requirements for trenches in PEDAL process are (i) vertical side walls (ii) edge and surface roughness (iii) routing ability. In the following sections I have elaborately discussed effect of each of these requirements

3.1.1.1 Vertical trench sidewalls

PEDAL is an edge defined process and topography of arrays of nanowires fabricated along edges greatly depends on topography of trenches. As shown in figure 3.1, if trench walls are non-vertical, lines obtained on template will have sloped sidewalls. The template thus obtained might be unsuitable for nanoimprinting as it will make the mold release difficult, causing distortion of imprinted resist.
Figure 3.1 (a) Sloped side walls of trench gives sloped side walls of the template lines (b) SEM of cross-section of template obtained by PEDAL process shows sloped sidewalls of lines (c) Nanoimprint resist coated on substrate is heated and template is pressed at a certain pressure \( t < d \) (d) Imprinting causes resist reflow in the spaces on template (e), (f) Template removal causes resist removal.
where \( a \) = Thickness of deposited film,

\( \theta \) = Trench sidewall angle

\[ w = \frac{a}{\cos \theta} \] \hspace{1cm} \text{Equation 1}

\[ s = \frac{a}{\cos \theta} \] \hspace{1cm} \text{Equation 2}

Figure 3.2 (a) Nanoimprinted line width and (b) space width increases with increase in sidewall angle of the template.
Graph in figure 3.2 shows dependence of imprinted lines and spaces on side wall angle $\theta$ of lines on the template which is given by relations in equations 1 and 2. The analysis is done for 250 A wide template lines and spaces and for trench sidewall angle varying from 0 to 15 degrees. In this discussion resist left on substrate after template removal is called line and the area from where resist is removed is called space. It’s assumed that the template does not stick to the sample and can be removed, and while nanoimprinting there is no movement of mold in horizontal direction, thus eliminating resist distortion caused by mechanical motion of template and substrate in horizontal direction. From graph in figure 3.2 it’s evident that as sidewall angle increases, line and space width increases. For ideal condition i.e. sidewall angle of 0 degree, lines and spaces obtained after nanoimprinting are of same width as the thickness of deposited films. Dimensions of lines and spaces obtained after nanoimprinting does not depend on depth of selective etch $d$ or thickness of the imprint resist $t$, given $t<d$. As shown in figure 3.1 (f), it is possible that nanoimprinting using nanowire template with lines having nonvertical side walls will give tapered profile of resist left on the substrate. This resist profile might be unsuitable to mask the substrate in reactive ion etching in which reactive ions will tend to etch resist more at the bottom, causing increase of etched width and decrease in spacing. The tapered resist profile can be used for lift-off of thin metal films permeable to lift-off solution. From the graph we can see that width of imprinted lines and spaces increases with increase in sidewall angles. Simulation results show that trenches obtained in RIE recipes with side wall angle of 15 degree causes just 3% increase from target design widths which is the thickness of deposited films. This suggests that non-vertical sidewalls of trench can still provide templates suitable for imprinting, although maximum allowable sidewall angle depends on design tolerance.
Figure 3.3 (a) (b) Directional metal deposition by e-beam evaporation technique on template with non-vertical trench side walls (c), (d) Lift-off of the metal by wet etching one layer which leaves narrower nanowires and wider spaces than template lines and spaces.

\[ w = a \cos \theta - d \tan \theta \] Equation 3
\[ s = a \cos \theta + d \tan \theta \] Equation 4

where \( a \) = thickness of film deposited,
\( \theta \) = trench sidewall angle, \( d \) = depth of selective wet etch
Figure 3.4 (a) Width of nanowires obtained after lift-off of metal on template with nonvertical sidewalls decreases and (b) spacing increases with increase in trench sidewall angle.
Hard lift-off of thin metal on nanowire template with sloped trench sidewalls will give metal nanowires on the template without using nano-imprinting, however, width $w$ and spaces $s$ of the metal nanowires in an array will differ from target line-width and space-width value. It is assumed here that there is complete removal of metal deposited on the material being etched in lift-off solution. It’s been also assumed that metal film thickness is very small as compared to line widths and there is insignificant change in the width of a metal nanowire across its height. The dimensions of metal lines left on template after lift-off is given by equations 3 and 4. Graph in figure 3.4 shows that as sidewall angle increases, width of metal nanowires left on the template after lift-off decreases and spacing increases, with pitch remaining same. Widths of lines and spaces obtained after lift-off not only depend on sidewall angle but also on depth $d$ of selective wet etch. Analysis has been done for sidewall angle varying from 0 to 15 degrees and for depth of selective wet-etch from 10 nm to 100 nm. Standard deviation in widths of nanowire and spaces obtained after lift-off is more for higher values of depth. Lift-off of metal done on template with sidewall angle of 0 gives metal nanowires with width $a$ and spacing $a$ same as initial design irrespective of the depth of selective wet etch. Lift-off done on nanowire template with 15 degree sidewall angle and 100 nm depth of selective wet etch, will give 90 % deviation from initial design widths. This deviation decreases with decrease in depth of selective wet etch. Lift-off done on template with 15 degree sidewall angle and 10 nm depth of selective wet etch will give 6.8 % deviation form initial design values. This deviation decreases to 2.8 % for the depth of 5 nm. Hence in ideal lift-off conditions, PEDAL template with sloped sidewalls can be used for hard lift-off, and the deviation of width of lift-off nanowires and spaces can be controlled within 3% if depth of selective wet etch is kept less than 5 nm.
3.1.1.2 Edge and surface Roughness

Photolithography and etching process used to define trenches should have minimum edge and surface roughness as in the sub-25 nm scale, roughness in nanometer range, can propagate through the line width structures affecting linearity of nanowires as shown in figure 3.5.

Figure 3.5 (a) Step edge roughness causes nonlinearity of the template lines and spaces
(b) SEM of the top view of the template obtained by PEDAL process using trench with rough step edges formed by high energy RIE etch process.

One of the obvious causes of step-edge roughness is photolithography process used to define route in photoresist layer. This can be true for step edge roughness in dimensions above the resolution of i-line photolithography process which is used to define route in resist. This also suggests that for edge roughness in nanometer range, smaller than resolution of i-line lithography process, possible cause is not photolithography but etching steps used for etching trenches. Anisotropic etching of trenches can be done by RIE process which etches substrate using high energy reactive ion etching, or by the wet etch like high temperature KOH etches.
In RIE process surface roughness of the etched feature greatly depends on the physical etching mechanism and increases with increase in energy of reactive ions. In anisotropic etch process using KOH solution [1-5], edge roughness depends on the concentration and temperature of wet etch solution; and alignment of the features on the mask to the substrate. Figure 3.6 shows the rough step edge obtained in KOH wet etch solutions due to slight misalignment of trench edges.

![Figure 3.6 Trenches form rough edges after etching in 40% by weight KOH solution at 70°C due to misalignment of trenches.](image)

**3.1.2 Etch processes for defining trenches**

In this section I have discussed two different approaches to etch trenches in silicon wafer. One approach is using reactive ion etching mechanism which involves dry etching of the substrate using highly reactive ions generated by applying high radio frequency voltages across two electrodes in high vacuum chamber. Other approach is using wet etch solutions, typically potassium hydroxide solution at high temperatures, which has preferential etching of silicon atoms oriented in certain planes [6-10].
3.1.2.1 Reactive Ion etching- Theory

Typically in semiconductor industry, dry etches are used to define high aspect ratio vias and trenches. It’s been shown in research elsewhere [11] that Deep Reactive Ion Etch (DRIE) and Inductively Coupled Plasma Reactive Ion Etches (ICPRIE) can achieve the side wall angles of 89.5 for high aspect ratio trench etches. Gas composition used for high anisotropic etches are $\text{C}_4\text{F}_8/\text{CO}/\text{O}_2/\text{Ar}$, $\text{CHF}_3/\text{CF}_4/\text{CO}/\text{Ar}$, $\text{SF}_6/\text{HBr}/\text{O}_2$. In this research SEMIGROUP 1000, a parallel plate reactive ion etcher was used. Gases available on this system for experimentation were CHF$_3$, O$_2$, SF$_6$, and Ar.

![Diagram](image)

Figure 3.7 (a) Isotropic etch component of RIE process causes undercut (b) Polymer byproduct redeposition reduces undercut by preventing further etching of sidewalls (c) Excessive byproduct redeposition at the bottom of the trench causes tapering.
To get a vertical sidewalls, CHF$_3$ gas is used instead of SF$_6$ as SF$_6$ has high isotropic etch property (figure 3.7 (a)). Fluorocarbon gases with high carbon content improves sidewall angle of etched features as polymer byproducts of RIE reaction deposit on sidewalls and prevent it from etching further and preventing undercut (figure 3.7 (b)). However too much fluorocarbon also causes tapering of trench because of build-up of fluorocarbons at the bottom interferes with etching mechanism. Oxygen is used in the plasma to passivate trench side walls from chemical etchants which improves the anisotropic property of etch process. Too much oxygen causes dilution of reactive etchants and thus slows down the etch rate. It also causes etching of the polymer byproducts formed by fluorocarbon gases and reduces the shielding effect. Hence to get a highly anisotropic etch there has to be a good balance between the sidewall passivation by oxygen, rate of polymer build-up and etching of polymer byproduct by oxygen and dilution of active etchants.

CHF$_3$ reacts with the underline substrate to form CF$_2$ which can react with atomic fluorine to form CF$_3$ thus decreasing active fluorine concentration. Surface modification during etching processes may occur because of formation of unstable silicon compounds. There are several possibilities for surface reactions which provide etching action of Si by CHF$_3$ plasmas [12, 13]. The direct reactions are

\[ e^- + CHF_3 \rightarrow CHF_2 + F + 2e^- \]

\[ Si + 4F \rightarrow SiF_4 \]
In addition to stable tetrafluorosilane, other fluorosilanes, such as SiF$_3$ and SiF$_2$ may be formed. These fluorosilanes are unstable and may decompose according to disproportion reaction, given below, eventually forming stable tetrafluorosilane.

\[ 2\text{SiF}_2 \rightarrow \text{Si} + \text{SiF}_4 \]

\[ 4\text{SiF}_3 \rightarrow 4\text{Si} + 3\text{SiF}_4 \]

Etch rate of silicon decreases with increase in CHF$_3$ due to mass transport limitation of the reactive species across the deposited layer and surface modification via redeposition of reaction products discussed above. Addition of O$_2$ to CHF$_3$ plasma causes reduction in the recombination of CHF$_2$ with Fluorine atoms, as in the presence of oxygen, formation of CO and CO$_2$ is more favored than the fluorocarbon recombination. This will increase the etch rate initially but at higher oxygen concentration, etch rates reduces due to the dilution of reactive fluorine atoms, as observed in experiments discussed in section 3.1.2.2.

Figure 3.8 (a) Physical etching of surface by low energy ions shown by path 1 and physical etching of high energy ions shown by path 2 (b)Etching of surface by reactive ions with high mean free path shown by path 1 and by ions with low mean free path shown by path 2.
Reactive ion etch mechanism has two etching components, chemical etching component and physical etching component. Chemical etching is governed more by reactive atoms than ions. Ions and heavy nonreactive atoms play major role in physical etching mechanism. Anisotropicity of the RIE etch mechanism can be greatly increased by increasing the physical etching component as it’s more directional and depends on the energy and the arrival angle of impinging ions and atoms. The kinetic energy of impinging species can be increased to increase physical etching component, by increasing RF power or applied voltage. However at high RF power, reactive ions can have sufficiently high energies after first collision with substrate, to cause the sputtering even at side walls as shown in figure 3.8 (a) making etching less anisotropic. Very high energy ions also cause increased surface roughness of the substrate due to high impact. Hence there is need to find the optimum energy which can give good anisotropic etch as well as less surface roughness.

High mean free path of the ions reduces scattering of impinging reactive atoms and ions in the plasma, thus restricting their arrival angle at the trench side wall within 90 degrees (figure 3.8 (b)). Mean free path of impinging ions is inversely proportional to pressure and can be increased by reducing the pressure. At higher pressures, mean free path of arriving ions is comparable to trench dimensions, and therefore there is high probability of scattering of impinging ions due to collisions. At high pressures, arrival angle of reacting species at trench sidewalls increases to 180 degrees as shown in figure 3.8(b) and gives less control over the directionality of etch.
3.1.2.2 RIE Experiments

The theory discussed in previous sections gives us good understanding of variables to be tuned in order to get good anisotropic trench etches. These variables are relative concentration of fluorocarbon gas and oxygen gas, RF power and pressure. As mentioned earlier, availability of gases for experimentation was restricted to only CHF$_3$, O$_2$, Ar and SF$_6$. Hence in the following experiment attempts have been made to get trenches with vertical side walls using fluorocarbon gas CHF$_3$ and sidewall passivating oxygen gas. All experiments were done at low pressure of 30 mTorr and intermediate power of 150 W as low pressure gives long mean free path of reactive species and high power increases the directionality of the physical etch. The parameters changed were relative concentration of CHF$_3$ and oxygen to determine the dependence of anistropicity on relative concentration of these gases. SEMs of cross-sections of trenches obtained for four different relative compositions of CHF$_3$ & O$_2$ is shown in figure 3.9 and measurements are shown in graph in figure 3.10. Minimum sidewall angle of the trench is obtained for the RIE recipe using 20 sccm CHF$_3$ and 20 sccm O$_2$ at 30 mTorr and 150 W. The sidewall angle measured was 15 degrees. If this etching method is incorporated in the PEDAL process and template obtained is used for lift-off, then from the previous analysis we know that for 10 nm depth of selective wet etch 10 nm we will get 6.8 % deviation form initial design values. This deviation decreases to 2.8 % for the depth of 5 nm. If the template with 15 degrees trench sidewall angle is used for nanoimprinting, then from analysis done previously, there will be just 3 % increase in imprinted lines from initial design widths, which is the thickness of films deposited. So depending on the design tolerance, RIE recipe providing 15 degree sidewall angle can still be
used to make templates suitable for nanoimprinting or lift-off, although maximum allowable sidewall angle depends on design tolerance.

Figure 3.9: Trench cross-section obtained with RIE etching at 30 mTorr and 150 W using CHF$_3$:O$_2$ ratio equal to (a) 20 sccm: 20 sccm (b) 20 sccm: 5 sccm (c) 10 sccm: 20 sccm (d) 20 sccm: 10 sccm.
Figure 3.10 Shows the sidewall angle and etch rate of the trenches etched in a-Silicon using RIE at 30 mTorr and 150 Watts. The results above are for CHF₃:O₂ equal to 20 sccm: 40 sccm, 20 sccm: 20 sccm, 20 sccm: 10 sccm and 20 sccm: 5 sccm

3.1.2.3 Trench Etch using KOH solution

Since RIE processes using available gases didn’t give ideal results on anisotropic etching of trenches, other set of experiments were carried to analyze anisotropic etch using wet etchant like hot KOH solution. KOH solution shows preferential etching of silicon {100} and silicon {110} plane over silicon {111} plane; with relative etch rates depending on KOH concentration and temperature [4, 5-9]. This anisotropic wet etch property of KOH solution can be used to define trenches with steep vertical sidewalls on <110> wafers, because <110> plane intersect <1-11> and <-1 1 1> plane at right angle along (1 -1 -2) and (1 -1 2) axis respectively as shown in the figure 3.11.
Figure: 3.11 (a), (b) Shows planes <-111> and <1-11> intersecting <110> at right angles along (1-12) and (-112). The angle between these two axes is 70.53. (c), (d) shows the SEM of trench with vertical sidewalls obtained on Si <110> wafer after etching in 40 % by wt. KOH solution at 70 C

The axis’ at which <110> plane intersects <1-11> and <-1 1 1> plane at right angle i.e. (1 -1 -2) and (1 -1 2) directions lie at an acute angle of 70.53 degree and obtuse angle of 109.47 degree rather than right angle[4]. Hence the routing ability of lines fabricated by PEDAL process is restricted to the scheme shown in figure 3.12 if KOH solution is used for defining trenches.
Figure 3.12: Shows the routing scheme of the nanowires if anisotropic KOH wet etch is used for defining trenches in Si<110>. The routes are aligned along (1-12) and (-112) directions.

Anisotropicity of the trenches etched in the above route will only be obtained if the fabrication process used for opening windows in the masking layer on Silicon <110> substrate produces sharp acute corners or obtuse corners. However in actuality, there is always the possibility of rounding of the corners as shown in figure 3.13 (a). This rounding of corners is observed more in acute corners than obtuse corners due to the resolution of the photolithography process, which in this project is i-line photolithography, as well as due to subsequent etch processes used in opening the window in masking layer like photoresist develop process and silicon nitride etch process. In linear regions of the route, it’s easy to obtain vertical sidewalls of trenches by proper alignment of mask to substrate, however at or around the corners of the route, nonvertical sidewalls are observed due to rounding of etched
corners. This exposes various planes other than vertical <1-11> and <-111> plane to the KOH solution, like <113>, <771>, <11-1>, <111> planes which are also etched slower than <110> plane as shown in the graph in figure 3.16 [7]. The step profile obtained around corners is either a fastest etching or the slowest etching plane in KOH solution. From research published elsewhere [4, 7, 8] it’s been experimentally observed that in KOH solution the etch fronts are {113} planes at masked acute corners and {771} planes at masked obtuse corners.

![Figure 3.13](image1)

**Figure 3.13:** (a) shows ideal mask and non-ideal, mask for routing using anisotropic KOH wet etch for defining trench on Si<110>. Rounding of acute corners due to limitation of lithography and subsequent mask defining etch steps (b) Rounding of acute corners exposes non-vertical etch fronts like <-111> and <111> planes.

In this research etch fronts around open acute corners are found to be <11-1> and <111> planes which intersect the <110> plane at 57.7 along (-110) direction as shown in figure 3.14 (a). The results were verified by doing the geometrical calculations as shown. However at
open obtuse corners, the etch fronts are observed to be <1-11> and <-1 1 1> plane which as mentioned earlier intersect the <110> plane at right angles. The reason for this observation might be that at acute open corners the distance between adjoining edges, a and b (figure 3.13 (a)), reaches dimensions less than the resolution of photolithography tool farther to the point of intersection and hence causes significant rounding of acute open corners.

Figure 3.14 (a) SEM of the trench etched in Si<110> wafer using 40 % by weight KOH solution at 70 C. <111> and <11-1> etch fronts are exposed at acute open corners (b) calculations confirming <111> and <11-1> etch front planes.
This rounding of corners exposes \{11-1\} and \{111\} planes instead of \{1-11\} and \{-111\} plane to KOH etchant, thus giving sloped trench sidewalls. However at obtuse corners, the distance between edges b and c reaches dimension less than the resolution of photolithography very near to the point of intersection causing less rounding effect. As a result \{11-1\} and \{111\} planes are not significantly exposed to the etchant, and we get \{1-11\} and \{-111\} planes as etch fronts giving the vertical sidewalls at the open obtuse corners. At the masked acute and obtuse corners, more etch front planes like \{771\} and \{113\} planes were observed as shown in the figure 3.15.

![Figure 3.15: SEM of the top view of the trench profile obtained in Si\{110\} using 40 % by wt. KOH solution at 70 C. Dotted lines denotes edges of mask opening aligned along (1-12) and (-112) directions. Nonvertical sidewalls are observed along the corners of the route](image-url)
Again here it is reiterated that emergence of etch front planes depend on the reaction rate of different planes exposed to KOH wet etch solution, with slowest etching planes deciding the trench wall profile by acting as etch stop and fast-etching planes deciding the trench profile by reactively eroding.

![Graph showing etch rates of different planes relative to {113} plane in Si <110> wafer using KOH wet etch solution at 70 C](image)

**Figure 3.16:** Shows etch rates of different planes relative to {113} plane in Si <110> wafer using KOH wet etch solution at 70 C [ref 7].

### 3.2 Thin film deposition

Once trench with steep vertical sidewalls is etched on Silicon wafer by anisotropic wet etch of silicon or by anisotropic reactive ion etching of silicon, the deposition process of thin films like silicon nitride and amorphous silicon is a deciding factor in determining the width, spacing, and roughness of the nanowire template. Important properties of the deposited films for defining templates using PEDAL process are surface roughness, conformality, wafer scale uniformity, run to run uniformity, and mechanical strength.
3.2.1 Surface roughness

In PEDAL technique, film deposition process used to deposit alternate layer of thin films should provide thin films with minimal surface roughness. As shown in figure 3.17, high surface roughness of deposited films not only will increase edge roughness of line and spaces on the template but will also increase roughness of sidewalls of those lines. Increased sidewall edge roughness is one of the important reasons for sticking of molds in nanoimprinting causing distortion of the imprinted features. The surface roughness of deposited material greatly depends on the deposited material, deposition chemistry and deposition conditions. Low pressure chemical vapor deposition reactor with Silane gas will deposit films with more surface roughness at 635 C (polysilicon deposition) than at lower temperatures 535 C (amorphous-silicon deposition). However, dichlorosilane (DCS) and ammonia gas in the reactor will deposit smoother films even at higher temperatures like 775 C (silicon nitride deposition). In PEDAL process, amorphous films with surface roughness less than 10 Å is preferred to fabricate sub-25 nm wide nanowires and spaces to keep critical dimension variation due to film roughness less than 5 %.

Figure 3.17: Surface roughness of the films directly affects the edge roughness and surface roughness of lines on the template fabricated by PEDAL process.
Figure 3.18  AFM of (a) Silicon wafer surface (b) LPCVD Polysilicon on Silicon (c) LPCVD Silicon Nitride on Silicon (d) LPCVD Amorphous Silicon on Silicon (e) LPCVD Silicon Nitride on LPCVD amorphous Silicon on silicon (f) LPCVD Amorphous Silicon on LPCVD Silicon Nitride on Silicon
Measurements of surface roughness done using AFM are listed in Table 2. From measurements amorphous silicon and silicon nitride are recognized as excellent candidate for PEDAL process to fabricate sub-25 nm nanowires, as their surface roughness is less than 6 A. Polysilicon film has higher surface roughness of 16 A due to partial crystallization of amorphous films, and hence its use in PEDAL process is avoided.

**Table 3: Surface Roughness measurements of LPCVD deposited materials done using AFM.**

<table>
<thead>
<tr>
<th>Serial No</th>
<th>Material</th>
<th>Rms roughness (Angstroms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Silicon</td>
<td>0.7</td>
</tr>
<tr>
<td>2.</td>
<td>Polysilicon on Silicon</td>
<td>13.55</td>
</tr>
<tr>
<td>3.</td>
<td>Amorphous Silicon on Silicon</td>
<td>2.81</td>
</tr>
<tr>
<td>4.</td>
<td>Silicon Nitride on Silicon</td>
<td>5.86</td>
</tr>
<tr>
<td>5.</td>
<td>Amorphous Silicon on Silicon Nitride on Silicon</td>
<td>4.99</td>
</tr>
<tr>
<td>6.</td>
<td>Silicon Nitride on amorphous Silicon on Silicon</td>
<td>4.86</td>
</tr>
</tbody>
</table>
3.2.2 Conformality

Conformality is defined as the property of a deposited film to evenly cover a step. In LPCVD process, three general types of step coverage are observed for deposited materials as shown in the figure 3.19. A highly conformal film has even thickness along walls of a trench or step as shown in figure 3.19(a).

Figure 3.19: Step coverage of deposited films (a) Uniform coverage resulting due to long mean free path and low reactive sticking coefficient (RSC) of reactants (b) Nonconformal step coverage for long mean free path and high RSC (c) Nonconformal step coverage for short mean free path and high RSC.
In LPCVD deposition it has been shown that an important mechanism for transport of material into gaps, holes and for uniform step coverage is through multiple adsorption and re-emission of reactants from the surface as shown in figure 3.20, i.e. from precursors having low reactive sticking coefficients (RSC). When such “reflections” occur many times, flux of the precursor to the surface inside a hole may differ very less from the flux onto a horizontal surface. Low RSC results in a uniform surface concentration all over exposed surface regardless of the topography and gives completely uniform thickness. Reactive sticking coefficients of precursors in LPCVD greatly depend on reactants as well as the reaction temperature, for example in LPCVD deposition of silicon the reactive sticking coefficient is given by Arrhenius relation shown below [19]

\[ \gamma_{SiH_4} = 0.054e^{-\frac{0.81eV}{kT}} \]

where \( \gamma_{SiH_4} \) is the RSC of silane molecule to Si surface

Figure 3.20 (a) Precursor with high reactive sticking coefficient (b) Precursor with low reactive sticking coefficient
Hence, for the same reaction chemistry, high temperature depositions can provide more conformal films than lower temperature depositions. This is attributed to higher kinetic energy of reactant molecules at higher temperatures and low RSC. For e.g. LPCVD reactor with silane gas will deposit films with less conformality at 535 C than at 635 C. Also high temperature deposition at around 775 using dichlorosilane and ammonia will provide highly conformal step coverage of silicon nitride.

Figure 3.21 Conformality measurements of (a) LPCVD polysilicon (b) LPCVD amorphous silicon (c) LPCVD silicon nitride

<table>
<thead>
<tr>
<th>Measurement</th>
<th>LPCVD Polysilicon</th>
<th>LPCVD Amorphous Silicon</th>
<th>LPCVD Silicon Nitride</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>1084.7 nm</td>
<td>762.71 nm</td>
<td>403.5 nm</td>
</tr>
<tr>
<td>b</td>
<td>1101.7 nm</td>
<td>619.2 nm</td>
<td>403.5 nm</td>
</tr>
<tr>
<td>c</td>
<td>1050.8 nm</td>
<td>728.8 nm</td>
<td>403.5 nm</td>
</tr>
<tr>
<td>β</td>
<td>5 degree (approx)</td>
<td>5 degree (approx)</td>
<td>5 degree (approx)</td>
</tr>
</tbody>
</table>
When the reactants adsorb and react without surface migration due to high RSC, the deposition rate depends on mean free paths (MFP) and arrival angles of the gas molecules. For reactants with MFP greater than dimensions of the step on substrate, arrival angle of molecules at the top surface is 180 and at side of the step arrival angle is less than 90 and varies given by analysis done later in this chapter. Due to this, film thickness at side walls is less than the thickness at top and we also get variable thickness of the films along trench sidewalls.

\[
\lambda = \frac{1}{\sqrt{2\pi a^2 n}} \quad \text{--- Equation 6}
\]

\[
\pi a^2 \times \text{cross-sectional area of colliding molecules of effective diameter } a
\]

\[
n = \frac{P N_A}{RT} \quad \text{--- Equation 7}
\]

\[
\lambda = \frac{RT}{\sqrt{2\pi a^2 P N_A}} \quad \text{--- Equation 8}
\]

where \( \lambda \) is the mean free path,

- \( n \) is density of molecules,
- \( \pi a^2 \) cross-sectional area of colliding molecules of effective diameter \( a \)
- \( N_A \) is the Avagadro’s number = \( 6.022 \times 10^{23} \) atoms/molecule

Reactants with low MFP will have arrival angle of 270 at the top edges giving thicker deposits at these edges as shown in the figure 3.19(c). The mean free path of a molecule is inversely proportional to pressure and directly proportional to temperature as given by equation 8 [16-19]. Hence for the conformal films, suitable for PEDAL process low pressure chemical vapor deposition is preferred. The diameter of the silane, dicholrosilane and ammonia molecule is less than 10 Angstroms [20, 21] which gives the MFP greater than 30.
microns for deposition pressure up to 300 mTorr and temperature more than 500 C. This value of MFP is several times higher than trench dimensions which are 2 to 5 microns wide and 2 to 5 microns deep. Hence for general numerical analysis of effect of nonconformal films, it’s been assumed that the MFP is very large.

3.2.2.1 Effect of Nonconformal film deposition on the PEDAL template profile

In PEDAL process highly conformal film deposition is preferred as it will give dimensions of lines and spaces on the template same as thicknesses of deposited thin films. Highly conformal films will also provide vertical side walls of lines on the template, suitable for nanoimprinting as nonvertical sidewalls cause distortion of imprinted features on substrate after mold removal. Nanowire templates with vertical sidewalls is also suitable for hard metal lift-off as the dimensions of lines and spaces on template can be preserved in metal nanowires obtained after hard lift-off. Nonconformal film deposition will give lines and with dimensions different from the target value which is thickness of deposited materials. As shown in figure 3.22 nonconformal film deposition also gives nonvertical sidewalls of lines on the template.

In LPCVD, mean free path of reactants is several times larger than the trench width and spacing on substrate which in this project is varied from 2 to 5 microns. The main cause for nonconformal film deposition in LPCVD is high reactive sticking coefficient of reactants. To study the effect of non-conformal film deposition and to evaluate the severity of requirement of conformal film deposition in PEDAL process, simulations were done for the condition with reactive sticking coefficient equal to unity i.e the reactants stick to the silicon surface on
first strike with no surface migration. In LPCVD deposition, for the condition where MFP of reactants is high and reactive sticking coefficient is unity, thickness of material deposited on any exposed surface is directly proportional to the arrival angle of reactants on that surface [22] as shown in the figure 3.23. Analysis done here considers that top surface film thickness obtained in nonconformal film deposition is given by equation 9. On trench sidewalls, thickness of first film deposited can be approximated by equation 11 and sidewall angle is given by equation 12.

Figure 3.22  (a) LPCVD with reactants having high reactive sticking coefficient gives non-conformal film deposition of the films in stack (b) Polymer is spin coated on the film stack (c) the stack and polymer is etched with non-selective RIE recipe (d) selective wet etch of a material in the stack.
Extending this relation of film thickness to the arrival angle, calculations are done for determining film thickness and sidewall angle for subsequent film deposition as given by equations 13 to 18. Results of simulations done for forty eight film depositions each with top film thickness of 250 A is shown in figure 3.24.

Figure 3.23 (a) LPCVD using reactants with high reactive sticking coefficient gives noncomformal films with thickness proportional to arrival angle of the reactants (b) Nonconformal deposition provides layers with different sidewall angle and thickness.
a = k\pi, \quad \text{k is some constant} \ldots \text{Equation 9}

\textbf{Layer 1}

\[ \theta_1 = \tan^{-1}\left(\frac{d}{w}\right) \ldots \text{Equation 10} \]
\[ b_1 = k\left(\frac{\pi}{2} - \theta_1\right) \ldots \text{Equation 11} \]
\[ \beta_1 = \tan^{-1}\left(\frac{d}{a/b_1}\right) \ldots \text{Equation 12} \]

\textbf{Layer 2}

\[ \theta_2 = \tan^{-1}\left(\frac{d + a}{w - a}\right) - \beta_1 \ldots \text{Equation 13} \]
\[ b_2 = k\left(\frac{\pi}{2} - \theta_2\right) \ldots \text{Equation 14} \]
\[ \beta_2 = \tan^{-1}\left(\frac{d}{a - b_1 - b_2}\right) \ldots \text{Equation 15} \]

\textbf{Layer 3}

\[ \theta_3 = \tan^{-1}\left(\frac{d + 2a}{w - 2a}\right) - \beta_2 \ldots \text{Equation 16} \]
\[ b_3 = k\left(\frac{\pi}{2} - \theta_3\right) \ldots \text{Equation 17} \]
\[ \beta_3 = \tan^{-1}\left(\frac{d}{3a/b_1 - b_2 - b_3}\right) \ldots \text{Equation 18} \]

where,

\(w\) is the width of the trench
\(a\) is the thickness of the deposited layer on top planar surface of the trench
\(\theta_i\) denotes the arrival angle of the molecules for layer \(i\) deposition at depth \(d\) in trench from the surface
\(\beta_i\) denotes the sidewall angle of the deposited layer \(i\) at depth \(d\) in trench from surface
\(b_i\) denotes the thickness of the deposited layer \(i\) at depth \(d\) in trench from the surface

Similarly, values of thickness and sidewall angles for subsequent layer deposition can be found out
Figure 3.24 (a) Run to run film thickness and (b) side wall angle at varying depth of planarization for trench width of 10 microns considering nonconformal LPCVD deposition process with high reactive sticking coefficient reactants and top surface film thickness of 250 A.
From simulations it’s evident that for a given width of trench, the thickness of film from run to run on sidewall inside trench varies most for shallow depth of planarization. This indicates that in PEDAL process if a-silicon and silicon nitride stack is planarized to smaller depths then widths of lines and spaces in an array will vary most. As shown in graph, the effect of nonconformal film deposition is less for deeper depth of planarization. Hence variation in the width of lines and space will be less if the stack is planarized to the greater depth. As mentioned earlier one of the most important consideration of a nanowire template is the sidewall angle of line-width structures on the template. The graph in figure 3.24 (b) shows that for smaller depth of planarization, the value of maximum sidewall angle obtained is more than the value of maximum side-wall angle for deeper depth of planarization. Hence a template obtained by planarizing at shallower depth not only has the high variation in the line-width dimensions but also higher sidewall angles. The graph in figure 3.25 shows standard deviation as the percentage of average width obtained by planarizing template at different depths for same trench width. Numerical simulation shows that as we increase the depth of planarization, the standard deviation as the percentage of average width decreases. Hence, in PEDAL process, choosing greater depth of planarization provide better results than choosing shallower depth of planarization.

The graph in figure 3.26 shows effect of trench width on the PEDAL template formed by nonconformal film deposition process with reactants having mean free path several magnitudes higher than the trench dimensions, as well as having reactive sticking coefficient equal to unity. The graph is based on the same relation as given by equation 9 to 18.
Figure 3.25. (a) Average line width, standard deviation and (b) side wall angle of lines and spaces at varying depth of planarization for trench width of 10 microns considering nonconformal LPCVD deposition process with high reactive sticking coefficient reactants and top surface film thickness of 250 A.
Figure 3.26 (a) Average line width, standard deviation and (b) side wall angle of lines and spaces for varying trench width and at depth of planarization of 5 microns considering nonconformal LPCVD deposition process with high reactive sticking coefficient reactants and top surface film thickness of 250 A.
The standard deviation of width of lines on template as percentage of average width of lines increases as trench width decreases. Hence to obtain PEDAL template with less dimensional variance wider trenches are preferable over narrower trenches. The graph in figure 3.26 shows that maximum sidewall angle of a line in nanowire template have higher values for narrower trenches, and sidewall angles of lines can be reduced by increasing the trench width.

The effect of non-conformal film deposition as we scale down t dimensions is studied by carrying out simulations similar to the analysis done above. Graphs in figure 3.27 show the average width and standard deviation of lines for the nonconformal deposition of materials of top surface thickness of 10 nm. The graphs shows same trend as that obtained for the nonconformal deposition of 25 nm thick films. Standard deviation as the percentage of average line width as well as sidewall angle will be small for deeper level of planarization and for wider trenches.

If we compare the effect of nonconformality on the PEDAL template formed by deposition of films of top surface thickness of 25 nm to that of the template formed by depositions of films with top surface thickness of 10 nm, we see that the standard deviation of film thickness as the percentage of the average width is smaller for the case with film thickness of 10 nm. Also maximum sidewall angle of the line-width of PEDAL template is less for the film thickness of 10 nm. This suggests that the quality of the mold obtained by PEDAL process, with regards to the variation as the percentage of the average width, and the sidewall angle, improves as we try to scale the dimensions of the line and spaces on template.
Figure 3.27 (a) Average line width , standard deviation and (b) side wall angle of lines and spaces at varying depth of planarization for trench width of 10 microns considering nonconformal LPCVD deposition process with high reactive sticking coefficient reactants and top surface film thickness of 100 A.
Figure 3.28 (a) Average line width, standard deviation and (b) side wall angle of lines and spaces for varying trench width and at depth of planarization of 5 microns considering nonconformal LPCVD deposition process with high reactive sticking coefficient reactants and top surface film thickness of 100 Å.
Nanowire templates formed by nonconformal film deposition might not be suitable for nanoimprinting, depending on nanoimprint methodology and process tolerance, as nonvertical sidewall angles can cause adhesion of molds to thermal nanoimprint resist resulting in distortion of lines and spaces as shown in figure 3.29. Dimensions of resist near the substrate surface are same as the top surface of lines and spaces on PEDAL template. However, nanoimprinting will cause tapering of thermal resist profile left on the substrate after removal of mold. As discussed in section 3.1.1.1, the quality of pattern transfer depends on etch process used to etch patterns onto underlying substrate. RIE etching of substrate may cause etching of resist at the bottom causing increase in width of patterns etched in the substrate. These nanoimprint templates obtained by PEDAL process involving nonconformal deposition of films can be used for hard lift-off of thin metal films permeable to lift-off solutions. As shown in the figure 3.30, nonvertical sidewalls and varying line widths in an array, will cause the deviation of nanowire widths from initial target value which is suppose to be same as thickness of deposited materials in ideal condition. The graph in figure 3.31 shows simulation results for lift-off of metal on PEDAL template in the best case scenario previously analyzed i.e. for the deeper depth of planarization, and wider trenches. The simulations are based on relations depicted in equations 19 to 24. As the depth of selective wet etch is increased, deviation of lift-off line-widths and spaces from initial template dimension increases. The pitch of lift-off nanowires and spaces remains same irrespective of depth of selective wet etch and is equal to the pitch of line-width structure on initial PEDAL template. From the analysis done above we can conclude that a PEDAL template can be used for lift-off for fabricating on-template nanowires, and lift-off will give less deviation of
nanowire widths and spaces from pre-lift-off template dimension if the depth of selective wet etch is minimum.

Figure 3.29 (a) Nanoimprinting using PEDAL template with lines having sloped sidewalls due to noncomformal LPCVD deposition process (c) Mold removal causes scraping of resist and tapering of resist profile on the substrate.
Figure 3.30 (a) e-beam evaporation of metal on the PEDAL template with lines and spaces having sloped sidewalls due to non-conformal LPCVD process (b) Best case of lift-off assuming the metal is completely lifted off from the surface which is being etched in the lift-off solution.
\[ s_1 = b_1 + d \tan \beta_1 \] 
Equation 19

\[ w_1 = b_2 - d \tan \beta_2 \] 
Equation 20

\[ s_2 = b_3 + d \tan \beta_3 \] 
Equation 21

\[ w_2 = b_4 - d \tan \beta_4 \] 
Equation 22

\[ s_3 = b_5 + d \tan \beta_5 \] 
Equation 23

\[ w_3 = b_6 - d \tan \beta_6 \] 
Equation 24

where \( b_1 \) and \( \beta_1 \) are the value of film thickness and sidewall angle from the analysis done previously for non conformal film deposition.

Figure 3.31(a) nanowire width and spaces (b) pitch, obtained after metal lift-off on PEDAL template in fig. 3.23 (b) for depth of selective wet etch 10 nm, 100 nm.
3.2.3 Deposition rate and wafer scale uniformity

Widths of lines and spaces in an array on PEDAL process defined template are decided by thickness of deposited films. Thinner the deposited films narrower are the lines and spaces. To fabricate an array of lines and spaces with same width it’s necessary that the deposition process be slow and repeatable. In a case with fast deposition process, the deposition time for thin films may be lower than the time needed for the gas flows in the LPCVD system to stabilize thus causing problem in repeatability of thin film deposition. Fabricating line-width structures with less than 25 nm pitch will require deposition rate to be less than 50 A/sec in LPCVD system as the system used in this project is reported to take around 3 minutes to stabilize. Slow deposition rate helps repeatability of the thin film deposition process thus reducing variance of widths of lines and spaces in an array.

At intermediate temperatures and low pressures, where deposition is reaction rate limited, the deposition rate is given by equation 25

\[
k_s = k_o e^{\frac{-E_a}{kT}}
\]

where \( k_s \) is the deposition rate,

\( E_a \) is activation energy

Hence decreasing deposition temperature gives lower deposition rate and better dimensional control. However as mentioned earlier in section 3.2.1, low temperature increases reactive sticking coefficient of reacting molecules given by equation 5, thus making films nonconformal. Hence there is a trade-off between better dimensional control by better
conformality at high deposition temperature, and better dimensional control by process repeatability using slower deposition process at lower temperatures.

In LPCVD reactor depositing polysilicon and amorphous silicon, Silane is used as the precursor gas. Formation of silicon from decomposition of silane gas is given by chemical reaction shown below

$$\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2$$

The deposition rate of silicon at three different temperatures is shown in the figure 3.32 below. The plot does not show Arrhenius relation at all temperatures. This is because at higher temperature the reaction becomes faster than the rate at which unreacted silane arrives at the surface. When this occurs and the reaction is said to be mass-transport limited and deposition rate depends on the reactant concentration, reactor geometry and the gas flow. When the rate of reaction is slower than the rate of reactant arrival, the deposition is surface-reaction limited, and critical variables are reactant concentration and temperature. From the graph shown in figure 3.32, it can be said that deposition at 535 C and 550 C are reaction rate limited with activation energy of value 1.72 eV, which matches well with values mentioned in literature [17]. However at higher temperature of 635 C where we see deviation from Arrhenius relation the reaction is mass transport limited. The deposition rate can also be decreased by decreasing partial pressure of precursor gases. In this research partial pressure of gases were not changed as the desired deposition rate of 43 A/min, required for repeatable deposition of thin a-silicon films as thin as 150A, was readily obtained at 535 C using 30 % silane (flow rate 60 sccm) with total flow rate of 200 sccm and at 130 mTorr.
Figure 3.32 Deposition rate of silicon at various temperatures in LPCVD system using 30% Silane gas at 130 mTorr with total flow rate of 200 sccm.

One of the most important requirements for wafer scalability of the PEDAL process for making an array of line-width structures is the uniformity of widths of lines and spaces in an array. The graph in figure 3.33(a) shows average a-silicon film thickness from run to run, deposited in 5.5 minutes using 30% silane gas at 535°C with total flow rate of 200 sccm at 130 mTorr. Wafer scale average amorphous silicon thickness varies from 225.6 Å to 237.7 Å, with overall average value of 231.9 Å. This suggests that average width of the line in array of line-width structure obtained in PEDAL process using this deposition process will be 231.9 Å in ideal case. The graph in figure 3.33(b) shows run to run average amorphous silicon thickness deposited using above mentioned process condition for 3 minutes. The wafer scale average amorphous silicon thickness varies from 126 Å to 142 Å with overall average value of 135.28 Å. This suggests that average width of a line in an array obtained in
PEDAL process using this deposition process will be 135.28 Å.

Figure 3.33: Run to run wafer scale average of LPCVD a-silicon film thickness at 535 C using 30% Silane at 130 mTorr with total flow rate of 200 sccm for (a) 5.5 min and (b) 3 minutes
Other important factor deciding wafer scalability of PEDAL process is the uniformity in the width of each single nanowire and space in an array across the wafer. In PEDAL process this will be decided by the uniformity of film deposited. As shown in graph in figure 3.34, for the deposition time of 5.5 minutes, the standard deviation of the film thickness from run to run across 4 inch wafer is from 1 A to 8 A. Similarly for the deposition times of 3 minutes the standard deviation of the film thickness from run to run across 4 inch wafer is from 1A to 11A. We can predict that similar result should be seen in the uniformity of widths of a-silicon lines in PEDAL defined template given other requirements like vertical trench sidewalls is also achieved in the process.

In the deposition process of thin silicon nitride films LPCVD reactors uses dichlorosilane and ammonia gas as precursor. Silicon Nitride is deposited by the chemical reaction shown below:

\[
3\text{SiH}_2\text{Cl}_2 + 10 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 6 \text{NH}_4\text{Cl} + 6 \text{H}_2
\]

As shown in graph in figure 3.35, at temperatures above 700 C, arrhenius relation is observed with activation energy of 1.62 eV i.e. around 37.136 Kcal/mol which is close to the value published [24, 25]. The deposition rate can be decreased by decreasing deposition temperature. In the temperature range of this experimentation, i.e. from 700 C to 800 C deposition rate varied from 14.7 A/min to 61.2 A/min. In the course of this research, silicon nitride film was deposited at 775 C using 120 sccm Ammonia gas and 40 sccm dichlorosilane gases with the total pressure of 300 mTorr. The deposition rate at this temperature was found to be 41 A/min. As discussed earlier in section 3.2.2, thin silicon...
nitride film deposited at 775 C was found to be highly conformal making this deposition process very suitable for the PEDAL technique.

Figure 3.34: Run to run standard deviation of LPCVD a-silicon film thickness at 535 C using 30 % Silane at 130 mTorr with total flow rate of 200 sccm for (a) 5.5 min and (b) 3 minutes.
Silicon nitride also has the very high fracture more than 0.1 GPa [26, 28, 29] making it excellent material for nanoimprinting application which is done at the pressure of 15-100 bar. Nanoimprinting of 100 nm dots and 500 nm lines is also demonstrated with silicon nitride templates using 4 % PMMA solution at 100 bars and 185 C curing temperature [27].

Figure 3.35: Deposition rate of silicon nitride at various temperatures in LPCVD system using 120 sccm Ammonia gas and 40 sccm dichlorosilane at 300 mTorr.

The deposition rate of silicon nitride can also be decreased by changing partial pressure of Dichlorosilane and ammonia. In this research partial pressure of these gases were not changed as the deposition rate of the 41.5 A/min required for repeatable deposition of silicon nitride films as thin as 150 A was readily obtained at 775 C.

As with the case in amorphous silicon deposition, the uniformity in silicon nitride film thickness across the wafer in one run, and from run to run directly affects the uniformity in
width of a single line and uniformity in width from one line to another in an array. Graph in figure 3.36(a) shows run to run average thickness silicon nitride film deposited in 6 minutes using 120 sccm Ammonia gas and 40 sccm Dichlorosilane gases with total pressure of 300 mTorr. The wafer scale average of silicon nitride thickness varies from 246.2 Å to 237.5 Å from run to run with overall average value of 242 Å. This suggests that average width of lines in array of line-width structure obtained using this deposition process in PEDAL process will be 246.2 Å. Graph in figure 3.36(b) shows run to run average silicon nitride film thickness deposited using above mentioned process condition for 3.0 minutes. The wafer scale average of silicon nitride film thickness obtained varies from 124.3 Å to 136.2 Å with overall thickness value of 131.45Å. This suggests that average width of the line in an array on PEDAL defined template obtained using this deposition process will be 131.45 Å.

As mentioned earlier, an important factor deciding the wafer scalability of PEDAL process is the uniformity in width of each nanowire and space in an array across the wafer. In PEDAL process this is decided by the uniformity of thin film deposited. As shown in graph in figure 3.37, for deposition time of 6 minutes, run to run standard deviation of film thickness across 4 inch wafer is from 4Å to 9 Å. Similarly for deposition time of 3 minutes, run to run standard deviation of film thickness across 4 inch wafer is from 3Å to 9Å. Since good uniformity is thickness of deposited film is observed, we can predict that similar result should be seen in the uniformity of widths of silicon nitride lines in PEDAL defined template.
Figure 3.36: Run to run wafer scale average of LPCVD silicon nitride film thickness at 775 C using 120 sccm Ammonia gas and 40 sccm dichlorosilane at 300 mTorr (a) 6 min and (b) 3 minutes.
Figure 3.37: Run to run standard deviation of LPCVD silicon nitride film thickness at 775 C using 120 sccm Ammonia gas and 40 sccm dichlorosilane at 300 mTorr (a) 6 min and (b) 3 minutes.
The width of lines and spaces obtained by PEDAL process depends on trench profile, thickness and conformality of films deposited. Using above mentioned thin film deposition processes for silicon nitride and amorphous silicon films on 3 microns wide and 2 microns deep trenches with smooth vertical sidewalls, we can predict width of lines and spaces obtained on nanowire template. Graph 3.38 shows the calculated widths and spaces on the template, using results of silicon nitride film deposition process done for 6 minutes and amorphous silicon film deposition process done for 5.5 minutes as well as considering 100 % conformality of silicon nitride films and 81 % conformality of a-silicon at the depth of 100 nm (figure 3.21). If silicon nitride layer defines lines and amorphous silicon defines spaces, then we will get lines of average width of 242 A and standard deviation from 4 A to 9 A, same as that of silicon nitride film thickness. Spaces on the template will be 81 % of average amorphous silicon film thickness of 232A due to nonconformality of a-silicon films. Hence average space width in the PEDAL template will be 184 A with standard deviation less than 1nm. As shown in graph in figure 3.38 average of estimated pitch of array of line and spaces on the template is 432.17 with standard deviation of these average values of 3.1 A.

Similarly we can calculate widths of lines and spaces on PEDAL defined template obtained by PEDAL process using previously described deposition process of silicon nitride and a-silicon thin films, each done for 3 minutes. If silicon nitride defines lines and amorphous silicon defines spaces, then from calculations we will get lines of average width of 131.45 A and standard deviation between 3A to 9A, same as that of silicon nitride film thickness. Again considering the effect of nonconformality of deposited a-silicon films, average space width in the PEDAL template will be 110.9 A with standard deviation less than 1nm. As
shown in graph in figure 3.39, average of estimated pitch of nanowire array in PEDAL defined template is 241.87 with standard deviation of these average values of 4.10 Å.

Figure 3.38: Calculated pitch of line-space structures obtained on the PEDAL template using thin film measurements (3.33 a, 3.36 a) and conformality results.

Figure 3.39: Calculated pitch of lines & spaces obtained on the PEDAL template using thin film measurements (3.33 b, 3.36 b) and conformality results.
3.3 Planarization

In this research all planarization processes have been done using plasma etching method in parallel plate Semigroup 1000 system. There are multiple planarization schemes experimented in the course of this project, including one recipe planarization, one step multiple recipes planarization, and multiple steps one recipe planarization. The most important planarization requirement for PEDAL process to make a nanoimprint mold is to obtain uniform heights of silicon nitride lines. As shown in figure 3.40 three different schemes are considered for planarization of a-silicon and silicon nitride stack deposited on steps etched in silicon <110> wafer.

![Figure 3.40: Different schemes of planarization process](image)

(a) Scheme A  (b) Scheme C

(c) Scheme B  (d) Scheme C

Figure 3.40: Different schemes of planarization process
In scheme A, polymer is spun on the wafer after a-silicon and nitride stack is deposited. For this topography to provide planar surface after planarization step, it’s important that the polymer is viscous enough to cover the trench without dishing (figure 3.40(b)). Dishing effect can be minimized by reducing the width of the trench by a-silicon deposition before polymer coat as shown in figure 3.40(c). If one step–one recipe planarization process is used in scheme A, then it’s very important that the planarization recipe be very nonselective i.e. etch rates of silicon nitride, a-silicon, silicon <110> and polymer to be same. Even a little selectivity causes the surface to be non-planar as shown in simulations later. Since in planarization we need uniform silicon nitride line heights, the requirements for planarization process can be eased to obtain combination of etch recipe which are non-selective to silicon nitride – amorphous silicon, amorphous silicon - polymer, to be used in two step RIE process discussed later in this chapter.

3.3.1 Planarization Experiment

Planarization experiments were done in Semigroup 1000 parallel plate RIE equipment. Gases connected to the semigroup available for experimentation were CHF₃, SF₆, O₂ and Ar. In RIE process using SF₆/O₂ gases, etch rate of Silicon increases with the concentration of oxygen and then decreases at higher Oxygen concentration. This is attributed to the fact that addition of oxygen to SF₆ plasma causes two effects, one is to prevent SF₆ formation in plasma obtained upon recombination process by forming SO₂F₂ and SOF₄ [30, 31]. The second effect is dilution of the reactant species SF₄, F₂, S₂F₂ SF₂ and mainly the highly reactive fluorine atom. Addition of oxygen to SF₆ also increases the etch rate of silicon nitride at first due to increase in fluorine atom concentration in plasma, but later it stays
almost constant, unlike the case of silicon, mainly because fluorine atom etch silicon nitride at lower rate than amorphous silicon and hence the effect of dilution is enhanced in silicon etch process rather than silicon nitride etch process. With this preliminary understanding of etching behavior using SF₆ and O₂ gas, conclusions in this research are made experimentally without analyzing and discussing plasma physics.

The graph in figure 3.41 shows results of RIE experiments done by varying oxygen concentration from 0 to 23 sccm and keeping SF₆ constant at 15 sccm, RF power of 100 watts and chamber pressure of 30 mTorr. As discussed above, with increase in oxygen concentration etch rate of amorphous silicon increases at first due to reduced SF₆ formation by recombination and then decreases due to dilution of fluorine atoms in plasma. Similar behavior is seen in etching Silicon <110>. At oxygen concentration of around 18 sccm, a-silicon etch is found to be very less selective over silicon nitride as well as silicon <110>. However, from the graph we can see that for this choice of gases, power and pressure mentioned in this experiment, the results are not repeatable as evident by the spread of data points for any particular concentration. The selectivity Si₃N₄: a-Si: Si<110> at oxygen concentration of 17.5 sccm is found to be varying from 1:0.92:1.06 to 1:0.954:1.06. Also for this etch recipe, selectivity to polymer Shipley 1813 was found to be very low as it etched more favorably than silicon nitride, a-silicon and silicon <110>. Hence this recipe could not be used for one step-one recipe planarization of the template for scheme A and B. It can be seen that at oxygen concentration of 12.5 sccm, the selectivity between silicon <110>, a-silicon and Shipley 1813 is 1.05:1:0.98. Hence, this recipe can be used as a part of two step process, if schemed C is used for planarization, where etching is carried out till level A at
oxygen concentration of 12.5 sccm and then till level B at oxygen concentration of 17.5 sccm.

Figure 3.41: Etch rates (Angstroms/min) of Silicon nitride, amorphous silicon, silicon<110> and polymer Shipley 1813 measured for RIE process at 30 mTorr and power of 100 W using 15 sccm SF$_6$ and varying oxygen concentration

In above experiments one of the reasons for etch rate variation form run to run observed, can be due to the etch sensitivity of a-silicon and photoresist on oxygen concentration. This sensitivity of the etch rates on the oxygen concentration emphasizes the fact that the etching nature is more chemical than physical. Hence a little variation in oxygen concentration, which can be due to the equipment itself, causes significant change in the etch rates of a-silicon and photoresist. In next set of experiments of determining a planarization process less
sensitive to chemical composition, an attempt is made to make the etching process more physical in nature while utilizing the chemical nature of etch process to tune the etch rates. High concentration of inert heavy gas Argon is used for making etching more physical, and low relative concentration of SF₆ and CHF₃ is used to control chemical nature to the etch process. Experiments were done in Semigroup RIE 1000 parallel plate RIE equipment at pressure of 30 mTorr and RF power of 100 W. The concentrations of Argon and SF₆ were kept constant at 88 sccm and 5 sccm respectively, and the concentration of CHF₃ was varied from 5 to 25 sccm. In this experiment, the etch rates were lower than the experiment done using SF₆ and O₂, but there still was variation in the etch rates from run to run for the same etch condition as shown in graph in figure 3.42. Both a-silicon and silicon nitride etch rates were found to be less sensitive to varying CHF₃ concentration. This can be due to the fact that etching is predominantly due to heavy Argon gas, as expected, and the effect of CHF₃ is minimal due to dilution. However, chemical nature of etching due to CHF₃, even though relatively small, can be seen in increasing of etch rates of a-silicon and silicon nitride with the increase in CHF₃ concentration. Both polymer Shipley 1813 and V40 were found to be more sensitive to dilution of Argon gas by increase in CHF₃ concentration, and their etch rates decreased as CHF₃ concentration was increased, unlike the case for silicon nitride and a-silicon. This can be due to the possibility that polymers are less sensitive to fluorocarbon gas and dominant nature of polymer etching in above gas composition is the physical etching due to heavy inert gas Argon. In above experiments, variation in etch rates and selectivity from run to run for same etch conditions, can clearly be due to equipment limitations, as similar behavior was also observed for etch recipes using SF₆ and O₂ gas discussed previously.
Figure 3.42: Etch rates of Silicon nitride, amorphous silicon, polymer Shipley 1813 and V40 measured for RIE process at 30 mTorr and power of 100 W using 88 sccm Argon, 5 sccm SF$_6$ and varying CHF$_3$ concentration.

3.3.2 Planarization Techniques

In this section I have briefly discussed various planarization techniques experimented in the course of this project. The experiments were designed after getting preliminary understanding of planarization process by simulations. Three different techniques were experimented on various schemes shown in figure 3.40. These techniques are one step process, multi-step process, etch-recess-coat and repeat process.
3.3.2.1 Single Step RIE planarization technique

To get preliminary understanding of planarization, and its dependence on etch selectivity, numerical simulations of the etching were done for the template structure shown in figure in scheme A. In these simulations rounding of the deposited films at the edges of trench was ignored and hence the outcomes are the approximations. Nonetheless, simulation does show the dependence of PDEAL template profile on the selectivity of etch recipe. Graphs in figure 3.43 show profiles for different cases of etch selectivity for fast as well as slow etches. Simulations are done for silicon nitride and amorphous silicon film thickness of 250Å each and polymer coating of thickness 14000Å. As shown in graph 3.43(a), for a slow etch recipe with etch selectivity of silicon nitride, a-silicon and Shipley 1813 of 1:1.1:0.93; the template is not planar with maximum difference between silicon nitride line heights of 7.93e-8 m. Same is true for the fast etch recipe with same etch selectivity as shown in graph 3.43(b). Simulations show spacer like formation even if etch recipe is just little selective towards a-silicon than nitride. The nanoimprint mold obtained using this planarization recipe will not be useful for nanoimprinting due to high difference in silicon nitride line heights.

Similar spacer like formation was observed for simulations in which etch recipe was little selective to silicon nitride over amorphous silicon. The graph in figure 3.44 is for the recipe with etching selectivity of silicon nitride, amorphous silicon and Shipley 1813 of 1.0.93:1.1. The outcome is similar to that of the case discussed above except that silicon nitride, which etches more than a-silicon, is recessed below the level of planarization, just opposite to the case discussed above in which it stands above the level of planarization. In this case the maximum difference of the height of silicon-nitride lines is calculated to be 5.19e-8 m which
will make the template is unsuitable for nanoimprinting.

Figure 3.43: Simulation results of the planarization using Scheme A and RIE recipe with (a) silicon nitride etch rate = 1e-8 m/min, a-silicon etch rate = 1.13e-8 m/min, Shipley 1813 etch rate = 9.3 e-9 m/min (b) silicon nitride etc rate =1e-6 m/min, a-silicon etch rate = 1.13e-6m/min and Shipley 1813 etch rate = 9.3e-7 m/min
In both the cases discussed above, maximum difference in heights of silicon nitride depend on relative etch rates of silicon nitride and a-silicon, and not on etch rates of polymer and silicon\text{<110>}. This is due to simplification of the condition used for simulation, which neglects the capping effect (figure 3.45) of a layer on underlying layers caused mainly due to rounding of deposited materials at edges of a trench. Although deviation from simulation results can be observed in practice, the aim of these simulations is to set a stage for experimentation without providing exact values of planarity. It’s logical to guess that capping effect will cause just little deviation from results obtained in these simulations, if the etch rates of silicon nitride; a-silicon and polymer are highly non-selective.

Figure 3.44: Simulation results of the planarization using topography A and RIE recipe with silicon nitride etch rate = 1e-8 m/min, a-silicon etch rate = 9.3e-9 m/min, Shipley 1813 etch rate = 1.13e-8 m/min.
Figure 3.45: (a) Simplified model used for numerical analysis of planarization process (b) capping effect due to the rounding of films deposited at the edges of trench. (c),(e) planarization by neglecting capping effect and considering capping effect (d),(f) considering capping effect
In experiments done using one step one recipe technique discussed above, RIE recipe with Ar + CHF$_3$ + SF$_6$ gases was used. From the graph 3.42, at CHF$_3$ concentration of 10 sccm, the etch rate selectivity of silicon nitride, a-silicon and polymer Shipley 1813 varies from 1:1:0.96 to 1:1.13:0.93. Since, in this gas composition, the polymer etches less selectively to silicon nitride and a-silicon, unlike the case of SF$_6$ + O$_2$ etch recipes, scheme A (figure 3.40) can be also be used for planarization. As discussed in the numerical simulation shown previously, the planarization done using above recipe at CHF$_3$ concentration of 10 sccm can provide spacer like structure with varying silicon nitride line heights. Similar behavior was obtained in actual experimentation as shown in SEM in figure 3.46.

![SEM of the cross-section of the PEDAL template obtained in topography B after planarization by RIE process using 10 sccm CHF$_3$, 5 sccm SF$_6$, 88 sccm Argon at 30 mTorr and 100 watts.](image)

**Figure 3.46**: SEM of the cross-section of the PEDAL template obtained in topography B after planarization by RIE process using 10 sccm CHF$_3$, 5 sccm SF$_6$, 88 sccm Argon at 30 mTorr and 100 watts.
3.3.2.2 Multiple Step RIE planarization technique

In an attempt to improve planarization of silicon nitride lines, by taking into account run to run variation in etch rates of silicon nitride, a-silicon, polymer and silicon<110> for same gas composition, simulations for multiple step RIE process were done using scheme C (figure 3.40), neglecting rounding of deposited films at top edges of trench. In simulations, the etch selectivity of silicon nitride and a-silicon was changed from 1:0.86 for one step to 1:1.2 for other step and each of these steps were repeated alternatively, each for the fixed duration of 2.5 min and 2 min respectively. Graph in figure 3.47 (a) shows heights of silicon nitride and amorphous silicon lines with respect to the top surface of trench in Si <110> wafer, obtained by using multiple steps etch process. The maximum difference in heights of silicon nitride lines is 21 nm which is good improvement from the value of 79.2 nm obtained for one step–one recipe planarization process discussed previously. Graph in figure 3.47 (b) shows simulation result using same alternating etch recipes with silicon nitride and a-silicon etch selectivity changing from 1:0.86 for one step to 1:12 for the other step, each for shorter duration of 65 sec and 75 seconds respectively. In this case the planarization is greatly improved with the maximum difference in heights of silicon nitride lines being 8.2 nm, significantly better than the cases discussed previously. Multiple step planarization process is also tolerant to slight deviations of etch-selectivity, unlike the case of one step one recipe planarization process. The graph in figure 3.48 shows the simulation result for alternating etch recipe with silicon nitride and a-silicon etch selectivity changing from 1:0.76 for one step to 1:1.43 for other step each for shorter duration of 65 seconds and 75 seconds respectively. In this case planarization is similar to the one shown in graph 3.47 (b) with maximum difference in heights of silicon nitride lines being 9.25 nm.
Figure 3.47: Simulation results of the planarization using multiple step RIE recipe using alternating etch recipes with the etch selectivity changing from 1:0.86 for one step to 1:12 for the other step, each for fixed duration of (a) 2.5 minutes and 2 minutes respectively (b) 65 sec and 75 sec respectively.
Figure 3.48: Simulation results of the planarization using multiple step RIE recipe using alternating etch recipes with the etch selectivity changing from 1:0.76 for one step to 1:1.42 for the other step, each for fixed duration of 65 sec and 75 sec respectively.

The multiple step planarization process discussed above is useful for the scheme D, in which it can be used in the planarization from level A to Level B. Again here it’s important to realize that simulations are done neglecting the capping effect of a layer on underlying layers caused mainly due to rounding of deposited materials at edges of a trench. Although deviation from simulation results can be observed in practice, the aim of these simulations is to set a stage for experimentation without providing exact values of parameters like the selectivity and duration of each etch step in multiple step etch scheme. It’s logical to guess that capping effect will not give significant deviation from results obtained in these simulations, if the RIE recipe is highly non-selective to silicon nitride and a-silicon.
In multiple step RIE planarization experiment, the gas concentration of the variable gas i.e. Oxygen gas concentration in SF$_6$ + O$_2$ RIE recipes, is changed from step to step. These concentrations were changed above and below concentrations at which non-selective etches were observed. i.e. in case of SF$_6$+ O$_2$ gas recipe, O$_2$ gas concentration was changed from 15 sccm in one step to 19.5 sccm in other step of multiple steps etch recipe. From the experiments done earlier we know that at the Oxygen concentration of 15 sccm the etch selectivity of silicon nitride and a-silicon is around 1: 0.85 and at the concentration of 19.5 sccm the selectivity is 1.32: 1. This selectivity changes from run to run as shown in the graph in figure 3.41 by the spread of etch rates for a particular gas composition. Each of these steps was repeated alternatively, each for the fixed duration of 2.5 min and 2 min respectively. From the SEM results shown in figure 3.49, we can see that due to complexity of the multiple steps RIE process, although spacer like formation is not observed in experiments, it’s difficult to observe simulation results in actual experiment.

Figure 3.49: SEM of the cross-section of the PEDAL template obtained by multiple step RIE technique.
3.3.2.3 **Etch-recess coat and repeat process**

Due to complexity of multiple step RIE technique and the requirement for precise control of equipment to get desired planarity, another technique to get nanoimprint mold with leveled silicon nitride lines namely etch-recess-coat and repeat process is developed. In this process, after first attempt of planarization using any of the previously discussed techniques that is the one step or multiple step RIE process; a-silicon layer is recessed by selectively wet etching to a certain depth less than 100 nm. The whole wafer is then spin-coated with polymer Shipley 1813 or V40, and the RIE process is repeated to etch the structure up to the level above a-silicon lines as shown in figure 3.50. If a desired planarization is not achieved the process can be repeated. This scheme can be used even if the etch recipe is selective to either of silicon nitride or polymer. However as shown by numerical simulations later, with increase in etch selectivity number of repeats needed to achieve desired planarization also increases.

![Figure 3.50: Etch –Recess –Coat and Repeat planarization scheme.](image)

Figure 3.50: Etch –Recess –Coat and Repeat planarization scheme.
Figure 3.51: Simulation results for etch recess coat and repeat planarization scheme using RIE process with etch selectivity of the silicon nitride, a-silicon and polymer of 1: 1.1: 0.93, after (a) one repeat and (b) second repeat.

Simulation results shown in figure 3.51 is for the case in which initial planarization is done using one step process considering recipe with etch selectivity of silicon nitride, a-silicon and polymer of 1: 1.1: 0.93 followed by spin coating of the mold with polymer and
planarizing with the same recipe. As shown in the graph, after first repeat the maximum difference between heights of silicon nitride line is improved from the value of 79 nm to 5.8 nm, and after second repeat even better planarization is obtained with maximum difference in silicon nitride line height of 0.45 nm.

Figure 3.52: SEM of the cross-section of PEDAL template obtained by recess coat etch and repeat planarization process with one repeat using 88 sccm Ar, 5 sccm SF$_6$, 10 sccm CHF$_3$ at 30 mTorr and power of 100 W.

SEM shown in figure 3.52 is obtained by using scheme D, in which planarization till level A is done by using 15 sccm SF$_6$ and 12.5 sccm O$_2$ at 30 mTorr and power of 100 W. Planarization from level A to level B is done using 88 sccm Ar, 5 sccm SF$_6$, 10 sccm CHF$_3$ at 30 mTorr and power of 100 W. Approximately 100 nm of amorphous silicon is then selectively etched in a-silicon etchant and then the wafer is spin coated with approximately
14000 Å of polymer Shipley 1813 followed by etching with same recipe using Ar, SF₆ and CHF₃ mentioned above. From the AFM measurements discussed in next chapter, maximum difference in the silicon nitride line heights is measured to be less than 10 nm.

As mentioned earlier, any RIE process can be used for the recess-coat-etch and repeat process. However number of repeats depends mainly on the etch selectivity to silicon nitride and polymer. Number of repeats increases with increase in selectivity of the etch recipe. For analysis, numerical simulations were done for arbitrary recipe with etch selectivity of silicon nitride, a-silicon and polymer of 1: 10: x, where x is varied from 1.13 to 10. Results shown in graphs in figure 3.53 are obtained for planarization of stack of alternate layers of silicon nitride and a-silicon, each 250 Å thick. Number of steps for planarization were determined for the condition to get the maximum differences between heights of silicon nitride lines less than 5 Å.

From results shown in figure 3.53 it’s obvious that number of repeats increases with increase in selectivity between silicon nitride and polymer. Also maximum difference between heights of silicon nitride lines decreases exponentially at higher number of repeats. Graph in figure 3.54 shows that number of repeats increases almost linearly with increase in selectivity between silicon nitride and polymer. At high selectivity, recess-etch-coat and repeat process will be limited by the depth of trench and total time of process repetitions to get the silicon nitride line planar to desired value.
Figure 3.53: Simulation results obtained for recess-coat etch and repeat process for RIE process with etches selectivity of silicon nitride, a-silicon, Polymer of (a) 1:10:1.13 (b) 1:10:2 (c) 1:10:5
Figure 3.53: Simulation results obtained for recess-coat etch and repeat process for RIE process with etches selectivity of silicon nitride, a-silicon, Polymer of (d) 1:10:8 (e) 1:10:10
Summary

In this chapter, theory and development of PEDAL process has been discussed. Experiments have been designed after getting preliminary analysis of the processes. This approach led to a successful development of the process and successful demonstration of template fabrication with wafer-scale arrays of sub-25 nm line-width structures. Some of the key points from all this discussion can be summarized as listed below.

1) **Trench Etch:** RIE etch recipes giving highly anisotropic trenches with desired route are successfully used in semiconductor industry, hence this step does not pose a significant challenge in PEDAL process. Although it’s been shown that wet etches like KOH etch can provide highly anisotropic trenches, routing is restricted to a particular design. Conditions are obtained by simulations to minimize deviation from design values in line widths obtained.
from nanoimprinting and pedal lift-off process. These conditions are obtained after making some basic assumptions in each case, which are no lateral distortion of features and no sticking of molds in nanoimprinting, and complete removal of metal from the surface which is etched in lift-off solution.

2) Thin film deposition: LPCVD can provide conformal films and wide range of material choices to get desired conformality and deposition control. It’s been shown by simulations that PEDAL process is tolerant to nonconformal film deposition, and the effect of nonconformality on linewidth deviation can be reduced by making trenches wider and increasing depth of planarization. It’s been also found from simulations that standard deviation in widths as percentage of average widths reduces as we scale down the linewidths. Nonconformity of thin films deposition can also be used to scale down the linewidths as film thickness on trench sidewalls decreases with increase in depth inside a trench. Minimum film surface roughness, run to run film thickness uniformity and wafer scale film thickness uniformity are other important requirements, which directly affect the quality of molds. Scaling the PEDAL technique below 10 nm linewidth dimensions can be achieved by reducing the gas flows and thus decreasing the deposition rate. Alternatively, Atomic Layer Deposition (ALD) process can also be used as it is capable of depositing monolayer of conformal thin films.

3) Planarization: One of the most important challenges in PEDAL process is planarization of silicon nitride lines. In planarization approach using RIE processes, it’s been shown by simulation as well as experimentation, that requirement for the non-selective etch recipes can
be eased in etch recess coat and repeat technique. This technique improves the planarity with each repeat and the number of repeats to get desired planarization depends on the etch selectivity of the processes.
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CHAPTER 4

4. NANOIMPRINT MOLD AND METAL LIFT-OFF RESULTS

In this chapter results of PEDAL process for making sub-25 nm wide nanowire molds and metal nanowires are discussed. As discussed in previous section, throughout the course of this project many experiments have been done for getting desired results, mainly, vertical trench sidewalls, conformal deposition of silicon nitride and a-silicon films, and planarization. Results shown here are for the molds and metal nanowires obtained after integrating the most successful of all the experiments done. For the brevity of the chapter only the most significant results from the all the experiments have been reproduced in this chapter for further analysis.

4.1 PEDAL and PEDAL lift-off process

<table>
<thead>
<tr>
<th>Serial No.</th>
<th>Process step</th>
<th>Process description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>JTB 111 Clean -</td>
<td>10 minutes (JTB111: H$_2$O$_2$: DI water = 965: 212: 4823)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DI water rinse – 6 cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blow dry with nitrogen</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Silicon nitride</td>
<td>LPCVD deposition, DCS = 40 sccm, Ammonia = 120 sccm, pressure = 300 mTorr, Temperature = 775 C, deposition rate = 41 Å/ min, time = 24 min, Thickness = 1000 Å (approx.)</td>
<td></td>
</tr>
<tr>
<td>Serial No.</td>
<td>Process step</td>
<td>Process description</td>
<td>Comments</td>
</tr>
<tr>
<td>-----------</td>
<td>----------------------</td>
<td>-------------------------------------------------------------------------------------</td>
<td>----------</td>
</tr>
</tbody>
</table>
| 3         | Photolithography     | Bake = 5 min @ 115 C  
Spin HDMS @ 4000 rpm, 40 sec  
Spin Shipley 1813@ 4000 rpm, 40 sec  
Pre-exposure bake @ 115 C, 1 min  
Exposure on Karl-Suss MA6 contact aligner for 8-10 sec, Develop- MF 319 for 30 sec, Post develop bake @ 115 C for 5 min |          |
| 4         | Silicon nitride etch | RIE etch in SEMIGROUP 1000 system  
SF$_6$ = 15 sccm, O$_2$= 17.5 sccm, Power = 100W, pressure = 30 mTorr, time = 2.5 min, etch rate = 510 A/min (average), target = 1000 A |          |
| 5         | Photoresist Strip    | Nanostrip solution 1, time = 6 min  
Nanostrip solution 2, time = 3 min  
DI water rinse 6 cycles  
Blow dry with nitrogen |          |
| 6         | Trench etch          | 40 % KOH wet etch @ 70 C  
Etch rate = 193 A /sec (Average)  
Time = 110 sec, Target etch = 2 microns (approx), DI water rinse 6 cycles, Blow dry with nitrogen | Stirring required to reduce surface roughness |
| 7         | Silicon nitride etch | Hot Phosphoric acid (Transene N etch)  
Etch rate = 125 A/min @ 180 C  
Time = 9 min  
Target etch = 1000 A  
DI water rinse 6 cycles, N$_2$ Blow dry |          |
<table>
<thead>
<tr>
<th>Serial No.</th>
<th>Process step</th>
<th>Process description</th>
<th>Comments</th>
</tr>
</thead>
</table>
| 8         | RCA clean         | SC1 clean ( NH\textsubscript{4}OH : H\textsubscript{2}O\textsubscript{2} : H\textsubscript{2}O = 1:1:5) @ 75 C, time = 10 min  
DI water rinse 6 cycles  
SC2 clean( HCl : H\textsubscript{2}O\textsubscript{2} : H\textsubscript{2}O = 1:1:5)  
@ 75 C, time = 10 min, DI water rinse 6 cycles, Blow dry with nitrogen |
<p>| 9         | Buffer a-silicon  | LPCVD deposition, Silane = 60 sccm, pressure = 130 mTorr, Temperature = 550 C, deposition rate = 69 A/min, time = 15 min, target = 1000 A |
|           | deposition        |                                                                                        |                          |
|           |                   | <strong>Wafers are divided into two batches of 10 wafers each</strong>                               |                          |
| 10 A      | LPCVD silicon     | LPCVD deposition, DCS =40 sccm, Ammonia = 120 sccm, pressure = 300 mTorr, Temperature = 775 C, deposition rate = 41 A/ min, time = 6 min, Thickness = 250 A (approx.) |
|           | nitride           |                                                                                        | Batch 1                   |
| 11 A      | LPCVD a-silicon   | LPCVD deposition, Silane = 60 sccm, pressure = 130 mTorr, Temperature = 535 C, deposition rate = 45 A/min, time = 5.5 min, target = 250 A |
|           | Deposition        |                                                                                        | Batch 1                   |
|           |                   | <strong>REPEAT above processes (10 A,11 A) on Batch 1, alternating for 16 times each (depending on number of nanowires, repetitions can be increased or decreased)</strong> |                          |
| 10 B      | LPCVD silicon     | LPCVD deposition, DCS = 40 sccm, Ammonia = 120 sccm, pressure = 300 mTorr, Temperature = 775 C, deposition rate = 41 A/ min, time = 3 min, Thickness = 120 A (approx.) |
|           | nitride deposition|                                                                                        | Batch 2                   |</p>
<table>
<thead>
<tr>
<th>Serial No.</th>
<th>Process step</th>
<th>Process description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>11 B</td>
<td>LPCVD a-silicon deposition</td>
<td>LPCVD deposition, Silane = 60 sccm, pressure = 130 mTorr, Temperature = 535 C, deposition rate = 45 A/min, time = 3 min, target = 135 A</td>
<td>Batch 2</td>
</tr>
<tr>
<td></td>
<td><strong>REPEAT</strong> above processes (10 B, 11 B) on Batch 2, alternating for 24 times each (depending on number of nanowires, repetitions can be increased or decreased)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>LPCVD a-silicon deposition</td>
<td>LPCVD deposition, Silane = 60 sccm, pressure = 130 mTorr, Temperature = 535 C, deposition rate = 45 A/min, time = 180 min, target = 8000 A</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td>13</td>
<td>Polymer spin coat</td>
<td>Spin Shipley 1813 @ 4000 rpm , 40 sec Bake @ 115 C, 1 min</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>RIE etch</td>
<td>RIE etch in SEMIGROUP 1000 system SF$_6$ = 15 sccm, O$_2$= 12.5 sccm, Power = 100 W, pressure = 30 mTorr, time = 20 min, etch rate = 803 A/min (average), Target = 16000 A</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td>15 A</td>
<td>RIE etch</td>
<td>RIE etch in SEMIGROUP 1000 system SF$_6$ = 15 sccm, O$_2$= 17.5 sccm, Power = 100 W, pressure = 30 mTorr, time = 25 min, etch rate = 520 A/min (average), Target = 13000 A</td>
<td>Batch 1</td>
</tr>
<tr>
<td>15 B</td>
<td>RIE etch</td>
<td>RIE etch in SEMIGROUP 1000 system SF$_6$ = 15 sccm, O$_2$= 17.5 sccm, Power = 100 W, pressure = 30 mTorr, time = 23 min, etch rate = 520 A/min (average), Target = 12000 A</td>
<td>Batch 2</td>
</tr>
<tr>
<td>Serial No.</td>
<td>Process step</td>
<td>Process description</td>
<td>Comments</td>
</tr>
<tr>
<td>-----------</td>
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<td>--------------------------------------------------------------------------------------</td>
<td>-------------------------------</td>
</tr>
<tr>
<td>16</td>
<td>SC 1 clean</td>
<td>SC1 clean ((\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1:1:5) @ 75 ^\circ\text{C}, \text{time} = 10 \text{ min})</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DI water rinse 6 cycles</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td><strong>Due to run-to run variation of etch recipes and spin –coating of Shipley 1813, SEM measurements are needed after process 16 to make sure all the stack is etched.</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>a-silicon etch</td>
<td>Recess etch of a-silicon</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{HNO}_3 : \text{NH}_4\text{F} : \text{H}_2\text{O} = 21 : 1 : 11)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Etch rate = 80 A/sec, Time = 10 sec, Target = 800 A,</td>
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<td></td>
<td></td>
<td>DI water rinse – 6 cycles</td>
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<tr>
<td></td>
<td></td>
<td>Blow dry with nitrogen</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Polymer Coat</td>
<td>Spin coat Shipley 1813 @ 4000 rpm, @ 40 sec, Bake @ 115 ^\circ\text{C} for 1 min</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td>19</td>
<td>RIE etch</td>
<td>RIE etch in SEMIGROUP 1000 system</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{SF}_6 = 15 \text{ sccm}, \text{O}_2 = 12.5 \text{ sccm}, \text{Power} = 100 \text{ W}, \text{pressure} = 30 \text{ mTorr}, \text{time} = 16 \text{ min}, \text{etch rate} = 803 \text{ A/min (average)}, \text{Target} = 13000 \text{ A})</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>RIE etch</td>
<td>Ar = 88 sccm, (\text{SF}_6 = 5 \text{ sccm}, \text{O}_2 = 0 \text{ sccm}, \text{CHF}_3 = 10 \text{ sccm, Power} = 100 \text{ W}, \text{pressure} = 30 \text{ mTorr, time} = 5 \text{ min, etch rate} = 240 \text{ A/min (average)}, \text{Target} = 1200 \text{ A})</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td><strong>Due to run-to run variation of etch recipes and spin –coating of Shipley 1813, SEM measurements are needed after process 20 to make sure etching is done to desired level.</strong></td>
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<td></td>
</tr>
<tr>
<td>Serial No.</td>
<td>Process step</td>
<td>Process description</td>
<td>Comments</td>
</tr>
<tr>
<td>-----------</td>
<td>------------------</td>
<td>-------------------------------------------------------------------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>21</td>
<td>Photoresist Strip</td>
<td>Nanostrip solution 1, 6 min</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Nanostrip solution 2, 3 min</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DI water rinse 6 cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blow dry with nitrogen</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>SC1 clean</td>
<td>SC1 clean (NH$_4$OH : H$_2$O$_2$: H$_2$O = 1:1:5) @ 75 C, time = 10 min</td>
<td>Batch 1 and Batch 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DI water rinse 6 cycles</td>
<td></td>
</tr>
</tbody>
</table>

Each batch is divided into two sub-batches, one for fabricating nanoimprint mold and other for on-template palladium nanowires

<table>
<thead>
<tr>
<th>Serial No.</th>
<th>Process step</th>
<th>Process description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>a-silicon etch</td>
<td>Recess etch of a-silicon</td>
<td>Batch 1 and Batch 2 for making nanoimprint molds</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HNO$_3$: NH$_4$F: H$_2$O = 21 : 1: 11</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Etch rate = 80 A/sec, Time = 10 sec, Target = 800 A</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>DI water rinse – 6cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blow dry with nitrogen</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Silicon nitride</td>
<td>49 % HF solution, etch rate = 97 A/min, time = 10 min, target = 1000 A,</td>
<td>Batch 1 and Batch 2 for Pd nanowire</td>
</tr>
<tr>
<td>etch</td>
<td></td>
<td>DI water rinse – 6 cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blow dry with nitrogen</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>JTB 111 clean</td>
<td>10 minutes (JTB111: H$_2$O$_2$: DI water = 965: 212: 4823)</td>
<td>Batch 1 and Batch 2 for Pd nanowire</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DI water rinse – 6 cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blow dry with nitrogen</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>Palladium deposition</td>
<td>E-beam evaporation of Pd, @ 0.1 A/sec, Pressure = 4 uTorr, time = 1000 sec, target = 100 A</td>
<td>Batch 1 and Batch 2 for Pd nanowire</td>
</tr>
<tr>
<td>Serial No.</td>
<td>Process step</td>
<td>Process description</td>
<td>Comments</td>
</tr>
<tr>
<td>-----------</td>
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<td>--------------------------------------------------------------------------------------</td>
<td>---------------------------------</td>
</tr>
<tr>
<td>27</td>
<td>Metal Lift-off</td>
<td>a-silicon etch</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HNO₃ : NH₄F: H₂O = 21 : 1: 11</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Etch rate = 80 A/sec, Time = 20 sec, Target = 1500 A, Gentle stirring</td>
<td>Batch 1 and Batch 2 for Pd</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DI water rinse – 6 cycles</td>
<td>nanowire</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blow dry with nitrogen</td>
<td></td>
</tr>
</tbody>
</table>

4.2 43 nm pitch template and palladium nanowires

In order to evaluate the efficacy of above PEDAL process for making the nanoimprint mold, measured dimensions of lines and spaces on the mold are compared to the calculated values. Also, the planarity of the mold is determined from SEM cross-section and AFM measurements. The graph in figure 4.1 shows average a-silicon film thickness from run to run, deposited in 5.5 minutes using 30 % silane gas at 535 C with total flow rate of 200 sccm at 130 mTorr. Wafer scale average amorphous silicon thickness varies from 225.6 A to 237.7 A, with overall average value of 231.9A. Other important parameter deciding wafer scalability of PEDAL process is the uniformity in width of each single nanowire and space in an array across the wafer. In PEDAL process this is decided by the uniformity in thickness of film deposited. As shown in graph in figure 4.2, for deposition time of 5.5 minutes, the standard deviation of film thickness from run to run across 4 inch wafer is from 1A to 8A.
Figure 4.1: Run to run wafer scale average of LPCVD a-silicon film thickness at 535 C, 30 % Silane (60 sccm) at 130 mTorr with total flow rate of 200 sccm for 5.5 min.

Figure 4.2: Run to run standard deviation of LPCVD a-silicon film thickness at 535 C using 30 % Silane at 130 mTorr with total flow rate of 200 sccm for 5.5 min.
As with the case in amorphous silicon deposition, the uniformity in silicon nitride film thickness across the wafer in one run, and from run to run, directly affects the uniformity in the width of a single line and uniformity in the width from one line to another in an array in the PEDAL process defined nanowire template. Graph in figure 4.3 shows the run to run wafer scale average silicon nitride film deposited in 6 minutes using 120 sccm Ammonia gas and 40 sccm Dichlorosilane gases with total pressure of 300 mTorr. The wafer scale average of silicon nitride thickness varies from 237.5 Å to 246.2 Å from run to run with overall average value of 242 Å. As mentioned earlier an important parameter of the wafer scalability of PEDAL process is the uniformity in width of each nanowire and space in an array across the wafer and in PEDAL process this is decided by the uniformity of thin film deposited. As shown in graph in figure 4.4, for deposition time of 6 minutes, the run to run standard deviation of film thickness across 4 inch wafer range from 4Å to 9Å.

![Graph showing run to run wafer scale average of LPCVD silicon nitride film thickness at 775 C using 120 sccm Ammonia gas and 40 sccm dichlorosilane at 300 mTorr for 6 min.](image)

Figure 4.3: Run to run wafer scale average of LPCVD silicon nitride film thickness at 775 C using 120 sccm Ammonia gas and 40 sccm dichlorosilane at 300 mTorr for 6 min.
Figure 4.4: Run to run standard deviation of LPCVD silicon nitride film thickness at 775 C using 120 sccm Ammonia gas and 40 sccm dichlorosilane at 300 mTorr for 6 min.

The width of lines and spaces obtained by PEDAL process depends on trench profile as well as thickness and conformality of films deposited. Using above mentioned thin film deposition processes for silicon nitride and amorphous silicon films on 2 microns wide and 3 microns deep trenches with smooth vertical sidewalls, we can predict width of lines and spaces obtained on the nanowire template. Graph 4.5 shows the calculated widths and spaces on the template, using the results of silicon nitride film deposition process done for 6 minutes and amorphous silicon film deposition process done for 5.5 minutes as well as considering 100 % conformality of silicon nitride films and 81 % conformality of a-silicon at the depth of 100 nm from surface of trench.
If silicon nitride layer defines lines and amorphous silicon defines spaces, then we will get lines of average width of 242 Å and standard deviation from 4 Å to 9 Å, same as that of silicon nitride film thickness. Spaces on the template will be 81% of average amorphous silicon film thickness of 232Å due to nonconformality of a-silicon films. Hence average space width in the PEDAL template will be 184 Å with the standard deviation less than 1nm.

From the graph in figure 4.5, the average of estimated pitch of array of line and spaces on the template is 432.17 with 3.1 Å standard deviation.

SEM in figure 4.6 shows the typical top view and cross-section of nanowire template. Measurements of dimensions were done using SEM images and conclusions are made based
on measured values. Although care has been taken to minimize the errors, it’s left to the
discretion of readers to account for the error that might be associated with this methodology.
Some of the factors adding to errors are the charging of the silicon nitride layer, and tilt in
sample loading. In order to assess the uniformity in line width and spacing of template
across entire 4 inch wafer, width of nanowire and space number 1 (from figure 4.6 (a)) was
measured and the results are shown in graph in figure 4.7.

Figure 4.6: SEM of top view of PEDAL template shows 17 silicon nitride lines with
average width of around 24 nm spaced at average distance of around 18 nm.
From the measurements, average width of line was found to be 23.75 nm with standard deviation of 1.4 nm, whereas average spacing was found to be 17.1 nm with the standard deviation of 1.27 nm. From the measurements we can conclude that average values of widths of lines and spaces on templates differ by over 10 Å from the values for first line and space calculated by thin film deposition measurements shown in graphs 4.1 and 4.3, and the standard deviation observed is more than twice the predicted.

Figure 4.7: Wafer scale measurement of first line and space shown in figure 4.6(a), gives average line width of 23.75 nm and space width of 17.1 nm.

Measurements were also done to assess the uniformity of the adjoining lines and spaces in an array on the template. These results are shown in figure 4.8. From the measurements it is observed that in an array average width of the line is around 23.94 nm with the standard deviation of 3.64 nm and average spacing is around 17.27 nm with the standard deviation of
2.11 nm. This gives us the average pitch of the array of lines on the template to be around 41.5 nm with the standard deviation of 4.67 nm. These average values are close to the values calculated from the film thickness measurements which gives average width of lines as 242 Å and average width of the space as 184 Å.

One of the possible reasons for observing higher standard deviation in the measurements can be limitations of the SEM technique used to determine the values of line and space width. More elaborate measurement technique like TEM will be needed to find the possible cause of observing deviation from the predicted value.

![Template line and spaces](image)

**Figure 4.8: Measurement of lines and spaces in an array shown in figure 4.6 (b), gives average line width of 242 Å and space width of 184 Å**

SEM of the cross-section of these templates and AFM of the surface of these templates were taken to determine the planarity of the molds. As shown in figure 4.9 the templates obtained
show good planarity and the maximum difference between heights of silicon nitride lines was measured to be around 10 nm which is less than the width of lines and spaces on the template. The nanoimprint template thus obtained can be used for nanoimprinting of lines and spaces with 43 nm pitch. It’s important to bring to the attention of readers that from the simulations on planarization discussed section 3.3.2.3, silicon nitride line heights can be made more planar by repeating etch-recess-coat-repeat process until desired planarity is achieved depending on nanoimprinting needs.

Figure 4.9: SEM showing planarity of silicon nitride lines of nanoimprint template fabricated by PEDAL process.
Figure 4.10: AFM using super sharp tips, of the nanoimprint template fabricated by PEDAL process shows planarity of silicon nitride lines with maximum difference between heights of silicon nitride lines measured to be around 10 nm, and pitch is around 42 nm. Sharp edges are not observed in the AFM images due to AFM tip convolution.
AFM of the surface of individual lines on the template fabricated by PEDAL process was also done to find the surface roughness of these lines. Low surface roughness of the line surface contacting nanoimprint resist is needed for reducing adhesion of nanoimprint molds to the substrate and improving quality of nanoimprinting. As shown in the AFM images below, mean roughness of surface of silicon nitride line was measured to be less than 10 Å, suggesting that surface of template obtained by PEDAL process is suitable for nanoimprinting.

Figure 4.11: AFM for measuring the surface roughness of silicon nitride lines on the nanowire template shown in figure 4.9
Metal Nanowires can be fabricated on-template without using nanoimprinting by doing lift-off of evaporated metal on template itself. In an attempt to demonstrate the usability of PEDAL template for making Palladium nanowires, 100 A of Palladium was evaporated on the template using e-beam evaporation method. The a-silicon layer was then selectively wet-etched in silicon etchant with gentle stirring which leaves palladium nanowire on silicon nitride layer. SEM in figure 4.12 shows the top view of palladium nanowires obtained by PEDAL lift-off technique and the figure 4.13 shows the comparison of template dimension and nanowire dimensions obtained lift-off.

![Figure 4.12](image1.png)

**Figure 4.12:** SEM of top view of nanowires obtained after lift-off of 100 A thick Palladium film on the template shown in figure.

The average width of the Pd nanowires obtained after lift-off was found to be 27.26 nm with the standard deviation of 2.28 nm and the average spacing was measured to be 14.83 nm with
standard deviation of 1.83 nm. This gives us the average pitch of the Pd nanowire arrays to be 41.89 nm with standard deviation of 3.30 nm.

Figure 4.13: Measured (a) line width, space width and (b) pitch on nanowire template before and after lift-off of 100 A thick Pd film.
These measurements show that after lift-off the width of the nanowire increases and spacing decreases from the value of the lines and spaces on the template. One of the reasons for observing increase in line width and decrease in space width might be improper lift-off. This can be due to deposition of the metal at the side walls of the a-silicon lines, which might not have been removed in lift-off. Since amorphous silicon films are non-conformal, side walls of the lines and spaces on the template are sloped. Ebeam evaporation might deposit metals on these sloped sidewalls. If the deposited metal film is not removed in the lift-off solution, which is the silicon etchant, then we can see the increase in nanowire width after lift-off. Sloped side-walls of lines and spaces on template can also be obtained if sidewalls of trench are non-vertical. Extremely high resolution imaging techniques like TEM is needed to further investigate but it’s excluded in the course of this research as the aim of the lift-off technique was to demonstrate the usability of PEDAL templates as lift-off template for making metal nanowires directly on the template without using nanoimprinting techniques.

4.3 22 nm pitch template

In another set of experiments, to scale down the line-width dimensions on template obtained by PEDAL process, attempt is made to fabricate sub 15 nm wide nanowires. The process is similar to the one described previously for making sub-25 nm nanowire molds. In order to evaluate the efficacy of PEDAL process for making nanoimprint mold of lines and spaces with width less than 15 nm, measurements are compared to the calculated values. Also, the planarity of the mold is determined from the SEM cross-section and AFM.
Figure 4.14: Run to run wafer scale average of LPCVD a-silicon film thickness at 535°C using 30% Silane (60 sccm) at 130 mTorr with total flow rate of 200 sccm for 3 min.

The graph in figure 4.14 shows run to run average amorphous silicon thickness deposited in 3 minutes using LPCVD process at 550°C and 130 mTorr using 30% Silane with total flow rate of 200 sccm. The wafer scale average amorphous silicon thickness varies from 126 Å to 142 Å with overall average value of 135.28 Å. The standard deviation of the film thickness from run to run for the deposition times of 3 minutes across 4 inch wafer ranges from 1 to 11 Å as shown in graph in figure 4.15.
Figure 4.15: Run to run wafer scale standard deviation of LPCVD a-silicon film thickness at 535°C using 30% Silane (60 sccm) at 130 mTorr with total flow rate of 200 sccm for 3 min.

Graph in figure 4.16 (a) shows run to run average silicon nitride thickness deposited in 3 minutes at 775°C and 300 mTorr using 120 sccm Ammonia gas and 40 sccm Dichlorosilane gases. Wafer scale average of silicon nitride film thickness obtained varies from 124.3 Å to 136.2 Å with overall thickness value of 131.45Å. Run to run standard deviation of film thickness across 4 inch wafer for the deposition time of 3 minutes ranges from 3 Å to 9 Å as shown in graph 4.16 (b).
Figure 4.16: (a) Run to run wafer scale average and (b) standard deviation of LPCVD silicon nitride film thickness at 775°C using 120 sccm Ammonia gas and 40 sccm dichlorosilane at 300 mTorr for 3 min

We can calculate widths of lines and spaces on PEDAL defined template obtained by PEDAL process using measured results from the deposition process of silicon nitride and a-
silicon thin films, each done for 3 minutes. If silicon nitride defines lines and amorphous silicon defines spaces, then from calculations we will get lines of average width of 131.45 Å and standard deviation between 3Å to 9Å, the values same as that of silicon nitride film thickness due to 100% conformality of film. Again considering the effect of nonconformality of deposited a-silicon films, average space width in the PEDAL template will be 110.9 Å with standard deviation less than 1nm. The graph in figure 4.17 shows the calculated run to run estimated pitch. The average of the estimated pitch of nanowire array in PEDAL defined template is 241.87 Å with the standard deviation of these average values of 4.10 Å.

![Graph showing average film thickness](image)

**Figure 4.17:** Calculated pitch of lines and spaces obtained on the PEDAL template after considering 81% conformality of a-silicon film and 100% conformality of silicon nitride film.
Figure 4.18: (a) (b) SEM of top view of PEDAL template shows 25 silicon nitride lines with average width of 13 nm spaced at average distance of 9 nm.
SEM in figure 4.18 shows the typical top view of nanowire template. Measurements of dimensions were done using the SEM images and conclusions are made based on measured values. As with the case of sub-25 nm nanowire template, care has been taken to minimize the errors associated with charging of the silicon nitride layer, and tilt in sample loading.

In order to assess the uniformity in the nanowire width and spacing of template across the entire 4 inch wafer, width of nanowire and space number 1 (from figure 4.18(b)) was measured and the results are shown in the graph in figure 4.19. From measurements, average width of line was found to be 13.1 nm with standard deviation of 2.6 A, whereas average spacing was found to be 8.0 nm with standard deviation of 5.1 A.

![Template lines and spaces](image)

**Figure 4.19:** Wafer scale measurement of first line and space shown in figure 4.18(b), gives average line width of 13.1 nm and space width of 8.0 nm.
Measurements were also done to assess the uniformity of the adjoining lines and spaces in an array on the template. These results are shown in figure 4.20. From the measurements it is observed that on the template average width of the line is around 13.12 nm with the standard variance of 2.7 Å and average spacing is around 9.42 nm with standard deviation of 9.1 Å. This gives us the average pitch of the lines on the template to be around 22.6 nm with the standard deviation of 9.32 Å. The value of silicon nitride lines on the template are close to the values calculated from the film thickness measurements shown in figure 4.16, which gives average width of lines as 131.45 Å. However, value of average space width on template is 70 % of the value calculated from film measurements instead of 81 %, possibly because of the underestimation of nonconformality of deposited a-silicon films with film thickness in sub-15 nm scale. Other factor can also be limitations of SEM technique as discussed earlier.

Figure 4.20: Measurement of lines and spaces in an array shown in figure 4.18(b), gives average line width of 131 Å and space width of 92 Å.
SEM of the cross-section of these templates and AFM of the surface of these templates were taken to determine the planarity of the molds. As shown in figures 4.21 and 4.22, the templates obtained show good planarity and the maximum difference between heights of silicon nitride lines is around 3 nm which is less than half of width of lines and spaces on the template. The nanoimprint template thus obtained can be used for nanoimprinting of lines and spaces with dimensions less than 15 nm. As mentioned earlier, silicon nitride line heights can be made more planar by repeating etch-recess-coat-repeat process until desired planarity is achieved depending on nanoimprinting needs.

Figure 4.21: SEM showing planarity of silicon nitride lines of nanoimprint template fabricated by PEDAL process.
Figure 4.22: AFM using super sharp tips, of the nanoimprint template fabricated by PEDAL process shows planarity of silicon nitride lines with maximum difference between heights of silicon nitride lines measured to be around 3 nm. Sharp edges are not observed in the AFM images due to AFM tip convolution.
PEDAL lift-off technique of 100 Å thick Pd films on these templates was not successful. One of the main problems encountered was the adhesion of metal on adjoining lines, probably due to sloped sidewalls of template lines or non-vertical evaporation of palladium, making the lift-off the palladium difficult in the lift-off solution. From the lift-off results on templates in both lots, it’s evident that as we scale down the dimensions, main challenge is not scaling of template line-widths but replicating these line-widths on the metal nanowires obtained after lift-off. This will require more engineering of the e-beam deposition and lift-off technique.

4.4 Results - Routing

One of the important attributes of PEDAL process for defining nanowires is its ability to route the sub-25 nm nanowires. In conventional photolithography, dimensions of the wires around the corners are limited by the optical interference which causes distortion of the developed resist profile. To take care of this problem, special mask designs which have optical proximity correction at the corners are needed. The mask design will become increasingly difficult as the dimensions of line-width structures scale down to sub-50 nm pitch. Since in PEDAL process such small dimensions of wires are obtained by thin film deposition, problems due to photolithography do not arise around the corners of the route. In PEDAL process, successful routing of nanowires greatly depends on the topography of trenches which are fabricated by either reactive ion etching or by using anisotropic wet etch solutions like KOH solution. Each of these methods has limitations which are discussed in detail in section 3.1.1. RIE experiments discussed in 3.1.2.2 were unable to provide vertical sidewalls of etched trenches and the best anisotropicity with the side wall
Figure 4.23: Shows nanowire routing capability of PEDAL process used to fabricate nanoimprint template.
angle of 15 was observed along the entire route for 20 sccm CHF₃ and 20 sccm O₂ at 30 mTorr and 150 W. Whereas in case of trench etching on Silicon<110> using 40 % by weight KOH solution, the sidewall angle was near 90 degrees along the linear region but along the corners, the sidewall angles deviated significantly from 90 (figure 3.15 and 3.16). This deviation was attributed to etch front planes different than vertical <-111> and <1-11> plane, which might be exposed because of rounding of the masking features at acute corners of the route due to photolithographic limitations. As mentioned in section 3.1.1.1, nanoimprint template with trench sidewall angle of 15 degree causes just 3 % deviation from the initial design values and can be used for nanoimprinting. Hence for demonstrating nanowire routing capability of the PEDAL process, RIE process has been used to define routes of trenches. Since these experiments were aimed at demonstrating various routing capability of lines on the nanowire template, SEM was done to verify the continuity of these lines around the corners of the route, without doing actual dimensional measurements. It will be logical to say that the uniformity analysis done in section 4.1 and 4.2 will also be applicable to the values of widths of lines and spaces around the corners as these values will depend on the thickness of deposited films irrespective of trench route. As shown in figure 4.23, PEDAL process retains continuity of lines along the corners without causing distortion in widths, and also provides good control of the routing of lines and spaces (4.23(e), 4.23(f)).

**Summary:**

In this chapter detailed processes used for the successful demonstration of fabrication of arrays of linewidth structures with 42 nm pitch and 22 nm pitch are discussed. It’s been observed that the wafer-scale uniformity and in-array uniformity of lines depend directly on
the wafer scale and run-to run uniformity of thin film deposition process. Conformality of films also greatly affects the widths of the lines and spaces on template and exact values of conformality are needed for successful design of experiments. Lift-off process poses another significant challenge in making on-template metal nanowires as final dimensions of metal nanowires not only depend on the sidewall angle and topography of template lines but also on the e-beam evaporation technique. For exact replication of the dimensions from mold onto metal nanowires, there is a need to avoid oblique evaporation on template and more lift-off experiments are needed in this direction.
5. PALLADIUM THIN FILMS AND NANOWIRES RESULTS

In section 4.2, results on array of palladium metal nanowires at 43 nm pitch obtained by lift-off technique were shown without discussing much about the electrical continuity of these nanowires. The PEDAL lift-off process failed to produce good results at 22 nm pitch due to adhesion of adjacent metal nanowires and one of the main reasons predicted was deposition of metals on the sidewalls of a-silicon lines. High resolution measurements like TEM is needed for further analysis and engineering of successful lift-off technique at such small dimensions. In this section results on electrical measurements of Palladium thin films and nanowires are presented. Parameters for different thin film resistivity models proposed [1-3] have been extracted from these thin film measurements which are subsequently been used to predict resistances of 100 micron long nanowires of different widths [4-8].

5.1 Palladium thin film resistivity

Resistivity of metal wires has been known to increase when lateral dimensions are scaled down to 100 nm and below. This is the region where lateral dimensions are comparable to mean free path of the electron. The phenomenon has been well established for long times in films and the most used theories and models are Fuchs and Sondheimer, and Mayadas and Shatzkes theory as discussed below.

A simplified form of Fuchs and Sondheimer (FS) theory [2, 3, 6] to express the electrical resistivity of thin films based on diffusive scattering (surface scattering) can be given by
where $\rho$ is the film resistivity, $l$ is the ratio of the film thickness $t$ to electron mean free path $\lambda$, $\rho_o$ is the resistivity of infinitely thick film or the bulk resistivity.

It was shown by Mayadas and Shatzkes [3, 8] that the experimentally measured resistivity not only depends on the ordinary Fuch’s size effect, but also on scattering due to grain boundaries and the effect of grain boundaries on resistivity is seen more in thinner films. The approximate expression for film resistivity, based on Mayadas and Shatzkes (MS) theory can be expressed by equation 28

$$\rho = \rho_o \{1 + \frac{3}{8l} (1 - p)\}, \quad l > 0.1 \quad \text{............................................................Equation 26}$$

$$l = \frac{t}{\lambda} \quad \text{..................................................................................................Equation 27}$$

$$\alpha = \frac{\lambda R}{d(1 - R)} \quad \text{..................................................................................................Equation 29}$$

where $d$ is the average grain diameter, $\lambda$ is mean free path of electron, $t$ is thickness of film, $R$ is the grain boundary reflection coefficient, $p$ is speculiarity parameter.

Very little study has been done to investigate size effect in nanowires where the dimensions have been reduced in two lateral dimensions perpendicular to the direction of electric current. Most of the studies involve nanowires with widths greater than 100nm where the size effect is very small. For smaller linewidhts and heights little data have been published for metals like copper, silver, gold and palladium. In order to predict the parasitic resistance of
nanowires, to be used in high density interconnects structures, it’s important to go beyond the usual consideration of resistivity as constant with respect to thickness and width, and to characterize size effect quantitatively in order to facilitate reliable predictions. Values of length, width and thickness of films and wires can be determined by physical measurements. However, specular parameter and reflection coefficient is determined by the fitting the resistivity values obtained by electrical measurements to simulated values. Values of mean free length of electron and bulk resistivity is determined by plotting product of resistivity and thickness versus thickness of films, which according to equation 1 should be straight line for thickness greater than 10% of mean free path of electrons. The slope of the graph will provide the bulk resistivity of metal and the intercept will give the value of $\lambda(1-p)$. The resistivity of thin films for various film thickness from 20 A to 200 A were measured using four point measurements on 4 inch wafer as shown in figure 5.1. The relation between measured voltage and applied current is given by equation 31-34. Resistivity values are plotted in figure 5.2.

Figure 5.1: Four point measurement technique to measure resistivities of thin films
\[ \rho = 2\pi s \frac{V}{I} F_1 F_2 F_3 \] \hfill \text{Equation 31}

\[ F_1 = \frac{t/s}{2 \ln(\sinh t/s/\sinh t/2s)} \] \hfill \text{Equation 32}

\[ F_2 = \frac{t/s}{2 \ln(\cosh t/s/\cosh t/2s)} \] \hfill \text{Equation 33}

\[ F_3 = \frac{\ln 2}{\ln 2 + \ln[(D/s)^2 + 3/(D/s)^2 - 3]} \] \hfill \text{Equation 34}

where \( t \) is thickness of film, \( s \) is distance between adjacent probes, \( D \) is the distance of probes from sample edges.

As shown in graph in figure 5.2(b), plot of product of measured resistivity and thickness shows linear dependence as predicted by equation 26 for the film thickness values greater than 100 A. The slope of the plot for thickness values greater than 100 A gives the bulk resistivity of palladium as \( 1.07 \times 10^{-6} \) ohm-m and \( \lambda (1-p) \) as \( 3.258 \times 10^{-8} \) m. Using the value of bulk resistivity and \( \lambda (1-p) \) obtained from above analysis, resistivity values obtained by Fuchs and Sondheimer theory is plotted for different film thickness as shown in figure 5.3.

Significant deviation of the values simulated using FS theory from the measured values was observed for thinner films because the resistivity due to grain boundary reflection is significant possibly due to smaller [9]. At higher film thickness, measured values match well
with simulated values as expected, because FS theory which neglects grain boundary scattering, will match the measured values only at higher thickness of films where the grains are bigger [9] causing less reflection of carriers.

Figure 5.2: (a), (b) Product of measured resistivity and film thickness plotted versus film thickness follows FS theory for higher thickness values.
Simulations were done using Mayadas and Shatzkes theory by using several values of specular coefficient and reflection coefficient in the range of 0 to 1. Good fit of simulated values to measured values was observed for the specular coefficient of 0.4 and reflection coefficient of 0.54 as shown in graph 5.3. Using the value of intercept obtained from the graph 5.2, mean free path of electron in palladium film was calculated to be 71.9 nm.

![Resistivity Vs. Pd. film thickness](image)

Figure 5.3: Shows the measured resistivity as well as the resistivity calculated using FS and MS theory.

5.2 Palladium nanowires

In order to determine the resistivity of palladium nanowires, templates were fabricated using the PEDAL Lift-off process designed for one nanowire. As mentioned earlier one of the limitations of using PEDAL process is looping of nanowires along trench boundaries. Hence to avoid looping, long trenches with open ends, routing straight from one end of the wafer to
the other end were fabricated. PEDAL process was modified as shown in figure 5.4 to get good insulation of palladium nanowires and the contacts from substrate and a-silicon layer. This was obtained by etching more a-silicon during palladium lift-off process, which increases the exposed surface area of silicon nitride line. Upon drying the template, silicon nitride lines are pulled to trench sidewalls due to stiction effect, giving insulation of amorphous silicon layer as shown in SEM in figure 5.5.

Figure 5.4: Modification of PEDAL process to fabricate single nanowire. (a) deposition of insulating silicon nitride layer on the trench prior to other steps of PEDAL, (b),(c) planarization, silicon nitride selective wet etch and ebeam deposition of metal (d) lift-off of metal causes stiction effect and insulation of a-silicon layer.
In above experiment, 100 micron long nanowires with widths of 24 nm, 38 nm and 47 nm were fabricated. Resistances were measured at very low current density, less than $5 \times 10^4$ Amp/cm$^2$, with applied current less than 500 nAmps. These measurement conditions assured no electromigration failure which otherwise would have been observed for higher current densities. Contacts to these wires were made by e-beam deposited 1500 A thick aluminium metal pads.

![SEM of cross section of template obtained after lift-off of metal shows insulation of a-silicon layer due to stiction effect.](image)

**Figure 5.5:** SEM of cross section of template obtained after lift-off of metal shows insulation of a-silicon layer due to stiction effect.

A model that employs physical parameters has been used for analysis of the nanowire resistivity data. It is based on the work of FS and MS theory explained earlier. The compact version of this model [4, 5, 7] is as follows.

$$
\rho = \rho_0 \left\{ \frac{1}{3(1 - \frac{1}{2} \alpha + \alpha^2 - \alpha^3 \ln(1 + \frac{1}{\alpha}))} \right\} + \frac{3}{8} C(1 - p) \frac{1 + AR \lambda}{AR \frac{w}{w}}, \quad \lambda > 0.1 \quad \text{Equation 30}
$$

$$
\alpha = \frac{\lambda R}{d(1 - R)}
$$

$$
AR = \frac{t}{w} \quad \text{Equation 31}
$$
C = 1.2 for rectangular cross-section of wires

Here C is a constant depending on the profile of cross-section of the wires, AR is the aspect ratio.

Figure 5.6: (a) simulated resistivity and (b) simulated and measured resistance of 100 micron long and 100 A thick nanowires with varying widths (c) Schematic of I-V measurement technique for measuring wire resistance (d) Typical I-V curve of palladium nanowires.
Using values of specular coefficient, reflection coefficient, mean free path of electron and bulk resistivity of palladium films determined from thin film measurements, simulations were done based on equation 30 to predict the resistivity and resistance of 100 micron long nanowires of varying widths and fixed thickness/height of 100 A. Graph 5.6 shows that resistance due to grain boundary scattering remains constant with varying width as grain size mainly depends on thickness and not on length and width of nanowires. However, resistivity due to surface scattering increases with decrease in nanowire width, suggesting more surface effect in narrower nanowires. Hence, increase in resistivity of nanowires at smaller widths can be attributed to the increase in surface scattering. Using the simulated resistivity values, resistance of palladium nanowires was calculated using the relation $R = \rho l/A$. As shown in graph 5.6(b), four-point resistance measurements showed more deviation from the simulated values for the case of narrower nanowires of width 240 A than for the wider nanowires of width 470 A.

For the nanowires with average width of 24 nm and length 100 microns, the measured resistance was 17.5 Mohms, which is around three times the simulated resistance of 5.18 Mohms. For nanowires with average width 47 nm and length 100 microns, the measured resistance was 5.96 Mohms which is around twice the simulated resistance 3.29 Mohms. With the experimental results mentioned in this chapter, it’s very premature to give the exact reason for this deviation of measured values from the simulated results. Some of the reasons can be incorrect determination of specular and reflection coefficient, and distance between grain boundaries not really equal to the thickness of the film as assumed. More experiments and measurements are needed to determine exact model for predicting nanowire resistance,
however it’s been excluded in this research as the main aim of this experiments was to find the electrical continuity of nanowires, which is very well proved to be true by measured conductivity of these wires.

Summary

In this chapter, electrical characteristics of palladium thin films and palladium nanowires are discussed. PEDAL process was modified to get the insulation of contacting pads to the substrate and the a-silicon layer by using the property of stiction between two surfaces in contact with the evaporating liquid. Also, an attempt has been made to get the understanding of scattering mechanisms in thin films based on widely used Fuchs and Sondheimer, and Mayadas and Shatzkes theory. It’s been found that resistivity of thin films increases with decrease in film thickness due to increased grain boundary scattering. From the measurements of resistances of nanowires it’s been found that for particular thickness/height of wires, surface scattering increases as we decrease the width of wires. Although exact model to predict the resistance of nanowires was not obtained due to restrictions imposed by design of experiment and limited understanding of the cross-section of metal nanowires, the electrical continuity of wires is successfully demonstrated.
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CHAPTER 6

6. CONCLUSION

The main focus of this entire project was to address the key issue of nanofabrication which is lithography. Conventional lithography techniques, like e-beam lithography, EUV, Focused ion-beam are widely researched and developed lithography processes and are commercially available. Although, high cost of the whole lithography process using these conventional techniques is a key issue, it’s not limiting its use in semiconductor industry. However, in capital intensive semiconductor industry there is always the need for cost-effective, reliable and high yield alternative techniques. To assist in reducing costs of fabrication, unconventional lithographic techniques like nanoimprinting have immerged from the research in the university labs to the level of global commercialization. This unconventional technique is not used stand-alone but in conjunction with the conventional techniques to achieve the objective. The research presented in this thesis is also intended to assist the semiconductor industry, sensor industry and research labs to achieve one goal, which is cost-effective, reliable and controlled fabrication of wafer-scale nanowire arrays. There are numerous, current as well as future applications of arrays of metal, semiconductor or insulator nanowires (appendix A) and Planar Edge Defined Alternate Layer process definitely can make significant contribution to such applications. Other than ease of fabrication technique, “true” wafer-scalability and relatively low cost of fabrication of nanowires using PEDAL process, one of the significant aspect of this technique is it’s scaling ability. In conventional techniques where light source, optics of the system and resist decide the resolution of the lithography technique, in PEDAL it is simply dependent on thickness of thin
films. Thinner the films, narrower are the nanowires. In this project, which is first effort on PEDAL technique, nanowires as small as 13 nm and spaces as small as 8 nm have been readily achieved. With great sense of optimism it can be said that with more experiments and using different materials and deposition techniques like Atomic Layer Deposition, nanowire template with line width as small as 5 nm or even narrower can be readily achieved, the challenge which still exists in conventional techniques. Other important feature of PEDAL technique, also recognized by the other researchers, is its routing ability. In conventional techniques, due to the optical interference or interaction of electrons, line widths around the corners of the route are distorted. Complicated mask designs involving optical proximity corrections are needed to correct this distortion. As we scale down the dimensions, designing such masks becomes increasingly difficult. In PEDAL process this issue is inherently taken care of by conformal thin film deposition and no such problem in routing is foreseen as we scale down the dimensions of nanowires. Process tolerance is one of the deciding factors of accepting any process in manufacturing environment. In this thesis, it’s been proposed methodically using simulations, how the PEDAL process can be made tolerant to various processing steps, mainly conformality of thin films and selectivity of planarizing RIE recipes. The success of this process is also demonstrated by the good dimensional control and wafer scale uniformity of the line widths fabricated using PEDAL process.
APPENDIX A: APPLICATION OF NANOWIRES.

Metal, semiconductor and insulator nanowires have many applications ranging from chemical and biological sensors, high frequency electromechanical resonator, Nano-electromechanical switches to high density cross-bar memory structures. In this section I have briefly summarized some of current and future applications of nanowires. As with the case of nanoimprinting using mold patterned with conventional photolithography, the alignment of the imprinted patterns using PEDAL defined template also depends on the preciseness of nanoimprinting tools and technique, as well the patterns on mold itself. As mentioned earlier, PEDAL process gives nanoimprint template with precise location, length and route of nanowires, with accuracy depending on the lithography technique used to define trenches. In all applications of nanowires discussed in this chapter, nanoimprinting using PEDAL process defined template can be adopted, but complete integration with subsequent processes will rely on the nanoimprinting technique. Alternatively for simple applications like sensors, on-template lift-off process can be used to make nanowires of desired material which can be directionally deposited on the template. Getting the template itself requires several processing steps like RIE and LPCVD and hence more ingenuity will be required in integrating the PEDAL lift-off technique with the other processing steps. In this chapter, only applications of nanowires and line-width structures are discussed and no process integration study is been done, as it will require complete knowledge of the subsequent process steps.
1) Tin-oxide Gas sensors

Researchers from the University of California at Santa Barbara, US, have produced 60 nm-diameter wires from tin oxide (SnO$_2$). This is significant, as this is the most widely used gas sensing material, forming the basis of most semiconductor gas sensors. At around 60 nm, the nanowires are so small that surface gas adsorption alters their bulk electronic structure and tests have shown that they act as conductors in the absence of oxygen, but become insulators when this gas is present. Combustible gases such as carbon monoxide increase the wire’s conductivity. The group has also fabricated a novel type of GASFET using these nanowires. This uses a 60nm wire, several microns long, deposited onto a 300 nm-thick SiO$_2$ film grown thermally on a heavily boron-doped (0.02Vcm) silicon substrate (Figure A1). The substrate is used as the gate electrode and the source and drain electrodes are Ti (20 nm) and Au (200 nm) micropads, vapour deposited on the ends of the SnO$_2$ nanowire. These GASFET structures gives increased sensitivity to presence of gases and can easily be integrated with planar electronic technologies with multiple, individually-addressable active elements. An application could be indoor air quality, where the arrays would provide an instantaneous, spatially-coherent measure of the chemical composition of an entire building’s atmosphere. This could yield highly sensitive, intelligent sensors which, in time, could mimic the sensing capability and cognitive pattern-recognition abilities of a mammalian nose.
Figure A1: Gas sensing tests on individual nanowires as a function of temperature and (flowing) ambient gas composition (a) SnO$_2$ nanowires deposited on SiO$_2$/Si, outfitted with vapor-deposited Au/Ti electrodes. I-V characteristics for nanowire measured in (b) inert (c) in oxidizing environment (d) The log of conductance versus temperature for individual nanowire in dry N$_2$ and N$_2$ + 10 % O$_2$ atmospheres.

Reference:


[2] Klmakov, A; Zhang, Y; Cheng, G; Moskovits, M; Advanced Materials 2003, 15, No. 12, 997-1000
2) Hydrogen Sensor

Hydrogen sensors and hydrogen-activated switches were fabricated from arrays of mesoscopic palladium wires. Researchers prepared palladium mesowire arrays by electrodeposition onto graphite surfaces which later were transferred onto a cyanoacrylate film (figure A2). Exposure to hydrogen gas caused a rapid (less than 75 milliseconds) reversible decrease in the resistance of the array that correlated with the hydrogen concentration over a range from 2 to 10%. The sensor response appears to involve the closing of nanoscopic gaps or break junctions in wires caused by the dilation of palladium grains undergoing hydrogen absorption. Wire arrays in which all wires possessed nanoscopic gaps reverted to open circuits in the absence of hydrogen gas. The morphology of the nanowires was analyzed using SEM and AFM in order to understand the properties responsible for the high sensitivity of the nanowires. SEM images showed that the nanowires contain nanogaps in absence of H$_2$. Upon exposure to H$_2$, the Pd absorbed hydrogen, resulting in the expansion of Pd grains. This expansion results in the closing of the nanogaps (Figure A3).

Reference:

[1] Favier, F; Walter, E; Zach, M; Benter, T; Penner, R; Sceince, Volume 293, 21, 2227-2230 (2003).
Figure A2: (A) Schematic diagram of a PMA-based hydrogen sensor or switch. (B) SEM image [400 um (h) by 600 um (w)] of the active area of a PMA-based hydrogen sensor. (C) PMAs were prepared by electrochemical step edge decoration at graphite surfaces and transferred to a cyanoacrylate film.

Figure A3: The first exposure of a new sensor to hydrogen. In this case, an irreversible transition from mode I to mode II operation was observed (bottom). Mechanism proposed for mode II sensor operation (top). Mode I sensors operate by an identical mechanism, with some mesowires remaining conductive in the H₂.
3) Silicon Nanowire Sensors

Planar semiconductors can serve as the basis for chemical and biological sensors in which detection can be monitored electrically and/or optically (1-4). For example, a planar field effect transistor (FET) can be configured as a sensor by modifying the gate oxide (without gate electrode) with molecular receptors or a selective membrane for the analyte of interest; binding of a charged species then results in depletion or accumulation of carriers within the transistor structure (1, 2). An attractive feature of such chemically sensitive FETs is that binding can be monitored by a direct change in conductance or related electrical property).

The physical properties limiting sensor devices fabricated in planar semiconductors can be readily overcome by exploiting nanoscale FETs (5-9). First, binding to the surface of a nanowire (NW) or nanotube (NT) can lead to depletion or accumulation of carriers in the "bulk" of the nanometer diameter structure (versus only the surface region of a planar device) and increase sensitivity to the point that single-molecule detection is possible. Second, the small size of NW and NT building blocks and recent advances in assembly (9, 10) suggest that dense arrays of sensors could be prepared. Indeed, NT FETs were shown recently by Dai and co-workers to function as gas sensors (11). Calculations suggested that direct binding of electron-withdrawing NO\textsubscript{2} or electron-donating NH\textsubscript{3} gas molecules to the NT surface chemically gated these devices.

Boron-doped silicon nanowires (SiNWs) were used to create highly sensitive, real-time electrically based sensors for biological and chemical species. Amine- and oxide-functionalized SiNWs exhibit pH-dependent conductance that was linear over a large dynamic range and could be understood in terms of the change in surface charge during
protonation and deprotonation. Biotin-modified SiNWs were used to detect streptavidin down to at least a picomolar concentration range. In addition, antigen-functionalized SiNWs show reversible antibody binding and concentration-dependent detection in real time. Lastly, detection of the reversible binding of the metabolic indicator Ca$^{2+}$ was demonstrated. The small size and capability of these semiconductor nanowires for sensitive, label-free, real-time detection of a wide range of chemical and biological species could be exploited in array-based screening and in vivo diagnostics.

References:


Fig. A4: NW nanosensor for pH detection. (A) Schematic illustrating the conversion of a NWFET into NW nanosensors for pH sensing. The NW is contacted with two electrodes, a source (S) and drain (D), for measuring conductance. (zoom)APTES-modified SiNW surface illustrating changes in the surface charge state with pH. (B) Real-time detection of the conductance for an APTES modified SiNW for pHs from 2 to 9; the pH values are indicated on the conductance plot. (inset,top). Plot of the time-dependent conductance of a SiNW FET as a function of the back-gate voltage (inset,bottom) Field-emission scanning electron microscopy image of a typical SiNW device. (C) Plot of the conductance versus pH; the red points are experimental data, and the dashed green line is linear fit through this data. (D) The conductance of unmodified SiNW (red) versus pH. The dashed green curve is a plot of the surface charge density for silica as a function of pH.
4) **Piezo resistors for mechanical sensors**

Piezoresistance effect is widely used as a sensing principle of integrated pressure sensors, accelerometers, and atomic force microscopy (AFM) cantilevers. Especially for the AFM cantilevers, there are two major detection methods. One is piezoresistive detection and the other is optical laser detection. In general, the optical detection has higher sensitivity than the piezoresistive detection. Therefore, the piezoresistive cantilever is used for large arrays of data storage cantilevers, ultra-small high-bandwidth cantilevers and bio-chemical mass sensing, such as DNA (deoxyribonucleic acid) mass in a micro fluid channel where optical detection is difficult to apply. However, a drawback of less sensitivity in the conventional piezoresistive cantilever gives a limitation for MEMS applications. In order to improve sensitivity, Harley and Kenny published excellent consideration for design and process of the piezoresistive cantilever. According to them, resistance change in an ideal piezoresistive cantilever having rectangular shape is given by

\[
\frac{\Delta R}{R} = \frac{6\pi l}{wt^2} F
\]

where \(\pi_l\) is longitudinal piezoresistance coefficient, \(l\) is length, \(w\) is width, \(t\) is thickness and \(F\) is applied force. The resonance frequency is proportional to \(t/l^2\) and spring constant is proportional to \(t^3/l^3\). Based on this preliminary consideration, the resistance change and bandwidth for the piezoresistive cantilever with specified spring constant are increased by decreasing thickness and mass with keeping \(t/l\) constant. Recent progress of the piezoresistive cantilever fabrication process contributes to realize submicron thickness cantilever with fN of force resolution. However, in order to achieve higher force resolution,
i.e., below fN resolution, reduction of thickness and mass of the piezoresistor and the cantilever to nanometric scale must be done as deduced from (1). This resolution is necessary to detect masses of ultrasmall objects such as molecule and ion, which are main targets in the biochemical sensing. A p-type silicon (Si) nanowire piezoresistor, whose minimum cross-sectional area is 53 nm 53 nm (figure A5), was fabricated by combination of thermal diffusion, EB (electron beam) direct writing and RIE (reactive ion etching). The maximum value of longitudinal piezoresistance coefficient [011] of the Si nanowire piezoresistor was found to be 48X10^{-5} (1/MPa) at surface impurity concentration of 5 X 10^{19} (cm^3) and it has enough sensitivity for mechanical sensor applications. The longitudinal and transverse piezoresistance coefficient [011] of the Si nano-wire piezoresistor increases with decrease in the cross-sectional area giving increased sensitivity to applied force as implied by equation (1).

Figure A5: (a) SEM image of Silicon nanowire (b) size effect on longitudinal and transverse piezoresistance coefficient.
Table 1: Geometry and resistivity of silicon nanowires.

<table>
<thead>
<tr>
<th>No.</th>
<th>Thickness (nm)</th>
<th>Width Top (nm)</th>
<th>Width Mean (nm)</th>
<th>Width Bottom (nm)</th>
<th>Length (µm)</th>
<th>Cross section area (nm²)</th>
<th>Aspect ratio</th>
<th>Resistance (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>53</td>
<td>30</td>
<td>53</td>
<td>75</td>
<td>3</td>
<td>4065</td>
<td>1.01</td>
<td>56.7</td>
</tr>
<tr>
<td>2</td>
<td>65</td>
<td>54</td>
<td>101</td>
<td>147</td>
<td>3</td>
<td>6482</td>
<td>0.65</td>
<td>24.2</td>
</tr>
<tr>
<td>3</td>
<td>65</td>
<td>63</td>
<td>133</td>
<td>202</td>
<td>3</td>
<td>8731</td>
<td>0.49</td>
<td>18.3</td>
</tr>
<tr>
<td>4</td>
<td>65</td>
<td>163</td>
<td>233</td>
<td>302</td>
<td>3</td>
<td>15231</td>
<td>0.28</td>
<td>10.4</td>
</tr>
<tr>
<td>5</td>
<td>65</td>
<td>263</td>
<td>333</td>
<td>402</td>
<td>3</td>
<td>28231</td>
<td>0.20</td>
<td>7.3</td>
</tr>
</tbody>
</table>

Reference:

5) Nanowire LEDs

Nanowires and nanotubes carry charge and excitons efficiently, and are therefore potentially ideal building blocks for nanoscale electronics and optoelectronics. Carbon nanotubes have already been exploited in devices such as Feld-effect and single electron transistors, but the practical utility of nanotube components for building electronic circuits is limited, as it is not yet possible to selectively grow semiconducting or metallic nanotubes. Researchers have shown the assembly of functional nanoscale devices from indium phosphide nanowires, the electrical properties of which are controlled by selective doping. Gate-voltage dependent transport measurements demonstrate that the nanowires can be predictably synthesized as either n- or p-type. These doped nanowires function as nanoscale feld-effect transistors, and can be assembled into crossed-wire p-n junctions that exhibit rectifying behavior. Significantly, the p-n junctions emit light strongly and are perhaps the smallest light-emitting diodes that have yet been made (figure A6). Taken as a whole, the results provide a rational approach for the bottom-up assembly of nanoscale electronic and optoelectronic devices. The demonstrated ability to assemble active devices in the absence of multi-billion-dollar fabrication lines is critically important to the field. The broad range of nanowire materials now available and the clearly defined ability to control their electronic properties will make possible nanoscale LEDs that cover the entire visible and near-infrared range (for example, GaN nanowires for blue colors). These Nanoscale light sources might be useful in creating new types of highly parallel sensors and for optical interconnects in nanoelectronics.

Reference:
Figure A6: Parallel and orthogonal assembly of nanowires with electric fields. (a), Schematic view of alignment by electric field. The electrodes (shown orange) are biased at 50±100 V after a drop of nanowire solution is deposited on the substrate (blue). (b) Parallel array of nanowires aligned between two parallel electrodes. The nanowires were suspended in chlorobenzene and aligned using an applied bias of 100 V. (c) Spatially positioned parallel array of nanowires obtained following electric-field assembly using a bias of 80 V. Inset, 15 pairs of parallel electrodes with individual nanowires bridging each diametrically opposed electrode pair. (d) Crossed nanowire junction obtained using layer-by-layer alignment with the electric field applied in orthogonal directions in the two assembly steps. The applied bias in both steps was 80 V. Scale bars in b-d, 10um.
Figure A7: Optoelectrical characterization of nanowire p-n junctions. (a) Electroluminescence (EL) image of the light emitted from a forward-biased nanowire p-n junction at 2.5 V. Inset, photoluminescence (PL) image of the junction. Scale bars, 5mm. (b) I-V characteristics; inset in this inset, FE-SEM image of the junction itself. (Scale bar is 5 um). The n-type and p-type nanowires forming this junction have diameters of 65 and 68 nm, respectively. (c) EL spectrum of the junction shown in a (d) EL spectrum recorded from a second forward-biased crossed nanowire p-n junction. Inset, EL image shows that the EL originates from the junction region. The n-type and p-type nanowires forming this junction have diameters of 39 and 49 nm, respectively.
6) Logic Gates and Computation from Assembled Nanowire Building Blocks

Miniaturization in electronics through improvements in established top-down fabrication techniques is approaching the point where fundamental issues are expected to limit the dramatic increases in computing seen over the past several decades. Researchers have proposed an approach in which functional device elements and element arrays have been assembled from solution through the use of electronically well-defined semiconductor nanowire building blocks. They have shown that crossed nanowire p-n junctions and junction arrays can be used to create integrated nanoscale field-effect transistor arrays with nanowires as both the conducting channel and gate electrode. Nanowire junction arrays have been configured as key OR, AND, and NOR logic-gate structures with substantial gain and have been used to implement basic computation (figure A8). A two-input OR gate was realized by using a 2(p) by 1(n) crossed p-n junction array with the two p-Si NWs as inputs and the n-GaN NW as the output. Also note that assembly of more p-n junctions would produce a multiple input OR gate, i.e., a 1 by \( n \) junction array for an \( n \)-input OR gate. An AND gate can be fabricated from a 1(p-Si) by 3(n-GaN) multiple junction array. In this structure, the p-Si NW is biased at 5 V; two of the GaN NWs are used as inputs, and the third is used a gate with a constant voltage to create a resistor by depleting a portion of the p-Si NW. A logic NOR gate was assembled by using a 1(p-Si) by 3(n-GaN) cNW-FET array. The NOR gate was configured with 2.5 V applied to one cNW-FET to create a constant resistance of 100 megohms, and the p-SiNW channel was biased at 5 V. The two remaining n-GaN NW inputs act as gates for two cNW-FETs in series. In this way, the output depends on the resistance ratio of the two NW-FETs and the constant resistor.
Figure A8: Nanowire nano-logic gates. (A) Schematics of logic OR gate constructed from a 2 by 1 crossed NW p-n junction. (B) The output voltage versus the four possible logic address level inputs: (0,0); (0,1); (1,0); (1,1), where logic 0 input is 0 V and logic 1 input is 5 V. (Inset) The output-input (Vo-Vi) relation. The solid and dashed red (blue) lines show Vo-V_{i1} and Vo-V_{i2} when the other input is 0 (1). (C) The experimental truth table for the OR gate. (D) Schematic of logic AND gate constructed from a 1 by 3 crossed NW junction array. (E) The output voltage versus the four possible logic address level inputs. (Inset) The Vo-Vi, (F) The experimental truth table for the AND gate. (G) Schematic of logic NOR gate constructed from a 1 by 3 crossed NW junction array. (H) The output voltage versus the four possible logic address level inputs. (Inset) The Vo-Vi relation. The slope of the data shows that device voltage gain is larger than 5. (I) Measured truth table for the NOR gate.
Figure A9: Nanowire computation. (A) Schematic of logic XOR gate constructed with the output from an AND and a NOR as the input to a second NOR gate. (B) Schematic for logic half adder. (C) Truth table for logic XOR gate. (D) XOR output voltage versus input voltages. The solid and dashed red (blue) lines show $V_o-V_{i1}$ and $V_o-V_{i2}$ when the other input is 0 (1). The slope of the $V_o-V_i$ data shows that the gain exceeds 10. The XOR gate was achieved by connecting the output electrodes of an AND and NOR gate to two inputs of another NOR gate. (E) The output voltage versus the four possible logic address level inputs for the XOR gate. (F) Experimental truth table for the logic half adder. The logic half adder was obtained by using the XOR gate as the SUM and an AND gate as the CARRY.

Reference:

[1] Huang, Y; Duan, X; Cui, Y; Lauhon, L; Kim, K; Lieber, C; Science, Vol 294, 1313-1317.
7) Cross-Bar memory

In order to realize functional nano-electronic circuits, three problems need to be solved: invent a nanoscale device that switches an electric current on or off; build a nanoscale circuit that controllably links very large numbers of these devices with each other and with external systems in order to perform memory and/or logic functions; and design an architecture that allows the circuits to communicate with other systems and operate independently of their lower-level details. At the device level, researchers in molecular electronics have achieved significant progress recently, demonstrating tunneling junction, and devices with negative differential resistance, electrically configurable switches and transistors made from a single carbon nanotube, or a single molecule. At the circuit level, devices have been connected together to separately perform basic memory and logic functions. Architectural issues are still in the early stages, but designs suitable for nano-electronic circuits have been discussed and patented. To satisfy all three of the above requirements, researchers at Hewlett Packard proposed nanoscale circuits based on configurable crossbar architecture to connect molecular switches in a two-dimensional grid. A crossbar has several advantages. First, the wire dimensions can be scaled continuously down to molecular sizes, while the number of wires in the crossbar can be scaled up arbitrarily to form large-scale generic circuits that can be configured for memory and/or logic applications. Second, it requires only $2^N$ communication wires to individually address $2^N$ nanowires with a demultiplexer, which allows the nanocircuit to communicate efficiently with external circuits and systems, for example, CMOS. Third, it is a reconfigurable architecture that can tolerate defective elements generated during the nanofabrication process. Fourth, the simple physical structure of the crossbar makes nanoscale fabrication feasible and potentially inexpensive.
Molecular electronics offers the prospect of scaling device dimensions down to a few nanometers, which is not possible for Si-based devices. However, the density of circuits with molecular components is still limited by the lithography used in electrode and connection fabrication. For practical reasons, not only high resolution but also low cost and high throughputs are required for lithography geared for manufacturing. However, today’s production tools do not yet have the resolution to produce 30-nm half-pitch structures. Stanley’s group at Hewlett Packard has reported the fabrication of a 1-kbit cross-bar molecular memory (figure A10) at an unprecedented density of 28 Gbits/cm² (30-nm half-pitch) using nanoimprint lithography. The memory density can be greatly increased by reducing the pitch even further.

Reference:

[1] Wu,W; Jung, G-Y; Olynick, D; Straznicky, J; Li, Z; Li, X; Ohberg, D; Chen, Y; Wang, S-Y; Liddle, J; Tong, W; Williams, S; Applied Physics A, 80, 1173-1178 (2005).

[2] Chen, Y; Jung, G-Y; Ohlberg, D; Li, X; Stewart, D; Jeppesen, J; Nielsen, K; Stoddart, J; Williams, S; Nanotechnology, 14, 462-468 (2003).
FIGURE A10: (a), (b) Top view of imprinted cross-bar memory structure (c) Schematic representation of the crossbar circuit structure. A monolayer of the [2]rotaxane (green) is sandwiched between an array of Pt/Ti nanowires (gold, left–right) on the bottom and an array of Pt/Ti nanowires (gold, up–down) on the top. (d) Electronic characteristic of a single device measured from an on-chip control device (rotaxane molecule). It shows the switching hysteresis.
8) Array Based architecture for FET based nanoscale electronics

Advances in our basic scientific understanding at the molecular and atomic level place us on the verge of engineering designer structures with key features at the single nanometer scale. This offers us the opportunity to design computing systems at what may be the ultimate limits on device size. At this scale, we are faced with new challenges and a new cost structure which motivates different computing architectures than we found efficient and appropriate in conventional very large scale integration (VLSI). Researchers have sketched a basic architecture for nanoscale electronics based on crossing arrays of carbon nanotubes, silicon nanowires, and nano-scale FETs (figure A11). This architecture can provide universal logic functionality with all logic and signal restoration operating at the nanoscale. The key properties of this architecture are its minimalism, defect tolerance, and compatibility with emerging bottom-up nanoscale fabrication techniques. The architecture further supports micro-to-nanoscale interfacing for communication with conventional integrated circuits and bootstrap loading.

The molecular-scale wires can be arranged into interconnected, crossed arrays with nonvolatile switching devices at their cross-points; these crossed arrays can function as programmable-logic arrays and programmable interconnect. Using nanoscale FET devices provides both signal restoration and programming support for the nonvolatile switches. The result is a programmable logic device that can be configured to compute any logical function and that operates entirely at the nanoscale. Defect-tolerance is an essential component of this architecture allowing it to cope with the high defect rates associated with bottom-up synthesis.
The architecture sketched here is an existence proof, demonstrating a complete, plausible scheme for achieving molecular-scale logic from these building blocks. There are numerous components of the architecture that certainly merit further optimization (e.g., energy reduction, decoder fabrication, array customization, self programming, and yield enhancements). At this point, even the detailed behavior of the basic wires and devices are highly experimental. Assembly procedures and reliability are active areas of current research. Many of the components here may not be feasible or operational as currently envisioned. Nonetheless, there are many technological alternatives available for each of the key components, and it seems likely that we can find at least one viable path through the emerging set of technologies. Simultaneous development of architecture with technology allows us to see what the emerging technology can and cannot do and push back on the technology development to engineer the essential features, which will make the technology viable for implementing computations.

Figure A11: overall assembly of functional nanowires.
Figure A12: (a) Diode OR arrangement (b), (c) Programmable DIODE OR array.

Figure A13: (a) FET logic arrangement (b) NT-NW FET arrangement

Reference:


9) ROOM TEMPERATURE SINGLE ELECTRON MEMORY

Among a variety of proposed single-electron devices, the single-electron memory, has the special importance in the light of use in large scale integrated (LSI) circuits. There are two reasons to emphasize memory rather than logic. One attractive aspect is that we can use single-electron devices only in a memory cell, whereas we keep using conventional CMOS technology in the peripheral circuitry. Changing everything on the chip from the conventional technology to the new one is difficult in the sense of technology itself as well as economics and human factors. The above hybrid approach is a far more realistic scenario. Another reason is the fundamental difficulty with the single-electron device when it is used in a logic functional unit. The communication with another distantly placed logic unit is a fundamental requirement for a logic device. However, the single-electron devices (generally) have poor current-drive capability and are far inferior in such communication capability as compared to conventional CMOS devices. Although no one can deny the possibility of future emergence of clever ideas to overcome this difficulty, it strongly limits the use of those devices in logic circuits. Recently, researches in this field have also been placing more emphasis on memory. The first device clearly aimed at single-electron memory operation was made and analyzed by Nakazato et al.. The device had write, read, and retention functions using GaAs/AlGaAs structures, and the measured characteristics were confirmed to agree with Coulomb blockade model. Dresselhaus et al. also demonstrated metal-based memory device based on Al/Al₂O₃ technology and obtained similar results. All these experiments were conducted at very low temperatures. To understand in-depth physics, low-temperature operation is not a problem or may be desirable. However, to apply these devices in electronics, low-temperature operation strongly limits the range of applicable field, and the
potential impact on the industry/society. However, room-temperature operation requires large Coulomb energy accomplished only with sub-10-nm structure, which is beyond the current lithography limitation.

The first room-temperature memory device based on single-electron tunneling was operated by Kazuo Yano’s et.al. Their idea was to use very thin poly-silicon with film thickness below 10 nm, in which nanostructures were naturally formed, making an abrupt surge of operating temperature to room temperature possible. Based on this structure, operation of single electron transistor and synchronous single-electron transfer device at room temperature has also been demonstrated. The poly-Si was suitable for reducing parasitic capacitances around the active region when it is surrounded by silicon dioxide film. The fabricated device was an ultrathin-film transistor with channel poly-Si width and gate lengths of 100 nm. The channel poly-Si (or nano-Si) was as thin as 3.4 nm on the average (figure A14). They used the same concept to demonstrate an array of 8 x 8 array of memory using cross arrangement (figure A15). This memory-cell array consists of ladder-shaped poly-Si lines, in which channel poly-Si corresponds to a rung and data/source poly-Si lines correspond to side pieces. A group of channel poly-Si’s covered by a word line constitutes a sector, the basic write/read unit. The source line is shared by two adjacent cells to reduce the cell area, yielding a $6F^2$ cell area, where $F$ is the feature size.
Figure A14: (a) The SEM microphotograph of the fabricated memory. Nano-Si is sandwiched by amorphous silicon dioxide (b) Measured drain current versus gate voltage. The drain-source voltage is 50 mV. The gate-voltage sweep rate is 4 V/min. The maximum gate voltage in a sweep loop is: (a) 24 V (○); 28 V (□); 32 V (♦); 36 V (•); 40 V (■); (b) 44 V (♦); 48 V (•); 52 V (■); and (c) 56 V (•); and 60 V (■).
Figure A15: (a) Schematic structure of ladder-shaped Coulomb memory cell array. Word line (WL), data line (DL), and source line (SL) are poly-Si. (b) microphotograph of an 8 X 8-bit memory-call array (c) Schematic of read-write operation of memory.

REFERENCE:

[18] YANO, K; ISHI, T; SANO, T; MINE, T; MURAI, F; HASHIMOTO, T; KOBAYASHI, T; KURE, T; PROCEEDINGS OF IEEE, VOL. 87, NO. 4, 633-651 (1999)
APPENDIX B: LOOPING

As mentioned in Chapter 1, one of the issues in making nanoimprint mold of arrays of nanowires using PEDAL process is the looping of the nanowires as shown in figure below. This looping of lines will also be observed on the thermal resist after nanoimprinting as well as after fabricating metal nanowires on the template by lift-off technique. In case of lift-off technique the looping can be eliminated by selective etching of the metal in these loops, thus requiring one photolithography and etching step (figure B1)

Figure B1: (a) Looping of lines and spaces on template fabricated by PEDAL process (b) Mask for the etch step to eliminate looping on template.

However in case of nanoimprinting, looping of imprinted lines can be eliminated by using the property of selective planarization in Scheme C (figure 3.40). Selective planarization gives planar surfaces on the narrower trenches whereas wider trenches will
Figure B2: (a) Topography of narrow trenches is more planar after deposition of stack and buffer a-silicon layer followed by spin coat (b) non-selective RIE process gives leveled surface suitable for nanoimprinting features in the stack in case of narrow trenches (c) Polymer coating on wider trenches gives dishing effect and hence non-planar surface on the trench (d) non-selective RIE process gives non planar surface (e) Dishing effect prevents complete removal of resist by the lines in the stack after nanoimprinting (shown by dotted lines) (f) One possible trench pattern to avoid looping of lines in nanoimprinting
give dish like profile to the stack of silicon nitride and a-silicon as shown in figure B2. If this template is used for nanoimprinting, only the planar surface of the template in contact with resist can completely displace the thermal resist, thus imprinting lines in resist. Dishing effect will prevent the lines in the stack around wider trenches from displacing the thermal resist completely (figure B2 (e)) and these lines will not be imprinted in resist. Hence for avoiding looping of nanowires in nanoimprinting, trench pattern shown in figure B2(f) can be used, where the narrower section of the trench decides the route of imprinted nanowires and the wider section at the ends prevents looping.
APPENDIX C: NANOIMPRINTING

Initial attempts are made to use PEDAL defined molds for nanoimprinting. Nanoimprinting experiments were done using single nanowire molds as well as molds with nanowire arrays. Both these molds were fabricated by PEDAL process as described in Section 4 and Section 5, with average width of silicon nitride lines equal to 23 nm and average spacing equal to 18 nm.

NXR 1020 Resist was spun on 4’ silicon wafer at 3000 rpm for 60 sec. The thickness of the resist film is predicted to be around 170 nm (Figure C1). The resist is soft baked in Nitrogen ambient at 90 C for 2 hours to evaporate most of the solvent in the resist.

![Spin Curve of NXR-1020 Resist (6%)](image)

**Figure C1: NXR 1020 resist thickness dependance on spin speed (source nanonex)**

Nanowire template, approximately 2 inch by 2 inch is used for nanoimprinting purposes,
although in actuality 3 inch wafers can be imprinted using Obducat nanoimprint system. Imprinting is done at 15 bar of pressure at 120°C for 1 minute. The wafers are cooled to room temperature, before removing the molds.

![Figure C2: (a), (b) Nanoimprinting results of isolated lines (c), (d), Nanoimprinting results of array of 16 lines and spaces using Templates fabricated by PEDAL process.](image)

Nanoimprinting is very sensitive not only to the quality of mold but also to the method of nanoimprinting itself. Nanoimprinting of dense feature requires different experimental setting than the isolated features [1]. The same conclusion can also be derived from the
nanoimprinting experiments done in this project. As shown in the figure C2(a) and C2(b), nanoimprinting of isolated lines did produce nanoimprinted lines on the resist, even though dimensions didn’t match the dimensions on the template. This might be due to residual resist layer left on the substrate (which is usually removed by descum step). However, nanoimprinting of array of lines was clearly unsuccessful due to resist distortion upon mold removal. Slight adhesion of the mold was also observed in some of these experiments.

Due of to some success in nanoimprinting we can speculate that with elaborate nanoimprinting experimental analysis we can find the conditions conducive to the successful nanoimprinting of the line-width structures on PEDAL define template. Successful nanoimprinting will be needed for experimenting with novel applications as mentioned in Appendix A and this might be one of the interesting future works of this project.

Reference: