Abstract

Di SPIGNA, NEIL HALEN. Electronic Devices and Interface Strategies for Nanotechnology. (Under the direction of Paul D. Franzon.)

Evaporation of ultra-thin layers of refractory metals onto glass substrates represents a relatively simple method of fabricating discontinuous metal films. The utility of these films in nanotechnology is based on the ability to control their morphology. In this dissertation, control of discontinuous palladium films is demonstrated as the morphology is tailored for various applications. First, the films are successfully engineered to provide molecular scaffolding in the NanoCell. A dependency of the film morphology on the pattern density is observed which potentially could be exploited to provide wafer-scale morphology tuning with only a single evaporation. Next, electrical characterization of gold nanocrystal capacitors showed significant increases in the flat band voltage shift as the gold particle density increased. The density scaling of gold and palladium films was investigated revealing a linear dependence of gold on decreasing evaporation thickness and an exponential dependence for palladium. A palladium particle density of 1.03×10^{12} particles cm^{-2} was achieved, exceeding the theoretical target density for non-volatile memory applications. A novel technique to further increase this particle density is demonstrated.

Another application for discontinuous metal films is for stochastic interface strategies. Interfacing the nanoworld with the microworld represents a critical challenge to fully integrated nanosystems. Unfortunately, not all applications can tolerate random or incomplete connectivity that can result from stochastic solutions. Therefore, a novel structure is presented that permits complete and deterministic cross-connect of orthogonal wiring arrays without the need for any critical translational alignment. Deterministically connecting 10nm wires directly to 3μm wires would require a translational alignment to

within only about 6μm. It is shown that there is no restriction placed on the minimum nanowire pitch and that the design is independent of the technology used to fabricate the nanowires. The process is relatively simple and is presented from a fabrication perspective, critically evaluating the effect of potential processing errors on the design. A proof-of-concept structure is fabricated and analyzed, demonstrating the feasibility of this design.

ELECTRONIC DEVICES AND INTERFACE STRATEGIES FOR NANOTECHNOLOGY

by

NEIL HALEN Di SPIGNA

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Doctor of Philosophy

ELECTRICAL ENGINEERING

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APPROVED BY:

Dedication

This work is dedicated to my parents who have been completely supportive of me. I love you both with all of my heart. Without you, this would not have been possible. Thank you.

Biography

Neil Halen Di Spigna, son of Luigi and Bettyann Di Spigna, was born on October 8, 1977 and raised in Monroe, NY. He graduated high school from John S. Burke Catholic High School in Goshen, NY in 1995. Neil attended college at the State University of New York at Geneseo where he majored in Applied Physics, Computer Science and Mathematics and graduated with a Bachelor of Science in 1999. He attended graduate school at Duke University in Durham, NC where he received his Master of Science in Electrical and Computer Engineering in 2001.

Acknowledgements

I would like to take this opportunity to thank the many people that have contributed to this dissertation and assisted me over the course of my graduate work.

I will start by thanking my advisor Dr. Paul Franzon who gave me the opportunity to pursue this goal. He showed great patience with me when I was trying to find a topic and allowed me tremendous freedom to pursue my interests. He always valued my time which is greatly appreciated. He has treated me with a great deal of respect and his professionalism is inspirational.

I would like to thank Dr. Veena Misra, Dr. John Muth and Dr. Gregory Parsons for their suggestions and comments that have greatly improved this dissertation. Dr. Muth has met with me several times to discuss my work and has made several suggestions that I had not previously thought to explore, particularly concerning characterization. Dr. Misra has also provided a lot of feedback especially concerning applications for my work and has made her lab, equipment and graduate students abundantly available to me. Dr. Misra and Dr. Parsons taught a Nanotechnology class that I thoroughly enjoyed and helped spark my interests in this field. Mostly, all three have given excellent feedback on the direction of this research, which has greatly improved the quality of my work.

Thanks to members of the NCSU Nanofabrication facility, in particular, Dr. Ginger Yu, Joan O'Sullivan, Henry Taylor and Harold Morton. Dr. Yu was instrumental in teaching me about the cleanroom and processing during her IC Fabrication course. She has more specifically helped with much of the fabrication of the fanout structure discussed in Chapter 3 of this dissertation. Joan O'Sullivan also contributed to that processing and has trained me on several of the tools necessary to complete my work. Most notably however, she has been a constant support regarding some personal health issues. Henry Taylor has aggressively assisted me with the E-beam evaporator which my

work in Chapter 4 of this dissertation is so heavily dependent upon. Harold Morton has been a great help to me when I have had problems running tools, particularly in photo. Many thanks for all their help.

Thanks to Dale Batchelor, Rich Fiore and Roberto Garcia of the Analytical Instrumentation Facility here at NCSU. Dale has been a constant source of help concerning my work in scanning electron microscopy, which can be found throughout this dissertation. Everyone at AIF has been abundantly available and willing to assist me. Many thanks.

I would like to thank Protochips, Inc for supplying the support films that enabled the high resolution STEM work found in Chapter 4 of this dissertation. In addition, I would like to thank Materials Analytical Services, Inc for their help in imaging those samples.

I would like to thank members of Paul's research group that have been very supportive. Dr. John Damiano has always been available to help answer questions on processing or suggest ideas on alternate applications for my work. He has been very generous with his time and it is much appreciated. Dr. Stephen Mick has been very helpful concerning how to present my research, how to handle certain graduate school milestones and in proofreading my work. He has greatly improved the quality of several of my presentations as well as my publications. Sriv Gowda of Dr. Misra's group helped tremendously with the CV characterization and interpretation found in Chapter 4 of this dissertation. David Winick, Dr. Steve Lipa and Sachin Sonkusale have also helped me at various times and in various ways over the course of my research.

I would like to thank Dr. David Nackashi for helping me with all of the processing found in this dissertation. In addition, he has provided daily feedback and direction and has taught me a great deal about being a project leader. Much of the work in this

dissertation has its foundation in his work and he has always been available to bounce ideas off of. He has assisted me in too many ways to fully elaborate in this acknowledgement. Mostly however, I have enjoyed his friendship and our numerous talks about college basketball.

I would like to thank Christian Amsinck who I worked very closely with. From our lunch discussion on the daily direction of our work, to his tremendous help at getting me started when I first joined the group. I appreciate him letting me beat him in basketball…every time, and I appreciate his constant friendship which has made my time at NCSU much more enjoyable.

Along these lines, I would like to thank Dr. Christine Kelleher who has been a tremendous inspiration to me. I have enjoyed her friendship, guidance and appreciated her housing me. I would also like to thank Nathan Cefaratti, Eileen Donlon, Lindsay Maguire and Erika Spear, who whether it was through their visits, phone calls, letters or emails, have all made my time in graduate school much more enjoyable. Thank you very much.

I would like to thank Steven, Louis, Michael, Jennifer, and last but not least, Christian Di Spigna. My family has been tremendously supportive of me and I love each and every one of them very much. Finally, I would like to thank Kari Spear for all of her love and support. She was always there for me when I was not feeling well. All is full of love.

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Chapter 1

Introduction

Nanotechnology is the science of manipulating materials at the nanoscale. The ability to fabricate nanoscale electronic devices is essential for the continued development of nanoscience and the miniaturization of integrated circuits. Connecting these materials to the outside world represents a major challenge to fully integrated nano-systems. This dissertation investigates these issues through research on electronic devices and interface strategies for nanotechnology.

A literature review is presented in Chapter 2 appropriately tracing a bottom-up path from the great potential of nanotechnology up through architectures specifically designed for nanotechnology. The paradigm of molecular electronics is investigated and the challenges in the fabrication of characterization structures for molecular-scale devices are discussed. This represents only one of numerous applications for nanofabrication and therefore several nanofabrication techniques are then presented and critically analyzed. Once structures can be fabricated at the nanoscale, they must be interfaced and integrated into nano-systems. Nanoscale interface strategies are reviewed, and the motivation for the demonstration of a determinant fully-connected interface strategy without the need for nano-precision alignment is presented. Finally, the implications of commonly predicted nanotechnology principles, such as self-assembly and the potential for high defect densities, and their impact on architectural design are discussed.

In Chapter 3, a simple approach is presented that permits fully deterministic cross-connect of orthogonal wiring arrays without the need for nanoprecision alignment. The process flow is presented and the equations that govern the novelty of such a design are derived. The conditions that permit deterministic connection of target nanowires with target mircowires are defined. The effects of potential fabrication errors on this design are critically analyzed. An alternate process flow that potentially could be more tolerant to these fabrication errors is described. Finally, the design, fabrication and characterization of a proof-of-concept structure are presented.

Chapter 4 presents research on discontinuous palladium films. The utility of these films is predicated on the ability to control their morphology. This control is demonstrated through the tailoring of the film morphology for applications of molecular scaffolding, sensors, and non-volatile memory. The scaling of discontinuous palladium films is investigated and quantitatively compared to that of gold. Finally, a novel technique to increase the particle density is presented.

Chapter 5 concludes with a review of the major contributions of this dissertation as well as suggestions for the direction of future research.

Chapter 2

Literature Review

The semi-conductor industry has made tremendous progress over the past few decades, as predicted by Gordon Moore as early as 1965. [1] Moore's Law, later generalized to include exponential growth in any area related to the semi-conductor industry, has largely been achieved by most measures. [2] Unfortunately, due to limitations in the current integrated circuit technology, it is believed that new paradigms will have to be developed to continue this trend. One such field under investigation is molecular electronics, in which molecules are used to build electronic devices. Their small size and the vast diversity of molecules that can be synthesized make them an attractive technology. Whether it involves synthesis of complex molecules, modeling current transport, fabricating characterization structures or developing architectural strategies that exploit bottom-up assembly, any new nanotechnology will require a cross-disciplinary effort to continue the scaling of integrated circuits.

Fundamental scaling limitations exist that are independent of materials, devices, circuit or architectural design. From a thermodynamics perspective, in order to prevent unintended state transitions, the energy necessary to generate a binary transition must be significantly greater than the average thermal energy or noise. From a quantum mechanical perspective, the Heisenberg uncertainty principle places a limit on the product of the switching energy and the transition time. From an electromagnetics perspective, a wave traveling down an interconnect can only propagate as fast as the speed of light within the material. [3, 4] These represent fundamental limitations that are largely independent of the technology. However, there are more pragmatic limitations to the scaling of metal-oxide-semiconductor field effect transistors (MOSFETs) that dominate today's integrated circuits.

One scaling limitation to MOSFETs is the leakage through ultra-thin gate oxides, which increases exponentially as the dielectric gets thinner. Another limitation is the scaling of the threshold voltage. Since the subthreshold slope does not scale well,

decreasing the threshold voltage will effectively increase the off state current. In addition, random channel resistances caused by the discreteness of dopants can cause device parameter variability resulting in control problems. Another limitation is scaling the transistor channel length. If the channel length is too short, electrons can tunnel between the source and drain increasing the off state current. [5] One must also consider that optimization of MOSFETs can often be application specific. For example, DRAMs require low leakage for high retention times and thus a high threshold voltage is preferable. A concern in SRAMs is avoiding random dopant fluctuations in order to ensure that the transistor characteristics are similar. Balancing the thickness of the gate dielectric for speed, leakage and robustness is essential for Flash memories. [6] While optimization is often application specific, the cost of today's facilities and lithographic techniques represents a universal economic limitation to continued development. [7]

Although there are serious practical limitations to the scaling of MOSFETs, a comparison to the fundamental limits reveals that there is still tremendous potential for computational power. [3, 8] A famous quote by Richard Feynman in 1959 suggested that "there is plenty of room at the bottom". This has inspired researchers to investigate new paradigms based on bottom-up assembly to continue the trend of modern technology. [4] Some of these areas include single electron transistors, quantum dot cellular automata, carbon nanotube FETs, nanowire FETs, DNA computing, resonant tunneling diodes, and molecular electronics. [6, 9]

Aviram and Ratner first proposed molecular rectifiers back in 1974. [10] Since that time, molecular electronics has seen rapid growth in the advanced synthesis of many diverse molecules. [11] Understanding current transport through molecules is an essential step to engineering molecular devices. Typically Hartree-Fock self-consistent-field (SCF) theory, Green's function techniques (GF), and density functional theory (DFT) have all been used to model current transport. Unfortunately, researchers must be extremely careful in their application of these theories as they may be susceptible to computational anomalies. [12] In addition, their use in verifying actual experimental data is often complicated by the often unknown physical nature of the characterization structure at the

molecular scale. In fact, building reliable characterization structures is one of the fundamental challenges in the field of molecular electronics.

This literature review therefore begins in Section 2.1 by considering some of the current characterization structures and when applicable, the proposed current transport mechanisms. Section 2.2 reviews both conventional and unconventional nanofabrication techniques, as the ability to fabricate nanoscale features is the driving force behind nanoscience and the continued miniaturization of integrated circuits. Interfacing these nanoscale patterns to the microscale world, which has particular significance to the remainder of this dissertation, is covered in Section 2.3. Once a nanoscale interface strategy has been established, incorporating this into an architectural design that exploits the advantages of bottom-up assembly is explored in Section 2.4. Finally, Section 2.5 summarizes and reviews the core challenges to developing a nanotechnology based on molecular electronics.

2.1 Characterization Structures

As previously mentioned, building reliable characterization structures is one of the fundamental challenges in the field of molecular electronics. In this section, several different approaches to this challenge are reviewed.

2.1.1 Crossed-Wire Tunnel Junction

One test structure that has proved quite versatile in molecular electronics research is the crossed-wire tunnel junction shown below.

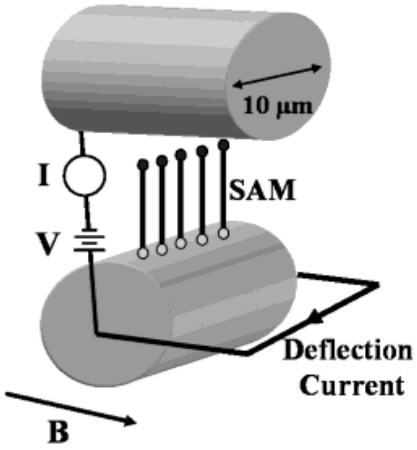


Figure 2.1: Crossed-Wire Tunnel Junction. From [13] "Effect of Bond-Length Alternation in Molecular Wires"

Kushmerick and researchers at the Naval Research Laboratory use two 10μm crossed gold wires with a self-assembled monolayer attached to one of the wires. Their initial separation of ~1mm is reduced using the Lorentz force generated by increasing the deflection current in the wire perpendicular to a magnetic field. [14] This characterization structure enabled them to investigate the role of asymmetric contacts on molecular charge transport. Two types of oligo(phenylene ethynylene) OPE molecules were used in this study: one synthesized symmetrically with thioacetyl functional groups on both ends of the molecule while the other asymmetric molecule had a thioacetyl group only on one end. It was found that the symmetric molecule exhibited a symmetrical I-V response, while the asymmetric molecule showed significant rectification behavior. Using extended Huckel theory (EHT) and Green's function techniques, they showed that their experimental data was in qualitative agreement with theoretical predictions. Thus, the same molecular core can have very different I-V responses depending upon the metal-molecule junctions. [15] In more recent research, they demonstrated the ability to fine tune this rectification by controlling the interaction strength of the asymmetric metal-molecule contact. As the interaction strength increases from a physical bond to a strong chemical bond, the rectification response decreases. [14]

Another application of this structure was testing the dependence of charge transport on bond-length alternation. It had previously been thought that oligo(phenylene vinylene) (OPV) molecules have higher conductance compared to OPE molecules due to their higher level of coplanarity and thus better π-conjugation. However, matching theory with experimental results using the crossed-wire test-bed, Kushmerick *et al.* argued that the higher conductivity is also a function of the smaller bond-length alternation in OPV versus OPE molecules, and cautioned that this must be considered when investigating charge transport. [13]

The crossed-wire tunnel junction has also been used to test conductance scaling. Using the rectifying response of the asymmetric OPE molecules from before; Kushmerick *et al.* measured the I-V response for various deflection currents. It was found that as the deflection current increased, thus expanding the contact area, the magnitude of the response increased. They calculated a scaling factor that when divided out of the data caused it to converge onto a fundamental curve, which they considered to represent the charge transport of a minimum number of molecules, even as few as one. They show that the conductance scales linearly with the number of molecules contacted, and therefore conclude that there is little coupling between the molecules in the monolayer. Thus, each molecule can be treated individually and one can expect linear superposition of conductance in π-conjugated systems. [16] Further supporting this experiment, they tested symmetric OPE and OPV molecules in both the crossed-wire tunnel junction and using scanning tunneling microscopy (STM). One major difference between these methods is the contact area. The STM is likely to contact as few as one molecule while the crossed-wire tunneling junction was thought to be contacting about 10^3 molecules. It turns out that multiplying the STM results by a factor of 10^3 resulted in good agreement with the crossed-wire results, for both OPE and OPV molecules. Thus, a direct comparison for multiple molecules in separate test-beds resulted in the same conclusions: that each molecule can be considered discretely and that transport did not significantly involve intermolecular hopping. [17, 18]

While this test structure has demonstrated great versatility, it is difficult to conceive how it can be integrated into devices. Relatively large contact areas and the inability to know exactly how many molecules are being contacted are additional limitations of this structure. As discussed, the use of STM as the top probe minimizes the contact area to near atomic precision.

2.1.2 Scanning Probe Microscopy

The strength of scanning probe microscopy in characterization is its ability to measure very small numbers of molecules, including the potential of measuring a single molecule. In essence, it has the potential to act as a base-case experiment for other test-beds, just as Kushmerick and Blum used it to test their crossed-wire tunnel junction structure. Unfortunately, understanding current transport using scanning probe microscopy has been challenging. [19] Generally, researchers have utilized either scanning tunneling microscopy (STM) or conductive probe atomic force microscopy (AFM). Both techniques involve molecular self-assembly on top of a conductive surface, commonly gold. In scanning tunneling microscopy, the tip remains separated from the molecules by keeping the tunneling current constant. Thus, one is actually measuring the resistance of the tunneling gap in series with the molecule. Unfortunately this results in measurements that couple the electronic conductivity of the molecules with their physical nature. [20] In atomic force microscopy, a controlled load is used to place the conductive tip in contact with the target measurement. While these results are typically easier to analyze, one has to consider the stress on the film caused by the applied load. In general, both approaches have been used successfully to investigate molecular devices.

In fact, researchers at Arizona State University have utilized both methods in trying to understand current transport using SPM techniques. In particular, their experiments were focused on molecules chemically bonded to a metallic conductor on both sides. They used AFM to measure 1,8-octanedithiol molecules inserted into an octanethiol monolayer, in which the dithiols were capped with gold nanoparticles. Their measurements showed a series of increasing IV curves, which they argued represented an increasing number of measured molecules. When the current was divided by a fitted

integer divisor, the data collapsed onto a single fundamental curve, which they considered to be the characteristic of a single molecule. One important aspect to note was that the fundamental curve was not strongly dependent on the applied load of the tip, in direct contrast with previous non-bonded top contact results. Therefore, they stress the importance of chemically bonding the top contact and claim that the non-bonded contact will dominate the electrical responses, resulting in irreproducible and unreliable data. [21] These results were further supported in a later experiment that involved investigation of the exponential decay factor associated with decanedithiol, dodecanedithiol, and the previous octanedithiol molecules. [22]

Weiss *et al.* have used STM to investigate switching phenomena in OPE molecules inserted into a dodecanethiolate monolayer. In previous experiments, they have argued that the molecules insert at structural domain boundaries and substrate step edges, that individual molecules can be distinguished, and that they are more conductive than the surrounding monolayer. [23] The switching phenomenon, as shown in Figure 2.2, is suggested to be a result of conformational changes of the molecules.

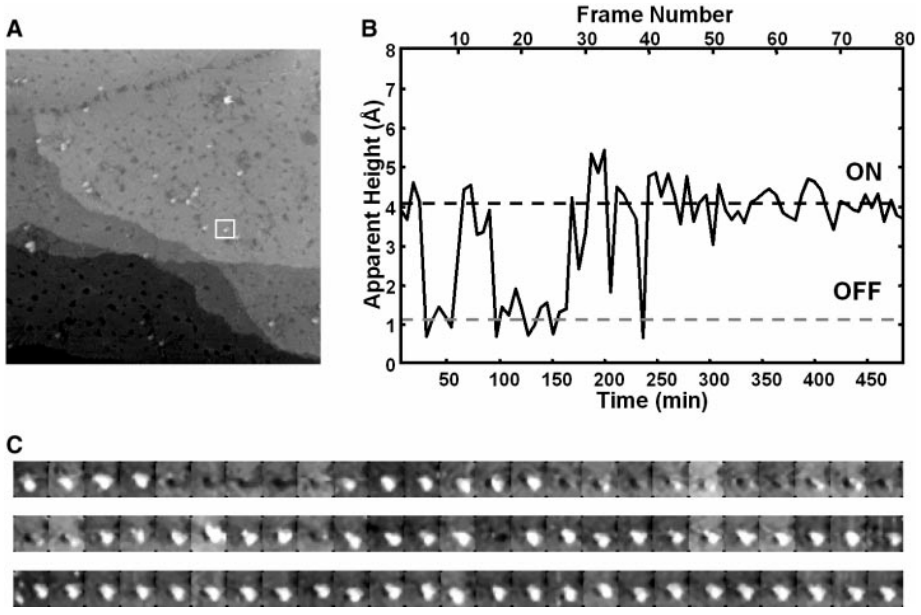


Figure 2.2: Switching Phenomena Observed using STM. From [24] "Conductance Switching in Single Molecules Through Conformational Changes"

In this figure, the time elapsed ‘blinking’ is evidence of switching in the bi-stable OPE molecules. Investigating this switching, they tested its dependence on the quality and defect density of the host SAM. They produced a SAM with reduced quality by decreasing the allotted attachment period, while producing a SAM with improved quality by annealing it in the presence of a dodecanethiol vapor. They concluded that when the host SAM allowed for greater movement, they witnessed an increased percentage and speed at which the molecules switched, thus concluding that conformational change was the cause of the switching. [24] However, there has been other research that suggests that the switching in SPM measurements is a result of the bottom Au-S bond breaking and reattaching. This argument is based on STM measurements on molecules in which ring rotations are not possible and yet switching is still observed. [25]

Other key research using SPM includes Gittins work on characterizing electronic switching in redox-active molecules. [26] Wold and Frisbie demonstrate continued characterization of metal-molecule-metal tunnel junctions using AFM to vary the load on varying chain lengths of alkanethiols on gold. [27, 28] In a rather atypical use of AFM, Williams *et al.* use the probe tip to act as a mechanical force applicator rather than a second electrode, in hopes of characterizing observed switching in a functionalized crossbar structure. They conclude that their switching is a result of metal filament formation and dissolution. [19] Simplicity, versatility and the ability to test small numbers of molecules make SPM techniques attractive; while limitation to only two electrodes, often asymmetric, and data interpretation represent its potential drawbacks.

2.1.3 Mechanically Controllable Break Junction

The mechanically controllable break junction (MCB) is another characterization structure with the potential to measure small numbers of molecules. A metal wire, typically thinned, is mounted on a flexible substrate in the presence of a molecular solution and is bent until the wire breaks. The molecularly functionalized wires are then slowly brought back into contact. This process can be visualized in Figure 2.3.

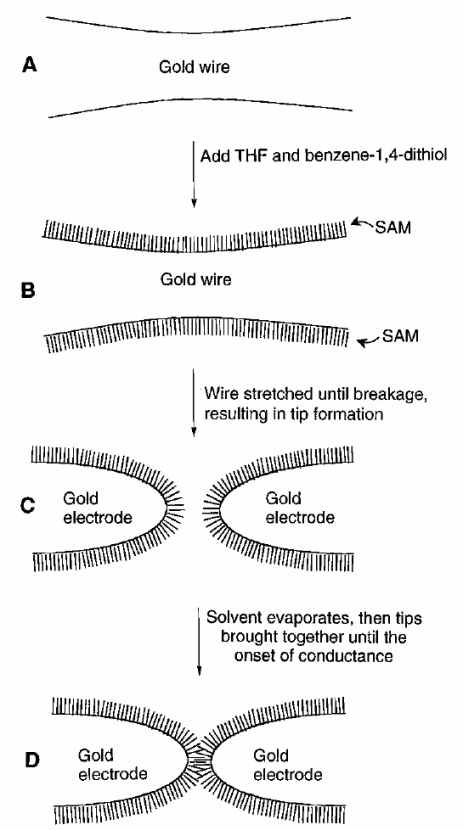


Figure 2.3: Mechanically Controllable Break Junction. From [29] "Conductance of a Molecular Junction"

Reed *et al.* used benzene-1,4-dithiol on gold electrodes spaced about 80Å apart, and based on their IV measurements that appear indicative of a Coulomb staircase, they concluded that it is possible that they are measuring the conductance through a single molecule. [29] These same IV trends are also observed by Reichert *et al.* who used the MCB to test symmetric and asymmetric versions of a molecule consisting of a rigid rod-like central axis. The asymmetric molecules resulted in asymmetric IV responses. Oftentimes, the asymmetry in the curve took on its 'mirrored' image, strongly suggesting that small numbers of molecules were being measured; otherwise one might expect an averaging out of this characteristic. Only symmetric molecules resulted in symmetric IV responses, however, manipulating the contacts had a strong influence on the overall

characteristic, leading them to believe that the atomistic nature of the contacts has a significant influence on the measured response. [30, 31] Kergueris *et al.* presents further evidence that the step-like nature of the IV responses indicates the measurement of only a few molecules. In addition, they also notice a dependence on the IV curves to slight mechanical perturbations in the contacts, a sentiment echoed by Reichert. In particular, they witnessed the existence of many stable states as the gap distance was altered, further showing the dependence of the IV response on the molecule-metal contact. [32] Clearly the uncertainty of the geometry of the molecule-metal contact is one potential drawback of this technique, while symmetric electrodes and the ability to measure small numbers of molecules are its main advantages.

2.1.4 Electrochemical Narrowing

Another method to achieve nanoscale separations is to use electrochemical deposition to narrow the gap between two metallic electrodes. Morpurgo *et al.* defined two gold leads by electron beam lithography with an initial spacing of 50 – 400nm. Gold was then electrochemically deposited on the leads while an *in situ* resistance measurement end-pointed the deposition. The process was reversible if the electrodes were unintentionally shorted by electrochemically dissolving the gap. In this fashion they were able to fabricate electrode separations on the 1 nm scale. [33] Recent experiments suggest that platinum is more robust than gold and can be deposited with a finer grain size. Additionally, they demonstrated greater control of the process and showed how it can be extended for larger gaps if so desired. [34] Others extended this process to copper and cobalt as well as demonstrating asymmetric electrodes composed of different metals. Changes to the experimental setup allowed for self-limiting electrochemical deposition, in which once a gap shorts it is automatically dissolved. This process is continuous, allowing for multiple nanoscale gaps to be fabricated in parallel. [35] As shown in Figure 2.4, Kashimura *et al.* has extended this technique to a three-terminal junction, which has represented a major fabrication challenge in nanotechnology. [36]

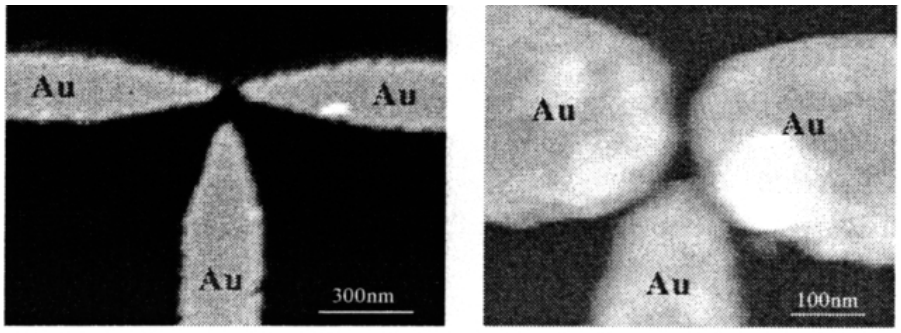


Figure 2.4: Three-Terminal Junction formed by Electrochemical Deposition. From [36] "Fabrication of Nano-Gap Electrodes Using Electroplating Technique"

Tao *et al.* showed how the current increases in a stepwise fashion while depositing copper. They found that each discrete step represented a gap decrease of about 0.5Å. Since this distance is smaller than the size of a copper atom, they concluded that the nature of growth as the copper was deposited was based on structural relaxations and energetically favorable reconfigurations, resulting in stable nano-gaps with sub-angstrom precision. [37] Finally, this technique has been directly applied to molecular characterization. Park *et al.* formed self-assembled monolayers of 1,4-benzenedimethanethiol (BDMT) on two electron beam lithographically defined platinum leads separated by about 100nm. Platinum was electrochemically deposited onto one lead until a current response was measured. Typically three different types of responses were measured, only one of which they believed to actually represent current transport through the BDMT SAMs. Unfortunately only five out of the thirty trials resulted in a molecular response. [38] However, electrochemical deposition represents a simple, easily controllable, and robust process to achieve nanoscale separated metallic electrodes with various metals. Unknown tip geometry and the discrete nature of growing the leads can complicate current transport measurements and modeling.

2.1.5 Dielectrophoresis

Electrochemical deposition reduces the distance between two electrodes, eliminating the need to fabricate gaps at the nanoscale. Similarly, dielectrophoretically

trapping a conductive particle between two electrodes accomplishes the same goal. Dielectrophoresis involves the movement of polarizable particles in an AC electromagnetic field. It allows for the investigation of single particles at the micron and submicron scale. In only a single step a particle can be moved to an area and then immobilized. Negative dielectrophoresis can be a contact-less technique in which the particles are immobilized in a field minimum, not in contact with any electrode or surface. [39] In addition, it works with just about any material, being limited only by differential polarizability of the particle with respect to the medium, making it a very versatile laboratory technique. Amlani *et al.* measured the IV characteristics of two layers of molecules by coating two proximal probes with a SAM and then dielectrophoretically trapping a conductive colloid in between, as shown in Figure 2.5. Using a molecule that had previously exhibited negative differential resistance (NDR), their measurements resulted in the presence of two NDR peaks, as one might expect with two of these molecules in series. [40]

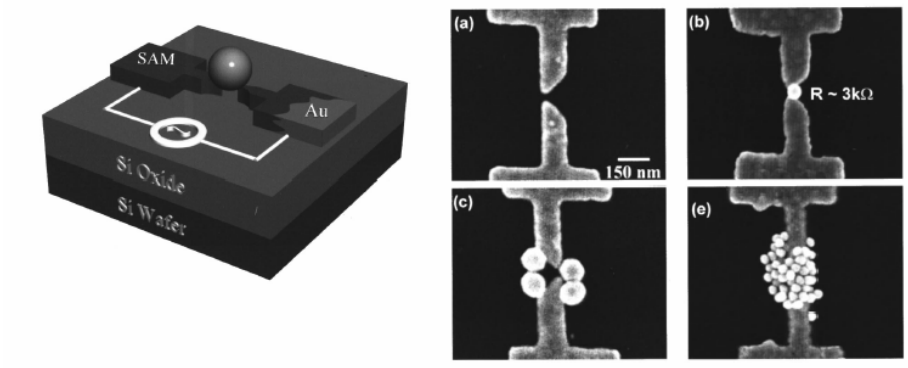


Figure 2.5: Gold Nanoparticle Bridging NanoGap with SAM. From [40] "An approach to transport measurements of electronic molecules"

Khondaker *et al.* used dielectrophoresis to bridge electrodes initially separated by as much as 1μm. Using current-induced electromigration, they created a small gap between the dielectrophoretically trapped particles. They subsequently trapped 3nm thiol coated gold nano-particles in this gap and measured the current-voltage response. [41, 42]

Unfortunately, controlling and end-pointing dielectrophoresis can be challenging since there are many experimental parameters that require optimization. Solution flow caused by heating or evaporation can create unpredictable turbulence in the solution, acting to destabilize trapped particles or even prevent trapping completely. In the particular case of trapping conductive particles, large currents can flow once the particles electrically short two electrodes. These currents can actually cause electromigration and strong localized heating. Ambiguity in the number of contacts and molecules being characterized is another potential drawback of this technique.

2.1.6 Top Contact Evaporation

One of the more challenging aspects of characterization structures is fabrication of the second contact. Reed's nanopore structure is characteristic of an approach in which the second contact is evaporated on top of the molecules, as illustrated in Figure 2.6.

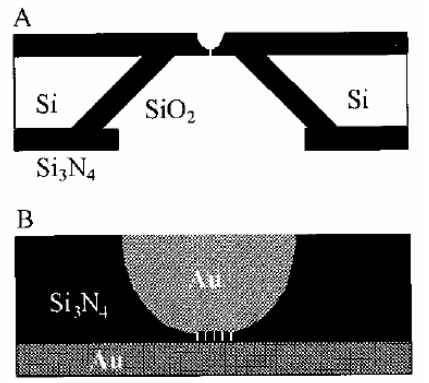


Figure 2.6: Cross-section of the Nanopore. From [43] "Large On-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device"

Fabrication of the nanopore starts with a low-pressure chemical vapor deposition (LPCVD) of a Si_3N_4 film on a silicon wafer. A 400 micron square is opened up in the nitride and the exposed silicon is anisotropically etched, resulting in a suspended nitride membrane on the opposite side of the wafer. The nanopore is fabricated in this membrane through electron beam lithography and reactive ion etching (RIE). Gold is

evaporated into the nanopore, molecules are assembled, and then gold is evaporated on the opposite side to form the top contact. [43] One of the major issues facing top contact evaporations involves preventing damage to the underlying molecules. To ensure this, the evaporations were performed under low temperatures and with very low evaporation rates. These methods were aimed at reducing the kinetic energy of the evaporating material when it contacted the SAM. Additionally, the active area was kept smaller than the domain size of the SAM in hopes of having a highly ordered defect free monolayer. [44]

This structure was used to measure the current transport through an OPE molecule containing a nitroamine redox center. The result was an IV characteristic which showed negative differential resistance (NDR) with a peak-to-valley ratio of about 1030:1, as illustrated in Figure 2.7. [43] Rawlett *et al.* performed conducting probe AFM measurements on similar molecules that resulted in good qualitative agreement with Reed's data. Since the AFM is potentially measuring only a single molecule, this would imply that the NDR was intrinsic to the molecules and rules out any intermolecular phenomena. [45]

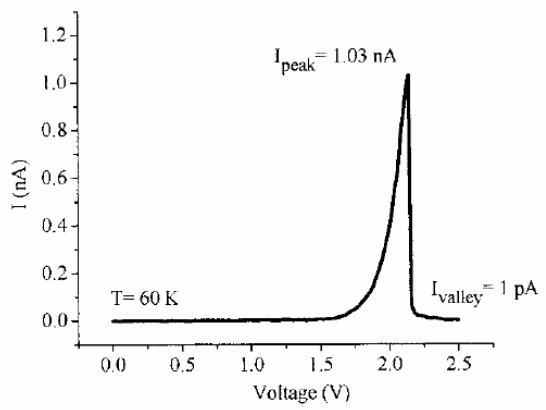


Figure 2.7: Negative Differential Resistance. From [43] "Large On-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device"

Reed *et al.* proposed that the origin of the NDR was due to a reversible electrochemical redox reaction. As the voltage increases, the molecule undergoes an electron reduction allowing current to flow. As the voltage increases even further, an additional reduction occurs, which effectively blocks the current path. [43] This theory is further supported by cyclic voltammetry measurements, in which the conduction peak falls between two electron reduction potentials. [46] Recently, researchers from Northwestern University suggested that hysteretic, switching, and NDR effects in molecular systems containing redox centers could be the result of polaron formation on the molecule, rather than a charging mechanism or conformal changes. [47]

Another area investigated with the nanopore is current transport through alkanethiols. It has largely been reported that the transport mechanism through these molecules is tunneling. However, this cannot be confirmed without temperature dependence measurements, since tunneling is not dependent upon the temperature, while hopping conductance and thermionic emission are. Thus, Reed *et al.* measured the current through octanethiols, dodecanethiols, and hexadecanethiols varying the temperature to as low as 80K. Based on their measurements, which showed little to no dependence on the temperature, they were able to confirm that the transport mechanism is indeed tunneling. [48, 49]

Unfortunately, there are still some issues facing top contact evaporations. In particular, questions still exist on the condition of the SAM after evaporation, as expressed by other researchers who have also performed top contact evaporations. [50] There exists the possibility that the evaporating metal will punch through the SAM. Another major concern is the asymmetry of the contacts, which is a reoccurring theme in molecular electronics. In this structure, the bottom contact is chemisorbed while the top contact is physisorbed. It has already been shown how sensitive current transport measurements are to the contacts.

2.1.7 Mercury Drop Top Contact

Clearly the top contact is an issue in molecular characterization structures. One rather simple structure employs mercury as the top contact. In experiments by Whitesides *et al.*, a liquid mercury drop functionalized with an alkanethiol SAM is dropped on top of a silver film also functionalized with a SAM. The top Hg/SAM electrode conforms to the bottom SAM/Ag electrode, minimizing any mechanical damage, surface roughness or shorting issues that can occur with top contact evaporations for example. Based on their measurements they conclude that the transport mechanism through the bi-layer SAM is superexchange tunneling. Some of the disadvantages of this structure include its relatively large contact area, limited temperature range flexibility, and difficulty integrating it into a large scale device. [51, 52, 53]

While there is a nice diversity of characterization structures to select from, each of them has their own advantages and limitations. Some involve a large contact area, while others measure very few molecules but are difficult to interpret or have responses that are dependent upon the tip geometry. Some are inherently non-integratable or have limited application, while others potentially result in damage to the underlying SAM. In addition, it is believed that the formation of metallic filaments through electromigration may be complicating the interpretation of the some of the results. Thus, there is no single characterization structure that has become the standard for screening molecules. On the other hand, it is promising that researchers have tested similar molecules in different structures and found good qualitative agreement between the results. Coupling this with careful application of modeling transport theory leads to optimism in our future understanding of electrical transport through molecules.

2.2 Nanofabrication Techniques

Characterization structures are engineered to measure the current response and charge transport mechanisms through molecules. They represent a specific application of nanofabrication. However, there are many other applications for nanoscale devices

including bio-sensors, nanoelectromechanical systems (NEMS), optoelectronic devices and many others. [54] Nanofabrication is not only essential to the development of nanoscience, but also to the continued miniaturization of integrated circuits. It is with this motivation that numerous methods to pattern at the nanoscale have been developed, as summarized in Figure 2.8.

pattern formation using[a]	basis for intrinsic limitations	strategies to circumvent the limitations
photons		
UV, DUV, EUV, and X-rays	diffraction	contact mode, near-field exposure
	depth of focus	nonlinear photoresists
particles		
electrons and ions	electrostatic interactions	neutral atoms
	writing is serial	projection
	small field of writing	arrays of sources
neutral atoms	de Broglie wavelength	
machining		
AFM, STM, NSOM, and electrochemical	writing is serial	arrays of probes
	small field of writing	
physical contact	van der Waals forces	
printing, molding, and embossing	speed of capillary filling	low-viscosity solutions
	adhesion of mold and replica	surface modification
self-assembly	control over order, domain size, and density of defects	
surfactant systems		
block copolymers		
crystallization of proteins and colloids		
deposition	low flexibility in patterning and fabrication of masks or templates	
cleaved edge overgrowth		
shadowed evaporation		
size reduction		
glass drawing	low flexibility in patterning; reproducibility	
compression of elastomeric masters or molds		
controlled reactive spreading		
edge-based technologies		
near-field phase-shifting photolithography	diffraction	
topographically directed photolithography	diffraction	
topographically directed etching		

[a] Abbreviations: UV (ultraviolet), DUV (deep ultraviolet), EUV (extreme ultraviolet); AFM (atomic force microscope); STM (scanning tunneling microscope); and NSOM (near-field scanning optical microscope).

Figure 2.8: Methods of Nanofabrication. From [54] “Unconventional Methods for Fabricating and Patterning Nanostructures”

Photolithography has been the dominant pattern-transfer technology in integrated circuit fabrication for many years. Patterning is achieved when photons pass through transparent features on a mask and chemically alter photo-sensitive resists. Contact lithography involves placing the mask in contact with the substrate, while projection lithography uses lenses in between the mask and substrate to demagnify the pattern. Since

contact lithography is a 1x technique, implying only one-to-one feature size pattern transfer, its potential for nanofabrication is limited. However, the resolution of contact lithography can be extended below the wavelength of the incident light by using evanescent waves, referred to as near-field lithography. Due to their exponential decay, these waves mandate very close proximity between the mask and the resist, and therefore cannot be used in patterning with projection lithography. Unfortunately, contamination, bowing or warping of rigid masks, and resist profiles can lead to non-uniform gaps between the surface and the mask. In addition, features on the substrate can be damaged as the mask is brought into contact. This physical contact can also result in a slight shift in the mask which can make accurate nanoscale alignment practically impossible. [54] All of these issues can make accurate wafer-scale nanofabrication using contact lithography very difficult. Approaches that address some of these issues include the use of a near-field scanning optical microscope (NSOM), or alternatively using 'soft' conformal masks. [55, 56]

The use of lenses in projection lithography demagnifies the features on the mask making nanoscale fabrication more practical and mask fabrication more economical. However, the resolution is limited by Rayleigh diffraction which is proportional to the wavelength of the incident light divided by the numerical aperture of the lens system. Typically ultraviolet light is used; however, smaller structures have required smaller wavelengths. From ultraviolet to deep ultraviolet (DUV) to extreme ultraviolet (EUV) to x-rays, reduction of the wavelength has been one method used by researchers to offset the limitations of Rayleigh diffraction. Unfortunately, new high resolution photoresists must be developed and the optics for focusing shorter wavelengths becomes increasingly more complex and expensive, requiring new materials for lenses and masks, as they must be transparent to smaller wavelengths. Alternatively, one can improve the resolution by increasing the numerical aperture. However, the depth of focus is another critical parameter in photolithography and is proportional to the wavelength of the incident light divided by the square of the numerical aperture. Thus, while increasing the numerical aperture can improve the resolution, it dramatically reduces the depth of focus. [54] Use

of very thin resists is one method to help mitigate a reduced depth of focus. Since reducing the wavelength requires the use of new and costly materials, and increasing the numerical aperture adversely affects the depth of focus, researchers have also attempted to optimize the proportionality constants. Generally, these constants are a function of many parameters, including the processing, resists, masks, and lenses of the system. Combined with the use of shorter wavelengths with novel schemes such as off-axis illumination, immersion lenses, optical proximity correction, chemically amplified photoresists, or top surface image techniques; photolithography has been used to pattern features less than 50nm. [57]

The trend of wavelength reduction continues with the use of electrons and ions to pattern nanoscale features. In fact, electron beam lithography (EBL) has been used to successfully pattern sub-10nm features. [58] The resolution of this typically mask-less technique is dependent upon the initial spot size, the interaction of the electron beam in the resist, and any backscattered electrons from the substrate. Interaction of the beam with the resist can take the form of elastic and inelastic scattering events. Elastic scattering broadens the beam by altering the trajectories of the incoming electrons. Inelastic scattering can result in the production of secondary electrons at lower energy levels which can expand the interaction volume. The use of low energy beams combined with thin optimized resists and thin substrates can theoretically reduce this interaction volume. Alternatively, increasing the accelerating voltage, and thus the energy of the incoming electron beam, will reduce the spot size of the beam, minimizing the potential feature size. [59]

Focused ion beam lithography (FIB) is analogous to electron beam lithography. One difference is that ions lose their energy much faster than electrons resulting in a smaller interaction volume in the resist and thus the potential for improved resolution. Unfortunately, ions are heavier particles and can cause damage to the underlying substrate. In addition, the current density is significantly less than in electron beam lithography resulting in longer scanning times. [60] In general, throughput is the major obstacle to scanning beam lithography. EBL and FIB are both serial techniques and so

using them for mass production is impractical. There has been research dedicated to electron and ion projection lithography as well as the use of multiple sources that could enable parallel pattern transfer. [61, 62, 63] While each of these methods has its own challenges, the goal of each is to increase the throughput of scanning beam lithography which is essential if this technology to be used for mass production.

Even further reduction in the ultimate theoretical resolution to almost atomic level precision can be achieved using scanning probe lithography (SPL). While there are numerous techniques utilizing scanning probes to pattern nanoscale features, including the aforementioned NSOM, they generally involve deposition of some 'ink' onto a substrate or locally modifying the resist or surface. An example of the former would include dip-pen nanolithography (DPN), in which an AFM tip is coated with molecules or other 'inks'. As the tip is scanned across the substrate, the 'ink' will transfer from the tip to the surface, resulting in pattern formation as small as 15nm. [64] Understanding how the 'ink' transfers to the substrate is critical to optimizing the resolution of this technique, which is dependent upon the transfer and spreading of the ink as well as the physical geometry of the scanning tip. [65]

Other examples of SPL include using the probes to remove or displace material, to locally expose resist, create indent profiles or cause selective oxidation. [59] The main drawback to these techniques is that they are inherently serial and thus not scalable. One way to increase the throughput is to use multiple probes. [66, 67, 68] However this can greatly increase the complexity and cost of the system.

Another group of techniques uses topographic edges to pattern nanoscale features, commonly referred to as edge-based lithography. One example of this technology is the superlattice nanowire pattern transfer (SNAP) technique developed by Heath ***et al.*** In this process, AlGaAs layers are selectively etched from a GaAs/AlGaAs supperlattice on the edge of a substrate. An angular metal evaporation is the performed, followed by the transfer of this metal onto a silicon substrate. This technique can produce well defined nanoscale metallic wires at a sub-20nm pitch. [69] Other edge-based technologies include the previously mentioned near-field phase-shifting photolithography, topographically

directed photolithography, and a controlled undercutting technique. [70] In the latter process, photolithography is performed on top of a metal layer which is then isotropically wet etched, undercutting the resist. A second metal deposition is performed, followed by a liftoff step leaving behind 50nm features where the resist was undercut. While this represents a very simply method to achieve nanometer scale features, the overall pitch is still limited by the resolution of the original photolithography. [71] These are just samples of the many different types of edge-based lithography; however, in general, one is limited in the types of patterns that can be fabricated using these methods.

Thus far most of the techniques have represented top-down approaches. In contrast, using chemical self-assembly or directed assembly may lead to systems built from the bottom up that are potentially cost efficient, highly versatile, have molecular-scale resolution, can reject defects and can self-repair, but tend to be limited to regular or random structures. How this may affect architectural design is a critical issue that will be addressed later in this chapter. In general, self-assembly has tremendous potential and may represent the future of nanofabrication.

Unfortunately, each of the nanofabrication techniques above has its own set of challenges. Whether it is the cost of the technique, its serial nature, or the limited types of patterns that can be produced, one must consider the application when choosing a nanofabrication strategy. For example, while electron beam lithography may not be suitable for mass production, it is excellent for fabricating nanoscale masks or stamps that can be used in Imprint Lithography. Imprint Lithography represents an alternative nanofabrication approach that is potentially cost efficient, has high-throughput, and can fabricate arbitrary patterns.

There are three general types of Imprint Lithography, as shown in Figure 2.9.

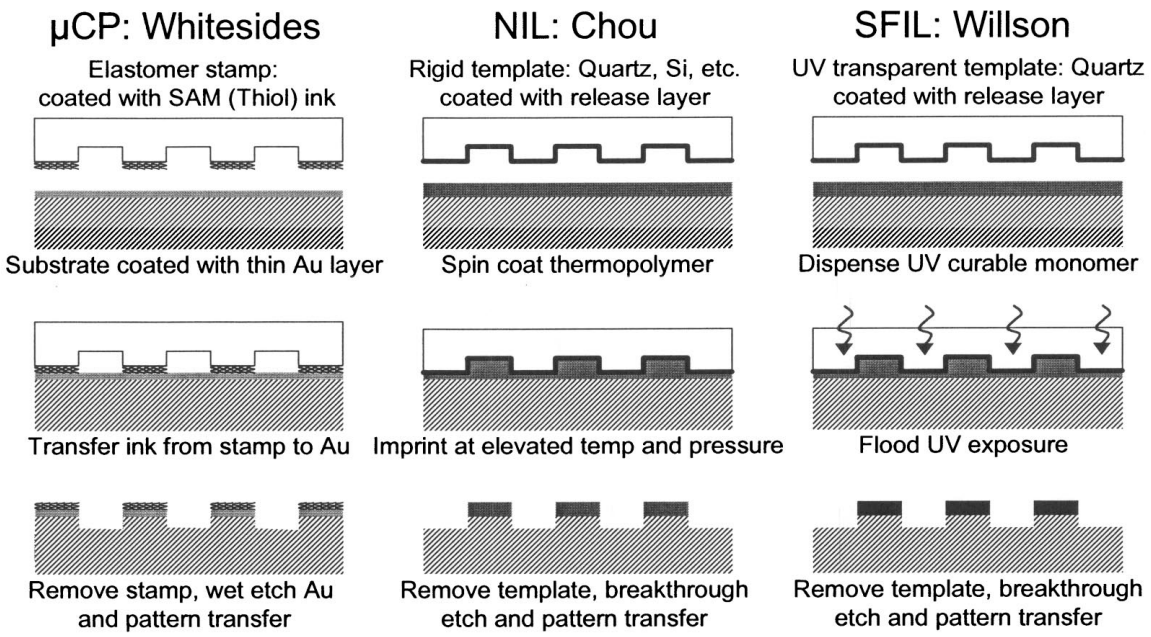


Figure 2.9: Types of Imprint Lithography. From [59] "Nanofabrication"

Soft lithography involves the use of flexible elastomeric stamps, such as poly(dimethylsiloxane) (PDMS) elastomers, which allow for conformal contact with surfaces. An example of soft lithography is micro-contact printing, which involves the transfer of some form of chemical 'ink', a self-assembled monolayer of hexadecanethiols for example, onto a target surface. Success can depend on how quickly and highly organized the 'ink' transfers to the surface. Any propensity of the 'ink' to spread out post-assembly will result in feature distortions. One unique advantage of this technique is that it allows tremendous flexibility and control over the chemical nature of the target surfaces. Other types of soft lithography include replica molding, microtransfer molding, and nanotransfer printing. [72] An example of the latter involves the assembly of a glue-like SAM onto a target surface. A stamp covered with a gold "release" layer is then brought into contact with the covalent "glue", resulting in pattern transfer. [73]

Photocurable nanoimprint lithography (P-NIL), or step and flash imprint lithography (S-FIL), typically involves the use of UV-transparent stamps that are pressed into a photo-curable polymer. The polymer is then irradiated until curing is complete. The

stamp is removed, and the resulting pattern can be anisotropically etched into the substrate to complete the pattern transfer. One of the unique advantages of this method is the use of a transparent stamp, which enables standard mask alignment techniques. In addition, curing can be performed at room temperature which relaxes the constraints on temperature sensitive materials as well as potentially improving throughput. [74, 75] This technique has been used to fabricate lines on the order of 5nm. [76]

The final type of Imprint Lithography is Nanoimprint Lithograhpy (NIL) or Hot-Embossing lithography. In this method, the target substrate is coated with a thermoplastic polymer. The polymer is heated above its glass transition temperature, T_g, such that it becomes a viscous fluid. The stamp is pressed into the free flowing polymer and then the system is allowed to cool. The polymer sets, the stamp is removed, and the resulting pattern can be transferred into the substrate through an anisotropic etch. [77] In this fashion, features below 10nm have been successfully fabricated. [78]

Although these are very encouraging results, there are still some significant challenges facing Imprint Lithography. [79, 80] One of these challenges is aligning multiple layers. Except for photocurable imprint lithography, stamps are typically opaque, and thus require non-traditional alignment schemes. The alignment can be further complicated by thermal expansion and mechanical instability. Minimizing thermal coefficient differences between the mask and stamp, or using polymers that can be imprinted at lower temperatures can help reduce the thermal effect. Mechanical instability can result if the substrate and stamp are not exactly parallel to each other, or if there is any non-uniform pressure distribution. Optimization of the printer design can help reduce this instability. [81]

Sticking between the stamp and substrate poses another challenge to Imprint Lithography. As the size of the printed features decreases, the overall surface area increases. This leads to an increase in the van-der-Waals attraction between the stamp and substrate and thus increases the potential for sticking. Optimizing the stamping conditions, using custom-made polymers, and using anti-adhesion layers can all help to reduce sticking. Unfortunately, anti-adhesion layers can represent a significant fraction of

the critical dimension of nanometer sized features, and can distort the pattern dimensions. Thus, using monomolecular anti-adhesion layers is essential for very small features. [82, 83]

Polymer material transport is another critical issue that can affect print quality. [84] This can depend on the molecular weight of the polymer, as well as the magnitude and rate of the applied pressure and temperature. [80] Stamp design, pattern density and relief patterns all need to be considered when optimizing the stamping conditions. Balancing positive and negative features in localized areas on a stamp is critical for patterning nanoscale features. [85]

Stamp lifetime is another critical issue due to the high cost of fabricating the original master. Unlike projection mode photolithography where demagnification can allow for mask fabrication at dimensions greater than the fabricated critical dimension, imprint lithography is a 1x technique, so the patterned structures are the same dimensions as those on the mask. Thus, replacement masks using the aforementioned nanofabrication techniques, typically electron beam lithography, will be relatively expensive. Therefore, new methods of nanoscale pattern fabrication are under development. [86] There is much interest in finding alternate methods of nanoscale feature and imprint lithography stamp fabrication.

One distinct advantage of Imprint Lithography is the ability to fabricate three dimensional patterns. Although other methods exist, they are not easily accomplished with photolithography, scanning beam lithography, scanning probe lithography, and many edge-based lithography techniques. Using a three dimensional mask, Chou was able to fabricate T-gate structures with 40nm bases. [87] Scanning beam lithography is used for the fabrication of three dimensional stamps, and can be extended to multiple step levels. [88, 89] Along with the potentially high throughput, relatively low cost and the ability to fabricate arbitrary patterns, including 3D patterns, Imprint Lithography represents a nice alternative to conventional nanoscale fabrication.

While both conventional and unconventional nanofabrication approaches have been demonstrated, each possesses its own distinct advantages and limitations.

Depending on the application and possibly even more importantly, resources, different approaches may be better suited. In conclusion, Figure 2.10 summarizes many of the nanofabrication approaches and their corresponding physical dimensions.

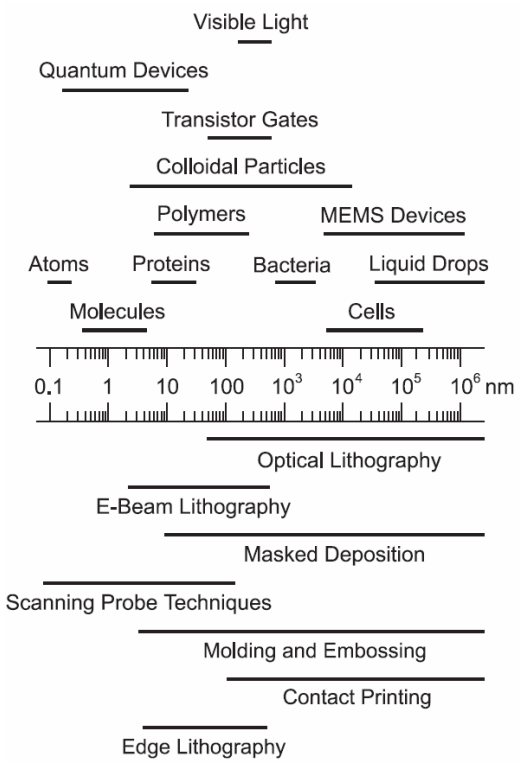


Figure 2.10: Scales and Nanolithography Techniques. From [70] "Patterning: Principles and Some New Developments"

2.3 Interfacing the Nano-World

Now that nanoscale wires and devices can be fabricated, it is necessary to consider how to connect these nano-features to the micro-world. Addressing this interface represents the next major obstacle to testing, nano-computing, and fully integrated nano-systems. [69, 90, 91, 92] Successful interface strategies require both physical connection to the nano-world, as well as retention of the nanoscale pitch. The latter implies decoding, so that several nanowires are addressed by one or fewer microwires. In addition,

minimizing the frequency at which the micro-world is interfaced is another method to help maintain the functional density of the nanoscale. Generally, solutions to interfacing have required nano-precision alignment or stochastic assembly resulting in random or even incomplete connectivity.

Researchers at Harvard University have demonstrated an approach based on chemically modified cross-points in a nanowire-FET crossbar architecture to achieve decoded nanowire addressing. Target cross-points were lithographically opened and treated with a solution of tetraethylammonium chloride, lowering the threshold voltage of the NW-FET. This enabled signal transfer between nanowires and target output wires, while non-target cross-points remained isolated. A ‘decoding pattern’ is built into the crossbar by targeting certain junctions for chemical modification. [90]

Ziegler and Stan have proposed a crossbar architecture in which nanowires and microwires are separately etched through the use of a two-step masking process as shown in Figure 2.11. [93]

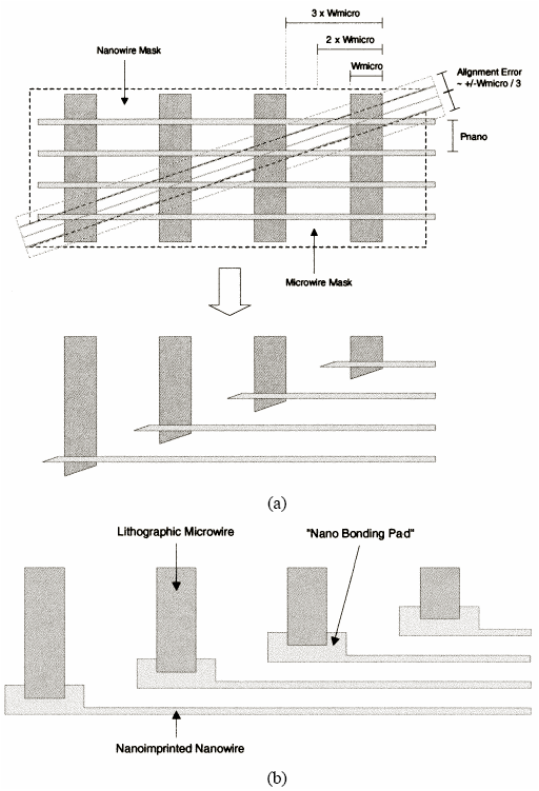


Figure 2.11: Complementary Masking and Etching of Cross-Wires. From [93] "CMOS/Nano Co-Design for Crossbar-Based Molecular Electronic Systems"

Obviously from a materials perspective, this assumes that the two sets of cross-wires can be etched selectively with respect to each other. Then, instead of aligning nanowires, this structure requires only mask alignment. If the geometry of the nanowires can be tailored, they propose the use of "nano bonding pads" to further reduce the necessary alignment precision. Decoding is programmed into the nanowire crossbar array through the use of diode-resistor logic. [94] Advantages of this strategy include simplicity, deterministic addressing and the potential for fault tolerance.

DeHon has proposed the use of nanoscale vias combined with customizable nano-via decoding patterns as shown in Figure 2.12.

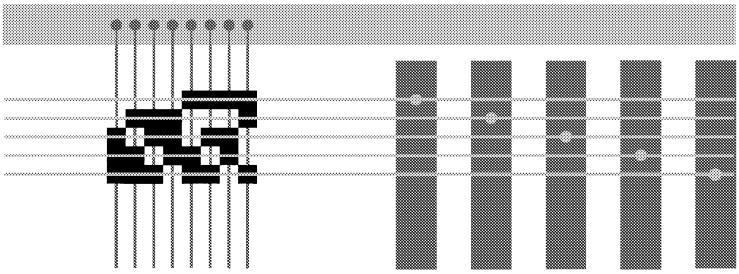


Figure 2.12: Customizable Nano-Via Decoding Patterns. From [91] "Array-Based Architectures for FET-Based, Nanoscale Electronics"

The nanoscale vias, represented by circles on the right, allow nanowires to directly connect to microwires accomplishing pitch reduction. These 'address' nanowires connect to an orthogonal set of 'core' nanowires through a customized nano-via decoding pattern, on the left. At each opening in the pattern, the two orthogonal sets of nanowires connect exhibiting FET behavior. The structure as diagrammed represents a scheme in which two address nanowires AND-ed together control one core nanowire, thus allowing for a larger set of nanowires to be controlled by a smaller set of microwires. Alternatively, in hopes of avoiding lithographic processes to pattern nanoscale features, as would be necessary for the nano-via decoding pattern, DeHon and collaborators have proposed a stochastic architecture in which controlled doping profiles of silicon nanowires acting as FETs are used to encode addressing, as shown in Figure 2.13.

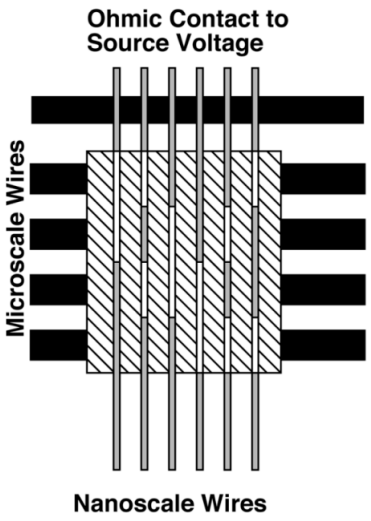


Figure 2.13: Modulated Nanowire Doping Profiles for Interfacing. From [92] "Stochastic Assembly of Sublithographic Nanoscale Interfaces"

In this system, the nanowires should be assembled, using the Langmuir-Blodgett technique, with a thin oxide separating them from the microwires. The different shades along the nanowires represent different doping profiles. The highly doped regions of the nanowires, shaded in gray, have a high threshold voltage. For these regions, it requires a higher voltage to deplete the carriers from the channel to stop conduction. In regions of low doping, represented in white, the threshold voltage necessary to deplete the channel and stop conduction is much lower. The addresses are coded into the nanowires through controlled placement of the doping profiles. With a large enough sample space, most of the wires can be uniquely addressed and the mapping can be discovered. [92, 95]

Other stochastic solutions include Kuekes and Williams proposed random assembly of nanometer-sized gold dots in between micro- and nanowires followed by programming and post-discovery of the existing address space. [96] This approach depends on a high density of gold colloids in the crossbar area. In addition, the wires must definitively connect or remain unconnected; otherwise there could be isolation problems. Yet another stochastic solution involves a hierarchical approach demonstrated by Tour *et al.* in which random nanoscale discontinuous gold islands are deposited and

bridged by molecularly functionalized metal nanowires that connect to lithographically defined micro-leads. [97, 98] They have successfully demonstrated control of the morphology of the discontinuous films, as well as a high selective attachment density of functionalized nanowires to these films. Essential to this research is that the films follow the Volmer-Weber growth mechanism. This formation is characterized by three-dimensional nucleation and island growth as shown in Figure 2.14.

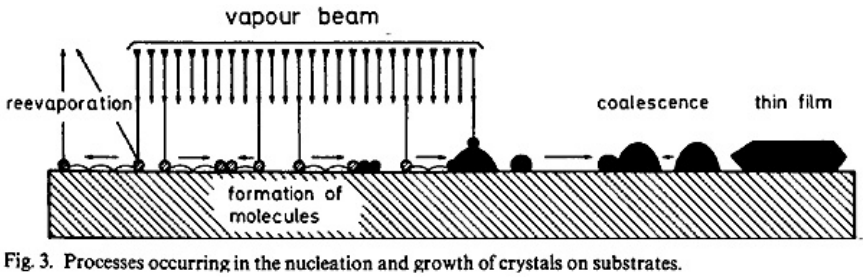


Fig. 3. Processes occurring in the nucleation and growth of crystals on substrates.

Figure 2.14: Volmer-Weber Growth Mechanism. From [99] "Heterogeneous Nucleation and Growth of Thin Films"

As more material is deposited, the islands conglomerate until eventually the film becomes continuous. This thickness, referred to as the critical thickness, is defined electrically as the point in which an electrically discontinuous film becomes electrically conducting. The position, slope, and width of this transition are dependent upon the condition of the substrate, the nature of the deposit, and certain ambient conditions including temperature and pressure. [100] Other methods of thin film formation include the van der Merwe mechanism, which represents layer-by-layer growth, and the Stranski-Krastanov mechanism, characterized by the formation of an initial monolayer followed by island growth. These methods are distinguished by the interaction strength between the deposited atoms and the substrate. [99] There are several ways to form discontinuous films, including but not limited to: electrodeposition, condensation of evaporated materials, condensation by sputtering techniques, post-deposition heat treatments and post-deposition ion-bombardment of continuous films. [101, 102, 103, 104] These experiments typically involve various metals, often gold and silver, deposited on various

substrates, frequently glass or carbon. There has also been great interest in palladium films due to their potential as hydrogen sensors. [105, 106, 107] Tour *et al.* used gold discontinuous films deposited using e-beam evaporation on top of a thermally grown silicon dioxide film. [98] Whether it be from hierarchical assembly using discontinuous films, other stochastic processes or precise alignment to nanoscale features, interfacing to the nano-world is essential to the development of fully integrated nano-systems.

2.4 Architectures for Nanotechnology

Thus far, it has been shown that molecules can be synthesized, molecular transport can be modeled and measured using characterization structures, and arbitrary nano-patterns can be fabricated and interfaced to the micro-world. How this all fits into an architectural design is the next level of abstraction that must be considered. One of the major differences between molecular electronics and current technologies is in the fabrication approach. Lithography dominates current processing techniques. Fundamentally, it represents a top-down approach, since it involves using excess materials and then removing what is unnecessary. Nanotechnology strives for a more bottom-up approach in which circuits are self-assembled, sometimes referred to as Chemically Assembled Electronic Nanocomputers (CAENs). [50, 108] Figure 2.15 compares some of the characteristics of these two approaches. As one might expect, these differences have a tremendous impact on architectural design.

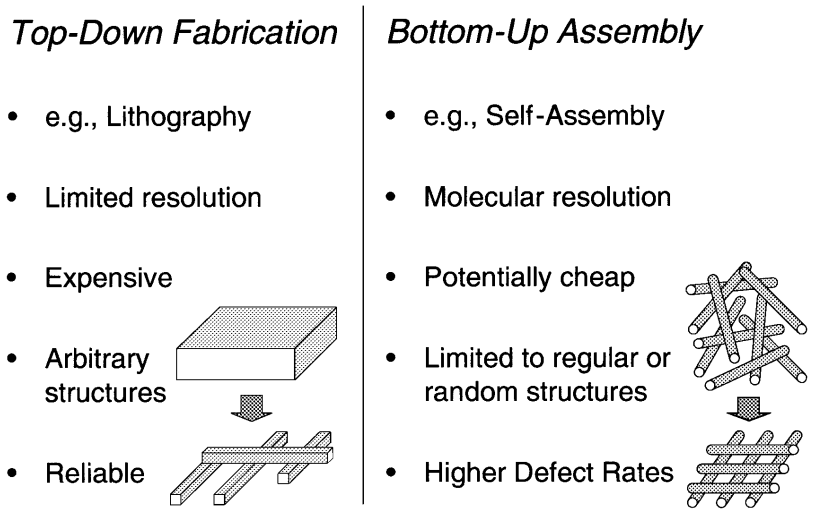


Figure 2.15: Comparing Top-Down Fabrication vs. Bottom-Up Assembly. From [93] "CMOS/Nano Co-Design for Crossbar-Based Molecular Electronic Systems"

The first difference to consider is the expectation that chemical synthesis will result in higher defect rates compared to today's solid-state fabrication methods. From an architectural perspective, 'defect tolerance' implies correct operation in the presence of hardware defects. Modern techniques, such as built-in redundancy and error correction, typically rely on low defect density, and therefore may not be as effective in bottom-up inspired architectures. [109] Thus, a great deal of research has been focused on investigating reconfigurable architectures. These types of architectures are able to tolerate defects in hardware by *reconfiguring* around them.

The primary example of a reconfigurable architecture is Hewlett Packard's Teramac machine. In this experiment, researchers intentionally used cheap and defect-prone parts for its construction. A software routine was used to identify these parts and then remap the intended function onto the reliable parts, resulting in a machine with superior performance as compared to today's single-processor computers. One of the lessons learned as a result of this experiment included the necessity for a high degree of connectivity to allow for rerouting and thus reconfiguration. In fact, wires were the most

abundantly used component in the Teramac, followed by switches and memory. The use of cheap but defective parts clearly emulates what is expected from self-assembled structures. Thus, HP successfully demonstrated the potential of reconfigurable architectures for nanotechnology. [8]

Another difference between top-down and bottom-up approaches is the type of structures that can be fabricated. Generally, architectures can be divided into three categories: deterministic, quasi-regular and stochastic, each representing less fabrication control than the prior. [109] Deterministic architectures, resembling top-down approaches, allow for almost arbitrarily complex designs and typically require no post-fabrication programming. Quasi-regular architectures have their functionality integrated into periodic and highly regular structures. Stochastic architectures are based on random or pseudo-random fabrication in which functionality is discovered post-fabrication or programmed. Bottom-up assembly tends to lend itself to either Quasi-regular or Stochastic type architectures due to its fabrication limitations. For these architectures to be viable, a high computational density must be achieved.

One example of a stochastic architecture is the NanoCell. In this system, bistable molecules are interconnected by an underlying random distribution of colloids, discontinuous films and/or nanowires. In theory, the system is trained to perform logic or memory post-fabrication, based on voltage pulses that switch the molecules on or off. These pulses originate from lithographically defined wires surrounding the perimeter of the active area, as shown in Figure 2.16.

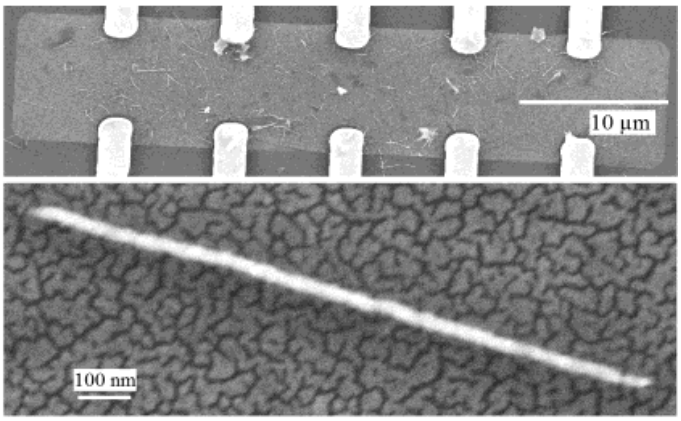


Figure 2.16: The NanoCell. From [97] "NanoCell Electronic Memories"

Simulations based on genetic algorithms using omniscient switching have demonstrated the potential functionality of such a structure. [110] More recent experiments suggest that current transport through the NanoCell is based on the breaking and reforming of metallic filaments, rather than molecular conduction. [97] Thus, the current focus of the NanoCell project is towards metal-less fabrication. However the strength of this design is in the concept that a disordered random system can be programmed post-fabrication to perform memory or logic. While fabrication of random structures has been demonstrated, configuring stochastic architectures post-fabrication remains very challenging. A compromise between stochastic architectures and deterministic architectures in both fabrication and configuration difficulty is the Quasi-regular architecture.

The most common quasi-regular architecture utilizes the crossbar array. Typically, a functional layer is sandwiched between two orthogonal sets of wires, as depicted in Figure 2.17.

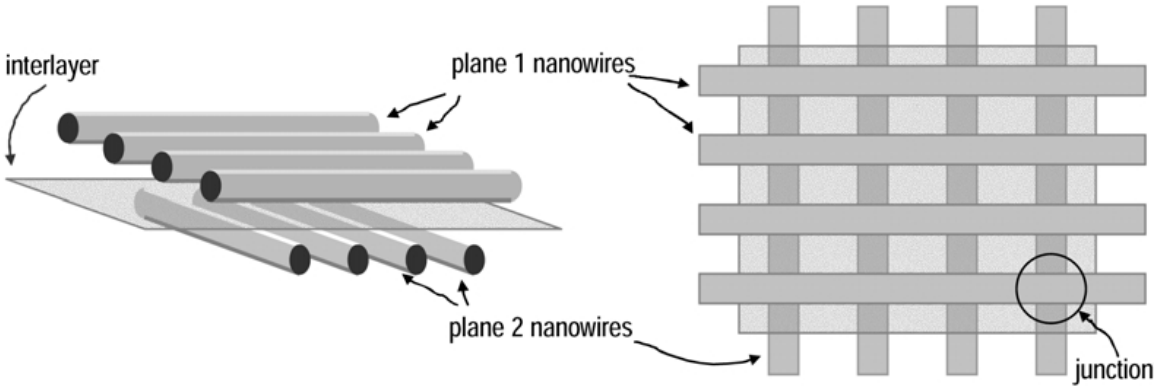


Figure 2.17: Crossbar Array. From [111] "CMOS-like Logic in Defective, Nanoscale Crossbars"

With bistable molecules as the interlayer, each junction could be written to and read from through a careful choice of the voltage levels applied to each wire. [112] Programming decoders into the crossbar allows for memory addressing as well as memory-based logic. [94] This relatively simple architecture is inherently redundant, reconfigurable and allows for high-device densities, making it very attractive to the nano-community.

Unfortunately, there are several limitations to the crossbar architecture. To start, the scalability of these architectures can be limited by the interconnect impedance. [113] Worst-case parasitic optimization is inhibited by the regularity of the structure. In addition, self-assembly strongly implies the use of two-terminal devices since self-assembly of three-terminal devices remains very challenging. Diode-resistor logic, so common to the field, lacks both gain and inversion. In theory, the latter can be remedied by including both the signal and its complement, certainly a non-optimal solution. The lack of gain restricts the scaling of the crossbar without signal restoration. Some authors have proposed the use of a CMOS interface to remedy this, a design commonly referred to as "nano on CMOS" (NoC). While the functional distribution and granularity of the nano components remain open ended issues, NoC introduces significant versatility into architectural design. [93, 114]

"Nano on CMOS" is an example of a hybrid architecture. It will be very difficult for any nanotechnology to directly compete with well established and well funded CMOS technology. Thus, many researchers believe that hybrid architectures represent the more immediate future for molecular electronics. In particular, combining silicon technologies with molecular technologies may enable CMOS to overcome certain physical barriers while simultaneously improving its performance, as suggested for memory applications. [115, 116]

Architectures for nanotechnology tackle many unique design problems. In particular, self-assembly plays a major role in the complexity of structures that can be fabricated and their inherent defect density. As a result, reconfigurable quasi-regular or stochastic architectures have garnered the most attention from researchers. Some degree of programming post-fabrication seems likely. In addition, there is also great potential in combining molecular and silicon technologies. Perhaps there is yet another design that will prove useful for computational nanotechnologies. For example, an embryonics approach based on self-repair and self-replication inspired by molecular biology may be a more natural paradigm for molecular electronics. [117] Architecture is still an open ended issue that will require continued development and creativity.

2.5 Conclusion

The semi-conductor industry has made tremendous progress keeping pace with Moore's law, however current silicon technology scaling appears to be running out of steam. Nevertheless, comparing predicted physical limitations to fundamental limitations reveals that there is still tremendous potential to continue scaling. Therefore new paradigms must be investigated that can continue current trends. One such area is molecular electronics in which molecules are used as electronic devices. While great strides have been made in the synthesis of diverse complex molecules, modeling charge transport is still very challenging. Researchers need to be very careful in their application of models that can suffer from computational anomalies. In addition, truly supporting

experimental data with theoretical models remains challenging due to the often unknown nature of the characterization structures at the atomic scale.

A number of creative characterization structures have been developed to measure the electrical response of molecules. These include the crossed-wire tunnel junction, scanning probe microscopy techniques, the mechanically controllable break junction, structures employing electrochemical narrowing or dielectrophoresis, and evaporated and mercury drop top contact test-beds. They range from contacting large areas to as little as one molecule. Several researchers have reported qualitative agreement when testing similar molecules in different structures. One recurring theme is the importance of the metal/molecule/metal contacts. Whether they are symmetric, asymmetric, physically bonded or chemically bonded, the contacts have a tremendous impact on the current response. Even the atomistic nature of the probes can alter the response. One of the problems with many of the current characterization structures is that they cannot be easily integrated into devices. Other issues include questions on their reliability, difficulty in forming the top contact, and in interpretation of their results. There is no single characterization structure that has become the standard for screening molecules, however much has been learned with the diverse collection of structures currently developed.

Building characterization structures for molecular electronics is only one application of nanofabrication. The ability to pattern nanoscale features is essential for the continued development of nanoscience and the miniaturization of integrated circuits. Several methods to fabricate at the nanoscale include: photolithography with smaller and smaller wavelengths, electron beam lithography, focused ion beam lithography, scanning probe lithography, edge-based lithography and chemical self-assembly. Unfortunately, the high cost, low throughput or limited types of patterns that can be fabricated with the above methods can limit their use in mass production. Nanoimprint lithography has been suggested as a possible solution to these problems. Unfortunately, imprint lithography comes with its own set of challenges, including alignment, adhesion, thermal effects, material transport and stamp lifetime. While ones application and available resources currently determine the most appropriate nanofabrication technique; it remains to be seen

which method, if any, will replace photolithography as the predominant fabrication method.

While nanoscale patterns can be fabricated, connecting them to the outside world represents the next major challenge to fully integrated nano-systems. Interfacing with the nano-world requires both pitch reduction and decoding, so multiple nanowires can be controlled by fewer microwires, thus retaining the pitch advantage of the nanoscale. Most of the current solutions to the interface challenge require either some degree of nano-alignment or involve a stochastic process which may not guarantee full connectivity. In addition, this area has remained largely theoretical, since few of the solutions to this problem have actually been fabricated. An opportunity therefore exists for the demonstration of a determinant fully-connected interface without the need for nano-precision alignment.

Assuming molecules can be synthesized, modeled, characterized, interconnected and interfaced to the micro-world; the next challenge is integrating this into a system-level architecture. It is believed that molecular electronics will take a bottom-up approach to fabrication, with self-assembly playing a significant role. The implications of this affect architectural design. For example, bottom-up assembly is expected to result in a relatively high defect density making it important to consider architectures that are both default tolerant and reconfigurable. Self-assembly of three-terminal devices remains challenging, generally limiting researchers to diode-resistor logic that lacks both gain and inversion. It is believed that molecular architectures will be highly periodic, thus crossbar arrays have been studied extensively. Alternatively, stochastic architectures in which post-fabrication programming and discovery is required are also under investigation. Perhaps there are other architectural designs that can better exploit the characteristics of self-assembly. It is likely that hybrid architectures with current silicon technologies, as well as sensors and other application specific systems, are more likely in the immediate future for molecular electronics. While molecular electronics has made tremendous strides, there is still a great deal of challenges, and thus opportunity, for research in this field.

Chapter 3

Nanowire Fanout and Interconnect Structure

Physically interfacing the nanoworld with the microworld presents a critical challenge for testing, nanocomputing, and fully integrated nanosystems. Successful interface strategies require physical connection to the nanoworld without compromising functional density. In this chapter, a simple approach is presented that permits fully deterministic cross-connect of orthogonal wiring arrays without the need for nanoprecision alignment. It is independent of the technology used to fabricate the nanowires, enabling interconnect and fanout for technologies in which alignment remains very challenging, such as in nanoimprint lithography. The design exploits the system geometry, particularly angles, to solve the problem of pitch reduction. However, no restrictions are placed on the minimum size of the nanowire pitch. Rather than mask alignment precision, the challenge of pitch reduction is shifted to the ability to fabricate structures at the micrometer-scale. The approach is fully determinant, avoiding connectivity issues that can arise from stochastic solutions. The purpose of this study is to prove through analysis and derivations that the system is both feasible and scalable to dimensions appropriate for molecular and ultra-dense electronics. In addition, the process is relatively simple and is presented from a fabrication perspective, critically addressing the effect of potential processing errors on the structure. A demonstration of this concept has been fabricated and characterized.

This chapter is organized as follows. In Section 3.1 the system is presented and the system variables are defined. Section 3.2 demonstrates the novelty of the design, particularly the elimination of any critical x-y alignment during fabrication. In Section 3.3 the equations that govern the system are derived. Section 3.4 compares various alignments and identifies an interesting novelty of the design. Section 3.5 addresses how potential fabrication errors could affect the system. Section 3.6 presents an alternate process flow using multi-level imprinting that has several advantages. In Section 3.7, the

design, fabrication and characterization of a proof-of-concept structure is reviewed. Finally, Section 3.8 summarizes the major points made in this chapter.

3.1 Process Flow

The basic process flow, shown in Figure 3.1, begins with fabrication of the nanowire array at a target wire width and spacing, w_1 and s_1 respectively. Next, the wires are covered with a thin insulator. A cut is made in the insulator at a certain angle, ϕ, and width, w_c. Finally, perpendicular connecting wires are fabricated at a target wire width and spacing, w_2 and s_2 respectively.

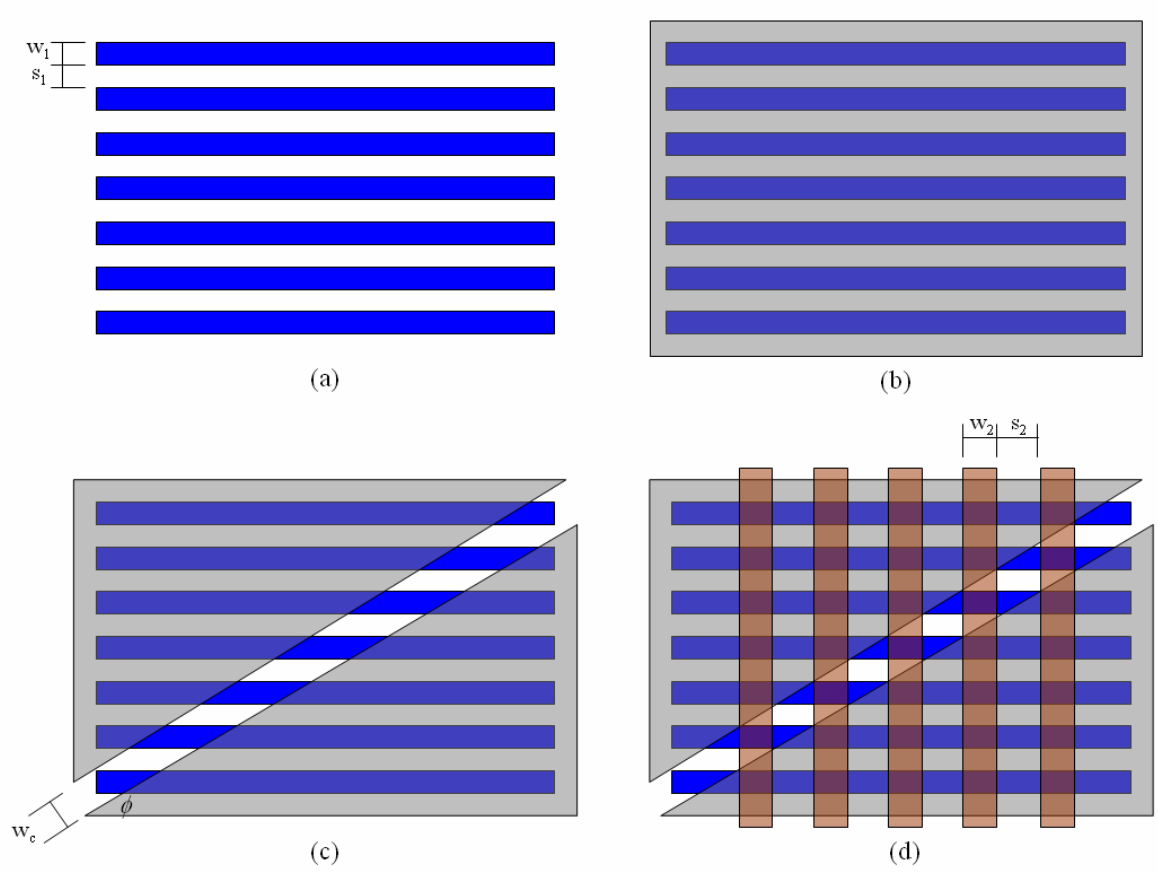


Figure 3.1: Basic Process Flow for Fanout Structure: (a) fabricate nanowire array, (b) cover with insulator, (c) open cut in insulator and (d) fabricate connecting wire array.

The two sets of wires remain electrically isolated everywhere except in the insulator cut. Ideally, each microwire will connect to one and only one nanowire. In this way, fanout from the nano-world to the micro-world is achieved. The ‘nanowire’ array does not physically have to be at the nano-scale, therefore in this work these wires will often be referred to as horizontal wires (or hwires). Similarly, connecting wires will often be referred to as vertical wires (or vwires) since they can be either nano- or micro-sized, depending on the application of the structure.

3.2 Novelty

The novelty of this design is that there exists a set of values for the physical dimensions of the system such that the two orthogonal wire arrays can connect without any critical x-y alignment, as demonstrated in Figure 3.2. Note, the oxide will no longer typically be drawn but is replaced with the oxide cut and is still assumed to be isolating the two sets of wires everywhere except in the cut. In this example, the connecting wires are increasingly ‘misaligned’ in the horizontal direction. The first system depicts a configuration in which microwire m_1 connects nanowire n_1, m_2 connects n_2, and m_3 connects n_3. As shown in the second system, a slight misalignment of the microwires has no affect on the connectivity of the system. In the final system, the wires are ‘misaligned’ beyond a certain tolerable allowance resulting in an alternate configuration in which an additional microwire m_0 connects n_1, m_1 now connects n_2, and m_2 now connects n_3.

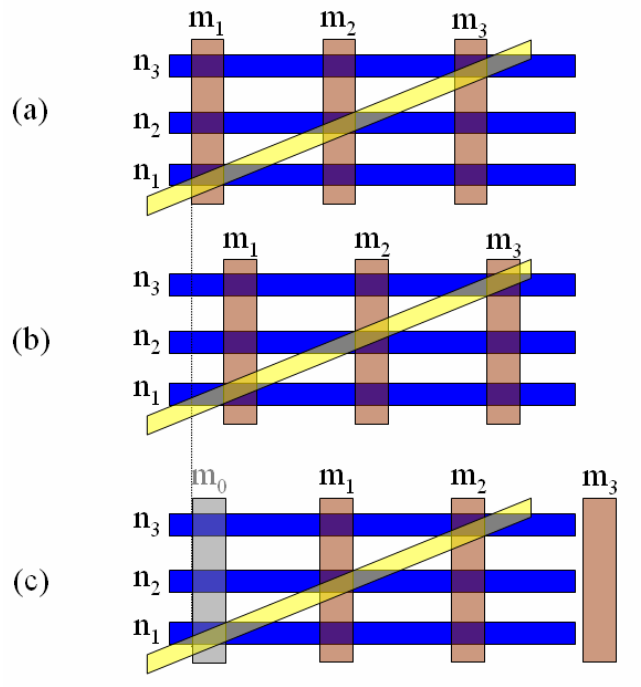


Figure 3.2: Demonstration of Novelty. As the connecting wires are increasingly 'misaligned' from (a) to (c), the system remains one-to-one connected.

By padding with extra wires, e.g. m_0, complete connectivity can still be guaranteed despite any gross misalignment. Thus, complete cross-connect of regular arrays of wires can be achieved without the limitation of any critical translational alignment.

3.3 Unique Connectivity

Only systems whose geometry meets a certain set of criteria will be able to exploit the novelty of this design. In this section, the fundamental equation relating the two wire array pitches and the insulator cut angle is derived. In addition, the optimal cut width and optimal vertical wire pitch that guarantee unique one-to-one connectivity are derived.

3.3.1 Insulator Cut Angle

One important feature of this design is that there is no theoretical limitation placed on the nanowire pitch. It can be as small or as large as desired, and represents the critical

dimension of the system. To assist in deriving this pitch, the simple 2x2 system is considered as in Figure 3.3.

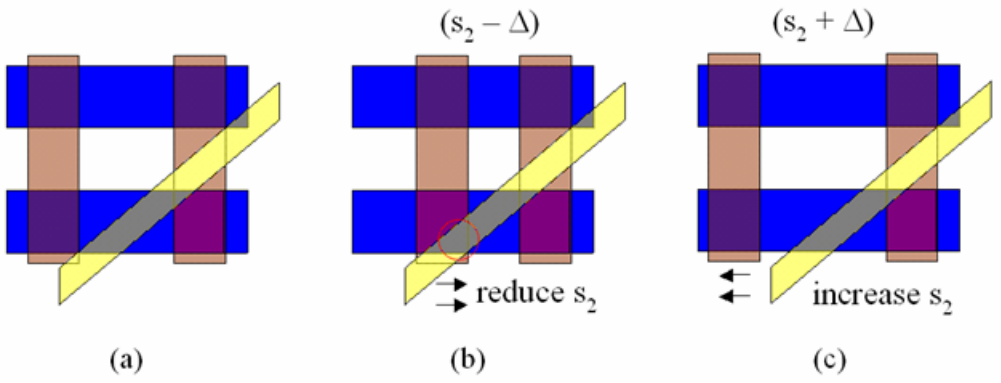


Figure 3.3: Varying the Vertical Wire Spacing: (a) the initial system, (b) the spacing is reduced causing a short and (c) the spacing is increased having no effect on the system.

As shown in Figure 3.3(b), when the left vwire is moved closer to the right vwire, reducing s_2 and thus the vertical wire pitch, the bottom hwire shorts both vwires together. This would imply that the vertical wire pitch has to be large enough so that the cut travels at least the horizontal wire pitch; otherwise, two vertical wires can be shorted by one horizontal wire. However, when s_2 is increased, effectively increasing the vertical wire pitch, there is no shorting. With the help of Figure 3.4, this relationship is derived.

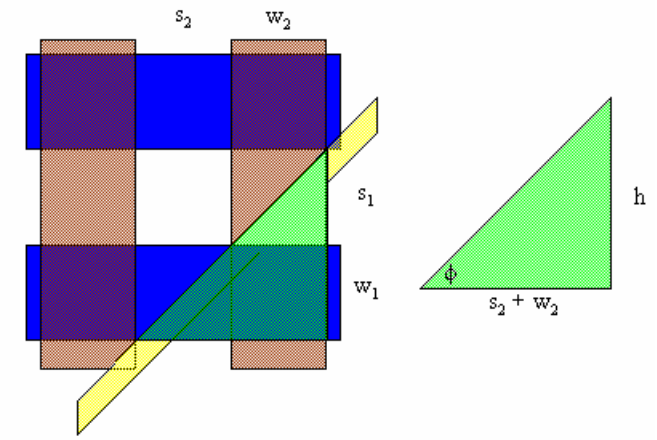


Figure 3.4: Deriving the Maximum Pitch

Let h equal the distance the cut travels over the vertical wire pitch, than from above:

$h \geq (s_1 + w_1)$, and since $h = (s_2 + w_2) \tan \phi$, therefore: $(s_2 + w_2) \tan \phi \geq (s_1 + w_1)$.

Now consider the impact of varying the vertical wire pitch by sliding the right vertical wire rather than the left, as demonstrated in Figure 3.5.

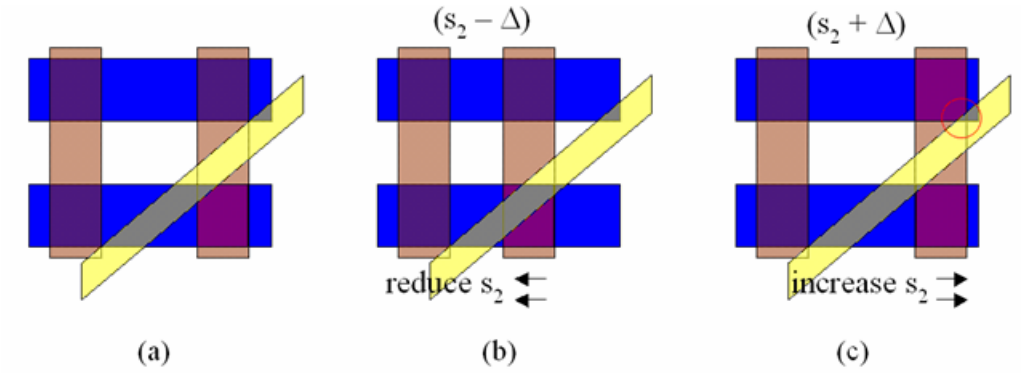


Figure 3.5: Alternate Variation of the Vertical Wire Spacing: (a) the initial system, (b) the spacing is reduced having no effect on the system and (c) the spacing is increased causing a short.

In this example, when the right vwire is moved closer to the left vwire, reducing s_2 and thus the vertical wire pitch, there is no effect on the connectivity. However, increasing the vertical wire pitch by sliding the right vwire further from the left wire causes one vertical wire to short two horizontal wires. This leads to the derivation of the following requirement: $(s_2 + w_2) \tan \phi \leq (s_1 + w_1)$.

Thus, opposite inequalities were derived depending on which vwire was moved. The difference between sliding the left vwire versus the right vwire was simply choosing an alternate point of rotation, as demonstrated in Figure 3.6.

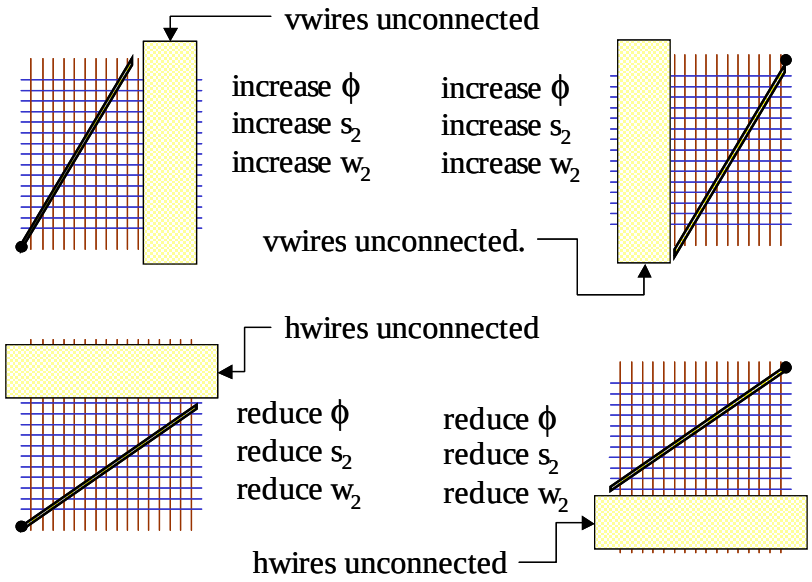


Figure 3.6: Examining the Relationship of the Vertical Wire Pitch and the Cut Angle

Increasing the pitch is equivalent to increasing the cut angle; just as decreasing the pitch is equivalent to decreasing the cut angle. From Figure 3.6, it is clear that any inequality has the potential to result in open connections. The connectivity of the system would then become size dependent. Therefore, the fundamental equation governing the two wire array pitches and the insulator cut angle is the equality:

$$(s_2 + w_2)\tan f = (s_1 + w_1) \qquad \textit{Equation 3.1}$$

From this equation, the insulator cut angle can be solved for:

$$f = \tan^{-1}\left[\frac{(s_1 + w_1)}{(s_2 + w_2)}\right] \qquad \textit{Equation 3.2}$$

An example of a system in which this angle is not achieved is illustrated in Appendix A.1.

Investigating the relationship between the size of the connecting wires and the insulator cut angle helps to illustrate the versatility of this structure. Figure 3.7 depicts this relationship for an assumed nanowire width of 10nm.

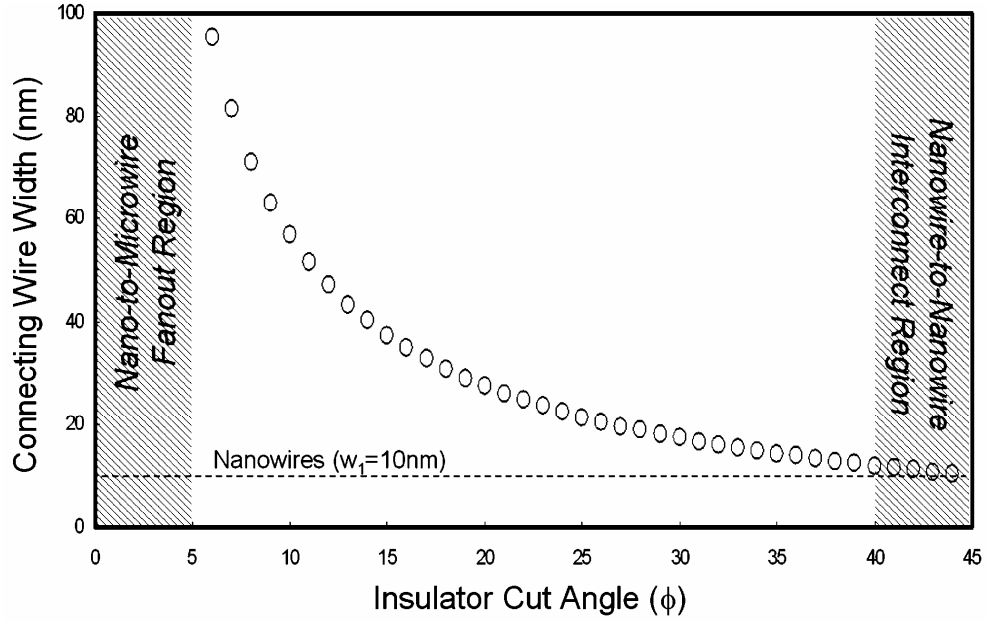


Figure 3.7: Connecting Wire Width vs. Insulator Cut Angle

Choosing the appropriate insulator cut angle depends upon the desired connecting wire width. To fanout from 10nm wires to wires greater than 100nm in width, cut angles less than 5^o would be necessary. Alternatively, at a cut angle of 45^o, the two sets of wires would have equivalent dimensions and nanowire interconnect is achieved. Thus, the desired application of this design governs the choice of the cut angle. It is important to note that as the connecting wire width increases, the nanowires must run defect free over relatively longer distances. Thus, there exists a tradeoff between full fanout and the ability to fabricate long nanowire arrays. Hierarchical application of this technique is one way to balance this tradeoff.

While the equations derived in this section govern the wire array pitches and the cut angle, the dependency on the cut width has yet to be determined. The maximum cut

width, minimum cut width, and the minimum cut width to maximize the contact area, can all have important implications on the design of the system. These equations have been derived and discussed in Appendix A.2. The next section derives the optimal cut width and the optimal connecting wire dimensions needed to guarantee unique connectivity.

3.3.2 Optimal Equations

While the above equations govern the total wire pitches and the cut angle; they are not enough to guarantee one-to-one connectivity. Two additional criteria must be met: to avoid shorts, no connecting wire can contact multiple nanowires; and to avoid opens, each connecting wire has to contact at least one nanowire. From these requirements, the optimal cut width and the optimal connecting wire dimensions are derived. If these optimal dimensions are fabricated, there will exist a unique one-to-one mapping between nanowires and connecting wires.

The optimal vertical wire and spacing dimensions necessary to exploit the novelty of this design are derived with the definition of two new variables, c_2 and g_2, as illustrated in Figure 3.8.

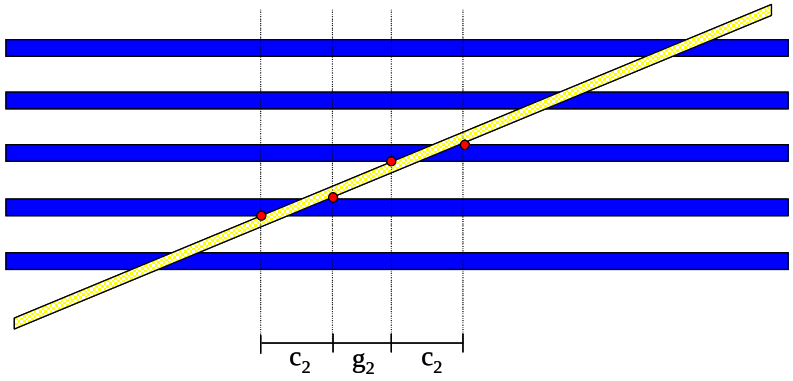


Figure 3.8: The Optimal Vertical Wire Pitch

c_2 is the width of a vertical wire that would contact the horizontal wire over the entire cut opening. g_2 is the width at which a vertical wire could completely miss the cut, or the gap between two successive c_2's. Thus, if w_2, the vertical wire width, is less than or equal to g_2, there is no way for it to contact multiple horizontal wires. Similarly, if s_2,

the vertical wire spacing, is greater than or equal to c_2, there is no way for two vertical wires to connect the same horizontal wire. This may seem counterintuitive since the vertical wire width is being defined as the gap in which it could theoretically miss both horizontal wires, but this is necessary to ensure there is no shorting. Similarly, defining the vertical wire spacing as the width of a wire that would completely intersect the horizontal wire over the extent of the cut is counterintuitive, but necessary to prevent opens. The values for c_2 and g_2, and thus the vertical wire pitch dimensions, are derived with the help of Figure 3.9.

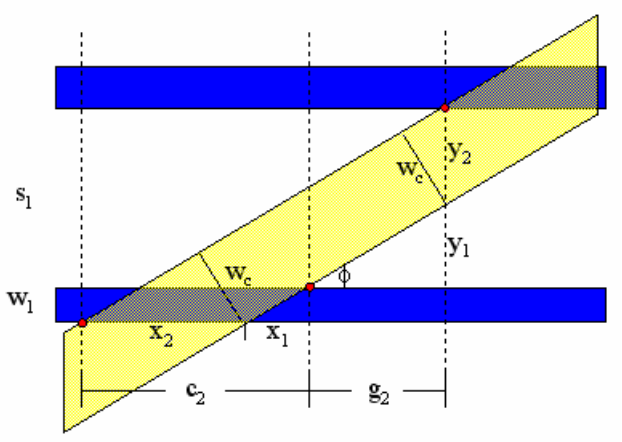


Figure 3.9: Deriving the Optimal Vertical Wire Pitch

Deriving c_2:

$c_2 = x_1 + x_2$, where $x_1 = w_1 / \tan \phi$ and $x_2 = w_c / \sin \phi$, therefore:

$c_2 = w_1 / \tan \phi + w_c / \sin \phi$,

Deriving g_2:

$g_2 = y_1 / \tan \phi$, where $y_1 = s_1 – y_2$, where $y_2 = w_c / \cos \phi$, and therefore:

$g_2 = (s_1 – w_c / \cos \phi) / \tan \phi$, or distributing the tangent denominator:

$g_2 = s_1 / \tan \phi – w_c / \sin \phi$.

Setting $s_2 = c_2$ and $w_2 = g_2$ defines the optimal vertical wire pitch.

$$s_2 = \frac{w_1}{\tan f} + \frac{w_c}{\sin f},\ w_2 = \frac{s_1}{\tan f} - \frac{w_c}{\sin f}$$ *Equation 3.3*

Now that the optimal vertical wire pitch has been derived, the optimal cut width must be investigated. The optimum cut width needs to guarantee connection to one and only one horizontal wire. To guarantee connection to at least one nanowire, the cut must span at least the nanowire spacing, s_1, over the connecting wire width, w_2. If the cut is too narrow, the connecting wire may not intersect the target nanowire, as shown in Figure 3.10. To avoid this, there must be a minimum condition on the vertical distance the cut travels over the width of the connecting wire: $h_1 + h_2 > s_1$.

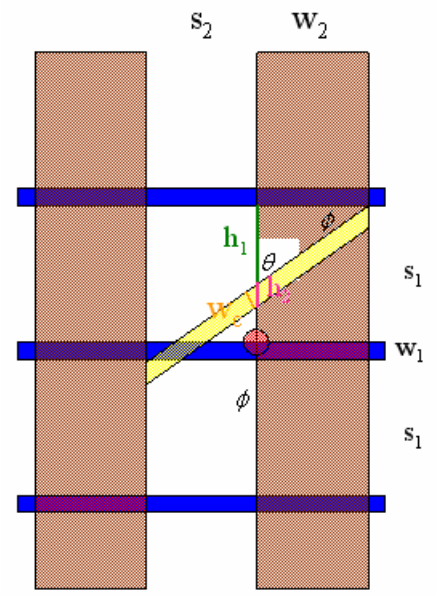


Figure 3.10: Deriving the Optimal Cut Width

To guarantee connection to no more than one horizontal wire, the cut must travel no more than one nanowire spacing, s_1. Thus the combination of these two requirements results in the equality being the optimum condition. Therefore, the optimal cut width is derived:

$h_1 + h_2 = s_1$, where $h_1 = w_2 \tan \phi$, and $h_2 = w_c / \cos \phi$, and thus:

$w_2 \tan \phi + w_c / \cos \phi = s_1$, and solving for w_c results in:

$$w_c = (s_1 - w_2 \tan f)\cos f \qquad \textit{Equation 3.4}$$

Notice that depending on the dimensions of the system, there is potential for the optimal cut width to be negative and thus non-physical. These conditions and their implications on the system are discussed in Appendix A.3. The equivalency of the optimal cut width and the optimal vertical wire pitch is proven in Appendix A.4, since clearly the optimal conditions cannot be mutually exclusive.

As previously mentioned, there are no minimum limitations placed on the nanowire pitch. A designer chooses the target nanowire pitch and the resulting insulator cut angle is defined in Equation 3.2, the optical vertical wire pitch is defined in Equation 3.3, and the optimal cut width is defined in Equation 3.4. Fabricating these optimal dimensions guarantees that the system will be uniquely connected, but there is no guarantee on what that connectivity will be. In fact, in the example given to demonstrate the novelty of this design, the connectivity of the system changed after a certain 'tolerable allowance' in the alignment. Microwire (m_i) no longer connected nanowire (n_i), but rather nanowire (n_{i+1}). This is adequate for applications that simply require complete connectivity, or for those in which the resulting connectivity can be discovered post-fabrication or reconfigured, but *not* for applications in which a pre-determined connectivity is required. For example, consider a non-symmetric system with unique molecular devices at the cross-points, as illustrated in Figure 3.11.

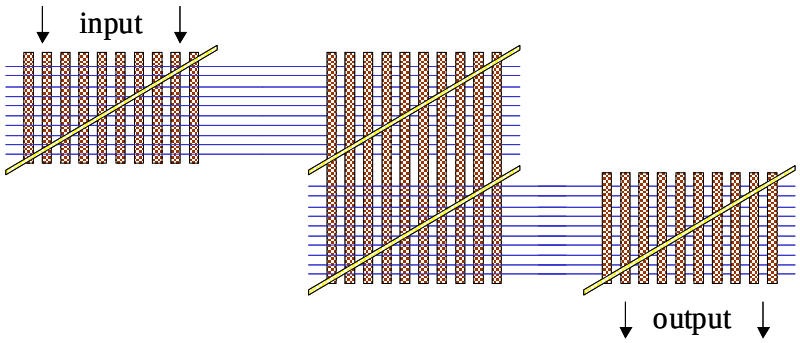


Figure 3.11: Example of System in which Specific Connectivity Matters

If it is critical to ensure the sequence of logic on the input, than each vertical wire and horizontal wire would have to be connected as designed to execute the desired function. For applications like these in which certain vertical wires must be connected to target horizontal wires, the alignment must fall within an allowable displacement. Deriving this alignment tolerance, which is investigated in the next section, is essential to establishing the alignment boundaries for a target connectivity.

3.4 Deterministic Connectivity

Although any alignment will interconnect the two orthogonal sets of wires, not all alignments are equally desirable. For example, consider Figure 3.12 which demonstrates three different alignments of the cut, all made at the target cut angle.

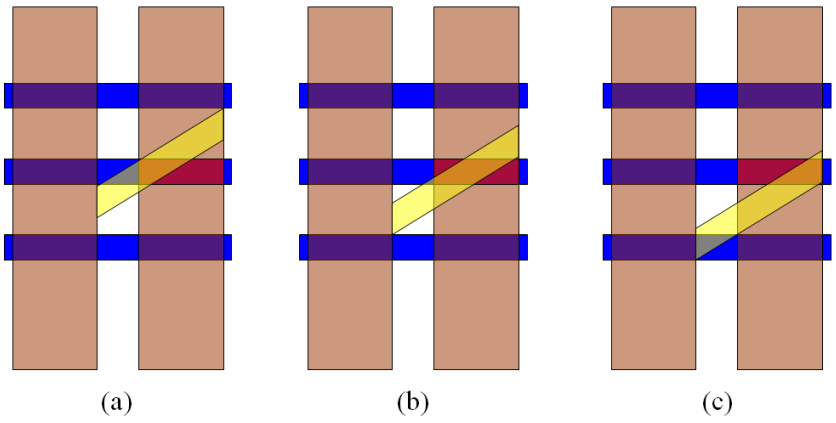


Figure 3.12: Example of Different Alignments

Clearly the center alignment might be advantageous since it results in the largest contact area. However, are there advantages to an alternate alignment? Is it possible to deterministically connect target nanowires with target microwires? In this section, these questions are answered and in doing so, a key novelty of the design is demonstrated.

3.4.1 Establishing the Alignment Tolerance for Deterministic Connectivity

In order to understand the affect the alignment has on the connectivity of the system, it is important to establish the limitations on this alignment. Deriving this alignment tolerance is essential to establishing the alignment boundaries for achieving a target connectivity. To accomplish this requires an analysis of several different alignments. This analysis is indexed on aligning the cut to the rectangle made by the right most vertical wire, w_2, and the top most horizontal spacing, s_1, indicated by a brown square in Figure 3.13.

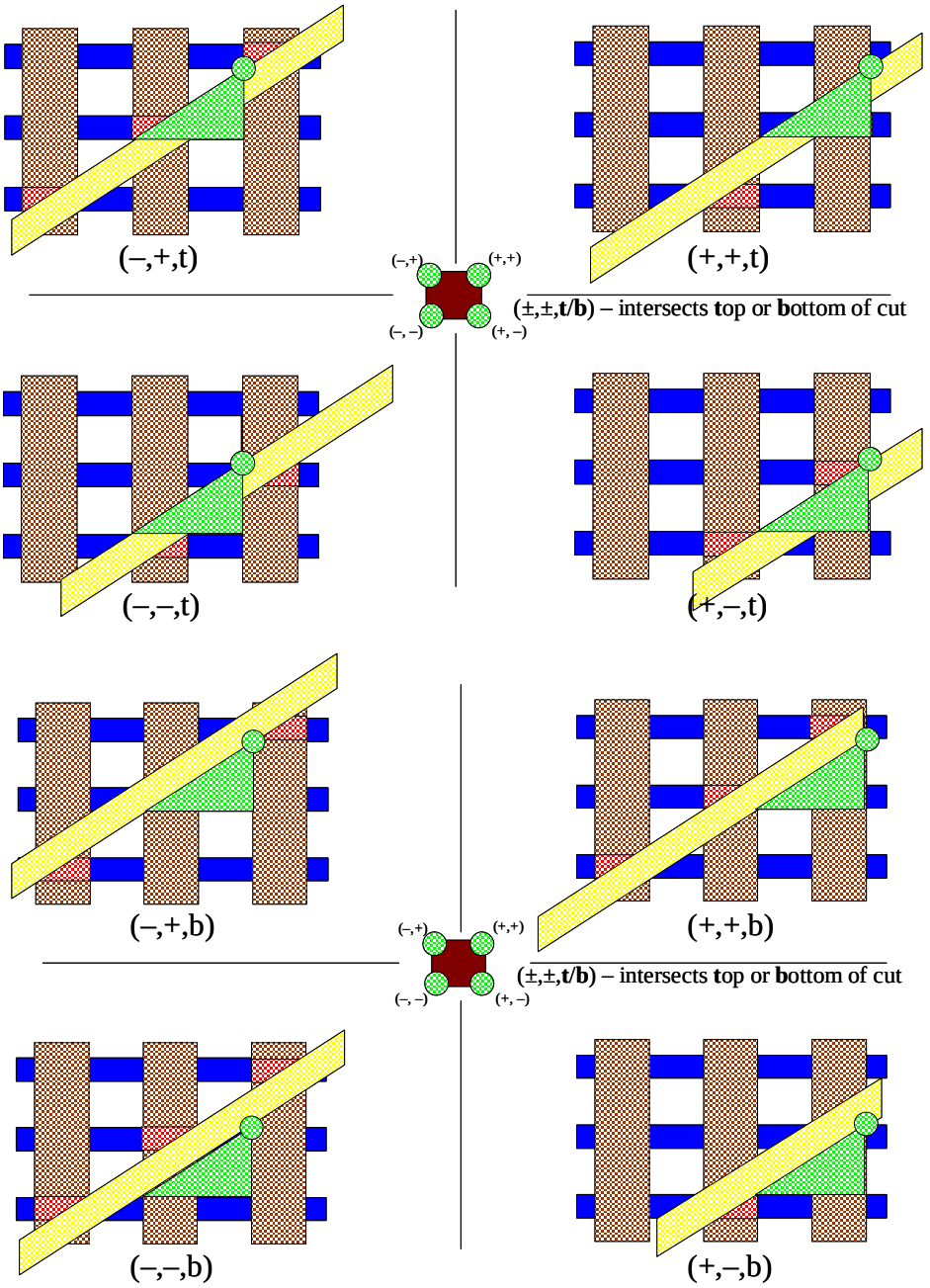


Figure 3.13: Examples of Cut Alignment Boundaries

The first two coordinates in the ordered triplet that indexes these alignments represents the location on the target square that the cut intersects, indicated by a green circle. The third coordinate represents whether the top or bottom of the cut intersects that

point. For each alignment, the horizontal and vertical tolerable displacement is derived, i.e. how far the cut can travel horizontally and vertically before it intersects a non-target junction. An example, based on the (–,–,b) alignment, is shown in Figure 3.14.

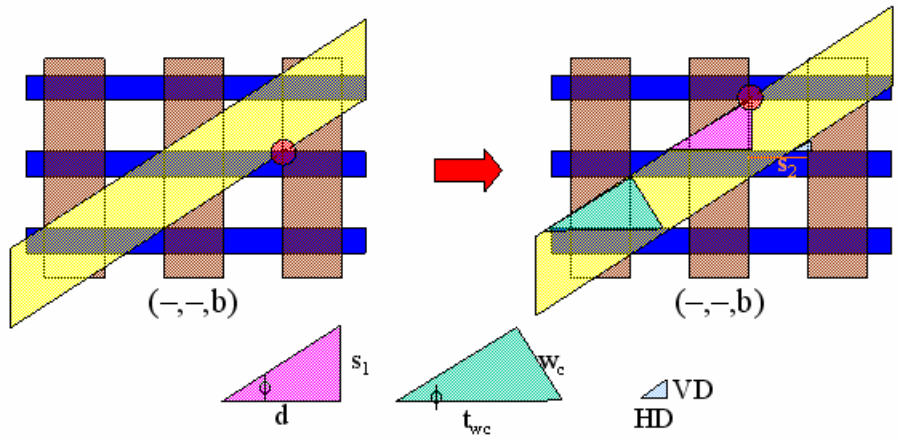


Figure 3.14: Analysis of Alignment (–,–,b)

The left system depicts the original alignment; while the right system depicts an alignment in which the cut is shifted to the furthest point without intersecting a non-targeted junction. The distance of this horizontal/vertical shift is called the horizontal/vertical displacement. With the help of Figure 3.14, the displacements for alignment (–,–,b) are derived:

Horizontal Displacement (HD) = $s_2 + d - t_{wc}$, where $d = s_1 / \tan \phi$ and $t_{wc} = w_c / \sin \phi$ so:

$HD = s_2 + s_1 / \tan \phi - w_c / \sin \phi$,

From Figure 3.14, it is obvious that the vertical displacement is just the product of the horizontal displacement with the tangent of the cut angle, therefore:

$VD = s_1 + s_2 \tan \phi - w_c / \cos \phi$,

Notice that in this example, there is only tolerance for the cut to shift up or to the left. Any infinitesimal movement of the cut down or to the right results in intersecting a non-targeted junction. Therefore, this point is considered to be in the bottom right corner

of the allowable displacement window, as will be discussed later. The next alignment considered, (+,+,b), is shown in Figure 3.15.

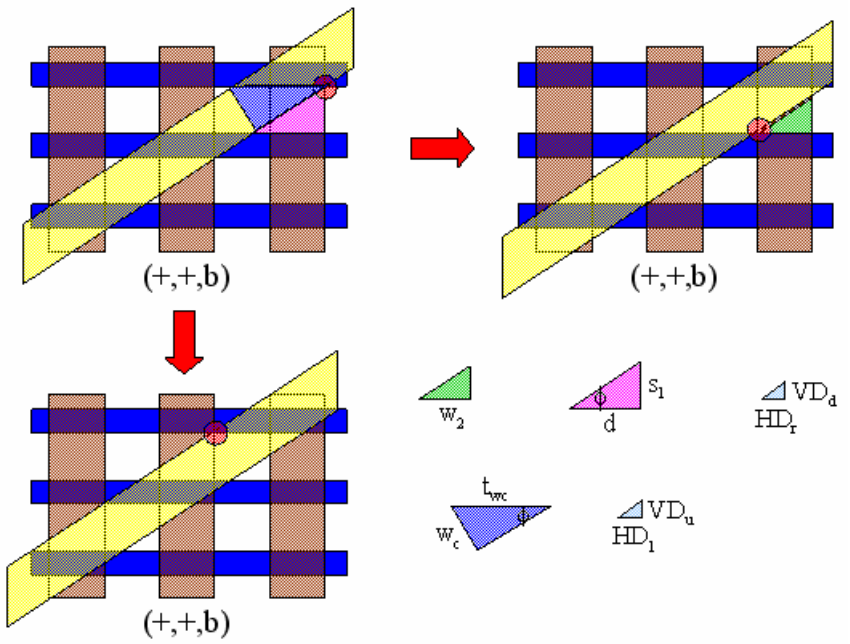


Figure 3.15: Analysis of Alignment (+,+,b)

The top left system depicts the original alignment; while on the right is the structure with the alignment shifted down and to the right. Below the original structure is the alignment shifted up and to the left. Obviously the original alignment was *not* on a boundary of the displacement window since there was tolerance for the cut to move in any direction and still avoid connections to non-target junctions. The distances of the componential shifts are calculated with the help Figure 3.15.

HD_r (HD to the right) = $d - w_2$, where $d = s_1 / \tan \phi$ so:

$HD_r = s_1 / \tan \phi - w_2$,

VD_d (VD down) = $HD_r \tan \phi$ or:

$VD_d = s_1 - w_2 \tan \phi$,

HD_l (HD to the left) = $s_2 + w_2 - t_{wc}$, where $t_{wc} = w_c / \sin \phi$ and so:

$HD_l = s_2 + w_2 – w_c / \sin \phi$,

VD_u (VD up) = $HD_l \tan \phi$ or:

VD_u (VD up) = $(s_2 + w_2) \tan \phi – w_c / \cos \phi$,

The sum of the componential displacements should equal the total displacements derived above for the boundary alignment (–,–,b). First for the horizontal components:

$HD_r + HD_l$ should equal HD,

$HD_r + HD_l = (s_1 / \tan \phi – w_2) + (s_2 + w_2 – w_c / \sin \phi)$, rearranging and canceling out w_2:

$HD_r + HD_l = s_2 + s_1 / \tan \phi – w_c / \sin \phi$, which is HD, as expected.

For the vertical components:

$VD_d + VD_u$ should equal VD,

$VD_d + VD_u = (s_1 – w_2 \tan \phi) + ((s_2 + w_2) \tan \phi – w_c / \cos \phi)$, canceling out $w_2 \tan \phi$:

$VD_d + VD_u = s_1 + s_2 \tan \phi – w_c / \cos \phi$, which is VD, as expected.

Thus, HD and VD represent the full displacements, i.e. the maximum distance the cut can travel before a non-target junction is connected. The componential displacements represent the displacement in a certain direction for an alignment that has tolerance to move in any direction. A careful analysis of the alignments reveals that there are four pairs that are equivalent due to the symmetry of the structure: (–,+,b) and (+,+,t); (–,–,t) and (+,–,b); (–,+,t) and (+,+,b) and finally (–,–,b) and (+,+,b). Deriving the displacements for all of the alignments (not shown here for brevity) results in the alignment tolerance window illustrated in Figure 3.16.

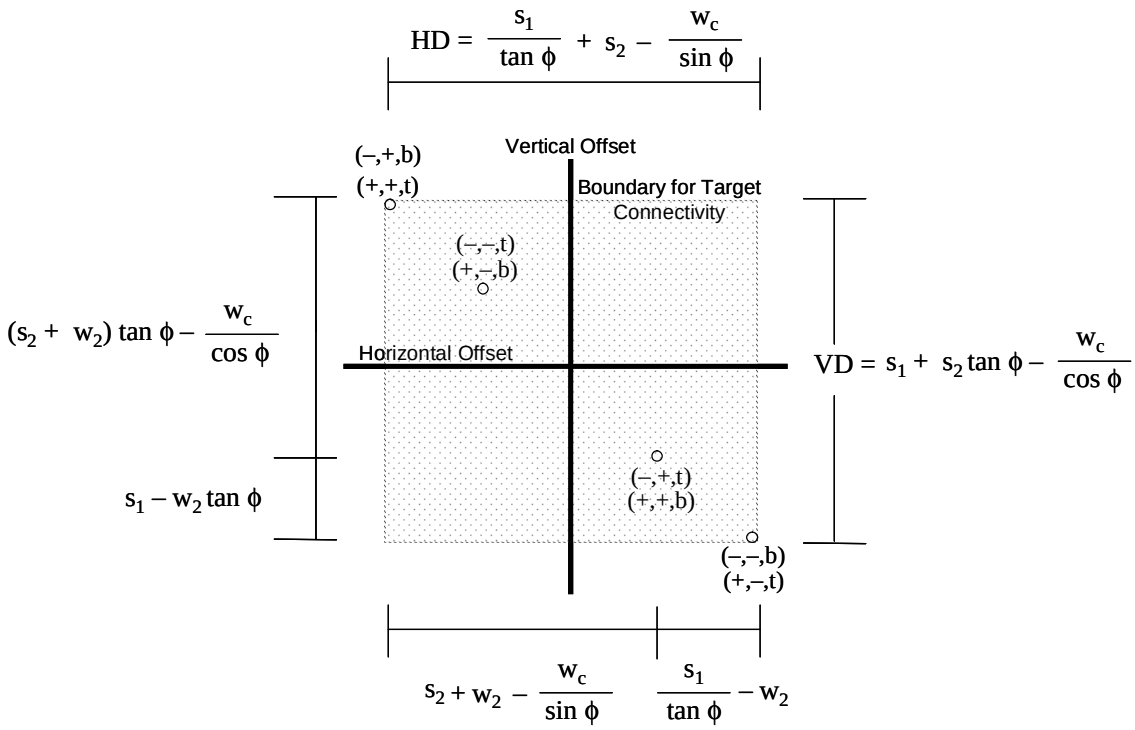


Figure 3.16: Alignment Tolerance Window for Target Connectivity

As an example, consider the point (–,–,b) from above. For that alignment it was shown that the only directions the cut could move without shorting a non-target junction were up and to the left. In Figure 3.16, that alignment is located in the bottom right corner, just on the boundary for target connectivity. The only directions it can move within the window are up and to the left, and it is HD and VD away from the top left corner of the window, just as derived. Now consider the other example, alignment (+,+,b). Its exact placement in the window depends on the cut width; however, it is not on the boundary and has tolerance to move in any direction, the magnitude of which is as derived. Thus, this window is critical in visualizing the limitations on the alignment. HD and VD govern the amount of allowable alignment tolerance before microwire (m_i) no longer connects nanowire (n_i) but rather nanowire ($n_{i\pm1}$). Clearly targeting an alignment at the center of this window would be preferred, since this would allow for the maximum alignment tolerance in any direction. Appendix A.5 investigates the design impact of this

center alignment, as well as the allowable alignment tolerance for both the optimal dimensions and for the maximum cut width. The next section demonstrates another novelty of this design that arises out of this alignment tolerance; that nanometer-alignment can be achieved at the micrometer-scale.

3.4.2 Translating Nanometer-Alignment to the Micrometer-Scale

In this three level process, there are two translational alignments required: horizontal and vertical alignment of the oxide cut, and horizontal and vertical alignment of the connecting wires. The symmetry of the system eliminates the need to vertically align the connecting wires assuming they are sufficiently long. This implies that the only vertical alignment necessary is that of the oxide cut. The previously defined vertical displacement tolerance, VD, represents the maximum vertical alignment tolerance of the cut to the nanowires before microwire (m_i) would no longer connect nanowire (n_i) but rather nanowire ($n_{i\pm1}$), therefore:

$$Cut\ Alignment\ Tolerance = s_1 + s_2 \tan f - \frac{w_c}{\cos f} \qquad \textit{Equation 3.5}$$

Fortunately, assuming the oxide cut will intersect each of the nanowires, any misalignment of the cut can be compensated for during alignment of the connecting wires. This would effectively eliminate any critical limitation on the translational alignment of the oxide cut. In this process, the connecting wire mask would be aligned to the oxide cut mask. Since the symmetry of the system eliminated any vertical alignment of the connecting wires, only a horizontal alignment is necessary. The previously defined horizontal displacement tolerance, HD, represents the maximum horizontal alignment tolerance of the connecting wires to the oxide cut before microwire (m_i) would no longer connect nanowire (n_i) but rather nanowire ($n_{i\pm1}$), therefore:

$$Connecting\ Wire\ Alignment\ Tolerance = s_2 + \frac{s_1}{\tan f} - \frac{w_c}{\sin f} \qquad \textit{Equation 3.6}$$

Thus, as long as the connecting wires can be aligned within this tolerance, deterministic or target connectivity is achievable. The impact of this is significantly different depending upon the application of the structure: fanout from the nano- to the microworld ($\phi < 5^o$) or nanowire interconnect ($\phi \approx 45^o$). This is illustrated in Figure 3.17 in which the connecting wire alignment tolerance is plotted as a function of the insulator cut angle, ϕ.

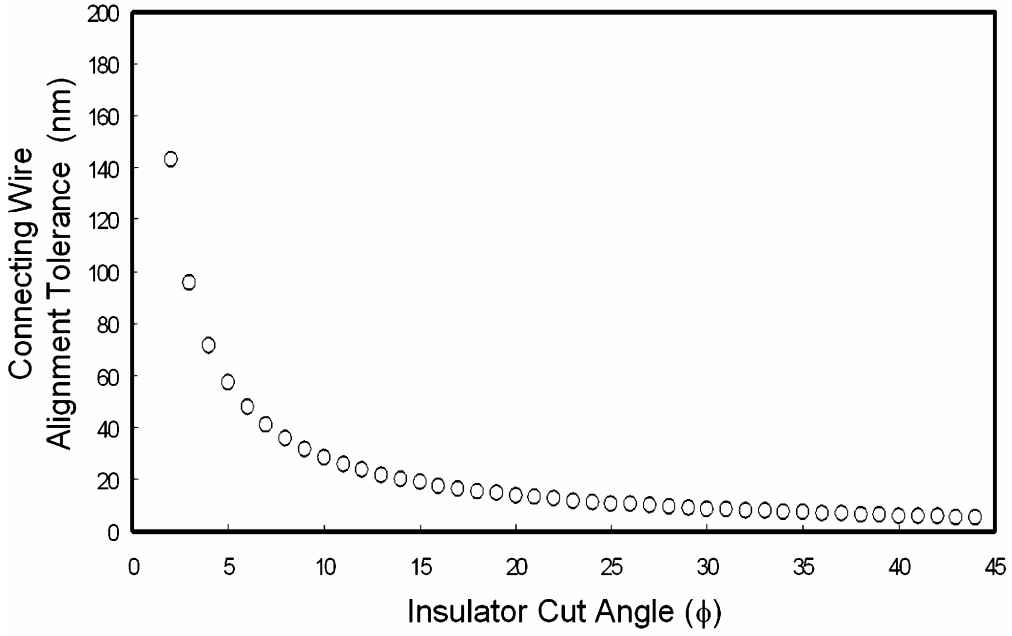


Figure 3.17: Connecting Wire Alignment Tolerance for Deterministic Connectivity vs. Insulator Cut Angle

The allowable tolerance is very small for nanowire interconnect applications. Thus, a predetermined connectivity may not be achievable, but complete connectivity can still be guaranteed through the padding of additional wires, as discussed in previous sections. Alternatively, the connecting wire alignment tolerance becomes very large for fanout applications. In fact, the connecting wire alignment tolerance is generally on the order of the connecting wire pitch, s_2+w_2. This implies that connecting micrometer-scale

wires to target nanowires requires only a micrometer-scale precision alignment. For example, connecting 10nm wires directly to 3μm wires separated by about 3μm would only require translational alignment precision to within about 6μm. Thus, for fanout applications it is possible to guarantee both complete *and* deterministic connectivity. This represents another significant feature of this design; 'nano-alignment' can be achieved at the micrometer-scale. This is a very powerful concept that permits target nanowires to be connected to target microwires with only a micrometer-scale alignment.

In this section, the limits on the alignment have been derived, a target alignment has been identified, and a novelty of this structure that permits nano-alignment at the micrometer-scale was presented. Thus, it has been shown that complete connectivity can be guaranteed for both fanout and nanowire interconnect, and deterministic connectivity can be guaranteed for fanout applications without the need of any critical translational alignment. However, this is predicated on the ability to fabricate the wires and oxide cut at target dimensions. The next section considers the affects potential fabrication errors can have on the connectivity of the system.

3.5 Potential Fabrication Errors

In this section, several potential fabrication errors are considered and their effects on the system connectivity are derived. In particular, processing issues that result in offsets from the target dimensions and rotational misalignment of both the insulator cut and the connecting wires are discussed.

3.5.1 Offsets from the Targeted Optimal Dimensions

Deviation from the targeted optimal dimensions of the system can result from over or under development, difficulty in opening up thin insulator cuts, wet etches, lateral components to directional etches, or even descum processes. Their effects on the system connectivity are analyzed from the top-down, starting with offsets from the optimal connecting wire pitch.

3.5.1.1 Offsets from the Optimal Connecting Wire Width and Spacing

Typical processing errors that would result in non-optimal connecting wire dimensions would not change the total connecting wire pitch, but rather the distribution of that pitch into the wire width and spacing. Thus, the sum of $s_2 + w_2$ would remain the same, but the individual components would change. Both the optimal connecting wire width and spacing were derived in Equation 3.3. Recall that two new variables were defined to derive this optimal pitch, c_2 and g_2. c_2 was the width of a vertical wire that would contact the horizontal wire over the entire cut opening. g_2 was the width at which a vertical wire could completely miss the cut. The optimal vertical wire width, w_2, was set equal to g_2, and the optimal vertical wire spacing, s_2, was set equal to c_2. To explore how any deviation from these values affects the connectivity of the system, a probability analysis is performed based on the discrete alignment system depicted in Figure 3.18.

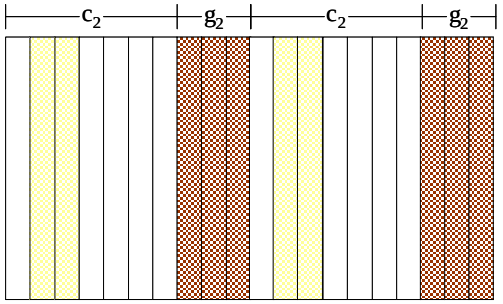


Figure 3.18: Discrete Alignment System

In this figure, two full pitches are shown and each pitch contains ten discrete alignment blocks. Seven (minus two yellow blocks) of those blocks are white and represent c_2. Three of the blocks are brown and represent g_2. If the vertical wire aligns in c_2, it will connect to an underlying horizontal wire. If the wire aligns in g_2, there will be no connection to the underlying horizontal wire. The yellow transparent blocks represent the actual (potentially non-optimal) vertical wire. So in this example, the optimal wire width, g_2, is three blocks, while the actual fabricated wire width, in yellow, is only two blocks, w_2.

To study the effect of non-optimal vertical wire widths, the yellow window representing the actual vertical wire is shifted across the full pitch, and the connectivity based on each resulting alignment is recorded. Continuing with the example, the alignment shown results in a connection since the wire aligns in the c_2 region. If the wire slides one spot to the left, there is still no effect on the connectivity of the system. However, if the wire slides several blocks to the right, there are two distinct alignments such that the fabricated vertical wire (yellow blocks) will fall completely in g_2, and thus not connect to the horizontal wire. Thus two of the possible ten alignments result in open systems. Notice that there is no possibility for a short since the actual fabricated wire is thinner than the optimal wire width, and so there is no way for one vertical wire to intersect multiple horizontal wires. This analysis is repeated for all of the potential vertical wire widths and the results are summarized in Table 3.1.

Table 3.1: Discrete Connection Probability

w_2	P_{short}	P_{open}
0	0	1
1	0/10	3/10
2	0/10	2/10
3	0/10	1/10
4	0/10	0/10
5	1/10	0/10
6	2/10	0/10
7	3/10	0/10
8	4/10	0/10
9	5/10	0/10
10	1	0

In this example, any fabricated wire width other than four blocks results in some probability that there will be either an open or a short. Clearly if the fabricated connecting wire has no physical width, the probability for an open is 100%. Similarly, if the fabricated wire width spans the entire vertical wire pitch, there is a 100% probability of a short. From this analysis, one can derive a piecewise discrete connection probability function, where Δx is the size of one alignment block:

$$P_{short} = \begin{bmatrix} 0 & w_2 = 0 & 1 \\ 0 & w_2 \le g_2 & \dfrac{g_2 - w_2 + \Delta x}{c_2 + g_2} \\ -\left(\dfrac{g_2 - w_2 + \Delta x}{c_2 + g_2}\right) & w_2 > g_2 & 0 \\ 1 & w_2 = c_2 + g_2 & 0 \end{bmatrix} = P_{open}$$

Recall that g_2 is the optimal w_2, and c_2 is the optimal s_2. Also consider that for a physical system, the actual vertical wire array can continuously align across the horizontal wire/oxide cut structure, so taking the limit as the block size approaches zero results in the following connection probability function:

$$P_{short} = \begin{bmatrix} 0 & w_2 = 0 & 1 \\ 0 & w_2 \le w_{2\_opt} & \dfrac{w_{2\_opt} - w_2}{s_2 + w_2} \\ \dfrac{-\left(w_{2\_opt} - w_2\right)}{s_2 + w_2} & w_2 > w_{2\_opt} & 0 \\ 1 & w_2 = s_2 + w_2 & 0 \end{bmatrix} = P_{open} \qquad \textit{Equation 3.7}$$

A graphical representation of this probability function is shown in Figure 3.19, in which the probability of a short or open is plotted versus the actual fabricated wire width.

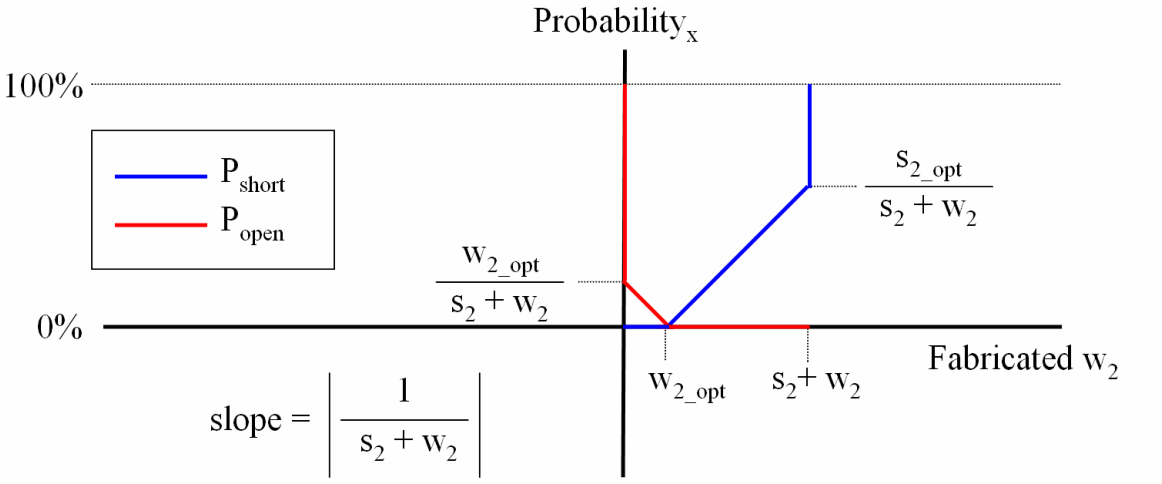


Figure 3.19: Connection Probability vs. Actual Fabricated Connecting Wire Width

Clearly if the fabricated wire width, w_2, is equal to the optimal wire width, there is no possibility for either an open or a short, which is the novelty of the design. It is also interesting that the probabilities for shorts and opens share a similar slope. This symmetry implies that there is no reason to bias the process towards over- or under-developing the structures. Deviation in either direction has the same overall impact on the connectivity. Unless that is, one considers an open worse or superior to a short, or if the optimal wire width makes up an overwhelmingly small or large percentage of the total pitch and there is little tolerance before a connectivity error.

The combination of this analysis with the novelty of the design is described in Appendix A.6. The next section describes how this analysis is affected by offsets in the target cut width.

3.5.1.2 Offsets from the Optimal Cut Width

The optimal cut width was derived in Equation 3.4 and is on the order of the nanowire dimensions. Accurately opening up very thin oxide trenches can be a challenging fabrication task. Consider the system in Figure 3.20 in which the actual fabricated cut width, indicated by red lines, is thinner than the target cut width, indicated in yellow as usual.

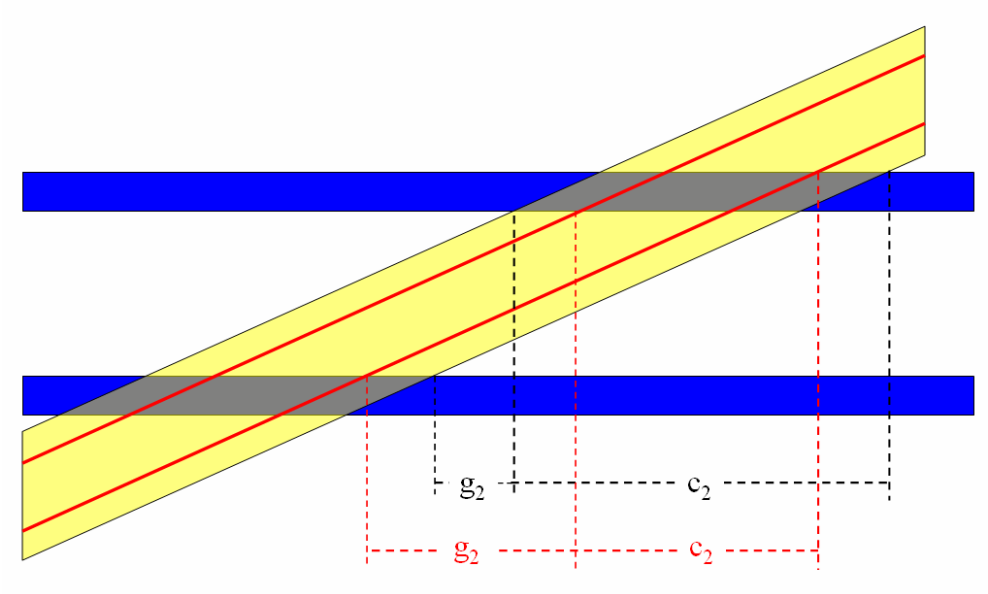


Figure 3.20: Non-Optimal Cut Width

As long as the cut angle does not change, the total vertical wire pitch ($s_2 + w_2$) remains the same, as shown in Appendix A.7. However, the distribution of the pitch changes, since c_2 and g_2 are both dependent upon $w_c / \sin \phi$. As the cut width decreases, the target optimal wire width increases while the target optimal spacing decreases. This affects the connection probability function since it is dependent upon these dimensions. Figure 3.21 shows a connection probability function for a system in which the cut width is fabricated thinner than targeted.

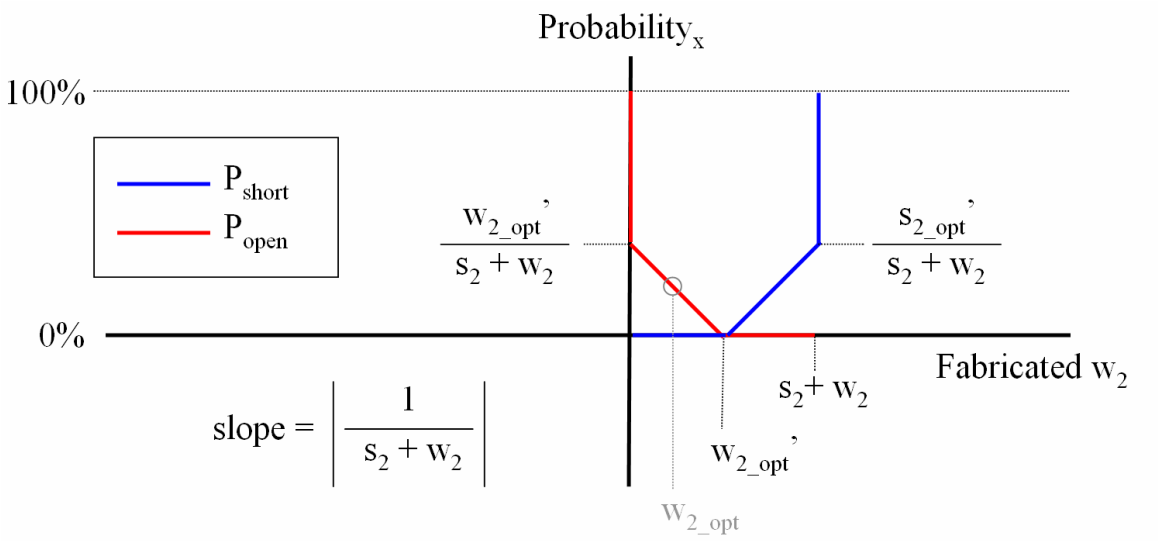


Figure 3.21: Connection Probability vs. Actual Fabricated Connecting Wire Width for Non-Optimal Cut Width

In this example, the optimal vertical wire width and spacing have changed. The new target dimensions are indicated as w_{2_opt}' and s_{2_opt}'. The problem arises in that the vertical wire width on the mask is still targeting the original w_{2_opt}, and so even if the vertical wires are fabricated 'perfectly' as designed, there will exist some probability for an open. Of course any deviation in the fabricated vertical wire width will combine with any deviation in the cut width. This implies that the two errors could potentially compound or offset. Suppose for example that the cut width was fabricated too thin but the vertical wires were fabricated too wide. These errors would work to offset each other and the novelty of the design could be exploited if the new vertical wire width could be biased towards w_{2_opt}'. The next section considers the effect deviations from the targeted nanowire width and spacing would have on the connection probability function.

3.5.1.3 Offsets from the Designed Nanowire Width and Spacing

Any error in the fabrication of the nanowire array would not likely change the total pitch, but rather the distribution of that pitch into the nanowire width and spacing. Recall from Equation 3.4 that the optimal vertical wire pitch is dependent upon the

nanowire width and spacing. Therefore, any deviation in these values would affect the connection probability function. This implies that a similar analysis to deviation in the optimal cut width can be made for fabrication errors in the nanowire array. Any deviation from the target nanowire width and spacing changes the target vertical wire dimensions. Offsets in the target nanowire dimensions combine with both offsets in the optimal cut width and offsets in the optimal vertical wire dimensions.

3.5.1.4 Alignment Dependence Connectivity in Non-Optimal Systems

It was shown in the previous sections that for non-optimal systems, there is a probability for either opens or shorts. In this section, several non-optimal systems are considered which demonstrate that this probability is alignment dependent, and therefore impacts fanout systems differently than nanowire interconnect. Figure 3.22 shows a system in which the vertical connecting wires were fabricated larger than targeted.

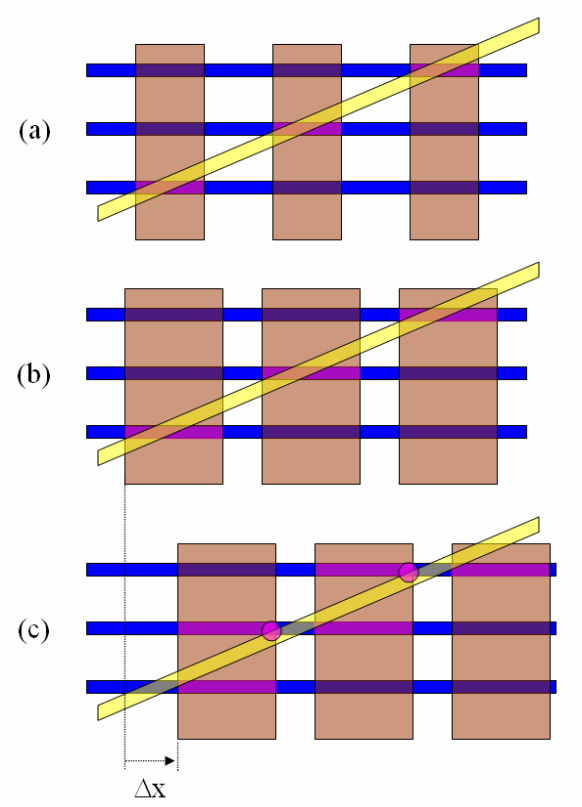


Figure 3.22: Shorting in a Non-Optimal System. (a) System with optimal connecting wire dimensions; (b) system with wider connecting wires but with correct connectivity and (c) system with wider connecting wires with an alignment that results in shorting

Figure 3.22a shows a system with the optimal connecting wire dimensions. There is no critical restriction on the translational alignment, thus the novelty of the design. In the second system, the connecting wires were fabricated wider than targeted, which from Equation 3.7 would suggest that there is some probability for shorting. However, in spite of these non-optimal dimensions, the depicted alignment still results in a properly connected system. In the final system, this alignment has shifted Δx and effectively shorted the entire structure. Each vertical wire connects two horizontal wires and similarly, each horizontal wire is connecting multiple vertical wires in a step-like fashion such that the entire structure is shorted. Thus, the probability for opens or shorts defined by Equation 3.7 implies the entire system is shorted or left open and that probability is

dependent upon the alignment. Figure 3.23 demonstrates a system that is left completely open from vertical wires that were fabricated thinner than targeted.

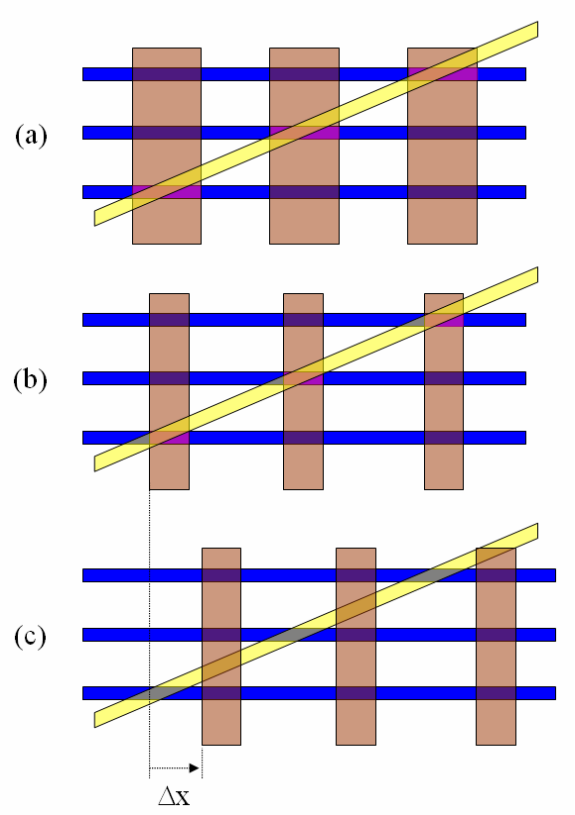


Figure 3.23: Unconnected Non-Optimal System. (a) System with optimal connecting wire dimensions; (b) system with thinner connecting wires but with correct connectivity and (c) system with thinner connecting wires with an alignment that leaves the structure completely unconnected

Examples of systems in which connectivity errors arise from offsets in the designed cut width or nanowires dimensions are demonstrated in Appendix A.8. The connectivity of these systems is still dependent upon the alignment of the vertical connecting wires. The impact of these connectivity errors is different for fanout systems than for nanowire interconnect. Consider a fanout system in which the target 3µm connecting wires were actually fabricated to be 3.3µm wide. From Equation 3.7, this would result in a 5% chance of a system short. Fortunately, when fanning out from the

nano- to the microworld, it was shown that the alignment tolerance is on the order of the connecting wire pitch. In this example, there would still exist a 5.7μm alignment window to avoid shorts. Thus, these errors have minimal impact on fanout applications since the alignment tolerance is very large, and the percentage error would be relatively small. For nanowire interconnect applications however, these probabilities could surface as yield hits.

All of the cuts in this section were made at the target cut angle derived in Equation 3.2. Similarly, the vertical connecting wires were fabricated perfectly perpendicular to the horizontal nanowires. The next section considers the effect any rotational misalignment would have on the connectivity of the system.

3.5.2 Rotational Misalignment

Another potential fabrication error that must be considered is the effect of rotational misalignment on the system. Although the novelty of the design eliminates any critical translational alignment; rotational alignment of the insulator cut, Figure 3.24a, and the perpendicular connecting wires, Figure 3.24b, is still necessary.

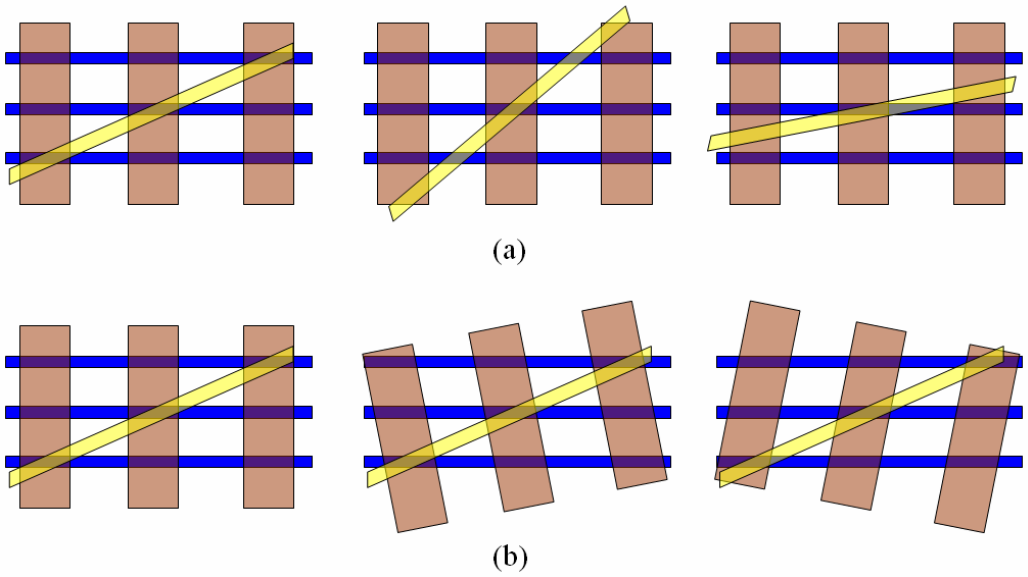


Figure 3.24: Rotational Misalignment (a) of the insulator cut, and (b) connecting wires

The next section investigates the connectivity effects of rotational misalignment from the target insulator cut angle defined by Equation 3.2.

3.5.2.1 Rotational Misalignment of the Insulator Cut

Figure 3.25 demonstrates two systems in which rotational misalignment of the insulator cut results in connectivity errors.

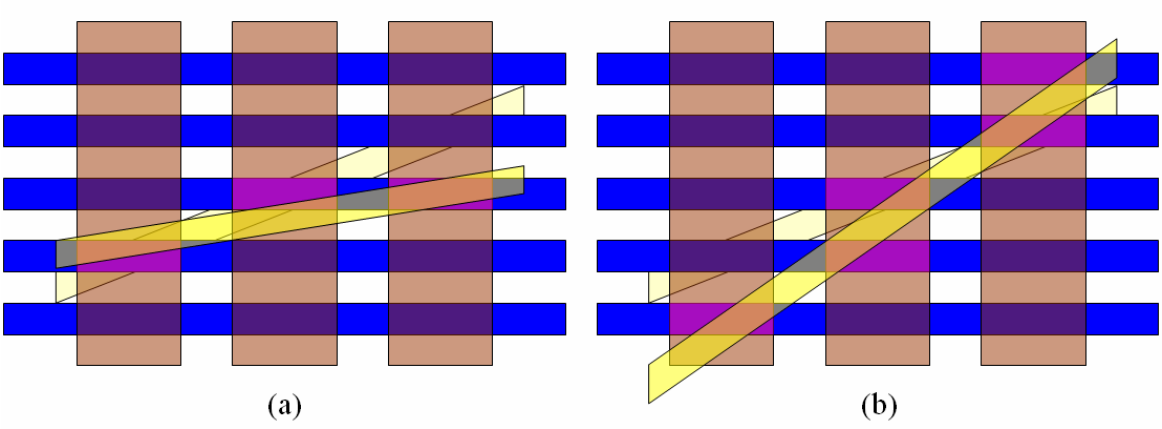


Figure 3.25: Examples of Systems with Rotational Misalignment of the Insulator Cut. The cut is fabricated at an angle (a) less than or (b) greater than the target angle.

The cut in the left system is made at an angle smaller than the target cut angle and results in redundancy in the vertical wires. The limit of this type of misalignment would be a horizontal cut that would intersect only one horizontal wire; effectively shorting all vertical wires together. The cut in the right system is larger than the target cut angle and results in redundancy in the horizontal wires. The limit of this type of error would be a vertical cut that would intersect only one vertical wire; effectively shorting all horizontal wires together. In between these limits exists a system in which the first open or short is about to occur. It is at this point that the tolerable rotational misalignment of the system is defined.

Stating that there is a rotational misalignment implies that there is a point at which the cut is rotated about. For this analysis, the point of rotation is assumed to be at the

corner of the structure. Implications from this assumption are discussed in Appendix A.9. The further from the point of rotation, the larger the equivalent translational offset becomes for a change in angle. This implies that under certain assumptions on the location of this point, any errors that occur from a rotational misalignment will occur first at the junctions farthest away from the point of rotation. This concept is demonstrated in Figure 3.26.

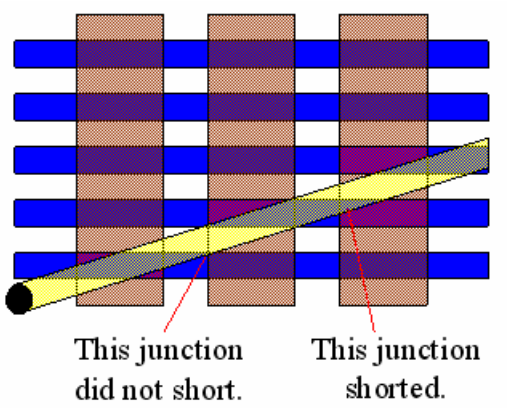


Figure 3.26: Junctions Furthest from the Point of Rotation are the Limiting Case

Thus, it is important to analyze the junctions furthest from the point of rotation in determining the limitation on the allowable rotational misalignment. To accomplish this, both types of errors must be considered; shorts and opens, as depicted in Figure 3.27.

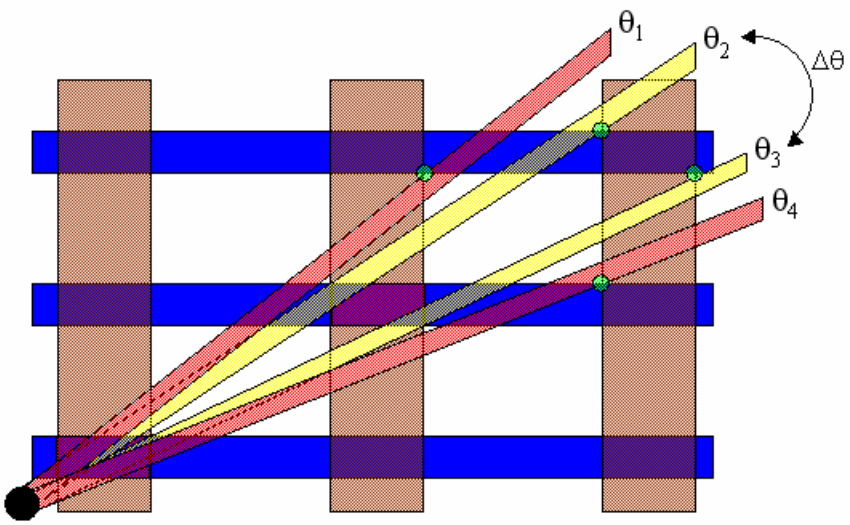


Figure 3.27: Example of a System in which Avoiding an Open Limits the Tolerable Rotational Misalignment

In this figure, the yellow cuts are at angles on the border of connecting the last junction. That is, the insulator cut angle has to be within θ_2 and θ_3 to avoid leaving the last top-right junction open. The red cuts are at angles on the border of connecting non-target junctions. That is, if the cut angle is larger than θ_1, it will connect the middle vertical wire with the top horizontal wire. If the cut angle is any smaller than θ_4, it will connect the right vertical wire with the middle horizontal wire. Clearly in this system, the cut would leave the last junction open before it would connect the non-target junctions, since θ_2 and θ_3 are a subset of angles θ_1 and θ_4. Therefore, in this example, avoiding an open limits the tolerable rotational misalignment of the cut. Figure 3.28 presents an alternate system in which avoiding the connection of non-target junctions is the limiting angle.

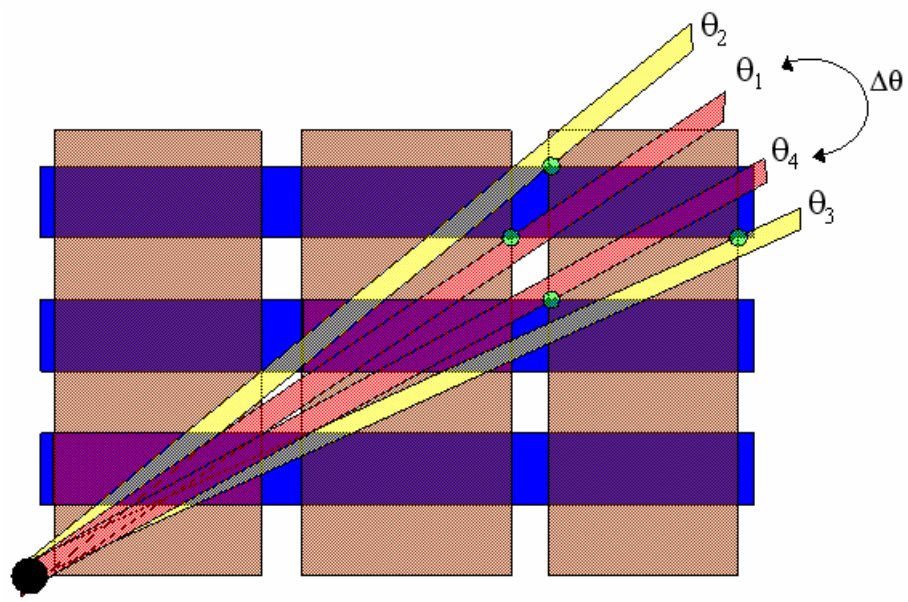


Figure 3.28: Example of a System in which Avoiding Connection to Non-Target Junctions Limits the Tolerable Rotational Misalignment

In this example, a larger percentage of the vertical wire pitch was distributed into the wire width. Now θ_1 and θ_4 are limiting the allowable rotational misalignment. Any increase past these angles results in connecting non-target junctions. Thus, to understand the connectivity effects of rotational misalignment of the insulator cut, the conditions in which shorts and opens first occur must be determined. This requires the derivation of the four angles defined in the above examples. This analysis was performed and is included in Appendix A.9. However, this is not the only rotational misalignment that must be considered. Any non-orthogonality in the connecting wire array can also lead to connectivity errors and is considered in the next section.

3.5.2.2 Rotational Misalignment of the Vertical Wires

Figure 3.29 demonstrates a system in which rotational misalignment of the vertical wires results in a connectivity error.

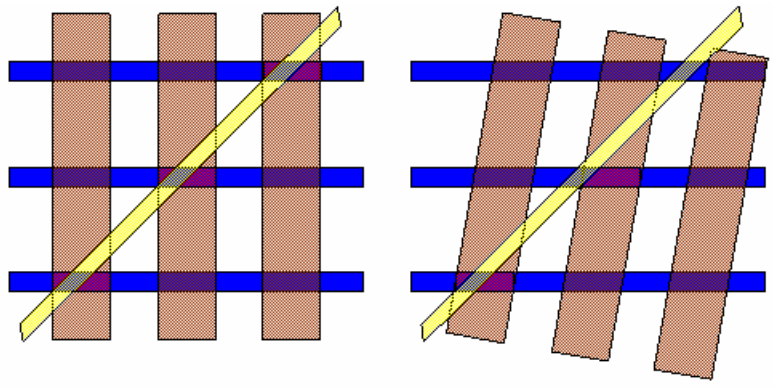


Figure 3.29: Rotational Misalignment of the Vertical Wires

In this system, the top right junction is left open. As with rotational misalignment of the insulator cut, the rotational misalignment of the vertical wires in which a connectivity error first occurs must be derived. The first step in such an analysis is defining the equivalent vertical wire pitch caused by this rotational misalignment. This involves calculating the projection of the vertical wire and spacing onto the horizontal nanowire axis, as demonstrated in Figure 3.30.

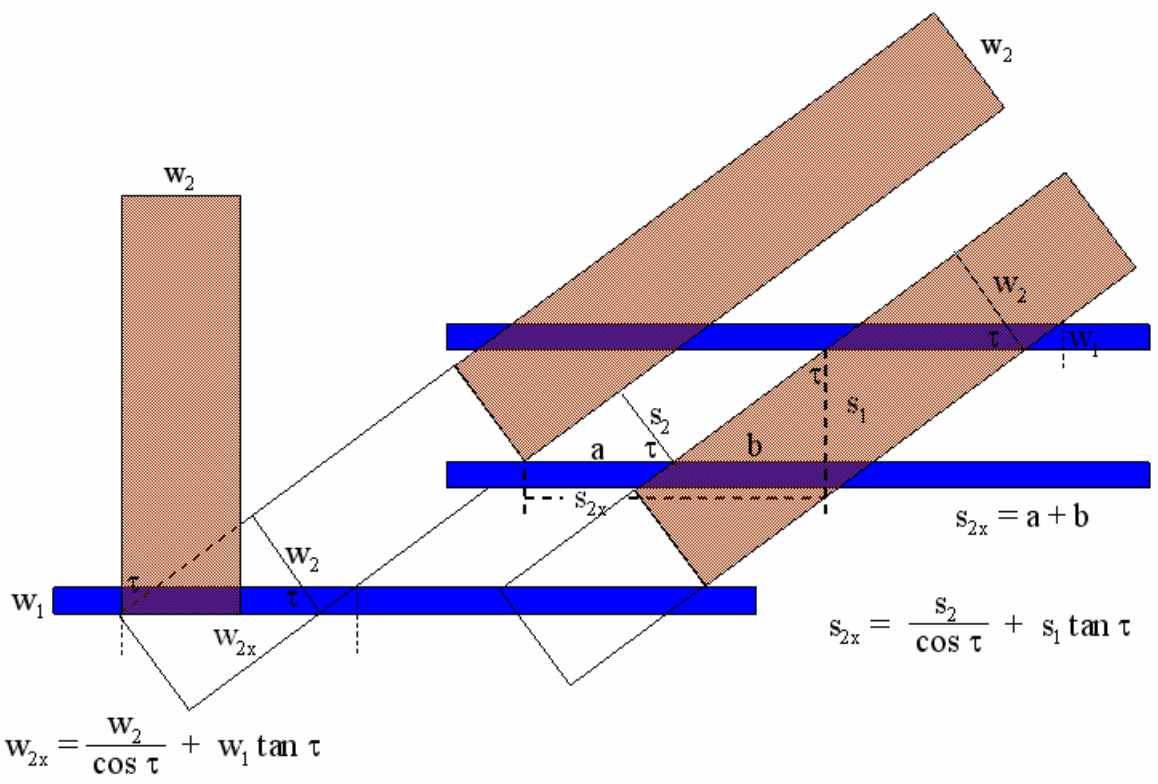


Figure 3.30: Deriving the Equivalent Vertical Wire Pitch

In this figure, angular deviation from 90^o, or completely orthogonal connecting wires, is denoted by tau, τ. The equivalent vertical wire width is derived:

$w_{2x} = w_2 / \cos \tau + w_1 \tan \tau$

The equivalent vertical wire spacing is derived:

$s_{2x} = s_2 / \cos \tau + s_1 \tan \tau$

Notice that for non-perpendicular connecting wires, the new equivalent vertical wire pitch is not equal to the original pitch. This is how the top-right junction was left open in the previous example, which is repeated in Figure 3.31 with the equivalent vertical wire pitch superimposed in gray.

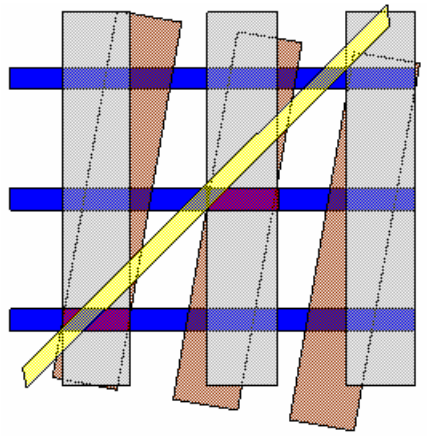


Figure 3.31: Example System with Superimposed Equivalent Vertical Wire Pitch

The rotational misalignment of the vertical wires caused an increase in the equivalent vertical wire pitch. This increase in the pitch resulted in the cut missing the top-right junction. Notice the similarity of this figure to Figure 3.27, in which the connectivity errors that could arise from a rotational misalignment of the cut were identified. The cut in this figure resembles the cut made at an angle θ_2 in Figure 3.27, only considering the equivalent vertical wire pitch rather than the original pitch.

Rotational misalignment of the vertical wires can be in the direction of the cut, as illustrated in the previous example, or alternatively it can be in the direction opposite the cut, as shown in Figure 3.32.

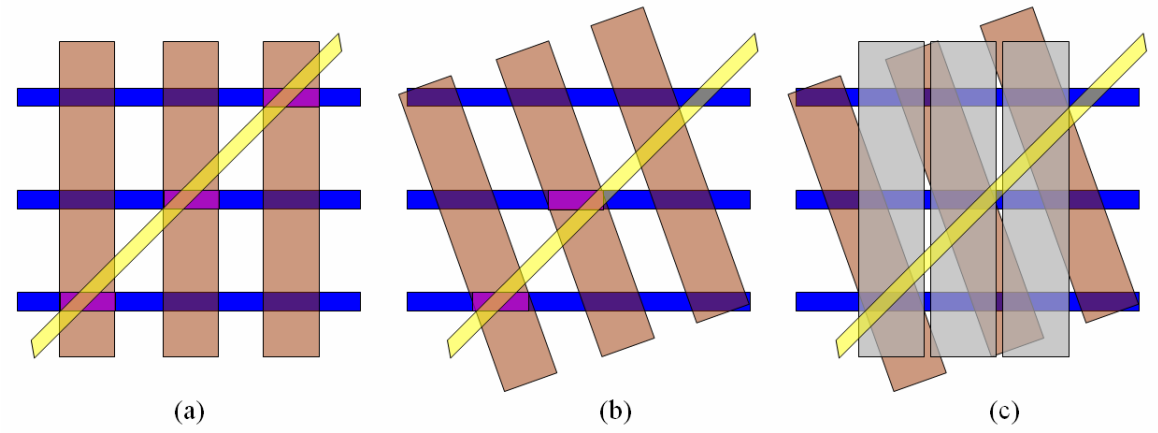


Figure 3.32: Example System of Vertical Wires Rotationally Misaligned in the Direction Opposite the Cut. (a) Initial system, (b) Rotational misalignment of the vertical wires, (c) Superimposed Equivalent Vertical Wire Pitch

The rotational misalignment of the vertical wires in the direction opposite the cut caused a decrease in the equivalent vertical wire pitch. This decrease in the pitch resulted in the cut missing the top-right junction. Once again notice the similarity of this figure to Figure 3.27, in which the cut in this figure resembles the cut made at an angle θ_3. It turns out that a similar analysis to rotational misalignment of the cut can be performed for rotational misalignment of the vertical wires only using the equivalent vertical wire pitch. The conditions in which rotational misalignment of the connecting wires first causes an open or short in the system are derived. This analysis can be found in Appendix A.10 and from it, the tolerable rotational misalignment of the vertical wires was derived. A summary of the results of this analysis, as well as the results from analyzing the rotational misalignment of the insulator cut, is given in the next section.

3.5.2.3 Connectivity Dependence on Rotational Misalignment

The insulator cut should be made at the angle ϕ derived in Equation 3.2, and the vertical connecting wires should be made perpendicular to the nanowires. To analyze the impact of deviation from these angles, the conditions in which a single open or short first

occurs was derived for both rotational misalignments. Angular offset from the target cut angle is denoted by θ, whereas angular offset from perpendicular connecting wires is denoted by τ. A summary of the results can be seen in Figure 3.33, which compares the tolerable rotational misalignment before a single open or short occurs for both θ and τ for various cut angles to achieve a desired system size. . The system size is defined as the number of nano- to microwire connections.

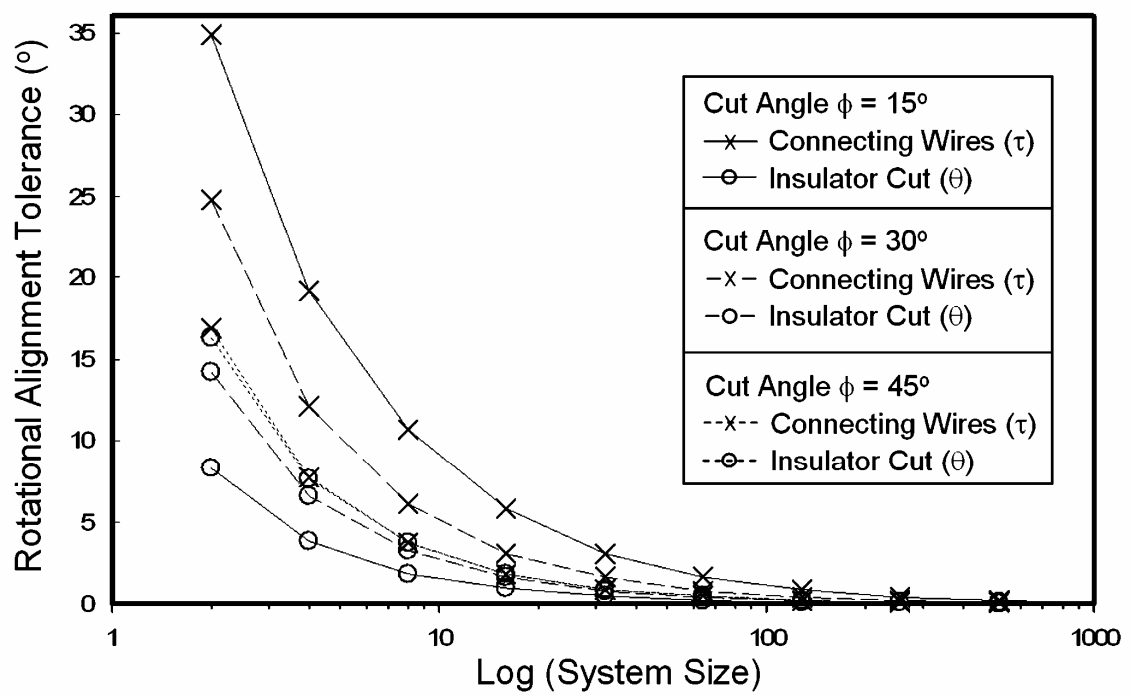


Figure 3.33: Rotational Misalignment Tolerance vs. Log (System Size)

As expected, the rotational misalignment tolerance falls off with increasing system size. At smaller cut angles, i.e. fanout applications, there is significantly more tolerance for rotational misalignment of the connecting wires than there is for rotational misalignment of the insulator cut. As one approaches nanowire interconnect applications, $\theta = 45^{o}$, the two cases converge. Thus, the best case for rotational misalignment of the cut is only equal to the worst case for rotational misalignment of the connecting wires. This implies that the cut rotational alignment is more critical, and represents the greater

limitation to the scalability of this structure. Fortunately, using alignment marks placed towards the edge of large wafers, relatively precise rotational alignment can be achieved.

In this section, the impact of offsets from the target optimal dimensions was analyzed and shown to result in a probability for a completely open or shorted system. This probability was alignment dependent and had little impact on fanout applications since the percentage error was be relatively small. However, for nanowire interconnect applications, these errors could surface as yield hits. The impact of rotational misalignment was then considered. The rotational misalignment tolerance before the first open or short occurred was derived for both offsets from the target cut angle as well as non-orthogonality in the connecting wires. These types of errors were found to limit the scalability of this design, as the tolerable rotational misalignment dropped off quickly with increasing system size. In the next section, an alternate process flow is presented to improve the scalability of this design.

3.6 Alternate Process Flow to Improve Scalability

In this section, an alternate process flow is presented that addresses many of the issues that were raised in previous sections. The first part of this section will set up the motivation behind designing an alternate process flow. In particular, this new design will eliminate the necessity of making an insulator cut. The process flow will be presented and a comparison to the original process flow will be made. Any theoretical limitations to this new design will be addressed.

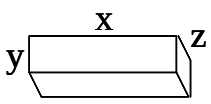
3.6.1 Motivation

Although it is possible to eliminate the translational components of the alignment, the rotational components are limiting the scalability of the structure. The larger the structure, the more restrictive rotational alignment becomes. Another concern is that the insulator cut width can be on the order of the critical dimension. Opening up very small trenches can be very challenging. Ideally, all of the critical dimensions would be

fabricated at the same time. This would eliminate the need to perform two nanofabrication steps. It is with this motivation that the following process flow was developed, using multi-level nanoimprinting to self-align vias to the underlying nanowires.

3.6.2 Alternate Process Flow Using Multi-Level Imprinting

The major concept of the alternate process flow is to use multi-level imprinting to fabricate the nanowires and vias in the same imprint step and thus eliminate the insulator cut. In doing this, all critical dimensions are fabricated together and the vias are 'self-aligned' to the nanowires. The target dimensions for the vias are given in Figure 3.34.



Let $x = c_2$, $y = w_1$
z = to be solved experimentally

Figure 3.34: Via Dimensions for Alternate Process Flow

Following the optimal condition analysis presented previously, x is set equal to c_2 and y is set equal to w_1. The height of the vias will depend on the system variables as well as the material set used in fabricating these structures. Ideally it will balance the ease of imprinting with the requirement of electrical isolation between non-connecting wires. Opposite of the traditional via, where the top layer is brought down to the bottom layer, in this process the bottom layer is brought up to the top layer. The novelty is to build the vias into the imprint mask at a third depression level, as demonstrated in Figure 3.35.

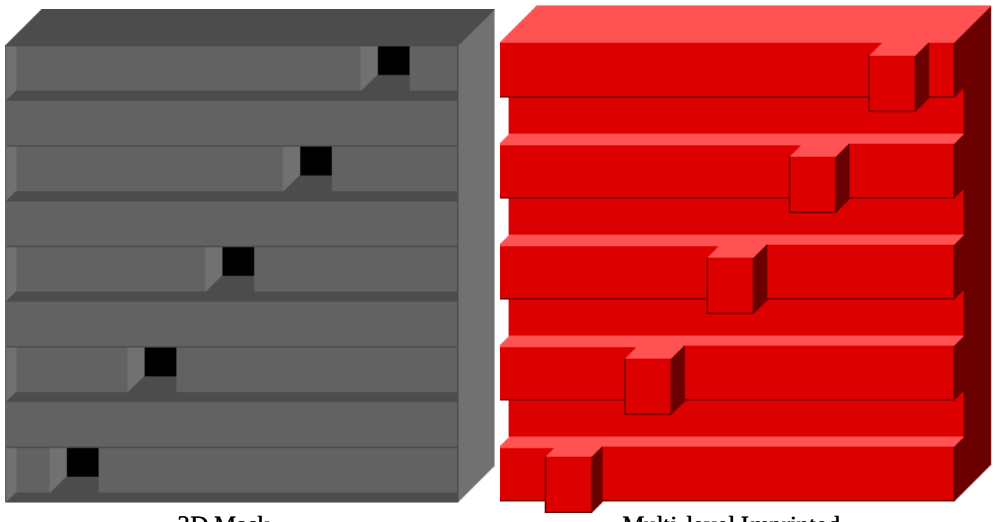


Figure 3.35: Multi-Level Mask and Imprint Pattern

A theoretical process flow is described in Figure 3.36 along with the accompanying 3D top view diagrams.

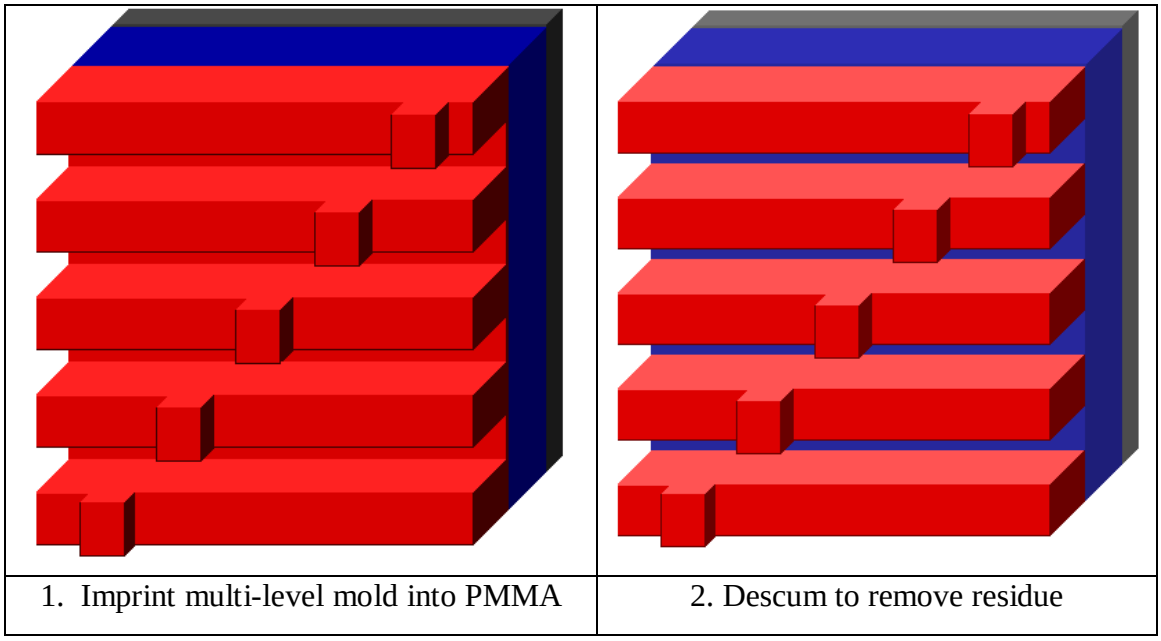
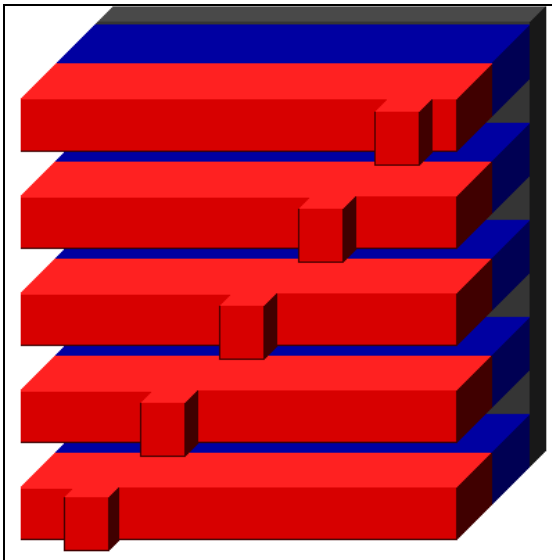
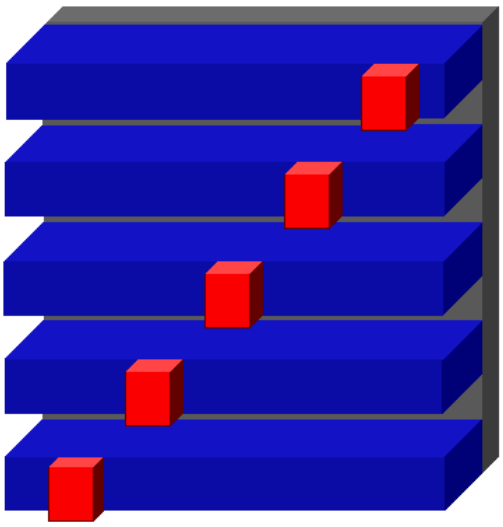


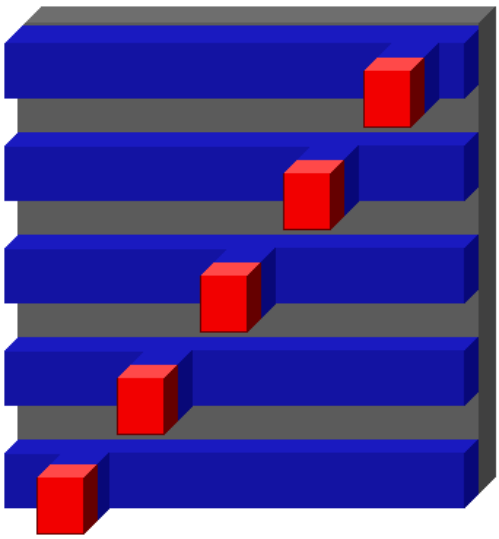
Figure 3.36: Alternate Process Flow



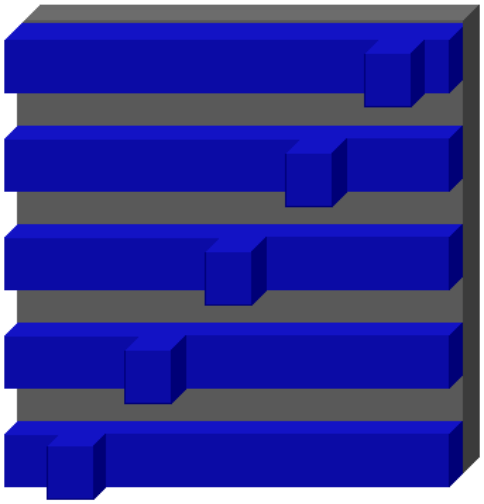
3. Selective directional etch of underlying material



4. Remove first level of PMMA

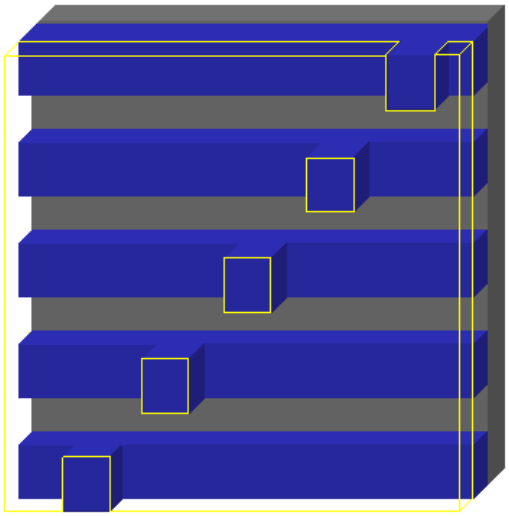


5. Partial directional etch of underlying material

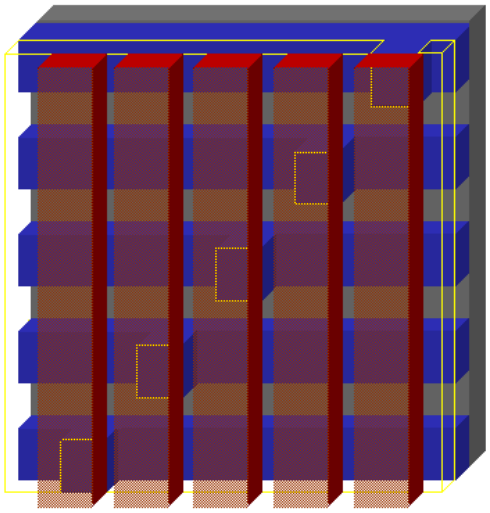


6. Remove remaining PMMA

Figure 3.36 (continued)



7. Apply dielectric



8. Fabricate connecting wires.

Figure 3.36 (continued)

The first step is to imprint the multi-level pattern into the PMMA. The mask has three levels; the base level (l_0) and then two additional levels (l_1,l_2) that will end up being the nanowires and the vias, respectively. The second step is to descum the residual l_0 resist. Typically some l_0 resist is left behind since pressing the mask too deep into the PMMA can lead to damage. The next step is to perform a dry etch on the underlying material creating the nanowire spacing, s_1. The fourth step is to remove the l_1 resist, thus exposing the nanowires everywhere except at the vias. A partial dry etch is then performed. This etch should be end-pointed by the desired nanowire thickness and should be thick enough so that a dielectric can isolate the nanowire array from the connecting wire array. The remaining l_2 resist is then removed exposing the vias. In the seventh step, a dielectric is applied and any polishing necessary to expose the vias is performed. Finally, the connecting wires are fabricated without any critical translational alignment. The final cross-sections are compared in Figure 3.37.

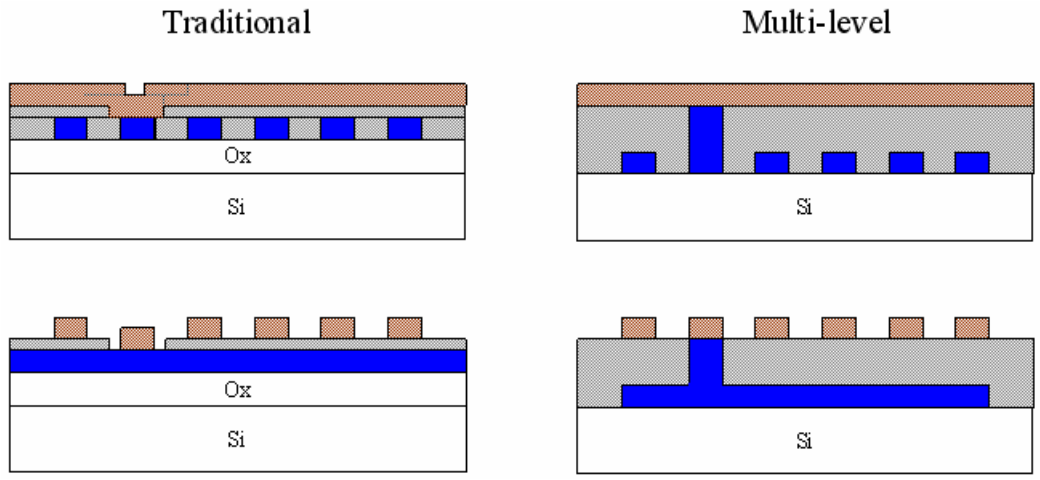


Figure 3.37: Comparing the Traditional Process with the Multi-Level Alternative

In the traditional process flow, the connecting wire fills down through the oxide cut to connect to the nanowire; while in the multi-level process, the bottom nanowire is built up to the connecting wire. There is no cut in this process and therefore there is no cut rotational alignment. In fact, an entire alignment step is eliminated from the traditional process flow. In addition, all critical dimensions are fabricated in the same nanofabrication step and the vias are 'self-aligned' to the nanowires. The contacts are present after the critical level is fabricated.

This process eliminates the insulator cut; however, rotational alignment of the vertical connecting wires is still required. While this alignment did limit the scalability of the design, it was not as strict as rotational misalignment of the insulator cut. As discussed in Appendix A.11, if the vias can be fabricated at non-traditional geometries, the alternate process flow can improve the tolerance to rotational misalignment of the vertical wires. In the next section, an actual proof-of-concept is fabricated and characterized, demonstrating the feasibility of this design for fanout and nanowire interconnect applications.

3.7 Proof-of-Concept Structure

The design, process flow, fabrication and characterization of proof-of-concept structures are presented in this section. The two wire arrays were uniquely connected, electrically isolated, and yielded wafer-scale.

3.7.1 Design and Fabrication

The layout for this design was created using Cadence Virtuoso and fabrication was performed at the NCSU Nanofabrication Facility (NNF). A typical layout of the structures is presented in Figure 3.38, along with the corresponding cross-section.

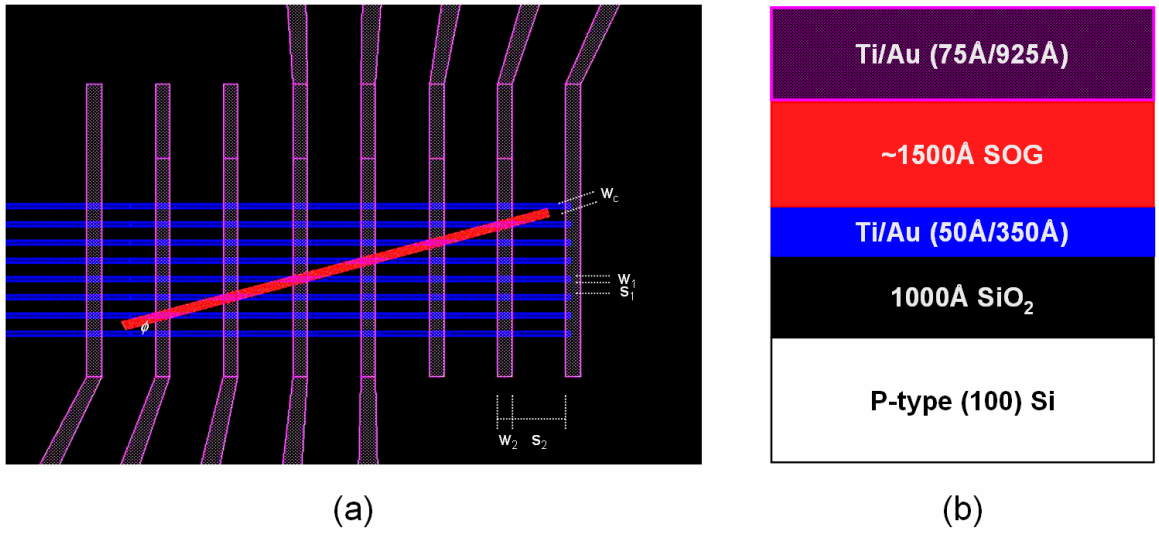


Figure 3.38: Structure Design (a) Layout, (b) Cross-Section

The size of the interconnect structures were 6x6, even though eight lines are drawn for both the horizontal and vertical wires. Two additional wires were used for each wire array to prevent errors caused by pattern density changes common in submicron lithography. Three different structures were designed, all with different system dimensions as shown in Table 3.2. 'Structure 1' had the smallest horizontal wire width at 600nm, which represented the smallest line size consistently reproducible in the stepper used for this fabrication. 'Structure 2' had the same horizontal wire pitch as 'Structure 1',

but had more of that pitch distributed into the wire width. In addition, the horizontal and vertical wire widths differed by only 0.2μm. 'Structure 3' had the largest features and had the smallest cut angle, more closely approximating fanout applications. While none of the structures represented any relatively extreme pitch reduction, the vertical wire pitch of the final structure was over four times the horizontal wire pitch.

Table 3.2: Proof-of-Concept Structure Dimensions

	Structure 1	Structure 2	Structure 3
w_1	0.6μ	0.8μ	1.2μ
s_1	1.5μ	1.3μ	1.7μ
ϕ	16.5^o	14.7^o	13.6^o
w_c	1μ	1μ	1.2μ
w_2	1.5μ	1μ	2μ
s_2	5.6μ	7μ	10μ

The structures were fabricated on top of a 1000 angstrom thick silicon dioxide film, thermally grown on a 4" (100) p-type, 1-10 ohm-cm silicon wafer. An i-Line GCA 800 DSW wafer stepper was used to pattern as thin as 600nm 'nanowires'. The wires were formed using a bilayer resist stack for lift-off patterning of a 350 angstrom layer of gold on top of a 50 angstrom adhesion layer of titanium. Honeywell Accuglass 111 Spin-On Glass was applied and then annealed at 300^oC to form a 1500 angstrom interlevel dielectric. The oxide cut was patterned, followed by an anisotropic reactive ion etch (RIE) of the underlying dielectric. Finally, the connecting wires were fabricated by depositing 75 angstroms of titanium and 925 angstroms of gold, once again patterned using a liftoff process. Shown in Table 3.3 is the detailed process flow for this fabrication.

Table 3.3: Process Flow Traveler for Fabrication of Proof-of-Concept Structures

Step	Descritption
1	JTB-111 Clean (if needed)
2	Wet Thermal Oxidation (1000Å) 1000^{o}C Steam for 8 mins
3	Metal 1 Photolithography Solvent Clean (Acetone Soak – 1 min; Methanol Soak – 1 min) Dehydration Bake (115^{o}C for 5 mins) HMDS Spin (4000rpm for 40 secs) MicroChem LOR1A Spin (3000rpm for 40 secs; thickness: ~1200Å) Hardbake (150^{o}C for 10 mins) Shipley 510A Spin (4000rpm for 40 secs; thickness: ~10,000Å) Softbake (90^{o}C for 1 min) Expose GCA Stepper (108mJ, 0.6 secs, focal point from FE Matrix) Post-Exposure Bake (115^{o}C for 1 min) Develop MF-319 for 60 secs
4	Metal 1 Evaporation – E-Beam 50Å Ti 350Å Au
5	Metal 1 Liftoff Soak and Spray with n-methyl-pyrrolidone Sonicate for 15 secs
6	Inter-level Dielectric Deposition Dehydration Bake (115^{o}C for 5 mins) Honeywell Accuglass T-11 111 Spin-On-Glass (4000rpm for 40 secs) Pre-Cure (90^{o}C for 1 min) Cure (280^{o}C for ~3 hours)

Table 3.3 (continued)

7	Insulator Cut Photolithography Solvent Clean (Acetone Soak – 1 min; Methanol Soak – 1 min) Dehydration Bake (115^{o}C for 5 mins) HMDS Spin (4000rpm for 40 secs) Shipley 510A Spin (4000rpm for 40 secs; thickness: ~10,000Å) Softbake (90^{o}C for 1 min) Expose in GCA Stepper (108mJ, 0.6 secs, focal point from FE Matrix) Post-Exposure Bake (115^{o}C for 1 min) Develop MF-319 for 60 secs
8	Reactive Ion Etch Parameters: 60mTorr, CHF_3 – 20sccm, O_2 – 5sccm, 5 mins From monitor wafers: ~350Å/min Microposit 1165 soak for 10 mins (Strip Photoresist)
9	Metal 2 Photolithography Solvent Clean (Acetone Soak – 1 min; Methanol Soak – 1 min) Dehydration Bake (115^{o}C for 5 mins) HMDS Spin (4000rpm for 40 secs) MicroChem LOR5A Spin (3000rpm for 40 secs; thickness: ~5500Å) Hardbake (150^{o}C for 10 mins) Shipley 510A Spin (4000rpm for 40 secs; thickness: ~10,000Å) Softbake (90^{o}C for 1 min) Expose GCA Stepper (108mJ, 0.6 secs, focal point from FE Matrix) Post-Exposure Bake (115^{o}C for 1 min) Develop MF-319 for 60 secs
10	Contact Preparation O_2 Plasma Descum (600mT, 300W, 60 sccm O_2, 90s)

Table 3.3 (continued)

11	Metal 2 Evaporation – E-Beam 75Å Ti 925Å Au
12	Metal 2 Liftoff Soak and Spray with n-methyl-pyrrolidone Sonicate for 15 secs

The structures yielded wafer-scale; an example of which is shown in Figure 3.39. This image is of ‘Structure 3’ which had the largest dimensions and the smallest cut angle.

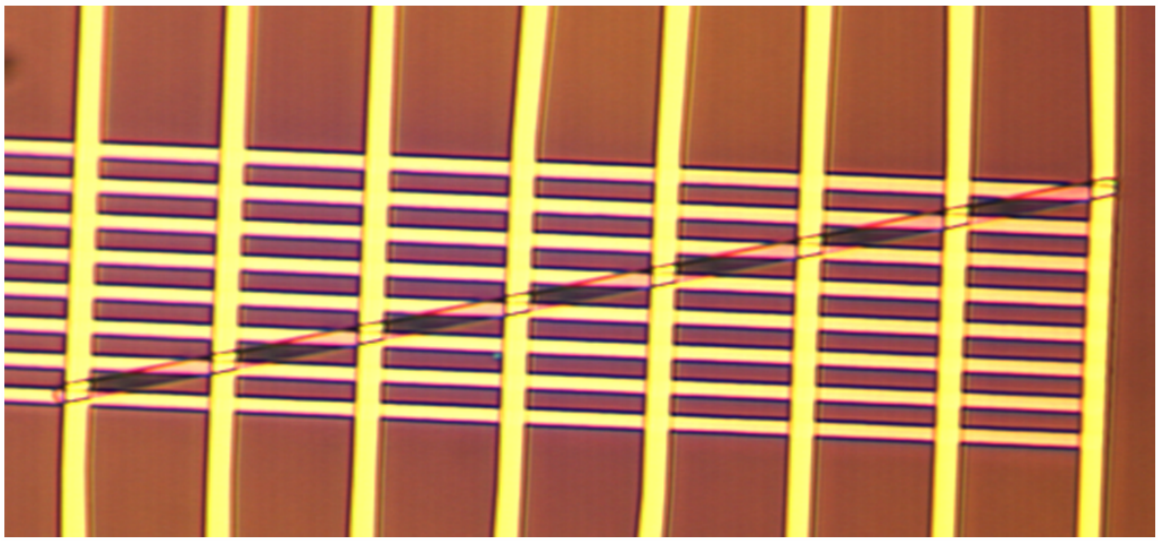


Figure 3.39: Image of Fabricated Structure 3

All of the dimensions were fabricated relatively close to the target dimensions. Therefore, it should be noted that it was a point of emphasis to only perform a coarse translational alignment in the stepper. This was done to help demonstrate the novelty of the design. From this figure it is apparent that each connecting wire connects one and

only one ‘nanowire’. This is further evidenced by the SEM of ‘Structure 1’, which had the smallest ‘nanowire’ width of 600nm, as shown in Figure 3.40.

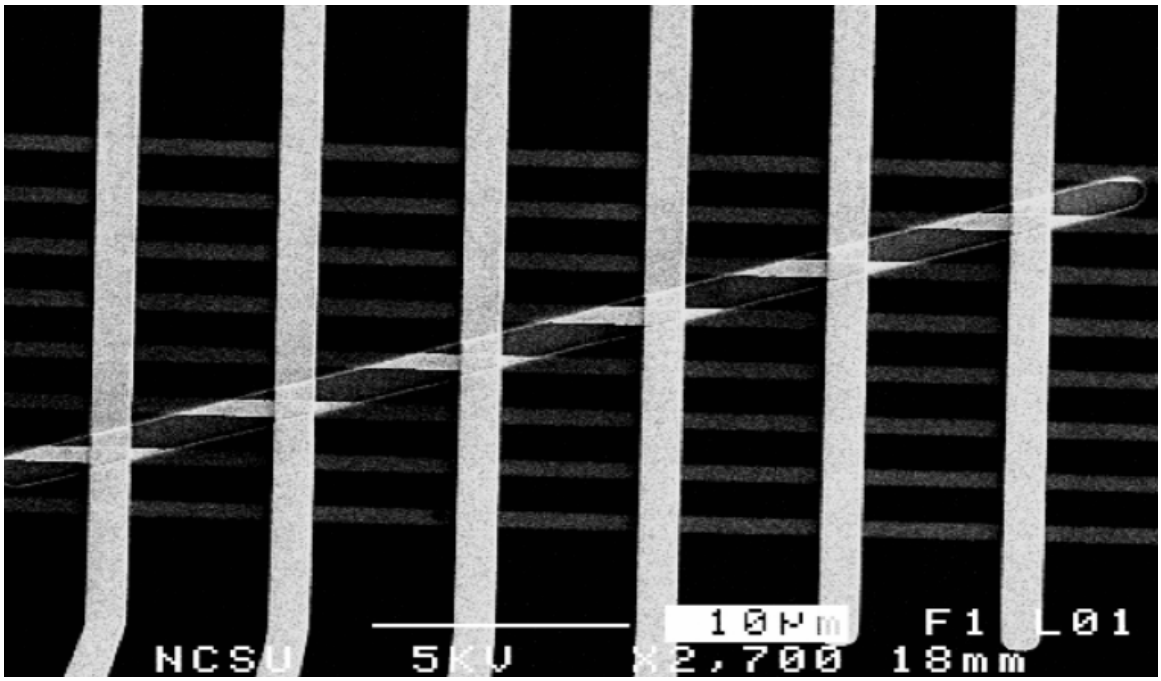


Figure 3.40: SEM of Fabricated Proof-of-Concept Structure

For this structure, it is obvious that the cut was fabricated wider than the targeted one micrometer. From the theoretical analysis, this error could result in the probability of a complete system short, depending upon the alignment. Clearly shorting did not occur in this structure, demonstrating the novelty of the design that the alignment window is large for fanout applications and therefore any deviation from the optimal dimensions has minimal impact on the connectivity since it represents a relatively small percentage of the alignment window. This demonstrates the robustness of the design. Clearly these images suggest unique connectivity; however electrical characterization is necessary to test the integrity of the oxide as well as the contacts.

3.7.2 Electrical Characterization

The current-voltage characteristics of the fabricated proof-of-concept structure are shown in Figure 3.41.

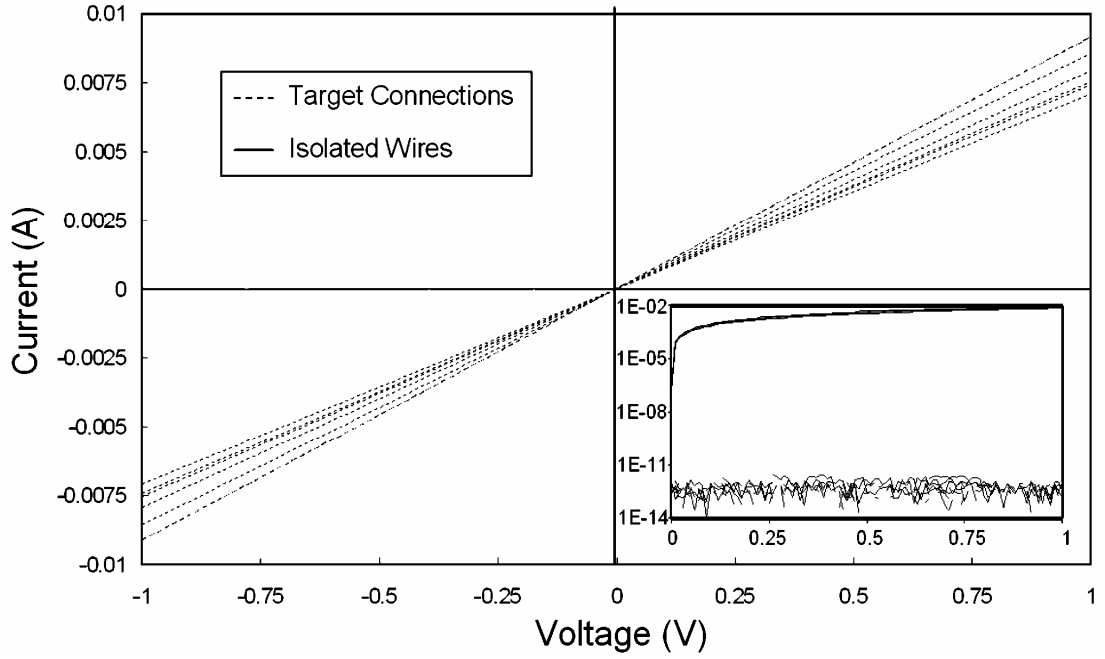


Figure 3.41: Electrical Characterization of Proof-of-Concept Structure

Target connections are made successfully while non-target connections remain electrically isolated. Clearly the oxide cut was completely opened, resulting in good ohmic contact between the two wire arrays. Conductivity differences between the target connections are caused by the wire resistance of the 'nanowires'. Due to the angle of the cut, the connections to each 'nanowire' are at different distances from the probe pads. The theoretical resistance calculated for wires of this thickness, length, and material set were in excellent agreement with the measured values. This analysis can be found in Appendix A.12. Overall, each intended connection resulted in ohmic contact; while each unintended connection remained electrically isolated, successfully demonstrating the fabrication of this proof-of-concept structure.

3.7.3 Scaling Considerations

Scaling the ‘nanowires’ into the nano-regime should have no theoretical impact on the design, thus allowing 600nm wires to be fabricated for the proof-of-concept structure. However, there are some practical issues that need to be considered as the nanowires are more aggressively scaled; the first of which is contact resistance. Clearly, the novelty of this design is such that a structure can result in which the connecting wires are only infinitesimally contacting the nanowires. This possibility is unavoidable, but as previously mentioned, it can be mitigated by targeting the center alignment, and thus the maximum contact area. In addition, ensuring that the insulator cut is completely opened is essential to reducing the contact resistance.

Another issue to consider when scaling to the nano-regime is any non-uniformity in the nanowire width. Oftentimes nanowires are fabricated with some degree of width and spacing non-uniformity [19], [20]. It is unlikely that this will have any significant impact on the connectivity of the structure, causing only random individual shorts or opens. Any full scale connectivity effects can be modeled using the probability analysis for non-optimal dimensions considering the average deviation caused by the imperfections in the nanowire fabrication.

Finally, it was stated that successful interface strategies require both physical connection to the nanoworld and retention of functional density. This latter requirement can often involve connecting a larger set of nanowires with a smaller set of microwires. Although not the goal of this dissertation, there is nothing intrinsic about this design that would prevent some form of decoding. An extension of this technique using multiple cuts with active elements at the cross points could accomplish decoding. A simpler solution would be to separate the pitch reduction from the decoding and program the latter into the nanowire crossbar fabric, as previously suggested [13].

3.8 Summary

In this chapter, the theory behind the nanowire fanout and interconnect structure was presented that permits complete and deterministic interconnect of orthogonal wiring arrays without the need for any critical translational alignment. Example systems were included to demonstrate this property and applications to nanotechnology were discussed. The optimal equations defining the system geometry to guarantee unique connectivity were derived. Two unique applications of this structure, fanout from nanowires to microwires and nanowire interconnect, were identified and are controlled by the choice of the insulator cut angle. Several distinctions based on these applications were made, including the ability to deterministically connect target nanowires and connecting wires. The alignment tolerance for deterministic connectivity was derived to be on the order of the connecting wire pitch. This implied that for nanowire interconnect, deterministic connectivity cannot be guaranteed without nanoprecision alignment; however, complete connectivity can still be guaranteed through the padding of additional wires. Alternatively, for fanout applications, deterministic connectivity was achievable since target nanowires could be connected to target microwires. This represents another significant novelty of this design, that nanoprecision alignment can be effectively translated to the micrometer-scale. Rather than mask alignment precision, the challenge of pitch reduction is shifted to the ability to fabricate structures at the micrometer-scale.

Several potential fabrication errors were then investigated. The connection probability function was derived for non-optimal dimensions. From this derivation, the probability for an open or short caused by any deviation in the optimal connecting wire width, cut width or nanowire dimensions could be calculated. Examples of systems with non-optimal dimensions revealed that these probabilities resulted in complete system shorts or opens, and was alignment dependent. This alignment dependency suggested a difference in how these errors impacted the design depending upon the application. For nanowire interconnect, these errors could surface as yield hits. For nanowire fanout, the alignment tolerance is very large, and the percentage error would be relatively small, thus having very little impact.

Rotational misalignment of both the insulator cut angle and the perpendicular connecting wires was then investigated. The conditions in which an error first occurred were derived for both cases. It was shown that the amount of rotational misalignment tolerance falls off quickly with increasing system size, limiting the scalability of the design. It turned out that the best case for rotational misalignment of the insulator cut was only equal to the worst case for rotational misalignment of the connecting wires. This implied that the cut rotational alignment is more critical, and represents the greater limitation to the scalability of this structure. An alternate process flow using multi-level imprinting was presented that eliminated this rotational alignment of the insulator cut. In this process, the cut is replaced with nanovias that are fabricated bottom-up to connect to the microwires, rather than the more traditional top-down approach. In addition, since the nanowires and vias are fabricated in the same level, this eliminates the need for multiple nanofabrication steps. The nanowires and nanovias are 'self-aligned' since they are fabricated together using multi-level imprinting.

A proof-of-concept structure using the traditional process flow was fabricated and characterized demonstrating the feasibility of this design. Target connections were made successfully while non-target connections remain electrically isolated. The smallest 'nanowires' that could be reproducibly fabricated were 600nm in width. Scaling the 'nanowires' into the nano-regime should have no theoretical impact on the design, thus allowing 600nm wires to be fabricated for the proof-of-concept structure. However, several practical issues to further scaling were identified and discussed. Overall, a design was presented, critically analyzed, and fabricated that permits complete and deterministic interfacing between the nanoworld and the microworld without the need for any critical translational alignment.

Chapter 4

Discontinuous Palladium Films

Discontinuous metal films have found great application in the field of nanotechnology. The versatility of these films is predicated on the ability to control their morphology. Inter-island spacing, particle diameter, uniformity and density are some of the critical properties of the film that determine their success for potential applications. Understanding the growth and controlling the morphology of discontinuous metal films has therefore become critical to the advancement of the many different areas of nanotechnology. Tailoring the film morphology of discontinuous palladium films for target applications such as molecular scaffolding, sensors, and non-volatile memory, is demonstrated in this chapter.

This chapter is organized as follows. In Section 4.1, the theory behind the formation of discontinuous metal films is outlined. Section 4.2 discusses the calibration of the E-beam evaporator as well the process to fabricate discontinuous palladium films. In Section 4.3 these films are engineered to function as a molecular scaffold in the NanoCell. Section 4.4 discusses the pattern density dependence of the final film morphology and how this can be utilized for wafer-scale morphology tuning. Section 4.5 addresses how these films can be used for non-volatile memory applications. In this discussion, the morphology of gold films is quantitatively compared to palladium films. The scaling of these films in both density and average particle area is investigated. Section 4.6 introduces a novel technique to increase the density of these palladium films while fabricating a target particle size. Finally, Section 4.7 summarizes the major points made in this chapter.

4.1 Theory

Thin film deposition generally follows one of three types of growth formation distinguished by the interaction strength between the deposited atoms and the substrate.

[99] Layer-by-layer growth is characteristic of the van der Merwe mechanism. [118] The Stanski-Krastanov mechanism is characterized by the formation of an initial monolayer followed by island growth. [119] Finally, the Volmer-Weber mechanism is characterized by three-dimensional nucleation and island growth. [120] Evaporation of refractory metals onto glass substrates has long been known to follow the Volmer-Weber growth mechanism, which is governed by the weak interaction between the impinging metal atoms and the substrate. As more material is deposited, the islands grow through Ostwald ripening and coalescence. [121, 122] Eventually the film will become continuous as more metal is evaporated. The process can be reversed, as a thin continuous film can be made discontinuous through techniques such as post-deposition ion-bombardment or post-deposition heat treatments. [103, 104, 105]

Discontinuous metal films have found great application in the field of nanotechnology. They have been used as interconnect scaffolds for molecular memories [97, 98] as well as in stochastic nanowire interface applications [96]. They have been utilized for numerous sensor applications including local surface plasmon resonance for biosensing [123, 124], and the use of palladium discontinuous films for hydrogen sensors. [105, 106, 107] Recently, these films have garnered much attention for their use in metallic nanocrystal nonvolatile memory applications. [125, 126, 127, 128] Their value to these applications strongly depends upon the ability to control their morphology. Therefore, this chapter will focus on the controlled formation of discontinuous palladium films as the application-driven technology requires further island scaling. First, however, the fabrication of discontinuous palladium films is discussed.

4.2 Fabrication

Palladium is deposited on top of a 1000Å thermal oxide using E-beam evaporation. The system uses a Thermionics, Inc. 5-position electron gun for evaporation, and a Sycon, Inc. STM-100 quartz crystal microbalance for measuring film thicknesses. The base pressure for the evaporations is $5*10^{-6}$ Torr, with a target evaporation rate of about 0.5 Å/s. Evaporations were timed and endpointed using the

average thickness as displayed by the Sycon thickness monitor. Three parameters affect this measurement: the material density, material z-factor and the equipment tooling factor. [129] Numerous experiments were performed to fine tune these values in attempts to reduce the error in the thickness measurements and allow for more accurate comparisons with the previous analysis on gold discontinuous films.

4.2.1 E-Beam Calibration

In calibrating the E-beam system, the first parameter tested was the tooling factor of the equipment. The tooling factor is a system geometry correction that accounts for the difference in location between the substrate and the thickness sensor. Figure 4.1 shows the physical layout of the E-beam evaporator. The pre-established tooling factor for this E-beam evaporator was 77%.

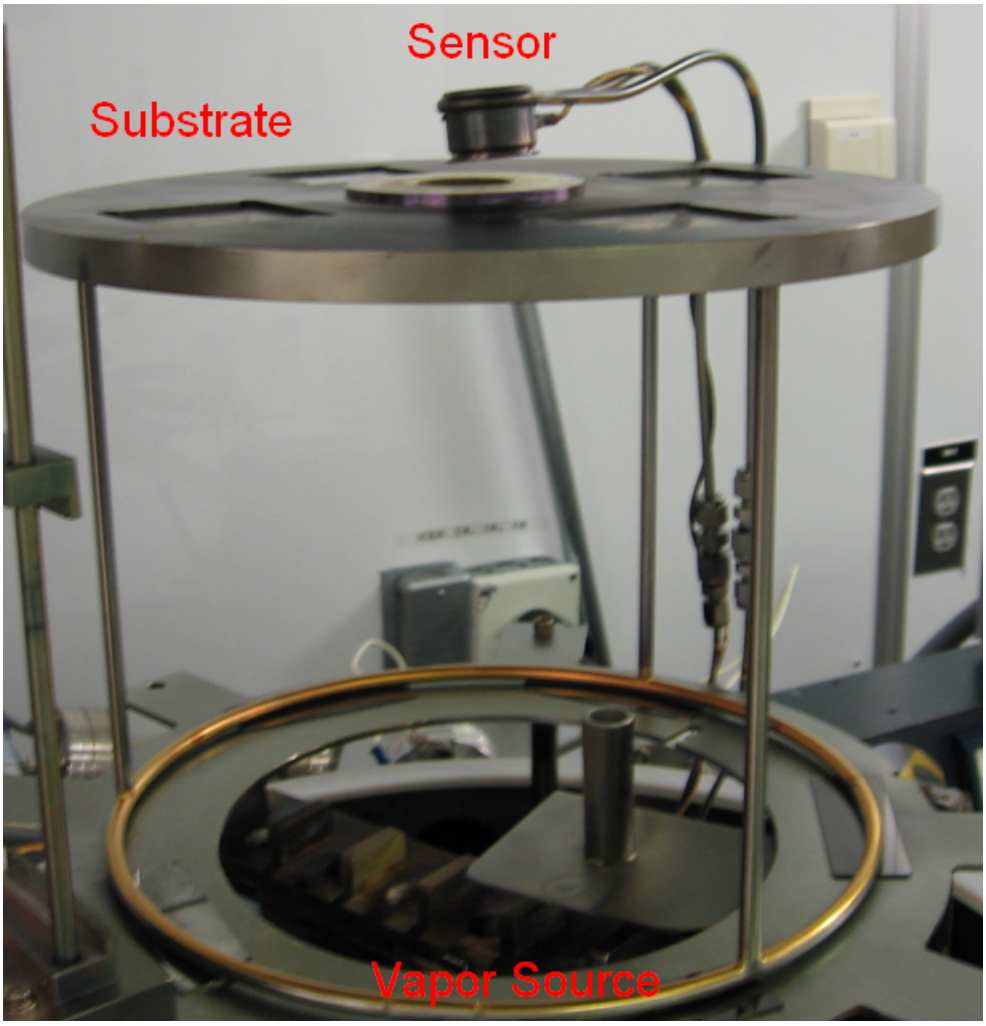


Figure 4.1: E-Beam Evaporator System Geometry

The procedure used to determine the tooling factor closely follows that which is outlined in the Sycon Instruments Thickness Monitor User Manual. [129]. A 1000Å thick gold film was deposited through a shadow mask using a tooling factor of 100% and using the bulk density and z-factor parameters for gold, 19.32 gccm and 0.381 respectively. The actual evaporated thickness was then measured using a Sloan Dektak II profilometer, resulting in approximately 800Å of gold being deposited at the center of the wafer. Using Equation 4.1, this correlated to a tooling factor of 80%.

$$Tooling\ Factor = 100 \times \frac{(Acutal\ Measured\ Thickness)}{(Sensor\ Displayed\ Thickness)} \qquad Equation\ 4.1$$

Considering the vertical resolution of the profilometer is 50Å and the exact center of the wafer as it was placed in the sample holder could only be approximated, this value was believed to be in agreement to the previously established 77% tooling factor. A possible cause for any true physical discrepancy could originate from the use of different sample holders, as shown in Figure 4.2.

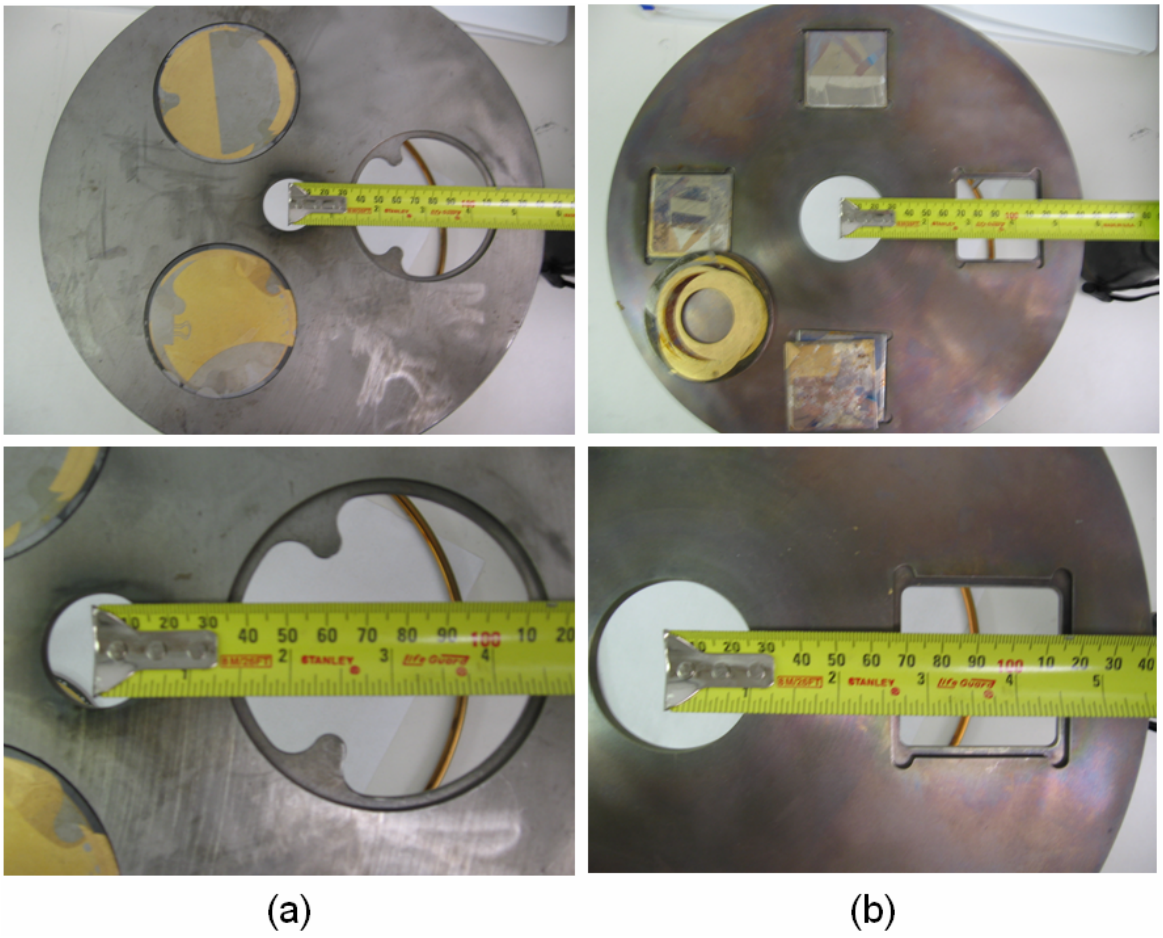


Figure 4.2: Sample Holders for E-Beam Evaporator (a) Custom Fabricated Holder from which 80% Tooling Factor was Attained and (b) Original Sample Holder in which Previously Established 77% Tooling Factor Originates

Figure 4.2(a) shows a custom fabricated sample holder for increased evaporation coverage for 3" wafers. Figure 4.2(b) shows the original sample holder used for the 77% tooling factor calibration experiments. Notice how the distance from the center of the plate to what would be considered the center of the sample is different between the two holders. In the case of the sample holder shown in Figure 4.2(b), the center of the sample is further away, about 3.75 inches, from the sensor than for the sample holder illustrated in Figure 4.2(a), about 3 inches. The increased distance would effectively decrease the tooling factor, since the evaporated thickness would be smaller further away from the source. Thus, this could be the cause of this difference between the 80% tooling factor established from these experiments and the previously established 77% tooling factor for this E-Beam evaporator.

Convinced of the relative accurateness of both the tooling factor and the previous depositions using gold; the next sets of experiments were aimed at investigating the deposition of palladium. Using the confirmed tooling factor, palladium was evaporated using the bulk values for the density and z-factor. Subsequent profilometer measurements revealed a significant statistical difference between the Sycon monitor thickness and the actual measured thickness. Therefore, the next set of experiments was aimed at testing the material parameters for palladium, i.e. the density and z-factor.

Closely following the procedure outlined to determine the material density; a 1000Å thick palladium film was deposited through a shadow mask using a tooling factor of 100%, a z-factor of 1.000, and the bulk density for palladium, 12.0 gccm. Every attempt was made at placing the wafer as close to the thickness sensor as possible. Numerous profilometer measurements were taken on the area of the wafer that was closest to the sensor. A corrected density value of 10.78 ± 0.42 gccm was calculated using the formula given in Equation 4.2.

$$Corrected\ Density = \frac{(Bulk\ Density) * (Sensor\ Displayed\ Thickness)}{(Actual\ Measured\ Thickness)} \qquad \textit{Equation 4.2}$$

The range in the corrected density value takes into account one standard deviation of error in the actual measured thicknesses. In addition, an appreciable distance between the wafer and the sensor still existed despite every effort to place them in close proximity. This resulted in the thickness deposited on the wafer being less than that deposited at the sensor, implying the actual measured thickness may be undervalued in the calculation. This would effectively depreciate the corrected density, leading one to assume that the value would most likely be less than the calculated 10.78 gccm. Therefore, the corrected density value was assumed to be in between 10.36 and 10.78 gccm. This range is highlighted in Figure 4.3, which plots the results of several experiments aimed at further isolating the corrected density value.

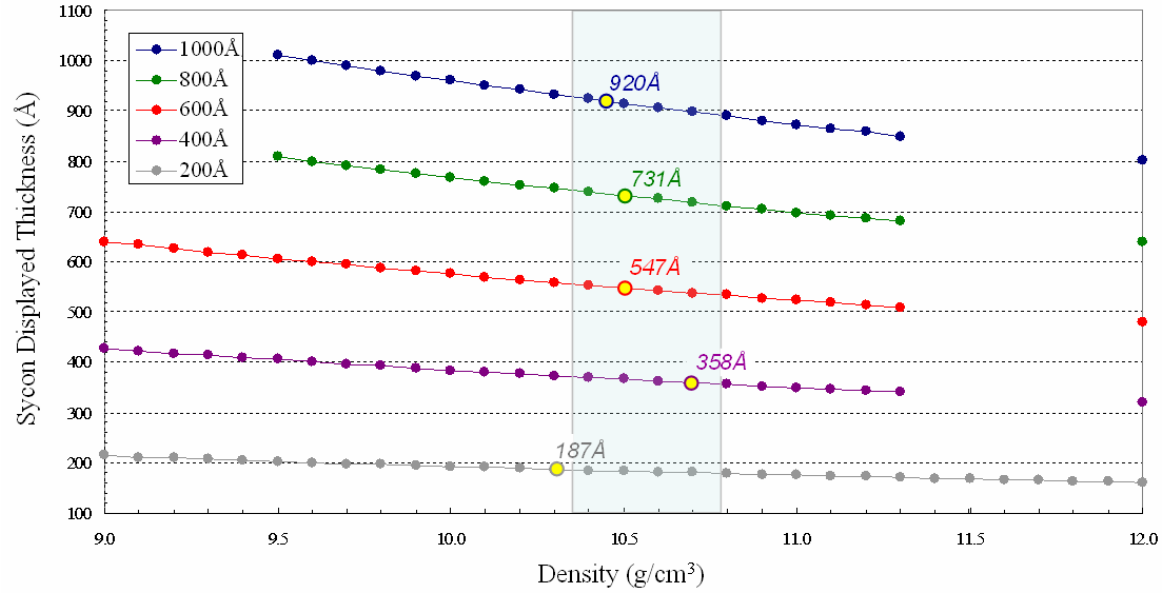


Figure 4.3: Sycon Displayed Thickness (Å) vs. Density (gccm)

In each experiment, a different thickness, ranging from 1000Å down to as thin as 200Å, was evaporated using a tooling factor of 100%, and the bulk density and z-factor for palladium. After the evaporation, the tooling factor was set to 80% and the density was cycled through. As the input density changed, the reading from the displayed Sycon

monitor thickness was recorded and plotted. The films thicknesses were than measured using the profilometer, the results of which are noted and highlighted on each data set.

Except for the thinnest evaporated film, which has the highest percentage of error in the profilometer measurements, all of the measured average thicknesses fell within the expected range for the corrected density value. From this set of experiments, that value was determined to be 10.51 ± 0.17 gccm. Thus, for experiments comparing gold with palladium, we used the corrected density of 10.5 gccm, a tooling factor of 80% and the bulk z-factor of 0.351, which seemed to have minimal impact on the thickness reading and is expected to be very close to the bulk value. [129]

4.2.2 Morphology Dependence on Post-Evaporation Anneal

Once the E-beam evaporator was calibrated and the ability to deposit target thicknesses was established, fabricating discontinuous palladium films was the next objective. Electrical characterization of palladium films deposited as thin as 8Å exhibited ohmic behavior, suggesting that post-evaporation processing was required. The films underwent a rapid thermal anneal in an Argon environment using an AG Associates Rapid Thermal Anneal Heatpulse 210M. Electrical measurements post-anneal revealed that the films became electrically open, as shown in Figure 4.4.

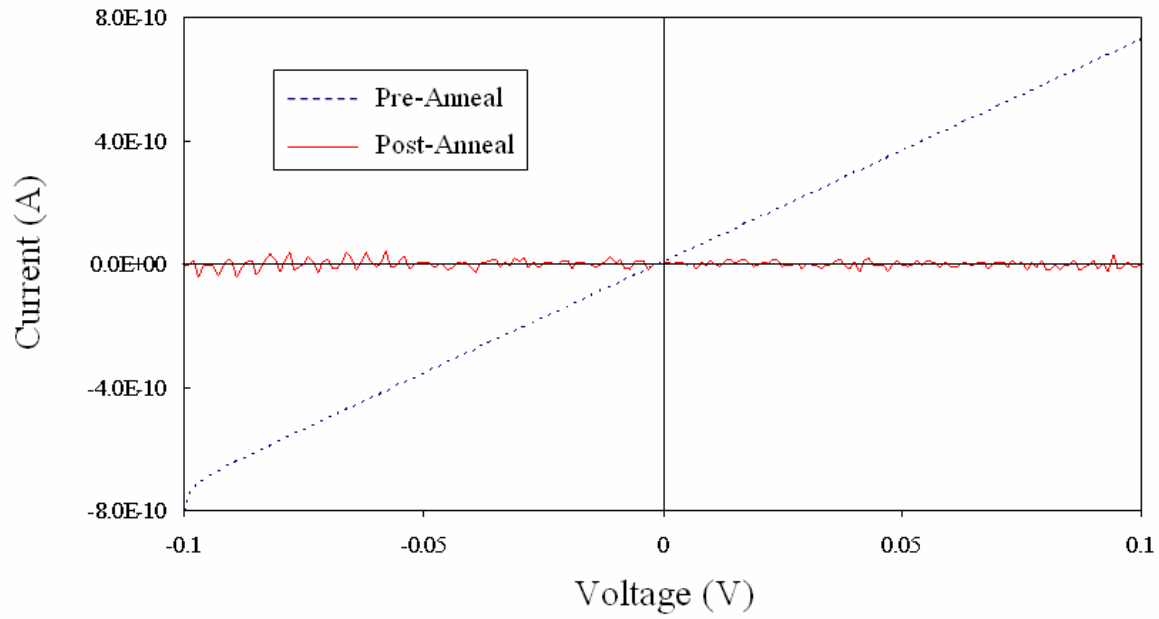


Figure 4.4: Current-Voltage Characteristics of an 8Å Pd Film Pre- and Post-Anneal

The dependence of the film morphology on the initial evaporated thickness, and both the duration and temperature of the heat treatment was analyzed. Although the dependence of the film morphology on these variables is convoluted, analyzing them individually did lead to some general observations. The first of which, concerning the duration of the heat treatment, was that the morphology generally did not change much after a certain duration. This is demonstrated in Figure 4.5 in which the thickest film that was evaporated, 160Å, was heated at the lowest temperature tested that would make the films discontinuous. It was believed that the thickest film heated at the lowest temperature would require the maximum duration heat treatment, thus setting the upper bound for the duration.

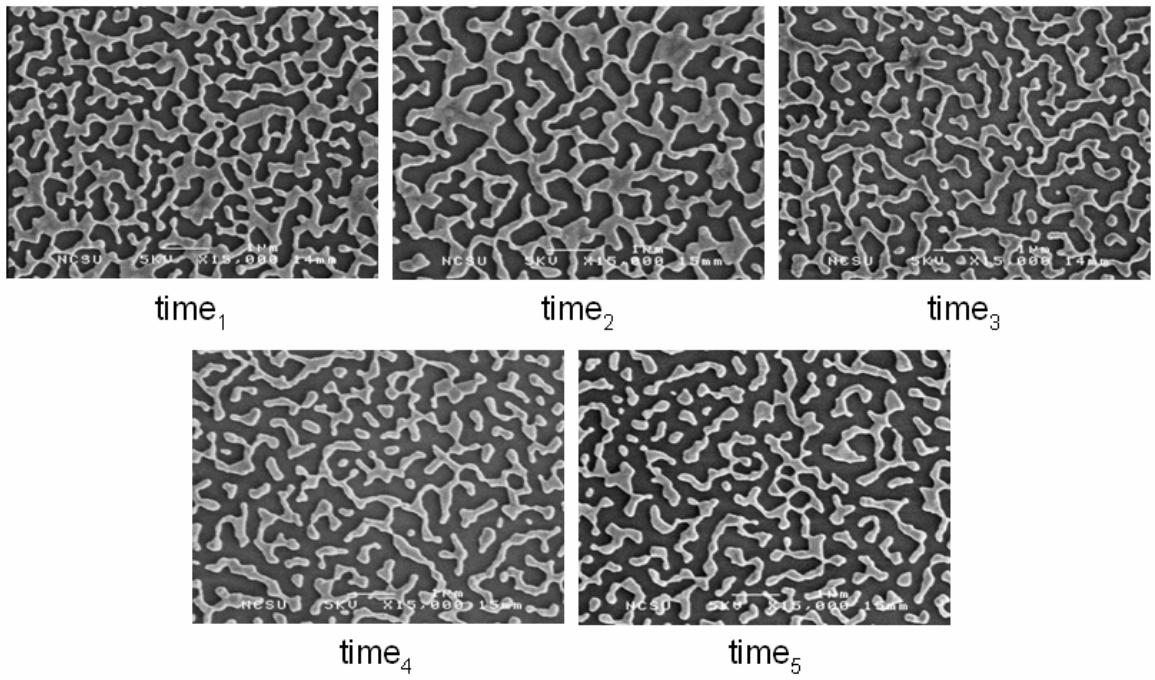


Figure 4.5: 160Å Palladium Film Heated for Various Durations

In this figure, $time_i$ is less than $time_{i+1}$. Clearly after a certain duration, $time_4$, the morphology seemed to reach a steady-state or equilibrium. Another general observation was that the temperature did not seem to have a significant impact on the final morphology. Figure 4.6 shows an 80Å thick film heated at various temperatures. Until a certain temperature was reached, the film remained continuous, demonstrating that as long as the eutectic temperature of the material is reached, the temperature did not have a significant impact on the final morphology of the film, at least in the range tested.

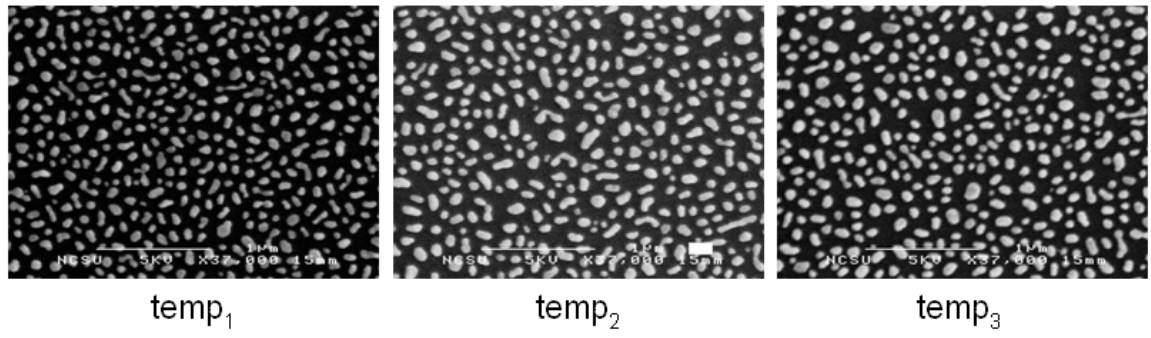


Figure 4.6: 80Å Palladium Film Heated at Various Temperatures

In this figure, $temp_i$ is less than $temp_{i+1}$. Thus, as long as the films were heated above a certain activation temperature for a certain duration, they seemed to reach a final equilibrium or steady-state morphology, which suggests the existence of some local minimum energy state that bodes well for controllability. However, comparing Figures 4.5 and 4.6 reveals very unique final morphologies. The major difference between these experiments was the initial evaporated thickness, which turned out to be the most significant contributor to the final morphology. Figure 4.7 summarizes these trends illustrating the dependence of the final morphology on these variables.

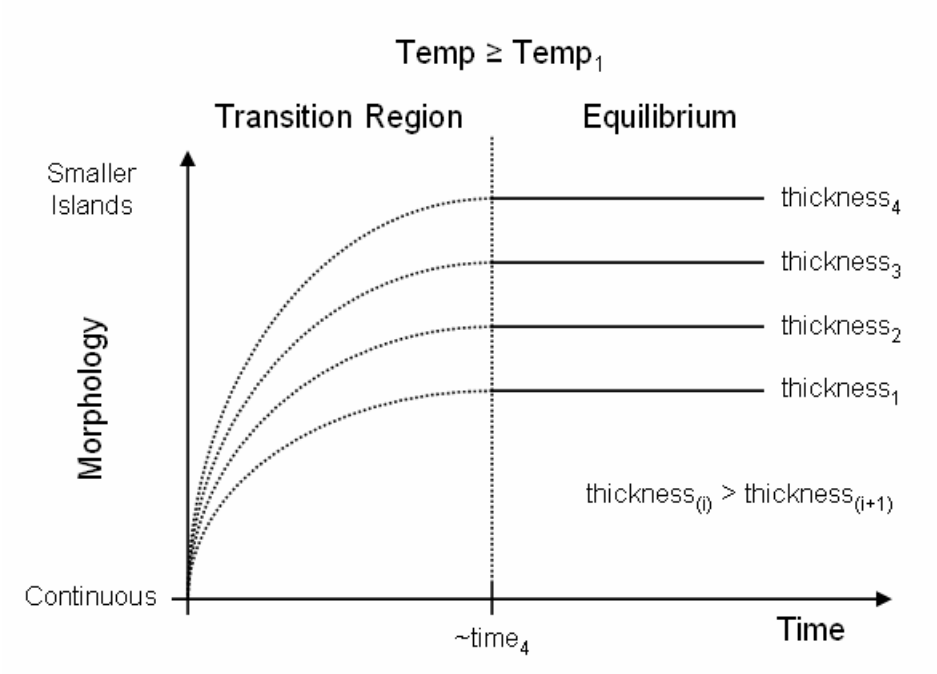


Figure 4.7: General Trends in Controlling the Palladium Morphology

Also depicted in this figure is how the morphology scales with initial evaporated thickness. Controlling this thickness allows one to engineer films towards specific applications, including molecular scaffolding, sensors, and nonvolatile memory. Control of the morphology will be further demonstrated in the scope of applications of these films for nanotechnology.

4.3 Applications for Molecular Electronics

Discontinuous metal islands have found application as scaffolding for molecular electronic characterization structures, interfaces, and architectures. [40, 96, 110] An example of an architecture that utilizes discontinuous metal films is the aforementioned NanoCell, in which bistable molecules are interconnected by an underlying random distribution of colloids, discontinuous films and/or nanowires. In theory, the system is trained to perform logic or memory post-fabrication based on voltage pulses that switch the molecules on or off. Experiments with gold NanoCells suggest that current transport is based on the breaking and reforming of metallic filaments, rather than molecular conduction. [97] Thus, metals with a higher melting point and less likely to electromigrate, such as palladium, are preferable. To utilize discontinuous metal films for NanoCell applications, three basic requirements exist:

(1) The islands must be large enough so that a molecularly functionalized nanorod could bridge two islands.
(2) The films should be patterned using standard lithographic techniques.
(3) The current must pass between the functionalized nanorods and not between the islands themselves, i.e. the films are electrically discontinuous.

The first challenge was to engineer the morphology of the films such that a molecularly functionalized nanorod could bridge two islands. The gap distance between the metal leads coming into the NanoCell was generally between one to five micrometers.

Thus, the islands had to be small enough so that they did not short the leads but long enough so that two rods could fall across one island creating an electrical path through the molecules. Figure 4.8 shows the results of several evaporations aimed at engineering this target morphology. From these results, it was decided that while 130Å may produce islands that are too small, the islands in the 140Å film ran the risk of shorting the leads. Therefore, for NanoCell applications, a 135Å palladium film was evaporated and subsequently annealed.

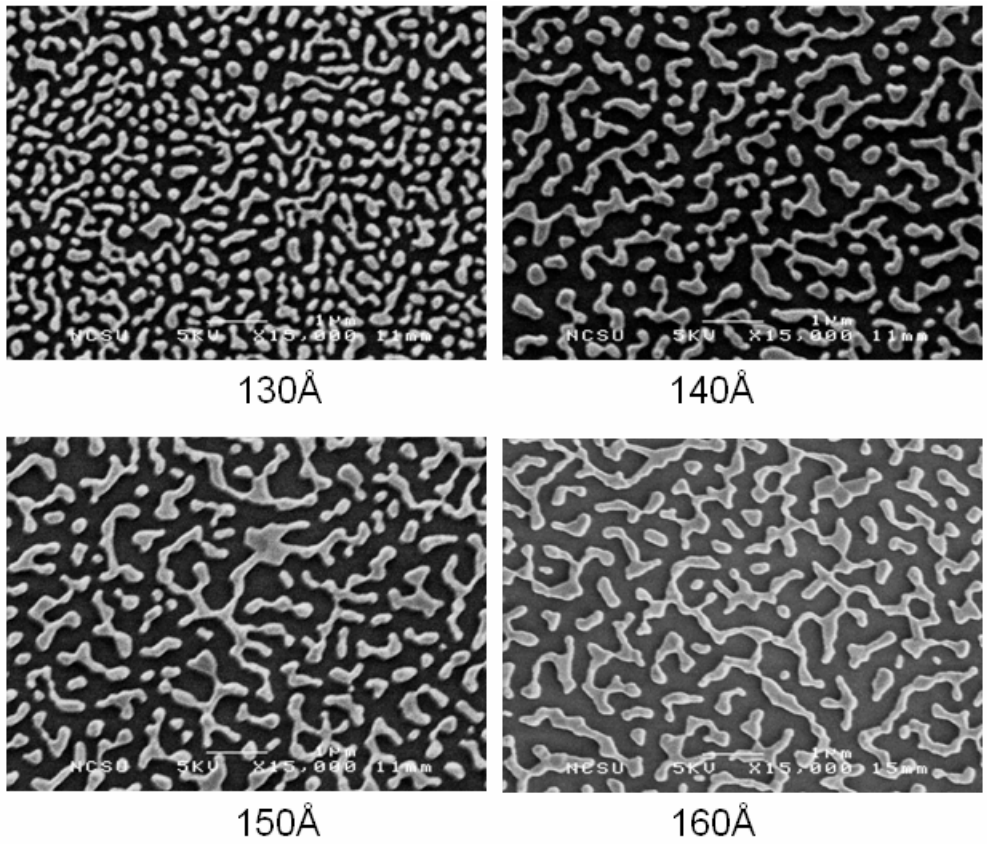


Figure 4.8: Engineering the Morphology for NanoCell Applications

Now that a target morphology satisfying the first requirement for NanoCell applications was attained, the next step was to fabricate patterned NanoCells with the target palladium films in the active areas. To pattern the films, a liftoff technique was

utilized similar to one described previously. [130] The active areas were defined prior to the leads, ensuring that only the target areas underwent a rapid thermal anneal. An example of a fabricated palladium NanoCell can be seen in Figure 4.9, accompanied with its Current-Voltage characteristics.

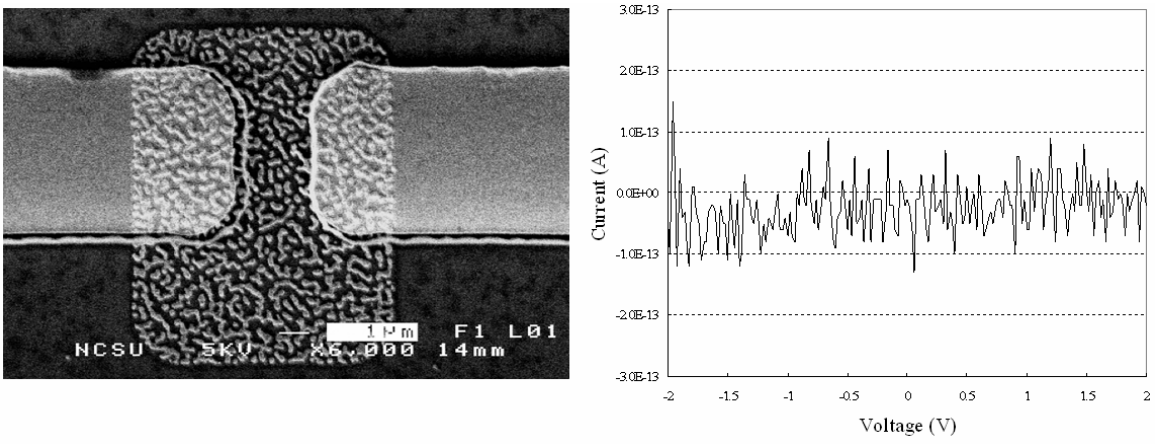


Figure 4.9: Patterned Palladium NanoCell with Electrically Open IV Characteristics

From this figure, one can clearly see that the films were both patternable and electrically discontinuous, satisfying the final two requirements for application to the NanoCell. Thus, the fabricated samples were shipped to Rice University for molecular attachment. Mono-nitro dithiol OPEs were attached to palladium nanorods and assembled inside the NanoCells, as shown in Figure 4.10.

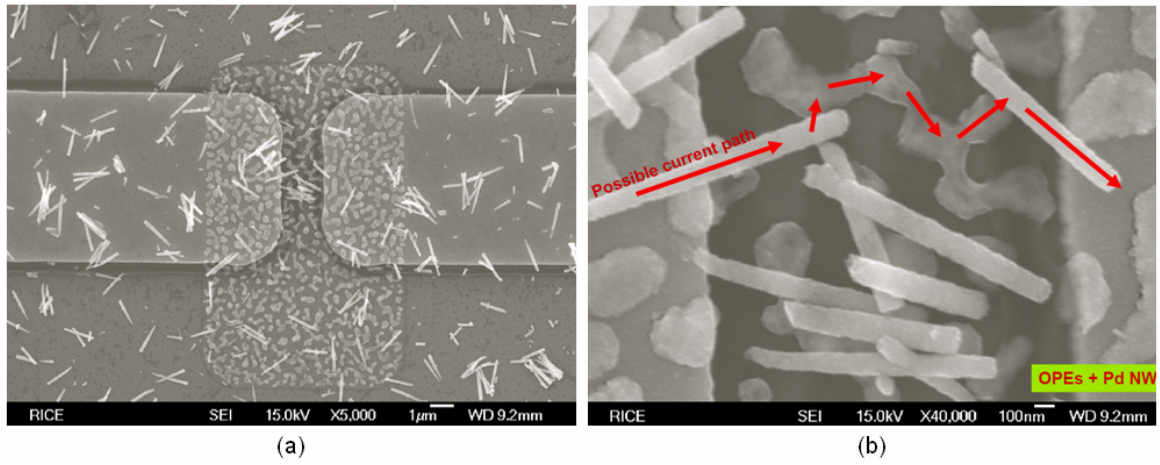


Figure 4.10: Functionalized NanoCell (a) Patterned Palladium NanoCell with Functionalized Pd Nanorods (b) Magnified Image of Active Area Showing Possible Conduction Path (Courtesy Rice University)

Figure 4.10(b) shows a possible conduction path through the functionalized nanorods, successfully demonstrating the potential of these films to be used as molecular scaffolds. However, during their fabrication, an unexpected result was observed in which the morphology of the film for smaller patterns became dependent upon the surrounding pattern density. This effect is examined in the next section, as well as some of the potential implications.

4.4 Applications for Sensors – Pattern Density Dependence

In the process of patterning discontinuous palladium films for NanoCell applications, it became apparent that the pattern density also influenced the final morphology of the film. Figure 4.11 demonstrates this dependency.

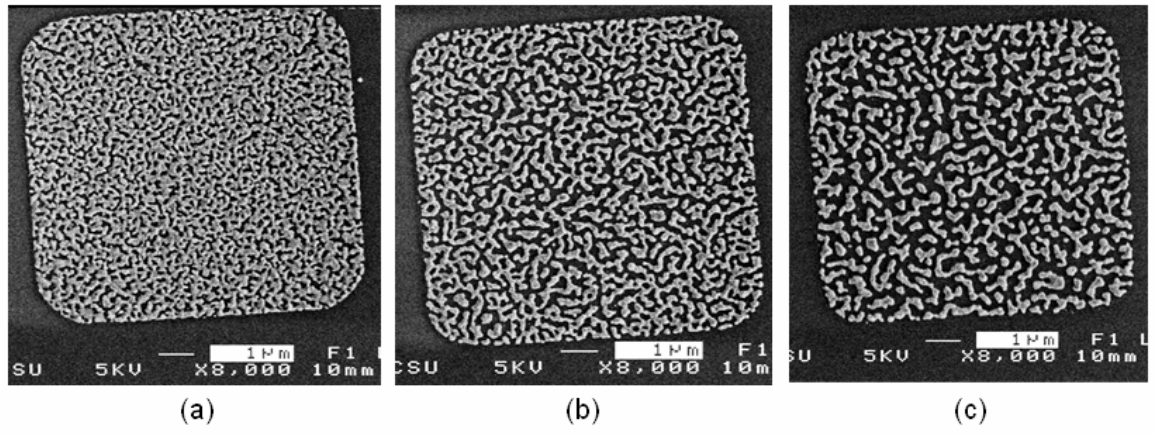


Figure 4.11: Pattern Density Effect.

Several unique structures were designed to test the NanoCell, all with various surrounding pattern densities. In Figure 4.11(a) for example, there were very few patterns close to the illustrated active area. The resulting film morphology is clearly not what was expected from a 135Å palladium film. As the probe pattern density increased, the resulting morphology more closely resembled that of the blanket film evaporation, until as in Figure 4.11(c), the film morphology is what is expected for this evaporation thickness.

It is believed that the surrounding pattern density is acting as heat sources for the film in the active areas. As this density increases, the active areas experience a heating effect more closely resembling that of a blanket evaporation. In all cases, the morphology of larger structures resembled that of the blanket evaporation, suggesting that there is a pattern size limit in which the films resemble infinite sheets and pattern density has no effect.

As previously mentioned, the utility of these films is largely based on the ability to control their morphologies. If the morphology is largely governed by the initial thickness, than applications with different morphology property requirements would require multiple evaporations and possibly multiple photolithography steps. Exploiting this pattern density effect could lead to wafer-scale control of the film morphology with only a single evaporation, significantly reducing manufacturing costs. Consider for

example, the use of discontinuous metal films for surface plasmon resonance sensors. [124, 125] If the morphology of the films could be controlled through this pattern density effect, than the surface plasmon resonance wavelength could theoretically be tuned wafer-scale. Thus, unique detectors could be fabricated with only a single evaporation. Current efforts to test this technique are underway. Overall, numerous applications could be impacted by the ability to control the morphology of the films wafer scale using only a single evaporation.

4.5 Applications for Non-Volatile Memory

4.5.1 Theory and Motivation

Discontinuous metal films have garnered much attention recently for their use in metallic nanocrystal nonvolatile memory applications. [125, 126, 127, 128] In conventional floating gate nonvolatile memory, a continuous layer of polysilicon is deposited between two dielectrics. The state of the device is determined by the absence, State 1, or presence, State 0, of charge on the floating gate, as demonstrated in Figure 4.12. When there is no charge on the floating gate, the device operates similarly to a typical MOSFET. However, when the floating gate is charged, the presence of this charge shields the channel from the control gate, shifting the threshold voltage. The drain current is sensed to determine the state of the device. A device in “State 1” will conduct current at the read voltage while a device in “State 0” will not. This device is considered non-volatile since the floating gate is sandwiched between two dielectric layers and retains its charge when the power is turned off.

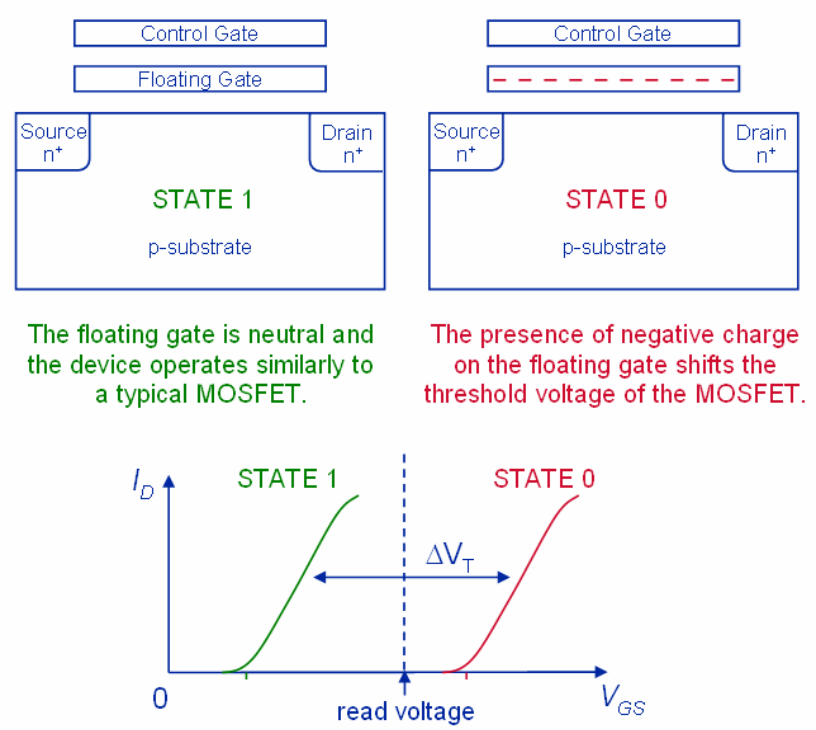


Figure 4.12: Operation of Conventional Floating Gate Non-Volatile Memory

Unfortunately, any point defect in the oxide will discharge the continuous floating gate, which significantly limits the scalability of these devices. The use of electrically isolated nanocrystal storage elements helps solve this problem and allows for more aggressive scaling of the tunneling dielectric. This leads to more efficient charge transfer to the floating gate; enabling high speed, low voltage, and low power programming. The distributed nature of the charge in the nanocrystals results in excellent immunity to stress induced leakage current, improving data retention. The immunity of discrete nanocrystals from point defects in the tunnel oxide improves data endurance. [131]

The use of metallic nanocrystals rather than the more conventional silicon nanocrystals also has its advantages. The larger work function of metals compared to the electron affinity of silicon results in a higher tunneling barrier height; creating a deeper potential well and reducing leakage current, further improving data retention and endurance. The large diversity of available work functions allows greater design

flexibility to engineer the data retention/programming efficiency tradeoff. Metallic nanocrystals also allow for tighter threshold voltage control which can lead to more stable and uniform device characteristics. In addition, there is greater potential to scale metallic nanocrystals compared to their silicon counterparts. [126] Ultimately, nanocrystal non-volatile memory devices have the potential to scale beyond the ITRS roadmap for conventional Flash devices, as shown in Table 4.1.

Table 4.1: Comparing Nanocrystal NVM with Conventional Embedded FLASH

	Nanocrystal NVM			Current Embedded FLASH (Based on 2005 ITRS [132])
Dielectric Thickness	Tunnel: 2.5–3nm range [125, 133, 134, 135, 136] Control: 5–10nm range [133, 134, 135, 136, 137]			Tunnel: 8.5–9.5nm range Control: 11–13 nm range
Threshold Shift / Program Voltage	<u>Vth Shift</u>	<u>Volt Sweep</u>	<u>Ref</u>	Write Voltage: 12V
	2.5V	2V to -4V	[125]	
	0.75V	± 2V	[138]	
	1.1V	± 3V	[138]	
	0.95V	3V to -4V	[133]	
	> 1V	± 3V	[136]	
Data Retention Time	Demonstrated 10^6s (~1.5 wks) [127, 139] Extrapolated out to 10 years [140] High Temp Accelerated Tests → 10 yrs [134]			> 10 years
Data Endurance (Write/Erase Cycles)	Demonstrated for 10^6 cycles [133, 134, 138, 140] > 70% of Threshold Shift to 10^9 cycles [133] Demonstrated for 10^9 cycles [141]			> 10^5 cycles
Programming Speed	10µs Program Time [135] Sub-10µs Program / sub-100ms Erase [139] 10µs Program / 100µs Erase [142]			1µs Program Time 10ms Erase Time
Integration / Maturity	Silicon Nanocrystal Memory Arrays of 1Mbit [135] and 4Mbit [139] Demonstrated			In Production
Scaling Potential	Promising			Challenging

Clearly this demonstrates that equivalent and often improved performance and technology metrics are achievable with nanocrystal nonvolatile memory as compared to the current embedded Flash devices. However, there are certain technology requirements placed on the nanocrystals. It has been theorized that the target density for nanocrystal non-volatile memory should be at least 10^{12} particles/cm^2, which would represent 100 nanocrystals in a 100nm x 100nm square area. The deposition method must result in planar nanocrystal formation such that the dielectric thickness separating the substrate from the nanocrystals is constant. Tight control of the particle size, inter-particle distance, distribution, and uniformity is preferred, since these film properties directly affect the electrical properties of the device. [131] The inter-particle distance impacts data retention since it affects the amount of lateral charge redistribution. Morphologies with smaller islands at similar high densities could therefore have data retention advantages. A tight distribution of the islands sizes and film uniformity are important to minimize the variability in the threshold voltage distribution. It is important to establish how the nanocrystal uniformity can impact the device characteristics, but to do so requires an understanding of the uniformity of the deposition process. This is investigated in the following section.

4.5.2 Thickness Uniformity using E-beam Evaporation

It has been shown that the initial thickness of the evaporated film has the largest impact on the resulting morphology. It was the morphology difference between the top and bottom of the wafer, closest to and furthest from the evaporation source, which initially suggested this dependency. Understanding the thickness uniformity across-the-wafer is critical for applications of these discontinuous films whose success typically depends on achieving certain morphology requirements. Alternatively, exploiting these uniformity differences in test structures and understanding its effect on device characteristics can assist in optimizing these films for a target application. It is with this motivation that experiments were performed to understand the thickness uniformity of our process in our E-beam Evaporator.

The vapor stream density of small-area evaporators can be described by Equation 4.3. [143] Small-area evaporators are those in which the dimensions of the crucible target are much smaller than the distance between the target and the substrate.

$$\Phi(a) = \Phi_o \cos^n a \qquad \textit{Equation 4.3}$$

This equation is typically valid for angles less than 30^o. Φ_o is the thickness of the film directly over the target at $\alpha = 0^o$. The exponent, n, compensates for physical non-idealities of the evaporation. These include deformation of the evaporant, surface tension of the evaporant, inadequate evaporant loaded in the crucible, and high evaporation rates. The deformation of the evaporant can cause the emitting vapor to become concave. High surface tension of the evaporant, such that the crucible walls are not wet, can cause the emitting vapor to become convex. Inadequate evaporant can cause the crucible walls to obstruct the vapor projection. Finally, high evaporation rates can result in a vapor cloud forming above the evaporant that acts as a virtual evaporant source. Typically, the evaporation rate has a strong impact on the resulting thickness distribution. As the evaporation rate increases, the exponent used to model the thickness distribution also increases. Thickness uniformity from evaporation rates of about 50Å/s have been modeled using an exponent between 2 and 3, whereas evaporation rates as high as 1000Å/s have been modeled using an exponent of 6. [143] Typically, for the relatively low evaporations rates used in our experiments, ~1Å /s, the exponent would be expected to fall between 1 and 2, more closely resembling the simple cosine distribution model.

The film thickness evaporated from a small-area source onto a parallel plane surface is derived using the vapor stream density distribution. The thickness reduction factor is given in Equation 4.4.

$$\frac{d_s}{d_o} = \frac{1}{\left[1+\left(\frac{r}{h}\right)^2\right]^{(n+3)/2}}$$

Equation 4.4

In this equation, d_s is the thickness of the film at the point of consideration. d_o is the thickness of the film directly above the vapor source at $\alpha=0^o$. As was previously shown in Figures 4.1 and 4.2, r is the radial distance between the point directly above the vapor source to the point of consideration, and h is the source-to-substrate distance, measured to be about 10.5 inches for our setup.

From Equation 4.4, the thickness uniformity across-the-wafer can be calculated once the exponent, n, is determined. To determine this exponent, 200Å of palladium were evaporated onto a 3" wafer patterned using a liftoff process. The thickness across-the-wafer was than determined measuring along the central axis of the wafer using a JEOL 5200 Atomic Force Microscope. The results of these measurements and the theoretical predictions of the thickness uniformity are shown in Figure 4.13.

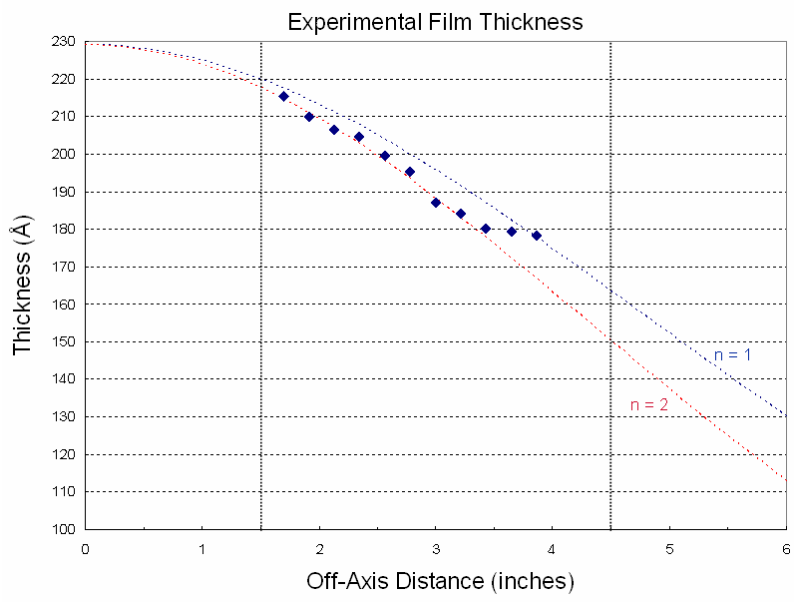


Figure 4.13: Thickness Uniformity Across-the-Wafer

From this figure, it is clear that the value for the exponent likely falls between 1 and 2, as one would expect for low evaporation rates. To try and further narrow down this range, the samples fabricated to test the E-Beam calibration were measured at their edges using the Profilometer. The value for the exponent was than extrapolated by fitting these two measurements, closest to and furthest from the source; the results of which are shown in Table 4.2.

Table 4.2: Extrapolating the Cosine Exponent for the Thickness Uniformity Analysis

	Closest To Source		Center Thickness		Furthest From Source		n
	Measured	Theory	Measured	Theory	Measured	Theory	
Au	899	898	795	795	699	699	2.2
Pd	1014	1013	920	897	788	789	2.2
Pd	983	983	896	891	778	777	1.2
Pd	829	829	731	760	675	674	0.7
Pd	762	762	674	676	595	596	2.1
Pd	597	601	547	547	480	480	1.0

Obviously the measured and theoretical values closest to and furthest from the source agree, since these values were fitted in the extrapolation. Concerning the measured and theoretical center thicknesses, which were not directly fitted in the analysis, four of the six experiments agree to within 5Å, while the other two are about 20Å and 30Å different. Finally, it is apparent that the extrapolated exponent for our E-beam process is in the expected range and averages out to about n = 1.6. Across a 3" wafer in our system this would result in a thickness difference of about 29%. Now that the thickness uniformity of our process is understood, it is important to investigate how this

difference affects the device characteristics of non-volatile memory fabricated using these discontinuous films.

4.5.3 Electrical Characterization of Nanocrystal Capacitors

Structures were fabricated to investigate the potential of these discontinuous films for non-volatile memory applications. A typical cross-section of one of these structures is shown in Figure 4.14(a).

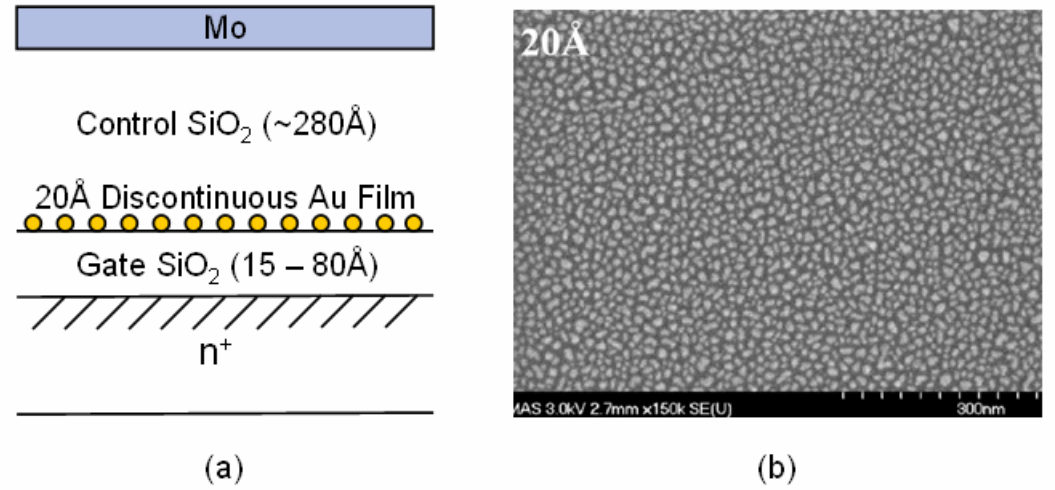


Figure 4.14: Nanocrystal Capacitors (a) Typical Cross-Section and, (b) SEM of 20Å Au Film [130]

The capacitors were fabricated on 4" (100) heavily doped n-type silicon wafers. A gate oxide was thermally grown and then progressively stepped into a hydrofluoric acid etch such that each row of die had a different gate dielectric thickness. 20Å of gold was than evaporated on top of this oxide. Previous experiments suggested that this thickness resulted in gold particles that were on average 10 nm in diameter and dispersed at a density of about $4x10^{11}$ particles/cm^2. [130] An SEM of the typical resulting morphology for this thickness is shown in Fig 4.14(b). A control dielectric of 280Å was deposited by plasma enhanced chemical vapor deposition (PECVD). This relatively large

thickness compared to the thinner gate dielectric would minimize charge transport between the floating and control gate. Finally, Molybdenum gates were deposited and patterned using a lift-off process. Figure 4.15 shows a top view wafer map of the fabricated samples.

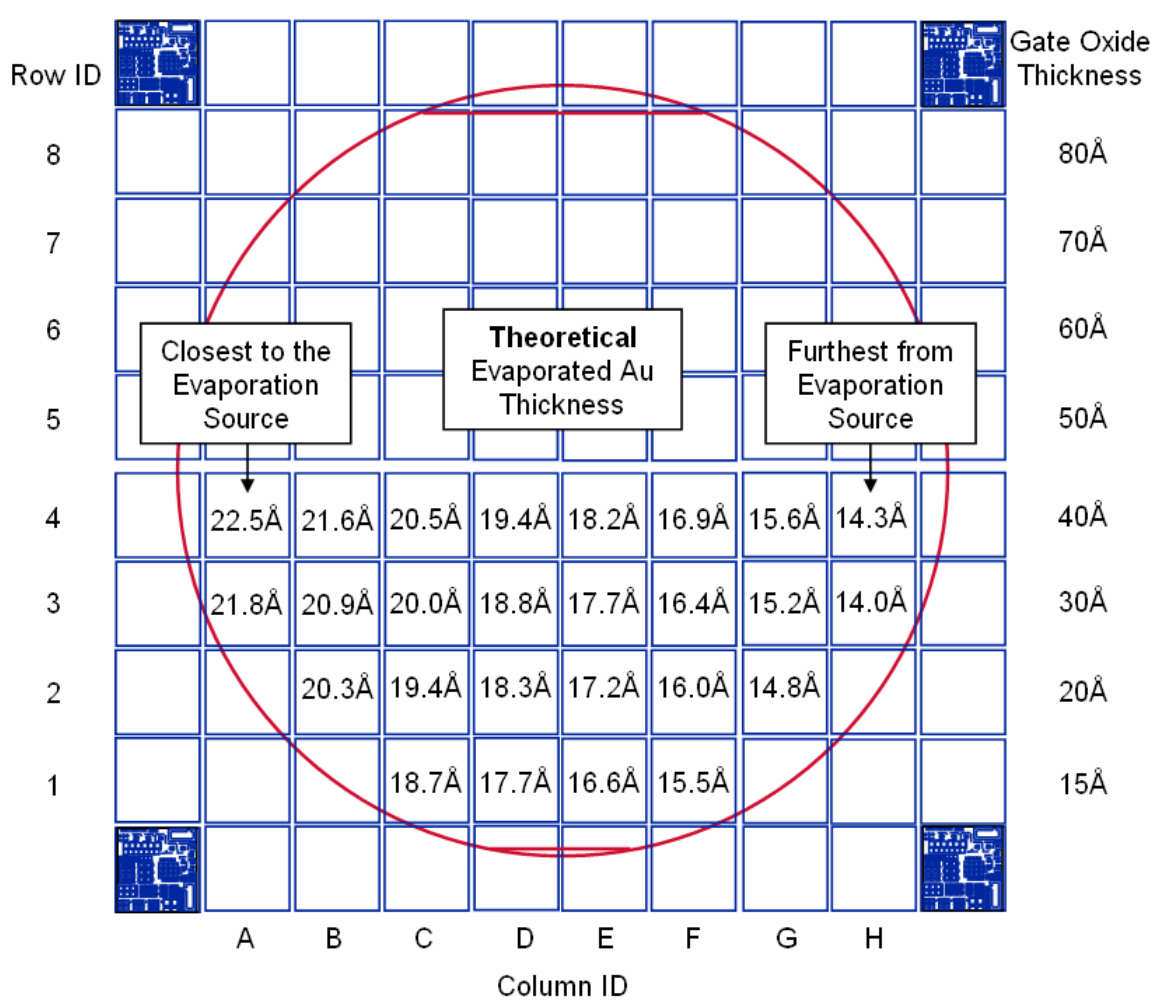


Figure 4.15: Wafer Map of Fabricated Samples

From this figure, it is clear that the gate oxide thickness varies across rows, and the evaporated gold thickness varies maximally across columns. The theoretical evaporated gold thicknesses are based on the uniformity analysis using an exponent of n

= 1.6 and our system dimensions. There are numerous sources of error involved in such a calculation, so listing absolute values with three significant figures to represent true physical thicknesses is not the intended interpretation, but rather that the gold thickness should decrease on the order of 1Å across each column of the wafer. Finally, a control wafer was fabricated with similar capacitors except without the gold nanocrystals. Thus any device characteristics on the process wafer could be compared to the control wafer to help in determining their origin.

In theory, a floating gate device should have a hysteretic capacitance-voltage characteristic. A negative voltage applied to the top control gate will positively charge the floating gate. As the applied gate voltage is swept forward, the positive charge stored in the floating gate reduces the voltage necessary to fully compensate for the work-function difference between the metal and the semi-conductor, resulting in a negative shift in the flat-band voltage. As the applied gate voltage is further increased, electrons tunnel into the floating gate reversing its charge. For a negatively charged floating gate, an additional positive charge must be applied to the top gate, resulting in a positive shift of the flat-band voltage on the reverse sweep. In summary, the presence of positive charge on the floating gate during the forward sweep causes a negative shift of the flat-band voltage, while the presence of negative charge on the floating gate during the reverse sweep causes a positive shift of the flat-band voltage. This produces the hysteretic CV characteristic typical of floating gate memories.

Using an HP 4284A precision LCR meter, Figure 4.16 shows the results of 1-MHz Capacitance-Voltage characteristics measured for devices with a 100μm x 100μm square top control gate and a 40Å thick tunneling dielectric. The measurements were performed at room temperature and in parallel circuit mode. There were no write/erase voltage pulses applied to the top gate. The devices were simply swept from inversion to accumulation and back. From these bidirectional sweeps, a large flat band voltage shift was observed, indicating successful charging of the nanocrystal floating gate.

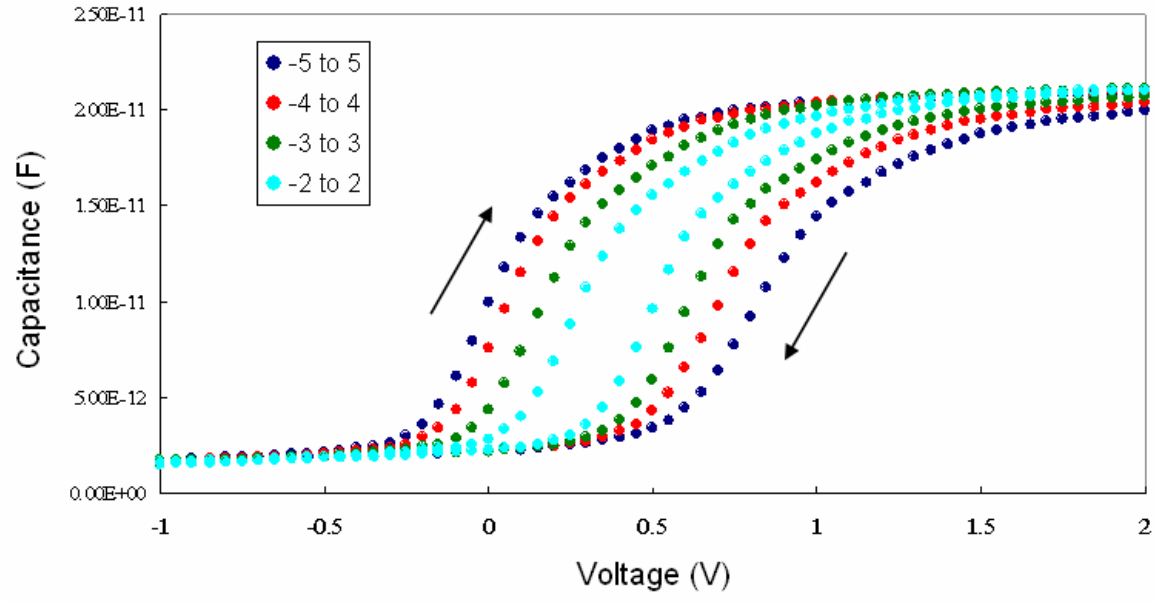


Figure 4.16: CV Characteristics of 100µm x 100µm Au Nanocrystal Capacitors

The magnitude of the flat-band voltage shift is proportional to the total amount of charge stored in the nanocrystals. Assuming that the nanocrystals are not saturated, one would expect the larger sweeps to have larger voltage shifts, as witnessed in Figure 4.16. Alternatively, none of the CV measurements on any of the die on the control wafer showed any signs of hysteresis. Thus, it is assumed that the presence of the gold nanocrystals is the origin of the flat-band voltage shift, as anticipated.

As numerous devices across-the-wafer were tested, one interesting trend was noticed concerning the effect the gold particle size had on the threshold voltage shift. As the off-axis distance from the evaporation source increased, the theoretical evaporated gold thickness decreased. A decrease in the evaporated thickness would decrease the particle size and increase the particle density. The flat-band voltage shifts of similar devices across three different columns of the wafer are shown in Figure 4.17. Even this minimal thickness difference caused by the solid angle of evaporation had appreciable affects on the threshold voltage shift.

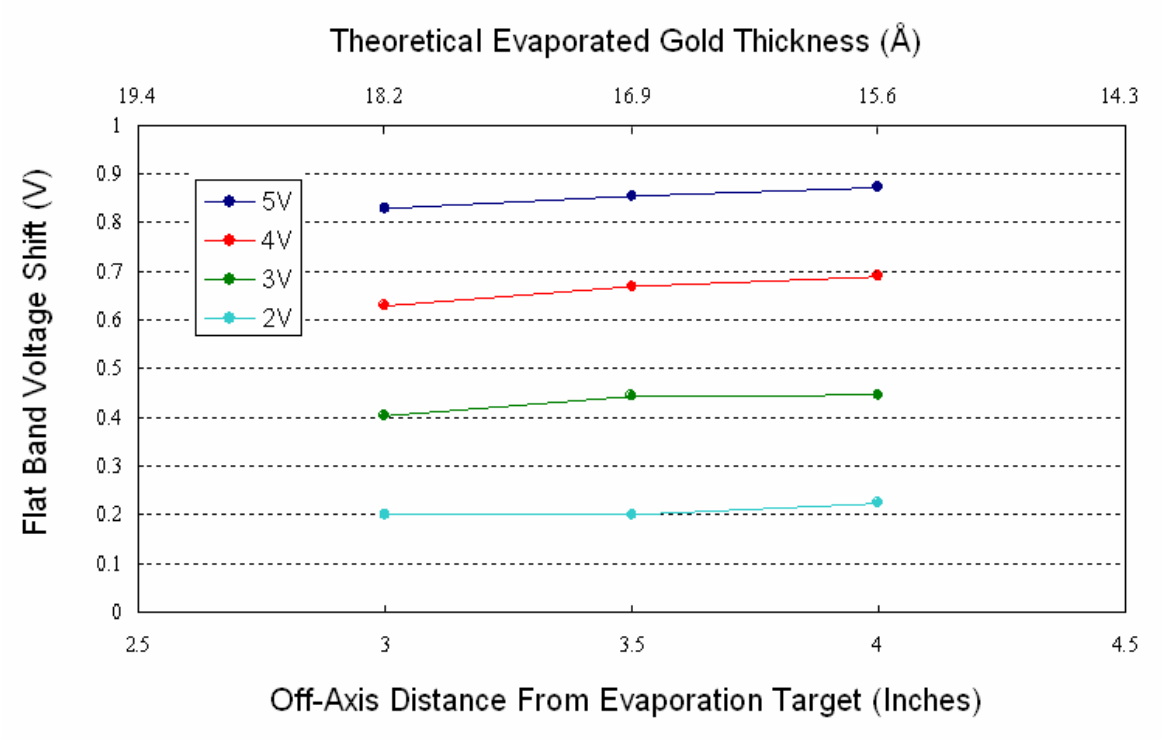


Figure 4.17: Flat Band Voltage Shift vs. Evaporated Gold Thickness

These results are summarized in Table 4.3. Except for the 5V sweep, the average increase in the flat band voltage is over 10%. Considering that only about a 2 to 2.5Å thickness difference is expected, this represents a rather significant increase; suggesting that even further scaling of the gold islands could lead to even more substantial improvements in the flat band voltage shift. It is with this motivation that experiments were performed to try and further scale both the gold and palladium islands.

Table 4.3: Measured Flat Band Voltage Shifts

Voltage Sweep	$\Delta(\Delta V_{FB})$	% Increase
-2 to 2V	0.02V	12%
-3 to 3V	0.04V	11%
-4 to 4V	0.06V	10%
-5 to 5V	0.04V	5%

4.5.4 Scaling Gold and Palladium Nanocrystals

Concerning the scaling of gold discontinuous films, it was previously shown that as the evaporation thickness was reduced, the mean island size decreased while the particle density increased. A custom Matlab program was written to enable digital image extraction of film properties such as particle size, distribution, density, and fill factor. [130] This program was extended and tailored for use in the following analysis on the scaling of palladium films.

Several thicknesses of palladium were evaporated onto a 1000Å thermal oxide grown on 3" wafers. Samples with evaporated thicknesses greater than 40Å were imaged using a JEOL 6400F Field Emission SEM. Stage movement allowed for complete coverage of the wafer and the samples were imaged every 5mm across the axis perpendicular to the evaporation source. The results of several evaporations are shown in Figure 4.18, which demonstrates the scaling of the palladium films with respect to the initial evaporated film thickness.

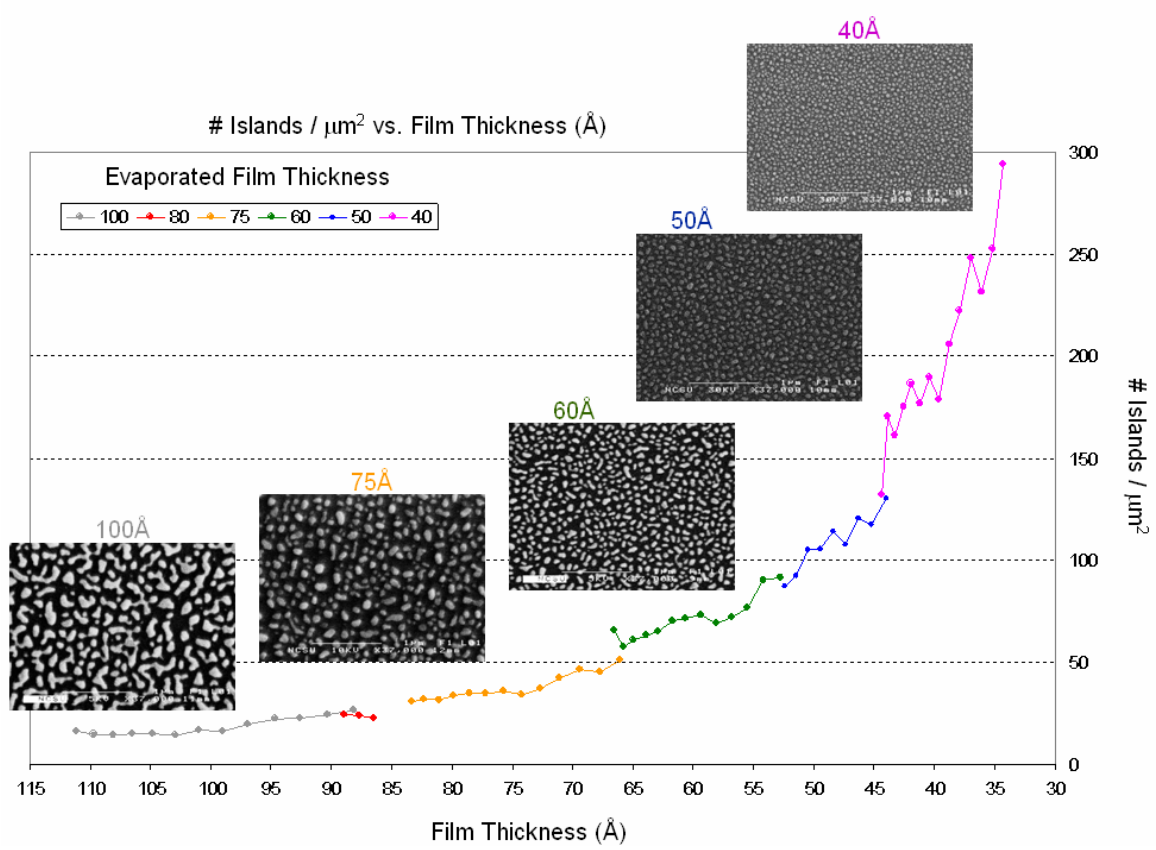


Figure 4.18: Scaling of Palladium Films

From Figure 4.18, the relative continuous nature and overlap of the interfaces between different palladium evaporation thicknesses supports the validity of the E-beam calibration and uniformity analysis. Sample images taken at 37,000x magnification are shown for each of the evaporations and demonstrate the scaling of the palladium islands. The resolution and contrast of films thinner than 40Å were not sufficient for quantitative analysis using the JEOL 6400F Field Emission SEM. Therefore, all films evaporated less than 40Å, as well as all gold films, were imaged by Materials Analytical Services in Raleigh NC using a Hitachi S-4700 FESEM. Data for gold films evaporated between 60Å and 20Å comes from previous work. [130] A summary of the results of the post processing image analysis comparing the scaling of palladium and gold are shown in Figure 4.19.

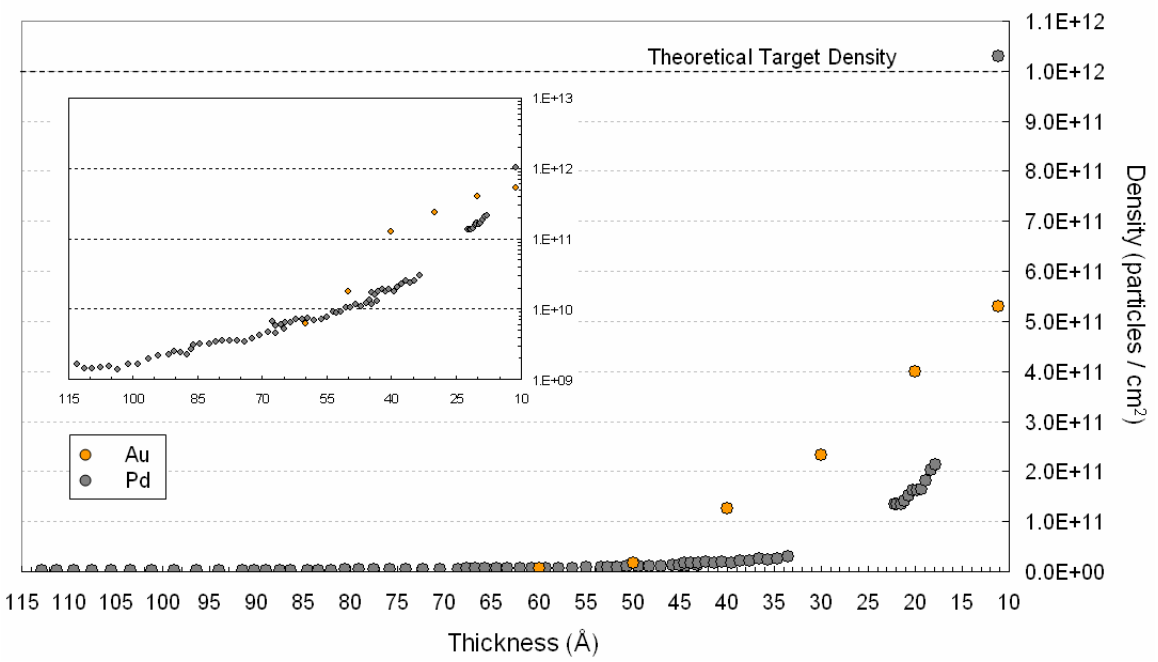


Figure 4.19: Comparing the Scaling of Palladium and Gold

Comparing the gold and palladium films, clearly there are very different trends as the films scale. At about 50Å, the gold particle density seems to scale linearly with decreasing evaporated thickness while the palladium scaling seems to be more exponential in nature. At thinner films, the density of the palladium outscales that of the gold, as demonstrated in Figure 4.20 which shows the results of evaporating 10Å of both palladium and gold.

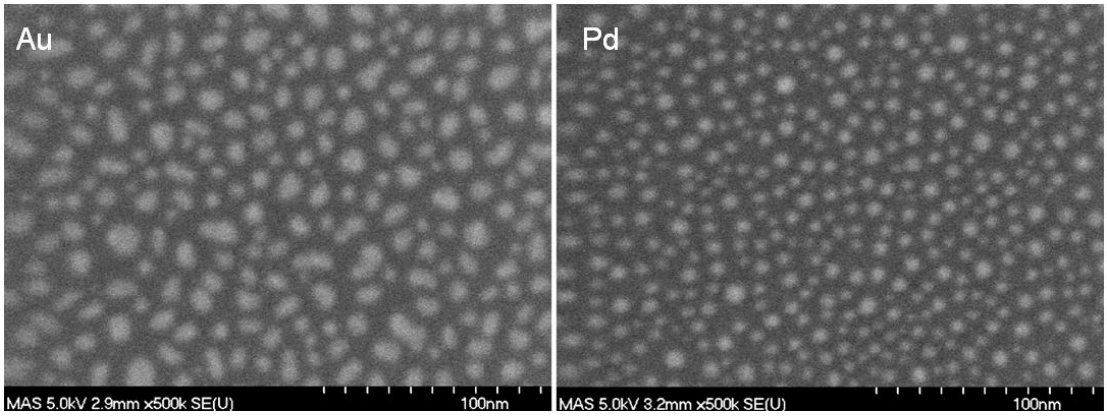


Figure 4.20: SEMs Comparing 10Å of Pd with 10Å of Au

The density of the gold islands is about 0.53 x 10^{12} particles cm^{-2}, while the density of the palladium islands is about 1.03 x 10^{12} particles cm^{-2}. This represents an important density milestone, since as previously mentioned, it has been theorized that the target density for nanocrystal non-volatile memory should be at least 10^{12} particles cm^{-2}, which would represent 100 nanocrystals in a 100nm x 100nm square area. [131] For the palladium nanocrystals shown in Figure 4.20, not only is this density exceeded, but even further scaling may be possible, perhaps even into the realm of single electron memory applications.

The next film property to consider is average particle area, which is shown in Figure 4.21 as the thickness of the evaporated palladium decreases.

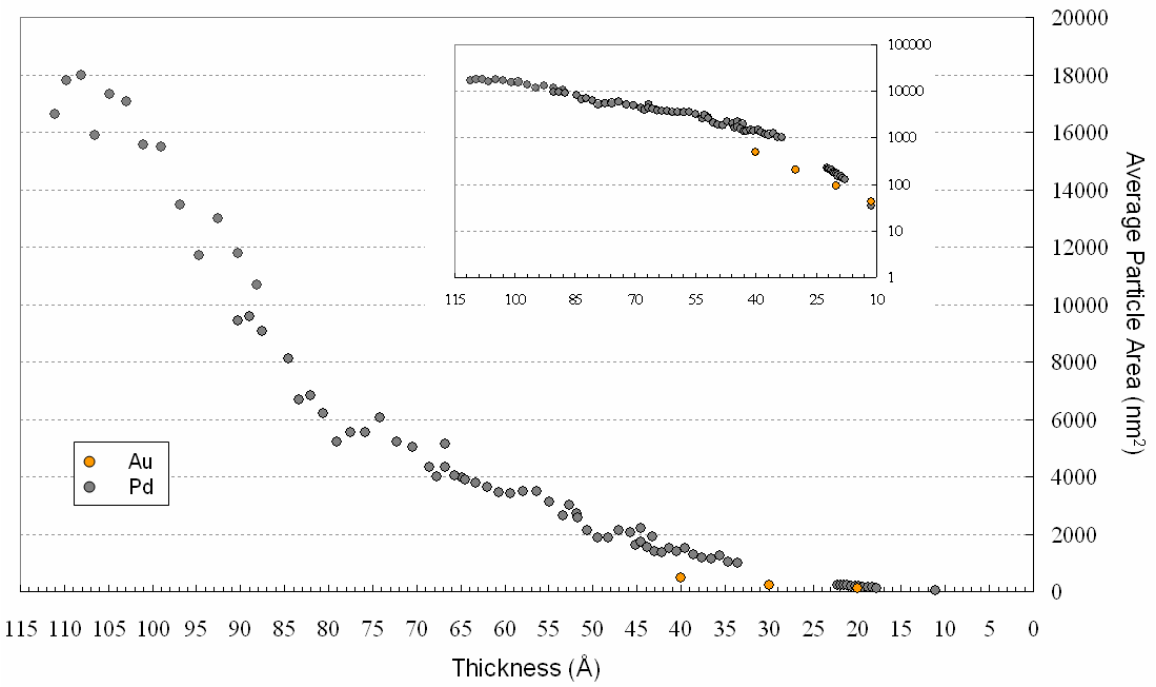


Figure 4.21: Average Particle Area (nm^2) vs. Evaporated Film Thickness

As expected from the density analysis, the thinner evaporated palladium results in smaller particles sizes. From the log inset, the thinnest evaporated film of 10Å results in an average particle area of about $30nm^2$. Unfortunately, this data could not be obtained from the previous high magnification images, as the resolution and signal contrast were not high enough for an accurate area analysis but were sufficient for accurate particle counts. Therefore, to attain this data, 10Å of palladium was evaporated onto Protochips DuraSiN™ Films. These films provide low scatter substrates enabling quantitative transmission electron microscopy analysis. The samples were annealed and then imaged by Materials Analytical Services using a Hitachi HD2000 STEM. A high resolution image of one of these samples is shown in Figure 4.22.

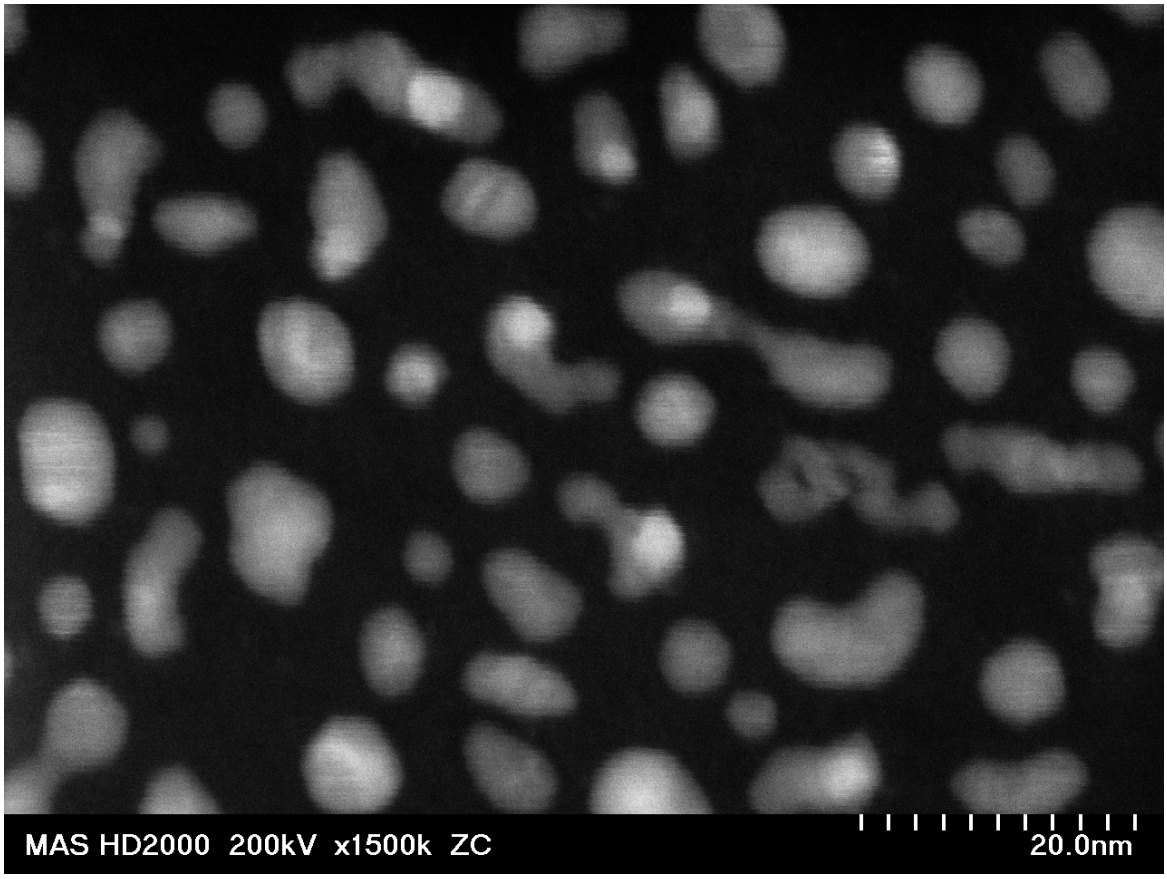


Figure 4.22: High Magnification STEM of 10Å Pd

Assuming spherical particles, the average particle diameter was about 6.3 ± 1.8 nm. The distribution of these particle diameters is shown in Figure 4.23.

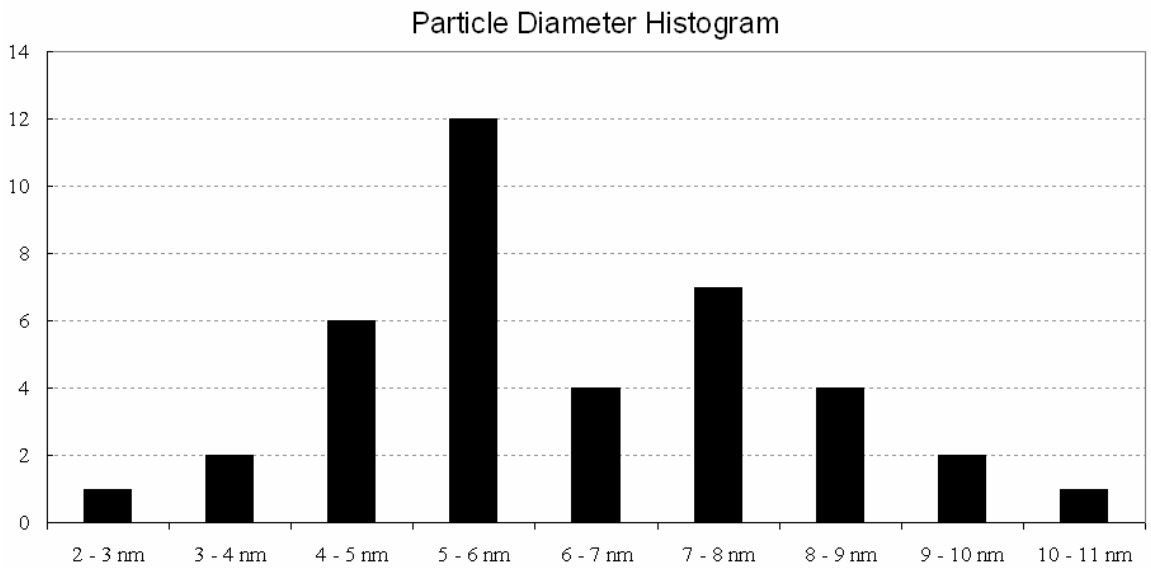


Figure 4.23: Particle Diameter Histogram for 10Å Pd

From this figure, it is clear that the overwhelming majority of particles, 29 out of 39 particles, have a diameter between 4-8nm. However, thirty-nine particles in the image area depicted in Figure 4.22 represents a density of only about $8x10^{11}$ particles cm^{-2}, significantly below the $1.0x10^{12}$ particles cm^{-2} previously achieved for this evaporation thickness. There are several possible explanations for this difference, the first of which involves systematic error in the image analysis. Figure 4.22 is at such a high resolution that a significant percentage of particles are located on the edge of the image and therefore not counted. Including all fourteen edge particles over-inflates the particle count resulting in a particle density of about $1.08x10^{12}$ particles cm^{-2}. Clearly for an accurate particle count, an image at a smaller magnification is necessary, as shown in Figure 4.24.

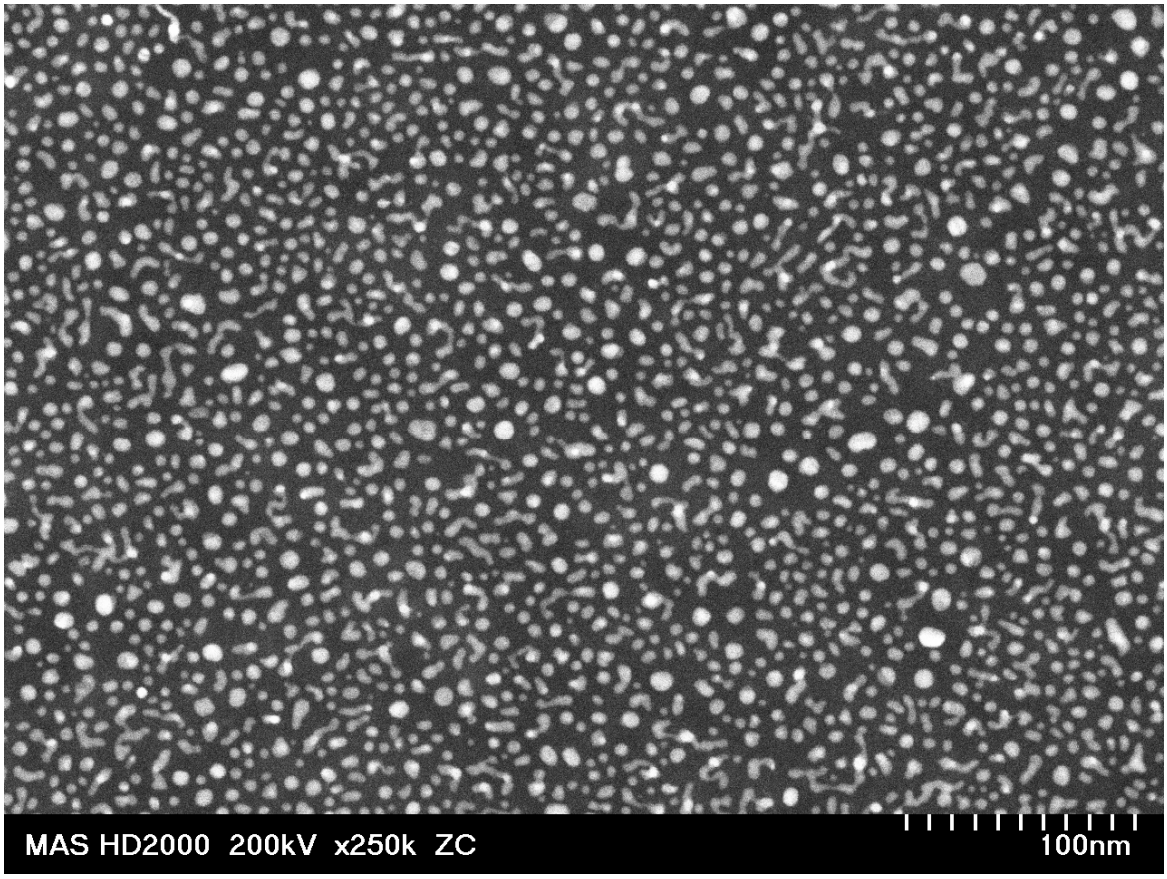


Figure 4.24: Low Magnification STEM of 10Å Pd

Images from four different locations on the DuraSiN^{TM} films substrate were taken and analyzed resulting in an average particle density of about 9.39×10^{11} particles cm^{-2}. This is still below the target density achieved previously. A possible reason for this would be the difference in substrates. It was previously shown that statistically significant differences in film morphology existed when gold was evaporated onto a 1-10 Ω-cm silicon boron-doped wafer with 1000Å of silicon dioxide grown in a wet thermal process compared to films evaporated onto a 0.01 Ω-cm silicon heavily boron-doped wafer with a 37Å silicon dioxide grown in a dry thermal process. [130] These differences were attributed to surface effects due to the different density and surface roughness of the oxide. Clearly the silicon nitride films of the STEM substrates are different than the wet

thermal 1000Å silicon dioxide surfaces used for the previous evaporations. In addition, the two substrates could have different thermal properties during the anneal.

It is worth mentioning that the electron beam in the E-beam Evaporator was adjusted before the evaporation onto the DuraSiN^{TM} Films. This adjustment was made to more centrally steer the beam into striking the crucible. This resulted in a noticeably higher evaporation rate which could have caused slightly more material to be deposited. Manually opening the shutter and resetting the thickness monitor introduces variation into the experiment. While the exponential dependence of the palladium particle density on the initial evaporated thickness enabled the target density to be achieved, it also represents a tradeoff in controllability. Very small variations in the initial evaporated thickness could result in statistically significant differences in the film morphology. Ideally, very slow evaporations rates would be used to improve the run-to-run repeatability.

Finally, a Brightfield image transmission electron micrograph of 10Å of Pd evaporated on the DuraSiN^{TM} films was taken to investigate the crystalline nature of these films, as shown in Figure 4.25.

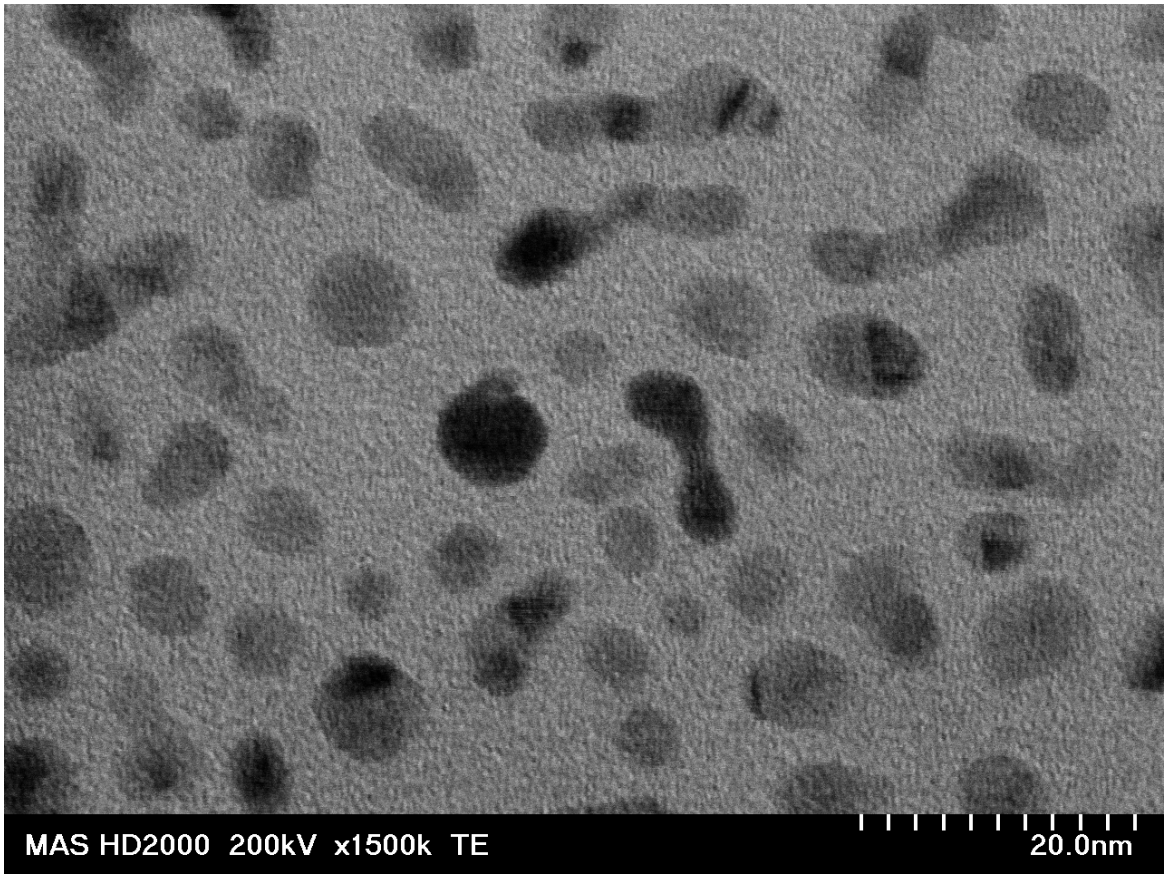


Figure 4.25: High Resolution Brightfield Image of 10Å Pd

On several of the smaller particles in this image, facets are noticeable which would indicate a crystalline structure. On many of the larger particles evidence possibly suggesting crystal twinning is noticeable. Therefore, it is believed that the palladium particles are polycrystalline in nature with some evidence of single grains.

4.6 High Density Evaporation Technique

As shown in the previous section, the target density for non-volatile memory applications of 1.0×10^{12} particles cm^{-2} was achieved. Suppose that even further density scaling was required. Clearly decreasing the initial evaporated thickness is one way to achieve higher densities, but it was also shown that for this exponential dependence, further reduction of the evaporation thickness could present some controllability issues. Alternatively, suppose there was an application in which a certain particle size was required at a target density. Thus far the density and particle size have been interdependent; that is, choosing one defines the other. In this section, a technique is described that permits further increases in particle density for a given particle size.

Figure 4.26(a) shows the standard morphology of a 50Å Pd film. In Figure 4.26(b), a film with approximately the same average particle size but with a much higher density is shown. A quantitative analysis of this image is complicated by the increased density since it becomes difficult to determine which islands are connected. That being said, the average particle area of the two films agreed and was approximately $3000 nm^2$ per particle. The density of the original film was about 80 particles μm^{-2} while the high-density film is about 140 particles μm^{-2}, which considering that there is an increased number of edge particles in the higher density film, could be undervaluing the true value.

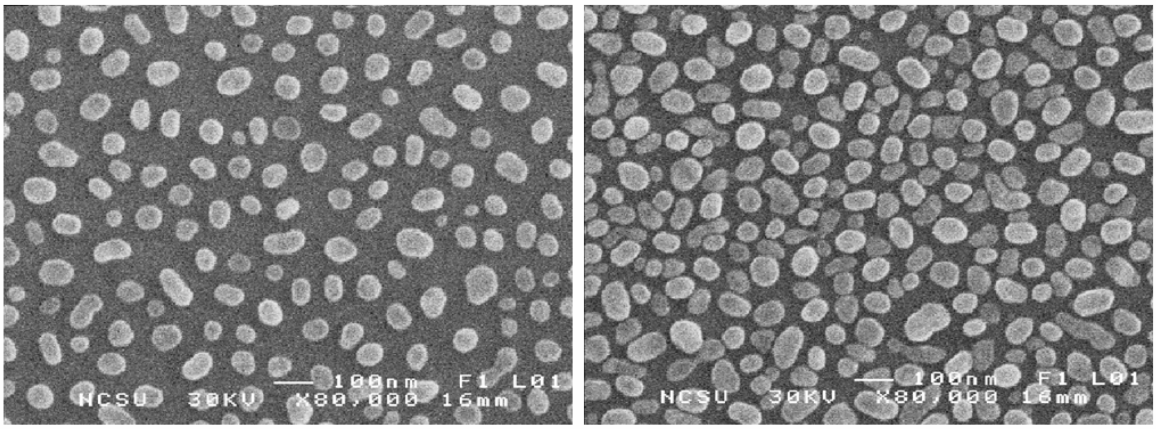


Figure 4.26: Controlling the Particle Density (a) Straight Evaporation, (b) High Density Technique

Now consider that in Figure 4.26(b), the inter-particle spacing has significantly decreased. Perhaps this technique could be utilized for the realization of the original NanoCell concept in which the islands would be so dense that molecules could directly bridge their gaps rather than requiring overlaying functionalized nanowires. While these are just some possible applications for this process, clearly this represents a clear path to achieve higher density discontinuous metal films.

4.7 Summary

In this chapter, the controlled formation of discontinuous palladium islands was presented. Numerous experiments were performed to ensure that relatively accurate and reproducible film thicknesses were being deposited in the E-beam evaporator. This involved verifying the tooling factor for the system as well as investigating the material parameters of palladium. The process to make these films discontinuous involved post-deposition heat treatments. The resulting film morphology dependency on the temperature, heat pulse duration, and initial film thickness was analyzed. As long as the films were heated above a certain activation temperature for a certain duration, they

seemed to reach a final equilibrium or steady-state morphology. This suggests the existence of some local minimum energy state which bodes well for controllability. The final morphology was largely governed by the initial evaporated thickness. Based on this control, different morphologies were engineered for several different nanotechnology applications.

The first application for these palladium discontinuous films was for use in the NanoCell. Films were fabricated such that molecularly functionalized palladium nanorods could bridge palladium islands. The structures were electrically discontinuous, permitting current to pass only between the functionalized nanorods and not between the islands themselves. During the patterning of these structures, an interesting effect was observed in which the smaller patterned areas did not reach the expected steady-state morphology. In fact, the film morphology for these devices became pattern density dependent. It is believed that the nearby patterns act as heat sources for these smaller patterns. In all cases, the morphology of larger patterns resembled that of the blanket evaporation, suggesting that there is a pattern size limit in which the films resemble infinite sheets and pattern density has no effect. Several possible applications in which this effect could be exploited were then suggested. Ideally, using this pattern density effect could potentially result in wafer-scale morphology control with only a single evaporation.

Next, application of discontinuous metal films for non-volatile memory was discussed. Several advantages over traditional continuous floating gate devices and even over silicon nanocrystal counterparts were identified. However, to exploit these advantages, several requirements on the film morphology existed; including a high particle density and good particle uniformity. Along these lines, several experiments were conducted to establish the thickness uniformity using our process in the E-beam evaporator. Once this was established, electrical testing of gold nanocrystal capacitors was performed. The hysteretic CV curve typical of floating gate memory was measured. No such hysteresis existed in control devices without the discontinuous gold film. It was also noticed, that as the evaporated film thickness decreased across the wafer, the flat band voltage shift increased. In fact, for a theoretical difference of only about 2Å across

the wafer, statistically significant increases in the flat band voltage shift were observed. This suggested that even further scaling of the gold islands could lead to even more substantial improvements in the flat band voltage shift. It is with this motivation that experiments were performed to try and further scale both the gold and palladium islands.

Numerous experiments were preformed to investigate the scaling of palladium islands. When compared to gold, it was obvious that the gold scaled linearly with decreasing evaporation thickness, while the palladium scaled exponentially. At thicknesses below about 15Å, the palladium actually outscaled the gold. In fact, at 10Å, the palladium island density was greater than the theoretical target density for nanocrystal memories of $1.0x10^{12}$ particles cm^{-2}. Not only did palladium outscale gold, but palladium has a higher melting point and is more amenable to back-end processing, resulting in easier integration with standard semiconductor manufacturing. The average particle diameter was then investigated for palladium islands was found to be about 6.3 ± 1.8 nm. The crystalline nature of the film was then investigated using Protochips DuraSiN™ Films that provided low scatter substrates enabling quantitative transmission electron microscopy analysis. From these images, it is believed that the palladium islands are polycrystalline in nature.

Finally, a novel technique was presented in which the densities of these films could be increased almost limitlessly. Several possible applications for these films were suggested, including the original concept of the NanoCell. Overall, the ability to engineer these morphologies based on different application requirements was demonstrated, showing tremendous control over the film morphology. It is this control that will enable discontinuous metal films to be successfully utilized in various applications in Nanotechnology.

Chapter 5

Conclusions and Future Work

Interface strategies for Nanotechnology have generally required either nanoprecision alignment, which remains very challenging; or stochastic assembly, which can result in incomplete connectivity. In this dissertation, a structure was presented that permits fully deterministic cross-connect of orthogonal wiring arrays without the need for any critical translational alignment. Rather than mask alignment precision, the challenge of pitch reduction is shifted to the ability to fabricate structures at the micrometer-scale. Target nanowires can be deterministically interconnected with only a micrometer-precision alignment. In addition, there is no restriction placed on the minimum nanowire pitch and the design is independent of the technology used to fabricate the nanowires. The process is relatively simple and is presented from a fabrication perspective, critically addressing the effect of potential processing errors on the structure. A proof-of-concept structure was successfully fabricated and characterized demonstrating the feasibility of this design. Possible directions for future work include fabricating the structures and purposely misaligning the connecting wires to physically demonstrate the novelty of this design. In addition, nanowires smaller than the 600nm proof-of-concept wires could be fabricated to validate this design at the nanoscale. The alternate process flow using multi-level nanoimprinting to eliminate the insulator cut level, and thus the strictest limitation to the scalability of this design, could be demonstrated. Finally, applying this interface strategy to test novel nanofabrication techniques, such as the planar edge defined alternate layer (PEDAL) process utilized to fabricate nanowires, would demonstrate the practical utility of this design.

While discontinuous metal films have been used for stochastic nanowire interface strategies, this represents only one of the numerous applications for these films in the field of Nanotechnology. The versatility in the application of these films is based on the ability to control their morphology. In this dissertation, tremendous control of the morphology of discontinuous palladium films was demonstrated as the morphology was

tailored for various applications. First, the films were successfully engineered to provide molecular scaffolding in the NanoCell. During the fabrication of these devices, a dependency of the film morphology on the pattern density was observed. It was suggested that this dependence could potentially be exploited to provide wafer-scale morphology control with only a single evaporation. Next, application of these films for non-volatile memory was tested with the fabrication of gold nanocrystal capacitors. Electrical characterization of these devices revealed a strong flat band voltage shift dependence on the particle density. In fact, the flat band voltage shift increased significantly with only minimal increases in the particle density. This suggests that further scaling of the nanocrystal density could result in further device optimization. Therefore, the scaling of gold and palladium films was investigated. It was found that while the gold particle density increased linearly with decreasing initial evaporation thickness, the palladium particle density increased exponentially. The theoretical target density for nanocrystal non-volatile memory is $1.0x10^{12}$ particles cm^{-2}. For palladium nanocrystals, not only was this density exceeded, but potential for even further scaling is anticipated, perhaps even into the realm of single electron memory applications. In addition to high scalability, palladium has a high-melting point and is amenable to back-end processing, resulting in easier integration with standard semiconductor manufacturing. A novel technique was developed and demonstrated that could increase the particle density if required.

Clearly, there are design tradeoffs incorporated into the theoretical target density for nanocrystal non-volatile memory. For example, the inter-particle distance impacts data retention since it affects the amount of lateral charge redistribution. An obvious direction would be to build a device model in which these design tradeoffs could quickly be analyzed. Ideally this would establish additional film morphology requirements that could be tailored for device optimization. It was shown that as the gold particle size scaled, the flat band voltage shift increased. It was then shown that palladium outscales gold discontinuous films. An obvious next step would be to fabricate and characterize palladium nanocrystal capacitors using the conditions that resulted in the theoretical target density. One natural question that arises is how much further can the palladium

continue scaling, and what benefit, if any, does this have for non-volatile memory applications. Another advantage of comparing palladium with gold is that they have similar bulk work functions, 5.12 and 5.1 respectively, which potentially represents an ideal control in isolating the effect island morphology has on the electrical characteristics of these devices. Understanding how the morphology affects device performance will enable one to determine fabrication requirements for the manufacturability of such devices as well as identify potentially successful fabrication strategies. In addition, understanding this dependence will enable device performance optimization.

Another possible direction for future research includes further investigation of the pattern density effect. It was suggested that wafer-scale surface plasmon resonance tuning could be achieved exploiting this effect. To these ends, a mask was designed to test this concept in hopes of achieving this with only a single evaporation. Samples are currently being fabricated and tested. Finally, perhaps the novel high density technique could be employed for the realization of the original NanoCell concept in which the islands would be so dense that molecules could directly bridge their gaps rather than requiring overlaying functionalized nanowires. Overall, there are many directions this research can be taken, a reflection of the numerous applications discontinuous metal films have in Nanotechnology.

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Appendix

A Supporting Theory for Fanout and Interconnect Structure

A.1 Example System NOT at the Target Insulator Cut Angle

Figure A.1 shows an example of the connectivity problems that can arise from a system in which the target insulator cut angle derived in Equation 3.2 is not achieved.

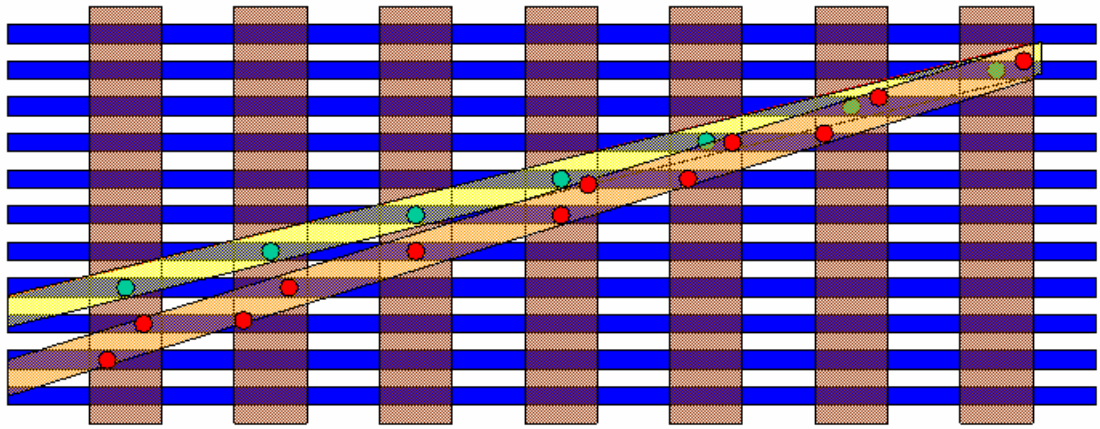

Figure A.1: Example System NOT at the Target Cut Angle

The yellow cut in the above figure is made at the target cut angle. Notice how each vwire connects (symbolized by green circles) one and only one hwire. Alternatively, the red cut is made at some angle greater than the maximum pitch angle. Notice how five of the seven vwires connect (symbolized by red circles) more than one hwire. There are even three hwires that connect more than one vwire. Any deviation in the target cut angle results in a system whose connectivity becomes size dependent. Obviously this must be avoided if the novelty of the design is to be exploited.

A.2 Investigating the Cut Width

While clearly the optimal cut width should be targeted, it is important to derive the bounds on the cut width to understand the allowable fabrication tolerance. The maximum cut width before shorting is guaranteed is derived with the help of Figure A.2.

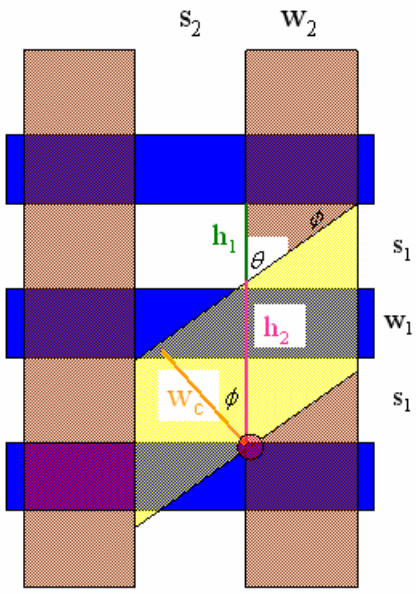

Figure A.2: Deriving the Maximum Cut Width

If the cut width is too wide, one vertical wire could potentially connect multiple horizontal wires. In the example above, the right most vwire would short the two bottom hwires. To avoid this, there must be a condition on the vertical distance the cut travels over the width of the vertical wire, w_2:

$h_1 + h_2 < s_1 + w_1 + s_1$, where $h_1 = w_2 \tan \phi$ and $h_2 = w_c / \cos \phi$, and thus:

$w_2 \tan \phi + w_c / \cos \phi < s_1 + w_1 + s_1$, and solving for w_c results in:

$$w_c < (2s_1 + w_1 - w_2 \tan f)\cos f \qquad \textit{Equation A.1}$$

This is the width that if exceeded guarantees that multiple hwires will be intersected by one vwire. A sanity check reveals that for $\phi=0^o$, $w_c < 2s_1 + w_1$, which makes physical sense being that if the cut is wider than this, it would intersect multiple hwires. Notice that this does *not* guarantee that a cut thinner than this will not short, but only guarantees that if this cut width is exceeded, there will definitely be shorting. Now

the focus is turned to deriving the minimum cut width, i.e. the width necessary to connect to at least one hwire over each pitch, which is derived with the help of Figure A.3.

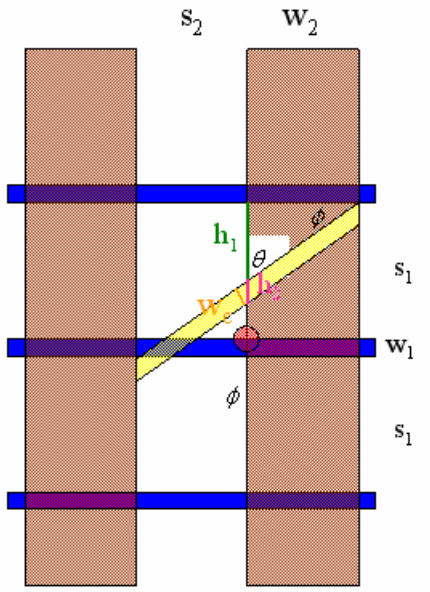

Figure A.3: Deriving the Minimum Cut Width

If the cut is too narrow, the vertical wire may not intersect the target horizontal wire. In the example above, the cut misses the target connection between the right most vwire and the middle hwire. To avoid this, there must be a minimum condition on the vertical distance the cut travels over the width of the vertical wire, w_2:

$h_1 + h_2 > s_1$, where $h_1 = w_2 \tan \phi$, and $h_2 = w_c / \cos \phi$, and thus:

$w_2 \tan \phi + w_c / \cos \phi > s_1$, and solving for w_c results in:

$$w_c > (s_1 - w_2 \tan f)\cos f \qquad \textit{Equation A.2}$$

This is the cut width that guarantees that at least one hwire is connected. A sanity check reveals that for $\phi=0^o$, $w_c > s_1$, which makes physical sense being that if the cut were thinner than this, there would be no guarantee that it would connect an hwire.

Another important cut width to consider is the minimum cut width to achieve the maximum contact area. Depending on the dimensions of the two sets of wires and the alignment, the contact area may be very small, resulting in a large contact resistance. It would therefore be desirable to utilize the maximum contact area. The minimum contact width such that the full contact area is used is derived below with the help of Figure A.4.

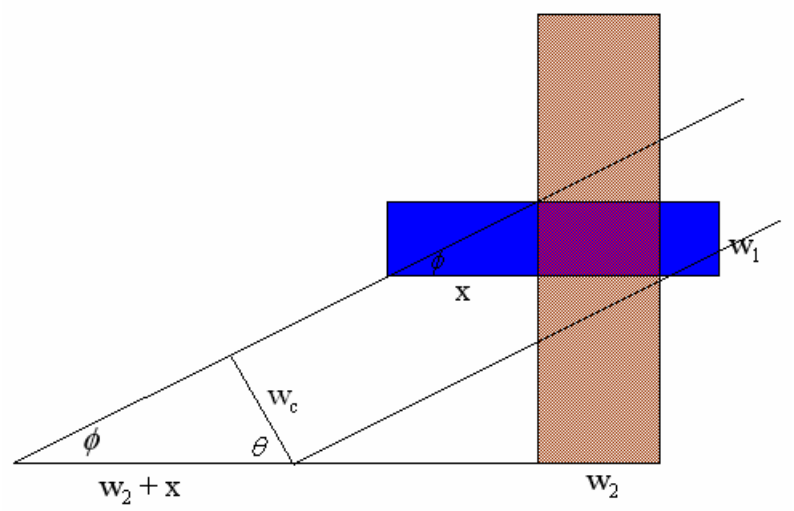

Figure A.4: Deriving the Minimum Cut Width to Maximize the Contact Area

Notice that the entire area made by the intersection of w_1 and w_2 is opened up for contact. From this graph:

$x = w_1 / \tan \phi$, $w_c = (w_2 + x) \sin \phi$, solving for w_c:

$w_c \geq (w_2 + w_1 / \tan \phi) \sin \phi$, and distributing the sin and rearranging:

$$w_c \geq w_1 \cos f + w_2 \sin f \qquad \textit{Equation A.3}$$

Now, revisiting the maximum cut width equation, one can derive an alternate form using the Equation 3.1:

$w_c < (2s_1 + w_1 - w_2 \tan \phi) \cos \phi$; now expanding and regrouping terms…

$w_c < s_1 \cos \phi + (s_1 + w_1) \cos \phi - w_2 \sin \phi$

Using Equation 3.1 ($(s_2 + w_2) \tan \phi = (s_1 + w_1)$), substitute for $(s_1 + w_1)$:

$w_c < s_1 \cos \phi + ((s_2 + w_2) \tan \phi) \cos \phi - w_2 \sin \phi$, distributing the cos and regrouping:

$w_c < s_1 \cos \phi + s_2 \sin \phi + w_2 \sin \phi - w_2 \sin \phi$, canceling out terms:

$$w_c < s_1 \cos f + s_2 \sin f \qquad \textit{Equation A.4}$$

It is interesting comparing this version of the maximum cut width to the minimum cut width needed to maximize the contact area. They are similar inequalities except that the max cut width depends upon the spacing, while the minimum cut width needed to maximize the contact area depends on the wire widths, which makes intuitive sense. For equal pitches there will be a tradeoff in these equations.

The equations derived above are explored in Figure A.5 versus the insulator cut angle for a system with a 20nm equally distributed nanowire pitch and an equally distributed vertical wire pitch.

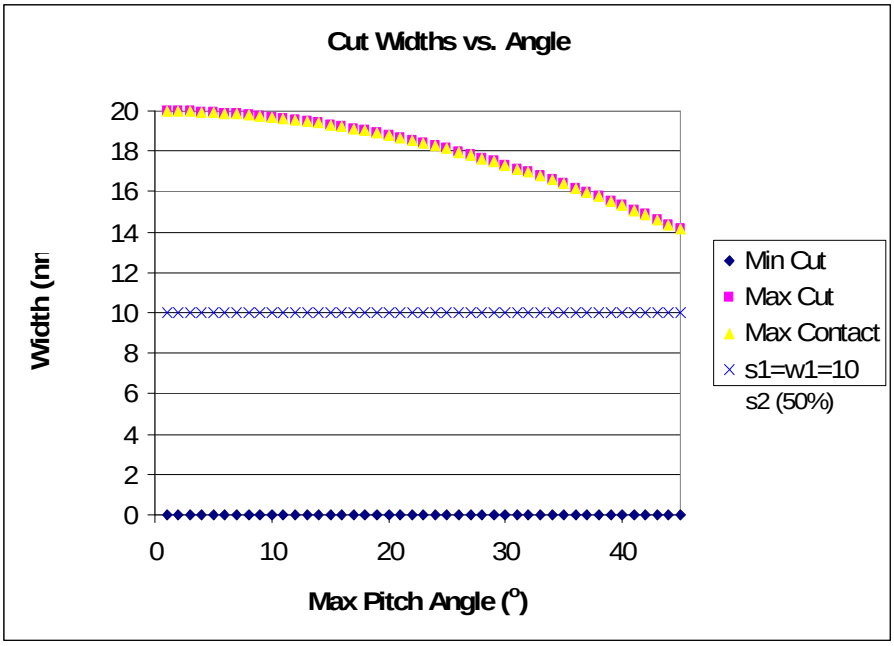

Figure A.5: Exploring the Derived Cut Widths

At very small angles, the maximum cut width is about twice the size of the nanowires. However, the minimum or optimal cut width for this system is zero. This implies that the dimensions of this system would not be able to exploit the novelty of this design. Figure A.6 depicts a system with an optimal cut width of no dimension.

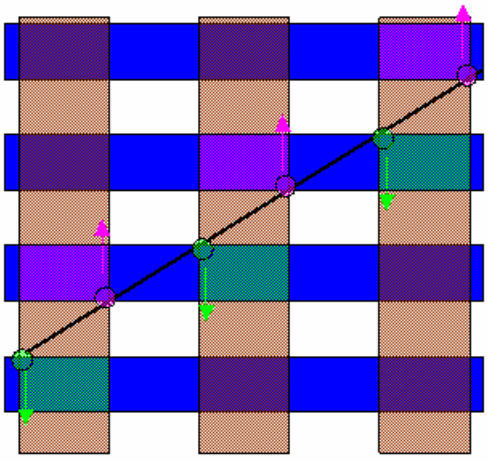

Figure A.6: Example of a System with an Optimal Cut Width of Zero

If there is any width to the cut, the possibility will exist to connect both the green and purple junctions at the same time. The cause of this was that both half-pitches were equal. Remember that the optimal cut width is given as:

$w_c = (s_1 - w_2 \tan \phi) \cos \phi$, and the target cut angle is:

$(s_2 + w_2) \tan \phi = (s_1 + w_1)$, now considering equal half-pitches ($s_1=w_1$ and $s_2=w_2$):

$2s_2 \tan \phi = 2s_1$, canceling out terms:

$s_2 \tan \phi = s_1$, now with $s_2=w_2$ this becomes:

$w_2 \tan \phi = s_1$, and substituting this into the optimal cut width results in:

$w_c = (s_1 - w_2 \tan \phi) \cos \phi$, or $w_c = (s_1 - s_1) \cos \phi$ or $w_c = 0$.

Thus distributing the pitch equally between the spacing and wired width will not permit the novelty of the design. Since the spacing and wire width must be different, the

following analysis investigates the effects of increasing the spacing versus increasing cut width. Figure A.7 demonstrates the impact of increasing the spacing.

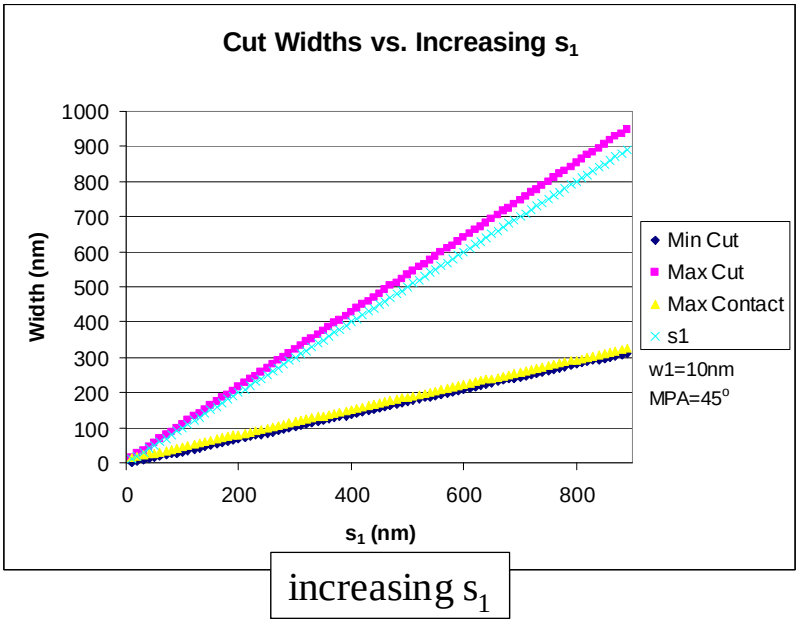

Figure A.7: Impact of Increasing the Spacing on the Cut Width

In the above figure, w_1 is held constant and s_1 is increased. The maximum cut width follows s_1 very closely, while the optimal cut width and the minimum cut width to get the maximum contact area increase, but at a smaller rate. This is compared to the impact of increasing the wire width while holding the spacing constant, as demonstrated in Figure A.8.

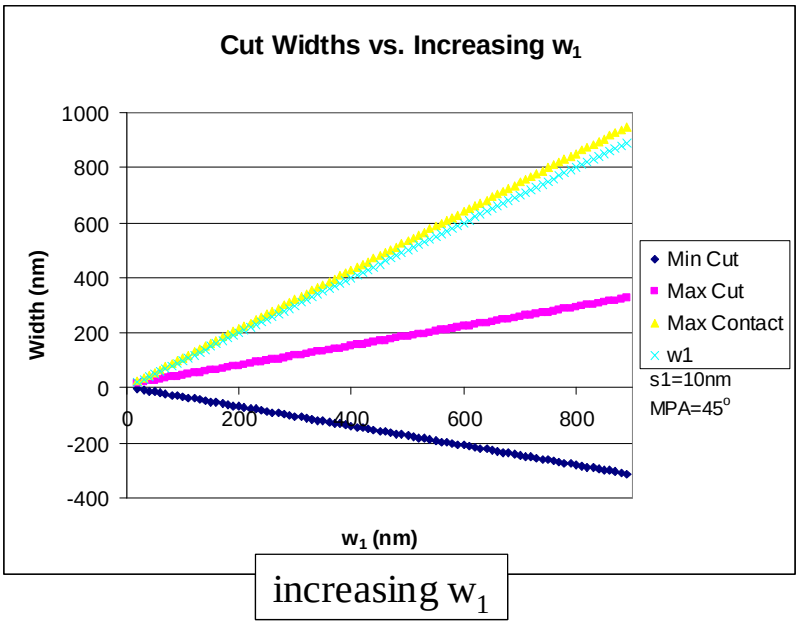

Figure A.8: Impact of Increasing the Wire Width on the Cut Width

From this figure, the minimum cut width to maximize the contact area is greater than the maximum cut, implying there is no way to maximize the contact area. Also shown for this system is that the optimal cut width is negative, which is clearly non-physical. Figure A.9 depicts a system with a negative optimal cut width.

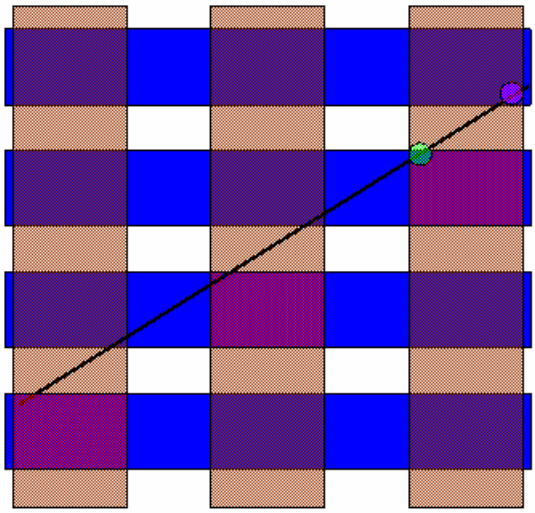

Figure A.9: Example of a System with a Negative Optimal Cut Width

Notice in this figure that an infinitely thin cut is already shorting multiple junctions. Of course, a vertical shift of the cut would result in a correctly connected system. Unfortunately, this 'shift' is akin to an alignment, so while a negative optimal cut width can still give full one-to-one connectivity, it cannot guarantee it without alignment. Thus, increasing the wire width will not exploit the novelty of the deisgn. Clearly it is desirable to increase the spacing rather than the wire width. Figure A.10 investigates the distribution of a constrained nanowire pitch into the spacing.

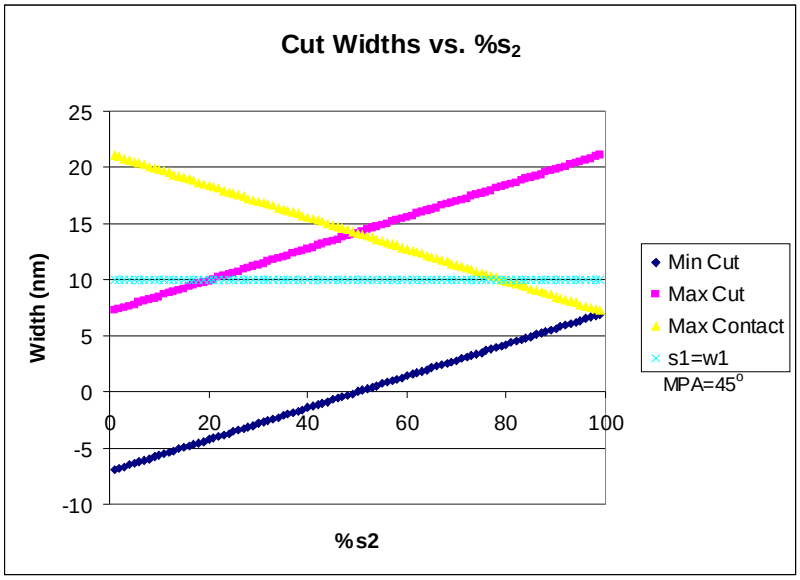

Figure A.10: Examining the Effect of the Distribution of the Pitch on the Cut Width

When a higher percentage of the total pitch is distributed into the wire width, all of the points less than 50% on the x-axis, the same trends are seen as they were with simply increasing the wire width. The minimum cut width to maximize the contact area is greater than the maximum cut width and the optimal cut width is non-physical. Clearly distributing more of the pitch into the spacing is preferable, and necessary to exploit the novelty of this design.

A.3 Limitations on the Pitch Distribution

The optimal cut width was derived in Equation 3.4 as:

$$w_c = (s_1 - w_2 \tan f)\cos f$$

If $(w_2 \tan \phi)$ is greater than s_1, the optimal w_c becomes negative, which obviously is non-physical. Thus, the following condition on the wire width, w_2, is given:
$w_2 < s_1 / \tan \phi$, or similarly starting from $w_2 \tan \phi < s_1$, add to both sides $(s_2 + w_2) \tan \phi$:
$w_2 \tan \phi + (s_2 + w_2) \tan \phi < s_1 + (s_2 + w_2) \tan \phi$, now expanding terms on the right side:
$w_2 \tan \phi + (s_2 + w_2) \tan \phi < s_1 + s_2 \tan \phi + w_2 \tan \phi$, subtracting $w_2 \tan \phi$ from both sides:
$(s_2 + w_2) \tan \phi < s_1 + s_2 \tan \phi$, using Equation 3.1, substitute $(s_1 + w_1)$ for the left side:
$s_1 + w_1 < s_1 + s_2 \tan \phi$, subtracting s_1 from both sides:
$w_1 < s_2 \tan \phi$.

Thus, the following two equivalent conditions must be met to exploit the novelty of this design:

$$w_1 < s_2 \tan f,\ w_2 < \frac{s_1}{\tan f} \qquad \textit{Equation A.5}$$

A.4 Equivalence of the Optimal Dimensions

To prove the equivalence of the optimal cut width and the optimal wire width, it is shown that the cut width for both the optimal space and optimal wire width; is the optimal cut width. To start, it is shown that w_c in the optimal s_2 is the optimal cut width.
Starting with $s_2 = w_1 / \tan \phi + w_c / \sin \phi$, solve for w_c:
$w_c = (s_2 - w_1 / \tan \phi) \sin \phi$, now distributing the $\sin \phi$:

$w_c = (s_2 \sin \phi - (w_1 \sin \phi) / \tan \phi)$, now multiplying by $\cos \phi / \cos \phi$:

$w_c = [(s_2 \sin \phi - (w_1 \sin \phi) / \tan \phi)] (\cos \phi / \cos \phi)$, distributing the $\cos \phi$ denominator:

$w_c = (s_2 \tan \phi - (w_1 \tan \phi) / \tan \phi)] \cos \phi$, reducing the second term:

$w_c = (s_2 \tan \phi - w_1) \cos \phi$, adding and subtracting the term $w_2 \tan \phi$:

$w_c = (s_2 \tan \phi + w_2 \tan \phi - w_2 \tan \phi - w_1) \cos \phi$, using Equation 3.1:

$w_c = (s_1 + w_1 - w_2 \tan \phi - w_1) \cos \phi$, canceling w_1 terms:

$w_c = (s_1 - w_2 \tan \phi) \cos \phi$, which is the equation for the optimal cut width.

Now it is shown that the w_c in the optimal w_2 is the optimal cut width.

Starting with $w_2 = s_1 / \tan \phi - w_c / \sin \phi$, solve for w_c:

$w_c = (s_1 / \tan \phi - w_2) \sin \phi$, now multiplying by $\cos \phi / \cos \phi$,

$w_c = (s_1 / \tan \phi - w_2) \sin \phi (\cos \phi / \cos \phi)$, distributing in the outside term:

$w_c = (s_1 / \tan \phi - w_2) \tan \phi \cos \phi$, distributing the $\tan \phi$ term inside:

$w_c = (s_1 - w_2 \tan \phi) \cos \phi$, which is the equation for the optimal cut width!

Thus, the equivalence between the optimal cut width and the optimal pitch has been proven. Not only are the equations equivalent, but also the conditions necessary to exploit the novelty of this structure are equivalent. For example, it was shown that the target insulator cut angle had to be achieved so that the oxide cut could keep up with the pitch of the wires. Therefore, this requirement must be satisfied by the optimal pitch equations if they are equivalent. Below shows that the optimal pitch satisfies Equation 3.1:

$s_2 + w_2 = (w_1 / \tan \phi + w_c / \sin \phi) + (s_1 / \tan \phi - w_c / \sin \phi)$, cancel out the $w_c / \sin \phi$ terms:

$s_2 + w_2 = w_1 / \tan \phi + s_1 / \tan \phi$, take out $\tan \phi$ term from right and multiply into left:

$(s_2 + w_2) \tan \phi = w_1 + s_1$, which is Equation 3.1.

Another condition guaranteed that the cut width be non-negative. This required that the following condition must be met, $w_2 > s_1 / \tan \phi$. Notice the similarity between this condition and the optimal wire width, $w_2 = s_1 / \tan \phi - w_c / \sin \phi$. If the original condition is not met, this would imply that the term $w_c / \sin \phi$ is negative, which would be non-physical. Thus, it has been shown that the optimal pitch and the optimal cut width are equivalent, and the conditions on the two equations are similarly equivalent.

A.5 Investigating the Alignment Tolerance

The optimal cut width, w_c, is inserted into the equations for HD and VD to determine the alignment tolerances for the optimal dimensions:

$HD = s_2 + s_1 / \tan \phi - w_c / \sin \phi$, where plugging in the optimal w_c, $(s_1 - w_2 \tan \phi) \cos \phi$:

$HD_{opt} = s_2 + s_1 / \tan \phi - ((s_1 - w_2 \tan \phi) \cos \phi) / \sin \phi$, combining the sin and cos:

$HD_{opt} = s_2 + s_1 / \tan \phi - ((s_1 - w_2 \tan \phi) / \tan \phi$, expanding and distributing the tan:

$HD_{opt} = s_2 + s_1 / \tan \phi - s_1 / \tan \phi + w_2$, canceling out the $s_1 / \tan \phi$ term:

$HD_{opt} = s_2 + w_2$, which is simply the vertical wire pitch.

This is intuitive since the optimal pitch was designed for this very feature; that is over every vertical wire pitch the hwire connection just shifts over one vwire, and thus no alignment is necessary. After this result, it is expected that VD_{opt} will be the horizontal wire pitch. That derivation is shown below:

$VD = s_1 + s_2 \tan \phi - w_c / \cos \phi$, where plugging in the optimal w_c, $(s_1 - w_2 \tan \phi) \cos \phi$:

$VD_{opt} = s_1 + s_2 \tan \phi - ((s_1 - w_2 \tan \phi) \cos \phi) / \cos \phi$, canceling out the cos:

$VD_{opt} = s_1 + s_2 \tan \phi - s_1 + w_2 \tan \phi$, canceling out the s_1 terms:

$VD_{opt} = s_2 \tan \phi + w_2 \tan \phi$, applying the Equation 3.1 equality:

$VD_{opt} = s_1 + w_1$, which is the horizontal wire pitch.

Thus, under optimal conditions, the alignment must fall within the respective pitches to guarantee a target connectivity. Every pitch shift in the cut results in the connection between successive wires. Now consider the displacement if the maximum cut width is used. Intuition would suggest that there is no tolerable allowance if the cut is as wide as possible.

$HD = s_2 + s_1 / \tan \phi - w_c / \sin \phi$, plug in the maximum w_c, $(2s_1 + w_1 - w_2 \tan \phi) \cos \phi$:

$HD = s_2 + s_1 / \tan \phi - ((2s_1 + w_1 - w_2 \tan \phi) \cos \phi) / \sin \phi$, combining cos and sin:

$HD = s_2 + s_1 / \tan \phi - (2s_1 + w_1 - w_2 \tan \phi) / \tan \phi$, distributing tan:

$HD = s_2 + s_1 / \tan \phi - 2s_1 / \tan \phi - w_1 / \tan \phi + w_2$, canceling one $s_1 / \tan \phi$:

$HD = s_2 + w_2 - s_1 / \tan \phi - w_1 / \tan \phi$, applying Equation 3.1:

$HD = s_2 + w_2 - (s_2 + w_2)$: canceling out:

$HD = 0$, which makes sense. Now calculating the VD:

$VD = s_1 + s_2 \tan \phi - w_c / \cos \phi$, plugging in the maximum w_c, $(2s_1 + w_1 - w_2 \tan \phi) \cos \phi$:

$VD = s_1 + s_2 \tan \phi - ((2s_1 + w_1 - w_2 \tan \phi) \cos \phi) / \cos \phi$, canceling out the cos:

$VD = s_1 + s_2 \tan \phi - 2s_1 - w_1 + w_2 \tan \phi$, canceling out one $-s_1$ and rearranging:

$VD = s_2 \tan \phi + w_2 \tan \phi - (s_1 + w_1)$, applying Equation 3.1:

$VD = s_1 + w_1 - (s_1 + w_1)$, canceling out:

$VD = 0$.

Thus, as expected, if the maximum cut width is used, there is no displacement tolerance, since the cut width already occupies the entire window.

From the alignment displacement window, it would appear that the center alignment would be preferred. This would allow for the maximum tolerance in any direction, assuming any misalignment to be random. To accomplish this, it would be necessary to ensure that the horizontal and vertical displacements are equal both above and below the cut, as illustrated in Figure A.11.

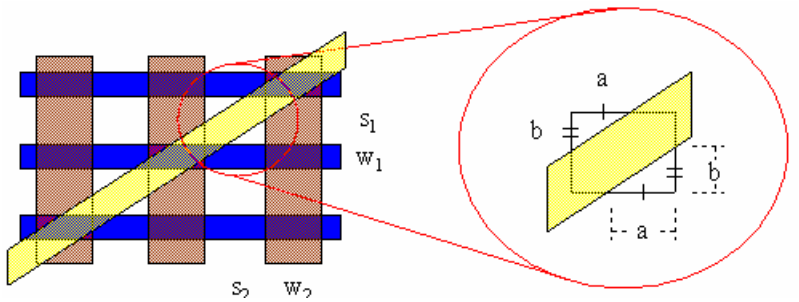

Figure A.11: Defining the Center Alignment

Obviously, for the center alignment, it is assumed that $HD_c = ½HD$ and $VD_c = ½VD$. With the help of Figure A.12, the derivation for HD_c follows:

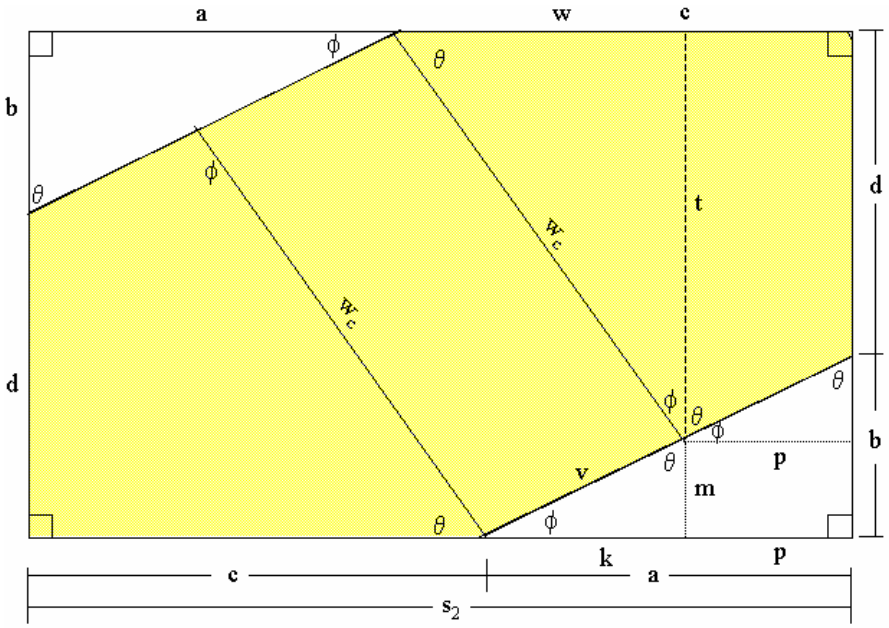

Figure A.12: Deriving the Center Alignment

From the graph, $w = w_c \sin \phi$, $t = w_c \cos \phi$, $m = s_1 - t$ and $k = m / \tan \phi$, plugging in: $k = (s_1 - w_c \cos \phi) / \tan \phi$, now $p + k = a = HD_c$, $p + w = c$, and $a + c = s_2$, therefore: $(p + k) + (p + w) = s_2$, which rearranging is $2p + k + w = s_2$, and solving for p:

$p = ½ (s_2 – k – w)$, now plugging this into $HD_c = ½(s_2 – k – w) + k$ or:

$HD_c = ½ (s_2 + k – w)$, now plugging in k and w:

$HD_c = ½ (s_2 + (s_1 – w_c \cos \phi) / \tan \phi – w_c \sin \phi)$, now distributing the $\tan \phi$:

$HD_c = ½ (s_2 + s_1 / \tan \phi – w_c \cos \phi / \tan \phi – w_c \sin \phi)$, reducing the $\cos \phi / \tan \phi$ term:

$HD_c = ½ (s_2 + s_1 / \tan \phi – w_c \cos^2 \phi / \sin \phi – w_c \sin \phi)$, multiply the last term by sin/sin:

$HD_c = ½ (s_2 + s_1 / \tan \phi – w_c \cos^2 \phi / \sin \phi – w_c \sin^2 \phi / \sin \phi)$, combining terms:

$HD_c = ½ (s_2 + s_1 / \tan \phi – w_c (\cos^2 \phi + \sin^2 \phi) / \sin \phi)$, substituting in for trig identity:

$HD_c = ½ (s_2 + s_1 / \tan \phi – w_c / \sin \phi)$, and concluding:

$HD_c = ½ HD$.

Thus, a center alignment, as defined above, results in half the overall tolerance in any direction. Assuming one does not have knowledge of any misalignment bias towards a certain direction, the center alignment should be targeted. Finally, this section will conclude with a graphical analysis of the allowable alignment tolerances, as shown in Figure A.13.

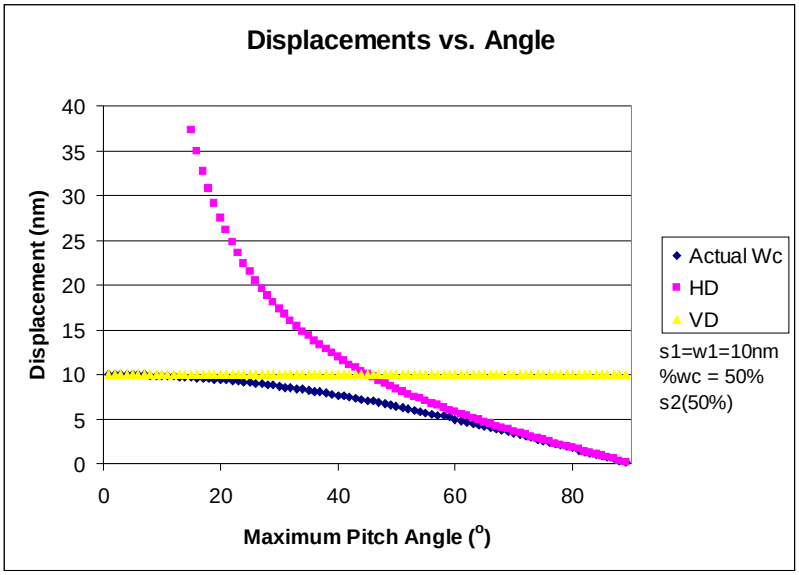

Figure A.13: Examining the Horizontal and Vertical Displacements

Unfortunately, any graph of the horizontal and vertical displacements depends largely on the system parameters, so having a general case displacement graph may not be overly predictive. Notice that only 50% of the maximum cut width was used as the actual cut width. Obviously if 100% of the cut width were used there would be no room for displacement and both the HD and VD curves would flat line at zero. Also notice that the optimal cut width was not used. Obviously for the optimal cut with it was derived above that HD and VD become the vertical and horizontal wire pitches respectively. Finally notice that the optimal cut width for the above system would be zero, since the half-pitches are equal.

The first trend that one notices from the above graph is that VD is independent of the angle. To understand this, we apply the above system definitions to the equation for VD and derive the general expression for VD's dependence on the angle.

$VD = s_1 + s_2 \tan \phi - w_c / \cos \phi$

Now we used a fraction of the maximum cut width:

$w_{c\_actual} = P(2s_1 + w_1 - w_2 \tan \phi) \cos \phi$, where P is some Percentage of the maximum cut width. So plugging the actual cut width back into VD:

$VD = s_1 + s_2 \tan \phi - P(2s_1 + w_1 - w_2 \tan \phi) \cos \phi / \cos \phi$, canceling out cos terms:

$VD = s_1 + s_2 \tan \phi - P(2s_1 + w_1 - w_2 \tan \phi)$, distributing P:

$VD = s_1 + s_2 \tan \phi - 2Ps_1 - Pw_1 + Pw_2 \tan \phi$, adding and subtracting in $(1 - P)\, w_2 \tan \phi$:

$VD = s_1 + s_2 \tan \phi - 2Ps_1 - Pw_1 + Pw_2 \tan \phi + [(1 - P)\, w_2 \tan \phi - (1 - P)\, w_2 \tan \phi]$

Now $(1 - P)\, w_2 \tan \phi + P\, w_2 \tan \phi$ is simply equal to $w_2 \tan \phi$ so replacing:

$VD = s_1 - 2Ps_1 - Pw_1 + (s_2 + w_2) \tan \phi - (1 - P)\, w_2 \tan \phi$, using Equation 3.1:

$VD = s_1 - 2Ps_1 - Pw_1 + s_1 + w_1 - (1 - P)\, w_2 \tan \phi$, combining and rearranging:

$VD = 2s_1 - 2Ps_1 + w_1 - Pw_1 - (1 - P)\, w_2 \tan \phi$, factoring terms:

$VD = 2s_1(1 - P) + w_1(1 - P) - (1 - P)\, w_2 \tan \phi$, factoring out (1–P):

$VD = (1 - P)(2s_1 + w_1 - w_2 \tan \phi)$, using Equation 3.1:

$(s_2 + w_2) \tan \phi = (s_1 + w_1)$, factoring out w_2 from the left:

$(s_2 / w_2 + 1) w_2 \tan \phi = (s_1 + w_1)$, isolating $w_2 \tan \phi$ term:

$w_2 \tan \phi = (s_1 + w_1) / (s_2 / w_2 + 1)$, plugging this back into VD:

$VD = (1 - P)(2s_1 + w_1 - ((s_1 + w_1) / (s_2 / w_2 + 1)))$.

Which is the general form. So when $s_2 = w_2$ as in the above figure:

$VD = (1 - P)(2s_1 + w_1 - ((s_1 + w_1) / (1 + 1)))$, combining and distributing:

$VD = (1 - P)(2s_1 + w_1 - \frac{1}{2}s_1 - \frac{1}{2}w_1)$, combining:

$VD = (1 - P)(1.5s_1 + 0.5w_1)$, which one already sees is independent of the angle, but continuing with $P = \frac{1}{2}$ and $s_1 = w_1 = 10nm$:

$VD = (1 - \frac{1}{2})(1.5(10) + 0.5(10)) = \frac{1}{2}(15 + 5) = \frac{1}{2}(20) = 10nm$, which is exactly what the figure shows.

HD is much simpler to explain and follows:

$w_{c\_actual} = \frac{1}{2}(2s_1 + w_1 - w_2 \tan \phi) \cos \phi$, remember $s_1 = w_1$ and $s_2 = w_2$ which would imply:

$(s_2 + w_2) \tan \phi = (s_1 + w_1)$, is equal to $2w_2 \tan \phi = 2w_1$ or $w_2 \tan \phi = w_1$ and so:

$w_{c\_actual} = \frac{1}{2}(2s_1) \cos \phi$, which is simply equal to $s_1 \cos \phi$, plugging this into HD:

$HD = s_2 + s_1 / \tan \phi - s_1 \cos \phi / \sin \phi$, simplifying:

$HD = s_2 + s_1 / \tan \phi - s_1 / \tan \phi$, reducing:

$HD = s_2$, which is just $s_1 / \tan \phi$.

Next, the dependence of the displacements on the percentage of the maximum w_c is shown in Figure A.14.

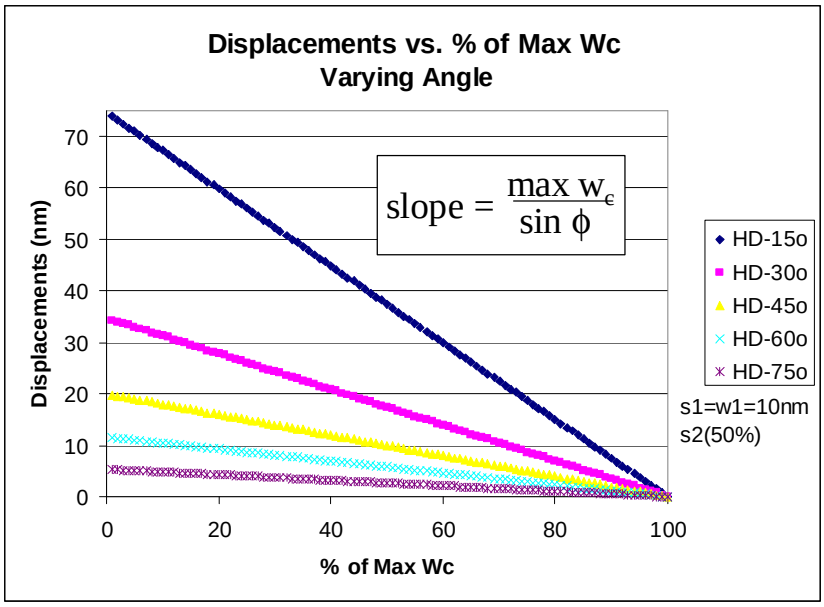

Figure A.14: Horizontal Displacement vs. Percentage of Maximum Cut Width

Each line represents a different cut angle. Obviously it would be desirable to use less of the maximum cut to improve the alignment tolerance. Similarly, using smaller cut angles, and thus fanout applications, would also improve the alignment tolerance. However, the previous systems assumed half-pitches, which was shown previously to have a non-physical optimal cut width. Suppose it was possible to increase the overall pitch, the question of whether it is more beneficial to increase the wire width or the spacing arises once again, which is addressed in Figure A.15. Clearly, as in the analysis of the cut width, increasing the spacing rather than the wire width is preferred.

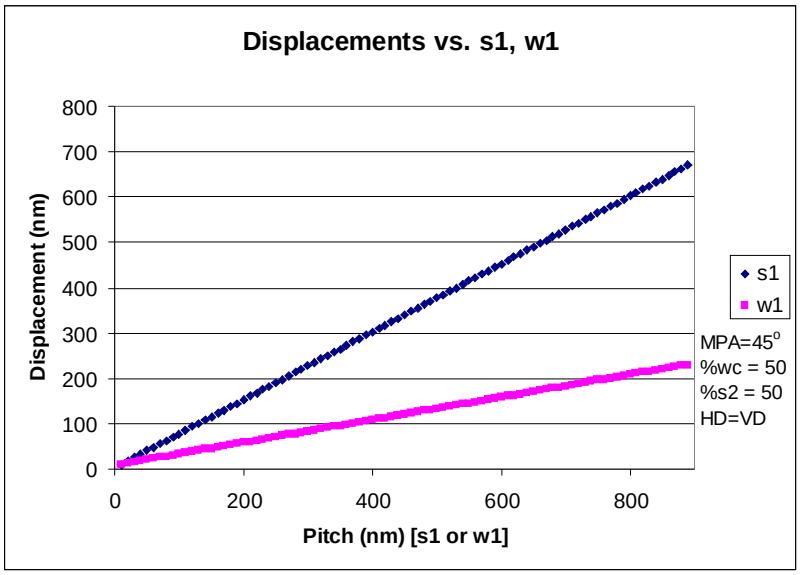

Figure A.15: Influence of Increasing Pitch on Horizontal Displacement

A.6 Impact of Non-Optimal Dimensions on Deterministic Connectivity

Figure A.16 demonstrates connection between the alignment-less novelty of this design with the probability function for non-optimal systems.

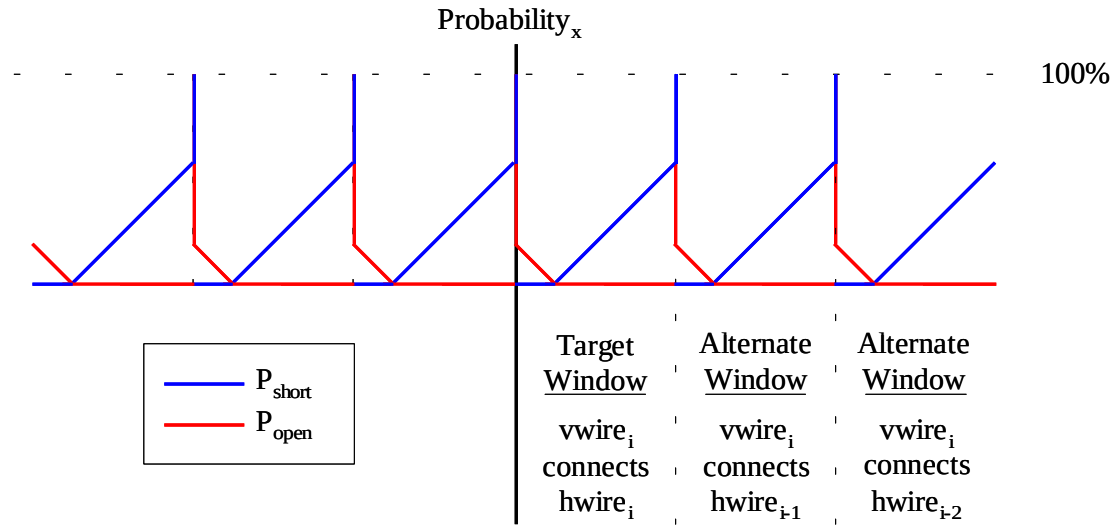

Figure A.16: Connection Probability Combined with the Structure Novelty

The x-axis is no longer w_2, but rather represents the distribution of the pitch within each alignment window. This figure combines the wire alignment with the connection probability function. For example, $vwire_i$ can fall in the first window and connect $hwire_i$, and within that window the connection probability function applies. Alternatively if the vertical wires are misaligned by one full pitch, this has no affect the connection probability function, but simply results in $vwire_i$ connecting $hwire_{i-1}$ with the connection probability function still applying within that pitch window.

A.7 Independence of the Vertical Wire Pitch on Cut Width Deviation

As long as the cut angle does not change, the total vertical wire pitch ($s_2 + w_2$) remains the same, since c_2 depends on w_c and g_2 depends on wc, but their sum does not. c_2 and g_2 are listed below for reference:

$c_2 = w_1 / \tan \phi + w_c / \sin \phi$,

$g_2 = s_1 / \tan \phi - w_c / \sin \phi$

Their sum:

$c_2 + g_2 = w_1 / \tan \phi + w_c / \sin \phi + s_1 / \tan \phi - w_c / \sin \phi$, canceling out w_c terms:

$c_2 + g_2 = w_1 / \tan \phi + s_1 / \tan \phi$

Thus, $c_2 + g_2$, and thus the total vertical wire pitch, does not change when the cut width is not fabricated as targeted.

A.8 Additional Examples of Systems with Non-Target Dimensions

Figure A.17 shows a system in which the cut width was fabricated wider than targeted.

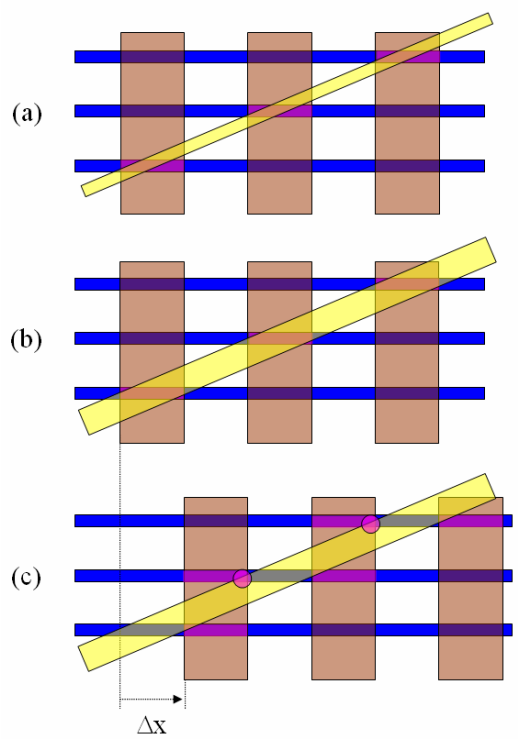

Figure A.17: Shorting in Non-Optimal System. (a) System with optimal cut width; (b) system with thicker cut width but with correct connectivity and (c) system with thicker cut width with an alignment that results in shorting

In Figure A.17(a), the system is fabricated with the optimal cut width. There is no critical restriction on the translational alignment, thus the novelty of the design. In the second system, the cut width is fabricated wider than targeted. From the analysis in Section 3.5.1.2, this would alter the optimal connecting wire dimensions. In Figure A.17(b), the optimal connecting wire dimensions assuming the correct cut width are fabricated. The system is still correctly connected, but this becomes dependent upon the alignment as shown in the final system in which shorting has occurred. So even if the connecting wires are fabricated optimally, any deviation in the cut width has the effect of changing what those optimal dimensions should be. If this deviation cannot be compensated for prior to the connecting wires being fabricated, then there will exist some

probability for connectivity errors. Deviation from the target nanowires has a similar effect, as shown in Figure A.18.

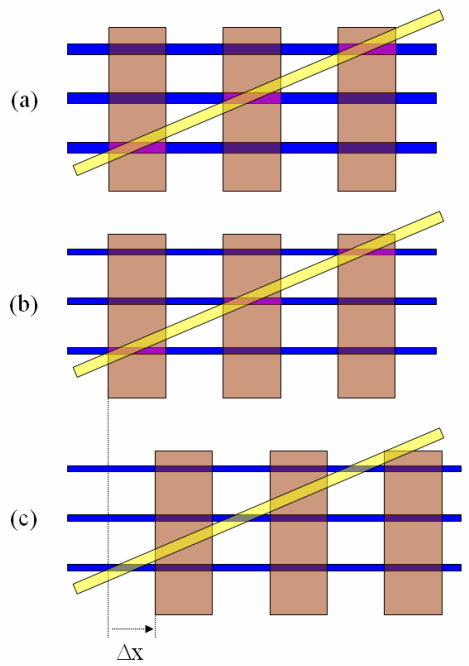

Figure A.18: Alternate Shorting in Non-Optimal System. (a) System with nanowires fabricated as designed; (b) system with nanowires fabricated thinner than intended but with correct connectivity and (c) system with thinner nanowires that leaves the structure completely unconnected.

In this example, the nanowires were fabricated thinner than designed. This resulted in an alignment dependent probability that the structure will be left completely open, as demonstrated in Figure A.18(c). These probabilities can be calculated from Equation 3.7.

A.9 Derivation of the Insulator Cut Rotational Misalignment Tolerance

Stating that there is a rotational misalignment of the insulator cut implies that there is a point at which the cut is rotated about. There are two points of rotation that are important to this analysis, as show in Figure A.19.

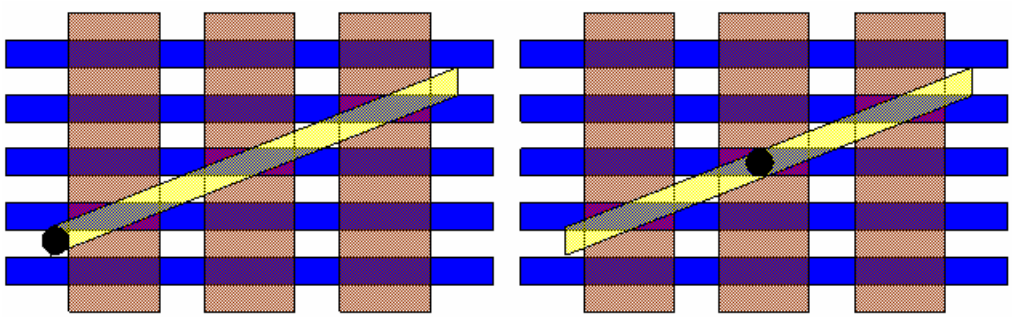

Figure A.19: Critical Points of Rotation for Analysis of Rotational Misalignment

The cut can rotate about a point at the corner of the structure, or about a point in the middle. First, a rotation about a point on the corner is studied, and then its relationship to a point of rotation about the center is studied after.

There are two types of errors to avoid, shorts and opens, both of which are depicted in Figure A.20 by red and yellow cuts respectively.

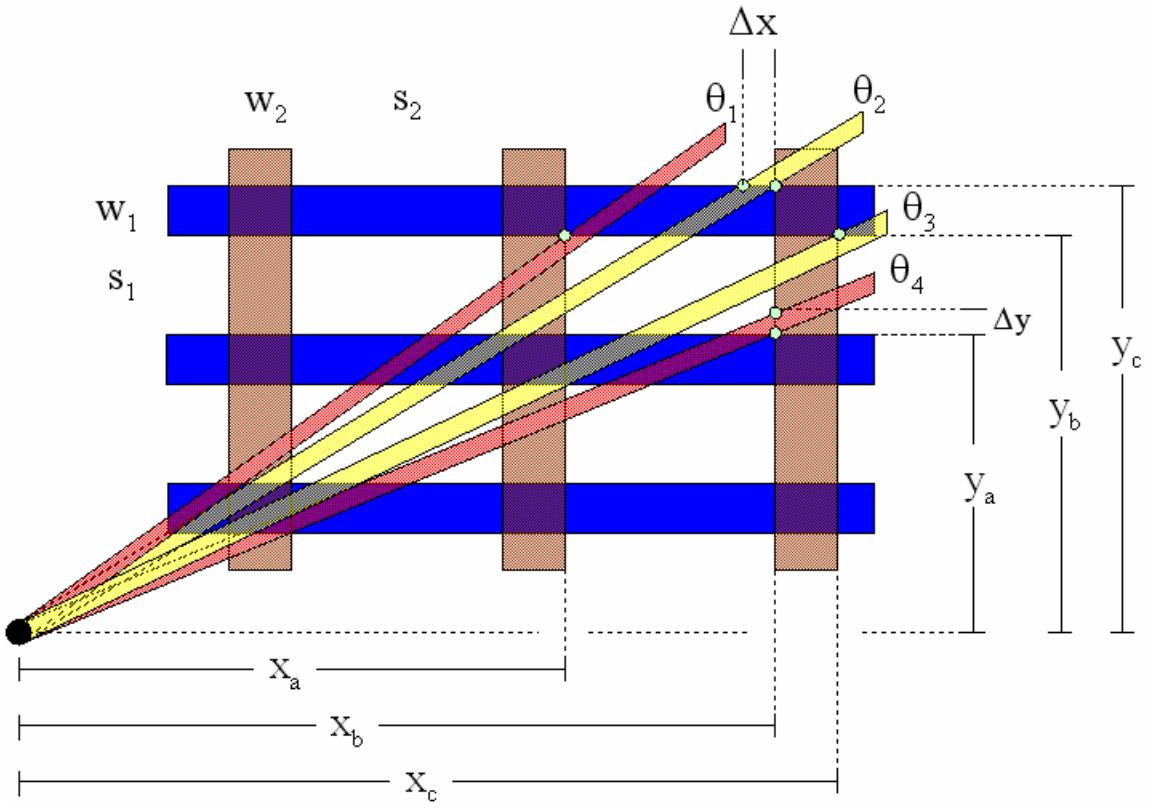

Figure A.20: Two Possible Error Types: Opens and Shorts

The yellow cuts are at angles on the border of connecting the last junction. That is, the actual cut angle has to be in between θ_2 and θ_3 to avoid leaving the last junction open. The red cuts are at angles on the border of connecting non-targeted junctions. That is, if the actual cut angle is larger than θ_1 it will connect the middle vwire with the top hwire and if it is smaller than θ_4, the cut will connect the right vwire with the middle hwire. Before solving for the angles, Δx and Δy are derived with the help of Figure A.21.

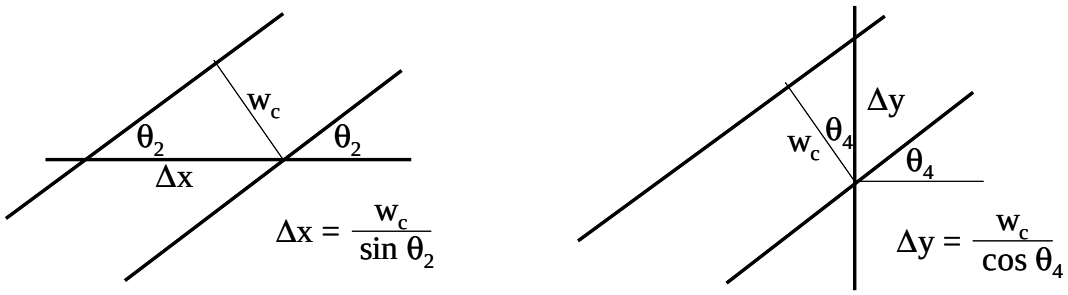

Figure A.21: Calculating Δx and Δy

Thus $\Delta x = w_c / \sin \theta_2$ and $\Delta y = w_c / \cos \theta_4$ as shown in the figure. Now solving for the tangent of the angles in terms of x_a, y_a, s_1, s_2, w_1 and w_2:

$\tan \theta_1 = y_b / x_a$, where $y_b = y_a + s_1$ and so:

$\tan \theta_1 = (y_a + s_1) / x_a$.

$\tan \theta_2 = y_c / (x_b - \Delta x)$, where $\Delta x = w_c / \sin \theta_2$ and $x_b = x_a + s_2$ and $y_c = y_a + s_1 + w_1$ so:

$\tan \theta_2 = (y_a + s_1 + w_1) / (x_a + s_2 - w_c / \sin \theta_2)$.

$\tan \theta_3 = y_b / x_c$, where $y_b = y_a + s_1$ and $x_c = x_a + s_2 + w_2$ so:

$\tan \theta_3 = (y_a + s_1) / (x_a + s_2 + w_2)$,

$\tan \theta_4 = (y_a + \Delta y) / x_b$, where $\Delta y = w_c / \cos \theta_4$ and $x_b = x_a + s_2$ so:

$\tan \theta_4 = (y_a + w_c / \cos \theta_4) / (x_a + s_2)$.

Now solving for x_a and y_a with the help of Figure A.22:

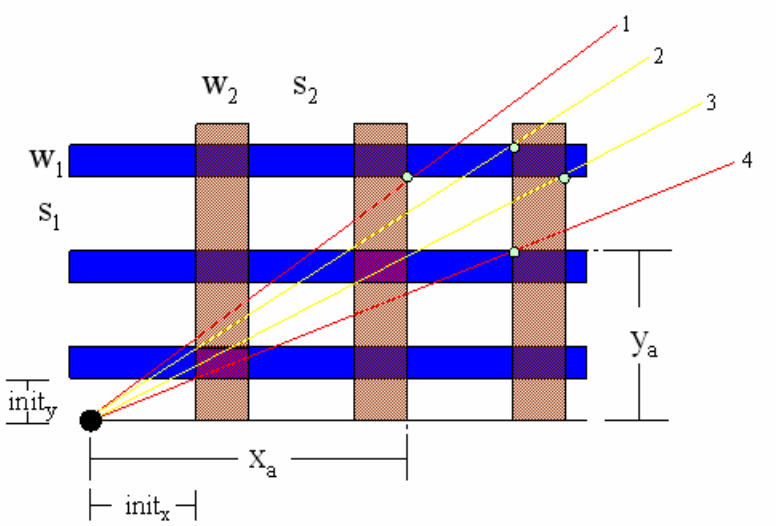

Figure A.22: Calculating x_a and y_a

A square structure (nxn) is assumed since typically the application for this design would be connect equal number of hwires and vwires and thus:

$x_a = w_2(n–1) + s_2(n–2) + init_x$

$y_a = w_1(n–1) + s_1(n–2) + init_y$

where $init_x$ and $init_y$ are the horizontal and vertical components of the distance of the point of rotation to the beginning of the structure, respectively.

Previously it was stated that there were conditions on $init_x$ and $init_y$ such that any errors in the structure occur at the points farthest away from the point of rotation. These conditions are identified with the help of Figure A.23.

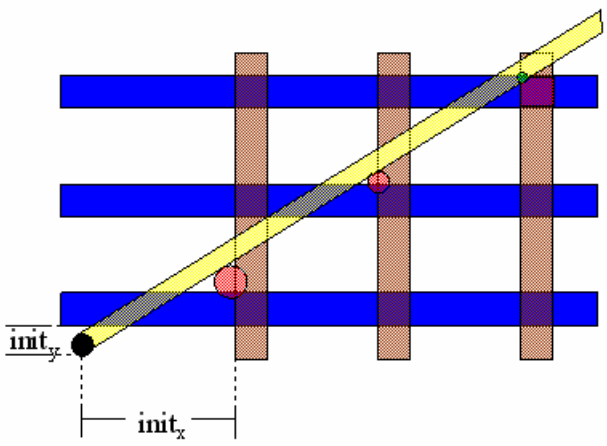

Figure A.23: Example of Unacceptable Conditions on $init_x$ and $init_y$

This figure depicts an example in which the cut misses the closer junctions but intersects the junction furthest away from the point of rotation. Ideally, the connection of a junction closer to the point of rotation will be a subset of the connectivity of the furthest junction. To guarantee this, the conditions on $init_x$ and $init_y$ are given below:
$init_x = ns_2 + mw_2$ and $init_y = ns_1 + mw_1$ where $m = (n - 1)$ or n. That is, the point of rotation must keep up with the pitch of the structure.

Now that x_a and y_a have been derived and the conditions on $init_x$ and $init_y$ have been identified, the angles are solved for:

$$\theta_1 = \tan^{-1} [(w_1(n-1) + s_1(n-1) + init_y)/(w_2(n-1) + s_2(n-2) + init_x)].$$
$$\theta_3 = \tan^{-1} [(w_1(n-1) + s_1(n-1) + init_y)/(w_2n + s_2(n-1) + init_x)].$$

Now θ_2 and θ_4, which based on the chosen alignment are dependent upon w_c complicating their derivations, are solved with the help of Maple and are *not* reduced into x_a and y_a for simplicity:

$$\theta_2 = \tan^{-1} [(((½(y_c(-2w_cy_c + 2(y_c^2x_b^2 - x_b^2w_c^2 + x_b^4)^{½}))/(y_c^2 + x_b^2))+w_c)/x_b)/$$
$$(½((-2w_cy_c + 2(y_c^2x_b^2 - x_b^2w_c^2 + x_b^4)^{½}))/(y_c^2 + x_b^2))].$$

$$\theta_4 = \tan^{-1}[(((½(y_a(-2w_cy_a + 2(y_a^2x_b^2 - x_b^2w_c^2 + x_b^4)^{½}))/(y_a^2 + x_b^2)) + w_c)/x_b)/$$
$$(½((-2w_cy_a + 2(y_a^2x_b^2 - x_b^2w_c^2 + x_b^4)^{½}))/(y_a^2 + x_b^2))].$$

Thus, the four angles that determine the allowable rotational deviation have been derived. It would be nice to have a physical intuition as to which case will limit the angle, so the following is the derivation of when $\theta_1 > \theta_2$ and when $\theta_4 < \theta_3$.

$\theta_1 > \theta_2$ implies that $\tan\theta_1 > \tan\theta_2$ which implies:
$(y_a + s_1) / x_a > (y_a + s_1 + w_1) / (x_a + s_2 - \Delta x)$, taking the cross product:
$(y_a + s_1)(x_a + s_2 - \Delta x) > (y_a + s_1 + w_1)x_a$, distributing terms:
$x_ay_a + x_as_1 + y_as_2 + s_1s_2 - y_a\Delta x - s_1\Delta x > x_ay_a + x_as_1 + x_aw_1$, canceling terms:
$y_as_2 + s_1s_2 - y_a\Delta x - s_1\Delta x > x_aw_1$, pulling out s_2 on the left and rearranging:
$s_2(y_a + s_1 - \Delta x/s_2(y_a + s_1)) > x_aw_1$, substituting $y_b = y_a + s_1$ and dividing by s_2:
$y_b - y_b(\Delta x/s_2) > x_aw_1 / s_2$, substituting $x_a = y_b / \tan\theta_1$:
$y_b - y_b(\Delta x/s_2) > y_bw_1 / s_2\tan\theta_1$, canceling out y_b, and redistributing:
$\tan\theta_1 (1 - \Delta x/s_2) > w_1/s_2$.

Now, assume that Δx is rather small, and is effectively zero, then $\theta_1 > \theta_2$ when:
$\tan\theta_1 > w_1/s_2$ or physically, when θ_1 is greater than the angle made by the vertical space and the horizontal wire. A similar analysis can be made such that $\theta_4 < \theta_3$ when:
$\tan\theta_4 < s_1/w_2$ or when θ_4 is less than the angle made by the horizontal space and the vertical wire. Of course remember that these are assuming very small cuts and thus Δx and Δy are effectively zero particularly for fanout, and less so for nanowire interconnect. Concluding, the allowable rotational deviation in the cut angle is equal to:

Insulator Cut Rotational Misalignment Tolerance = $\text{MIN}(\theta_1 - \theta_3, \theta_1 - \theta_4, \theta_2 - \theta_3, \theta_2 - \theta_4)$

Thus far, a point of rotation about the edge of the structure was considered. What effect would a point of rotation in the center of the structure have on the above derived equations? If fact, there is very little theoretical difference between the two scenarios. A rotation point in the center is just a subset of a rotation point at the edge. The system size is halved resulting in an approximate doubling of the rotational allowance. In general, as the system size increases or the rotational allowance goes to zero, the limit of reducing the system size by a factor of two is to increase the rotational allowance by a factor of two.

Now that the insulator cut rotational misalignment has been derived, it is important to understand how this affects the scalability of this structure. This analysis starts with a graph of the rotational allowance versus the cut angle for various system sizes, as shown in Figure A.24.

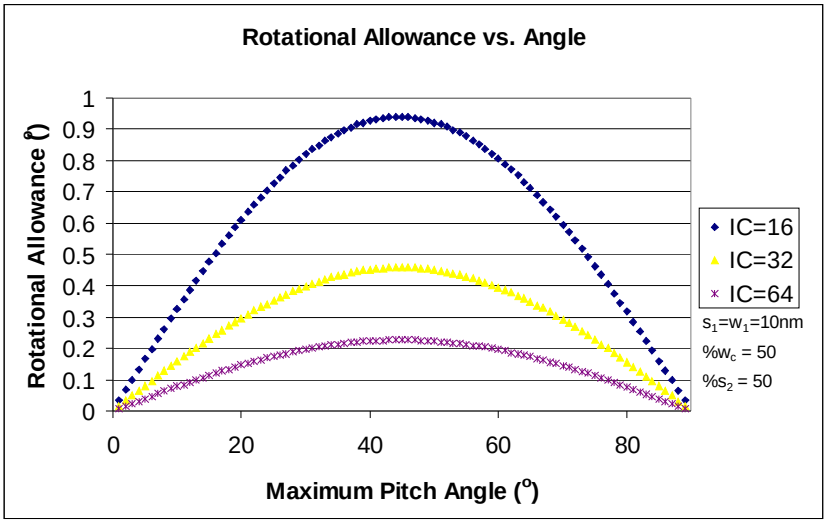

Figure A.24: Dependence of Rotational Allowance on the Insulator Cut Angle

The above graph shows that the rotational allowance is greatest when interconnecting nanowires to nanowires at a 45° angle. As the difference in sizes between the two sets of wires increases, the amount of rotational allowance decreases. One also notices that as the interconnect size goes from 16x16 to 64x64, the rotational

allowance decreases significantly. This relationship is further examined in Figure A.25 in which the rotational allowance is calculated for various system sizes. The maximum pitch angle was chosen to be 45^{o}, which gives the maximum rotational allowance value for each system size.

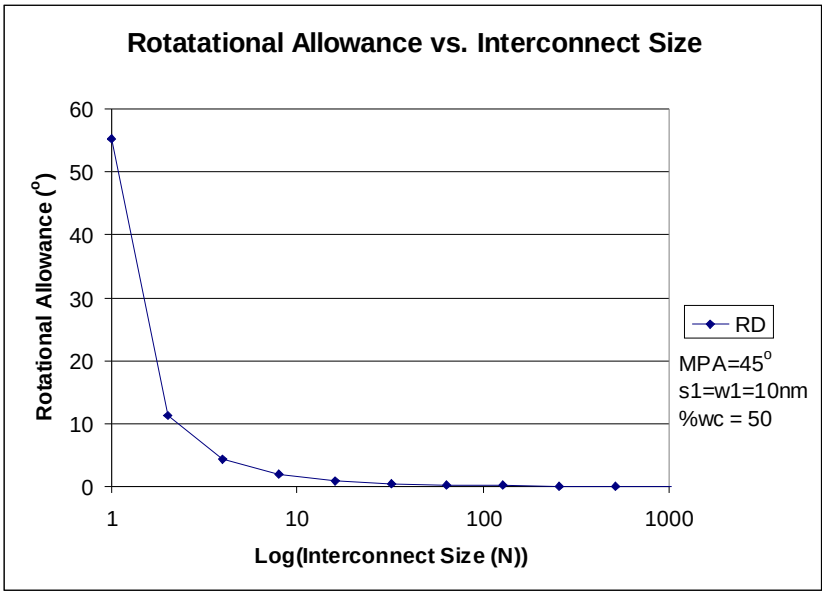

Figure A.25: Dependence of Rotational Allowance on the System Size

As the system size increases, the rotational allowance decreases rapidly. This does not bode well for scaling and suggests that extremely precise cut angles are necessary for very large structures. Notice that the rotational allowance of a 1x1 system was given as 55^{o} in the above figure, which is not intuitive. Recall that there were two types of errors that could occur, shorts and opens. Shorts were defined by the cut intersecting non-target junctions, or more specifically intersecting neighboring junctions of the junction furthest away from the point of rotation. Obviously, there are no neighboring junctions for a 1x1 system, but the equations process the system as if there still were junctions to avoid intersecting. In fact, Figures A.26 and A.27 show exactly what is being returned by the equation for this type of error in the 1x1 system.

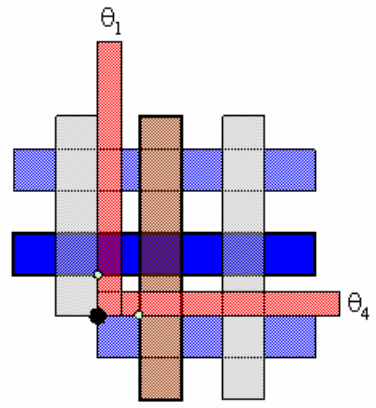

Figure A.26: Avoiding Shorts in a 1x1 System

Obviously no such error would exist if the cut were to extend further since there are no wires for it to short. However, the 55^{o} rotational allowance is originating from avoiding leaving the target junction open, as shown in Figure A.27.

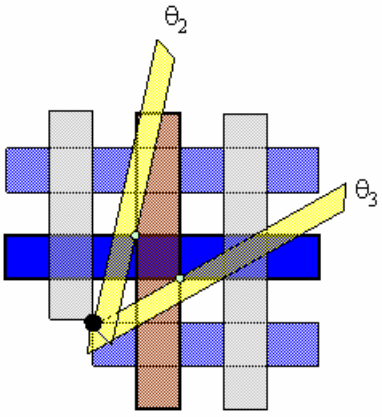

Figure A.27: Avoiding an Open in a 1x1 System

Thus, the analysis is still correct for a 1x1 system since this open error is limiting the rotational allowance. Obviously this value is heavily dependent upon the values of $init_x$ and $init_y$.

Figure A.28 shows the rotational allowance for various distributions of the pitch.

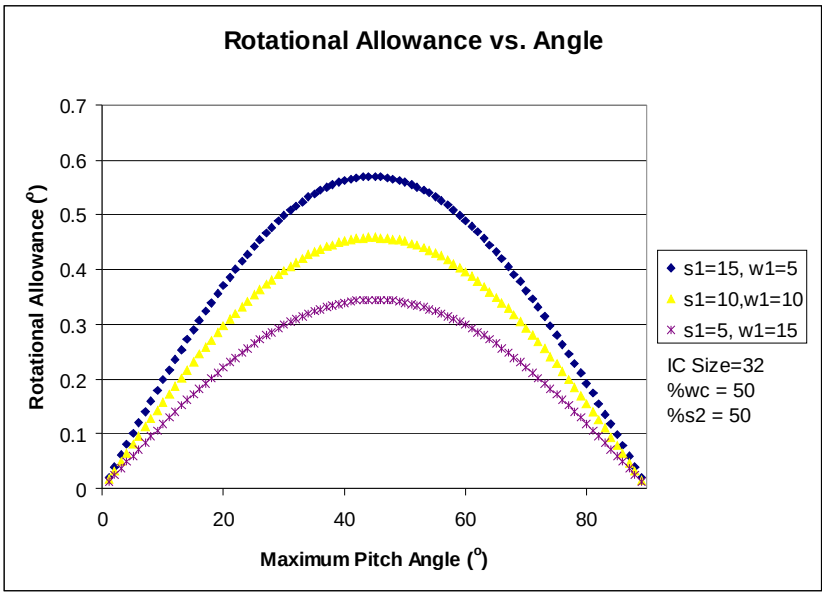

Figure A.28: Rotational Allowance for Various Distributions of the Pitch

It is clear that once again, distributing more of the pitch into the spacing is preferred. However, the gains in rotational allowance are less than a factor of two, clearly not enough address the scaling issue. Figure A.29 investigates increasing the spacing, rather than just the distribution of that spacing from the total pitch.

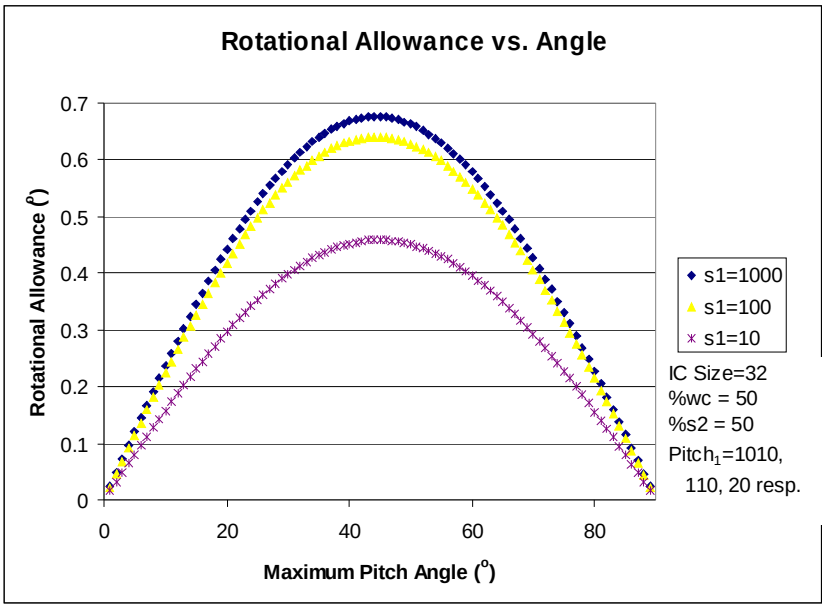

Figure A.29: Rotational Allowance for Increased Spacing

While increasing the spacing does improve the rotational allowance, its impact diminishes. Finally, consider utilizing more or less than the maximum cut width. Thus far, 50% of the maximum cut width was assumed. Figure A.30 investigates the impact of cut width on rotational allowance.

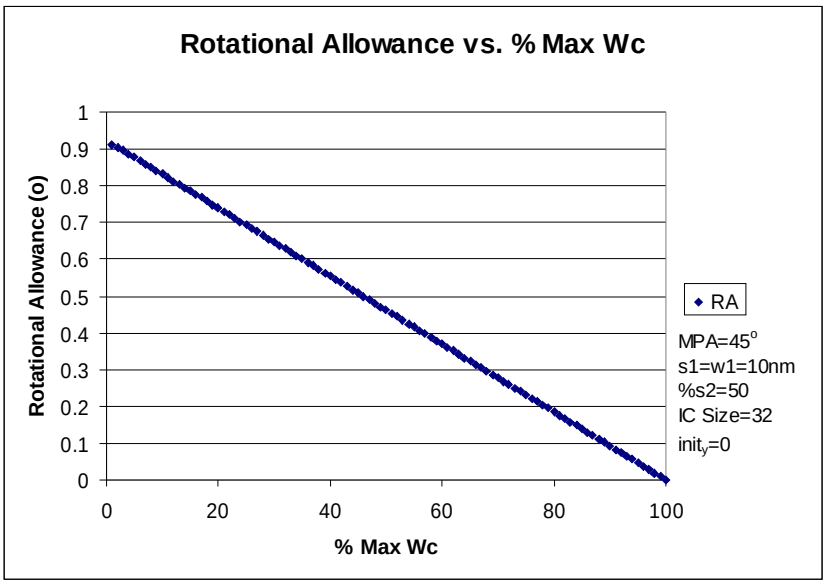

Figure A.30: Dependence of the Rotational Allowance on the Cut Width

Clearly one would prefer to use the smallest cut width possible to improve the rotational allowance. Unfortunately, the cut width will become the critical dimension if it is decreased too much. It does not seem possible that changing the system parameters will have a tremendous impact on the rotational allowance. The real problem is that any error in the rotational alignments of the structure is intrinsically not scalable. The rotational allowance is strongly dependent upon the size of the structure. Therefore, an alternate process flow is presented in Section 3.6 to eliminate the rotational alignment of the cut.

A.10 Derivation of the Vertical Wire Rotational Misalignment Tolerance

As suggested in Section 3.5.2.2, to derive the rotational misalignment tolerance of the vertical wires, an equivalent vertical pitch is derived and than a similar analysis to rotational misalignment of the insulator cut is performed. For misalignment in the direction of the cut, this equivalent vertical pitch was derived as:

$w_{2x} = w_2 / \cos \tau + w_1 \tan \tau$

$s_{2x} = s_2 / \cos \tau + s_1 \tan \tau$

where angular deviation from 90^o, or completely orthogonal connecting wires, is denoted by tau, τ.

Figure A.31 depicts a system in which rotational misalignment of the vertical wires resulted in an increase of the equivalent vertical pitch, which is the pitch illustrated. This increase resulted in the cut missing the last junction, similar to a θ_2 error from the rotational misalignment of the insulator cut analysis. With the help of this figure, the rotational misalignment of the vertical wires that would result in this type of connectivity error is derived. Since these errors are dependent upon the alignment of the cut to the structure, an alignment is assumed to be $init_x$ and $init_y$ to the left and below the first junction respectively.

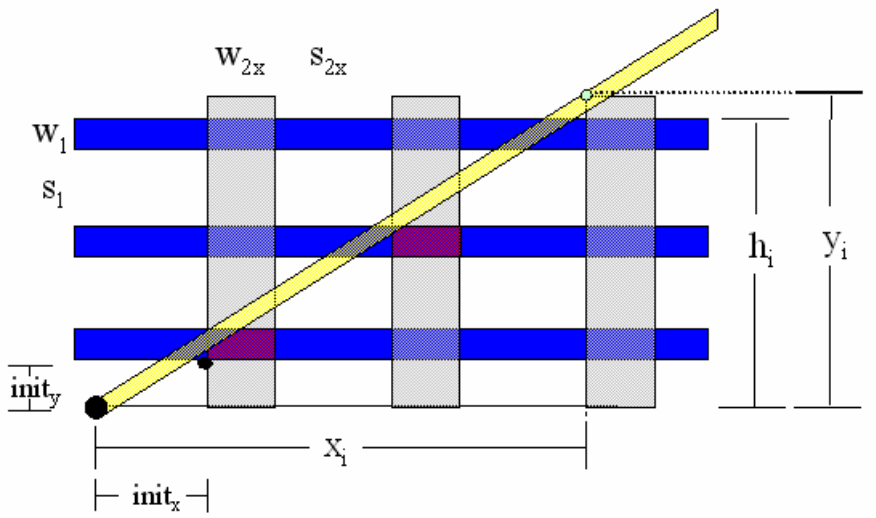

Figure A.31: Deriving the Rotational Misalignment of the Vertical Wires that Results in an Open

From the figure, it can be shown that the condition for the last target junction to be left open is: $y_i - w_c / \cos \phi > h_i$. These variables are defined as:

$x_i = s_{2x} (i - 1) + w_{2x} (i - 1) + init_x$,

$y_i = x_i \tan \phi$,

$hi = s_1 (i - 1) + w_1 (i) + init_y$,

Unfortunately, s_{2x} and w_{2x} as defined can lead to false connections. In other words the system can actually be open but the model predicts that it is connected. This can be seen in Figure A.32 where the cut is not intersecting the physical wire, but just catches the equivalent wire resulting in a falsely identified error.

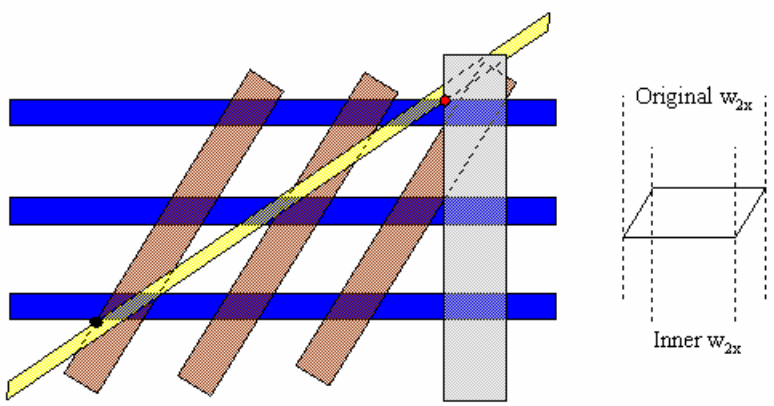

Figure A.32: Potential for False Positives

Fortunately redefining w_{2x} from the horizontal projection of the vertical wire to the inside square of the parallelogram formed by the intersection of the two crossing wires eliminates these false positives. Unfortunately this results in the possibility of false opens. However, the geometry of the structure prevents this error from propagating past the next junction, so using the inner w_{2x} will result in interconnect size limitations accurate to within one connection. Thus, the new w_{2x} and s_{2x}, now denoted w_{2x}^{+} and s_{2x}^{+}, are derived as:

$$w_{2x}^{+} = | w_2 / \cos \tau - w_1 \tan \tau |,$$

$$s_{2x}^{+} = (s_{2x} + w_{2x}) - w_{2x} = (s_2 + w_2) / \cos \tau + (s_1 + w_1) \tan \tau - | w_2 / \cos \tau - w_1 \tan \tau |,$$

The redefinition of the s_{2x} and w_{2x} results in a distance, Δx, between the start of the equivalent pitch and the assumed alignment, as shown in Figure A.33.

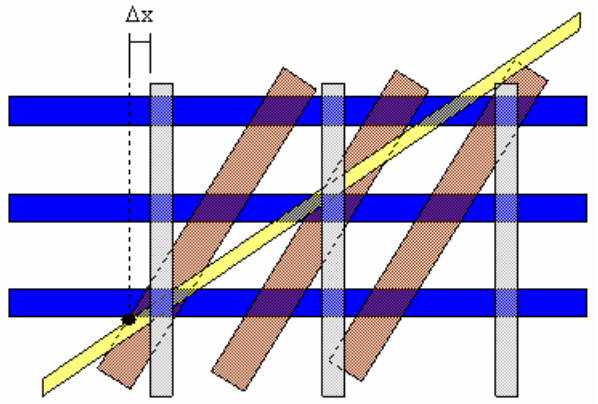

Figure A.33: System with Redefined Equivalent Vertical Wire Pitch

Factoring this value, $w_1 \tan \tau$, into the previously derived equations results in:

$x_i = s_{2x}^{+} (i - 1) + w_{2x}^{+} (i - 1) + w_1 \tan \tau + init_x$,

$y_i = x_i \tan \phi$,

$hi = s_1 (i - 1) + w_1 (i) + init_y$,

The target junction will be open when:

$(s_{2x}^{+} (i - 1) + w_{2x}^{+} (i - 1) + w_1 \tan \tau + init_x) \tan \phi - w_c / \cos \phi > s_1 (i - 1) + w_1 (i) + init_y$.

Assuming $init_x = init_y = 0$ and using Maple to solve for i:

$i > ((w_c / \cos \phi) + (s_{2x}^{+} + w_{2x}^{+} - w_1 \tan \tau) \tan \phi - s_1) / ((s_{2x}^{+} + w_{2x}^{+}) \tan \phi - (s_1 + w_1))$

This defines the size of the system in which an offset of τ in the vertical wires results in an open i^{th} junction. Along with opens, shorting errors can occur with non-perpendicular crossing wires. Figure A.34 will help derive the size of the system in which a shorting error will occur.

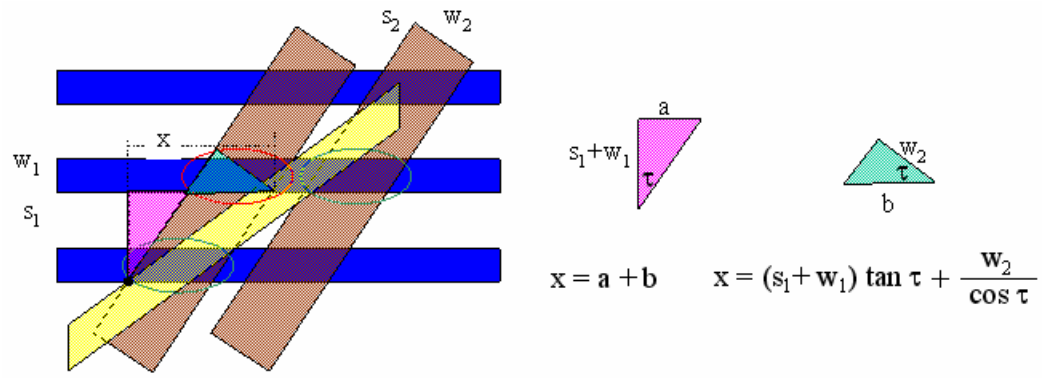

Figure A.34: Deriving the Rotational Misalignment of the Vertical Wires that Results in a Short

In order to avoid shorting of the left vwire, the cut must travel greater than x in the horizontal direction over one horizontal wire pitch, $s_1 + w_1$. The distance the cut travels over one horizontal wire pitch is $(s_1 + w_1) / \tan \phi$. To avoid shorting over the entire structure, the distance the cut travels each pitch must be greater than the distance the vertical wire travels each pitch plus the cumulative distance of the spaces between each pitch, or expressed as an equation:

$((s_1 + w_1) / \tan \phi)(i - 1) > ((s_1 + w_1) \tan \tau + w_2 / \cos \tau)(i - 1) + (s_2 / \cos \tau)(i - 2)$.

In keeping with previously established convention, the inequality is reversed such that the interconnect size in which the error, in this case a short, occurs is derived. Solving for i:

$i > [((s_1 + w_1) \tan \tau + w_2 / \cos \tau) + 2(s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)] /$

$[((s_1 + w_1) \tan \tau + w_2 / \cos \tau) + (s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)]$.

Before continuing, it is important to identify the complete set of errors that can occur. The prior two derivations were for opens/shorts for systems in which the misalignment of the vertical wires results in an effectively larger equivalent pitch. Figure A.35 illustrates this point as well as identifying other possible errors that could occur and is analogous to the analysis for rotational misalignment of the insulator cut.

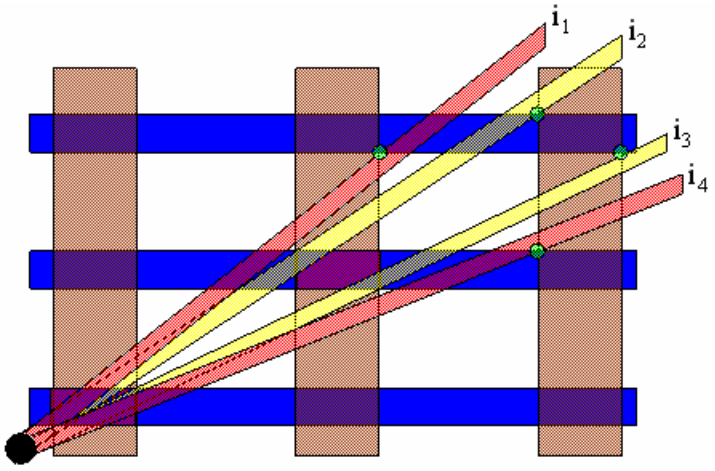

Figure A.35: Two Possible Errors Types: Opens and Shorts

i_1 and i_4 represent shorting errors while i_2 and i_3 represent open errors. In order for i_3 or i_4 to result from misaligned vertical wires, the new equivalent pitch would have to be less than the ideal or targeted pitch. To understand if this can even occur, s_{2x} and w_{2x} are reexamined. Recall the total equivalent vertical wire pitch:

$s_{2x} + w_{2x} = (s_2 + w_2) / \cos \tau + (s_1 + w_1) \tan \tau$,

The questions is, can this be less than $s_2 + w_2$? For a value of τ between 0 and 90^o, the only range under consideration for this analysis, $\tan \tau$ is positive and so the second term always increases the equivalent pitch. Along that same reasoning, $\cos \tau$ is always positive and less than or equal to one. This implies that the first term is always greater than $s_2 + w_2$. Therefore, when the wires are rotated in the direction of the cut, there is no way for the equivalent vertical wire pitch to be less than the ideal pitch. Thus, summing up:

$i_1^+ > [((s_1 + w_1) \tan \tau + w_2 / \cos \tau) + 2(s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)] /$

$[((s_1 + w_1) \tan \tau + w_2 / \cos \tau) + (s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)]$.

$i_2^+ > ((w_c / \cos \phi) + (s_{2x}^+ + w_{2x}^+ - w_1 \tan \tau) \tan \phi - s_1) / ((s_{2x}^+ + w_{2x}^+) \tan \phi - (s_1 + w_1))$.

$i_3^+ >$ N/A

$i_4^+ >$ N/A

Does this imply that i_3 and i_4 cannot occur? Perhaps for misalignment of the vertical wires in the direction of the cut, however, Figure A.36 shows an example of a system in which misalignment of the vertical wires in the opposite direction as that of the cut angle results in an open error.

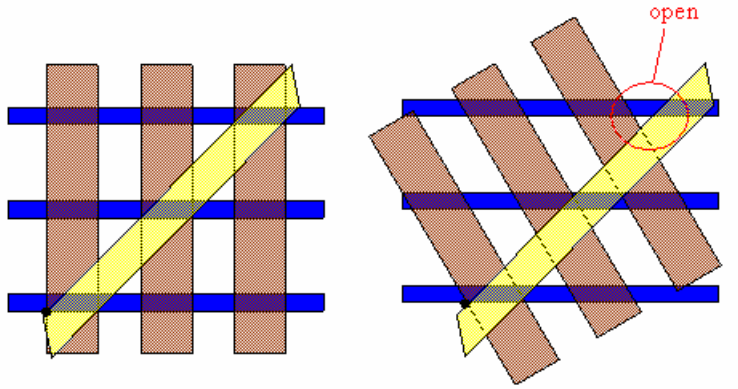

Figure A.36: Rotation Opposite the Direction of the Cut

Once again the derivation begins with deriving the equivalent vertical wire pitch with the help of Figure A.37. Tau is still defined as the angular offset of the vertical wires from the vertical axis.

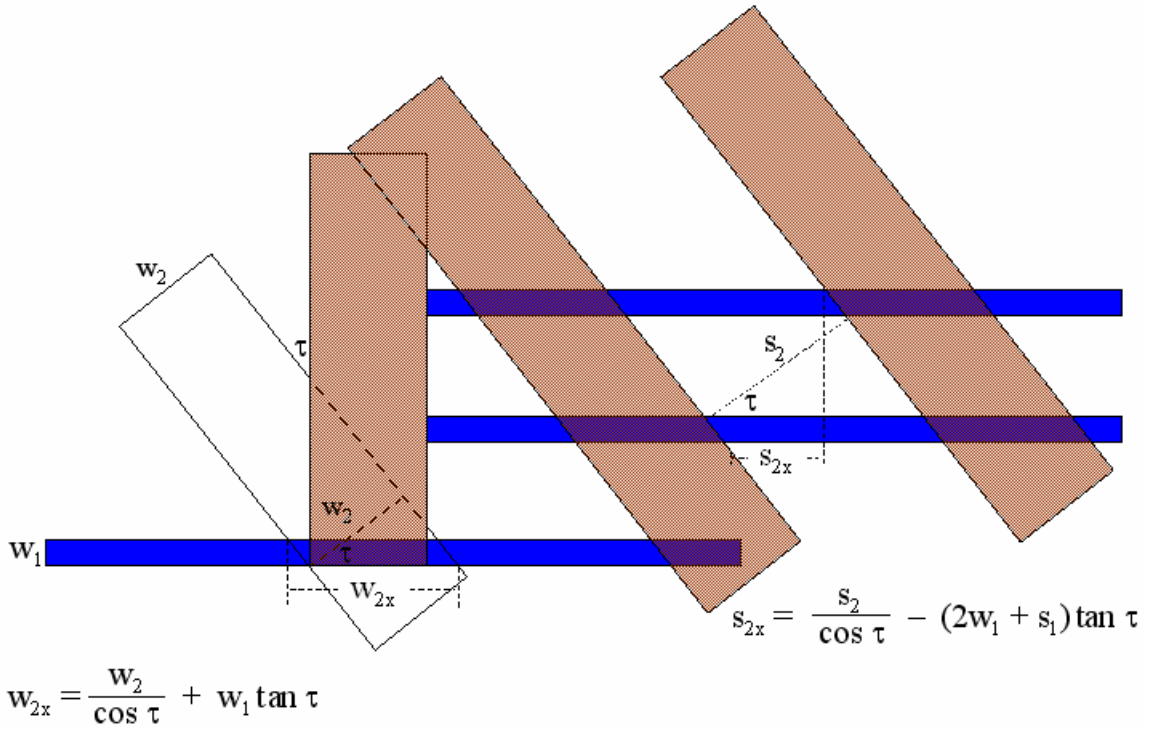

Figure A.37: Deriving the Equivalent Vertical Wire Pitch for Rotation of the Wires Opposite the Cut Angle

The new equivalent vertical wire width, w_{2x}^-, is once again the horizontal projection of the non-perpendicular wire width derived as $w_{2x}^- = w_2 / \cos \tau + w_1 \tan \tau$. The new equivalent spacing, s_{2x}^-, is once again the distance between the intersections of consecutive vwires with consecutive hwires derived as $s_{2x}^- = s_2 / \cos \tau - (2w_1 + s_1) \tan \tau$. From these equations, the total equivalent pitch is investigated:

$s_{2x}^- + w_{2x}^- = ((s_2 / \cos \tau - (2w_1 + s_1) \tan \tau) + (w_2 / \cos \tau + w_1 \tan \tau)$, combining terms:

$s_{2x}^- + w_{2x}^- = (s_2 + w_2) / \cos \tau - (s_1 + w_1) \tan \tau$,

At $\tau = 0^o$, $\tan \tau = 0$ and $\cos \tau = 1$; therefore under conditions with no deviation:

$s_{2x}^- + w_{2x}^- = s_2 + w_2$, as one would expect.

Notice however, that in this case the new equivalent pitch can be less than the targeted pitch. Therefore, errors i_3 and i_4 can occur in this system. Figure A.38 will help in deriving i_3 errors.

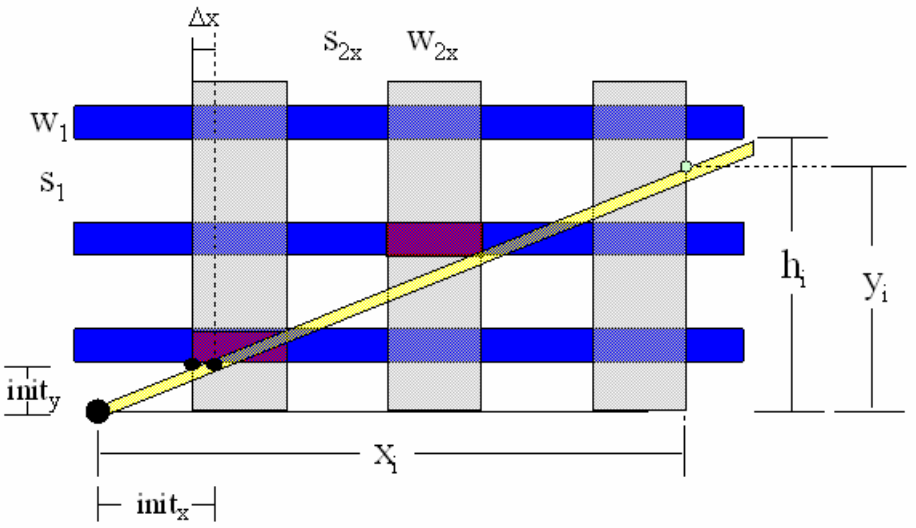

Figure A.38: Deriving the Rotational Misalignment of the Vertical Wires that Results in an Open Below the Target Junction

From the figure it can be shown that the condition for the last target junction to be left open is: $y_i < h_i$. These variables are defined as:

$x_i = s_{2x}^{-} (i - 1) + w_{2x}^{-} (i) - w_1 \tan \tau + init_x$,

$y_i = x_i \tan \phi$,

$hi = s_1 (i - 1) + w_1 (i - 1) + init_y$,

The target junction will be open when:

$(s_{2x}^{-} (i - 1) + w_{2x}^{-} (i) - w_1 \tan \tau + init_x) \tan \phi < s_1 (i - 1) + w_1 (i - 1) + init_y$,

Assuming $init_x = init_y = 0$ and using Maple to solve for i:

$i_3^{-} > ((s_1 + w_1) - (s_{2x}^{-} + w_1 \tan \tau) \tan \phi) / ((s_1 + w_1) - (s_{2x}^{-} + w_{2x}^{-}) \tan \phi)$.

This represents the maximum interconnect size before an open occurs. Figure A.39 will help in deriving the maximum size before a short occurs.

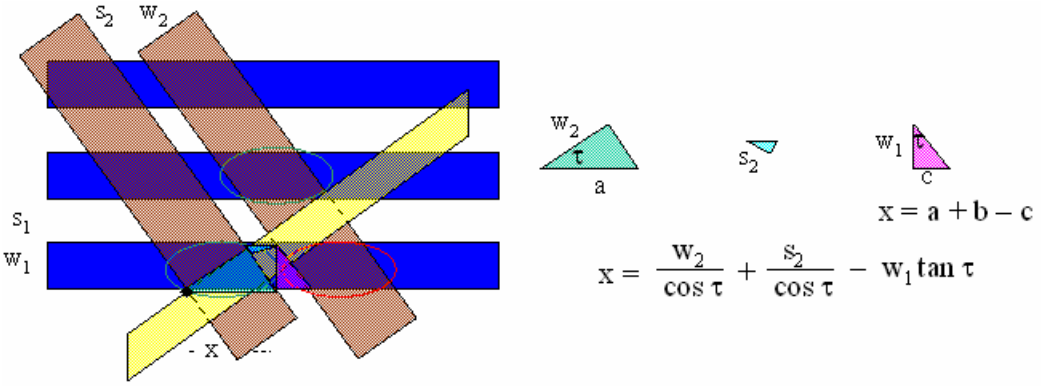

Figure A.39: Deriving the Rotational Misalignment of the Vertical Wires that Results in a Short of the Junction Below the Target

The distance the cut travels over w_1 is $(w_1 / \tan\phi) + (w_c / \sin\phi)$. In order to avoid shorting of the right vwire, the distance the bottom of the cut travels each pitch must be less than the distance the non-perpendicular wire and space travel over w_1, $x = (s_2 + w_2) / \cos\tau + s_2 / \cos\tau - w_1 \tan\tau$, minus the overshoot distance between wire junctions, or expressed as an equation:

$((w_1 / \tan\phi) + (w_c / \sin\phi))\,(i - 1) + ((s_1 / \tan\phi) - (w_c / \sin\phi))\,(i - 2) < ((s_2 + w_2) / \cos\tau - w_1 \tan\tau)\,(i - 1) - (s_1 \tan\tau)\,(i - 2)$

Once again the inequality is reversed such that the interconnect size in which the error, in this case a short, occurs is derived. Solving for i:

$i_4^- > [((w_1 / \tan\phi) + (w_c / \sin\phi)) + 2((s_1 / \tan\phi) - (w_c / \sin\phi)) - ((s_2 + w_2) / \cos\tau - w_1 \tan\tau) + 2(s_1 \tan\tau)] / [((w_1 / \tan\phi) + (w_c / \sin\phi)) + ((s_1 / \tan\phi) - (w_c / \sin\phi)) - ((s_2 + w_2) / \cos\tau - w_1 \tan\tau) + (s_1 \tan\tau)]$.

Thus i_1^+, i_2^+, i_3^- and i_4^- have been derived, the subscripts defining the type of error and the superscripts defining the direction of tau. It was shown that i_3^+ and i_4^+ do not exist between 0 and 90^o since in this range a rotation of the vertical wires in the direction of the cut could only result in an increasing pitch. Do i_1^- and i_2^- error exist for rotation of the vertical wire sin the direction of the cut? To answer this question, the derivation for the equivalent vertical wire pitch is revisited. It was shown:

$s_{2x}^{-} + w_{2x}^{-} = (s_2 + w_2) / \cos \tau - (s_1 + w_1) \tan \tau$,

The system that has been studied thus far is one in which the second term, $(s_1 + w_1) \tan \tau$, was dominating the first term and thus the equivalent pitch was less than the ideal pitch. For other systems or values of τ, the first term will dominate and the equivalent pitch will increase until it is larger than the ideal pitch. Thus, for rotation of the vertical wires opposite of the cut angle, i_1^{-} and i_2^{-} can exist. Solving for the angle in which the equivalent vertical wire pitch is equal to the ideal pitch:

$\tau = 0^o$ and $\tau = \tan^{-1} ((2(s_1+w_1)(s_2+w_2)) / ((s_2 + w_2)^2 - (s_1 + w_1)^2))$.

If the two angles are equivalent at zero, and then the equivalent pitch starts decreasing and then the two angles are equal again, there must be a turning point in which the equivalent pitch stops decreasing and starts increasing again. To find this angle, the derivative of the equivalent pitch is set equal to zero and solved:

$d/dt\ (s_{2x}^{-} + w_{2x}^{-}) = 0$,

$(s_2 + w_2) \sin \tau / \cos^2 \tau - (s_1 + w_1) \sec^2 \tau = 0$, solving for τ:

$\tau = \tan^{-1} ((s_1+w_1) / [(s_2 + w_2)^2 - (s_1 + w_1)^2]^{½})$.

Thus, two new variables have been defined:

$$t = \tan^{-1}\left[\frac{2(s_1 + w_1)(s_2 + w_2)}{(s_2 + w_2)^2 - (s_1 + w_1)^2}\right] \qquad \textit{Equation A.6}$$

$$t = \tan^{-1}\left[\frac{(s_1 + w_1)}{\sqrt{(s_2 + w_2)^2 - (s_1 + w_1)^2}}\right] \qquad \textit{Equation A.7}$$

The Pitch Equivalency Angle (PEA) is the angle in which the equivalent pitch is once again equal to the ideal pitch. The Pitch Turning Angle (PTA) is the angle in which the equivalent pitch stops decreasing and starts increasing. To help visualize this, Figure A.40 shows an example of a system in which rotation of the wires opposite the direction of the cut results in an increased equivalent pitch.

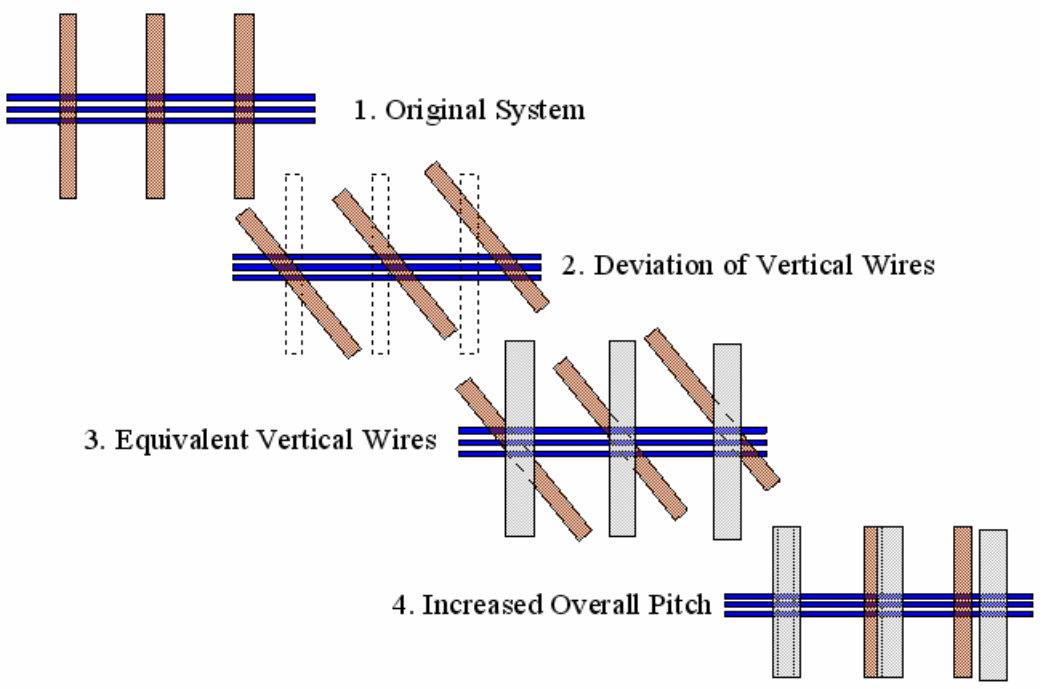

Figure A.40: Example System of Increasing Equivalent Pitch with Rotation in the Direction Opposite of the Cut Angle

The figure begins with the initial system. The next step is a rotational misalignment of the vertical wires by an angle of 59^{o} opposite the direction of the cut. The equivalent vertical wire pitch is then drawn on the structure. Finally, the original vertical wire pitch is superimposed with the equivalent vertical wire pitch. Clearly the equivalent vertical wire pitch has increased. Thus, if the pitch can increase, it is necessary to solve for i_1^- and i_2^-. Figure A.41 will help in deriving i_2^-.

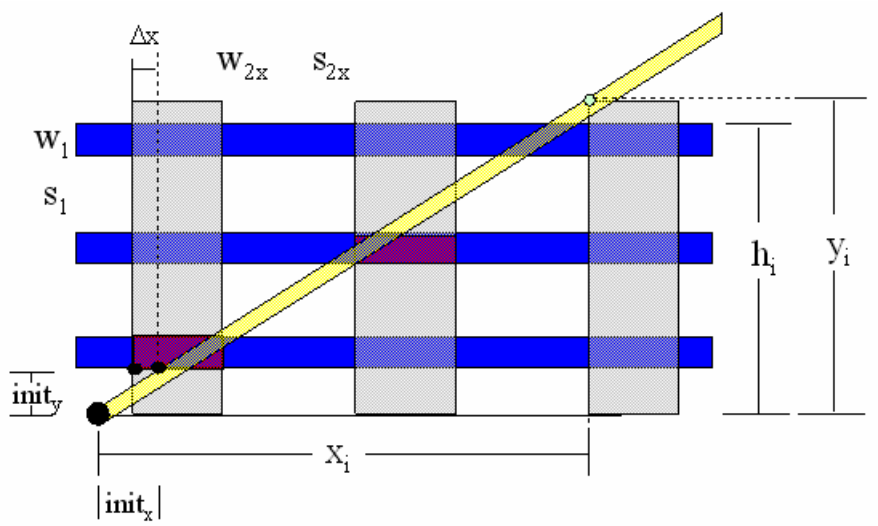

Figure A.41: Deriving the Rotational Misalignment of the Vertical Wires that Results in an Open Above the Target Junction

From the figure, it can be shown that the condition for the last target junction to be left open is: $(y_i - w_c / \cos \phi) > h_i$. These variables are defined as:

$x_i = s_{2x}^{-} (i - 1) + w_{2x}^{-} (i - 1) - w_1 \tan \tau + init_x$,

$y_i = x_i \tan \phi$,

$hi = s_1 (i - 1) + w_1 (i) + init_y$,

The target junction will be open when:

$(s_{2x}^{-} (i - 1) + w_{2x}^{-} (i - 1) - w_1 \tan \tau + init_x) \tan \phi - w_c / \cos \phi > s_1 (i - 1) + w_1 (i) + init_y$,

Assuming $init_x = init_y = 0$ and using Maple to solve for i:

$i_2^{-} > ((w_c / \cos \phi) + (s_{2x}^{-} + w_{2x}^{-} + w_1 \tan \tau) \tan \phi - s_1) / ((s_{2x}^{-} + w_{2x}^{-}) \tan \phi - (s_1 + w_1))$.

This represents the maximum interconnect size before an open occurs. Figure A.42 will help in deriving the maximum size before a short occurs.

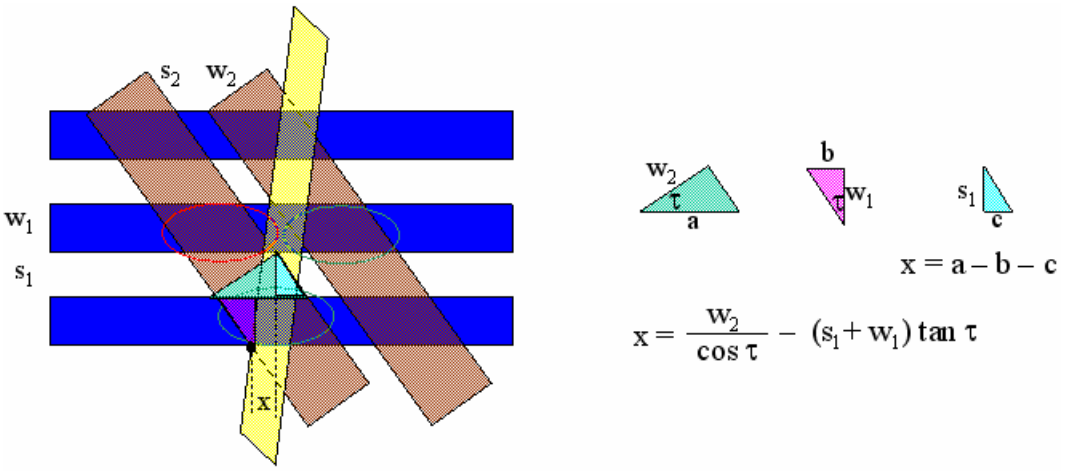

Figure A.42: Deriving the Rotational Misalignment of the Vertical Wires that Results in a Short of the Junction Above the Target

The distance the cut travels over the horizontal wire pitch is $(s_1 + w_1) / \tan \phi$. In order to avoid shorting of the left vwire, the distance the cut travels each pitch must be greater than the distance the non-perpendicular wire travels each pitch, $x = w_2 / \cos \tau - (s_1 + w_1) \tan \tau$, plus the cumulative distance of the spacing between each vwire, or expressed as an equation:

$((s_1 + w_1) / \tan \phi)(i - 1) > (w_2 / \cos \tau - (s_1 + w_1) \tan \tau)\ (i - 1) + (s_2 / \cos \tau)\ (i - 2)$.

The inequality is reversed such that the interconnect size in which the error, in this case a short, occurs is derived. Solving for i:

$i_1^- > [(w_2 / \cos \tau - (s_1 + w_1) \tan \tau) + 2(s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)] /$

$[(w_2 / \cos \tau - (s_1 + w_1) \tan \tau) + (s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)]$.

Thus, all of the equations that govern shorts and open errors have been derived when the vertical wires are rotated opposite the direction of the cut and are repeated below:

$i_1^- > [(w_2 / \cos \tau - (s_1 + w_1) \tan \tau) + 2(s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)] /$

$[(w_2 / \cos \tau - (s_1 + w_1) \tan \tau) + (s_2 / \cos \tau) - ((s_1 + w_1) / \tan \phi)]$.

$i_2^- > ((w_c / \cos \phi) + (s_{2x}^- + w_{2x}^- + w_1 \tan \tau) \tan \phi - s_1) / ((s_{2x}^- + w_{2x}^-) \tan \phi - (s_1 + w_1))$.

$i_3^- > ((s_1 + w_1) - (s_{2x}^- + w_1 \tan \tau) \tan \phi) / ((s_1 + w_1) - (s_{2x}^- + w_{2x}^-) \tan \phi)$.

$i_4^- > [((w_1 / \tan \phi) + (w_c / \sin \phi)) + 2((s_1 / \tan \phi) - (w_c / \sin \phi)) - ((s_2 + w_2) / \cos \tau - w_1 \tan \tau) + 2(s_1 \tan \tau)] / [((w_1 / \tan \phi) + (w_c / \sin \phi)) + ((s_1 / \tan \phi) - (w_c / \sin \phi)) - ((s_2 + w_2) / \cos \tau - w_1 \tan \tau) + (s_1 \tan \tau)]$.

Thus, the impact of any non-perpendicularities in the vertical wires, both in the direction of the cut and opposite the cut, has been derived based on the system parameters and τ, the measure of angular offset of the vertical wires. The focus of this section shifts to understanding how this rotational misalignment tolerance affects the connectivity of the system.

Any non-perpendicularity in the vertical wires, τ, resulted in a new equivalent vertical wire pitch derived for both an angular offset in the direction of the cut and opposite the cut, as shown in Figure A.43.

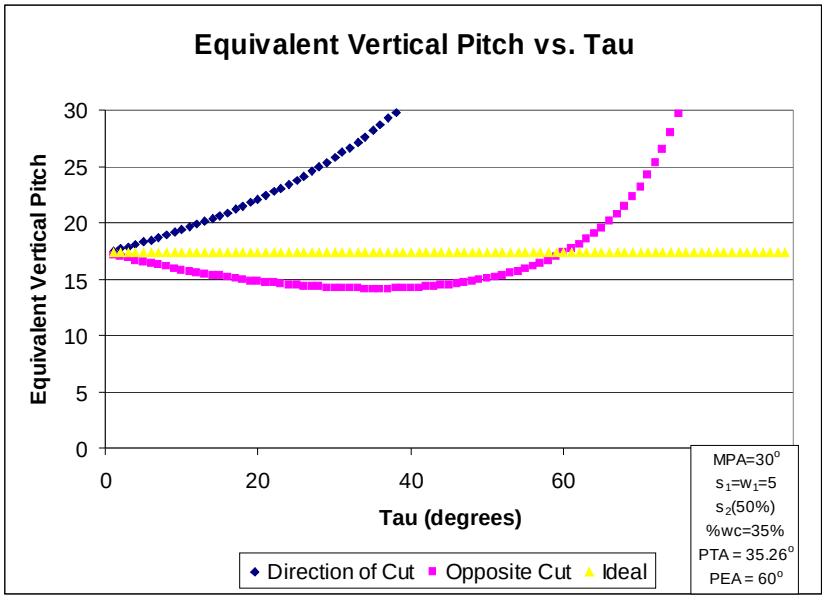

Figure A.43: Equivalent Vertical Wire Pitch

For rotation in the direction of the cut and for the range of τ between 0 and 90^o, recall that the equivalent vertical wire pitch could only increase. This is clearly seen in the above figure. However, for rotation in the direction opposite the cut, the equivalent

vertical wire pitch would decrease and depending upon the system variables, begin to increase again at what was defined to be the Pitch Turning Angle. From the above figure, one can see that at 35.26°, the equivalent vertical wire pitch for angular misalignment opposite the cut direction starts to increase again. Finally at what was derived to be the Pitch Equivalency Angle, the equivalent vertical wire pitch becomes equal to the ideal pitch once again. Recall that in the region in which the pitch is decreasing, only errors i_3 (open) and i_4 (short) can occur, while in regions in which the pitch is increasing, only errors i_1 (short) and i_2 (open) can occur. For misalignments opposite the cut angle, all types of errors can occur in different angle regions. This can be seen in Figure A.44, which superimposes i_3/i_2 on top of the equivalent vertical wire pitch for a rotational misalignment of the vertical wires opposite the angle of the cut.

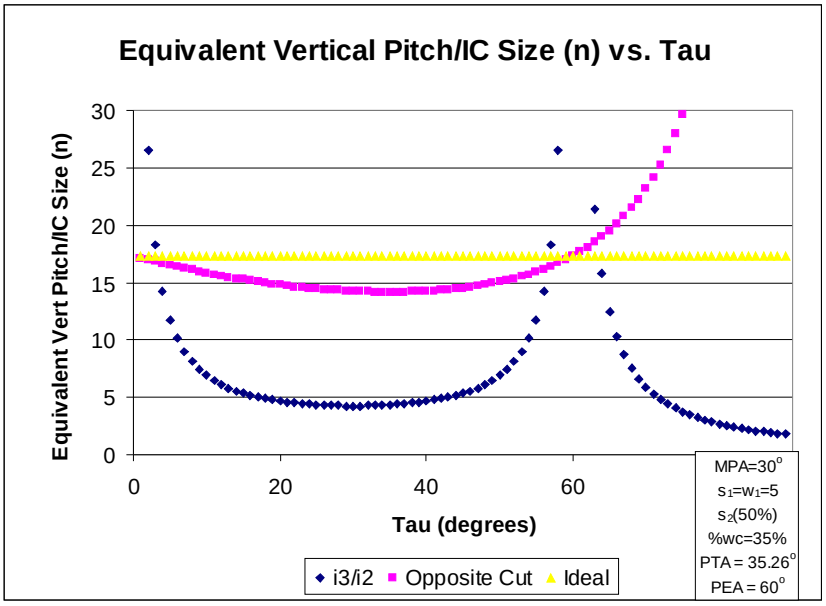

Figure A.44: Equivalent Vertical Wire Pitch Opposite Cut with i_3/i_2 Superimposed

At 0°, the system scales infinitely, as is expected. The equivalent pitch then decreases, as does the scalability of the structure. At 60°, where the equivalent pitch is equal once again to the ideal pitch, the structure once again scales infinitely. Between 0° and 60°, i_3 errors can occur while above 60°, i_2 errors can occur. While they are not the

same error, they are both opens and are therefore grouped together on full angle sweeps. Not all systems meet the required conditions to have PTA and PEA less than 90^o. For example, Figure A.45 shows such a system and shows all of the possible errors and their respective limitations on the interconnect size.

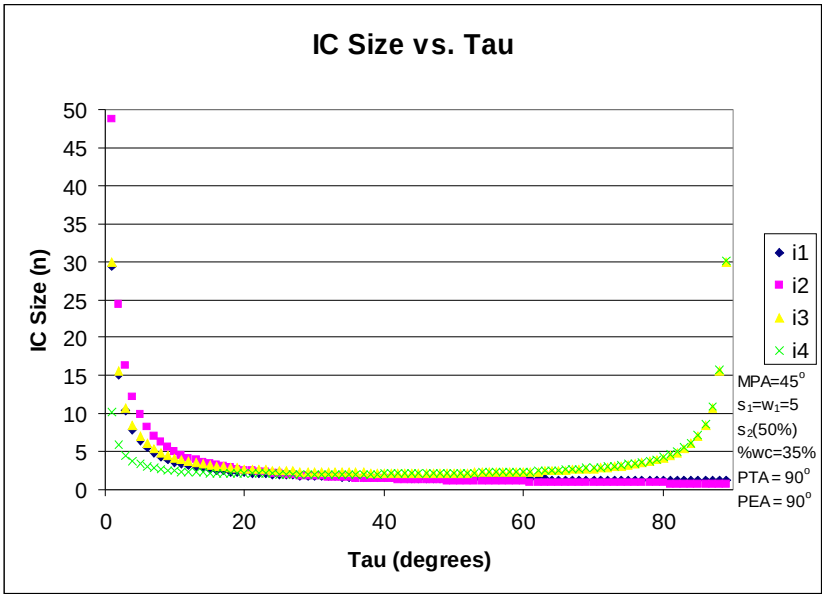

Figure A.45: Equivalent Vertical Wire Pitch Opposite Cut with i_3/i_2 Superimposed for Alternate System

In general, any rotational error in the vertical wires significantly reduced the scalability of this system. With this in mind, it is important to understand the impact of the system variables on the scalability in hopes of optimizing the system to improve this scaling. Figure A.46 shows the dependence of the system size on τ for all four types of errors while varying the Maximum Pitch Angle from 15^o to 75^o.

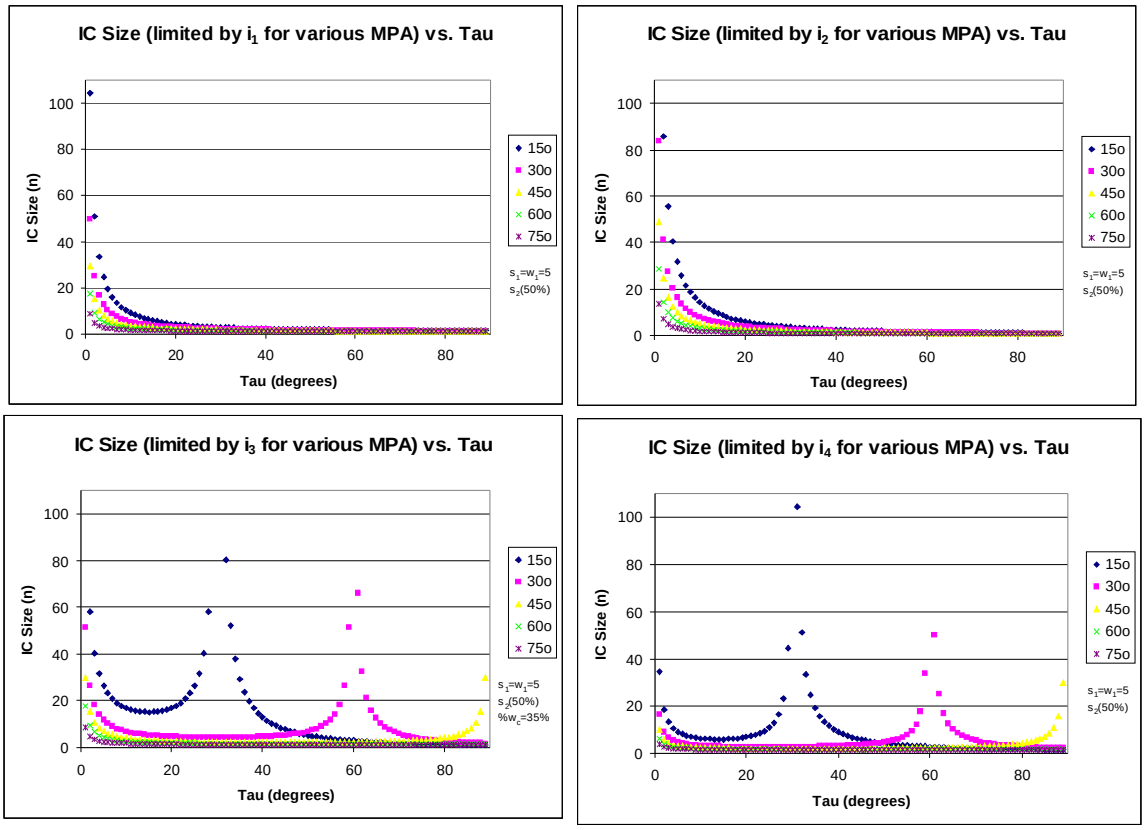

Figure A.46: IC Size vs. τ for Various Insulator Cut Angles

Clearly, the larger the insulator cut angle, the quicker the scalability degrades for all error types. Thus to improve system scalability one would employ smaller cut angles. Interestingly, for rotation opposite the cut direction, increasing the cut angle shifts the PTA and PEA towards larger angles. This is in agreement with the derivations for these equations. Next, the dependency of the scalability on the cut width is investigated. Recall that only i_2 and i_4 are dependent upon the cut width due to the chosen alignment. Of course alternate alignments could have been chosen but one alignment had to be chosen since this analysis is alignment dependent.

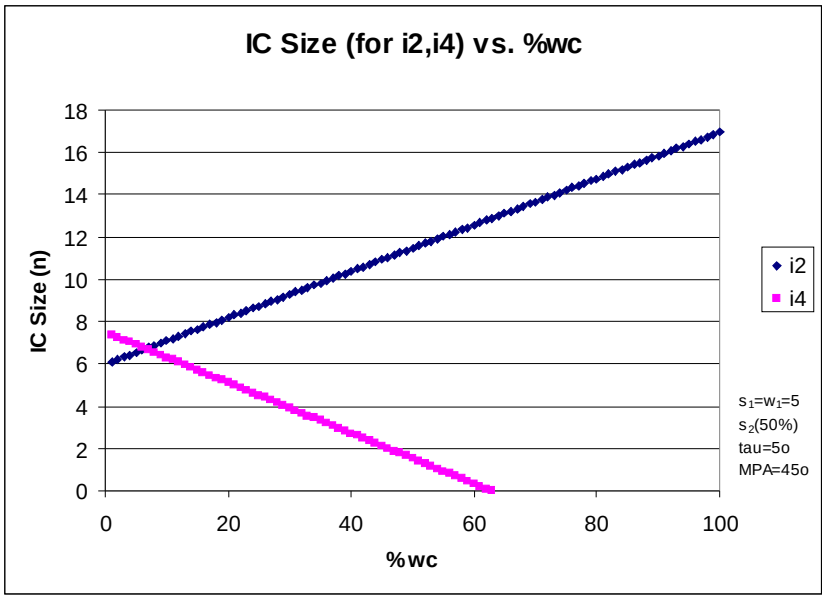

Figure A.47: IC Size vs. $\%w_c$

Clearly, it is shown in Figure A.47 that as the cut width increases, i_2 improves while i_4 degrades. This is intuitive since i_2 represents an open error, so the larger the cut width, the less likely it will miss the target junction. Meanwhile, i_4 is a shorting error, so the larger the cut width the quicker it will short a non-target junction. Falling below zero for i_4 implies that the initial state of the system is shorted. One important aspect is the linear dependence on w_c, implying that the scaling is not as strongly dependent upon the cut width than it was on the insulator cut angle. Thus, the influences of the cut angle and the cut width have been analyzed, leaving only the wire widths and spacing for both vertical and horizontal wire pitches. Figure A.48 shows the dependence of i_2 and i_4 on s_1 versus τ, and the dependence of i_1 and i_3 on s_2 versus τ.

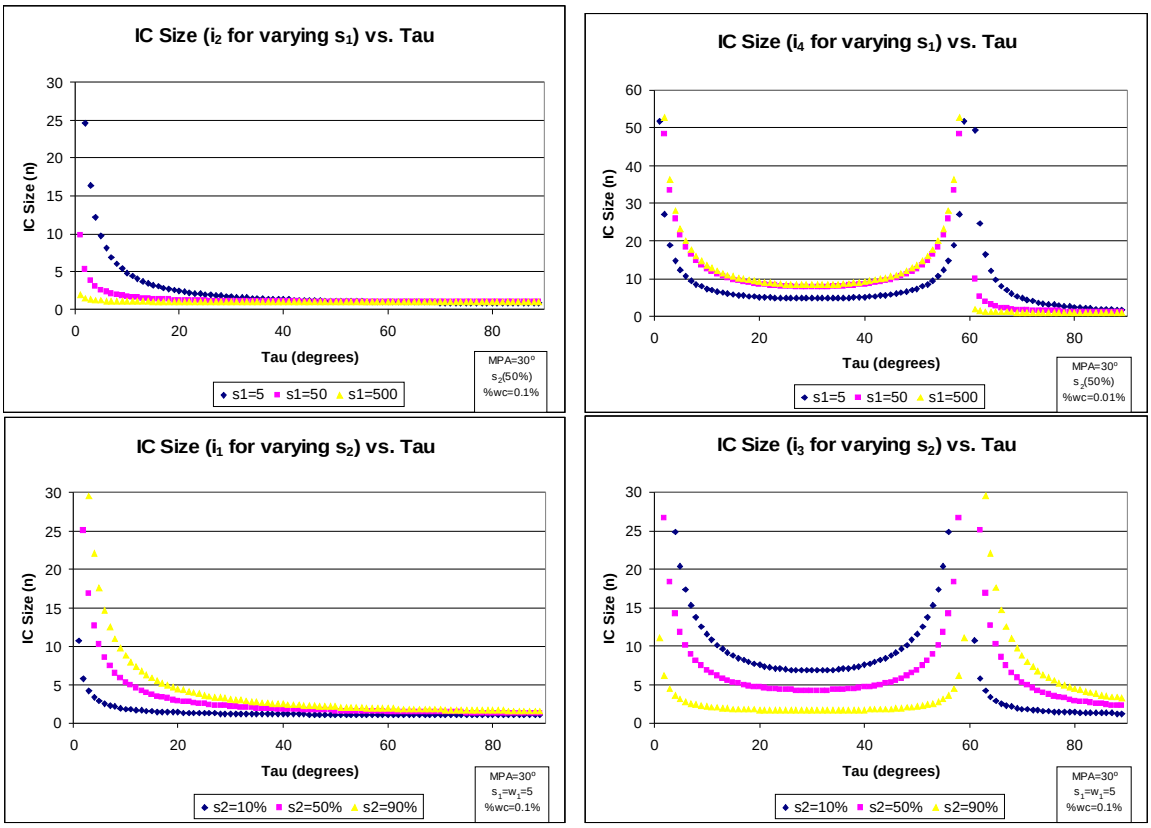

Figure A.48: IC Size vs. τ for Various Spacings

Clearly, as s_1 increases i_2 degrades while i_4 improves and similarly as s_2 increases, i_3 degrades while i_1 improves. Unfortunately this does not bode well for scaling since improving one error just makes another more restrictive. However, the dependence of i_2 and i_4 on s_2 and i_3 and i_1 on s_1 has not yet been considered. It turns out that there is no dependence of i_2 and i_4 on s_2 and i_3 and i_1 on s_1. To understand this, consider what happens to a system when only one of the spacings is increased individually, as shown in Figure A.49.

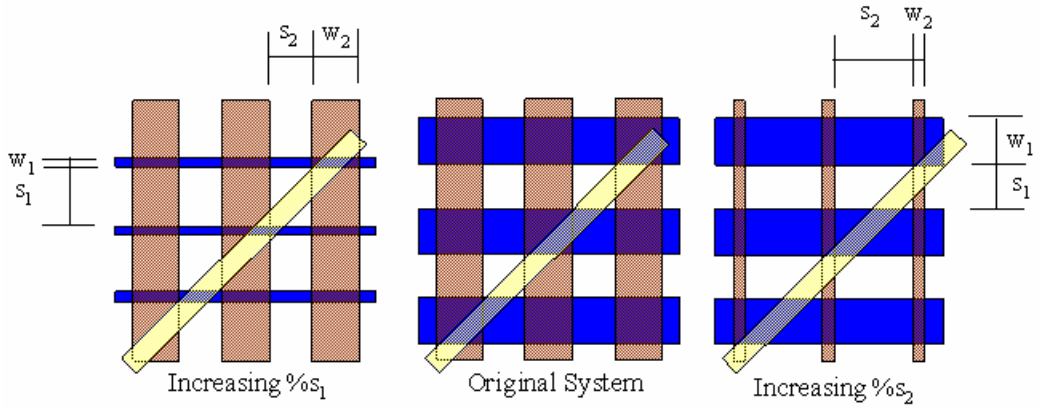

Figure A.49: Effect of Changing Spacing

In the middle of Figure A.49 is the original system. To the left, the $\%s_1$ has been increased while keeping w_c and ϕ constant. Clearly, the distances from the cut to i_1 and i_3 have not changed! Now it makes intuitive sense why i_1 and i_3 are not dependent on s_1; the distances between the cut and those errors have not changed! Meanwhile, the distance from the cut to i_4 has increased while the distance from the cut to i_2 has decreased. Recalling from above, an increase in s_1 improved i_4 while degrading i_2. Once again, this makes intuitive sense since their distances increased/decreased respectively. The same argument can be made when increasing s_2. This is a novelty of the structure that will be exploited later on in this chapter. One other interesting point is that by increasing all variables by a certain factor, one does not change the dependence of the scaling on τ. This is interesting because if the entire system scales by a certain factor, it has no impact on the potential interconnect size. This allows for the use of largely scaled structures for proof of concept experiments, at least concerning misalignment of the vertical wires.

Now that the impact of cut angle, $\%w_c$ and the vertical and horizontal wire pitches have been determined, it is important to discuss how the system might be optimized to improve connectivity. Clearly, one would want to use a small cut angle. This is a nice solution for fanout, but for nanowire interconnect where the cut angle is limited to be close to 45^o, this is not practical. There could be alternate designs with multiple cut

angles that have the potential to reduce the cut angle, however these represent rather significant design alterations. Both the cut width and pitch require a balancing act because increasing either results in improving certain errors while simultaneously degrading others. Optimization of non-perpendicularities for nanowire interconnect will therefore be very system specific, i.e. no general optimization strategy exists. These types of errors are intrinsic to all fanout and interconnect structures that require orthogonal wiring arrays.

A.11 Impact of Alternate Process Flow on Rotational Misalignment Tolerance

This section considers the impact of the alternate process flow on the rotational misalignment tolerance of the vertical wires. Figure A.50 shows how each of the four types of errors are affected by the alternate process flow.

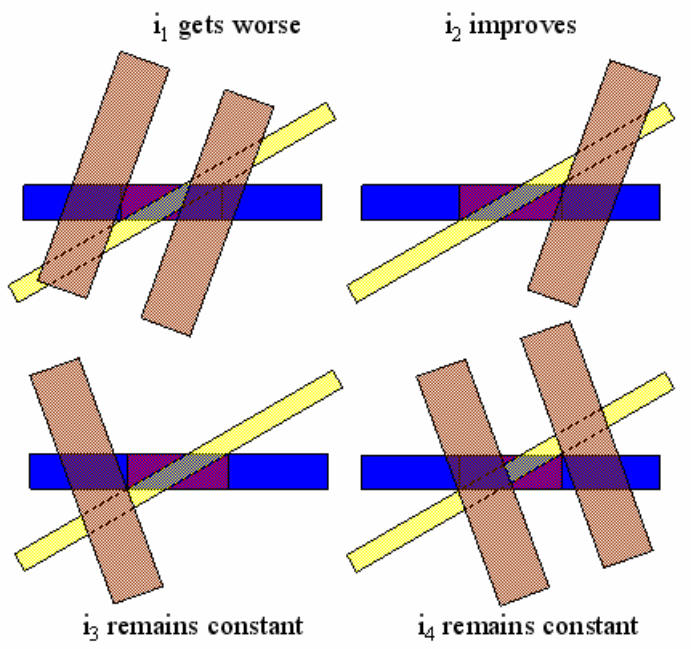

Figure A.50: Effect of Alternate Process Flow on Misaligned Vertical Wires

In this figure, the red squares represent the vias and the yellow cuts are included purely for reference. i_1 for rotation of the vertical wires in the direction of the cut actually decreases from the new design. Clearly the non-target left vwire intersects the upper-left corner of the via, and not the lower-left corner of the via where the cut would intersect. Thus, the new design adversely affects i_1. Conversely, i_2 actually improves because the cut can now intersect the bottom-right corner of the via after it has already missed the upper-right corner, where the cut would intersect. Looking at i_3 for rotation of the vertical wires in the direction opposite the cut, the intersection point is the bottom-left corner of the via. Thus, i_3 is not affected by the alternate process flow. Similarly, the critical corner for i_4 is the upper-right, which again is not affected by the process flow. Concluding, the alternate process flow adversely affects i_1, improves on i_2 and has no effect on i_3 or i_4.

Is the only effect of using the alternate process flow a tradeoff between i_1 and i_2? In fact, there are ways to avoid adversely affecting i_1. For example, altering the shape of the via could eliminate any negative impact of the alternate process flow on i_1. Recall that it was the upper-left corner that resulted in the decreasing of i_1. Consider Figure A.51 in which this corner is removed.

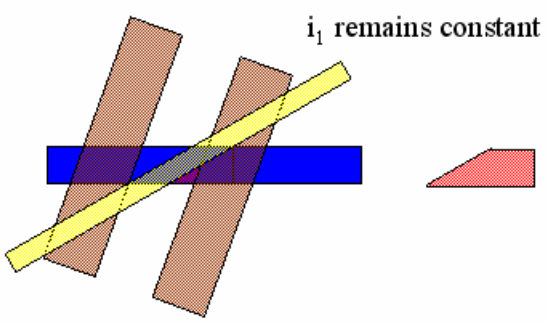

Figure A.51: Changing the Via Shape to Improve i_1

The result is that i_1 is no longer affected by the alternate process flow. There are some issues with this solution, including a potential decrease in the contact area. Another way to improve i_1 is to trade off on i_3. Increasing the percentage of the vertical wire pitch

that went into the spacing improved i_1 while adversely affecting i_3. Thus, depending on the particular constraints of the aligning system and the actual structure, the errors (shorts or opens) can be tailored. Thus, the alternate process flow can be made to have little to no impact, or even improve on the vertical wire rotational misalignment tolerance.

A.12 Comparison of Theoretical and Measured Wire Resistances

Due to the angle of the cut, the connections to each 'nanowire' are at different distances from the probe pads, which can be seen in Figure A.52.

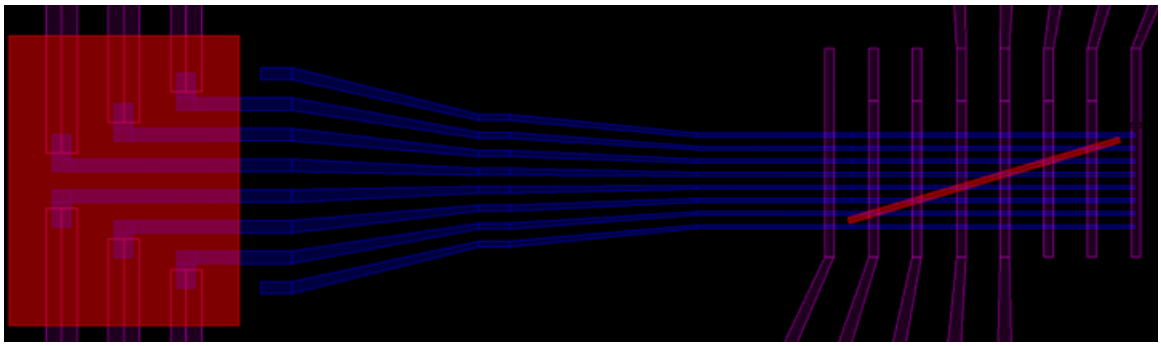

Figure A.52: Layout of Horizontal Wires

The lines drawn in blue represent the horizontal wires, while the red layers represent the insulator cut layer. For each connection, the theoretical wire resistance must be calculated based on the evaporated thickness, length and material set. Clearly the bottom left connection should theoretically have the least resistance since the current travels the least through the thinnest wires. The lines drawn in purple represent the vertical connecting wires and are fabricated thicker than the horizontal nanowires. Similarly, each wire resistance must be calculated for these wires to arrive at an expected theoretical resistance. As shown in Figure A.53, there are two sets of thick wires and one set of thin wires through which the current travels.

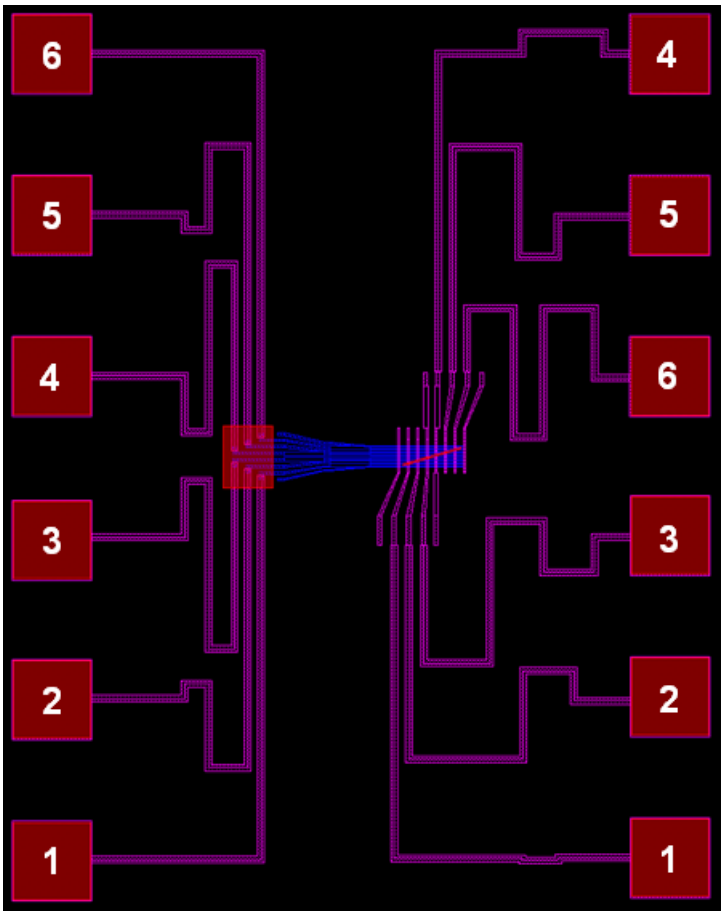

Figure A.53: Top-View of Structure Layout

The thick wires on the left of the layout are all designed with equal lengths. The resistance is given by:

$$R = \frac{r * length}{thickness * width} \qquad \textit{Equation A.8}$$

The resistivity of gold at room temperature is about 2.2×10^{-8} Ω m. [ref] The length, thickness and width of these wires are 415.1μm, 925Å, and 5μm respectively. Therefore, the resistance of the thick wires on the left of the layout is about 19.75Ω. Including the Ti adhesion layer into the calculation alters the wire resistance by less than

a tenth of an Ohm, which is statistically insignificant and is therefore excluded. Deviation in the target wire width from processing biases would have a more significant impact.

Calculating the wire resistance of the nanowires is more complicated since across their length there are multiple sections at different designed widths. The lengths and widths of each section has been listed in Table A.1.

Table A.1: Designed Lengths and Widths of Nanowires (dimensions in microns)

	Section 1		Section 2		Section 3		Section 4		Section 5		Section 6		Section 7	
Wire	L	W	L	W	L	W	L	W	L	W	L	W	L	W
6	37.6	0.6	25	0.6	30	0.8	5	1	30	1.5	18.45	2	4	3
5	30.6	0.6	25	0.6	30	0.8	5	1	30	1.5	28.5	2	4	3
4	23.6	0.6	25	0.6	30	0.8	5	1	30	1.5	38.45	2	4	3
3	16.6	0.6	25	0.6	30	0.8	5	1	30	1.5	38.45	2	4	3
2	9.5	0.6	25	0.6	30	0.8	5	1	30	1.5	28.5	2	4	3
1	2.5	0.6	25	0.6	30	0.8	5	1	30	1.5	18.45	2	4	3

Table A.2: Theoretical Wire Resistance of Nanowires

Wire	Resistance (Ω)
6	111.5
5	107.3
4	103.1
3	95.8
2	85.2
1	74.7

This analysis is repeated for the thick connecting wires on the right-side of this structure.

Table A.3: Designed Lengths and Widths of Connecting Wires (dimensions in microns)

	Section 1		Section 2		Section 3		Section 4		Section 5	
Wire	L	W	L	W	L	W	L	W	L	W
6	7.5	1.5	8.5	1.5	32	2.25	10.2	3	415.1	5
5	9.6	1.5	8.5	1.5	32	2.25	10.2	3	415.1	5
4	11.7	1.5	8.5	1.5	32	2.25	10.2	3	415.1	5
3	11.2	1.5	0	0	32	2.25	22.1	3	415.1	5
2	9.1	1.5	0	0	32	2.25	22.1	3	415.1	5
1	7	1.5	0	0	32	2.25	22.1	3	415.1	5

Table A.4: Theoretical Wire Resistance of Connecting Wires

Wire	Resistance (Ω)
6	26.5
5	26.8
4	27.1
3	26.7
2	26.3
1	25.9

Finally, to account for the probe resistance and probe to probe pad contact resistance, two probes were dropped on metal 2 and measured resistance was 14.1Ω. Thus, all of the individual theoretical resistances are tabulated and compared to the

measured resistance from the Current-Voltage characteristics from Section 3.7.2. The results are shown in Table A.5.

Table A.5: Comparing Theoretical and Measured Wire Resistances

Wire	Theoretical (Ω)	Measured (Ω)
6	108	109
5	118	117
4	128	126
3	134	133
2	137	135
1	140	141

From Table A.5 it is clear that the measured wire resistance was in agreement with the theoretically calculated resistance. Obviously the difference in the measured resistances is due to the angle of the cut as suggested. The only theoretical resistance not accounted for in this analysis was the contact resistance between the two sets of wires. However, this resistance would be relatively equivalent for each junction, and therefore only serve to shift the theoretical expectations. The trend across the wires would not change, and it is this trend that is in agreement. Factors such as the actual fabricated wire width, as suggested early, is also adding to uncertainty in the theoretical predictions. It so happens that the absolute values are in agreement, but the agreement of the relative trends is supporting the theory that the differences are due to the angle of the cut. The above analysis is for 'Structure 3'. Clearly, two other structures with different dimensions were fabricated. Table A.6 summarizes an analogous analysis for 'Structure 1'.

Table A.6: Comparing Theoretical and Measured Wire Resistances for ‘Structure 1’

Wire	Theoretical (Ω)	Measured (Ω)
6	135	135
5	145	144
4	156	161
3	164	164
2	168	168
1	172	174

Once again, the expected theoretical values for the resistance were in excellent agreement with the measured values.