ABSTRACT

GHOSH, DIPANKAR. Tunable Microwave Devices Using BST (Barium Strontium Titanate) And Base Metal Electrodes. (Under the direction of Jon – Paul Maria)

The enormous growth in the wireless communication industry and the need for low cost, reliable, high bandwidth, data links has resulted in a demand for active circuits that operate at microwave and millimeter wave frequencies. Microwave devices such as filters, phase shifters, matching networks, and antennas form an integral part of modern communication systems. Traditionally ferrite and semiconductor based material have been used in these devices. The drawback of such devices stems from the fact that semiconductor based devices have high losses at microwave frequencies and ferrite materials are slow to respond to input signals. Currently there is a huge research interest in utilizing ferroelectric thin films for tunable microwave devices since they have high tunability, low loss, fast switching speeds and good power handling capability at GHz frequencies.

Barium strontium titanate, Ba$_{1-x}$Sr$_x$TiO$_3$, 0 ≤ x ≤ 1, (BST), a solid solution perovskite, is a potential candidate for integration into microwave devices. BST ferroelectric thin films are attractive for radio frequency and microwave applications due to its high figure of merit, thermal stability and ease of integration into microelectronic circuits. However, for many non-military uses, the high cost of conventionally processed ferroelectric thin film / BST based devices is a limiting factor. This high cost stems from single-crystalline sapphire, MgO, or LaAlO$_3$ substrates, and Pt or Au metallization commonly used in microwave devices. Here we present a device process and materials complement offering a low cost alternative.
Planar interdigitated capacitors $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ (BST) thin films with Cu top electrodes were fabricated on polycrystalline alumina substrates using a single step photolithographic technique and lift-off process. RF magnetron sputtering was used for fabrication of BST thin films while Cu thin films were thermally evaporated. The dielectric tunability of the $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ IDCs was 40% for an applied electric field of 12 V/µm, which corresponds to 3 µm electrode gap spacing and a 35 volt dc bias. Low frequency (1MHz) loss measurements reveal a dielectric $Q$ (Quality factor) $\sim$ 100 while a device $Q$ of $\sim$ 30 is obtained at 26 GHz. Leakage current measurements of the BST planar varactors show current densities of $1.0 \times 10^{-6}$ A/cm$^2$ for an electric field of 10 V/µm. These dielectric characteristics (tunability and $Q$ value) are comparable to numerous reports of IDCs with BST films prepared on expensive single crystalline substrates using noble metallization. As such, this technology is significantly less expensive, and amenable to large volume manufacturing.

A tunable 3rd order combline bandpass microwave filter based on BST thin films on polycrystalline alumina substrate and Cu electrodes was fabricated and characterized at room temperature. Fabrication was done using a single step photolithographic technique and metal lift off process. Tuning was achieved using an interdigital varactor configuration (Cu / BST / Alumina). The center frequency of the filter was 1.85 GHz and was tuned to 2.05 GHz upon application of 125 V. The insertion loss was 4.5 dB at 0 V and this decreased to 3.5 dB at 125 V. The return loss was found to be better than 9 dB at all applied fields. In addition, the filter also exhibited low power consumption (< 6 µW) and low intermodulation distortion (IP3 = 38 dBm).
A microwave phase shifter based on Cu transmission lines on BST thin film/alumina substrate was fabricated and tested. The X–band (8 - 12 GHz) phase shifter showed a phase shift of 18° for an applied bias of 130 V at 10 GHz and had an insertion loss of only 1.1 dB at zero bias at 10 GHz. The return loss was better than 19 dB for all bias states. This insertion loss is among the best reported to date for a microwave phase shifter. The initial phase shifter results look promising and it exhibits a figure of merit of 17°/dB.

In this work we report the fabrication, characterization, and process optimization for tunable microwave devices using low cost materials, simple and inexpensive processing routes entirely compatible with large volume manufacturing. This thesis represents the first comprehensive demonstration of integrated microwave devices using ceramic substrates and base metallization incorporating ferroelectric thin film technology at room temperature.
TUNABLE MICROWAVE DEVICES USING BST (BARIUM STRONTIUM TITANATE) AND BASE METAL ELECTRODES

by

DIPANKAR GHOSH

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APPROVED BY:

Michael B. Steer

Mark A. Johnson

Angus I. Kingon

Jon – Paul Maria
Chair of Advisory Committee
DEDICATION

মা ও বাবাকে

To my parents
Dipankar Ghosh is from Kolkata, (formerly Calcutta), West Bengal, India. From 1995 – 1999 he attended the Indian Institute of Technology (IIT, Kharagpur) where he received the Bachelor of Technology (Hons.) degree in Metallurgical and Materials Engineering. He spent four wonderful years with great friends and had a gala time. In 1999 Dipankar completed his B.Tech thesis entitled “Synthesis and characterization of Co-cermet nanoclusters for ferrofluid applications” under the tutelage of Dr. S. Ram and Dr. S.K. Roy. For this work he was awarded the Usha Martin Endowment Award for the best senior design project work in the department.

In 1999 Dipankar enrolled in the Materials Science and Engineering program at University of Cincinnati, Ohio, USA. He worked with Dr. R.N.Singh on high temperature mechanical properties of fiber reinforced ceramic matrix composite. He received a Master of Science degree for his dissertation entitled “Crack propagation and fracture resistance behavior under fatigue loading of a ceramic matrix composite” in 2002.

In 2002 he traveled to North Carolina State University to pursue further graduate studies in the Department of Materials Science and Engineering. After a brief appointment as a Teaching Assistant, he joined the Electroceramic Thin film Group headed by Dr. Jon - Paul Maria for his Ph.D.

His research focused on integration, process development, and characterization of ferroelectric thin films in frequency agile radio frequency / microwave devices for communication systems.
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1.0 LITERATURE REVIEW

1.1 Introduction to Tunable Microwave Devices

In recent years there has been a rapid growth of communication systems including satellite, bluetooth, ultra-wide band (UWB), 3G wireless phones, and optical network systems [1]. All these systems use a number of tuned RF (radio frequency) and MW (microwave) circuits. RF frequencies refer to the 20 kHz - 300 MHz range while MW spectra range from 300 MHz - 300 GHz. To sustain this growth in the wireless communications segment it is imperative to design and fabricate frequency agile RF front ends for operation in various frequency bands. Thus frequency tunable RF and microwave components will be in huge demand due to their frequency agile characteristic [1]. In addition, high performance, cost effective, small size, and low-operation voltage components are required in the current and next generation communication systems. These requirements impose significant challenges on current tunable circuit technologies and illustrate the need for new materials, designs and technologies to meet these challenges.

Technologies that can meet such requirements for the communications spectrum (as shown in Fig. 1.1.1) will be able to meet the stringent demands on battery life, size, weight and cost constraints of modern communication systems.
Tunable circuits refer to analog circuits which contain a LC where L refers to an inductor element (units are given in H, Henry) while C refers to a capacitor element (units are given in F, Farad). The resonant frequency (f) of any MW device is inversely proportional to the square root of the product of LC. Mathematically it can be expressed as:

\[ f = \frac{1}{\sqrt{LC}} \]

Hence by changing either the L or C value the resonant frequency of the circuit can be changed. Tunable circuits are designed in such a way that they respond optimally when functioning at a specific frequency, power level or impedance, and less optimally under alternative conditions.

Wireless systems are usually a more cost effective way of providing communication service than wired networks. Tunable circuits, such as filters, matching
networks, antenna, and phase shifters offer the flexibility to adapt to changes in various operating conditions, such as frequency, RF drive level or impedance environment; properties that are very attractive from a wireless communications perspective. These components can be tuned over a broad operational range, for ex. filters can work in multiple frequency spectra and different standards, and impedance matching networks can be adjusted for various amplifier power level. Thus, tunability in these circuits gives the designer a great advantage in meeting the strict frequency and power requirements of wireless communications systems, even in the changing operating environment intrinsic to such systems.

The potential of using ferroelectric materials for integration into tunable microwave devices have been recognized since the early 1960’s \cite{3, 4} and their properties have also been well documented in the open literature. The original idea of utilizing bulk ferroelectric materials in tunable devices was not very successful because of difficulty achieving low capacitance values with good tunability values at moderate dc voltage levels. Also integration of bulk films in devices is cumbersome. In the past decade or so, extensive work has begun to realize this potential of utilizing ferroelectric thin films in tunable devices. This resurgence in interest is mainly driven by two factors:

(a) The realization that ferroelectric thin films in tunable MW circuits will lead to dramatic miniaturization and reduction of manufacturing cost.

(b) Due to recent advances in ferroelectric thin film technology the quality of ferroelectric films has improved to the point where properties are attractive from device perspective, and integration with semiconductor technology is realistic.
Ferroelectrics offer an excellent array of properties such as variation in capacitance (and hence the dielectric permittivity, $\varepsilon$) with applied voltage, low dielectric loss (tan $\delta$), high power handling capability, and possibility of integration into microelectronic components [5]. Thus components using ferroelectric thin films can be used in the field of microwave engineering for field dependent capacitors, frequency agile filters, variable beam scanning phase shifters, tunable resonators, and matching networks for amplifiers and antennas.

### 1.1.1 Competing technologies for Microwave Devices

To realize and appreciate the capabilities and potential of using ferroelectric thin films in tunable circuits it is important to understand the various competing technologies for making MW devices. Currently there are five enabling technologies for the design and fabrication of continuous tunable circuits. These are based on mechanical tuning, ferrite materials, MEMS, semiconductor varactors and ferroelectric materials. The earliest forms of tunable circuits were all based upon mechanical tuning, e.g., the rotary vane adjustable waveguide phase shifter first proposed by Fox in 1947 [6]. Mechanical circuits are inexpensive, easy to fabricate and have very low loss and possess good power handling capability. However they come in large sizes and have rather low tuning speed and are therefore cumbersome.

The first electronically variable ferrite phase shifter was reported by Reggia and Spencer in 1957 [7]. Ferrites are made by mixing iron oxide with oxides or carbonates of one or more metals such as zinc (Zn), manganese (Mn), nickel (Ni) or magnesium (Mg) and require tunable magnetic fields to operate. Ferrites are capable of handling large
power levels and have faster switching times (few $\mu$s ~ tens of $\mu$s) compared to mechanical tuning circuits. On the downside ferrite based circuits have large size and mass and have high power consumption. In addition tunable ferrite devices are difficult to integrate with microstrip, stripline and finline circuits because of the tuning circuit geometry (ex. an induction coil).

In the 1960s, semiconductor diodes (based on the semiconductor p-n junction) were introduced in tunable circuits for the first time and are the dominant devices for imparting tunability [8, 9]. They have small dimensions (size in $\mu$ms), very fast tuning speeds ($<1\ \mu$s for PIN diode and $<1\ \text{ns}$ for FET), and high tunability (3:1~10:1). In addition, they can be easily integrated with monolithic microwave integrated circuits (MMICs). However semiconductor based varactors suffer from the junction noise and have poor power handling capability. Semiconductor varactors perform well at low frequencies but suffer from Q degradation at higher frequencies due to series resistance losses. A Schottky barrier semiconductor varactor consists of a p-n junction and the capacitance is controlled by the reverse bias voltage which in turn also influences the junction width and the capacitance. To get high tunability, the p-n junction should be lightly doped so that the depletion width is significantly changed with small changes in applied voltages. However, since the undepleted portion of the semiconductor layer also acts as one of the electrodes, lightly doped layers are resistive and contribute to high loss at MW frequencies. Another problem is poor RF power handling capability. Low capacitance varactors, which are necessary for MW circuits, are made by decreasing the capacitor area ($A \sim \mu\text{cm}^2$). Typically the space charge depletion widths in such devices are about 1 - 5 $\mu$m and thus the maximum amount of power that can be
transmitted without compromising signal integrity is about 1 mW. Thus it is difficult to
design p-n junction based varactors which simultaneously meets the requirements of high Q and good power handling capabilities at GHz frequencies.

More recently in the early 1990s, interest has emerged in microelectromechanical systems (MEMS) where tunability is obtained by the physical movement of a component which changes the capacitance of the device [10]. MEMS devices have low loss at RF and MW frequencies and can handle higher power levels. These devices can be very small and use electrostatic, electrostrictive, piezoelectric or thermal effects to produce the movement [11]. However, they have some disadvantages that include low tunability (<1.5:1, or 50%), slow switching speed (2 - 100 µs), and high bias voltage (50 - 100 V) requirements. In addition, they require stringent hermetically sealed packaging, which is costly and therefore makes them difficult and expensive to integrate.

The final approach for making tunable devices is to employ ferroelectric based varactors [12-21]. When a direct-current (dc) voltage is applied to a ferroelectric film, the dielectric constant of the film can be decreased by nearly an order of magnitude, thus changing the high-frequency wavelength in the microwave device.

They exhibit fast tuning speed, low loss at RF and microwave frequencies, and can handle more power than semiconductor varactors. In addition they are small sized and lightweight and since they tune via an applied DC field, they have low power consumption. The C-V curve is symmetric with respect to the bias voltage; thus there is no requirement for reverse bias as with semiconductor varactors. They can be also used in bulk form so that planar circuits such as coplanar waveguide and microstrip lines can be directly fabricated on them. In addition, thin film ferroelectrics can be used in both
parallel plate and interdigital capacitor configuration, both of which offer reasonable integration possibilities for microelectronic circuits. The recent results obtained from ferroelectric varactors indicate their potential for making tunable RF front ends [17-21].

Table 1.1.1.1 shows a chart for comparing various technologies for fabricating tunable circuits based on various parameters such as tunability, Q factor, biasing field, tuning speed, power handling, IMD (Intermodulation distortion), packaging, and cost of manufacturing.

Table 1.1.1.1: Competing technologies for tunable circuits

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<tbody>
<tr>
<td>Tunability</td>
<td>Moderate</td>
<td>Good</td>
<td>High</td>
<td>Good</td>
<td>Very good</td>
</tr>
<tr>
<td>Q factor</td>
<td>Very good</td>
<td>Very good</td>
<td>Moderate</td>
<td>Very good</td>
<td>Very good</td>
</tr>
<tr>
<td>Control voltage</td>
<td>-</td>
<td>&lt; 20V</td>
<td>&lt; 20V</td>
<td>2-20 V</td>
<td>50-100 V</td>
</tr>
<tr>
<td>Tuning speed</td>
<td>Slow</td>
<td>Moderate</td>
<td>Fast</td>
<td>Fast</td>
<td>Slow</td>
</tr>
<tr>
<td>Power handling</td>
<td>Good</td>
<td>Good</td>
<td>Moderate</td>
<td>High</td>
<td>Moderate</td>
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<tr>
<td>Packaging</td>
<td>Standard</td>
<td>Standard</td>
<td>Hermetic</td>
<td>Standard</td>
<td>Hermetic</td>
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<tr>
<td>Cost</td>
<td>Low</td>
<td>Low</td>
<td>Moderate/High</td>
<td>Low</td>
<td>High</td>
</tr>
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</table>
Since devices based on ferroelectric materials have a wide spectrum of excellent properties they present an attractive technology for the design of tunable circuits. This technology may allow microwave devices that have very low power requirements and are lightweight, compact, robust, and affordable from a manufacturing point of view.

1.2 INTRODUCTION TO FERROELECTRICITY

1.2.1 Historical background

From a historical point of view the Greeks were the first to observe the effect of polar materials, pyroelectricity in this case, more than twenty-three centuries ago [22]. The Greek author Teophrastus noted that the mineral “lyngourion” (probably tourmaline) showed the property of being able to attract little bits of wood. The tourmaline group has the general formula of \( AX_3 Y_6 (BO_3)_3 Si_6 O_{18} (O, OH, F)_4 \). The A site can be occupied by either calcium or sodium. The X can be aluminum, iron, lithium or magnesium. The Y is usually aluminum, but can also be chromium or iron. Sometimes potassium can be found in the A position, some manganese can be in the X position and some vanadium can occupy the Y position, but these elements are usually not represented in the formulas of the tourmaline members. This behavior occurred upon heating or cooling of the mineral in question and thus Teophrastus had observed the accumulation of electrostatic charges due to temperature changes, thus the pyroelectric effect.

This was the first recorded observation of the broad field of ferroelectricity. In the 18th century, similar investigations of pyroelectricity were utilized to understand the nascent field of electrostatics. During the nineteenth century, research in pyroelectricity became more quantitative. As electrical measuring techniques became more sophisticated
the study of pyroelectric materials became more systematic [23]. In the following century these contributions were applied to other emerging fields such as thermodynamics, mineralogy, crystal physics, etc.

1.2.2 Piezoelectricity

Piezoelectricity was discovered in 1880 by the Curie brothers [24] in France when Jacques and Pierre Curie speculated that the electrical effects due to non-uniform heating of quartz crystals might be caused by pressure. Piezoelectricity is a phenomenon where dielectric displacements are induced in a crystal when appropriate stresses are applied. The effect is linear, with reversal of the stimulus resulting in a reversal of the response [25].

All polar crystals show piezoelectricity. In the direct piezoelectric effect electrical charge is generated in the crystal when mechanical stress is applied and is given by the following equation (for small values of stress):

\[ D_i = d_{ijk} \cdot \sigma_{jk} \]

where \( D_i \) is the dielectric displacement, \( d_{ijk} \) is the piezoelectric coefficient and \( \sigma_{jk} \) is the stress applied.

In the indirect piezoelectric effect the converse effect is observed, i.e., when an external electrical field is applied a strain is generated in the crystal and this is represented in the following equation:

\[ \varepsilon_{jk} = d_{ijk} \cdot E_i \]
where $\varepsilon_{jk}$ is the strain and $E_i$ is the applied electric field. The direct piezoelectric effect is used in mechanical sensor applications while the indirect piezoelectric effect is used in mechanical actuator applications.

Forty years after the discovery of piezoelectricity, Joseph Valasek [26] in the USA discovered ferroelectricity in 1921 while studying Rochelle salt (NaKC$_4$H$_4$O$_6$, 4H$_2$O). However Rochelle salt was first prepared by Elie Seignette nearly three centuries earlier in La Rochelle, France, and it was known as Siegnette salt in Europe from where the term Siegnette-electricity was coined to describe ferroelectricity [27]. Later potassium dihydrogen phosphate and a number of its isomorphs were recognized as ferroelectrics. Then during the Second World War, Barium Titanate (BaTiO$_3$), the prototype of many oxide ferroelectric perovskites was discovered [28]. This was a great engineering breakthrough and for many years BaTiO$_3$ was used as a high K dielectric in many engineering applications. After this discovery, research in the field of ferroelectric materials increased in a spectacular way. In the second half of the 20th century significant research was done to investigate the piezoelectric, pyroelectric, and ferroelectric effects of materials and today these materials are commonly used in all fields of engineering [29].

1.2.3 Ferroelectricity

Ferroelectric materials have permanent electric dipoles and therefore exhibit a spontaneous polarization, i.e. polarization even without an applied field. Among the 32 crystal classes (point groups) 11 of them have a center of symmetry. Being centrosymmetric they cannot have a polar character and hence cannot be ferroelectrics.
When an external electric field is applied the positive and the negative charged atoms will be displaced with respect to the equilibrium position in the unit cell. The resulting strain of the cell will be the same upon reversal of the electric field, thus showing electrostrictive character. The 21 remaining crystal classes lack a center of symmetry, they may have one or more polar axes, and (except for the cubic class 432) show piezoelectric effects. However, just piezoelectric response does not guarantee spontaneous polarization in any material. In some cases, e.g., quartz (a piezoelectric material), polar directions are arranged in such a way that they self-compensate and cancel out spontaneous polarization and only exhibit a piezoelectric response when subjected to inhomogeneous stress and not hydrostatic stress. Among the 21 point groups without an inversion center there are 10 polar groups which possess a unique polar axis. Such crystals may display spontaneous polarization parallel to the polar axis. This spontaneous polarization is temperature dependent, resulting in the pyroelectric effect (variation in the degree of polarization due to change in temperature). All ferroelectric crystals belong to a pyroelectric crystal class and have the additional property that an external field can reverse their spontaneous polarization. Thus ferroelectric character cannot be determined solely from crystallographic characterization. This reversible polarization response manifests itself as a hysteresis loop in the response of polarization to an external electric field which is very similar to the hysteresis loop seen in ferromagnetic materials [27, 29].

In general ferroelectric properties may be summarized as follows:

1. Ferroelectric materials possess a unique polar axis and therefore lack a center of symmetry and therefore contain electric dipoles in the lattice.
They undergo a transformation from a higher crystal symmetry paraelectric phase to a lower crystal symmetry ferroelectric phase when cooled below a certain temperature known as Curie temperature \( T_c \). The dielectric permittivity rises to a peak at the Curie temperature and above that it decreases according to the well known Curie-Weiss law which is given below:

\[
\varepsilon_r = \frac{C}{(T-T_o)}
\]

where \( \varepsilon_r \) is the dielectric permittivity, \( C \) is the Curie constant and \( T_o \) is the Curie-Weiss temperature \( (T_o \leq T_c) \). At temperatures close to the Curie point, other thermodynamic properties (elastic, optical, and thermal properties) of ferroelectric crystals also exhibit large anomalies.

When cooled below the Curie temperature spontaneous polarization occurs and the higher to lower symmetry crystal transformation causes an increase in the crystal volume leading to a strain in the system. In order to minimize this strain the system exhibits domain structure which is a hallmark of ferroelectric materials.

Thus domains are regions of uniformly oriented spontaneous polarization in a ferroelectric crystal. Domains contain uniform alignment of electric dipoles and the boundary between two domains is called the domain wall. The domain walls typically range in thickness from 1-10 lattice parameters across, and 90° domain walls are thicker than 180° domain walls. They can be regarded as abrupt changes in the polarization direction. Domain walls are characterized by the angle between the directions of polarization on either side of the wall. Generally, domains are formed to reduce the energy of the system. The size and structure of the domains depend on many factors.
including crystal symmetry, defect structure, magnitude of the spontaneous polarization, grain size, as well as sample geometry and the method of sample preparation [30, 31].

1.2.4 Dielectric constant of ferroelectric thin films

The physical quantity that describes the stored electric charge per unit area is called the electric displacement vector \( \mathbf{D} \) and it is expressed as follows:

\[
\mathbf{D}_i = \varepsilon_0 \mathbf{E}_i + \mathbf{P}_i
\]

where \( \varepsilon_0 \) is the permittivity of free space, \( \mathbf{E}_i \) is the applied electric field, and \( \mathbf{P}_i \) is the induced polarization of the material.

The net polarization can be written in terms of the susceptibility as follows:

\[
\mathbf{P}_i (\mathbf{E}) = \varepsilon_0 \chi_{ij} \mathbf{E}_i
\]

where \( \chi \) is the dielectric susceptibility.

Thus the relative permittivity can be defined in terms of the susceptibility that is directly related to the polarization mechanisms in a material.

\[
\mathbf{D}_i = \varepsilon_0 (1 + \chi_{ij}) \mathbf{E}_j = \varepsilon_0 \varepsilon_r \mathbf{E}_j
\]

where \( \varepsilon_r \) is the relative permittivity given by:

\[
\varepsilon_r = \frac{\varepsilon}{\varepsilon_0}
\]

The relative permittivity is therefore the ratio of the permittivity of the material (\( \varepsilon \)) to the permittivity of free-space (\( \varepsilon_0 \)). It is thus a direct measure of the polarizability of a material and will govern both the phase variation and attenuation of an imposed field in the material [29]. Thus, is a complex quantity with both real and imaginary parts and can be written as:

\[
\varepsilon_r = (\varepsilon' - j\varepsilon'') = \varepsilon' (1 - j \tan\delta)
\]
The real part of the permittivity ($\varepsilon'$) is the dielectric constant and is determined by the magnitude of the polarization. It determines the amount of electrostatic energy stored per unit volume in a material for a given applied field, i.e. the amount of charge stored in a capacitor. The imaginary component of the permittivity ($\varepsilon''$) is called the loss factor and is governed by the lag in polarization upon application of the field and the energy dissipation associated with charge polarization. It represents the energy loss in a material (heat). This energy loss appears as an attenuation of the applied field and is usually measured relative to the dielectric constant in terms of the loss tangent ($\tan\delta = \varepsilon''/\varepsilon'$). In terms of an electrical circuit, $\tan\delta$ represents the resistive part of the impedance and is directly proportional to the electrical conductivity. For most good dielectrics, the loss angles are very small and nearly constant over a wide range of frequencies. For this reason the loss tangent $\tan\delta$ is usually quoted as a figure of merit of capacitor. For tunable device applications one possible dielectric quality factor $Q$ can be defined as $Q = (1/\tan\delta)$.

1.2.5 Polarization Mechanism in ferroelectrics

The polarization response in a ferroelectric material is the sum of two basic mechanisms: (a) the intrinsic contribution due to interactions of the lattice dipoles with the external stimulus and (b) the extrinsic response due to movement of domain walls and alignment of defects [32].

When an external electric field is applied to a ferroelectric crystal, the dipoles become stretched thus creating a larger polarization. An ideal ionic crystal can be assumed to contain harmonic oscillators, where the restoring force is linear function of...
the displacement. However in a real ionic crystal an anharmonic oscillator model is valid due to the local field created by the neighboring atoms. In such crystals spontaneous polarization occurs when the dipole – dipole interaction force is greater than the restoring elastic force. It has been shown that crystals whose oxygen octahedrons are arranged in certain configuration have higher fields and hence higher dipole-dipole force, e.g., when octahedrons are connected through their corners as in perovskites. Also oxygen octahedrons which contains transition metal ions, e.g., Ti$^{4+}$, Zr$^{4+}$ etc., that have noble gas electronic configuration after elimination of the s and d shell electrons, show higher electronic polarizability. Octahedrons with such ions have a large number of electronic states with similar energies and a relatively small gap between the s and d bands. Thus transition of electrons to a higher excited state is relatively easier and this ensures a high electronic polarizability of the octahedron [32]. These constitute the intrinsic (i.e. lattice response) contribution to the polarization mechanism.

The movement of the domain wall and defects under external electric and mechanical fields also contributes to the dielectric constant as well as the piezoelectric and elastic constants and increases the net polarization and constitutes the external (i.e. non lattice) response to polarization [27, 31]. In real ferroelectric materials, electrical and elastic defects and imperfections are always present that might interact with domain walls in various ways. In most cases the defects inhibit domain-wall movement, thus reducing the polarization, and this is known as domain wall pinning or clamping. Some common examples of domain wall pinning defects are oxygen vacancies and electrons trapped in the domain-wall area. The study of these extrinsic contributions is much more
complicated, since a detailed knowledge of the domain-wall structure, type of defects present, and their possible interaction with domain walls is often lacking.

When doing CV (current voltage) measurements using an impedance analyzer it is possible to apply a small-amplitude AC signal along with a DC bias on a ferroelectric sample as shown in Fig 1.2.5.1. The signal is now a small AC ripple superimposed on a DC voltage. The small initial rise in the permittivity value with DC field can be attributed to increased movement of the domain walls which become ‘free’ from defects which lock them at zero-DC field. Also partial switching of some domains having small coercive fields contributes to this increased permittivity [31, 32].

As the applied DC field is increased even further, the extrinsic contribution is reduced because most of the domains have been switched or have become immobile due to elastic constraints [29, 32, 33]. Ideally the sample becomes a single domain structure and only lattice or intrinsic contributions are present. Therefore, at high applied fields, the AC signal is probing primarily the intrinsic contribution to dielectric response.
As the DC bias is decreased, the constraints are gone and the domain walls can begin to move in response to the AC voltage, and thus the dielectric response increases. Domain wall motion involves energy and thus creates dielectric loss. Thus in the CV curve we observe that capacitance and dielectric loss peaks at zero bias (when domains can fully switch and the material is dielectrically soft) and the values are at minimum at high DC bias (when there is no further domain wall movement) [31]. This gives rise to the typical “bell shaped” CV curve that determines the tunability of a ferroelectric material.
Ferroelectrics display a characteristic “butterfly loop” in their capacitance voltage relationships, as shown in Fig. 1.2.5.1. The maxima in the CV plot for a ferroelectric show can show two distinct peaks. This is due to different coercive fields for 180° and non-180° domains present in the ferroelectric sample [31, 32].

As explained in the earlier section when a ferroelectric material is heated above the Curie temperature (T_c), it transforms into a higher crystal symmetry paraelectric or non-polar phase. This phase is characterized by the absence of any hysteretic behavior, unlike the ferroelectric phase, and hence the CV response of a paraelectric material does not show any “butterfly loop” characteristics.

The dielectric response of ferroelectrics can also be explained by the conventional Landau theory and is based upon an expansion of the Helmholtz free energy (F) with respect to the polarization (P) [34]. For the situation where the polarization is collinear with the macroscopic electric field E in the material, the Helmholtz free energy (F) is given by the following equation:

$$F= \left(\frac{\alpha}{2}\right) P^2 + \left(\frac{\beta}{2}\right) P^4$$

From equation of state we know that \(\frac{\delta F}{\delta P} = E\). Differentiating the above equation with respect to P we get,

$$E= \left(\frac{\delta F}{\delta P}\right) = \alpha P + 2\beta P^3$$

The relative dielectric permittivity (\(\varepsilon\)) is given by:

$$\varepsilon = \left(\frac{1}{\varepsilon_0}\right) \left(\frac{\delta P}{\delta E}\right) = \left(\frac{1}{\varepsilon_0}\right) \left\{1/ (\alpha + 6\beta P^2)\right\}$$

This expression describes the dielectric permittivity both in the presence and absence of an external DC bias field. In the absence of DC bias field, P = 0, and we get:

$$\varepsilon = \left(\frac{1}{\varepsilon_0\alpha}\right)$$

18
In the presence of a DC field we get:

$$\varepsilon_{DC} = \left(1/ \varepsilon_0 \right) \left\{1/ \left(\alpha + 6\beta P_{DC}^2\right)\right\}$$

where $P_{DC}$ is the polarization induced by the bias field. Thus we see that under an applied external field the denominator in the above equation increases and thus $\varepsilon$ decreases as external bias is increased. Thus the dielectric permittivity is maximum at zero bias and goes down with increasing DC bias.

**1.2.6 Tunability**

For microwave circuits the most important property of ferroelectric circuit elements is the strong dependence of their dielectric permittivity ($\varepsilon$) on the applied bias electric field ($E$). This characteristic is commonly known as tunability ($n$) defined as below:

$$n\ (\%) = \{100 \times (\varepsilon_{(\min\ V)} - \varepsilon_{(\max\ V)}) / \varepsilon_{(\min\ V)}\}$$

where $\varepsilon_{(\min\ V)}$ and $\varepsilon_{(\max\ V)}$ are the dielectric permittivity values at the minimum applied bias and maximum applied bias respectively.

Another way of defining tunability is by the ratio of the dielectric permittivity of the material at zero electric field to its permittivity at some non-zero electric field, as given by:

$$n = (\varepsilon_{(\min\ V)} / \varepsilon_{(\max\ V)})$$

The dielectric loss in ferroelectrics, the second most important microwave metric, is not as negligibly small as that of many common microwave dielectric ceramics. Dielectric loss tangent (tan $\delta$) must be taken into account while designing a MW circuit using ferroelectric material. The temperature dependence of the dielectric permittivity at
the operation temperature interval is another important issue [34]. Usually there is a trade
– off between tunability and loss tangent and the MW engineer has to judiciously choose
the material with the optimal trade-off between these two parameters for a better device
performance. This optimal trade-off may be found by a parameter called the figure of
merit (FOM) given by:

\[ FOM = \frac{\text{tunability}}{\text{loss tangent}} \]

Usually to have a high FOM, ferroelectric materials used in MW devices are in their
paraelectric state close to the Curie temperature to ensure high dielectric permittivity,
tunability and low loss tangent. One must realize, however, that figures of merit are of
limited use when comparing materials because the figure of merit calculation may change
dramatically depending on the application of interest.
1.3 Introduction to BST thin films

1.3.1 Materials science of BST thin films

BST (Barium Strontium Titanate, $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$, $0 \leq x \leq 1$) is a solid solution of $\text{BaTiO}_3$ and $\text{SrTiO}_3$. $\text{BaTiO}_3$ is ferroelectric at room temperature (Curie point, $T_c = 130^\circ\text{C}$) while $\text{SrTiO}_3$ is a quantum paraelectric or incipient ferroelectric (extrapolated Curie point, $T_c < 0\text{ K}$) \[34\]. The lattice parameter and the Curie temperature depend on the $(\text{Ba} / \text{Sr})$ ratio which can be modified. Another important parameter is the $\{(\text{Ba} + \text{Sr}) / \text{Ti}\}$ ratio which should be as close to 1 as possible for optimum electrical properties \[35\].

$(\text{Ba, Sr}) \text{TiO}_3$ crystals exist in both cubic and a tetragonal symmetry depending on composition $(\text{Ba} / \text{Sr})$. The transformation point of the crystal system is the Curie temperature $(T_c)$. If temperature is below the Curie temperature BST exhibits tetragonal symmetry (polar phase) while at temperatures above the Curie temperature, it has cubic symmetry (paraelectric phase). BST belongs to the perovskite family (named after the mineral $\text{CaTiO}_3$) which has the general formula $\text{ABO}_3$. In the structure $\text{ABO}_3$ the A site can be occupied by a cation with oxidation states of +1, +2, or +3 while the B site is occupied by a cation with oxidation states of +3, +4 or +5. In BST, the A site is occupied by Ba and Sr (oxidation states of +2) atoms while B site is occupied by Ti (oxidation states of +4) while O ion is in the oxidation state of -2. The distribution of different atoms in the BST crystal cell is shown in figure 1. $\text{Ba}^{2+}$ and $\text{Sr}^{2+}$ and ions are located in the eight angular point seats of the cubic crystal cell, and $\text{O}^{2-}$ ion is located in the face center of the three pairs of parallel faces, while $\text{Ti}^{4+}$ is located in the center of the cubic cell. The spontaneous polarization in BST ferroelectric state is usually attributed to the distortion of both cation and anion sublattices.
In the perovskite structure the A and B sites can accommodate many other ions with different electric charges and radii, but the relation between the ion radii must satisfy the Goldschmidt structure factor [36] which is given by:

\[ t = \frac{(r_A + r_O)}{\left(\sqrt{2} \,(r_B + r_O)\right)} \]

where \( r_A \) is A ion radius, \( r_B \) the B ion radius, \( r_O \) the \( O^{2-} \) ion radius, and \( t \) is the Goldschmidt structure factor. Usually for achieving the perovskite structure \( t \) should be between 0.8 and 1.1. Ideally it should be as close to 1 as possible for getting cubic symmetry.

Fig 1.3.1.1: The perovskite unit cell of BST (without and with the application of an electric field)
Let us examine this tolerance factor for BST. Putting the values for $r_{\text{Sr}} = 0.127$ nm (coordination number is 12), $r_{\text{Ba}} = 0.143$ nm (coordination number is 12), $r_{\text{Ti}} = 0.064$ nm (coordination number is 6), and $r_{\text{O}} = 0.132$ nm (coordination number is 6) we have $t_{\text{Sr}} = 0.934$, and $t_{\text{Ba}} = 0.992$. Therefore both are within tolerable limits in the allowance factor range, and the structure is stable for a perovskite. Also both Ba$^{2+}$ and Sr$^{2+}$ can replace each other to form a continuous solid solution, leading to different cell parameters and a smoothly varying Curie temperature. The crystal lattice parameter increases from 3.905 Å (lattice parameter for SrTiO$_3$) to 3.994 Å (lattice parameter for BaTiO$_3$) with reduction of strontium content or the increase of barium content. The $T_c$ drops by 3.4 °C for every mole % addition of the Sr content to the original BaTiO$_3$ content [37]. The effect of various compositions on the transition temperature of BST is shown in Fig 1.3.1.2.

Fig. 1.3.1.2: Illustration of various compositions on the lattice parameter and Curie temperature of BST [38].
In the case of bulk polycrystalline BST ceramic the relationship between the Curie temperature and barium content was derived as \( T_C = (371x - 241) \) where \( x \) is the Ba content and in the case of thin film BST the equation was \( T_C = (185.23x - 176.04) \) according to Tahan et al. [39]. The difference in the Curie temperature between bulk polycrystalline and thin film BST have been widely explained by a “clamping effect” of the substrate on the thin film [39]. However these explanations are not consistent with known relationships between mechanical stress and \( T_C \) of single crystal ferroelectrics, thus are unlikely to provide an accurate description.

### 1.3.1.1 Microstructure of BST thin films

Noh et al. studied the crystallization temperature of BST thin films by synchrotron radiation method [40]. An amorphous film of BST was sputtered on MgO substrate and heated to study the crystallization behavior. At \( T \approx 500 - 600 \) °C, a metastable intermediate phase was observed while full crystallization took place close to \( T = 700 \) °C.

The two main orientation of BST thin films are the (100) and (110). According to York et al. [41] the (100) orientation is more preferable as it leads to smoother films [35] and optimum dielectric properties. Two processing parameters have the greatest influence on the orientation of BST thin films. They are the deposition temperature and the substrate. Lee et al. [42] found that the (110) component decreased as the deposition temperature was increased. BST thin films were sputtered on Pt/SiO\(_2\)/Si substrate at temperatures of 500 - 650 °C. It was found that (110) orientation was the majority component while (100) formed the minority component at the lower end of the deposition
temperature and the films had poor crystalline quality. At deposition temperature of 650 °C the films had good crystalline quality and it had a majority of (100) component.

Generally crystallization in perovskite thin films can be induced by \textit{in–situ} or \textit{ex–situ} heat treatment. In the case of \textit{in–situ} crystallization the substrate temperature is kept relatively high (T > 550 °C). \textit{Ex–situ} crystallization is carried out by conventional annealing methods or RTA (rapid thermal annealing) technique to induce crystallization in amorphous perovskite thin films deposited at lower deposition temperatures [43].

\textbf{1.3.2 BST device technology}

Most ferroelectric thin film capacitors are based on two basic types of geometries. One is the parallel plate or the MIM (metal insulator metal) structure in which the ferroelectric thin films is sandwiched between two metallic layers and the other is the IDE (interdigitated electrode) structure in which the ferroelectric layer is directly deposited on the substrate and the metal lines form interdigitated structure on the thin film surface. These two different geometries are shown in Fig.1.3.2.1.

![Fig.1.3.2.1: Two different configurations of thin film capacitors; MIM and IDC.](image-url)
In general, interdigital devices are simpler to fabricate and integrate into circuits since it requires only single step metallization compared to the MIM configuration where three steps are required (patterning the bottom electrodes, the dielectric and the top electrode). IDEs require higher tuning voltages than the MIMs since a large part of the field passes through air and not the dielectric as in the latter case. For parallel plate capacitors, BST films are deposited directly on the bottom electrode on the substrate. The distance between the electrodes is basically the BST film thickness (usually < 1 µm) and therefore much shorter than the finger spacing (3 - 20 µm) in the interdigital structures. Since tuning is a function of the applied electric field, the control voltages in the case of MIMs are much less than that of IDCs. Typical operating voltages for interdigital capacitors are in the range of 100 V’s while MIMs typically require < 30 V. Smaller spacing between the fingers help in decreasing the control voltages required for tuning in the case for IDEs. However the ability to fabricate small finger spacing depends on the type of substrate and the photolithographic resources available. Another advantage of IDEs is that the ferroelectric thin film can be directly deposited on the substrate and therefore can be annealed at higher temperatures to improve the crystallinity of the ferroelectric thin film. In the case of MIMs the difference in the CTE of the film and the bottom metal electrode may impose limitation on the annealing temperature limits. Thus there exist tradeoffs between the IDE and the MIM structure which are summarized in table 1.3.2.1.
Table 1.3.2.1: Tradeoffs between IDE and MIM configuration

<table>
<thead>
<tr>
<th>IDE</th>
<th>MIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polarization in horizontal direction</td>
<td>Polarization in vertical direction</td>
</tr>
<tr>
<td>Single step photolithography</td>
<td>Complex photolithography (3 step process)</td>
</tr>
<tr>
<td>High operating voltages (50 – 150 V)</td>
<td>Low operating voltages (5 - 30 V)</td>
</tr>
<tr>
<td>Low capacitance values (0.1 – 10 pF)</td>
<td>High capacitance values (5 – 200 pF)</td>
</tr>
</tbody>
</table>

Another advantage of using IDCs is that it is possible to have very small value capacitors \((C = 0.1 - 10 \text{ pF})\) even when using modest sized IDEs. This is very advantageous when designing and fabricating MW devices, where the impedance of the circuit is fixed at 50 \(\Omega\) [44]. For a MW circuit the impedance is given as follows:

\[
\chi_c = 50 \Omega = \frac{1}{(\omega C)} = \frac{1}{(2 \pi f C)}
\]

where \(\chi_c\) is the AC impedance of the circuit, \(\omega\) is the angular frequency, \(f\) is the frequency of operation and \(C\) is the capacitance value. Using the above equation we have for \(f = 1 \text{ GHz}\), \(C = 3.2 \text{ pF}\) and for \(f = 10 \text{ GHz}\), \(C = 0.32 \text{ pF}\). As it is obvious from the above equation the value of \(C\) gets progressively smaller as the value of \(f\) (frequency of operation) increase since \(C\) and \(f\) are inversely related. Higher or lower capacitance values will cause signal reflections because of impedance mismatch and lead to higher losses in the MW device. Such small values of capacitance are easy to get in the IDE configuration since a substantial part of the field applied in this case passes through the air (low permittivity value) rather than the ferroelectric film (high permittivity value).
itself. Such low values of capacitance are however difficult to achieve in the MIM configuration as explained in the following section.

For MIM configuration the capacitance value is given by:

\[ C = \varepsilon_o \varepsilon_r (A / t) \]

where \( C \) is the value of capacitance, \( \varepsilon_o \) is the permittivity, \( \varepsilon_r \) is the dielectric constant, \( A \) is the area of the electrodes and \( t \) is the thickness of the dielectric. For a \( C \) value of 1 pF, dielectric constant of 500 and a film thickness of 0.5 \( \mu \)m the area comes out to be 113 \( \mu \)m\(^2\). Thus for an MIM capacitor we need to have 10.6 \( \mu \)m x 10.6 \( \mu \)m (for \( A \sim 113 \ \mu \)m\(^2\)) lines to be integrated with cm sized lines with multiple micron thickness required for microstrip or coplanar circuits. Because of the high dielectric constant of the BST films, the small value of capacitance required in MW circuits can only be achieved by having small contact areas typically in the \( \mu \)m\(^2\) range, requiring tight lithographic tolerances. Thus integrating MIM capacitors is challenging in MW circuits from a fabrication point of view. IDCs on the other hand are of modest sizes and hence integration in MW devices is much easier.
1.4 Substrates for microwave devices

The important parameters that influence the design of a MW device are the frequency of operation, substrate, thin film, top electrode, and gain and voltage requirements. In this chapter the requirements of substrates used in microwave circuit are discussed.

The history of laminates and substrates for use in MW devices dates back to the 1950s [45]. Initially low dielectric constant plastics were used but these had problems due to radiation effects and intercircuit coupling. Later PTFE / glass cloth laminates (dielectric constant, $\varepsilon = 2.7$) became popular and overcame many problems that its predecessor had. By decreasing the glass concentration in this laminate the dielectric constant was further reduced to 2.45 and this became the first industry standard laminate. In the 1960’s MW circuits were usually fabricated on woven Teflon fiberglass material known as 3M K6098 [46]. It had a dielectric constant of 2.55, and had 1 oz Cu on both sides. Other laminates such as PTFE / glass microfiber and PPO (polyphenylene oxide) were also widely used during that era [46, 47].

During the mid and late 60s high purity (99.5%) alumina substrates were introduced in MW circuits. It had two attractive properties: - high dielectric constant ($\varepsilon \sim 10$) and smooth surface finish. Alumina substrates with higher purity (99.6 % and 99.7 %) and smaller particle size were introduced in the MW device market in the 1970s. Today the most widely used alumina substrates have a purity of 99.7% and 99.8 %.

Today the microwave designer has many materials to choose from depending upon the end application. Here it is important to distinguish between two terms that are used for the same purpose in the MW circuit world. These are “laminates” and
“substrates”. Usually laminates refer to ‘soft’ material such as Teflon (PTFE) which may contain fiberglass or ceramic reinforcement for mechanical integrity. On the other hand, ceramic materials are known as “hard” substrates and are usually $\text{Al}_2\text{O}_3$ (polycrystalline alumina or single crystalline sapphire), MgO (Magnesium oxide), and LaAlO$_3$ (Lanthanum aluminate).

The important parameters for the substrate used in MW devices are the dielectric constant, loss tangent, CTE (coefficient of thermal expansion), size, cost, and availability [45].

The dielectric constant is the ratio of stored charge in the material to the stored charge in air. The wavelength or the velocity of the microwave signal changes when it travels through the substrate. This is given by the following formula:

$$\lambda = \frac{c}{(f \sqrt{\varepsilon})}$$

where $\lambda$ is the wavelength, $c$ is the velocity of light in vacuum, $f$ is the frequency of operation, and $\varepsilon$ is the permittivity of the material.

Another important factor is the dissipation loss. Dissipation loss ($\tan \delta$) is the ratio of the energy dissipated to the energy stored in the material. From a device metrics point of view the dissipation loss in the substrate should be as low as possible to minimize the total loss in the MW device.

CTE (Coefficient of thermal expansion) of a material is the parameter that defines how much the material changes its dimensions when it is heated or cooled. It is expressed in parts per million per degree change in temperature. The CTE of the MW substrate should be as close to the CTE of the film deposited on the substrate as possible since a large difference will lead to compressive or tensile strains at the film / substrate interface.
and will lead to film cracking. Hence from a design point of view CTE of the MW substrate is an important factor while fabricating a MW device.

Another important factor that should be considered from the substrate point of view is the flatness or the surface roughness of the substrate. Flat surfaces are required to ensure proper operation of vacuum fixture during exposure and good contact with the mask during UV light exposure in photolithography. The surface finish on the substrate decides the limits of the photolithographic process for fabrication of the MW device.

1.4.1 Polycrystalline ceramic alumina substrate

To date, most ferroelectric thin film microwave devices have been fabricated on single crystal substrates such as MgO [48, 49], LaAlO$_3$ [48, 49], and Al$_2$O$_3$ (sapphire) [16, 50]. This approach has been adopted because these substrates offer very low loss tangent values, and conventional processing teaches that epitaxial BST thin films, which can be grown on such single crystal substrates at high temperature ( $T \geq 650 ^\circ C$ ) offer optimal ferroelectric properties. Conventional thinking teaches us that ideal performance of functional materials is best achieved by minimizing crystallographic imperfections such as grain boundaries and defects, and chemical imperfections such as variations in the stoichiometry. To this end, most MW design engineers use single crystal substrates as the starting templates for deposition of ferroelectric thin films by various means such as RF sputtering [16, 41, 51], MOCVD( metal organic chemical vapor deposition) [52 - 54], and PLD( pulsed vapor deposition) [55 - 57].

These single crystal substrates however, are expensive, and many are available only in small dimensions. If the technology of tunable ferroelectric microwave devices is
to be realized, materials solutions allowing the optimal properties in economical or manufacturable embodiments must be developed. In this investigation we have chosen polycrystalline Alumina ($\text{Al}_2\text{O}_3$) substrates. These are comparatively low cost and available in dimensions suitable for large area film deposition; for instance 6” polished alumina wafers which are compatible with tooling for 150 mm Si wafers. Alumina is also attractive for its excellent microwave properties, when prepared with high purity, polycrystalline alumina exhibits a loss tangent of $10^{-4}$ in microwave frequencies. Furthermore, the thermal expansion coefficient of alumina ($\text{CTE} \sim 9 \text{ ppm @} \text{RT}$) is similar to BST, thus annealing to temperatures above 700 °C is possible without cracking the deposited thin film [58].

Table 1.4.1.1 summarizes the physical properties of the alumina substrate (Intertec Southwest Inc., Tucson, AZ) used in this work.

<table>
<thead>
<tr>
<th>Material</th>
<th>$\text{Al}_2\text{O}_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant ($\varepsilon$)</td>
<td>10.0</td>
</tr>
<tr>
<td>Dissipation factor (tan $\delta$) @1 MHz</td>
<td>0.0001</td>
</tr>
<tr>
<td>Surface finish</td>
<td>&lt; 50 nm rms (1x 1 µm scan)</td>
</tr>
<tr>
<td>Thickness</td>
<td>625 µm</td>
</tr>
<tr>
<td>CTE</td>
<td>9 ppm</td>
</tr>
<tr>
<td>Purity</td>
<td>&gt; 99.6 %</td>
</tr>
<tr>
<td>Price</td>
<td>$25$ for a 4.5 ” x 4.5 ” x 625 µm wafer</td>
</tr>
</tbody>
</table>
1.5 Electrodes for Microwave devices

When designing or fabricating MW devices using ferroelectric thin films attention is most often directed to the properties and preparation of the dielectric. Metallization used in MW devices is equally important and is the more dominant mechanism for loss, especially at MW frequencies. Devices cannot tolerate high levels of dc resistance while still maintaining low insertion loss and hence metals used for electrodes in MW devices should be carefully chosen.

The properties of the metal electrodes used in MW devices that are of primary importance are the conductivity of the metal, ease of patterning, cost and availability. Good electrical conductivity is important since the metal, used either as top electrode or as a ground plane, must carry high frequency currents with as little loss as possible. Table 1.5.1 below summarizes the resistivity values of different metals of technological interest.

Table 1.5.1: Resistivity data sheet for different metals

<table>
<thead>
<tr>
<th>Noble Metal</th>
<th>Resistivity( μΩ-cm)</th>
<th>Base metal</th>
<th>Resistivity( μΩ-cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ag</td>
<td>1.6</td>
<td>Cu</td>
<td>1.7</td>
</tr>
<tr>
<td>Au</td>
<td>2.2</td>
<td>Al</td>
<td>2.7</td>
</tr>
<tr>
<td>Ir</td>
<td>5.1</td>
<td>W</td>
<td>5.4</td>
</tr>
<tr>
<td>Ru</td>
<td>7.7</td>
<td>Mo</td>
<td>5.7</td>
</tr>
<tr>
<td>Pt</td>
<td>10.6</td>
<td>Ta</td>
<td>13.5</td>
</tr>
<tr>
<td>Pd</td>
<td>10.8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
In most practical cases the loss or attenuation in metals is calculated by assuming that the metal is a good conductor as opposed to perfect conductor. A good conductor is a special case in which the conductive current \( J = \sigma E \) is assumed to be much higher than the displacement current \( J = j \omega \varepsilon E \) so that \( \sigma \gg \omega \varepsilon \). Most metals can be assumed to be good conductors for practical purposes [44]. Skin depth is a measure of how far electrical conduction takes place in a conductor, and is a function of frequency. At DC (i.e. 0 Hz) the entire conductor is used regardless of its thickness. As the cross-sectional area of a wire is doubled, the DC resistance per unit length decreases by half, as expected from Ohm's law. At RF frequencies, the effect that conductor thickness has on its conductance is non-linear (actually, a negative exponential!) There is a limitation on the conductance that can be achieved, and increasing the thickness of the metal electrode indiscriminately in MW devices to reduce RF losses will not reduce the RF resistivity.

The well-known equation for skin depth or characteristic depth of penetration is given below. Note that skin depth \( \delta_s \) is a function of only three variables, frequency \( (f) \), resistivity \( (\rho) \), and relative permeability \( (\mu_r) \).

\[
\delta = \sqrt{\frac{2}{\omega \mu \sigma}}
\]

where \( \omega \) is the angular frequency \( (\omega = 2\pi f) \), \( \sigma \) is the electrical conductivity, and \( \mu \) is the permeability of the metal. The current density \( J \) in an infinitely thick plane conductor decreases exponentially with depth \( (d) \) from the surface, as follows:

\[
J = J_0 e^{\left(-\frac{d}{\delta_s}\right)}
\]

where \( \delta_s \) is the skin depth and \( J_0 \) is the current density at the surface. Thus at a depth of \( d = \delta_s \) the current is \( 1/e \) (about 0.37) times the current at the surface. Thus skin depth can
also be defined as the depth in which the current density decreases to \((1/e)\) times that of the surface current. When \(d = 3\delta_s\) (i.e. thickness of metal is 3 times the skin depth at a particular frequency) the current is \((1/e^3)\) (about 0.05) times the current at the surface. Thus for one skin depth the current density is 37 % of that of surface current density while this value decreases to only 5 % for three skin depths. In other words 95 % of current flows through the top three skin depths of the metal.

From a device metrics point of view what this means is that since the skin depth is extremely small for good conductors at microwave frequencies, only thin metal plating is necessary for low loss microwave components. A list of skin depths for some metals at 10 GHz is given in table 1.5.2.

Table 1.5.2: Data sheet showing skin depths of metals at 10 GHz.

<table>
<thead>
<tr>
<th>Metal</th>
<th>Skin depth (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ag</td>
<td>0.640</td>
</tr>
<tr>
<td>Cu</td>
<td>\textbf{0.660}</td>
</tr>
<tr>
<td>Au</td>
<td>0.786</td>
</tr>
<tr>
<td>Al</td>
<td>0.814</td>
</tr>
<tr>
<td>W</td>
<td>1.176</td>
</tr>
<tr>
<td>Pt</td>
<td>1.648</td>
</tr>
</tbody>
</table>
Thus by judiciously choosing the metal and calculating the skin depth at different frequencies we can have MW devices with low insertion loss. For ex., at 10 GHz, 3 skin depths of Cu, i.e. 1.98 µm is electrically equivalent to 4.95 µm of Pt. Not only is Cu (base metal) much cheaper than Pt (noble metal) but patterning 1.98 µm of any metal is much easier than patterning 4.95 µm of metal from a microfabrication point of view.

1.5.1 Copper technology and device integration issues

BST-based and other thin film perovskite based devices usually incorporate noble metallization like Pt, Au, or Ir [16, 19, 52, 59, 60] because they are in most instances non-reactive in contact with oxides and their large work functions provide blocking, or Schottky contacts. Though these properties are attractive, the expense associated with these choices and the difficulty in patterning provides limitations, especially for volume application. Furthermore, the high resistance values of Pt and Au necessitate multiple micron layer thicknesses for suitably low sheet resistances: this only exacerbates the patterning issues. To overcome these difficulties we have investigated copper metallization in this work. Though Cu has recently been introduced in the semiconductor integrated chip (IC) industry for interconnect lines, limited work has been reported using it as an electrode material for thin film oxide based devices. This is due to its inherently poor adhesion and its tendency to oxidize and react in ambient atmosphere [61]. Some recent reports, however, have shown that provided the proper synthesis conditions, copper can be used as a reliable electrode with BST. Cu was chosen as the top electrode metal in the current study since it provides the highest conductivity of any base metal, it is inexpensive, and it can be easily etched using wet chemical means.
1.6 BST device characterization

In order to integrate BST thin films in RF and MW devices a detailed characterization of the frequency and the field dependency of both the dielectric permittivity (tunability) and the dielectric loss tangent ($\tan\delta$) of BST is required. Also at MW frequencies loss due to metallization dominates and hence finding the Q (quality) factor at GHz frequencies is not as straightforward as for low frequencies since metallization effects have to be considered. Thus accurate characterization of BST thin films at MW frequencies require detailed modeling and special characterization techniques.

In this section, measurements, modeling and characterization of the BST capacitors will be described.

Measurement methods for ferroelectric materials can be broadly divided into three groups [34, 44):

(a) Direct methods: Here the capacitance and the loss tangent of the capacitor of the ferroelectric material are measured using an impedance analyzer or by evaluating the scattering matrix (S parameters) [62] obtained from a network analyzer.

(b) Waveguide methods: Here the S parameters of the ferroelectric containing waveguide are measured using a network analyzer.

(c) Resonance methods: In this particular method the characteristics of the resonator which contains the ferroelectric material are measured.

For circuits containing ferroelectric material, the measurement method and the type of measurement set up depends on the frequency range of operation and the sample geometry (thin film, bulk or thick film). For circuits operating in the frequency range 10-
30 GHz the circuit dimensions are small compared to the electromagnetic signal or wavelength and the tunable capacitor can be regarded as a lumped element [34, 44]. The lumped element model of a circuit assumes that each element is an infinitesimal point in space. The capacitance and the loss tangent associated with this capacitor can be measured directly by an impedance analyzer. At higher frequencies (f > 30 GHz) measurements substantially more complicated since the dimensions of the capacitors become comparable to the electromagnetic signal and hence the capacitors can no longer be considered as lumped elements. Also, the impedance of the capacitors become quite small compared to the resolution of the impedance analyzer.

The dielectric permittivity of a MIM or parallel plate capacitor is given by the following formula:-

\[
\varepsilon_r = \frac{C \cdot t}{\varepsilon_0 A}
\]

where \( \varepsilon_r \) is the relative dielectric permittivity, \( C \) is the capacitance, \( t \) is the thickness of the ferroelectric thin film and \( A \) is the area of the electrodes. For the planar or the interdigitated capacitor the formula is not straightforward and because of its geometry the electric field is distributed between the ferroelectric thin film, air and the substrate. Two formulas are used for these types of capacitors and they are based on conformal mapping techniques. They are due to Farnell [63] and Gevorgian [64]. Both of these formulae using a conformal mapping technique to compute the capacitance value of the IDE structure. Farnell’s formula is based on a simple analytical model which takes into consideration a two layered substrate (e.g., a dielectric film on a substrate), film thickness, IDE finger length, the no. of fingers, and the capacitance value of the IDC [63]. On the other hand, Gevorgian’s model is more rigorous and uses CAD – oriented
models for a large variety of IDCs on a three-layered substrate and is valid up to frequencies in the X-band (8-12 GHz). The derivation is based on partial capacitance method and considers the capacitance between the IDE fingers and the fringing capacitance of the finger ends [64]. However, detailed discussions of these models are beyond the scope of this thesis.

For both kinds of capacitors, measurements to several MHz can be done using an impedance analyzer where both the values of the capacitance and the loss tangent are obtained directly. For higher frequencies, a network analyzer is used to measure the S parameters and then the capacitance and the loss tangent values are extracted from the measured data using a suitable modeling technique.
1.7 BST thin film fabrication

The technological applications of oxide thin films are varied and diverse. These extend from MEMS applications such as piezo microactuators, micromotors and micropump actuation; force, vibration, and chemical sensors as well as biosensors; very small scale micro-reaction vessels for chemical and biological (lab on a chip) sensing; ferroelectric memories; information storage; electro-optical devices for military and civil thermal imaging based on the pyroelectric effect, ferroelectric thin film decoupling capacitors for integration with Si-CMOS chips; microwave devices for high frequency telecommunications utilizing the high dielectric constant of ferroelectric materials and many more [27, 32]. These applications utilize a wide range of oxide thin film properties that include dielectric, ferroelectric, piezoelectric, electrostrictive, pyroelectric, optical, electro-optic, and magnetic responses, as well as electronic conduction, ionic conduction, and superconductivity in some cases. As an illustration, the various applications of BST thin films utilizing the properties mentioned above are shown in Fig 1.7.1. These ceramics represent an important world market, which has been experiencing steady growth in recent years [43].

Over the last few decades many processes have been developed for growth of oxide thin films [34, 43]. A wide variety of techniques have been used for the deposition of electroceramic thin films, and these can be divided into three general categories:

(a) Physical vapor deposition: radio-frequency and magnetron sputtering, ion beam sputtering, molecular beam epitaxy (MBE), and pulsed laser deposition (PLD)

(b) Chemical solution deposition: sol–gel and metal-organic decomposition
For any growth process to be incorporated into a viable manufacturing process certain requirements must be met. These are listed as below:

(a) The process should be compatible for large volume manufacturing and scalable to large areas

(b) The ability to produce high quality films with reproducible properties at the lowest processing temperature possible.

(c) The ability to control microstructure and stoichiometry.

(d) The ability to produce films with uniform thickness and conformality.

(e) The growth process should be low cost from a manufacturing point of view.

In this section the various growth processes relevant to BST thin film processing are discussed. However this discussion is, for the most part, limited to fabrication of BST
thin films directly on a substrate (IDC type configuration) with top metal electrodes rather than BST thin films on a metallized substrate (MIM configuration) with top and bottom electrodes.

1.7.1 Deposition technologies for BST thin films

1.7.1.1 Chemical solution deposition (CSD)

Chemical solution deposition (CSD) or wet chemical synthesis method offer many advantages for preparing ferroelectric thin films such as low cost of operation and a comparatively simple fabrication infrastructure (i.e., no vacuum). In this processing route it is straightforward to introduce the right dopant concentration in the film for tailoring its property according to the end application. Consequently many research groups have actively pursued the preparation of ferroelectric thin films by chemical solution deposition [65-70].

The basic principle involved in the solution deposition of perovskite films is to prepare a homogeneous solution that contains the necessary cation species that may later be applied to a substrate. The four basic steps involved in the fabrication of thin films by this process are as follows:

(a) Preparation of the precursor solution containing the right cations

(b) Deposition of the solution on the substrate by spin-coating (this step might be repeated several times depending on the thickness of the film used)

(c) Low-temperature heat treatment for drying, and thermolysis of organic species (T ~ 300 °C - 400 °C), and formation of an amorphous film

(d) Higher temperature heat treatment (T ~ 600 °C - 1100 °C) for densification and crystallization of the film into the desired metal oxide phase
Depending upon the solution used in processing, different types of deposition and thermal processing conditions are used to control film densification and crystallization for the preparation of the ferroelectric thin film.

Solution preparation of perovskite thin films usually involves the use of metalorganic compounds that are dissolved in a common solvent. Metal alkoxide compounds, $M(OR)_x$, where $M$ is a metal and $R$ is an alkyl group, metal carboxylates, $M(OOCR)_x$, and metal $\beta$-diketonates, $MO_x(CH_3-COCHCOCH_3)_x$ are usually the starting reagents. This selection is dictated by solubility and reactivity considerations and the type of solution precursor species desired. The chemical properties of the sol gel precursor solutions can be changed by modifying the organic ligands attached to the metal cations or using different stabilizer and solvent chemistry to form complex precursor solutions. Due to the difference in the nature of the precursor solution the gelation behavior is also different which ultimately affects the metal oxide thin film properties after subsequent heat treatment [71, 72].

Most investigations studying the influence of the precursor solution on the dielectric properties of the film has been carried out on PZT (Lead zirconate titanate) thin films. The nature of the precursor solution affects the density, texture, and crystallization behavior of the film as well as it’s dielectric and optical properties [71]. Schwartz et al. [71, 72] have shown most completely the influence of precursor chemistry on the crystallization behavior, texture and surface morphology of the deposited PZT films.

The development of chemical solution deposition (CSD) processes for perovskite thin films dates to the mid-1980s when Fukushima and co-workers [65] prepared PZT thin films by MOD (metalorganic decomposition) while Budd et al. [66,67] used sol-gel
processing. These were the first demonstrations of preparation of perovskite thin films by wet chemical methods. Later the sol-gel technique has been applied to the preparation of various types of ferroelectric thin films which include metal titanate and zirconate thin films such as PbTiO$_3$, BaTiO$_3$, BaSrTiO$_3$, PbZrO$_3$, Pb(Zr,Ti)O$_3$ (PZT), PbLaZrTiO$_3$ (PLZT), metal niobate films such as LiNbO$_3$, SrBaNbO$_3$ (SBN), PbBaNbO$_3$ (PBN) and some ferroelectric relaxors such as Pb(Mg$_{1/3}$Nb$_{2/3}$)O$_3$ (PMN), Pb(Mg$_{1/3}$Nb$_{2/3}$)O$_3$.PbTiO$_3$ (PMNT), PbFe$_{0.5}$Nb$_{0.5}$O$_3$ (PFN) and PbZrTiNbO$_3$ (PZTN) [32, 43, 71, 73].

Compared to research reports on sol gel processing of PZT or Pb based ferroelectric thin films there are a substantially smaller set of reports on CSD process for preparation of BST thin films. A slightly modified version of CSD processing of BST thin films was reported by Soyama et al. [74]. The authors reported fine patterned (10 $\mu$m) BST thin films synthesized on a metallized Si substrate from a photosensitive sol gel using UV radiation. The precursors were Barium Acetate, Strontium Acetate and Titanium Isopropoxide and the solvent was Acetic acid. This solution was spin coated on a Pt / Ti / SiO$_2$ / Si substrate and heat treated at 150 °C for 5 - 10 min and then exposed to UV radiation ($\lambda$ = 254 nm) through a mask. The film was developed in dilute ethanol to obtain a negative image of BST thin film. Subsequently the film was heated at 650 °C for 10 min (this step was repeated multiple times to get the desired film thickness) and then crystallization anneal was done at 750 °C for 1 hr. Dielectric measurements revealed a permittivity of 224 and dielectric loss tangent of 0.04 which is comparable to values obtained by conventional sol gel processing.

A group at the University of Puerto Rico [75] has reported the feasibility of using CSD process for making BST thin films on LAO for tunable microwave device
applications. Sol gel BST thin films were fabricated on single crystalline LAO using Barium acetate, Strontium acetate, and Titanium iso propoxide as the precursors. Ethylene glycol was added to completely dissolve the precursors. For thin film deposition the solution was diluted by adding acetic acid and then spin coated on the substrate followed by crystallization anneal in air at 1050 °C for 2 hours. The phase shifter structure was made on the BST films using a photolithographic lift off process using Au / Ti metallization. The phase shifter showed a phase shift of 266 ° at 400 V (53 V/ µm) and an insertion loss of 6.5 dB at 0 V and 4.8 dB at high bias. Thus the figure of merit (defined as the phase shift per unit insertion loss at 0 V) is 40.9 ° / dB at a frequency of 14.2 GHz. This performance is comparable to the BST thin film phase shifter of the same design using PLD process which had a figure of merit of 49 ° / dB at the same frequency.

Recently a group at Los Alamos National Lab has demonstrated the feasibility of processing BST thin films by polymer assisted deposition (PAD) [76, 77]. In PAD technique aqueous solutions of metal precursors are combined with a water-soluble polymer. The desired viscosity of the process is controlled by the polymer and it also coordinates with the metal ions to prevent formation of metal – oxide oligomers which lead to premature precipitation. Thus a homogeneous and uniform distribution of metal precursors is created in the solution that leads to the formation of uniform metalorganic films upon thermal decomposition. In PAD process stable metal complexes are used as the source of metal ions and therefore stoichiometric compounds are easy to make here than in sol gel processing.

Y.Lin et al. have demonstrated epitaxial BST thin films on LAO substrates using PAD process [76, 77]. The precursor solution consists of three different aqueous
solutions of Ba, Sr and Ti bound to polymers. Ti was bound to PEIC (carboxylated – polyethylenimine) while Ba and Sr was bound as EDTA (ethylenediaminetetraacetic acid) complex to PEI (polymer polyethylenimine). The solutions were mixed according to the desired final stoichiometry of BST and then spin coated on LAO substrates. Thermal treatment was done in oxygen and then polymer pyrolysis was done at 500 °C. Subsequently crystallization anneal was done at 1000 °C for 1 hour. Structural characterization was done using XRD and TEM and revealed epitaxial BST structure on LAO. Dielectric properties were tested using CPW (coplanar waveguide) lines and the tunability and the permittivity values obtained were comparable to BST thin films grown on LAO by PLD [78]. The successful growth of metal-oxide thin films by PAD suggests that PAD is a promising alternative approach to the growth of high-quality epitaxial metal-oxide thin films. However the dielectric properties of such films are not necessarily better than those deposited by other physical and / or chemical vapor deposition.

CSD techniques have been used so far to develop high quality ferroelectric thin films for various applications. This technology is simple and rapid, needs little capital investment and allows good control over stoichiometry. MW device quality BST thin films have been demonstrated using this CSD technique.

1.7.1.2 Pulsed Laser Deposition (PLD)

Pulsed Laser Deposition (PLD) technique has been used to grow high-quality films of various ferroelectric oxide materials [79-82] for many years. In the PLD method a pulsed laser beam is focused onto the surface of the target at an oblique angle such that the substrate can sit directly in front of the target surface. A highly intense UV laser beam
is focused on a spot on the target where the high energy density during the laser pulse (about 1 GW within 25 ns) ablates almost any material. The interaction of the pulsed laser beam with the target produces a plume of material that is transported towards the heated substrate placed directly in the line of the plume. This method is quite flexible in preparing films under a wide range of deposition conditions.

Most PLD systems consists of (a) an excimer laser beam source, usually a KrF ($\lambda = 248$ nm) laser beam, $P = 1-5$ J/cm$^2$ ($f \sim 1-5$ Hz) is used (b) a rotating target holder with capacity to sequentially position various targets under the laser beam in order to fabricate multilayered heterostructures in situ; and (c) a substrate holder which can be heated to high temperature of $T \sim 750$ °C. More details of PLD systems and the physics behind the ablation and related deposition processes can be found in a recent review [83].

Pulsed Laser Deposition is appropriate for the fabrication of complex oxide materials, since it has the following advantages:

(a) It can be used to deposit both pure elements and multicomponent compounds.

(b) The rate of deposition is relatively high compared with other physical deposition methods.

(c) Deposition temperatures are relatively low due to high-energy plume.

(d) Deposition optimization can be very rapid

Srivastava et al. [57] have reported improvements in electrical and dielectric properties of BST thin films (doped with Ag) prepared by PLD. Doped (5 wt %) and undoped BST thin films were prepared by PLD using a LPX 300 KrF excimer laser with 5 Hz pulse frequency. The authors report that doped BST thin film capacitors (Ag / BST / LaNiO$_3$ / LAO) show a leakage current that is an order of magnitude less than ($J = 40$ nA/
cm² for doped films compared to J = 500 nA/ cm² for undoped films at 100 kV/cm²) the undoped one. This improvement in the electrical properties of the BST thin films was attributed to the enhancement in oxygenation and unpinning of domain wall characteristics in the presence of Ag. However the authors do not mention about the tunability or the dielectric loss of the thin films in this case.

Heteroepitaxial Ba₀.₆Sr₀.₄TiO₃ films were deposited on LAO and MgO substrates using PLD [7]. IDE (Au / Ag / BST / LAO or MgO) structures were fabricated and microwave measurements were done in the range of 1-20 GHz [48]. The authors report a tunability of 65% for an applied field of 7 V/µm and a Q (quality factor) of 4 at 20 GHz. In this paper the strain effects on tunability is investigated by XRD. The authors conclude that the magnitude of the strain rather than the type of strain (tensile or compressive) affects the tunability which varies inversely with strain.

D.M.Bubb [55] et al. deposited BST thin films on MgO substrates using PLD process using a pO₂ of 50 m Torr using a substrate temperature of 730 °C. The laser fluence at 248nm was 1.9 J/m². The target had a composition of Ba₀.₆Sr₀.₄TiO₃ : 1 %WO₃. The authors demonstrate that it is possible to fabricate low loss films (Q ~ 600 @ 6 GHz) for microwave applications. However the tunability reported is rather low (n = 12 %) for tunable MW applications.

Thus there are numerous reports of fabrication of BST thin films by PLD. Studies have demonstrated that the background gas pressure during deposition, substrate to target distance, laser energy and wavelength, and target-substrate relative geometric arrangement have a significant effect on oxide film composition, microstructure and properties. It has been demonstrated that BST thin films made by PLD have good
electrical and dielectric properties and hence can be used for MW applications. However there are problems associated with PLD process. Issues such as formation of droplets or particulates [84], deposition on large area substrates [32], and problems with volume manufacturing are yet to be addressed. Also, the limited degree of conformal deposition is envisioned as problematic.

1.7.1.3 Metal organic chemical vapor deposition (MOCVD)

Metalorganic Chemical Vapor Deposition (MOCVD) is a technique for synthesis of thin films based on chemical reaction of special chemicals called metalorganic precursors in a vapor phase. The metalorganic precursors are transported into the reactor chamber using hydrogen carrier gas. High temperature in the chamber decomposes the precursors and the liberated atoms recombine forming a compound. This takes place on substrates placed on a radiatively heated susceptor resulting in film growth [85-88].

In MOCVD process, for ferroelectric thin films the precursors are usually vapor-phase mixtures of metal alkoxides or diketonates. The essential elements of an MOCVD process consists of precursor chemistry, the delivery method for introducing the chemistry into the CVD chamber and the deposition process [86].

MOCVD is a versatile and promising deposition technique, offering the potential for large area growth, and having the advantages of good composition control, high film uniformity, good control over doping and excellent conformal step coverage on non-planar substrate geometries[85, 86]. However, an essential requirement of the MOCVD process is the availability of suitable precursors which should ideally possess a number of properties as given below:
(a) Optimum volatility to achieve acceptable oxide growth rates at moderate evaporation temperatures.
(b) Clean decomposition without the incorporation of residual impurities.
(c) Wide temperature window between evaporation and thermal decomposition.
(d) Long and stable shelf-life for liquid injection MOCVD method.
(e) Good compatibility with other co-precursors during the growth of complex oxides.
(f) Easily manufactured in high yield at low cost.
(g) Low hazard chemicals with minimal toxicity.

T. Kawahara et al. [86] prepared thin films of BST on Pt/SiO$_2$/Si substrates by liquid source CVD method using precursors such as Ba(DPM)$_2$, Sr(DPM)$_2$ and TiO(DPM)$_2$ (DPM = dipivaloylmethanato; C$_{11}$H$_{19}$O$_2$) dissolved in THF. By optimizing the deposition procedures a reproducibility of (+/-) 3% for the film composition was achieved using this process. Step coverage of 72%, obtained at substrate temperature of 753 K using the above mentioned precursors was better than those obtained using other Ti sources such as Ti(O-i-Pr)$_4$ (TTIP) and Ti(O-i-Pr)$_2$(DPM)$_2$. The electrical properties of the 48 nm thick BST film, deposited at T$_s$ = 753 K using TiO(DPM)$_2$, were as follows; dielectric constant (ε) = 230, leakage current = 6.7 x10$^{-6}$ A/cm$^2$ at 1.65 V, and dielectric loss tangent of 0.013.

J.F. Roeder et al. [89] at ATMI, CT, have reported BST thin films produced by liquid delivery method using solutions of (a) (pmdeta)Ba(thd)$_2$, (pmdeta)Sr(thd)$_2$ and Ti(OiPr)$_2$(thd)$_2$ where pmdeta is N, N, N’,N’’-pentamethyldiethylene triamine and (b) (teg) Ba(thd)$_2$, (teg)Sr(thd)$_2$ and Ti(OiPr)$_2$(thd)$_2$ where teg is tetraglyme. The authors
found that high quality BST ferroelectric thin films can be deposited by MOCVD using both types of precursors. The BST thin films fabricated had similar electrical properties (films had permittivity value of 240, leakage current of $1.0 \times 10^{-9}$ A/cm$^2$ at 1 V, and low dielectric loss of 0.003).

The Electroceramic Thin Film group at NCSU has fabricated IDEs (Cu/ Cr/ BST/ Alumina) using BST films fabricated by ATMI using MOCVD technique. Details of the processing method are discussed elsewhere [90]. The IDEs were tested for tunability and quality factor at MW frequencies. Tunability values of 40% at 300 KV/cm, low frequency dielectric Q (quality factor) $\sim$ 100 and a device Q of 17 at 26 GHz was obtained [90].

MOCVD is a flexible technique, which allows the controlled growth of highly conformal films on planar and high-aspect ratio substrates. It is also a scalable process and large area substrates can be used for volume manufacturing at high deposition rates. Limitations of this process are the lack of suitable precursors for film growth, complex process parameter field and little in-situ control of the film growth process. Despite these advantages there have been relatively few studies on the MOCVD of BST thin films, especially BST thin films directly on ceramic substrates for IDE type configuration for application in MW devices.
1.7.2 RF Sputtering

Sputtering is a widely used processing technique for fabrication of metal and ceramic thin films [91-93]. An effect of glow discharge process is sputtering in which a surface is physically bombarded by energetic ions and the target atoms are physically ejected. The sputtered ions travel through the plasma and during this process undergo many collisions with different plasma species such as metal ions, gas ions, neutrals, and electrons before depositing on a substrate which is usually at a elevated temperature. Sputtering can be either DC (direct current) or RF (radio frequency) depending upon the nature of the target. DC power is used when the target is conducting, e.g., a metal, while RF can be used for both conducting and insulating, e.g., a ceramic target. Fig. 1.7.2.1 shows the two types of sputtering methods. Sometimes a magnetic field is applied by using a magnetron to increase the sputtering yield. In the presence of magnetic field the electron residence time increases in the plasma which leads to higher ion collision probability and therefore higher discharge currents. This is known as magnetron sputtering. More detailed discussion of sputtering process can be found elsewhere [92]. Reactive sputtering can be used for processing solid solutions, alloys or compounds. Reactive sputtering in a mixture of Argon (inert gas) and Oxygen (reactive gas) has been used for fabrication of oxide thin films since the 1970s.

1.7.2.1 Basics of Sputtering

After being ejected from the target surface the sputtered atoms have energies in the range of 10 - 40 eV and therefore velocities of about 3 - 7 x 10^5 cm/s. To have a high sputter yield it is imperative to have as many of the sputtered ions deposited on the
substrate as possible. To meet this goal the target and the substrate are closely spaced. Usually this is in the range of 5-10 cm. The mean free path (average distance traveled by a molecule before it collides with another molecule) of an ion is given by:

$$\lambda = \frac{0.05}{P}$$

where P (sputtering pressure) is in torr and $\lambda$ (mean free path) is in mm.

Fig. 1.7.2.1: Illustration of DC and RF sputter deposition process.

The mean free path of sputtered atoms at typical sputtering pressure is typically less than 5-10 cm. For ex. at 5 mTorr sputtering pressure the mean free path is ~ 1 cm. Thus the probability that the ejected molecule will suffer one or more collisions with the sputter gas while traveling towards the substrate is quite high. Thus three scenarios are possible under such circumstances:

(a) The sputtered atoms may arrive at the substrate with reduced energy (1-2 eV).
(b) They might be backscattered to the target or the chamber walls.

(c) They might lose so much energy that they move by diffusion in the same way as neutral gas atoms.

Thus sputtering gas pressure can impact various film deposition parameters such as deposition rates and composition of film.

One problem with sputtering of oxide thin films is resputtering of the growing films due to negative ions and reflected neutrals that lead to morphological changes on the film surface [94]. The presence of these morphological changes is a function of deposition rate, energy and flux of bombarding ions, angle of incidence of bombarding ions. Some studies have predicted that resputtering can be minimized by thermalizing (reducing the energy of the ions emanating from the target) the energetic species in the plasma either by off axis sputtering or using high sputtering pressure. Another contentious issue is whether to use a stoichiometric oxide target or use an elemental target. The target properties to look for are target purity and stoichiometry. The effect of various parameters on the quality of oxide thin films made by sputtering makes this quite a complex process. Various issues such as growth temperature, partial pressure of oxygen and total sputtering pressure, stoichiometry control, conformal growth, growth rates, and sputter yield have to be addressed to ensure the growth of high quality oxide thin films by sputtering.

In recent years researchers have studied the property and structure of thin films by varying different parameters of RF magnetron sputtering process such as substrate temperature, RF power, total sputtering pressure, ratios of partial pressure of Ar and O₂, the composition of the target, and the type of substrate.
Kim et al. [95] studied the effects of total pressure of working atmosphere on composition and properties of 80 nm thick BST (Ba:Sr = 0.5:0.5) thin films prepared by RF magnetron sputtering on platinised Si substrate. When the O₂ : Ar ratio was fixed at 1:5, the ratios of \((\text{Ba + Sr}) / \text{Ti}\) changed with a variation of the total gas pressure from 22–58 m Torr, and the deposition composition was deviated from the target composition, while the variation of \(p\text{O}_2: p\text{Ar}\) ratios had little effect on composition chemistry of thin films. The BST thin films exhibited a dense polycrystalline morphology, high dielectric constant \((\varepsilon = 430–530)\), high tunability \((n = 74\%)\) when \((\text{Ba + Sr}) / \text{Ti}\) ratios were > 0.85. Lower dielectric loss (0.0047) was observed for the sample with a \((\text{Ba + Sr}) / \text{Ti}\) ratio of 0.73.

Xu et al. [49] have studied the effect of substrates and post deposition annealing on the dielectric properties of BST thin films sputtered on MgO and LAO single crystalline substrates. They found that BST / MgO samples showed higher tunability than BST/ LAO samples. This was attributed to tensile stress in the former sample compared to compressive stress in the latter sample. Tunability improved significantly by post annealing in air at 900 °C for 5 hours. The sample grown under optimum condition showed a tunability of 22 % under an applied field of 10 kV /mm and a loss tangent of 0.0023 at a frequency of 1 MHz at room temperature.

P. Padmini et al. [41] at UCSB have studied the effect of texturing on tunability of BST thin films. RF sputtering was used to deposit BST thin films on Pt (100 nm)/TiO₂ (100 nm)/SiO₂ (100 nm)/Si substrates. The authors report that (100) textured BST thin films show increased tunability under optimized deposition conditions which is given by \(T_{\text{substrate}} = 550 \degree\text{C}, \text{ Ar} / \text{O}_2\) ratio of 90/10, and a total sputtering pressure of 50 mTorr.
These films exhibit a phase pure crystalline film, which is predominantly (100) oriented. According to the authors film growth on substrates that give rise to biaxial tension in the film (when $\text{CTE}_{\text{film}} > \text{CTE}_{\text{substrate}}$ where CTE is the thermal coefficient of expansion) results in the polar axis of the material orienting itself along the substrate surface. The authors attribute the higher tunability in the BST films due to this in-plane orientation of the polar axis.

Extensive work has been performed on sputter-deposition of ferroelectric thin films so far using both single multicomponent oxide and multiple elemental metallic targets. The main advantages of this process are the high throughput, the possibility to sputter on large area substrates, good adhesion of films, and the ability to get stoichiometric and conformal films. The sputtering processes described in this review are being developed for use in research laboratories and for commercial production of ferroelectric thin film-based MW devices. Various sputtering parameters such as RF power, sputtering gas pressure, substrate temperature, ratio of the sputtering gases are important since they determine to a large extent the composition and microstructure of the films which ultimately determines the dielectric properties of the films for MW applications.
1.8 Top Electrode Deposition

1.8.1 Various deposition technologies

From a device metrics point of view the most desirable electrical characteristics for BST thin-film varactor technology are high tunability, low device loss (or high Q-factors), and good power-handling capability. The technology for integration of ferroelectric thin films into MW device is still in its nascent stage and numerous problems have to be solved before it can mature into large scale manufacturing technology. The optimization of the growth process for BST thin films, top electrode metal and a suitable process flow for fabrication and integration of these films in the devices are the main sources of difficulty. The fabrication technology for the metallization process is very important and key issues must be addressed judiciously by the researchers in the field.

An important part of the processing is the metallization process for the top electrode. When preparing tunable MW devices for communication applications most often attention is invested in the preparation of the ferroelectric thin film compared to the metallization process. Metallization, however, is equally important and loss due to metallization is the most important mechanism for device loss especially at GHz frequencies [18, 52, 60, 96].

Two kinds of varactors, vertical (parallel-plate or MIM) or planar (interdigitated or IDC), are possible using BST thin films. The details of the two configurations, i.e. MIM and IDC are described in detail in section 2.9. For the interdigitated capacitors, BST films are directly deposited on the appropriate substrate (for ex LAO, MgO, sapphire, or polycrystalline alumina) followed by top interdigitated electrode
metallization. Material deposition techniques such as sputtering, and thermal evaporation are compatible with high production requirements and have been extensively used in the production of MW devices. DC sputtering is a widely used deposition technique for a variety of metals. Sputtering is done at low gas pressures in a plasma environment. It has been largely employed for the following reasons: most materials can be volatilized by bombardment of positive ions; it has high deposition rates and shows uniformity over large areas.

However thermal evaporation is the deposition method of choice for doing metallization for MW devices especially if the fabrication process involves a lift off process since thermal evaporation is a much more “line of sight” process compared to sputtering and this helps in metal lift off. Sputtering is a much more energetic process than thermal evaporation since it involves a plasma of energetic ions and this heats up the photoresist making metal lift off process very difficult and sometimes impossible. In thermal evaporation technique the average energy of vapor atoms reaching the substrate surface is generally low (tenths of eV). This is an advantage here since the photoresist is not adversely affected and since evaporated film adhesion is not as good as in sputtered films, metal lift off is much easier.

Y. Liu et al. [16] have used thermal evaporation to deposit Au as the top electrode for a MW phase shifter using BST thin films on single crystalline sapphire. 0.4 µm of Au was used as metallization for the IDEs while 1.5 µm of Au was deposited elsewhere to complete the transmission lines. A lift off process was used to define the IDE structure while the transmission lines were fabricated by an etch back technique.
J. Xu et al. [49] also have taken a similar approach by depositing a thin layer (10 nm) of Cr followed by 100 nm of Au by thermal evaporation to complete the metallization structure for the Au/ BST/ MgO and Au / BST/ LAO IDCs.

D. Kim et al. [50] from Georgia Institute of Technology fabricated a 2.4 GHz MW phase shifter using BST thin films on sapphire. Here the metallization stack consists of Au (250 nm) / Cu (2200nm) / Cr (30nm). Once again thermal evaporation was used for metallization of the top electrodes.

Similarly Bellotti et al. [48] have used e-beam evaporation to complete the metallization stack for the top electrodes for fabrication of BST thin film IDCs on LAO and MgO. Here the metallization stack consists of 1.5 µm of Ag and a thin capping layer of Au on top. Numerous researchers have used thermal evaporation technique for fabricating top electrodes in MW devices.

A suitable metallization process for fabricating MW devices should have the following characteristics: (a) It should be compatible with the whole process flow (b) It should be possible to get low resistivity metal thin films using the process (c) The process should enable thick metallization for achieving low insertion loss of devices. Thus thermal evaporation is the deposition method of choice for fabricating top electrodes in MW devices. Sputtering has also been used in a few cases but the advantage of using evaporation method far outweigh that of sputtering and is thus the more popular method for making top electrodes in MW devices.

1.8.2 Thermal Evaporation

The properties of thin films depend to a large extent on the fabrication process and the technique used. The fundamental process involved in physical vapor deposition
(PVD) of thin films is the removal of atoms from a solid or a liquid by energetic means, and the subsequent deposition of those atoms on the substrate [92]. Different kinds of PVD processes include thermal evaporation, laser ablation, physical sputter deposition, and arc-based emission.

Fig.1.8.2.1: Schematic of thermal evaporation process.

In vacuum thermal evaporation deposition technique, a material (in this case a metal) is heated under vacuum conditions until evaporation occurs as shown in Fig. 1.8.2.1. The material vapor condenses in form of thin film on the cold substrate surface. Usually low pressures are used (P < 10^{-6} torr) to obtain good quality films. Under such low pressures, the mean free path of vapor atoms is the same order as the dimensions of the vacuum chamber, so these particles travel in straight lines from the evaporation source towards the substrate. In thermal evaporation the average energy of vapor atoms reaching the substrate surface is generally low (tenths of eV). This affects the morphology of the films, often resulting in a porous morphology and films with poor adhesion property.
In thermal evaporation different techniques are used to heat the material to be evaporated. The two most widely used methods are: (a) resistance heating or thermal evaporation method (utilizing Joule effect) or (b) e-beam evaporation, utilizing a high-energy electron beam (E ~ few keV) from an electron beam gun. Thus the two popular evaporation technologies differ in the heating method. In resistive evaporation, a tungsten or molybdenum boat, containing the source material, is heated electrically with a high current to make the material evaporate. In e-beam evaporation, an electron beam is aimed at the source material causing local heating and evaporation.

Evaporative sources fall into two general classes; quasi equilibrium and non-equilibrium [91, 97]. In the first case, the evaporation process occurs under nearly steady state equilibrium with its vapor. An example of this type of source is the Knudsen cell. In this case the orifice is small compared to the remaining interior surface area of the cell, and losses through the aperture are mostly a perturbation on the dynamics of the liquid-vapor equilibrium in the cell.

On the other hand the non-equilibrium evaporation source can be thought of as an open source, where a small region of liquid material evaporates off into a large, low pressure volume. Since the pressure in the region of this liquid source is low, there is no return or equilibrium of the evaporated vapor flux to the source. Some examples of this kind are the boat, the crucible, and the e-beam source [98].

The boat used in evaporation is usually made of some kind of refractory metal, such as W, Mo or Ta, which is then heated by passing a large current (Joule effect) through the band of metal forming the boat. Here the evaporant material is usually completely melted, and this may sometimes lead to chemical reaction between the
evaporant species and boat material. Thus care is taken to ensure that the metal to be evaporated and the boat material are immiscible in the temperature range required for evaporation. Evaporation deposition occurs by placing a sample in the direct line-of-sight of the source. Usually the distance between the source and sample is kept between 10 – 100 cm for the practical reasons of allowing a larger deposition area and to limit sample heating by optical radiation emanating from the source. The flux emitted from the source follows a cosine distribution law and the deposition rate of the film scales as roughly the inverse of the square of the distance between the source and the substrate. Since the evaporated flux in many sources can be quite significant (µm s/min) at short distances, it is possible to deposit on a fairly large area at a reasonable rate [99, 100].

Thermal evaporation is an important technology for thin film fabrication and has certain advantages such as high growth rate and good uniformity of deposited films. It has been widely employed in the MW world for making top electrodes for MW devices. In this section the basics of thermal evaporation and a brief literature review of thermal evaporation technique used for depositing top electrode in MW devices is covered.
1.9 Microwave Devices

1.9.1 Microwave filter

Microwave filters are widely used in radar, satellite, and mobile communication systems. Bandpass and band reject filters are used in the receiver front end to ensure that only signals in the specified frequency range enter the receiver [32, 101]. In the ideal case a MW filter should have the following characteristics:

(a) A flat pass band response, i.e. low insertion loss over the whole pass band.
(b) Low return loss.
(c) Out of band rejection below and above the pass band should become very high as close as possible to the pass band edges. In other words the filter should have steep skirts at passband edges.
(d) They should have high power handling capability.
(e) Fast tuning response.
(f) Should have small size and mass.
(g) Should be inexpensive.

The characteristics of an ideal lossless MW filter are shown in Fig.1.9.1.1. Electronically tunable filters are required for many applications in frequency agile wireless communication systems [101]. So far these filters have been successfully implemented by using varactors [102-104], MEMs [105, 106], and ferroelectric thin films [19-21, 52, 107, 108].
At NASA Glenn, Subramanyam et al. have fabricated a (YBCO/SrTiO$_3$) thin-film K-band tunable bandpass filter on a LAO substrate [107, 108]. The two-pole filter had a center frequency of 19 GHz and bandwidth of 4%. A schematic of the filter is shown in Fig. 1.9.1.2. Tunability was achieved through the nonlinear temperature dependence and the dc electric field dependence of the relative dielectric constant of SrTiO$_3$ thin films. A center frequency shift of 0.85 GHz was obtained at 400 V DC bias and 77 K without any degradation in the insertion loss of the filter.
Fig. 1.9.1.2: Schematic of the YBCO/STO/LAO filter [107].

The field dependence of one of the filter's $S_{21}$ and $S_{11}$, at 77 K, measured at an input power level of $+10$ dBm are shown in Fig. 1.9.1.3.

Fig. 1.9.1.3: Experimental data showing the filter's $S_{21}$ and $S_{11}$ characteristics [107].

With increasing bias voltage, the center frequency of the filter shifted from 17.4 GHz at no bias to 19.1 GHz at 500V bias, giving a tunability factor of 9 %. With applied bias, both $S_{11}$ and $S_{21}$ improved as shown in the figure.
BST thin film-based low pass and band pass filters were reported by Tombak et al. at NCSU [19, 52]. These circuits used lumped inductors and tunable BST capacitors forming a 3\textsuperscript{rd} and a 5\textsuperscript{th} order Chebychev low pass filter at RF frequencies. The parallel plate BST capacitors had a Pt/ BST (70:30)/ Pt/SiO\textsubscript{2}/Si configuration. MOCVD technique was used to grow the 300nm thick BST thin films at ATMI. For the 3\textsuperscript{rd} order low pass filter, the maximum measured insertion loss in the pass-band was 0.8 dB and return loss better than 10 dB for all frequencies as shown in Fig. 1.9.1.4. The frequency of the filter tuned from 160 MHz to 210 MHz (30% tunability) with 9 V applied bias.

Fig. 1.9.1.4: Experimental data for 3\textsuperscript{rd} order filter's insertion and return loss with change in applied bias [52].

For the 5\textsuperscript{th} order low pass filter, the tunability was about 40\%. The insertion loss of the band pass filter was 7 dB at 0 V and reduced to 5.1 dB at 10 V as shown in Fig. 1.9.1.5. However all the circuits used here utilized discrete BST MIM capacitors for fabricating the devices. Thus it was more of a “packaged” system than an “integrated” system.
BST based MW filters have already been commercialized. Paratek Microwave Inc. has commercialized two types of BST-based bandpass filters [109]. Filters based on hybrid microstrip line configuration (f ~ 2 GHz) [110] and finline waveguide resonator configuration (f ~ 22.5 and 38.5 GHz) [111] have been reported. The first device is a 4-pole microstrip combline bandpass filter with tunable BST capacitors. The insertion loss at the pass band was 7.7 dB at 200 V, while the center frequency tuned from 2.16 to 2.36 GHz (9.3% tunability). On the other hand the three-pole finline filter operating at 22.5 GHz showed a maximum insertion loss of only 2 dB. A tunability of 2.2% was achieved with 300 V bias voltage. The other 2-pole finline filter had an insertion loss of 3 dB at 38.5 GHz and a tunability of only 1% at 200 V. The tunable capacitors used in these filters were fabricated using thick film (8 µm) BST interdigital capacitors (Au/BST/MgO).

This chapter gives a brief overview of MW filters and the work that has been done so far in integrating ferroelectrics in such devices. Despite frequency-agile filters
being of paramount importance in microwave systems, surprisingly few MW filters based on ferroelectric materials have been reported in the open literature. The potential of ferroelectric materials for microwave applications has been known for many years. However, it is only recently that interest and technology has developed to a stage that practical devices have been demonstrated. Integration of ferroelectric thin film technology in frequency agile filters gives the potential for a number of miniaturized and highly functional MW components capable of multitasking at different frequency bands.
1.9.2 Microwave phase shifter

The phase shifter is by far the simplest MW component that can be produced by utilizing ferroelectric materials and hence it has been reported by a large number of research groups [16, 34, 43, 50, 75, 115]. Phase shifters are used in the beam steering circuitry of phased array antennas for wireless communication systems. These antennas are made up of 2D arrays of radiating elements spaced ($\lambda_o / 2$) apart, where $\lambda_o$ is the wavelength of the signal in air. The angle at which the antenna beam is radiated or received is given by the angle at which constructive interference occurs between the radiating elements. The phase shift between adjacent radiating elements ($\phi$) required to produce a scan angle ($\theta_o$) is given as:

$$\phi = \frac{2\pi}{\lambda_o} s \sin \theta_o$$

where $s$ is the distance between the radiating elements. The scan angle ($\theta_o$) is assumed to be relative to the broadside, i.e. normal to the plane of radiating elements. Thus by changing the phase difference between the radiating elements the direction of the antenna beam can be steered. This phase difference can be achieved by utilizing phase shifters.

Phase shifters simply consist of a ferroelectric transmission line of appropriate length. A transmission line is usually modeled as a lumped element circuit consisting of a distributed series inductance and a distributed shunt capacitance (neglecting the distributed series resistance and shunt conductance). The transmission line must be matched to the external 50 $\Omega$ impedance and have low loss. It should also exhibit large phase shifts, with application of applied electric field and also capable of handling large power loads. The phase change ($\phi$) from input to output of the line is given by [112]:

69
$$\phi = \omega \cdot \sqrt{(L C_{\text{line}})}$$

where $\omega$ is the angular frequency, $L$ is the inductance of the line, and $C_{\text{line}}$ is the capacitance of the line.

Tunable BST capacitors (either MIM or IDC) are placed periodically along the length of the transmission line, capacitively loading the line, and the phase shift becomes:

$$\phi = \omega \cdot \sqrt{(L [C_{\text{line}} + C_{\text{BST}}])}$$

Now $C_{\text{BST}}$ (capacitance of tunable BST varactor) can be changed by changing the applied bias and thus the amount of phase shift can also be changed. This is the basic principle behind the operation of a phase shifter.

The first phase shifter using BST was reported by Flaviis in 1997 [113]. Bulk BST with thickness as high as 0.1 - 0.15 mm was used in the microstrip line circuit. A phase shift of 165° was obtained at 2.4 GHz with insertion loss ~ 3 dB when a bias voltage of 250 V was used. In 1999, Van Keuls et al. [114] reported a thirteen-section Ku-band coupled microstrip phase shifter, in which BST interdigital capacitors were used as the series coupling components. A phase shift of 200° was obtained at a frequency of 14 GHz with insertion loss of 4.7 dB by using a bias voltage of 400 V.

Perhaps the most comprehensive work on phase shifters based on ferroelectric thin films has been done at UCSB. York et al. has reported several phase shifters using parallel plate and interdigital BST capacitors [16, 17, 115, 116]. Acikel et al. have demonstrated an X-Band 180° phase shifter using parallel plate MIM BST capacitors [115]. The BST capacitors were used in the periodically loaded CPW line as shown in Fig. 1.9.2.1. The circuit provided 240° phase shift with an insertion loss of 3 dB at 10 GHz at room temperature when 17.5 V dc bias was applied.
The MW characteristics of the phase shifter are shown in Fig. 1.9.2.2. The phase shifters show a figure of merit of $93^\circ / \text{dB}$ at 6.3 GHz and $87^\circ / \text{dB}$ at 8.5 GHz. This circuit achieved the best figure of merit reported in the literature for the BST phase shifters. The figure of merit for a phase shifter is defined as the phase shift (in degrees) / loss (dB).
In this chapter the basics of a MW phase shifter is covered. Recent work on utilizing ferroelectric thin films in phase shifters is discussed. BST based phase shifters offer a single analog control voltage, reasonable loss at GHz frequencies, negligible power consumption, high power handling capability, small size, high reliability, and low cost and thus look very promising for improving the system performance in a wireless communication network.
References:


(2) http://www.lbl.gov/MicroWorlds/ALSTool/EMSpec/EMSpec2.html


(22) E.R. Caley and J.F.C. Richards, “Theophrastus on stones”, Columbus, OH, Ohio State University, (1956)


(34) A.K. Tagantsev, V.O. Sherman, K.F. Astafiev, J. Venkatesh and N. Setter,


(38) P. M. Suherman, T. J. Jackson and M. J Lancaster, “Broadband Microwave Characterization of Ferroelectric Thin Films”, Portfolio Seminar, University of Birmingham, UK, April 2004


(47) T. Donegan, “PTFE Substrates Require Special Care in Fabrication”, Microwaves, (1982)


(90) Jayesh Nath, Dipankar Ghosh, Jon-Paul Maria, Michael B. Steer, Angus I. Kingon, Gregory T. Stauff, “Microwave Properties of BST Thin Film Interdigital


109) www.paratek.com


2.0 RESEARCH OBJECTIVES AND APPROACHES

Recently numerous investigations have focused on integration of ferroelectric thin films for use in MW devices for communication purpose taking advantage of the high tunability, low loss at GHz frequencies, fast tuning speed, and power handling capability of ferroelectric materials. Most of this work in MW device involves epitaxial ferroelectric thin films grown on single crystal substrates using noble metal electrodes. In most cases epitaxial BST thin films have been used because of perceived advantages including high figure of merit and thermal stability etc.

Conventional wisdom teaches us that epitaxial ferroelectric thin films grown at high temperature will most likely simulate the highly sought after properties (high tunability and low loss tangent) of single crystal ferroelectrics. To this end most MW designers and researchers have used single crystalline substrates such as MgO, LAO, and sapphire on which epitaxial BST thin films can be grown at high temperatures (T~ 600 - 750 °C). Not only are these substrates expensive they are also only available in limited sizes and shapes. According to conventional technology, noble metallization is the best case scenario for MW devices since they form stable non reactive Schottky contacts. To this end most MW circuits have utilized noble metals such as Pt, Au and Ir in the metallization process. However noble metals are very expensive and patterning them is cumbersome since it usually involves hazardous and toxic etching reagents. Another important parameter is the microfabrication technique used for making the MW devices. Many MW devices use a MIM configuration since it allows more efficient control over the tuning voltages. However MIM geometry requires complex three step (i.e. patterning the bottom electrode, the dielectric film, and the top electrode) microfabrication
technique, and preparing devices with suitably small capacitance values require challenging lithographic dimensions.

In this project the central goal is to successfully design and demonstrate a complementary technology and process flow for integration of BST thin films in MW devices that is not only cost effective but exhibits competitive performance. If the technology of tunable ferroelectric microwave devices is to be realized the above goals must be met. To achieve this central goal a set of individual but significant challenges have to be overcome. They are summarized below.

In this work we have used polycrystalline alumina as the MW substrate. It is inexpensive, available in varied shapes and sizes and “MW friendly”. The challenge with using ceramic substrates are related to surface imperfections and limits of polishing which make photolithography and microfabrication on these difficult. Consequently the goal was to engineer the compatibility of ceramic alumina substrates with the whole process flow for BST based MW devices.

Here we have used RF sputtering as the deposition tool for making BST thin films. In the past there have been many demonstrations of high quality BST thin films using this process. The challenge here was to identify a low temperature deposition condition that provides competitive ferroelectric properties in contrast to the high temperature deposition process traditionally used for fabricating epitaxial BST thin films on single crystalline substrates. Various BST thin film processing parameters, such as deposition temperature, sputtering pressure, annealing time and temperature, were modified to achieve optimum tunability and dielectric loss.
The next technical challenge was to integrate base metal in the metallization process. Cu was chosen as the metal of choice since it has the highest conductivity of all base metals; it is inexpensive and widely available. However there are some issues that need to be addressed while using Cu in metallization process such as poor adhesion to oxide thin films, large CTE mismatch with BST, and reactivity at ambient atmospheres. The primary goal here was to engineer the compatibility of Cu metallization with BST based MW devices.

The final challenge lay in demonstrating a suitable microfabrication process flow. IDC (planar capacitor) configuration was used since integrating IDCs in MW circuits is much easier than MIM (parallel plate capacitor) configuration. A modified bi-layer lift off photolithographic process, which allowed patterning small feature sizes (3 - 6 μm) with multiple μm thickness for achieving low insertion loss in the device, was developed and used in this work. This process uses chemicals that are compatible with both BST and Cu thin films. This is a simple, single step process as opposed to complex lithographic process used in the traditional MIM configuration for making MW devices.

Finally a “real world” MW band pass filter and phase shifter based on a low cost package (Cu/ BST / alumina) are fabricated and tested. Their performance is evaluated with respect to other reported MW devices using epitaxial ferroelectric thin films on single crystalline substrates and noble metallization.

This work demonstrates the feasibility of using ceramic alumina substrates, polycrystalline BST thin films, base metal Cu metallization and single step microfabrication technique for making MW devices. In summary it is demonstrated that BST thin film integrated MW devices based on widely available, inexpensive materials
and processing technology that is entirely amenable to high volume manufacturing, can show competitive performance. The performance of tunable dielectric components based on this technology looks very promising and is likely to play a major role making future wireless communication cost effective and more efficient.
3.0 EXPERIMENTAL PROCEDURE

3.1 Processing of BST thin films

In this work we have used RF (radio frequency) magnetron sputtering to deposit $(\text{Ba}_{0.6}\text{Sr}_{0.4})\text{TiO}_3$ thin films on 625 $\mu$m thick polished alumina substrate (Intertec Southwest Inc., Tucson, AZ) using a 4" stoichiometric ceramic BST $(\text{Ba}_{0.6}\text{Sr}_{0.4})\text{TiO}_3$ target (Super Conductor Materials Inc., NY). A Ba: Sr composition of 60:40 was chosen such that the BST was in the paraelectric state at room temperature and close to the Curie temperature thus providing an optimum figure of merit value for the BST films. A schematic of the RF sputtering chamber is shown in Fig. 3.1.1.

Before deposition, the alumina samples were cleaned using acetone and methanol and then a dehydration bake was done at 150 °C for 5 min. The substrate holder is designed in such a way that it can be heated to elevated temperatures (T $\sim$700 °C) and could be rotated to ensure uniform deposition during the sputtering process. The chamber vacuum was maintained by a Alcatel turbo pump roughed with a Alcatel rotary vane pump.
Sputter deposition was performed at two different substrate temperatures, 130° C and 300° C, for 60 minutes using an 30° off axis geometry in an argon / oxygen mixture (Ar: O₂ = 5:1) to obtain uniform film thickness and optimal stoichiometry. A deposition time of 60 minutes gave a film thickness of 600 nm. The film thickness was verified using a Sloan Dektak – 2 profilometer. Note that in this sputter arrangement, despite the 30° incident angle, the gun normal pointed at the center of the substrate. The sputtering pressure during deposition was varied between 5 and 12.5 mTorr in increments of 2.5 mTorr. The deposition conditions are summarized in Table 3.1.1.
Table 3.1.1: Deposition conditions for RF sputtering of BST thin films

<table>
<thead>
<tr>
<th>Target</th>
<th>$\text{Ba}<em>{0.6} \text{Sr}</em>{0.6} \text{TiO}_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF power</td>
<td>300 W</td>
</tr>
<tr>
<td>Reflected power</td>
<td>25-30 W</td>
</tr>
<tr>
<td>Target to sample distance</td>
<td>8.5”</td>
</tr>
<tr>
<td>Sputtering gas (Ar:O$_2$)</td>
<td>5 :1</td>
</tr>
<tr>
<td>Base pressure of chamber</td>
<td>$5.0 \times 10^{-5}$ Torr</td>
</tr>
<tr>
<td>Sputtering pressure</td>
<td>5.0, 7.5, 10.0, 12.5 mTorr</td>
</tr>
<tr>
<td>Deposition temperature</td>
<td>300 °C</td>
</tr>
<tr>
<td>Deposition time</td>
<td>60 min</td>
</tr>
</tbody>
</table>

After deposition the BST / alumina sample was annealed *ex – situ* in air between 650 °C and 1000 °C respectively in an air furnace to crystallize and densify the BST samples. Annealing time was varied between 1 and 72 hours. Optical microscopy was used to check for any signs of cracking after annealing.
3.2 Characterization Tools

3.2.1 XRD (X-ray diffraction)

Structural characterization of the BST thin films was done by XRD using a 4-circle Bruker AXS D-5000 using a HI-STAR area detector. The X-Ray source was Cu K$_\alpha$ radiation generated at 40 kV and 30 mA. Typical scans were collected for a duration of 15 minutes. This instrument is well suited for phase identification of crystalline thin films and was primarily used for this purpose in this work. A screen shot of the XRD is shown in Fig. 3.2.1.1.

Fig. 3.2.1.1: Screenshot of the XRD scan of the BST / alumina sample.
3.2.2 AFM (Atomic Force Microscopy)

Microstructural characterization was done using AFM (Atomic Force Microscopy). AFM operates by measuring the atomic forces between the probe and the sample. These forces depend on a number of factors such as the type of sample and probe, distance between probe and sample, and sample surface contamination. AFM does not require conducting samples and thus can be used for insulators, such as ferroelectric thin films, as well as for conductors. The AFM instrument consists of a cantilever, usually made of silicon nitride, silicon, or silicon oxide with a sharp tip mounted on its end. The tip is usually made from silicon nitride. Laser light is focused on the cantilever top and reflected to a segmented, position sensitive photodetector. The cantilever is brought close to the sample surface and rastered in the x–y direction using piezoelectric scanners. By keeping the photodetector signal constant and by varying the sample height through a feedback arrangement, gives the vertical sample height variation compared to a base line.

An AFM can operate in various modes. In contact mode the tip is in contact with the sample surface. In tapping mode, the tip is excited to vertical oscillations close to its resonance frequency. As the tip approaches the sample surface, the attractive forces increase causing a decrease in resonance frequency. Since the amplitude is kept constant, the tip-sample distance also remains constant. In this mode the probe exerts negligible frictional force on the sample and therefore the surface damage is minimized.

A CP Research Thermomicroscope AFM was used in the tapping mode to determine surface microstructure, roughness and grain size of the BST thin films on
alumina substrate. Scans were done over 1 x 1 µm² areas. All measurements were done with the help of Jon Ihlefeld, Electroceramic Thin Film Group, MSE Department, NCSU.

3.2.3 Four-point probe

Electrical resistivity measurements of the Cu thin films were done by a Magnetron Instruments (model M - 700) four-point probe capable of measuring both the resistivity and the type of conductivity (n type or p type) of the samples. Before measuring a calibration sample was used to test for measurement accuracy. The sheet resistance was found out in (Ω / □) and then the value of sheet resistance was multiplied by the thickness to get the resistivity values.

3.2.4 Profilometer

Profilometry is a fast and simple method to measure film thickness. It works by gently dragging a mechanical stylus across the sample surface. The stylus is placed in contact with, and then gently dragged along the surface of the substrate. The vertical deflection measures the change in step height and the trace is recorded with high accuracy. To measure the thickness of thin films used in this work, part of the substrate was covered with a rectangular piece of Scotch Tape during film deposition. After the thin film deposition, the tape was removed and film thickness was then measured over the step. For the experiments done in this work a Dektak Sloan – 2 profilometer was used. The instrument was calibrated prior to use to ensure accurate measurements.
3.3 Thermal Evaporation

3.3.1 Cu thin film fabrication

Cu thin films for the top electrodes were fabricated using a dual deposition chamber which consists of a resistive thermal evaporator cell along with a DC sputtering cell. A schematic of this instrument is shown in Fig. 3.3.1.1. The chamber vacuum was maintained by a Varian M6 diffusion pump roughed with a Leybold Trivac rotary vane pump.

Fig. 3.3.1.1: Illustration of the dual deposition chamber (thermal evaporator cell and DC sputtering cell)
The boat source used for resistive heating was made from W (Tungsten). It was resistively heated by passing a large current through it. OFHC (Oxygen Free High Conductivity) Copper O-rings were cut into small pieces (~ 5 x 5 mm), cleaned using acetone and methanol, and used as the source for thermal evaporation of Cu. Samples were mounted on a rotatable substrate manipulator using vacuum grease such that the sample was directly in the line-of-sight of the source. Vacuum grease was used to ensure good mechanical and thermal contact between the sample and the substrate manipulator. The rotatable substrate manipulator was water cooled at all times to ensure that the photoresist patterned sample did not get heated up during the thermal evaporation process. The distance between the sample and the source was maintained at 5”. A heat shield, with a 1” circular opening to ensure the line-of-sight geometry between source and sample, was placed between the source and the sample to minimize sample heating from radiation from source.

To ensure low insertion loss of MW devices, thick, low resistance electrodes are necessary since at GHz frequencies losses due to metallization begin to dominate [1-3]. For current devices \( t \) (thickness) > 1 \( \mu \text{m} \) of copper with \( \rho \) (resistivity) < 3 \( \mu \Omega \text{-cm} \) is required. Cu does not adhere well to oxide surfaces and hence thin adhesion layers (20-30 nm) of Ti, Cr or TiW are usually used to promote adhesion [4]. Metal with large heats of oxide formation such as Cr, Ti, Ta etc acts as the “glue” between Cu and the oxide thin film. Also the metallization needs to be patterned by a photolithographic lift-off method with 3-5 \( \mu \text{m} \) features. DC sputtering can be used to prepare Cu top electrodes \( (t > 1 \, \mu \text{m}) \) with Cr or Ti adhesion layer. However conditions providing thick, low resistivity Cu harden the patterned photoresist, making lift-off very difficult.
For these various reasons, we chose thermal evaporation as the method of choice for depositing top electrodes for MW devices. The thermal evaporation chamber was modified to make a dual deposition chamber in which both off axis DC sputtering and thermal evaporation is possible as shown in the figure above. The advantage of using this modified system is that in-situ deposition of Cr thin film (adhesion layer) by DC sputtering and Cu thin film (top electrode) by thermal evaporation is possible without breaking vacuum.

First Cr was presputtered for 3 minutes to ensure that the metallic Cr target was clean and free from impurities and then the water cooled substrate manipulator was rotated such that Cr could be sputtered from the 1” target onto the sample. An on-axis geometry was used in this case and Ar was used as the sputtering gas. Next the sample was rotated yet again by using the rotatable substrate manipulator such that it was aligned with the evaporation source. The chamber was pumped down to the required base pressure and then thermal evaporation was started by increasing the current from the power source in increments of 50 A. The power source for the thermal evaporator was operated in the constant current mode. The details of the in situ Cr dc sputtering and the Cu thermal evaporation process are given in Table 3.3.1.1 and Table 3.3.1.2 respectively.

Periodically the chamber walls were cleaned and the Cu films deposited on the chamber walls were stripped off. Similarly the evaporation boats were also changed as needed to ensure a clean and efficient deposition process.
Table 3.3.1.1: Deposition conditions for Cr sputtering

<table>
<thead>
<tr>
<th></th>
<th>Cr</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC power</td>
<td>25 W</td>
</tr>
<tr>
<td>Target to sample distance</td>
<td>2”</td>
</tr>
<tr>
<td>Sputtering gas</td>
<td>Ar (10 sccm)</td>
</tr>
<tr>
<td>Base pressure of chamber</td>
<td>1.0 x 10^{-6} Torr</td>
</tr>
<tr>
<td>Sputtering pressure</td>
<td>20 x 10^{-3} Torr</td>
</tr>
<tr>
<td>Presputtering time</td>
<td>3 mins</td>
</tr>
<tr>
<td>Deposition time</td>
<td>2 min</td>
</tr>
</tbody>
</table>

Table 3.3.1.2: Deposition conditions for thermal evaporation of Cu

<table>
<thead>
<tr>
<th></th>
<th>OFHC Cu pieces</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC power</td>
<td>400-500 W</td>
</tr>
<tr>
<td>Target to sample distance</td>
<td>5”</td>
</tr>
<tr>
<td>Base pressure of chamber</td>
<td>5.0 x 10^{-7} Torr</td>
</tr>
<tr>
<td>Pressure during evaporation</td>
<td>1.0 x 10^{6} Torr</td>
</tr>
<tr>
<td>Evaporation time</td>
<td>25 - 60 min</td>
</tr>
</tbody>
</table>

By using this dual deposition system the challenges of Cu deposition can be overcome; Cr thin film adhesion layer and multiple μm thickness Cu thin films are possible without breaking vacuum and without damage to the patterned resist on the sample.
3.4 Microfabrication

3.4.1 Bilayer lift off process

In this work a modified bilayer photolithographic process was developed and used to pattern the metallization required for the MW devices. A single step bilayer lift off process was chosen since it uses benign organic chemicals which do not react with BST thin films. In contrast wet chemical agents used for etching Cu such as CuCl$_2$ + HCl (Cupric chloride + Hydrochloric acid), FeCl$_3$ + HCl (Ferric chloride + Hydrochloric acid) and (NH$_4$)$_2$S$_2$O$_8$ (Ammonium persulphate) reacts with BST and also produces toxic by products. Another option is reactive ion etching (RIE) process [4 - 6]. It produces very fine features and is a well known microfabrication process. However patterning Cu electrode material involves Cl$_2$-based chemistry which is harmful for oxide materials such as BST. A summary of the various microfabrication techniques available and their pros and cons are summarized in Fig. 3.4.1.1.
Microfabrication process

Fabrication technique

**Wet etch**
- Well known process
- Inexpensive
- Harmful chemicals for BST
- Toxic products
- Undercut problem for Cu

**Plasma etch**
- Well known process
- Small feature sizes
- Expensive process
- Harmful chemicals for BST

**Bi layer lift off process**
- Inexpensive
- Benign chemicals for BST and Cu
- Single step process
- Limited by aspect ratio of features

Fig. 3.4.1.1: A schematic of various microfabrication processes.

Individual IDCs and IDC integrated MW devices were fabricated on the BST/alumina samples by photolithography and a bilayer metal lift off process. A bilayer technique using positive imaging photoresist Shipley 1813 and MicroChem LOR (Lift off resist) 5A, was used for patterning the metallization lines. LORs used in bi-layer resist processes can produce sub micron profiles, do not intermix with g-line, i-line or deep UV resists and do not require an additional exposure step [7]. MicroChem’s LOR lift-off resists are based on the PMGI (polydimethylglutarimide) chemistry. They are used in combination with conventional positive resists and are available in a wide range of film thicknesses and undercut rates. LOR A resists dissolve at different rates in the developer
and thus have a different undercut rate than the positive photoresist Shipley 1813. This undercut helps in the lift off process.

The advantages of LOR resists are: (a) submicron linewidth control, (b) finely tuned undercuts, (c) no reaction or mixing with imaging resists (no scum), (d) good adhesion to Si, III-V and II-VI and oxide thin film materials, (e) simple bi-layer fabrication process which does not require additional flood exposure, development, amine treatment or toxic chemical soak steps, (f) it can be used for multiple micron deposition processes depending on the feature sizes.

Fig. 3.4.1.2: Spin speed vs. film thickness for LOR A series resists [7].

The entire process flow for the bi layer photolithographic process is outlined below:

1. Spin coat acetone and methanol on sample at 3000 rpm for 40 s using a Headway Research Inc. spin coater.

2. Dehydration bake at 140 °C for 2 min.

3. Spin coat LOR 5A at 3000 rpm for 40 s for a thickness of 550 nm.

4. Bake LOR 5A at 140 °C for 2 min.

5. Spin coat LOR 5A at 3000 rpm for 40 s for a thickness of 550 nm.

6. Bake LOR 5A at 140 °C for 2 min.
(7) Spin coat LOR 5A at 3000 rpm for 40 s for a thickness of 550 nm.

(8) Bake LOR 5A at 140 °C for 4 min.

(9) Spin coat Shipley1813 at 3000 rpm for 40 s for a thickness of 1300 nm.

(10) Bake Shipley1813 at 115 °C for 1 min.

(11) Mask alignment using MA 6 Karl Suss contact mask aligner in the ST + soft contact mode.

(12) Exposure to UV light (I line, \( \lambda = 365 \) nm) at \( I = 15 \) mW / cm\(^2\).

(13) Development in MF 319.

(14) DI water rinse and blow dry with dry N\(_2\).

LOR A series resists are ideally suited for thin-film processes but in this work the process was tuned such that this resist could be made to work for much thicker film (> 1.0 \( \mu \)m) lift off process. For clean lift-off processing, the LOR film should be thicker than the metal thickness, typically 1.2 to 1.3 times the thickness of the metal film. Thus for individual IDCs where thin metallization (0.1-0.3 \( \mu \)m) was required, optimum LOR 5A thickness needed was 0.5 \( \mu \)m while for MW devices, where thick metallization is required, ~1.5 \( \mu \)m of LOR 5A is needed to get a 1.0 \( \mu \)m metal lift off. In the first case single step spin coating and baking of LOR 5A is sufficient to get the required thickness. However to get 1.5 \( \mu \)m thickness of the lift off resist multiple coatings of LOR 5A are necessary. Hence LOR 5A was spin coated and baked 3 times to get the required thickness. Baking was done in three steps of 2, 2 and 4 minutes respectively at 140 °C. Baking photoresists essentially hardens it and turns it into a thermal insulator. Hence the longest baking time was reserved for the last step such that all the three LOR 5A layers are baked properly.
Once suitable patterns were prepared, a two-layer metallization stack was deposited. Initially, a thin layer of Cr (20 nm) was dc magnetron sputter deposited and subsequently (500 -1500 nm) of Cu was deposited by thermal evaporation in the dual deposition system as explained in chapter 3.3. To complete the circuit fabrication, lift-off was performed by immersion into MicroChem PG remover at 60 °C and subsequent ultrasonication in the same solution at room temperature for 15 seconds. The samples were then thoroughly rinsed in DI water and blow dried in N₂. A schematic of the whole photolithographic process flow is shown in Fig. 3.4.1.3.

![Photolithographic Process Flow](image)

Fig. 3.4.1.3: Illustration of the bilayer lift off process.

### 3.4.2 IDC geometry

As mentioned in the previous section the BST thin film IDCs were prepared using a bilayer lift off process. The geometry of the IDC is shown in Fig. 3.4.2.1. The geometry
of an IDC is characterized by the following parameters: \( W \) = width of the fingers, \( S \) = spacing between the fingers, \( L \) = length of fingers, \( E \) = spacing between finger and pad, \( W_f \) = width of pad, and \( N \) = no. of fingers.

For the various IDCs used in this work the dimensions of the various parameters were as follows: \( W = 3 - 10 \ \mu m, \ S = 3 - 10 \ \mu m, \ L = 50 - 1000 \ \mu m, \ E = 3 - 10 \ \mu m, \ W_f = 50 - 100 \ \mu m, \ N = 6 – 60. \)

Fig. 3.4.2.1: Schematic of a BST interdigitated capacitor

After fabrication of the IDCs, they were inspected in an optical microscope. Furthermore the dimensions of the IDCs were verified using SEM (Scanning Electron Microscopy). A Hitachi S3200 SEM was used for this purpose. The micrographs shown in Figs. 3.4.2.2 and 3.4.2.3 show the IDEs as part of a MW filter structure and a close up of an IDE respectively.
Fig. 3.4.2.2: SEM Micrograph of an IDC as part of a Microwave filter (450 X)

Fig. 3.4.2.3: SEM micrograph of an IDC close up (2500 X)
3.5 Electrical Characterization

3.5.1 Low frequency measurements

The electrical characterization of the IDCs was carried out by various instruments. For low frequency measurements (upto ~10MHz), CV (capacitance – voltage) and C-f (capacitance –frequency), a HP 4192 LF impedance analyzer was used. The HP 4192 A LF impedance analyzer can be used in the frequency range of 5 Hz- 13 MHz. CV measurements were done as cycle sweeps (negative voltage , -35V, to positive voltage , + 35V, and back to negative voltage, -35 V ) to check for any possible hysteretic behavior or spontaneous switchable polarization. None were observed within the limits of our instrument resolution. The initial bias was set at –35 V and swept to +35 V in 2 V increments. All discrete IDC measurements were done at a frequency of 1 MHz since the capacitance values measured were rather low (C ~ 0.2-10 pF) compared to typical MIM capacitors (C ~ 30 - 500 pF). An AC oscillation level of 0.05 V was used for all measurements.

The current voltage (IV) characteristics were determined using a Keithley 617 programmable electrometer. The measurements were carried out using a step voltage ramp, where the current was measured at the end of each voltage step. To eliminate transient processes, a delay time was employed before the current values were collected. A voltage step of 1 V, a pre test relaxation time of 5s, and a delay time of 3s were used in all cases. The measurements use DC signals and so the issue of test frequency does not arise here. All leakage current measurements were done at room temperature.
3.5.2 Microwave measurements

The frequency dependence of the capacitance and loss tangent was measured using an Agilent (model E 4991A) impedance analyzer. Cascade Microtech GS probes with a pitch of 150 µm was used for this purpose. The measurement setup was calibrated using a commercial standard. All frequency sweeps were done at room temperature between 1 MHz and 1 GHz.

The microwave properties (1 to 26.5 GHz) were measured in a one-port configuration using a HP 8510 C Network Analyzer as shown in Fig. 3.5.2.1. Prior to testing, one port OSL (open, short, 50 Ω load) calibration was performed. A 100 µm pitch GS probe was used, and reflection (S11) data was treated using a model [8] which takes into account series resistance, inductance and a parallel resistor- capacitor circuit. Detailed account of the model is given in the results and discussion section (4.2.2). This allowed determination of the device quality factor which includes contributions from the dielectric, substrate, and metallization lines.

Fig. 3.5.2.1: IDC under test in the HP 8510 C Network Analyzer
3.6 Fabrication of a Microwave filter

Tunable filters using BST thin film varactor can be implemented using various topologies. There are basically two choices for each topology: lumped element or distributed implementation. A distributed element approach was chosen for this work since it allows the integration of the BST varactor in the circuit in the same fabrication step, this helps maximize the Q by reducing the series resistance [9]. A 3\textsuperscript{rd} order combline bandpass filter was designed with center frequency of 1.75 GHz and 3 dB passband of 20 % of the center frequency. The filter was designed using the MFilter synthesis tool in Genesys suite of EDA from Eagleware [10] by Jayesh Nath, ECE, NCSU. This initial design was then modified and optimized for fabrication.

All width and spacing for the filter design were made equal so that the filter was symmetrical about the y-axis. The nominal electrical length of the resonator was 60 ° and the impedance was 60 Ω. A tapped design was used for the input and output feed and the impedance of the feed line were 50 Ω. The schematic of the optimized filter is shown in Fig. 3.6.1.

The filter parameters were as follows: \( w = 550 \ \mu\text{m}, s = 450\mu\text{m}, L_1= 5900\mu\text{m}, \) \( L_2= 4600 \ \mu\text{m}, W_f = 6000 \ \mu\text{m}, L_f = 5225 \ \mu\text{m}. \) At the end of each BST varactor a DC blocking capacitor with a rating of 200 V was attached. This serves as the bias point for the BST varactors while providing a RF ground path for the high frequency AC signal. Parasitic resistances and inductances were also modeled in the design phase and filter parameters were adjusted to get the desired filter response. The layout of the filter was done in ADS (Advanced Design System).
RF magnetron sputtering technique was used to deposit 600 nm (Ba$_{0.60}$Sr$_{0.40}$) TiO$_3$ thin films on polycrystalline alumina substrate (Intertec Southwest Inc., Tucson, AZ). Details of the RF sputtering conditions are described in section 3.1.1. The alumina substrates were 14 mm x 14 mm in size and 625 µm in thickness. After deposition the BST/alumina samples were annealed at 900° C in air for 20 hours to obtain fully dense and crystalline BST perovskite structure. A modified photolithographic bi layer lift-off process was used to define the fingers of the interdigital varactor and the feed electrodes as described in section 3.4.1. The metallization scheme consists of two steps. First a thin layer of Cr (20 nm) was sputtered and this was followed by deposition of 500 nm – 1500 nm of Cu, either by sputtering or by thermal evaporation (in the dual deposition chamber). Finally a capping layer of Pt (20 nm) was deposited on top of the Cu layer. This was done to prevent the ambient oxidation of Cu and also to assist in the wire
bonding to the surface. Metal lift off was done by immersing the sample in Microchem Remover PG solution to define the complete filter structure.

Then the backside of the alumina substrate was metallized using two different procedures. In the early stages of the filter fabrication (Series - 1 filters), metallization of the backside consisted of sputtered Cr (20 nm) and sputtered Cu (1000 nm), this acts as the ground plane. After the fabrication of the filter on the alumina substrate the filter assembly was done on a high frequency laminate (see Fig. 3.6.2) using conductive epoxy.

![Fig. 3.6.2: Schematic of the assembled filter on the high frequency laminate.](image)

The top Cu surface of the board served as the common ground plane. For Series - 1 filters a “via” or “through wafer interconnect” process was not used. Thus the ground connections at the end of the resonators were made by “ground-wrapping” using conductive epoxy. The additional resistance (approximately 1 $\Omega$ for each ground connection made) introduced by this technique of ground were taken into account in the simulation. The input and output connections to the filter was made using a J-Micro CPW-to-Microstrip adaptor [11]. The adapters were wire bonded to the input and output.
feed lines using a ball bonder. At each stage of assembly the integrity of the contacts was carefully monitored.

For filters fabricated in the later stages of the research work (Series - 3 filters), via or through wafer interconnect process was introduced. Vias (diameter - 250 µm, height - 625 µm) were laser drilled in the alumina substrate. The backside of the alumina sample was sputtered (Cr, 20 nm as adhesion layer and Cu, 100 nm as seed layer) and then electroplated in a CuSO₄ solution to make a 10 µm thick Cu ground plane. This way contact was made from the transmission lines on the top side of the filter to the ground plane Cu and this process eliminated the need for additional conductive epoxy and J-Micro CPW – to - Microstrip adaptor. For Series-3 filters, the filters could be tested directly “on chip” rather than using adaptors as in Series -1 filters.

Fig. 3.6.3: Filter under test in the HP 8510 Network Analyzer.
The filter was measured (see Fig. 3.6.3) on a HP 8510 C Network Analyzer using a 150 μm pitch GSG (ground-signal-ground) probe from GGB industries [12]. All measurements were done at room temperature. A LRM (line-reflect-match) calibration was done using CS-5 calibration substrate from GGB industries. The BST varactors were biased using a HP 4142 B parameter analyzer and DC probes at one end of the DC blocking capacitors. All varactors were tuned in tandem though it is also possible to tune them independently. The DC bias was varied from 0 V to the maximum bias possible, depending on the IDCs, (180 - 200 V) in steps of 25 V and the S parameter data was recorded at each bias point. From the S parameters the MW characteristics of the filter such as the insertion loss ($S_{21}$) and the return loss ($S_{11}$) were extracted. Measurements and performance of the MW filter will be discussed in details in the results and discussion section.
3.7 Fabrication of a Microwave phase shifter

Low loss and inexpensive MW phase shifters are required to improve performance and reduce the cost of phase arrays in wireless communication systems. Ferroelectric thin films such as BST have been investigated as a potential candidate for integration into such devices [13, 14]. In these circuits, the BST either forms a fraction of the substrate or the entire microwave substrate, on which the conductors are deposited [15, 16]. In this work we follow the second approach and the phase shifter design is based on BST IDCs periodically loading a transmission line.

An X-band (8 - 12 GHz) periodically loaded phase shifter was fabricated to provide adequate phase shift with low loss at 10 GHz. The Bragg frequency for the periodically loaded line was chosen to be ~ 50 GHz. The loading BST capacitors have a zero bias design capacitance of 80 fF. To preserve the symmetry, 8 pairs of BST IDCs were connected in parallel from the CPW center conductor to both ground planes. The line consisted of the center conductor width ($w$) of 200 µm, ground to ground spacing $d = 340$ µm, and unit cell length of $l_{\text{section}} = 1150$ µm. Alumina substrate thickness was 625 µm. A schematic of the MW phase shifter is shown in Fig. 3.7.1.

The process flow for the MW phase shifter is quite similar to MW filter and a brief description is provided below. The first step in the fabrication process was the deposition of BST (Ba : Sr =60 : 40) thin films on the polycrystalline alumina substrate by RF sputtering at 300 °C as described in section 3.1.1. Then a crystallization anneal was done ex-situ in air at 900 °C for 20 hours. Then the BST/alumina samples were patterned by using bi layer resists (Shipley 1813 + LOR 5A). Metallization was done in
the dual deposition chamber using dc sputtered Cr (20 nm) and thermally evaporated Cu (1000 nm). The electrodes were patterned by liftoff process to complete the whole phase shifter structure.

Fig. 3.7.1: Schematic of the X-band phase shifter

The phase shifter was measured using a HP 8510 C Network Analyzer using a 150 µm pitch GSG (ground-signal-ground) probe from GGB industries at room temperature. Measurements were done by Dr. Zhiping Feng, Dr. Wael Fathelbab, and Jayesh Nath, ECE, NCSU. The circuit measurements and the performance will be discussed in detail in the results and discussion section.
References:


(7) http://www.microchem.com/product/lor.htm


Bandpass Filter Using Thin – Film Barium Strontium Titanate (BST) Varactors”,

(10) http://www.eagleware.com

(11) http://www.jmicrotechnology.com

(12) http://www.ggb.com


4. RESULTS AND DISCUSSION

4.1 BST thin film structure property relationship

4.1.1 XRD and Low Frequency Electrical measurements

The intent of this work is to illustrate the ability to prepare high quality BST thin devices using both inexpensive materials and processes. Following this methodology, a low deposition temperature is desired since vacuum system design becomes increasingly complex and expensive when high temperature instrumentation is needed. Furthermore, with high temperatures, the persistence of thermal gradients, and the propensity for thermal drift add considerable challenge when attempting to establish a robust large area process.

To identify the optimal preparation conditions for BST thin films on alumina, sets of films were prepared and analyzed where a series of sputtering conditions and post deposition anneals were investigated. The optimization was judged primarily by electrical tunability since this provides the most pertinent indication of film quality.

Percentage tunability (n) is defined as follows:

\[ n = \{100 \times \frac{C_{\text{min V}} - C_{\text{max V}}}{C_{\text{min V}}}\} \]

where \( C_{\text{min V}} \) and \( C_{\text{max V}} \) are the capacitance values at the minimum and maximum applied bias respectively. For the instrument that we used in this work, HP 4192A LF impedance analyzer, the minimum and maximum bias levels correspond to 0 V and 35 V respectively.

The first step in the optimization of the BST thin film growth by RF sputtering was the deposition temperature. Deposition was done at two different temperatures, 130
°C and 300 °C. Increasing deposition temperature to 450 °C did not improve tunability. Hence higher temperature deposition was not pursued.

For reference, Fig. 4.1.1.1 shows an x-ray diffraction pattern of a BST film deposited on alumina at 130 °C and post annealed in air at 650 °C for 1 hour. This represents the smallest thermal budgets used in this study. For comparison, a diffraction pattern is also shown for a BST film deposited at 300 °C and post annealed at 900 °C for 20 hours. This represents the thermal budget for the optimized BST films used in this work.

Fig. 4.1.1.1: XRD scans for BST/ alumina (#) samples after post deposition anneal in air at 650 °C for 1 hour and 900 °C for 20 hours.
A small increase in peak intensity for BST, esp. the (100) and (200) reflections, was observed for the 300 °C deposition, 900 °C and 20 hour anneal consistent with the appreciably larger thermal budget.

The electrical tunability, however, easily identified major differences between samples. Figs. 4.1.1.2 through 4.1.1.4 show the dependency of tuning on deposition temperature, sputtering pressure, and post annealing temperature and time.

Fig. 4.1.1.2: Variation of tunability in BST IDCs optimized for sputtering pressure and BST deposition temperature with $T_{\text{anneal}} = 650$ °C, 1 hour annealing time.
Fig. 4.1.1.2 shows the effect of the change in tunability of the BST IDCs with the deposition temperature and the sputtering pressure. Sputtering pressure was varied from 5 mTorr to 12.5 mTorr in increments of 2.5 mTorr. The maximum tunability was observed for a sputtering pressure of 10 mTorr for both deposition temperatures and the tunability increased with increasing the deposition temperature from 130 °C to 300 °C.

Determining the electrical quality of BST thin films when using IDEs (interdigitated electrodes) is challenging given the difficulty in determining the field distribution inside the dielectric. This is in contrast to the MIM structure where the field is calculated by simply dividing the applied bias by the thickness of the dielectric (since the polarization is in the vertical direction here because of the parallel plate structure). For all the tunability data discussed in this section the applied field in the IDC was estimated by dividing the maximum applied voltage (35 V) by the IDC finger spacing (3 µm) giving a field of approximately 12 V/µm or 120 kV/cm.

Now that the BST deposition temperature and the sputtering pressure was fixed, the next step in the BST optimization process was the determination of the optimum annealing temperature. Annealing was done ex-situ in air between 650 °C and 1000 °C for 1 hour. The effect of annealing temperature on the tunability of BST thin film IDCs is shown in Fig. 4.1.1.3. Tunability increased in a linear fashion from 650 °C (n = 22 %) till 900 °C (n = 29%) and then plummeted as the annealing temperature was increased to 950 °C (n = 19%).
Fig. 4.1.1.3: Variation of tunability in BST interdigitated capacitors optimized for various post deposition annealing temperature for 1 hour at $P_{\text{deposition}}=10 \text{ mTorr}$ and $T_{\text{deposition}}=300 \text{ °C}$

After the annealing temperature was fixed, the optimum annealing time had to be determined. Post deposition annealing time was varied from 1 to 72 hours. The effect of annealing time on the tunability is illustrated in Fig. 4.1.1.4. Tunability of BST IDCs increased with increasing annealing time up to 20 hours and then saturated. For ex. tunability values of 40 % were obtained for $T_{\text{anneal}} = 900 \text{ °C}$, $t = 20 \text{ hours}$ while tunability was $\sim 41\%$ when annealing time was increased to 72 hours.
Fig. 4.1.1.4: Variation of tunability in BST IDCs optimized for various post deposition annealing time at $P_{\text{deposition}}=10\text{mTorr}$, $T_{\text{deposition}}=300\,^{\circ}\text{C}$ and $T_{\text{anneal}}=900\,^{\circ}\text{C}$

XRD scan of the BST / alumina sample annealed at 950 °C for 1 hour revealed 2 unknown peaks at $2\theta = 28.5^\circ$ and $29.5^\circ$ respectively. These peaks are not present in the samples annealed at lower temperatures. Fig. 4.1.1.5 shows XRD scan of the samples deposited under identical conditions but annealed for 1 hour at 900 °C and 950 °C respectively.
From the phase diagram of BaO - SrO – TiO₂ -Al₂O₃ [1], we find that various binary oxide compounds such as 3SrO.Al₂O₃, SrO.Al₂O₃, SrO.2Al₂O₃, and SrO.6Al₂O₃, can be formed in this system above 900 °C. Presumably the chemical modification of BST as well as film cracking is likely to be the cause for this sudden decrease of tunability above 900 °C. However detailed TEM cross sectional analysis of the BST alumina samples are required to confirm this hypothesis.
The optimal conditions, as listed in Table 4.1.1.1, for BST thin film deposition on polycrystalline alumina substrates provided 40% tuning at 35 volts - the limit of our measurement instrumentation.

Table 4.1.1.1: Optimal conditions for BST thin film fabrication

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RF power</td>
<td>300 W</td>
</tr>
<tr>
<td>Sputtering gas (Ar:O₂)</td>
<td>5 :1</td>
</tr>
<tr>
<td>Sputtering pressure</td>
<td>10.0 mTorr</td>
</tr>
<tr>
<td>Deposition temperature</td>
<td>300 °C</td>
</tr>
<tr>
<td>Deposition time</td>
<td>60 min</td>
</tr>
<tr>
<td>Annealing Temperature</td>
<td>900 °C</td>
</tr>
<tr>
<td>Annealing time</td>
<td>20 h</td>
</tr>
</tbody>
</table>

Fig. 4.1.1.6 shows the dielectric characteristics (capacitance and loss tangent vs. voltage) of the optimized BST thin film IDCs (with 3 µm IDE finger width and spacing) on polycrystalline alumina substrates. The capacitance changed from 0.375 pF at 0 V to 0.224 pF at 35 V. Hence a tunability of 40% is obtained at an applied bias of 35 V or an equivalent field of 12 V/µm. The loss tangent (tanδ) is found to be 0.011 and hence a dielectric Q (quality factor) of ~ 100 is obtained at 0 V. This loss tangent value decreases to 0.004 (Q = 250) for an applied bias of 35 V at 1 MHz.
Fig. 4.1.1.6: Dielectric tunability and loss tangent data for the optimized Cu / BST / alumina IDCs. All measurements were performed at 1 MHz at room temperature.

Fig. 4.1.1.7 shows the capacitance and loss tangent versus frequency plot in the MHz - GHz range. As seen, there is very small dispersion in the capacitance characteristics. At 500 MHz the loss tangent value is 0.011 which is the same as what we observe at lower frequency for zero bias. However close to 1 GHz the loss tangent value rises rapidly. This dispersion is probably due to parasitics not accounted for in the circuit model for determining the DUT (device under test) loss at these frequencies. Hence the loss tangents of the BST films can also be considered as frequency independent [2, 3].
Fig. 4.1.1.7: Frequency dependence of the capacitance and loss tangent of the Cu/ BST / alumina IDCs

Interdigitated capacitors (IDCs) are useful components in integrated microwave circuits because of their simplicity of fabrication, low capacitance values, and ease of integration into MW devices [4]. However detailed electrical characterizations of IDCs or planar capacitors are less common, unlike that of the more commonly used MIM or parallel plate capacitor. In this section various electrical characteristics of the BST IDCs with respect to their geometry or configuration are discussed.
Fig. 4.1.1.8: Plot showing the dependence of the capacitance value on the IDC finger spacing. The IDCs had a finger length of 1000 µm and the number of fingers was 10. All values are measured at 0 V bias at 1MHz frequency level.

Fig. 4.1.1.8 shows how the capacitance value of the BST IDCs scales with the finger spacing. The plot shows that for 3 µm finger spacing the capacitance value is 3.86 pF while for 10 µm finger spacing, $C = 1.33$ pF. Thus with increasing the finger spacing the value of the capacitance monotonically decreases.
Fig. 4.1.1.9: Plot showing the dependence of the tunability on the IDC finger width and spacing. The maximum applied bias was 35 V and measurements were done at 1MHz frequency.

Fig. 4.1.1.9 shows the variation in tunability as a function of the IDC finger spacing. The plot shows that for 3 µm finger spacing the dielectric tunability is 40 % while for 10 µm finger spacing the tunability is only 12 %. For both cases the maximum applied bias was 35 V. Again we observe the same trend as in the earlier plot, i.e. the tunability decreases with increasing the IDC finger spacing.
Fig. 4.1.1.10: Plot showing the dependence of the capacitance value on the number of IDC fingers. The IDCs had 10 µm width and spacings and the finger length was 1000 µm. All values are measured at 0 V bias at 1MHz frequency level.

The dependence of the capacitance value on the number of IDC fingers for the same finger width, spacing, and length is shown in Fig. 4.1.1.10. As the number of fingers increases so does the capacitance value.

Figs. 4.1.1.8 - 4.1.1.10 show an interesting trend about the BST thin film IDCs. This effect is because of the way the electric field penetrates the high permittivity BST thin film and the low permittivity alumina substrate due to the different IDC
configuration. Penetration depth is related to finger spacing and decrease of finger spacing result in significant increase of the high permittivity ferroelectric layer contribution for the capacitance and hence tunability. Finger spacing increase results in more field passing through the low permittivity substrate rather than the high permittivity ferroelectric thin film as shown in Fig. 4.1.1.11. Therefore the capacitance value and the tunability increases as the finger spacing is decreased for the IDCs. As the number of fingers is increased, the electric field covers more of the high permittivity ferroelectric layer and hence the capacitance value increases.

![Electric Field lines](image)

Fig. 4.1.1.11: Schematic showing the distribution of the electric field lines in (a) IDE with smaller finger spacing and (b) IDE with larger finger spacing.

Table 4.1.1.2 and Table 4.1.1.3 show the variation of capacitance for different no. of IDE fingers and the variation of capacitance for different halfwidths of IDE fingers as reported by Gevorgian et al. [5].
Table 4.1.1.2: Variation of capacitance for different no. of IDE fingers [5]

<table>
<thead>
<tr>
<th>No. of fingers</th>
<th>5</th>
<th>10</th>
<th>20</th>
<th>50</th>
<th>205</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance(pF)</td>
<td>0.0475</td>
<td>0.0945</td>
<td>0.183</td>
<td>0.453</td>
<td>1.86</td>
</tr>
</tbody>
</table>

Table 4.1.1.3: Variation of capacitance for different finger halfwidth of IDEs [5]

<table>
<thead>
<tr>
<th>Finger halfwidth (µm)</th>
<th>2.5</th>
<th>5.0</th>
<th>10.0</th>
<th>15.0</th>
<th>20.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance (pF)</td>
<td>2.3</td>
<td>3.0</td>
<td>4.0</td>
<td>4.3</td>
<td>5.0</td>
</tr>
</tbody>
</table>

From the table it is clear that the capacitance value increases with increase in the no. of fingers. Also as the finger widths increase, and the finger spacings decrease, the value of capacitance increases. Thus the trends observed here are consistent with the models developed for IDCs by Gevorgian et al. [5] using a partial capacitance, conformal mapping technique.

As mentioned earlier, finding the electrical quality of BST thin films in IDC is not as straightforward as MIMs, given the difficulty in determining the field distribution inside the dielectric. Furthermore, the µm range finger spacing consistent with very small value capacitors makes the application of very high fields difficult given the voltage limitations common to impedance measuring instrumentation. As such, direct comparison to more thoroughly characterized MIM structures is difficult. In this study, we have
attempted to address this issue by preparing BST films using identical deposition parameters, and the same annealing temperatures in MIM configuration.

Specifically, we used the process developed by Laughlin et al [6] for preparing BST thin films directly on Cu foils since this allows access to 900 °C annealing range. Furthermore, the Cu substrate provides a favorable comparison to the Cu IDEs deposited on the BST/ alumina stacks. Also the BST thin films were prepared by the same RF magnetron sputtering process for both cases. In Fig. 4.1.1.12 we compare tunability – electric field and dielectric loss- electric field plot for a BST parallel plate capacitor (MIM) with data from a BST / alumina planar capacitor (IDC). The field for the MIM capacitor was calculated by assuming parallel plate configuration, while the field for the IDC was estimated by dividing the applied voltage by IDE finger spacing of 3 µm. The C-E traces are nearly identical for the overlapping field range. In reference to tunability, this suggests that BST prepared on alumina is of similar quality, and if smaller finger spacings or larger voltages were applied, greater tuning would be observed.

Many authors have suggested that MIM configuration offers better control over tuning voltages than IDC geometry [7, 8]. Here we demonstrate that under the same applied electric field, subject to our approximation of field in an IDC, both MIMs and IDCs tune in an identical way.
Fig. 4.1.1.12: Tunability – field traces for MIM (●) and IDE (○) BST film capacitors prepared using the same sputtering conditions and post annealing temperature.

Note however that the loss tangent for the IDC is lower. The value of the capacitor in the IDC configuration is below 1 pF, and we note that this value is approaching the edge of the range where an HP 4192A provides high accuracy loss tangent values. When the same structures were measured using the Agilent E 4991 A network analyzer, loss tangents were comparable to the MIM material as shown in Fig. 4.1.1.7.
4.1.2 AFM analysis

Fig. 4.1.2.1 shows an AFM image of a BST (600nm) / alumina sample deposited at 300 °C and then annealed in air at 700 °C for 1 hour. The film show grains having an average grain size of 40 nm. Grain size was determined using a linear intercept method. The rms (root mean square) surface roughness was determined over a 1x1 µm² area of the films. The rms surface roughness is a measure of the peak-to-valley distance between the grain peaks and the underlying continuous film. A rms surface roughness of 3.5 nm was observed for these BST thin films.

Fig. 4.1.2.1 AFM image (1µm x 1µm scan) of BST sample deposited at 300 °C and annealed at 700 °C for 1 hour in air.
Fig. 4.1.2.2 shows an AFM image of a BST (600nm) / alumina sample deposited at 300 °C and then annealed in air at 800 °C for 1 hour. The average grain size was 45 nm. An rms roughness of 4.5 nm was observed for these films for a 1x 1 μm$^2$ scan.

Fig. 4.1.2.2 AFM image (1μm x 1μm scan) of BST sample deposited at 300 °C and then annealed at 800 °C for 1 hour in air.

AFM image of BST sample deposited at 300 °C and then annealed in air at 900 °C for 1 hour is shown in Fig. 4.1.2.3. Average grain size was about 75 nm and a rms surface roughness of 3.8 nm was observed for these BST films.
The grain sizes of these BST films are comparable to those reported in the open literature for BST thin films deposited by RF sputtering [6, 9]. In contrast the rms surface roughness of the BST thin films is nearly an order of magnitude better than those reported for sputtered BST thin films [9-11]. Such high surface smoothness of BST thin films is critical for achieving an abrupt, low loss interface between the BST thin film and the metal top electrode in microwave circuits [4].

The micrographs of the BST thin films exhibit dense, well crystallized, void and crack free microstructure composed of multigrains that are randomly oriented. Increase in grain size was observed for the BST thin films annealed at higher temperature. These results suggest that the increase in tunability of the BST thin film IDCs that are deposited at 300 °C and then annealed at 700 °C for 1 hour compared to the ones that were deposited at 300 °C and then annealed at 900 °C for 1 hour are due to the “size effects”
that are observed in many ferroelectric thin films [12, 13]. According to this effect thin film ferroelectrics show a decrease in dielectric permittivity with decrease in grain size. This decrease has been linked by many authors to the presence of a low permittivity layer at the grain boundaries or electrode/film/substrate interfaces [14].
4.1.3 Leakage current analysis

The leakage current of a dielectric thin film is a measure of the electrical quality of the film and is directly correlated to the resistive loss mechanisms [4, 14]. A leakage current measurement taken from the Cu / Cr / BST / alumina IDC is shown in Fig. 4.1.3.1. This BST was sputtered at 300 °C on alumina and then annealed at 900 °C for 20 hours.

![Graph showing leakage current vs. applied field for BST thin film IDCs.](image)

Fig. 4.1.3.1: Leakage current vs. applied field for BST thin film IDCs.

As shown in Fig. 4.1.3.1, for an applied field of 10 V/µm the leakage current is 1.39 x 10^-10 A. For an IDC configuration the calculation of the area of the electrodes is not as straightforward as MIMs because of its geometry. Hence the plot shows the
leakage current (A) rather than the conventional leakage current density (A/cm²). However the author estimated the IDC area to be roughly 1.3 x 10⁻⁴ cm² which gives a leakage current density of 1.0 x 10⁻⁶ A / cm² for an electric field of 10 V/ µm. These leakage current values are consistent with several literature examples where BST overall quality is well established.

Some authors report on a top electrode anneal that is necessary to achieve low dielectric loss and low leakage current values for BST based capacitors [12, 15, 16]. All such reports are concerned with BST MIM capacitors which usually incorporate noble metallization such as Pt or Au. The top electrode anneal is done after top electrode deposition and consists of annealing the BST MIM samples in air at ~ 500 °C for 30 minutes.

In this work thin layer of Cr (20nm) was used as an adhesion layer for Cu top electrode in the BST thin film IDC configuration. Here a top electrode annealing process is rather challenging to implement since it is difficult to preserve Cr integrity during post-deposition anneals. From the Richardson – Ellingham diagram for oxides [17] we find that pO₂ (partial pressure of Oxygen) required to prevent the oxidation of Cr to Cr₂O₃ is in the order of 10⁻³⁶ to 10⁻³⁴ Torr at T = 500 - 600 °C, and such reducing conditions are difficult to implement. Note that regardless of the top electrode anneal, low dielectric loss (0.011 @ 1MHz at zero bias) and low leakage current (J= 1.0 x 10⁻⁶ A / cm² at 10 V/ µm) values of BST thin film IDCs are observed.
4.1.4 Microwave characterization of BST IDCs

This chapter deals with characterization and modeling of discrete BST varactors at MW frequencies. The low frequency measurements of the BST thin film IDCs have been presented previously. The high frequency measurements are important for accurate estimation of the MW circuit performance at GHz frequencies.

The quality factor (Q) is used to characterize losses in lumped circuit elements. Quality factor can be defined as the ratio of stored energy to the average energy dissipated in the system per cycle. At low frequencies the Q is simply the inverse of the dielectric loss since the metallization loss can be ignored at such frequencies. However for MW frequencies, finding the device Q is not so straightforward and is a function of both the dielectric loss and the metallization loss as given below [2, 18]:

\[
\frac{1}{Q_t} = \frac{1}{Q_{BST}} + \frac{1}{Q_m} = (\tan \delta + \omega C_p R_s)
\]

where \( Q_t \) is the total device quality factor, \( Q_{BST} \) is dielectric (BST) quality factor, \( Q_m \) is the quality factor contribution from the metallization, \( \tan \delta \) is the dielectric loss, \( \omega \) is the angular frequency, \( C_p \) is the capacitor value, and \( R_s \) is the series resistance.

Fig. 4.1.4.1 shows the calculated dependence of the overall quality factor as a function of frequency based on the above equation. The individual contributions of the dielectric and the metallization to the overall Q are also highlighted. Here values of \( C_p = 1 \) pF, \( \tan \delta = 0.010 \), \( R_s = 0.03 \) \( \Omega \) are assumed. It can be assumed that \( Q_{BST} \) remains constant over the frequency range of interest [3]. From the plot it is clear that metallization Q, i.e. \( Q_m \), dominates at high frequencies and has a greater effect on the overall device Q. Therefore, focus must be on \( R_s \) in order to increase the total Q of MW devices.
Here $C_p = 1 \text{ pF}, \tan \delta = 0.010, R_s = 0.03 \Omega$ is assumed.

One way to reduce $R_s$ is to increase the electrode thickness, $t$, as $R_s$ is inversely proportional to $t$, according to Ohm’s law. However, there are difficulties associated with increasing the electrode thickness from a microfabrication point of view. Etching or lift-off of metals becomes increasingly challenging as the metallization thickness goes up. The other way is to decrease the resistivity of the metal or in other words use the metal with the highest electrical conductivity. To that end, Cu was used as the top electrode material in this work since it has the highest conductivity of all base metals.
S - parameters are normally used to characterize high frequency networks, where simple models valid at lower frequencies cannot be applied [4, 19]. S – parameters (Scattering Parameters) are the reflection and transmission coefficients between the incident and reflection waves as shown in Fig. 4.1.4.2. The behavior of a device under linear conditions at microwave frequency range can be described by such parameters. Each parameter is usually characterized by magnitude, decibel and phase. The expression in decibel is 20 log (S$_{ij}$) because s-parameters are voltage ratios of the waves.

![Diagram of S parameters](image)

Fig. 4.1.4.2: A 2 port network showing the various S parameters.

The various S parameters are S$_{11}$, S$_{21}$, S$_{12}$, and S$_{22}$. They are defined below:

- S$_{11}$: Input reflection coefficient of 50 W terminated output.
- S$_{21}$: Forward transmission coefficient of 50 W terminated output.
- S$_{12}$: Reverse transmission coefficient of 50 W terminated input.
- S$_{22}$: Output reflection coefficient of 50 W terminated input.
The microwave properties (1 to 26.5 GHz) of the BST thin film IDCs were measured in a one-port configuration using a Hewlett Packard 8510 C Network Analyzer. The IDCs had 15 fingers which had 3 µm width and spacing and were 50 µm long. The IDC [Cu (500 nm) / Cr (20 nm) / BST (600 nm) / alumina] had a capacitance value of 0.6 pF. Details of the testing procedure are discussed in section 3.5.1.

For any type of passive circuits represented by admittance or impedance the quality factor (Q) can be defined as follows:

\[
Q = \left| \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \right|
\]

where \(Z_{11}\) is the impedance of the circuit and \(\text{Im}\) and \(\text{Re}\) are the imaginary and the real parts of \(Z_{11}\) respectively. Reflection (\(S_{11}\)) data was collected and treated using a model which takes into account series resistance (Rs), inductance (Ls) and a parallel resistor (Rp) - capacitor (Cp) circuit [4]. The model is illustrated in Fig. 4.1.4.3. This allowed determination of the device quality factor which includes contributions from the dielectric and the metallization.

![Lumped element model for BST IDCs at GHz frequencies.](image)
The quality factors (Q) for the BST IDCs is shown in Fig. 4.14.. From the plot we see that devices show high device Q values (100 - 120) at low frequencies (below 1 GHz) and the Q factor decreases asymptotically as the frequency increases and a Q value of ~ 30 is obtained at 26.5 GHz. The low frequency Q value is dominated by the dielectric loss and is in close agreement with the data in section 4.1.1. Metallization losses begin to dominate at MW frequencies and this causes the Q value to decrease to 30 at the high end of the frequency spectrum.

![Quality factor vs. frequency plot for BST IDCs.](image)

Fig. 4.1.4.4: Quality factor vs. frequency plot for BST IDCs.
For ferroelectric thin film MW devices the two most important parameters are the
dielectric tunability and the quality factor (Q value). We compare the present data with
several recent literature examples in Table 4.1.4.1.

Table 4.1.4.1: Literature values for tunability, tuning field, device quality factor,
metallization and substrate used for BST based MW devices. In all cases, the tuning field
is estimated by dividing the applied voltage by the IDE finger spacing.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tunability (%)</td>
<td>40</td>
<td>45</td>
<td>64</td>
<td>40</td>
<td>65</td>
<td>26</td>
</tr>
<tr>
<td>Electric Field (V/µm)</td>
<td>12</td>
<td>90</td>
<td>35</td>
<td>13.3</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>Q (@ n GHz) C =0.6pF</td>
<td>30 (26)</td>
<td>&gt;20 (24)</td>
<td>28 (2.4)</td>
<td>9 (9)</td>
<td>4 (20)</td>
<td>-</td>
</tr>
<tr>
<td>Metallization</td>
<td>Cu/Cr</td>
<td>Au</td>
<td>Au/Cu/Cr</td>
<td>Au/Cr</td>
<td>Au/Ag</td>
<td>Au</td>
</tr>
<tr>
<td>Substrate</td>
<td>Alumina</td>
<td>Sapphire</td>
<td>Sapphire</td>
<td>MgO</td>
<td>MgO/LAO</td>
<td>LAO</td>
</tr>
</tbody>
</table>

This table illustrates that this base metal top electrode (Cu), polycrystalline
ferroelectric (BST) thin film, ceramic substrate (alumina)-based technology is
comparable, and in some cases superior to conventional noble metal electrode, epitaxial
thin film BST, single crystalline substrate technologies.
4.2 Cu thin film characterization

Base metal Cu has been used in this work as the top electrode of choice since it is inexpensive, readily available and has the highest conductivity among base metals. Keeping in mind that metallization losses are very important at MW frequencies it is imperative to obtain low resistivity Cu to minimize ESR (Equivalent Series Resistance) in MW devices.

Fig. 4.2.1: Plot of resistivity of thermally evaporated Cu vs. the deposition pressure.

\[ \rho_{\text{Cu}} = 1.7 \, \mu\Omega \cdot \text{cm} \]
The resistivity of as deposited thermally evaporated Cu as a function of the deposition pressure is shown in Fig. 4.2.1. The electrical resistivity (\(\rho\)) of bulk Cu is 1.7 \(\mu\Omega\) cm at room temperature. At a deposition pressure of \(1.0 \times 10^{-5}\) torr, \(\rho_{\text{Cu}} = 3.7 \mu\Omega\) cm is obtained for as deposited thermally evaporated Cu thin films. This value is about 46% of that of bulk conductivity of Cu. As the deposition pressure decreased to \(5.0 \times 10^{-8}\) torr, \(\rho_{\text{Cu}} = 2.3 \mu\Omega\) cm for as deposited Cu thin films is obtained. This value is about 75% of that of bulk conductivity of Cu. Also the resistivity value tends to saturate as the deposition pressure is lowered as evident from the plot.

The chemical purity of evaporated films mainly depends on three factors: (a) impurities that are initially present in the source (b) impurities that contaminate the source from the crucible, heater or other support materials and (c) impurities that originate from the residual gases present in the vacuum system [25, 26]. For this work the first two factors can be considered constant under all deposition conditions. The improvement in the conductivity of the as deposited Cu thin films from 46% to 75% of the bulk value can be explained by Matthiessen’s rule for electrical conduction in metal thin films [25].

This rule was originally proposed for bulk metals but is valid for metal thin films too. It states that various electron scattering states processes that contribute to the total resistivity of a metal is given by:

\[
\rho_T = \rho_{\text{th}} + \rho_i + \rho_d
\]

where \(\rho_T\) is the total resistivity of the metal, \(\rho_{\text{th}}, \rho_i,\) and \(\rho_d\) are the thermal, impurity and the defect resistivities respectively. Impurity atoms, incorporated in the metal thin films, locally disrupt the periodic electric potential of the lattice and leads to electron scattering
and therefore higher resistivity values. Here as the deposition pressure is decreased the presence of gaseous impurities such as oxygen and nitrogen decreases and hence $\rho_i$ (impurity resistivity) contribution to the total resistivity decreases. However grain size plays an important role in determining the electrical resistivity of metals, since grain boundaries act as electron scattering centers. Grain sizes in bulk Cu are usually in the tens of $\mu$m range, whereas grain sizes in Cu thin film are usually in the tens – hundreds of nm range [25]. Thus the metal microstructure in thin films poses an inherent limitation to the electrical resistivity that can be achieved.

Hence we see a dramatic improvement in the conductivity value of Cu thin films, as the deposition pressure is lowered, that is crucial for minimizing metallization losses in the MW devices. Thus we see that a clean deposition system is critical for obtaining low resistivity Cu and thus better metallization which will have a profound influence on the overall device quality.
4.3 Microwave Device Results

4.3.1 Microwave filter

Microwave filters are widely used in satellite, radar, and mobile communication systems [4, 27-29]. Electrical filters are used for frequency-selective transmission, which enables them to transmit energy in one or more passbands and to attenuate energy in one or more stopbands. In a LC resonant circuit, a tunable capacitor can be used to tune the resonant frequency. This simple principle can be utilized in filters where capacitance tuning can change the frequency response of the filter.

Multipole filters composed of mutually coupled resonators are commonly used in microwave circuits [27, 30]. Usually multipole filter can be constructed as a combination of single resonators. In a N pole Chebyshev filter, a chain of N resonators are used in which there is coupling between the neighboring resonators. The 1st and the Nth resonators are coupled to an external port, which is a microstrip line in this case. In such a design the steepness of the filter skirts with increasing N upto a value which is determined by the Q of the resonator [30]. However higher the number of resonators, more is the insertion loss of the filter. In this work the value of N was chosen to be 3 for the sake of simplicity of design and ease of fabrication.

Here a 3rd order combline bandpass Chebyshev filter was designed with center frequency of 1.75 GHz and 3 dB passband of 20 % of the center frequency [31]. For a filter, one can define a frequency tunability factor as the ratio of the change in center frequency with applied bias to the original center frequency.

The filter was designed using the MFilter synthesis tool in Genesys suite of EDA from Eagleware. Though all the filters discussed in this section had the same design, they
were fabricated in different ways as far the metallization is concerned. The measurement results with respect to the different filter architecture are discussed below.

4.3.1.1 Series - 1 Microwave Filter

In the early stages of the filter fabrication (Series - 1 filters), top metallization consisted of sputtered Cr (20nm) as an adhesion layer and sputtered Cu (500nm). Backside metallization stack was as follows: (a) sputtered Cr (20 nm) and (b) sputtered Cu (1000 nm) which acts as the ground plane. Resistivity (ρ) of the DC sputtered Cu was 4.2 µΩ-cm. After the fabrication of the filter on the alumina substrate the filter was assembled on a high frequency laminate using conductive epoxy. The layer stack up of the Series – 1 filter is shown in Fig. 4.3.1.1.1.

For Series - 1 filters a “via” or “through wafer interconnect” process was not used and the top Cu surface of the FR - 4 substrate board served as the common ground plane. Thus the ground connections at the end of the resonators were made by “ground-wrapping” using conductive epoxy (ρ < 0.001 Ω-cm). The input and output connections
to the filter was made using a J-Micro CPW – to - Microstrip adaptor. The adaptors were wire bonded to the input and output feed lines using a ball bonder. The detailed filter architecture is shown in Fig. 4.3.1.1.2.

Fig. 4.3.1.1.2: Schematic of the Series - 1 Microwave filter architecture showing the “ground wrapping” technology.

The BST varactors at the end of the resonators had a capacitance value of 1.16 pF at 1 MHz at zero bias. This value decreased to 1.02 pF at 35 V. Thus a tuning of 12% was obtained for an applied field of 5.5 V / µm (since the finger spacing in the IDC was 6 µm). The dielectric loss (tanδ) decreased from 0.012 at 0 V to 0.006 at 35 V at a frequency of 1 MHz. A representative CV plot of the BST thin film IDC used in the filter circuit is shown in Fig. 4.3.1.1.3.
Fig. 4.3.1.1.3: CV plot for BST thin film IDCs used in the filter circuit. Measurements done at 1 MHz.

The microwave characteristics of the Series - 1 MW filter can be seen in Fig. 4.3.1.1.4. The filter is centered at 1.7 GHz with a bandwidth of 400 MHz. In other words the filter will allow signals to pass through in the 1.5 to 1.9 GHz range at zero bias. Similarly for an applied bias of 125 V, where the center frequency is 2.0 GHz, the filter will allow signals to pass through in the 1.8 GHz to 2.2 GHz range. It should be noted that the measured 1 dB bandwidth of the filter was 400 MHz compared to the designed value of 300 MHz. Broadening was presumably due to parasitics that were not accounted
This difference can be attributed to the metallization losses and also the parasitics associated with the filter assembly.

![Graph showing measured insertion loss of the Series-1 filter vs. frequency as a function of applied bias.](image)  

**Fig. 4.3.1.1.4:** Measured Insertion loss of the Series-1 filter vs. frequency as a function of applied bias.

The center frequency of the filter tuned from 1.7 GHz at zero bias to 2.0 GHz at 125 V bias at room temperature. The tuning thus achieved was 18 % and the filter is capable of covering the GPS and the GSM bands at 1800 and 1900 MHz respectively [4, 30]. Frequency tuning of the resonator is proportional to the capacitance tuning of the BST varactor used in the IDC configuration in the filter. The mid-band insertion loss was 10.5 dB at 0 V and this decreased to 8.2 dB at 125 V bias. The decrease in insertion loss
with increasing bias is in part due to increased Q factor of the BST varactors and also in part due to improved matching that results due to a change in capacitance [32].

The return loss of the filter was better than 10 dB at all bias voltages as shown in Fig. 4.3.1.1.5. This indicates that the impedance of the circuit does not vary strongly with bias and is close to 50 Ω under all bias conditions.

Fig. 4.3.1.1.5: Measured Return loss of the Series - 1 filter vs. frequency as a function of applied bias.

One of the prime requirements for a MW device is low power consumption. The total leakage current drawn by all three BST capacitors for different bias voltages and the corresponding power consumed is listed in Table 4.3.1.1.1. The total DC power
consumer by the filter was less than 6 µW over the entire range of bias voltage investigated.

Table 4.3.1.1.1: Leakage current vs. bias for Series - 1 filters.

<table>
<thead>
<tr>
<th>Bias Voltage (V)</th>
<th>Leakage current(nA)</th>
<th>Power consumed (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>22.84</td>
<td>0.57</td>
</tr>
<tr>
<td>50</td>
<td>28.36</td>
<td>1.42</td>
</tr>
<tr>
<td>75</td>
<td>36.68</td>
<td>2.75</td>
</tr>
<tr>
<td>100</td>
<td>43.96</td>
<td>4.40</td>
</tr>
<tr>
<td>125</td>
<td>45.36</td>
<td>5.67</td>
</tr>
</tbody>
</table>

The rather high insertion loss of the Series - 1 filter is primarily due limited thickness of the electrode metal (0.5 µm) and also due to the higher resistivity or lower conductivity of sputtered Cu, which is about 40 % of that of bulk Cu. The skin depth of Cu metal at the frequency of operation of the filter is 1.34 µm and 3 skin depth of metal will ensure that 95% of the current flows in it; thus there is considerable room for improvement as far as the insertion loss of the device is concerned. In the next section we will demonstrate how the insertion loss of the filter can be improved by improving the metallization, by increasing the thickness of the metal and by improving upon the resistivity of the metal itself, and by improvement in the filter design.
4.3.1.2 Series-2 Microwave Filter

The next improvement in the fabrication of the MW filter was in the top metallization technique. Instead of using DC sputtering method to fabricate Cu top electrodes, a thermal evaporation technique was used. The advantages of using thermal evaporation vis - a - vis sputtering is discussed in section 1.8.1.

The layer stack up of the Series - 2 filter is shown in Fig. 4.3.1.2.1. The top electrode was 1 µm of thermally evaporated Cu. Resistivity ($\rho$) of the thermally evaporated Cu was 2.3 $\mu\Omega$-cm. The filter architecture was essentially the same as in Series-1 filters (see Fig. 4.3.1.1.2), i.e. the filter was glued onto a FR - 4 substrate and a “ground wrapping” technique was used.

![Layer stack up of Series - 2 filters.](image)

A photograph of the assembled filter on the FR - 4 laminate is shown in Fig. 4.3.1.2.2. The position of the BST thin film IDC at the end of the each of the three resonators is highlighted.
The MW characteristics of the 3rd order filter can be seen in Figs. 4.3.1.2.3 and 4.3.1.2.4. The filter is centered at 1.60 GHz with an insertion loss of 6.55 dB as seen from the $S_{21}$ vs. frequency plot in Fig. 4.3.1.2.3. The filter was designed to have a center frequency of 1.75 GHz. This downward shift in the center frequency can be explained by a slight increase in the resonator length due to the use of the epoxy for “ground-wrapping”. The BST thin film varactors at the end of the resonators had a value of 1.1 pF,
dielectric Q of ~ 100 at 1 MHz and had a device Q factor of ~ 20 in the 1-2 GHz range at zero bias.

Fig. 4.3.1.2.3: Measured Insertion loss of the Series - 2 filter vs. frequency as a function of applied bias.

The center frequency of the filter tuned from 1.60 GHz at zero bias to 2.00 GHz at 200 V bias as seen in the plot above. For an applied bias of 200V, the BST varactor at the end of the resonator tuned 50% and this lead to a frequency tuning of 25 % for the filter. Similar to the filter described in the earlier section, this filter is also capable of covering the GPS (1800 MHz) and the GSM (1900 MHz) bands. The mid-band insertion loss was 6.55 dB at zero bias and this decreased to 4.3 dB at 200 V bias.
The return loss of the filter was better than 10 dB for all bias levels as shown in Fig. 4.3.1.2.4.

Fig. 4.3.1.2.4: Measured Return loss of the Series-2 filter vs. frequency as a function of applied bias.

A comparison of the measured and simulated zero bias filter response is shown in Fig. 4.3.1.2.5. The measured data closely agrees with the simulated data and the slight discrepancy at the high end of the frequency range can be attributed to parasitic inductances and capacitances which become substantial at GHz frequencies. For the sake of clarity, the comparison is shown only for two ends of the bias range, but the model holds ground at all bias voltages.
Fig. 4.3.1.2.5: Plot showing the comparison of modeled (broken lines) vs. measured data (solid lines) at 0 V and 200 V bias for the Series - 2 filter.

A summary of the filter performance is given in Table 4.3.1.2.1. It shows the frequency shift, insertion loss, and return loss of the filter as a function of the applied bias.
Table 4.3.1.2.1: Summary of Series - 2 filter data as a function of applied bias.

<table>
<thead>
<tr>
<th>Bias Voltage (V)</th>
<th>Center Frequency (GHz)</th>
<th>Insertion Loss (dB)</th>
<th>Return Loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.60</td>
<td>6.50</td>
<td>10.00</td>
</tr>
<tr>
<td>25</td>
<td>1.64</td>
<td>6.13</td>
<td>10.30</td>
</tr>
<tr>
<td>50</td>
<td>1.74</td>
<td>5.80</td>
<td>11.00</td>
</tr>
<tr>
<td>75</td>
<td>1.80</td>
<td>5.33</td>
<td>12.00</td>
</tr>
<tr>
<td>100</td>
<td>1.84</td>
<td>4.90</td>
<td>12.35</td>
</tr>
<tr>
<td>125</td>
<td>1.89</td>
<td>4.70</td>
<td>12.94</td>
</tr>
<tr>
<td>150</td>
<td>1.92</td>
<td>4.45</td>
<td>13.40</td>
</tr>
<tr>
<td>175</td>
<td>1.95</td>
<td>4.37</td>
<td>13.90</td>
</tr>
<tr>
<td>200</td>
<td>2.00</td>
<td>4.30</td>
<td>14.70</td>
</tr>
</tbody>
</table>

The insertion loss of the Series - 2 filter at zero bias is 6.5 dB compared to 10.5 dB for the Series - 1 filter. This dramatic improvement of 4 dB in the insertion loss is primarily due to the following reasons: (a) thicker metallization (1 µm of evaporated Cu for Series - 2 filters compared to 0.5 µm of sputtered Cu for the Series - 1 filters) (b) improvement in the electrical conductivity of the deposited Cu films (conductivity of thermally evaporated Cu is 75% that of bulk Cu whereas conductivity of sputtered Cu is only 40% that of bulk Cu).

Note that the basic filter architecture is the same in both cases and an epoxy “ground wrapping” technique is used in both cases. The use of a “via process” and
elimination of wirebonds at the input and output of the filter should enable reduction of parasitics and further reduction in the insertion loss. This will be demonstrated in the next section for the Series-3 filters.

4.3.1.3 Series-3 Microwave Filters

For the Series-3 filters, via or through wafer interconnect process was introduced. The backside metallization consisted of sputtered Cr (20 nm as adhesion layer) and Cu (100 nm as seed layer), and electroplated 10 µm thick Cu. Electrical contact from the transmission lines on the top side of the filter to the bottom ground plane Cu was made through the vias and this process eliminated the need for “ground wrapping” technique and the wire bonding for the J-Micro CPW-to-Microstrip adaptor. A little amount of Ag epoxy was used to reinforce the contact through the vias. However the top metallization was still the same as in Series-2 filters, i.e., 1 µm thermally evaporated Cu with resistivity (\(\rho\)) of 2.3 \(\mu\Omega\)-cm. The layer stack up of the Series-3 filter is shown in Fig. 4.3.1.3.1.

![Layer stack up of Series-3 filters](image)

**Fig. 4.3.1.3.1**: Layer stack up of Series - 3 filters.
The new and improved filter architecture using electroplated via and backside metallization is shown in Fig. 4.3.1.3.2. This new architecture for the Series - 3 filters allowed “on chip” testing since the MW test probes could be directly placed on the probe pads. This is in marked contrast to the Series - 1 and Series - 2 filters which involved wire bonds and J-Micro CPW-to-Microstrip adaptors for testing. This eliminated unwanted resistance parasitics and resulted in improved insertion loss of the filter.

Fig. 4.3.1.3.2: Schematic of the Series - 3 filter architecture showing the via technology.

A photograph of the Series - 3 filter showing the location of the BST IDCs at the end of the resonators, the probe pads and the vias is shown in Fig. 4.3.1.3.3. Now the filter could be directly tested “on chip” because of the improved design.
Fig. 4.3.1.3.3: Photograph of the Series - 3 filter showing the location of the BST IDC varactors at the end of the resonators, the probe pads and the vias.

The center frequency of the filter was 1.85 GHz at zero bias and tuned to 2.05 GHz for 125 V DC bias as seen in the plot Fig. 4.3.1.3.4. The slight upward shift in the center frequency is due to the fact that the BST thin film varactors at the end of the resonators had a slightly lower value than the design value of 1.1 pF. The filter is centered at 1.85 GHz with a bandwidth of 400 MHz. The mid-band insertion loss was 4.5 dB at zero bias and this decreased to 3.5 dB at 125 V bias. This improvement in the insertion loss with applied bias is again due to higher dielectric quality factor of BST varactors at the end of the resonators and improved impedance matching with changing capacitance.
The measured return loss of the filter was better than 9 dB for all bias levels as shown in Fig. 4.3.1.3.5.
Fig. 4.3.1.3.5: Measured Return loss of the Series - 3 filter vs. frequency as a function of applied bias.

The insertion loss of the Series - 3 filter at zero bias is 4.5 dB compared to 6.5 dB for the Series - 2 filter. Thus an improvement of 2 dB in the insertion loss has been achieved due to better integrated architecture. The “ground wrapping” technique, wire bonds and the CPW – to -Microstrip adapter at the input and output introduces additional losses in the device. In this integrated process they were eliminated leading to further improvement in the filter insertion loss.

Though tuning voltages for the filters are rather high compared to parallel plate BST varactors or MIMs, the fabrication process for the IDC integrated circuit is simpler
and inexpensive. It should also be noted that such high voltages can be readily achieved in non-portable devices using DC to DC converters at low capital cost [33].
4.3.1.4 IMD (Intermodulation Distortion) results

One of the most attractive features of any frequency tunable devices is their ability to transmit high levels of microwave power without any unacceptable signal degradation due to generation of intermodulation distortion (IMD) [4, 26, 34]. For transmitter applications, the intermodulation generated by the nonlinearity of the MW filters should be suppressed to permit the use of high input power.

When two input signals with frequencies $\omega_1$ and $\omega_2$ are applied to a filter, we get only two output signals with frequencies $\omega_1$ and $\omega_2$, provided that the filter has no nonlinearity. These output signals are called fundamental signals.

If the filter does have some nonlinearity, however, we get various output signals with frequencies that differ from $\omega_1$ and $\omega_2$ in addition to the fundamental signals. The additional signals, which are generated by intermodulation caused by the nonlinearity of the filter, include signals with frequencies of $n\omega_1$ and $n\omega_2$ {harmonics}, $(\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$ {second order IMD}, and $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ {third order IMD}. In particular, third-order intermodulation (IM3) is a serious problem because it produces spurious signals within the passband of the filters. A summary of the different types of distortion caused by IMD and the harmonics generated is schematically shown in Fig. 4.3.1.4.1.

A convenient quantitative measure of nonlinearity is the third-order intercept, IP3, which is defined as the input power at which extrapolations of the fundamental and IM3 signal curves intersect [31, 32]. High IP3 values indicate low nonlinearity and better powerhandling capability of any passive device.
Fig. 4.3.1.4.1: Intermodulation distortion caused by signal transmission in non linear components [4].

The linearity of the tunable filters fabricated using BST thin film IDCs were characterized using a conventional two-tone intermodulation test while ensuring that passive intermodulation of the test set was negligible [32]. Results of the two-tone test are shown in Fig. 4.3.1.4.2 with a third-order intercept point (IP3) of 38 dBm. Note that the relatively higher tuning voltages required for IDCs compared to MIMs renders them insensitive to a large swing in RF voltages and, therefore, leads to improved linearity, thus affording a much higher IP3.
Tunable devices are intrinsically non linear and therefore susceptible to the generation of IMD and harmonic signals. The measurements performed on the filters indicate that the filters are capable of providing RF tuning at high RF signal levels while maintaining low signal distortion, so as not to impair system performance, as evident from the high IP3 value of 38 dBm.
4.3.2 Microwave Phase Shifter

The capacitive tuning ability of ferroelectric BST thin film technology is commonly employed in phase shifters. Phase shifting devices have various applications in wireless communications systems, e.g., “smart antennas” based on phased arrays [4].

A MW phase shifter was designed for X-band (8 - 12 GHz) to provide adequate phase shift with low loss at 10 GHz. Details of the design and the fabrication process are described elsewhere. A detailed photograph of the MW phase shifter using Cu transmission lines on BST thin film / alumina substrate is shown in Fig. 4.3.2.1.

Fig. 4.3.2.1: Photograph of four X-band phase shifters showing the position of the BST IDC varactors.
The measurement results from the X-Band phase shifter circuit are presented in Figs. 4.3.2.2-4.3.2.5.

![Graph showing differential phase shift as a function of applied bias at 10 GHz.](image)

**Fig. 4.3.2.2:** Differential phase shift as a function of applied bias at 10 GHz.

The differential phase shift with respect to applied voltage is plotted in Fig. 4.3.2.2. The circuit shows a modest phase shift of 18° at 10 GHz for an applied bias of 130 V.

The next plot (Fig. 4.3.2.3) shows the insertion loss of the phase shifter circuit at different frequency levels for zero bias. The insertion loss is only 1.1 dB at 10 GHz and the maximum insertion loss is 2.2 dB at 15 GHz at 0 V.
Fig. 4.3.2.3: $S_{21}$ characteristics of the BST thin film IDC loaded phase shifter as a function of frequency of operation at zero bias.

Fig. 4.3.2.4 shows the insertion loss as a function of applied bias at a frequency of 10 GHz. At zero bias the insertion loss is 1.1 dB which decreases to 0.7 dB with an applied bias of 130 V. Thus the insertion loss variation over all the bias states is less than 0.5 dB in the same frequency range.
Fig. 4.3.2.4: $S_{21}$ characteristics of the BST thin film IDC loaded phase shifter as a function of applied bias at 10 GHz.

The return loss is higher than 19 dB at 0 V in the frequency range of interest as evident in Fig. 4.3.2.5.
Fig. 4.3.2.5: $S_{11}$ characteristics of the microwave phase shifter as a function of frequency at zero bias.

The measured insertion loss for this phase shifter, 1.1 dB at 10 GHz, is among the lowest reported for a ferroelectric thin film integrated MW phase shifter [4, 7, 8, 20, 21, 35]. A common way to define the performance of a phase shifter is the figure of merit, which is defined as the differential phase shift divided by the maximum insertion loss for zero voltage state, at the operating frequency [4]. For the phase shifter reported in this work a figure of merit of 17 °/dB at 10 GHz is obtained. The best ever phase shifter
performance has been reported by York et al. at UCSB [10]. They have reported a figure of merit of 93 °/dB at 6.3 GHz and 87 °/dB at 8.5 GHz. This circuit was capable of a 0 - 250° continuous phase shift at 10 GHz with an insertion loss of 3.1 dB at 10 GHz. Note that these phase shifters used BST thin film MIM configuration in which a tuning ratio of 2.5:1 or higher can be routinely achieved at voltage levels of ~20V. Because of the MIM configuration in these circuits, higher electric fields could be readily applied leading to more capacitance tuning and hence higher phase shifts. In our designs we have chosen a planar capacitor configuration, for ease of fabrication and low cost, in which the IDC finger spacing was 6 µm. It is expected that with smaller finger spacing, higher tuning and subsequently higher phase shift can be obtained while still maintaining low insertion loss. Thus the phase shifter performance looks very promising and with some modifications in the design and the fabrication process, the figure of merit can be expected to increase substantially.
References:


(33) Jayesh Nath, Dipankar Ghosh, Wael Fathelbab, Jon-Paul Maria, Angus I. Kingon, Paul D. Franzon, and Michael B. Steer, “A Tunable Combline Bandpass Filter


5.0 CONCLUSIONS

Agile RF (radio frequency) and MW (microwave) components, which are low cost, low loss and capable of multitasking at different frequency bands form an important part of many modern communication and remote sensing systems. In this thesis the scope and motivation for integrating Barium Strontium Titanate (BST) thin film varactors in frequency agile MW devices has been discussed, and the advantages over other competing technologies, such as ferrites, MEMS, and semiconductors have been presented.

Various researchers have worked on integrating ferroelectric thin films in tunable microwave circuits for some time. Traditionally such devices have incorporated expensive single-crystal substrates such as sapphire, MgO or LaAlO$_3$, and noble metallization such as Pt or Au rendering them cost prohibitive. In this work we have chosen low cost polycrystalline alumina substrates and Cu metallization.

The initial thrust of this research work was optimizing of processing conditions for RF sputtered Ba$_{0.60}$Sr$_{0.40}$TiO$_3$ thin films on polycrystalline alumina substrates and characterizing BST IDCs (interdigitated capacitors) at RF / MW frequencies. XRD and AFM results indicate randomly oriented, crystalline, void free microstructure. For the optimized Cu / BST /alumina IDCs a dielectric tunability of 40% at 12V/µm, a dielectric $Q$ of ~ 100 at 1 MHz and a $Q$ of ~ 30 at 26 GHz at zero bias is obtained. These values are comparable and in some cases superior to BST thin film based devices fabricated using expensive single-crystalline substrates and noble metallization.

The BST thin films show low leakage current characteristics ($J = 1.0 \times 10^{-6}$ A/cm$^2$) for an electric field of 10 V/µm. Permittivity and loss tangent of BST thin films
were frequency independent, while conductor losses begin to dominate device $Q$ in the GHz range.

The second part of the thesis deals with MW device issues. Available BST varactor device configurations, such as MIM and IDE have been compared. A planar capacitor (IDC) topology was chosen for integration into MW circuits since it enables single step fabrication and provides very small capacitance values. A modified photolithographic lift off process, that enabled patterning 3-5 $\mu$m features with > 1$\mu$m metal thickness, was developed and used in this work. Both scientific and engineering approaches were used to overcome the various material and device integration challenges.

These BST IDC varactors were incorporated as the tuning component in several integrated microwave circuits including a $3^{rd}$ order Chebychev combline band pass filter and a X – band (8 - 12 GHz) phase shifter. These prototypes clearly demonstrate the feasibility of this technology for wireless communication.

The optimized filter was centered at 1.85 GHz and tuned to 2.05 GHz for an applied bias of 125 V. The mid-band insertion loss was 4.5 dB at zero bias and this decreased to 3.5 dB at 125 V bias. Return loss was better than 9 dB for all bias levels. Filter performance was enhanced by optimization of metallization process and improvement in filter design and architecture. The filter also exhibited low power consumption ($< 6 \mu$W), and low intermodulation distortion (IP3 = 38dBm).

The X – band phase shifter showed a phase shift of 18° for an applied bias of 130 V at 10 GHz and had an insertion loss of only 1.1 dB at zero bias at 10 GHz. The return loss was better than 19 dB for all bias states. Though modest phase shift was achieved,
the insertion loss is among the best ever reported. The first prototype of the phase shifter show promise and exhibits a figure of merit of 17 °/ dB. In addition the MW phase shifters are compact, occupying an area of only 0.4 mm² and low mass.

A low cost device package (base metal, Cu / polycrystalline ferroelectric film, BST/ ceramic substrate, alumina) is presented and its performance is evaluated against conventional MW designs. To our knowledge this is the first comprehensive demonstration of an integrated MW device using ceramic substrates and base metallization incorporating ferroelectric thin film technology at room temperature.

We have shown that low cost, high performance and compact tunable microwave devices can be prepared using inexpensive materials, and simple and inexpensive processing routes entirely compatible with large area deposition. These designs and processes appear to be compatible with the performance and manufacturability requirements of predicted MW device technologies.
6.0 FUTURE WORK

The future work is focused in four areas: understanding the mechanism behind the enhanced tunability of BST thin films that have experienced higher thermal budgets, investigation of microfabrication processes and innovative circuit designs that allow higher aspect ratio feature sizes, minimized control voltages, and lower the insertion loss. Investigation of an adhesion layer that will allow top electrode annealing and a study of dielectric reliability is also envisioned.

As we have observed earlier, the BST thin films that are deposited at higher temperature and annealed at higher temperature for longer times have higher dielectric tunability than BST films deposited at lower temperatures and annealed at lower temperatures for shorter times. AFM studies show an increase in grain size for the samples with higher thermal budgets. However detailed microstructural studies including cross sectional TEM is required to study the grain morphology and to gain an understanding of the effect behind the enhanced tunability.

It is essential to improve the conductor loss and tunability performance for optimizing the MW device performance. Future efforts must be directed towards improving both of these factors. For minimizing metallization losses, at least three skin depths of metal layers are required. A more rigorous optimization including improved lithographic tools and more tightly controlled ambient conditions are likely to be necessary for this procedure. This will in turn provide lower voltage tuning with reduced metallization loss. Innovative designs in the varactor topology such as having wider IDC fingers while keeping small finger spacings are likely to complement the resolution of this issue. Wider fingers, and hence larger finger area, will decrease the electrode series
resistance and therefore minimize metallization loss while smaller finger spacings will allow lower control voltages. Also novel microfabrication techniques such as selectively electroplating the conductor lines in the MW circuit to increase the metallization thickness should be explored.

In this work we have utilized sputtered Cr thin films as an adhesion layer for thermally evaporated Cu top electrodes. Because of the presence of Cr, it is difficult to do any top electrode annealing since it is very challenging to maintain the integrity of Cr during post deposition top electrode anneals from thermodynamic considerations. It is worthwhile to investigate alternate adhesion layers such as IrO\(_2\) (Iridium oxide). This may allow post deposition electrode anneals and will possibly lower the resistivity of the as deposited Cu top electrodes; this will ultimately reduce the conductor losses.

For some device applications, it may be necessary to achieve lower leakage currents. Literature studies of leakage current in BST IDC are non existent unlike the well documented studies in case of BST MIMs. In this work some preliminary work has been done in this direction but more detailed work is necessary to compare leakage current in BST planar and parallel plate capacitor configurations. Finally, reliability characterization of BST varactors needs further attention. As very little is known regarding BST reliability and lifetime in IDC geometry, a comprehensive investigation is critical to determine the appropriateness of this material and its preparation technology in service.