ABSTRACT

MA, LEI. Gallium Nitride Heterogeneous Source Drain MOSFET. (Under the direction of Assistant Professor Doug W. Barlage).

This work focuses on device design, device processing and characterization of Gallium Nitride heterogeneous source drain MOSFET and MISFET transistors. The unique material properties of GaN make it one of the best candidates for high power, high frequency semiconductor devices. Comparing with other GaN based devices, GaN based MOSFET has the advantages of low gate leakage, low power consumption which is critical for both high power, high frequency applications and low power digital applications. One of the challenges of GaN MOSFET research is that it is difficult to achieve heavily doped source/drain. We investigate some of the other methods excluding ion implantation to achieve the carrier rich source/drain regions for GaN MOSFET. Highly doped GaN to form regrown source/drain has been demonstrated in our group as one of the possible solutions. To further improve GaN based MOSFET performance and to explore some of the other alternative solutions, in this research, GaN heterogeneous source drain MOS structures are explored which allow maximum dopant incorporation and maximum abruptness in the source/drain regions to maximize the transistor's cut off frequency as well as the critical I_{on}. The device is designed on unintentionally doped GaN film on Sapphire grown by MOCVD. Ni is used as Schottky barrier source/drain. Si_3N_4 is used as gate dielectric material. The detailed device process flow is designed carefully to mitigate the gate drain shorting problem and the device vertical profile is designed using low mesa height to maintain gate metal connectivity between gate metal on top of the gate dielectric and the gate interconnect metal pad. The device process

flow of the GaN Schottky barrier MOSFET/MISFET is compatible with commonly used GaN HEMT and MESFET process flow with one additional photolithography step. The final device processing time is much decreased comparing with other methods to form source/drain for GaN MOSFET device.

The fabricated devices are normally on with a threshold voltage of -7V. The other electrical performances of the GaN SB-MISFET include low pinch off current and very low gate leakage current (below 5pA). For a device with W/L=100μm/0.7μm, the maximum drain current and maximum transconductance achieved are 88.4μA/mm and 17.2μS/mm. Moreover, the device is the first time demonstration of depletion mode n-channel Schottky barrier MISFET on GaN film grown on Sapphire to our best knowledge. The device demonstrated has also the capability of doing high frequency characterizations. The successful demonstration of the GaN SB-MISFET shows the feasibility of using Schottky metal as source/drain material for GaN MOSFET and MISFET design.

Gallium Nitride Heterogeneous Source Drain MOSFET

By

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APPROVED BY:

Dr. John F. Muth	**Dr. Leda Lunardi**
Dr. Doug W. Barlage **Chair of Advisory Committee**	**Dr. Mark Johnson**

DEDICATION

To the memory of my dear mother
Zhao, Yuqin
(1945-2002)

To My father
Ma, Huansheng

To my brother
Ma, Zhengkun

To my sister
Ma, Lili

And to my wife
Li, Lei

BIOGRAPHY

Lei Ma was born in the town of Ledu, Qinghai province, China in June 1976. He moved with his parents to the city of Xining, the capital of Qinghai in 1988 where he graduated from Qinghai high school in 1995. Then he joined the University of Science and Technology of China (USTC) located at Hefei, Anhui province. Five years later he graduated with a Bachelor of Science in physics. He enrolled as a Master's student at University of North Carolina at Chapel Hill in August 2000 and got his M.S degree in physics in 2002. Upon completion of the Master's program he enrolled as a Ph.D student at North Carolina State University in August 2003. He studied RF and Microwave semiconductor devices and microwave circuit design under the supervision of Dr. Doug W. Barlage. His graduate research focuses on Nanoelectronics, RF and microwave semiconductor devices particularly GaN based MOSFET processing development, device characterization and device modeling. His other research interests involve novel semiconductor materials, diluted magnetic semiconductor (DMS) based spintronic devices, semiconductor device physics and semiconductor device modeling.

He was an Intern Engineer at RF Micro Devices (RFMD), Greensboro, NC in summer 2006 where he worked on GaAs HBT breakdown analysis using pulsed IV measurement, correlation between HBT breakdown and device ruggedness, and GaAs based BiFET transistor TCAD modeling.

Lei Ma is a student member of American Physics Society (APS), and Institute of Electrical and Electronics Engineers (IEEE).

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The staffs at Photonic Laboratory and Advanced Electronic Materials Processing Center at North Carolina state university deserve a special mention for their assistance during the course of this work, in particular Mr. Joe Matthews, Dr. Ginger Yu for their help with the training and suggestion on device fabrication.

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Chapter 1

Introduction

1.1 Overview of GaN FET Transistors

As wireless communication technology moves forward, the power and linearity performance requirements placed upon the power amplifier in these systems become more difficult to meet. Currently, silicon LDMOS power transistors are the output devices of choice for base station power amplifiers, but as the limits of operability of these devices are reached, there will be a need for a semiconductor material that can fulfill the requirements of the third generation of wireless technology. The unique electronic properties of Gallium Nitride (GaN), such as wide bandgap therefore high breakdown field, high critical electric field, high thermal conductivity, high electron mobility and high saturated electric velocity et al. make GaN the prime candidates for high power, high frequency applications. GaN based HEMTs have already created the record breaking output power densities at X, Ku band, and Ka band, [1-4].

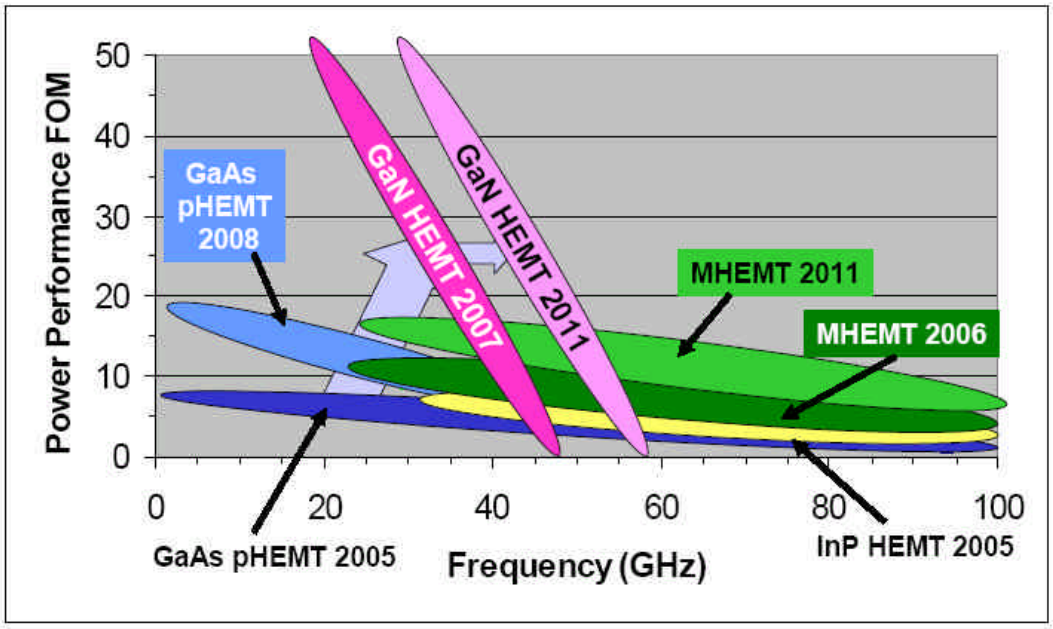

Figure 1.1: ITRS 2005 Roadmap: Evolution of production power devices 2005-2011 [5].

Figure 1.1 was published as “Radio Frequency and Analog/Mixed-signal technologies for wireless communications” in the 2005 international technology roadmap for semiconductors (ITRS). It shows power performance of different semiconductor technologies versus the device operating frequencies. The figure of merit (FOM) is monolithic microwave integrated circuit (MMIC) power density (W/mm) times MMIC SS gain per stage (dB) at application center frequency (typical 10%-20% bandwidth). As shown in the roadmap, the InP HEMT, and MHEMT shows their advantages in high speed application, and GaN HEMT is expected to be dominant in high power application from 20GHz to 60GHz.

Gallium nitride (GaN) bas been the topic of intense research and development activities during the past 10 years. The beginning of GaN based field effect transistors (FETs) research can be dated back to 1990s. The first report of GaN based transistors was by Khan et al. [6] [7]. In 1993, they demonstrated a GaN MESFET and an AlGaN/GaN HEMT, both

transistors had gate lengths of 4um, the MESFET has a g_m of 23 mS/mm and I_{ds}(max) of 180 mA/mm at V_{gs} = 0 V, V_{ds} = 20 V. The HEMT has a g_m of 28 mS/mm and I_{ds}(max) of 50 mA/mm at V_{gs} = 0.5 V, V_{ds} = 25 V. The first microwave measurement results on GaN based transistors were published by Binari et al., for a GaN MESFET with f_T of 8GHz and f_{max} of 17GHz for a gate length of 0.7um [8]. Since these early results, significant improvements have been made in material quality and device processing. AlGaN/GaN 2DEG mobility up to 2019 cm^2/Vs has been achieved for growth on 8H-SiC and 1600 cm^2/Vs for growth on sapphire by M. Shur's group RPI in 1998 [9]. The saturation current has been pushed to 1.6 A/mm and the transconductance has reached 340 mS/mm [10]. The state of the art AlGaN/GaN HEMT in 90s has a f_T of 140GHz by Eastman and coworkers at Cornell University [11]. The power density of 6.8 W/mm at 10GHz has been achieved by Sheppard et al. [12]. On the other hand, in 1994, the demonstration of a heterostructure bipolar transistor (HBT) using *p*-type 6H SiC as the base and *n*-type GaN as the emitter was reported [13]. Then the demonstration of a HBT using AlGaN/GaN material system was reported in 1998 [14]. The early rapid improvements made in the performance of the GaN based FETs during 1990s are discussed in the review [15]. In the new 2000 millennium, more improvements on GaN HEMT have been reported. The highest room temperature electron mobility of 2DEGs in GaN HEMT on sapphire has been achieved to 2050 cm^2/Vs which is approaching the state of the art for HEMT grown on SiC [16]. The record breaking power density of 30 W/mm at X band was demonstrated by U. K. Mishra's group at UC Santa Barbara [3]. The enhancement mode GaN HEMT and AlGaN/GaN/InGaN/GaN DHEMT have been reported by K. J. Chen and K. M. Lau's research group at Hong Kong University of Science and Technology in China [17-20].

The GaN based FET including MESFET and particularly HEMT have attracted so much research attention, however the GaN MESFET and HEMT have been also facing several challenges. First, the device performance degrades at RF drive due to current dispersion which basically shows different device RF and pulsed current comparing with device DC current. Some studies of the dispersion and surface states associated with the GaN HEMT have been reported. [21-24]. And Si_3N_4 and p-GaN have been used to passivate the surface states [22] [25] [26]. Second, the HEMT suffers from the real space charge transfer effect which leads to degraded current performance [27]. To addressing the problems facing GaN HEMTs, the idea of GaN MOSHFET has been proposed to reduce the real space charge transfer effect by M. A. Khan's group at University of South Carolina and M. S. Shur's group at RPI. [28-30]. The most recent result from Khan's group is a AlGaN/InGaN/GaN MOS-DHFET with RF output power of 15 W/mm at 2GHz and peak drain current of 1.67 A/mm [31].

While the GaN HEMT and MOSHFET are promising for high power and high current applications, the GaN MOSFET or MISFET are potential candidates for future low power high speed digital applications and for high power high speed applications if certain dielectric material can be deposited on GaN to achieve high inversion channel carrier concentration. In 1998 the first GaN MOSFET was fabricated by Ren et al. at University of Florida [32] [33]. One of the major issues of GaN MOSFET fabrication is the dielectric materials. Unlike Si, the lack of native oxide for III-V compound semiconductors had prevented the incorporation of MOS structures that are critical to the creation of compound semiconductor based MOSFET. However recently Freescale Semiconductor, Inc., one of the world's largest semiconductor companies announced the breakthrough of the gate dielectric

materials research for high performance GaAs MOSFET [34-36]. The successful demonstration using Ga_2O_3/Gd_2O_3 as the gate dielectric materials enables the merging of III-V compound semiconductors' better electron transport properties with device scalability provide by high K dielectric.

There are several dielectric materials which have been applied to GaN MOSFET structure including SiO_2, Si_3N_4, Ga_2O_3, Gd_2O_3, MgO, et al. and the combination layers of the insulator materials mentioned here. Since Ren et al. have made the first GaN MOSFET using Ga_2O_3/Gd_2O_3 as the dielectric in 1998 [32] [33], several other dielectric materials have been successfully demonstrated on GaN MOSFETs. S. Arulkumaran et al. at Nagoya Institute of Technology in Japan investigated SiO_2, and Si_3N_4 as dielectric for GaN depletion model MOSFET with low interface state density [37]. In 2000, R. Therrien, G. Lucovsky and R. Davis at North Carolina State University made GaN MOSFET using SiO_2 and they modeled Ga_2O_3 as the gate dielectric material for GaN device indicating that Ga_2O_3 might be a better dielectric material for GaN MOSFET [38]. T. P. Ma's group at Yale University has demonstrated using $SiO_2/Si_3N_4/SiO_2$ as the gate dielectric for GaN MOSFET [39]. K. W. Lee et al. at National Cheng Kung University in Taiwan have demonstrated using SiO_2 by liquid phase chemical vapor deposition (LPCVD) for GaN MOSFET [40]. Y. Irokawa et al. at Toyota Central Research and Development Laboratories, Inc. in Japan collaborated with F. Ren's group and S. J. Pearton's group at University of Florida and C. C. Pan et al. at National Central University in Taiwan used MgO as the gate dielectric for GaN MOSFET [41] [42]. In 2005, K. Matocha, T. P. Chow and R. J. Gutmann at Rensselaer Polytechnic Institute (RPI) demonstrated the SiO_2 as gate dielectric with implanted source drain for circular normally off GaN MOSFET [43].

A significant limitation in the fabrication of III-N MOSFET relates to the formation of ohmic contacts for enhancement-mode MOSFET structures. Unlike existing III-N HFET devices, which include a high free carrier density two dimensional electron gas (2DEG) in the semiconductor substrate, a MOSFET in either accumulation or inversion mode requires low free carrier concentrations for the semiconductor channel to have an off-state. The applied gate bias enhances the free-carrier density in the channel, turning on the FET. Unfortunately, a low free-carrier density substrate is problematic for the formation of ohmic contacts, a problem usually dealt with in silicon MOS through self-aligned ion implantation. The high annealing temperatures (1100°C-1500°C) associated with activating implanted dopants to substitutional sites limits the use of ion implantation for III-N MOSFET fabrication [43][44]. In 2006, F. Ren's group and S. J. Pearton's group at University of Florida in collaboration with C. J. Pan et al. at National Central University in Taiwan and P. Bove, et al. at Picogiga International SAS in France have demonstrated the thermal diffused source/drain formation for GaN MOSFET [45]. Our group collaborating with Dr. Mark Johnson's group in department of material science and engineering at NCSU explores some of the alternative methods to achieve carrier rich source/drain for GaN MOSFETs. We have successfully demonstrated the n^+ GaN source/drain regrowth for GaN MOSFET application [46].

Another important alternative method to achieve carrier rich source/drain for MOSFET is using metal to form Schottky barrier source/drain, this idea has been applied to Si MOSFET for about 40 years [47] [48] and it is attracting more research interests [45-64] for aggressively scaled Si MOSFET. In 2006, using Schottky metal as source/drain has been proposed the first time on GaN MOSFET by H. B. Lee et al. at Kyungpook National

University in Korea in collaboration with Y. H. Bae at Uiduk University in Korea and M. B. Lee at Daegu New Technology Agency in Korea [65]. Our group quickly realized the advantages of using metal as the Schottky barrier source/drain for GaN based MOSFET and MISFET devices. Therefore this work is dedicated to GaN Schottky barrier MOSFET and Schottky barrier MISFET device design, device processing and device characterizations.

1.2 Motivation and Objectives

Even though GaN based MESFET and HEMT have been demonstrated with excellent device characteristics, they have several drawbacks. The leakage from the Schottky gate of such devices is a major concern for operation at elevated temperatures. The real space charge transfer causes the decrease of drain current at high gate bias and the formation of the parasitic MESFET conduction in the AlGaN cap layer. And the RF current dispersion degrades the device performance at high frequency which is caused by the presence of surface states between source and drain. Due to these drawbacks, the devices demonstrated usually have low gate swing voltage, low gate breakdown, certain gate lag in the transient analysis.

As an alternative, the use of an insulated gate metal oxide semiconductor (MOS) structure has some advantages to address the problems facing HEMT and MESFET. The main advantages are:

1) MOSFET reduces both gate leakage and power consumption, and it has much better temperature sensitivity since it does not suffer from the severe leakage encountered in Schottky based devices.

2) MOSFET eliminates the charge transfer effect and the gate breakdown problem.

3) MOSFET supports larger gate swing voltage which usually results in better linearity than HEMT and MESFET,

4) Unlike MESFET and HEMT, MOSFET can use high temperature implantation to form highly doped source and drain without compromising the gate contact.

5) Circuit design can be simplified since MOSFET can be used to form single supply voltage control circuit for power transistors.

6) The use of MOSFET also allows the use of complementary devices and thus producing less power consumption and simple circuit design.

Moreover with the rapid development of a suitable insulator for GaN MOSFET structure, and currently available techniques to achieve low density of GaN-insulator interface states in GaN MOSFET devices [28-40] [66], GaN based MOSFET is possible to achieve competitive performance comparing with GaN HEMT in high power and high frequency applications.

GaN is also a potential candidate for very short channel devices because of its large bandgap, high saturation velocity and overshoot velocity, and high thermal conductivity. As the Si CMOS keeps scaling down, the short channel effect is getting more pronounced, comparing with Si, GaN has more advantages of suppressing the source/drain leakage, supporting larger drive current, and ease the restriction of the device cooling [67].

The traditional Si MOSFET uses either ion implantation or thermal diffusion to form the source/drain. However for GaN MOSFET source/drain implantation, very high activation temperature over 1500°C is needed [44] which sets a high thermal budget for GaN MOSFET device processing. The high activation temperature also roughens the GaN surface and makes it difficult to grow high quality oxide. The GaN MOSFET source/drain formed by Si dopant

thermal diffusion at temperature 800°C - 1000°C is investigated and demonstrated with improved device performance comparing with ion implanted GaN MOSFET [45]. To further improve the GaN MOSFET performance and to look for a device with novel source/drain materials combined with novel structures which has the scalability beyond the traditional silicon CMOS. The idea of Schottky metal source/drain is adopted from Si Schottky barrier MOSFET. The actual advantages of the Schottky barrier MOSFET on GaN have been extended beyond that of the Si Schottky barrier MOSFET mainly because:

1) The manufacturing process for GaN SB-CMOS is simpler than conventional bulk CMOS, requiring fewer process and photolithography steps. The process is fully compatible with the existing silicon CMOS technologies and does not require novel process equipment.

2) The Schottky metal can be used as the carrier rich source/drain, therefore the device manufacturing can exclude the ion implantation and thermal diffusion which requires high temperature for dopant activation. Metal source/drain also mitigates the scaling limitation of S/D doping profile control, sheet resistance, and contact resistivity et al.

3) Schottky barrier MOSFET has superior control of off state leakage current due to intrinsic Schottky potential barrier, and it also helps to eliminate the parasitic bipolar actions, furthermore it eliminates some of the short channel effects for aggressively scaled MOSFET such as GIDL (gate induced drain leakage).

Therefore GaN based heterogeneous source drain MOS structures are explored in this research. With advantages from GaN channel material and heterogeneous source drain Schottky barrier MOS structure, we expect to see a novel device with promising performance in low power high speed digital application, and possibility for high power high frequency application.

1.3 Outline of the Dissertation

This Dissertation is divided into six chapters.

Chapter 1 is intended as an overview of the history of GaN electronics devices and introduction of the GaN based field effect transistors including MESFET, HEMT, MOSHFET, and MOSFET. The motivation of GaN MOSFET research especially GaN Schottky Barrier MOSFET is introduced.

Chapter 2 introduces some of the basic semiconductor device physics of GaN including the crystal structure, band structure, electron transport property, and polarization effect. It is followed by the MOSFET device modeling using ISE-TCAD, with the emphasis on III-V compound semiconductor MOSFET transistor, particularly InSb and GaN MOSFET. The planar InSb MOSFET is simulated to compare with Si MOSFET. Various types of SOI MOSFETs are simulated to compare the GaN based MOSFET with their Si counterpart.

Chapter 3 starts with the introduction of the source/drain techniques for GaN based MOSFETs with the emphasis on the regrown source/drain and Schottky metal source/drain. The source/drain formation processes are compared and the metal liftoff to pattern the source/drain is selected. The ungated GaN MOSFET structure also called n-i-n structure is fabricated as a testing structure in the middle of GaN Schottky barrier MOSFET device processing steps. The n-i-n testing structures with regrown source/drain and Schottky metal source/drain are characterized and also modeled using TCAD. The metal-GaN Schottky barrier height has been reviewed. Finally the GaN wet etch techniques are reviewed and GaN binary etch is explored.

Chapter 4 demonstrates the pulsed doped GaN MESFET investigated in this work. The chapter starts with a brief introduction of the idea of pulse doped GaN film. It is

followed by a detailed MESFET device processing steps on this pulse doped GaN film and the DC characterization of the fabricated GaN MESFET. The RF characterization of the low dimension device with gate length of 0.7 μm is shown. Several key device parameters such as gate capacitance, sheet carrier concentration, output conductance, and low field mobility have been extracted from the high frequency S parameter measurements. Detailed analysis and comments on these MESFET have been included in the chapter along with the presentation of the device electrical characteristics. The chapter ends with a summary of these MESFETs performance.

Chapter 5 demonstrates the depletion mode GaN SB-MISFET for the first time to our best knowledge. The chapter starts with a brief introduction of the different gate dielectric materials which have been applied to GaN MOSFET and MISFET devices. It is followed by introducing the idea of using Schottky barrier metal as the source/drain for GaN MOSFET and MISFET devices. Then the detailed GaN SB-MISFET device processing steps is described for a device fabricated on GaN film grown by MOVPE on sapphire. The DC characterization of the fabricated GaN SB-MISFET are shown for FatFET device with gate dimension of 100μm × 50μm and RFFET device with gate dimension of 100μm × 0.7μm. Furthermore, this is the first time demonstration of such small gate length GaN MISFET with the capability of doing high frequency characterization. RF characterization of the low dimension device with gate length of 0.7 μm is shown. Several key device parameters such as gate capacitance, sheet carrier concentration, output conductance, and low field mobility have been extracted from the high frequency S parameter measurements. Detailed analysis and comments on these GaN SB-MISFET have been included in the chapter along with the

presentation of the device electrical characteristics. The chapter ends with a summary of these novel GaN SB-MISFETs performance.

Chapter 6 summarizes the research results and provides guidelines for future research directions.

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Chapter 2

GaN Device Physics Background and TCAD modeling

This chapter starts with introduction of some of the basic semiconductor device physics of GaN including the crystal structure, band structure, electron transport property, and polarization effect. It is followed by the MOSFET device modeling using ISE-TCAD, with the emphasis on III-V compound semiconductor MOSFET transistor, particularly InSb and GaN MOSFET. The planar InSb MOSFET is simulated to compare with Si MOSFET. Then various types of SOI MOSFETs are simulated to compare the GaN based MOSFET with their Si counterpart.

2.1 Basic Semiconductor Device Physics

2.1.1 Crystal Structure

In the periodic table of the elements, Silicon (Si) and Germanium (Ge) are 4a elements, Aluminum (Al), Gallium (Ga), Indium (In) are all 3a elements, while Nitrogen (N), Phosphorous (P), Arsenic (As), Antimony (Sb) are all 5a elements. The III-V compound

semiconductor can be formed by combining the 3a elements with 5a elements, for instances, the electron configuration is [Kr] $5s^2 4d^{10} 5p^1$ for Indium and [Kr] $5s^2 4d^{10} 5p^3$ for Antimony, by sharing the 5p electrons through the covalence bond, the compound of Indium Antimonide (InSb) forms; the electron configuration is [Ar] $4s^2 4p^1$ for Gallium and [He] $2s^2 2p^3$ for Nitrogen, by sharing the 4p and 2p electrons through the covalence bond, the compound of Gallium Nitride (GaN) forms. Similarly, GaAs, InP and other III-V compound semiconductors can be formed in the same way. However, for some of the compound semiconductors such as GaAs, GaN, and ZnS etc, the crystal structure can be different depends on how the atoms pack. The zinc blende structure is formed by the face centered-cubic close-packing; the wurtzite structure is formed by hexagonal close-packing.

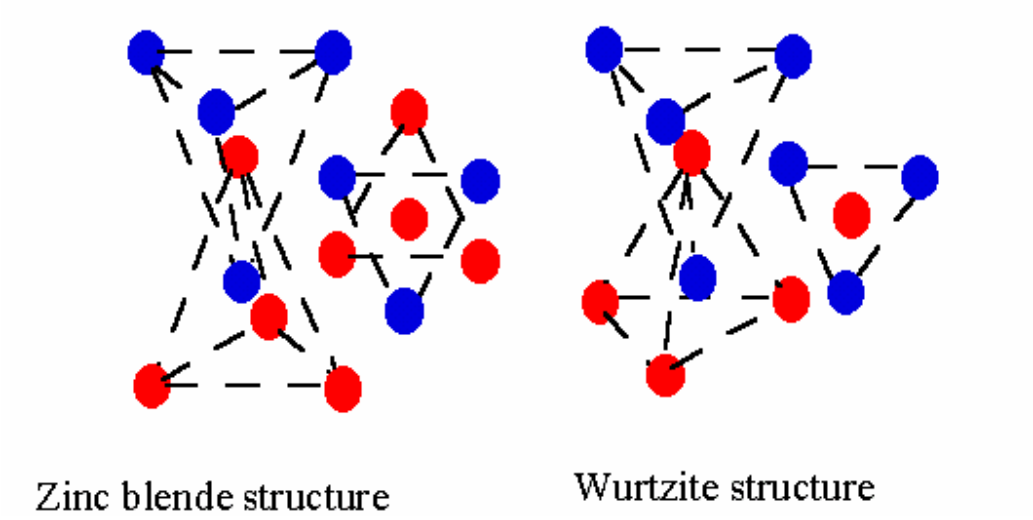


Figure 2.1: Zinc Blende and Wurtzite structure difference in close-packing [1].

For GaN, there are two kinds of crystal structures, either zinc blende or wurtzite. Actually, the zinc blende structure can be viewed as two interpenetrating face-centered cubic (FCC) lattices, and the wurtzite structure forms by two interpenetrating hexagonal closed-packed lattices.

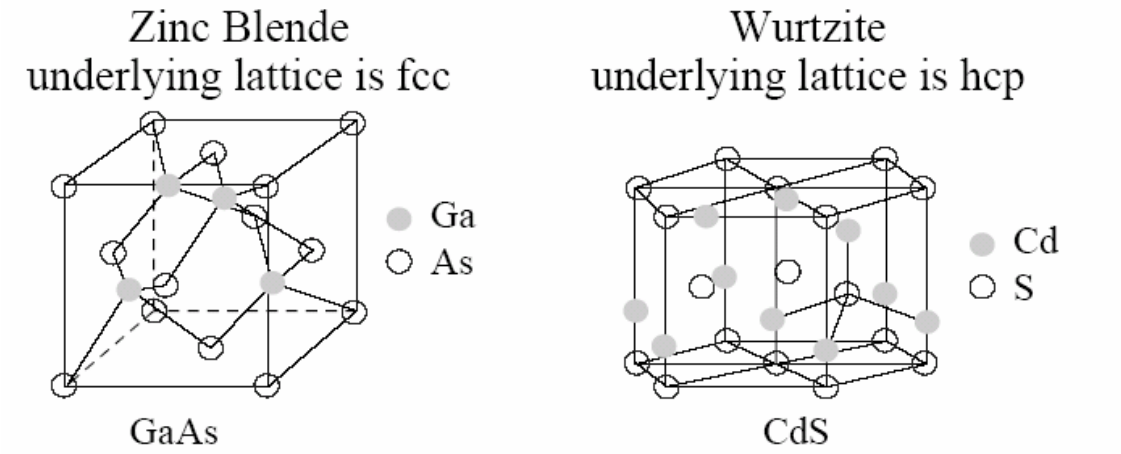


Figure 2.2: Zinc Blende and Wurtzite crystal structure

For SiC, however, things get even more complicated. SiC can form either cubic close-packing structure or one of the several different kinds of hexagonal close-packing structures. There are more than 200 different polytypes, the most important are: 3C-SiC which is zinc blende structure, 2H-SiC, 4H-SiC, 6H-SiC which are different kinds of wurtzite structures, 15R-SiC, 21R-SiC, 24R-SiC, et al. which are different rhombohedral structures.

2.1.2 Energy Band

For different semiconductors, their energy bands in reciprocal space vary because of the different crystal lattice structures and bonding mechanisms. The following figure shows the calculated wurtzite GaN energy bands by Bloom et al. [2]. There are several conduction bands and valence bands shown and it is considered a full band calculation.

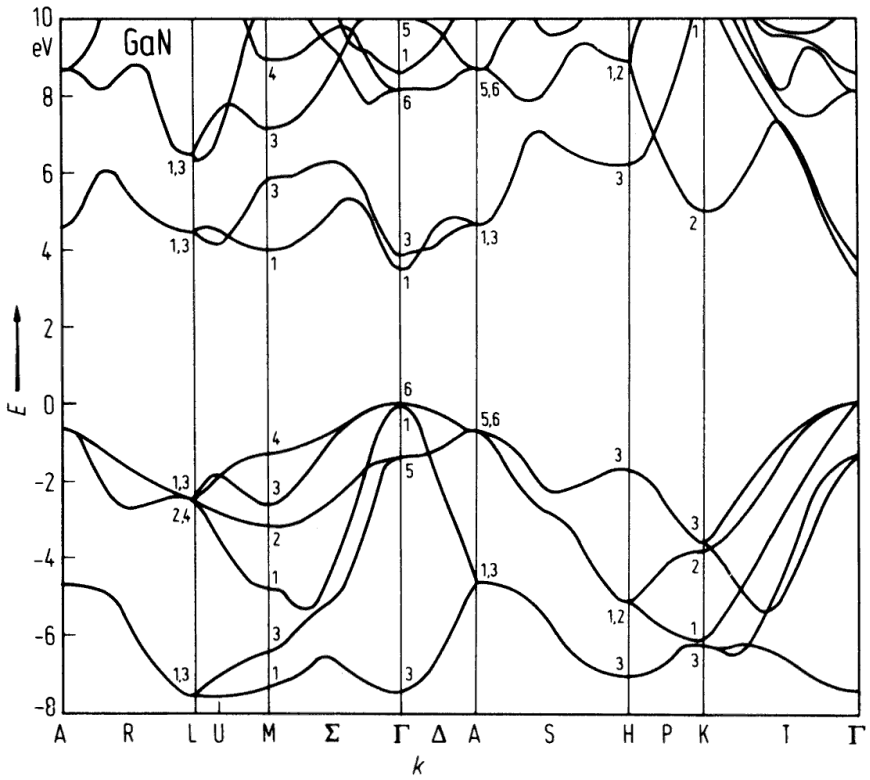
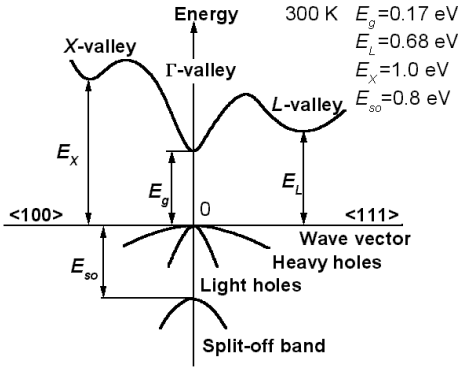


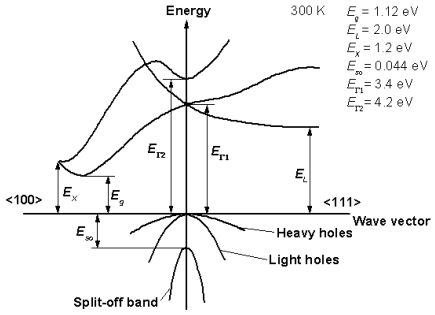
Figure 2.3: Calculated Wurtzite band structure [2].

However according to Fermi-Dirac statistics, most of the electrons in conduction band are in the bottom valley of conduction band edge, most holes in valence band are in the top peak of valence band edge.

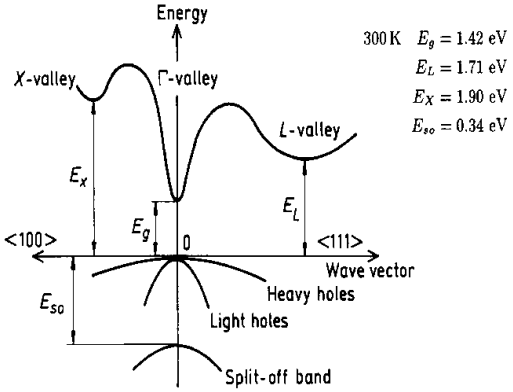
Because a full band calculation is very computing intensive, usually the simplified band structures are widely used instead of full band structures. And more importantly the general device modeling using the simplified band structure as an approximation agrees with the fabricated device. The following figures show the simplified band structure of InSb, Si, GaAs, zinc blende GaN and wurtzite GaN. Si has indirect band gap, and InSb, GaAs, and GaN have direct band gap which make them suitable for optoelectronic applications.



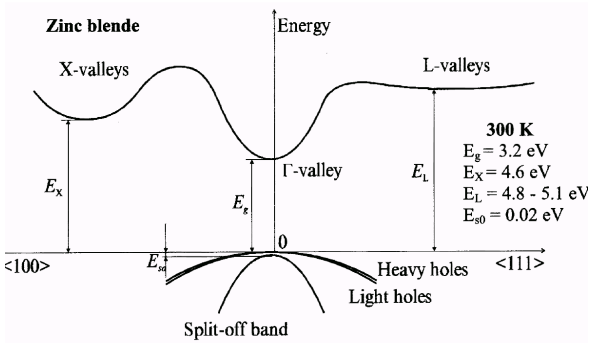
(a) InSb band structure [3].



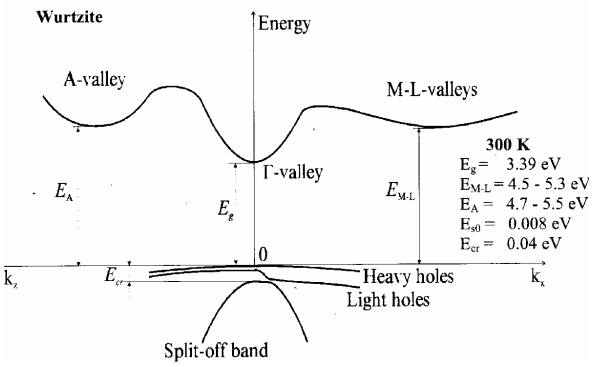
(b) Silicon band structure [3].



(c) GaAs band structure [3].



(d) Zinc Blende GaN band structure [4].



(e) Wurtzite GaN band structure [4].

Figure 2.4: Band structures of (a) InSb, (b) Si, (c) GaAs, (d) zinc blende GaN and (e) wurtzite GaN [3][4].

The effective mass in general is tensorial with components m_{ij}* defined as the second derivative of energy with respect to wave vector k:

$$\frac{1}{m_{ij}\,*} = \frac{1}{\hbar^2}\frac{\partial^2 E}{\partial k_i \partial k_j} \tag{2.1}$$

Because of the conduction band consists of a set number of sub-bands, for Si there are six ellipsoids as the constant energy surfaces along <100> direction; for Ge there are eight half-ellipsoids along <111> direction; for GaAs, the constant energy surface is a sphere. By fitting the experimental band structure results to parabolic bands, we can obtain electron effective masses: one for GaAs, two for Ge, and two for Si, m_l* along the symmetry axes and m_t* transverse to the symmetry axes [5]. From above figures, the E-k relationship of different semiconductors can be used to derive the effective mass of density of states. We notice that the larger curvature of the energy band, the smaller effective mass it is. The electron effective mass of InSb is as low as $0.013m_0$ [6]; the electron effective mass of GaAs, zinc blende GaN and wurtzite GaN are $0.063m_0$ [3], $0.13m_0$ [7], and $0.20m_0$ [7], respectively. And the electron effective mass of Si is $0.98m_0$ for longitudinal direction, $0.19m_0$ for transverse direction [3]. The effective mass of holes are defined similarly but with consideration of three folds degeneracy at k=0 (Γ point) which include heavy hole, light hole band, and a split-off band. Comparing with the hole effective mass $0.81m_0$ of Si, the hole effective mass of InSb is $0.43m_0$; the hole effective mass of GaAs, zinc blende GaN and wurtzite GaN are $0.53m_0$, $1.4m_0$, and $1.50m_0$, respectively [3].

The figure 2.5 is a summary of the bandgap versus lattice constant for some of the semiconductors. At room temperature, InSb is the semiconductor with the narrowest bandgap

0.17eV, zinc blende GaN has a bandgap of 3.2eV, and wurtzite GaN has a wide bandgap of 3.4eV.[7]

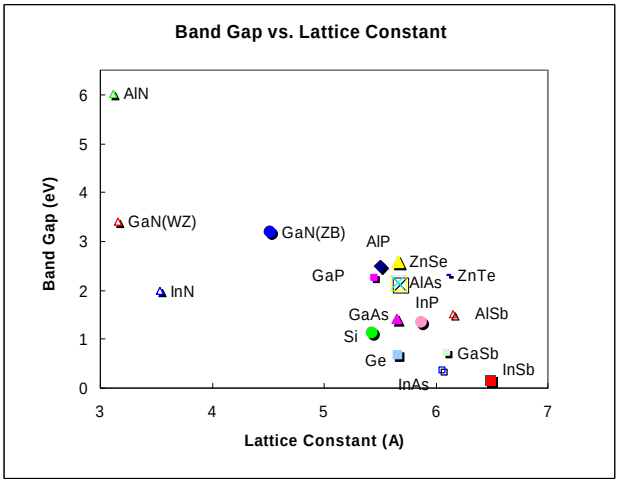


Figure 2.5: Band Gap vs. Lattice constant for some semiconductor materials.

2.1.3 Carrier Transport

Carrier transport is very important for device operation and the carrier transport modeling is one of the most important parts in device modeling. At low field, the drift velocity v_d is proportional to the electric field E, with the proportionality constant μ is defined as the mobility:

$$v_d = mE \tag{2.2}$$

For nonpolar semiconductors such as Si and Ge, the presence of acoustic phonons and ionized impurities usually results in scattering which degrades the mobility. For polar semiconductors such as GaAs, the optical phonon scattering is significant. In addition, the intravalley scattering, intervalley scattering and other mechanisms will also affect mobility. For III-V compound semiconductor such as GaAs, GaN, and InSb, the intervalley scattering is also called transferred electron effect for high energy electrons excited from Γ valley to

satellite valleys such as L valley and X valley in high electric field. Since the electron effective mass is greatly increased in L valley and X valley, the mobility will decrease at certain electric field which more often is seen as negative differential resistance effect in the III-V based electric devices.

It is worth mentioning the mobility in equation 2.2 is for bulk semiconductor materials. For device channel mobility, the transverse electric field which is normal to the direction of the carrier movement will further degrade the carrier mobility. For instance, MOSFET devices which rely on the inversion channel, the channel mobility is degraded by Coulomb scattering at low normal field, by surface phonons and surface roughness scattering at large normal field. [8]

The following figure summarizes the electron drift velocity versus longitudinal electric field for several bulk semiconductor materials. In comparison, InSb has very high electron drift velocity and also high mobility; on the other hand, GaN has very high saturation field, and high peak drift velocity.

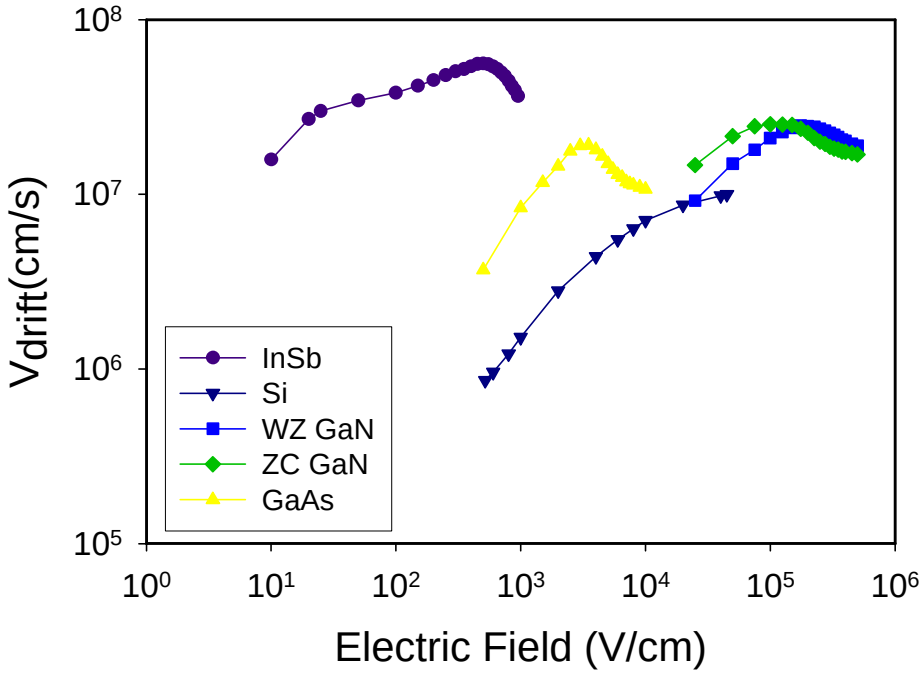


Figure 2.6: Drift velocity versus Electric field for InSb [9], Silicon [10], GaAs [11], wurtzite GaN and zinc blende GaN. [12][13]

As device scales down to sub-100 nanometer scale, the channel length is comparable or even smaller than the electron mean free path. In this case, electrons may acquire higher velocity than their equilibrium drift velocity as shown in figure 2.6. In the extreme case, some electrons may not experience any collisions during the transport. This mode of electron transport is called ballistic transport and the ultra-fast device might be realized with this effect. The GaN ballistic transport has been studied by Michael S. Shur's group and Lester F. Eastman's group and the Monte Carlo simulation shows GaN has much higher velocity overshoot than GaAs.[14][15]

2.1.4 Material Parameters

The bulk material parameters are summarized for Si, GaAs, InSb and GaN in the following table. GaN demonstrates superiority transport properties for high temperature, high-power applications.

Table 2.1: Material parameters of Si, GaAs, GaN and InSb

	Silicon	GaAs	GaN	InSb
Bandgap Energy (E_g eV)	1.12	1.42	3.41	0.17
Dielectric Constant (e_r)	11.8	12.8	9	17.7
Thermal Conductivity (k_{th} W/cm/K)	1.5	0.46	2.3	0.18
Dielectric Breakdown (E_b V/cm)	$3x10^5$	$5x10^5$	$5x10^6$	$1x10^3$
Saturation Velocity (v_{sat} cm/s)	$1x10^7$	$2x10^7$	$3x10^7$	$6x10^7$
Electron Mobility (μ_e cm^2/Vs)	1350	8500	1200	7800
Hole Mobility (μ_h cm^2/Vs)	450	400	~200	850

2.1.5 GaN Spontaneous and Piezoelectric Polarization

III-Nitride heterostructures are of interest for device applications such as blue laser, blue and UV LEDs, and power electronics. Comparing with traditional semiconductor Si and GaAs devices, GaN has two different lattice crystal structures: zinc blende and wurtzite. The wurtzite crystal structure exhibits a variety of material properties that are different from conventional zinc blende structures. Of particular interest are spontaneous polarization and piezoelectric polarization effects which recent researches have revealed to be very important in the design and analysis of nitride heterostrucure devices.

The spontaneous polarization in wurtzite structure is caused by its lower symmetry comparing with zinc blende structure. The spontaneous polarization, P_{sp}, is a nonzero dipole

moment in the crystal with or without external influence such as strain or applied electric field. The direction of the spontaneous polarization depends on the nitride crystal polarity. We define the nitride crystal polarity is along the negative c axis [000 $\bar{1}$] direction from cation terminated Ga face to anion terminated N face. Numerical values for the spontaneous polarization along (0001) axis have been calculated for the binary III-Nitride semiconductors. They are -0.029 C/m^2 for GaN, -0.081 C/m^2 for AlN and -0.032 C/m^2 for InN. [16]

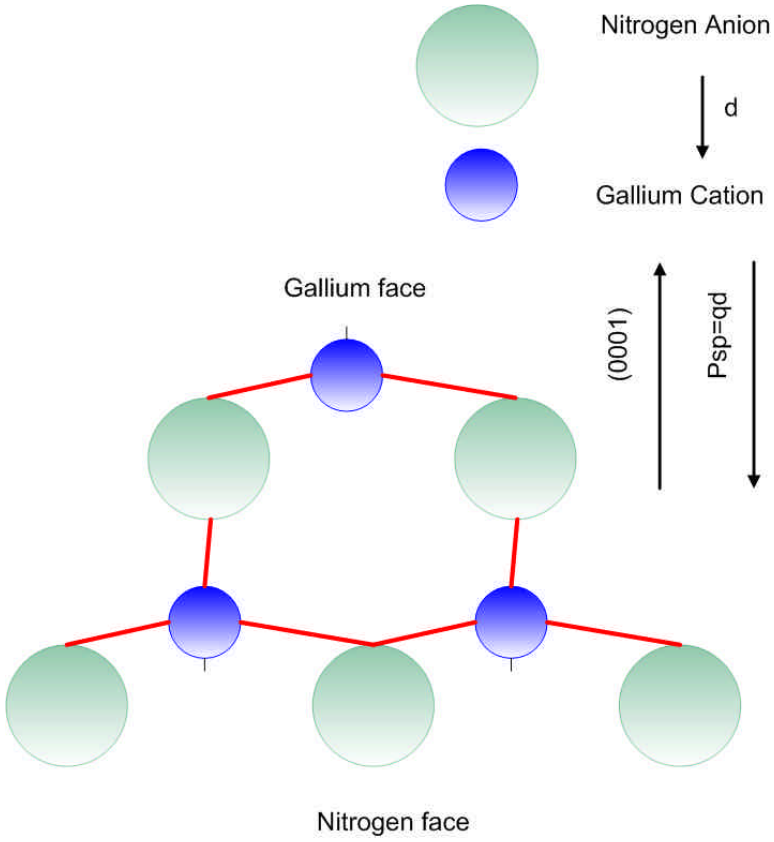


Figure 2.7: Schematic diagram of Wurtzite GaN crystal polarity and spontaneous polarization, modified from [17]

Both the wurtzite and the zinc blende crystal structure are non-centrosymmetric, and therefore both possess nonzero piezoelectric moduli. The piezoelectric moduli d_{ijk} and e_{ijk}

form third-rank tensors that relate the piezoelectric polarization field P_{pz} to the stress tensor σ_{jk} and ε_{jk}, respectively, via the relations:

$$P_{pz,i} = d_{ijk} s_{jk} = e_{ijk} e_{jk}, \; s_{ij} = c_{ijkl} e_{kl} \tag{2.3}$$

where c_{ijkl} is the elastic tensor of the crystal. Some of the tensors have non-vanishing elements only at certain indices due to crystal symmetry. A coherently strained III-Nitride epitaxial layer grown in the (0001) orientation will therefore posses a nonzero piezoelectric polarization field aligned along the (0001) direction. If we assume a free-surface boundary conduction which means stress tensor $s_{zz} = s_3 = 0$, we obtain the following equations for piezoelectric polarization field P_{pz} along the z direction (the epitaxial growth direction) for a nitride alloy grown on strain relaxed GaN.

$$P_{pz,z} = 2(e_{31} - \frac{c_{13}}{c_{33}} e_{33}) e_1 = 2(e_{31} - \frac{c_{13}}{c_{33}} e_{33}) \frac{a_{GaN} - a}{a} \tag{2.4}$$

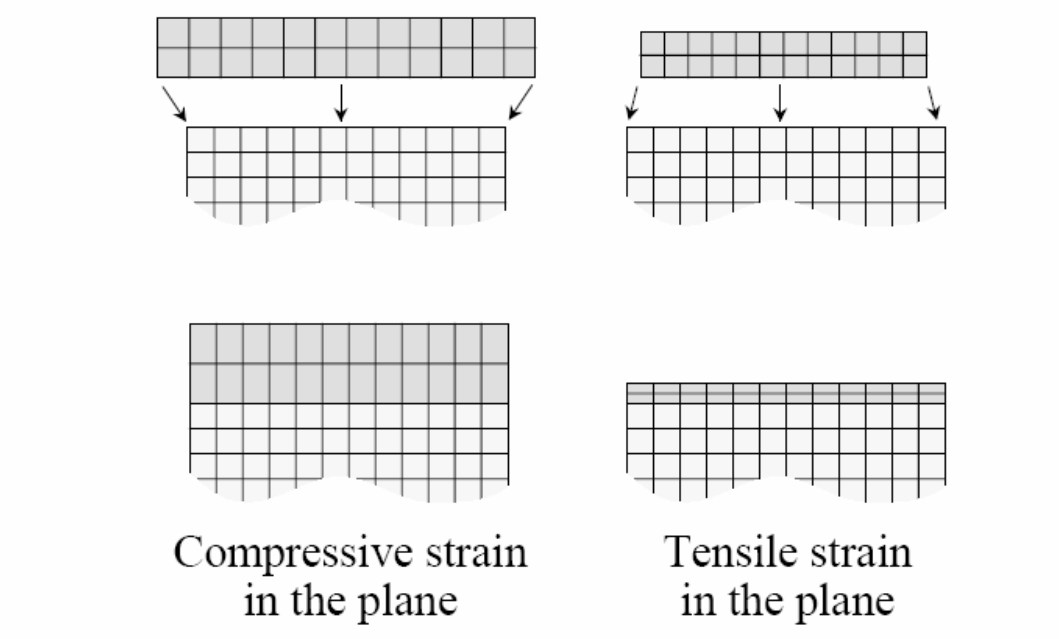


Figure 2.8: Schematic of compressive strain and tensile strain

The direction of the piezoelectric polarization depends on if the (0001) epitaxial film grown is under tensile or compressive strain. AlGaN grown on GaN have negative P_{pz} due to tensile strain, therefore P_{pz} is along the $[000\bar{1}]$ direction,; while InGaN grown on GaN have positive P_{pz} due to compressive strain therefore P_{pz} is along [0001] direction.

The spatial variation in the spontaneous and piezoelectric polarization fields will give rise to a polarization induced electrostatic charge density ρ_{pol}, the relation is described in the equation:

$$\nabla \bullet P = \nabla \bullet (P_{sp} + P_{pz}) = -r_{pol} \qquad (2.5)$$

This charge density will be present in heterostructures and it will influence internal electric field, electrostatic potential and mobile carrier distributions.

2.2 III-V Device Analysis and Device Modeling

TCAD simulation tools are valuable aids to perform device performance optimization and trend analysis on novel devices. Among several commercial available TCAD simulators, ISE-TCAD (now Synopsys_sentaurus) is capable of doing 2D and 3D device simulation which makes it a good choice for FinFET and TriGate MOSFET simulations. Another advantage of ISE-TCAD is it has Monte-Carlo simulator integrated in the TCAD bundle and therefore in addition to drift-diffusion, hydrodynamic model, Monte-Carlo simulation can be used to simulate 2-D device as well. Therefore in my device modeling and simulation study, ISE-TCAD is used to model several III-V based MOSFET devices.

2.2.1 InSb Quantum Well Transistor

Since 2004 Intel in collaboration with QinetiQ has successfully demonstrated 200nm and 80nm gate length “quantum well” transistors using indium antimonide. [18] [19] These InSb based transistors could become a promising candidate for making very fast microprocessors in the middle of the next decade. Therefore InSb based device simulation becomes important in device design and engineering for device performance optimization. However there are very few reports on InSb based device simulation so far, this study explores the InSb MOSFET simulation based on ISE-TCAD. We investigate the InSb based MOSFET device performance including turn on, turn off current, sub-threshold swing, DIBL, et al as gate length decreases.

InSb is a direct bandgap III-V material, its band structure is shown in Figure 2.6(a). Comparing with other semiconductors, InSb has the narrowest band gap (Eg= 0.17eV), low electron effective mass at the bottom of conduction band, and low hole effective mass at the top of valence band. At the bottom of conduction band, InSb has a very large non-parabolicity factor around 5 which deviates from the traditional parabolic model of the E-k relationship. [20] However the carrier concentration has less than one order of magnitude difference between the traditional parabolic model and the modified model considering of the parabolicity factor. [21] To simplify the simulation, in this work we use the traditional parabolic model for carrier concentration calculation. The density of states (DOS) at the bottom of conduction band and at the top of valence band is high as shown in Table 2.2. The intrinsic carrier density is also very high. Comparing with other semiconductor materials, the intrinsic carrier concentration of InSb is about six orders of magnitude higher than that of

Silicon, nine orders of magnitude higher than that of GaAs. This large number of minority carriers cause high junction reverse saturation current.

TABLE 2.2: InSb, Si and wurtzite GaN Material parameters

	Silicon	GaN	InSb
Bandgap Energy (E_g eV)	1.12	3.41	0.17
m_Γ (m_0)	0.98(m_l)	0.2	0.14
m_L (m_0)	0.19 (m_t)	N/A	0.25
m_{hh} (m_0)	0.49	1.1	0.43
m_{lh} (m_0)	0.16	0.3	0.015
Nc (cm^{-3})	$2.8x10^{19}$	$2.3x10^{18}$	$4.5x10^{18}$
Nv (cm^{-3})	$1.04x10^{19}$	$4.6x10^{19}$	$7.3x10^{18}$
Ni (cm^{-3})	$1.45x10^{10}$	~$1.0x10^{10}$	$1.9x10^{16}$

~Intrinsic Carrier concentration (Ni) for GaN is approximate for unintentionally doped GaN.
* material parameters are summarized from [3].

For InSb, the highest bulk electron mobility reported is 7.8×10^4 $cm^2V^{-1}s^{-1}$ and the highest hole mobility reported is 800 $cm^2V^{-1}s^{-1}$, this makes fast devices based on InSb possible. Several standard mobility models are used for InSb based devices. For high accuracy of simulation, we have to extract the model parameters from published data. The following several key model parameters are extracted and used in the device simulation:

1) Arora model [22] for electron mobility doping dependent effect.

$$m_{dop} = m_{\min} + \frac{m_d}{1+(\frac{N_i}{N_0})^{A^*}} \tag{2.6}$$

$$m_{\min} = A_{\min}(\frac{T}{T_0})^{a_m} \tag{2.7}$$

$$m_d = A_d(\frac{T}{T_0})^{a_d} \tag{2.8}$$

$$N_0 = A_N(\frac{T}{T_0})^{a_N} \tag{2.9}$$

$$A^* = A_a \left(\frac{T}{T_0}\right)^{a_a} \tag{2.10}$$

Where $N_i = N_A + N_D$ denotes the total concentration of ionized impurities, T_0=300K and T is the lattice temperature. All the other parameters are also accessible in the DESIS InSb parameter file. We use the curve fitting technique to extract the Arora mobility model parameters as shown in Table 2.3 for GaAs, wurtzite GaN and InSb. The basic idea is using the fitted parameters from both 77K and 300K curves [23] shown in Figure2.9, the total 8 independent parameters in Arora model can be calculated, for example from equation 2.7, we can get:

$$a_m = \log\left(\frac{m_{\min}}{A_{\min}}\right) / \log\left(\frac{T}{T_0}\right) \tag{2.11}$$

TABLE 2.3: Fitted GaAs, GaN and InSb Arora model parameters

	GaAs	GaN	InSb
$A_{min}(cm^2V^{-1}S^{-1})$	2136	88	-4140
α_m	-0.7457	-0.67	-0.4176
$A_d\,(cm^2V^{-1}S^{-1})$	6331	2200	$1.17x10^5$
α_d	-2.687	-4	-0.2528
$A_N\,(cm^2V^{-1}S^{-1})$	$7.345x10^{16}$	$1.25x10^{17}$	$1.0x10^{17}$
α_N	3.535	1.9	7.4462
A_a	0.6273	0.98	0.513
α_a	-0.1441	-0.15	0.2483

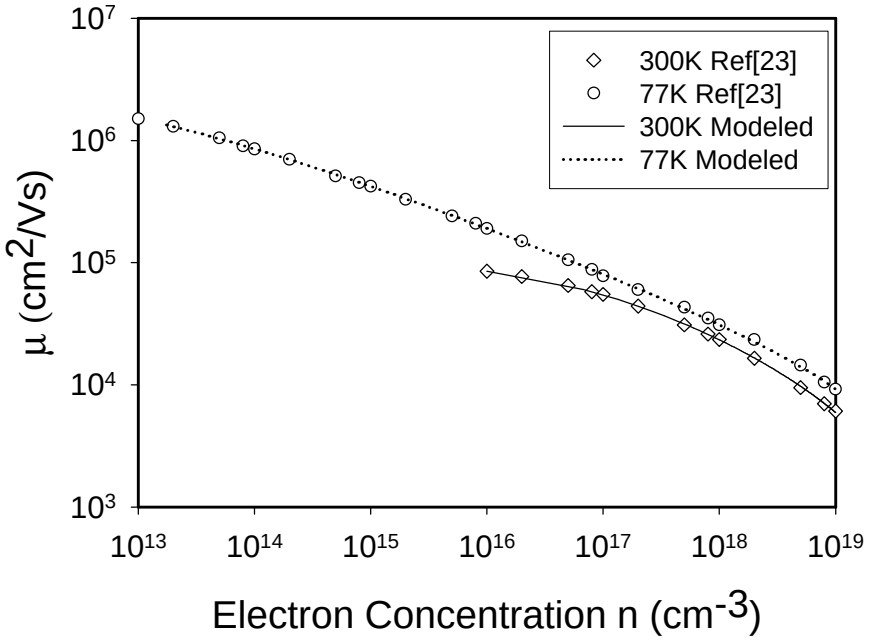


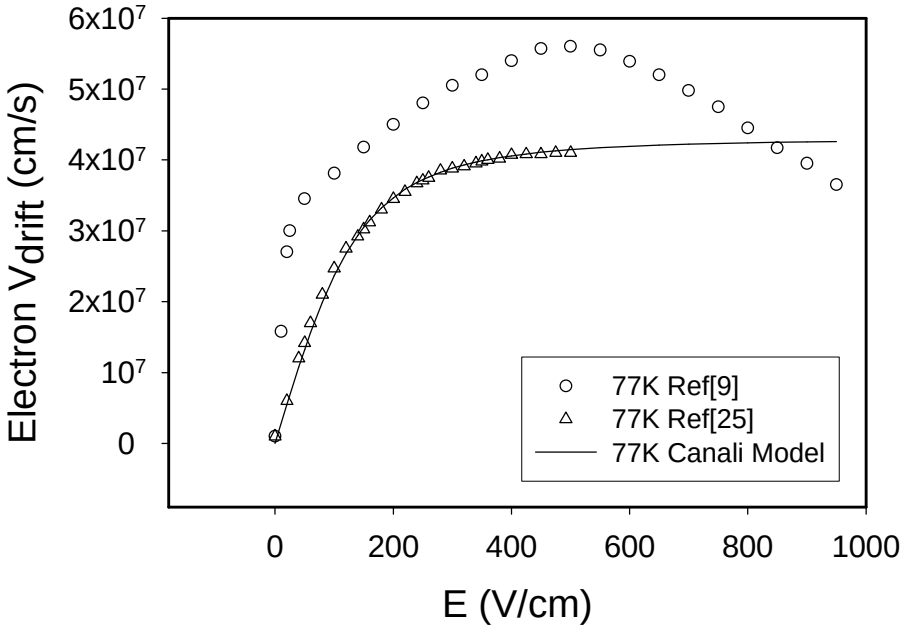
Figure 2.9: InSb Doping dependent electron mobility

2) Canali model [24] for electron mobility High field saturation.

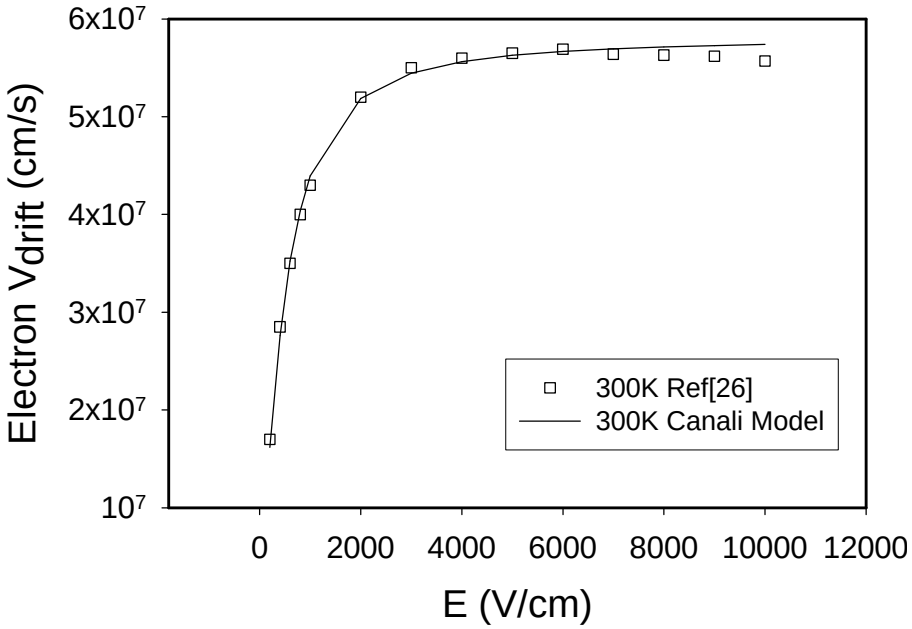
We use Canali model for InSb High field saturation as described by the following equations where m_{low} denotes the low field mobility, the exponent b is temperature dependent according to Eq. 2.13. The modeled high field saturation mobility is plotted with the published data at 77K [9] [25] and at 300K [26] in Fig. 2.10.

$$m(F) = \frac{m_{low}}{[1+(\frac{m_{low}F}{v_{sat}})^{b}]^{\frac{1}{b}}} \tag{2.12}$$

$$b = b_0(\frac{T}{T_0})^{b_{\exp}} \tag{2.13}$$



(a) 77K Bulk InSb drift velocity field dependent



(b) 300K Bulk InSb drift velocity field dependent

Figure 2.10: InSb electron velocity data and model at 77K and 300K

3) The mobility transferred electron effect model. [8]

The mobility transferred electron effect model is included to model the negative differential mobility for high driving fields. Adding transferred electron effect improves the accuracy of the mobility saturation model. However the transferred electron effect has not been observed on InSb QW transistor yet, therefore the model is not considered in modeling for the InSb based FET devices.

$$m = \frac{m_{low} + (\frac{v_{sat}}{F})(\frac{F}{E_0})^4}{1+(\frac{F}{E_0})^4} \tag{2.14}$$

4) Velocity high field saturation model. [8]

Both Canali model and transferred electron effect model assume the high field velocity saturation model as described in the following equation:

$$V_{sat} = A_{vsat} - B_{vsat}(\frac{T}{T_0}) \quad \text{for } V_{sat} > V_{sat,\min}\text{, otherwise } V_{sat} = V_{sat,\min} \tag{2.15}$$

All the high field saturation model parameters are listed in the following table 2.4.

TABLE 2.4: GaAs, GaN and InSb High field saturation model parameters

	GaAs	GaN	InSb
$\mu_{low}(cmV^{-1}s^{-1})$	8500	1000	78000
β_0	2	1.7	2
β_{exp}	0	0	0
A_{vsat}	$1.35x10^7$	$2.1x10^7$	$5x10^7$
B_{vsat}	$3.6x10^6$	0	0
E_{0_Tref} (V/cm)	4000	$1.5x10^5$	500
V_{satmin} (cm/s)	$5x10^5$	$1.5x10^7$	$3x10^7$

5) Auger recombination

Auger processes are important for narrow band gap materials where activation energy is low, and the Auger recombination and generation therefore are relatively easy to occur at nominal device operation condition. High Auger generation and recombination is another main reason that InSb based device has high leakage current. Auger recombination is implemented in ISE-TCAD using the standard Shockley-Read-Hall (SRH) recombination model. The standard SRH recombination is implemented in DESSIS with the doping dependence and trap assisted tunneling effect.

6) InSb tunneling effect

Band-to-Band tunneling is another reason that could cause the leakage current. Due to narrow band gap, even at the moderate doping of the p-n junction, one would expect substantial tunneling current. The band to band tunneling is modeled as an Recombination-Generation process, according to [27].

$$R_{bbt} = -\frac{1}{q}\nabla \cdot J_{bbt} = -\frac{1}{q}\frac{dJ_{bbt}}{dy}\cdot \nabla y = -\frac{dJ_{bbt}}{dE}\cdot F \tag{2.16}$$

Here the R_{bbt} is the band to band tunneling contribution to the recombination. J_{bbt} is the band to band tunneling current density. ψ is the electrostatic potential. E is the carrier energy. F is the force on the carrier.

$$R_{bbt} = -B\,|F|^{s}\; D(F, E, E_{fn}, E_{fp})e^{-F_0/|F|} \tag{2.17}$$

For direct band transition s =2, for indirect band transition, s =5/2 to include electron-phonon interactions. B and F_0 are material dependent parameters. Their values for InSb are determined according to Kane's model [28]. D is a function that accounts for the relative position of the electron and hole Fermi levels in the neutral regions (region $x_n<x<x_p$

in Fig. 2.11) and the influence of perpendicular electron motion on tunneling probability [29]. In forward bias, it accounts for the well known peak in the tunneling current observed in an Esaki diode. An expression of D (F, E, E_{fn}, E_{fp}) which is valid in zero and reverse bias and which is suitable for implementation in a device simulator can be obtained from. [21] The function virtually equals zero for x<xn in Fig.2.12, because in this region there are no final states into which an electron can tunnel. For x>xp, this function also equals zero because there are no initial states from which electrons can tunnel. For xn<x<xp or equivalently, when the tunneling energy E1 lies between E_{fn} and E_{fp}, this function equals unity.

$$D(y, E_{fn}, E_{fp}) = \frac{1}{e^{(-E_{fp}-qy)/kT}+1} - \frac{1}{e^{(-E_{fn}-qy)/kT}+1} \qquad (2.18)$$

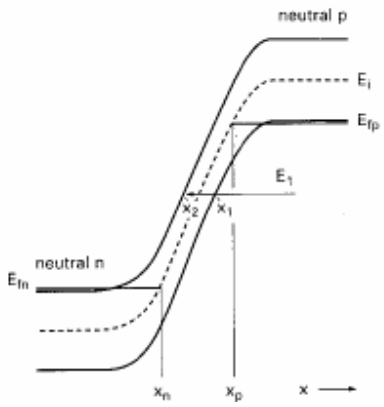


Figure 2.11: Schematic of energy band diagram of a reverse-biased p-n junction. The Band to band tunneling mechanism is indicated

Hydrodynamic mode of transport equations [30] [31] in DESSIS of ISE-TCAD [8] are used to account for energy transport of carriers. The device self heating effect is also simulated by including the thermodynamic model. [32] To study the inversion layer quantization effect, the Quantum model 1-D density gradient model is used. [33] [34]

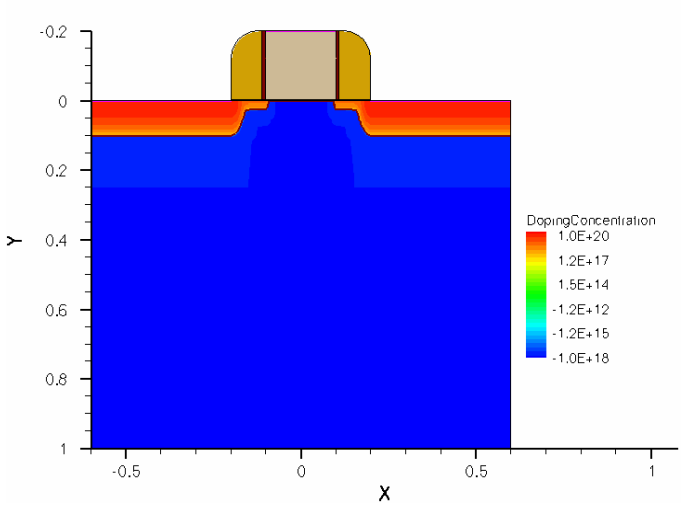


Figure 2.12: InSb Planar MOSFET structure in TCAD

Fig. 2.12 shows the InSb based planar NMOS transistor. The substrate is p type doped with a constant doping profile and the doping concentration is 1×10^{18} cm^{-3}, the source/drain is n type doped with a Gaussian distribution and the peak doping concentration is 1×10^{20} cm^{-3}, the extension junction is n type doped with a Gaussian distribution and the peak doping concentration is 5×10^{18} cm^{-3}. We use the aluminum as metal gate where the metal work function is 4.75 eV. We assume idealized InSb devices with 1nm gate oxide thickness.

The scaling effect of InSb based planar MOSFETs have been simulated, the drain current versus gate voltage at 1 volt drain bias is shown in Fig. 2.13. In the device models, the Arora mobility model, Canali mobility high field saturation model, and velocity saturation model are included. Theoretically, for InSb based devices, transferred electron effect model is needed for more accurately mobility modeling, the L valley at the bottom of conduction band is the satellite band giving the negative differential mobility, and the E_L =0.68 eV is very low comparing to other III-V compound semiconductors so the critical field for electrons to start transferring from Γ valley to L valley is relatively low as shown in Fig.

2.6 (a), so the negative resistance should occur at relatively low field which is simulated for a InSb NMOS transistor with gate length of 200nm as shown in Fig. 2.14. However the transferred electron effect has not been observed on InSb QW transistor yet, therefore the transferred electron effect model is not considered in the electron mobility models for the InSb based FET devices in this work. The Fig. 2.15 shows the simulated output characteristics of the same InSb NMOS transistor without the transferred electron effect.

Another advantage of InSb based MOSFET is the high current driving capability shown in Fig. 2.15 where the drain current of InSb NMOS is almost three times as high as the drain current of Si NMOS of InSb MOSFE due to the high mobility of InSb.

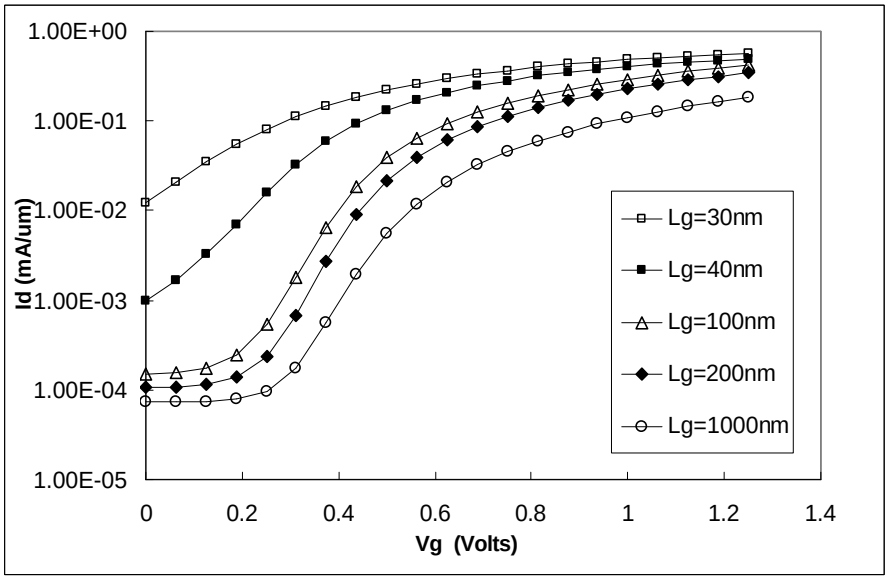


Figure 2.13: Id vs. Vgs for InSb Planar MOSFET Canali model

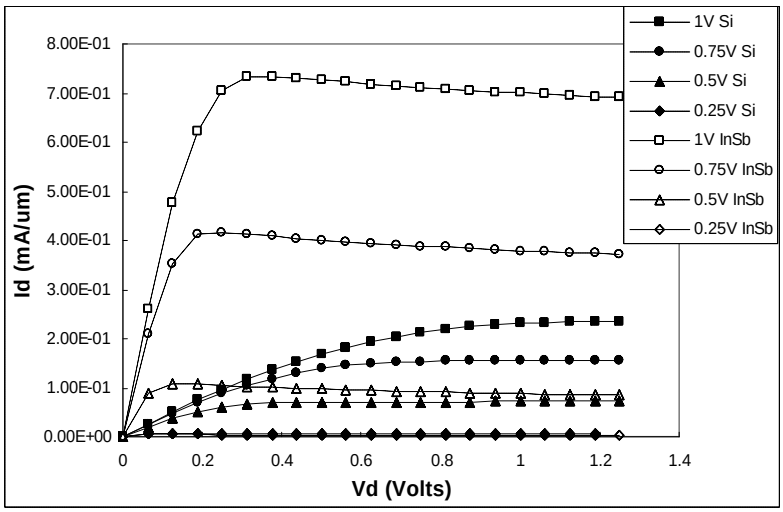


Figure 2.14: Id vs. Vd for InSb Planar MOSFET Canali model with transferred electron effect.

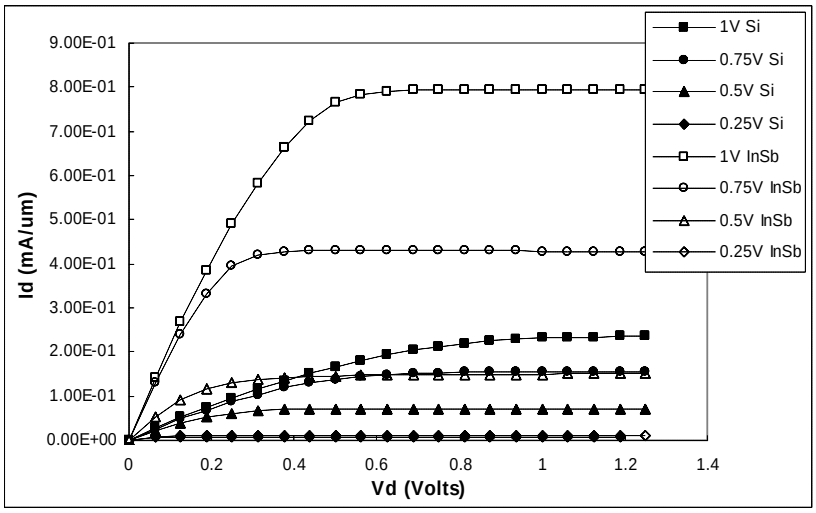


Figure 2.15: Id vs. Vd for InSb Planar MOSFET Canali model.

The silicon based devices are also simulated for comparison, where we used the standard Philips unified mobility model [35] which is available and has been calibrated in ISE-TCAD. Both off state leakage current and turn on current of InSb MOSFETs is much higher than that of silicon devices as shown in Fig.2.16. The high turn on current is due to high mobility of InSb. High off state leakage current however is because InSb has large

intrinsic carrier density (n_i =1.9×10^{16} cm^{-3}) which is six order of magnitude higher than that of silicon. Several techniques have been demonstrated to reduce leakage current of InSb based devices, such as exclusion and extraction [36], electromagnetic carrier depletion [37], low temperature operation etc. From Fig.2.16, both leakage current of Si and InSb devices increase as the device scales down, but leakage current for InSb NMOS shows a less increasing rate than silicon NMOS as the device scales, which shows the InSb devices might have the similar leakage current as silicon device in sub 50nm regime. A traditional method to reduce off state leakage current of InSb device is device cooling as shown in Fig.2.17. At 200K the InSb NMOS has more than two orders of magnitude less leakage current

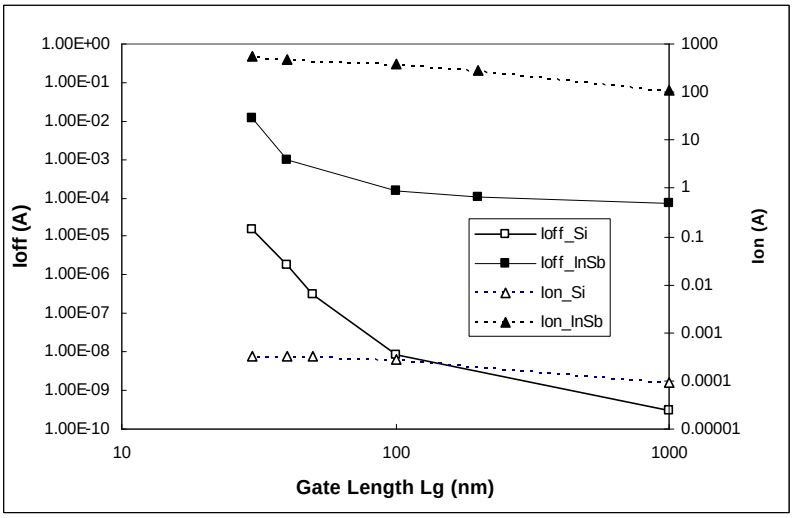


Figure 2.16: Off state leakage current/turn on current of InSb NMOS and Si NMOS

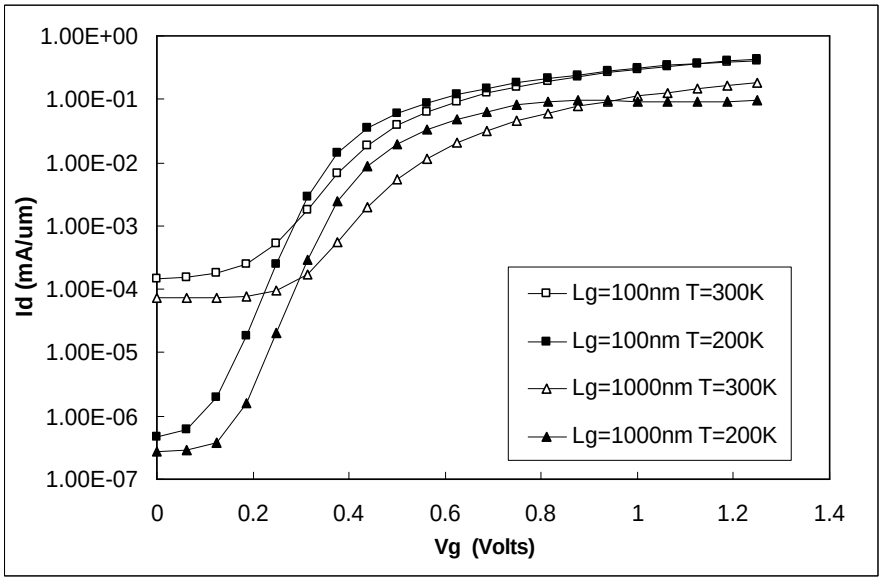


Figure 2.17: Id/W vs. Vg for InSb NMOS at 200K and room temperature

Fig.2.18 shows the DIBL and transconductance affected by device scaling for both InSb and Si. The InSb devices have larger DIBL for sub 100nm device sizes, and have similar transconductance as their Si counterparts. Fig.2.19 shows InSb devices have larger sub-threshold swing than their silicon counterparts and the sub-threshold swing degradation with device sizes. The threshold roll-off as device scales down seems have similar effect for both InSb devices and Si devices.

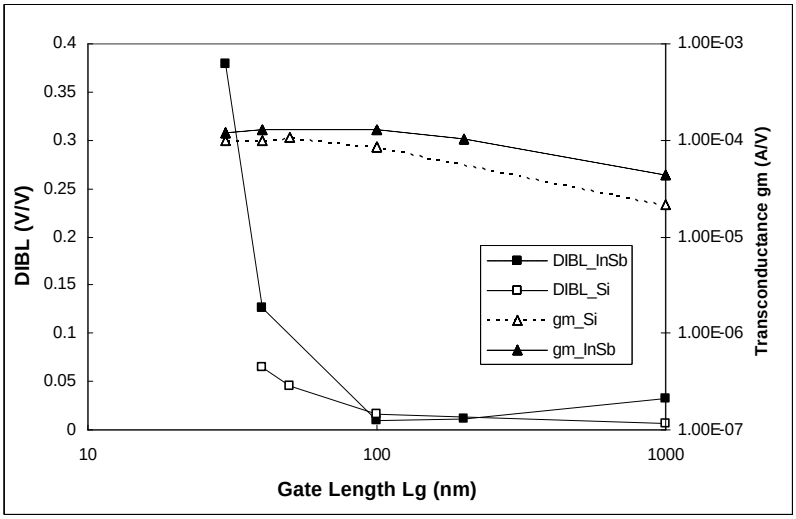


Figure 2.18: DIBL and transconductance of InSb and Si NMOS

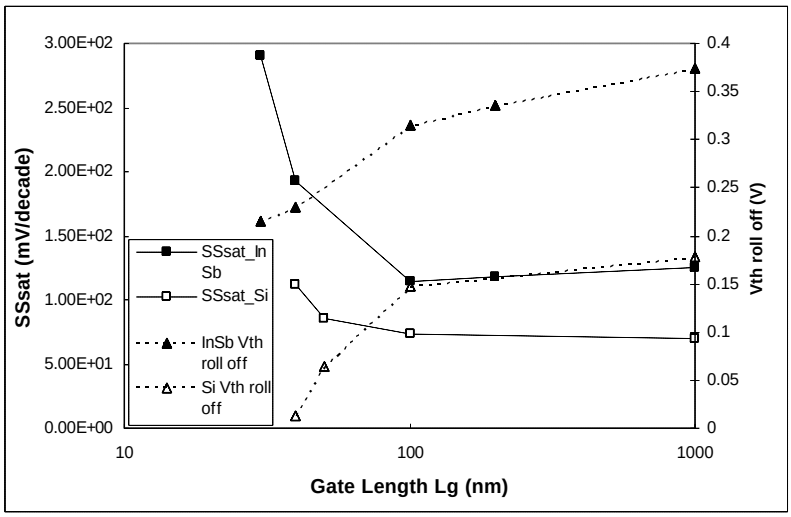


Figure 2.19: Subthreashold swing and threshold voltage roll off

To summarize, we presented a device modeling and simulation approach for InSb based MOSFET devices. The InSb experimental data reported in literature have been evaluated to serve as the basis of the InSb device physics model such as InSb bandgap narrowing, carrier doping dependent mobility, field dependent mobility, high field velocity saturation and transfer electron effect. Hydrodynamic (HD) transport model is used for device simulation to account for non-equilibrium carrier dynamics. 1D density gradient

approximation for quantum mechanical effect is also considered in the simulation. Other effects such as Impact ionization, tunneling, trap, self heating, et al. are considered in the device model. InSb physics based models are developed and InSb based devices such as planar MOSFET and Silicon on insulator (SOI) MOSFET is simulated using device simulator ISE-TCAD. Our study shows that InSb based MOSFET is a promising device for low power high speed applications.

2.2.2 GaN MOSFET

Silicon MOS transistors have been scaled down for over 30 years, and the gate length has reached sub-60nm in products and 5nm in the research level. Several different silicon on insulator (SOI) structures such as FinFET [38, 39], Trigate [40, 41], and Omega-field-effect transistor (OFET) [42, 43] devices have been receiving attention as potential device candidate for nanoscale silicon MOSFET. The FinFET structure we studied in this work is one type of vertical double gate SOI structure, the channel is surrounded by the two thin layer of oxide as gate oxide and the top thick layer of insulator as shown in Fig. 2.20. The TriGate structure is also called triple gate structure looks like FinFET but the top gate oxide is also very thin so the channel is surrounded by three oxide layers as shown in Fig. 2.21. The Omega-FET is the structure where the channel can be further wrapped around by the gate oxide layer, the extreme case of the OFET structure is the cylindrical channel fully wrapped around by the gate oxide as shown in Fig. 2.22. The triangular channel MOSFET structure is on kind of double gate SOI structure, but the cross section view of the channel is not in a traditional rectangular shape but in the triangular shape as shown in Fig. 2.23. All of the SOI structures mentioned here have been proposed before and the simulation work has been done

individually. Some of the SOI device structure comparison has been studied. However there has not been a study to compare all these different SOI device structures together for device optimization.

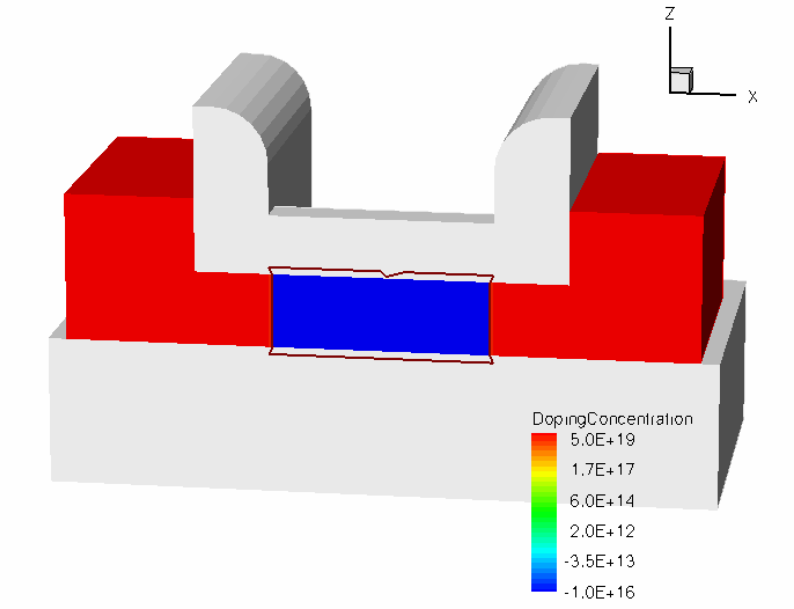


Figure 2.20: The FinFET MOSFET structure

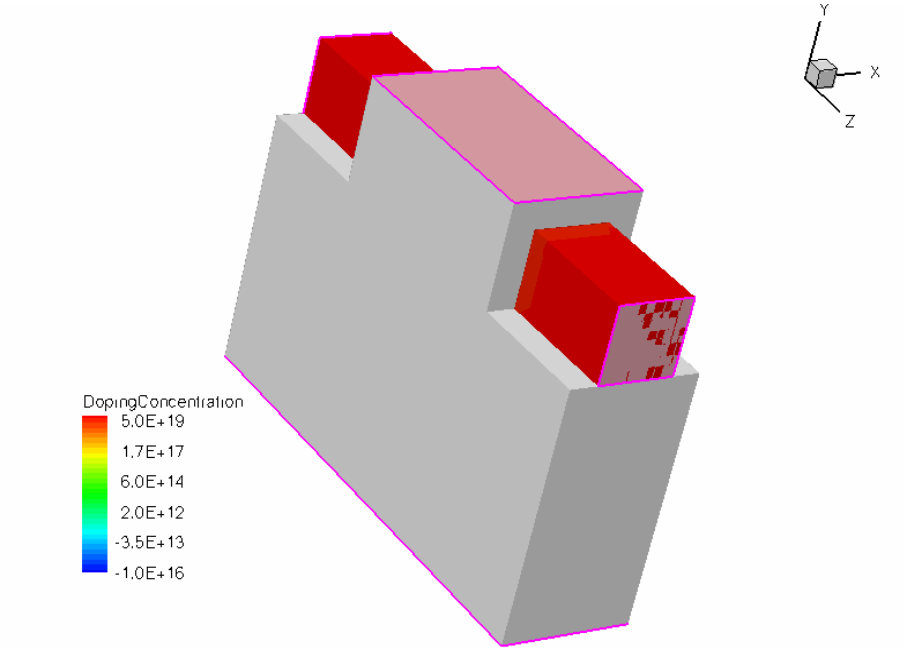


Figure 2.21: The Tri-Gate MOSFET structure

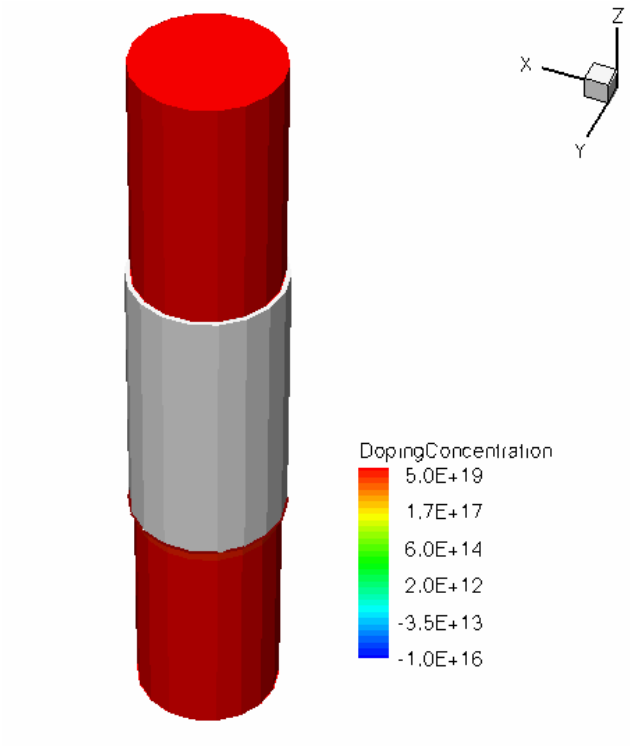


Figure 2.22: The OMEGA Gate MOSFET structure

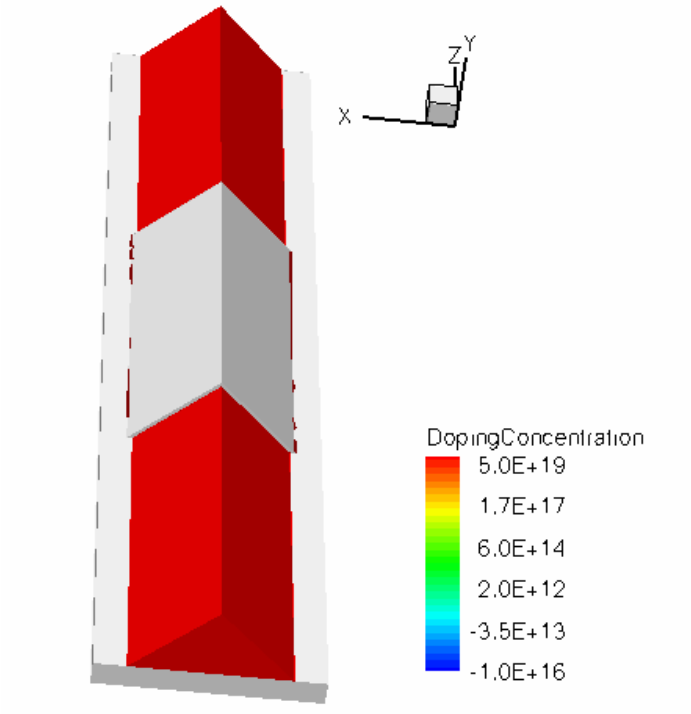


Figure 2.23: The Triangular channel MOSFET structure

GaN has been the topic of intense research and development activities during the past years. The progress in GaN has demonstrated successful devices such as GaN based HFET, and more importantly GaN based MOSFET [44]. While the wide-band gap of GaN, the high critical electric field, high thermal conductivity, high electron mobility and saturated electric velocity make GaN useful for high power, high frequency semiconductor devices. These properties of GaN also make GaN based MOSFET potential candidate for low power, high frequency applications. Therefore GaN based MOSFET is modeled and simulated in this study to compare with the silicon based MOSFET.

In this work, we simulated silicon and GaN based sub-100nm gate length SOI devices, the device performance and characteristics such as saturation current, off state leakage current, threshold voltage, sub-threshold swing and drain induced barrier lowering (DIBL)

are compared through the above SOI structures. Silicon and GaN as channel materials are also compared for these different SOI structures for projecting the device performance for very short channel SOI MOSFETs.

For both silicon and GaN based devices we have studied, we use p-type substrate with a doping concentration of 1×10^{16} (cm^{-3}) and n-type source/drain with a doping concentration of 5×10^{19} (cm^{-3}). We use aluminum as the gate metal with the work function of 4.75 eV. The gate oxide thickness is set at 1nm. The hydrodynamic mode of transport equations in DESSIS of ISE-TCAD are used to account for energy transport of carriers. The device self heating effect is also modeled by including the thermal-dynamic model. To study the inversion layer quantization effect, the Quantum model 1-D density gradient model is used. For Si based MOSFET, we use the Philips unified mobility model [45] which was initially used primarily for bipolar devices, and later on it is widely used for MOS devices and is well calibrated in ISE-TCAD simulator [8]. For GaN based MOSFET, we use Arora mobility model, with Canali model as high field saturation model to account for the high saturation field and velocity of GaN bulk material. The detailed method of device modeling is the same as the approach for InSb MOSFET modeling described in last section, and the GaN model parameters are listed in table 2.3, and table 2.4.

The silicon based SOI devices are simulated using the TCAD simulator DESSIS. The simulated FinFET has a 10nm H_{fin}, and 40nm T_{fin}. H_{fin} is the height of the Si fin, it is defined as the distance between the top gate to the substrate oxide. T_{fin} is the thickness of the Si fin, it is defined as the distance between the front and back gate. The channel width is therefore $2\times H_{fin}$. The device current is normalized to the channel width. As a validity check of the simulation result, the simulated Si FinFET results agree well with the published FinFET with

60nm gate length [46] [47] considering that the different oxide thickness and different gate metal have been used in this work.

The following Figure 2.24 shows the Id-Vg curves at Vds =1V of several SOI MOSFETs with the gate length of 45nm. The multiple SOI structures have all shown better sub-threshold slope than planar non-depleted MOSFET. The triangular channel MOSFET from the simulation seems also a good candidate for better control of the sub-threshold leakage current. One of the figure of merit (FOM) of digital device is Ion/Ioff ratio, as seen in Figure 2.25, the triangular channel MOSFETs simulated have demonstrated larger Ion/Ioff ratio for above 20nm gate length devices. All MOSFETs show very low Ion/Ioff ratio as device scales down to sub-20nm. Quantum effects have to be taken into account for accurately simulation of device performance beyond this 20nm node. Figure 2.26 shows the threshold voltage roll off due to device scaling. As shown here, the multiple gate devices have the benefit of better control the threshold voltage roll off and less device performance variations due to processing variations. Triangular channel MOSFETs also demonstrated comparable threshold roll off among the other SOI structures. Figure 2.27 shows the transconductance of triangular channel MOSFET is lowest among all the MOSFET structures.

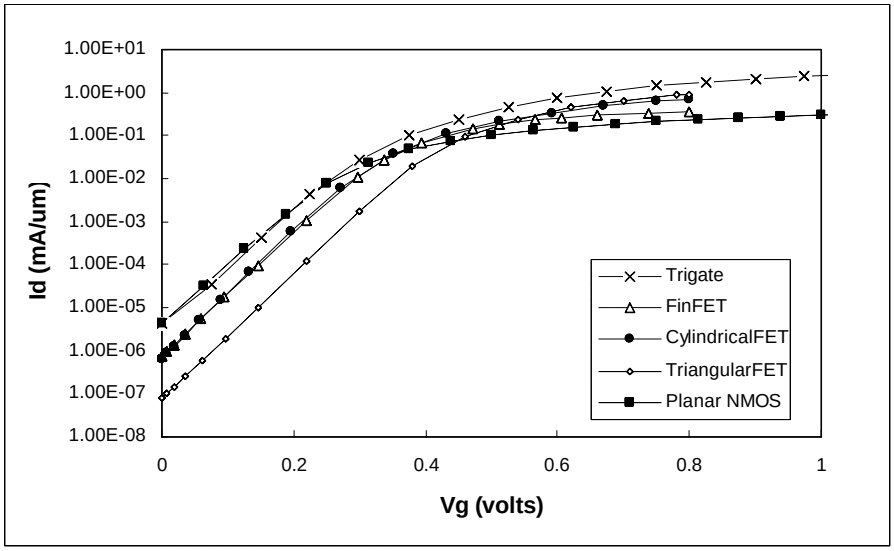


Figure 2.24: The Id vs.Vg for gate length of 45nm MOSFETs

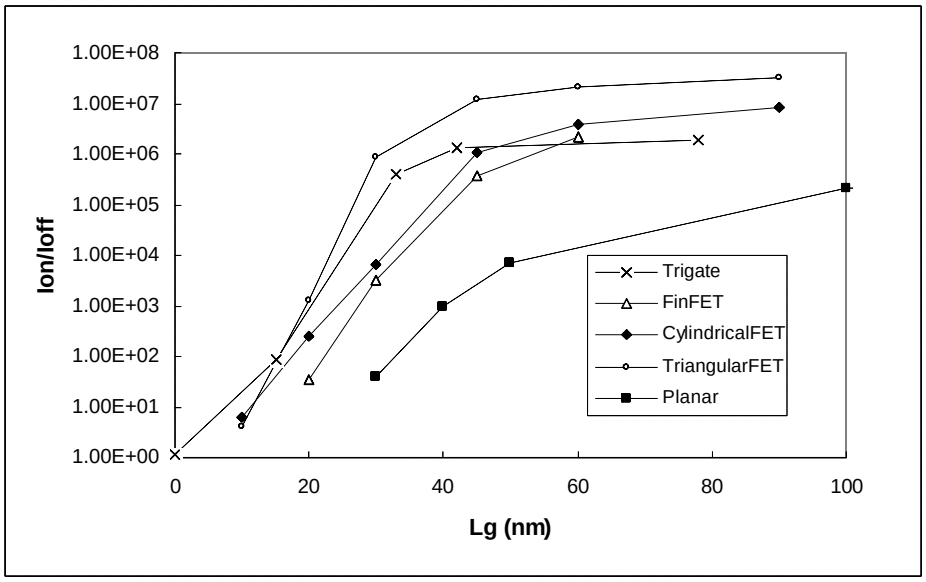


Figure 2.25: The I_{on}/I_{off} ratio vs. gate length for several Si SOI MOSFET structures

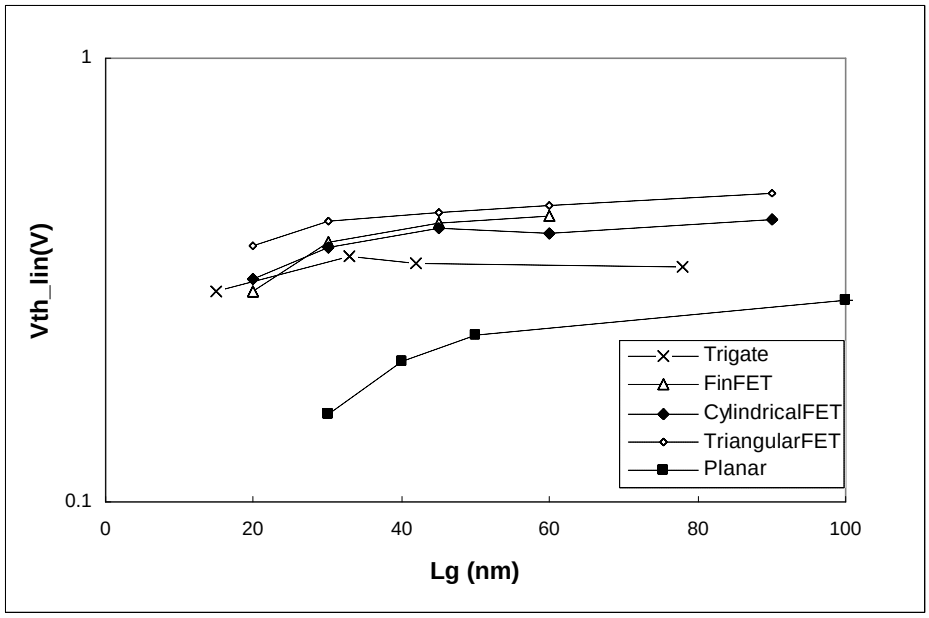


Figure 2.26: The threshold voltage vs. gate length for several Si SOI MOSFET structures

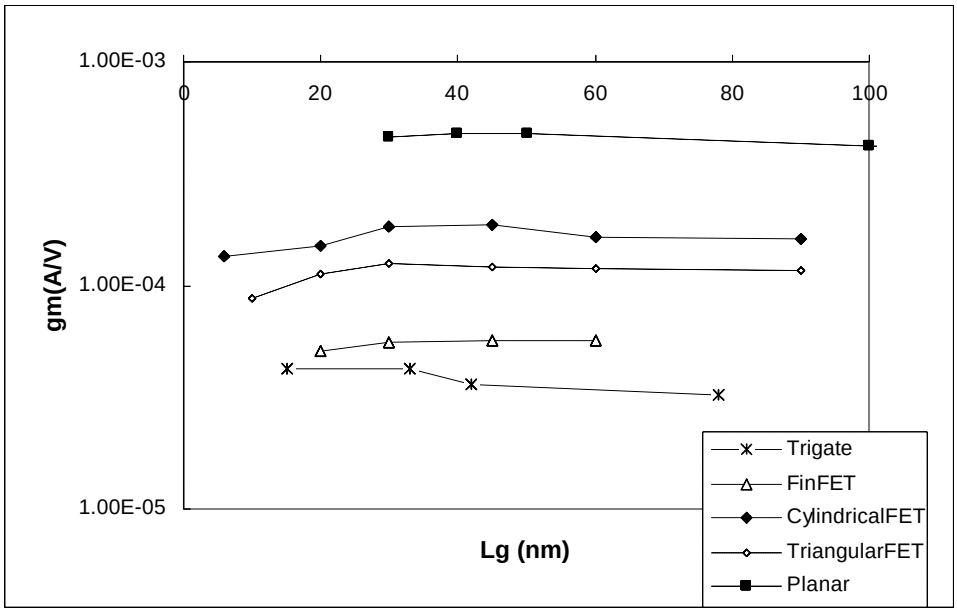


Figure 2.27: The Transconductance vs. gate length for several Si SOI MOSFET structures

The GaN based SOI devices are modeled and simulated, the following Figure 2.28 shows the Id-Vg curves at Vds =1V of several SOI MOSFETs with the gate length of 45nm. Comparing the multiple silicon SOI structures and GaN based SOI structures. We find the

GaN triangular channel MOSFET shows better sub-threshold slope and low off state leakage current. From figure 2.29, in general, for low dimensional devices, GaN based MOSFETs have all shown better I_{on}/I_{off} ratio than Si based MOSFETs. The lower I_{off} is because GaN has larger band gap, lower intrinsic doping concentration and lower minority carrier concentration, all these lead to lower junction leakage current which is the major concern for short channel devices. GaN device has lower I_{on} than Si device for longer gate length, this is because here we assume the electron mobility in bulk GaN can achieve 1000 cm^2/Vs which is less than electron mobility in bulk Si. We believe as processing technology advances, electron mobility in GaN MOSFET can also increase. As device scales down, the junction leakage contribute more to I_{off} than the mobility to I_{on}, therefore the FOM I_{on}/I_{off} ratio of GaN is better than Si as we simulated. The threshold roll off and small signal transconductance of GaN based MOSFETs show similar characterization with silicon based MOSFETs, and therefore we are not going to show them in the paper but the GaN based MOSFETs show larger transconductance. Using I_{on}/I_{off} = 10000 as a critical ratio for digital applications, beyond 20nm gate length, silicon based MOSFETs are not satisfying this requirement and GaN based MOSFETs with much better I_{on}/I_{off} ratio are potential candidates for future generation digital devices.

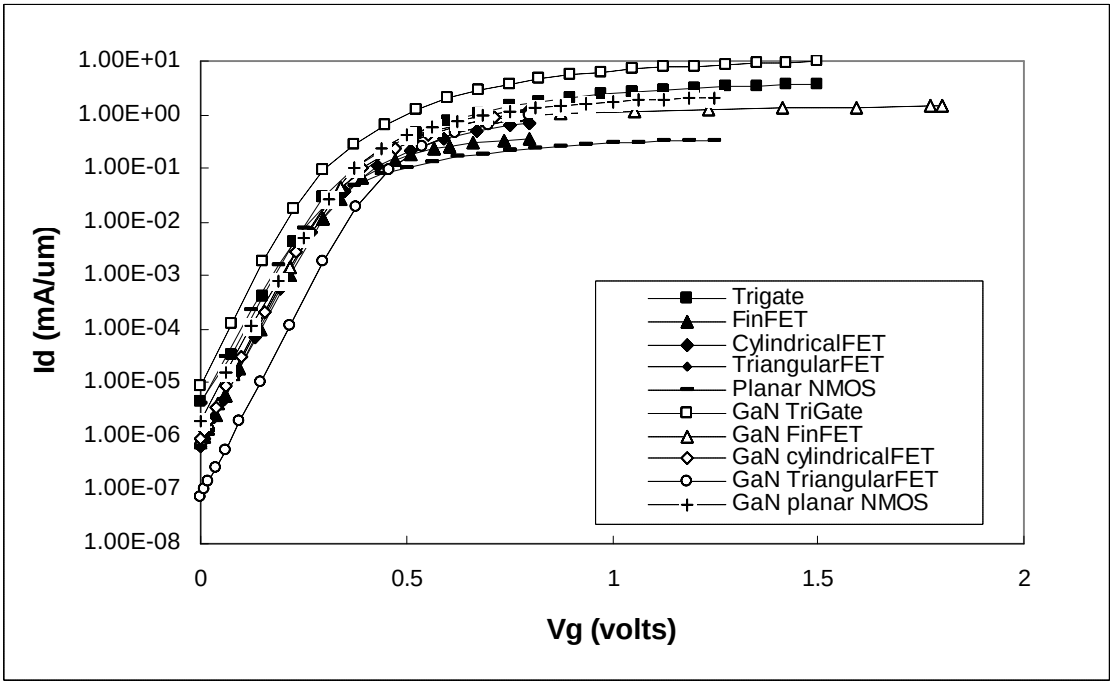


Figure 2.28: The Id vs. Vg for gate length of 45nm MOSFETs for several Si and GaN SOI MOSFET structures

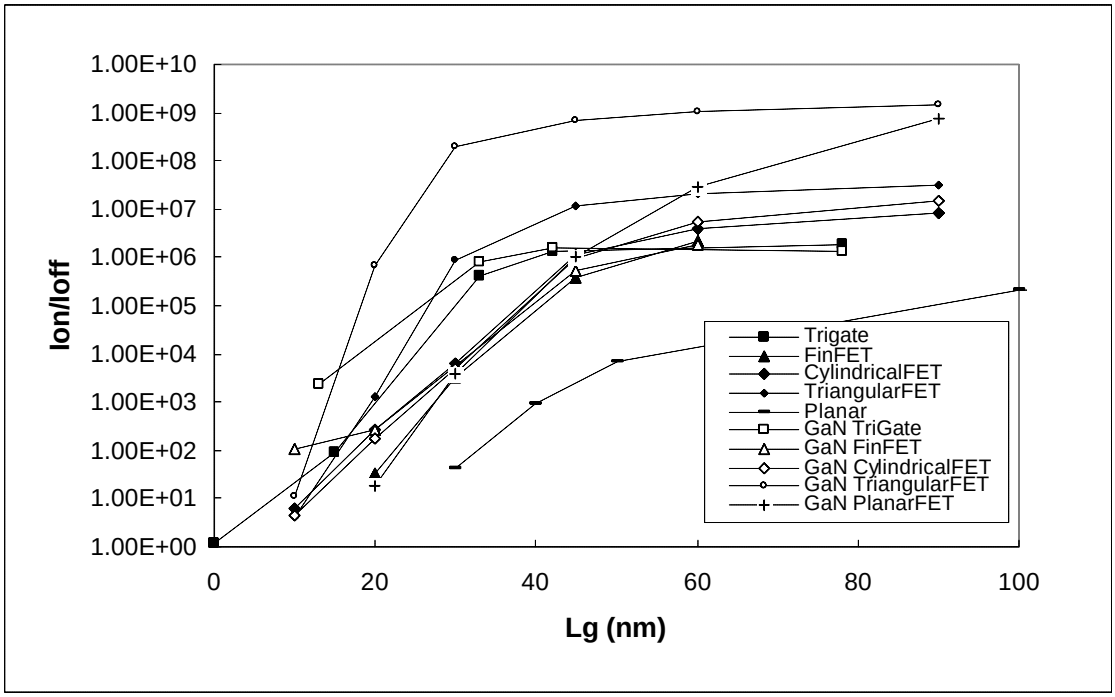


Figure 2.29: The I_{on}/I_{off} ratio vs. gate length for several Si and GaN SOI MOSFETs structures

In conclusion, Sub-100nm gate length silicon and GaN based SOI n-type MOSFET are modeled and simulated using ISE-TCAD. Several silicon SOI structures such as planar fully depleted SOI, FinFET, Tri-Gate MOSFET, cylindrical channel (OMFET) and triangular channel MOSFETs have been studied to compare the structure dependence of the device performance. Silicon and GaN as channel materials are also compared for these different SOI structures for projecting the device performance for very short channel SOI MOSFETs. Our study shows that for sub-100nm gate length, GaN based transistors have better Ion/Ioff ratio and higher small signal transconductance than silicon based transistors. And GaN and Si based devices have comparable performance such as sub-threshold slope and threshold roll off, etc. However for sub 20nm gate length, the simulation results show that while it is not satisfying for silicon based device for digital applications, GaN based transistors have lower off state leakage current, less short channel effect than Silicon based transistors. Therefore they are good candidates for future generation digital applications. The TCAD study shows that GaN could be a promising candidate for making short channel device as the GaN processing technology is advancing.

2.3 Summary

In this chapter, the relevant semiconductor device physics are introduced first, the special properties of GaN such as two kinds of crystal structure, band structure, transport properties and polarization are briefly discussed. Several III-V devices are modeled using TCAD simulation tool. The device modeling procedure is discussed in detail for InSb based MOSFET and the study shows that InSb based MOSFET might be a promising candidate for

low power application. The Si based SOI structures are simulated using TCAD and compared for device structure optimization. Then GaN based MOSFET and several GaN based SOI devices are simulated to compare with their Si counterpart. The study shows that GaN based MOSFETs can be promising candidate for making short channel device as the GaN processing technology is advancing.

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Chapter 3

GaN Source/Drain Techniques, Metal-GaN Schottky Contact and GaN Wet Etch Study

This chapter starts with the introduction of the source/drain techniques for GaN based MOSFETs with the emphasis on the regrown source/drain and Schottky metal source/drain. The source/drain formation processes are compared and the metal liftoff to pattern the source/drain is selected. The ungated GaN MOSFET structure also called n-i-n structure is fabricated as a testing structure in the middle of GaN Schottky barrier MOSFET device processing steps. The n-i-n testing structures with regrown source/drain and Schottky metal source/drain are characterized and also modeled using TCAD. The metal-GaN Schottky barrier height has been reviewed. Finally the GaN wet etch techniques are reviewed and GaN binary etch is explored.

3.1 GaN Source Drain Regrowth

A significant limitation in the fabrication of GaN MOSFET relates to the formation of ohmic contacts for MOSFET structures. A MOSFET in either accumulation or inversion mode requires low free carrier concentrations for the semiconductor channel to have a low

off-state current. Unfortunately, a low free-carrier density substrate is problematic for the formation of ohmic contacts, a problem usually dealt with in silicon MOS through self-aligned ion implantation. For GaN MOSFET, however, the high annealing temperatures (1100°C-1500°C) associated with activating implanted dopants to substitutional sites limits the use of ion implantation for III-N MOSFET fabrication [1][2]. The high activation temperature not only roughens the GaN surface and makes it difficult to grow high quality oxide, but also set a very high thermal budget on GaN MOSFET device processing. Therefore to minimize the high thermal budget in GaN MOSFET processing, several other methods to achieve carrier rich source/drain excluding ion implantation have been investigated in 2006.

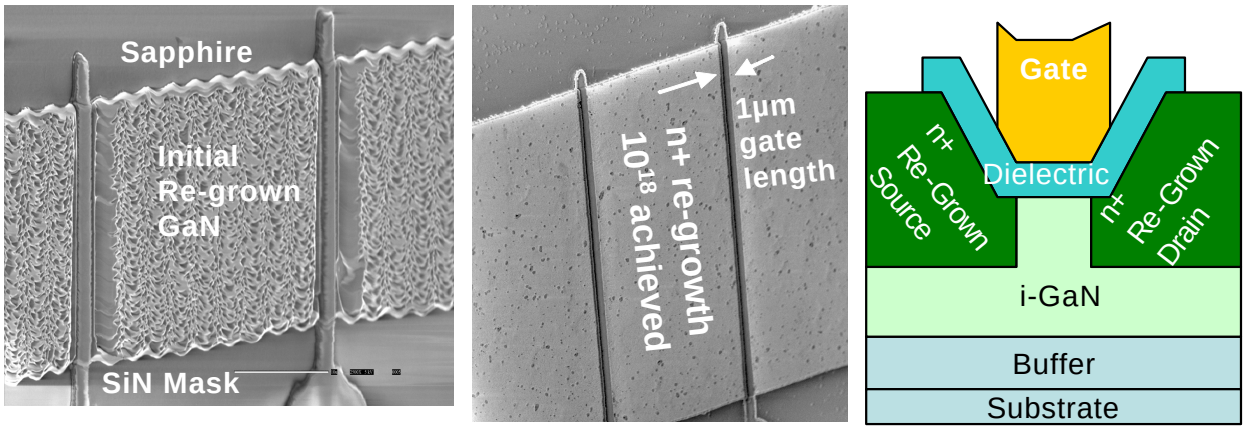
F. Ren's group and S. J. Pearton's group at University of Florida in collaboration with C. J. Pan et al. at National Central University in Taiwan and P. Bove, et al. at Picogiga International SAS in France have demonstrated a GaN MOSFET with the source/drain formed by Si thermal diffusion at temperature range from 800°C to 1000°C. The device demonstrated a maximum drain current of 35μA/mm and maximum transconductance of 7μS/mm at V_{ds}=7V. The calculated diffusivity was faster than in the implanted GaN indicating the promises of using thermal diffusion to form the source/drain for GaN MOSFET [3].

Our group collaborating with Dr. Mark Johnson's group in Dept. of Material Science and Engineering at NCSU has explored the alternative methods to achieve carrier rich source/drain for GaN MOSFETs. We have successfully demonstrated the n^+ GaN source/drain regrowth for GaN MOSFET application [4-6]. The GaN MOSFET and MISFET processing starts with intrinsic GaN film grown on sapphire. The source/drain regions are

identified by the photolithography process followed by lift-off and reactive ion etching using Cr-Ni mask. The thickness to determine the etch stop is measured by Dektak profilometer and the metal etch is performed to remove the Cr-Ni mask. The structure is then ready for source/drain regrowth and it is transferred to the MOCVD reactor. Then highly doped n+ GaN regions are selectively grown on the recess regions. The Si_3N_4 layer grown earlier was used as a selective mask. The re-growth was done at various temperatures and the morphology was optimized by precursor flow. Morphology, before and after re-growth, was examined by JEOL JSM 6400 scanning electron microscopy at 5kV. Si_3N_4 layer was removed with 10% HF and a 300A of gate dielectric was deposited. The contact regions were also identified by the photolithography process followed by a Ti-Al-Mo-Au ohmic metal deposition using e-beam and lift off. The resistivity of the re-growth region was lower than 2×10^{-4} ohm-m for a silicon doping concentration of $\sim5\times10^{18}/cm^3$.

Fig. 3.1 shows the SEM images of the initial regrowth, the optimized regrowth and the schematic diagram of the final device cross-section. The initial attempts demonstrating capacity for selective re-growth is shown in (a). Selectivity was demonstrated but it lacked sufficient uniform morphology for device demonstration. The morphologies of non-uniform nucleation in Figures 3.1(a) resemble that of a similar growth performed by Suda *et al.* using MOMBE at 800^oC which resulted in cubic GaN [7]. For re-growth to occur there should be a GaN template material in the recess. Hence, the etch stop during the recess etch is a very important step in device processing. The process was optimized to deliver uniform morphology re-grown contacts as indicated in the middle SEM graph (b). This study also agrees with a re-growth of GaN on etched GaN templates by He *et al* using plasma MBE

where a lowering of temperature enhanced coalescence and uniform growth [8]. The schematic diagram of the final MOSFET made utilizing these contacts is shown in (c).



(a) (b) (c)

Figure 3.1: SEM images of the initial regrowth (a), the optimized regrowth (b), and the schematic diagram of the final GaN MOSFET (c).

3.2 Metal Source Drain for MOSFET

Another important alternative method to achieve carrier rich source/drain for MOSFET is using metal to form Schottky barrier source/drain, this idea has been applied to Si MOSFET for about 40 years [9] [10] and it is attracting more research interests [11-16] for aggressively scaled Si MOSFET.

The metal source drain Schottky barrier MOSFET (SB-MOS) was first investigated by Nishi in 1966 when he submitted a Japanese patent on the idea [9]. In 1968, Lepselter and Sze published the first paper on the topic focusing on a PMOS bulk device employing PtSi for the S/D regions.[10] This PMOS has poor performance with room temperature drive current ten time lower than a conventional MOSFET. In 1981, Koeneke showed how the

lateral gap between the edge of the S/D electrodes and the gate electrodes strongly affects the drive current of the device, with a smaller gap resulting in significantly higher performance.[17][18] Later in 1980s, a variety of Schottky barrier MOS device structures were studied, including the first Schottky barrier NMOS by Mochizuki and Wise [19], devices employing interfacial doping layers between the metal S/D and the channel [18][20][21] and asymmetric devices in which the source is metal and the drain is doped silicon. [22][23]. Sugino et al. and Swirehun et al. realized the SB-MOS can essentially eliminate parasitic bipolar effect and demonstrated a CMOS structure having an SB-PMOS device and conventional NMOS device, which was immune to latchup and substantially reduced soft-error rates and improved circuit reliability for both memories and logic applications [20][24][25]. The pre-1994 SB-MOS literature established proof of concept but at the same time suffered from low performance due to device architecture and process-technology issues.

Since 1994, Tucher et al. [26] and Snyder [27] realized the advantages for device scaling of SB-MOS technology, state of the art SB-CMOS process technology has significantly advanced. Actually the manufacturing process for SB-CMOS is simpler than conventional bulk CMOS, requiring fewer process and photolithography steps. The process is fully compatible with the existing silicon CMOS technologies and does not require novel process equipment. Various research groups have demonstrated more technology improvements for SB-MOS devices, for example, lower channel doping reduces the junction and gate capacitance, therefore enhances the frequency response of the device [28]. In 1999, Wang et al. demonstrated a bulk 27-nm-channel-length PtSi SB-PMOS device with a drive current of 350 μA/um, which initially set the standard for drive current performance for

highly scaled SB-CMOS technology [29]. In 2004, John Snyder's group reported SB-PMOS with cutoff frequency (f_T) of 280GHz for sub-30nm device [11] which was the best f_T reported for any silicon MOS transistors. B. Y. Tsui et al. demonstrated a 25nm Schottky-barrier FinFET with drive current of 750μA/um and I_{on}/I_{off} ratio of 10^9 [12]. H. Sato, et al. shows increase drive current by Pt/W protection film on Er. The drive current of Schottky – Barrier NMOS were improved twice as much as the Schottky-Barrier NMOS without protection. The drain currents achieved were 11μA/um for NMOS at V_{ds}=1.5V and V_{gs}=2V, and 16μA/um for PMOS at V_{ds}=-1.5V and V_{gs}=-2V. A CMOS inverter was demonstrated using the same process [13]. Zhu et al. reported using several silicides for SB-NMOS S/D formation, including $ErSi_x$, $DySi_x$, and $YbSi_x$, Where YbSi proved improved manufacturability and a 240% improvement in SB-NMOS Ion performance [14]. In 2005, Kinoshita et al. disclosed a high performance 50-nm-gate-length SB-NMOS using 10nm interfacial dopant layer between the source and drain [15]. This device has only 20% greater off state leakage current than conventional NMOS devices fabricated by the same process. A first sub-100-nm-gate-length SB-CMOS ring oscillator has been demonstrated using the above mentioned interfacial doping layer (also known as dopant-segregation) technique.

The SB-MOSFET technology offers an alternative to traditional CMOS technology with promise to bypass the scaling limitation of S/D doping profile control, sheet resistance, contact resistivity et al, with superior control of off state leakage current due to intrinsic Schottky potential barrier, and with elimination of parasitic bipolar actions, et al. SB-MOSFET is considered a candidate with inherent physical scalability to sub-10nm devices.

More recently the Schottky barrier MOSFET concept is adopted from Si to other semiconductor materials. In 2005, Zhu et al. reported germanium pMOSFETs with Schottky-barrier germanide source/drain with high-K gate dielectric and metal gate [16].

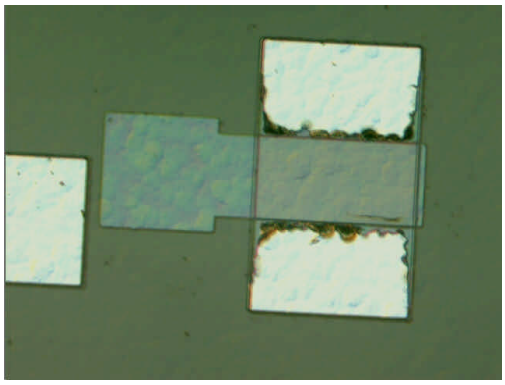
In 2006, using Schottky metal as source/drain has been proposed the first time on GaN MOSFET by H. B. Lee et al. at Kyungpook National University in Korea in collaboration with Y. H. Bae at Uiduk University in Korea and M. B. Lee at Daegu New Technology Agency in Korea [30]. Our group quickly realized the advantages of using metal as the Schottky barrier source/drain for GaN based MOSFET and MISFET devices. While using low barrier Schottky metal as source/drain for MOSFET is an attractive solution to aggressively scaled silicon MOSFETs, it is a more attractive solution to GaN MOSFETs. The actual advantages of the Schottky barrier MOSFET on GaN have been extended beyond that of the Si Schottky barrier MOSFET mainly because:

1) The manufacturing process for GaN SB-CMOS is simpler than conventional bulk CMOS, requiring fewer process and photolithography steps. The process is fully compatible with the existing silicon CMOS technologies and does not require novel process equipment.

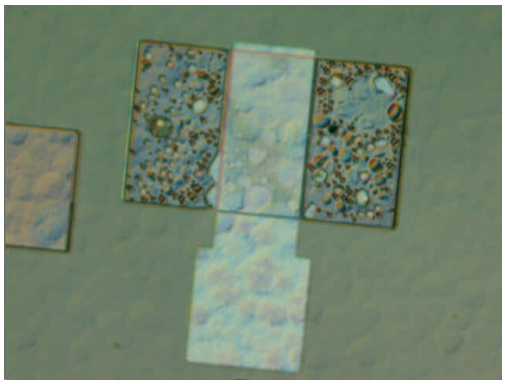
2) The Schottky metal can be used as the carrier rich source/drain, therefore the device manufacturing can exclude the ion implantation and thermal diffusion which requires high temperature for dopant activation. Metal source/drain also mitigates the scaling limitation of S/D doping profile control, sheet resistance, and contact resistivity et al.

3) Schottky barrier MOSFET has superior control of off state leakage current due to intrinsic Schottky potential barrier, and it also helps to eliminate the parasitic bipolar actions, furthermore it eliminates some of the short channel effects for aggressively scaled MOSFET such as GIDL (gate induced drain leakage).

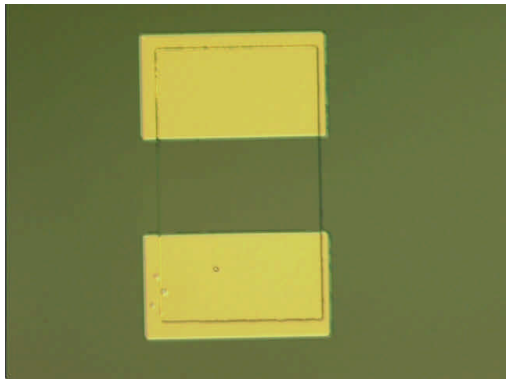
Experimentally both titanium and nickel have been deposited on GaN as the Schottky metal for the source drain. The experiments on patterning metal source/drain via metal wet etch indicated that the pattern of the source/drain is difficult to control as shown in figure 3.2 (a) and (b). Therefore other method to pattern the source/drain in device process flow has to be designed to avoid using metal wet etch in our final GaN MOSFET recipe. Finally, the redesigned device process recipe uses additional ohmic level photo lithography step and metal lift off to accomplish the goal. This way the pattern of the source/drain is defined by photolithography and lift off which is much cleaner process than metal wet etch. The photo exposure time is well designed to ensure the final Schottky metal completely fills the source/drain area. The Schottky metal patterning in the source/drain regions using our new recipe is shown in figure 3.2 (c).



(a) Ni source/drain using wet etch



(b) Ti source/drain using wet etch



(c) Ni source/drain using lift off

Figure 3.2: Ni source/drain and Ti source/drain using wet etch (a), (b) and using lift off (c).

Overall for metal source/drain patterning via either metal wet etch or metal lift off, it is difficult to creating extension source/drain junction under the gate for the MOSFET. The

finally successful fabricated device using above methods does not have any extension junction and the source/drain spacing is larger than the gate length. Therefore finite series resistance exists and the device is not optimized. This is one of the drawbacks, but due to the current limitation of GaN wet etching technique, the extension junction in GaN is difficult to achieve using method other than ion implantation and thermal diffusion.

3.3 GaN n-i-n Structure

The n-i-n structure is a device structure of MOSFET without gate dielectric and gate metal. The source-channel-drain structure is a two terminal semiconductor device. The channel material is intrinsic semiconductor. The n-i-n structures classically show space charge limited transport due to the lack of background doping. With a bias few times greater than the thermal voltage (kT/q), the IV characteristics of these devices exhibit space charge limited transport and the I-V characteristics are given by the Mott-Gurney limit [31]:

$$J = \frac{9\varepsilon_s \mu_n V_d^2}{8L^3} \tag{3.1}$$

In our GaN MOSFET process, the GaN n-i-n structure serves as an appropriate device structure to compare the regrown source/drain and the Schottky metal source/drain. This is mainly because it is easy to be fabricated and tested, and it is just the intermediate structure right there available in the middle of the processing steps during our GaN MOSFET or GaN heterogeneous source drain MOSFET fabrication. The following figure shows one example GaN n-i-n structure we fabricated. The detailed processing steps will be described in next chapter.

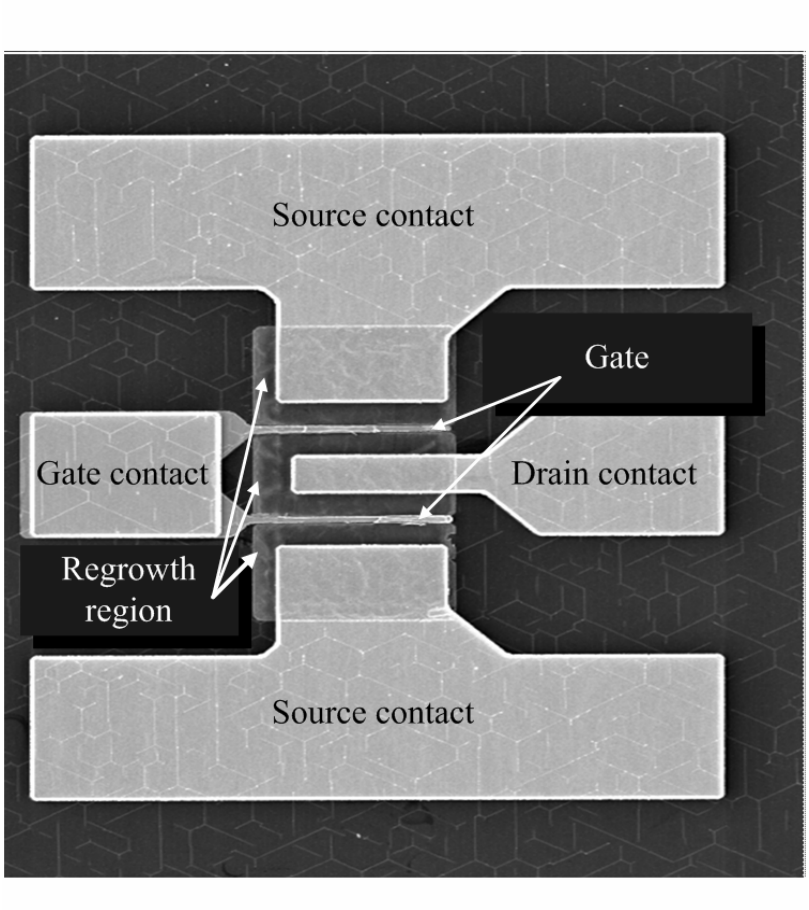
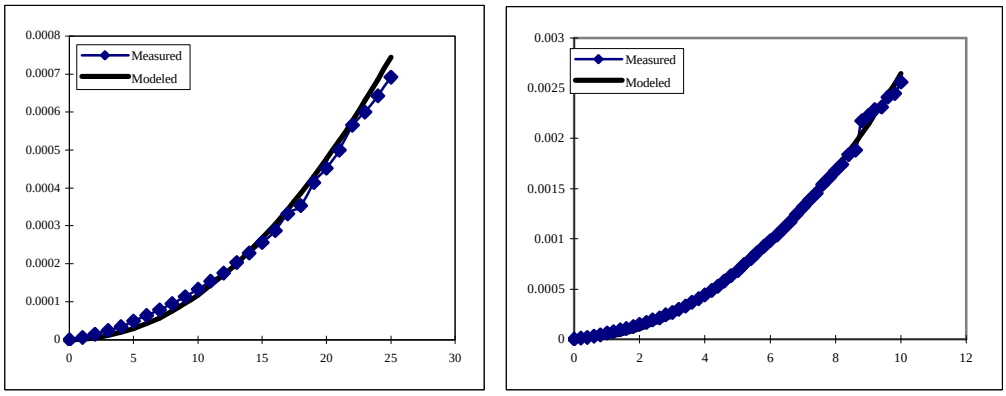


Figure 3.3: SEM Micrograph indicating the layout of the n-i-n structure.

Two types of n-i-n structures have been fabricated. First n-i-n structure has selected area epitaxial re-growth of n^+ doped GaN with source/drain doping concentration of $5\times10^{18}cm^{-3}$. Second n-i-n structure has metal (Ti) as source/drain. The DC characteristics of both structures are shown in figure 3.4. The output characteristics of both n-i-n structures are curve fitted according to Mott-Gurney limit. The calculated channel mobility is 85 $cm^2V^{-1}s^{-1}$ and 625 $cm^2V^{-1}s^{-1}$ for the regrown source/drain n-i-n structure and the titanium source/drain n-i-n structure, respectively.



(a) (b)

Figure 3.4: (a) Measured (close circle) and modeled (solid line) current-voltage characteristics of n-i-n structures with re-growth. Assuming a source-drain doping of $5x10^{18}$ cm^{-3}. Calculated mobility for this device was 85 $cm^2V^{-1}s^{-1}$. (b) Measured and modeled characteristics of n-i-n structures with Ti source-drain regions. Calculated mobility in this case is 625 $cm^2V^{-1}s^{-1}$.

The ISE-TCAD is used to generate the GaN n-i-n structures, figure 3.5 shows the regrowth source drain n-i-n structure, and the metal source drain structure is similar to this except that the source drain area is all metal Ti. The numeric simulator DESSIS in ISE-TCAD is used to do the drift-diffusion calculations.

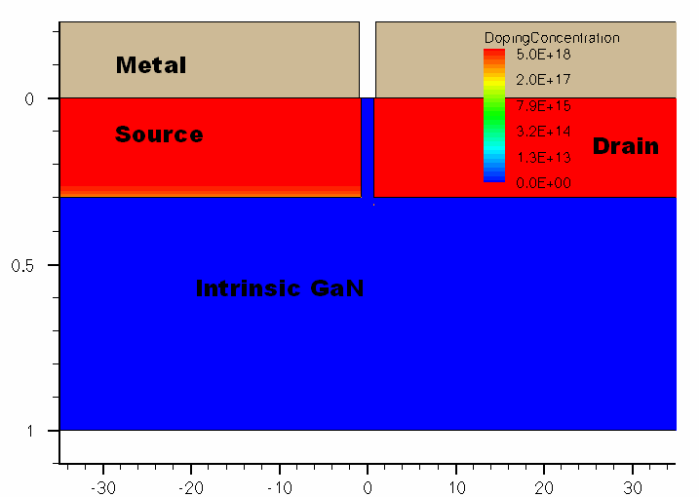


Figure 3.5: The doped GaN source drain n-i-n structure in TCAD simulation.

For regrown source/drain n-i-n devices, in order to obtain a better fit to our measurements, the low field electron mobility is used 85 cm^2/Vs. In this study, several different cases of trapping effects were introduced, the current voltage DC simulation results are shown in Figure 3.6. At low field there is disagreement between the model and the measurement data. So certain traps have to be introduced for a more accurate device modeling. After introducing mid-bandgap deep donor level (or hole neutral traps) into the GaN material, the low field current (red dot) is approaching the measurement current. While with deep acceptor level introduced, the simulation (Green Square) shows the low field current deviates further from the measurement current.

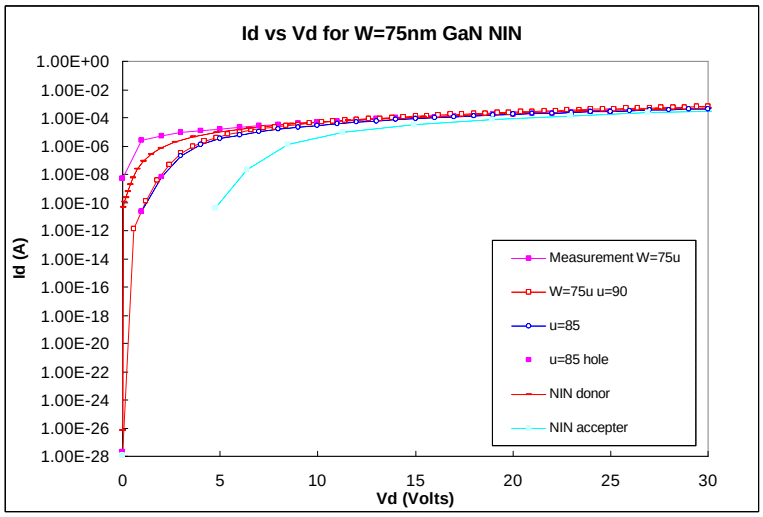
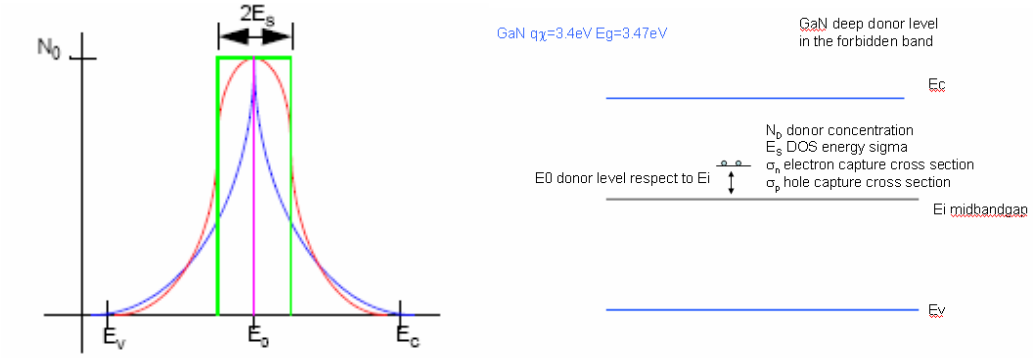


Figure 3.6: the IV curve for GaN n-i-n structure with donor introduced and accepter introduced.

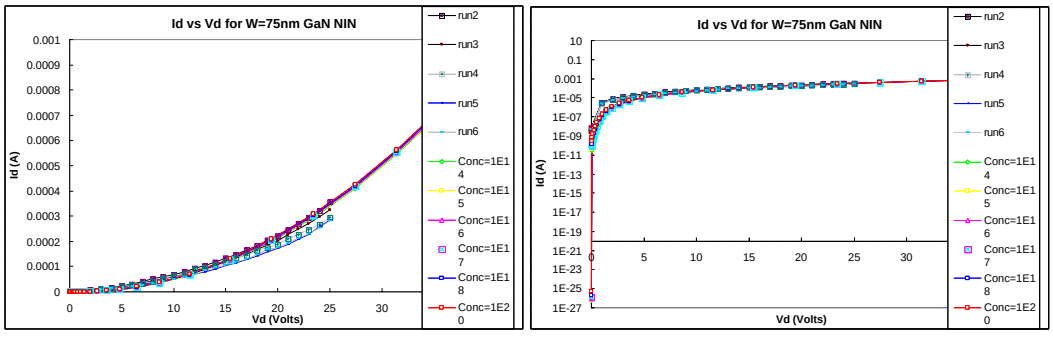
To further model the trap effect, we need to understand the trap parameters in TCAD. The TCAD trap models give us the following parameters for the donor traps (Figure 3.7).



(a) (b)

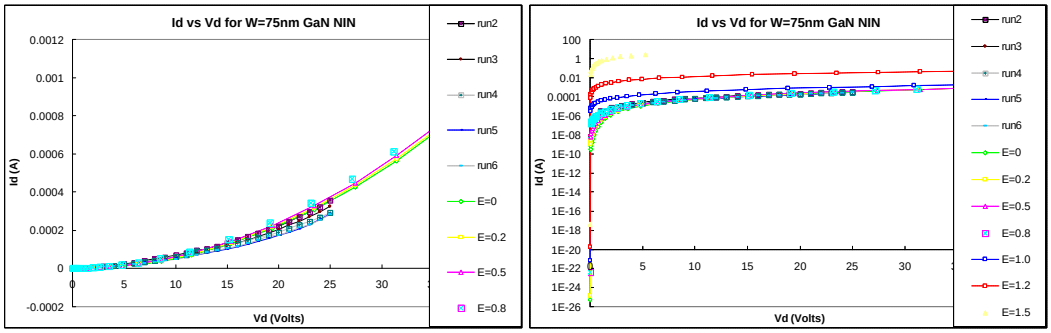
Figure 3.7: the trap model in TCAD. (a) Trap energy distribution. (b) One level Trap Parameters in band gap.

The single level trap effect is modeled and simulated, the effect on trap parameter such as donor concentration N_D, and trap energy level E_0 with reference to GaN mid bandgap level is shown in the Figure 3.8 and 3.9. The other trap parameters do not contribute to the DC simulation in our TCAD trap model. From Figure 3.8, with higher trap concentration, the low field current simulated is closer to the measurement, but the high field current simulated is also increased and start to deviate from the measurement. From Figure 3.9, the trap energy level also affect the DC current simulation, the trap level E_0=0.5eV matches closely with measurement current.



(a) (b)

Figure 3.8: the IV curve of n-i-n structure simulated for different donor concentrations comparing with several measurement runs. (a) Linear scale. (b) Semi-log scale.



(a) (b)

Figure 3.9: the IV curve of n-i-n structure simulated for different donor levels comparing with several measurement runs. (a) Linear scale. (b) Semi-log scale.

The metal (Ti) source drain n-i-n devices are also modeled. In this case, the calculated value of mobility for this device is 625 $cm^2V^{-1}s^{-1}$ as shown in figure 3.4. In TCAD, after introducing uniform trap distribution, we can model the n-i-n structure very well with low field mobility of 625 $cm^2V^{-1}s^{-1}$ as shown in figure 3.10.

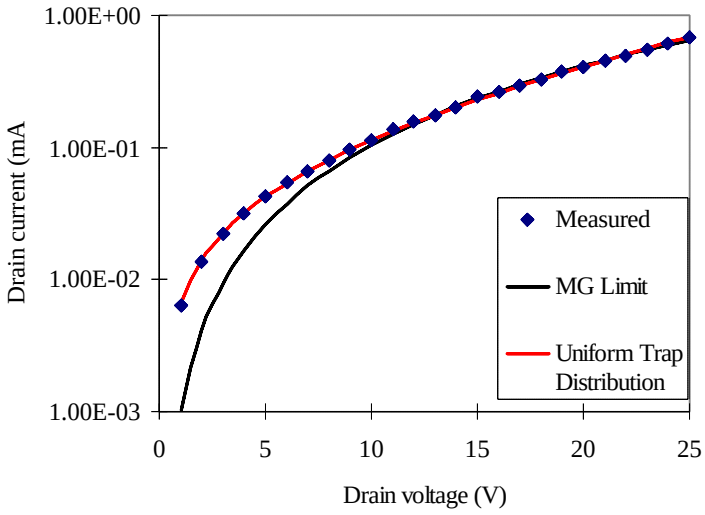


Figure 3.10: Measured and TCAD modeled IV curve for n-i-n structure with Ti source/drain

The n-i-n device characteristics show the successful fabrication and demonstration of both highly doped re-growth source drain and metal source drain. The TCAD model is in agreement with the calculated channel mobility. This is an important step not only in the fabrication of GaN based FETs but also in developing accurate device physics models.

3.4 Metal-GaN Schottky Contact

Schottky contacts to GaN and AlGaN/GaN hetero-structures are a fundamental component of many devices. And it is one of the most critical components for Schottky Barrier GaN MOSFET. As III-V nitride materials attract more research attentions these years, some of the fundamental problems for nitride semiconductor devices have been solved. To summarize the efforts of Schottky and Ohmic contacts research for nitride semiconductors, a number of reviews have been published [32-35].

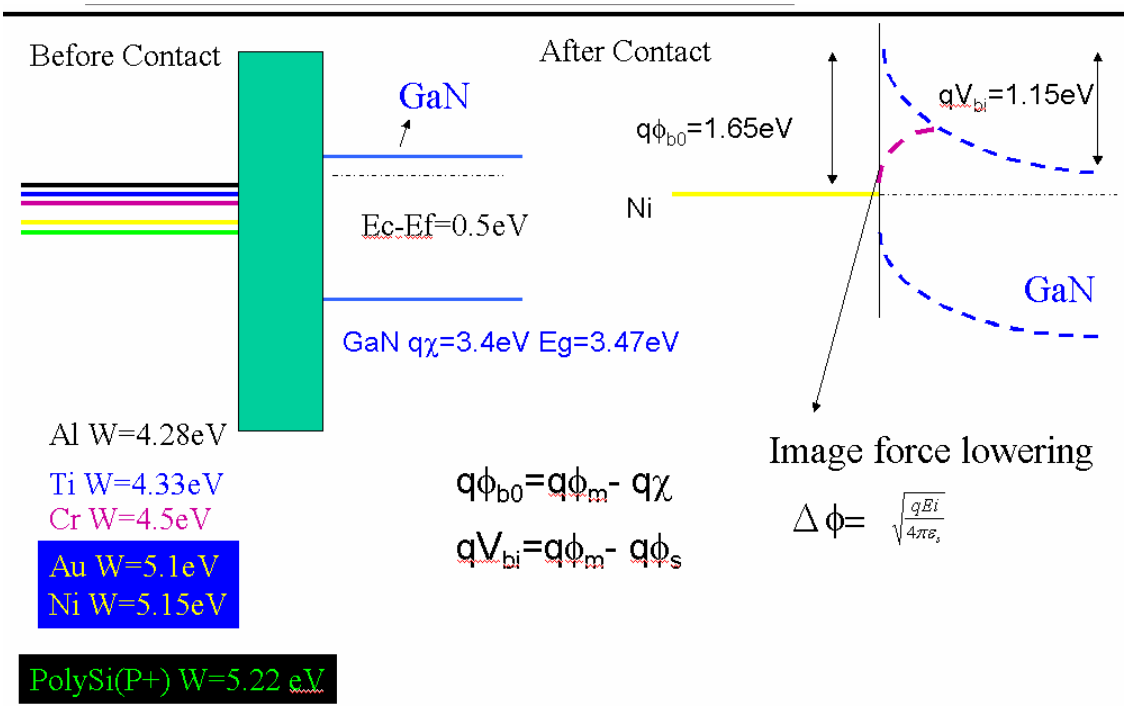


Figure 3.11: Metal and GaN before and after contact

Figure 3.11 shows several metal work functions and the simplified GaN band structure. After contact, in the ideal case, we assume there is no interfacial energy states, the build in potential V_{bi} and the Schottky potential barrier can be given by:

$$qV_{bi} = f_m - f_s \tag{3.2}$$

$$qf_{b0} = qf_m - qc \tag{3.3}$$

Where ϕ_m is metal work function and ϕ_s is semiconductor work function, χ is the semiconductor electron affinity. With the image force lowering, the actual barrier will be:

$$qf_b = q(f_{b0} - \Delta f) \tag{3.4}$$

$$\Delta f = \sqrt{\frac{qEi}{4pei}} \tag{3.5}$$

The Schottky junction can be characterized by I-V measurement based on the well known thermionic emission-diffusion theory:

$$I = I_s(e^{\frac{qV}{nkT}} - 1) \tag{3.6}$$

$$I_s = A_e A^* T^2 e^{-\frac{qfb}{nkT}} \tag{3.7}$$

$$A^* = \frac{4pqm^* k^2}{h^3} \tag{3.8}$$

Where A_e is the contact area, and A* is the effective Richardson constant. The I-V characterization of the Schottky junction gives the ideality factor n and reverse saturation current I_s as shown in the following figure. From the reverse saturation current, the barrier height can be calculated from equation 3.4.

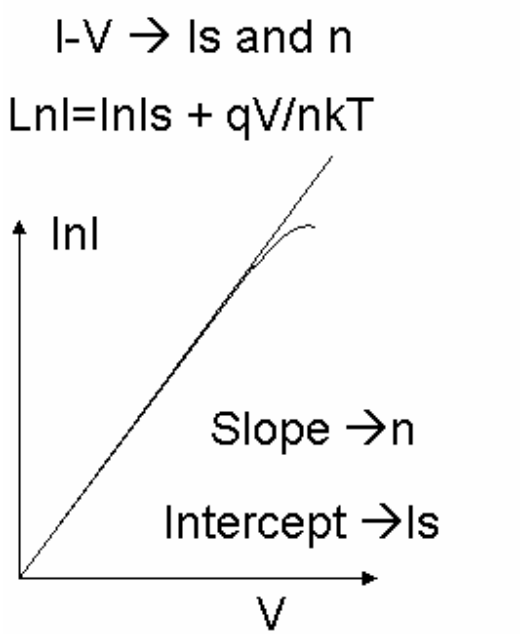


Figure 3.12: Schematic of I-V characteristics of Schottky junction.

Another method to characterize the Schottky junction is using the temperature dependent of reverse saturation current for barrier height. It is abbreviated as I-V-T and is shown in figure 3.13. The Schottky barrier height can be derived from equation 3.6.

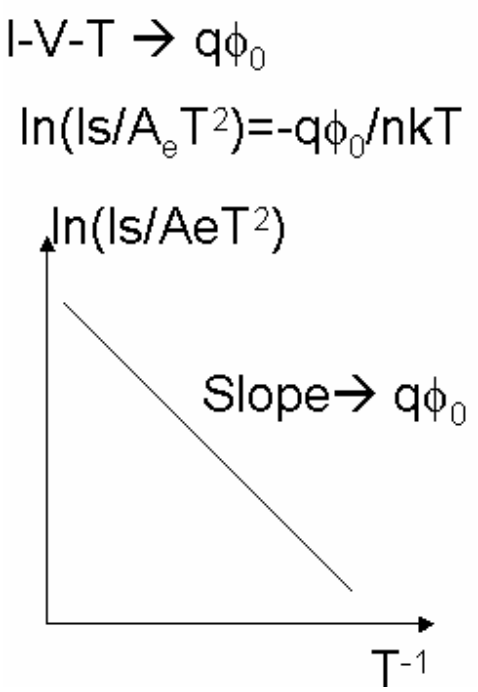


Figure 3.13: Schematic of I-V-T characteristics of Schottky junction

The C-V characterization of the Schottky junction is based on the depletion capacitance measurement.

$$W = \sqrt{\frac{2e_s(V_{bi} - V - kT/q)}{qNd}} \tag{3.9}$$

$$C = \frac{e_s Ae}{W} \tag{3.10}$$

$$\frac{1}{C^2} = \frac{2}{Ae^2 qNde_s}(V_{bi} - \frac{kT}{q} - V) \tag{3.11}$$

Using the biased dependent depletion capacitance, we can calculate the build in potential and the barrier height based on equation 3.11. The basic idea is shown in figure 3.14.

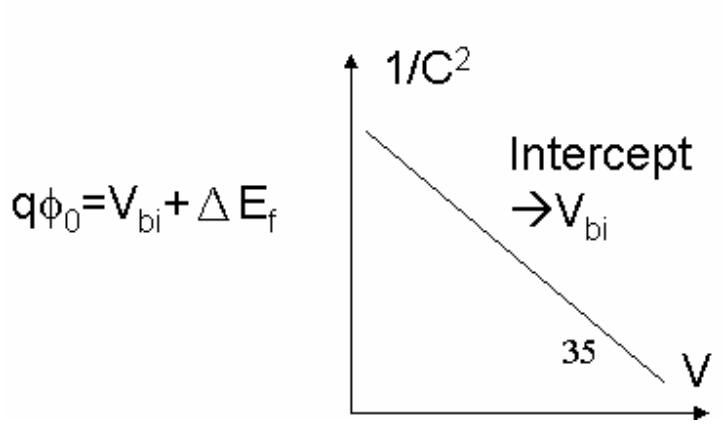


Figure 3.14: Schematic of C-V characteristics of Schottky junction

However, most of the metal semiconductor contacts are not as simple as the ideal case. A more detailed energy band diagram of a metal n-type semiconductor contact is shown in the following figure 3.15.

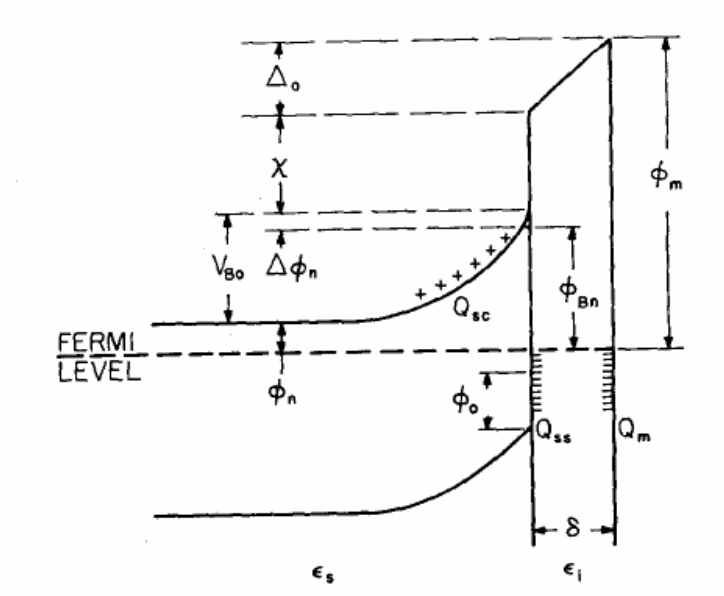


Figure 3.15: Energy band diagram of metal n-type semiconductor contact with an interfacial layer of the order of atomic distance. [36]

With the assumption of (1) with close contact between the metal and semiconductor and with an interfacial layer of atomic dimension, this layer will be transparent to electrons

meaning it is very easily for electron to tunnel through, and it can withstand potential across it. (2) the surface states per unit area per electron volt at the interface are a property of the semiconductor surface and are independent of the metal. Knowing the surface charge and space charge, the more completed equation for barrier height has been derived as:

$$Q_{sc} = \sqrt{2qe_s N_d (f_{bn} - V_n + \Delta f - kT/q)} \tag{3.12}$$

$$Q_{ss} = -qD_s (Eg - qf_0 - qf_{bn} - q\Delta f) \tag{3.13}$$

$$Q_m = -(Q_{ss} + Q_{sc}) = -\frac{e_i \Delta}{d} \tag{3.14}$$

Where the Q_{sc} is the space charge in the depletion layer of semiconductor, Q_{ss} is the acceptor surface charge, and Q_m is the opposite charge on the metal surface for charge neutrality. The Δ is the potential across the interfacial layer. And it can be derived from the band diagram:

$$\Delta = f_m - (c + f_{bn} + \Delta f) = -d\frac{Q_m}{e_i} \tag{3.15}$$

The final barrier height can be calculated from equation 3.20 to 3.22 and is shown in the following equations.

$$c_1 = \frac{2qe_i N_d d^2}{e_i^2} \tag{3.16}$$

$$c_2 = \frac{e_i}{e_i + q^2 dD_s} \tag{3.17}$$

$$f_{bn} = [c_2 (fm - c) + (1 - c_2)(\frac{Eg}{q} - f_0) - \Delta f] + \{\frac{c_2^2 c_1}{2} - c_2^{3/2}\sqrt{c_1 (f_m - c) + (1 - c_2)]\frac{Eg}{q} - f_0)\frac{c_1}{c_2} - \frac{c_1}{c_2}(V_n + \frac{kT}{q}) + \frac{c_2 c_1^2}{4}}\} \tag{3.18}$$

With c_1 very small (of the order of 0.01V) and the above barrier height can be approximated by the following equations.

$$f_{bn} = c_2 f_m + c_3 \tag{3.19}$$

$$c_3 = -c_2 c + (1 - c_2)(\frac{Eg}{q} - f_0) - \Delta f \quad (3.20)$$

The two extreme cases are 1) too much interfacial traps, when Ds→ infinity, so c_2→0. The above equation reduces to.

$$qf_{bn} = (Eg - qf_0) - q\Delta f \quad (3.21)$$

And 2) ideal case without interfacial traps, when Ds→0, so c_2→1. The above equations reduce to ideal case.

$$qf_{bn} = qf_m - qc - q\Delta f \quad (3.22)$$

The more general equation is sued to fit the experimental results and therefore the density of the interfacial traps can be calculated from the fitted constants. And the surface energy levels ϕ_0 for several semiconductors are close to one third of the band gap which indicated that the high peak density of surface states or defects near one third of the gap from the valence band edge. And for many III-V compound semiconductors, the Fermi level is pinned and the barrier height is independent of the metal.

Various GaN Schottky junctions have been fabricated and studied. The following tables summarize several metals for GaN Schottky contact and the Schottky barrier height. Among all the metals which have being investigated so far on GaN, titanium (Ti), nickel (Ni), and Chromium (Cr) are the most promising candidates for their low Schottky barrier on GaN.

TABLE 3.1: Several metal properties [37]

	work function	Resistivity	thermal expansion	thermal conductivity
	(eV)	(10^{-6}Ohm-cm)	10^{-6}(1/K)	W/cm K
Potassium (Pt)	5.65	9.6	8.8	0.716
Nickel (Ni)	5.15	6.16	13.4	0.907
Palladium (Pd)	5.12	9.78	11.8	0.715
Gold (Au)	5.10	2.05	14.2	3.17
Tungsten (W)	4.55	4.82	4.5	1.74
Chromium (Cr)	4.50	11.80	4.9	0.937
Titanium (Ti)	4.33	39	8.6	0.219
Niobium (Nb)	4.30	15.20	7.3	0.537
Aluminum (Al)	4.28	2.42	23.1	2.370
Tantalum (Ta)	4.25	12.20	6.3	0.575
Magnesium (Mg)	3.66	4.05	24.8	1.56

TABLE 3.2: Metal p-GaN Schottky contact properties [37]

Metal	Ideality factor n	Barrier Height (eV)		
		I-V-T	I-V	C-V
Gold (Au)	1.27		0.57	
				2.48
Potassium (Pt)	1.15		0.50	
Nickel (Ni)	1.44		0.50	
Titanium (Ti)	1.36		0.65	

TABLE 3.3: Metal n-GaN Schottky contact properties [37]

Metal	Ideality factor n	Barrier Height (eV)			Richardson Constant A* (Acm-2K-2)
		I-V-T	I-V	C-V	
Gold (Au)	1.03	0.844		0.94	0.006
	1.04	0.91		1.01	0.0092
	1.04	0.88	0.87	0.98	14.68
	1.4		0.98	1.16	
	1.15		1.03	1.03	
Palladium (Pd)	1.04	0.92	0.94	1.07	3.24
	1.09	0.96	1.11	1.24	0.04
	1.14	0.91		0.94	0.44
Nickel (Ni)	1.04	0.99	0.95	1.13	11.2
	1.15	0.66		0.56	
	1.17		1.15	1.11	
	1.14		0.95	0.96	
	1.11		0.93	1.03	
	1.10	0.69		0.92	0.129
Potassium (Pt)	1.05	1.08	1.01	1.16	64.7
	1.10		1.13	1.27	
	1.21	1.03		1.04	6.61
	1.0		1.10	1.10	
Titanium (Ti)	1.29	0.25			0.02
	1.28	0.58		0.59	
	1.08		0.65	0.68	
Silver (Ag)	1.57		0.7		
Lead (Pb)	1.28		0.72		
Chromium (Cr)	1.05	0.53		0.58	
NiSi	1.17		1.03	1.25	
PtSi	1.10		0.85	0.87	

3.5 GaN etching

The GaN processing techniques is crucial in order to achieve good performance of GaN based devices. Many GaN etching methods have been tried. The most of GaN etch are done by plasma etching which has disadvantages such as easy to generate ion-induce damages and difficult to obtain smooth etched sidewall [38][39]. Several wet GaN etch techniques have been tried including photo-enhanced electrochemical (PEC) wet etch [40][41][42], photo-assisted cryogenic etch (PAC) [43], crystallographic wet etch [44], photo-assisted anodic etch [45], wet chemical digital etch of GaAs at room temperature [46], and PEC binary etch using $K_2S_2O_8$ and KOH [47]. In this study, the PEC binary GaN etching technique using potassium persulphate $K_2S_2O_8$ and potassium hydroxide KOH is selected among the above GaN wet etching techniques. Instead of using an ultraviolet (UV) light source, we try not to use any special light sources. For better surface roughness control, we employed a technique named digital etch. The experimental details and the experimental results will be shown in the later sections of this section.

Several etching techniques have been reviewed and the etch rate and surface roughness are summarized in figure3.16, figure 3.17 and table 3.4. The GaN samples for these wet etch experiments are generally lightly Si doped with the concentration 5×10^{16} cm^{-3} to 10^{17} cm^{-3}.

The following figure shows several of the published data of GaN wet etch rate. As can be seen the GaN wet etch usually requires an oxidization agent and a reduction agent. The citric acid/H_2O_2 wet etch [44] shows the highest etch rate about 580 nm per minute, while other etch techniques such as KOH PEC [38] [39], and tartaric acid/ethylene glycol etch [43] also show promising etch rate.

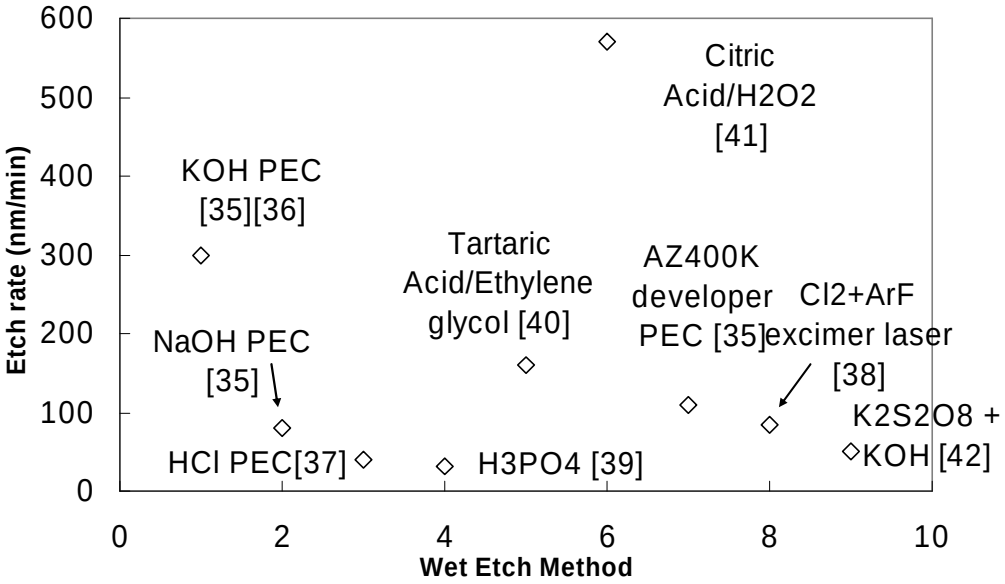


Figure 3.16: Etch rate of several etching techniques.

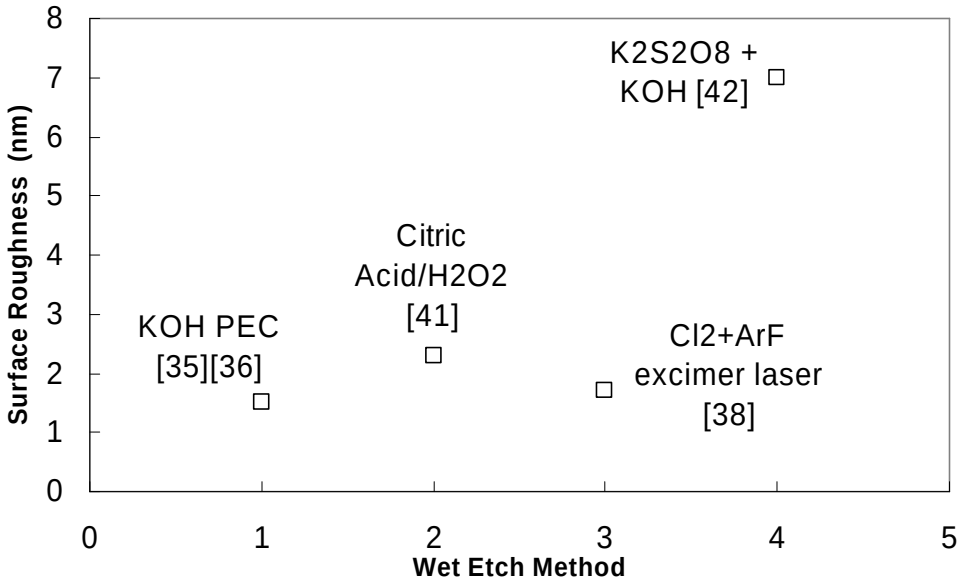


Figure 3.17: GaN surface roughness after etch using several etching techniques.

TABLE 3.4: Review of different GaN Etching Techniques.

No.	Electrolyte used	Method	Etch Rate (nm/min)	Roughness
1	KOH	PEC[38][39]	50 for 0.02M >300 for 0.04M	1.5nm
2	NaOH	PEC[38]	80	NA
3	HCl	PEC[40]	1.5-40	NA
4	H_3PO_4	Crystallographic wet etch[42]	13-32	NA
5	Tartaric Acid/Ethylene Glycol	Photo-assisted Anodic etching[43]	160	81.5nm
6	AZ400K developer	PEC[38]	110	NA
7	Cl_2+ArF excimer Laser (dry etch)	PAC[41]	84 @210K	1.7nm
8	$K_2S_2O_8$ + KOH	PEC[45]	50	7nm
9	Citric Acid/H_2O_2 (2:1) (GaAs etching)	Oxidation/ Reduction[44]	570	2.3nm

However besides etch rate, the surface roughness is crucial to GaN based device processing. Figure 3.16 shows the published data of GaN surface roughness after wet etch. The potassium hydroxide (KOH) PEC etch and Cl_2 with ArF excimer laser etch show promising GaN surface roughness after etching. The potassium persulfate/potassium hydroxide ($K_2S_2O_8$/KOH) etching method [45] shows a good surface roughness too.

In our experiment, the PEC binary GaN etching method is selected because of the following reasons: 1) Binary etch enables better control and precision as shown in figure 3.16 and table 3.4. 2) It does not require sophisticated equipment. 3) It can be conducted at both

room temperature and higher temperature. 4) It does not require any electrode. And 5) External stimulus are not required.

Several GaN samples are grown on C plane sapphire substrate by MOCVD. The thicknesses of two n-GaN films are about 500nm and 700nm respectively. The intrinsic GaN film is about 1um, and the p-GaN film is about 1um. The aluminum nitride (AlN) buffer layer is used between GaN and sapphire. The Si is used as n type dopant, the n-GaN doping concentration is 5×10^{18} cm-3 and 1×10^{18} cm-3, respectively. The p-GaN is doped with Mg and the doping concentration is about 1×10^{16} cm^{-3}.

All of the GaN films have been patterned with a LED mask, then 200 nm Ni layer has been deposited on the GaN films using E-beam deposition, after Ni lift-off, the patterned GaN films left with Ni and GaN films.

The $K_2S_2O_8$ used in the etch acts as an oxidizing agent and KOH acts as a reducing agent. The relevant reactions in the GaN binary etch might be the following according to Bardwell et al. [45], but in our experiment the extra ultraviolet light source is not used, instead luminescence light source is used which might give small trace of ultraviolet light:

$$GaN + photon \rightarrow GaN + e^{-} + p^{+} \tag{3.23}$$

$$GaN + 3p^{+} \rightarrow Ga^{3+} + \frac{1}{2}N_2 \tag{3.24}$$

$$S_2O_8^{2-} + 2e^{-} \rightarrow SO_4^{2-} \tag{3.25}$$

$$S_2O_8^{2-} + photon \rightarrow 2SO_4^{-*} \tag{3.26}$$

$$SO_4^{-*} + OH^{-} \rightarrow SO_4^{2-} + OH^{*} \tag{3.27}$$

$$SO_4^{-*} + e^{-} \rightarrow SO_4^{2-} \tag{3.28}$$

$$OH^- + e^- \rightarrow OH^- \tag{3.29}$$

$$O_2 + OH^- \rightarrow O_3^- + H^+ \tag{3.30}$$

The etching process is carried out in the following cycles: 1) Soak in 5% $K_2S_2O_8$ solution for 30 seconds; 2) wash in DI water for 30 seconds; 3) Soak in 10% KOH for 30 seconds; 4) wash in DI water for 30 seconds; 5) repeat above steps for 50 cycles. 6) Blow dry with Nitrogen. Following the above procedure, we have tried the $K_2S_2O_8$/KOH binary etch on intrinsic GaN, n-GaN and p-GaN films at room temperature, 50°C, and 75°C.

The Dektak 3030 profilometer is used to measure the GaN surface profile before and after the binary etch. The patterned Ni to GaN step height difference before and after binary etch is the GaN etched away.

Figure 3.18 shows the intrinsic GaN, n-GaN and p-GaN films etch rate (in nm/cycle) versus temperature from room temperature 25°C up to 75°C. Note 1 cycle takes about total 2minutes (30 seconds' of 5% $K_2S_2O_8$, 30 seconds' of KOH and 60 seconds of DI water). The etch rate is not as high as in [45] because of two reasons. First, we didn't use additional ultraviolet light source which can obviously increase the chemical reaction rate. Second, we did in the "Digital" way of wet etch, so basically we intentionally reduce the GaN etch rate in order to achieve better surface roughness control.

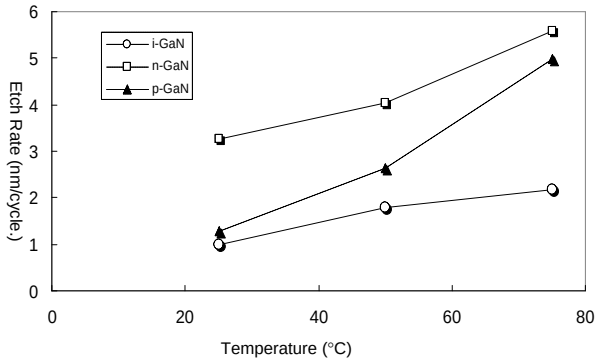


Figure 3.18: GaN $K_2S_2O_8$/KOH binary etch rate vs. temperature.

Figure 3.19 plotted the etch rate achieved in nm per minute versus one over temperature. The etch rate is plotted as log scale, the linearity of the etch rate curves show that the GaN wet etch rate versus temperature also follows Arrhenius law relation. The GaN wet etch rate is around 1nm/min. and increase to around 2nm/min. at 75°C. And the n-GaN has highest etch rate, the possible reason might be higher doping concentration and more defects which make it easier for initial etching to start.

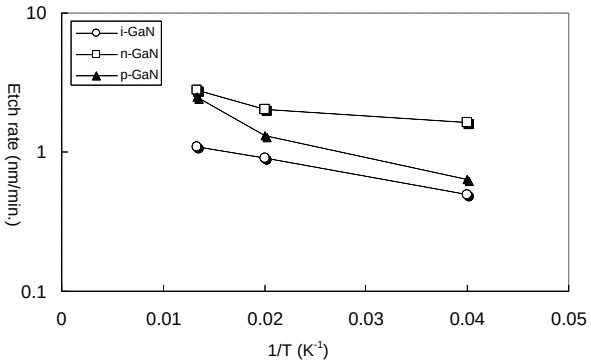
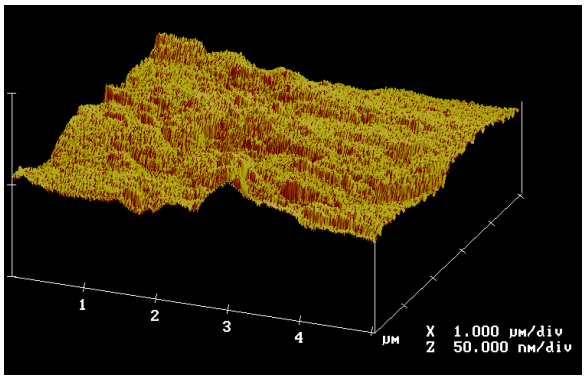


Figure 3.19: GaN $K_2S_2O_8$/KOH binary etch rate Arrhenius law.

Besides Dektak profile measurement, we also used AFM for surface topology and roughness measurement. The AFM image of GaN surface before and after GaN binary etch are shown in figure 3.20 and 3.21. The AFM image is taken by a contact mode AFM scan,

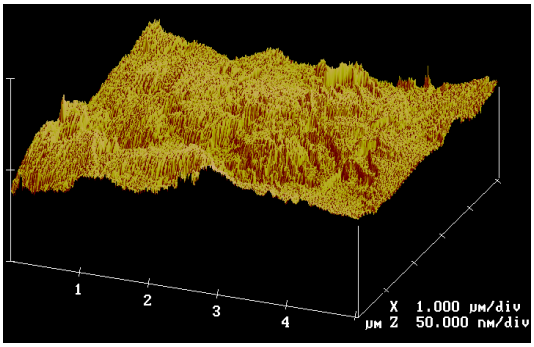
the X and Y directions are the scan area, the Z direction shows the surface roughness. The AFM image shows that the GaN surface is smooth before GaN etch which justified our MOCVD growth techniques.



n-GaN surface roughness 3.8nm before etch

Figure 3.20: n-GaN surface RMS roughness before etch measured by AFM

Figures 3.21 shows the n-GaN film surface roughness after GaN etch. The surface roughness is calculated by RMS.



n-GaN surface roughness 4.9nm after etch

Figure 3.21: n-GaN surface RMS roughness after etch measured by AFM

The purpose of this study is to initiate the research on room temperature GaN wet etch without UV light which is more applicable to industry wet etch as in Si device processing. To fully understand and improve the binary wet etch process, much effort would be required for much more detailed experiment designs such as GaN films with different doping concentration, broader temperature range, and more AFM surface roughness measurements to achieve the conclusion with more statistics significance. However all these are beyond the scope of my current research focus and the binary wet etch will be further explored in our group and gradually applied to certain steps of our GaN device processing.

To summarize this section, the $K_2S_2O_8$/KOH binary etch is successfully performed on intrinsic GaN, n type doped GaN and p type doped GaN films on sapphire at room temperature and elevated temperature, respectively. The etch rate-temperature relationship agree with Arrhenius law. The etch rate is relatively low but it can control the surface roughness with high precision. The in-depth study is needed for the binary etch, but the room temperature experimental results shown in this study demonstrated very promising results of GaN surface roughness control.

3.6 Summary

In this chapter, several GaN source/drain techniques are discussed with emphasis on regrown source/drain and Schottky metal source/drain. The advantages of using Schottky metal as source/drain for GaN MOSFET are discussed in details. The experimental method to fabricate metal source/drain on GaN is discussed. The n-i-n structures with both regrown

source/drain and Schottky metal (Ti) are fabricated and characterized. The n-i-n structures are furthered modeled using ISE-TCAD and both modeled mobility and the calculated channel mobility indicate the advantage of using Schottky metal for source/drain on GaN. The metal-GaN Schottky contact is reviewed and the prospective metal candidates for GaN Schottky barrier MOSFET are selected. Finally the GaN wet etch techniques are reviewed and the binary etch is studied, the experimental results show good GaN wet etch surface smoothness control indicating promising application for GaN devices.

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Chapter 4

Demonstration of a pulse doped channel GaN MESFET

This chapter demonstrates the pulsed doped GaN MESFET investigated in this work. The chapter starts with a brief introduction of the idea of pulse doped GaN film. It is followed by MESFET device processing steps on this pulse doped GaN film and the DC characterization of the fabricated GaN MESFET. The RF characterization of the low dimension device with gate length of 0.7 μm is shown. Several key device parameters such as gate capacitance, sheet carrier concentration, output conductance, and low field mobility have been extracted from the high frequency S parameter measurements. Detailed analysis and comments on these MESFET have been included in the chapter along with the presentation of the device electrical characteristics. The chapter ends with a summary of these MESFETs performance and discussions on the possibility to improve the device performance.

4.1 Pulse Doped GaN film

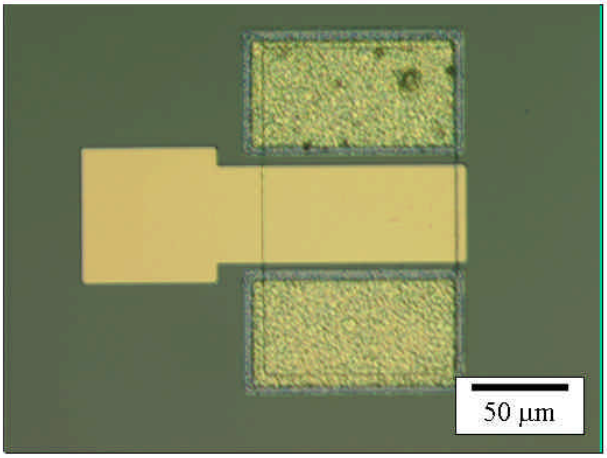
The different polar faced GaN films have been successfully grown by MOVPE by Professor Sitar's group in department of material science and engineering at North Carolina State University. [1] [2] Among these films, I fabricated GaN MESFET on one 2 inch wafer with pulsed doped channel GaN film. The GaN film growth procedures include surface preparation of sapphire substrate, followed by low temperature AlN deposition with anneal. Then 1.5μm thick intrinsic GaN is deposited on AlN buffer layer, followed by 30nm thick GaN films with Si pulsed doping concentration of 4×10^{17} cm^{-3}. Finally a 30nm undoped GaN cap layer is grown on the top of the pulsed doped channel layer. The cap layer is undoped and therefore serves a purpose of surface protection, it will increase the surface smoothness and reduce the doped GaN trapping effect in the channel surface area. The detailed film growth is described in [1] [2].

4.2 GaN MESFET Experiment and DC Characteristics

The device processing takes place in a class 1000 clean room. The device mesa isolation is first formed by GaN reactive ion etching (RIE) in BCl_3 plasma. Then the source/drain is patterned by photolithography and ohmic metal Ti/Al/Ni/Au (15nm/150nm/80nm/80nm) is deposited. After metal lift off, the wafer is RTA annealed up to 800°C by 60 seconds to achieve better ohmic contact. The third level lithography is done by patterning the gate metal and Ni/Au (100/100nm) are deposited using e-beam deposition as Schottky gate metal. Finally 180nm-thick Au is deposited as interconnect metal. The four

level photolithography steps conclude the GaN MESFET and HEMT process flow. More detailed GaN MESFET process flow is listed in Appendix A.

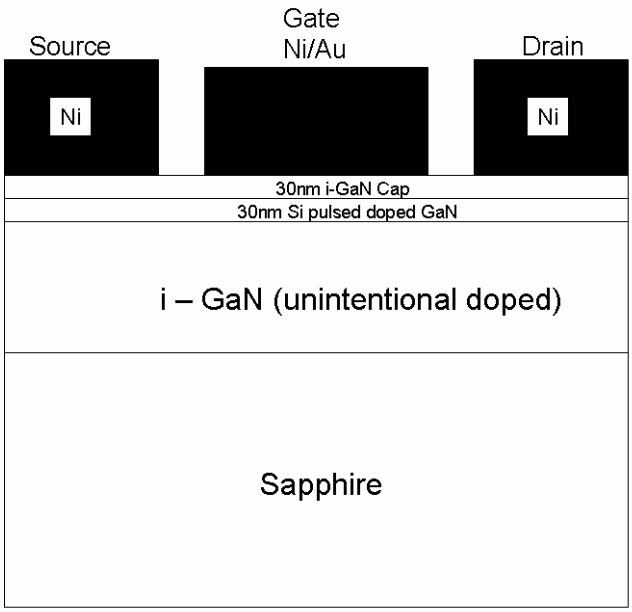
The FatFET device with gate length of 100μm and gate width of 50μm has been characterized and the device picture and device cross-section diagram are shown in Fig. 4.1(a) and (b).



Lg=50um
Wg=100um

S/D distance=60um
S/D length=66um
S/D width=115um

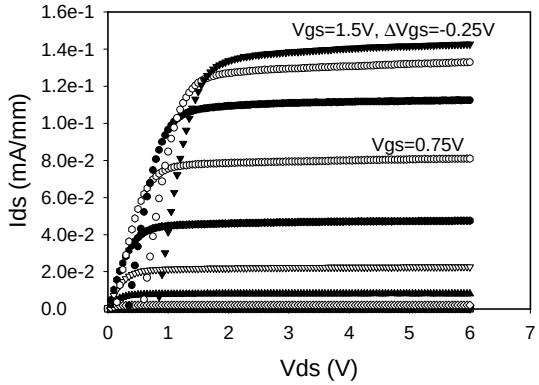
(a) FatFET picture



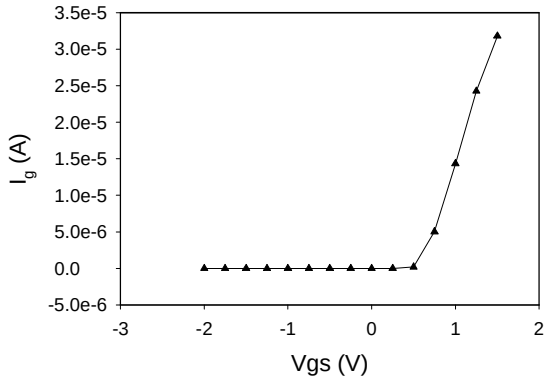
(b) FatFET cross-section

Figure 4.1: GaN MESFET for DC characterization. Device picture and device cross-section.

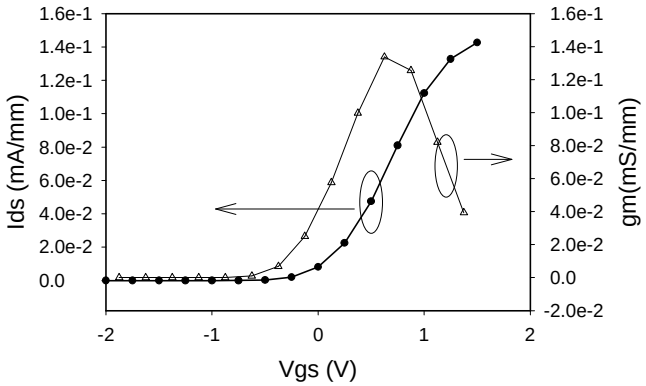
The DC electrical performance of the device is characterized by Parameter analyzer HP4155b. The device output characteristics Ids-Vds, gate Schottky diode, and device transfer characteristics are shown in Fig. 4.2 (a), (b) and (c), respectively. The device has a very good pinch off performance with a pinch off voltage of -1.25 volts and the achieved maximum drain current of 14.8μA at gate bias of 1.5V and drain bias of 6V which if normalized with respect to device width of 100μm is 0.148mA/mm. However the useful drain current density is 0.08mA/mm at gate bias of 0.75V which is the threshold of Schottky gate leakage. And the maximum transconductance is 13.4μS at gate bias of 0.75V and drain bias of 6V which is normalized to 0.134mS/mm. And the MESFET gate Schottky diode is turned on at gate bias above 0.75V, therefore the drain current and peak transconductance are all affected by the gate leakage at higher gate bias as seen in Fig. 4.2 (a) and (c). Above gate bias of 0.75 V, at low drain bias the drain current become negative due to the high Schottky gate leakage current as seen in Fig. 4.2 (a), the large gate leakage current flowing from gate to drain exceeds the nominal channel current from drain to source, which results the negative net drain current. At high drain bias, the drain current is degraded by the large gate leakage current flowing from drain to gate instead of to source. The same effect results the transconductance fall off the peak value sharply as the gate leakage starts increase exponentially as seen in Fig. 4.1 (c). This Schottky gate leakage affects the device gate voltage swing and therefore it sets a upper bound of the gate voltage for the device operation. In this case it is 0.75V.



(a) Output Characteristics with gate bias from -2V to 1.5V at step of 0.25V. Above 0.75V we can see the gate Schottky leakage current affecting the drain current.



(b) Gate metal-semiconductor Schottky junction current with drain biased at 0V. Above 0.75V we can see the gate Schottky diode is turned on.



(c) Transfer Characteristics

Figure 4.2: Electrical characteristics of GaN MESFET with gate dimension of 100μm × 50μm.

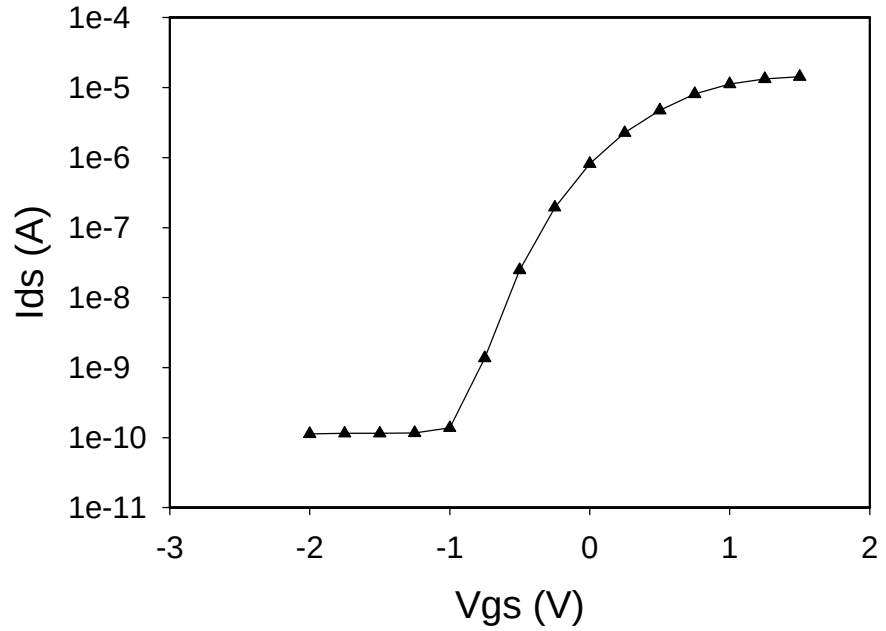


Figure 4.3: Transfer characteristics Ids-Vgs in logarithmic scale. The drain bias Vds is 6V.

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Fig. 4.3 shows the log scale drain current, the I_{on}/I_{off} ratio reaches above 10^5. The pinch off voltage is around -1 volts. Using MESFET pinch off voltage analysis, the pinch off voltage of the GaN MESFET can be derived using the following equations with corresponding thickness and doping structure as shown in Fig. 4.4.

$$V_{poff} = \frac{q}{2e} N_2[a^2 - (1 - \frac{N_1}{N_2})d^2] \qquad (4.1)$$

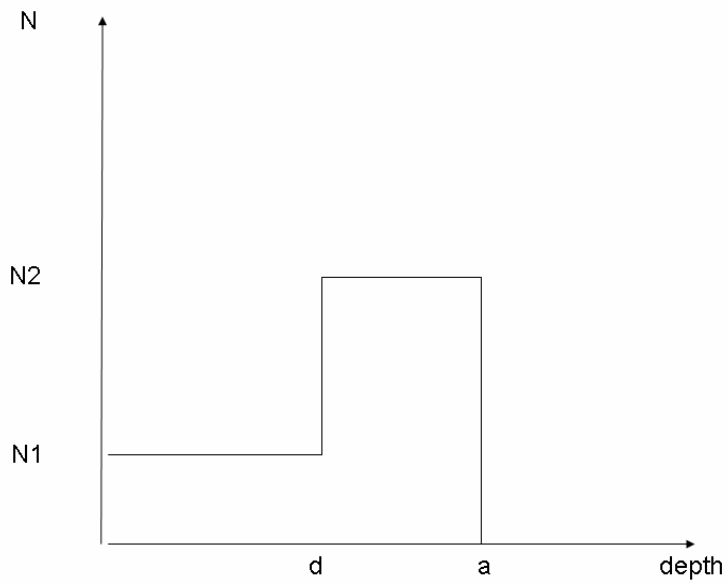


Figure 4.4: Pulse doped GaN doping profile.

The calculated pinch off voltage -1 volts with N1=0, N2= 4×10^{17} (cm^{-3}), cap layer thickness of 30nm, and channel thickness a-d of 30nm agrees well with the measurement results meaning the well controlled pulsed doping concentration and pulsed doped layer thickness.

4.3 Two Gate Finger GaN MESFET DC/RF Characteristics

4.3.1 DC Characteristics

On the same wafer, the two finger MISFET device with gate length of 0.7μm and gate width of 100μm has been characterized and the device picture is shown in Fig. 4.5 and the

device cross-section diagram is similar as shown in Fig. 4.1(b) with only difference in the two gate fingers, therefore it is not included in this context.

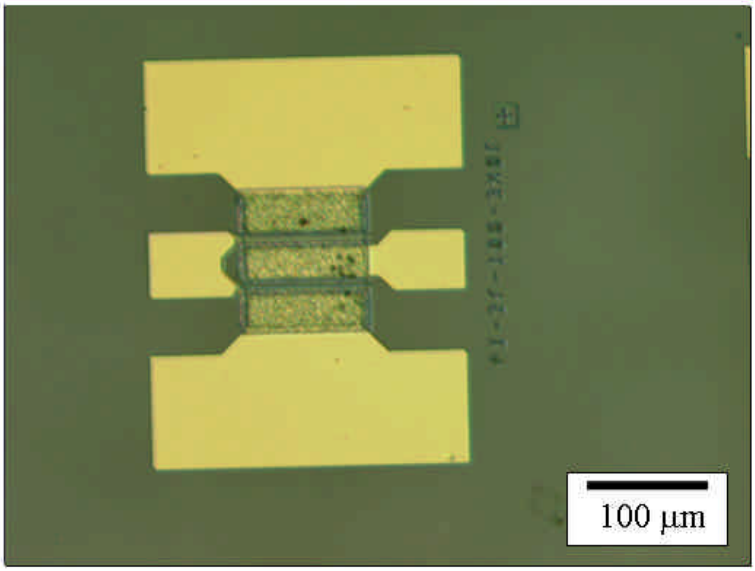
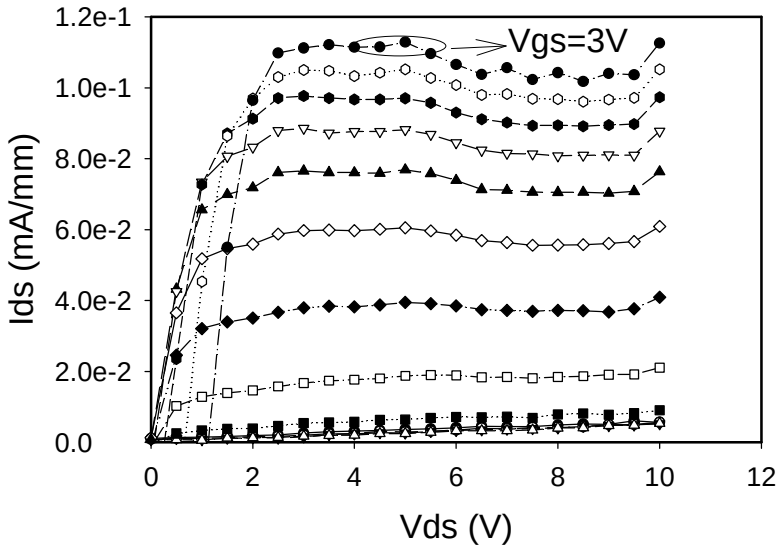


Figure 4.5: Two gate finger GaN MESFET picture.

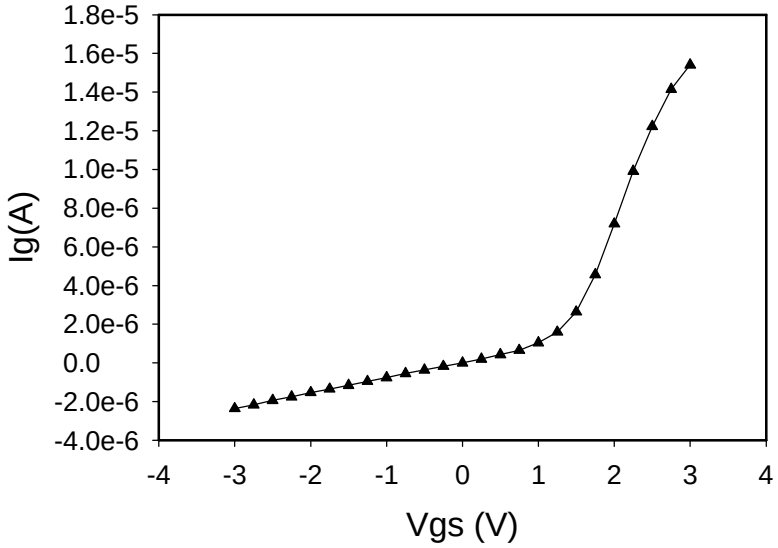
The DC electrical performance of the device is characterized by Parameter analyzer HP4142b. The device output characteristics Ids-Vds are shown in Fig. 4.6 (a) and (b). The device has a very good pinch off performance and the achieved maximum drain current normalized to device width is 67μA/mm at gate bias of 0.75 volts. From Fig. 4.6(b), the estimated gate Schottky diode is turned on at Vg=0.75V.

Similar Schottky gate leakage current is observed. And the device output characteristics shows that the drain source saturation current seems fluctuating due to light excitation. The measurement is done with indoor light on, with the light excitation, the electron generation and recombinations from the defect center play some roles and manifest

itself in the current at different drain bias. Close to 10 Volts, it seems there is the trend of drain current start increasing and it is caused by the device soft breakdown.



(a) Output Characteristics with gate bias from -3V to 3V at step of 0.5V. Above 0.75V we can see the gate Schottky leakage current affecting the drain current.



(b) Gate metal-semiconductor Schottky junction current with drain biased at 0V. Above 0.75V we can see the gate Schottky diode is turned on.

Figure 4.6: Output characteristics of two gate finger GaN MESFET with gate dimension of $2 \times 100\mu m \times 0.7\mu m$.

The device transfer characteristics Ids-Vgs is shown in Fig. 4.7 and Fig. 4.8. The pinch off voltage of the device is -1 Volts and the maximum transconductance is 0.0418mS/mm at Vds=10V. As the device scales down from 50μm to 0.7μm, we see the device performance degradation in both the drain current density decrease and transconductance decrease.

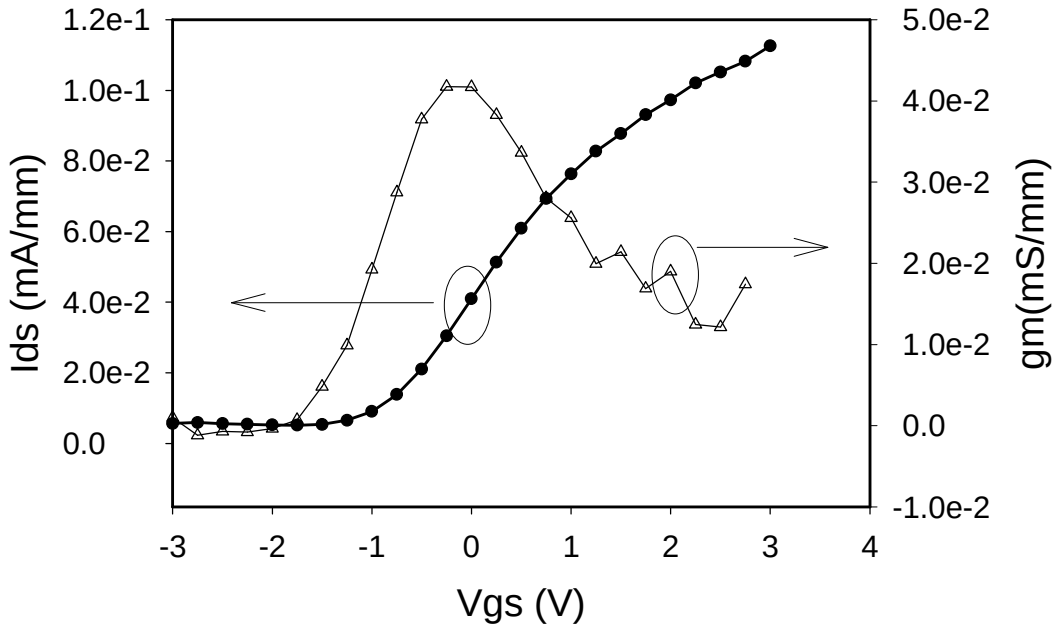


Figure 4.7: Transfer Characteristics Ids-Vgs and transconductance-Vgs at Vds= 10V.

Fig. 4.8 shows the log scale drain current, the maximum I_{on}/I_{off} ratio reaches above 100. The pinch off voltage is around -0.75 volts. This RF MESFET pinch off voltage is close to the FatFET MESFET pinch off voltage. However the two devices are different in the Ion/Ioff ratio by three orders of magnitude. The RF MESFET has a gate length of 0.7μm comparing with much larger gate length 50μm of the FatFET, we see the short channel effect comes into play a significant role when device scales.

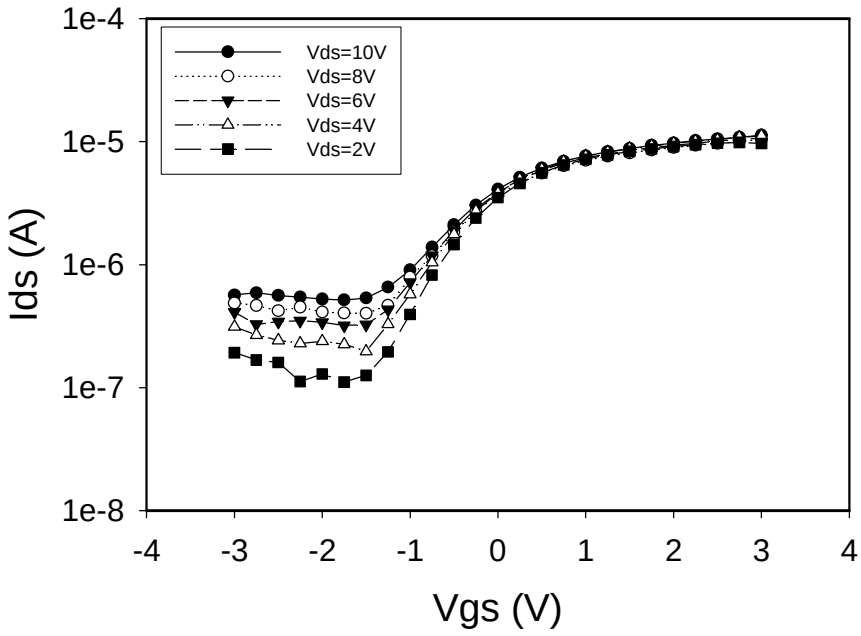
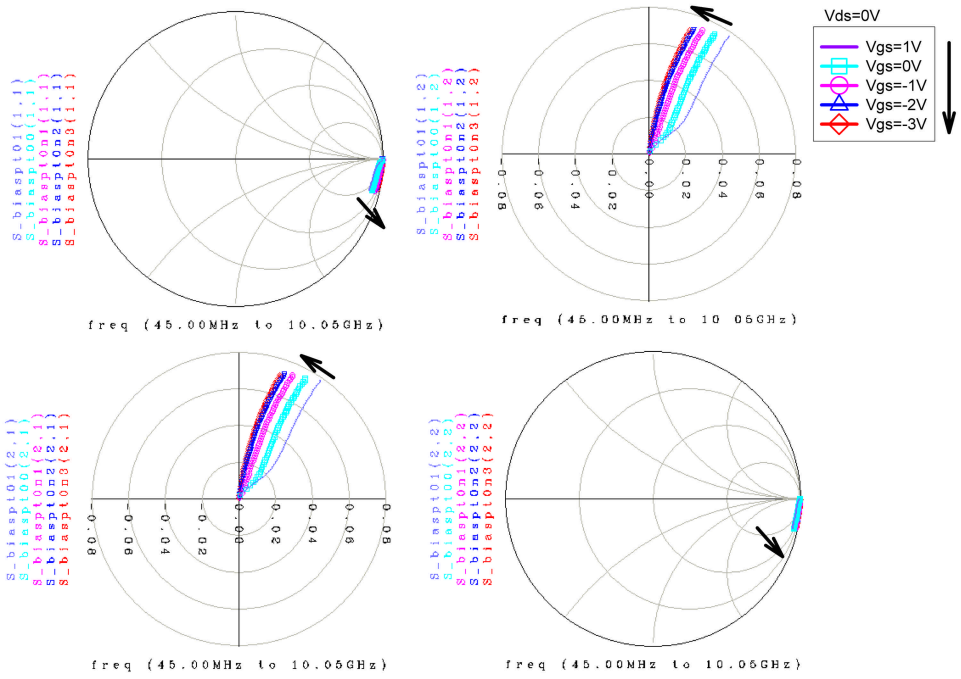


Figure 4.8: Transfer Characteristics Ids-Vgs in Semi-log scale. The drain bias Vds is from 2V to 10V at step of 2V.

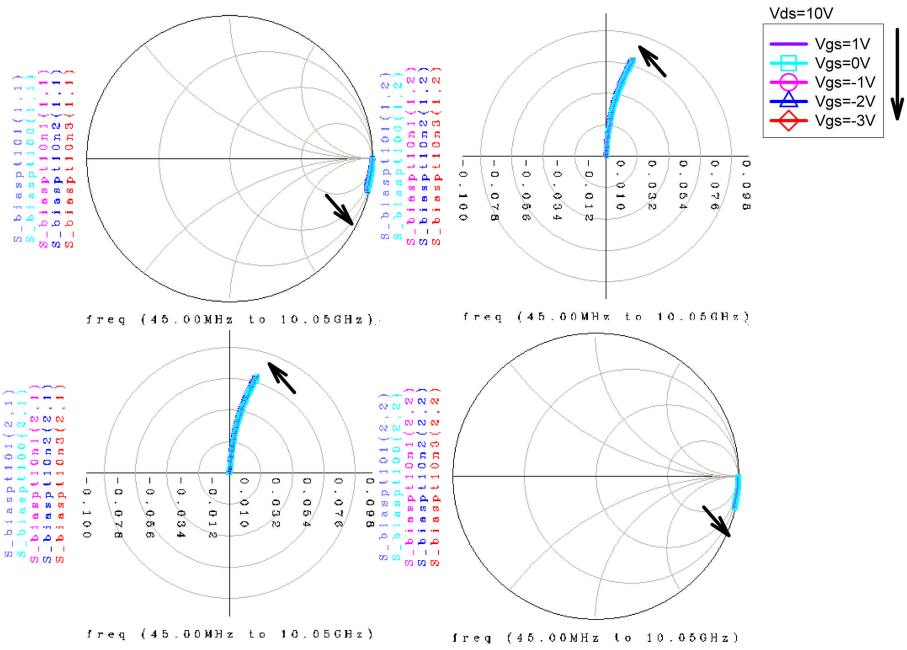
4.3.2 S Parameters Characteristics and Small Signal Model

The RF electrical performance of the device is characterized by a vector network analyzer HP8105B. The network analyzer has a 45MHz to 10GHz measurement range. GSG (ground signal ground) probes are used for the calibration and device characterizations. Short Open Load Thru (SOLT) calibration standards provided with the GSG probes are used to calibrate the system before measurement. This is also called off-wafer calibration because the calibration standards are located on different calibration substrates rather than on the device wafer. Using off-wafer calibration the reference plane is located at the probe tips and the transmission line effects of the RF device pad have to be de-embedded in order to extract the intrinsic device parameters.

The HP4142B is used to DC bias the device. The S parameter measurements are done for nested sweep of gate bias from -3V to 3V at step of 0.2V and drain bias from 0V to 10V at step of 2V. The S parameter data taken are in the frequency range from 45MHz up to 10GHz. The final S parameter results are shown in Fig. 4.9(a) for V_{ds}=0V and (b) for V_{ds}=10V. The gate bias range shown is from -3V to 1V to reflect the nominal MESFET operation biases. Therefore the S parameter data at gate bias above the turn on voltage of the GaN MESFET gate Schottky diode is not shown here.



(a) V_{ds}=0V



(b) V_{ds}=10V

Figure 4.9: Scattering Parameters results from 45MHz to 10GHz with drain bias at (a) 0V and (b) 10V.

The S parameters of the GaN MESFET show that at different bias conditions there is very little influence by channel on and off condition. Very low carrier density and high ohmic contact resistance make the reflection parameters S11 and S22 more capacitive. And this condition is very similar comparing with our GaN SB-MISFET characterization which is described in detail in next chapter of this dissertation. The equivalent circuit model of the GaN MESFET is shown in figure 4.10 with the intrinsic FET model and the parasitic elements. This is a general equivalent circuit model of a FET, the extrinsic elements such as the RF pad inductance and RF pad capacitance can be extracted and the intrinsic GaN MESFET elements can be obtained through de-embedding.

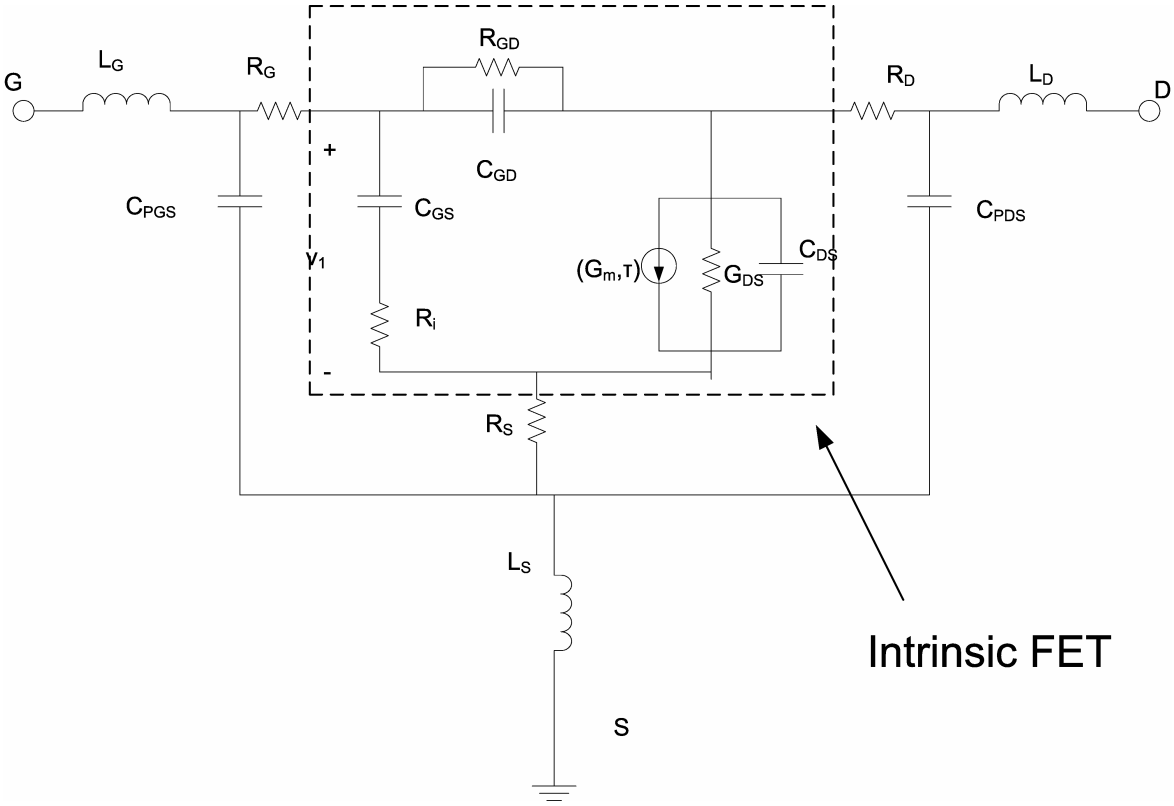


Figure 4.10: The extrinsic GaN MESFET small signal model

4.3.3 ColdFET Extraction

The detailed MESFET, and MOSFET intrinsic parameters extraction method can be found in [3] and alternative method to extract intrinsic parameters can be found in detail for MESFET and HEMT in [4]. In this work, the extraction method using coldFET method in [3] is used for the GaN MESFET.

The reverse coldFET is used to extract the parasitic capacitance. The MESFET gate is biased below pinch off, the drain is biased at zero volts, therefore no DC current flows in the device. Under this circumstance, the device small signal model can be simplified to capacitance network as shown in figure 4.11. For symmetric device, the gate to source capacitance C_{GS} is equal to the gate to drain capacitance C_{GD}, and we can set it as C_{dep}. The source to drain capacitance C_{DS} is much smaller than the other components and is negligible.

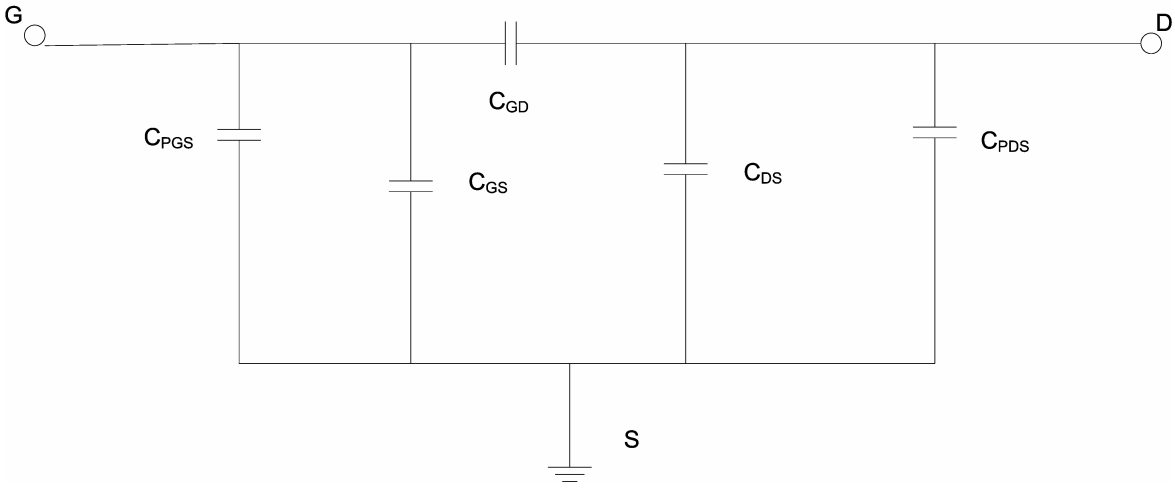


Figure 4.11: The reverse coldFET small signal model

The Y parameters of the network at low frequencies will only include extrinsic elements C_{PGS}, C_{PDS} and the depletion capacitances C_{GS} and C_{GD} with the common value of C_{dep}. The Y parameters can be written as:

$$Y_{11} = jw(C_{PGS} + 2C_{dep}) \tag{4.2}$$

$$Y_{12} = Y_{21} = -jwC_{dep} \tag{4.3}$$

$$Y_{22} = jw(C_{PDS} + C_{dep}) \tag{4.4}$$

From equations 4.2 to 4.4, the RF pad capacitances can be derived as:

$$C_{PGS} = \frac{imag(Y_{11} + 2Y_{12})}{w} \tag{4.5}$$

$$C_{PDS} = \frac{imag(Y_{22} + Y_{12})}{w} \tag{4.6}$$

The extracted RF pad capacitances for a 2 × 100 μm × 0.7 μm GaN MESFET is shown in figure 4.12. And the extracted low frequency C_{PGS} is 24.04 fF and C_{PDS} is 22.53 fF.

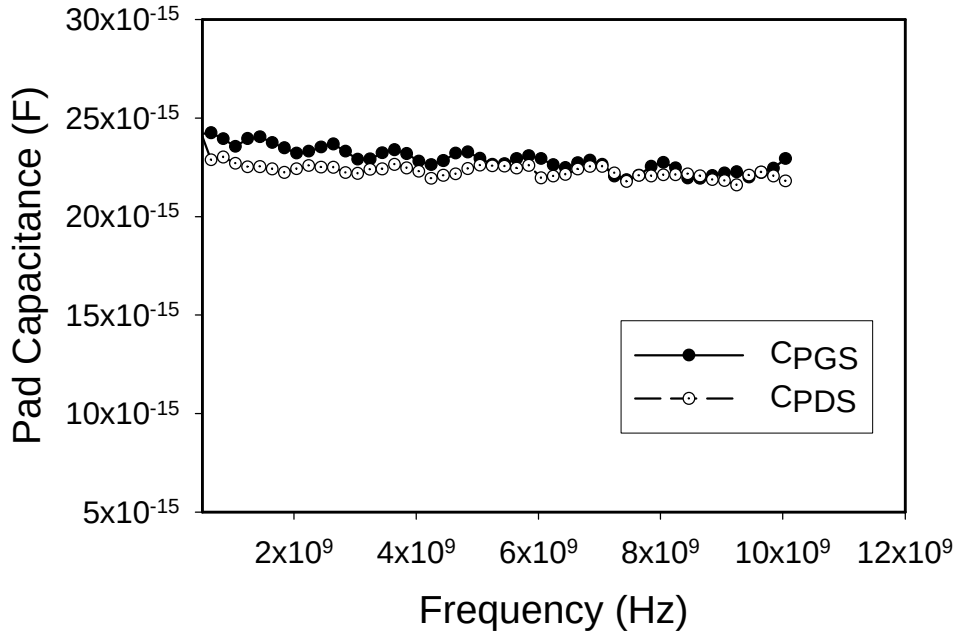


Figure 4.12: The extracted RF pad capacitances

The forward coldFET is used to extract the series resistance and series inductance. The MESFET gate is forward biased above gate turn on voltage, the drain is biased at zero volts. The gate depletion region becomes small with forward gate bias. Under this circumstance, the device small signal model is shown in figure 4.13. From the small signal model, the Z parameters can be obtained as:

$$Z_{11} = R_G + R_S + R_D + \frac{Rc}{2} + jw(L_G + L_S) \tag{4.7}$$

$$Z_{12} = R_S + \frac{Rc}{2} + jwL_S \tag{4.8}$$

$$Z_{22} = R_D + R_S + \frac{R_C}{2} + jw(L_D + L_S) \tag{4.9}$$

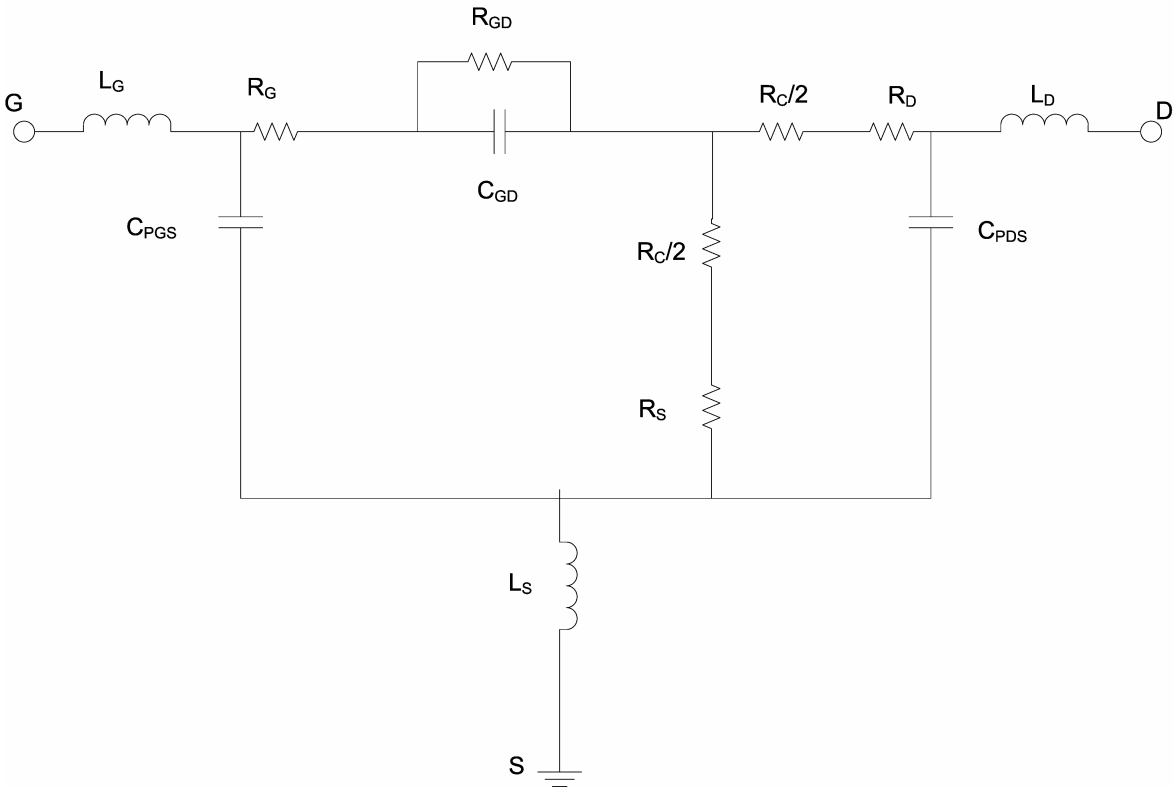


Figure 4.13: The forward coldFET small signal model

In deriving above Z parameters, based on the condition that the gate Schottky diode is fully turned on. As a result R_{GD} increases exponentially while C_{GD} increases much slower. Therefore the assumption that $\omega^2 C_{GD}^2 R_{GD}^2 << 1$ is used and the C_{GD} can be ignored.

The series resistances and inductances can be calculated from Z parameters from forward coldFET measurements:

$$R_S = real(Z_{12}) \tag{4.10}$$

$$R_D = real(Z_{22} - Z_{12}) \tag{4.11}$$

$$R_G = real(Z_{11} - Z_{12} - R_D) \tag{4.12}$$

$$wL_S = imag(Z_{12}) \tag{4.13}$$

$$wL_D = imag(Z_{22} - Z_{12}) \tag{4.14}$$

$$wL_G = imag(Z_{11}) - wL_S \tag{4.15}$$

Figure 4.14 shows the extracted series resistances, at high frequency the source series resistance R_S is 26.8 Ohm, the drain series resistance R_D is 45.7 Ohm, and the gate series resistance R_G is 88.9 Ohm.

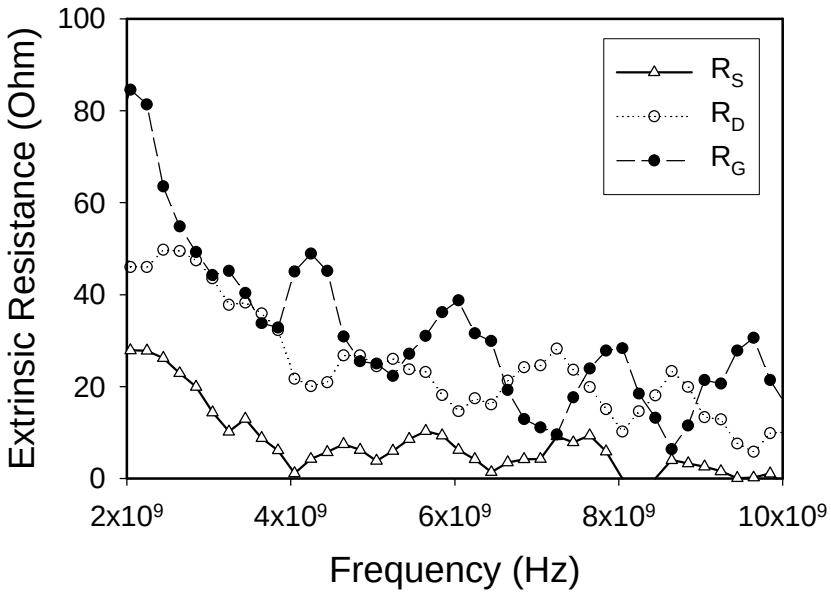


Figure 4.14: The extracted series resistance

Figure 4.15 shows the extracted series inductances. At high frequency the source series inductance L_S is 26.8 Ohm, the drain series inductance L_D is 45.7 Ohm, and the gate series inductance L_G is 88.9 Ohm. The inductances show negative values and are saturated at high frequency. The capacitive results show that the extra Schottky diode effect by the metal contact Ti/Al/Ni/Au (15nm/150nm/80nm/80nm) on the cap layer i-GaN. At this frequency range, the source/drain diode depletion capacitance is dominant in the imaginary part of Z parameters. The small signal model re-considered after adding the source/drain diode model is shown in figure 4.16.

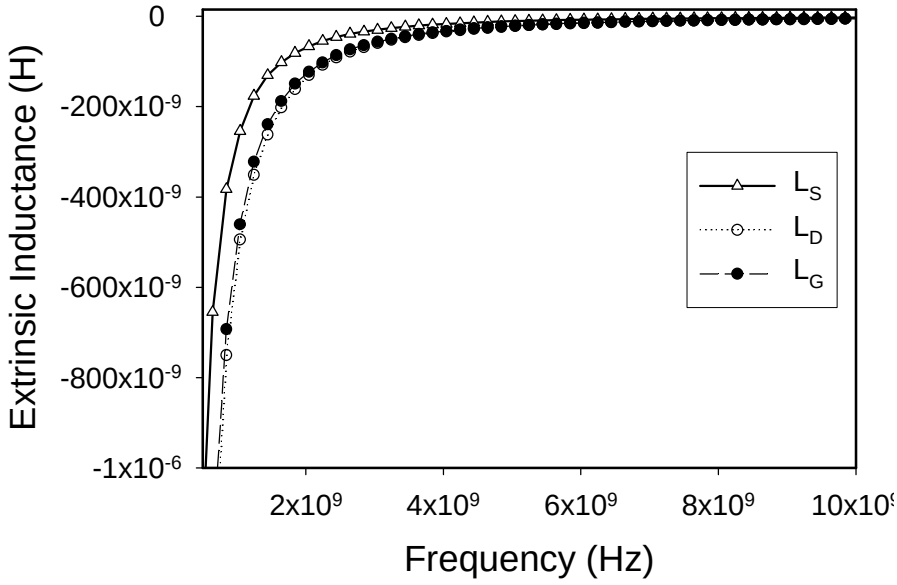


Figure 4.15: The extracted series inductance.

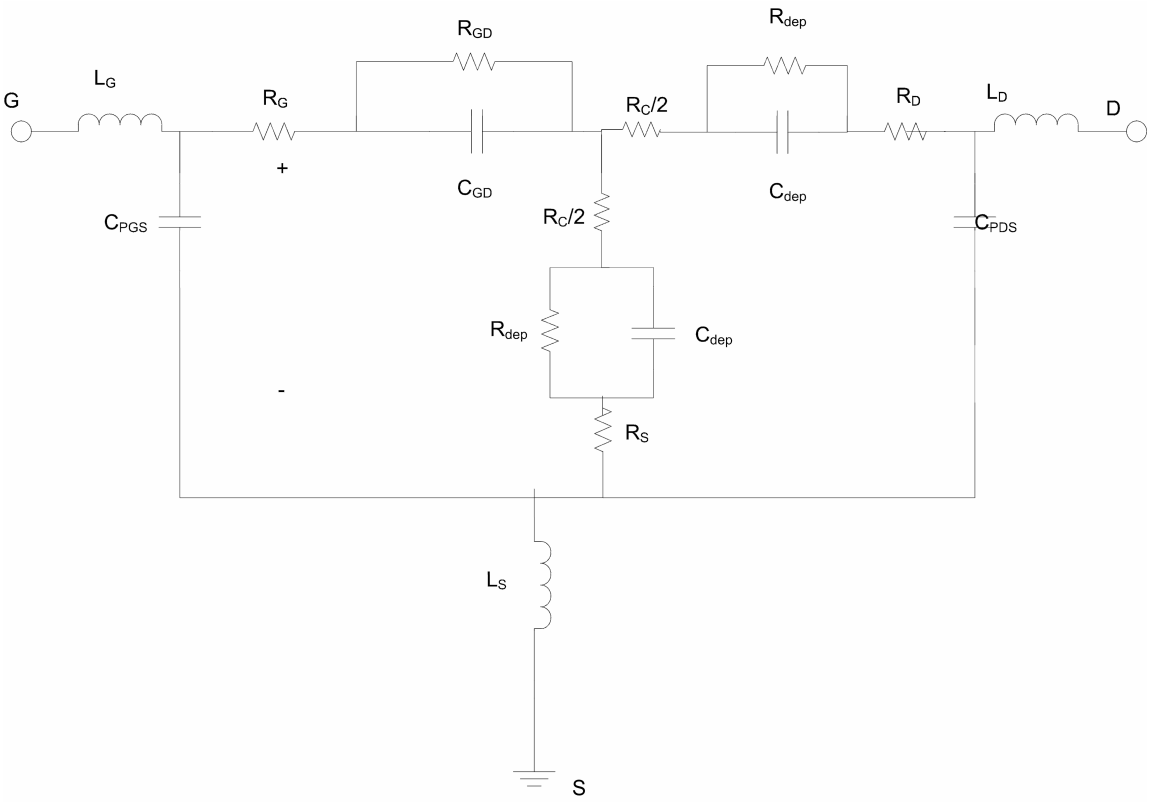


Figure 4.16: The forward coldFET small signal model with added source/drain diode model.

The extracted series inductances after considering the source/drain diode are calculated as:

$$L_S^{'} = \frac{imag(Z_{12})}{w} = L_S - \frac{R_{dep}^2 C_{dep}}{1 + w^2 C_{dep}^2 R_{dep}^2} \tag{4.16}$$

$$L_D^{'} = \frac{imag(Z_{22} - Z_{12})}{w} = L_D - \frac{R_{dep}^2 C_{dep}}{1 + w^2 C_{dep}^2 R_{dep}^2} \tag{4.17}$$

$$L_G^{'} = \frac{imag(Z_{11} - Z_{12})}{w} = L_G - \frac{R_{dep}^2 C_{dep}}{1 + w^2 C_{dep}^2 R_{dep}^2} \tag{4.18}$$

The L_S', L_D' and L_G' are the extracted negative series inductances due to the source/drain depletion capacitance effect as shown in figure 4.15. The actual series inductances from the forward coldFET model in figure 4.16 can be calculated as:

$$L_S = \frac{imag(Z_{12})}{w} + \frac{R_{dep}^2 C_{dep}}{1 + w^2 C_{dep}^2 R_{dep}^2} \tag{4.19}$$

$$L_D = \frac{imag(Z_{22} - Z_{12})}{w} + \frac{R_{dep}^2 C_{dep}}{1 + w^2 C_{dep}^2 R_{dep}^2} \tag{4.20}$$

$$L_G = \frac{imag(Z_{11} - Z_{12})}{w} + \frac{R_{dep}^2 C_{dep}}{1 + w^2 C_{dep}^2 R_{dep}^2} \tag{4.21}$$

The series inductances L_S, L_D and L_G are in the range from several pH to tens of pH, and the second terms with depletion capacitances in equation 4.16, 4.17 and 4.18 are in the tens of nH. Therefore the depletion capacitance term is dominant in the overall imaginary part of the Z parameter.

4.3.4 Intrinsic Device parameter Extraction

Fortunately, with the extracted overall series inductances L_S', L_D' and L_G', after parasitic de-embedding as shown in Appendix C, the intrinsic parameters of the MESFET can be extracted from the intrinsic Y parameters using the following equations.

$$Y_{11} = \frac{1}{R_{GD}} + \frac{R_i C_{GS}^2 w^2}{1 + w^2 R_i^2 C_{GS}^2} + jw\left(\frac{C_{GS}}{1 + w^2 R_i^2 C_{GS}^2} + C_{GD}\right) \tag{4.22}$$

$$Y_{12} = -\frac{1}{R_{GD}} - jwC_{GD} \tag{4.23}$$

$$Y_{21} = \frac{g_m e^{-jwt}}{1 + jwR_i C_{GS}} - \frac{1}{R_{GD}} - jwC_{GD} \tag{4.24}$$

$$Y_{22} = \frac{1}{R_{GD}} + g_{DS} + jw(C_{DS} + C_{GD}) \tag{4.25}$$

The gate capacitances C_{GS}, C_{GD} and output conductance G_{DS} can be calculated from intrinsic Y parameters:

$$C_{GD} = -\frac{imag(Y_{12})}{w} \tag{4.26}$$

$$\frac{C_{GS}}{1 + w^2 R_i^2 C_{GS}^2} = \frac{imag(Y_{11} + Y_{12})}{w} \tag{4.27}$$

$$g_{DS} = real(Y_{12} + Y_{22}) \tag{4.28}$$

With Ri in several Ohm, C_{GS} in fF, so the assumption $\omega^2 C_{GS}^2 R_i^2 << 1$ is used to simplify equation 4.27 to:

$$C_{GS} = \frac{imag(Y_{11} + Y_{12})}{w} \tag{4.28}$$

For small gate length device such as 0.7μm, the traditional C-V measurement is not applicable. Therefore the gate capacitance can be extracted from the S parameter measurements. Fig. 4.17, 4.18 and 4.19 show the extracted gate capacitances of the GaN MESFET at zero drain bias.

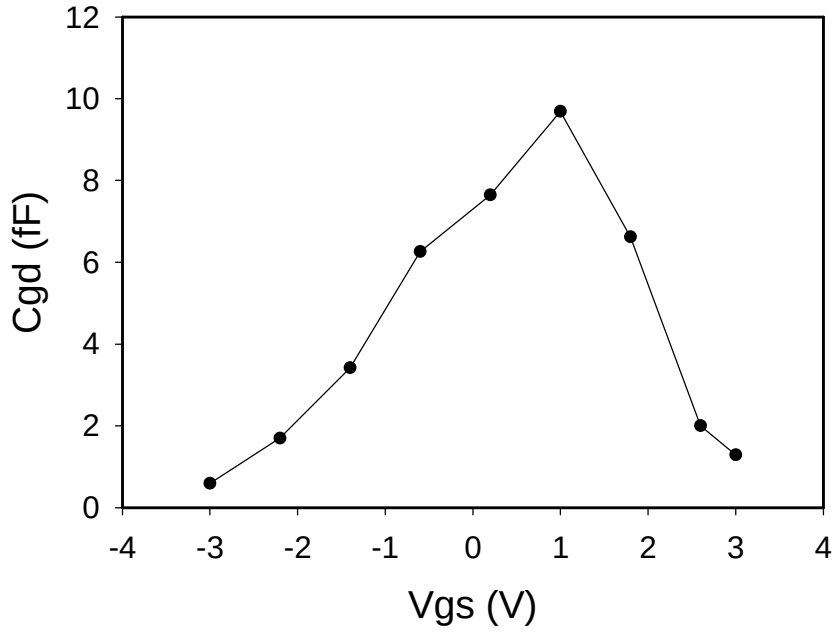


Figure 4.17: Extracted gate capacitance Cgd at 1.5GHz, with zero drain bias.

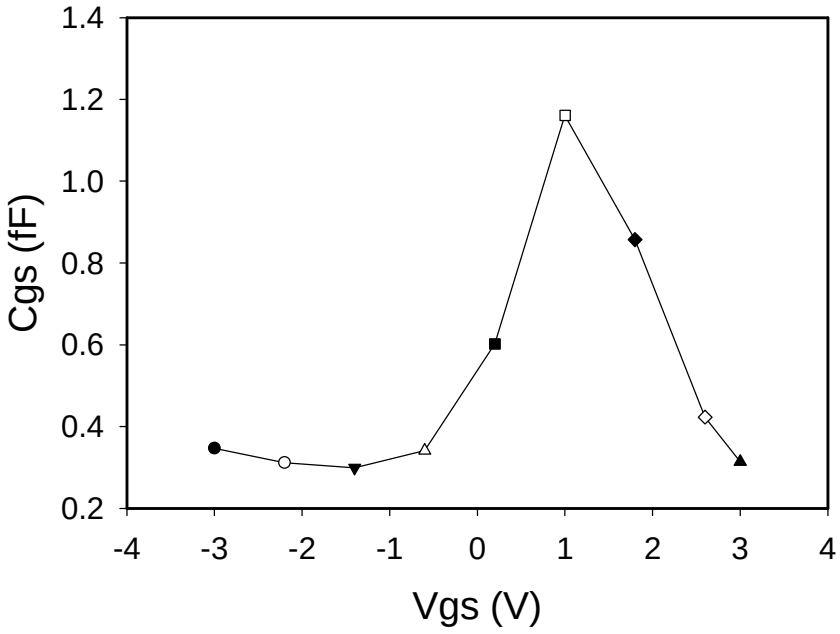


Figure 4.18: Extracted gate capacitance Cgs at 1.5GHz, with zero drain bias

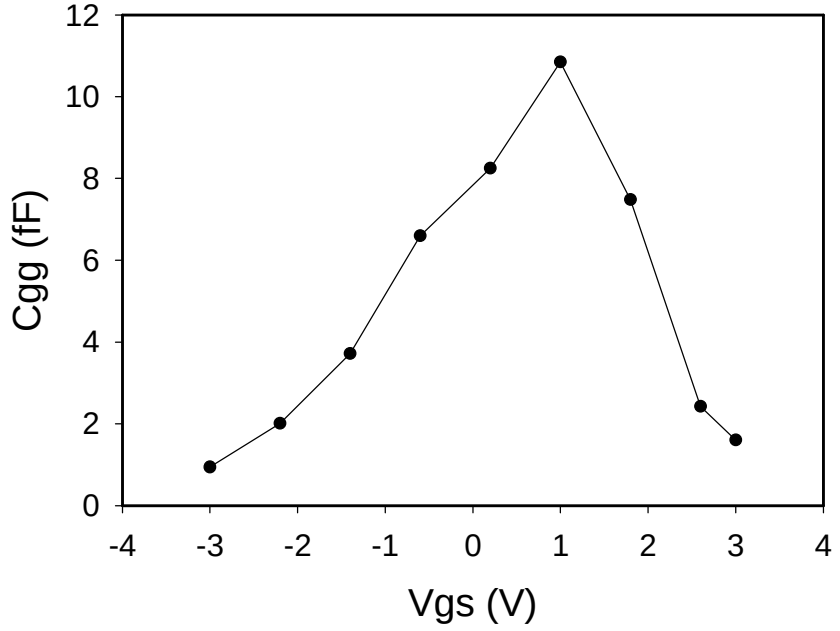
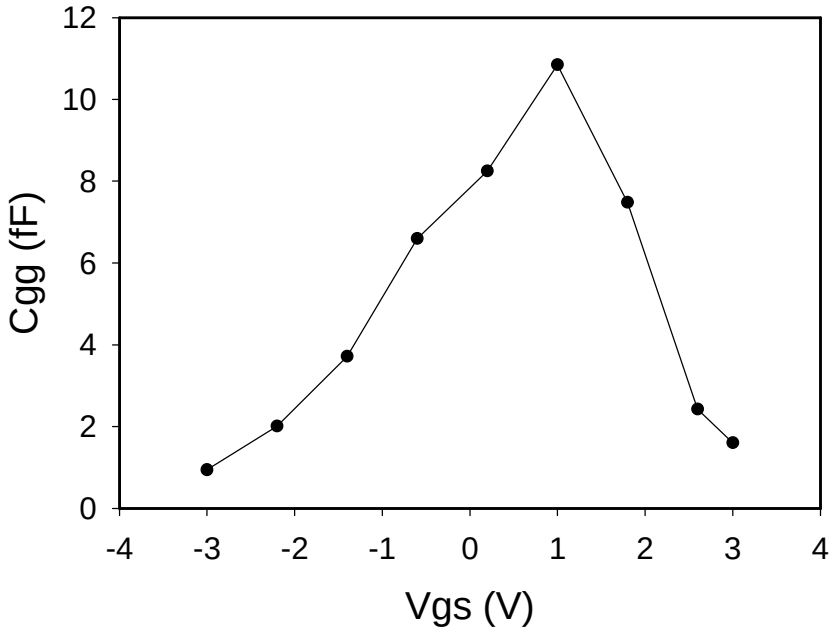


Figure 4.19: Extracted gate capacitance Cgg at 1.5GHz, with zero drain bias

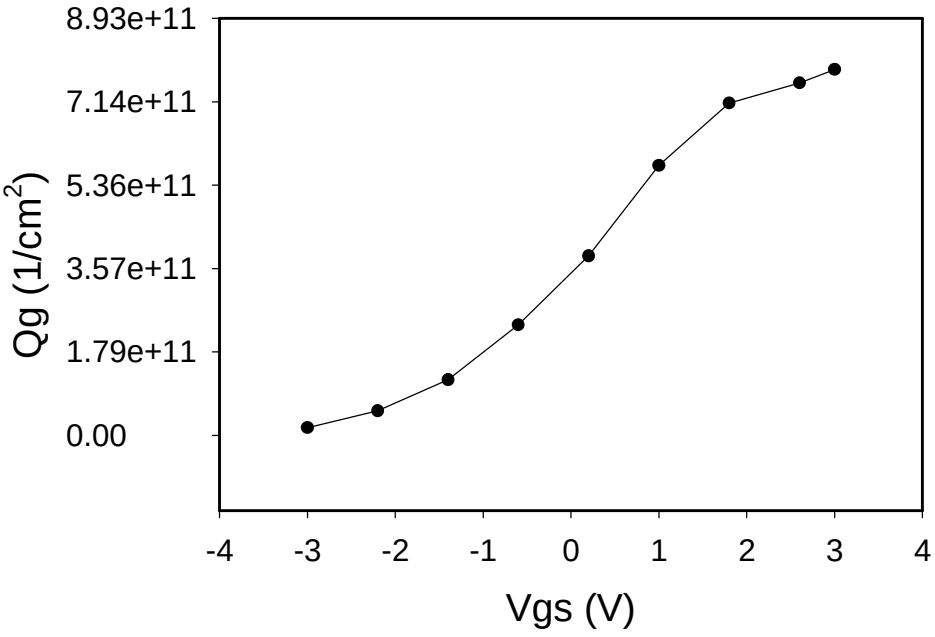
The extracted gate capacitance shows the trend of gate bias dependence. The increase of gate capacitances confirms that the device channel depletion region is modulated by gate bias. The gate capacitance extraction is in the range from 1 GHz up to 10GHz, and the figure shows 1.5GHz capacitances only. The extracted gate capacitances agree with high frequency C-V measurement in general depletion mode MOSFET and MISFET.

$$Q_s = \frac{1}{W * L}\int_{V_T}^{Vgs} C_{gc} dV_g \qquad (4.29)$$

The sheet charge controlled by gate capacitor can also be extracted by integrating the gate capacitance with respect to the gate bias as shown in above equation 4.29. Fig. 4.20 shows the extracted sheet charge for the 2×100μm×0.7μm GaN MESFET.



(a) Sheet charge integrated from Cgg.



(b) Sheet charge integrated from Cgg, normalized with gate area

Figure 4.20: Extracted sheet charge Qg at 1.5GHz, with zero drain bias.

We notice that after converting the sheet charge to the unit of $1/cm^2$, the MESFET sheet charge is in the order of 0 to $8.93 \times 10^{11}\ cm^{-2}$. This number is low comparing to the sheet charge density $1 \times 10^{13}\ cm^{-2}$ of 2DEG in GaN HEMT. This explains the low current and low transconductance of our device. To improve the device performance, the sheet charge has to be increased at least by one order of magnitude.

The output conductance is defined as the derivative of the Ids with respect to Vds as shown in the following equation:

$$G_{DS} = \frac{\partial I_{DS}}{V_{DS}} = \frac{m_{eff} W Q_S}{L} \tag{4.30}$$

The effective mobility can be calculated if the sheet charge Qs is known. The procedure to calculate low field effective mobility is shown in the following equation 4.31. The extracted output conductance is shown in Fig. 4.21 and the calculated low field mobility is shown in Fig. 4.22.

$$m = \frac{L^2 G_{ds}}{Q_s} \tag{4.31}$$

The output conductance is proportional to the sheet charge density; therefore it increases with the increasing of gate bias up to 0.75V. The peak in the output conductance is mainly introduced by the gate Schottky leakage which is pronounced when gate bias is above 0.75V. Therefore the output conductance and mobility extraction results are only useful for the gate bias lower than 0.75V.

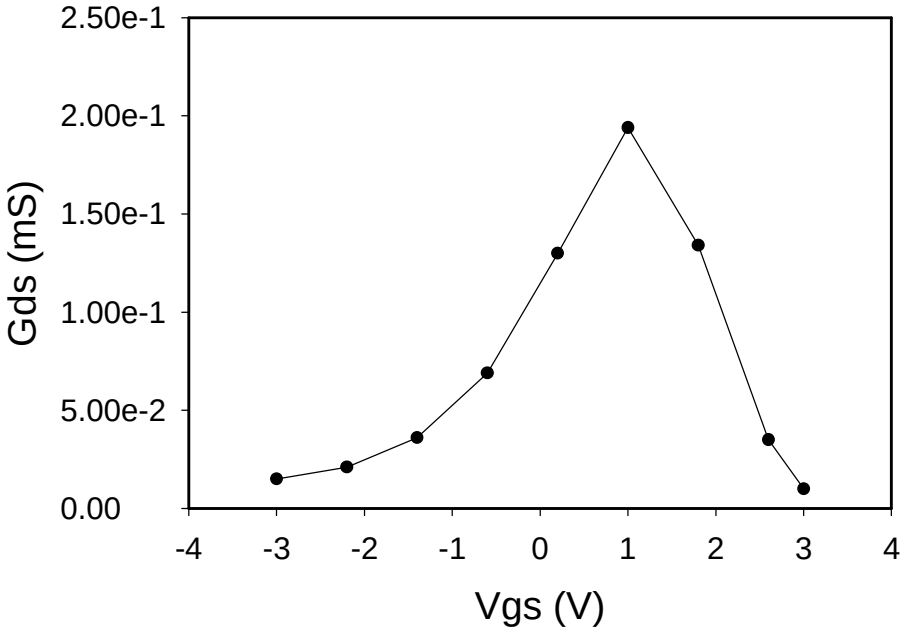


Figure 4.21: Extracted output conductance at 1.5GHz, at zero bias.

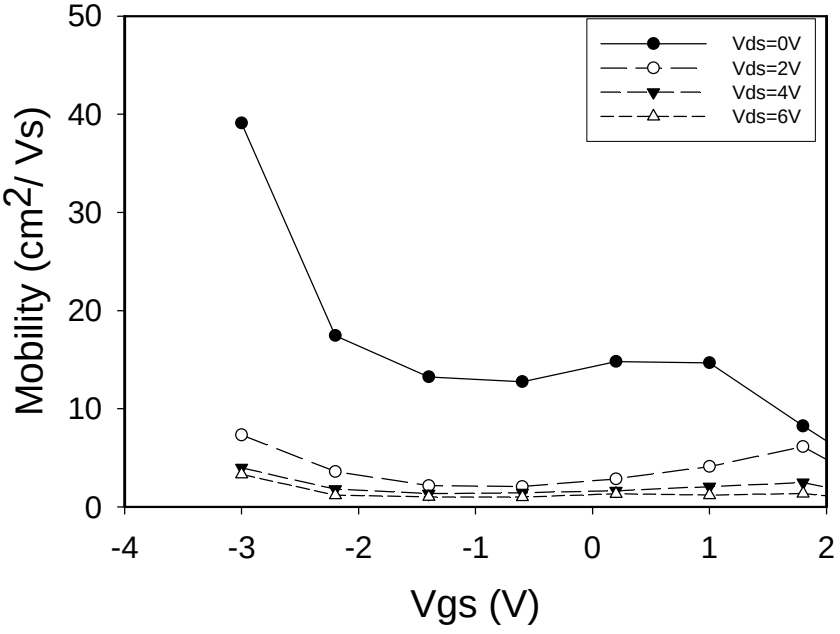


Figure 4.22: Calculated mobility vs. gate bias

The low field channel mobility in this pulse doped channel GaN MESFET reaches a maximum of 40 cm^2/Vs at low horizontal electric field which correspond to the calculated mobility at zero drain bias. As the gate bias increases, the mobility decreases because more carriers attracted to the GaN surface region where the surface roughness scattering is pronounced. As the drain bias increases, the channel mobility decreases sharply to below 10 cm^2/Vs. These mobility values are based on assumption that the device is biased on linear region. For drain bias above 2 volts, the device enters the saturation region already therefore these mobility values are not calculated with the valid assumption. However all these mobility values fall in range of the mobility for bulk GaN material. And the channel mobility of the MESFET is much less than the highest mobility achieved in two dimensional electron gas (2DEG) formed in GaN HEMT indicating the ionized donor scattering is very large in the pulsed doped channel layer.

4.4 Summary

In this chapter, the pulse doped concept for GaN material has been introduced. The pulse doped GaN material has been used to fabricate GaN MESFET. The DC and RF characterization results of tow devices are demonstrated in details. For the FatFET with a gate length of 50μm and a gate width of 100μm, the highest drain current normalized to device gate width achieved is 0.08mA/mm at gate bias of 0.75V, and the peak transconductance achieved is 0.134mS/mm. The I_{on}/I_{off} ratio of this device reaches 5 orders of magnitude. The MESFETs have a good pinch off performance with a pinch off voltage of -0.75V which agrees well with the theoretical calculation of the GaN doping profile. For the two gate finger MESFET with gate length of 0.7μm and gate width of 100μm, the highest

drain current achieved is 0.067mA/mm at gate bias of 0.75 V, and the peak transconductance achieved is 0.0418mS/mm. The I_{on}/I_{off} ratio of this device reaches 2 orders of magnitude. And the pinch off voltage is around -0.75V. Furthermore the high frequency S parameter measurements on this device are conducted from 45MHz up to 10GHz. The equivalent circuit model of the MESFET device is studied and the device extrinsic parasitic elements are extracted using coldFET technique. The intrinsic device model is obtained after de-embedding. Several key device parameters such as gate capacitance, sheet charge density, output conductance and effective channel mobility are calculated from the intrinsic device Y parameters. The sheet carrier concentration reaches up to around $7\times10^{11}cm^{-2}$, and the low field mobility reaches up to 40 cm^2/Vs. All these values achieved falls in range of the reasonable value of GaN MOSFET and MISFET which proves that this pulse doped channel concept in GaN material growth is very promising for current and future GaN electronic device research and development.

To improve the device performance, several issues have to be addressed including: 1) the channel doping concentration can be increased in order to increase the drain current which is currently the key parameter that falls much behind of the GaN HEMT devices. 2) the pulse doping width can be also increased to increase the overall channel carrier concentration. Both 1) and 2) can be considered to balance the trade off between the pinch off voltage and the maximum drain current drive. 3) using better quality GaN material with high bulk mobility. To be able to compete with GaN HEMT technology, the channel mobility has to be improved to a value close to the mobility of HEMT 2DEGs.

Reference

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[3] Krishnanshu Dandu, “Characterization and modeling of III-N MOS-HFETs for high frequency applications,” *Ph.D. Dissertation, NC* State University, 2006.

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Chapter 5

Demonstration of a Depletion Mode GaN Schottky Barrier MISFET

This chapter demonstrates the first time a depletion mode GaN Schottky barrier MISFET to our best knowledge. The chapter starts with a brief introduction of the GaN SB-MISFET device processing steps for a device fabricated on GaN film grown by MOVPE on sapphire. The DC characterization of the fabricated GaN SB-MISFET are shown for FatFET device with gate dimension of 100μm × 50μm and RFFET device with gate dimension of 2×100μm × 0.7μm. Furthermore, this is the first time demonstration of such small gate length GaN MISFET with the capability of doing high frequency characterization. The RF characterization of the low dimension device with gate length of 0.7 μm is shown. Several key device parameters such as gate capacitance, sheet carrier concentration, output conductance, and low field mobility have been extracted from the high frequency S parameter measurements. Detailed analysis and comments on these GaN SB-MISFET have been included in the chapter along with the presentation of the device electrical

characteristics. The chapter ends with a summary of these novel GaN SB-MISFETs performance and some discussions on the possibility to improve the device performance.

5.1 Dielectric

SiO_2, Si_3N_4, Ga_2O_3, Gd_2O_3, MgO, et al. have been successfully demonstrated as the gate dielectric on GaN MOSFET device since the first demonstration of GaN MOSFET in 1998 [1-11]. According to [3], SiO_2 and Si_3N_4 have been successfully deposited on GaN film and low interfacial states density $1x10^{11}$ $cm^{-2}eV^{-1}$ was achieved. From chemical bonding point of view, Si_3N_4 and GaN both have nitrogen atoms in their molecules. Therefore for a nitrogen terminated GaN surface with the dangling nitrogen bond, Si_3N_4 can form the silicon to nitrogen bond easily. Si_3N_4 is used for surface passivation on GaN HEMT devices [12-15]. I believe it should also be one the most suitable gate dielectric materials for GaN MOSFET devices. Another suitable gate dielectric material for GaN MOSFET is Ga_2O_3/Gd_2O_3 which has been demonstrated on both GaN MOSFET and GaAs MOSFET devices [16-18].

In this work, 150nm Si_3N_4 film is deposited as the gate dielectric using plasma enhanced chemical vapor deposition (PECVD) at 200 °C.

5.2 Schottky Metal Source/Drain

Schottky metal as source/drain contacts serve the purpose of providing electrons carrying electrical current into and out of the semiconductor. In this work, nickel is selected as the Schottky metal for source/drain mainly because of it can form stable Schottky contact on n-GaN, and its work function is 5.15eV which is around the mid-gap of GaN, therefore it

has the potential of being used as a common gate metal for both n type and p type GaN Schottky barrier MOSFET which reduces the process complexity. Titanium, chromium, and aluminum have also the potential of being used as the Schottky metal for the source/drain because of their specific work function and low Schottky barrier height with GaN [19]. Actually the first enhancement GaN SB-MOSFET is demonstrated with aluminum as the source/drain metal, where the output characteristics do not show the Schottky barrier mainly because aluminum work function is really close to the conduction band energy of GaN, and aluminum contact on n-GaN surface with appropriate annealing results with low Schottky barrier height and even ohmic contact can be achieved. [20] [21]

5.3 GaN Schottky Metal Source/Drain MOSFET Device Operating Mechanism

The basic idea of the SB-MOS band diagram is shown here. The space charge is shown as the grey color in the depletion regions in the surfaces of both metal and semiconductors. The mobile charge is shown as the green color in the conduction band (electron) or valence band (hole) as the semiconductor conducting type changes. The gate bias controls the conducting type of the device mainly in accumulation or inversion.

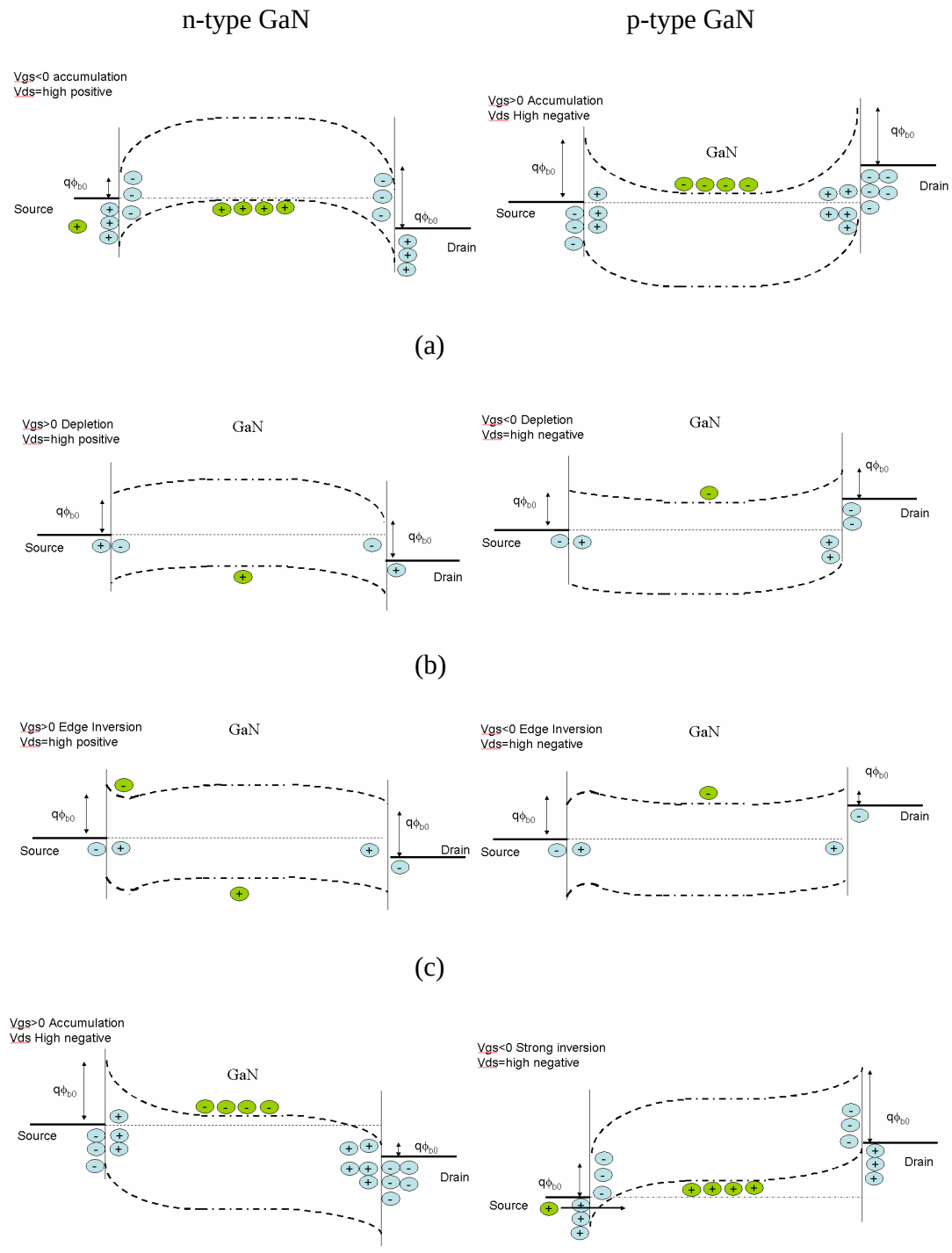


Figure 5.1: Schematic Band diagram of GaN Schottky Barrier NMOS and PMOS under different biases (a) Accumulation. (b) Depletion. (c) Edge inversion. (d) Inversion.

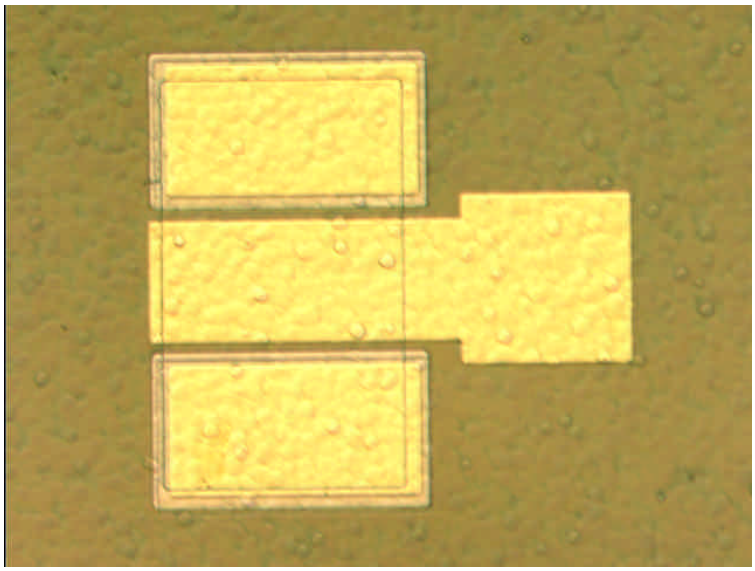
As the absolute gate bias keeps increasing (for PMOS the gate bias is negative), both n type semiconductor and p type semiconductor under the gate area are going through the accumulation, depletion, edge inversion, and total inversion steps. During accumulation and depletion there is very few electrons or holes can surmount the Schottky barrier by thermionic emission, therefore the current is very low and the device is in off state. As the gate bias keep increasing, the channel layers adjacent to the source and drain will get into the inversion first due to the external Schottky contact. As the gate voltage further increases, the total channel will get into inversion and the conducting channel forms due to both thermionic emission and tunneling through the Schottky barrier on the source side. On the drain side, the drain bias makes the Schottky junction forward biased, so the carriers will go through the junction without any barrier.

5.4 GaN Schottky Barrier MISFET Experiment and DC/CV Characteristics

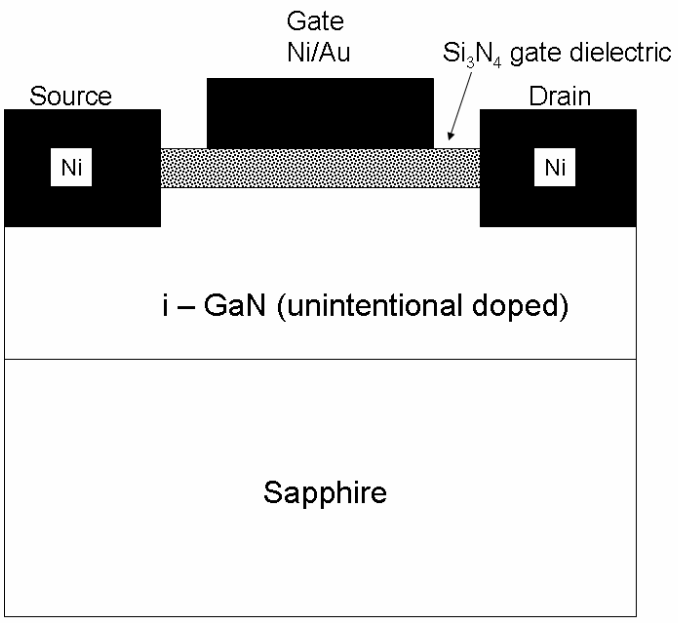
The SB-MISFET is based on GaN film grown by MOCVD on (0001) c-plane sapphire substrate. The substrate is nitridated at 1000 °C and a low temperature aluminum nitride (AlN) buffer layer was grown followed by 500nm thick unintentionally doped GaN. The device processing takes place in a class 1000 clean room.

The device mesa isolation is first formed by GaN reactive ion etching (RIE) in BCl3 plasma. Then 150nm Si3N4 is deposited as the masking layer using plasma enhanced chemical vapor deposition (PECVD). The source/drain recess area is defined by contact photo-lithography and formed using Si3N4 plasma enhanced RIE in CHF3 ambient followed

by GaN RIE in BCl3 plasma. 200nm-thick Ni is deposited in the recess area to form Schottky contact using electron-beam deposition tool. Ni/Au (100/100nm) is deposited using e-beam deposition for gate metallization. Finally 180nm-thick Au is deposited as interconnect metal. The FatFET device with gate length of 100μm and gate width of 50μm has been characterized and the device picture and device cross-section diagram are shown in Fig. 5.2(a) and (b).



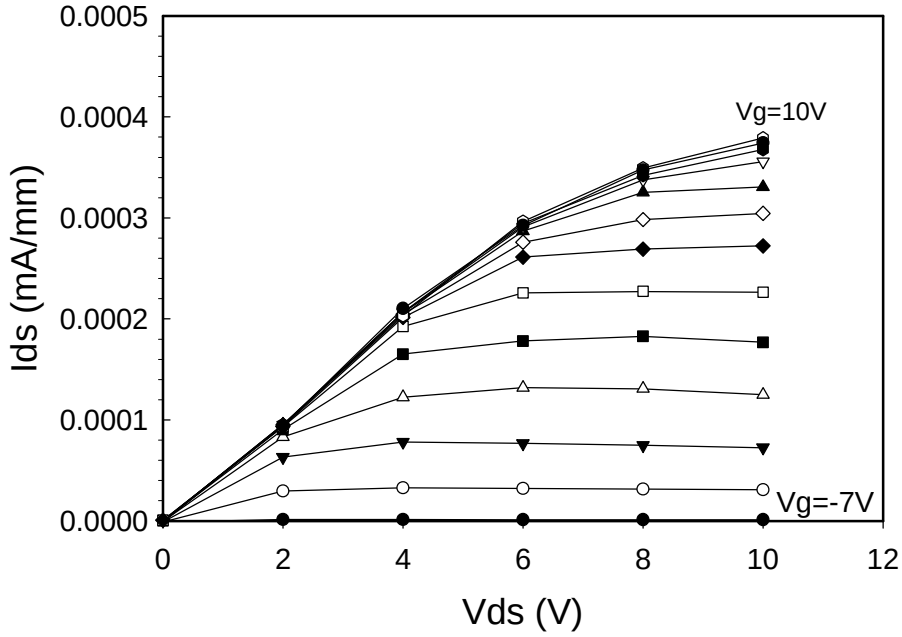
(a) FatFET picture



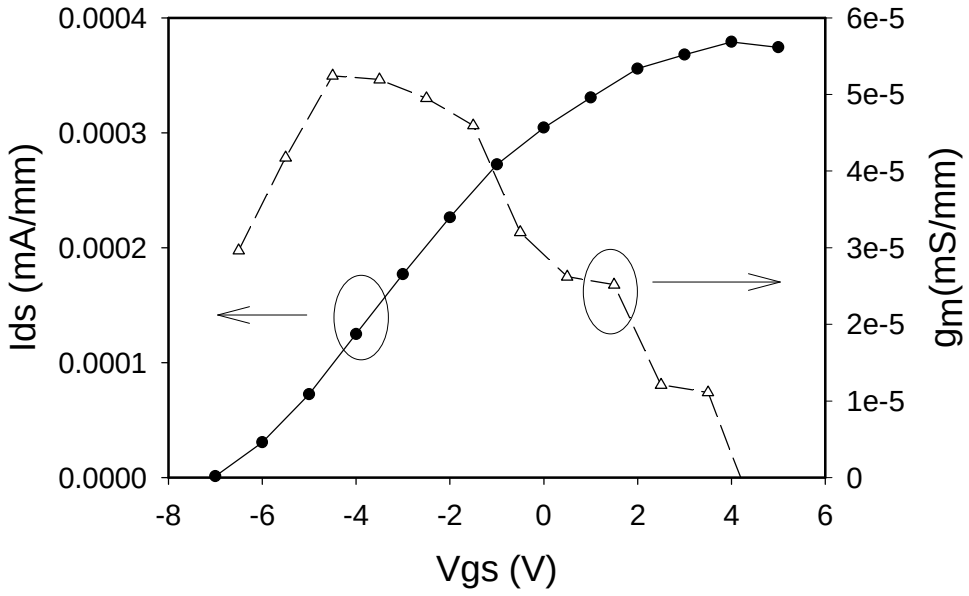
(b) FatFET cross-section

Figure 5.2: GaN SB-MISFET for DC characterization. Device picture and device cross-section.

The DC electrical performance of the device is characterized by Parameter analyzer HP4155b. The device output characteristics Ids-Vds and device transfer characteristics are shown in Fig. 5.3 (a) and (b), respectively. The device has a very low pinch off current and the achieved maximum drain current normalized to device width is 0.4μA/mm at both drain and gate bias of 10 volts. And the maximum transconductance is 0.05μS/mm at gate bias of -5 volts and drain bias of 10 volts. As the gate bias increases, the transconductance first increases and peaks at -3 V then decreases which can also be seen from the drain current spacing from the output characteristics in Fig. 5.3 (a).



(a) Output Characteristics



(b) Transfer Characteristics

Figure 5.3: Electrical characteristics of GaN SB-MISFET with gate dimension of 100μm × 50μm.

The CV performance of the device was conducted using Agilent 4279A C-V meter. The semiconductor parameter analyzer HP4155b was used to DC bias the device. The measurement is conducted with both the source and drain grounded and the gate is biased from -10V to 10V. Figure 5.3 shows the C-V characteristics of the GaN SB-MISFET with W/L =100μm/50μm at 800 KHz and 1 MHz. The MIS capacitance result shows the unintentionally doped GaN actually is n type doped. And the measured total gate capacitance is a series combination of the insulator capacitance C_i and the GaN depletion layer capacitance C_d.

$$C = \frac{C_i C_d}{C_i + C_d} \tag{5.1}$$

$$C_i = \frac{e_i}{d} \tag{5.2}$$

A simple calculation using the flat band capacitance C_{FB} as shown in equation 5.3 gives the GaN doping concentration of 1.3×10^{17} cm^{-3} which is a typical doping concentration of unintentionally doped GaN film grown by MOCVD.

$$C_{FB} = \frac{e_i}{d + \frac{e_i}{e_s} L_D} = \frac{e_i}{d + \frac{e_i}{e_s}\sqrt{\frac{kTe_s}{N_d q^2}}} \tag{5.3}$$

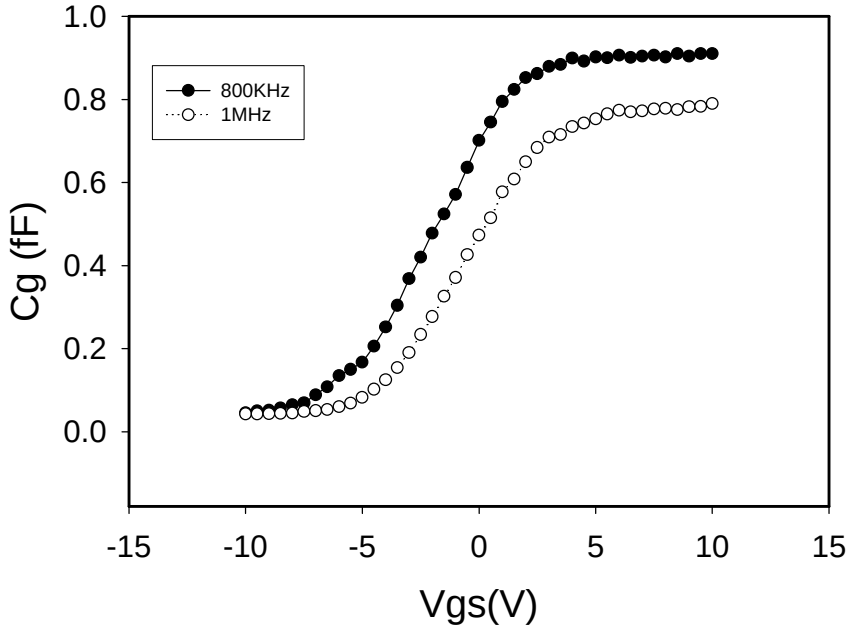


Figure 5.4: CV characteristics of GaN SB-MISFET with gate dimension of 100μm × 50μm.

Using MOSFET threshold analysis, the threshold voltage of the GaN MISFET can be derived with corresponding interfacial charge. The Ni/Au gate metal-GaN flat band voltage is mainly dictated by the interfacial charges because the metal semiconductor work function difference in this case is 0.015eV which is negligible. One assumption of GaN substrate is the intrinsic carrier density is 1×10^{10} cm^{-3}, and from the split C-V measurement the unintentionally doped GaN has an n type doping concentration of 1.3×10^{17} cm^{-3}. Because the insulating nature of the sapphire substrate, the body effect exists, with one assumption of body floating voltage of 2 volts, the calculation shows the depletion capacitance does not affect the threshold voltage of the device much (only contribute 0.0427eV). Therefore the most important parameter affecting the threshold of this GaN MISFET is interfacial charge.

$$V_{th} = V_{FB} + f_s + g\sqrt{f_F + V_{CB}} \qquad (5.4)$$

$$g = \frac{\sqrt{2e_{si}qN_a}}{C_{ox}} \tag{5.5}$$

$$f_s = 2\frac{k_B T}{q}\ln\left(\frac{N_a}{n_i}\right) = 2f_F \tag{5.5}$$

$$V_{FB} = f_{ms} - \frac{Q_i}{C_i} \tag{5.6}$$

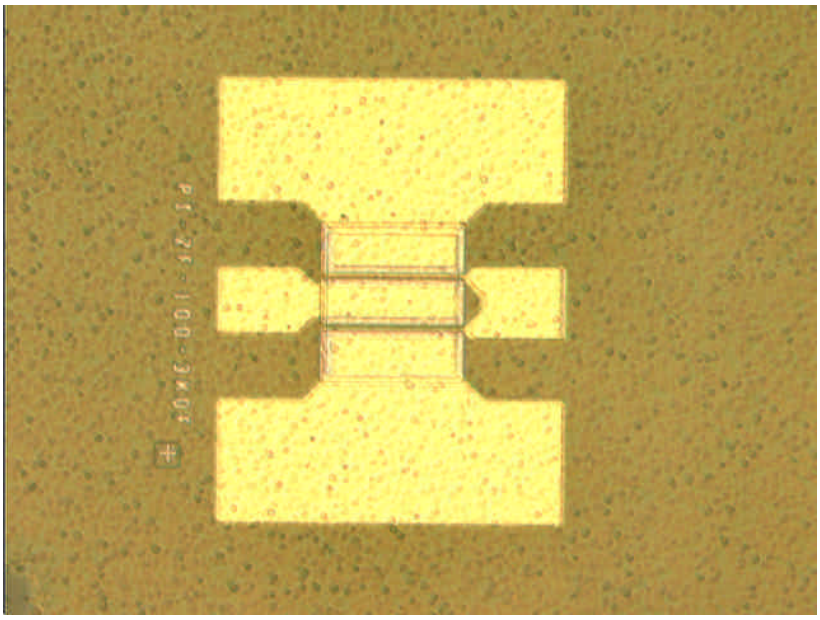
$$V_{th} = f_{ms} - \frac{Q_i}{C_i} + 2f_F + \frac{\sqrt{2e_{si}qN_a}}{C_{ox}}\sqrt{f_F + V_{CB}} \tag{5.7}$$

The spontaneous polarization charge of GaN is -0.029 C/m^2 or -2.9×10^{-6} C/cm^2. For Ga polar and nitrogen terminated GaN surface, without interfacial states, this spontaneous polarization charge correspond to a threshold voltage of -56 volts. However with the Si_3N_4 as gate dielectric, the majority of the polarization charge are neutralized by some positive interfacial charges and the net interfacial charge density is only -3.5×10^{-6} C/cm^2. The physical mechanism of the interfacial states might be that the Si_3N_4 passivates the GaN surface which reduces the un-bonded nitrogen atoms on the GaN surface, and the negative surface charges are therefore more or less neutralized by the decreased number of dangling nitrogen bond.

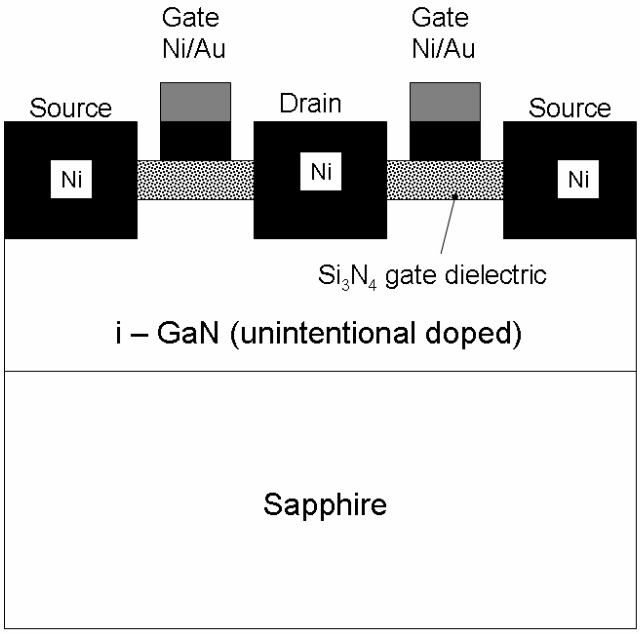
5.5 Two Gate Finger GaN SB-MISFET DC/RF Characteristics

5.5.1 DC Characteristics

On the same wafer, the two finger MISFET device with gate length of 0.7μm and gate width of 100μm has been characterized and the device picture and device cross-section diagram are shown in Fig. 5.5(a) and (b). The DC electrical performance of the device is characterized by Parameter analyzer HP4155b.



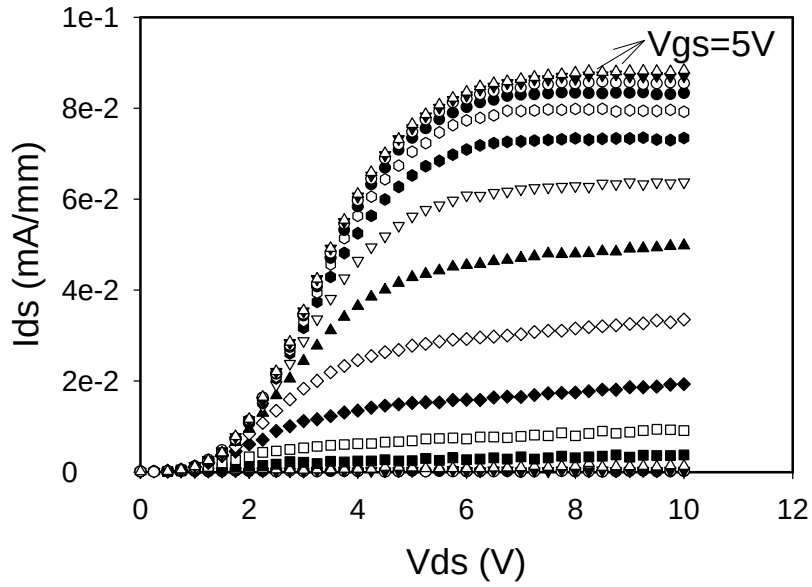
(a) Two gate finger GaN SB-MISFET picture



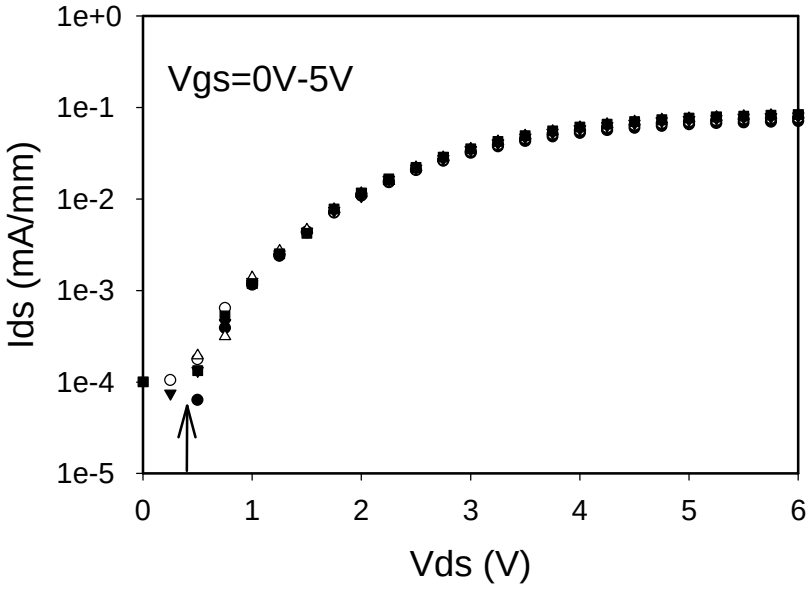
(b) Two gate finger GaN SB-MISFET cross-section

Figure 5.5: Two gate finger GaN SB-MISFET for DC and RF characterization.

The device output characteristics Ids-Vds are shown in Fig. 5.6 (a) and (b). The device has a very good pinch off performance and the achieved maximum drain current normalized to device width is 88.4μm/mm at gate bias of 5 volts. The graduate increase of the drain current at low drain bias indicates the existence of the Schottky barrier between the Ni drain/source and the unintentionally doped GaN channel. From Fig. 5.6(b), the calculated Schottky barrier height from this measurement is about 0.5eV which agrees with the published Ni/n-GaN Schottky barrier height data [22].



(a) Output Characteristics



(b) Semi-log scale of Output Characteristics

Figure 5.6: Output characteristics of two gate finger GaN SB-MISFET with gate dimension of $2\times100\mu m \times 0.7\mu m$.

The device transfer characteristics Ids-Vgs is shown in Fig. 5.7 and Fig. 5.8. The threshold voltage of the device is -7 Volts and the maximum transconductance is 0.0187mS/mm at Vds=10V. The I_{on}/I_{off} ratio of the device is around 1000. More importantly the gate leakage current is much less for the SB-MISFET than the Schottky gate leakage in MESFET devices shown in last chapter. The gate leakage current for the SB-MISFET was measured to be around 4×10^{-12} A for all the gate and drain biases. As shown in last chapter the gate leakage current easily increase to 3×10^{-5} A as the gate Schottky junction is turned on. For low power applications, the MOSFET and MISFET have their advantages over MESFET in that the MOSFET with the gate dielectric material inserted between the gate metal and the semiconductor channel. Therefore much less gate leakage and higher gate swing are expected.

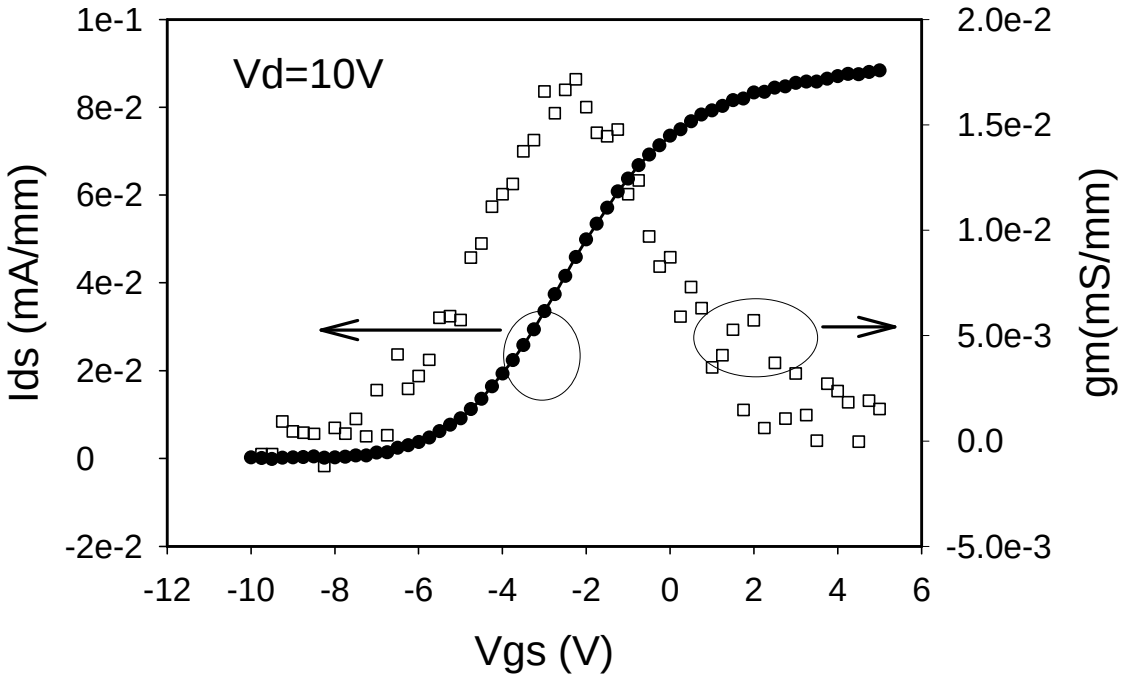


Figure 5.7: Transfer Characteristics Ids-Vgs and transconductance-Vgs at Vds= 10V.

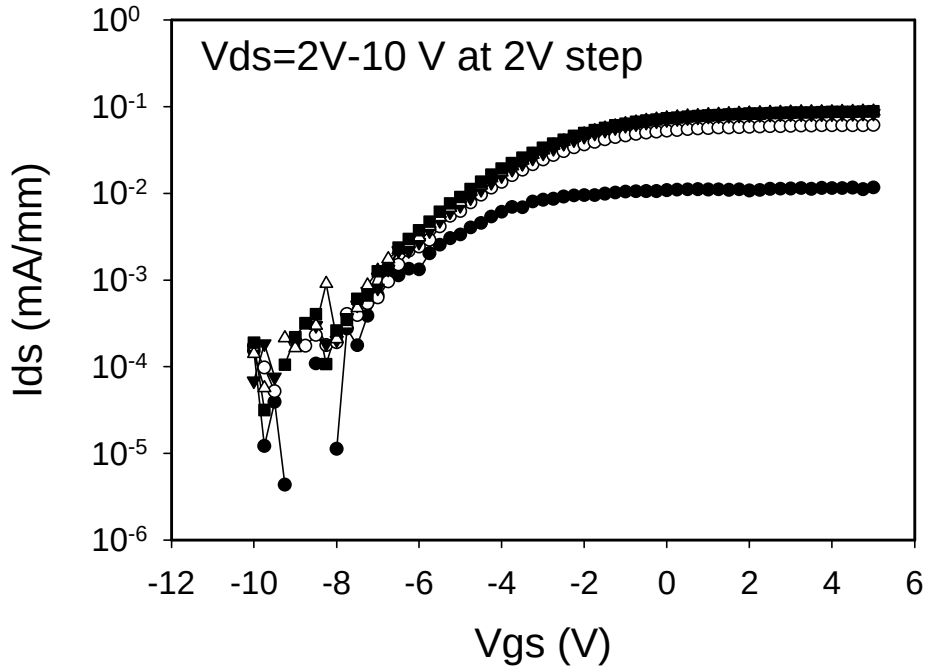
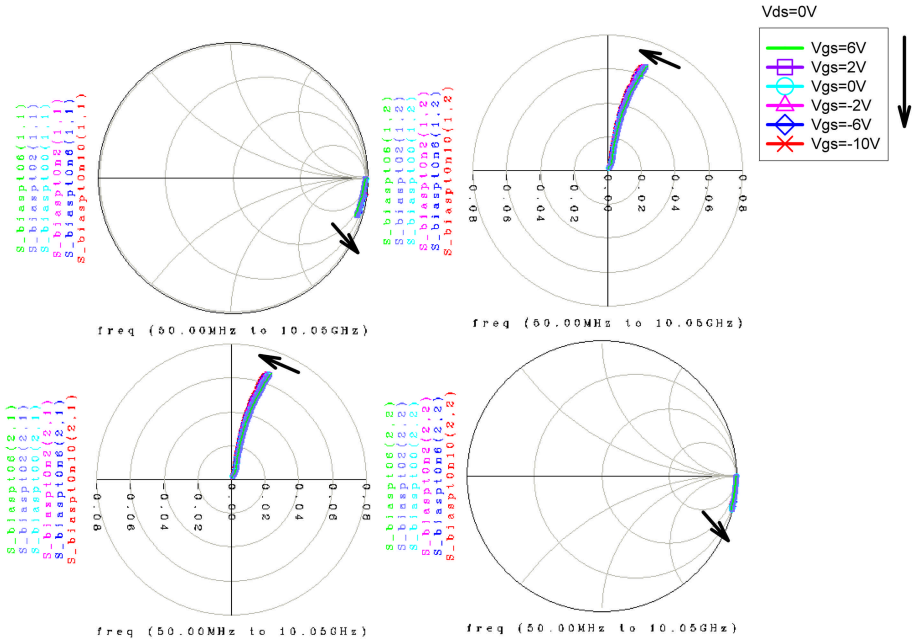


Figure 5.8: Transfer Characteristics Ids-Vgs in logarithmic scale. The drain bias Vds is from 2V to 10V at step of 2V.

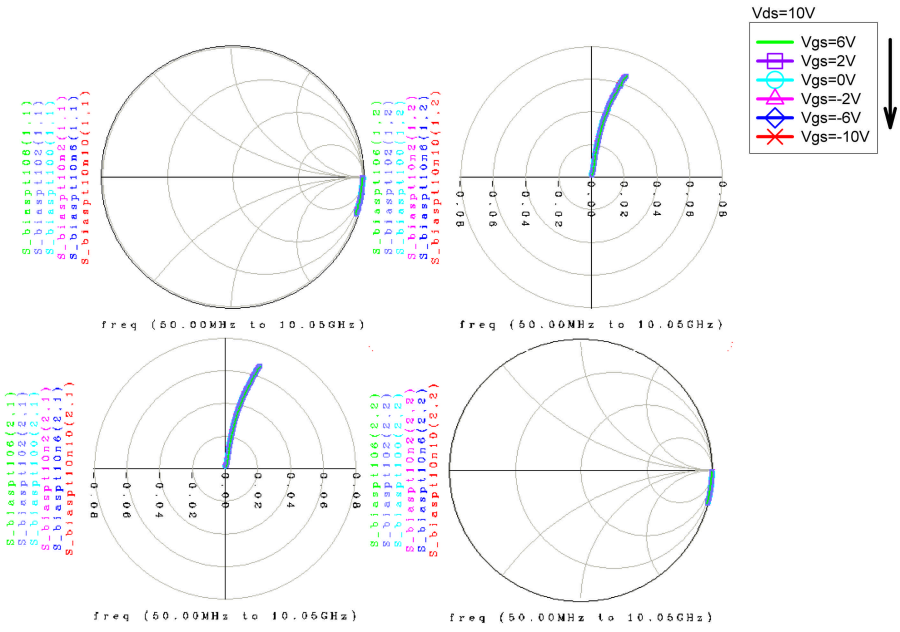
5.5.2 S Parameters Characteristics and Small Signal Model

The RF electrical performance of the device is characterized by Network analyzer HP8105b. The GSG (ground signal ground) probes are used for the calibration and device characterizations. Short Open Load Thru (SOLT) calibration standards provided with the GSG probes are used to calibrate the system before measurement. The HP4142b is used to DC bias the device. The S parameters measurements are from 50MHz up to 10GHz. The gate bias is from -10 V to 6V at step of 2V, the drain bias is from 0V to 10V at step of 2V. The S parameter results are shown in Fig. 5.9(a) and Fig. 5.9(b) for the two drain bias conditions, V_{ds}=0V, and V_{ds}=10V. Comparing the S parameters for this GaN SB-MISFET and published GaN HEMT, the less variation at different bias conditions indicates very little influence by

channel on and off condition. The very low carrier density and high depletion junction capacitance between the source/drain to the channel play a major role in S22.



(a) V_{ds}=0V



(b) V_{ds}=10V

Figure 5.9: Extrinsic Scattering Parameters from 50MHz to 10GHz and gate bias from -10V to 6V at step of 2V and drain bias at (a) 0V and (b) 10V.

In Fig. 5.10, the schematic diagram of the parasitic elements for the GaN MISFET is shown with the small signal depletion diode model between the source/drain to the channel. This extra feature of the SB-MISFET introduces a big depletion metal-semiconductor depletion capacitance which blocks the DC current. Therefore from the S22 measurements, the device looks like an open circuit.

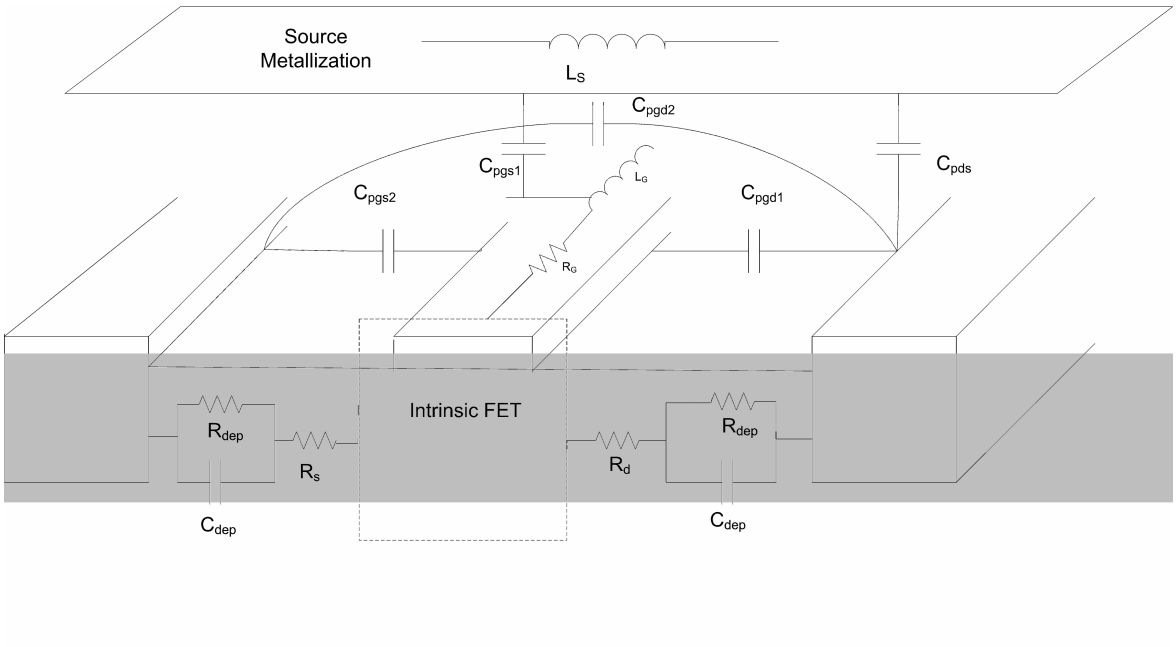


Figure 5.10: Schematic diagram of the parasitic elements for SB-MISFET.

The equivalent circuit model for the Schottky barrier source/drain MISFET is shown in figure 5.11. The MISFET small signal model has additional gate insulation capacitance C_i in series with the gate depletion capacitance comparing with the MESFET equivalent circuit model shown in last chapter. And the extrinsic elements such as the RF pad inductance and RF pad capacitance can be extracted similarly as shown in last chapter.

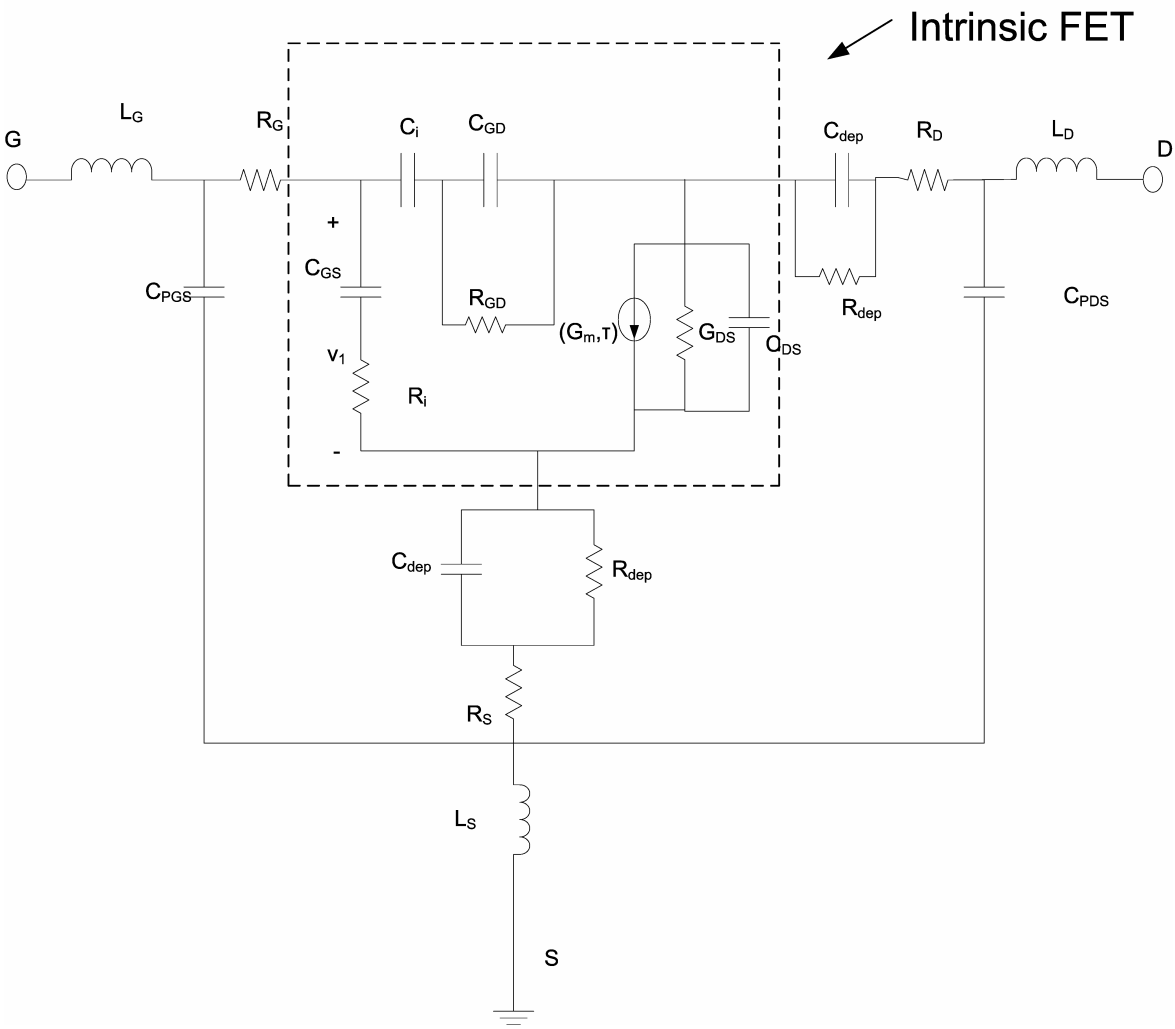


Figure 5.11: Small signal model of the SB-MISFET.

5.5.3 ColdFET Extraction

The reverse coldFET S parameters at gate biased of -10V are used to extract the RF pad capacitances for a $2 \times 100\ \mu m \times 0.7\ \mu m$ GaN Schottky barrier MISFET. The results are shown in figure 5.12. And the extracted low frequency C_{PGS} is 31.45 fF and C_{PDS} is 29.28 fF.

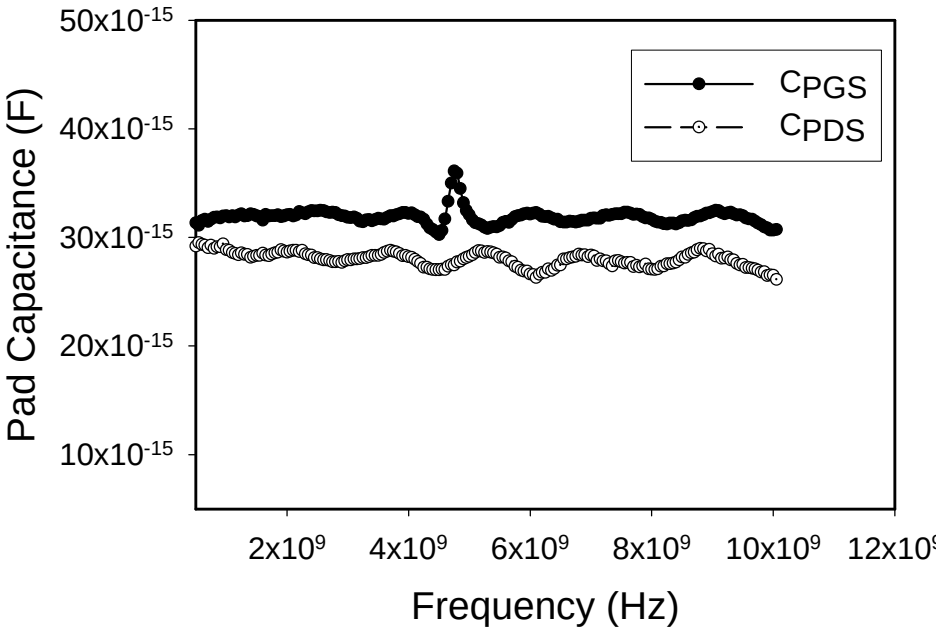


Figure 5.12: The extracted RF pad capacitances

The forward coldFET S parameters at gate biased of 6V are used to extract the series resistance and series inductance. The extracted results are shown in figure 5.13 and figure 5.14 for series resistances and series inductances, respectively. As shown in figure 5.13, at high frequency the source series resistance R_S is 4.12 Ohm, the drain series resistance R_D is 3.85 Ohm, and the gate series resistance R_G is 43.62 Ohm. In figure 5.14, at high frequency the source series inductance L_S is -2.3 nH, the drain series inductance L_D is -7.8 nH, and the gate series inductance L_G is -6.3 nH. Similar as the GaN MESFET demonstrated in last chapter, the Schottky barrier MISFET also shows the negative series inductance values and indicates that the Schottky diodes on the source and drain sides are formed from nickel-GaN. And the diode depletion capacitance is dominant in the imaginary part of the Z parameters of the device in the characterization frequency.

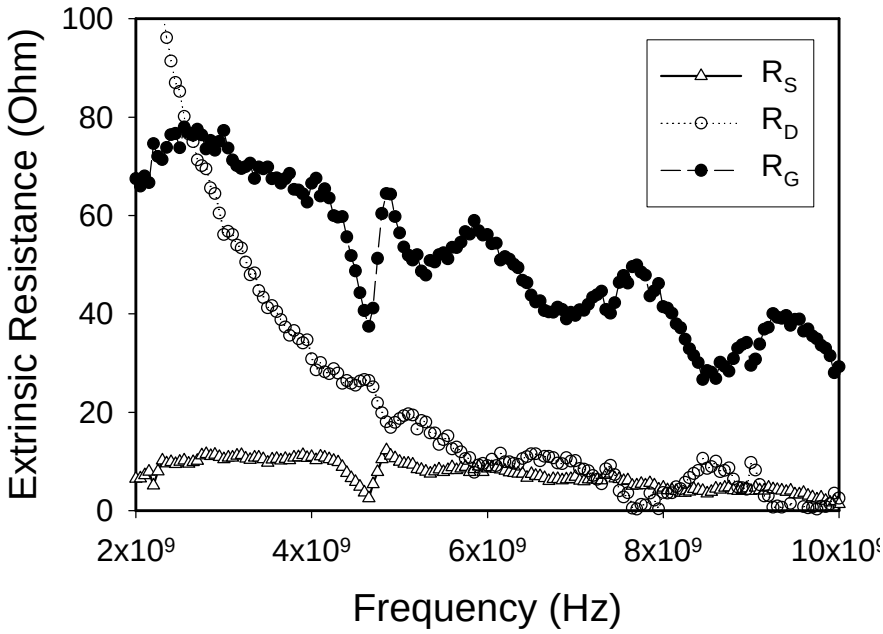


Figure 5.13: The extracted series resistances

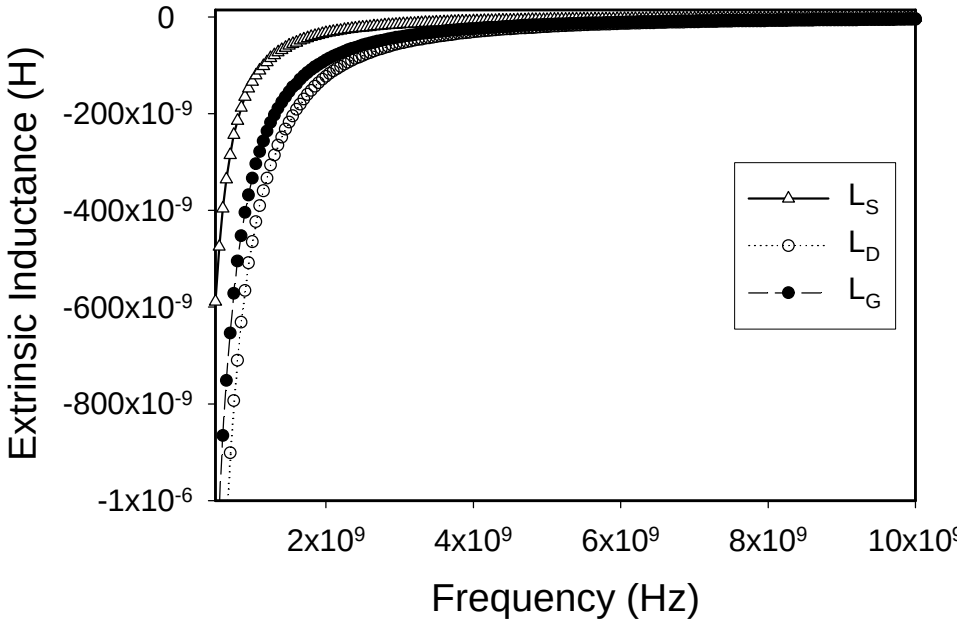


Figure 5.14: The extracted series inductances

5.5.4 Intrinsic Device parameter Extraction

Similar as the GaN MESFET, with the additional Schottky diode small signal model, the intrinsic device parameters can be extracted using de-embedding. The finally extraction results are shown in the following figures. Fig. 5.15, Fig. 5.16 and Fig. 5.17 shows the extracted Cgd, Cgs and Cgg for different gate bias conditions at high frequency (1.5GHz).

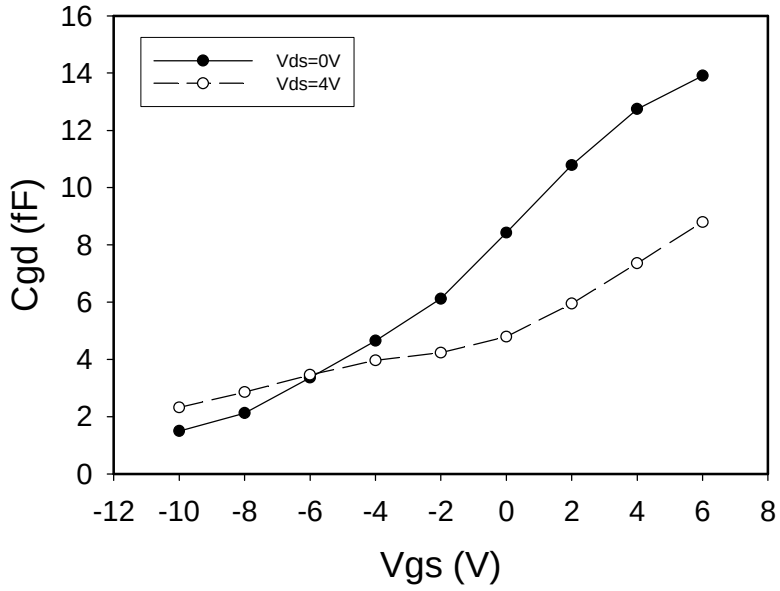


Figure 5.15: Extracted gate capacitance Cgd at 1.5GHz.

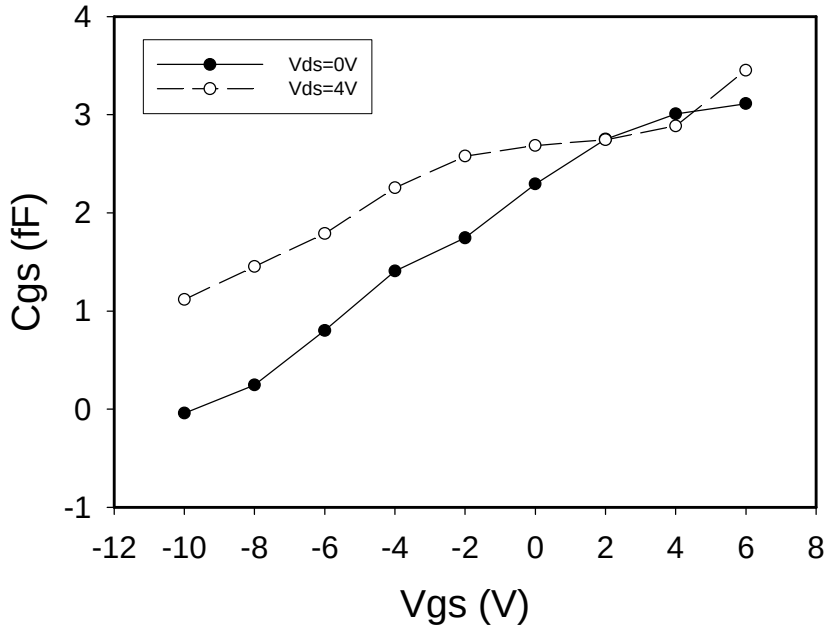


Figure 5.16: Extracted gate capacitance Cgs at 1.5GHz

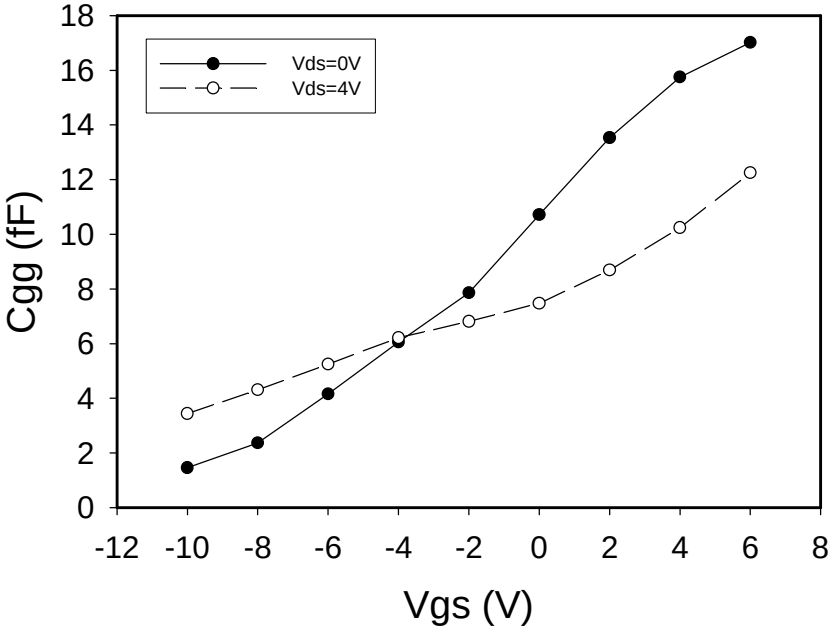
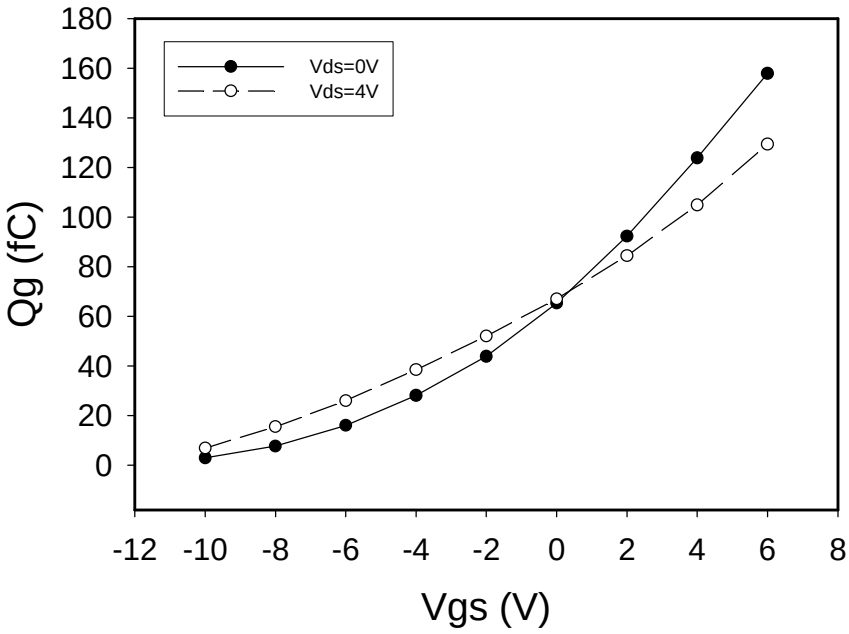


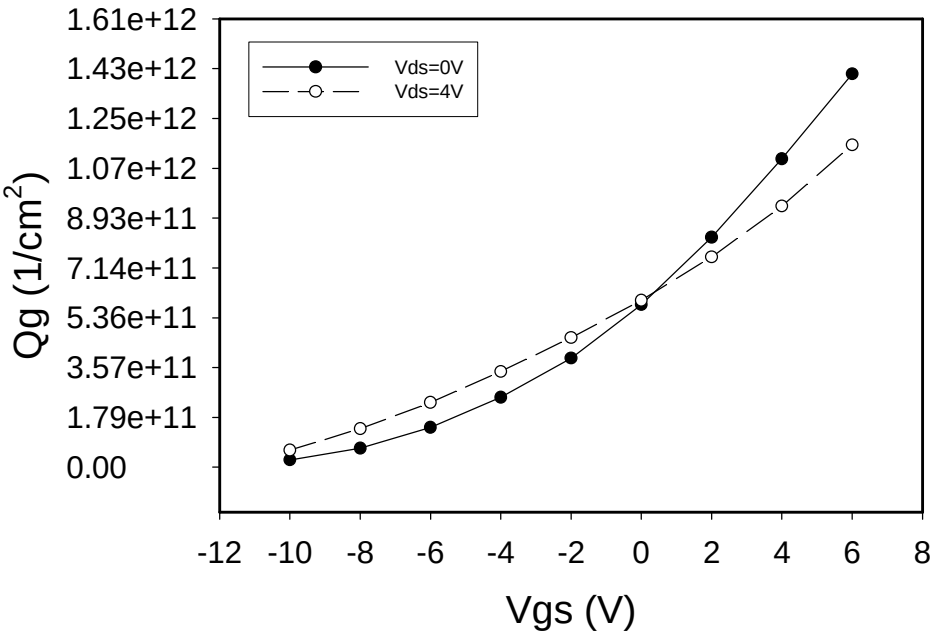
Figure 5.17: Extracted gate capacitance Cgg at 1.5GHz

The extracted gate capacitance shows the trend of gate bias dependence. The gate capacitances increase confirms that the device transition from depletion to accumulation while the gate bias increases. At more negative bias conditions, the channel is fully depleted therefore the gate capacitances reach to minimum which is the insulator capacitance in series with the depletion capacitance. At more positive bias conditions the gate channel is turned on, therefore the gate capacitances reach to maximum which is the insulator capacitance only. The gate capacitance extraction is in Giga hertz range from 1 GHz up to 10GHz, and the figure shows 1.5GHz capacitances only. The extracted gate capacitances agree with high frequency C-V measurement in general depletion model MOSFET and MISFET.

The sheet charge controlled by gate capacitor can also be extracted in the same way as described in chapter 4 of this dissertation. Fig. 5.18 shows extracted sheet charge for the 100μm×0.7μm GaN SB-MISFET. We notice that after converting the sheet charge to the unit of $1/cm^2$, the device sheet charge is in the order of 0 to $1.42 \times 10^{12}\,cm^{-2}$. This number is not very high comparing to the sheet charge density $1 \times 10^{13}\,cm^{-2}$ of 2DEG in GaN HEMT but it is higher than the sheet charge in the GaN MEFET introduced in last chapter. This explains the low current and low transconductance of our device and a little bit better performance than that of the GaN MESFET. To improve the device performance to the competitive level as that of the GaN HEMT, the sheet charge has to be increased at least one order of magnitude.



(a) Sheet charge integrated from Cgg.



(b) Sheet charge integrated from Cgg, normalized with gate area

Figure 5.18: Extracted sheet charge Qg at 1.5GHz

The output conductance is also extracted to calculate low field mobility using the same way as MESFET extraction described in last chapter. The extracted output conductance is shown in Fig. 5.19 and the calculated low field mobility is shown in Fig. 5.20. The low field mobility can reach as high as 40 cm^2/Vs indicating the promising of this GaN MOVPE growth technique. However the device design trade off exits in that we need higher doping concentration for channel material in depletion mode GaN MOSFET/MISFET, but with higher doped channel, the mobility will decrease due to the enhanced ionized donor scattering. For enhancement mode GaN MOSFET, lightly doped or intrinsic channel might be desired to reduce short channel effect. And better quality of the insulator materials for enhancement mode III-V MOSFET device have been demonstrated on GaAs and GaN using SiO_2, MgO, Ga_2O_3-Gd_2O_3, or other novel oxide materials.

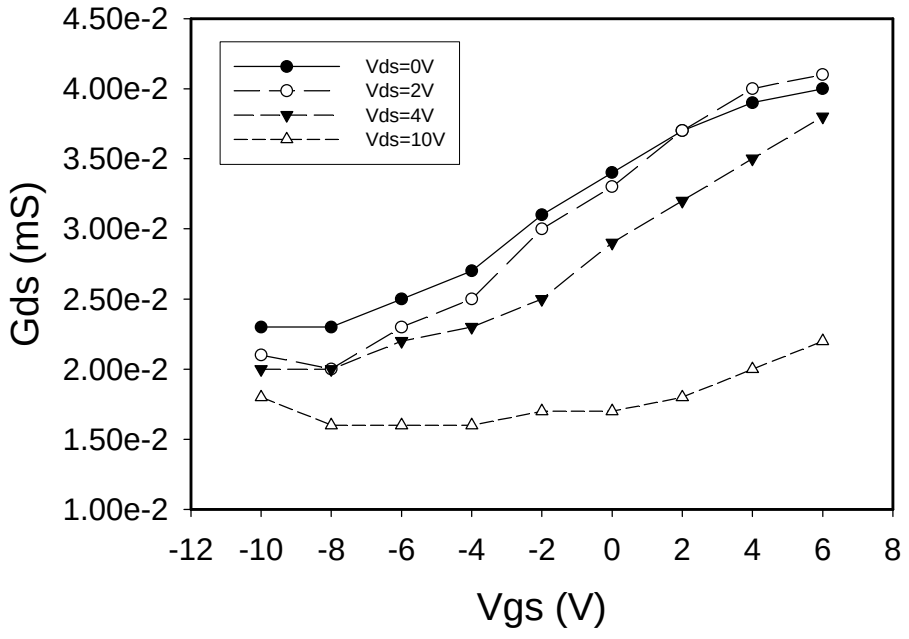


Figure 5.19: Extracted output conductance at 1.5GHz

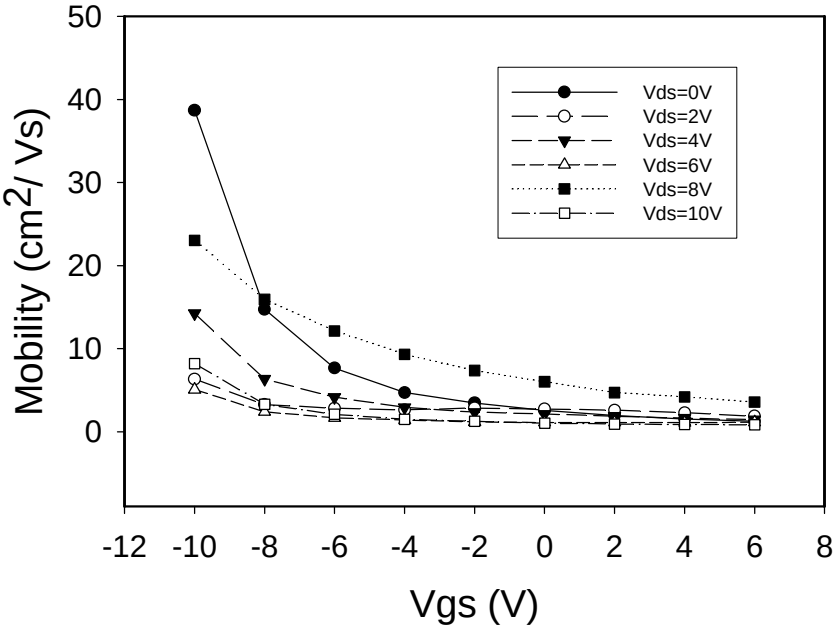


Figure 5.20: Calculated mobility vs. gate bias

5.5 Summary

In this chapter, the gate dielectric and Schottky metal as source/drain have been introduced for the Schottky barrier GaN MISFET devices. Depletion mode GaN SB-MISFET on unintentional doped GaN film grown on sapphire by MOCVD is successfully fabricated and demonstrated for the first time. The detailed device characteristics in DC and RF are studied in this work. For the FatFET with a gate length of 50μm and a gate width of 100μm, the highest drain current normalized to device gate width achieved is 0.4μA/mm at both gate and drain bias of 10V, and the peak transconductance achieved is 0.05μS/mm. The GaN Schottky barrier MISFETs have a low pinch off current 5pA with a pinch off voltage of -7V which agrees well with the theoretical calculation of the GaN doping profile and this N-face

GaN surface charge reduction due to Si_3N_4 passivation effect. For the two gate finger GaN Schottky barrier MISFET with a gate length of 0.7μm and a gate width of 100μm, the highest drain current achieved is 0.0884mA/mm at gate bias of 5 V, and the peak transconductance achieved is 0.0187mS/mm. The I_{on}/I_{off} ratio of this device reaches 3 orders of magnitude. And the pinch off voltage is around -7V. Furthermore the high frequency S parameter measurements on this device are conducted from 50MHz up to 10GHz. We find out similar to the MESFET introduced in last chapter, the Schottky contacts are having a large effect on the S parameters of the Schottky barrier MISFET device. The Schottky diode in the drain and source sides have to be considered in the device intrinsic parameter extraction. The device small signal model is studied and the extrinsic parasitic elements are extracted using ColdFET technique. The intrinsic device model is obtained after de-embedding. Several key device parameters such as gate capacitance, sheet charge density, output conductance and effective channel mobility are calculated from intrinsic Y parameters of the device at 1.5GHz. The sheet carrier concentration reaches up to around $1.42\times10^{12}cm^{-2}$, and the low field mobility reaches up to 40 cm^2/Vs. All these values achieved falls in range of the reasonable value of GaN MOSFET and MISFET and they are a little bit better than the GaN MESFET introduced in last chapter. However they are still much lower than their GaN HEMT counterparts.

With higher doping concentration in GaN channel, and high k dielectric material such as Ga_2O_3-Gd_2O_3, we expect to see great improvement of the device performance. The Schottky-barrier concept has been proved to be an effective method to achieve carrier rich source/drain for GaN based MOSFET and MISFET for power and digital applications.

Furthermore we demonstrated the first time for small dimension GaN SB-MOSFET, Scattering parameter measurements can be used to extract the gate capacitance.

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Chapter 6

Conclusions and Future Research Directions

6.1 Conclusions

This dissertation summarizes the results of my PhD research work on GaN heterogeneous source drain MOSFET.

The GaN electronics device research history was briefly introduced first, along with the state of the art GaN based field effect transistors including MESFET, HEMT, MOSHFET, and MOSFET. The several key motivations of GaN MOSFET research especially GaN Schottky Barrier MOSFET are listed as the following:

1) To address the RF dispersion problem, and real space charge transfer problem facing GaN HEMT.
2) To reduce gate leakage current therefore increase the gate swing and decrease the device power consumption.
3) To simplify the manufacturing process for GaN SB-CMOS and make it compatible with existing GaN MESFET and HEMT processes. And to search for alternative method excluding ion implantation to achieve carrier rich source/drain.

The studied GaN SB-MOSFET devices are potential candidate for future digital applications and possible candidate for future high power high frequency applications. The combination of GaN channel material and heterogeneous source drain material is the key for novel device design with improved device performance.

To understand better GaN MOSFET design and its potential applications, first the GaN theoretical studies were conducted. The basic semiconductor device physics and some relevant device physics for Wurtzite GaN were studied. And several different III-V compound semiconductor materials such as InSb, and GaN based devices has been studied and modeled using ISE-TCAD. The theoretical study shows the promising properties of aggressively scaled GaN based MOSFETs.

The processing techniques for GaN MOSFET source/drain were studied with emphasis on low temperature techniques such as regrown source/drain, and Schottky metal source/drain. The Schottky metal source/drain patterning was investigated using two different processes such as wet chemical etch and lift off. Finally the lift off process was selected for the device processing due to its better control of the metal source/drain patterning. The metal-GaN Schottky barrier contact was reviewed and the several suitable low barrier metals such as Al, Ni, Ti, and Cr were identified for GaN SB-MOSFET device. The GaN n-i-n structure has been fabricated and studied which serves as both a calibration of GaN heterogeneous source drain MOSFET device model, and a testing structure in our current processing flow. The GaN wet etch is very important for future generation GaN device process improvement. Therefore the GaN wet etch techniques were reviewed and binary wet etch was designed for an experiment, the detailed experimental results show the etch rate and surface roughness control.

The GaN MOSFET device processing flow was carefully designed which is compatible with GaN MESFET and HEMT device processing flow. Using the designed process flow, GaN MESFET and GaN Schottky barrier MISFET were fabricated.

The GaN MESFET on pulse doped GaN film has been demonstrated, two devices with different gate length were characterized using DC, and high frequency S parameter measurements. For the FatFET with a gate length of 50μm and a gate width of 100μm, the highest drain current normalized to device gate width achieved is 0.08mA/mm at gate bias of 0.75V, and the peak transconductance achieved is 0.134mS/mm. The I_{on}/I_{off} ratio of this device reaches 5 orders of magnitude. The MESFETs have a low pinch off current with a pinch off voltage of -0.75V which agrees well with the theoretical calculation of the GaN doping profile. For the RFFET with a gate length of 0.7μm and a gate width of 100μm, the highest drain current achieved is 0.067mA/mm at gate bias of 0.75 V, and the peak transconductance achieved is 0.0418mS/mm. The I_{on}/I_{off} ratio of this device reaches 2 orders of magnitude. And the pinch off voltage is around -0.75V. Furthermore the high frequency S parameter measurements on this device were conducted from 45MHz up to 10GHz. Several key device parameters such as gate capacitance, sheet charge density, output conductance and effective channel mobility were extracted from the device S parameters at 1.5GHz. The sheet carrier concentration reaches up to around $7\times10^{11}cm^{-2}$, and the low field mobility reaches up to 40 cm^2/Vs. All these values achieved falls in range of the reasonable value of GaN MOSFET and MISFET which proves that this pulse doped channel concept in GaN material growth is very promising for current and future GaN electronic device research and development. However the performance of the GaN MESFET above V_{GS}=0.75V is limited mainly by the large Schottky gate leakage current.

To overcome the Schottky gate leakage limitation of the GaN MESFET and HEMT, GaN MOSFET with Schottky barrier source drain has been investigated in this work. GaN Schottky barrier source drain MOSFET operational mechanism was studied with the band gap diagrams. A depletion mode GaN Schottky barrier MISFET was successfully designed and fabricated on MOCVD grown GaN film on Sapphire for the first time to our best knowledge. For the FatFET with a gate length of 50μm and a gate width of 100μm, the highest drain current normalized to device gate width achieved is 0.4μA/mm at both gate and drain bias of 10V, and the peak transconductance achieved is 0.05μS/mm. The GaN SB-MISFETs have a low pinch off current with a pinch off voltage of -7V which agrees well with the theoretical calculation of the GaN doping profile and this N-face GaN surface charge reduction due to Si_3N_4 passivation effect. For the two gate finfer RFFET with a gate length of 0.7μm and a gate width of 100μm, the highest drain current achieved is 0.0884mA/mm at gate bias of 5 V, and the peak transconductance achieved is 0.0187mS/mm. The I_{on}/I_{off} ratio of this device reaches 3 orders of magnitude. And the pinch off voltage is around -7V. Furthermore the high frequency S parameter measurements on this device are conducted from 50MHz up to 10GHz. The Schottky diode in the drain and source sides have to be considered in the device intrinsic parameter extraction. Several key device parameters such as gate capacitance, sheet charge density, output conductance and effective channel mobility are extracted from the device S parameters at 1.5GHz. The sheet carrier concentration reaches up to around $1.42\times10^{12}cm^{-2}$, and the low field mobility reaches up to 40 cm^2/Vs. All these values achieved falls in range of the reasonable value of GaN MOSFET and MISFET and they are a little bit better than the GaN MESFET.

Table 6.1 summarizes the performance of the GaN MESFET and the GaN Schottky barrier MISFET. The scaling advantage of the MISFET is confirmed by both the improving driving current I_{sat} and I_{on}/I_{off} ratio while device scale to smaller gate length. The MISFET has much less gate leakage current comparing with MESFET. And the sheet charge density also favors the MISFET.

TABLE 6.1: Summarize the performance of the GaN MESFET and GaN SB-MISFET

Performance	**MESFET 100㎜/50㎜**	**MESFET 100㎜/0.7㎜**	**SB-MISFET 100㎜/50㎜**	**SB-MISFET 100㎜/0.7㎜**
I_{sat}	**148mA/mm**	**80mA/mm**	**0.379mA/mm**	**88.4mA/mm**
G_m	**134mS/mm**	**41.8mS/mm**	**0.05mS/mm**	**18.7mS/mm**
I_{on}/I_{off}	**10^5**	**10^2**	**10^2**	**10^3**
I_g	**10^{-5} A at Vgs=1V**	**10^{-6} A at Vgs=1V**	**<$4x10^{-12}$ A**	**<$2x10^{-7}$ A**
Q_{sh}	**N/A**	**$5x10^{11}$ cm^{-2}**	**NA**	**$1.5x10^{12}$ cm^{-2}**
㎛$_{ch}$	**NA**	**40cm^2/Vs**	**NA**	**40cm^2/Vs**

Overall, the GaN heterogeneous source drain MOSFET has the merging advantages of GaN as channel material and heterogeneous source drain structures to supply conducting carriers. This study demonstrates for the first time nickel is used as Schottky barrier metal in a depletion mode GaN MISFET device. The device is first of its kind in nature and successfully proves the device design concept of using metal as source/drain for GaN MOSFET and MISFET. With in house capability of depositing Si_3N_4 and SiO_2 as gate

dielectric using PECVD, I believe both depletion mode and enhancement mode of GaN SB-MOSFET and SB-MISFET can be fabricated.

The Schottky-barrier concept is an effective method to achieve carrier rich source/drain for GaN based MOSFET and MISFET. This novel source/drain engineering on GaN FET design exluding high temperature processes such as ion implantation and thermal diffusion is one of its most important advantages. With low Schottky-barrier height realized with metal on GaN, the device performance can be improved dramatically. Moreover, this idea can be used on GaN HEMT as well to reduce the contact resistances and improve the device power performance. As semiconductor technology moves forward, the GaN electronics have great future not only in high frequency applications such as satellite, radar and wireless communication, but also in power electronics such as electrical sub-systems of emerging vehice, ship and aircraft technology. With improving device design and engineering, the GaN Schottky barrier MOSFET will provide competitive device performance in GaN electronics device family and occupy an important position.

6.2 Future Research Directions

There are several areas of future research can be done based on the concept of heterogeneous source/drain. First of all, the substrate material optimization can be done on various GaN films such as MBE grown GaN film on Sapphire and MOCVD grown GaN film on Sapphire, GaN film on SiC and Si might also be some of the options and trends for integration of GaN SB-MOSFET on Si Integrated Circuit. Second, the substrate doping type

and doping concentration could be optimized for certain device, eg. for depletion mode NMOS, the substrate doping concentration should be higher than 1×10^{18} cm^{-3} to achieve higher saturation current and transconductance. For enhancement mode NMOS however p type GaN substrate is necessary. Third, the gate dielectric material can be optimized. The Si_3N_4 has been used throughout this research. However, enhancement mode GaN MOSFETs have only been demonstrated with SiO_2 and Ga_2O_3-Gd_2O_3 et al as gate dielectrics. GaN MISFETs with only Si_3N_4 as gate dielectric are all depletion mode. Fourth, the Schottky metal for source/drain can be optimized based on the metal-GaN Schottky barrier height. Aluminum (Al) might be one of the metal giving lowest Schottky barrier height with n type GaN. Last but not least, the idea of Schottky barrier metal as source/drain could be extended to other materials such as highly doped poly-Si, highly doped amorphous Si, and various metal silicides to be used as source/drain material for GaN MOSFET application. The heterogeneous source/drain concept can also be further applied to GaN HEMT structure to reduce the series resistance and improve power handling capability of GaN HEMT.

Appendices

Appendix A

GaN MESFETs Fabrication Process Flow

PowerFET Mask Series

Step#	Process step
1	HCl, Acetone, Methanol cleaning
2	Photoresist coat: AZ5214, soft bake at 90°C 2 min
3	Mask level 1- Mesa, expose 8sec, develop 30sec
4	Cr/Ni (10nm/150nm) deposition via E-beam, metal lift off
5	GaN RIE in BCl_3 ambient, mesa formed, strip Cr/Ni
6	Photoresist coat: AZ5214, soft bake at 90°C 2 min
7	Mask level 2- Ohmic, expose 0.8sec, hard bake at 115°C 1.5min
8	Flood exposure 90sec, develop 30sec
9	Ohmic metal Ti/Al/Ni/Au deposition via E-beam, metal lift off
10	Photoresist coat: AZ5214, soft bake at 90°C 2 min
11	Mask level 3- Gate, expose 0.8sec, hard bake at 115°C 1.5min
12	Flood exposure 90sec, develop 30sec
13	Gate metal deposition via E-beam, metal lift off
14	Photoresist coat: AZ5214, soft bake at 90°C 2 min
15	Mask level 4- Internconnect, expose 0.8sec, hard bake at 115°C 1.5min
16	Flood exposure 90sec, develop 30sec
17	Interconnect metal deposition via E-beam, metal lift off

Appendix B

GaN Schottky Barrier MISFETs Fabrication Process Flow

PowerFET Mask Series

Step#	Process step
1	HCl, Acetone, Methanol cleaning
2	Gate dielectric deposition via PECVD
3	Photoresist coat: AZ5214, soft bake at 90°C 2 min
4	Mask level 1- Mesa, expose 8sec, develop 30sec
5	Cr/Ni (10nm/150nm) deposition via E-beam, metal lift off
6	GaN RIE in BCl_3 ambient, mesa formed, strip Cr/Ni
7	Photoresist coat: AZ5214, soft bake at 90°C 2 min
8	Mask level 2- Ohmic, expose 8sec, develop 30sec
9	Cr/Ni (10nm/150nm) deposition via E-beam, metal lift off
10	Gate dielectric RIE via PECVD
11	GaN RIE in BCl_3 ambient, source/drain patterned, strip Cr/Ni
12	Photoresist coat: AZ5214, soft bake at 90°C 2 min
13	Mask level 3- reuse Ohmic, expose 0.8sec, hard bake at 115°C 1.5min
14	Flood exposure 90sec, develop 50sec
15	Source/Drain Schottky metal deposition via E-beam, metal lift off
16	Photoresist coat: AZ5214, soft bake at 90°C 2 min
17	Mask level 4- Gate, expose 0.8sec, hard bake at 115°C 1.5min
18	Flood exposure 90sec, develop 30sec
19	Gate metal deposition via E-beam, metal lift off
20	Photoresist coat: AZ5214, soft bake at 90°C 2 min

21	Mask level 5- Internconnect, expose 0.8sec, hard bake at 115°C 1.5min
22	Flood exposure 90sec, develop 30sec
23	Interconnect metal deposition via E-beam, metal lift off

Appendix C

FET Extrinsic De-embedding Procedure

Step#	Process step
1	Measure S parameters, this is extrinsic S parameters
2	Convert S parameters to Z parameters
3	Z parameters subtract series inductances
4	Convert to Y parameters
5	Y parameters subtract pad capacitances
6	Convert to Z parameters
7	Z parameters Subtract series resistances, get intrinsic Z parameters
8	Intrinsic Z parameters convert to intrinsic Y parameters