ABSTRACT

GOWDA, SRIVARDHAN S. Investigation of Multi-state Charge-Storage Properties of Redox-Active Organic Molecules in Silicon-Molecular Hybrid Devices for DRAM and Flash Applications. (Under the direction of Prof. Veena Misra.)

Molecular electronics has recently spawned a considerable amount of interest with several molecules possessing charge-conduction and charge-storage properties proposed for use in electronic devices. Hybrid silicon-molecular technology has the promise of augmenting the current silicon technology and provide for a transitional path to future molecule-only technology. The focus of this dissertation work has been on developing a class of hybrid silicon-molecular electronic devices for DRAM and Flash memory applications utilizing redox-active molecules. This work exploits the ability of molecules to store charges with single-electron precision at room temperature.

The hybrid devices are fabricated by forming self-assembled monolayers of redox-active molecules on Si and oxide (SiO_2 and HfO_2) surfaces via formation of covalent linkages. The molecules possess discrete quantum states from which electrons can tunnel to the Si substrate at discrete applied voltages (oxidation process, cell write), leaving behind a positively charged layer of molecules. The reduction (erase) process, which is the process of electrons tunneling back from Si to the molecules, neutralizes the positively charged molecular monolayer.

Hybrid silicon-molecular capacitor test structures were electrically characterized with an electrolyte gate using cyclic voltammetry (CyV) and impedance spectroscopy (CV) techniques. The redox voltages, kinetics (write/erase speeds) and charge-retention characteristics were found to be strongly dependent on the Si doping type and densities, and ambient light. It was also determined that the redox energy states in the molecules communicate with the valence band of the Si substrate. This allows tuning of write and read states by modulating minority carriers in n- and p-Si substrates. Ultra-thin dielectric tunnel barriers (SiO_2, HfO_2) were placed between the molecules and the Si substrate to augment charge-retention for Flash memory applications. The redox response was studied as a function of tunnel oxide thickness, dielectric permittivity and energy barrier, and modified Butler-Volmer expressions were postulated to describe the redox kinetics. The

speed vs. retention performance of the devices was improved via asymmetric layered tunnel barriers.

The properties of molecules can be tailored by molecular design and synthetic chemistry. In this work, it was demonstrated that an alternate route to tune/enhance the properties of the hybrid device is to engineer the substrate (silicon) component. The molecules were attached to diode surfaces to tune redox voltages and improve charge-retention characteristics. N+ pockets embedded in P-Si well were utilized to obtain multiple states from a two-state molecule. The structure was also employed as a characterization tool in investigating the intrinsic properties of the molecules such as lateral conductivity within the monolayer.

Redox molecules were also incorporated on an ultra thin gate-oxide of Si MOSFETs with the intent of studying the interaction of redox states with Si MOSFETs. The discrete molecular states were manifested in the drain current and threshold voltage characteristics of the device. This work demonstrates the multi-state modulation of Si-MOSFETs' drain current via redox-active molecular monolayers. Polymeric films of redox-active molecules were incorporated to improve the charge-density (ON/OFF ratio) and these structures may be employed for multi-state, low-voltage Flash memory applications.

The most critical aspect of this research effort is to build a reliable and high density solid state memory technology. To this end, efforts were directed towards replacement of the electrolytic gate, which forms an extremely thin insulating double layer (~10 nm) at the electrolyte-molecule interface, with a combination of an ultra-thin high-K dielectric layer and a metal gate. Several interesting observations were made in the research approaches towards integration and provided valuable insights into the electrolyte-redox systems.

In summary, this work provides fundamental insights into the interaction of redox-energy states with silicon substrate and realistic approaches for exploiting the unique properties of the molecules that may enable solutions for nanoscale high density, low-voltage, long retention and multiple bit memory applications.

INVESTIGATION OF MULTI-STATE CHARGE-STORAGE PROPERTIES OF REDOX-ACTIVE ORGANIC MOLECULES IN SILICON-MOLECULAR HYBRID DEVICES FOR DRAM AND FLASH APPLICATIONS

By

Srivardhan Shivappa Gowda

A dissertation submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

ELECTRICAL ENGINEERING

Raleigh, North Carolina
December, 2006

APPROVED BY:

_____

LEDA LUNARDI

_____

ERIC ROTENBERG

_____

JONATHAN S. LINDSEY

_____

VEENA MISRA
Chair of advisory committee

To

my advisor Prof. Misra,

my dear Mom, Dad, sister Roopa,

and

loving memory of my dearest Grandmom

BIOGRAPHY

Srivardhan S. Gowda was born to Dr. B. N. Susheelamma and Prof. C. T. Shivappa Gowda, on Wednesday, August 9th 1978, in Mysore, India. Sriv has an older sister, Roopashree D. Gowda, who was born in December, 1973. Sriv did his primary through senior secondary schooling in Demonstration School, Mysore, India during the years 1984-1996. In January 1997, he joined Sri Jayachamarajendra College of Engineering (SJCE), University of Mysore, Mysore for undergraduate studies in Instrumentation Technology. During his time in SJCE, he was actively involved in activities of SJCE IEEE student chapter, served as Vice-chairman of the student chapter for years 1999-2000, and instrumental in organizing CYBERIA 2000, an annual national-level technical fete of the chapter. He also won the first place in software contest in CYBERIA 1999. In August 2000, he received a Bachelor of Engineering degree with a classification of first class with distinction from University of Mysore. He worked for eight months at ADP Wilco Ltd., Sydney, Australia as Analyst Programmer before leaving to United States for pursuing graduate studies.

In August 2001, he joined Masters program in the Department of Electrical and Computer Engineering at North Carolina State University. After working for a year with Dr. Greg Byrd in area of network processor architectures, he joined the molecular electronics research group of Prof. Veena Misra in fall of 2002. He received his Master of Science degree in Computer Engineering in August, 2003 and continued work in field of hybrid silicon-molecular devices for PhD program under the guidance of Prof. Misra. His research work has led to more than 10 original publications and 1 issued US patent. He was the receipt of 2005 Texas Instruments Graduate Fellowship Award for Leadership in Nanoelectronics and Best Student Poster Award at IMAPS Carolinas chapter's 2006 Scientific Symposium on Microelectronics. He will be completing PhD dissertation research in December 2006 and upon successful completion moving to Boise, ID to work for Intel NAND Flash group as Device Engineer.

ACKNOWLEDGEMENTS

This work is culmination of my graduate research studies at NCSU, and involved support from various individuals. I take immense pleasure in thanking all the hands and minds that played a part in giving this dissertation its final shape.

First and foremost, I express my heartfelt gratitude to my advisor Prof. Veena Misra, for giving me a wonderful opportunity to work in the area of molecular electronics and guiding me to successfully complete my graduate studies. To me, she has been a great teacher, source of inspiration, and an unfailing mentor. She has always been approachable for discussions and her suggestions have been invaluable for the progress of my research work over last four years. Her guidance has helped me to mature as a researcher and for that I am deeply indebted for the rest of my career. I also thank my committee members – Prof. Jonathan Lindsey, Prof Leda Lunardi, and Dr. Eric Rotenberg for agreeing to be part of my committee and for discussions regarding my dissertation research.

I have received a lot of help and support from my group members – Dr. Guru Mathur, Dr. Qiliang Li, Dr. Shyam Surthi, Mais Homsi, Dr. Qian Zhao, Dr. Smita Sarkar, Zhong Chen, Hakan Efe, and Greg Mulholland. In particular, I thank Guru for introducing me to Prof. Misra and enabling the opportunity to work in the group. He also imparted training on several research tools I have used at NCSU. I always enjoyed our extensive technical discussions and collaborative research work, which led to several publications. He was also a great roommate during my graduate studies and has been a great friend. I thank Qiliang, Shyam and Mais for all the assistance and training they gave me during the initial stages of my graduate research work. I am grateful to Qiliang for imparting valuable technical skills and assisting me in experimental work. Shyam spent lengthy hours in the cleanroom developing the process flow for the MoleFET devices, which helped me meet one of the key goals of my dissertation work.

I also express my gratitude to our research collaborators: (i) Prof. Jonathan Lindsey and his group at Dept. of Chemistry, NCSU for providing us the molecules that formed the basis for my research work, (ii) Dr. Thomas Sorenson and Dr. Rob Tenant at Zettacore Inc.,

for providing samples and technical inputs, and (iii) Prof. David Bocian and his group at University of California, Riverside.

My special thanks to staff members at NCSU: Joan O'Sullivan for all her assistance in the research facilities, Kaye Bailey for handling all the paperwork, Brian Carty for keeping IT systems running smoothly, Harold Morton and Henry Taylor for troubleshooting with me in the cleanroom when I had a problem with the tools. I also thank current and past members of Prof. Misra's other research groups for all their support and encouragement: Dr. Niv Biswas, Steven Novak, Dr. Heather Lazar, Dr. Saurabh Chopra, Bongmook Lee, Dr. Rashmi Jha, Yan Du, Dr. Jaehoon Lee, Dr. YouSeok Suh, and Dr. Bei Chen.

There are several people outside the graduate school who have helped me out and also made my life as PhD student worthwhile. A special round of thanks and appreciation goes to my friends at NCSU and elsewhere: Shubha, Vijay, Chethan, Steven, Bhavin, Chirayu, Vikram, Mayank, Shivakumar, Arvind, Hari, Prashant, Shilpa, Vyshak, Sham, Rashmi and Shuba, for all their support and encouragement. A special mention goes to Manju and Guru, who have been great friends over last five years and have gone out of their way to help me out at certain times.

It is difficult for me to put in words as to how thankful I am for my parents, my sister Roopa and my brother-in-law Dinesh. It is largely due to their love and unwavering support that I have been able to persevere and sustain momentum, especially through all the tumultuous times at graduate school, to achieve my goals. My parents have always encouraged me and strived hard to enable me to pursue my chosen career path. For that, I am eternally grateful to them. I am blessed to have a wonderful sister and brother-in-law, who have constantly supported me. Special thanks to my two awesome nephews, Shardul and Anshul, who made my vacation breaks enjoyable after long semesters.

Lastly, I thank Schumi and Ferrari for dominating the world of Formula 1 during the years I was in graduate school and making my Sundays worthwhile.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF TABLES (PUBLISHED)

LIST OF FIGURES

LIST OF FIGURES (PUBLISHED)

1 INTRODUCTION

1.1 Nano Information Processing and Storage

The continued scaling of CMOS technology for last 4 decades has propelled an extraordinary exponential growth of information technology. According to ITRS, the downscaling of silicon will run into severe physical and economic limitations in a decade or two. In order to sustain the growth of information technology beyond ultimately scaled CMOS, semiconductor industry is faced with daunting challenges of (i) integrating new technologies on the CMOS platform in the near term, and (ii) inventing one or more fundamentally new approaches of information storage and processing in the longer term [1].

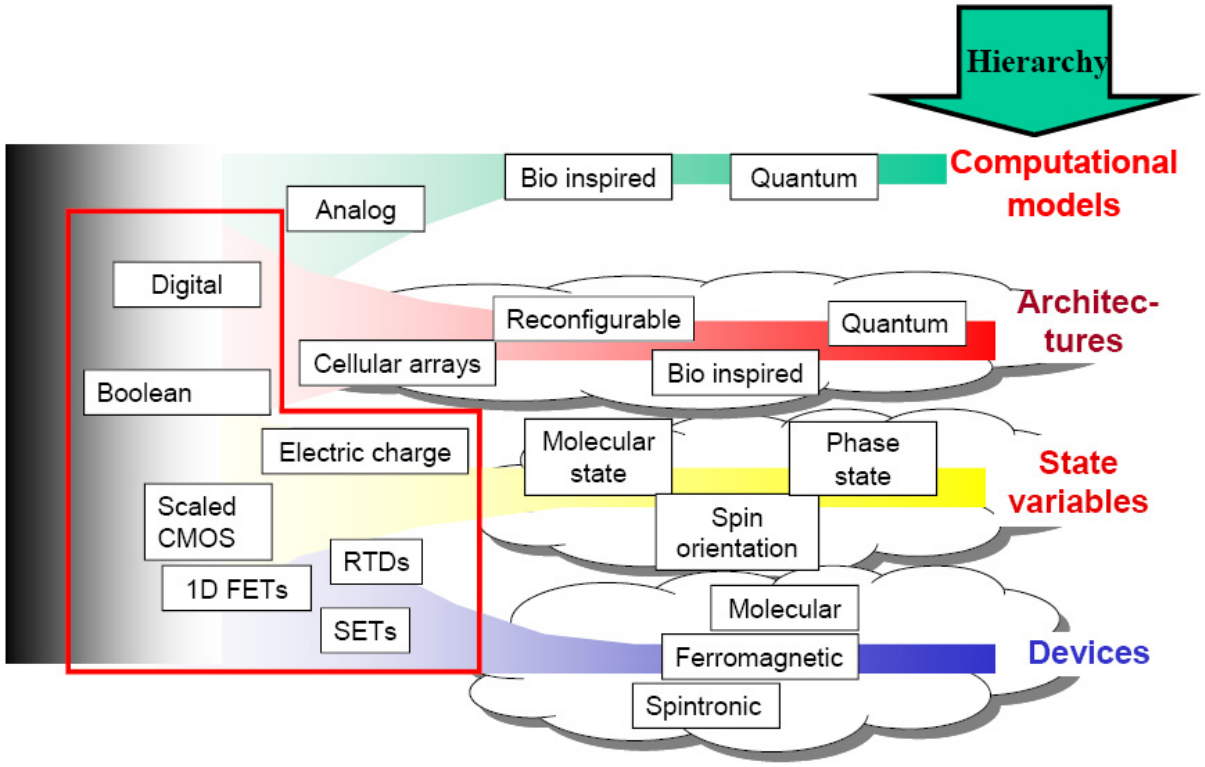


Figure 1.1 ITRS Nano Information Processing Taxonomy

The anticipation of end of silicon scaling has ushered in the new era of Nano information processing and storage, which involves non-classical CMOS efforts to enhance CMOS technology platform and will further require discovery of new means of physically representing, processing, storing and transporting information via new materials, process,

device, nano-architecture, and systems innovations. Fig. 1.1 shows the ITRS shows taxonomy for ITRS Nano information processing, outlining different layers of interacting technologies required to accomplish a system function. The elements shown in the red box represent current CMOS and other technologies based on charge as the computational state variable used in Boolean architecture enabling a digital computational model. The entries to the right of the red box grouped in the four categories summarize possible approaches to new device structures enabling some of the indicated new state variables to achieve the new nano-architectures and computational model. A new information processing technology will likely require an innovative and interactive combination of new elements in each of these layers.

1.2 CMOS Memory Technology

The current CMOS memory technology is projected by ITRS to scale down to 22 nm over the next decade [2]. The memory technologies can be differentiated into two categories based on the characteristic data retention time: (i) volatile memories with retention in range of milliseconds, and (ii) non-volatile memories with retention typically higher than 10 years. Among the current CMOS memory technologies, DRAM fits the former category while Flash fits the latter one. SRAM memory can be classified into volatile memory category where the memory state is preserved so long as voltage is applied. DRAM cell structure includes an access transistor (MOSFET) and a storage MOS capacitor (1T/1C cell). SRAM cell uses a bistable flip-flop structure consisting typically of six transistors (multi-T cell) to store the logic state. Flash cell is a modified conventional MOSFET structure (1T cell) with charge-storage node embedded in the gate dielectric stack. The details of cell structure and operation, and memory architecture of these CMOS memory technologies can be found in the references [3-5]. The research in emerging memory technologies are guided by existing CMOS memory technologies with a goal of providing the end-user with devices that behave similar to silicon memories. A strong theme in each of the candidate emerging research memory technologies is to integrate the memory option into CMOS platform in a seamless manner [2]. Because each of the new approaches attempts to mimic and improve on the capabilities of the present day memory technology, it is essential to understand the scaling trends of silicon memories and also list the key performance parameters of the existing baseline technologies. These parameters provide relevant benchmarks against which the

current and projected performance of each new emerging memory technologies is compared.

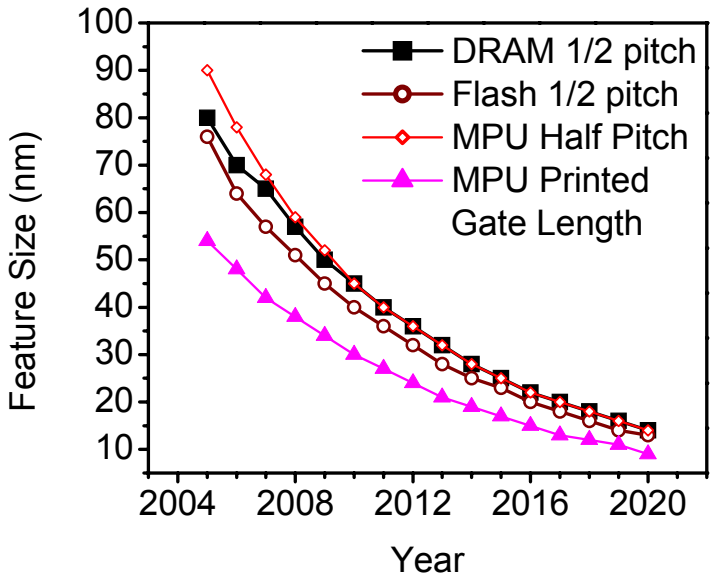


Figure 1.2 ITRS Scaling Projections for CMOS Memory and Logic Technologies

Fig. 1.2 shows the ITRS 2005 scaling projections for DRAM and Flash technologies along with that for CMOS logic (MPU) technology. It is essential to note that for DRAM and Flash technologies feature size corresponds to the half-pitch of the metal 1 layer [2]. Historically, DRAM has been the technology driver with tightest contacted metal pitch. However, we are in an era where there are multiple significant drivers of scaling. In case of Flash, along with half-pitch advancements, design factors have also been rapidly improved the Flash cell structure resulting in additional acceleration of functional density. Flash technology has also implemented electrical doubling of bits, enabling increased functional density independent of lithography half-pitch drivers.

Table 1.1 summarizes the cell structure and operation, and key performance parameters of the existing CMOS memory technologies. The ITRS projections for the year 2018 are also tabulated. As can be noted from the table, the major challenge is to achieve non-volatile memory requirement (>10 years) without compromising on the write/erase speeds and endurance (write cycles). Hence the goal of existing prototypical and emerging memory technologies is to build a universal memory which incorporates best features of

DRAM (fast write/erase, good endurance) and Flash (non-volatile). It is desirable for the technology to be amenable for integration on current CMOS platform so as to enable the realization of the System-on-a-chip (SoC) concept, which has been a long cherished dream of the semiconductor industry.

Table 1.1 Current Baseline Memory Technologies

		DRAM		SRAM	Floating Gate	
		Stand-alone	Embed-ded		NOR	NAND
Storage Mechanism		Charge on a capacitor		Interlocked state of logic gates	Charge on floating gate	
Cell Elements		1T1C		6T	1T	
Feature size F, nm	**2005**	80	130	90	130	130
	2018	18	25	18	25	25
Cell Area F^2	**2005**	7.5	12	140	10	5
	2018	5	12	140	10	5
Read Time	**2005**	<15 ns	1 ns	0.4 ns	14 ns	70 ns
	2018	<15 ns	<1 ns	70 ps	2.5 ns	12 ns
W/E time	**2005**	<15 ns	1 ns	0.4 ns	1 µs/10 ms	1 / 0.1 ms
	2018	<15 ns	0.2 ns	<0.1 ns	1 µs/10 ms	1 / 0.1 ms
Retention Time	**2005**	64 ms	64 ms	-	>10 y	> 10 y
	2018	64 ms	64 ms	-	>10 y	> 10 y
Write Cycles	**2005**	>3E16	>3E16	>3E16	>1E5	>1E5
	2018	>3E16	>3E16	>3E16	>1E5	>1E5

1.3 Prototypical Memory Technologies

There have been several research efforts over last decade to address the issue of extending and/or replacing silicon memories and a few among them have become mature prototypical technologies. The memory technologies discussed in this section have scaling limitations similar to CMOS memories. However, they have better performance in terms of retention time Vs processing speed (write/erase time) as compared to CMOS memory technologies. Although prototypes have been fabricated in each of these memory technologies to demonstrate the advantages, in most cases new material integration complexity has been a major drawback in implementing the same into large-scale

production. Table 1.2 summarizes the cell structure and operation, and key performance parameters of the existing prototypical memory technologies. The ITRS projections for the year 2018 are also tabulated.

Table 1.2 ITRS Summary of Prototypical Memory Technologies

		SONOS	FeRAM	MRAM	PCM
Storage Mechanism		Charge in gate insulator	Remanent polarization on a ferroelectric capacitor	Magnetization of ferroelectric contacts	Reversibly changing amorphous and crystalline phases
Cell Elements		1T	1T1C	1T1R	1T1R
Feature size F, nm	**2005**	100	130	180	90
	2018	20	25	22	18
Cell Area F^2	**2005**	7	34	25	7.2
	2018	5.5	16	16	4.7
Read Time	**2005**	14 ns	80 ns	<25 ns	60 ns
	2018	2.5 ns	<20 ns	<0.5 ns	< 60 ns
W/E time	**2005**	20μs/20ms	15 ns	<25 ns	50/120 ns
	2018	~10μs/10ms	1 ns	<0.5 ns	Not known
Retention Time	**2005**	>10 y	>10 y	>10 y	>10 y
	2018	>10 y	>10 y	>10 y	>10 y
Write Cycles	**2005**	1E7	1E13	>1E15	1E12
	2018	1E9	>1E16	>1E15	1E15

The following is a brief description of the prototypical memory technologies with advantages and challenges for each of the technologies:

1. **Ferroelectric Memory:** In ferroelectric memories, information is stored as a sign of electric polarization of a layer of a ferroelectric material [6, 7]. The ferroelectric film has the characteristic of a remnant polarization, which can be reversed by an applied electric field. Voltage pulses are used to write and read the digital information. The different state of the remnant polarization (+/-) causes different current behavior of the ferroelectric capacitor to an applied voltage pulse. This polarization may be read out either destructively (as in FeDRAM) or non-destructively (if it controls a readout FET as in case of FeFET, which is

categorized under emerging research memories). The advantages of ferroelectric memories are high density, fast write/erase and potential for non-volatility. The challenges are material complexity and compatibility with CMOS, and scaling [7].

2. **Magnetoresistive Memory:** At the heart of a Tunnel Magnetoresistance(TMR) device is a set of ferromagnetic layers separated by an insulating oxide layer (typically Al_2O_3) [8]. The electrical resistance of this arrangement depends on the magnetization direction of the two magnetic layers with respect to one another. The tunneling resistance for parallel magnetization defines one logic state while the resistance for anti-parallel alignment defines the other state. The cell is written by current-induced magnetic switching. The advantages and challenges of this technology are similar to Ferroelectric memory technology.

3. **Phase Change Memory:** It is also called Ovonic unified memory (OUM) and is based on a rapid reversible phase change effect in some materials under the influence of electric current pulses [9, 10]. In an OUM cell, a chalcogenide alloy is switched from a conductive crystalline phase to a highly-resistive amorphous phase under the effect of heating by current passed through a special heater. Data is read by measuring the resistance changes in the cell. OUM cells can be programmed to intermediate resistance values for multi-state data storage. The advantages include fast access times, long endurance, and good data retention. The challenges are decrease write current to make it compatible with CMOS, material complexity and scaling.

All of these prototypical memory technologies have been adopted by the semiconductor industry and are in different phases of development. Freescale Semiconductor announced the commercial availability of 4 Mb MRAM memory chip in July, 2006. Although all of these technologies have attracted industry to commercialize them, they are yet to prove themselves in the memory market.

1.4 Emerging Memory Technologies

There are several research efforts exploring a variety of memory mechanisms towards alternative building alternative memory technologies. The technologies listed in this

section are the ones acknowledged by ITRS as emerging memory technologies with significant number of representative research publications [1]. The most prominent of memory mechanisms being investigated include charge isolated by surrounding dielectrics; remnant polarization on a ferroelectric gate dielectric, and resistance change caused by a variety of phenomena.

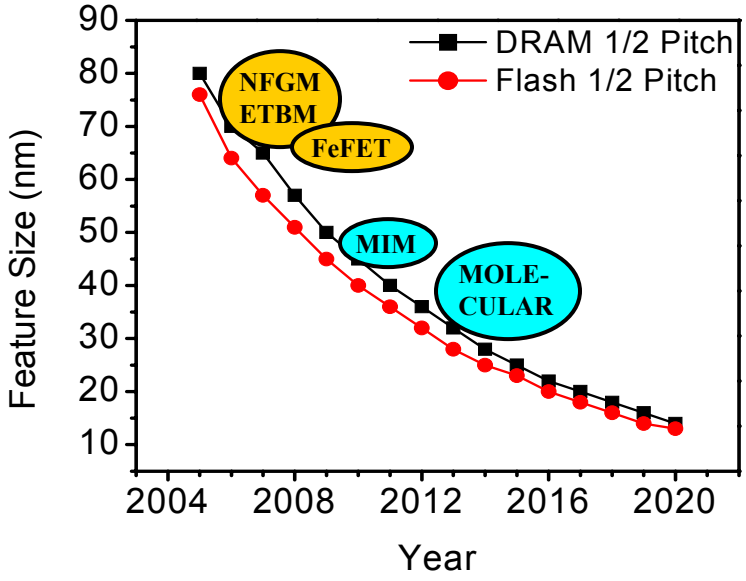


Figure 1.3 ITRS projected availability of emerging memory devices against the backdrop of CMOS memory technology scaling. The feature size of each emerging memory device corresponds to the projected size at the time of availability and NOT the best projected scaleable value. The devices represented in golden-colored oval: Nano-Floating Gate Memory (NFGM), Engineered Tunnel Barrier Memory (ETBM) and Ferroelectric FET (FeFET) have scaling issues to similar to that of silicon memory devices. The devices in blue-colored oval: Insulator Resistance Change (MIM) and Molecular are considered to be scaleable beyond silicon.

Fig. 1.3 shows the ITRS projected availability of emerging memory devices and Table 1.3 summarizes the device structures and operation, and best projected key performance parameters of these memory devices. A brief review is provided here and more detailed description of each of these memory devices with exhaustive list of relevant publications can be found in the ITRS 2005 Emerging Research Devices report [1].

1. **Nano-Floating Gate Memory (NFGM):** NFGM includes several possible evolutions of conventional floating gate and SONOS memories. NFGM includes proposals to improve the performance of the floating gate memory cells by replacing the conducting floating gate with discrete charge-trap storage node.

The charge injection to storage node can be by: (i) hot carrier injection and Fowler-Nordheim (FN) tunneling [11] or (ii) direct tunneling [12]. In NFGM the discrete charge-trap storage node consists of multiple nanocrystal dots or charge-trapping defects in insulator [13]. The multiple floating dots are separated and independent, and electrons are injected to the dots via different paths. The endurance and retention problem can be much improved in multi-dot (nanocrystal) memory. NFGM is a natural evolution of the conventional floating gate memory and offers only marginal improvements in operation parameters as can noted from Table 1.3.

Table 1.3 Emerging Research Memory Devices - ITRS Projected Parameters

	Nano-Floating Gate	Engineer-ed Tunnel Barrier Memory	Ferro-electric FET Memory	Insulator Resistance Change	Polymer Memory	Molecular
Storage Mechanism	Charge on floating gate	Charge on floating gate	Remnant polarization on a ferro-electric gate dielectric	Multiple mecha-nisms	Not known (N. k.)	Not known
Device Types	1.Nano-crystal 2.Direct Tunneling	Graded Insulator	FET with FE gate insulator	1. M-I-M 2. Solid Electrolyte 3. FE tunneling 4. FE-I-FE	M-I-M(nc)-I-M	1.Bi-stable Switch 2.Storage Capacitor
Cell Elements	1T	1T	1T	1T1R or 1R	1TIR or 1R	1T1R, 1R or IT1C
Availability	>2008	>2008	>2010	~2010	>2010	>2010
Initial Size F	80 nm	80 nm	Not known	65 nm	45 nm	45 nm
Best Size F	25 nm	10 nm	22 nm	5-10 nm	5-10 nm	5-10 nm
Cell Size F^2	8-10	8	8	8/5	8/5	5
Access Time	2.5 ns	2.5 ns	2.5 ns	<10 ns	<10 ns	< 10 ns
W/E Time	1 μs/10ms	1 ns	2.5 ns	<20 ns	N. k.	< 40 ns
Retention T	> 10 y	>10 y	>1 y	> 10 y	N. k.	N. k.
E/W Cycles	>1E5	>3e16	>3e16	>3e16	>3e16	>3e16

2. **Engineered Tunnel Barrier Memory (ETBM):** Engineered Tunnel Barrier in the floating gate memory allows for lowering of the voltage required for write/erase of the cell by providing high tunneling current at low applied voltage while maintaining good data retention. ETBM includes graded barrier floating gate memory [14] and variable oxide thickness floating gate memory [15]. The theory behind ETBM proposed concepts will be discussed later in chapter 3.

3. **Insulator Resistance Change Memory:** This category of emerging memory devices includes a range of metal-insulator-metal (MIM) systems which show electrical pulse induced resistance change effects. The material class is comprised of oxides, higher chalcogenides, semiconductors, as well as organic compounds including polymers. One variant is based on the cation transport, the cathodic reduction, and the growth of metallic filaments [16, 17]. The filament thus formed defines the low-resistance state of the device while oxidation dissolves the filament and returns the device to high resistance state. Another variant include formation and dissolution of metal filaments through ultra-thin high-k dielectric films [18]. If this effect can be controlled, memories based on this bi-stable switching process can be scaled to very low feature sizes.

4. **Polymer Memory:** The memory element consists of a organic-metal-organic triple layer sandwiched between two metal electrodes [19]. Although switching characteristics of these devices are similar to Insulator Resistance Change memory devices, it is suggested the switching mechanism is not associated with formation and dissolution of metal filaments. Recently, it was reported that a single-layer polymer M-I-M structure demonstrates similar behavior and hence the exact mechanism is unclear [20].

There are several other research memory devices that have been proposed and investigation as potential candidates for silicon memory extension and replacement. Single electron memory was considered as one of the most promising candidate technologies beyond silicon with expected device densities to achieve terabit memory. However, ITRS has dropped single electron memory from list of emerging research memory devices as it does not fit any application categories and also due to lack of realistic device demonstrations with practical application.

1.5 Molecular Electronics

Molecular electronics holds the promise to scaling the integrated circuits to nano dimensions by way of engineering the functionality of the electronic circuitry components into individual molecules. The researchers in the field claim to replace the conventional silicon based computing even before it hits the fundamental limits. The advantages of molecule based devices, outlined in later sections, would propel the technology as a candidate to replace and/or extend traditional silicon technology in the event of successfully wiring and integrating the engineered molecules on a giga-scale and beyond. However, critics are skeptical about the unreasonable promises held by some of the proponents of this technology. The promise of workstations that will operate for decades powered only by a small battery or 1000 Pentiums on the same base have attracted concerns [21].

In 2001, Science heralded molecular electronics as the Breakthrough of the year as scientists assembled molecules into basic circuits, mostly for memory applications, raising hopes for a new world of Nanoelectronics [22]. Several teams had wired up their first molecular scale logic and memory circuits, but were still faced with formidable task of taking the technology from demonstrations of rudimentary circuits to highly complicated integrated circuitry that can improve upon silicon's speed, reliability and low cost. There was also a need for understanding the mechanism involved when molecules are sandwiched between two electrodes as most of the theories and techniques pertained to structure and dynamics of molecules in solution.

The molecule-electrode interface is a critically important component of any molecular device and the state of the art of theory of the interface was and still is primitive. The possibility of damaging or unpredictably modifying the molecules during the contact formation was also of major concern. These factors fueled critics to raise doubts about the validity of the explanation of the mechanisms involved in the devices. In summer of 2003, the "Next-Generation Technology" suffered a minor setback when two of most prominent research groups acknowledged that some of their devices do not work as previously thought resulting in relegation of some of these devices from category of molecular electronics to molecule-enabled electronics [23]. However, this does not take away anything from the science that is emerging out of the research on molecular electronics. In spite of the above

setbacks, molecular devices are making fresh strides towards realistic logic and memory applications [24]. Despite the disadvantages and challenges the technology faces, there are numerous advantages that render molecules ideal for electronic applications, as Richard Feynman noted in his famous 1959 speech, “There is Plenty of Room at the Bottom.”

The present day technological goals of molecular electronics have been limited to computational and sensing applications, but it may not be the case in future. Interface to bio-systems, pathways toward molecular mechanical and nanomechanical devices are among the likely beneficiary of the successful development of the molecular-electronic integrated circuitry. The strongest of the proponents do admit that molecular electronics may not dethrone silicon from top of the computing world in near future, but “To say ‘never’ is foolish” says Edwin Chandross, a chemist retired from Bell Labs and critic of the field. However, molecular based systems may still work its way into applications, such as sensing, that silicon based electronics cannot handle in near future.

1.6 Advantages and Challenges of Molecular Electronics

1.6.1 Advantages

Molecular electronics is one of the candidate approaches for ITRS emerging new device technologies for information processing and storage beyond the domain of CMOS. For electronic applications, molecular structures have following major advantages:

1. **Scalability to nano-dimensions:** Molecules are several orders of magnitude smaller than present feature size with size scale between 1 and 100nm. So the inherent scalability of molecules permits functional nanostructures and very high device densities can be achieved.

2. **Self-Assembly:** Molecules have the potential to organize themselves on surfaces, in other words self-assemble, to form nanostructures. The chemically induced self-organization processes may be also exploited to assist the formation of highly regular molecular circuits.

3. **Synthetic tailorability:** The tools of molecular synthesis are highly developed. Hence, molecule's transport, binding and structural properties can be extensively varied by choice of composition and geometry.

4. **Low Power:** Due to a small number of electrons required for molecular switching processes, the switching energy may be significantly reduced compared to values for current and emerging research technologies.

5. **Recognition:** Molecular recognition can be used to modify electronic behavior, providing both switching and sensing capabilities on the single-molecule scale.

6. **Multi-state Cell:** Many molecules have multiple distinct stable geometric structures or isomers that can have distinct electronic and optical properties.

1.6.2 Challenges

Molecular electronics is faced with several challenges become it can mature into a competitive technologies. The major challenges are listed as follows:

1. **Large-scale Integration and Electrode Effects:** One of the biggest challenges molecular electronics has to overcome before it can become a competitive technology is wiring the functional nanostructures. This requires a high degree of reproducibility, defect tolerance and cost effectiveness. There is no potential cost effective solution to achieve high density molecular electronic circuitry. There are several researchers who have been successful in building rudimentary molecular circuits, primarily involving nanowire and carbon nanotube crossbars. In this configuration, two rectangular grids of either nanowires or nanotubes are laid down perpendicular to one another and molecules are sandwiched between intersections of the two grids. However, the challenge here is to figure out how to wire these molecular circuits into complex integrated circuitry for large scale logic and memory applications. Also, crossbars are usually prone to cell write/erase disturbs and may require integration of access diode or transistor at each intersection [18]. However, before attempting to resolve the integration issues, it is of paramount interest to address some of the issues pertaining to contacting the individual molecule or ensemble of molecules. The molecule-electrode

interface is a vital component of a molecular junction as it may limit current flow or completely modify the measured electrical response of the junction. In addition to these, the processing step of contacting the molecule might damage or modify the properties of the molecules resulting in unpredictable effects. The knowledge base of charge transport through molecules in a solid state setting and that on molecule-electrode interfaces is minimal. When molecules are sandwiched between two electrodes, the theories and analytical techniques based on solution-phase science is not completely applicable and hence there is need to develop new concepts. Also certain critical aspects of basic solid-state-device physics cannot be directly translated directly into the world of molecular electronics. It is difficult to adequately predict how the molecular orbitals' energy levels will align with the Fermi energy of the electrode. This is because molecular orbitals are spatially localized, whereas in solids the atomic orbitals form extended energy bands. Another consideration involves how the chemical nature of the molecule-electrode interface affects the rest of the molecule. The chemical interaction between the molecule and the electrode will likely modify the molecular energy levels or the barriers within the junction [25]. Therefore, the fundamental challenge is to develop an intuition of how molecules behave in solid-state settings and to use that intuition as feedback to molecular synthesis.

2. **Endurance and Thermal Stability:** There is wide scale skepticism about whether molecular electronics circuitry would have the reliability and endurance that would compare with that of the conventional silicon devices. At present, there is no molecular electronic logic or memory device that has been tested for reliability on a large scale basis. Another key requirement of a practical molecular electronic device is endurance over very large numbers of operational lifecycles over lifetime ($>10^{12}$). Several studies of molecular devices are carried out over a limited number of cycles, often at cryogenic temperatures. This is true with most of the published data and several of these devices lose their electronic properties after only after 10s or 100s of cycles. Also, for viable implementation of molecular components in electronic devices, the molecular materials must be robust under extreme conditions of temperature, including high temperature processing steps during manufacture (~400^{o}C) and relatively high temperature

operating conditions (~140^{o}C). The latter requirement stems from the facts that (i) heat dissipation in current chips causes operating temperatures to reach as high as 85^{o}C and (ii) these components must function in hard external environments with extremes in temperature. Most organic molecules thermally decompose at elevated temperatures, say 400^{o}C. So it is essential to use molecular synthesis to make the make the molecules stable at high temperatures.

3. **Gain for Logic:** Experimental demonstrations to date, of bistable switching performed using both two-terminal devices and three-terminal memory devices, are without gain [26]. Gain is a necessary feature in logic for sending signals through multiple devices. There is no such molecular device that has been identified to have gain. Two terminal molecular devices currently being explored act as digital switches or as analog diodes. It is technically unrealistic to expect gain in a two terminal setting especially if the switching is based on change in molecule's conduction properties. The three terminal molecular devices are mostly based on coulomb blockade and resonant tunneling effects at close to absolute zero temperatures.

4. **Non-volatility for Memory:** The retention times of most of the molecular memory devices varies from few seconds to maximum of ~one month. One of the biggest challenges of molecular memories is to increase the retention time to match the requirements for non-volatile memory (>10 years) in order to be as a candidate technology for universal memory.

1.7 Molecular Memory Research

Molecular memory encompasses individual molecules as building blocks of memory cells in which one or more bits of information are stored within the molecule. There are several different approaches involving conductivity-switching and charge-storage molecules adopted by various research groups and some of the prominent ones are discussed here. One experimentally demonstrated approach is based on reversible change of effective conductance of a molecule attached between two electrodes controlled by applied voltage. Other concepts of molecular memory involve combining molecular components with the

current memory technology, such as DRAM and floating gate memory. The ITRS recognizes molecular memory as one of the emerging technologies beyond CMOS for both logic and memory applications. Molecular memories are projected to be available beyond 2010 and perceived to be the most risky of the emerging memory technologies listed by ITRS [26]. This might be attributed to the fact that molecular memory is most recent of the technologies in the list and also due to the revelation that some of the earlier reported experimental results on molecular switches were affected by artifacts. Consequently ITRS insists that the knowledge base of molecular electronics needs further work [1, 26].

1.7.1 Conductance Switching Approaches

The most common approach in the molecular memory devices has been the bistable conductance switch device. The device generally has metal-molecule-metal structure with individual molecule expected to be sandwiched between two metal electrodes. It has been proposed the molecule can be reversibly switched between high (or low) and low (or high) conductance (or resistance) state by applying voltage pulses according the molecule (or the device) [27, 28]. The different conductance states define the written and erase state of the memory device. There are two main architectural approaches based on these devices:

1. **Molecular Crossbar Circuits:** In a crossbar circuit, the molecular component is typically sandwiched between the intersection of two crossing wires [29]. One of the molecules used in this work is the bistable rotaxane, which are sandwiched between the two metal nanowires at the crosspoints to act as reversible, electrically toggled switches. The switching mechanism was attributed to electromechanical transformation of rotaxane molecule between two stable mechanical states which exhibit different tunneling currents. However, recent experimental results by the same group with several types of molecules in the same device structure indicated that the switching observed or the hysteresis in current-voltage characteristics was independent of the molecule [30]. The same group then described that the charge transport mechanism was different from the proposed electromechanical switching mechanism of rotaxanes in solution phase. The conductance switching in these metal-molecule-metal structures have been now attributed to formation and dissolution of individual nanoscale

electrode metal filaments through the molecular layer [31]. The exact mechanism for filament formation and dissolution is not well understood.

2. **Nanocell Electronic Memories:** A nanocell is a two-dimensional network of self-assembled metallic particles connected by molecules that are believed to show reprogrammable negative differential resistance (NDR) based switching and memory storage effects [32]. The NDR observed in these metal-molecule-metal structures had been initially attributed to the single redox center contained in the self-assembled monolayers of the molecule. However, control experiments have suggested that the memory effect is more likely due to nanofilamentary metal switching mechanisms rather than molecular electronic behavior as proposed earlier [33].

1.7.2 Molecule Gated Nanowire Memory

This approach involves assembling bistable nanoscale switches nanowires (NWs) and redox active molecules as building blocks for non-volatile memory and programmable logic. The nanodevices consists of NW-FETs functionalized with redox-active molecules, where the redox species can store charges and thereby maintain NW-FETs in either a logic on or off state [34]. The exact mechanism of charge injection into redox-active molecules is not well understood. The approach is also faced with challenges relating to large-scale integration, endurance, thermal stability and data retention.

1.7.3 Hybrid Silicon-Molecular Approach

The hybrid silicon-molecular approach refers to incorporation of molecules into existing CMOS devices. The details of this approach will be discussed in next section. The research work presented in this dissertation is categorized under this approach.

1.8 Hybrid Silicon-Molecular Memory

Molecular electronics has been able to generate lot of interest as a potential candidate technology beyond silicon. However, as discussed in the previous sections, there are several daunting challenges that have impeded the progress of molecular electronics towards maturing into a competitive technology in near term. A hybrid/silicon molecular

approach may be instrumental in providing a transitional path to a future molecule-only technology and augmenting today's CMOS only technology [35, 36]. One such approach was proposed by researchers at North Carolina State University and University of California, Riverside. This approach involves utilizing redox-active organic molecules with multiple accessible (quantized) energy states as charge storage elements [37, 38]. This approach is different from most of the other approaches in the field in following two ways:

1. **Hybrid CMOS-molecular approach:** The redox-active molecules are incorporated onto existing CMOS devices by way of self-assembly on silicon surfaces.

2. **Discrete Charge-Storage:** This approach exploits ability of each individual molecule to store charges with single-electron precision at room temperature, and is fundamentally different from the conductance-switching approaches which are based on measuring the change in the conductivity of molecules. The charge storage in the hybrid devices are intrinsic property of the molecules. Hence, the amount of charge in the hybrid device depends on the number of molecules incorporated on the device, and not on the applied voltage as in case of a conventional capacitor.

As a consequence of the latter distinction, there is a difference in the device architecture as compared to that of the conductance-switching (metal-molecule-metal) devices, which are primarily regarded as resistors. The top (gate) electrode of a two-terminal hybrid silicon-molecular storage element is electrically insulated (dc-blocked) from the molecular layer but capacitively coupled to the same making the storage element a capacitor (metal-insulator-molecule-silicon). In other words, molecules can exchange charges only with silicon (or bottom electrode). The details of hybrid device structures and their operation will be provided in the next section.

1.8.1 Hybrid Silicon-Molecular Devices

The motivation of this approach is to develop a class of hybrid silicon-molecular memory devices that leverage on the knowledge base of the memory technology built on silicon while fully exploiting the unique properties of the molecules. The redox-active

molecules with quantized charge states are incorporated on silicon surfaces to obtain two kinds of devices which are equivalent to conventional DRAM and Flash memory cells. Fig. 1.4 shows the schematics of the hybrid silicon-molecular devices. In the MoleDRAM cell, a hybrid silicon-molecular capacitor acts as the storage capacitor and conventional MOSFET is used as an access transistor. The memory cell is written by applying an oxidizing voltage across the hybrid capacitor which electrons from molecules thereby leaving the molecular layers positively-charged. A reducing voltage on the capacitor returns the electrons to the molecules, which erases the memory cell by returning the molecules to neutral state. The state of the memory cell is read (destructively) by applying a reducing voltage and monitoring the current. The access transistor is gated ON during write, erase and read processes, and remains OFF during retention state. The advantages of the MoleDRAM cell over the conventional DRAM are: higher charge density, scaleable to molecular dimensions, lower power consumption (consequence of higher data retention time), low-voltage operation and multiple bits in single cell [39]. However, there are several challenges for this device that need to be overcome before the device can attempt to dethrone the silicon-based DRAM with the most important being making the top electrode contact to the molecules assembled on the silicon.

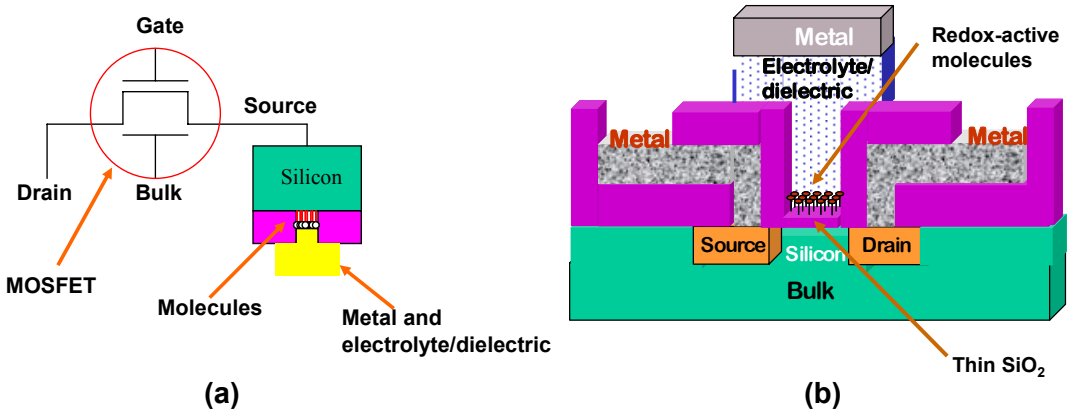


Figure 1.4 Schematics showing structure of hybrid silicon-molecular memory devices: **(a)** MoleDRAM mimics the conventional DRAM (1T1C cell) with hybrid silicon-molecular capacitor as storage capacitor and a conventional MOSFET as access transistor. **(b)** MoleFET is inspired by the conventional Flash cell with redox-active molecules incorporated on gate tunnel oxide acts as nano floating storage nodes.

The MoleFET device has redox-active molecules incorporated on ultra-thin layer of gate oxide (tunnel barrier) with the intent of modulating the channel potential utilizing the quantized charge states in the molecules [40]. Hence, the molecules serve to act as discrete charge-storage nodes or nano-sized floating nodes. The write/erase processes and states are similar to that of the MoleDRAM device. However, the read process is non-destructive and involves monitoring the drain current of the FET device while applying a gate voltage that has intermediate value of oxidizing and reducing voltages. The threshold voltage of the device is a strong function of charges in the molecule and hence the drain current value depends on the charge-state (positive or neutral) of the molecules. The advantages of MoleFET device include higher charge density, low-voltage of operation, limited lateral conductivity within the molecular layer and multiple bits in single cell. In addition to challenges similar to that of MoleDRAM cell, MoleFET device has the challenge of achieving data retention to meet the requirements for non-volatile memory.

1.9 Focus of my research

The main objective of this research work was to gain fundamental insights into the interaction of redox-energy states in the molecules with the silicon substrate and investigate approaches for exploiting the unique properties of the molecules that may enable solutions for nanoscale high density, low-voltage, long retention and multiple bit memory applications. In particular, the study was focused on the fabricating and characterizing the MoleFET device to evaluate the key performance parameters for suitability of the device for nano-Flash applications. The following initiatives were undertaken to that extent:

1. Investigate the properties of molecules self-assembled on Si surfaces to study the effect of Si doping type and density on the redox response (write/erase voltages and speeds, and charge retention).

2. Engineer the molecule-to-silicon barrier by utilizing ultra-thin tunnel barriers of SiO_2, HfO_2 with intent of enhancing the charge retention of the device. This involves studying the dependence of redox response on the tunnel barrier thickness, energy barrier and dielectric permittivity.

3. Engineer the substrate (silicon) component of the hybrid silicon-molecular devices as complement to molecule engineering in order to achieve novel functionality, modulate electrical properties of the device, and interrogate the intrinsic properties of the molecules.

4. Fabricate MoleFETs by incorporating the redox-active molecules on ultra-thin gate (tunnel) oxide of Si MOSFETs with the intent of studying the interaction of redox states with the Si MOSFETs and investigate towards Flash memory applications.

Lastly, there were efforts made towards achieving solid-state solutions for large-scale integration of the hybrid memory devices. Investigations to that extent involved attempts with goals of (i) completely replacing the electrolyte gate with solid-state layers, or (ii) making the electrolyte amenable to a hybrid electrolyte-{solid-state} integration.

1.10 Overview of the Dissertation

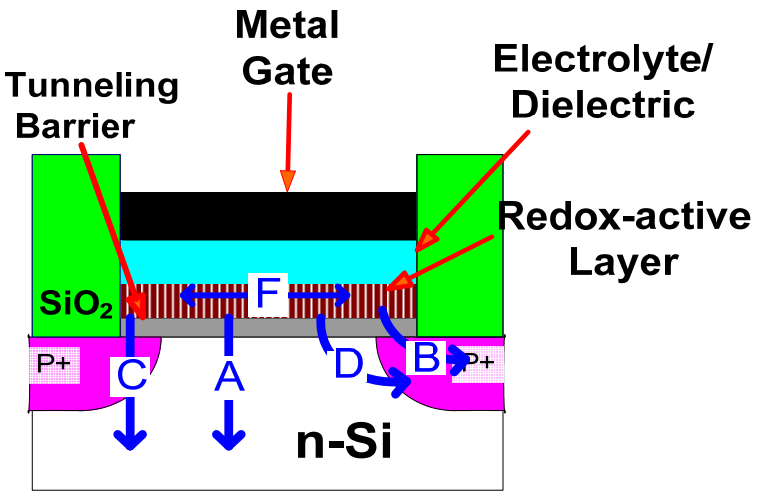


Figure 1.5 Schematic of MoleFET showing electrical pathways for the redox-states of molecules. Pathways **A** and **B** correspond to interaction of molecules, on channel and source/drain overlap respectively, directly with the respective silicon regions. Pathways **C** and **D** correspond to interaction of molecules with the diodes (p+/n and n/p+ respectively). Pathway **F** corresponds to lateral interaction of the redox-centers within the molecular layer.

The dissertation is divided into six chapters including the 'Introduction'. The second chapter includes details of the materials and experimental methods used in this study. The third chapter is 'Molecules on Si and Oxides' and it contains results and discussion on properties of redox-active molecules assembled on Si and oxide surfaces. Apart from

providing fundamental insights into the interaction of redox-states of the molecules with Si substrate and investigation towards the DRAM application, the knowledge gained from this chapter is useful in evaluating the electrical characteristics of the MoleFET device (particularly pathways **A** and **B** depicted in Fig. 1.5). The fourth chapter is 'Molecules on Silicon Diodes: Substrate Engineering' and it covers discussion about engineering the silicon component of the hybrid silicon-molecular devices to achieve novel functionality and study the intrinsic properties of the molecules such as lateral conductivity within the assembled molecular layers. Also, from the perspective of the MoleFET device, pathways **C**, **D** and **F**, illustrated in Fig. 1.5, are explored in this chapter. The fifth chapter has details about fabrication and characterization of the MoleFET devices and is titled 'Hybrid Silicon-Molecular FET'. It also includes discussion about modeling the interaction of redox-energy states with Si MOSFETs. Finally, sixth chapter summarizes the research work of this dissertation and provides future 'Outlook' for the area of hybrid silicon-molecular memory devices. The sixth chapter also includes 'Approaches towards Integration' and as the name suggests it contains results of preliminary efforts towards achieving solid-state integration for the hybrid silicon-molecular devices. Chapters 3 to 5 includes publications in the corresponding topic area and the chapters are built around the included papers.

1.11 References

[1] *International Technology Roadmap for Semiconductors 2005, Emerging Research Devices*, 2005.

[2] *International Technology Roadmap for Semiconductors 2005, Executive Summary*, 2005.

[3] S. M. Sze, "MOS Memory Structures," in *Semiconductor Devices, Physics and Technology*, 2nd ed. New York: Wiley, 2002, pp. 214-218.

[4] S. M. Sze, "Nonvolatile Memory Devices," in *Physics of semiconductor devices*, 2nd ed. New York: Wiley, 1981, pp. 496-506.

[5] P. Pavan and R. Bez, "The Industry Standard Flash Memory Cell," in *Flash Memories*, P. Cappelletti, C. Golla, P. Olivo, and E. Zanoni, Eds. Boston, Mass: Kluwer Academic Publishers, 1999, pp. 37-81.

[6] U. Bottger and S. R. Summerfelt, "Ferroelectric Random Access Memories," in *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*, R. Waser, Ed., 2nd ed: Wiley-WCH, 2005, pp. 565-587.

[7] K. Kim and Y. J. Song, "Current and future high density FRAM technology," *Integrated Ferroelectrics*, vol. 61, pp. 3-15, 2004.

[8] J. M. Slaughter, M. DeHerrera, and H. Durr, "Magnetoresistive RAM," in *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*, R. Waser, Ed., 2nd ed: Wiley-VCH, 2005, pp. 591-603.

[9] Y. N. Hwang, J. S. Hong, S. H. Lee, S. J. Ahn, G. T. Jeong, G. H. Koh, H. J. Kim, W. C. Jeong, S. Y. Lee, J. H. Park, K. C. Ryoo, H. Horii, Y. H. Ha, J. H. Yi, W. Y. Cho, Y. T. Kim, K. H. Lee, S. H. Joo, S. O. Park, U. I. Jeong, H. S. Jeong, and K. Kinam, "Phase-change chalcogenide nonvolatile RAM completely based on CMOS technology," 2003.

[10] W. Y. Cho, B. H. Cho, B. G. Choi, H. R. Oh, S. B. Kang, K. S. Kim, K. H. Kim, D. E. Kim, C. K. Kwak, H. G. Byun, Y. Hwang, S. J. Ahn, G. H. Koh, G. Jeong, H. Jeong, and K. Kim, "A 0.18-mu m 3.0-V 64-Mb nonvolatile phase-transition random access memory (PRAM)," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 293-300, 2005.

[11] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, "A silicon nanocrystals based memory," *Applied Physics Letters*, vol. 68, pp. 1377-1379, 1996.

[12] S. Lombardo, B. De Salvo, C. Gerardi, and T. Baron, "Silicon nanocrystal memories," *Microelectronic Engineering*, vol. 72, pp. 388-394, 2004.

[13] B. De Salvo, C. Gerardi, R. van Schaijk, S. A. Lombardo, D. Corso, C. Plantamura, S. Serafino, G. Ammendola, M. van Duuren, P. Goarin, W. Y. Mei, K. van der Jeugd, T. Baron, M. Gely, P. Mur, and S. Deleonibus, "Performance and reliability features of advanced nonvolatile memories based on discrete traps (silicon nanocrystals, SONOS)," *Ieee Transactions on Device and Materials Reliability*, vol. 4, pp. 377-389, 2004.

[14] K. K. Likharev, "Riding the crest of a new wave in memory," *Ieee Circuits & Devices*, vol. 16, pp. 16-21, 2000.

[15] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, and K. De Meyer, "VARIOT: A novel multilayer tunnel barrier concept, for low-voltage nonvolatile memory devices," *Ieee Electron Device Letters*, vol. 24, pp. 99-101, 2003.

[16] M. N. Kozicki, C. Gopalan, M. Balakrishnan, and M. Mitkova, "A low-power nonvolatile switching element based on copper-tungsten oxide solid electrolyte," *Ieee Transactions on Nanotechnology*, vol. 5, pp. 535-544, 2006.

[17] T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa, T. Nakayama, and M. Aono, "Nanometer-scale switches using copper sulfide," *Applied Physics Letters*, vol. 82, pp. 3032-3034, 2003.

[18] I. G. Baek, D. C. Kim, M. J. Lee, H. J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O. Park, H. S. Kim, I. K. Yoo, U.

Chung, J. T. Moon, and B. I. Ryu, "Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application," 2005.

[19] J. Y. Ouyang, C. W. Chu, C. R. Szmanda, L. P. Ma, and Y. Yang, "Programmable polymer thin film and non-volatile memory device," *Nature Materials*, vol. 3, pp. 918-922, 2004.

[20] D. Tondelier, K. Lmimouni, D. Vuillaume, C. Fery, and G. Haas, "Metal/organic/metal bistable memory devices," *Applied Physics Letters*, vol. 85, pp. 5763-5765, 2004.

[21] E. A. Chandross, "More on molecular electronics," *Science*, vol. 303, pp. 1137-1137, 2004.

[22] R. F. Service, "Molecules get wired," *Science*, vol. 294, pp. 2442-2443, 2001.

[23] R. F. Service, "Molecular electronics - Next-generation technology hits an early midlife crisis," *Science*, vol. 302, pp. 556-+, 2003.

[24] R. F. Service, "Molecular electronics - Nanodevices make fresh strides toward reality," *Science*, vol. 302, pp. 1310-1310, 2003.

[25] J. R. Heath and M. A. Ratner, "Molecular electronics," *Physics Today*, vol. 56, pp. 43-49, 2003.

[26] *International Technology Roadmap for Semiconductors 2003, Emerging Research Devices*, 2003.

[27] A. R. Pease, J. O. Jeppesen, J. F. Stoddart, Y. Luo, C. P. Collier, and J. R. Heath, "Switching devices based on interlocked molecules," *Accounts of Chemical Research*, vol. 34, pp. 433-444, 2001.

[28] J. Chen, W. Wang, M. A. Reed, A. M. Rawlett, D. W. Price, and J. M. Tour, "Room-temperature negative differential resistance in nanoscale molecular junctions," *Applied Physics Letters*, vol. 77, pp. 1224-1226, 2000.

[29] Y. Chen, G. Y. Jung, D. A. A. Ohlberg, X. M. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, and R. S. Williams, "Nanoscale molecular-switch crossbar circuits," *Nanotechnology*, vol. 14, pp. 462-468, 2003.

[30] D. R. Stewart, D. A. A. Ohlberg, P. A. Beck, Y. Chen, R. S. Williams, J. O. Jeppesen, K. A. Nielsen, and J. F. Stoddart, "Molecule-independent electrical switching in Pt/organic monolayer/Ti devices," *Nano Letters*, vol. 4, pp. 133-136, 2004.

[31] C. N. Lau, D. R. Stewart, R. S. Williams, and M. Bockrath, "Direct observation of nanoscale switching centers in metal/molecule/metal structures," *Nano Letters*, vol. 4, pp. 569-572, 2004.

[32] J. M. Tour, W. L. Van Zandt, C. P. Husband, S. M. Husband, L. S. Wilson, P. D. Franzon, and D. P. Nackashi, "Nanocell logic gates for molecular computing," *Ieee Transactions on Nanotechnology*, vol. 1, pp. 100-109, 2002.

[33] J. M. Tour, L. Cheng, D. P. Nackashi, Y. X. Yao, A. K. Flatt, S. K. St Angelo, T. E. Mallouk, and P. D. Franzon, "NanoCell electronic memories," *Journal of the American Chemical Society*, vol. 125, pp. 13279-13283, 2003.

[34] X. F. Duan, Y. Huang, and C. M. Lieber, "Nonvolatile memory and programmable logic from molecule-gated nanowires," *Nano Letters*, vol. 2, pp. 487-490, 2002.

[35] Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science*, vol. 302, pp. 1543-1545, 2003.

[36] R. A. Wolkow, "Toward hybrid devices," *Chemical & Engineering News*, vol. 79, pp. 228-228, 2001.

[37] K. M. Roth, N. Dontha, R. B. Dabke, D. T. Gryko, C. Clausen, J. S. Lindsey, D. F. Bocian, and W. G. Kuhr, "Molecular approach toward information storage based on the redox properties of porphyrins in self-assembled monolayers," *Journal of Vacuum Science & Technology B*, vol. 18, pp. 2359-2364, 2000.

[38] Q. L. Li, G. Mathur, M. Homsi, S. Surthi, V. Misra, V. Malinovskii, K. H. Schweikart, L. H. Yu, J. S. Lindsey, Z. M. Liu, R. B. Dabke, A. Yasseri, D. F. Bocian, and W. G. Kuhr, "Capacitance and conductance characterization of ferrocene-containing self-assembled monolayers on silicon surfaces for memory applications," *Appl Phys Lett*, vol. 81, pp. 1494-1496, 2002.

[39] W. G. Kuhr, A. R. Gallo, R. W. Manning, and C. W. Rhodine, "Molecular memories based on a CMOS platform," *Mrs Bulletin*, vol. 29, pp. 838-842, 2004.

[40] S. Gowda, G. Mathur, Q. Li, S. Surthi, and V. Misra, "Hybrid Silicon/Molecular FETs: A Study of the Interaction of Redox-Active Molecules With Silicon MOSFETs," *Nanotechnology, IEEE Transactions on*, vol. 5, pp. 258, 2006.

2 MATERIALS AND METHODS

2.1 Structure and Properties of Molecules

This research involves studies with several metallo-organic molecules that are redox-active and can attach to diverse set of surfaces including metals (e.g. Gold), semiconductors (e.g. silicon, TiO_2) and insulators (e.g. SiO_2, HfO_2) [1-8]. A redox-active molecule exhibits stable and reversible oxidation (lose an electron) and reduction (gain an electron) processes. Redox-active molecules can have cationic-accessible states, anionic-accessible states or both. A molecule is said to have cationic-accessible state if it can oxidize and become positively-charged. Anionic-accessible molecules can reduce and become negatively-charged. The molecules utilized in this research have cationic-accessible states [9]. The generic design of the molecules includes redox-active unit, a tether and a surface attachment group (linker). Charge in the molecule is stored in the distinct redox-states contained in the redox-active unit. The surface attachment group serves as mechanical role in linking (covalently) the molecule to the surface and an electronic role in providing communication between the surface and the redox-active unit. The tether connects the charge-storage unit to the linker and typically provides for an insulating barrier.

The redox-active unit of the molecule has discrete energy states which are accessible under fairly-low, well separated and quantized voltages. The guiding factors for the design of the redox-active unit are charge density (depends on molecule size and orientation), molecule-to-molecule charge isolation, stability of the molecule under thermal and electrical stress. Multiple energy states can be built into the redox-active unit. Fig. 2.1 shows chemical structure of the redox-active molecules. The most commonly used molecules in this study are ferrocenes (Fig. 2.1 molecule **1**) and metalloporphyrins (Fig. 2.1 molecule **2**). Ferrocene is the chemical compound with the formula $Fe(C_5H_5)_2$. Ferrocene is the prototypical metallocene, a type of metallo-organic chemical compound consisting of two cyclopentadienyl rings bound on opposite sides of a central metal atom. Such metallo-organic compounds are also known as sandwich compounds [10]. Ferrocene has single cationic-accessible stable and hence demonstrates two states: neutral and monopositive. Both ferrocene and ferrocenium ion (oxidized state) are very stable in air. Ferrocene can be

derivatized with different functional groups to attach to various surfaces [11-13]. The stable and reversible redox-active property of ferrocene makes it an attractive candidate molecule for information storage applications.

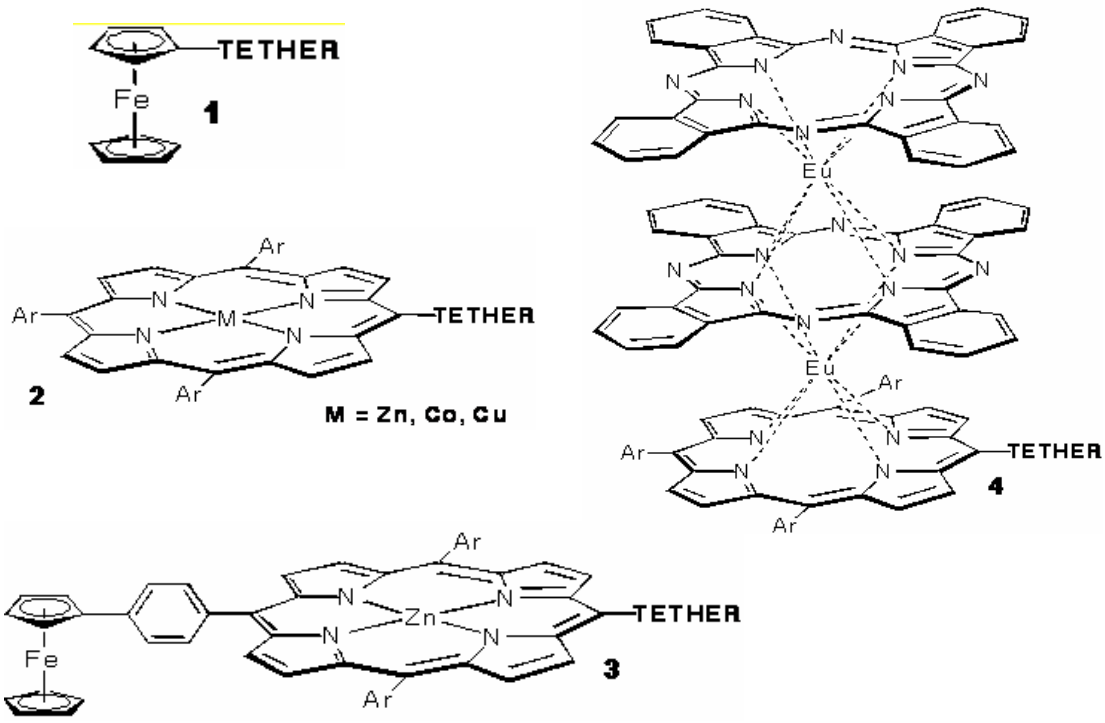


Figure 2.1 Structure of redox-active molecules. These can be derivatized with different tethers and linkers to attach to different surfaces. Molecule **1** is ferrocene, **2** is metalloporphyrin, **3** is ferrocene-porphyrin conjugate and **4** is triple decker porphyrin.

A porphyrin is a heterocyclic macrocycle made from 4 pyrrole subunits linked through 4 methine bridges. It is an aromatic compound that readily combines with metal atoms, coordinating them in the central cavity. Metal containing porphyrins are called metalloporphyrins and zinc (Zn) containing porphyrins are used in this study [14]. Zn-porphyrin has two cationic-accessible states and hence exhibits three states: neutral, monopositive and dipositive. Ferrocene-porphyrin conjugate (Fig. 2.1 molecule 3) and triple decker porphyrin (Fig. 2.1 molecule 4) have three and four cationic oxidation states, respectively [3, 6]. There are molecules with more elaborate structure that can afford up to eight cationic oxidation states at room temperature [4].

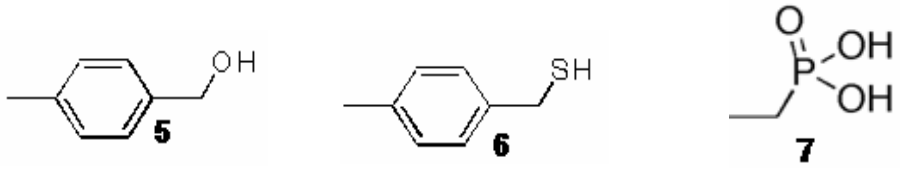


Figure 2.2 Structure of tethers and linkers. Compound **5** is benzyl alcohol and has alchohol linker for attachment to Si. Compound **6** is benzyl thiol and has thiol linker for attachment to gold surface. Compound **7** is phosphonate linker for attachment to SiO_2 surface.

Fig. 2.2 shows structure of a sample set of tethers and linkers used in this study. The linkers are designed to be surface-specific although some of them may be capable of covalently linking with wide variety of substrate material. Charging/discharging endurance and physical stability of the molecule linkage to the substrate are the key factors that govern the design of tether and linker. It is critical that the chemical linkage between the molecule and the substrate surface is robust and well-controlled (predictable) in order to achieve reproducible and highly-ordered molecular assemblies over large areas. The important performance parameters of the molecule such as molecule-to-substrate charge transfer rate, intrinsic charge-retention of the molecules and charge-access (redox) voltages can be tuned by systematic tether design [3, 12]. The most commonly used tethers and linkers in this study are benzyl alcohol (Fig. 2.2 compound **5**) and phosphonate (Fig. 2.2 compound **7**). The former compound is used for attachment to Si via –O-Si covalent linkage and the latter is typically used for attachment to SiO_2 surfaces –P-O-Si linkage [12, 13, 15].

The ferrocene and porphyrins functionalized with appropriate tethers and linkers have been shown to form densely-packed monolayers on Si, Au and SiO_2 surfaces with low-defect densities [11-14]. Some of the key demonstrated properties of these molecules are:

1. **Charge density:** The typical electrically extracted monolayer coverages (number of molecules/cm^2) for two-state ferrocene and three-state porphyrin monolayers on silicon are 2×10^{14} and 0.45×10^{14}, respectively [12]. These numbers are around an order of magnitude higher than the charge density achievable with conventional silicon capacitors [16]. Also, porphyrin polymer films can achieve surface coverages 50-fold greater than those of saturation-coverage porphyrins monolayers [1].

2. **Charge retention:** The intrinsic charge retention times for ferrocene and porphyrin on silicon are typically >100 seconds [12]. Hence, the intrinsic charge retention time of the

redox-active molecules far exceed that of the current CMOS DRAM memory (~ 64 ms), making the molecules attractive candidate for DRAM applications. However, the charge retention of the molecules falls short of meeting the requirements for nonvolatile memories, which is > 10 years. Hence, it is necessary to investigate approaches to enhance the retention by introducing additional or external barriers to prevent stored charge leakage.

3. **Thermal stability:** Porphyrin molecules assembled on Si are stable under high temperatures (~ 450 ^{o}C) for extended periods (~ 2 hours) during processing and also can survive moderate temperatures (~ 140 ^{o}C) during cell operation [9]. Ferrocene molecules may not have the same kind of thermal stability as their thermal decomposition temperature is expected to be less than 400 ^{o}C.

4. **Endurance:** Porphyrin molecules assembled on Si does not degrade under large numbers of write/erase cycles (10^{12}) in an inert atmosphere [9].

This section provided a brief overview of sample set of molecular components that are available and used in this research. Further details of the molecular components including their design and synthesis can be found be in the references listed. The next section lists the exact molecules (redox-active units functionalized with tethers and linkers) used in the study.

2.2 Process Flow for Fabrication of Devices

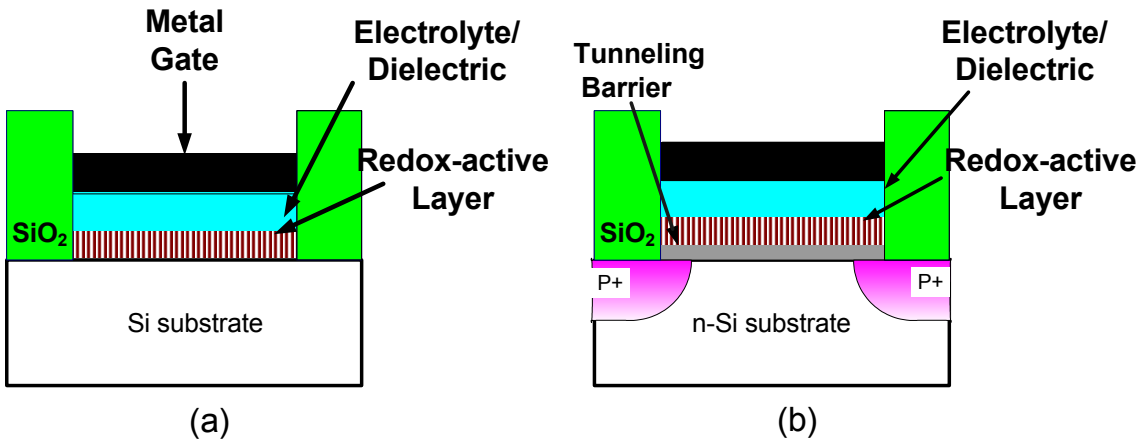


Figure 2.3 Schematic of hybrid silicon-molecular devices: **(a)** MoleDRAM (or Electrolyte-Molecule-Silicon) capacitor. **(b)** Hybrid silicon-molecular FET (MoleFET).

Fig. 2.3 shows the schematic of the hybrid silicon-molecular devices. The hybrid silicon-molecular or electrolyte-molecule-silicon (EMS) capacitor is the storage capacitor for the MoleDRAM memory device. The EMS capacitor also serves to act as an indispensable characterization tool in understanding the redox properties of the molecules particularly in the context of the MoleFET device. An EMOS (tunnel oxide between molecule and silicon) capacitor is also an essential characterization aid to the same extent. The redox-active layer in the Fig. 2.3 can be a self-assembled monolayer or an in-situ polymerized (multilayer) film. In a future molecule-only implementation the tunneling barrier and electrolyte components could be built into the redox-active molecular layer. However, in this study the attempt was to use the experience and technology built on silicon. P-channel enhancement FET device is utilized in this study since the redox-active molecules employed have cationic-accessible states or states that are accessible under negative gate voltages. P-channel enhancement FET is normally OFF with threshold voltage occurring at negative gate voltage.

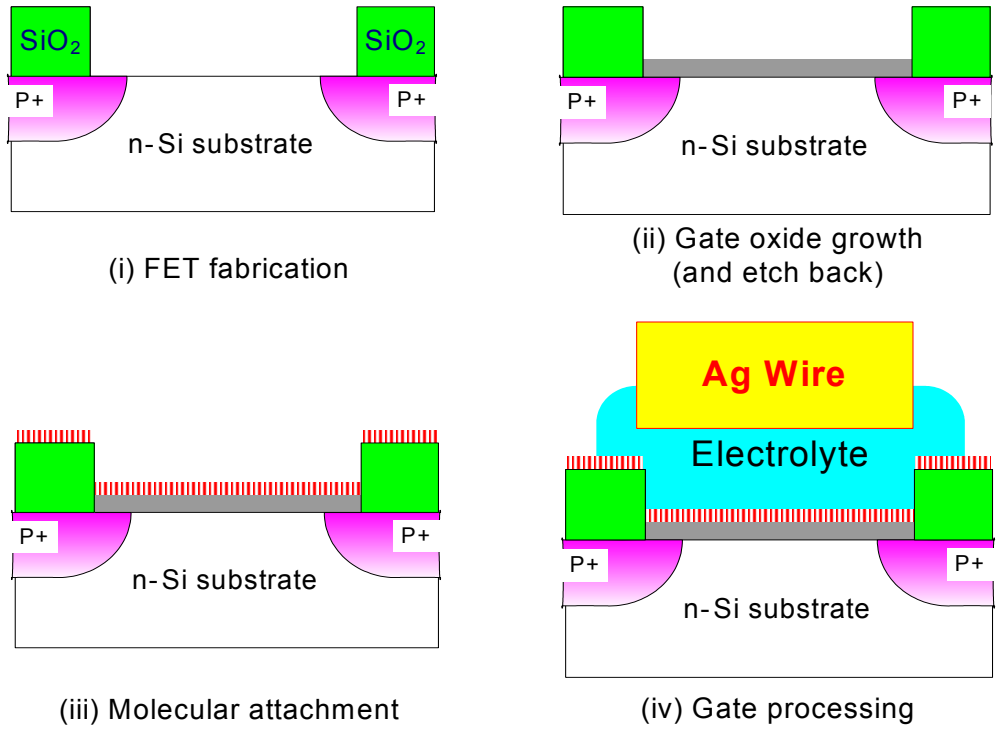


Figure 2.4 Process flow showing the fabrication of the hybrid silicon-molecular FET (MoleFET).

Fig 2.4 lists the steps involved in the process flow for fabrication of the MoleFET device. The process flows for the fabrication of EMS (or EMOS) capacitor is similar to that of

the MoleFET device except the first step and will be highlighted in the following description of the MoleFET process flow:

2.2.1 FET fabrication:

Conventional semiconductor fabrication techniques involving 5 level mask process flow based on replacement gate technology is used to fabricate the silicon FET. A replacement gate process forms the metal gate electrode after the activation of source-drain dopants and is necessary for the MoleFET fabrication since post molecule incorporation steps cannot involve any high temperature (> 450 ^{o}C) processing conditions. The activation of source-drain dopants typically involves temperatures > 800 ^{o}C. The details of FET fabrication steps will be presented in chapter 5. FETs were fabricated with varying gate lengths ranging from 10 to 200 μm. The gate width was identical to the length i.e. W/L = 1 in each case. Since the replacement gate process requires alignment of source-drain regions with respect to the gate, FETs were fabricated with varying source and drain overlap regions ranging from 0 to 5 μm in order to provide tolerance for photolithography alignment errors.

The corresponding initial step in the EMOS (or EMS) capacitor fabrication involves lithographically defining square active areas of varying dimensions ranging from 5x5 to 200x200 μm^2, which were isolated by a thermally grown 400 nm thick field SiO_2. The Si substrates used in this study were (100) oriented, boron (p-type) or phosphorous (n-type) doped, and of varying doping concentrations.

2.2.2 Gate oxide growth and etch-back

In case of the MoleFET device, around 3 nm of gate oxide (SiO_2) was grown using a RTA system with 5% oxygen-in-argon purging flow. The gate oxide, which acts as tunnel barrier to the molecule charging/discharging in the device, was etched back to desired thickness using 1 % hydrofluoric acid (HF). The etch-back (if required) is usually done right before the molecular attachment step. Although the EMS capacitor does not have the tunnel oxide in the final device structure, the gate oxide serves to act as a sacrificial oxide layer to passivate the Si surface and is completely etched off right before the molecular attachment. The 1% HF etch treatment also leaves the Si surface with hydrogen terminations that can be easily replaced by molecules reacting to form covalent linkages with Si.

2.2.3 Molecular attachment:

The redox-active molecules are covalently attached to Si and SiO_2 surfaces by wet chemistry techniques and the attachment process are carried out in inert atmospheres at elevated temperatures.

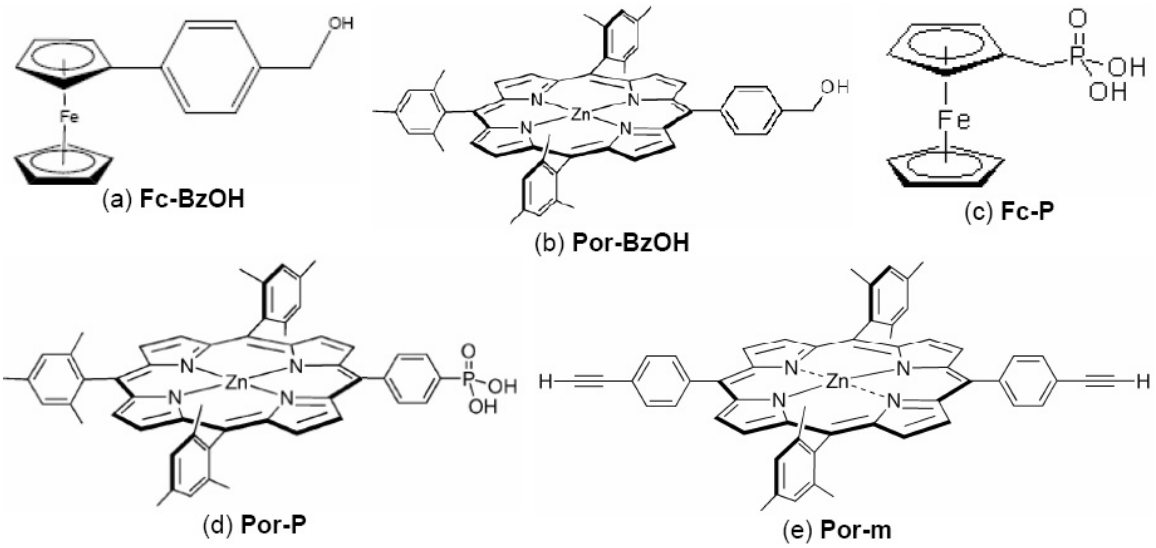


Figure 2.5 Structure of redox-active molecules used in this study: molecules shown in **(a)** and **(b)** attach to Si, **(c)** and **(d)** attachs to SiO_2, and **(e)** forms polymer films on various surfaces.

Fig. 2.5 shows chemical structure of redox-active molecules (redox-active units functionalized with tethers and linkers) used in this study. Zinc-porphyrins are the only kind of porphyrins used in this study and henceforth referred to as porphyrins. **Fc-BzOH** and **Por-BzOH** are ferrocene and porphyrin molecules functionalized with benzyl alcohol for monolayer attachment to Si surfaces. **Fc-P** and **Por-P** are ferrocene and porphyrin molecules functionalized with phosphonate linker for monolayer attachment to SiO_2. Por-m is porphyrin molecule functionalized with acetylene at two ends and forms multilayer films by way of in-situ polymerization on various surfaces [1]. The steps involved in molecular attachment are listed as follows:

I. The desired redox-active compound is dissolved in appropriate solvent to form a solution typically with concentration of 1mM. In case of molecular solution that is used for in-situ polymerization (**Por-m**), the concentration is determined by the target film thickness or number of layers [1]. The solvents used in general are: (i) benzonitrile (BN) or tetrahydrofuran (THF) for molecules with alchohol linker i.e.

Fc-BzOH and **Por-BzOH**, (ii) dimethylformamide (DMF) or THF for molecules with phosphonate linkers i.e. **Fc-P** and **Por-P**, and (iii THF for in-situ polymerization of **Por-m**. THF is generally used when the attachment temperatures are ~ 400 ^{o}C.

II. Substrate samples that are freshly etched using 1 % HF are transferred to sealed, argon-purged environment. The samples remain in inert argon-purged environment throughout the attachment process.

III. The molecular solution is transferred to the attachment surface and the sample is maintained at elevated temperature to provide for activation energy required for formation of covalent bonding between molecules and the surface. There are two techniques to achieve this: (i) drop-coat or (ii) spin-coat. The former technique is a repetitive process (6 times) of placing a small quantity of the solution in the active areas of sample and maintaining the sample at elevated temperature for 5-8 minutes. The temperatures at which the samples are maintained are: (i) 90 ^{o}C for ferrocene molecules i.e. **Fc-BzOH** and **Fc-P** and (ii) 180-200 ^{o}C for porphyrin monolayer attachments i.e. **Por-BzOH** and **Por-P**. The Por-m is typically attached using the spin-coat technique, which involves transferring the molecular solution onto the sample, spinning the sample at low to moderate speeds (~ 300 rpm) and baking the sample at 400 ^{o}C for 2 minutes. Spin-coat technique can also be used in attachment of porphyrin monolayers.

IV. The last step of molecular attachment is ultra-sonic rinse of the samples with dichloromethane (DCM) or THF in order to remove molecules that are not attached to the surface. This is typically repeated three times to ensure complete removal of unattached molecules.

It is essential to note that the conditions stated here for monolayer attachment are the ones optimized for densely-packed monolayers in previous studies [17, 18]. However, monolayer attachment is a self-saturating process and hence, there is a small to moderate tolerance (~ 10 %), which gives flexibility for the attachments conditions such as bake temperatures and times, solution concentration etc. However, the same is not true for in-situ polymerization of **Por-m** and there is significant variation in film thickness even under tightly controlled set of film-forming conditions [1].

In the molecular attachment step, substrates surfaces are exposed to organic solvents under elevated temperatures. This may possibly be damaging to the substrate surfaces and induce interface traps, surface states, etc., especially in Si and SiO_2, thereby impacting the electrical characteristics of the hybrid devices. In order to ensure that any unique electrical characteristics observed can be convincingly attributed to redox-related charging/discharging and circumvent misinterpretation of experimental artifacts, it is essential to perform control experiments alongside actual device fabrication and characterization. The control devices are fabricated incorporating non-redox molecules shown in Figure 2.6.

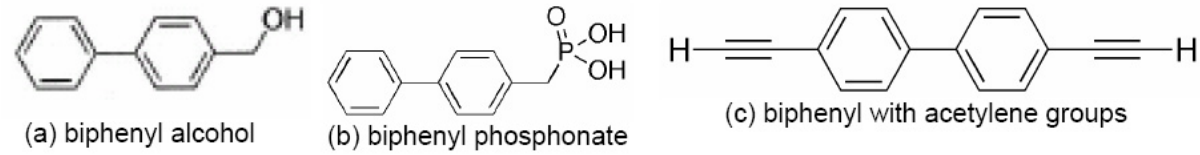


Figure 2.6 Structures of non-redox molecules used for control experiments in this study. **(a)** has alcohol linker for attachment to Si, **(b)** has phosphonate linker for attachment to SiO_2, and **(c)** forms polymer films.

Biphenyl alcohol (Fig. 2.6(a)) and biphenyl phosphonate (Fig. 2.6(b)) serve as control for redox-active molecules attached to Si and SiO_2, respectively. Biphenyl with acetylene groups (Fig. 2.6(c)) forms polymer films on various surfaces and is used as control for redox-active polymer (**Por-m**). A control device is subjected to same processing conditions and has identical structure as the actual test device.

2.2.4 Gate processing:

For test devices, gate consists of a conducting electrolyte deposited on top of the molecular layer and a metal wire dipped in the electrolyte, which serves as a gate electrode. One of the main criteria for selection of a suitable electrolyte is the requirement of the electrolyte to be non-aqueous and chlorine-free. This is because, under electrical stress, moisture can attack the covalent linkage of the molecules with substrate and chlorine can attack the redox-centers in the molecules. The most commonly used electrolyte and metal electrode used in this study are 1M tetrabutyl ammonium hexafluorophosphate (TBA-HPF) in propylene carbonate (PC) and silver wire. The purification of electrolyte to minimize the concentration of unwanted constituents such as moisture, dissolved oxygen etc., and chemical-etch treatment of silver wire are indispensable steps of gate processing.

The liquid electrolyte was used for initial studies towards understanding the intrinsic properties of the redox-active molecules, interaction of redox-state with Si and proof of concept devices. However, for large-scale integration and practical applications, it is necessary to either employ a solid-state gel/polymer electrolyte or replace the electrolyte with equivalent solid-state components. There were attempts made to that extent and some of the details will be discussed in chapter 6.

2.3 Electrical Characterization

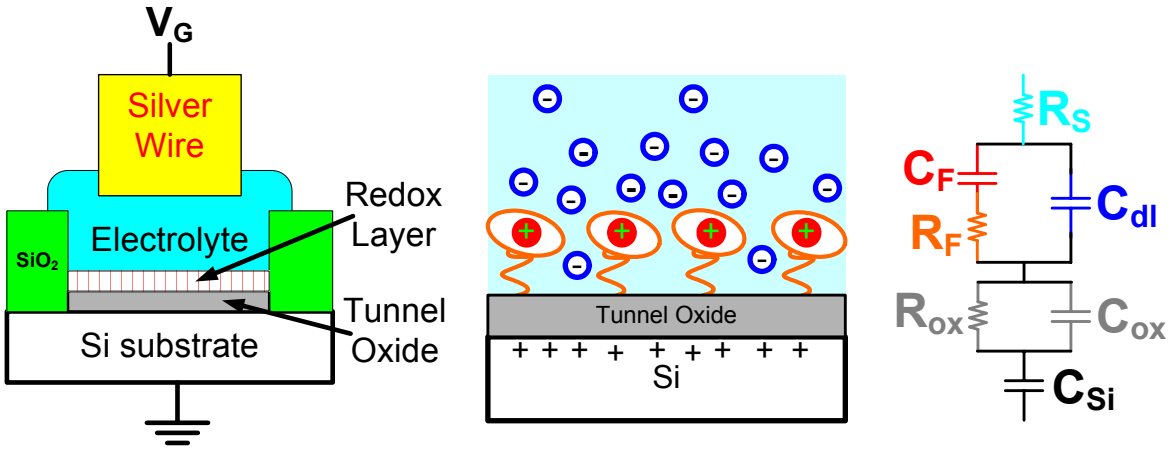


Figure 2.7 (a) Schematic of electrical characterization setup for EMOS capacitor. **(b)** Charges in electrolyte-molecule-oxide-Si half-cell under oxidizing gate bias ($-V_G$). **(c)** Equivalent circuit for EMOS capacitor.

Fig. 2.7 (a) shows the experimental setup for the electrical characterization of EMOS/EMS capacitors. The electrolyte serves three vital roles in the hybrid device: (i) dc-blockage with reasonably high breakdown field at the contact surface, (ii) highly efficient screening of the redox and background charges (gate to molecule coupling capacitance > 10 μF/cm^2) and (iii) charge transfer within the bulk of the electrolyte by ionic conduction. Fig. 2.7 (b) shows the charges at electrolyte-molecule interface and electrolyte-electrode interface when an oxidizing gate voltage is applied. The negative ions, which diffuse towards molecules and electrode surface under the negative bias, screen the positive charges in the molecule (oxidized state) and background charges including positive charges in Si and any interface or bulk charges in the oxide. A detailed discussion about the role of electrolyte will be provided in chapter 6. From the electrochemistry perspective, the EMOS structure shown

in Fig. 2.7 (b) is one-half of the electrochemical cell. Silver wire and electrolyte is the other half of the cell. Since the role of gate-electrode is to supply charges to electrolyte that ultimately results in diffusive layer of counter-ions at the electrolyte-molecule interface, the top half-cell can be electrically modeled as a resistor in series with EMOS half cell. The value of this series resistor can become infinitesimal by appropriate selection of the gate electrode and electrolyte, and purification treatments. Hence, in this study the electrolyte is considered the gate and metal electrode is considered as just a contact to the electrolyte. The electrical equivalent of the EMOS capacitor is given as shown in Fig 2.7 (c). $\mathbf{R_s}$ is the gate series resistance, $\mathbf{C_F}$ is the redox-related (faradaic) molecule capacitance, $\mathbf{R_F}$ is the faradaic molecule resistance associated with tunneling resistance of the molecule tether-linker, $\mathbf{C_{dl}}$ is electrolyte double-layer capacitance, $\mathbf{C_{ox}}$ and $\mathbf{R_{ox}}$ are the capacitance and resistance components of the tunnel oxide, and $\mathbf{C_{Si}}$ is the Si capacitance.

The electrical characterization techniques employed in this research are: (i) cyclic voltammetry (CyV), (ii) impedance spectroscopy (CV-GV), (iii) charge-retention measurements, and (iv) conventional MOSFET characterization techniques. The last one is primarily for the electrical characterization of the MoleFET device.

2.3.1 Cyclic Voltammetry (CyV)

CyV is a DC current-voltage (IV) characterization technique, wherein the gate voltage is ramped at constant rate in negative direction (oxidizing scan) and back (reducing scan) as shown in Fig. 2.8 (a) and the resulting displacement gate current is measured [19, 20]. Fig. 2.8 (c) shows a representative CyV curve of an EMOS capacitor. The peaks observed in the measured current are associated with the oxidation (red curve in negative current axis) and the reduction (green curve in positive current axis) of the molecules. When an oxidizing gate voltage is applied (negative $\mathbf{V_G}$ ramp indicated by red line in Fig. 2.8 (a)), each molecule loses an electron which tunnels into Si substrate across the tunnel barrier (molecule tether-linker and tunnel oxide) leaving the molecular layer positively charged. This is the written state of the cell. On application of the reducing voltage (reverse scan), electron tunnels back into each molecule thereby returning the molecular layer to neutral state as shown in Fig. 2.8 (b). This is the erased state of the cell.

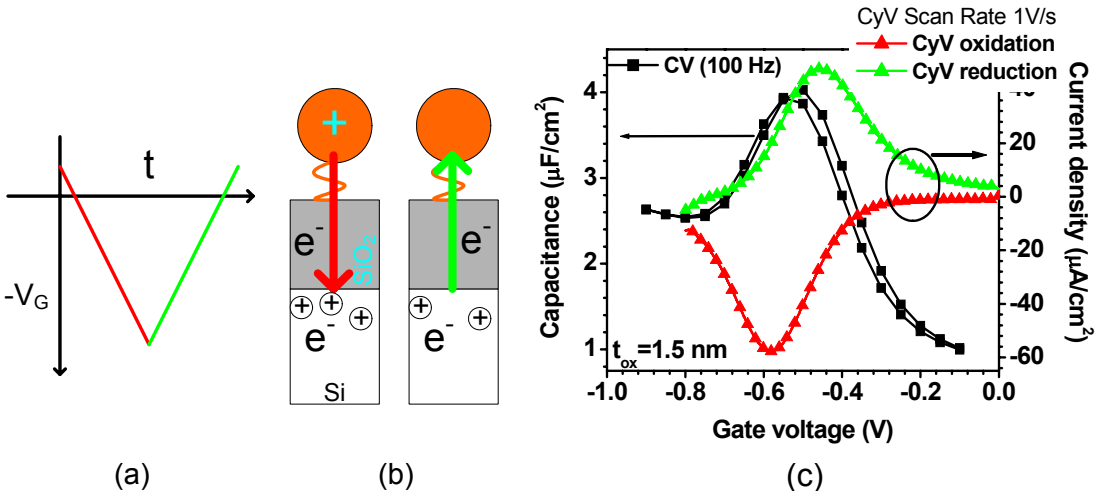


Figure 2.8 (a) Cyclic voltammetry voltage vs. time relationship. (b) Schematic showing direction of electron movement during oxidation and reduction and the resulting charge on the molecule at the end of each process. (c) Representative cyclic voltammetry (CyV) and capacitance voltage (CV) curves of an EMOS capacitor. The molecule used is **Fc-P** and tunnel oxide thickness ($\mathbf{t_{ox}}$) is 1.5 nm.

The key parameters of the CyV technique are: (i) scan rate ($d\mathbf{V_G}/d\mathbf{t}$), and (ii) scan voltage range (start, end $\mathbf{V_G}$). The information provided by the CyV measurements on molecular charge storage and the interpretation of the same in terms of the performance parameters of the memory cell are as follows:

I. The charge density (C/cm^2) associated with the faradaic (redox) process can be determined from the area under the oxidation or reduction peak. The molecular layer coverage or number of molecules per unit area can be estimated from the charge density considering each molecule loses an electron.

II. The peak current (I_p) vs. measurement scan rate has linear relationship with redox-active molecules that are surface immobilized and square-root dependence for molecules dissolved in solution. The linearity of I_p w.r.t scan rate is true for reversible or Nerstian immobilized redox systems.

III. The oxidation and reduction peak voltages (V_{OX} and V_{RED}) determine the write and erase voltages, respectively for both DRAM and Flash memory cells. The reduction peak voltage also corresponds to the read voltage for MoleDRAM memory cell, and the separation between oxidation and reduction peaks determines the non-destructive read window for MoleFET memory cell.

IV. The separation (ΔV_P) between the peak potentials V_{OX} and V_{RED}, along with half-peak width (h_{PW}), provides information about molecules to substrate charge transfer rates. ΔV_P and h_{PW} are monitored as function of the measurement scan rate to kinetic rate constants for molecular charging and discharging, which correspond to write/erase speeds of the memory cell. Also, the redox systems are classified as reversible (Nerstian) or quasi-reversible based on ΔV_P and h_{PW} from the electrochemistry perspective [19]. This aspect influences the selection of suitable electrochemical model for charge-transfer kinetics and will be discussed in chapter 3.

V. The background current (non-faradaic) in CyV is typically associated with charging current of the electrolyte double layer capacitance ($\mathbf{C_{dl}}$). Also, the background current can sometimes provide information about the electrode surface, like an increasing background current at higher $\mathbf{V_G}$ is usually indicative of the irreversible oxidation of the substrate surface.

CyV is the most extensive used characterization technique in this study and further details of the technique and the theory will be presented in chapter 3. All CyV measurements in this study were done using a CHI 600A electrochemical analyzer.

2.3.2 Impedance Spectroscopy (CV-GV)

This is an AC measurement technique to study the frequency dependence of redox charging/discharging in the molecules. It involves extraction of the capacitance-voltage (CV) and conductance-voltage (GV) curves assuming either a parallel or series connection circuit model of a capacitance connected with parallel conductance or series resistance [21]. Peaks associated with charging and discharging of the redox states are observed in the CV [22]. Fig. 2.8 (c) shows a representative CV plot (black curve) for an EMOS capacitor. The faradaic capacitance ($\mathbf{C_F}$) and electrolyte double-layer capacitance ($\mathbf{C_{dl}}$) can be estimated from low-frequency CV analyses of a EMS capacitor ($\mathbf{t_{ox}} \rightarrow 0$, $\mathbf{C_{ox}} \rightarrow \infty$). From the EMOS equivalent circuit (Fig. 2.7 (c)), it is known that the parallel combination of $\mathbf{C_F}$ and $\mathbf{C_{dl}}$ appears in series with $\mathbf{C_{ox}}$ and $\mathbf{C_{Si}}$. Hence, for an EMS capacitor, $\mathbf{C_F}$ and $\mathbf{C_{dl}}$ can estimated in region of gate bias when $\mathbf{C_{Si}} \rightarrow \infty$, which is the case for p-type Si under $-\mathbf{V_G}$ or accumulation of the Si surface. The accumulation capacitance of an EMS capacitor

corresponds to $\mathbf{C_{dl}}$ and $\mathbf{C_F}$ is a voltage dependent capacitor which is accessible around the redox peak potentials.

CV used in this study is a quasi-static measurement technique where a frequency dependent AC small-signal is superimposed on a DC gate bias ($\mathbf{V_G}$), which is ramped at a very slow rate. A hold time is introduced at each $\mathbf{V_G}$ step to ensure the device is equilibrated so as to circumvent any transient effects that may cause error in the measurements. Capacitance value is calculated from the device impedance (both magnitude and phase) measured at each $\mathbf{V_G}$ step using the selected equivalent circuit model (parallel or series). The key parameters of the CV technique are: (i) small-signal frequency, (ii) small-signal amplitude, and (iii) DC-voltage range.

The study of dependence of CV characteristics of EMOS capacitor on small-signal frequency and amplitude gives an indication about the intrinsic redox charge-transfer rates of the molecules and the ion migration rate in the electrolyte [23]. Since the redox charge-transfer rates are reasonably high, the ion migration rate is the rate-limiting factor in most cases. A more extensive study of the redox properties using CV-GV can be found in another student's dissertation [24]. The CV-GV measurements in the current study were done using an HP 4284A LCR meter.

2.3.3 MoleFET Characterization

The hybrid silicon-molecular (MoleFET) devices were characterized using conventional MOSFET IV measurements along with CyV and CV-GV techniques. An HP 4155B semiconductor parameter analyzer was used to obtain I_D-V_G, I_D-V_D and I_G-V_G characteristics of the MoleFET device. The threshold voltage (V_T) of the device was extracted from the I_D-V_G characteristics using linear extrapolation method [25]. Further details of the experimental setup and analyses will be provided in chapter 5.

2.3.4 Charge Retention Measurements:

Data retention of the memory devices is one of the most important parameters that need to be quantized. As discussed previously, the current CMOS DRAM devices have data retention of ~ 64 ms and hence the data has to continuous refreshed making it a power-hungry device. The MoleDRAM device has significantly gains over the current DRAM in this

aspect as the retention is at least couple of orders higher in magnitude. Since the timescale involved for loss of charge is significantly small, it is necessary to use pulse IV techniques to accurately quantify the charge retention in MoleDRAM capacitor (EMS) devices. One such technique is Open Circuit Potential Amperometry (OCPA). However, the Flash memory devices have requirement of > 10 years data retention and the timescale for loss of charge is relatively large. Hence, charge retention measurements can be done on the EMOS test structure or MoleFET device using modified CyV or MOSFET-IV techniques.

The two techniques mentioned above are described as follows:

I. OCPA: This is a pulse technique developed by Roth et. al. at University of California, Riverside (UCR) and is described in [11]. The technique involves determination of the OCP of the electrochemical cell (EMS capacitor), which serves as read voltage. Reading the cell at OCP presents a method to completely discriminate the faradaic (redox) current from the background current on a fast timescale. Hence, the OCPA method is able to quantify charge and subsequently the charge-retention associated with the redox of the molecules without any interference from background charge such as charges from the electrolyte double layer. In this technique, a write pulse voltage of appropriate width is applied across the EMS (EMOS) capacitor to oxidize the redox-active layer and after a wait time during which the device is open-circuited, remaining oxidized charge is read at OCP by using an in-house built high-bandwidth current monitor. This process is repeated for varying wait times and a plot of log (charge) vs wait time is generated. The slope of the plot gives the charge-retention half-life ($\boldsymbol{t}_{1/2}$) and the intercept yields the total faradaic charge ($\mathbf{Q}_0$) written in the device. The charge-retention time of these devices is characterized by $\boldsymbol{t}_{1/2}$, which is defined as the time taken by the faradaic charge to decay to half the initial value ($\mathbf{Q}_0$).

II. Modified CyV/IV technique: In devices where the oxidation and reduction processes occur at non-overlapping voltages i.e. ΔV_P > width of the oxidation/reduction peak at its base, it is possible to used a variation of CyV technique to measure the charge retention times. One such device is the EMOS capacitor where oxidation and reduction are completely separated from each other for $\mathbf{t_{ox}}$ beyond a certain value. In this technique, an oxidizing CyV scan is used to

write the hybrid capacitor. The charge is read after a wait time by using a reducing CyV scan (or a second oxidizing scan). The amount of charge retained in the capacitor after the wait time is given by integrating the current peak w.r.t time in the reducing scan (or difference of the total written charge and charge obtained during the second oxidizing scan). This technique is elaborated in [26]. Similarly in MoleFET devices, charge retention measurements are done using a variation of the conventional MOSFET IV characterization techniques since the timescales involved is significantly larger than those for the MoleDRAM devices.

2.4 References

[1] Z. M. Liu, I. Schmidt, P. Thamyongkit, R. S. Loewe, D. Syomin, J. R. Diers, Q. Zhao, V. Misra, J. S. Lindsey, and D. F. Bocian, "Synthesis and film-forming properties of ethynylporphyrins," *Chemistry of Materials*, vol. 17, pp. 3728-3742, 2005.

[2] L. Y. Wei, K. Padmaja, W. J. Youngblood, A. B. Lysenko, J. S. Lindsey, and D. F. Bocian, "Diverse redox-active molecules bearing identical thiol-terminated tripodal tethers for studies of molecular information storage," *Journal of Organic Chemistry*, vol. 69, pp. 1461-1469, 2004.

[3] A. Balakumar, A. B. Lysenko, C. Carcel, V. L. Malinovskii, D. T. Gryko, K. H. Schweikart, R. S. Loewe, A. A. Yasseri, Z. M. Liu, D. F. Bocian, and J. S. Lindsey, "Diverse redox-active molecules bearing O-, S-, or Se-terminated tethers for attachment to silicon in studies of molecular information storage," *Journal of Organic Chemistry*, vol. 69, pp. 1435-1443, 2004.

[4] D. Gryko, J. Z. Li, J. R. Diers, K. M. Roth, D. F. Bocian, W. G. Kuhr, and J. S. Lindsey, "Studies related to the design and synthesis of a molecular octal counter," *Journal of Materials Chemistry*, vol. 11, pp. 1162-1180, 2001.

[5] D. T. Gryko, C. Clausen, K. M. Roth, N. Dontha, D. F. Bocian, W. G. Kuhr, and J. S. Lindsey, "Synthesis of "porphyrin-linker-thiol" molecules with diverse linkers for studies of molecular-based information storage," *Journal of Organic Chemistry*, vol. 65, pp. 7345-7355, 2000.

[6] D. T. Gryko, F. Zhao, A. A. Yasseri, K. M. Roth, D. F. Bocian, W. G. Kuhr, and J. S. Lindsey, "Synthesis of thiol-derivatized ferrocene-porphyrins for studies of multibit information storage," *Journal of Organic Chemistry*, vol. 65, pp. 7356-7362, 2000.

[7] K. Muthukumaran, R. S. Loewe, A. Ambroise, S. I. Tamaru, Q. L. Li, G. Mathur, D. F. Bocian, V. Misra, and J. S. Lindsey, "Porphyrins bearing arylphosphonic acid tethers for attachment to oxide surfaces," *J Org Chem*, vol. 69, pp. 1444-1452, 2004.

[8] R. S. Loewe, A. Ambroise, K. Muthukumaran, K. Padmaja, A. B. Lysenko, G. Mathur, Q. L. Li, D. F. Bocian, V. Misra, and J. S. Lindsey, "Porphyrins bearing mono or tripodal benzylphosphonic acid tethers for attachment to oxide surfaces," *J Org Chem*, vol. 69, pp. 1453-1460, 2004.

[9] Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science*, vol. 302, pp. 1543-1545, 2003.

[10] R. Dagani, "Fifty years of ferrocene chemistry," *Chemical & Engineering News*, vol. 79, pp. 37-38, 2001.

[11] K. M. Roth, J. S. Lindsey, D. F. Bocian, and W. G. Kuhr, "Characterization of charge storage in redox-active self-assembled monolayers," *Langmuir*, vol. 18, pp. 4030-4040, 2002.

[12] K. M. Roth, A. A. Yasseri, Z. M. Liu, R. B. Dabke, V. Malinovskii, K. H. Schweikart, L. H. Yu, H. Tiznado, F. Zaera, J. S. Lindsey, W. G. Kuhr, and D. F. Bocian, "Measurements of electron-transfer rates of charge-storage molecular monolayers on Si(100). Toward hybrid molecular/semiconductor information storage devices," *Journal of the American Chemical Society*, vol. 125, pp. 505-517, 2003.

[13] Q. L. Li, S. Surthi, G. Mathur, S. Gowda, V. Misra, T. A. Sorenson, R. C. Tenent, W. G. Kuhr, S. Tamaru, J. S. Lindsey, Z. M. Liu, and D. F. Bocian, "Electrical characterization of redox-active molecular monolayers on SiO2 for memory applications," *Applied Physics Letters*, vol. 83, pp. 198-200, 2003.

[14] K. M. Roth, D. T. Gryko, C. Clausen, J. Z. Li, J. S. Lindsey, W. G. Kuhr, and D. F. Bocian, "Comparison of electron-transfer and charge-retention characteristics of porphyrin-containing self-assembled monolayers designed for molecular information storage," *Journal of Physical Chemistry B*, vol. 106, pp. 8639-8648, 2002.

[15] Q. L. Li, S. Surthi, G. Mathur, S. Gowda, Q. Zhao, T. A. Sorenson, R. C. Tenent, K. Muthukumaran, J. S. Lindsey, and V. Misra, "Multiple-bit storage properties of porphyrin monolayers on SiO2," *Applied Physics Letters*, vol. 85, pp. 1829-1831, 2004.

[16] W. G. Kuhr, A. R. Gallo, R. W. Manning, and C. W. Rhodine, "Molecular memories based on a CMOS platform," *Mrs Bulletin*, vol. 29, pp. 838-842, 2004.

[17] Q. Li, "Approach towards Hybrid Silicon/Molecular Electronics for Memory Applications," in *Electrical and Computer Engineering*. Raleigh, NC: North Carolina State University, 2004, pp. 152.

[18] G. Mathur, "Redox-Active Organic Molecules on Silicon and Silicon Dioxide Surfaces for Hybrid Silicon-Molecular Memory Devices," in *Electrical and Computer Engineering*. Raleigh, NC: North Carolina State University, 2005, pp. 23-24.

[19] A. M. Bond, *Broadening Electrochemical Horizons: Principles and Illustration of Voltammetric and Related Techniques*: Oxford University Press, 2002.

[20] A. J. Bard and L. R. Faulkner, "Potential Sweep Methods," in *Electrochemical Methods: Fundamentals and Applications*, 2nd ed: John Wiley & Sons, Inc., 2001, pp. 226-260.

[21] D. K. Schroder, in *Semiconductor Material and Device Characterization*, 2nd ed. New York, 1998, pp. 88-90,116-117.

[22] Q. L. Li, G. Mathur, M. Homsi, S. Surthi, V. Misra, V. Malinovskii, K. H. Schweikart, L. H. Yu, J. S. Lindsey, Z. M. Liu, R. B. Dabke, A. Yasseri, D. F. Bocian, and W. G. Kuhr, "Capacitance and conductance characterization of ferrocene-containing self-assembled monolayers on silicon surfaces for memory applications," *Appl Phys Lett*, vol. 81, pp. 1494-1496, 2002.

[23] G. Mathur, S. Gowda, L. Qiliang, S. Surthi, S. Tamaru, J. Lindsey, and V. Misra, "Hybrid CMOS/molecular memories using redox-active self-assembled monolayers," *Proceedings of Nanotechnology, 2005. 5th IEEE Conference on*, vol. 1, pp. 307, 2003.

[24] G. Mathur, "Redox-Active Organic Molecules on Silicon and Silicon Dioxide Surfaces for Hybrid Silicon-Molecular Memory Devices," in *Electrical and Computer Engineering*. Raleigh, NC: North Carolina State University, 2005.

[25] D. K. Schroder, "Threshold Voltage," in *Semiconductor Material and Device Characterization*, 2nd ed. New York, 1998, pp. 242-244.

[26] G. Mathur, S. Gowda, Q. L. Li, S. Surthi, Q. Zhao, and V. Misra, "Properties of functionalized redox-active monolayers on thin silicon dioxide - A study of the. dependence of retention time on oxide thickness," *Ieee Transactions on Nanotechnology*, vol. 4, pp. 278-283, 2005.

3 MOLECULES ON SILICON AND OXIDES

3.1 Introduction

The design and implementation of hybrid silicon-molecular devices requires fundamental understanding of the behavior of the redox-energy states in the molecules on the various parameters of silicon substrate such as doping type and density, and also on the silicon-molecule energy barrier.

The biggest challenge in the field of molecular electronics is to model the electronic coupling between the molecule and silicon [1]. This is because molecules have orbitals which are discrete quantum states for electrons in the molecules and are spatially localized, whereas in Si the atomic orbitals form extended energy bands. Hence, it is difficult to adequately predict how the molecular orbitals' energy levels will align with the Fermi energy of the Si electrode. In this chapter, experimental results and discussions are presented towards modeling of the silicon-molecule electronic coupling. This study involves understanding of the effect of Si doping type and density on redox voltages and kinetics and charge retention characteristics of the molecules. An unpublished manuscript entitled "Experimental study and modeling of the effect of silicon substrate doping type and density on the write/erase voltages and speeds in hybrid silicon-molecular memory devices." is included as part of the discussion on the aspect of exploring the electronic models for silicon-molecule interface.

The energy barrier between molecule and silicon will impact the critical cell parameters of the hybrid silicon-molecular memory devices. The design of this barrier will be guided by trade-off arising out of write/erase speed vs. data retention requirements. As discussed in the previous chapter the MoleDRAM device has stringent requirements on the write/erase speeds while the MoleFET (Flash) needs to meet the nonvolatile retention specifications. The energy barrier has primarily two components: (i) intrinsic to molecules provided by the tether-linker of the molecule, and (ii) extrinsic tunnel barrier provided by insulating oxides such as SiO_2, HfO_2 etc. on the Si surface. The former component will be adequate to meet the specifications for MoleDRAM. However, latter component will have to be explored and engineered in order to fulfill the criterion for non-volatile memory

specifications. The later part of this chapter involves studies on properties of redox-active molecules on ultra-thin single dielectric layer and bilayer tunnel barriers. A paper entitled "Engineering the Tunnel Barrier in Hybrid Silicon-Molecules Devices" is included that contains discussion on impact of the tunnel oxide thickness, oxide barrier height, and dielectric permittivity on the performance parameters of the memory cell. Also a proposal to engineer the tunnel barriers to enhance the speed vs. retention performance by employing layered tunnel barriers is presented.

The next section details electrochemical theory of cyclic voltammetry to model the molecule-to-Si charge-transfer kinetics.

3.2 Theory of Cyclic Voltammetry [2, 3]

The cyclic voltammogram for a simple oxidative electron-transfer process when the reduced/neutral (*A*) and oxidized/positive (*B*) forms of the redox-active species are immobilized on an electrode surface,

$$A \overset{E_0, k_0, \alpha}{\Leftrightarrow} B^+ + e^- \tag{1}$$

can be described in terms of three parameters: (i) E_0, the reversible formal potential or intrinsic redox potential (voltage referenced to the electrode on which the redox-active species is immobilized, though in electrochemistry it is referenced to the top electrode). (ii) k_0, the charge-transfer rate constant (s^{-1}) measured at E_0. The value of k_0 determines how far the redox peak potentials (V_{OX} and V_{RED}) are removed from E_0 at a particular scan rate. (iii) α, the charge-transfer coefficient (dimensionless parameter). α predominantly affects the shape and not the position of the voltammetric response and, typically, it has a value of 0.5.

The relationship between the three parameters mentioned above, the applied gate voltage (V_G) and the current may be represented by the Butler-Volmer equation:

$$I = -qA_D k_0 \left(\Gamma_{RED} \exp\left[(\alpha - 1)(V_G - E_0)q / k_B T\right] + \Gamma_{OX} \exp\left[(\alpha)(V_G - E_0)q / k_B T\right]\right) \tag{2}$$

where A_D is the electrode area and k_BT/q is the thermal voltage at temperature T. The symbol Γ_{RED} denotes the fraction of the surface coverage of the reduced form of the compound i.e., the neutral state represented by *A* in equation (1), and Γ_{OX} represents the fraction of oxidized form of the compound i.e., the ionized state *B*. The equations presented in this discussion have been modified to suit the normal convention in field of solid-state electronics. Hence, the voltage and current polarities might be reversed as compared to identical equations in electrochemistry textbooks such as [2].

In the case of fast electron-transfer kinetics, the current equation can be simplified by using Nernst equation as discussed below. The molecule-electrode systems can be categorized into three groups based on the relative rates of the molecule-to-electrode electron transfer and the cyclic voltammetry (CyV) scan rate: (i) reversible, (ii) irreversible, and (iii) quasi-reversible [2].

3.2.1 Reversible Process

The extent of electrochemical reversibility of a process is related to the kinetics of the electron transfer at the electrode system. For a fast electron transfer reaction, equilibrium is achieved rapidly and the system is defined as being electrochemically reversible. In other words, both the forward and reverse electron-transfer reaction steps are rapid. This is true in case of EMS capacitors. Under conditions of electrochemical reversibility, the Nernst equation

$$V_G = E_0 - \frac{k_B T}{q} \ln\left\{\frac{\Gamma_{OX}}{\Gamma_{RED}}\right\} \tag{3}$$

applies for the process described in equation (1). The timescale of the CyV experiment is also a determining factor for process to be described as electrochemically reversible. Thus, an electron-transfer process may be termed reversible at CyV scan rate of 50 mV/s, but irreversible or quasi-reversible at a higher scan rate, say 100 V/s. In the process described by equation (1) the ion that must be transported in the electrolyte to provide for screening of the charge in the oxidized molecule is omitted for sake of simplicity, even though this ion transport rather than the molecule-to-electrode electron-transfer may be rate-determining in the process. Hence, for CyV measurements at high scan rates

(> 100 V/s) the system may appear to be quasi-reversible in spite of electron-transfer being facile, which is the case for EMS capacitors in this study.

For a CyV experiment, the equilibrium current is given by the rate of change of the redox state of the redox centers:

$$I = qA_D \frac{d\Gamma_{RED}}{dt} = -qA_D \frac{d\Gamma_{OX}}{dt} \tag{4}$$

where A_D is the area of the device. Combining the equations (3), (4) and the relationship for the total surface coverage

$$\Gamma_{MOL} = \Gamma_{RED} + \Gamma_{OX} \tag{5}$$

gives the expression for the current in terms of gate voltage and scan rate $\nu = dV_G / dt$

$$I = \frac{q^2 \nu A_D \Gamma_{MOL}}{k_B T} \frac{\left[\exp\left\{-\left(V_G - E_0\right)q / k_B T\right\}\right]}{\left[1 + \exp\left\{-\left(V_G - E_0\right)q / k_B T\right\}\right]^2} \tag{6}$$

For this reversible process, the peak current for both oxidation and reduction components of the CyV occurs at the gate voltage V_G where $V_G = E_0$, and the magnitude of the peak current is given as

$$\left|I_P\right| = \frac{q^2}{4k_B T} \nu A_D \Gamma_{MOL} \tag{7}$$

which has a negative value for oxidation and positive value for reduction. The peak current has linear relationship with the scan rate for a reversible process as can be seen from equation (7). If the redox centers are dissolved in the electrolyte solution, the peak current has square root dependence on the scan rate for a reversible process. Hence, a plot of peak current vs scan rate is typically used to verify whether the redox centers are immobilized on the surface.

The area under the peak corresponds to the total number of electrons transferred which is equal to the number of molecules in the device area A_D since each molecule

contributes one electron to each redox state (peak). Hence, the total molecular surface coverage (Γ_{MOL}) can be electrically extracted by using the following equation

$$\Gamma_{MOL} = \frac{A_P}{vqA_D} \tag{8}$$

The peak width at half-height width, h_{pw}, is also an important experimental parameter in CyV and for a reversible process

$$h_{PW} = 3.53\frac{k_B T}{q} \tag{9}$$

which is around 91 mV at 300 K.

The model and methods presented in this section are utilized in CyV analysis of the EMS capacitors to study the properties of the molecules directly attached on Si surfaces.

3.2.2 Irreversible and Quasi-reversible Process

A process is termed irreversible at a particular scan rate when the electron-transfer rate is too slow for equilibrium to be maintained. In the intermediate regions when the response lies between the reversible and irreversible, it is said to be quasi-reversible. Since the rate of change of potential is now faster than the rate of adjustment of the redox centers, the current lags behind the potential, and enhanced separation of the oxidation and reduction peaks is observed. This is the case for EMOS capacitors where in the external barrier due to tunnel oxide slows down the molecule-to-electrode charge transfer process. From the dependence of the peak separation on the scan rate, and also from the wave shape, it is possible to derive the magnitude and the potential dependence of the charge-transfer rate constants. However, for a non-reversible process, an analytical theoretical solution is not available and a 'finite difference' simulation is required, using a model of the potential dependence of the electron-transfer rate constants, rather than the Nernst equation [4].

The simplest model used to describe the electron transfer between surface attached molecule redox-center and an electrode is based on Butler-Volmer theory [5]. This model is

based on a transition-state approach to the electron-transfer process, and the equation for the electron transfer rates for the oxidation and reduction processes are given as

$$k_{OX} = k_0 \exp\left(\frac{(\alpha - 1) q (V_G - E_0)}{k_B T} \right) \tag{10}$$

$$k_{RED} = k_0 \exp\left(\frac{\alpha q (V_G - E_0)}{k_B T} \right) \tag{11}$$

The most important kinetic parameter in this equation is k_0, the rate constant at $V_G = E_0$. In case of EMOS capacitors, k_0 can be modified to be a function of the oxide thickness and the intrinsic k_0 of the molecule obtained from the EMS capacitor. The expression for modified charge-transfer rate constants would be provided, later in this chapter, in discussion on the properties of molecules on SiO_2.

The measured current in terms of the rate constants (equation (10) and (11)) is given by

$$I = qA_D \left(k_{RED} \Gamma_{OX} - k_{OX} \Gamma_{RED} \right) \tag{12}$$

where Γ_{OX} and Γ_{RED} are the instantaneous surface coverages of the oxidized and reduced forms of the redox species, respectively, and the sum of these quantities is Γ_{MOL} at any instant of time as given by equation (5) with their initial values given by equation (3). The applied potential is $V_G = V_G^* + \nu t$, where V_G^* is the initial gate voltage, ν is the scan rate (V/s), and t is time. To simulate CyV, V_G is changed in small increments thereby allowing the reaction to proceed during time intervals of $dt = dV_G/\nu$ at rates according to equations (10) and (11). The instantaneous values of Γ_{OX} and Γ_{RED} at each potential is calculated from their initial values and the oxidative or reductive charges passed since the start of the gate potential sweep. Finally, the current is calculated from equation (12).

The model and methods presented in this section are utilized with slight modifications in CyV analysis of the EMOS capacitors to study the properties of the molecules attached on tunnel oxide surfaces. It can be used for reversible systems although the simplified Nernstian model presented in previous section is adequate for the same.

3.3 Ferrocene and Porphyrin on Silicon

The discussion on this topic is presented in an unpublished manuscript included in next few pages. It covers the following:

1. Effect of Si doping type: p-Si vs. n-Si on the redox response of the molecules.
2. Effect of doping density
3. Effect of ambient light
4. Proposed model for electronic coupling of redox states with band in Si.

Experimental study and modeling of the effect of silicon substrate doping type and density on the write/erase voltages and speeds in hybrid silicon-molecular memory devices.

Srivardhan Gowda, Guru Mathur, and Veena Misra

Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695 USA

Abstract

The design and implementation of emerging hybrid silicon-molecular memory devices requires the understanding of the interaction of the molecular energy states and the energy bands in the silicon. The redox-active molecules have tunable charge states, which are quantized at room temperature. In this work, monolayers of the redox-active molecules, with cationic accessible states, were incorporated on p- and n-type silicon (100) substrates of varying doping concentrations. The redox voltages and kinetics were found to be strongly dependent on the silicon doping concentrations, and ambient light in case of n-Si substrate, while there was no significant impact of substrate doping concentration or ambient light in case of p-Si substrate. These results suggest the redox-energy state in the molecule aligns deep within the valence band of the silicon substrate. Hence, we propose a new model for electronic coupling and charge-transfer at the molecule-semiconductor interfaces. Also, the write/erase processes can be tuned by engineering the silicon substrate.

The anticipation of downscaling of silicon devices facing severe physical limitations in foreseeable future has prompted the exploration of alternative materials for use in electronic devices. Molecular electronics has spawned considerable interest and several organic molecules have been proposed for use as electronic active materials [1-3]. However, challenges related to large-scale integration of molecular materials have impeded the maturity of molecular electronics into a competitive technology. Hybrid silicon-molecular approaches have the promise of augmenting current silicon technology and also provide a path to future molecule-only technology [4, 5]. Our approach, explained in [1, 5-8], exploits the ability of individual molecules to store charges with single-electron precision at room temperature. The approach involves formation of a monolayer to a few layers of redox-active molecules via covalent linkages on Si and SiO_2 substrates for memory applications. The molecules possess discrete quantum states from which electrons can tunnel to the Si substrate at discrete applied voltages (oxidation process, cell write), leaving behind positive charges. The reduction (erase) process, which is the process of electrons tunneling back from Si to the molecules, neutralizes the positively charged molecular monolayer. The molecules have been incorporated in the Si MOSFETs and the discrete molecular states manifested in the threshold voltage and drain current characteristics of the device at room temperature [9, 10]. The salient features of the hybrid devices are low-voltage operation, multiple-states in single cell, and excellent charge retention and coverage characteristics [1, 5-10]. The charge storage characteristics are intrinsic molecular property, hence the hybrid devices may be ultimately scaleable to nano-dimensions [11]. Collectively, these characteristics make the hybrid silicon-molecular devices attractive for use in high-density charge storage memory devices such as DRAM or FLASH.

The critical facets for evaluation of the molecules for feasibility and implementation of hybrid silicon-molecular memories are: (i) physical and chemical properties of molecular monolayers assembled on silicon substrate, and (ii) comprehensive understanding of the electronic coupling of molecules with the silicon substrate. The former aspect has been extensively studied in terms of molecular monolayer surface coverages, defect densities, robustness and thermal stability for two-state ferrocene and three-state porphyrin containing monolayers on Si formed via Si-O-C covalent linkages [1, 12, 13]. The latter aspect involves the nature of the alignment of redox energy states in the molecule with the energy bands in the silicon substrate and governs the redox-charge state access potentials and charge

transfer rates. These factors ultimately determine the design parameters of the memory cells such as access, store and retention times. Hence it is essential to study effect of the Fermi level in the bands of silicon on the redox charging and discharging to gain better understanding of the energy states in the molecules and their behavior. We have previously reported the effect of doping type in silicon substrate on the redox potentials for ferrocene molecule [5]. In this report, we explore the dependence of redox response of ferrocene and porphyrin energy states on the carrier type and concentration on silicon and present a model using energy band diagrams based on the experimental data.

METHODS

Fabrication of hybrid silicon-molecular capacitor

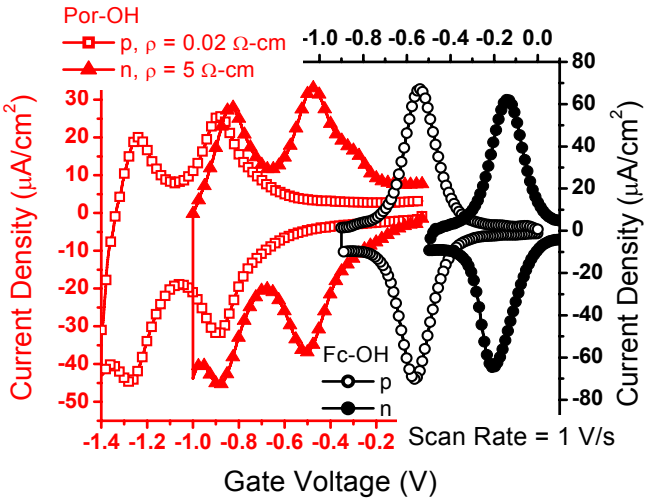
P- and n- type silicon wafers, with (100) orientation, were used as substrates. The dopant densities of the substrates used varied from 1×10^{15} to 10^{18} cm^{-3}. Active areas of sizes varying from 2.5×10^{-5} to 4×10^{-4} cm^2 were defined using a 400 nm thick thermally grown field oxide. A sacrificial oxide of 10 nm was grown in these active areas and etched back just before molecular attachment using 1% HF to obtain a smooth Si surface. The redox-active molecules used in this study were a ferrocene and a Zn(II) trimesitylporphyrin, each derivatized with benzyl alcohol linker for attachment to the Si surface via the formation of a Si-O bond. The molecules (designated Fc-BzOH and Por-BzOH, respectively) have been shown to form dense and stable monolayers on Si surface [13]. Fc-BzOH has two-charge states (neutral and monopositive) and Por-BzOH has three-charge states (neutral, monopositive and dipositive). The molecular attachment to Si surface was carried out in an Argon environment at elevated temperatures (80 °C for Fc-BzOH; 170 °C for Por-BzOH) using benzonitrile as the solvent. The samples were subjected to ultra-sonic rinse using dichloromethane as solvent to remove the excess molecules not covalently attached to the surface.

Electrochemical characterization

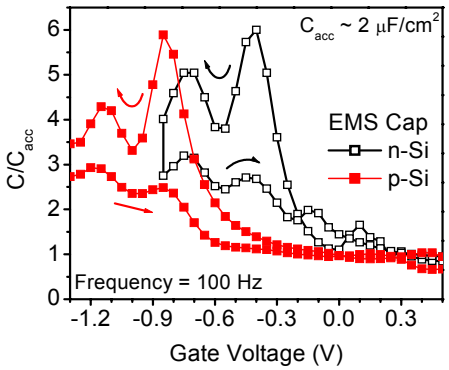
A 1 M solution of tetrabutyl ammonium hexafluorophosphate was used as an electrolyte gate for electrical characterization. Silver wire was used as the gate electrode. These electrolyte-molecule-silicon (EMS) capacitor structures were characterized under inert atmospheres using cyclic voltammetry (CyV), capacitance-voltage (CV) and conductance-voltage (GV) measurement techniques. CyV was performed using a CHI600A

electrochemical analyzer and the CV-GV characteristics were obtained using a HP 4284A LCR meter.

RESULTS AND DISCUSSION



(a)



(b)

Fig. 1 (a) CyV of EMS capacitors of Fc-BzOH on n-Si, Fc-BzOH on p-Si, Por-BzOH on n-Si, and Por-BzOH on p-Si. The doping density of p-Si and n-Si substrates were 3×10^{18} cm^{-3} and 1×10^{15} cm^{-3} respectively. The lower half of the current corresponds to oxidation, while the upper half corresponds to reduction. Top-x, right-y axes correspond to Fc-BzOH CyVs and bottom-x, left-y axes correspond to Por-BzOH CyVs. **(b)** Capacitance-Voltage (CV) characteristics of EMS capacitors of Por-BzOH on n-Si, and Por-BzOH on p-Si. The arrows indicate the sweep direction of the gate voltage. The gate voltage sweep in negative direction corresponds to oxidation and the reverse (positive) sweep corresponds to reduction.

Ferrocene molecule (Fc-BzOH) has a single cationic accessible state and porphyrin molecule (Por-BzOH) has two cationic accessible states. These states manifest as current peaks in the cyclic voltammetry (CyV) and capacitance and conductance peaks in impedance spectroscopy (CV-GV) measurements. Figure 1 shows CyV of Fc-BzOH and Por-BzOH molecules on p-Si and n-Si substrates under ambient light. The peaks observed are associated with oxidation and reduction of the molecules in the monolayers. The negative current peaks (bottom-half) correspond to oxidation of the redox states and the positive current peaks correspond to reduction of the redox states. The redox peak potentials of molecules on p-Si occur at higher negative gate voltages as compared to n-Si. This applies to both Fc-BzOH and Por-BzOH molecules as can be seen in Figure 1.

Impedance spectroscopy (CV-GV) measurements also revealed identical differences in the redox potentials for p-Si Vs n-Si substrates (Figure 1 (b)).

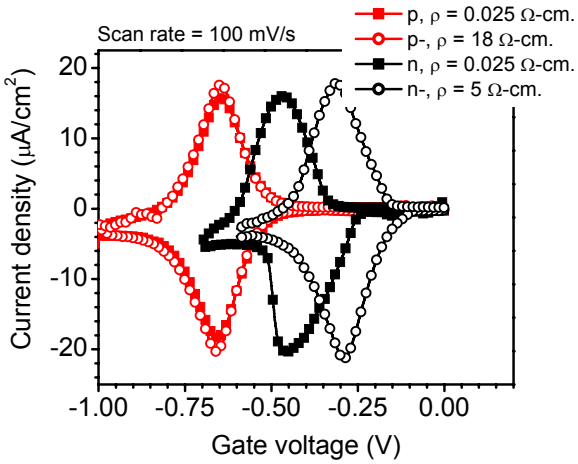


Fig. 2 CyV of EMS capacitors with Fc-BzOH on n and p type Si substrates for two different doping concentrations each: effect of Si doping type and density on the redox voltages. The measurement scan rate is 100 mV/s.

From flatband-voltage(V_{FB}) extraction using the CV-GV measurements, it was also established that the electrolyte utilized in this work acts like a p+ gate indicating that the p-Si surface is accumulated in the region of the redox-activity, while n-Si surface is depleted in the same voltage ranges. Also, in case of p-Si substrates redox peak voltages and redox response were unaffected by the dopant density as can be observed from Figure 2, where redox peaks for Fc-BzOH occur at gate voltage of -0.65 V for two different dopant densities. However, in case of the n-Si substrate redox peak potentials were found to increase with increasing dopant density (Figure 2) for a fixed ambient light intensity and measurement scan rate (rate of change of gate potential).

Fast scan CyVs further revealed that the oxidation process was rate-limited while the reduction process did not have rate-limitation in case of n-Si substrates. The oxidation process rate was enhanced by increasing the light intensity and the extent of recovery in the oxidation rate was greater in lower doped n-Si sample. There was no impact of intensity of light or absence of light on oxidation and reduction processes for p-Si substrates even at fast scan (< 1kV/s) CyVs. The dependence of oxidation rate on dopant density and ambient

light for n-Si substrates were further evidenced in slow scan CyV under dark ambient, where no oxidation was observed (Figure 3). The oxidation process recovers with increasing light intensity and when the intensity of the light is increased beyond the value at which the oxidation peak completely recovers the redox peak potential shifts to lower gate voltages (Figure 3). The shift in redox voltage is proportional to the intensity of ambient light and is greater in magnitude for a lower doped n-Si substrate as compared to that for a higher doped substrate for fixed CyV scan rate and light intensity.

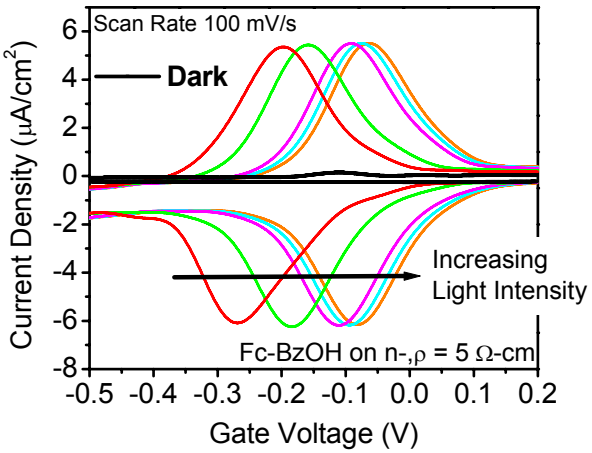
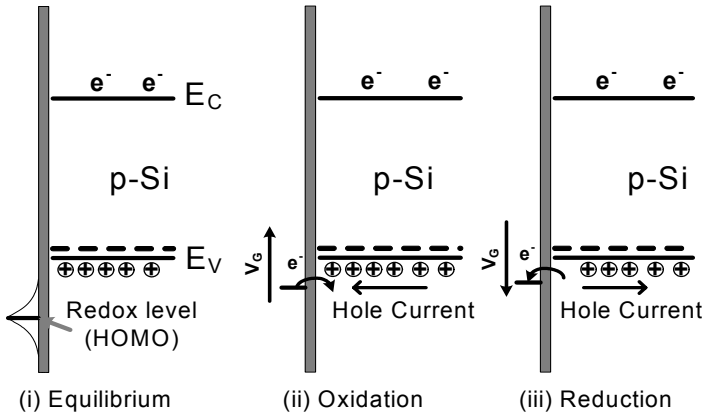


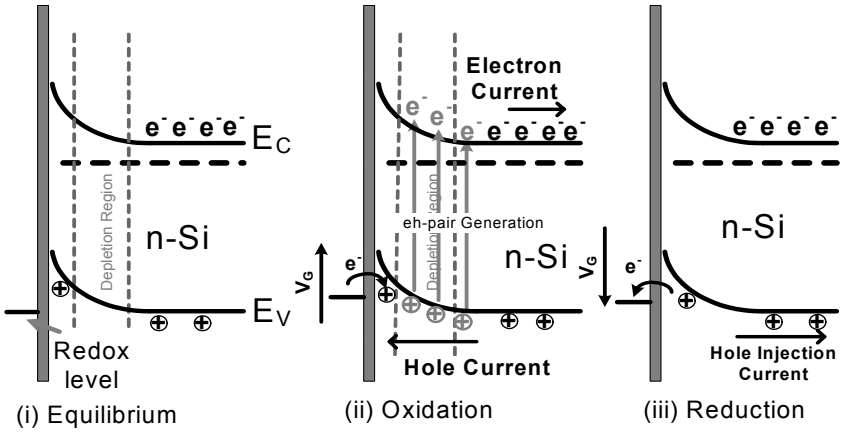
Fig. 3 CyV of EMS capacitor with Fc-BzOH on lightly-doped (1×10^{15} cm^{-3}) n-Si substrate, under dark and ambient light of varying intensities, showing effect of the light on redox response. The measurement scan rate is 100 mV/s.

In order to understand and model the experimental observations, it is essential to determine if the redox energy states couple with either the conduction or valence band in Si. When a molecule is formed from its constituent atoms, the atomic orbitals (AOs) of individual atoms overlap with one another to create molecular orbitals (MOs), which are discrete quantum states for electrons in the molecules. The filled MO with maximum energy is termed as the Highest Occupied Molecular Orbital (HOMO) and depicts the first cationic-accessible state. The empty MO with least energy is called the Lowest Unoccupied Molecular Orbital (LUMO) and depicts the first anionic-accessible state. MOs are spatially localized and there exists no interactions between individual molecules in the densely-packed monolayer to form extended energy bands. This is also substantiated by our previous experimental evidence of the limited intermolecular interactions within molecular monolayers of Fc-BzOH on Si [14] and no inter-dependence of the ferrocene-porphyrin

redox states in single-molecule [15] or mixed FcBzOH-PorBzOH monolayer configurations [16]. Hence the energy levels of MOs in the molecules remain discrete and are not expected to be affected by the Fermi level in the silicon. If it is assumed that the HOMO level of the molecules lines up with and exchanges charges with the conduction band in the Si, it is expected that: (i) oxidation is a kinetically fast process in n-Si as the electron from the redox state injected into the conduction band would be readily swept away, and (ii) reduction process in rate-limited in p-Si as conduction band is devoid of electrons necessary for injection into the redox state. However, the experimental observations presented in previous sections are in contravention of these expectations, which suggests that the redox states electronically couple with the valence band in the Si.



(a)



(b)

Fig. 4 Band diagrams showing redox-related charge transfer processes for **(a)** Fc-BzOH on p-Si substrate, and **(b)** Fc-BzOH on n-Si substrate.

In the initial equilibrium condition, the redox energy level of the molecule can be thought of as being at a lower electronic potential than the valence band edge (E_V) of Si. The p-Si surface is accumulated with voltage drop in the silicon surface (ψ_{Si}) being negligible. A negative gate voltage raises the energy of the electrons in the molecules resulting in tunneling of electron to the valence band of the silicon through an energy barrier associated with the linker. Since holes are available in valence band of the p-Si to recombine with the injected electrons, oxidation is not a rate-limited process. Also, electrons are available in the valence band of Si for reduction of molecules when the gate voltage is relaxed (Figure 4(a)). The molecule-Si interface for p-Si is similar to molecule-metal interface and hence the redox voltages for ferrocene and porphyrin on p-Si is similar to that of gold surface [17]. However, in case of n-Si, silicon surface is depleted and the potential drop (ψ_{Si}) is significant. Also, holes are not available in the valence band of n-Si to recombine with electrons injected from the molecules during oxidation and need to be generated in the space-charge region by thermal generation as shown in Figure 4(b). Hence oxidation process is rate-limited for n-Si since minority (holes in n-Si) carrier generation is a slow process and can be enhanced by steady-state optical excitation. Reduction process in n-Si is not rate-limited since the electrons necessary for reduction are readily available in valence band of n-Si. Since ψ_{Si} is significantly large in n-Si and is a strong function of the dopant density and the surface photo-voltages developed due to the optical excitation, redox voltages for molecules on n-Si varies with substrate dopant density and ambient light.

In summary, redox-active molecules with cationic-accessible states have characteristics of ohmic contact on p-Si and that of Schottky diode on n-Si. It can be predicted by extension of the proposed model that anionic-accessible states of redox-active molecules would couple with the conduction band of the silicon substrate and would exhibit complimentary p-Si Vs n-Si behavior.

REFERENCES

[1] Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science*, vol. 302, pp. 1543-1545, 2003.

[2] J. R. Heath and M. A. Ratner, "Molecular electronics," *Physics Today*, vol. 56, pp. 43-49, 2003.

[3] C. P. Collier, E. W. Wong, M. Belohradsky, F. M. Raymo, J. F. Stoddart, P. J. Kuekes, R. S. Williams, and J. R. Heath, "Electronically configurable molecular-based logic gates," *Science*, vol. 285, pp. 391-394, 1999.

[4] R. A. Wolkow, "Toward hybrid devices," *Chemical & Engineering News*, vol. 79, pp. 228-228, 2001.

[5] S. Gowda, G. Mathur, L. Qihang, S. Surthi, Z. Qian, J. S. Lindsey, K. Mobley, D. F. Bocian, and V. Misra, "Hybrid silicon/molecular memories: co-engineering for novel functionality," *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pp. 22.1.1, 2003.

[6] K. M. Roth, N. Dontha, R. B. Dabke, D. T. Gryko, C. Clausen, J. S. Lindsey, D. F. Bocian, and W. G. Kuhr, "Molecular approach toward information storage based on the redox properties of porphyrins in self-assembled monolayers," *Journal of Vacuum Science & Technology B*, vol. 18, pp. 2359-2364, 2000.

[7] Q. L. Li, S. Surthi, G. Mathur, S. Gowda, V. Misra, T. A. Sorenson, R. C. Tenent, W. G. Kuhr, S. Tamaru, J. S. Lindsey, Z. M. Liu, and D. F. Bocian, "Electrical characterization of redox-active molecular monolayers on SiO2 for memory applications," *Applied Physics Letters*, vol. 83, pp. 198-200, 2003.

[8] W. G. Kuhr, A. R. Gallo, R. W. Manning, and C. W. Rhodine, "Molecular memories based on a CMOS platform," *Mrs Bulletin*, vol. 29, pp. 838-842, 2004.

[9] S. Gowda, G. Mathur, Q. Li, S. Surthi, and V. Misra, "Hybrid Silicon/Molecular FETs: A Study of the Interaction of Redox-Active Molecules With Silicon MOSFETs," *Nanotechnology, IEEE Transactions on*, vol. 5, pp. 258, 2006.

[10] S. Gowda, G. Mathur, Q. Li, S. Surthi, Q. Zhao, J. S. Lindsey, D. F. Bocian, and V. Misra, "Modulation of drain current by redox-active molecules incorporated in Si MOSFETs," *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, pp. 707, 2004.

[11] Q. Zhao, Y. Luo, S. Surthi, Q. L. Li, G. Mathur, S. Gowda, P. R. Larson, M. B. Johnson, and V. Misra, "Redox-active monolayers on nano-scale silicon electrodes," *Nanotechnology*, vol. 16, pp. 257-261, 2005.

[12] A. Balakumar, A. B. Lysenko, C. Carcel, V. L. Malinovskii, D. T. Gryko, K. H. Schweikart, R. S. Loewe, A. A. Yasseri, Z. M. Liu, D. F. Bocian, and J. S. Lindsey, "Diverse redox-active molecules bearing O-, S-, or Se-terminated tethers for attachment to silicon in studies of molecular information storage," *Journal of Organic Chemistry*, vol. 69, pp. 1435-1443, 2004.

[13] K. M. Roth, A. A. Yasseri, Z. M. Liu, R. B. Dabke, V. Malinovskii, K. H. Schweikart, L. H. Yu, H. Tiznado, F. Zaera, J. S. Lindsey, W. G. Kuhr, and D. F. Bocian, "Measurements of electron-transfer rates of charge-storage molecular monolayers on Si(100). Toward hybrid molecular/semiconductor information storage devices," *Journal of the American Chemical Society*, vol. 125, pp. 505-517, 2003.

[14] S. Gowda, G. Mathur, Q. Li, S. Surthi, and V. Misra, "Approach for investigating lateral conduction in self-assembled monolayers," *Applied Physics Letters*, vol. 87, pp. 262115, 2005.

[15] D. T. Gryko, F. Zhao, A. A. Yasseri, K. M. Roth, D. F. Bocian, W. G. Kuhr, and J. S. Lindsey, "Synthesis of thiol-derivatized ferrocene-porphyrins for studies of multibit information storage," *Journal of Organic Chemistry*, vol. 65, pp. 7356-7362, 2000.

[16] Q. L. Li, G. Mathur, S. Gowda, S. Surthi, Q. Zhao, L. H. Yu, J. S. Lindsey, D. F. Bocian, and V. Misra, "Multibit memory using self-assembly of mixed ferrocene/porphyrin monolayers on silicon," *Adv Mater*, vol. 16, pp. 133-+, 2004.

[17] K. M. Roth, J. S. Lindsey, D. F. Bocian, and W. G. Kuhr, "Characterization of charge storage in redox-active self-assembled monolayers," *Langmuir*, vol. 18, pp. 4030-4040, 2002.

Note to readers: This is an unpublished manuscript. The actual published version may be modified.

- end of manuscript -

3.4 Porphyrin Polymers on Silicon

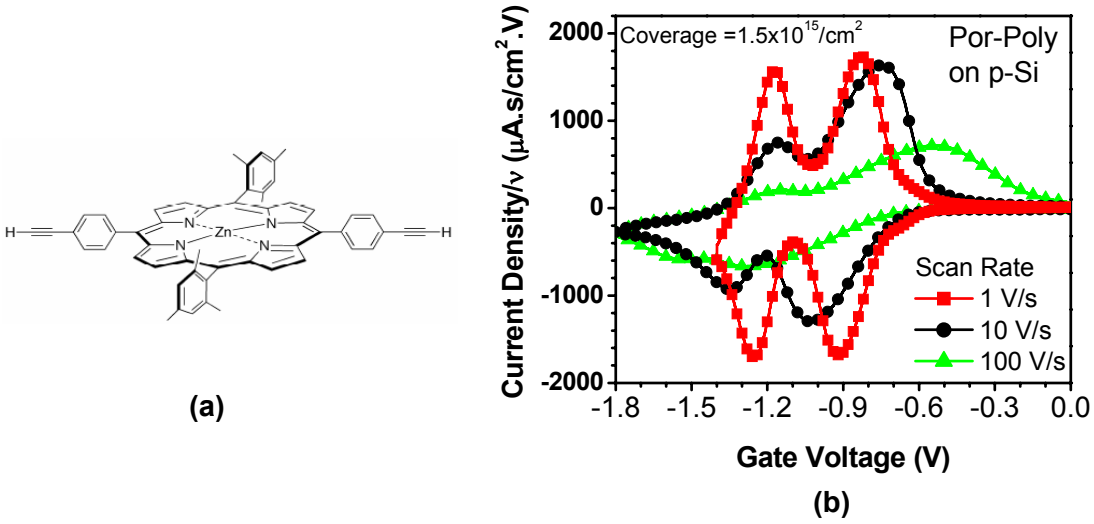


Figure 3.1 (a) Structure of porphyrin molecule functionalized with acetylene groups (**Por-m**). This molecule is used to form porphyrin polymer (**Por-Poly**) on Si and SiO_2 surfaces by using in-situ polymerization technique. **(b)** CyV characteristics of Por-Poly film attached on P-Si surface. The multi-layer film retains the quantized states of individual molecules.

The saturation monolayer coverages for porphyrin (**Por-BzOH**) on Si is less half that for the ferrocene (**Fc-BzOH**) on Si. As discussed previously, the increasing the number of redox states in the molecule to achieve multi-state in single cell results in a larger molecule, which reduces the charge density. One of the ways to increase the charge density in such a scenario, say for porphyrin, is to incorporate multi-layer films on Si. Fig. 3.1 (a) shows the chemical structure porphyrin molecule derivatized with acetylene groups at the ends (**Por-m**) and this molecule is used for in-situ polymerization to form porphyrin polymer (**Por-Poly**) on Si and ultra-thin SiO_2 surfaces [6]. The details of the polymerization process were given in chapter 2. The porphyrin polymer retains the quantized energy states within individual molecules as evidenced by current peaks in CyV associated with redox charging and discharging (Fig. 3.1 (b)). The CyV-extracted surface coverage was found to be as high as 1.5 x 10^{15} #/cm^2 for thickest **Por-Poly** film, which is almost 30-fold greater than saturation-coverage achievable with porphyrin monolayers. It was observed from the fast-CyV measurements that the redox kinetics slowed down (Fig. 3.1 (a)) with increasing thickness of the polymer film (or redox charge density) suggesting that these polymers are intrinsically slow. Hence, there is a charge-density vs. speed performance trade-off

associated with the porphyrin polymer films. Detailed electrical characterization of these films can be found in another student's dissertation [7].

The **Por-Poly** films were incorporated in MoleFETs for improving read window of the device and multi-state demonstration. The results and discussion on these aspects will be presented in chapter 5.

3.5 Ferrocene on Oxide Layers on Silicon

3.5.1 Need for Oxide Layers

The ultra-thin oxide layers are placed between redox-active molecule and silicon substrate primarily to enhance charge-retention time of the MoleFET device so as to meet the nonvolatile retention requirements as discussed earlier. Additionally, the oxide layer also serves to passivate the dangling bonds on the Si surface. The saturation surface monolayer coverages (number of molecules/cm^2) for ferrocene (**Fc-BzOH**) and porphyrin (**Por-BzOH**) on Si (100) are 2 x 10^{14} and 0.45 x 10^{14}, respectively [8]. The surface density of Si (100) is approximately 1.5 x 10^{15} atoms/cm^2. Even in case of the smallest molecule, there are greater than 80 % of the Si atoms that are not bonded to any molecule in the monolayer and may result in dangling bonds. Hence, it is essential to passivate Si surface with a layer of thermal oxide to minimize interface trap density (D_{it}). A large value of D_{it} will introduce undesired characteristics in case of the FET device.

The oxide layer on silicon essentially serves two purposes: (i) tunnel barrier for enhanced charge retention, and (ii) passivation of Si surface. The former functionality of the oxide layer is explored in rest of this chapter.

3.5.2 Properties of Ferrocene on SiO_2 and HfO_2/SiO_2 Layers

The discussion on this topic is presented in a publication included in next few pages. It covers the following:

1. Redox response dependence on SiO_2 thickness.
2. Modified Butler-Volmer Model
3. Asymmetric Tunneling: Substrate Effect
4. Need for high-K Tunnel Barriers
5. Asymmetric Layered Tunnel Barrier on Silicon

Engineering Tunnel Barriers in Hybrid Silicon/Molecular Memory Devices

Srivardhan Gowda, Guru Mathur and Veena Misra

Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695, USA

This paper appears in: IEEE-NANO 2006, Sixth IEEE Conference on Nanotechnology, 2006.
Publication Date: 17-20 June 2006. Volume: 1
On page(s): 93 – 96

Abstract— This paper discusses the role of asymmetric tunneling across oxide barriers in Hybrid Silicon/Molecular devices. Devices incorporating redox-active (ferrocene) molecules on silicon dioxide (SiO_2) of varying thickness and Hafnium dioxide (HfO_2)/SiO_2 stack on p-Si substrates were investigated as charge storage elements. The reduction (erase) process was found to be increasingly rate-limited as compared to oxidation (write) process with increasing SiO_2 thickness. This is attributed to asymmetric tunneling rates mainly due to a lower potential drop across the tunnel barrier for a given gate voltage during reduction process as compared to oxidation, resulting from higher surface potential drop in Si. Although increased SiO_2 thickness provides for improved retention, it severely retards write process. This can be overcome by employing asymmetric layered barrier of HfO_2/SiO_2 which enhances effect of inherent asymmetric tunneling rates and also speeds up the write process due to higher relative permittivity and lower barrier offsets of HfO_2/SiO_2 on Si as compared to SiO_2. This behavior can be utilized to improve retention properties of these hybrid memory devices with minimal deterioration in write times.

Keywords – Ferrocenes, hybrid, memory, redox-active, tunnel barriers, silicon/molecular.

This work was supported by Zettacore Inc., and CNID (DARPA/DMEA Award No. H94003-05-2-0504).

I. INTRODUCTION

Molecular electronics has spawned considerable interest as a potential candidate technology beyond silicon [1-3]. However, there are several challenges that need to be overcome before molecular electronics can mature into a competitive technology. A hybrid silicon/molecular approach may be instrumental in providing a transitional path to a future molecule-only technology and augmenting today's CMOS only technology [4,5]. Our approach, explained in [1,5-6] exploits the ability of individual molecules to store charges with single-electron precision at room temperature, and is fundamentally different from most of the other approaches which are based on measuring the change in the conductivity of molecules [2,3]. The hybrid devices are fabricated by forming self-assembled monolayers of redox-active molecules on Si or silicon dioxide (SiO_2) surfaces [5,6]. The molecules possess discrete quantum states from which electrons can tunnel to the Si substrate at discrete applied voltages (oxidation process), leaving behind a positively charged layer of molecules. The reduction process, which is the process of electrons tunneling back from Si to the molecules, neutralizes the positively charged molecular monolayer. The charge-transfer processes can also be perceived as holes from valence band of Si tunneling into molecules and vice-versa. We have recently determined that the cationic redox energy states in the molecules communicate with the valence band of Si substrate [7]. The molecules have been incorporated in the Si MOSFETs to modulate the threshold voltage and drain current characteristics of the device [8]. The hybrid devices with quantized states, along with low-voltage operation, multiple-state, and excellent charge retention and coverage characteristics may be attractive for use in charge storage memory devices such as DRAM or FLASH [5-10].

In hybrid silicon/molecular capacitors with molecules on SiO_2 on p-Si substrates, we have previously reported the write and erase voltages shifting to more positive and negative values, respectively, from the intrinsic redox potential (E_0) of the molecules with increasing tunnel barrier thickness [9,10]. In this paper, we present a model based on Butler-Volmer theory and show new observations of asymmetric tunneling across the oxide barrier. Also, results of hybrid capacitor with Hafnium dioxide (HfO_2)/ SiO_2 tunnel barrier will be discussed.

II. EXPERIMENTAL

A schematic of the hybrid silicon/molecular capacitor structure is shown in Fig. 1. P-type Si wafers doped with $1x10^{18}$ cm^{-3} of boron atoms were used. A 145-Å SiO_2 was grown in the active areas and etched back using 1 % HF to obtain varying oxide thicknesses. The HfO_2/SiO_2 stacks were fabricated by ALD methods as reported in [11] and consisted of 4 nm HfO_2 with 1 nm interfacial SiO_2. The inset in Fig. 1 shows the redox-active molecule used in this study, ferrocenyl phosphonate (**Fc-P**). This molecule possesses two stable charge states: neutral and monopositive; and has the ability to form a dense and stable monolayer on SiO_2 surfaces [6]. The molecule solution used for the attachment procedure was a 1 mM solution of the molecule in dimethyl formamide. This solution was placed on the sample, which was maintained at 80°C in an Argon environment. Electrical characterization was performed using CHI600 electrochemical analyzer and HP4284A LCR meter.

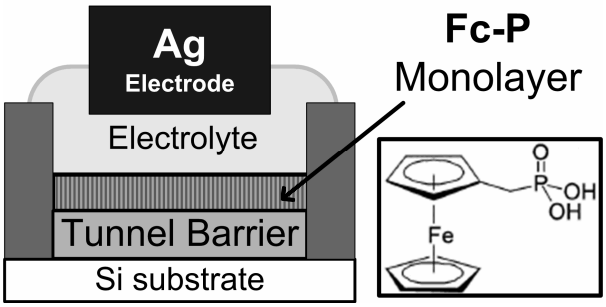


Fig. 1 Schematic of a hybrid silicon/molecular capacitor with a monolayer of molecules attached to SiO_2 surface. Gate electrolyte is contacted by Ag electrode. Inset shows the chemical structure of ferrocenyl phosphonate, **Fc-P**.

III. RESULTS AND DISSCUSSIONS

Fig. 2 show cyclic voltammetry (CyV) characteristics of hybrid silicon/molecular capacitors with **Fc-P** attached on varying thickness of SiO_2 on p-Si substrates. The peaks in the current are associated with the oxidation (negative current) and reduction (positive current) of the redox-active molecules. A negative gate voltage raises the redox energy state (HOMO) of the molecule and results in tunneling of a hole into the molecule from the valence band of the Si substrate through the tunneling barrier layer. This is the oxidation

process which leaves the molecules in the positive charged or written state. A reverse voltage sweep causes hole to tunnel from the molecule to the valence band of Si substrate thereby reducing the molecule. The molecules in the monolayer become neutral, which is the erased state of the memory cell. As can be seen from the Fig. 2, there is increased shifting of the oxidation and reduction peaks (ΔV_P), to higher negative and positive gate potentials, respectively, from E_0 with increasing SiO_2 thickness [10]. Also, the half-peak widths (h_{PW}) of the oxidation and reduction processes increase with increasing oxide thickness indicating slowing of charge-transfer processes between molecules and Si substrate. Increasing measurement scan rates for a given oxide thickness has a similar effect with increased splitting between the oxidation and reduction peaks [10].

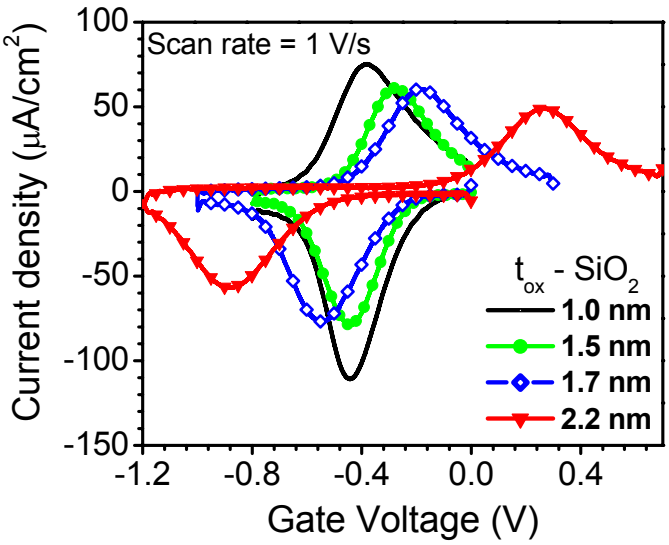


Fig. 2 CyV characteristics of hybrid silicon/molecular capacitors incorporating **Fc-P** with varying SiO_2 thickness at a scan rate of 1 V/s.

The impact on oxidation and reduction processes with increasing SiO_2 thickness can attributed to two factors – (i) lowering of charge tunneling rate across the barrier, and (ii) increasing voltage drop across SiO_2 (V_{OXIDE}) resulting in lower voltage drop across molecule (V_{MOL}) for a given gate bias. This can be modeled using Butler Volmer theory [12]. Accordingly, the oxidation and reduction charge-transfer rates (k_{OX} and k_{RED}, respectively) can be given as follows:

$$k_{OX} = k_0 \, e^{[(\alpha-1)(V_{GATE}-E_0-V_{OXIDE})q/k_BT]} \quad (1)$$

$$k_{RED} = k_0 `e^{[(\alpha)(V_{GATE} - E_0 - V_{OXIDE})q/k_B T]} \quad (2)$$

$$k_0 ` = k_0 \times T \quad (3)$$

$$T \propto 1/e^{t_{ox}\phi_B} \quad (4)$$

where V_{GATE} is the applied gate voltage, α is a constant typically with value of 0.5 for reversible redox systems. k_0` is the modified charge-transfer rate constant at $E_0$. As shown in (3), $k_0$` is mathematical product of the intrinsic charge-transfer rate constant of the molecule (k_0), which has been previously characterized to be fast [1], and the charge transmission probability (T) across the barrier at E_0. The transmission probability has inverse exponential dependence on the oxide thickness (t_{ox}) and barrier height (ϕ_B) assuming direct tunneling as dominant mechanism for ultra-thin oxide barriers (t_{ox} < 3nm) used in this study. From (1)-(4), it is evident, that the k_{OX} decreases with increasing t_{ox} and hence necessitates higher negative applied gate voltages for oxidation process at a given scan rate. Similarly, reduction process requires higher positive gate potentials with increasing t_{ox}. However, it is important to note that the E_0 of the system is not modified as the sign of V_{OXIDE} follows that of the V_{GATE}.

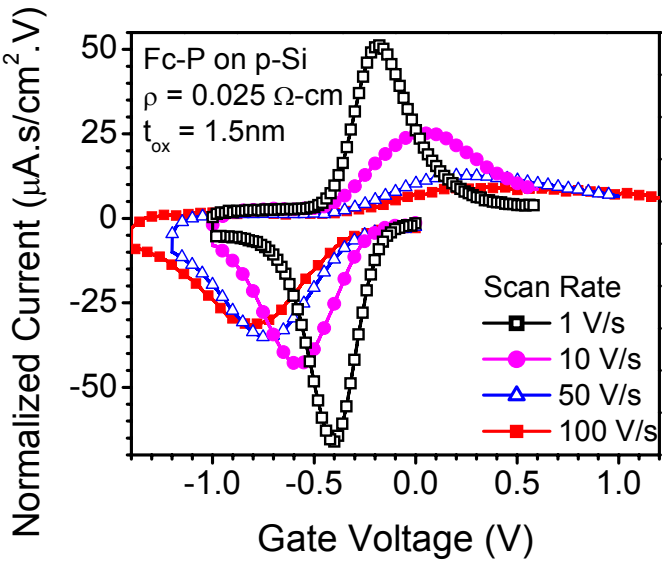


Fig. 3 CyV of **Fc-P** on 1.5nm of SiO_2 on p-Si: effect of fast-scan rates on oxidation and reduction peaks.

The model detailed above is employed to explain new observations of asymmetric tunneling in hybrid capacitors with SiO_2 tunnel barrier in the next section. The subsequent section discusses results of the devices incorporating molecules on bilayer (HfO_2/SiO_2) tunnel barrier.

A. Asymmetric Tunneling

The data presented so far, which is primarily slow-scan CyV, suggests that oxidation and reduction process have identical charge-transfer rates with symmetric shifting in oxidation and reduction peaks about $\boldsymbol{E_0}$. However, the fast-scan CyV (>1V/s) reveals that charge-transfer rates during reduction is significantly slower as compared to that during oxidation process.

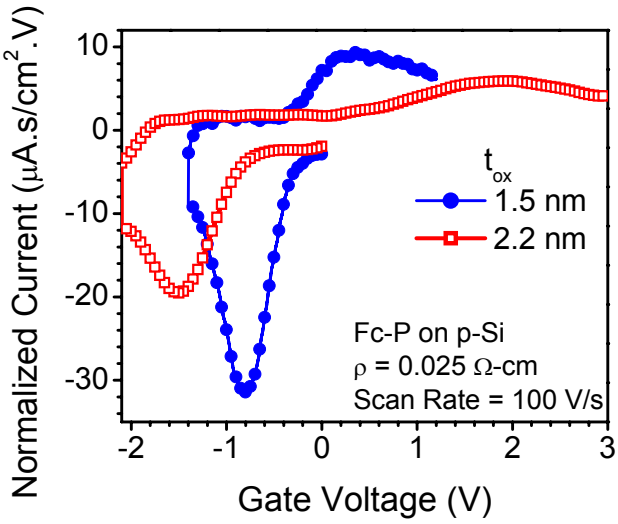


Fig. 4 Fast-scan CyV of **Fc-P** on SiO_2 on p-Si: effect of oxide thickness on asymmetric tunneling behavior.

As can be seen from Fig. 3, with increasing scan rate, $\boldsymbol{\Delta V_P}$ for reduction peak is increasing by a greater magnitude as compared to that for oxidation peak. Also, the $\boldsymbol{h_{PW}}$ for reduction peak is greater than $\boldsymbol{h_{PW}}$ for oxidation peak at higher scan rates, further indicating the asymmetric tunneling rates across the barrier. Fig. 4 shows that this behavior is amplified by increasing $\boldsymbol{t_{ox}}$ for a given scan rate. Fig. 5 along with Table 1 summarizes the observations confirming asymmetry in the oxidation and reduction rates in the hybrid device. The reason for these observations is detailed below.

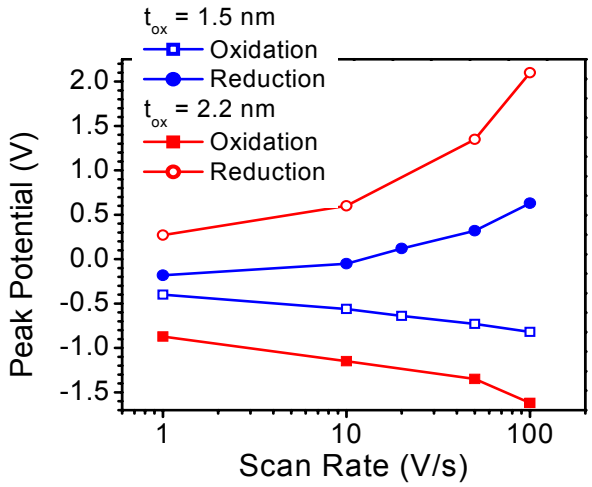


Fig. 5 Redox peak voltage versus Scan rate extracted from Fast CyV of **Fc-P** on SiO_2 on p-Si: effect of oxide thickness at higher scan rates on oxidation and reduction peak voltages.

Table 1. EFFECT OF OXIDE THICKNESS AND SCAN RATE ON ΔV_P AND HALF-PEAK WIDTH

t_{ox}(nm)	ΔV_P(100V/s) - ΔV_P(1V/s) * | h_{pw}(100V/s)	
	Oxidation (V)	*Reduction (V)*
1.5	-0.42 | 0.5	0.81 | 1.1
2.2	-0.75 | 0.9	1.83 | 2.6

**Difference in values of ΔV_P @ 100 V/s scan rate and ΔV_P@1V/s.*

In Impedance Spectroscopy measurements, conductance peaks associated with depletion of Si were observed at gate voltages more positive than E_0 for the hybrid devices [6]. This indicates that the p-Si substrate is in accumulation for gate voltage during the oxidation process, with energy profile of the barrier oxide as shown in Fig. 6(a). As the measurement scan rate is increased (or t_{ox} is increased for a given scan rate), reduction process is shifted to more positive gate voltages and Si surface starts getting depleted. This causes an additional voltage drop in Si (ψ_s) as shown in Fig. 6(b). Hence, for a given gate voltage, there is a decrease in V_{OXIDE} resulting in lowering of tunneling rate across the oxide as compared to that during oxidation, resulting in an asymmetric T.

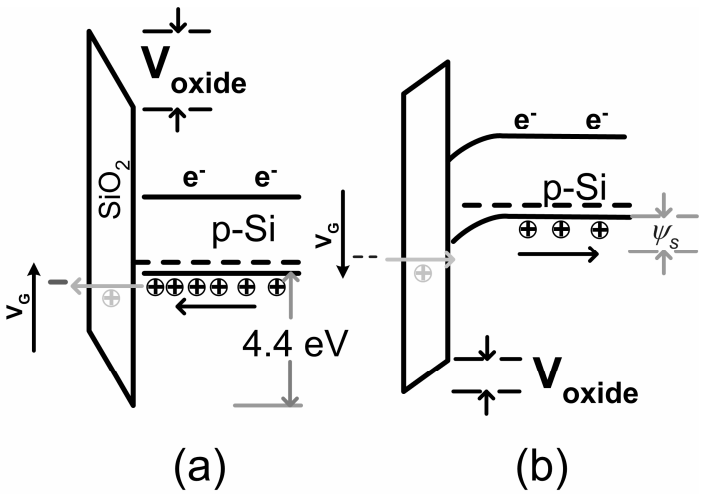


Fig. 6 Band diagrams showing redox processes in hybrid capacitor with **Fc-P** on SiO_2 on p-Si substrate. (a) Gate voltage scan direction towards oxidation of the molecule. (b) Gate voltage scan direction towards reduction of the molecule

There was no effect of optical excitation on the scan rate dependence of the reduction process indicating that minority carrier generation has little or no contribution to reduction process becoming rate-limited, which is expected since the molecule primarily communicates with valence band of the Si substrate. The asymmetry in tunneling rates necessitates k_0` in (1) and (2) being replaced by $k_0`,_{OX}$ (=k_0*T_{OX}) and $k_0`,_{RED}$ (=k_0*T_{RED}), respectively to accurately model the effect.

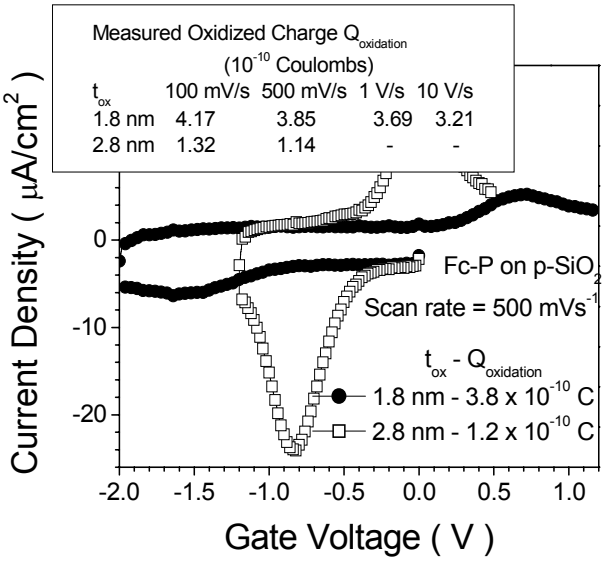


Fig. 7 CyV characteristics of hybrid silicon/molecular capacitor incorporating **Fc-P** with varying SiO_2 thickness at a scan rate of 500 mV/s.

Although, increasing oxide thickness improves retention time [10], it severely retards oxidation rate for t_{ox} > 2.5 nm when direct tunneling across SiO_2 barrier becomes negligible as can be seen in Fig.7. For the case of t_{ox} = 2.8 nm, the written charge becomes dramatically low even for slow-scan CyV. In order to overcome these constraints and also further exploit the asymmetric tunneling behavior, asymmetric layered tunnel barrier involving HfO_2/ SiO_2 stack was employed in the hybrid capacitor.

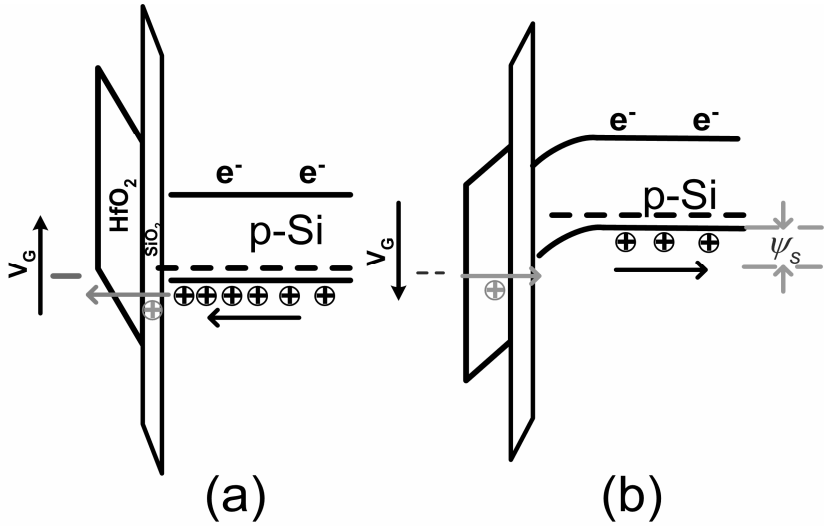


Fig. 8 Band diagrams showing redox processes in hybrid capacitor with **Fc-P** on HfO_2/SiO_2 on p-Si substrate. (a) Gate voltage scan direction towards oxidation of the molecule. (b) Gate voltage scan direction towards reduction of the molecule.

B. Asymmetric Layered Tunnel Barrier (HfO_2/SiO_2)

HfO_2 has higher relative permittivity (~20) and has a net lower barrier to holes (valence band offset ~3.4 eV on Si) as compared to thick SiO_2. This is due to the fact that under certain negative gate voltage conditions, the holes encounter a very small tunneling barrier owing to difference in band gap of SiO_2 and HfO_2 [13]. In addition, the voltage drop across the HfO_2 layer (V_{OXIDE}) in a hybrid capacitor is lesser by a factor of 3 as compared to SiO_2 owing to their relative permittivity differences. Hence the redox peaks are expected to be sharper and allow for larger operational temperatures. From (1)-(4), it is evident, charge-transfer rates (k_{OX} and k_{RED}) are dramatically modified for HfO_2/SiO_2 as compared to SiO_2 of identical thickness. Hence, it is possible to employ physically thicker barrier with HfO_2 to improve charge retention properties while maintaining reasonably fast charge-transfer rates.

High-k/SiO_2 dielectric stacks have been previously shown to have tunneling currents which are asymmetric with electric field direction [13]. Also, bilayer tunnel barriers have been proposed for improving retention time in non-volatile memories without compromising on the write speeds [14]. An HfO_2/SiO_2 stack incorporated in the hybrid device as a tunnel barrier would provide for asymmetric layered tunnel barrier as depicted in Fig. 8. As seen in Fig. 8(a), for oxidizing gate potentials, hole from substrate first tunnels through the higher barrier potential material (SiO_2) and experiences only a minimal barrier from the HfO_2 layer. However, during the reduction process, hole from molecule experiences barriers of both layers resulting in a significantly lower transmission probability ***T*** as compared to the oxidation case (Fig. 8(b)). This asymmetric tunneling due to layered barrier augments the asymmetry owing to asymmetric drop in Si surface, which was detailed in the previous section, resulting in reduction charge-transfer becoming significantly rate limited as compared to oxidation (Fig. 9). As observed in Fig. 10, the ΔV_P for reduction peak is significantly greater than that for oxidation peak even at slow scan CyV. The rate limitation of reduction process with HfO_2 is significantly greater than SiO_2 supporting large asymmetry between oxidation and reduction. The use of these barriers coupled with redox molecules can enable the FLASH like hybrid MOSFET based memories where molecules are incorporated within the gate dielectric stack.

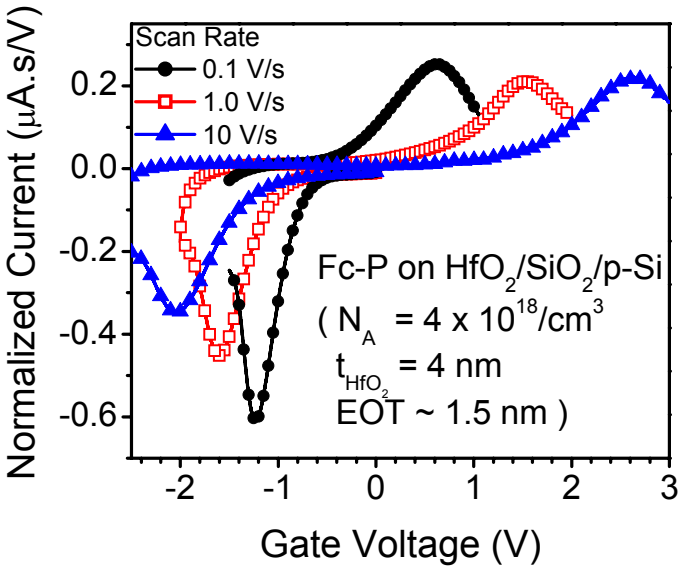


Fig. 9 CyV of **Fc-P** on 4nm of HfO_2 on ~1nm of interficial SiO_2 on p-Si. The equivalent oxide thickness (EOT) of the HfO_2/SiO_2 stack was ~ 1.5 nm.

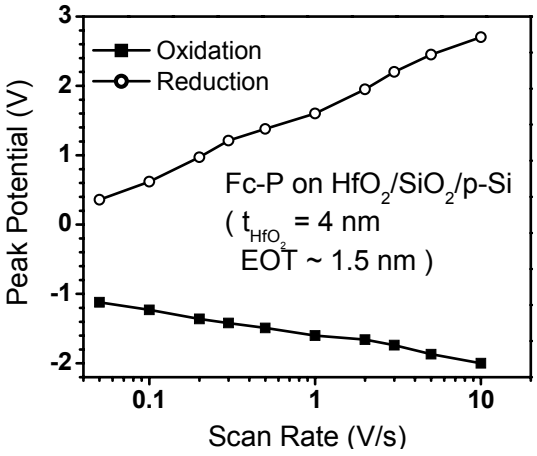


Fig. 10 Redox peak voltage versus Scan rate extracted from CyV of **Fc-P** on HfO_2/SiO_2 on p-Si.

IV. CONCLUSIONS

Hybrid silicon/molecular memory devices were fabricated by incorporating redox-active molecules on HfO_2/SiO_2 tunnel barrier on p-Si substrates. It was demonstrated that by utilizing HfO_2, it is viable to increase the physical thickness of the tunnel barrier to improve charge retention properties of the device with minimal degradation in write speeds as compared to SiO_2. The write/erase voltages and speeds, and the retention properties of these hybrid memory devices can be tuned by engineering the tunnel barrier via asymmetric layered tunnel barriers and also by engineering the Si substrate via asymmetric potential drops in Si surface. Hybrid silicon/molecular memory devices with low-voltage operation and long retention times can thus be realized.

REFERENCES

[1] Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science*, vol. 302, pp. 1543-1545, 2003.

[2] C. P. Collier, E. W. Wong, M. Belohradsky, F. M. Raymo, and J. R. Heath et al., “Electronically configurable molecular-based logic gates,” *Science*, vol. 285, pp. 391-394, Jul. 1999.

[3] J. R. Heath and M. A. Ratner, "Molecular electronics," *Physics Today*, vol. 56, pp. 43-49, 2003.

[4] R. Wolkow, "Toward hybrid devices," *Chemical & Engineering News*, vol. 79, pp. 228-228, 2001.

[5] S. Gowda, G. Mathur, Q. Li, S. Surthi, Q. Zhao, and V. Misra et al., “Hybrid silicon/molecular memories: Co-engineering for novel functionality,” in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2003, pp. 22.1.1-22.1.4.

[6] Q. Li, S. Surthi, G. Mathur, S. Gowda, T. A. Sorenson, and V. Misra et al., “Electrical characterization of redox-active molecular monolayers on SiO_2 for memory applications,” *Appl. Phys. Lett.*, vol. 83, pp. 198-200, Jun. 2003.

[7] S. Gowda, G. Mathur, Q. Li, and V.Misra, unpublished.

[8] S. Gowda, G. Mathur, Q. Li, S. Surthi, Q. Zhao, J. Lindsey, and V. Misra, “Modulation of drain current by redox-active molecules incorporated in Si MOSFETs,” in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2004, pp. 707-710.

[9] G. Mathur, S. Gowda, Q. Li, S. Surthi, S.-I. Tamaru, and V. Misra et al., “Hybrid CMOS/molecular memories using redox-active self-assembled monolayers,” in *Proc. IEEE Nanotechnology*, 2003, pp. 307-310.

[10] G. Mathur, S. Gowda, Q. Li, S. Surthi, Q. Zhao, and V. Misra, “Properties of functionalized redox-active monolayers on thin silicon dioxide – a study of the dependence of retention time on oxide thickness,” *IEEE Trans. Nanotech.*, vol. 4, Mar. 2005.

[11] R. Jha, L. Jae Hoon, B. Chen, P. Majhi, G. Brown, and V. Misra et. al., "Evaluation of Fermi level pinning in low, midgap and high workfunction metal gate electrodes on ALD and MOCVD HfO/sub 2/ under high temperature exposure," in*. IEEE Int. Electron Devices Meeting Tech. Dig*, 2004, pp. 295-298.

[12] A. M. Bond, *Broadening Electrochemical Horizons—Principles and Illustration of Voltammetric and Related Techniques*. New York: Oxford Univ. Press, 2002, pp. 128–151.

[13] E. M. Vogel, K. Z. Ahmed, B. Hornung, G. Lucovsky, J. R. Hauser, and J. J. Wortman et al., "Modeled tunnel currents for high dielectric constant dielectrics," *IEEE Trans. on Electron Devices*, vol. 45, pp. 1350-1355, 1998.

[14] K. K. Likharev, "Layered tunnel barriers for nonvolatile memory devices," *Applied Physics Letters*, vol. 73, pp. 2137-2139, 1998.

-- End of the publication --

3.6 More on Asymmetric Layered Barriers

The usual uniform tunnel barrier cannot simultaneously satisfy conditions of both high write/erase speeds (or low voltages) and high charge-retention (characterized by the leakage through tunnel oxide). Hence, it is necessary to employ graded tunnel barrier fabricated by appropriately varying the band offsets (ϕ) and dielectric constants (k) [9, 10]. This would result in effective lowering of the barrier under an applied bias without significantly reducing the barrier under no-bias condition. The idea behind this concept is to increase the current-voltage slope of the tunnel barrier so as to keep current swing between retention and programming conditions reasonably high at low operating voltages. This barrier lowering effect would mean increase in the storage node program/erase speed with minimal comprise on the charge-retention. However, the realization of ideal graded tunnel barrier is extremely difficult and layered tunnel barrier (stack of dielectric materials) is a realistic approach to this end [9, 10].

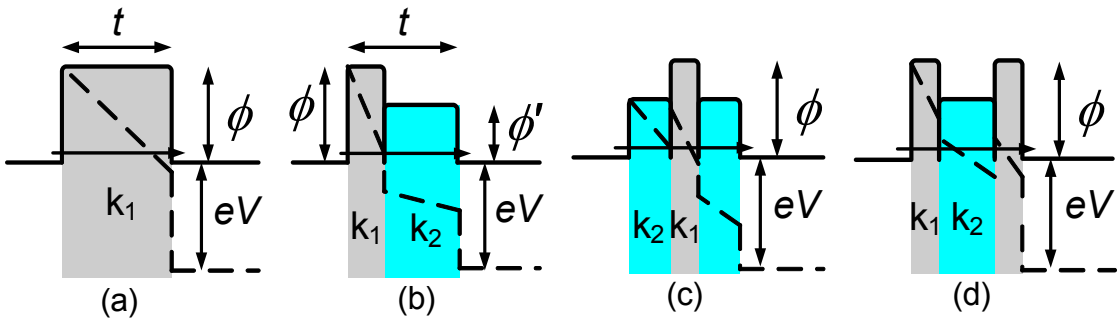


Figure 3.2 Band diagrams illustrating the engineered tunnel barrier concept at flatbands (solid lines) and under applied bias V (dotted lines). It is desirable that in the layered stacks the dielectric material with higher band offset has lower dielectric constant ($k_1 < k_2$) resulting in a larger electric field for a given applied bias. As a result of differences in the band offsets and dielectric constants, there is effective lowering of barrier in the case of layered stacks [**(b)** bi-layer (asymmetric) barrier, **(c)** & **(d)** tri-layer (symmetric) barrier] as compared to single-layer case [**(a)**]. The relative thickness of layers can be appropriately varied to enhance the barrier lowering effect.

As shown in Fig. 3.2 (a) & (b), bilayer (asymmetric) tunnel barrier allows for either lower voltage or higher speed write as compared to single layer barrier, but keeps erase process slow. Symmetric layered tunnel barriers [Fig. 3.2 (c) & (d)] provide for higher erase speeds as well. There have been some proposals, with simulations, of layered stacks with silicon compatible dielectric materials systems for conventional CMOS Flash memory [9, 11, 12], and same concept can be coupled with redox-active molecular elements for the MoleFET Flash applications.

3.6.1 Need for Metal Substrates

The bilayer tunnel barrier has tunneling current which is asymmetric with the electric field direction. A bilayer tunnel oxide stack consisting of HfO_2/SiO_2 was used on p-Si substrate to create asymmetric in the tunneling rates associated with the oxidation and reduction processes of the molecules as discussed previously. However, the observed asymmetry in the redox processes is most likely a cumulative effect of two factors: (i) substrate effect: asymmetric potential drop in Si surface, and (ii) barrier effect: asymmetric tunneling across the barrier. In order to study the later effect exclusively, it is necessary to employ metal substrate as they do not encounter any significant space-charge related potential drops at the surface.

Bilayer stacks of HfO_2 (conduction band offset ϕ_C ~ 1.5 eV, valence band offset ϕ_V ~ 3.4 eV, relatively permittivity k ~ 20 on Si) and Al_2O_3 (ϕ_C ~ 2.8 eV, ϕ_V ~ 2.8 eV, k ~ 8 on Si) are suitable dielectric materials that can be employed in asymmetric layered tunnel barrier investigations on metal substrates. Ultra-thin uniform layers of HfO_2 and Al_2O_3 bilayer (and even tri-layer symmetric) stacks can be fabricated on TiN substrates using atomic layer deposition (ALD) process.

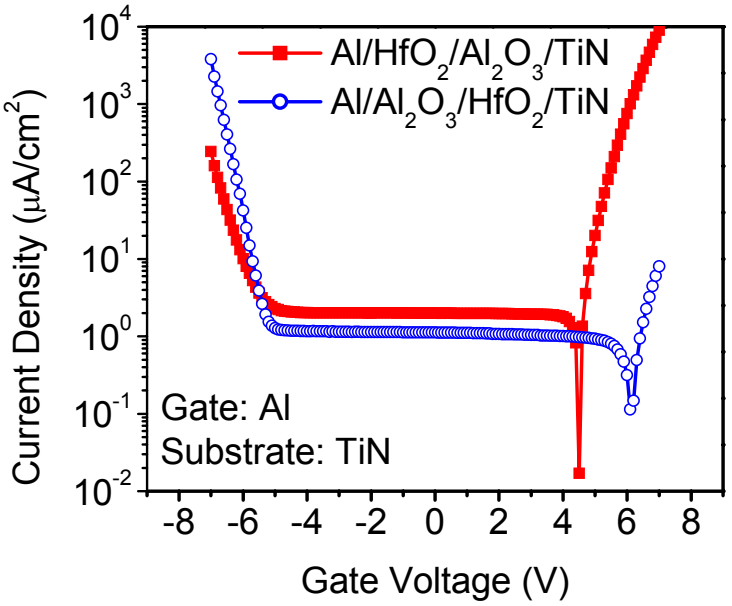


Figure 3.3 Dry DC leakage (IV) measurements of MIM capacitors consisting of HfO_2 and Al_2O_3 bilayer stacks. The target thickness of HfO_2 and Al_2O_3 are around 4 nm and 2 nm, respectively.

Metal-insulator-metal (MIM) capacitors were fabricated incorporating bilayer stacks of HfO_2 (~ 4 nm) and Al_2O_3 (~ 2 nm) on TiN substrate with evaporated Al as gate material, and the asymmetric tunneling properties of the stacks were observed as presented in Fig. 3.3. As expected from the concept and band diagrams presented in Fig. 3.2, the tunneling current (Fowler-Nordheim regime) in case of $Al/HfO_2/Al_2O_3/TiN$ capacitor was significantly higher as compared to $Al/HfO_2/Al_2O_3/TiN$, when electron tunnels from TiN substrate to Al gate (Fig. 3.3). Also, observation consistent with the expectation was made in the reverse polarity further elucidating the asymmetric tunneling across the barrier with respect to electric field direction. This can be coupled with molecule states by incorporating molecules on the bilayer stack to achieve asymmetry in oxidation and reduction rates for the MoleFET device.

3.7 Summary

Electrically stable monolayers of redox-active molecules, two-state ferrocene and three-state Zn-porphyrins, were assembled on Si and Oxide (SiO_2, HfO_2) surfaces by wet chemistry attachment techniques. The ferrocene molecule has single cationic-accessible charge (monopositive) states and Zn-porphyrins have two cationic accessible charge (dipositive) states. The molecules that attach to Si are functionalized with alcohol linker for attachment via Si-O-C covalent linkages and the molecules that attach to SiO2 are functionalized with phosphonate linker for attachment via Si-O-P linkages. Electrical characterization of the molecular monolayer immobilized on Si surface was carried out using DC measurement (cyclic voltammetry) and AC measurement (impedance spectroscopy) techniques.

Redox-active molecules were attached to Si surface of varying doping type and concentration to study the effect of the doping type and concentration on the redox response of the molecules. The redox response is characterized in terms of redox voltages (memory cell write/erase voltages), rate kinetics (memory cell write/erase speeds) and charge retention (memory cell data retention time). Redox peak potentials were found to be lower in case of n-doped Si as compared to p-doped Si. Redox response was independent of the dopant concentration, measurement scan rate and ambient light in case of P-Si. However, in

case of N-Si redox response was strong function of these parameters. Redox peak potential increased with increasing dopant concentration for a given light intensity for N-Si. Also, for a given dopant concentration, redox peak potential was shifted to lower negative gate voltages with increasing ambient light intensity.

It was determined from the experimental observations and analysis that the redox-energy level within the molecules lines up within the valence band edge of the Si, and it exchanges charges with the valence band during redox processes. The differences in the redox response exist in P-Si vs. N-Si substrates due to the state of the Si surface during the redox events in each case. The Si surface is accumulated in case P-Si, while it is depleted in case of N-Si.

The molecule-to-silicon barrier was augmented by placing an ultra-thin layer of tunnel oxide (SiO_2, HfO_2) to enhance charge-retention of the hybrid silicon-molecular devices for Flash applications. The redox properties were studied as function of tunnel oxide thickness, energy barrier and dielectric permittivity. Oxidation peak potential shifted to higher negative gate voltages and the reduction peak potential shifted to lower negative gate voltages with increasing oxide thickness, thereby creating a region of no-redox in the voltage axis, which serves as a window for non-destructive cell read in case of the MoleFET device. In case of P-Si the reduction (erase) process was found to be increasingly rate-limited as compared to oxidation (write) process with increasing SiO_2 thickness. This is attributed to asymmetric tunneling rates mainly due to a lower potential drop across the tunnel barrier for a given gate voltage during reduction process as compared to oxidation, resulting from higher surface potential drop in Si. The disparity in potential drops in Si is attributed to the fact that at higher SiO_2 thickness, the reduction peak potentials are shifted to higher positive gate voltages driving the silicon surface into depletion region.

Increasing SiO_2 thickness (t_{ox}) does increase charge retention but dramatically slows down the redox rate kinetics (or write/erase times) for $t_{ox} > 2.5$ nm. It was demonstrated that by utilizing HfO_2, it is viable to increase the physical thickness of the tunnel barrier to improve charge retention properties of the device with minimal degradation in write speeds as compared to SiO_2. HfO_2 has higher relative permittivity (~20) and has a net lower barrier to holes as compared to SiO_2. A further improvement in speed vs. retention performance trade-off can be made by employing asymmetric or symmetric (trilayer stack) layered tunnel

barriers. ALD deposited layers of ultra-thin HfO_2 and Al_2O_3 are ideal candidates for these barrier engineering investigations.

3.8 References

[1] J. R. Heath and M. A. Ratner, "Molecular electronics," *Physics Today*, vol. 56, pp. 43-49, 2003.

[2] A. M. Bond, *Broadening Electrochemical Horizons: Principles and Illustration of Voltammetric and Related Techniques*: Oxford University Press, 2002.

[3] A. J. Bard and L. R. Faulkner, "Potential Sweep Methods," in *Electrochemical Methods: Fundamentals and Applications*, 2nd ed: John Wiley & Sons, Inc., 2001, pp. 226-260.

[4] F. A. Armstrong, H. A. Heering, and J. Hirst, "Reactions of complex metalloproteins studied by protein-film voltammetry," *Chemical Society Reviews*, vol. 26, pp. 169-179, 1997.

[5] A. J. Bard and L. R. Faulkner, "Butler-Volmer Model of Electrode Kinetics," in *Electrochemical Methods: Fundamentals and Applications*, 2nd ed: John Wiley & Sons, Inc., 2001, pp. 92-107.

[6] Z. M. Liu, I. Schmidt, P. Thamyongkit, R. S. Loewe, D. Syomin, J. R. Diers, Q. Zhao, V. Misra, J. S. Lindsey, and D. F. Bocian, "Synthesis and film-forming properties of ethynylporphyrins," *Chemistry of Materials*, vol. 17, pp. 3728-3742, 2005.

[7] G. Mathur, "Redox-Active Organic Molecules on Silicon and Silicon Dioxide Surfaces for Hybrid Silicon-Molecular Memory Devices," in *Electrical and Computer Engineering*. Raleigh, NC: North Carolina State University, 2005.

[8] K. M. Roth, A. A. Yasseri, Z. M. Liu, R. B. Dabke, V. Malinovskii, K. H. Schweikart, L. H. Yu, H. Tiznado, F. Zaera, J. S. Lindsey, W. G. Kuhr, and D. F. Bocian, "Measurements of electron-transfer rates of charge-storage molecular monolayers on Si(100). Toward hybrid molecular/semiconductor information storage devices," *Journal of the American Chemical Society*, vol. 125, pp. 505-517, 2003.

[9] K. K. Likharev, "Layered tunnel barriers for nonvolatile memory devices," *Applied Physics Letters*, vol. 73, pp. 2137-2139, 1998.

[10] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, and K. De Meyer, "VARIOT: A novel multilayer tunnel barrier concept, for low-voltage nonvolatile memory devices," *Ieee Electron Device Letters*, vol. 24, pp. 99-101, 2003.

[11] J. D. Casperson, L. D. Bell, and H. A. Atwater, "Materials issues for layered tunnel barrier structures," *Journal Of Applied Physics*, vol. 92, pp. 261-267, 2002.

[12] E. Cimpoiasu, S. K. Tolpygo, X. Liu, N. Simonian, J. E. Lukens, K. K. Likharev, R. F. Klie, and Y. Zhu, "Aluminum oxide layers as possible components for layered tunnel barriers," *Journal of Applied Physics*, vol. 96, pp. 1088-1093, 2004.

4 MOLECULES ON SILICON DIODES: SUBSTRATE ENGINEERING

4.1 Introduction

The main focus initially on investigating the redox properties of molecules on Si diodes was to identify the redox pathways in the MoleFET device for a better understanding of the operation of the device. However, the studies of molecules on Si diodes revealed interesting characteristics and opened up new avenues for achieving novel functionalities in the hybrid silicon-molecular devices. It was realized that engineering the substrate (silicon) component of the hybrid devices as complement to molecule engineering may enable access to novel device functionalities and modulate properties of the hybrid device. The discussion on this aspect is presented in a published paper included in this chapter.

One of the device structures that emerged out of the substrate engineering exploration was the N+ or P+ pockets embedded in the P-well or N-well Si substrate. A novel approach to measure lateral conductivity or molecule-to-molecule interactions within the molecular layer was proposed and demonstrated. A second published paper is included in this chapter, which contains the results and discussion on lateral conductivity measurements.

The objectives of the experiments and the exact procedural details of the same are given in the publications included. The next section includes a brief overview of the experimental details about the fabrication of Si diodes and electrical characterization set up used in the studies on substrate engineering.

4.2 Experimental

4.2.1 Fabrication of Si Diodes

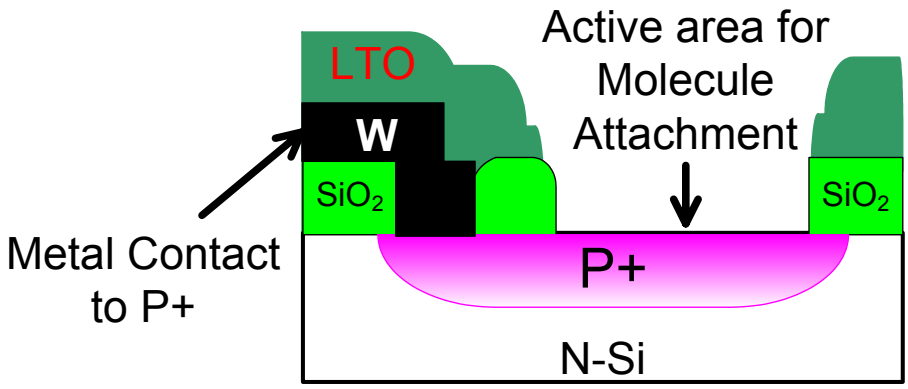


Figure 4.1 Cross-section schematic of P+/N Si diode fabricated using a 5 mask level CMOS process flow based on MoleFlash mask set. N-Si is contacted through back of the wafer and there is a direct metal contact to the P+ doped region. The active area for molecule attachment on P+ is defined by an isolation field oxide.

The Si diodes (N+/P and P+/N) were fabricated using conventional CMOS processing techniques. Fig. 4.1 shows cross-sectional schematic view of P+/N Si diode fabricated using a 5 level mask level CMOS process flow. The mask set that was used for the flow is called MoleFlash. The details of the layout of structures (including diodes) can be found in Appendix 1, and the list of actual process steps including the process parameters is given in MoleFlash process-log as Appendix 2. The MoleFlash mask set also contains the FET structures used in the MoleFET studies, which are discussed in the next chapter. An overview of the process steps is presented in the FET fabrication and the same applies to the diode structures. The P+/N diodes are obtained by PMOSFET fabrication process flow, while N+/P are obtained from the NMOSFET flow.

The N+ pockets in P well structures used in the substrate engineering and lateral conductivity studies were also fabricated using the MoleFlash mask set process flow. These structures are called ratio capacitors and do not have any direct metal contact to the N+ pockets.

The molecules functionalized with alcohol linkers are assembled on these device structures by attachment techniques described in chapter 2.

4.2.2 Electrical Characterization

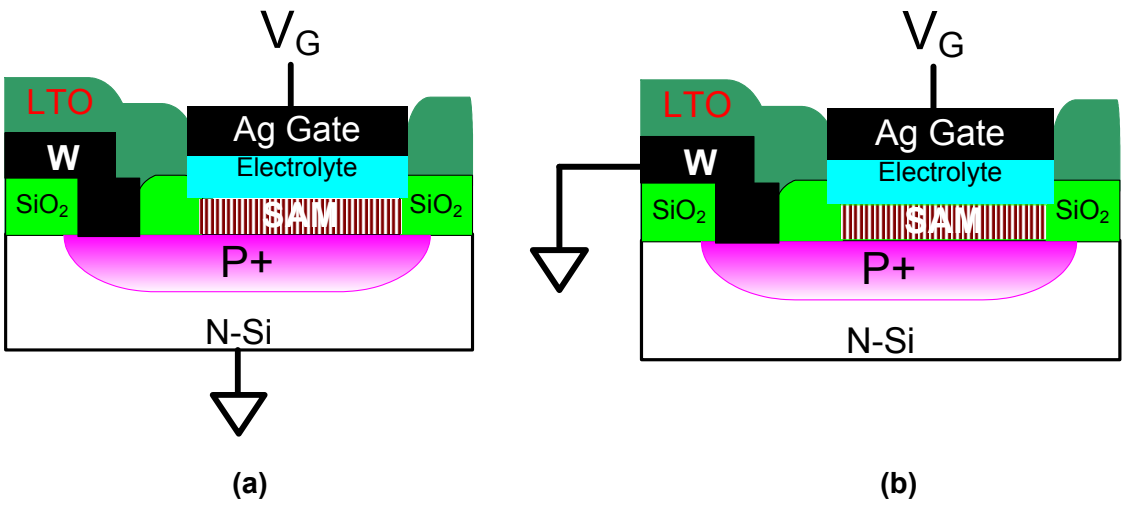


Figure 4.2 Experimental setup for electrical characterization of molecules on: **(a)** P+/N diode, and **(b)** P+ Si.

The diode device structure shown in Fig. 4.1 is used for electrical characterization of molecules on both P+/N Si diode (using back contact) and P+ Si (using the metal contact to P+). Fig. 4.2 shows the experimental setup used for the characterization of the two electrical pathways in the diode structure. Similarly, on the N+/P Si diode structure, electrical characterization of molecules on N+/P Si diode and N+ Si can be carried out. The electrical characteristics of these structures are presented in the next section.

4.3 Ferrocene on Diodes

The discussion on this topic is presented in a publication included in next few pages. It covers the following:

1. Fc-BzOH on N+/P and P+/N : Redox Voltage Tuning
2. Multi-bit using Substrate Engineering
3. Charge-retention Enhancement in Diodes
4. SPICE simulations for Molecules on Diodes

Hybrid Silicon/Molecular Memories: Co-Engineering for Novel Functionality

Srivardhan Gowda[1], Guru Mathur[1], Qiliang Li[1], Shyam Surthi[1], Qian Zhao[1], Jonathan Lindsey[2], Ken Mobley[3], David F. Bocian[4] and Veena Misra[1]

1. Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695 USA
2. Department of Chemistry, North Carolina State University, Raleigh, NC
3. Zettacore Inc. Denver, Colorado 80222, USA
4. Department of Chemistry, University of California, Riverside, CA 92521, USA

Tel 919-515-7356 Fax 919-515-5055 email: vmisra@ncsu.edu

This paper appears in: Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International.
Publication Date: 8-10 Dec. 2003
On page(s): 22.1.1 - 22.1.4

Abstract

The properties of silicon in hybrid CMOS/molecular capacitors were successfully engineered to produce multiple bit and long retention-time devices. Charge storage molecules were attached to silicon substrates to produce multiple bit and long retention time characteristics that may be attractive for nanoscale high density memory applications.

Introduction

A hybrid silicon/molecular approach, where molecules are integrated with silicon devices, can provide a bridge between CMOS-only and future molecular-only technologies [1-4]. The advantages of molecular-based memory devices include nanoscale size, low voltage operation and multiple-state properties. Multiple-state behavior can be built into the molecular structure via molecular design and chemical synthesis. For example, the porphyrin molecule shown in Fig. 1(a) exhibits three states: neutral, monopositive, and dipositive [5]. More elaborate molecular structures have been devised that afford up to seven positively charged states [6]. A complementary route to obtain multiple states entails the use of relatively simple molecules (with as few as two states) in conjunction with engineered substrates.

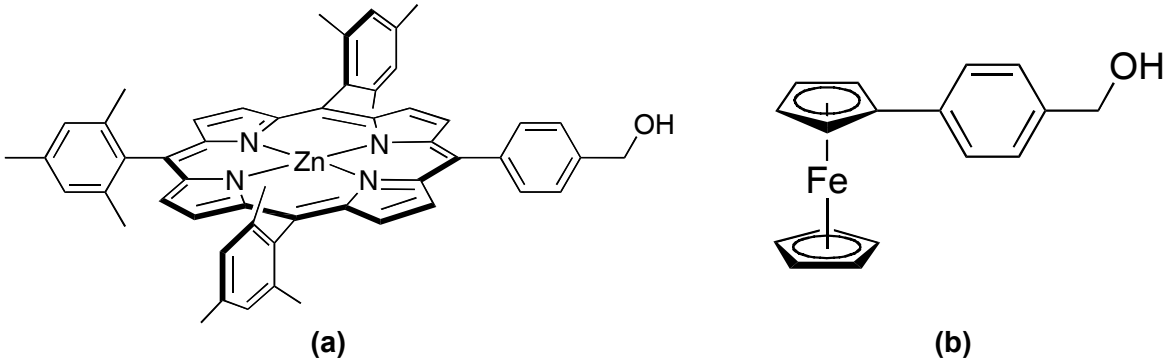


Fig. 1 (a) Molecular structure of an alcohol-derivatized Zn tetraarylporphyrin. **(b)** Molecular structure of **Fc-BzOH**.

In this work we report on the use of N+ (or P+) pockets embedded in p-well (or n-well) Si substrates as a means of obtaining multiple states from a two-state molecule. Another critical parameter for memory devices is charge-retention time. Values of the retention time can also be tuned by alterations of the molecular design [7,8]. In this work we also report on utilizing N+/P and P+/N diodes to increase the charge-retention times of redox-active monolayers. Both of these strategies illustrate engineering of the silicon component in hybrid silicon-molecular devices. We believe that co-engineering both the silicon and molecular components will enable access to novel device functionalities that may not be possible with silicon or molecular devices alone.

Experimental

The redox-active compound used in this study was 4-ferrocenylbenzyl alcohol (**Fc-BzOH**), the structure of which is shown in Fig. 1(b). The ferrocene unit exhibits two states: neutral and monopositive.

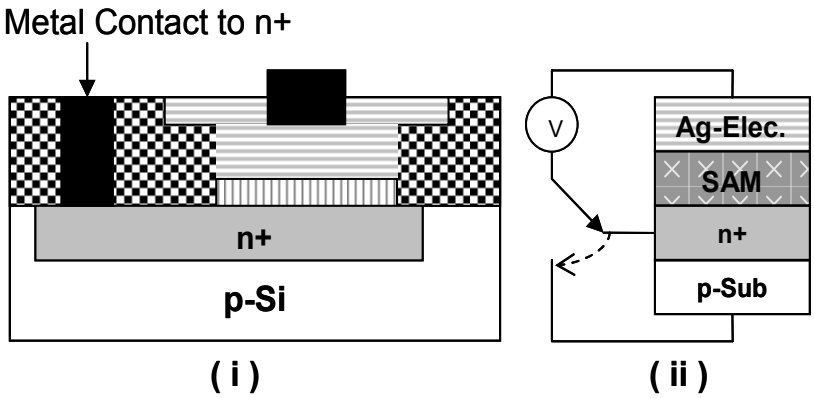


Fig. 2 (i) Schematic of an n+/p diode structure, with a self-assembled monolayer of **Fc-BzOH** attached on the n+. Gate electrolyte and Ag electrode are also shown. There is a metal contact to the n+ layer through the isolation SiO_2. **(ii)** Schematic equivalent of the electrical connections made during characterization. Note that one end of the voltage source is connected to the silver electrode, while the other end is either connected to the n+ contact or the p-substrate (back side contact).

A schematic of the basic molecular capacitor structure is shown in Fig 2. The architecture of the capacitor contains electrolyte-molecule-silicon layers, denoted EMS. Arrays of N+ (P+) regions were formed in p-well (n-well) with varying area ratios (Table 1a). In addition, N+/P and P+/N diodes, and N and P area capacitors were also fabricated. The ferrocene and porphyrin molecules of the type shown in Fig 1 have demonstrated excellent thermal stability (up to 200–400 °C), excellent endurance, long retention times, high densities and low voltage redox potentials [4-10]. The solution used to form a monolayer on silicon was prepared by dissolving 1 mg of Fc-BzOH in 200 µL of benzonitrile. The sample was maintained at 100 °C during the attachment procedure which has been described previously [5]. Electrical analysis was performed using a CHI 600 electrochemical analyzer and an HP 4284A LCR meter. Characterization of charge-retention times was done by the open circuit potential amperometry (OCPA) technique using National Instruments LabVIEW and a UCR High-Bandwidth Current Monitor [7].

Results and Discussion

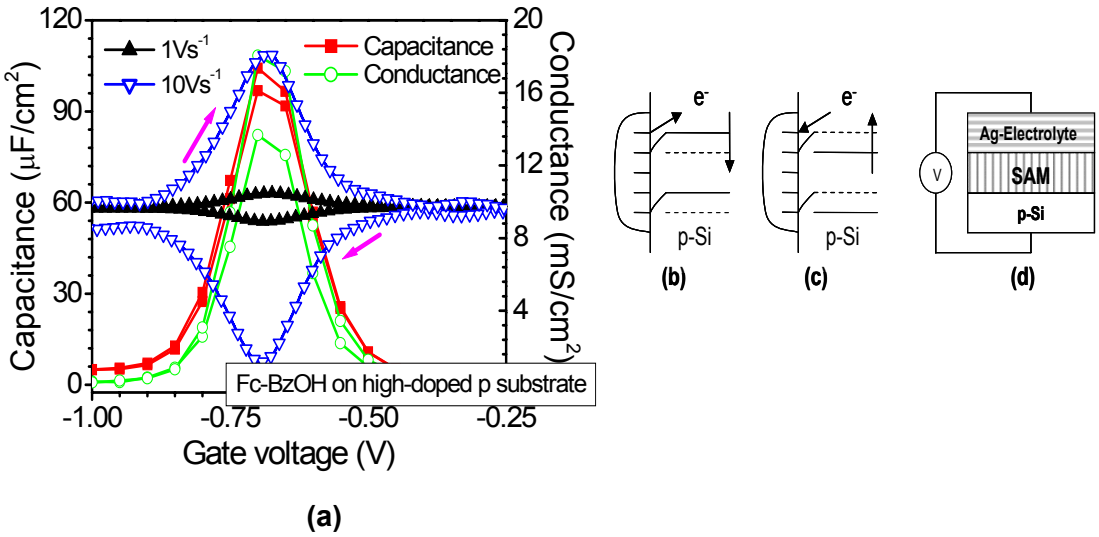


Fig. 3 (a) Cyclic voltammetry (CyV), capacitance and conductance voltage (CV and GV) of **Fc-BzOH** on high-doped p type substrate. Peaks in CV and GV correspond to those in CyV. **(b)** and **(c)** Energy band diagrams for oxidation and reduction of the molecules respectively. The former corresponds to the read cycle while the latter corresponds to the write cycle. **(d)** Schematic equivalent of the electrical connections for characterization.

Cyclic voltammetry (CyV) and conventional capacitance-conductance (CV-GV) measurements were performed to characterize the **Fc-BzOH** attached to high-doped p-Si substrates. As shown in Fig. 3(a), the peaks observed at -0.65V for all measurements are associated with the oxidation and reduction (redox) processes of the molecules. As shown in Fig. 3(b), the application of an oxidizing voltage causes each molecule to lose an electron to the Si substrate, resulting in a positively charged monolayer (written state). When a reducing voltage is applied, electron-transfer returns the molecules to the neutral state (erased state). The charge stored in the oxidized monolayer can be read either destructively by erasing and measuring the discharge current or non-destructively via a field effect transistor.

Fc-BzOH SAMs also were prepared on low-doped n or p substrates. In each case, the CyV measurement shows the expected redox peaks (Fig. 4). However, the oxidation peak potential is ~350mV lower for n-Si than for p-Si. This observation is attributed to the alignment of the molecular Fermi level and the Fermi level of the surface, which is different

for n and p-Si. In addition, any voltage drops that associated with the contacts to these low doped substrates can also shift the redox potentials.

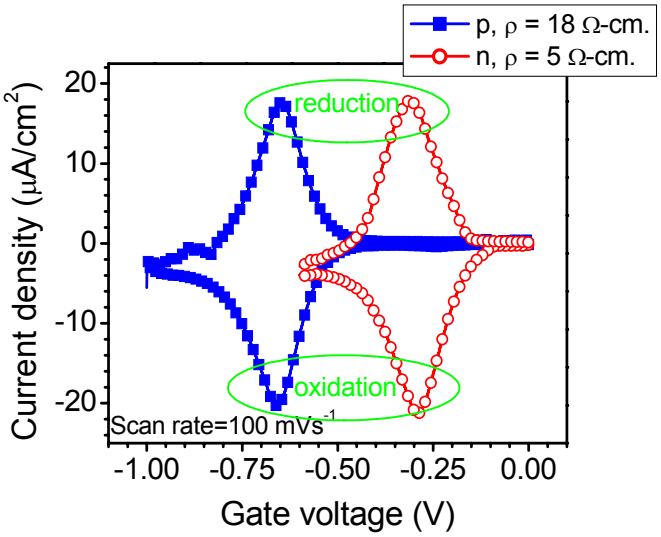


Fig. 4 CyV of **Fc-BzOH** attached to low-doped n and p type substrate at a scan rate of 100 mV/s.

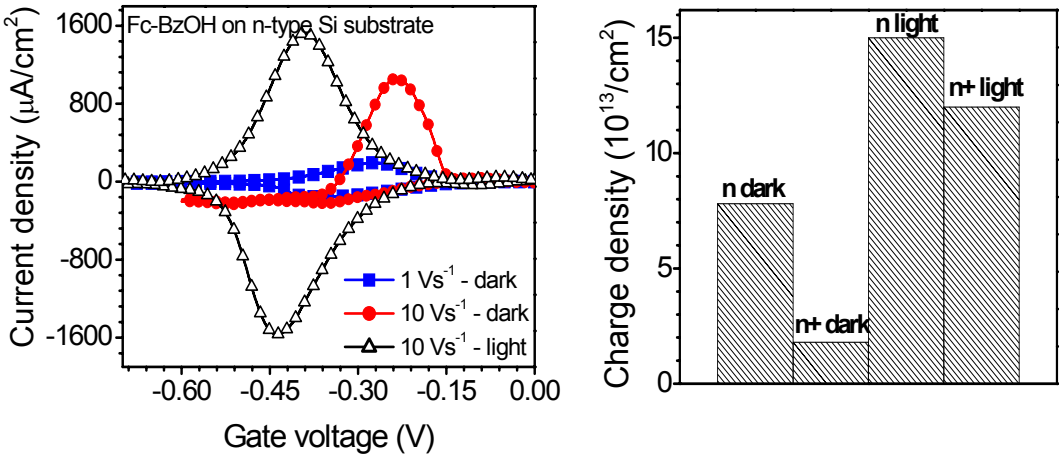


Fig. 5 CyV of **Fc-BzOH** on low-doped n type substrate: effect of scan rate and light on minority carrier generation and hence the oxidation peak.

Fig. 6 Effect of light and doping density on oxidation of monolayer of **Fc-BzOH** on n substrate: charge density from CyV at 10 V/s.

The effect of the number of minority carriers in n-Si on the writing and erasing processes was examined in two ways, i) by altering the scan rate and ii) by illuminating the sample. As shown in Fig. 5, when the scan rate is increased from 1 Vs^{-1} to 10 Vs^{-1}, the

oxidation peak shifted to a lower potential value and increased in intensity. Upon full illumination, the peak increased further in intensity and shifted to a higher potential value. Because the writing process requires that the electrons leaving the molecules recombine with holes in the substrate, the n-Si requires a source of minority carriers when the scan rates are high. The effects of illumination must originate with the underlying Si layer and not the **Fc-BzOH** monolayers. The dependence of observed redox behavior on minority carrier generation is shown in Fig. 6. As shown, the amount of charge measured is lower under dark conditions and for heavily doped substrates both of which are conditions that reduce minority carrier concentration.

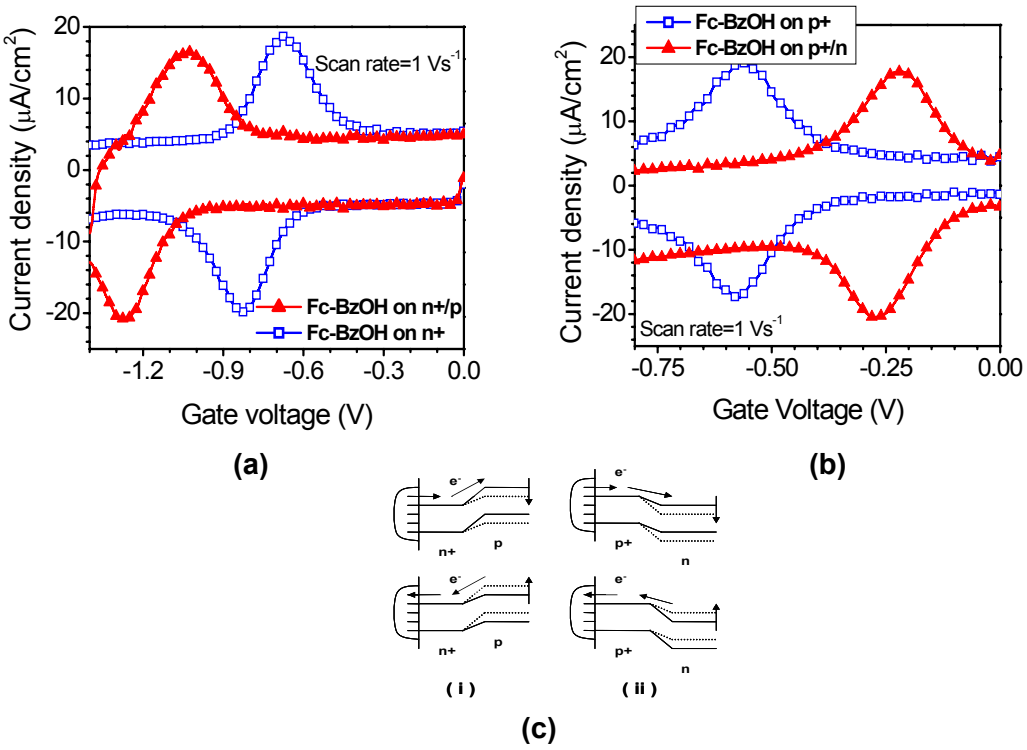
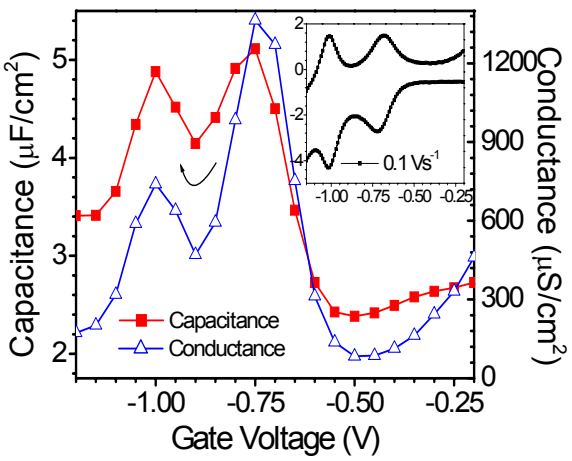


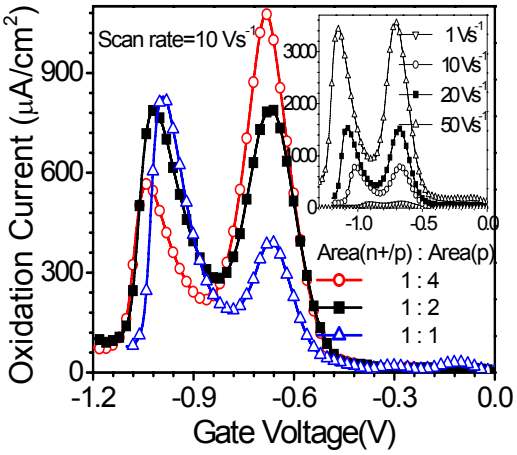
Fig. 7 (a) CyV of **Fc-BzOH** on n+ and n+/p diode: effect of forward-biased diode characteristics on redox peak potentials. Doping density of the n+ region is in the order of 1×10^{21} cm^{-3}. (b) CyV of **Fc-BzOH** on p+ and p+/n diode: effect of reverse-biased diode characteristics on redox peak potentials. Doping density of the p+ region is in the order of 1×10^{21} cm^{-3}. **(c) (i)** and **(ii)** Band diagrams for redox processes of molecules attached to n+/p and p+/n diode structures respectively. The top and bottom figures represent the oxidation process and reduction processes, respectively. The top arrows indicate the direction of electron flow and the side arrows indicate the movement of the energy levels as the voltage is scanned during the redox processes.

The effect of forward-biased diode characteristics on redox characteristics of **Fc-BzOH** monolayers (attached to n+/p diodes) was examined. Fig. 7 (a) shows that a

negative shift of ~450mV is observed in the redox potentials when **Fc-BzOH** monolayers are attached to n+/p diodes, compared with attachment directly on p substrates. This shift is associated with the voltage drop occurring across the diode (the oxidation process does not require the diode to be fully on to initiate). On the other hand, a positive shift of ~300mV is observed in the redox peak potential of the **Fc-BzOH** monolayers attached to p+/n diodes (Fig. 7 (b)). The direction of the shift is associated with the reversal of the direction of the built-in potential of the p+/n diode (Fig. 7 (c)). This result suggested that the shifts in potential could be exploited in memory devices.



8



9

Fig. 8 CV and GV of **Fc-BzOH** on capacitor structure with parallel paths of p and n+/p. Two peaks correspond to redox of molecules through the two parallel paths. Inset: CyV (current density vs. gate voltage) of the structure at a scan rate of 100 mV/s.

Fig. 9 Oxidation current density from CyV of **Fc-BzOH** on capacitors with parallel paths of p and n+/p. The ratio of the areas of n+/p and p varies from 1:1 to 1:4. Scan rate is 10 V/s. Inset: Oxidation current for a particular ratio (1:2) of n+/p and p at varying scan rates.

To take advantage of these shifts in potential, we prepared **Fc-BzOH** monolayers in structures with n+ pockets embedded in a p-well (or p+ pockets embedded in an n-well). CV-GV and CyV measurements of n+ pockets in a p-Si capacitor shows two distinct redox peaks (Fig. 8). The two peaks are attributed to two parallel paths of electron transfer: 1) electron transfer between molecules and p-Si and 2) electron transfer between molecules and n+/p-Si diodes (Table 1 (a)). The existence of two redox peaks illustrates the existence

of independent parallel EMS paths. In addition, these results indicate that the molecules are discrete and do not conduct to a significant degree in the lateral direction. The absence of lateral conduction (versus conduction with the surface) is not surprising given the discrete nature of the molecules, the absence of lateral connections between molecules, and the presence of a tether between the molecules and the surface.

The relative magnitudes of the oxidation peak current are obtained from the CyV measurements. As indicated in Fig. 9, the peak intensities are proportional to the relative areas of the n+ and p- Si regions. For p+ pockets in n-well, only one peak is observed since both p+/n and n-Si have the same peak potential, as seen in Table 1 (a).

Structure	Peak potential (V)	
n	0.32	
p	0.67	
n+/p	1.08	
p+/n	0.32	
n+/p : p :: 1:1	1st peak 0.67	2nd peak 0.99
n+/p : p :: 1:2	0.67	1.02
n+/p : p :: 1:4	0.68	1.04
p+/n : n :: 1:1	0.35	

(a)

Structure	Charge density (10^{14}/cm^2)		
	1st peak	2nd peak	Total
n+/p : p :: 1:1	0.35	0.65	1.00
n+/p : p :: 1:2	0.60	0.50	1.10
n+/p : p :: 1:4	0.90	0.30	1.20
p+/n : n	1.40	-	1.40

(b)

Table 1 (a) Peak potentials for **Fc-BzOH** on various structures. Two peaks appear for the capacitor structures with parallel paths of n+/p and p, corresponding to the two parallel paths. **(b)** Redox-active charge density for **Fc-BzOH** on capacitor structures with varying ratios of n+/p and p (or p+/n and n). Two peaks appear for the capacitor structures with parallel paths of n+/p and p, corresponding to the two parallel paths. Charge densities are calculated by dividing the area under peak by the active area (100 μm^2) times the electronic charge. Charge densities obtained on n or p substrate ~ 1.3×10^{14} cm^{-2}.

The effects of scan rate on redox behavior of the **Fc-BzOH** monolayers on n+/p diode structures is shown in Fig. 10 (a). At scan rates higher than 5 V/s, the reduction current decreased for molecules attached to n+/p diodes. To evaluate whether the lack of the reduction current also impacted the subsequent oxidation, various wait times were implemented between scans where 1 scan cycle includes oxidation and reduction. As shown in Fig. 10 (b), a decrease in the wait time between cycles resulted in a commensurate decrease in subsequent oxidation current. Indeed, continuous scanning revealed that after the disappearance of the reduction current, the next oxidation current was minimal. Similarly, the use of light to modulate the number of minority carriers altered

the observed redox characteristics with scan rate and/or wait time between scans (Fig. 10 (c)). As light intensity was increased, the subsequent oxidation currents were found to match the initial currents. The mechanism leading to the above observations will be discussed in the next section.

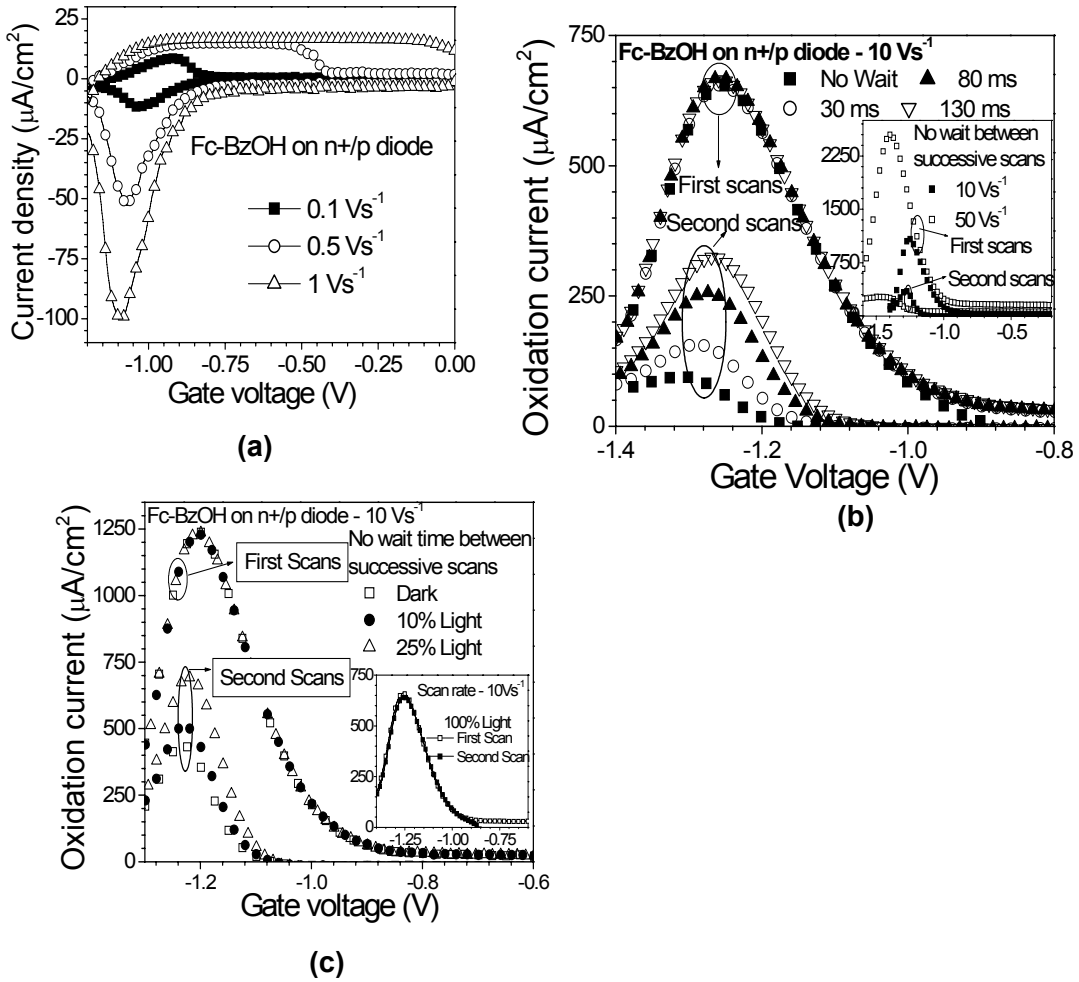


Fig. 10 (a) CyV of **Fc-BzOH** on n+/p diode structures at varying scan rates: effect of scan rate on reduction. **(b)** Effect of wait time between scans on oxidation of **Fc-BzOH** on n+/p diode structures. The gate was at a potential less negative than the reduction potential during the wait time between scans. The oxidation peak in the second scan is lower than that in the first, but increases with increasing wait time. Inset: Oxidation current at two different scan rates, 10 V/s and 50 V/s, with no wait time between subsequent scans at each scan. **(c)** Effect of light on oxidation current density of **Fc-BzOH** on n+/p diode structures. The oxidation current in the second scan increases with increasing light intensity. Inset: Oxidation current density remains the same in the second scan when the light intensity is 100%.

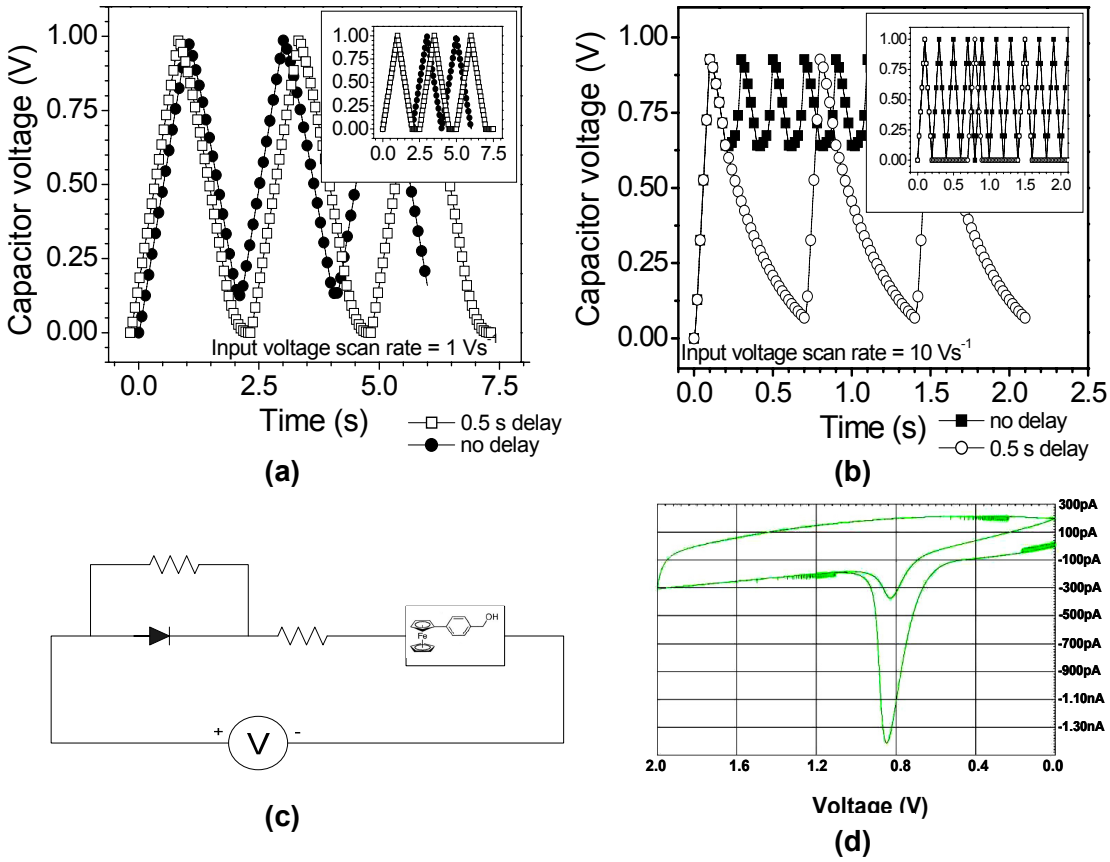


Fig. 11 (a), (b) Hspice simulations of the voltage across the capacitor as the input is scanned from 0 to 1 V, at a scan rate of 1V/sec (Fig. 11 (a)) and 10 V/s (Fig 11 (b)). Two different wait times (0 and 0.5sec) are used. Inset shows the input signal. **(c)** HSpice circuit model used for **Fc-BzOH** attached on diode structures. The monolayer along with the electrolyte was modeled as a capacitor with a small resistance in series. The resistance in parallel to the diode was added to accommodate leakage in real diodes. **(d)** Simulation plots from a series combination of Zettacore spice model for **Fc-BzOH** and the diode structures. Two successive scans of CyV at a scan rate of 10 V/s with no wait time between scans. Voltage shown is at the substrate and not at the gate.

Spice simulations were performed on the basis of the results shown in Figs. 7-11. The simulations revealed that during the on (oxidizing) sweep, the voltage across the capacitor rapidly reaches the input potential because the diode is conducting; however, during the off (reducing) ramp, the capacitor discharge is limited by the diode reverse leakage. For example, longer wait times, slower scan rates or illumination will allow the capacitor to discharge, thereby allowing the molecules to reduce (Figs. 11 (a),(b)). However, under very fast ramps, the capacitor is now allowed to discharge and therefore a reducing voltage will not develop across the molecules. This can be a very attractive route to achieve

non-volatile memory. To prove the above mechanism, a Zettacore spice model (Fig. 11 (c)) for the **Fc-BzOH** monolayer was modeled in series with the diode structures. The simulations were in good agreement with experimental observations, as shown in Fig 11d. The charge-retention times (measured via OCPA techniques [7]) indicate that the **Fc-BzOH** monolayers on n+/p-Si diodes had $t_{1/2}$ values of 200 seconds as compared to 80 seconds for molecules attached to directly to p-Si capacitors. This indicates that the reduction processes are suppresses in diode structures thereby increasing retention times.

Conclusions

The properties of silicon in hybrid CMOS/molecular capacitors were successfully engineered to produce multiple bit and long retention-time devices. Such hybrid silicon-molecular approaches may enable solutions for nanoscale high density, low voltage, long retention and multiple-bit memory applications.

References

[1] K.M.Roth et al., J.Vac. Sci. Technol. B 18 (2000).

[2] C.P.Collier et al., Science 285 (1999).

[3] S.K.Coulter, J.Vac.Sci.Technol. A 18 (2000).

[4] K.M.Roth et al., J.Am.Chem.Soc., Vol. 125 (2003).

[5] D.T.Gryko et al., J.Org.Chem., 64 (1999).

[6] K. Schweikart, et al., J. S. *J. Mater. Chem. 12,* 2002.

[7] K.M.Roth et al., Langmuir 18 (2002).

[8] G.Mathur et al., IEEE Nano2003.

[9] Q.Li et al.,Appl.Phys.Lett., Vol. 81(2002).

[10] Q.Li et al.,Appl.Phys.Lett., Vol. 82(2003).

- end of publication –

4.4 Porphyrins on Diodes

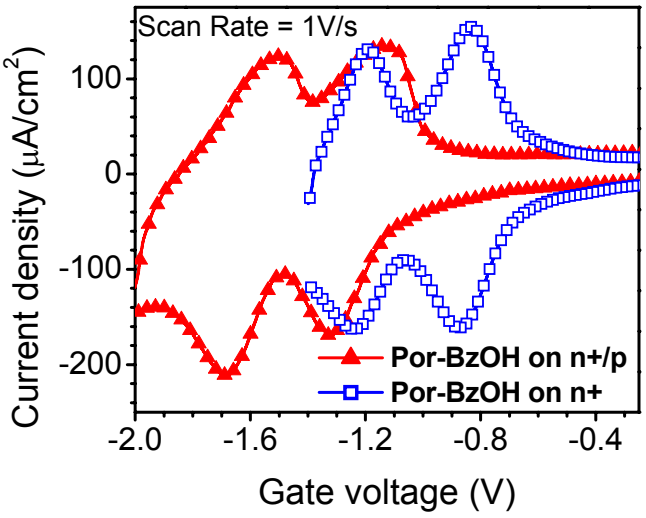


Figure 4.3 CyV of **Por-BzOH** on N+ and N+/P diode: effect of forward-biased diode characteristics on redox peak potentials.

As discussed previously, the redox peak potential of ferrocene (Fc-BzOH) was shifted to higher negative gate voltage by using N+/P diode. The shift was attributed to the built-in potential of the diode that needs to be overcome for holes to diffuse from P to N+ region. The holes are required to combine with the electrons injected from the molecules that are oxidized (lose election). To further confirm the redox-potential tuning using diodes, three-state (two redox-charge states) porphyrin (Por-BzOH) molecules were attached to N+/P diode structures, which were described earlier. A negative shift of ~ 450 mV was observed in the redox potentials of Por-BzOH monolayer attached to N+/P diode, compared to directly on P substrate, as can be seen in Fig. 4.3. This is similar to the observations with Fc-BzOH on diodes presented earlier.

4.5 A Note on Band Diagrams

In the discussion on ferrocene on Si diodes included in the publication, the band diagrams for redox-charge transfers were presented assuming the redox-energy state communicates with the conduction band in Si i.e., the molecules exchanges electrons into and from conduction band in Si during oxidation and reduction, respectively. However, it was determined at a later point of time, that redox-energy state in the molecule aligns deep

within the valence band edge of the Si and exchanges charges with the valence band during redox processes, as discussed in chapter 3. In light of this revelation, the band diagrams are corrected as shown in Fig. 4.4.

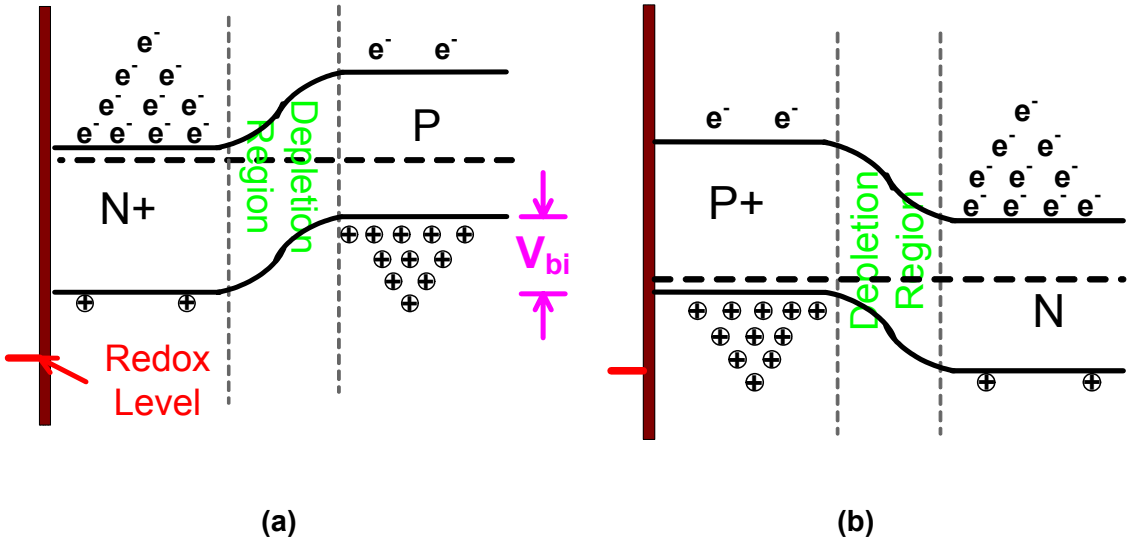


Figure 4.4 Band diagrams for redox-level line up with Si diodes at no external applied bias for: **(a)** molecules attached to N+/P diode, and **(b)** molecules attached to P+/N diode.

In case of the molecules attached on N+/P Si diode (Fig. 4.4 (a)), the oxidizing potential drives the diode into forward-bias regime, thereby causing diffusion of the holes from valence band of the P-Si into that of N+ Si. However, for the diffusion of holes across the depletion region of the diode, the built-in potential (V_{bi}) has to be overcome. Hence, the applied gate potential needs to accommodate V_{bi} in addition to the drop across the molecules to cause oxidation (molecule losing electron into Si). The holes diffusing from the P-Si are required to recombine with the electrons tunneling into Si from the redox-state for oxidation of the molecules. This is the reason for the redox potentials of the molecules on N+/P diode to be shifted to higher negative gate voltage as compared to just P-Si substrate.

In case of the molecules attached to the P+/N Si diode (Fig. 4.4 (b)), the oxidizing potential drives the diode into reverse-bias regime further extending the depletion region. Although the direction of the electric field across the depletion region is to push the holes in the valence band at the interface of depletion region and N-Si region towards the P+ region, the valence band of N-Si is devoid of holes. This is similar to just the N-Si case discussed in chapter 3. So the electron-hole pairs have to be generated in the depletion region by

external (optical) excitation and this is also associated with photo-voltage generation across the depletion region as in case of N-Si. The polarity of the photo-voltage is in the direction of aiding the oxidation process i.e., positive on the P+ side and negative on N side. Hence, the optical excitation generates the holes in the valence band needed to recombine with the electrons from the molecules during oxidation and also shifts the oxidation potential to a lower negative voltage. This is the reason for the redox potentials of the molecules on P+/N diode to be shifted to lower negative gate voltage as compared to just P-Si substrate.

4.6 N+ Pockets in P-Si Well

As discussed earlier in the publication, ferrocene was attached to N+ pockets in P-Si well to create parallel redox paths associated with the N+/P diode and P-Si regions. There were two novel utilities proposed and demonstrated of this structure, namely,

1. Multiple-bits by engineering the Si (substrate).

2. Lateral conductivity detection in the redox-active layer.

The second utility of the structure is explored more in detail in this section and is presented in a publication included below.

Approach for investigating lateral conduction in self-assembled monolayers

Srivardhan Gowda, Guru Mathur, Qiliang Li, Shyam Surthi, and Veena Misra[1]

Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695 USA

This paper appears in: APPLIED PHYSICS LETTERS 87, 262115 (2005)

Received 15 April 2005; accepted 28 October 2005; published online 29 December 2005

Abstract

Lateral conductivity within a monolayer is a key factor in the implementation of emerging dense molecular memory devices since it determines the degree of cross talk between cells. Lateral interactions within a monolayer could also lead to loss of charge through defective sites. Existing characterization techniques are limited to probing the electrical communication between molecules and attached electrodes. In this paper we demonstrate a test structure consisting of n type and p type doped silicon islands to isolate vertical conduction from lateral conduction. This structure is a useful characterization tool for tailoring the intrinsic properties of the molecules for information storage.

 (DOI: 10.1063/1.2152112)

Recently, many molecules with interesting charge conduction and charge storage properties have been proposed for potential use in electronic devices.[1,2] The electron transfer rate from the molecules within the monolayer to the attached substrate has also been well characterized and found to be strongly dependent on the intrinsic molecular properties.[1,3] Although the electron transfer rate studies result in providing fundamental insight about the molecule-substrate interactions, they do not reveal the characteristics of intermolecular or lateral conductivity of the molecules within the monolayer. Understanding the interaction between molecules is critical since the presence of lateral conductivity in molecular memories would lead to a loss of charge in the form of crosstalk in dense memory arrays or charge loss through defective sites present in the monolayer. There have been several efforts to evaluate lateral conduction in self-assembled monolayer films of conductance-based molecules.[4,5] However, these methods were not successful due to the requirements of the very low current detection limit and better molecule-electrode contact.[4] In addition, scanning tunneling microscopy-based measurements failed to separate out the vertical and horizontal current components.[5] Although Majda et al., have studied lateral electron transport in redox-active molecular assemblies, the observed conductivity was essentially attributed to the diffusion of the loosely bound charge carriers in the polymer or in the bilayer.[6,7] An extension of similar work utilizing nanocrystalline metal oxide films on conducting support could not rule out, on a theoretical basis, the electroactivity of the redox-active molecules with the metal oxide film effectively failing to decouple vertical and lateral conduction pathways.[8] Also, the issue of redox-active molecules getting adsorbed on the conducting support was not addressed, which could contribute heavily to the observed redox activity. Therefore, to date no efficient and reliable techniques to quantify lateral conductivity mechanism have been demonstrated.

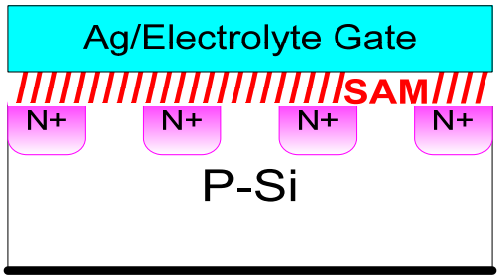


FIG. 1. Schematic of the device structure to detect lateral conduction in a self-assembled monolayer (SAM). It consists of two dimensional array of N+ pockets embedded in p-well silicon substrate. The ratio of areas of N+ and P regions has been varied.

In this paper, we have built and utilized a silicon-based device structure that can detect lateral conductivity between individual molecules present in a self-assembled monolayer. In this structure, the attached surface consists of a collection of *N*-doped and *P*-doped islands that can effectively decouple vertical conductivity from the lateral conductivity of a monolayer. The arrays of doped islands are representative, in configuration and dimensions, of cells of dense molecular memory arrays, thus making the device presented here relevant for investigation of lateral charge transfer and crosstalk in molecular memories. The device structure is useful in evaluating intermolecular interactions in immobilized monolayer films with a low lateral to vertical conductivity ratio, which is the key requirement in the case of molecular films for information storage. As shown in Fig. 1, the structure consists of phosphorus-doped pockets (*N*+) implanted within a boron-doped silicon well (*P*-Si). The number of *N*+ pockets within the *P*-Si was varied to change the area of the *N*+ regions relative to the *P*-Si regions while keeping the total area constant. In addition, *N*+ /*P* diode structures were also fabricated as controls wherein both the *P* substrate and the *N*+ regions had separate contacts (Fig. 2).[9]

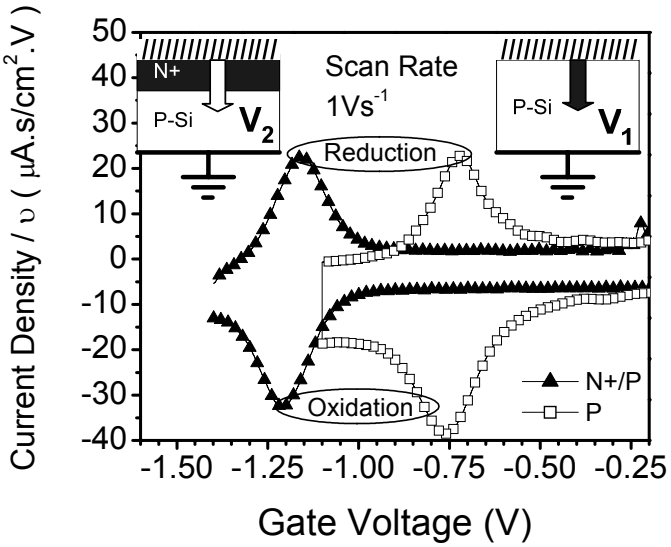


FIG. 2. Cyclic voltammetry (CyV) of Fc-BzOH attached to *P*-Si and *N*+/*P*-Si substrates with the right and left insets showing the respective device schematics. The voltages $\mathbf{V_1}$ and $\mathbf{V_2}$ correspond to the redox potentials of the **Fc-BzOH** attached to *P*-Si and *N*+ /*P*-Si substrates, respectively.

The molecules selected for this study are redox-active ferrocenyl-benzyl alcohol (**Fc-BzOH**), which have been shown to form highly dense, covalently bonded self assembled monolayers (SAMs) on silicon substrates with low oxidation potentials.[1,10] The solution used to form a monolayer of the redox-active compound on silicon was prepared by

dissolving 1 mg of Fc-BzOH in 200 μl of benzonitrile. The samples were maintained at 100 °C during the attachment procedure in an argon-purged environment. For electrical characterization, a solution of 1.0 M tetrabutylammonium hexafluorophosphate in propylene carbonate was used as conducting gate electrolyte and a silver wire served as the counter/reference electrode. Electrical characterization of the monolayer was performed via cyclic voltammetry[11] using a CHI 600A electrochemical analyzer. Control samples consisting of just P-Si substrates were also used.

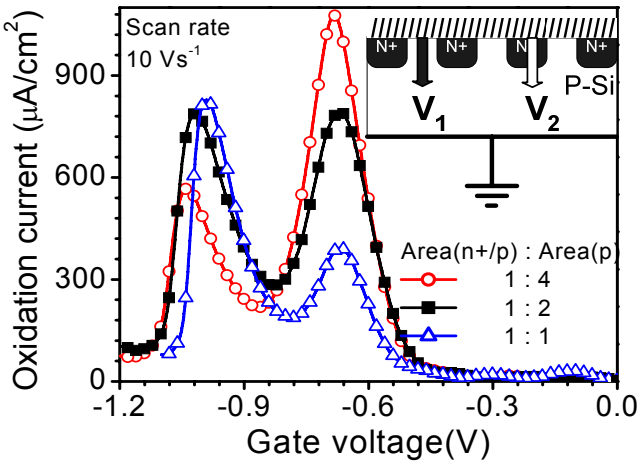


FIG. 3. Oxidation current density from CyV of **Fc-BzOH** on the device structures with varying ratios of the areas of *N*+ /*P* and *P* regions. Two peaks correspond to the redox of the molecules through the two separate routes namely, *P*-Si and *N*+ /*P*-Si with redox potentials $\mathbf{V_1}$ and $\mathbf{V_2}$, respectively. The inset shows the existence of two independent routes for the redox of the molecules attached on the structure.

The cyclic voltammetry (CyV) of **Fc-BzOH** on *P*-Si and on *N*+ /*P*-Si diodes are shown in Fig. 2. As seen, the oxidation of molecules attached to *N*+ /*P*-Si are shifted to higher potentials ($\mathbf{V_2}$) as compared to molecules attached to *P*-Si ($\mathbf{V_1}$). This shift is attributed to the barrier that arises due to built-in potential of the diode that is formed within the substrate when *N*+ region is implanted in the *P*-Si.[9] Next, the **Fc-BzOH** molecules were attached to samples containing *N*+ pockets within a *P*-Si well (island structure). As shown in the inset of Fig. 3, in this configuration, the molecules have two potential routes for oxidation: (i) through the *P*-Si at a potential of $\mathbf{V_1}$ and (ii) through the *N*+ /*P*-Si pockets at a potential of $\mathbf{V_2}$. If the molecules laterally communicate with each other, then as soon as the applied voltage reaches $\mathbf{V_1}$, all the molecules would oxidize through the *P*-Si regions. On the other hand, if the molecules do not laterally communicate with each other, then two separate

and independent routes are expected, one through *P*-Si at $\mathbf{V_1}$ and another through *N*+ /*P*-Si at $\mathbf{V_2}$. As shown in Fig. 3, indeed two separate and independent peaks are observed with the above structures suggesting that lateral communication between the molecules is negligible. Furthermore, as the area of the *N*+ region is increased relative to the *P*-Si, it is found that the amplitude of the second peak increases in proportion to the increasing *N*+ area. This also confirms that the molecules in the monolayer are evenly spaced out without any significant aggregations or vacant sites, as has been shown previously.[1] The presence of such defects in significant numbers will introduce an additional charge transfer mechanism similar to that in macromolecular systems that will limit the ability to accurately quantify lateral conduction. The peak potential of the first peak is close to the value of $\mathbf{V_1}$, whereas the peak potential of the second peak is slightly lower than the value of $\mathbf{V_2}$. The difference observed in these potentials will be discussed later. These measurements confirm that the lateral conductivity in this monolayer is suppressed and these molecules behave as discrete and independent entities. In addition, this structure also allows the splitting of a single redox peak into two separate peaks which may have applications in multiple bit memories.

Even though the above results suggest that lateral conductivity is negligible under the selected measurement conditions, tunneling between closely spaced adjacent molecules is expected to have some finite value. Therefore, the system can be envisioned as having two kinetic rates: (i) the vertical conduction rate between the molecule and the substrate, $\boldsymbol{k_1}$, and (ii) the lateral conduction rate between molecules, $\boldsymbol{k_2}$ (Fig. 4(a)). Previous measurements of $\boldsymbol{k_1}$ have revealed very fast time constants indicating that $\boldsymbol{k_1}$ will always be faster than the measurement scan rate.[1] Now, if the measurement scan rate is selected to be faster than $\boldsymbol{k_2}$, then lateral conductivity will have a negligible impact on the measured characteristics, i.e., two distinct peaks will be observed. However, if the scan rate is decreased such that the scan rate is now slower than $\boldsymbol{k_2}$, then lateral conductivity will impact the measurement and majority of the molecules can be oxidized and reduced through the lower voltage ($\mathbf{V_1}$) path. These expected mechanisms are indeed manifested in the experimental observations as shown in Fig. 4(b). At low scan rates, where the measurement rate is slower than $\boldsymbol{k_2}$, the dominance of lateral conductivity results in only one peak at $\mathbf{V_1}$ for the island structure. On the other hand, at higher scan rates, the impact of lateral conductivity is negligible and two distinct peaks are observed. The inset of Fig. 4(b) shows

the behavior of **Fc-BzOH** attached to the *N*+ /*P* diode at various scan rates. Unlike the island structure, the *N*+ /*P* diodes maintain a peak potential of $\mathbf{V_2}$ independent of scan rate since only one path exists for redox activity. Also, there is a linear dependence of peak current amplitude on the scan rate, reiterating that the molecules are immobilized on the silicon surface and amount of redox species in solution is insignificant.[1] These observations indicate that the tunneling rate between **Fc-BzOH** molecules in a self-assembled monolayer is slower than the vertical tunneling rate between the molecules and the substrate.

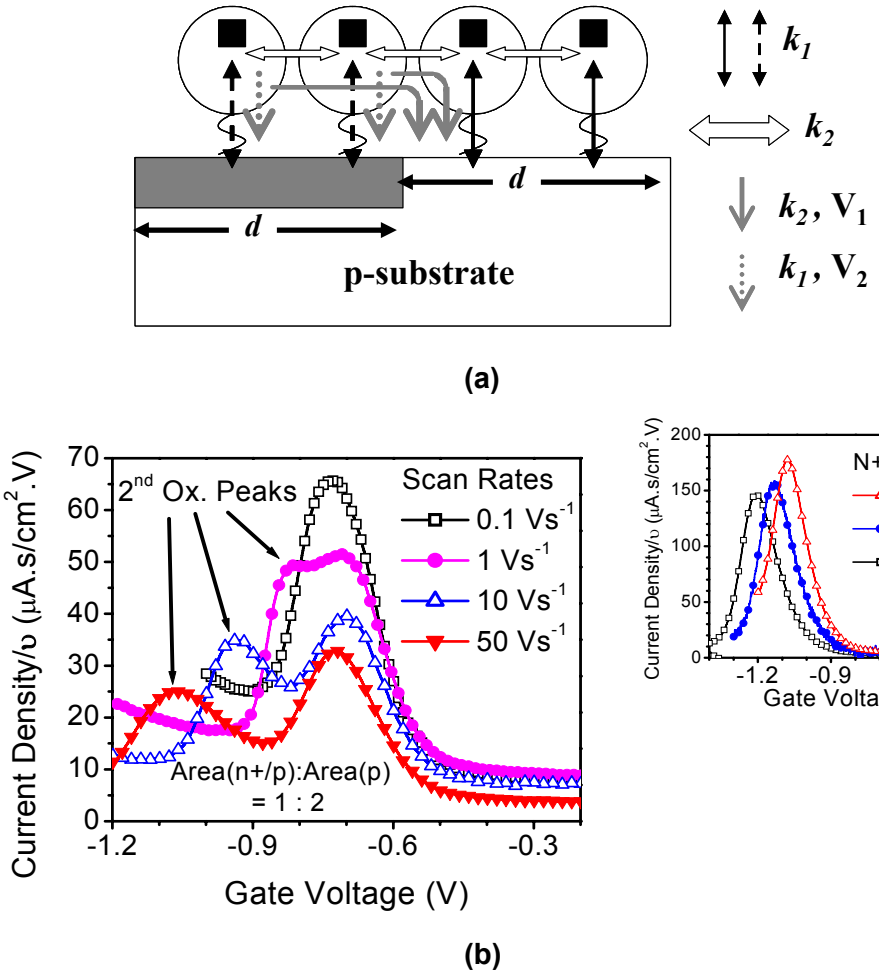


FIG. 4. (a) Schematic showing existence of two different conduction paths (vertical and lateral) for molecules attached on the device structures. The molecules on *N*+ /*P* region have two routes to oxidize, higher potential ($\mathbf{V_2}$) but kinetically faster ($\boldsymbol{k_1}$) vertical path, and lower potential ($\mathbf{V_1}$) but kinetically slower ($\boldsymbol{k_2}$) lateral path. **(b)** Oxidation current from CyV (normalized with respect to scan rate) of **Fc-BzOH** on the device structure at different scan rates showing the emergence of second peak at faster scan rates. There is just one oxidation peak at the lowest scan rate (0.1 V/s). The inset shows oxidation current from CyV of **Fc-BzOH** on just *N*+ /*P*-Si diodes at different scan rates.

It should also be noted that the peak potential of the second peak in the island structure is lower than $\mathbf{V_2}$ at low scan rates but approaches $\mathbf{V_2}$ at high scan rates. This is attributed to the decreasing impact of lateral conduction as scan rate is increased. The rate of lateral conductivity depends on intrinsic $\boldsymbol{k_2}$ rate and the distance between the two regions which determines the tunneling probability. In order to obtain $\boldsymbol{k_2}$, the dimension of the islands ***d*** (Fig. 4(a)) must be decreased to circumvent the effects of tunneling and approach an intrinsic lateral conductivity rate. If ***d*** is <50 nm, $\boldsymbol{k_2}$ can be directly estimated assuming only a few hopping events. An extension of this method would be studying the relationship of ***d*** against the cutoff scan rate. Another method to indirectly quantify $\boldsymbol{k_2}$ is to determine the lateral charge migration coefficient $\boldsymbol{D_E}$ (also referred to as apparent diffusion coefficient with units of cm^2/s), utilizing choronocoulometry technique,[12] as a function of monolayer coverage assuming electron-hopping as the dominant mechanism for lateral charge transfer and estimating $\boldsymbol{k_2}$ from the slope of the $\boldsymbol{D_E}$ vs coverage curve.[13] These methods are currently being pursued to quantitatively estimate $\boldsymbol{k_2}$ and will be discussed in a future publication. There is a possibility that redox species present in the solution could contribute to the measured charge and result in errors in $\boldsymbol{k_2}$ extraction, however, this effect is expected to be small for dense immobilized monolayers as being studied here. Finally, it is expected that $\boldsymbol{k_1}$ and $\boldsymbol{k_2}$ can be tuned with synthetic tailoring of molecules such as modulation of the facial encumbrance and tether properties.[3]

In summary, we have used a silicon device structure to probe the lateral conductivity of a self-assembled monolayer of redox-active molecules of **Fc-BzOH**. We have found that the lateral communication between individual molecules in this monolayer is minimal as compared to the vertical conductivity. The device structure used in this paper can be extended to a variety of redox-active monolayers to detect intermolecular interactions within monolayers. In principle, these devices can also be used to assess the lateral conductivity of non-redox-active conductive monolayers; however, they require higher precision measurements.

This work was supported by Zettacore Inc., and the CNID (DOD/DARPA/DMEA) program. The authors would like to thank Jonathan S. Lindsey at the Department of Chemistry, NCSU for providing them with molecules employed in this work.

References

1. K. M. Roth, A. A. Yasseri, Z. M. Liu, J. S. Lindsey, W. G. Kuhr, and D. F. Bocian, J. Amer. Chem. Soc. **125**, 505 (2003).

2. D. K. James and J. M. Tour, Chem. Mater. **16**, 4423 (2004).

3. A. Balakumar, A. B. Lysenko, C. Carcel, V. L. Malinovskii, D. T. Gryko, K. H. Schweikart, S. Loewe, A. Yasseri, Z. M. Liu, D. F. Bocian, and J. S. Lindsey, J. Org. Chem. **69**, 1435 (2004).

4. A. Inoue, W. Mizutani, T. Ishida, and H. Tokumoto, Appl.Phys. a-Mater. **66**, S1241 (1998).

5. T. Ishida, W. Mizutani, U. Akiba, K. Umemura, A. Inoue, N. Choi, M. Fujihira, and H. Tokumoto, J. Phys. Chem. B, **103**, 1686 (1999).

6. C. J. Miller and M. Majda, J. Electroanal. Chem. **207**, 49 (1986).

7. C. A. Goss, C. J. Miller, and M. Majda, J. Phys. Chem. **92**, 1937 (1988).

8. P. Bonhote, E. Gogniat, S. Tingry, C. Barbe, N. Vlachopoulos, F. Lenzmann, P. Comte, and M. Gratzel, J. Phys. Chem. B, **102**, 1498 (1998).

9. S. Gowda, G. Mathur, Q. Li, S. Surthi, Q. Zhao; J.S. Lindsey, K. Mobley, D.F. Bocian and V. Misra, Tech. Dig. – Int. Electron Devices Meet. **2003**, 22.1.1 (2003).

10. Q. Li, G. Mathur, M. Homsi, S. Surthi, V. Misra, V. Malinovskii, K. H. Schweikart, L. H. Yu, J. S. Lindsey, Z. M. Liu, R. B. Dabke, A. Yasseri, D. F. Bocian, and W. G. Kuhr, Appl. Phys. Lett. **81**, 1494 (2002).

11. A. J. Bard and L. R. Faulkner, in *Electrochemical Methods-Fundamentals and Applications.* (Wiley, New York, 2002), pp. 590..

12. A. J. Bard and L. R. Faulkner, in *Electrochemical Methods-Fundamentals and Applications.* (Wiley, New York, 2002), pp. 603, 613.

13. D. N. Blauch and J. M. Saveant, J. Amer. Chem. Soc. **114** (9), 3323 (1992).

- end of publication -

4.7 Summary

The properties of the molecules can be tailored by molecular design and synthetic chemistry. In this work, it was demonstrated that an alternate route to tune/enhance the properties of hybrid device was to engineer the substrate (silicon) component.

N+/P Si and P+/N Si diode were fabricated using conventional CMOS processing techniques. The Si diodes were fabricated using the mask set for the FET fabrication discussed in the next chapter. Redox peak potentials shift to higher negative gate voltage in case of molecules on N+/P Si diode by around 450 mV as compared to that for molecules on just P-Si and this was attributed to built-in potential of the diode. The molecules on P+/N Si diode have similar redox behavior as that on N-Si substrate. The redox peak potential in this case shifts to a lower negative gate voltage as compared to molecules on just P-Si. This shift is a function of the ambient light and can be attributed photo-voltage generated across the reverse biased diode depletion region.

Charge retention of the molecules is enhanced on N+/P Si diode as the reduction is a rate-limited process. This is attributed to the reverse recovery time of a forward-biased diode. Increasing the ambient light intensity speeds up the diode reverse recovery process thereby increasing the rate of reduction of molecules. SPICE simulations were carried out to further illustrate the fact that the slow diode reverse recovery pins the voltage across the molecules to an oxidizing value, which slows down the reduction or discharge of molecules.

N+ pockets in p-well Si structures were used to demonstrate the concept of achieving multi-bit by substrate engineering. It was shown that by attaching two-state ferrocene to these structures, it is possible to obtain three-state hybrid silicon-molecular capacitor.

A novel method to detect and estimate the lateral conductivity within immobilized molecular layer was proposed and demonstrated using the N+ pockets in p-well substrate structure. It was qualitatively shown that the lateral conduction rate within self-assembled monolayer of ferrocene was significantly slower as compared to the vertical interaction with the Si substrate. However, in order to accurately quantify the intrinsic molecule-to-molecule

conduction rate within an assembled molecular layer, the critical dimension of the N+ pockets have to be comparable to that of the molecules (~ < 5 nm).

5 HYBRID SILICON-MOLECULAR FET

5.1 Introduction

One of the primary objectives this research work was to fabricate hybrid silicon-molecule FET by incorporating the redox-active molecules on the ultra-thin gate oxide and evaluate the electrical characteristics of the device for multi-state nano-floating gate memory (NFGM) applications. The basic concept and the fabrication of the MoleFET device were introduced in first and second chapters. It may be recalled that the first step of the MoleFET process flow was fabrication of the Si FET using conventional CMOS processing techniques. The details of the Si FET fabrication will be presented in this chapter. As mentioned previously, the results and discussion from preceding chapters serves as the knowledge base in better understanding of MoleFET characteristics detailed in the current chapter.

The aim of assembling redox-active molecules on an ultra-thin gate (tunnel) oxide of Si FET device is to use the quantized redox-charge states in the molecules to modulate the threshold voltage of the device. Hence, the molecules acts as discrete nano-sized charge-storage nodes and the MoleFET device can be considered as a candidate for the nano-floating gate memory proposed by ITRS [1]. The results and discussion on single bit MoleFET device containing monolayer of ferrocene (**Fc-P**) is presented in a published paper that is included in this chapter. Another published paper, included in the Appendix 3, contains electrical characterization data of the MoleFET device and preliminary analysis of the same. The paper included in this chapter has more comprehensive discussion of the MoleFET electrical results and outlines certain issues with the MoleFET that needs to be addressed to improve key memory characteristics of the device. This is followed by discussion on using redox-active porphyrin polymers to improve the non-destructive read window of the MoleFET device and achieve multi-bit device.

5.2 Fabrication of Si FET Device

5.2.1 FET Layout

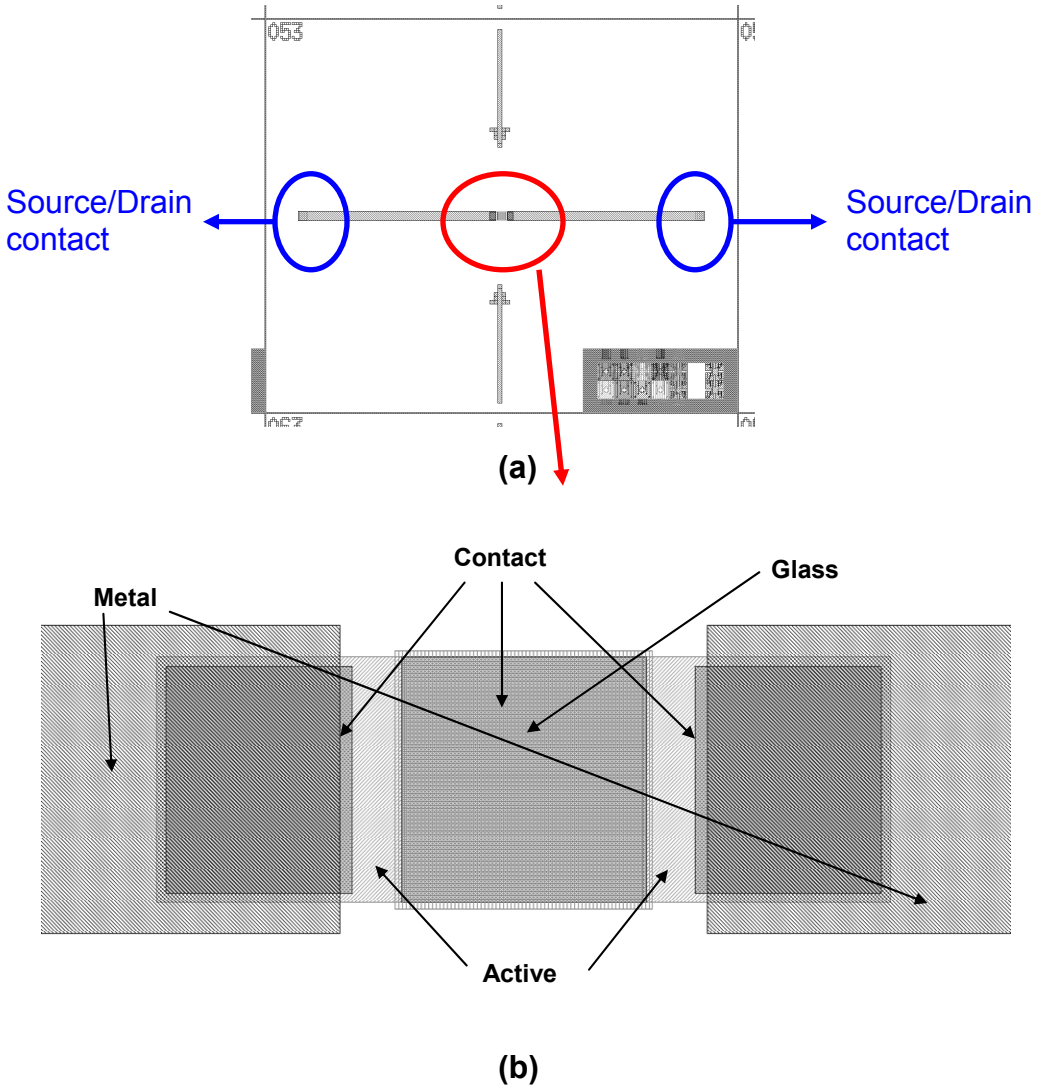


Figure 5.1 (a) Layout of a typical MoleFlash Die. The MoleFET structure lies horizontally across the die, with the FET in the middle of the Die (marked by red circle) and the Source/Drain pads (blue circles) at the edge of the die. **(b)** Layout of a typical FET. The first layer mask is Zero (not shown here) is used for making the lithography alignment marks.

The Si FET fabrication involved 5-level mask set based on replacement gate technology. The MoleFET mask set also included several characterizing devices (test structures) such as capacitors, diodes, sheet resistance test structures, lithography testers and verniers, TLM structures etc. The typical layout of MoleFET device (Fig. 5.1) is provided

in this section. Further details, such as device dimensions, alignment marks, die numbers, etc., of the FET layout and all other structures on the MoleFlash mask set are described in Appendix 1. A typical MoleFlash Die has dimensions of ~ 1 cm x 1cm and MoleFlash Die containing MoleFET structure is shown in Fig. 5.1 (a). The MoleFET structures lies horizontally across the die, with the FET in the middle of the Die (marked by red circle in the Fig. 5.1 (a) and shown in Fig. 5.1 (b)). The Source/Drain contacts are pulled out towards the edge of the die (marked by blue circle in the Fig. 5.1 (a)) in order to accommodate manual electrolyte gate deposition. The vertical arrows on the Die enable the electrolyte gate to be well-centered over the FET device. The arrows also act as a guide for the molecular drop-attachment processing.

The five mask layers in the MoleFlash mask set are: (i) Zero, (ii) Active, (iii) Contact, (iv) Metal, and (v) Glass. The layout of FET showing the last four levels is shown in Fig. 5.1 (b). The Zero level is used for making lithography alignments at the wafer level. Each level after that is primarily aligned to the preceding level. However, there are secondary alignment marks to align to any of the previous levels. The processing steps involved in each of these mask levels will be described in next section.

5.2.2 FET Process Flow

An overview of the processing steps involved in each of the mask levels of MoleFlash mask set is provided here and a detailed description (including details such as temperature, time, film thickness, tools used etc.,) is included in process-log as Appendix 2. Fig. 5.2 depicts the cross-sectional view of the PMOSFET device fabrication and corresponds to the top (flight) view of the FET layout shown in Fig. 5.1 (b).

1. **Zero Layer:** Lithography alignment marks are made at wafer level by etching them into Si. The sequence of steps in this layer involved, starting from blanket Si (100) n-type (phosphorous-doped) polished wafers, is: (i) JTBaker wafer cleaning → (ii) photolithography to pattern the alignment marks (pre-coat hard bake, photoresist spin-coat, pre-exposure soft bake, exposure, develop, and post-develop hard bake) → (iii) descum using plasma asher to improve resist edge profile → (iv) wet etch Zero layer Si using poly etch → (v) resist strip.

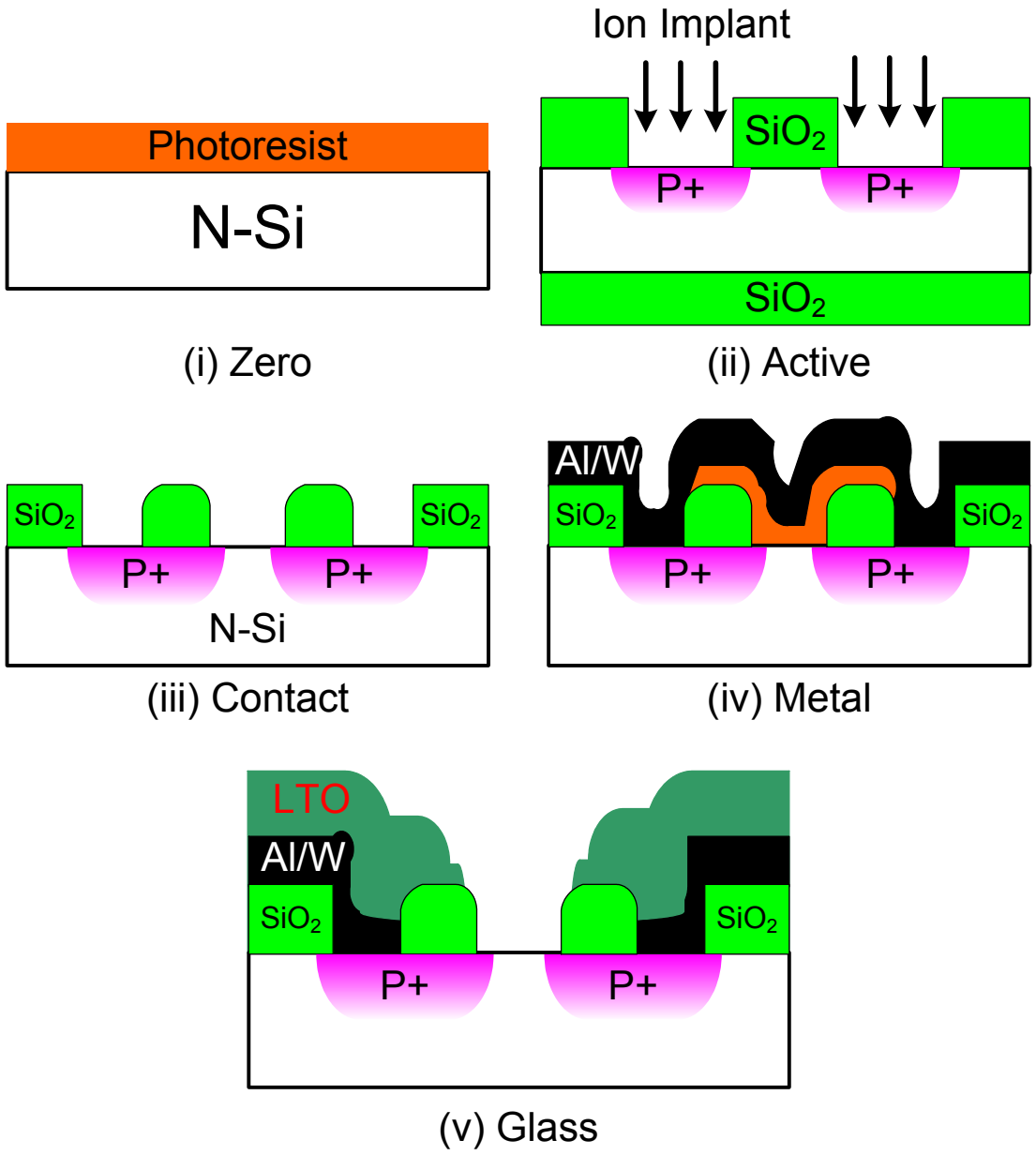


Figure 5.2 FET process flow (MoleFlash mask levels): cross-sectional view of FET active area. The figure corresponding for each level shows the critical step at that level and might not be cross-sectional view at the end of the level. The final cross-sectional view of the FET device is shown in **(v)**.

2. **Active Layer:** The P+ source-drain regions are defined by ion implantation of boron atoms using patterned wet oxide layer as mask. The sequence of steps is: (i) JTBaker clean → (ii) wet oxide (~ 100 nm) growth for ion implant mask → (iii) photolithography to pattern oxide as mask for ion implantation including wafer backside photoresist coat →

(iv) descum → (iv) wet oxide etch using buffered oxide etch (BOE) to open up source-drain regions → (v) strip resist → (vi) JTBaker clean → (vii) ion (boron) implantation → (viii) wet oxide etch to completely remove mask oxide layer (both front and back).

3. **Contact Layer:** Isolation (field) oxide is grown, and holes to gate region and source-drain regions (vias for metal contact) are opened up by patterning the oxide using the contact layer mask. The thermal oxidation step also serves as an implant anneal to activate the source-drain dopants. The sequence of steps is: (i) JTBaker wafer cleaning → (ii) field (wet) oxide growth → (iii) photolithography → (iv) descum → (v) wet oxide etch to open up the holes to gate region and source-drain regions→ (vi) resist strip.

4. **Metal Layer:** Metal contacts to source-drain regions are formed by lift-off processing of the sputtered metal. The metal typically used is tungsten (W). The sequence of steps is: (i) JTBaker wafer cleaning → (ii) photolithography for metal lift-off → (iii) descum → (iv) source-drain remnant oxide etch (BOE) → (v) back-door etch using 1% hydrofluoric acid (HF) → (vi) metal deposition (W sputtering or aluminum/titanium evaporation) → (vii) lift-off processing.

5. **Glass Layer:** Low temperature oxide (LTO) is deposited as passivation layer using low pressure chemical vapor deposition (LPCVD) process, and holes to gate region and end of the metal lines to source-drain regions by patterning the oxide using the contact layer mask. The sequence of steps is: (i) LTO (~ 400 nm) deposition → (ii) photolithography → (iv) descum → (v) wet oxide etch to open up the holes to gate region and metal contact pads → (vi) resist strip.

The details of the Si FETs fabricated using the process flow described above were given in the second chapter along with the rest of the subsequent steps (gate oxide growth and etch-back, molecular attachment, and gate processing) involved in fabrication of the MoleFET device. Some of these steps are mentioned again in the experimental section of the published paper included in the next section.

5.3 Single-bit MoleFET incorporating ferrocene

The discussion on this topic is presented in a publication included in next few pages. It covers the following:

1. MoleFET concept
2. Properties of electrolyte gate
3. Modulation of drain current: high V_T devices
4. Modulation of V_T: low V_T devices
5. Issues with MoleFET device for Flash application

Hybrid Silicon/Molecular FETs: A Study of the Interaction of Redox-Active Molecules With Silicon MOSFETs

Srivardhan Gowda, Student Member, IEEE, Guru Mathur, Student Member, IEEE, Qiliang Li, Member, IEEE, Shyam Surthi, Member, IEEE, and Veena Misra, Senior Member, IEEE

This paper appears in: Nanotechnology, IEEE Transactions on
Publication Date: May 2006
Volume: 5, Issue: 3
On page(s): 258 – 264

Abstract

Redox-active molecular monolayers were incorporated in silicon MOSFETs to obtain hybrid silicon/molecular FETs. Cyclic voltammetry and FET characterization techniques were used to study the properties of these hybrid devices. The redox-active molecules have tunable charge states, which are quantized at room temperature and can be accessed at relatively low voltages. The discrete molecular states were manifested in the drain current and threshold voltage characteristics of the device, confirming the presence of distinct energy levels within the molecules at room temperature. This study demonstrates the modulation of Si-MOSFETs' drain currents via redox-active molecular monolayers. The single-electron functionality provided by the redox-active molecules is ultimately scalable to molecular dimensions, and this approach can be extended to nanoscale field-effect devices including those based on carbon nanotubes. The molecular states coupled with CMOS devices can be utilized for low-voltage, multiple-state memory and logic applications and can extend the impact of silicon-based technologies.

Index Terms — Charge storage molecules, hybrid silicon/molecular devices, molecular electronics, monolayer, MOSFETs, redox-active molecules.

I. INTRODUCTION

The field of molecular electronics has generated considerable interest in the last decade with several research efforts geared toward employing molecules in logic and memory applications. Recently, several molecules with interesting charge-conduction and charge-retention properties have been proposed for use in electronic devices [1]–[5]. The inherent scalability to molecular dimensions without loss of functionality and the ability to tune the intrinsic properties by synthetic chemistry make molecules attractive for potential use in future ultra-dense integrated circuitry. It is expected that the ongoing feature-size reduction in silicon technology would run into physical and economic limitations in a decade or two. Although replacing silicon with molecule-only technology in the near future is considered to be a formidable task, it is widely believed that a hybrid approach involving incorporation of molecules into silicon devices may be instrumental in augmenting today's CMOS-only technologies [6], [7].

The hybrid approach exploits the unique properties of organic molecules, leveraging on the strength of existing silicon technology. We are engaged in developing a class of hybrid silicon/molecular devices utilizing redox-active molecules [8]–[10]. Our approach, explained elsewhere [1], [8], [9], exploits the ability of individual molecules to store charges with single-electron precision at room temperature and is fundamentally different from most of the other approaches which are based on measuring the change in the conductivity of molecules [3], [11]–[13]. The hybrid devices are fabricated by forming self-assembled monolayers of redox-active molecules on silicon or silicon-dioxide surfaces. Physical and chemical properties of monolayers assembled on various surfaces have been investigated in terms of their surface coverages, defect densities, and stability [1], [9], [14]–[19]. A direct correlation was observed between the molecular design, the coverages, defects, and the electrical properties. Furthermore, it was found that the attachment procedures had a large impact on determining the coverage densities and endurance of the monolayers.

The properties of the redox-active molecules can be tailored by molecular design and synthetic chemistry. Multiple-state behavior can be built into the molecular structure with the states being accessible at relatively low voltages. For example, the porphyrin molecule exhibits three discrete states: neutral, monopositive, and dipositive, with the states accessible at negative gate voltages with magnitudes < 1.4 V when attached to silicon [9].

More elaborate molecular structures that afford up to seven positively charged states have also been devised [20]. The charge densities in the redox-active monolayers are typically > 5 x 10^{13} charges/cm^2, which is at least an order of magnitude higher than that achievable in conventional Si capacitors. Furthermore, the total charge is determined by the coverage of the molecules and not by the applied voltage, as is the case for conventional dielectric capacitors [10]. It has been previously demonstrated that devices with a monolayer of porphyrin molecules on silicon can endure more than 10^{12} operational (charging/discharging) lifecycles and are stable under elevated temperatures of 400 ^{o}C for extended periods of time [1].

In this study, these molecules with well-characterized charge storage mechanisms were incorporated in silicon PMOSFETs to modulate the threshold voltage characteristics of the devices by utilizing the quantized energy states within the molecules. The monolayers of two-state ferrocene-based molecules were formed on ultrathin gate oxides via self-assembly to obtain hybrid silicon/molecular FETs. Conventional cyclic voltammetry (CyV) was used to verify the presence of redox-activity in these devices. CyV is an electrochemical technique used to study electron-transfer mechanisms in a redox system. In this measurement, potential is varied linearly with time in forward and reverse directions, and the resulting displacement current is recorded as a function of potential, which is equivalent to recording current versus time [21]. In our case, the forward sweep is in the negative gate potential direction and corresponds to oxidation or removal of electrons from the molecule to the silicon substrate while the reverse sweep corresponds to a reduction of the molecule [8]. The measured current is a function of the potential sweep rate and has two components: 1) background charging current and 2) Faradaic current. The former component is dependent on the background capacitance, which is constant with respect to applied voltage, while the latter component is due to redox of the molecules. The modulation of device characteristics was studied using a semiconductor parameter analyzer. An application of oxidizing gate potential causes each molecule to lose an electron to the silicon substrate through the gate oxide, leaving the monolayer positively charged. This results in a shift in the threshold voltage of the device to a more negative value, thereby lowering the drain current. The magnitude of the threshold shift $|\Delta V_T|$ due to redox charge, Q_{redox} is given as

$$\left|\Delta V_T\right| = \frac{Q_{redox}}{C_{gm}} \quad (1)$$

where C_{gm} is the gate-to-molecule capacitance.

When a reducing gate potential is applied, electrons from the silicon tunnel back into the molecules through the oxide barrier returning the monolayer to its neutral state, which decreases the threshold voltage back to the original value. The oxidation and reduction processes are manifested as current peaks in cyclic voltammetry and correspond to the write and erase processes of the device, respectively. The oxidation and reduction peak potentials effectively determine the write and erase voltages of the device. It is essential to have significant separation between the peak potentials as the separation defines the window for nondestructive read operation when these devices are used in memory applications. The separation in peak potentials is a strong function of the oxide barrier thickness, and the read window is found to improve with increasing thickness of the gate oxide [22]. Intrinsically, the electron transport to and from the molecule is extremely fast (of the order of tens of nanoseconds), and the charge retention is of the order of hundreds of minutes [9]. The oxide layer acts as a tunneling barrier for the electrons and improves the charge-retention characteristics of the device [23]. Hybrid silicon/molecular capacitor structures were fabricated as controls to optimize the redox (write/erase) potentials and charge-retention characteristics.

The hybrid FET devices with quantized states at room temperature, along with low-voltage operation, potential for multistate, and excellent charge-retention characteristics, may be attractive for use in charge storage memory devices such as 1T-DRAM and FLASH. More importantly, these molecules behave like discrete charge storage entities and, hence, intermolecular interactions within the monolayer are insignificant as compared to molecule-to-substrate interactions [6]. Effectively, this approach enables the assembly of nanoscale charge storage islands with a high degree of uniformity and repeatability, with the ability to remove charges from the island with single-electron precision at room temperature. The properties of hybrid silicon/molecular FETs were studied with the intent of understanding the interactions of redox-active molecules with silicon MOSFETs and investigating towards application in memory and logic functions.

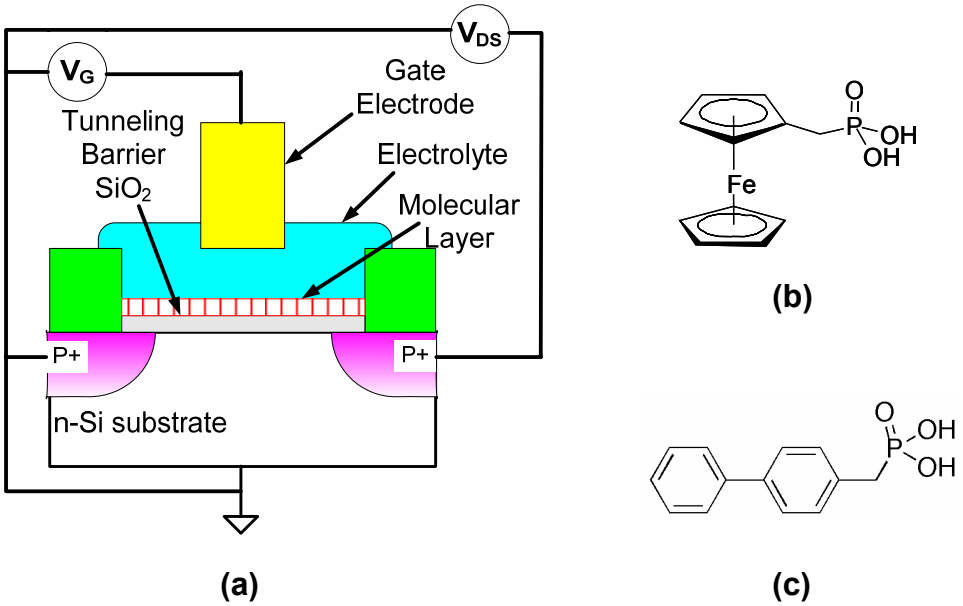


Fig. 1. (a) Schematic of a hybrid Si/molecular PMOSFET with a SAM of **Fc-P** attached on the gate oxide. Electrolyte is contacted by an Ag electrode. **(b)** Chemical structure of the **Fc-P** molecule. This molecule exhibits two cationic states: neutral and monopositive. **(c)** Chemical structure of the **Bz-P** molecule. This molecule is NOT redox-active and was used in control experiments.

II. EXPERIMENTAL SETUP

A schematic of the hybrid silicon/molecular PMOSFET is shown in Fig. 1(a). The redox-active molecule used in this study was ferrocenyl phosphonate [**Fc-P**, see Fig. 1(b)]. The ferrocene unit exhibits two stable states: neutral and monopositive (i.e., it becomes positively charged after oxidation when a negative gate voltage with magnitude higher than the write voltage is applied). For control experiments, the non-redox molecule biphenyl phosphonate (**Bz-P**) was used [see Fig. 1(c)]. The experiments in this study were confined to PMOSFETs since **Fc-P** becomes cationic under negative gate voltages, which are of interest in PMOSFETs. The MOSFETs used in the experiments were fabricated using a five-level mask process based on replacement gate technology. PMOSFETs of gate lengths varying from 10 to 100 μm with varying dimensions of source–drain overlap regions (2.5 to 5 μm) were fabricated. The gate width was equal to the gate length for all devices. Gate oxide of varying thicknesses (1–3 nm) was grown by thermal oxidation. Capacitor test structures with identical oxide thicknesses were also fabricated for control experiments. The molecular solution used to form self-assembled monolayers (SAMs) on silicon dioxide was

prepared by dissolving 1 mg of these compounds in 200 μl of dimethyl formamide. The samples were heated to 90 ^{o}C during the attachment in an argon-purged environment. After attachment, the samples were cleaned by sonication (three times) in dichloromethane. For electrical characterization, a solution of 1-M tetrabutylammonium hexafluorophosphate in propylene carbonate was used as the gate electrolyte, and silver wire was used as the counter/reference electrode. Electrical analyses were performed using a CHI 600 electrochemical analyzer for CyV measurements and an HP 4155B semiconductor parameter analyzer for FET device characterization.

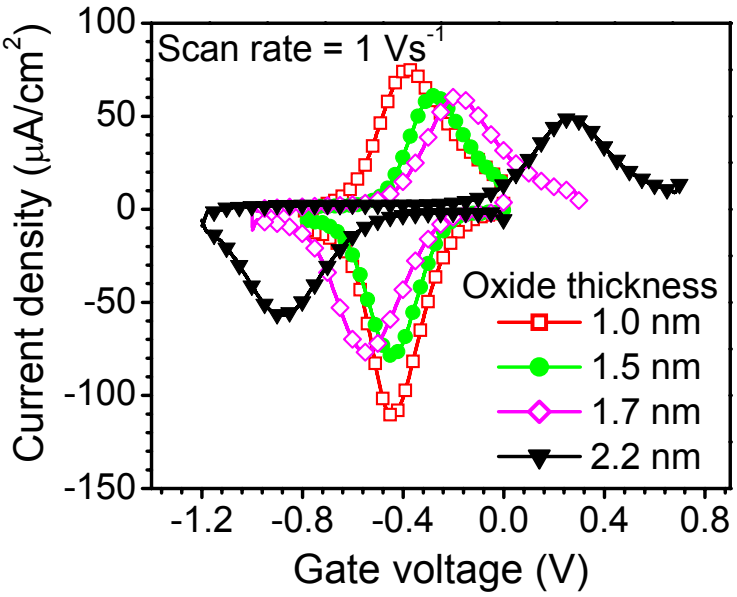


Fig. 2. CyV of electrolyte-molecule-oxide-silicon capacitors with **Fc-P** attached to oxide on p-Si, with t_{ox} varying from 1.0 to 2.2 nm. The scan rate is 1 V/s. Peaks in the lower half (negative currents) correspond to oxidation, and peaks in the upper half (positive currents) correspond to reduction of the molecules. The peak separation increases with increasing oxide thickness.

III. RESULTS AND DISCUSSION

Fig. 2 shows the forward and reverse scans of CyV of redox-active molecules (**Fc-P**) attached to varying oxide thicknesses (1.0–2.2 nm) on p-silicon substrate. The negative and positive current peaks observed are associated with the oxidation and reduction of the molecules, respectively.

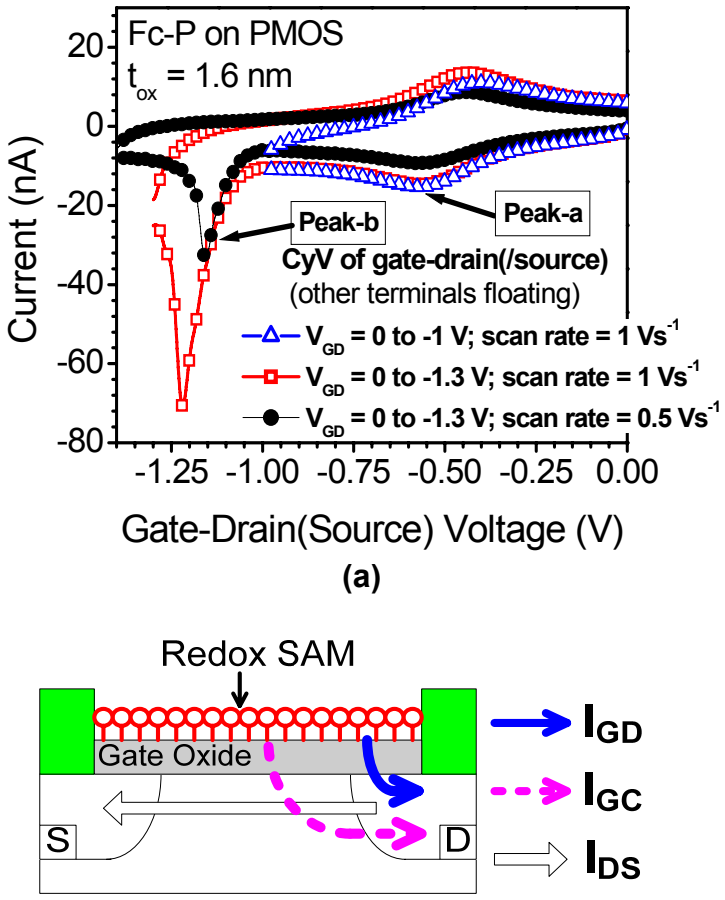


Fig. 3. (a) CyV of gate–drain (or source) of a hybrid PMOS with **Fc-P** on the gate oxide. The other terminals are floating. The two oxidation peaks correspond to molecules on the overlap (peak-a, *P*+) and the channel (peak-b, *N/P*+) regions, with the latter occurring at a more negative potential. The reduction peak of molecules on the channel is subdued [6]. **(b)** Schematic showing different routes for molecules in a hybrid FET to become oxidized. I_{GD} and I_{GC} represent redox paths for molecules on the channel and overlap regions, respectively. I_{DS} represents the drain current.

Typical charge densities obtained from the area under the CyV peaks are ~10^{14} charges/cm^2. The oxidation peak potential, which corresponds to the write voltage of the device, shifts to higher negative values with increasing oxide barrier thickness, whereas the reduction peak potential (erase voltage) shifts to higher positive values. Effectively, increased separation between oxidation and reduction peak potentials leads to a region of no redox, as seen in the CyV of the device with 2.2-nm oxide (see Fig. 2), which provides an adequate read window in the FET configuration. This increasing peak separation is attributed to the lowering of the electron tunneling rate with increased oxide barrier

thickness, which necessitates higher gate voltages for redox of the molecules [22]. Increasing the measurement scan rate for a given oxide thickness also has similar effects as increasing the oxide thickness and results in increasing the separation of redox peak potentials. This is due to the decreased time available for tunneling of electrons. Similar behavior was observed for n-silicon substrate capacitor test structures as well. Increasing the oxide barrier also results in longer retention times, though at the cost of slightly higher write/erase voltages.

Fig. 3(a) shows the gate-to-drain CyV currents for a PMOSFET with an Fc-P SAM on a 1.6-nm gate oxide. The molecules in the monolayer potentially have two independent routes to get oxidized and reduced. The existence of dual redox paths for N pockets embedded in a P-well has been previously reported [6] and is attributed to negligible intermolecular interactions (lateral conduction) within the monolayer. The molecules on the channel take the N/P+ (diode) path, and molecules on the overlap regions take the P+ path, as illustrated by $\boldsymbol{I_{GC}}$ and $\boldsymbol{I_{GD}}$, respectively, in Fig. 3(b). The oxidation peak potential for the $\boldsymbol{I_{GC}}$ path is expected to be higher (or equal to) in magnitude than that for the $\boldsymbol{I_{GD}}$ path due to the requirement of channel inversion for molecules on the channel to get oxidized [6]. The two peak potentials are equal when the threshold voltage (V_{T0}) of the FET is lower (or equal) in magnitude than the characteristic oxidizing potential (V_{oxd}) for **Fc-P** attached to oxide on P-silicon (approximately 0.5 V for 1.6-nm-thick oxide at a scan rate of 1 V/s). The two observed peaks in Fig. 3(a) correspond to oxidation occurring in the overlap region ($\boldsymbol{I_{GD}}$) between the gate and drain (lower $|V_{GD}|$, peak-a) and that occurring in the channel via $\boldsymbol{I_{GC}}$ once inversion is reached (higher $|V_{GD}|$, peak-b). The channel and overlap oxidation peaks can also be observed in the gate–substrate (source–drain tied to substrate) CyV with the former occurring at a higher negative gate voltage. Thus, the requirement for oxidation of molecules on: 1) channel is $|V_G| > \max(|V_{T0}|, |V_{oxd}|)$ and 2) overlap regions is $|V_{GD}|$ (or $|V_{GS}|$) $> |V_{oxd}|$, where max( ) implies the higher of the two values within the parenthesis.

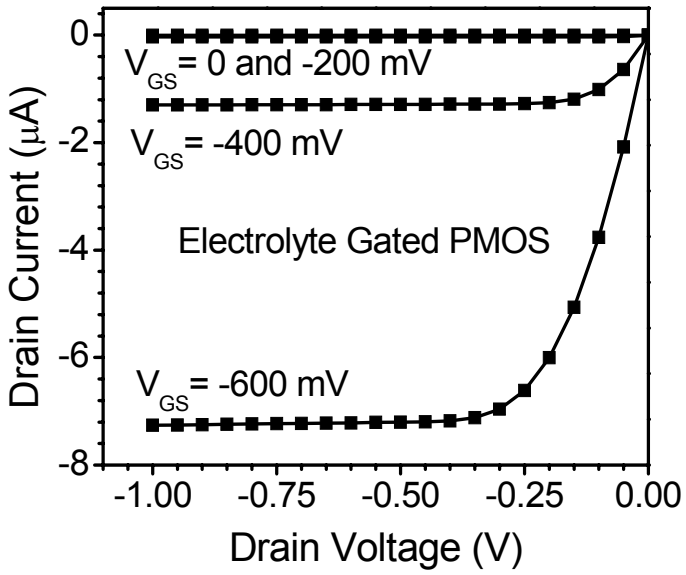


Fig. 4. Transistor characteristics (I_D–V_D) of an electrolyte-gated PMOS (no molecules) with native oxide on the gate. The electrical double layer formed at the electrolyte–electrode interfaces provides an excellent tunnel barrier and causes inversion in the channel.

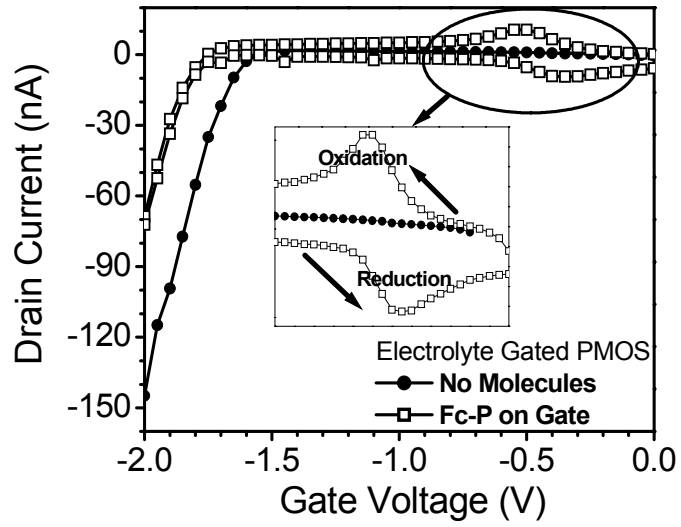


Fig. 5. Transfer characteristics (I_D –V_G) of a hybrid PMOSFET with 2.8-nm gate oxide. The peaks in the subthreshold region are associated with redox of molecules in the overlap regions. The oxidation and reduction currents are swapped because the gate current is in the opposite direction of the drain current. MOSFET without any molecules did not show any such peaks.

Investigating the function of electrolyte as the gate, it was observed that electrolyte-gated FET with only native oxide has excellent transistor characteristics, as presented in

Fig. 4. This is attributed to the presence of an ultra thin double layer (~ 1 nm) that forms at the electrolyte–oxide interface and acts as an excellent dc tunnel barrier. The formation of the electrical double layer at the electrolyte–solid interface is explained by Helmholtz theory [24]. The double-layer capacitance $\boldsymbol{C_{dl}}$, which appears in series with the native oxide capacitance, is sufficiently large to maintain a high I_D/I_G ratio and easily turn the transistor on. The redox-active molecules were incorporated onto this platform, and the transistor device characteristics were studied. It should be noted that $\boldsymbol{C_{dl}}$ is the gate-to-molecule capacitance ($\boldsymbol{C_{gm}}$) which figures in (1). Hence, it is essential for to be low-valued in order to maximize the threshold voltage shift for a given value of molecular redox charge.

Fig. 5 shows the I_D–V_G behavior of a PMOSFET with **Fc-P** molecules attached to a 2.8-nm gate oxide. As V_G is increased, oxidation of the molecules occurs in the forward scan, and the reduction occurs during the reverse scan. The direction of the oxidation and reduction currents is swapped because the gate current is in the opposite direction to the drain current. The redox peaks are observed in the subthreshold region and are attributed to molecules on the gate–drain overlap region since the channel is not yet inverted. As seen in Fig. 5, there were no peaks observed in control PMOSFET samples without molecules. Fig. 6(a) shows the I_D–V_D behavior of the hybrid FET device in the subthreshold region. In this measurement, at the start (V_D = 0), for gate voltages $|V_{GD}| > |V_{oxd}|$ ~ 0.5 V, molecules on the gate–drain overlap region are oxidized. As V_{DS} is increased, these molecules remain oxidized until $|V_{GD}| < |V_{red}|$ ~ 0.3 V, beyond which they get reduced. V_{red} is the characteristic reduction potential for **Fc-P** attached to oxide on p-silicon substrate. Distinct peaks in the drain currents are observed owing to reduction of molecules in the overlap region ($\boldsymbol{I_{GD}}$). Since this is a transient effect and the molecules in the overlap region do not affect the channel potential, the drain current recovers to its original value once all of the molecules in the overlap region are reduced, as seen in Fig. 6(a). However, when $|V_G| > |V_{T0}|$ (~ 1.8 V, in this case), the molecules on the channel also get oxidized along with the overlap molecules, at the start of the measurement (V_{DS} = 0). This creates a layer of positive charges over the channel, thereby shifting the threshold voltage to a higher negative value, the magnitude of which is given by (1). Now, as V_{DS} is increased, positively charged channel molecules near the drain are also reduced along with the overlap molecules when $|V_{GD}| < |V_{red}|$. The threshold voltage is, hence, decreased to a lower value, thus causing an increase in the drain current. This effect is observed in Fig. 6(b), where the drain currents do not recover to

the pre-reduction values after reduction peaks. Fig. 6(c) shows the plot of the change in the drain current (ΔI_D) versus gate voltage (V_G). As expected, ΔI_D has a linear relationship with V_G when the transistor is in the linear region of operation, owing to a constant decrease in V_T associated with the reduction of molecules on the channel near the drain end. This further indicates that the redox charge density in the molecular monolayer is a constant, irrespective of the applied gate voltage.

To further study the modulation of threshold voltage and hysteresis, I_D–V_G characteristics were measured on a PMOSFET with < 1 nm gate oxide. As shown in Fig. 7, hysteresis was observed in the MOSFET containing redox-active molecules, whereas no such hysteresis was observed in case of control MOSFETs either: 1) without molecules or 2) with non-redox molecules (Bz-P). In the forward scan, with increasing gate voltage, the redox-active molecules get oxidized and become positively charged, resulting in an increase of the threshold voltage. This is seen as a progressive lowering of the drain current in the forward scan as compared to that of the control MOSFETs. During the return scan, many of these molecules still remain in the oxidized state, thus causing a lower drain current. However, significant reduction of the oxidized molecules occurs during the return scan, given that the separation between the oxidation and reduction peaks (or the read window) is not large for oxides nm at a measurement scan rate of 1 V/s. This results in a lower value of hysteresis than expected from the number of molecules/charges present.

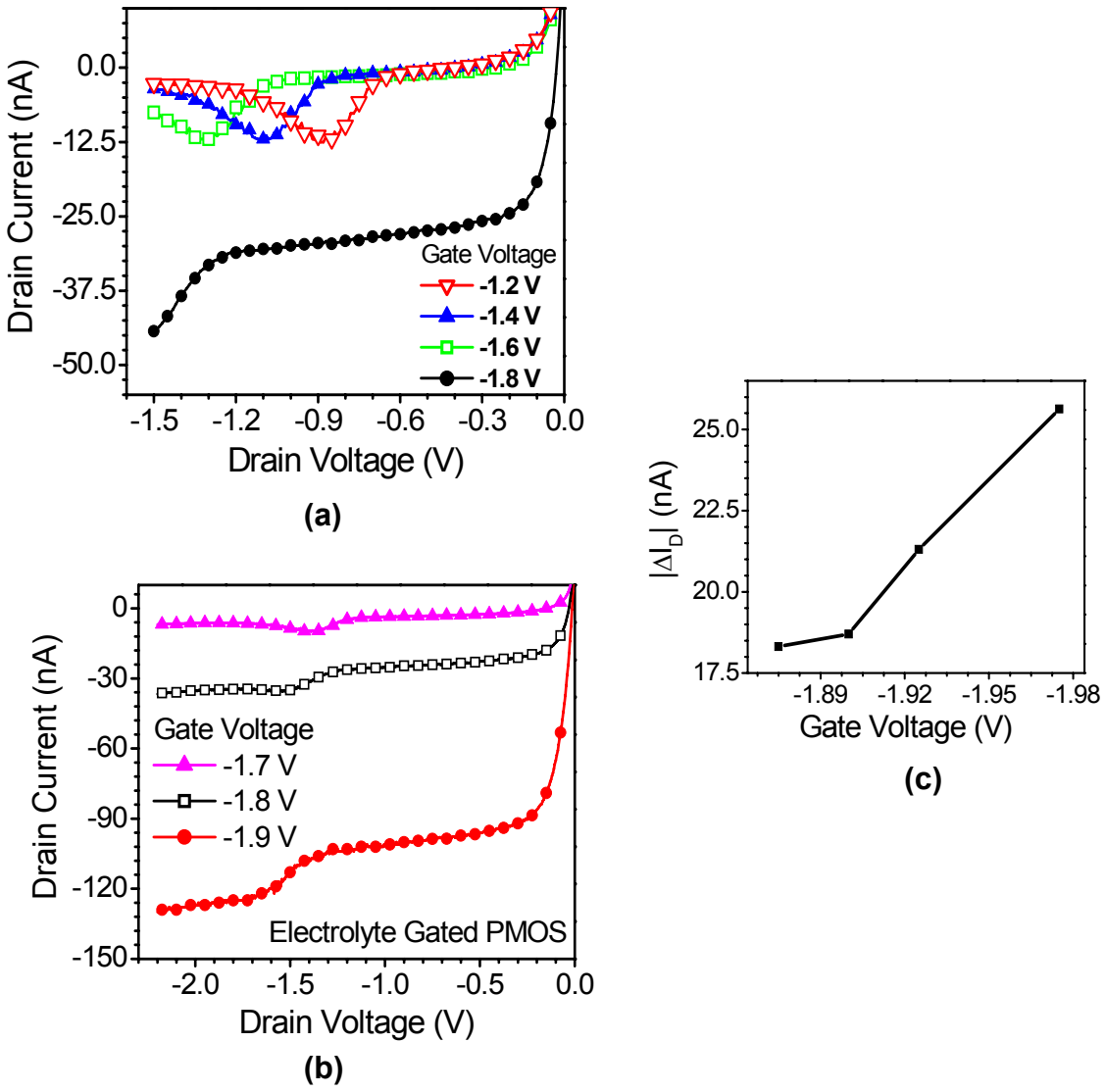


Fig. 6. Transistor characteristics in subthreshold region of hybrid PMOS with 2.8-nm gate oxide. The peaks are associated with the reduction of molecules in the overlap region. There is no increase in the drain current after the reduction of the oxidized molecules on the overlap region. **(b)** Transistor characteristics of hybrid PMOSFET with 2.8-nm gate oxide, with the transistor turned on. There is an increase in the drain current after the reduction of the oxidized molecules on the channel close to the drain terminal. **(c)** Change in drain current (ΔI_D) versus gate voltage for the hybrid PMOSFET with 2.8-nm gate oxide, showing a linear dependence when the device is turned on, indicating a constant decrease in threshold voltage due to reduction of oxidized molecules on the channel near the drain terminal.

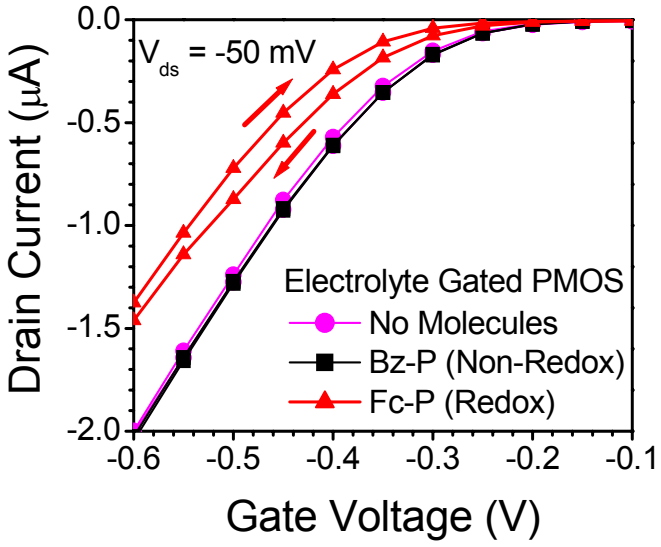


Fig. 7. Transfer characteristics of hybrid PMOSFETs with redox molecules (**Fc-P**), non-redox molecules (**Bz-P**), and no molecules on the gate oxide. The gate-oxide thickness is 1.2 nm. The arrows indicate the direction of the voltage sweeps for the hybrid device with redox molecules. There exists no hysteresis between the forward and reverse scans for the control FETs with either: 1) non redox molecules or 2) no molecules.

As discussed previously, one of the ways to improve the read window is to increase the measurement scan rate [see Fig. 8(a)]. Hence, the value of hysteresis increases with increasing measurement scan rate [see Fig. 8(b)]. In order to further confirm that the amount of hysteresis depends on the extent of oxidation of the molecules, the scan range V_G of was varied (see Fig. 9). As shown, there is an increase in the value of hysteresis as the scan range is increased, and this value saturates when the range is large enough to completely oxidize all of the molecules. The range of redox activity is indicated by the gate–substrate CyV plotted as the secondary *y*-axis [see Fig. 9(c)]. The value of hysteresis can also be increased by employing a thicker gate oxide. It was found that increasing the thickness from < 1.0 to 1.3 nm creates a larger window between oxidation and reduction and consequently improves the hysteresis even at lower scan rates. It is essential to use a better write–erase strategy involving pulse techniques to accurately quantify the threshold voltage shift due to redox charges. Also, the molecule-to-gate screening distance as defined by the electrolyte double-layer thickness (~ 1 nm) makes $\boldsymbol{C_{gm}}$ significantly large 25 μF/cm^2 [25]. As mentioned previously, this would result in a small threshold-voltage shift (ΔV_T). Since it is desirable to keep the electrolyte double-layer thickness small to obtain low write voltages, it becomes

necessary to increase Q_{redox} to obtain large ΔV_T, as shown in (1). Even higher charge densities can be obtained by using multiple layers of redox-active molecules which can afford charge densities as high as ~ 10^{15} charges/cm^2 [26]. The high charge densities along with discrete multiple states accessible at room temperature make this approach highly attractive for future memory devices.

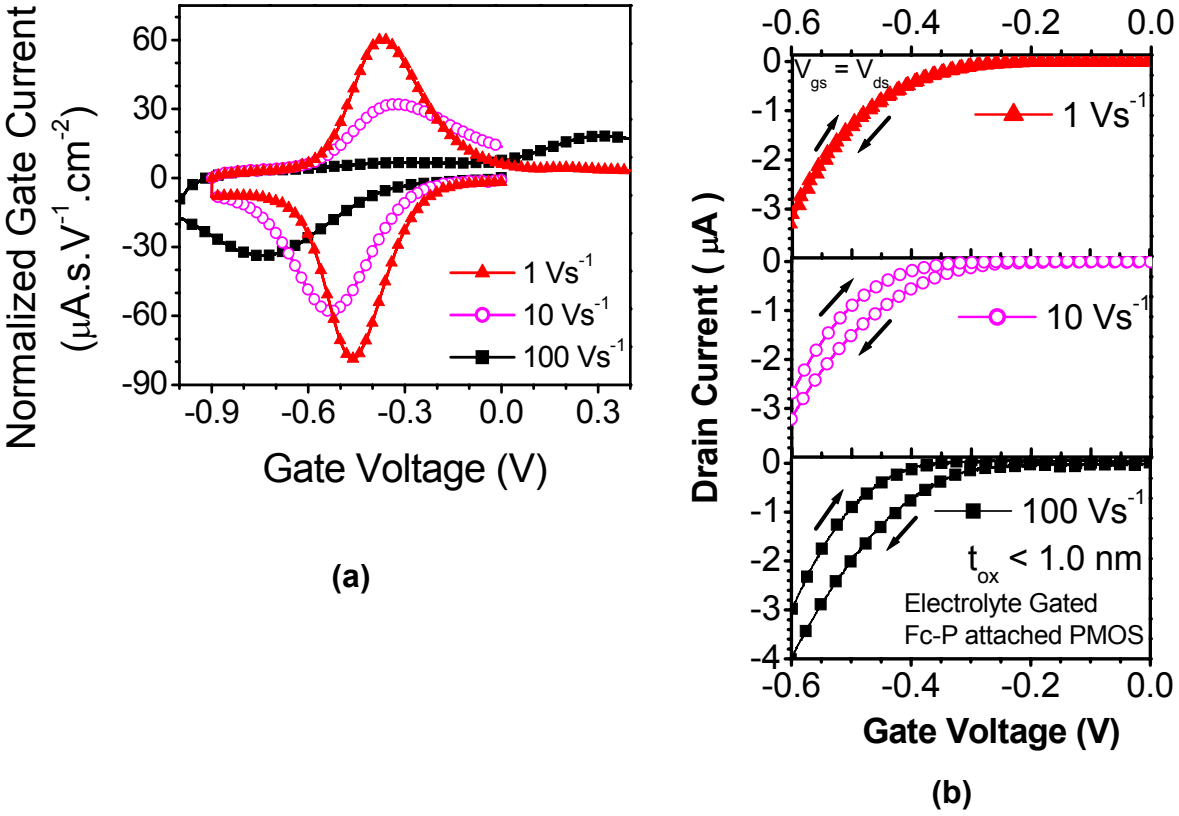


Fig. 8. (a) Gate–substrate CyV of hybrid PMOS, with < 1 nm gate oxide, at the varying scan rates with source and drain tied to ground. **(b)** Transfer characteristics of the hybrid PMOS, at corresponding gate-voltage scan rates, showing the effect of scan rate on the redox-related hysteresis.

IV. CONCLUSION

Hybrid silicon/molecular FETs were fabricated by incorporating redox-active molecules in PMOSFETs. The presence of discrete charge states of the molecules was manifested in the threshold voltage, drain current, and hysteresis characteristics at room temperature. Hysteresis characteristics were dependent on the barrier oxide thickness, the number of molecules involved in redox activity, and the measurement scan rate. This paper

provides the proof of concept for electronic devices using redox-active molecules in MOS transistors. Information can be stored in the discrete states of molecules with multiple states, which can provide quantized threshold voltage shifts. Molecular states can be utilized for low-voltage, low-power, multiple-state memory, and logic applications.

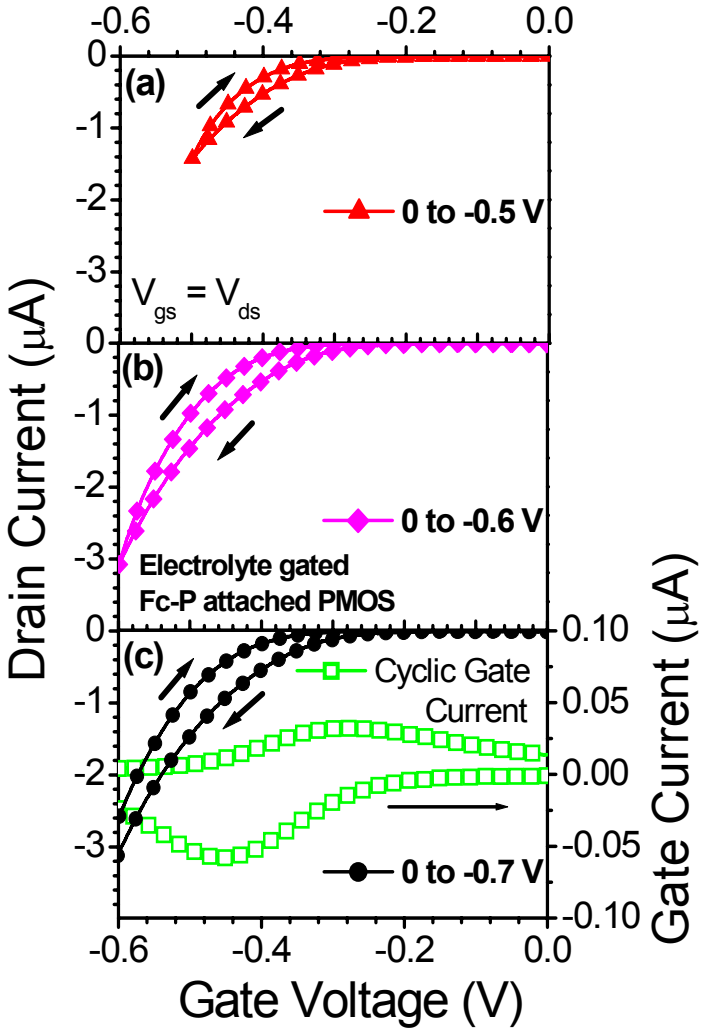


Fig. 9. Transfer characteristics of hybrid PMOS with < 1 nm gate oxide showing the dependence of hysteresis on gate voltage scan range: (a) 0 to - 0.5 V, (b) 0 to - 0.6 V, and (c) 0 to - 0.7 V. Gate-to-substrate CyV of this device, plotted on the secondary y-axis of (c), shows that the amount of hysteresis is directly correlated to the redox charge.

ACKNOWLEDGMENT

The authors would like to thank J. S. Lindsey, Department of Chemistry, North Carolina State University, for providing us with molecules employed in this study and D. F. Bocian, Department of Chemistry, University of California at Riverside, for discussions.

REFERENCES

[1] Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science*, vol. 302, pp. 1543–1545, 2003.

[2] A. R. Pease, J. O. Jeppesen, J. F. Stoddart, Y. Luo, C. P. Collier, and J. R. Heath, "Switching devices based on interlocked molecules," *Accounts Chem. Res.*, vol. 34, pp. 433–444, 2001.

[3] C. P. Collier, E. W. Wong, M. Belohradsky, F. M. Raymo, J. F. Stoddart, P. J. Kuekes, R. S. Williams, and J. R. Heath, "Electronically configurable molecular-based logic gates," *Science*, vol. 285, pp. 391–394, 1999.

[4] J. M. Tour,W. L.Van Zandt, C. P. Husband, S. M. Husband, L. S.Wilson, P. D. Franzon, and D. P. Nackashi, "Nanocell logic gates for molecular computing," *IEEE Trans. Nanotechnol.*, vol. 1, no. 2, pp. 100–109, Jun.,2002.

[5] J. R. Heath and M. A. Ratner, "Molecular electronics," *Phys. Today*, vol. 56, pp. 43–49, 2003.

[6] S. Gowda, G. Mathur, Q. Li, S. Surthi, Q. Zhao, J. Lindsey, K. Mobley, D. Bocian, and V. Misra, "Hybrid silicon/molecular memories: Co-engineering for novel functionality," in IEDM'03 Tech. Dig., 2003, pp. 22.1.1–22.1.4.

[7] R. Wolkow, "Toward hybrid devices," Chem. Eng. News, vol. 79, pp. 228–228, 2001.

[8] Q. L. Li, G. Mathur, M. Homsi, S. Surthi, V. Misra, V. Malinovskii,K. H. Schweikart, L. H. Yu, J. S. Lindsey, Z. M. Liu, R. B. Dabke, A. Yasseri, D. F. Bocian, and W. G. Kuhr, "Capacitance and conductance characterization of ferrocene-containing self-assembled monolayers on silicon surfaces for memory applications," Appl. Phys. Lett., vol. 81, pp. 1494–1496, 2002.

[9] K. M. Roth, A. A. Yasseri, Z. M. Liu, R. B. Dabke, V. Malinovskii, K. H. Schweikart, L. H. Yu, H. Tiznado, F. Zaera, J. S. Lindsey, W. G. Kuhr, and D. F. Bocian, "Measurements of electron-transfer rates of charge-storage molecular monolayers on Si(100). Toward hybrid molecular/semiconductor information storage devices," J. Amer. Chem. Soc., vol. 125, pp. 505–517, 2003.

[10] K. M. Roth, J. S. Lindsey, D. F. Bocian, and W. G. Kuhr, “Characterization of charge storage in redox-active self-assembled monolayers,” Langmuir, vol. 18, pp. 4030–4040, 2002.

[11] J. Chen, W. Wang, M. A. Reed, A. M. Rawlett, D. W. Price, and J. M. Tour, “Room-temperature negative differential resistance in nanoscale molecular junctions,” Appl. Phys. Lett., vol. 77, pp. 1224–1226, 2000.

[12] C. N. Lau, D. R. Stewart, R. S. Williams, and M. Bockrath, “Direct observation of nanoscale switching centers in metal/molecule/metal structures,” Nano Lett., vol. 4, pp. 569–572, 2004.

[13] H. R. Tseng, D. M.Wu, N.X. L. Fang, X. Zhang, and J. F. Stoddart, “The metastability of an electrochemically controlled nanoscale machine on gold surfaces,” Chemphyschem., vol. 5, pp. 111–116, 2004.

[14] L. Y.Wei, K. Padmaja,W. J. Youngblood, A. B. Lysenko, J. S. Lindsey, and D. F. Bocian, “Diverse redox-active molecules bearing identical thiol-terminated tripodal tethers for studies of molecular information storage,” J. Organic Chem., vol. 69, pp. 1461–1469, 2004.

[15] A. Balakumar, A. B. Lysenko, C. Carcel, V. L. Malinovskii, D. T. Gryko, K. H. Schweikart, R. S. Loewe, A. A. Yasseri, Z. M. Liu, D. F. Bocian, and J. S. Lindsey, “Diverse redox-active molecules bearing O-, S-, or Se-terminated tethers for attachment to silicon in studies of molecular information storage,” J. Organic Chem., vol. 69, pp. 1435–1443, 2004.

[16] K. M. Roth, D. T. Gryko, C. Clausen, J. Z. Li, J. S. Lindsey,W. G. Kuhr, and D. F. Bocian, “Comparison of electron-transfer and charge-retention characteristics of porphyrin-containing self-assembled monolayers designed for molecular information storage,” J. Phys. Chem. B, vol. 106, pp. 8639–8648, 2002.

[17] G. A. Schick, I. C. Schreiman, R. W. Wagner, J. S. Lindsey, and D. F. Bocian, “Spectroscopic characterization of porphyrin monolayer assemblies,” J. Amer. Chem. Soc., vol. 111, pp. 1344–1350, 1989.

[18] K. Muthukumaran, R. S. Loewe, A. Ambroise, S. I. Tamaru, Q. L. Li, G. Mathur, D. F. Bocian, V. Misra, and J. S. Lindsey, “Porphyrins bearing arylphosphonic acid tethers for attachment to oxide surfaces,” J. Organic Chem., vol. 69, pp. 1444–1452, 2004.

[19] R. S. Loewe, A. Ambroise, K. Muthukumaran, K. Padmaja, A. B. Lysenko, G. Mathur, Q. L. Li, D. F. Bocian, V. Misra, and J. S. Lindsey, “Porphyrins bearing mono or tripodal benzylphosphonic acid tethers for attachment to oxide surfaces,” J. Organic Chem., vol. 69, pp. 1453–1460, 2004.

[20] D. Gryko, J. Z. Li, J. R. Diers, K. M. Roth, D. F. Bocian,W. G. Kuhr, and J. S. Lindsey, “Studies related to the design and synthesis of a molecular octal counter,” J. Mater. Chem., vol. 11, pp. 1162–1180, 2001.

[21] A. J. Bard and L. R. Faulkner, Electrochemical Methods-Fundamentals and Applications. New York: Wiley, 2002, pp. 239–243.

[22] G. Mathur, S. Gowda, Q. Li, S. Surthi, S. Tamaru, J. Lindsey, and V. Misra, “Hybrid CMOS/molecular memories using redox-active self-assembled monolayers,” in Proc. IEEE-Nano Conf., vol. 2, 2003, pp. 307–310.

[23] G. Mathur, S. Gowda, Q. L. Li, S. Surthi, Q. Zhao, and V. Misra, “Properties of functionalized redox-active monolayers on thin silicon dioxide—A study of the dependence of retention time on oxide thickness,” IEEE Trans. Nanotechnol., vol. 4, pp. 278–283, 2005.

[24] A. J. Bard and L. R. Faulkner, Electrochemical Methods-Fundamentals and Applications. New York: Wiley, 2002, pp. 12–19.

[25] B. E. Conway, “Transition from ‘supercapacitor’ to ‘battery’ behavior in electrochemical energy storage,” in Proc. 34th Int. Power Sources Symp., 1990, pp. 319–327.

[26] Z. M. Liu, I. Schmidt, P. Thamyongkit, R. S. Loewe, D. Syomin, J. R. Diers, Q. Zhao, V. Misra, J. S. Lindsey, and D. F. Bocian, “Synthesis and film-forming properties of ethynylporphyrins,” Chem. Mater., vol. 17, pp. 3728–3742, 2005

- End of publication -

5.4 MoleFET incorporating Porphyrin Polymer

As discussed earlier, one of the ways to improve the read window or increase the magnitude of the threshold voltage shift due to redox charge (ΔV_T) is to increase the redox charge density ($\boldsymbol{Q_{redox}}$). Porphyrin polymer (**Por-Poly**) film with charge density as high as ~ 10^{15}/cm^2 can be formed on Si or ultra-thin SiO_2 surfaces by in-situ polymerization of porphyrin monomer molecules functionalized with two acetylene groups (**Por-m**). The details of the **Por-Poly** attachment and electrochemical characteristics were given in second and third chapters, respectively. The following sections discuss electrical properties of MoleFET device incorporating **Por-Poly** film.

5.4.1 Improving Read Window

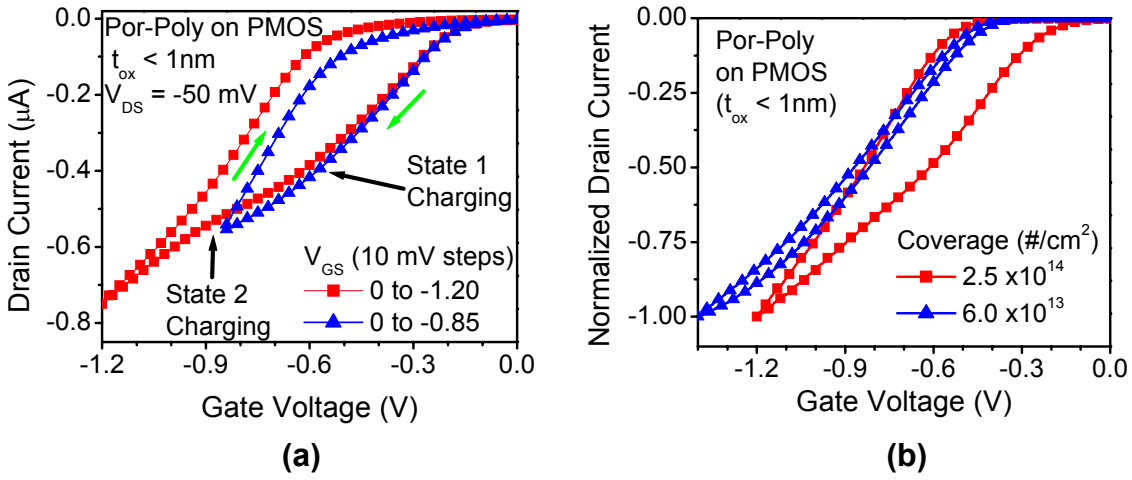


Figure 5.3 I_D-V_G characteristics of MoleFET device incorporating porphyrin polymer (**Por-Poly**) films showing: **(a)** two-step hysteresis associated with the two redox-charge states of porphyrin, and (b) dependence of magnitude of threshold-voltage shift (ΔV_T) on charge-density in the **Por-Poly** film. The green arrows indicate the gate voltage (V_G) sweep direction.

Fig. 5.3 shows I_D-V_G characteristics of the MoleFET (electrolyte gate) incorporating **Por-Poly** film on an ultra-thin tunnel oxide ($\boldsymbol{t_{ox}}$ < 1 nm) of PMOS Si FET. Two-state hysteresis was observed corresponding to the redox-charge states of the porphyrin molecules, as can be seen in Fig. 5.3 (a). The magnitude of hysteresis or ΔV_T of single (first) redox-state was improved to ~ 250 mV as compared to that of MoleFET incorporating a ferrocene (**Fc-P**) monolayer, which was around 50 mV. As expected, this suggests that increasing the charge density in the molecular layer does increase ΔV_T. Further, ΔV_T was

studied as function of redox-charge density by varying the number of molecules in the **Por-Poly** film and it was observed that the magnitude of ΔV_T correlated to the coverage (extracted from the gate-substrate CyV) of the **Por-Poly** film (Fig. 5.3 (b)). However, in case of MoleFET with higher coverage of the **Por-Poly** film, the intrinsic (or virgin) threshold voltage (V_{T0}) of the device was lower than that of the device with lower coverage. This contravenes the expectation of a higher V_{T0} for the MoleFET with higher coverage since the **Por-Poly** film thickness is higher (i.e. background capacitance is lower). So there is a strong possibility that with increasing **Por-Poly** film thickness, there is increasing inclusion of background positive charges (not related to redox) in the bulk of the film, which is gating the device to a lower V_{T0}. Increasing the Por-P thickness to obtain coverage ~ 5 x 10^{14} cm^2 further shifted V_{T0} to positive gate voltages suggesting that the density of non-redox bulk charges increased thereby gating the device to depletion mode. This can be observed in Fig. 5.4 (a), where the V_{T0} of the device is ~ + 0.6 V. I_D-V_D characteristics of the device was in agreement with this V_{T0} value and also, the source-to-drain IV also further confirmed that the FET device was indeed ON with gate terminal floating (or grounded), as can be seen from Fig. 5.4 (b). The charging/discharging of non-redox bulk charges in **Por-P** film may also contribute to the observed hysteresis although experiments with control non-redox polymer films suggested that such a contribution might be small.

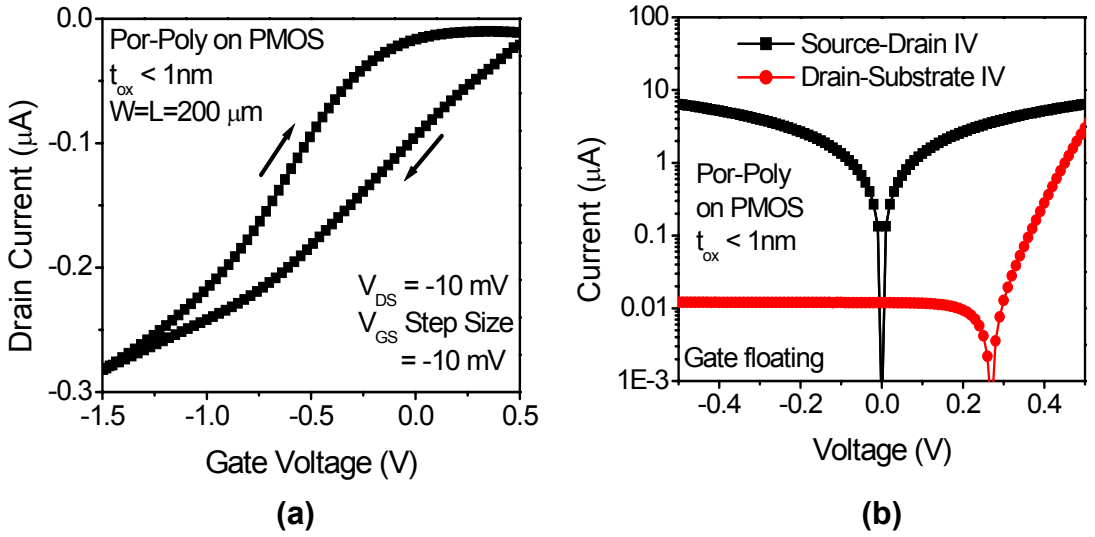


Figure 5.4 (a) I_D-V_G characteristics of MoleFET with **Por-P** film (coverage ~ 5 x 10^{14} cm^2) showing positive V_{T0} of the device. **(b)** Source-Drain IV showing the FET channel is conductive (ON state) even with gate floating (or grounded) and the origin of this current not related to source/drain to substrate diode reverse leakage (Drain-Substrate IV).

5.4.2 Multi-bit MoleFET

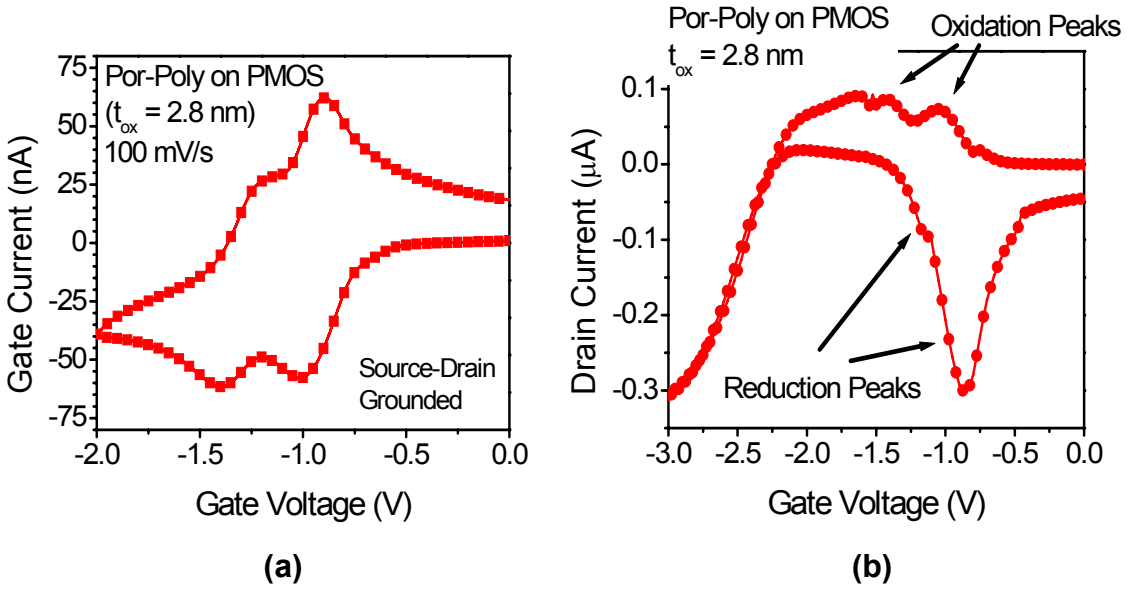


Figure 5.5 High V_T MoleFET device incorporating **Por-Poly** film. **(a)** Gate CyV with source-drain terminals grounded. **(b)** I_D-V_G showing peaks in the subthreshold region associated with redox of molecules on the gate-to-source/drain overlap regions.

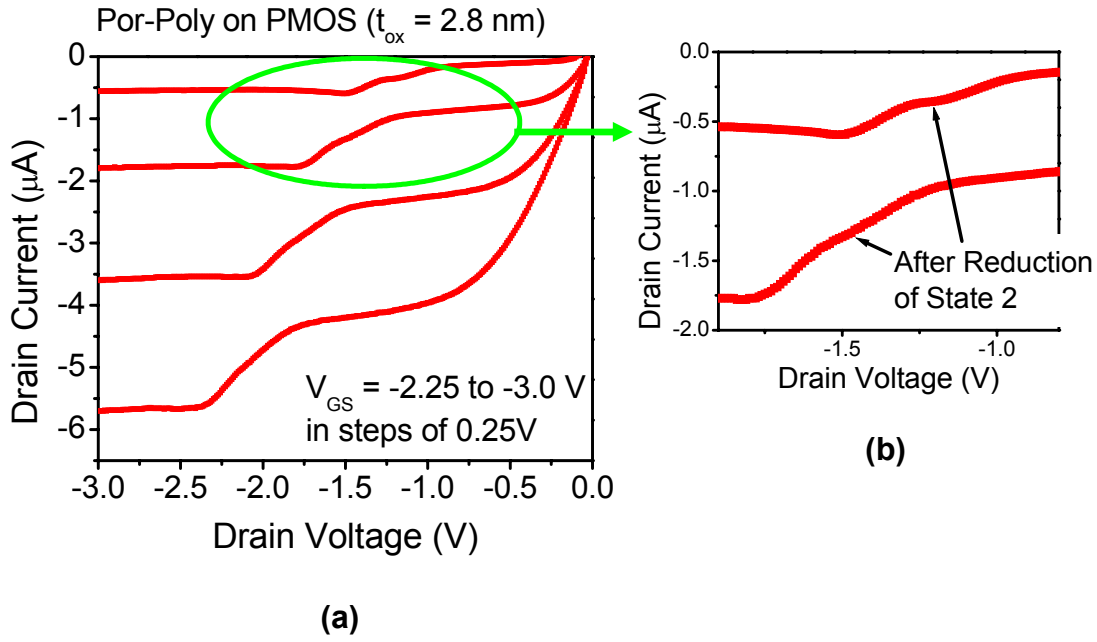


Figure 5.6 (a) I_D-V_D characteristics of High V_T MoleFET incorporating **Por-Poly** film showing two-step increase in drain current associated with reduction of oxidized (both states) porphyrin molecules on the channel region near the drain. The transistor was ON for the gate voltages shown (V_{T0} ~ 1.8 V). **(b)** Magnified view of a portion of plot in (a) showing a plateau in I_D-V_D after reduction of the second oxidized state of the porphyrin molecules.

MoleFETs with higher V_{T0} (thicker gate oxide) were fabricated incorporating porphyrin polymer (**Por-Poly)** films, and observations similar to high V_T devices containing ferrocene (Fc-P) monolayers, discussed in earlier in this chapter, were made. Fig. 5.5 (a) shows the gate-to-substrate CyV, with source-drain terminals grounded, of one such device. The I_D-V_G characteristics of the device is shown in Fig. 5.5 (b), where in the peaks associated with redox of molecules on the source/drain overlap regions are observed in subthreshold region of the curve. As mentioned previously, the direction of the oxidation and reduction currents is swapped because the gate current is in the opposite direction to the drain current. Further, I_D-V_D characteristics of the device, for gate voltages higher than V_{T0}, (Fig. 5.6) showed a two-step increase in the drain current associated with reduction of porphyrin molecules on the channel region near the drain of the device. Each step increase in drain current corresponds to reduction of one redox-state of the porphyrin, which has two redox-charge states. The first step increase (traversing along the scan direction, which is negative drain voltage direction) is due to reduction of the second porphyrin redox state. Since the separation of the two redox states is very small as can be observed from the reduction scan of the gate CyV shown in Fig 5.5 (a), the two-step increase is not very apparent. However, magnifying a portion of Fig. 5.6 (a), as shown in Fig. 5.6 (b), it can be observed that there exists a small plateau (constant dI_D/dV_D) and the increase in the drain current is indeed a two-step event. Also, I_D-V_D characteristics of the device in subthreshold region showed two transient peaks related to the reduction of porphyrin molecules on the overlap region. Hence, this demonstrates multi-state modulation of the drain current of Si FET using redox-active molecules with multiple states.

Fig. 5.7 shows the comparison of FET characteristics of the MoleFET device containing ferrocene monolayer vs. the device containing porphyrin polymer film. Essentially, the drain current modulation observed in both the devices is characteristic of the redox-centers contained in the respective device: (i) ferrocene has single redox state with characteristic redox potential of around - 0.5 V on p-Si and porphyrin has two redox states with access potentials of -0.9 and -1.2 V. The redox transient peaks observed in sub-threshold region of the MoleFET devices (Fig. 5.7 (a)) and the drain current increase step transition voltages (V_{GD} in Fig. 5.7 (b)) are consistent with these values. (ii) ferrocene is incorporated as monolayer, whereas porphyrin is in polymer with redox-charge density of latter being around 5X that of the former in case of the devices compared in Fig. 5.7. This

difference is reflected in the respective magnitudes of the current density. It should be noted that current axis for the MoleFET containing ferrocene is the secondary (right) y-axis in case of Fig. 5.7.

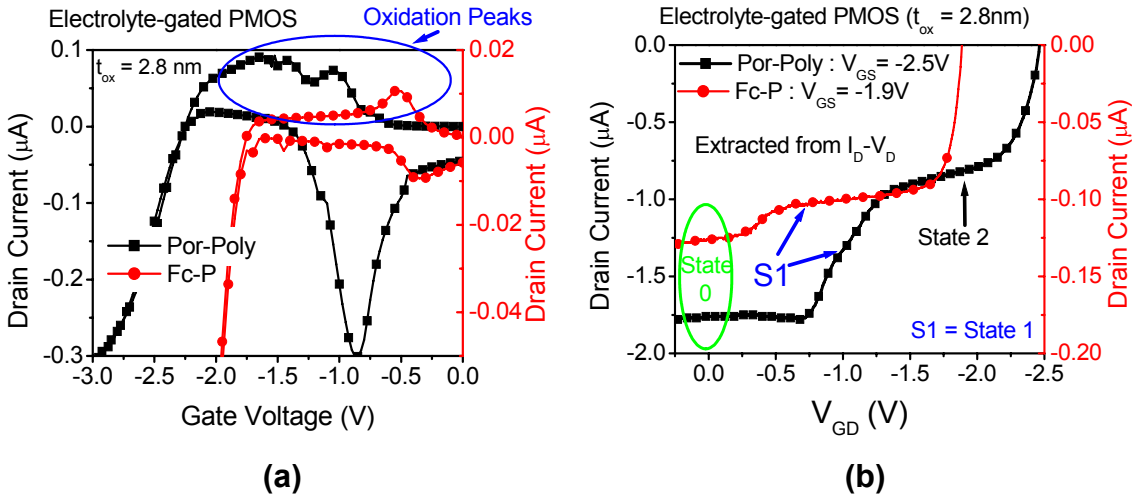


Figure 5.7 Comparison of characteristics of MoleFET containing ferrocene (single redox-state) monolayer (**Fc-P**) vs. MoleFET containing porphyrin (two redox-states) polymer (**Por-P**). The drain current of **Fc-P** MoleFET corresponds to the secondary y-axis shown in red.

5.5 Summary

Based on the findings discussed in chapters 3 and 4, the redox-active molecules were incorporated on an ultra thin gate-oxide of Si MOSFETs with the intent of studying the interaction of redox states with Si MOSFETs and investigating for Flash applications. PMOS FET devices were used in these studies since the redox-active molecules utilized have cationic-accessible states, which are accessible under negative gate voltages. This is region of transistor operation for the PMOS enhancement-mode devices. In order to use the NMOS devices, molecules with anionic-accessible states are required.

PMOS FET devices were fabricated using conventional CMOS processing techniques. The FET process flow was based on replacement-gate technology and had 5-level mask set. The molecules were attached on ultra-thin gate oxide and an electrolyte gate was used for electrical characterization.

The quantized energy states in the molecules manifested in the drain current and threshold voltage characteristics of the PMOS device at room temperature. Transient peaks

associated with redox of molecules were observed in the sub-threshold region of I_D-V_G characteristics of MoleFET device confirming the interaction of the redox-energy states with the Si FET. The I_D-V_D characteristics of the MoleFET device displayed the modulation of the drain current due to redox-energy states.

The modulation of threshold voltage characteristics due to redox-charge was observed as hysteresis in the FET transfer (I_D-V_G) characteristics. Hysteresis characteristics were dependent on the barrier oxide thickness, the number of molecules involved in redox activity, and the measurement scan rate.

The magnitude of hysteresis was relatively small (~ 50 mV) in case of MoleFET containing redox-active monolayers due to large value of the electrolyte double-layer capacitance. The magnitude of hysteresis (or read window) was significantly improved by increasing the redox charge densities using redox-active polymer films.

Multi-state modulation of the drain current and threshold voltage characteristics of the FET device was demonstrated by incorporating three-state (two cationic-accessible redox-states) porphyrin molecules.

5.6 References

[1] *International Technology Roadmap for Semiconductors 2005, Emerging Research Devices*, 2005.

6 SUMMARY AND FUTURE OUTLOOK

The primary focus of this research work was to gain fundamental insights into the interaction of redox-energy states with silicon substrate and explore approaches for exploiting the unique charge-storage properties of the redox-active molecules in hybrid silicon-molecular memory devices for DRAM and Flash applications. The specific goals of this study were listed in the “Focus of my research” section in chapter 1.

6.1 Conclusion and Specific Findings

The research efforts of this dissertation work led to a better understanding of the redox-energy states in the molecules. More importantly, the properties of the molecules were evaluated from a perspective of hybrid silicon-molecular devices in order to achieve realistic solutions for molecule-based memory applications. The following is list of specific contributions and findings of this work:

I. Electrically stable monolayers of redox-active molecules, two-state ferrocene and three-state Zn-porphyrins, were assembled on Si substrates by wet chemistry attachment techniques. The molecules have cationic-accessible charge states and attach to Si surface via Si-O-C covalent linkages. Electrical characterization of the molecular monolayer immobilized on Si surface was carried out using DC measurement (cyclic voltammetry) and AC measurement (impedance spectroscopy) techniques.

II. The effect of Si doping type and concentration on the redox response of the molecules, in terms of redox voltages (memory cell write/erase voltages), rate kinetics (memory cell write/erase speeds) and charge retention (memory cell data retention time), were studied.

    a. Redox peak potentials were found to be lower in magnitude in case of n-doped Si as compared to p-doped Si.

b. Redox response was independent of the dopant concentration, measurement scan rate and ambient light in case of P-Si. However, in case of N-Si redox response was strong function of these parameters.

c. Redox peak potential increased in magnitude with increasing dopant concentration for a given light intensity for N-Si. Also, for a given dopant concentration, redox peak potential was shifted to lower negative gate voltages with increasing ambient light intensity.

d. It was determined from the experimental observations and analysis that the redox-energy level within the molecules lines up within the valence band edge of the Si, and it exchanges charges with the valence band during redox processes.

e. The differences in the redox response exist in P-Si vs. N-Si substrates due to the state of the Si surface during the redox events in each case. The Si surface is accumulated in case P-Si, while it is depleted in case of N-Si.

III. The molecule-to-silicon barrier was augmented by placing an ultra-thin layer of tunnel oxide (SiO_2, HfO_2) to enhance charge-retention of the hybrid silicon-molecular devices for Flash applications. The redox properties were studied as function of tunnel oxide thickness, energy barrier and dielectric permittivity.

a. Oxidation peak potential shifted to higher negative gate voltages and the reduction peak potential shifted to lower negative gate voltages with increasing oxide thickness, thereby creating a region of no-redox in the voltage axis, which serves as a window for non-destructive cell read in case of the MoleFET device.

b. In case of P-Si the reduction (erase) process was found to be increasingly rate-limited as compared to oxidation (write) process with increasing SiO_2 thickness. This is attributed to asymmetric tunneling rates mainly due to a lower potential drop across the tunnel barrier for a given gate voltage during reduction process as compared to oxidation, resulting from higher surface potential drop in Si.

c. Increasing SiO_2 thickness (t_{ox}) does increase charge retention but dramatically slows down the redox rate kinetics (or write/erase times) for $t_{ox} > 2.5$ nm.

d. By utilizing HfO_2, it is viable to increase the physical thickness of the tunnel barrier to improve charge retention properties of the device with minimal degradation in write speeds as compared to SiO_2. HfO_2 has higher relative permittivity (~20) and has a net lower barrier to holes as compared to SiO_2.

e. A further improvement in speed vs. retention performance trade-off can be made by employing asymmetric (HfO_2/Al_2O_3 bilayer stack) or symmetric (trilayer stack) layered tunnel barriers.

IV. The properties of the molecules can be tailored by molecular design and synthetic chemistry. In this work, it was demonstrated that an alternate route to tune/enhance the properties of hybrid device was to engineer the substrate (silicon) component.

a. Redox peak potentials shift to higher negative gate voltage in case of molecules on N+/P Si diode and shifts to lower negative gate voltages in case of P+/N Si as compared to molecules on just P-Si.

b. Charge retention of the molecules is enhanced on N+/P Si diode as the reduction is a rate-limited process. This is attributed to the reverse recovery time of a forward-biased diode. SPICE simulations were carried out to further illustrate this.

c. N+ pockets in p-well silicon substrate were used to demonstrate the concept of achieving multi-bit by substrate engineering.

d. A novel method to detect and estimate the lateral conductivity within immobilized molecular layer was proposed and demonstrated.

V. The redox-active molecules were incorporated on an ultra thin gate-oxide of Si MOSFETs with the intent of studying the interaction of redox states with Si

MOSFETs and investigating for Flash applications. PMOS FET devices were used in these studies since the redox-active molecules utilized have cationic-accessible states, which are accessible under negative gate voltages (PMOS transistor operation region). In order to use the NMOS devices, molecules with anionic-accessible states are required.

a. The quantized energy states in the molecules manifested in the drain current and threshold voltage characteristics of the PMOS device at room temperature.

b. The modulation of threshold voltage characteristics due to redox-charge was observed as hysteresis in the FET transfer (I_D-V_G) characteristics. Hysteresis characteristics were dependent on the barrier oxide thickness, the number of molecules involved in redox activity, and the measurement scan rate.

c. The magnitude of hysteresis (or read window) was significantly improved by increasing the redox charge densities using redox-active polymer films.

d. Multi-state modulation of the drain current and threshold voltage characteristics of the FET device was demonstrated by incorporating porphyrin molecules.

6.2 Approaches towards Integration

The results and discussion presented in this dissertation, so far, pertains to electrolyte gate as the top contact. The role of the electrolyte was discussed in chapters 2. As discussed previously, the electrolyte makes an ideal contact to the molecules and facilitates the evaluation of the unique properties of redox-active molecules for nano-scale memory applications. There have been several demonstrations of electronic (non-molecule) devices incorporating solid-state electrolytes such as (i) nano-scale conductance (resistive) switch [1-3], and (ii) electrolyte-gated nanotube FET [4, 5]. Although, hybrid silicon-molecular memory devices with solid-state electrolyte can be potential route for large-scale integration, an alternative approach replacing the electrolyte (double-layer) with a

combination of ultra-thin high-K dielectric and metal gate (Fig. 6.1) is definitely a more viable solution.

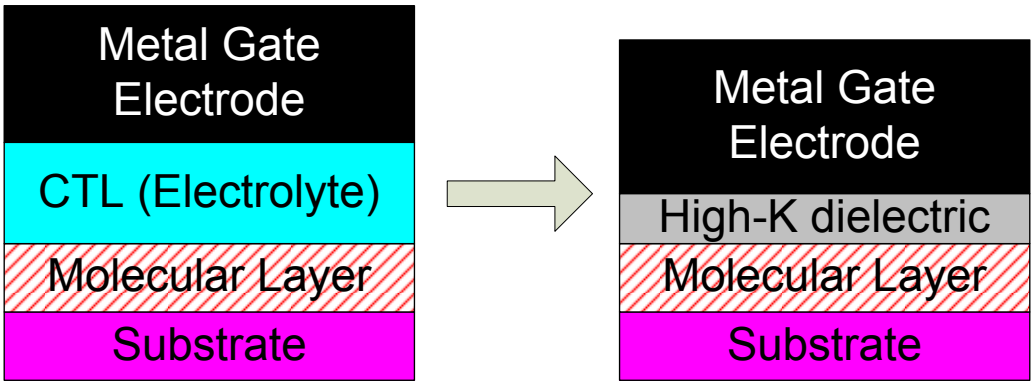


Figure 6.1 Schematic depicting the concept of replacement of electrolyte gate with a combination of ultra-thin high-K dielectric layer and metal gate. Electrolyte is considered as a charge-transfer layer (CTL) as the electrolyte provides screening charges in close proximity to molecules in form of ions.

The main advantages of a complete solid-state solution over electrolyte-based integration approach are as follows:

1. Ease of Integration: Complete solid-state solution can be easily integrated into the current industry-standard CMOS process flows. For example, in case of DRAM applications, the hybrid capacitor can be integrated at back-end of the line (BEOL) as certain molecules have been shown [6] to survive the highest temperatures (400 ^{o}C) involved in the BEOL. In case of solid-state electrolytes, the integration into CMOS platform is not as trivial and overcoming the challenges involved such as thermal instability, process variability etc., can be monumental.

2. Faster Cell Operation: As discussed in chapter 2, the redox-state charges in the molecules are screened by the ionic charges in the electrolyte. One of the circuit elements of electrolyte-gated hybrid capacitor is the series resistance ($\mathbf{R_s}$) of the electrolyte attributed to the migration of ions in the bulk of the electrolyte. Since ion movement is typically slower as compared to electronic conduction, $\mathbf{R_s}$ adds considerable amount of parasitic delay, thereby slowing down the charging/discharge rates of the cell. However, a complete solid-state solution,

where the redox charges are screened by electrons in the metal gate, will circumvent this problem enabling faster cell operation.

The following sections contain experimental attempts to replace the electrolyte gate and characterize the redox-charge states in the molecules in a completely solid-state cell. These efforts were primarily targeted for the DRAM applications where the hybrid capacitor can be integrated at the BEOL with access transistor in the front-end of the line (FEOL). Also explored was a hybrid integration approach involving both metal gate over high-k dielectric, and electrolyte, which may reduce $\mathbf{R_s}$. Preliminary results of solid-state MoleFETs are also presented in a later section.

6.2.1 Fabrication of Solid-State Cell

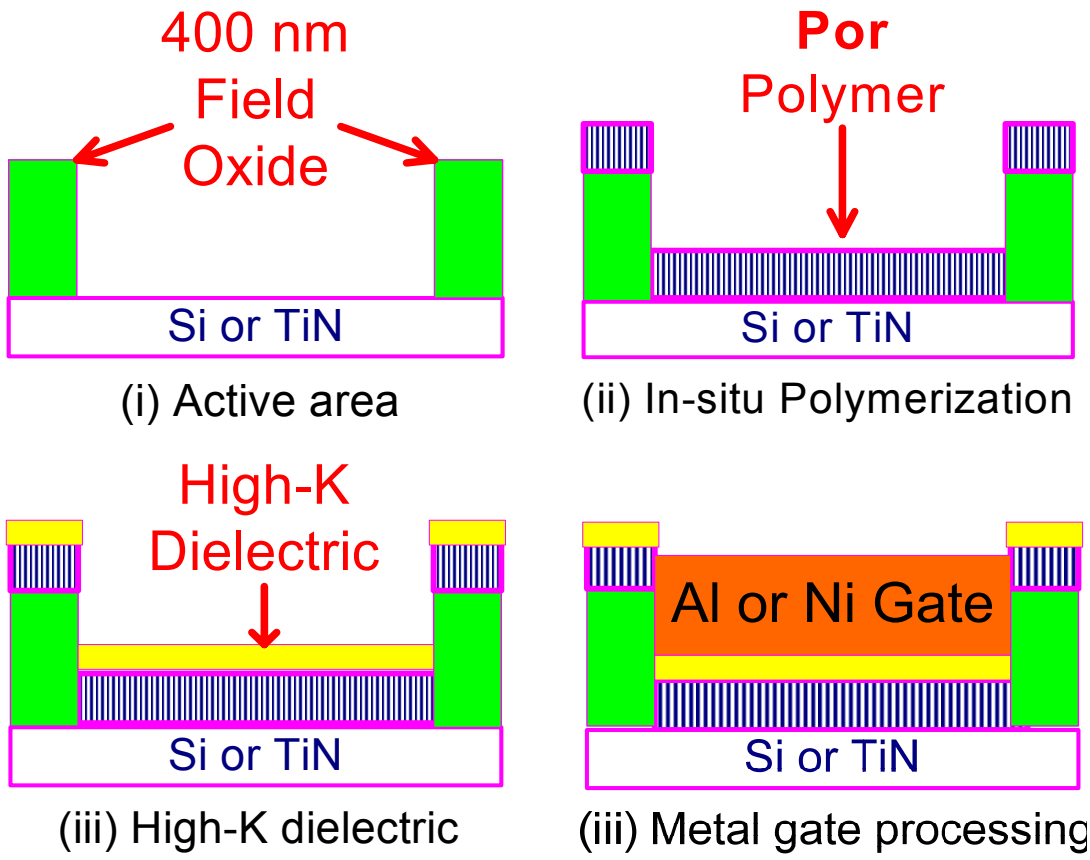


Figure 6.2 Process flow for fabrication of solid-state (dry) hybrid silicon-molecular capacitor.

Solid-state hybrid capacitors were fabricated on Si and titanium nitride (TiN) substrates. In the semiconductor industry, TiN is widely employed as diffusion barriers and contact metal for interconnects and is commonly processed in BEOL [7]. Hence TiN was chosen as a metal substrate for the integration explorations since the hybrid capacitors are incorporated in BEOL for DRAM applications. Also, experiments were carried out with Si substrate to as a control and also to investigate for MoleFET solid-state integration.

Fig. 6.2 shows steps involved in the fabrication of the solid-state cell. Active area of the cell (typically 100 μm x 100 μm) was defined by: (i) using a 400 nm field oxide in case of Si substrate, or (ii) patterning the TiN and depositing isolation LTO. This was followed by surface treatment with 1% hydrofluoric acid (HF) and in-situ polymerization to form **Por-Poly** film using techniques described in chapter 2. Polymer films of the redox-active molecules were employed instead of the monolayers since the former were expected (and were found) to be more resilient to processing of solid-state over-layers. Non-redox polymer films were used as controls. The high-K dielectric used in most of the experiments in this work was Aluminum Nitride (AlN). AlN was deposited using reactive sputtering of Al in N_2. Other dielectric layers investigated include Alumina (Al_2O_3) and Hafnium dioxide (HfO_2) deposited by atomic layer deposition (ALD). Aluminum (Al) or Nickel (Ni) gate (~ 150 nm) was deposited by thermal evaporation through a shadow mask. Experiments were also carried out by patterning the Al gate by photolithography (lift-off or etch) processing techniques. Control capacitors with metal gate deposited directly over the **Por-Poly** films were also fabricated. More details about the process flow can be found in another student's dissertation [8].

6.2.2 Completely Dry Cell: Capacitance-Voltage Characteristics

The current-voltage (IV) characteristics of completely dry cell (Al/AlN/**Por-Poly**/Si) exhibited parallel-plate (MIM) capacitor behavior. Further, capacitance-voltage (CV) measurements were performed on these capacitors. The CV characteristics of the capacitors revealed peaks (shoulder) and also shift in flatband-voltage in the form of hysteresis (Fig. 6.3). Peaks in CV are typically suggestive of high density of interface traps (D_{it}) at the Si-polymer interface. The simulated CV characteristics of the capacitors indicated that peaks in CV are observed only if the D_{it} were greater than $5x10^{13}$ /cm^2.

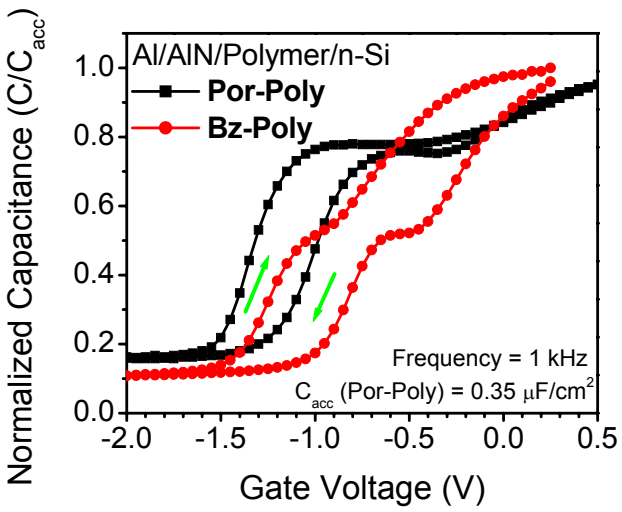


Figure 6.3 CV characteristics of Al/AlN/Polymer/n-Si capacitors. The thickness of Al and AlN films were around 150 nm and 40 Å, respectively. **Bz-Poly** is a control (non-redox) polymer. The concentration of attachment solution was around 4mM in case of **Por-Poly** and estimated film thickness was 20 nm.

Hysteresis or flatband voltage shift in negative direction is indicative of positive charge-trapping in the bulk of the film. The interface traps and bulk charges that manifested as peaks and hysteresis in CV characteristics may not be related to the redox-charge centers in the **Por-Poly** film as similar characteristics were also observed in case of capacitors with control (non-redox) polymer (Fig. 6.3). However, CV characteristics of another type of control capacitors without any organic polymer did not exhibit any hysteresis indicating that the charge centers were located in the bulk of the polymer film. These control capacitors (Al/AlN/Si) had Si surface exposed to polymerization solvent, ambient and temperatures.

In case of **Por-Poly** capacitors, it was observed that the width of the peaks in CV increased with increasing thickness of the dielectric layer on top of the polymer film similar to that in simulated CV. The peaks in the simulated CV disappeared when the states were moved away from the silicon interface and this was observed in the experiments as well when the polymer film was on top of a thin SiO_2. The magnitude of the hysteresis varied between 0.5-2.0 V depending on the thickness of the dielectric layer. Although, CV measurements suggest that the polymerization process and the polymer film might be origin

of the interface traps and bulk charges, these measurements do not provide any information regarding the charging and discharging of redox-states in **Por-Poly** film.

6.2.3 Completely Dry Cell: Photoelectric Effect

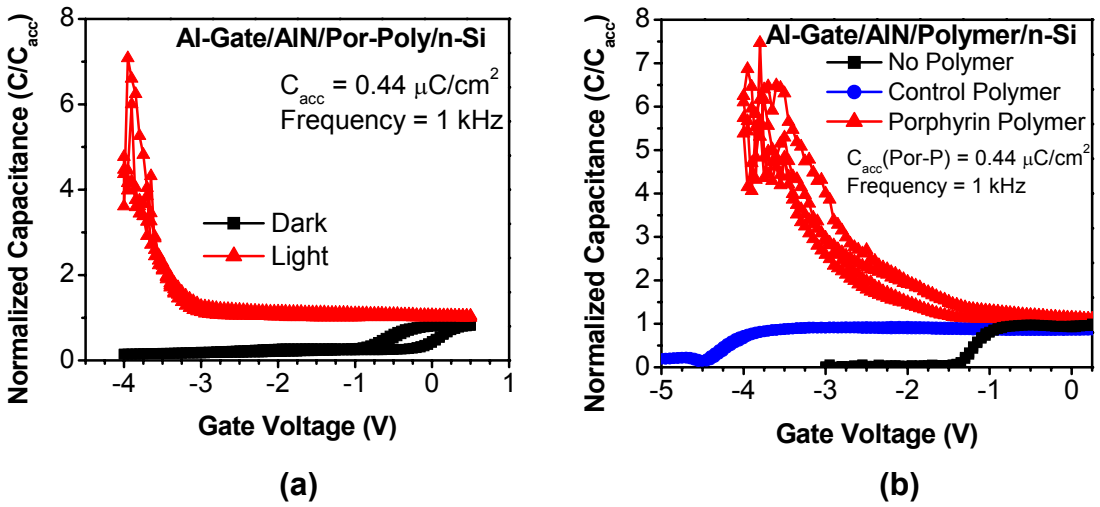


Figure 6.4 CV characteristics of Al/AlN/Polymer/n-Si capacitors showing photoelectric effect: **(a)** Depletion capacitance of capacitor containing **Por-Poly** increases beyond accumulation capacitance under ambient light conditions. **(b)** Depletion capacitance of control capacitors: (i) containing control (**Bz-Poly**) polymer, and (ii) without any polymer (just polymerization control) does not increase beyond accumulation capacitance. The thickness of Al and AlN films were around 150 nm and 40 Å, respectively.

In the recent years there has been research to explore, evaluate, and develop non-conventional solar electric technologies utilizing multi-porphyrin arrays [9-11]. Our collaborators (Jonathan Lindsey, NCSU and David, Bocian, UC Riverside) are involved in design and synthesis of porphyrin-based artificial light-harvesting arrays that rival those in plant photosynthetic systems. One of the simplest configurations for an organic solar-cell employing multi-porphyrin array is to attach one end of the array to a planar wide band-gap semiconductor [11]. Towards that extent we investigated the opto-electronic properties of **Por-Poly** on Si substrates by performing CV measurements of **Por-Poly** containing capacitors (Al/AlN/**Por-Poly**/n-Si) were carried out under ambient light and dark conditions. N-Si doping type was selected for these measurements so as to drive the silicon surface to depletion for negative gate voltages and enable separation of charges, if any, produced in **Por-Poly** film under irradiation. As can be seen in Fig. 6.4 (a), the capacitance of the device increases to significantly higher values for negative gate voltages as compared to the

accumulation capacitance of the device under ambient light. The increase in capacitance is indicative of a generation process in the stack or change in dielectric constant of **Por-Poly** film due to a photo-induced process. The control capacitors: (i) incorporating non-redox polymer and (ii) without any molecules (but silicon surface exposed to thermal treatment with solvent) did not exhibit increase in capacitance values in the same gate voltage range, as shown in Fig. 6.4 (b).

This work needs further exploration for possible low-cost solar-cell applications.

6.2.4 Completely Dry Cell: Resistive Switching with Metal Substrates

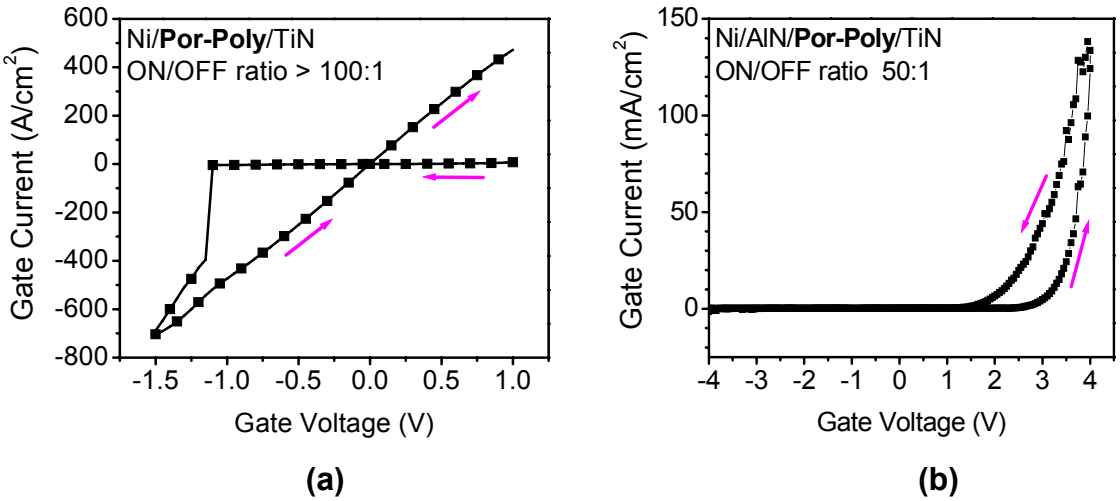


Figure 6.5 Resistive-switching observed in: **(a)** Ni/**Por-Poly**/TiN, and **(b)** Ni/AlN/**Por-Poly**/TiN capacitors. The thickness of Ni and AlN films were around 150 nm and 40 Å, respectively. The concentration of attachment solution was around 4mM for **Por-Poly** and estimated film thickness was 20 nm.

Insulator resistance change memory is one of the prominent emerging research memory concepts as discussed in chapter 1. Resistance (conductance) switching is observed in variety of concept devices, which consist of ultra-thin insulating barriers (such as high-K dielectrics, organic films etc.) sandwiched between two metal electrodes. The exact mechanism is not clear but the bistable resistive switching is widely attributed to formation and dissolution of metal nano-filaments through the insulating barrier [12]. There are other fancy theories to explain the switching mechanisms although corroborating experimental evidences are limited: (i) voltage induced switching between Fowler-Nordheim

tunneling (OFF or low conductance state) and Frenkel-Poole tunneling (ON state), (ii) switching between space-charge limited tunneling (OFF state) to trap-assisted tunneling (ON state) [13, 14]. It has been also found that the electrode materials have a strong role to play in the resistive switching characteristics [13]. However, it is yet to be determined if the switching is related to changes in the electrode-insulator interface(s) or bulk of the insulator.

Resistive switching was observed in dry measurements of our capacitors incorporating **Por-Poly** film in a variety of stack configurations. The phenomena were irreversible and unpredictable in case of capacitors with: (i) Si substrates (say Al/**Por-Poly**/Si or Al/AlN/**Por-Poly**/Si), and (ii) Al gate and TiN substrate. However, reversible resistive switching, with relatively small device-to-device variations, was observed in case of Ni-gated capacitors containing **Por-Poly** film on TiN substrate (Fig 6.5). Some of the key observations made with resistive-switching phenomena in the Ni-gated, TiN substrate capacitors containing **Por-Poly** film were:

I. The magnitudes of the ON/OFF currents (ON/OFF ratio) were more predictable and the switching endurance was generally higher in case of capacitors incorporating ultra-thin layer of AlN between Ni-gate and **Por-Poly** film as compared those with Ni directly on **Por-Poly** film.

II. The magnitude of the ON-state current density was significantly lower (by almost 4 orders) in case of capacitors with AlN (Fig. 6.5 (a)) as compared those without AlN layer (Fig. 6.5 (b)).

III. The ON/OFF ratio was generally higher and the switching voltages were lower in case of capacitors with Ni directly on **Por-Poly** as compared to capacitors with AlN layer (Fig. 6.5).

In summary, reversible and stable resistive switching was observed in Ni/**Por-Poly**/TiN capacitors. Inclusion of ultra-thin layer of dielectric film such as AlN greatly reduces the ON-state current density with minimal degradation in the ON/OFF ratio but increases the switching voltage. Also, the AlN layer improves the endurance of resistive-switching operation. These results suggest that the mechanism of switching is related to the electrode-polymer interface, and may not be

directly linked to the bulk of the polymer film or the redox-charge centers in the polymer film.

6.2.5 Electrolyte Probe Measurements

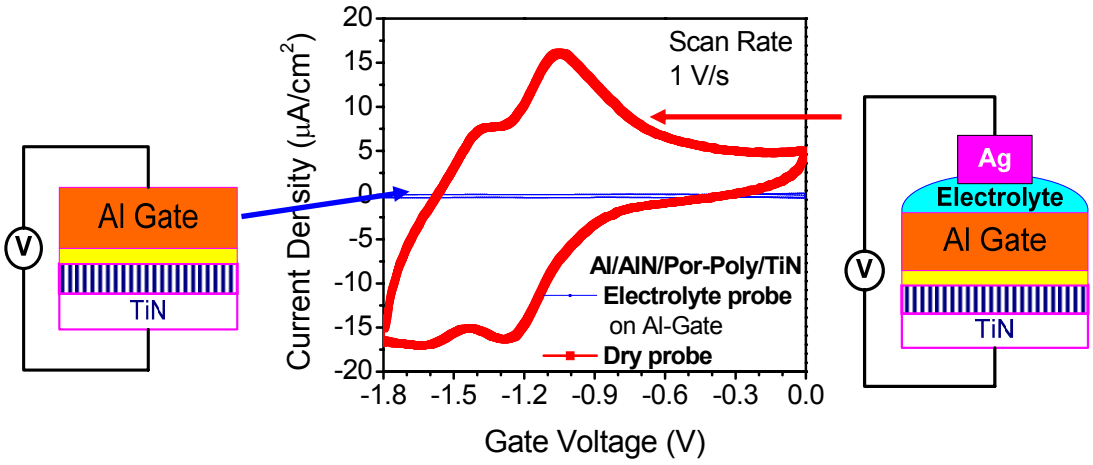


Figure 6.6 Cyclic Voltammetry (CyV) characteristics of Al/AlN/**Por-Poly**/TiN capacitor: (i) completely dry measurement, and (ii) electrolyte-probe on top of Al gate. The thickness of Al and AlN films were around 150 nm and 40 Å, respectively. The concentration of attachment solution was around 4mM for **Por-Poly** and estimated film thickness was 20 nm.

Dry voltammetry (CyV) of Al/AlN/**Por-Poly**/TiN showed only parallel-plate capacitor charging without any distinct redox behavior as can be seen in Fig 6.6. However, the same structures measured with an electrolyte probe revealed peaks in current corresponding to charging and discharging of two redox states of the porphyrin molecule (Fig. 6.6). The measurement is termed connected drop (CD). This indicates that the porphyrin polymer survived the deposition of solid-state capping layers thereby retaining the redox properties. Similar measurements were also made in case of capacitors with (i) Si substrate (Al/AlN/**Por-Poly**/Si), and (ii) Ni gate (Ni/AlN/**Por-Poly**/TiN). The measured charge-density (or coverage) was typically an order of magnitude lower than that compared to the starting coverage of **Por-Poly** film (i.e. coverage measured with electrolyte probe directly on **Por-Poly**/TiN). In the CyV measurement of electrolyte gated **Por-Poly**/TiN control capacitors, it was found that there was timing effect with the magnitude of redox peak currents increasing with measurement and this has been detailed in another student's dissertation [15]. Similar timing effect was also observed in case of CyV characteristics of electrolyte-probe on AlN/**Por-Poly**/TiN capacitors. However, no such timing (or insignificant) effect was observed

in case of CD measurements. The redox-related peaks were observed in the first CyV scan and the magnitude of redox peak currents did not increase significantly.

The absence of redox-related peaks in completely dry cell measurement can be attributed to one of the two reasons – (i) CyV measurement is much slower compared to redox kinetics in dry cell and hence cannot capture the transients associated with charging and discharging of molecules, or (ii) it is necessary for the screening charges to be in close proximity of the molecules in the polymer film for oxidation (molecule losing an electron) and electron-hopping in the polymer film and this may be provided for in case of electrolyte gate where in the counter-ions can possibly migrate/diffuse through the metal gate into the matrix of the polymer film. Several experiments were carried out to identify the exact reason for these observations and some of these are discussed in the next few sections.

6.2.6 Floating Drop Measurements

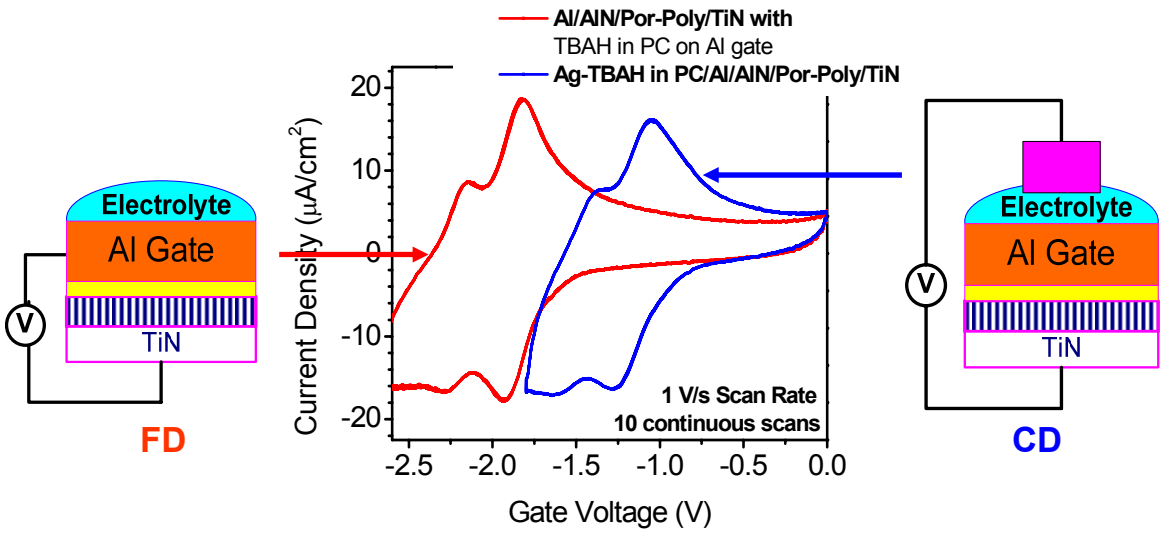


Figure 6.7 CyV of characteristics of Al/AlN/**Por-Poly**/TiN capacitor: (i) floating drop (FD): CyV across Al gate and TiN with electrolyte drop on top of Al gate not connected or electrically floating, and (ii) connected drop (CD): electrolyte-probe on top of Al gate. The thickness of Al and AlN films are around 150 nm and 40 Å, respectively. Electrolyte used was 1 M TBAH in propylene carbonate (PC) and silver (Ag) wire was used to contact the electrolyte in the CD measurement. The concentration of attachment solution was around 4mM for **Por-Poly** and estimated film thickness was 20 nm.

A very interesting observation made with electrolyte on top of Al gate measurements was that peaks associated with charging and discharging of the porphyrin redox-states were

detected in the CyV across Al gate and TiN substrate with an electrolyte drop on top of the Al gate (Fig. 6.7). This measurement is termed floating drop (FD) since the electrolyte drop is electrically open and not connected to any part of CyV measurement circuit. More details of FD measurement set up can be found in Appendix 4. There was a difference in redox peak potentials of around 800 mV between FD and CD measurements as can be observed in Fig. 6.7. This difference is attributed to the gate materials that come into effect in each of these measurements. In case of FD, Al appears to serve as gate, while Ag is the gate in case of CD. When an Al wire was used to contact the electrolyte in CD measurement the redox peak potentials was shifted to higher negative gate voltage by 800 mV as compared to CD measurement with Ag wire. Some of the key observations made in FD measurements of Al/AlN/**Por-Poly**/TiN are listed as below:

1. The measured coverage (and redox peak currents) was identical in case of FD and CD measurements for a given sample. Also, there was no timing effect observed with continuous CyV scans (scan rate < 10 V/s) in FD arrangement and this is similar to observations made with CD measurements.

2. An IV-meter (HP 4155 B) was used to monitor the potentials of the floating terminals in case of FD and CD measurements. Hence, potential at electrolyte floating drop contacted via Ag wire was measured using Voltage-Monitor Unit (VMU) of the IV-meter during FD measurements using the same instrument. Also, potential at floating Al gate was monitored while a CD measurement scan was done. In both the measurements, it was revealed that a potential difference of ~ 800 mV exists between Ag-wire contacting the electrolyte drop and Al gate, when one of the terminals is left floating. Hence, there is open-circuit potential or pseudo-battery potential of 800 mV between Ag-electrolyte-Al, which accounts for the difference in the potentials of FD and CD with Ag wire measurements. This data is presented in Appendix 4 as Fig. 2.

3. CyV measurement of modified FD or CD arrangement where in the electrolyte drop was contacted to Ag wire and tied to Al gate revealed that the redox peak potentials were around half-way between that obtained in pure FD and CD with Ag wire i.e., 400 mV lower negative voltage than FD. This arrangement is termed CD(Ag) + Gate. Also, a pure FD (or pure CD with Ag) measurement scan

following CD(Ag) + Gate measurement indicated some sort of memory effect of potentials in the electrolyte as the redox peak potentials were lower negative (or higher negative) than that of the original pure FD (or pure CD with Ag) measurements and the redox potentials relaxed to the original value after a wait time in minutes.

4. There were no peaks observed in CyV of modified FD arrangement where the electrolyte drop was contacted by a Ag wire, which was then connected to an isolated ground (GND) reference i.e., the electrolyte drop was no longer floating but connected to GND. CyV characteristics of this set up was similar to that completely dry cell (i.e. parallel-plate MIM behavior). However, the magnitude of capacitance was higher in former case as compared to completely dry scenario.

It was observed that in case of FD measurements, the top-most material of the gate directly in contact with the floating electrolyte drop determines the redox peak potentials. The following three results illustrate this point and are presented in Appendix 4 as Fig. 3 and Fig. 4:

I. Redox peak potentials of FD measurements with capacitor structures that had Ni instead of Al as gate material (i.e. Ni/AlN/**Por-Poly**/TiN capacitor) were identical to CD measurements on the same structure using Ag wire. Hence, the redox peak potentials of FD with Al/AlN/**Por-Poly**/TiN structure were higher negative gate voltage by around 800 mV as compared FD with Ni/AlN/**Por-Poly**/TiN.

II. A 10 nm of Ni layer was sputtered on top of the Al gate in the Al/AlN/**Por-Poly**/TiN. Redox peak potentials with the new structure (Ni/Al/AlN/**Por-Poly**/TiN) were higher negative by only 100 mV as compared to CD measurements on the same structure using Ag wire. Hence, the redox peak potentials of FD with Ni/Al/AlN/**Por-Poly**/TiN were similar to that of FD with Ni/AlN/**Por-Poly**/TiN, suggesting that the gate material in contact with electrolyte drop determined the redox peak potential rather gate material closer to the **Por-Poly** film.

III. A 15 nm of Al layer was sputtered on top of the structure mentioned in the last paragraph (Ni/Al/AlN/**Por-Poly**/TiN) to obtain an Al/Ni/Al/AlN/**Por-Poly**/TiN

structure. Redox peaks potentials of FD with this structure were higher negative by around 600 mV as compared to CD measurements on the same structure. Hence, the redox peak potentials of this structure were closer to that of Al/AlN/**Por-Poly**/TiN further illustrating the point that the top-most material of the gate determines the FD characteristics of the cell.

Table 6.1 summarizes these observations of varying redox peak potentials with different gate stack configurations.

Table 6.1 Summary of porphyrin first redox-state peak potential in various cell configurations with respect to the peak potential of electrolyte-gated AlN/**Por-Poly**/TiN control.

Metal Gate (on AlN/**Por-Poly**/TiN)	Measurement Type	Peak potential w.r.t control
Al (150 nm)	CD with Ag	- 800 mV
	FD	0
	CD (Ag) + Gate	- 400 mV
	FD with drop GND	No peaks (MIM behavior)
Ni (150 nm)	CD with Ag	0
	FD	0
Ni(10 nm)/Al	FD	-100 mV
Al(15 nm)/Ni/Al	FD	-600 mV

Another key observation made with the FD measurements was that the peak in CyV associated with charging and discharging of redox-states were detected only if the floating electrolyte drop was directly on the capacitor active area (TiN post). When the electrolyte drop was moved away from the active area, parallel-plate behavior was observed in FD CyV measurements although electrolyte drop was within the Al gate on the overlap region. The

redox peaks recovered in the FD measurements when the electrolyte drop was moved back into the active area of the capacitor under investigation. Hence, the redox charging/discharging was captured in FD CyV measurements only when electrolyte was in contact with the metal gate and also directly over the active area of the capacitor. It may not be possible to access the redox states by contacting the electrolyte to metal gate at a remote location. This is presented in Appendix 4 as Fig. 5.

One of the possible explanations for the redox-related peaks observed in FD measurement can be migration/diffusion of electrolyte solution through the metal gate into the porphyrin polymer film. The diffusion of electrolyte can be through pinholes in the metal gate or through the matrix of the metal gate along the grain boundaries. In order to check for pinholes in the metal gate film, FIB/SEM images (Fig. 6.8) of the capacitor cross-section and Al gate top view were captured. Although, no defects or pinholes were detected, existence of pinholes with dimensions significantly smaller the resolution limit of our SEM tool could not ruled out.

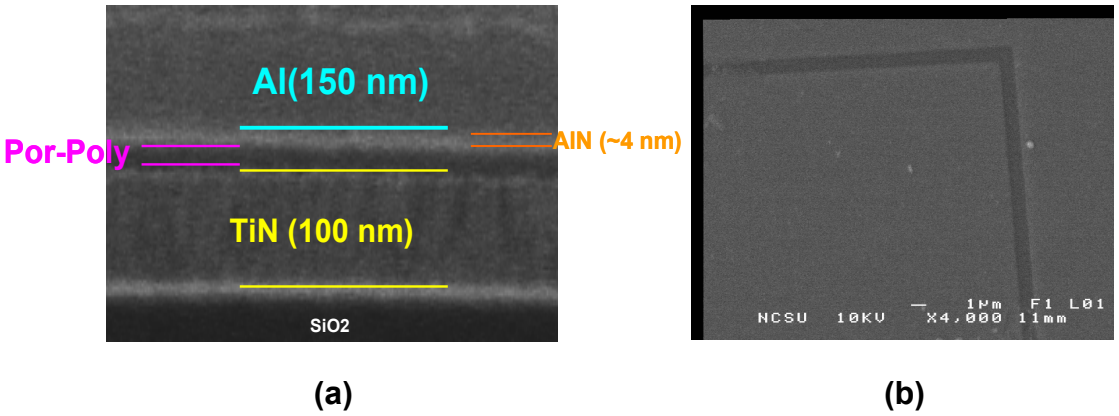


Figure 6.8 Focussed Ion Beam (FIB)/ Scanning Electron Microscopy (SEM) images of Al/AlN/**Por-Poly**/TiN capacitors: **(a)** cross-sectional view of the active area and **(b)** top (flight) view of Al gate. The intersecting dark lines, which are perpendicular to each other in the top view is the trench isolation in the TiN substrate and define the active area of the capacitors. The concentration of attachment solution was around 4mM for **Por-Poly** and estimated film thickness was 20 nm.

Another possible reason for unique observations in FD measurements was incorporation porphyrin molecules into the metal gate (Al or Ni) during evaporation (resistive-heated) of the gate. However, XPS analysis could not detect any presence of porphyrin molecules in the few top atomic layers of Al gate (See Appendix 4, Fig. 6).

In summary, the observation of redox-related peaks in the FD measurements presents new integration opportunities, which are presented in a later section. However, the exact mechanism of transfer of counter-charges required to screen the redox-charges in the molecular layer is not well-understood. There are several possible explanations that can explain these observations and two of the prominent possible mechanisms are described in Fig. 6.9.

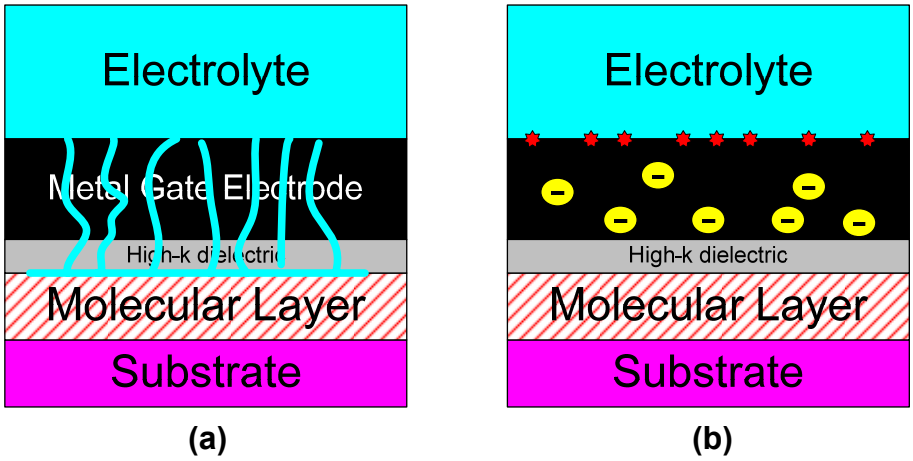


Figure 6.9 Schematic showing two of the several possible mechanism for transfer of charges necessary to screen the redox charges in the molecular layer: (a) Diffusion of electrolyte solution through matrix of (or nano-sized pinholes in) the metal gate, or (b) Reaction at electrolyte-metal gate interface, which may induce slow mobile charges in the metal gate that diffuse towards the molecular layer.

6.2.7 Role of High-K Dielectric Layer

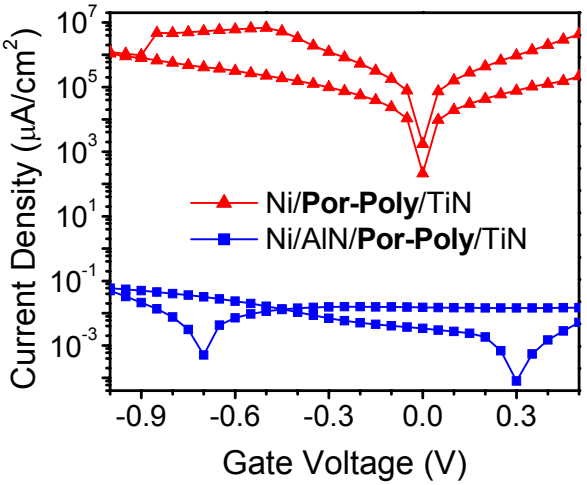


Figure 6.10 IV (dry leakage) measurements of Ni-gated, TiN substrate capacitors containing **Por-Poly** film: (i) with 4 nm AlN layer between Al gate gate and **Por-Poly**, and (ii) without the AlN layer.

The basis for using ultra-thin high-K (AlN) layer between the metal gate and **Por-Poly** film was to replicate the electrolyte double-layer for completely solid-state cells. However, the AlN has a significant role in the {solid-state}-electrolyte hybrid (FD) measurements as well. FD measurements of capacitors without the AlN layer (Al/**Por-Poly**/TiN) did not show any redox-related peaks as the DC leakage current density was very high (almost 5 orders of magnitude higher than the redox peak current value), as can be observed in Fig. 6.10. Also, the resistive-switching and irreversible capacitor device breakdown (electrically shorting of the metal electrodes) was observed even at low gate voltages (~ 1 V) in majority of the devices that were characterized. Incorporating an ultra-thin layer of AlN between the metal gate and **Por-Poly** film resulted in decreased DC leakage by six orders of magnitude (Fig. 6.10). The DC leakage current densities of the Al/AlN/**Por-Poly**/TiN were typically well (at least an order of magnitude) below 1 $\mu A/cm^2$ for gate voltages as high as 3 V. This enabled detection of redox-related peaks in the FD measurements of the structures since the redox peak current values were generally in 10 s of $\mu A/cm^2$ at slow scan rates (i.e. < 10 V/s). Hence, the AlN layer plays the role of an essential DC-blocking layer. It is also expected to act as diffusion barrier to oxygen/moisture, thereby enhancing the stability and electrical endurance of the molecular layer.

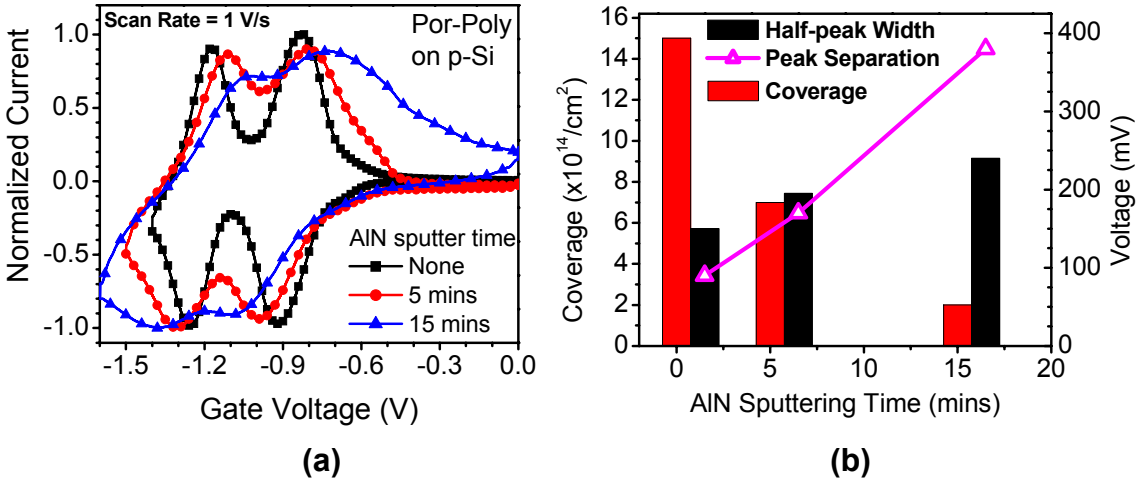


Figure 6.11 Modification of porphyrin redox properties due to the AlN layer: **(a)** Normalized CyV plots of electrolyte-gated AlN/**Por-Poly**/TiN structures with varying AlN thickness at scan rate of 1 V/s. The structure with no AlN is control electrolyte-gated **Por-Poly**/TiN structure. The thickness of AlN is estimated to around 1.2 nm and 4 nm for sputter times of 5 mins and 15 mins, respectively. **(b)** Plot of redox parameters (half-peak width, separation between oxidation and reduction peak, and charge-density/coverage extracted from the first redox peak of porphyrin) vs. AlN thickness.

As discussed earlier, electrolyte probe measurements revealed that the redox centers of the molecules in porphyrin polymer (**Por-Poly)** on silicon and titanium nitride (TiN) surfaces are preserved after the deposition of subsequent high-k dielectrics. It was also found in electrolyte probe measurements of AlN-capped **Por-Poly** that as the thickness of the high-K layer (AlN) increased, the measured redox-charge density decreased, and the redox-kinetics became slower (Fig. 6.11). As can be observed in Fig. 6.11 (a), there is increased separation in potentials of oxidation and reduction peaks, and peak broadening with increasing AlN thickness. This indicates decrease in oxidation and reduction charge-transfer rates with increasing AlN thickness. In addition, the endurance of the porphyrin layers capped with high-K dielectric improved. In summary, the multi-state charge-storage property of redox-active porphyrin polymer is modified in presence of ultra-thin high-K layers. The reasons behind the observed modulation of the redox properties of AlN-capped porphyrin are dependent on the mechanism of redox charging/discharging in CD and FD measurements.

6.2.8 Electrolyte-Last Approach

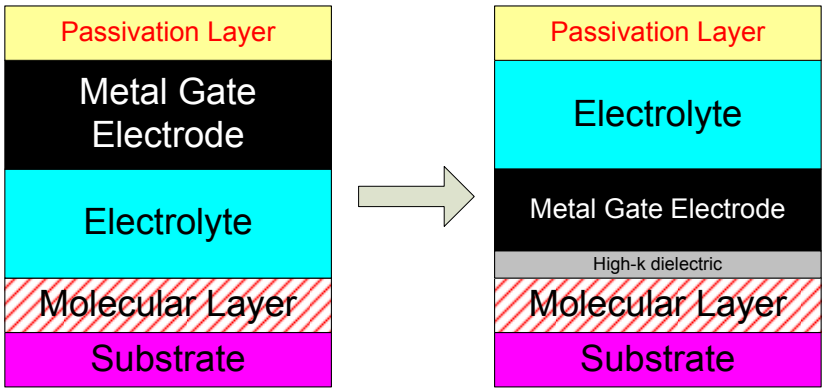


Figure 6.12 Schematic depicting the Electrolyte-Last approach for integration.

Although, a complete solid-state integration approach without incorporation of electrolyte is highly desired and considered ideal, at the time of writing there was no evidence to fact that electrolyte can be completely replaced while preserving the unique properties of the hybrid silicon-molecular charge storage devices. A {solid-state}-electrolyte hybrid approach based on the FD measurement discussed in the previous section is proposed and has the promise of a realistic integration solution. The exact working principle of the FD phenomena is not clear. However, the FD experimental results suggest that an

electrolyte-last approach can be employed as depicted in Fig. 6.12. As mentioned earlier, the key challenges in integrating solid electrolyte directly on top of the molecular layer are: (i) reducing the parasitic series resistance of the electrolyte and increasing the gate-to-molecule coupling ($\mathbf{C_{GM}}$), which necessitates processing of an ultra-thin electrolyte layer to keep the contact metal gate to molecular distance minimum, and (ii) difficulties in processing a good metal contact on the electrolyte layer. This is overcome by the electrolyte-last approach, where the electrolyte is processed after the metal gate-contact and also the distance of the metal gate to molecular layer is fixed by the thickness of the high-K layer between the metal gate and molecular layer. Also, if it is determined that the mechanism of screening charge transfer in FD measurements is due to migration/diffusion of the electrolyte solution through the matrix of (or nano-sized pinholes) in the metal gate, the electrolyte diffusion process can be enhanced by patterning nano-holes in the metal gate as pictured in Fig. 6.13.

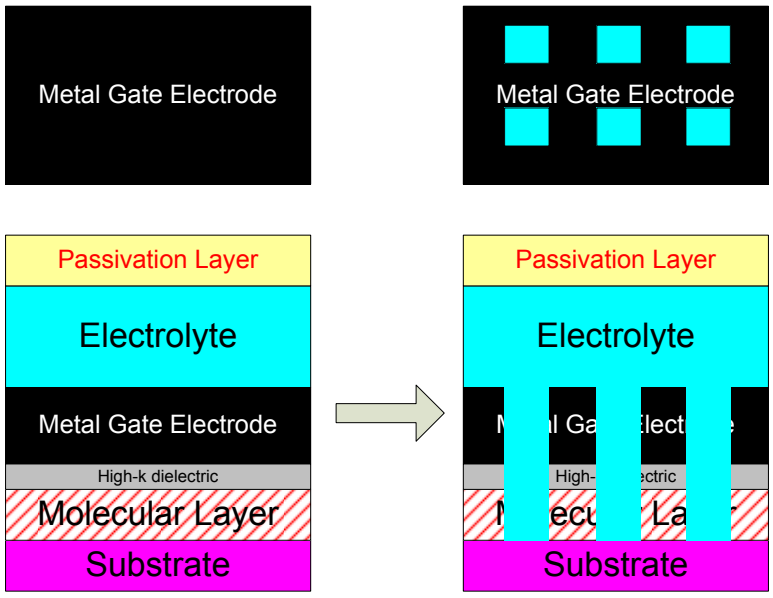


Figure 6.13 Schematic showing a variation of electrolyte-last integration approach.

6.2.9 Preliminary Results on Solid-State MoleFETs

Solid-state MoleFET were fabricated by incorporating **Por-Poly** film on an ultra-thin gate oxide of PMOS Si FET. The structure and electrical characterization setup is shown in Fig. 6.14. The Si FET fabrication and **Por-Poly** attachment was done using procedures detailed in chapters 2 and 5. There were several interesting observations made in the FET characteristics of the device. Preliminary results indicated manifestation of redox-states in modulation of FET characteristics under totally dry measurement conditions and some of the observations made were similar to those observed with electrolyte-gated MoleFET devices. Some of these results are tabulated in Appendix 5. However, more work needs to be done by including controls for better understanding of these results.

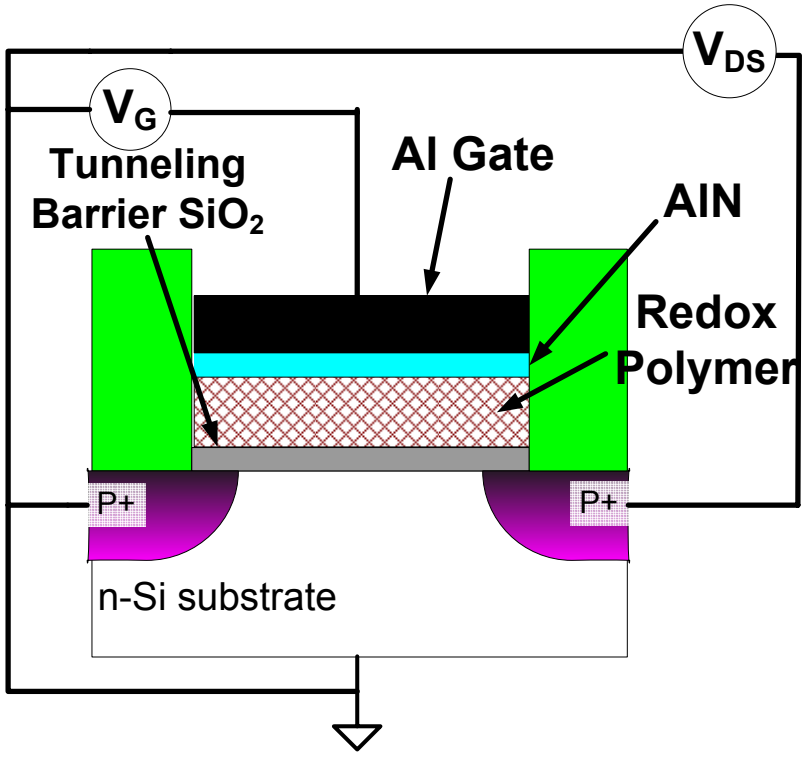


Figure 6.14 Schematic showing the structure and characterization setup of solid-state MoleFET device incorporating **Por-Poly** film.

6.3 A Note on Electrolyte

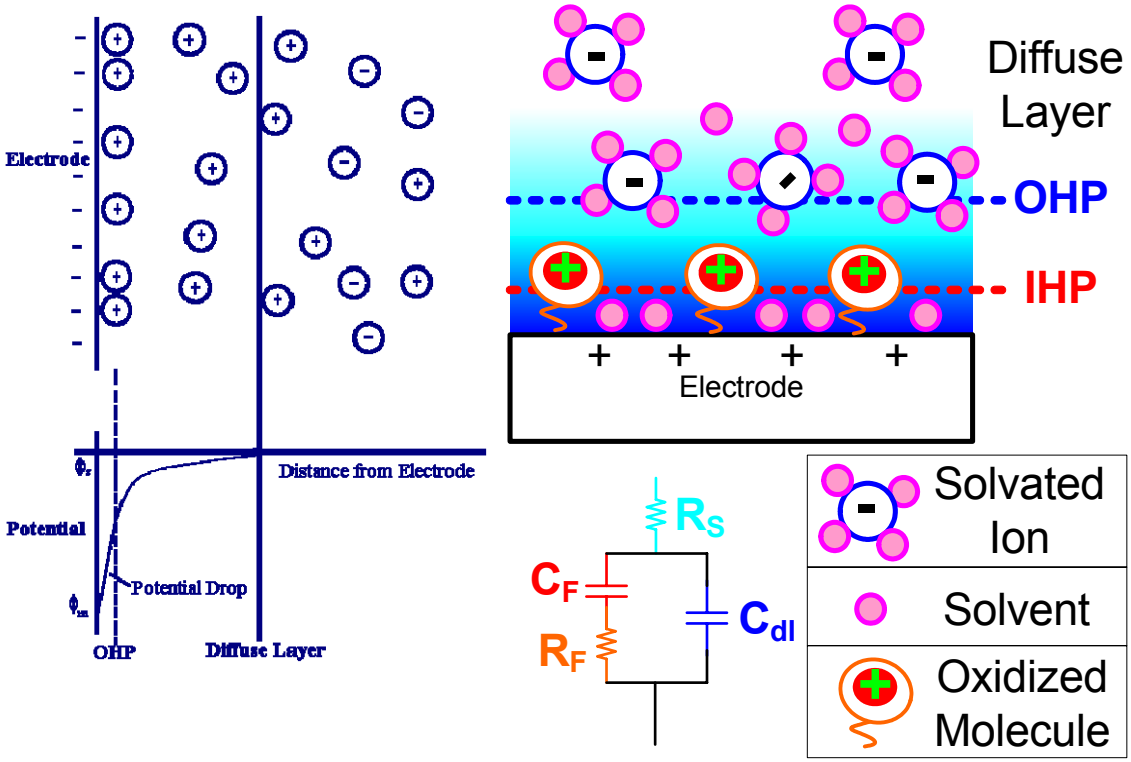


Figure 6.15 Role of Electrolyte: **(a)** Schematic showing charge and potential distribution an electrolyte-electrode interface without any molecules attached. A positive voltage is applied to the electrode with respect to the electrode bulk. The conditions depict the silver electrode contacting electrolyte in the electrolyte-gated hybrid silicon-molecular devices. OHP stands for Outer Helmholtz Plane. Most of the applied potential is dropped across the OHP-layer and electrode surface which gives to a very high field at the electrolyte-electrode interface. **(b)** Schematic showing charge distribution electrolyte-electrode interface with a monolayer of redox-active molecules attached to the electrode surface. The potential distribution is depicted by the background color gradient where darker shade of blue indicates higher electric field. A negative (oxidizing) voltage is applied to the electrode in the situation portrayed. IHP stands for Inner Helmholtz Plane.

The experiments on approaches for integration revealed that electrolyte may be an indispensable part of the hybrid silicon-molecular charge storage devices. In order to appreciate the unique properties of the electrolyte, it is essential to further look into the role of the electrolyte and intricate details of the electrolyte-molecule-electrode (Si or metal) interfaces (Fig. 6.15).

There are various models that have been proposed for electrolyte-electrode interface (without any redox-active species) [16, 17]. In the simplest model, the charge on the electrode is balanced by a layer of solvated ions (of opposite charge) held at the electrode surface by Coulombic attraction. This arrangement is often referred to as the electric double layer. When a negative potential is applied to the electrode, negative charges at the electrode surface attracts the positive charged solvated ions in the electrolyte, which diffuse towards the electrode surface. The attracted ions form a layer of positive ions close to the electrode surface, separated by the solvent molecules, which surround the charged ions. This sheet of positive ions is called the Outer Helmholtz Plane (OHP). The ions at OHP are held attracted towards the electrode surface by the Coulombic attraction and separated by solvent molecules that surround the ions. The Coulombic attraction extends beyond the OHP into next layer called diffuse layer, where there is competition between the ordering effect of the Coulombic attraction and the disordering effect of the thermal motion. Initially, any applied potential across the electrode and the electrolyte solution causes the ion migration to set up the OHP layer and hence bulk of the electrolyte away from the OHP can be modeled as a series resistor $\mathbf{R_s}$. However, once there is significant amount of positive ions at OHP, majority of the applied potential drop appears across the OHP and electrode surface as shown in Fig. 6.15 (a). In effect, the bulk of electrolyte behaves like a battery as it transfers the applied potential to OHP with minimal drop across the diffuse layer, and this can be considered as a pseudo-battery effect. The distance between OHP and electrode is determined by size of the solvent molecules and is typically only a few angstroms thick. As significant part of the applied potential is dropped across this distance (i.e., the electrical or electrolyte double layer), it gives rise to a very high field. The field is highest exactly at the electrolyte-electrolyte interface and falls exponentially moving away from the electrode surface in the electrolyte solution. In summary, the interfacial region can be viewed as two layers of opposite charges separated by a dielectric material (solvent). Hence, it is often treated as a capacitor and modeled as double layer capacitance, $\mathbf{C_{dl}}$ in the equivalent circuit. From the discussion above, it can be seen that $\mathbf{C_{dl}}$ appears in series with $\mathbf{R_s}$.

The polarity of potentials and charges discussed until now resembles that of the half-cell corresponding to the silver-electrolyte interface in the electrolyte-gated hybrid silicon-molecular devices. The polarity of the charges and potentials are reversed at the other half-cell i.e. electrode with immobilized redox-active molecules. Electrolyte double layer with

reverse polarities of charges are also formed across the redox-active molecular layer as shown in Fig 6.15 (b). When a positive potential is applied on the electrode with respect to electrolyte solutions, a very high electric field at the electrode surface causes redox-centers in the molecules to lose electrons, which tunnel across the linker into electrode. The positive-charged molecules (which define the Inner Helmholtz Plane) are screened by the negative ions in the electrolyte. This interaction can also be viewed as capacitive and modeled as faradaic capacitance, $\mathbf{C_F}$ and appears in parallel with $\mathbf{C_{dl}}$.

To summarize, the unique properties of the electrolyte which make it a daunting challenge to replace with a completely solid-state stack are:

1. **Pseudo-battery effect**: As mentioned earlier, once the electrical double layer is setup, most of the applied voltage is transferred to appear across the double layer, in which the molecules are embedded. This enables the molecules states to be accessed in a relatively narrow voltage range as the electric field at the electrolyte-electrode interface is very high. However, in case of the solid-state cell, the capacitance of the high-K dielectric layer (say AlN) appears in series to the faradaic capacitance, which results in significant portion of the applied potential dropped across the high-K layer.

2. **Embedding Molecules in Double-Layer**: In electrolyte-molecule-electrode system, the counter-ions in the electrolyte screen the redox charges in the molecular layer at very close proximity and also the charges in the metal electrode. This makes $\mathbf{C_{dl}}$ appear in parallel to $\mathbf{C_F}$ as noted earlier and allows very high charge-density in the molecular layer. It is extremely difficult to mimic this system in a completely solid-state cell where in a highly ordered molecular array has to be embedded in an ultra-thin high-K dielectric layer.

3. **High-K with High Breakdown Field**: The dielectric constant of the solvent determines the capacitive coupling between the screening charges (counter-ions) and the redox-charges in the molecular layer. The dielectric constants of the solvents typically used are as high as 60, which enable high charge density at relatively low electric fields. Also, these solvents have relatively very high breakdown field (> 50 MV/cm) as compared to solid-state dielectrics.

4. **Nearly perfect DC-block**: The double layer behaves like a nearly ideal capacitor with excellent DC-leakage characteristics. This limits the possibility of charges in the molecules to leak into electrolyte and enables good charge-retention characteristics. It is definitely a challenge (and probably impractical) to find a solid-state high-K layer that can block DC current when it is only a few angstroms thick.

It is essential to note that the electrolyte is an integral part of the molecular memory cell and the unique properties (or advantages) of the cell.

6.4 Future outlook

There are few aspects of this research work that needs to be explored further and also there is a potential for some of the findings of the work to be applied in realistic molecule-based memory devices. The following is a list of suggested experiments and explorations:

I. Molecules on other semiconductors: This work has extensive studies of behavior of redox-active molecules on Si substrates and it led to some inferences about the electronic interaction of the redox-energy states with the bands in the solids. However, to have a more comprehensive understanding of the electronic coupling between the discrete energy states in the molecules and the bands in the semiconductors, it is necessary to investigate the redox properties on other semiconductor materials. It is suggested specifically to use semiconductor materials which have band-gap energies significantly different from Si, such as SiC (wider band gap), strained SiGe (smaller band-gap) etc.

II. Diodes as access device for memory crossbar architectures (Fig. 6.16): There have several proposals for memory crossbar architectures, as they are highly efficient in terms of achieving high density memory. The proposals pertain to using conductance-switching molecules as active memory device. However, cell disturb is a major cause of concern with limits large-scale implementation of the same. One of the most prominent proposals to circumvent this problem is to use the diode as access device, which would lead increase in cell size but still has better scaling

potential as compared to using a transistor. As an extension of this concept, the diode work presented in chapter 4 can be utilized for implementation of the memory crossbar using redox-active molecules as active memory device (or storage element).

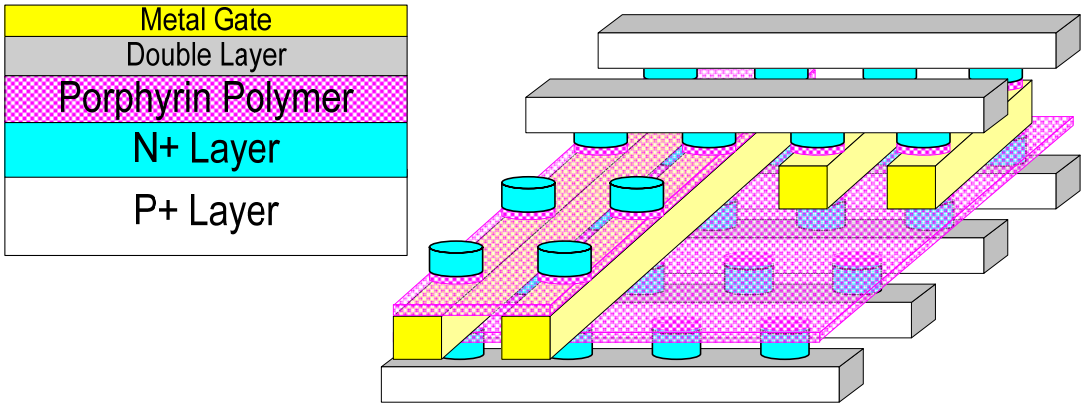


Figure 6.16 Schematic depicting the concept of diode as access device for 3D molecular memory crossbar.

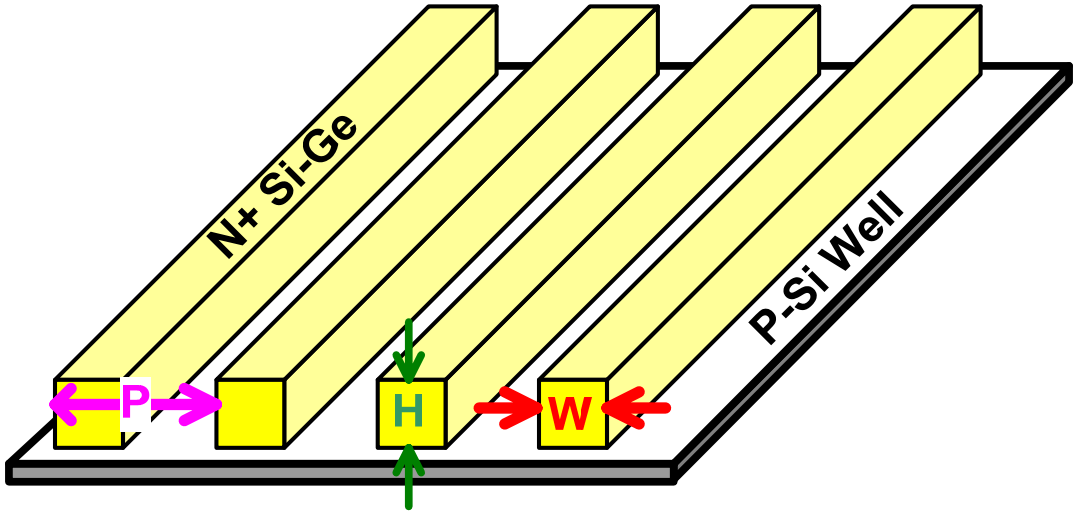


Figure 6.17 Schematic showing the proposed structure for quantitative measurement of lateral conductivity within molecular layer.

III. Quantitative lateral conductivity measurement (Fig. 6.17): As discussed in chapter 4, in order to truly quantify the intrinsic lateral conduction rate within an

assembled molecular layer, it is necessarily to reduce the dimension of the N+ pockets to that of the molecules (i.e. ~ < 5 nm). N+ doped Si nanowires on P-Si with width (W), height (H) and pitch (P) of less than 5 nm each. One of the ways to achieve this structure is by (i) epitaxial growth of N+ doped SiGe on P-Si substrate → (ii) pattern SiGe layer using photolithography and SiGe-selective dry-etch to obtain N+ doped SiGe nanowires on P-Si substrate.

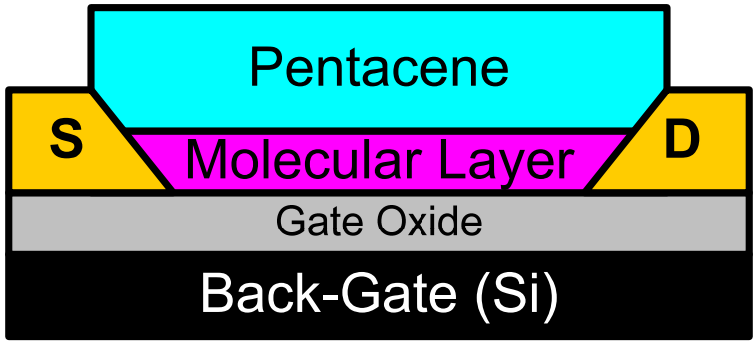


Figure 6.18 Schematic showing the cross-section of proposed molecule based organic-TFT Flash device.

IV. Non-volatile organic-TFT memory device (Fig. 6.18): Recently, there has been lot of attention drawn to non-volatile memories based on organic-Thin Film Transistor (o-TFT) for flexible-electronic Flash applications. This work demonstrated proof of concept for modulating the drain current and threshold voltage characteristics in Si FET devices by using redox-active molecules. The same can be extended for o-TFT based Flash devices since the redox-active organic molecules should be amenable for integration into organic semiconductor devices.

6.5 References

[1] T. Sakamoto, N. Banno, N. Iguchi, H. Kawaura, S. Kaeriyama, M. Mizuno, K. Terabe, T. Hasegawa, and M. Aono, "Three terminal solid-electrolyte nanometer switch," *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 475, 2005.

[2] T. Sakamoto, S. Kaeriyama, H. Sunamura, M. Mizuno, H. Kawaura, T. Hasegawa, K. Terabe, T. Nakayama, and M. Aono, "A nonvolatile programmable solid electrolyte nanometer switch," *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pp. 290, 2004.

[3] F. Q. Xie, L. Nittler, C. Obermair, and T. Schimmel, "Gate-controlled atomic quantum switch," *Physical Review Letters*, vol. 93, pp. -, 2004.

[4] C. G. Lu, Q. Fu, S. M. Huang, and J. Liu, "Polymer electrolyte-gated nanotube field-effect carbon transistor," *Nano Letters*, vol. 4, pp. 623-627, 2004.

[5] S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, and P. L. McEuen, "High performance electrolyte gated carbon nanotube transistors," *Nano Letters*, vol. 2, pp. 869-872, 2002.

[6] Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science*, vol. 302, pp. 1543-1545, 2003.

[7] J. D. Plammer, M. D. Deal, and P. G. Griffin, "Interconnects and Vias," in *Silicon VLSI Technology: Fundamentals, Practice and Modeling*. Upper Saddle River, NJ: Prentice Hall, Inc., 2000, pp. 695-707.

[8] G. Mathur, "Redox-Active Organic Molecules on Silicon and Silicon Dioxide Surfaces for Hybrid Silicon-Molecular Memory Devices," in *Electrical and Computer Engineering*. Raleigh, NC: North Carolina State University, 2005, pp. 98-104.

[9] K. Muthukumaran, L. H. Yu, I. Sazanovich, E. Hindin, C. Kirmaier, J. R. Diers, D. F. Bocian, D. Holten, and J. S. Lindsey, "Self-assembled light harvesting arrays," *Abstracts of Papers of the American Chemical Society*, vol. 226, pp. U207-U208, 2003.

[10] A. Ambroise, R. W. Wagner, P. D. Rao, J. A. Riggs, P. Hascoat, J. R. Diers, J. Seth, R. K. Lammi, D. F. Bocian, D. Holten, and J. S. Lindsey, "Design and synthesis of porphyrin-based optoelectronic gates," *Chemistry of Materials*, vol. 13, pp. 1023-1034, 2001.

[11] D. F. Watson, G. M. Hasselmann, and G. J. Meyer, "Solar Energy Conversion with Ordered, Molecular, Light Harvesting Arrays," *Proceedings of NCPV and Solar Program Review Meeting*, pp. 442-444, 2003.

[12] *International Technology Roadmap for Semiconductors 2005, Emerging Research Devices*, 2005.

[13] S. Seo, M. J. Lee, D. C. Kim, S. E. Ahn, B. H. Park, Y. S. Kim, I. K. Yoo, I. S. Byun, I. R. Hwang, S. H. Kim, J. S. Kim, J. S. Choi, J. H. Lee, S. H. Jeon, S. H. Hong, and B. H. Park, "Electrode dependence of resistance switching in polycrystalline NiO films," *Applied Physics Letters*, vol. 87, pp. -, 2005.

[14] D. Tondelier, K. Lmimouni, D. Vuillaume, C. Fery, and G. Haas, "Metal/organic/metal bistable memory devices," *Applied Physics Letters*, vol. 85, pp. 5763-5765, 2004.

[15] G. Mathur, "Redox-Active Organic Molecules on Silicon and Silicon Dioxide Surfaces for Hybrid Silicon-Molecular Memory Devices," in *Electrical and Computer Engineering*. Raleigh, NC: North Carolina State University, 2005.

[16] A. M. Bond, *Broadening Electrochemical Horizons: Principles and Illustration of Voltammetric and Related Techniques*: Oxford University Press, 2002.

[17] A. J. Bard and L. R. Faulkner, *Electrochemical Methods: Fundamentals and Applications*, 2nd ed: John Wiley & Sons, Inc., 2001.

APPENDICES

Appendix 1 MoleFlash Mask Set Documentation

Molecular Transistor Mask Set

March 2002

This document provided by

Protochips, Inc.
P.O. Box 32766, Raleigh, NC 27606

Point of Contact:
john@protochips.com

This document details the structures found on the MoleFlash mask set.

NOTE: It is important that any individual fabricating devices or characterizing devices that were fabricated using this mask set refer to the *actual layout data* to verify the information contained in this document. Please direct any questions regarding the mask set or this documentation to the Point of Contact listed on the cover.

Table of Contents

Floorplan

The floorplan of the MoleFlash mask set is shown below in Figure 1. Each die is marked with a unique number in its top left corner, as shown in Figure 2. The die numbering sequence is shown below. During processing, the wafer should be centered on the mask center as indicated by the dashed circle shown below.

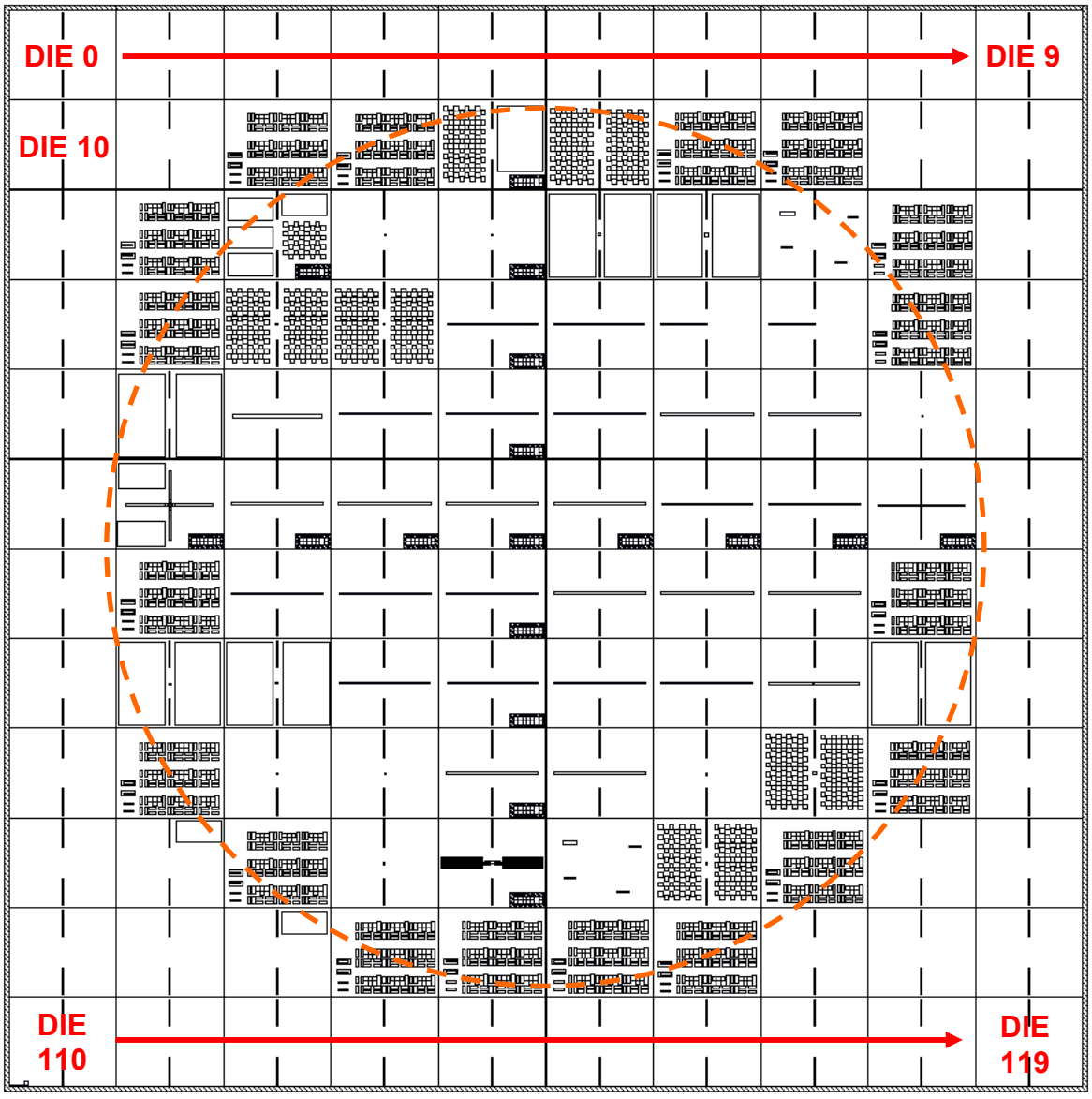


Figure 1. Floorplan of the MoleFlash mask set with die number sequence indicated

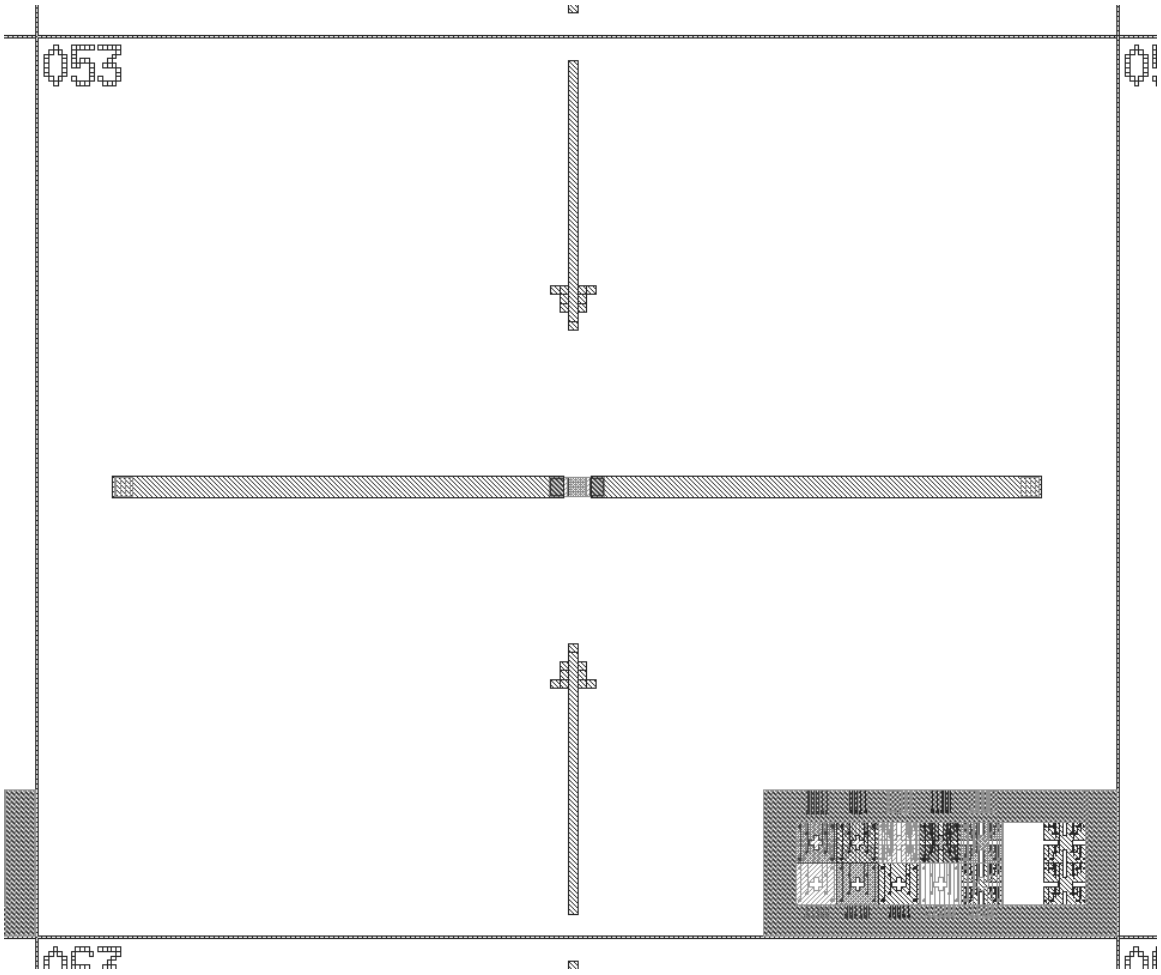


Figure 2. Typical MoleFlash Die. The MFET structure lies horizontally across the die, with the FET in the middle of the die and the S/D pads at the edge of the die. Die number is found in the upper left corner of the die. The vertical arrow features present on the metal mask enable the PDMS well to be centered over the structure while accelerating liftoff of the metal layer.

Alignment marks

Cross-style alignment marks are provided. Alignment marks are provided such that all layers can be aligned to all previous layers. Since the first process layer, “active”, is an implant layer, an initial “zero” layer is included to provide etch marks to allow alignment back to the implanted layer. Moreover, additional alignment marks are provided on the zero and metal layers to enable alignment of any future mask layers to be used with this mask set. The alignment marks are shown in Figure 3 below, while the alignment tree is shown in Figure 4.

Alignment marks are located in horizontal and vertical arrays down the center of the wafer in the x- and y-directions. The actual accuracy achieved during alignment can be measured post-process using the Vernier marks detailed in “Protochips Test Structures”

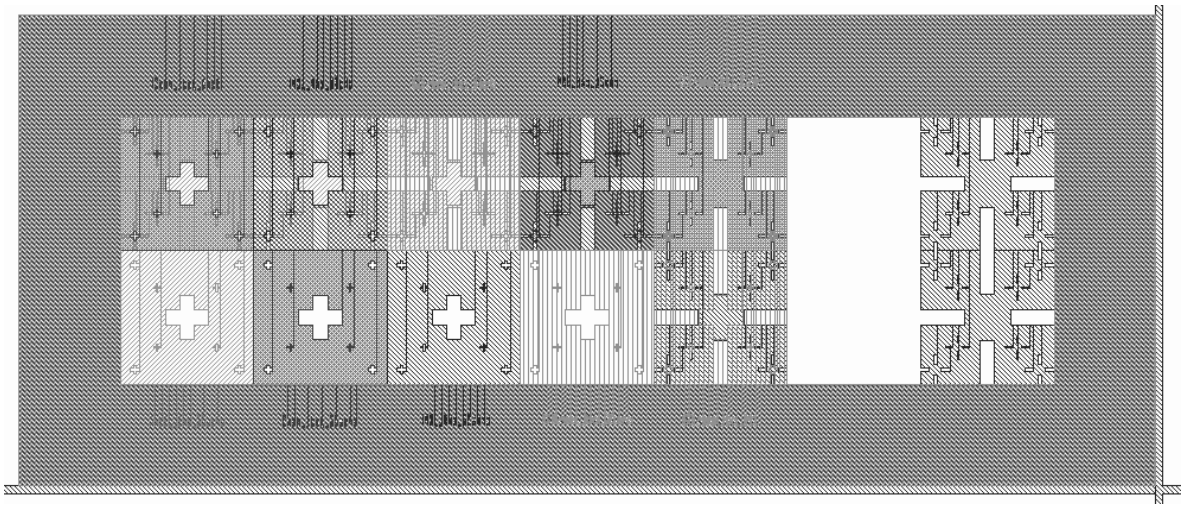


Figure 3. Alignment Marks found on the MoleFlash mask set

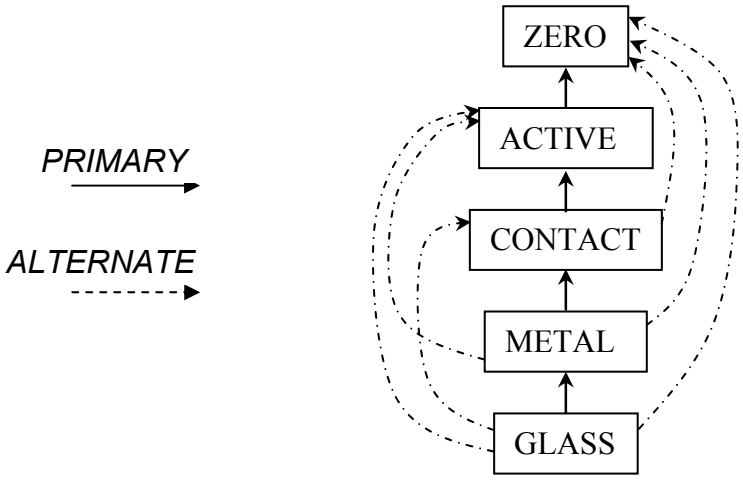


Figure 4. Alignment tree for the MoleFlash mask set.

Molecular Transistors

Transistor structures are formed as follows: The Active layer defines the area of the n+ S/D implants. The contact layer opens holes over both the gate region and the S/D regions. The metal layer is used to create interconnect from the S/D region to the pad area. The glass layer is used to open holes over the gate area (for the PDMS well) and also over the ends of the metal interconnect (thus creating pads). A typical transistor can be seen in Figure 5 below with the layers indicated. **Please see the layout for specific information.**

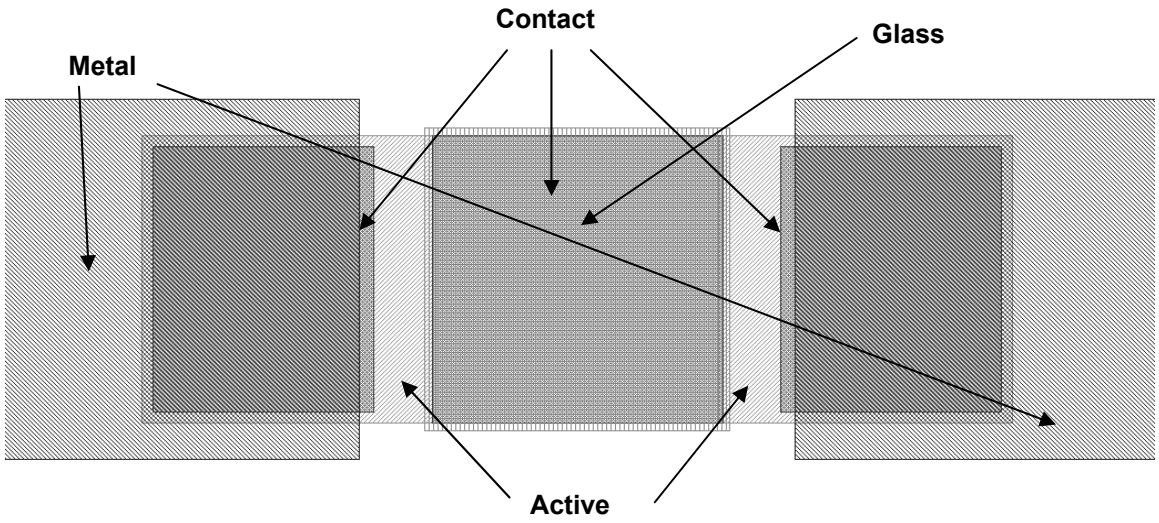


Figure 5. Typical transistor layout

Transistor structures are as follows:

MFET “200a2”
Location: Die 055
Gate area: W=L=200um
S/D overlap of gate=10um

MFET “200a”
Locations: Die 052, Die 067, Die 085
Gate area: W=L=200um
S/D overlap of gate=5um

MFET “200b2”
Location: Die 054
Gate area: W=L=200 um
S/D overlap of gate=2.5um

MFET “200b”
Location: Die 047, Die 066, Die 084
Gate area: W=L=200 um
S/D overlap of gate=0um (no overlap)

MFET “200c2”
Location: Die 053
Gate area: W=L=200 um
S/D overlap of gate= -2.5um

MFET “200c”
Location: Die 046, Die 065
Gate area: W=L=200 um
S/D overlap of gate= -5um

MFET “100a”
Location: Die 045, Die 064, Die 076
Gate area: W=L=100um
S/D overlap of gate=5um

MFET “100b”
Location: Die 044, Die 063, Die 075
Gate area: W=L=100 um
S/D overlap of gate=0um (no overlap)

MFET “100c”
Location: Die 043, Die 062
Gate area: W=L=100 um
S/D overlap of gate= -5um

MFET “50a”
Location: Die 035, Die 057, Die 074
Gate area:W=L=50um
S/D overlap of gate=5um

MFET “10a”
Location: Die 034, Die 056, Die 073
Gate area: W=L=10 um
S/D overlap of gate=2.5um

MoleFlash Capacitor Test Structures

Capacitor test structures are centered in the die for use with a PDMS well, unless otherwise noted. Several types of capacitors are available on the mask set as listed below.

Capacitors on p-substrate

P-substrate capacitors are formed using a shape of a given area on the contact layer, then opening that shape using the glass layer. The single capacitor is a single square, while the parallel capacitor uses an array of squares on the contact layer. An example of the single capacitor is shown in Figure 6.

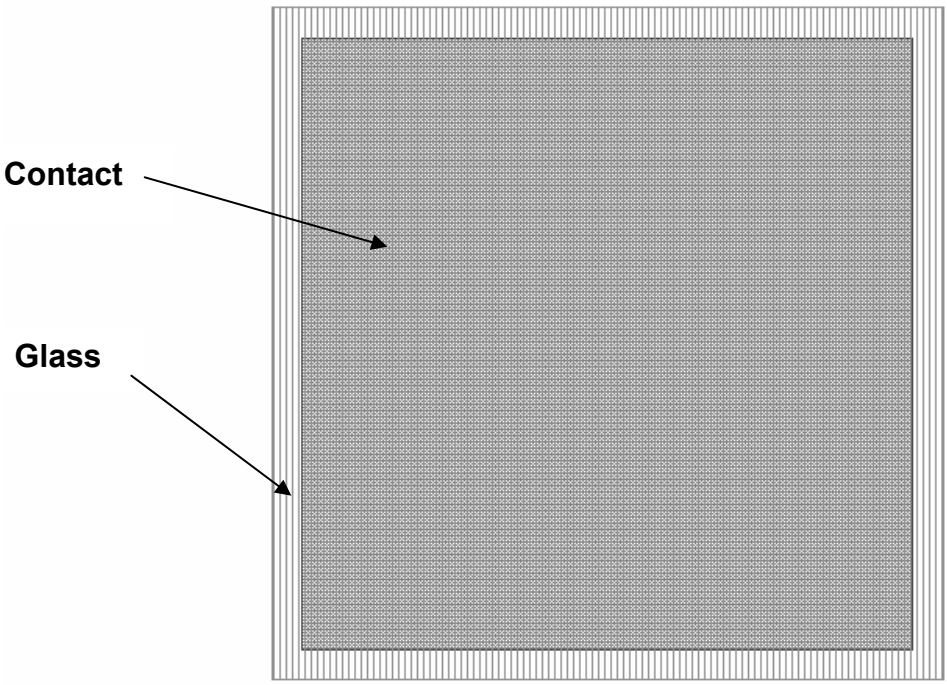


Figure 6. Single p-substrate capacitor structure with layers indicated

P-substrate capacitors are as follows:

Capacitor “CAP_single200”
Single 200um x200um
Location: Die 032, Die 072

Capacitor “CAP_single100”
Single 100um x100um
Location: Die 033, Die 082

Capacitor “CAP_single50”
Single 50um x 50um
Location: Die 023, Die 083

Capacitor “CAP_single10”
Single 10um x10um
Location: Die 024, Die 048

Capacitor “CAP_parallel100”
Parallel squares 5um x 5um (total area equal to 100x100)
Location: Die 025, Die 096

Capacitor “CAP_parallel200”
Parallel squares 10um x 10um (total area equal 200x200)
Location: Die 026, Die 087

Capacitors on N+

Capacitors on n+ are similar to caps on p-substrate, except here the capacitors are located over an active square, hence the substrate is doped n+. A contact to the n+ layer is made by extending the implant region out to a contact. The metal runs to a pad outside the extent of the PDMS well. See layout for more details.

Capacitors on N+ are as follows:

Capacitor “CAP_single100n”
Single 100um x 100um
Location: Die 036

Capacitor “CAP_single200n”
Single 200um x 200um
Location: Die 037

N+/P-sub Ratio Capacitors

Capacitors have arrays of active (n+) squares within a large p-substrate region. The ratio of n+ to p-substrate area is varied while the total area is fixed. These structures are intended to investigate the attachment to both n+ and p surfaces. The layout of a N+/P-sub capacitor is shown in Figure 7.

N+ / P-sub Ratio Capacitors are as follows:

Capacitor "CAP_np200"
Total area=40,000 um2 (200um x 200um)
N+ area= 14x14 array of 10x10um squares
Ratio of n+ / p-sub: approx. 1:1
Location: Die 086

Capacitor "CAP_ np200b"
Total area=40,000 um2 (200um x 200um)
N+ area= 13x10 array of 10x10um squares
Ratio of n+ / p-sub: approx. 1:2
Location: Die 093

Capacitor "CAP_ np200c"
Total area=40,000 um2 (200um x 200um)
N+ area= 9x9 array of 10x10um squares
Ratio of n+ / p-sub: approx. 1:4
Location: Die 071

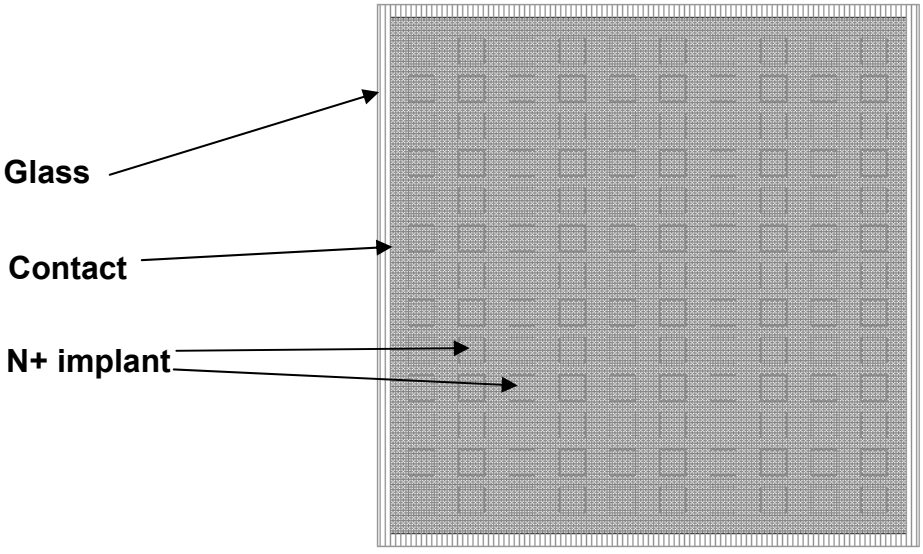


Figure 7. N+ / P-sub capacitor structure with layers

Ring Capacitors

These capacitors have a ring of metal around (but not within) the perimeter of the contact cut. The metal ring surface is then exposed during the glass cut step. These structures are NOT intended for use with a PDMS well; rather, the structures should be used with a drop of electrolyte. Single ring caps have a single ring of metal around the capacitor, while the parallel ring cap has a “mesh” of metal such that each contact cut is surrounded by metal.

Capacitor “ringCAP_single200”
Single 200um x 200um cap
Location: Die 027, Die 095

Capacitor “ringCAP_single100”
Single 100um x 100um cap
Location: Die 027, Die 095

Capacitor “ringCAP_single50”
Single 50um x 50um cap
Location: Die 027, Die 095

Capacitor “ringCAP_parallel200”
Parallel squares 10um x 10um (total area equal 200x200)
Location: Die 027, Die 095

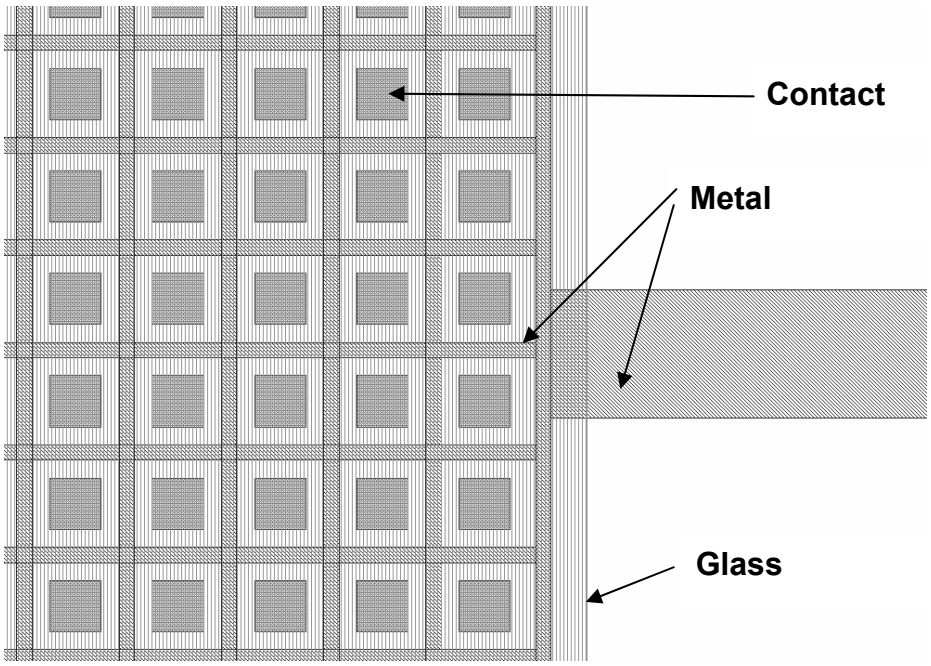


Figure 8. Ring capacitor – parallel configuration

Sheet Resistance Test Structure

The sheet resistance test structures are “Greek cross” type where current is forced between two adjacent terminals while voltage is measured on the opposite pair of terminals. Symmetry is maintained for all terminals.

Cross structure for S/D region: “Kelvin_100” (shown below)
Metal lines run from the pads down to contacts on the ends of the S/D implants.
Location: Die 051

Cross structure for the gate region: “Kelvin_200”
Metal lines run up to the glass cut and protrude 5um into the PDMS well.
Location: Die 058

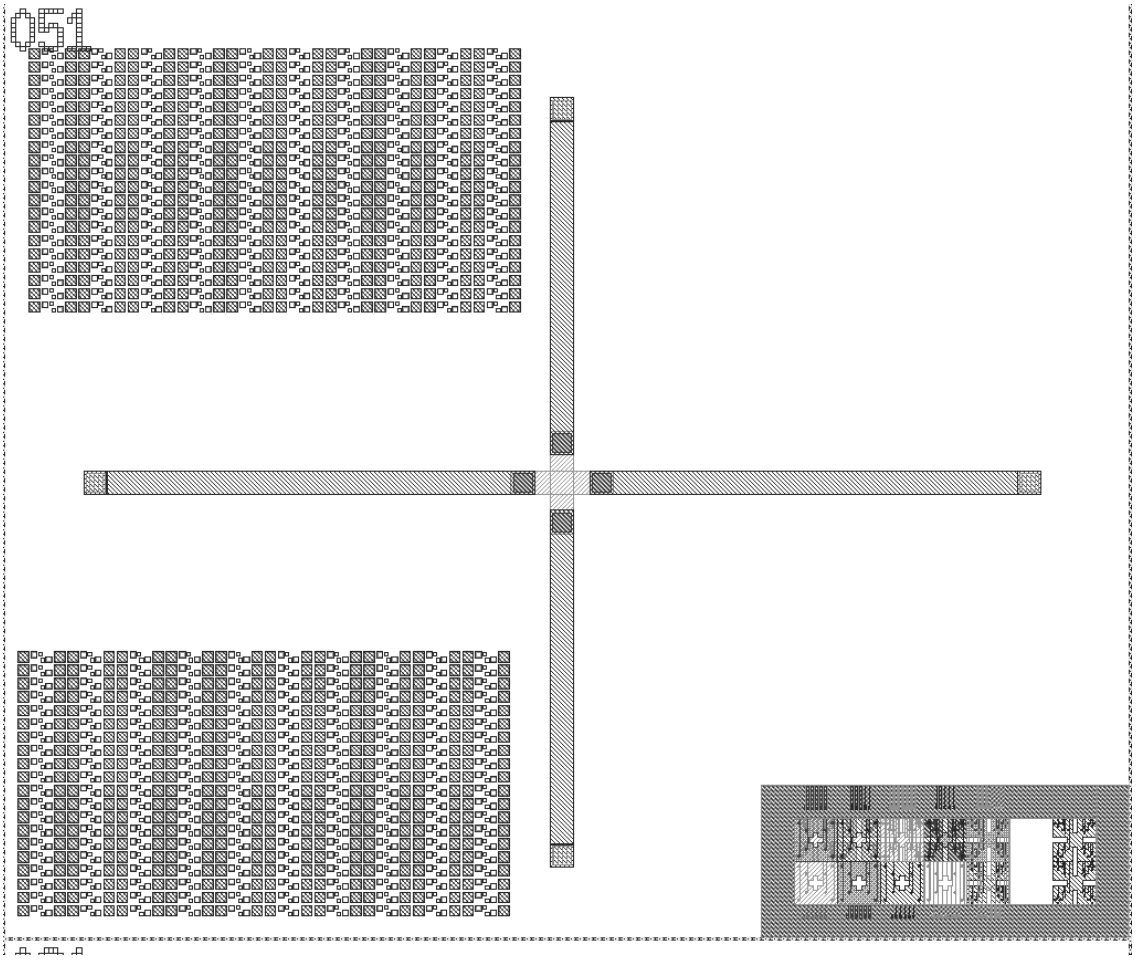


Figure 9. Cross structure for measuring sheet resistance of N+ S/D layer

DRAM Test Structures

Two structures are included with varying capacitor area (1x and 4x). Structures consist of a wide, short MFET with the source of the MFET connected to a capacitor. The capacitor is placed outside the PDMS well (near a pad) and is created with a drop of electrolyte that is independent of the well. The source pad can be used to monitor the capacitor voltage. The capacitor is charged by applying a voltage to the MFET drain while turning on the FET using the PDMS well gate. The DRAM test structure is shown in Figure 10 below - see layout for more information.

DRAM tester “DRAM_2”
Gate area: W=200 um, L=20um with 5um overlap
Capacitor: 200um x 200um
Location: Die 042

DRAM tester “DRAM_3” (shown below)
Gate area: W=200 um, L=20um with 5um overlap
Capacitor: four 200um x 200um in parallel
Location: Die 077

Figure 10. DRAM test structure with MFET and capacitor

Neuron Test Structures

Structures consist of doped source/drain regions with contact/glass cuts above the channel forming the gate (similar to MFET structures listed above). Here, however, an additional gate terminal is provided to capacitively couple charge to a neuron placed in the gate/channel region. The metal or active layer is used for the coupling. See layout for more information.

Neuron tester “neuron_array_wpads”
Four devices total, two coupling schemes with two devices each
Location: Die 094

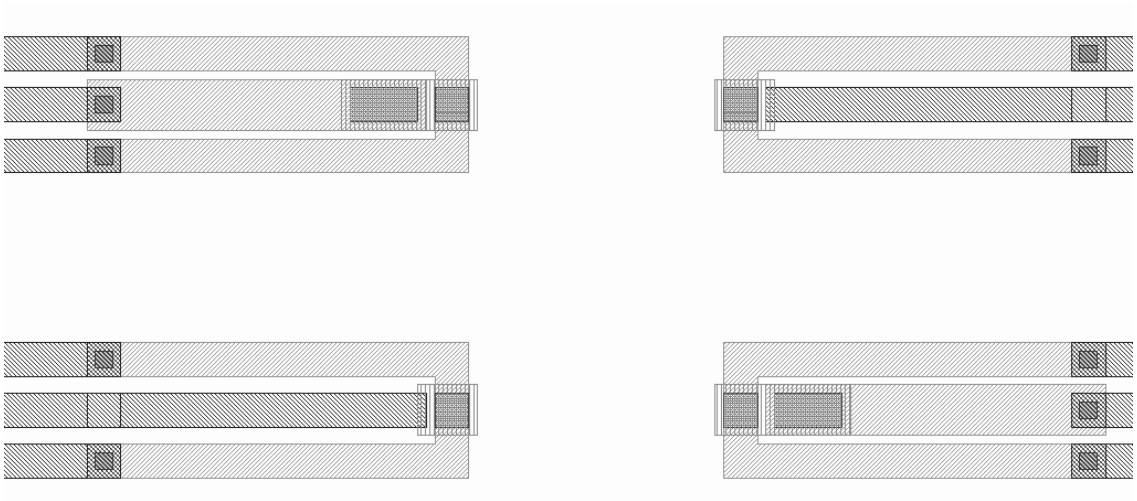


Figure 11. Neuron Test Structure

Characterization Array

The “characterization array” contains several structures useful for physical and electrical process characterization. The characterization arrays are placed in the following die: 012, 013, 016, 017, 021, 028, 031, 038, 061, 068, 081, 088, 092, 097, 103, 104, 105, and 106. Please note that many of the above die are “partial” die such that a portion of the array may occasionally fall outside the wafer surface – this is intentional. For all structures, please see the layout for more details. The top level cell name is “test_die”.

Structures included in the characterization array (see also Figure 12):

(1) *Verniers* (active/zero, active/contact, contact/metal, metal/glass) – used for determining alignment accuracy, these structures are placed in both the x- and y- direction
(2) *Profilometer squares* – large area regions used for measuring step heights from layer to layer with the profilometer
(3) *TLM structures* – used for measuring contact and sheet resistance using the transfer-length method. Metal-to-N+ and metal-to-p-sub TLM structures are included
(4) *Contact chains* – a series connection of metal-n+ and metal-psub contacts, used for verifying continuity of the contact layer but NOT specific resistance.
(5) *Lithography testers* – lines with various widths/pitchs/spaces to verify lithography on all layers

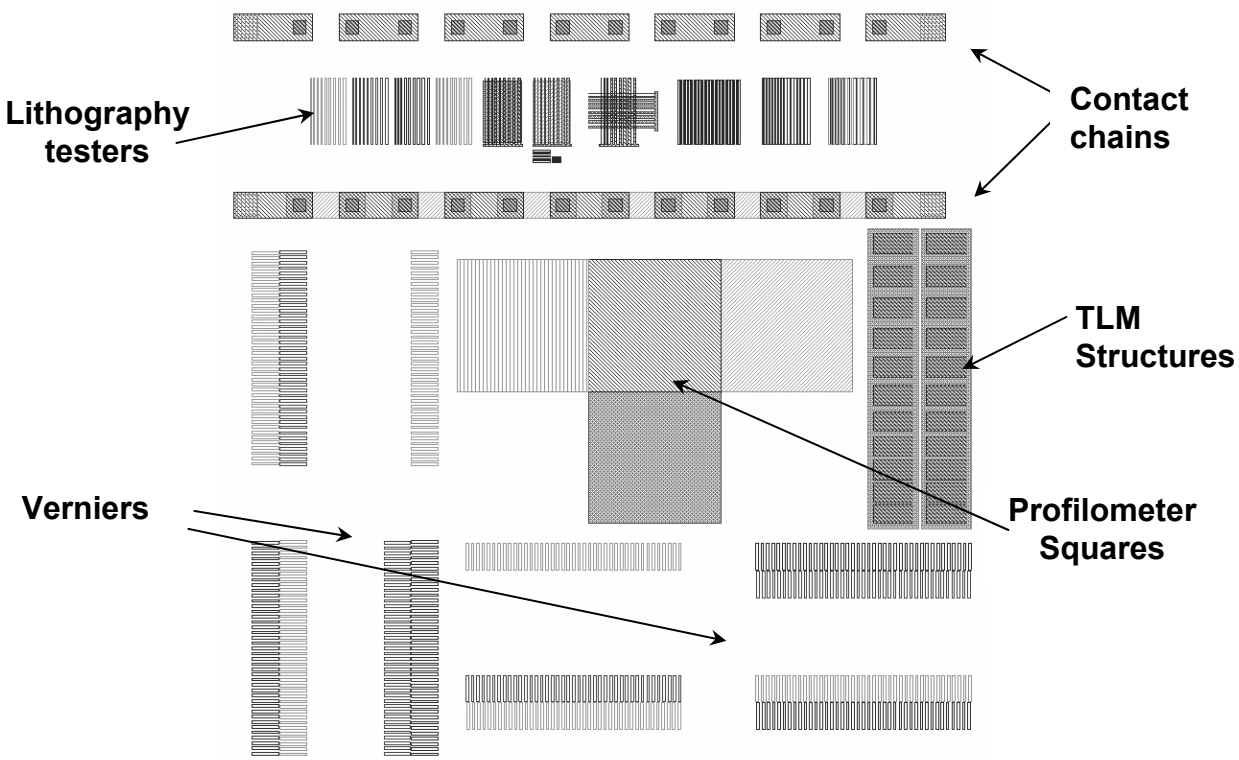


Figure 12. Characterization Array Structures

Shortflow Capacitor Structures

Shortflow capacitor structures are near the edge of the wafer. The substrate capacitors consist of a square active region fully enclosed by a metal square. The overlap of metal with active varies with the size of the capacitor. The field capacitors consist of a metal square WITHOUT the active region such that the metal square lies on the field oxide. These are designated “shortflow” capacitors since they are incompatible with the baseline MoleFlash process, thus necessitating an alternate (shortflow) process.

Shortflow capacitor structures include:

Capacitor array “CAP_veena” (Figure 13)
ALL are substrate capacitors
Structures: Active region area W=L=10um with 1um metal overlap
Active region area W=L=20um with 3um metal overlap
Active region area W=L=30um with 3um metal overlap
Active region area W=L=50um with 6um metal overlap
Active region area W=L=100um with 6um metal overlap

Capacitor array “CAP_veena2” (Figure 14)

substrate capacitor structures:

Active region area W=L=200um with 6um metal overlap
Active region area W=L=300um with 6um metal overlap
Active region area W=L=500um with 6um metal overlap

field capacitor structures:

Metal area W=L=200um
Metal area W=L=300um
Metal area W=L=500um

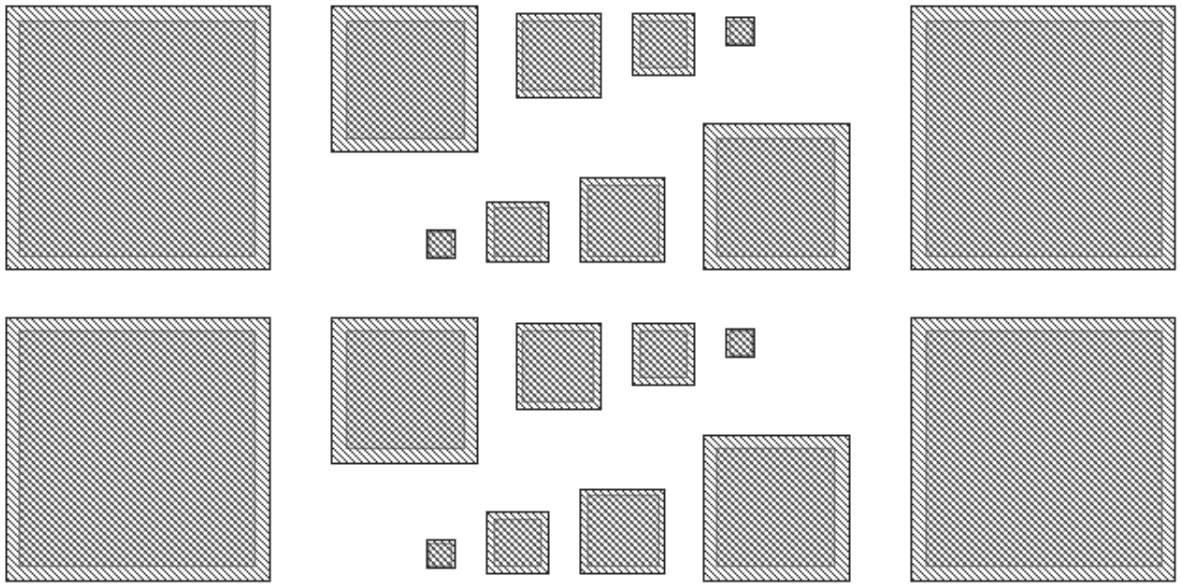


Figure 13. Shortflow Capacitors “CAP_veena”

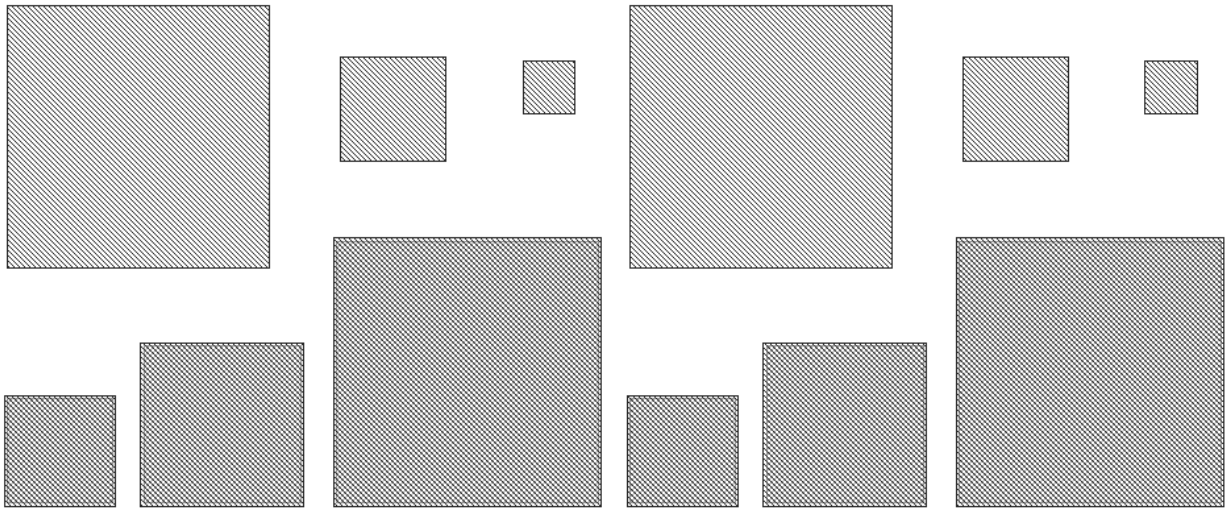


Figure 14. Shortflow Capacitors “CAP_veena2”

Appendix 2 MoleFlash Process Log

Run Name: (PMOS/NMOS LOT Date:)

Shyam Surthi, Guru Mathur, Qiliang Li and Sriv Gowda
Advisor: Dr. Veena Misra

Number of 4 inch p/n-type (_ doped) (100) wafers: _____; Resistivity: _____ ohms-cm

Monitor wafers: Resistivity: _____ ohms-cm

Lot# _____

Run specifications: 5 masks including a zero level mask.

1. Label wafers

- Wafer ID's:
- Monitor wafer ID's:
- Monitor wafer for sheet resistance ID (1):
- Measure sheet resistance: Process _____, Monitors _____ Ω-cm
- Comments: Check the wafer numbering for previous lot and continue with that numbering.
- Date: Operator:

2. JTB Baker Clean

- Wafer ID's:
- Time: 10 min
- Comments:
- Date: Operator:

3. Photolithography #1-Pre-coat bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments: Start resist coating immediately after the bake.
- Date: Operator:

4. Photolithography #1-Resist coat

- Wafer ID's:
- Resist ID: 1813 (positive resist)
- Spin speed/time:

- Amount of resist used: _____ cc
- Comments: This level is dark field
- Date: Operator:

5. Photolithography #1-Pre-exposure bake

- Wafer ID's:
- Temperature/Time: 115°C/1 min
- Comments:
- Date: Operator:

6. Photolithography #1- Expose

- Wafer ID's:
- Mask set: Moleflash (1st Mask)
- **Level Name: Zero**
- Time:
- Comments: No alignment, Zero level mask. Check the exposure time.
- Date: Operator:

7. Photolithography #1-Develop

- Wafer ID's:
- Time: 60 sec.
- Comments:
- Date: Operator:

8. Photolithography #1–Post-develop bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments:
- Date: Operator:

9. Descum

- Wafer ID's:
- System: Asher
- Program: Standard #1
- Comments: Inspect the wafers!!!
- Date: Operator:

10. Wet Etch Zero Layer Si (Use Poly Etch)

- Wafer ID's:
- Monitor Wafer ID (1):
- **Poly etch followed by rinse & dry**
- Time:
- Thickness etched: ~1500Å (desired), Actual: _____ Å
- Comments: Need monitor wafer!!! MUST do step height measurement on monitor wafer before etching the process wafers.
- Date: Operator:

11. Strip resist and inspect

- Wafer ID's:
- Solution: Nanostrip
- Time: 10 min each bath
- Comments:
- Date: Operator:

12. JTB Baker Clean

- Wafer ID's:
- Time: 10 min
- Comments:
- Date: Operator:

13. Grow (diffusion mask) oxide -100 nm

- Wafer ID's:
- Monitor Wafer ID (1):
- Furnace: D1
- Temperature/Time: 1000 C/20 min (Check!)
- Ambient:
- Measure Thickness:
- Comments: Need 1 monitor wafer!!!
- Date: Operator:

14. JTB Baker Clean

- Wafer ID's:
- Time: 10 min
- Comments:
- Date: Operator:

15. Photolithography #2A-Pre-coat bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments: Comments: Start resist coating immediately after the bake.
- Date: Operator:

16. Photolithography #2A-Resist coat backside

- Wafer ID's:
- Resist ID: 1813 (positive resist)
- Spin speed/time:
- Amount of resist used: _____ cc
- Comments: Coating the back side of the wafer
- Date: Operator:

17. Photolithography #2A-Pre-exposure bake

- Wafer ID's:
- Temperature/Time: 115°C/1 min
- Comments: Heat the wafers with front side down
- Date: Operator:

==========➔ Develop? Rinse & spin dry?➔==========

18. Photolithography #2-Resist coat front side

- Wafer ID's:
- Resist ID: 1813 (positive resist)
- Spin speed/time:
- Amount of resist used: _____ cc
- Comments: This level is dark field, now coating the front side
- Date: Operator:

19. Photolithography #2-Pre-exposure bake

- Wafer ID's:
- Temperature/Time: 115°C/1 min
- Comments: Heat the wafers with back side down
- Date: Operator:

20. Photolithography #2-Align and expose

- Wafer ID's:
- Mask set: Moleflash (2^{nd} Mask)
- **Level Name: Active____ 1^{st} Alignment**
- Time:
- Comments: Check the exposure time.
- Date: Operator:

21. Photolithography #2-Develop

- Wafer ID's:
- Time: 60 sec.
- Comments:
- Date: Operator:

22. Photolithography #2–Post-develop bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments:
- Date: Operator:

23. Descum

- Wafer ID's:
- System: Asher
- Program: Standard #1
- Comments: Inspect the wafers!!!
- Date: Operator:

24. Wet etch oxide (BOE)

- Wafer ID's:
- Monitor wafer ID (Monitor from step # 13):
- Thickness from oxidation (Step #13):
- Time:
- Comments: After etch, measure the oxide thickness. Should be < 1-2 nm.
- Date: Operator:

25. Strip resist and inspect

- Wafer ID's:
- Solution: Nanostrip
- Time: 10 min each bath
- Comments:
- Date: Operator:

26. JTB Baker Clean

- Wafer ID's:
- Time: 10 min
- Comments: The wafers should go to diffusion immediately after the clean.
- Date: Operator:

27. NMOS: Diffusion of junctions (Phosphorous), PMOS: Send wafers for Implant

- Wafer ID's:
- Monitor Wafer ID (2):
- Standard Recipe (P): 900 C/30 min
- Junction depth estimate:
- Lateral diffusion estimate:
- Sheet resistance: _____
- Glass thickness: _____
- Comments: Need monitor wafers!!! Measure sheet resistance and glassy layer thickness for monitors. **WAFER LOADING**: Back-to-back, front of each wafer facing P disk source (P-Si-Si-P-Si-Si-P).
- Date: Operator:

28. NMOS-only: P-Deglaze (Etch glassy layer), PMOS: Skip this step

- Wafer ID's:
- Glassy layer thickness from diffusion (Step #26):
- Time:
- Comments: Overetch the glassy layer to avoid P contamination in BOE.
- Date: Operator:

29. Wet etch oxide (BOE)

- Wafer ID's:
- Monitor wafer ID (Monitor from step # 13):
- Thickness from oxidation (Step #13):
- Time: Should be same as Step #23 BOE
- Comments: Etch the oxide on both sides.
- Date: Operator:

30. JTB Baker Clean

- Wafer ID's:
- Time: 10 min
- Comments:
- Date: Operator:

31. Grow field oxide (100 nm)

- Wafer ID's:
- Monitor Wafer ID's (2): one from step #26 (_____), _____
- Furnace: D4 (not D1)
- Temperature/Time:
- Ambient:
- Measure Thickness:
  - Blank monitor: _____; Diffusion Monitor: _____
- Comments: **MUST have one monitor wafer from the P-diffusion step as oxidation monitor wafer.** The oxide growth rates are vastly different on p and n^{++} regions.
- Date: Operator:

==========→ BANK SOME WAFERS?? ←==========

32. JTB Baker Clean

- Wafer ID's:
- Time: 10 min
- Comments:
- Date: Operator:

33. Photolithography #3-Pre-coat bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments: Comments: Start resist coating immediately after the bake.
- Date: Operator:

34. Photolithography #3-Resist coat

- Wafer ID's:
- Resist ID: 1813 (positive resist)
- Spin speed/time:
- Amount of resist used: _____ cc
- Comments: This level is dark field
- Date: Operator:

35. Photolithography #3-Pre-exposure bake

- Wafer ID's:
- Temperature/Time: 115°C/1 min
- Comments:
- Date: Operator:

36. Photolithography #3-Align and expose

- Wafer ID's:
- Mask set: Moleflash (3rd Mask)
- **Level Name: Contact____ 2nd Alignment**
- Time:
- Comments: Check the exposure time.
- Date: Operator:

37. Photolithography#3-Develop

- Wafer ID's:
- Time: 60 sec.
- Comments:
- Date: Operator:

38. Photolithography #3-Post-develop bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments:
- Date: Operator:

39. Descum

- Wafer ID's:
- System: Asher
- Program: Standard #1
- Comments: Inspect the wafers!!!
- Date: Operator:

40. Wet etch majority of oxide (BOE)

- Wafer ID's:
- Monitor wafer ID (1 from step #30):
- Starting thickness from oxidation step (BLANK monitor): _____
- Time: _____
- Thickness left (BLANK monitor): _____
- **Comments**: Etching oxide on the gate. Leave behind at least 10-15 nm oxide on gate!!! In this step, use the thickness of **BLANK monitor** from step #30.

- Time: Same as that for BLANK monitor _____
- Starting thickness from oxidation step (DIFFUSION monitor): _____
- Thickness left (DIFFUSION monitor): _____
- **Comments**: **MUST** etch the DIFFUSION monitor wafer for same time and measure the thickness remaining. Break the monitor(s) into 2-4 pieces!!!
- Date: Operator:

41. Strip resist and inspect

- Wafer ID's:
- Solution: Nanostrip
- Time: 10 min each bath
- Comments:
- Date: Operator:

42. JTB Baker Clean

- Wafer ID's:
- Time: 10 min
- Comments:
- Date: Operator:

==========→ BANK SOME WAFERS?? ←==========

43. Photolithography #4-Pre-coat bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments: Comments: Start resist coating immediately after the bake.
- Date: Operator:

44. Photolithography #4- Resist coat

- Wafer ID's:
- Resist ID: Shipley 1813 (positive resist)
- Spin speed/time:
- Amount of resist used: _____ cc
- Comments: No HMDS on this spin!!!!
- Date: Operator:

45. Photolithography #4 - Pre-exposure bake

- Wafer ID's:
- Temperature/Time: 115°C/1 min
- Comments:
- Date: Operator:

46. Photolithography #4- Align and expose

- Wafer ID's:
- Mask set: Moleflash (4th Mask)
- **Level Name: Metal 1____ 3rd Alignment**
- Time:
- Comments: Check the exposure time.
- Date: Operator:

47. Photolithography #4-Develop

- Wafer ID's:
- Time: 60 sec.
- Comments:
- Date: Operator:

48. Photolithography #4-Post-develop bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments:
- Date: Operator:

49. Descum

- Wafer ID's:
- System: Asher
- Program: Liftoff #5
- Comments:
- Date: Operator:

==========➔ BANK SOME WAFERS?? ➔==========

50. Back door etch

- Wafer ID's:
- Solution: 1% HF
- Time: 5 min
- Comments: Evaporate metals immediately after the backdoor etch!
- Date: Operator:

51. Sputter metal - W (100 nm)

- Wafer ID's:
- System:
- Temperature/Time: Pressure:
- Comments:
- Date: Operator:

52. Lift-off Metals

- Wafer ID's:
- Solution: Microchem 1165 Lift-off Tank
- Time:
- Comments: Use ultarsonicator with 1165 remover solution after soaking the wafers for 1-2 hours.
- Date: Operator:

==========➔ **NITRIDE** or **LTO**?? ➔==========

53. LPCVD Si_3N_4 -100 nm or LTO 400 nm

- Wafer ID's:
- Monitor Wafer ID's (2):
- Temperature/Time:
- Ambient:
- Pressure:
- Comments: Need 2 monitor wafers!!!
- Comments: **LTO Wafer loading: Back-to back**!!!
- Date: Operator:

54. Photolithography #5-Pre-coat bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments: Comments: Start resist coating immediately after the bake.
- Date: Operator:
-

55. Photolithography #5-Resist coat

- Wafer ID's:
- Resist ID: 1813 (positive resist)
- Spin speed/time:
- Amount of resist used: _____ cc
- Comments:
- Date: Operator:

56. Photolithography #5-Pre-exposure bake

- Wafer ID's:
- Temperature/Time: 115°C/1 min
- Comments:
- Date: Operator:

57. Photolithography #5-Align and expose

- Wafer ID's:
- Mask set: Moleflash (5^{th} Mask)
- **Level Name: Glass ____ 4^{th} Alignment**
- Time:
- Comments:
- Date: Operator:

58. Photolithography #5-Develop

- Wafer ID's:
- Time: 60 sec.
- Comments:
- Date: Operator:

59. Photolithography #5–Post-develop bake

- Wafer ID's:
- Temperature/Time: 115°C/5 min
- Comments:
- Date: Operator:

60. Nitride Etch or LTO Etch

- Wafer ID's:
- Monitor wafer ID (1 from step 46):
- Time:
- Solution:
- Comments:
- Date: Operator:

61. Strip resist and inspect

- Wafer ID's:
- Solution: 1165 Remover
- Time: 10 min each bath
- Comments:
- Date: Operator:

End of Process Flow (if no backside metal contact)

****

Process Flow for Backside Metal Contact (if needed)

* Note: Starred steps are not necessary if nitride wet etch is performed right before Al evaporation. If not, then they are necessary to remove native oxide from sitting around.

62. Front Side Resist Coat*

- Wafer ID's:
- Resist ID: Shipley 1813
- Date: Operator:

63. Front side Resist bake*

- Wafer ID's:
- Temperature/Time: 115°C/ 5 min
- Date: Operator:

64. Etch backside in BHF until clear*

- Wafer ID's:
- Solution: 10% HF
- Date: Operator:

65. Evaporate Al backside- Al (0.1-0.5 μm)

- Wafer ID's:
- System:
- Temperature/Time:
- Pressure:
- Date: Operator:

66. Strip front side resist and inspect*

- Wafer ID's:
- Solution: Accustrip
- Time: 10 min
- Date: Operator:

Appendix 3 IEDM 2004 MoleFET Paper

Modulation of drain current by redox-active molecules incorporated in Si MOSFETs

Srivardhan Gowda, Guru Mathur, Qiliang Li, Shyam Surthi, Qian Zhao, Jonathan S. Lindsey*, David F. Bocian†, and Veena Misra.

Dept. of Electrical & Computer Engineering, North Carolina State University, Raleigh, NC, USA

*Dept. of Chemistry, North Carolina State University, Raleigh, NC, USA

†Dept. of Chemistry, University of California, Riverside, CA, USA

This paper appears in: Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International

Publication Date: 13-15 Dec. 2004

On page(s): 707 - 710

Modulation of Drain Current by Redox-Active Molecules Incorporated in Si MOSFETs

Srivardhan Gowda, Guru Mathur, Qiliang Li, Shyam Surthi, Qian Zhao, Jonathan S. Lindsey*, David F. Bocian†, and Veena Misra

Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695 USA
** Department of Chemistry, North Carolina State University, Raleigh, North Carolina 27695 USA*
† Department of Chemistry, University of California, Riverside, CA 92521 USA
Tel 919-515-7356 Fax 919-515-5055 email: vmisra@ncsu.edu

Abstract

Redox-active molecular monolayers were incorporated in MOSFETs to modulate the device characteristics. The discrete molecular states were manifested in the drain current characteristics indicating the presence of distinct energy levels at room temperature.

Introduction

Hybrid silicon/molecular technology involving incorporation of molecules onto silicon devices may be instrumental in augmenting today's CMOS only technologies [1-3]. The advantages of molecular-based memory devices include nanoscale size, low voltage operation and multiple-state properties. Multiple-state behavior can be built into the molecular structure via molecular design and chemical synthesis. For example, the porphyrin molecule exhibits three discrete states: neutral, monopositive, and dipositive. More elaborate molecular structures have been devised that afford up to seven positively charged states [4]. When coupled with CMOS devices, these discrete states can enable single electron functionality in logic and memory devices. *In this work, we report for the first time, the modulation of drain current by redox-active monolayers attached to MOS transistors. The presence of the redox states of the molecule are observed in the drain current characteristics, which confirm the existence of discrete energy states within the molecules. These molecular states can be utilized for low-voltage, multiple-state memory and logic applications and can extend the impact of silicon-based technologies.*

Experimental

Capacitor structures (Fig. 1a) were fabricated by forming self-assembled monolayers (SAMs) of molecules on varying thicknesses of SiO_2 on n and p-Si substrates. The redox-active molecule used in this study was *ferrocenyl phosphonate* (Fc-P, Fig. 1b). The ferrocene unit exhibits two states: neutral and cationic redox state (becomes positively charged after oxidation). For control experiments, the non-redox-active molecule *biphenyl phosphonate* (Bz-P) was used (Fig. 1c). The MOSFETs used in the experiments were fabricated using a 5 level mask process based on replacement gate technology. PMOSFETs of varying gate lengths from 10 to 100 μm with 2.5 to 5 μm source-drain overlap regions and gate width being equal to the gate length were fabricated. Gate oxide of varying thicknesses was grown by thermal oxidation. The molecules selected for this work have shown excellent stability (up to 400°C), excellent endurance, high densities and low redox voltages [4,5]. The solution used to form SAMs on silicon oxide was prepared by dissolving 1 mg of these compounds in 200 μl of dimethyl formamide. The sample was maintained at 90 ºC during the attachment procedure in an argon-purged environment [6]. The electrical analyses were performed using a CHI 600 electrochemical analyzer and an HP 4155B semiconductor parameter analyzer.

Results and Discussion

Figs. 2(a) and 2(b) show the forward and reverse scans of cyclic voltammetry (CyV) of redox-active molecules (Fc-P) attached to varying oxide thicknesses on p- and n-Si substrates, respectively. The negative and positive current peaks observed are associated with the oxidation and reduction of the molecules, respectively. Application of oxidizing gate potential causes each molecule to lose an electron to the Si substrate resulting in a positively charged monolayer. This corresponds to the written state. When a reducing voltage is applied, electrons tunnel from Si through the oxide barrier onto the molecules to return the monolayer to neutral state (erase state). Typical charge densities obtained from the area under the CyV peaks are $\sim 10^{14}$ charges/cm^2. The oxidation and reduction peak potentials separate further as the oxide thickness is increased owing to the increase in the tunneling barrier [7]. Increasing the measurement scan rate also results in a larger peak separation (Fig. 3a). As will be discussed, the increase in tunnel barrier results in longer retention times (Fig. 3b) at the cost of slightly higher oxidation and reduction potentials[8]. Fig. 4 shows the schematic of a hybrid silicon/molecular PMOSFET and illustrates the multiple paths (I_{GD}, I_{GC}) via which the molecules can become oxidized and reduced. The existence of dual redox paths for N pockets embedded in P-well has been previously reported [1] and is attributed to negligible lateral conductivity of these SAMs. Fig. 5a shows the gate to drain CyV currents for an Fc-P SAM of a PMOSFET with 1.6 nm gate oxide. The two observed peaks correspond to oxidation occurring in the overlap region (I_{GD}) between gate

and drain (lower V) and that occurring in the channel once inversion is reached via I_{GC} (higher V). The channel peak position is shifted to higher potentials due to the requirement of $V_G > V_T$[1]. The overlap and channel oxidation peaks can also be observed in the gate-substrate current (Fig. 5b). The higher potentials are again associated with the channel peaks due to the gate voltage required to invert the channel.

Fig. 6 displays the transistor characteristics (I_D-V_D) of an electrolyte-gated PMOS device with only a native oxide on channel. As shown, the ultra thin double layer (~10Å) that forms due to the electrolyte provides an excellent tunnel barrier and maintains a high I_D/I_G ratio allowing the transistor to easily turn on. Fig. 7 shows the I_D-V_G behavior of a PMOSFET with Fc-P molecules attached to a 2.8 nm gate oxide. As V_G is increased, oxidation of the molecules occurs during the forward scan, and reduction occurs during the reverse scan. As shown in Fig. 7, redox peaks are observed in the sub-threshold region of this device and are attributed to molecules on overlap region since the channel is not yet inverted. This is further supported by the swap in the oxidation and reduction currents due to gate-drain current being in opposite direction to the channel drain current. Fig. 8a shows I_D-V_D behavior in the sub-threshold region. In this measurement, the molecules are initially oxidized (since V_G is higher than V_D) and become reduced as V_{DS} is increased. Distinct peaks in the drain current are observed owing to reduction of molecules in the overlap region (I_{GD}). Since this is a transient effect and the molecules in the overlap region do not affect the channel potential, the I_D recovers to its original value once the molecules are reduced. However, when $V_G > V_T$, the channel molecules are also oxidized creating a layer of positive charges that will increase the V_T. Now, as V_{DS} is increased, these channel molecules are reduced and the V_T is decreased back to its original value. This effect can be observed in Fig. 8b, where the drain current, after reduction peaks, does not recover to its pre-reduction value (Fig. 8b). As expected, the change in drain current (DI_D) has a linear relationship with gate voltage (V_G) owing to a constant decrease in V_T associated with the reduction of molecules (Fig. 8c).

To further study the modulation of V_T and hysteresis, I_D-V_G characteristics were measured on a PMOSFET with <1.0 nm gate oxide. As shown in Fig. 9a, hysteresis was observed in the MOSFET containing the redox molecules whereas no hysteresis was observed on MOSFETs either i) without molecules or ii) with non-redox molecules. As the gate voltage is increased, the molecules become oxidized and positively charged resulting in an increase of V_T. During the return scan, many of these molecules still remain in the oxidized state causing a lower drain current. The amount of hysteresis also depends on the extent of oxidation (Fig. 9c). However, significant reduction of the molecules is expected to occur even during the return scan, given that the separation between oxidation and reduction peaks is not large for oxide <1 nm. This results in a lower value of hysteresis than expected from the number of molecules/charges present. An increase in the scan rate increases the amount of hysteresis (Fig. 9b). The hysteresis can be further increased by a slightly thicker oxide (Fig. 10a). Increasing the thickness from <1 nm to 1.3 nm creates a larger window between oxidation and reduction and consequently improves the hysteresis even at low scan rates (Fig. 10b). Fig. 11 illustrates the memory effect of the redox state with increased oxide barrier thickness indicating the improved retention properties. In summary, this work has provided the proof of concept for using redox-active molecules in MOS transistors. Information can be stored in the discrete states of molecules with multiple states which can provide quantized threshold voltage shifts.

Conclusions

Hybrid silicon/molecular FETs were fabricated by incorporating redox-active molecules in PMOSFETs. The presence of discrete charge states of the molecules was manifested in the threshold voltage, I_D and hysteresis characteristics. Multi-bit nanoFLASH devices, with low voltage operation, can be realized by using such multiple charge-state molecules.

Acknowledgements

This work is supported by DARPA Moletronics Program No. MDA972-01-C-0072 and Zettacore Inc. We would also like to thank Protochips Inc., for mask design and layout of the test structures.

References

1. S. Gowda, G. Mathur, Q. Li, D. F. Bocian, J. S. Lindsey, V. Misra et al., "Hybrid silicon/molecular memories: co-engineering for novel functionality," *IEDM'03 Tech. Dig*., pp. 537-540, 2003.
2. K. M. Roth, A. A. Yasseri, Z. M. Liu, J. S. Lindsey, W. G. Kuhr, D. F. Bocian et. al., "Measurements of electron-transfer rates of charge-storage molecular monolayers on Si(100). Toward hybrid molecular/semiconductor information storage devices," *J. Amer. Chem. Soc.*, vol. 125, pp. 505-517, 2003.
3. C. P. Collier, E. W. Wong, M. Belohradsky, J. F. Stoddart, R. S. Williams, and J. R. Heath, "Electronically configurable molecular-based logic gates," *Science*, vol. 285, pp. 391-394, 1999.
4. D. Gryko, J. Z. Li, J. R. Diers, D. F. Bocian, W. G. Kuhr, and J. S. Lindsey, "Studies related to the design and synthesis of a molecular octal counter," *J. Org. Chem.*, vol. 69, pp. 1435-1443, 2004.
5. Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science,* vol. 302, pp. 1543-1545, 2003.
6. Q.Li, S. Surthi, G. Mathur, S. Gowda, V. Misra, J. S. Lindsey et. al., "Electrical characterization of redox-active monolayers on SiO_2 for memory applications," *Appl.Phys.Lett*., vol. 83, pp. 198-200, 2003.
7. G Mathur, S. Gowda, Q. Li, S. Surthi, J. S. Lindsey and V. Misra, "Hybrid CMOS/molecular memories using redox-active self-assembled monolayers," *Proc. IEEE-Nano*, pp. 307-310, 2003.
8. G. Mathur, S. Gowda, Q. Li, S. Surthi, J. S. Lindsey and V. Misra, "Properties of functionalized redox-active monolayers on thin silicon oxide: a study of the dependence of the retention time on the oxide thickness," *IEEE Trans. Nanotech* , in press.

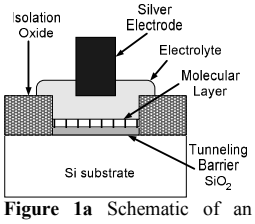


Figure 1a Schematic of an Electrolyte-Molecule-Oxide-Silicon (EMOS) capacitor, with self-assembled monolayer of Fc-P attached on the SiO_2 surface. Gate electrolyte is contacted by Ag electrode.

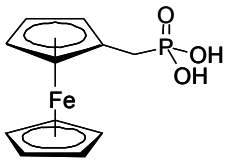


Figure 1b Chemical structure of Fc-P molecule. This molecule exhibits two states (neutral and monopositive).

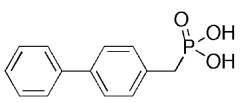


Figure 1c Chemical structure of Bz-P molecule. This molecule is NOT redox active and was used in control experiments.

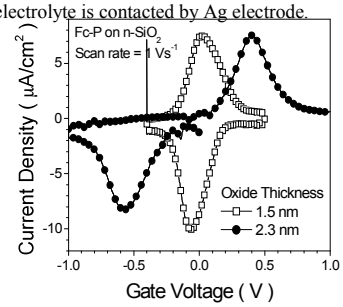


Figure 2b CyV of EMOS capacitors with Fc-P on oxide on n-Si, with two different oxide thicknesses (1.5 and 2.3 nm). Scan rate is 1 V/s. The peak separation increases with increasing t_{ox}, as with p-Si.

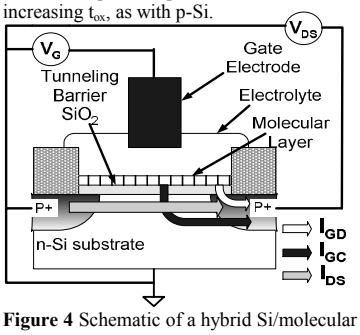


Figure 4 Schematic of a hybrid Si/molecular PMOSFET with a self-assembled monolayer of Fc-P attached on the gate oxide. Gate electrolyte is contacted by Ag electrode. The block arrows show the different currents. I_{GC} and I_{GD} represent redox parths for molecules on the channel and the overlap regions, respectively. I_{DS} represents drain current.

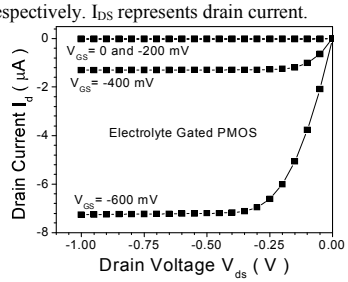


Figure 6 Transistor characteristics (I_D-V_D) of an electrolyte-gated PMOS (no molecules) with native oxide on the gate. The applied gate voltage causes migration of ions in the electrolyte resulting in the formation of a double layer at the electrolyte-native oxide interface, which causes inversion in the channel.

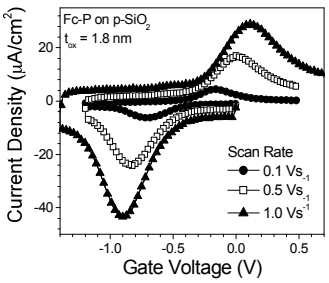


Figure 3a CyV of EMOS capacitors with Fc-P on 1.8 nm oxide on p-Si, showing the effect of scan rate on peak separation.

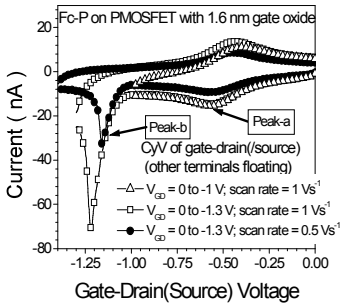


Figure 5a CyV of gate-drain (or source) of a hybrid PMOS with Fc-P on the gate oxide. The other terminals are floating. The two oxidation peaks correspond to molecules on the overlap (peak-a, p+) and the channel (peak-b, n/p+) regions, with the latter occurring at a more negative potential. The reduction peak of molecules on the channel is subdued [1].

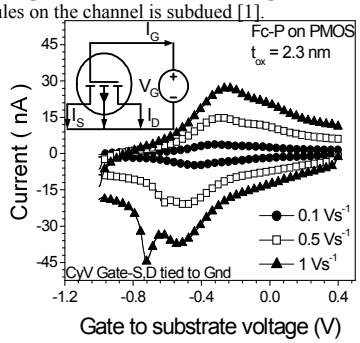


Figure 5b CyV of gate-substrate of a hybrid PMOS with Fc-P on gate oxide. Source and drain terminals are tied to ground. Effect of scan rate on the second redox peak associated with molecules on channel. Inset shows the electrical connections made for the measurement with direction of the currents indicated.

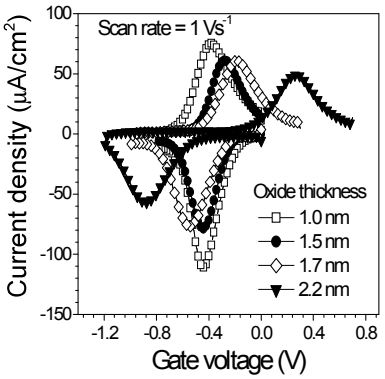


Figure 2a Cyclic votammetry (CyV) of EMOS capacitors with Fc-P on oxide on p-Si, t_{ox} varying from 1.0 to 2.2 nm. Scan rate is 1 V/s. Peaks in the lower half (negative currents) correspond to oxidation and peaks in the upper half (positive currents) correspond to reduction of the molecules. The peak separation increases with increasing oxide thickness.

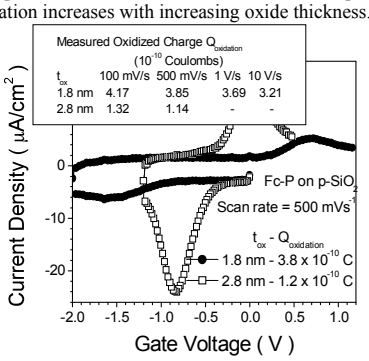


Figure 3b CyV of EMOS capacitors with Fc-P on oxide on p-Si, with two different t_{ox} (1.8 and 2.8 nm). Scan rate is 500 mV/s. The area under the redox peaks for the capacitor with 2.8 nm oxide is significantly smaller than that for the capacitor with 1.8 nm oxide, which indicates decreasing redox charge with increasing t_{ox}. Inset shows the measured charge at different scan rates for the two capacitors.

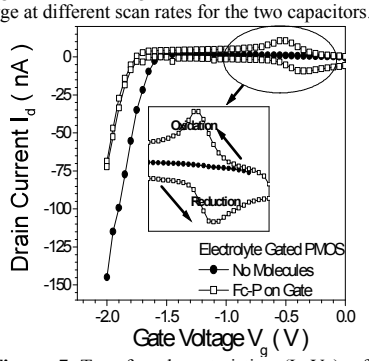


Figure 7 Transfer characteristics (I_D-V_G) of a hybrid PMOSFET with 2.8 nm gate oxide. The peaks in the sub-threshold region are associated with redox of molecules in the overlap regions. The oxidation and reduction currents are swapped because the gate current is in the opposite direction of the drain current. MOSFET without any molecules did not show any such peaks.

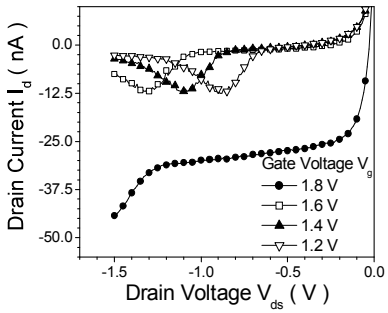


Figure 8a Transistor characteristics of hybrid PMOS with 2.8 nm gate oxide, with the transistor in the sub-threshold region. The peaks are associated with the reduction of molecules in the overlap region. There is no increase in the drain current after the reduction of the oxidized molecules on the overlap region.

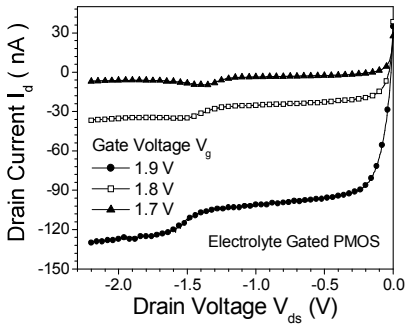


Figure 8b Transistor characteristics of hybrid PMOSFET with 2.8 nm gate oxide, with the transistor turned on. There is an increase in the drain current after the reduction of the oxidized molecules on the channel close to the drain terminal.

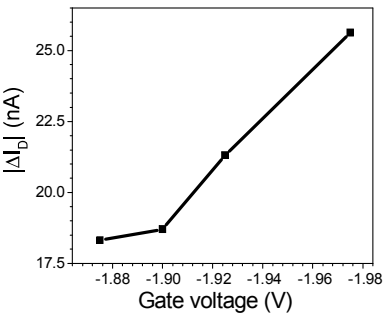


Figure 8c Change in drain current (DI_D) versus gate voltage for the hybrid PMOSFET with 2.8 nm gate oxide, showing a linear dependence when the device is turned on, indicating a constant decrease in threshold voltage due to reduction of oxidized molecules on the channel near the drain terminal.

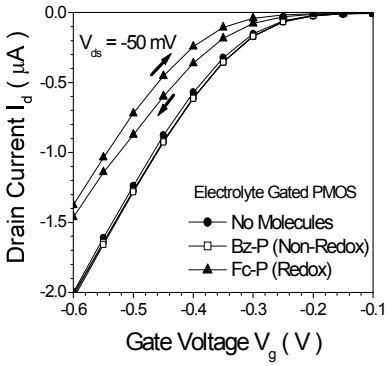


Figure 9a Transfer characteristics of hybrid PMOSFETs with redox molecules (Fc-P), non-redox molecules (Bz-P) and no molecules on the gate oxide. The gate oxide thickness is 1.2 nm. The arrows indicate the direction of the voltage sweeps for the hybrid device with redox molecules. There exists no hysteresis between the forward and reverse scans for the devices with non-redox and no molecules.

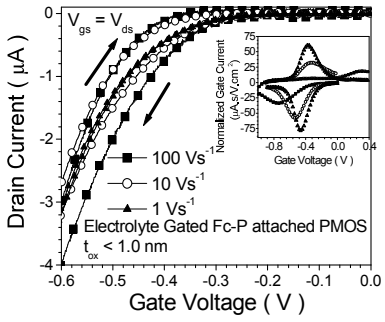


Figure 9b Transfer characteristics of hybrid PMOS with < 1 nm gate oxide: effect of scan rate on the redox-related hysteresis. Inset shows CyV of gate-substrate at the same scan rates with source and drain tied to ground.

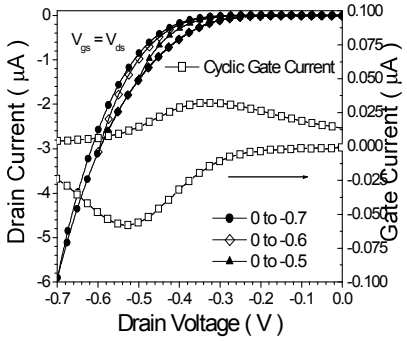


Figure 9c Transfer characteristics of hybrid PMOSFET with < 1 nm gate oxide: effect of the gate voltage scan range on hysteresis. CyV of this device shows that the amount of hysteresis is directly correlated to the redox charge.

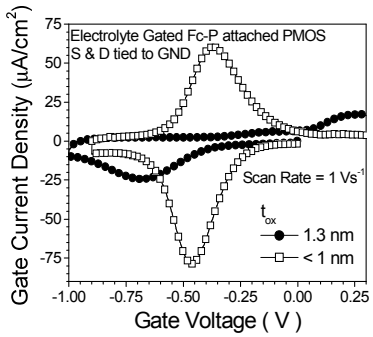


Figure 10a CyV of gate-substrate on hybrid PMOS with the source and drain tied to ground. Gate oxides of the devices are 1.3 nm and < 1 nm.

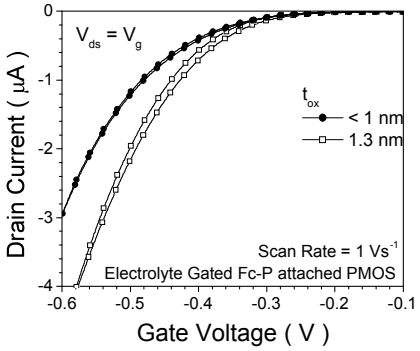


Figure 10b Transfer characteristics of the two devices at 1 V/s. The redox-related hysteresis is greater for the device with thicker oxide. The threshold voltage of the device with thinner oxide is slightly higher than that of the device with thicker oxide due to the higher density of screened charges (oxidized molecules) in a given voltage range.

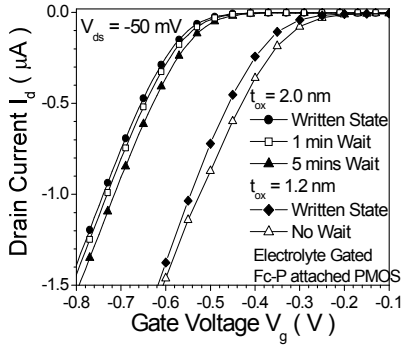


Figure 11 Memory effect exhibited in hybrid PMOS devices with increased oxide thickness. The device with 2 nm gate oxide retained the written state for over a minute and recovered to the erased state after 5 minutes. The device with 1.2 nm gate oxide retained charge for a shorter period.

Appendix 4 Floating Drop Experiments

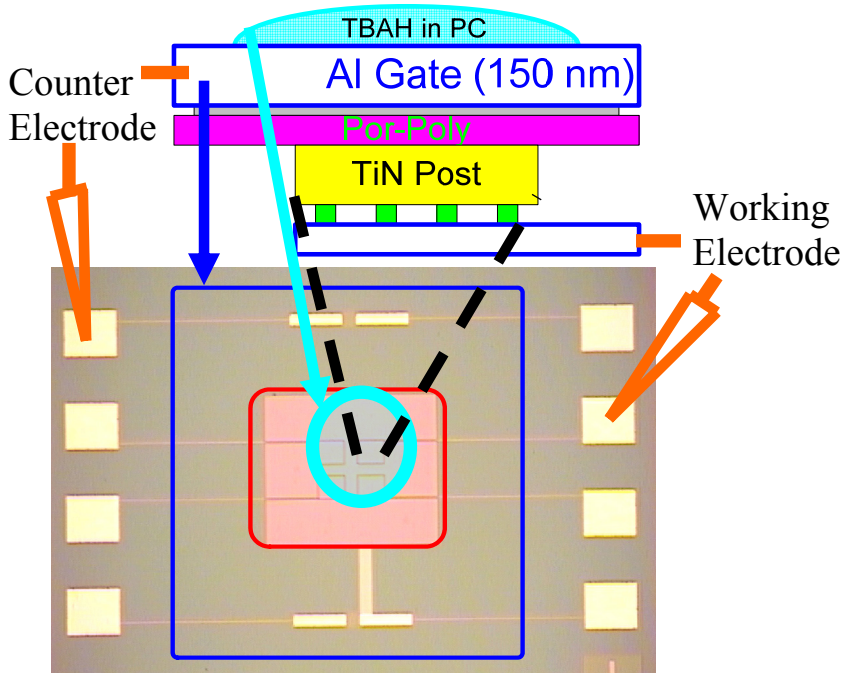


Figure 1 Schematic showing test die layout and experimental setup for floating drop (FD) measurements. The bottom half of the figure shows top-view of layout of the test capacitors (4 TiN substrate posts in each die). The top half shows the cross-sectional view of one of the capacitors (Al/AlN/**Por-Poly**/TiN). The thickness of the AlN layer is generally around 4 nm. The estimated thickness of the **Por-Poly** film depends on the concentration of the attachment solutions and is typically around 5, 10, and 20 nm for the concentrations of 1, 2 and 3 mM, respectively. Area of each capacitor is defined by the area of the TiN post, which is 100 μm x 100 μm. AlN is sputtered through a shadow mask which opens up within red square shown in the top view and Al gate is evaporated through a shadow mask which opens up within blue square. The electrolyte drop is confined within the Al gate. In CyV measurements, the gate voltage is applied at the counter electrode with reference to the working electrode. In case of FD measurement, counter electrode is connected to the Al gate (along with reference electrode) and the working electrode is contacted to the TiN post.

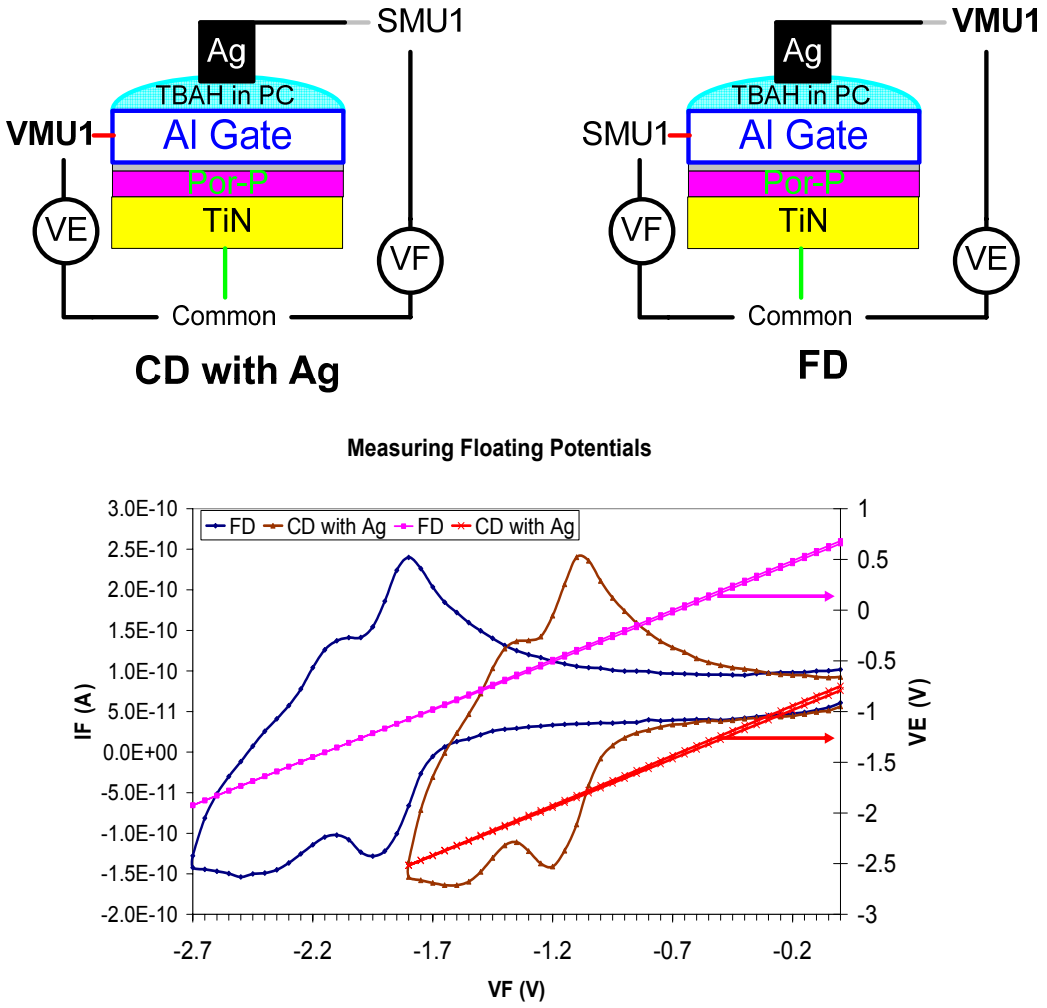


Figure 2 Schematic of measurement setup and the plot of floating potential measurements using an IV-meter (HP 4155 A) of a Al/AlN/**Por-Poly**/TiN capacitor. SMU stands for Source-Measure Unit and VMU stands for Voltage-Monitor Unit. VMU has input impedance in giga-ohm range and can monitor voltage at a terminal without sinking the charges at the terminal. In CD with Ag measurement here, potential at floating Al-gate is monitored during CD measurement scan. In FD measurement here, potential at floating electrolyte drop is monitored by contacting with an Ag wire. The thickness of Al and AlN films were around 150 nm and 40 Å, respectively. IF is the current measured at SMU1.

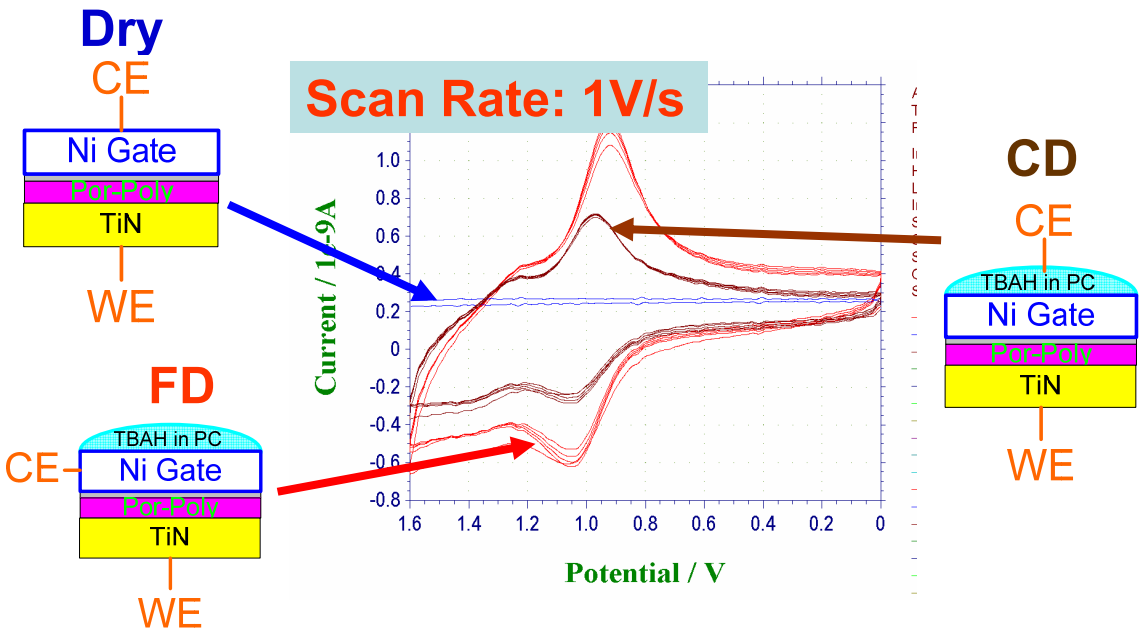


Figure 3 CyV of characteristics of Ni/AlN/**Por-Poly**/TiN capacitor: (i) Completely Dry, (ii) FD, and (iii) CD with Ag wire contacting the electrolyte drop on Ni gate. The voltage axis in the plots correspond to substrate voltage with respect to gate, which is reverse in polarity of the gate voltage in the plots in main part of the dissertation. In CyV measurements, the gate voltage is applied at the counter electrode (CE) with reference to the working electrode (WE).

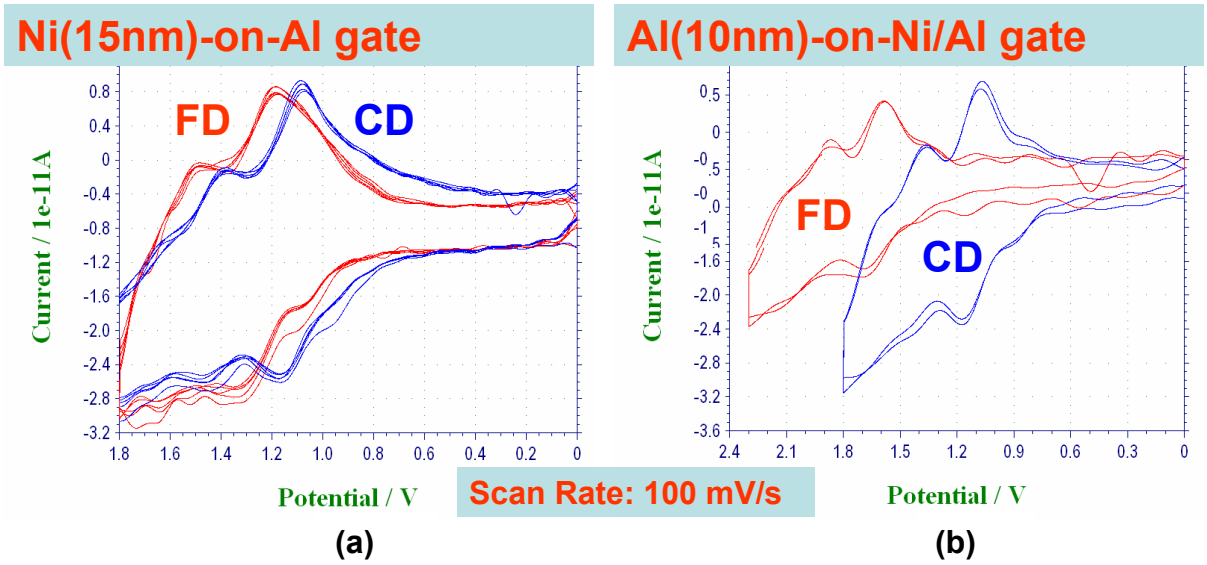


Figure 4 FD measurements showing that the top-most metal in contact with the floating electrolyte drop determines the redox peak potential: **(a)** Redox peak potential in case of FD measurement for Ni(15nm)/Al/AlN/**Por-Poly**/TiN capacitor were closer to that in CD measurement for the same

structure. **(b)** Redox peak potential in case of FD measurement for Al(10nm)/Ni(15nm)/Al/AlN/**Por-Poly**/TiN capacitor shifted to higher negative 500 mV as compared to that in CD measurement for the same structure, and was similar to FD measurement for the Al/AlN/**Por-Poly**/TiN capacitor structure. The CD measurement in both cases was done using Ag wire. The thickness of Al and AlN films were around 150 nm and 40 Å, respectively. The voltage axis in the plots correspond to substrate voltage with respect to gate, which is reverse in polarity of the gate voltage in the plots in main part of the dissertation.

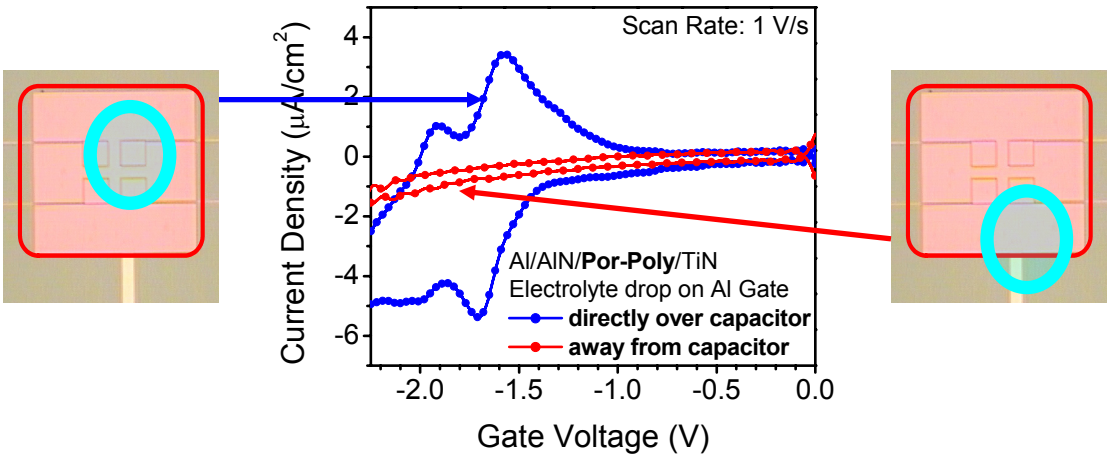
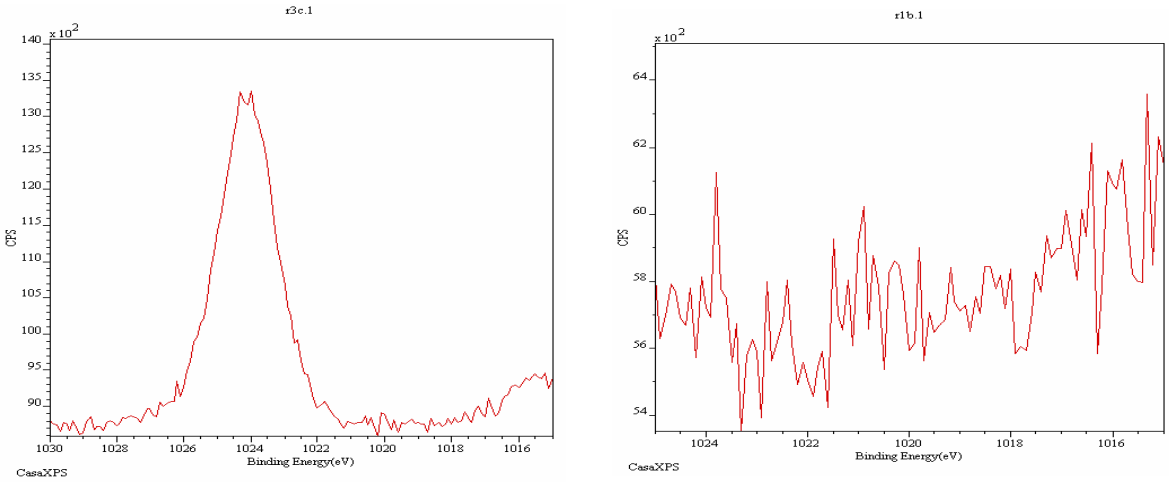


Figure 5 FD measurements showing that the redox peaks are observed only when the floating drop is directly on top of the capacitor active area (TiN post). When the electrolyte is not directly on the capacitor (TiN post), but within the Al gate on the overlap region, FD CyV shows parallel-plate capacitor behavior similar to completely dry measurements. The blue oval in the top-view layout indicate the electrolyte-drop and the top-right capacitor is the device under test.



(a) **(b)**

Figure 6 XPS analysis results of : **(a)** control **Por-Poly** film on TiN substrate showing prominent peak associated with zinc (Zn), and (b) Al gate on AlN/**Por-Poly**/TiN, which did not show any Zn peak. The porphyrins used in this work contain Zn. The thickness of Al and AlN layers were 150 nm and 4 nm, respectively.

Appendix 5 Solid-State MoleFETs

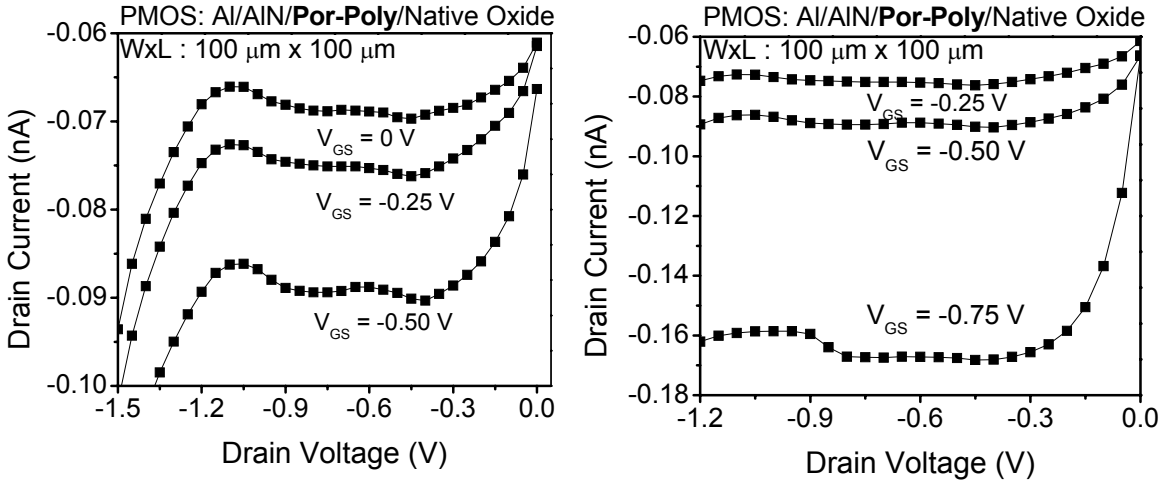


Figure 1 I_D-V_D characteristics of solid-state MoleFET incorporating **Por-Poly** film. Peaks are observed in the sub-threshold (V_T = - 1.5 V) transfer characteristics of the device similar to electrolyte-gated high-V_T MoleFET devices presented in chapter 5 of the dissertation. However, a two-step increase in drain current was not observed in the I_D-V_D characteristics for gate voltages higher than the V_T of the device.

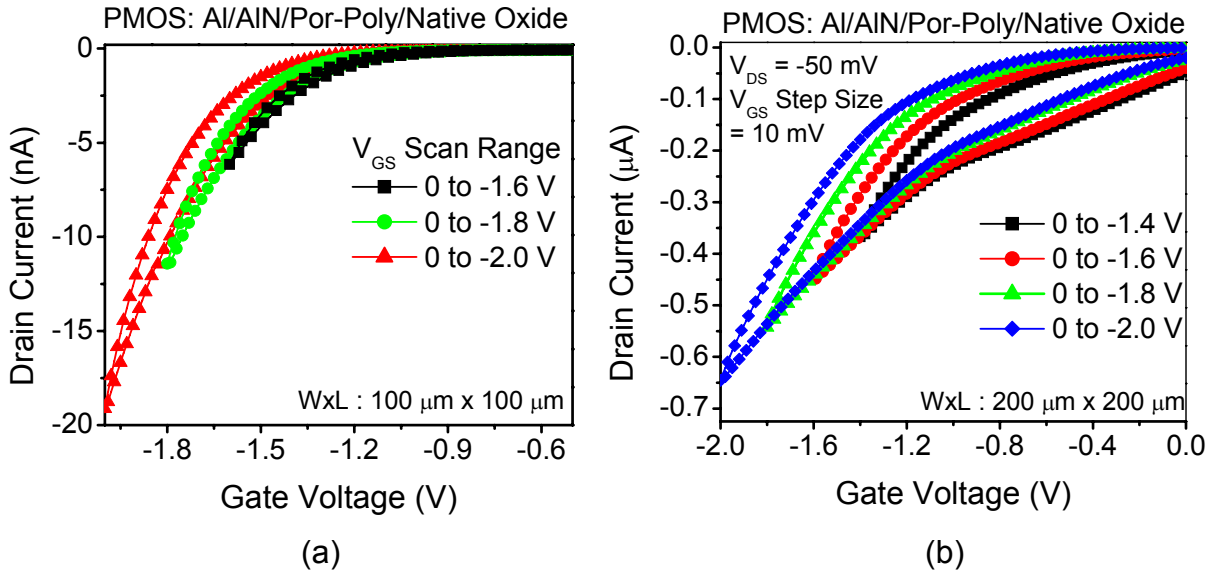


Figure 2 I_D-V_G characteristics of solid-state MoleFET showing scan-range dependent hysteresis: **(a)** High-V_T device, and **(b)** Low-V_T device.