ABSTRACT

HAJ-MAHARSI, MOHAMED YASSINE. Novel DC Ring Topology and Protection System – a Comprehensive Solution for Mega City Power Grids. (Under the direction of Dr. Alex Q. Huang.)

The development of mega cities leads to increased load concentration and brings additional challenges to managing the electrical grid while keeping power available for critical loads. Techniques using FACTS devices are being applied to alleviate power management difficulties and to confine faults in their originating areas in order to limit the risk of cascading failures in the grid. The addition of many FACTS devices often results in control and protection coordination difficulties, power oscillations between connected networks, subsynchronous resonance problems, and torsional interactions with nearby generator units. The most effective solution is obtained when the individual AC subsystems representing sources and loads are decoupled so a fault in a given subsystem is not propagated to another subsystem. This solution can be achieved by the deployment of a DC system where power sources and loads are connected to the DC bus through voltage source converters. For a mega city, this would be conceived as a DC ring feeding multiple loads and connected to remote and local power sources.

Unfortunately, the lack of fast DC circuit breakers has been one of the key issues affecting extensive applications of DC systems with common DC buses; a DC fault would discharge all the capacitors of the DC bus and cause delays in system recovery and possibly a wide system collapse.

In this research, I provide a comprehensive solution to mega city power grid problems by proposing a DC system topology that enables grid expansions without affecting existing protection settings or changing existing AC breaker ratings. I also propose the means for protecting the DC system by designing a fast DC breaker and developing a control algorithm capable of isolating DC faults without blocking converter stations or depleting DC bus capacitors. My contribution is three folds:

1) I modeled and simulated Shanghai power grid and performed a study to identify short circuit and voltage stability problems using data provided by ABB corporate research located in China. I built on the work that had been performed in ABB China by considering different contingencies and I applied solutions using individual FACTS devices such as FCL, SVC-Light®, and HVDC-Light®. I analyzed the results from each solution in order to assess its merits and limitations in dealing with fault current and voltage stability problems. Then I presented a novel DC ring topology that provides redundancy, better protection against cascading faults, and does not increase short circuit levels. With this topology, adding loads or power sources does not impact system protection or performance.

2) I proposed two novel designs for a DC circuit breaker that is of critical importance to DC applications using multiple converter stations. The proposed designs solve the problem of DC fault clearing without causing significant voltage drops, current oscillations, or shutting down of any converter station connected to the DC bus. The DC breaker rated at a voltage of 320 kV and a current of 3000 A can interrupt DC currents as high as 70 kA within 800 μs.

3) I proposed a novel placement of the DC circuit breakers within the DC ring topology combined with an intelligent protection algorithm that optimizes fault detection and isolation without affecting the rest of the DC system. The protection scheme uses local measurements and special coordination techniques for clearing solid faults and uses differential measurements to identify and isolate high impedance faults.

Novel DC Ring Topology and Protection System – a Comprehensive Solution for Mega City Power Grids

by
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DEDICATION

I dedicate this work to my lovely wife Hounaida
and lovely daughters Safa and Sarah.

BIOGRAPHY

The author, Mohamed Yassine Haj-Maharsi, was born in Tunisia, in 1964. Mohamed received his B.S. and M.S. degrees in Electrical Engineering from "*University de Quebec à Trois-Rivières*", Canada, in 1987 and 1989 respectively.

Mohamed joined ABB corporate research in 2000 after he had spent ten years of technical and managerial experience with IREQ (Hydro-Quebec Research Institute) where he had been involved in activities covering design reviews of different FACTS technologies supplied to utilities by ABB, GE, Siemens, and Westinghouse.

In ABB corporate research, Mohamed has been particularly active in developing new protection products with improved performance and reliability. He also led the development and implementation of novel algorithms for detecting high impedance faults and pushed creative ideas for high and medium voltage technology improvement.

Mohamed has many publications in ABB review journals, IEEE journals, and conferences. He is also the author of 45 patents and invention disclosures covering a wide range of applications. Mohamed won the inventor of the year award for both 2007 and 2008 and received the circle of excellence award in 2008 from ABB corporate research in USA.

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LIST OF ABBREVIATIONS

ABBREVIATION	DEFINITION
AC	Alternating Current
ACCB	Alternating Current Circuit Breaker
CB	Circuit Breaker
CSC	Current Source Converter
CSI	Current Source Inverter
DC	Direct Current
DCCB	Direct Current Circuit Breaker
EPC	Equidistant Pulse Control
ETO	Emitter Turn-Off thyristor
FACTS	Flexible Alternating Current Transmission System
FCL	Fault Current limiter
FCLCB	Fault Current Limiting Circuit Breake
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage Direct Current
HVDC-Light	HVDC with voltage source converter
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Controlled Thyristor
IPC	Individual Phase Control
PFC	Pulse Frequency Control
PPC	Pulse Period Control, and Pulse Phase Control
PWM	Pulse Width Modulation
SF6	Sulfur hexafluoride
SSR	SubSynchronous Resonance
SSTI	SubSynchronous Tortional Interaction
STATCOM	Static Synchronous Compensator
SVC	Static VAR Compensator
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

CHAPTER 1 INTRODUCTION

1.1 Background and motivation for this work

Mega cities are characterized by heavy concentration of industrial and residential loads with different degrees of power quality requirements. Hospitals, data centers and automated factories are more sensitive to voltage fluctuations and harmonics than other loads. The high concentration of businesses and people in mega cities

raises also the question of power availability and security. Therefore, these cities are fed through multiple power paths and from many power sources to ensure redundancy as well as reliability. However, fast increasing loads and their densities augment the short-circuit current to levels that challenge existing circuit breaker ratings and their protection coordination.

Mega city multi-infeed issues are arising in places like Beijing, Shanghai & Guangzhou, already characterized by voltage transient problems caused by millions of air conditioning units, typical heavy loading, and huge short-circuit current levels. Moreover, due to limited construction areas and strict environmental requirements, it is inevitable to remove power plants from city centers and import power from remote locations. For example, power imports from outside the city has contributed to two thirds of the whole electricity consumption in Beijing, while short current levels in Shanghai are dangerously reaching 63 kA; the highest current level existing circuit breakers can handle. These high short-circuit current levels have prevented the expansion of power grids to meet fast increasing loads and demographic development.

In order to resolve power management in mega cities with minimum environmental impacts, underground substations along with high voltage AC cables are introduced into urban areas. Other techniques such as network partition schemes are widely adopted to restrain short-circuit current levels. For example, the 220 kV system of

Beijing power grid is divided into East and West subsystems, and that of Shanghai power grid is divided into several subsystems. Other apparatus such as series reactors and fault limiting devices are also introduced to limit the fault current at levels existing circuit breakers can interrupt.

Unfortunately, such AC based solutions are reaching their capability limits in solving mega city problems and a new solution approach is required. As most of the mega city problems are related to power quality, system protection, and reliability, the decoupling of the mega city AC network into subnetworks that are easily manageable constitutes an attractive solution. This can be achieved using a DC distribution or subtransmission system where a DC ring surrounding the city is fed from local and remote power sources. Residential and industrial city loads are then hooked to the DC ring through voltage source converters that will regulate power factor, control power flow and reduce fault current levels.

The successful implementation of such solution is contingent: 1) to the existence of an intelligent network topology that easily connects power supplies to sensitive loads even during faults, 2) to the implementation of a fast protection scheme that isolates faulty segments of the DC system without shutting OFF any converter station or depleting DC capacitor banks, and 3) to the availability of a DC fault management device or DCCB capable of quickly interrupting DC currents without creating voltage arcs or introducing current oscillations.

These elements of success are the focus of this research where I made special efforts on analyzing state of the art solutions and assessing their limits. The analysis outcome provided the catalyst for proposing a different approach to solving mega city power grid problems through innovation in system topology, apparatus design, and protection implementation.

1.2 State of the art; technology and practices

The work I present in this dissertation involves fault current limiting devices and practices, voltage regulation devices, active and reactive power controls, as well as DC fault interrupting devices. Due to the amount of data and the independent nature of these subjects, I decided to discuss them in separate chapters and let the reader choose which one to read. I provide a full description of these chapters in the dissertation outline.

1.3 Dissertation outline

Through this research, I provide a novel and comprehensive solution to mega city power grids by identifying the proper DC system topology, designing the required protection device, and implementing the right control algorithm. I achieved this work in many phases starting with system analysis to better identify the problems and requirements of city grids. I used Shanghai power grid as a testbed for my study. I

applied devices such as FCL, SVC-Light®, and HVDC-Light® as possible solutions to certain grid problems and I assessed their merits and limitations. An overview of these technologies is deemed necessary and is reported in separate chapters. As of the dissertation it is organized into eight chapters as follows:

Chapter 1: Introduction

In this chapter, I present the background and motivation for this research activity and I describe how this document is organized.

Chapter 2: Overview of fault current limiting devices

Some utilities faced with increased fault current levels had looked for solutions such as upgrading existing circuit breakers to higher ratings, splitting highly loaded buses, and placing fault current limiter devices in critical locations. In this chapter, I report different current limiting devices and I discuss their characteristics. The main goal of introducing these devices is to assess their potential in solving fault current problems in mega cities; a problem that is tackled in Chapter 5.

Chapter 3: Overview of voltage regulating devices

In this chapter, I provide an overview of the technology used for reactive power compensation and I outline the design principle and operation of the SVC as well as

of the STATCOM (referenced here as SVC-Light®). The goal of discussing particularly these two devices is to understand their contribution in addressing voltage instability and power flow control problems. These devices are considered when solutions to improve voltage regulation, increase system stability, and enhance power factor are discussed.

Chapter 4: Overview of HVDC technologies

In this chapter, I conduct a background research on HVDC and HVDC-Light® in order to assess the state of the art of the technology and its applications. I provide detailed description and comparison of current source converter and voltage source converter based HVDC systems and I survey possible applications and their relative impacts on the power grid. I deemed important to introduce this material to the reader because HVDC technology plays a big role on the solutions I have proposed to solve power grid problems.

Chapter 5: DC ring topology; a novel solution for mega city applications

In this chapter, I model and simulate Shanghai power grid and perform a study to characterize short circuit and voltage stability problems. I use system data provided by ABB corporate research located in China and complement their work by introducing other solution scenarios. Then I present a novel solution based on a DC

ring topology using voltage source converters to connect loads and power sources without impacting system short circuit level. Then, I identify the need for a fast protection system that would isolate DC faults without disconnecting sensitive loads, depleting DC bus capacitors, or blocking converter stations.

Chapter 6: Novel designs of a DC circuit breaker

In this chapter, I identify the need for a fast DCCB as one of core elements required for a successful implementation of a DC ring topology around a mega city such as Beijing or Shanghai. A fast DCCB will also make possible the application of multiterminal HVDC-Light® system with a common DC bus, the realization of a wind farm with a DC collector, and the proper protection of a navy ship equipped with a DC distribution grid. In this chapter, I present two novel designs for a DCCB to address both unidirectional and bidirectional power flows. The performance of the DCCB is proven through simulation performed for different fault contingencies.

Chapter 7: Novel DCCB deployment in a DC ring and protection techniques

In this chapter, I present a DC ring topology with properly placed DCCBs and a detailed fault protection scheme for application in a system using multiple HVDC-Light® stations. The proposed protection scheme uses local measurements and special coordination techniques for detecting and clearing low impedance faults and

it uses differential measurements to identify and isolate high impedance faults. Digital simulation performed for different contingencies confirmed the performance of the protection scheme in locating and clearing DC faults without interrupting power supply to sensitive loads.

Chapter 8: Summary and future work

In this chapter, I present the main findings of the work I performed for this dissertation. These findings include the characterization of mega city power grid problems and their applied solutions. I emphasize the merits and limitations of these solutions and I highlight my novel and comprehensive approach to solving power grid problems. Then I identify some of the remaining challenges for future investigation.

CHAPTER 2 OVERVIEW OF FAULT CURRENT LIMITING DEVICES

When electrical loads in big cities increase they require rethinking of how power is distributed and how the grid is protected. This requirement is driven by the voltage instability concerns and increased fault current levels caused by additional power demands. Incremental addition of loads and power sources to a given bus increases

the fault current to levels no longer sustainable by existing protection equipment. Consequently, utilities are forced to upgrade their protection devices, split the main buses into two or three secondary buses that would be served by smaller transformers, or install fault current limiting devices in critical paths.

There is a multitude of devices capable of addressing the issue of increased fault current while keeping a tradeoff between fault control and power grid performances. These devices have merits and limitations and their operating principles and applications differ from each other.

In this chapter, I report different current limiting devices and I discuss their characteristics. The main goal of introducing these devices is to assess their potential uses in solving fault current problems in mega cities; a problem that is tackled in Chapter 5.

2.1 Introduction

The development of mega cities around the world such as Tokyo, Mumbai, Beijing, Shanghai, Guangzhou, and Dhaka leads to increased load concentration and brings additional challenges to managing power on already strained networks while keeping power availability at higher rates. The increase in power demand requires addition of new local generation units or importing power from remote regions. This will in turn increase the fault current levels and would require an upgrade of

protection devices and an update of control strategies on the power grid. Some utilities faced with increased fault current levels had looked for solutions such as upgrading circuit breakers to higher current interruption levels, splitting highly loaded buses, and placing fault current limiter devices in critical current paths.

In this chapter, different current limiting devices are reported and their characteristics are discussed. The main goal of introducing these devices is to assess their potential in solving fault current problems in mega cities; a problem that is tackled in Chapter 5.

2.2 Structure of this chapter

This chapter covers FCL devices and application practices. The introduction and outline of this chapter are reported in sections 2.1 and 2.2 respectively. In section 2.3 different placement options of the FCL are discussed. In sections 2.4, 2.4.1 through 2.4.6 different type of FCL devices are discussed based on their designs and mode of operations. The conclusion of this chapter and a list of references are provided in section 2.5 and 2.6 respectively.

2.3 FCL applications

Fault current limiter principle of operation consists of inserting additional impedance in the path of the fault to limit its current to levels that can be interrupted by

protection equipment. The insertion of the additional impedance can be achieved in different ways depending on the nature of the limiting device. For devices using non-super conducting material, the insertion can be permanent in the form of a reactor placed to increase the fault impedance in critical fault paths. It can also be in a form of a special transformer having high leakage impedance. This approach is cost effective but increases losses, reduces the stiffness of the network, and leads to voltage control problems. The other alternative is to switch-in the impedance upon detection of the fault. This method has the merit of intervening only during faults and of leaving the network impedance unchanged during normal operations.

For devices, where the impedance changes when subjected to high currents, there is no need for switching mechanisms. The device, in this case, is permanently connected and shows near zero impedance for normal currents but quickly increases its impedance in presence of high current levels. Such a device can be realized using a resonant LC circuit, a superconducting inductor, a superconducting resistor, or a liquid metal based material.

The choice of location for a fault current limiter is dependent on the problem to be addressed and some locations would lead to better utilization of the device than others. In practice, three locations are commonly used; the first, shown in Figure 2-1, places the FCL in series with the main transformer in order to protect the entire bus. This configuration is the most used and it favors the use of a single large transformer

with low leakage impedance that maintains good voltage regulation. The use of an FCL in this location provides fault current limitation to all the feeders departing the bus and eliminates the need to upgrade their protection equipment.

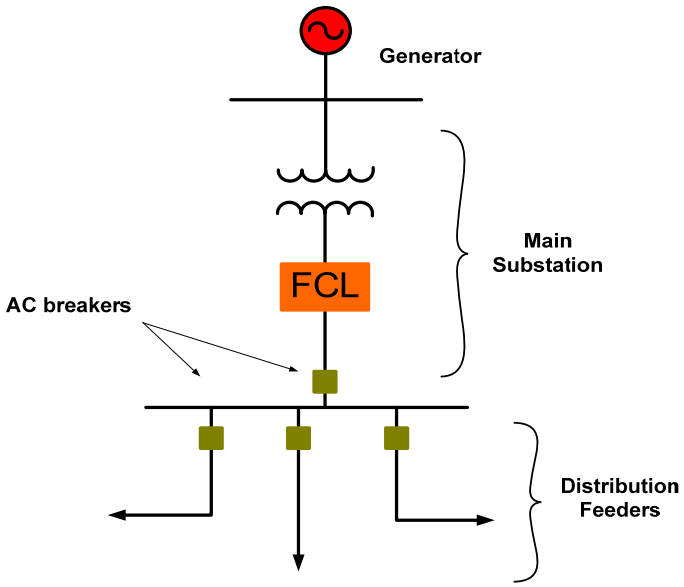

Figure 2-1: FCL in a substation main position

The second location, shown in Figure 2-2, places the FCL on a single feeder leaving the main bus in order to selectively protect underrated equipment and reduce the cost of the solution. In this configuration, a small and less expensive FCL can be used to reduce fault current on overstressed equipment such as cables, circuit breakers, and transformers.

The third location, shown in Figure 2-3, places the FCL in a bus-tie position in order to protect both buses in case of a fault. In this particular configuration any faulted

bus receives the full fault current of only one transformer. Additional advantages of this configuration include: better use of transformer rating because any excess capacity from one bus is available to the other. Also the fact of paralleling the transformer reduces the impedance and makes the system stiffer so resulting in good voltage regulation and eliminates the need for tap-changing transformer.

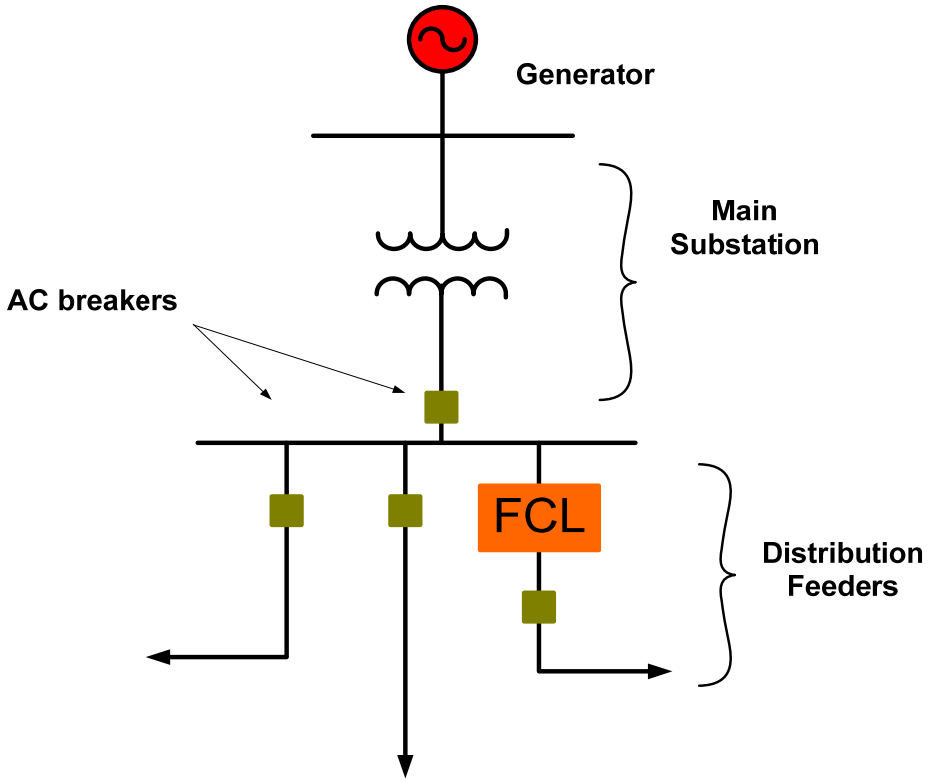

Figure 2-2: FCL in a substation feeder position

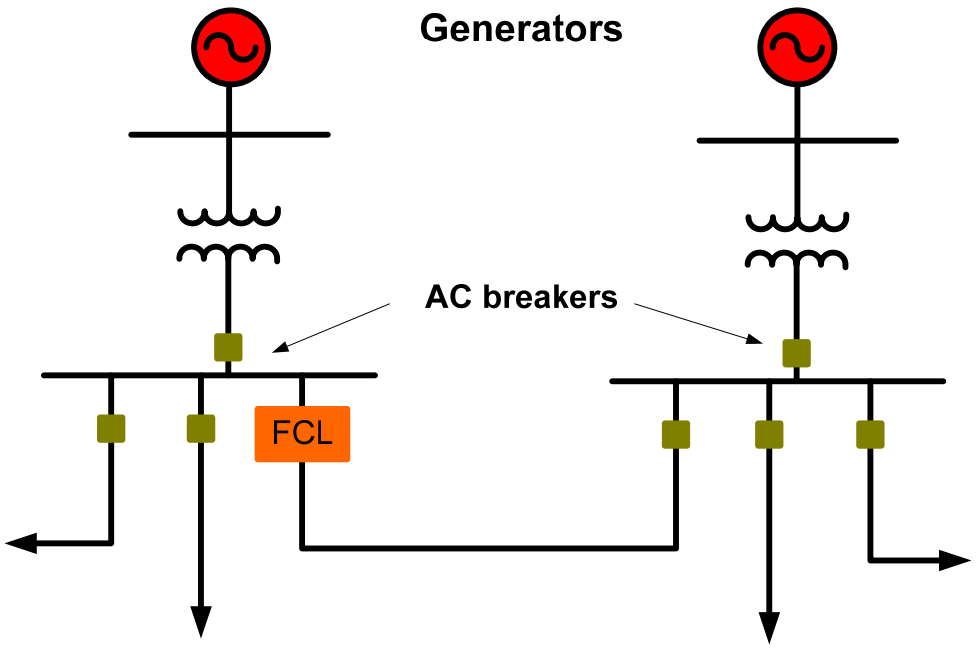

Figure 2-3: FCL in a bus-tie position

2.4 Fault current limiters

There are different existing devices for current limiters using conventional power electric elements such as resistors, reactors, capacitors, and transforms. These components can be inserted in permanence into the grid or switched-in when a fault is detected. The difference in implementation costs will define which alternative is more appropriate for a given situation.

Other FCL devices are based on the characteristics of certain materials that change the impedance of the device as function of its temperature. These devices include superconducting or polymer materials. These are self triggered and return to prefault state when the fault is cleared. In the following subsections, an overview of certain FCL devices is presented.

2.4.1 Reactors

Reactors are the simplest means of limiting fault currents in power grids. Therefore, they are commonly used in substations and in other locations in the feeders. A rector is permanently connected to the power grid and does not need any special equipment or control mechanism for its operation. Consequently, a reactor is the most cost effective current limiting device in the market. But this cost does not take into account the power losses in the reactor or the increased system impedance that makes the network weaker and complicates voltage regulation. Therefore, it is important to correctly size the reactor and choose the proper placement for its installation [01].

Some utilities choose to place the current limiting reactor in the neutral point of the circuit. This choice is adequate for balanced systems that do not experience a lot of three-phase to ground faults. The neutral connection makes the reactor invisible under balanced normal condition or reduces the losses of the reactor under slight

system imbalance. The claim is that, only a portion of the load current would flow through the reactor during slight imbalance by contrast to full load current when the reactor is placed elsewhere.

2.4.2 High impedance transformer

A high impedance transformer is characterized by high leakage impedance specifically designed to limit fault current. The principle of operation of this transformer is equivalent to a conventional low impedance transformer in series with a reactor. The cost of constructing a high impedance transformer is more than that of a regular transformer due to special winding designs and limited orders.

The performance of a high impedance transformer in limiting fault currents is the same as that of a rector and its use results in the same power losses and voltage regulation problems.

2.4.3 Tuned LC circuit

The Tuned LC circuit uses the principle of impedance compensation employed in transmission line to reduce line impedance. In the FCL shown in Figure 2-4, the total impedance of the device is a combination of a series inductor L_1 and a parallel L_2C circuit containing a nonlinear inductor L_2. Under rated currents, the equivalent impedance of the parallel L_2C circuit is capacitive and is equal in amplitude to that of

inductor L_1. Therefore, Z_{FCL} is zero when the system is operating under normal conditions. During faults, inductor L_2 saturates and limits the voltage drop across the capacitor making the overall impedance inductive. This solution uses the intrinsic characteristic of a nonlinear reactor to detune the L_2C circuit and changes the impedance seen by the power grid without any external means. The solution employs conventional elements and can be used in medium and high voltage applications [02].

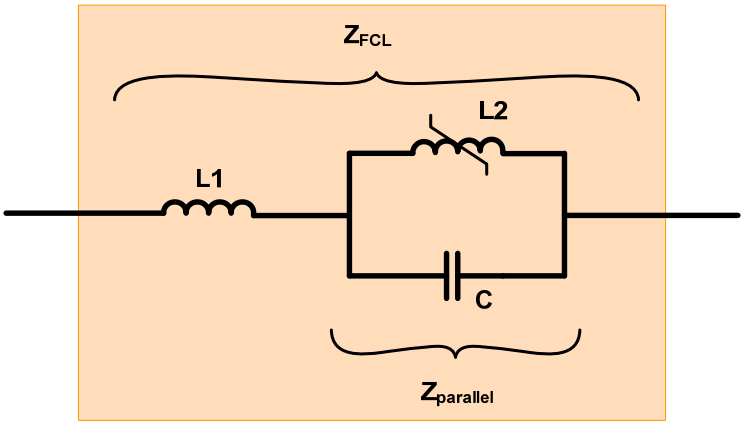

Figure 2-4: FCL based on a tuned LC circuit

2.4.4 Polymer PTC resistor based FCL

The polymer PTC resistor is based on a polymer composite that is sensitive to temperature. The composition of the polymer includes conductive material based-particles that are in contact to each other and provide a path for current flow under ambient temperature. Therefore, during normal system operation, the PTC device is

characterized by a low resistance. When a fault occurs, the current through the device increases and causes the polymer to heat and expand. The expansion of the polymer disconnects the conducting particles and turns initially low resistive current paths to high resistive current paths.

The principle of polymer PTC is widely used in low power consumer electronics such as resettable fuses, self-regulated heaters and so on. In power applications, ABB had developed a distribution voltage PTC device in year 1999. The device is rated for applications up to 12 kV and showed encouraging performance. More details of this device are reported in [03].

2.4.5 Liquid metal current limiters

Liquid metal applications have been investigated by many researchers around the world and many patents using liquid metal were filed [04].

The principle of operation of certain devices using liquid metal is based on the change of state of the metal when subjected to high currents. At current levels resulting in normal operating temperatures a column of liquid metal used as conductor exhibits low impedance. When a fault occurs in the system resulting in a higher current through the column, the liquid heats up and reaches a temperature where it changes states; part of the liquid becomes vapor and provides high resistive path to the current. When the fault is cleared by a protecting device such as a circuit

breaker, the current through the column is interrupted and the liquid metal cools back to its prefault temperature. The cooling time may vary depending on the cooling mechanism in place.

Overview of liquid metal FCL patents indicated that some designs are based on the high magnetic field present in the constriction known as “Pinch effect” [05].

This effect is a direct consequence of the contraction of the liquid metal in presence of magnetic filed. A contracted liquid metal sees its molecules compacted which increases the current density resulting in increased current carrying capacity.

2.4.6 Superconductive fault current limiters

Superconducting material is characterized by an interesting feature making its application in power system such as transformers, machines, and FCL devices the focus of research and evaluation by many product developers and research labs.

The ability of superconducting material to exhibit near zero impedance at certain operating conditions and high impedance at others is particularly useful for fault current limiting applications. The variables governing the change of state of a superconducting material are current density, magnetic field, and temperature. These three variables define the boundaries of the superconductivity zone as illustrated in Figure 2-5.

In a FCL using superconducting material, the device is electrically invisible when the power system is operating under normal conditions. The temperature of the superconducting material is maintained by a dedicated cooling system to ensure a critical temperature is not breached. When a fault occurs, the current passing in the FCL heats the superconducting material and causes it to quench. When quenched, the superconducting material reverts to its normal state with impedance much higher than that exhibited during normal system operations. This high impedance limits the fault current to levels that are sustainable by existing protection equipment [06].

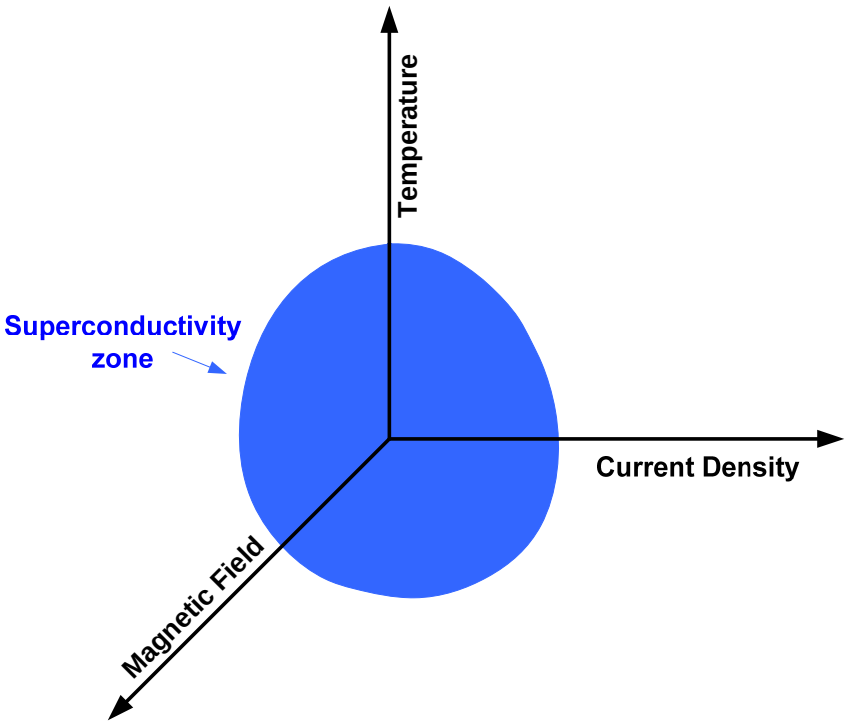

Figure 2-5: Properties of superconductors

Superconductivity material is used to design FCL devices using resistors and inductors [07]. Both designs are being investigated by researchers to better identify their relative merits and limitations. So far the resistor based FCL offers simpler design, smaller foot print and lower cost solution than the inductive one.

One of the technical challenges facing the use of superconducting material in general is the heat management and the time cycle for the material to cool back to its superconducting state. Actually obtained performances require up to 17 hours for the material to gain its superconductivity features from ambient temperature. This limitation prohibits the use of superconducting material in FCL devices due to the repetitive nature of faults and the reclosing practices implemented by utilities in their protection relays.

2.5 Conclusion

This chapter discussed the FCL principle and overviewed some of the devices contemplated for practical system implementations. Cost effective devices using conventional elements such as reactors and high impedance transformers are simple to implement but have drawbacks on voltage regulation and losses. Devices using tuned LC circuits and presenting near zero impedance for normal system operations and high impedance during faults constitute the best solution to limiting

fault currents because of their simple implementation, self triggered feature and cost effectiveness.

FCL devices based on superconducting materials are facing challenges that require a technological breakthrough for these devices to become economically and operationally viable. Actual technologies require long time cycle to cool the material and are characterized by hot spots that may jeopardize the correct operation of the device.

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CHAPTER 3 OVERVIEW OF VOLTAGE REGULATING DEVICES

In this chapter, I provide an overview of the technologies of reactive power compensation and I outline the different design and operation principles of Static VAR Compensators (SVC) as well as Static Synchronous Compensator (SVC-Light®). The goal of discussing particularly these two devices is to understand their

contribution in addressing some of the issues mega city power grids are facing such as voltage instability and power flow control. These devices are considered when solutions to improve voltage regulation, increase system stability and enhance power factor are discussed.

3.1 Introduction

Power systems are subjected to load fluctuations and transients that cause voltage values to deviate from their nominal levels. In order to keep the system within safe operating limits, voltage levels should be controlled by managing the supply or absorption of reactive power in selected buses of the AC network. This reactive power management also known as VAR compensation addresses one of the most important system issues; power quality.

Power quality has different faces and can be addressed using adequate VAR control devices [01]. In general, VAR compensation is also directly translated to voltage support that is required to minimize voltage fluctuations or provide flicker control at a given location. VAR compensation improves system stability and controls power factor resulting in a maximum active power transfer to the load. VAR compensation is also used to follow seasonal or more transient load profiles and to control over-voltages in some radial segments of the AC network [02] which, in turn, protects equipment and prevents cascading faults and blackouts [03].

Before the advances in power electronic switches such as thyristors and IGBTs, reactive power compensation has been achieved using over-excited synchronous machines without mechanical load also known as synchronous condensers for continuous voltage regulation and fixed or switched reactors for discrete voltage regulation. As thyristor switches became commercially available and microcomputers provided sufficient computational power, automatic VAR regulators using controlled or switched reactors and switched capacitors known as SVCs were introduced to provide VAR compensation on any desired range of power. An SVC with controlled reactor provides continuous reactive power control and imitates the behavior of a synchronous condenser with faster response time, fewer losses, and reduced maintenance [04]. An SVC requires synchronizing voltages for its thyristor switches to commutate which limits the device contribution on reactive power during deep voltage collapses. This limitation was removed with the introduction of the self-commutated PWM converters knows also as voltage source converters. Using an appropriate control scheme, a voltage source converter combined with a capacitor bank allows the realization of a device capable of synthesizing a voltage that is controlled in both amplitude and phase and permits the generating or absorbing of reactive current with a subcycle speed [05]. This device is called Static Synchronous Compensator or SVC-Light®. Because, an SVC-Light® is based on a voltage source

converter it can operate at voltages lower than the normal voltage regulation range and can generate more reactive power than an equally rated SVC.

In this chapter, descriptions of a switched capacitor, a switched reactor, a synchronous condenser, an SVC, and an SVC-Light® are provided. A comparison of SVC and SVC-Light® characteristics is also reported.

3.2 Structure of this chapter

The introduction and structure of this chapter are provided in sections 3.1 and 3.2 respectively while section 3.3 discusses voltage regulation using shunt capacitors and shunt reactors. Synchronous condensers application in reactive power control is reported in section 3.4. SVC and SVC-Light® descriptions and characteristics are reported in sections 3.5 and 3.6 respectively. Finally, sections 3.7 and 3.8 provide, respectively, a conclusion and a list of references.

3.3 Shunt capacitor and shunt reactor

The general use of switched reactor is to control line voltages during line tripping or load shedding. Initially, the use of shunt reactors employed low cost switches and circuit breakers to control slow electrical events that can be coordinated in advance. Figure 3-1 shows an inductor and a capacitor connected to an AC bus through mechanical switches.

With the advances in power electronic switches, thyristor switched shunt reactors started to play more roles on dynamic voltage regulation and transient control either in standalone applications or in combination with shunt capacitors. Shunt capacitors are used in the same way as shunt reactors. But, because a capacitor draws a leading current it has been used to compensate for inductive loads such as induction motors in order to correct the power factor and optimize real power transfer. The first use of shunt capacitors for power factor correction was in 1914 [06]. The rating of a shunt capacitor is a function of the inductive load and the desired power factor correction. For a widely fluctuating load, a fixed capacitor bank does not provide an optimal solution since it may lead to either over or under compensation. Therefore, incremental switching of capacitor banks is used to cope with slow load variations [07]. Capacitor banks are switched into or switched out of the AC system using circuit breakers and relays. Some switching synchronization is needed to avoid high inrush currents that can damage the contacts of the switching apparatus [06].

To illustrate the principle of reactive power compensation using shunt elements I consider the circuit of Figure 3-2 where a source is feeding an inductive load. In Figure 3-2.a the system is uncompensated and the source is delivering both active and reactive power to the load. This delivery of the non useful reactive current causes an extra stress to the source and produces losses in the AC lines. By adding a capacitor near the load that will supply the needed reactive power, the

reactive current coming from the source is reduced or eliminated and only active power is transmitted on the line as shown in Figure 3-2.b. Reducing or eliminating the transfer of reactive power back and forth between loads and sources can also help with voltage and thermal stability.

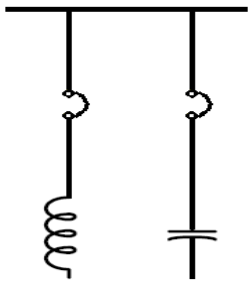

Figure 3-1: Mechanically switched inductor and capacitor

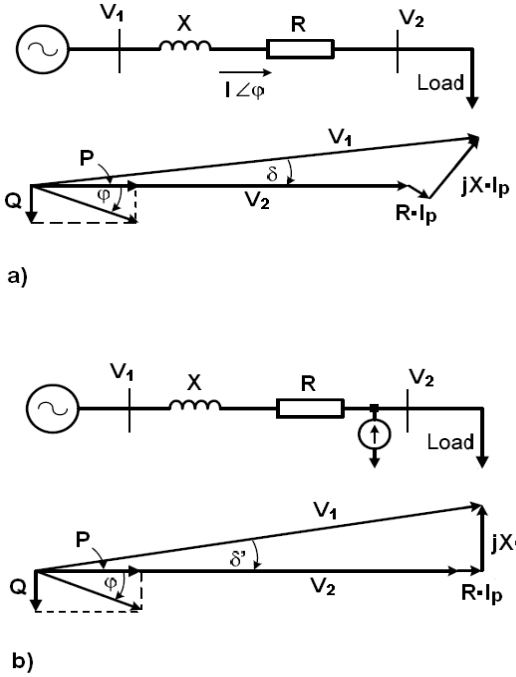

Figure 3-2: Compensation of a simple AC system

3.4 Synchronous condensers

Synchronous machines used as motors are known to load the power line with leading power factors; a feature that was proven useful in canceling out lagging power factors caused by induction motors and inductive loads. Originally, large industrial synchronous motors came into wide use because of this ability to correct the lagging power factors of induction motors. This leading power factor can be exaggerated by removing the mechanical load and over exciting the field of the synchronous motor. Such a device is known as a synchronous condenser.

Synchronous condensers have been used in voltage and reactive power control for more than 50 years. The control of generation or absorption of reactive power is performed by adjusting the field current of the synchronous machine.

When used with the appropriate exciter circuit, a synchronous machine can provide continuous and smooth reactive power control and help maintain voltage stability for both distribution and transmission systems. The voltage stability is achieved by maintaining the voltage levels within desired ranges under varying load conditions or contingency situations.

The disadvantage from using a synchronous condenser comes from the huge foundation work and the specialized equipment needed to start and protect the machine. Other considerations related to machine response time that is inadequate to deal with fast transients or rapid load variations should also be made. Besides, a

synchronous condenser has bigger installed cost per MVA and generates more losses than an equivalent SVC but it has a good overload capability [01] that surpasses that of an SVC and an SVC-Light® alike.

3.5 SVC

The SVC is a shunt device of the Flexible AC Transmission Systems (FACTS) family using power electronics to control power flow and improve transient stability on power grids. The SVC regulates voltage at its terminals by controlling the amount of reactive power injected into or absorbed from the power system. When system voltage is low, the SVC generates reactive power by presenting capacitive impedance to the AC bus. When system voltage is high, it absorbs reactive power by presenting inductive impedance to the AC bus. The variation of reactive power is performed by switching capacitor and inductor banks connected on the secondary side of a coupling transformer. Each capacitor bank is switched on and OFF by thyristor switches. Reactors can be operated in two modes; either switched ON and OFF or phase-controlled. The advantage of controlled reactor is the ability to continuously regulate the system voltage. However, a controlled reactor generates more harmonics than a switched one. An SVC can contain any number of switched and controlled reactors in combination with any number of switched capacitors. A

single-line diagram of a simple static VAR compensator and its control system is shown in Figure 3-3.

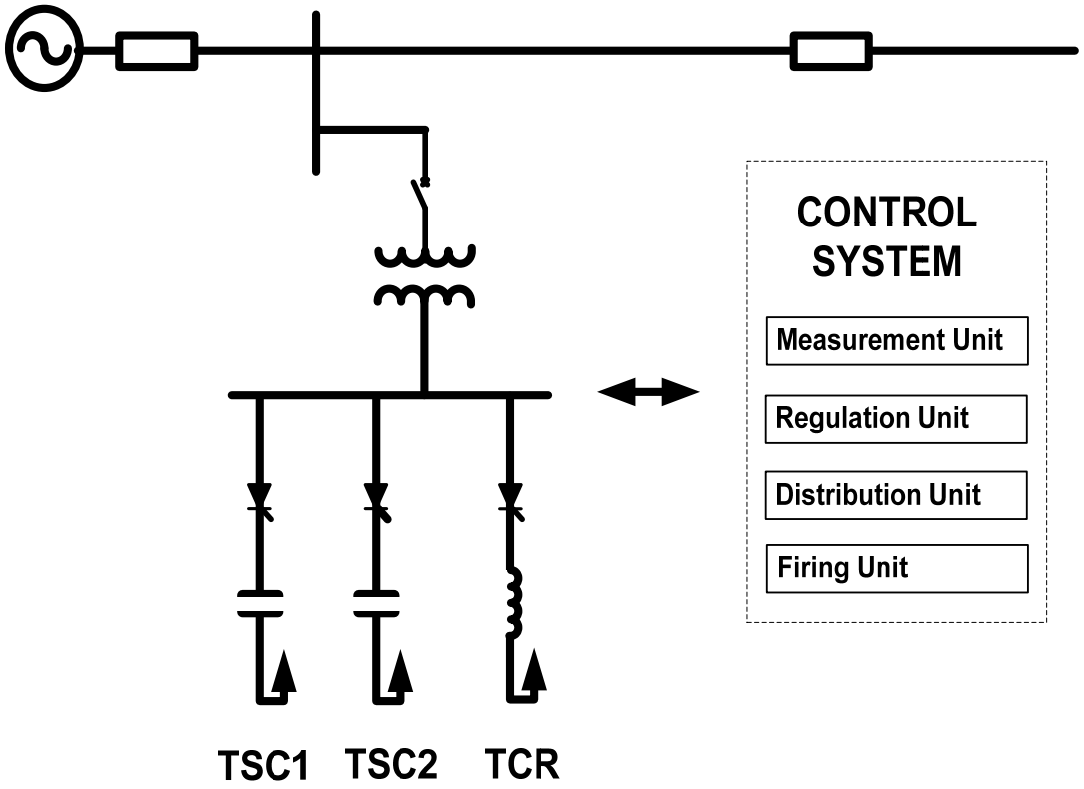

Figure 3-3: A simple SVC with its control system

The control system of an SVC consists of three major units:

- A measurement unit evaluating the positive-sequence voltage to be controlled. There are many ways of extracting the positive sequence out of the measured signals but the most used method consists of a Fourier analysis using a one-cycle running average window.

- A voltage regulation unit that uses the voltage error defined as the difference between the measured voltage and the desired or reference voltage to determine the SVC reactive power output needed to keep the system voltage constant. The output of the SVC is called the susceptance and denoted mostly by the letter B. In most industrial SVCs, the regulator gains are adaptive and depend on the network short circuit level. The method of adapting the gain as function of the strength of the network is also called gain scheduling and has the merit to optimize the SVC step response without causing voltage overshoots or system instabilities.
- A distribution unit that is based on the amount of required reactive power output determines the required combination of capacitor and reactor banks to connect. For a switched capacitor and inductor banks SVC, the number of branches and their sizes determine how small the SVC control steps will be. For an SVC using controlled reactor, the distribution unit calculates the number of capacitor banks that results in a minimum firing angle α for the reactor branch. Because a small α generates less harmonics and is the desired way of operation.

3.5.1 V-I characteristic of an SVC

The SVC can be operated in voltage regulation mode or in reactive power control mode. When the SVC is operated in voltage regulation mode, it implements a V-I characteristic as shown in Figure 3-4.

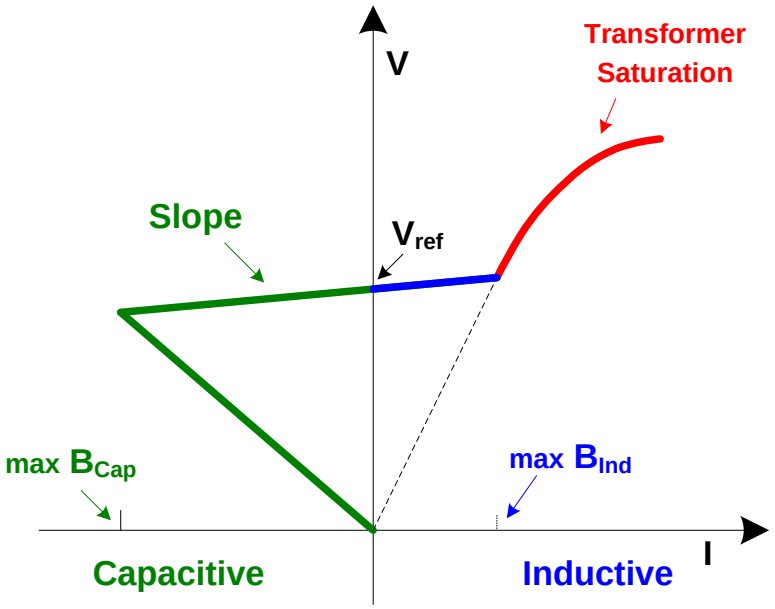

Figure 3-4: V-I characteristic of an SVC

The output of the SVC is calculated based on the difference between the measured AC voltage and the desired or reference voltage. The output or susceptance B of the SVC is, however, limited by the installed capacitor and reactor banks and these installed values are not required to be identical. The installed capacity determines two boundaries defining the maximum values B can take. These two values are maximum capacitive (max B_{cap}) and maximum inductive (max B_{Ind}) as shown in Figure 3-4.

As long as the SVC susceptance B stays within the maximum and minimum susceptance values imposed by the total reactive power of installed capacitor and

reactor banks, the voltage is regulated at the reference voltage V_{ref}. In practice, a voltage droop between 1% and 4% is used to ensure stable behavior of the SVC especially in presence of other voltage control devices acting on the same network.

When the voltage at the AC bus is lower than the desired value, a capacitive current is produced by the SVC. As indicated by the green color in Figure 3-4, the capacitive current is also function of the voltage and drops as the voltage drops rendering the SVC ineffective at very low voltage levels.

When the voltage at the AC bus is higher than the desired value, an inductive current is presented by the SVC shown in blue in the V-I characteristic. The SVC can only output a limited value of inductive current beyond which a higher AC voltage will cause the connecting transformer to saturate as shown with red color in V-I characteristic.

The time response of an SVC to system voltage changes depends on the voltage regulator gains, the droop reactance, and the system strength. In practice, a lookup table is used for gain scheduling based on online measurement of the short circuit level of the system. The table is calculated in advance for different values of network impedance covering plausible system contingencies.

3.6 SVC-Light®

The SVC-Light® is a shunt device of the Flexible AC Transmission Systems (FACTS) family using power electronics to control power flow and improve transient stability on power grids. The SVC-Light® regulates voltage at its terminal by controlling the amount of reactive power injected into or absorbed from the power system. When system voltage is low, the SVC-Light® generates reactive power (SVC-Light® capacitive). When system voltage is high, it absorbs reactive power (SVC-Light® inductive).

The variation of reactive power is performed by means of a Voltage Source Converter (VSC) connected on the secondary side of a coupling transformer. The VSC uses forced-commutated power electronic devices to synthesize a voltage controlled in amplitude from a DC voltage source. The principle of operation of the SVC-Light® is depicted in Figure 3-5 that shows the active and reactive power transfer between a source V_1 and a source V_2. In the figure, V_1 represents the system voltage to be controlled and V_2 is the voltage generated by the VSC.

In steady state operation, the voltage V_2 generated by the VSC is in phase with V_1 ($\delta = 0$), so that only reactive power is flowing ($P = 0$). If V_2 is lower than V_1, Q is

flowing from V_1 to V2 (SVC-Light® is absorbing reactive power). On the contrary, if V_2 is higher than V_1, Q is flowing from V_2 to V_1 (SVC-Light® is generating reactive power). The amount of reactive power is given by Q.

A capacitor connected on the DC side of the VSC acts as a DC voltage source. In steady state the voltage V_2 has to be phase shifted slightly behind V_1 in order to compensate for transformer and VSC losses and to keep the capacitor charged.

VSC technologies use Pulse-Width Modulation (PWM) techniques to synthesize a sinusoidal waveform from a DC voltage source with a typical chopping frequency of a few kilohertz. Harmonic voltages are cancelled by connecting filters at the AC side of the VSC. This type of VSC uses a fixed DC voltage Vdc. Voltage V_2 is varied by changing the modulation index of the PWM modulator.

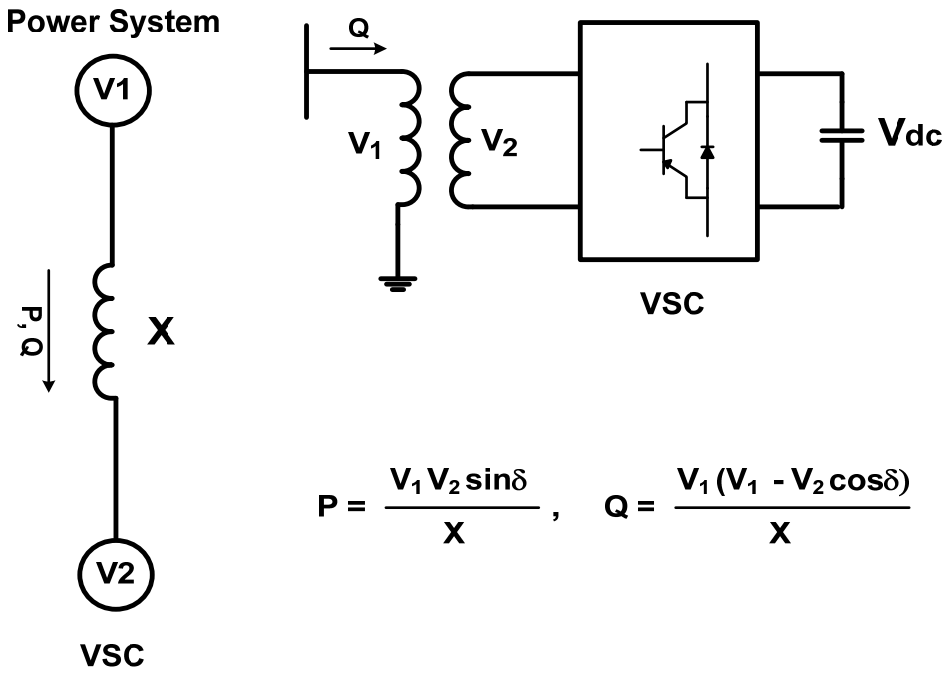

Figure 3-5: Operating principle of an SVC-Light®

3.6.1 V-I characteristic of an SVC-Light®

The SVC-Light® can be operated in voltage regulation mode or in reactive power control mode. When the SVC-Light® is operated in voltage regulation mode, it implements a V-I characteristic as shown in Figure 3-6.

As long as the reactive current stays within the minimum and maximum current values (-Imax, +Imax) imposed by the converter rating, the voltage is regulated at the reference voltage. In practice a droop between 1% and 4% is used to ensure a stable operation of the control.

The SVC-Light® performs the same functions as the SVC. However, at voltages lower voltage levels, the SVC-Light® can generate more reactive power than the SVC. This is due to the fact that the maximum capacitive power generated by an SVC is proportional to the square of the system voltage (constant susceptance) while the maximum capacitive power generated by an SVC-Light® decreases linearly with voltage (constant current). This ability to provide more capacitive reactive power during a fault is one important advantage of the SVC-Light® over the SVC. In addition, the SVC-Light® will normally exhibit a faster response than the SVC because the SVC-Light® has no delays associated with the thyristor firing.

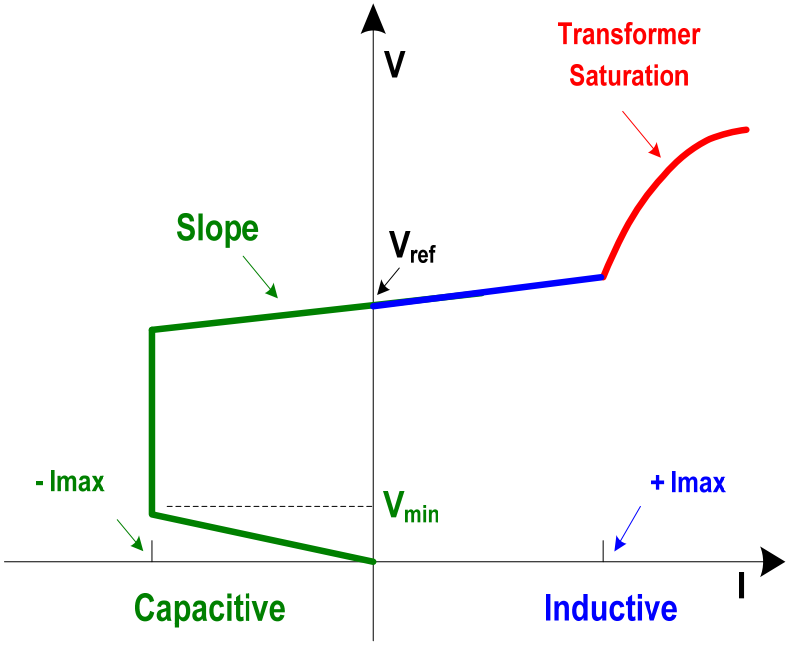

Figure 3-6: V-I characteristic of an SVC-Light®

3.7 Conclusion

A simple description of reactive power compensator devices has been presented to illustrate their principles of operation, their merits as well as their limitations. Starting from the need to regulate a voltage at an AC bus, classical solutions using simple shunt capacitors and reactors were first employed. These solutions using relays and circuit breakers exhibited sluggish performance and needed extensive maintenance efforts. The introduction of power electronic switches such as thyristor valves propelled the use of passive capacitor and reactor banks to a more dynamic

dimension where voltage regulation is performed within a cycle of the system frequency.

The development of voltage source converter based on IGBT switches introduced dramatic improvement to the concept of reactive power compensation. Characterized by a subcycle dynamic response, zero inertia, no contribution to the short-circuit current, and the ability to control many variables, VSC became the center element of the advanced FACTS devices for series and shunt applications. Installed projects of FACTS devices using voltage source converter technology saw great success in improving power system performance, increasing reliability and power quality.

These VAR compensators will be used on a wider scale as demands for grid performance and reliability become an even more important factor. These devices provide better grid controllability that permits a safe utilization of the system assets close to their physical limits without causing stability problems and in case of contingencies help the system with a fast and controlled recovery.

3.8 References

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CHAPTER 4 OVERVIEW OF HVDC TECHNOLOGIES

In this chapter, I conduct a background research on HVDC and HVDC-Light® in order to assess the state of the art of the technology and its application. I provide detailed description and comparison of current source converter and voltage source converter based-HVDC systems and I survey possible applications and their relative impacts on the power grid. I deemed important to introduce this material to the

reader because HVDC technology plays a big role on the solution I propose to solve power grid problems.

4.1 Introduction

The term HVDC stands for High Voltage Direct Current and is today a well proven technology employed for power transmission all over the world. The method is very flexible and can be used to transfer electrical power over long distances using overhead lines or under water cables.

Two converter stations are to be used: one rectifier and one inverter. Electrical power is taken from one point in an AC network and converted to DC with the help of the rectifier station. The DC power is transmitted by overhead lines or by submarine cables, converted back to AC power at the inverter station and finally injected into the receiving AC network.

The final decision to choose HVDC instead of conventional AC transmissions depends on a number of factors and the main reason often changes between different projects. Some advantages with HVDC compared to HVAC are the following:

- The controllability of the power flow will increase. Both the power direction and the power level can be controlled very accurately and rapidly.

- HVDC transmission lines have lower losses than AC lines for the same power capacity. The losses in the converter stations have of course to be added, but above a certain break-even distance, the total HVDC transmission losses become lower than the AC losses. HVDC cables also have lower losses than AC cables.
- For long submarine cable links HVDC is the only possible technical solution.
- When connecting two asynchronous AC networks together, a HVDC link has to be implemented.

Two types of technologies are actually used for HVDC applications: one is using current source inverters and is known as HVDC classic and the other is using voltage source inverters and is known as HVDC-Light®. These two technologies are described in the following sections.

4.2 Structure of this chapter

The introduction and outline of this chapter are reported in sections 4.1 and 4.2 respectively. The technology of HVDC classic using thyristor valves is described in section 4.3. The VSC based HVDC known as HVDC-Light® technology is discussed in section 4.4. The two converter topologies used to build VSCs for high voltage applications, their control philosophies, and protection mechanisms are reported in subsections 4.4.1.

Some of the HVDC applications reported in section 4.5 include asynchronous systems in section 4.5.1, system congestion and bottlenecks in section 4.5.2, flicker control in 4.5.3, loop flow elimination in section 4.5.4, managing unbalanced loads in 4.5.5, improving system voltage stability in 4.5.6, and damping power oscillations in 4.5.7. Most of the reported applications can be achieved by HVDC classic or HVDC-Light® with different degrees of performance. In presence of nearby generations, the potential of subsynchronous oscillations or subsynchronous torsional interactions caused by HVDC converters is discussed in section 4.6. The conclusion of this chapter and a list of references are provided in sections 4.7 and 4.8 respectively.

4.3 HVDC classic

The conventional HVDC transmission is called HVDC Classic and is based on a current source converter (CSC), which is a line-commutating converter. The valves in the converter are made out of several thyristors connected in series and parallel configuration. The valves are then connected in so called Graetz bridge modules, as shown in Figure 4-1. In the figure, phase to ground voltages are identified as V_a, V_b, and V_c. The transformer is represented by its leakage reactor X and the thyristor switches are tagged T_1 through T_6. The thyristors conduct in pairs as (T_1-T_2), (T_3-T_4),

and (T_5 - T_6) with overlap conduction between adjacent legs during current commutation. The output of the bridge is a DC current I_d, and a DC voltage U_d.

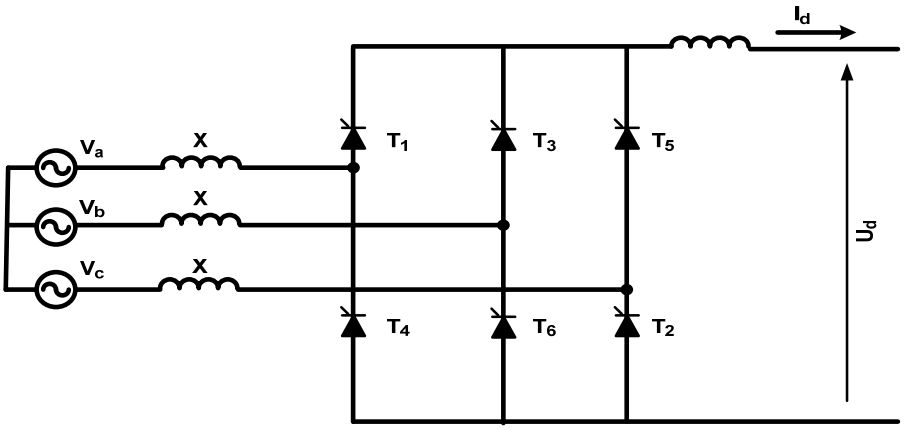

Figure 4-1: Simplified 6-pulse converter bridge

A 12-pulse converter bridge can then be built by connecting two 6-pulse bridges in series. The bridges are then connected separately to the AC system by means of converter transformers, one of Y-Y winding structure and another of Y-Δ winding structure, as shown previously in Figure 4-2.

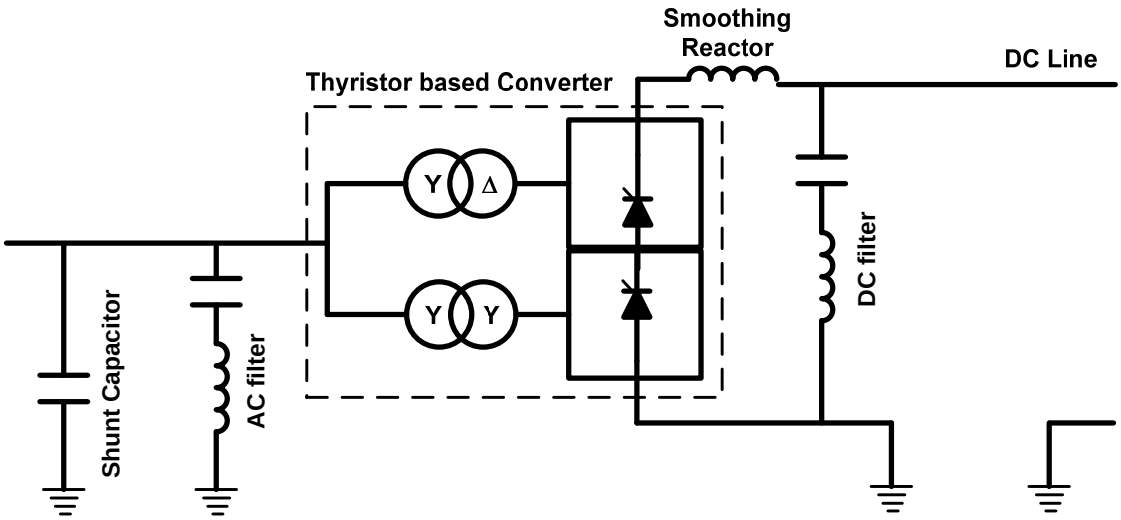

Figure 4-2: Simplified 12-pulse converter bridge

Regarding operation and control of an HVDC link, two basic methods for generating gate pulses are discussed below:

1. Individual phase control (IPC): used in early HVDC projects. The main feature of this scheme is that the firing pulse generation for each phase (or valve) is independent of each other and the firing pulses are rigidly synchronized with the commutation voltages. The major drawback of IPC scheme is the aggravation of harmonic stability problem, characterized by magnification of non-characteristic harmonics in steady state.

2. Equidistant pulse control (EPC): In this scheme, the firing pulses are generated in steady state at equal intervals of 1/pF, where p is the number of pulses and

F is the fundamental frequency. There are three variations of the EPC scheme; pulse frequency control (PFC), pulse period control, and pulse phase control (PPC).

Although EPC scheme has replaced IPC scheme in modern HVDC projects, it has certain limitations. The first drawback is that under unbalanced voltage conditions, EPC results in less DC voltage compared to IPC. EPC scheme also results in higher negative damping contribution to torsional oscillations, and it has more impact when HVDC is the major transmission link from a thermal station.

4.4 HVDC-Light®

VSC based HVDC (HVDC-Light®) is the latest technology to transfer power by means of direct current. The first project using Light technology with insulated gate bipolar transistors (IGBT) was a 10 km long test transmission link between Hellsjon and Grengesberg, located in the central part of Sweden. The project transmitted 3 MW and was commissioned in March 1997. HVDC-Light® is based on VSC, which is a self-commutating converter. The valves are made out of devices using modules of IGBT switches with anti-parallel connected diodes. The method uses pulse width modulation (PWM) with a very high switching frequency. The development of HVDC-Light® technology within ABB is being made in different stages, which are called generations. The first generation using forced commutation was called generation A

and uses a two-level bridge configuration while the second generation (generation B) uses a three-level bridge configuration.

4.4.1 Control and protection

Hardware and software have gone hand in hand in development. The hardware has gone from vacuum tubes to transistors to integrated analogue circuits to integrated digital circuits to single board multiprocessor computers, and always at higher and higher clock speeds. This development has permitted the implementation of more and more functions into the control, and the performing of more of them digitally. At present, all functions in a HVDC converter station are performed digitally, including the most demanding ones, such as current control and the active filter control. An additional feature that the development has made possible and practical to achieve is full redundancy in control as well as in protection systems. To further increase the reliability and availability of the control systems as such, the self-diagnosing capabilities have increased dramatically, and even extended to the supervision of incoming signals, comparing them continuously against acceptability windows that are in turn updated by the prevailing conditions. The development has also touched the intra-station communication between different pieces of equipment; it is no longer the obvious answer to use hardwire signals (current, voltage, status) all the way to control rooms or through control islands; instead, the signals are converted to

digital as close as possible to the source, and transmitted digitally, through optical fibers to the control room.

The principles given above not only eliminate interference from the switchyard into the control building; they also permit an extremely high degree of integration of the different protection, control and monitoring functions. At present, full integration makes it possible to comprise not only the converter control, but the DC and AC sides as well, with, for example, transformer protection, tap changer control, reactive power control, transient fault recording, sequence of events recording, etc. The integration allows a much higher degree of utilization of the main circuit equipment capabilities.

With the appearance of high switching frequency components, such as IGBTs it becomes advantageous to build VSC using PWM technology. The AC voltage is created by very fast switching between two fixed voltages. The desired fundamental frequency voltage is created through low pass filtering of the high frequency pulse modulated voltage.

In HVDC-Light®, PWM is used for generation of the fundamental voltage. Using PWM, the magnitude and phase of the voltage can be controlled freely and almost instantaneously within certain limits. This allows independent and very fast control of active and reactive power flows. From a system point of view, VSC acts as a zero-inertia motor or generator that can control active and reactive power almost

instantaneously. Furthermore, it does not contribute to the short circuit power, as the AC current can be controlled.

As a consequence, no reactive power compensation equipment is needed at the station, and only an AC filter is installed. The HVDC-Light® reactive power controller can automatically control the voltage in the AC network, without influencing the control of active power. In power supply applications, the active power is often controlled to match a set-point. Reactive power generation and consumption of a HVDC-Light® converter can be used for compensating the needs of the connected network within the rating of a converter. As the rating of the converters is based on maximum currents and voltages, the reactive power capabilities of a converter can be traded against the active power capability.

The voltage control of a station constitutes an outer feedback loop and generates a reactive current demand signal in such a way as to maintain the set voltage on the network bus. Because of the short response time of the system for AC voltage control, the AC bus voltage can be kept constant during transients and other disturbances. Flicker is also mitigated to a higher degree. It is thus possible to use the controllability of HVDC-Light® to stabilize the voltage in fault situations.

An interesting feature of VSC is its ability to supply a passive network having no generation components. When supplying a passive network, the static converter

controls the amplitude and frequency of the AC voltage. Such a function can be of importance even if the HVDC-Light® system is connected to an active AC network, as it may become islanded and passive as a result of system faults. An island situation in an AC system can occur if a nearby AC breaker trips due to a fault. The HVDC-Light® system can be programmed to switch from active power regulation to frequency control following a breaker opening or in presence of frequency deviation. This makes HVDC-Light® very useful for transmission of electrical power to offshore platforms. HVDC-Light® can also be used for multiterminal operation, thus connecting together various platforms with one transmission link.

4.5 HVDC applications

HVDC and HVDC-Light® systems are applied to transfer power over long distances, integrate wind farms to the grid, connect asynchronous systems, solve loop flow problems, damp power oscillations, and help with voltage stability concerns. Some applications are better done with HVDC-Light® due to its use of VSCs and PWM techniques. Such applications include flicker control, offshore power connection, and multiterminal systems using a common DC bus. In the following sections, I will concentrate on HVDC-Light® applications and discuss the contribution it brings to the power grid.

4.5.1 Asynchronous systems connection

The interconnected AC networks that tie the power generation plants to the consumers are in most cases large. Even when these networks operate at the same nominal frequency, there are always some variations that may complicate or make an AC connection between these networks impossible.

An AC tie between two asynchronous systems needs to be very strong to not get overloaded. If a stable AC tie would be too large for economical power exchange needs, or if the networks wish to retain their independence, than a HVDC link is the solution. In some parts of the world (South America and Japan) 50 and 60 Hz networks are bordering each other and it would be impossible to exchange power between them using AC lines or cables. A HVDC link is then the only alternative.

4.5.2 Bottlenecks

The term Bottleneck is often interchangeable to congested transmission paths or interfaces. A transmission path or interface refers to a specific set of transmission elements between two neighboring control areas or utility systems in an interconnected electrical system. A transmission path or interface becomes congested when the allowed power transfer capability is reached under normal operating conditions or as a result of equipment failures and system disturbance conditions. The key impact of Bottlenecks is the reduction of system reliability; the

inefficient utilization of transmission capacity and generation resources, and the restriction of healthy market competition. The ability of transmission systems to deliver the energy is dependent on several factors that are limiting the system, including thermal constraints, voltage constraints, and stability constraints. These transmission limitations are usually determined by performing detailed power flow and stability studies for a range of anticipated system operating conditions. Thermal limitations are the most common constraints, as warming and consequently sagging of lines is caused by the current flowing in the wires of the lines and other equipment. In some situations, the effective transfer capability of transmission path or interface may have to be reduced from the calculated thermal limit to a level imposed by voltage constraints or stability constraints.

Bottlenecks may be relieved by the use of a HVDC or a HVDC-Light® link in parallel with the limiting section of the grid as shown in Figure 4-3. By using the inherent controllability of the HVDC system, the power system operator can decide the amount of power to be transmitted by the HVDC system and consequently that to be transmitted by the AC link.

Longer AC lines tend to have stability constrained capacity limitations as opposed to the higher thermal constraints of shorter lines. By using the inherent controllability of a HVDC system in parallel with the long AC lines, the power system can be stabilized and the transmission limitations on the AC line can be relaxed.

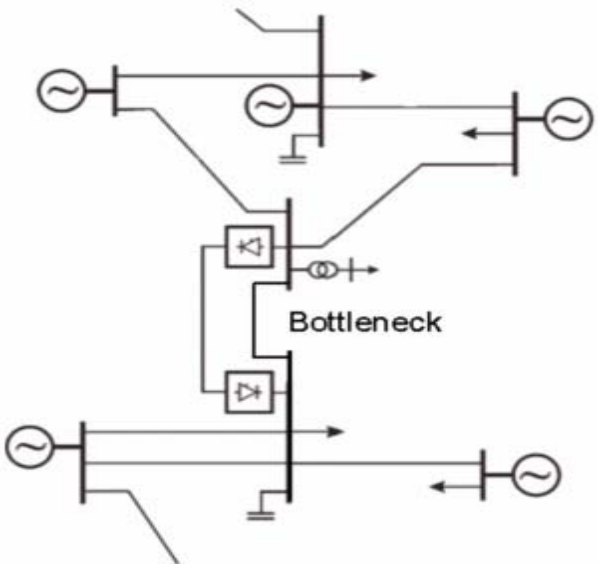

Figure 4-3: HVDC-Light® in parallel with an AC line

4.5.3 Flicker control

Voltage Flicker can either be a periodic or aperiodic fluctuation in voltage magnitude i.e. the fluctuation may occur continuously at regular intervals or only on occasions. Voltage Flicker is normally a problem with human perception of lamp strobing effect but can also affect power processing equipment such as UPS systems and power electronic devices. Slowly fluctuating periodic flickers, in the 0.5 to 30 Hz range, are considered to be noticeable by humans. A voltage magnitude variation of as little as 1.0% may also be noticeable.

The main sources of flicker are industrial loads exhibiting continuous and rapid variations in the load current magnitude. This type of loads includes Electric Arc Furnace (EAF) in the steel industry, welding machines, large induction motors, and

wind power generators. High impedance in a power delivery system will contribute further to the voltage drop created by the line current variation.

A HVDC-Light® working as a SVC-Light® is an effective method to address the problem of flicker. The unbalanced, erratic nature of an EAF causes significant fluctuating reactive power demand, which ultimately results in irritating electric lamp flicker to neighboring utility customers. In order to stabilize voltage and reduce disturbing flicker successfully, it is necessary to continuously measure and compensate rapid changes by means of extremely fast reactive power compensation. SVC-Light® uses voltage source converters to improve furnace productivity similar to a traditional SVC while offering superior voltage flicker mitigation due to fast response time.

4.5.4 Loop flow

The terms Loop Flow and Parallel Path Flow are sometimes used interchangeable to refer to the unscheduled power flows, that is, the difference between the scheduled and actual power flows, on a given transmission path in an interconnected electrical system.

Unscheduled power flows on transmission lines or facilities may result in a violation of reliability criteria and decrease available transfer capability between neighboring control areas or utility systems.

The reliability of an interconnected electrical system can be characterized by its capability to move electric power from one area to another through all transmission circuits or paths between those areas under specified system conditions. The transfer capability may be affected by the contracted path designated to wholesale power transactions, which assumes that the transacted power would be confined to flow along an artificially specified path through the involved transmission systems. In reality, the actual path taken by a transaction may be quite different from the designated routes, determined by physical laws not by commercial agreements, thus involving the use of transmission facilities outside the contracted systems. These unexpected flow patterns may cause so-called Loop Flow and Parallel Path Flow problems, which may limit the amount of power these other systems can transfer for their own purposes.

4.5.5 Unbalanced load

An unbalanced load is a load which does not draw balanced current from a balanced three-phase supply. Typical unbalanced loads are loads which are connected phase to neutral and also loads which are connected phase to phase. Such loads are not capable of drawing balanced three-phase currents. They are usually termed single-phase loads.

A single-phase load, since it does not draw a balanced three-phase current, will create unequal voltage drops across the series impedances of the delivery system. This unequal voltage drop leads to unbalanced voltages at delivery points in the system. Blown fuses on balanced loads such as three-phase motors or capacitor banks will also create unbalanced voltage in the same fashion as the single-phase and phase to phase connected loads. Unbalanced voltage may also arise from impedance imbalances in the circuit that deliver electricity such as untransposed overhead transmission lines. Such imbalances give the appearance of an unbalanced load to generation units.

An unbalanced supply may have a disturbing or even damaging effect on motors, generators, poly-phase converters, and other equipment. The foremost concern with unbalanced voltage is overheating in three-phase induction motors. The percent current imbalance drawn by a motor may be 6 to 10 times the voltage imbalance, creating an increase in losses and in turn an increase in motor temperature. This condition may lead to motor failure.

Modern electric rail system is a major source of unbalanced loads. Electrification of railways, as an economically attractive and environmentally friendly investment in infrastructure, has introduced an unbalanced and heavy distorted load on the three-phase transmission grid. Without compensation, this would result in significant unbalanced voltage affecting most neighboring utility customers. The HVDC-Light®

inverter station can generate voltages to elegantly be used to restore voltage and current balance in the grid, and to mitigate voltage fluctuations generated by the traction loads.

4.5.6 Voltage instability

Voltage instability is basically caused by an unavailability of reactive power support in an area of the network, where the voltage drops uncontrollably. Lack of reactive power may essentially have two origins: firstly, a gradual increase of power demands without the reactive part being met in some buses or secondly, a sudden change in the network topology redirecting the power flows in such a way that the required reactive power cannot be delivered to some buses.

The relation between the active power consumed in the considered area and the corresponding voltage is expressed in a static way by the P-V curve (also called “nose” curve) as shown in Figure 4-4. The increased values of loading are accompanied by a decrease in voltage (except in case of a capacitive load). When the loading is further increased, the maximum loadability point is reached, beyond which no additional power can be transmitted to the load under those conditions. In case of constant power loads, the voltage in the node becomes uncontrollable and decreases rapidly. This may lead to the partial or complete collapse of a power system.

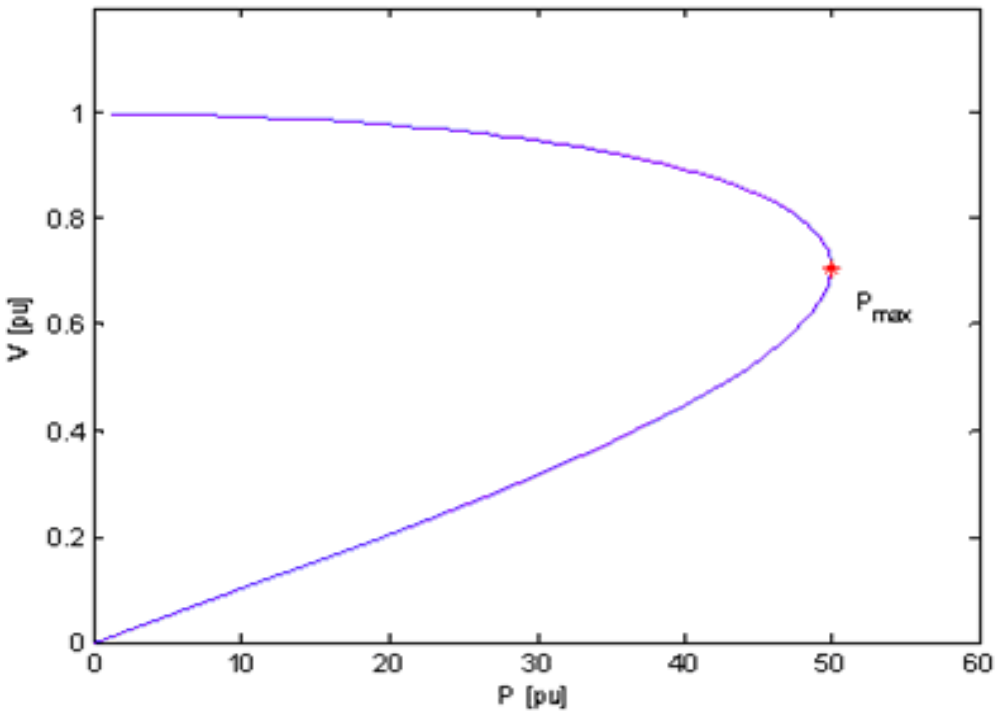

Figure 4-4: PV curve

HVDC-Light®, when connected to the grid, can provide dynamic voltage support in response to system disturbances and balance the reactive power demand of large and fluctuating industrial loads. A HVDC-Light® is capable of both generating and absorbing variable reactive power continuously as opposed to discrete values of fixed and switched shunt capacitors or reactors. With continuously variable reactive power supply, the voltage at the bus may be maintained smoothly over a wide range of system operating conditions. This entails the reduction of network losses and provision of sufficient power quality to the electric energy end-users.

4.5.7 Power oscillations

Oscillations of generator angle or line angle are generally associated with transmission system disturbances and can occur due to step changes in load, sudden change of generator output, transmission line switching, and short circuits. Depending on the characteristics of the power system, the oscillations may last from 3 to 20 seconds after a severe fault. During such angular oscillation period significant variations in voltages, currents, and power flows will take place. It is important to damp these oscillations as quickly as possible because they cause many power quality problems as well as mechanical wear in power plants. The system is also more vulnerable if further disturbances occur.

The active power oscillations on a transmission line tend to limit the amount of power that may be transferred; this may result in stability concerns or utilization restrictions on the corridors between control areas or utility systems. This is due to the fact that higher power transfer can lead to less damping and thus more severe and possibly unstable oscillations.

The HVDC damping controller is a standard feature in many HVDC projects in operation. It normally takes its input from the phase angle difference in the two converter stations. Figure 4-5 from ABB website shows a comparison of power oscillation damping using different control strategies with HVDC-Light®.

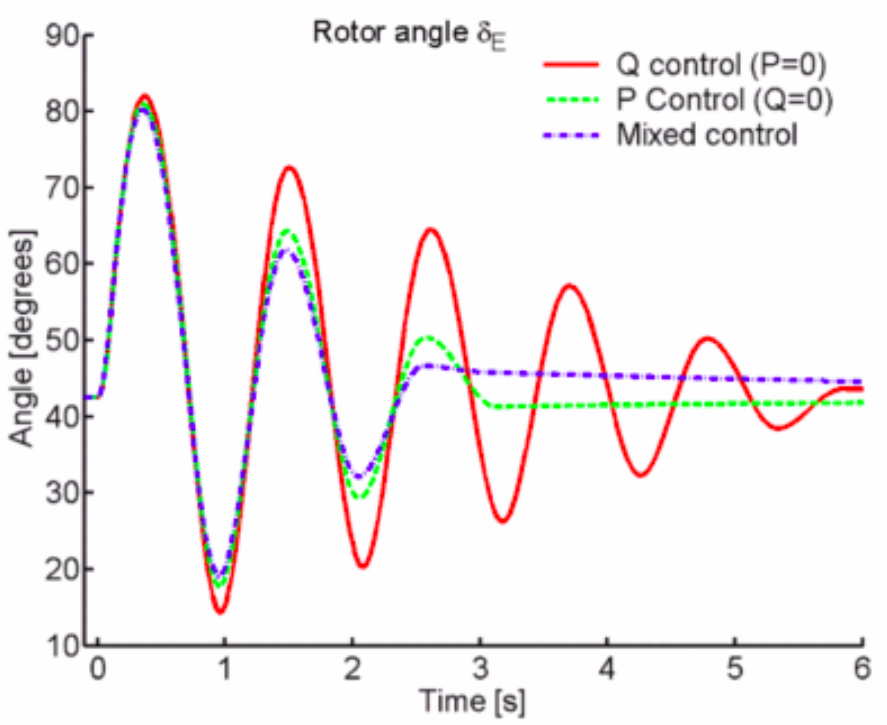

Figure 4-5: Power oscillation damping using HVDC-Light®

4.6 Subsynchronous torsional interactions

Subsynchronous Torsional Interactions (SSTI) occurs when the induced subsynchronous torque in the generator is close to one of the torsional natural modes of the turbine-generator shaft. When this happens, generator rotor oscillations will build up and this motion will induce armature voltage components at subsynchronous frequencies. Moreover, the phase of this induced subsynchronous frequency voltage is such that it sustains the subsynchronous torque. If this torque equals or exceeds the inherent mechanical damping of the rotating system, the

system will become self-excited. This phenomenon is called torsional interaction and occurs in the frequency range of 10 to 40 Hz.

The most common example of the natural mode subsynchronous oscillation is found in networks that include series capacitor compensated transmission lines or at the rectifier side of a HVDC transmission link. When connecting the rectifier side of a HVDC transmission link to an AC network with a turbo generator, the rectifier contributes with negative damping in the subsynchronous frequency range. Depending on the AC network configuration, this may increase the risk of SSTI in the generator system.

Hydro generator systems are not SSTI sensitive when connected to a HVDC transmission link. This is due to the fact that the mechanical damping for possible subsynchronous torsional frequencies is considerably high, and also because the natural torsion frequencies are at higher frequencies compared with thermal generators.

The first experience of HVDC interaction with turbine-generator torsional vibration occurred at Square Butte Electric Coop Project in North Dakota in 1977, where tests had been planned to determine the impact of a special power modulation control applied to the HVDC terminal on turbine-generator torsional vibrations at the adjacent unit. The tests showed that the relatively high gain power modulation control did indeed destabilize the first torsional mode of vibration at 11.5 Hz. Field

modifications were made initially, which allowed operation under limited conditions. These modifications were immediately followed by an analysis of the interaction, which led to further control system modifications that allowed stable operation under all but extreme system contingencies. Thus, there are some applications for which supplementary damping controls for HVDC converters are essential to ensure a net positive damping contribution to torsional modes of vibration for all turbine-generator units in the vicinity of the HVDC system.

The interaction between turbine-generator shaft vibrations and HVDC systems consists of four basic transfer functions:

- From generator shaft speed to DC current independent of HVDC control action
- From the DC current regulator output to generator shaft torque independent of shaft speed
- The DC current regulator and HVDC system
- From generator shaft speed to torque independent of HVDC control action

There are three primary mechanisms involved in the first and last transfer functions, i.e., from generator shaft speed to HVDC current and generator electrical torque. The first one involves the change in AC voltage magnitude due to a change in generator shaft speed. This arises from the speed voltage effect of an electrical machine with constant flux linkages. As shown in [14], this effect has primary

influence over the interaction at frequencies above 15 to 20 Hz for typical systems with equidistant firing.

The second mechanism involves the change in AC voltage magnitude at the rectifier bus due to a change in generator angle based upon the conventional steady-state AC phasor network solution. This effect is only important at low frequencies and with a moderate parallel AC transmission system. For the case of radial operation, this mechanism has virtually no impact on the torsional interaction.

The third mechanism arises with equidistant firing control and is caused by a change in firing angle due to a shift in the voltage phase of the AC network following a change in generator angle. This mechanism has primary influence over the interaction below 15 to 20 Hz.

4.7 Conclusion

A background research on HVDC and HVDC-Light® was conducted to assess the state of the art of the technology and its applications. Detailed description and comparison of current source converter and voltage source converter based HVDC was provided. A survey of possible applications of HVDC-Light® was also discussed. These applications included transfer of power over long distances, integration of wind farms to power grids, connection of asynchronous systems, solving loop flow problems, damping of power oscillations, and helping with voltage stability issues. I

also noted that some applications are better implemented with HVDC-Light® due to its use of VSC and PWM techniques. Such applications include flicker control, offshore power connection, and multiterminal systems using a common DC buses.

4.8 References

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CHAPTER 5 DC RING TOPOLOGY; A NOVEL SOLUTION FOR MEGA CITY APPLICATIONS

The development of mega cities such as Tokyo, Mumbai, Beijing, Shanghai, Guangzhou, and Dhaka leads to increased load concentration and brings additional challenges to managing power on already strained networks while keeping power available to critical loads. Problems such as power factor regulation, power quality,

voltage stability, increased short circuit level and environmental impact are not easily solved by conventional techniques such as adding parallel lines, shunt capacitors, or new substations. To ensure power availability and redundancy, mega cities are fed from multiple power sources using AC and DC links with AC terminal connections through transformers to city loads. This topology presents risk of cascading failures and total blackout should a problem happen anywhere in the AC network even when a comprehensive protection scheme is deployed.

Techniques using FACTS devices are being applied in some areas to alleviate power management difficulties but the increased rate of cities expansions forces utilities to overrate these FACTS devices or increase their numbers which may results in control coordination problems, power oscillation, subsynchronous resonance, and subsynchronous torsional interaction to nearby generator units.

The most effective solution is obtained when the individual AC systems representing sources and loads are decoupled so a fault in a given zone is not propagated to other zones. This solution can be achieved by a DC system where power sources and loads are connected to the DC bus through voltage source converters. For a mega city, this would be conceived as a DC ring feeding the load and connected to multiple remote and local power sources.

In this chapter, I model and simulate Shanghai power grid and perform a study to characterize short circuit and voltage stability problems. I use system data provided

by ABB corporate research located in China and complement their work [03] by introducing other solution scenarios. Then I present a novel solution based on a DC ring topology using voltage source converters to connect loads and power sources without impacting system short circuit level. Then, I identify the need for a fast protection system that would isolate DC faults without disconnecting sensitive loads, depleting DC bus capacitors, or blocking converter stations.

5.1 Introduction

Mega cities are characterized by heavy concentration of industrial and residential loads with different degrees of power quality requirements. Hospitals, data centers and automated factories are more sensitive to voltage fluctuations and harmonics than other loads. The high concentration of businesses and people in mega cities raises also the question of power availability and security. Therefore, these cities are fed through multiple power paths and from many power sources to ensure redundancy as well as reliability. However, fast increasing loads and their densities augment the short-circuit current to levels that challenge existing circuit breaker ratings and their protection coordination.

Mega city multi-infeed issues are arising in places like Beijing, Shanghai & Guangzhou, already characterized by voltage transient problems caused by millions of air conditioning units, typical heavy loading, and huge short-circuit current levels

[01]~[07]. Moreover, due to limited construction areas and strict environmental requirements, it is inevitable to remove power plants from city centers and import power from remote locations. For example, power imports from outside the city has contributed to two thirds of the whole electricity consumption in Beijing, while short current levels in Shanghai are dangerously reaching 63 kA; the highest current level existing circuit breakers can handle[08]~[10]. These high short-circuit current levels have prevented the expansion of power grids to meet fast increasing loads and demographic development.

In order to resolve power management in mega cities with minimum environmental impacts, underground substations along with high voltage AC cables are introduced into urban areas [06]. Other techniques such as network partition schemes are widely adopted to restrain short-circuit current levels [07]. For example, the 220 kV system of Beijing power grid is divided into East and West subsystems, and that of Shanghai power grid is divided into several subsystems. Other apparatus such as series reactors and fault current limiting devices are also introduced to limit the fault current at levels existing circuit breakers can interrupt.

Unfortunately, such AC based solutions are reaching their capability limits in solving mega city problems and a new approach is required. As most of the mega city problems are related to power quality, system protection, and reliability, the decoupling of the mega city AC network into subnetworks that are easily

manageable constitutes an attractive solution. This can be achieved using a DC distribution or subtransmission system where a DC ring surrounding the city is fed from local and remote power sources. Residential and industrial city loads are then hooked to the DC ring through voltage source converters that will regulate power factor, control power flow and reduce fault current levels.

The successful implementation of such solution is contingent: 1) to the existence of an intelligent network topology that easily connects power supplies to sensitive loads even during faults, 2) to the implementation of a fast protection scheme that isolates faulty segments of the DC system without shutting-OFF any converter station or depleting DC capacitor banks, and 3) to the availability of a DC fault management device or DCCB capable of quickly interrupting DC currents without creating voltage arcs or introducing current oscillations.

The merit of a DC distribution or subtransmission system in increasing voltage stability, reducing short-circuit current levels, and enhancing power quality is analyzed using Shanghai power grid as a testbed. System benefits of other solutions using single FACTS device approaches are also analyzed.

In this chapter, I provide a description of the Shanghai power grid along with a characterization of its voltage and power quality requirements. Then, I apply the following solutions to address these requirements:

- FCL devices to reduce the fault current and alleviate the stress on the circuit breakers protecting the grid.
- SVC-Light® combined with FCL devices to provide both voltage support and fault current reduction.
- HVDC-Light® placed in different locations to assess its impact on voltage stability and short circuit level reduction.
- Complete DC ring as a replacement of the 500 kV AC lines surrounding the city.

5.2 Structure of this chapter

The introduction and structure of this chapter are provided in sections 5.1 and 5.2 respectively. Section 5.3 provides a description of the Shanghai power grid along with a characterization of its short-circuit current, dynamic voltage stability, and power flow control problems. These problems are analyzed through simulation and reported in 5.3.1, 5.3.2, and 5.3.3 respectively.

In section 5.4, different solutions to solve the problems identified in section 5.3 are analyzed; these solutions using FCL devices, SVC-Light®, and HVDC-Light® are studied and reported in 5.4.1, 5.4.2, and 5.4.3 respectively.

In section 5.5, a novel solution based on a DC ring topology using VSC stations to comprehensively meet all power grid requirements is proposed. Section 5.6 reports

the main findings of this chapter and section 5.7 lists the relevant references that were consulted during this study.

5.3 The Shanghai power grid

The evolving Shanghai power grid faces enormous challenges in the areas of generation, transmission and distribution of the rapidly increasing amounts of electrical energy in demand. Its development should address issues of congestion, voltage stability, short-circuit power restriction, permits, and scarcity of land or right of way. Solutions including power flow controllers, fault current limiters, and high voltage transmission systems are considered for potential implementation.

In this section, an equivalent model of the Shanghai power grid projected for 2012 is modeled in order to investigate solutions for the issues this network is facing. The simulation is executed using the ABB power transient software analyzer (SIMPOW) where detailed modeling of the generators including exciters and governors is performed. Half of the total load is modeled as inductive motors and the other as constant impedances.

The VSCs are modeled using an injection model that is suitable for analysis of power flows and dynamics in power grids. The model interacts with other network elements to asses the dynamic performance and stability of the power system.

Because the harmonics and DC transient components can be eliminated by separately installed filters, they have been neglected in the injection model.

The model uses positive sequence voltages and currents and is valid for symmetrical condition only. The AC voltage and current quantities are represented by phasors that vary with time during transients.

The model of the VSC shown in Figure 5-1 consists of a filter modeled as a shunt capacitor, a reactor representing the transformer leakage and a fundamental frequency voltage source. The converter losses are represented by shunt resistors R1 and R2 connected on the DC line.

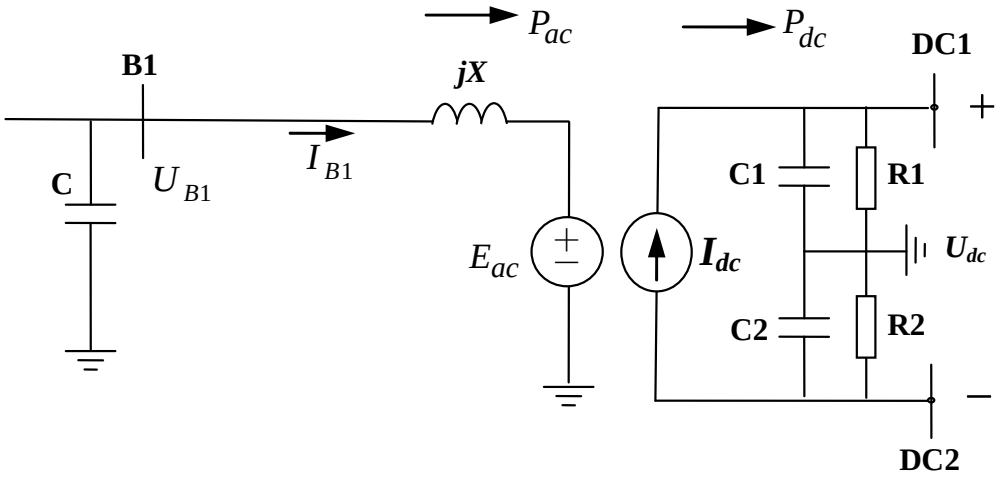

Figure 5-1: Injection model of an VSC

The DC capacitances C, C1, and C2 as well as the resistances R1 and R2 are modeled by standard components available in SIMPOW. The control uses the

voltages at buses B1, DC1, and DC2 as well as the current in the reactor X to control independently the active and reactive power of the converter.

A HVDC link is modeled using two converters connected by a cable. The equations describing the model behavior are detailed in [02] and an example of data entry for a HVDC-light to SIMPOW is provided in APPENDIX B.

5.3.1 Short-circuit current level

The development of the Shanghai power grid is driven by a load forecasted to increase up to 23 GW by 2012. The single-line diagram of the projected 2012 Shanghai power grid shown in Figure 5-2 comprises two 500 kV AC loops and several 220 kV AC subsystems. The grid supplied power is provided from local and remote sources where 18% come through two 500 kV DC lines, 22% through 500 kV AC lines and the remaining 60% are locally generated.

The grid as planned is relatively strong and could weather most of the system transients. It could even survive the loss of the inner 500 kV AC loop. However, as the load is set to increase, additional electric power will be needed through local or remote sources. But, the limited availability of construction sites will derail the addition of more 500 kV substations or further divide the 220 kV grids. Therefore, high short-circuit current will become a challenge and a limiting factor for the development of the power grid.

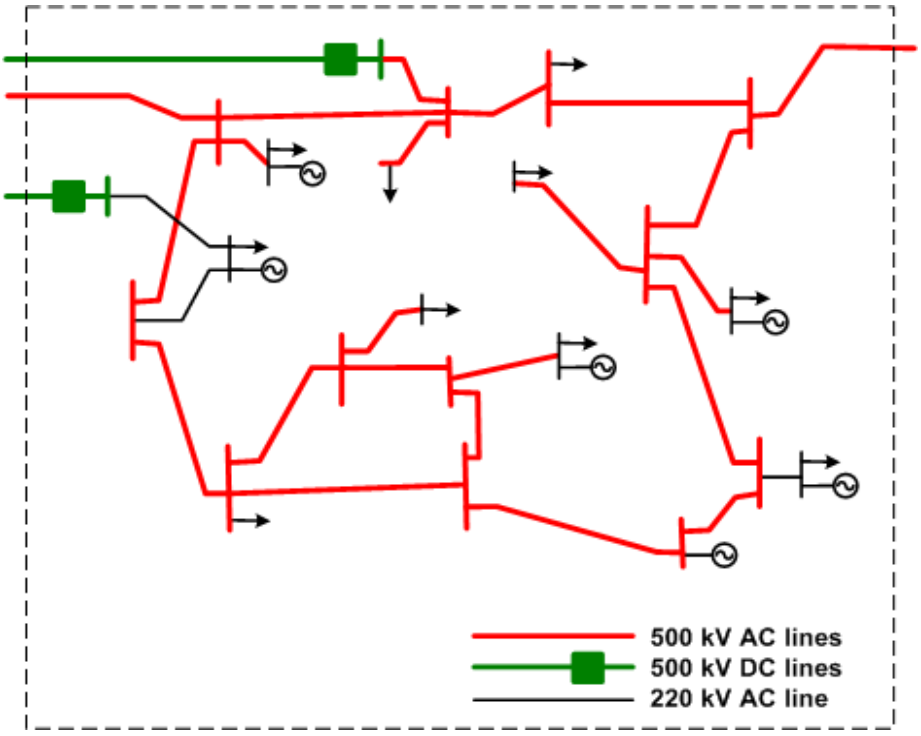

Figure 5-2: Single-line diagram of Shanghai power grid

With the 2012 forecasted load, the short-circuit current of the 500 kV AC system exceeds 55 kA and that of the 220 kV AC system exceeds 45 kA [08]~[10] as shown in Figure 5-3 for different voltage levels.

With the projected load increase beyond 2012, the maximum short-circuit current for the 500 kV AC system will exceed the capabilities of existing circuit breakers limited at 65 kA. Therefore, Shanghai power grid planners are looking for measures to reduce the short-circuit current levels without impacting the reliability or efficiency of

the system. Some of the investigated technologies include series reactors and other current limiting devices.

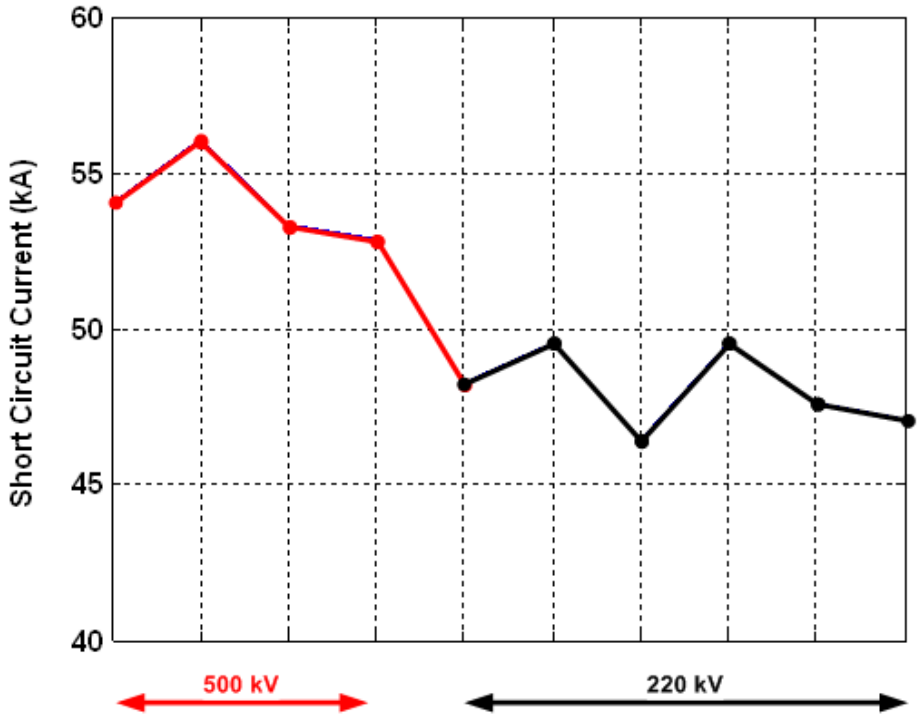

Figure 5-3: Short-circuit current in Shanghai power grid

5.3.2 Dynamic voltage instability

As the Shanghai power grid is also characterized by dense load areas it is subjected to voltage instability problems [01], [04] especially at the 220 kV subsystems that lack local dynamic voltage support [05]. This issue becomes more evident in summer period where a huge number of air conditioning units kick-off and cause huge voltage fluctuations pushing, sometimes, the system out of its stability limits.

The problem of voltage stability is illustrated by the transient performance of the power grid under fault conditions. Many fault cases were simulated at different locations but results of particular interests were reported for the two areas A1 and A2 indicated in Figure 5-4.

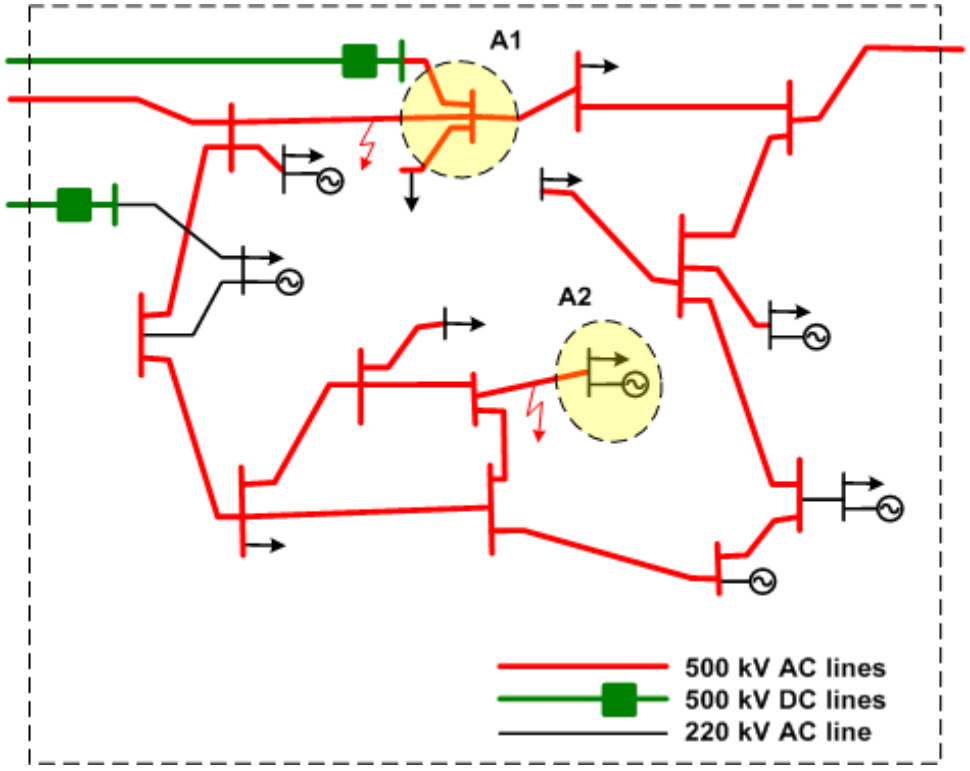

Figure 5-4: Voltage stability problems

In A1, a three-phase to ground fault was initiated at the 500 kV bus and cleared 5 cycles later by tripping the line located at the left of the fault. The tripping of the line opened the outer 500 kV loop and rendered the portion of the network connected to the inverter of the HVDC link weak. Under this contingency combining a three-phase

fault and a weak network, commutation failures did happen in the inverter of the existing HVDC link causing a further decline in the AC voltage and preventing voltage recovery to pre-fault values as depicted in Figure 5-5.

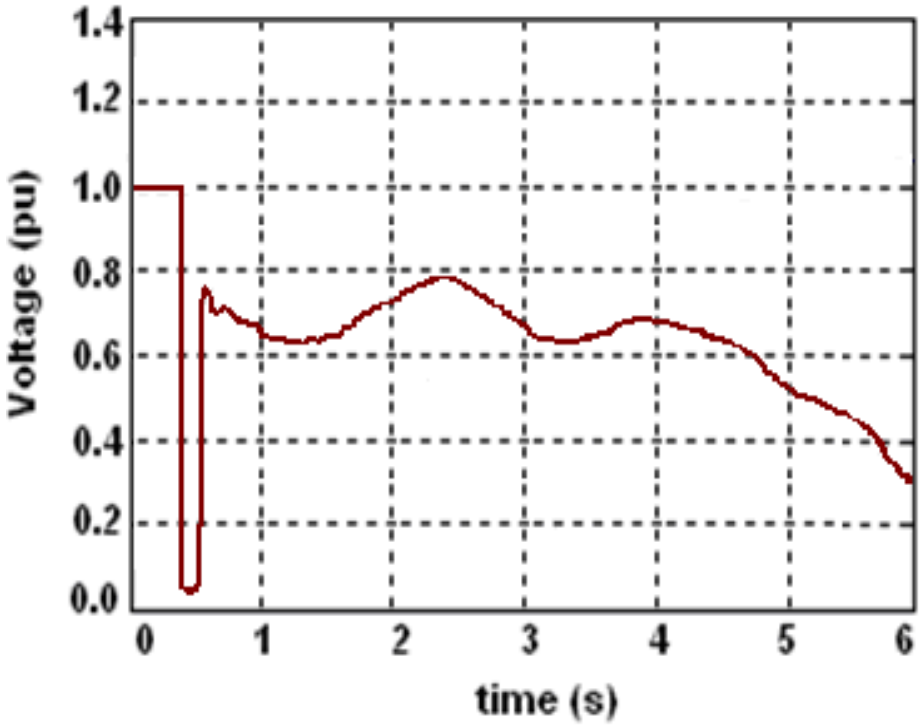

Figure 5-5: Voltage response at A1

Location A2 is near the center of the city and has a local generation plant to help serve the load. When a fault is initiated at the 500 kV AC line connecting A2 to the inner loop and then cleared by tripping the line from both ends, A2 became islanded and its post-fault voltage remained around 0.8 pu as shown in Figure 5-6.

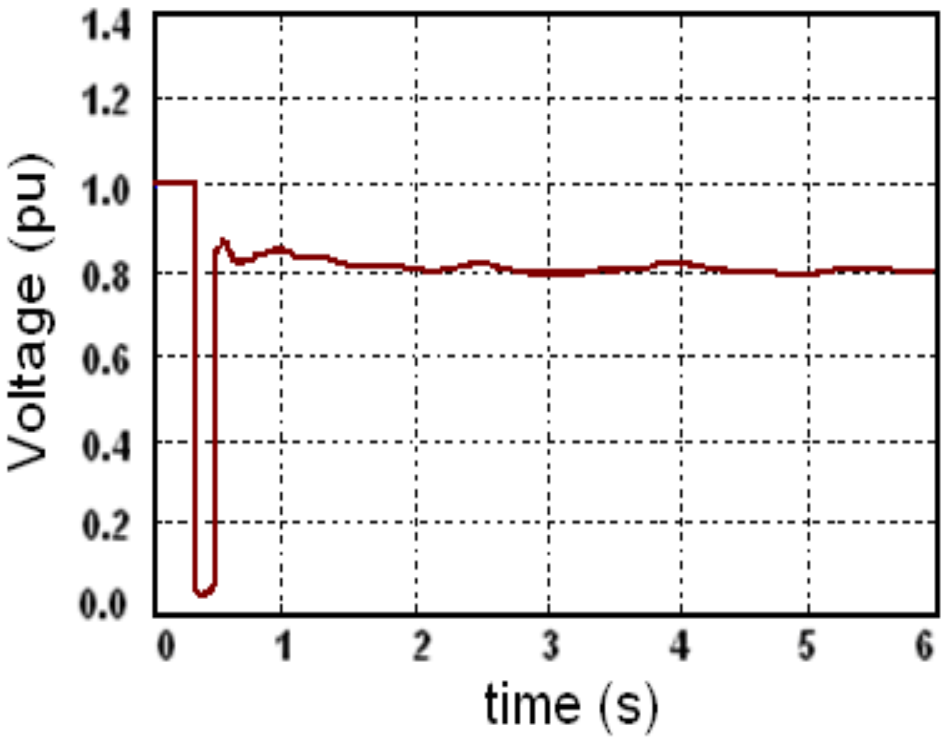

Figure 5-6: Voltage response at A2

5.3.3 Feeding bulk power into city center

As it was reported in many papers, the load demand increases rapidly in growing cities of China which need more electrical power to be fed into city center [06]. The increased need for power transfer to the city can be addressed by installing new high voltage lines or adding local generation plants. Either of these options is not always easy to implement due to scarcity of available land, right of way, and negative environmental impact.

A new overhead line needs a right of way that is not easy to get with tightening environmental regulations. Furthermore, the audible noise from high voltage lines may require a width of the right-of-way of up to 200 meters depending on where the line passes (residential or commercial areas). The width of the right-of-way can reach the 360 meters nearby schools to limit health risks caused by exposure to electro magnetic fields. However, the impact of high voltage lines passing next to housing compound will reduce the property value. This effect may be significant up to one km from the line.

Underground AC cables can solve the problem of right-of-way but would have reactive power balancing problems, increased short circuit level and limited transmission distance [11]. An AC cable exhibits a large generation of reactive power during low load, which raises problems with over-voltage levels, forcing measures such as voltage regulation to be implemented.

DC cable option shows no technical limits to the transmission distance and does not contribute to short circuit level. In fact, DC cable improves reactive power balance and for a given cable dimension, the power handling is higher for DC than for AC. The power handling improvement is possible due to better utilization of the insulation and lower losses in conductors and shields attributed to DC cables.

5.4 Applied solutions and their limitations

In section 5.3 a description of the Shanghai power grid was provided and challenges such as increased short-circuit current, voltage stability and power flow control were discussed.

In this section, I address these challenges and identify a solution for each one of them. The merit of each solution is assessed along with the limits of its contribution to fix one or many of Shanghai power grid problems.

The aim of this section is not meant to be an exhaustive screening of all possible solutions, but to show that a particular problem can be addressed by an existing FACTS device. It is also the goal to show that a solution addressing a particular problem such as short-circuit current has a localized effect and does not address other problems such as voltage stability. Therefore, to fix short circuit and voltage stability problems on all buses, many FACTS devices should be placed in locations prone to this or that problem. This would make the power grid complicated to operate and does not shield it from future expansion in load or generator capacity.

By presenting individual solutions as implemented in existing grids and by defining their limitations, I prepare the ground for a more comprehensive approach that combines the advantages of all individual solutions without adding complication to grid operation or expansion.

In this section, I investigate ways to limit fault current levels, control power flows, and improve voltage stability in the Shanghai power grid.

5.4.1 Fault current limiting strategy

There are many devices available that can be used to reduce fault currents by dynamically increasing the fault impedance in the fault pathway. A survey of the fault limiting technology is presented in Chapter 2.

In this section, I am considering a FCL device composed of a series LC circuit as shown in Figure 5-7. The LC circuit is tuned to present zero impedance at fundamental frequency.

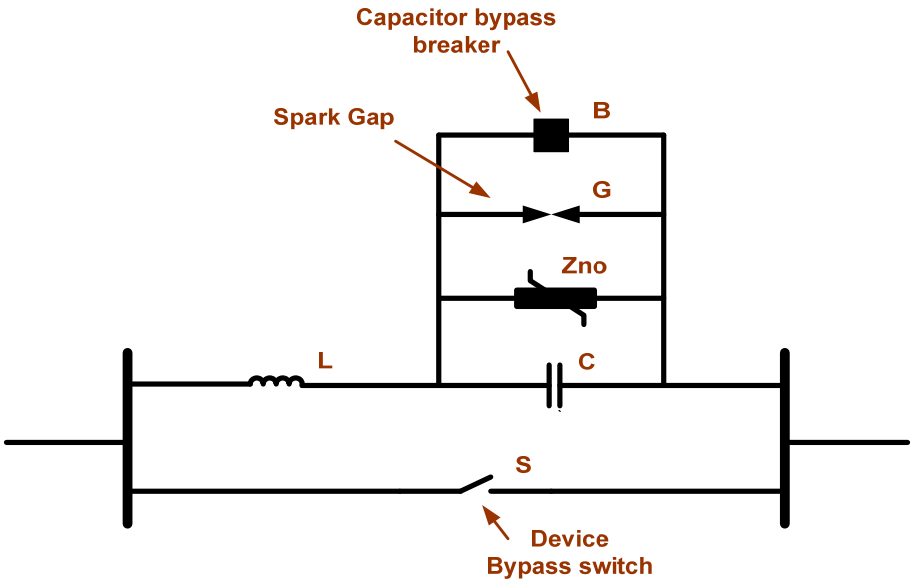

Figure 5-7: Single line diagram of a FCL device

During normal operation, the switch S, the spark gap G, and the breaker B are all open so that both the inductance and the capacitor are inserted in the line. When a fault is detected, the capacitor is shorted using the fast acting speed of the spark gap G followed by the closure of breaker B. this maneuver of bypassing the capacitor bank will leave the inductor in the circuit to limit the fault current. When the fault is cleared, the capacitor is reinserted in series with the inductor.

The FCL device can be installed in series with a transmission or distribution line or between two buses. These two configurations are presented in Figure 2-2 and Figure 2-3 respectively. In a line connection, the FCL can be installed, for example, at an exporting bus of large generators to limit their contribution when a fault occurs. In bus connection, the impedance of the entire loop will increase when the fault occurs. This is, by far, the most used topology to limit fault currents.

Based on the short circuit results calculated in section 5.3.1, the five locations shown in Figure 5-8 were selected as optimal placements for FCL devices during simulations. The FCL devices are inserted, in bus connection, into the 500 kV outer loop to reduce the short-circuit currents of both 500 kV and 220 kV systems. The parameters of the simulated devices listed in Table 5-1 are selected to reduce the fault currents under 45 kA for the 220 kV systems and 50 kA for the 500 kV systems.

Table 5-1: Parameters of installed FCL devices

Name	Voltage	Inductance	Capacitance
FCL1	500 kV	15 ohm	-15 ohm
FCL2	500 kV	15 ohm	-15 ohm
FCL3	500 kV	15 ohm	-15 ohm
FCL4	500 kV	15 ohm	-15 ohm
FCL5	500 kV	15 ohm	-15 ohm

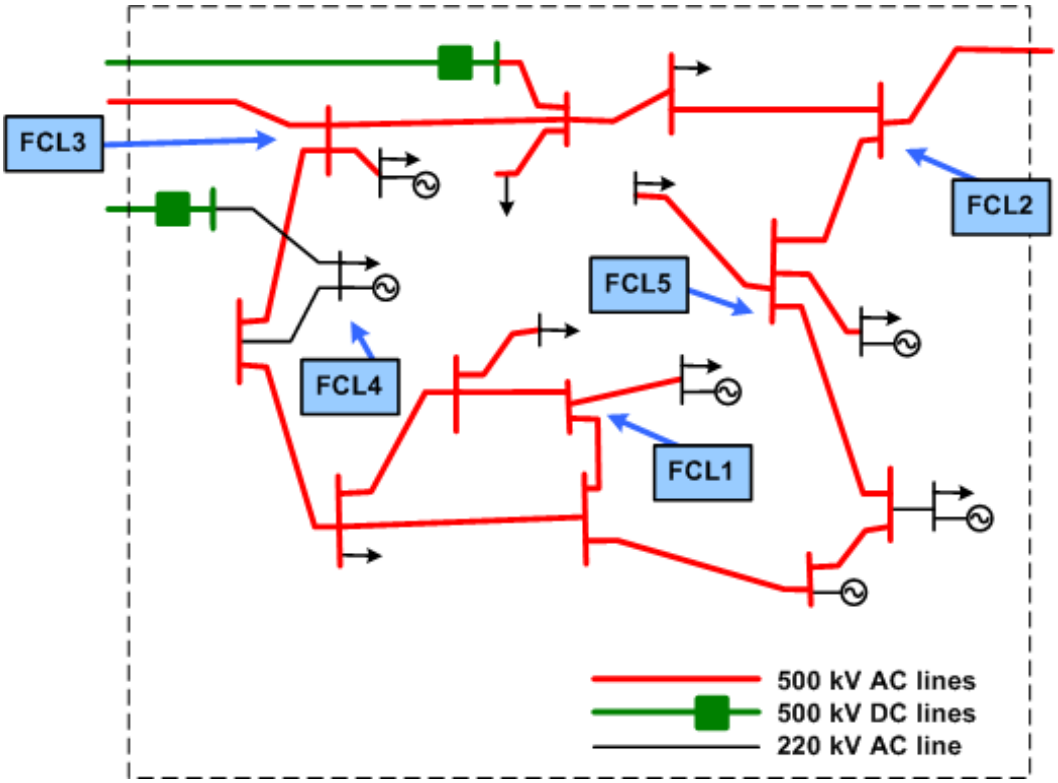

Figure 5-8: Placement of FCL devices

Simulation results compiled in Figure 5-9 show the effectiveness of FCL devices in reducing the short-circuit current and alleviate the stress on circuit breakers protecting the grid.

However, these devices do not address the voltage stability issues because their contribution consists only on increasing the impedance of the network during faults. No reactive power support is provided by these devices and no power flow control can be obtained from their actions. In fact, a FCL causes problems for protection coordination because it changes the network impedance during faults. This would require recalibration of all distance and differential protection relays settings based on the new impedance values. Furthermore, any changes of loading or generation capacity would probably involve modifications to existing FCL devices or addition of new ones. Any of these alternatives would involve the tedious recalibration of the protection relays based on the new network impedances.

Because addressing the fault current alone does not represent a comprehensive solution to city grid problems, FCL devices do not represent the optimal solution. Therefore, other alternatives should be considered.

To address voltage regulation and voltage stability, a SVC-Light® can be used in combination with FCL devices. The placements and ratings of both SVC-Light® and FCL devices are identified by a load-flow and stability studies of the grid.

In section 5.4.2, a combination of one SVC-Light® and five FCL devices are used to address both fault current and voltage stability problems existing in the shanghai power grid.

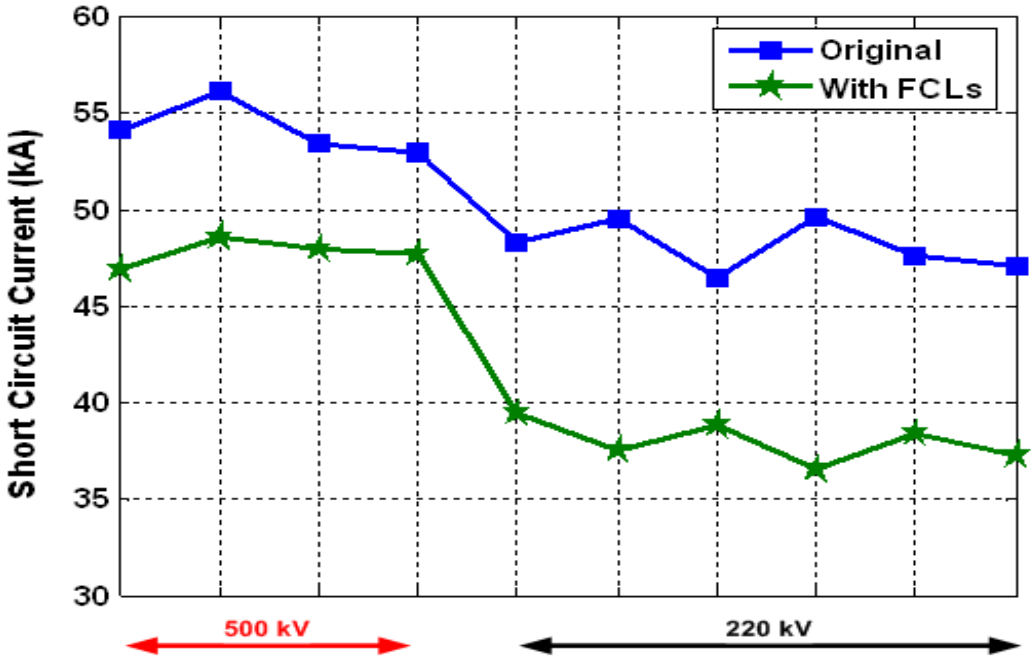

Figure 5-9: Short-circuit current with FCL devices

5.4.2 Combined voltage support and fault current limiting strategy

In section 5.4.1, I discussed the contribution of FCL devices in reducing fault currents and alleviating stresses on circuit breakers protecting the power grid. But I also noted that FCL devices do not have the capability for regulating the voltage or providing power flow control and, consequently, their addition to the power grid do not solve the voltage stability problems.

In this section, a SVC-Light® is added to the FCL devices in order to provide voltage support by regulating reactive power at the area indicated in Figure 5-10. The selection of the SVC-Light® placement was reached after a stability study of the original network showed a vulnerability of the existing HVDC inverter to faults. The study performed in section 5.3.2 revealed a risk of commutation failures for the existing inverter that causes the voltage to collapse (see Figure 5-5) in presence of a three-phase to ground fault.

The study also showed that a minimum installation of a 250 MVA is needed to meet the voltage stability requirement at the indicated location. For the simulation, a 300 MVA SVC-Light® was selected and installed using the low voltage winding of an existing transformer in that location.

The addition of the SVC-Light® helped support the voltage after the fault is cleared and by doing so prevented extended commutation failures of the existing inverter from happening. The performance of the SVC-Light® on improving voltage stability is reflected on the voltage waveform presented in Figure 5-11. By contrast, recall that the same fault initiated on the original grid caused the voltage to collapse due to commutation failures of the nearby inverter and the lack of voltage support (see Figure 5-5).

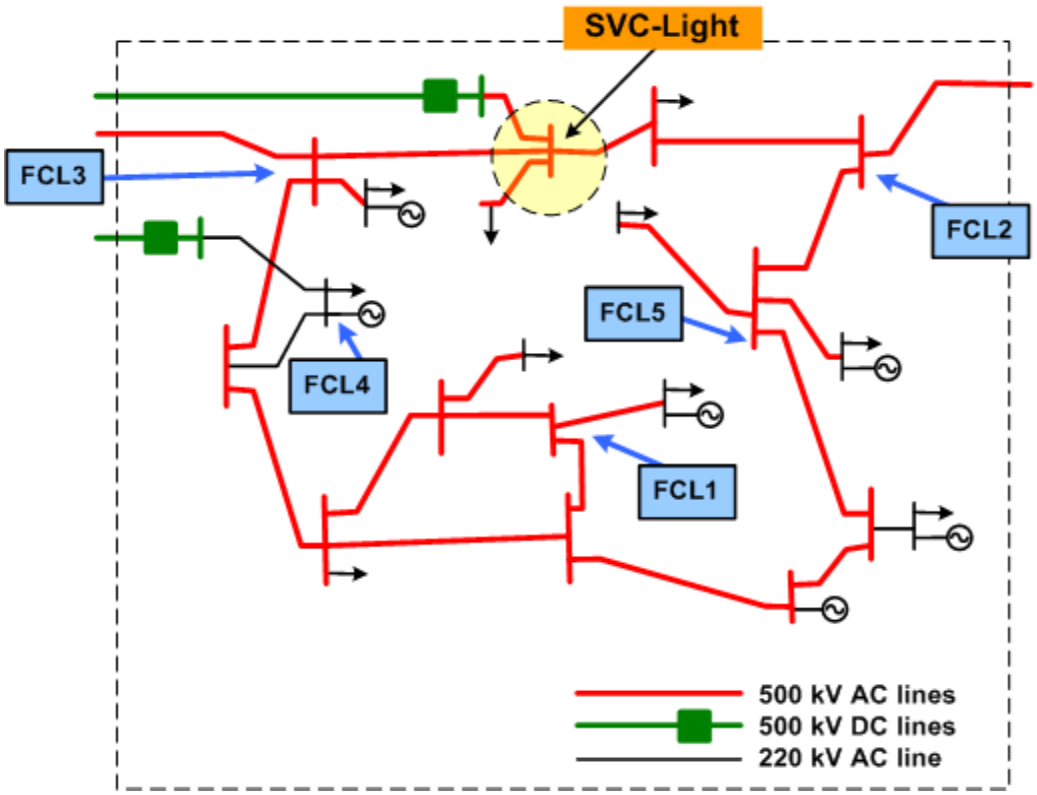

Figure 5-10: Placement of an SVC-Light® (STATCOM) and FCL devices

As a conclusion, the solution presented as a combination of a SVC-Light® and a number of FCL devices addressed two issues; voltage regulation and fault current limiting. I should first point out that for a more complex grid; more than one SVC-Light® may be needed in combination with FCL devices to effectively address fault currents and voltage stability issues. This would raise control coordination difficulties and increase the cost of the solution. Even with increased and well placed SVC-Light® and FCL devices, I can not address power flow control in a rigorous way. It is

possible to have a limited power flow control by controlling the voltage levels in different buses using SVC-Light® devices, but this approach remains limited in its scope and effectiveness.

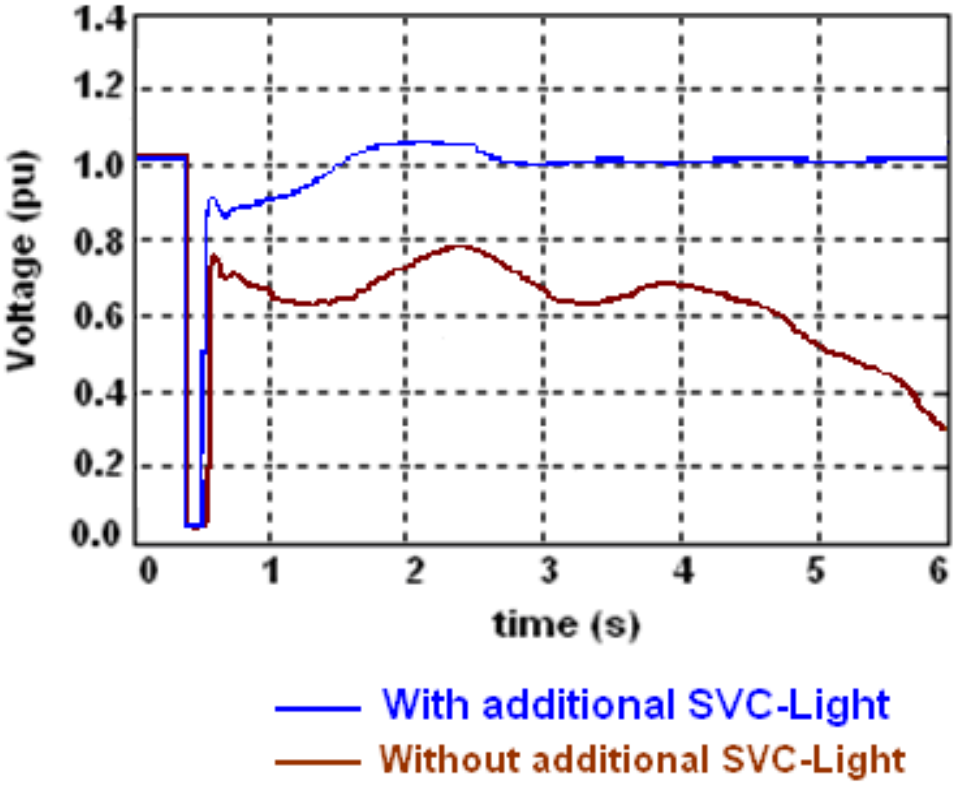

Figure 5-11: Performance of an SVC-Light® on voltage stability

Therefore, a different solution needs to be considered. The solution should, not only, reduce fault current but also regulate voltage as well as active and reactive powers in the grid. Such a solution can take many forms such as phase-shifting transformer in combination with a voltage regulating device, an inter-phase controller, a unified

power flow controller or a HVDC-Light® link. Since the concept of operation of all these devices is the same, I will only discuss the HVDC-Light® and evaluate its contribution to solve the Shanghai power grid problems.

In the following sections, an analysis of the contribution of a HVDC-Light® link to the grid stability, power flow control, and fault current limiting is performed for different placements of HVDC-Light® within the Shanghai power grid.

5.4.3 HVDC-Light® based solutions

VSC are becoming the main converter types in modern power electronics. Their characteristics and operation flexibilities allow the implementation of a wide range of complex power conditioning devices based on scalable and proven simple converter modules. VSC technology has enabled the development of HVDC-Light® systems with converter stations that require smaller filters and no local generations or synchronous condensers and with control properties far superior to those of classic HVDC using thyristor switches.

Through a number of HVDC-Light® installations, the advantages, reliability and flexibility of the technology had been verified. Encouraging experience includes superior control properties and very high availability.

Direct current transmission in the form of classical HVDC or HVDC-Light® is the only efficient means of controlling power flow in a network. Due to converter control of the transmitted power, HVDC cables can never become overloaded. Furthermore, an AC network connected with neighboring grids through HVDC links may, at worst, lose the power transmitted over the link. If the neighboring grid goes down - the HVDC transmission will act as a firewall against cascading disturbances.

HVDC-Light®, when connected to the grid, can provide dynamic voltage support in response to system disturbances and balance the reactive power demand of large and fluctuating industrial loads. A HVDC-Light® is capable of both generating and absorbing variable reactive power continuously as opposed to discrete values of fixed and switched shunt capacitors or reactors. With continuously variable reactive power supply, the voltage at the bus may be maintained smoothly over a wide range of system operating conditions. This entails the reduction of network losses and provision of sufficient power quality to the electric energy end-users.

In the following sections, HVDC-Light® technology is used in Shanghai power grid to address challenges such as power flow control, huge fault current values and voltage stability concerns.

5.4.3.1 Short circuit limiting capability

The present option places the HVDC-Light® link in the 500 kV loop as a substitution to one of its AC segments. The addition of the HVDC-Light® contributes to power flow management and voltage regulation. It also limits the fault currents by splitting the 500 kV loop as well as by controlling the converters reactive power output.

The placements of the HVDC-Light® considered for simulation are shown in Figure 5-12. One particular feature of configuration (A) in Figure 5-12 is that one of the converters of the HVDC-Light® is located nearby the existing HVDC inverter feeding the loop. This placement would provide reactive power support and prevent commutation failures of the existing thyristor-based inverter. It also helps with starting the existing HVDC link since the new HVDC-Light® uses VSC and is capable of black starting a network.

During the simulation of these configurations the active power control model of all schemes at sending ends is constant DC voltage and that at receiving ends is constant active power. The reactive power control model on both ends is set as constant reactive power to avoid the influence of control strategies.

Because the HVDC-Light® doesn't transmit reactive power, some capacitor values are adjusted to conserve the same power flow as that of the original power grid. Also,

to meet the same power flow requirements, the ratings of the added HVDC-Light® links shown in Figure 5-13 are set according to the values provided in Table 5-2.

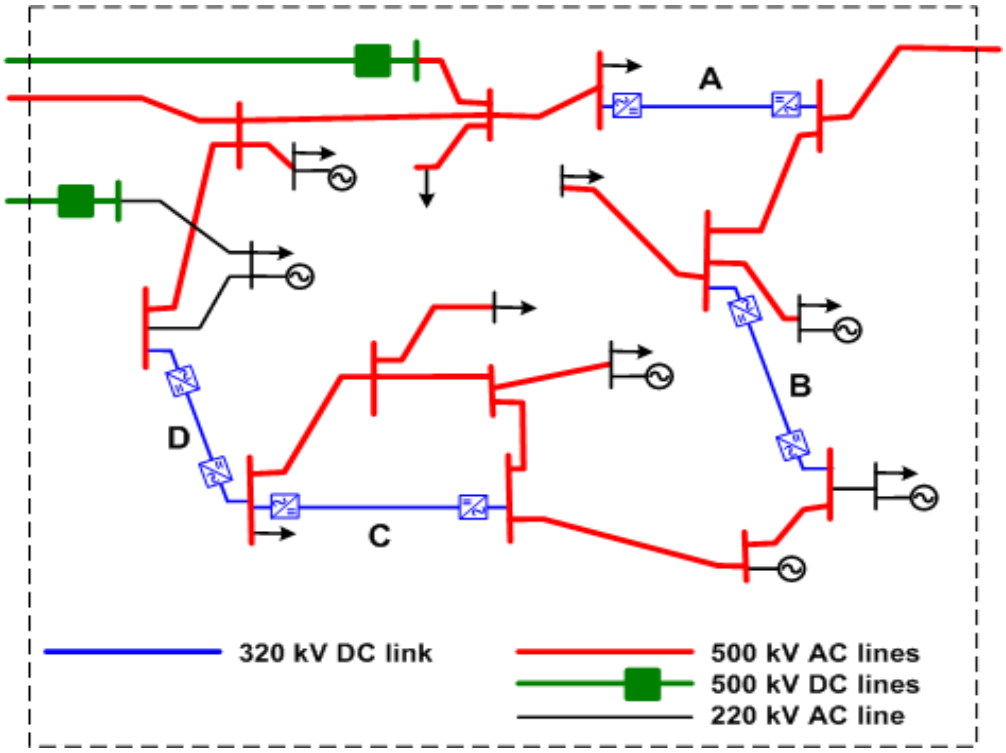

Figure 5-12: Placement of HVDC-Light® links in the 500 kV outer loop

Table 5-2: Ratings of HVDC-Light® systems

No	Capacity(MVA)	Voltage(kV)	Length(km)
Configuration A	**900**	**±320**	**30**
Configuration B	**500**	**±320**	**15**
Configuration C	**800**	**±320**	**30**
Configuration D	**900**	**±320**	**20**

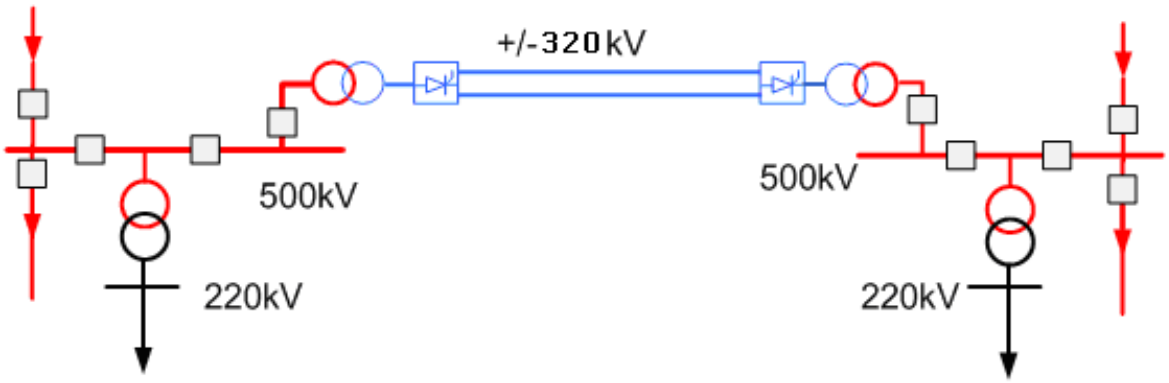

Figure 5-13: One-line diagram of a HVDC-Light® link

The short circuit calculations for the different placements of HVDC-Light® links show a reduction of fault currents as compared to the original grid. However, at certain 220 kV buses, the fault current still exceeds the 45 kA limit of existing AC breaker as shown in Figure 5-14.

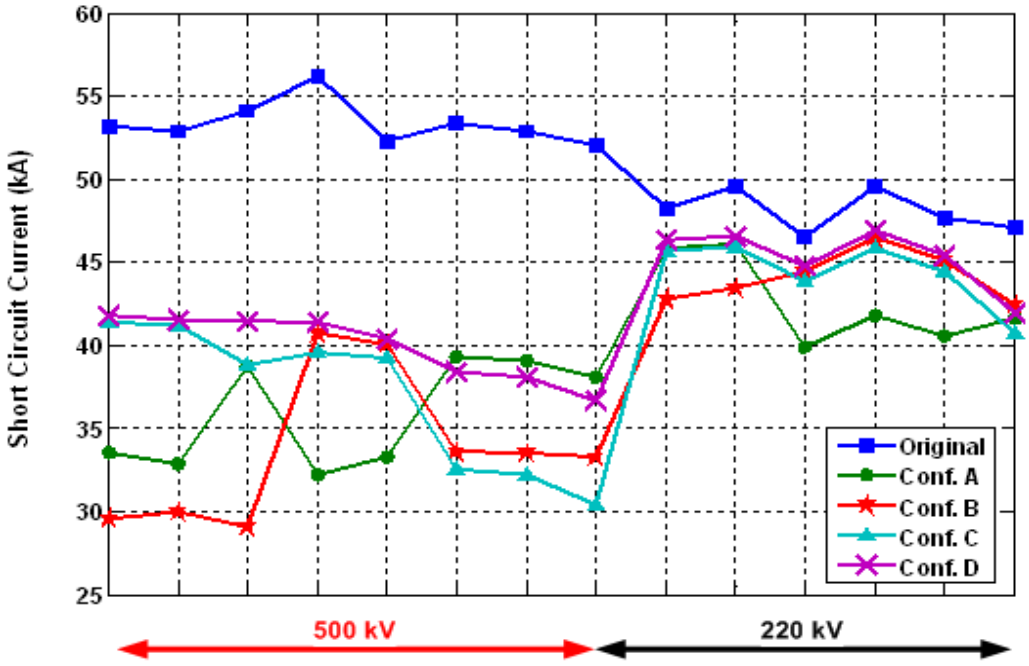

Figure 5-14: Short-circuit currents for different placements of HVDC-Light®

As a conclusion, adding a HVDC-link to the 500 kV loop as a replacement of one of its AC segments reduces the short-circuit current to levels bellow the threshold of 45 kA for certain buses but does not represent a comprehensive solution. Therefore, a HVDC-Light® solution needs to be combined with other current limiting devices or more than one DC link placed in different locations should be considered for the solution to be technically viable. Furthermore, any subsequent changes to the network loading or supplied generation would challenge once again the rating and positioning of the DC links. Thus, based on the short circuit performance alone, this

solution lacks economical justification unless other technical features can be obtained such as voltage regulation and power flow control.

In the following section, simulation assessing the performance of an added DC link to the 500 kV loop under fault conditions is performed. This simulation is based on configuration (A) of Figure 5-12 but the obtained results are general and can be applied to other configurations as well.

5.4.3.2 Voltage regulation and system stability

To demonstrate the voltage regulation capability of the HVDC-Light® link in the context of the Shanghai power grid, I selected configuration (A) of Figure 5-12 as a test case. The particular interest for this configuration (reproduced in Figure 5-15) is its close proximity to the existing current source inverter.

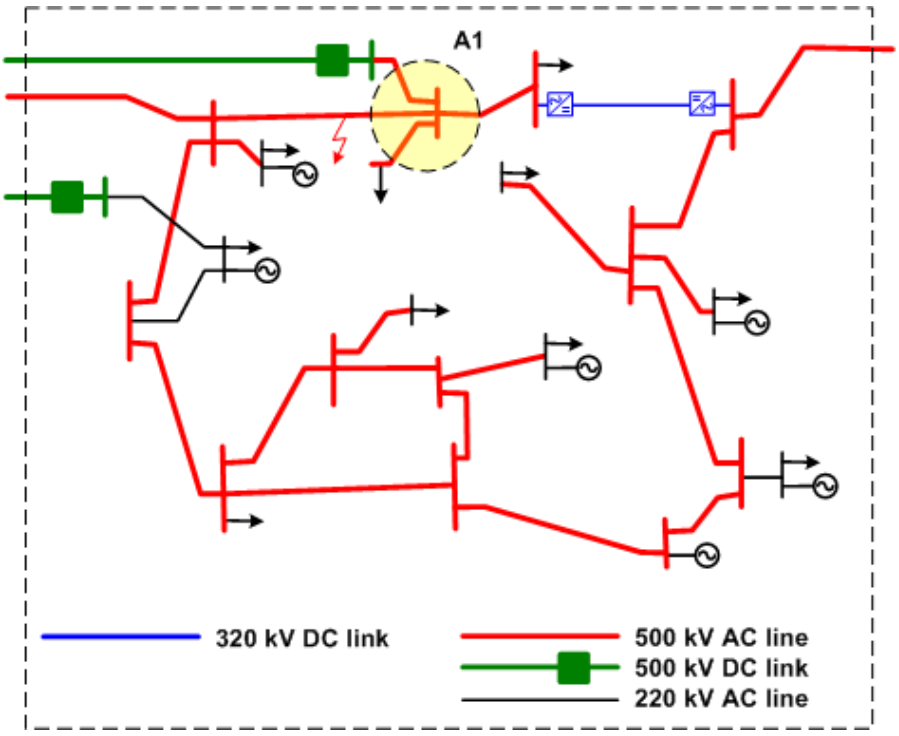

Figure 5-15: AHVDC-Light® placed near an existing current source inverter

We recall from section 5.3.2 that this inverter exhibited commutation failures in presence of a nearby fault initiated on the 500 kV loop. When the same fault was repeated with the added HVDC-Light® link, the bus voltage recovered to its pre-fault value due to the voltage support provided by the voltage source converter of the additional DC link. Figure 5-16 shows the voltage at the converter bus during the fault and compares the voltage profiles obtained with and without the additional HVDC-Light® contribution.

The addition of a HVDC-Light® on the 500 kV loop contributed to voltage stability due to the nature of the VSC in supporting bus voltage by reactive power regulation.

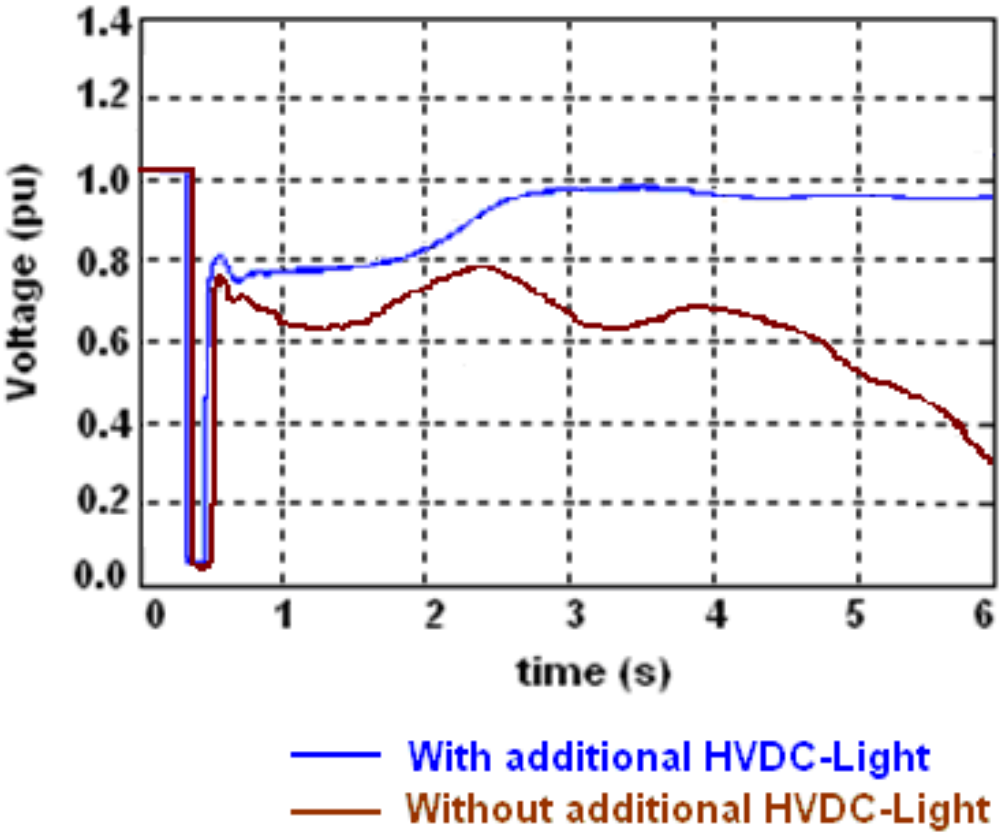

Figure 5-16: Voltage profiles with & without an additional HVDC-Light® link

This particular feature was demonstrated by placing the new link near an existing current source inverter that used to exhibit commutation failures when subjected to faults. The performance of the system was enhanced for that particular location but other subsystems connected to the 500 kV loop may still witness voltage stability

issues. As the aim of this study is not to pinpoint every single location that is impacted by voltage stability but to show that such a problem exists in Shanghai power grid and that an introduction of a HVDC-Link can only address problems for the subsystems located in its neighborhood. This exercise is meant to be a prelude to a more comprehensive solution that is presented and discussed in the following sections.

5.5 DC ring topology as a comprehensive solution

In the previous sections, I discussed solutions that addressed individual issues of the Shanghai power grid and I concluded that these solutions should be combined and placed in many locations of the grid to attain an acceptable fault current levels and voltage stability across the power grid. I also stated that these solutions when added together would make the power grid complicated and difficult to coordinate its controls. Furthermore, any future load or supplied generation increase would require additional tuning or new installations of these device-based solutions.

In this section, a more comprehensive solution based on a multiterminal use of HVDC-Light® stations is introduced. The detailed analysis of this solution and the required protection devices and algorithms are the subject of a subsequent chapter. In this chapter, only quantitative analysis of fault current limitation and voltage

stability is assessed without elaborate modeling of VSC stations controls and protections.

we recall from Chapter 4 that one important characteristic of HVDC-Light® technology is that the DC voltage in a two-terminal DC transmission system is constant in all modes of operation. Therefore, there is no DC voltage reversal connected with power reversal as required with classic HVDC links. The system can be viewed as a DC bus and any converter can feed power into the bus or extract power from it without affecting converters not involved in the changed power flow direction. This makes it easy, from a control point of view, to make multiterminal HVDC links. Based on this characteristic, the proposed solution consists of a number of HVDC-Light® stations linking AC subsystems to a DC ring as shown in Figure 5-17. Any of the AC subsystems can represent active or passive networks.

Because the power grid is divided into different networks, the fault current level for each one is governed by its generation capacity only. No fault contribution from other networks is possible. This, in fact, is a very important feature because it allows unlimited loading growth of the city grid without affecting existing AC breakers ratings or their protection settings.

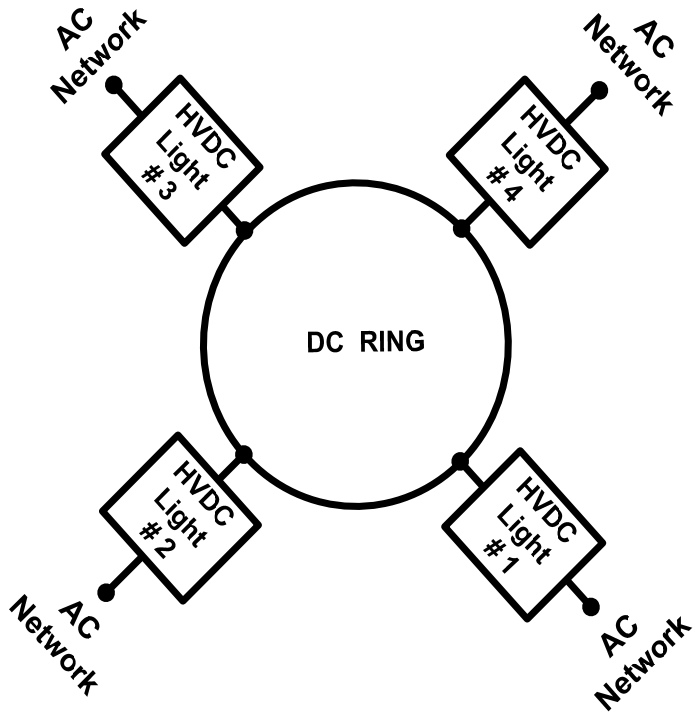

Figure 5-17: DC ring topology

The DC ring can be seen as a buffer between AC networks limiting the fault current to the inherent values of the subsystems and preventing faults from propagating between isolated subsystems.

The challenge for a successful DC ring application is three fold: 1) the choice of a mechanism to easily connect HVDC-Light® stations so loads and sources can be easily upgraded, 2) the protection coordination to be applied in order to properly locate and isolate DC faults, and 3) the fast protection device that can detect and

clear a DC fault without shutting OFF the HVDC-Light® stations or discharging the capacitors of the DC ring into the fault.

However, before addressing the above described challenges, let's verify that the proposed DC ring solution satisfies the two basic requirements I discussed in the previous sections; current fault limitation and voltage stability.

5.5.1 DC ring as a replacement of 500 kV AC loops

In this configuration, I replace the 500 kV AC loops of Shanghai power grid with two ±320 kV DC loops to which the remaining portions of Shanghai power grid are connected through VSC stations. Two possible configurations can be considered; 1) replace the inner 500 kV loop with a DC ring and 2) replace the outer 500 kV with a DC ring.

The first configuration shown in Figure 5-18 covers a limited portion of the total Shanghai grid but presents a cost effective solution for most of the grid problems. The city center that includes most of the loads will be powered through this DC ring with better voltage regulation and fault tolerance.

The utility planners can add more loops surrounding clusters of loads in a phased approach until all major AC subsystems are isolated from each others. These DC rings can replace entirely the existing AC loops or be connected in parallel with them.

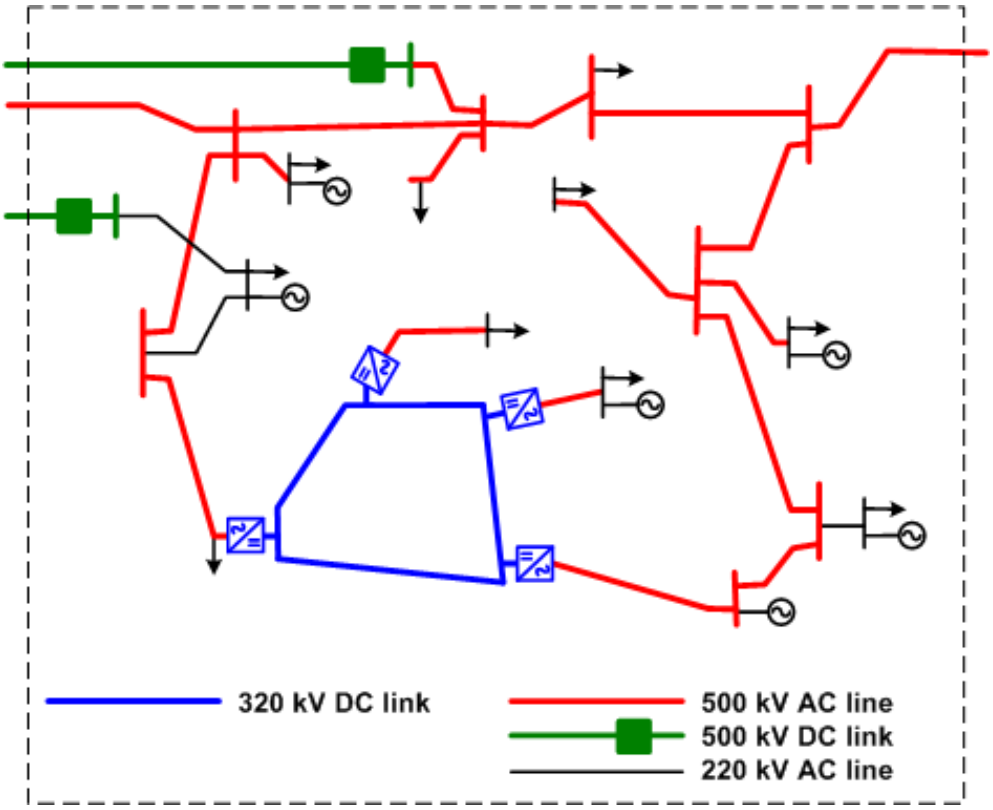

Figure 5-18: Replacement of the inner AC loop with a DC ring

The second configuration shown in Figure 5-19 replaces the outer 500 kV loop with a DC ring. The AC subsystems are then connected to the ring via VSC stations that share the same DC voltage. The ratings of these stations can be differently adapted to the subsystems to which they are connected. In this section I am considering this configuration for analysis and I am confident the outcome can also apply to the previous one.

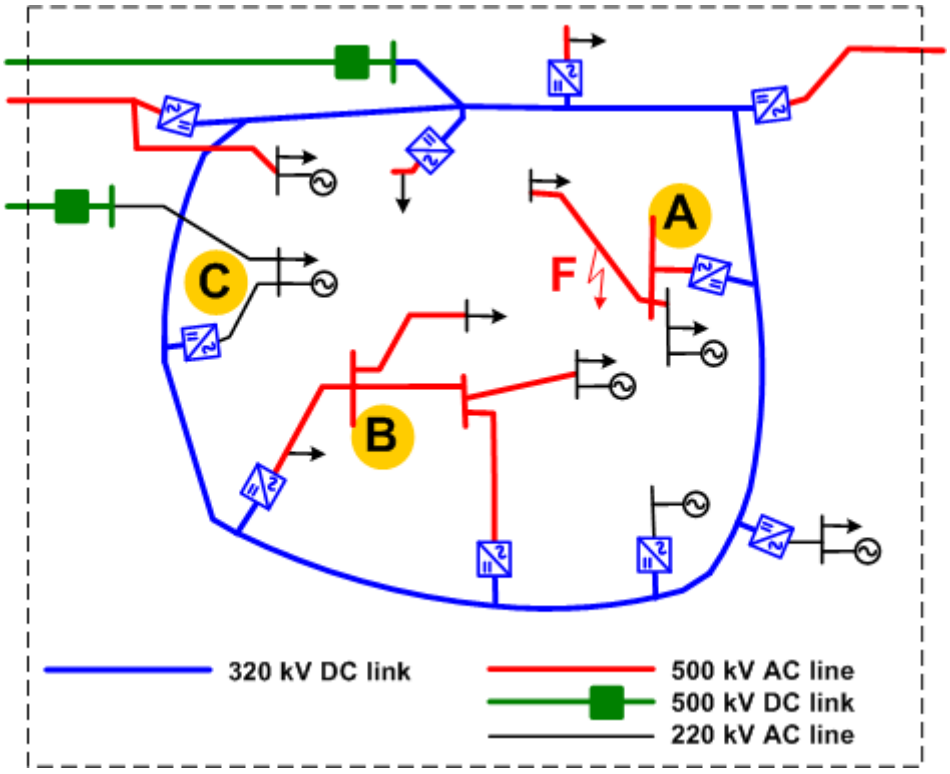

Figure 5-19: Replacement of the outer AC loop with a DC ring

By applying the DC ring topology shown in Figure 5-19, the Shanghai power grid becomes completely decoupled into many subsystems. Some of the subsystems contain generators and others contain only loads. It is then expected that fault current levels in each of these subsystems is no more than what local generators can supply since any contribution from other subsystems or from the DC system is prohibited by the VSC stations. The results of the short circuit calculation for the Shanghai grid with this DC ring topology are reported in Figure 5-20.

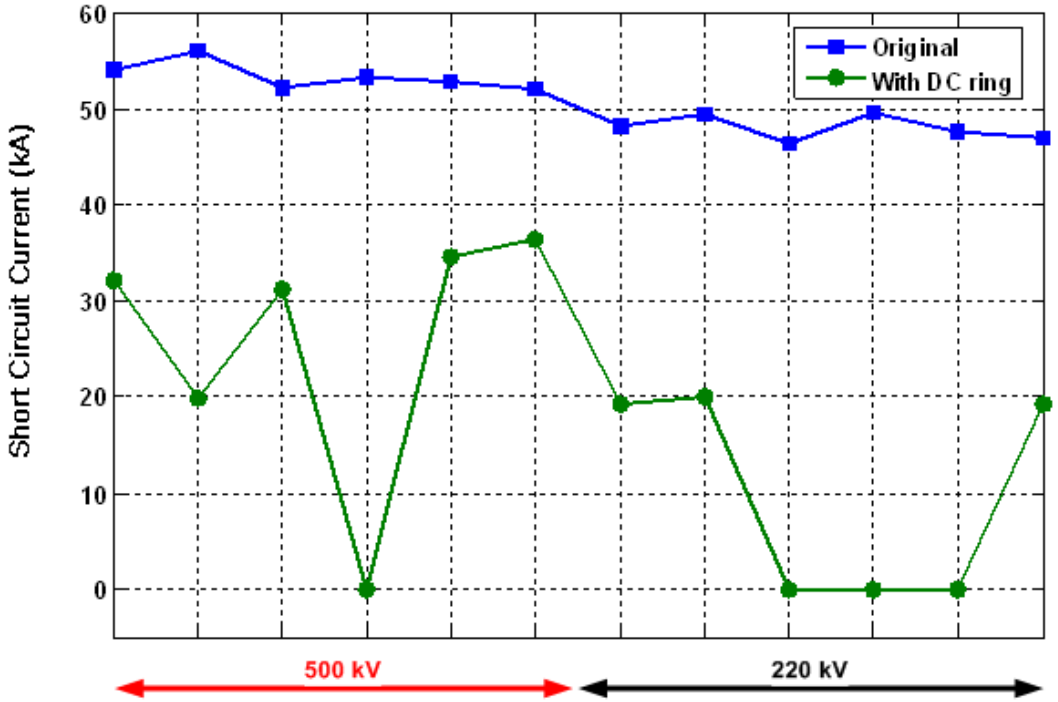

Figure 5-20: Fault current levels with and without a DC ring

Also, because of the ability of VSC stations on controlling active and reactive powers, voltage stability and power factors are improved across the whole grid. The need of shunt capacitors and shunt reactors is reduced and the power transfer between the DC ring and each subsystem is tightly controlled ensuring flexible and reliable pathways for energy transit.

For simulation purposes, I fixed the rating of all HVDC-Light® stations to 1000 MW at a DC voltage of ±320 kV which result in a DC current of 1563 A. Then I initiated

three-phase to ground faults at different locations in the AC grid and the results I obtained showed increased system stability and quick voltage recovery.

Figure 5-21 shows the voltage response for a fault initiated at point F. The fault is initiated at 0.3 seconds and cleared at 0.45 seconds. The biggest drop of voltage is for the bus located at a short electric distance from the fault. In the case of Figure 5-21, this voltage is indicated by the red trace and corresponds to voltage at bus A. The other buses are decoupled by the DC link and experienced a small disturbance. With better control and protection algorithms, the disturbances during faults can be reduced even further.

As you have probably noticed, no faults on the DC link were initiated. These cases were not forgotten but avoided because the outcome is known. When a fault is initiated on the DC link, the only course of action is to block the converters and then try to clear the fault from the supply side; in this case by using the AC breakers located in the 500 kV lines. This is not the best way of using a sophisticated power grid. I should be able to detect a DC fault and clear it without blocking any converter station and without discharging the capacitors of the DC link. For that reason, I need to develop a rapid protection algorithm and more importantly a rapid DC breaker. These two tasks will be addressed in the following chapters.

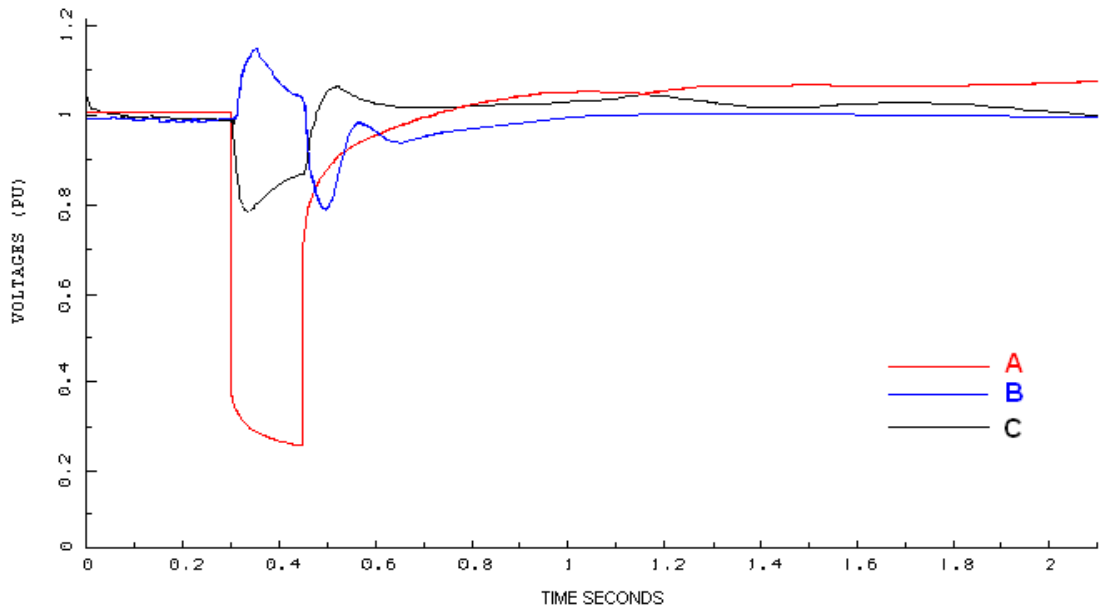

Figure 5-21: Voltage response for a fault at bus F

5.6 Conclusion

In this chapter, I described the problems that mega city power grids are facing in terms of fault current levels and voltage stability and I discussed solutions that address individual issues of the Shanghai power grid. I concluded that these solutions should be combined and placed in many locations of the grid to attain an acceptable fault current levels and voltage stability across the power grid. I also found that these solutions when added together would complicate control coordination and protection settings. Furthermore, any future load or supplied generation increase would require additional tuning or new installations of these

device-based solutions. Then, I presented a comprehensive solution based on a multiterminal use of HVDC-Light® stations sharing a common DC bus in a ring topology. This topology provides redundancy, better protection against faults, and does not increase short circuit levels. Adding loads or power sources does not impact system protection or performance. However, I also identified that a need for special protection against DC faults must be satisfied for the solution to be practical. Therefore, a DC breaker circuit and a fast protection algorithm will be provided in the following chapters to complete the solution I discussed here.

5.7 References

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CHAPTER 6 NOVEL DESIGNS OF A DC CIRCUIT BREAKER

In the previous chapter, I identified the need for a fast DC breaker as one of the core elements required for a successful implementation of DC ring topologies around mega cities. A fast DC breaker will also make possible the application of multiterminal HVDC-Light® with a common DC bus, the realization of wind farm with

a DC collector, and the proper protection of a navy ship equipped with a DC grid. In this chapter, I present two novel designs for a DC breaker that address both unidirectional and bidirectional power flows. The validity of each design is proven using simulation to assess its performance under solid and high impedance faults.

6.1 Introduction

With the introduction of different types of converters into the AC system, protection issues related to fault interruption emerged. To protect the system against the non self-extinguishing DC faults, a need for DC Circuit Breakers (DCCB) was immediately felt.

The lack of a fast DCCB has been one of the key issues affecting extensive applications of DC systems. For high voltage DC systems and multiterminal DC systems using VSCs, a DC fault would discharge all the capacitors causing delays in system recovery and possible wide system instabilities.

Protection philosophies from AC system drifted into the protection of these new mixed ACDC systems and fault interruption was done by employing high voltage high power AC Circuit Breakers (ACCB) on the AC side. The use of ACCB has deferred the development of the high power DCCB and low cost alternatives for fault interruption involving crowbars and fuses were also borrowed from AC protection. In addition to this, the ability to control the complete converter delayed the

development of DCCB. Besides being prone to arcing and restrikes, mechanical circuit breakers clearing times are limited by the speed of the contacts that take up to 150 ms to move apart. These clearing times are not suitable for multiterminal DC applications especially when VSCs are used.

For DC applications using common DC buses or ring topology, such as wind farms, naval distribution systems, multiterminal transmission systems and distribution systems, it is critical to mitigate and clear the fault before discharging the capacitor banks into the fault. Therefore, a fast fault detection algorithm and a fast circuit breaker capable of clearing times lower than 1.0 ms should be designed. Since, only power electronic can achieve response times that short, it is advised to design a breaker in modular arrangement and cheaper cost using semiconductor switches.

The advent of complete gate controllable devices like the GTO, IGCT and ETO, stimulated the development of DCCBs. Various types of DCCBs based on such devices have been reported in literature [01] through [06] but their rating and cost remain prohibitive for most applications.

Different ideas for solid-state breaker were proposed including those that integrate the CB functionality into the converter itself by choosing switching devices and operating them in the active region of their characteristics using gate voltage control [11], [12]. The most apparent solution suitable for high power applications points towards utilization of thyristor based circuit breaker; this creates a design challenge

since a thyristor interrupts current only when they reach a very minimum level. This implies a parallel resonant circuit should be designed and rated to compensate for the maximum fault current in the thyristor.

The principle function of a CB is to interrupt short-circuit current under fault condition while under normal operation it should carry the rated load current with high efficiency. Thus, the main requirements for a CB are [07]:

1. The CB should be able to interrupt a short-circuit current, normal rated current, or lower, and interrupting this current quickly without causing an abnormal voltage transients.
2. The CB should be a good conductor and have low voltage drop and low conducting losses. It should withstand normal currents as well as short-circuit currents thermally and mechanically.
3. The CB should withstand the short circuit for a certain time required to decide whether the fault is sustained or transient and whether to interrupt it or not.
4. When open, the CB should be an excellent insulator, and should withstand the normal as well as the transient voltages between phases and phase to ground.
5. The CB should be able to close a shorted circuit quickly and safely.

Thus, for the new solid state DCCB to be put to practical use and to operate successfully, it must provide at least the same level of functionality as mentioned

above. Different designs have been reported in literature with different degrees of merits and deficiencies. Some of these designs will be discussed for comparison purposes and new designs will be proposed.

6.2 Structure of this chapter

This chapter comprises seven major sections covering the state of the art of DCCBs and describing novel designs based on thyristor switches. The content of these sections is given bellow:

1. Section 6.1 provides a description of the motivation for designing a DCCB and outlines the design requirements.
2. Section 6.2 outlines the structure of this chapter.
3. Section 6.3 provides an overview of existing technologies. It discusses DCCBs using air-blast and SF6 AC breakers in 6.3.1, hybrid DCCBs in 6.3.2, and existing DCCB topologies using thyristors in 6.3.3. Commercial products and IP searches are provided in 6.3.4 and 6.3.5 respectively.
4. Section 6.4 describes two novel designs for DCCBs; a unidirectional and a bidirectional design. The modeling, analysis and validation of these two designs are provided in 6.4.1 and 6.4.2 respectively.

5. Section 6.5 provides practical design considerations for realizing the proposed DCCB using datasheets of existing diodes and thyristors. The rating of power electronic devices is calculated in 6.5.1, the design of snubber circuits for diodes and thyristors is performed in 6.5.2, the triggering techniques for series-connected thyristors are reported in 6.5.3, spurious triggering due to electro-magnetic interference is covered in 6.5.4, signal and power supply shielding considerations are discussed in 6.5.5, and gating related issues are reported in 6.5.6.
6. Section 6.6 concludes this chapter with a summary of the main important results and introduces the following chapter that discusses the protection scheme to be implemented with the proposed DCCB.
7. Section 6.7 lists some of the references that were consulted during this study.

6.3 State of the art on DC circuit breakers

In the early days of the HVDC technology, there was no need for DCCBs, when all transmissions were point-to-point, allowing complete control of currents by converter actions, even under faults. In principle, the same approach is valid for multiterminal HVDC systems as well. However, it would be necessary to shut down the entire system in order to isolate and remove a fault from any branch of the multiterminal DC system. This situation encouraged the development of DCCBs, which, with or

without converter control action (depending on their design) can switch out or reconnect parts of the system [08].

There are three types of DCCBs; the first utilizes ACCB as a main interrupting element, the second uses both PE switches and mechanical switches, and the third is purely PE device based.

6.3.1 DC circuit breaker based on AC breaker concepts

The first high voltage DCCB started as a research project initiated by Bonneville Power Administration (BPA) and the Electric Power Research Institute (EPRI) around 1980. The project resulted in the development of two prototypes of DCCB based respectively on the air-blast and the SF6 ACCBs.

6.3.1.1 Air-blast based HVDC breaker prototype

The prototype of HVDC breaker was developed by BBC and was based on the four-break type DLF 550 kV breaker as its main switching element [02]. As it is shown in Figure 6-1, the breaker consists of four modules. Each module consists of a switching element in parallel with an LC circuit and a protecting arrester.

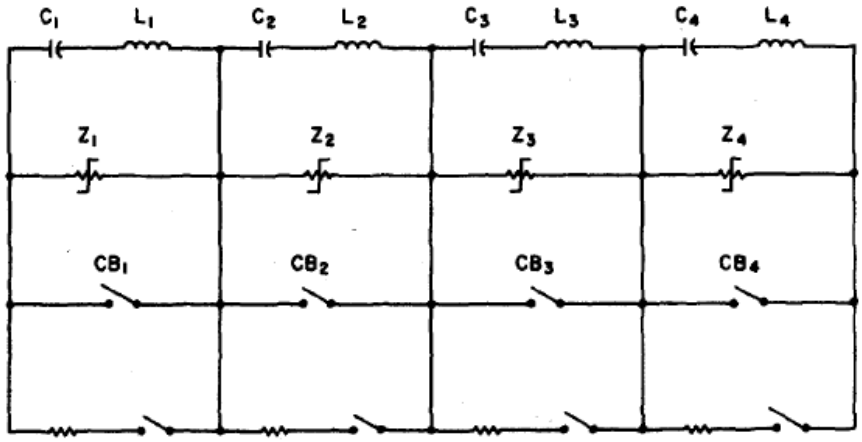

Figure 6-1: Air-blast HVDC breaker prototype [02]

The operation of the four modules is simultaneous and identical, therefore, only the first module containing CB_1, Z_1, C_1 and L_1 will be considered for analyzing the breaker operation.

As the circuit C_1-L_1 and the energy absorber Z_1 are permanently connected across CB_1, they are shorted and unexcited whenever CB_1 is closed. When a fault is detected and in order to interrupt the DC current, CB_1 is first opened. The departure of the contacts of CB_1 creates a voltage arc across CB_1. This arc initiates a current oscillation in the C_1-L_1-CB_1 loop at the natural frequency of the loop normally tuned at a frequency between 4 and 7 kHz.

As the DC current is diverted from CB_1 to C_1-L_1, the voltage arc increases due to the negative voltage-current characteristics of the arc in CB_1. This will create a positive

feedback that increases the oscillating current amplitude until it reaches the current to be interrupted. This results on a current zero through CB_1 allowing the switch contacts to completely depart from each other.

Once CB_1 is open, the DC current flows through C_1-L_1 causes the capacitor to charge rapidly until its voltage value reaches the conducting threshold of the arrester Z_1. At that voltage level, Z_1 conducts and dissipated the energy from the system. When the system energy is absorbed by Z_1, the current ceases to flow and the interruption process is completed.

For this particular application, the LC circuit natural frequency was set around 6 kHz and the arrester voltage at 175 kV yielding to a 700 kV for the combined four modules.

6.3.1.2 SF6 based HVDC breaker prototype

The prototype based on the SF6 AC breaker was developed by Westinghouse [02]. It uses the LWR 550 kV as its main switching element. The breaker is composed of four identical modules as shown in Figure 6-2 and the principle of operation is similar to the BBC prototype. The main difference between the Westinghouse and the BBC prototypes resides in the resonant circuit design. For the Westinghouse prototype, there is no added inductance and the capacitor is inserted by an independent

vacuum switch (VS) when the interrupter reaches the desired gap and develops an optimal gas flow conditions.

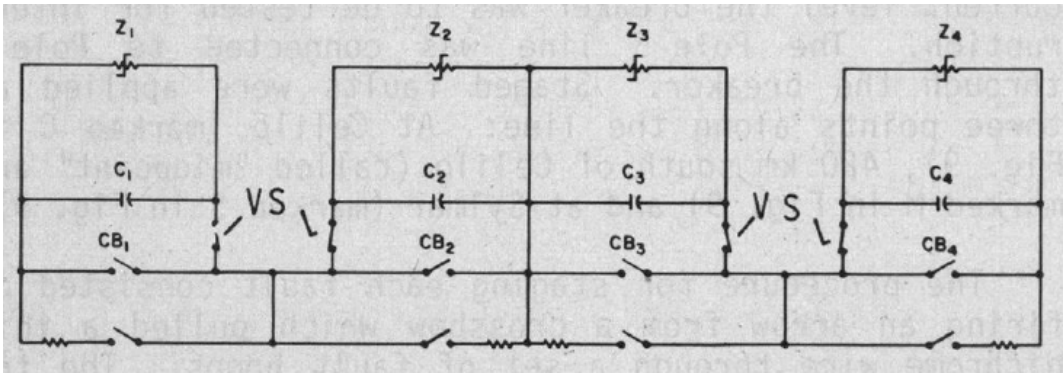

Figure 6-2: SF6 HVDC breaker prototype [02]

The two HVDC breaker prototypes from BBC and Westinghouse incorporate slow moving contacts and exhibit clearing time as slow as 150 ms. Attempts has been made to improve the response time of these breakers by improving the design of the AC breakers used as interrupting elements as well as by tuning the LC resonant circuit and actively charging the capacitor as shown in Figure 6-3.

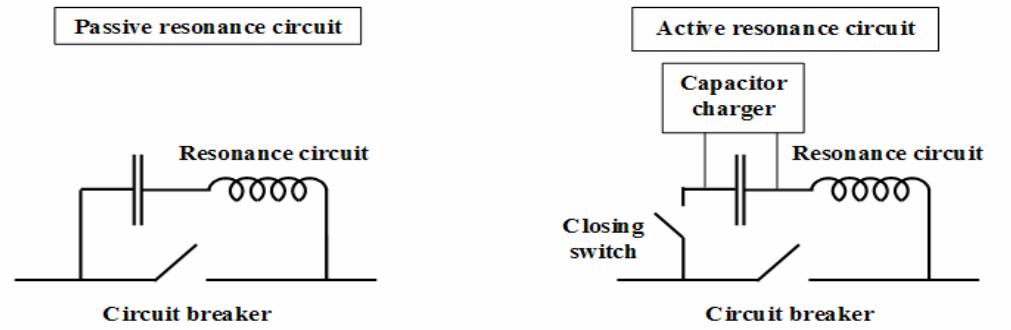

Figure 6-3: Passive and active resonant circuit

6.3.2 Hybrid DC circuit breaker

Modern semiconductor devices like GTO, IGBT and IGCT are now available with moderate to high current and voltage ratings. They also have very robust short circuit safe operating area [09]. Some concepts for Fault Current Limiting Circuit Breaker (FCLCB) have been proposed in recent literature [04], [06], and [10].

The integration of both mechanical breakers and static switches allows a combination of the former current carrying capabilities and the latter high speed arc less interrupting characteristics.

In order to keep the benefits of static interruption, an ultra fast contact opening is required. During the last two decades, several solutions have been proposed in this context [17], including hybrid breakers with thyristors [18], [19] or GTOs [20]. The recent venue of the IGCT switch, with its new performance opened new perspectives in the field of hybrid switching techniques.

A hybrid arrangement of three different parallel paths for fault current limiting and interruption is presented in [04]. The hybrid FCLCB consists of three parallel paths; path A as shown in Figure 6-4, consists of a fast operating mechanical transfer switch, path B consists of a semiconductor unit and a fast disconnecting switch, and path C consists of a current limiting impedance combined with a load switch. Since a single GTO can carry the current only in one direction, it is installed with a four-Diode Bridge to save costs (see D_1 to D_4 of path B in Figure 6-4), thus providing

unipolar conditions for the GTO for both polarities of the fault current. This semiconductor unit is called SEM.

The operation of the FCLCB is discussed here in brief. When a fault occurs, the ultra fast transfer switch (FTS) opens within a few hundred μs and produces an arc voltage drop of several tens of volts. However, the arc voltage is much too small for the purpose of short-circuit current limitation. Therefore, a GTO with a high current turnoff capability is employed to force the fault current onto the limiting impedance (path C).

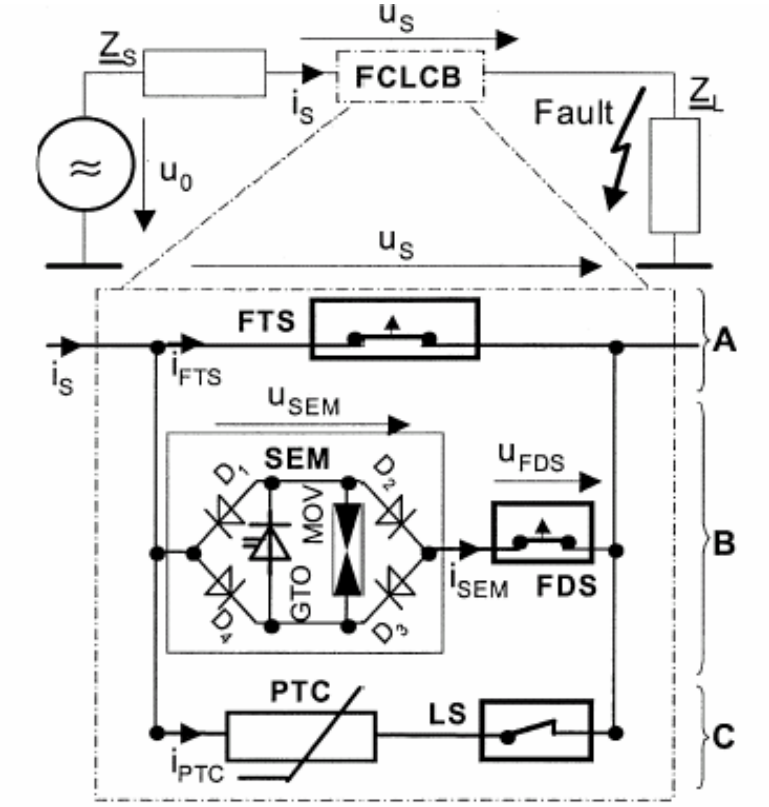

Figure 6-4: Hybrid fault current limiting circuit breaker [04]

Under normal operation, all three switches (FTS, FDS, and LS) are closed. When a fault occurs, the FTS is triggered by the protection unit that detects the fault. Due to contact separation of the FTS, an arc voltage builds up across the opening double contact gap and the current commutates from path A onto path B. Then, the GTO is turned OFF forcing the current onto the PTC resistor in path C. Turning OFF the GTO causes a very high di/dt and an excessive voltage rise due to the self inductance of the loop B-C. As a consequence, the voltage U_S jumps up to approximately 4.5 kV, and a further rise is limited by the Metal-Oxide Varistor (MOV).

When the current is completely transferred onto the PTC resistor the massive power dissipation within the PTC resistor leads to a temperature rise which, in turn, results in a significant increase of resistivity due to the resistor positive temperature coefficient. Along with the further rise of the current, a nonlinear increase of the voltage across the FCLCB occurs. The drive of the fast opening disconnecting switch (FDS) is triggered immediately after the GTO is switched OFF and opens without arcing, thus protecting the SEM from further voltage rise.

When the current finally crosses zero, it is interrupted by the switch LS. Contrary to the FTS, this has a voltage-free pause after arcing and it opens without arcing at all.

6.3.3 Thyristor based DC circuit breaker

The principal advantage of using thyristor based DCCB is the fast clearing time it can achieve as well as the high power rating it can handle. These features enable the DCCBs to clear faults without discharging the DC line capacitors in contrast with the electro-mechanical circuit breakers.

Due to the characteristic of thyristors and their inability to interrupt non-zero currents, the design of a DCCB using thyristors must incorporate a circuit capable of imposing zero current through the thyristor switch.

Many topologies have been reported in literature. In [14] the author used a forced commutated thyristor circuit for a 1000 V and 4000 A rating and in [15] a MOS controlled thyristor was used for a 300 V and 75 A rating.

The author in [21] discussed the four DCCB topologies shown in Figure 6-5. All the circuit topologies considered are based on the parallel capacitor current commutation principle. For all four circuit topologies the main thyristor T_1 carries the load current when the DCCB is closed. Figure 6-5.a shows the basic DCCB topology which achieves current interruption by turning ON thyristor T_2 when a fault is detected on the load side causing the pre-charged capacitor C to discharge into the cathode of thyristor T_1 forcing a current zero. After the thyristor T_1 has blocked, the commutation circuit formed by C, L and T_2 is interposed between the source and the fault, and following a resonant loop of current, thyristor T_2 blocks at current zero

completing the current interruption. The DCCB relies on an external power supply to pre-charge the commutation capacitor C. Because of the use of a diode D in the charging circuit, it is necessary to incorporate a high series resistor R which causes the time between an interruption and the next closing to be generally long.

The topology shown in Figure 6-5.b introduces a thyristor T_3 in place of the diode in the charging circuit. The use of the thyristor enables the charging circuit to be isolated during current interruption and hence reduces the dead-time.

The topologies shown in Figure 6-5c and Figure 6-5d permit the charging of the commutation capacitor from the DC rail and eliminate the need of an external power supply.

In the topology of Figure 6-5.c when a fault is detected thyristor T_2 is turned ON, and a resonant circuit is formed by C-T_1, T_2 / D_2-L-C, in which the capacitor voltage polarity is such that the resonant current adds to the fault current through T_1, further stressing T_1 thermally. When the thyristor T_1 blocks at current zero the commutation circuit is interposed between the source and the fault. Following a further resonant loop of current, the diode D_2 blocks at current zero and the fault interruption is complete.

The topology in Figure 6-5.d behaves in a similar manner to the topology of Figure 6-5.c, except that the problem of increased thermal stress is alleviated by arranging the positive loop of the resonant current to flow in the circuit formed by C-T_3 and L.

The negative resonant current flow in the loop C-L-D_2 and T_2 forces the fault current in the thyristor T_2 to zero.

For both of these circuits initial charging is done from the rail via C, L, and R_C. The value of R_C must be made high to ensure that the circuit current passes through zero after the commutation circuit is interposed between the source and the fault. However, this does not contribute to the DCCB dead time as at the end of a current interruption the polarity of the commutation capacitor voltage is in the correct direction to turn OFF the thyristor T_1.

In all these applications, the contactor or breaker was required to deal with source inductances as well as load inductances. Interrupting the current causes the voltage at the breaker output contacts to fall towards zero. The energy stored in the inductance of the load circuit can be dissipated by commutating it to a freewheeling diode as the output voltage attempts to go negative.

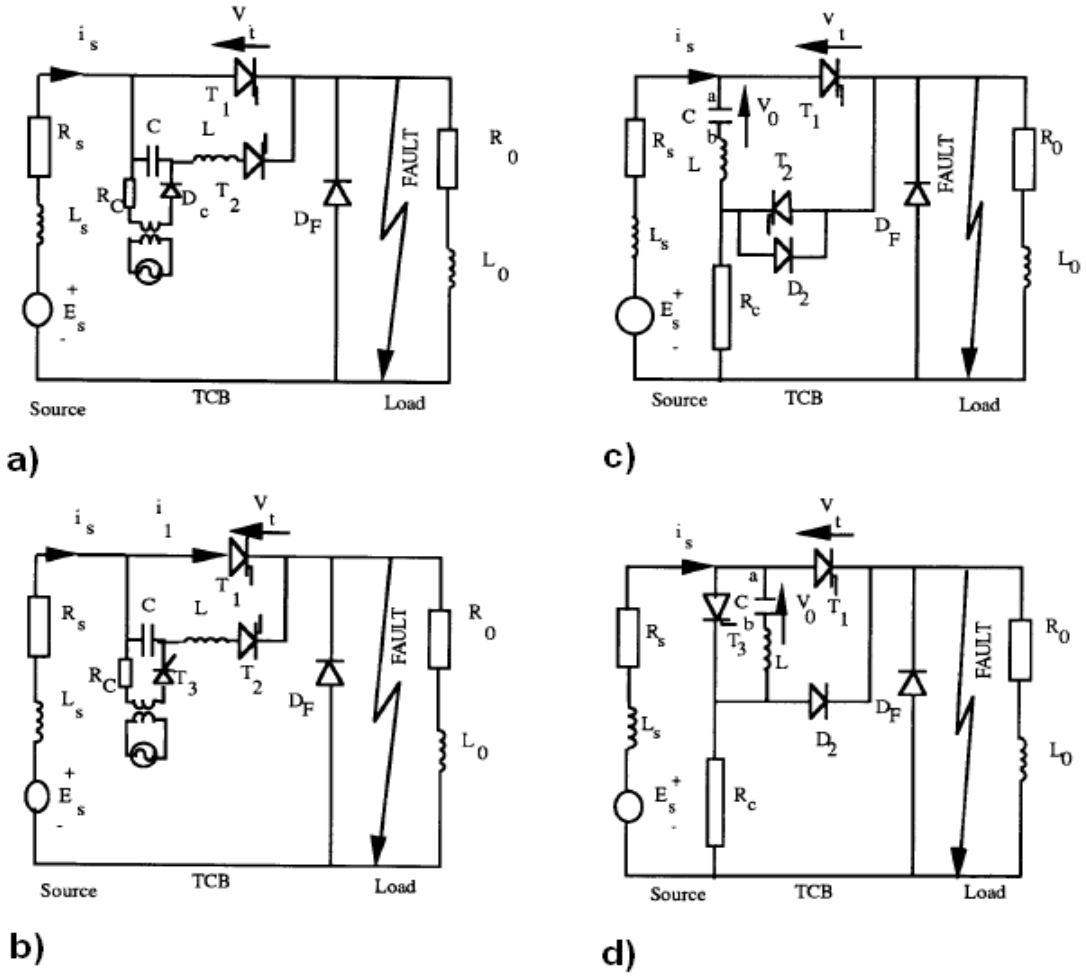

Figure 6-5: Thyristor based DCCB topologies [21]

Interrupting the source current causes the voltage across the breaker input to rise. This over-voltage must be limited to the rating of the semiconductor switches in a static breaker. There are a number of alternatives for absorbing or dissipating this energy including RC or RCD snubbers, MOVs, and the series combination of MOVs and spark gaps [14], [16]. If the source inductance is accessible, active devices can

short circuit it as the breaker opens [14]. Another alternative is to operate semiconductor switches in their active region to provide well defined over-voltage clamping [15]. Using these techniques, the clamping voltage is usually chosen to be between 1.5 and 2 times the DC supply voltage, which is a compromise between semiconductor breakdown voltages and the energy dissipated in the energy absorption components [15].

6.3.4 Commercial solutions

ABB has developed high voltage circuit breaker based on both vacuum and oil filed interrupting device. Recently, ABB has offered a DCCB that integrates sensors and protection logic. The description of this integrated DCCB from ABB is given in the next section. It is not clear who is competing with ABB on the DCCB product for HVDC application since many of the related activities might be held secret. Even patent search did not show recent activities.

6.3.4.1 ABB SACE Emax DC breaker

Integrated AC breakers have been on the market for many years. The approaches adopted, however, could not directly be transferred to the DC version. A whole range of aspects had to be fundamentally redesigned.

ABB SACE Emax DC shown in Figure 6-6 is the only breaker of its type on the market. It is opened by an electromagnetic and it is set apart by a unique mix of features and characteristics:

- Wide range of protection functions and relevant settings taking full advantage of an electronic trip unit with standard features (overload, selective and instantaneous short circuit) and advanced features under- and over-voltage, polarity unbalance, reverse power flow, zone selectivity and thermal memory). Both polarities are protected so as to detect and extinguish all possible types of fault whatever the type of distribution system.
- No need for an auxiliary power supply: all protection and measurement functions are performed in self-supply mode by means of the voltage module.
- Full integration: The trip unit, current and voltage sensors and connections are completely integrated in the breaker. The breaker is officially certified and compliant with the main shipping registers and every unit tested at production facilities.
- High electrical performance: rated currents from 800 A up to 5000 A, operating voltages up to 1000 V, rated short circuit levels up to 100 kA and rated short-time withstand current up to 100 kA.
- A complete set of measurements: currents, voltages, power, energy counter.

- A wide range of communication and automation functions: communication module with the Modbus RTU protocol and, thanks to the FieldBus Plug system, Profibus and Devicenet, Bluetooth connectivity for local configuration, programmable contacts for warning and alarm indications and load control function.

Advanced HMI and diagnostic information: graphic display, trip indicators, continuous checking of wiring integrity, hand- portable test unit, data recording for the most recent 20 trips and 80 events, and a data logger function (recording all measurements at a sampling frequency of up to 4800 Hz for 27 seconds and with a configurable trigger).

The system architecture of the new DC breaker shown in Figure 6-7 comprises:

- A shunt for current measurement and protection
- An override sensor for instantaneous back-up protection
- An electronic trip unit
- An actuator to open the breaker (trip coil).

Figure 6-6: ABB SACE Emax DC breaker

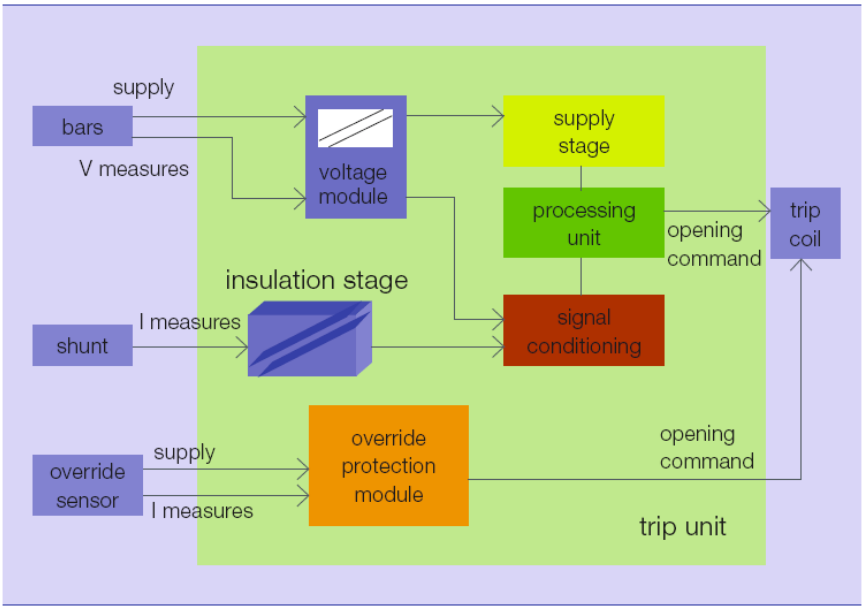

Figure 6-7: Product architecture of the circuit breaker

The trip unit uses the same architecture as the present Emax AC series. The hardware has been enhanced to meet the DC unit's higher insulation and lower signal processing requirements.

The software has been modified to measure direct current (mean value instead of RMS) and to adapt the protection algorithms to the new measuring method.

The trip unit itself is equipped with optional modules to add functionalities. Examples of these are:

- A communication module providing a galvanically insulated interface to a supervisor system.
- A signaling module equipped with contacts that can be used to drive external devices. It can also be configured as an input.

The electronic trip unit is powered from the breaker's main terminals via an integrated "voltage module," the integrated override sensor (override protection module) or an external insulated power supply (24 VDC). The voltage module also provides the voltage measurements that the trip unit requires for further signal analysis, such as power measurements, and to perform over-voltage, under-voltage and reverse power protection functions.

6.3.5 IP situation

There are a lot of patents covering this particular subject but none has covered the designs proposed in this dissertation. The most relevant of these patents are listed hereafter.

1. Solid-state DC circuit breaker US 6,952,335B2, Virginia Tech 2005
2. Commutating type DC circuit breaker arrangement US 5,402,297, Hitachi 1995.
3. Commutating type DC circuit breaker arrangement US 5,452,170, Hitachi 1995.
4. Hybrid circuit-breaker for interrupting currents having high DC components US 5,296,661, Alstom SA 1994.
5. Commutating type DC circuit breaker arrangement EP 0556616 A1, Hitachi 1993.
6. High tension DC current-limiting circuit breaker US 5,121,281, GEC Alstom SA 1992.
7. Solid-state trip unit for DC circuit-breakers US 4,956,741, Westinghouse Electric Corp 1990.
8. Driving apparatus for DC circuit breakers US 4,862313, Hitachi 1989.
9. DC circuit breaker US 4,618,905, Hitachi 1984.

10. DC Circuit Breaker apparatus US 4,458,121, Tokyo Shibaura Denki Kabushiki 1984.

11. High-voltage DC circuit breaker apparatus US 4,578,730, Hitachi 1983.

12. DC Circuit Breaker apparatus US 4,442,469, Tokyo Shibaura Denki Kabushiki 1982.

13. DC circuit breaker US 4,216,513, Hitachi 1978.

14. Voltage dividing DC circuit breaker and method, US 3,777,179, Hughes Aircraft Company 1973.

6.4 Proposed DC circuit breaker designs

Thyristor switches are the most used for high voltage and high power applications, a DCCB using thyristors would be reliable and economically viable. In the following sections, I discuss two topologies for realizing a DCCB with thyristors as the main switching devices.

The first topology describes a unidirectional DCCB used in applications where current is not supposed or allowed to be reversed as it is the case with conventional HVDC links. The inductance can be omitted or reduced to a minimal value of the link where the DCCB has enough inductance.

The second topology derived from the first one uses a Graetz circuit formed by diodes so the current inside the breaker flows always in the same direction even when the power flow is reversed. This permits the use of a single inductor that will not oppose a sudden change in current direction. More details in this topology are provided in subsequent sections of this chapter.

In both topologies a visible disconnect switch is added to ensure physical isolation and comply with safety regulations.

6.4.1 Unidirectional DC circuit breaker

The proposed topology for a unidirectional DCCB presented in Figure 6-8 includes one surge arrestor, one inductor, one capacitor, one diode, and three thyristor switches. The additional mechanical switch is optional and does not interfere with the normal operation of the breaker. It is added to remove concern of certain utilities over the galvanic isolation capability of thyristors and also because some regulations dictate a visible disconnection before any line can be serviced.

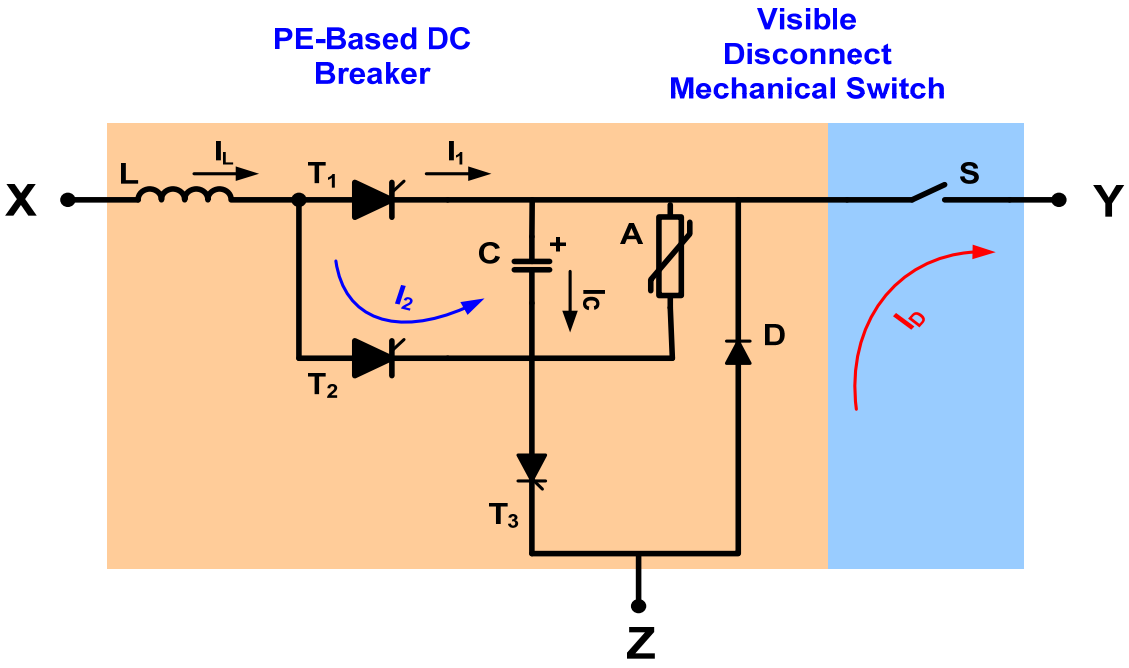

Figure 6-8: Novel unidirectional DCCB using thyristors

Due to the placement and orientation of the thyristor switches and the diode, there are six possible paths for the current to flow between points X, Y, and Z. By assuming the switch S does not exist and point Y is directly connected to the DCCB, I obtain the following paths:

- Path #1: from X to Y through inductance L, and thyristor T_1
- Path #2: from X to Y through inductance L, thyristor T_2, and capacitor C
- Path #3: from X to Z through inductance L, thyristor T_1, capacitor C, and thyristor T3
- Path #4: from X to Z through inductance L, thyristors T_2, and thyristor T_3

- Path #5: from Y to Z through capacitor C, and thyristor T_3
- Path #6: from Z to Y through diode D

Note that path #4 shorts the source at point X and can not be cleared. Therefore, path #4 will not be considered.

6.4.1.1 Circuit analysis

To understand the operation of the DCCB, I consider a simple circuit containing a single DC source, a resistor, and an inductor representing line and load impedances. I assume the mechanical disconnect switch in a closed position and all initial conditions to be null. The thyristor switches are represented by a red or green line reflecting ON or OFF states respectively.

To first energize the DCCB, thyristors T_1 and T_3 receive a continuous trig signal pushing them into conduction (ON state) as shown in Figure 6-9. This would present the current with two paths; a path from X to Z that will charge the capacitor C and a path from X to Y that will feed the load. When the capacitor is completely charged, the current through T_3 becomes null and the thyristor stops conducting.

When a fault is detected on the Y side, the triggering pulses of thyristor T_1 and T_3 are removed and T_2 is triggered with a short pulse. The capacitor is now in parallel with T_1 and forces a current through thyristor T_2. The inductance L will oppose sudden changes of the current I_L; therefore, the forced current I_2 has to come out of

I_1. If the capacitor was dimensioned correctly, than the current I_2 will be big enough to nullify I_1 and thyristor T_1 will be blocked. As I_2 flows to the fault, the capacitor C charges and causes I_2 to decrease until its value reaches zero.

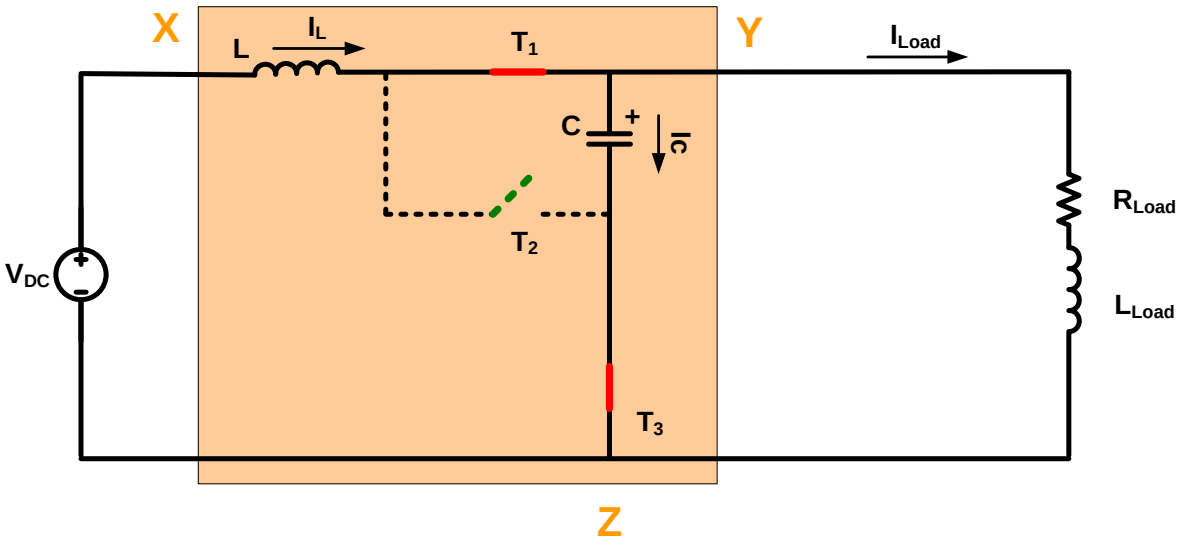

Figure 6-9: Configuration for normal operation

The sequence of transferring the current from T_1 to T_2 and blocking both T_1 and T_2 can happen in as little as 300 us. This would isolate any source connected in point X from the fault but is not enough to completely dissipate the energy stored in system inductances; therefore, a route for fault current is provided through the freewheel diode D as shown in Figure 6-10. Once the fault current is zero, the disconnect switch is operated to indicate an open circuit. The fault is then completely isolated from the source at point X. The philosophy used to interrupt the current uses zero

current switching or soft switching and does not produce any oscillations in voltage or current.

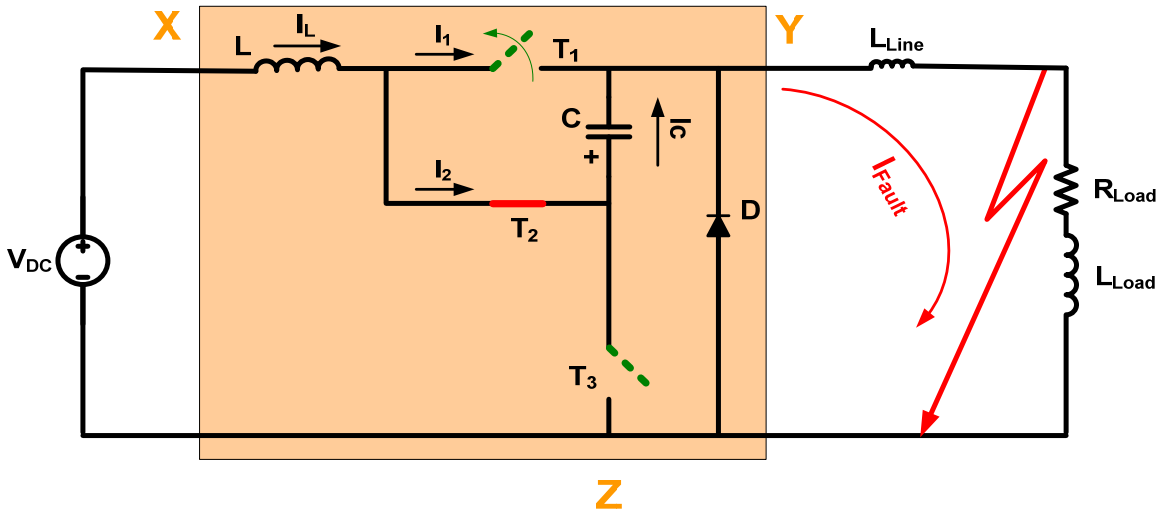

Figure 6-10: Configuration during fault

6.4.1.2 Transient performance

The DCCB is intended for DC applications rated at 320 kV and 3000 A. Therefore, to assess its performance, the ratings of all the components used in the design should be determined and applied to the test circuit shown in Figure 6-11. The test circuit consists of the following three modules:

1. On the left side, the power source is modeled as an infinite DC source behind a resistor. The resistor is used to simulate the voltage drop at the input of the DCCB and to quantify the impact of a fault on the DC bus voltage. The value of

the source voltage is set at 320 kV and a voltage drop of around 1.0% at 3000 A is represented by a resistance of 1.0 Ω.

2. On the right side, the line or cable is modeled as a lumped resistor in series with an inductor and the load is modeled as a lumped resistor in series with an inductor. The line inductor is used to verify the operation of the freewheel diode in providing a path for dissipating stored energy when the main source is isolated. The value of the line inductance is set to 0.3 mH. The sum of resistances of the line, the conducting thyristors, and the connectors is set to 0.5 Ω. The load resistor is used to limit the current in normal operation to its rated value of 3000 A. Therefore, the value of the resistive load is set to 105.17 Ω making the total resistance from source to load equal to 106.67 Ω.

3. In the center with a yellow background, the model of the unidirectional DCCB is shown. The model includes an inductor, a capacitor, a diode, three thyristors, and an arrester. The arrestor is placed across the capacitor to protect it from over-voltage during faults. The arrester has 4 columns. Each column is rated at 10 kA for a total current rating of 40 kA. The voltage level of the arrester is chosen to be 25% higher than the source voltage (320 kV * 1.25 = 400 kV).

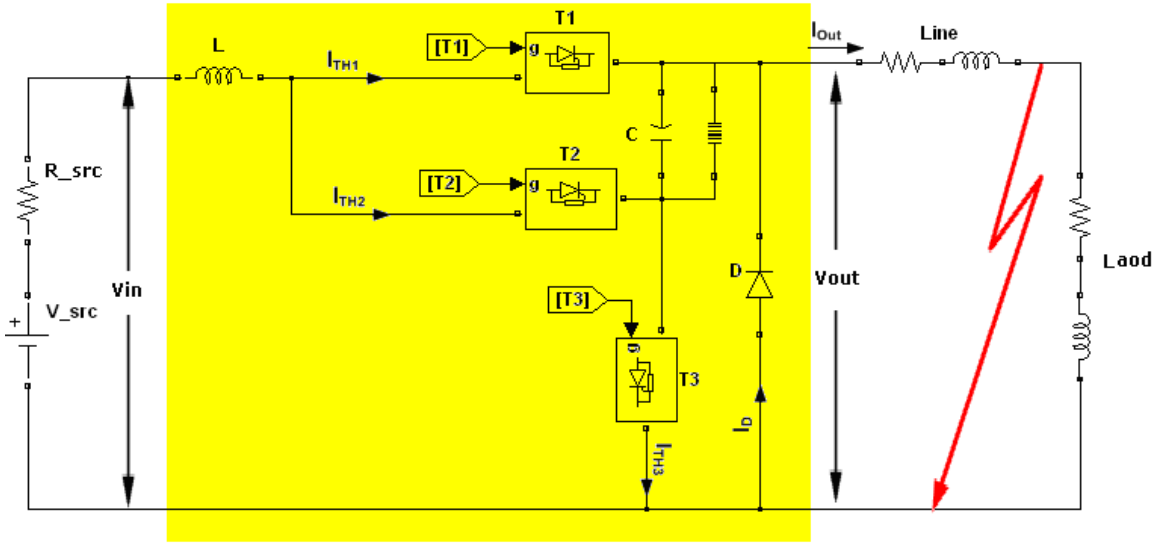

Figure 6-11: Simulation circuit using MATLAB®

6.4.1.2.1 Rating of the inductor

When a fault is applied in the location shown in Figure 6-11, the model is reduced to its equivalent circuits presented in Figure 6-12 where L represents all the inductances and R all the resistances except for the load that is shorted. In our case R is the sum of source resistance, line resistance, and DCCB internal resistance. The value of R is set at 1.5 Ω. Before detecting the fault, thyristor T_2 is open and the simulated circuit is reduced to a simple RL network where the only path for the current is through thyristor T_1. The general solution for the current of an RL circuit is given in (6-1) with k a constant that depends on the initial value of the current i(t).

$$i(t) = \frac{V}{R} + k e^{-\frac{R}{L}t} \qquad (6\text{-}1)$$

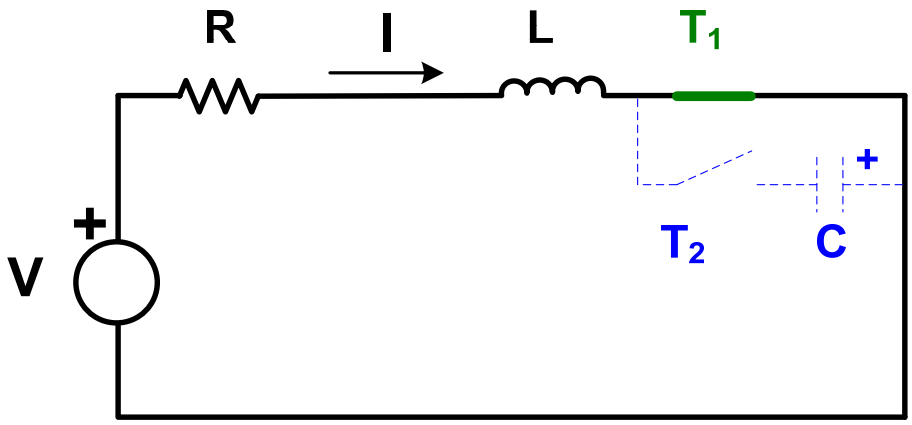

Figure 6-12: Equivalent circuit of the DCCB during fault

From equation (6-1) the maximum short-circuit current level is limited by the value of resistor R which is system related and can not be changed. For the value of R fixed before at 1.5 Ω, The maximum fault current is 213.3 kA. This value is very big and should be limited to values a commercial thyristor can handle. One way of limiting the fault current is to interrupt it while its value is still low as illustrated in Figure 6-13.

The figure shows three traces of currents. The red trace represents the current through inductance L and is denoted i_L, the green trace represents the current through thyristor T_1 and the blue trace represents the current through thyristor T_2 in series with the capacitor C. Thyristor T_1 and T_2 currents are denoted i_{T1} and i_{T2}

respectively. When the RL circuit is first energized, the current i_L is equal to i_{T1} and rises exponentially following the dashed red line in Figure 6-13. However, if at time τ_1 thyristor T_2 is switched ON and inserted the capacitor in the circuit then the current with a value i_1 commutates to the lesser resistive path provided by this capacitor that is initially charged in reverse polarity. The current through T_1 becomes null and the thyristor turns OFF. Now the inductor current i_L flows through the capacitor and is the same as i_{T2}. As the capacitor charges, its current diminishes and becomes null at time τ_2. Therefore, the source current is limited to i_1 and becomes null at time τ_2.

By defining the maximum allowable value for the current through thyristor T_1 to be i_1 and by setting the current commutation time to τ_1, I can calculate a value for the inductance L that satisfies these requirements.

The maximum time for detecting and clearing the fault is a function of the hardware and software used to detect and clear the fault. In any event and especially when using solid state switches a time lower than 1 ms is targeted for clearing a DC fault. The detection of the fault can be performed in as fast as 100 μs using digital or analog circuits. In our case, I fix the maximum clearing time at 1 ms and the

detection time at 200 μs. If the system could detect and clear the fault in a faster time than the outcome will be better in terms of maximum current to interrupt and mitigating the DC voltage dip.

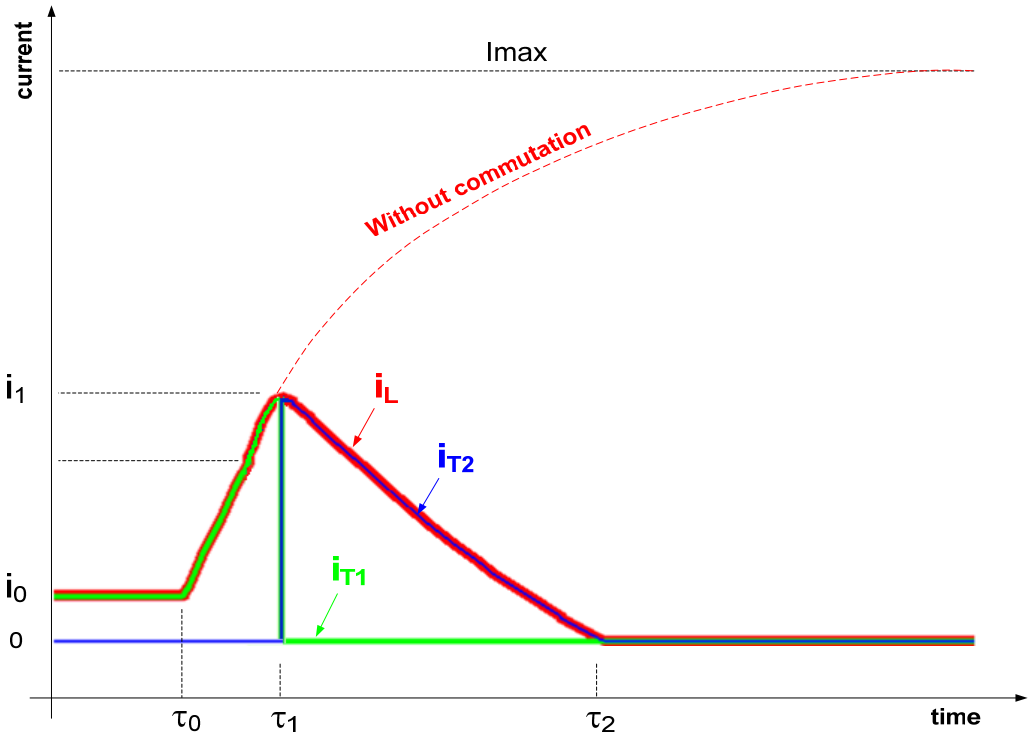

Figure 6-13: Current waveforms during commutation from T_1 to T_2

The maximum allowable value for the fault current is contingent to the capability of the switches in handling such current and the allowable DC voltage drop at the input of the DCCB. Based on the source resistance fixed before at 1.0 Ω, a 10% decrease of the DC voltage at the input of the DCCB corresponds to 32 kV. This represents

the voltage drop across the source resistor when 32 kA passes through it. For our calculation a current of 10 pu = 30 kA will be used.

By considering the system running at rated voltage and current before the fault occurs and setting i_o as the initial condition for the current, I can calculate the constant k in equation (6-1) and obtain a new expression of the current as shown in equation (6-2).

$$i(t) = \frac{V}{R} + (i_o - \frac{V}{R}) e^{-\frac{R}{L}t} \qquad (6\text{-}2)$$

With the initial current value i_o equals to the rated current of 3000 A, the detection time ($\tau_1 - \tau_0$) set at 200 μs, the current i_1 at time τ_1 set at 30 kA, the source voltage fixed at 320 kV, and the total resistance fixed at 1.5 Ω, I can solve for the inductance and obtain L = 2.18 mH. This inductance represents the inductance of the DCCB and that of the line. The inductance of the DCCB alone is 1.88 mH and is obtained by subtracting 0.3 mH from the calculated 2.18 mH inductance.

$$i(t) = \frac{V}{R} + (i_o - \frac{V}{R})\, e^{-\frac{R}{L}t}$$

$$i_1 = \frac{V}{R} + (i_o - \frac{V}{R})\, e^{-\frac{R}{L}(\tau_1 - \tau_0)} \Rightarrow L = -\frac{R \times (\tau_1 - \tau_0)}{\ln(\frac{R \times i_1 - V}{R \times i_o - V})}$$

$$\left| \begin{array}{l} V = 320\,\mathrm{kV} \\ R = 1.5\,\Omega \\ \mathrm{ibase} = 3\,\mathrm{kA} \\ i_1 = 10\,\mathrm{pu} = 30\,\mathrm{kA} \\ \tau_1 - \tau_0 = 200\,\mu\mathrm{s} \end{array} \right. \Rightarrow L = -\frac{1.5 \times 0.0002}{\ln(\frac{1.5 \times 30 - 320}{1.5 \times 3 - 320})} = 2.18\,\mathrm{mH} \qquad (6\text{-}3)$$

$$L_{DCCB} = L - L_{line} = 2.18 - 0.3 = 1.88\ \mathrm{mH}$$

6.4.1.2.2 Rating of the capacitor

Now that I have derived a formula to calculate the inductance L, I need to derive a formula to calculate a value for the capacitor C. The calculated capacitor should be able to carry at least the current i_1 initially flowing through the inductor L. In theory, the capacitor current is only limited by the resistance of the circuit where it is connected. Therefore, when a capacitor is subjected to a voltage step its current value tends to infinity. In practice, each capacitor has a maximum dv/dt due to

internal resistances and inductances. The value of dv/dt depends on the capacitor designs and building materials and is available in manufacturer's datasheets.

From the thyristor datasheet presented in appendix C.2, the value of the critical current rise (di/dt) is 1000 A/μs. Since a good design allows at least 30% safety margin I considered a di/dt of only 700A/μs. Therefore, at least 30 kA/(0.7 kA/μs) = 42.86 μs is required to commutate 30 kA between T_1 and T_2. During this time interval, the capacitor voltage should go from –320 kV to +320 kV. Therefore, a maximum dv_c/dt of 640 kV/43.86 μs = 14.9 kV/μs is needed. The selected capacitor should at least have the capability of handling a voltage buildup with the calculated rate. With the dv_c/dt known, I calculate a value of C as shown in equation (6-4).

$$\frac{dv_c}{dt} = \frac{1}{C} i_c(t) \Rightarrow C = \frac{dt}{dv_c} i_c(t)$$

$$\left| \begin{array}{l} \dfrac{dv_c}{dt} = 14.9\,\text{kV}/\mu\text{s} \\ i_c(\tau_1) = i_1 = 30\,\text{kA} \end{array} \right. \Rightarrow C = \frac{dt}{dv_c} i_1 = \frac{30\,\text{kA}}{14.9\,\text{kV}/\mu\text{s}} = 2.01\mu\text{F} \qquad (6\text{-}4)$$

The calculated capacitor should also withstand a DC voltage of 400 kV and a transient voltage of 720 kV. The 720 kV value comes from the fact that the capacitor can be charge at -400kV and then connected to +320 kV.

6.4.1.2.3 Rating of the diodes, thyristors and snubbers

In order to keep this section short, I decided to report the details of rating the power electronic devices and their snubbers in section 6.5. In that section I use common design practices to choose the proper thyristor or diode to use and I define the working voltages based on safety margins. I also outline calculation of individual snubber parameters and provide advices with respect to gate drive design.

6.4.1.2.4 Simulation results

With the model parameters known, I simulated the DCCB shown in Figure 6-11 using MATLAB® Simulink® software and the test circuit presented in Figure 6-14. The parameters used to perform the simulation are summarized in Table 6-1. I set the fault application time at 20 ms and the fault detecting speed at 200 μs which can be achieved easily using on-the-shelf controller equipments. All other parameters in the table were defined earlier in the text.

The results of the simulation are converted in pu values using a voltage base of 320 kV and a current base of 3 kA. The voltage profiles of the source voltage V_{src}, the input voltage V_{in}, the output voltage V_{out}, and the capacitor voltage V_{cap} are shown in Figure 6-15. In the first frame of the figure, the source voltage shown in blue is constant because it represents an infinite source. The green trace represents the

voltage at the input of the DCCB immediately after the source impedance. The fault current starts building up at 20 ms and cause a maximum voltage drop of 11%.

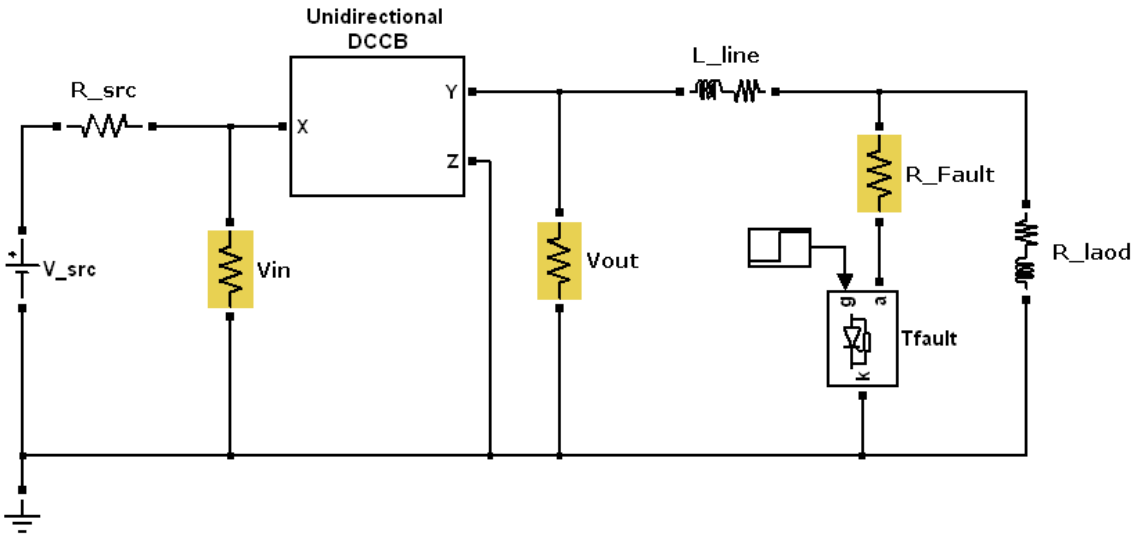

Figure 6-14: Setup for simulating the unidirectional DCCB

Table 6-1: Parameters of the DCCB used for simulation

Parameters		Value	Unit
Source			
	V_src	320	kV
	R_src	1.00	Ω
DCCB			
	L	1.88	mH
	C	2.01	μF
	Snubber Resistor	2684	Ω
	Snubber Capacitor	0.0385	μF
	Arrester protection voltage	400	kV
	Arrester current rating	40	kA
Line/Cable			
	L_line	0.30	mH
	R_line	0.50	Ω
Load			
	R_Load	105.17	Ω
	R_fault	0.15	Ω
Fault			
	Application time	20	ms
	detection time	200	μs

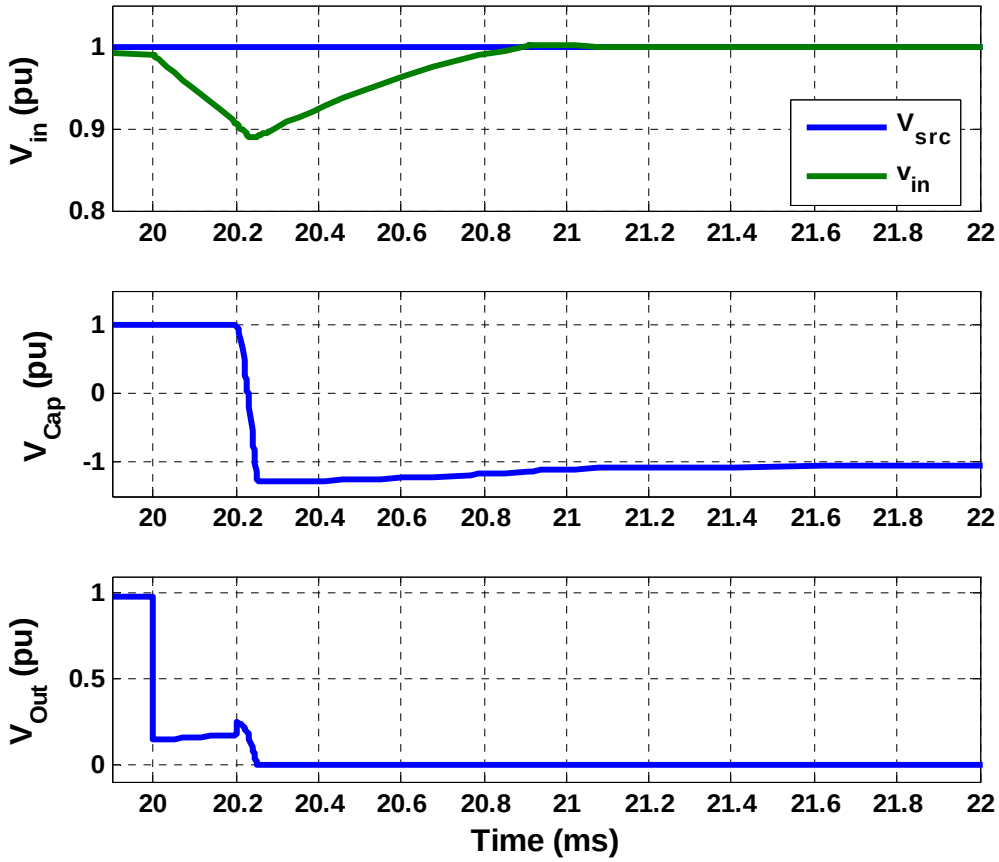

Figure 6-15: Voltage profiles during a DC fault

The second graph in Figure 6-15 shows the voltage profile across the capacitor during a fault. Initially, the capacitor was charged to +1.0 pu which corresponds to the rated system voltage. When the fault is detected and thyristor T_2 is switched ON inserting the capacitor in the path of the fault, the polarity with which the capacitor was initially charged makes the difference of potential across T_2 equals 2.0 pu; twice

the voltage across T_1. Therefore, the current is forced to flow through the capacitor and starts charging it to a reverse polarity. The voltage goes from +1.0 pu to -1.0 pu with an overshoot that is dissipated by the arrester placed in parallel with the capacitor.

The third graph in the figure displays the voltage V_{out} at the output of the DCCB which corresponds to the voltage at the point where the fault is applied. The transition of the voltage value from +1.0 pu to near zero indicates that the fault is initiated at 20 ms. The voltage does not go completely to zero in the beginning because of the fault impedance that creates a small voltage drop seen between 20 and 20.2 ms. This voltage drop increases during the switching of the capacitor due to the contribution of the capacitor current to the fault.

In Figure 6-16, I show the commutation of the current from thyristor T_1 to thyristor T_2. The thick trace displayed in green represents the current i_L in the inductor, the trace with medium thickness displayed in red represents the current in thyristor T_1, and the thin trace displayed in blue represents the current in thyristor T_2.

Before the fault is initiated, the current i_L flows to the load through T_1 and its value is equal to +1.0 pu ($i_L = i_{T1} = +1.0$ pu). When the fault is initiated at 20 ms, both currents rise to feed the fault. At 20.2 ms, the protection algorithm detects the fault and

initiates a control command to switch ON thyristor T_2. This causes the capacitor to be inserted in the fault path and its inrush current forces the current to flow through T_2. At this moment, the current i_L passes through T_2 as indicated by the green and blue traces while the current i_{T1} becomes null. The inductive current is then completely transferred from T_1 to T_2. As the capacitor charges, its current reduces until it reaches zero around 20.9 ms. The current in the inductor is now null meaning that the source is galvanically isolated from the fault. This does not imply that the fault current is also null because some stored energy in the line inductance needs to be dissipated as shown in Figure 6-17.

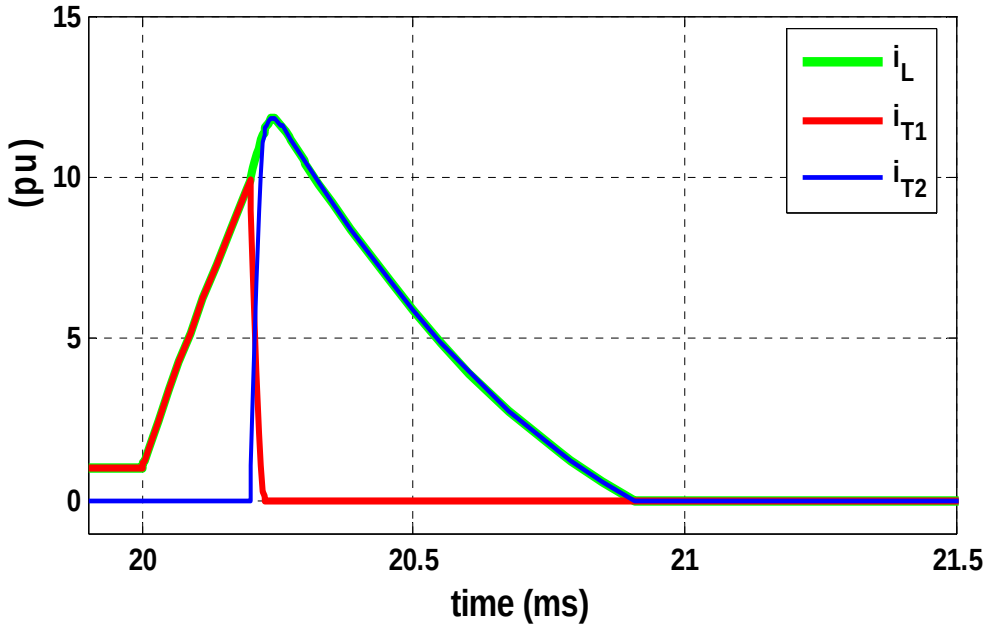

Figure 6-16: Current commutation between thyristors T_1 and T_2

In Figure 6-17 I reproduced the inductor current i_L and added the fault current i_{fault} and the freewheel diode current i_D in order to explain the mechanism with which the stored energy in the line inductance is dissipated. As I had explained in the previous paragraphs, the current i_L is forced to zero by the capacitor and the rate with which it reaches zero depends on how fast the capacitor charges and reaches the voltage V_{in}. This dynamic imposed by the capacitor on i_L can be different from that imposed by the line inductance on i_{fault}. Consequently the values of I_L and I_{fault} differ at a certain point of time and the difference is supplied through the freewheel diode that provides a path for the fault current to flow until it becomes null.

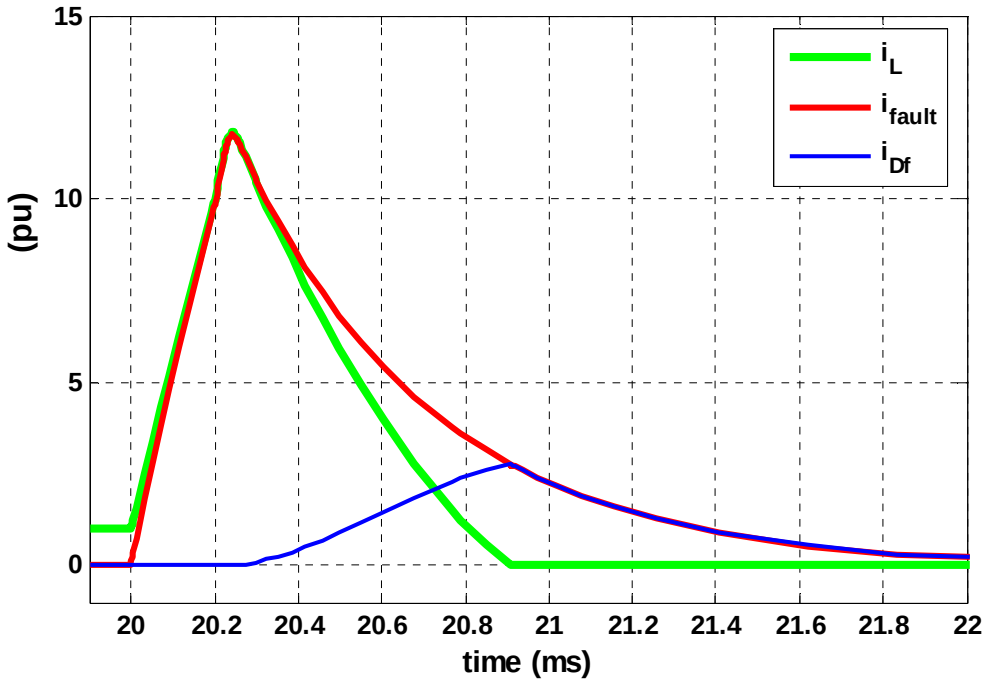

Figure 6-17: Dissipation of the stored energy through the freewheel diode

The duration of conduction of the diode and the amplitude of its current are function of the resistance and the inductance of the line. The inductance determines the amount of stored energy and the resistance determines how fast this energy can be dissipated.

6.4.2 Bidirectional DCCB

The unidirectional DCCB presented in the previous sections can be mounted in anti-parallel configuration and provide bidirectional functionality for applications requiring power reversal. However, the presence of the inductance in the unidirectional model

of the DCCB opposes any sudden change of current and limits the rate at which power reversals can be achieved. Nevertheless, that inductance is critical to limit voltage drop and prevent DC bus capacitors from discharging. The problem facing applications of DC bus collectors in wind farms or in multiterminal HVDC-Light® topologies remains the fast protection against DC faults and the ability to handle quick DC power reversals. This problem is more apparent in the case of a DC ring where current can instantly change direction due to configuration, load, or supply changes. Here again, the challenge is not only to detect and isolate the fault but to do it without incurring big DC voltage drops or blocking any of the converter stations connected to the DC ring.

Proposed design

In this section, I propose another novel design for a DCCB using thyristors and diodes that is capable of clearing DC faults without discharging DC bus capacitors or opposing quick power reversals. The proposed bidirectional DCCB topology is shown in Figure 6-18 and comprises one inductor, one capacitor, one surge arrestor, three thyristors, and five diodes. Four of the five diodes form a Graetz circuit so only one inductor is needed whether the DC current flows from X to Y or Y to X. The fact that the current through the inductor does not change polarity allows instantaneous

changes in the current flow between X and Y. This is particularly critical for applications using VSCs where the power flow can change direction very quickly.

To explain the operation for this topology, I consider a current flowing from point X to Point Y in the model shown in Figure 6-18. The only path that the DC current can take is the one formed by D_1, L, T_1, D_2, and S. Also, every time a current flows through T_1, the capacitor gets charged through thyristor T_3 until its voltage reaches the cathode voltage of T_1. During a DC fault on the Y side, the pulse of thyristors T_1 is turned OFF and thyristors T_2 is triggered. This causes the capacitor to suddenly discharge through point Y which forces all the current to flow through T_2 and allows T_1 to block. Then the capacitor charges in reverse polarity until the current in T_2 decreases to zero and the thyristor blocks. In meantime any imbalance between inductor current and fault current flows through the diode D_F as long as the stored energy in the system is not completely dissipated. The operation for current flowing from Y to X is similar to the one just described with the path being formed by S, D_3, L, T_1, and D_4. The role of the disconnect switch is to visibly show an open contact and to ensure physical and not only galvanic fault isolation.

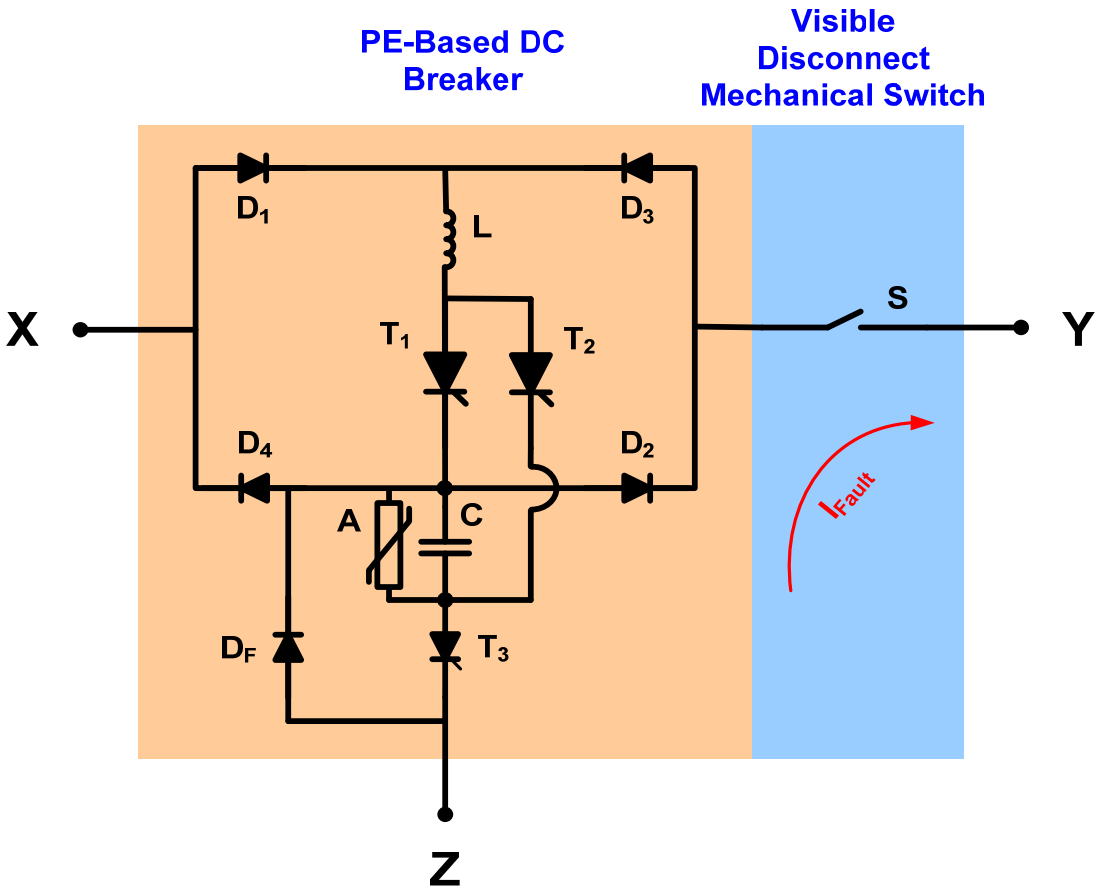

Figure 6-18: Novel bidirectional DCCB using thyristors

I have described the principle of operation of the DCCB when I introduced the unidirectional model. I have calculated values for C and L that provide a total clearing time less than 900 μs and that cause no more than 11% voltage drop under the most severe DC fault. The values of C and L will be used with the bidirectional model to simulate its transient behavior and compare it to that obtained with the unidirectional model.

Using MATLAB® Simulink®, I modeled the bidirectional DCCB using standard building blocks for thyristors, diodes, surge arrester, and other passive elements as shown in Figure 6-19. The surge arrestor that is connected across the capacitor to protect it from over-voltage has the same rating as the one used earlier with the unidirectional DCCB. I also used the parameters provided in Table 6-1 to perform three simulation cases. The first two cases simulate DC faults on the X and Y sides respectively and the third case demonstrates the power reversal handling of the DCCB.

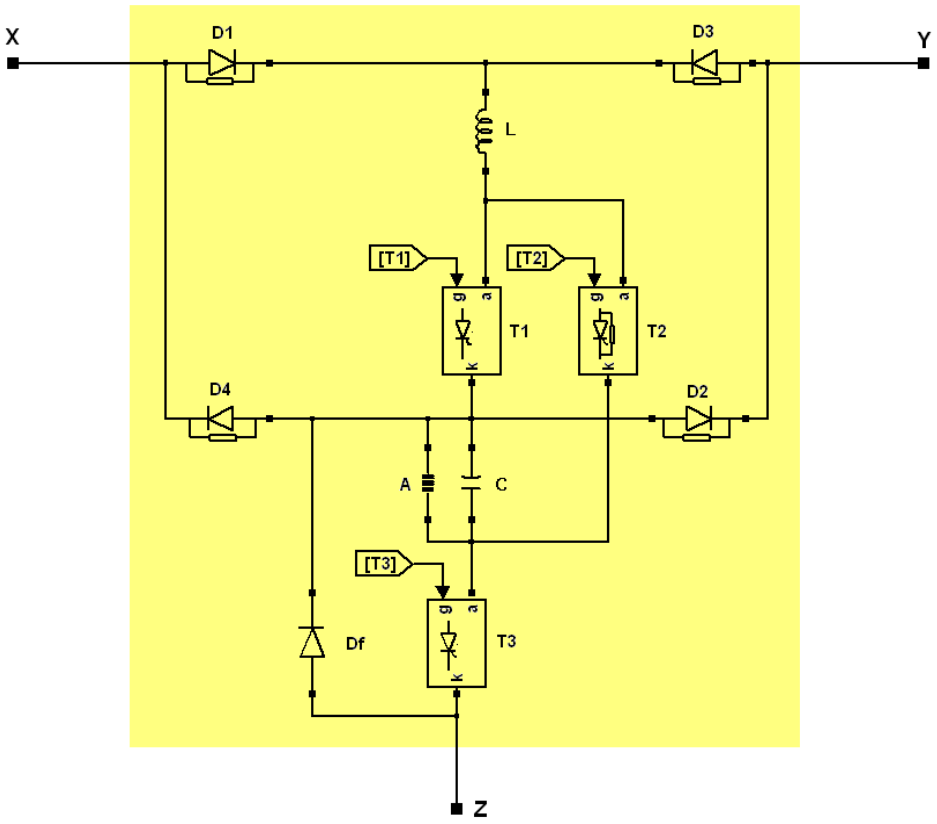

Figure 6-19: Model of the bidirectional DCCB

6.4.2.1 Case 1: DC fault at point X

To perform the first test case I used the circuit of Figure 6-20 where I connected the source to point Y, the load to point X, and point Z to the ground. Then I applied a solid DC fault between the load and the line inductance. The choice of this fault location results in stored energy in line inductance that will be dissipated through diode freewheel D_f of the DCCB. The results of the simulation for the first case are shown by the four graphs of Figure 6-21.

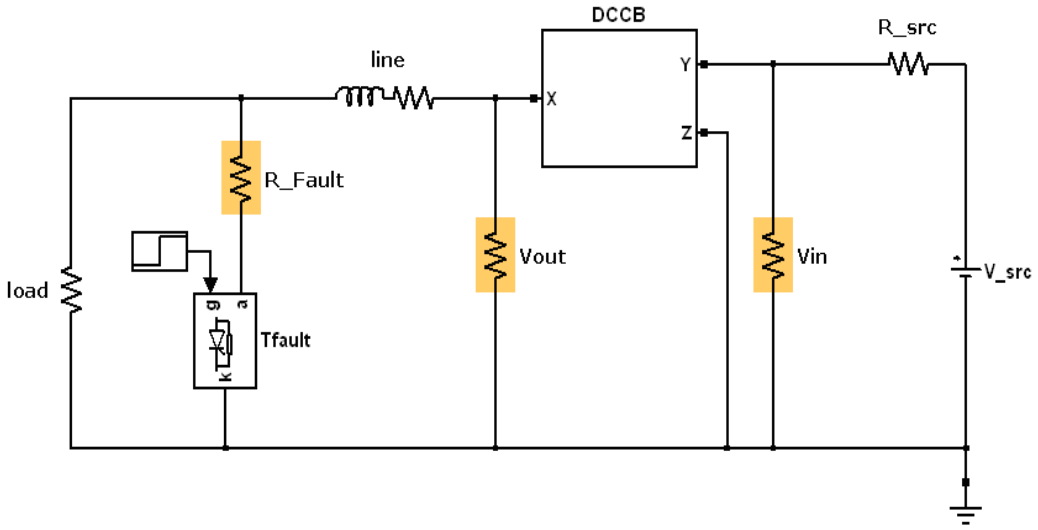

Figure 6-20: Setup for simulating a DC fault at point X

The first two graphs depict waveforms representing the currents in all five diodes D_1 through D_4 and D_f. In this case, the current flows from point Y to point X using the path provided by diodes D_3 and D_4. Therefore, currents of these two diodes are not null but those of non conducting diodes D_1 and D_2 are null.

It can be seen from the results that the currents in diodes D_3 and D_4 cease to be identical when the current i_L of the inductor commutates fromT_1 to T_2. From that instant, the current in D_3 becomes the same current flowing through the capacitor that decreases exponentially as the capacitor charges. This current becomes null around 20.9 ms. Diode D_4 carries the fault current that decreases with a slower rate

than the capacitive current due to the inductance of the line. The difference between capacitive and fault current is provided from the ground through the freewheeling diode D_f.

The third graph of the figure has three signals representing currents in the inductor, in thyristor T_1, and in thyristor T_2. The purpose of this graph is to show the successful commutation of current i_L from T_1 to T_2 as I explained in sections 6.4.1.1 and 6.4.1.2 when I analyzed the circuit and transient performance of the unidirectional DCCB.

The forth graph depicts the correlation between fault current, inductive current, and diode currents. This graph shows the role of the freewheel diode D_f in providing a path for fault current when the power source is isolated from the fault. Without this diode, the circuit will not function properly and a huge dv/dt across the inductor will appear and may destroy the DCCB. Identical results were obtained with the unidirectional DCCB where detailed analysis is provided in sections 6.4.1.1 and 6.4.1.2.

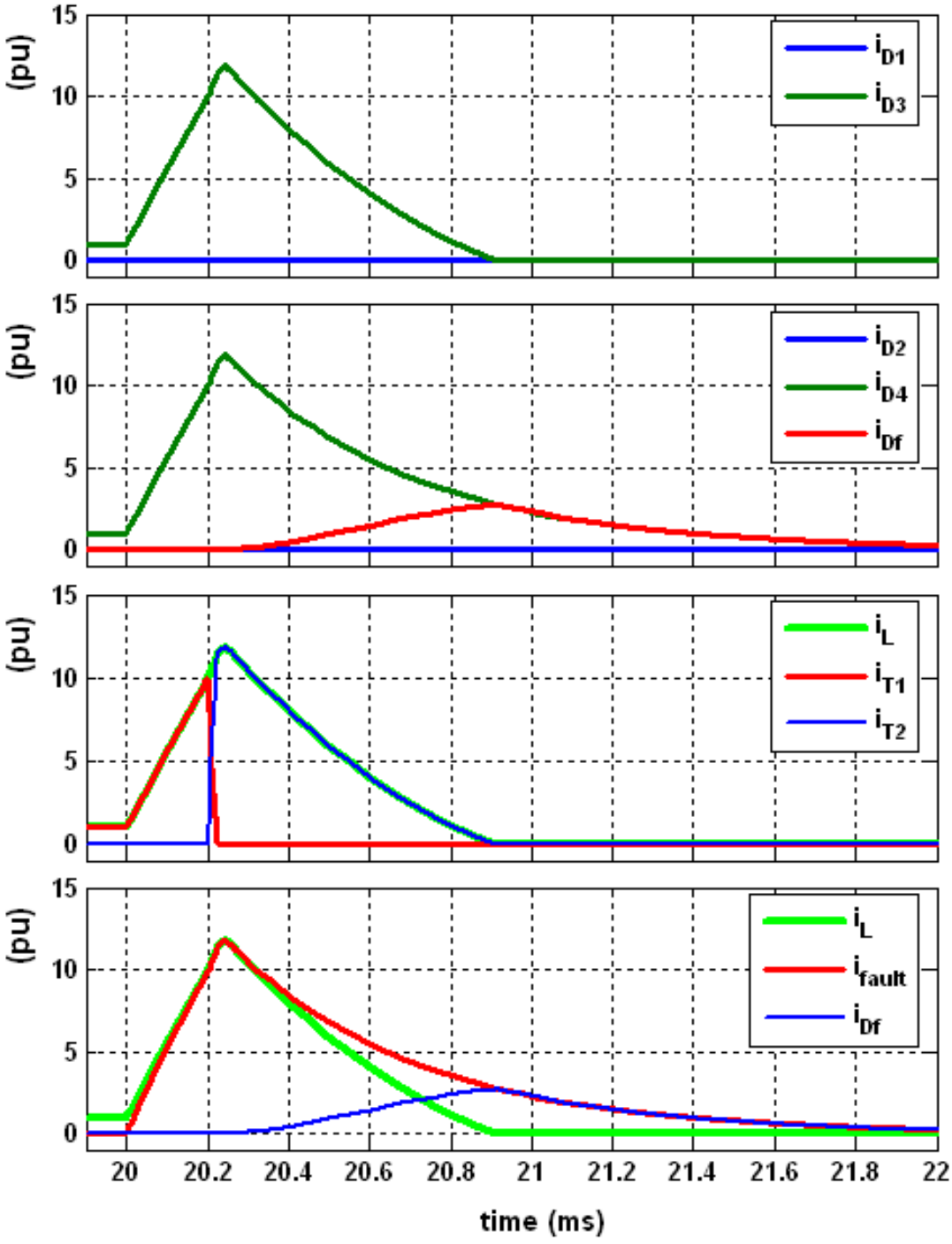

Figure 6-21: Waveforms for a DC fault at the X side of the DCCB

6.4.2.2 Case 2: DC fault at point Y

To perform the second test case I used the circuit of Figure 6-22 where I connected the source to point X and the load to point Y. Point Z is connected to the ground as before. Similar to the previous case, I applied a solid DC fault between the load and the line inductance and reported the results in Figure 6-23.

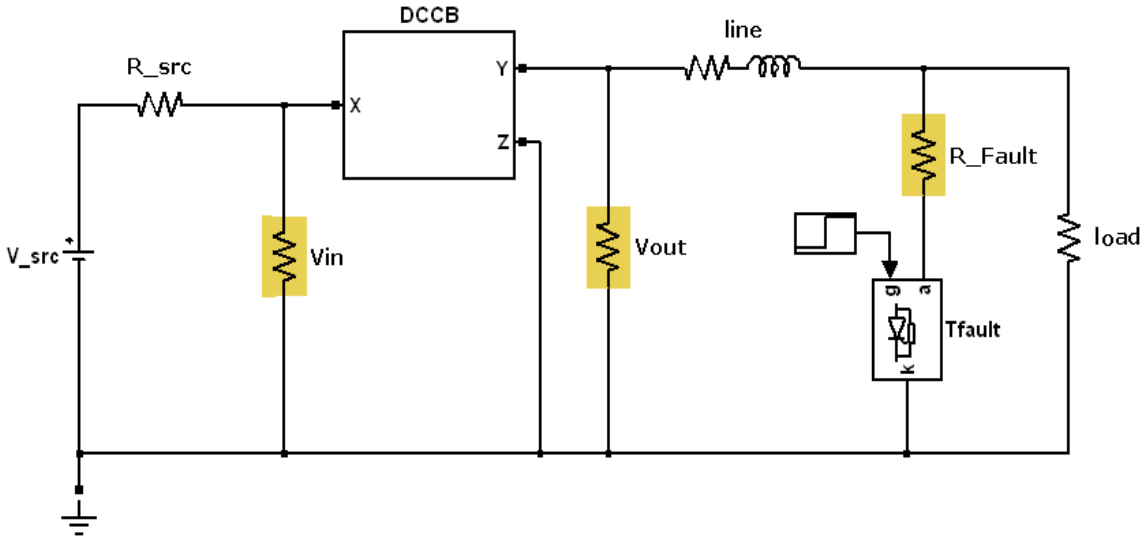

Figure 6-22: Setup for simulating a DC fault at point Y

The purpose of this test case is to show that the performance of the DCCB in clearing the DC fault is the same whether the fault occurs in point X or in point Y. This identical performance is easily verified by comparing graphs 3 and 4 of Figure 6-21 and Figure 6-23.

The first two graphs show waveforms representing the currents in all five diodes D_1 through D_4 and D_f. In this case, the current flows from point X to point Y using the path provided by diodes D_1 and D_2. Therefore, currents of these two diodes are not null but those of non conducting diodes D_3 and D_4 are null.

Similar to the previous test case, the currents in diodes D_1 and D_2 cease to be identical when the current i_L of the inductor commutates fromT_1 to T_2. From that instant, the current in D_1 becomes the same current flowing through the capacitor that decreases exponentially as the capacitor charges. This current becomes null around 20.9 ms. Diode D_2 carries the fault current that decreases with a slower rate than the capacitive current due to the inductance of the line. The difference between capacitive and fault current is still provided from the ground through the freewheel diode D_f. One important remark is that the direction of the current i_L in the inductor is the same for both cases which will play a critical role in the third test case where power reversal is simulated.

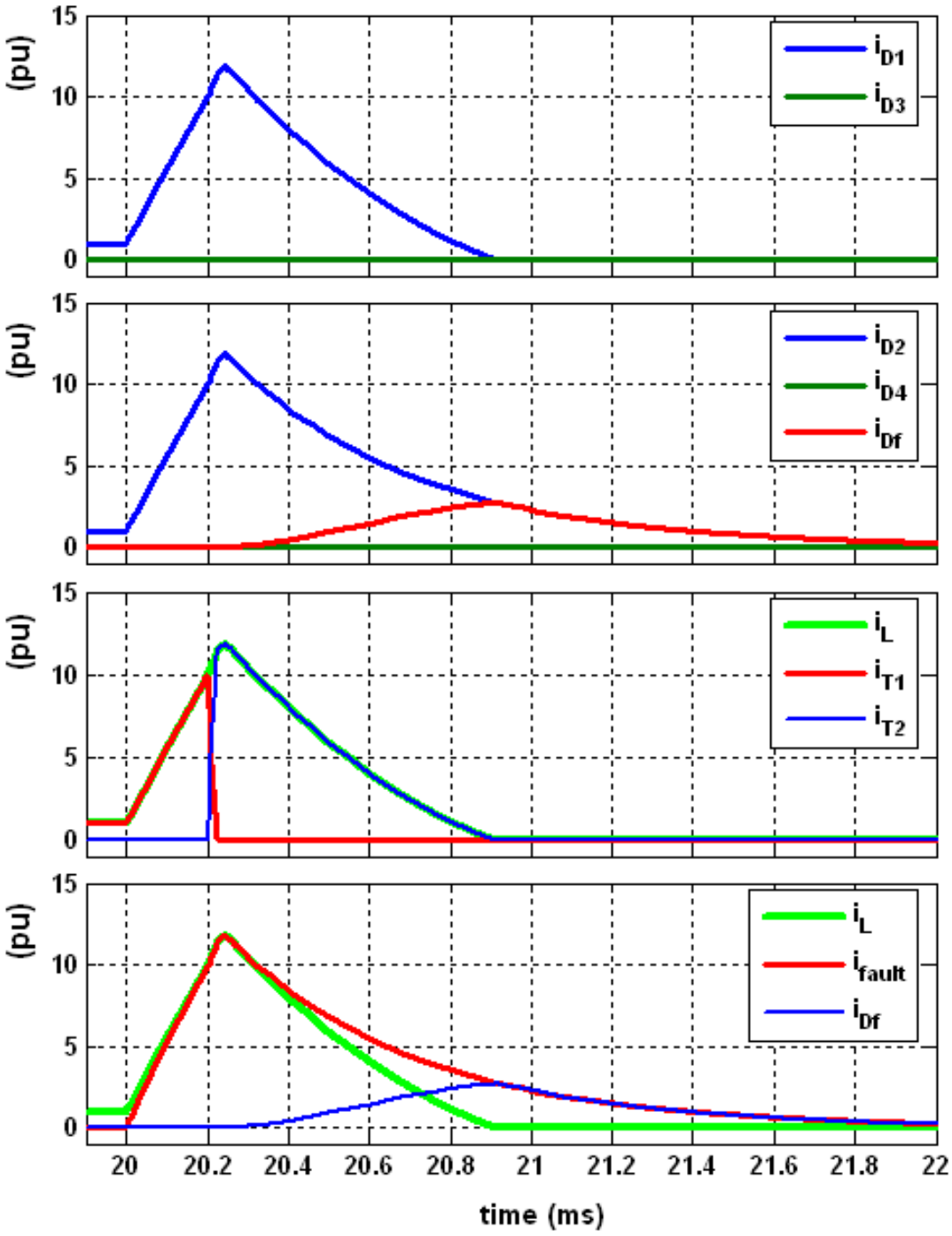

Figure 6-23: Waveforms for a DC fault at the Y side of the DCCB

6.4.2.3 Case 3: DC power reversal

In order to perform a simulation for power reversal, I implemented in Simulink® the circuit shown in Figure 6-24 where two DC-controlled sources were used. The simulation starts with controlled source #1 having a higher value than that of controlled source #2. The difference of voltage was calculated to provide a line current of +1.0 pu flowing from point X to point Y. At 20 ms, I increased the voltage of source #2 and decreased that of source #1 to get a line current of -1.0 pu flowing from point Y to point X.

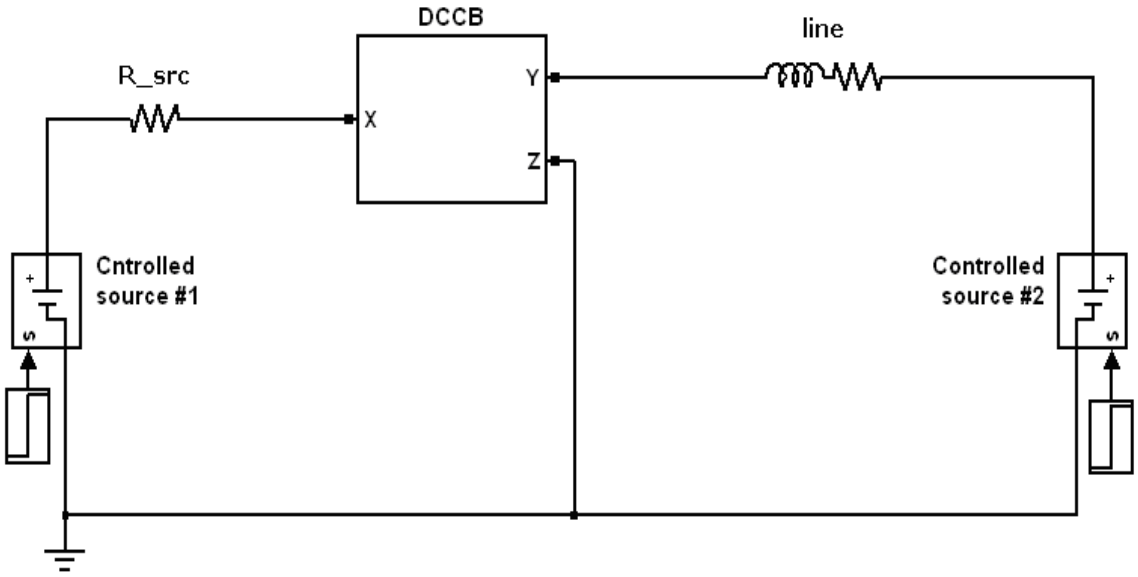

Figure 6-24: Setup for simulating a DC power reversal

The results of the simulation are reported in the four graphs of Figure 6-25. The first graph shows the current i_L flowing through the inductance L of the DCCB. This value of this current is reduced during the transition but the current does not change direction during power reversal because it is provided with an alternate path within the Graetz Bridge. The reversal of the line current i_{line} is clearly seen in the second graph where it is displayed using the blue color. The current i_{line} goes from +1.0 pu at 20 ms to -1.0 pu at 22.5 ms. This transition which is made with a time constant that is function of line inductance is made possible because diodes D_3 and D_4 took over the current from diodes D_1 and D_2. As the current i_{line} changes sign it passes through zero while the current i_L in the inductor of the DCCB is only reduced by 20%. This is due to the ability of the current i_L to circulates in the closed loop formed by inductor L, thyristor T_1, diode D_1, and diode D_4. If the situation were reversed and the line current goes from -1.0 pu to +1.0 pu than the loop for i_L will be formed by inductor L, thyristor T_1, diode D_2, and diode D_3. The fact that I could inverse line current direction without major opposition from the inductance of the DCCB is extremely important because I can choose bigger values for this inductance and obtain better fault current limiting capabilities. With lower fault current levels the

drop in DC voltage becomes negligible which opens the door for applications with common DC bus including the DC ring proposed for solving mega city problems.

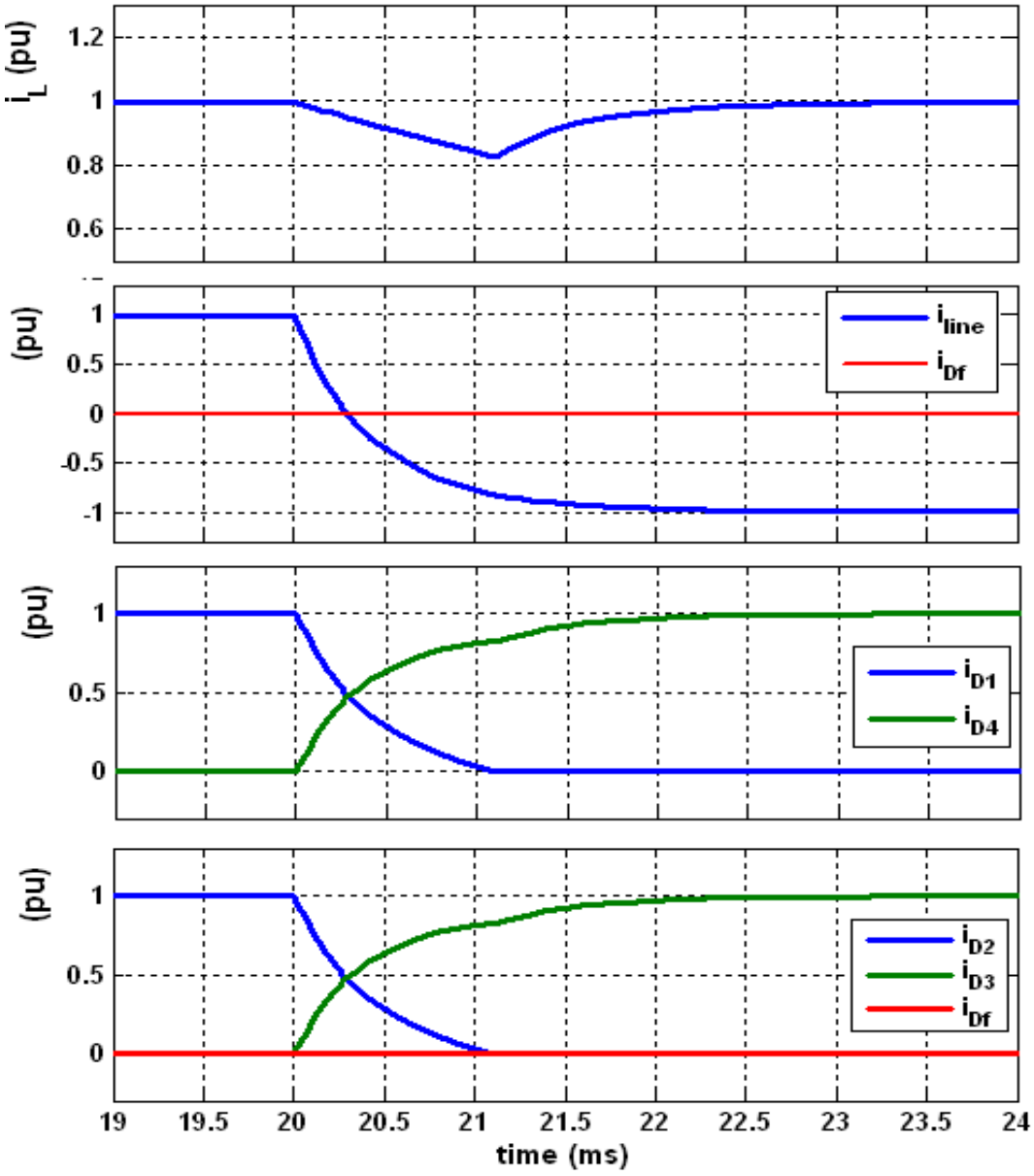

Figure 6-25: DC power reversal

6.5 Practical considerations and datasheets

In This section I calculate the rating of the power electronic devices such as diodes and thyristors used in the model of the DCCB. I also calculate the parameters of the snubber circuit for each of these devices and use them in the simulation. I also provide some practical advices and recommendations with respect to the gate drive and triggering mechanisms for potential implementation of the DCCB.

6.5.1 Rating of the power electronic devices

The rating of power electronic switches takes into account voltage and current transients that impose a safety margin during the design. Ford a DCCB, the DC voltage is controlled which means that voltage safety margins can be reduced. But the presence of a continuous DC voltage across the thyristor leads to a higher probability of cosmic ray failure or of thermal runaway, thus making the DC working voltage the determinant rating factor.

In a DCCB, there is only one voltage rating which have to be considered: the DC voltage that determines the cosmic radiation failure rate and long-term leakage current stability. This voltage is given by:

$$V_{DR} = V_{DC} \times \left(1 + \frac{y}{100} \right) \qquad (6\text{-}5)$$

where y is a safety factor that has to be selected based on switching conditions and stray inductances. For the calculation of the required voltage rating, a safety margin of about 50% is used for low stray inductances and for medium stray inductances, a safety margin of about 60% is used. As the DCCB operates only during faults and it switches only at zero current, the safety margin can be reduced to 30%. The preferred device rating is then normally selected as the next highest standard device voltage rating. Using equation (6-5) I can calculate the voltage V_{DR} for all thyristors and diodes of the DCCB as follows:

$$V_{DR} = 320\,\text{kV} \times \left(1 + \frac{25}{100}\right) = 400\,\text{kV} \qquad (6\text{-}6)$$

In appendix C.1 I provide the datasheet of diode 5SDF10H6004 that has a DC voltage rating of 3800 V and the following current characteristics:

V_{RRM}	=	6000 V
$I_{F(AV)M}$	=	1100 A
I_{FSM}	=	18×10^3 A
$V_{(T0)}$	=	1.5 V
r_T	=	0.6 mΩ
$V_{DC\text{-}link}$	=	3800 V

Diode

5SDF 10H6004

The I_{FSM} of 18 kA is the current the diode can handle for 10 ms at a junction temperature of 125^0C. From the datasheet provided in appendix C.1, the I_{FSM} for 1

ms is 44 kA. The simulation results that I performed showed that the fault current is limited to 36 kA. Hence the diode current is also limited at 36 kA for less than 100 μs and decreases exponentially afterwards. Since the $V_{DC\text{-}link}$ voltage of the diode is limited to 3800 V, I need 106 of these diodes connected in series to obtain the desired DC voltage rating of $106 \times 3800 = 402800\,\mathrm{V} > 400\,\mathrm{kV}$.

In appendix C.2, I provide a datasheet of thyristor 5STP42U6500 that has a working voltage of 3300 V and the following characteristics:

V_{DRM}	=	6500 V
$I_{T(AV)M}$	=	3460 A
$I_{T(RMS)}$	=	5440 A
I_{TSM}	=	71.4×10^3 A
V_{T0}	=	1.24 V
r_T	=	0.162 mΩ

Thyristor

5STP 42U6500

The selected thyristor can withstand a current of 71.4 kA for 10 ms at a junction temperature of 110^0C which is adequate for the DCCB. I need, however 122 thyristors connected in series to get $122 \times 3300 = 402600\,\mathrm{V} > 400\,\mathrm{kV}$.

6.5.2 Designing the snubber circuits

The snubber circuits have two functions in series-connected thyristors. The first function is to ensure even voltage distribution among the connected thyristors so no one single device is subjected to a voltage higher than its rating. The second function is to protect the device against over-voltage during turnoff process. For a valve composed of series-connected thyristors, each single thyristor should have its own snubber as shown in Figure 6-26. In the figure, L represents the contacts and line inductance and its value is of the order of 1000 μH. The calculation of the RC circuit is explained hereafter.

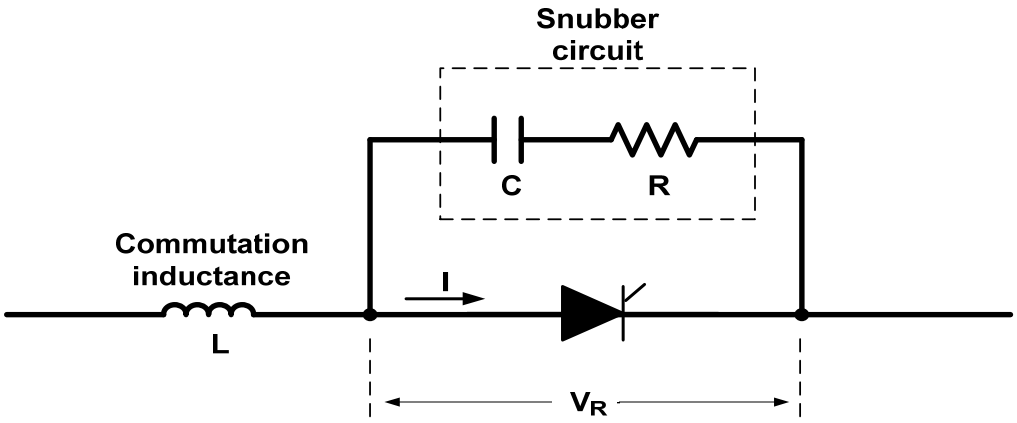

Figure 6-26: Thyristor with an RC snubber circuit

The typical voltage and current profiles that occur across the thyristor during turnoff process are displayed in Figure 6-27. In the figure V_0 corresponds to the normal

operating voltage and V_{RM} the maximum allowable voltage across the thyristor. A proper design of the RC snubber would keep the ration V_{RM}/V_0 at a low level.

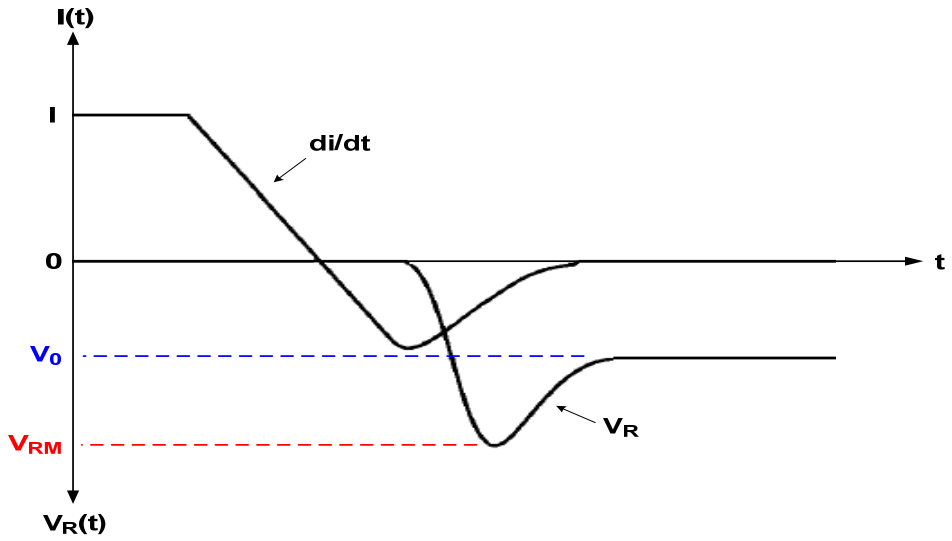

Figure 6-27: Voltage and current profiles during the turnoff process

Given an operating voltage V_0 and assuming a known value for the commutation inductance L, I can calculate the current fall rate di/dt from the ratio V_0/L. Using the calculated di/dt value I obtain a value for Q from the thyristor datasheet. By fixing a desired ratio V_{RM}/V_0, I can find the value of the capacitor C by reading $Q/(C \cdot V_0)$ at the maximum of the curve shown in Figure 6-28. Now that C and L are known, I can read the value R^2C/L on the horizontal axis of the curve and obtain a value for R.

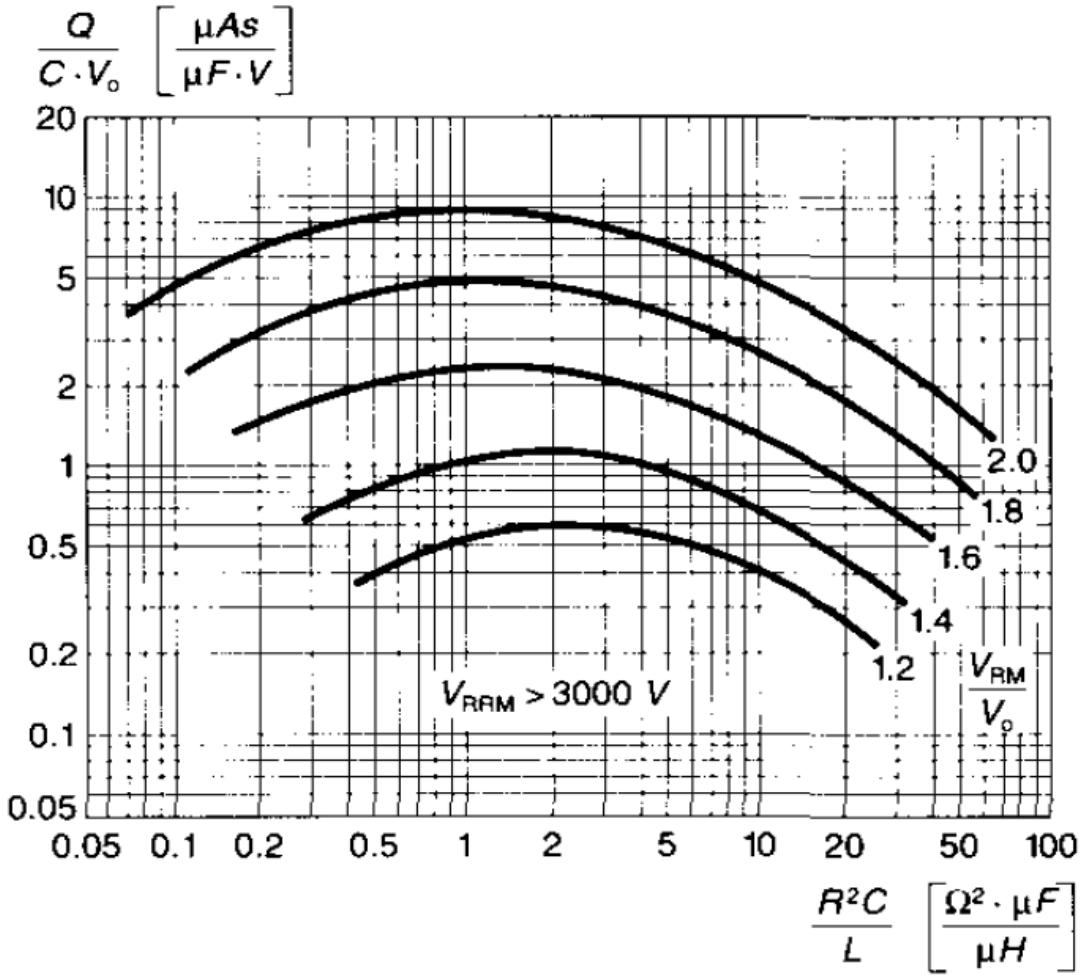

Figure 6-28: Curves for determining optimal RC snubber values [22]

From the datasheet provided in appendix C.2, I can read that the thyristor 5STP42U6500 has a working voltage V_0 of 3300 V. The selection of the voltage V_{RM} is based on the same factor of 1.25 used in equation (6-6) to calculate V_{DR}. Therefore, the maximum voltage overshoot will be set to only 25% yielding a voltage

V_{RM} of 3300 * 1.25 = 4125 V. In Figure 6-28 there is no curve corresponding to a ratio of 1.25. Therefore, I interpolate a curve and I estimate its maximum to be $Q/(C \cdot V_0)$ = 0.7 μAs/μF·V. Assuming that the value of the commutation inductance is set to 1000 μF, I calculate di/dt = 4125 V/1000 μF = 4.125 A/μs. From fig. 10 of the thyristor datasheet I obtain Q = 10000 μAs at $110^0 C$. Then, I calculate the capacitor C as follows:

$$C = \frac{10000\,\mu\text{As}}{3300\,\text{V}\,\frac{0.7\,\mu\text{As}}{\mu\text{F}\times\text{V}}} = 4.329\,\mu\text{F} \qquad (6\text{-}7)$$

The value obtained for C corresponds to the minimum value required to ensure desired performance. Since a higher value is permitted I chose a standard capacitor value of 4.7 μF.

From the horizontal axis of Figure 6-28 and using C = 4.7 μF, I calculate the resistor R as follows:

$$\frac{R^2 C}{L} = \frac{2.2\Omega^2\,\mu\text{F}}{\mu\text{H}} \Rightarrow R = \sqrt{\frac{2.2\Omega^2\,\mu\text{F}}{\mu\text{H}} \times \frac{L}{C}} = \sqrt{\frac{2.2\Omega^2\,\mu\text{F}}{\mu\text{H}} \times \frac{1000\,\mu\text{H}}{4.7\,\mu\text{F}}} = 21.6\Omega \qquad (6\text{-}8)$$

Again, I chose the nearest standard value of 22 Ω to be used for the snubber circuit.

The values of R and C calculated correspond to one single thyristor. For the simulation, I calculate aggregated values of R and C representing 122 series connected thyristors as follows:

$$C_{total} = \frac{4.7\mu F}{122} = 0.0385\mu F \text{ and } R_{total} = 22 \times 122 = 2684\Omega \qquad (6\text{-}9)$$

The values of C and R are calculated using the thyristor datasheet but are also suitable for the diode because the characteristics of the selected diode are similar to that of the thyristor. The values of C_{total} and R_{total} were used to model the snubbers for both the thyristors and diodes during the simulation presented in the previous sections of this chapter.

6.5.3 Triggering considerations for series-connected thyristors

When a valve is assembled of series-connected thyristors, one needs to make sure that all individual devices switch in the same time otherwise the slower device will be subjected to a voltage level that exceeds its blocking capability and destroy it. Besides the importance of providing simultaneous trigger-signals for all thyristors, the differences in delay times that these signals incur should be minimized. This can be achieved by the application of a strong gate pulse with a high di/dt.

Another consideration for the series-connected thyristors is the voltage imbalances at turn-ON. These imbalances in voltage are caused by differences in internal device parameters and junction temperatures. One way of addressing this issue is to add an RC snubber across each thyristor. In most switching applications, an RC snubber circuit is needed to limit voltage overshoot during reverse recovery. In the DCCB

proposed designs, the need for RC circuits is only for voltage balancing during turn-ON.

6.5.4 Spurious triggering due to electro-magnetic interference

In most applications, the valves are placed in environments that are rich with electro-magnetic interferences which might cause spurious triggering of the switches. To reduce the noise sensitivity, the inductance of the gate lead should be minimized. This can be achieved by mounting the gate driver as close as possible to the thyristor and by twisting the gate leads or by using shielded coaxial cables. These gate leads or coaxial cable should be placed away from high voltage or high current parts to avoid electromagnetic interferences or voltage flashover.

6.5.5 Signal transmission and power supply for the gate-drive unit

The thyristor that is placed at a high voltage potential receives its control signals from a control system that is at ground potential. Therefore, a galvanic separation of these two systems operating at two voltage potentials is absolutely necessary. Depending on the voltage level of the power system, one can choose from different approaches to achieve this goal.

For low voltage systems, a pulse transformer is an adequate solution to transfer a pulse current to the thyristor gate while providing required isolation. However, this solution is not practical for medium and higher voltage systems where the gate pulse

is generated by a local circuit located at high voltage levels. The common design practice is to send the gate control signals from the control unit to the gate driver using optical fibers. The gate driver is normally powered from a separate power supply or directly from the anode voltage.

The preferred design for the DCCB is to use a current closed loop that is inductively coupled to the gate driver of each thyristor. This approach has two advantages; 1) the gate driver is only powered when the current pulse is applied which eliminates any spurious triggering caused by electro-magnetic interference, and 2) all thyristor devices receive synchronized pulses because their gate drivers are inductively coupled to the same current flowing through the closed loop.

6.5.6 Gate current, gate drive, and load line recommendations

In practice, a gate pulse pattern as shown in Figure 6-29 is used to trigger thyristor valves. This pattern is found in the ABB thyristor datasheet provided in APPENDIX C and embodies important characteristics that guarantee proper triggering of the device. Even though a current I_{GT} is specified for thyristor triggering, practical experience showed that a current with much bigger amplitude is required to accomplish proper triggering of the thyristor. Because the gate current should not exceed the maximum allowed I_{FGM} rating of 10 amperes indicated in the data sheet, faster current rise is selected to achieve the required dynamic performance as

depicted in Figure 6-29. The parameters of the pulse that affect thyristor turn-ON delay time, fall time of the anode voltage, and switching energy losses are I_{GM}, di_G/dt, and $t_p(I_{GM})$. A high I_{GM} and di_G/dt are very important since they enhance all thyristor characteristics.

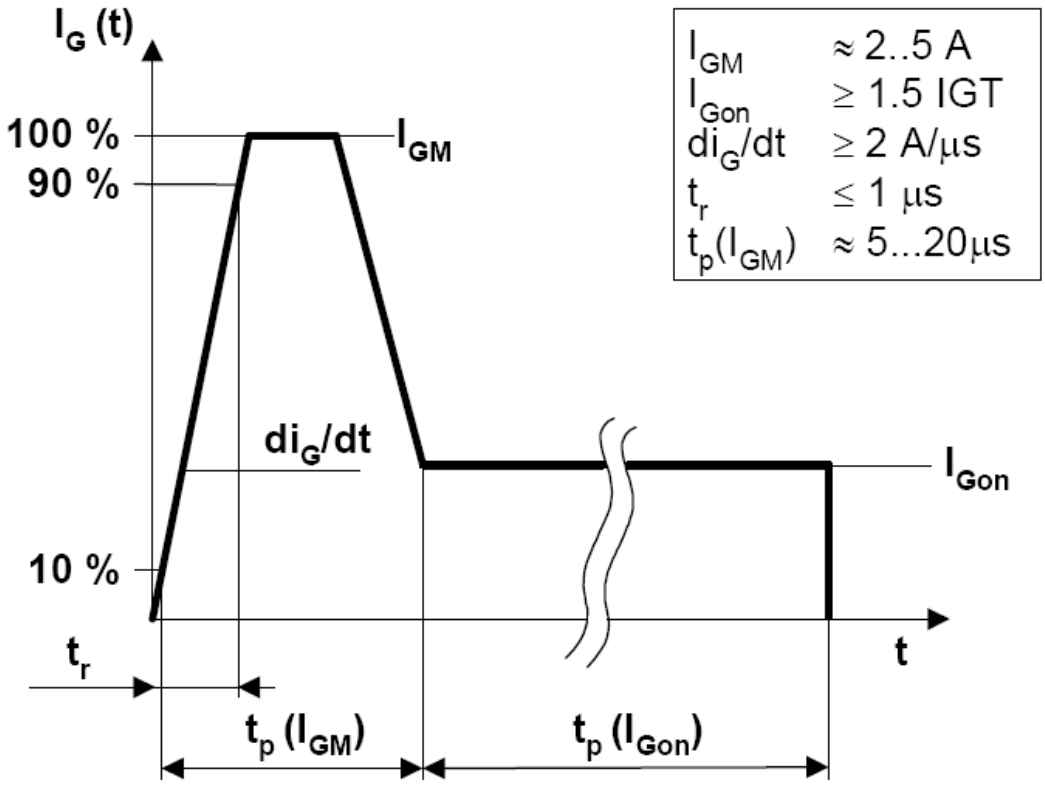

Figure 6-29: Recommended gate-pulse for thyristors

The datasheet of any thyristor would indicate a maximum value for I_{GM}, but does not specify any limit for di_G/dt. Therefore, di_G/dt is only limited by the gate driver design.

There is, however, some relationships between the value of di_G/dt and the duration $t_p(I_{GM})$ of the pulse overshoot that need to be observed for achieving proper triggering of thyristors.

For $di_G/dt \geq 20$ A/μs a duration $t_p(I_{GM})$ of 5 μs is sufficient to ensure proper triggering of the thyristor. However, durations longer than 20 μs are required for $di_G/dt \leq 5$ A/μs. The requirement of pulse duration during overshoot is critical to ovoid turning OFF of the thyristor when its gate current drops too quickly.

The value of the gate current during overshoot should be calculated using appropriate load lines as shown in Figure 6-30. This approach of designing the gate driver to exhibit a given di_G/dt and I_{FG} avoids the risk of distorting the gate current and ensures optimal triggering of the thyristor.

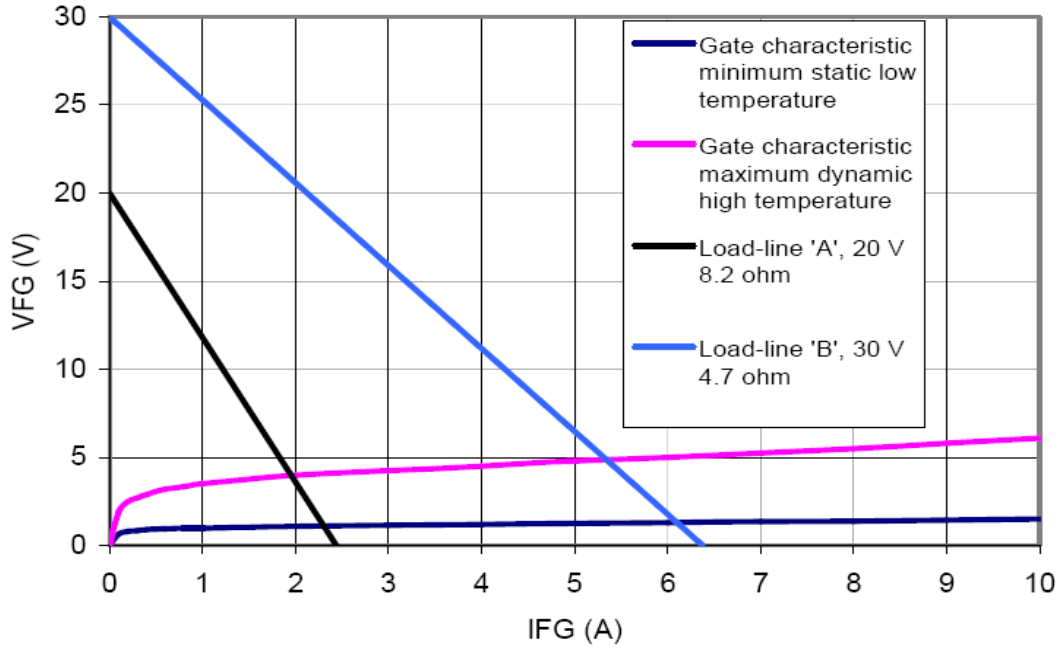

Figure 6-30: Example of gate driver load-lines

For example, load-line B in Figure 6-30 is characterized by a voltage V_{FG} of 20 V and an impedance of 8.2 Ω suggests a gate current of 1.8 A for maximum dynamic high temperature operations and 2.3 A for minimum static low temperature performances. An average value of 2.0 A can be chosen for normal applications. Whereas load-line B corresponds to a voltage V_{FG} of 30 V and an impedance of 4.7 Ω results in a gate current of 5.5 A. This load-line is recommended for applications with series and / or parallel-connected thyristors.

6.6 Conclusion

In this chapter, I proposed two novel designs for a DCCB to be used in applications with common DC buses such as wind farms, multiterminal city in-feed, and the novel DC ring topology proposed for solving mega city problems. The first design dealt with a unidirectional DCCB where the current is permitted to flow in one direction only. The design used an inductor, a capacitor, three thyristors, and one diode. I derived formulas to calculate optimal parameters of the model that limit the fault current and reduce the DC voltage drop during faults. I analyzed the circuit and simulated its behavior under fault conditions to obtain extremely good transient performances. Simulation results showed that the DCCB is able to quickly isolate DC faults and limit DC voltage drops to less than 11.0%.

The second design addressed a bidirectional DCCB that is of critical importance to DC applications using multiple converter stations. The proposed design solves the problem of DC fault clearing without causing voltage sparks, current oscillations, or shutting down of any converter stations connected to the DC bus. The DC voltage drop can be as low as 5.0% with proper selection of the DCCB parameters. The current through the breaker can change direction instantly without causing any transients to the DC system. A feature that is critical to DC systems with voltage source converters that can change power direction very quickly. Also, the fact that this DCCB limits the fault current and reduces the drop in DC voltage to negligible

values opens the door for applications with common DC bus including the DC ring proposed for solving mega cities problems.

6.7 References

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CHAPTER 7 NOVEL DCCB DEPLOYMENT IN A DC RING AND PROTECTION TECHNIQUES

In this chapter, I present a DC ring topology with properly placed DC circuit breakers and a detailed fault protection scheme for applications in a multiterminal system using HVDC-Light®. The proposed protection scheme uses local measurements and special coordination techniques for clearing low impedance faults and uses

differential measurements to identify and isolate high impedance faults. Digital simulation confirmed, under different DC fault types, the performance of the protection scheme in locating the fault and clearing it without interrupting power supply to sensitive loads.

7.1 Introduction

VSC technology has enabled development of HVDC-Light® systems with converter stations that require smaller filters and no local generation or synchronous condensers, and with control properties far superior to those of classic HVDC using thyristor switches.

Through a number of HVDC-Light® installations, the advantages, reliability and flexibility of the technology had been verified [01], [02]. Encouraging experience includes superior control properties and very high availability.

An important characteristic of HVDC-Light® technology is that the DC voltage in a two-terminal DC transmission system is constant in all modes of operation. Therefore, there is no DC voltage reversal connected with power reversal as required with classic HVDC. Because the DC system can be viewed as a bus and any terminal connected to the bus can feed power into the bus or extract power from

it without affecting stations not involved in the changed power flow direction, it is easy from a control point of view to make multiterminal HVDC links.

The challenge for a successful multiterminal application is three fold; first is the choice of a topology to easily connect many HVDC-Light® stations so power supply to sensitive loads remains available during faults, second is the protection coordination to be applied in order to properly locate and isolate DC faults, and third is the global control of the multiterminal system currents and voltages to optimize active power flows, regulate bus voltages and enhance overall system dynamics.

Some papers had already discussed multiterminal applications using HVDC-Light® [03], [04], [05] and focused in different aspects of the system. In [04], the authors had proposed a protection strategy against DC faults with, however, a major drawback: the entire HVDC network is required to be de-energized in order to isolate the fault.

In this chapter, I propose a configuration topology to connect multiple HVDC-Light® stations as well as a protection strategy to properly clear DC faults without shutting off healthy portions of the DC network. The control aspect of the multiterminal system is not the scope of this work and will not be addressed here.

7.2 Structure of this chapter

This chapter comprises eight major sections covering the deployment of DCCBs in a DC ring topology and the protection techniques to be applied so a DC fault is quickly detected and isolated without blocking any converter station or isolating healthy segments from the grid. The content of these sections is given bellow:

1. Section 7.1 provides a description of the motivation for developing a protection scheme for DC systems that is different from conventional ones used to protect AC systems.
2. Section 7.2 outlines the structure of this chapter.
3. Section 7.3 provides a detailed description of the DC ring configuration and the placement techniques of DCCBs.
4. Section 7.4 describes the different types of faults that can occur on the DC ring and outlines the protection techniques to be implemented.
5. Section 7.5 describes the protection algorithm that comprises a detection module reported in 7.5.1, a coordination module in 7.5.2, and a recloser module in 7.5.3.
6. Section 7.6 reports simulation results that validate the performance of the DCCB and the protection algorithm in detecting and isolating DC faults. Two

types of DC faults were considered; a solid fault reported in 7.6.1 and a high impedance fault reported in 7.6.2.

7. Section 7.7 concludes this chapter with a summary of the main important results and introduces the following chapter that presents recommendations for future work.

8. Section 7.8 lists some of the references that were consulted during this study.

7.3 DC network configuration

The proposed scheme, shown in Figure 7-1, consists of a number of HVDC-Light® stations attached to a DC ring via bidirectional DCCBs. Any of these stations can be connected to an active or passive network.

The DCCBs are placed on the line-ends such that a fault occurring on the DC ring, say at point A in Figure 7-1, can be isolated by opening the DCCBs of the faulty segment. For example, a fault on point A can be cleared by opening the DCCBs located on the right of HVDC-Light® #3 and on the left of HVDC-Light® #2. This action will isolate the faulted section from the rest of the DC ring without blocking any HVDC-Light® station. Therefore, power continues to be supplied to healthy sections of the DC network.

When the fault occurs at a terminal, say point B in Figure 7-1, it will be fed by DC currents flowing through the adjacent DCCBs as well as by AC currents through the converter station. Blocking of the DCCBs will isolate the fault from the DC side but will not disconnect it from the converter station. In such case, blocking the IGBT switches of the converter station, at point B, will not clear the fault since the diode bridge continues to feed the fault from the AC network. Therefore, this fault will be cleared by the AC breaker connecting the HVDC-Light® terminal to the AC network.

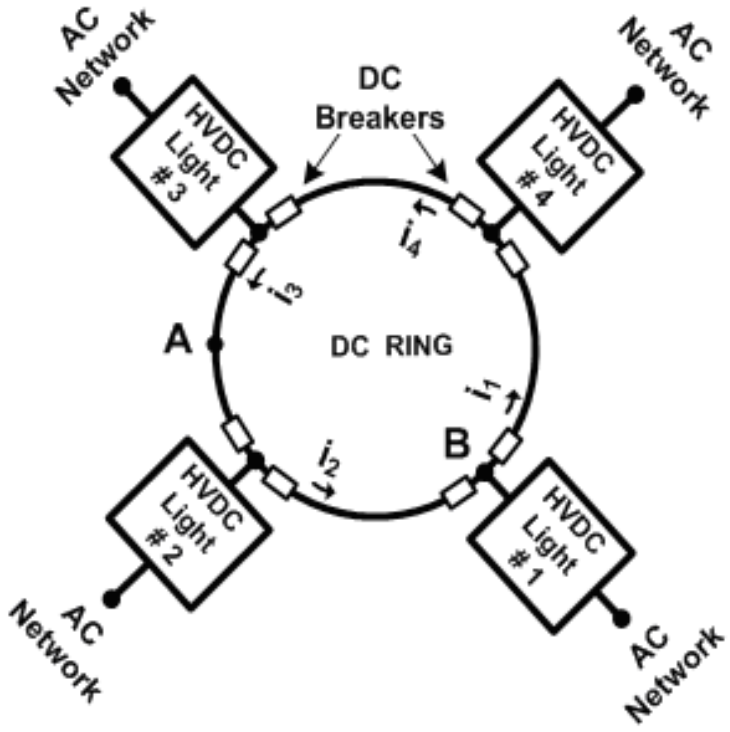

Figure 7-1: Multiterminal topology and DCCBs placement

In both cases mentioned above, only the faulty section of the DC network is isolated, thus maintaining a continuous supply of power to sensitive loads connected to the healthy parts of the DC ring.

7.4 Fault detection and protection coordination

There are mainly two types of faults that can occur on the DC ring: low impedance or high impedance faults. During low impedance faults the DC voltage collapses and all currents on the ring flow in the direction of the fault. The detection of this type of faults can be achieved using local measurements of DC voltage and currents. By monitoring the DC voltage, the change in DC currents amplitude and their direction reversal it is possible to detect and precisely locate faults on the DC ring. A comprehensive protection algorithm is developed and discussed in the following sections.

During high impedance faults, the change of voltage can be negligible and quickly corrected by the voltage regulators of the converter stations. The fault current amplitude is, in most cases, less than 10% of the load current and the protection algorithms can not differentiate this fault from a normal load increase especially when only local measurements are used. In order to detect high impedance faults on the DC ring a differential protection scheme should be implemented. A detailed

discussion of this scheme including communication techniques of measured quantities are presented in this chapter.

In a ring configuration, all the DCCBs will see a fault happening in point A or B and try to clear it. The proper sequence, however, is to have the closest breaker act to isolate the fault while the more distant ones remain closed to maintain power supply to healthy segments of the ring. As opposed to radial distribution feeder where upper-stream protection relays actions are delayed so protection devices near the fault can act first, in a ring configuration the concept of upstream or downstream coordination does not apply. Therefore, a novel method of protection coordination based on local measurements is developed. Details of this method are presented in the following sections.

7.5 Protection algorithm

The protection algorithm presented in Figure 7-2 comprises a fault detection module, a protection coordination module, and a recloser module. This algorithm can be implemented using fast controller or a flexible programmable gate array to achieve fast response time. The protection sequence is described in the following sections:

7.5.1 Fault detection module

The fault detection module has two components; one based on local voltage and current measurements outputs a fault signal F1 and the second based on local and remote current measurements outputs a fault signal F2. The fault signal F1 captures a condition where the local current (I_{DC}) or its rate of change rises above a maximum value (I_{max}) and the voltage (V_{DC}) drops bellow a minimum value (V_{min}). On the other hand, F2 rises when the difference in current at both ends of a line exceeds a threshold (I_{dif}). Either one of these two signals F1 and F2 will generate a DC_Fault signal that would run through an anti-bumping logic before getting into the protection coordination module.

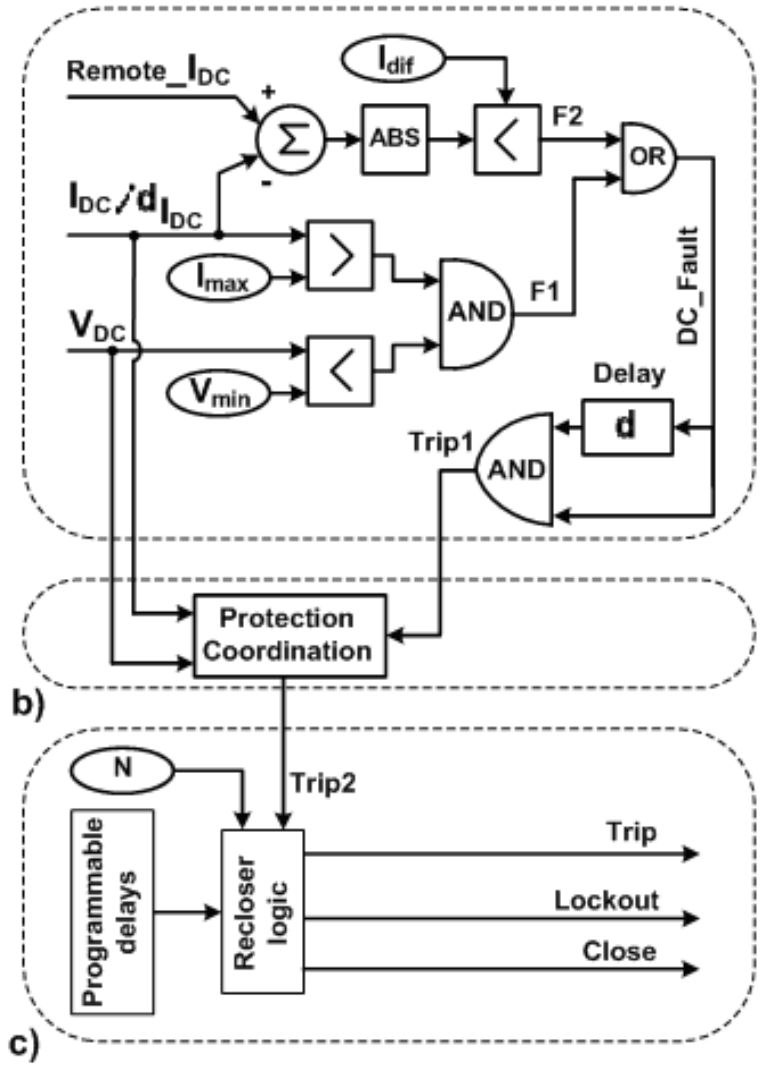

Figure 7-2: Protection algorithm; a) fault detection module, b) protection coordination module, and c) recloser module

The anti-bumping is achieved by passing the DC_Fault signal through an AND gate with its delayed image. The delay defines the minimum time required for the signal

to be maintained before it is considered valid. Figure 7-3 depicts two cases: one showing a short lived DC_Fault signal that does not trigger the trip signal Trip1 and another showing a DC_Fault signal that persists more than the required delay and triggers the trip signal. The Trip1 signal goes through the protection coordination module to be processed.

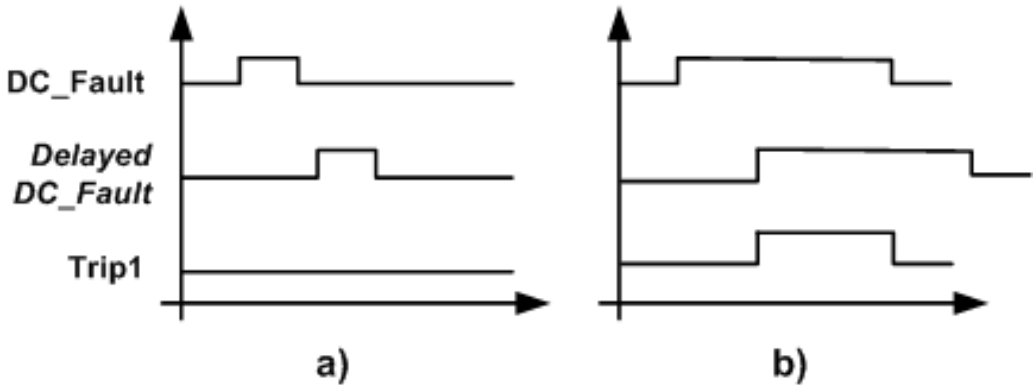

Figure 7-3: Anti-bumping logic: a) non valid fault signal, b) valid fault signal

7.5.2 Protection coordination module

The protection coordination module uses local measurements of currents and voltages to identify which breaker should clear the fault as shown by the functional diagram of Figure 7-4. In this figure, the DC voltage is first passed through a 50 ms averaging filter then held for 50 ms during normal operating conditions and 10 seconds during faults. The 10 second holding time is required to ensure the calculated DC voltage represents pre-fault value and is not corrupted by transients

due to faults. In this case I assume the fault is completely cleared within 10 seconds as it is usually the case. This time includes all possible reclosing actions to be performed.

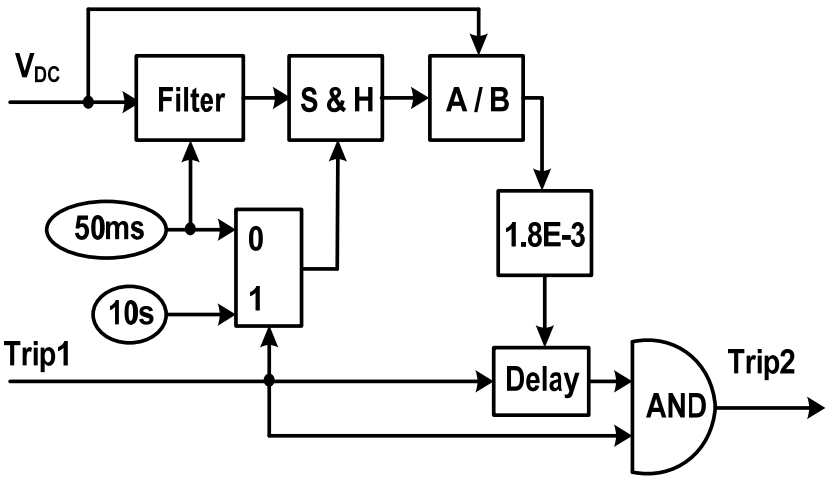

Figure 7-4: Protection coordination based on local measurements

The measured value of DC voltage is then used as a voltage base to evaluate the voltage drop during faults expressed in p.u. Then the voltage reading during faults is translated into delays that are imposed to the DCCBs. The shortest delay will be attributed to the steepest voltage drop reflecting a shorter electric distance to the fault. The goal is to attribute fast actions to the DCCB close to the fault and slower ones to the DCCBs located farther away from the fault. These delays are calculated by multiplying the DC voltage by a factor and applying it as input to the programmable delay block as shown in Figure 7-4. In the simulation, the factor gain

was set to 1.8E-3 so that a maximum of 1.8 ms delay is applied during normal operations.

7.5.3 Recloser module

The recloser module implements a simple logic similar to what is commonly used in feeder automation. Its function is to reclose the DCCB after a certain time delay of its previous trip in a hope that the fault was cleared. The recloser action can be repeated N times before a lockout (a permanent trip) of the breaker is initiated. Figure 7-5 shows the recloser functional diagram.

The signal Trip2 coming from the protection coordination is passed through a rising edge block to generate a pulse each time the signal makes a transition from 0 to 1 state. The generated pulse is used to perform the following actions:

- Trip the DC circuit breaker
- Increase the counter by one. The output of the counter is compared to the user defined maximum reclosing actions N for which a lockout will be initiated. The counter output is also used as an index for selecting a distinct time delay from a vector of values for each reclosing.
- Reset the timer. The timer is reset whenever a pulse is received. If no pulse were received for a time defined by Delay + 2s then the fault is considered

cleared and the counter is reset to zero. This resets the delay to a default D0 value.

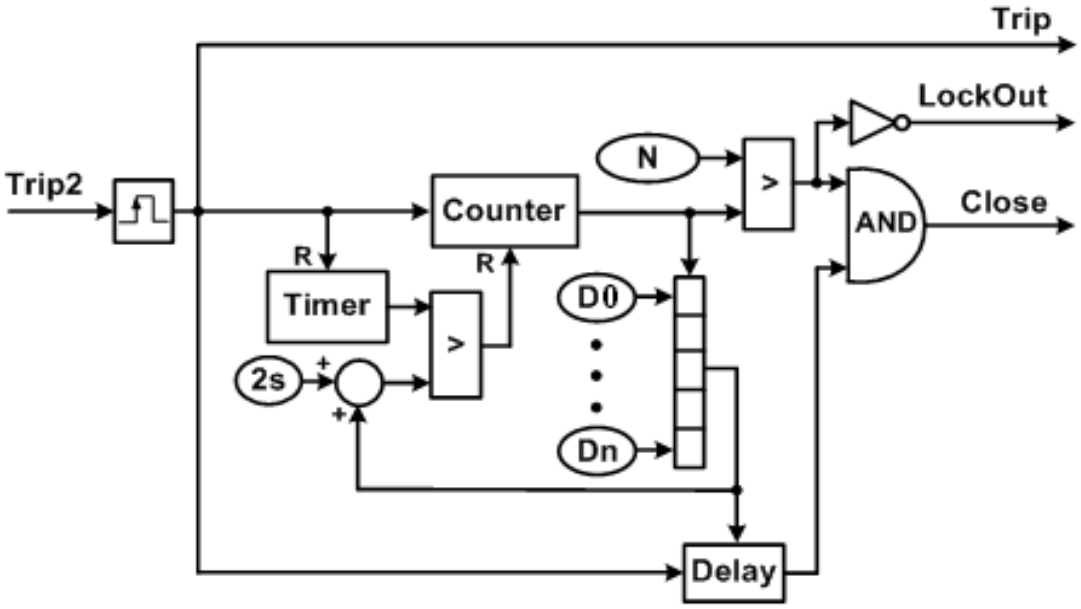

Figure 7-5: Recloser functional diagram

7.6 Simulation results

To verify the algorithm I used the setup shown in Figure 7-6 and the parameters provided in Table 7-1. In Figure 7-6, I connected four DCCBS in cascade to simulate a portion of the proposed DC ring topology. I represented three VSCs by equivalent RC circuits as shown in the orange boxes. Voltage source converters VSC1 and VSC2 represent HVDC-Light stations connecting passive networks to the DC ring while VSC3 represents a HVDC-Light station connecting a power source.

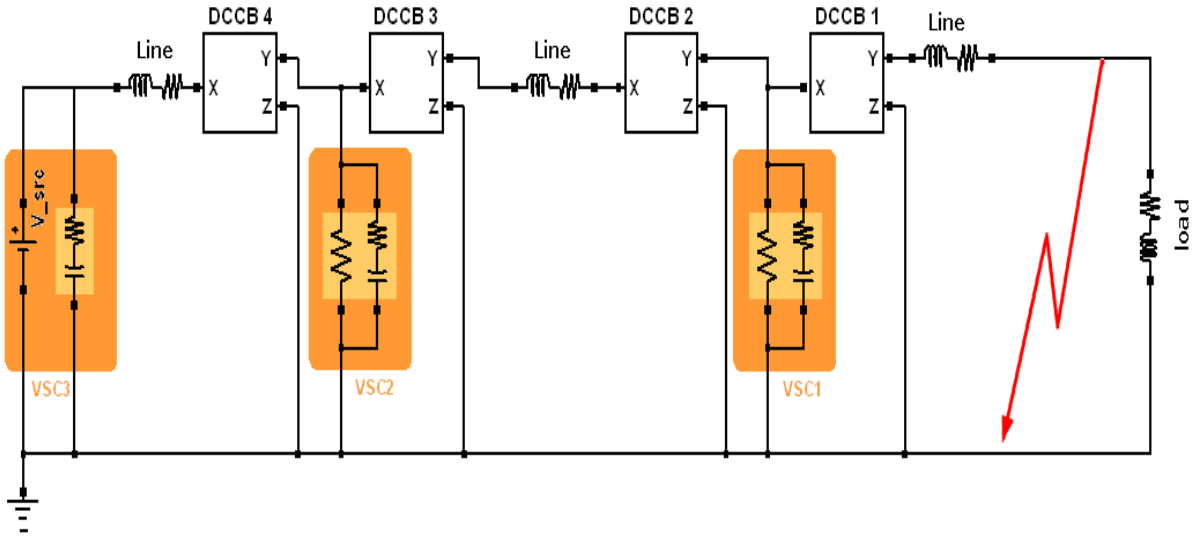

Figure 7-6: Test setup for a solid DC fault

In order to test the proposed protection algorithm and assess the performance of its modules I performed two simulation cases; a solid DC fault and a high impedance fault. The solid DC fault aims at verifying local algorithm performance in mitigating the fault while the high impedance tests the accuracy of the differential protection scheme.

Table 7-1: Parameters used for simulating a DC fault

Parameters		Value	Unit
VSC1			
	R shunt	250	Ω
	R series	0.05	Ω
	C	0.20	μF
VSC2			
	R shunt	350	Ω
	R series	0.05	Ω
	C	0.16	μF
VSC3			
	V_src	320	kV
	R	1.00	Ω
	C	0.32	μF
DCCB			
	L	3.20	mH
	C	2.01	μF
	Snubber Resistor	2684	Ω
	Snubber Capacitor	0.0385	μF
	Arrester protection voltage	400	kV
Line/Cable			
	L_line	0.30	mH
	R_line	0.50	Ω
Load			
	R_Load	190.00	Ω
	L_load	10.00	mH
Fault			
	Application time	20	ms
	detection time	300	μs

7.6.1 Solid DC fault

To perform this simulation case, I applied a fault near DCCB1 with the expectation that only this circuit breaker will trip and isolate the fault and I grouped the results under six graphs shown in Figure 7-7. In graph #1, the voltage at the output of DCCB1 goes to near zero due to its electrical proximity to the fault. However, the voltage at the output of DCCB2 is higher because of the voltage drop across the reactor inside DCCB1. Since each DCCB exhibits an internal voltage drop, a distinct difference between these voltages is obtained and will be exploited for protection coordination as I explain in the following paragraphs.

The graph #2 of Figure 7-7 shows the currents inside the DCCBs. The initial currents of the various DCCBs are function of the loads they are feeding. For this particular setup, DCCB1 curries the current of the end load only, DCCB2 carries the current of DCCB1 and that of VSC1, DCCB3 carries the current of DCCB2 and that of VSC2, and DCCB4 carries the current of DCCB3 and that of VSC3. As DCCB2 and DCCB3 are connected in series without any shunt load in between, their currents are identical and only that of DCCB3 can be seen in the graph. When the fault was initiated at 20 ms, I immediately witnessed a jump on the current values and a drop on the voltages of the circuit breakers. For this simulation, I fixed the detection threshold at 0.8 pu for the voltages and 3.0 pu for the currents. When these two conditions are met simultaneously, a Trip1 signal is initiated. These trip signals are

displayed in graph #3 of the figure. At the moment Trip1 signals are initiated, the voltage levels of the corresponding DCCBs are recorded and translated into time delays following the procedure explained in section 7.5.2.

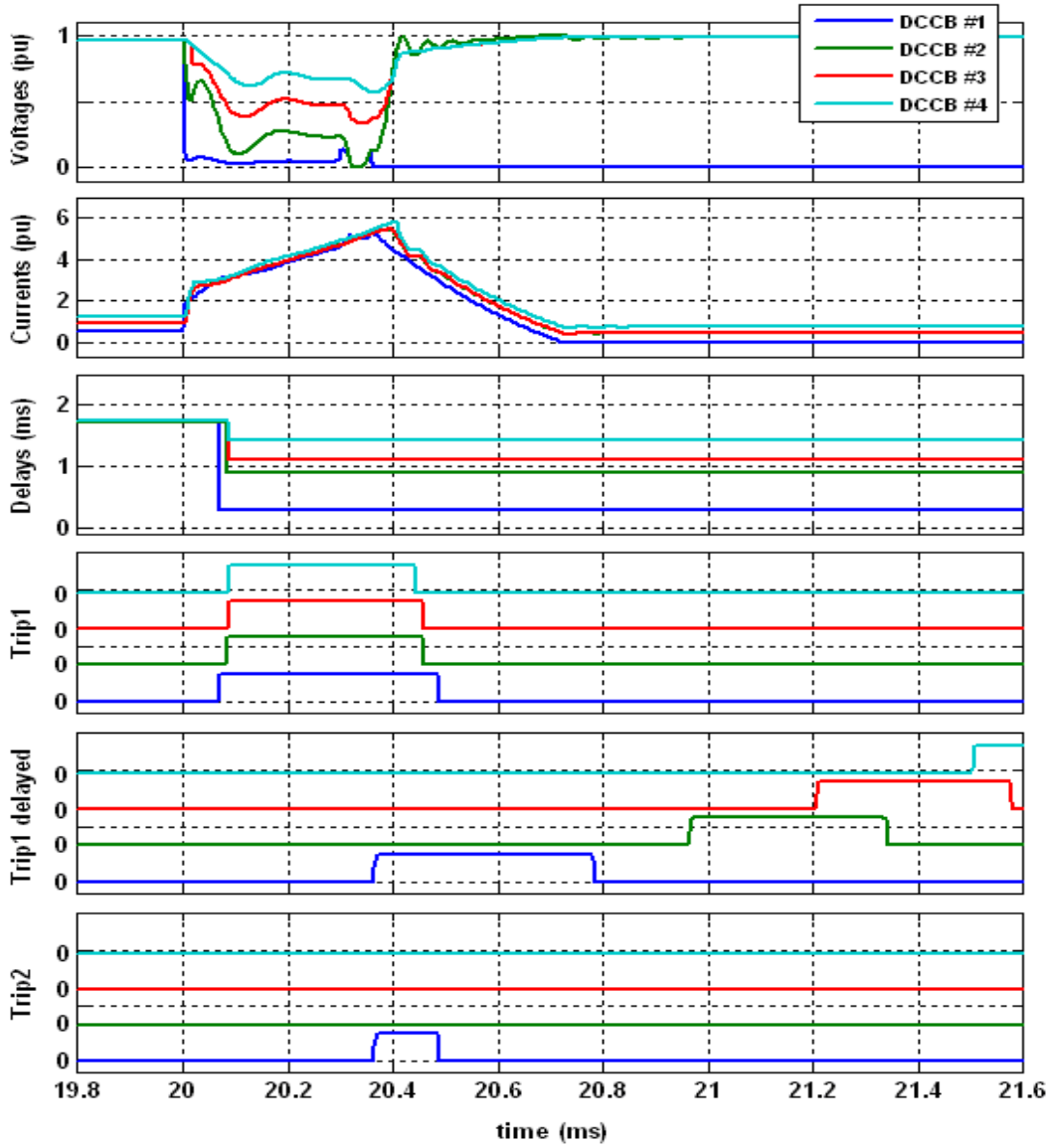

Figure 7-7: Protection algorithm verification with a solid DC fault

The time delays shown in graph #4 are applied to the signals Trip1 to implement protection coordination that reflects the electric distance between the DCCBs and the fault location. I clearly see that the farther a DCCB is from the fault the longer the delay its gets.

The delayed signals of graph #5 are then AND gated with the original Trip1 signals to produce the commands of the various DCCBs. All signals in graph #6 are null except of that of DCCB1. When DCCB1 is tripped, the voltages in graph #1 revert to their pre-fault values and eliminate the voltage condition for detecting a fault. Therefore, all signals in graph #3 become null.

The tripping of DCCB1 completes the loop of detecting, coordinating and isolating the DC fault from the source. In practice, a fault can be of fugitive nature caused by ionized air, trapped animal or for aerial lines a bird or a tree branch contact. In such case the tripping of the line removes the faults completely without any further personal involvement. Therefore, utilities use reclosing practices to clear this type of faults. In general, two or three tries are applied before declaring a fault to be permanent and locking out the breaker.

In the test I had performed, I set the number of recloser actions to 2. This means that the DCCB will trip a first time, reclose the line on the fault, trip a second time and lock out. The time between recloser actions is normally in the order of seconds. But in our case, I set the time to 39 ms to show the reader the actions of the recloser.

The time of 39 ms starts counting once the current in the DCCB is null. The results are reported in Figure 7-8 and grouped in 6 different graphs similar to the previous case. The first four graphs report the same information as in Figure 7-7. The main difference is reflected in the repetition of the fault that is caused by the recloser action. A close look at the DCCB1 current in graph #1 reveals that it has a non zero value before the first occurrence of the fault. After the fault is cleared by opening the line, this current became null and remained that way until the DCCB1 closed on the fault in an attempt to restore power. The closing action occurred at time t = 60 ms by supplying a short pulse to trigger the main thyristor of the DCCBs. This close signal is shown in graph #6. Closing the line on a fault has triggered the protection algorithm to execute again and clear the fault.

As the counter of the recloser increases whenever a trip (signal Trip2) is initiated, it reaches the preset number of 2 when the second fault clearing is performed. This concludes that the fault is a permanent one and a lockout signal is raised as shown in graph #6 of Figure 7-8.

The lockout signal is used to open the mechanical switch that is placed in series with the DCCB in order to provide visual indication that the line is not powered so service personnel can proceed with the needed repairs. At this point, the line can not be reenergized automatically by the recloser actions. A command should be send by an operator to close the line once the causes of the DC fault are removed.

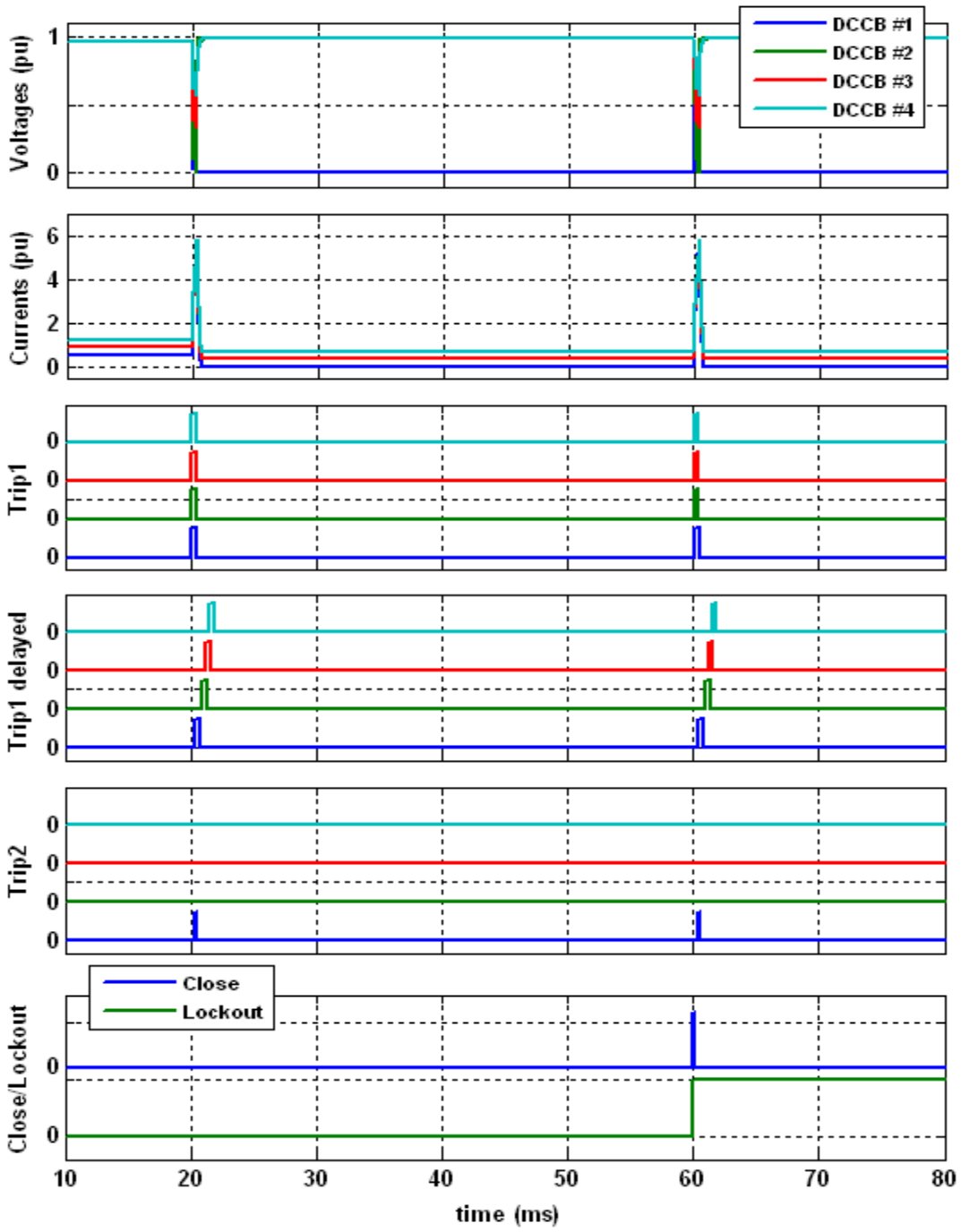

Figure 7-8: Simulation results with recloser actions

7.6.2 High impedance fault

High impedance faults simulate, for example, a contact of overhead lines with a tree or cable incipient faults for underground installations. The currents exhibited by high impedance faults are not large enough to be detected by conventional protection algorithms. Therefore, I implemented a differential protection scheme that requires knowledge of the current values in both ends of a line or a cable. Communication of remote quantities can be done using the power lines or an independent Ethernet infrastructure. I used the test circuit presented in Figure 7-9 to perform the high impedance fault test by initiating a fault between DCCB2 and DCCB3. The fault impedance is set to exhibit a fault current of 0.1 pu. All other parameters of the test circuit are provided in Table 7-1.

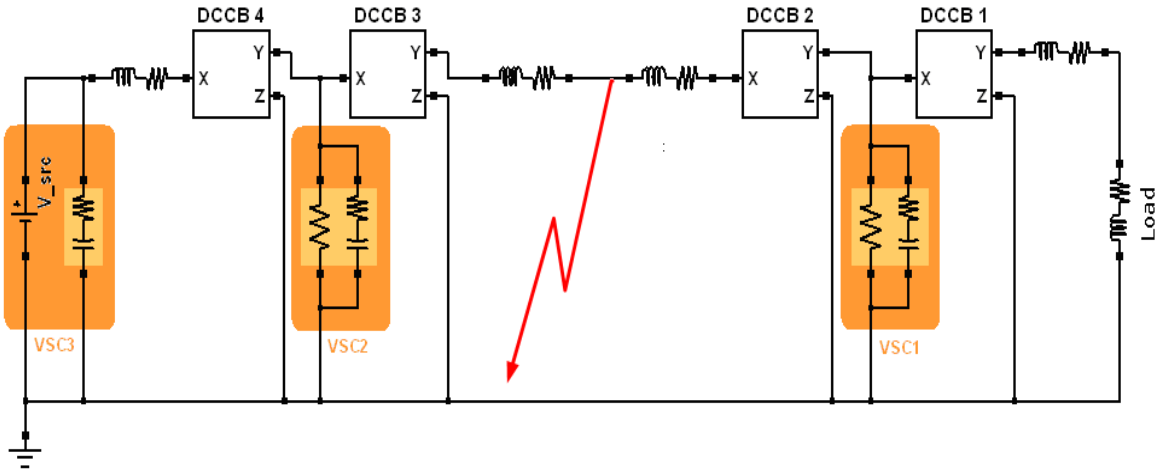

Figure 7-9: Test setup for a high impedance fault

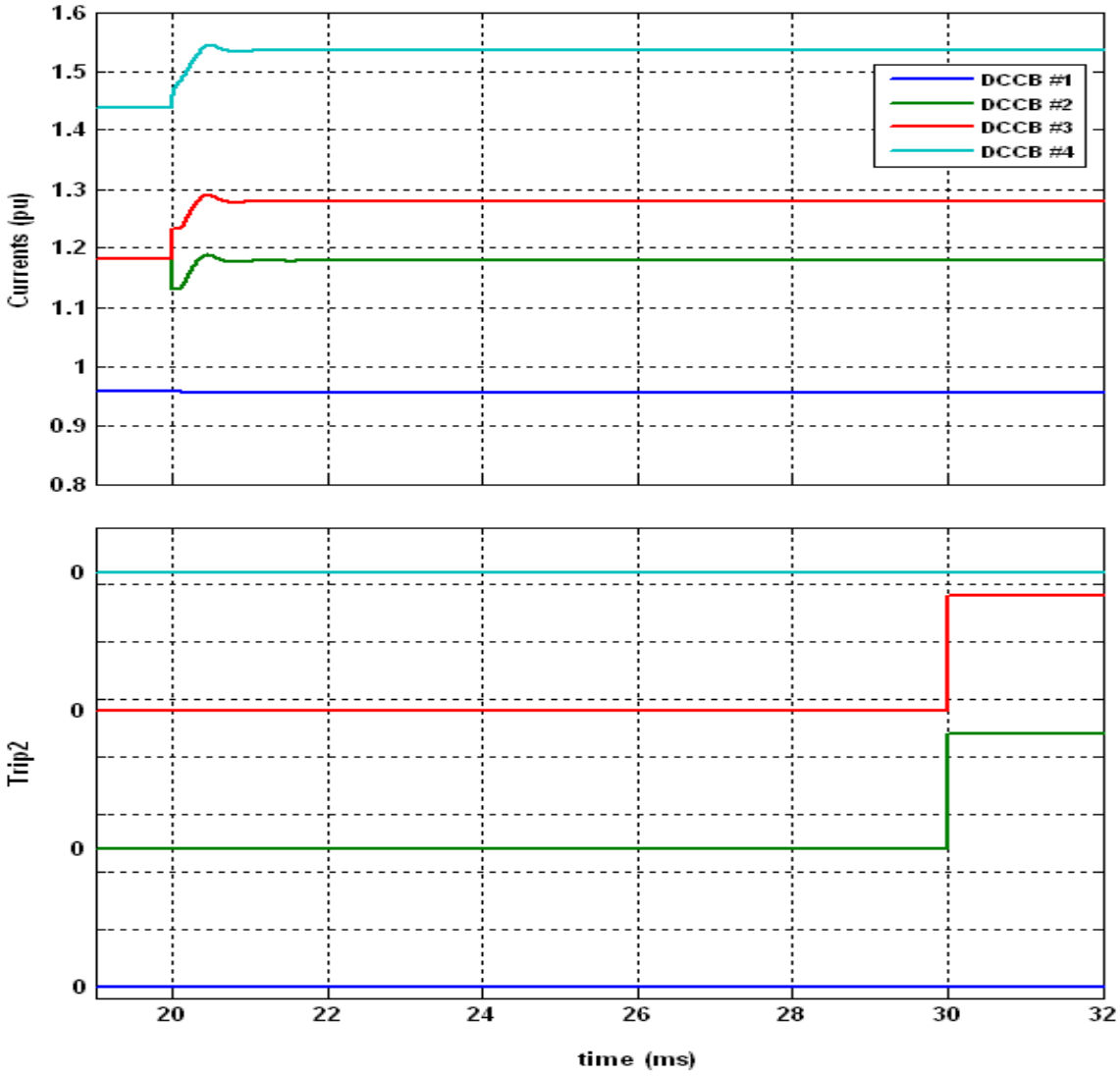

Figure 7-10: Simulation results for a high impedance fault

Before the fault is initiated, the currents in DCCB2 and DCCB3 are identical as shown in the first graph of Figure 7-10. After the fault is initiated, these two currents

cease to be equal and the difference is picked up by the protection algorithm. In practice, the difference in current values should persist for at least 10 seconds before raising a flag. The purpose of this delay is to weather any transient condition. For the case I simulated, the wait time is set at 10 ms. Therefore, the trip signals for DCCB2 and DCCB3 were initiated 10 ms after the fault is detected. Some utilities would prefer to trip the line and try to clear the fault and others use the trip signal as an indication and send service personnel for investigation. In this case, I did not initiate a trip to the circuit breakers to open the line.

7.7 Conclusion

A DC ring topology with properly placed DC circuit breakers and a detailed fault protection scheme are presented for application in a multiterminal system using HVDC-Light®. The proposed protection scheme uses local measurements and special coordination techniques for clearing low impedance faults and uses differential measurements to identify and isolate high impedance faults. The different protection modules consisting of fault detection, protection coordination and reclosing actions are discussed. The protection algorithm modules are designed for real-time applications and their code is optimized for implementation in the DC breaker electronic board using flexible programmable gate arrays.

Digital simulation of the proposed protection scheme is conducted for solid and high impedance DC fault types. The performance of the protection in detecting the fault and clearing it without interrupting power supply to healthy segments of the DC network was proven.

7.8 References

[01] U. Axelsson, A. Holm, C. Liljegren, M. Åberg, K. Eriksson, O. Tollerz," The Gotland HVDC-Light® project – experiences from trial and commercial operation," CIRED 2001, Amsterdam, Netherlands, June 2001.

[02] L. Ronström , B. D. Railing, J. J. Miller, P. Steckley, G. Moreau, P. Bard, J. Lindberg, "Cross Sound Cable Project Second Generation VSC Technology for HVDC," Cigré Session 2004, B4-102.

[03] W. Lu and B. Ooi, "Premium Quality Power Park Based on Multiterminal HVDC," IEEE Trans. Power Delivery. vol. 20, N. 2, April 2005.

[04] L. Tang, B. Ooi, "Protection of VSC-Multiterminal HVDC against DC Faults," 33rd IEEE Power Electronics Specialists Conference, Queensland, Australia, 2002.

[05] W. Lu and B.-T. Ooi, "DC overvoltage control during loss of converter in multiterminal voltage-source converter-based HVDC (M-VSC-HVDC)," IEEE Trans. On Power Delivery; vol. 18, pp. 915–920, July 2003.

CHAPTER 8 SUMMARY AND FUTURE WORK

In this chapter, I present the main findings of the work I performed for this dissertation. These findings include the characterization of mega city power grid problems and the various solutions that were applied to solve them including the novel and comprehensive approach put forward to solve the grid fault current excessive levels and voltage stability issues.

8.1 Summary

In this dissertation, I identified the problems that power grids are facing in terms of fault current levels and voltage instability using Shanghai power grid as a testbed. I discussed solutions using FACTS devices such as FCL, SVC-Light®, and HVDC-Light® that address individual issues of the Shanghai power grid and I concluded that these solutions should be combined and placed in many locations of the grid to attain acceptable performances. I also found that these solutions when added together would complicate control coordination and protection settings. Furthermore, any future load or supplied generation increase would require additional tuning or new installations of these device-based solutions. Then, I presented a novel solution based on a multiterminal use of HVDC-Light® stations sharing a common DC bus in a ring topology. This topology provides redundancy, better protection against faults, and does not increase short circuit levels. Adding loads or power sources does not impact system protection or performance. However, I also identified that a need for special protection against DC faults must be satisfied for the solution to be practical. Therefore, a new DC breaker design and a fast protection algorithm were developed and tested through simulation.

The design addresses a bidirectional DCCB that is of critical importance to DC applications using multiple converter stations. The proposed design solves the problem of DC fault clearing without causing excessive voltage drops, current

oscillations, or shutting down of any converter stations connected to the DC bus. The DC voltage drop can be as low as 5.0% with proper selection of the DCCB parameters. The current through the breaker can change direction instantly without causing any transients to the DC system. A feature that is critical to DC systems with VSCs that can change power direction very quickly. Also, the fact that this DCCB limits the fault current and reduces the drop in DC voltage to negligible values opens the door for applications with common DC bus including the DC ring proposed for solving mega city problems.

The DCCB was used in a novel DC ring topology with a new protection scheme that solves the problem of protection coordination in a loop system. Digital simulation of the proposed topology along with the proposed protection scheme is conducted for different DC fault types. The performance of the protection in locating the fault and clearing it without interrupting power supply to sensitive loads was proven.

8.2 Future work

When multiple VSC stations are connected to a common DC bus, the problem of control coordination between these stations becomes evident. Hunting problems between the different controllers should be addressed. Furthermore, when any given converter station changes power direction and goes from supplying to absorbing power, or vise-versa, a concerted action should be implemented to conserve DC

power flow balance. The decision between localized or distributed control intelligence to deal with this problem is not yet clear and it represents a challenging subject for investigation.

Appendices

APPENDIX A PUBLICATIONS

A.1 Papers in refereed conference proceedings

1. Mohamed Maharsi, Vaibhav D Donde, Alex Q. Huang; "Novel topology and protection strategy for a multiterminal HVDC-Light® system," Conference. IREP SYMPOSIUM 2007: Bulk Power System Dynamics and Control - VII, Charleston, South Carolina, USA, August 19-24, 2007.

2. Mohamed Yassine, Haj-Maharsi, Alex Q. Huang, “Investigating Subsynchronous Oscillations,” 3rd Annual SPEC Seminar, May 2007, Raleigh, North Carolina, USA.

3. Mohamed Maharsi, Vaibhav D Donde, Alex Q. Huang; “Protecting VSC in a loop System,” 3rd Annual SPEC Seminar, May 2007, Raleigh, North Carolina, USA.

A.2 Papers in ABB review journal

1. Mohamed Y. Haj-Maharsi, Deia Bayoumi, Thomas G. Sonsinski, Doug Voda, “Creating a control and protection relay for medium voltage distribution feeders,” ABB review, ISSN 1013-3135, Nº 3, 2007, pages. 39-41.

2. Ratan Das, Deia Bayoumi, Mohamed Y. Haj-Maharsi, “A vote of confidence for ABB’s high impedance fault detection system,” ABB review, ISSN 1013-3135, Nº 3, 2007, pags. 42-45.

APPENDIX B HVDC-LIGHT DATA ENTRY

```
System data as entered for SIMPOW simulation

!-----------------------------------------

!

! HVDC-Light System data

! ---------------------------------------------------------------------
```

```
SHUNT
! Shunt capacitors
      Light_R1  R=5000 C=60E-6
      Light_I1  R=5000 C=60E-6
      Light_DC1 R=2E6  C=7E-6
      Light_R2  R=5000 C=60E-6
      Light_I2  R=5000 C=60E-6
      Light_DC2 R=2E6  C=7E-6
END
!
PWM
 LIGHT_REC ACBUS1  Light_R1 DC1=Light_R2 TYPE=DSL/LIGHT_V1_OPTPOW/
           SN=400  UN=415   TAU=0.98
           Pctrl=1 UacCtrl=1  Pref =.9573  UacRef=1
!
 LIGHT_INV ACBUS2  Light_I1   DC1=Light_I2  TYPE=DSL/LIGHT_V1_OPTPOW/
           SN=700  UN=415   TAU=1.01
           Pctrl=0 UacCtrl=1  UacRef=1
END
```

```
NODES
! AC Connections
 ACBUS1 UB=195 TYPE=AC AREA=1 REGION=1
 ACBUS2 UB=195 TYPE=AC AREA=1 REGION=1
!
! DC Connections
 Light_R1  UB=320 TYPE=DC AREA=1       REGION=1
 Light_R2  UB=320 TYPE=DC AREA=1 UI=-1 REGION=1
 Light_DC1 UB=320 TYPE=DC AREA=1       REGION=1
 Light_DC2 UB=320 TYPE=DC AREA=1 UI=-1 REGION=1
 Light_I1  UB=320 TYPE=DC AREA=1       REGION=1
 Light_I2  UB=320 TYPE=DC AREA=1 UI=-1 REGION=1
! ------------------------------------------------------------------------
LINES
! Cable parameters
 Light_R1  Light_DC1 TYPE=6 R=0.27 LL=0
 Light_DC1 Light_I1  TYPE=6 R=0.27 LL=0
 Light_R2  Light_DC2 TYPE=6 R=0.27 LL=0
 Light_DC2 Light_I2  TYPE=6 R=0.27 LL=0
END
```

```
TRANSFORMERS
! Transformer parameters
 B019 ACBUS1 SN=525 UN1=533 UN2=415 EX12=0.0001 ER12=0.0
 B032 ACBUS2 SN=525 UN1=241 UN2=415 EX12=0.0001 ER12=0.0
END
!
SHUNT IMPEDANCES
! Q settings
 B019  Q= 325  UN=525
 B004  Q=-360  UN=525
!
! Invoking the HVDC-Light Model
DSL-TYPES
 LIGHT_V1_OPTPOW(BUS1,BUS2,DC1,SN,UN,TAU,Pref/0/,Qref/0/,UacRef/1/,
                 UdcRef_Inv/0.94/,Pctrl/I{0,1}/,UacCtrl/I{0,1}/,
                 IdOrd0/0/,IqOrd0/0/,D_UdcRef0/0/,TPW1,STATUS)
END
```

APPENDIX C DATASHEETS

C.1 Diode

V_{RRM}	=	6000	V
$I_{F(AV)M}$	=	1100	A
I_{FSM}	=	18×10^3	A
$V_{(T0)}$	=	1.5	V
r_T	=	0.6	mΩ
$V_{DC\text{-}link}$	=	3800	V

Fast Recovery Diode

5SDF 10H6004

Doc. No. 5SYA1109-02 Oct. 06

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Optimized for use as freewheeling diode in high-voltage GTO converters**
- **Industry standard housing**
- **Cosmic radiation withstand rating**

Blocking

Maximum rated values [1)]

Parameter	Symbol	Conditions	Value	Unit
Repetitive peak reverse voltage	V_{RRM}	f = 50 Hz, t_p = 10ms, T_{vj} = 125°C	6000	V
Permanent DC voltage for 100 FIT failure rate	$V_{DC\text{-}link}$	Ambient cosmic radiation at sea level in open air. (100% Duty)	3800	V

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Repetitive peak reverse current	I_{RRM}	$V_R = V_{RRM}$, T_{vj} = 125°C			50	mA

Mechanical data

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_m		36	40	44	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			200	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				0.83	kg
Housing thickness	H		26.2		26.6	mm
Surface creepage distance	D_S		30			mm
Air strike distance	D_a		20			mm

Note 1 Maximum rated values indicate limits beyond which damage to the device may occur

On-state

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. average on-state current	$I_{F(AV)M}$	Half sine wave, T_C = 85 °C			1100	A
Max. RMS on-state current	$I_{F(RMS)}$				1700	A
Max. peak non-repetitive surge current	I_{FSM}	t_p = 10 ms, T_{vj} = 125°C, V_R = 0 V			18×10^3	A
Limiting load integral	I^2t				1.62×10^6	A^2s
Max. peak non-repetitive surge current	I_{FSM}	t_p = 1 ms, T_{vj} = 125°C, V_R = 0 V			44×10^3	A
Limiting load integral	I^2t				968×10^3	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_F	I_F = 2500 A, T_{vj} = 125°C			3	V
Threshold voltage	$V_{(T0)}$	T_{vj} = 125°C I_F = 200...6000 A			1.5	V
Slope resistance	r_T				0.6	mΩ

Turn-on

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward recovery voltage	V_{FRM}	dI_F/dt = 500 A/µs, T_{vj} = 125°C			150	V

Turn-off

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery current	I_{RM}	di/dt = 300 A/µs, I_{FQ} = 1000 A,			1000	A
Reverse recovery charge	Q_{rr}	T_j = 125°C, V_{RM} = 2900 V,			6000	µC
Turn-off energy	E_{rr}	C_S = 3 µF (GTO snubber circuit)			5	J

Thermal

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}		-40		125	°C
Storage temperature range	T_{stg}		-40		125	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled F_m = 36...44 kN			12	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 36...44 kN			24	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 36...44 kN			24	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled F_m = 36...44 kN			3	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 36...44 kN			6	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_{th\,i}(1 - e^{-t/\tau_i})$$

i	1	2	3	4
$R_{th\,i}$(K/kW)	7.440	2.000	1.840	0.710
τ_i(s)	0.4700	0.0910	0.0100	0.0047

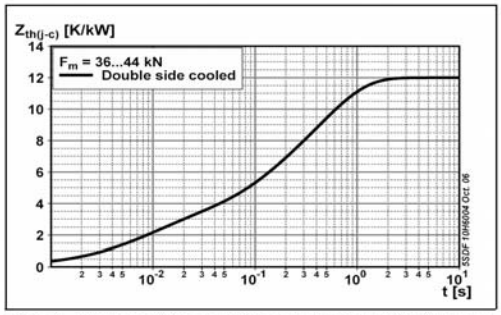

Fig. 1 Transient thermal impedance junction-to-case

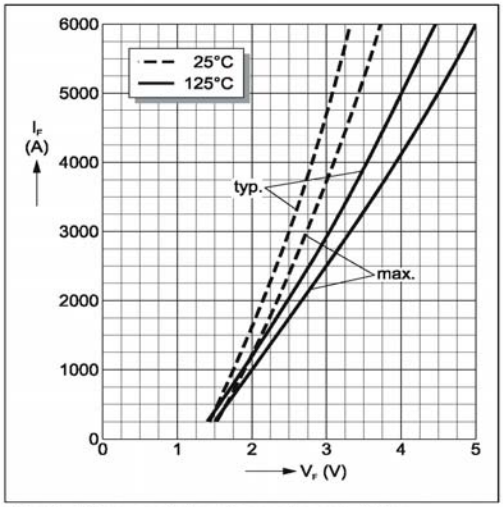

Fig. 2 Max. on-state voltage characteristics

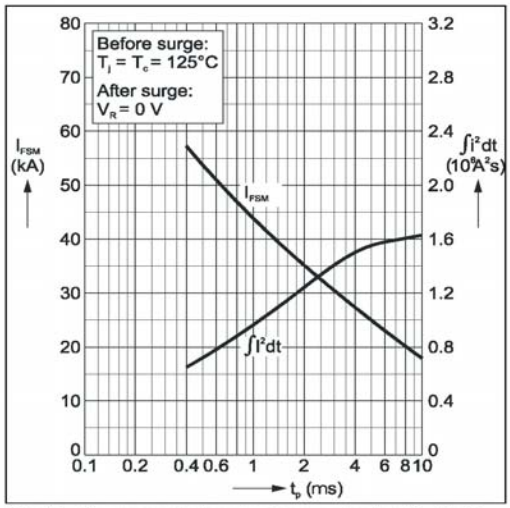

Fig. 3 Surge on-state current vs. pulse length. Half-sine wave

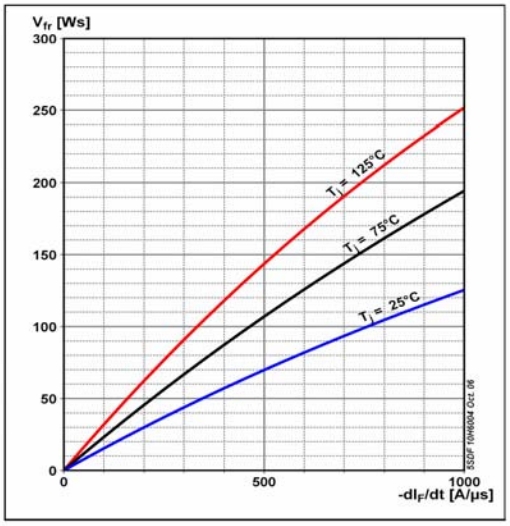

Fig. 4 Forward recovery vs. turn on di/dt (max. values)

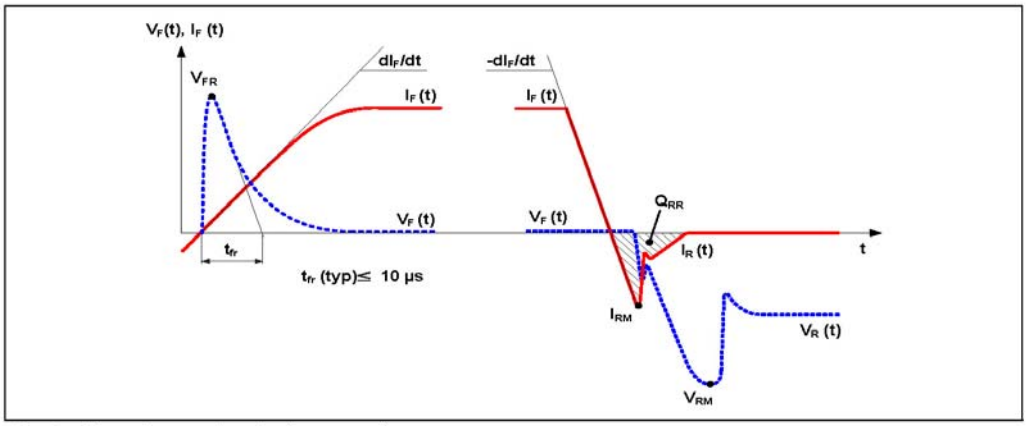

Fig. 5 General current and voltage waveforms

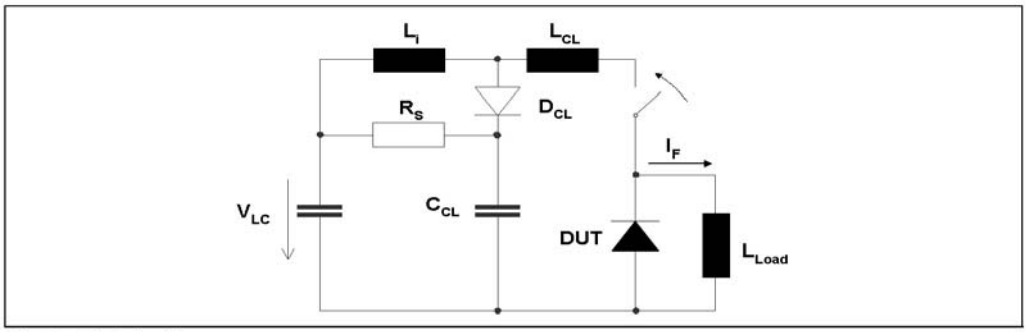

Fig. 6 Test circuit.

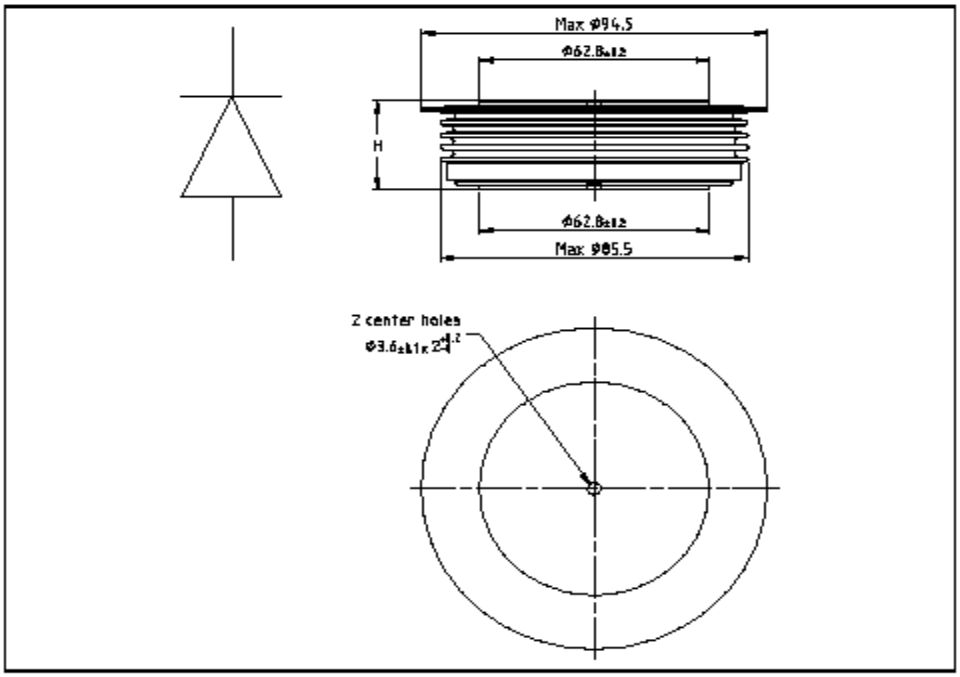

Fig. 7 Outline drawing, all dimensions are in millimeters and represent nominal values unless stated otherwise

Related documents:

Doc. Nr	Titel
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors
5SZK 9104	Specification of environmental class for pressure contact diodes, PCTs and GTO, STORAGE available on request, please contact factory
5SZK 9105	Specification of environmental class for pressure contact diodes, PCTs and GTO, TRANSPORTATION available on request, please contact factory

Please refer to http://www.abb.com/semiconductors for current version of documents.

ABB Switzerland Ltd
Semiconductors
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Doc. No. 5SYA1109-02 Oct. 06

C.2 Thyristor

V_{DRM}	=	6500 V
$I_{T(AV)M}$	=	3460 A
$I_{T(RMS)}$	=	5440 A
I_{TSM}	=	71.4×10^3 A
V_{T0}	=	1.24 V
r_T	=	0.162 mΩ

Phase Control Thyristor

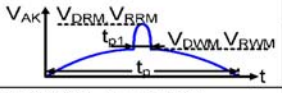
5STP 42U6500

Doc. No. 5SYA1043-03 May 07

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate**

Blocking

Maximum rated values [1)]

Parameter	Symbol	Conditions	5STP 42U6500	Unit
Max. surge peak forward and reverse blocking voltage	V_{DSM}, V_{RSM}	t_p = 10 ms, f = 5 Hz T_{vj} = 5…110°C, Note 1	6500	V
Max repetitive peak forward and reverse blocking voltage	V_{DRM}, V_{RRM}	f = 50 Hz, t_p = 10 ms, t_{p1} = 250 µs, T_{vj} = 5…110°C, Note 1, Note 2	6500	V
Max crest working forward and reverse voltages	V_{DWM}, V_{RWM}		3300	V
Critical rate of rise of commutating voltage	dv/dt_{crit}	Exp. to 3750 V, T_{vj} = 110°C	2000	V/µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DRM}	V_{DRM}, T_{vj} = 110°C			700	mA
Reverse leakage current	I_{RRM}	V_{RRM}, T_{vj} = 110°C			700	mA

Note 1: Voltage de-rating factor of 0.11% per °C is applicable for Tvj below +5 °C
Note 2: Recommended minimum ratio of V_{DRM} / V_{DWM} or V_{RRM} / V_{RWM} = 2. See App. Note 5SYA 2051.

Mechanical data

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		120	135	160	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				3.6	kg
Housing thickness	H	F_M = 135 kN, T_a = 25 °C	34.8		35.5	mm
Surface creepage distance	D_S		56			mm
Air strike distance	D_a		22			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

On-state

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, T_c = 70 °C			3460	A
RMS on-state current	$I_{T(RMS)}$				5440	A
Peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 110 °C, sine wave after surge: $V_D = V_R$= 0 V			71.4×10^3	A
Limiting load integral	I^2t				25.5×10^6	A^2s
Peak non-repetitive surge current	I_{TSM}	t_p = 8.3 ms, T_{vj} = 110 °C, sine wave after surge: $V_D = V_R$= 0 V			76.14×10^3	A
Limiting load integral	I^2t				24.6×10^6	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	I_T = 3000 A, T_{vj} = 110 °C			1.71	V
Threshold voltage	$V_{(T0)}$	I_T = 2000 A - 6000 A, T_{vj}= 110 °C			1.24	V
Slope resistance	r_T				0.162	mΩ
Holding current	I_H	T_{vj} = 25 °C			200	mA
		T_{vj} = 110 °C			100	mA
Latching current	I_L	T_{vj} = 25 °C			900	mA
		T_{vj} = 110 °C			700	mA

Switching

Maximum rated values [1)]

Parameter	Symbol	Conditions		min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	T_{vj} = 110 °C, I_{TRM} = 3000 A,	Cont. f = 50 Hz			250	A/µs
Critical rate of rise of on-state current	di/dt_{crit}	$V_D \leq$ 1880 V, I_{FG} = 2 A, t_r = 0.5 µs	Cont. f = 1Hz			1000	A/µs
Circuit-commutated turn-off time	t_q	T_{vj} = 110°C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs, $V_D \leq 0.67 \cdot V_{DRM}$, dv_D/dt = 20 V/µs		800			µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery charge	Q_{rr}	T_{vj} = 110°C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs	4000		5800	µAs
Reverse recovery current	I_{RM}		50		100	A
Gate turn-on delay time	t_{gd}	T_{vj} = 25 °C, $V_D = 0.4 \cdot V_{RM}$, I_{FG} = 2 A, t_r = 0.5 µs			3	µs

Triggering

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$			see Fig. 9		W

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	T_{vj} = 25 °C			2.6	V
Gate-trigger current	I_{GT}	T_{vj} = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 110 °C	0.3			V
Gate non-trigger current	I_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 110°C	10			mA

Thermal

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				110	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled F_m = 120...160 kN			4	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 120...160 kN			8	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 120...160 kN			8	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled F_m = 120...160 kN			0.8	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 120...160 kN			1.6	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	2.695	0.814	0.330	0.162
τ_i(s)	0.9692	0.1332	0.0177	0.0042

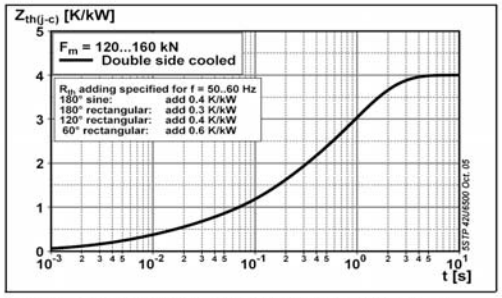


Fig. 1 Transient thermal impedance (junction-to-case) vs. time

Max. on-state characteristic model:

$$V_{T25} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 800 – 100000 A

A_{25}	B_{25}	C_{25}	D_{25}
123.8×10^{-6}	91.68×10^{-6}	192.1×10^{-3}	-2.905×10^{-3}

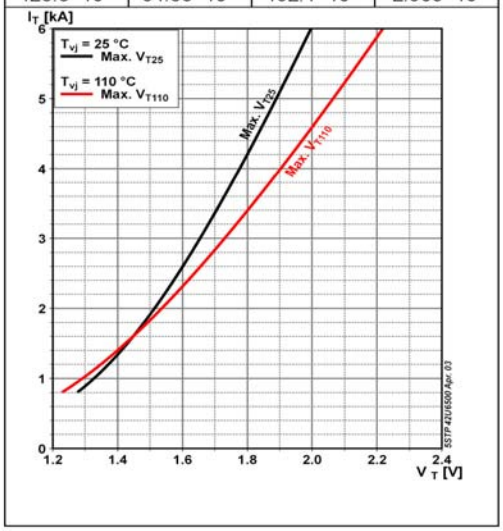


Fig. 2 On-state voltage characteristics

Max. on-state characteristic model:

$$V_{T110} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 800 – 100000 A

A_{110}	B_{110}	C_{110}	D_{110}
136.1×10^{-6}	117.2×10^{-6}	165.6×10^{-3}	957.5×10^{-6}

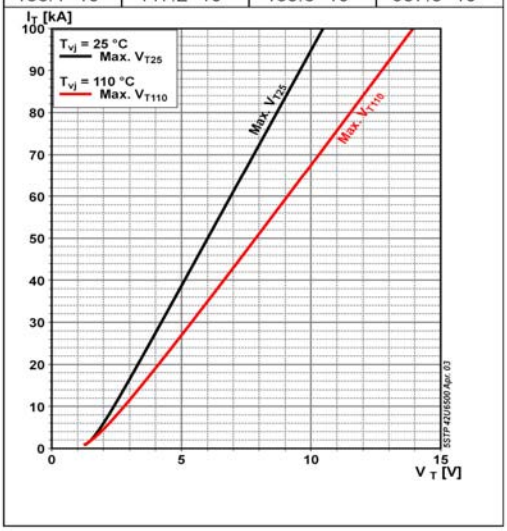


Fig. 3 On-state voltage characteristics

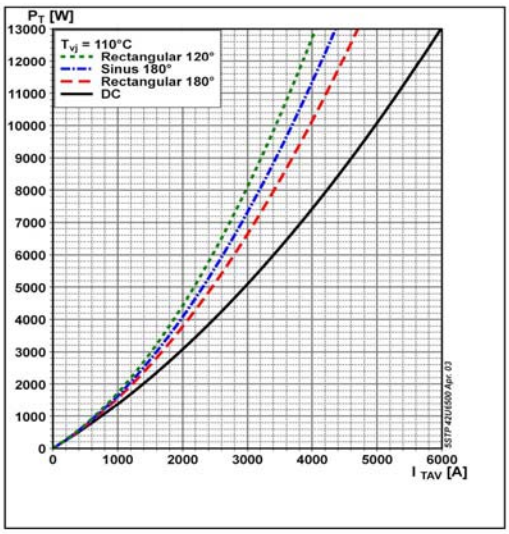


Fig. 4 On-state power dissipation vs. mean on-state current, turn-on losses excluded

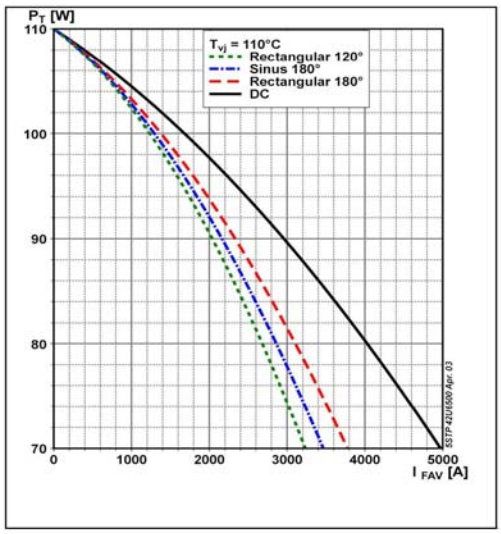


Fig. 5 Max. permissible case temperature vs. mean on-state current, switching losses ignored

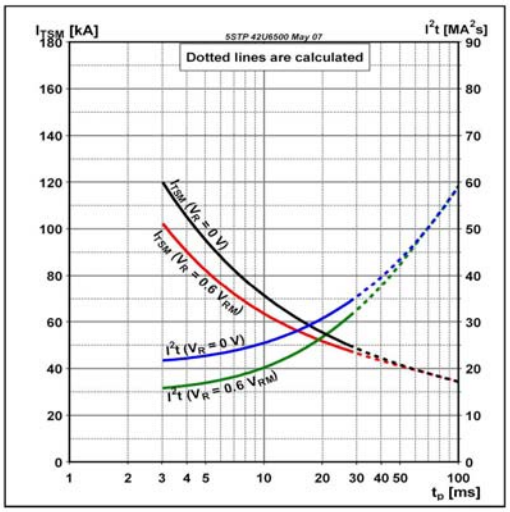


Fig. 6 Surge on-state current vs. pulse length, half-sine wave

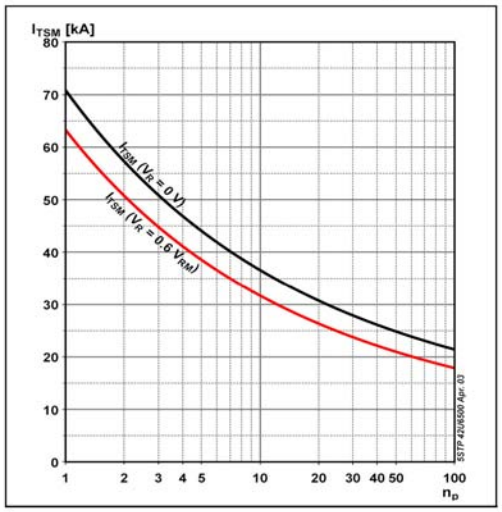


Fig. 7 Surge on-state current vs. number of pulses, half-sine wave, 10 ms, 50Hz

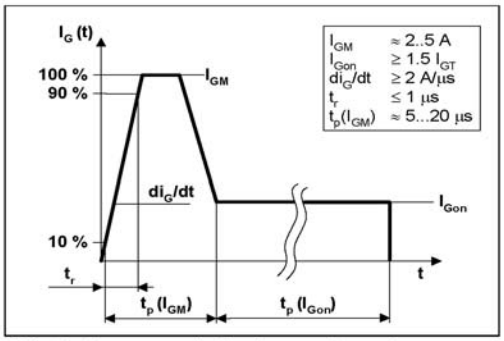


Fig. 8 Recommended gate current waveform

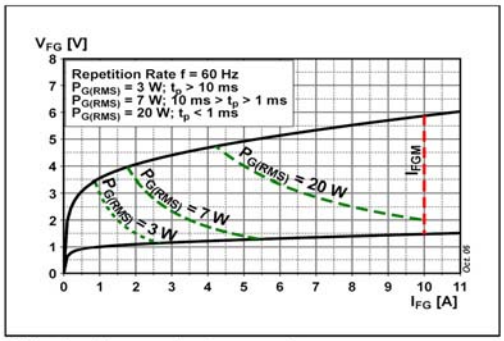


Fig. 9 Max. peak gate power loss

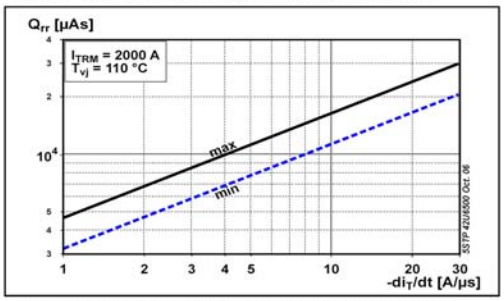


Fig. 10 Reverse recovery charge vs. decay rate of on-state current

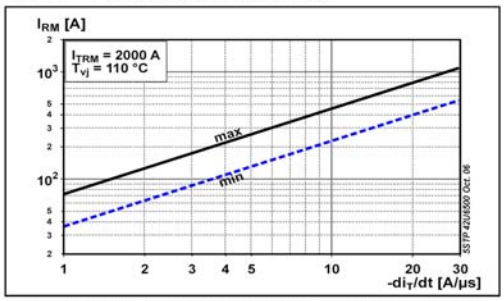


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current

Turn-on and Turn-off losses

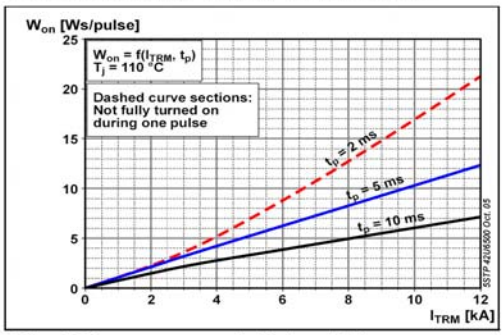


Fig. 12 Turn-on energy, half sinusoidal waves

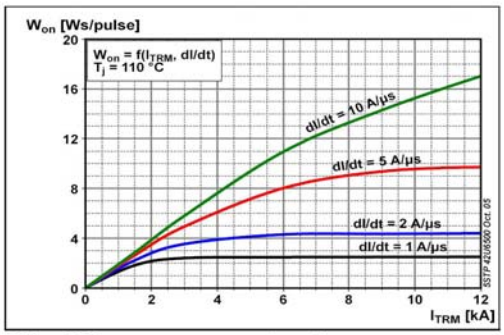


Fig. 13 Turn-on energy, rectangular waves

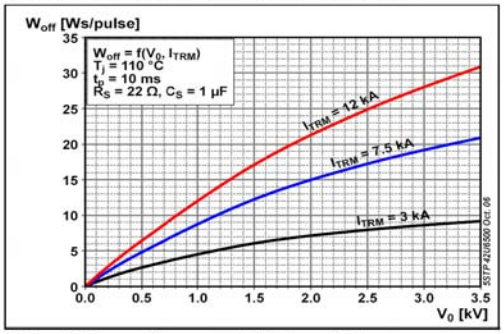


Fig. 14 Turn-off energy, half sinusoidal waves

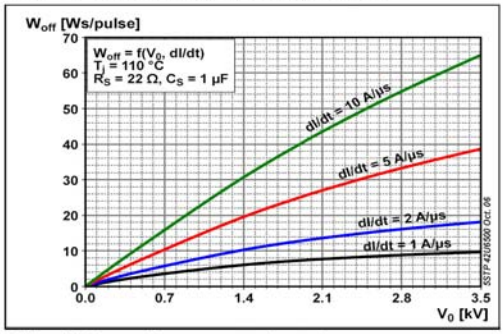


Fig. 15 Turn-off energy, rectangular waves

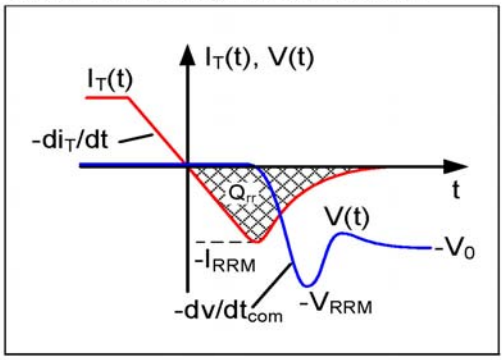


Fig. 16 Current and voltage waveforms at turn-off

Total power loss for repetitive waveforms:

$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

where

$$P_T = \frac{1}{T}\int_0^T I_T \cdot V_T(I_T)\ dt$$

Fig. 17 Relationships for power loss

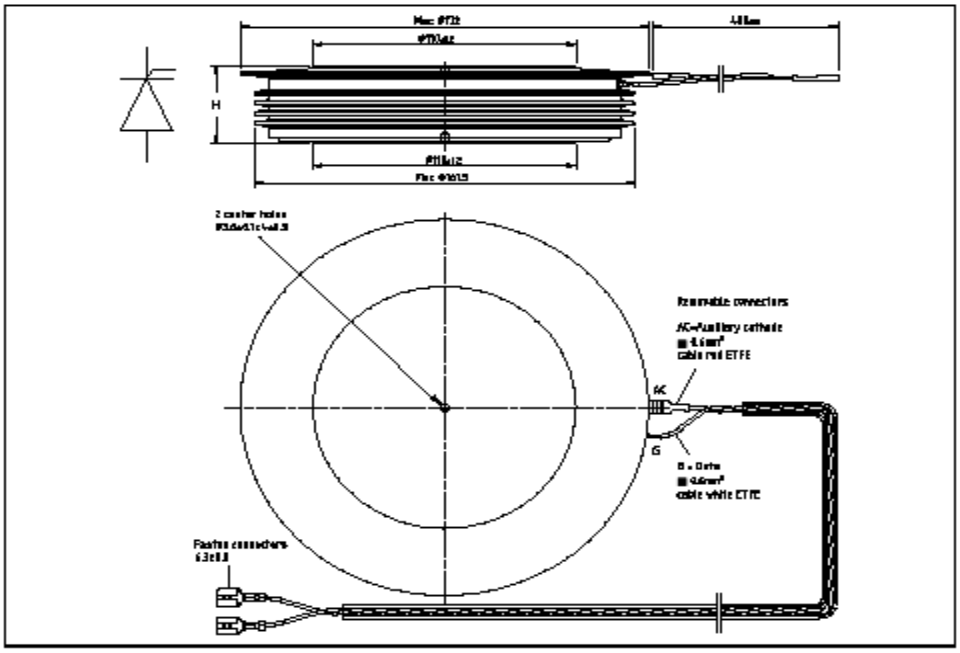


Fig. 18 Device Outline Drawing

Related documents:

5SYA 2020	Design of RC-Snubber for Phase Control Applications
5SYA 2049	Voltage definitions for phase control thyristors and diodes
5SYA 2051	Voltage ratings of high power semiconductors
5SYA 2034	Gate-Drive Recommendations for PCT's
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors
5SZK 9104	Specification of environmental class for pressure contact diodes, PCTs and GTO, STORAGE available on request, please contact factory
5SZK 9105	Specification of environmental class for pressure contact diodes, PCTs and GTO, TRANSPORTATION available on request, please contact factory

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