ABSTRACT

LOPATIN, SERGEI. Atomic and Electronic Structure of Interfaces in Materials Systems for Future Semiconductor Devices. (Under the direction of Gerd Duscher.)

Because of the intrinsic limits of the Si/SiO_2 based industry, there is a great trend towards the monolithic integration of new materials into already well developed silicon technology. Some of those materials are GaAs (which is widely used for production of light-emitting diodes, solar cells, and high-power transistors), Ge (which forms Si/SiGe heterostructures and thus opens the way for carrier mobility enhancement and band structure engineering), HfO_2 and Al_2O_3 (which are among the most promising materials for urgently required substitution of SiO_2 as a high-κ dielectric). These materials can be used for the fabrication of optoelectronic devices with improved characteristics. Having lasted for several decades now, downscaling reaches the limit, in which a critical device dimension approaches the size of one atom. At this level of the miniaturization, it is not the bulk material, but the interface between the two materials that what controls the properties of the resulting optoelectronic device. Thus, the characterization of precise atomic arrangements at different interfaces and the influence of these arrangements on the optoelectronic properties of interfaces is required (as identified in the International Technical Roadmap of Semiconductors - ITRS). Therefore, in this study, a combination of experimental scanning transmission electron microscopy (STEM) techniques and density functional theory calculations was used as a research tool for the characterization of interfaces between materials. The used methods consisted of atomic-resolution Z-contrast imaging and electron energy-loss spectroscopy, and modeling of different interface structures. The STEM instruments used for the study were equipped with

prototypes of spherical aberration correctors, enabling to achieve the highest resolution currently available both in space and energy. The above combination of experimental and theoretical methods was applied to study interfaces between Si/GaAs, Si/Ge, Ge/SiO$_2$, Si/HfO$_2$ and Si/Al$_2$O$_3$. All these materials interfaces play an important role in the contemporary semiconductor industry, have high potential for future applications and, thus, are currently under detailed investigation. As the result of the present research, a new dislocation configuration at the Si/GaAs interface was reported for the first time and the atomic structure model of this dislocation has been revealed. The influence of this dislocation structure on the electrical properties of the Si/GaAs interface was analyzed. Also, the transition from Si to GaAs and from Si to Ge at corresponding interfaces was described with atomic precision, focusing on the changing electrical properties of Si. For the first time, the interface between Ge and SiO$_2$ was shown to have "ideal" characteristics (chemical abruptness and sharpness). This indicates the potential, both for a more successful use of Ge in high-speed devices (it is shown to form an excellent interface with oxides) and for advances in interface engineering to enhance performance in electronic devices. The features of Si/HfO$_2$ and Si/Al$_2$O$_3$ interfaces, namely the distribution and bonding of Si and Hf across the interface, and the formation of charged SiO$_2$ islands at the Si/Al$_2$O$_3$ interface were also studied. These results for interfaces in materials systems, important for both the present state and the future of the semiconductor industry, show the significance of a basic understanding of the atomic structures of these interfaces for a rapid development of new electronic devices.

ATOMIC AND ELECTRONIC STRUCTURE OF INTERFACES

IN MATERIALS SYSTEMS FOR FUTURE SEMICONDUCTOR DEVICES
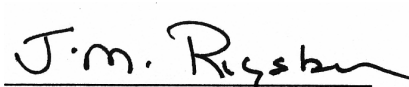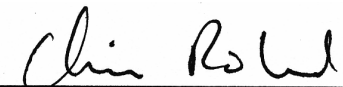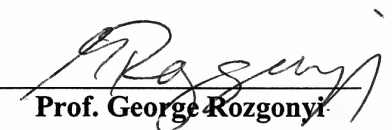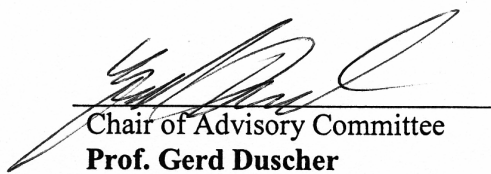
by

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A dissertation submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

MATERIALS SCIENCE AND ENGINEERING

Raleigh

2003

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BIOGRAPHY

Sergei Lopatin was born November 23, 1974 in Borisov, Republic of Belarus. He received his elementary and secondary education at high school #137 of the hero-city Minsk, Belarus, graduating with honors in 1991. He then began his college career joining Belarus State University, where he was a student at the Department of Physics, and where he received his Master degree in Physics graduating with honors in July, 1996.

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ACKNOWLEDGEMENTS

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1. INTRODUCTION

At present time the more and more increasing demands of the technology and communications market push the manufacturers of optoelectronic devices towards further reduction of the dimensions of the active device in the integrated circuits to obtain greater functionality and performance at lower cost. Traditional Si-based semiconductor technology has almost exhausted its own resources and future development is impossible without the introduction of other materials, such as GaAs (which is widely used for production of light-emitting diodes, solar cells, and high-power transistors), Ge (which forms Si/SiGe heterostructures and thus opens the way for carrier mobility enhancement and band structure engineering) and urgently required high-κ dielectrics for substitution of SiO_2 as an insulator.

Moreover, having continued for several decades, downscaling reaches the limit, where a single device dimension approaches the size of an atom. At such a level of miniaturization, the characteristics and behavior of resultant optoelectronic devices are controlled not by the properties of the bulk material, but rather by the interface between two materials. Thus, the characterization of precise atomic arrangements at different interfaces is urgently required for the understanding of the structure-property relationships.

While characterizing interfaces between materials, different issues can be addressed such as coherency, the existence of surface states and dangling bonds, chemical abruptness, problems with interdiffusion, thermal stability, etc. Without any doubt, the Si/SiO_2 interface has been the most studied and characterized from different point of views, because its excellent and so far unique properties determined the growth of the semiconductor industry for several decades. Enormous amounts of time and human resources were devoted to the investigation of the properties of this interface and it is naturally chosen in this study as a

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bench mark or reference point to compare or contrast with the properties of other interfaces investigated here. Hence, the present research is organized as follows.

The "Literature Review" section provides a summary of today's knowledge of Si/SiO_2 interface properties and its main advantages. The Si/SiO_2 interface is the benchmark that has to be met for any new materials system for almost every application. It is followed by the detailed consideration of current status of scientific research in the field of semiconductor and dielectric materials such as GaAs, Ge, HfO_2, and Al_2O_3, i.e. materials studied here.

The combination of scanning transmission electron microscopy techniques (Z-contrast imaging and electron energy-loss spectroscopy) and calculations based on the density functional theory is selected for the characterization of structure-properties relationships of $Si/GaAs$, Si/Ge, Ge/SiO_2, Si/HfO_2 and Si/Al_2O_3 interfaces. The description of those experimental and theoretical methods is given in the "Methods and Tools" section. Specific attention is concentrated on the advantages of spherical aberration corrector, the development of which pushed the resolution of electron microscopy to the truly atomic level.

The choice of materials (interfaces) is stipulated by the attempt to consider different sides of possible transitions from traditional Si and SiO_2 to other materials, i.e. first to consider structure-property relationships of Si as a crystalline semiconductor in contact with other crystalline semiconductors ($Si/GaAs$ and Si/Ge), then to focus the attention on the connection of amorphous SiO_2 with crystalline materials (Ge/SiO_2), and finally, to switch to the interfaces between Si and amorphous materials (Si/HfO_2 and Si/Al_2O_3). Such an approach determined the sequence of the results presented in "Results and Discussions".

At last, the summary of the obtained results and deductions as well as the directions of the future research is given in "Conclusion" section.

2. LITERATURE REVIEW

2.1. Si/SiO$_2$ Interface

The first working silicon transistor was built by Gordon Teal in 1954 when sufficiently pure silicon could be produced [1]. The next big jump in transistor evolution came with the development of the metal oxide semiconductor field effect transistor (MOSFET) in 1960 by John Atalla [1]. The silicon based MOSFET became the most common transistor in our days and the share of silicon devices in the world-wide market reaches an overwhelming 95%.

The tremendous growth of the Si-based industry over the last several decades is directly related to the combination of an easily available semiconductor and an excellent natural oxide, SiO$_2$, which serves as an insulator and as a protecting passivation layer. The combination Si/SiO$_2$ is the basis for the MOSFET that can be integrated monolithically in enormous quantities in a very large-scale integration (VLSI) technology [2].

There are a number of factors determining the excellent chemical, mechanical and electrical properties of the Si/SiO$_2$ interface. First among these are the flexibility of the amorphous SiO$_2$ network and the high potential for glass formation. When oxidized, Si forms four bonds to oxygen atoms. The Si–O bond is about 50% ionic and the ionicity is below a critical value, so the bond is qualitatively covalent and directional [3]. The oxygen atoms are two-fold coordinated, with a large bond angle and a weak bond-bending force constant. The low average coordination and the "floppiness" of the oxygen site mean that SiO$_2$ is a very good glass-former [4].

As a result, in terms of charged defects the Si/SiO$_2$ interface is so far unique. Even though the Si oxidation process causes a 120% volume expansion, the defect density and stress are low. The flexibility of the SiO$_2$ network, and particularly of the oxygen site, is

enough to minimize the number of interface dangling bonds. The same works not only for the interface but for the oxide layer itself.

In general, defects in the oxide are critical to its performance as a gate dielectric. Defects in SiO_2 are well understood. As a covalent solid, its defects are (1) dangling bonds on Si and O atoms and (2) the oxygen vacancy, known as the E' center. Si dangling bonds are undesirable because they form states in the middle of the Si bandgap that can trap charge. Si dangling bonds in the SiO_2 can trap charge and can also cause soft (reversible) breakdown. However, the defect density in SiO_2 is very small, primarily because its large cohesive energy makes defects energetically costly and also because the flexibility of its network allows them to reconstruct. More over, there is an additional method for removing dangling bond defects, i.e. the injection of hydrogen. Hydrogen atoms diffuse rapidly in SiO_2 and can passivate any dangling bonds at the Si/SiO_2 interface or the SiO_2 layer, and so remove these states in the gap:

$$\equiv Si' + H' \rightarrow \equiv Si\text{–}H.$$
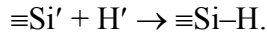
The density difference of Si and SiO_2 due to the volume expansion creates certain difficulties in devising atomic models of the interface. Despite extensive work, neither the atomic-scale structure nor the composition (or gradient) in the transition region are well understood – there has been no universally accepted "conventional" model [5]. But the existing crystalline models suffice to show the main issues. There are more dangling bonds on the ideal Si surface than on a SiO_2 surface because of the density difference. To join a Si lattice to a SiO_2 network, some Si bonds on the Si side must be tied off to each other. This can be done by pairing off dangling bonds on the Si surface as Si–Si bonds or by placing

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bridging oxygens between the pairs. The remaining Si dangling bonds are then connected to oxygen dangling bonds on the SiO_2 side to give a defect-free interface.

Also, different models say that between a crystalline Si substrate and an amorphous oxide overlayer there is a transition region consisting of a mixture of Si in various oxidation states: Si^{1+}, Si^{2+}, Si^{3+}, where Si has one, two, and thee first nearest-neighbor oxygen atoms, respectively. Si^{x+} (x=1,2,3) is also frequently referred to as suboxide. Together with dangling bonds those suboxides introduce energy levels in the bandgap, thus degrading the quality of a dielectric. Recent experiments of Muller *et al.* [6] demonstrated that in the best case it takes at least 2 monolayers of mixed suboxide for the transition from the Si substrate to the stoichiometric SiO_2.

Buczko et al. [7] addressed the mechanisms that control abruptness of the Si/SiO_2 interfaces by considering the energetics of different possible structures produced by "theoretical" layer-by-layer deposition of SiO_2 onto Si (see Figure 1). In the case of the Si (001) surface, a set of judiciously chosen *ab initio* calculations suggest that abrupt interfaces (those with one layer of only Si^{2+} oxidation states directly followed by Si^{4+}, i.e. stoichiometric SiO_2) generally have lower energy. The origin of this result can be traced to the softness of the $Si-O-SiO_2$ angle and the particular geometry of this surface, which imposes order in the interface layer. These effects make suboxide bonds energetically costly, thus setting the stage for potentially perfect interfaces.

However it is noted in [7], that the entropic considerations that normally introduce defects (in this case, suboxide bonds) to lower the free energy at finite temperatures must be taken into account. Moreover, two distinct but energetically degenerate ordered structures are possible at the interface region. Inevitably, the real Si/SiO_2 interface structures are made of

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two types of domains. It is these domain boundaries, plus entropy effects within domains, that are the likely cause of the observed suboxide [6] and dangling bonds [8].
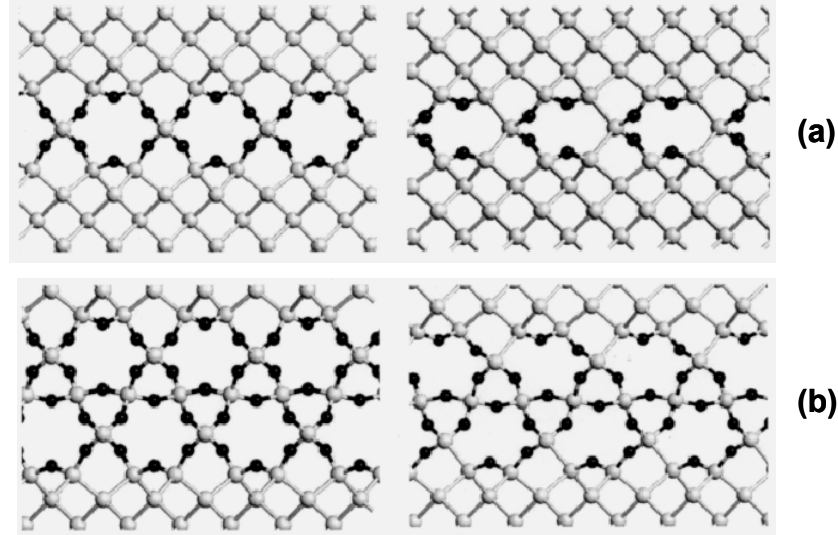
Figure 1. Examples of Si-SiO$_2$-Si superstructures with one (a) and two (b) oxide layers. The left panels are abrupt interfaces; the right panels have suboxide bonding (after [7]).

So there are natural limitations for the minimum thickness of SiO$_2$ layer to serve as a gate dielectric. While those limits are not reached, the use of amorphous, thermally grown SiO$_2$ as a gate dielectric in complimentary-metal-oxide-semiconductor (CMOS) processing offers several key advantages:

- The very high SiO$_2$ bandgap of nearly 9 eV, and a Si/SiO$_2$ potential barrier for electrons (conduction band offset) of more than 3 eV, making SiO$_2$ an excellent insulator (resistivity $\geq$ $10^{15}\Omega$ cm) even when the layer thickness is reduced to a few nanometers.

- Thermal and chemical stability, needed for the high-temperature processing and mass production of integrated circuits.

- The high quality of the Si/SiO$_2$ interface. In modern CMOS processing, defect charge densities are of the order of ~10^{10}/cm^2, and mid-band gap interface-state densities are

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~10^{10}/cm^2 eV. This, in part, results from post-annealing in a hydrogen-containing ambient, which passivates dangling bonds. This excellent interface allows for high mobility of the carriers in the MOSFET channel and high device performance.

- Low charge trapping and splendid reliability.

All these properties of Si/SiO$_2$ interfaces combined together are the key to the fabrication of more than 40 million transistors with identical electrical behavior on a single Si chip as is commercially available in our days.

2.2. Si/GaAs Interface

Compound semiconductor materials and devices have been the topic of research for more than 30 years by a large number of engineers and scientists in a large number of varied institutes. Gallium arsenide (GaAs) is a III-V compound semiconductor and probably the second most common semiconductor material after Si. It has some unique properties that make it ideal for use in applications that silicon is ill-suited for.

Table 1. Comparison of some basic materials properties of Si and GaAs at room temperature (from [9]).

		Silicon	Gallium Arsenide
Lattice constant (Å)		5.43	5.65
Energy gap (eV)		1.12	1.42
Band gap type		Indirect	Direct
Bulk mobility (cm^2 V^{-1} s^{-1})	**Electrons**	1450	8500
	Holes	505	400
Thermal conductivity (W cm^{-1} °C^{-1})		1.4	0.46

Gallium arsenide forms a face centered cubic lattice with a basis of one gallium and one arsenic atom in what is called a zincblende structure. Table 1 compares some fundamental properties of GaAs and Si [9]. The energy difference of 0.3 eV in the bandgap has a profound effect on the intrinsic properties of these semiconductors. First of all is the high isolation and low parasitics enjoyed by GaAs devices.

The direct nature of the energy gap in GaAs, in contrast to Si, is the origin of the highly favorable optical transition probabilities. This single factor explains the existence of the highly efficient photoluminescence properties of GaAs, as well as justifying its suitability for fabrication of light emitting diodes and lasers.

The charge carrier mobility of GaAs is probably the most advertised parameter of this semiconductor. The charge carrier mobility μ is itself the most important transport parameter of a semiconductor material. It describes the linear relation between the average carrier drift velocity v and an external electrical field E in the low-field limit (and in the absence of external magnetic fields):

$$v = \mu \cdot E .$$

The electron mobility in GaAs is significantly higher than that in Si, and it is this parameter which allows the higher speed performance of GaAs devices over Si. However the hole mobility in GaAs is significantly lower than the electron mobility and this disparity leads to a less favorable situation for the possibility of implementing complimentary device structure for circuits in GaAs.

At the same time the thermal conductivity of GaAs is almost a factor of 3 worse than that of Si. That means there is an inherent limitation of GaAs crystals in moving heat from device areas to the heat-sinking areas.

High performance applications of GaAs are found ranging from wireless communications and digital synthesis, through high speed computing. One of the earliest reports of a high performance GaAs IC was recorded in 1974 [10], which referred to Schottky metal-semiconductor field effect transistors (MESFETs) fabricated on semi-insulating (SI) GaAs substrate. Today the GaAs MESFET is the fundamental block of GaAs IC technology. However, other III-V technologies have also been developed, and offer different combinations of advantages and disadvantages. The junction field effect transistor (JFET) is very closely related to the MESFET. The major difference is that JFET uses a pn-junction rather than a Schottky barrier as a control element. The use of a pn-junction results in a larger barrier height, almost as large as the energy gap. JFET technology has been demonstrated to be capable of fabricating low power/high density random access memory (RAM) with high radiation tolerance [11], as well as high density/high speed LSI gate arrays [12].

Both MESFET and JFET IC are typically fabricated by ion implantation into bulk SI GaAs wafers. In contrast, a number of advanced III-V devices are fabricated on epitaxial layers of III-V compounds. Epitaxial material technology can also be used for homostructures, but this crystal growth technology opens the door to the world of heterostructure devices. Heterostructure FET technologies utilize at least two III-V compounds with different bandgap energies. They are based on the same fundamental principle, and are known by the variety on names: the selectively doped heterostructure transistor (SDHT), the high electron mobility transistor (HEMT), the two-dimensional electron gas field effect transistor (TEGFET), the modulation doped FET (MODFET), and the heterostructure insulated gate FET (HIGFET) [13]. The heterojunction bipolar transistor (HBT) is also a grown epitaxial structure. The major advantage of those devices is that they

have a very high transconductance and the potential for very high speed operations (analog signal processing, analog-to-digital conversion, microwave power amplification).

There are several other III-V device technologies which are based on epitaxial materials. These include: resonant tunneling diodes (RTD), hot electron transistors (HET), permeable base transistors (PBT), semiconductor-insulator-semiconductor FETs (SISFET), the metal-insulator-semiconductor FETs (MISFET), and pseudomorphic HEMTs (P-HEMT). These are all epitaxial devices and, thus, they have a potential to be fabricated in the (III-V)-on-Si configuration.

The epitaxy of gallium arsenide on silicon has a number of objectives [14]. GaAs may serve as a material system by itself, for example GaAs/AlGaAs lasers and photodetectors can be used for interchip communication in Ultra Large Scale Integrated (ULSI) circuit systems. On the other hand, GaAs may serve as a base system (substrate) for integrating other compound semiconductors to silicon, i.e. other compound semiconductors can be grown on Si substrates using a GaAs buffer layer. In this way, for instance, InSb based infra-red detectors can be monolithically integrated to the Si based charge coupled devices (CCD) image processing systems.

Besides monolithic integration, the GaAs epitaxy on Si has many other advantages. The important ones are as follows.

• Large diameter wafer production requires a highly developed technology. GaAs on Si allows for exploitation of the mature Si wafer technology to produce large diameter GaAs epilayers that can just as effectively function as "GaAs substrates".

• Since Si has a superior thermal conductivity and GaAs has better electronic properties (Table 1), then the Si/GaAs heteroepitaxial system may exploit the individual

properties of the constituents to yield a highly optimized overall system. As a result, GaAs circuits fabricated on Si substrate can exhibit higher resistance to thermal burnout and runaway than those fabricated on GaAs substrate.

- Silicon also exhibits superior mechanical properties. To achieve the same mechanical strength as GaAs on Si, the GaAs on GaAs requires thicker substrate. Thicker substrates increase the cost and weight, and may require new processing equipment to accommodate the increase in thickness. Especially for space-based applications like solar cells on satellites, the GaAs on Si is a better choice than GaAs on "thicker" GaAs.

- Si wafer cost practically a small fraction of GaAs wafer. The process of epilayer growth is expensive, but for structures that inherently require epitaxial growth, i.e. heterostructures, MODFETs, quantum wells, etc., the extra effort involved in the growth of GaAs on Si is insignificant.

As a result of the impressive progress in epitaxial growth of GaAs on Si, all the main electrical and optical GaAs devices and GaAs buffered devices grown on Si substrate have been successfully demonstrated and their properties have been compared with the same devices grown on GaAs substrate. Majority-carrier devices have demonstrated properties equivalent to their counterparts on GaAs. For example, FETs, being majority-carrier devices, are less sensitive to crystal quality then lasers and other minority-carrier devices. Consequently, FETs were the first devices to be realized in GaAs on Si. The first report of the fabrication of GaAs MESFETs on Si was from Choi *et al.* through the use of Ge intermediate layers [15]. Shortly thereafter the same group reported MESFETs directly grown on Si [16]. Although the overall performance of these MESFETs was quite

comparable with MESFETs on GaAs substrates, the noise performance was considerably degraded due to the presence of structural defects.

The issue of defects at the Si/GaAs interface (first of all dislocations) is even more serious for minority charge carrier devises such as bipolar transistors, light emitting diodes, detectors and solar cells. For example, since Si has a density less than a half of GaAs and may be used as a light-weight substrate, a single-crystal cascade with Si as the bottom cell and a III-V alloy on the top looks promising for concentrator solar systems, especially for those destined for space-based operation. Such cells, with each material absorbing in a different portion of the solar spectrum, could achieve conversion efficiencies as high as 36% [17]. However, recombination losses at dislocations are the limiting factor in determining the performance of Si/GaAs solar cells. The first Si/GaAs solar cells yielded conversion efficiencies of 12 % (AM1) [18], but there are indications [19], that the reduction of dislocation density may significantly improve Si/GaAs solar cells characteristics.

In general, the epitaxial growth of GaAs on Si is not without inherent problems. The important ones among the many are growth initiation of a polar (GaAs) semiconductor on a non-polar one (Si), the 4.1% lattice mismatch between silicon and gallium arsenide (Table 1), and the 60% mismatch in thermal expansion coefficient. The quality of the surface is also critical for epitaxial growth.

The surfaces of all semiconductors contain steps in the atomic scale, including the surface aligned along the principal low index planes. Steps are simply atoms missing from their places in the crystal. The crystal has an ideal surface up to the step, and beyond the step edge the surface atoms correspond to "second-layer" atoms in the ideal surface. When just a monolayer of atoms is missing, the step is said to be a monolayer high. The edge atoms at the

step are similar to the surface atoms and have dangling bonds; some of these dangling bonds may rebond at the step edge. The rebonding of edge dangling bonds influences the formation energy and stability of steps and can be altered by high temperature or chemical treatment.

The presence of monolayer high surface steps can lead to antiphase domains in GaAs on Si. The crystalline structures of Si and GaAs consist of two interpenetrating face centered cubic Bravais lattices. In the case of Si, the two f.c.c. are the same. It is invariant of rotation of $\pi/2$ and [011] and [$01\bar{1}$] direction are equivalent. In the case of GaAs, one f.c.c. lattice is occupied by Ga and the other by As, and the [011] and [$01\bar{1}$] directions are not equivalent. This distinction is very visible in the (100) planes of GaAs which consist of alternating layers of Ga and As. When GaAs is grown on GaAs substrate, the Ga and As atoms experience no ambiguity in choosing lattice sites, but that is not the case when epilayers of GaAs are grown on Si (100). The lattice sites on the (100) planes are indistinguishable and so there are no preferential nucleation sites for Ga and As. To make matters worse, silicon bonds well to both Ga and As. If the growth is started with simultaneous exposure to gallium and arsenic molecular beams, gallium may form the initial layer on some areas of the substrate and arsenic on the rest of the surface, i.e. the first monolayer is part Ga and part As on the Si substrate. This results in As-As or Ga-Ga bond boundaries which are called anti-phase boundaries (APBs). The formation of APBs is aided by monolayer high steps. Anti-phase boundaries are charged structural defects. The epilayer containing APBs may behave as a highly compensated semiconductor degrading the performance of devices fabricated on it. However, the formation of APBs requires large energies, and inherent growth kinetics may not favor them. So it is possible to grow APB-free epilayers in spite of the presence of monolayer high steps [20].

More serious problem of manufacturing GaAs devices integrated in silicon technology is associated with the lattice mismatch of 4.1% between GaAs and Si. This mismatch leads to the creation of a large number of interfacial dislocations (misfit dislocations). Dislocation densities of the order of 10^6 cm^{-2} are generally observed at the GaAs/Si interface.

Dislocations affect the quality of the epilayer in several different ways. For instance, introducing dangling bonds, they form non-radiative recombination centers. The number of these centers can be even increased under intense photon fluxes, such as those in lasers. Another example is the increase in the ease of impurity diffusion and segregation along the line of dislocation threading; thus Si can diffuse from the substrate and cause autodoping in the epilayer.

Dislocations are often specified in terms of Burgers vectors. The commonly occurring dislocations in zincblende and diamond semiconductors can be classified in two different ways: (1) those whose Burgers vectors are parallel to the growth (Si/GaAs interface) plane and (2) others. The former is called a type I dislocation and the latter type II [21].

If the crystal growth direction is [001] and the dislocation line direction is [1$\bar{1}$0], then Burgers vectors [101]/2 and [01$\bar{1}$]/2 both form a 60° angle with the dislocation line (type II dislocations). These 60° dislocations may originate from the steps on the free surface [22]. These two dislocations may react to form a type I dislocation with a Burgers vector of [110]/2, which is perpendicular to the dislocation line (90° dislocation). The 90° dislocation relieves the strain energy more efficiently than other dislocations because it is aligned with the strain relaxation direction.

Dislocations generally move by slip along crystallographic planes which contain both their Burgers vector and the dislocation line, i.e. the (100) plane for type I dislocation and

(111) plane for type II dislocation. The (111) planes are easy slip planes in GaAs. So type II dislocations can easily move up through the GaAs epilayer and reach the surface. Such a propagation of dislocations from the interface through the epilayer is called threading. Besides causing impurity diffusion, threading lines also cause partial short circuiting of p-n junctions and degradation of optical and electrical properties of epilayers.

In the last few years, the dependence of interface dislocations on growth conditions and post growth treatment has been investigated extensively and a number of promising techniques have been proposed for the reduction of dislocation densities and strain in hetero epitaxially grown layers to achieve high performance devices on Si [23, 24, 25], and yet it remains a serious issue. It should be mentioned that the lattice mismatch between GaAs and another "popular" semiconductor material, namely Ge, is much lower that for Si, which may benefit the combined integration of GaAs and Ge into Si technology. So it is the Ge to be discussed in the next section.

2.3. Si/Ge Interface

The properties of the Si/SiO$_2$ material system make it ideally suited for digital applications with a very high level of complexity. On the other hand, a variety of fast-growing market segments, especially in the areas of millimeter-wave and optical communication, appear to be outside the scope covered by the electronic and optoelectronic properties of Si. Therefore, in the last 30 years a substantial research and development effort has been dedicated to the development of alternative semiconductors with superior high-frequency behavior and optoelectronic functionality. For example, the properties of many III–V compound semiconductor heterostructures have been investigated thoroughly, and

several device types are now available commercially. Prominent examples are quantum well transistors (often referred to as HEMTs (high-electron-mobility transistors) or MODFETs (modulation-doped field-effect transistors)) and quantum well lasers. Both exploit the band offset of a heterostructure for the confinement of carriers in a quantum well defined by the energetically favorable material. HEMTs with high-frequency cut-off frequencies of several 100 GHz have been demonstrated, which are far beyond anything conceivable with Si transistors.

However, although properly designed III–V heterostructures can excel in almost every category of electronic and optoelectronic properties, they completely lack a natural oxide or other insulator with the quality and versatility required for a very large-scale integration (VLSI) technology. The problems associated even with a moderate level of integration density are thus a fundamental drawback of III–V compound heterostructures, which will restrict the market volume that can be addressed by these materials in the near future.

The analysis of the benefits and limitations of the semiconductor systems presently employed for commercial devices may suggest that a combination of the Si/SiO$_2$ system (with its VLSI capability) and a heterostructure (enabling the design freedom of bandgap and band offset) could be a very powerful means for expanding the performance range of contemporary integrated circuits (ICs). For example, it has been known for many years that by adjusting the semiconductor bandgap, the bipolar device switching speed can be boosted.

As a straightforward step in that direction, the growth of GaAs and other III–V mixed semiconductors on Si substrates has been pursued for quite some time [14]. The successful production of light emitting diodes [26] and FETs fabricated that way was demonstrated. As a result, over the past seven to ten years those materials have captured a large portion of

today's highest performance applications. Functionality improvement using these rather exotic materials, however, comes at a high price — cost and manufacturability. Moreover, the substantial lattice mismatch and anti-phase boundary formation in the III–V heterostructure make this a troublesome combination of materials in terms of epitaxial growth and long-term stability of the devices. In this respect, the $Si/Si_{1-x}Ge_x$ is a much better suited heterosystem, because of "natural" matching of Si and Ge.

The existence of Ge was predicted by Russian chemists Mendeleev in 1871 as "Ekasilikon" and the element was found by Winkler, a professor of chemistry, in 1886 and was given a name after the country of discovery (Germany). Ge is a silvery-white brittle semiconductor of the carbon group in the periodic table. It is stable in air and water and is unaffected by alkalis and most acids. Its physical properties are very similar to those of Si which precedes it in the same group. Whereas Si is almost the most abundant element on earth, Ge is found only in trace amounts in some coals and ores. Pure Ge is produced by reduction of the oxide and ultra high purity material is obtained by zone refining. It is this material that was used for the creation of the very first solid state amplifier, earning Bardeen, Brattain and Shockley the Nobel Prize in Physics in 1956 [1].

The structural and chemical properties of Ge and Si are very similar, which eases epitaxial growth and the application of standard Si technologies. Silicon and germanium are the only group-IV elements that are completely miscible, i.e. they form a continuous series of solid substitutional solutions with gradually varying properties (such as resistivity) over the entire composition range. The elements and the random Si_xGe_{1-x} alloys crystallize in the cubic diamond lattice with a lattice parameter that increases almost linearly [27] with x. The maximum mismatch amounts to 4.2% between pure Si and pure Ge. The fundamental

bandgap in both Si (1.1 eV) and Ge (0.66 eV) is indirect, and remains so for all compositions in the Si_xGe_{1-x}. Though the bandgap variation is strongly effected by strain in Si_xGe_{1-x} crystal, the band structure can be tuned within the relatively wide margins given by pure Si and Ge by means of these alloys.

As mentioned in (2.2), the most important transport parameter of a semiconductor material is the carrier mobility μ. The mobility μ is directly proportional to the transport scattering time τ and indirectly proportional to the effective mass m^* of the respective carrier:

$$\mu = e \cdot \tau / m^*,$$

where e is the electron charge.

Table 2. Room-temperature bulk mobilities of electrons and holes in unstrained, undoped Si and Ge (from [9]).

		Silicon	Germanium
Bulk mobility (cm^2 V^{-1} s^{-1})	**Electrons**	1450	3900
	Holes	505	1800

Within the limits of the wave-vector-independent relaxation time approximation, τ is the sum of all reciprocal scattering times associated with the various scattering mechanisms. Thus the mobility is limited by the mechanism with the smallest scattering time. The main scattering mechanisms in the elemental (nonpolar) semiconductors are scattering at acoustic and optical phonons ('lattice scattering'), and scattering at ionized and neutral impurities [28]. In Si_xGe_{1-x} crystals, random alloy scattering contributes as a fourth independent mechanism. Strain may affect all scattering mechanisms.

The smaller effective mass of Ge [9] contributes to the significantly larger values of both electron and hole mobilities compared to those of Si (see Table 2 for comparison and as a

reference for the subsequent examples). The hole mobility of Ge is especially worth mentioning, since it is higher than in any of the III–V compounds, and matches the electron mobility of Si to within 20%.

At the present time Ge is a semiconductor material, industrially used for the large-scale production of various electronic devices, such as, for example Ge photocapacitive MIS infrared detectors [29], light emitting diodes [26], and for rather unknown applications such as solar cells, that provide the electrical supply of telecommunication satellites [30]. Even the Ge-nanocrystal films deposited by the cluster-beam evaporation technique are attractive materials for application to light emitting devices in future [31]. But it is the enhanced electron and hole mobilities and the possibility of the band structure tailoring in combination with Si, that attracts the most attention to Ge. The obvious advantages of $Si/Si_{1-x}Ge_x$ heterosystems were recognized at an early stage of heterostructure research, with the first report on the Si/SiGe superlattice appearing back in 1975 [32].

The enhancement of carrier mobility is one of the most attractive features derived from the band engineering utilizing $Si/Si_{1-x}Ge_x$ heterostructures and it can open the way to surpassing the limit of conventional Si MOSFETs. Especially, the hole mobility of Si-based materials which limits the performance of complementary MOS type circuits is expected to be enhanced by the strain originating from the lattice mismatch in SiGe heterostructures. Thus, for example, Irisawa *et al.* [33] reported that solid source molecular beam epitaxy was used for a successful growth of $Si_{0.3}Ge_{0.7}$/strained Ge channel/$Si_{0.3}Ge_{0.7}$ heterostructures with ultrahigh hole mobility on Si (100) substrates. Suppression of parallel conduction, which commonly exists in SiGe heterostructures was achieved by employing n-type doping in thick SiGe buffer layers, which resulted in the drastic increase of room-temperature (RT) Hall hole

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mobility up to 2100 cm^2/V·s. Using this technique, p-type MOSFETs without parallel conduction are successfully fabricated and the peak effective hole mobility of 2700 cm^2/V·s at RT was obtained, which is much higher than that of bulk Ge drift mobility [9]. The main reason for large enhancements of the mobility are the very small effective mass of holes in the strained Ge (~0.01 of free electron mass) and the absence of alloy scattering which can be a dominant scattering mechanism in SiGe alloy.

Since SiGe allows a change of the bandgap by varying the Ge content of the alloy, SiGe also seems to be a promising material for a perfect spectral match of a photocell to a given thermophotovoltaics emitter. SiGe photocells can either be produced from SiGe wafers or from thin, epitaxial structures on Si substrates. Bulk SiGe can be ruled out as substrates, both because of the inherent problems of pulling homogeneous SiGe crystals, and because such substrates would jeopardize the one advantage of the Si/SiGe heterosystem, namely its compatibility with existing silicon technologies. It is therefore mandatory to employ Si substrates. For the review of recent achievements and problems in this area see Bitnar [34].

As was mentioned above, for Si$_x$Ge$_{1-x}$ alloys, the lattice parameter increases almost linearly with x. As a result, it is possible to engineer a virtual substrate to match the lattice parameter of the desired material. A virtual substrate is essentially either a SiGe layer on Si substrate with linearly grading Ge concentration forming a strain-relaxed substrate or a dislocation-free strain-relaxed SiGe-on-insulator (SGOI) layers, which successful production for MOSFETs is already demonstrated [35]. Thus because there is only a 0.07% lattice mismatch between GaAs and Ge, the virtual substrate, graded from Si to 100% Ge, can be used to obtain high-quality GaAs thin films with threading dislocation densities <3·10^6 cm^{-2} [36] and InGaAs quantum wells, which outperform those on pure Ge substrates in terms of

the luminescent efficiency [37]. Those GaAs films, grown on the SiGe virtual substrates, in their turn allowed the construction of working optical links, consisting of a GaAs PIN-LED as the light source, a waveguide and a GaAs PIN detector diode.

Silicon-based heterostructures with high electron and hole mobilities have come a long way from the discovery of strain as a new and essential parameter for band structure engineering and the subsequent demonstration of quite rudimentary modulation doping effects, to the present state of electron and hole mobilities, which surpass those achieved in the Si/SiO_2 material combination by almost an order of magnitude. This development allows now not only the production of such devices as heterojunction bipolar transistors, modulation-doped field effect transistors, resonant tunneling diode, and photodetectors, but also the performance of experiments that were for a long time an exclusive domain of III–V materials.

2.4. Ge/Oxide Interface

However, a critical step for the device fabrication is to grow a high-quality dielectric, which would be useful for the gate, mask, and device isolation. As a "natural" choice, preserving compatibility with Si technology, one can use a SiO_2 for this purpose, for instance, oxidizing the layer of SiGe. Conventional thermal oxidation of SiGe alloys first of all revealed a selective oxidation for silicon, rejecting Ge from the oxide layer and thus resulting in the pileup of Ge at the oxide-substrate interface [38]. This Ge-rich interfacial layer in metal-oxide semiconductor (MOS) devices may be the reason for high fixed oxide charge and interface state densities, and poor breakdown characteristics. For example, in [39] the wet oxidation of SiGe strained layers by rapid thermal processing revealed a fixed

negative oxide charge density in the range of 10^{11}-10^{12} cm^{-2} and the interface trap density (in the midgap region) of about 10^{12} cm^{-2} eV^{-1}. Furthermore, the density of this fixed interface charge at the SiGe/SiO$_2$ interface is found to increase with the Ge concentration in the commensurately grown SiGe layer.

At the same time, there are indications, that the quality of the SiGe/SiO$_2$ interfaces may be significantly improved. An insulator structure involving the use of an ultrathin (~28Å), pseudomorphic Si interlayer between the SiO$_2$ gate dielectric and the Ge semiconductor substrate was proposed [40] for Ge metal-insulator-semiconductor (MIS) structures. Capacitors formed with such a structure on both n- and p-Ge show midgap interface-state densities of 5·10^{10} cm^{-2} eV^{-1} and no hysteretic. It is important that such a concept may have implications in the development of metal-insulator-semi-conductor systems in a broad class of materials, especially those whose native oxides are unstable and detrimental to the formation of a good electrical interface. Of particular interest, of course, is the SiGe materials system where appreciable success has been demonstrated in applying such a concept to gate formation on the Si/SiGe heterostructures [41].

Although matching the electrical properties of the Si/SiO$_2$ interface is still a real challenge, the truly outstanding properties of Si-based heterostructures and their basic compatibility with Si technologies, is what allows SiGe to play an important role in the field of solid state electronics.

2.5. Si and High-κ Dielectrics

As mentioned in section (2.1) the incredible growth of the Si-based industry over the last several decades is directly related to the extraordinary properties of Si/SiO$_2$ system. But

despite all the excellent attributes of SiO$_2$, the continued downscaling of SiO$_2$ gate dielectrics is approaching its natural limits [42]. The main concerns include unacceptably high leakage current (requirements differ for high performance and low-power applications, but leakage current density is still of concern for both) and dielectric reliability under the required operating voltages. For example, a typical leakage current density for 15-Å-thick SiO$_2$ at 1 V is ~1 A/cm^2. At the same time, the dominant transport mechanism through SiO$_2$ films less than ~30 Å thick is direct tunneling of electrons or holes. In this case, the leakage current increases exponentially with decreasing thickness. Thus, for the SiO$_2$ thickness of 10 Å, the leakage current density approaches 100 A/cm^2 at the same operating voltage.

From a fundamental standpoint, it has been suggested that 7 Å is the physical thickness limit for SiO$_2$, because the SiO$_x$ suboxide region at any Si/SiO$_2$ interface is ~3.5 Å thick (there are two Si/SiO$_2$ interfaces — at the channel and at the gate electrode) [6]. At or below this thickness, the oxide should effectively be an electrical short between the gate electrode and the channel. To avoid this problem the thickness of the gate dielectric should be increased, but to preserve the same capacitance it must be made of a material with a higher dielectric constant κ.

In the simple case, if the thickness of the SiO$_2$ gate is $t_{eq} = 1$ nm, then the thickness of the alternative dielectric employed to achieve equivalent capacitance is given by

$$t_{high-k} = \frac{\kappa_{high-\kappa}}{3.9} t_{eq},$$

which for dielectric constant $\kappa = 16$ results in a physical thickness of ~ 4 nm. For such a thickness the leakage current poses no problem.

Mainly for that reason, a great amount of research effort has been applied recently in an attempt to identified and fabricate a high-κ dielectric that is capable of replacing SiO_2 in CMOS integrated circuits. For several candidate materials, such as Al_2O_3, HfO_2 and ZrO_2, operating devices have been fabricated. Until now, however, no one has demonstrated that all of the desirable electrical properties of Si/SiO_2 system can be reproduced.

The choice of new high-κ gate dielectric materials to replace SiO_2 is stipulated by a number of issues [43], which might be divided into two broad categories: (1) fundamental materials properties that include permittivity, band structure and the associated band offsets for carrier transport, thermodynamic stability in direct contact with Si, and film morphology; and (2) device processing, integration, and performance issues such as interface quality, gate compatibility, process compatibility, and reliability. The issues from both categories must be simultaneously addressed for any successful gate dielectric solution. See the MRS Bulletin **27(3)** (2002) for a concise review of high-κ dielectric materials in integrated devices.

2.5.1. *Permittivity and Bandgap*

Selecting a gate dielectric with a higher permittivity than that of SiO_2 is clearly essential. For many simple oxides, permittivities have been measured on bulk samples and in some cases on thin films. For the more complex materials, the dielectric constants may not be well known. The required permittivity must also be balanced against the barrier height for the tunneling process. For electrons tunneling (leaking) from the Si substrate (channel) to the gate, this barrier is the conduction band offset, ΔE_C. In order to obtain low leakage currents, it is desirable to find a gate dielectric that has a sufficient ΔE_C value to Si and perhaps to other gate metals that may be used at some point. If the experimental value is $\Delta E_C < 1.0$ eV,

it will likely preclude using these oxides in gate dielectric applications, since thermal emission or tunneling of carriers would lead to unacceptably high leakage currents [6,44]. This requirement for $\Delta E_C < 1.0$ eV is nontrivial for some of the alternative gate oxides.

For example, $SrTiO_3$ has a bandgap of 3.3 eV. Its bands must be aligned symmetrically on Si for each band offset to be >1 eV, but in general, the lineup is asymmetric and both calculations [44] and experiments [45] say that this material has $\Delta E_C < 0.1$ eV. On the other hand, an oxide with a wide gap, such as ZrO_2 (5.8 eV) or HfO_2 (6 eV), has less of a problem. Nevertheless, this requirement constrains the choice of gate oxide, as many candidate oxides have quite small electron barriers.
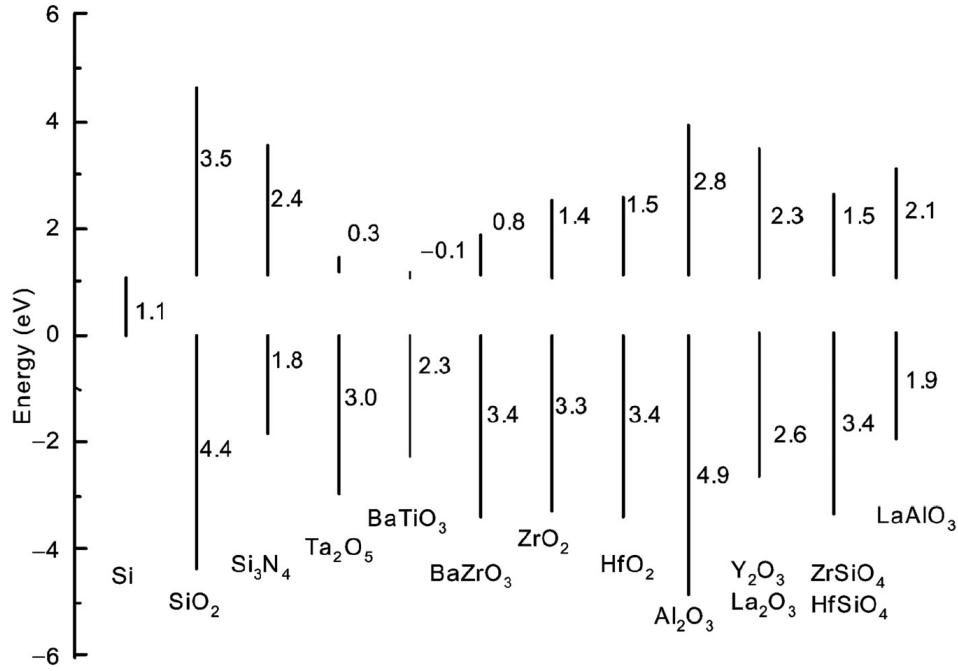
Figure 2. Band offsets for high-κ dielectrics on Si (from [46]).

The band alignments of the gate oxides can be measured by photoemission (which measures the valence to valence band energy) or by internal photoemission (which measures

the Si valence to oxide conduction-band energy). Alternatively, they can be calculated [46]. The calculated offsets are summarized in Figure 2. These values agree well with experimental values found subsequently in [45, 47, 48, 49].

One can see that the oxides of Zr, Hf, La, Y, and Al, and the silicates of Zr and Hf, all have conduction-band offsets of more than 1 eV. In practice, the hole offsets are always bigger than 1 eV, so they cause no problem.
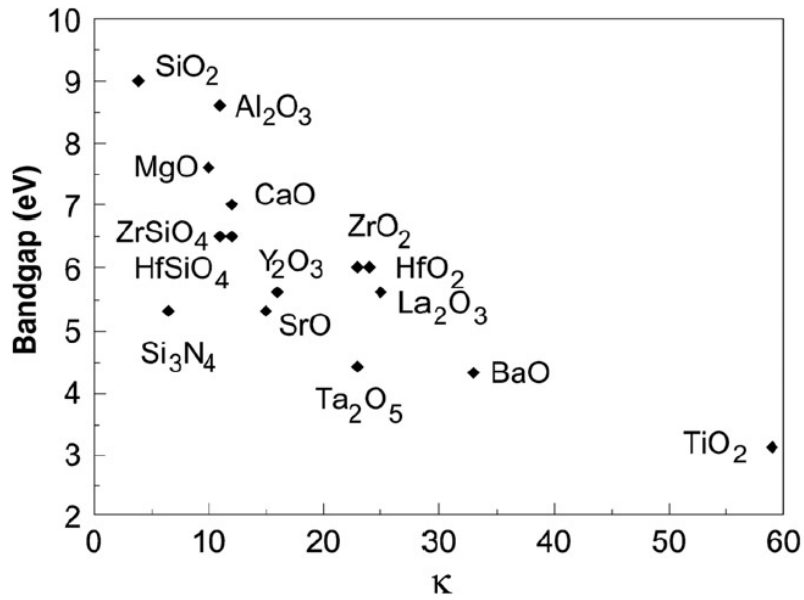
Figure 3. Dielectric constant κ versus band gap for candidate gate oxides (from [46]).

Since many potential gate dielectrics do not have reported ΔE_C values, the closest, most readily attainable indicator of the band offset is the bandgap E_G of the dielectric. A large E_G generally corresponds to a large ΔE_C, but the band structure for some materials also has a large valence-band offset ΔE_V, which constitutes most of the bandgap of the dielectric. For high-κ materials, the dielectric constant and bandgap of a given material generally exhibit an inverse relationship, as it is demonstrated in Figure 3.

There are a number of unary oxides with $\kappa > 3.9$ that exhibit E_G values above 5 eV. Therefore, assuming reasonable symmetry of the band edges, many could have useful band offsets for device applications. Because of this relationship between bandgap and permittivity, a common assumption is that a dielectric with $\kappa > 25$ is required to replace SiO_2; this is actually not necessary. The more relevant consideration is whether the desired device performance can be obtained without producing unacceptable off-state (leakage) currents or reliability characteristics. For example, if a single dielectric layer could be used, then even a material with $\kappa > 12 \div 20$ could result in a physical dielectric thickness of 35–50 Å, required for 0.1-μm CMOS technology. Because of the general requirement of bandgap alignment, many promising materials with high dielectric constant can be ruled out as viable gate dielectric candidates.

2.5.2. Thermodynamic Stability on Si

Another criterion that significantly reduces available materials is thermodynamic stability on Si. For example, such materials as Ta_2O_5, TiO_2, and $(Ba, Sr)TiO_3$ are thermodynamically unstable in direct contact with silicon at all temperatures between the room temperature and the ~1000 °C needed for MOSFET fabrication, as demonstrated by the reaction between silicon and Ta_2O_5 [50]:

$$\frac{12}{13}Si + Ta_2O_5 \xrightarrow{\Delta G_{1000K}^0 = -413.332\ kJ/mol} 2TaSi_2 + \frac{5}{2}SiO_2,$$
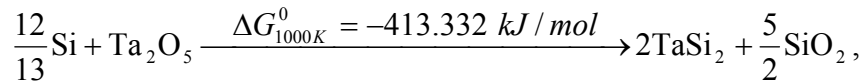
where ΔG_{1000K}^0 is the free-energy change of the system when the reaction between reactants and products, all taken to be in their standard state, proceeds in the direction indicated at a temperature of 1000 K.

Similar reactions exist between silicon and TiO_2 and $(Ba, Sr)TiO_3$ [51]. Furthermore, the reaction products all involve unwanted low-κ dielectrics (i.e., SiO_2, $SrSiO_3$, and $BaSiO_3$). Such low-κ reaction layers in series with the desired high-κ dielectrics rapidly nullify the benefits of the high-κ dielectrics when a capacitance corresponding to the SiO_2 physical thickness of ~10 Å is needed. Experimental observations of interfacial reactions [52, 53] are consistent with these thermodynamics expectations.

To comprehensively assess the thermodynamic stability of potential high-κ dielectrics in contact with silicon, a thermodynamic approach was used in [54]. The binary oxides were found to have a significantly higher dielectric constant κ than those few non-conducting binary nitrides that are stable or potentially stable in contact with silicon. This thermodynamic approach was extended to multi-component oxides comprised of candidate binary oxides. The result is a relatively small number of silicon-compatible gate-dielectric materials with κ substantially greater than that of SiO_2 and an optical bandgap ≥5 eV. These results are summarized in Figure 4, which is complimentary to Figure 2.

In Figure 4 materials where the full dielectric tensor is known are denoted with solid circles (●). The variation of κ with orientation is indicated by the dashed line between two solid circles, one denoting the orientation where κ is minimal and the second where κ is maximal. Open circles (o) indicate materials where the complete dielectric-constant tensor is not known. The hash-marks indicate the boundary region: a bandgap at least 4 eV and preferably exceeding 5 eV.

Silicon-compatibility, high κ, high optical bandgap and band alignment are just some of many requirements that a successful alternative gate dielectric must posses. But they mark a

starting point for additional considerations, such as density of electrically active defects at the Si/dielectric interface or interface quality.
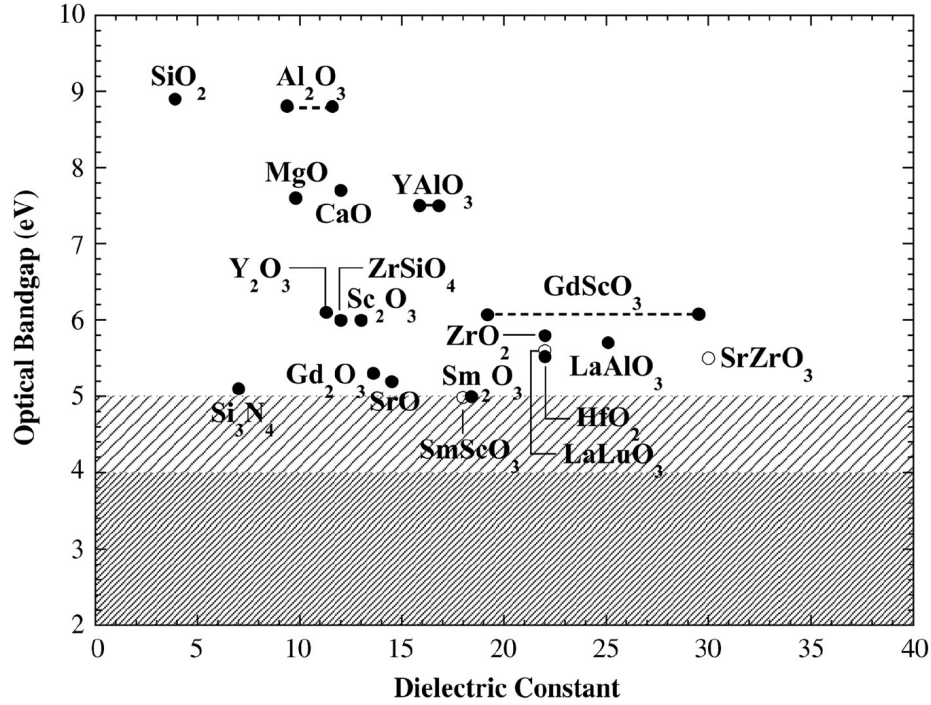
Figure 4. Dielectric constant κ versus optical bandgap E_G of alternative gate dielectrics that are likely to be stable in contact with silicon (from [54]).

There are indications [55] that thermodynamically stable systems, such as ZrO_2 and HfO_2 and their pseudo-binary variants may allow for control of the Si/dielectric interface quality and provide a solution in the search for high-κ gate dielectrics. For example, it has been shown [56] that an extremely thin, ~3.5-Å SiO_x, $1 < x < 2$, layer can be made to form at the Si/Zr- silicate interface. This very thin SiO_x film can be beneficial for device properties as an underlayer for a high-κ film; however the SiO_x has a very low dielectric constant and are, therefore, undesirable in the far future. Also, it is very difficult to achieve and control an interfacial layer this thin while depositing most other materials. The κ values of silicates are

substantially lower than those of pure HfO_2 and ZrO_2, but this tradeoff for interfacial control may be acceptable as long as the resulting leakage currents are low enough. At the same time it is shown in [57] that considerable Zr interdiffusion into Si substrates is observed under aggressive annealing (up to 1100 °C), which is not the case for the Hf [58]. Also, recent results on pure HfO_2 are very encouraging and show good electrical performance [59,60]. Thus, it is HfO_2 that will be discussed in the next section.

2.5.3. Si/HfO₂ Interface

As a candidate for alternative high-κ dielectric, HfO_2 attracts particular attention since it combines the desirable high dielectric constant of about 25 with thermal stability [55]. At the same time, to suppress electron tunneling from Si to the gate, the oxide must constitute a sufficient energy barrier. As follows from Figure 2, the theoretically estimated value for the conduction band offset ΔE_C at the Si/HfO₂ interface is about 1.5 eV [46].

However, in [61] the electron energy band alignment at the Si/HfO₂ interfaces with different inter-layers (Si_3N_4, SiON, and SiO_2) was directly determined by internal photoemission of electrons and holes from (100) Si into HfO_2. It is shown that, irrespective of the interlayer type, the energy barrier for the Si valence electrons equals to 3.1 ± 0.1 eV, yielding the conduction band offset of 2.0 ± 0.1 eV. Photoemission of holes is reported to be effectively suppressed by SiON and SiO_2 inter-layers, and yet it is observed to occur across the Si_3N_4 interlayer with a barrier of 3.6 ± 0.1 eV, which corresponds to a Si/HfO₂ valence band offset of 2.5 ± 0.1 eV. The HfO_2 band gap width of 5.6 eV, thus derived from the band offsets, coincides with the bulk value obtained from the oxide photoconductivity spectra.

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In contrast to Zr, hafnium interdiffusion into silicon is very limited. In [58] the interdiffusion of Hf and Si from $(HfO2)_{1-x}(SiO2)_x$ thin films deposited on Si (100) was studied using X-ray photoelectron spectroscopy, time-of-flight secondary ion mass spectrometry, high resolution transmission electron microscopy, and Rutherford backscattering spectrometry in combination with chemical etching. It is shown that after extreme rapid and conventional furnace thermal annealing treatments, Hf incorporation into Si is limited to less than 0.5–1 nm from the interface.

In general, physical and electrical properties of HfO_2 films on Si substrates may differ depending on the way they are obtained. As reported in [62], the oxidation of Hf metal films deposited directly on the Si substrate results in the electrically stable amorphous $HfSi_xO_y$ interfacial layer and the high-k HfO_2 film simultaneously. It is speculated that Hf silicate film acts as a barrier to the oxidation of the Si substrate. Therefore, the subsequent heat treatment in either O_2 or N_2 only increases the thickness of HfO_2 film via the diffusion of Si and O atoms, resulting in thickness reduction of the amorphous $HfSi_xO_y$ film. This phenomenon causes the increase of the effective dielectric constant, while maintaining the excellent interfacial properties: the equivalent oxide thickness and the leakage current density of the Pd–HfO_2/$HfSi_xO_y$–Si capacitor were 1.4 nm and 5×10^{-3} A/cm^2 at 2 V after compensating the flatband voltage of 1 V, respectively.

It is also reported by Hoshino $et\ al.$ [59] that, if the HfO_2/Si(001) interfaces are formed by reactive DC sputter deposition of Hf followed by HfO_2, then Hf buffer layer prevents the growth of SiO_2 at the interface, and the presence of the Hf layer leads to the formation of Si-rich silicate-like interlayers. If no buffer layer is used, the formation of SiO_2 is reported. It is also suggested that the Hf buffer layer suppresses the O diffusion toward the interface and

thus the thicker the buffer layer, the thinner the Hf-silicate interlayer. As a result the deposition condition of HfO_2(1.3 nm)/Hf(1.3 nm) has achieved the highest permittivity of 28 for HfO_2(3.6 nm) and 8 for the silicate layer (1.7 nm).

Changes in the composition of the atomic layer deposited, uncapped hafnium dioxide films, as a function of anneal temperature were evaluated by Lysaght *et al.* [60] with several analytical techniques including: X-ray reflectivity, HRTEM, and medium energy ion scattering. It is shown that such measurements of the Si/high-κ interface layer are inconclusive and may be misinterpreted to suggest the presence of an $Hf_xSi_{1-x}O_2$ ($x\sim0.5$) transition layer. It is also demonstrated that high-temperature annealing of uncapped films may result in the formation of voids which propagate through the dielectric layer into the silicon substrate.

The defects at the HfO_2/(111)Si interface obtained by atomic layer chemical vapor deposition were studied in [63] by electron spin resonance (ESR) method. Several signals are reported, dominated by one due to a silicon dangling bond at the Si/dielectric interface. This center is speculated to be similar to, but not identical to, Si/SiO_2 interface silicon dangling bonds. Comparison between ESR and capacitance versus voltage measurements suggests that these dangling bond centers play an important role in Si/ HfO_2 interface traps, whose density is in the range of $\sim10^{11}$–10^{12}/cm^2 eV.

2.5.4. *Si/Al$_2$O$_3$ Interface*

Al_2O_3 has dielectric constant $\kappa \approx 11$. Although this dielectric constant is not that high as in the case of HfO_2, the optical bandgap of Al_2O_3, is almost 9 eV (see Figure 4); the calculated conduction band offset is 2.8 eV and the hole offset is almost 5 eV (Figure 2).

This fits Al_2O_3 well into the requirements of band alignment with Si. As a result, Al_2O_3 is another prime candidate for an alternative gate dielectric and it is currently under intensive investigation [3, 55].

In contrast to HfO_2 which usually shows microcrystalline structure, the as-deposited Al_2O_3 layer is amorphous. That automatically eliminates the problem of grain boundaries that may serve as the paths for high leakage and diffusion.

From the thermodynamic point of view, the dielectric Al_2O_3 appears to be stable with respect to reaction with the poly-Si gates throughout typical CMOS processing (see [55] and ref. 34–36 in it). However, both boron and phosphorous dopant diffusion have been observed with Al_2O_3 gate dielectric, which causes significant, undesired shifts of V_{FB} and V_T values.

In [64] a combination of two complementary depth profiling techniques with sub-nm depth resolution, nuclear resonance profiling and medium energy ion scattering, and cross-sectional high-resolution transmission electron microscopy were used to study compositional and microstructural aspects of ultrathin (sub-10 nm) Al_2O_3 films on silicon. According to Gusev *et al.*, all three techniques yield similar results that can be summarized as follows. Ultrathin Al_2O_3 films deposited on Si (or on the bottom oxide or oxynitride layer) by the atomic layer chemical vapor deposition (ALCVD) technique show: (i) good uniformity; (ii) Al_2O_3 stoichiometry; and (iii) abrupt interfaces. However the spatial resolution obtained in the above experiments was not specified and the statement of abruptness is quite questionable.

The electrical properties and the carrier transport mechanisms of Al_2O_3 gate dielectric thin films deposited on Si by reactive DC magnetron sputtering were studied in [65]. The results indicate that higher temperature annealing in oxygen ambient is helpful to treat

interfacial traps at the Si/Al_2O_3 interface and to improve the electrical properties of Al_2O_3 gate dielectric films. These results are confirmed by Shao *et. al.* [66] in the study of ultrathin Al_2O_3 films deposited on n-Si substrates by low-pressure MOCVD. It was found that post-annealing was necessary for ultrathin Al_2O_3 films to obtain good electrical properties and that post-annealing in an O atmosphere could effectively eliminate the carbon contamination of Al_2O_3 films.

The quality of Al_2O_3 film on Si substrate may be strongly influenced by the pre-deposition treatment of the Si surface (which eventually becomes a part of the interface). The effects of various interface preparations on ALCVD deposited Al_2O_3 dielectrics properties were investigated in [67] by X-ray photoelectron spectroscopy (XPS), attenuated total reflection Fourier transform infrared spectroscopy (ATR-FTIR), medium energy ion scattering (MEIS) and transmission electron microscopy (TEM). On H-terminated Si the initial growth rate of Al_2O_3 is very low. The slow initial growth rate arises from the fact that hydrogen effectively passivates the Si surface and thus leads to inhomogeneous island nucleation. For OH-terminated Si, the initial Al_2O_3 growth is much faster than the H-terminated case, with little inhibition. For the N-terminated Si, the initial growth rate lies between that displayed on the H-terminated and OH-terminated Si surfaces.

Although post-annealing in an O atmosphere could improve electrical characteristics (reducing charge traps and eliminating contamination), the exposition of already deposited high-κ film to air may cause the growth of interfacial SiO_2. For example, following ten cycles of Al_2O_3 deposited on a H-terminated Si surface, SiO_2 was found to grow dramatically upon air exposure [67], which might be due to rapid oxygen transport through the ultrathin dielectric, or incomplete coverage of the underlying Si by an inhomogeneous dielectric

overlayer. This interfacial SiO_2 layer is undesirable since, having a comparably low dielectric constant, it effectively reduces the equivalent oxide thickness (EOT) and may increase the leakage current. Therefore, caution must be taken to prevent prolonged exposure of such high-k materials to an oxidizing environment, especially if the sample is at elevated temperatures.

To summarize, the above examples concerning HfO_2 and Al_2O_3 demonstrate that an alternate gate dielectric material that *simultaneously* satisfies all of the considerations has yet to be determined, but several promising candidates have been identified. Nevertheless, matching the outstanding electrical properties of SiO_2 clearly presents a significant challenge.

3. METHODS AND TOOLS

3.1. Aberration Corrected TEM/STEM

Since the invention by Knoll and Ruska [68] in 1932, the transmission electron microscope (TEM) has undergone many improvements and over the past three decades it has become the instrument of choice whenever questions of microstructural characterization arise in materials science. For example, the electrical or mechanical behavior of interfaces for many systems and their dependence on defects could be explained by this tool.

Images of atomic resolution have been acquired by using conventional TEM since the late 1970s. By using a field emission electron source (FEG), Crewe *et al.* [69] succeeded in detecting individual atoms and atomic clusters on a scanning transmission electron microscope (STEM) in the early 1970s. However, the production of magnetic lenses for electron microscopes has not progressed far enough and magnetic lenses still suffer significant imperfection. One of the major defects of magnetic lens which seriously limits the resolution of contemporary TEM or STEM systems is spherical aberration.
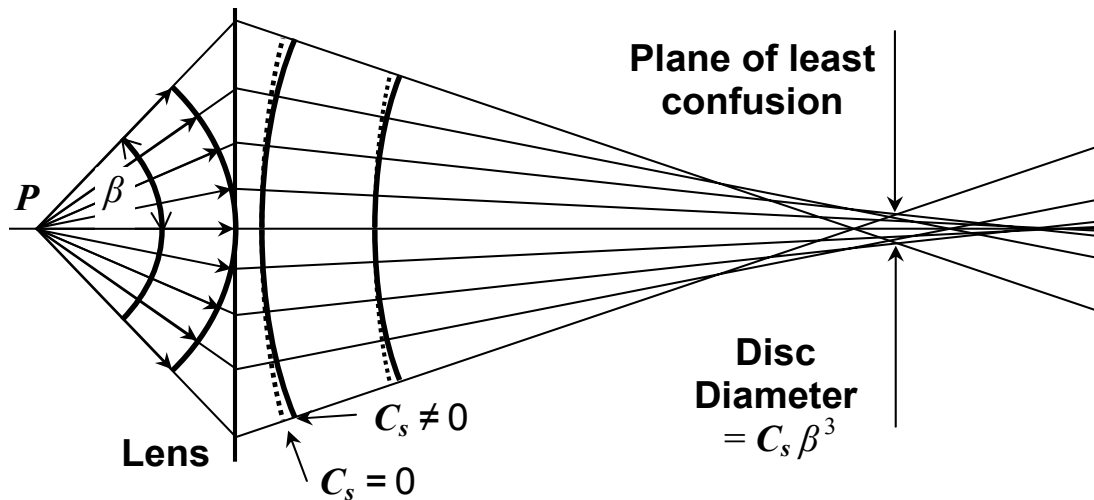
Figure 5. Spherical aberration in the lens causes wavefronts from a point object P to be spherically distorted (after [70]).

The defect is caused by the lens field acting inhomogeneously on the off-axis rays. The schematic representation of the spherical aberration effects is shown in Figure 5 [70]. The further off axis the electron is, the more strongly it is bent back toward the axis. As a result a point object **P** is imaged as a disk of a finite size. This disk has a minimum radius in the plane of least confusion. The minimum radius is defined by the spherical aberration coefficient C_s. If other factors which might influence the resolution are corrected, then the approximate expression for the resolution limit r_{min} due spherical aberration is given by [70]:

$$r_{min} = 0.91(Cs\lambda^3)^{1/4},$$

where λ is the electron wavelength. Typically, the value for $r_{min} \sim 0.25 - 0.3$ nm, but the high resolution instruments have $r_{min} \sim 0.15$ nm.

The spherical aberration problem was well understood from the very start. In 1947, Scherzer [71] demonstrated that a typical magnetic round lens would always have a positive spherical aberration coefficient and there was thought to be little hope of canceling out aberrations using round lenses. At the same time, Scherzer pointed out three possible ways to correct the limiting aberrations: (1) use of non-rotationally symmetric fields (multipoles), (2) use of lenses with charge on axis (including mirrors), and (3) use of time varying fields. Unfortunately, the realization of this suggestion proved to be difficult although it was shown by Koops et al. [72] and Hely [73] that a multipole may function in principle. However, the technical problems (first of all the adjustment of all multipole lenses in the corrector) were too complex to be tackled by the means available at the time, and even as recently as 7 years ago [74], the imminent advent of practical aberration correctors for electron lenses was thought unlikely.

Nevertheless, three different types of aberration correctors have now improved the resolution of electron microscopes into which they have been incorporated [75, 76, 77]. The one that was developed specifically for a dedicated STEM VG HB 501 in Oak Ridge national laboratory [77], is of particular interest because it was used for the present study. Initially it was a proof-of-principal instrument, which indeed improved the resolution of VG501 operating at 100 keV, but did not cross the threshold of attaining better resolution than any other microscope operating at the same primary voltage. Just two years ago a second-generation corrector was designed [78], which has crossed this important threshold.
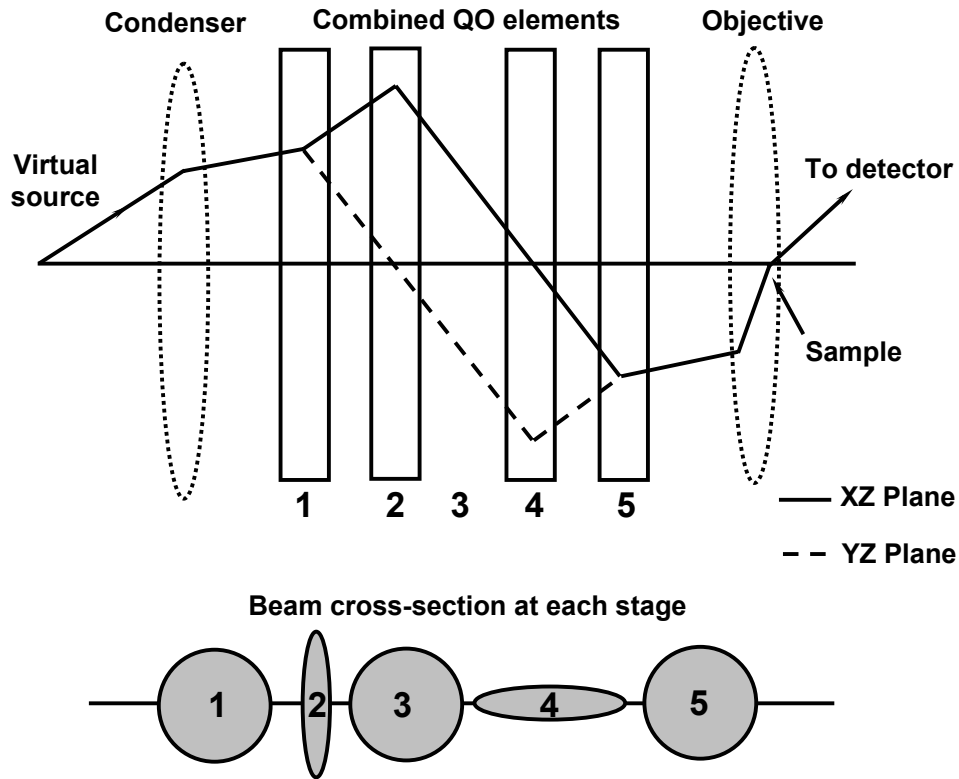
Figure 6. Principle scheme of the quadrupole-octupole correction of spherical aberration in STEM.

The corrector itself is of the quadrupole-octupole type. It uses 4 quadrupoles and 3 octupoles, without combining them into compound elements. The idea behind that corrector

is shown schematically in Figure 6. It is impossible to compensate aberrations while preserving the round symmetry of the electron beam cross-section, but one can stretch the beam in one direction with a quadrupole and then correct aberrations in this direction with an octupole. Then the round shape of the beam cross-section can be restored and the same procedure repeated for another direction.

For the STEM system, the major characteristic determining the resolution limit is the smallest achievable size of the electron beam (probe) and electron current density in it (see more in the next session). By running an aberration corrector in the VG HB 501 it is possible to focus the electron probe below 1 Å [78], and that automatically increases the current density as it is shown in Figure 7.

(a) **(b)**

FWHM
= 0.7 Å

FWHM
= 1.9 Å
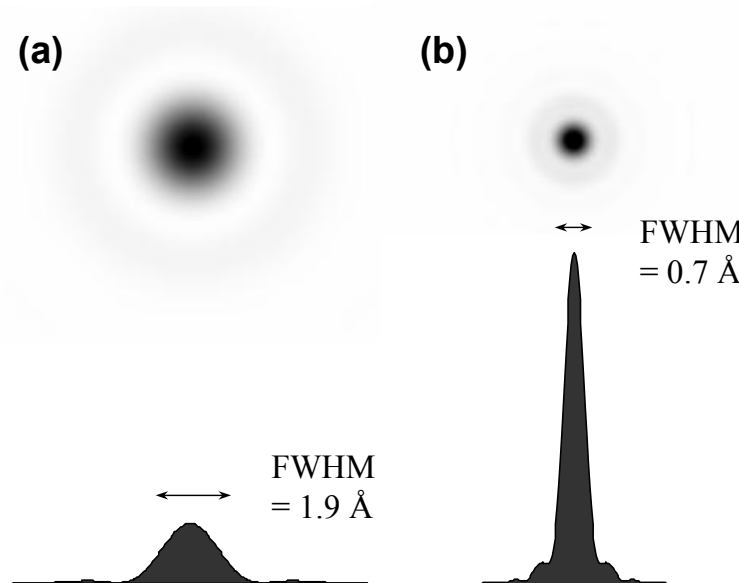
Figure 7. The intensity profile of the electron beam of (a) non-corrected and (b) C_s corrected VG HB501 STEM.

In order to reach 1 Å probe size with aberration corrected STEM, it is necessary to control all aberrations (up to fifth order) with a high degree of precision, i.e. self-consistently

adjust all quadrupoles and octupoles in the corrector. For that purpose an autotuning Ronchigrams based method was developed. This method uses the fact that the local magnification in a Ronchigram [see Figure 8 (a) and (b)] is related to the second derivative of the aberration function. Thus, one can determine magnification by recording a Ronchigram, then move the probe on the sample by a calibrated amount in a particular direction, record a second Ronchigram, find out how sample features in a different parts of the Ronchigram have moved from one Ronchigram to the other by cross-correlation, and repeat the procedure while moving the probe in a perpendicular direction.
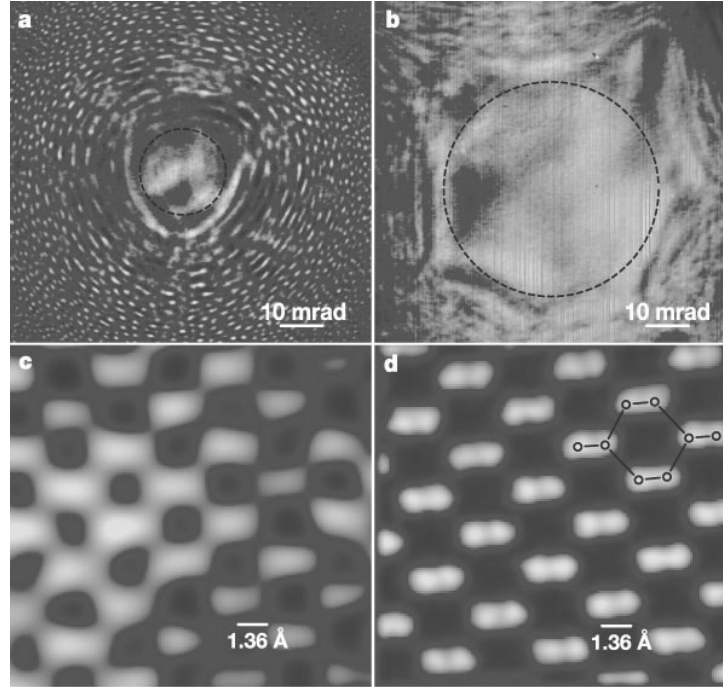
Figure 8. The results of imaging of a $Ge_{0.3}Si_{0.7}$ alloy without aberration correction (a) and (c), and with aberration correction (b) and (d) (from [79]).

Typical results which can be obtained by the use of aberration corrected STEM [79] are demonstrated in Figure 8. The shadow maps in (a) and (b) (Ronchigrams) show regions of minimum contrast at the centre defining an area of constant electron phase, appropriate for

use in forming a small probe. The larger available area using aberration correction produces the smaller probe, consistent with the Heisenberg uncertainty relation. Figure 8 (c) and (b) shows the resulting crystal image. The dramatic contrast between the images is obvious.

This successful aberration correction is linked to recent technical advances: (1) computation of electron optical parameters is now possible for non-rotationally symmetric systems, allowing practical designs to be simulated with high accuracy; (2) mechanical fabrication tolerances have advanced materially in the past 15 years; (3) high stability electronic components have become available in the past 10 years, allowing the packaging of many very high stability, computer-controlled power supplies in a small space; and (4) high-speed small computers are now available for real-time processing of the shadow map Ronchigram data to obtain aberration parameters. It is believed now that aberration correction technology combined with the inherent power of the STEM instrument opens the way for routine imaging and analyzing of materials at sub-Å resolution and thus the characterization of defects and interfaces between materials.

3.2. Z-contrast Imaging

The scanning transmission electron microscope differs significantly from its conventional counterpart since in order to form an image of a specimen it is not necessary to refocus scattered electrons. The image is formed simply by detecting the electron flux scattered in some direction as a function of probe position. Therefore, it becomes a simple matter to include electrons scattered through angles considerably larger than the scattering angles employed in a conventional TEM, increasing both the efficiency of the imaging process as well as the atomic number or Z sensitivity. It was this realization that motivated the original

development of STEM by Crewe and his co-workers [69]. Specifically, an annular detector was employed having an inner angle just greater than the optimum objective aperture angle and a large outer angle. As a result, spectacular images were obtained of a single heavy atoms supported on thin carbon film.

The key to high resolution STEM is the formation of an electron probe of atomic dimensions. Figure 9 shows a schematic of the experimental microscope conditions, the relationship between the probe, the specimen and the detectors (such as the EELS detector which is to be discussed in the next section), as well as some typical experimental results.
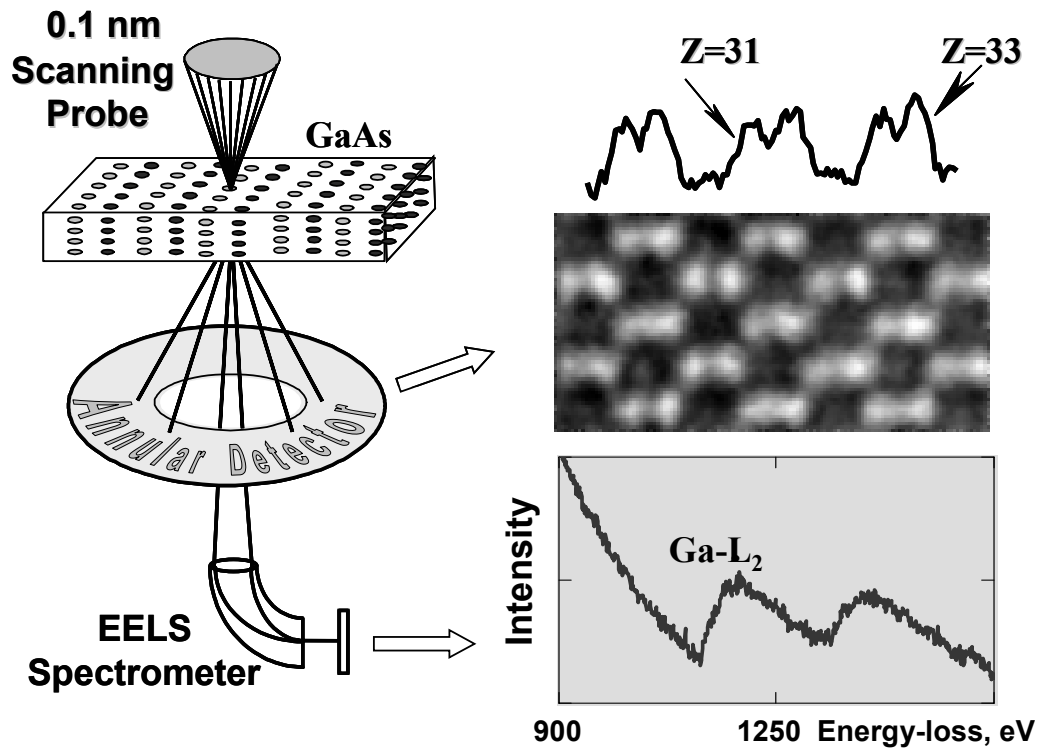
Figure 9. Schematics of atomic resolution Z-contrast imaging and EELS.

Essentially, for either dedicated STEM [80] or one of the more modern TEM/STEM instruments [81], the electron optics of the microscope above the specimen is aligned in such

a way as to make the probe as small as possible on the surface of the specimen. For a given acceleration voltage, the size of the probe is primarily dependent on the spherical aberration coefficient of the probe forming lenses.

The tuning and optimizing of the electron probe can be achieved most readily with the electron Ronchigram or shadow image [see Figure 8 (a) and (b)] because this image is very sensitive to electron optics aberrations and defocus. For example, when the excitation of each electron optics component (i.e. lens) is slightly changed, very small misalignments become apparent by translations in the pattern that depart from circular symmetry.

Z-contrast images [80, 82] are formed by collecting the high-angle scattering on an annular detector (Figure 9). A crystalline sample is oriented to a low-order zone axis (to "look" along columns of atoms while maximizing the "empty" space between the columns) and scanned by the focused electron probe of STEM. Detecting the scattered intensity at high-angles and integrating over a large angular range effectively averages coherence effects between neighboring atomic columns in the specimen. Thermal vibrations reduce the coherence between atoms in the same column to residual second order correlations between near neighbors [83]. This allows each atom to be considered as an independent scatterer. Scattering factors may be replaced by cross-sections, and these approach a Z^2 dependence on atomic number.

The interpretation of Z-contrast images can be aided by the use of the object function concept [84] which is illustrated in Figure 10. The crystalline specimen consists of an array of atomic columns (a) for which the potential (or cross-section) for high-angle scattering can be represented by an object function (b). For very thin specimens, where there is no dynamical diffraction, the experimental image (c) (the detected intensity versus probe

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position) can be interpreted as a simple convolution of the probe intensity profile and the object function [80].
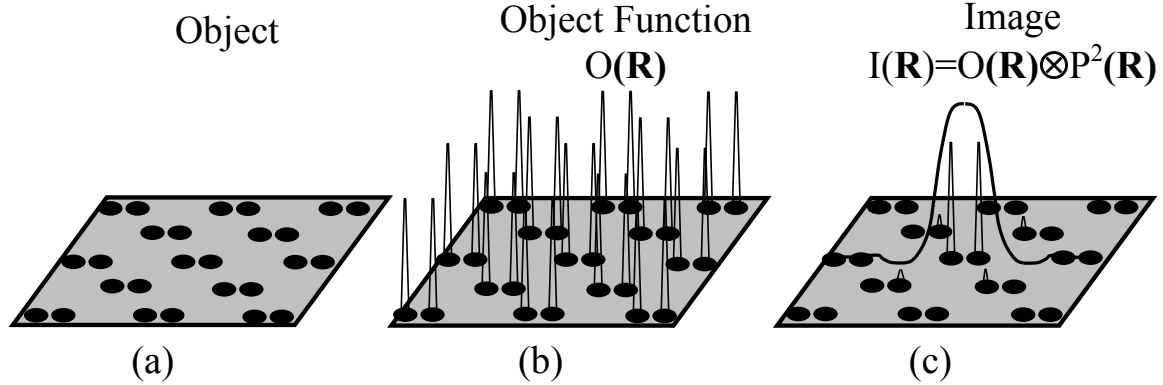
Figure 10. Schematic representation of the experimental probe and the object function convolution [from 84].

The small width of the object function (~0.02 nm) means that the spatial resolution is limited only by the probe size of the microscope (the optimization of which is achieved using the Ronchigram, as mentioned above). For a crystalline material in a zone-axis orientation, where the atomic spacing is greater than the probe size, the atomic columns are illuminated sequentially as the probe is scanned over the specimen. A directly interpretable, atomic resolution compositional map is thus generated (see, for example, Figure 16 in "Results and Discussions" section), in which the intensity depends on the average atomic number Z of the atoms in the columns.

This result also holds true for thicker specimens. It has been noted that for specimens in zone axis orientations, the STEM probe forms narrow spikes around the atomic columns as it propagates [85]. This effect is caused by the coherent nature and large angular spread of the STEM probe, which leads to the tightly bound *s*-type Bloch states adding constructively and the less localized states interfering destructively [80]. This effect is enhanced for scattering

processes such as high-angle thermal diffuse scattering that are localized at the atomic cores, causing a great reduction in beam broadening. With only one dominant Bloch state, dynamical diffraction effects are largely removed and manifest themselves only as a columnar channeling effect, thus maintaining the thin specimen description of the image as a simple convolution of the probe intensity profile and an object function, strongly peaked at the atom sites. The phase problem associated with the interpretation of conventional high-resolution TEM images is therefore eliminated.

In thin specimens, the dominant contribution to the intensity of a column is always its composition, although, due to the higher absorption of the heavy strings, the contrast does decrease with increasing specimen thickness and in very thick crystals there is no longer a high resolution image. Besides the atomic resolution, a great sensitivity to atomic composition is a major advantage of Z-contrast imaging method. As demonstrated in Figure 9 by analysis of Z-contrast image intensity one can differentiate between elements, for example, with atomic numbers Z as close as 31 (Ga) and 33 (As).

In some cases (e.g. a high Z number of species), the Z-contrast method even allows the imaging of a single impurity atom in a crystalline matrix as shown in Figure 11. The heavy Bi atom embedded in a particular atomic column of Si significantly increases the scattering cross-section, resulting in higher local intensity of the Z-contrast image, and, thus, being detected. Moreover, knowing the thickness of Si matrix, by appropriate calibration of Z-contrast intensity one can, in principle, find the depth of those Bi atoms within the sample. In other words, one can determine the atomically precise 3D-distribution of Bi atoms. This might be very handy, for example, for impurity diffusion analysis.

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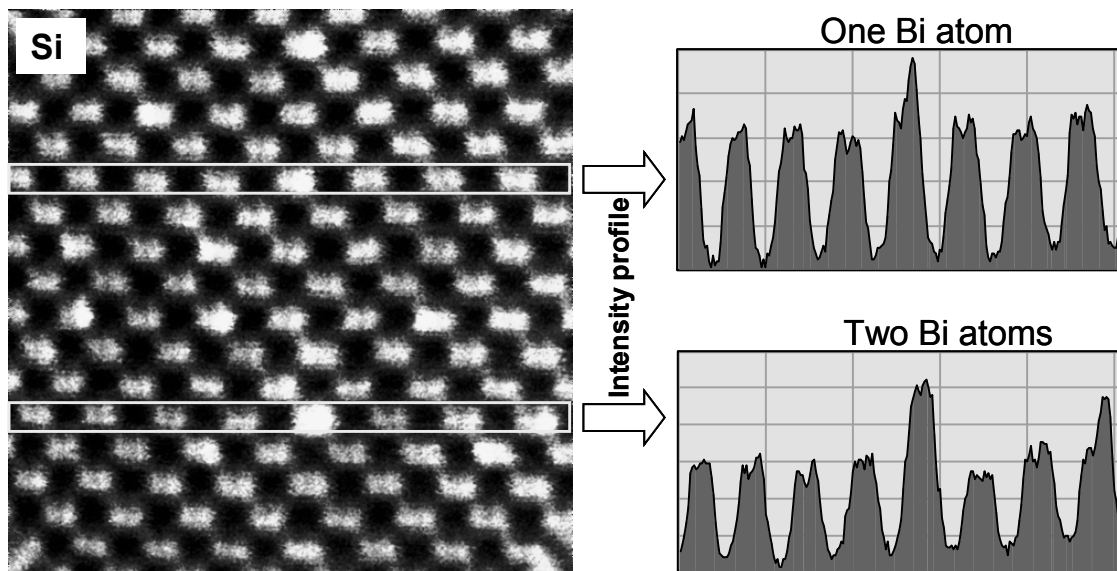
Figure 11. Imaging of single Bi atoms in Si(110) (by A. Lupini, VG HB501UX with Nion Aberration Corrector, 100 kV).

The structure of materials next to defects and interfaces can become extremely complicated, causing difficulties in determining the precise 3D composition. However, provided an atomic column is continuous through the crystal, reconstructions will only result in a change of column intensity and not a contrast reversal [86]. Therefore the atomic structure in the region of defects and interfaces can, in large part, still be determined from the image.

Presented in this study the atomic resolution images of different interfaces are obtained by the use of the VG HB603 UX dedicated STEM, operating at 300 kV and having an optimum probe diameter less than 0.13 nm (even without aberration corrector).

3.3. Electron Energy Loss Spectroscopy

As can be seen from Figure 9, the arrangement of the annular detector used for *Z*-contrast imaging is such that electrons scattered to low-angles can be used for simultaneous electron

energy loss spectroscopy. This means that the *Z*-contrast imaging can be used to position the electron probe over a particular structural feature for the acquisition of a spectrum [87, 88].

Electron energy-loss spectroscopy is the analysis of the energy distribution of electrons that have interacted inelastically with the specimen. These inelastic collisions can provide information about the electronic structure of the specimen atoms, their bonding and nearest-neighbor distributions.
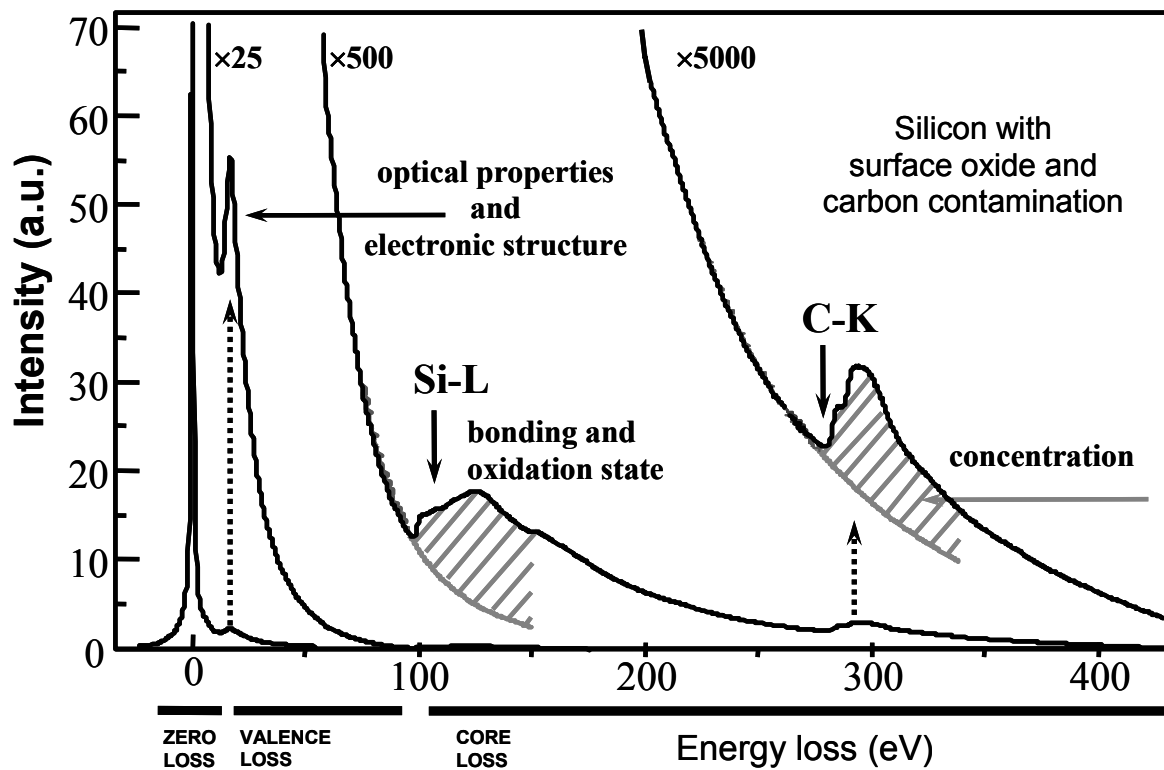
Figure 12. EELS of Si, revealing different information at different energy scales. (Courtesy of Gerd Duscher)

To analyze the energy-loss spectra one usually can deal with three principle regions as schematically shown in Figure 12:

• The zero-loss peak, which consists primarily of elastic forward-scattered electrons, i.e. the electrons that have completely retained the beam energy. Since the spectrometer has a

finite energy resolution, the zero-loss peak also contains electrons that suffer minor (irresolvable) energy losses, mainly due to phonon excitation. So, the zero-loss peak defines the energy resolution and is essential in calibration of the spectrum. Zero-loss also constitutes the background for other regions. It is usually removed for the purpose of analysis ease.

• The low-loss (or valence loss) region up to an energy loss of ~70 eV contains electrons which interact with the weakly bound outer-shell electrons of the atoms in the specimen, i.e. electrons that set up plasmon oscillations or generate inter- or intra-band transitions. Plasmons are longitudinal wave-like oscillations of weakly bound electrons. Plasmon losses dominate in materials with free-electron structures, such as Li, Na, Ma, and Al, but occur to a greater or lesser extent in all materials. The weakly bound outer-shell electrons, involved in the inter- or intra-band transitions, control the reaction of an atom to an external field, and, thus, the low-loss region may characterize the dielectric and optical properties of material.

• Electrons in the high-loss or core loss region interact with the more tightly bound inner-shell or core electrons. When the electron beam transfers a sufficient energy to K, L, M, N, or O shell electrons to move it outside the attractive field of the nucleus, as illustrated in Figure 13, the atom is said to be excited or ionized. The ionization process is characteristic of the atom involved and so the signal is a direct source of elemental information. The energy-loss spectrum associated with ionization is called the ionization edge.

The ionization starts with the transition of an inner-shell electron into the available energy level in the conduction band (see Figure 13). The minimum energy for this transition constitutes the ionization threshold or ionization edge onset in the energy-loss spectrum. The probability for such a transition determines the shape of the ionization edge and it closely

related to the density-of-states (DOS) [89] in the conduction band. DOS in its turn depends on the atomic species and the bonding to the neighboring atoms, and, thus, bonding information can be retrieved from the core loss EELS. Moreover, the integration of an EELS spectrum under the ionization edge and appropriate calibration may provide quantitative information about specific elements in the specimen (see Figure 12) [90].
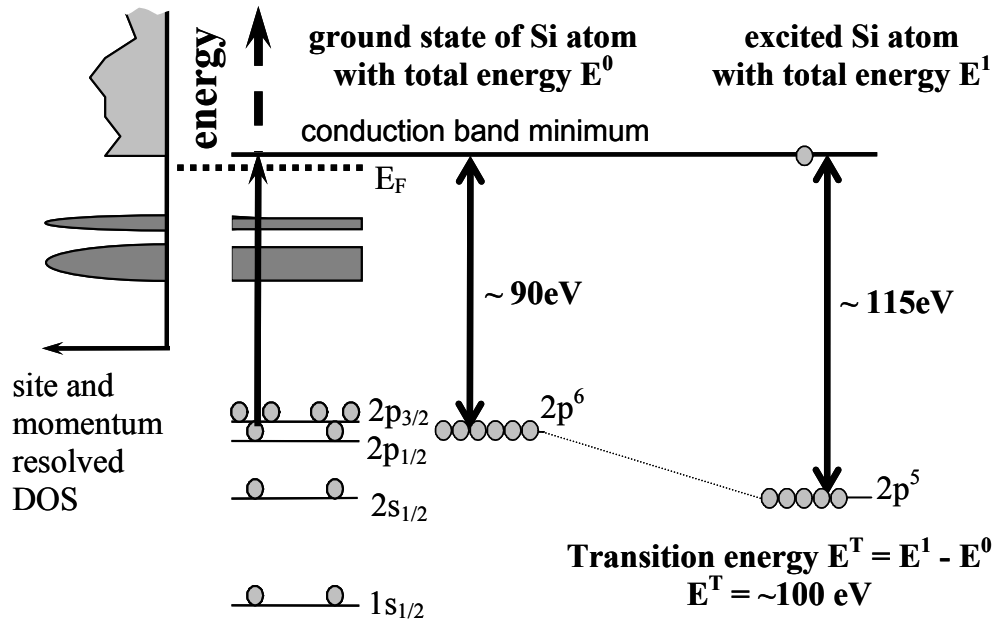
Figure 13. The origin of Si-L$_{2,3}$ ionization edge in EELS.

To be able to correlate the spectrum precisely with the structural feature seen in the image, it is essential that the spectrum have the same atomic resolution as the *Z*-contrast image. The ultimate resolution in electron energy-loss spectroscopy performed in a transmission electron microscope is defined by two factors: the physical limit is set by the spatial extent of the interaction between the excited atom and the fast electron (impact parameter), while the diameter of the electron beam (probe) adds an instrumental limitation. Quantum mechanical treatments of the impact parameter give localization of the scattering

event for higher losses below 0.1 nm (for 100 keV incident energy). This is much broader than the width of the object function for Z-contrast imaging, but for most practical purposes the dominating factor controlling spatial resolution in EELS remains therefore the probe diameter. For crystalline materials in zone-axis orientations, coherent effects are averaged and the description of the spectrum in terms of a convolution of the probe with an object function is valid (Figure 10).

An important aspect of this experimental approach is that the probe channeling discussed for *Z*-contrast imaging will also preserve the spatial resolution of the spectrum, thereby allowing atomic resolution analysis of the electronic structure to be achieved. The specimen drift is also a problem, but for the acquisition times of less than 5 s used in all practical applications discussed here, the 1Å/minute drift of the microscope does not induce a significant broadening effect.

The instrument used for all EELS results presented in this study is located in Oak Ridge National Laboratory the VG HB501 UX dedicated STEM, operating at 100 kV. It provides 0.3 eV energy resolution for EELS and an optimum probe diameter of less the 0.13 nm due to the aberration corrector installed [78]. The spectrometer/detection system follows the same basic principles as all currently available parallel detection systems for EELS in TEM/STEM [91]. However, the original magnetic sector prism serial spectrometer, supplied by VG, is modified by McMullan [92]. Here, two quadrupoles are added at the exit slit of the spectrometer to magnify and project the energy dispersive plane onto a YAG scintillator. The image so formed on the scintillator is optically coupled to an efficient multi-phase pinned CCD camera. The aim in using this CCD camera is to provide high efficiency for the low signal levels that are expected from the use of a small probe (without aberration corrector)

and the study of energy-losses above 100 eV. In fact, using this concept, single electron sensitivity is reached in the instrument used in this study. At the same time the signal level is significantly improved itself by the use of aberration corrector which, together with smaller probe size, provides higher current density. Altogether, these allow acquisition times for most core edges of interest to be limited to 1 s. This is a crucial factor for atomic resolution EELS because longer exposure times limit not only the spatial resolution by instabilities of the microscopes but also enhance the possibility of sample damage.

Typical EELS results (courtesy of Gerd Duscher) which could be almost routinely obtained from the described instrument (before aberration correction being installed) are shown in Figure 14. The Si-$L_{2,3}$ ionization edge changes its shape and energy onset as the electron probe moves across the Si/SiO$_2$ interface (Z-contrast image of the Si/SiO$_2$ interface is obtained at VG HB603 dedicated STEM).
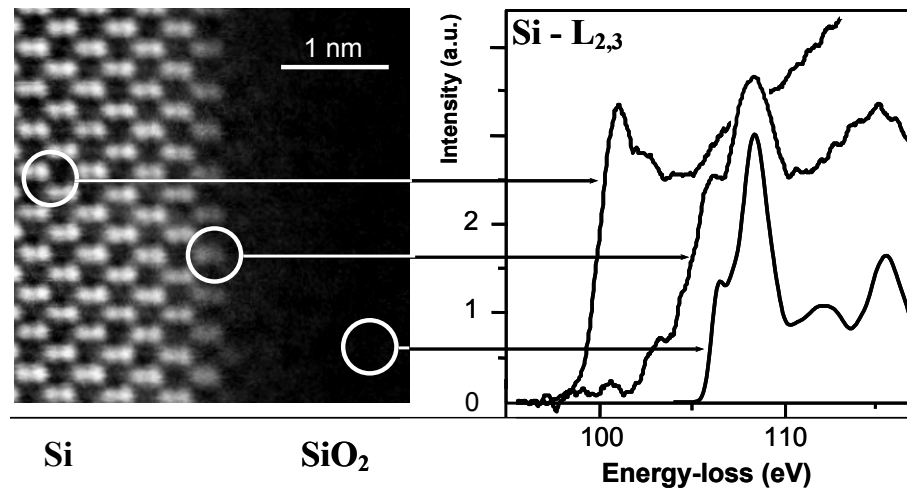
Figure 14. Z-contrast image and EELS of the Si/SiO$_2$ interface.

One finds the Si-$L_{2,3}$ edge onset in the crystalline Si part (Si^{0+}) to be at 99.8 eV with a first maximum at about 101 eV, whereas the SiO$_2$ spectrum (Si^{4+}) is characterized by main

absorption features at 106 and 108 eV. The EELS from the interface region corresponds to the mix of intermediate oxidation states (Si^{1+}, Si^{2+}, Si^{3+}). Even without aberration corrector, for the optimum probe diameter of the whole 0.22 nm (for VG HB501), such results with near-atomic resolution represented a significant interest, for example, for comparison with theoretical calculations and modeling of the Si/SiO_2 interface (see below section 3.4).

In it current state, with aberration corrector installed, the VG HB501 UX dedicated STEM fulfills all conditions to obtain real atomic column resolution in EELS [88]. Although thus far the highest available energy resolution and the highest available spatial resolution have not been achieved simultaneously, the combination of STEM and EELS allows one to approach the quantum mechanical limit for spatial resolution in EELS.

3.4. Density Functional Theory

So, the combination of *Z*-contrast imaging and EELS allows us to obtain precise information on the atomic structure, chemical composition and electronic structure at interfaces and defects on the atomic scale. However, having obtained this wealth of information, the question remains as to how to incorporate it into a model for the interface that will allow us to understand the structure-property relationships. There are many theoretical methodologies that can be used to understand the structure-property relationships, ranging in complexity from *ab-initio* calculations to empirical potentials that have their origins in crystal chemistry. In order to calculate properties of the solid state one must in principle solve the Schrödinger (or Dirac) equation for an enormous number of interacting particles. Since it is not possible to solve this equation analytically for nontrivial systems, one has to find numerical schemes. However, it is rather obvious that even modern numerical

techniques for solving differential equations will fail for a many particle system containing more than only a few particles. Therefore, one has to find some method that can simplify the mathematical model of the system.

One of the simplifications used frequently in solid state physics is the Born-Oppenheimer approximation. Since the mass of the atomic nuclei is at least three orders of magnitude larger than the mass of the electrons one can keep the nuclei at fixed positions while solving the electron problem.

Nowadays, probably the most successful and most often used technique to solve the remaining many electron problem is based on the density-functional theory (DFT), which is based on two publications: the first by Hohenberg and Kohn [93] and the next by Kohn and Sham [94]. Two main principles are the foundation of density-functional theory:

1. All ground-state properties are functionals of the ground-state density $n(\vec{r})$.

For a system with a non-degenerate ground-state, it immediately follows that the ground-state itself, i.e. the many-particle wave-function of the ground-state, is a functional of the ground-state density. In particular, the ground state energy of the system is a density functional.

This first principle determines the basic strategy that can be used to deal with the many electron system of a solid. Not the many-particle wave-function is the quantity which is to be determined, but the electron density $n(\vec{r})$. Since this function depends on only three independent spatial coordinates rather than on $O(10^{23})$, this is a great simplification of the numerical task.

2. The ground-state total energy functional is minimal for the correct ground-state density with respect to all densities leading to the correct number of electrons.

This second principle now gives a minimization principle which can be used to determine the ground-state density. If the form of the total energy functional is known, the ground state density can be determined using this second principle.

The exact expression for the functional, however, is not known, due to the complicated nature of the many-body problem. That especially applies to the part of the total energy functional, which is called the exchange-correlation energy and describes all many-body quantum contributions beyond the Hartree-approximation. But, over the years, due to a great amount of thoughtful work, more accurate, more "physical" and more practical approximations have continued to appear.

The most widely used approximation is the Local Density Approximation (LDA) or its spin-dependent version, the Local Spin Density Approximation (LSDA). In this approximation the exchange-correlation energy is chosen to be at every point $\vec{r}$ the exchange-correlation potential of a free electron-gas with a uniform density of $n(\vec{r})$. The exchange-correlation energy is then no longer a functional of the density but just a function. This approximation is exact in the limit of a free electron-gas with uniform density, and one would expect that the approximation also performs reasonably well for a slowly varying density $n(\vec{r})$ such as the weakly perturbed electron gas. However, experience has shown that this approximation works well even for systems which have very inhomogeneous electron densities such as atoms and molecules.

To simulate properties of solids and to correlate them with experiential results for better understanding of structure-property relationships, the Vienna Ab-initio Simulation Package (VASP) based on DFT was used in the present study. VASP is a complex package for performing *ab-initio* quantum-mechanical molecular dynamic (MD) simulations using

pseudopotentials and a plane wave set. The approach implemented in VASP is based on the (finite temperature) local-density approximation with the free energy as the variational quantity and an exact evaluation of the instantaneous electron ground state at each MD-step using efficient matrix diagonalization schemes and an efficient Pulay [95] charge density mixing. The interaction between ions and electrons is described using ultrasoft Vanderbilt pseudopotentials or the projector augmented wave method. Both techniques allow a considerable reduction of the necessary number of plane-waves per atom for transition metals and first row elements. Generally not more than 100 plane waves per atom are required to describe bulk materials. Forces and the full stress tensor can be easily calculated with VASP and used to relax atoms into their instantaneous ground-state.

Although DFT, in principle, requires only the treatment of the overall charge density, in practice, the calculation of the (single-electron) wave functions is necessary to evaluate the kinetic-energy term, since the form of its density functional is not known. While this makes the calculation a little more tedious, it has, on the other hand, the advantage that the electronic band structure is calculated within a DFT calculation as a side product. The band structure calculated in that way is known to be highly accurate for valence bands, but severely underestimates the band gap due to the insufficient treatment of the exchange term in LDA or related approximations. However, the conduction bands are also found to be well described. Thus, if one can determine the onset of the conduction bands from a method other than the plain DFT band structure, then EELS spectra can be simulated. This is indeed possible by all electron calculations, as outlined in [89].

It was already mentioned the excellent properties of Si/SiO_2 interface make it an important object for comparison with the data obtained from other systems in this study. That

is why the results of *ab initio* calculations of the EELS spectra for the Si/SiO$_2$ interface are introduced here.

In *Z+1* approximation the examined atom is replaced by the element with atomic number *Z+1* in order to compensate the core-hole shift caused by the electron-excitation process. Duscher *et al*. [89] have shown that the *Z+1* approximation predicts the near-edge EELS spectrum reasonably well within standard pseudopotential density-functional calculations.
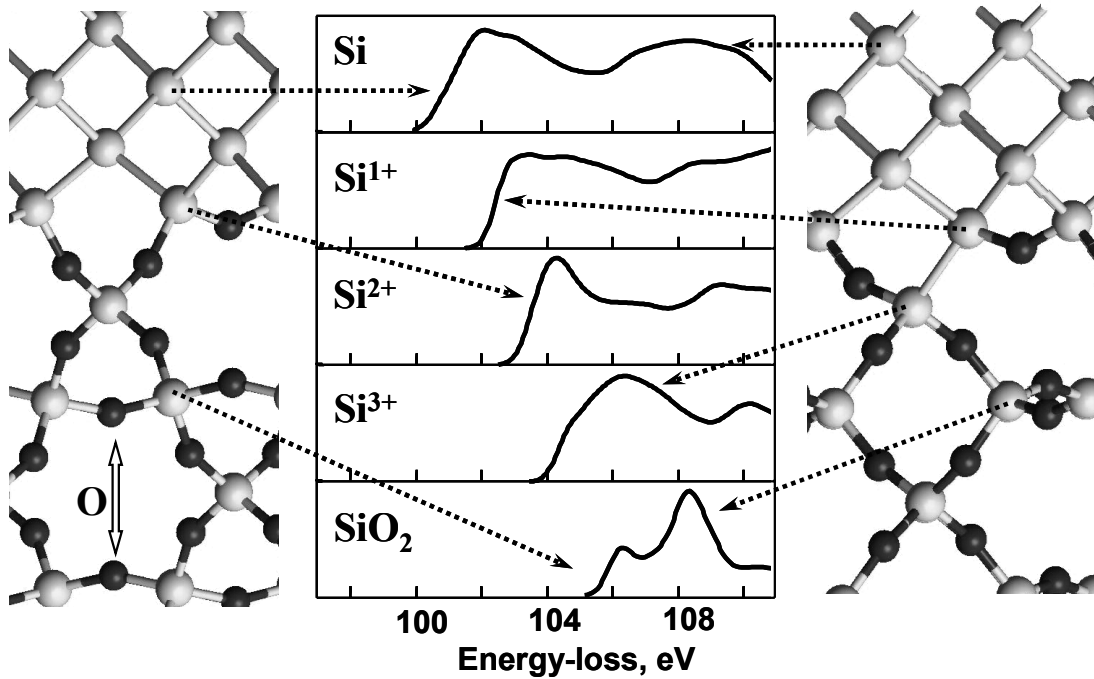
Figure 15. Calculated Si-L$_{2,3}$ edges at the Si/SiO$_2$ interface with respect to an abrupt interface model (on the left) and a sub-oxide interface model (on the right). (Courtesy of Gerd Duscher)

Two structures were selected for the theoretical EELS calculation. The first structure has an atomically abrupt interface, where all-perfect Si has one transition layer with Si^{2+} atoms (two O neighbors each), followed by perfectly 4:2 connected SiO$_2$ (Figure 15, left). In the second structure, the suboxide characteristics are introduced by removing the O atom from one Si-O-Si bond, which results in a structure with Si^{1+} and Si^{3+} atoms (Figure 15, right).

If the orbital and spatially resolved electronic conduction band DOS for the Si atoms in the different oxidation states are calculated and lined them up as described in [89], one can see that each oxidation state has its distinct shape and peak position as shown in Figure 15. Whereas Si^0 and Si^{4+} have very distinct spectra with prominent peaks at 102 eV for bulk Si and 108.5 eV for Si^{4+} respectively that can be easily detected (compare to experimental results in Figure 14), it is more difficult to sort out the intermediate oxidation states in the measured spectra (spectrum from interface region in Figure 14).

General analysis of the obtained data revealed that only the model of the interface with a sub-oxide layer is in agreement with experimental results from the thermally grown Si/SiO_2 interfaces.

4. RESULTS AND DISCUSSIONS

4.1. Si/GaAs Interface

Although the presence of dislocations at Si/GaAs interfaces was shown experimentally in recent years, the detailed nature of these dislocations has not been clarified. The aim of this study was to determine the atomic and electronic structure of 60° and 90° dislocations at the Si/GaAs interface and to clarify their influence on the electronic and optical properties of this interface. For that purpose the VG HB603 U dedicated STEM (300 kV) was used to resolve individual atomic columns in Si or GaAs. The dedicated STEM VG HB501 (100 kV) was used for imaging the dislocations and simultaneous electron EELS of the silicon edge at the dislocation cores.

The GaAs-thin films were grown by MOCVD at 650° C on a Si (001) substrate. Cross-section [110] samples were prepared by standard mechanical polishing and ion milling [70].

4.1.1. Z-contrast Imaging

Figure 16 shows a typical Z-contrast image of the Si/GaAs interface. GaAs is heavier than Si and therefore appears brighter in the Z-contrast image. The ellipse-like bright spots are formed by two neighboring columns of Ga and As (or Si). The distance between such columns in the $(1\bar{1}0)$ projection is 0.14 nm in GaAs (larger than the electron probe size), and should show up as two circular spots that touch (so called "dumbbells").

The intensity profile along one atomic plane in the [001] direction reveals polarization of "dumbbells" on the GaAs side far enough from the interface (free from stress field). This allows the differentiation between Ga and As atoms within one "dumbbell" and the

conclusion that GaAs is Ga terminated at the interface to Si. This fact is used for the determination of dislocation structures.
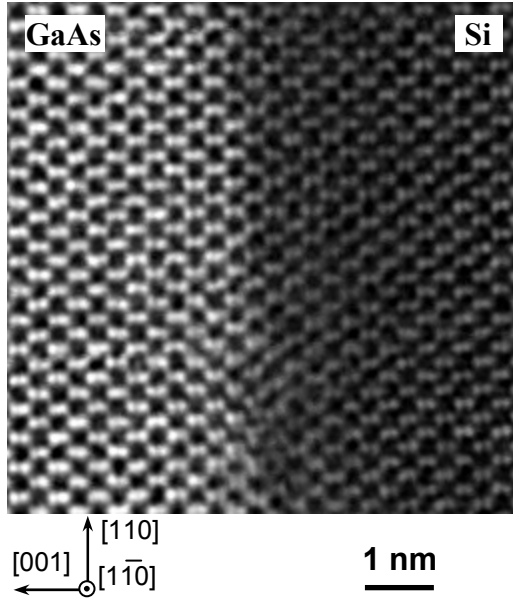
Figure 16. Z-contrast image of Si/GaAs interface.
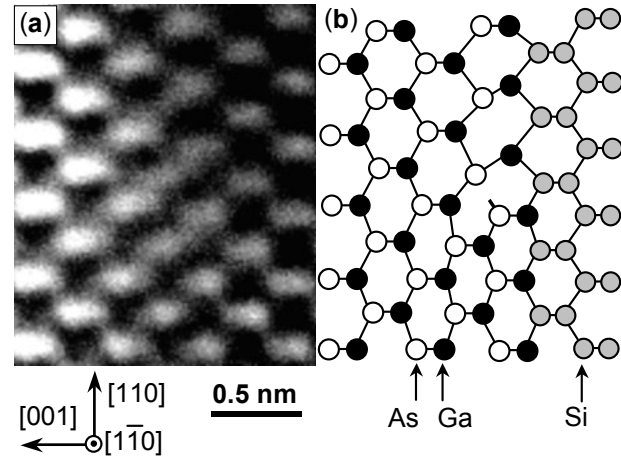
Figure 17. Z-contrast image of a 60° dislocation (a) and the structural model of the dislocation core (b).

Two regions can be clearly identified at this interface in Figure 16. One (the upper half of Figure 16) has a continuous transition of atomic planes from the GaAs to the Si side. The lower half demonstrates a certain distortion in transition, corresponding to a dislocation. Neighboring atomic columns in a "dumbbell" are not distinguishable in the vicinity of the dislocation core due to the stress fields caused by the dislocations. Such a stress field changes the channeling conditions of the atomic columns. Specifically a tilt near the surface can occur as a result of surface reconstruction. For the purpose of this study, this resolution degradation is not crucial because it is still possible to distinguish between overlapping and single atomic columns. A single column appears as a near circle, whereas two overlapping columns that are unresolved appear as an ellipse.

The number of 60° dislocations observed in this study was relatively small because most of them reacted to form 90° dislocations. Figure 17 presents a Z-contrast image of a 60° dislocation (a) and its corresponding atomic model (b). The dislocation core is compact and asymmetric. It forms an eight-sided polygon (octo-ring), which contains a single column of As atoms with a coordination different from the surrounding matrix. This constitutes a so-called dangling/broken bond, which is expected to cause additional energy levels in the band gap (midgap states) [96]. In this study, the exact atomic structure of a 60° dislocation at the Si/GaAs interface has been directly determined experimentally.
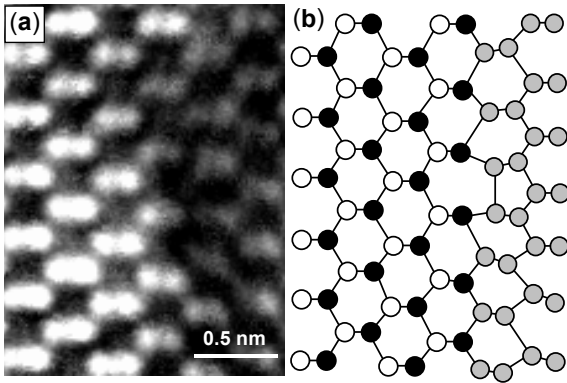
Figure 18. Z-contrast image of a reconstructed 90° dislocation (a) and the structural model of the dislocation core (b).
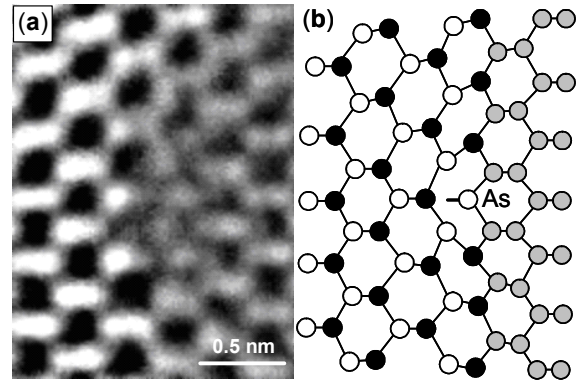
Figure 19. Z-contrast image of a non-reconstructed 90° dislocation (a) and the structural model of the dislocation core (b).

In contrast to the 60° dislocations, the 90° dislocations at the Si/GaAs interface showed a symmetrical configuration. Two different types of 90° dislocations were observed.

The reconstructed 90° dislocation is shown in Figure 18. This dislocation causes even less distortion of the surrounding matrix than the 60° dislocations. In this configuration, there are no broken bonds and the well-known core structure consisting of 5- and 7-fold ring units is observed. Unexpectedly, another type of 90° dislocation was found. This 90° dislocation is

not reconstructed but consists of structural units of 6- and 8-fold rings (Figure 19). A single As column is present at the center of the dislocation core, which causes dangling bonds. The presence of this As column seems to be the reason for a strong stress field around the dislocation core. As a result, the position of neighboring atoms and the relative distance between them are different from those of the reconstructed dislocation (compare Figure 18(b) and Figure 19(b)).

4.1.2. EELS

To complete the compositional profile across the Si/GaAs interface and to determine the possible influence of dislocations on electrical properties of this interface, the EELS measurements were employed.
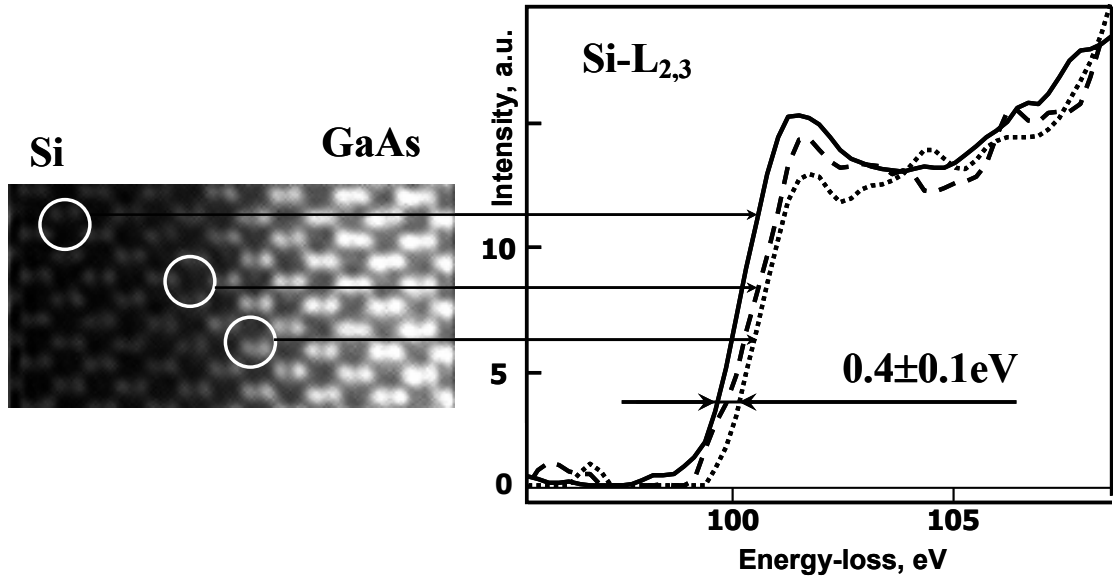
Figure 20. EELS of the Si-$L_{2,3}$ edge from the planar Si/GaAs interface (no dislocations).

Figure 20 shows the spatial distribution of the Si-$L_{2,3}$ edge shape across the Si/GaAs interface at the region containing no dislocations. This distribution shows a noticeable shift

of 0.4 eV of the Si-$L_{2,3}$ ionization edge at the planar Si/GaAs interface suggesting an opening of the Si band gap. Together with the intensity profile of a Z-contrast image, the EELS data also demonstrate that the Si/GaAs interface is graded and it takes several atomic planes for transition from Si to GaAs.
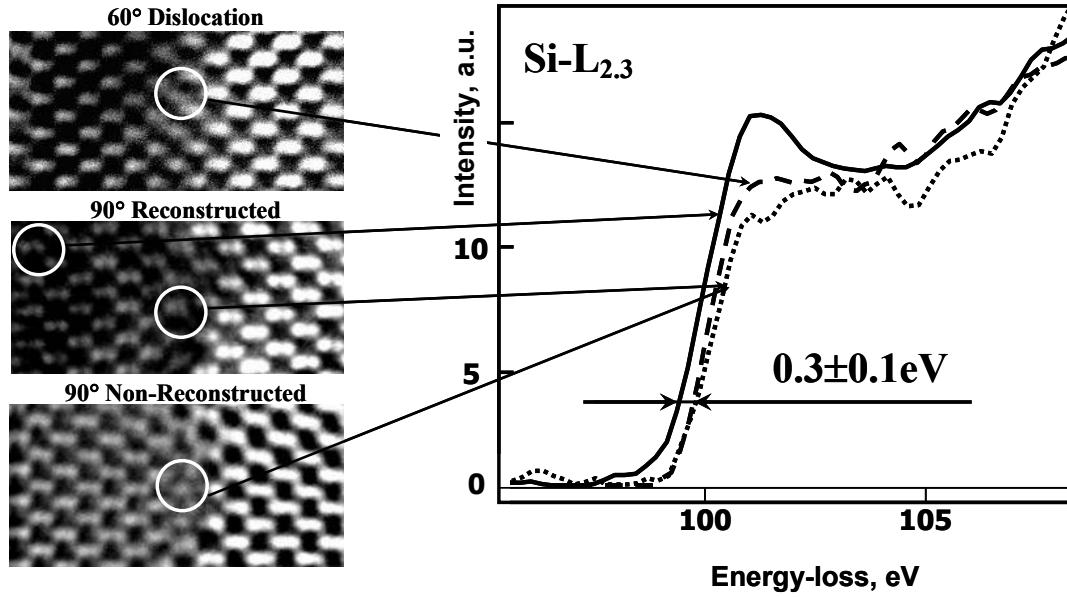
Figure 21. Comparison of Si-$L_{2,3}$ edges obtained from bulk Si and dislocation cores at the Si/GaAs interface.

Figure 21 demonstrates the shape of the Si-$L_{2,3}$ edge in bulk Si (solid line) compared to those from the dislocation cores at the Si/GaAs interface. Also, a noticeable shift of 0.3 eV of the Si-$L_{2,3}$ ionization edge is seen. Within experimental accuracy this is the same shift as in the case of the planar interface.

4.1.3. Calculations

The resolution degradation of Z-contrast imaging around dislocations (due to the stress field) does not allow the differentiation of which type of atom (Si, Ga or As) forms an additional atomic column at the core of non-reconstructed 90°dislocations. To refine the

structure of 90° non-reconstructed dislocations *ab initio* calculations based on density functional theory were used. First of all, two super-cells were built to calculate the energy difference between reconstructed and non-reconstructed dislocations. The super-cell for the reconstructed dislocation [region 1 in Figure 22 (a)] consists of 12 Si, 25 Ga, and 25 As atoms (62 altogether). For the model of the non-reconstructed dislocation, one more Ga atom is added in to the super-cell as an atom with a dangling bond in the core [region 2 in Figure 22 (b)]. The choice to use Ga atom was conditioned by the fact that, in the studied sample, GaAs was Ga terminated at the interface to Si. In order to meet periodic boundary conditions in X, Y, and Z directions, another dislocation (reconstructed) is introduced in both super-cells [region 3 in Figure 22 (a) and (b)].
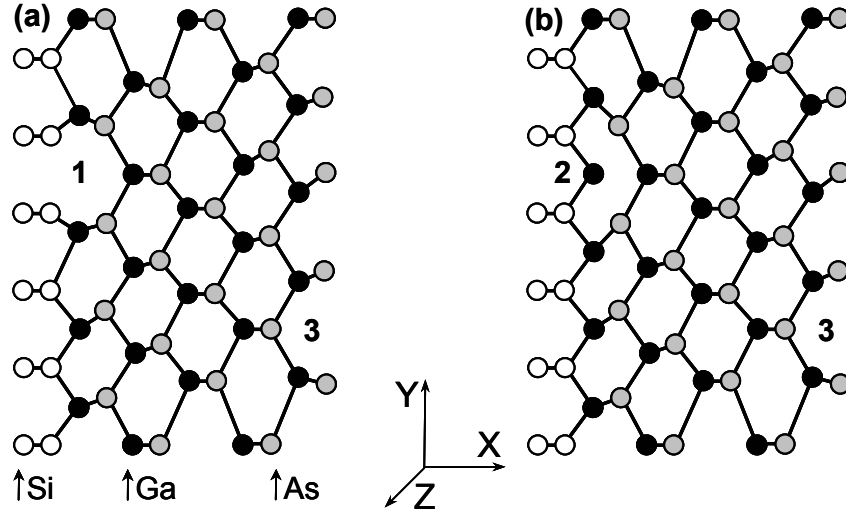
Figure 22. Initial super-cells for reconstructed (a) and non-reconstructed (b) dislocations.

The ionic and electronic subsystems of both super-cells were relaxed by means of VASP package to obtain the total energies which then were compared. It turned out that the energy of the relaxed super-cell for the non-reconstructed dislocation is lower by $\Delta E(rec \rightarrow non) =$

3.5 eV, which was expected since that super-cell has one more atom. The increase of super-cell size incurred by adding 24 more Si atoms in the X direction did not result in a significant change of $\Delta E(non \rightarrow rec)$ (less then 0.1 eV), which implies that this new number of atoms (87) in the super-cell is satisfactory for energy estimation. Thus, from the energy point of view, the geometrical structure of non-reconstructed 90° dislocations is not contradictive.

To establish the elemental structure of non-reconstructed 90° dislocations three models (similar to the super-cell in Figure 22 (b) with the additional 24 Si atoms) were analyzed in search for the one with the minimum total energy. These models differed by the type of atom (Si, Ga, As) forming a single atomic column at the core of the non-reconstructed 90° dislocation [region 2 in Figure 22 (b)]. Calculations revealed that transition from the structure with Ga atom in the dislocation core to the structure with Si atom lowers the energy by $\Delta E(Ga \rightarrow Si) = 2.2 \pm 0.1$ eV. At the same time, transition from Ga to As atom lowers the energy by $\Delta E(Ga \rightarrow As) = 2.9 \pm 0.1$ eV.

Moreover, the chemical potential of different species was taken into account by calculation of the corresponding energies of single atom in pure Si, As, and Ga. Those calculations showed that the exchange Ga→As should lower the energy by 1.4 eV (but the actual change $\Delta E(Ga \rightarrow As)$ is bigger), while the exchange Ga→Si should lower the energy by 3.4 eV [which does not happen for $\Delta E(Ga \rightarrow Si)$]. Thus, the structure with an As column at the core of the non-reconstructed 90° dislocation is energetically preferable. It is this structure is shown in Figure 19(b).

As soon as the structure of the non-reconstructed 90° dislocation is clarified, it is important to examine the possible electrical activity of the dislocation core, in other words to

find out if it may introduce energy levels in the bandgap. For that purpose, an even larger Si/GaAs super-cell (consisting altogether of 103 atoms) was constructed [see Figure 23(d) or Figure 24(d)]. After atoms relaxation, the density-of-states (DOS) for this super-cell was calculated. The main results of these calculations are summarized in Figure 23 and Figure 24.

Figure 23. Calculated DOS of Si atoms (a, b, c) with respect to their position in the relaxed Si/GaAs super-cell (d) with reconstructed and non-reconstructed 90° dislocations. The dotted line corresponds to bulk Si.

Although from direct analysis of the obtained DOS, the bandgap of the considered super-cell did not become apparent, its virtual position can be identified by the location of Fermi level which corresponds to the top of the valence band and by the fact that for pure Si *ab initio* calculations in the local density approximation result in the value of bandgap of ~ 0.7 eV. The Fermi energy for the Si/GaAs super-cell was found to be $E_F = 3.47$ eV. After that, the following may be concluded from the calculated DOS. First, the density-of-states in the valence band of Si atoms at the Si/GaAs interface is higher than that of bulk Si.

Second, close to the Fermi level, in the energy range that should correspond to the bandgap of this semiconductor structure, the DOS of the Si atom located at the core of the

non-reconstructed 90° dislocation has a significantly higher value [Figure 23(c)] compared to the DOS of an atom corresponding to bulk Si [Figure 23(a)]. The same is true for the DOS of the As atom at the core of the non-reconstructed 90° dislocation compared to the DOS of an As atom in bulk GaAs [see Figure 24(c) and Figure 24(a)]. This implies the existence of energy levels in the bandgap of the semiconductor structure containing the non-reconstructed 90° dislocation, i.e. the electrical activity of this type of dislocation. At the same time, Si and As atoms located at the core of the reconstructed 90° dislocation do not exhibit a significant difference in the DOS compared to the bulk Si or GaAs [compare Figure 23(b) to Figure 23(a); and Figure 24(b) to Figure 24(a)], thus confirming the electrical neutrality of the reconstructed 90° dislocation.

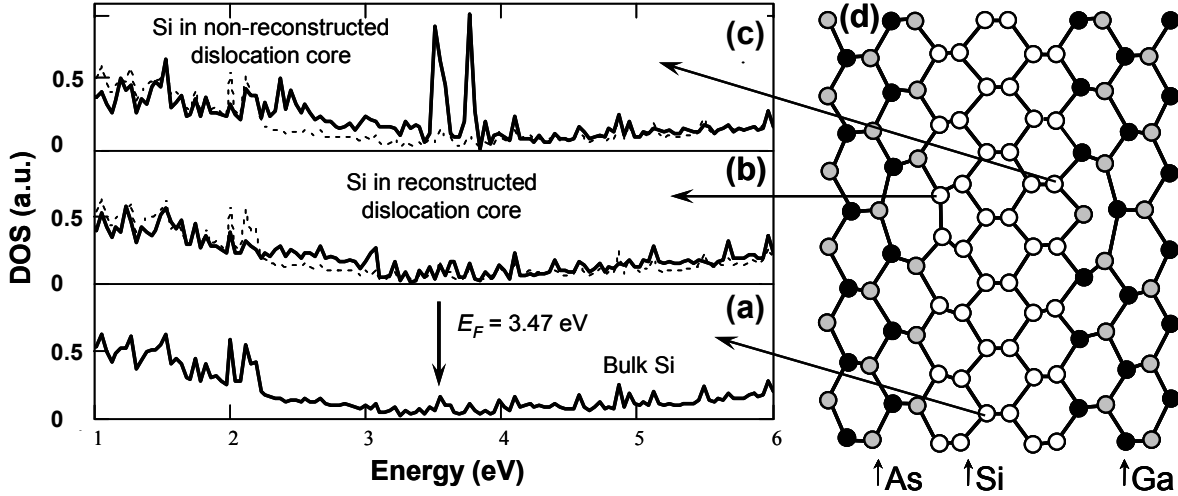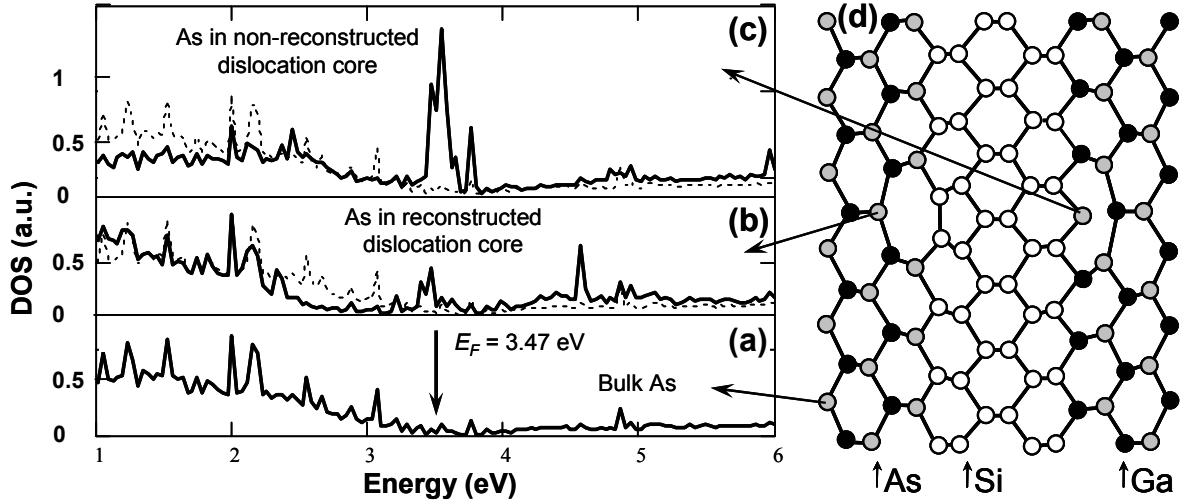**Figure 24.** Calculated DOS of As atoms (a, b, c) with respect to their position in the relaxed Si/GaAs super-cell (d) with reconstructed and non-reconstructed 90° dislocation. The dotted line corresponds to bulk As.

4.1.4. Discussion

Possible structures of 90° dislocations in diamond and diamond-like materials were discussed theoretically decades ago by Hornstra [97]. The following point was specifically

stressed: two types of 90° dislocations with [110]/2 Burgers vectors and (001) glides plane may exist in diamond and diamond-like structures, and these two types cannot simply be transformed into each other.

A single atomic column at the center of a dislocation core and the resulting dangling bonds are specific features of the non-reconstructed 90° dislocation (Figure 19). A similar structure of threading dislocations in GaN was reported in [98] and [99] (compare Figure 19(b) and Figure 25). However, the structure of non-reconstructed 90° dislocations at the Si/GaAs interface, obtained in this study directly from Z-contrast images and confirmed by computer modeling, is demonstrated for the first time [100].
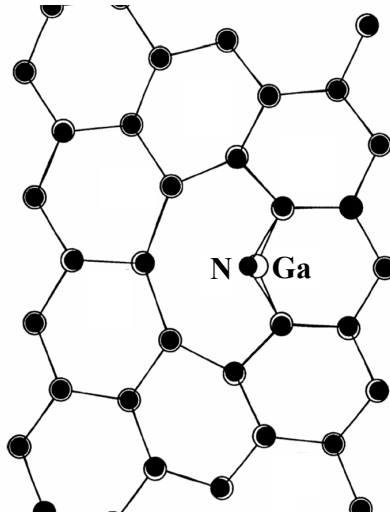
Figure 25. The relaxed core of a threading edge dislocation in GaN from [99].

The reconstructed dislocation structure can be obtained from the non-reconstructed one by omitting the atoms with free bonds (Figure 18). This reconstructed dislocation is known to exist in diamond and diamond-like materials. Its structure was calculated theoretically in Si and Ge [101]. It should be noted that the tendency towards reconstruction is relatively weak

in GaAs [99]. This may be the reason that we found different dislocation core structures than those in Si or Ge.

The shift of the ionization edge, in general, might be caused by the stress field at the interface due to the lattice mismatch between two materials (which is the case for Si and GaAs). At the same time, the presence of the dislocation changes the local picture of the stress field significantly. One would then expect to find the difference in the shift of ionization edge at different places along the interface. The EELS data, however, show approximately the same shift of the Si-$L_{2,3}$ ionization edge both at the planar Si/GaAs interface and right at the dislocation core. Thus, it is more reasonable to suggest that the shift of Si ionization at the interface is a reflection of a core level shift of Si due to the increasing concentration of atoms (Ga and As) with a higher number of valence electrons (see more in 4.2.3 about core level shift at the Si/Ge interface). The calculations of the DOS confirmed the increase of the valence electron density for Si atoms at the Si/GaAs interface (Figure 23).

Going back to the question of the electrical activity of dislocations, it should be mentioned that 60° dislocations are expected to introduce energy levels in the bandgap. For that reason, the search for a treatment process to make 60° dislocations recombine into 90° dislocations (supposedly electrically neutral) was launched. Apparently to some extent this goal was achieved in the process used for the production of the studied sample. Although not completely eliminated, the number of 60° dislocations was significantly reduced. However, the finding of electrically active 90° dislocations imposes new difficulties on the way to a good Si/GaAs interface. Since non-reconstructed 90° dislocations were discovered just recently, the mechanism of their formation and a possible way to avoid or passivate them are still to be found.

4.1.5. Summary

Z-contrast imaging confirmed the existence of 60° and 90° dislocations at the Si/GaAs interface. Thus, it is a semi-coherent interface. It is also a graded interface, i.e. transition from Si to GaAs occurs over several atomic planes (about 2 unit cells), where the properties of the material is neither like bulk Si, nor like bulk GaAs.

Atomic structures of dislocations were obtained with resolution high enough to distinguish a single atomic column of gallium or arsenic. As a result, the observation of the structure of non-reconstructed 90° dislocations with dangling bonds was possible. Since both 60° and non-reconstructed 90° dislocations apparently exhibit dangling bonds, one may expect both types of dislocations to cause energy levels in the bandgap. For the non-reconstructed 90° case the existence of energy levels in the bandgap is confirmed by *ab initio* calculations of the DOS. Therefore, this type of dislocation is detrimental to the electrical and optical properties of the Si/GaAs interface. Based on the reported here results, a possible solution for an electro-optically good interface can only be achieved through segregation to the dislocation core. Further modeling is needed to determine which element could lift the states associated with these dislocations out of the band gap. Since such an approach does not guarantee success and because of the recent developments in the deposition of Ge on Si, the author would favor a Ge layer between Si and GaAs (for the integration of optoelectronic devices into silicon technology).

4.2. Si/Ge Interface

A recent extension of the traditional silicon technology is the mixing of germanium into the silicon wafer material. This newer process is the driving force behind the current explosion in low-cost, lightweight, personal communications devices like digital wireless handsets. By combining silicon with germanium, semiconductor manufacturers are able to achieve a performance close to the characteristics of gallium arsenide (much faster than Si devices) at a considerably reduced cost comparable to traditional Si-based technologies. In this connection, the characterization of atomic arrangements at the interface between Si and Ge is urgently required.

For this study, the Ge film on a Si substrate was fabricated at the Oak Ridge National Laboratory by Ge implantation with 100 keV Ge$^+$ ions at a fluency of ~10^{16} cm^{-2} and subsequent high-temperature (800° C) wet oxidation, as described in [102]. The Ge is ejected during the oxidation step from the oxide and piles up on the substrate side of the interface (sometimes called the "snow-plowing effect" [102,103]) forming nearly pure epitaxial layers of Ge on Si substrates with a very smooth interface. However, Si/Ge/SiO$_2$ systems have been found to have significantly worse electrical properties than Si/SiO$_2$ systems [103,104]. All the cross-section [110] samples for Z-contrast and EELS measurements were prepared by standard mechanical polishing and ion milling [70].

4.2.1. Z-contrast Imaging

Figure 26 (a) shows a typical Z-contrast image of a sample with the Si substrate aligned in the [110] direction. The Ge layer is brighter since Ge is heavier then Si. The "dumbbell" structure is clearly seen both on the Z-contrast image (bright double spots) and in the

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intensity profile (as double peaks) across the Si/Ge interface [Figure 26 (b)]. While far from the interface on the Si side the intensity profile is practically flat, at the very interface there is a certain slope as marked in Figure 26 (b). This slope results from the atomic mass increase at the transition from Si to Ge, which extends over 3-4 dumbbell layers (about 1.5 nm).
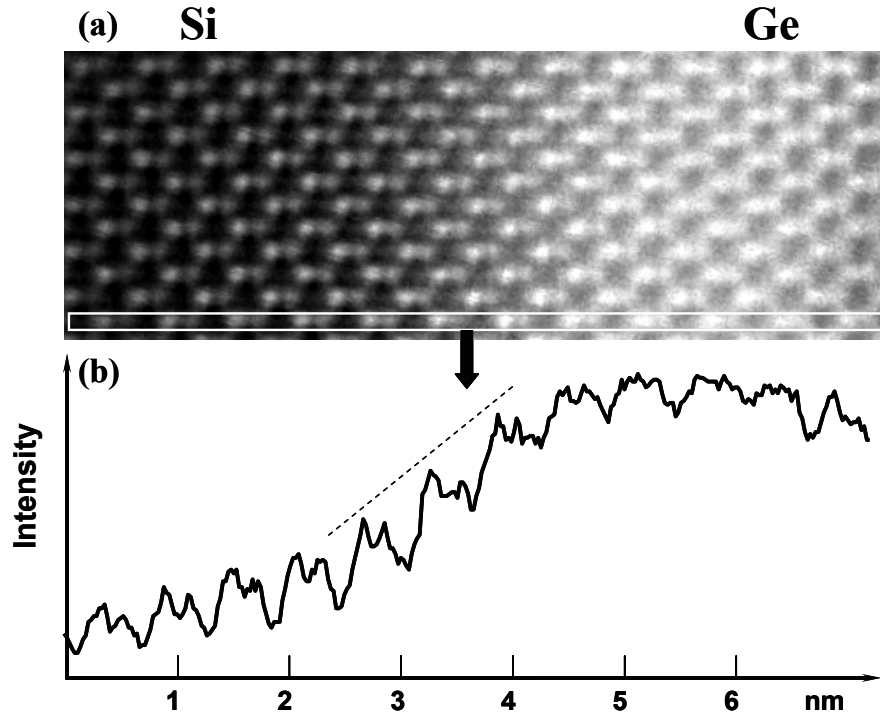
Figure 26. Z-contrast image of a Ge film on a Si substrate (a) and intensity profile of the Z-contrast image along one atomic plane across the interface as indicated in the micrograph (b).

The scrupulous analysis of all Z-contrast images of the studied Si/Ge interface revealed neither atomic layer steps nor dislocations, which indicates an atomically flat interface. Nevertheless, some structural defects, apparently induced by ion implantation [105, 106], were still present. A few stacking faults were detected along the Si/Ge interface, with an average distance between them of about 70-80 nm. A typical stacking fault crossing the Si/Ge interface is shown in Figure 27, where the distinctive change of dumbbell orientation can be identified.
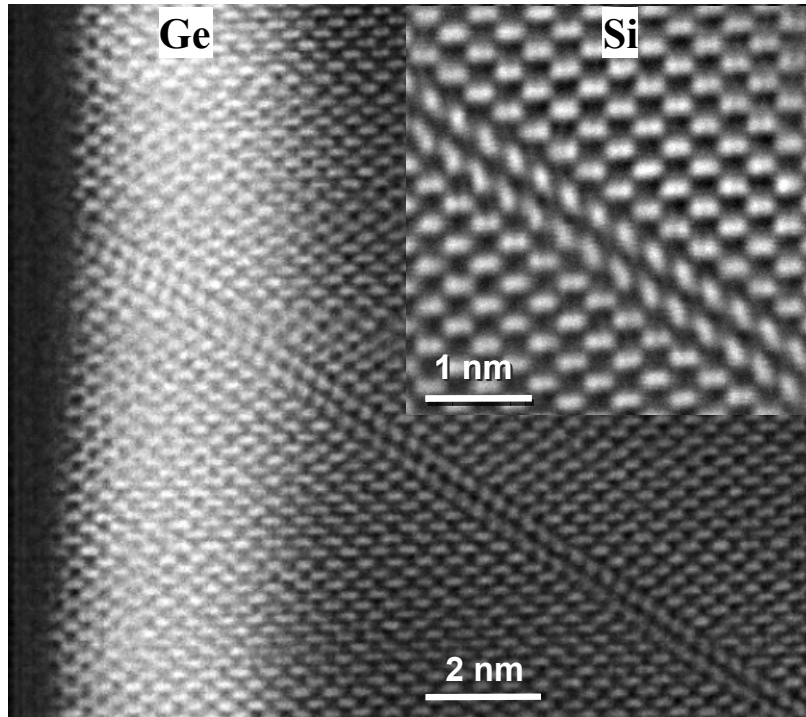
Figure 27. Stacking fault in the Si/Ge system.

4.2.2. EELS

In search for chemical heterogeneity across the Si/Ge interface and to study the possible influence of Ge on the position and shape of the Si-$L_{2,3}$ ionization edge, the EELS analysis was performed. Spectra were recorded as a line-scan, i.e. continuously, moving from one atomic plane to the next one.

Figure 28 shows the spatial distribution of the Si-$L_{2,3}$ edge shape across the Si/Ge interface. Compared to bulk Si (solid line) the spectra from the region next to the Ge are shifted (about 0.4 eV maximum) towards higher energies (as in the case of Si/GaAs) and also have a modified shape. Also, similarly to the Si/GaAs interface, the transition from Si to Ge occurs gradually (over several atomic planes). This observation directly correlates with data from Z-contrast images.
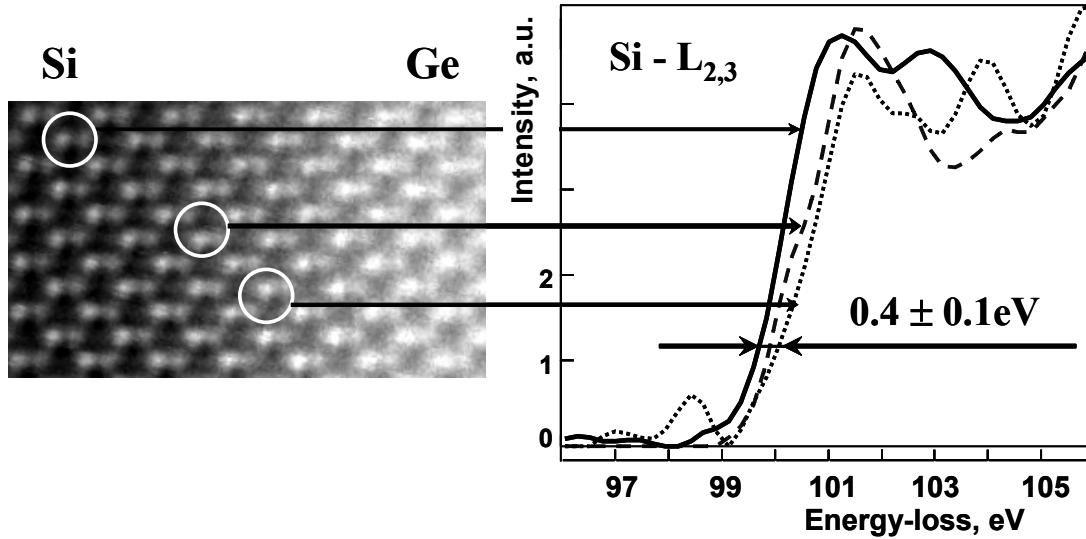
Figure 28. The distribution of the Si-L$_{2,3}$ ionization edges across the Si/Ge interface.

4.2.3. Discussion

Z-contrast imaging together with EELS confirmed that Ge implantation into a Si substrate and subsequent high-temperature wet oxidation may result in an atomically flat (no dislocations or steps) interface between Si and Ge. The presence of stacking faults induced by ion implantation may cause the degradation of the electrical properties of the Si/Ge interface, and could be one of the reasons for the worsened properties of the Si/Ge/SiO$_2$ system. This problem, however, can be solved by the appropriate selection of ion dose and energy, and annealing treatment [105].

The pile-up in the examined sample leads to the compact Ge layer which contains no Si within the detection limits (about 5 at. %). In this Ge layer, in the direction parallel to the interface, the lattice constant corresponds to that of the Si lattice. Thus essentially, the studied sample has a layer of pure, completely strained Ge on Si substrate. One can expect to find significantly enhanced mobility (higher than even in pure bulk Ge) of charge carriers in such a layer [33].

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The EELS analysis shows that the shift of the Si-$L_{2,3}$ ionization edge at the Si/Ge interface has the same character as the shift at the Si/GaAs. The Ge film is strained and there is a significant stress at the interface, which can modify the band structure of both Si and Ge. That is also the case for the Si/GaAs interface. At the same time, different stress conditions do not seem to influence the character of the Si-$L_{2,3}$ ionization edge shift (i.e. towards higher energies, see Figure 21). Those two materials, GaAs and Ge, have different characteristics (for example different band gaps), and yet they result in similar behavior of the Si-$L_{2,3}$ ionization edge at the interface. What they have in common, however, is the number of valence electrons, which is bigger than that in Si. Thus, with an increase of GaAs or Ge concentration around Si, there is an effective Coulomb repulsion of Si core electrons by the increasing number of valence electrons. This repulsion lowers the energy of inner shell electrons (core level shift) and is observed as an ionization edge shift towards higher energy in SiGe [107].

4.2.4. *Summary*

Z-contrast imaging demonstrates that the interface between Si and Ge can be produced as a coherent, atomically flat, graded interface, with transition taking about 1.5-2 nm. Providing that the stacking fault problem is solved, the Ge on Si system with such an interface quality (no dangling bonds and associated charge traps) may be used for improvement of charge carrier mobility and thus has a potential for application in high performance devices. EELS measurements of the Si-$L_{2,3}$ ionization edge suggests a core level shift at the transition from Si to Ge, which might be important to the understanding of band structure modifications in SiGe alloys.

4.3. Ge/SiO$_2$ Interface

Although Ge exhibits significantly enhanced electronic and optoelectronic properties [9] compared to Si, it was believed to completely lack a natural oxide or other insulator to form an interface with the quality of Si/SiO$_2$. In the following, it is shown that the interface between Ge and SiO$_2$, fabricated as described in [102], is not only as good as, but significantly better than the Si/SiO$_2$ interface, and embodies the ideal case of only *one* transitional layer. For this purpose, the same sample as in section (4.2) was studied. This time, however, the concentration is on the side where Ge is covered by SiO$_2$.

4.3.1. Z-contrast Imaging

A typical Z-contrast image of the sample is shown in Figure 29 (a), where Si, Ge, and SiO$_2$ regions can be observed. The SiO$_2$ region appears the darkest since SiO$_2$ is less dense and has effectively the smallest atomic number Z, compared to bulk Si or Ge.
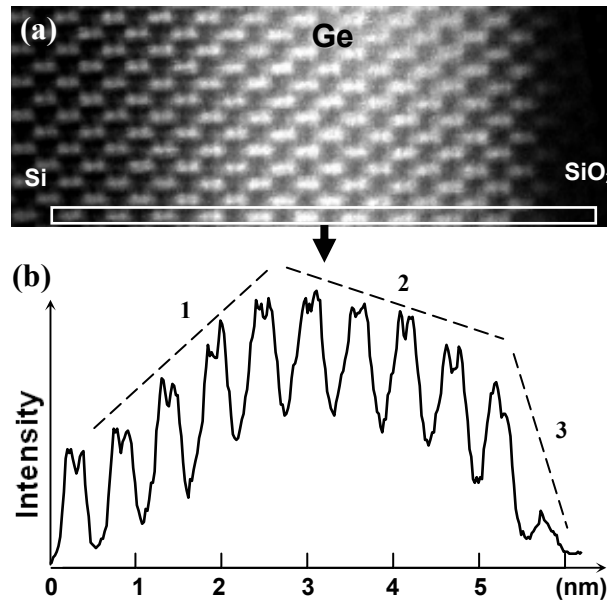
Figure 29. Z-contrast image of a Ge film on a Si substrate covered by SiO$_2$ (a); intensity profile of the Z-contrast image along one atomic plane across the interface as indicated in the micrograph (b).

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The corresponding intensity profile in Figure 29 (b) demonstrates 3 distinct slopes. Slope 1 is already identified in (4.2.1). Slope 2 corresponds to a nearly linear change in the Ge film thickness as a result of the wedge-shaped sample (see section 4.3.2). The sudden drop of intensity (slope 3) indicates a compositional change in the last "dumbbell" layer before the interface. Thus, nearly all of the compositional change from Ge to SiO_2 takes place within approximately one transitional layer right next to the interface.
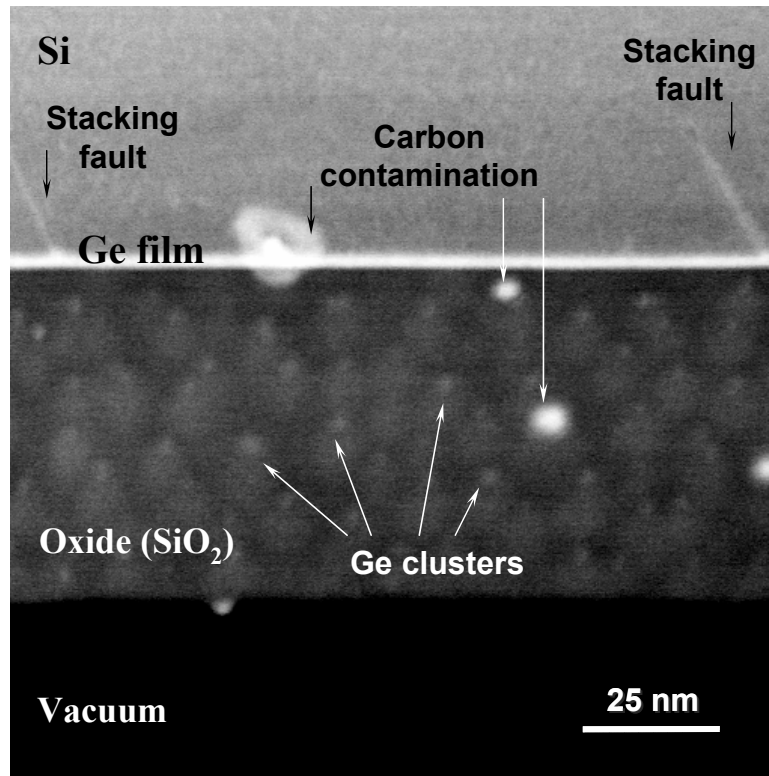
Figure 30. Low magnification Z-contrast image of Ge film on a Si substrate covered by SiO_2.

Low magnification Z-contrast images of the studied sample (see Figure 30) revealed the non-homogeneous intensity distribution in the amorphous oxide region (SiO_2), starting 10-15 nm away from the Ge film. Based on the results of later performed simulations this non-homogeneity can be identified as Ge clustering.

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4.3.2. EELS

To gain further insight into the atomic configuration of the Ge/SiO$_2$ interface and the Si oxidation states, EELS measurements of the Si-$L_{2,3}$ edge were employed. Since initially it was expected for the spectra to look similar to those of regular Si/SiO$_2$ interfaces, the experimental results of EELS measurements at a thermally grown Si/SiO$_2$ interface are also displayed here. For both Si/SiO$_2$ and Ge/SiO$_2$ interfaces, the spectra have been recorded with a spatial step-width of approximately 1.4 Å (inter-atomic spacing of the (100) planes of Ge or Si), and thus have a resolution of single atomic layers.
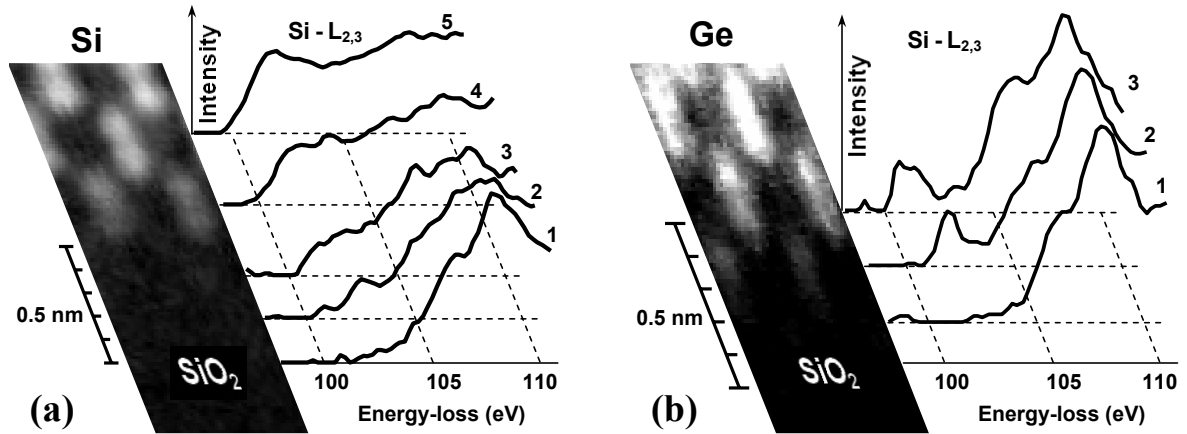
Figure 31. Line-scan EELS of Si-L$_{2,3}$ ionization edge across (a) the Si/SiO$_2$ interface, (b) the Ge/SiO$_2$ interface.

Figure 31(a) shows the spatial distribution of the Si-L$_{2,3}$ edge shape across the thermally grown Si/SiO$_2$ interface. Stoichiometric SiO$_2$ appears no sooner than 0.5 nm away from the interface (spectrum 1). On the transition to bulk Si, the ionization edge undergoes certain transformations, corresponding to the absorption features of the intermediate oxidation states Si^{3+}, Si^{2+}, Si^{1+} (compare to the theoretical calculation in Figure 15). As a result, a minimum of three transition layers (spectra 2-4) with a mixture of all intermediate oxidation states has

been found for all Si/SiO$_2$ interfaces [6]. Such a diffuse profile is not consistent with a chemically abrupt interface.

This is in stark contrast to the measured EELS spectra for the Ge/SiO$_2$ sample, which are shown in Figure 31(b). All spectra show Si^{4+} signals from the surface oxide in this extremely thin sample (see Figure 32), and the Si^{4+} signal might be further increased by the delocalization of the inelastic scattering process. This poses no problem, since the following analysis is based on the signals of the oxidation states less than 4+.

oxide (SiO$_2$)

Si/Ge

Figure 32. The thickness profile of the studied Si/Ge/SiO$_2$ sample.

The ionization edge which corresponds to completely oxidized Si^{4+} is observed on the amorphous side just 2 Å away from the last crystalline layer (Figure 31(b), spectrum 1). One layer away from the oxide at the first crystalline layer, a clear signal of Si^{2+} [108, 109] appears (Figure 31(b), spectrum 2), showing remarkable resemblance to the theoretical calculation in Figure 15. In the second crystalline layer, the signal of bulk Si (Si^{0+}) was found with the modifications typical for bulk SiGe (Figure 31(b), spectrum 3), which looks different from pure Si due to the core level shift caused by Ge [107].

The EELS data analysis from subsequent atomic layers on the crystalline side of the interface shows that within one or two atomic layers the Si concentration falls below the detection limit (about 5 atomic %). No linear intensity increase typical for the mix of suboxide oxidation states in non-abrupt Si/SiO$_2$ interface (e.g. Figure 31(a), spectrum 2) is detected.

4.3.3. Calculations

For the better understanding of the thermal oxidation process of SiGe at different Ge distributions and oxidation conditions and also to examine Ge as a possible cause for the poor electrical properties of Si/Ge/SiO$_2$ systems, a Monte Carlo model similar to the model in [110] was formulated and density-functional calculations were used with experimental results for the parameters [109]. Calculations were performed in collaboration with W. Windl and T. Liang from Ohio State University.

First, the density-functional based *ab initio* calculations were used to determine the energy per bond for Si and Ge atoms with different numbers of Si, Ge, and O neighbors. An energy expression thus was obtained as a function of the number of bonds to be used for the acceptance/rejection criterion in the Monte Carlo simulation:

$$E[\text{eV}] = -2.23n_{\text{GeGe}} - 2.47n_{\text{SiGe}} - 2.71n_{\text{SiSi}} - 7.07n_{\text{GeOGe}} - 8.05n_{\text{SiOGe}} - 8.94n_{\text{SiOSi}},$$

where the subscript represents the bond type and *n* is the number of the given bond type. In such a model the exact structure of the disordered oxide is not important, just the coordination, so the modeled oxide structure was based on the initial diamond structure and thus consists of (compressed) high-cristobalite. Although the different numbers are highly dependent on the strain, the energy *differences* remain nearly unchanged when homogeneous pressure is applied to the system. Thus, assuming homogeneous strain, one can neglect the local-pressure dependence.

The above expression for the energy indicates that the formation of Ge-O-Ge bonds dramatically increases the system energy as compared to Si-O-Si bonds. In other words, from an energetics point of view, Ge atoms "prefer" to stay away from the oxide region.

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In the next step, diffusion-limited oxidation was assumed and simulated by adding O atoms at the interface at a rate commensurate with experimental oxidation rates [103] and theoretical results for O_2 and H_2O diffusion through SiO_2 [110]. Since Ge is the much more mobile atom in the alloy, only hopping of Ge was considered with local-concentration dependent hopping rates adjusted to experimental results of Ge diffusion in oxide [110] and SiGe alloys [111].

The mechanism of the snow-plowing effect that leads to the Ge pile-up can be demonstrated on a reduced-scale model with a shallow Ge implant. An implanted Ge dose of 1×10^{16} cm^{-2} was assumed with a Gaussian distribution peaking at 11 nm with a lateral straggle of $\sigma = 4$ nm. The Monte Carlo simulation demonstrated that at high temperatures (1000° C), Ge becomes mobile in the Si matrix, and is also ejected out of the growing oxide at an appreciable rate due to the strong repulsive interaction between Ge and O. This results in the formation of pure SiO_2 right above an increasing pile-up of Ge. However, once the Ge concentration reaches about 3.0×10^{22} cm^{-3} (~60 at.%), the room for the Ge escaping from the oxide front becomes too limited (there are no Si atoms left in direct neighborhood to swap places with) despite the Ge diffusion deeper into the substrate, and the oxide starts to incorporate Ge.

The predicted Ge concentration is never higher than 5 at.% for the thin oxides that can be grow in our small simulation system and is on the order of magnitude of 1/10 of the Ge concentration on the substrate side. The threshold of ~60 at.% is in agreement with all reports of the formation of mixed oxides [112]. There, however, usually low-temperature oxidation had to be employed to produce an appreciable amount of Ge in the oxide.

4.3.4. Discussion

The results, combined from Z-contrast imaging and EELS, provide the base for the following model of Ge/SiO_2 interface (Figure 33). The first atomic layer in the crystalline part of the Ge/SiO_2 interface consists of partially oxidized Si^{+2}. This is confirmed by a comparison of the position and the shape of the $Si-L_{2,3}$ ionization edge (Figure 31(b), spectrum 2) with theoretical calculations for Si^{+2}. The EELS data and Z-contrast imaging from the second crystalline layer indicates a mixture of Si and Ge.
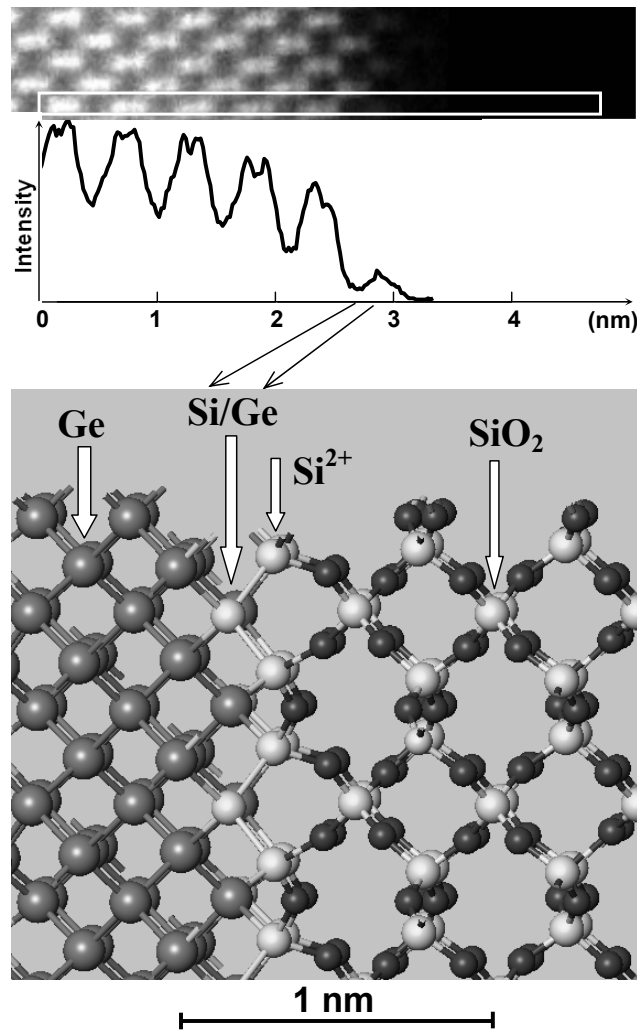

Figure 33. The model, deduced from experimental results, for the atomic structure of the Ge/SiO_2 interface.

Thus, the obtained data suggest an atomically sharp structure for this interface, with a layer of mixed Si and Ge, then with one transition layer, containing only Si^{2+} and pure oxide after only ~2 Å. This finding of a high-quality interface for the Ge/SiO_2 sample is consistent with recent high-temperature oxidation results [103] in which, however, no atomically abrupt interface has been observed. At the same time, these findings are in contrast with previous work [104, 113], but those studies dealt with higher Ge concentrations or lower oxidation temperatures.

As described in [40], the use of an ultrathin (~28Å), pseudomorphic Si interlayer between the gate dielectric SiO_2 and the Ge semiconductor substrate may result in the formation of an interface with midgap interface-state densities of $5 \cdot 10^{10}$ cm^{-2} eV^{-1} (comparable to the Si/SiO_2 interface). Here it is shown, that in the studied sample a layer with a significant concentration of Si between Ge and SiO_2 is formed in a natural way as a result of ion implantation and subsequent wet oxidation [102], thus one can expect that this Ge/SiO_2 interface has electrical properties comparable to the Si/SiO_2 interface.

At the same time, theoretical modeling predicts that what was originally interpreted as pure SiO_2 in [2] might indeed contain a small amount of Ge, provided that the Ge incorporation into the oxide is not eliminated by out-diffusion of Ge for longer oxidation times. This surprising finding is confirmed by Z-contrast imaging (Figure 30), where the apparent clustering of Ge atoms appears as a strongly non-uniform intensity distribution in the amorphous region. There are also very recent experiments based on X-ray photoelectron spectroscopy and Rutherford back scattering spectrometry for short oxidation times that confirm the above modeling and indeed find Ge in the oxide in small concentrations – usually 1/10 of the Ge concentration in the substrate which is in excellent agreement with the

Monte Carlo prediction – even for high-temperature oxidation [112]. Furthermore, the XPS spectra suggest Ge^0 and Ge^{4+} as well as Si^0 and Si^{4+} as the only oxidation states occurring in non-negligible concentrations. Although XPS might not detect the oxidation states around the interface due to their low fraction of the overall examined volume, this result shows that the Ge in the oxide should be predominantly in the form of GeO_2 or in the form of elemental clusters.

4.3.5. *Summary*

The sum of investigations thus shows that the examined Ge/SiO_2 interface is atomically flat (no steps) and unprecedented chemically sharp, with one layer of Si^{2+} as the only intermediate oxidation state. This is a strong improvement over common Si/SiO_2 interfaces, which in the best case [6] have at least two interface layers and display a mix of all intermediate oxidation states, which can serve as traps for charge carriers and contribute to mobility degradation [89].

The experimental results and modeling also suggest the presence of small amounts of Ge in the oxide, which might be the major cause of the enhanced charge trapping in SiGe/oxide systems reported in the literature [109]. An appropriate choice of etch/re-deposition steps could remedy this problem, enabling the manufacture of Ge-based devices with perfect interfaces to the oxide.

4.4. Si/HfO$_2$ Interface

As pointed out in (2.5), a number of materials are currently under consideration to replace SiO$_2$ and SiO$_x$N$_y$ as a key component of Si-based integrated-circuit technology: the gate dielectric for the transistor. Selecting new high-κ gate dielectric materials systems requires the consideration of many properties. Here, the interface quality issue is addressed concerning the particular system of Si/HfO$_2$.

Two samples provided by "Motorola, Inc" were investigated. Both samples were produced by Hf atomic layer deposition and subsequent oxidation in a low oxygen atmosphere. The SiO$_2$ buffer layer of about 5Å was formed on the Si substrate prior to Hf deposition. One sample, which is identified here as the test sample, was subjected to the additional heat treatment of the Si substrate with SiO$_2$ buffer layer before Hf deposition. This led to the significant improvement of electrical properties of the resultant Si/HfO$_2$ interface, compared to the control sample (prepared without additional heat treatment).

The elemental profile of the control and test samples was compared to the elemental profile of another set of samples with a Si/HfO$_2$ interface provided by the group of Prof. Robert J. Nemanich (NC State University). The initial procedure for their production was the same as for the control sample (with varying SiO$_2$ buffer layer thickness). However, plasma oxidation was performed to produce final the HfO$_2$ layer.

Unlike the systems discussed in the previous sections, in the case of the Si/HfO$_2$ interface, the cross-section [110] samples for Z-contrast and EELS measurements were prepared by the cleavage technique. While limited in applicability to crystalline samples only, this technique introduces a lesser amount of artifacts and material damage than the

traditional preparation technique. It also provides practically uniform thickness of the sample within the scanned area, thus simplifying the analysis of Z-contrast imaging and EELS.

4.4.1. Z-contrast Imaging

Figure 34 shows Z-contrast images of the Si/HfO$_2$ interface from both the control and the test samples. The Hf region effectively has larger average Z number than Si and therefore appears brighter in the Z-contrast image. The intensity profile for the test sample is slightly wider in the Hf region, which might indicate a deviation in the Hf deposition or oxidation processes.

Both samples demonstrate an amorphous region between crystalline Si substrate and the HfO$_2$ film. The composition of this region is to be clarified by EELS analysis.
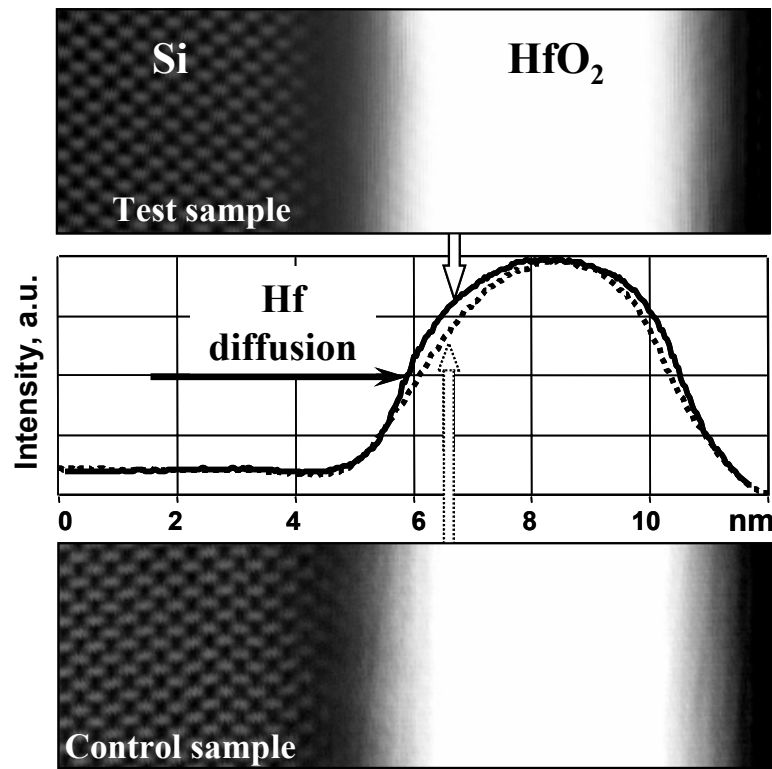
Figure 34. Z-contrast images of Si substrate with HfO$_2$ film and corresponding intensity profile.

In terms of interface roughness, the significant difference was found between the control and the test sample. As demonstrated in Figure 35, a considerable number of atomic plane steps were observed at the interface of the control sample (see about steps in 2.2). At the same time the Si/HfO$_2$ interface of the test sample turned out to be atomically flat.
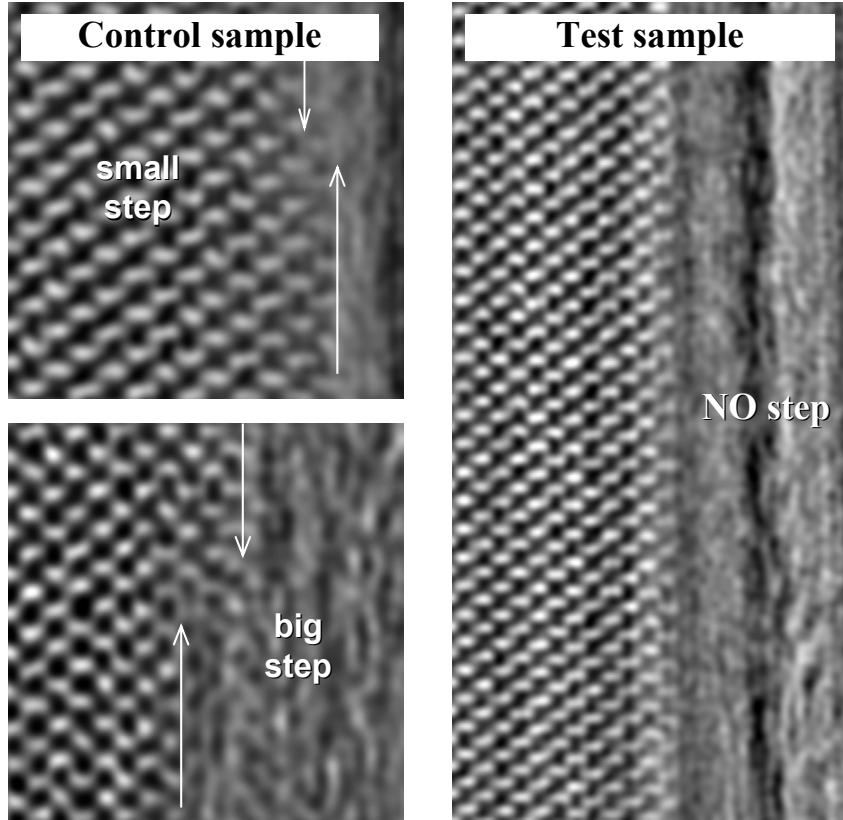
Figure 35. Z-contrast images (Fourier filtered) of the control and the test samples showing different roughness of the Si/HfO$_2$ interface.

Both the control and the test sample showed partial re-crystallization of the HfO$_2$ film. This is clearly shown in Figure 36. The orientation and lattice type of the HfO$_2$ are different from those of Si. Thus, the HfO$_2$ lattice is not completely distinguished in Z-contrast images, where the orientation corresponds to the Si zone axis [110]. The presence of an amorphous transitional layer between the Si substrate and the HfO$_2$ film was also observed for all

samples from another set (i.e. from Nemanich group). The width of this layer correlated but exceeded the width of the SiO_2 buffer layer produced before Hf deposition.
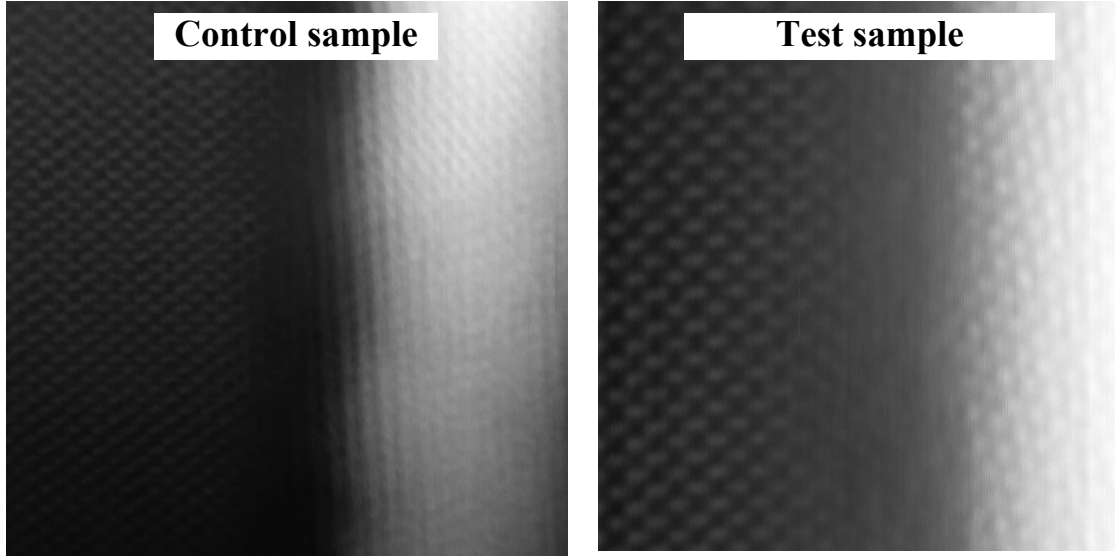
Figure 36. Z-contrast images of control and test samples showing crystallization of the HfO_2 film.
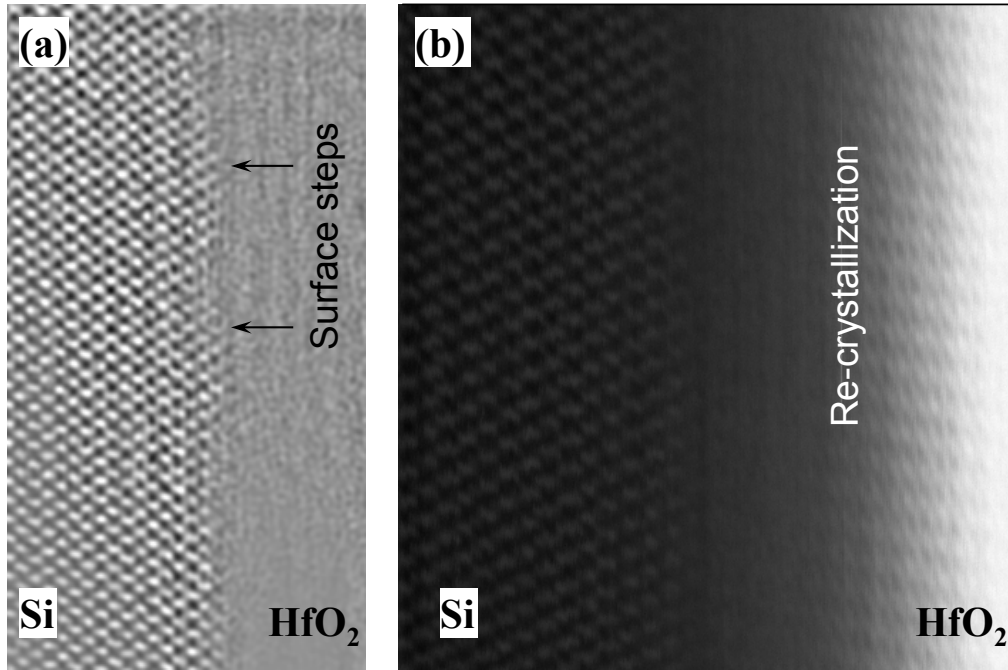
Figure 37. Z-contrast images of the Si/HfO_2 interface from Nemanich group samples, showing (a) steps on the Si surface, and (b) re-crystallization of the HfO_2 film.

All samples from that set (Nemanich group) also showed significant roughness of the Si surface [Figure 37 (a)] as in the case of control sample, and partial re-crystallization of the HfO_2 film [Figure 37 (b)] even of samples that were not annealed.

4.4.2. EELS

Figure 38 shows the spatial distribution of the Si-$L_{2,3}$ edge shape across the Si/HfO_2 interface in the control sample. It is seen that the amorphous region between the Si substrate and the HfO_2 film contains non-oxidized Si and/or only partially oxidized Si. At the same time, going from the Si towards the HfO_2 film, the corresponding Z-contrast image demonstrates a persistent increase of intensity over the amorphous region. The signature of Si^{4+} appears in the Si-$L_{2,3}$ ionization edge almost 1 nm from the last crystalline layer of Si. Then on the HfO_2 side within 2-3 Å, the concentration of Si drops below detection limits showing no trace of the Si edge in EELS.
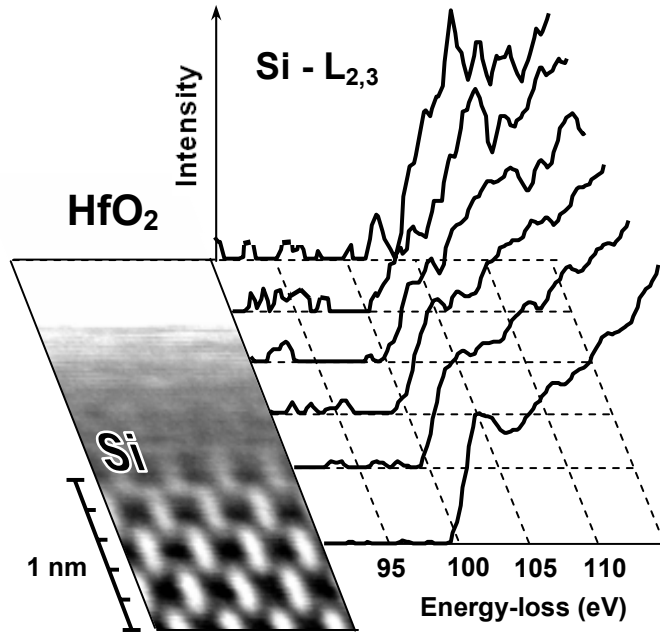
Figure 38. Line-scan EELS of the Si-$L_{2,3}$ ionization edge across the Si/HfO_2 interface of the control sample.

The spatial distribution of the Si-$L_{2,3}$ edge shape across the Si/HfO$_2$ interface in the test sample has the same as the control sample. However, the signature of Si^{4+} appears in the Si-$L_{2,3}$ ionization edge approximately 2 Å closer to the last crystalline layer of Si in the case of the test sample.

The above results are different from what was observed on samples by the Nemanich group. As was mentioned, all of them contained an amorphous transitional layer between the Si substrate and HfO$_2$. However, the signal of oxidized or partially oxidized Si is recorded everywhere in this layer and no presence of amorphous non-oxidized Si was detected.

Figure 39. Line-scan EELS of the Si-$L_{2,3}$ ionization edge across the Si/HfO$_2$ interface of the sample with a 2.4 nm SiO$_2$ buffer layer (sample from Nemanich group)

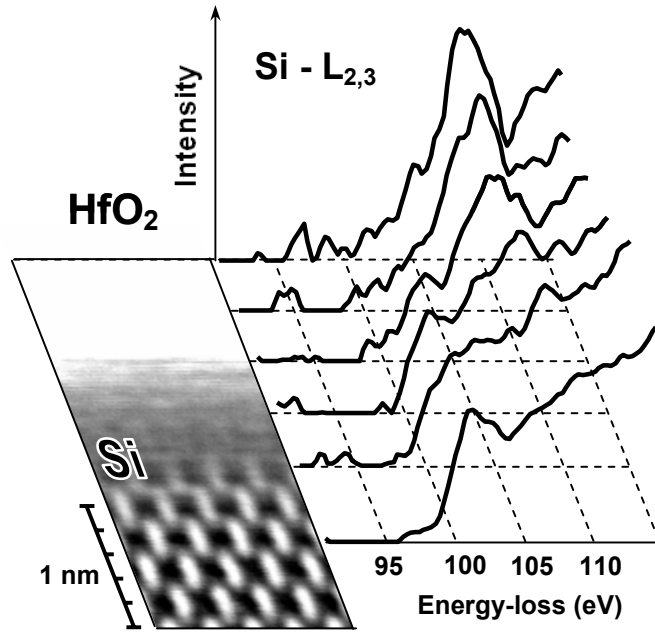Typical results are demonstrated in Figure 39, showing the line-scan EELS of the Si-$L_{2,3}$ ionization edge across the Si/HfO$_2$ interface of the sample prepared with a 2.4 nm SiO$_2$ buffer layer and not annealed. The signature of Si^{4+} appears immediately after the last crystalline Si layer, and, in fact, the presence of oxidized silicon is detected in the transitional

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layer (between Si substrate and HfO$_2$ film) at least 0.5 nm wider than the initial SiO$_2$ buffer layer. The width of the area containing oxidized or partially oxidized Si exceeded the width of the initial SiO$_2$ buffer layer for all samples in that set.

4.4.3. Discussion

The Z-contrast images from both the control and test sample show a region where amorphous Si (non-oxidized as shown by EELS) is present. Since the Z-contrast imaging shows an increase of intensity over this region towards HfO$_2$ film, this region apparently consists of Hf$_x$Si$_{1-x}$. So far, the presence of such a layer, preceding HfSi$_x$O$_y$ (where the signature of oxidized Si is observed in EELS), is not reported in the literature. The observation in this study of a Hf$_x$Si$_{1-x}$ layer at the Si/HfO$_2$ interface might be stipulated by the use of the cleavage preparation technique, which does not introduce artificial oxidation of the sample as it is the case for ion milling [70].

The analysis of both the control and test samples and comparison to another set of samples provided the remarkable observation that oxidation in a low oxygen atmosphere of an Hf film on a Si substrate with a SiO$_2$ buffer layer apparently eliminates the SiO$_2$ buffer layer, leaving an amorphous Hf$_x$Si$_{1-x}$ interlayer between Si and HfO$_2$. Since another set of samples produced by plasma oxidation (i.e. different oxygen conditions) showed rather the opposite effect of an increase of the area containing oxidized Si, it is even more reasonable to attribute the reduction of the SiO$_2$ buffer layer to the low oxygen partial pressure. This is different from the phenomenon described in [59], when Hf silicate film acts as a barrier to the oxidation of the Si substrate and, if no buffer layer used, then SiO$_2$ formation occurs.

The EELS data also suggest that the heat treatment effectively reduced the amorphous Hf$_x$Si$_{1-x}$ interlayer between Si and HfO$_2$. This seemed to be primarily caused by the

improvement of the interface between the Si substrate and the SiO_2 buffer layer, due to eliminating atomic steps on the Si surface (as might be deduced from Figure 35) and associating with them dangling bonds. Thus, better interface quality is apparently the reason for a significant improvement of electrical properties of the test sample interface.

At the same time, there is still a problem with crystallization of HfO_2 films (as demonstrated for both samples in Figure 36) under the processing temperatures of 600°C and above; grain boundaries, associated with crystallization, may serve as the high leakage paths.

This study also suggests that the use of the cleavage technique for samples preparation allows the observation of unique features of the materials (such as the transitional Hf_xSi_{1-x} layer), which might be obscured by other preparation techniques due to their intrinsic imperfections.

4.4.4. Summary

Summarizing the results of these investigations, it may be concluded that the quality of the Si/HfO_2 interface is enhanced by heat treatment, reducing the frequency of atomic steps and associated dangling bonds. At the same time, even after the heat treatment, this interface is not chemically sharp and transition from Si to HfO_2 occurs through a number of intermediate layers. Some of them, however, may act as a barrier for the interdiffusion, playing a positive role for interface stability. The elemental profile across the Si/HfO_2 interface (the increase or reduction of intermediate or transitional layers) may be controlled by the variation of oxygen partial pressure during the oxidation stage. This feature might be used so that the SiO_2 layer can be reduced without leaving amorphous silicon behind, but resulting in a direct Si/HfO_2 interface.

4.5. Si/Al$_2$O$_3$ Interface

The quality of the interface between Si and Al$_2$O$_3$, which is another candidate for an alternative high-κ dielectric, is addressed in this section. Samples provided by the group of Prof. Gerald Lucovsky (NC State University) were investigated. The Al$_2$O$_3$ films were produced by plasma assisted chemical vapor deposition on H-terminated Si substrate. The SiO$_2$ buffer layer of 9Å was formed on the Si substrate prior to Al$_2$O$_3$ deposition. Post-deposition heat treatment at elevated temperatures (about 900° C) was applied. Fixed positive charges were detected at the interface of resultant samples.

All the cross-section [110] samples for Z-contrast imaging and EELS measurements were prepared by standard mechanical polishing and ion milling [70].

4.5.1. Z-contrast Imaging
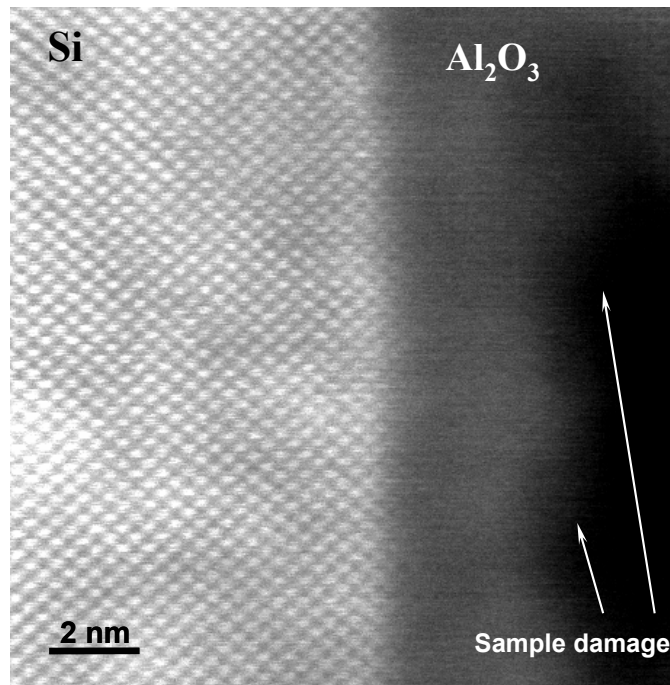
Figure 40. Z-contrast images of Si substrate with Al$_2$O$_3$ film.

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The sample studied was very sensitive to electron-beam damage. The electron probe, fixed for a quite short time (several seconds) on a certain spot at the Al_2O_3 side, caused an inevitable material destruction as denoted on Figure 40, which shows Z-contrast images of the interface between crystalline Si and amorphous Al_2O_3. The Si/Al_2O_3 interface appears to be straight and atomically flat. The waviness of the interface in the Z-contrast image in Figure 40 is attributed to sample drift. However, the elemental sensitivity of Z-contrast imaging is not sufficient in this case and the change of chemical composition across (and maybe along) the interface has to be clarified by EELS.

4.5.2. EELS
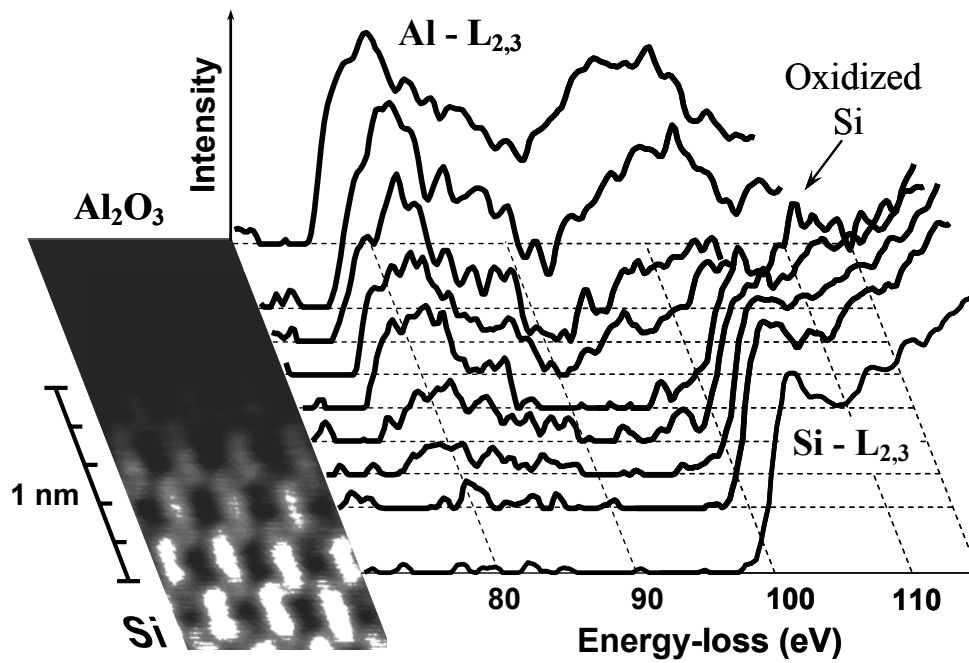
Figure 41. Line-scan EELS of the Si- and Al-$L_{2,3}$ ionization edge across the Si/Al_2O_3 interface.

In the course of experiments, 25 EELS line-scans across the Si/Al_2O_3 interface (at different parts of the sample) were performed. Approximately 85% of them demonstrated

behavior expected for the transition from Si to Al_2O_3. Typical results from this set of EELS line-scans is depicted in Figure 41, which shows the spatial distribution of the Si-$L_{2,3}$ and Al-$L_{2,3}$ edge shapes across the Si/Al_2O_3 interface.

The main features of this distribution are the following. First of all, the crystalline part of the interface is made predominantly of Si (as shown by the Si-$L_{2,3}$ edge). The presence of Al is also detected in the crystalline part (3-4 atomic layers from the amorphous region), suggesting diffusion of Al into the Si substrate. Second, the oxidized Si atoms are present only in the very narrow region (about 1.5 Å) directly at the transition region from the crystalline to the amorphous part. The signal of stoichiometric Al_2O_3 appears on the amorphous side approximately 5 Å away from the crystalline region.

Surprisingly, the EELS line-scans of another type were also recorded (15% out of the total number). Those line-scans demonstrated features typical for the thermally grown Si/SiO_2 interface (see Figure 31) and showed no presence of Al or Al_2O_3 in the substrate or in the amorphous side within 2-3 nm from the interface. This finding suggested the acquisition of an EELS line-scan along the Si/Al_2O_3 interface to search for the variations of the Al-$L_{2,3}$ edge intensity. The results of this line-scan and subsequent processing are summarized in Figure 42.

The spectra for this type of line-scan were recorded with a spatial step of about 4 nm along the interface (as schematically shown in Figure 42). In other words, each individual spectrum was recorded while the electron probe scanned a rectangular area of the sample with a width of 4 nm. The intensities of the recorded Al-$L_{2,3}$ edges varied significantly (from strong and pronounced to barely detectable, close to the noise level). The area under each individual spectrum was calculated and plotted as a function of position along the interface.

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As mentioned in section (3.3), the area under the ionization edge of a specific element directly relates to this element's concentration in the specimen. Thus, the obtained plot (the area under the Al-$L_{2,3}$ ionization edge versus distance), within the accuracy of a scaling factor, corresponds to the Al concentration profile along the Si/Al_2O_3 interface.
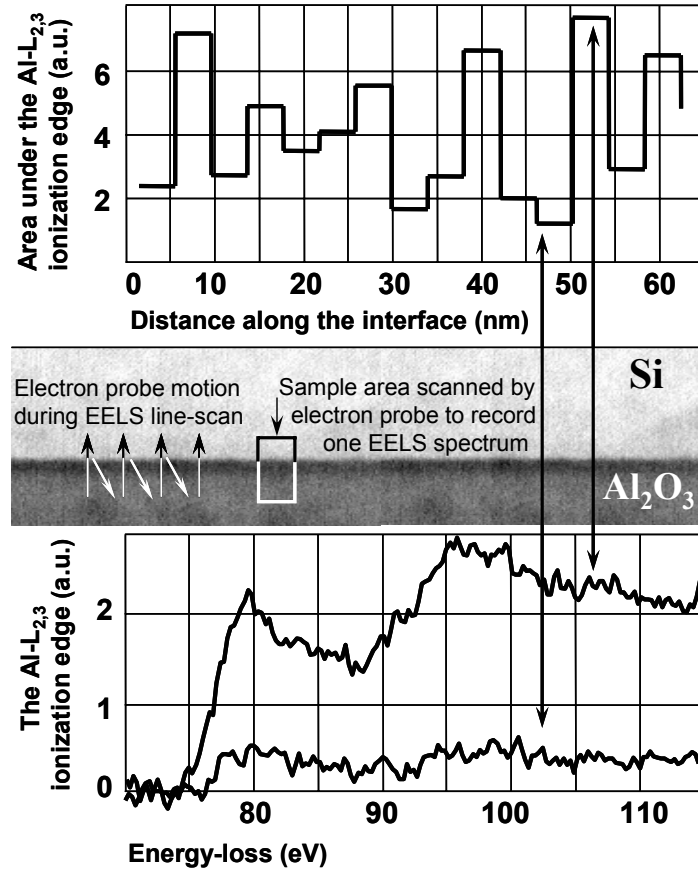
Figure 42. Results of the line-scan along the Si/Al_2O_3 interface.

4.5.3. Discussion

For those regions where a "normal" transition from Si to Al_2O_3 is observed, the Z-contrast images and the EELS data provide the following information. The presence of stoichiometric Al_2O_3 just 5 Å away from the last crystalline layer suggests that, from the atomic configuration point of view (i.e. crystalline structure – amorphous region relationship)

the Si/Al$_2$O$_3$ interface is rather abrupt and comparable to the Si/SiO$_2$ interface. At the same time, the compositional change occurs over the wider range (additional 5-10 Å) mostly because of interdiffusion of Al and Si. Penetration of Al into the substrate is undesirable since this may significantly influence the electrical properties of the interface.

As mentioned in [67], the Al$_2$O$_3$ growth on H-terminated silicon may go through inhomogeneous island nucleation. This is apparently the case for this sample, where areas of preserved SiO$_2$ were observed.

The existence of SiO$_2$ islands on the Si surface (inside the amorphous Al$_2$O$_3$ region) was confirmed directly by an EELS line-scan across the interface (showing transition from Si to SiO$_2$, see Figure 31), and by an EELS line-scan along the interface (showing the variation of Al concentration, see Figure 42). In the latter case, the concentration of Al never dropped below detection limits. This can be explained by the fact that scanning and simultaneous EELS recording was performed at low magnification, i.e. over a wide area (as shown in Figure 42), and those regions scanned by the beam to take each EELS spectrum exceeded the size of a single SiO$_2$ island. Moreover, the line-scan along the interface was performed at a rather thick site of the sample (about 10 nm deep) and any SiO$_2$ island (whose size is estimated as 4-5 nm) on the surface of the sample could be followed by an Al$_2$O$_3$ region a few nm below, thus showing the presence of Al everywhere in the line-scan. Knowing the existence of SiO$_2$ islands on the Si surface, it is reasonable to assume now that the positive charge detected at the Si/Al$_2$O$_3$ interface of the studied sample is localized at the interfaces between SiO$_2$ islands and the Al$_2$O$_3$ matrix.

4.5.4. Summary

The results for the Si/Al$_2$O$_3$ sample studied here thus suggest that, locally, the Si/Al$_2$O$_3$ interface can demonstrate high abruptness and "fast transition" towards stoichiometric Al$_2$O$_3$. However, the chosen method of production (CVD on H-terminated Si surface) has some critical issues with Al$_2$O$_3$ layer non-homogeneity (in a large scale) along the interface and with the interdiffusion of Al and Si. The solution for the uniformity problem may lie in the use of another type of surface preparation for the deposition, for example OH-terminated Si surface, as suggested in literature [67]. Lower thermal budgets and the use of thicker buffer layers for diffusion barriers may prevent Al penetration into the Si substrate.

The non-homogeneity of the Al$_2$O$_3$ layer and SiO$_2$ islands may be the cause of a fixed positive charge observed at the Si/Al$_2$O$_3$ interface and, in general, this leads to the degradation of the electrical properties of the interface (for the purpose of gate dielectrics). At the same time, those islands formation and their possible "self-organization" on the surface of a semiconductor may find an application in a new generation of nano-devices, for which the existence of a fixed charge at a specific place might be beneficial for patterning.

5. CONCLUSIONS

Starting from the natural desire for comfortable life conditions at the level of an individual human being and finishing with the global concepts of economic competitiveness, one can invent a numerous number of reasons to explain the fact of today's demands for (opto-)electronic devices with greater and faster functionality and performance at lower cost. No matter what the real reason is, today's semiconductor industry has to introduce new materials systems with enhanced properties while continuing to downscale and shrink the dimensions of a single active device (e.g. transistor) in integrated circuits.

An essential part of new materials introduction is the need for characterization of structure-proprieties relationships of interfaces between those new materials. As a bench mark for the properties of interfaces in materials systems, it is quite reasonable to use the results obtained from the Si/SiO_2 interface since the extraordinary properties of this interface enabled the development of Si based technology and the growth of the semiconductor industry for almost half of a century.

The characterization of structure-proprieties relationships of interfaces at the current and future level of nanoscale devices requires atomic precision. As demonstrated in the present study, not a single tool but a comprehensive approach should be used to achieve such a precision in characterization. It is shown that the combination of Z-contrast imaging, electron energy-loss spectroscopy and density functional theory provides the required atomic (or close to atomic) resolution, especially with the usage of an aberration corrector for scanning transmission electron microscopes.

The application of said combination of the experimental and theoretical methods to the interfaces studied here revealed and/or confirmed the following. The interface between Si

and GaAs film produced by MOCVD is a semi-coherent and chemically diffused (graded), i.e. as a result of interdiffusion, the compositional change from Si to GaAs takes about 2 unit cells. Lattice mismatch between Si and GaAs is accommodated by the creation of misfit dislocations. Among those just recently observed, the non-reconstructed 90° dislocation contains dangling bonds. As a result, it is electrically active (introducing states in the bandgap) and thus is detrimental to the electrical and optical properties of the Si/GaAs interface. To improve the properties of this interface the segregation to the non-reconstructed 90° dislocation core is suggested. This requires further modeling to find an element suitable for passivation. A more radical solution, though, would be the use of a virtual substrate (on Si substrate) made of material such as Ge with a lesser mismatch to GaAs.

The use of Ge for that purpose is quite promising since Ge films produced by ion implantation and subsequent oxidation can form a coherent (without steps, dislocations and dangling bonds) interface with Si. Although the Si/Ge interface is also graded and transition from Si to Ge takes about 1.5-2 nm, probably the main imperfection degrading the electrical properties of this interface is constituted by stacking faults produced as a result of ion implantation. However, an appropriate change in the ion implantation procedure may eliminate this problem leaving intact all the advantages of Si/Ge interfaces and SiGe heterostructures, such as improvement of charge carrier mobility and the possibility of band structure engineering.

The successful incorporation of Ge into the Si technology sounds even more accomplishable due to the here discovered possibility to produce an atomically flat and an unprecedented chemically abrupt Ge/SiO$_2$ interface, thus providing an excellent insulating and protecting material for Ge as a semiconductor. Surprisingly, the atomic arrangement at

the Ge/SiO$_2$ interface is possibly so abrupt that it might surpass even the quality of Si/SiO$_2$ interface where SiO$_2$ is a "natural" oxide. At the same time, the electrical characteristics of the Ge/SiO$_2$ interface, mainly the enhanced charge trapping, are yet to be improved. The major cause of the enhanced charge trapping in Ge/oxide systems is suggested to be the presence of small amounts of Ge in the oxide. This presence of Ge in the oxide is predicted theoretically and confirmed experimentally. Knowing the cause, one can search for the remedy, which in this case should be a number of appropriate etch/re-deposition steps. Progresses in that direction may enable the manufacture of Ge-based devices with perfect interfaces to the oxide.

As another direction in research for further development of semiconductor devices, the search for substitutional high-κ dielectrics has brought some positive results. Although the interface between Si and HfO$_2$ is chemically not as sharp as the Si/SiO$_2$ interface and there are transitional layers (with oxidized and some time amorphous Si) that lower the total dielectric permittivity of resultant insulating layer, it is shown that the quality of the Si/HfO$_2$ interface may be enhanced by the heat treatment, reducing the atomic steps and associated dangling bonds. Moreover, the variation of oxygen partial pressure during the Hf oxidation stage is suggested for control of the width of transitional layers so that, in principle, they can be completely reduced, resulting in a direct Si/HfO$_2$ interface with a high-κ dielectric side. The re-crystallization of the HfO$_2$ layer so far is seem to be unavoidable, but apparently it poses no significant problem since the use of HfO$_2$ films for next generations of memory chips has been announced by several semiconductor companies.

The Al$_2$O$_3$ is another promising candidate for high-κ dielectrics. The interface between Si and Al$_2$O$_3$ can demonstrate high abruptness and "fast" Al$_2$O$_3$ stoichiometry, comparable to

the Si/SiO$_2$ interface. Problems associated with large scale non-homogeneity along the Si/Al$_2$O$_3$ interface and the interdiffusion of Al and Si potentially can be fixed by the appropriate surface preparation (OH-terminated Si) and lowering the thermal budget (below 900° C). The formation of SiO$_2$ islands and the associated fixed charges inside the Al$_2$O$_3$ layer, though undesirable for the purpose of the gate dielectric, may be beneficial for the design of new nano-devices requiring charge localization.

In summation, the results obtained in this study suggest that reliable information about the structure-properties relationships in the materials systems considered (Si/GaAs, Si/Ge, Ge/SiO$_2$, Si/HfO$_2$, Si/Al$_2$O$_3$) is the key for successful application of these materials in the future semiconductor devices. The atomic and electronic structure characterization of interfaces in materials systems provides not only the knowledge of their essential properties but also the directions for their further improvements.

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