ABSTRACT

GAO, YAN. Analysis and Optimization of 1200V Silicon Carbide Bipolar Junction Transistor. (Under the direction of Dr. Alex Q. Huang.)

This research focuses on the modeling, design, optimization and characterization of Silicon Carbide bipolar junction transistor (SiC BJT). A two-dimensional numerical device simulator ISETCAD is used to model, design and optimize the SiC BJT’s cell structure. A base resistance model has been developed for the SiC BJT and the model is used to evaluate the layout of the real SiC BJTs. A number of important SiC BJT characteristics that are different from Si BJT, such as the current gain, conductivity modulation, emitter size effect and the difference between $BV_{CEO}$ and $BV_{CBO}$ are investigated theoretically and experimentally. The dynamic characteristics section mainly focuses on the comparison of SiC BJT power loss versus popular Si power devices like Si IGBT. The small energy loss and a square reverse biased safe operation area (RBSOA) of the SiC BJT are theoretically and experimentally demonstrated, along with an analysis of SiC switching characteristics. Short-circuit capability has been investigated for the SiC BJT. The unique SiC BJT operational degradation issue is investigated through a series of experiments and possible degradation mechanisms are identified. The Ph.D research also includes the design and fabrication of a monolithic solution of SiC BJT and SiC rectifier for the first time. The characterization of the BJT/rectifier device is given in this dissertation. This novel device will help the system to reduce the size, cost and increase the reliability. Based on the BJT structure, some novel device structures are also proposed in this work. Simulation study results have shown that these devices are very promising to further improve the performance of SiC BJTs.
Analysis and Optimization of 1200V Silicon Carbide Bipolar Junction Transistor

by
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BIOGRAPHY

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Yan Gao’s interests lie in the modeling and design of devices and circuits for power system.
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Chapter 1 Introduction

There are significant needs for more efficient, higher voltage power semiconductor devices. Application needs range from more efficient power supplies for computers and consumer appliances to electric automobile power converters, and more efficient long distance high voltage power transmission. The constant development of power semiconductor devices has always been a major factor facilitating these applications and the development of new applications.

Over the last five decades, silicon (Si) has been the dominant material used for power semiconductor devices due to well controlled material property and matured device fabrication process technology. Today, Si is still the dominating material in the field of power devices. However, it is now widely recognized that silicon power-switching devices are reaching their theoretical limits of performance, as established by fundamental material parameters like the critical field for avalanche breakdown. The power transistors for 600 V and above based on Si have either a relatively high specific on resistance or significant switching power losses, which both result in high power dissipation. In addition, the maximum allowed operating temperature of Si power devices is typically 125 °C, which cannot satisfy the demand of an increasingly dense power electronics system design, such as the traction inverter used in electric vehicle.

In recent years, wider band gap semiconductors have gained remarkable attention as the need for new power device materials grows due to limited Si material properties and the increasing power densities of power electronic systems. Silicon carbide is a wide band
gap semiconductor that possesses extremely high thermal, chemical, and mechanical stability. SiC has the advantage of high thermal conductivity, high breakdown electric field, and saturated carrier velocity compared to other semiconductor materials, which makes it an ideal material for power devices. The commercial availability of single-crystal SiC wafers in the early 1990s led to a resurgence of activity in the development of SiC electronic devices. SiC power devices can now be fabricated with high quality material compared to other possible wide bandgap materials. Four-inch diameter SiC wafers were recently introduced to the market for commercial applications.

Due to the development of better and better SiC materials, remarkable progress has been made in SiC power devices in recent years. Over the past decade, many of the optimistic attributes of SiC power devices have been experimentally demonstrated and confirmed. Many high power SiC devices, such as diodes, transistors and thyristors have been demonstrated and SiC Schottky diodes for 600 V and 1200 V are now commercially available [3,5]. When these devices are used in a system, the low on resistance, high temperature sustaining and fast switching abilities will allow the system to work under higher frequencies, resulting in the passive components shrinking and offering an attractive cost savings. Some of the most promising applications with high demands on power density or operating temperature are hybrid electric vehicles, motor drives and power converters.

Among the SiC power devices, SiC JFET and MOSFET are unipolar devices. In order to obtain a reasonable on-state resistance, SiC Junction Field Effect Transistor (JFET) is usually designed as a normally-on device. This greatly limits the application of this
device due to the complex driver design. SiCED GmBH (a spin-off from Infineon) proposed a solution of SiC JFET in series with a Si MOSFET to make the module normally off [6,7]. But this configuration cannot work in very high temperature due to the Si limitation, thus limiting the advantage of SiC devices.

MOSFET is a very popular Si power switch due to its simple gate drive interface and good static and dynamic performances. Similarly, SiC MOSFET also attracts a lot of attentions [8,9,10,11]. However, due to the immature fabrication process of SiC/SiO$_2$ structure, the SiC MOSFET performance still suffers from the low effective channel mobility, which limits the on state performance of SiC MOSFETs. The SiC MOS structure may operate reliably at temperatures up to 200 ºC which is beyond the range of Si switches, however some major gate dielectric reliability issues may keep this device from being used at the extreme temperatures required by many applications [12].

Since the forward drop of a power unipolar device increases sharply with blocking voltage, most of the high-voltage high-current applications employ bipolar devices. IGBT, as a bipolar device, is widely used in converter application. However, for an IGBT, the forward voltage drop cannot be reduced below the one diode on-state drop. Since SiC has a much larger diode turn-on voltage due to its bandgap, SiC IGBT’s conduction loss exceeds silicon IGBT for low blocking voltages [13,14,15]. For this reason, the SiC-IGBT is viable option for applications that require a high breakdown voltage of 5kV and more. Other challenges faced by IGBT include the lack of highly conductive p-type substrates [14].

3
As a bipolar device, conductivity modulation will help to reduce the forward voltage drop. Compared to other bipolar devices, like IGBT and GTO, BJT does not have the junction voltage needed to overcome in order to conduct current. Also, the process complexity is reduced greatly as compared to SiC MOSFETs, rendering the SiC Bipolar Junction Transistor (BJT) a promising high power switching device. Although considerable progress has been made in recent years [16,17,18], challenges that could potentially prevent this device from reaching its full potential still exist. For example, the low common emitter current gain is one of the major technical challenges to the application of SiC BJT. The improvement of the current gain of SiC BJTs is complex since it depends on several parameters including the thicknesses and doping levels of the base and emitter layers, the material quality, and the surface passivation. The goal of this research is to improve the performance of 4H-SiC BJT with the complete study and analysis of 4H-SiC BJT using modeling and experiments. The basic operating principle, the operating limit, and the effect of both process and layout parameters will be analyzed in detail.

1.1 Background

In this section, the basic material properties and advantages of SiC are described. SiC as a wide band gap semiconductor material has a high critical field and a high thermal conductivity, making it an excellent material for high power, high temperature, and high frequency power applications.
1.1.1 Crystal Structures and Polytypes

SiC consists of Si and C atoms, which are both group IV element materials. Each Si atom shares electrons with four C atoms, which means that each atom is bonded covalently to four neighbors, and vice versa. The basic structural unit is shown in Figure 1.1. The approximate bond length between Si and C atoms is 1.89 Å and the length between Si-Si or C-C atoms is 3.08 Å.

Figure 1.1 The basic structural unit in SiC [19].
SiC embodies a characteristic known as a polytypism which means that the material can possess more than one crystal structure. Each crystal structure is called a polytype. The different polytypes are defined by their stacking sequence. The different stacking sequences for 3C, 4H, and 6H in SiC are illustrated in Figure 1.2.

1.2 Physical and Electrical Properties

SiC has a high critical field of about $2 \cdot 10^6$ V/cm, a high thermal conductivity of 3-4 W/cm.K, and a high saturated carrier velocity of $2 \cdot 10^7$ cm/s. These properties make SiC devices good candidates for high power, high temperature, and high frequency applications. The physical properties of SiC and other semiconductor materials are compared in Table 1.1.
Table 1.1 Electrical property of SiC and other semiconductors

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>GaN</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap, $E_g$ (eV at 300K)</td>
<td>1.12</td>
<td>1.43</td>
<td>3.4</td>
<td>2.4</td>
<td>3.0</td>
<td>3.2</td>
</tr>
<tr>
<td>Critical field, $E_c$ (V/cm)</td>
<td>$2.5 \times 10^5$</td>
<td>$3 \times 10^5$</td>
<td>$3 \times 10^6$</td>
<td>$2 \times 10^6$</td>
<td>$2.5 \times 10^6$</td>
<td>$2.2 \times 10^6$</td>
</tr>
<tr>
<td>Thermal conductivity, $\lambda$ (W/cmK at 300K)</td>
<td>1.5</td>
<td>0.5</td>
<td>1.3</td>
<td>3-4</td>
<td>3-4</td>
<td>3-4</td>
</tr>
<tr>
<td>Saturated electron drift velocity, $V_{sat}$ (cm/s)</td>
<td>$1 \times 10^7$</td>
<td>$1 \times 10^7$</td>
<td>$2.5 \times 10^7$</td>
<td>$2.5 \times 10^7$</td>
<td>$2 \times 10^7$</td>
<td>$2 \times 10^7$</td>
</tr>
<tr>
<td>Electron mobility, $\mu_n$ (cm²/V.s)</td>
<td>1350</td>
<td>8500</td>
<td>1000</td>
<td>1000</td>
<td>500</td>
<td>950</td>
</tr>
<tr>
<td>Hole mobility, $\mu_p$ (cm²/V.s)</td>
<td>480</td>
<td>400</td>
<td>30</td>
<td>40</td>
<td>80</td>
<td>120</td>
</tr>
<tr>
<td>Dielectric constant, $\epsilon_r$</td>
<td>11.9</td>
<td>13.0</td>
<td>9.5</td>
<td>9.7</td>
<td>10.0</td>
<td>10.0</td>
</tr>
</tbody>
</table>

1.2.1 Wide Energy Bandgap

Electronic devices using SiC can operate at extremely high temperatures without suffering from intrinsic conduction effects because of the wide energy bandgap.

1.2.2 High Breakdown Electric Field

SiC can withstand a voltage gradient (or electric field) more than eight times greater than that in Si or GaAs without undergoing avalanche breakdown. This high breakdown electric field enables the fabrication of very high-voltage, high-power devices such as diodes, power transistors, power thyristors and surge suppressors, as well as high power microwave devices. Additionally, it allows the devices to be placed very close together, providing high device packing density for integrated circuits.
From Table 1.1, SiC has a high critical field \( E_c \) of about 2 MV/cm. This value is about 10 times higher than that of Si. Considering the parallel-plane and abrupt N+/P junction, the relationship between critical electrical field and the breakdown voltage is given in Eqn. (1.1)

\[
V_B = \frac{E_c W}{2} \tag{1.1}
\]

Where \( V_B \) is breakdown voltage, \( E_c \) and \( W \) are the critical field and the width of the drift region, respectively. So, to realize the same breakdown voltage, SiC device needs a much thinner drift length due to the high \( E_c \).

Assuming the current flows through the drift region uniformly without current spreading effects, the ideal specific on-resistance of the drift region is in Eqn.(1.2)

\[
R_{on-sp} = \frac{W}{N\epsilon\mu} = \frac{4V_B^2}{\epsilon\mu E_c^3} \tag{1.2}
\]

To realize the same breakdown voltage, an SiC device will have smaller specific on-resistance due to the high \( E_c \). The \( R_{on-sp} \) comparison between SiC and Si is shown in Figure 1.3. For the same breakdown voltage, the SiC device will have a \( R_{on-sp} \) around 1000 times lower than Si device. That means SiC device will have lower conduction loss for the same breakdown voltage design.
1.3 Improving SiC Technology

SiC devices can also operate at high frequencies (RF and microwave) because of the high saturated electron drift velocity of SiC.

SiC offers superior material properties to meet higher power performance challenges. Continuous power switches, power diodes, and pulsed power switches fabricated from SiC offer reductions in on-state resistance and switching loss over conventional silicon power devices. For a given power rating, these components can operate at a higher duty cycle, leading to a reduction in the size of inductors and transformers in power circuits. SiC power electronics also extend solid state technology by offering higher breakdown voltage levels than current silicon technology, addressing voltage levels now managed by electromechanical switch technology.
As shown in Table 1.2, SiC devices can operate at higher temperatures and thus require less cooling. The higher blocking voltages, as compared to silicon devices, allow for the design of smaller and simpler high voltage components. Improved thermal management of semiconductors and passive components through upgraded packaging would allow more current to be handled by a given device and lead to improved power density designs.

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>4H-SiC</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Band Gap (eV)</td>
<td>1.12</td>
<td>3.26</td>
<td>SiC devices can operate at much higher temperatures</td>
</tr>
<tr>
<td>Electric Breakdown Field (kV/cm)</td>
<td>300</td>
<td>2200</td>
<td>SiC can withstand much larger voltage gradients</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm. °C)</td>
<td>1.5</td>
<td>3-3.8</td>
<td>SiC can efficiently conduct heat away from high power junctions</td>
</tr>
</tbody>
</table>

Power conversion equipment developed using SiC technology is projected to significantly reduce the workload and maintenance requirements for current and future carriers. As an example, use of SiC power conversion on Navy ships is expected to reduce the current conversion equipment size by approximately 60% and achieve weight savings approaching 2.68 tons for each converter implemented with the new 2.7 MVA transformer technology [1].

The major areas of the SiC device development are as follows [2]:

10
1. SiC wafer and substrate fabrication: The key dominating issues here lie in reducing the physical flaws and defect densities in the wafers (such as tubular voids, referred to as micropipes and the overall residual wafer stress), and increasing wafer sizes for more cost effective fabrication. Four inch zero micropipe density SiC wafers are now commercially available [3].

2. SiC physics and device development: This means not only the theoretical design of SiC devices, but also the practical issues associated with layout and manufacturing processes and the building of the devices or ICs. Device engineers mainly focus on this development.

3. SiC dielectrics and Passivation: One of the key steps in making discrete devices capable of withstanding high temperatures is proper device passivation. New materials are needed for use in device fabrication as well as final passivation coatings.

4. SiC device modeling: The ability to develop and validate accurate device models is crucial in today’s world of computer simulations. End users should be able to simulate their circuit and system designs using device models, or they are unlikely to apply the devices themselves. Device engineers mainly focus on this development.

5. SiC packaging: Due to the high temperature operation most conventional packaging technologies are unworkable and new technologies are needed. High temperature brazes or phase change materials are needed to allow for attachment of the SiC die. In addition, conventional power wire bonding based on aluminum must be replaced with a new technology that can withstand the high operating temperatures as well as the high currents found in many of the proposed applications.
6. **SiC applications**: Currently, the most promising applications for SiC are power-electronics systems and drives, RF modules, and simple sensors. The key here is that organizations with access to SiC devices can make great strides in developing applications over those that must work completely from a theoretical perspective.

### 1.4 The Basic Principle of BJT Operation

The bipolar junction transistor (BJT) was invented by John Bardeen, Walter Brattain, and William Shockley at Bell Laboratories in 1947 [4]. Even though the importance of BJT has been challenged by the metal oxide semiconductor based field effect transistor (MOSFET), the BJT still has important applications that combine high power and high speed. The npn BJT is more widely used than the pnp BJT, because the electron mobility is higher than hole mobility.

The bipolar power transistor is fundamentally a current-controlled three-terminal switch. It has common emitter and common base configurations. The common emitter configuration is more prevalent.
The basic principle of operation of the BJT is the control of the collector current by the base emitter voltage. In the forward-active mode, the base-emitter junction is forward biased and the base-collector is reverse biased. The current transport between the emitter and collector for an NPN transistor in the common base configuration is shown in Figure 1.4 with depletion boundaries and the internal current components indicated. The electrons injected from the emitter constitute the current $I_{nE}$. Most injected electrons, which are the minority carriers in base, will reach the collector ($I_{nC}$). Some electrons will recombine with majority carriers holes in base ($I_{RB}$). The majority carrier holes injected from base give rise to $I_{pE}$. Some electrons and holes will also recombine in the space charge region of the forward biased emitter-base junction ($I_R$). Finally, the reverse-saturation current of the base-collector junction is designated as $I_{CO}$. 

Figure 1.4 Internal current components in a NPN bipolar transistor
1.4.1 Common Emitter Current Gain

When the base-emitter junction is forward biased and the base-collector junction is reverse biased, the n-p-n BJT is biased into its active region. The current transport between the emitter and collector for an NPN transistor in the common base configuration is shown in Figure 1.5 with depletion boundaries and the internal current components indicated. The current \( I_{nE} \) is the electron current injected from emitter to the base. The current \( I_{nc} \) is the electron component at base-collector junction.

![Diagram of NPN bipolar transistor with current components](image)

**Figure 1.5 Current components in a NPN bipolar transistor for gain calculation**

Using the current components, the common emitter current gain can be written as:

\[
\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_{nE}}{\Delta I_E} \cdot \frac{\Delta I_{nc}}{\Delta I_C} \cdot \frac{\Delta I_C}{\Delta I_{nc}} \quad (1.3)
\]

The first term refers to as the emitter injection efficiency or gamma \( \gamma \). This is a measurement of the ability of the emitter to inject electrons into the base region in an
efficient manner. The second term refers to base transport factor, $\alpha_T$. This is a measure of the ability for electrons that injected into the base from the emitter to reach the collector-base junction. The third term refers to the collector efficiency. This is a measure of the ability of electrons to transport through the collector region. In the case of a reverse biased collector-base junction, a strong electric field is established within a depletion region at this junction. The electrons transported through the base region are swept out by this electric filed into the collector region. At collector biases well below the avalanche breakdown voltage of the collector-base junction, this process occurs without loss of electrons.

In the case of a power bipolar transistor, it is necessary to consider both the emitter injection efficiency and the base transport factor in analyzing the current gain, because unlike signal transistors the power transistors must be designed with relatively large base thickness to prevent punch-through breakdown.

Now, assuming that the base emitter space charge recombination current $I_R$ can be neglected as is the case if the material quality of the base emitter junction is high, then the emitter injection efficiency $\gamma$, which is the injected electron current from the emitter divided with the total emitter current, is defined by Eqn. (1.4)

$$\gamma = \frac{I_{\text{ne}}}{I_E} \approx 1 + \frac{N_B D_E W_B}{N_E D_B W_E}$$

(1.4)

where $N_B, N_E =$ base and emitter doping concentration (cm$^{-3}$),
$D_B, D_E =$ base and emitter minority carrier diffusion coefficients (cm$^2$/sec),
$W_B, W_E =$ base and emitter region widths (cm)
Eqn. (1.4) holds if \( W_E \) is much smaller than the hole diffusion length \( L_{pE} \) in the emitter. If the opposite is true, then \( W_E \) should be replaced by \( L_{pE} \).

The base transport factor can be obtained:

\[
\alpha_T \approx \frac{1}{\cosh(W_B / L_n)} \tag{1.5}
\]

Assuming the diffusion length is much longer than the base width \( W_B \), the base transport factor can be calculated using the following expression:

\[
\alpha_T \approx 1 - \frac{W_B^2}{2L_n^2} \tag{1.6}
\]

Two important parameters in the characterization of the bipolar transistors are the common base current gain \( \alpha \) and common-emitter current gain \( \beta \). The common-emitter current gain \( \beta \) is defined as the ratio of the collector and base currents as shown in Eqn (1.7).

\[
\beta = \frac{I_C}{I_B} = \frac{\alpha}{1 - \alpha} \tag{1.7}
\]

1.4.2 Breakdown Voltage

There are two mechanisms that can limit the breakdown voltage of bipolar transistors. One phenomenon is called punch-through and it limits the open-base breakdown voltage if the total dose of the base doping is too low. As the reverse bias of the base-collector junction is increased, the base-collector depletion region can extend through the base.
region and reach the base-emitter depletion region. The second breakdown mechanism is the avalanche breakdown process.

(a) Open Emitter Breakdown Voltage $BV_{CBO}$ [20]

When BJT is operated with no connection to the emitter terminal (open emitter configuration) and a positive bias is applied to the collector terminal with respect to the base terminal, the breakdown voltage in this mode is referred to as the open emitter breakdown voltage ($BV_{CBO}$). In this mode of operation, the breakdown voltage of the device is like the breakdown of a p/n- diode breakdown.

(b) Open Base Breakdown Voltage $BV_{CEO}$ [20]

When the BJT is operated with no connection to the base terminal (open base configuration), the breakdown voltage in this mode is referred to as the open base breakdown voltage ($BV_{CEO}$). In this configuration, the leakage current flowing across the base-collector junction must flow across the emitter-base junction. Thus, the leakage current is amplified by the gain of bipolar transistor, resulting in significant enhancement in the leakage current.

The leakage current for an open base transistor is shown in Eqn.(1.8).

$$I_k = I_C = \frac{I_L}{(1-\alpha)}$$  \hspace{1cm} (1.8)
Where $\alpha$ is the common base current gain of the BJT, and $I_L$ is the sum of the space-charge-generation and diffusion current across the base-collector junction. The common base current gain is given by:

$$\alpha = \gamma_{E} \cdot \alpha_{T} \cdot M$$  \hspace{1cm} (1.9)

Where $\gamma_{E}$ is the emitter injection efficiency, $\alpha_{T}$ is the base transport factor, and $M$ is the avalanche multiplication factor. The multiplication factor ($M$) can be empirically related to the collector bias by:

$$M = \frac{1}{\left[1 - (V_{CE} / BV_{CBO})^{n}\right]}$$  \hspace{1cm} (1.10)

From Eqn(1.8), it can also be concluded that the collector current approaches infinity when the common base current gain approaches unity.

Thus the open base breakdown voltage ($BV_{CBO}$) can be obtained from the condition:

$$M(BV_{CEO}) = \frac{1}{\left[1 - (BV_{CEO} / BV_{CBO})^{n}\right]} = \frac{1}{\alpha_{o}}$$  \hspace{1cm} (1.11)

Where $\alpha_{o}$ is the common base current gain at low collector biases where the avalanche multiplication factor is equal to unity. From this equation, it can be shown that:

$$BV_{CEO} = \frac{BV_{CBO}}{(\beta_{o})^{\frac{1}{n}}}$$  \hspace{1cm} (1.12)

Where $\beta_{o}$ is the common emitter current gain at low collector biases when the multiplication factor is unity and $n$ is an empirical constant. Generally, $n$ is between 3 and 6 in silicon [20]. With Si, in general, the common emitter current gain at low current...
levels is large, leading to an open base breakdown voltage that is substantially smaller than the open emitter breakdown voltage.

### 1.4.3 Conductivity Modulation

When both the base-emitter junction and the base-collector junction are forward biased, the n-p-n BJT is biased into its saturation region. During the on-state current flow, as the current density increases, the injected carrier density also increases and ultimately exceeds the relatively low background doping of the N-drift region. When the injected hole density becomes much greater than the background doping, charge neutrality in the N-drift region requires that the concentrations of holes and electrons become equal. These concentrations can become far greater than the background doping level resulting in a large decrease in the resistance of the i-region as shown in Figure 1.6.

![Figure 1.6 Carrier distribution profiles in the base and collector regions of a BJT under conductivity modulation conditions.](image-url)
This phenomenon, called conductivity modulation, is an extremely important effect that allows transport of a high current density through the bipolar device with low on-state voltage drop. Using BJT as a bipolar transistor, the conductivity modulation in the drift region can overcome the large on-state power dissipation in unipolar devices at high blocking voltages due to increased drift layer thickness. So, for silicon, when the voltage rating is above 300V, the bipolar devices are preferred over the unipolar devices in the on-state power dissipation.

1.4.4 Reverse Biased Second Breakdown Characteristics

The current-voltage boundary within which a power bipolar transistor can be operated without destructive failure is defined as its safe-operation-area or SOA. At low current levels this boundary is determined by the onset of avalanche breakdown(BVCEO or BVCEO). At low voltage levels this boundary is determined by the maximum current that the leads can handle without fusing. When the current and voltage are simultaneously large, the device experiences high instantaneous power dissipation. The safe operation of the device is then determined by either a thermal limitation or by an instability - referred to as second breakdown - to distinguish it from the previously discussed avalanche breakdown observed at low current levels.

The second breakdown is particularly important to operation of the bipolar transistor with inductive loads. The typical turn-off waveforms of the BJT under the inductive load are shown in Figure 1.7 and the trajectory is shown in Figure 1.8.
Figure 1.7 Typical turn-off waveforms under inductive load of BJT

Figure 1.8 Turn-off trajectory under inductive load

The over-shoot voltage is due to the presence of a high di/dt across any stray inductance in the circuit during turn-off. During turn-off, the reverse base drive current first extracts base stored charge from the edge of emitter. As a consequence, the emitter current tends to constrict to the center of the emitter finger. In this case, the total current flowing
through the transistor tends to remain constant while the emitter conduction area decreases. The current density at the center of the emitter then increases drastically during the turn-off process. In this case, base widening effect may occur. The peak electric field shifts from BC junction to the drift and substrate n-/n+ junction. Figure 1.9 illustrates this process, the electric field distribution shifting from 1 to 2 then to 3. The slope of distribution 3 is determined by the current density. As the current density increases, the slope increases. Once the peak electric field reaches the critical electric field, breakdown occurs. Due to the current crowding during turn-off, the extremely high current density may lead to the onset of breakdown at voltages well below the designated value. Figure 1.10 shows the typical safe operation area of Si BJT [47]. From Figure 1.10, we see the maximum operation current for this Si BJT is only 6A under the 750V bus voltage. Once the turn-off trajectory touches any point outside this area, the device turn-off will fail. The SOA is hence significantly reduced by the second breakdown. This is one of the major reasons that today’s applications uses power MOSFETs instead of BJT. MOSFETs does not have second breakdown due to its pure unipolar current conduction mechanism.
SiC BJT has the same basic operating principle as Si BJT. However, advances in SiC material make SiC BJT overcome some of the above mentioned limitations imposed by silicon. While SiC unipolar devices are commercially available from multiple vendors [3, 5], this research investigates the current obstacles in improving and optimizing the performance of 4H-SiC bipolar junction transistors.
1.5 Outline of Dissertation

Chapter 2 provides a brief review of the state-of-the-art study of SiC BJT. The main parameters are compared between different studies, and the electrical models of SiC used for the simulation study throughout the dissertation are presented. Cell structure optimization will be discussed based on those models. A base resistance model is proposed and used for the layout design.

Chapter 3 provides the main fabrication steps of SiC BJT. The real fabricated SiC BJT characteristics are also discussed in this chapter. The conductivity modulation in SiC BJT is analyzed, and a thorough comparison of the SiC BJT and the popular Si power device, Si IGBT is presented in this chapter. An analytical analysis of the SiC BJT inductive switching is also presented in this chapter.

In Chapter 4 the square safe operation area of the SiC BJT is demonstrated theoretically and experimentally. The SiC BJT short-circuit capability was demonstrated experimentally. Simulation study shows the theoretical limit of the short-circuit limit factor.

In Chapter 5, the reliability issue - an important issue for the commercialization of SiC BJT - is discussed in this chapter. Two main types of degradation phenomena are provided, and plenty of experimental results are provided, helping to pinpoint causes of degradation. Besal plan dislocation and surface quality are cited as two main reasons for degradation.
In Chapter 6 the monolithic solution of SiC BJT and diode is discussed. The proposed structure, layout, and real fabricated device characteristics are outlined. The proposed solution can help to reduce the peak reverse recovery current, system size, and cost.

In Chapter 7 two types of new structures are proposed. Simulation studies regarding these structures are presented with all structures showing promising characteristics.

Chapter 8 concludes the dissertation, stating the author’s contributions and providing guidelines for future work.
Chapter 2 Modeling and optimization of SiC BJT

2.1 Review of SiC BJTs

The typical cross-section view of a SiC power NPN Bipolar Junction Transistor (BJT) is shown in Figure 2.1. The mobility of electrons is also higher than holes’ hence the on-resistance of NPN transistor (or the saturation voltage $V_{CE(sat)}$) will be lower than the PNP BJT. Additionally, the lack of good quality of p+ substrate makes NPN BJT attracting more attention than PNP BJT.

Generally, two approaches have been used to fabricate NPN SiC-BJTs. One is epitaxial growth of the emitter with a p+ implanted base contact region in the base layer (Figure 2.1 (a)). The other is an n+ implanted emitter region on a base layer after etch removal of the p+ base epitaxial growth (Figure 2.1 (b)).
Today, n+ epitaxial grown structures are preferred because the junction defects at the base and emitter interface generated by implantation are hard to recover completely in the annealing step. To avoid the implantation damage at the injection junction, the epitaxial emitter structure is used as shown in Figure 2.1(a).

The implanted emitter SiC BJT was demonstrated by RPI group with a common emitter current gain of 8 and breakdown voltage 1KV [21]. A 1.8kV, 3.8A epitaxial emitter bipolar junction transistor was demonstrated by S-H Ryu et al. [17]. A maximum current gain of 20 was measured together with a $BV_{CEO}$ of 1800V for devices with an emitter pitch of 23$\mu$m. Recently, A. Agarwal et al. from Cree Inc [22] have demonstrated devices with a blocking voltage of 1600 V with current gains as high as 45 in the active region. The improved current gain was achieved by growing both the base and emitter layers in the same epi reactor and thus improving the base-emitter interface. An epitaxially grown
p+ base contact region instead of implantation has been demonstrated by KTH group with a current gain only 6 [23]. The current gain reduction is presumably caused by a local reduction of the emitter efficiency by the highly doped p+ region and possibly also by a reduction of the carrier lifetime in the very high doping of $N_A=4 \times 10^{20} \text{cm}^{-3}$ [23].

Contrary to the behavior of conventional silicon devices, the current gain of these devices was found to decrease with temperature. The fact that the forward drop increases and the current gain decreases makes this device ideal for paralleling and prevents thermal runaway problems. Another interesting aspect of these devices is that the emitter size effect (ESE) was observed, meaning that current gain was found to decrease with decreasing emitter stripe width. This effect was credited to an increasing ratio of emitter periphery to emitter area of the device and the accompanying enhancement in the surface recombination of minority carriers.

A review of experimentally obtained SiC BJTs results is presented in Figure 2.2 and Table 2.1. The theoretical limit for unipolar SiC power devices is also shown in Figure 2.2. Figure 2.2 clearly demonstrated that the performance of the SiC BJT is better than that of the MOSFET from the on-resistance point of view. This is due to the more uniform bulk current conduction mechanism of the BJT as compared to the surface channel and then vertical current conduction mechanism of the MOSFET.
Figure 2.2 Comparison between demonstrated SiC BJTs and SiC MOSFETs
Table 2.1 Review of SiC BJTs

<table>
<thead>
<tr>
<th>Group</th>
<th>Emitter (Doping([cm^3])/Thickness (µm))</th>
<th>Base (Doping([cm^3])/Thickness (µm))</th>
<th>Collector (Doping([cm^3])/Thickness (µm))</th>
<th>Common Emitter Current Gain (β)</th>
<th>Ron,sp (mΩ.cm²)</th>
<th>BVCEO (kV)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Purdue</td>
<td>1e19/1</td>
<td>1e17/1</td>
<td>8e14/50</td>
<td>15</td>
<td>78</td>
<td>3.2</td>
<td>41</td>
</tr>
<tr>
<td>Cree</td>
<td>*/0.75</td>
<td>2.5e17/1</td>
<td>2.5e15/20</td>
<td>20</td>
<td>10.8</td>
<td>1.8</td>
<td>17</td>
</tr>
<tr>
<td>RPI</td>
<td>Implanted</td>
<td>2e17/1</td>
<td>4e15/12</td>
<td>8</td>
<td>50</td>
<td>0.5</td>
<td>21</td>
</tr>
<tr>
<td>Cree</td>
<td>*/0.75</td>
<td>2e17/1</td>
<td>4.4e15/15</td>
<td>11</td>
<td>8</td>
<td>1.3</td>
<td>89</td>
</tr>
<tr>
<td>Purdue</td>
<td>1e19/1</td>
<td>1e17/1</td>
<td>2.4e15/20</td>
<td>55</td>
<td>8</td>
<td>0.5</td>
<td>90</td>
</tr>
<tr>
<td>Rutgers</td>
<td>*/0.7</td>
<td>3e17/0.8</td>
<td>6e15/12</td>
<td>32</td>
<td>17</td>
<td>0.7</td>
<td>91</td>
</tr>
<tr>
<td>Rutgers</td>
<td>1e20/1</td>
<td>8.5e17/1.4</td>
<td>7e14/50</td>
<td>7</td>
<td>33</td>
<td>9.2</td>
<td>92</td>
</tr>
<tr>
<td>RPI</td>
<td>1e19/0.8</td>
<td>2.3e17/1</td>
<td>1e15/45</td>
<td>9</td>
<td>56</td>
<td>4</td>
<td>93</td>
</tr>
<tr>
<td>KTH</td>
<td>9e19/0.4</td>
<td>1e17-1e18/0.4</td>
<td>5e15/15</td>
<td>6</td>
<td>*</td>
<td>1</td>
<td>23</td>
</tr>
<tr>
<td>KTH</td>
<td>9e19/0.3</td>
<td>4e18/0.3</td>
<td>8e15/10</td>
<td>5</td>
<td>*</td>
<td>-</td>
<td>87</td>
</tr>
<tr>
<td>Cree</td>
<td>*/1.5</td>
<td>2e17/1</td>
<td>4.8e15/15</td>
<td>40</td>
<td>22.5</td>
<td>1</td>
<td>16</td>
</tr>
<tr>
<td>Rutgers</td>
<td>1.3e19/0.8</td>
<td>2.9e17/1</td>
<td>5.5e15/15</td>
<td>5</td>
<td>5.7</td>
<td>1.6</td>
<td>18</td>
</tr>
<tr>
<td>KTH</td>
<td>5e19/0.6</td>
<td>3e17/0.7</td>
<td>4e15/15</td>
<td>64</td>
<td>*</td>
<td>1.1</td>
<td>88</td>
</tr>
</tbody>
</table>

* not mentioned in the paper.

Optimization of the current gain is quite complex since the current gain depends on the device cell structure as well as the parameters such as the material quality and the surface passivation. Optimal design is also important for device reliability.

For high voltage BJT structures, the collector doping needs to be low enough to form a thick drift region of 10-15 µm for a 1200 V SiC device. Also, the base should be designed with a sufficiently high doping dose to avoid punch-through at the maximum
required blocking voltage. On the other hand, the doping concentration in the emitter usually needs to be large compared to the base doping for high emitter injection efficiency, resulting in a high current gain. However, as the emitter doping concentration increases, doping induced band-gap narrowing is effectively increased, and above some doping level the emitter injection efficiency starts to decrease. In addition, as the emitter is highly doped, the diffusion length of the minority carrier in the emitter is decreased due to increasing Auger recombination. Bandgap narrowing and Auger recombination reduce the emitter injection efficiency and thus the current gain. The high-level injection occurring in the base at high current densities also results in a reduction of the emitter injection efficiency.

An accurate modeling of all relevant physical mechanisms is indispensable for identifying the impact of material properties on basic device characteristics and for device design and optimization. Furthermore, the interpretation of measurement results supported by numerical simulation is presently of particular interest in order to separate characteristics resulting from non-optimal material quality from those resulting from material properties inherent to SiC.

**2.2 Electrical Models of SiC**

The commercial software Integrated Systems Engineering (ISE) TCAD 10.0 [32] is used for the simulation study. In this section, the critical physical models are discussed.
2.2.1 Mobility Model

DESSIS, a part of ISE TCAD software, uses a modular approach for the description of the carrier mobility. In the simplest case, the mobility is a function of the lattice temperature. This so-called constant mobility model is for undoped materials. For doped materials, the carriers scatter with the impurities. This leads to a degradation of the mobility. Doping dependent mobility is expressed in Eqn.(2.1) based on the Masetti model [25].

\[
\mu_{dop} = \mu_{min1} \exp\left(\frac{P}{N_i}\right) + \frac{\mu_{const} - \mu_{min2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}}
\]  

(2.1)

Where \(N_i\) denotes the total concentration of ionized impurities. The reference mobilities \(\mu_{min1}, \mu_{min2}\), the reference doping concentrations \(P_c, C_r,\) and \(C_s,\) and the exponents \(\alpha\) and \(\beta\) are shown in Table 2.2.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter name</th>
<th>Electronics</th>
<th>Holes</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\mu_{min1})</td>
<td>mumin1</td>
<td>0</td>
<td>15.9</td>
<td>Cm²/(Vs)</td>
</tr>
<tr>
<td>(\mu_{min2})</td>
<td>mumin2</td>
<td>0</td>
<td>0</td>
<td>Cm²/(Vs)</td>
</tr>
<tr>
<td>(\mu_1)</td>
<td>mu1</td>
<td>0</td>
<td>0</td>
<td>Cm²/(Vs)</td>
</tr>
<tr>
<td>(P_c)</td>
<td>Pc</td>
<td>0</td>
<td>0</td>
<td>cm⁻³</td>
</tr>
<tr>
<td>(C_r)</td>
<td>Cr</td>
<td>1.94e17</td>
<td>176e19</td>
<td>cm⁻³</td>
</tr>
<tr>
<td>(C_s)</td>
<td>Cs</td>
<td>3.43e20</td>
<td>6.1e20</td>
<td>cm⁻³</td>
</tr>
<tr>
<td>(\alpha)</td>
<td>Alpha</td>
<td>0.61</td>
<td>0.34</td>
<td>1</td>
</tr>
<tr>
<td>(\beta)</td>
<td>beta</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

The Canali model [34] originates from the Caughey–Thomas [35] formula but has temperature-dependent parameters. At high electric fields, the carrier drift velocity \((V_d)\)
saturates due to an increase of the optical phonon scattering and reaches the saturation velocity \((v_{\text{sat}})\). The high-field mobility can be expressed as Eqn.(2.2).

\[
\mu(F) = \frac{\mu_{\text{low}}}{1 + \left(\frac{\mu_{\text{low}}F}{v_{\text{sat}}}\right)^\beta}
\]  

(2.2)

Where \(\mu_{\text{low}}\) denotes the low field mobility.

### 2.2.2 Incomplete Ionization

Dopants can be considered to be fully ionized at room temperature if the impurity levels are sufficiently shallow. However, when impurity levels are relatively deep compared to the thermal energy \((k_B T/q)\) at room temperature, incomplete ionization must be considered. The donor and acceptor energy levels in SiC are deeper than the thermal energy at room temperature, so the dopants in SiC are not fully ionized even above room temperature. For these situations, DESSIS has an ionization probability model based on activation energy as shown in Eqn.(2.3) and (2.4).

\[
N_D^+ = \frac{N_D}{1 + g_D \exp \left( \frac{E_{F_n} - E_D}{k_B T} \right)} \quad \text{for} \quad N_D < N_{D^+\text{Crit}}
\]  

(2.3)

\[
N_A^- = \frac{N_A}{1 + g_A \exp \left( \frac{E_A - E_{F_p}}{k_B T} \right)} \quad \text{for} \quad N_A < N_{A^-\text{Crit}}
\]  

(2.4)

Where \(E_{F_n}\) and \(E_{F_p}\) are the quasi-fermi levels, \(E_D\) and \(E_A\) are the donor and acceptor energy level, respectively. Due to the lack of specific information for SiC, the donor level degeneracy factor \(g_D\) and acceptor level degeneracy factor \(g_A\) are usually assumed to have
the same values as in Si. For nitrogen donor levels in 4H-SiC, a dopant ionization energy $E_{C}-E_{D} < 100$ meV and $g_{D}=2$ can be used. The p-type doping can be achieved with Al acceptors with ionization energy $E_{A}-E_{V} = 191$ meV and $g_{A} = 4$.

### 2.2.3 Recombination

The carrier recombination model is the Shockley-Read-Hall (SRH) equation. The Shockley-Read-Hall (SRH) recombination rate $R_{SRH}$ can be defined as

$$R_{net}^{SRH} = \frac{np - n_{1,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}$$

(2.5)

with:

$$n_1 = n_{1,eff} e^{E_{trap}/kT}$$

(2.6)

$$p_1 = n_{1,eff} e^{-E_{trap}/kT}$$

(2.7)

Where $\tau_n$ and $\tau_p$ are the electron and hole lifetimes, respectively, $E_{trap}$ is the difference between the defect level and intrinsic level. These lifetimes depend on material, temperature and defect concentration. Common SRH carrier lifetimes are in the range of 0.1–2 μs in 4H-SiC epitaxial layers but can be significantly reduced in ion implanted material.
2.2.4 Interface States

SiC/SiO₂ interface has electrically active trap density centers at least two orders of magnitude higher than Si/SiO₂ interface [36]. The pinning of the Fermi level at the surface of SiC and SiO₂ affects the physical properties of the system [36,37,38]. The 2-D and 3-D demonstration of the Fermi level pinning in the simulation is shown in Figure 2.3.

(a) 2-D demonstration of Fermi level pinning of energy bandgap

(b) 3-D demonstration of Fermi level pinning of energy bandgap

Figure 2.3 Surface Fermi level pinning in simulation
We analyze surface recombination in SiC BJT using the Shockley-Read-Hall (SRH) theory of recombination in the presence of Fermi level pinning due to surface states. In our simulation, constant densities of traps were assumed at the mid-bandgap. A capture cross-section of $\sigma=6\times10^{-15}\text{ cm}^2$ was used. The interface states density was determined by the matching of simulation results to the real measurement results. The traps energy level $E_o$ is set at the mid-bandgap level of 4H-SiC which is shown in Figure 2.4.

![Figure 2.4 Trap energy distribution](image)

**2.3 Cell Structure Optimization**

The simulated SiC BJT structure with the mesh grid is shown in Figure 2.5. The mathematical definition of optimization is, “to obtain the best possible design properties by changing the setting of independent variables in a continuous manner.” The design variables of the SiC BJT are as follows:

- Emitter Width
• Emitter Thickness
• Emitter Doping
• Base Emitter Space
• Base Doping

Figure 2.5  Structure and mesh grids used in the simulation

2.3.1 Emitter Width

(a) Emitter Size Effect

As mentioned in the simulation model section, under today’s processing technology, the interface states density between SiC/SiO₂ is much higher than that between Si/SiO₂. These interface states will function as the recombination center, which will cause the surface recombination current to be an important base current component that degrades
the current gain. Some minority carriers injected from the emitter recombine with the
base majority carriers at the surface. This surface recombination current, \( I_{B,\text{surf}} \), has no
contribution to the current gain. This base current component is proportional to the
emitter periphery rather than the emitter area, unlike the collector current. This effect
often appears in the Heterojunction Transistors and is not obvious in the Si BJT. In our
study of the SiC BJT, we can clearly see this effect. This is because the SiO₂/SiC
interface quality is not very good, and the surface recombination current is high. With the
Emitter Size Effect, the base current can be expressed as Eqn.(2.8) [39].

\[
\frac{J_c}{\beta} = (J_{BQN} + J_{BSCR} + J_{BP}) + K_{Bsurf} \cdot \frac{P_E}{A_E}
\]  

(2.8)

Where \( J_c \) is the collector current density, \( J_{BQN} \) and \( J_{BSCR} \) are the base bulk and quasi-
neutral, space charge recombination current densities, respectively, and \( J_{BP} \) is the back-
injection current density. \( K_{Bsurf} \cdot P_E \) is the emitter periphery surface recombination current,
\( A_E \) and \( P_E \) are the emitter area and periphery respectively [40]. \( K_{Bsurf} \) in A/cm is the
normalized surface recombination current.
Simulations were carried out to study the emitter size effect on SiC BJT. Figure 2.6 shows the half-cell structure used in our simulations. Emitter length and width were defined in Figure 2.6. In the simulation, “b” is the emitter length and “a” is the emitter width. Decreasing “a” causes an increase in $P_E/A_E$. In the 2D simulation, only the effect of “a” can be simulated. So $P_E/A_E$ is expressed by $1/a$ in Figure 2.7, where the $J_c/\beta$ as a function of the $P_E/A_E$ ratio is shown.
From Eqn.(2.8), the slope of the lines in Figure 2.7 is the normalized periphery recombination base current $K_{B,\text{surf}}$ and is shown in Figure 2.12. It shows that as the collector current density increases from 12 to 200 A/cm$^2$, the slope $K_{B,\text{surf}}$ also increases, which will cause a decrease of the current gain at high collector current density.
Figure 2.8 shows the beta as a function of current density at different emitter widths. As the emitter size decreases, the gain shifts down. Improving the quality of SiC/SiO\(_2\) interface is important to get a high gain especially for narrow emitter fingers. As emitter size increases above a certain value (16\(\mu\)m in our case), the gain stops increasing. This is due to the current crowding effect at the edges of the emitter, which starts to dominate. Therefore, 10\(\mu\)m is recommended as the optimum emitter width design value.

(b) Measurement Results

Devices with different emitter widths on the same chip were fabricated at Cree. The three emitter widths were 6\(\mu\)m, 8\(\mu\)m and 10\(\mu\)m respectively. I-V characteristics were measured by Tektronix 370A curve tracer. The extracted common emitter current gain from the measured I-V characteristics as a function of collector current density is shown in Figure 2.9.

Figure 2.9 Measured current gain as a function of collector current density with different emitter width
From Figure 2.9, the 10µm emitter width BJT has the highest gain because it has the smallest emitter periphery over area (P_E/A_E) ratio. At I_b=100mA, V_{ce}=5V, the current gain increases from 34 to 44 as the emitter width goes from 6µm to 10µm as shown in Figure 2.10. Figure 2.11 shows experimental plots of J_c/\beta as a function of P_E/A_E at current densities of 12, 100, and 200 A/cm². Similar to the simulation results shown in Figure 2.7, the result indicates an increasing effect of the surface current at higher current density.

![Emitter Size Effect](Image)

Figure 2.10 Current gain as a function of emitter width
Figure 2.11 Emitter Size Effects for $J_c=12$, 100 and 200A/cm$^2$ (The slope in the graph is the normalized periphery recombination base current)

Surface recombination currents extracted by measurement and simulation data are shown together in Figure 2.12, which clearly shows the increase of the normalized periphery surface recombination current as a function of collector current density. Since this is a two-dimensional simulation, the value extracted by simulation data is smaller than that by the measured three-dimensional value, but they have the same trend. Figure 2.12 also shows that the surface recombination current of today’s SiC BJT is comparable to that of the Heterojunction Bipolar Transistors (HBTs) [40], and it is much larger than that of Si BJT which has a very mature processing technology.
Both the simulation and experiment results show that in today’s SiC BJT, Emitter Size Effect (ESE) plays a role in determining the common emitter current gain. As current density increases, the effect is more and more obvious. For the first time, surface recombination current is reported by the extraction from both measurement and simulation data for today’s SiC BJT. Designers need to take this effect into account during device design. An optimum value in emitter size exists that minimizes the surface recombination current effect and the emitter current crowding effect.

### 2.3.2 Emitter Thickness

Due to the high doping concentration in the emitter, the diffusion length for the holes \((L_p)\) is small. The continuity equation for holes in the emitter is given by Eqn. (2.9)[20]:

\[
\frac{d^2p}{dx^2} - \frac{p}{L_p^2} = 0
\]  

(2.9)
If the thickness of the N⁺ emitter is much larger than the diffusion length, the hole concentration decays exponentially with distance from the junction to its equilibrium value. The solution for the hole distribution is given by Eqn.(2.10):

$$p(x) = P_E(0) \cdot \exp\left(-\frac{x}{L_p}\right)$$  \hspace{1cm} (2.10)

With x increasing away from the junction edge, the hole current flowing at the emitter-base junction is then given by Eqn(2.11):

$$J_p(0) = qD_{PE}\left[\frac{dp}{dx}\right]_{x=0}$$  \hspace{1cm} (2.11)

Using Eqn. (2.10) and (2.11)

$$J_p(0) = \frac{qD_{PE}P_{OE}}{L_{pe}} \exp\left(\frac{qV_{BE}}{kT}\right)$$  \hspace{1cm} (2.12)

The common emitter current gain, as determined by the emitter efficiency, is given by Eqn.(2.13) [20]:

$$\beta_E = \frac{D_{nB}n_{nB}L_{pe}}{D_{pE}P_{oE}W_B}$$  \hspace{1cm} (2.13)

If the intrinsic concentrations in the emitter and base regions are denoted as $n_{icE}$ and $n_{icB}$, respectively, the injection efficiency limited current gain can be related to the doping concentrations in the emitter ($N_{DE}$) and base ($N_{AB}$) regions:

$$\beta_E = \left(\frac{D_{nB}}{D_{pE}}\right)\left(\frac{L_{pe}}{W}\right)\left(\frac{N_{DE}}{N_{AB}}\right)\left(\frac{n_{icB}^2}{n_{icE}^2}\right)$$  \hspace{1cm} (2.14)

The above equation was derived under the assumption of a thick emitter region and no recombination in the base region. If the diffusion length for the holes in the emitter is not
much smaller than the emitter width ($W_E$), the holes injected into the emitter region can
diffuse through it and reach the emitter (ohmic) contact. This effect will decrease the gain
greatly.

As long as the Emitter depth is longer than the hole diffusion length in Emitter, the
increase of the emitter has little effect as shown in Figure 2.13. When the Emitter depth
is smaller than 2µm, the gain begins to drop. So 2 µm is recommended as the Emitter
depth for an optimized BJT.

![Beta vs Jc (with different Emitter depth)](image)

Figure 2.13  Simulated beta as a function of Jc with different emitter depth

### 2.3.3 Emitter Doping

From Eqn.(2.14) a very low base doping concentration and a very high emitter doping
concentration are desirable to achieve a high gain. However, an increase in the emitter
doping is accompanied by a reduction in the diffusion length due to Auger recombination
and by an increase in the emitter intrinsic carrier concentration due to band gap narrowing. These effects counteract the increased doping concentration.

Figure 2.14 shows simulation results of $\beta$ as a function of emitter doping. As emitter doping rises to higher than $2e19\text{cm}^{-3}$, the gain decreases instead of increasing. $2e19\text{cm}^{-3}$ is the optimum doping concentration here.

![Figure 2.14 Simulated beta as a function of emitter doping](image)

### 2.3.4 Base Doping

From Eqn.2.14, it is evident that the lower the base doping, the higher the gain, but there is a trade off with the breakdown voltage. Too low base doping will cause the low punch through breakdown before the avalanche breakdown. A reduction in the base doping concentration leads to a low reach-through breakdown voltage and a poor output conductance due to depletion of the base region. Although these effects can be prevented
by increasing the base width, this will also result in reduction of the current gain. A low base doping concentration results in a high base sheet resistance, which degrades current distribution under the emitter in the on-state and the storage time during turn-off. So reducing the base doping is not a good way to increase the gain.

In order to make sure the breakdown voltage won’t suffer, the total charge in the base should be fixed. However, different doping profiles have advantages in the performance. When the base doping profile is graded as in Figure 2.15, a built-in electric field in the graded base as shown in Figure 2.16 will help injected electrons from the emitter to transit more quickly through the base, reducing the base recombination.

![Figure 2.15 Graded base doping profile](image-url)
In order to see the effect of the build-in field, the number of impurities per unit area in the base (also called the Gummel number) is kept the same.

For the uniform base doping, the Gummel number can be obtained by following.

$$N_b \times W_b = 3.4e16 \times 1\mu m = 3.4 \times 10^{12} \text{#/cm}^2.$$  

For the graded base doping, the Gummel number can be obtained by following.

$$Q_b = \int N_b dx \approx \frac{1}{2} (6e15 + 5e16) \cdot 10^{-4} = 3.25 \times 10^{12} \text{#/cm}^2.$$  

Figure 2.17 shows the simulation results with different base doping profiles. The graded base case has higher gain. The difference in the gains is believed to be related to the accelerating effect due to the build-in electric field introduced by the graded base doping profile.
2.3.5 Spacing Between p+ Base Implant and Emitter Effect

As the p+ base contact implant is brought closer to the emitter edge, the current gain decreases. It may be due to the p+ base contact implant introducing defects into the SiC that are not completely removed during the implant activation aneal [41]. This effect can be seen in Figure 2.18. As the space between the p+ implant and emitter decrease from 4µm to 1µm, the gain of BJT decreases monotonically.

Figure 2.19 shows the lateral electron distribution in the base. In the case of 1µm space between the p+ implant and emitter, which is shorter than the electron diffusion length, electron density drops to nearly zero once it reaches the p+ implant. The defects at the p+ implant cause a very high recombination rate. This recombination current provided by the base does not contribute to the total current gain. In the case of 5µm BE space, lateral
electron density will drop to zero before they reach the base implant. In this case, the defects introduced by the base implant will not affect the current gain.

When designing a BJT, the space between Base and Emitter should be minimized, provided it is longer than the electron diffusion length. The space between Base and Emitter will introduce the extrinsic base resistance. As the space increases, the extrinsic base resistance will increase, causing more current crowding and surface recombination current which will decrease the current gain.
Figure 2.19 Lateral electron distribution in the base

Figure 2.20 shows the maximum current gain as a function of the space between p+ implant and emitter edge. When the space is larger than 3µm, the space effect is not so obvious. In the real devices, due to process variation, 5µm was chosen. In reference [23], they proposed a new technique to fabricate the extrinsic base using epitaxial regrowth of the extrinsic base layer, thereby avoiding the space effect between p+ and emitter edge.

Table 2.3 lists the design trends for various parameters.
Figure 2.20 Maximum current gain as a function of space between p+ implant and emitter edge

Table 2.3 A summary of the optimized SiC BJT

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Design Trend</th>
<th>Design Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Width(µm)</td>
<td>Optimized</td>
<td>10</td>
<td>Limited by ESE and the emitter current crowding</td>
</tr>
<tr>
<td>Emitter Thickness(µm)</td>
<td>Thinner</td>
<td>2</td>
<td>Limited by the minority carrier diffusion length in the emitter</td>
</tr>
<tr>
<td>Emitter Doping(cm⁻³)</td>
<td>Higher</td>
<td>2e19</td>
<td>Limited by the Auger recombination and bandgap narrowing</td>
</tr>
<tr>
<td>Base Emitter Space(µm)</td>
<td>Shorter</td>
<td>4</td>
<td>Limited by the high recombination caused by the p+ implantation induced defects</td>
</tr>
<tr>
<td>Base Doping(cm⁻³)</td>
<td>Lower</td>
<td>Graded</td>
<td>Helped by the build in electric field introduced by the graded doping</td>
</tr>
</tbody>
</table>
2.4 Base Resistance Model

Base resistance is important for characterizing the large and small-signal behavior, switching characteristics, and noise performance of high-speed bipolar transistors. The accurate determination of the base resistance is essential for BJT design and modeling. It is known that the base resistance decreases as the operating current increases due to base conductivity modulation, base push-out in high-level injection, and current crowding effects [20]. The crowding is the tendency for current to flow at the edge of the intrinsic base region at high-level current injection due to a voltage drop along the base current path in the intrinsic base region. Accurate modeling of base resistance is complicated due to its distributed nature and operating point dependence [42].

Modeling and computation of the base resistance based on the debiasing and current crowding effect in the two-dimensional (2-D) intrinsic base region of BJT’s are needed to study and optimize the BJT layout. Figure 2.21 shows the top view of a typical stripe BJT with double metal layout used for base resistance study. The die area is 1500µm by 1500µm square. Two types of finger length: 34 fingers of 1336µm and 19 fingers of 880µm.

Base current flows from the base pad, through the peripheral metal to the finger metal and then into the base. In effect, base resistance consists of peripheral metal resistance, finger metal resistance, contact resistance and semiconductor base cell resistance. Each resistance is modeled in the next section. The whole base resistance model was developed by a small area test BJT layout. Then the model was implemented to a large area device,
in which the base debiasing effect is more important. The comparison between different layouts was based on this model.

Figure 2.21 BJT layout used for base resistance study

2.4.1 Metal Resistance

Base current flows from the base pad and distributed to each cell. The metal resistance is calculated in this section.

(a) Metal Two Peripheral Metal Resistance

The top peripheral metal is split into four parts as shown in Figure 2.21. For part 1, the metal resistance can be calculated as follows:
\[ \rho = 2 \mu \Omega \cdot cm, \quad L = 880 \times 10^{-4} cm, \quad s = \frac{(1500 - 1336) \times 10^{-4}}{2} \times 2 \times 10^{-4} = 1.64 \times 10^{-6} cm^2 \]

\[ R_{mp,1} = \rho \frac{L}{s} = 0.1073 \Omega \]

2\(\mu\)m is the metal thickness and is used for area calculation.

Similar methods can be applied to part 2-4.

\[ R_{mp,2} = 0.1629 \Omega \]
\[ R_{mp,3} = 0.1629 \Omega \]
\[ R_{mp,4} = 0.1073 \Omega \]

(b) Metal Resistance for One Cell

Base current flows through the top metal to the first layer of metal. The scenario of the first layer metal resistance calculation is as follows. Every 88\(\mu\)m is considered one cell, so the 1336\(\mu\)m finger is composed of 15 cells and the 880\(\mu\)m finger is composed of 10 cells.

\[ \rho = 2 \mu \Omega \cdot cm, \quad l = 88 \times 10^{-4} cm, \quad w = 5 \mu m \ (metal \ finger \ width), \]

\[ Rs(sheet \ resis) = \frac{\rho}{t(metal \ 1 \ thickness)} = \frac{2}{1} = 0.02 \Omega \cdot \square \]

\[ R_{mc} = Rs \frac{l}{w} = 0.352 \Omega \]

(c) Cell Contact Resistance

Another part of the base resistance is the contact resistance.
Specific contact resistance $1.2e-4 \, \Omega \cdot \text{cm}^2$ is used to calculate the contact resistance for cells.

\[
R_{c,sp} (\text{specific contact resis}) = 1.2 \times 10^{-4} \, \Omega \cdot \text{cm}^2, \quad l = 88 \times 10^{-4} \, \text{cm}, \quad w = 5 \mu\text{m},
\]

\[
R_e = \frac{R_{c,sp}}{l \times w} = 27.3 \, \Omega
\]

### 2.4.2 Cell Model

After the metal resistance calculation, the semiconductor base resistance is modeled as follows.

Schematic diagram of the active region in the BJT is shown in Figure 2.22. Every base finger provides base current to two BE junctions.

![Schematic diagram of the active region in the BJT.](image)

Figure 2.22 Schematic diagram of the active region in the BJT.

#### (a) Cell Base Resistance

ISE TCAD was used to simulate one BJT 88\(\mu\)m long. Figure 2.23 shows 2-D simulation of BE junction I-V of an 88\(\mu\)m cell, showing the turn-on voltage of 3.1V and the slope \(R_{b}=12.66\Omega\).
Based on the above simulation, a saber model was built for the BE junction. The schematic is shown in Figure 2.24.

The 3.1V voltage source is used to model the turn on voltage. The 12.66Ω resistor represents the base resistance on one side of BJT cell in Figure 2.22. Two of these pair consist of one cell base model.
(b) Saber Model

Base current flow distribution of the entire device is shown in Figure 2.25 in the top-view.
Figure 2.26 shows the saber model for BJT base fingers. The base current flows from the base pad, goes through the metal resistors $R_{mp}$, and then to each finger. When the current goes along the finger, it goes through the contact resistance $R_c$ and into the base. From one cell to the other cell, the current needs to go through cell metal resistance between the two, $R_{mc}$.

**2.4.3 Complete Base Resistance Model**

Based on the above discussion, Figure 2.27 shows the entire base resistance model implemented in Saber simulator.

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Using the above model, the current distribution among cells can be calculated and is shown in Figure 2.28. The minimum current density is $J_{\text{min}}=6.78\mu\text{A}/\mu\text{m}$ and the maximum current density is $J_{\text{max}}=14.5\mu\text{A}/\mu\text{m}$. The ratio of the minimum current density cells area to the total area ($S_{\text{min}}/S_{\text{total}}$) is 24.57%. These cells are dangerous during the BJT turn-off. Since they are located far from the base pad, they are the last part to be turned off. The current will divert from the “off” cells to these “on” cells, causing the
increase of the current density in these cells to extremely high values. It may damage the cells and the device. Similarly, the ratio of the highest current density cells area to the total area ($S_{\text{max}}/S_{\text{total}}$) is 3.1%. These cells are dangerous during the BJT turn-on. Since the cells are located near the base pad, they are the first part to be turned on which will cause current crowding to the cells, leading to damage of the device.

![Current Distribution Among Cells](image)

Figure 2.28 Current distribution among cells

From the analysis above, for a layout, a uniform base current distribution is desired. It will help to optimize the performance and reliability of the BJT. This is even more important as the device area is increasing.

Based on this model, the different BJT layouts can be evaluated. Next, three larger BJT layouts will be discussed based on the above model.
2.4.4 Base Resistance Model for Large Area BJTs

Three types of BJT layouts with an area of 4.24mm x 4.24mm and a current rating of 30A will be evaluated based on the previous model. They will be compared in terms of base resistance. The large ratio of the minimum current density cells area to the total area means a relatively more uniform base current distribution. Similarly, the large ratio of the maximum current density cells area to the total area means a relatively more uniform base current distribution and a smaller ratio of the maximum current density to the minimum current density means a relatively more uniform base current distribution.

(a) Structure Type –I:

![Figure 2.29 Type-I BJT layout](image)
Chip size is 4.24 mm x 4.24 mm with the active area 4 mm x 4 mm. The base pad is in the middle of the BJT. Perpendicular bus lines conduct the current to different fingers and the peripheral. The corresponding dimensions of the BJT layout are shown in Figure 2.29. The current distribution of the layout type I is shown in Figure 2.30, the cell number as a function of the current density range.

![Current Distribution Layout Type 1](image)

Figure 2.30 Current distribution for layout type-I

The maximum current density is about five times that of the smallest current density in this layout, $J_{\text{max}}/J_{\text{min}}=4.9$. The smallest current density cells cover a large part of the total area. So in this case, the largest current density cells should be noted. From Figure 2.30, it shows the area ratio of large current density cells to the total area ($S_{\text{large current}}/S_{\text{total}}$) is only 1.364%. These 1.364% cells will turn on faster than the other cells on the chip, which may cause current crowding in these cells.
Figure 2.31 shows the maximum and minimum current density cell distribution in the layout. The green dots show the part of cells that have the lowest current density. The red dots show the part of cells with the highest current density. As expected, the highest current density cells are located close to the pad and the lowest current density cells located far from the base pad. Besides, it is not convenient in making a connection of this layout BJT with an anti-parallel diode.

(b) Structure Type – II

Structure type II is similar to type I with the base pad at the bottom of the BJT. Perpendicular bus lines conduct the current to different fingers and the peripheral. There are a total of 74 pairs of emitter and base fingers per quarter, including 66 pairs of long
fingers and 8 pairs of short fingers. The corresponding dimensions of the BJT layout are shown in Figure 2.32.

The current distribution of the layout type II is shown in Figure 2.33, the cell number as a function of the current density range.

Figure 2.32 Layout type-II
For type II layout, the maximum current density is about 68 times of the smallest current density ($J_{\text{max}}/J_{\text{min}}=67.9$). The lowest current density cells take a large part of the total area.

So in this case, the largest current density cell should be noted. Figure 2.33 reveals the area ratio between large current density cells and the total area is only 0.74%. This 0.74% of cells will be turned on faster than other cells, which may cause current crowding in these cells.

Figure 2.34 shows the maximum and minimum current density cells distribution in the layout. The green dots show the part of the cells with the lowest current density. The red dots show the cells with the highest current density. As expected, the highest current density cells are located close to the pad and the lowest current density cells are located at the top of the chip and far from the base pad.
In structure type II, the base pad is moved from the middle to the bottom, and the base current needs to go through the whole chip to go into the base of the top cells. Compared with structure type I, the uniformity of the type II layout is worse, but it is easier for the connection to the anti-parallel diode.

(c) Structure Type III:

Base pads are located both at the bottom and on the top of the BJT. Bus lines conduct the current to different fingers from the middle of the chip layout. There are total of 158 pairs of emitter and base fingers per half of the chip. The corresponding dimensions of the BJT layout are shown in Figure 2.35.
The current distribution of the layout type III is shown in Figure 2.36, the cell number as a function of the current density range. The maximum current density is about six times the size of the smallest current density in this layout ($J_{\text{max}}/J_{\text{min}}=6$). The smallest current density cells cover a large part of the total area. So in this case, the largest current density cells should be noted. Figure 2.36 reveals the area ratio between large current density cells and the total area is only 0.46%. These 0.46% cells will be turned on faster than other cells, which will cause current crowding in these cells.
Figure 2.36 Current distribution of layout type-III

Figure 2.37 shows the maximum and minimum current density cells locations in the layout. The green dots show the cells with the lowest current density. The red dots show the cells with the highest current density. As expected, the highest current density cells are located close to the pad and the lowest current density cells located far from the base pad, and are in the middle of each half chip.
Figure 2.37 Maximum and minimum current density cells location in type-III layout

The comparison between the three types of layouts is shown in Figure 2.38. Type-I is the best since it has the smallest $J_{\text{max}}/J_{\text{min}}$ ratio and largest $S_{\text{largecurrent}}/S_{\text{total}}$ ratio. From the base current distribution uniformity point of view, the type-I layout will have more uniform current distribution. However, the type-I layout is not convenient for the connection with the anti-parallel diode in a package. So in the real application, type III is an alternative choice. Alternatively, monolithic solutions give better performance with the integration of BJT and the anti-parallel diode on the same chip.
Figure 2.38 Three layouts comparison

Type-I
\[ \frac{S_{\text{large current}}}{S_{\text{total}}} = 1.364\% \]
\[ \frac{J_{\text{max}}}{J_{\text{min}}} = 4.9 \]
Best

Type-II
\[ \frac{S_{\text{large current}}}{S_{\text{total}}} = 0.74\% \]
\[ \frac{J_{\text{max}}}{J_{\text{min}}} = 67.9 \]
Worst

Type-III
\[ \frac{S_{\text{large current}}}{S_{\text{total}}} = 0.46\% \]
\[ \frac{J_{\text{max}}}{J_{\text{min}}} = 6.09 \]
middle
Chapter 3 SiC BJT Fabrication Techniques and Device Characterization

The 1200V SiC BJT samples were fabricated by Cree Inc. The cross-section of the SiC BJT is shown in Figure 3.1. In this chapter, the key process steps and the characterization of the fabricated device are discussed.

![Figure 3.1 SiC BJT](image)

**3.1 Fabrication Steps**

One of the main advantages of SiC device technology is the compatibility with Si processing technology compared with other wide bandgap materials. However, there are some differences from Si process technology because of the chemical inertness and the thermal stability of SiC. First of all, wet chemical etching is almost impossible in SiC at room temperature. Instead, plasma etching is available for definition of mesa-etched
structures in SiC. The diffusivity of impurities in SiC is orders of magnitude lower than in Si and so diffused doping profiles aren’t usually considered for SiC devices. Generally, ion implantation and epitaxial growth are needed for proper doping concentrations. Finally, much higher temperatures are needed for thermal oxidation, annealing of metal ohmic contacts, and activation of implanted impurities.

The main fabrication steps are shown in Figure 3.2 [16,17,22] The starting wafer is a n+/p/n-/n+ substrate with 4.8e15 cm⁻³ for the drift layer. P layer is 1µm thick and 2e17cm⁻³ doped. The top n+ is 0.5µm 2e19cm⁻³ doped. The key masking steps are shown as following [16,17,22]:

(a) Starting wafer

(b) Emitter etch

(c) Base implantation

(d) Mesa Etch
The chip layouts of fabricated BJTs are shown in Figure 3.3 and Figure 3.4, respectively. The base and emitter pads for the striped devices are located at the right corner and in the middle, respectively. The emitter stripes are 1336 μm long and 10 μm wide. It was discussed in the previous chapter that 5 μm is the spacing between the p-contact and the...
emitter sidewall in order to achieve the best device performance. If the contact is brought any closer, the implantation-induced damages start to have a detrimental effect on the device. The cell pitch is 25μm. Two-level metal is required for this structure in order to isolate the emitter and base contacts [16,17,22].

The junction termination extension (JTE) structure is designed to be 120μm long with 15 zones of p-type charge. The channel stop implantation is 5μm wide and it is placed 30μm away from the edge of the JTE [16,17,22].

Figure 3.3 Chip layout
3.2 Characterization

The top-view and the packaged sample of an inter-digitized BJT with an active area of 0.0225cm² (1.5mm by 1.5mm) are shown in Figure 3.5. It was characterized and some phenomena significantly different from Si BJTs are analyzed theoretically and experimentally.
3.2.1 Voltage Blocking Capability

As discussed in section 1.4.2, for different BJT operation modes, the breakdown voltage is different. For Si BJT, the value of $BV_{CEO}$ is smaller than $BV_{CBO}$. However, in SiC BJTs, the measured difference between $BV_{CEO}$ and $BV_{CBO}$ is not as obvious as Si BJTs as shown in Figure 3.6 because of the low current gain at low current densities.
Figure 3.6 $BV_{CEO}$ and $BV_{CBO}$ of SiC BJT

Figure 3.7 Gummel plot for SiC BJT

Figure 3.7 shows the Gummel plot of the 1200V SiC BJT. At $I_c=3\mu A$, the common emitter current gain is only 1.875. As the current increases, the gain increases. At $I_c=30\mu A$, the current gain is 6. The increase in current gain is due to the less domination
of space charge recombination current in the base current. The current gain increases with
the current increase, resulting in more obvious different between $\text{BV}_{\text{CEO}}$ and $\text{BV}_{\text{CBO}}$.

$\text{I}_c=2\times10^{-6},$
$\text{BV}_{\text{CEO}}=1576V,$
$\text{BV}_{\text{CBO}}=1624V,$
$\text{BV}_{\text{CES}}=1649V$
$\Delta V=\text{BV}_{\text{CBO}}-\text{BV}_{\text{CEO}}=48V$
$\beta=1.83$

$I_c=2\times10^{-4},$
$\text{BV}_{\text{CEO}}=1812V,$
$\text{BV}_{\text{CBO}}=2018V,$
$\text{BV}_{\text{CES}}=2044V$
$\Delta V=\text{BV}_{\text{CBO}}-\text{BV}_{\text{CEO}}=206V$
$\beta=12.1$

Figure 3.8 $\text{BV}_{\text{CEO}}, \text{BV}_{\text{CBO}}, \text{BV}_{\text{CES}}$ at different current level

Figure 3.8 shows the $\text{BV}_{\text{CEO}}, \text{BV}_{\text{CBO}}$ and $\text{BV}_{\text{CES}}$ (base and emitter are shorted) at different
current levels. It shows that at very low current level, there is not much difference
between these breakdown voltages. As current increases to 200$\mu$A, the breakdown
voltage $\text{BV}_{\text{CEO}}$ is about 200V less than $\text{BV}_{\text{CBO}}$.

Because of the defects in SiC wafers, usually the breakdown voltage measurements are
made with the current limit less than 50$\mu$A. Under such low breakdown current, the gain
of SiC BJT is low so that the difference between $\text{BV}_{\text{CEO}}$ and $\text{BV}_{\text{CBO}}$ is not as obvious as Si
BJT.
3.2.2 Forward I-V Characteristics

In this section the forward characteristics of devices fabricated on the 15μm thick drift layer are evaluated. Figure 3.9 shows the typical I-V characteristics under room temperature and 150°C by curve tracer of a 0.225mm² active area device (pitch = 25μm) with the inter-digitized stripe design. The device was heated by a hot plate.

![Figure 3.9 I-V characteristics by curve tracer](image)

(a) Conductivity Modulation in the Drift Region

As a bipolar device, conductivity modulation of the drift region will reduce the on-resistance so that the conduction loss will be reduced when the BJT is in on-state. From Figure 3.9, it should be noted that the curves corresponding to the different base currents are overlapped in the saturation region and the quasi-saturation region is absent. This output characteristic is similar to a unipolar device that has no conductivity modulation of the collector layer at room temperature. The slope of the I-V curve represents the resistance of the drift layer. The measured on-resistance of SiC BJT is 4.1mΩ·cm². This
value is larger than the theoretical resistance of the 15µm thick drift layer doped at 4.8x10^{15} \text{ cm}^{-3}, which is about 2.4m\Omega \cdot \text{cm}^2.

From Figure 3.9, conductivity modulation can not be seen. Previously, the lack of conductivity modulation was explained by poor minority carrier life-time in the base and collector regions, and especially at the B-C interface in [22]. In order to study the conductivity modulation in SiC BJT, numerical simulations were used. Figure 3.10 shows a good match of the simulation with the measured results at I_b=60mA. Based on this simulation, the forward conduction mechanism in the saturation region can be analyzed in detail.

![Ic_Vce](image)

**Figure 3.10 Forward I-V curve measurement and simulation**

Figure 3.11 shows the hole density distribution across the BJT at different base currents. It shows that as the base current increases, the conductivity modulation is clearly shown by the increased level of holes (minority carrier). For the 1200V SiC BJT under
consideration, since the collector donor doping concentration is quite high even for a high voltage device such as the one under study, the high level injection (hence observable conductivity modulation) only occurs when the current density is very high, which is different from the Si device.

Figure 3.11 Hole density distribution at different base currents in the BJT

Figure 3.12 Carriers distribution at $I_C=1.26A$, $V_{CE}=0.349V$
At $I_c=1.26\,\text{A}$, $V_{CE}=0.349\,\text{V}$ and $I_b=190\,\text{mA}$, the electron and hole density distributions along a cut at the edge of the emitter is shown in Figure 3.12. From Figure 3.12, we can see that both hole and the electron densities are already higher than the collector doping concentration, indicating high level injection under this condition. There is obvious conductivity modulation in the device. So why is the observed on-resistance still higher than the theoretical on-resistance?

First, conductivity modulation is defined as the conductivity of the collector region being increased beyond its unmodulated conductivity. This is different from the voltage we are measuring from C to E, $V_{CE}$. If we use $V_{CE}/I_c$ to obtain $R_{on-sp}$, then one must know that the $V_{CE}$ is the total voltage drop from C to E, which is not the same as the voltage drop in the collector region. Therefore we must distinguish the difference between these two concepts.

To clarify the point, the internal potential distribution of the SiC BJT is shown in Figure 3.13 under the same operating conditions as Figure 3.12. Due to the significant voltage drop across the base region, as well as across the contact resistance $R_C$ and $R_E$ that need to be included in the model to obtain a satisfactory match in Figure 3.10, the voltage drop in the drift region is only 78 mV, as shown in Figure 3.13. If we use this value to calculate the on-resistance in the collector drift region, the specific resistance is only 1.39 mohm.cm$^2$, which is already significantly smaller than the specific resistance of the 15um thick drift layer doped at $4.8\times10^{15}$ cm$^{-3}$ (2.38 mohm.cm$^2$). This simulation suggests that one can’t use the measured $V_{CE}/I_c$ to determine if there is conductivity modulation or not.
Figure 3.13 Potential distribution across the BJT at $I_c=1.26A$, $V_{CE}=0.349V$

Figure 3.14 Horizontal current density distribution

Another important factor in assessing the conductivity modulation issue is that the current conduction in the BJT is strongly non-uniform. Therefore, the terminal resistance measured using $V_{CE}/I_c$ is hardly a good measure of the internal conductivity.
As clearly shown in Figure 3.14, the lateral current density distributions in the SiC BJT at the same operating conditions as Figure 3.12, the conductivity under the emitter is much higher than in those locations far from the emitter. The non-uniform current distribution in the base and collector region will result in a much higher calculated $R_{on-sp}$ value using $V_{CE}/I_C$ although the internal conductivity may be already very high.

Due to the base current de-biasing effect, a large chip area of BJT’s performance is also strongly related to the device layout. Those cells that are closer to the base pad will have smaller base resistance so those cells will have higher conductivity modulation than other cells which are far away from the base pad. One must take note of this issue because this de-biasing effect does not happen in the power MOSFET, which is why the $R_{on-sp}$ value is a good indication of the current conduction capability even for a large size power MOSFET.

Another important factor is that for the same amount of hole increase ($\Delta p$), the contribution on the increase of conductivity in SiC BJTs is smaller than that in Si BJTs because SiC’s hole mobility is smaller than Si hole mobility as explained in Eqn(3.1) and Eqn.(3.2).

*Assume under high level injection.*

$$\Delta n \approx \Delta p >> N_D$$  
(3.1)

$$\frac{\Delta \sigma_{Si}}{\Delta \sigma_{SiC}} \approx \frac{\Delta p \cdot q \cdot (\mu p_{Si} + \mu n_{Si})}{\Delta p \cdot q \cdot (\mu p_{SiC} + \mu n_{SiC})} \approx 2.4$$

$$\frac{\Delta I_{Si}}{\Delta I_{SiC}} = \frac{V_{CE} \cdot \Delta \sigma_{Si}}{V_{CE} \cdot \Delta \sigma_{SiC}} \approx 2.4$$  
(3.2)
Where $N_D$ is the drift region doping concentration. $\mu_{\text{psi}}=465 \text{ cm}^2/\text{v.s}$, $\mu_{\text{nsi}}=1365 \text{ cm}^2/\text{v.s}$ and $\mu_{\text{psic}}=109 \text{ cm}^2/\text{v.s}$, $\mu_{\text{nsic}}=673 \text{ cm}^2/\text{v.s}$ represent the hole and electron mobility of Si and SiC respectively [52].

Assume the current is uniform in the drift region. Under the same $V_{CE}$, the ratio of the current increase because of the conductivity modulation between Si and SiC is around 2.4 times. So conductivity modulation in Si BJTs is more obvious than in SiC BJTs.

To design a Si BJT to have the same $BV_{CBO}$ as the SiC BJT, a drift doping at around $8 \times 10^{13} \text{ cm}^{-3}$ has to be used. Assume the same electric field in drift region of Si and SiC BJTs when operating in the saturation region, the ratio of the drift current density in the drift region can be calculated in Eqn. (3.3).

$$\frac{J_{d_{\text{si}}}}{J_{d_{\text{sic}}}} = \frac{N_{D_{\text{si}}} \cdot q \cdot \mu_{n_{\text{si}}} \cdot E}{N_{D_{\text{sic}}} \cdot q \cdot \mu_{n_{\text{sic}}} \cdot E} = \frac{8 \times 10^{13} \cdot 1365}{4.8 \times 10^{15} \cdot 673} \approx 0.03 \tag{3.3}$$

From Eqn.(3.3), we can see that in order to get high-level injection, the required current density of SiC is much higher than that of Si. Electric field in the drift region usually is very small when BJT is in saturation region, so the carrier density has a dominate role in the current. To conduct a certain amount of current, for the SiC BJT, only the electrons from the ionized dopant in the drift region are enough, while for Si BJT, high level injection is needed to obtain that current density. This is another reason why for the same $BV_{CBO}$ BJTs, Si BJT is easier to see the conductivity modulation than the SiC.

The high surface recombination current can also be a reason for the lack of conductivity modulation. When the surface recombination current is high, a large part of base current is wasted at the surface instead of being injected into the collector for modulation. Once
the surface condition is improved, the conductivity modulation will begin to appear, although it may not as obvious as Si BJTs due to reasons previously discussed. Cree Inc. recently proved this with a finished BJT lot in which the surface was carefully treated during the manufacture, as shown in Figure 3.15. We can see the separation of collector currents with different base currents in the saturation region of the SiC BJT with a current gain of 71.

![Figure 3.15 BJT with conductivity modulation](image)

**Figure 3.15 BJT with conductivity modulation**

(b) **Common Emitter Current Gain**

Common emitter current gain is one of the most important parameters for SiC BJT application. For the recently fabricated SiC npn BJT, the common emitter current gain ($\beta$) of 4H-SiC BJT as a function of collector current density ($J_c$) has been investigated by pulse measurements and by device simulations. By using the pulse measurements with very low duty ratios, the BJT self-heating effect can be avoided.

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Common emitter current gain was measured using an experimental setup as shown in Figure 3.16. A pulse generator with rise and fall pulse time 5ns and 5µs pulse duration was used to supply the Base signal. The signal frequency of 20 Hz was used to eliminate self-heating effect. A commercial MOSFET driver [46] was used to increase the Base driving current. The signals in the Base and Collector circuits were measured with an oscilloscope. A fixed $V_{CE} = 25.3$ V was used to ensure that the transistor remained in its active region. The measured current gain as a function of collector current in a wide range is shown in Figure 3.17. Our simulation result is also shown in Figure 3.17, in which it shows that our model can perfectly describe the experimental result. As shown in Figure 3.17, $\beta$ decreases very fast as $J_c$ increase, this characteristic of SiC BJT will affect its application under high current density. Investigation on why this occurs is important for SiC BJT application.

![Experiment setup for measurement of $\beta$ as a function of collector current density](image)
Figure 3.17 Measured and simulated current gain vs the collector current density at 300K

Figure 3.18 shows a number of simulated curves of current gain as a function of collector current density. Curve ‘a’ is the measured result by the pulse measurement. Curve ‘b’ is the simulation curve with both the SiC/SiO\textsubscript{2} interface states traps and the BE junction epi-interface states traps (By curve fitting, a constant density of states $D_{IT}=7 \times 10^{10}$ cm\textsuperscript{2}eV\textsuperscript{-1} at the interface of SiC/SiO\textsubscript{2} and a constant density of states $D_{IT}=1.5 \times 10^{12}$ cm\textsuperscript{2}eV\textsuperscript{-1} at the Base-Emitter epi-interface were assumed at the mid-bandgap and a capture cross-section of $\sigma=6\times10^{-15}$ cm\textsuperscript{2} was used for both of them).

Curve ‘c’ is the simulation result that only the SiC/SiO\textsubscript{2} interface traps with the same density and capture cross-section were included. Figure 3.18, shows that with the BE junction epi-interface traps, the common Emitter current gain drops significantly among the whole collector current density range. It also shows that as $J_c$ increases, the gain difference between these two cases also increases. Curve ‘b’ matches the measured curve
‘a’ very well. From Figure 3.18, it is clearly shown that the epi-interface traps at the BE junction is the key factor that limit the current gain.

![Beta vs Jc](image)

Figure 3.18. Current gain vs collector current density

The aforementioned emitter size effect mentioned in section 2.3.1 is also an important reason for the lower current gain.

One important thing to point out is that although the current gain has potential to be significantly improved in the SiC BJT, the measured gain is already much higher than the conventional Si power BJT in both the saturation and the active regions. As shown in Figure 3.15, even in the saturation region, the BJT still has a current gain of 50, which is impossible for Si power BJTs because Si BJT must have a much large drift region hence much large base drive current in the saturation region.
(c) Forward I-V Characteristics at High Current Levels

Because of the limitation of a typical curve tracer in terms of maximum current capability, the I-V characteristics at very high currents cannot be measured using the curve tracer. However, the output characteristics at high current are very important for power electronics application. Therefore, in order to get the high current I-V characteristics pulse measurements were performed. The results are shown in Figure 3.19.

By the pulse test, the collector current up to 28A (1244A/cm²) was measured with a base current of 1A. As the current goes higher, the curves corresponding to different base currents start to separate in saturation region and a visible quasi-saturation region starts to appear, indicating conductivity modulation. The measured on-resistance at $I_B=0.9A$ and $I_C=10A$ is $3.8\, \text{m} \Omega \cdot \text{cm}^2$, significantly lower than that measured at lower base currents.

![Pulse test of IV Curves](image-url)
(4.5mΩ·cm² for I_B=0.4A, I_C=6.1A). The common emitter current gain as a function of collector current follows the same trend as our pulse gain measurement, which is shown in Figure 3.20. The difference between the current gains is because of the base width modulation due to the different V_CE.

![Figure 3.20 Beta vs Jc extracted from pulse IV curves](image)

(d) V_CE Offset Voltage

A collector to emitter several hundred millivolts offset voltage is observed in the SiC BJT, as shown in Figure 3.21. This offset comes from the different forward I-V characteristics of BE and BC junctions in the SiC BJT.
Figure 3.21 SiC BJT $V_{CE\text{OFFSET}}$

Figure 3.22 shows the measured forward I-V curves of the BE and BC junction of SiC BJTs at room temperature. It shows, for the SiC BJT, the BE junction has a greater junction voltage at the same forward drive current than the BC junction diode.

Figure 3.22 SiC BJT BE, BC junctions forward I-V curves
In [53], this difference is attributed to the high emitter contact resistance. According to the study here, the difference between the two diodes comes from the built-in potential difference due to the doping concentration difference. This is verified by the simulation of a simple pn diode with doping profiles corresponding to base, emitter and collector to present BE and BC diode respectively. The I-V results are shown in Figure 3.23. Both Si and SiC diodes show the voltage difference between BE and BC diode.

So, the $V_{ce}$ offset in the common emitter output characteristic is the potential difference caused by the doping concentration. In the following section, the build in potential was calculated according to the doping for Si and SiC respectively.

According to Eqn.(3.4), the build-in potential for BE and BC diode for Si and SiC are calculated and summarized in Table 3.1.

\[
\text{Build-in potential equation:} \\
V_{bi} = \frac{k \cdot T}{q} \ln\left(\frac{N_A \cdot N_D}{ni^2}\right) 
\] (3.4)
Table 3.1 Build-in potential and voltage offset of Si, SiC BE and BC diode

<table>
<thead>
<tr>
<th></th>
<th>$V_{biBE}$ (V)</th>
<th>$V_{biBC}$ (V)</th>
<th>$\Delta V$ @same $I_b$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>0.989</td>
<td>0.773</td>
<td>0.073</td>
</tr>
<tr>
<td>SiC</td>
<td>2.997</td>
<td>2.782</td>
<td>0.07</td>
</tr>
</tbody>
</table>

The built-in potential difference will cause the I-V characteristic difference between BE and BC diode for both Si and SiC BJT. Using the ideal diode Shockley equation expressed in Eqn.(3.5), the calculated I-V curves are shown in Figure 3.24. From Eqn.(3.5), the $\Delta V$ between BE and BC junction voltage drop at the same base current is demonstrated by Eqn.(3.6). The result for Si and SiC is shown in Table 3.1.

$$J = J_s \cdot (e^{qV/kT} - 1)$$  with  $$J_s = \frac{q \cdot D_p \cdot P_{no}}{L_p} + \frac{q \cdot D_n \cdot N_{po}}{L_n}$$  

(3.5)
\[ \Delta V = \frac{\ln \left( \frac{J_{sbC}}{J_{sbe}} \right) \cdot k \cdot T}{q} \] (3.6)

The measured I-V characteristic of Si BJT [54] is shown in Figure 3.25. An offset is also observed for Si BJT. BE and BC diode I-V characteristics are shown in Figure 3.26. Under the same base current, there is a voltage difference between BE and BC diode.
3.2.3 Power Loss Evaluation

Today, in converter applications, when the voltage rating is higher than 600V, Si IGBT is the preferred power device because of its superior current carrying capability compared
to Si power MOSFETs. As more promising SiC devices are developed, this situation will likely to change. The 1200V SiC BJT studied in this dissertation, not only overcomes the problem of the second breakdown issue found in Si BJT, but also has a better static and dynamic performance than a Si IGBT. Here, the static and switching characteristics of the SiC BJT at a bus voltage of 600V are measured by pulse experiments. Comparison of the total power loss is carried out with the state-of-the-art Si IGBT and it shows that SiC BJTs are very promising competitors to Si IGBT.

(a) Conduction Loss

The conduction loss of BJT depends on the conduction current and forward voltage drop. Figure 3.27 shows the forward voltage drop comparison of SiC BJT and Si IGBT. A state-of-the-art 1200V IGBT has been selected for comparison [48]. The IGBT has a forward voltage drop of 3.3V at Jc=100A/cm² while the forward voltage of the SiC BJT is only 0.59V, much smaller than the Si IGBT. This means the conduction losses in the SiC BJT will be much smaller than that of Si IGBT. One reason for this is that in Si IGBTs, the channel and the JFET regions’ resistance contributes to the total on-state resistance of the device, while there is no counterpart resistance in the SiC BJT structure. The 0.7 V turn-on voltage in the IGBT PN junction also results in an additional conduction voltage drop. Another important fact is that there is a much thinner and higher doped drift layer in the SiC BJT compared to a Si IGBT with the same blocking capability. Although the conduction modulation of SiC BJT is not as good as the Si IGBT,
the above merits allow it to have a much smaller on-state resistance and a lower conduction loss.

![Figure 3.27 Output characteristics comparison between SiC BJT and Si IGBT](image)

(b) Switching Characteristics

The SiC BJT switching characteristics were measured by double-pulse testing with a bus voltage of 600V. A MOSFET gate driver with a 2.5Ω base resistor was used to drive the base of the BJT. A SiC schottky diode [49] was used as a freewheeling diode. The test setup and the equivalent circuit are shown in Figure 3.28 (a) and (b), respectively. The turn-on and turn-off waveforms at a bus voltage 600V are shown in Figure 3.29 which show the fast turn on and turn off of SiC BJT.
Figure 3.28  Circuit and schematic of the switching test
Figure 3.29 Detailed SiC BJT switching waveforms

Figure 3.30 Turn off loss vs turn off current
The switching loss and the turn off time of SiC BJT as a function of turn off current are shown in Figure 3.30 and Figure 3.31 under the bus voltage 700V and inductive load conditions. The turn off time and turn off energy are both much smaller than the commercialized same rating Si IGBT [48]. In order to make it more clear, the same voltage rating Si IGBT [48] was also measured under the same test condition as SiC BJT. The same SiC schottky diode [49] was used as the free wheeling diode. The turn on and turn off losses of SiC BJT as a function of operating current are shown in Figure 3.32. The turn-off and turn-on losses of SiC BJT are both much smaller than those of Si IGBT as shown in Figure 3.33. For the IGBT during on-state, the minority carrier charge stored in the drift region causes the characteristic “tail” in the current waveform of the IGBT at turn-off. This tail increases the turn-off losses and increases the dead time between the conduction of two devices in a half-bridge. On the other hand, for the SiC BJT, the turn-off mechanism is different resulting in a MOSFET-like turn-off with no current tail. The
SiC BJT has a much shorter turn off time and better switching characteristics than Si IGBT. Figure 3.34 shows trade-off between the on-state voltage and turn off losses of the SiC BJT and Si IGBT. The BJT shows a figure of merit ($E_{off}V_{ce}$) that is 56 times greater than the IGBT.

![Figure 3.32 Turn on and Turn off losses vs operating current density for SiC BJT](image)

Figure 3.32 Turn on and Turn off losses vs operating current density for SiC BJT
Figure 3.33 Comparison of switching loss vs $J_c$ between SiC BJT and Si IGBT.

BJT, as a current driven device, the driver loss is higher than the voltage driven device. Moreover, for a Si BJT, usually a negative voltage is needed to turn the Si BJT off safely. The complex driver design makes the application of Si BJT even more unattractive.
However, a SiC BJT, as previously demonstrated, can be turned off successfully with zero base voltage. This is because of SiC BJT is free of second breakdown as we will discussed in chapter 4. This feature makes SiC BJT easier to use. In a typical application with a switching frequency of $f=10$ kHz and a duty-cycle of $D=0.7$, the IGBT [48] driver loss $P_{\text{driver,IGBT}}=Q_g \cdot V_g \cdot f=0.025W$. For SiC BJT under test, the driver loss, $P_{\text{driver,BJT}}=(I_b^2 \cdot R_b + I_b \cdot V_{be}) \cdot D=1.06 W$, with a $I_B$ of 400mA and $R_B$ of 2.5ohm. Other losses can be obtained from Figure 3.32, Figure 3.33 and Figure 3.34. In Figure 3.35, a total loss comparison at $J_c=100A/cm^2$ is shown. Although the driver loss of SiC BJT is much higher than Si IGBT, all other losses including the turn-on, turn-off, and conduction loss of 4H-SiC BJT are much smaller than Si IGBT, making the total loss of 4H-SiC BJT($E_{\text{total}} = 295.9 \mu J$) much lower than Si IGBT($E_{\text{total}} = 5342 \mu J$). A power electronics system equipped with SiC BJT will therefore have a much higher efficiency. The comparison shows that SiC BJT has much lower conduction and switching losses than Si IGBT. Moreover, a square RBSOA makes the SiC BJT more attractive for hard-switching applications. Although the loss penalty of driving a BJT with a base current is large compared to the IGBT driving loss, the total loss in the SiC BJT is much smaller than that of the Si IGBT. This makes the 1200V SiC BJT more attractive for switching applications than the 1200V Si IGBT.
3.2.4 Analysis of 1200V SiC BJT Inductive Switching

Previously, in section 3.2.2, we discussed that bipolar characteristics are not obvious in SiC BJT. So when discussing the switching characteristics, we can analyze SiC BJT in the similar way in which we discussed MOSFETs. The simplified model (as shown in Figure 3.36) can be used for switching model study. Since BE junction is forward-biased, the junction capacitance $C_{be}$ is mainly the diffusion capacitance. While BC junction is usually reverse-biased, the junction capacitance $C_{bc}$ is usually the depletion capacitance.
Figure 3.36 SiC BJT equivalent circuit used for switching analysis

(a) Turn on Process:

Figure 3.29 indicates the turn on period consists of the current rising period and the voltage dropping period. During the period when the current is rising, the diffusion capacitance, $C_{bc}$ is charged. Since the collector voltage stays the same as the bus voltage during this time period, $C_{bc}$ keeps the status as the BJT is off. During the periods when the voltage is falling, the collector voltage drops while the collector current stays constant for the load current. The depletion capacitance, $C_{bc}$ is discharged by a constant current. In this section, the rising and falling of current and voltage during turn-on and turn-off will be analyzed separately.

Current rising period

During turn on, the collector current increases as the charge on $C_{bc}$ accumulates. The diffusion capacitance is shown in Eqn.(3.7) [50], where $L_p$, $L_n$ are the diffusion length of
holes and electrons respectively. $P_{nobe}$ is the acceptor concentration in the base and $N_{pobe}$ is the donor concentration in the emitter. $V_{be}$ is the voltage across the BE junction. $kT$ is the thermal energy.

$$C_{be}(V) = \frac{q}{kT} \left( \frac{q \cdot L_p \cdot P_{nobe}}{2} + \frac{q \cdot L_n \cdot N_{pobe}}{2} \right) e^{\frac{qV_{be}}{kT}}$$ (3.7)

Figure 3.37 shows the diffusion capacitance $C_{be}$ as a function of BE junction voltage. $C_{be}$ has an exponential relationship with $V_{be}$. Before the turn on voltage of BE junction $V_o$, $C_{be}$ is very small. It takes almost zero time for $C_{be}$ to be charged to $V_o$. $V_{be}$ can be expressed as Eqn.(3.8). $V_B$ is the external base supply voltage, and $R_B$ is the equivalent base resistance during turn off. It includes external base resistance, driver resistance, BJT internal base resistance, and BJT emitter resistance. The collector current can be
expressed by Eqn. (3.9) as a function of time [50], where \( W_b \) is the width of base. \( D_n \) is the diffusivity coefficient of electrons in the base.

\[
V_{be}(t) = V_o + (V_B - V_o)(1 - e^{-\frac{t}{R_b C_b}})
\]  
(3.8)

\[
J_c = \frac{qD_n}{W_b} N_{pob} \cdot e^{\frac{qV_{be}(t)}{kT}}
\]  
(3.9)

During turn-on, the collector current rises as a function of time for analytical calculation and the real experiment are shown in Figure 3.38. This analytical result describes the collector current behavior during SiC BJT turn-on very well.

![Figure 3.38 IC rising during turn on](image_url)
From Eqn.(3.9), the collector rising speed $dJ_c/dt$ is a function of $J_c$ itself. So the higher $J_c$, the faster the collector current will rise. The SiC BJT was tested under bus voltage 600V, collector current 0.29A, 1.84A and 3.84A. Figure 3.39 shows the collector current rising as a function of time during turn-on at different load currents. As $I_c$ increases, the rising slope of $I_c$ becomes larger.

Concerning the above equations, factors that affect $I_c$ rising include: (a) charging current $I_b$ to diffusion capacitance $C_{be}$, which is decided by $V_B$ and $R_B$ -- the larger $V_B$ or the smaller $R_B$ is, the faster $I_c$ rises. And (b) $I_c$, the higher the load current is, the faster $I_c$ rises.

**Voltage falling period:**

Under the inductive load turn on, after the collector current rises to the load current, the collector-emitter voltage drop($V_{ce}$) starts to fall. The falling is realized by discharging the
depletion capacitance $C_{bc}$, $C_{bc}$ is the depletion cap as shown in Eqn.(3.10), where $N_c$ is the collector doping concentration.

$$C_{bc} = \sqrt{\frac{q \cdot N_c \cdot \varepsilon_0 \cdot \varepsilon_s}{2 \cdot V_{ce}(t)}}$$  \hspace{1cm} (3.10)

Discharging capacitance $C_{bc}$ can be expressed as Eqn.(3.11)

$$C_{bc} \cdot \left( \frac{d}{dt} V_{ce}(t) \right) = J_b - \frac{J_c}{\beta_{act}}$$  \hspace{1cm} (3.11)

The right side is the base current used to discharge $C_{bc}$. $\beta_{act}$ is the gain in active region. If we modify it, we can get Eqn.(3.12). $V_{bus}$ is the bus voltage.

$$\sqrt{V_{ce}(t)} = \sqrt{V_{bus}} - \frac{1}{\sqrt{2 \cdot q \cdot N_c \cdot \varepsilon_s \cdot \varepsilon_0}} \cdot \left( J_b - \frac{J_c}{\beta_{act}} \right) \cdot t$$  \hspace{1cm} (3.12)
The collector voltage falling as a function of time is presented by Eqn. (3.12). The analytical calculation and the real experiment are shown in Figure 3.40.

Eqn. (3.12) shows $dV_{ce}/dt$ is positively related to collector current density. The SiC BJT was tested under bus voltage 600V, collector current 0.29A, 1.87A and 3.84A. Figure 3.41 shows the collector voltage falling as a function of time during turn on at different load currents. As $I_c$ increases, the time for $V_{ce}$ to decrease becomes longer.
From above equations, factors that affect $V_{ce}$ falling are: (a) bus voltage ($V_{bus}$); the higher $V_{bus}$, the longer collector voltage falling time, (b) base current ($J_b$); the larger $J_b$, the shorter collector voltage falling time, (c) load current density ($J_c$), the larger $J_c$, the longer collector voltage falling time, and (d) current gain in active region ($\beta_{act}$); the larger of the gain, the shorter collector voltage falling time.

(b) Turn off Process:

Storage time is related to the excess charge. For SiC BJT, storage time is much shorter than voltage rising time. Similar to the turn-on process, the turn-off process can be treated as two periods. One is the voltage rising period during which the current keeps constant as the load current. The other is the current falling period, during which the current falls while the voltage keeps the bus voltage.
Voltage rising period

Similar to the turn on process, the voltage rising period is caused by the charging of the depletion capacitance $C_{bc}$. The voltage rising as a function of time is described in Eqn.(3.13), where $K\cdot J_c$ is the current that used to charge the $C_{bc}$, as shown in Figure 3.42. $V_f$ is the forward voltage drop. $V_{be}$ is the voltage required to keep the $(1-K)\cdot J_c$ current goes through emitter during the $V_{ce}$ rising.

$$\sqrt{V_{ce}(t)} - \sqrt{V_f} = \frac{\sqrt{2\cdot K\cdot J_c}}{\sqrt{q\cdot N_c \cdot \varepsilon_s \cdot \varepsilon_0}} \cdot (t)$$  \hspace{1cm} (3.13)

$$K\cdot I_c = \frac{V_{be}}{R_b}$$

Figure 3.42 Collector current path during turn off
The collector voltage rising as a function of time for analytical calculation and the real experiment are shown in Figure 3.43. From Eqn.(3.13), $V_{ce}$ rising speed is also positively related to collector current density $J_c$. The SiC BJT was tested under bus voltage 600V, collector current 0.82A, 5.26A and 11.28A. Figure 3.44 shows the collector voltage falling as a function of time during turn on at different load current. As $I_C$ increases, the time for collector to emitter voltage $V_{ce}$ to get to bus voltage is shorter.
From the above equation, factors that affect $V_{ce}$ rising are: (a) collector current density ($J_c$); the higher $J_c$, the faster $V_{ce}$ rising time, and (b) base resistance ($R_b$); the larger $R_b$, the longer the $V_{ce}$ rising time.

**Current falling time:**

After the voltage rising, there is still a voltage across capacitance $C_{be}$. This voltage is necessary to keep the collector current during the voltage rising time. The current dropping is realized by discharging the capacitance $C_{be}$ by the route shown in Figure 3.45.
The discharging of capacitance $C_{be}$ can be expressed by Eqn.(3.14), where $V_o$ is the turn on knee voltage of BE junction.

$$V_{be}(t) = V_o \cdot e^{\frac{-t}{R_b \cdot C_{be}}} \quad (3.14)$$

$$J_c = \frac{q \cdot D_n}{W_b} \cdot N_{pobe} \cdot e^{q \cdot V_{be}(t) \cdot \frac{1}{k \cdot T}} \quad (3.15)$$

Eqn.(3.15) shows the current density as a function of the voltage across the BE junction.

The collector current falling as a function of time for analytical calculation and the real experiment are shown in Figure 3.46.
Figure 3.46 Current falling during turn off

Figure 3.47 $I_c$ falling during turn off with different collector current
The SiC BJT was tested under bus voltage 600V, collector current 0.812A, 1.82A and 5.26A. Figure 3.47 shows the collector current falling as a function of time during turn on at different load current. As $I_c$ increases, $I_c$ decreases with a larger slope.

From the above equations, factors affect the $I_c$ falling are: (a) load current($I_c$); the higher $I_c$, the faster $I_c$ falling, and (b) base resistance($R_b$); the larger $R_b$, the longer $I_c$ falling time.
Chapter 4 Analysis of the Safe Operation Area (SOA) of SiC BJTs

4.1 Introduction

Power switches are frequently employed in hard-switching applications where the device is required to turn off high currents under inductive load conditions. In this topology, the power device is subjected to severe stress (a high current and voltage simultaneously) during turn-on and turn-off. The ruggedness of devices used in such applications is important, and a large safe operation area (SOA) for the devices is a desired feature. However, SOA, $V_{ce(on)}$ and $E_{on}$ (turn on loss) have conflicting requirements. A careful trade off must be performed between these three parameters.

4.2 RBSOA (Reverse Biased Safe Operation Area)

A large reverse biased safe operation area (RBSOA) is a desirable feature in order to turn off the device safely in such applications. In this section, the RBSOA of the SiC BJT will be discussed both theoretically and experimentally. For conventional Si power BJTs, turn-off switching results in current constriction leading to excessive current density in a small region of the device. The excessive current density results in device failure characterized by a rapid collapse of collector blocking voltage (second breakdown). Typically, the device is destroyed within nanoseconds after the voltage collapse.
For the Si BJT switch, the reason for second breakdown is usually characterized as the electric field shift from the BC junction to the n-/n+ junction. The current constriction to the middle of the emitter will cause the breakdown at collector n-/n+ junction at a much lower voltage. Such an avalanche is destructive because it injects holes (acting as the base current), resulting in more electrons injected from the emitter. This is called “Avalanche Injection” [44]. Because, during turn off, the current is constricted to the middle of the emitter, and because of the relative low n drift doping to sustain a required blocking voltage, the avalanche injection happens at a very low current density in Si high power BJT [45] hence resulting in a very small RBSOA.

4.2.1 Theory

The critical current that causes the second breakdown is expressed by Eqn (4.1).

\[
BV(J_c) = \frac{E_c^2}{\frac{-2 \cdot q}{\epsilon_0 \epsilon_r} \cdot (N_c - \frac{J_c}{q \cdot v_s})}
\]

(4.1)

Where \(E_c\) is the avalanche breakdown electric field (V/cm), \(\epsilon\) is the permittivity of the semiconductor (F/cm), \(N_c\) is the collector doping concentration (cm\(^{-3}\)), \(v_s\) is the electron saturation velocity (cm/s) and \(J_c\) is the collector current density (A/cm\(^2\)). It is important to note that during turn-off, the current distribution is not uniform. The current density \(J_c\) shown in Eqn. (4.1) is the localized collector current density underneath the middle of the emitter finger.
Figure 4.1 shows the relationship between localized current density and breakdown voltage at which point avalanche injection occurs for Si and SiC BJT. From Figure 4.1, it is clear that SiC BJT has a much higher avalanche injection critical current density than that of Si BJT. This means the SiC BJT is virtually free of second breakdown because the current density required to cause second breakdown is much higher than operation currents. This is a very important conclusion for SiC BJT because it eliminates one of the major factors as to why Si BJT is replaced by MOSFET and IGBT. Without the second breakdown, the failure mechanism for SiC BJT is the first breakdown (avalanche breakdown). At a higher current density, this breakdown voltage could be lower than the BV_{CEO} due to the false turn-on [44,45] of the transistor during turn off since the strong horizontal current flows under the emitter.

Figure 4.1 Si and SiC breakdown voltage vs collector current when avalanche injection occurs.
Inductive turn-off simulations on the 1200V SiC BJT similar to that reported by Cree were carried out using ISE TCAD[32] in order to understand the physics of the device operation.

![Collector Voltage and Current Waveform](image)

Figure 4.2 Turn off failure waveform because of false turn on at $V_{CE}=1600V$, $I_c=9A$

Figure 4.2 shows the failed turn-off collector voltage and current waveforms. The failure is caused by the horizontal flowing of the reverse base current, which will cause a lateral voltage drop across the base. If the lateral voltage drop across base-emitter junction is larger than the BE junction turn-on voltage, the BJT will be turned on again during turn off. Figure 4.3 shows the electron current flow after the turn-off failure. It shows that the middle part of the BJT was turned on. In this case, the BJT fails to be turned off at a very high current and high voltage condition.
4.2.2 Experimental Results

In order to verify the theory that predicts a very large RBSOA for the SiC BJT, switching experiments were carried out on a 1200V SiC BJT. The test setup and the equivalent circuit are shown in Figure 3.28. A simple MOSFET driver [46] in parallel with the base emitter junction is used to drive the BJT. Without applying a negative base voltage, SiC BJT can be successfully turned on and turned off.

Our experiment results show that this 1200V BJT can be safely turned off at 1100V, 67A (2990A/cm²), corresponding to 3.7 MW/cm² peak turn-off power density. The successful turn-off waveforms were shown in Figure 4.4. This is an extremely high power density indicating that no early “second breakdown” occurs. Due to limited device samples, we did not continue the testing into higher voltages.

A comparison of the RBSOA of a 1500V commercial Si BJT [47] and the tested SiC BJT is shown in Figure 4.5. Two Y axes in Figure 4.5 are in current density. There is orders of magnitude difference between them. The simulated RBSOA boundary caused by the false
turn-on is also summarized in Figure 4.5. This limitation is very large, so it is not a major issue when considering a SiC BJT’s RBSOA. Figure 4.5 clearly shows that SiC BJT has a much larger RBSOA than Si BJT. A square RBSOA of SiC BJT is demonstrated in our experiments; this robust turn-off capability makes SiC BJT more attractive for converter applications. This is the first reported SiC BJT RBSOA measurement. We did not observe false turn-on in the experiments although the simulations show this as an ultimate limitation on the RBSOA. Our bus voltage was around 1100V which is much lower than the bus voltage under the turn-off failure conditions in simulations; therefore the base width modulation is smaller, signifying a lower base resistance. It needs a much higher current to force the BJT to be turned on during turn-off.

![Figure 4.4 Single pulse measurement successful turn-off waveforms (Vce=1100v, Ic=67A)](image)

Figure 4.4 Single pulse measurement successful turn-off waveforms (Vce=1100v, Ic=67A)
Figure 4.5 SiC and Si BJT RBSOA comparison (ST2310FX was used for comparison)

4.3 Short-Circuit Performance of a SiC BJT

In applications where a system fault is possible, power switches are expected to have a minimum short-circuit withstand time. Short-circuit switching is one of the most severe stress conditions on the device, since a large current flows through the device while it is supporting the entire bus voltage. Short-circuit operation of a device over a long period of time will inevitably lead to device destruction. If the device can sustain a longer short-circuit condition, malfunction detection and protection in the system is easier to be designed. The Si IGBT has this short-circuit capability and typical short-circuit condition can last for 10 to 20µs. Many studies have been done to analyze the failure phenomena of the Si IGBT short-circuit failure mechanism [55-58]. Si power BJT, on the other hand,
does not have short-circuit capability due to existence of the so called forward biased second breakdown [20].

There are, in general, two destruction modes for power devices: the thermal mode and the electrical mode. Thermal destruction is caused by thermal runaway of the silicon chip. Electrical destruction occurs when power dissipation of the silicon chip exceeds a critical level. It is well known that the electrical destruction of Si power bipolar junction transistors (BJT) occurs when power dissipation in the chip is greater than 200 kW/cm$^2$ and caused by avalanche injection [59-62].

Based on that knowledge, SiC BJTs short-circuit capability was studied. 2-D simulation by ISETCAD was used to investigate the short-circuit capability limit. 2.25mm$^2$ is used, corresponding to the area of a 5A SiC BJT device. The cell structure used in the simulation is shown in Figure 4.6. 500µm N+ substrated was included and the ambient temperature was set at 300K.
4.3.1 Thermal Limit

Non-isothermal equations are incorporated into the device simulations to account for the device self-heating that results from high power loss involved during the short-circuit operation. Short-circuit was simulated for SiC BJT with $V_{ce}=600\text{V}$, $I_b=400\text{mA}$ and $T_{case}=300\text{K}$. Pulse width was set until it was long enough to destroy the device.
Figure 4.7 Transient simulation of different current density (solid lines) and maximum temperature (dashed lines) in the device (nonisothermal simulation). $V_{ce}=600V$, $T_{case}=300K$.

Figure 4.7 shows transient $J_c$ and maximum temperature $T_{MAX}$ waveforms. This figure indicates the $J_c$ starts to increase to a very large value when the temperature is beyond 2000K. Destruction occurs long after the power peak. Self-heating can be observed which is indicated by the decreasing of collector current with the increase of time. In the collector current $I_{c3}$ case, data at time points $t_1$ and $t_2$ were recorded. Please note the acceptor in the base has been completely ionized at both temperatures. As time increases, maximum temperature inside the cell increases, resulting in the reduction of the bandgap. As we know, the semiconductor bandgap decreases as the temperature increase, which will result in more recombination. The injection efficiency reduces as the temperature increases as shown in Figure 4.8. The destruction energy for three cases is shown in
Figure 4.9. In all cases, destruction occurs around the energy of 30 J/cm$^2$. This is a much larger value than the reported destruction energy value for Si IGBTs [58,64].

Figure 4.8 Current density distribution at different time points. (A cut along x=4.9µm)
Figure 4.9 Transient simulation of different current density (solid lines) and energy density (dashed lines) in the device (non-isothermal simulation). $V_{ce}=600V$, $T_{case}=300K$.

Figure 4.10 (a) shows one simulation result with three times marked. $t=t_1$ marks the time when the current is at its peak or the peak power dissipation point. $t=t_2$ marks the time when the current starts to rise. $t=t_3$ marks the time when the device fails. Figure 4.10 (b) shows the temperature distribution in the device at three time points. From $t_2$ to $t_3$, the temperature increases from about 2000K to 2500K and the device fails.
In order to investigate what happens in the BJT at 2000K, the BE junction diode of n+ emitter and p base was simulated at different temperatures. The results are shown in Figure 4.11.
The built-in potential of the SiC BJT BE junction pn diode decreases from 2.8V at 300K to 0V at 2000K. The temperature of the device increases and consequently the effective intrinsic carrier concentration ($n_{ie}$) inside the device increases according to Eqn.(4.2) [50].

$$n_i(T) = \sqrt{N_e(T) \cdot N_c(T) \cdot \exp\left(-\frac{E_g}{2kT}\right)} \quad (4.2)$$

At about 2000K, the intrinsic carrier concentration is about the same as the base background doping, as is the case with pure thermal failure.
4.3.2 Electrical Limit

The main contributing factor of Si BJT destruction is the avalanche injection while the thermal effect is considered to be secondary. However, in the case of SiC BJT, as Figure 4.7 shows the peak power dissipation is already as high as 1.5MW/cm². The device is destroyed long after the peak power point. From our RBSOA study, we saw that the avalanche injection happens at a much higher current density. Therefore, in the case of SiC BJT, the thermal effect is the first factor in device destruction.

4.3.3 Experimental Results

As we know, the ability of an IGBT to withstand fault currents can be improved by reducing the gate voltage applied to the device. Lower gate voltage reduces the saturation current magnitude which is the short-circuit current going through the circuit, resulting in the longer short-circuit sustainable time. Similarly, a lower base operating current of a SiC BJT will result in a lower collector current in short-circuit condition. However, there is a trade-off between the short-circuit withstand time and the transistor turn-on loss. The turn-off losses are not usually affected by the base current.

Before the short-circuit experiment was conducted, the $R_{on}$ and $E_{on}$ as a function of base current were tested, and the results shown in Figure 4.12. By considering turn-on loss and on-resistance, $I_b=400mA$ was chosen as the operating base current.
Figure 4.12 Experimentally obtained on-state resistance and turn-on loss as a function of base current. Main power supply = 600V, and case temperature = 300 K.

Figure 4.13 Short-circuit test circuit

The test circuit for short-circuit measurement was set as shown in Figure 4.13. The device under test was directly connected to a constant voltage supply whose voltage was set to 600V. Then 2-20µs base pulses were applied to the device. During the base on-pulse, the devices were driven into and stayed in the active region. At the end of the pulse,
the device was switched off. The base current was changed from 0A to 400mA. Under short-circuit load, the SiC BJT will be destroyed with a sufficiently long base pulse width at usual base operating conditions. Typical waveforms of this mode at standard conditions ($I_b = 400mA$, $V_{CE} = 600$ V and case temperature at start point, $T_{case} = 300$ K) are shown in Figure 4.14. Immediately after the base emitter junction was turned on, the $J_c$ shows saturation characteristics because the BJT works in the active region. At this point $V_{CE}$ has a constant about 600V and the collector current is about 12A. The energy dissipation per unit area is about 6.4J/cm$^2$. The short-circuit current is about 2.4 times of the rated current. This number is smaller than the typical Si IGBT value (5~6 times) [63,64]. For a similarly rated power devices, the SiC BJT is therefore expected to have a smaller short-circuit current which will result in less short-circuit power dissipation. In fact, the reduction of the short-circuit current allows both the device ruggedness and the maximum allowable short-circuit time to be enhanced, so the design of the protection circuit can be less critical.
Figure 4.14 Experimentally obtained short-circuit waveforms of non-destruction under a standard condition. Main power supply = 600 V, $I_B =400mA$, and case temperature = 300 K.

Figure 4.15 Experimentally obtained short-circuit waveforms of destruction under a standard condition. Main power supply = 600 V, $I_B =400mA$, and case temperature = 300 K.

For the above tested BJT, if the device was triggered into short-circuit condition again after a 20µs short-circuit test, a device failure was observed. The destroyed SiC BJT’s behavior under short-circuit condition is shown in Figure 4.15. In this case, the device is
not turned on at all and the collector current is zero when the base current increases to about 700mA. Such a failure was not observed if the device was repeatedly triggered into a short-circuit condition for less than 20µsec. The device could always be successfully turned off after the short-circuit tests.

The destroyed device exhibits a shorted BE junction and the BC junction is still good. No obvious damage can be visually observed on the device chip. Figure 4.16 shows the BE, BC junction characteristics after the device failure. BC junction is still good for both forward and reverse characteristics, whereas BE junction is shorted and behaves like a resistor.
For the first time, the limitation factors of short-circuit capability were investigated. It is found that – different from Si BJT and Si IGBT - the first limitation factor of SiC BJT is the thermal limitation. Simulation studies showed that the critical temperature of SiC BJT is about 2000K, at which point the BE junction is wiped out. This temperature limitation is much higher than the well-known Si devices temperature limitation (650K) [58].

For the first time, the short-circuit capability of SiC BJT was investigated experimentally. The device failed when the BE junction shorted and the whole device failed into an open
This is different from most Si power device failure phenomena in which the devices fail into a short circuit. This interesting failure phenomenon is a good protection for the entire system. However, the experiments did not agree with the simulation results which has predicted a much longer short-circuit withstanding capability. Possible reasons for this failure are as follows. The quality of the BE junction is not high since the emitter is fabricated by RIE etching. Etching will introduce a lot of defects along the interface as well as the mesa edge. This BE junction, fabricated by immature technology, is easier to be damaged under high current, high voltage, and high temperature stress conditions.
Chapter 5 Analysis of SiC BJT Degradation under Normal and Stressed Operating Conditions

5.1 Introduction

Studies presented in previous chapters demonstrate that the SiC BJT is a very promising power semiconductor switch. However, before the device can be commercialized, its long term reliability must be studied. It has been observed, that SiC BJTs show degraded DC characteristics after as little as 15 minutes of operation. Examples of such degradations are shown in Figure 5.1. The current gain reduces, the on-resistance in the saturation region increases, and the slope of the output characteristics in the active region increases or the Early Voltage decreases [65]. It is still unclear on what determines the degradation of SiC BJT and very few literatures are available on this topic.
5.2 Degradation Phenomenon Type I

In order to pinpoint the reasons for degradation, numerous experiments were carried out on the 1200V SiC BJT. Two types of degradation phenomena are observed: one is shown in Figure 5.2, where the family I-V curves collapse, and the other type is as shown in Figure 5.3, where the family I-V curves are similar with pre-stressed ones, with small R_{on} and current gain (β) changes after the degradation.
Figure 5.2 Degradation phenomenon type I

Figure 5.3 Degradation phenomenon type II
After stress, devices showing the type I phenomena were analyzed by electron-beam-induced current (EBIC) at University of South Carolina, after removal of all the contact metals and oxides. EBIC images were obtained by contacting the probe to the metal free base surface, grounding the collector and floating the emitter. The degraded device shows the high stacking fault activity in the BC junction as shown in Figure 5.4. Whereas samples showing the type II degradation phenomena show much less stacking fault activity. Therefore, if there is stacking fault activity in the device, after degradation, it will show the type I phenomena similar to that observed in the drift layer of a SiC PiN diode. In the case of the SiC PiN diode, degradation causes the forward voltage drop to drift to a much higher value [66,67,68]. In the PiN diodes, the energy needed for the expansion of the stacking fault comes from the electron-hole recombination in the conductivity modulated drift layer. The expanded stacking faults reduce the carrier
lifetime and lead to an increase in forward voltage drop. Similar to PiN diode, in the BJT base or collector, the recombination of electron-hole pairs can give rise to stacking faults when it is flooded with electron-hole pairs during the operation of the device, which can then reduce the lifetime of the minority carriers locally and resulting in the reduced current gain and the increased on-resistance [69].

5.3 Degradation Phenomenon Type II

Then what causes the type II phenomenon? In order to answer this, a series of experiments were carried out and several different effects on degradation were evaluated separately. The following effects were evaluated by the experiments:

(a) BE, BC junction effect;
(b) Time of stress effect;
(c) Stress current density level effect;
(d) BE spacing effect;
(e) Gummel plots;
(f) Temperature effect;

In experiments (a), (b), (c), and (d), small chip size test FATBJTs were used. As shown in Figure 5.5, the FATBJTs have a single emitter periphery of 800µm, with the active area 200µm×200µm. The possibility of having basal plane dislocations on such a small area is low so that the stacking fault activity can be eliminated in these experiments.
(a) BE, BC junction effect

The BC and BE junctions were stressed separately for two groups FATBJT to test effects on degradation by the BE and BC junctions. For device group A, BE and BC junctions were stressed successively under the same conditions as shown in Figure 5.6 (a). Device group B from the same wafer was chosen. BC junction was stressed first, and then BE junction was stressed as shown in Figure 5.6 (b). All stress conditions were under DC base current (I_b=100mA) for 15mins. At witnessed, the BC junction stress caused little or none degradation, whereas BE junction stress caused more degradation. The results did not change no matter what the stress sequence was.

So, it is concluded that the BE junction is more important during the degradation, possibly because the RIE etching induced defects at the emitter mesa cause more surface recombination when current is flowing through the BE junction.
(b) Stress time effect:

For FATBJT device group C, the BC junctions were stressed at $I_{bc}=100mA$ (250mA/cm²) for 10mins, 20mins and 30mins. As shown in Figure 5.7, there is no obvious change on
the family I-V curves as the stress time increases. These results indicate the BC junction and the top surface of the base region do not contribute much to the degradation.

![BC Junction Stress vs Time](image)

Figure 5.7 Time effect on BC junction stress

For the FATBJT device group D, the BE junctions were stressed from 10mins to 60mins with the BE junction current 100mA at room temperature. The family I-V curves were recorded every 10mins. As shown in Figure 5.8, current gain ($\beta$) decreases as time increases. The decreasing $\beta$ as a function of time is shown in Figure 5.9. The current gain continues to decrease with a reduced decreasing speed as time passes.

Again, it is clear that the BE junction contributes to the degradation much more than the BC junction. Since the surface is more related to the BE junction than the BC junction, it is suspected the defects or interface states at the surface will continue to be induced by
the stress, which will increase the surface recombination current, thereby reducing the current gain.

Figure 5.8 Time effect on BE junction stress

Figure 5.9 Beta as a function of time under the same base current
(c) Current level effect:

FATBJT group E was then stressed under the different current densities. The BE junctions were stressed for 30mins with the base emitter current density at 5mA (12.5A/cm²), 20mA (50A/cm²) and 100mA (250A/cm²) respectively. The results are shown in Figure 5.10.

Table 5.1 and Figure 5.11 show the increasing trend of current gain degradation as the stress current density increases.

![Current Density Effect On Degradation](image)

Figure 5.10 Stress current density effect on degradation

<table>
<thead>
<tr>
<th>I_{be} (A/cm²)</th>
<th>12.5</th>
<th>50</th>
<th>250</th>
</tr>
</thead>
<tbody>
<tr>
<td>Δβ @I_b=10mA</td>
<td>0.3</td>
<td>0.8</td>
<td>1.2</td>
</tr>
</tbody>
</table>
These results indicate that degradation is current density level related. Basically, the stress level can be evaluated by the time integral of the stress current or the charge [70]. The degradation level will increase as the stress level increases due to more surface recombination.

(d) BE spacing effect:

FATBJT with different spacing between emitter edge and the base p+ contact was designed and fabricated. The designed BE spacing is 3µm, 5µm, 7µm, 10µm and 15µm. These devices were stressed under the same condition: BE junctions were stressed with $I_{bc}=100$mA DC current for 10mins at room temperature. Figure 5.12 shows the pre-stress current gain as a function of BE spacing. The low current gain of the 3µm BE spacing
BJT is due to the implantation introduced defects as aforementioned. Table 5.2 and Figure 5.13 show $\Delta \beta$ as a function of BE spacing with the same base current.

Figure 5.12 Current gain as a function of BE spacing under the same base current

<table>
<thead>
<tr>
<th>BE spacing(µm)</th>
<th>3</th>
<th>5</th>
<th>10</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta \beta$ @Ib=7mA</td>
<td>4.857</td>
<td>3.428</td>
<td>2.143</td>
<td>2.071</td>
</tr>
</tbody>
</table>
These results indicate that for shorter BE spacing device, there are more chances for electron and hole pairs to be recombined at the surface. For longer BE spacing devices, the surface recombination is limited by the electron and hole supply since the surface recombination velocity is decided by the trap density, the cross-section for capture of electron and holes and the electron and hole concentrations at the surface [71]. Less surface recombination will cause less surface defects induction, and therefore, less degradation.

(e) Gummel plots

The NPN BJT Gummel plot shows the common-emitter transfer characteristics of the BJT in the forward active regime. The collector-emitter voltage, $V_{ce}$, is kept at a constant bias. The collector current, $I_c$, and base current, $I_b$, versus the base-emitter voltage, $V_{be}$,
are measured. The Gummel plot is a semilog plot of $I_c$ and $I_b$ (logarithmic scale) vs. $V_{be}$ (linear scale). This plot is very useful in device characterization because it reflects on the quality of the emitter-base junction. A number of other device parameters can be garnered either quantitatively or qualitatively directly from the Gummel plot: the DC current gain, base and collector ideality factors, and series resistances and leakage currents. The Gummel plot was recorded before and after stress of SiC BJT to investigate the quality of BE junction by Keithley Instruments. Figure 5.14 (a) shows the Gummel plot and Figure 5.14 (b) shows the family curves before and after stress of a 5A, 4kV SiC BJT. The stress condition was BE junction stress with collector open under DC current 3A for 30 minutes. The ideality factor of the collector current and the base current is 1 and 2 respectively. The high ideality factor of base is due to the interface traps at the base-emitter junction and surface. Also this figure shows that before and after degradation there is no change in the collector ideality factor, but there is an increase of the base ideality factor. The increase of base current can be explained by the stress-induced generation of traps in the SiC/oxide interface. The generated traps would enhance the surface recombination and tunneling and thus $I_b$ increases [79,80].
(f) Emitter size effect in degradation

From the above observation, it is possible that the surface quality is a key cause of type II degradation, especially in the mesa edge between the emitter and the base interface. SiC/SiO₂ interface has electrically active trap density centers at least two orders of
magnitude higher than Si/SiO$_2$ interface [72]. Emitter Size Effects were also
demonstrated in today’s SiC BJTs, and the surface recombination current was found to be
comparable with published results for Heterojunction Bipolar Transistors [73]. BJTs with
diameter width 10µm and 6µm on the same chip are fabricated at Cree. 6µm emitter width
(W$_E$) BJT has a larger emitter periphery over area (P$_E$/A$_E$) ratio. I-V characteristics
comparison between 10µm W$_E$ BJT and 6µm W$_E$ BJT is shown in Figure 5.15(a). It
shows 6µm W$_E$ BJT has the lower gain and larger R$_{on}$ due to more surface leakage
current.
The degradation caused by the stronger emitter size effect is similar to that caused by operational stress, as shown in Figure 5.15 (b).
Degradation experiments were conducted on two BJTs with different emitter width. After the initial measurements, the devices on wafers were stressed at 3.5A for a given amount of time. The devices were powered down, allowed to cool, and then the output characteristics were recorded. As shown in Figure 5.16, 10µm W_E BJT degraded less than 6µm W_E BJT, meaning that the surface does play a role in the degradation effect.
(g) Thermal effect and electrical effect separation

In order to understand if the self-heating is playing a role in the degradation, a pulse switching stress tests were performed. A fan and low switching frequency were used to ensure that there was no temperature rise. The common emitter output and BE and BC junction characteristics were recorded before and after the pulse stress. The total charge, expressed as Current $\times$ Time was used as the measurement of the stress. The total pulse stress is shown in Figure 5.17 and Figure 5.18, corresponding to 285 minutes under 10A DC current stress. Comparison of BE and BC junction characteristics before and after stress are shown in Figure 5.17. No obvious change is observed for these two junctions. However, there is obvious degradation in I-V characteristics of the BJT, as shown in Figure 5.18.

Figure 5.17 BE, BC junction I-V before and after pulse stress
The total degradation reported in [65] is the combination of electrical and thermal effects. Our results show that electrical stress alone can cause significant degradation.

Another set of experiments were conducted on two FATBJTs from the same wafer to test the thermal effect on degradation. They were stressed under room temperature and 200ºC separately. The stress condition was 150mA base-emitter DC current with collector open for 10 minutes. All of the family curves were recorded under room temperature. The results are shown in Figure 5.19. More degradation was observed for BJT degraded under 200ºC. This could be due to the thermal enhancement of the recombination induced defects effect [74]. This is consistent with the previous results.
Figure 5.19 Stress results under room temperature (a) and 200°C (b)
Figure 5.20 shows the Gummel plots measured from room temperature to 175°C for a 10μm BE spacing FATBJT. As the temperature increases, both the base and the collector currents increase. The ideality factor of the base current increases from 4.3 at room temperature to 5 at 175 °C. As we know, the ideality factor of the space charge recombination current is 2 [50]. This high ideality factor indicates the carrier tunneling mechanism at the base emitter and oxide interfaces [81,82].

5.3.1 Type II Degradation Summary

Experimental results discussed so far indicate that the possible mechanisms for type II degradation can be the increase of the surface recombination current and the surface defect assisted tunneling.
Another support to this conclusion comes from the recombination enhanced (or induced) defect reaction (REDR) theory [74]. The carrier capture or recombination processes at deep traps can induce or enhance dissociation and/or migration of the defect or impurity centers. The energy liberated by the electronic transition promotes the dissociation reaction athermally. The net amount of energy released during a recombination cycle is precisely the energy gap. So REDR is expected to be more powerful in the wide band gap semiconductors [75]. The hot electrons generated by Auger recombination are important in generating the interface states, and energy from such carriers is sufficient to create interface states [76, 15]. Due to the RIE etched mesa structure, the surface recombination current and perimeter tunneling current component [83] cause the emitter size effect of the SiC BJT. After stress, the increase of the interface states can increase the surface recombination and the tunneling current between base and emitter, which can be explained by more energy states within the forbidden gap to assist recombination and tunneling [78, 79].

5.4 Verification of Surface Recombination Factor on Degradation

Additional simulations were conducted to verify the effect of the surface recombination on the degradation. The pinning of the Fermi level at the surface of SiC and SiO₂ affects the physical properties of the system [72][77][84]. We analyze surface recombination in SiC BJT using the Shockley-Read-Hall(SRH) theory of recombination in the presence of Fermi level pinning due to surface states. So in our simulation, by matching with the real
experimental I-V curves, a constant density of traps $D_{IT} = 3.8 \times 10^{11} \text{cm}^{-2}\text{eV}^{-1}$ were assumed at the mid-bandgap for pre-stress devices. A capture cross-section of $\sigma = 6 \times 10^{-15} \text{cm}^2$ was used. $R_E$ was introduced as the emitter metal resistance.

Experiment I-V traces before and after stress with $I_B=200\text{mA}$ are shown in Figure 5.21. Simulation traces with different densities of interface traps are also shown in Figure 5.21. Also, in simulation, after stress, there is a minute increase of $R_c$ because of thermal effect.

A good matching with stressed device is obtained when the simulated trap density increases to $1 \times 10^{12} \text{cm}^{-2}\text{eV}^{-1}$. The agreement between the initial and stressed device demonstrates the applicability of physics-based device simulation to device reliability issues and verifies surface related recombination is a key factor in the degradation of the SiC BJT.

![Figure 5.21 Output Characteristics of SiC BJT before and after Stress (measurements and simulations)](image-url)
5.4.1 Extraction of Surface Recombination Factor Extraction

As discussed before, Emitter Size Effect was observed in the SiC BJT. This means the surface related recombination current cannot be ignored for today’s SiC BJT. So, the surface related recombination factor needs to be extracted and the result will then show whether there is an increase of the surface recombination factor. The extraction method can be found in [73].

The normalized periphery recombination base current $K_{B\text{surf}}$ is shown in Figure 5.22. It clearly shows $K_{B\text{surf}}$ increased after stress. This means the operation stress will cause the surface related recombination of SiC BJT to increase so that the current gain decreases and $R_{on}$ increases.

![Normalized periphery surface recombination current as a function of collector current density $J_C$ for conventional structure](image)

Figure 5.22 Normalized periphery surface recombination current as a function of collector current density $J_C$ for conventional structure
Some recommendations are provided here for solving the degradation issue of the SiC BJT. First, the material, n-drift layers grown with the hex etch basal plane dislocations (BPD) reduction process reduce the density of BPDs that propagate from the substrate into the epitaxial layers during growth [85]. The type I phenomenon can be mostly eliminated once the hex etched wafer is used. Second, regarding the surface, the quality of base emitter junction interface with the oxide is very important. Right now, the RIE process step will definitely introduce some defects at the base-emitter junction and at the surface, causing the severe problem of degradation. Therefore, the more mature SiC/SiO₂ interface process needs to be investigated.
Chapter 6 Monolithic Integration of SiC BJT With SiC Diode

In a typical power electronics converter such as that used to drive a motor in the electric vehicle, an anti-paralleled diode is always needed as the free-wheeling diode when the current flows in the reverse direction of the switch as shown in Figure 6.1. Power MOSFET-based converters have the flexibility of employing the reverse conducting body diode integrated in the device structure. However, such an integral diode is absent in the BJT hence necessitates the use of an external discrete diode. Compared with using two discrete devices, integrating a power switch and a freewheeling diode into a single chip can reduce the cost, size and packaging parasitics, and increase the reliability. In this chapter, a novel monolithically integration of SiC BJT with either a PiN or Merged PiN Schottky rectifier is proposed, designed and characterized. Process steps are described and compared with SiC BJTs.

Figure 6.1 Schematic configuration of bridge converter
**6.1 Device structure**

Monolithically, a rectifier can be integrated with a BJT by leaving the middle area of the total chip for realization of the rectifier. SiC BJT and the anti-parallel rectifier share the common terminals and high voltage termination.

**6.1.1 BJT+ PiN**

The conventional anti-paralleled diode is a PiN diode. The advantage of this approach is a low forward voltage drop due to the conductivity modulation during the forward conduction. The disadvantage is the long turn-off time needed to remove the excess carriers stored during on-state, resulting in a large reverse recovery current, slow switching speeds and large switching losses. However, compared with Si PiN, for the same blocking voltage, SiC PiN’s much higher doping concentration and much shorter thickness in the drift region make its reverse recovery current much smaller than that of a Si PiN diode. Figure 6.2 shows the proposed novel device schematic cross-section along the BJT and diode boundary. The p base is used as the anode of PiN. A trench filled with oxide is used to isolate the BJT and the diode. The edges of the trench bottom are protected by two implanted p belts as shown in Figure 6.2.
6.1.2 BJT+ MPS

Another diode structure, the Merged PiN Schottky (MPS) diode [20] was used to integrate with SiC BJT in order to achieve an even better trade-off between static and switching characteristics. The MPS combines the advantages of the PiN diode and the Schottky diode. Figure 6.3 shows the proposed novel device cross-section of the MPS diode together with the BJT. Titanium was used as the Schottky contact.
One important design parameter in the MPS is the Schottky opening window width as defined in Figure 6.3. The ISE TCAD numerical device simulator was used to optimize the design. According to Figure 6.3, a p+ belt is located at the boundary edge of the PiN and the Schottky contact in the diode. The simulation cell structure is shown in Figure 6.4. The doping profile of the p+ belt is shown in Figure 6.5. A 0.7µm p+ junction depth was assumed. In this design, at blocking voltage 1200V, the surface electric field value at the Schottky contact with different p+ spacing is shown in Table 6.1. The two p+ belts form the JFET region to protect the Schottky surface from the high electric field in order to reduce the leakage current. The smaller the window, the smaller the surface electric field. However, the smaller window will also introduce higher forward voltage drop, as shown.
in Figure 6.6. Considering both parameters, as well as the process feasibility, 5µm was chosen as the Schottky opening design.

![Figure 6.4 Cell structure used for MPS design](image)

![Figure 6.5 Doping profile of p+ belt in MPS](image)
### Table 6.1 Surface electric field value with different p+ space opening

<table>
<thead>
<tr>
<th>JBS Space (μm)</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>No P (only Schottky)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{\text{surface}}$(MV/cm)</td>
<td>1.12</td>
<td>1.24</td>
<td>1.30</td>
<td>1.35</td>
<td>1.47</td>
</tr>
<tr>
<td>$V_f$(V)@ $J_c=100A/cm^2$</td>
<td>1.065</td>
<td>0.980</td>
<td>0.967</td>
<td>0.95</td>
<td>0.895</td>
</tr>
</tbody>
</table>

![Figure 6.6 Trade-off curves with different schottky window opening](image)

#### 6.2 Device Fabrication

Prototype samples of the novel integrated device have been fabricated for 1200V blocking capability to demonstrate the integration concept. Compared to conventional SiC BJT, only one extra mask for a SiC BJT/PiN device is needed, and two extra masks are required for the SiC BJT/MPS device design. As a control, we also fabricated a conventional SiC BJT.

In Table 6.2, the main process steps and the comparison between BJT and the BJT/PiN device are outlined.
Table 6.2 BJT with PiN diode key process steps

<table>
<thead>
<tr>
<th>Mask name</th>
<th>BJT</th>
<th>BJT+PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Etch</td>
<td>Emitter</td>
<td>Emitter</td>
</tr>
<tr>
<td>BASE imp/ Base Etch</td>
<td>P+ for base contact</td>
<td>P+ for base contact/ P+ for diode area</td>
</tr>
<tr>
<td>Mesa etch</td>
<td>Active area</td>
<td>Active area, BJT/Diode area separation</td>
</tr>
<tr>
<td>JTE imp</td>
<td>JTE termination</td>
<td>JTE termination</td>
</tr>
<tr>
<td>Channel stop</td>
<td>Channel stopper</td>
<td>Channel stopper</td>
</tr>
<tr>
<td>JBS impl</td>
<td>nothing</td>
<td>Diode edge +Mesa edge implant</td>
</tr>
<tr>
<td>Aneal all</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ox (thermal + HTO)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal ox growth</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Econt</td>
<td>Emitter contact/ back contact</td>
<td>Emitter contact/ back contact</td>
</tr>
<tr>
<td>Annealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Base cont</td>
<td>Base ohmics</td>
<td>Base ohmics/ diode ohmics</td>
</tr>
<tr>
<td>Annealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Base metal</td>
<td>Base metal/ diode area</td>
</tr>
<tr>
<td>IMD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Open for emitter</td>
<td>Open for emitter</td>
</tr>
<tr>
<td>M2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PI</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

“JBS implantation” mask is needed for the BJT/PiN device to form the protection p+ belts at the boundary of the diode and the BJT.

The main process steps and the comparison between the BJT and the BJT/MPS device are mentioned in Table 6.3:
Table 6.3 BJT with MPS diode key process steps

<table>
<thead>
<tr>
<th>Mask name</th>
<th>BJT</th>
<th>BJT+MPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Etch</td>
<td>Emitter</td>
<td>P+ for base contact</td>
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<tr>
<td>BASE imp/ BaseEtch</td>
<td>P+ for base contact/ P+ for diode area</td>
<td></td>
</tr>
<tr>
<td>Mesa etch</td>
<td>Active area</td>
<td>Diode/BJT separation, MPS(PIN/schottky) area formation</td>
</tr>
<tr>
<td>JTE imp</td>
<td>JTE termination</td>
<td>JTE termination</td>
</tr>
<tr>
<td>Channel stop</td>
<td>Channel stopper</td>
<td>Channel stopper</td>
</tr>
<tr>
<td>JBS impl</td>
<td>nothing</td>
<td>Diode edge + PIN edge in MPS diode area+ Mesa edge implant</td>
</tr>
<tr>
<td>Aneal all</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ox (thermal + HTO)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal ox growth</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Econt</td>
<td>Emitter contact/ back contact</td>
<td>Emitter contact/ back contact</td>
</tr>
<tr>
<td>Anealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Base cont</td>
<td>Base ohmics</td>
<td>Base ohmics/ PIN ohmics</td>
</tr>
<tr>
<td>Annealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SBD contact</td>
<td>nothing</td>
<td>SBD contact for Schottky in MPS</td>
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<tr>
<td>Anealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Base metal</td>
<td>Base metal/ diode area</td>
</tr>
<tr>
<td>IMD</td>
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</tr>
<tr>
<td>Via</td>
<td>Open for emitter</td>
<td>Open for emitter</td>
</tr>
<tr>
<td>M2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PI</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Similar to BJT/PiN, a “JBS implantation” mask is needed to form the protection p+ belts. In addition, a “Schottky contact mask” is needed to form the Schottky contact in the MPS diode.

The layout of the integrated device is shown in Figure 6.7. Devices active area is 1.5mm by 1.5mm. The diode area is around 17.77% of the total area and located in the middle of
the device. The diode anode and BJT emitter are shorted by metal layer two and JTE is used as the total device termination.

![Figure 6.7 BJT integrated with different diode layout](image)

The detailed layouts at the boundary of the SiC BJT and integrated diode are shown in Figure 6.8 and Figure 6.9. For MPS, the area ratio between the PiN and Schottky diode is 50%.
Figure 6.8 Layout detail of SiC BJT/PiN diode

Figure 6.9 Layout detail of SiC BJT/MPS diode
6.3 Device Characterization

The fabricated devices were measured. Figure 6.10 shows, at room temperature, forward I-V of the integrated rectifiers. BJT/MPS device shows a little larger voltage drop than BJT/PiN device.

![I-V Characteristics](image)

Figure 6.10 I-V characteristics of the fabricated integrated diode

Figure 6.11 shows the I-V characteristics of the BJT with integrated diode at room temperature and at 200 °C. The current gain is about 53 for BJT/PiN and 56 for BJT/MPS, respectively, at room temperature. At 200 °C, BJT/PiN still has a current gain about 33 and BJT/MPS has a current gain about 36, which is much better than Si BJTs. It shows this design of BJT/diode does not negatively affect the BJT performance. Instead, it betters the performance to some extent, as shown in Figure 6.12. The benefit may come from the layout, where there is one more base bus line around the diode that will improve the base current distribution.
Figure 6.11 BJT/PiN Diode (a) BJT/MPS diode (b) family curves at room temperature and 200°C
The blocking characteristics of the control BJT and the BJT/Diode are shown in Figure 6.13. BJT/Diode devices show relatively lower BV_{ceo} than the control BJT. This might be because of the electric field crowding at the corner of the p+ belts which are designed to protect the boundary of the BJT and diode. In order to verify this, 2-D simulations using the ISETCAD [32] simulation tool were conducted. Figure 6.14 shows the cell structure used for blocking capability simulations at the boundary of BJT and diode. In real fabrication, the p+ belts implantation dose was around 5.4e14 #/cm^2, with the depth around 0.3µm. Figure 6.15 shows the simulated blocking capability BV_{ceo} of this design. Under these fabrication conditions, the simulated blocking voltage of the BJT/Diode device was about 1000V (50% activation rate was assumed). In order to see where the breakdown point is in this design, Figure 6.16 shows the leakage current path when the breakdown occurs. It demonstrates that the electric field crowding at the edge of the p^+ corner located at the boundary of the BJT and diode is the reason for early breakdown.
One way to solve this issue is to bring these two p belts closer and use higher energy implantation to realize the deeper p+ belts. When the distance between these two p+ belts is 2µm instead of 4µm, with a depth of 0.7µm, the BV\text{CEO} blocking result is shown in Figure 6.17, which is already above the 1200V designed blocking voltage.

![Figure 6.13 BVCEO of control BJT and BJT with different design of diode](image)

Figure 6.13 BVCEO of control BJT and BJT with different design of diode

![Figure 6.14 Cell structure used for SiC BJT/Diode breakdown study](image)

Figure 6.14 Cell structure used for SiC BJT/Diode breakdown study
Figure 6.15 Blocking capability of BJT/Diode in simulation

Figure 6.16 Leakage current flow lines when breakdown happens in simulation
The switching characteristics of the fabricated BJT/PiN and BJT/MPS devices are shown in Figure 6.18 and Figure 6.19, respectively. The test condition was bus voltage=600V and collector current=2.2A with an inductive load. Figure 6.20 shows (in terms of reverse recovery peak current), that the integrated MPS diode exhibits 36.4% reduction, and 30% reduction on the reverse recovery charge.
Figure 6.18 Turn off waveforms of switching BJT and reverse recovery of designed PiN diode

Figure 6.19 Turn off waveforms of switching BJT and reverse recovery of designed MPS diode
6.4 Summary

A novel power device that integrates an anti-parallel rectifier with the conventional SiC BJT has been introduced and successfully demonstrated. The design is very simple and easy to implement.

The forward static characteristics of BJT in the monolithic solution show the competitive performance compared to its discrete counterpart, whereas the blocking characteristics show some degradation. The possible reasons are analyzed using two-dimensional simulations and future improvement in design was proposed. Dynamic characteristics of the BJT/MPS demonstrated great improvement in reverse recovery peak current and total charge. This new integrated device is very attractive for power electronics applications.
Chapter 7 Novel New BJT Structures

Some new promising devices based on the studied SiC BJT are proposed in this section. Great performance was demonstrated through simulation studies.

7.1 Thick Emitter + Thin Emitter Structure

Until now, achieving higher common emitter current gain has been a major technical challenge in SiC BJT development. In this section, a novel BJT structure which improves the current gain of SiC BJT greatly is proposed. Figure 7.1 shows the novel structure. A 150Å thin n+ emitter is inserted between the extrinsic base and the oxide.

![Figure 7.1 Proposed thin+thick emitter structure](image-url)
7.1.1 Principle

The thin emitter in Figure 7.1 will introduce an emitter resistance horizontally, which will introduce a strong horizontal electric field in the thin emitter. The strong horizontal field will cause less hole injection to the surface, which will help to reduce the surface recombination. Figure 7.2 shows the voltage potential across the BE junction which equals the potential in the base minus the potential in the emitter. In the thin emitter region, the potential drop across the BE junction decreases from 2.85V at 5µm, the edge of the thick emitter, to 2.76V at 9µm, where it is close to the base contact. The BE junction’s potential drop in the extrinsic base is therefore smaller than that in the intrinsic base, resulting in smaller hole injection into the thin emitter, hence the surface region. In other words, the thin emitter acts like a passivation layer for the SiC/SiO₂ interface. For the conventional BJT, there is no barrier formed by the thin n+ emitter, supply of holes to the surface recombination centers is very easy.

![Figure 7.2 Voltage potential across the BE junction of conventional BJT and the proposed structure BJT](image)

Figure 7.2 Voltage potential across the BE junction of conventional BJT and the proposed structure BJT
Figure 7.2 also shows that the thick emitter region in the novel device is more forward biased than the conventional device and has a more uniform potential distribution than in the conventional case, resulting in a higher injection of electrons from the thick emitter region. This will reduce the on resistance and emitter current crowding effect.

Figure 7.3 shows the electron and hole current distribution along the cutline AB at Y=1.95µm as shown in Figure 7.1. The hole current density in the thin emitter is much smaller than that in the thick emitter, which is as we expected from the potential distribution. It should be noticed that the current density in the thin emitter is composed of the vertical current as well as the lateral current due to the two dimensional electric field.

![Figure 7.3 Electron and hole current distribution (Y=1.95µm cut, in the thin emitter)](image)
Figure 7.4 I-V characteristic of the proposed structure and the conventional structure

Figure 7.4 shows that the I-V characteristics comparison of the proposed novel structure and the conventional structure. It shows the proposed structure can achieve a much higher common emitter current gain and a smaller $R_{on}$ than the conventional structure.

### 7.1.2 Structure Optimization

The proposed novel BJT performance can be further improved by some additional optimizations. These improvements are investigated here.

(a) **Thin Emitter Width Effect**
Keeping the thick emitter width 5µm unchanged, and the thin emitter width was varied. The I-V characteristics with different thin emitter width are shown in Figure 7.5. Figure 7.6 shows the thin emitter width effect on current gain and the forward voltage drop.

Figure 7.5 Thin emitter width effect

Figure 7.6 Thin emitter width effect on current gain and the forward voltage drop
As the thin emitter width increases from 2 µm to 5µm, the current gain increases while the forward voltage drop decreases. This is because as the thin emitter width increases, more of the total area works as the emitter. When the thin emitter width increases from 5 µm to 8µm, not much change in the current gain and forward voltage drop is observed. This is because when the thin emitter is too wide, the current spreading effect in the collector counteracts the benefit from the thin emitter.

(b) Thick Emitter Width Effect

Keeping the thin emitter width 5µm unchanged and the thick emitter width was varied. The I-V characteristics with different thick emitter widths are shown in Figure 7.7.

Figure 7.7. I-V with different thick emitter width
Figure 7.8 shows the thick emitter effect on current gain. As the thick emitter width increases from 2 µm to 5µm, the current gain increases. When the thick emitter width increases from 5 µm to 8µm, there is not much change in gain. This is because as the thick emitter width increases, the middle part of the emitter will become less and less forward biased and thus contributes less to the total current gain.

(c) Thin Emitter Thickness

In this proposed structure, the thickness of the thin emitter is a key parameter, it cannot be too thick, otherwise, the lateral emitter resistance will be too small to be effective in reducing hole injection. Figure 7.9 shows the current gain as a function of thin emitter thickness. As the thin emitter thickness increases, the gain decreases. However, even when the thickness increases to 0.2µm, the current gain is still much higher than the
conventional structure. A thicker thin emitter makes the proposed device more practical to make. Since the distance from the thin emitter to the base contact is short, the implantation induced defects which are not included in simulations have to be considered in this case. To eliminate the implantation damage, a regrowth base contact is recommended.

![Beta as a function of thin emitter thickness](image)

Figure 7.9 Beta as a function of thin emitter thickness

**Figure 7.9 Beta as a function of thin emitter thickness**

(d) **Equivalent Circuit of the Novel BJT**

Figure 7.10 shows the equivalent circuit of the proposed structure. $R_{E1}$ introduced by the thin emitter helps to realize the higher potential distribution in the intrinsic base, which helps to increase the current gain. $R_{suf}$ is introduced to present the surface leakage current. $R_{E1}$ and $R_{suf}$ usually are not in a conventional BJT model. If the $R_E$ is adjusted to be in a
distribution mode, the emitter current crowding can be completely relieved. However, that will also increase the fabrication complexity and cost.

![Figure 7.10 Equivalent circuit of the proposed structure](image)

**7.2 Double Epitaxial Base Structure**

We know from section 2.3.5 that the space between the base contact and the emitter cannot be too small in order to get rid of the effect of the implantation introduced defects at the base contact. However, a large BE spacing will introduce a large extrinsic base resistance, which can induce a locally forward biased base collector junction and a premature current from the base to collector at on-state. This will increase the on-state collector-emitter voltage, and the effect becomes more severe for low current gains [94].
In order to solve the problem, a double epitaxial base structure is proposed. Figure 7.11 shows the proposed structure. After the emitter etching process step, a highly doped p+ layer is epi grown on top of the conventional p base. This highly doped p+ layer has a much smaller resistance than the conventional extrinsic base resistance. Base current from the base contact will prefer to flow through the p+ base resistance.

Figure 7.11 Proposed double epitaxial base structure
Figure 7.12 shows the I-V comparison between the double epi-base and the conventional structures. It clearly shows that the proposed structure has a much higher current gain and smaller $R_{on}$ than the conventional structure. The reason for the difference can be explained by Figure 7.13. It shows the lateral potential distribution in the base for double epi-base and conventional structures. For the double epi-base structure, there is almost no voltage drop from the base contact to the emitter edge (from 12.5µm to 5µm). For the conventional structure, most of the base voltage is dropped in the extrinsic part. This results in the higher base forward voltage in the intrinsic base region in the double epi-base structure, resulting in high current gain and low $R_{on}$ as shown in Figure 7.12.
7.2.1 Structure Optimization

After discussion of the working principle, some important structure parameters will be investigated here.

(a) Epi-p+ base thickness

The thicker the p+ epi-layer, the smaller the resistance. Since this proposed structure favors the small resistance of the second p+ epi-base, it is expected that a thicker p+ epitaxial extrinsic base should result in a better performance. However, Figure 7.14
shows the opposite results. The structure with 0.1µm epi-p+ layer has a much better performance (higher current gain and smaller $R_{on}$).

![Figure 7.14 I-V comparison between structures with different thickness of epi-p+ layer](image)

This can be explained by Figure 7.15. At the sidewall of the emitter, the interface of the epi-p+ layer and the emitter forms a parasitic diode that does not contribute to the BJT operation. We want to keep the diode area as small as possible. The 0.5µm thickness epi-p+ structure has a diode area 5 times of that in the 0.1µm thickness epi-p+ structure. Moreover, in both cases, $R_{epi}$ (epi-p+ layer resistance) $\ll R_{ext}$ (extrinsic base resistance), then the parasitic diode will dominate the ultimate performance.
(b) Second epi-p base doping

The key point of this proposed structure is the $Repi << Rext$ so that the conventional extrinsic base can be bypassed. The doping concentration of the second epi-p base layer cannot be too low.
Figure 7.16 helps to illustrate this. Second epi-p layer with 0.1µm thickness and the doping concentration of 1e16 cm\(^{-3}\), 6e17 cm\(^{-3}\), and 8e18 cm\(^{-3}\) are simulated and compared.

\[
R = \rho \frac{L}{S} = \frac{1}{nq\mu} \frac{L}{S}
\]  
(7.1)

By Eqn.(7.1), the extrinsic base resistance \(R_{\text{ext}}=0.789\Omega\) can be obtained. The epi-p+ base resistance, \(R_{\text{epi}}\) is 35.9 \(\Omega\) and 0.045 \(\Omega\) for the second epi-p layer with doping concentration 1e16 cm\(^{-3}\) and 8e18 cm\(^{-3}\) respectively. For the 1e16 cm\(^{-3}\) case, there is no benefit from the second epi-p layer base. That is why in Figure 7.16, 1e16 cm\(^{-3}\) doped epi-p layer has a worse performance than the conventional one.
Chapter 8 Conclusions and Plan of Future Study

8.1 Major Contributions

Compared with other bipolar devices like SiC IGBT and SiC GTO, SiC BJT does not need to overcome the junction voltage in order to conduct current. Also, SiC BJT does not involve oxide reliability and process complexities associated with SiC MOSFETs. Therefore, SiC BJT is a very promising high-power switching device that worth detailed investigation and study.

The research work presented in this dissertation, documented detailed investigation of 1200V SiC BJT devices, using numerical models and experiments. Various devices are designed and fabricated through the partnership with Cree Inc. Major contributions of the research work are:

1) Development of an accurate numerical model for the SiC BJT

For the first time, an accurate numerical simulation models was developed and calibrated for the 1200V SiC BJT. The model, for the first time, accurately accounts for the contribution of surface recombination. Through the use of the developed model, design parameters including emitter thickness, emitter doping, emitter width, base doping, and the spacing between emitter edge and p+ implant were decoupled and optimized separately. The optimal value for each parameter was obtained for a specific breakdown voltage. In the emitter width design, the Emitter Size Effect was demonstrated for the first time and the surface recombination factor was extracted.
2) *A base resistance model was developed for large area BJT design*

A base resistance model was developed to evaluate the layout of large area BJTs. Based on this model, the large current rating device layouts were compared and analyzed. This model can be used to study large-scale SiC BJT or some other devices. This study showed that the layout would affect the current distribution among the device greatly, thereby affecting the dynamic characteristics and the reliability of the device.

3) *First ever demonstration of the absence of second breakdown in SiC BJT*

The absence of second breakdown and a square RBSOA was demonstrated theoretically and experimentally for the first time for the 1200V SiC BJT. This is a very important contribution, since it eliminates one of the most important reasons why Si BJT was replaced by Si MOSFET and Si IGBT. For the first time, the SiC BJT short-circuit capability was also demonstrated. Simulation study showed the theoretical limit of short-circuit capability can be as high as 30J/cm², much larger than silicon power devices.

4) *Comprehensive investigations of SiC BJT degradation issue*

The reliability issue of SiC BJT was studied. Two degradation phenomena under the operational stress were observed and classified. A number of related experiments were designed and conducted. And from these experiments, causes for the degradation were proposed. The basal plane dislocation was proposed to be the mechanism causing the family curves collapse, while the surface recombination current induced defects effects was identified as the mechanism of the type II degradation phenomena. The contribution made in this part of research paved the way for the final commercialization of SiC BJT.

5) *First ever demonstration of monolithic SiC BJTs with integral diode*
The monolithic solution of SiC BJT with SiC diode was proposed, designed, fabricated and characterized. The integrated diode showed good forward I-V curves and showed excellent improvement in reverse recovery current. The reduced parasitic would increase the system reliability and size.

6) Innovative device structures to achieve current gain exceeding 100

Two innovative device structures were proposed and studied. These devices have potentials to deliver a current gain of more than 100, significantly widening SiC BJT’s appeal to various applications.

### 8.2 Future works

The research discussed in this dissertation lays the groundwork for a number of future works. First, power electronics application study using the developed BJT can be accelerated. Second, the new proposed BJT/Diode device can be optimized and implemented for real commercial applications.

The thesis contains recommended fabrication method to achieve degradation-free SiC BJT. Experimental verification is needed. The two proposed new structures showed very promising characteristics. These new structures can be considered for fabrication and characterization.
References


2. Juan Carlos Balda, Fred Barlow, Alexander B. Lostetter, Alan Mantooth “Silicon-Carbide (SiC) Electronics”

3. Cree Inc. website www.cree.com


10. Tsunenobu Kimoto, Hajime Kosugi, Jun Suda, Yosuke Kanzaki, and Hirohiku Matsunami, “Design and Fabrication of RESURF MOSFETs on 4H-SiC(0001), (11-20), and 6H-SiC(0001)” IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, NO. 1, JANUARY 2005


14. Ranbir Singh, Member, IEEE, Sei-Hyung Ryu, Member, IEEE, D. Craig Capell, and John W. Palmour, Member, IEEE “High Temperature SiC Trench Gate p-IGBTs” IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 3, MARCH 2003

204


21. Yi Tang, Jeffrey B. Fedison and T. Paul Chow,” High-Voltage Implanted-Emitter 4H-SiC BJTs” IEEE ELECTRON DEVICE LETTERS, VOL. 23, NO. 1, JANUARY 2002


28. Y. Li, et. al” High-Voltage (3 kV) UMOSFETs in 4H-SiC’ IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 49, NO. 6, JUNE 2002

29. Sei-Hyung Ryu,et.al “10-kV, 123-m cm2 4H-SiC Power DMOSFETs” IEEE ELECTRON DEVICE LETTERS, VOL. 25, NO. 8, AUGUST 2004


31. Naruhsa Miura,et.al “Successful Development of 1.2 kV 41-SiC MOSFETs with the Very Low On-Resistance of 5 mQcm²” Proceedings of the 18th International Symposium on Power Semiconductor Devices & IC's 2006. Page(s):1 - 4

32. ISE TCAD Release 10.0 manual


37. Sang Youn Han, et al. ‘Interpretation of Fermi level pinning on 4H-SiC using synchrotron photoemission spectroscopy’ APPLIED PHYSICS LETTERS VOLUME 84, NUMBER 4 26 JANUARY 2004


46. Datasheet Microchip TC4420/29

47. Datasheet ST2310FX, High Voltage Fast-Switching NPN Power Transistor.

48. Datasheet IRGP20B120U-E
49. Datasheet Cree CSD06060


51. Xiaojun Xu; Huang, A.Q.; Yan Gao; Zhong Du; Agarwal, A.; Krishnaswami, S.; Sei-Hyang Ryu; 400kHz, 300W SiC BJT Based High Power Density PFC Converter” IEEE Power Electronics Specialists Conference, 2006 page(s) 1-5.


54. Datasheet STHD1750FX


73. Yan Gao, Alex Q. Huang, Sumi Krishnaswami, Anant K. Agarwal, Charles Scozzie ‘Emitter Size Effect in 4H-SiC BJT’ IPEMC 2006


77. Sang Youn Han, et al ‘Interpretation of Fermi level pinning on 4H-SiC using synchrotron photoemission spectroscopy’ APPLIED PHYSICS LETTERS VOLUME 84, NUMBER 4 26 JANUARY 2004


91. Yanbin Luo, et al, “High Voltage (>1 kV) and High Current Gain (32) 4H-SiC Power BJTs Using Al-Free Ohmic Contact to the Base” IEEE ELECTRON DEVICE LETTERS, VOL. 24, NO. 11, NOVEMBER 2003


93. Santhosh Balachandran, “4 kV 4H-SiC Epitaxial Emitter Bipolar Junction Transistors” IEEE ELECTRON DEVICE LETTERS, VOL. 26, NO. 7, JULY 2005