ABSTRACT

JUR, JESSE STEPHEN. Lanthanide-based Oxides and Silicates for High-κ Gate Dielectric Applications. (Under the direction of Angus I. Kingon.)

The ability to improve performance of the high-end metal oxide semiconductor field effect transistor (MOSFET) is highly reliant on the dimensional scaling of such a device. In scaling, a decrease in dielectric thickness results in high current leakage between the electrode and the substrate by way of direct tunneling through the gate dielectric. Observation of a high leakage current when the standard gate dielectric, SiO_2, is decreased below a thickness of 1.5 nm requires engineering of a replacement dielectric that is much more scalable. This high-κ dielectric allows for a physically thicker oxide, reducing leakage current. Integration of select lanthanide-based oxides and silicates, in particular lanthanum oxide and silicate, into MOS gate stack devices is examined. The quality of the high-κ dielectrics is monitored electrically to determine properties such as equivalent oxide thickness, leakage current density and defect densities. In addition, analytical characterization of the dielectric and the gate stack is provided to examine the materialistic significance to the change of the electrical properties of the devices.

In this work, lanthanum oxide films have been deposited by thermal evaporation on to a pre-grown chemical oxide layer on silicon. It is observed that the SiO_2 interfacial layer can be consumed by a low-temperature reaction with lanthanum oxide to produce a high-quality silicate. This is opposed to depositing lanthanum oxide directly on silicon, which can possibly favor silicide formation. The importance of oxygen regulation in the surrounding environment of the La_2O_3-SiO_2 reaction-anneal is observed. By controlling the oxygen available during the reaction, SiO_2 growth can be limited to achieve high stoichiometric ratios of La_2O_3 to SiO_2. As a result, MOS devices with an equivalent oxide thickness (EOT) of 5 Å and a leakage current density of 5.0 A/cm^2 are attained. This data equals the best value achieved in this field and is a substantial improvement over SiO(N) dielectrics, allowing for increased device scaling.

High-temperature processing, consistent with the source/drain activation anneal in MOSFET processing, is performed on lanthanum-silicate based MOS devices with Ta or

TaN gate electrodes and a W metal capping layer. The thermal limit of Ta is observed to be less than 800 °C, resulting in a phase transformation that can result in uncontrolled shifting of the MOS device flat-band voltage. TaN is observed to be more thermally stable (up to 1000 °C) and results in an increase in the capacitance density suggesting that it impedes oxygen reaction with silicon to produce SiO_2. It is later observed that a W metal capping layer can serve as a high-oxygen source, which results in an increased interfacial SiO_2 formation. By limiting the oxygen content in the W capping layer and by utilizing a thermally stable TaN gate electrode, control over the electrical properties of the MOS device is acquired. To determine the stability of amorphous lanthanum-silicate in contact with investigated by means of back-side secondary ion mass spectroscopy profiling. The results are the first reported data showing that the lanthanum incorporated in the silica matrix doe not diffuse into the silicon substrate after high temperature processing.

The decrease in the device effective work function ($\phi_{M,eff}$) observed in these samples is examined in detail. First, as a La_2O_3 capping layer on HfSiO(N), the shift yields ideal-$\phi_{M,eff}$ values for nMOSFET deices (4.0 eV) that were previously inaccessible. Other lanthanide oxides (Dy, Ho and Yb) used as capping layers show similar effects. It is also shown that tuning of $\phi_{M,eff}$ can be realized by controlling the extent of lanthanide-silicate formation. This research, conducted in conjunction with SEMATECH and the SRC, represents a significant technological advancement in realizing 45 and sub-45 nm MOSFET device nodes.

LANTHANIDE-BASED OXIDES AND SILICATES FOR HIGH-κ GATE DIELECTRIC APPLICATIONS

By

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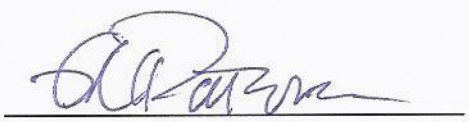

Gregory Parsons
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BIOGRAPHY

Jesse Stephen Jur was born on January 18th, 1979 as the youngest of seven children to parents Dr. Tim and Sarah Jur in Columbia, South Carolina. Being from such a large family, he learned the value of family and working as a unit to accomplish goals, while at the same time always seeking to create an individual identity.

His interest in science was founded at an early age, engaging in research for science fair projects that culminated into invitations to the International Science and Engineering Fair in 1996 and 1997. Jess graduated from Brookland-Cayce High School in 1997 and subsequently began his college career at The University of South Carolina in the Chemical Engineering department. At USC, Jess was provided with opportunities to conduct research in the area of Li-batteries, fuel cells, and supercritical carbon dioxide. His work with supercritical CO_2 led to an invitation to spend a summer with IBM research at the T.J. Watson research facility in New York in 1999. His experience at IBM led to three patents, the first of which was submitted at the age of 20. Jess was awarded an Energy Research Undergraduate Laboratory Fellowship from Lawrence Berkeley National Laboratory in 1999. At LBNL, Jess spent a year on various projects including a global project to search for physical evidence of neutrinos by way of double-beta decay. Enjoying his time in California, Jess embarked on a summer internship in the summer of 2001 working for Nanogram Corporation in San Jose, CA.

During Jess's undergraduate career, his willingness to participate in research projects from SC to NY to CA provided him with wonderful experiences and opportunities including living in the Bronx and in Berkeley, making friends, exploring a number of research avenues, and attending a number of conferences. Jess returned to The University of South Carolina to complete his undergraduate degree in the fall of 2001. After graduation, and prior to beginning his doctorate at North Carolina State University, Jess worked as a Process Development Engineer at NanoGram Corporation. Jess then a Masters in Chemical Engineering at Johns Hopkins University (2003). At JHU, Jess worked on a project doing density function theory of liquid membranes under the advisement of Prof. Marc Donohue.

Jess's work experience at NanoGram Corp. and graduate research assistantship at JHU, helped him realize that he favored applied research. This set in motion his pursuit of a Ph.D. at North Carolina State University in the Department of Materials Science and Engineering. Before moving to North Carolina to begin graduate school, Jess married Ardath Paige Presler on July 17, 2004. Paige and Jess have made their home in Raleigh for the past three years, where Paige, sharing the love of research, is a chemical engineer employed at RTI International.

Under the advisement of Prof. Angus Kingon and with much help from Dr. Dan Lichtenwalner and Prof. Jon-Paul Maria, Jess has focused his work on studying properties of lanthanide-based high-k dielectric materials for high-end transistor devices. Always enticed by interesting research opportunities, Jess jumped at the chance to work with AMD at IBM's 300 mm device fabrication facility in Fishkill, NY in the summer of 2006. While with AMD, Jess investigated the use of laser spike anneal processing on high-κ/metal gate stacks.

During his doctorate career, Jess has enjoyed spending his free time competing in the Raleigh Dart League where he was named to the division all-star team in multiple seasons, playing golf with his friends and family, and being the vice president of the local University of South Carolina Alumni Association. After receiving his Doctorate of Philosophy from North Carolina State University in August of 2007, Jess has accepted a joint post-doctoral position with Dr. Mark Johnson, of NCSU, and two entrepreneurial technologies companies, Kyma and Semprius.

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I would like thank the contributions from a number of research groups for their efforts in analytical characterization. Namely, Drs. Frank Zhu, Fred Stevie and Robert Garcia from NCSU (SIMS); Prof. Susanne Stemmer, Melody Agustin, Yan Yang, and Joel Cagnon from UC Santa Barbara and Prof. Gerd Duscher, Fude Liu, and Viera Vankova from NCSU (HRTEM and EELS); Prof. Eric Garfunkel, Dr. Torgny Gustafsson and Lyudmile Goncharova from Rutgers University (MEIS). I would like to especially recognize Dr. Stevie and Prof. Maria for who educated me on XPS and XRD, respectively.

There's one person in particular to whom I owe a debt of gratitude: my spouse, Paige. She experienced the ups and downs, late nights and early mornings, beside me at all times. Her steadfast support and advice provided me with what I needed on a day-to-day basis to finish my degree.

I consider myself very lucky to have had constant support and guidance from my parents, Dr. Tim and Sarah Jur, and my wonderful family throughout my life. I would not have developed such a strong work ethic nor found my love of science and engineering without each of them. With such a strong family network, life's challenges have not appeared so challenging. Finally, Joe Jur and Ian Carlton, my best friends in life who have always been the constants in my life when all else is ever changing. Thank you all for assisting me in achieving my doctorate in Materials Science and Engineering and getting me to where I am today.

The last 3 years of my doctorate experience would have been drastically different if I not had the support of my friends and classmates. In particular, I would like to thank Spalding Craft, Jon Ihlefeld, Mark Losego, Patrick Daniels, Seyman Aygün, Peter Lam, Michelle Casper, Erin Gross, Chris Oldham, Matt Walker, and Brian Laughlin. Due in part to these people, my pursuit of a doctorate degree will always be thought of as one of the best times in my life.

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1. INTRODUCTION

This dissertation details the development of lanthanide-based oxides and silicates for use in future generation metal-oxide-semiconductor field effect transistor (MOSFET) devices. The research presented in this dissertation was originally part of a collaboration with the Semiconductor Research Corporation Front End Processing Center (Task ID: 616.026). This project, started in 1997, was tasked to identify front end processing issues associated with the implementation of a high-κ dielectric and a metal gate into standard MOSFET processing. The term of the project ended in 2006. Since that time, the research was based on direct collaboration with SEMATECH Corp. and member companies.

In order to scale down the dimension of high-end MOSFET devices, the use of an alternate gate dielectric with a higher dielectric constant is necessary because leakage currents through sub-1.5 nm SiO_2 films are undesirably high. However, the integration of such a high-κ material has many identified and unidentified deleterious effects that make their use in a commercial devices still premature. It is thought that intermixing the high-κ dielectric with the natural SiO_2 oxide can serve as a route for the gradually insertion of the high-κ into the MOS gate stack. This work identifies processing and materialistic issues with lanthanide based-oxides, in particular the use of lanthanum oxide. Justification for the use of lanthanide-based oxides and silicates over that of hafnia-based oxides is provided.

1.1 Outcomes

The research presented in this dissertation resulted in the following technical outcomes:

1) A unique process for reaction between a La_2O_3/SiO_2 bi-layer to form a homogenous and amorphous lanthanum silicate layer was developed to retain the enhanced dielectric properties expected from such a silicate.

2) The thermal stability of the Ta and TaN electrode on the lanthanum-silicate MOS devices was examined. As a result, TaN was identified as the more thermally stable

metal electrode, resulting in enhanced device properties. The diffusion barrier properties in relation to oxygen through Ta-based metal electrodes were identified.

3) A tungsten capping layer is observed to be a source of high oxygen content that can cause a reduction in the enhancement observed by using a high-κ dielectric. By optimizing the growth of tungsten, the oxygen content can be decreased substantially.

4) Atomic diffusion of lanthanum, from the lanthanum silicate, into the silicon substrate is not observed by back-side secondary ion mass spectroscopy. It is reported that the lanthanum incorporation into an amorphous silicate is most likely responsible for this observation.

5) The use of a lanthanide (La, Dy, Ho and Yb) oxide capping layer on HfSiO(N)/SiO_2/Si, results in effective work function values ideal for the nMOSFET devices. MOSFET devices with such an MOS structure (La), fabricated in collaboration with SEMATECH, results in excellent device data.

6) The effective work function of lanthanum silicate devices (without the HfSiO(N) interlayer) is shown to be tailored by the extent of silicate formation during the silicate reaction anneal. The extent of silicate formation can be enhanced and lessened by incorporation of additional oxygen and nitrogen into the silica interfacial layer, respectively.

2. LITERATURE REVIEW

2.1 MOSFET Device

The most important device in integrated circuit technology is the field effect transistor (FET). First proposed in the 1930's by Lilienfeld,[1-3] the concept of the FET was implemented by Shockley, Bardeen, and Brattain at Bell Labs in 1947.[4, 5] The impetus of their work was to find a replacement for the frequency mixer element in microwave radar receivers. Current technology at the time was tube-based, and was slow. Working with a solid-state device based on a germanium semiconductor crystal, a triode device was developed. The naming of the new device as voted on by a select committee at Bell Labs. Among the choices was 'iotatron' and 'transistor'.[6] The term 'iotatron' is originated from the ninth letter of the Greek alphabet and was to symbolizing the device's size minimization compared to a vacuum tube. The term 'transistor' is based on the fact that the solid state device is a current controlled device. Note that the vacuum tube is voltage controlled device, which is defined by 'trans-conductance'. John Pierce, a colleague of Brattain, properly observed that the defining property of the new device was its 'trans-resistance', thereby originating the term 'transistor'. The device design soon led to the bipolar junction transistor developed by Shockley. It was not until the 1960's that the silicon-SiO_2 transistor design was introduced by Kahng and Attala,[7,8] now coined the metal-oxide-semiconductor FET (MOSFET).

2.1.1 Functionality

In its essence, a transistor is a four-terminal device that allows for control of electron flow between two electrodes, regulated by a gate electrode (the semiconductor body also acts as a terminal).[9] **Figure 2.1** shows the four-terminal device, with the terminals as the source, drain, gate, and body. The body consists of a semiconductor material (such as silicon) that must be modified to allow for increased electrical current conduction. At room temperature, lattice vibrations result in a small quantity of electrons with enough thermal energy to transfer from the valance band to the conduction band. The concentration of these free

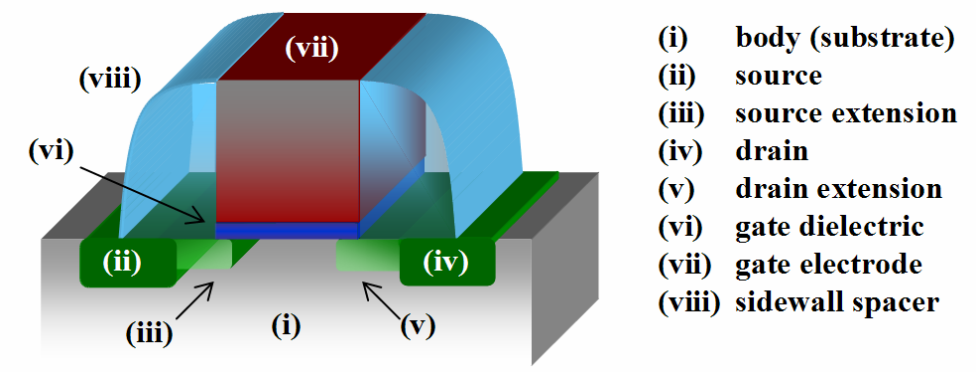


Figure 2.1: *Standard design of a four-terminal metal-oxide-semiconductor field effect transistor. Adapted from Tsividis.*[9]

electrons is the intrinsic carrier concentration of the semiconductor (~10^{10}/cm^3 for a crystal lattice of 5x10^{22} atoms/cm^3). For every electron that separates from an atom, a vacancy (or hole) is left behind into which an electron from another atom can be captured. A hole can be considered as the positive charge equivalent to a negatively charge electron. In the presence of an external field, free electrons have a coordinated motion that yields a current flow. Intrinsically, the number of electrons and holes are equivalent. The number of holes or electrons can be increased significantly by adding impurity atoms to the silicon lattice from Group IIIB or Group VB elements. For example, Group VB impurity atoms donate one additional valance electron beyond that required for perfect bonding to the silicon lattice. The extra electron is easily freed from the impurity atom at a low thermal energy, leaving a behind a fixed positive charge. In this situation, the free electrons and the fixed holes are referred to as the majority and minority carriers, respectively. By adding a required impurity concentration (typically >10^{16}/cm^3) a donor level is created in the silicon band gap, and the silicon is denoted as n-type. A parallel comparison can be made with Group IIIB impurity atoms to silicon that yield an acceptor level, in which the silicon is denoted as p-type. The principle of doping the semiconductor is very important for allowing high current levels to be achieved in the MOSFET device.

In the MOSFET device, the source and drain electrodes are doped opposite of the semiconductor impurity type. Therefore, when the drain is biased with a voltage, V_D,

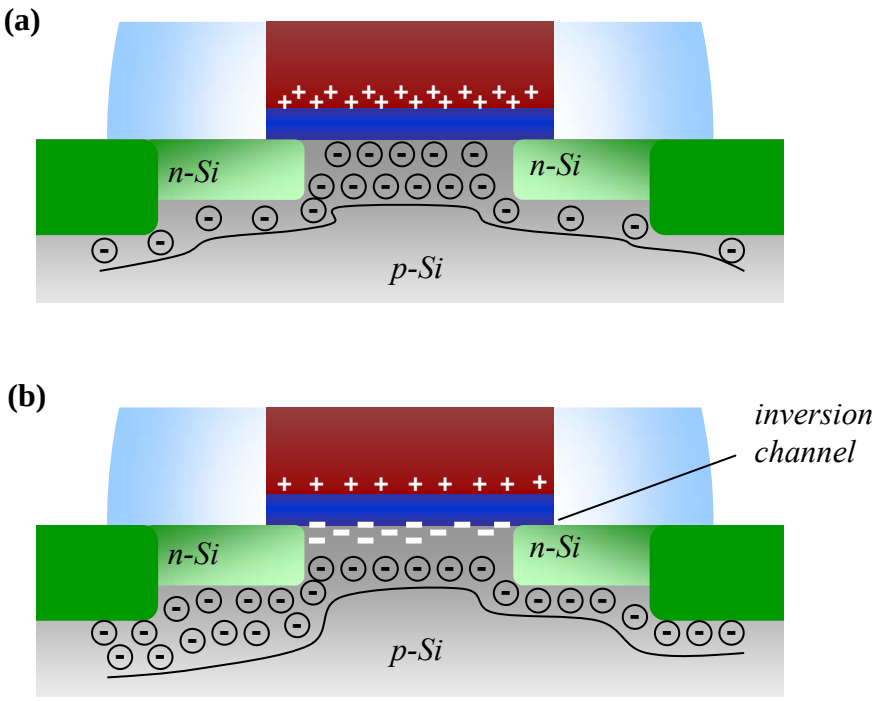


Figure 2.2: *Metal-oxide-semiconductor field effect transistor with a p-type Si substrate in (a) depletion and (b) inversion state. Adapted from Tsividis.*[9]

(referenced to the source) current does not flow in the spacing between the source and the drain. With a sufficiently large negative bias applied to the gate, V_G, holes are attracted to the semiconductor-oxide interface. This situation is aptly named the accumulation state of the MOSFET. As the voltage is increased, V_G begins to repel holes away from the dielectric/semiconductor interface, leaving a depleted region as shown in **Fig. 2.2 (a)**. Note in the figure that a circled charge represents a fixed carrier in the silicon lattice due to the impurity dopant. With a sufficiently large positive biased V_G, free electrons are attracted to the dielectric/semiconductor surface. This is the MOSFET state called inversion, as shown as **Fig. 2.2 (b)**, and is the main operative state of the MOSFET device. When the MOSFET is in inversion, a channel between the source and drain is available for current flow through the drain, I_D, with an applied V_D. The minority carrier that is the channel defines the nomenclature of the device as a nMOS for this example, or pMOS in the case of a positive charged channel.

The characteristic trend of I_D as a function of V_D for an increasing V_G is shown in **Fig. 2.3 (a)** for a pMOS device. As V_G increases (negatively) a larger drain current is realized. Measured at constant drain voltage, a characteristic trend of logarithmic of I_D as a function V_G is obtained, as shown in **Fig. 2.3 (b)**. The ON-state and OFF-state current of the MOSFET device in terms of the drain current are labeled in **Fig. 2.3 (b)** as I_{ON} and I_{OFF}, respectively. Using the gradual channel approximation,[9] the drain current can be approximated,

$$I_D = \frac{W}{L}\mu_{eff}C_{inv}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \qquad \text{Equation (2.1)}$$

The transient current and the saturation current, $I_{D,sat}$, of the characteristic trend in **Fig. 2.3 (b)** can be modeled by **Eqns. (2.2)** and **(2.3)**, respectfully:

$$\left.\frac{\partial I_D}{\partial V_G}\right|_{V_D \to 0} = \frac{W}{L}C_{inv}\mu_{eff}V_D \qquad \text{Equation (2.2)}$$

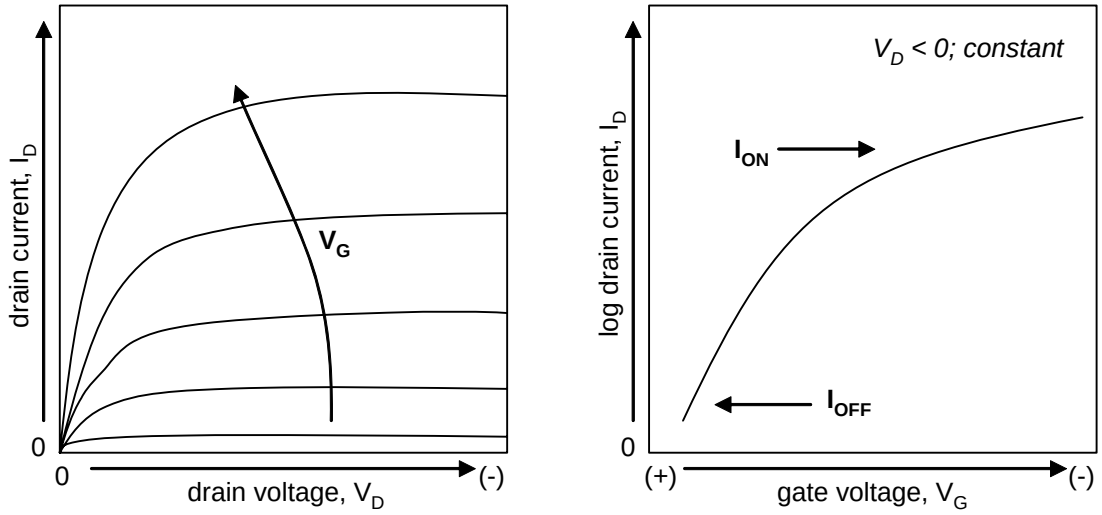


Figure 2.3: *(a) Characteristic drain current (I_D) as a function of drain voltage (V_D, supply voltage) for increasing gate voltage, V_G, biasing and (b) characteristic log I_D vs. V_G for at a constant (-) V_D.*

$$I_{D,sat} = \frac{W}{L}\mu_{eff}C_{inv}\frac{(V_G - V_T)^2}{2}$$ Equation (2.3)

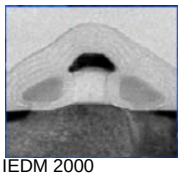
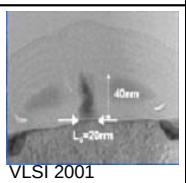
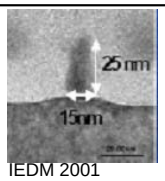
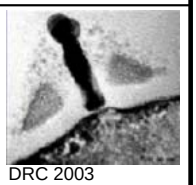
with W being the channel width, L being the channel length, μ_{eff} being the effective mobility, C_{inv} being the capacitance density with the channel in inversion, and V_T being the threshold voltage. Note that the threshold voltage of the device, which can be determined by an extrapolation to the y-intercept in a plot of I_D vs. V_G, defines the point at which inversion begins.

It is important to understand what the mobility term appearing in **Eqns. (2.2)** and **(2.3)** refers to with respect to the substrate and the device.[10] Mobility defines the average velocity of carriers to be transported in a semiconductor material either by hole or electron movement within their respective bands. There exists both a fundamental mobility that is calculated from basic principles and a measured mobility that takes in account the effect of the measurement field (i.e. conductivity, Hall, or drift mobility). In a MOSFET, the mobility is dictated by contact resistances and defects related to the structure and materials of the device. Therefore, the mobility described in this context is an *effective mobility,* μ_{eff}, of the device. Note that there also exists a field effect mobility that takes into account the μ_{eff} dependence on the gate voltage. For simplicity, μ_{eff} will be used to better understand the motivation of device scaling.

2.1.2 Standard Processing

Processing can be divided into two categories, front end of line (FEOL) and back end of line (BEOL). FEOL processes involve those up to first metal layer and offset spacers, observed by cross-sectional transmission electron microscopy in **Table 2.1**. The end product of the FEOL processes is a stand-alone operative MOSFET. For comparison, **Fig. 2.4** shows the SEM cross section of the BEOL that involves the metal interconnects that can have more than seven metal layers. The standard FEOL processing sequence is summarized in **Fig. 2.5**. Based on this standard sequence, FEOL processing for MOSFET devices consists of > 50 processing steps, depending on the modifications. The lithography processes, which are not

Table 2.1: *Cross-sectional transmission electron microscopy of present and future transistor technology nodes.*

Technology Node	90 nm	65 nm	45 nm	32 nm	22 nm
x-TEM	 IEDM 2002	 IEDM 2000	 VLSI 2001	 IEDM 2001	 DRC 2003

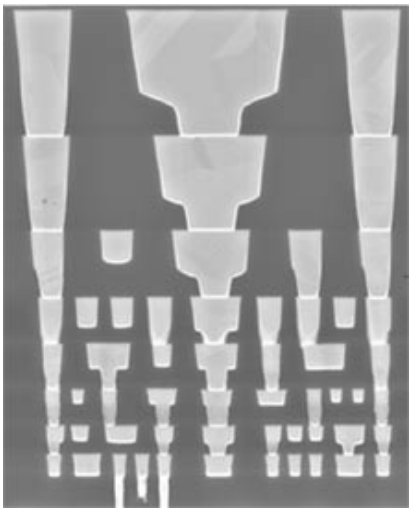


Figure 2.4: *Transistor device after BEOL interconnect processing to Metal 8 for a CMOS device.*

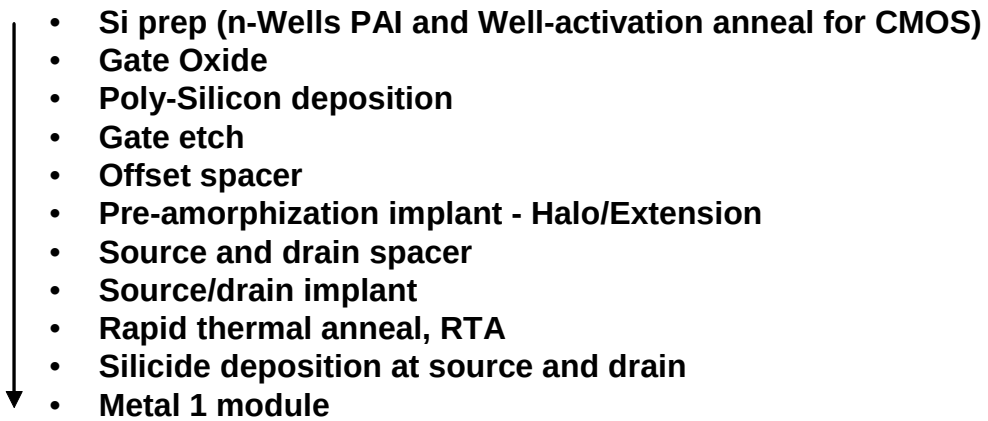


Figure 2.5: *FEOL processing flow summary for CMOS device processing from substrate preparation to Metal 1.*

shown, account for many of the process steps. It is noted that the current gate electrode used is a poly-silicon layer that is doped to provide an appropriate metal work function. From a materials perspective, one of the most stringent processing steps is a high-temperature, short time anneal that occurs after the dopant implant to activate the impurities in the source, drain, and poly-silicon gate regions of the transistor device. This annealing must provide a suitable energy to diffuse the dopant into the silicon to the required junction depth and incorporate the dopant in the silicon lattice (activation). The current industrial practice is a 5-10 second activation anneal ranging between 995 and 1050 °C. The diffusion of atoms between heterojunctions often occurs with such a thermal budget (time-temperature). Consequently, a reduction of the rapid thermal anneal (RTA) temperature could have a favorable influence on the gate stack. An alternative to subjecting the gate stack to a high-temperature anneal would be to rearrange the process flow to activate the source and drain dopants prior to the deposition and patterning of the gate dielectric and gate electrode. This gate-last, or reverse-gate, processing route would allow the gate stack to be subjected to a decreased thermal exposure (~500-600 °C). However the gate involves more photolithography processing steps, preventing its implementation into mainstream devices processing.

2.1.3 Device Scaling Theory

Recall that the momentum for transistor technology was to enhance the speed of device operation. The complimentary metal-oxide-semiconductor (CMOS) device, which utilizes both a pMOS and nMOS side-by-side, is the standard logic device. A CMOS inverter is shown in schematic form in **Fig. 2.6**. The switching speed, τ, of such an inverter is the discharge time for the capacitance load of the nMOS and the time required to charge the pMOS to its load capacitance and follows,

$$\tau = C_{total} V_D \left(\frac{1}{I_D^n + I_D^p} \right) \qquad \text{Equation (2.4)}$$

with C_{total} being the total gate capacitance (including junction and interconnect capacitances). An increase in drain current for the both the pMOS and nMOS allows for a faster MOSFET device.[11] This relates to **Eqn. (2.3)**, as a need for a larger $I_{D,sat}$. An increase in $I_{D,sat}$ may be achieved by increasing the effective mobility, decreasing the channel length, or increasing the capacitance. Note that V_T is limited by the thermal operation of the device (kT = 25 mV; operating temperature of MOSFET $\approx$ 100 °C) and increasing V_G causes an increased field across the oxide that promotes unwanted leakage from the gate to the channel (substrate). Mobility, as previously implied, can be increased by eliminating the resistances and defects associated with the physical MOSFET device structure. Reducing the channel length decreases the physical travel distance of the electron exchange between the source and drain. Also, a reduction in oxide thickness increases the capacitance, which means higher carrier concentration and improved inversion for a similar applied voltage. The ideal case for scaling suggests that if all dimensions of the transistor are scaled and dopant densities are increase by a factor α, then the scaled MOSFET device will have the same electric field configuration.[12] This principle, known as constant field scaling, results in an increase in switching speed and a decrease in dimensionality by a factor α and α^2, respectively. **Table 2.2** shows the constant field scaling factors for a number of the MOSFET physical parameters. These factors have provided the means for scaling of the MOSFET device, a progression historically described by Moore's Law.

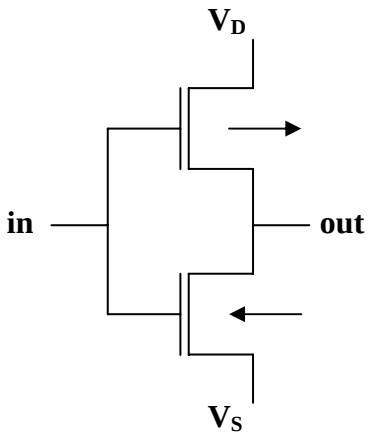


Figure 2.6: *The electronic diagram of a CMOS inverter.*

Moore's Law was a concept proposed by Gordon Moore in 1965 and states that devices are scaled 50% every two to three years. Initially set out as a simple observation, the goal of the high-end MOSFET industry is now to keep up with the principle described by Moore's Law. As a guideline for the industry, the International Technology Roadmap for Semiconductors (ITRS) provides industry and academia with a proposed scenario involving all device related properties and materials for the scaling of the MOSFET device to the 22 nm transistor node (minimum half-pitch of the first metal interconnect) expected to be introduced by the year 2016.[13] Currently the high-end MOSFET industry, supplying integrated circuits to the server and CPU markets, is based on a 65 nm node. It is the goal for some industrial companies to reach 45 nm MOSFET devices by early 2008, a metric that was originally established by the ITRS. For a better perspective of scaling according to the ITRS roadmap, **Table 2.3** shows channel length (or gate length), supply voltage, equivalent physical oxide thickness, and gate leakage required of transistor nodes between 65 and 22 nm. Parametrics are shown for both the high-performance and low-standby power devices to better understand the strict

Table 2.2: *The constant-electric field scaling factor for different physical parameters of the MOSFET device.*

Physical Parameter	Constant-electric field scaling factor
Channel length	$1/\alpha$
Insulator thickness	$1/\alpha$
Electric field in device	1
Voltage	$1/\alpha$
On-current per device	$1/\alpha$
Doping	α
Area	$1/\alpha^2$
Capacitance	$1/\alpha$
Gate delay	$1/\alpha$
Power dissipation	$1/\alpha^2$
Power density	1

Table 2.3: *Performance and materials metrics for high performance and low standby power devices as defined by the International Technology Roadmap for Semiconductors.*

high performance	*units*	2007 65 nm	2010 45 nm	2013 32 nm	2016 22 nm
Physical gate length	*nm*	25	18	13	9
Power supply	*V*	0.8	0.6	0.5	0.4
Equivalent physcial oxide thickness	*nm*	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Gate leakage @ 100 °C	$\mu A/\mu m$	$4x10^3$	$1.7x10^4$	$5.4x10^4$	$1.1x10^5$

low standby power		2007 65 nm	2010 45 nm	2013 32 nm	2016 22 nm
Physical gate length	*nm*	32	22	16	11
Power supply	*V*	1.1	1.0	0.9	0.9
Equivalent physcial oxide thickness	*A*	1.2-1.6	0.9-1.3	0.8-1.2	0.7-1.1
Gate leakage @ 100 °C	$\mu A/\mu m$	0.0031	0.014	0.044	0.091

strict requirements associated with the low-standby power CMOS devices for server and CPU chips. Trends include a decrease in channel length and physical oxide thickness, a decrease in the power supply voltage, and a gradual increase in the allowable leakage current density. The transition to smaller nodes exposes problems within the MOSFET device structure that must be resolved either through processing modification or material alteration. Issues that are of great importance for sub-65 nm nodes include interconnect engineering in BEOL processing and lithography, junction engineering, channel engineering, gate dielectric and metal gate electrode FEOL processing. These issues are to be addressed separately with respect to the MOSFET device design and its processing challenges. Specific emphasis will be placed on the those issues related to the metal-oxide semiconductor 'gate stack' that is

formed in the framework of the MOSFET device. Within the context of the gate stack, gate dielectric will be discussed in detail.

2.1.4 Device Scaling Difficulties

The difficulties that arise in meeting the metrics outlined by the ITRS roadmap for low-standby power CMOS devices has been the driving focus of semiconductor research in both academia and industry. Issues that are of great importance for sub-65 nm nodes include interconnect engineering in BEOL processing and lithography, junction engineering, channel engineering, gate dielectric and metal gate electrode in FEOL processing.

As the name suggests, interconnects that are formed during BEOL processing link the individual MOSFET devices, as shown previously in **Fig. 2.4**. The time delay of an integrated circuit is dependent on the line resistance and line capacitance. The value of the time delay is also known as the RC constant. The RC constant can be lowered by a decrease in metal resistivity or a minimization of the dielectric constant of the interconnect materials.[14] The metal resistivity is decreased by introducing a different metal (i.e. AlCu to Cu). Low-κ materials are realized by introducing fluorine, carbon or hydrogen into SiO_2.

Lithography is the foundation of layer by layer device processing which enables the reproduction of fine features and patterns in polymeric layers for the purpose of transferring those patterns through etching and lift-off. A main obstacle for scaling is the minimum line width achieved through lithography.[12,14] To overcome this obstacle, a common practice has been to reduce the optical wavelength of the exposure lamp. The wavelength of light has been reduced from using a 248 nm exposure wavelength (supplied by a KrF laser) down to < 190 nm wavelengths (supplied by a ArF laser). The most likely choice for next generation lithography is an EUV lithography technique that uses energetic photons with a wavelength of ~11-13 nm and has high wafer throughput compared to alternative options.

The origin of junction (source and drain contacts) engineering was the recognition of an ability to reduce the short channel effects that are observed with scaling. As the channel length is scaled, the electric field produced by the drain can extend through the channel and

affect the channel potential near the source. To reduce this affect, the junction depth of the source and drain needs to be minimized. Recent practice has also required a reduction in the junction thickness to less than 22 nm.[13] An extension to these contacts allows an even shallower pathway that links the source/drain contacts to the channel. However, parasitic resistance related to the junction hinders current flow from the channel to the contact.[15,16,17] **Figure 2.7** shows the parasitic resistances that are due to the junction, extension, and channel. The current through the channel is always going to be affected by the channel resistance, R_{chan}. As current enters the extension and contact it can be substantially limited by the other parasitic resistances. As the current leaves the channel, it flows through an accumulation region, the spreading of the extension, and the contact. Typically, it is required that these additional resistances total < 10% of R_{chan}. The accumulation, R_{acc}, and spreading, R_{sprd}, resistances are a result of diffusion of the dopants during the rapid thermal anneal (RTA, 1000 °C, 5 seconds) required for dopant activation into the silicon lattice. The need for an abrupt profile is being realized by changing the activation anneal to a short-time high-temperature anneal using flash lamp anneal (FLA), spike annealing, or laser spike annealing (LSA).[17] LSA permits substrate heating to a temperature > 1300 °C for a μs-ms time frame. This process not only reduces the extent of dopant diffusion, but allows for an increased activation of dopants needed to reduce contact resistance. It is arguable that the contact

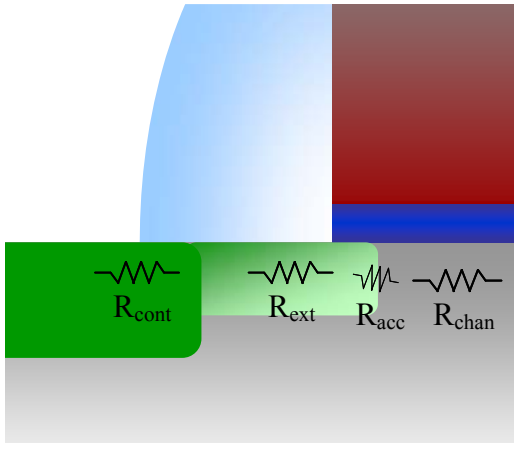


Figure 2.7: *Parasitic resistance at source (or drain) junction with the channel is shown as a summation of the contact, extension, accumulation resistances.*

resistance will ultimately limit scaling. According to the ITRS roadmap, future technology nodes require a contact resistance $<10^{-8}$ Ω cm in order to remain on par with the channel resistance. In order to achieve such values, the silicon must be doped to $> 2 \times 10^{20}$ cm^{-3}, a level beyond the solubility of most dopants at a temperature 1000 °C, but may be reached with introduction of technologies such as LSA.

Channel engineering has led to effective mobility enhancement by introducing stress to the channel.[17,18] This has been done by using epitaxial $Si_{1-x}Ge_x$ in the source and drains and the addition of a stress liner on the gate electrode. With a $Si_{1-x}Ge_x$ source and drain, the silicon in the channel is compressed and yields up to a four-fold increase in the hole mobility. The use of stress liner (such as silicon nitride), induces a tensile stress on the channel, the result being a higher electron mobility. Alternatively, the mobility has been shown to be increased by changing the channel surface crystal orientation to optimize current flow.

2.2 Gate Stack Scaling

To introduce gate stack scaling, it is useful to first review the principles of the gate stack as a separate entity outside of the MOSFET. This metal-oxide semiconductor structure can also be described as a capacitor.

2.2.1 MOS Capacitor

For the most part, the MOS capacitor has already been introduced in the discussion of the four-terminal MOSFET. A MOS capacitor is a two-terminal device that consists of a gate electrode and substrate separated by a gate dielectric, shown in **Fig. 2.8**, a structure that is typically referred to as the gate stack.[9,19] In essence, it is the operational heart of the MOSFET. Just as in the case with the MOSFET, sweeping the gate voltage can induce majority and minority carrier response in the substrate underneath the dielectric. **Figures 2.9 (a)-(e)** show the capacitor (with a p-type semiconductor) in standby, accumulation, flat-band, depletion, and inversion. With a sufficiently positive and negative voltage, an accumulation and inversion layer is obtained in the channel. Since opposite facing electrodes are not present (i.e. source and drain of the MOSFET), the observation of the accumulation,

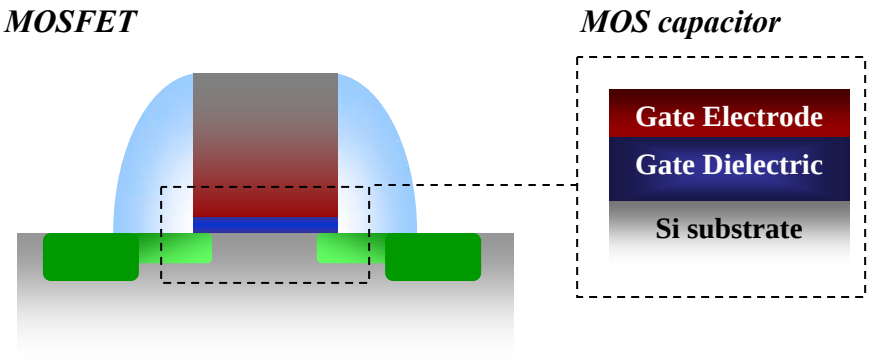


Figure 2.8: *The metal-oxide-semiconductor (MOS) capacitor is displayed as the 'gate stack' of the MOSFET device.*

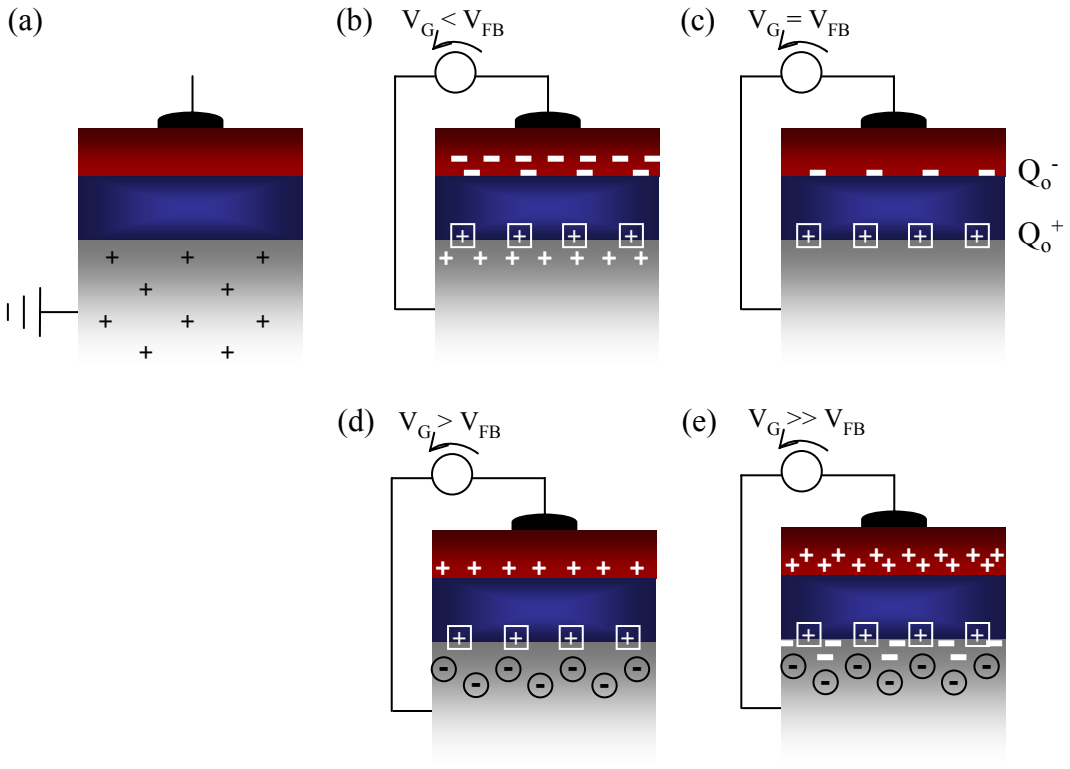


Figure 2.9 (a)-(e): *The metal-oxide semiconductor capacitor in (a) standby [no bias], (b) accumulation [$V_g < V_{FB}$], (c) flat-band [$V_g = V_{FB}$], (d) depletion [$V_g > V_{FB}$], and (e) inversion [$V_g >> V_{FB}$].*

depletion and inversion states of the channel can be observed by measuring the device capacitance. **Figure 2.10** shows the characteristic low-frequency and high-frequency trends of the capacitance as a function of applied gate voltage. It is first observed that the oxide capacitance follows,

$$C_{ox} = \frac{\kappa \varepsilon_O A}{t_{ox}} \qquad \text{Equation (2.5)}$$

with κ being the dielectric constant (also referred to as permittivity) of the oxide, ε_O being the permittivity of free space (8.85×10^{-3} fF/μm), A being the gate electrode area, and t_{ox} being the thickness of the oxide. The variation of the capacitance arises from the fact that the apparent thickness of the capacitor increases with an increase of the depletion region. In accumulation and inversion, the capacitance is only a measure of the physical thickness of the oxide. It is also observed from **Fig. 2.10**, that the capacitance trend is a function of the measurement thickness. At high frequencies, the minority carrier is unable to respond and the majority

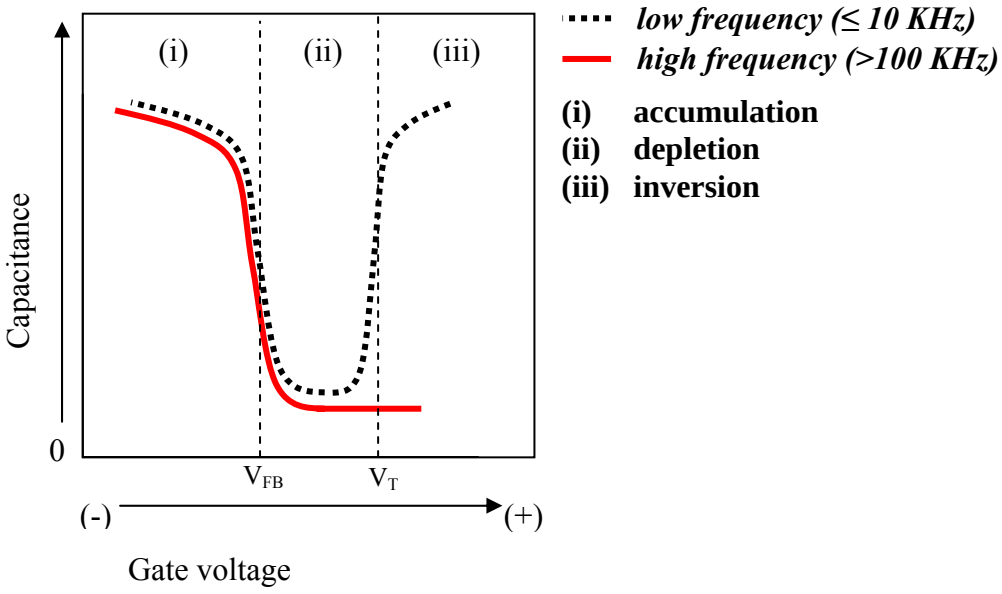


Figure 2.10: *The three operating regions of the device shown for a capacitance-voltage (CV) measurement of an MOS device at a low measurement frequency (<10 kHz, black-dashed line) and a high measurement frequency (> 100 kHz, red line).*

carriers are able to respond in negative gate bias, or accumulation. Given this information, thickness of the oxide can be determined provided that the area of the capacitor and the dielectric constant of the oxide are known. The natural oxide on a silicon substrate is SiO_2 and has been the historical choice for the dielectric, with a dielectric constant of $\kappa_{SiO2} = 3.9$. As a gate electrode, a poly-silicon layer is used. The benefit of using a poly-silicon electrode is that the work function of the electrodecan be tuned with appropriate doping. For a pMOS device (n-Si substrate) the appropriate metal work function is ~5.0 eV. For an nMOS device (p-Si substrate) the appropriate metal work function is ~4.0 eV. As will be discussed in **§2.2.2**, the use of a poly-silicon electrode prevents suitable scaling of the MOSFET device.

To understand the electronic implications of using alternate materials, it is useful to observe the band diagram of such a device.[20] The band diagram of p-type and n-type silicon MOS capacitors are shown in **Figs. 2.11 (a)** and **(b)**, respectively. In the figures, there is assumed no applied charge and the work function of the metal allows for alignment between the metal and semiconductor. Therefore in this situation, the work function of the electrode, $q\phi_M$, is aligned with the Fermi energy level of the semiconductor, E_F, and the flat-band voltage is equal to zero. The electron affinity, $q\chi$, defines the offset of the semiconductor conduction band (4.05 eV for Si), and the band gap of the semiconductor (1.1 eV) defines the subsequent offset to the valance band. The doping concentration in the semiconductor defines the E_F. Note that the position of the E_F is closer to the valance band for the p-type semiconductor shown in **Fig. 2.11 (a)** and closer to the conduction band for the n-type semiconductor shown in **Fig. 2.11 (b)**.

The presence of charge at the oxide/semiconductor interface (interface traps), distributed charges in the oxide (fixed charge), or misalignment between the semiconductor Fermi energy level and the metal work function results in a field across the oxide and band bending. The gate voltage needed to resume a 'flat' profile across the entirety of the band diagram is referred to as the flat-band voltage. Additional voltage (negative for p-type, positive for n-type) is required to reach accumulation. This applied voltage is observed as further band bending in the semiconductor and an additional field across the oxide. The final remark

concerning the band diagram is band gap energy, E_G, of the dielectric. It is noted that band alignment between the semiconductor and oxide is a property of the bulk materials and their interface. The origins of band alignment are not fundamentally understood. Typically this alignment is not symmetric with respect to the silicon, resulting in a value of the conduction band offset, $q\Phi_B$, being of lower magnitude than the valance band offset (not shown in **Fig. 2.11 (a)** and **(b)**). For example, SiO_2 in contact with silicon has a band gap of 9.0 eV, a conduction band offset of 3.2 eV and a valance band offset of 4.7 eV.[21] The height of the conduction band offset essentially defines the insulating quality of the dielectric in that it

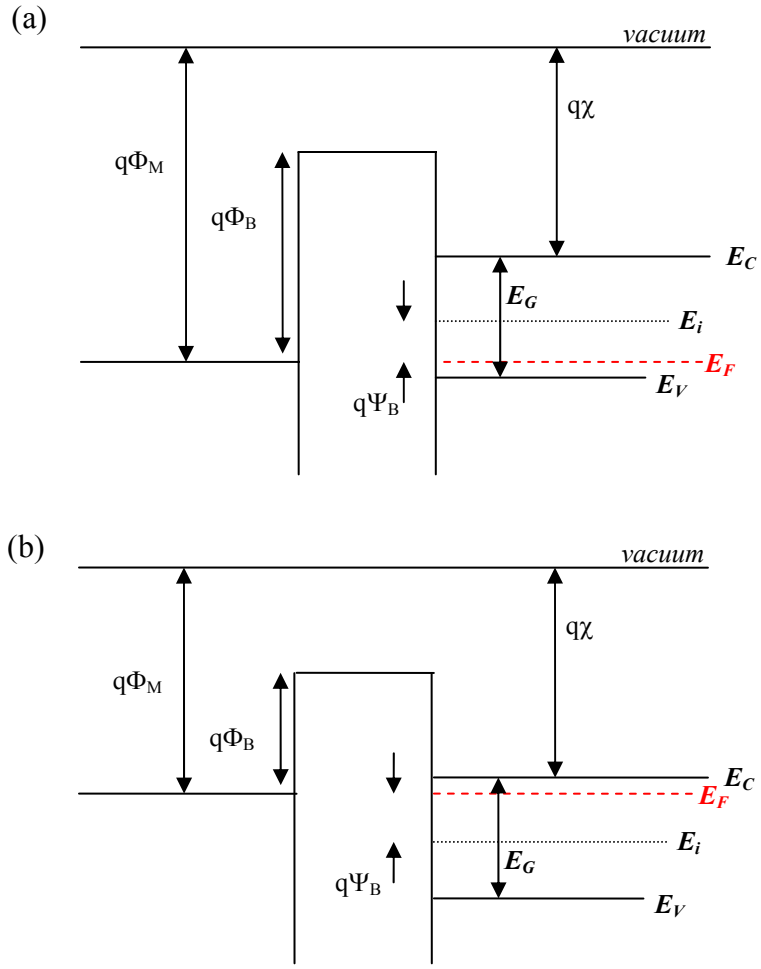


Figure 2.11: *The energy band diagrams of the MOS device with a (a) p-type semiconductor and (b) n-type semiconductor.*

separates electron movement from the electrode to the semiconductor. Note the interrelated importance of the magnitude of the conduction band offset, flat-band voltage, and voltage required to reach accumulation. For insulating properties to be retained, the voltage required to obtain flat-band and accumulation must be lower than the conduction band offset. In this way, the electrode work function is very important in defining the allowable operating voltage of the capacitor.

2.2.2 Gate Electrode

A main problem with the poly-silicon gate electrode is the formation of a poly-depletion layer that extends the electrical thickness of the dielectric beyond its physical thickness.[16,22] The electrical thickness is defined as the distance between the charge centers in the gate electrode and the substrate. When the electrode is biased to bring the channel to inversion, the mobile carriers of the poly-silicon closest to the dielectric are pushed away from the interface. This yields a depletion layer that is ~3-4 Å in thickness and is electrically indistinguishable from the dielectric, a region that is referred to as poly-depletion. The inversion layer in the channel also acts in a similar manner and adds an additional 3-6 Å to the electrical thickness of the device. Whereas the substrate inversion layer is necessary for operation of the device, the poly-depletion can be lowered by the introduction of a metal gate electrode. With a metal there exists an infinite supply of electrons for conduction and the affect of the poly-depletion is decreased below 1-2 Å.

2.2.3 Gate Dielectric

As noted earlier, the native oxide on silicon is SiO_2 and has been used since nearly the onset of MOSFETs. In **Table 2.1**, it is noticed that for the 45 nm node, a dielectric thickness < 12 Å is necessary. A SiO_2 thickness reduction to this level leads to current leakage from the gate electrode to the substrate; a process of direct tunneling as the electrons are transmitted through the length of the dielectric. There are multiple mechanisms for this to occur. Foremost, a single monolayer of SiO_2 has a thickness of 7-8 Å. It has been shown that a SiO_2 thickness < 2 monolayers leads to lowering in the conduction band, which serves as the

potential barrier holding electrons in the gate electrode and resists electron flow to the substrate.[23] In addition, without the appropriate scaling of the MOSFET operating voltage, a high field across the oxide is present, leading to increased leakage. In fact, an MOS device with a 15 Å SiO_2 thickness has been reported to have a leakage current density > 100 A/cm^2. This leakage is a combination of direct tunneling and Fowler-Nordheim tunneling that can occur with the appropriate band bending.[10] Note the Fowler-Nordheim tunneling can also occur with thicker SiO_2 if a sufficiently high voltage is applied across the oxide. The ITRS roadmap requires leakage current density < 10 A/cm^2 for future MOSFET nodes. There are few options for decreasing this leakage. The most promising option for leakage reduction is the introduction of an oxide with a dielectric constant greater than that of SiO_2. An increase in the dielectric constant allows for an equivalent SiO_2 thickness that is smaller than the actual thickness of the dielectric. The equivalent oxide thickness, or EOT, is determined by,

$$EOT = t_{high-\kappa} \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} \qquad \text{Equation (2.6)}$$

with $t_{high\text{-}k}$ and $\kappa_{high\text{-}k}$ defined as the physical thickness and dielectric constant of the dielectric, respectively. **Figure 2.12 (a)** shows the physical thickness of dielectric as a function of dielectric constant required to obtain a specific EOT, as defined by **Eqn. (2.6)**. It is observe that to achieve an EOT of 10 Å, a dielectric of physical thickness of 20 Å and a dielectric constant of 7.5 is required. The benefit of introducing this new dielectric material is obvious. Considering the shortfalls of SiO_2 with a reduction in thickness, it is useful to define a thickness boundary of the newly proposed dielectric layer. **Figure 2.12 (b)** shows the dielectric constant as a function of EOT for an increasing physical dielectric thickness.

Noting that the dielectric must be at least ~20 Å in thickness, the overall dielectric constant for the oxide must be > 7.5 to achieve and EOT of 10 Å and > 15 to achieve an EOT of 5 Å. It is noted that this simplified calculation does not consider the complexities of introducing the new dielectric into the 'gate stack' or the observation of poly-depletion that occurs within the gate, which makes the required dielectric constant much higher.

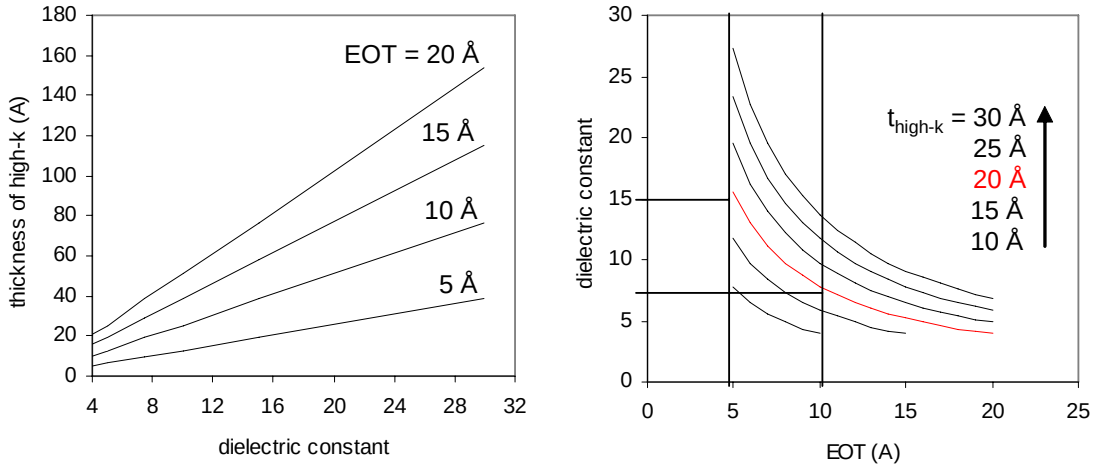


Figure 2.12: *The physical thickness of high-κ dielectric as a function of dielectric constant required to obtain a specific EOT.*

As the dielectric is scaled below 4.0 nm, a benefit of introducing nitrogen into SiO_2 was observed.[24] It is shown that nitrogen incorporation increased the dielectric constant ($\kappa = 7$ for Si_3N_4) and decreased boron penetration from the poly-silicon gate electrode to the channel. It was shown that the boron penetration acted to displace the prescribed minority/majority carrier concentrations, resulting in a decrease in device effective mobility. A nitrogen concentration less then 10% is necessary to prevent this diffusion and can be incorporated into SiO_2 by annealing in a N_2O, NH_3 or NO ambient. As the dielectric is scaled to 2.0 nm, a higher nitrogen concentration (15-20%) is necessary and must be incorporated using a plasma nitridation. However, a high nitrogen concentration is shown to introduce scattering defects that results in a decrease in the effective mobility. Therefore, the solution of nitrogen incorporation is limited and can only be used to obtain EOT values as low as 1.3 nm.[22] The leakage limitation of a gate dielectric based merely on SiO_2 (with or without nitrogen addition) has created the need for a replacement material that has superior dielectric properties than what is currently available. These materials are commonly referred to as high-κ dielectrics, even though their permittivity values range between $8 \rightarrow 35$, a range orders of magnitude lower than that achievable in complex ferroelectric and dielectric crystals.

2.3 High-κ Dielectrics

2.3.1 Introduction

A dielectric material is that which becomes polarized when subjected to an electric field. The dielectric constant, or permittivity, of a material is a relative measure of electronic polarizability. In microelectronics, dielectrics are found in parallel-plate capacitor structures such as a metal-insulator-metal (MIM) or a metal-oxide-semiconductor (MOS). The MIM device configuration is typically used to store charge for use in random-access-memory (RAM).[25] The MOS device is integral to a MOSFET device, in which the oxide is used to gate the flow of current in an adjacent semiconductor that connects two electrodes (source and drain). As MOSFET devices are scaled, a high-κ gate dielectric is needed to replace SiO_2 or SiO(N) films due to their high leakage currents when the thickness is decreased below 1.5 nm.[22,25] Existing problems with implementing a high-κ dielectric into industrial transistor processing routes has prevented an easy integration of the new dielectric into the gate stack. MOSFET processing (FEOL) induces a number of problems with respect to the gate stack that must be overcome through a change in processing conditions or materials properties. These issues include:

- Phase transformation and/or decomposition of the gate dielectric at high temperatures.
- Formation of a defective interface with the silicon substrate.
- Formation of a SiO_2-rich interfacial region that prevents the scaling of the equivalent oxide thickness, EOT.
- Replacement of the poly-silicon gate electrode with a metal gate that is suitable for CMOS functionality.

For a high-κ dielectric to replace SiO_2 in the MOSFET gate stack, it would be ideal for the material properties to be similar to that of the SiO_2. This objective is not entirely possible.

Materials conditions required for implementing a high-κ material into the gate stack include: [21,22,26,27]

- A dielectric constant high enough to see benefit for replacement.
- A band offset large enough to prevent unsuitable leakage between the gate and the substrate.
- Thermodynamic stability of the high-κ material in contact with both silicon and the choice of a gate electrode.
- High-temperature stability required in standard MOSFET processing.
- Low defect density in the dielectric and at the dielectric/substrate interface to prevent the decrease of MOSFET electrical properties (i.e. V_T instability and mobility decrease).

All of these issues and requirements are interrelated in one way or another. These issues are raised at this juncture to introduce the difficulty in simply replacing a material in the gate stack. Each will be introduced in this section in the context of the required properties of the dielectric required and the thermodynamic stability of the dielectric with MOSFET processing. First, it is necessary to define the growth processes that are common to high-κ dielectrics. The characteristics of the dielectric that are useful for MOSFET devices and subsequent scaling will be discussed in detail. By introducing the relationship between the dielectric constant and band gap of the dielectric, it will be observed that the range of dielectrics allowable in MOSFET devices will be decreased significantly. The same will be done by understanding the thermodynamics of the high-κ systems, particularly in contact with silicon. The advantage of tailoring the processing to create a metal silicate dielectric will be discussed. Following this discussion, a succinct review of lanthanide oxides and silicates will be provided.

2.3.2 Growth Processes

Deposition of high-κ materials for an MOSFET device is no different than most other thin film processing in that it depends heavily on the delivery of the oxide for growth and on the post-deposition annealing of the film.[28] The focus of this section is the growth process of the high-κ materials.

The deposition of high-κ dielectrics can be segregated into three categories:[29]

- chemical vapor deposition (i.e. metal organic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD)).
- solution deposition (i.e. sol-gel).
- physical vapor deposition (i.e. radio-frequency and magnetron sputtering, ion beam sputtering, pulsed laser ablation, E-beam evaporation, and molecular beam deposition).

Just as in most other devices, for high-κ implementation into standard CMOS processing, it is important that the deposition technique ideally have:

- thickness uniformity (± 2 Å) across the wafer (up to 300 mm) even when processed with an ultra-thin film thickness (< 25 Å).
- oxidation control/supply during growth.
- composition uniformity.
- high wafer throughput.

Metal organic chemical vapor deposition (MOCVD) uses gases or evaporated liquids to deliver metal cations for oxide formation. Each is limited by the availability of the appropriate gas or liquid metal-precursors needed for different high-κ dielectrics. MOCVD typically utilizes metal alkoxides or β-diketonates precursors that must be dissolved in an

inert solvent.[29] To be introduced into the system, the precursor must have satisfactory volatility for vapor phase transport to the substrate. To overcome this problem, a technique of liquid injection MOCVD is used by incorporating the precursor in a high-volatility solvent. It is important for the precursor to be soluble and stable in the solvent over a long period of time. Complications are magnified when more than one precursor is being used for deposition.

Atomic layer deposition (ALD) is similar to MOCVD, in the fact that metal organic precursors are again used as a means of delivery. However, the continuous deposition that described the MOCVD technique is a better described as a successive pulse deposition for ALD. The gaseous precursor is introduced to the substrate surface and then flushed with an inert gas. This procedure takes advantage of a self-limiting layer formation that restricts growth to one or two monolayers. An oxidizing atmosphere is introduced, allowed to react with the deposited material, and subsequently flushed. The process is repeated until the desired thickness is achieved. Precursor definition is much more complex as it needs to have good thermal stability on the heated substrate and it must be tailored for rapid reaction with the absorbed nucleophilic reactants such that the ligands are efficiently removed.[29]

As the name implies, physical vapor deposition, involves a solid source material that is vaporized in order to transport the material to a new platform in vacuum. This process is done by either bombarding the source material with positive ions (r-f and magnetron sputtering), photon (pulsed laser ablation), and electrons (E-beam evaporation) or by heating the source material to the point that it begins to evaporate at low pressure. Note that the solid source can either consist of the material needed for deposition (i.e. oxide) or a pure metal that can react with a gas species in the vacuum.

Both MOCVD and ALD methods have been proven ideal for large substrates, good composition control, and excellent film uniformity. However the precursor chemistry, particularly for more complicated dielectrics, has limited the growth and utilization of the technique. Solution deposition is not ideal for the thin films (< 10 nm) and the same can be said concerning a wide range of the physical deposition techniques. In this work, molecular

beam deposition is primarily used due to ability to have excellent control of the deposition rate, thickness and oxygen delivery during film processing. It is noted that throughput of a molecular beam deposition process is very low compared to other PVD or CVD methods. However, the methodology is very useful in understanding the principle consequence of processing.

To appreciate the importance of oxygen control during film growth, it is important to understand that the growth of high-κ materials is a non-equilibrium process. The oxygen content in the processing is typically high enough to oxidize both the dielectric being grown and the underlying SiO_2. The latter is unwanted in terms of acquiring a dielectric with a high overall dielectric constant. In this way, dielectric film growth is a non-equilibrium process. However, kinetically this can be controlled.[30] For example, consider the rate of incidence, R, of a gaseous species on a flat surface,

$$R = 3.513x10^{22}\frac{P}{\sqrt{MT}} \qquad \text{Equation (2.7)}$$

with P being pressure (Torr), T being the temperature (K), and M being the mass of the incident atom (a.u.). The oxidation rate of the silicon, t_{rxn}, can be calculated as,

$$t_{rxn} = \chi N_{Si} \qquad \text{Equation (2.8)}$$

with χ being the sticking coefficient between an oxygen and silicon atom (assume ~1), and N_{Si} being the surface density of silicon atoms ($6.74x10^{14}/cm^2$). At a pressure of 1 Torr and at room temperature, the silicon surface can be oxidized in less then two microseconds. If the oxygen pressure during deposition were to be decreased to $1x10^{-6}$ Torr, then the oxidizing time would be approximately 2 seconds. It is obvious that a decrease in oxygen pressure during deposition will allow for less oxidation of the silicon. Taking this idea to the extreme, studies have been conducted that deposit thin metal films in a UHV environment to maintain the pristine interface of the silicon, and then perform an oxidizing anneal.[31]

Just as in the case of controlling the oxygen reaction with the SiO_2, a similar reaction process can be considered for pure metal deposition. The reaction to form the oxide is highly dependent on the oxidizing atmosphere in the molecular beam deposition chamber. The excellent ability to control this atmosphere, and subsequent oxygen in the dielectric, is further enhanced by low deposition rates that can be achieved using molecular beam evaporation (as low as 0.025 Å/s).

2.3.3 Dielectric Constant - Band Gap Energy Relationship

As mentioned previously with respect to SiO_2, a decrease in the oxide thickness can result in increased leakage by means of direct Fowler-Nordheim tunneling between the gate electrode and the substrate. With the introduction of the high-κ dielectric, which allows for a thickness increase in the dielectric, a benefit is observed since the leakage current density is exponentially dependent and the capacitance is linearly dependent on thickness. However, the leakage current density is also exponentially dependent on the barrier height between the gate electrode and the conduction band of the dielectric. Therefore a decrease in the band offset below a certain point can negate the improvement made to leakage by increasing the thickness of the high-κ dielectric.[32]

Appearances of other types of the leakage mechanisms are observed with a decrease in band offset, such as Schottky emission and Poole-Frankel emission.[20] The most common types of leakage mechanisms are shown in **Fig. 2.13**. In general, Schottky emission, or thermionic emission, occurs when an electron from the gate (or substrate) has an energy greater than the conduction band offset. Poole-Frankel emission utilizes electron trap defects in the bulk or interface of the dielectric to 'hop' through the dielectric. To serve as a suitable barrier to leakage, the conduction band offset needs to be > 1.1 eV.

The band gap energy, E_G, is the difference between the conduction band minimum and the valance band maximum, with the conduction band offset (Φ_B in **Fig. 2.11**) being the value of importance for preventing leakage current. **Figure 2.14** shows the conduction and valance band offset for a number of appropriate dielectrics. Certain trends can be understood for the

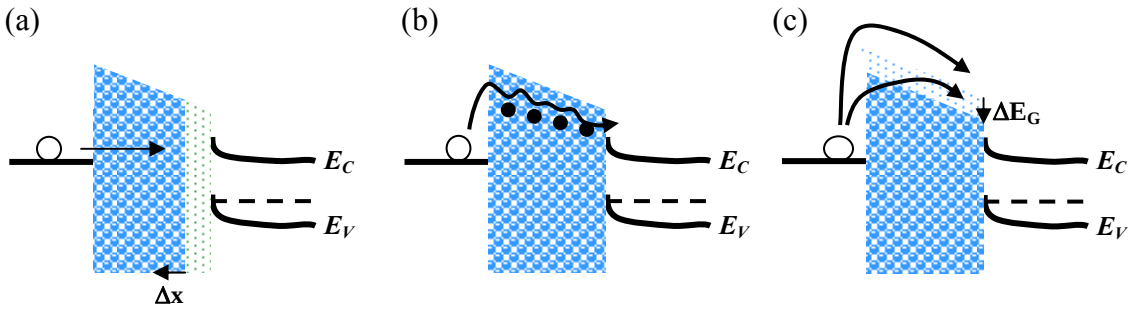


Figure 2.13: *Common leakage mechanisms observed in dielectric materials in clued (a) Fowler-Nordheim tunneling (direct), (b) Frenkel-Poole tunneling (trap-assisted), and (c) Schottky emission (thermionic). In the figure the open circle represents the charged species of the gate electrode.*

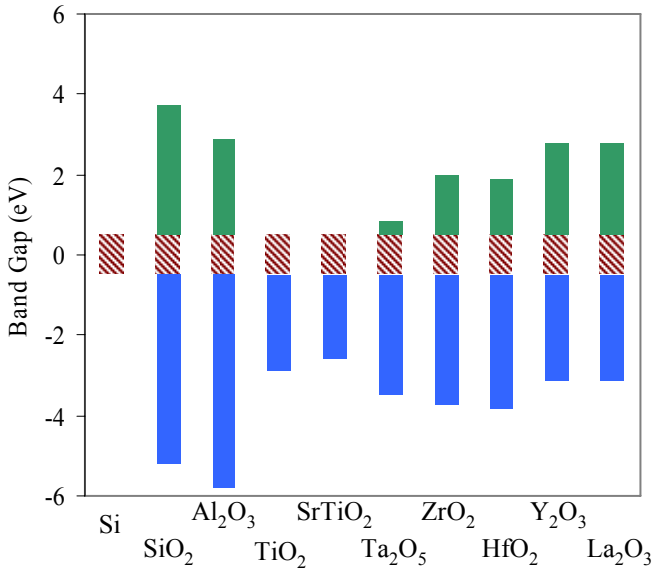


Figure 2.14: *The band gap, including the conduction and valance band offsets, as determined for prospective high-κ dielectrics in contact with silicon (E_G = 1.1 eV). Adapted from Robertson.*[33]

band gap and the conduction band offset. Of the oxides shown, SiO_2 has the highest band gap energy (9 eV). The Si-O bonds are characterized as σ bonds formed from sp hybrid orbitals. The band gap energy is evaluated by the energy difference between bonding and antibonding orbitals. For transition metal oxides (quadra-valant, covalent bonding), the band gap is decreased. In this case E_G is determined by the valance band of the filled oxygen 2p orbitals and the conduction band by the empty transition metal d orbitals. The band gap can be increased by filling the d orbital.[33] In this way, the band gap can be increased for transition metals from 3d to 5d and from Column IV to Column III. In general, it is observed that conduction band offset generally increases with the band gap of the dielectric.

An alternate route for increasing the conduction band offset is to disrupt the balance of the density of states (DOS) within the valance and conduction band.[33] For oxides with ionic bonding, the valance band also considers the oxygen p states (anions) and the conduction band similarly considers the metal d-states (cations). By changing the metal from a quadra-valant to a tri-valant, the valance band DOS increases in relation to the conduction band DOS, increasing the conduction band offset. This relationship is why M_2O_3-oxides have a higher conduction band offset then MO_2-oxides. Ideally, the high-κ replacement would have a higher permittivity and band gap (i.e. of SiO_2). Unfortunately, the band gap of dielectrics is generally shown to decrease with an increase in permittivity. **Figure 2.15** shows the relationship of band gap energy to permittivity for a number of dielectrics.[27,33] This relationship can be derived starting with the fact that the static permittivity of a dielectric, ε, has both an electronic and a lattice contribution,[27,34]

$$\varepsilon = \varepsilon_{electron} + \varepsilon_{lattice} \qquad \text{Equation (2.9)}$$

The electronic contribution, $\varepsilon_{electon}$, is commonly defined as the optical dielectric constant and is typically < 6.0 for high-κ dielectrics useful for high-performance MOSFETs studied in this work. The magnitude of the permittivity is due to the lattice contribution evaluated as,

$$\varepsilon_{lattice} = \frac{Ne^2 Z_T^{*2}}{m\omega_{TO}^{\ 2}} \qquad \text{Equation (2.10)}$$

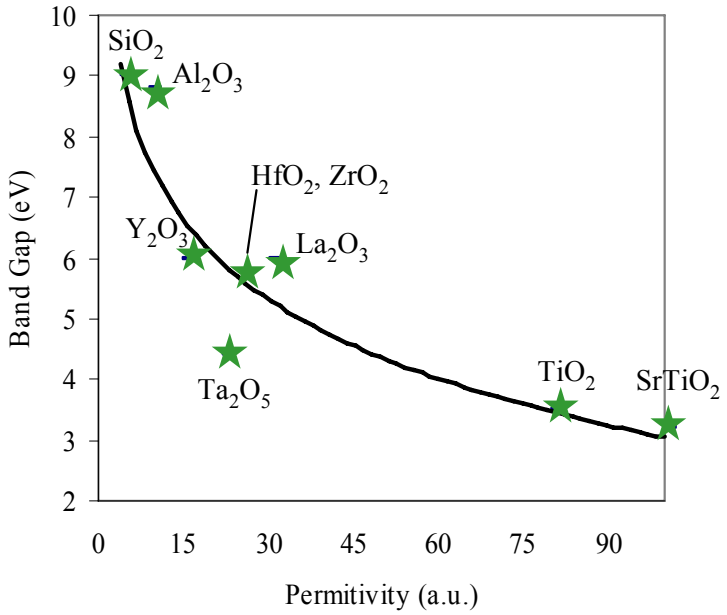


Figure 2.15: *The band gap energy, E_G, of prospective high-κ dielectrics as a function of permittivity (dielectric constant). Adapted from Robertson.*[33]

Here N is defined as the number of ions per unit volume, e is defined as the electronic charge, Z_T^* is defined as the transverse effective charge, m is defined as the reduced ion mass, and ω_{TO} is defined as the frequency of the transverse optical phonon (TO). Note that a negative ω_{TO} is indicative of a ferroelectric material. The dielectric constant is heavily controlled by the magnitude of transverse effective charge, defined as,

$$Z_T^* = 4\alpha(1-\alpha^2)n \qquad \text{Equation (2.11)}$$

Here, n is a material dependent constant (equal to 2 for s-p interaction (oxides such as SiO_2) and 7/2 for p-d interactions (high-κ dielectrics). The term α is the polarity of the dielectric and can be defined as the disproportion between ionic and covalent nature of the oxide bond,

$$\alpha = \frac{E_{bond,ionic}}{\left(E_{bond,covalent}^{\ 2} + E_{bond,ionic}^{\ 2}\right)^{1/2}} \qquad \text{Equation (2.12)}$$

Here, $E_{bond,covalent}$ and $E_{bond,ionic}$ are the respective energies formed from a covalent and ionic bond. The square root of the squared sum of the energies (the denominator of **Eqn. (2.12)**) is

also defined as the band gap energy. Thus, an inverse relation exists between the dielectric constant and the band gap energy of the dielectric.

Since the band gap energy (and band offset) decreases with an increase in dielectric permittivity, the number of potential dielectrics that can be used in the MOSFET structure is decreased. Dielectrics with higher permittivity (i.e. $SrTiO_3$ with $\varepsilon = 200$ @ room temperature) are typically used for dynamic RAM (DRAM) devices, where recharging of each MIM capacitor is necessary due to high leakage rates. Obviously the function of the dielectric in a MOSFET device is very different, as the leakage must be minimized at all cost to control the channel. The most suitable dielectric in terms of high permittivity and high conduction band offset appear to be 4d and 5d quadra-valant metals oxides (HfO_2 and ZrO_2) and tri-valant metal oxides (lanthanides, Ln_2O_3). The potential of lanthanide oxides will be discussed in **§2.4**.

2.3.4 Thermodynamic & Kinetic Considerations

As noted in **§2.1.2**, the most stringent (and deleterious) MOSFET FEOL processing step is the source/drain activation anneal that consists of a 5-10 second activation anneal ranging between 995 and 1050 °C. However, a gate-last approach is being examined as a method to reduce the thermal exposure to ~500-600 °C by performing the activation anneal prior to the gate stack deposition.[25] Annealing to passivate defects would still be necessary after the gate dielectric and electrode deposition. Nevertheless, a the dielectric must be able to withstand mid-level (500-600 °C) and a high-temperature (~1000 °C) annealing in order to be considered as a suitable replacement for SiO_2 in MOSFET.

Recall that the underlying objective in implementing a high-κ dielectric is to realize a gain in capacitance as well as physical thickness. In order for this to happen, it is preferred that the SiO_2 be removed completely and the high-κ be in direct contact with the silicon, since capacitance of stacked dielectric is evaluated in series,[19]

$$\frac{1}{C_{total}} = \frac{1}{C_1} + \frac{1}{C_2} \cdots + \frac{1}{C_n} \qquad \text{Equation (2.13)}$$

This implies that an interfacial layer consisting of pure or partial SiO_2 results in a decrease in the overall capacitance of the gate stack. In addition, metal silicide formation can lead to defect traps that serve to assist leakage current mechanisms. Therefore, it appropriate to also examine the silicide and SiO_2 formation that is expected at the interface between silicon and the high-κ dielectric.

Principle in identifying how suitable a high-κ would be in replacing SiO_2 is the thermodynamic stability of a high-κ material in contact with silicon. There are four common reaction scenarios for metals oxides that are deposited on silicon (reactions shown unbalanced):[35]

$$MO_x + Si \leftrightarrow M + SiO_2 \qquad \text{Equation (2.14)}$$

$$MO_x + Si \leftrightarrow MSi_z + SiO_2 \qquad \text{Equation (2.15)}$$

$$MO_2 + Si \leftrightarrow M + MSi_xO_y \qquad \text{Equation (2.16)}$$

$$MO_2 + Si \leftrightarrow MSi_z + MSi_xO_y \qquad \text{Equation (2.17)}$$

with *M* being the metal cation of the high-κ metal oxide being grown. Each reaction scenario considers that one product may be energetically favorable over another. For example, the first reaction (**Eqn. (2.14)**) would result in MO_2 decomposition and SiO_2 formation if the SiO_2 were more favorable product than the metal oxide. Thermodynamically, the standard Gibbs free energy of formation of the metal oxide, $\Delta G_f^{o}{}_{,high\text{-}\kappa}$, is less negative than the standard free energy of formation of SiO_2, $\Delta G_f^{o}{}_{,SiO2}$. Likewise, **Eqns. (2.15)** and **(2.17)** suggest that a metal silicide could be formed and **Eqns. (2.16)** and **(2.17)** suggest that a metal silicate could be formed. If energetically favorable, SiO_2 or silicate formation results in a decrease in the overall dielectric constant of the oxide. A metal silicide results in a leakage increase and a mobility decrease due to defect formation.[36]

In terms of SiO_2 formation compared to metal oxide formation, **Fig. 2.16** shows ΔG_f^o as a function of temperature for a number of high-κ dielectrics. This type of plot, also referred to as an Ellingham diagram, allows for comparison of the reactions on a per mole O_2 basis. It is observed that the majority of high-κ dielectrics that are thought of as candidate replacements for SiO_2, have a lower ΔG_f^o than SiO_2. This means that in contact with silicon and with sufficient thermal energy, the high-κ metal reaction with oxygen is favored over a similar reaction with silicon. The equilibrium oxygen pressure can be calculated from ΔG_f^o by,

$$pO_2 = P_{atm} \exp\left(\frac{\Delta G_f^o}{RT}\right) \qquad \text{Equation (2.18)}$$

with P_{atm} being atmospheric pressure (760 Torr), T being the temperature, and R being the

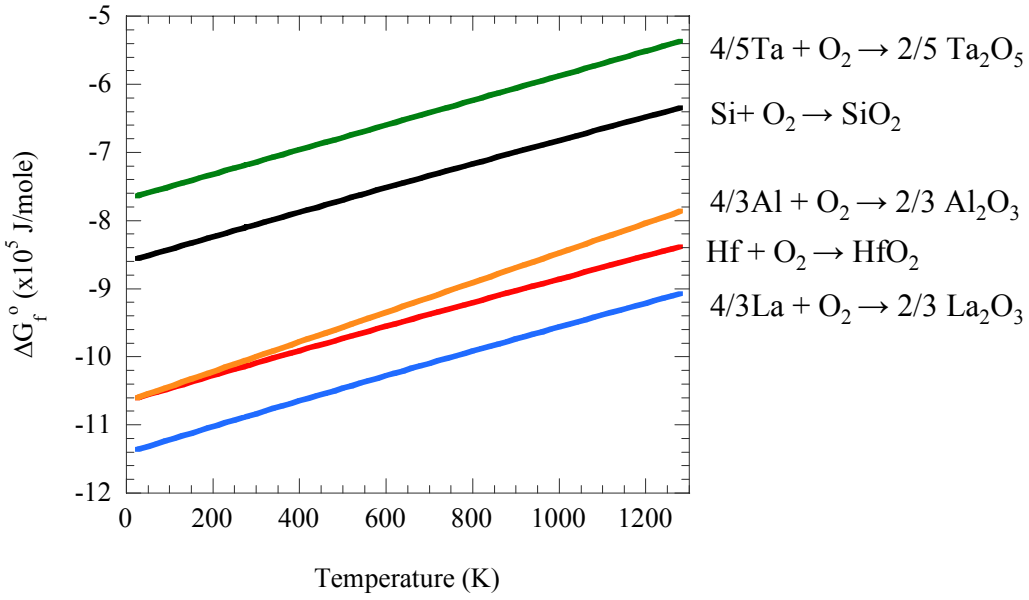


Figure 2.16: *Ellingham diagram of representative high-κ dielectrics showing the free energy of formation as a function of temperature. Free energy of formation determined for the reaction equations shown to the right of the figure are calculated on a per mole basis.*

universal gas constant (8.314 J/mol K). For SiO_2 at 1000 K, a pO_2 $<10^{-29}$ Torr is required for decomposition of the oxide. For La_2O_3, the decomposition occurs at a 1000 K when the pO_2 is less then 10^{-40} Torr. Therefore, oxide decomposition is highly unlikely.

The stability of high-κ oxides in terms of silicide formation or preference to SiO_2 formation has been well analyzed. For example, a problem observed with many complex dielectric systems used in oxide superconductors, ferroelectrics and ferromagnetics is the instability of the oxide on SiO_2. In an analysis to examine buffer layers for such complex oxides that are unstable on silicon, a suitable set of dielectrics have been identified as appropriate buffer layers by evaluating the reaction **Eqns. (2.14)-(2.17)**. It is noted that this study is primarily focused on epitaxial film growth of complex dielectrics. A number of oxides that have melting points or decomposition temperatures less then 1000 K are deemed unacceptable for subsequent epitaxial growth of the complex oxide that require >1000 K deposition temperatures. Also, a lack of thermodynamic data on silicide formation (**Eqn. (2.15)**) and silicates (**Eqn. (2.17)**) prevents a complete analysis of a number of systems, in particular the lanthanide oxides. A set of oxides for which the required thermodynamic data available in literature suggest stability on silicon included SrO, CaO, BaO, HfO_2, ZrO_2, Al_2O_3, Y_2O_3, and La_2O_3.[35] This list of oxides is preliminary, given the lack of data and the systems chosen to study based on thermal limits. This list does, however, offer insight as to candidate dielectrics to achieve a reaction free interface with silicon for MOSFET devices and for use as buffer layers. For an example of the latter, it is shown that TiO_2 is unstable on silicon as it is favors formation of SiTi and Si_2Ti over TiO_2. However, by using a stable SrO buffer layer on silicon, it is possible to achieve $SrTiO_3$ growth without observing the instabilities.

The thermodynamic analysis described thus far is sufficient for examining the driving force for reactions to proceed for oxides of sufficient oxidation and crystallization (epitaxial). However, poor dielectric performance after the high-temperature annealing can result from the oxidation condition and morphology of the dielectric. In an effort to compromise, silicates are proposed as being much more stable, leading to a discussion and analysis of metal silicates in comparison to metal oxides.

Although it has been shown in the Ellingham diagram, **Fig. 2.16**, that metal oxides are stable down to extremely low oxygen pressures, oxygen vacancies still exist in high-κ dielectrics after growth. During growth processing, as discussed earlier in **§2.3.2**, the oxygen pressure during physical vapor deposition growth methods can significantly alter the oxidation rate of both the silicon surface and the metal being deposited. In a similar way, chemical vapor deposition methods can also succumb to similar problems, by insufficient reaction between the precursor and the oxygen. It is believed that the ΔG_f^o for an oxygen deficient metal oxide can be lowered by an increase in oxygen content (oxidation anneal) or by reaction with silicon.[37] The latter, of course, being the formation of a silicide. The basis for this is the existence of an equilibrium state for every oxide in which some oxygen vacancies are allowed without forming a silicide. For example, provided with sufficient bulk thermodynamic data it was determined that a 6% deficiency of oxygen is allowed for zirconium oxide (i.e. $ZrO_{0.94}$). If additional oxygen vacancies are created beyond this point, a silicide is likely to form.

Perfectly lattice matched epitaxial oxides, like the buffer oxide previously mentioned, are a theoretically ideal solution for high-κ dielectrics.[35] However, wafer throughput is very low using epitaxial growth methods. Also, the thermal stability of epitaxial films is often insufficient and interfaces, even when epitaxial, appear to involve complicated structures often including "silicate" phases ~1-2 Å thick. In comparison to polycrystalline films, amorphous dielectrics are preferred since grain boundaries and surface facets are observed to be leakage current pathways.[22] In addition, some amorphous films can have a homogenous and featureless morphology, thus having excellent reproducibility. Unfortunately, the crystallization temperature for some potential high-κ materials in MOSFET devices is below 900 °C. It is obvious that a thermal budget required for the source/drain activation anneal (1000 °C, 5 sec) will result in a polycrystalline dielectric for most desirable high-κ dielectrics. In fact, the crystalline nature of the films is realized even during the film growth itself. By using a glass-former, such as SiO_2, it is possible to increase the resistance to crystallization.[22] Additionally, it may be feasible to retain the naturally ideal interface of SiO_2 and silicon, which would serve as a buffer layer for high-κ dielectric overlayer.[22]

However, the system must be carefully tailored due to the decrease in capacitance from the SiO_2 incorporation.

When considering a silicate system, it is necessary to examine phase separation that can lead segregated regions of metal oxide and SiO_2.[38] The metal oxide would thereby have an increased opportunity to form a silicide via the reaction scenarios already discussed. The stability of metal-oxide silicate systems is best understood using a phase diagram analysis. For example, consider the phase diagrams of the ZrO_2-SiO_2, HfO_2-SiO_2 and La_2O_3-SiO_2 systems show in **Figs. 2.17-19**. A common feature among the phase diagrams is a liquid-liquid immiscibility region that tends to higher SiO_2 concentrations. Note that the liquid-liquid immiscibility region is expected to exist for the HfO_2-SiO_2 system due the broad

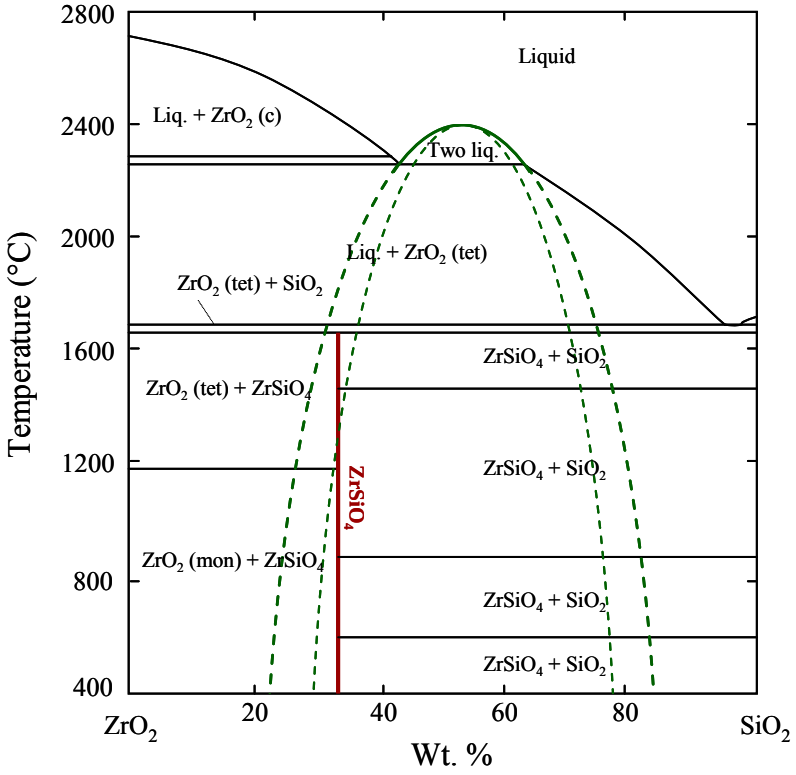


Figure 2.17: *The thermodynamic phase diagram for ZrO_2 – SiO_2 chemical. Adapted from Maria.*[39]

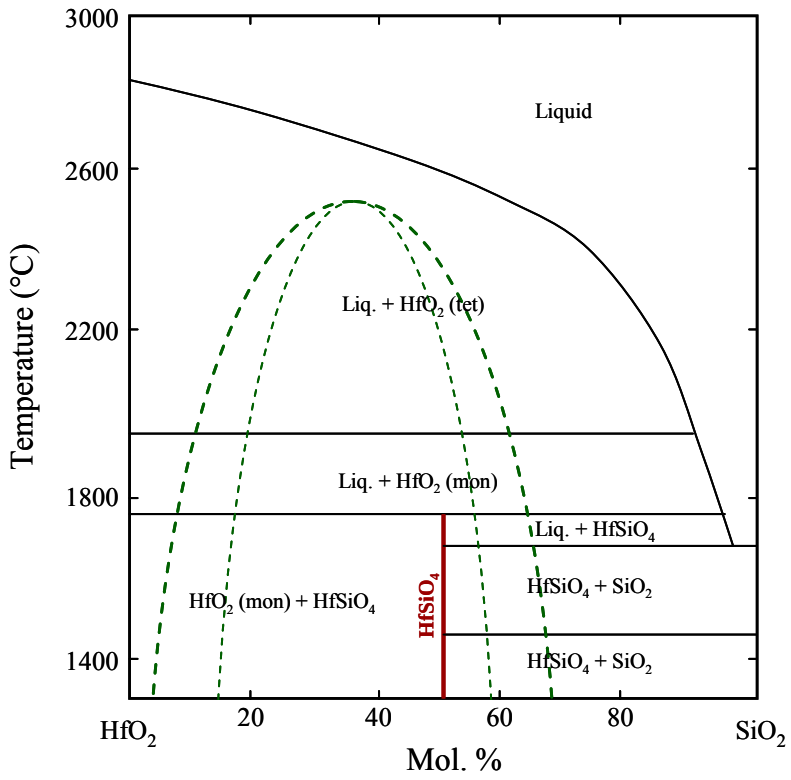


Figure 2.18: *The thermodynamic phase diagram for HfO_2 – SiO_2 chemical. Adapted from Maria.*[39]

nature of the sub-liquidus line.[39] In the hafnia and zirconia systems, a single silicate phase is shown as $MSiO_4$ (or MO_2:SiO_2), lying within liquid-liquid immiscibility region known for ZrO_2-SiO_2 and expected for HfO_2-SiO_2 systems. Therefore, as the film is quenched, the equilibrium state of the metal silicates is formed along with the metal oxides. This phase separation leads to pockets of crystalline HfO_2 and ZrO_2 in an amorphous metal silicate media.[38,40] Considering the La_2O_3-SiO_2 system, the liquid-liquid immiscibility region is far removed from the $LaSiO_5$ (La_2O_3:SiO_2) equilibrium state, being closer to SiO_2. As a result, a silicate with a congruent melting point is formed with compositions between $LaSiO_5$ and the $La_2Si_2O_7$ (La_2O_3:$2SiO_2$). Upon quenching and subsequent cooling, the silicate nature of the film is retained along with a SiO_2 intermixing.[38] For this to occur, a significant amount of intermixing between the metal oxide and SiO_2 is required. Most importantly, the glass-forming capabilities of SiO_2 in the metal oxide are retained in that the crystallization

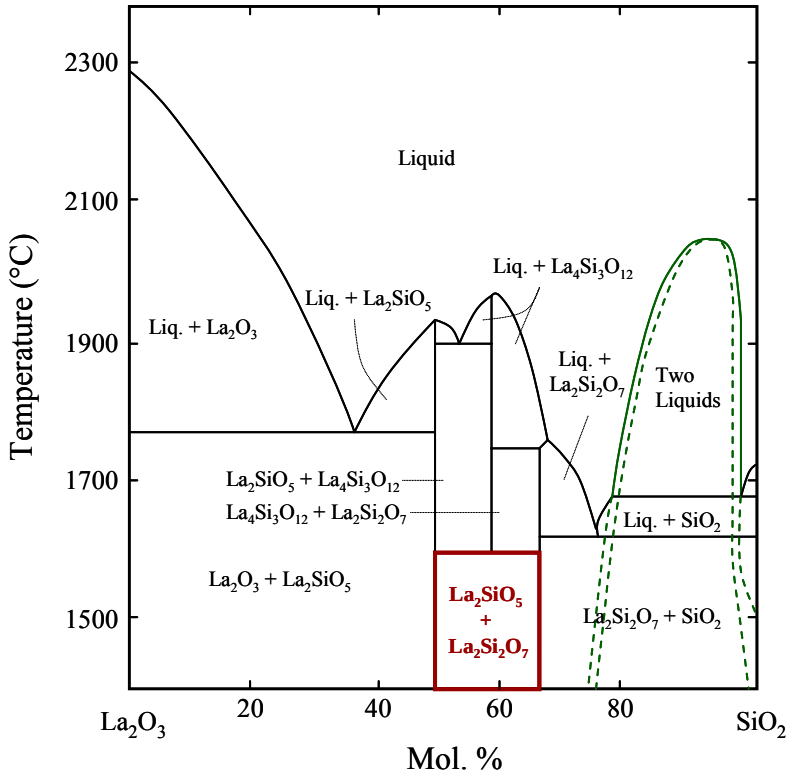


Figure 2.19: *The thermodynamic phase diagram for La_2O_3 – SiO_2 chemical system. Adapted from Maria.*[39]

temperature can be increased well beyond that of La_2O_3. An added benefit of the silicate reaction is that SiO_2 created at the silicon interface is likely to react with oxides such as La_2O_3 to form a silicate. This silicate reaction has the opportunity to increase the overall capacitance of the dielectric. The negligible influence of the liquid-liquid immiscibility region is observed for most tri-valant metal oxides (Y, Sc, and lanthanide silicates[41]) with subtle differences.

Thus far, metal oxide stability on silicon and the tendency for silicate formation has been discussed. It is necessary at this point to project the possible outcomes of annealing a high-κ dielectric on silicon with and without a silica buffer layer. This analysis considers that the high-κ oxide reaction is more favorable than SiO_2 formation (**Eqn. (2.14)**). First consider a metal oxide deposited on the bare silicon and subject to annealing (in an oxidizing environment), as shown in **Fig. 2.20**:

- *RS1* (*reaction sequence 1*) considers a metal silicide being formed based on ΔG_f^o of either reaction or due to the fact that oxygen is unable to react quick enough with the oxygen deficiency of the metal oxide to prevent the onset of metal silicide formation.

- In *RS2*, the oxygen from the annealing environment first satisfies the oxygen deficiency in the metal oxide to the point that the oxide is stoichiometric. The excess oxygen diffuses to the substrate and reacts to form SiO_2 and continues to increase in thickness, remaining unreacted with the metal oxide.

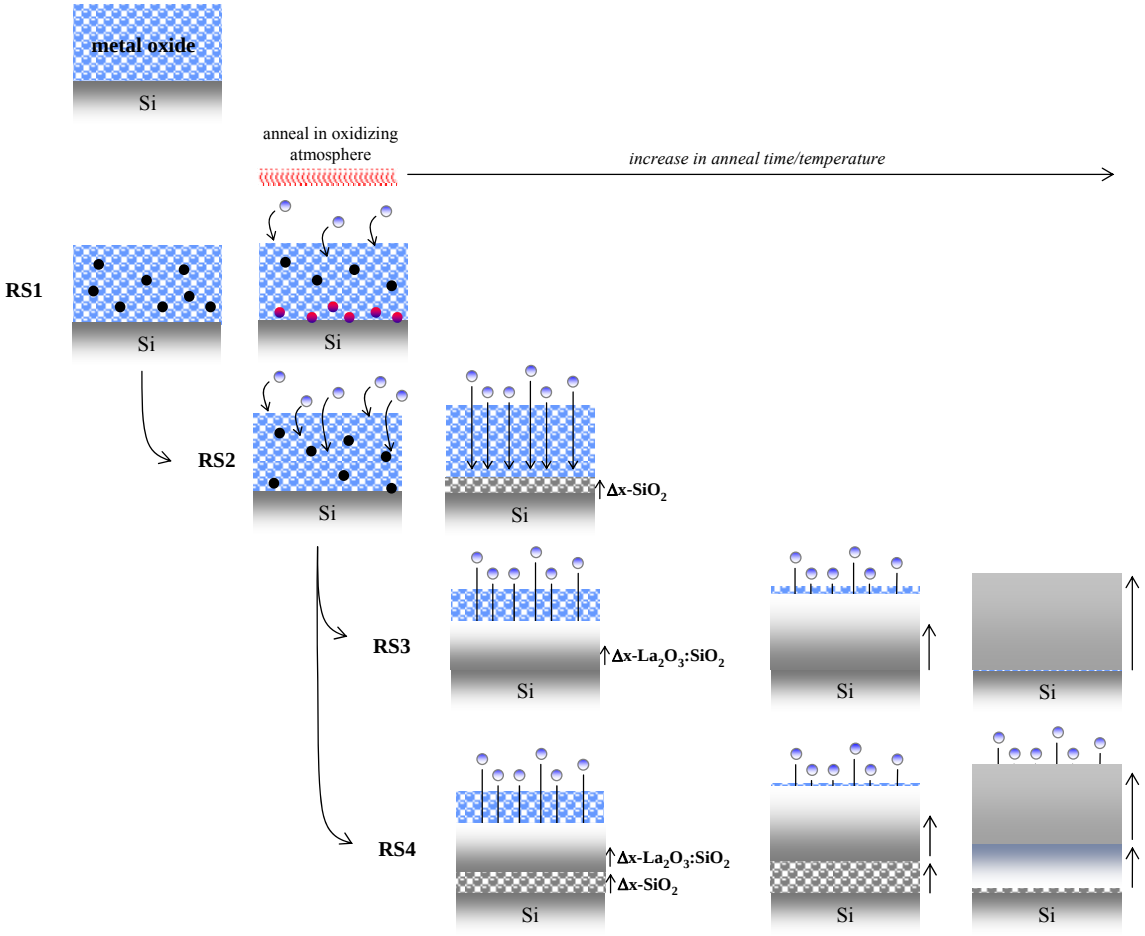


Figure 2.20: *Various reaction sequences (RS) that are predicted based on thermodynamic and kinetic considerations outlined in the text, for oxides that prefer metal oxide formation over SiO_2 formation.*

- *RS3* considers the possibility of the silicate reaction. As the SiO_2 is being formed at the silicon interface, it in turn is reacting with the metal oxide to form a silicate. A concentration gradient of reacted SiO_2 arises (high SiO_2 at the silicon interface to a low SiO_2 at the upper interface of the metal oxide) with concentrations of the metal silicate at the equilibrium states. As SiO_2 formation increases, the concentration gradient decreases until an equilibrium point is reached.

- *RS4* is similar to *RS3* in that a silicate reaction takes place. However, the formation of SiO_2 is more rapid than the reaction to form a silicate. A concentration gradient exists, but is heavily weighted toward the silicon interface due to rampant SiO_2 formation. An equilibrium point is never reached.

Note that similar reaction sequences can be observed with a pre-existing SiO_2 interfacial layer that is much thinner than the metal oxide deposited on it. The only substantial difference is the ability for the pre-existing interfacial SiO_2 layer to slow the diffusion of oxygen to the silicon interface and prevent the silicide formation of *RS1*. Note that with an interfacial oxide already present, SiO_2 growth during annealing is no longer needed to prevent silicide formation. This means that the ideal anneal environment would be that in a low oxygen pressure.

In general, the consequence of anneal processing the gate dielectric can be classified under one of the four reaction sequences (*RS1-RS4*), depending highly on rates of reaction and the amount of oxygen present during the growth and annealing. The majority of studies on dielectric growth and performance deal with controlling the oxidation state of the dielectric, the interfacial SiO_2 formation, the silicate reaction, and the oxidizing environment of the anneal. Examining *RS1-RS4* and relating to the thermodynamic and kinetic properties described earlier, it is obvious that each of these reactions plays an integral role in the control of the final dielectric composition. It is also interesting to point out the kinetic limitations that are observed. If enough oxygen in the anneal environment is available, then SiO_2 growth can out-weight the high-κ dielectric affect in *RS2* and *RS4*. The ideal case would be *RS3*, where the silicate reaction is limited by the equilibrium state of the silicate, though in

practice this rarely occurs. A lesson learned from this analysis is that there might be many ways to achieve similar low EOT results, but the oxygen pressures, thermal budgets, and film thicknesses must be controlled precisely.

2.4 Lanthanide-based Oxides

In comparison to other dielectrics such as HfO_2, there is very little experimental data on the lanthanide (or rare earth) oxides. For a working list of references on lanthanide oxide studies pertaining to the use as replacement high-κ materials, the reader is referred to **Tables 2.4-2.7**. **Table 2.4** lists references in accordance with growth processes commonly used. The categories are divided into chemical vapor deposition (CVD), atomic layer deposition (ALD), vacuum deposition techniques such as molecular beam or E-beam (MBD, EBD) and other physical vapor deposition techniques (i.e. RF-sputtering and pulsed laser). Each growth process has been previously discussed in **§2.3.2**. **Table 2.5** separates the literature focusing on electrical characterization into categories of capacitance-voltage (CV) or current-voltage (IV), interface trap density (D_{IT}), MOSFET device analysis, and band offset alignment on silicon. **Table 2.6** partitions the literature with respect to analytical characterization, the categories being x-ray diffraction (XRD), x-ray photoemission spectroscopy (XPS), transmission electron microscopy (TEM), and depth profiling (i.e. electron energy loss, Auger, or secondary ion mass spectroscopy). Finally, **Table 2.7** lists references that concern lanthanide silicate formation. It can be approximated from this working list that the majority of the analysis is associated with La, Pr, Gd, Dy, and Er-oxide. In terms of a silicate, the majority of the analysis has been with La, Pr, and Gd-silicate. The suggestion is that there is a recognized ease of processing with these particular lanthanide elements in terms of thin film deposition, stability on silicon, and acquisition of electrical data.

It is also noted that few MOSFET device characterization studies have been performed with respect to these lanthanide oxides. The indication is that research concerning these oxides is still in its infancy and unsuitable in consideration of standard MOSFET processing. A justification in this regard is that the majority of the referenced work has been published

since 2000. This list does not include work on the lanthanide inclusion into a HfSiO(N) gate stack, in which benefits applicable to the MOSFET device function has been observed,[42,43] a topic of **Chapter 6**. Description of selected publications will be appropriately referenced in **Chapters 4-6**, while discussing the work presented concerning film and device processing, electrical characterization, and analytical characterization. Since the majority of this work has to do with lanthanum oxide and silicate, specific attention is directed toward lanthanum-based dielectrics properties.

Table 2.4: *Literature references for information on lanthanide oxide growth methodology using chemical vapor deposition (CVD), atomic layer deposition (ALD), vacuum deposition techniques such as molecular beam or electron-beam (MBE, EBD) and other physical vapor deposition techniques (i.e. RF- sputtering and pulsed laser).*

	CVD	ALD	MBD or EBD	other-PVD
La	29, 44, 45, 46, 47, 48, 49, 50, 51	52, 53, 54, 55	38, 56, 57, 58, 59, 60, 61, 62	
Ce			63, 64, 65	66
Pr	29, 44, 45, 67, 68, 69	29, 70, 71	41, 56, 69, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82	83, 84
Nd	29, 44, 45, 85, 86, 87	88, 89	90, 91	92
Pm				
Sm	45	88	56, 93, 94, 95, 96	83
Eu	45, 97	88	56, 98	45, 97
Gd	29, 44, 45, 99, 100	29, 71, 88	56, 57, 101, 102, 103, 104, 105, 106,	107
Tb	45	108	83	45
Dy	45	88	95, 109, 110, 104	111, 112
Ho		88	95, 113	
Er	45	88, 114, 115	116, 117, 118, 119	83, 120
Tm	45	88		45
Yb	45	121, 122	56, 58, 109, 123	83
Lu		121, 122, 124, 125, 126, 127	56, 108, 122	128, 129

Table 2.5: *Literature references for information on lanthanide oxide electrical characterization divided into categories of capacitance-voltage (CV) or current-voltage (IV), Interface trap density (D_{IT}), MOSFET device analysis, and band offset alignment with silicon.*

	CV/IV	D_{IT}	MOSFET	Band Offsets
La	38, 44, 47, 51, 52, 53, 55, 56, 58, 59, 60, 61, 62, 130, 131, 132, 133	44, 59, 134, 133	135, 136, 137	47
Ce	63, 66, 138, 139	138, 139	63, 66, 138, 139	138, 139
Pr	29, 44, 56, 70, 74, 81, 83, 140	44	78	73, 81, 141, 142, 143
Nd	44, 90, 144, 85, 92, 88	44, 90	44, 85, 88, 90, 92, 144	44, 90
Pm				
Sm	56, 83, 88, 93, 94, 140			96, 145
Eu	56, 88, 97, 98, 146	146		
Gd	44, 56, 99, 101, 102, 104, 106, 107, 140, 147	44		
Tb	83, 108			
Dy	88, 104, 110, 111, 112, 140, 148, 149	109, 150	111, 150	
Ho	88, 113			
Er	83, 88, 116, 117, 118, 119, 120			
Tm	88			
Yb	56, 58, 83, 121, 123	109, 121		123, 145
Lu	56, 108, 121, 122, 124, 128, 129, 151	121, 128		127

Table 2.6: *Literature references for information on lanthanide oxide analytical characterization divided into categories of x-ray diffraction (XRD), x-ray photoemission spectroscopy (XPS), transmission electron microscopy (TEM), and depth profiling (electron energy loss spectroscopy, Auger, or secondary ion mass spectroscopy).*

	XRD	XPS	TEM	Depth Profiling
La	**44, 29, 51, 52, 53, 54**	**44, 47, 50, 51, 53, 131, 132, 152, 153**	**44, 51, 55, 57, 58, 60, 130**	**51, 57, 130, 134, 153, 154**
Ce	**63, 64, 66**	**155**	**63, 64**	
Pr	**29, 44, 68, 70, 72, 75, 79, 83**	**44, 69, 74, 76, 82, 83, 140, 156, 157**	**44, 72, 74**	**70, 76, 143**
Nd	**29, 44, 85, 87, 88, 89, 90, 92**	**44, 80, 92**	**44, 144, 87**	
Pm				
Sm	**88, 93, 95**	**95, 140**		
Eu	**88, 97, 146**	**156**		
Gd	**29, 44, 99, 103, 107**	**44, 99, 103, 104, 140, 147, 156**	**44, 57, 102, 105, 106**	**57, 105, 158**
Tb				
Dy	**88, 95, 112, 148**	**95, 104, 110, 140, 159**	**110**	**160**
Ho	**88, 95**	**95**		
Er	**88, 117, 118, 120, 161, 162, 163**	**120**	**116, 117, 162, 164**	**116**
Tm	**88**			
Yb		**122, 156**	**58**	
Lu		**124, 122, 151**	**126, 128, 129**	**160**

Table 2.7: *Literature references for information on lanthanide silicate formation.*

La	**29, 38, 39, 45, 50, 51, 57, 131, 154, 165, 166, 167, 168, 169, 170, 171, 172, 173**
Ce	**65, 155**
Pr	**29, 41, 45, 67, 69, 70, 76, 79, 80, 81, 82, 84, 143, 157, 174, 175**
Nd	**92, 45, 176, 177**
Pm	**45**
Sm	**45**
Eu	**45**
Gd	**45, 57, 105, 147, 158, 159, 178**
Tb	**45**
Dy	**45, 110**
Ho	
Er	**45, 120**
Tm	**45**
Yb	**45, 122, 178**
Lu	**122, 151, 178**

2.4.1 Structural and Thermodynamic Considerations

Lanthanide (La-Lu) based oxides are of interest beyond MOSFET devices specifically in applications of solid oxide fuel cells, and ferromagnetics. All naturally occur on earth except for promethium, which is radioactive. In reality, lanthanides are more abundant in the Earth's crust than many transition metals. In their pure oxide form, lanthanide oxides can be differentiated by stable structures found at room temperature: hexagonal P3m, (La_2O_3–Nd_2O_3), monoclinic C2/m (Pm_2O_3–Gd_2O_3), and cubic Ia3 (Tb_2O_3–Lu_2O_3). Metastable polymorphs are known to exist for Pm_2O_3 (hexagonal and cubic) and Sm_2O_3–Gd_2O_3

cubic).[179] Upon annealing, additional phase transformations are known to occur, such as La_2O_3 transforming from a hexagonal phase to a cubic phase.

Various properties of the lanthanide elements and lanthanide oxides obtained from literature are shown in **Table 2.8**. Provided is the electron configuration of the lanthanide elements as well as the bond length, ionic radius, enthalpy of formation, and standard enthalpy of formation (ΔH_f^o) of the oxides and silicates.[179,180,181]

The standard Gibbs free energy of formation of the lanthanide-based oxides as a function of temperature is shown in **Fig. 2.21** for the sesquioxide reaction,[180]

$$2Ln + \frac{3}{2}O_2 \leftrightarrow Ln_2O_3 \qquad \text{Equation (2.19)}$$

It is observed that all of the lanthanide oxides are prone to reaction with oxygen when evaluating the trivalent state of the metal ions. Based on the earlier comparison between La_2O_3 and SiO_2, shown in **Fig. 2.16**, all are assumed to be more reactive with oxygen than SiO_2. In addition a periodic trend is observed. **Figure 2.22** shows ΔG_f^o evaluated at 1000 K as a function of increasing atomic number and compared to the ionic radius for the same group. As the ionic radius is decreased, the negative energy of formation between the lanthanide metal and oxygen increases. Not adhering to this trend are Eu and Yb oxides. **Figure 2.23** show the results (also shown in **Table 2.8**) of a survey study conducted that averages literature data on the standard enthalpy of formation, ΔH_f^o, for the lanthanide oxides. The same trend is observed with outliers being Eu and Yb. It is shown in **Table 2.8** that the f-orbital of Eu and Yb are half and fully filled, respectively. This results in a divalent state of the metal that requires an added energy for transition to the trivalent end state.

A deleterious aspect of lanthanide oxides is the relatively high hydroscopic nature of the materials. As a high-κ material in a MOSFET, it is thought that moisture absorption in the oxide might result in a degradation of the electrical properties of the device. An XPS study comparing the hydroxide formation of various lanthanide oxides shows that the hydroscopic nature of the oxide decreases with an increase in electronegativity and a decrease in ionic

Table 2.8: *Pertinent properties of the lanthanide oxides and silicates.* ΔH_f^o *values obtained from Adachi.*[180]

	Electron configuration	Ln-O bond length nm	Ln-O ionic radius nm	ΔH_f^o @ 298.15K kJ/mol	Ln-silicate ΔH_f @ 298.15K kJ/mol	Ln-silicate ΔH_f^o @ 298.15K kJ/mol
La	[Xe] $5d^1 6s^2$	0.246	0.123	-1791.6±2.0	-63.7	-2766.0
Ce	[Xe] $4f^1 5d^1 6s^2$	0.244	0.115	-1813.0±2.0	-60.8	-2784.5
Pr	[Xe] $4f^3 6s^2$	0.238	0.114	-1809.9±3.0	-60.4	-2781.0
Nd	[Xe] $4f^4 6s^2$	0.238	0.112	1806.9±3.0	-59.6	-2777.2
Pm	[Xe] $4f^5 6s^2$	---	---	---	---	---
Sm	[Xe] $4f^6 6s^2$	0.235	0.106	-1823.0±4.0	-57.1	-2790.8
Eu	[Xe] $4f^7 6s^2$	0.233	0.106	-1650.4±4.0	-57.1	-2618.2
Gd	[Xe] $4f^7 5d^1 6s^2$	0.232	0.104	-1819.7±3.6	-56.2	-2786.6
Tb	[Xe] $4f^9 6s^2$	0.230	0.100	-1865.2±6.0	-54.2	-2830.1
Dy	[Xe] $4f^{10} 6s^2$	0.229	0.099	-1863.4±5.0	-53.7	-2827.8
Ho	[Xe] $4f^{11} 6s^2$	0.228	0.098	-1883.3±8.2	-53.2	-2847.2
Er	[Xe] $4f^{12} 6s^2$	0.227	0.096	-1900.1±6.5	-52.1	-2862.9
Tm	[Xe] $4f^{13} 6s^2$	0.225	0.094	-1889.3±5.7	-51.0	-2851.0
Yb	[Xe] $4f^{14} 6s^2$	0.224	0.093	-1814.5±6.0	-50.4	-2775.6
Lu	[Xe] $4f^{14} 5d^1 6s^2$	0.223	0.092	-1877.0±7.7	-49.8	-2837.5

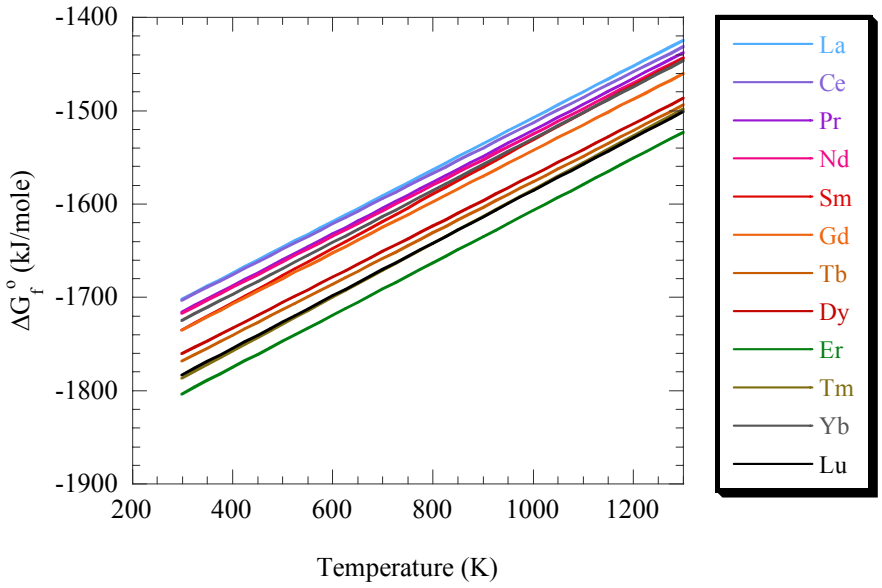


Figure 2.21: *Ellingham diagrams of representative for the lanthanide oxides high-κ dielectrics showing the free energy of formation as a function of temperature. Free energy of formation determined on a per mole basis.*

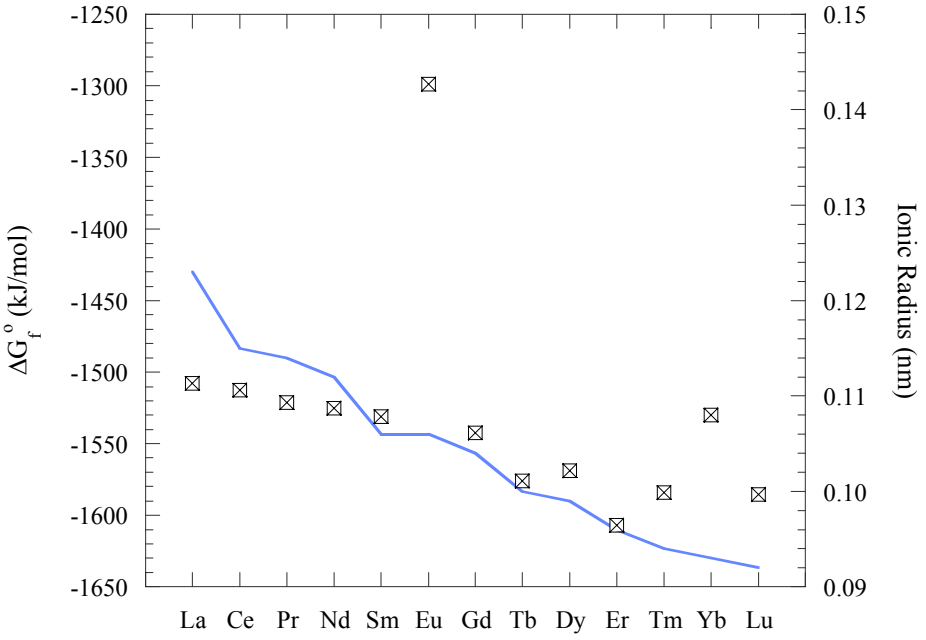


Figure 2.22: *Standard free energy of formation of the lanthanide oxides as a function of atomic number plotted against the ionic radius.*

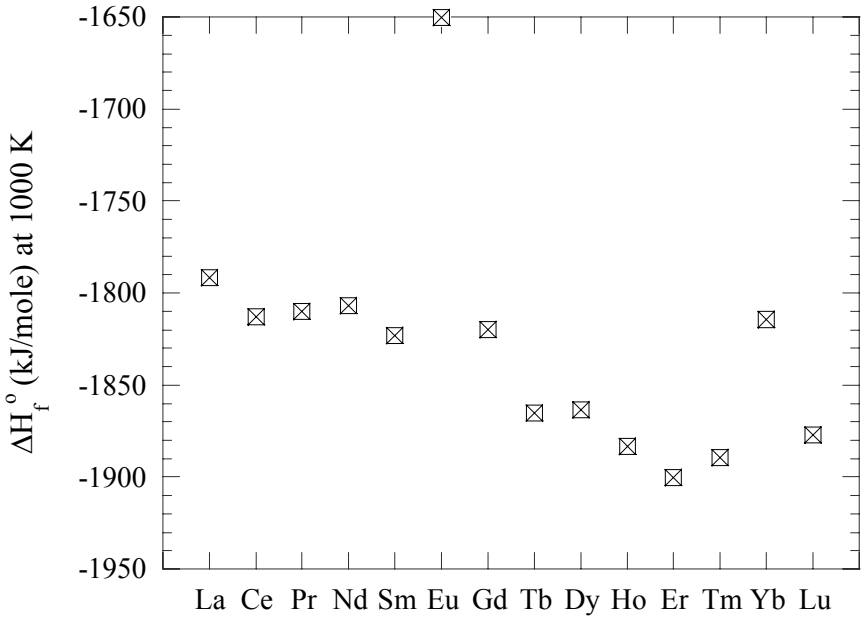
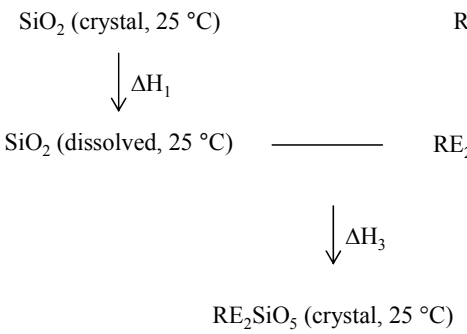


Figure 2.23: *The standard enthalpy of formation of the lanthanide oxides as a function of atomic number.*

radius.[140] It is thought that this result is due to the fact that the –OH radical has a similar outer electron configuration as a halogen atom (Group VIIB: Fl, Cl, Br, etc.); that is, a high electronegativity (≥ 3.0). Therefore, it is expected that the –OH radical has a similar high reactivity with metals having a low electronegativity. The lanthanide elements have a low electronegativity (≤ 1.5) and can therefore be prone to ionic bonding to form a hydroxide. It has also been determined that the hydroxide formation is noticeably slowed if the lanthanide oxide is reacted with SiO_2 to form a silicate.[166]

There is very little thermodynamic data available in literature on lanthanide silicates. However, general trends have been able to be determined using what sparse data is available. A main contributor has been the study in which the enthalpy of formation for Y_2SiO_5 and Yb_2SiO_5 was determined using high-temperature drop solution calorimetry.[182] The cycle used to predict the enthalpy of formation for the silicate is shown in **Fig. 2.24**, with an included table showing the enthalpy of formation predicted for Yb_2SiO_5. It was determined that the a linear relationship exists between ΔH_f^o of the metal silicates and the ionic potential,



for Yb_2SiO_5

ΔH_1	38.26	±	0.72	kJ/mol
ΔH_2	135.77	±	4.70	kJ/mol
ΔH_3	-223.5	±	6.45	kJ/mol
ΔH_{tot}	-49.45	±	8.17	kJ/mol

Figure 2.24: *The thermodynamic cycle used for an estimation of the formation enthalpy for lanthanide silicate. The table to the right lists the enthalpies used to approximate the enthalpy of the formation of Yb_2SiO_5. Adapted from Liang.*[182]

$$IP = \frac{z}{r} \qquad \text{Equation (2.20)}$$

with z being the ionic charge (+3) and r being the ionic radius. The ionic potential is strictly a measure of the basicity of the oxide, which aids in defining how stable a compound is when combining a basic and acidic oxide. In this case, the SiO_2 is the common factor relating the silicates of various lanthanide elements. The relationship with respect to atomic number of the lanthanide ions is listed in **Table 2.8** and plotted in **Fig. 2.25** with respect to predicted values for enthalpy of formation. The standard enthalpy of formation can also be predicted if the formation energies of the lanthanide metal oxide and the silica are added to the thermodynamic cycle. This cycle is shown in **Fig. 2.26**, along with the standard enthalpy of formation prediction for Yb_2SiO_5. Here it is observed that the standard enthalpy of formation for the silicate is much more negative than that of SiO_2 and Ln_2O_3, suggesting that silicate is the favored reaction when the two are in intimate contact. From the data for the standard enthalpy of formation of the lanthanide oxides provided by Cordfunke et al.[179] and shown in **Table 2.8**, it is possible to predict the standard enthalpy of formation for all of the lanthanide silicates. For the thermodynamic cycle shown in **Fig 2.26**, ΔH_1 (enthalpy of formation of SiO_2) is -910.7 kJ/mol and the ΔH_2 (enthalpy of formation for Ln_2O_3) is provided from **Table 2.8**, and the sum of ΔH_3-ΔH_5 is that derived from the enthalpy of formation and ionic potential relationship.

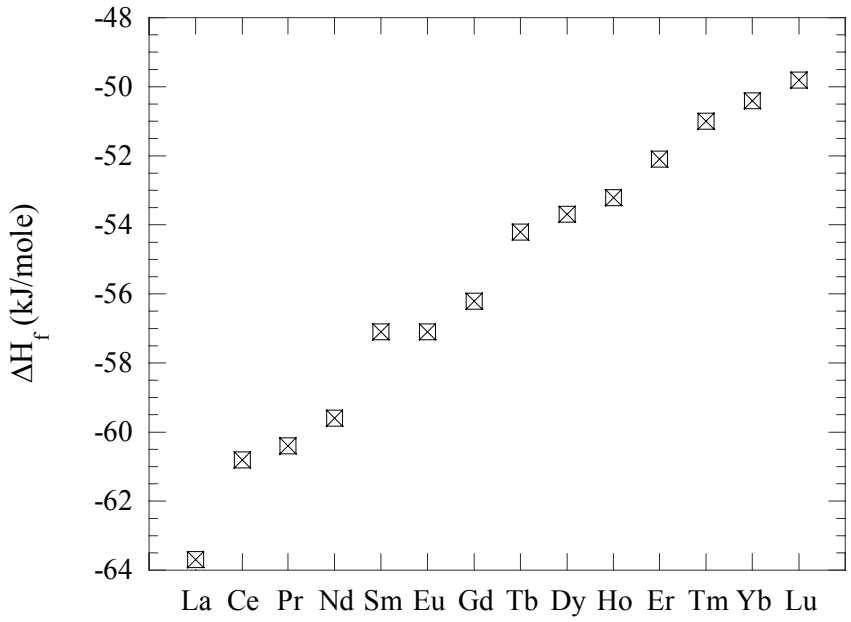
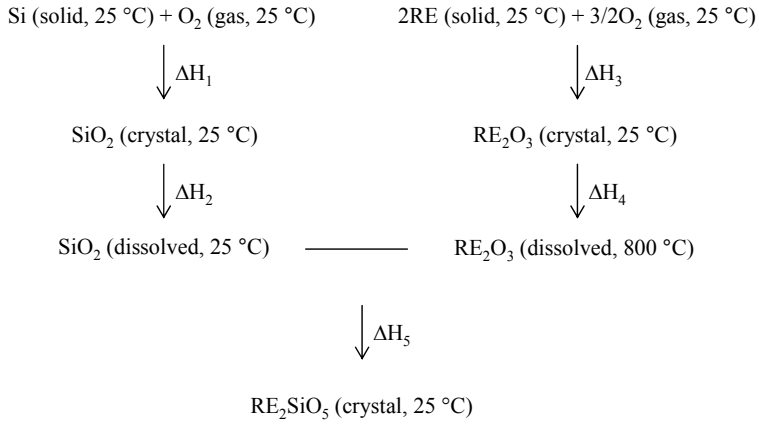


Figure 2.25: *The formation enthalpy for the various lanthanide oxides as approximated by the linear interpolation of the ionic potential (**Eqn. (2.19)**) and formation enthalpy.*



for Yb_2SiO_5

ΔH_1	-910.7	kJ/mol
ΔH_2	38.26 ± 0.72	kJ/mol
ΔH_3	-1814.6	kJ/mol
ΔH_4	135.77 ± 4.70	kJ/mol
ΔH_5	-223.48 ± 6.45	kJ/mol
ΔH_{tot}	-2774.75 ± 8.2	kJ/mol

Figure 2.26: *The thermodynamic cycle used for an estimation of the standard enthalpy of formation for lanthanide silicates. The table to the right lists the enthalpies used to approximate the standard enthalpy of the formation of Yb_2SiO_5. Adapted from Liang.*[182]

Figure 2.27 compares the calculated values for the standard enthalpies of formation for SiO_2, the lanthanide oxide, and the lanthanide silicate. For all cases, the silicate is the favorable reaction and is highly exothermic. The values given here agree well with values in a work that determined the enthalpies of formation for La-silicide, oxide, and silicate. These values were determined by total energy and force calculations using density functional theory.[183] In the work, standard enthalpies of formation of -1817.8, -2869.5, and -373.4 kJ/mol were obtained for La-oxide, La-silicate, and La-silicide, respectively. A majority of the value differential for the silicate, (-2765.9 kJ/mol based on work by Liang[182] and Cordfunke[179]) is due to the fact that different values of the enthalpy of formation for SiO_2 were used. It is worth noting that the silicide formation is the least favorable reaction route, although none of the analysis takes into consideration that the oxide or silicate could be oxygen deficient, a condition which can lead to a thermodynamic route for silicide formation.

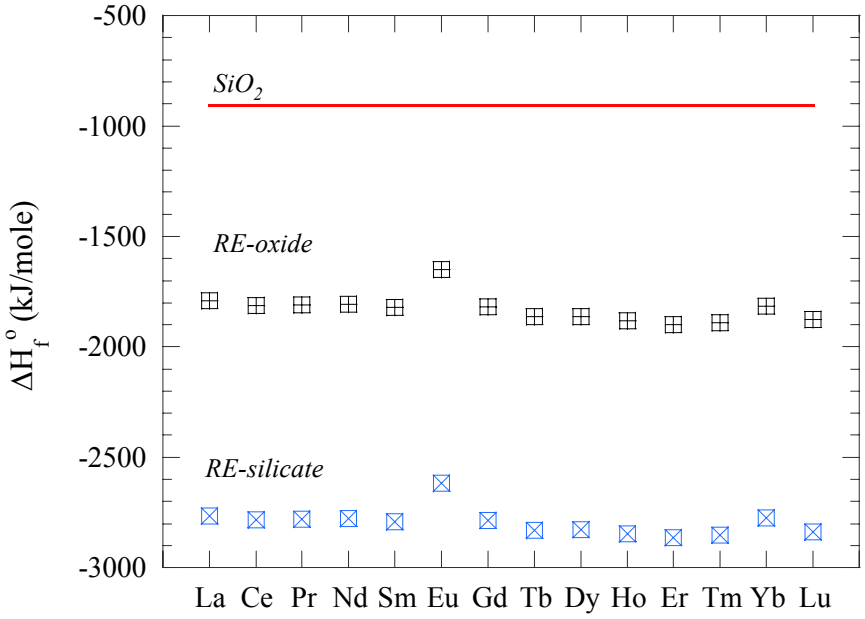


Figure 2.27: *A comparison of the standard enthalpy of formation for the lanthanide oxides (black), silicates (blue), and SiO_2 (red).*

2.4.2 Electrical Considerations

As noted in §2.3.3, the band gap of oxides is a measure of the difference between the valance band and the conduction band. For most oxides the valance band refers to the filled level of the oxygen 2p orbital. For lanthanide oxides, an additional 4f orbital needs to be considered.[180] When the f-orbital energy level lies between the standard conduction and valance bands, the band gap is determined by the energy difference between the highest filled state of the f-orbital and lowest empty state of the d-orbital. **Figure 2.28** shows the periodic trend observed for the band gap of the lanthanide oxides. For La_2O_3, the 4f orbital is empty and the valance band is given by the O-2p orbital. The half filled f-orbital (Gd) and the fully filled f-orbital (Lu), (see **Table 2.8**) represent configurations that have high stability. This is a result of the 4f energy level being below the valance band determined by the O-2p orbital. Therefore the band gap energy is of similar magnitude (E_G ~5.5 eV) for La_2O_3, Gd_2O_3 and Lu_2O_3. An anomaly is observed in E_G before these high stability cases that is onset at Ce_2O_3

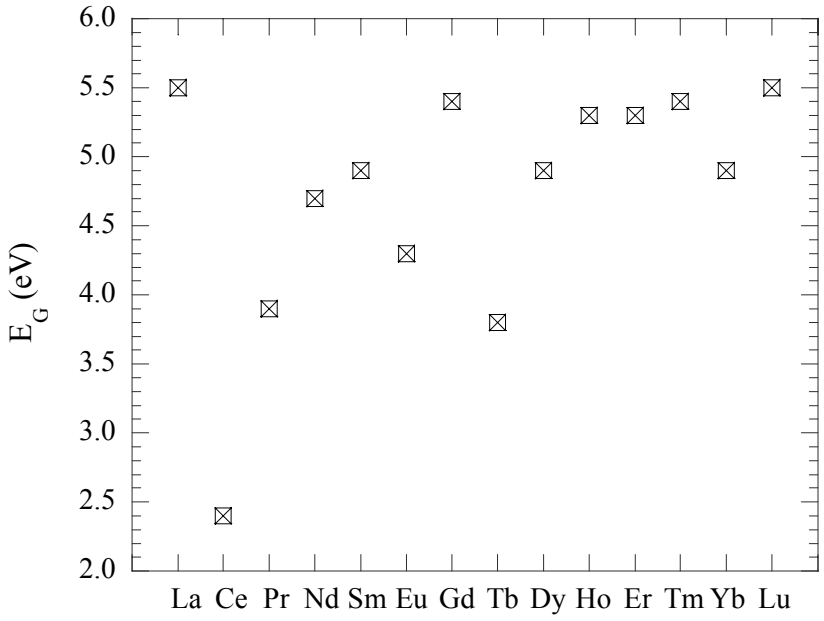


Figure 2.28: *The band gap energy of the various lanthanide oxides as a function of atomic number.*

and Tb_2O_3. Here the f-orbital energy level is greater than the valance band. This results in a decrease in E_G to a value which is approximated be the energy difference between the highest filled level of the 4f orbital and the lowest empty level of the 5d orbital. Note that this is an intra-atomic property as opposed to a inter-atomic property when E_G depends on the lanthanide metal and oxygen bond.

The dielectric constant and subsequent MOS electrical properties are known to vary depending on substrate preparation, growth method, growth thickness, annealing temperature, annealing condition, structural phase of film, etc. This variation in electrical properties makes a comparative analysis of the lanthanide oxides very difficult, especially when dealing with a metal oxide that is so prone to silicate reaction. Nevertheless, some classical bulk work has been performed on bulk dielectric properties, including an associated modeling of the observed trend.[184] Using bulk crystalline oxides, the dielectric constant was determined by capacitance measurements. **Figure 2.29**, shows the relationship between the

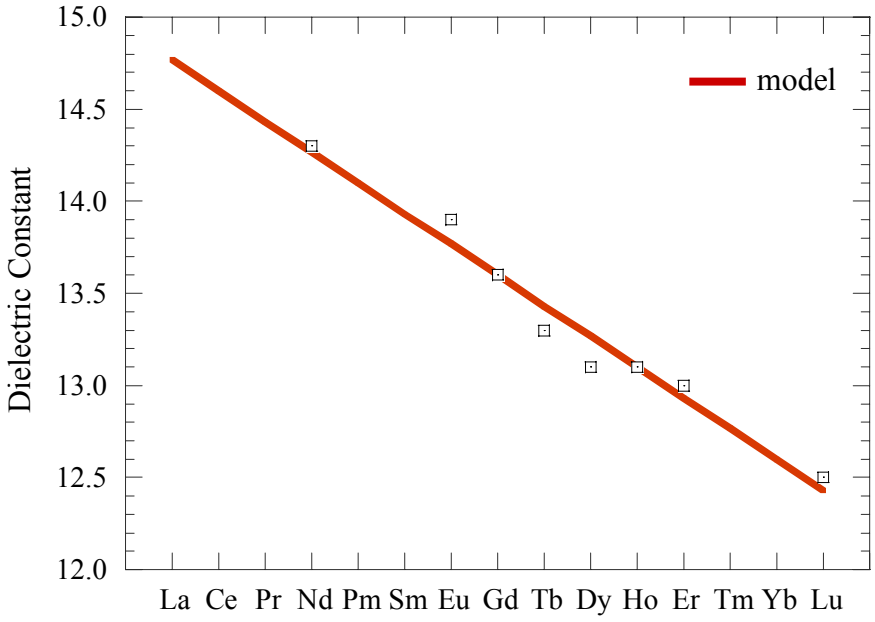


Figure 2.29: *The dielectric constant modeled (red) and observed experimentally in bulk crystals for various lanthanide oxides. Adapted from Xue.*[184]

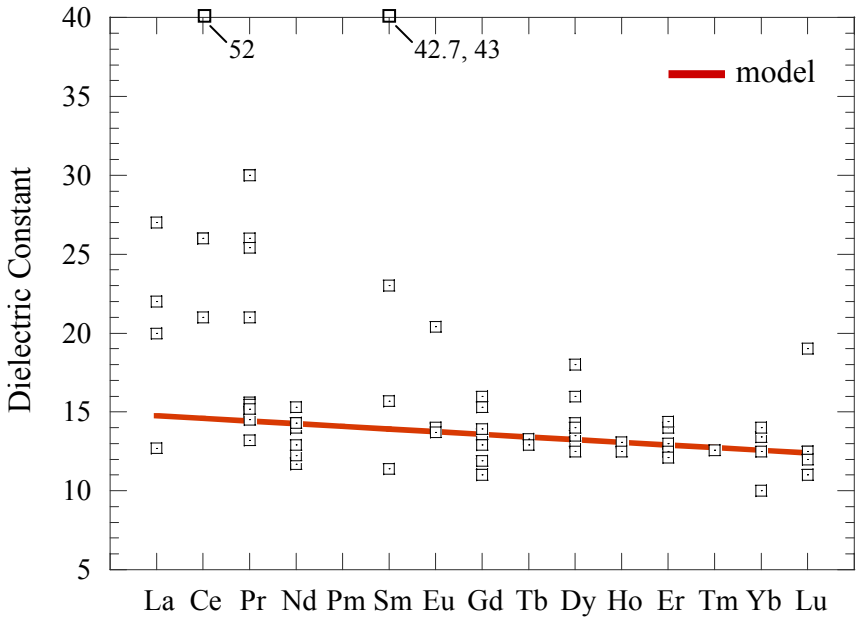


Figure 2.30: *A literature survey of the dielectric constant obtained for the various lanthanide oxides. Raw data and references shown in **Table 2.5**.*

lanthanide element (or atomic number) and the dielectric constant as determined experimentally in the study. Notice that the permittivity has a linear relationship with atomic number, for which the ionic radius and polarizability are also linearly dependent (polarizability decreases as the number of 4f electrons increases).[180] For the most-part, the dielectric constant of a solid can be predicted by the polarizability of the constituent atoms.[184] The linear interpolation of the dielectric constant to the entire set of lanthanide oxides is shown in **Fig. 2.29**.

Figure 2.30 shows a literature survey of the dielectric constant for lanthanide oxides along with the model of the predicted dielectric constant from literature.[184] The raw data along with references is presented in **Table 2.9**. It is evident that the dielectric constant varies significantly beyond the model prediction and bulk values observed in **Fig. 2.29**. As mentioned previously, the variation is due to variable growth processing, structure, and annealing of the thin films. For combinatorial oxides, such as silicates, the Clausius-Mossotti equation can be used for predicting the dielectric constant,

$$\varepsilon = \left(V_m + 2\alpha_D \frac{4\pi}{3}\right) / \left(V_m - \alpha_D \frac{4\pi}{3}\right) \qquad \text{Equation (2.20)}$$

where V_m is the molar volume and α_D is the total polarizability of the oxide.[184] Just as in the prediction of the oxide permittivity above, the Clausius-Mossotti equation takes into consideration an (oxide) additive rule, which allows for the total polarizability to be predicted by summing the contributions of the individual atoms.[185] An interesting result of the Clausius-Mossotti equation is the fact that the dielectric constant is also a function of molar volume, which can be altered by density of the oxide. It is determined that a decrease in V_m will result in an increase in dielectric constant. This is an important point in dealing with silicate films, due to the fact that the density of the films are not a linear function of the ratios

Table 2.9: *Dielectric constants obtained from literature for the various lanthanide oxides. Data is plotted in **Fig. 2.30** for succinct analysis.*

	model[184]	
La	14.77	22[58], 20[60], 27[133], 12.7[44]
Ce	14.6	52[138], 26[60], 26[186], 21[187]
Pr	14.43	15[72], 30[73], 26[188], 15[188], 21[70], 30[74], 13.2[189], 15.5[187], 25.4[75], 14.5[44], 15.2[190]
Nd	14.27	14.3[185], 11.8[90], 14[144], 15.3[85], 11.7[92], 12.25[90], 14.3[44], 2.9[190]
Pm	14.1	---
Sm	13.93	42.7[93], 43[94], 11.4[190], 23[97], 15.7[190]
Eu	13.77	13.9[185], 20.4[98], 13.7[187], 14[101]
Gd	13.6	13.6[185], 16[102], 11[103], 11.7[99], 12.9[187], 13.9[190], 11.9[44], 15.3[190]
Tb	13.43	13.3[185], 12.9[187]
Dy	13.27	13.1[185], 13.5[109], 18[110], 12.5[187], 14.3[190], 16[190]
Ho	13.1	13.1[185], 12.5[187]
Er	12.93	13[185], 12.5[187], 14[116], 12.1[161], 14.4[117]
Tm	12.77	12.6[185]
Yb	12.6	13.4[185], 12.5[191], 10[121], 14[192]
Lu	12.43	12.5[185], 12.5[187], 12[124]; 11[121]; 11[192]; 19[193]; 12[193]

of M_2O_3 to SiO_2. For example, consider the equilibrium states of the La_2O_3:SiO_2 system. The densities of La_2SiO_5 (5.72 g/cm^3) and $La_2Si_2O_7$ (4.85 g/cm^3) are greater than the linear interpolated density (4.4 and 3.7 g/cm^3), allowing for an approximation of a higher dielectric constant. In essence this allows for an increase in capacitance by mixing of the two species.

2.5 Concluding Remarks and Prospectus

From the analysis of literature the following key observations are made, which also serve as motivation for this research effort:

- Incorporating high-κ dielectrics into silicon-based gates stacks may resolve MOSFET scaling issues associated with gate leakage in the device.

- The choice of a high-κ must simultaneously consider permittivity, band gap energy, and thermodynamic and morphological stability in contact with silicon. Thought band alignment is not perfectly understood, a limiting factor may be the inverse proportionality between permittivity and band gap.

- Experimental observations suggest that lanthanide-based oxides offer suitable stability on silicon and silicate forming capabilities.

In general, lanthanide-based oxides have not been studied in great detail in comparison to Hf-based dielectric counterparts. The extent to which research that has been conducted with the Hf-based oxides, in particular with their growth, has ultimately led to their inclusion (along with the addition of a metal gate) in recent announcements[194,195] for 45 nm gate stack designs by TI, IBM, Intel, and NEC. This represents the first generation in which a high-κ dielectric will be used in the manufacturing of a high-end MOSFET device. It can be observed in the literature that, in using a high-temperature processing route, HfSiON is the most suitable choice of the hafnia-based dielectric. For this dielectric, the nitrogen allows for the increases phase separation resistance of the silicate, therefore preventing crystallization of the HfO_2.[17,196] A major problem of hafnia-based dielectrics is the Fermi level pinning that occurs at the gate electrode/dielectric interface.[197,198,199] The Fermi level pinning mechanism

prevents a suitable metal work function needed to match the band-edges of the silicon, resulting in inaccurate values of threshold voltage. This adds difficulty to an already existing problem with identifying a processing route suitable for making a CMOS (nMOS and pMOS) device that requires two metals with work functions to meet the appropriate band edges of silicon.

In the research presented here, lanthanum-based dielectrics are investigated as La_2O_3 has a slightly higher dielectric constant (27) and band gap energy (5.5 eV) than HfO_2.[200] Most important is that lanthanum silicate may perform better with thermal annealing than hafnium silicate.[38,39] The fact that the silicate is a favored reaction means that unique (and undeveloped) methods of processing optimization can be investigated. Recent developments also suggest that the presence of lanthanum allows for a reduction in the Fermi level pinning effect. In this work, lanthanide-based dielectrics were at first examined as a suitable replacement for SiO_2, but can now also be considered as a replacement or modification for hafnia-based dielectrics in both the current and future technology nodes.

3. EXPERIMENTAL

3.1 Thin Film Processing

A general outline for the MOS capacitor formation and anneal processing is shown in **Fig. 3.1**. The processing follows that of the gate stack production in standard MOSFET production. This section describes those processes involved in creating the MOS capacitor and the subsequent annealing of the device.

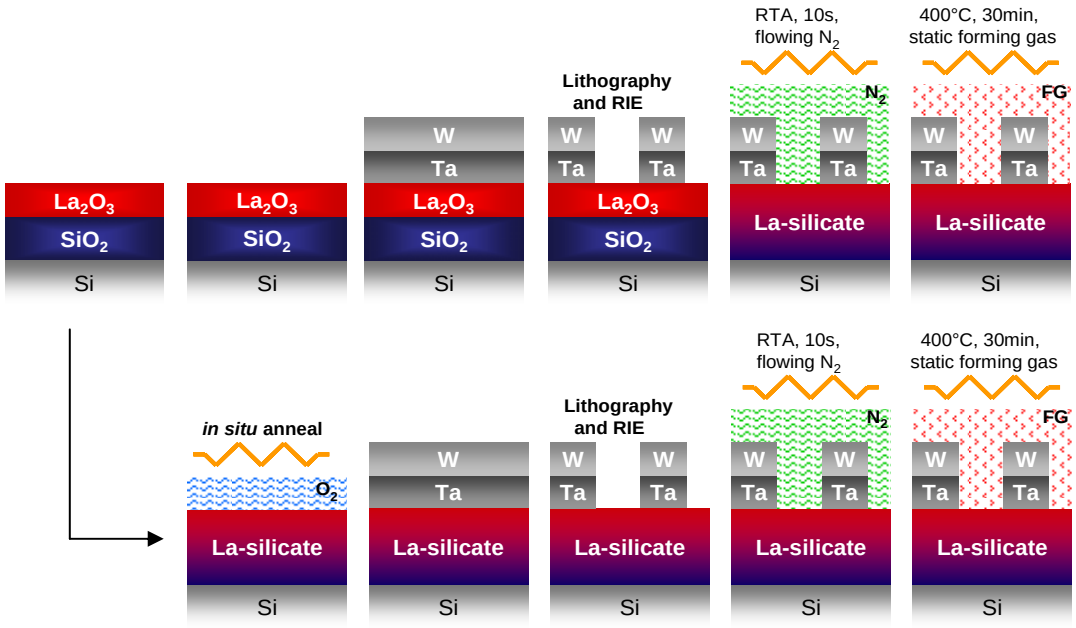


Figure 3.1: *General outlines for MOS capacitor formation and anneal processing. The process deviates by performing an in situ anneal on select samples.*

3.1.1 Oxide Growth

RCA Chemical Oxide

The silicon substrates (n-type (Sb-doped, 0.02 Ω cm) and p-type (B-doped, 0.05 Ω cm) Si(001)) were first treated by a standard RCA (Radio Corporation of America) clean process,

yielding an 8-10 Å layer of SiO_2. The RCA-cleaned process consists of a SC1 sequence (5 minute soak in $5H_2O$:$1NH_4OH$:$1H_2O_2$ at 75 °C; 5 second dip in buffed oxide etchant) to first remove the native oxide and residue on the silicon substrate followed by an SC2 sequence (5 minute soak in $5H_2O$:1HCl:$1H_2O_2$ at 75°C) to form a uniform silica chemical oxide layer. The RCA process was conducted in the clean room facility at the North Carolina State University Nanofabrication Facility (NNF).

Lanthanum Oxide

Lanthana-based gate dielectrics are deposited using reactive evaporation in an ultrahigh vacuum (UHV) molecular beam epitaxy (MBE) system. The effort to design the system was led by Robert Wallace,[201] while at Texas Instruments, and was contracted to be built by SVT Associates, Inc. MBE system, shown in **Figs. 3.2 (a)** and **(b)**, is designed for processing 8 inch (200 mm) diameter substrates and consists of three main chambers: loadlock, cluster, and growth. A mechanical transfer system allows movement of the wafers between

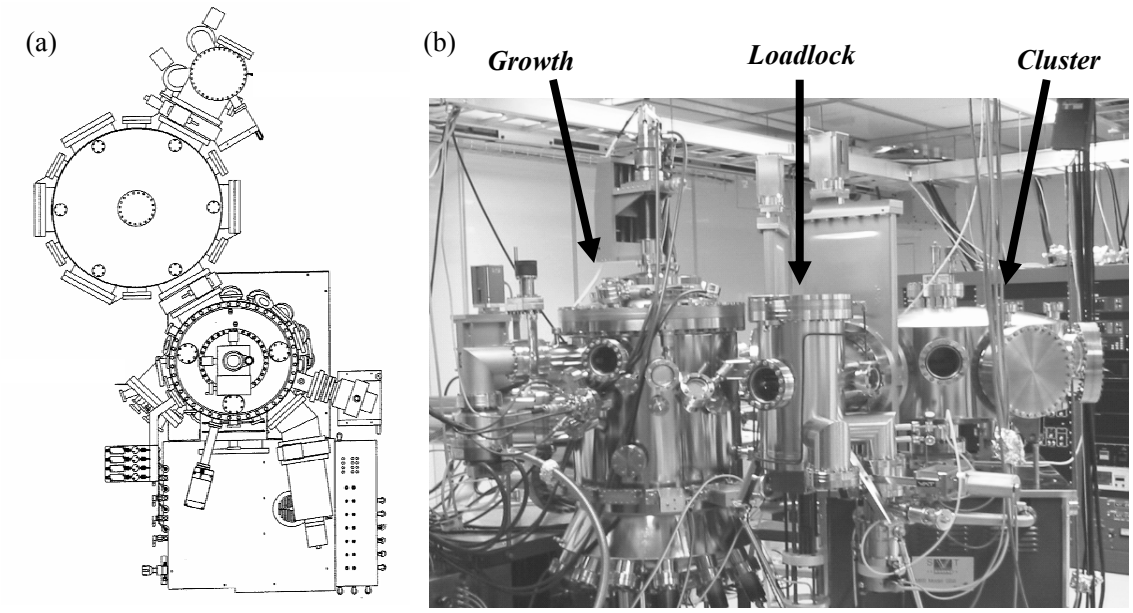


Figure 3.2: (a) *Schematic and* (b) *photograph of molecular beam deposition system used for lanthanum oxide growth, in situ annealing, and Ta electrode deposition.*

chambers, which are divided by 12" gate valves. The background pressure of the system is $< 1 \times 10^{-9}$ Torr and is maintained by using a turbomolecular pump, a cryogenic pump, and a titanium sublimation pump. Evaporation techniques available in the growth chamber includes an 8-well E-beam evaporation source used for metal deposition, a single silicon E-beam evaporation source, and six ports available for effusion cell sources. A rotating substrate manipulator/holder, capable of substrate heating to 950 °C is situated at the center of the system. Growth of metals and metal oxides thickness was measured by a quartz crystal rate monitor.

Extensive investigation as to La_2O_3 growth had previously been performed by Maria et al. [38,39,171] A brief description of the procedure as employed by this investigation is as follows: Lanthanum is evaporated using a high-temperature effusion cell at a temperature of 1700 °C. During growth, the deposition pressure is maintained at 5×10^{-7} to 1×10^{-6} Torr by controlled high-purity oxygen flow using a mass flow controller. The substrate manipulator is typically maintained at 200 °C (although some experiments required variable deposition temperatures). A growth rate of ~ 0.05 Å/s was maintained at these conditions and monitored by quartz crystal rate monitoring (Density (La_2O_3): 6.51 g/cm^3; Z-factor: 1.00, and Tooling Factor: 220 %).

An *in situ* annealing process was conducted on selected samples to allow for the reaction between the lanthanum oxide and silica chemical oxide. This anneal was performed immediately after the lanthanum oxide growth by heating the substrate manipulator at a ramp rate of 20 °C/min (from 200 °C) to a temperature of 500 °C. At times, the manipulator temperature was altered during the *in situ* anneal. It is noted that the ramp time to the set-point temperature was typically slower than the prescribed ramp rate. In addition, the PID controller created a temperature overshoot of ~25 °C. The dwell time at a temperature greater than the set-point was 20 min before it was allowed to cool. The chamber pressure was held at the growth pressure (5×10^{-7} to 1×10^{-6} Torr) and was turned off when the manipulator temperature cooled to < 300 °C. At this time, the chamber pressure was $< 1 \times 10^{-8}$ Torr. The sample was removed when the temperature was < 180 °C.

3.1.2 Metallization

Electrode

In the experiments, both Ta and TaN electrodes were used for electrode metals in the MOS gate stack. Ta was E-beam evaporated *in situ* after the lanthanum oxide deposition or after the *in situ* anneal. Ta was deposited at electron beam conditions of 8 kV and 0.3 Amps and a chamber pressure < 1 x 10^{-8} Torr. A growth rate of ~5 Å/s was maintained at these conditions and monitored by a quartz crystal rate monitoring (Density (Ta): 16.6 g/cm^3; Z-factor: 0.26, and Tooling Factor: 45%).

TaN was deposited *ex situ* by using a DC magnetron sputtering system that was specially designed and built, by the author, for this project. **Figures 3.3 (a)** and **(b)** shows the general schematic and also a photograph of the sputtering system. The deposition system consists of two-chambers, one allowing for sample loading and the other for TaN deposition. The background pressure of the system is in the mid-10^{-9} Torr range after low temperature bakeout. The leak rate of the system is unable to be checked due to the fact that there is no gate valve between the turbo molecular pump and the chamber. However, a residual gas analyzer (RGA) connected to the system does allow for monitoring of H_2O, O_2 and N_2 that would be an indication of air leakage into the system. The gas delivery lines were exhaustively leak checked to ensure a background pressure of 10^{-7} Torr (chamber) when the gas delivery MFCs were 100 % open. A hydrocarbon trap was placed in the roughing line to reduce hydrocarbon back draft to the chamber (hydrocarbons were also monitored by the RGA). Samples were transfer to the deposition system using a magnetic transfer arm with an attached lock-and-key mechanism.

An AJ Vacuum DC magnetron sputtering gun was used for sputtering a 1.5" 99.99% Ta target in an Ar/N_2 atmosphere for TaN deposition. The ultra high purity (UHP) Ar and N_2 flow was controlled by MFCs (10 sccm max) and the chamber pressure was controlled by a butterfly valve (located in between sputter chamber and the turbo molecular pump) that

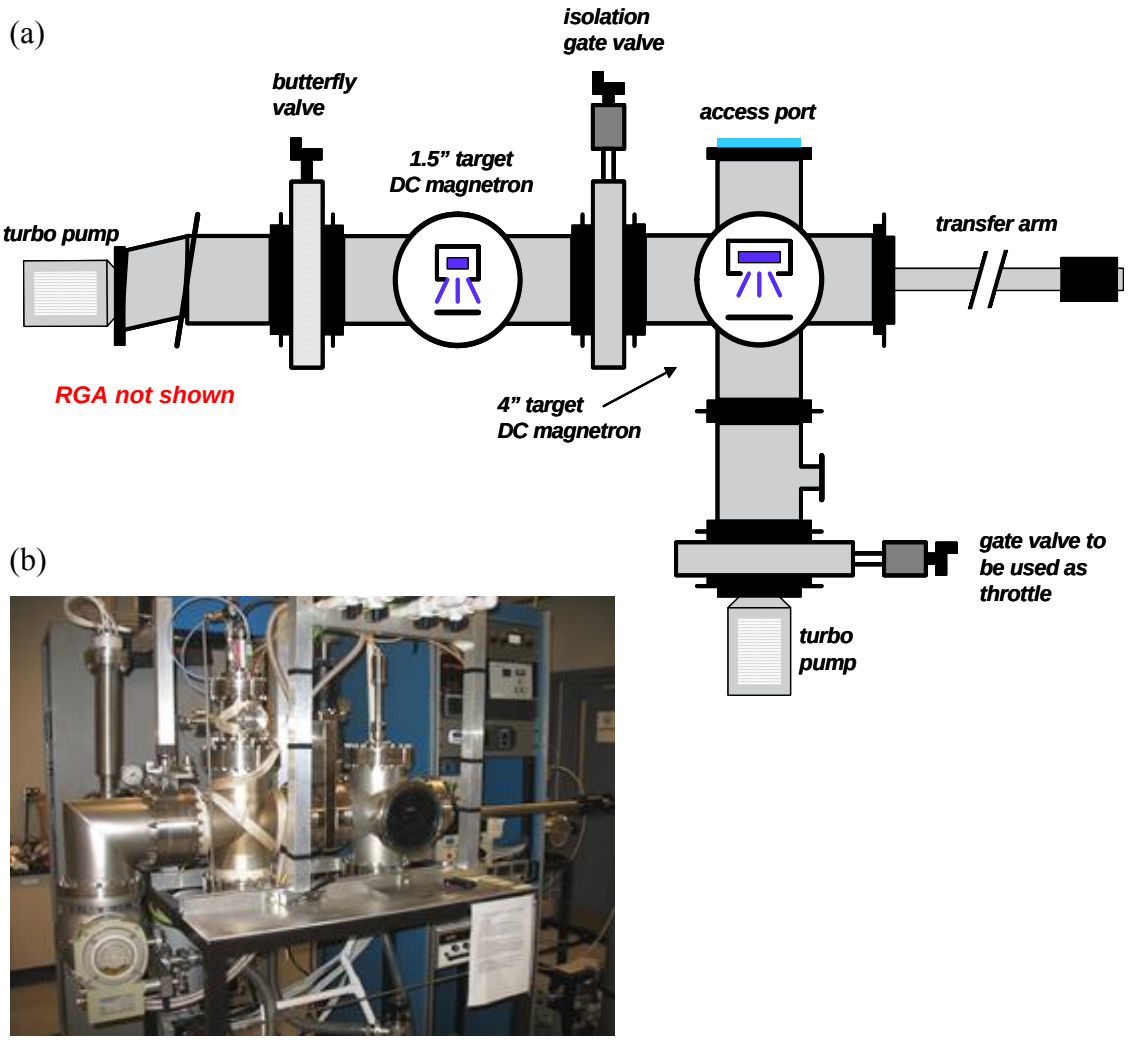


Figure 3.3: (a) *Schematic and* (b) *photograph of DC magnetron sputtering system used for TaN electrode deposition and W contact metal deposition.*

allowed for a maximum system pressure of ~5.0 mTorr. The deposition pressure was monitored by a convectron pressure gauge calibrated for atmosphere (760 Torr) and vacuum (0.0 at Pressure < 1 x10^{-4} Torr). Prior to TaN deposition, the Ta target was pre-sputtered (sample protected by rotate-able shutter) for 1 min to remove residual TaN formation at the target surface. More detailed TaN growth conditions, including x-ray diffraction characterization, to determine optimum deposition conditions for producing thermally stable cubic-TaN is described in **§5.4**.

Contact

In this work, tungsten (W) is used for a metal contact in that it offers a lower electrical resistivity (compared to the metal electrode) for subsequent device testing. W was deposited using the loading chamber of the sputtering system shown in **Fig. 3**. DC magnetron sputtering of a 50 cm (4") 99.95% pure W (200-250 W for 15 sec) resulted in 500-750 Å thick films (as determined by Dektak profilometry. Prior to deposition, the W target was pre-sputtered for 3 minutes to remove residual oxygen that was absorbed on the surface of the W as result of opening the system to atmosphere to retrieve/load the samples. The samples were also coated on the backside of the silicon substrate, again to reduce contact resistance.

Note that by using the loading chamber of the TaN deposition system for W deposition, the samples were not exposed to atmosphere in-between the electrode and W metal growth procedures. The setup also allowed for shadow-mask electrode deposition. These two benefits are contrary to the Ta processing procedure described previously in that the sample was exposed to atmosphere prior to DC sputtering of W and shadow masking is not a possibility using the MBE tool, requiring MOS devices to be formed by lithography and etch procedures. The benefit of the shadow mask MOS capacitor devices is a lower cost (NNF cleanroom charges for photolithography and etch), a quick processing turnaround, and an ability to avoid over-etching that can cause an unwanted leakage increase. However, MOS devices defined by photolithography and etch are uniform and of precise thickness. Shadow-masked devices need to be measured using optical microscopy to verify the dimensions of device.

3.1.3 Photolithography and Etch

The photolithography and reactive ion etch tools in the NNF Class 100 cleanroom at North Carolina State University were used in this work to produce MOS capacitor devices. The photolithography process includes a spin-on of the photoresist, photoresist annealing for hardening, masked exposure to UV light, and finally the removal of the exposed photoresist. At this point the photoresist protects the area that defines the MOS capacitors. A thickness

of ~1200 nm Shipley 1813, a positive photoresist, was applied to the samples by a chemical spin-on method at a spin rate of 4000 rpm for a time of 40 seconds. A 'soft bake' (90 °C, 1 min) of the photoresist allowed for removal of the photoresist solvent and prepared the sample for contact mask exposure. The exposure unit, a Karl Suss MA-6 mask aligner, uses a 350 W Mg lamp that is capable of exposing the photoresist at a wavelength of 250 nm in an exposure time of 12 seconds. To prevent exposure to particular areas, a mask designed to create 50 μm x 50 μm to 200 μm x 200 μm capacitor designs was in direct contact with the sample. To remove the exposed photoresist, the samples were soaked in a photoresist development bath. A 'hard-bake' of the photoresist was then conducted to prepare the samples for the etch procedure.

A Semigroup 1000TP reactive ion etch (RIE) system was used to remove the W contact metal and the Ta/TaN gate electrode metal in areas in-between the unexposed photoresist that protects that capacitor dimensions. It was important to create an etch recipe (gas composition, etch time) that effectively removed the metals, but not completely etch the photoresist. In this work, a gas composition of 6/1:SF_6:O_2 throttled to a pressure of 40 mTorr was used with a cathode voltage of 200 V to attain etch rate of 250 Å/min for Ta and 500 Å/min for W. Etch rates were determined systematically using Dektak profilometry. After RIE, the residual photoresist was removed by an acetone wash to allow for the uncovering of the MOS capacitor devices. An image of the final MOS capacitor structure on the silicon substrate is shown in **Fig. 3.4**.

3.1.4 Annealing

An AG Associates Heat-Pulse 210 was used to anneal the samples at temperatures of 400-1000 °C for dwell times of 1 to 60 seconds. The temperature was monitored using a thermocouple attached to a silicon substrate that was capable of withstanding high temperatures. A ramp rate of 95 °C/s was possible from room temperature to 400 °C, followed by a 10 second dwell before ramping to 1000 °C. The anneal chamber was able to be sealed to allow for a flow of gas during the anneal. Flowing gases available included a nitrogen gas (from supplied house gas line), forming gas (5% H_2 in N_2), and argon (UHP).

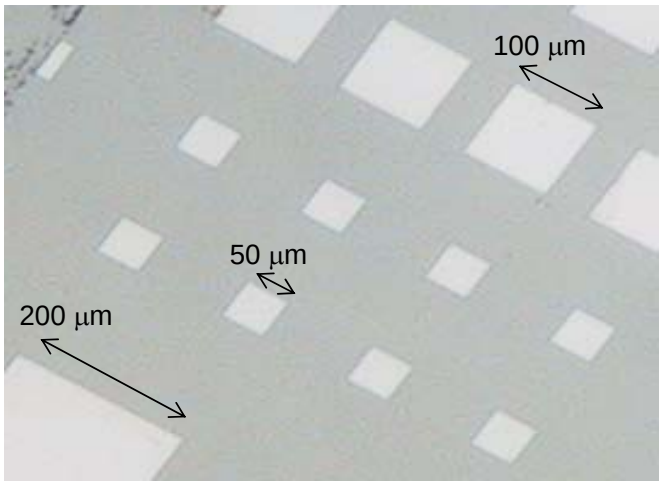


Figure 3.4: *Capacitor structures on silicon substrate after photolithography and reactive ion etch.*

A stable cool rate was not possible in the system, but the cool down was typically < 30 sec to achieve temperatures < 250 °C. The samples were removed once the temperature decreased below 200 °C.

For some samples, a forming gas anneal was used in an attempt to passivate defects in the oxide and at the oxide/semiconductor interface. The forming gas anneal (1-5% H_2 in N_2) was typically 400-450 °C for 30 min and was performed in a horizontal tube furnace with closed ends, so as to allow for gas flow during the anneal. The samples were moved into the hot zone of the tube furnace after a sufficient time to allow the environment of the anneal chamber to be flushed with the forming gas (~5 min). After an anneal time of 30 min, the samples were removed to a cool end of the furnace and allowed to cool (< 100 °C) before purging the system with N_2 (or Ar) and removal from the furnace.

3.2 MOS Electrical Characterization

3.2.1 Capacitance-Voltage

Electrical testing of capacitance and conductance with respect to the voltage applied to the gate electrode (C-V and G-V, respectively) was performed using an HP 4192A impedance

analyzer probe station. A first probe was placed in contact with the top layer of the capacitor and a second was placed in contact with a Pt-coated substrate upon which the silicon substrate was placed. From the measurement, equivalent oxide thickness (EOT) and effective fixed charge (Q_{eff}) and flat-band voltage (V_{FB}) were obtained from modeling the C-V curves with the NCSU Hauser modeling program.[202] In most cases high-κ dielectric films have a high density of interface states (D_{IT}) that results in an inflection in the C-V curve. Unfortunately, the Hauser model is unable to model such an inflection. To use the Hauser model effectively, the data must be carefully modified to remove the inflection and still keep the overall trend of the C-V curve. **Figures 3.5 (a)-(c)** shows the procedure for analyzing a

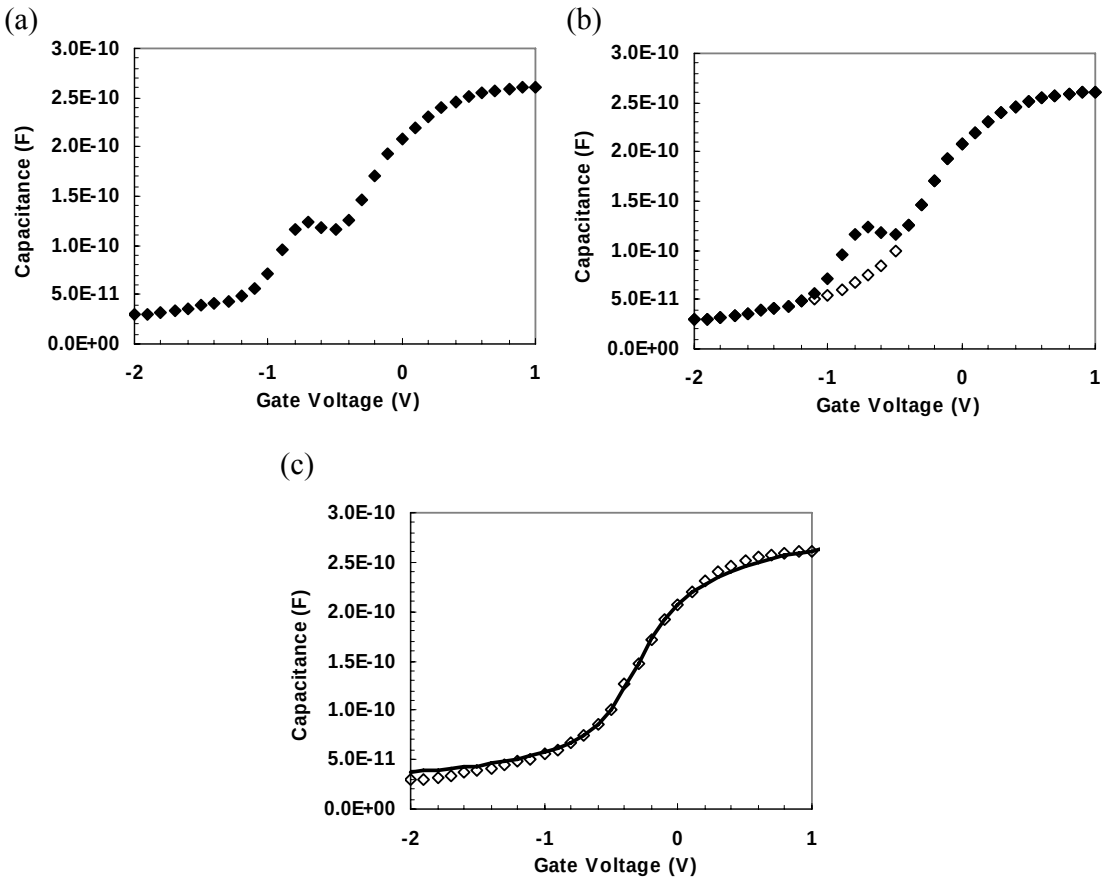


Figure 3.5: *(a) An example C-V curve with D_{IT} inflection in the transient region of the C-V curve, (b) modification of C-V curve to remove the inflection, and (c) subsequent modeling with NCSU Hauser model.*

C-V curve with a D_{IT} inflection (**Fig. 3.5 (a)**), subsequent removal (**Fig. 3.5 (b)**), and fitting with the NCSU Hauser model (**Fig. 3.5 (c)**). Note that the NCSU Hauser model only provides information on the effective fixed charge, Q_{eff}, and not the D_{IT},

$$Q_{eff}\left(\frac{e^-}{cm^2}\right) = \frac{\left(V_{FB,ideal} - V_{FB}\right)}{EOT}\frac{\varepsilon_o \kappa_{SiO_2}}{q} \qquad \text{Equation (3.1)}$$

with $V_{FB,ideal}$ being the ideal flat-band based on the doping concentration in the semiconductor and the work function of the metal. Electrical results were obtained from either 50µm x 50µm to 200µm x 200µm square capacitor areas, and measured from 10 kHz to 5 MHz using a 0.1 V measurement step size. For shadow masked capacitors structures, the capacitor area was ~0.00035 cm^2 and was confirmed using optical microscopy.

3.2.2 Current-Voltage

In a similar way to the C-V measurement, the leakage current was measured with respect to applied voltage (J-V) using an HP 4145A semiconductor parameter analyzer probe station. Again a two probe system, the electrical data was obtained by increasing (or decreasing) the voltage from 0.0 V. The leakage current density of the device was measured by the flat-band voltage (obtained from modeling of the C-V curve) offset +/- 1 V, depending on substrate type (n-type or p-type). This step was taken to ensure that the leakage was known with respect to the accumulation state of the MOS device.

3.2.3 Density of Interface States

The density of interface states, D_{IT}, can be determined from an MOS capacitor by the use of the AC conductance method.[10,19] The method involves measuring the complex admittance of an MOS device as a function of frequency at a number of different voltages. Using this method, the semiconductor conductance was able to be calculated using an AC equivalent circuit by,

$$G_S = \frac{G_m}{\left(\frac{G_m}{\omega C_{OX}}\right)^2 + \left(1 - \frac{C_m}{C_{OX}}\right)^2}$$ Equation (3.2)

with C_{OX} being the oxide capacitance (also accumulation capacitance), ω being the angular frequency, C_M being the measured capacitance as function of frequency, and G_M being the measured conductance as a function of frequency. An example of the conductance data plotted as a function of log (ω) is shown in **Fig. 3.6**. D_{IT} was calculated from the magnitude of the peak of the G_s/ω curves at a given bias from,

$$D_{IT} = \frac{C_S}{qA} cm^{-2} eV^{-1}$$ Equation (3.3)

where A is the area of the measured device and C_s is the semiconductor capacitance determined by,

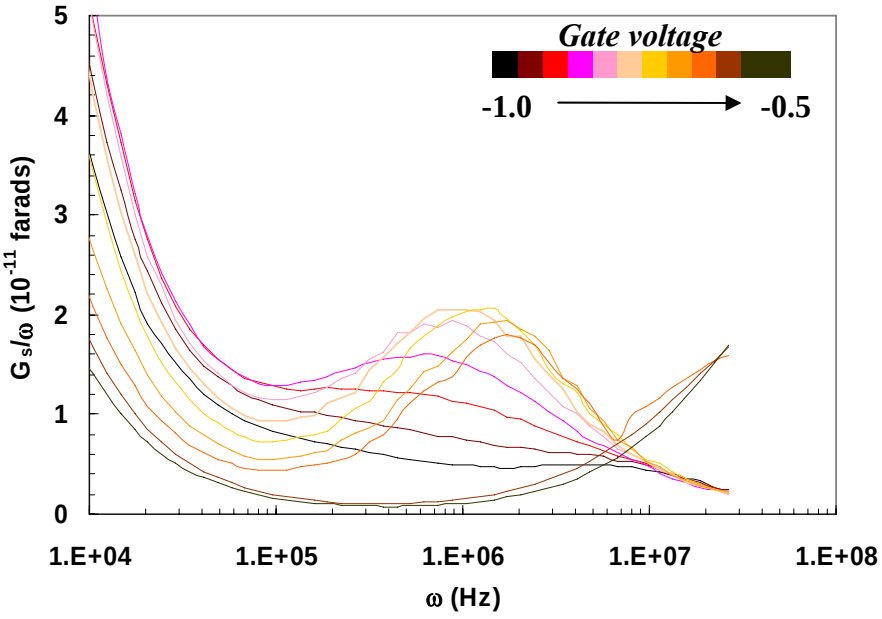


Figure 3.6: *An example G_S/ω plot vs. ω following the AC conductance method.*

$$C_S = 2\frac{G_S}{\omega}$$ Equation (3.4)

In addition, at a given bias, the angular frequency of the peak reports the interface trap's time constant and the width is an indication as to the of the change in surface potential across the capacitor. Additional presentation of the D_{IT} measurement pertaining to the MOS devices examined in this work is provided in §5.7.

3.3 Analytical characterization

3.3.1 X-ray Diffraction

X-ray diffraction was conducted with a Bruker AXS D-5000 diffractometer equipped with a Hi-Star area detector, operated with Cu-Kα radiation (30 kV, 20 mA). Theta-two theta (θ-2θ) scans were performed with 0.01 degree step sizes with chi, phi = 180 degrees.

3.3.2 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) was conducted on the oxide films without a metal electrode. Characterization was performed using a Riber LAS3000 XPS system equipped with a two stage cylindrical mirror-style analyzer (MAC2). Spectra was acquired with a Mg Kα (1253.6 eV) non-monochromatic x-ray source, a take-off angle of 75° from surface, and a 0.1 eV step size. The C-1s binding energy (285.0 eV) was used as the offset reference. The chemical bonding states of the O-1s were evaluated using a CASA XPS peak fitting program.

3.3.3 Transmission Electron Microscopy

Transmission electron microscopy (TEM) was performed at the University of California at Santa Barbara (Prof. Susanne Stemmer) and at North Carolina State University (Prof. Gerd Duscher).

Cross-sectional transmission electron microscopy (TEM) samples were prepared by standard sample preparation techniques, with ion milling using 3.3-kV Ar ions as the final step. High-resolution TEM (HRTEM) was performed using a field-emission TEM (Tecnai F30 U-TWIN, Cs=0.52 mm) operated at 300 kV. HAADF imaging and EELS in STEM were performed using a field-emission TEM (Tecnai F20 S-TWIN) equipped with a Gatan imaging filter (GIF) and operated at 200 kV. EELS spectra were obtained using a 2-mm GIF entrance aperture and a 0.5-eV/ch dispersion to include both O *K*-edge (at 532 eV) and La-$M_{4,5}$ edges (at 849 and 832 eV, respectively). The probe size for EELS was estimated to be 3.5 Å based on the resolution in the HAADF images. The energy resolution was 1.5–1.7 eV (full width at half maximum of the zero-loss peak). Each spectrum was acquired for 15 s to obtain a sufficient signal-to-noise ratio, and specimen drift was about 5 Å during this time, further reducing the spatial resolution. After appropriate background subtraction, chemical profiles were generated from spectral counts by integration over suitable energy ranges. Such profiles showed qualitative changes in the concentration of a given element along the profiled line and did not represent true relative elemental concentrations. The preceding details the analysis procedure for those samples analyzed at the University of California at Santa Barbara. A similar analysis was conducted by North Carolina State University.

3.3.4 Medium Energy Ion Scattering

Medium energy ion spectroscopy (MEIS) was performed at Rutgers University by Prof. Garfunkel and Dr. Gustaffson. The MEIS experiments were performed using 130.8-keV H+ beams using a double alignment geometry in the (110) scattering plane. The incoming beam was aligned with the Si (100) channeling direction and the detector axis was aligned with the ($1\bar{1}1$) crystallographic axis. The scattering geometry chosen was ideal for reducing the background backscatter signal from bulk silicon and for allowing a detailed study of the weak O signal. The backscattered ion energies were analyzed with a high-energy-resolution toroidal electrostatic ion detector ($\Delta E/E$~0.1%).[203,204] Simulations of the backscattered ion energy distribution provided depth profiles and thicknesses of the analyzed film. A key assumption is that the film densities are known or can be approximated from films of known

composition. At the surface of films, MEIS provides a depth resolution of 3 Å and the resolution decreases with depth due to the statistical nature of the ion-solid interaction. In order to get detailed information about the dielectric, a metal electrode was not deposited. Therefore, the films may have been subject to hydroxide formation (especially for lanthanum oxide) and possibly high SiO_2 growth during high-temperature anneal (if oxygen was present in the anneal environment).

3.3.5 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) was performed by the Analytical Instrumentation Facility (AIF) at North Carolina State University. Both front-side (metal to semiconductor) and back-side (semiconductor to metal) depth profiles were measured with a CAMECA IMS-6f magnetic sector SIMS using a 10nA Cs^+ ion bombardment over a 180 x 180 μm^2 area. This provided detection of the positive secondary ions from a 60 μm diameter optically gated region at the center of the raster. A 5 kV primary accelerating potential and a -1 kV secondary potential was used for an impact energy of 6 kV. The angle of incidence was 27 degrees with respect to substrate normal.

For back-side SIMS, sample preparation involved the mechanical polishing of the Si substrate to 200-300 nm beneath the lanthanum silicate interface with the silicon.[205] A requirement for sample preparation is that the top capping layer must adhere well to the epoxy used to mount the sample during polishing. In this study, the tungsten capping layer provided sufficiently strong adhesion.

4. LANTHANUM OXIDE-BASED MOS DEVICES: LOW-TEMPERATURE PROCESSING

4.1 Introduction

In order to scale down the dimension of a metal-oxide-semiconductor field effect transistor (MOSFET), the use of an alternative gate dielectric with a higher dielectric constant is necessary, because leakage currents through sub-1 nm SiO_2 films are undesirably high. To investigate the limits of scaling, a low-temperature process study of lanthanum silicate, a potential replacement for SiO(N), is investigated. The intrinsic electrical properties required for alternative high-κ materials include a high dielectric constant, high band gap energy, and ideal band offsets when in contact with silicon. Other important materials issues are the ability to keep interface SiO_2 growth to a minimum, and to maintain a stable amorphous phase after high-temperature processing. In order to circumvent the high-temperature process, routes have been defined that lower the thermal budget significantly. The thermal budgets defined in this work are of the same order of magnitude of the low-temperature processing routes.

As explained in **§2.3-2.4**, the formation of a silicate can be beneficial in reducing the expected interfacial SiO_2 that is created during processing, keeping the pristine interface quality that is unique to the Si/SiO_2 interface, and preventing the crystallization of the gate dielectric with high-temperature annealing. In this way, the silicate can be thought to be the natural progression from using pure SiO_2 to a purely high-κ gate dielectric.

La_2O_3 is a candidate to replace SiO_2 due to its high dielectric constant ($\kappa \sim 27$) and band gap energy (5.5 eV) and conduction band offset (~ 2.3 eV). A lanthanum silicate dielectric has a lower dielectric constant than La_2O_3 due to the SiO_2 incorporation, but is predicted to have higher temperature stability in the amorphous phase compared to other high-κ silicates. As observed in the La_2O_3:SiO_2 phase diagram (**Fig. 2.19**), a composition region consisting of La_2SiO_5 and $La_2Si_2O_7$ is observed. For tetravalent high-κ dielectrics, such as HfO_2 and ZrO_2, a single equilibrium state exists as $MSiO_4$. However, a liquid-liquid immiscibility region, as

observed in their phase diagram (see **Figs. 2.17, 2.18**), prevents stability of such a phase after high-temperature annealing. This lack of stability results in phase segregation and the possible crystallization of the high-κ regions of the dielectric. Efforts have been made to incorporate nitrogen into the system to prevent crystallization. For lanthanum oxides (and most of the other lanthanides) this liquid-liquid immiscibility region is far removed from the equilibrium states, thereby allowing the silicate form to remain undisturbed after high-temperature annealing.

The purpose of this chapter is to examine alternate routes to achieve such a lanthanum silicate formation with the goal of obtaining the lowest possible equivalent oxide thickness (EOT) and leakage current density (J) for metal-oxide-semiconductor (MOS) devices. These properties for MOS devices relate to the ability to obtain scaled MOSFET devices with a higher operating current and a lower standby state current.

It has been observed for annealing of most high-κ dielectrics, high-temperature annealing results in growth of SiO_2 at the silicon interface. Therefore, a low-temperature processing route to form lanthanum silicate is described in this chapter as a means for obtaining the desired device qualities. It is believed that once the optimum device quality is achieved after low-temperature annealing, similar device properties can be obtained after high-temperature annealing that is required for source-drain activation anneal in standard MOSFET processing. Further, the low-temperature processing investigated is consistent with proposed thermal budgets for 'reverse-gate' processing.

4.2 Process Definition

4.2.1 Thickness Optimization for Silicate Formation

Prior to defining the experimental plan, it is useful to predict the outcome of alloying lanthanum oxide and SiO_2. In doing so, the optimum thickness required to produce a lanthanum silicate with compositions between the equilibrium concentrations of La_2SiO_5 and $La_2Si_2O_7$ observed in the phase diagram of the La_2O_3:SiO_2 system can be predicted. Note

that if the thin film is deficient in SiO_2, a pure lanthanum oxide and La_2SiO_5 will be produced. If the film is deficient in La_2O_3, the dielectric will rich in SiO_2, resulting in a decrease in the optimum dielectric constant. This simple study will also serve to predict the lowest achievable EOT possible provided the reaction between differing lanthanum oxide thicknesses and the SiO_2 thicknesses is achieved by growth of a chemical oxide (8-10 Å) silica layer on the silicon substrate (process defined in **§3.1**). Note that the following study is based on the assumption that there is a complete reaction between La_2O_3 and SiO_2.

The objective is to deposit a thin lanthanum oxide film on SiO_2. Assuming reaction between the films with a product of the form $(La_2O_3)_{1-x}(SiO_2)_x$, the mole fraction of SiO_2, χ_{SiO2}, can be calculated as,

$$\chi_{SiO_2} = \frac{N_{SiO_2}}{N_{La_2O_3} + N_{SiO_2}} \qquad \text{Equation (4.1)}$$

In the calculation N_{SiO2} and N_{La2O3}, the densities of the films are defined as ρ_{La2O3} = 6.51 g/cm^3 and ρ_{SiO2} = 2.23 g/cm^3.

From this expression (**Eqn. 4.1**) the proposed dielectric constant can be estimated as,

$$\kappa_{(La_2O_3)_{1-x}(SiO_2)_x} = \chi_{SiO_2}\kappa_{SiO_2} + \left(1 - \chi_{La_2O_3}\right)\kappa_{La_2O_3} \qquad \text{Equation (4.2)}$$

with the κ_{SiO2} = 3.9 and κ_{La2O3} = 27.

The EOT of the silicate can be subsequently predicted by,

$$EOT = t_{(La_2O_3)_{1-x}(SiO_2)_x}\frac{\kappa_{SiO_2}}{\kappa_{(La_2O_3)_{1-x}(SiO_2)_x}} \qquad \text{Equation (4.3)}$$

where $t_{(La2O3)1-x(SiO2)x}$ is the thickness of the silicate product, which is dependent on the known densities of La_2O_3, La_2SiO_5, $La_2Si_2O_7$, and SiO_2. **Figure 4.1** shows the experimental values

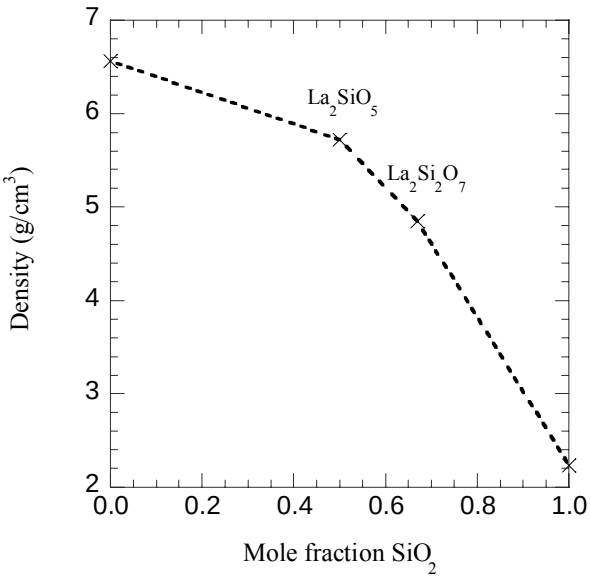


Figure 4.1: *Density of silicate alloys considering the known density values for La_2SiO_5 and $La_2Si_2O_7$. The density approximation for the calculations in §4.2.1 are a linear interpolation of the three observed regions.*

for the density of each compound as a function of SiO_2 content. The densities provided are based on crystalline densities; amorphous densities will most likely be different. Note that a linear interpolation between La_2O_3 and SiO_2 underestimates the known densities of La_2SiO_5 ($\rho_{La2SiO5}$ = 5.72 g/cm^3) and $La_2Si_2O_7$ ($\rho_{La2Si2O7}$ = 4.85 g/cm^3). Also note that the higher densities of lanthanum silicate compositions allow for a decrease in EOT with mixing. To estimate densities in the regions between the known densities, a linear interpolation is used based on mole fractions between the compositions of known density (that is SiO_2-La_2SiO_5, La_2SiO_5-$La_2Si_2O_7$, $La_2Si_2O_7$-SiO_2). To vary the mole fraction of SiO_2 in the film stack, the thickness of the La_2O_3 film is varied. **Figure 4.2** shows that the lanthanum oxide thickness is plotted as a function of the mole fraction of SiO_2. Data sets are obtained for varying SiO_2 thickness. Observe that the mole fraction of SiO_2 goes to unity as the thickness of La_2O_3 decreases. In the same way, the mole fraction of SiO_2 decreases substantially as the thickness of La_2O_3 is decreased. Recall that the thickness of the SiO_2 layer on Si (RCA chemical oxide) is predicted to be 8-10 Å. Therefore, a La_2O_3 thickness between 8 and 20 Å is required to ensure that the resultant silicate product is within the ideal compositions of

lanthanum silicate (La_2SiO_5 and $La_2Si_2O_7$). Additional SiO_2 growth might be expected upon annealing (oxygen in an annealing atmosphere reacting with the silicon substrate), thereby increasing the amount of La_2O_3 required to form the desired compositions. For an increase of 5 Å, the required La_2O_3 thickness range increases to 28 Å. A safe range for ensuring the correct reaction product can be predicted to be 10-15 Å La_2O_3.

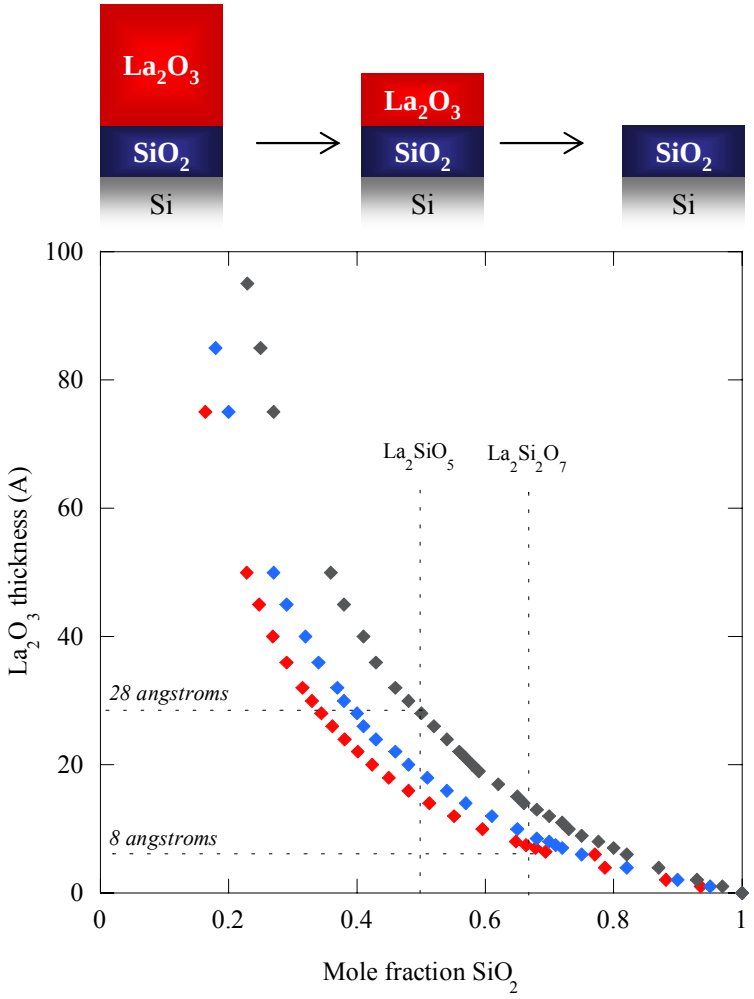


Figure 4.2: *Plot of the La_2O_3 thickness as a function of mole fraction of SiO_2. The mole fraction is varied by increasing the thickness of La_2O_3. Results of calculations for varying SiO_2 thicknesses are shown.*

Figure 4.3 shows the predicted EOT of the alloyed films. Note that the EOT value for χ_{SiO2} = 1 is equivalent to the SiO_2 film thickness (as the La_2O_3 film thickness is zero). A minimum in the calculated EOT values is observed to lie in required lanthanum silicate compositions. It is shown that an optimized EOT value as low as 4.6 Å can be achieved for a SiO_2 thickness of 8 Å, given an appropriate thickness of La_2O_3 (between 8 and 10 Å). For slightly thicker SiO_2 film of 15 Å, the lowest obtainable EOT is ~8.5 Å, corresponding to a La_2O_3 of ~14-18 Å. By forming a silicate alloy with the desired compositions, the effective dielectric constant of the entire dielectric can be varied between 10 and 17.

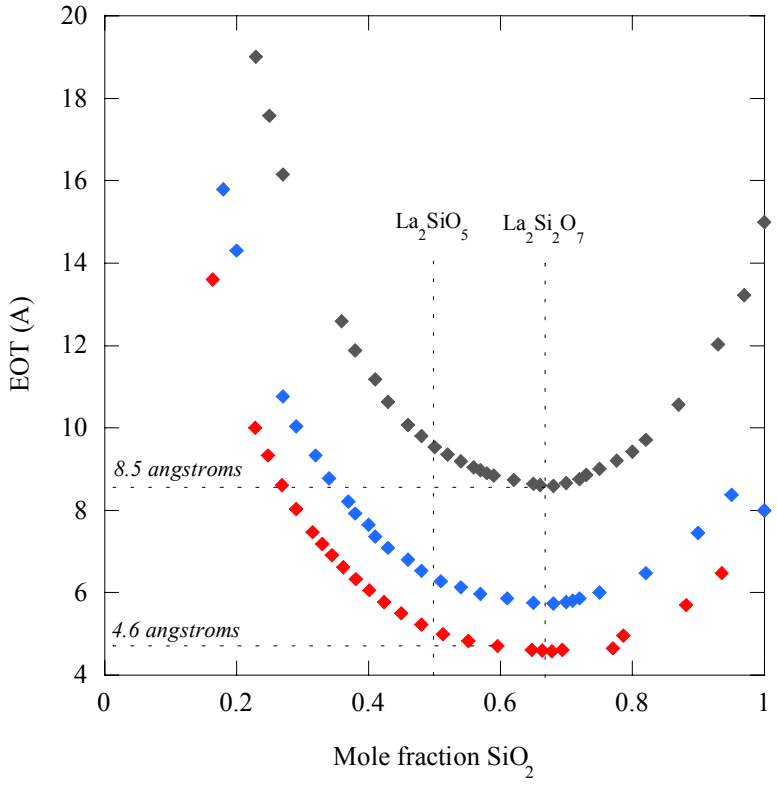


Figure 4.3: *Plot of EOT as a function of mole fraction of SiO_2. The mole fraction is varied by increasing the thickness of La_2O_3. Results of calculations for varying SiO_2 thicknesses are shown.*

4.2.2 Experimental

The basic study in §4.2 serves to define the appropriate La_2O_3 thickness required to achieve the lowest possible EOT of MOS devices. Deleterious effects are observed with a decrease in either species outside of the required compositions predicted by the La_2O_3:SiO_2 phase diagram. The gate stack design that was used is shown in **Fig. 4.4**.

*For a more detailed explanation of each of the individual processing steps, the reader is referred to **Chapter 3**. A summary of the experimental plan is as follows:*

In this work, an n-type (Sb-doped, 0.2 Ω cm) Si(001) was first prepped by performing an RCA clean process, yielding 8-10 Å layer of SiO_2. Lanthanum oxide was deposited by thermal evaporation at a pO_2 of $1x10^{-6}$ Torr and substrate temperature of 100 °C. The deposition rate of the La_2O_3 of approximately 0.05 Å/s was used to achieve a final thickness of 10-15 Å, as monitored by a quartz crystal rate monitor. For some samples, an *in situ* anneal was performed at temperatures between 500-600 °C for 30 minutes at a pO_2 of $5x10^{-7}$ Torr. For lanthanum oxide, the gate electrode must be deposited *in situ* because of the sensitivity of lanthanum oxide to moisture, causing subsequent positive charge.[206] Tantalum is deposited *in situ* via E-beam evaporation at a pressure $4x10^{-8}$ Torr to protect the dielectric from the formation of $La(OH)_3$ after exposure to atmosphere. The choice of Ta as the top electrode is also ideal due to its having a work function near the midgap energy of silicon. For a metal contact layer, 50 nm of W was deposited *ex situ* using a DC magnetron sputtering system. Capacitor devices were masked using standard photolithography techniques and followed by a reactive ion etch (RIE). Some of the samples were subjected to post-metallization annealing (PMA, or RTA) conducted at temperatures of 400 °C for varying anneal times. Electrical testing of capacitance and leakage current as a function of applied gate voltage was performed using both an HP 4192A impedance analyzer and an HP 4145A semiconductor parameter analyzer. The NCSU Hauser model was used to determine EOT and flat-band voltage (V_{FB}). Analytical characterization of the films included high-resolution

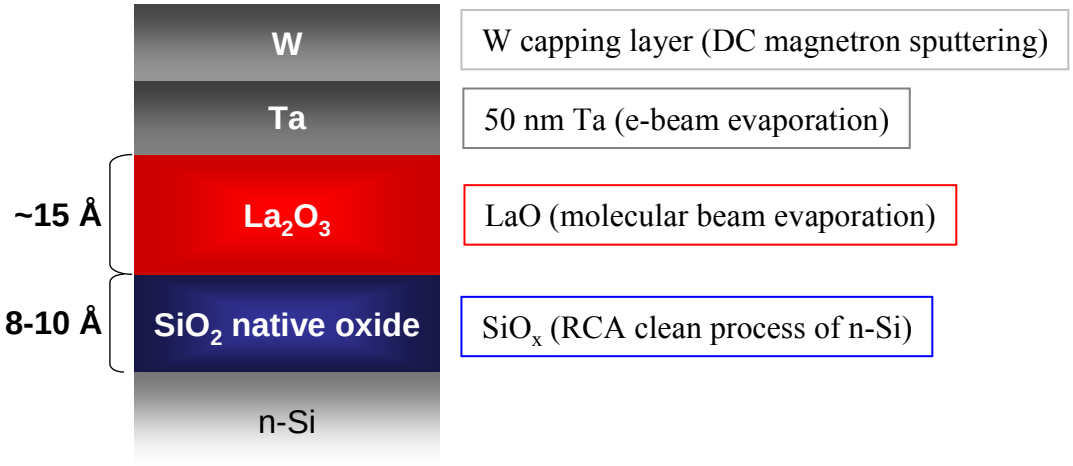


Figure 4.4: *Final MOS gate stack design used for experimental processing to investigate silicate formation at low-temperatures.*

transmission electron microscopy (HRTEM), electron energy loss spectroscopy (EELS) and high-angle annular dark field imaging by scanning transmission electron microscopy (HAADF-STEM) was conducted at the University of California at Santa Barbara, medium energy ion mass spectroscopy (MEIS) conducted at Rutgers University, and x-ray photoelectron spectroscopy (XPS) conducted at North Carolina State University.

4.3 Silicate Formation: *ex situ* Annealing

MOS devices consisting of 10-15 Å of lanthanum oxide on a RCA chemical oxide are analyzed after *ex situ* annealing in a nitrogen environment. **Figure 4.5** shows the HRTEM and the corresponding lanthanum composition analysis of the gate stack design. The HRTEM image and the EELS profiles of the lanthanum confirm that a bi-layer dielectric exists with very little intermixing between the SiO_2 and the La_2O_3 overlayer. The total dielectric layer is approximated to be 25 Å in thickness consisting of ~17 Å of La_2O_3 and 8 Å of SiO_2. Both layers appear to have an amorphous morphology that is attributed to the low substrate temperature of the substrate during deposition. Capacitance-voltage measurements (C-V) of the MOS devices after annealing the La_2O_3/SiO_2 bi-layer, shown in **Fig. 4.6**, show an increase in the capacitance density with anneal time at 400 °C. Note that from **Eqn. (2.7)**,

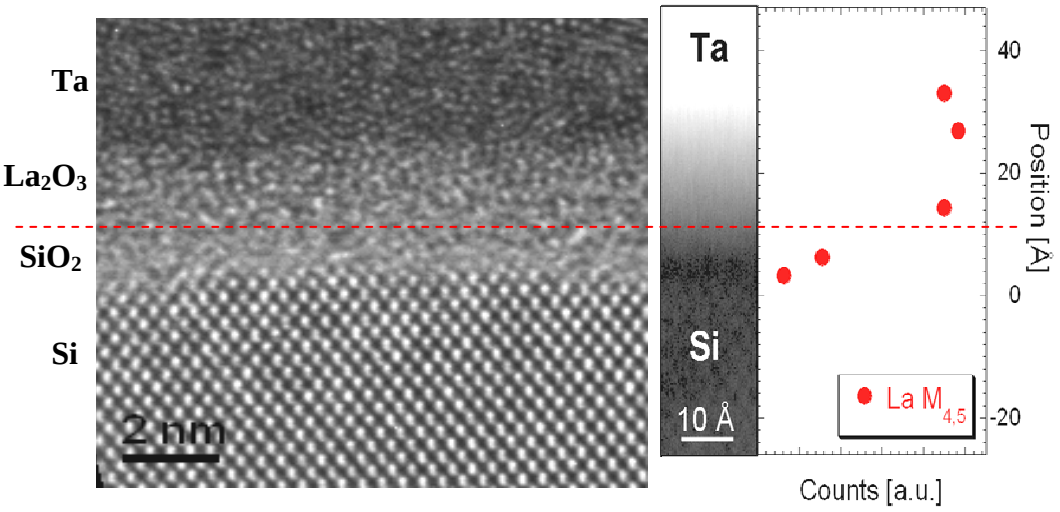


Figure 4.5: *HRTEM of the La_2O_3/SiO_2 bi-layer prior to any ex situ annealing. EELS and HAADF-STEM of the La concentration variation in the bi-layer is shown.*

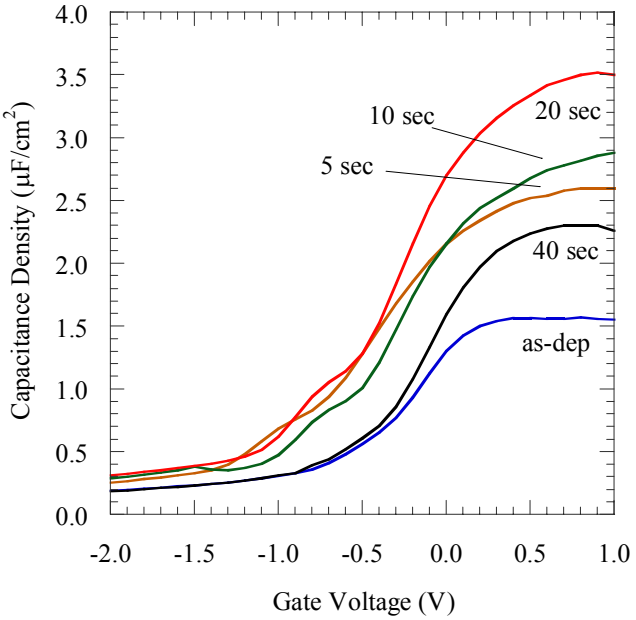


Figure 4.6: *C-V measurements of the La_2O_3/SiO_2 bi-layer (labeled as-deposited) and of the bi-layer annealed ex situ at a temperature of 400 C for 5, 10, and 20 seconds in nitrogen. Solid line represents (-) → (+) voltage sweep. Dashed line represents (+) → (-) voltage sweep. C-V characteristics measured at 1 MHz.*

the increase in capacitance density corresponds to a decrease in the EOT. The EOT for the W/Ta/La_2O_3/SiO_2/Si device decreases from 1.57 nm for the as-deposited bi-layer stack to a minimum of 0.69 nm after 20 s. **Figure 4.7** shows variations in EOT as a function of anneal time for the C-V curves in **Fig. 4.6**. In general, the variation observed for the EOT correlates with the variation observed for the leakage current density. After the anneal time is increased above 20 s an undesirable increase in the EOT and leakage current density is observed. The fluctuation in EOT, namely the initial reduction and the subsequent increase, implies that the silica layer has changed as a result of the RTA treatment. Given the observation of the reduction in EOT from that of the bi-layer, it is predicted that a lanthanum silicate has been formed at the expense of the chemical oxide SiO_2 layer, as described in **§4.2**.

The samples were analyzed by HRTEM in conjunction with EELS to observe the influence that *ex situ* annealing has on the overall dielectric thickness, morphology, and composition variation of the lanthanum oxide/silicate. **Figures 4.8 (a)-(c)** shows the HRTEM images of the of the MOS stack annealed at a temperature of 400 °C for 10, 20 and 40 seconds, respectively. The original bi-layer thickness of ~25 Å is reduced to ~16 Å after 20 seconds

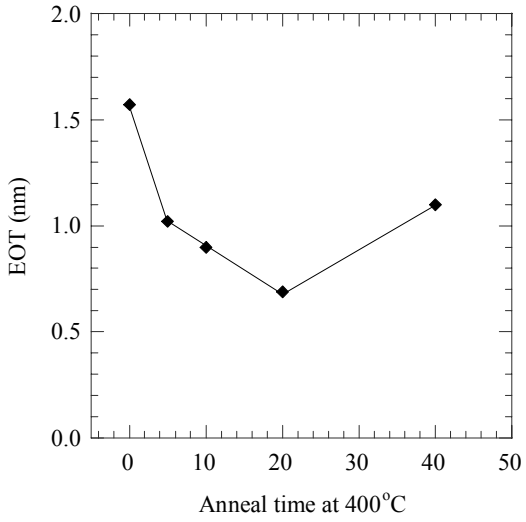


Figure 4.7: *EOT plotted as a function of anneal time at 400 °C in a nitrogen environment. EOT extracted from C-V measurements using NCSU Hauser model.*

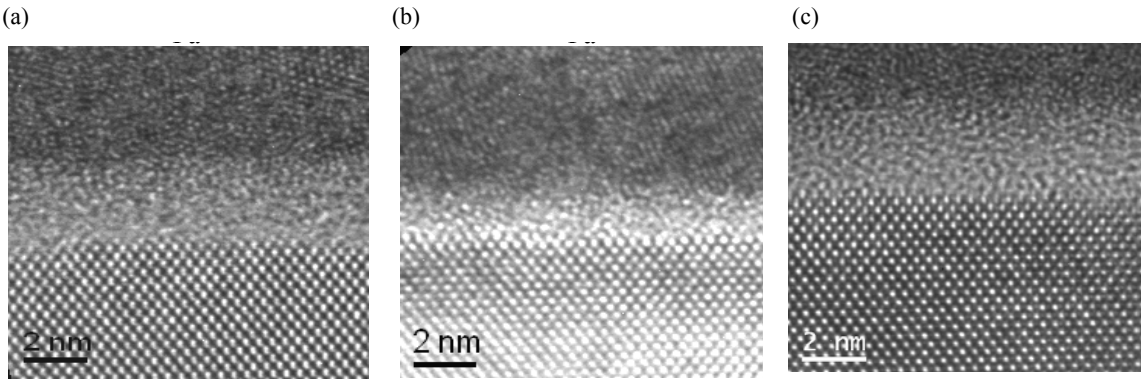


Figure 4.8: *HRTEM of the La_2O_3/SiO_2 bi-layer annealed ex situ at 400 °C for 10, 20, and 40 seconds.*

of annealing. The change in thickness could be due a densification of the individual layers, densification due to silicate formation, or reduction of SiO_2 caused by gettering of oxygen by the Ta electrode or high-κ dielectric. **Figure 4.8 (c)** shows that after a 40 s anneal, the physical thickness increases which agrees well with the electrical data that shows an increase in EOT. **Figures 4.9 (a)-(c)** shows the compositional information for La examined throughout the stack for the as-deposited stack and those stacks annealed for 20 and 40 s, respectively. On the left of each composition plot, a HAADF-STEM image is presented that provides information about the stack. Note that the brightness of the HAADF-STEM image is inversely proportional to the atomic number. Therefore, Ta and La appear bright and the Si and SiO_2 appear dark. In **Fig. 4.9 (a)** an SiO_2 layer is observed in the HAADF-STEM image that is no longer present after 20 s of annealing. This is a clear indication that the SiO_2 interfacial layer has been removed. After annealing the gate stack, a higher concentration of lanthanum is present near the silicon surface and there is a decrease of the gradient observed in the as-deposited sample. After a 40 s anneal, there is an indication that some La could have diffused into the Ta layer. Ta is observed to be unstable on SiO_2, but stable on La_2O_3. Therefore, a reaction product of lanthanum silicate could serve as route for reaction between the La and Ta layers. Such a reaction product could result in an increase in leakage current density that is observed for the 400 °C, 40 s *ex situ* anneal.

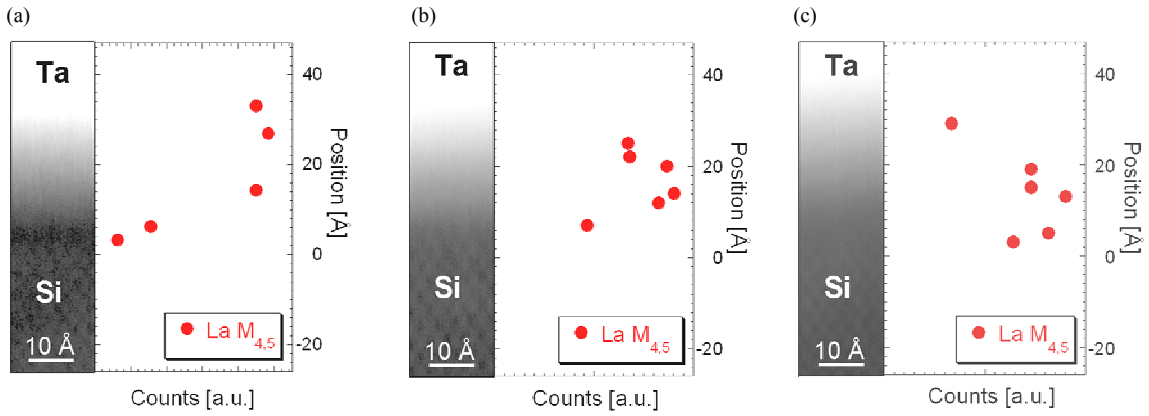


Figure 4.9: *EELS and HAADF-STEM of La in the La_2O_3/SiO_2 bi-layer annealed ex situ at 400 °C for 10, 20, and 40 seconds in nitrogen.*

From the electrical data and the HRTEM/EELS/HAADF-STEM analysis, it is probable that silicate formation is occurring to reduce the thickness and EOT of the samples. At the same time SiO_2 formation occurs due the presence of oxygen in the gate stack or anneal environment that reacts with the silicon substrate, resulting in an increase in overall dielectric thickness and EOT increase. It is noted that despite the probable formation of the SiO_2, lanthanum is still observed at the interface between the dielectric and silicon, but is intermixed in a silica rich silicate. The intermixing results in an overall decrease in the effective dielectric constant to ~10 after the long time anneal.

4.4 Silicate Formation: *in situ* Annealing

It is observed, for the *ex situ* annealing of the La_2O_3/SiO_2 bi-layer, that SiO_2 growth at the silicon interface may be resulting in an increase in the overall thickness and EOT of the gate stack. The source of the oxygen is possibly either from soluble oxygen in the tantalum electrode that could be released upon annealing or from trace oxygen present in the anneal environment itself. The anneal environment of N_2 gas could also have some trace oxygen that can find its way to the silicon substrate through grain boundaries in the poly-crystalline Ta electrode. Finally, the tungsten capping layer could also be serving as a supply of oxygen. Considering these oxygen sources, there arises a need for enhanced control of the oxygen available during the silicate reaction anneal. One method for mitigating the influence

of the oxygen that may be available during the *ex situ* anneal is to anneal the bi-layer in a low pO_2 environment immediately after the La_2O_3 growth on the SiO_2 chemical oxide, while still in the growth chamber. The pO_2 of this *in situ* anneal can be precisely controlled by regulating the ultrahigh purity O_2 gas flow into the chamber to achieve pressures of 10^{-8} to 10^{-6} Torr.

Immediately after growth of the lanthanum oxide, the substrate was subjected to a 500 °C, 30 min *in situ* anneal at 5 x 10^{-7} Torr. After the *in situ* anneal, the samples were capped with an electrode and processed to create MOS devices. No additional *ex situ* annealing was performed. **Figure 4.10** shows the resultant HRTEM for the bi-layer film with an *in situ* anneal at a pressure of 5x10^{-7} Torr. It is observed that the bi-layer that exists prior to the *in situ* anneal (**Fig. 4.5**) is no longer present. Instead a homogenous layer that is amorphous in morphology and is approximately 2.0 nm in thickness is formed. Simulation of MEIS for the bi-layer dielectric after the *in situ* anneal, shown in **Fig. 4.11**, provides information concerning the dielectric composition and thickness. Simulation suggests a homogenous dielectric La_2O_3:$4SiO_2$ that is ~12.5 Å thick. The high concentration of the SiO_2 is likely due

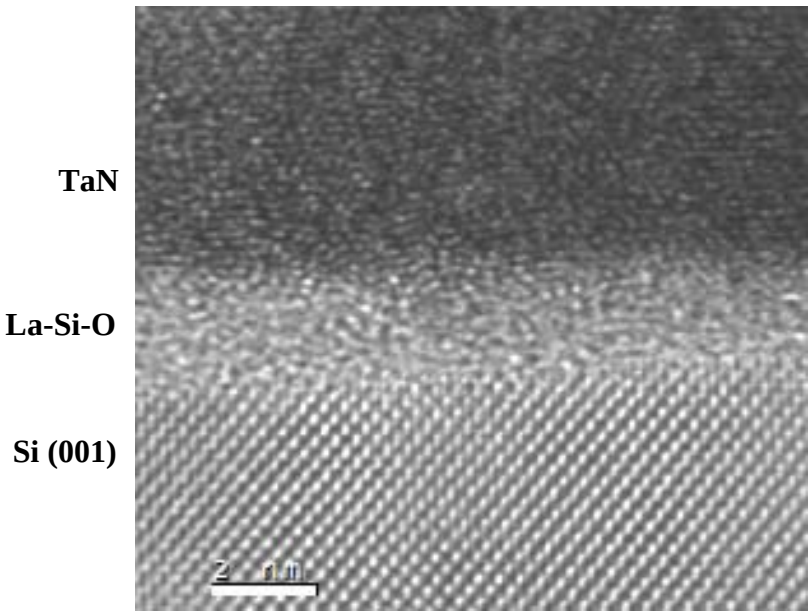


Figure 4.10: *HRTEM of the La_2O_3/SiO_2 bi-layer annealed in situ at 500 °C for 30 min at 5x10^{-7} Torr.*

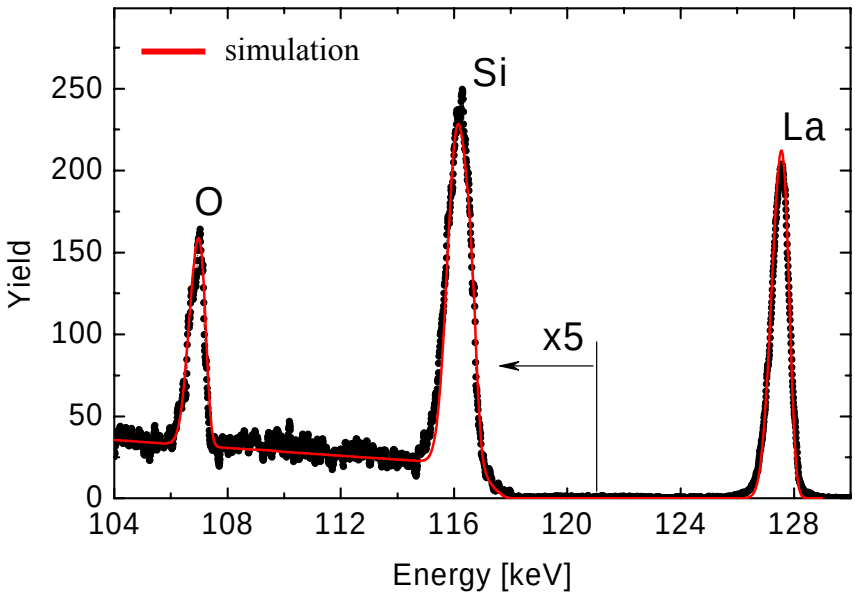


Figure 4.11: *MEIS of the of the La_2O_3/SiO_2 bi-layer annealed in situ at 500 °C for 30 min at $5x10^{-7}$ Torr.*

to hydroxide formation resulting from the fact that MEIS characterization requires that there be no capping layer present on the dielectric. In the MEIS simulation, the silicon concentration in the silicate is obtained from the relative La and O peak areas from the MEIS spectrum and the expected oxidation states of each element. An increase in oxygen concentration from the hydroxide will directly result in increased silicon concentration. The important result to be derived from the MEIS is that no interfacial SiO_2 is observed within the spatial resolution and detection limit of the technique, as can be seen from the goodness of fit for the La and O peak areas. The thickness observed by MEIS is less than that obtained by HRTEM, probably due to differences in film density values for the MEIS simulation and the actual film.

It might be expected that the EOT can be specifically tailored by controlling the temperature of the *in situ* anneal in the low pO_2 environment. **Figs. 4.12** and **4.13** shows the capacitance density and leakage current density for the $Ta/La_2O_3/SiO_2/Si$ MOS devices after a 600 °C, 30 min *in situ* anneal at 5 x 10^{-7} Torr. Modeling of the C-V curves provides an EOT value of

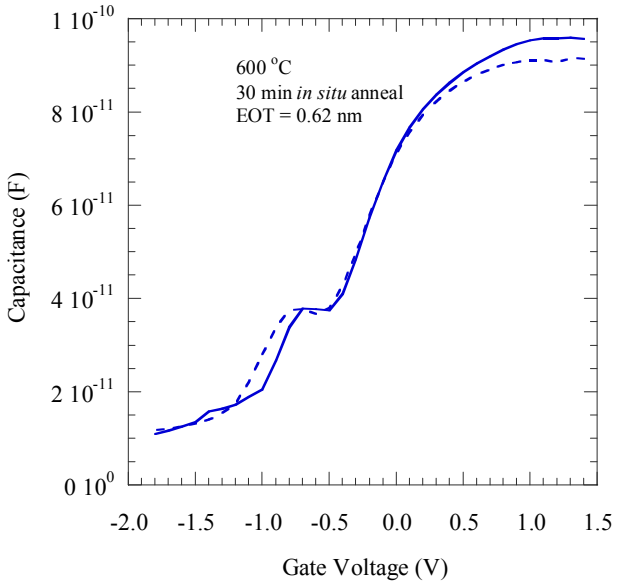


Figure 4.12: *C-V measurements of the La_2O_3/SiO_2 bi-layer after an in situ at 500 and 600° C for 30 min at 5x10^{-7} Torr. Solid line represents (-) → (+) voltage sweep. Dashed line represents (+) → (-) voltage sweep. C-V characteristics measured at 1 MHz. EOT values extracted from C-V measurements using NCSU Hauser model.*

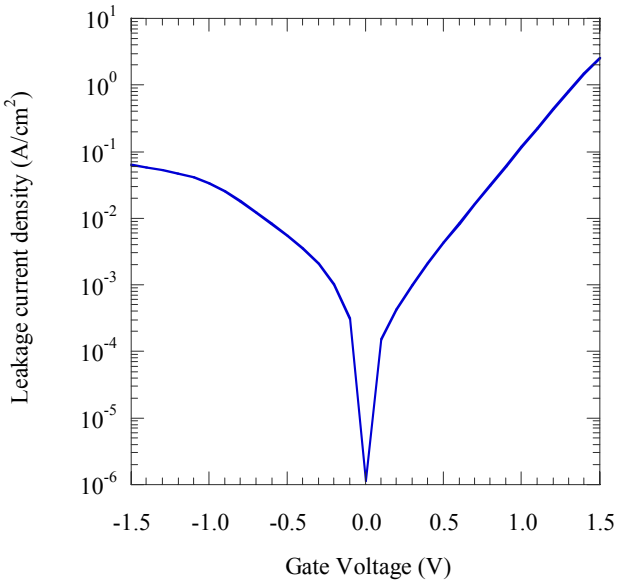


Figure 4.13: *J-V measurements of the La_2O_3/SiO_2 bi-layer after an in situ at 500 and 600° C for 30 min at 5x10^{-7} Torr. J evaluated at a V_{FB} + 1 V.*

4.9 Å and 6.3 Å for the 500 and 600° C, 30 min *in situ* anneals, respectively. The leakage current density is evaluated to be 5.0 A/cm^2 (500 °C) and 0.06 A/cm^2 (600 °C) for the devices, evaluated at a V_{FB} + 1V.

4.5 Conclusions

The alloying of a La_2O_3/SiO_2 bi-layer (15.7 Å EOT, J @ V_{FB}+1V > 10 A/cm^2) to form a lanthanum silicate has been observed at temperatures as low as 400 °C. The result is a decrease in the overall EOT to 6.9 Å and a decrease in J @ V_{FB}+1V = 0.7 A/cm^2). However, device characteristics deteriorate with the low-temperature *ex situ* annealing at longer times possibly due to,

- oxygen release from the gate electrode/capping layer resulting in a silica rich silicate (i.e. increase in EOT)
- oxygen uptake from the annealing environment, resulting in a silica rich silicate
- dielectric reaction with Ta causing an increase in leakage

Each of these events limits the device scaling (low EOT, J) at higher temperatures. In this regard, a method is presented which allows precise control of the oxygen content during the silicate reaction anneal by way of an *in situ* anneal of the La_2O_3/SiO_2 bi-layer stack prior to electrode capping and removal from the growth chamber. In doing so, the EOT is reduced to values as low as 5 Å, but at the cost of leakage. It is noted the processing temperature is consistent with 'reverse-gate' MOSFET processing that requires a temperature less than 500-600 °C. For MOSFET standard processing, these values offer promise for creating MOS devices with improved properties even after the high-temperature annealing that is required for source/drain dopant activation. To achieve this result, it is apparent that the parasitic events observed as a byproduct of low-temperature *ex situ* annealing must be accounted for and significantly decreased.

5. LANTHANUM OXIDE-BASED MOS DEVICES: HIGH-TEMPERATURE PROCESSING

5.1 Introduction

As metal-oxide-semiconductor field effect transistor (MOSFET) devices are scaled, a high-κ gate dielectric is needed to replace SiO_2 films due to their high leakage currents when thickness decreases below 1.5 nm.[25] The implementation of a high-κ dielectric to replace SiO(N) dielectric in a MOSFET device requires an operational optimization of the MOS gate stack while still adhering to the stringent requirements to process the transistor device. The severe thermal requirement needed for source/drain dopant activation typically results in an increase in the oxide thickness and unwanted reaction between different layers of the gate stack. High defect levels and impurity diffusion found in high-κ materials and at the Si interface result in a decrease in the mobility of the semiconductor and unwanted threshold voltage values. [22,207] The goal of this chapter is to examine the effect of the high-temperature source/drain activation anneal on the MOS gate stack based on a lanthanum silicate. A gate metal will be used as a replacement for common poly-silicon electrode, as it allows for a reduction in the poly-depletion (see §2.2.2). In order to learn more about the electrical and materials based mechanisms, an effort has been made in investigate the effects of increasing the thermal budget of the gate stack up to the source/drain activation anneal temperature/time.

In **Chapter 4**, a low-temperature processing route for formation of lanthanum silicate was investigated. It was determined that precise anneal environment control was required to prevent unwanted SiO_2 growth during the reaction anneal. Therefore, an *in situ* anneal was administered to the La_2O_3/SiO_2 bi-layer in the molecular beam deposition chamber, prior to gate metal deposition. As a consequence, MOS devices with 0.5 nm equivalent oxide thickness (EOT) and relatively low leakage were formed. SiO_2 growth is observed even with low-temperature annealing, provided a sufficient supply of oxygen is present so as to allow oxygen to diffuse to the silicon interface. Although an *in situ* anneal (to form the lanthanum silicate) in a controlled pO_2 environment is shown to decrease this SiO_2 formation, the gate

stack is still required to undergo the subsequent MOSFET process, which includes the high-temperature (995-1050 °C, 5-10 sec) source/drain activation anneal. To gain a true measure of how well the high-κ dielectric will perform in a MOSFET device, it is necessary to observe the effect of this anneal. However, the gate dielectric properties can be unfairly judged if the gate electrode is not itself thermally stable itself or acts as a supply of oxygen. The first two sections of this chapter, **§5.3** and **§5.4** deal with optimization of the gate electrode. The optimization of the tungsten metal capping layer in terms of thermal stability and oxygen concentration is investigated in **§5.5**. Once the gate stack materials have been optimized, it is then important to examine the thermal stability of lanthanum-silicate on silicon. In **§4.4**, the result of the *in situ* anneal was the consumption of the SiO_2 by the La_2O_3 allowing for the appearance of lanthanum close to the silicon substrate. This suggests that the lanthanum may diffuse into the silicon, particularly after a high-temperature anneal. In order to enhance observations of lanthanum diffusion into the silicon, a back-side secondary ion mass spectroscopy method is utilized and results are described in **§5.6**. Finally in **§5.7**, the density if interface traps and the fixed charge of the lanthanum silicate based MOS capacitors is reported.

5.2 Process Definition

5.2.1 Experimental

*For a more detailed explanation of each of the individual processing steps, the reader is referred to **Chapter 3**. A summary of the experimental plan follows.*

In this work, an n-type (Sb-doped, 0.2 Ω cm) and p-type (B-doped, 0.5 Ω cm) Si(001) are prepared by performing an RCA clean process, yielding 8-10 Å layer of SiO_2. Lanthanum oxide was deposited by thermal evaporation at a pO_2 of $1x10^{-6}$ Torr and substrate temperature of 200°C. The deposition rate of the La_2O_3 of approximately 0.05 Å/s was used to achieve a final thickness of 10-15 Å, as monitored by a quartz crystal rate monitor. The fabrication of the MOS devices is outlined in **Fig. 5.1**. Following the positive results in

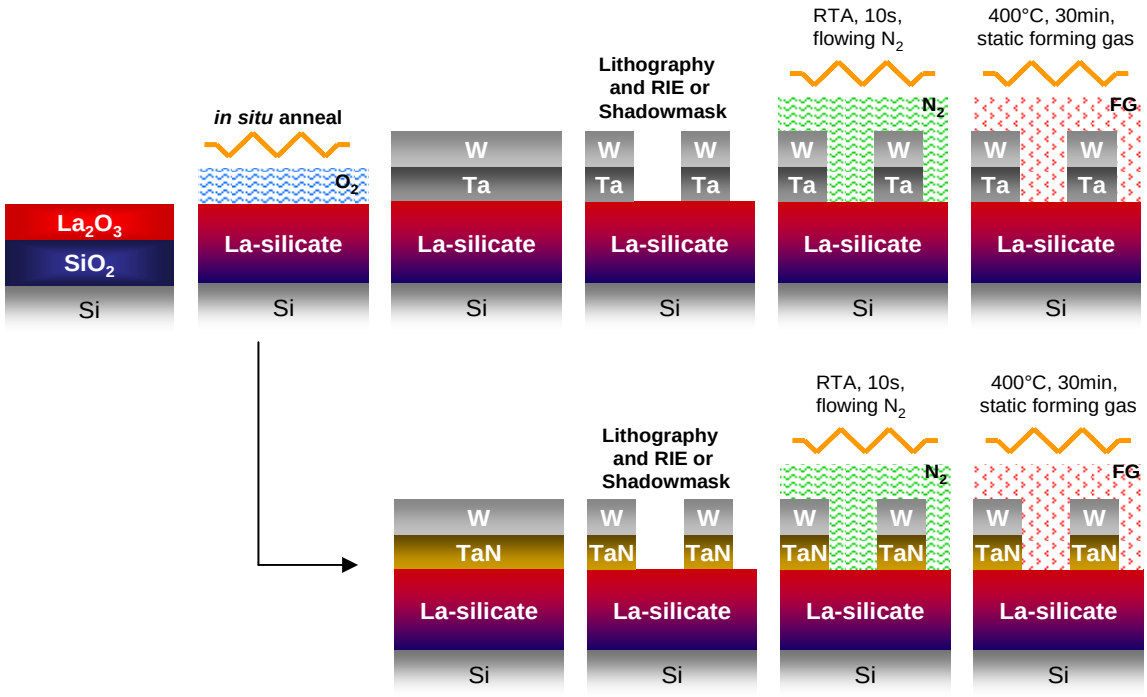


Figure 5.1: *General process outline consisting SiO_2 chemical oxide formation, La_2O_3 growth, in situ reaction anneal, metallization (Ta and TaN), subsequent capacitor formation, and annealing.*

§4.4, an *in situ* anneal was performed at a temperature 500 °C for 30 minutes at a pO_2 of $1x10^{-6}$ Torr. Tantalum and tantalum nitride are investigated as gate electrodes. Ta is deposited *in situ* via E-beam evaporation at a pressure $4x10^{-8}$ Torr and TaN was deposited *ex situ* using a DC magnetron sputtering system a metal contact. Care was taken to reduce the exposure of the lanthanum silicate to atmosphere prior to TaN deposition. Following the electrode deposition, a tungsten capping layer was deposited for enhanced electrical contact. For capping of Ta, the W was deposited *ex situ* via DC magnetron sputtering. For capping of TaN, the W was deposited in a connected DC magnetron sputtering chamber such that vacuum was not broken between deposition of the metal layers. Detailed optimization of TaN and W growth is provided in their respective sections, **§5.4** and **§5.5.**

Capacitor devices were masked using standard photolithography techniques and subsequently reactive ion etched (RIE), although some devices were also shadow deposited

to bypass the photolithography and RIE processing. Post metallization annealing (PMA, or RTA) was conducted at temperatures between 400-1000 °C for varying anneal times. Electrical testing of capacitance and leakage current as a function of applied gate voltage was performed using an HP 4192A impedance analyzer and an HP 4145A semiconductor parameter analyzer, respectively. The NCSU-CVC model was used to determine equivalent oxide thickness and flat-band voltage (V_{FB}). Analytical characterization of the films included high-resolution transmission electron microscopy (HRTEM) and high-angle annular dark field imaging by scanning transmission electron microscopy (HAADF-STEM) was conducted at the University of California at Santa Barbara and North Carolina State University and medium energy ion mass spectroscopy (MEIS) conducted at Rutgers University. X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS, front-side and back-side) was conducted at North Carolina State University in the Analytical Instrumentation Facility (AIF). In addition x-ray diffraction (XRD) was conducted with the Electroceramic Thin Film group at NCSU.

5.3 MOS Characterization with Tantalum Electrode

The MOS gate stack based on the lanthanum silicate was first analyzed with the use of a tantalum gate electrode. Tantalum has several properties that make it ideal for use as a gate electrode in MOSFET devices, such as a high melting point, thermodynamic stability in contact with lanthanum oxide (i.e. $-\Delta G_f^o$ (La_2O_3) > $-\Delta G_f^o$ (Ta_2O_5)),[208] and ease of etch processing. Most importantly, the work function of Ta (4.2 eV)[209] is ideal for nMOS devices that require a work function near that of 4.0 eV, the band edge for p-type Si. On the down side, Ta is reactive in contact with SiO_2 to from a silicide.[210,211] Therefore, it is questionable whether or not Ta is able to withstand high-temperature processing on lanthanum silicate.

Figure 5.2 shows the capacitance-voltage measurements for the W/Ta/$LaSiO_x$/Si devices annealed between 400 and 1000 °C for 10 s in nitrogen. As the anneal temperature is increased, a decrease in the accumulation capacitance density is observed, resulting in a increase in EOT from 0.67 nm after a 400 °C, 10 s anneal to 1.57 nm after a 1000 °C, 10 s

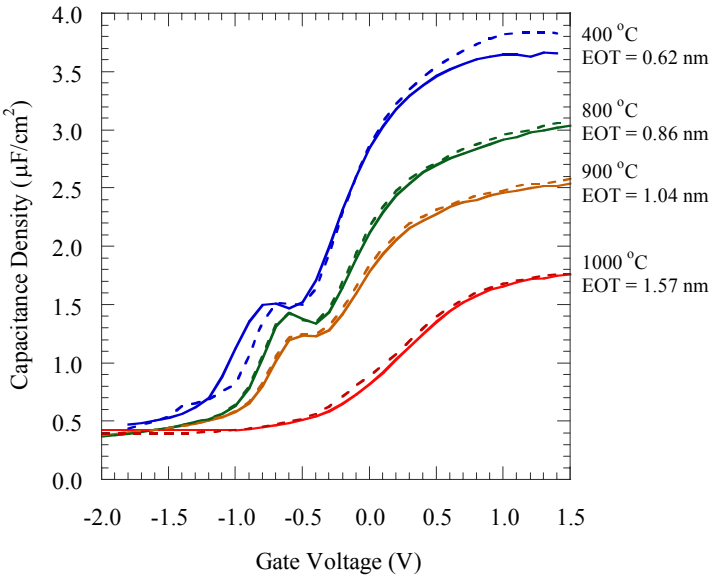


Figure 5.2: *C-V measurements of W/Ta/LaSiO$_x$/Si MOS devices after annealing ex situ at temperatures of 400 – 1000 °C for 10 s in nitrogen. Solid line represents (-) → (+) voltage sweep. Dashed line represents (+) → (-) voltage sweep. C-V characteristics measured at 1 MHz. EOT values extracted from C-V measurements using NCSU Hauser model.*

anneal. In addition, the inflection observed in the transient region between the depletion and accumulation is minimized and the V_{FB} is shifted positive. Note that this inflection is a result of a high interface trap density (D_{IT}), which will be discussed in **§5.7**. The increase in EOT is most likely due to oxygen reaction with the silicon substrate to produce interfacial SiO_2, thereby minimizing the effect of the high-κ dielectric that is observed after a 400 °C anneal.

Figure 5.3 shows the measured leakage current density as a function of device EOT. For comparison, the leakage current density as a function of EOT for SiO_2 is shown. After low-temperature annealing, the trend observed follows what would be expected for thin SiO_2 formation. Following this trend, the leakage current density of the lanthanum silicate is approximately six orders of magnitude less than the leakage current density of SiO_2 at similar

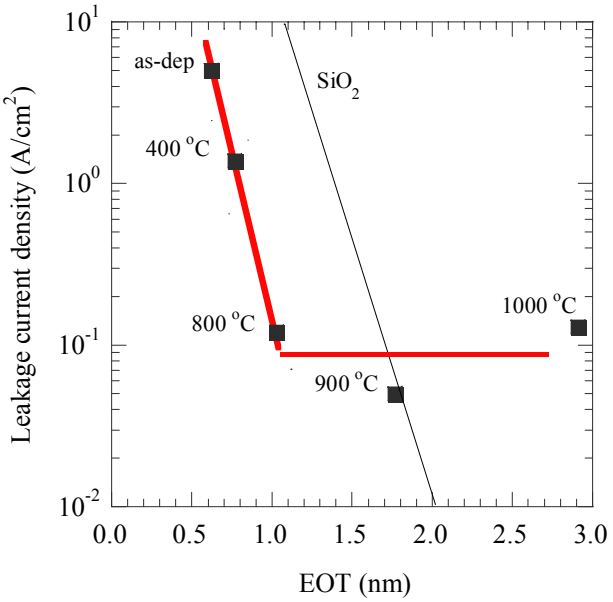


Figure 5.3: *Leakage current density plotted as a function of EOT for W/Ta/LaSiO$_x$/Si MOS devices after annealing ex situ at temperatures of 400 – 1000 °C for 10 s in nitrogen.*

thicknesses. What is troubling is the fact that after anneal temperatures > 800 °C, the trend of the leakage current density no longer follows that expected simply by SiO_2 growth. Recall that the measured value for the leakage current density is reported at a flat-band voltage +1 V. As observed in the C-V measurement in **Fig. 5.2**, the flat-band voltage is constant for the low-temperature annealed samples, but a positive shift is observed after high-temperature annealing. As a result, the leakage current density is evaluated at a much higher voltage after high-temperature annealing. Due to this increased field across the oxide, it is reasonable to assume that leakage would increase. Additional evidence to the fact that the V_{FB} shift is responsible for this unwanted increase in leakage current density with respect to EOT is provided in **Fig. 5.4**. Here, similar trends are shown using both p-type and n-type silicon substrates. An offset is observed such that the leakage current density of the p-type samples is higher than that of the n-type samples. A result of the V_{FB} shift, leakage current density of the p-type samples is measured at a higher field than the n-type samples. Such an increase in EOT and increase in leakage make it unacceptable for this MOS gate stack to be

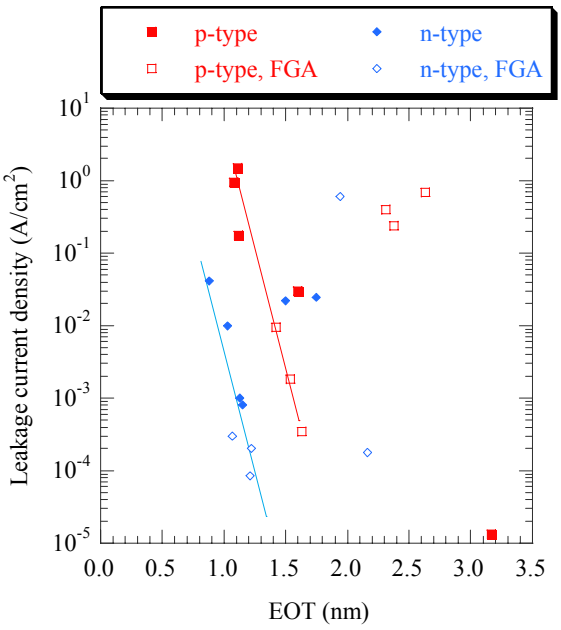


Figure 5.4: *Leakage current density plotted as a function of EOT for W/Ta/LaSiO$_x$/Si MOS devices with n-type and p-type silicon after ex situ annealing at temperatures of 400 – 1000 °C for 10 s in nitrogen.*

considered for standard MOSFET processing requiring high-temperature annealing (> 800 °C). However, the device data observed with low-temperature annealing make this gate stack an attractive candidate for low-temperature 'reverse-gate' processing.

The obvious solution to fixing the problem of increased leakage current density with high-temperature annealing is to reduce the observed flat-band voltage shift. A logical source of the V_{FB} shift would be the change in the work function of the Ta electrode. XRD of the Ta, shown in **Fig. 5.5**, was used to better understand the state of the as-deposited Ta electrode with an increase in anneal temperature in nitrogen. In the as-deposited state, the metastable β-Ta is the most likely identification[212] and is common for low-temperature Ta deposition.[213] The fine grain structure yields very broad peak widths that add uncertainty to the identification. Little change in the phase of the Ta is observed with anneal temperatures ≤ 800 °C. However, an increased anneal temperature results in a significant reaction with the nitrogen anneal environment and a phase transformation to α-Ta. The formation of a Ta_2N[214] phase by annealing the Ta in nitrogen agrees with reports in literature.[210] A similar phase

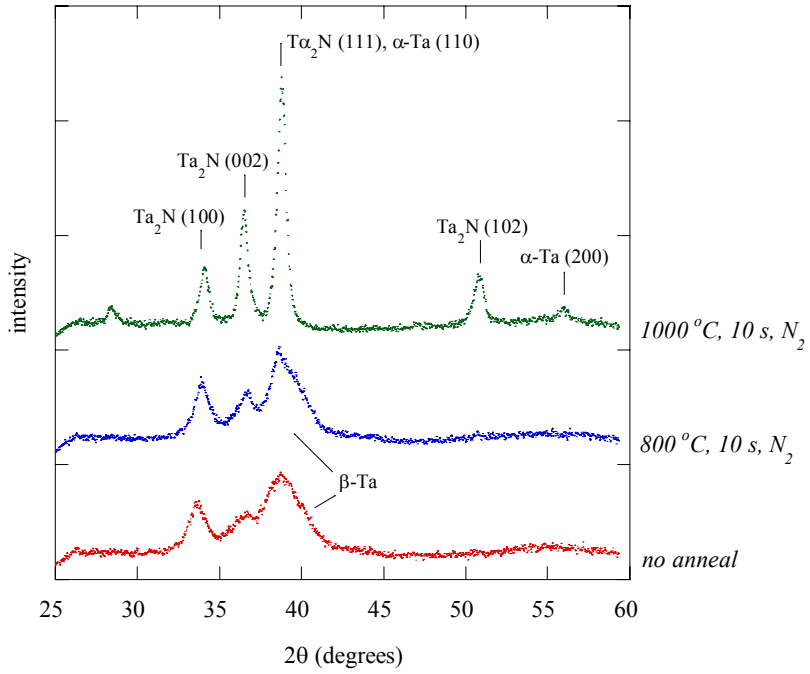


Figure 5.5: *XRD patterns of Ta after deposition (no anneal) and after annealing at temperatures of 800 and 1000 °C for 10 s in nitrogen.*

transformation of the Ta electrode is observed with a W capping layer. Such instability of the gate electrode could lead to the observed flat-band voltage shift. Even, if it is not the solution to the flat-band voltage shift problem, it would be advantageous to use a more thermally stable gate metal.

5.4 MOS Characterization with Tantalum Nitride Electrode

Perhaps a better choice for the gate metal is stoichiometric TaN. As opposed to Ta, which is thermally unstable in contact with SiO_2, TaN is stable.[211] Unfortunately, the work function is highly dependent on the nitrogen concentration in the TaN. The literature reports values for the TaN work function to be between 3.8[209] and 4.5-4.7 eV.[215] It is noted that the work function of a metal can be determined by the flat-band voltage as a function of different dielectric thicknesses.[19] By examining the y-axis intercept, the work function is determined independent of the dielectric's fixed charge component. By evaluating the y-intercept as EOT goes to zero, the work function of the metal can be derived. This method is only valid

if the condition of the dielectric (i.e. fixed charge, composition) is constant throughout the high-κ dielectric. Therefore, for the processing of the lanthanum silicate discussed in this work, the method is invalid since it would be necessary to vary the SiO_2 interfacial layer for corresponding thickness changes in La_2O_3. The SiO_2 growth is limited by the RCA growth method. In addition, upon annealing, the composition of the lanthanum is changing throughout the dielectric. Since an accurate assessment of the TaN work function cannot be made in this work, care must be taken to avoid the alteration in the TaN throughout processing. Only then can a comparison be made between data sets with similar processing.

To deposit the TaN electrode, an ultra-high vacuum deposition system was constructed as described in **§3.1.2**. Optimization of the TaN growth consisted of first altering the pressure of the system with a constant Ar/N_2 flow ratio, and then optimizing the flow ratio at a constant pressure. The films were analyzed by XRD, the results of which are shown in **Figs. 5.6** and **5.7**. The XRD patterns are shown with the subsequent α-W metal capping layer. With constant Ar/N_2 flow ratios, an increase in deposition pressure resulted in a better definition of the (111) and (220) diffraction peaks of cubic-TaN.[216] The (110) α-W diffraction peak[217] reduced the ability to observe the (200) peak of TaN. A pressure of 4.5 mTorr, was the maximum pressure able to be achieved given the butterfly valve used to toggle pressure in the system. Using that pressure, the Ar/N_2 flow ratio was optimized. As shown in **Fig, 5.7**, a flow ratio of 12.5/1:Ar/N_2 provided the most well defined diffraction peaks for TaN, specifically the (200) TaN diffraction peak. It is noted that an increase in the flow ratio of Ar/N_2 greater than 10/1 resulted in a polycrystalline phase that most likely consists of multiple Ta_xN_y phases. The thermal stability as observed by XRD of the various flow ratios are shown in **Fig. 5.8**., after a 1000 °C, 5 s anneal in nitrogen. Note that the flow ratio of 10/0:Ar/N_2 results in a as-deposited β-Ta phase which subsequently results in Ta_2N consistent with the results presented in **§5.3** for Ta grown by E-beam evaporation.

For all conditions in which cubic-TaN was found in the as-deposited state, the 1000 °C, 5 s anneal in nitrogen resulted in no phase transformation. The MOS devices with a TaN electrode were subsequently processed using a pressure of 4.5 mTorr and a flow ratio of

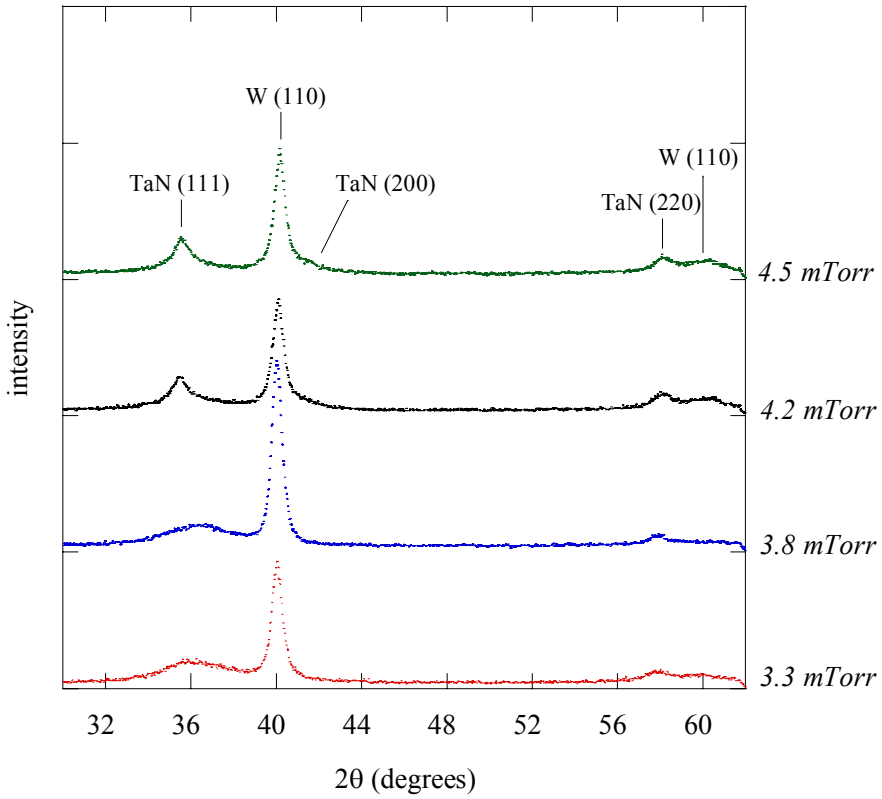


Figure 5.6: *XRD patterns of TaN as a function of deposition pressure deposited via DC magnetron sputtering at a Ar/N_2 flow ratio of 15/1 and target power of 75 W.*

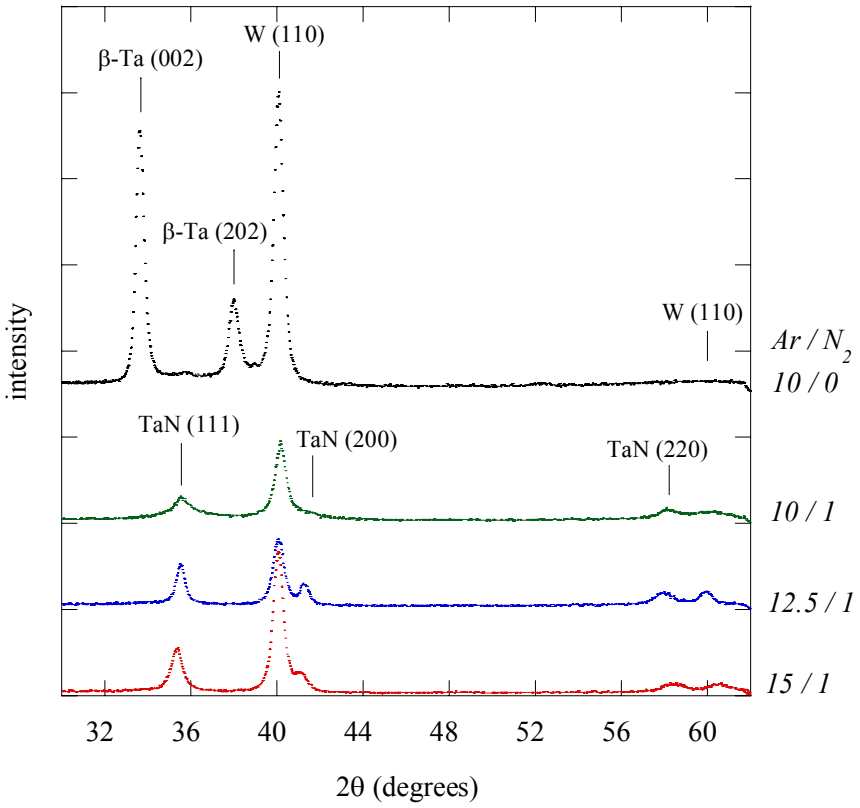


Figure 5.7: *XRD patterns of TaN as a function of Ar/N_2 flow ratio deposited via DC magnetron sputtering at a pressure of 4.5 mTorr and a target power of 75 W.*

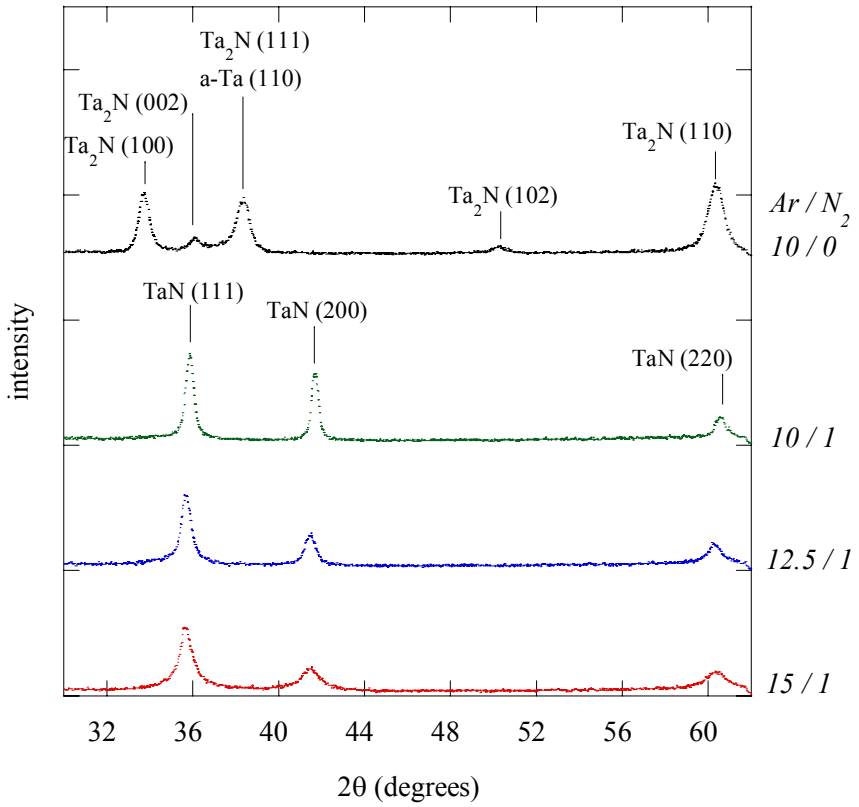


Figure 5.8: *XRD patterns of TaN (and Ta) after a 1000 °C, 5 s anneal in nitrogen. Diffraction patterns shown for various Ar/N_2 flow ratios deposited via DC magnetron sputtering at a pressure of 4.5 mTorr and a target power of 75 Watts.*

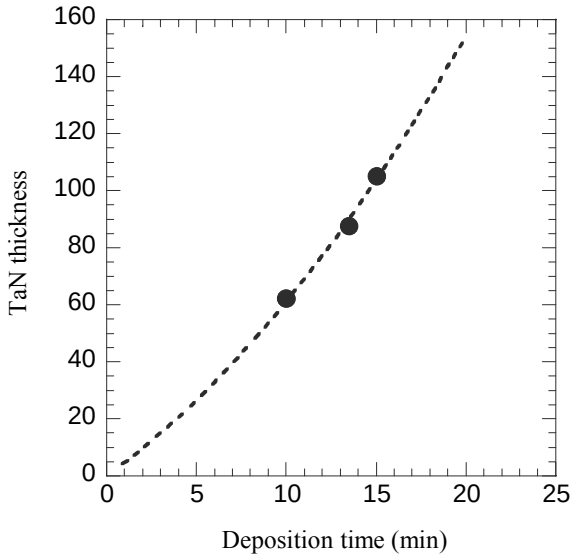


Figure 5.9: *TaN thickness as a function of deposition time at a pressure of 4.5 mTorr, Ar/N_2 flow ratio of 12.5/1, and a target power of 75 W. Thickness determined using Dektak profilometry.*

12.5/1:Ar/N_2. The deposition rate for this condition, using Dektak profilometry, is observed from **Fig. 5.9** to be ~60 Å/min. The thickness of metal nitride electrodes is observed to have a deleterious effect on device properties.[218] Therefore, a thickness of TaN was targeted to be less then 20 nm.

Figures 5.10 and **5.11** show the EOT and V_{FB}, respectively, extracted from the capacitance-voltage measurements for the W/TaN/$LaSiO_x$/Si devices annealed between 400 and 1000 °C for 10 s in nitrogen. The large increase in the EOT as observed for the Ta electrode after 800 °C annealing, is not observed when using a TaN electrode. After a 1000 °C, 10 s anneal, an EOT of ~ 1.1 nm is observed for the gate stack using a TaN electrode. This represents an extremely low EOT value given the processing conditions, indicating a decrease in the allowable SiO_2 formation at the silicon interface. From the flat-band voltage measurements shown in **Fig. 5.11**, the TaN is observed to have a work function < 4.0 eV, and is slightly lower than that of Ta. This is reasonable considering that the work function for TaN has been reported to be as low as 3.8 eV.[209] However the presence of positive fixed charges (i.e. oxygen vacancies) are known to reduce the effective work function of the gate stack. In

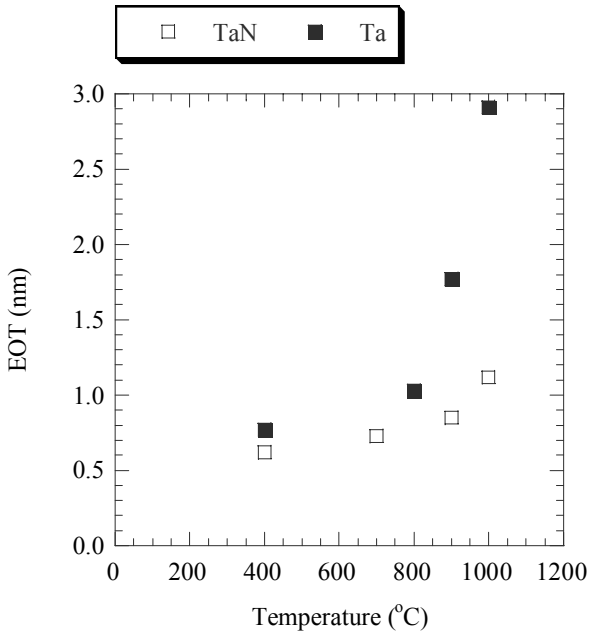


Figure 5.10: *EOT as a function of ex situ anneal temperature for Ta and TaN electrodes in W/Ta(N)/LaSiO$_x$/Si MOS devices. Ex situ annealing performed at temperatures of 400 – 1000 °C for 10 s in nitrogen. EOT extracted from C-V measurements using NCSU Hauser model.*

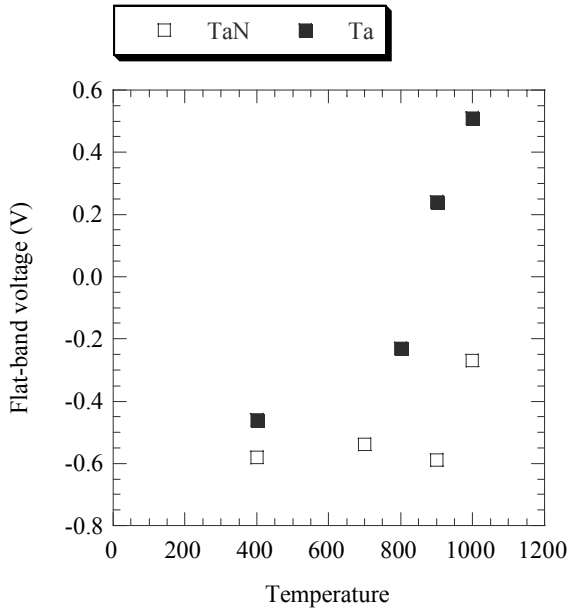


Figure 5.11: *V_{FB} as a function of ex situ anneal temperature using Ta and TaN electrodes on W/Ta(N)/LaSiO$_x$/Si MOS devices. Ex situ annealing performed at a temperatures of 400 – 1000 °C for 10 s in nitrogen. V_{FB} values extracted from C-V measurements using NCSU Hauser model.*

addition, work functions of metals are known to be different, based on varying the high-κ dielectric with which it is in contact. Nevertheless, the flat-band voltage is not observed to shift at temperatures below at least 900 °C. As a result, the leakage current density as a function of EOT, as shown in **Fig. 5.12**, does not experience an increase in leakage current density with high-temperature annealing as does an MOS device with a Ta electrode. For comparison, **Fig. 5.12** also shows the leakage current density for HfO_2[219], La_2O_3[56], and thicker $LaSiO_x$.[220] It is noted that the leakage current density reported for La_2O_3 and $LaSiO_x$ are only for low-temperature annealing of the gate stack.

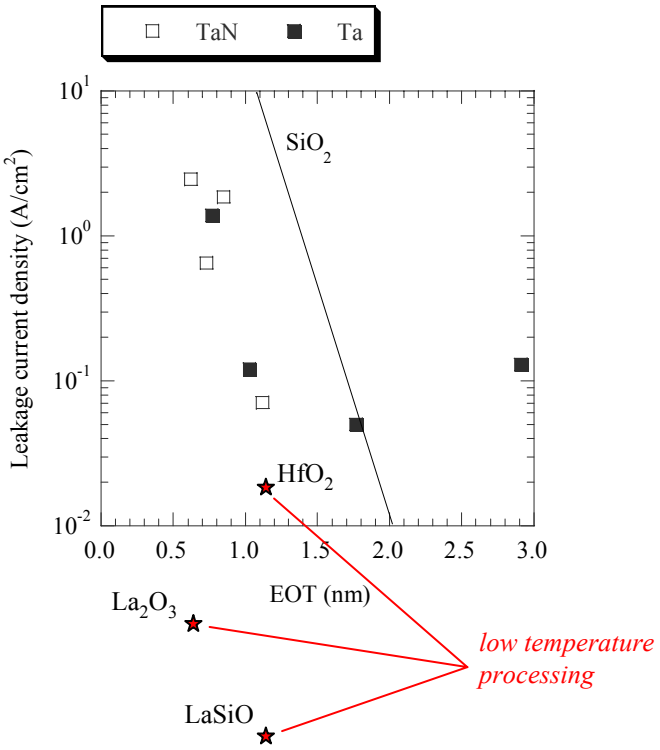


Figure 5.12: *Leakage current density plotted as a function of EOT using Ta and TaN electrodes on W/Ta(N)/$LaSiO_x$/Si MOS devices after ex situ annealing at temperatures of 400 – 1000 °C for 10 s in nitrogen. Comparison is made for literature reports for low-temperature annealing HfO_2[219], La_2O_3[56], and thicker $LaSiO_x$[220].*

It is observed that for annealing the W/TaN/$LaSiO_x$/Si gate stack at shorter times, a decrease in EOT is observed with values as low as 0.99 nm after a 1000 °C, 5 s annealing in N_2. Unfortunately, this also suggests that the EOT might be uncontrolled with higher anneal times. **Figure 5.13** shows the capacitance-voltage measurements as a result of annealing the MOS gate stack at 1000 °C for 1-20 s. **Figure 5.14** shows the extracted EOT values as a function of anneal time. It is observed that the EOT increases nearly 1.5 nm for every 10 seconds of anneal time at 1000 °C.

In summary, TaN is shown as an improvement over Ta in use on the lanthanum silicate-based MOS gate stack. Such a stack is promising for use in standard MOSFET processing requiring high-temperature annealing. Although EOT and leakage are decreased after a high-temperature anneal, the reported EOT values still increase with 1000 °C annealing. This result indicates that the source of oxygen still remains either in the annealing environment or in the tungsten capping layer.

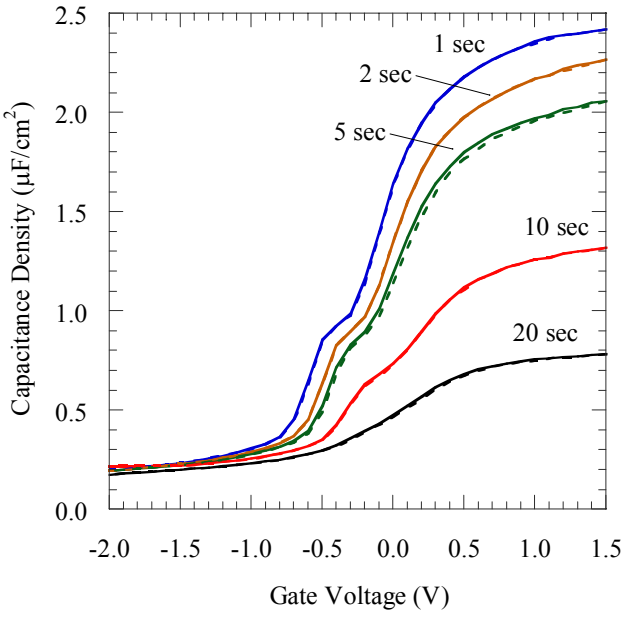


Figure 5.13: *C-V measurements of W/TaN/$LaSiO_x$/Si MOS devices after annealing ex situ at a temperature of 1000 °C for 1 - 20 s in nitrogen. Solid line represents (-) → (+) voltage sweep. Dashed line represents (+) → (-) voltage sweep. C-V characteristics measured at 1 MHz.*

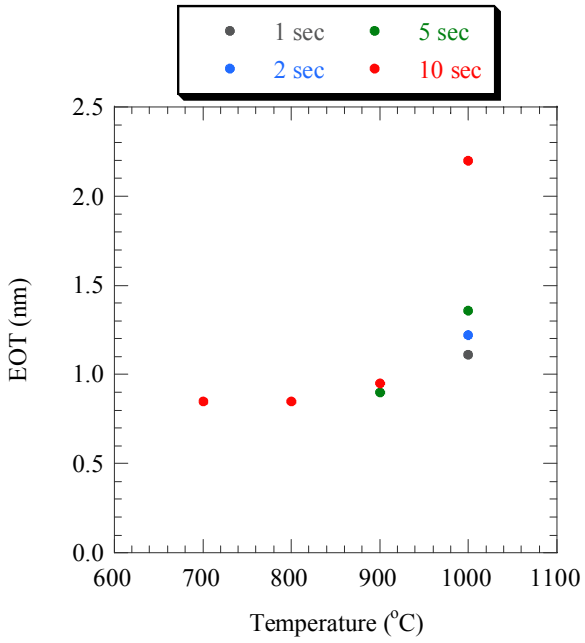


Figure 5.14: *EOT for W/TaN/LaSiO$_x$/Si MOS devices shown as a function of ex situ anneal time and temperature. Ex situ annealing performed at a temperature of 700 - 1000 °C for 1 - 20 s in nitrogen. EOT extracted from C-V measurements using NCSU Hauser model.*

5.5 Affect of Tungsten Metal Capping

The consequence of tungsten metal purity on the electrical properties of an annealed MOS gate stack with a lanthanum silicate gate dielectric is also investigated. As a function of anneal temperature, EOT has been reported for Ta and TaN gate electrodes with a W capping layer. The data indicates that the high-temperature phase stability of the TaN compared to Ta when annealed at temperatures ≥ 800 °C resulted in better control over the characteristics of the gate stack. Improvement in EOT to values < 1 nm for anneal temperatures up to 900 °C was observed with a TaN electrode. However, EOT is still determined to increase at higher anneal temperatures to undesired values and is shown to vary with anneal time, suggesting an undetermined source of oxygen in the gate stack or in the anneal environment.

Tungsten has been previously observed to be a source of oxygen when used as a gate metal in a W/HfO$_2$ gate stack design.[221] Upon annealing in a low pO$_2$ environment, an EOT

increase suggested that the W was a source of oxygen. The incorporation of oxygen in W is the subject of an interesting discussion in literature.[222,223] Tungsten films can be deposited in an equilibrium body centered cubic structure, α-W, or in a non-equilibrium cubic phase termed β-W (generally thought to be stabilized by a high-oxygen concentration, similar in structure to W_3O). The oxygen concentration in α-W can be as high as 12 at.% and as high as 14-19 at.% in β-W.[222] In this work, tungsten is used as an electrically conductive capping layer in a TaN/$LaSiO_x$/Si MOS capacitor device. The purity of the deposited tungsten phase as a function of deposition condition is examined before and after annealing to thermal budgets required for MOSFET source/drain activation. The affect of the oxygen concentration in the tungsten on EOT is presented.

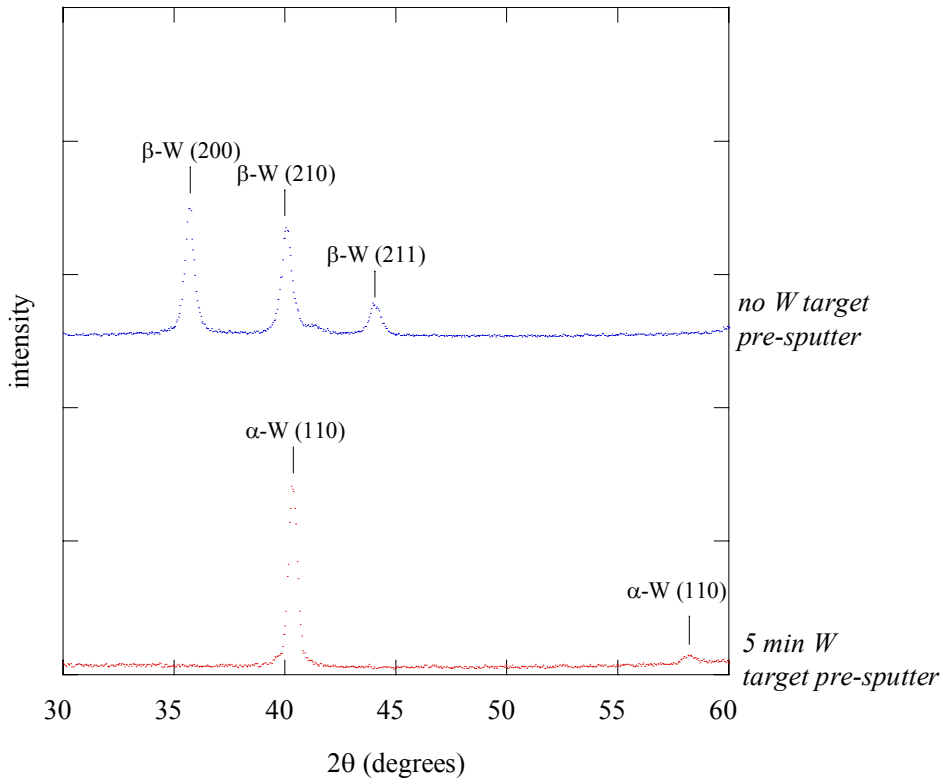


Figure 5.15: *XRD patterns of tungsten deposited on SiO_2 via DC magnetron sputtering with and without a 5 minute target pre-sputter.*

In order to determine the effect that the tungsten film quality has on the overall properties of the gate stack after annealing, the as-deposited films must first be characterized. The deposition of W on SiO_2 was first investigated by XRD, shown in **Fig. 5.15**. The resultant growth of W was determined to be in the non-equilibrium β-phase (or W_3O)[224] For continuity, the W films on TaN were grown simultaneously with the W films grown on SiO_2. In both cases, a β-W phase was observed. Upon annealing, a transformation from β-W to the equilibrium α-W occurs. The XRD of tungsten deposited on SiO_2 after a five minute pre-sputter is also shown in **Fig. 5.15**. In this case, the α-W phase was observed and remains stable after high-temperature annealing, suggesting a significantly lower concentration of oxygen in the thin film. It is noted that the pre-sputtered W on TaN gave conflicting results, producing α-W and β-W. Therefore, the XRD analysis of the oxygen concentration in W based on that grown on TaN is not sufficient evidence to predict a low concentration of oxygen in the pre-sputtered tungsten.

In addition to XRD, SIMS was used to analyze the relative concentrations of each species throughout the samples prior to *ex situ* annealing of the gate stack (50 nm W/50 nm TaN/$LaSiO_x$/Si). **Figure 5.16** shows the SIMS profiles for the gate stacks with tungsten that was pre-sputtered (solid line) and tungsten that was not pre-sputtered (dashed line). The oxygen profile has been highlighted. The pre-sputtered tungsten has a factor of 20 less oxygen than the deposited tungsten without the pre-sputter. An oxygen peak is also observed at the interface between W and TaN that is most likely due to air exposure of the TaN creating a thin oxide at the surface.

Figure 5.17 shows a HRTEM image of the TaN/W interface. The thin amorphous region at the interface does suggest that an oxide has formed. At this time the significance of high-oxygen concentration at W/TaN interface remains undetermined. Samples were then annealed at a temperature of 1000 °C for times ranging from 1-20 seconds. **Figure 5.18** shows a linear SIMS profile of the oxygen concentration in the gate stack before and after annealing. A 1000 °C, 10 sec anneal of the gate stack with low- oxygen concentration in the

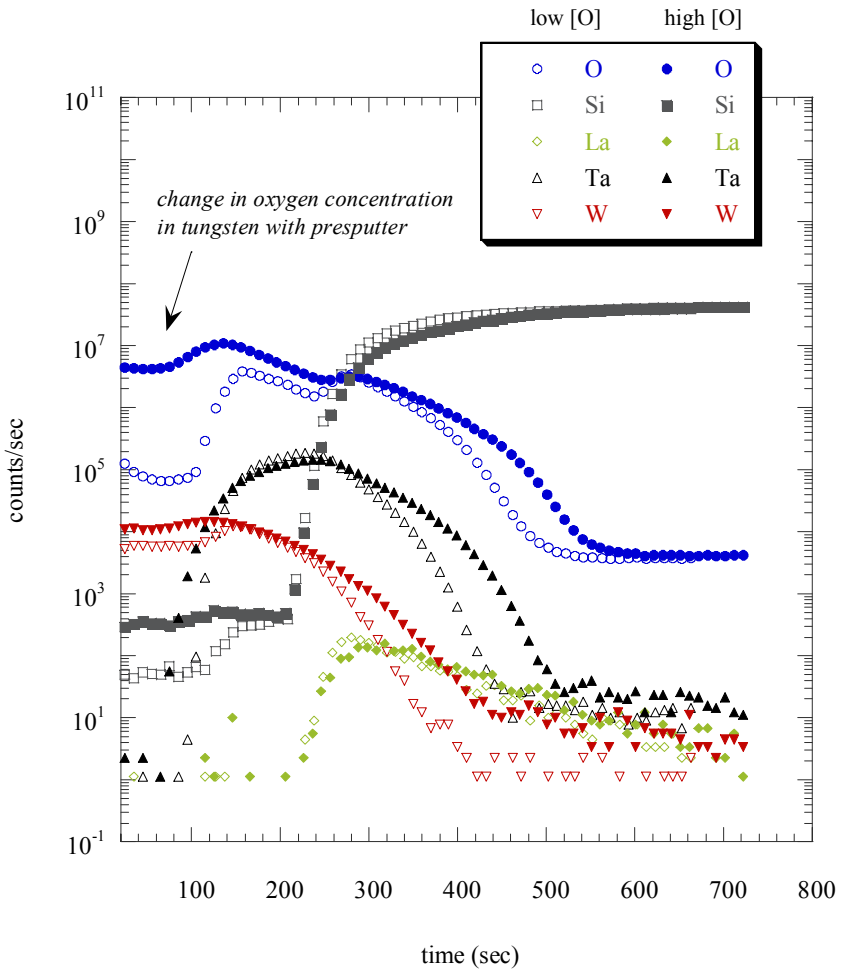


Figure 5.16: *SIMS profiles of W/TaN/LaSiO$_x$/Si gate stacks with and without a 5 minute W target pre-sputter.*

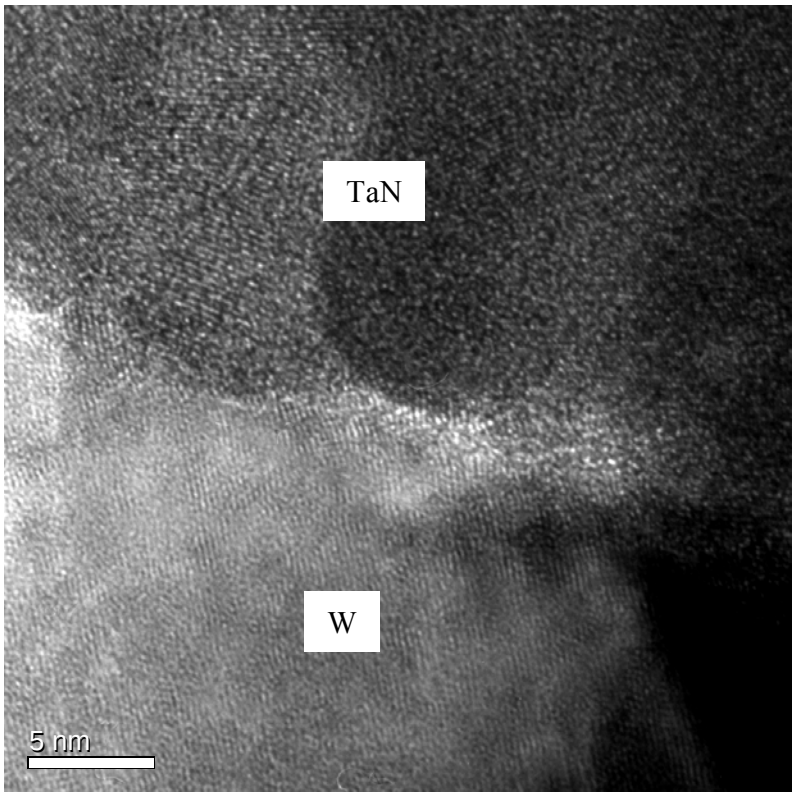


Figure 5.17: *HRTEM of the TaN/W interface prior to ex situ annealing. Tungsten deposited with low-oxygen concentration (pre-sputter).*

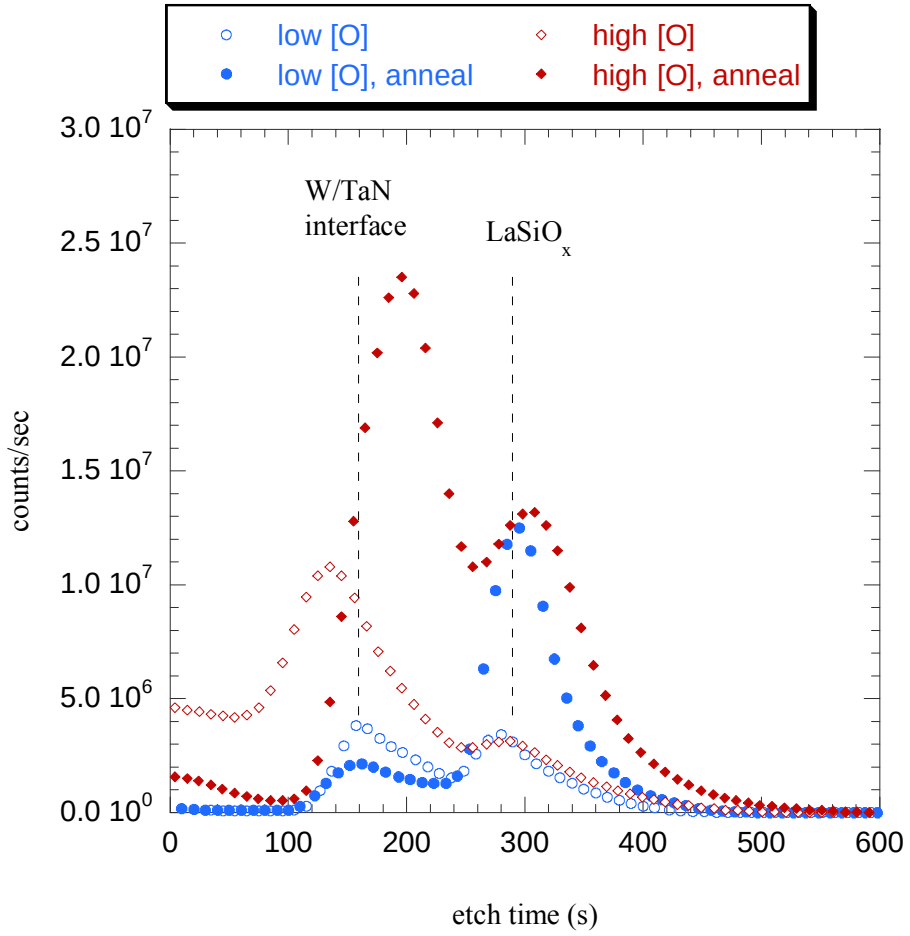


Figure 5.18: *SIMS profile of oxygen concentration throughout a W/TaN/LaSiO$_x$/Si gate stacks, with and without a 5 minute W target pre-sputter, before and after annealing at 1000 °C for 10 s.*

W (pre-sputtered) results in a change of oxygen concentration in the tungsten and at the W/TaN interface. The overall oxygen concentration in the dielectric increases, which is an indication that either the gate stack was initially under-oxidized or a SiO_2 interfacial layer is being formed. For the gate stack with high-oxygen concentration in the W, annealing results in a decrease in oxygen concentration of the tungsten and an increase in oxygen concentration at the W/TaN interface and in the dielectric. **Figure 5.19** shows a HRTEM image of the W/TaN interface consisting of an increased amorphous region. It is noted that the presence of Ta_2O_5 is expected since TaN is energetically favorable to the formation of an

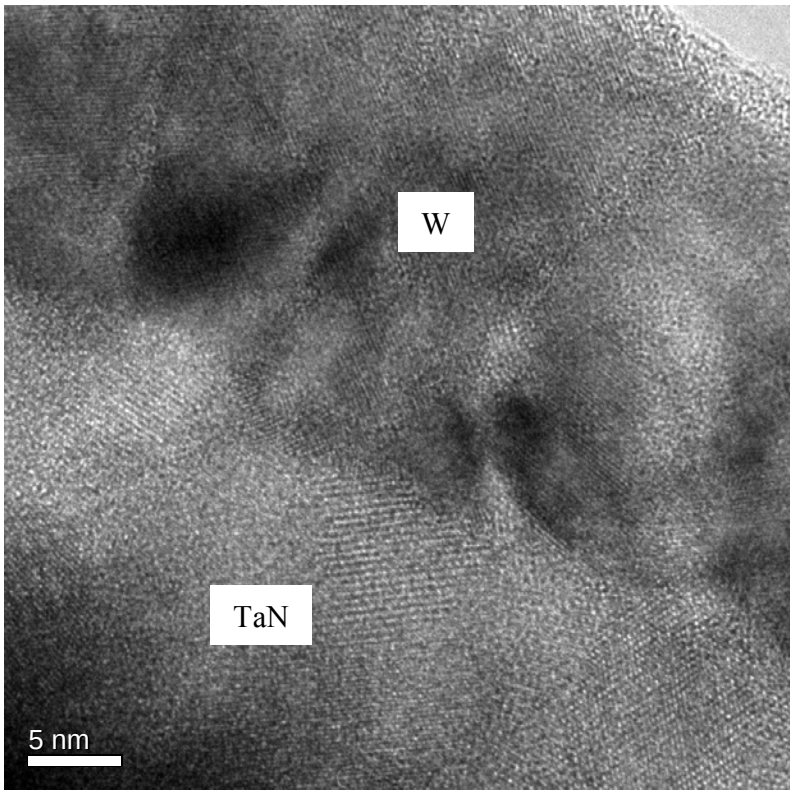


Figure 5.19: *HRTEM of the TaN/W interface prior after ex situ annealing at 1000 °C for 10 s in nitrogen. The tungsten was deposited with a low-oxygen concentration (pre-sputter).*

oxide in the presence of oxygen, therefore acting as an oxygen sink. The large post-annealing discrepancy in oxygen concentration for the low and high-oxygen concentration tungsten gate stacks is a sign that the tungsten condition should have a major effect on the properties of the film.

In **Figs. 5.20 (a)-(c)**, it is observed by HRTEM and HAADF-STEM that the thickness of the dielectric is enlarged with increased oxygen concentration in the tungsten after annealing. The thickness is observed to decrease from 30 Å to 22 Å by processing with the high-oxygen containing W with annealing at 1000 °C for 10 sec. Despite the high-temperature annealing, and amorphous nature of the film is retained from the *in situ* annealed state observed in **Fig.**

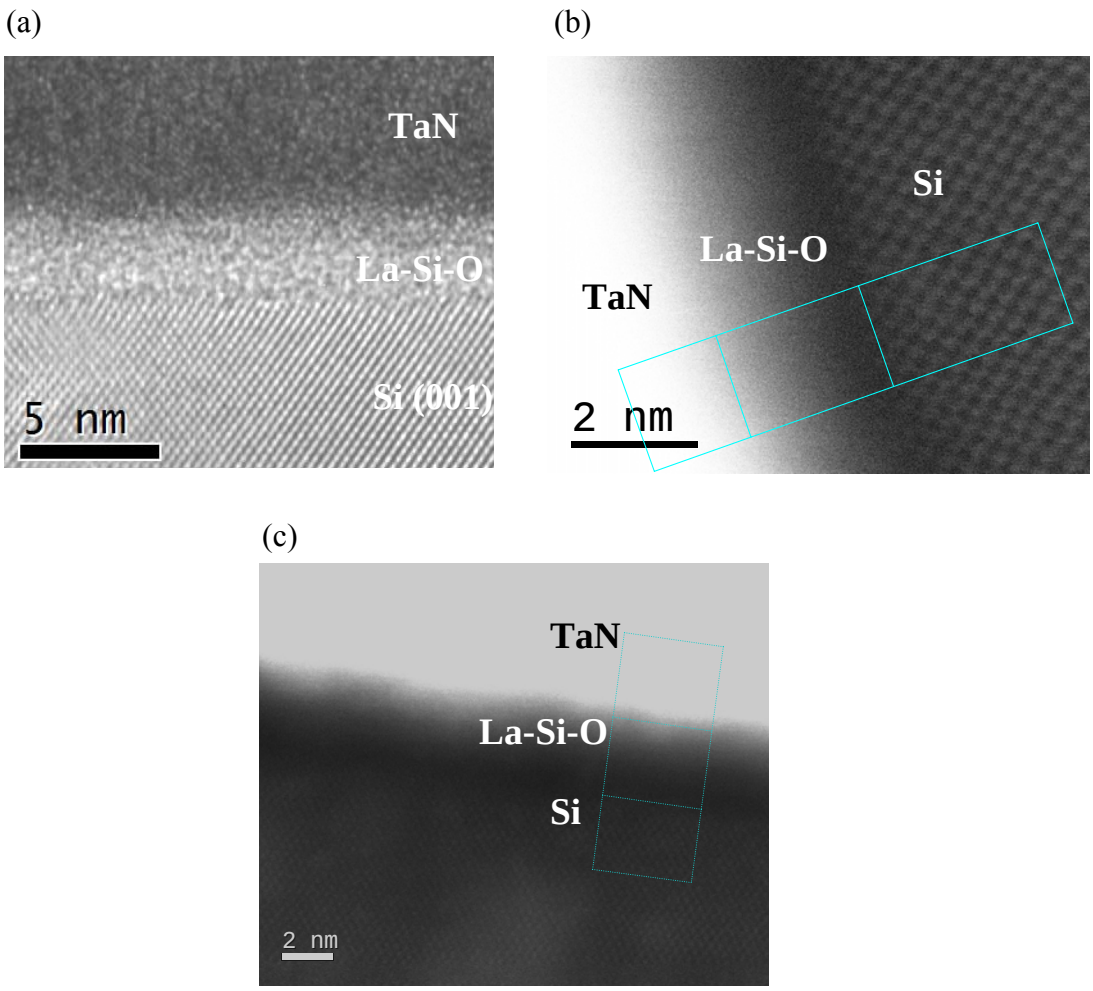


Figure 5.20: *HRTEM and HAADF-STEM of W/TaN/LaSiO$_x$/Si gate stacks after an ex situ annealing at 1000 °C for 10 s in nitrogen for (a), (b) low and (c) high-oxygen concentration W.*

4.10. The EOT extracted from the C-V measurements, also agree with the observation that the actual physical thickness is decreased by using low-oxygen containing tungsten during processing. **Figure 5.21** shows the variation of EOT as a function of anneal time at 1000 °C for the two tungsten capping layers. Observe that, with high-oxygen concentration in tungsten, the EOT increases with anneal time, whereas tungsten with low-oxygen concentration results in minimal EOT increase. An EOT as low as 11 Å is achieved after processing at 1000 °C for 10 s for the tungsten with low-oxygen concentration. The hysteresis is measured to be < 10 mV and the leakage current density is 0.035 A/cm^2 at a V_{FB}

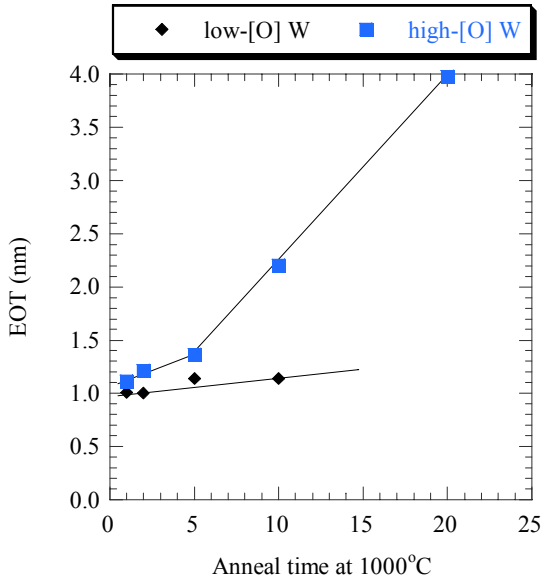


Figure 5.21: *EOT for W/TaN/LaSiO$_x$/Si MOS devices shown as a function of ex situ anneal time at a temperature 1000 °C in nitrogen. Data is shown for gate stack consisting of low and high-oxygen concentration tungsten. EOT extracted from C-V measurements using NCSU Hauser model.*

+ 1 V. The large increases in EOT is most probably due to the oxygen in the tungsten diffusing to the Si and reacting to form a SiO_2 interfacial layer, as SIMS would indicate. This is a reasonable conclusion since an oxygen concentration of < 5 at% (in 50 nm of W) is necessary for 30 Å of SiO_2 growth. Recall that upon annealing, the formation of Ta_2O_5 due to the reaction between oxygen and TaN is favored. The corresponding EOT increase in the presence of high-oxygen concentration in the tungsten is possibly due to a sufficient conversion of the TaN allowing increased oxygen diffusion to the silicon interface.

A modification to the processing flow was conducted to in order to observe the effect of annealing the gate stack prior to tungsten deposition (i.e. on a blanket TaN/LaSiO$_x$/Si gate stack) **Figures 5.22** and **5.23** shows the resultant EOT and V_{FB} variation with anneal time compared to previously reported data with a TaN electrode. By first comparing EOT data with the presence of low and high-oxygen concentration tungsten, it is observed that the TaN does not act as a sufficient barrier to the atomic oxygen that is incorporated in the W lattice. In comparing the case with no tungsten capping layer, the TaN acts as a sufficient barrier to

molecular oxygen from the anneal environment. It might be considered that tantalum nitride is more effectively reduced and reacted to form tantalum oxide in the presence of atomic oxygen as opposed to molecular oxygen. Nevertheless, the best results are observed with the TaN gate electrode working in concert with low-oxygen concentration tungsten. In this case the tungsten either acts as an appropriate diffusion barrier to molecular oxygen by either directly blocking the diffusion of oxygen or acts to retain the oxygen without allowing the oxygen to proceed through the TaN.

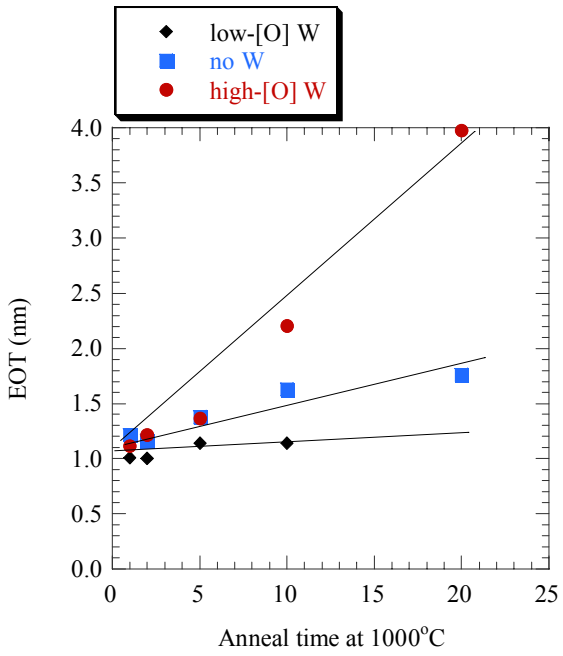


Figure 5.22: *EOT for W/TaN/LaSiO$_x$/Si MOS devices shown as a function of ex situ anneal time at a temperature 1000 °C in nitrogen. Data is shown for gate stacks annealed with no tungsten, as well as low and high-oxygen concentration tungsten. EOT extracted from C-V measurements using NCSU Hauser model.*

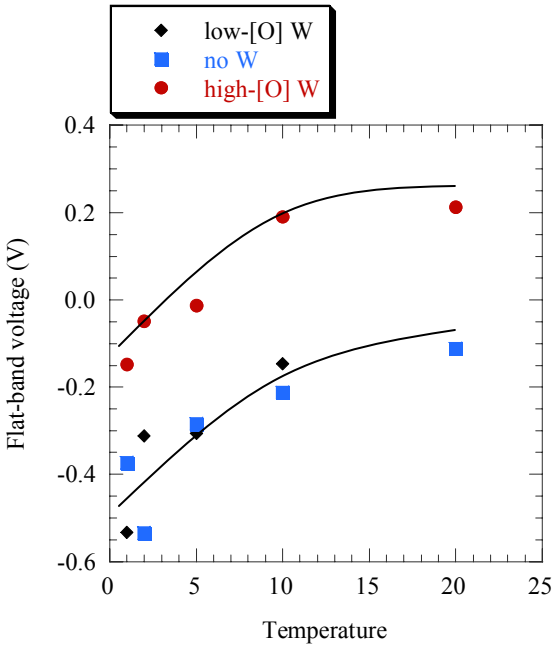


Figure 5.23: *V_{FB} for W/TaN/LaSiO$_x$/Si MOS devices shown as a function of ex situ anneal time at a temperature 1000 °C in nitrogen. Data is shown for gate stacks annealed with no tungsten, as well as low and high-oxygen concentration tungsten. V_{FB} extracted from C-V measurements using NCSU Hauser model.*

5.6 Stability of Lanthanum Silicate on Silicon

For a new high-κ dielectric to be introduced into current CMOS technology, it is well understood that the dielectric-substrate interface must have amongst other properties minimal defects, a thin low-κ interfacial region, and kinetic stability, as well as no diffusion of stack elements into the channel region of the device so as to cause carrier mobility degradation.[22,207] §5.4-5.6 discusses the optimization of the electrical properties of lanthanum silicate based MOS capacitors with a TaN electrode and W capping layer while enduring the high thermal budget (e.g. 1000 °C, 10 s) required for dopant activation in the source and drain regions. Yet undetermined, however, is the diffusion of lanthanum into the substrate.

The preference for metal diffusion from other lanthanum based high-κ materials into the Si substrate is well documented.[225,226,227] For $LaAlO_x$, silicate formation is still observed after

annealing, a condition attributed to Si penetration from the substrate.[226] Experimentally observed lanthanum and aluminum diffusion into the silicon was found to be related to the crystallization of the lanthanum aluminate.[227] The authors determined that lanthanum begins diffusing into the silicon substrate at an anneal temperature of 940 °C, which is also observed to be the point at which $LaAlO_x$ begins to show crystallization. A similar correlation between crystallization of the dielectric and the metal diffusion into the substrate has been shown for $ZrSiO_x$ on silicon.[228] These results suggest that the silicate formation at the interface does not necessarily prevent metal diffusion into the substrate. However, $HfSiO_x$, yields a conflicting result, credited to the spinodal decomposition to HfO_2 and an interfacial SiO_2 that prevents the Hf diffusion.[229]

To examine the potential for lanthanum diffusion into the silicon substrate, SIMS was utilized. However, the preferred front side directionality of the SIMS profiling, through the dielectric and into the substrate, is not optimum for determining the profile of a target metal atom when the region of interest is of low concentration, lying underneath a layer of high concentration. The so called "knock-on" effect can create a false impression of the metal atom diffusion into the layer of lower concentration beneath it. Thus, in this study the lanthanum diffusion into the substrate was monitored using a back-side SIMS approach that avoids the lanthanum "knock-on" effect observed in front side SIMS profiling.

Figure 5.24 shows the back-side SIMS profiling of the lanthanum-silicate/silicon-substrate gate stack before and after a 1000 °C, 10 second nitrogen anneal. From the SIMS profiles, ^{139}La does not diffuse into the substrate after annealing. The oxygen analysis at the substrate interface shows a higher oxygen concentration in the sample after the anneal. However, it is difficult to reach conclusions about the oxygen in the insulator layer. In addition, ^{181}Ta and ^{185}W were not observed in the substrate after annealing. This indicates that the thin dielectric is without high diffusion rate paths, such as grain boundaries, which could otherwise be created by crystallization of the dielectric. Preventing atomic diffusion of species from the gate dielectric and the gate metal is important for retaining the channel mobility of the MOSFET device.

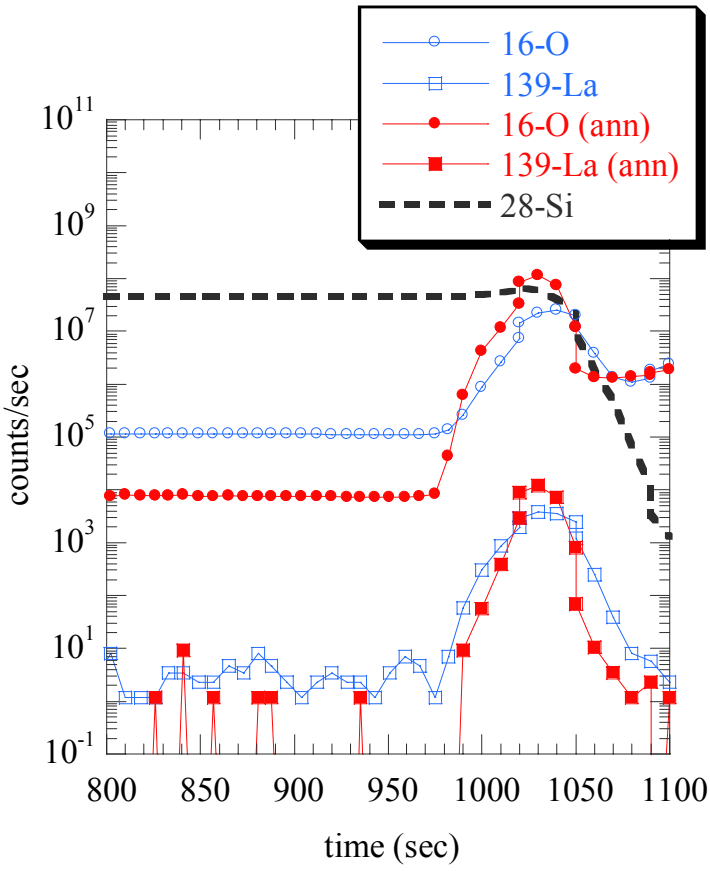


Figure 5.24: *Back-side SIMS profiles La, O and Si from a W/TaN/LaSiO$_x$/Si gate stacks before and after ex situ annealing at 1000 °C for 10 s in nitrogen.*

Recall that prior to the 1000 °C, 10 sec anneal, an EOT value as low as 0.5 nm has been reported (§4.3.2). After the high-temperature anneal, oxygen diffusion into the dielectric during the anneal appears to increase the EOT and also the physical thickness of the devices. It has been shown that interfacial SiO_x, if formed, reacts with the $LaSiO_x$ already present, resulting in a decreasing concentration of lanthanum toward the substrate interface. This process has been shown to occur with low-temperature – long-time processing (400 °C) and with high-temperatures – short time processing (1000 °C). Therefore, a SiO_x interfacial layer at the $LaSiO_x$ and silicon interface would not necessarily prevent lanthanum diffusion, as it may in the case of a $HfSiO_x$ system. In addition, by keeping the lanthanum in the silicate

matrix, the tendency for crystallization of the dielectric is reduced in comparison to La_2O_3 (see **Fig. 5.20 (a)**).

Reasons that lanthanum does not diffuse into the substrate under these conditions is most likely due to the initial low-temperature silicate formation, and the thermodynamic stability of the lanthanum silicate. Examining the respective phase diagrams (**Figs. 2.18** and **2.19**), lanthanum silicate, unlike hafnium silicate, does not have the tendency to decompose into MO_x and SiO_2 after a high-temperature anneal. Considering the glass forming nature of SiO_2, the amorphous phase of $LaSiO_x$ is able to be retained to a high-temperature.

5.7 Defect Analysis of Lanthanum Silicate on Silicon

The presence of defects in the dielectric can have substantial ramifications on the performance of the MOSFET device. A few of these defects can be monitored by measurement of the MOS capacitor. The two defect types considered in this section are interface traps and the fixed charges. Their affect on the MOS device, can be noticed in modeling of the gate voltage,[19]

$$V_G(\phi_s) = \left[\phi_s - \frac{Q_{SC}(\phi_s)}{C_{OX}}\right] + \left[\phi_{ms} - \frac{Q_{eff}}{C_{OX}}\right] + \left[\frac{Q_{IT}(\phi_s)}{C_{OX}}\right] \qquad \text{Equation (5.1)}$$

where, ϕ_s is the surface potential, ϕ_{ms} is the difference in the work function of the metal and semiconductor, C_{OX} is the oxide capacitance, Q_{SC} is the semiconductor charge, Q_{eff} is the effective fixed charge, and Q_{IT} is the interface trap charge. The first term in **Eqn. (5.1)** provides the ideal C-V curve that is based only on the charge of the semiconductor. The second terms represents a fixed value offset (independent of the surface potential). Fixed charges are present throughout the dielectric and can result in a large shift in the flat-band voltage. An example of fixed charge is the presence of oxygen vacancies that appear as positive charges the dielectric, which results in a negative shift in the flat-band voltage. Recall that a shift in the flat-band voltage is reflected on the MOSFET threshold voltage. In addition, it is noted that the polarity of the fixed charge results in similar shift for both p-type

and n-type MOS devices. That is, a positive fixed charge will result in a negative shift for an MOS device on n-type and p-type silicon.

The last term in **Eqn (5.1)** represents the influence of D_{IT} on the gate voltage. Note that D_{IT} is a function of applied surface potential. As the name suggest, the interface traps are predominantly located at the dielectric/silicon interface, such as silicon dangling bonds produced by imperfections in bonding coordination of the dielectric and silicon. A high density of interface traps can result in a phonon scattering that can decrease the maximum mobility in the MOSFET channel. D_{IT} levels > 10^{11} ev^{-1} cm^{-2} can result in such deterioration. Evidence of a high D_{IT} has been suggested previously in **§5.3** and **5.4** by the observation of an inflection in the C-V curves. There it is noted that the inflection is reduced after high-temperature annealing. Unfortunately, the NCSU Hauser model only allows for a smooth fitting of the C-V curve and thus, does not take into consideration the inflection observed when the capacitor nears depletion. The origin of the inflection is due to a lag in the interface trap response with an applied AC voltage at a sufficiently low frequency. This creates empty interface trap levels below the Fermi level. When a higher energy electron in silicon is captured by a lower energy interface trap state, loss occurs in the form of phonon scattering. The loss is read by the conductance curve in which a peak is observed based on the capture probability of the interface traps and the number of interface traps present. **Figure 5.25** shows the representative C-V measurement and G-V measurement for MOS devices on n-type and p-type silicon. A pMOS (with n-type silicon), a low (or (-) voltage) results in no electron trapping. As V_G is increased, electrons are pulled from the silicon and begin to fill the interface traps. On the reverse sweep, the traps are emptied. Note that for an nMOS device (with p-type silicon), the inflection is not observed since positive charges appear as an additional V_{FB} shift.

A useful method to evaluate interface trap density, D_{IT}, from conductance measurements is the often used conductance method, described in more detail in **§3.2.3**. Note that the use of the conductance method does not depend on the work function of the metal. This is quite important considering the possible variation of the work function. **Figure 5.26** shows the D_{IT}

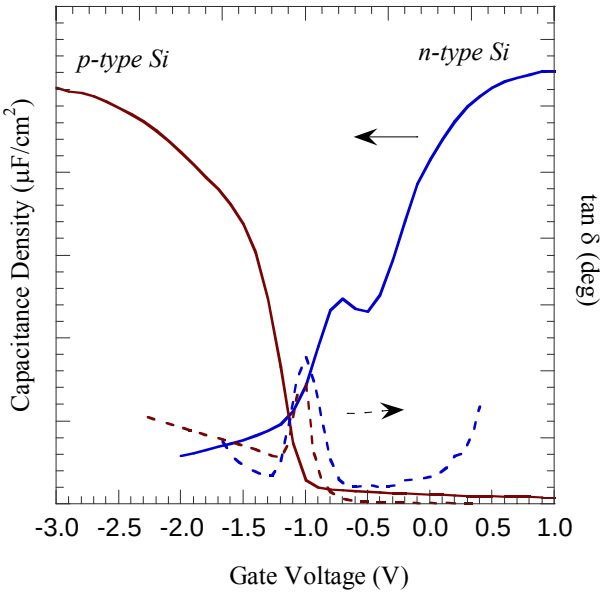


Figure 5.25: *Representative C-V (solid) and G-V (dashed) measurements showing the effect of interface traps on each respective curve for MOS devices on n-type and p-type silicon.*

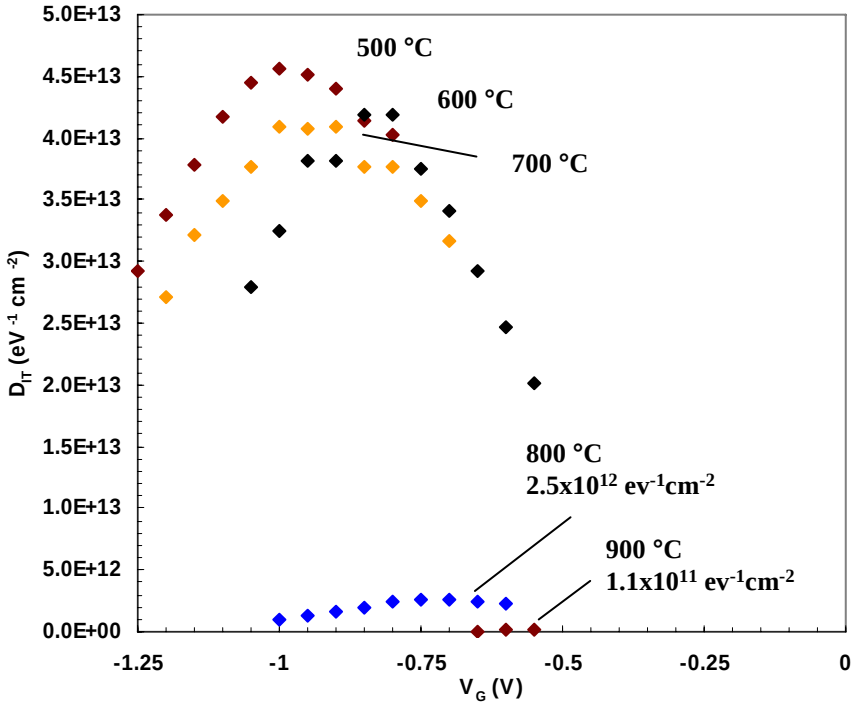


Figure 5.26: *D_{IT} plotted as a function of gate voltage for a W/Ta/$LaSiO_x$/Si MOS devices annealed at temperatures of 500 - 900 °C for 10 s in nitrogen.*

as a function of gate voltage for a W/Ta/$LaSiO_x$/Si gate stack annealed between temperatures of 500 and 900 °C for 10 sec in nitrogen. The D_{IT} values are observed to decrease substantially as the anneal temperature is increased. For samples with a TaN electrode capped with high-oxygen concentration in the W, D_{IT} decreased with anneal time increase at 1000 °C. D_{IT} concentrations decreased from $1x10^{12}$ $cm^{-2}eV^{-1}$ for a 1 second anneal to $1.5x10^{11}$ $cm^{-2}eV^{-1}$ after a 10 second anneal. For samples with low-oxygen concentration in the tungsten, D_{IT} values were ~$2.5x10^{13}$ $cm^{-2}eV^{-1}$, independent of anneal time. As might be expected, the SiO_2 growth at the dielectric/silicon interface creates an optimal interface with low defect densities. However, this occurs at the expense of the EOT. Further investigation is needed to attempt a reduction in defects while not increasing the EOT.

From **Fig. 5.11**, a positive shift in the flat-band voltage is observed to voltages that correlate with the ideal flat-band voltage (which is based on a proposed metal work function). It is important to point out that the NCSU Hauser model assumes a constant work function of the metal to evaluate the effective fixed charge as the change of the flat-band voltage with respect to the ideal flat-band voltage. In reality, the flat-band voltage is more likely to be shifted negatively. This would be expected of a high-κ dielectric that has a high density of positive charges, as is observed in most high-κ dielectrics. Considering this, the positive fixed charge is observed to be decreased with anneal temperature and is increased for the MOS gate stack with a Ta electrode that has higher EOT growth. From **Fig. 5.23**, the effect of oxygen on the flat-band voltage shift of TaN-based MOS gate stacks is very apparent. The sample annealed with the high-oxygen concentration tungsten results in a positive shift compared to the gate stack annealed that had ideal oxygen diffusion. Considering that the metal work function is expected to be consistent with all processing data sets, work function variation can not explain the observed shift. These results imply that the oxygen vacancies are being filled when oxygen is available to the dielectric. However, it is apparent from recent results (presented in **Chapter 6**) that oxygen vacancies alone cannot explain such magnitudes of shifting. Instead the possibility of a dipole formation or strain formation by the intermixing of the lanthanum silicate is examined.

5.8 Conclusions

While the inclusion of the high-κ gate dielectric into a MOS gate stack has an obvious benefit, the surrounding material must be optimized prior to passing judgment on the performance of the gate dielectric. This is exactly the case observed in this chapter. Only after a thermally stable TaN was used in concert with a high purity tungsten capping layer did the benefit of the lanthanum silicate gate dielectric appear. After high-temperature annealing, consistent with that required for the source/drain activation anneal of standard MOSFET processing, the MOS device showed the ability to retain an EOT of 1.1 nm and a leakage current density of 0.035 A/cm^2. Even though the EOT is increased in comparison to the as-deposited dielectric after the *in situ* anneal, the leakage is considerable less than that of SiO_2 at such a thickness (> 100 A/cm^2).

In the processing optimization of the MOS gate stack, diffusion barrier properties of the TaN were analyzed. It was observed that the diffusion resistance of TaN to molecular oxygen is much greater than that with respect to atomic oxygen. This resistance to both can be enhanced/resolved by the use of a W capping layer, which also serves to enhance electrical contact. A defect analysis was considered based on the interface trap density and the fixed charge of the dielectric. It was observed that the oxygen diffusion allowed by Ta and by TaN results in a decrease in the defect levels. D_{IT} and fixed charges are reduced by the growth of SiO_2 at the interface and filling of oxygen vacancies, respectively.

The thermal stability of the lanthanum silicate in the optimized gate stack was examined by use of a back-side SIMS analysis. This analysis procedure was chosen since it has the ability to provided detailed information of the dielectric/semiconductor interface by avoiding the knock-in effect observed by profiling from the W to the substrate. No diffusion of lanthanum into the substrate was observed and it is probable that the amorphous nature of the dielectric prevents the diffusion.

6. EFFECTIVE WORK FUNCTION CONTROL USING LANTHANUM OXIDE INCORPORATION

6.1 Introduction

The introduction of high-κ dielectric material in the metal-oxide-semiconductor field effect transistors (MOSFET) gate stack design provides a technique to reduce the high leakage current resulting from the thinning of the SiO(N) dielectric currently being used.[22,25] In addition, a replacement of the poly-silicon gate electrode with a metal electrode serves to decrease the electrical thickness even further. While much progress has been made towards developing a suitable high-κ dielectric replacement, issues with developing appropriate gate metals with work functions such that the device threshold voltage, V_T, meets both band-edges of silicon (for CMOS devices) has been difficult, especially for thermally stable metal nitrides that have a mid-gap work function. In addition, nitride and silicide alloys have properties which can vary significantly with processing.[32]

New research has been focused on manipulating the gate stack in order to achieve desired V_T values through an *effective* work function shift, $\phi_{m,eff}$, of the gate metal by sandwiching an additional ultra-thin high-κ dielectric layer between the gate dielectric and gate metal.[42,43,230] For example, a TaN/LaO_x/$HfSiO_x$/SiO_2/Si gate stack has been shown to yield MOSFET devices with a V_T that is consistent with an effective work function of 4.0 eV, ideal for n-channel MOS (nMOS) devices.[42]

A natural progression of the gate stack design, meeting the requirements of increased capacitance while maintaining low leakage characteristics, would include continual thinning of the Hf-based dielectric interlayer, potentially leading to its complete removal. In this situation the dielectric would be a LaO_x:SiO_x reacted bi-layer. In this regard, the benefit of $LaSiO_x$ is explored in comparison to the alternate $HfSiO_x$-based gate stack design and initial steps in realizing the control over the effective work function is explored.

6.2 Mechanisms for Work Function Control

The affect of the metal work function, or gate stack's effective work function, alteration is examined by the use of band diagrams and corresponding capacitance-voltage measurements in **Figs. 6.1 (a)-(f)**. **Figure 6.1 (a)** shows the Schottky model for a MOS structure with an n-type Si (complete diagram is shown in **Fig. 2.11 (b)**). According to the Schottky model, the Fermi level of the metal is aligned to the Fermi level of the Si, defined by the majority carrier doping. For such a structure, a metal work function of 4.1 eV is ideal to preserve a flat-band voltage of 0 V, as shown in **Fig. 6.1 (b)**. If $\phi_M > 4.1$ eV, a field is formed across the oxide, which must be compensated by a magnitude ΔV to re-cover V_{FB}. Even with an ideal work function metal, a field can be intrinsically formed within the oxide by either a distributed charge or a localized charge. For example, the case of the distributed charge within the confines of the dielectric is shown in **Fig. 6.1 (c)**. In this scenario, positive charges in the oxide, with a field equivalent to ΔV, result in a shift of V_{FB} to a more positive voltage (**Fig. 6.1 (d)**). In essence, the work function of the metal appears to be altered to an effective value, dependant on the entire MOS gate stack. A similar result is observed for the case of a localized charge state at the oxide-metal interface, shown in **Figs. 6.1 (e) and (f)**. Again, the resultant V_{FB} and $\phi_{M,eff}$ is altered by a magnitude ΔV.

Based on the analysis of the band diagrams, a number of mechanisms have been proposed in literature, which broadly can be divided into the categories of 'distributed' and 'localized' charges. In terms of distributed charges, the most prevalent in the case of high-κ dielectrics may be oxygen vacancies, which can serve as positively charged donors.[231] For multilayer stacks, these charges may be disproportionate among the different layers. A localized charge layer can also exist via an interface dipole that is created between layers of different material compositions.[42,43,230,231,232,233] As an example, consider the previously mentioned gate stack design. The mechanism by which the lanthanum oxide affects the dielectric is shown in **Fig. 6.2**. After a high-temperature anneal it has been proposed that the lanthanide cation (La) has

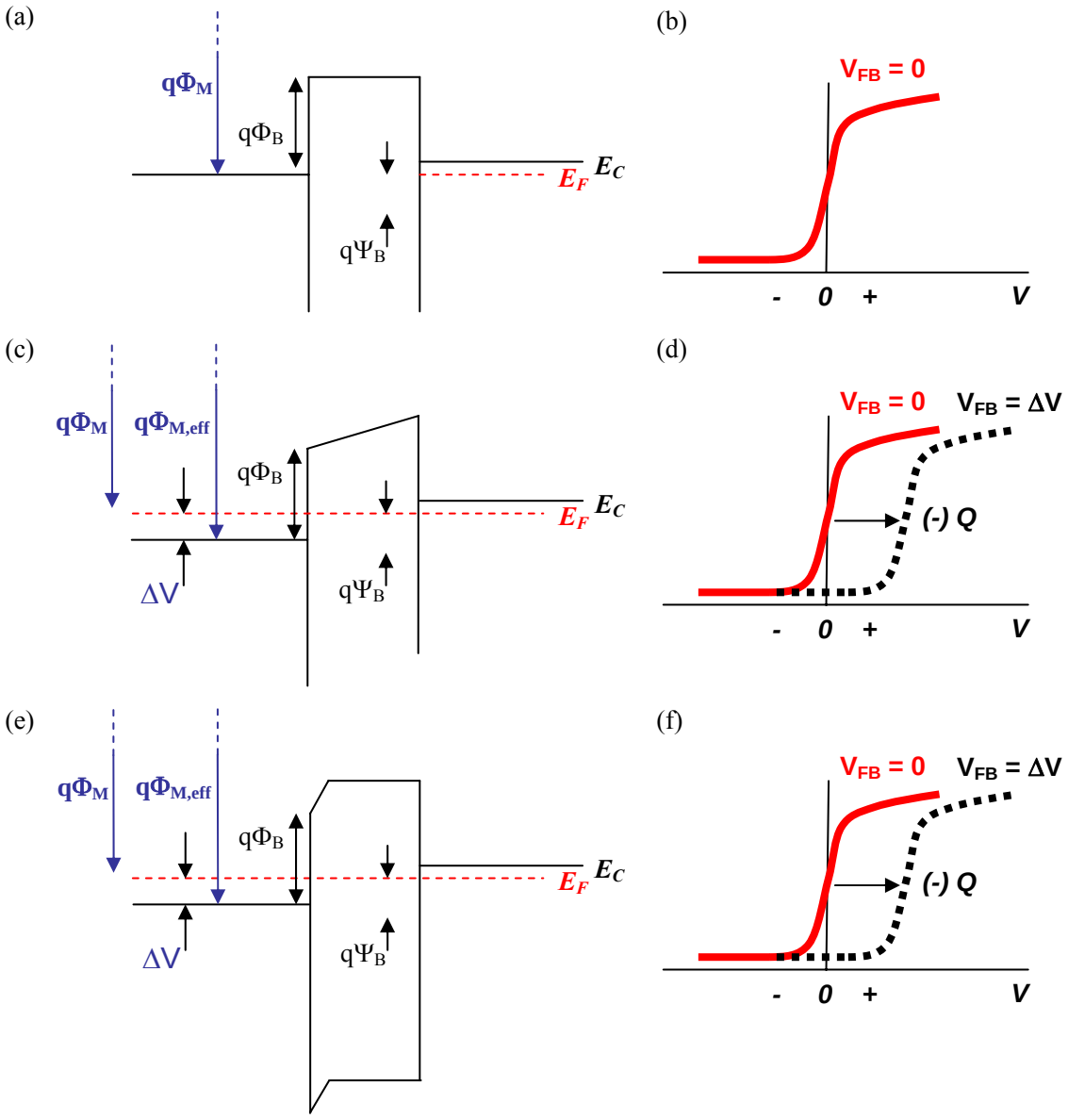


Figure 6.1: *Band diagram and representative C-V measurement for MOS structure with (a),(b) ideal ϕ_M for n-type Si, (c),(d) distributed charge within the oxide, and (e), (f) localized charge at the oxide-metal interface.*

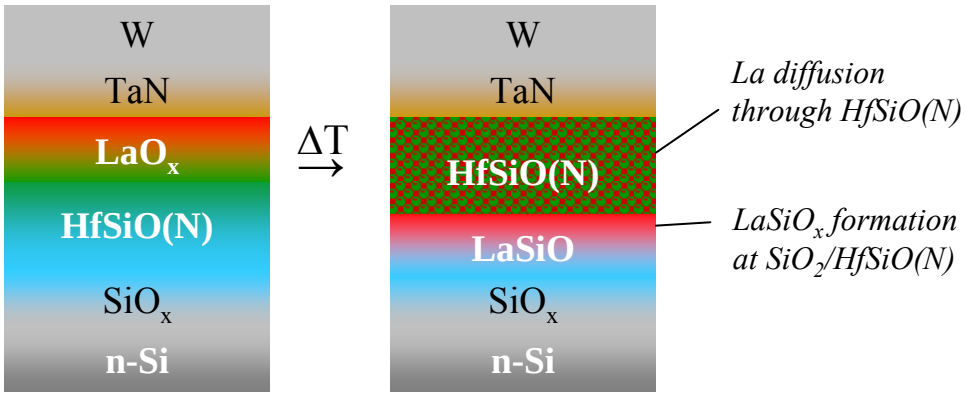


Figure 6.2: *Mechanism by which lanthanum is proposed to incorporate after annealing of a La_2O_3/HfSiO(N)/SiO_2/Si gate stack. Adapted from Al-Shareef et al.*[42]

diffused throughout the HfSiO layer and reacts to form a silicate at the interface between the $HfSiO_x$ and SiO_x. A total dipole moment associated with the interface between a lanthanide-containing silicate and the SiO_x layer, displayed in **Fig. 6.3**, can be defined based on thermodynamic, electronegativity, and ionic radius differences.[232] Similarly, an interface dipole has been proposed at the metal-dielectric interface that follows the principles of the generalized charge neutrality (GCNL) theory.[231,233] An interface dipole could also be due to the mechanical bond strain associated with the heterovalent interface bonding.[234] The result is a localized fixed charge at the internal dielectric/dielectric interface can have a magnitude

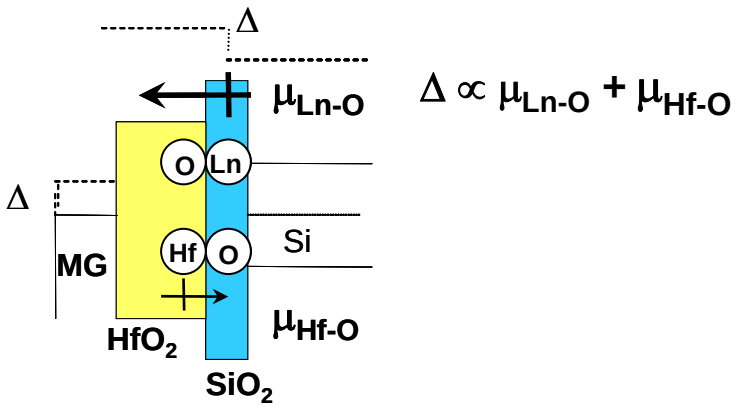


Figure 6.3: *Formation of an interface dipole at the HfO_2 and lanthanide silicate internal dielectric interface proposed to alter the effective work function of a gate stack. Adapted from Sivasubramani et al.* [232]

as high as 10^{12} cm^{-2} and is difficult to improve for high-κ silicates that have congruent melting points, such as La and Y-silicates. Regardless of the cause, this interface dipole results in a shift in the band offset at an interface, and is electrically observed as a positive or negative internal field.

6.3 Process Definition

6.3.1 Experimental

HfSiO and HfSiON dielectrics obtained from SEMATECH were used in order to study the effects of a lanthanum oxide capping layer on the $\phi_{m,eff}$ values. A similar stack design as that shown in **Fig. 6.2** is considered. The gate stacks consisted of HfSiO (20% SiO_2) and HfSiON (20% SiO_2, 15% N) films with a thickness of 15 Å and 25 Å on a 10 Å thermal oxide on p-type Si(001) substrates. On these stacks, a 5 Å capping layer of lanthanum oxide was deposited by molecular beam deposition of lanthanum in a pO_2 of $1x10^{-6}$ Torr at a deposition rate of 0.05 Å/s and a substrate temperature of 200 °C. Additional comparison was made with alternate lanthanide of dysprosium, holmium and ytterbium. The oxides of these lanthanides were deposited at similar conditions to the lanthanum oxide (pO_2 of $1x10^{-6}$ Torr, 200 °C), courtesy of the Electroceramic Thin Film Group at NCSU.

To investigate $LaSiO_x$ without the HfSiO interlayer, the silicate dielectric was formed by an *in situ* anneal serving to react the deposited lanthanum oxide with a silica chemical oxide in a controlled oxygen environment. Prior to lanthanum oxide deposition, n-type Si(001) substrates were prepared with a chemical oxide using the RCA clean process. Lanthanum oxide films with a thickness of 10 Å were deposited using the same conditions described previously. To promote the reaction between the lanthanum oxide and the silica, the substrate was heated *in situ* to 500 °C for 30 minutes while maintaining a pO_2 of $1x10^{-6}$ Torr. Variations of the process route, shown in **Fig. 6.4**, included either a room temperature five minute ozone exposure of the chemical oxide silica, or a 700 °C, 30 minute ammonia anneal prior to the lanthanum oxide deposition. Following all dielectric processing, a TaN gate

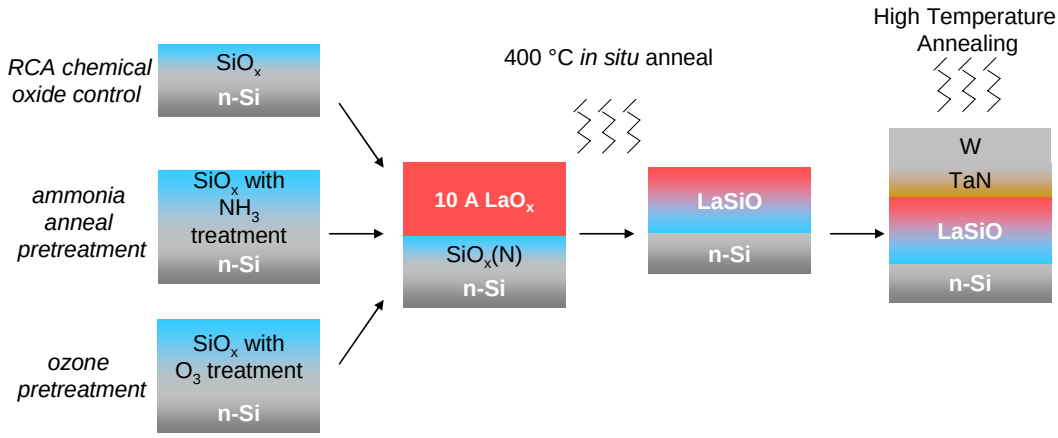


Figure 6.4: *Experimental processing outline for MOS devices consisting of the control SiO_2 chemical oxide and alterations to the chemical oxide including ozone and ammonia anneal pretreatments.*

electrode and W capping layer were deposited by DC magnetron sputtering through a shadow mask to form MOS capacitors. The gate stacks were annealed in a nitrogen atmosphere at temperatures of 700-1000 °C for 5-10 seconds. To evaluate the MOS devices, electrical measurements such as capacitance-voltage (C-V) and gate leakage-voltage (J-V) were conducted using HP 4192A impedance analyzer and HP 4145A semiconductor parameter analyzer probe stations, respectively. Equivalent oxide thickness, EOT, and flat-band voltage, V_{FB}, are extracted from the C-V measurements using the NCSU Hauser model. X-ray photoelectron spectroscopy (XPS) was conducted to analyze the lanthanum silicate formation after the *in situ* anneal and after *ex situ* RTA. High resolution transmission electron microscopy (HRTEM) and high-angle annular dark field imaging by scanning transmission electron microscopy (HAADF-STEM) was conducted by to analyze the stacks before and after annealing. In addition, back-side secondary ion mass spectroscopy was used to examined the diffusion of the lanthanide cations into the silicon substrate.

6.4 Lanthanide Capping of Hafnium-Based Dielectrics

To examine evolution of lanthanum's influence on $HfSiO/SiO_2$ and $HfSiON/SiO_2$ gate stacks, each structure was annealed at temperatures of 400, 700 and 1000 °C for 10 sec in N_2. **Figures 6.5** and **6.6** show the C-V curves obtained for $HfSiO/SiO_2$ bi-layers without and with

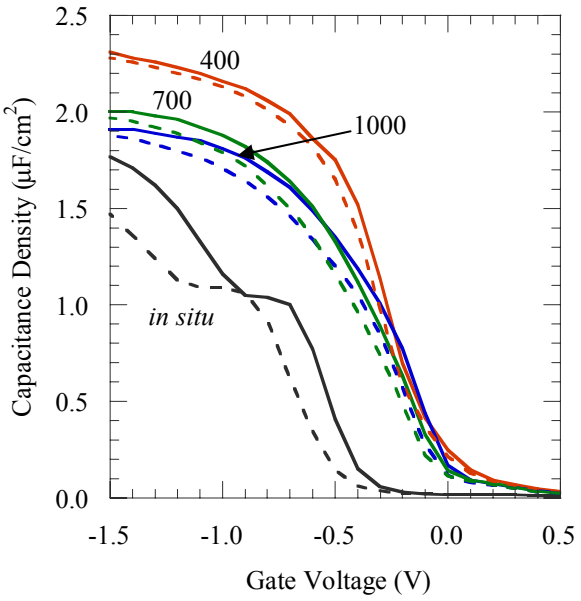


Figure 6.5: *C-V measurements for un-annealed and annealed TaN/HfSiO/SiO$_x$/Si MOS devices capacitor structures. Solid line represents (+) → (-) voltage sweep. Dashed line represents (-) → (+) voltage sweep. C-V characteristics measured at 100 kHz.*

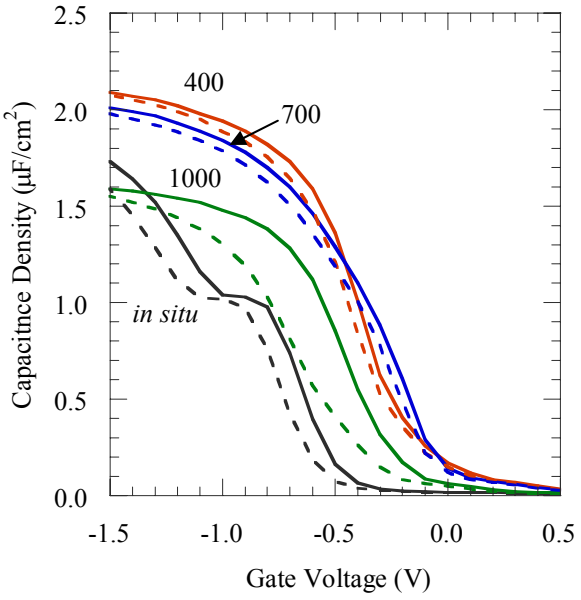


Figure 6.6: *C-V measurements for un-annealed and annealed TaN/LaO$_x$/HfSiO/SiO$_x$/Si MOS devices capacitor structures. Solid line represents (+) → (-) voltage sweep. Dashed line represents (-) → (+) voltage sweep. C-V characteristics measured at 100 kHz.*

a lanthanum oxide capping layer, respectively. In the samples processed, there exists an initial positive V_{FB} shift after a low-temperature (400 °C) anneal, possibly due to a charge reduction associated with annealing the lanthana-capped dielectric, and/or an increase in the work function of the TaN gate electrode with annealing. As shown in **§5.4**, x-ray diffraction of the metal electrode and tungsten electrode has shown that the cubic TaN phase persists with annealing, although the work function of TaN has been shown in the literature to vary between 3.8 and 4.7 eV, based on nitrogen content.[209,215] After higher temperature annealing, a negative shift is observed in lanthanum capped HfSiO (**Fig. 6.6**), whereas virtually no shift is observed in the HfSiO without lanthanum capping (**Fig. 6.5**). **Figure 6.7** shows the V_{FB} as a function of anneal temperature for the HfSiO and HfSiON gate stacks with and without the lanthanum oxide capping layer, from the data in **Figs. 6.5** and **6.6**. The difference represents the affect that the lanthanum oxide capping layer has on the flat-band voltage at a given anneal temperature. A negative V_{FB} shift is observed in the lanthanum oxide capped samples relative to the control samples as the anneal temperature is increased above 400 °C. After a 1000 °C, 5 s anneal, the negative voltage shift due to lanthanum with a HfSiO and HfSiON dielectric interlayer is -184 mV and -122 mV, respectively. It is noted that the EOT values, extracted using the NCSU Hauser model, are 1.35 nm and 1.25 nm for the uncapped HfSiO and HfSiON gate stacks, respectively. The addition of a 15 Å lanthanum oxide capping layer results in a minimal (< 5 Å) increase in EOT.

The gate stack consisting of lanthanum oxide capping on the HfSiON dielectric layer is analyzed by HRTEM and HAADF-STEM, shown in **Figs. 6.8 (a)** and **(b)**. The HRTEM shows evidence that the dielectric is amorphous and that the multiple layers are present in the dielectric. From HAADF-STEM imaging, **Fig. 6.8 (b)**, and an observation of the respective intensity distribution throughout the stack (shown as an inset in **Fig. 6.8 (b)**), there is a clear identification of the layer thicknesses as 11 Å SiO_2/15 Å HfSiON/15 Å La_2O_3 (error of ± 0.1 nm). Annealing the stack at a temperature as low as 400 °C for 5 s (HRTEM and HAADF-STEM shown in **Figs. 6.9 (a)** and **(b)**) results in some change to the dielectric stack. At this point the thicknesses are reported to be 13 Å SiO_2/13 Å HfSiON/14 Å La_2O_3 (error of ± 0.1 nm). The slight increase in SiO_2 thickness

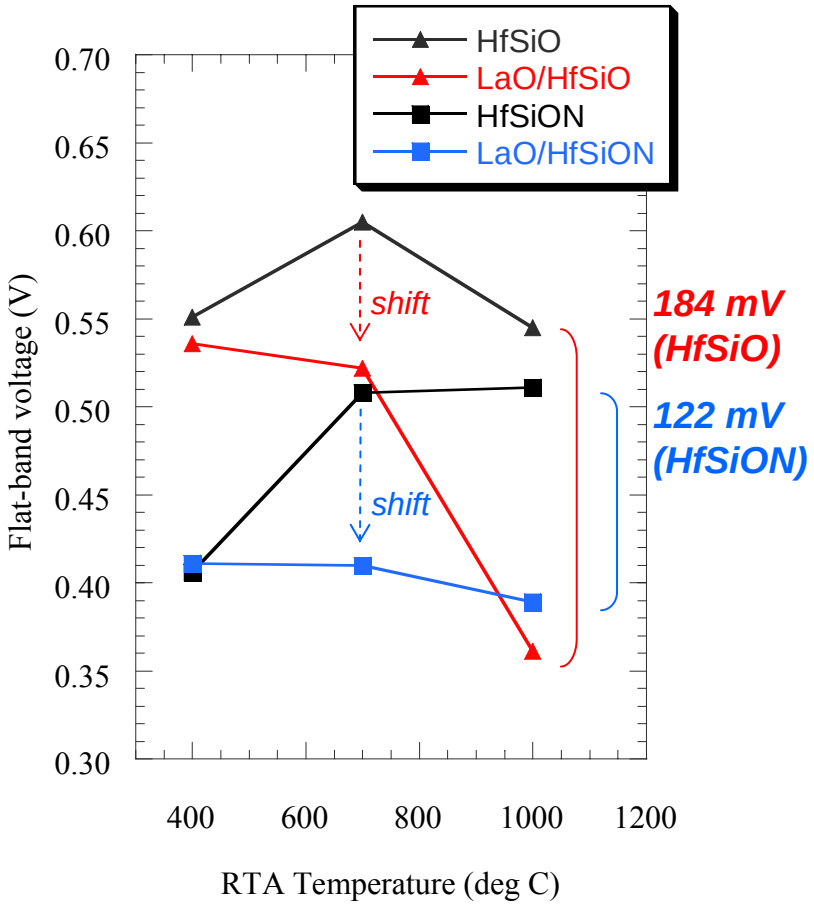


Figure 6.7: *V_{FB} shift for un-annealed and annealed HfSiO and HfSiON-based MOS devices with and without a LaO_x capping layer. Ex situ annealing was conducted for 5 sec in N_2. V_{FB} extracted from C-V measurement using NCSU Hauser model.*

might be expected from residual oxygen in the gate stack resulting in SiO_2 growth. The possible reduction in the lanthanum oxide and HfSiON thickness might indicate some intermixing with SiO_2, although this is most likely a result of densification in the respective dielectric layers. After 1000 °C, 5 s annealing HRTEM and HAADF-STEM, shown in **Figs. 6.10 (a)** and **(b)**, results in a relatively undefined high-κ dielectric layer. The thickness of the stack is now shown to be 14 Å SiO_2/28 Å Hf(La)SiON (error of ± 0.1 nm). While the SiO_2 layer is still apparent, these results neither confirm nor deny the presence of lanthanum in the SiO_2 interfacial layer. However, considering that the EOT value is ~1.4 nm for the

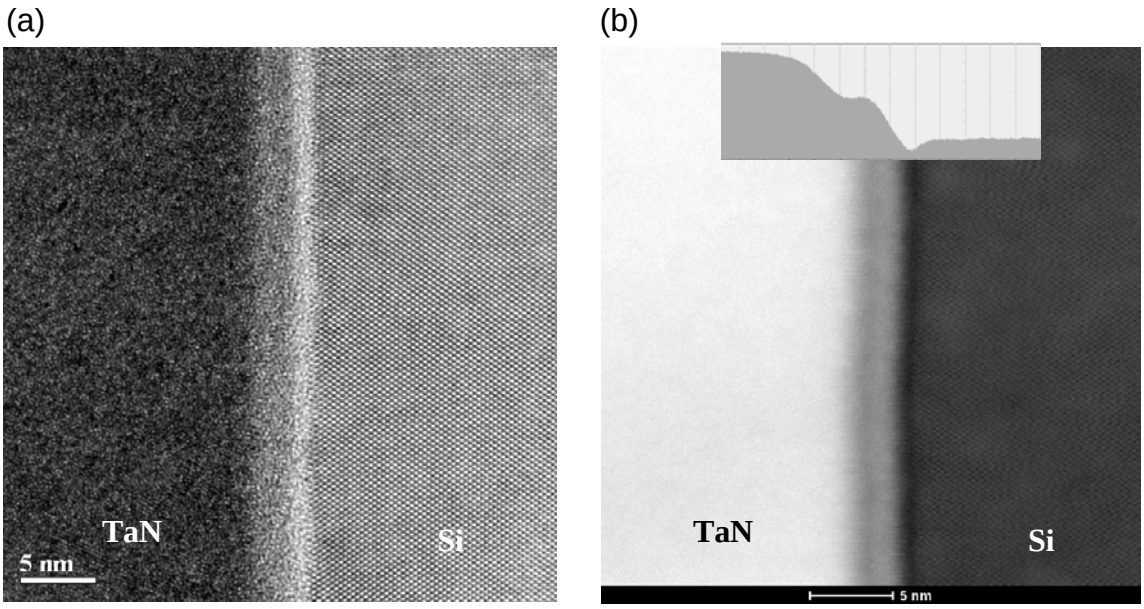


Figure 6.8: **(a)** *HRTEM and* **(b)** *HAADF-STEM of the W/TaN/La_2O_3/ HfSiON/SiO_2/Si gate stack prior to annealing.*

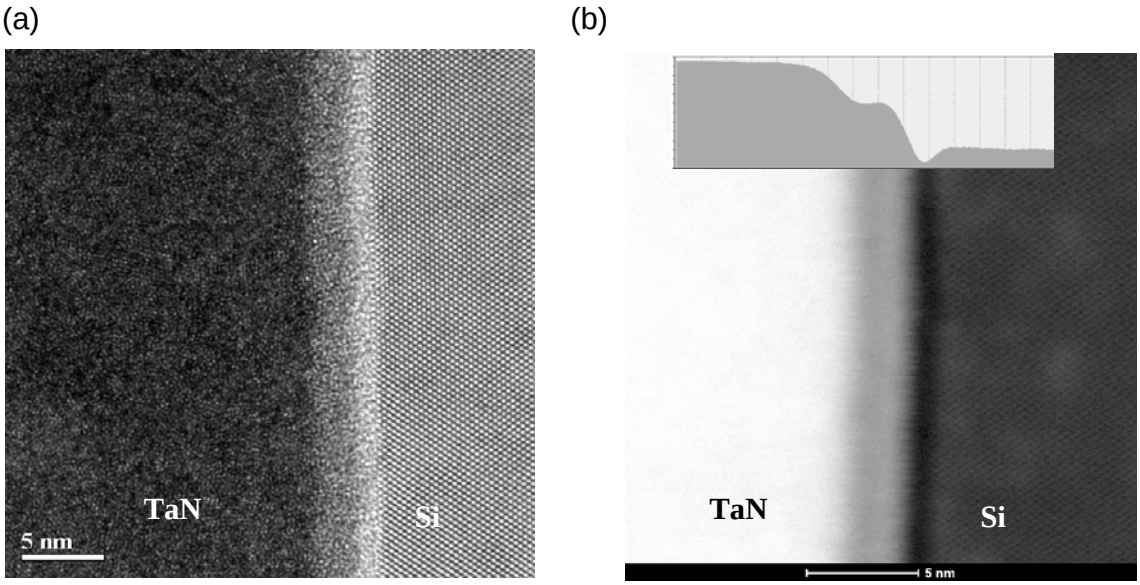


Figure 6.9: **(a)** *HRTEM and* **(b)** *HAADF-STEM of the W/TaN/La_2O_3/ HfSiON/SiO_2/Si gate stack after ex situ annealing of 400 °C for 5 s.*

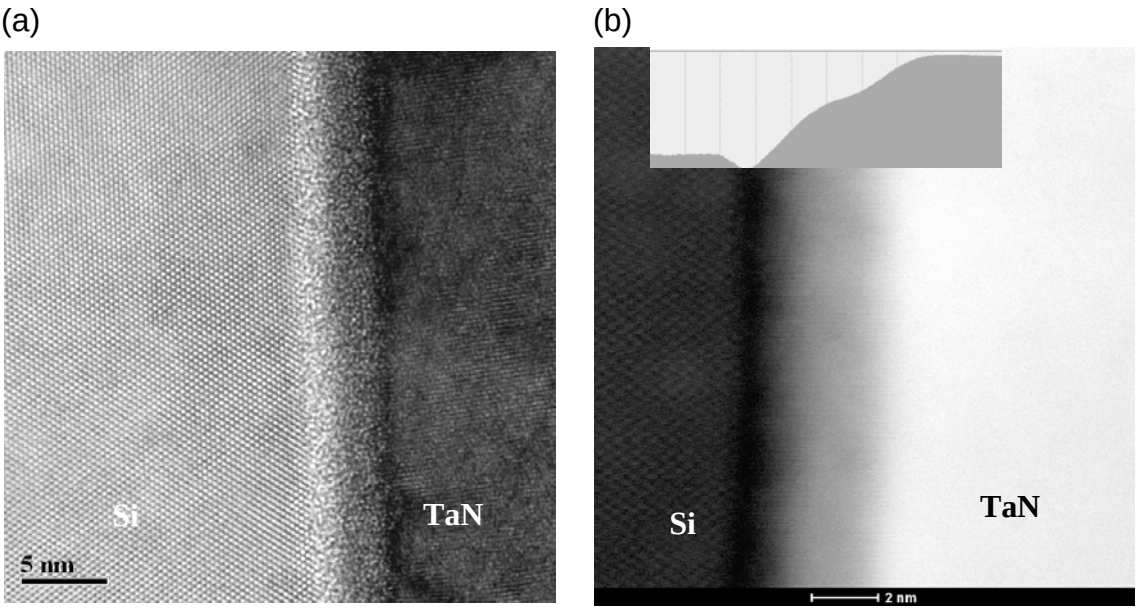


Figure 6.10: **(a)** *HRTEM and* **(b)** *HAADF-STEM of the W/TaN/La_2O_3/HfSiON/SiO_2/Si gate stack after ex situ annealing of 400 °C for 5 s.*

lanthanum capped HfSiON stack after a 1000 °C, 5 sec anneal, some intermixing is believed to be occurring.

For hafnia-based dielectrics, a negative V_{FB} shift is shown to be created by the presence of a lanthanum oxide capping layer on HfSiO and HfSiON dielectrics on SiO_2. The comparative V_{FB} shift between the dielectric with and without lanthanum oxide cap (**Fig. 6.7**) increases with an increase in anneal temperature. This is consistent with reports of diffusion of lanthanum toward the substrate, resulting in a localized defect state or interface dipole at the high-κ silica interface.[232] The offset is not as significant for the lanthanum oxide capped HfSiON (-122 mV) compared to HfSiO (-184 mV) after annealing at 1000 °C for 5 sec, implying that the nitrogen serves as a diffusion barrier for lanthanum toward the substrate. MOS devices had an EOT between 1.25 and 1.35 nm after the 1000 °C anneal, and would be expected to decrease with a thinner HfSiO or HfSiON interlayer.

The flat-band voltage shift is also analyzed for various alternate lanthanide capping layers on HfSiON. **Figure 6.11** shows the respective shifts for 5 Å capping layers of lanthanum,

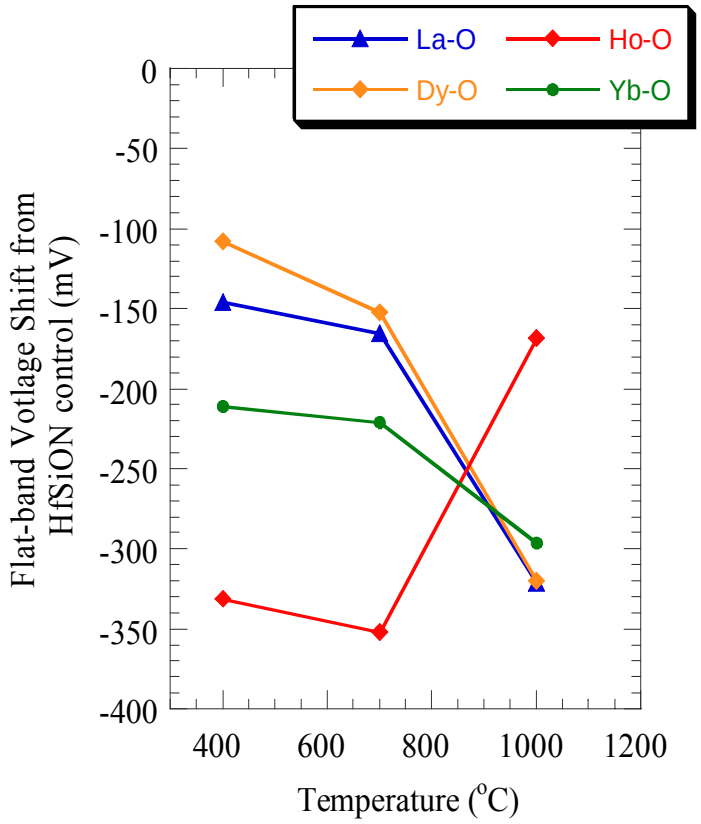


Figure 6.11: *Flat-band voltage shift as a function of anneal temperature for 5 Å lanthanide (La, Dy, Ho, and Dy) oxide capping layers on 15 Å HfSiON.*

dysprosium, holmium, and ytterbium oxide on 15 Å HfSiON with respect to a gate stack without the lanthanide capping layer. Compared to previous results, a significant shift is observed even after low anneal temperatures, most likely due to the thin HfSiON layer (15 Å) used in the analysis. At temperatures below 1000 °C, a significant variation is observed in the magnitude of the V_{FB} shift is observed for the different lanthanides in the gate stack. The magnitude of the shift suggests that the diffusion/reaction might be a function of lanthanide (Ho > Yb > La > Dy), however the mechanism cannot be explained by simply ionic radius comparison. After a 1000 °C anneal temperature, a similar magnitude of V_{FB} shift is observed for capping layers of lanthanum, dysprosium and ytterbium oxide. From the interface dipole model predicted by Sivasubramani et al.,[232] a decrease in the dipole magnitude is expected (~25 %) for the various lanthanide oxides compared to lanthanum

oxide. Unexpectedly, the holmium oxide shows a significantly different trend compared to the other lanthanide capping layers on HfSiON.

To further examine the ability to use these lanthanide oxides as capping layers on HfSiON in real MOSFET devices, the stability of such lanthanide cations on silicon must be examined. In order to do so, the annealed gate stacks were characterized by back-side SIMS. Using this process, it has been previously determined in **§5.6** that La cation diffusion is prevented by the incorporation of lanthanum in the silica matrix. **Figure 6.12** (a)-(c) shows the back-side SIMS profiles of 15 Å Ln-O capping layers on 25 Å HfSiON/10 Å SiO_2/Si gate stacks after 1000 °C, 10 sec annealing. It is observed form **Figs. 6.12 (a)** and **(b)** that the La and Dy cations are present only in the dielectric layer, suggesting that the diffusion of Dy into the silicon substrate, like La, may be impeded by its incorporation into the SiO_2 (or in this case HfSiON) matrix and is acceptable for use in standard MOSFET processing that includes a high-temperature anneal. **Figure 6.12 (c)** shows a Ho reaction layer ~100 nm into the silicon substrate. The observation of Ho cation diffusion in the substrate indicates that MOSFETS process at high temperatures with such a stack would incur high mobility degradation. The presence of the Ho cation in what would be the silicon channel also gives reason to the observed V_{FB} shift difference observed in **Figure 6.11**.

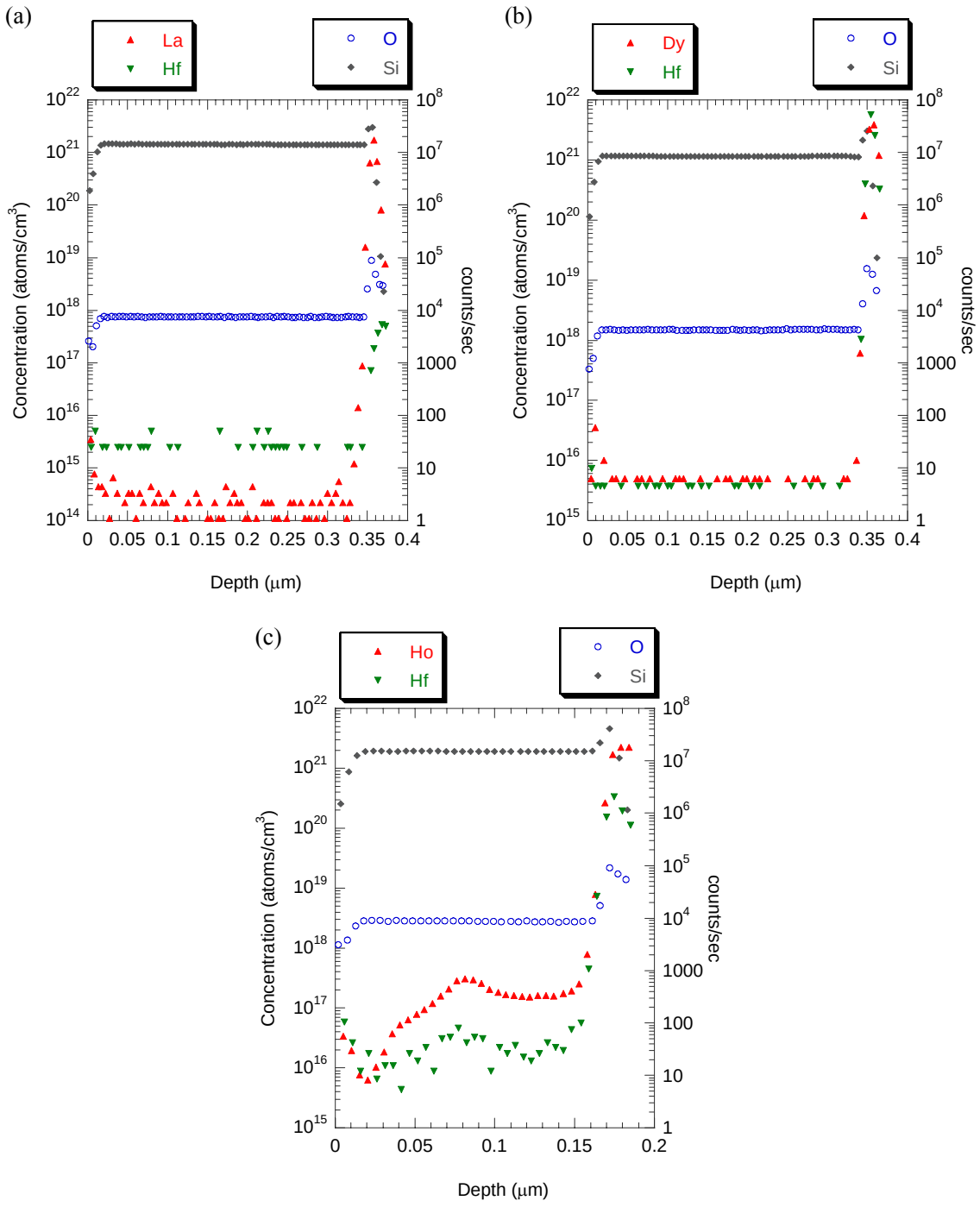


Figure 6.12: *Back-side SIMS profiles (a) La, (b) Dy and (c) Ho from a W/TaN/Ln-O/HfSiON/SiO_2//Si gate stacks after ex situ annealing at 1000 °C for 10 s in nitrogen.*

6.5 Lanthanum Silicate

As it has been shown that the lanthanum oxide induces a negative V_{FB} shift on the C-V curve, it is useful to examine the shift without the presence of a HfSiO(N) dielectric interlayer. XPS was first used to evaluate the silicate formation via the *in situ* anneal of the lanthanum oxide deposited on the chemical oxide with different pretreatments (either no pretreatment, ozone exposure, or ammonia anneal). **Figure 6.13** shows the O 1s binding energy of the lanthanum silicate dielectric with no pretreatment of the chemical oxide, comparing the as-fabricated spectrum (after the *in situ* reaction anneal) with that obtained after a 700 °C, 5 sec RTA. For comparison, the O 1s binding energy of the lanthanum

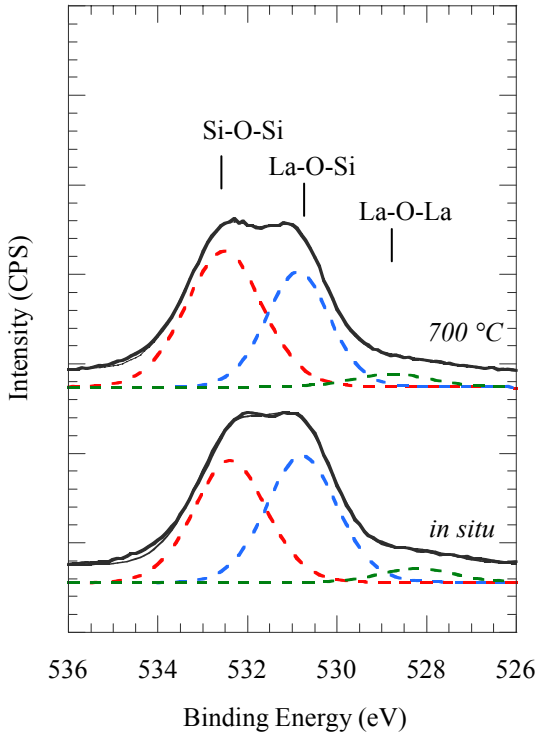


Figure 6.13: *O 1s XPS binding energies of $LaSiO_x$\Si with no chemical oxide pretreatment prior to and after annealing.*

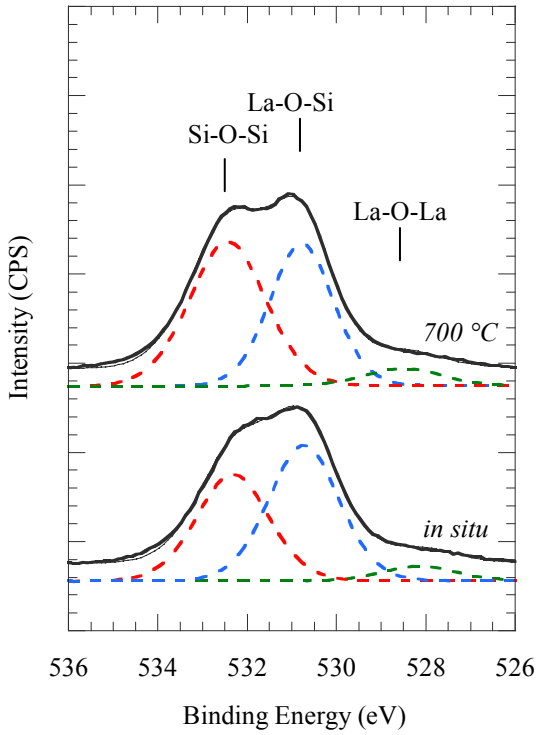


Figure 6.14: *O 1s XPS binding energies of $LaSiO_x$\Si with a ozone pretreatment to the chemical oxide prior to and after annealing.*

silicate dielectric with the ozone or ammonia anneal pretreatment is shown in **Figs. 6.14** and **6.15**, respectively. All samples have O 1s peak locations associated with primarily Si-O-Si (533 eV) or La-O-Si (531.1 eV), with only small amounts of unreacted La-O-La (529.3 eV) present, and peak positions correspond well with literature values.[51,167, 235] It is worth noting that a control sample with no *in situ* anneal is a iniquitous comparison due to the high affinity of lanthanum hydroxide formation. Lanthanum silicate, formed during the *in situ* reaction anneal, has been shown to be much more stable than lanthanum oxide in atmosphere[166] and therefore the O 1s binding energy was peak-fitted successfully without the La-O-H peak (532 eV). It is apparent that after the *in situ* anneal, the dielectric with the ozone pretreatment has a larger O 1s peak associated with La-O-Si peak (relative to the Si-O-Si peak) than the dielectric with no pretreatment. This suggests that the ozone pretreatment serves to catalyze the silicate formation during the *in situ* reaction anneal. On the other hand, the dielectric with the ammonia anneal pretreatment has a relatively smaller O 1s peak associated with

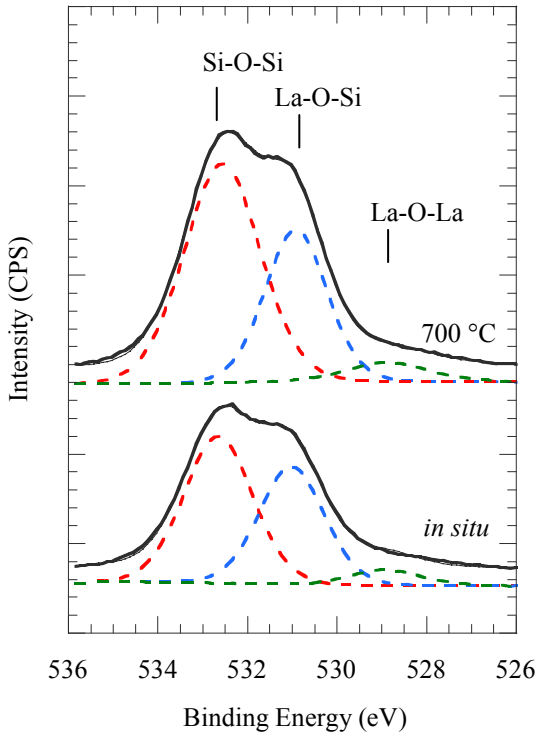


Figure 6.15: *O 1s XPS binding energies of $LaSiO_x$\Si with a 700 °C ammonia anneal pretreatment to the chemical oxide prior to and after annealing.*

La-O-Si peak. As anticipated, based on the reduction of the flat-band voltage shift with the HfSiON interlayer compared to the HfSiO interlayer, the inclusion of nitrogen in the chemical oxide retards the silicate formation. **Figures 6.13-6.15** also show that after a 700 °C, 5 sec anneal, the Si-O-Si peak increases relative to the La-O-Si peak, for all pretreatment conditions, associated with SiO_2 growth. After a 1000 °C, 5 sec anneal the O 1s peak associated with Si-O-Si (not shown in **Figs. 6.13-6.15**) increases significantly suggesting SiO_2-rich interfacial layer growth. As these samples analyzed by XPS are uncapped, trace oxygen from the RTA N_2 allows this observed interface layer growth to proceed.

The C-V curves for the control sample route are shown in **Fig. 6.16** for the *in situ* annealed and *ex situ* annealed MOS devices at 400 °C and 700 °C for 10 s. The capacitance of the sample increases after the 700 °C anneal and then decreases with additional annealing. This is not the case for all the process routes examined. As shown in **Fig. 6.17** the capacitance

decreases with *ex situ* annealing when an ozone pretreatment is conducted prior to the lanthanum oxide growth and *in situ* anneal. However, the total capacitance is higher after the *in situ* anneal. In this case, the ozone pretreatment appears to increase the total amount of oxygen for the initial growth of the lanthanum oxide and, as observed in the XPS results, subsequently promotes the lanthanum silicate formation during the *in situ* anneal. As shown in **Fig. 6.18**, with an ammonia anneal pretreatment to the chemical oxide the capacitance remains relatively unchanged with *ex situ* annealing. A comparison of the EOT values for all sample process routes is shown in **Fig. 6.19 (a)**. In the case with no pretreatment, the capacitance increase (or EOT decrease) with *ex situ* annealing can only be due to continued formation of the silicate (thus elimination of interfacial SiO_2). The ammonia anneal pretreatment of the silica chemical oxide most likely results in a SiO(N) dielectric with a higher dielectric constant than SiO_2 or a slight thinning of the SiO_2, therefore yielding a lower EOT value after the lanthanum oxide deposition and *in situ* anneal. Observation of a N

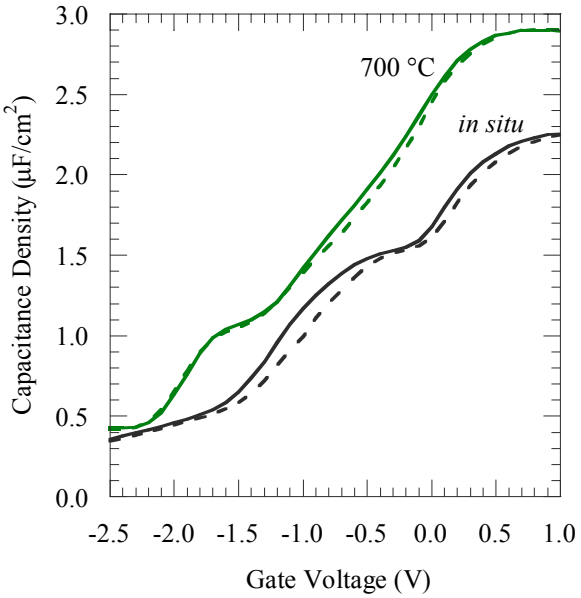


Figure 6.16: *C-V measurements for W/TaN/LaSiO$_x$/Si MOS devices with no chemical oxide pretreatment. Solid line represents (-) → (+) voltage sweep. Dashed line represents (+) → (-) voltage sweep. C-V characteristics measured at 1 MHz.*

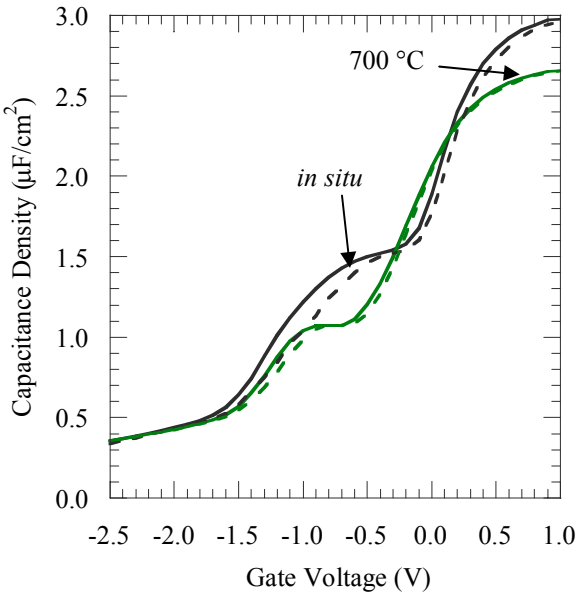


Figure 6.17: *C-V measurements for W/TaN/LaSiO$_x$/Si MOS devices with ozone exposure pretreatment to the chemical oxide. Solid line represents (-) → (+) voltage sweep. Dashed line represents (+) → (-) voltage sweep. C-V characteristics measured at 1 MHz.*

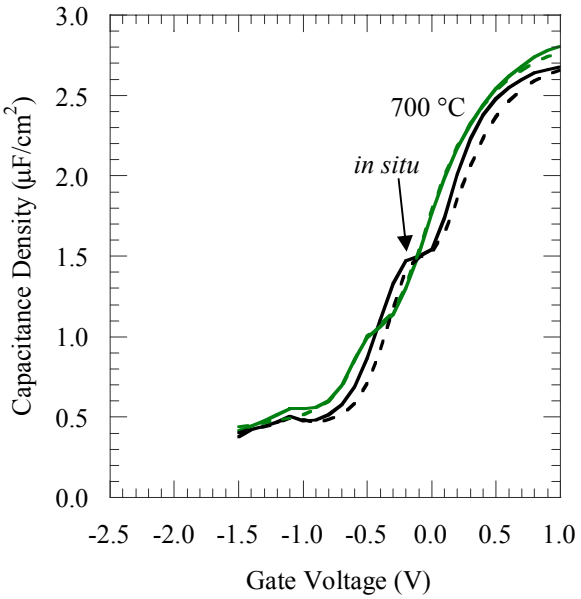


Figure 6.18: *C-V measurements for W/TaN/LaSiO$_x$/Si MOS devices with 700 °C ammonia anneal pretreatment to the chemical oxide. Solid line represents (-) → (+) voltage sweep. Dashed line represents (+) → (-) voltage sweep. C-V characteristics measured at 1 MHz.*

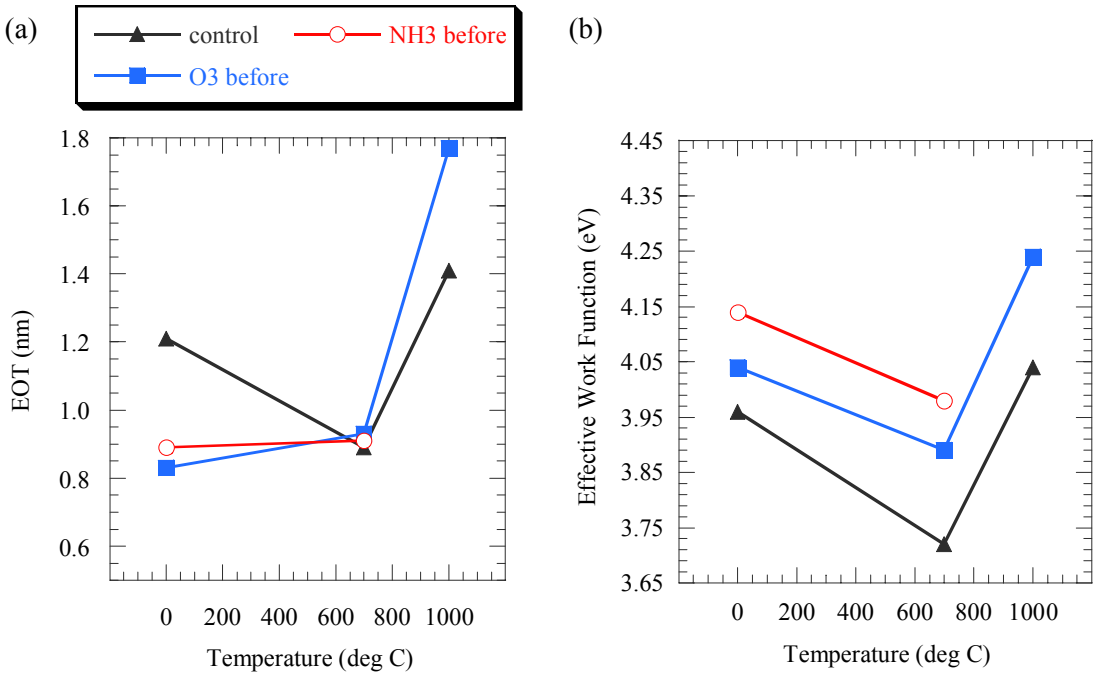


Figure 6.19: *(a) EOT and (b) $\phi_{m,eff}$ as determined by C-V measurements in situ and ex situ annealed samples processed with no chemical oxide pretreatment, ozone exposure pretreatment, and 700 °C ammonia anneal pretreatment. Also, annealing was conducted for 5 sec in N_2; C-V characteristics measured at 1 MHz; EOT and V_{FB} extracted from C-V measurement using NCSU Hauser model.*

1s peak at 298 eV (XPS spectra not shown) is evidence that nitrogen is present in the dielectric. Considering that the nitrogen in HfSiO(N) prohibits reaction of the lanthanum capping layer with an underlying SiO_2,[230] it is expected that the reaction between the lanthanum oxide and the SiO(N) is very sluggish. After the 700 °C anneal, the EOT values for all sample process routes is nearly identical at 0.9 nm. Gate leakage values at V_{FB} + 1 V are measured to be 0.6 A/cm^2 for the control, 0.3 A/cm^2 for the ozone pretreatment, and 0.08 A/cm^2 for the ammonia anneal pretreatment process routes. For all cases, the EOT increases and leakage decreases after the 1000 °C, 10 s anneal, most likely due to silica formation at the substrate interface from free oxygen residing in the W capping layer., as described in §5.5.

To compare the V_{FB} shift for these sets of samples, an effective work function is defined,

$$\phi_{m,eff,} = \phi_m - (V_{FB} + V_{FB,ideal}) \qquad \text{Equation (6.1)}$$

which can be determined from the input work function and the fixed charge determined from the NCSU CVC modeling program. A comparison of the $\phi_{m,eff}$ for all sample process routes is shown in **Fig. 6.19 (b)**. With only an *in situ* anneal, the lowest $\phi_{m,eff,}$ of 3.96 eV occurs for samples following the control process route with no additional treatments. In comparison, a ammonia anneal pretreatment and a ozone pretreatment yields $\phi_{m,eff}$ values of 4.14 and 4.04 eV, respectively. With a 700 °C, 10 s *ex situ* anneal, a decrease in $\phi_{m,eff}$ is observed irrespective of the process route prior to annealing. The wide variation in the voltage shift for the various process routes remains with only negligible variation in EOT (**Fig. 6.19 (a)**). The effective work function is then increased with the 1000 °C, 10 s *ex situ* annealing for all process routes with a corresponding EOT increase.

These lanthanum silicate results provide insights into the mechanisms controlling the negative V_{FB} shift. From these lanthanum silicate results, and the analysis of the lanthana capped Hf-based dielectric from this and related studies,[230,232] it is observed that increased lanthanum silicate formation near the substrate should result in an increased negative V_{FB} (or effective work function) shift. Based on the XPS results, after the *in situ* anneal, the level of silicate formation varies with chemical oxide pretreatment. The observation of a negative shift in the effective work function (or flat-band voltage) confirms a presence of a positive charge state which can be described as both localized and distributed. For example, the data is in agreement with a proposed interface dipole that emerges with lanthanum reacting with silica after diffusing through a hafnia-based interlayer. The fact that the presence of nitrogen in the chemical oxide retards this shift also supports this localized charge state mechanism. After 1000 °C annealing, where an SiO_2 interface layer is observed to be rapidly growing, the magnitude of the shift is decreased. This again correlates with the fact that a localized charge state exists and the distance to the Si interface is being increased after the 1000 °C anneal. However, the shift is also reduced by exposing the chemical oxide to an ozone pretreatment, a process condition that is shown to increase the lanthanum silicate formation. Therefore, it is suggested that the ozone pretreatment allows for the passivation of distributed charge

states, such as oxygen vacancies, that are most likely distributed throughout the lanthanum oxide. It is reasonable to propose that, for the case with no ozone pretreatment, these oxygen defects are unable to be passivated by the low pO_2 environment of the *in situ* anneal. It is also worthwhile to note that it is possible that the ammonia anneal could serve the same purpose as the ozone treatment by incorporation of –N or –NH bonds to satisfy the oxygen vacancies.

The effective work function provided in **Fig. 6.19 (b)** also shows that the relative shifts present after the *in situ* anneal continue throughout *ex situ* annealing, suggesting that the charge state phenomena is unable to be neutralized by annealing. This implies the existence of defects with high-temperature stability, such as bond constraint related localized charge states in silicates with a high congruent melting points[234] The incorporation of differing oxygen and nitrogen contents in the silicate (via ozone or ammonia pretreatments) could allow for reduced strain and effective variation in the localize charge state density.

With a 700 °C *ex situ* annealing, a large decrease in the voltage shift for all samples is observed, which would be attributed to the diffusion of lanthanum to the substrate. In addition, the same variation in effective work function associated with *in situ* anneal is still generally present, indicating that passivation of the defects is not yet able to occur with the 700 °C *ex situ* anneal. Interestingly, the EOT for each of the MOS devices is 0.9 ± 0.2 nm and the effective work function tuning is ~300 mV. The leakage current densities for these devices are < 0.6 A/cm^2. Note that the interface trap density observed by the inflection in the C-V curve is nearly identical with annealing for each process route (2.0 ± 0.5 x 10^{13} $eV^{-1}cm^{-2}$), showing that the shift is not dependant on the condition of the substrate interface. With the rapid EOT increase after a 1000 °C *ex situ* anneal, the effect of the localized charge state is dampened by the SiO_2 growth. With a better oxygen diffusion-barrier electrode, a wide range for effective work function tuning would be expected even after the high-temperature anneal.

6.6. Conclusions

For use in nMOS devices the metal gate work function is required to be ~4.10 eV, a value that is lower than the work function of most thermally stable nitride electrodes. Therefore, a method to decrease the effective work function by introducing a negative voltage shift is required. Incorporation of lanthanides (La Dy, Ho and Yb) in the dielectric is shown to invoke such a voltage shift. Cation diffusion into the silicon substrate is not observed for La and Dy after high temperature annealing (1000 °C, 10 s). However, back-side SIMS clearly shows a reaction front with the use of Ho incorporation. In general, it is shown that a Hf-based dielectric interlayer reduces the affect of the lanthanide by moderating the reaction between cation and underlying silica. The presence of the Hf-based dielectric increases the overall EOT, which also needs to be minimized. A lanthanum oxide layer deposited directly on a silica chemical oxide results in a larger negative V_{FB} shift, as the Hf-based dielectric is no longer present to slow the diffusion. An ozone and ammonia anneal pretreatment is shown to help control the overall negative shift and expand the obtainable gate stack effective work function from 3.75 and 4.25 eV, taking into consideration all anneal temperatures and corresponding EOT values. The shifting is consistent with localized and distributed mechanisms suggested in literature. After a 700 °C, 5 s anneal, a work function tuning span of 300 mV was achieved, while maintaining an EOT of 0.9 nm and a leakage current density < 0.6 A/cm^2. It is apparent that the reaction between lanthanum oxide and silica is essential in creating a positive charge state, which agrees with localized or distributed mechanisms presented in literature.

7. Conclusions and Future Work

This dissertation serves to analyze and report upon the use of lanthanide-based high-κ dielectrics for high-end metal-oxide-semiconductor field effect transistor (MOSFET) devices. Lanthanum oxide was studied by electrical and analytical means in the framework of an MOS gate stack. This dielectric was chosen due to its optimal electrical properties and high thermodynamic stability in the silicate phase. The electrical data obtained for such a stack is of unparallel electrical quality under processing temperatures compatible with identified low and high-temperature MOSFET processing routes. Materials characterization provides a detailed analysis as to high-quality of the devices. The first section of this chapter summarizes the innovative and technical accomplishments that have been reported in the dissertation. The final section briefly overviews the future direction of the high-κ dielectric in terms of future transistor design.

7.1 Conclusion

The following is a review of the conclusions from the work in this dissertation:

- The low temperature reaction between lanthanum oxide (grown by thermal evaporation) and a silica chemical oxide is observed to occur at temperatures as low as 400 °C. *Ex situ* annealing results the formation of the silicate along growth of SiO_2, reducing the device properties. A controlled pO_2 anneal results in optimization of the device properties by reducing the extent of SiO_2 growth during the anneal.
- Using this controlled low temperature processing route, devices are realized with a 0.5 nm equivalent oxide thickness (EOT) and a leakage current density (J) of 5 A/cm^2 (evaluated at flat-band voltage + 1 V).
- TaN is observed to be a higher quality gate electrode than Ta based on thermal stability in a nitrogen anneal and the result of higher quality devices after annealing. With a TaN electrode, EOT values are observed to be as low as 1.1 nm (J < 0.5 A /cm^2) after a 1000 °C, 10 s anneal in nitrogen.

- Interface trap density is observed to decrease with anneal time to values < 1 x 10^{-10} eV^{-1} cm^{-2}, but is highly dependent on SiO_2 growth during annealing. Routes for reducing D_{IT} with a concurrent reduction in EOT have not been identified.
- The tungsten capping layer, used for attaining good electrical contact, is shown to have the ability to contain high quantities of oxygen. Upon annealing the oxygen can be released and allowed to diffuse to the silicon substrate, resulting in a degradation of the device properties.
- The diffusion barrier properties of TaN to oxygen are reported by the observation of EOT increase (i.e. SiO_2 growth from O_2 reacting with silicon). It is predicted that atomic oxygen (from high-oxygen concentration tungsten) easily diffuses through TaN, more so than molecular oxygen. Enhanced barrier properties to oxygen are realized by the use of a low-oxygen concentration tungsten capping layer.
- The diffusion of atomic lanthanum, dysprosium and holmium into the silicon substrate is examined by using a back-side SIMS approach which enhances the detail of the dielectric/substrate interface. No diffusion of lanthanum or dysprosium is observed using the technique. Significant diffusion of holmium into the substrate is observed. Comparison to other lanthanum-based gate dielectrics suggests that the crystallization resistance of the silicate is responsible for the stability of the lanthanum and dysprosium based dielectric on silicon.
- Lanthanide (La, Dy, Ho, Yb) oxide capping of a HfSiO(N)/SiO_2/Si gate stack is shown to result in a negative flat-band voltage shift upon annealing. The use of such a shifting mechanism allows for hafnia-based nMOS compatible devices that are typically plagued by pinning of the Fermi energy level. The incorporation of nitrogen into the hafnia-interlayer reduces the V_{FB} shift (-122 mV for HfSiON, -184 mV for HfSiO) after a 1000 °C, 5 s anneal. HRTEM and STEM analysis indicates intermixing of the lanthanum oxide in the gate stack at temperatures as low as 400 °C.

- The resultant reduction of the effective work function is increased to ~300 mV for use of a lanthanum silicate. However, the magnitude of the reduction can be lowered and controlled by the incorporation of nitrogen and/or additional oxygen. In the work, an ammonia anneal and a ozone exposure to the chemical oxide was used to incorporate each species, prior to the lanthanum oxide deposition and silicate reaction anneal. It was shown that the various pretreatments change the extent of silicate formation. The result allows for a +/- 150 mV (around 4.0 eV for TaN electrode) tailoring of the effective work function for the device. In addition, of the EOT to 0.9 nm and $J < 0.6$ A/cm^2 is realized for all samples after a 700 °C, 5 s anneal.
- Localized and distributed mechanisms reported (interface dipole, bond constraint theory, and oxygen-vacancy defects) in literature appropriately describe the observations of the flat-band voltage shifts.

7.2 Future Work

In the dissertation, a route for producing high-quality lanthanum silicate MOS devices has been covered in great detail. The interpolation of measured MOS properties to expected MOSFET properties can be inferred, but in general the MOSFET devices will be need to be created with lanthanum silicate to provide sufficient evidence that the dielectric will offer the added property gain observed in the MOS device. To date, the use of a lanthanum silicate in an actual MOSFET device flow has not been attempted. However, the use of the lanthanum oxide capping layer on HfSiO(N) has been shown to yield outstanding MOSFET properties. In doing so, lanthanum silicate is most likely occurring at the interface. The use of lanthanum silicate by itself is not too far fetched. However, precise control over the silicate formation and the mechanism by which the flat-band voltage is allowed to shift in such a stack must be realized.

As shown in **Chapter 6**, it is purposed that the control of the lanthanum silicate formation allows for tailoring of the effective work function of a device. The key is the formation of the internal dielectric interface (silicate). The phenomenon is described by multiple mechanisms that are purposed in literature, noting that multiple mechanisms are most likely

acting simultaneously. The observation of the similar relative shifts with annealing for all samples suggests that the bonding constraint defects formed during the initial anneal are nearly ‘frozen’ in place and are unable to be annealed out. If this is the case, then the controlled silicate formation could be a means for precision effective work function tailoring.

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