ABSTRACT

DANDU, KRISHNANSHU. Characterization and Modeling of III-N MOS-HFETs for High Frequency Applications. (Under the direction of Dr. D. W. Barlage).

This research focuses on the characterization and modeling of AlGaN/InGaN MOS-HFETs. DC and small signal S parameter measurements were used to characterize these FETs and the associated AlGaN/InGaN MOS heterojunction varactors. An equivalent circuit model was developed for the AlGaN/InGaN MOS varactor. The model fits measured S-parameters of the device from 45 MHz to 10 GHz over the entire operating range of the device (gate bias varies from -8V to 6V). The extracted gate capacitance indicated formation of an accumulation channel in the AlGaN barrier layer in forward bias ($V_g > 3V$). A physics-based large signal model has been developed for the varactor. The model utilizes the triangular well approximation to describe charge control at the heterointerface and takes polarization into account. Free carrier generation and neutralization of donor atoms in the AlGaN barrier layer are also taken into account. The model fits extracted gate capacitance in HFET mode of operation and exhibits the real space transfer of free charge into the barrier layer. The second part of this work focused on the small signal characterization and modeling of the MOS-HFETs. A direct extraction technique was implemented to extract the small signal components of a FET in presence of bias dependent series resistances. This method was used to the extract small signal equivalent circuits for the AlGaN/InGaN MOS-HFETs, which exhibited bias dependent source and drain resistance. In the third part, a large signal model has been developed for these devices using the linear charge control equation while taking polarization effects into account. The intrinsic device model uses a quasi two dimensional solution of the Poisson equation in the channel to take velocity saturation effects into account. Capacitances are modeled by developing analytical expressions for the channel charge, partitioned between source and drain. The model has been implemented in Agilent ADS using Verilog-A and is compared to measured DC IV and small signal parameters. The limitations of this model are discussed and methods to enhance it are proposed. Electrical characterization techniques to estimate thermal resistance of the device and low field mobility under a transverse field have been developed. Work done on characterization and modeling of GaN n-i-n structures utilizing re-grown source drain contacts is presented and discussed.
Characterization and Modeling of III-N MOS-HFETs for High Frequency Applications

by

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Dr. Mark Johnson
To my family and my teachers.
Biography

Krishnanshu Dandu was born to Chandrasekhar Reddy and Nalini Reddy in Varanasi, India on 12th February 1978. He graduated from St. John’s school in Varanasi and joined the Indian Institute of Technology, Kanpur India. Four years later he graduated with a Bachelor of Technology in electrical engineering. He enrolled as a Master’s student at N.C. State university in August 2001 and got his M.S. in electrical engineering in August 2003. Upon completion of the Master’s program he continued on as a Ph.D. student under the supervision of Dr. Barlage in microwave circuits and devices. During this work he performed research on modeling and characterization of III-nitride semiconductor devices and developed a significant interest in the physics and technology behind high frequency devices and circuits. He was an intern at Agilent Technologies, Santa Rosa, CA in summer 2004 and at R.F. Micro Devices in Greensboro, NC in summer 2005 where he got to work in the device modeling systems group and the device characterization group, respectively. Upon completion of the Ph.D. he will be joining the RF modeling group in Texas Instruments at Sunnyvale, CA. Krishnanshu’s interests lie in the modeling and design of devices and circuits for RF and microwave systems.
Acknowledgements

This work would not have seen the light of the day without the influence of various people. A major part of the credit for this work has to go to Dr. Barlage for providing inspiration and encouragement throughout the course of this work. Apart from the direct input into this work, the technical discussions on various subjects provided a valuable source of ideas that will hold me in good stead for years to come. From the initial training on microwave measurements and modeling to the final discussions of my work, I consider myself very fortunate to have worked with him. I would also like to thank Dr. Mark Johnson for providing the necessary suggestions and insights during the course of my work. I thank Dr. Leda Lunardi and Dr. Kevin Gard for serving as members of my Ph.D. advisory committee and providing input on my work during the examination process.

The collaborative nature of this work would not have been possible without the members of my research group. For this, I have to give special thanks to Yawei Jin, Lei Ma and Chang Zeng. The countless hours spent discussing technical and not so technical subjects played significant roles in paving a the path to completion of this work. I have to thank Chang and Lei for fabricating the devices and structures that kept me busy during a good duration of my stay here. Appreciation has to also go out to Dr. Yoga Saripalli and his colleagues in Dr. Mark Johnson’s group who grew the materials and developed the re-growth techniques for patterned GaN surfaces on which the MOS devices were fabricated by Chang and Lei. Last but not the least, I thank Dr. Dave Braddock of OSEMI Inc., Rochester, MN for providing the AlGaN/InGaN MOS-HFET devices that form the backbone of this work.

Beyond my research group, there have been various people that have influenced me during the past few years. A special round of thanks and appreciation goes out to friends and acquaintances here at NC State and elsewhere, who have made the time spent as a Ph.D. student both enjoyable and bearable during certain times.

I have to thank my family for being the ultimate source of strength and encouragement throughout my academic career and personal life. They have served as role models in various ways and I aspire to live up to their ideals. My brother deserves special thanks for being a very close friend and serving as an ideal counterfoil to me and my tendencies while providing the required support and encouragement. Finally, I have to thank Aneeta, my fiancee, for believing in me and my capabilities.
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Chapter 1

Introduction

1.1 Overview

The invention of the bipolar transistor in 1947 ushered in the electronics revolution and changed everyday life around us. Inventions and discoveries in semiconductor materials and devices have come rapidly in the 60 years since. Silicon (Si), as a result of its excellent interface with native silicon dioxide (SiO$_2$), has become the cornerstone of the industry and drives the digital age forward. The continued scaling of device dimensions which has approximately followed the oft quoted Moore’s law has pushed us into the regime of nanoscale structures and devices.

Development of microwave devices and circuits did not gain the same attention as Si based MOSFETs for digital applications until the 1980’s because of the lack of commercial applications. The major focus of microwave device and circuit development was toward military applications. Satellite television and their receivers ended up as the initial applications of microwave devices and circuits for the consumer market. The situation changed dramatically in the 1990’s when the first modern personal wireless communication systems reached critical mass. Within a relatively short span of 15 years, wireless devices and technologies have become an integral part of modern life. This has increased the intensity of research and development in this arena.

The need for high performance devices has distinguished microwave devices from
those geared toward digital applications. Microwave and wireless devices have relied on III-V semiconductors since the 1960’s when the GaAs MESFET was announced by Mead [1]. GaAs has significant advantages over Si for high speed devices because of higher electron mobility. This advantage was further advanced by the ability to grow heterostructures using molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD). The heterojunction bipolar transistor (HBT) and the heterojunction FET (HFET) utilized the heterojunction to improve device performance by controlling charge confinement and transport across a barrier.

The HFET, also referred to as the HEMT (high electron mobility transistor), the MODFET (modulation doped field effect transistor), the TEGFET (two dimensional electron gas field effect transistor) and the SDHT (selectively doped heterojunction transistor) evolved out of the superlattice structures proposed and studied by Esaki and Tsu in the late 1960’s [2]. These structures utilized alternating layers of GaAs and AlGaAs to transfer electrons from a doped AlGaAs layer to the undoped GaAs layer adjacent to it and the devices exhibited extremely high electron mobility because of the reduction in scattering from dopant atoms. Dingle and his co-workers at Bell laboratories were the first to demonstrate the modulation doping concept and realized the ability to utilize a superlattice with just two layers (AlGaAs and GaAs) as the basis for a FET [3]. The first HFET based on this concept was announced in 1980 [4]. Rapid development and new techniques of growing material layers with differing lattice constants have given rise to GaAs pseudomorphic HEMTs (pHEMTs) and metamorphic HEMTs (mHEMTs). As long as the thickness of the grown layer is smaller than a critical value, its crystalline structure adjusts to the underlying lattice constant. AlGaAs/InGaAs/GaAs pHEMTs are in commercial use in low noise amplifiers (LNAs) and power amplifiers (PAs). Metamorphic HEMTs promise higher frequency operation but they are still in research and development [5]. Eventually, the InP HEMT and MHEMT are expected to replace the pHEMT for millimeter wave (10GHz - 100 GHz) low noise and power amplifier applications.

One area that the current semiconductors in commercial production are lacking is for operation at high power, high frequency and high temperature. Wide bandgap materials such as SiC and GaN have generated immense interest in the last decade because of their promise to operate generate very high output power at high frequency and temperature. The specific material properties are discussed in the next section. SiC MESFETs and AlGaN/GaN HEMTs are the two device technologies being developed for commercial power
amplifier applications in the wireless infrastructure industry. Apart from this, defense applications also look forward to these technologies in order to replace some of the high power amplifiers and sources still based on vacuum tube technology [6].

An overview of the current and future applications of the various device technologies in research and development is provided in 1.1.

1.2 Wide Bandgap Materials

Wide band gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have drawn a lot of attention in device research because they can offer extremely high power densities. This has a significant impact on the design and development of power amplifiers (PA) for applications such as base stations for wireless communication systems, satellite communication systems and military electronics such as phased array radars.

A comparison of material properties of common semiconductors (table 1.1) indicates the advantages of wide bandgap materials for high power applications. The electron saturation velocity in GaN is $2 \times 10^7 \text{cm/s}$ which is twice the saturation velocity in Si and
GaAs. This translates into higher a higher $F_T$ at the same gate length while operating at high voltages. High voltage operation is also enhanced because of the large band gap of 3.4 eV for GaN which leads to a large breakdown field of 2000 kV/cm in comparison to 400 kV/cm for GaAs. For high power operation, thermal effects become critical and even in this GaN enjoys a significant advantage over GaAs because of it’s higher thermal conductivity. Finally, the lower dielectric constant of GaN ensures that the input and output capacitances of a device will be smaller in comparison to a similar sized GaAs or Si device. This makes it easier to design matching networks at the high frequencies where these devices will be deployed.

Table 1.1: Material parameters of selected semiconductors

<table>
<thead>
<tr>
<th>Material</th>
<th>$E_g$ (eV)</th>
<th>$\epsilon_r$</th>
<th>$E_c$ (kV/cm)</th>
<th>$\kappa$ (W/°K·cm)</th>
<th>$\mu_n$ (cm$^2$/V·s)</th>
<th>$v_s$ (x 10$^7$ cm/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>11.9</td>
<td>300</td>
<td>1.5</td>
<td>1500</td>
<td>1</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.43</td>
<td>12.5</td>
<td>400</td>
<td>0.54</td>
<td>8500</td>
<td>1</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>3.2</td>
<td>10</td>
<td>1800</td>
<td>4</td>
<td>1000</td>
<td>2</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>2.86</td>
<td>10</td>
<td>4000</td>
<td>3.5</td>
<td>500</td>
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<td>9.5</td>
<td>2000</td>
<td>2.3</td>
<td>1250</td>
<td>2.2</td>
</tr>
<tr>
<td>Diamond</td>
<td>5.6</td>
<td>5.5</td>
<td>5000</td>
<td>20-30</td>
<td>2200</td>
<td>2.7</td>
</tr>
</tbody>
</table>

1.3 Power Transistors

The RF power transistor market is currently dominated by Si LDMOS devices. However, these devices are not expected to operate efficiently beyond 3 GHz [5]. Also, Si is not an ideal material for operation at high temperatures due to the low bandgap.

The maximum power densities achievable from current technology high power FETs is of the order of 1 W per mm of gate periphery. To generate power levels higher than this, the devices would have to be either (i) scaled to large sizes or, (ii) designed as a complex module using power combining techniques so that several smaller devices working together can deliver the required power output. However, both approaches have drawbacks. The first approach leads to very small device impedances on both the input and output as a result of the extremely large capacitances present on both ports of the device, (this problem is magnified as we move higher up in frequencies). This complicates the design of matching networks to transfer power from the stage preceding the power amplifier in a communication
circuit (usually the modulator with an RF driver) and also from the device to a real load at the output (the antenna in a communication system). The second technique leads to large power amplifier modules depending on the number of stages being combined and decreases the operational reliability of the system.

With power densities in the range of 10-12 W/mm being reported for AlGaN/GaN HFET’s at X band [8], GaN and SiC FETs are poised to ease the restrictions on PA design and development for wireless infrastructure applications. These devices are expected to provide at least a factor of 5 improvement in power density over current high power devices [7]. As of now, commercialization of devices based on these technologies is facing numerous obstacles due to issues with material quality and defect densities which limit RF performance.

1.4 Motivation and Objectives

The main goal of this work is to characterize and model GaN based devices and structures that lead toward the development of a realistic GaN MOSFET. The specific device that forms the bulk of the study is the AlGaN/InGaN MOS-HFET. This device utilizes an oxide as the gate dielectric layer to reduce gate leakage in forward bias and act as a passivation layer to reduce the effects of trapping related dispersion.

An interesting opportunity has arisen out of GaN research. GaN-insulator inter-
faces have been demonstrated with a low density of interface states ($D_{it}$) leading to the demonstration of GaN MOSFETs [9]. The work in this thesis lays the groundwork for further investigation of the performance of GaN MOSFETs. The large signal model will be used to initiate circuit design activities using the AlGaN/InGaN MOS-HFETs.

The primary focus of research in our group is the development of true enhancement mode GaN MOSFET’s. This is motivated by the advantages of GaN for very short channel devices due to its large bandgap, high saturation velocity and overshoot velocity which are the limiting factors for MOSFETs with gate lengths 9 nm and beyond [10]. One of the components of this work is related to the characterization and modeling of n-i-n structures fabricated to demonstrate re-grown source drain contacts.
1.5 Outline of Dissertation

Chapter 2 provides the background on the devices and materials investigated in this work. The principles of HFET and MOSFET operation are outlined. The electronic properties of III-nitrides are discussed and finally a discussion of the state of the art in AlGaN/GaN HFETs and GaN MOSFETs is presented.

Chapter 3 presents a small signal model developed to extract the gate capacitance of the AlGaN/InGaN metal oxide semiconductor heterojunction FET’s (MOS-HFET’s). The characterization and modeling of this structure was the first step in pointing us toward the development of MOSFET’s in GaN. Following the development of the small signal model, a physics based model was developed for the gate capacitance. The results of this model are presented and the limitations of the model in its present form are discussed.

Chapter 4 outlines a small signal modeling procedure that was developed to model the MOS-HFET’s. This chapter presents a method to extract bias dependent series resistances.

Chapter 5 introduces the large signal model development for the AlGaN/InGaN MOS-HFET and discusses results obtained from it.

Chapter 6 discusses results from characterization and modeling of GaN n-i-n structures with regrown source/drain contacts. This characterization allows us to estimate effective electron mobility in the GaN samples with knowledge of physical dimensions of the device.

Chapter 7 summarizes the results from this research and provides guidelines for future work.
References


Chapter 2

Background

This chapter presents the background material pertaining to the characterization and modeling of devices that will be investigated. The chapter starts with a discussion of the electronic properties of III-nitrides, mainly focusing on polarization in the materials and its impact on the operation and modeling of heterojunction FETs. It is followed by an overview of the current status of GaN FET development. The devices considered in this discussion are the AlGaN/GaN HFET, MOS-HFET and GaN MOSFET. The chapter ends with a discussion of the various approaches that can be taken to develop a large signal model for a device and the approaches that have been taken until now to develop models for GaN FETs. A basic flow chart for developing a large signal model including dispersion and thermal effects is presented.

2.1 Polarization in III-Nitride materials

In this section, the basic equations required to calculate polarization in strained III-nitride layers are presented and the impact of polarization on charge control in HFETs is discussed. Most of the material in this discussion on polarization in III-nitride semiconductors and devices is derived from [1]-[5].

Wide bandgap III-V nitrides can exist in Wurtzite (WZ) and Zinc-Blende (ZB) crystal structures. The wurtzitic structure is the predominant form for semiconductor
Figure 2.1: An illustration of the convention used to determine polarity in wurtzite nitride films. The figure shows a Ga(Al)-polarity crystal with the bonds parallel to c-axis (horizontal in the diagram) going the cation (Ga or Al) to anion (N). The direction of spontaneous polarization in GaN and AlN is also shown with the higher magnitude of polarization in AlN represented by the length of the arrow. Polarization discontinuity at the interface between the two crystals is represented by $\Delta P_{sp}$ and leads to a positive polarization charge (Adapted from [1]).

device applications with the discussion in this chapter specifically referring to this. The wurtzite crystal is tetrahedrally coordinated and lacks inversion symmetry in the unit cell [1]. As a result, the crystals exhibit strong piezoelectric effects when strained along $<0001>$ direction. In addition to piezoelectric effects, wurtzite GaN has spontaneous polarization even in the absence of strain. The piezoelectric effect arises from lattice mismatch strain and thermal strain caused by the thermal expansion coefficient difference between the substrate and the epitaxial layers. The presence of defects in a crystal can reduce strain and lower the strength of piezoelectric polarization. Polarization is dependent on the polarity of the crystal [2]. The polarity of a crystal depends on whether the bonds along the c-direction are from cation (Ga) to anion (N) sites or vice versa. The convention used in setting up all polarization related equations is that the [0001] axis points from the face of the N plane to the Ga plane, and marks the positive z direction. When the bonds along the c-direction are from the cation to anion atoms, the crystal is said to be Ga polarity and the direction of the bonds from Ga to N along the c-direction marks the [0001] direction. In N polarity crystals the bonds along the c-direction are from the N to Ga atoms and marks the -z direction. This is illustrated in figure 2.1.

Polarization along the [0001] axis is of primary interest for device design because
this is the direction along which epitaxial films and heterostructures are currently grown. Let the spontaneous polarization and piezoelectric polarizations along the c-axis of the wurtzite crystal be denoted by $P_{SP}\hat{z}$ and $P_{PZ}\hat{z}$. $\hat{z}$ refers to the unit normal vector along the c-axis (positive along [0001] direction). Using ab-initio methods, Bernardini et. al. [3] calculated the spontaneous polarization charge in AlN, GaN and InN to be -0.081, -0.029 and -0.032 C/m$^2$. Piezoelectric polarization vector is given by the dot product of the piezoelectric and stress tensors and can be written as $\hat{P} = \hat{d} \cdot \hat{T}$ where $\hat{d}$ is the polarization vector and $\hat{T}$ is the stress tensor. In wurtzitic symmetry, the number of independent components of $\hat{d}$ reduces to three: $e_{15}$, $e_{13}$ and $e_{33}$. [1]. The index 3 refers to direction of c-axis and in structures with growth along [0001] axis only the $e_{31}$ and $e_{33}$ components are important. The piezoelectric coefficients $e_{33}$ and $e_{13}$ can be used to calculate the piezoelectric polarization using [2]:

$$P_{PE} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y)$$  \hspace{1cm} (2.1)$$

where $\epsilon_x$ and $\epsilon_y$ are the in-plane strain components and $\epsilon_z$ is the out of plane component. The in-plane strain is assumed to be equal in both directions and is given by

$$\epsilon_x = \epsilon_y = \frac{a-a_0}{a_0}$$  \hspace{1cm} (2.2)$$

where $a_0$ and $c_0$ are the equilibrium values of the in plane lattice parameter. The relation between the lattice constants of the hexagonal GaN is given as

$$\frac{c-c_0}{c_0} = -2\frac{C_{13}a-a_0}{C_{33}a_0}$$  \hspace{1cm} (2.3)$$

where $C_{13}$ and $C_{33}$ are elastic constants. Using equations 2.1 and 2.3 the amount of piezoelectric polarization in the direction of the c-axis can be determined by

$$P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)$$  \hspace{1cm} (2.4)$$

The values of constants required to calculated polarization in the three nitride materials are given in Table 2.1. For the Ga face crystals, the piezoelectric polarization in AlGaN is negative for tensile ($a > a_0$) strain and positive for compressive strain. Since the in-plane lattice parameter of GaN ($a_{GaN}$ is larger than that of AlN ($a_{AlN}$), the AlGaN layer in an AlGaN/GaN system is in tensile strain and piezoelectric polarization is negative. Therefore, in a Ga polarity crystal, the net polarization in AlGaN points toward the interface and is larger in magnitude than the polarization in GaN. Applying Gauss’s law at the interface, it
Table 2.1: Spontaneous polarization, piezoelectric coefficients, elastic constants and c-plane lattice constants of GaN, AlN and InN. Data taken from [2] - [4]

<table>
<thead>
<tr>
<th>wurtzite</th>
<th>AlN</th>
<th>GaN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{SP}$ [C/m$^2$]</td>
<td>-0.081</td>
<td>-0.029</td>
<td>-0.032</td>
</tr>
<tr>
<td>$e_{31}$ [C/m$^2$]</td>
<td>1.55</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$e_{33}$ [C/m$^2$]</td>
<td>-0.60</td>
<td>-0.49</td>
<td>-0.57</td>
</tr>
<tr>
<td>$C_{13}$ [GPa]</td>
<td>108</td>
<td>103</td>
<td>92</td>
</tr>
<tr>
<td>$C_{33}$ [GPa]</td>
<td>373</td>
<td>405</td>
<td>224</td>
</tr>
<tr>
<td>$a$ [Å]</td>
<td>3.112</td>
<td>3.189</td>
<td>3.54</td>
</tr>
</tbody>
</table>

can be shown that a net fixed positive sheet charge forms at the interface (see figure 2.2). This aids the formation of the sheet charge at the heterointerface. At this point it would be instructive to understand how polarization charge enters the Poisson equation and leads to the formation of a sheet charge at the interface. In presence of polarization, the Poisson equation is modified to include the polarization field as shown below.

$\nabla \cdot \mathbf{D} = \rho$ \hspace{1cm} (2.5)

where

$\mathbf{D} = \epsilon \mathbf{E} + \mathbf{P}$ \hspace{1cm} (2.6)

This leads to the following equation

$\nabla^2 \phi = -\frac{\rho}{\epsilon} + \frac{\nabla \cdot \mathbf{P}}{\epsilon}$ \hspace{1cm} (2.7)

where $\mathbf{P}$ is the polarization in the material and includes spontaneous as well as piezoelectric components. In systems where polarization varies with position, polarization charge appears as a source on the right hand side and can be written as

$\rho_{pol.} = -\nabla \cdot \mathbf{P}$ \hspace{1cm} (2.8)

It should be noted here that by convention, the polarization vector points from negative charge to positive charge unlike the regular electric field. Assuming that the strain in epitaxial layers in a crystal is isotropic and homogeneous, the total polarization inside the bulk crystal is position independent and hence the gradient of polarization on the right hand side is zero. As a result, the polarization term can be ignored while solving the Poisson equation inside the bulk crystal. However, in heterostructures or in FET’s where the polar nitride materials have interfaces with other materials, there is a discontinuity in
the polarization at the interface which leads to the formation of a polarization sheet charge at the interface. This charge is given by the negative gradient of polarization as shown in the previous equation and can be rewritten for the case of a sheet charge at an interface as:

$$\sigma_{\text{pol.}} = - (P_2 - P_1)$$  \hspace{1cm} (2.9)$$

where the subscript 1 refers to the bottom layer as shown in 2.2 for the specific case of Al$_x$Ga$_{1-x}$N/GaN interface. For AlGaN and InGaN alloys, the values of spontaneous polarization, lattice constant, piezoelectric constants and elastic constants are calculated by linear interpolation between the values of the constants for AlN(InN) and GaN:

$$C(x) = C_{\text{AlN}}x + C_{\text{GaN}}(1 - x)$$  \hspace{1cm} (2.10)$$

where C is the constant being calculated.

From the discussion above, the amount of polarization in AlGaN can be controlled by changing the mole fraction of Aluminum in AlGaN to control the sheet charge density in the electron gas. For layers thicker than a critical value, strain relaxation occurs which leads to a reduction in piezoelectric polarization. This has to be taken into account while modeling devices with a high Al mole fraction in the barrier layer of an HFET [57]. In the AlGaN/InGaN/GaN devices modeled in this study, all the layers are grown Ga face.

Figure 2.2: Polarization charge at the AlGaN/GaN interface. The positive z axis points along the [0001] crystallographic axis which points upwards for Ga face crystals. Polarization fixed charge is given by the negative gradient of polarization which creates the positive sheet charge at the interface in case of AlGaN/GaN heterojunction.
As discussed in [1], this structure maximizes the potential for sheet charge in the quantum well due to the largest discontinuity in the polarization at the AlGaN/InGaN interface. Assuming the layers are grown pseudomorphically, the InGaN layer is in compressive strain ($a_{\text{InGaN}} > a_{\text{GaN}}$) and the AlGaN layer grown on top of the InGaN layer is under tensile strain ($a_{\text{InGaN}} > a_{\text{AlGaN}}$). The polarization discontinuity at the InGaN/GaN interface is dominated by piezoelectric polarization and gives rise to positive sheet charge. The directions of the polarization charges and fields are shown in figure 2.3. Using equation 2.9, the polarization sheet charge density at the Al$_{0.2}$Ga$_{0.8}$N/In$_{0.05}$Ga$_{0.95}$N interface is calculated to be $1.3 \times 10^{13}$ cm$^{-2}$. Another advantage of using Indium in the channel layer is the higher conduction band discontinuity of the AlGaN/InGaN heterointerface than AlGaN/GaN leading to a tighter confinement of charge in the quantum well [33].

Figure 2.3: Polarization vectors in AlGaN, InGaN and GaN are shown here. In InGaN, the direction of piezoelectric polarization is opposite to spontaneous polarization and greater in magnitude leading to a net vector pointing toward the interface with AlGaN. This increases the polarization induced charge at the interface with AlGaN.
2.2 Charge Control in an HFET

The cross section of a simplified HFET structure is shown in figure 2.4. The corresponding band diagram for the HFET is shown next to the device cross section. Although more complicated structures are used in real devices, this figure illustrates the basic principles of an HFET quite clearly. The doped barrier layer forms a heterointerface with the undoped buffer layer underneath. As a result of the conduction band discontinuity, a quantum well forms at the interface and charge transfers from the barrier layer to the quantum well in the buffer layer. Charge control is achieved by placing a metal Schottky gate on top of the barrier layer that modulates the depletion region in the barrier layer. Below threshold, the sheet charge is fully depleted. Under normal operating conditions, the barrier layer is fully depleted and the channel layer is screened by the formation of the sheet charge at the interface. As the gate bias is increased, charge transfer into the barrier layer takes place as hot electrons in the channel can overcome the conduction band discontinuity.

An accurate description of the charge control in an HFET requires a self consistent solution of the Schroedinger and Poisson equations at the heterojunction. When the De
Broglie wavelength of electrons is of the same order as the dimensions of the well formed by conduction band bending at the heterointerface [18], energies are quantized. A detailed discussion of the electronic properties of two dimensional systems can be found in [8].

### 2.2.1 Impact of polarization on sheet charge density

Initial work by Bernardini et al. and then Ambacher et al. [3], [2] showed that polarization fields are the cause for the high sheet charge density observed in AlGaN/GaN HFETs. It is now accepted that polarization fields are the driving force that lead to the accumulation of free carriers in the quantum well [10]. This has been shown by various works that calculated the sheet charge at AlGaN/GaN interfaces using a self consistent solution of the Schroedinger - Poisson system of equations [9], [11]. The impact of polarization fields on the conduction band potential has to be taken into account in the Schroedinger equation [10]. Freeman presents the necessary equations required to solve the Schroedinger and Poisson equations while taking into account local stress variation throughout the structure. Jogai and Sacconi’s works [9], [11] go through the self consistent solution for AlGaN/GaN HFETs. Both works indicate the importance of polarization fields in creation of the sheet charge at the interface. Jogai’s work also indicates that the polarization charge itself does not act as conventional dopant atoms supplying free charge for conduction in the quantum well. Instead, it acts as the driving force that leads to accumulation of free charge in the quantum well. The free charge can be provided by a doped barrier layer (which is the case in the devices studied in this work), surface donor levels as proposed by Ibbetson et. al. [12] or from unintentionally doped barrier layers due to intrinsic defects and impurities in the as grown materials.

A commonly used alternative to the fully consistent solution of Schroedinger and Poisson equations is the triangular well approximation, in which the quantum well is assumed to be triangular in shape, allowing a closed form solution of the Schroedinger equation and the wavefunctions as well as Eigen energies are given by Airy functions. This approximation has been used in chapter 3 to model the gate capacitance of the AlGaN/InGaN/GaN varactor.
2.3 AlGaN/GaN HFETs

The first results from AlGaN/GaN HFETs were published by Khan and his co-workers in 1994[31]. Since the initial demonstration, considerable progress has been made in the development of these devices and currently AlGaN/GaN HFET’s show great promise for high power and high frequency applications. Various groups have reported power densities around 10 W/mm at X band [8]. Sandhu et al reported AlGaN/GaN HFET’s with 3.2 W/mm and 71% PAE at 20 GHz [13]. Recently, field plated AlGaN/GaN HFETs showing 30 W/mm at X band have been demonstrated [14] which is a 30x improvement in power density when compared to GaAs and Si devices used currently in commercial applications. Although most of the attention on AlGaN/GaN HFET’s has been focused on development for high power applications, a few groups have published results from microwave noise characterization which indicates that these devices might be also useful for low noise applications [18], [19], [20]. A high power oscillator operating at X band delivering 1.7W with a phase noise of -87 dBc/Hz at a 100 KHz offset in a 30 Khz bandwidth [21]. These studies indicate that AlGaN/GaN HFET’s also have potential for applications other than high power devices.

2.3.1 Issues Facing AlGaN/GaN HFETs

There are several issues still limiting the performance of AlGaN/GaN HFETs. As mentioned earlier, HFET’s showing up to 10 W/mm of power density at X band have been demonstrated. However, most of these devices were operating at 5-6 dB of gain compression while achieving these power levels [15], indicating operation under undesired non linearities and negating some of their potential advantages.

Dispersion

The reduction in microwave power output is related to an observed reduction in drain current measured under RF drive as compared to DC characteristics. Maximum power obtainable from a device in class A mode of operation can be given by

\[ P_{\text{max}} = I_{\text{max}} \times (V_{\text{breakdown}} - V_{\text{knee}})/8 \]  

(2.11)
As 2.11 indicates, the maximum power drive can degrade either through a decrease in the maximum saturation current from the device or because of an increase in the knee voltage. This is commonly referred to as “current slump” or “current collapse”. This phenomenon is commonly attributed to the presence of surface traps in the gate drain access region which leads to the formation of a “virtual gate” as carriers trapped in the region deplete the channel underneath [38]-[39]. Others have attributed this to buffer layer trapping wherein hot electrons under a high drain bias escape from the 2DEG and get trapped in the buffer layer traps [40]-[42]. Another effect of dispersion in current-voltage characteristics is a frequency dependent output conductance that increases at high frequencies and a reduced transconductance at high frequencies [43]. The transition frequency can range from 1Hz to 1 MHz depending on the time constants involved in electron capture and emission processes. Both effects have a detrimental impact on the linear gain obtainable from the device. It has also been observed that the RF breakdown voltages are lower than the DC values. This has been attributed to the formation of charge dipole domains at the gate drain edge under high field (high voltage) operation [17].

**Thermal Effects**

Accurate thermal modeling of GaN devices is of critical importance because of the high power density that these devices are expected to operate under. Thermal effects degrade the performance of a device through a reduction in low field mobility as well as high field saturation velocity. Currently, most GaN devices are fabricated on sapphire substrates because of the relatively low cost. Sapphire has a thermal conductivity of 0.48 W/(K.cm) and thermal effects are very significant. SiC has a thermal conductivity of 3.2 (W/K.cm) which can lead to much better power dissipation through the substrate. This has been borne out by studies which showed that the temperature rise in a device on sapphire substrates is 4 times the rise in a device on SiC [22]. Other materials with better thermal conductivity than sapphire being investigated for use as substrates are AlN, Si and GaN could potentially replace sapphire for high power applications.
2.4 GaN MIS-HFETs and MISFETs

Khan and co-workers demonstrated AlGaN/GaN MOS-HFETs and MIS-HFETs using SiO$_2$ and Si$_x$N$_y$ as the dielectrics [32], [33]. They showed that the gate leakage in these devices is reduced by 2-3 orders of magnitude in comparison to a normal HFET. Also, the charge control in these devices stays linear over a larger operating bias region leading to a constant transconductance over a larger gate bias. Higher transconductance and a larger gate voltage swing increase the linear range of operation of the devices for power amplifier applications.

Various groups have reported on DC current-voltage and capacitance-voltage characteristics of GaN MOSFET’s and MISFET’s [28]-[35]. However, these devices are depletion mode devices with a negative threshold voltage. Irokawa et al. demonstrated enhancement mode MgO/GaN MOSFETs with a threshold voltage of 6V exhibiting 5.4 $\mu$S/mm of transconductance at $V_{ds}=3$V and $V_{gs}=9$V [30]. These studies indicate that enhancement mode MOSFET’s are possible in the GaN system with the proper selection of a gate dielectric and gate metal.

Dielectrics for GaN MOSFETs and MOSHFETs

The basic electrical requirements for a compatible dielectric to any semiconductor in the fabrication of MOSFETs are a high dielectric constant, large bandgap, large conduction band offset and a high quality interface with a low interfacial state density $D_{it}$.

For development of MOSFETs and MOSHFETs a compatible gate dielectric that forms an interface with low density of trapping states with the underlying semiconductor is required. A high density of interface states leads to a pinning of the Fermi level. Fermi level pinning occurs when the density of interface states is large enough to exchange charge with the underlying semiconductor without allowing the gate to control the conducting channel in the device. The states also trap charge and cannot respond to high frequency signals which leads to the dispersion characteristics observed in HFETs. Traditionally, this has been difficult to achieve for III-V semiconductors such as GaAs due to chemical and structural defects that are present at the interface. The development of dielectrics for GaN FETs is very similar to the path followed in the attempt to develop dielectrics for GaAs MOSFETs.
A high dielectric constant is desirable as it increases the gate capacitance which leads to a better channel control. In recent years, the development of high $\kappa$ dielectrics has been the focus in silicon research due to device scaling into nanoscale dimensions. Most of the dielectrics that are investigated for III-V material systems have a higher dielectric constant than SiO$_2$. However, development of high $\kappa$ dielectrics has faced significant roadblocks due to the difficulties in incorporating them into the silicon MOSFET process flow.

High conduction band offsets and a large bandgap are essential to reduce gate leakage via the thermionic emission, and Fowler Nordheim tunneling mechanisms. A high interface state density can also increase leakage through a trap assisted tunneling mechanism.

The fabrication of III-V semiconductor MOSFET’s on GaAs never found great success because of the high density of interface states present at the oxide-semiconductor interface that led to Fermi level pinning. However, for n-type GaN MIS systems, interface state densities ($D_{it}$) in the range of low to mid $10^{11}$ cm$^{-2}$eV$^{-1}$ were obtained using SiO$_2$ as the gate dielectric [24]. Other dielectrics that have been used on GaN include Si$_3$N$_4$ [25], MgO [27] and Ga$_2$O$_3$ [26]. All of these interfaces were reported to have $D_{it} \approx 10^{11}$ cm$^{-2}$eV$^{-1}$ with the capacitance voltage curves showing little hysteresis. Ren et al. found that Sc$_2$O$_3$ had lower interfacial state density than Ga$_2$O$_3$ in their study. The results from these studies indicate that GaN MOS interfaces have lower interfacial state density than GaAs (10$^{12}$ for GaAs) at a similar stage of development. AlN has also drawn attention as a potential dielectric for GaN MISFETs because of the large bandgap of 6.2 eV and higher conduction band offset with GaN. The success of Ga$_2$O$_3$/Gd$_2$O$_3$ as a device quality dielectric on GaAs has motivated a lot of work on trying to replicate similar results in the nitride system. The devices investigated in this work use this oxide as the gate dielectric.

The development of GaN MOSFETs is motivated by several advantages when compared to AlGaN/GaN HFETs and Si RF CMOS devices for high frequency applications, which are listed below:

1. True enhancement mode operation with a single power supply for circuit applications, thus increasing power efficiency.

2. The higher saturation velocity of GaN provides a higher $f_t$-$L_g$ product than Si. Also, it has been shown that the overshoot velocity in GaN is much higher than the steady state peak velocity for a given field value and extends over a longer distance [37]. This
can be exploited for the design of short channel devices wherein the velocity overshoot phenomenon can be observed under switching electric fields.

3. Higher breakdown voltage in GaN allows higher power density in GaN MOSFET’s compared to Si MOSFET’s. Very high breakdown voltages for GaN MISFET’s have been reported [36].

4. High quality dielectric layers can reduce dispersion issues and hence, the linearity of GaN MOSFET’s can be higher.

5. Forward swing on the gate limited by the breakdown process unlike in a HFET, which is limited by the Schottky diode turn on. The drain current of a FET can be written as

\[ I_{DS} = \frac{W}{L} \mu_n C_i (V_g - V_T) \frac{dV_c(x)}{dx} \]  

(2.12)

For a given gate periphery, the drain current drive of a MOSFET can be higher than that of a HFET because of the higher gate capacitance and a larger gate voltage swing.

### 2.5 Large Signal Modeling of FETs

Simulation of nonlinear circuits is heavily dependent on the ability of active device models to be able to predict the nonlinear phenomena occurring within the device. Since GaN FETs are primarily intended for power amplifier applications, figures-of-merit such as power added efficiency (PAE), third order intermodulation (IMD3) and adjacent channel power ratio (ACPR) have to be predicted accurately by the simulation. This is even more important for communication protocols such as CDMA that use constant envelope modulation schemes, which require a high level of linearity from the system in order to achieve low bit error rates (BER).

Nonlinear phenomena in circuits arise from the intrinsic device nonlinearities. Nonlinearities arising from the current voltage relationship are well understood and receive the most attention. However, charge storage mechanisms (intrinsic capacitances) are also significant contributors to the nonlinear behavior of a circuit. Terminal charge conservation is essential to accurately model nonlinear devices and circuits. It has also been shown that capacitance based large signal models can introduce a DC component in the current at a
node [48]. Hence, charge based models are preferred for circuit simulation. Device models can be broken down into three main types depending on the methods used to formulate the constitutive nonlinear relationships.

### 2.5.1 Empirical Models

Most of the popular models used for circuit design in CAD tools are empirical models such as the BSIM series models for MOSFET’s, Materka, Curtice, and TOM models for MESFET’s and HFET’s. The popularity of these models stems from the fact that they are easily implemented in a circuit simulator and are simulated quickly, which is essential for circuit design. The current-voltage and capacitance-voltage characteristics are represented by some combination of non-linear functions such as power series (Cubic Curtice being an example) and hyperbolic functions (Angelov model). In general, these models are capacitance based with the nonlinear capacitances being defined as a function of the terminal voltages. Although the simulation for a well extracted model can be very accurate, the model itself does not have predictive properties and a new model has to be extracted every time a new device or process is to be used. Scaling properties of these models are also not well defined and precautions have to be taken when using devices of a different size than what was used to extract the model.

### 2.5.2 Table Based Models

Table based models were developed by Root [46] to model high frequency devices. These models use smooth interpolating functions to generate missing data between measured data points for the DC current-voltage and high frequency behavior of a device. These models are generic and can be used to model any FET device once formulated. However, they do not have any predictive properties and a large number of measurements are required to model non-linear characteristics accurately.

### 2.5.3 Physics Based Models

Physics-based models are based on a physical description of the device. An accurately formulated analytical description can be used to predict device performance before
measured data is available. However, model formulation in FET’s is complicated because of the inherent two dimensional nature of the device. A popular charge control model formulated for MOSFET’s is the EKV model [65] which linearizes (an approximation) the inversion charge \(Q_{i}^{t}\) and uses a single charge formulation for strong, moderate and weak regions of inversion. A more physically based model is the SP2001 model which is based on a surface potential formulation [66].

Physics based modeling of HFETs is more complicated than that of a MOSFET in some aspects. As mentioned earlier, description of charge control in an HFET is complicated by the quantized nature of the electron gas and a lower confinement of charge. An accurate solution of the sheet charge density \(n_s\) requires a self-consistent solution of the Poisson’s and 1-D Schrodinger’s equation. This is not a feasible approach for implementation in a circuit simulator and hence, various approximations have been suggested and used in modeling HFET’s. The commonly used approximations are linear in nature such as the one proposed by Delagebeaudeuf et. al., [67].

### 2.6 Modeling of GaN FET’s

Several large signal models of GaN HFET’s have been developed using popular compact models such as BSIM3 [54], [2], modified Angelov [53] and Cubic Curtice [55]. These works incorporate RC subnetworks to handle dispersion related time constants and thermal effects.

A physics-based model for GaN MESFET’s that includes dispersion effects has been proposed by Islam et. al. [49]. In this model, the authors attribute current collapse in MESFET’s to buffer layer trapping and propose the formation of a second depletion layer due to trapped charge that develops underneath the channel; in effect acting as a second gate that constricts the channel and reduces the drive current.

Albrecht et. al. developed a model in which the divides the source to drain region was divided into 5 distinct regions and charge balance equations relevant to each part of the channel were applied[60]. This model requires iterations to find a solution for the current-voltage and capacitance-voltage characteristics making it unsuitable for circuit design and simulations. However, it does provide very useful information for device design with the knowledge of a few physical parameters of the device without having to resort to full 2D
device simulations.

Charge control models based on the linear approximation have been developed for AlGaN/GaN HFET’s taking polarization induced charges into consideration [56] - [58]. The model developed in this work is also based on a linear charge control equation and is extended by taking velocity saturation and self heating into account.

2.6.1 Thermal Modeling

In semiconductor devices, thermal effects arise out of the Joule heating due to electrical power dissipation in the channel. This introduces a feedback mechanism into the characteristics of the device wherein increased heating degrades the drain current drive, which in turn, leads to a lower temperature rise. In a circuit simulator, this is implemented as an additional node in the device model so that the temperature rise is solved self consistently with electrical network.

Heat Flow Equation

In steady state, the general heat flow equation is given as

$$\nabla \cdot k(T) \nabla T(x, y, z) = -P(x, y, z)$$

(2.13)

where \( k \) is the thermal conductivity and \( P \) is the power density. If the thermal conductivity is assumed to be constant (independent of temperature) the equation reduces to Laplace’s equation

$$\nabla^2 T = -\frac{P}{k}$$

(2.14)

This equation can be solved analytically for a few geometries and boundary conditions. Such solutions have assumed the active channel area of the device as a rectangular, spherical or cylindrical heat source to come up with close form analytical expressions for the thermal resistance. Generally, the side walls are assumed to be adiabatic and heat transfer is allowed only through the substrate backside contact or the top surface. One of the popular compact analytical expressions was proposed by Cooke [61] and is given as

$$R_{TH} = \frac{1}{W_{diss}k} \frac{1}{\frac{2\pi(N-1)}{\ln M} - \frac{\pi(N-2)}{\ln P}}$$

(2.15)
where

$$M = \frac{2 \left[ \cosh \pi \frac{L_{ff} + L_{diss}}{4t_{chip}} \right]^{1/2} + 1}{\cosh \pi \frac{L_{ff} - L_{diss}}{4t_{chip}}} \left[ \cosh \pi \frac{L_{ff} + L_{diss}}{4t_{chip}} \right]^{1/2} - 1}$$

$$P = 2 \left( \frac{1 + \text{sech} \pi \frac{L_{diss}}{4t_{chip}}}{1 - \text{sech} \pi \frac{L_{diss}}{4t_{chip}}} \right)^{1/2}$$

(2.16)

(2.17)

Here $L_{diss}$ and $W_{diss}$ are the length and width of the gate fingers which are assumed to be the heat sources in the system. $L_{ff}$ is the gate finger pitch and $t_{chip}$ is the thickness of the substrate. One assumption made here is that the thickness of the substrate is much larger than the active device area thickness. This expression has been used successfully to calculate the thermal resistance in the large signal model developed in [55].

In general, the thermal conductivity of a material also depends on temperature and it can be approximated by

$$\kappa(T) = aT^b$$

(2.18)

where $a$ and $b$ are fitting parameters that are defined for different materials. As a result, the heat flow equation becomes nonlinear. Kirchoff’s transformation can be applied to linearize the equation. Based on this, Joyce showed that the transform temperature is related to the actual temperature as

$$T_{fic} = T_0 + \frac{1}{\kappa_0} \int \kappa T dT$$

(2.19)

Putting 2.18 in 2.19 and integrating we get

$$T_{act} = \left( \frac{\kappa_0(b+1)}{a} \right) (T_{fic} - T_0) + T_0^b + \frac{1}{b+1}$$

(2.20)

In device models, thermal effects are included by using a thermal subnetwork (see figure 2.5). The thermal resistance $R_{TH}$ gives the rise in channel temperature as

$$T_o = T_a + R_{TH} \cdot I_{DS} \cdot V_{DS}$$

(2.21)

The capacitance $C_{TH}$ is derived from measuring the time constants of the thermal transient in the device. It represents the amount of time taken by the system to reach thermal equilibrium and depends on the heat capacity of the material. Any number of subnetworks
Figure 2.5: Large signal model of a FET with (a) Dispersion subnetwork represented by $I_{\text{rf}}$, $R_{\text{rf}}$ and $C_{\text{rf}}$ and (b) Thermal subnetwork $R_{\text{th}}$ and $C_{\text{th}}$

can be used based on the observed time constants and expected physical structure of the device. However, most devices are modeled well using a single time constant representing the dominant one [62]. A standard large signal model of FETs including subnetworks for the dispersion and thermal effects is shown in figure 2.5.

2.7 Thermal Characterization of GaN FET’s

There are various ways of measuring the temperature in a device. The liquid crystal technique is based on an observed change in the polarization of reflected light of liquid crystals when they undergo a change from aligned to random state at a known temperature. This method was used in [22] to estimate the temperature of AlGaN/GaN HFETs on Si and
SiC. The limitations to this method are that the temperature resolution of the measurement is limited by the number of distinct liquid crystals available for measurement and the spatial resolution is limited by the size of the crystals (usually of the order of 1µm). Another popular method to measure temperature is the infrared imaging system. These systems are also limited in their resolution and measurement of channel temperatures which are less than 1µm.

Electrical characterization methods can also be used to estimate channel temperature. Pulsed IV measurement is one of the popular techniques in which the pulsing time and initial conditions can be varied to achieve a high degree of control over observed thermal and trapping related transients. Appropriate initial bias points can be selected to minimize one of the effects (thermal or trapping) while measuring the other. For example, pulsing from an initial bias point of \( V_{gs} = 0 \) and \( V_{ds} = 0 \) should minimize trapping effects at the gate to drain surface region and bulk trapping effects. Transient drain current can be measured under these conditions over a range of temperatures to calibrate the effect of temperature on the current. The method employed by Kuznik et. al. estimates the drain current drop at an increased temperature as

\[
\Delta I_{sat}(V_D) = -g_m (I_{sat} \Delta R_S + \Delta V_T) + I_{sat} \Delta v_{sat} / v_{sat} + V_D / R_{sub}
\]  

(2.22)

where \( \Delta R_s, \Delta V_T \) and \( \Delta v_{sat} \) are temperature driven changes in the source resistance, threshold voltage and electron saturation velocity respectively. \( R_{sub} \) represents the buffer layer leakage which can be neglected under normal operating conditions. The change in \( R_S \) is related to a decrease in the electron mobility with temperature. The authors assume that the change in threshold voltage \( \Delta V_T \) under pulsed bias conditions is related to the buffer layer trapping and neglect it by selecting HFETs that did not show a change in threshold voltage. Finally, the change in saturation velocity \( \Delta v_{sat} \) is also neglected with an error of 10%. With these approximations, \( \Delta I_{sat} \) can be expressed as

\[
\Delta I_{sat}(t) = -g_m I_{sat} \Delta R_S
\]  

(2.23)

To calibrate the dependence of \( \Delta R_S \) on temperature, I-V characteristics are measured over a range of temperatures at a low drain bias so that self-heating is minimized.

In our study we have used electrical characterization methods to estimate channel temperature and then compared it to the temperature predicted by the model. This method is based on a reconstruction of the current voltage characteristics using high frequency
output conductance extracted from S parameter measurements. At the typical frequencies where S parameters are measured, thermal effects are not able to respond and hence we can estimate the expected drive current without self heating. The details of this method are discussed in chapter 5.

2.8 Characterization of Dispersion Related Elements

Dispersion effects are characterized by pulsed bias measurements. These effects are represented in the large signal model by the $I_{rf}$, $R_{rf}$ and $C_{rf}$ elements as shown in figure 2.5. Low frequency measurements below 1MHz are used to determine the low frequency transconductance and output conductance. The ratio of low and high frequency values of transconductance and output conductance is used to determine the dispersion network elements.

A general methodology to develop and extract a large signal model is shown in figure 2.6. This work focuses on the small signal extraction procedures for the AlGaN/InGaN MOS-HFET and development of the intrinsic charge control model for the device along with the investigation of self heating in the device.
2.9 Contributions of this work

This work has focused on the characterization and modeling of AlGaN/InGaN MOS-HFETs. The overall goal of this research is to develop physics based models and an understanding of device operation in order to optimize device performance and explore circuit applications for these devices. A comprehensive modeling strategy to extract equivalent circuit parameters of the FETs has been developed. A technique to extract bias dependent source and drain series resistances has been developed and implemented.

The large signal model developed in this work uses the linear charge control approximation [67, 3]. In addition to the DC current-voltage modeling, a charge based capacitance model has been developed and compared to extracted small signal parameters from measured S parameter data. Transport in the channel takes into account drift currents and uses a quasi 2D Poisson solution to model velocity saturation in the channel. Thermal effects have been included by using a temperature dependent expression for low field mobility. Thermal resistance is calculated using the well known Cooke’s expression [61].

An equivalent circuit model was extracted for the AlGaN/InGaN MOS varactor. Extraction techniques have been outlined for the device using analytical expressions. A charge control model was developed to model the device capacitance. This model utilizes the triangular well approximation to calculate channel sheet charge and gate capacitance as a function of gate bias.

Finally, n-i-n structures with low temperature epitaxially re-grown source drain contacts were characterized. These structures are used as a test vehicle to ensure the efficacy of the re-growth process in order to fabricate carrier rich source drain regions for enhancement mode GaN MOSFETs.
References


[9] B. Jogai, “Free electron distribution in AlGaN/GaN heterojunction field-effect transis-

[10] J. C. Freeman, “Basic equations for the modeling of Gallium Nitride(GaN) high elec-

polarization effects on the output characteristics of AlGaN/GaN heterojunction modu-
450-457.

“Polarization effects, surface states and the source of electrons in AlGaN/GaN het-
250-252.


[17] R.J. Trew, “SiC and GaN Transistors - Is there one winner for Microwave power ap-

SiC for low noise applications,” *58th Device Research Conference. Conference Digest*,

teristics of AlGaN/GaN HEMTs on SiC substrates for broad-band low-noise amplifiers,”


[44] V.V. Afanas’ev, A. Stesmans, M. Passlack, and N. Medendorp, “Band offsets at the interfaces of GaAs(100) with Gd_xGa_{0.4}O_{0.6} insulators,” Applied Physics Letters, Vol. 85, No. 6, 2004, pp. 597-599.


Chapter 3

AlGaN/InGaN Heterojunction MOS Capacitor

3.1 Introduction

High frequency, small signal characterization and modeling of an AlGaN/InGaN heterojunction varactor is presented in this chapter. These devices include an oxide layer between the gate metal and the AlGaN barrier layer. The presence of an oxide layer is important to reduce gate currents, allowing the gate to be driven into forward bias, while maintaining control over the channel; therefore devices were biased from a negative gate bias of -8V to 6V. The extended operating range of these devices presented significant modeling challenges to be discussed in the chapter. A piecewise linear equivalent circuit model was developed based on the physics of the device. A physics based model has also been developed to study the charge control in these devices and to verify the gate capacitance extracted from the equivalent circuit model. This model is employed to study the impact of device parameters on charge control in the device.

Results from these devices indicated the presence of an interface with a low density of interface states that leads to the formation of an unpinned accumulation layer in forward bias.
3.2 The MOS Capacitor

A brief overview of the metal oxide semiconductor (MOS) capacitance structure is provided in this section. The discussion starts off by going through the model of a MOS varactor on a homogeneous semiconductor such as silicon. After the model is developed, the heterojunction device is compared and the model is extended to take into account the peculiarities of the system.

The MOS capacitor is a very important tool in understanding the performance of a gate dielectric. CV (capacitance voltage) characterization is used to gather various kinds of information about the metal-oxide-semiconductor system such as the flat band voltage ($V_{FB}$), doping density in the semiconductor ($N_D$), equivalent oxide thickness (EOT) and insulator dielectric constant ($\epsilon_{ox}$). Generally, these characterizations are carried out using quasi-static (low frequency) and high frequency (1 MHz) signals. A simple series RC model is sufficient to represent the characteristics of an ideal MOS capacitor. However, in the presence of gate leakage a parallel resistance is included in the circuit to model the leakage path through the dielectric. As gate leakage increases, it becomes necessary to increase the characterization frequency in order to resolve the capacitance of the structure [2]. In other words, as the leakage increases the parallel resistance decreases and will start to dominate the observed impedance of the parallel RC combination. To overcome this, the characterization frequency can be increased which will lead to lower value of impedance for the capacitor ($Z_{cap} = 1/(j\omega C)$) and hence, the capacitance can be measured once again. Based on the simple parallel RC model we can derive an approximate frequency limit required to characterize the gate capacitance based on the admittance of the circuit

$$Y_{||} = \frac{1}{R_g} + j\omega C_g$$

(3.1)

To observe the effects of the capacitance $\omega C_g$ has to be much greater than $1/R_g$. This gives us a very approximate lower limit on the frequency of characterization

$$\omega_c > \frac{1}{R_g C_g}$$

(3.2)

3.3 Experimental Setup

The characterized MOS varactor devices were RF structures with coplanar waveguide (CPW) pads. These devices were setup in a two port configuration with the drain
and source shorted (shown in figure 3.1). The underlying III Nitride HFET consisted of 30nm InGaN channel beneath a 20nm AlGaN donor layer uniformly doped with silicon to $1 \times 10^{18} \text{cm}^{-3}$. The III-N epilayers include a 500nm GaN buffer layer and were deposited by metal organic chemical vapor deposition (MOCVD) on sapphire. MOS DHFET devices with gate lengths of (Lg=1.4 µm) were fabricated using standard III-N processing methods. Titanium/aluminum/titanium/gold and nickel were ohmic source-drain and insulating gate contacts respectively.

Figure 3.2 shows the measured gate current of a 4 finger 25 µm unit width (4x25) MOSCAP device. As shown, in forward bias, the gate current at 5V is approximately 50 mA which is a very significant amount of leakage. As a rough estimate, this results in a leakage resistance of 100 ohms. Given the oxide thickness of 120 Å, gate width of 100 µm and gate length of 1.4µm, the oxide dielectric constant was estimated to be 8.3. Based on these values for gate resistance and capacitance, we can estimate the required frequency to characterize the gate capacitance as 10 GHz. The devices were characterized using an Agilent 4142 DC source and the 8510 Network Analyzer (figure 3.3). The DC source has a medium power SMU with a 100 mA rating which was used to drive the input port on the devices while the high power SMU with a 1A rating was used to bias the output.
Figure 3.2: Measured gate current of a 4x25 μm device with L_g=1.4μm.

Figure 3.3: DC and small signal measurement setup used to characterize all devices in this study.
In case of the capacitors being discussed here, the output port DC voltage was always set to 0V. The network analyzer had a 45 MHz to 26.5 GHz measurement range. The characterized devices use coplanar pads and GSG probes were used. Short Open Load Thru (SOLT) calibration standards provided with the probes were used to calibrate the system before measurement. The devices were characterized from 45 MHz to 10.05 GHz based on the results of the rough calculation shown above.

Instruments were controlled on a Windows PC using a utility developed in LABVIEW. The utility allows nested sweeping to sweep the gate/base bias as well as the drain/collector bias while performing S parameter measurements at each bias point. The DC data is saved as a text file which was imported into Excel for analysis. S parameter data can be downloaded either in the Touchstone or Citifile format for importing into ADS. Equivalent circuit parameter extraction was performed in ADS.

### 3.4 Equivalent Circuit Model

As mentioned above, a leaky gate dielectric can be modeled by a parallel RC block with a series resistance representing loss through the path. Additionally at high frequencies, parasitics arising from the transmission line effect of RF pads has to be included in the form of pad capacitances and inductances. All the elements have to be determined in order to be able to accurately model the measured S parameters.

In order to interpret the measured results and develop an equivalent circuit model for this device it is instructive to understand the physical processes occurring in the structure. At low gate bias values (large negative bias on the gate), the channel is essentially pinched off with both the AlGaN and InGaN layers being depleted. Under this condition, the device should have a very small gate capacitance because of the series connection of the oxide, AlGaN depletion layer and InGaN depletion layer. As the gate capacitance is increased beyond threshold (the gate bias at which charge starts accumulating in the quantum well formed by the heterojunction), a conducting sheet charge starts forming at the AlGaN/InGaN interface. During the formation of this sheet charge, we would expect a localized current to flow into the quantum well as a function of the gate bias. Additionally, the high frequency perturbation superimposed on the DC bias would modulate this charge giving rise to a capacitance associated with the sheet charge. This picture provides us an
Figure 3.4: Extracted input impedance of the MOS capacitor as a function of frequency. The behavior of the capacitor changes between a gate bias of (a)-7V and (b)4V.

The equivalent circuit consisting of a parallel RC block at the heterojunction at the interface of the AlGaN/InGaN layer. With increasing bias, the sheet charge density increases rapidly which leads to a decreasing value for the parallel resistance associated with this interface (referred to as R\text{sec} from here on). Simultaneously, the capacitance associated with the sheet charge increases rapidly as the charge layer is formed. This may be attributed to the modulation of the depletion region in the InGaN layer. As this is going on, the remaining part of intrinsic device between the gate contact and the two dimensional electron gas (2DEG) is essentially a depleted layer of AlGaN with an associated resistance in series with the gate oxide and its resistance, essentially another parallel RC block. This is displayed in figure 3.5(a).

Beyond the bias at which the sheet charge has been fully confined inside the quantum well, the device can be represented as a single RC block representing the depletion and oxide capacitance and its associated leakage path. With sufficiently high bias on the gate, real space transfer of charge starts into the AlGaN layer. This will lead to a reduction in the depletion width and the capacitance is expected to increase with increasing bias (shown in figure 3.5(b)). Finally, as the free charge in the AlGaN barrier layer starts accumulating underneath the gate oxide (assuming a good semiconductor dielectric interface), we would expect the capacitance to stabilize at the value representing the oxide capacitance. This is depicted in figure 3.5(c). Input impedance of the device can be calculated from two port measurements by using

\[
Z_{IN} = \frac{1}{Y_{11}}
\]

(3.3)

where \( Y_{11} \) is the input admittance of port 1. The real part of \( Z_{IN} \) is shown in figure 3.4 as a
function of frequency. The plots clearly show the variation in behavior of input impedance with bias. At a gate bias of -7V the impedance cannot be represented by a single parallel RC block whereas at a bias of 4V it shows the low pass characteristics expected from a series parallel RC block. This corroborates with the equivalent circuit model that has been developed based on device behavior.

### 3.4.1 Parameter Extraction

The equivalent circuit model developed above can be extracted using analytical expressions developed for a series parallel RC circuit beyond a gate bias of -6V because the device is represented by a single RC block. In this bias range, the input impedance can be written as

\[
Z_{11} = R_s + \frac{R_p}{1 + \frac{\omega^2 R_p^2 C_p^2}{1 + \frac{\omega^2 R_p^2 C_p^2}{1 + \frac{\omega^2 R_p^2 C_p^2}{}}}}
\]  
(3.4)

However, close to pinch off there are two parallel RC blocks in the equivalent circuit and this implies that the presence of gate leakage and series resistance complicates the extraction procedure to an extent. In this case, the two blocks have to be extracted one after the other. In the first pass, the dominant block is extracted by assuming that the circuit is represented by a single RC section. Following this, the extracted RC time constant can be subtracted from the input impedance of the device. The residue gives a good estimate of the second RC block which can be extracted using the single RC section expressions. Once the two RC blocks have been extracted, they are optimized along with the series resistance and the parasitic capacitance and inductance to get a good fit to the measured S-parameter data. Although this procedure involves some optimization to achieve a good fit, it still follows an analytical procedure in order to get an initial estimate of the elements, thereby increasing chances of obtaining a reasonable solution post optimization. The measured and modeled S-parameters are shown in figure 3.6 at two gate bias points. An accurate fit to the measured S-parameters is obtained in both extremes of operation.

### 3.5 Results and Discussion

The value of extracted inductance post optimization was 125 pH. This includes the inductance and ports one and two as they are in series and cannot be separated out. Gate
and source pad capacitances were estimated to be 6 pF and 16 pF respectively. Extracted values of all elements in the equivalent circuit model are shown as a function of gate bias in figure 3.7. The gate capacitance shown in 3.7(a) increases till the electron gas sheet charge forms and then stabilizes at 350 fF. This represents the depletion layer capacitance of the device. Beyond a gate bias of -2V the capacitance starts rising once again and stabilizes at 850 fF. As mentioned previously, using this value of oxide capacitance the dielectric constant of the oxide is estimated to be 8.3. Other parameters modeling the intrinsic device behave as expected based on the model developed. The series resistance decreases once the electron gas forms and stays constant until real space transfer into the barrier layer pushes the electrons into a high resistance region. This is a unique aspect in the modeling of MOS-DHFETs because the gate is pushed well into forward bias causing current conduction in regions with different conductivity. This has to be taken into account while modeling FETs.

### 3.5.1 Charge Density

From the extracted CV curve, sheet charge density can be estimated by

\[ n_s = \int C dV \]  

(3.5)

The integration is carried out over the voltages where capacitance is constant with bias. Using this, \( n_s \) in the 2DEG was estimated as \( 4.8 \times 10^{12} \) cm\(^{-2} \). In forward bias, the charge density in accumulation layer is equal to \( 7.6 \times 10^{12} \) cm\(^{-2} \). With a 2x higher density in the accumulation channel, the current density in forward bias will be 2x that of the current density in HFET mode of operation. This is more accurate at high drain bias where the electrons are velocity saturated and the difference in low field mobility between the two dimensional electron gas and bulk AlGaN is not a factor in determining \( I_{DS} \).

### 3.6 Physics based model for the Gate Capacitance

A model for the capacitance of the device has been developed under the HFET mode of operation. In this mode the device is primarily defined by modulation of charge at the hetero-interface between \( \text{Al}_x\text{Ga}_{1-x}\text{N} \) and \( \text{In}_x\text{Ga}_{1-x}\text{N} \). The MOSFET mode of operation has been modeled separately by using Fermi statistics in the \( \text{Al}_x\text{Ga}_{1-x}\text{N} \) layer by ignoring
the modulation of charge at the heterojunction. The assumptions used in modeling the capacitance of the varactor in HFET mode of operation are as follows:

1. Charge modulation in the parasitic In$_x$Ga$_{1-x}$N layer is ignored. This leads to an underestimation of capacitance in the sub-threshold region. In the devices characterized in this study, the InGaN layer is doped to $2 \times 10^{17}$ cm$^{-3}$ and is expected to exhibit significant deviation close to turn on. Well designed devices are expected to have much lower doping levels in order to minimize parasitic leakage in the off state.

2. Sheet charge in the quantum well is calculated by assuming that the barrier layer is fully depleted. This value of sheet charge forms the basis of analysis that calculates charges in the barrier layer and electric field at the gate. This approximation breaks down significant charge transfers into the barrier layer.

3. The quantum well is modeled using the triangular well approximation. This approximation is not accurate close to the sub-threshold region where the well broadens and carrier statistics are better represented by Boltzmann or Fermi functions. The approximation is also not valid once real space transfer starts into the GaN layer. Again, in this region it would be more appropriate to use Fermi statistics.

### 3.6.1 Model Development

An accurate solution for the charge in a quantum well at the hetero-interface requires a self-consistent solution of the Schroedinger and Poisson equations. Two dimensional confinement in the quantum well leads to quantization of electron states. The density of states for a two dimensional system with isotropic parabolic bands is $D(E) = \frac{4\pi m^*}{\hbar^2}$ and total sheet charge density in the quantum well can be written as:

$$n_s = DkT \left[ \ln \left( 1 + \exp \frac{E_f - E_0}{kT} \right) + \ln \left( 1 + \exp \frac{E_f - E_1}{kT} \right) \right]$$ (3.6)

where $E_0$ and $E_1$ are the lowest energy of the zeroth and first subbands, respectively. Under the assumption of a triangular potential well used in this work, the sub-band energies are given by Airy’s functions:

$$E_n = \left( \frac{\hbar^2}{2m} \right)^{1/3} \left( \frac{3}{2} \pi qF \right)^{2/3} \left( n + \frac{3}{4} \right)^{2/3}$$ (3.7)
where \( n=0,1 \) for the first two energy states and \( F \) is the electric field in the quantum well at the interface of the two materials.

Assuming the electron quasi Fermi level is constant in the semiconductor at equilibrium, we can write an energy balance equation relating the quasi Fermi level to applied gate bias (shown in figure 3.8). Taking the bottom of conduction band in the In\(_x\)Ga\(_{1-x}\)N layer at the AlGaN/InGaN interface as the reference energy level, we write down the following equation:

\[
\Delta E_c + qV_1 + qV_{ox} = E_F - qV_{gb} + \chi_{MS}
\]

where \( V_1 \) is the potential drop in the AlGaN barrier layer and \( V_{ox} \) is the drop in the oxide layer. \( V_1 \) and \( V_{ox} \) are calculated by solving Poisson’s equation in the barrier layer with appropriate boundary conditions.

As discussed in chapter 2, in presence of polarization Poisson’s equation has to be modified by considering the electric displacement vector rather than the electric field. The final equation is of the form:

\[
\nabla^2 \phi = \rho - \nabla \cdot \mathbf{P}
\]  

(3.9)

If the polarization is assumed to be position independent, the second term can be neglected. In this work, all layers are considered to be strained uniformly and hence have uniform polarization in the bulk. This assumption may not be valid in real devices due to different stress levels in different parts of the device structure [10]. Once the aforementioned assumption is made, the only region where polarization charge builds up is at the interfaces between the semiconductors and outside surfaces as calculated in chapter 2.

From a solution of the Poisson’s equation in the InGaN layer and neglecting the depletion region charge in the InGaN layer, we have

\[
n_s = \frac{\varepsilon_2 E_{i,2}}{q}
\]

(3.10)

where \( E_{i,2} \) is the electric field in the InGaN layer at the heterointerface. This establishes a relationship between the sheet charge density and the electric field which determines the energy levels in the quantum well. Denoting the electric field in the Al\(_x\)Ga\(_{1-x}\)N layer at the interface as \( E_{i,1} \), Gauss’s law can be applied to relate the electric fields as:

\[
E_{i,2} - E_{i,1} = \sigma_{12}
\]

(3.11)

where \( \sigma_{12} \) is the bound polarization sheet charge between the Al\(_x\)Ga\(_{1-x}\)N and In\(_x\)Ga\(_{1-x}\)N layers.
In order to write down Poisson’s equation in the Al\textsubscript{x}Ga\textsubscript{1−x}N barrier layer, we determine the ionized donor density and free electron concentration in the barrier layer as:

\begin{equation}
N_D^+ = \frac{N_D}{1 + 2 \exp \left( \frac{E_F-E_D}{k_BT} \right)} \tag{3.12}
\end{equation}

\begin{equation}
n_f = \frac{N_C}{0.27 + \exp \left( \frac{E_C-E_F}{k_BT} \right)} \tag{3.13}
\end{equation}

where \(N_D\) is the doping density in the AlGaN layer and \(N_C\) is the effective conduction band density of states. The expression for \(n_f\) is written using the Ehrenreich approximation for the fermi integral [6]. Taking the fermi level in the metal as reference (\(E_{Fm}=0\)) we can write the following expressions for the various energy levels:

\begin{equation}
E_F = q V_G \tag{3.14}
\end{equation}

\begin{equation}
E_C = E_{CO} - q \psi(x) \tag{3.15}
\end{equation}

\begin{equation}
E_D = E_{DO} - q \psi(x) \tag{3.16}
\end{equation}

\begin{equation}
E_{CO} = E_{DO} - E_d(x) \tag{3.18}
\end{equation}

where \(E_{CO}\) and \(E_{DO}\) are the conduction band energy level and donor energy level in Al\textsubscript{x}Ga\textsubscript{1−x}N in absence of the heterojunction and the gate. \(\psi(x)\) is the potential in the Al\textsubscript{x}Ga\textsubscript{1−x}N layer. All quantities are referred to the metal fermi level. Conduction band energy and donor energy levels are related to each other as [5]

\begin{equation}
E_{CO} = E_{DO} - E_d(x) \tag{3.18}
\end{equation}

where \(E_d\) is the donor ionization energy and is given as [1]

\begin{equation}
E_d(y) = \frac{13.6}{\left( \frac{m_{eff}}{m_0} \right)^2} \left( \frac{y}{T_0} \right)^2 \tag{3.19}
\end{equation}

All the energies and potentials referred to in these equations are shown in fig. 3.8.

Plugging these expressions into Poisson’s equation and integrating from the heterointerface to the oxide interface, we obtain the following expression for the electric field at the interface:

\begin{equation}
E_{AlGaN,oxide} = -\sqrt{E_{i,1}^2 + F1 + F2} \tag{3.20}
\end{equation}
where

\[ F_1 = N_D V_T \ln \left( \frac{\exp \left( -\frac{\psi_{\text{gate}}}{V_T} \right) + 2 \exp \left( \frac{V_G - E_{\text{DO}}}{V_T} \right)}{\exp \left( -\frac{\psi_{i,1}}{V_T} \right) + \exp \left( \frac{V_G - E_{\text{DO}}}{V_T} \right)} \right) \]  

(3.21)

\[ F_2 = N_C V_T \frac{0.27}{\ln \left( \frac{1 + 0.27 \exp \left( \frac{V_G + \psi_{\text{gate}} - E_{\text{DO}}}{V_T} \right)}{1 + 0.27 \exp \left( \frac{V_G + \psi_{i,1} - E_{\text{DO}}}{V_T} \right)} \right)} \]  

(3.22)

By taking the negative square root we are assuming that the conduction band in Al\(_x\)Ga\(_{1-x}\)N slopes upwards at the oxide interface. While this is valid in the HFET mode of operation, it may not be valid in the MOSFET mode of operation when the surface is expected to be in accumulation and slope down. Again, applying Gauss’s law at the AlGaN/oxide interface, the field in the oxide, \( E_{\text{ox}} \), is related to \( E_{\text{gate}} \) as

\[ \epsilon_1 E_{\text{AlGaN,oxide}} - \epsilon_{\text{ox}} E_{\text{ox}} = \sigma_{11} \]  

(3.23)

Assuming that the oxide is free of trapped charges, electric field is constant in the oxide. This give the relationship between gate charge and oxide field as

\[ Q_G = \epsilon_{\text{ox}} E_{\text{ox}} \]  

(3.24)

and the gate capacitance is given as

\[ C_G = \frac{\partial Q_G}{\partial V_G}. \]  

(3.25)

Using equations 3.23 and 3.25, and assuming that the polarization charge at the oxide/AlGaN interface is independent of gate bias, the gate capacitance, \( C_G \) is given as

\[ C_G = \epsilon_1 \frac{\partial E_{\text{AlGaN,oxide}}}{\partial V_G}. \]  

(3.26)

From here on we replace \( E_{\text{AlGaN,oxide}} \) with \( E_{\text{gate}} \) to shorten the expressions. Differentiating the electric field with respect to the gate voltage we reach a lengthy expression which can be written as:

\[ C_G = C_1 + C_2 + C_3 \]  

(3.27)

where

\[ C_1 = \frac{\epsilon_1}{E_{\text{gate}}} E_{i,1} \frac{\partial E_{i,1}}{\partial V_G}, \]  

(3.28)

\[ C_2 = \frac{q N_C}{E_{\text{gate}}} \left[ \frac{1}{0.27 + \exp \left( \frac{V_G + \psi_{\text{gate}} - E_{\text{DO}}}{V_T} \right)} - \frac{1}{0.27 + \exp \left( \frac{V_G + \psi_{i,1} - E_{\text{DO}}}{V_T} \right)} \right], \]  

(3.29)
\[ C_3 = \frac{qN_D}{E_{\text{gate}}} \left[ \frac{\exp\left(\frac{V_G - E_D}{V_T}\right)}{\exp\left(-\frac{\psi_{\text{gate}}}{V_T}\right) + 2 \exp\left(\frac{V_G - E_D}{V_T}\right)} \right]. \]  

(3.30)

To calculate the three capacitances, the conduction band energy in the AlGaN layer at the heterojunction and the oxide interface has to be determined with respect to the fermi level in the metal. From the band diagram (see figure 3.8), the two potentials can be expressed as:

\[ \psi_{i,1} = -V_G - \left(\frac{\Delta E_C - E_{F2}}{q}\right) \]  
(3.31)

\[ \psi_{\text{gate}} = -\chi MS - E_{\text{ox}1\text{ox}} \]  
(3.32)

Using equations 3.10 and 3.11 the electric field at the heterojunction \( E_{i,1} \) is:

\[ E_{i,1} = \frac{q\sigma}{\epsilon_1} - \frac{\sigma_{12}}{\epsilon_1} \]  
(3.33)

\( E_{F2} \) is referred to the bottom of the conduction band in the InGaN layer and is determined by solving the equations 3.6 and 3.8 simultaneously. Once \( \psi_{i,1} \) is determined \( \psi_{\text{gate}} \) is determined by simultaneously solving equations 3.32 and 3.20 using \( \psi_{\text{gate}} \) as the independent variable. This has to be done iteratively. With all the quantities determined, the gate capacitance is calculated as a function of gate bias.

### 3.7 Results and Discussion

The gate capacitance obtained from model is shown in figure 3.9. As we can see, the model matches extracted gate capacitance (see figure 3.7(a)) closely in the HFET mode of operation from a gate bias of -6V to -2V. Below -6V the capacitance deviates from extracted capacitance. This is because of the additional series capacitance of the depletion region in the InGaN layer that’s not taken into consideration here. The initial rise in gate capacitance is dominated by the narrowing of depletion region width. Eventually the InGaN layer is screened by the sheet charge at the interface.

The capacitance component \( C_1 \) is associated with the quantum well sheet charge. This capacitance can be further broken down into three components as shown in [4]. We investigate the behavior of these components to gain further insight. The capacitance of the sheet charge can be written as follows:

\[ C_{ns} = \frac{\partial n_s}{\partial V_G} \]  
(3.34)
Using equations 3.6 and 3.8, the gate capacitance arising from the sheet charge can be expressed as:

\[
\frac{\partial n_s}{\partial V_G} = \left( \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \right)
\]

(3.35)

where

\[
C_1 = \frac{1}{t_b} + \frac{\epsilon_{ox}}{\epsilon_2} 
\]

(3.36)

\[
C_2 = \frac{q^2 D}{t_b} \left( f(E_0) + f(E_1) \right)
\]

(3.37)

\[
C_3 = \frac{3}{2} \frac{q n_s^{1/3}}{\gamma_0 f(E_0) + \gamma_1 f(E_1)}
\]

(3.38)

where \( f(E_n) \) is the Fermi-Dirac function. \( C_1 \) is the capacitance of the barrier and oxide layers. As discussed in [4], \( C_2 \) can be interpreted as the variation of effective electron density per unit area in energy space. \( C_3 \) arises out of the variation of the distance of the charge centroid from the interface. The three capacitance terms are plotted in figure 3.10. As seen in the figure, the dominant capacitances close to threshold are \( C_2 \) and \( C_3 \).

1. We have neglected the charge in the InGaN layer which contributes an additional capacitance in the low gate voltage regime (close to the threshold voltage of the HFET). This reduces the effective gate capacitance because it is in series with the capacitance of the sheet charge.

2. Once we push the gate bias to the point where free charge density in the AlGaN barrier layer starts increasing significantly, the sheet charge density at the heterojunction starts to saturate. However this is not modeled by the equations used to determine the sheet charge density. In order to take this into account the fermi level \( E_{F2} \) measured with respect to the conduction band energy in the InGaN layer at the heterointerface has to be solved by taking the free charge in the barrier layer into account.

Eventually, the Fermi energy is pinned at a level determined by the device structure and the the sheet charge density at the heterointerface saturates, fixing the electric field in the AlGaN layer at the heterointerface.

To approximate these conditions, the sheet charge density can be represented using a polynomial function with two threshold voltages - the first one is the turn on voltage of the 2DEG whereas the second threshold voltage represents the gate voltage beyond which the sheet charge at the heterointerface is isolated from the gate. Beyond this point, free charge in the InGaN layer rises significantly and eventually forms an accumulation layer under the gate oxide.
3.8 Impact of Device Parameters on Charge Control

The gate capacitance model was utilized to study the impact of device parameters on charge control in the device. The parameters investigated were barrier layer doping density ($N_{D1}$), barrier thickness ($T_{\text{barrier}}$), oxide thickness ($T_{\text{ox}}$) and the Al, In mole fractions in the barrier and channel layers. In figure 3.11, threshold voltage is plotted against barrier layer doping density varying from $10^{15}$ cm$^{-3}$ to $10^{18}$ cm$^{-3}$. In the structure simulated, threshold voltage is fixed at -6.5V by polarization effects for doping densities below $10^{18}$ cm$^{-3}$. Figure 3.12 indicates the dependence of gate capacitance on barrier layer doping. Decreasing doping density to intrinsic levels ($10^{15}$ cm$^{-3}$) increases the effective gate swing over which capacitance stays constant (-4V to 2V). The effective gain in voltage swing in comparison to a device with doping density of $10^{18}$ cm$^{-3}$ is approximately 2V. This is desirable for increasing the linear operating range of the MOS-HFET. The impact of barrier layer thickness on gate capacitance is shown in figure 3.13 for a doping density of $10^{15}$ cm$^{-3}$. Decreasing thickness increases the gate capacitance but reduces gate voltage swing due to a decrease in threshold voltage. The real space transfer threshold is not impacted. In effect, voltage swing is traded off for gate capacitance. Oxide thickness has a smaller impact on threshold voltage and a negligible change in gate capacitance is predicted by the model (refer figure 3.14). Oxide thickness is expected to dominate capacitance in accumulation, where charge is located underneath the gate dielectric. Figures 3.16 and 3.15, indicate the significant impact of Al and In mole fraction on threshold voltage. The threshold voltage changes approximately by 5V for a 10% change in molefraction due to a change in polarization charge density accumulated at the interface. Based on the simulations, it is inferred that real space transfer threshold is impacted by barrier layer doping while other parameters mainly impact threshold voltage of the device. This can be used to design a MOS-HFET with linear charge control characteristics.

3.9 Summary

An equivalent circuit model for the capacitance of an AlGaN/InGaN MOS-HFET was developed in this chapter and the extracted gate capacitance indicates formation of an accumulation layer underneath the gate in forward bias. The charge control model was used to simulate gate capacitance of the device while varying device parameters. Based on
simulations, using an intrinsic layer would be preferable for improving linear charge control characteristics in the MOS-HFET. Other parameters can be adjusted for the required threshold voltage and gate capacitance.
Figure 3.5: Model developed based on the physical processes occurring in the device with varying gate bias.
Figure 3.6: Measured and modeled S-parameters of the 4x25 µm capacitor.
Figure 3.7: Extracted values of (a)\(C_g\) and (b)\(R_g\) (c)\(C_{sec}\) (d)\(R_{sec}\) (e)\(R_{series}\) for a 4x25 \(\mu\)m device.
Figure 3.8: Band diagram showing the potential and energies used in the analysis.

Figure 3.9: Capacitance of the AlGaN/InGaN MOS Varactor as predicted by the model (solid line). Red squares are the extracted data points from the equivalent circuit model.
Figure 3.10: Capacitance components associated with the sheet charge at the heterointerface. $C_G$ is the series combination of $C_1$, $C_2$ and $C_3$ which are the components as defined in equations 3.36, 3.37 and 3.38.

Figure 3.11: Threshold voltage is plotted against barrier layer doping density. For doping levels lower than $10^{18}$ cm$^{-3}$, threshold voltage is dominated by polarization effects.
Figure 3.12: Gate capacitance is plotted for three different values of doping density in the barrier layer. The lowest doping \( (N_{D1} = 10^{15} \text{ cm}^{-3}) \) exhibits the largest voltage swing over which gate capacitance stays constant.

Figure 3.13: Gate capacitance plotted for barrier thicknesses varying from 100 Å (minimum threshold voltage) to 300 Å (maximum threshold voltage). Maximum and minimum refer to the absolute value of threshold voltage.
Figure 3.14: Gate capacitance plotted for barrier thicknesses varying from 20 $\text{A}^\circ$ (minimum threshold voltage) to 100 $\text{A}^\circ$ (maximum threshold voltage). Maximum and minimum refer to the absolute value of threshold voltage.
Figure 3.15: Gate capacitance plotted for Indium mole fraction varying from 2% (minimum threshold voltage) to 8% (maximum threshold voltage). The doping density and Al mole fraction are fixed at $10^{15}$ cm$^{-3}$ and 15%. Threshold voltage changes by 5V. Maximum and minimum refer to the absolute value of threshold voltage.
Figure 3.16: Gate capacitance plotted for Aluminum mole fraction varying from 10% (minimum threshold voltage) to 20% (maximum threshold voltage). The doping density and In mole fraction are fixed at $10^{15} \text{ cm}^{-3}$ and 5%. Threshold voltage changes by 5V. Maximum and minimum refer to the absolute value of threshold voltage.
References


Chapter 4

Small Signal Modeling of

AlGaN/InGaN MOS Heterojunction FETs

This chapter presents the development of equivalent circuit models for FET’s and then discusses methodology followed in extracting the equivalent circuit parameters (ECPs) of AlGaN/InGaN/GaN metal oxide semiconductor (MOS) double heterojunction field effect transistors (DHFETs). The cross section of these devices is the same as that of the MOS capacitor that was shown in chapter 3 (see figure 3.1(a)). The RF structure of these devices is shown in figure 4.1; the location of probe tips is drawn in the figure.

4.1 Measurement Calibration

The most important step in generating high-frequency device models using measured S-parameters is accurate calibration of the vector network analyzer (VNA). VNA calibrations can be performed either “off-wafer” or “on-wafer” depending on whether the calibration standards are located on the same substrate as the devices or on a different cal-
Figure 4.1: Layout of the MOS-DHFET devices that were characterized in this study. The location of GSG probes during measurements is shown.

ibration substrate. On-wafer calibration brings the reference plane of measurement up to the device input, shown as planes BB’ in figure 4.1. With off-wafer calibration, the reference plane is located at the probe tips (AA’ in figure 4.1) and during subsequent analysis, the transmission line effects of the pad have to be de-embedded in order to be able to model the device itself. This is a critical step in generating device models for high-frequency applications because the device used in a circuit is devoid of any pad related effects. Transmission lines are often represented by a lumped element capacitor-inductor equivalent circuit. This representation is accurate up to a certain cut-off frequency beyond which the approximation becomes inaccurate. As the pads become larger, the associated cut-off frequency becomes smaller and thus significant high-frequency errors can creep into the modeling process.

The die’s on which devices were located did not have any on-wafer calibration standards available. Therefore, off-wafer SOLT calibration standards provided with the probes were used. In such a case, the pads can be de-embedded by using open and short pad structures on the measurement die. After calibration, the open and short structures are measured before characterizing the devices and then the measured S-parameters can be
deembedded using the following relations

\[ Y_{DUT\,open} = Y_{DUT} - Y_{OPEN} \]  
\[ Y_{SHORT\,open} = Y_{SHORT} - Y_{OPEN} \]  
\[ Z_{DUT\,deembed} = Z_{DUT\,open} - Z_{SHORT\,open} \]

For the measurements analyzed in this work, there were no deembedding structures present on the die either. Another option would be to perform an electromagnetic simulation of the pad structure and to use the s-parameters generated from simulation to deembed the pads. Extracted values of extrinsic elements in this work include the effects of pad parasitics.

### 4.2 Model Derivation

Equivalent circuit models provide a wealth of information about the intrinsic device as well as the parasitic elements that hinder device performance. The parameters are extracted over the range of biases under which the device is expected to operate. The most common usage of this information is to extract parameters of large signal models for devices. Another useful application of small signal parameters is in keeping track of process variations that can be caught early if the correct models are implemented. This section reviews the high frequency equivalent circuits used to model FET’s.

The intrinsic device is essentially the same for all FET’s with the differences in channel control primarily showing up in the bias variation of the capacitance and conductance parameters. However, the extrinsic (also known as parasitic) network can vary significantly depending on (i) physical structure of the device and (ii) frequency up to which the models are expected to be valid. As the frequency range of operation becomes higher, distributed effects become more significant and an increasing number of elements have to be included to model the electrical characteristics of the manifolds, substrate and access regions. All devices modeled in this work had unity gain cutoff frequencies \( f_T \) less than 15 GHz and hence, the frequency of characterization and modeling was well within the range in which the standard models are accurate. The model used in this study is shown in figure 4.2.
4.2.1 Extrinsic FET Model

The extrinsic elements in a FET model come from the pads, source and drain contacts and access regions, gate metallization and the source airbridge. This is shown in figure 4.3.

Inductances

Three inductances - $L_s$, $L_d$ and $L_g$ are included in the model. $L_s$ mainly comes from the inductance of the source metallization. Since this is a large piece of metal, the source inductance is usually the smallest of all three inductances. The source inductance will vary with the number of fingers in the device.

The drain inductance, $L_d$ represents the inductance of the output manifold metallization and the drain finger metallization. If the pads have not been de-embedded prior to extrinsic extraction the drain inductance will also include the output pad inductance from the reference plane located at the probe tip.

$L_g$, the gate inductance, is dominated by inductance of the metallization on the gate finger. It also includes contribution from the input manifold. Input pad inductance is included in $L_g$ if the pad has not been deembedded prior to ECP extraction.
Figure 4.3: This figure shows the cross section of a FET and relates the extrinsic parameters in the small signal equivalent circuit of a FET to their physical origin.

**Scaling of Inductances**

The gate inductance scales proportional to the unit gate width and inversely proportional to the number of parallel gate fingers and to determine the exact scaling factor a matrix of devices with different gate widths and number of fingers can be measured and then an empirical relation can be derived. In order to ensure repeatability, the pads should use probing marks. Such a method was used by Wood et al. [3] to derive the scaling of gate inductance as

$$L_g = \frac{L_{go} \times UW}{F^2}$$  \hspace{1cm} (4.4)

where UW is the unit width of the gate finger and F is the number of fingers. The drain inductance scales linearly with the unit gate width and inversely with the number of parallel drain fingers.

$$L_d \propto \frac{L_{do}}{\sqrt{F}} \times \frac{(\Delta \text{width})}{(\Delta \text{fingers})}$$  \hspace{1cm} (4.5)

The source inductance scales directly with the number of gate fingers because the inductance is dominated by the length of the source metallization which increases as the number of fingers increases.
Capacitances

Extrinsic capacitances model transmission line effects of the pad manifolds as mentioned previously. They also model the inter-metallization capacitances within the intrinsic device. The capacitances can be broken down into those which scale with gate width and the ones that are independent of dimensions. Capacitances that are dependent on gate width originate in the device metallization and hence can be again broken down into the ones that are dependent on bias and the ones that are not. The bias dependent extrinsic capacitances are primarily influenced by the depletion layer underneath the metallization. It is hard to separate the capacitances that depend on gate bias from the ones that do not. However, a method to separate the capacitances that scale with device width was suggested by Anholt and Swirhun [4]. Devices of varying widths are measured and the extracted extrinsic capacitances at the same bias point are plotted against the device width. This plot should be a straight line and extrapolation of the line to zero gate width gives the true value of parasitic manifold capacitances.

Resistances

The source and drain series resistances can be broken down into the resistance of the contact, spreading resistance and access region resistance. In HFETs the access region resistances are the dominant sources. The access region resistance is dominant for power devices because the source and drain are displaced from the gate in order to increase breakdown voltage by decreasing the fields at gate edges. The source and drain resistance scaled inversely with unit gate width and can be given as

$$R_{d,s} = \frac{R_{\text{sheet}}}{\text{width}}$$  \hspace{1cm} (4.6)

where $R_{\text{sheet}}$ is the sheet resistance of channel. The gate resistance is distributed because charges enter the channel along the entire gate width. Using a transmission line approximation the gate resistance can be written as

$$R_G = \rho_G \frac{W_f^2}{3WLh}$$  \hspace{1cm} (4.7)

This is different from the resistance measured using the dc end to end resistance method where the gate resistance is given as

$$R_{G,dc} = \rho_G \frac{W}{Lh}$$  \hspace{1cm} (4.8)
where $\rho_g$ is the specific resistance of the gate metal, $L$ is the gate length, $h$ is the thickness of gate metallization, $W$ is the gate width and $W_f$ is the gate finger width. The Gate resistance scales as

$$R_g = \frac{R_{go} \times (UW)^2}{F} \quad (4.9)$$

### 4.2.2 Intrinsic Elements

Small signal model is an equivalent circuit representation of the intrinsic device. The elements are obtained by a linear analysis of the device current-voltage and charge-voltage relations at a given bias point. The elements are expressed as

$$G_m = \frac{\partial I_{ds}}{\partial V_{gs}}|_{V_{ds}=\text{constant}} \quad (4.10)$$

$$G_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}|_{V_{gs}=\text{constant}} \quad (4.11)$$

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}}|_{V_{ds}=\text{constant}} \quad (4.12)$$

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}}|_{V_{gs}=\text{constant}} \quad (4.13)$$

Where $Q_G$ is the charge in device channel that is under gate control. These equations form the basic relationship between small signal models and large signal models. They are also heavily used in developing physics based large signal models and will be revisited again in chapter 4.

$C_{gs}$ and $C_{gd}$ are arise from the charge controlled by the gate in the source and drain regions. This includes terms arising from the modulation of charges in the channel, depletion regions in the source and drain access regions and fringing capacitances. The output capacitance $C_{ds}$ models the parasitic capacitance between source and drain and should be a very small in active operation.

The output conductance of a device is $G_{ds}$. $R_{ds}$ or $R_o$ has been used when it has been referred to as the output resistance. In saturation the output conductance should be very small and independent of gate and drain bias. There is a significant difference between DC and RF output conductance because of thermal and dispersion effects in FETs.

The product of $G_m$ and $R_{ds}$ is an indicator of the small signal gain of a device and is one of the figures of merit (FOM) used to evaluate the usefulness of a device.

Another parameter included in a small signal model that becomes significant at microwave frequencies is the transconductance delay parameter $\tau$ (‘tau’). This parameter
is required to model the time taken by charge to distribute between the drain and source as gate voltage changes. At low frequencies the redistribution can be considered to be instantaneous but as the frequency increases, the time taken by charge to rearrange between is no longer negligible in comparison to the rate at which the input signal changes.

Ri is a parameter that is contentious in its origin. The most plausible reason for including it in an equivalent circuit is to model the non-quasi-static (NQS) effect of charging the the gate to source capacitance at high frequencies [17]. This can be visualized as the of the path followed by electrons while moving in and out of the conducting channel. Electrically, this parameter also influences the overall delay of the device through the $R_i C_{gs}$ time constant. The effect of $R_i$ is visible only above certain frequencies and cannot be determined accurately below the NQS regime.

**Scaling of Intrinsic Parameters**

Intrinsic capacitances, transconductance and output conductance scale directly with the gate width. The gate leakage resistances also scale directly with gate width because leakage current is proportional to gate area.

### 4.3 Extraction Procedure

Although extraction of the ECP’s is possible using global optimization algorithms, this method has several pitfalls. Firstly, the optimization process can take a long time depending on the amount of data being used to extract the elements. Secondly, there can be multiple sets of ECP’s which fit the measured data accurately and there is a good chance that the optimizer settles in local minima depending on the initial guess. Direct extraction procedure was used to extract all the small signal models in this study [1],[2]. This method relies on an accurate determination of the extrinsic elements because the intrinsic elements are calculated by de-embedding the intrinsic device from the complete model. The most commonly used procedure to extract extrinsics is the ColdFET extraction. In this method, the drain to source bias is kept at 0V while the gate is biased in two different regions:

1. Below pinch-off so that the intrinsic device is essentially a depleted region. This is known as the reverse coldfet measurement and allows extraction of the pad capaci-
tances.

2. Gate biased in the forward region so that the gate diode is on and the diode conductance effectively shorts out the capacitance. Commonly referred to as the forward coldfet measurement, series resistances and inductances are extracted from this characterization method.

In general, the series resistances cannot be determined uniquely just from the forward coldfet measurement because there are 3 equations and 4 unknowns (will be discussed in more detail in the next section). This means that one of the resistances has to be determined using other methods such as DC measurements or analytical calculations.

Methods that use just a single off-state measurement to measure all the parasitics have also been suggested [5] but this method is very sensitive to the accuracy of extraction of the parasitic capacitances because of their dominance of the measured characteristics. To extract inductances accurately, the devices should be measured to very high frequencies but the measurements in this work were up to 20 GHz and hence, the inductances could not be extracted accurately using this method.

![Depleted region](image)

Figure 4.4: Device cross section of a FET biased below pinch-off. This illustrates the origin of the equivalent circuit of a reverse coldfet measurement.

### 4.3.1 Reverse ColdFET

When a device is biased below pinch-off, the device is depleted throughout (see figure 4.4) and it can be represented as a capacitive network. If the devices are symmetric,
the depletion capacitance from gate to drain and gate to source will be equal. This is shown in figure 4.8. Under these conditions, if the Y parameters are considered at low frequencies so that the contribution of the inductor can be neglected, they can be written as

\[ Y_{11} = j\omega (C_{p_{gs}} + 2C_{dep}) \]  
(4.14)

\[ Y_{12} = Y_{21} = -j\omega C_{dep} \]  
(4.15)

\[ Y_{22} = j\omega (C_{p_{ds}} + C_{dep}) \]  
(4.16)

\[ Y_{22} = j\omega (C_{p_{ds}} + C_{dep}) \]  
(4.17)

From these equations one can derive the pad capacitances to be

\[ C_{p_{gs}} = \frac{imag(Y_{11} + 2Y_{12})}{\omega} \]  
(4.18)

\[ C_{p_{ds}} = \frac{imag(Y_{22} + 2Y_{12})}{\omega} \]  
(4.19)

Extracted values of the pad capacitances for a 2x65 µm device is shown in figure 4.6.

4.3.2 Forward ColdFET

With the gate forward biased heavily (above the gate turn on voltage), the depletion region underneath the gate becomes small and localized leading to a parallel RC block equivalent circuit representation for the gate. This is shown in figures 4.7 and 4.8. Although the gate resistance has been shown as a lumped resistance in the equivalent circuit, in reality it is distributed along the width of the gate. From the equivalent circuit
Figure 4.6: Extracted pad capacitances plotted against frequency.
Once the gate diode is fully on, $R_{\text{diode}}$ decreases exponentially while the gate capacitance increases more slowly. As a result, $\omega^2 C_d^2 R_d^2 \ll 1$ and the diode capacitance can be ignored to give

$$Z_{11} = R_g + R_s + \frac{R_d}{1 + \omega^2 C_d^2 R_d^2} + j\omega(L_g + L_s - \frac{R_d^2 C_d}{1 + \omega^2 C_d^2 R_d^2})$$ (4.20)

It should be noted here that for a MOS device, this extraction method has to be modified somewhat. Instead of the Schottky diode we have a fixed oxide capacitance at the gate and a leakage resistance associated with it. In these devices, the leakage was high at a gate bias of 5V (as discussed in chapter 2) and a similar expression as 4.21 can be derived. The other $Z$ parameters can be written in a straightforward manner

$$Z_{22} = R_d + R_s + R_c + \frac{R_c}{2} + j\omega(L_d + L_s)$$ (4.22)

As displayed above, there are 4 unknowns and three equations. For short channel devices $R_c$ is negligible in comparison to the parasitic resistances leaving us with three equations and three unknowns. These equations can be solved simultaneously to get estimates of the
Figure 4.8: Equivalent circuit of a FET in forward coldfet measurement.

Series resistances and inductances

\[ R_s = \text{real} (Z_{12}) \]  
\[ R_d = \text{real} (Z_{22} - Z_{12}) \]  
\[ R_g = \text{real} \left( Z_{11} - Z_{12} - \frac{1}{R_g} \right) \]  
\[ L_s = \text{imag} (Z_{12}) \]  
\[ L_d = \text{imag} (Z_{22} - Z_{12}) \]  

The extracted inductances are shown in figure 4.9. Extracted series resistances are shown in figure 4.10.

Although this discussion takes us through the proper extraction procedure for series parasitic elements, the MOS-DHFET device has a channel that varies spatially through different layers. Therefore, the drain and source resistances have to be optimized along with the intrinsic elements at each bias points. To ensure accuracy of the results, the values of intrinsic elements obtained from the optimization step were compared to the results from direct extraction. The optimized values of series resistances were inputs to the direct extraction step.
Figure 4.9: Extracted Inductances of a 2x65 $\mu$m device from forward ColdFET measurement at $V_g=2V$. 
Figure 4.10: Extracted series resistances of a 2x65 µm device from forward ColdFET measurement at $V_g=2V$. 
4.3.3 A second method to extract series resistances

An alternative method to extract bias dependent series resistances is presented here. The advantage of this approach is that it removes the optimization step from the extraction process and series resistances can be extracted over a wide range of gate biases using the Cold FET measurements. This is based on the work presented in [6]. In the cold FET condition, the intrinsic device is represented by an alternative equivalent circuit with parallel RC blocks between the three terminals as shown in figure 4.11. In this representation, we are neglecting the presence of leakage paths, $R_{gs}$ and $R_{gd}$. From the circuit, the real parts of $Z$ parameters can be expressed as:

\[
\text{real} (Z_{11}) = R_g + R_s + \frac{A}{4} \tag{4.29}
\]
\[
\text{real} (Z_{12}) = \text{real} (Z_{21}) = R_s + \frac{A}{2} \tag{4.30}
\]
\[
\text{real} (Z_{22}) = R_d + R_s + A \tag{4.31}
\]

where,

\[
A = \frac{R_{ch}}{1 + \omega^2 C_x^2 R_{ch}^2} \tag{4.32}
\]
\[
C_x = C_{ds} + \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} \tag{4.33}
\]

The imaginary part of $Z_{22}$ is given as:

\[
\text{imag} (Z_{22}) = -\frac{\omega R_{ch}^2 C_x}{1 + \omega^2 C_x^2 R_{ch}^2} \tag{4.34}
\]
Figure 4.12: The quantity $-\frac{\omega}{\text{imag}(Z_{22})}$ is plotted here. The curve is a straight line with the slope and intercept as given in equation 4.35.

Dividing this expression by $\omega$ and inverting, we get:

$$-\frac{\omega}{Z_{22}} = \omega^2 C_x + \frac{1}{R_{ch}^2 C_x}$$  \hspace{1cm} (4.35)

This equation is plotted against $\omega^2$, and $R_{ch}$ and $C_x$ are extracted from the slope and intercept of the straight line. This is shown for in figure 4.12. Once these two quantities are estimated, $A$ can be calculated and hence $R_g$, $R_s$ and $R_d$ are extracted. In order to increase the accuracy of extraction, $R_g$ is extracted at a gate bias where the gate leakage is negligible ($V_{gs}=-2\text{V}$ in the devices studied here). Series resistances extracted by this method are used as a starting point in the optimization process described previously. Figure 4.13 shows the extracted value of $R_s$ and $R_d$ at a gate bias of $-2\text{V}$ indicating that the resistances are approximately equal to 22 ohm. This is close to the values obtained after the optimization process presented later on in this chapter.
4.4 Extraction of intrinsic elements

To determine intrinsic elements, the extrinsics are de-embedded using transformations between two port network parameters as shown in figure 4.14. Following this, the intrinsic elements can be extracted from the $Y$ parameters as

$$Y_{11} = \frac{1}{R_{gs}} + \frac{1}{R_{gd}} + j\omega(C_{gs} + C_{gd})$$  \hspace{2cm} (4.36)

$$Y_{12} = -\frac{1}{R_{gd}} + j\omega C_{gd}$$  \hspace{2cm} (4.37)

$$Y_{21} = g_m e^{-j\omega\tau} - \frac{1}{R_{gd}} - j\omega C_{gd}$$  \hspace{2cm} (4.38)

$$Y_{22} = \frac{1}{R_{gd}} + g_{ds} + j\omega(C_{ds} + C_{gd})$$  \hspace{2cm} (4.39)
From these equations the intrinsic parameters can be derived using the following expressions

\[
\frac{1}{R_{gd}} = -\text{real}(Y_{12}) \quad (4.40)
\]

\[
\frac{1}{R_{gs}} = \text{real}(Y_{11} + Y_{12}) \quad (4.41)
\]

\[
g_{ds} = \text{real}(Y_{22}) \quad (4.42)
\]

\[
C_{gd} = -\frac{\text{imag}(Y_{12})}{\omega} \quad (4.43)
\]

\[
C_{gs} = \frac{\text{imag}(Y_{11} + Y_{12})}{\omega} \quad (4.44)
\]

\[
C_{ds} = \frac{\text{imag}(Y_{22} + Y_{12})}{\omega} \quad (4.45)
\]

\[
g_m = \sqrt{(\text{real}(Y_{21} - Y_{12}))^2 + (\text{imag}(Y_{21}))^2} \quad (4.46)
\]

\[
\tau = \arctan\left(\frac{\text{imag}(Y_{21})}{\text{real}(Y_{21} - Y_{12})}\right) \quad (4.47)
\]

Since the series resistances varied with bias, they were optimized with the intrinsic elements to fit measured S-parameters. This is an iterative procedure and is continued until the error between measured and modeled parameters, given by 4.48 is minimized.

\[
E_{ij} = \sum \frac{|S_{mod_{ij}} - S_{meas_{ij}}|^2}{|S_{meas_{ij}}|^2} \quad (4.48)
\]

After the new values of \(R_s\) and \(R_d\) have been determined, the intrinsic elements are determined using equations shown above. If the extracted intrinsic elements did not match the optimized values of intrinsic elements, the source and drain resistance values can not be taken as accurate and the procedure is repeated to obtain a good set of values for the series resistances and the intrinsic elements. The extracted curves for intrinsic parameters as a function of frequency are shown in figures 4.15 to 4.17. The near constant values of small signal parameters versus frequency indicates the accuracy of extrinsic element extraction.

### 4.5 Results and Discussion

The devices showed a wide range of measured transconductance and DC current-voltage characteristics. Extrinsic peak DC transconductance as high as 90 mS/mm was measured for one of characterized devices. However, some other devices showed transconductance of 40 mS/mm. As a result it was not possible to investigate scaling properties
Figure 4.15: Extracted curves for (a) $C_{gs}$, (b) $C_{gd}$ and (c) $C_{ds}$ plotted versus frequency at $V_{gs}=-3\,\text{V}$ and $V_{ds}=10\,\text{V}$.

of the intrinsic small signal elements between the devices. Similarly, the peak $f_T = 12\,\text{GHz}$ at $V_{gs} = -2\,\text{V}$ and $V_{ds} = 10\,\text{V}$ were observed for 1.4$\mu\text{m}$ gate length devices also showed similar variation in characteristics. The observed threshold voltage was around -8V which is lower than the -4V generally found in AlGaN/GaN HFETs because of the oxide barrier. The extracted values of $f_T$ and $f_{\text{MAX}}$ are shown in figure 4.18. The allowable gate voltage swing on these devices is higher because of the lower gate leakage which allows the gate to be strongly driven into forward bias. Higher swing at the input of a device will provide a greater dynamic range in amplifier applications. In forward bias, the devices exhibited a peak transconductance of 20 mS/mm at $V_{gs} = 6\,\text{V}$ and $V_{ds} = 12\,\text{V}$ with a peak $f_T = 5\,\text{GHz}$ at $V_{gs} = 6\,\text{V}$ and $V_{ds} = 14\,\text{V}$.
Figure 4.16: Extracted curves for (a) $G_m$, (b) $G_{ds}$ and (c) $\tau$ plotted versus frequency at $V_{gs}=-3V$ and $V_{ds}=10V$. 
Figure 4.17: Extracted curves for (a) $R_{gs}$ and (b) $R_{gd}$ plotted versus frequency at $V_{gs} = -3V$ and $V_{ds} = 10V$. 
4.5.1 Small signal elements

Extracted values of the small signal elements for a 2x65 µm device are shown in figures 4.19 to 4.25. The elements are plotted against gate bias at a drain bias of 10V. Gate to source and gate to drain capacitance show the expected behavior from HFET’s in reverse bias (see figure 4.19). The capacitances mainly represent the junction capacitance at the source and drain contacts. Close to pinch-off the Al$_{0.2}$Ga$_{0.8}$N barrier layer is completely depleted and the values of both $C_{gs}$ and $C_{gd}$ are very small. As bias increases, the gate to source capacitance starts increasing with the formation of the electron gas which also leads to decreasing depletion region width. However, the depletion region on drain side does not change much because of the large reverse potential between the gate and drain. With the two-dimensional electron gas formed, the gate to source capacitance stabilizes. Once real space transfer starts into the Al$_{0.2}$Ga$_{0.8}$N barrier, both $C_{gs}$ and $C_{gd}$ increase rapidly with the two capacitances becoming roughly equal when the gate bias is symmetrical between the gate and drain. $C_{ds}$ represents the parasitic capacitance between source and drain contacts. This is a small value because of the large depletion region between the source and drain. The intrinsic ac transconductance $G_m$ is 90 mS/mm (refer figure 4.21) which is much higher.
Figure 4.19: Extracted values of $C_{gs}$ and $C_{gd}$ for a 2x65 µm, $L_g=1.4$ µm device at a drain bias of 10V.

than the extrinsic dc transconductance (see figure 4.22). In order to make a comparison between similar quantities, the extrinsic ac transconductance was calculated as

$$G_{me} = \frac{G_{mi}}{R_g + R_s} + 1 + G_{mi}R_s$$

(4.49)

This is shown in figure 4.22. The two values are comparable after the correction for resistances is applied. The slightly higher value of ac series resistance indicates that one of the resistances may be underestimated.

Measured output conductance of the device is shown in figure 4.23. In HFET mode of operation, the device has low output conductance. With increasing bias, real space transfer occurs. This leads to a broadening of the device channel and hence, the drain to source resistance decreases. This is a hindrance to true forward bias operation in this device.

The leakage resistances are shown in figure 4.24. $R_{gs}$ and $R_{gd}$ decrease rapidly in forward bias. Leakage between the gate and drain is much lower than gate and source. The larger leakage between gate and source is because of the higher charge concentration in the channel toward the source, while the channel closer to drain region is depleted of charges.
under high drain bias. At a lower drain bias the difference between the two resistances was much smaller.

An attempt was made to study scaling properties of the devices. However, only 5 characterized devices showed significant transconductance and amongst these devices, the variability was high. Extracted parameters did not follow the expected scaling trends. Hence the data is not presented in this report. A more thorough study of scaling properties will be performed on devices to be modeled further in this study.

The transfer time characteristic curve at a drain bias of 10V is shown in figure 4.25. Near pinch-off the device exhibits a high transfer time which is to be expected based on the fact that the device is almost off leading to very little charge transfer through the GaN buffer layer between source and drain. At higher bias, the transfer time stabilizes once the 2DEG channel forms leading to a near constant transfer time of 3 pS. In forward bias, the transfer time falls very rapidly and at high gate bias, the high leakage makes extraction of transfer time difficult (phase information is lost whenever there is a lot of leakage). The series resistances $R_s$ and $R_d$ are shown in figure 4.26. In the HFET mode of operation, the device shows a resistance of 19 ohms on the drain which increases to 45 ohms once
charge transfers into the barrier layer. The source resistance shows similar characteristics with the resistance being higher than drain resistance in reverse bias while it is lower in forward bias. The error between measured and modeled S parameters was calculated using the mean square expression:

$$\text{error} = \frac{\sum_{\text{frequency}} \sum_{i=1}^{2} \sum_{j=1}^{2} |S_{ij}(\text{freq})_{\text{measured}} - S_{ij}(\text{freq})_{\text{modeled}}|}{\text{Number of frequency measurements}}$$

(4.50)

In figure 4.27, the calculated error is plotted against gate bias for the 2x65 µm device modeled in this study. The error is within 10% from $V_{GS}=-8V$ to $V_{GS}=7V$. The error reaches a minimum at -2V and is maximum close to pinch off and at high gate bias. At $V_G=-2V$, charge is confined in the channel and the intrinsic device dominates measured S parameters. Close to pinch off and at high gate bias the effect of leakage resistances and parasitics becomes more dominant leading to the increased error.
Figure 4.22: DC transconductance compared to the extrinsic ac transconductance for the 2x65 µm device.

Figure 4.23: Output conductance of the 2x65 µm, L_g=1.4 µm device at a drain bias of 10V.
Figure 4.24: Leakage resistances of the 2x65 $\mu$m, $L_g=1.4$ $\mu$m device at 10V.

Figure 4.25: Transfer delay of the 2x65 $\mu$m, $L_g=1.4$ $\mu$m device at 10V.
Figure 4.26: Source and drain series resistance of the 2x65 \( \mu \)m, \( L_g=1.4 \) \( \mu \)m device.

Figure 4.27: Error between the measured and modeled S parameters calculated using 4.50.
4.6 Summary

FET small signal model development was presented. The importance of comprehensive modeling and extraction of parasitic elements was stressed and the commonly used methods to extract parasitic elements were outlined. Using the developed model, a methodology to extract the elements of AlGaN/InGaN MOS-HFETs was presented with experimental comparisons.
References


Chapter 5

Large Signal Model for the 

AlGaN/InGaN MOS-HFET

5.1 Introduction

A large signal, physics based model has been developed to explore the opportunities and limitations of the AlGaN/InGaN MOS-HFETs. This chapter goes through the development of the model equations and implementation in a commercial circuit simulator. The model is verified by comparing DC current voltage and small signal characteristics to measured and extracted DC and small signal parameters. The small signal parameters were extracted using the procedure described in chapter 4. Thermal effects have been included in the model and the operating temperature of the device was experimentally extracted from electrical measurements.

Compact models used for computer aided circuit design have various requirements in order to achieve accurate simulation results. The time spent in a commercial development cycle can be heavily impacted by the quality of models being used in the design stage. FET modeling has relied on empirical expressions to model various second order effects because of the inherent difficulties in describing the two dimensional nature of the device, unlike the popular models for bipolar devices that are described very accurately by physical models.
Despite the limitations of a physics based compact model for circuit design, the focus of this work has been to develop a physics based SPICE-like model that can be used for device optimization and circuit design. The model developed in this study is based on a physical description of charge control in the device. Another advantage of this development is that it affords an insight into the factors limiting device performance.

5.2 Device Structure

Figure 5.1 shows the cross section of the device modeled in this work. A description of the fabricated structure is presented here from [1]. The III-nitride heterostructures were synthesized in a vertical-flow, high-speed rotating substrate MOCVD system using high purity ammonia as well as tri-ethyl gallium (TEG), tri-methyl aluminum (TMA) and tri-methyl indium (TMI) injected sources using H₂ and N₂ carrier gases. The structures used in this work were deposited onto c-axis sapphire at 1040 °C following a low temperature AlN nucleation buffer layer following a previously described standard methods for III-N materials. The III-N structures of the depletion mode devices were based on substitutional and polarization doped AlGaN/InGaN/GaN HFET structures. III-N depletion mode HFET device structures consisted of a c-plane sapphire substrate on which a 500 nm buffer layer of undoped GaN followed by a 20 nm InGaN channel doped lightly with silicon to a concentration of 3x10¹⁷ cm⁻³. The source material flow rates were targeted to achieve indium concentration of x=20%; however at the higher substrate temperature, actual uniform indium concentration of x<5% is more likely. The top layer is a 30 nm thick Si doped AlₓGa₁₋ₓN with x=15% and doping concentration of 1x10¹⁸ cm⁻³. A Ga₂O₃/Gd₂O₃ gate
dielectric was then deposited on the semiconductor heterostructure layers using molecular beam epitaxy in conjunction with our industrial collaborator, OSEMI inc.

5.3 DC Current Model

5.3.1 Charge Control

The DC current-voltage equations developed in this model are based on a linear charge control analysis of the sheet charge at the heterojunction. A band diagram of the structure defining the various quantities and symbols that will be used in the analytical model is shown in figure 5.2. As discussed in chapter 3, an accurate solution of free charge in the device requires a self consistent solution of the Schrodinger and Poisson equations over the entire device structure. Such a solution requires numerical analysis and is not suitable for implementation in a compact model. To overcome this limitation, the triangular well approximation was used in the model for the MOS-HFET varactor. Although the solution still requires a numerical solution, the problem is simplified and a solution is reached rapidly using a Newton loop. The varactor model was able to accurately describe the gate capacitance in the HFET mode of operation. The charge control description for analyzing
the current voltage characteristics of the HFET is further simplified by using a polynomial fit to the triangular well approximation. In this work we use the linear charge control expression to model the sheet charge at the heterojunction. The approximation was initially used by Lee et. al. [2] in modeling of AlGaAs/GaAs HFETs and was also used recently to model AlGaN/GaN HFETs by Rashmi et. al. [3]. In this formulation, the fermi level $E_F$ versus channel charge equation is approximated as:

$$E_F = E_{F0} + an_s.$$  \hspace{1cm} (5.1)

The fitting constants were evaluated from the solution of the triangular well model used in chapter 3. This is shown in figure 5.3. The calculated values for $a$ and $E_{F0}$ are $3.66 \times 10^{-14} \text{V/cm}^2$ and 0.063 V at 300K. As shown in the figure, this equation deviates considerably from the charge density predicted by the triangular well model close to pinch-off (sub-threshold region). Ideally, to model the sub-threshold region accurately, the charge control equation should be solved taking three dimensional statistics into account. The triangular well approximation under-estimates the free carrier density close to the threshold voltage since it only takes two dimensional statistics into account. Hence, the actual error in estimation is lower than what is apparent in figure 5.3. For the first order model, we de-
cided to go ahead with linear sheet charge equation because it is accurate for the saturated region of operation which is the region of focus in this work.

Potential balance is applied through the device to give the following equation relating the sheet charge density in the channel to the applied terminal potentials (reproduced from chapter 3):

\[
n_s = \left( \frac{1}{q} \right) \left[ \frac{e_1}{t_b} + \frac{e_{ox}}{t_{ox}} \right] (\phi_{00} + \phi_{11} + \Delta E_C - E_F + V_{GB} - \chi_{MS}) + \sigma_{11} \left( \frac{1}{1 + \frac{C_{ox}}{C_b}} \right) \tag{5.2}
\]

where \( C_{ox} \) and \( C_b \) are the oxide and barrier layer capacitances, \( \phi_{00} \) and \( \phi_{11} \) are the potential drops in the barrier layer and the oxide layer due to the barrier layer doping and \( \sigma_{11} \) is the polarization induced sheet charge density at the AlGaN/InGaN interface. Using the linear approximation from equation 5.1, equation 5.2 is simplified to:

\[
qn_s (x) = C_{Geff} (V_{GS} - V_T - V_{CS} (x)) \tag{5.3}
\]

where,

\[
C_{Geff} = \frac{1}{\frac{t_{ox}}{e_{ox}} + \frac{t_b}{e_1} + \frac{a}{q}}. \tag{5.4}
\]

Here, \( \frac{a}{q} \) is additional capacitance term introduced into due linear approximation. Based on this, an effective thickness, \( \Delta t \) is defined

\[
\Delta t = \frac{e_1 \cdot a}{q}. \tag{5.5}
\]

With the previously calculated value for \( a \), \( \Delta t = 19 \mu m \). \( V_T \) is the threshold voltage and is given as:

\[
V_T = \chi_{MS} - (\Delta E_C - E_{F0}) - \phi_{00} - \phi_{11} - \frac{\sigma_{11}}{C_{ox}} \tag{5.6}
\]

5.3.2 Current Modeling

While operating under strong inversion, the drain current is dominated by the drift component and is given as:

\[
I_{DS} (x) = WC_{geff} z (x) v_{drift} \tag{5.7}
\]

where \( z (x) = V_{GS} - V_T - V_{CS} (x) \). \( z(x) \) is the effective gate to channel potential at a point \( x \) between the source and drain. \( C_{geff} \cdot z (x) \) represents the charge density in the channel. Figure 5.4 shows the symbols defined here. The velocity field curves for III-V semiconductors
are not modeled easily in a compact model because of velocity overshoot that occurs due to inter valley transfer. Full band Monte Carlo (MC) simulations indicate that the velocity field curves show two different mobilities before overshoot and saturation. The three parameter mobility model, given in equation 5.8 can be used to model materials exhibiting two different mobilities and overshoot.

$$v(E) = \frac{\mu_0 E + \mu_1 E \left( \frac{E}{E_0} \right)^\alpha + v_{sat} \left( \frac{E}{E_1} \right)^\beta}{1 + \left( \frac{E}{E_0} \right)^\alpha + \left( \frac{E}{E_1} \right)^\beta}$$  \hspace{1cm} (5.8)

Such an expression was used by Polyakov et. al. [5] to model GaN MESFETs. In their work, the parameters were extracted by fitting the expression to MC simulation results. Although such an expression can be used in a numerical TCAD simulator, it cannot be included in a compact model due to the inability to obtain a closed form integration of the drain current equation. In this model we utilize the Trofimenkoff equation, which is commonly used to model Si devices and is given as:

$$v_{drift} = \begin{cases} \frac{\mu_0 |E|}{1 + \frac{|E|}{E_0}} & E < E_{sat} \\ v_{sat} & E \geq E_{sat} \end{cases}$$  \hspace{1cm} (5.9)
Figure 5.5: Plot shows three commonly used variations of the Trofimenkoff expression: (a) $E_{c1} = E_{sat} = 2v_{sat}/\mu_0$; (b) $E_{c1} = \frac{E_{sat} v_{sat}}{\mu_0 E_{sat} - v_{sat}}$; (c) $E_{c1}$ tends to infinity. Curve (b) is used in this work.

Here $E_{c1}$ can be chosen in various ways to alter the curvature of the velocity field curves. In order to investigate the influence of the choice of this parameter, two different commonly suggested formulations were tested. In the first formulation, $E_{c1}$ is chosen to be equal to $E_{sat}$ where $E_{sat} = \frac{2\mu_0}{v_{sat}}$. The second formulation uses $E_{c1} = \frac{E_{sat} v_{sat}}{\mu_0 E_{sat} - v_{sat}}$. The behavior of these expressions as used in the Trofimenkoff equation is shown in figure 5.5. The first expression provides a sharp saturation whereas, the second formulation results in a more gradual saturation of the velocity field curve. Given the extended region over which the III-Nitride velocity field curves saturate, the second curve is more appropriate for approximating the transport characteristics of these materials. It has also been suggested that velocity overshoot is not observed in AlGaN/GaN HFETs because the conduction band discontinuity of AlGaN and GaN is smaller than the $\Gamma - L$ valley separation in GaN. This leads to real space transfer of charge into the barrier layer before velocity overshoot can occur [6].

As long as the device operates under the gradual channel approximation (GCA), the current is obtained by integrating equation 5.7 from the source to the drain. The boundary condition at the source is $z_0 = V_{GS} - V_T$ and at the drain is $z_L = V_{GS} - V_T - V_{DS}$. 
Using these boundary conditions, the final integrated result for drain current is given as:

\[
I_{DS} = \frac{W \mu_0 C_{Geff}}{2L} \times \frac{z_2^2 - z_1^2}{1 + \frac{z_0 - z_1}{\varepsilon_{ei} L}} \tag{5.10}
\]

In this formulation, the channel potentials refer to the intrinsic drain and source terminals. This method is adopted because equation development for the intrinsic device current is simplified and the series resistances are included in the circuit model as “hard” resistances (physical resistances that show up in all simulations - not just DC current voltage equations).

Under the gradual channel approximation, the influence of longitudinal and transverse fields is decoupled, with the transverse field accounting for charge control and the longitudinal field influencing carrier transport in the channel. This is the linear region of operation and is modeled by equation 5.10. Current saturation occurs when the carrier velocity saturates at the saturation velocity \(v_{sat}\). Under these conditions, the field at the drain end of the channel becomes two dimensional and for an accurate solution, the two dimensional poisson equation has to be solved. The classic work by Grebene and Ghandhi provides a solution of the two dimensional poisson equation in a JFET [7]. Later on, the same method was adopted for modeling velocity saturation in HFETs [8]. Although the complete solution to this problem is a Fourier series involving hyperbolic cosine terms, using a self consistent approach it has been shown that the potential in the pinched off region of the channel is well represented by the first harmonic term in the series. This potential drop across the pinched off region is given as:

\[
V_2 = \frac{2}{\pi} \left( t_b + t_{ox} + \Delta t \right) \sinh \left( \frac{\pi L_2}{2 \left( t_b + t_{ox} + \Delta t \right)} \right) \tag{5.11}
\]

where \(L_2 = L - L_1\) is the length of the pinched-off region (from \(L_1\) to \(L\) in figure 5.4. With this in mind it has to be noted that, once velocity saturation occurs in the channel, equation 5.10 is no longer valid beyond the point where the electric field (E) attains the saturated electric field value \(E_{sat}\). Denoting the distance of this point from the source end as \(L_1\), the current in region 1 (from 0 to \(L_1\)) is still represented by equation 5.10 with \(L\) being replaced by \(L_1\). The current in region 2 (from \(L_1\) to \(L\)) is fixed and is given as:

\[
I_{DS2} = W C_G z_{L1} v_{sat} \tag{5.12}
\]

The drain current at \(L_1\) from equation 5.10 is equated to the drain current in region 2 to give an expression for \(z_{L1}\) in terms of \(L_1\):

\[
z_{L1} = \frac{-K_0 \left( L_1 + \alpha z_0 \right) + \sqrt{K_0^2 \left( L_1 + \alpha z_0 \right)^2 + 4 \left( 1 - K_0 \alpha \right) z_0^2}}{2 \left( 1 - K_0 \alpha \right)} \tag{5.13}
\]
where \( K_0 = \frac{2v_{sat}}{\mu_0} \) and \( \alpha = \frac{1}{E_{c1}} \). This equation has to be solved simultaneously with the equation relating the total potential across the channel as:

\[
V_{DS} = z_0 - z_{L1} + V_2. \tag{5.14}
\]

where \( V_2 \) is given by equation 5.11. In the compact model this is accomplished by establishing a Newton loop inside the model that iterates to find the values of \( L_1 \) and \( z_{L1} \). The value of \( V_{DS} \) where drain current saturates can be obtained by setting \( L_1 = L \) and equating currents in the two regions of the channel. It can be shown that \( V_{DSS} \) is given by equation 5.13 with \( L_1 \) replaced by \( L \).

The major drawback of this formulation is that it is more computationally intensive than a purely analytical expression. However, it provides a physical model describing velocity saturation and channel length modulation effects. The next step is to extend the DC current model to include thermal effects. Before discussing the impact of temperature on model parameters, an experimental technique to estimate channel temperature is presented.

### 5.4 Estimation of Channel Temperature

In order to investigate the impact of self heating on device performance, thermal effects have been included in the device model. As outlined in chapter 2, the temperature rise in a device is directly proportional to the DC power dissipation in the channel. The devices characterized in this work were driven at a drain bias of 10V while delivering up to 1 A/mm of drive current, giving a DC power density of 10 W/mm of gate periphery. At such power densities, self-heating is expected to have a significant impact on device performance.

Extraction and modeling of thermal resistance becomes essential to the accurate modeling of these devices. In this work, the thermal resistance of these devices has been estimated using a combination of RF and DC measurements. The most significant impact of self heating is the change in output conductance seen in DC current voltage curves. However, S parameter measurements at high frequencies are independent of the impact of self heating because of the long time constants (on the order of mS) associated with heat transfer through most materials used in semiconductor devices. This has been experimentally observed in AlGaN/GaN HFETs using pulsed IV measurements in various works. As
Figure 5.6: Extracted and calculated values of output conductance of a 2x50 µm device at $V_{GS}=-2V$ are shown in this figure. The curve labeled “extrinsic” is calculated using equation 5.15. As a result, the output conductance of the device under RF excitation does not exhibit the negative differential behavior that is commonly witnessed in DC curves. This is observed in the output conductance plot (refer figure 4.23) shown in chapter 4. The output conductance shown in this plot is the intrinsic conductance of the device, devoid of the effect of series resistances - which reduce the total extrinsic conductance. From the equivalent circuit model (figure 4.2), the extrinsic output conductance at DC can be written as:

$$G_{DS, extrinsic} = \frac{G_{DS, intrinsic}}{1 + G_{DS, intrinsic} (R_D + R_S)} \quad (5.15)$$

The equation neglects the impact of leakage resistances $R_{GS}$ and $R_{GD}$. Figure 5.6 shows the extrinsic and intrinsic output conductance of the device as calculated from the small signal parameters. Also shown in the figure is the real part of $y_{22}$ measured at 45 MHz. This represents the raw extrinsic output conductance which includes the effect of feedback path between the gate and drain. The extrinsic conductance determined using the equivalent circuit parameters and $\text{real}(y_{22})$ are very close indicating the accuracy of neglecting the gate to drain resistance at the chosen gate bias of $V_{GS} = -2V$. The DC and extrinsic RF conductance are compared in figure 5.7. In saturation, the DC conductance is negative.
Figure 5.7: Output conductance of a 2x50 µm device, calculated from DC IV curves, is compared to calculated extrinsic output conductance ($V_{GS}=-2V$). High voltage region shows negative output conductance in DC characteristics indicating presence of self-heating.

indicating the presence of self heating effects, while the RF conductance is positive indicating the absence of self heating in high frequency measurements. However, it is noted here that the self heating arising out of quiescent point DC power dissipation is still present in the device. Since the output conductance is a differential quantity, the impact of DC heating is negligible. In equation 5.16, the second term includes the effect of DC heating but it’s much smaller than the first term and can be neglected [9].

$$\frac{dI_{ds}}{dV_{ds}} = \frac{\partial I_{ds}}{\partial T} \cdot \frac{\partial T}{V_{ds}} + \frac{\partial I_{ds}}{\partial V_{ds}} \bigg|_{T=T_0}$$

(5.16)

At a constant gate bias, drain current is reconstructed by integrating output conductance over drain bias. The difference between the curve reconstructed from small signal output conductance and DC curve can be attributed to self heating or dispersion effects from trapping charge trapping, if present. In order to ascertain the contributions of self heating and trapping mechanisms to the observed increase in output conductance, low frequency output conductance was measured using the HP4184 LCR meter. Figure 5.8 shows the output conductance measured by the LCR meter from 20 Hz to 1 MHz at a drain bias of 10V. The gate voltage is stepped from -8V to 0V. As indicated, the output conductance
at low frequencies does not increase significantly at a gate bias of -8V and -6V whereas there is a significant increase in the output conductance at higher gate voltages as the device turns on and drain current increases. At a gate bias of -8V and -6V, the electric field between gate and drain is maximum and hence, dispersion effects would be maximum under this condition. Since the conductance does not change significantly under these conditions, it leads us to attribute the entire difference in DC and RF output conductance at high gate biases to the impact of self heating. Figure 5.9 shows the reconstructed and DC IV curves at a gate bias of -2V. The high output conductance of this device in saturation leads to significant slope in the reconstructed curve. The difference between the DC and reconstructed curve is used to calculate the differential effect of DC power dissipation on current:

\[ K_0 = \frac{\Delta I_{ds}}{\Delta P_{diss,DC}} \]

In order to estimate the thermal resistance of the device, DC currents are measured at different ambient temperatures (refer figure 5.10). The measurements are carried out at a drain bias of 1V to minimize the impact self heating. From the measurements, a calibration
factor $C_0$ is determined where it can be written as:

$$C_0 = \frac{\Delta T}{\Delta I_{ds}} \quad (5.18)$$

The calibration curves are plotted in figure 5.11. Once the two quantities defined above have been determined, the thermal resistance is expressed as:

$$R_{th} = \frac{\Delta T}{\Delta P_{diss,DC}} = \frac{\Delta T}{\Delta I_{ds}} \times \frac{\Delta I_{ds}}{\Delta P_{diss}} \quad (5.19)$$

Using the above equations and measured data the thermal resistance is calculated and plotted in figure 5.12 as a function of drain bias for three different gate voltages. At the highest gate voltage of 0V, the channel temperature is estimated to be close to 1100 6oK. To estimate thermal resistance we plot the extracted values of temperature for $V_{GS} = -2V$ and 0V against DC power dissipation. As indicated in figure 5.13, the temperatures calculated at both gate biases line up at the same power level in the low DC power dissipation region. As the temperature increases, the curvature of this plot increases. Thermal resistance is estimated from the slope of the plot. At the low temperature region, the extracted value is approximately 81 °C-mm/W whereas in the high temperature region this slope increases to
Figure 5.10: Measured DC currents over temperature. These curves are used to calibrate the temperature dependence of the drain current.

170 °C-mm/W. As mentioned in chapter 2, thermal conductivity of most semiconductors is a decreasing as temperature increases. The thermal conductivity for Sapphire is plotted in figure 5.14 as a function of temperature. At 600 °K, thermal conductivity decreases to 0.2 W/(K-cm) explaining the doubling of thermal resistance at higher temperatures. It should be noted that the extraction procedure assumes the calibration factor $\Delta T/\Delta I_{DS}$ stays constant with temperature, which is less valid when the temperature changes significantly from the conditions under which the constant is measured. As temperature increases, the sensitivity of current to temperature decreases and the constant is expected to get smaller. Therefore, the real temperature is estimated to lie between the linear extrapolation shown in figure 5.13. The results of this extraction demonstrate the impact of self-heating in devices on Sapphire substrates. Switching to a substrate with higher thermal conductivity such as SiC or GaN can lead to enhanced current drive and improve device performance.
5.4.1 Implementation of Self-Heating in the Model

Thermal effects are included in the device model by using a thermal subnetwork consisting of a thermal resistance ($R_{th}$) and a capacitance ($C_{th}$) as discussed in chapter 2. The subnetwork acts as a low pass filter, with the corner frequency estimated to be around 1 kHz from the low frequency output conductance measurement (refer figure 5.8). Thermal resistance is calculated in the model using Cooke’s analytical expression presented in chapter 2. The calculated thermal resistance for the 2x50 $\mu$m device is 83.5 °C-mm/W for a 0.04 mm thick substrate with finger to finger distance of 10 $\mu$m, $L_{diss}$=0.25 $\mu$m and $W_{diss}$=100 $\mu$m. This agrees well with the experimentally extracted value of 81 °K-mm/W. If required, the model can also take the thermal resistance as an input to fit measured characteristics better. Thermal time constant is also provided as an input to the model and is estimated to be 1 mS from the 1 kHz corner frequency. This is a first order implementation and accurate thermal modeling in the device would require a thorough analysis of device structure and characterization using pulsed measurements to reveal the presence of multiple time constants, if any.

The model includes a fourth node providing the device temperature as an output.
Figure 5.12: Estimated channel temperature is plotted against drain bias for a 2x50 µm device at $V_{GS} = -$6, -2 and 0V.

During simulation, the difference of powers calculated during the previous and current iteration is set as the current flowing into the node. The net power dissipation in the device is calculated using the following expression:

$$P_{diss} = I_{ds} \cdot V_{ds} - \frac{d(C_{th} \cdot T)}{dt} \quad (5.20)$$

Since the node is left open, the simulator solves the system such that the net current at the temperature node is zero. This leads to the solution for $I_{DS}$ under self heating. The voltage at this node represents the difference between ambient and device temperatures.

### 5.5 Impact of Self-Heating on Model Parameters

The biggest impact of self heating on current voltage characteristics comes from the dependence of mobility on temperature. Scattering increases with temperature as carriers as well as lattice atoms gain energy. The various scattering processes are combined using Mathiessen’s rule to obtain the overall effective mobility. Full band Monte Carlo simulations have to be carried out to obtain the mobility. Ruden et al [10] proposed the follow expression
Figure 5.13: Estimated channel temperature is plotted against DC power density in the channel for a 2x50 μm device at $V_{GS} = -2$ and 0V.

for mobility based on fitting to the MC results:

$$\frac{1}{\mu} = a \left( \frac{N_I}{10^{17} \text{cm}^{-3}} \right) \ln \left( 1 + \beta_{CW}^2 \right) \left( \frac{T}{300} \right)^{-1.5} + b \left( \frac{T}{300} \right)^{1.5} + \frac{c}{\exp \left( \frac{\Theta}{T} \right) - 1}$$ (5.21)

where

$$\Theta = \frac{\hbar \omega_{LO}}{k_B} = 1065K$$ (5.22)

$$\beta_{CW}^2 = 3.00 \left( \frac{T}{300} \right)^2 \left( \frac{N_I}{10^{17} \text{cm}^{-3}} \right)^{-2/3}$$ (5.23)

$$N_I = (1 + k_c) N_D$$ (5.24)

$$a = 2.61 \times 10^{-4} V \text{scm}^{-2}$$ (5.25)

$$b = 2.90 \times 10^{-4} V \text{scm}^{-2}$$ (5.26)

$$c = 1.70 \times 10^{-2} V \text{scm}^{-2}$$ (5.27)

Here $a$, $b$ and $c$ are constants obtained from fitting to Monte Carlo results. $N_D$ is the donor concentration in cm$^{-3}$, $T$ is the ambient temperature in Kelvin and $k_c = N_A / N_D$ is the compensation ratio. This expression was derived for GaN. In our devices, the mole fraction of Indium is expected to be less than 5% and is expected to be close to the performance
Figure 5.14: Thermal conductivity of Sapphire plotted over a temperature range of 300 - 600 °K.

expected for GaN. For the devices investigated in this study, \( N_D = 3 \times 10^{17} \text{ cm}^{-3} \) and \( k_c = 0 \). Mobility is plotted as a function of temperature in figure 5.15. This expression is only valid up to 600 °K and might not be valid at the higher range of temperatures seen in this device.

As an alternative, the commonly used expression for silicon devices has also been provided:

\[
\mu = \mu_0 \left( \frac{T}{300} \right)^{\alpha} \tag{5.28}
\]

This expression is more suitable for optimization of model characteristics to fit measured data. From fitting the model to measured data, the value of \( \alpha \) was estimated to lie between -1.5 to -1.8. Saturated electron velocity \( v_{sat} \) is also temperature dependent and is modeled using the following expression:

\[
v_{sat}(T) = v_{sat}(T_0) - \Delta v_{sat} \frac{T}{T_0} \tag{5.29}
\]

Another parameter impacted by temperature is the band gap. Although, this model does not directly use the energy gap in calculation of model parameters, band gap enters the charge control model presented in chapter 3 through the conduction band discontinuity, \( \Delta E_C \). For GaN, based on measured band gap values at different temperatures the energy

\[
\Delta E_C = \begin{cases} 
\Delta E_{C0} & \text{for } T \leq T_{c1} \\
\Delta E_{C0} - \Delta E_{C2} \left( \frac{T}{T_{c2}} \right) & \text{for } T > T_{c1} 
\end{cases}
\]
Figure 5.15: Mobility in GaN plotted as a function of temperature. The layer is assumed to be doped at $3 \times 10^{17}$ cm$^{-3}$.

The gap can be written as [11]

$$E_g(T, K) = 3.504 - \frac{5.08 \times 10^{-4} T^2}{996 - T} \text{eV}$$ (5.30)

Corresponding expressions for energy dependent band gap of AlN and InN were not available in literature. Once again, considering that the Indium concentration is low (less than 5 %), we can approximate the bandgap of the channel layer with that of GaN. Sheet charge density in a quantum well is also expected to be a strong function of temperature in the channel as seen in the charge density expression:

$$n_s = D k T \left[ \ln \left(1 + \exp \frac{E_f - E_0}{kT} \right) \right] + \ln \left(1 + \exp \frac{E_f - E_1}{kT} \right)$$ (5.31)

Empirical expressions for the temperature dependence of the linear fit parameters, $E_{F0}$ and $a$ can be derived from simulations using the charge control model presented in chapter 3.

### 5.6 Experimental determination of mobility

In this section, a method to extract mobility in the channel of the device under active gate bias conditions is described. At low drain bias the device is in linear region of
operation and the entire channel is assumed to have uniform charge density. Under these conditions, the output conductance of the channel can be written as:

$$G_{DS} = \frac{W}{L} q\mu_n n_s$$  \hspace{1cm} (5.32)

where $qn_s$ is the total channel charge. The channel charge can be estimated by integrating gate to channel capacitance from threshold to the gate bias at which the charge is being calculated. This can be expressed as:

$$qn_s = \int_{V_T}^{V_{GS}} C_{gc} dV_{gs}.  \hspace{1cm} (5.33)$$

Using equations 5.32 and 5.33, the output conductance is calculated as:

$$\mu_n = \frac{L^2 G_{DS}}{qn_s}  \hspace{1cm} (5.34)$$

This technique of estimating mobility as a function of transverse electric field is the conductance-capacitance method and is employed to estimate the universal mobility curves for Si MOSFETs [15]. The commonly used procedure is based on the low frequency measurement of gate capacitance and channel conductance in the linear mode of operation. In this work, we use the extracted conductance and capacitance of the device from ColdFET measurements where the drain to source DC bias is fixed at 0V. Using a network analyzer, S parameters are measured with a very low ac voltage across the channel (estimated to be less than 5 mV at a -10 dBm power drive). Two major factors that can impact results from this method are the accurate determination of series resistance in the drain and source and dispersion arising out of trapping effects. Series resistances are extracted from the ColdFET measurement using the methods described in chapter 4 and will not be discussed here. The impact of series resistance is to reduce extrinsic output conductance as discussed previously in this chapter. The output conductance of a 50 $\mu$m unit gate width device under ColdFET conditions is shown in figure 5.16. The impact of dispersion on output conductance was investigated using low frequency conductance measurements. The results indicated that the ColdFET output conductance did not vary significantly with measurement frequencies between 20 Hz to 1 MHz (refer figure 5.17). Therefore, the impact of dispersion is assumed to be negligible. The gate capacitance under ColdFET conditions is obtained by adding the extracted gate to source and gate to drain capacitances:

$$C_{gg} = C_{gs} + C_{gd}$$  \hspace{1cm} (5.35)
Below the threshold voltage of -8V, a residual capacitance can be seen in the plot of $C_{gg}$ as shown in figure 5.18 and can be attributed to the fringing capacitances. This capacitance is subtracted from the $C_{gg}$ plot to give us $C_{gc}$, the gate to channel capacitance. Sheet charge density is obtained by integrating the capacitance from threshold to 0V. The integrated sheet charge density for a 2x50 µm device is shown in figure 5.19. With channel charge calculated, the mobility can be estimated. To plot mobility curves we estimate the average transverse electric field on an electron in the channel. As discussed in chapter 3, electric field at the heterointerface is given as: $E = \frac{q_n s}{\epsilon_s}$. Neglecting depletion charge in the InGaN buffer layer, electric field underneath the channel is negligible. Hence, the total average electric field is calculated to be $E = \frac{q_n s}{2\epsilon_s}$. This is plotted in figure 5.20. Under nominal operating fields close to 1 MV/cm, low field mobility is estimated to be close to 200 cm$^2$V$^{-1}$s$^{-1}$. This value of low field mobility is used in the large signal model. The extraction shows a large variation close to threshold. This is due to two factors:

- Errors in estimating threshold voltage.
- Increased error in estimating channel conductance at low gate bias due to the impact
Figure 5.17: Low frequency output conductance of 2x50 µm device measured from 20 Hz to 1 MHz with $V_{DS}=0V$. The gate bias is varied from -8V to 0V in steps of 2V with the -8V curve lowest and 0V curve highest.

5.6.1 Verification of DC Model

The DC model has been verified by simulating DC IV characteristics for the 2x50 µm device on which experimental data has been collected. The simulated and measured family of curves for the device are plotted in figure 5.21. The model fits measured IV characteristics accurately from a gate bias of -6V to -2V. Below -6V, the model is less accurate in the subthreshold region due to the following reasons:

- The linear charge sheet model cannot account for charge present in the subthreshold region. In order to take this into account, a higher order expression can be used. Another approach to extend this model would be to use the unified charge control model (UCCM) proposed by Byun et. al. for HFETs [13]. This expression was formulated after studying charge control behavior calculated using a self consistent Poisson-Schroedinger solver.
Figure 5.18: Gate capacitance of the 2x50 μm device with $V_{DS}=0V$. The gate to channel capacitance is calculated by subtracting fringing capacitance - estimated here to be 35 fF.

- This specific device has a n-doped channel with the InGaN layer doped to $3\times10^{17}$ cm$^{-3}$. This creates a subthreshold conduction path and is present even when the sheet charge region has fully formed. This is exhibited in the high output conductance values observed in RF measurements even in saturation. Since this is not a desirable feature in high performance devices, the effect was not included in the model. Future iterations of the device design should avoid a doped channel due to the negative impact on mobility as well as output conductance.

Beyond a gate bias of -2V the model over predicts the device current. The fit can be improved by a better optimization of parameters associated with the mobility expression and thermal resistance. The compression of current from predicted values can be attributed to the following reasons:

- At a high gate bias the high transverse field reduces effective mobility as plotted in figure 5.20. The exact analytical expression for this effect involves a numerical integral which cannot be implemented in a compact model. Borrowing from the expressions used in MOSFET modeling, a simplified analytical form that has shown a good fit to
the measured characteristics in MOSFETs is [12]:

$$\mu_{0eff} = \frac{\mu_0}{1 + \beta (V_{GS} - V_T)}$$  \hfill (5.36)

Figure 5.22 shows the modeled IV characteristics with $\beta = 0.05$. Although the fit at $V_{gs}=0$V improves, the fit degrades marginally in saturation region at lower gate biases. This issue could be solved by considering a field dependent expression for $\beta$ or by improving the expression.

- The second reason for compression in current drive arises out of the non ideal charge confinement in the quantum well of an HFET. At a gate bias of -2V, real space transfer into the AlGaN barrier layer starts as exhibited by the increasing gate capacitance in the characterized varactors (discussed in chapter 3). The gate capacitance model developed in chapter 3 also indicates an increasing in the free charge in the AlGaN barrier layer beyond a gate bias of -3V. With charge transferring to the barrier layer, sheet charge in the channel saturates. This is a well known phenomenon in HFETs and is observed in the charge characteristics calculated by the self consisted Schroedinger Poisson solver. Various empirical expressions have been suggested in literature and
one such work on modeling of AlGaAs/GaAs HFETs used the hyperbolic tangent function to produce a smoothly saturating curve [8]. This expression was calibrated to the results of a numerical self consistent solver to extract all the empirical parameters. A similar approach can be taken here to improve the fit at high gate biases. However, because of the presence of a gate dielectric, it is possible that the device exhibits the formation of a second channel underneath the gate at a forward gate bias. This can be modeled by using a second charge control equation with the appropriate threshold voltage. FAT (long channel) FET devices ($L_g = 50 \mu m$) exhibited a transconductance peak in the forward bias region [14]. This was not observed in the short channel RF devices. Possible reasons for this are discussed in the next section.

### 5.7 Impact of Series Resistances

The series resistances extracted in chapter 4 are bias dependent over the entire range of operation. However, in the HFET mode of operation, where this charge control
Figure 5.21: Simulated (solid line) and measured (circles) DC IV curves for the 2 finger, 50 µm device with a gate length of 0.25 µm.

model is valid, the series resistances are constant as seen in the extracted curve. For the 2x50 µm device the extracted resistances were 22 Ω on both source and drain from -6V to +1V on the gate. The extracted value of gate resistance is 7.7 Ω. The resistances extracted from small signal measurements were used to simulate the device characteristics.

Source and drain series resistances have a profound impact on device performance. As mentioned previously, intrinsic output conductance of the device is 3-4 times higher than the extrinsic conductance in the linear region of operation. The impact of a higher conductance in the linear region is to reduce the knee voltage of the current voltage characteristics. To investigate the impact of series resistance, simulations were performed with a reduced value of 5 Ω on both source and drain. Simulation results for both values of series resistance are plotted in figure 5.23.

As indicated by the figure, the knee voltage is reduced from a value of 5V at a gate bias of 0V to 3.5V at the same gate bias. The reduction in knee voltage has a direct impact on the maximum power obtainable from an amplifier. As a first order estimate, the maximum power obtainable from a class A amplifier is given as $P_{\text{max}} = I_{\text{DSat}} \cdot (V_{\text{DS0}} - V_{\text{knee}}) / 8$. With
Figure 5.22: Simulated (solid line) and measured (circles) DC IV characteristics including the transverse field effect on mobility.

$V_{DS0} = 10\text{V}$, the maximum power output from the device is calculated to be 37.5 mW for the device with $20\ \Omega$ resistance and 48.75 mW with $5\ \Omega$ series resistance. This is the DC power and can differ from RF power output due to dispersion effects (as has been commonly observed in AlGaN/GaN HFETs). High series resistances are also one of the reasons for the rapid roll off in device transconductance. The simulated transconductance shows a much more gradual roll off in the device with lower series resistance (refer figure 5.24. This result, combined with the current compression due to high temperature in the channel, indicates the reasons for not observing a secondary peak in transconductance that was observed in the long channel devices (refer figure 5.25). In the long channel devices ($L_g=50\ \mu\text{m}, W=100\ \mu\text{m}$), the channel resistance is higher than the source and drain resistances ($L_{GS}$ and $L_{GD}$ are less than $5\ \mu\text{m}$) and device performance is dominated by the channel underneath the gate.
5.8 Capacitance Model

Under transient and high frequency operation, an accurate analysis of the channel charge and associated device capacitances is required. In addition to the steady state drift equation, which was analyzed while developing the DC model, instantaneous operation of a FET requires a solution of the continuity equation. For the time dependent case, the two equations can be written as:

\[
\frac{\partial i_{ds}(x,t)}{\partial x} = WC_{Geff} \frac{\partial z(x,t)}{\partial t}
\]  \hspace{1cm} (5.37)

\[
i_{ds}(x,t) = WC_{Geff} \mu z(x,t) \frac{\partial z(x,t)}{\partial t}
\]  \hspace{1cm} (5.38)

Together these equations form a second order partial differential equation given by

\[
\mu \frac{\partial}{\partial x} \left[ z(x,t) \frac{\partial}{\partial x} z(x,t) \right] = \frac{\partial}{\partial t} z(x,t)
\]  \hspace{1cm} (5.39)
Figure 5.24: Simulated and measured DC transconductance characteristics: (a) Simulated with series resistance=22 Ω; (b) Series resistance=5 Ω; (c) Measured.

where,

\[ z(x, 0) = 0 \]  \hspace{1cm} (5.40)

\[ z(0, t) = v_{GS}(t) - V_T \]  \hspace{1cm} (5.41)

\[ z(L, t) = \alpha z(0, t) \]  \hspace{1cm} (5.42)

\( \alpha \) is the saturation coefficient defined as:

\[
\begin{cases}
1 - \frac{V_{DS}}{V_{DS, sat}} & V_{DS} < V_{DS, sat} \\
0 & V_{DS} \geq V_{DS, sat}
\end{cases}
\]  \hspace{1cm} (5.43)

A general solution of this equation cannot be obtained. However, under the quasi-static assumption, the time dependent quantities in the equation can be replaced with the time independent quasi-static quantities. The quasi-static approach assumes that the potential in channel responds instantaneously to applied terminal voltages.

Several approaches can be taken to model device capacitances. Conceptually the most simple approach would be to define \( C_{gs} \) and \( C_{gd} \) analytically and calculate the displacement currents through these capacitances. This is the approach followed by the Meyer
Figure 5.25: Measured DC transconductance of a long channel ($L_g=50 \ \mu m$) device. Transconductance peak is observed at a gate bias of 3V.

model that was popular in MOSFET models for digital circuit simulation. However, this approach suffers from charge non conservation issues which can lead to simulation errors in nonlinear circuits. The non conservation issues are overcome by modeling the charges directly as a function of terminal voltages. This approach insures that the model Once the charges are defined accurately the capacitances can be derived by differentiating the charges with respect to every pair of terminal voltages. In a three terminal FET such as the MOS-HFET investigated here, there are three charges associated with device - $Q_G$, $Q_S$ and $Q_D$. Each charge equation is dependent on all three terminal voltages. Hence, a total of 6 capacitances can be defined in the model - $C_{GS}$, $C_{GD}$, $C_{DS}$ and their reciprocal capacitances $C_{SG}$, $C_{DG}$ and $C_{SD}$. The first subscript refers to the charge function and the second subscript comes from the terminal voltage with respect to which it is differentiated.

Defining the terminal charges is a non trivial problem. Charge conservation allows us to write the gate charge as the negative summation of source and drain charges:

$$Q_G = -(Q_D + Q_S) \quad (5.44)$$

This leaves us with the problem of determining the source and drain charges. In reality, it is impossible to identify charges associated with the source and drain. Charge in the channel
is the physical quantity and must be partitioned to give the source and drain charges. In this work, the approach suggested in [17] has been followed. The source and drain charges are determined by a method of moments technique. Using this method, the source and drain charges are defined as:

\[ Q_S = -qW \int_0^L (L - x) n_s(x) \, dx \]  

(5.45)

and,

\[ Q_D = -qW \int_0^L x n_s(x) \, dx \]  

(5.46)

where \( n_s(x) \) is the sheet charge density given by the linear charge control equation 5.3. The equations are integrated from 0 to \( L_1 \) using \( z(x) \) as defined in the DC model. From \( L_1 \) to \( L \) the channel potential is taken to be constant and equal to \( z_{L_1} \). The integrated equations are lengthy and are presented in appendix A. Once the charges have been determined, these are defined in the device model and the terminal currents are modified from the DC equations as follows:

\[ I_D = I_{DS} + \frac{\partial Q_{\text{drain}}}{\partial t} \]  

(5.47)

\[ I_S = -I_{DS} + \frac{\partial Q_{\text{source}}}{\partial t} \]  

(5.48)

\[ I_G = \frac{\partial Q_{\text{gate}}}{\partial t} \]  

(5.49)

These equations are directly implemented in Verilog-A using the built in time derivative function. With the capacitance model implemented, all important intrinsic elements of a quasi-static model are accounted for. The gate current, as defined here, only includes the current arising out of displacement of charge during transient operation. DC components arising out of other processes such as tunneling have to be added to this expression.

### 5.8.1 Results and Discussion

The capacitance model was verified by comparing measured small signal parameters of a 2x50 \( \mu \)m device with the simulated small signal parameters. As discussed in chapter 4, the equivalent circuit parameters are directly related to \( y \) parameters and hence, these were used. Figure 5.26 shows the measured and extracted gate to source capacitance versus drain bias at a gate bias of -4V, which corresponds to the maximum \( F_T \) point. As shown in the figure, the model fits measured \( C_{gs} \) at -4V within 5% upto a drain bias of 4V.
Figure 5.26: Modeled and extracted gate to source capacitance for the 2x50 $\mu$m device.

but does not exhibit roll off in the high drain bias region leading to a maximum error of 15% at a drain bias of 10V. The roll off in $C_{gs}$ corresponds to self-heating effects. As discussed earlier, the impact of temperature is not modeled in the charge control expression. The fit can be improved further by considering temperature dependent linear model. $C_{gd}$ is shown in figure 5.27. The error in fit is less than 20% at a gate bias of -4V. $G_m$ and $F_T$ plots (figures 5.28 and 5.29) fit measured characteristics within 5% and 20% respectively at a gate bias of -4V. $F_T$ exhibits varying slope with drain bias and is not reproduced by this model. In the linear and saturation regions, the fit for $F_T$ is also less than 5%. Percentages are calculated as the error between measured and modeled values of the parameters with respect to the measured value. The transition from linear to saturation regions in the $F_T$ and $G_m$ curves indicates the possibility of higher order derivatives being discontinuous. This issue needs to be investigated further. It should be noted that results shown here are without any optimization of model parameters. The fit should improve upon further optimization. The model shows a similar error trend from -6V to -3V but the error increases significantly at -2V due to the charge compression phenomenon that was observed in DC characteristics as well. Further work on the model should investigate methods to model this phenomenon accurately.
Figure 5.27: Modeled and extracted gate to drain capacitance for the 2x50 μm device.

5.9 Gate Current Characterization

The presence of a gate dielectric in the MOS-HFETs reduces gate leakage in comparison to that of HFETs. Although HFETs were not characterized in this study, published literature indicates that the leakage of MOS-HFETs with dielectrics such as SiO$_2$ and Si$_3$N$_4$ is several orders of magnitude lower than that of Schottky gate HFETs.

Gate current did not change with temperature from 25 °C to 60 °C over a gate bias from -8V to 5V (figure 5.30). This indicates that the leakage currents are based on tunneling mechanisms. Trap assisted tunneling mechanisms (such as Frenkel-Poole) are also expected to be temperature dependent and hence are ruled out from consideration. Gate current from direct or Fowler-Nordheim tunneling mechanisms can be represented by the following expression: $J_g = V^2 \exp(-b/V)$, where $V$ is the effective voltage across the dielectric. A gate leakage model has to be developed and added to the full large signal model.

5.10 Summary

A large signal model based on the linear charge control equation was developed and implemented in a circuit simulator. The model fits extracted intrinsic small signal parameters of the device within a 20% error from a drain bias of 0V to 10V at a gate bias of
Figure 5.28: Modeled and extracted transconductance for the 2x50 µm device.

-4V. The model needs further improvement in charge control modeling to exhibit transconductance compression characteristics. The effect of temperature on device parameters such as mobility and series resistances should also be extracted experimentally. The use of a piecewise mobility model complicates charge expressions and introduces a discontinuity in third and higher order derivatives of charges. This is not desirable for non-linear circuit simulations and methods have to be developed to solve these issues.
Figure 5.29: Modeled and measured $F_T$ for the $2\times50 \ \mu\text{m}$ device.

Figure 5.30: Measured gate current over temperature.
References


Chapter 6

Analysis and Modeling of the N-i-N structure

6.1 Introduction

A significant limitation in the fabrication of III-N MOSFET relates to the formation of ohmic contacts for enhancement-mode MOSFET structures. Unlike existing III-N HFET devices, which include a high free carrier density two dimensional electron gas in the semiconductor substrate, a MOSFET in either accumulation or inversion mode requires low free carrier concentrations for the semiconductor channel to have an off-state. The applied gate bias enhances the free-carrier density in the channel, turning on the FET. Unfortunately, a low free-carrier density substrate is problematic for the formation of ohmic contacts, a problem usually dealt with in silicon MOS through self-aligned ion implantation. The high annealing temperatures associated with activating implanted dopants to substitutional sites limits the use of ion implantation for III-N MOSFET fabrication.

To overcome this limitation, we investigate a novel approach to fabricating carrier rich source and drain regions. In this work, selected area epitaxial re-growth of doped III-N materials has been developed to form source-drain contacts, yielding the needed n+/i/n+ or n+/n-/n+ or n+/p-/n+ structures. The structures have been electrically characterized
Figure 6.1: SEM of the n⁺-i-n⁺ structure fabricated with re-grown source drain regions. The structure shown has two gate fingers and gate length is 1.4 µm.

and modeled using DC and S parameter measurements.

6.2 Fabrication

Undoped GaN buffer layers were grown by metallorganic vapor phase epitaxy (MOVPE) using an in-house designed vertical flow showerhead, high speed rotating substrate reactor on 2 inch c-plane sapphire substrates. Prior to the growth of the high temperature GaN buffer, the substrate was 10 minute nitridated at 1000°C and a low temperature AlN buffer layer was grown. The precursors were NH₃ and TMGa. Growth was performed at 1040°C and 76 Torr chamber pressure. The V/III ratio was 2000 and the thickness of the buffer layers achieved was about 0.5μm/hour. Fabrication was performed in a class 1000 clean room. The intrinsic GaN and n-GaN regions were identified by the photolithography process followed by lift-off and reactive ion etching using Cr-Ni mask. The thickness to determine the etch stop is measured by Dektak profilometer and the metal etch is performed to remove the Cr-Ni mask. The substrate is later transferred to the MOCVD reactor for the re-growth of highly doped n+ GaN regions in the recess and a Si₃N₄ layer grown earlier was used as mask. The re-growth was done at various temperatures and the morphology
was optimized by precursor flow. Morphology, before and after re-growth, was examined by JEOL JSM 6400 scanning electron microscopy at 5kV. Si$_3$N$_4$ layer was removed with 10% HF and a 300Å of gate dielectric was deposited. The contact regions were also identified by the photolithography process followed by a Ti-Al-Mo-Au ohmic metal deposition using e-beam and lift off.

Figure 6.1 shows the actual device that was fabricated and characterized. This device has two gate fingers (for a MOSFET) and hence the measured device is two n-i-n structures in parallel. Figure 1 also shows the SEM images of the re-growth region. The thickness measured by Dektak profilometer was 300nm. The morphology looks smooth with pits on the surface as seen in the SEM images. The origin of these pits is possibly due to artifacts arising during the recess etching prior to re-growth.

6.3 Physical Model

The band diagram of a space charge limited region with n type contacts in thermal equilibrium is shown in figure 6.2. With a positive bias on one of the contacts (referred to as the drain) the barrier for carrier injection on the source side is lowered as shown in figure 6.3. Because of the lack of doping in the intrinsic region, space charge limited transport occurs.

6.3.1 Space Charge Limited Transport

Space charge limited transport in an intrinsic semiconductor can be calculated by solving the drift diffusion and poisson’s equations in the intrinsic region. The contacts are assumed to be infinite sources of carriers. The

$$J = q\mu_n nE + qD_n \frac{dn}{dx}$$  \hspace{1cm} (6.1)
$$\frac{dE}{dx} = -\frac{q}{\epsilon} n$$  \hspace{1cm} (6.2)

Substituting for $n$ from the first equation into the second and integrating we end up with

$$J_x = -\mu_n \frac{E^2}{2} - \mu_n \epsilon \frac{kT}{q} \frac{dE}{dx} + C$$  \hspace{1cm} (6.3)

where $C$ is a constant of integration. The second term in this equation can be neglected if
Because of low background doping in the region, we can approximate the electric field to be constant from the source to the drain and it can be estimated as $E = V/L$. Using this approximation, it can be easily shown that the inequality is satisfied for voltages greater than the thermal voltage (26 mV at room temperature). Above room temperature, with the second term neglected it can be easily shown that the current density is given by the Mott-Gurney limit:

$$J = \frac{9\epsilon\mu_n V^2}{8L^3}$$  \hspace{1cm} (6.4)

Grinberg and Luryi [2] presented an in-depth analysis of space charge limited transport in an n-i-n structure and came to the conclusion that with a drain bias $V_D > 10 \cdot \frac{kT}{q}$,
the IV characteristics of these devices exhibit square law behavior given by the Mott-Gurney limit. This equation holds in the high current or short base limit. Under low current conditions, the device essentially follows ohms law and the current is given as [1]:

\[ J_n = \frac{q\mu_n n_o V_d}{L} \] (6.5)

where \( n_o \) is the electron concentration in the semiconductor. There is a transition region between the two limits where the currents can be calculated from the accurate analysis.

6.4 Electrical Characterization and Analysis

DC current voltage (IV) characteristics of the n+i-n+i structures were measured up to 25V using the HP4142B DC source. S-parameters were also measured from 45 MHz to 5 GHz using the HP 8510C network analyzer to extract the capacitance of the device.

The characterized devices have a drain to source spacing of 1.9 \( \mu \)m and a gate width of 2x75 \( \mu \)m. Using the fabricated junction depth of 0.3 \( \mu \)m and a dielectric constant of 9.5 for GaN, the extracted value of electron mobility is 85 cm\(^2\)/V\cdot s (figure 6.4). The figure indicates that the measured IV characteristics are not modeled well in the low bias region. If a uniform trap distribution is assumed in the channel layer, the current density is given as [3]:

\[ J_n = \frac{2qn_o \mu_n V_{DS}}{L} \exp \left( \frac{2\varepsilon}{qN_t L^2 kT} V_{DS} \right) \] (6.6)

Using these characteristics, the product of \( n_o \cdot \mu_n \) can be extracted from the multiplication factor outside the exponential while the trap density can be extracted from the constant within the exponential. This characteristic fits the measured data within an error of 1%. The extracted trap density \( N_t \) was 1x10\(^{17}\) cm\(^{-3}\) and \( n_o \cdot \mu_n \) was calculated to be 8.71x10\(^{15}\) cm\(^{-1}\)V\(^{-1}\)s\(^{-1}\). Assuming an electron mobility of 250 cm\(^2\)/V\cdot s in the channel [3], the calculated value of background doping in the channel layer is 3x10\(^{13}\) cm\(^{-3}\). The extracted trap density compares well to similar results reported in [5].

6.4.1 High Frequency Characterization

Capacitance was extracted from the measured S-parameters using the 3 element model of series resistance, parallel resistance and capacitance as shown in figure 6.5. The
Figure 6.4: Measured and modeled characteristics of a 2 finger, 75 μm unit gate width n-i-n structure.
Figure 6.5: Three element equivalent circuit used to extract capacitance of the n-i-n structure.
extracted capacitance is independent of bias and frequency from 50 Mhz to 5 GHz is approximately equal to 65 fF. The n⁺-i-n⁺ structure is expected to have a constant capacitance because of the absence of a bias dependent depletion region.

6.5 Summary

n-i-n structures with re-grown source drain regions were characterized and modeled using space charge limited transport. The current voltage characteristics were modeled accurately by assuming a uniform trap distribution in the bulk material. The devices are used to test the success of low temperature epitaxial growth process for fabricating carrier rich source drain regions.
References


Chapter 7

Conclusions and Future Work

7.1 Conclusions

This work focused on developing a comprehensive characterization and modeling methodology of III-N MOS-HFETs for high frequency applications. AlGaN/InGaN/GaN MOS-HFETs with Ga$_2$O$_3$/Gd$_2$O$_3$ oxide were characterized. Long channel devices (FAT-FETs) exhibited a transconductance peak in forward bias at a gate voltage of 3V. This is not the behavior expected of an HFET. The increased transconductance in forward bias was accompanied by a high gate capacitance extracted from small signal S-parameter measurements. The results indicated presence of a conducting channel with mobile charge under forward gate bias.

An equivalent circuit model was developed for a MOS-varactor utilizing the same layer structure as the MOS-HFET. The model was developed from observed small signal characteristics over a wide gate bias range from -8V to 6V. Equivalent circuit parameters of the model have been related to physical sources in the device. The modeled s-parameters matched measured s-parameters over the entire bias range of operation of the device (from -8V to 6V). Gate capacitance extracted from this model clearly indicated the formation of a conducting accumulation channel in forward bias with a capacitance of 850 pF which is in the expected range of the gate oxide capacitance for a 100x1.4 $\mu$m$^2$ device. Dielectric constant of the gate insulator was estimated to be 9.3 using the extracted value of gate
capacitance in forward bias which is close to the normally reported value of 10.0 for Ga$_2$O$_3$.

A charge control model was developed to study the behavior of the device in a greater detail. The model was based on the triangular well approximation of the quantum well at the hetero-interface. Donor neutralization and free carrier generation in the barrier layer were taken into account. The model predicts measured gate capacitance over a gate bias range of -7V to 1V. In the subthreshold region, the model cannot reproduce the modulation of charge in the InGaN layer. In forward gate bias, the model loses validity as the concentration of free charge in the barrier layer increases. This is a result of neglecting charge in the barrier layer while calculating sheet charge density in the channel at the heterointerface. This was done to simplify the model formulation which otherwise requires a numerical integration to estimate the charges self consistently. The model indicated the start of charge transfer into the barrier layer at a gate bias of -3V and an increase in free electron concentration beyond 0V. This correlates with the observed increase in experimentally determined capacitance at a gate bias of -2V which is expected to commence with donor neutralization in the barrier layer.

In the next part of the work, small signal modeling methods for FETs were developed and an analytical direct extraction procedure to extract equivalent circuit parameters (ECPs) was been outlined. This was applied to extract the ECPs of MOS-HFETs over a gate bias of -8V to 5V at a drain bias of 10V. Gate leakage was high in these devices which was accounted for by adding leakage resistances in parallel to $C_{gs}$ and $C_{gd}$. The devices showed significant transconductance in forward bias which allows an enhanced gate swing with increased linearity for circuit applications. The series resistances $R_s$ and $R_d$ vary with bias due to real space transfer into the AlGaN barrier layer. Initially, a two step process to extract ECPs in the presence of bias dependent series resistances was adopted. This method included an optimization step. The extraction process was modified by developing a purely analytical method to extract series resistances with varying gate bias using cold FET measurements. The modified extraction procedure does not involve any optimization steps.

The modeling work was extended by developing a large signal model for the III-N MOS-HFET. A linear charge control model has been utilized in this initial attempt. The model takes into account velocity saturation in the channel by utilizing a first order solution of the quasi-2D Poisson equation. The implementation requires a newton loop inside the model to find the position in the channel where carriers attain saturated velocity. Mobility
has been modeled using the Trofimenkoff equation. Low field mobility is modeled using an expression that takes temperature and doping dependence into account. A technique to estimate mobility in the channel has been developed. This method uses the output conductance and gate capacitance data from cold FET measurements to estimate low field mobility as a function of transverse electric field. Thermal resistance of the device was estimated using output conductance data extracted from the equivalent circuit model and measured y parameters. This method allows estimation of channel temperature. Using this method the channel temperature was estimated to be 870 °K (600 °C) at a DC power dissipation of 5 W/mm. Cooke’s expression is used in the large signal model. For the device structure investigated, the model predicted a thermal resistance of 83.5 °K·mm/W in agreement with the experimentally extracted value of 81 °K·mm/W. Capacitances were modeled by partitioning the total channel charge between the source and drain using a first moments technique. This was adopted instead of using a capacitance based description in order to ensure charge conservation in the model. The model matches measured small signal parameters over a gate bias range of of -6V to -3V within an error of 25%. $V_t$ is also modeled within 20% upto -4V on the gate. However, the model deviates considerably from measurements at high gate biases, possibly due to charge compression in the channel. The capacitance model requires investigation to ascertain the reasons behind the inaccuracies. Finally, n-i-n structures fabricated as test devices to demonstrate carrier rich source drain regions for development of enhancement mode GaN MOSFETs were characterized and modeled. Space charge limited transport was observed in these devices. The measured current voltage characteristics are described by the Mott-Gurney relationship. However, a deviation between the Mott-Gurney law and measured characteristics in the low voltage regime was observed. Assuming a uniform distribution of traps within the band gap of the material, we were able to model the measured characteristics very accurately. The trap density is estimated to be $10^{17} \text{cm}^{-3}$. Further work is required to investigate these results thoroughly.

\section*{7.2 Future Work}

This research lays the groundwork for subsequent research which can lead in various directions. An important result from the characterization work has been the demon-
stration of a conducting channel at forward gate bias with mobile charge. Based on the results obtained from the initial III-N MOSHFETs two different options can be considered. The first option is to re-design the studied device to overcome the following limitations:

- High series resistances reduce linear range of operation and the maximum available power from the device due to increased knee voltages.

- Low thermal conductivity sapphire substrate leads to high channel temperatures of the order of 850 °K. Thermal nonlinearities adversely impact performance of amplifiers by introducing memory effects that lead to degradation in circuit and system characteristics such as intermodulation products and spectral regrowth.

- InGaN layer should be undoped (or unintentionally doped) in order to increase mobility and decrease output conductance in subthreshold region.

- Increasing the conduction band discontinuity at the heterointerface will delay the onset of real space transfer of charge into the barrier layer, thus enhancing the linear range of operation of the device. Conduction band discontinuity increases as the Al content in the barrier layer is increased. However, it should be noted that the polarization charge density also increases driving the threshold voltage more negative, which is generally undesirable.

The second option, based on the results from this work and related work around it, is to consider the development of enhancement mode III-N MOSFETs. For a MOSFET, identifying a compatible gate dielectric with low density of interface states is the critical step. The results presented here indicate that the Gallium Gadolinium Sesquioxide does form such an interface. This dielectric system suffers from the drawback of having a small conduction band discontinuity with GaN, which can lead to higher gate leakage currents than other dielectrics such as SiO$_2$. A successful MOSFET also requires a carrier rich source drain region which is hard to achieve in the III-N materials due to the inherent difficulties in doping the materials and also in activating the dopants. Innovative techniques will have to be developed to overcome this obstacle. One such attempt has already been made with the demonstration of re-grown source drain regions using the lateral epitaxial overgrowth technique. The challenges in developing and demonstrating a high performance III-N MOSFET are numerous. However, given the advantages of a MOSFET over an HFET
as outlined in chapter 2, this direction of research should prove to be the more rewarding and exciting one.

The characterization and modeling methods developed in this study also throw up various opportunities. A clear understanding of charge control in these III-N MOS-HFETs would require a self consistent solution of the Schroedinger Poisson equation. This is a significant undertaking but should prove to be a valuable tool in the investigation of small dimension MOSFETs. The impact of surface states on the sheet charge density needs to be investigated - analytically as well experimentally. An extension of the physical charge control model based on the triangular well approximation, taking a self consistent approach would be useful to confirm the validity of the model in forward gate bias region as well. This model can prove to be a useful tool in the optimization of the MOS-HFET structure for improved performance.

The mobility model needs to be verified and further work can be carried out on extraction of mobility at varying temperatures. This can be used to model temperature dependence of mobility accurately. Pulsed IV measurements have to be introduced into the characterization procedure to estimate and separate trapping and thermal time constants and the effects arising out of these phenomena. To extend the model into MOSFET region of operation, a modification of the charge control model taking into account subthreshold conduction and saturation of sheet charge density in forward bias is required. Such a model would introduce empirical parameters. In such a case, a self consistent extraction methodology for those parameters should be developed along with the model.

The large signal model can be improved in several areas. Improvements in the charge and capacitance modeling are required to match the measured high frequency data better. An extension of the model to include non quasi static effects would be required if the devices are expected to operate close to $F_T$. The mathematical conditioning of model equations needs to be tested rigorously under large signal simulations. Small signal $S$ parameter simulations indicate that the derivatives of capacitance equations might be discontinuous at the transition from linear to saturated region of operation. To overcome this, mathematically robust formulations have to be developed to remove discontinuities at the transition regions. Gate currents from tunneling have been characterized but not modeled in this work and this can form the basis of further work to characterize the behavior of different dielectrics on GaN.
Appendix A

Integrated Expressions for Drain and Source Charges

The integrated charge equations are presented in this appendix. As discussed in chapter 5, the drain and source charges are obtained by partitioning the channel charge using the first moment technique. The drain charge is given as:

\[ Q_D = -\frac{W C_{\text{eff}}}{L} \int_0^L x z (x) \, dx \]  

(A.1)

Recalling that the channel potential \( z(x) \) is fixed at \( z_{L_1} \) beyond \( x = L_1 \), the integral is split into two parts:

\[ Q_D = -\frac{W C_{\text{eff}}}{L} \left[ \int_0^{L_1} x z (x) \, dx + \int_{L_1}^L x z_{L_1} \, dx \right] \]  

(A.2)

where \( z(x) \) is the channel potential in the linear region of the channel and is given as:

\[ z(x) = -\frac{K_0 (x + \alpha z_0)}{2 (1 - K_0 \alpha)} + \frac{\sqrt{K_0^2 (x + \alpha z_0)^2 + 4 z_0^2 (1 - K_0 \alpha)}}{2 (1 - K_0 \alpha)} \]  

(A.3)

where \( K_0 = \frac{2 v_{\text{sat}}}{\mu} \). Integrating the first part of the integral from 0 to \( L_1 \), we first consider the term outside the square root in the expression for \( z(x) \). This term integrates (over 0 to \( L_1 \)) to:

\[ Q_{D11} = -\frac{K_0}{12 K_2} \left( 2 L_1^3 + 3 \alpha z_0 L_1^2 \right) \]  

(A.4)
where \( \alpha = \frac{1}{E_{C_1}} \) and \( K_2 = 1 - K_0 \alpha \) are as defined in chapter 5. Focusing on the term within the square root, the expression can be written as \( u^2 - a^2 \) or \( u^2 + a^2 \) depending on whether \( \frac{4z(0)K_2}{K_0} < 0 \) or vice versa. Here \( u = x + \alpha z_0 \) and \( a^2 = \frac{4z(0)^2K_2}{K_0} \) if \( \frac{4z(0)K_2}{K_0} < 0 \) or \( a^2 = \frac{4z(0)^2K_2}{K_0} \) if \( \frac{4z(0)K_2}{K_0} > 0 \). With this in mind, two solutions are possible to this part of the integral. When \( \frac{4z(0)K_2}{K_0} < 0 \), indefinite integration of the term results in:

\[
Q_{D12} = \frac{a^2\alpha z_0 \log \left( \frac{2\sqrt{u^2 - a^2} + 2u}{2} \right)}{2} + \frac{(u^2 - a^2)^{1.5}}{3} - \frac{\alpha z_0 u \sqrt{u^2 - a^2}}{2} \quad (A.5)
\]

The definite integral is calculated by replacing appropriate limits for \( u \), given as, \( u = \alpha z_0 \) and \( u = L_1 + \alpha z_0 \). Under the second condition, when \( \frac{4z(0)K_2}{K_0} > 0 \), the integral is calculated to be:

\[
-\frac{a^2\alpha z_0 \sinh^{-1} \left( \frac{u}{|u|} \right)}{2} + \frac{(u^2 + a^2)^{1.5}}{3} - \frac{\alpha z_0 u \sqrt{u^2 + a^2}}{2} \quad (A.6)
\]

Once again, the charge from this term is calculated by using the limits in terms of \( u \), defined above. The third term in the original integral from \( L_1 \) to \( L \) is integrated to:

\[
Q_{D2} = \frac{zL_1}{2} \left( L^2 - L_1^2 \right) \quad (A.7)
\]

At this point, all components of charge have been calculated and the total drain charge is given as:

\[
Q_D = -\frac{WC_{Geff}}{L} [Q_{D11} + (Q_{D12} (L_1 + \alpha z_0) - Q_{D12} (\alpha z_0)) + Q_{D2}] \quad (A.8)
\]

Depending on the sign of \( \frac{4z(0)K_2}{K_0} \), the expression for \( Q_{D12} \) changes between the two expressions listed above. This solution has potential for discontinuities in the higher order derivatives and in fact, the capacitances extracted from simulated S parameters show a kink under certain bias conditions. The piecewise form of this expression directly results from the piecewise form chosen for the mobility equation. An alternative to this would be to use the smoothly saturating expression discussed in chapter 5. However, the solution developed here is the complete charge equation for the chosen expression for mobility.

The source charge is also obtained following a similar formulation and will not be repeated here. In fact, the source charge is simplified to:

\[
Q_S = -WC_{Geff} \int_0^L z(x) \, dx - Q_D \quad (A.9)
\]

The first integral is similar in form to the expression integrated above, except for the absence of \( x \) as a multiplying factor in the integral. This is a standard form that can be found in a calculus textbook.