ABSTRACT

LI, DING. **Modeling and design of a transient voltage clamp assisted voltage regulator.** (Under the direction of Dr. Alex Q. Huang.)

New power management techniques for microprocessor have been introduced as well as the CPU technology itself advanced. One solution is to decrease the power supply voltage such that total power loss is reduced. From the introduction of Intel Pentium processor, a non-standard supply voltage which is less than 5V was adopted. From then on, CPU supply voltage keeps decreasing. On the other hand, the increasing transistors count in microprocessor demands a continuously increase of microprocessor's current.

The fundamental requirements for Voltage Regulators (VR) are: (1) small voltage deviation during fast dynamic transients from light load to heavy load and vice-versa. This requirement becomes tighter when supply voltage goes below 1V. (2) High power density due to the limited motherboard space. (3) High conversion efficiency (low power loss) because of the thermal management capability of the computer cooling system. All those requirements pose serious challenges for the VR design.

To meet the transient requirements, the concept of adaptive voltage position (AVP) design [4] was invented. Prior to this idea emerged, feedback control regulates the output voltage at a single point for the entire load range. As a result, the output voltage spike during load transient had to be smaller than half of the voltage tolerance window. However, if the output voltage drops with load increasing, the whole voltage tolerance range can be used for the voltage jump or drop during the transient. Another benefit of the AVP design is that the VR output power at full load is reduced, which greatly facilitates the thermal design. If the transients between the two steady states have no spikes and no oscillations, the AVP design

is optimal. The relation between the current and output voltage waveform reveals that the VR can be modeled as an ideal voltage source in series with a resistor Ro. In frequency domain, the output impedance of VR should keep constant from DC to high frequency.

In recent years the output current has increased while output voltage decreased. More and more space of the motherboard will be occupied by VRs, especially the output capacitors. It seems that high frequency is becoming the only solution to increase power density and save space. However, the conventional interleaving buck converter's performance suffers a lot as switching frequency increases. The main reason is that switching loss increases proportionally to frequency. Eventually the heat caused by power loss will reach the system designed thermal limit.

Transient voltage clamp (TVC) works in parallel with the switching regulator to achieve fast voltage regulation without bulk capacitors. At the mean time, switching frequency of main VR needs not to be increased. Traditional switch-mode regulators suffer from its slow transient response due to limited control bandwidth hence large output voltage spike. TVC is a parallel branch that will replace the bulk capacitors. Therefore, its AC output impedance should also match the impedance of bulk capacitors. According to the relationship between the parallel impedances on the microprocessor power delivery path, dynamic branch currents distribution causes high TVC current during load transient. A non-linear TVC control scheme is then proposed to achieve highest VR inductor current slew rate during load transient.

The power loss in the TVC circuits is the key issue which will prevents TVC from industrial applications. An extended total efficiency is defined as output energy divided by input energy during a period of time. By replacing the bulk capacitors with linear-type TVC, an extra loss

is added. It seems that this TVC loss is directly proportional to load transient frequency. Under such assumption, total efficiency degrades as load transient frequency increases. However further analysis with related to parallel impedances shows that this is not true. Due to high impedance at higher frequency, TVC will not respond to such high load transients. The maximum power loss in TVC is limited by the second “zero” of its impedance.

A two channel VR was built to evaluate the TVC performance in terms of transient response and power loss. Experimental results verified the aforementioned concepts and non-linear control scheme. Measured power loss in TVC is low and the transient response is comparable with the traditional bulk capacitors solution.

Modeling and design of a transient voltage clamp assisted voltage regulator

by

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Dr. Alex Q. Huang, Chair of the Advisory Committee

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Dr. Subhashish Bhattacharya Dr. Kevin Gard

To My Wife

Qiong Shi

BIOGRAPHY

Ding Li was born in Wuhan, Hubei, China in 1975. He received his Bachelor degrees in Electrical Engineering in 1997 and in Economics in 1998 from South China University of Technology respectively. Later, he joined Emerson Network Power Co., Ltd in China and had been working as an electrical engineer designing switch mode DC-DC converters. In 2003 he entered Virginia Tech as a master's student in Electrical Engineering. He had been working as a research assistant in Center for Power Electronics Systems for one year. From 2004 to 2006, he has been with Semiconductor Power Electronics Center in North Carolina State University, where he has done research on DC-DC voltage regulator for microprocessor power delivery and power management integrated circuits.

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I would like to extend a special thanks to all students at SPEC for their support and warmness. Encouragement from my friends outside of SPEC was also really helpful, and their support was really valued.

My heartfelt appreciation goes toward my parents, who have always encouraged me to pursue higher education. Finally, I thank my wife, Qiong Shi for her support and encouragement throughout my education, and my lovely son, his innocent smile keeps me always in a good mood no matter how challenging the situation will be. Their support means everything to me.

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CHAPTER 1 Introduction

1.1. Background: Voltage Regulators

The Moore's law, which states "transistor density doubles every eighteen months", has successfully predicted the evolution of microprocessors, as shown in Fig 1.1 [1]. It is predicted that in 2015, there will be tens of billions of transistors in a single microprocessor [2].

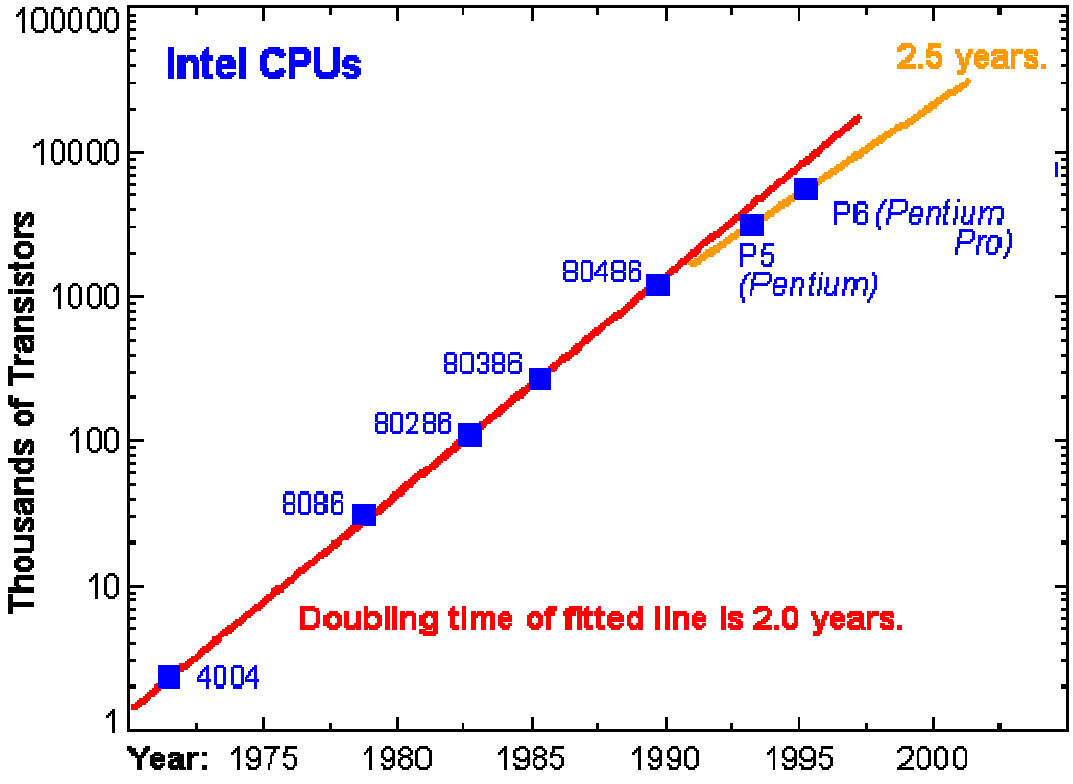

Fig.1.1 Moore's Law for Intel CPUs
April 20, 2000: The End of Moore's Law, from Technology Review

As the transistor count increases, microprocessor's computing performance also improves. As shown in Fig 1.2, the computing speed also followed the Moore's law in the past decades. However more transistors squeezing into the smaller spaces not only results in higher performance but also increases the power consumption of the microprocessor.

Today's technology enforces three percent power consumption of the microprocessor in order to achieve one percent of its performance improvement. [2] Because all the power consumed by CPU finally transferred to heat, stringent challenges have been posed on the thermal management. Eventually it becomes the barrier to prevent microprocessor from continuously improve its computing performance.

New power management techniques for microprocessor have been introduced as well as the CPU technology itself advanced. One solution is to decrease the power supply voltage such that total power loss is reduced. From the introduction of Intel Pentium processor, a non-standard supply voltage which is less than 5V was adopted. From then on, CPU supply voltage keeps decreasing. On the other hand, the increasing transistors count in microprocessor demands a continuously increase of microprocessor's current. [3] Fig 1.3 gives us the clear picture.

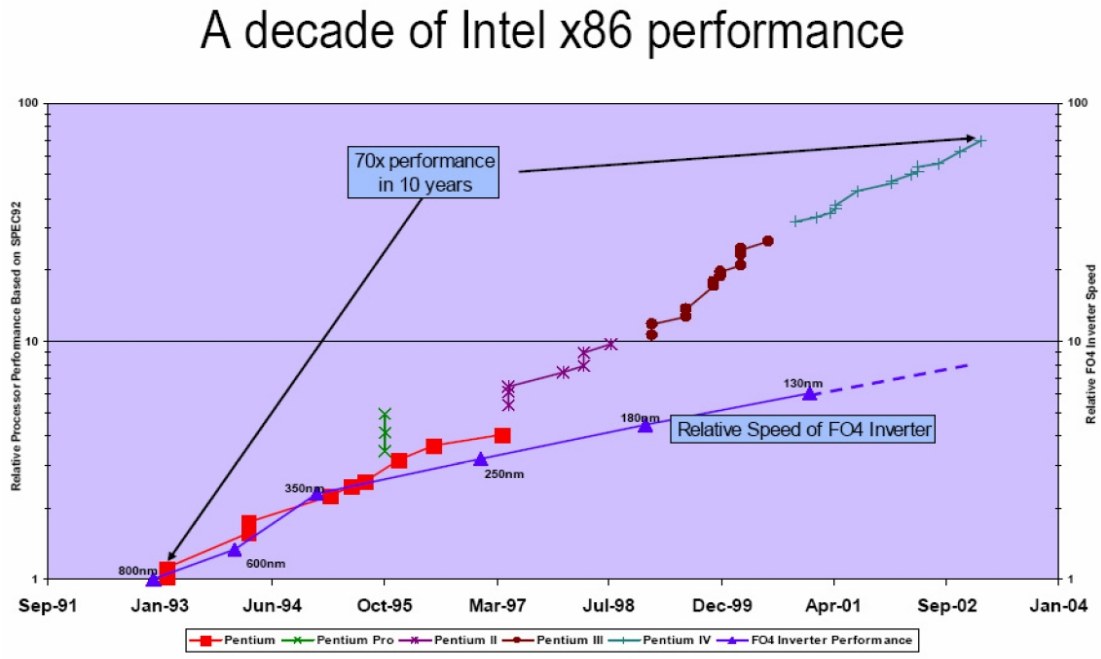

Fig.1.2 A decade of Intel x 86 performances

Fall 2005, from NC State University ECE521 Class notes

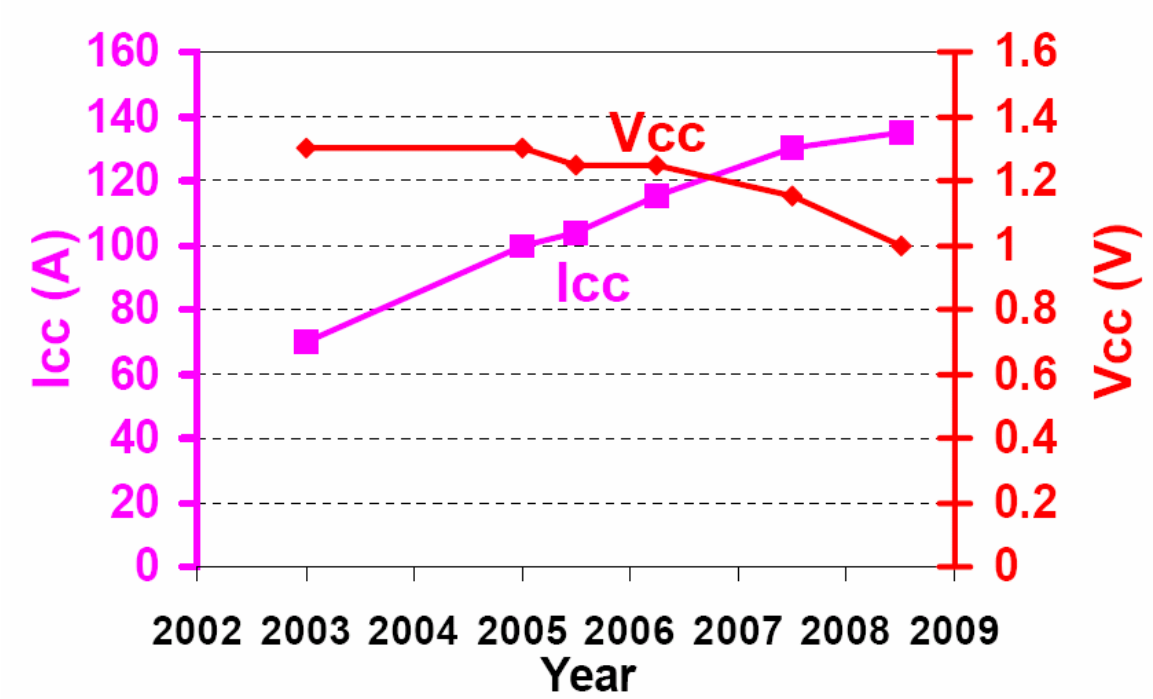

Fig.1.3. the roadmap for processor's required voltage and current

Although new technologies such as the multi-core structure for microprocessor may slow down the trend, it is expected that the challenges to the power supply is still strict. [3] Furthermore, due to the high computing speed, the microprocessor's load transition speed also increases. At the mean time, the voltage deviation window during the transient is becoming smaller and smaller since the output voltage keeps decreasing. The low voltage, high current, fast load transition speed, and tight voltage regulation impose challenges on the power supplies of the microprocessors.

In the early days, microprocessors were powered by a centralized silver box which provides 5V legacy voltage level. Due to the parasitic inductance and resistance of the interconnection between silver box and microprocessor, power quality is severely jeopardized. And it is no longer practical for the bulky silver box to provide energy directly

to the microprocessor for such low-voltage high-current applications. Therefore, the voltage regulator (VR) was introduced as the dedicated power supply.

In order to minimize the impact of parasitic impedance on the VR transient response, VRs need to be located very close to the microprocessors. There are basically two types of VRs: VR modules (VRM), which can be plugged into a standard socket on the motherboard, and the on-board VR (VRD), which is built directly on the motherboard, as shown in Fig 1.4. VRD can eliminate the problematic and costly connector that comes with VRMs. Most of today's low-end computer systems use VRD.

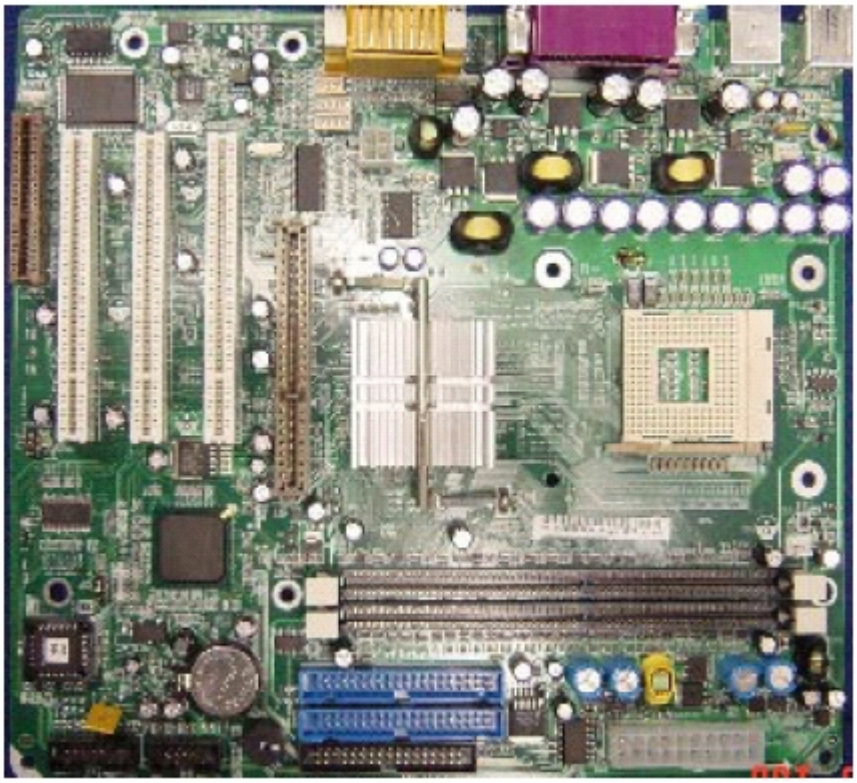

Fig.1.4 On board VR (VRD) on a motherboard based on Pentium IV microprocessor

The fundamental requirements for VRs are: (1) small voltage deviation during fast dynamic transients from light load to heavy load and vice-versa. This requirement becomes tighter when supply voltage goes below 1V. (2) High power density due to the limited

motherboard space. (3) High conversion efficiency (low power loss) because of the thermal management capability of the computer cooling system. All those requirements pose serious challenges for the VR design.

To meet the transient requirements, the concept of adaptive voltage position (AVP) design [4] was invented. Prior to this idea emerged, feedback control regulates the output voltage at a single point for the entire load range. As a result, the output voltage spike during load transient had to be smaller than half of the voltage tolerance window. However, if the output voltage drops with load increasing, the whole voltage tolerance range can be used for the voltage jump or drop during the transient. Fig. 1.5 shows the transient comparison between non-AVP and AVP designs. It is clear that the AVP design allows the use of fewer output capacitors. Another benefit of the AVP design is that the VR output power at full load is reduced, which greatly facilitates the thermal design. If the transients between the two steady states have no spikes and no oscillations, as shown in Fig. 1.6 (a), the AVP design is optimal. The relation between the current and output voltage waveform reveals that the VR can be modeled as an ideal voltage source in series with a resistor Ro, such that:

$$Ro = \Delta vo / \Delta io \tag{1.1}$$

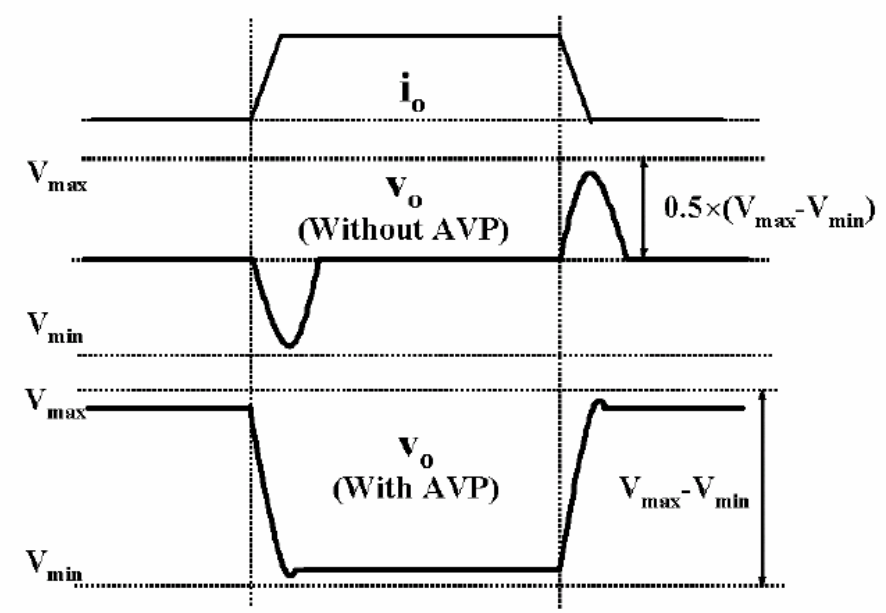

Fig 1.5 Transient response without and with AVP

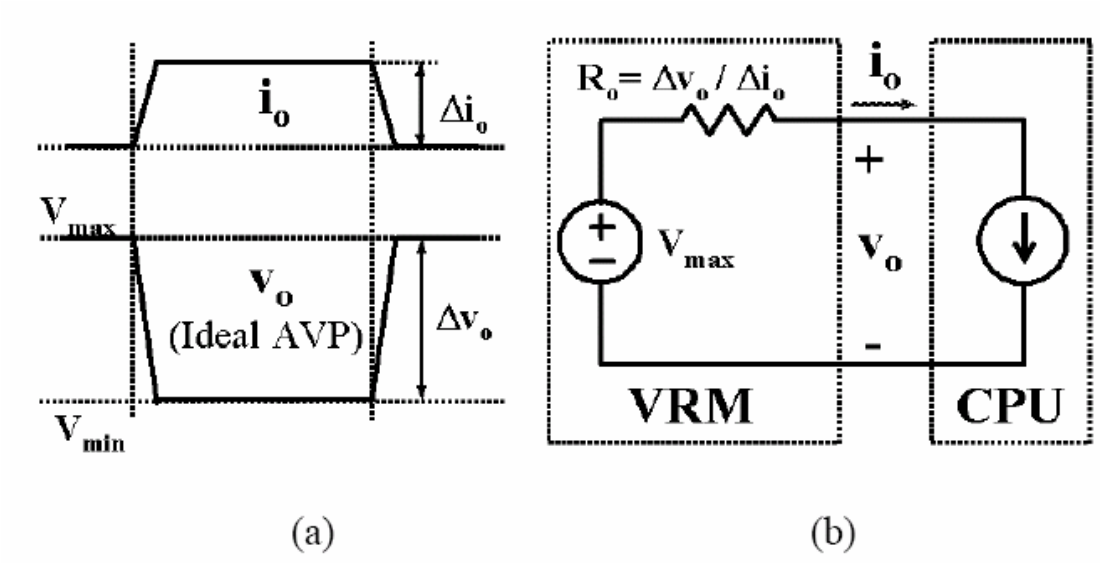

Fig 1.6 Ideal AVP design and VRM equivalent circuit

As the current rating becomes higher and higher, one single buck converter (Fig 1.7) is not sufficient to meet the requirement. Also low switching frequency requires a large filter inductor in order to keep the output voltage ripple within the specification. However large output inductor limits the energy transfer speed which means that output capacitors also need

to be large enough to suppress the output voltage spike during load transient. To reduce the output capacitors count, high inductor current slew rate is preferred so that the inductance needs to be small. However smaller inductance results in larger inductor current ripple in the steady state of circuit's operation, which means turn-off loss of switching device increases. On the other hand, larger inductor current ripple results in larger output voltage ripple. Sometimes the voltage ripple is even larger than the transient voltage spike. To shrink the output capacitance, Keep reducing filter inductance is not practical.

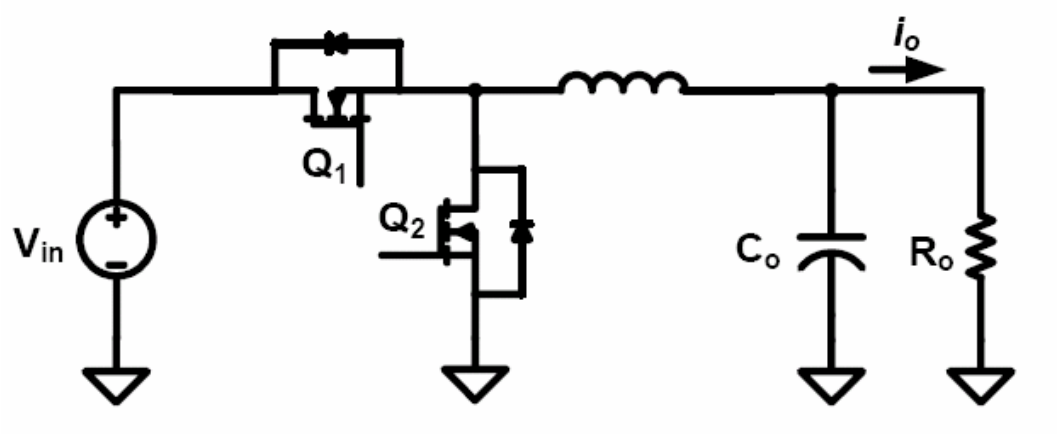

Fig.1.7 A single phase synchronous buck converter

The multiphase interleaving technique is introduced in 1990s' by phase shifting the duty cycles of adjacent channels with a degree of 360°/n, where n is the total channel number. With such multiphase buck converter, the output current ripples are greatly decreased because phase currents sum together and are partly cancelled each other (Fig 1.9). Therefore the steady-state output voltage ripples are significantly reduced, making it possible to use very small inductances in VRs to improve the transient responses.

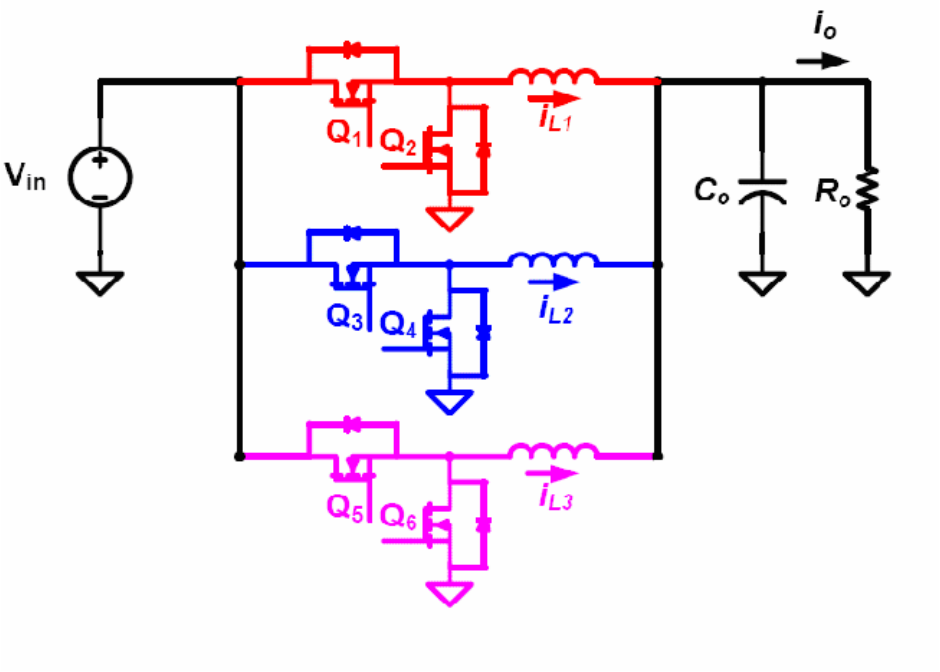

Fig.1.8 A multi-phase synchronous buck converter

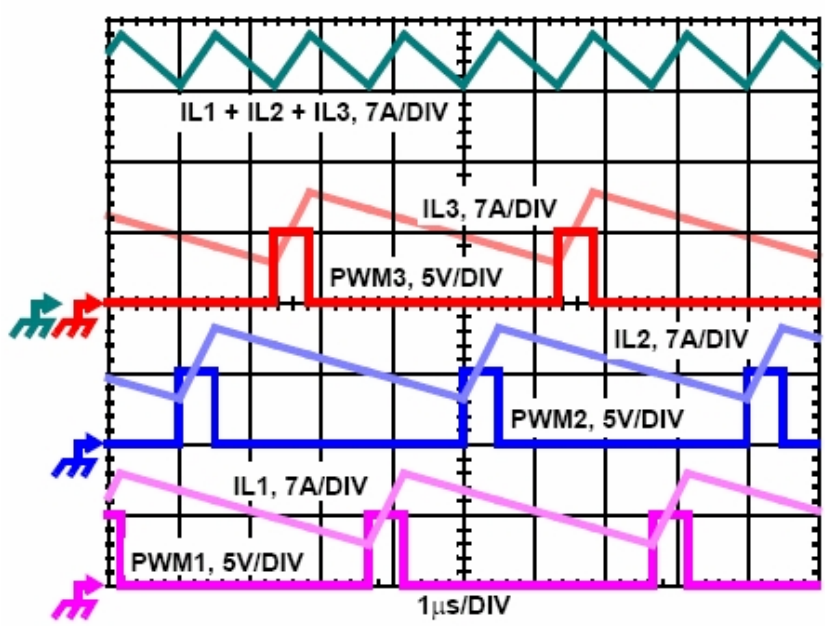

Fig 1.9 PWM and inductor current waveforms for a 3-phase buck converter

In recent years the output current has increased while output voltage decreased. More and more space of the motherboard will be occupied by VRs, especially the output capacitors. It seems that high frequency is becoming the only solution to increase power

density and save space. However, the conventional interleaving buck converter's performance suffers a lot as switching frequency increases. The main reason is that switching loss increases proportionally to frequency. Eventually the heat caused by power loss will reach the system designed thermal limit.

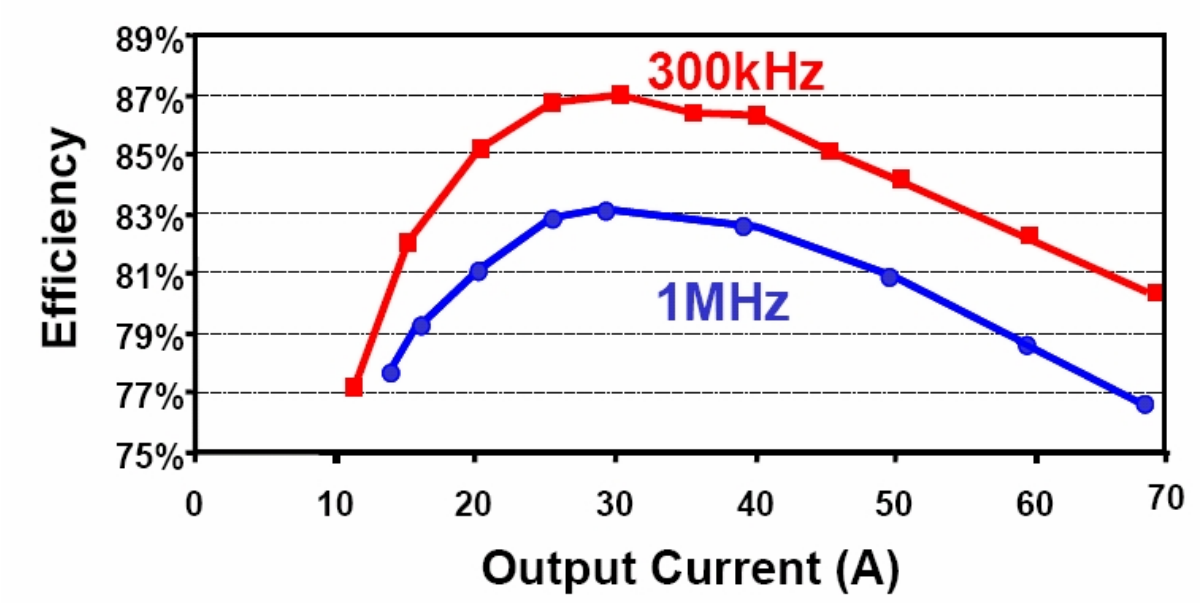

Fig.1.10 Converter Efficiency degrades with increased switching frequency
From Ren, Y., High frequency high efficiency two-stage approach for future microprocessors, Ph.D dissertation, Virginia Polytechnic Institute and State University, 2005

A two-stage VR was proposed to increase the converter efficiency. The core of two-stage structure is the high frequency, high efficiency second stage, which is composed of multi-phase buck converters and to handle the transient response. The first stage is to step down the input voltage to a certain intermediate bus voltage efficiently and simply. The high frequency is optional for the first stage. By such configuration, the switching device of second stage can be optimized more easily in terms of low loss and high switching frequency. For example, device breakdown voltage is lowered and duty cycle is extended. With increased switching frequency, VR control bandwidth can be pushed to such a high value

that the bulky polarized output capacitors can be totally replaced with ceramic caps, which means board area occupied by VR is dramatically reduced. However, the additional power stage takes up space and adds costs to VR so that it cancels the benefit of eliminating bulk capacitors.

The hybrid VR concept was introduced for the same purpose of reducing bulk capacitors. Basically it is an auxiliary regulator in parallel with the main switching VR. As the bandwidth of the auxiliary regulator is higher than the switching VR, it will help to suppress the output voltage spike during transients. Such auxiliary regulator can be switching type or linear type. Different topologies were proposed to implement the hybrid VR. In chapter two, these approaches will be discussed in more detail. The linear type regulator is the most concern in the thesis. Transient Voltage Clamp (TVC) is the name for such a regulator. The key point is that, TVC will be activated only during load transient. During the steady state operation, it should not interfere with the main switching VR. Otherwise the overall converter efficiency will be seriously reduced because of TVC power loss.

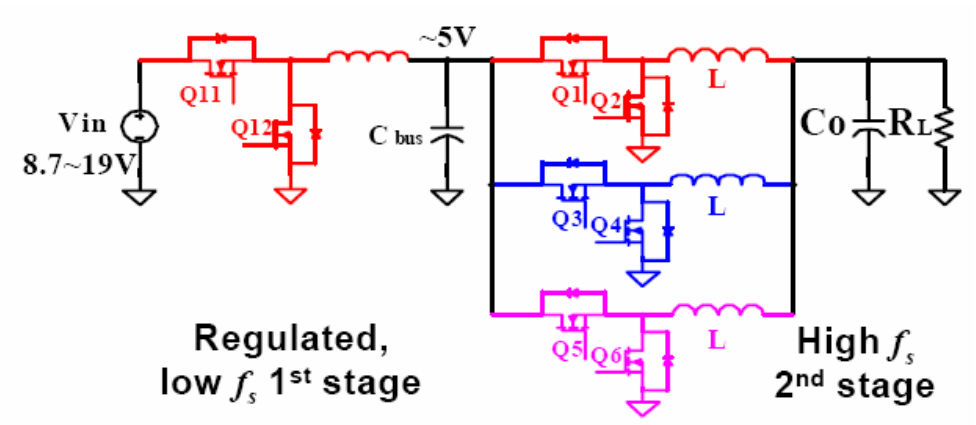

Fig 1.11 two-stage VR structure

From Ren, Y., High frequency high efficiency two-stage approach for future microprocessors, Ph.D dissertation, Virginia Polytechnic Institute and State University, 2005

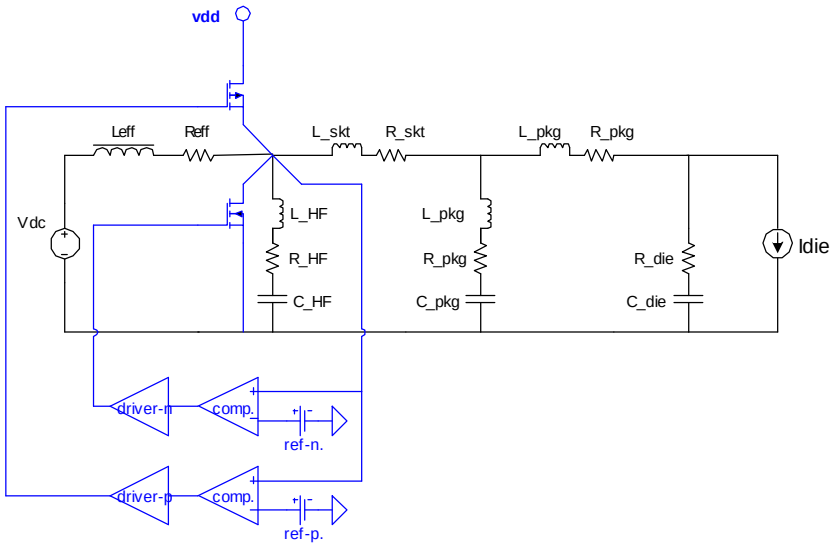

Fig 1.12 Linear-type Hybrid VR structure

Zhang, X.; Huang, A.Q., "Impacts of transient voltage clamp on CPU power delivery", Power Electronics Specialists Conference, 2004. PESC04. 2004 IEEE 35th Annual June 2004 Page(s):629 - 632 Vol.1

1.2. Objective of this work

The objective of this work is to apply Transient Voltage Clamp concept to implement hybrid VR, in which all the bulk capacitors are eliminated while keep the same load transient performance and the converter efficiency by means of keeping the main VR switching at low frequency. Fundamentally, TVC circuit plays a role as the substitute of bulk capacitors. So that bulky and expensive passive capacitors are replaced with silicon which can save both space and cost. In order to achieve this, existing transient voltage clamp structures are investigated. Parallel impedance concepts are introduced in order to analyze the currents distribution between main VR and TVC and output voltage spike during load transient. A non-linear TVC circuit with duty cycle saturation logic is proposed to minimize TVC power consumption during load transient. A two-phase buck converter with commercial VR controller working at optimized switching frequency in terms of high conversion efficiency is

designed in parallel with TVC to verify the output impedance idea and the novel non-linear TVC control. Both circuit simulations and hardware experiments are carried out.

1.3. Thesis Outline

The whole thesis is composed of five chapters. They are organized as follows. Chapter 1 is the introduction of VR background. The need for pushing VR control bandwidth is stressed. Two options are discussed: increasing switching frequency or parallel a high-bandwidth branch.

In chapter 2, several existing transient voltage clamp structures are reviewed in terms of performances based on output voltage spike and power losses.

In chapter 3, parallel output impedance concept is introduced and analyzed. A novel non-linear control of duty cycle saturation logic is proposed. By such, TVC current and VR inductor current slew rate during load transient can be maximized. TVC Power loss during load transient is minimized.

Chapter 4 introduces the hardware implementation by discrete components and related experimental verification of those ideas expressed in chapter 3.

Chapter 5 includes the summary of this work and future plan of integrated TVC circuits as the replacement of bulk capacitors.

CHAPTER 2 Literature Review on Existing Hybrid VRs

2. 1 Overview

In recent years several approaches were developed to improve VR's load transient performance. "Voltage Regulator using Switched Decoupling Capacitors" [5], the "Linear Voltage Regulator" [6], the "Single-Shot Transient Suppressor" [7], the "Load Corrector" [8], the "Active Clamp" [9], the "Hybrid Power Filter" [10], and the "Active Transient Current Compensator" [11] work as active filter to replace the traditional passive filters. However none of above methods is trying to replace the bulk capacitors. Besides, most of these approaches don't have a mechanism such that the main VR coordinates with active filter to have overall well-defined output impedance (AVP design) as well as minimizing the active filter's power loss during load transient. These limitations make the aforementioned ideas cannot be apply to industry yet.

2.2 Single Shot Transient Suppressor (SSTS)

As shown in Fig 2.1 [7], the SSTS injects electron charges to the microprocessor during load transients. Cextra has initially higher voltage than VO. Once load current increases, Saux will turn on and discharge Cextra. Therefore VO has a smaller voltage drop and Cdec can be reduced. Saux can be either triggered by detecting VO or from the CPU command. Basically there is no close-loop control of the injection current. The turn on time of Saux is arbitrary calculated and injection current is limited by Rlim. Obviously this scheme is not satisfactory because load transients are not predictable and today's CPU does

not have such a command to trigger the SSTS. However this approach give us the idea that active device can play a role as the filter to suppress VR output voltage spike.

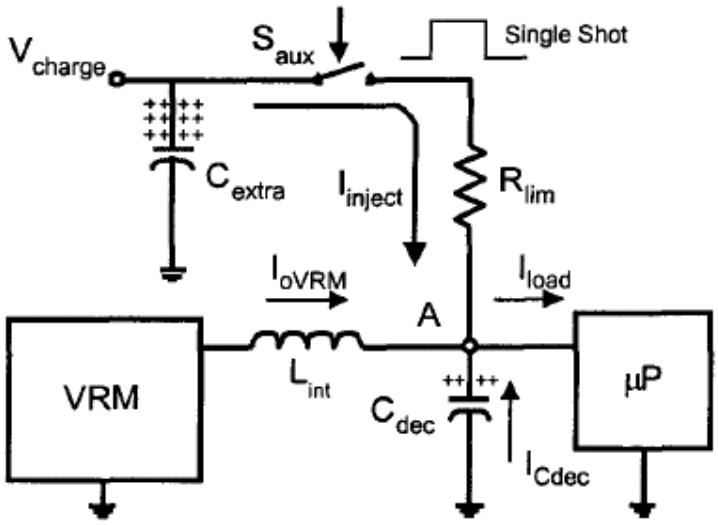

Fig 2.1 SSTS equivalent circuit during load step up [7]

2. 3 Reported Active Clamp Circuit

An improved scheme of active clamp circuit [9] was proposed and implemented in silicon. The Functional diagram is as following:

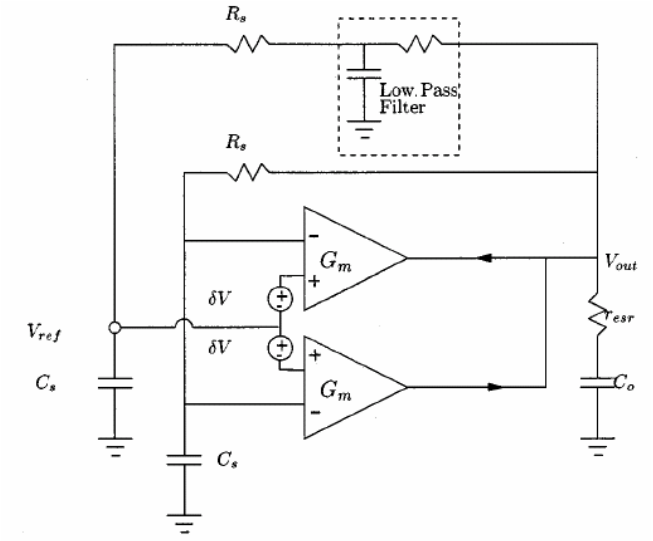

Fig 2.2 Functional schematic of active clamp circuit [9]

Vout is sensed and compared with Vref to generate the error signal which is amplified through the Gm block to a pull-up or pull-down current. This current is then injected or sinked to the output node in order to suppress the transient voltage spike. Because Gm is well controlled, the output impedance of the active clamp can be approximated as 1/Gm which can assure nearly first order smooth load transition. In order to keep active clamp from working during the steady state operation, i.e. when there is no load transition, a dead band δV is introduced (See Fig 2.3). Basically δV need to be greater than output voltage ripple so that active clamp will not be triggered all the time. Inside the Gm block, currents are amplified by multi-stage current mirrors. By this means Gm has high bandwidth.

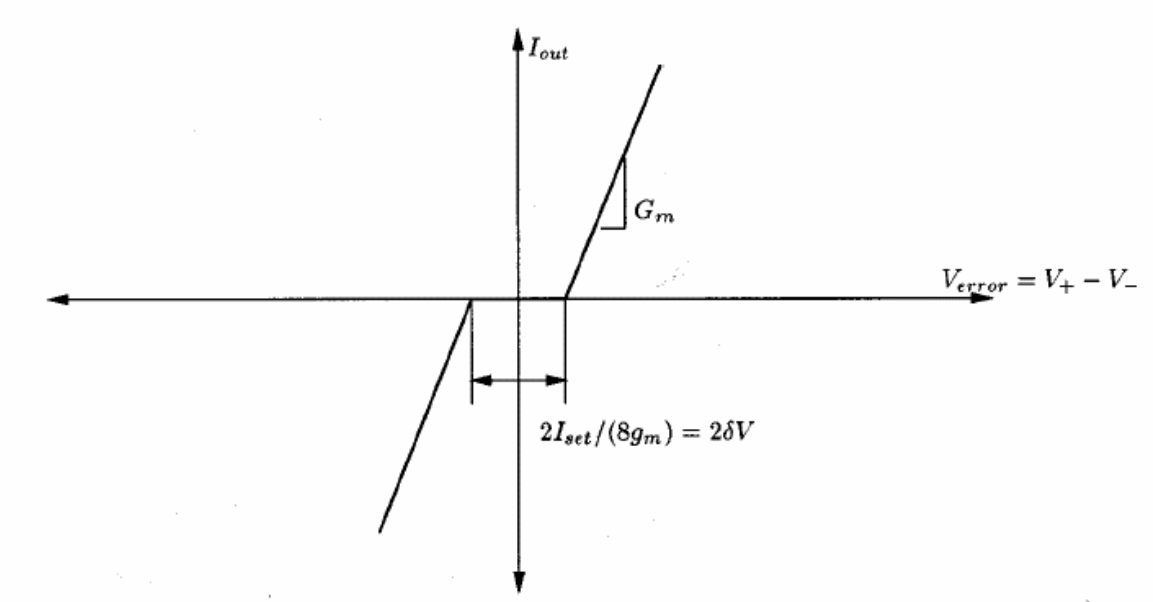

Fig 2.3 Transfer curve of output current versus input error voltage of active clamp [9]

The reference voltage Vref is generated through a low-pass RC filter directly from the output voltage. In order to get good performance, RC parameters need to be tuned carefully. Although the active clamp circuit is in parallel with switching regulator, there is no signal interaction between these two blocks. It has the benefit of independent operation, i.e. when a

designer is dealing with the switching regulator he does not need to worry about the clamp circuits. But from the power loss point of view, since all the energy stored in the inductor is dumped through the active clamp circuit during load transient, the power loss may increase dramatically if load transient frequency is high. There is no effort to minimize the power loss within active clamp during load transient.

2. 4 Active Transient Voltage Compensator (ATVC)

The linear type active clamp suffers from its high power loss because the energy is totally dissipated into transistors during load transient. A high-bandwidth switching mode regulator is then introduced to solve this problem. In [11], Active Transient Voltage Compensator is proposed. Below is the circuit diagram:

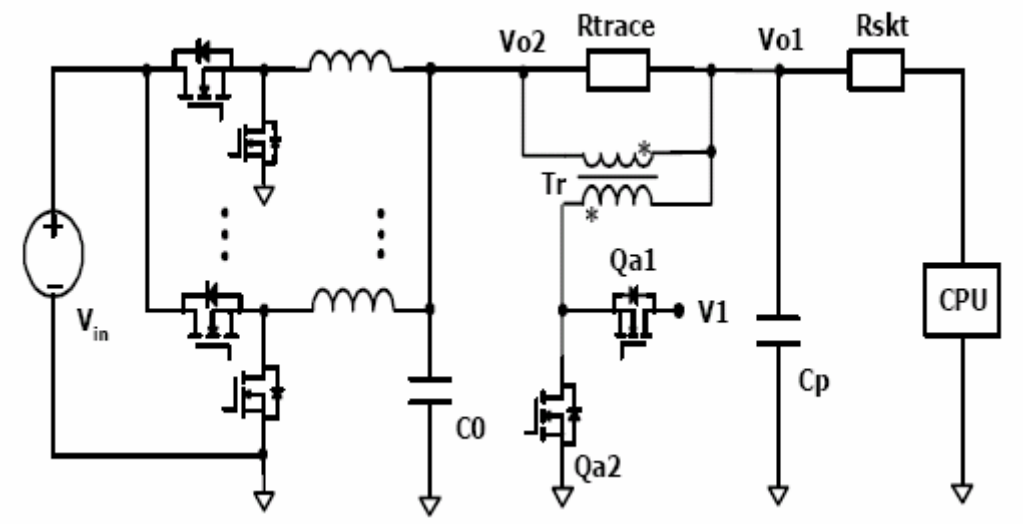

Fig 2.4 VR with parallel ATVC [11]

Basically ATVC can be considered as a bi-directional DC/DC converter. When load steps up, it delivers current to the output node as a buck converter. When load steps down, it sinks currents from the output node as a boost converter. So the power loss in ATVC during load transient is by the conduction loss and switching loss of ATVC itself, which has pretty

weak relation with the output voltage and current product. ATVC only engaged in transient periods and main VR can be optimized with better efficiency which mainly handles the dc current. Main VR switches at a frequency of 300 kHz while ATVC switches at 1.5 MHz. The transformer Tr magnifies ATVC injected current by the turns ratio thus ATVC itself will have smaller current stress.

The ATVC solution is quite decent in terms of reducing power loss during load transient. However the utilization of magnetic component (can be transformer or inductor) limit the space-saving efforts. Also ATVC's high bandwidth is due to its high switching frequency which cannot be raised unlimitedly. Finally, this is not a solution based on silicon, which means it is very hard to be integrated into a chip. All these drawbacks limit its application into the industry.

2.5 Summary

In this chapter, some active filter structures are introduced and compared. In general, linear regulator type active filters have the drawback of high power loss while switching-mode active filter has the issue of high-density integration. In order to make the transient voltage clamp as the basic building block to replace the bulky filter capacitors, special efforts need to be paid to minimize the power loss during load transient.

CHAPTER 3 Modeling and Design of a TVC- assisted Voltage Regulator

3.1 AVP and output impedance

As described in chapter 1, the AVP concept is to utilize the full voltage tolerance window for load transient. In this situation, VR can be modeled as an ideal voltage source with finite output impedance. Take Intel VRD10.0 specification for example: when there is no load VO equals to an initial value set by digital VID codes; when load current increases, VO drop according to the load line which is specified by $R_{LL.}$ This relation can be expressed as:

$$VO = VID - Io^* R_{LL} \quad (3.1)$$

However R_{LL} only specifies the DC load line which is related to VR's steady state operation. During load transient, VO can have voltage overshoot (load steps down) and undershoot (load steps up). This phenomenon is not only related to VR control bandwidth, but also related to parasitic inductance and resistance existing in the power delivery path.

The Extended Adaptive Voltage Positioning (EAVP) [12] concept was then developed to design and analyze the low impedance resonant free power delivery network, which utilizes and extends on the concept of AVP. The lumped power delivery model was adopted to simplify the analysis.

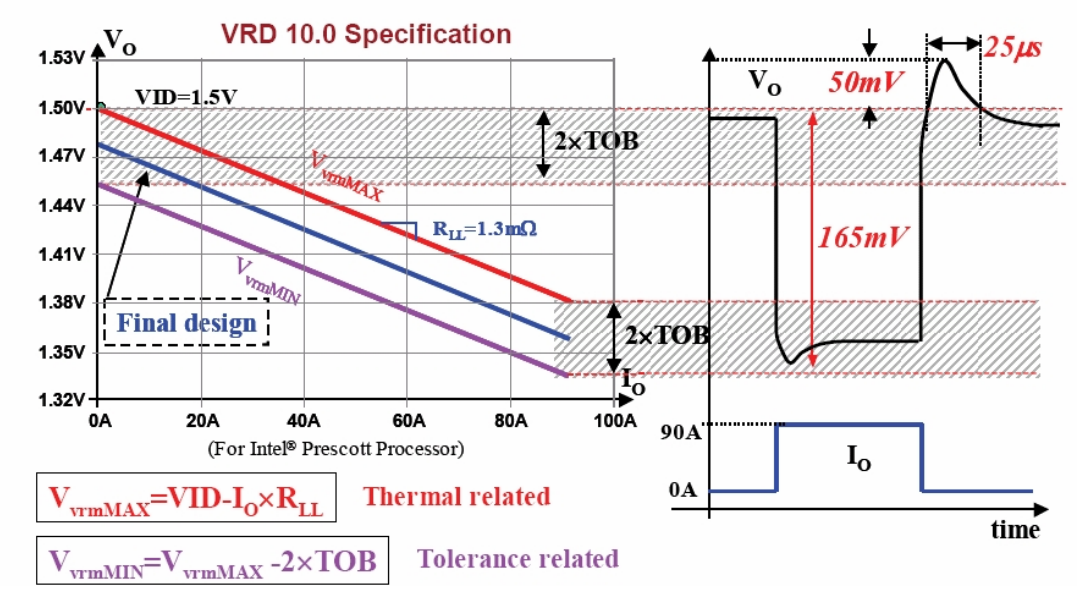

Fig 3.1 VRD10.0 load line and AVP transient response

As seen in Fig 3.2, through the microprocessor power delivery path, the parasitic inductance and resistance are lumped into one-dimension models. From left to right, the capacitors are bulk capacitors, middle-frequency (MF) capacitors, package capacitors and capacitors on die. Each capacitor branch is modeled as a serial RLC network which has an impedance transfer function of R+LS+1/(S*C), which has a U-shape bode plot. i.e., at low frequency, the slope is -20dB per decade, at the point of ESR zero, the slope becomes 0 dB per decade and at high frequency, the slope becomes +20 dB per decade because of the ESL effect. Voltage mode controlled VR combined with all those capacitors cover from DC to high frequency. An overall output impedance can be easily derived from the above bode plot. Since every impedance branch is in parallel, one can connect the 0 dB slope segments (They are always at the bottom.) together and form an approximately straight line as long as each of the two neighborhood impedances have the frequency overlap of their 0 dB slope segments.

To simplify the analysis, VR stage can be modeled as a closed-loop error amplifier (EA) with finite output impedance [12].

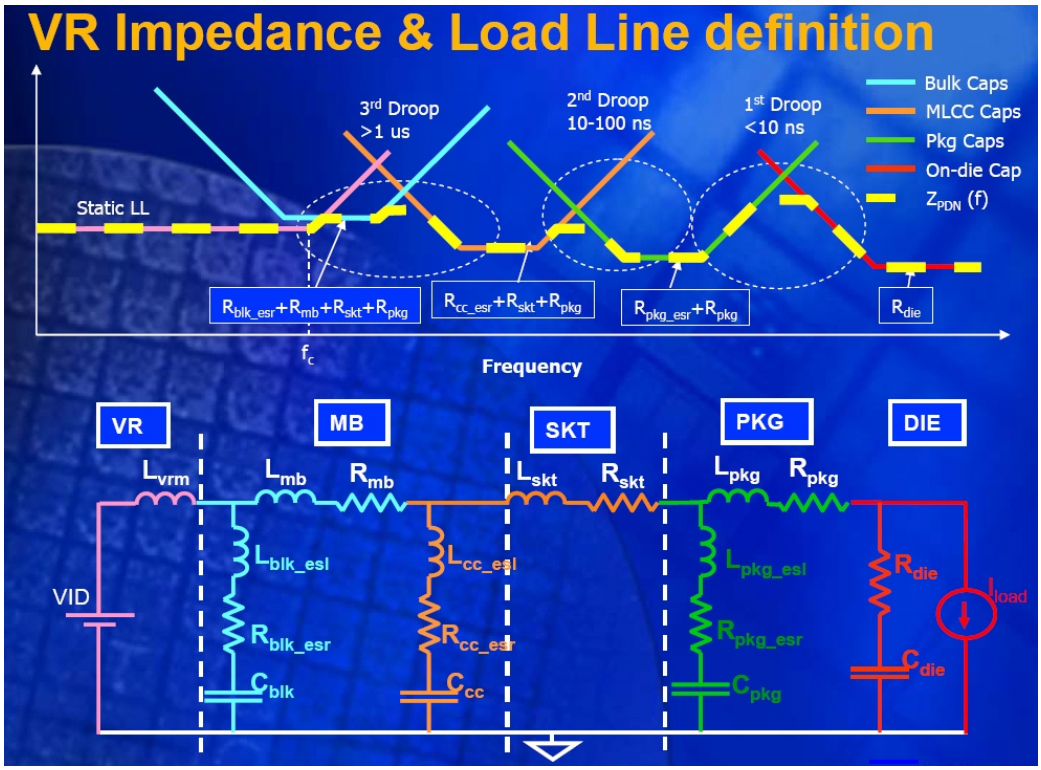

Fig 3.2 VR Impedance and Load Line definition [13]

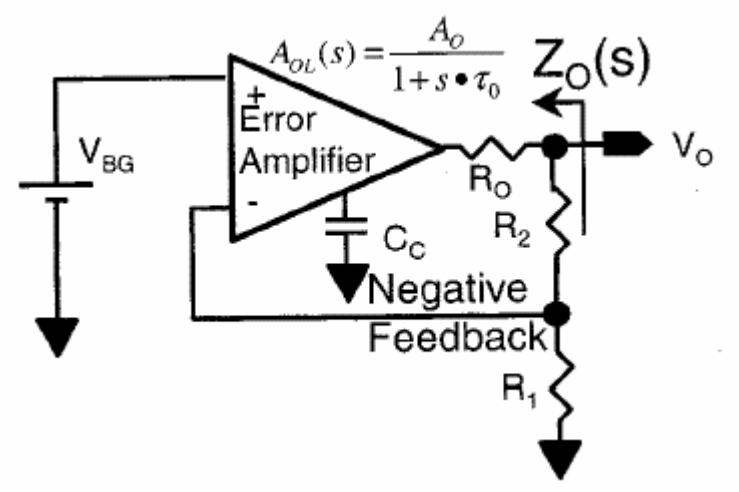

Fig 3.3 Simplified VR model

As shown in Fig 3.3, the EA has a high DC gain in the range of 10^5 - 10^6 and its transfer function can be expressed as:

$$A_{OL}(S) = \frac{A_0}{1 + s \cdot t_0} \tag{3.2}$$

The input and output relation is:

$$V_o = V_{BG} \cdot (1 + \frac{R_2}{R_1}) \tag{3.3}$$

Closed-loop output impedance is given by:

$$Zo(S) = \frac{Ro}{1 + b \cdot A_{OL}(S)} \tag{3.4}$$

Where β = R1/ (R1+R2). (3.5)

Substitute (3.2) into (3.4):

$$Z_O(s) = \frac{R_O}{1 + b \cdot A_{OL}(s)} = \frac{R_O}{1 + b \cdot A_0} \cdot \frac{(1 + s \cdot t_0)}{(1 + s \cdot \frac{t_0}{1 + b \cdot A_0})} \tag{3.6}$$

By assuming $\beta A_0 >> 1$, one can conclude that the closed-loop output impedance has a magnitude of Ro/ (1+ βA_0) which is much smaller than the open loop Ro. And the "zero" happens at $1/\tau_0$ which is the -3 dB frequency of EA.

Since we are going to eliminate the bulk capacitors, naturally TVC impedance needs to have the same impedance profile as what bulk capacitors have. As a result, TVC impedance needs to have the form of:

$$Z_{TVC}(s) = \frac{R_O \cdot (s + Wc)(s + W_{ESR})}{s \cdot W_{ESR}} \tag{3.7}$$

Where Wc is VR's control bandwidth, Ro is the designed VR output impedance and W_{ESR} is the ESR zero frequency of MF decoupling ceramic capacitors.

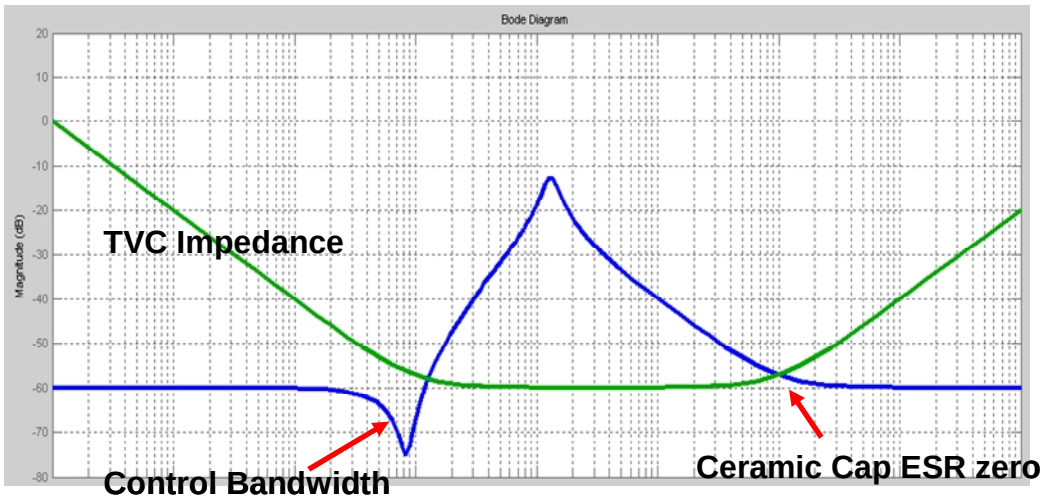

Fig 3.4 TVC Impedance replaces bulk capacitors impedance

In such a way, the overall impedance through the power delivery path can be a horizontal straight line.

3.2 TVC Design Based on output Impedance

Based on above discussion, the TVC circuit structure is developed as shown in Fig 3.5. By feedback VR output voltage to TVC compensator and connecting TVC output stage back to VR output node, TVC is in parallel with main VR. The output stage of TVC is a class AB amplifier which consists of a power BJT pair. Vref, $_{buck}$ equals to the output voltage when there is no load current (VID). Vref, $_{TVC}$ equals to Vref, $_{buck}$ and is connected to the positive input of TVC compensator. During steady state operation, TVC compensator output Vc equals to Vref, $_{TVC}$ due to the feedback resistor R1. In today's VR specification, R_{LL} is usually smaller than 2 mΩ while Io, max is smaller than 100A. From Eq. (3.1) we know that the voltage difference between VID and VO is at most 2 mΩ * 100A = 0.2V. And this voltage cannot forward bias the BJT pair since Vc equals to VID and VO is connected to

emitters of the BJTs. In summary, dead-band exists to make sure during steady state operation TVC will not be active thus no static power loss.

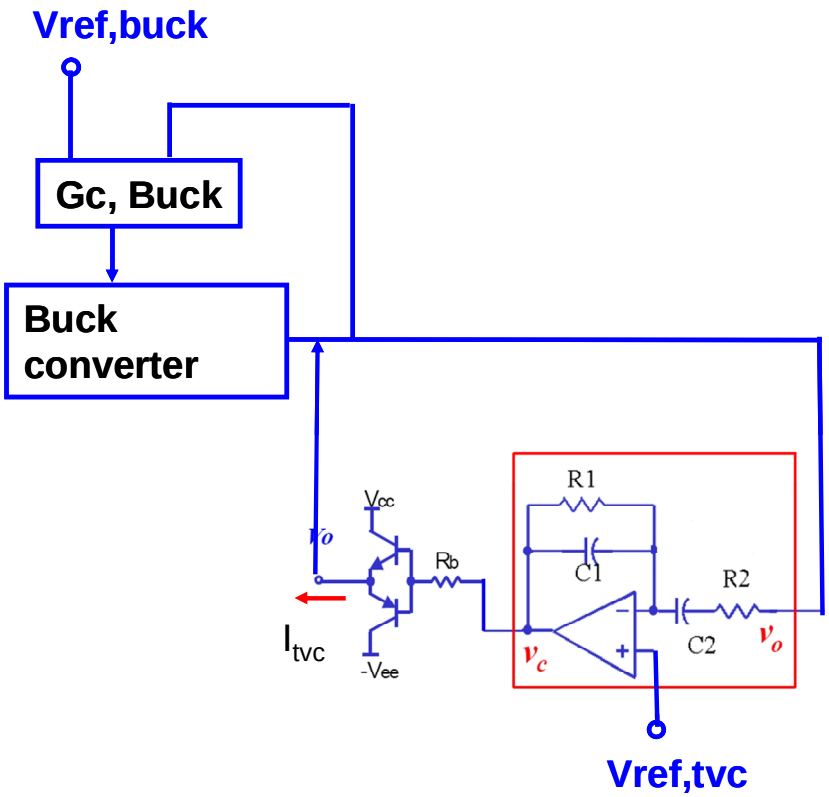

Fig 3.5 TVC structure

TVC output impedance is achieved by its compensator design. From Fig 3.5, the small signal transfer function of Vc / VO can be derived:

$$\frac{v_c}{v_o} = \frac{R_1 C_2 s}{(1+R_1 C_1 s)\cdot(1+R_2 C_2 s)} \tag{3.8}$$

Rewrite Eq. (3.8) as:

$$G_{C,TVC} = \frac{v_c}{v_o} = \frac{s * W_{ESR} * K}{(s+Wc)(s+W_{ESR})} \tag{3.9}$$

Where W_{ESR} is the ESR zero of ceramic caps, Wc is the VR's control bandwidth and K is the adjustable gain to achieve a specified $R_{LL.}$

By choosing R1, C1, R2 and C2, the object $W_{ESR,}$ Wc and K can be achieved:

$$W_c = \frac{1}{R_2 \cdot C_2} \tag{3.10}$$

$$W_{ESR} = \frac{1}{R_1 \cdot C_1} \tag{3.11}$$

$$K = \frac{1}{W_{ESR} \cdot R_2 \cdot C_1} \tag{3.12}$$

The class AB amplifier as TVC power stage is treated as a linear block whose transconductance equals to gm. That means a variation of Vc can result in the injecting or sinking current from the BJTs and the relationship between Vc and Itvc is linear. In the frequency range that we are interested in, this approximation is good enough for the analysis. Finally the transfer function of VO and Itvc becomes:

$$Z_{o,TVC} = \frac{v_o}{i_{TVC}} = \frac{v_o}{g_m * v_c} = \frac{1}{g_m G_{C,TVC}} = \frac{(s+Wc)(s+W_{ESR})}{g_m s * W_{ESR} * K} \tag{3.13}$$

This is the TVC output impedance which can replace the impedance of bulk capacitors.

In this case, 1/ (gm*K) need to be designed equal to R_{LL} to meet the AVP requirement.

3.3 Impact on VR Compensator Design of Removing Bulk Capacitors

As stated in 3.2, TVC only engaged during load transient because dead-band exists. During the steady-state operation, there is no bulk capacitor existing in the VR's power stage. Thus VR's transfer function needs to be re-calculated and the original compensator design is no longer suitable for the modified power stage transfer function.

Fig 3.6 shows the active droop control which implements AVP. The inductor current information is sensed and fed back to adjust the output voltage reference according to the droop requirement. Higher current means lower voltage reference. Then, the feedback control

forces the output voltage to follow the voltage reference. The infinite DC gain of the feedback compensator Av ensures that the values of the output voltage and the voltage reference are equal. Since the output voltage droop is related to the output load current, it can be controlled perfectly.

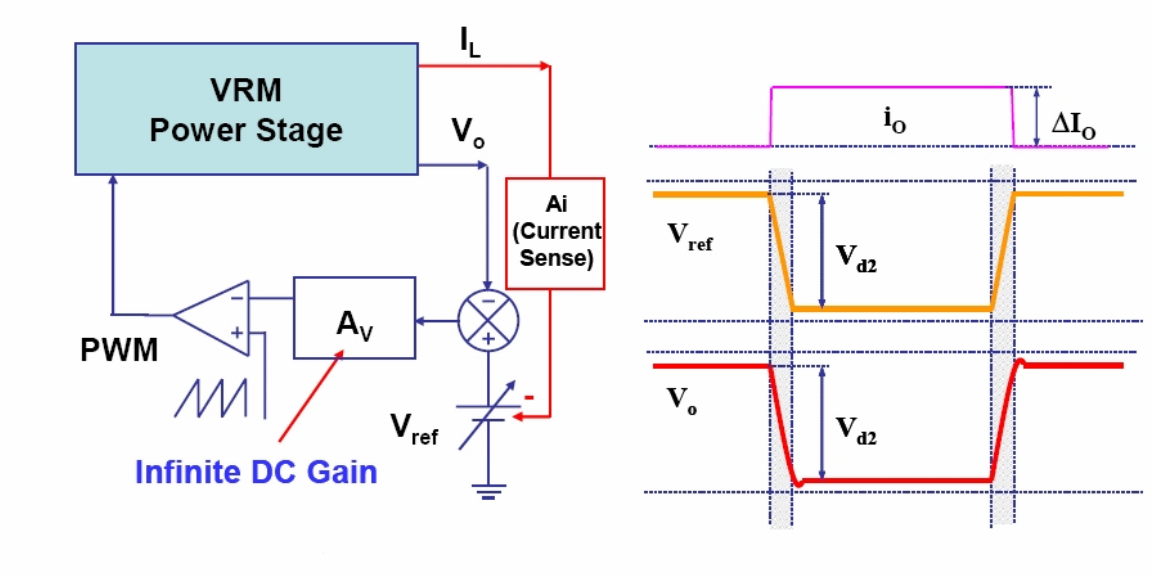

Fig 3.6 Concept of Active Droop Control

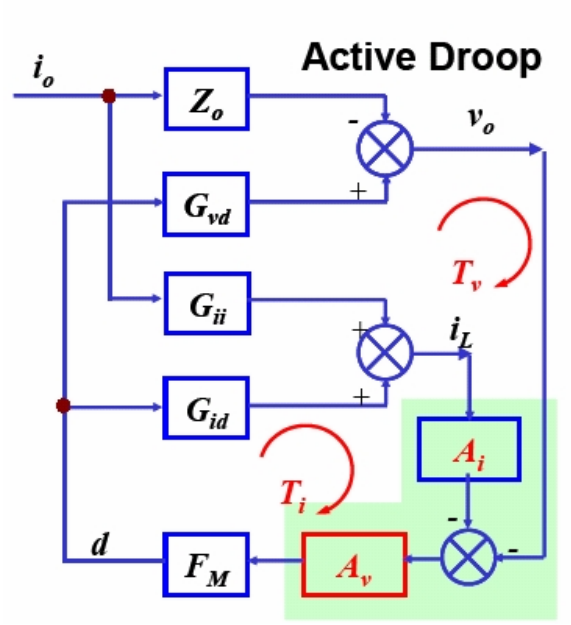

Fig 3.7 Active Droop Control Small Signal Model

The above figure shows Active Droop Small Signal Model and each block's transfer function can be expressed as the following:

$$Z_o(s) = R_L \frac{(1+s/w_{ESR})\cdot(1+s/w_L)}{1+s/(Q\cdot w_0)+s^2/w_0^2} \tag{3.14}$$

$$G_{vd}(s) = V_{in} \frac{1+s/w_{ESR}}{1+s/(Q\cdot w_0)+s^2/w_0^2} \tag{3.15}$$

$$G_{ii}(s) = \frac{1+s/w_{ESR}}{1+s/(Q\cdot w_0)+s^2/w_0^2} \tag{3.16}$$

$$G_{id}(s) = V_{in} \frac{s\cdot C}{1+s/(Q\cdot w_0)+s^2/w_0^2} \tag{3.17}$$

Where:

$$w_{ESR} = \frac{1}{C\cdot ESR_C} \tag{3.18}$$

$$w_L = \frac{L}{R_L} \tag{3.19}$$

$$w_0 = \frac{1}{\sqrt{C \cdot L}} \tag{3.20}$$

$$Q \approx \frac{\sqrt{L/C}}{R_L + ESR_C} \tag{3.21}$$

R_L includes the DC resistance of the inductor L, the conduction resistance Rds-on of top and bottom MOSFETs, and the parasitic resistance of the traces. The ESR_C is the ESR of the output capacitor C. The ω_0 is the power stage double pole.

Current-loop gain is:

$$T_i(s) = F_M \cdot G_{id}(s) \cdot Ai(s) \cdot Av(s) \cdot He(s) \tag{3.18}$$

where $H_e(s)$ models the current-sampling effect in current-mode control:

$$H_e(s) = 1 - \frac{s}{2\,fs} + \frac{s^2}{(p \cdot fs)^2} \tag{3.19}$$

And voltage-loop gain is:

$$T_v(s) = F_M \cdot G_{vd}(s) \cdot Av(s) \tag{3.20}$$

A high-bandwidth current-loop design can simplify the buck converter from a second-order system to a first-order system. When the current loop is closed and the voltage loop is open, the buck converter operates as an ideal current source, and its output impedance can be approximately represented as:

$$Z_{oi}(s) = \frac{1}{s \cdot C} + ESR_C = \frac{1 + s/w_{ESR}}{s \cdot C} \tag{3.21}$$

Consequently, the close-loop output impedance is:

$$Z_{oc}(s) = \frac{Z_{oi}(s)}{1 + T_2(s)} = \frac{(1 + Ti(s)) \cdot Zoi(s)}{1 + Ti(s) + Fm \cdot Gvd(s) \cdot Av(s)} \tag{3.22}$$

where $T_2(s)$ is the outer-loop gain which determines the system bandwidth and phase margin.

$$T_2(s) = \frac{Tv(s)}{1+Ti(s)} \tag{3.23}$$

In order to have constant output impedance Zoc, T_2 should have the form of:

$$T_2(s) = \frac{1}{R_{LL} \cdot C_o} = \frac{W_c}{s} \tag{3.24}$$

The voltage loop compensator has a transfer function of:

$$A_v(s) = K \cdot \frac{1+s/w_0}{s \cdot (1+s/w_p)} \tag{3.25}$$

where K is designed to have a high bandwidth current loop gain. All three loops (Ti, Tv and T2) have almost the same control bandwidths at the capacitor ESR zero. Fig. 3.8 also shows the closed-loop output impedance with this compensator design. It is almost constant.

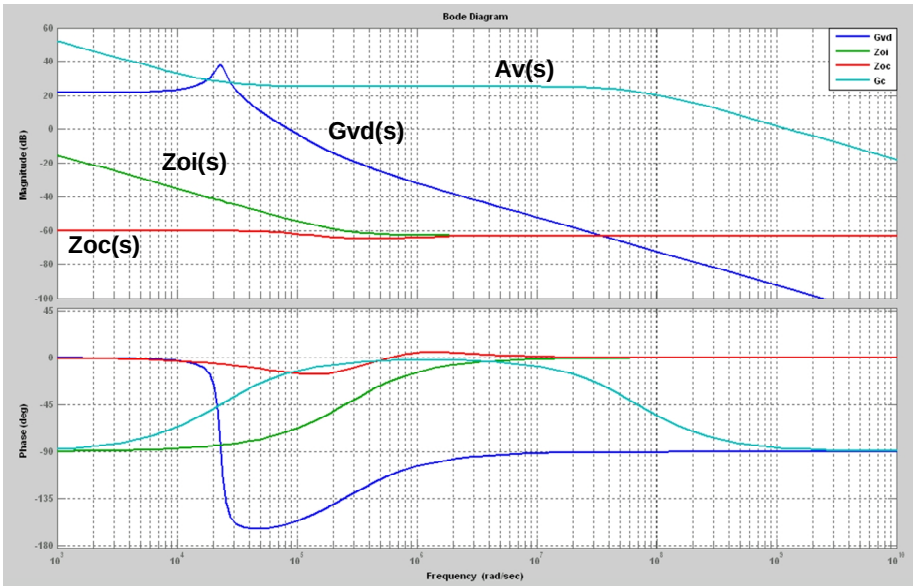

Fig 3.8 Constant Output Impedance design

However this is only the case to design a VR with bulk capacitors. If all the bulk capacitors are removed and only decoupling capacitors (MLCC) remain, the buck converter's

power stage changes. From Eq. (3.18), (3.20) and (3.21) we know that ω_{ESR} , ω_0 and Q increases due to reduced C value. Accordingly the Gvd(s) Bode plot shape changes. For example, ω_{ESR} of MLCC is in MHz range which is even higher than VR's switching frequency. Assume the control bandwidth is 1/6 of switching frequency, maximum ω_c is 2π*50 kHz. Since ω_{ESR} is much larger than ω_c, it cannot help much to increase the phase margin. Also when C is reduced to 1/10 ω_0 increases 10 times and is very close to switching frequency, the compensator gain needs to be largely reduced to keep the same control bandwidth and sufficient phase margin. Since in active droop control, current loop and voltage loop are coupled and share the same compensator, the current loop gain becomes much less and make the whole control more like a purely voltage mode control. All these reasons lead to the 3-pole 2-zero voltage mode compensator. Still the control bandwidth is kept at around 1/6 switching frequency. A typical 2-channel interleaving buck converter was simulated by Saber Sketch circuit simulation toolkit. The specifications are: Vin = 12V, Vout = 1.5V, Iout,max = 40A,Rdroop = 1mΩ. To meet such requirements, choose fsw = 330 kHz, inductance per channel = 680 nH, output capacitors are 10 pieces of 560uF Oscon capacitor in parallel with 20 pieces 22uF MLCC. The related load transient is shown in Fig. 3.9. By following the constant output impedance design guide line, one can get perfect AVP performance.

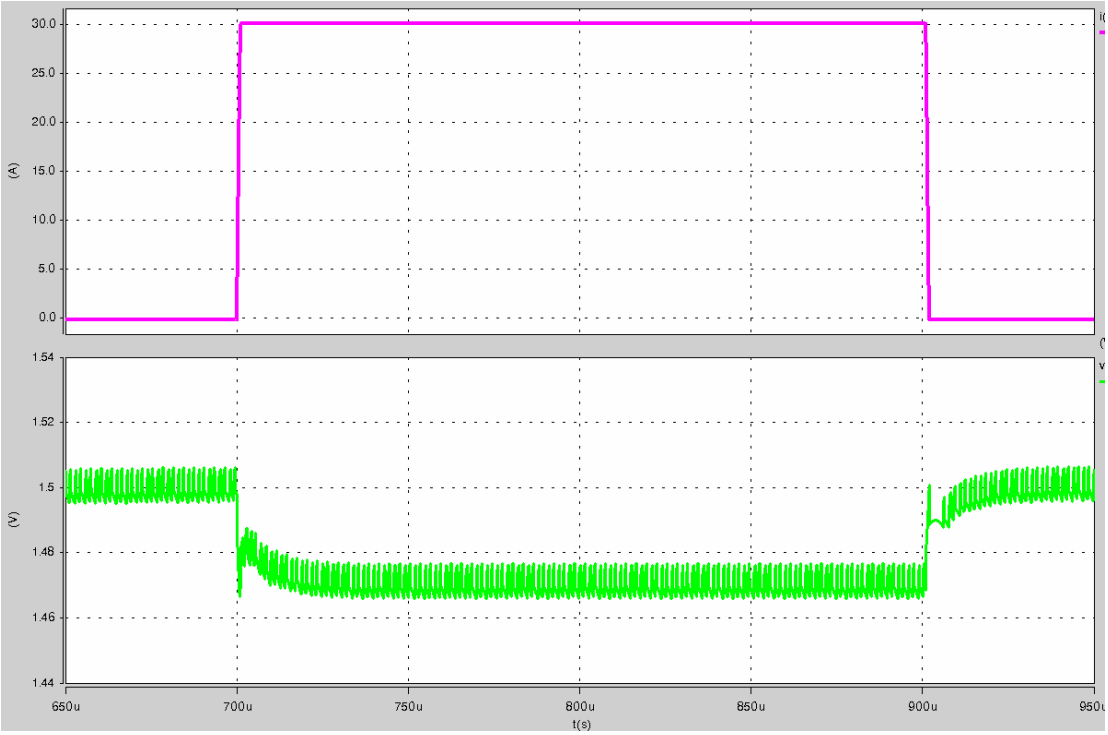

Fig 3.9 Simulated Load transient response using Oscon as output capacitors

However if all the Oscon capacitors are removed, the compensator need to be re-designed to keep VR stable. The following MATLAB script was used to choose the compensator Rs and Cs value according to above mentioned equations.

```
s= tf('s');
C0 = 0.5e-3;            % unit capacitance = 100uF
R0 = 0.2e-3;            % unit cap ESR = 1mOhms
Rdroop = 1e-3;          % Active droop = 1mOhms
n = round(R0/Rdroop);   % # of caps in parallel
C = n*C0;               % Output Capacitance
rC = R0/n;              % Total Cap ESR
Vg = 12;            % Input Voltage
Vo = 1.5;           % Output voltage
D = Vo/Vg;          % Duty Cycle
rL = 0.0005;        % Inductor DCR
```

```
Io = 30;              % Max Output current
delta_vo = 5e-3;
ts = 1.5e-6;
 fs = 1/ts;               % Switching frequency 330kHz
 Ws = 2*pi*fs;
 Wc = Ws/6;            % fc in Rad/S
 Wci = Wc;
delta_iL1 = C*8*fs*delta_vo;        % current ripple by C
delta_iL = delta_vo/rC;         % current ripple by ESR
L = 340e-9;
Q = sqrt(L/C)/(rL+rC);  % Power stage Q factor
W0 = 1/(sqrt(C*L)); % Resonant frequency
fc = Wc/pi/2;             % Desired control bandwidth in Hz
P1 = -1/(C*rC);     % pole to cancel ESR zero
P2 = -10*Wc;     % High frequency pole
K = 0.06*Wc/Vg/(1+Wci/W0)*(1+Wci/W0/Q+(Wci/W0)^2);          % Compensator gain
cc1 = 1e-9;      % compensator cap
rc1 = 1/(K*cc1);
cc2 = 1/(0.95*rc1*W0);
rc3 = 1/(P1*cc2);
rc2 = 1/(W0*cc1);
cc3 = 1/(rc2*P2);
Zo1 = tf([rC*L*C rC*rL*C+L rL],[L*C (rC+rL)*C 1]);  % open loop Zo
Gdv = tf([rC*C*Vg Vg],[L*C (rC+rL)*C 1]);          % duty to vo
Gii = tf([rC*C 1],[L*C (rL+rC)*C 1]);              % io to iL
Gdi = tf([C*Vg 0],[L*C (rC+rL)*C 1]);              % duty to iL
Gc = zpk([-W0 -W0*0.95],[0 P1 P2],K*P1*P2/W0^2);                  % Compensator Av
He = 1-s/(2*fs)+s^2/(pi*fs)^2;
Ti = Gc*Gdi*Rdroop*He;                            %current loop gain
Tv =Gc*Gdv;                                % Voltage loop gain
T2 = Tv/(1+Ti);                            % practical T2
```

```
Zoi = Zo1+Ti/(1+Ti)*Gdv*Gii/Gdi;          % Z with current loop closed
Zoc = Zoi / (1+T2);                       % close loop Zoc
```

The new total loop gain T2 and close-loop output impedance are shown in Fig 3.10 and Fig 3.11 respectively.

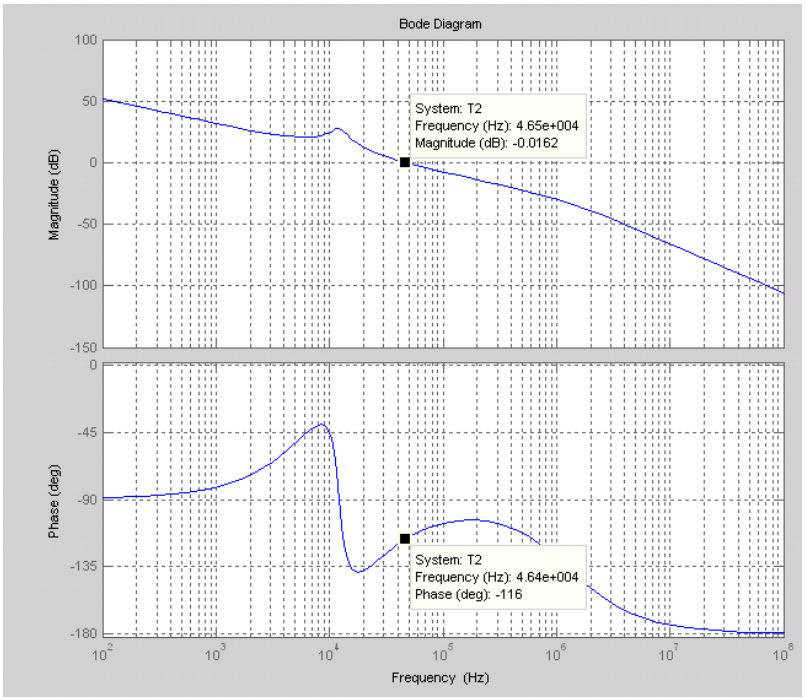

Fig 3.10 Total loop gain T2 with re-designed compensator after removing bulk caps

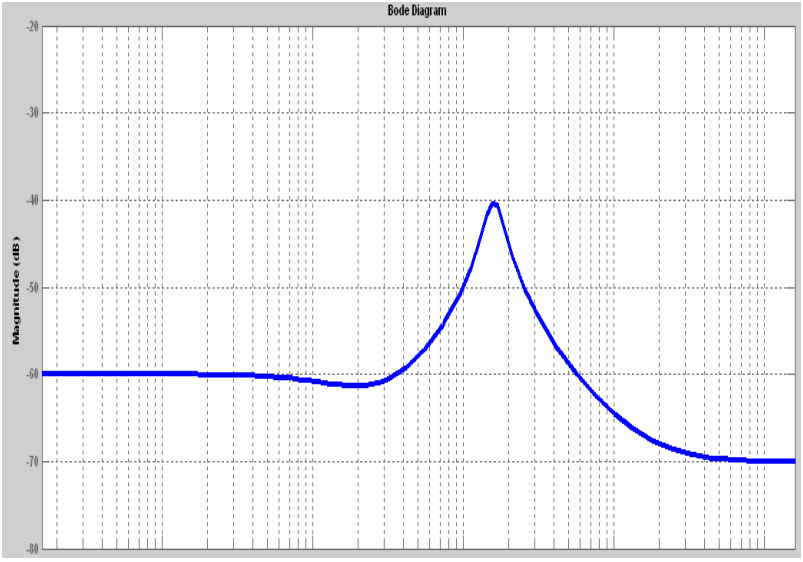

Fig 3.11 Close-loop output impedance after removing bulk caps

3.4 Parallel Impedance Concept

So far we discussed the relationship between output impedance and load transient response. However, impedances also are related to dynamic currents distribution in each parallel branch. In traditional solution, bulk capacitors store the energy from inductor and release it to load during transient thus no energy is lost ideally. On the contrary, linear regulator type TVC can only dissipate that energy. This results in extra power loss in the TVC circuits. As the load transient frequency goes higher and higher, ultimately the power loss will exceed the thermal limit of TVC packaging which is not acceptable. To simplify the analysis, a passive RLC circuit is introduced to model the parallel branches of VR, TVC and output capacitors.

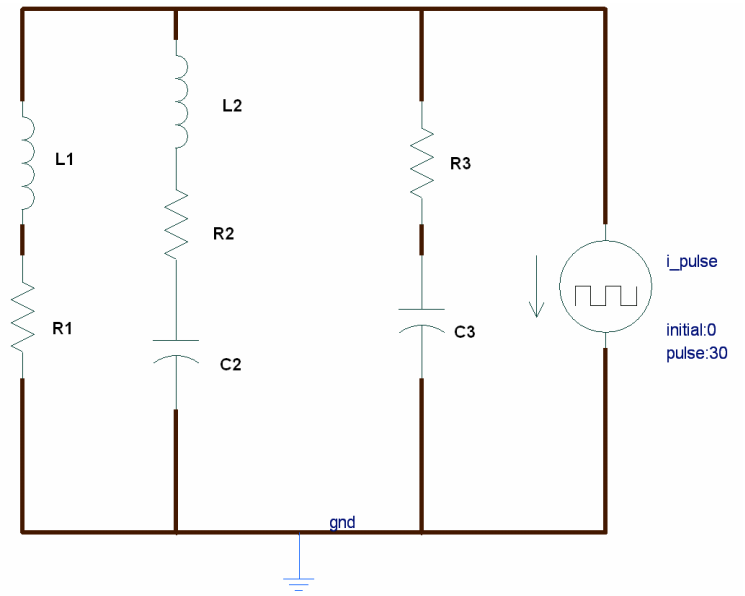

Fig 3.12 AC equivalent impedance of VR, TVC and output caps

From output impedance Bode plot, VR and TVC can be modeled as three branches in parallel. In Fig 3.12, from left to right are the close-loop output impedance given by control

bandwidth, TVC output impedance and output decoupling capacitors (MLCC) impedance respectively.

$$Z_{VR} = R_1 + L_1 \cdot s \tag{3.26}$$

$$Z_{TVC} = R_2 + L_2 \cdot s + \frac{1}{s \cdot C_2} \tag{3.27}$$

$$Z_c = R_3 + \frac{1}{s \cdot C_3} \tag{3.28}$$

Where:

$$R_1 = R_2 = R_3 = R_{droop} \tag{3.29}$$

$$w_c = \frac{R_1}{L_1} = \frac{1}{R_2 \cdot C_2} \tag{3.30}$$

$$w_{ESR} = \frac{1}{R_3 \cdot C_3} = \frac{R_2}{L_2} \tag{3.31}$$

The load transient is modeled as a current source. By giving the current source a step change, all three branch currents can be plotted out. Fig 3.13 shows the results.

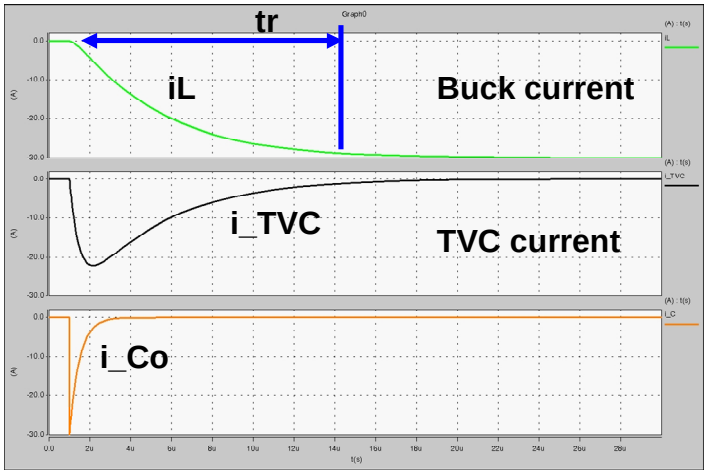

Fig 3.13 Step response of each branch currents

It seems that the decoupling capacitors only take the sharp edge of load current. Since we only focus the current distribution between VR and TVC, the output capacitor branch can be omitted. So Fig 3.12 can be further simplified to Fig 3.14.

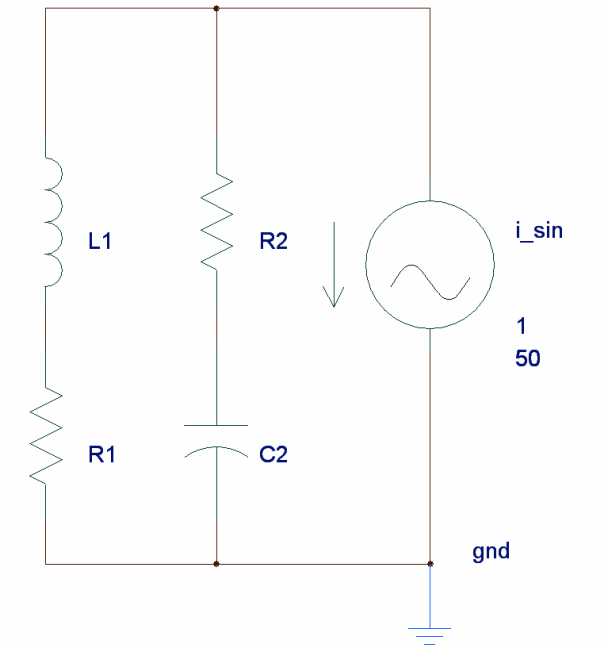

Fig 3.14 Simplified AC equivalent impedance of VR and TVC

Solve for the step response in time domain, one can get that:

$$iL(t) = 1 - e^{\frac{-R_1}{L1}t} \tag{3.32}$$

The inductor current rising time can be approximated as:

$$tr = \frac{2.2}{w_c} \tag{3.33}$$

And the inductor current slew rate is:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{\Delta Io * w_c}{2.2} \tag{3.34}$$

From Eq. (3.34) we can see that inductor current slew rate is determined by VR's control bandwidth. This is the case when the first zero of TVC impedance is equal to VR's control bandwidth. What if there is a "gap" ($\omega_{TVC} > \omega_c$) or "overlap" ($\omega_{TVC} < \omega_c$) between the two impedance curve? Further simulation shows that the "gap" will result in the output voltage overshoot (Same as after removing the bulk capacitors.) and the "overlap" makes the inductor current slew at a lower rate which simply means more power loss in the TVC branch.

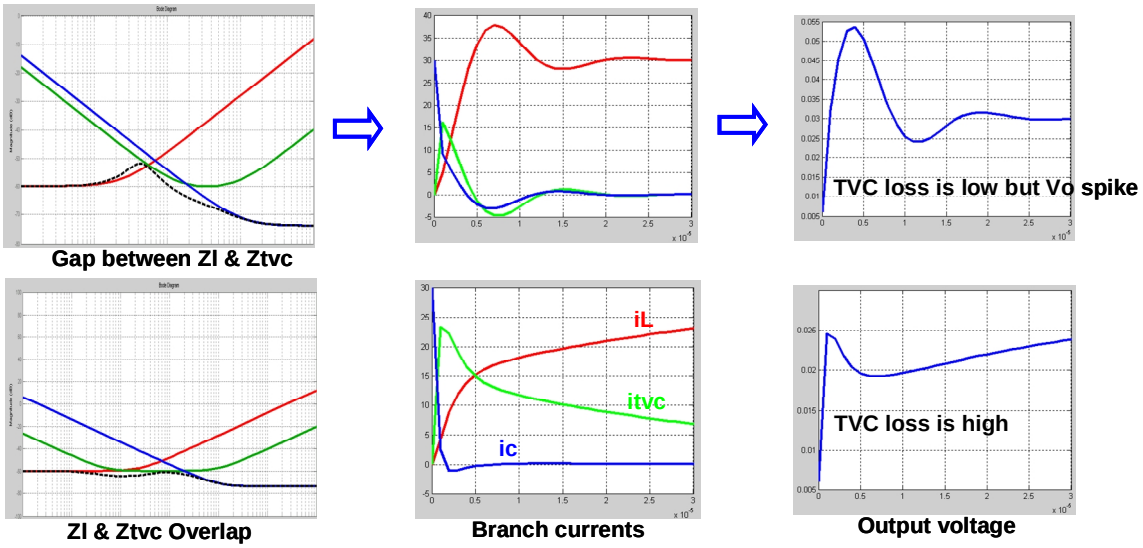

Fig 3.15 Branch current distribution and output voltage according to output impedance

Now the conclusion can be drawn that even with the optimized output impedance design, VR's inductor current slew rate is determined by control bandwidth which is finally limited by VR's switching frequency and compensator design. According to Eq. (3.33), if ω_c = 40 kHz·(2π) = $2.5 \cdot 10^5$ (Rad/s), tr=9(us). Assume a load step change from 30A to 0A and output voltage is 1.5V, the energy dissipated in TVC will be ½*ΔI*VO*tr = 200uJ. If the load transient has a frequency of 100 kHz, then the power loss caused by TVC is 20W which is even higher than the total power loss in the VR.

3.5 Proposed Non-linear Approach to Minimize Transient Power Loss

By simply following the constant output impedance design methodology, TVC circuit still suffers from high power loss introduced by high frequency load transient. The transient current distribution is set by the relationship between those parallel impedances. However a novel non-linear control method is proposed in order to fully utilize the VR's inductor slew rate capability. The block diagram is shown in Fig. 3.16.

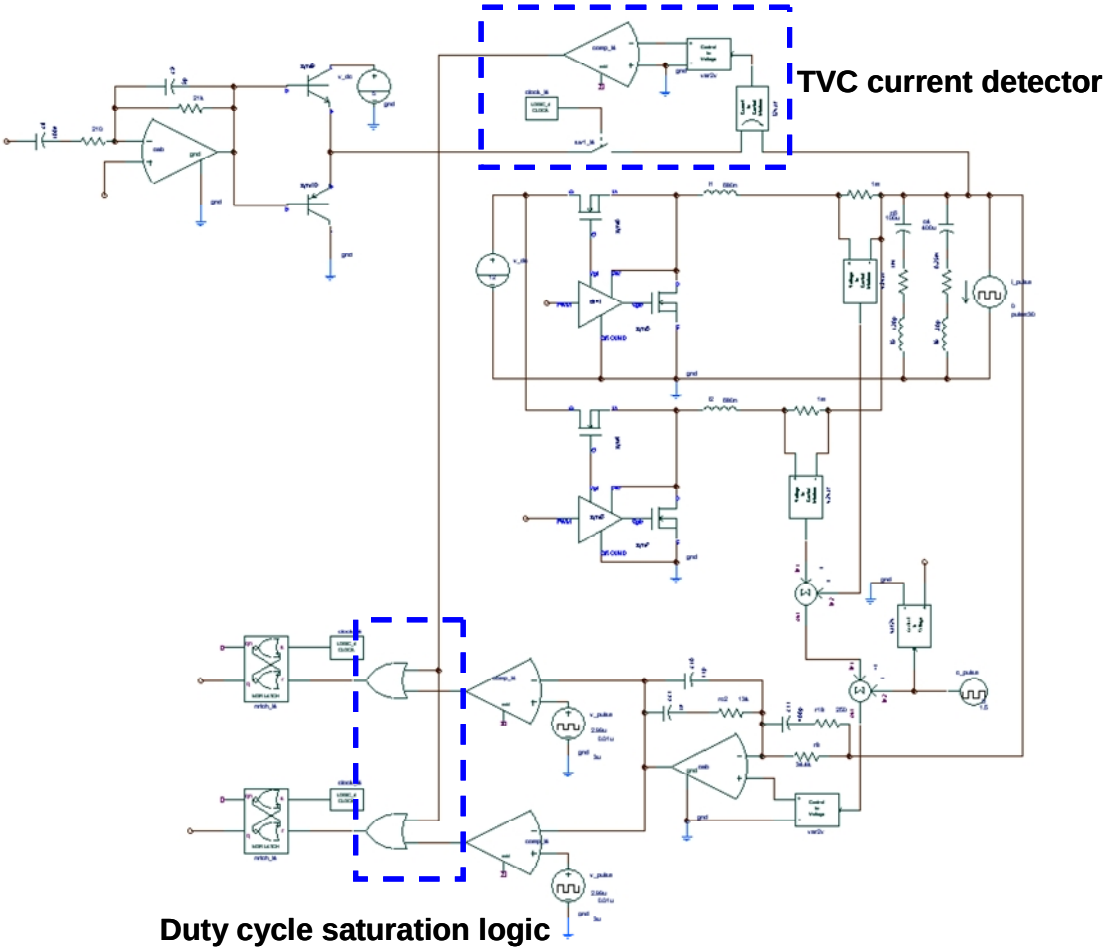

Fig 3.16 Non-linear TVC circuit diagram

The basic operation is described as following: during load transient, output voltage should have spike. This variation is sensed and amplified by the TVC compensator.

According to the TVC compensator design, only high frequency components of the signal can pass and get amplified. That is how the output impedance in different frequency range is covered by VR and TVC. A TVC current detector senses the currents going through TVC and generates a logic signal. This signal overrides the VR's PWM output signal and forces the inductor slewing at the highest rate it can achieve. This is called duty cycle saturation logic because it seems that the PWM duty is saturated (constant "0" or "1") during load transient. By such a way, TVC and VR's work are separated or "decoupled" during load transient.

However the introduction of non-linear control gives the problem that how to design the non-linear part such that a smooth transition is guaranteed. For the TVC current detector, a hysteresis window is required to make the comparator immune to unwanted sensing noise. Since the rising and falling edge of TVC current is considerably deep, a relatively large window is acceptable because even the large window will not give extra delay but help with immunity to noise. Since VR's duty cycle is saturated, if we consider VR as a black box, it has a new effective control bandwidth. This control bandwidth is defined only by the inductor current slew rate. The approximation is based on the 2nd order system step response because as compared with 1st order system, it has more constant slope.

$$fc' = \frac{di_L / dt}{4 * \Delta Io} \tag{3.35}$$

The TVC compensator needs to be re-designed according to the effective VR control bandwidth fc'. This is to make sure there is no impedance overlap between VR and TVC. Fig 3.17 shows how the effective control bandwidth changes with the duty cycle saturation logic. With the above design guide line, the same 2-channel buck converter after removing all bulk capacitors and adding non-linear TVC was simulated. Good performances were achieved in

terms of load transient response and TVC power loss. The waveforms are shown in Fig 3.18. We can see that during load step up and step down, duty cycle is saturated and highest inductor slew rate is achieved.

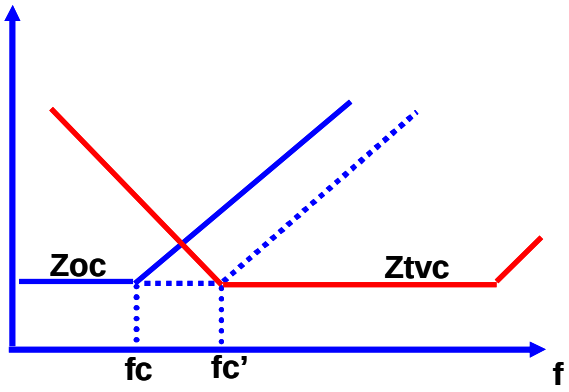

Fig 3.17 Ztvc design according to VR effective control bandwidth

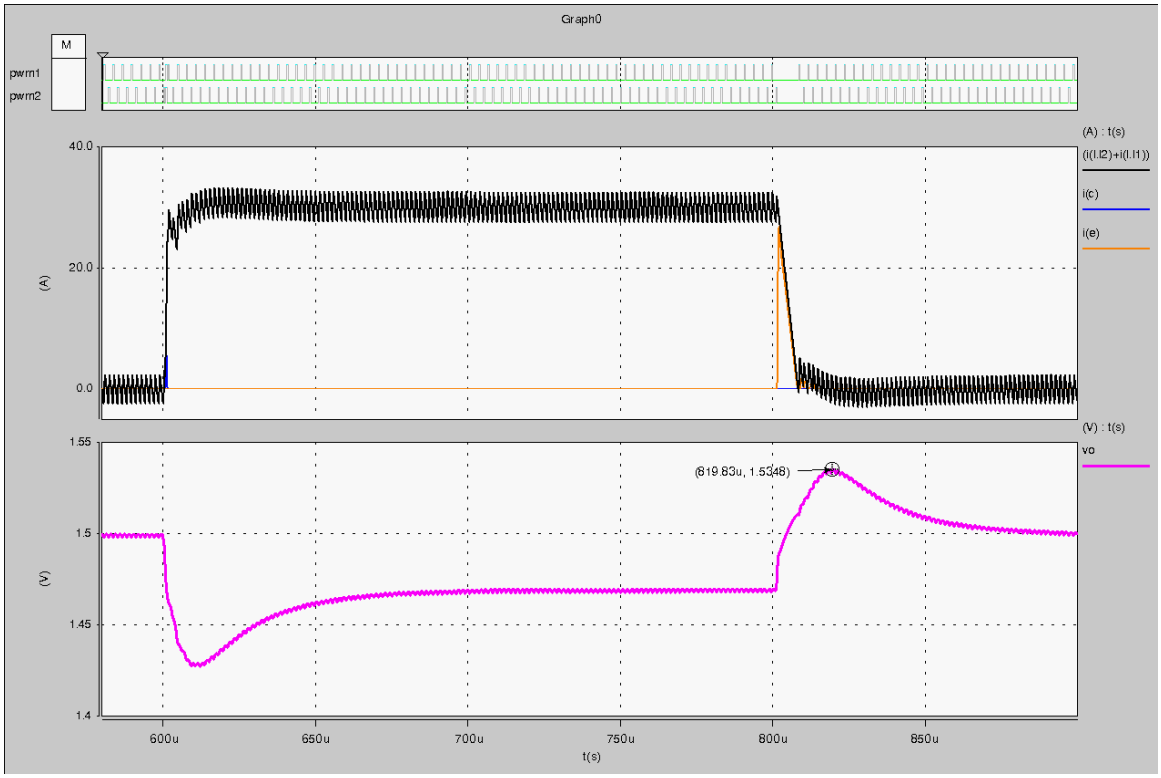

Fig 3.18 Load transient of VR combining non-linear TVC

3.6 Discussion of Load Transient Duty, Frequency and Total Efficiency

The efficiency of DC/DC converter is defined as total output power divided by total input power under the specified working conditions. The widely used efficiency curve is like this: Under steady-state operations, X axis is the static output current and Y axis is the total efficiency. However this curve does not consider the load changing conditions. Since a lot of DC/DC converter's load is always changing, like microprocessor, this efficiency definition is no longer a good criterion for evaluating the performance of DC/DC converter. For example, if the converter is always working under light load condition, it is better to minimize the light load power loss other than to optimize the efficiency under full load condition. In fact, very few converters always work under full load condition.

An extended total efficiency is thus defined as the total output energy divided by total input energy of a converter over a given period of time. To simplify the analysis, assume the load changes from zero to full load with a fixed duty d and fixed period T as shown in Fig 3.19.

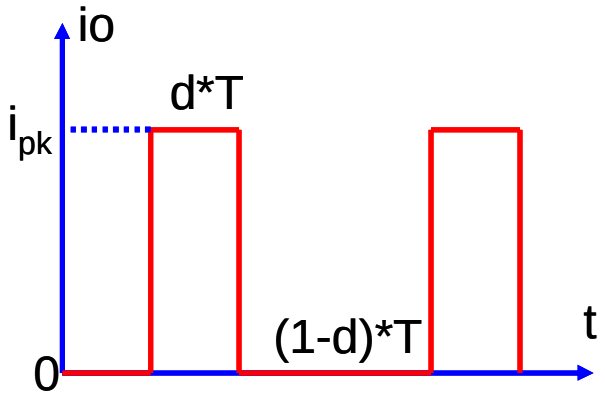

Fig 3.19 Simplified load changing scheme

Fig 3.20 shows a typical curve of converter power loss changing with output current. Because of driver loss, even if output current is zero, there is $P_{loss,min}$ which has a value around 0.5W.

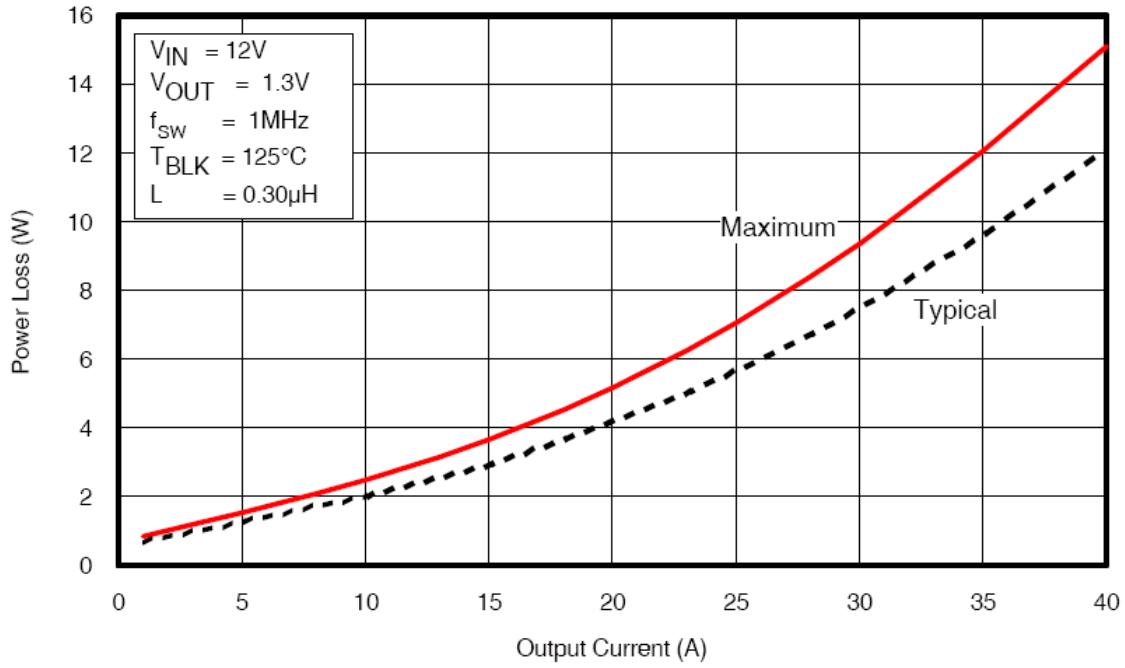

Fig 3.20 IRF iP2003A power loss vs. output current

(From IRF iP2003A datasheet)

The total efficiency is now given by:

$$h = \frac{\int_0^T P_o(t)\cdot dt}{\int_0^T [P_o(t)+P_{loss}(t)]\cdot dt} = \frac{\Sigma(P_o\cdot \Delta t)}{\Sigma[(P_o+P_{loss})\cdot \Delta t]} \tag{3.36}$$

$$= \frac{P_{o,\max}\cdot d\cdot T}{(P_{o,\max}+P_{loss,\max})\cdot d\cdot T+(1-d)\cdot T\cdot P_{loss,\min}}$$

$$= \frac{h_0\cdot D}{D+\frac{P_{loss,\min}}{P_{in,\max}}\cdot(1-D)}$$

$$= \frac{h_0}{1+\frac{1-D}{D}\cdot\frac{P_{loss,\min}}{P_{in,\max}}} \tag{3.37}$$

Where $P_{loss,min}$ is the power loss under no load condition, $P_{loss,max}$ is the power loss at full load, $P_{in,max}$ is the input power at full load, $P_{o,max}$ is the output power at full load and h_0 is the full load efficiency. From Eq. (3.37) and Fig 3.20, one can draw the curve of total efficiency changing with load duty. Noted that there is no frequency term in Eq. (3.37), which means total efficiency is not related to load transient efficiency. However since TVC loss is proportional to load transient frequency, if TVC replaces bulk capacitors then Eq. (3.37) will be re-written as:

$$h = \frac{h_0}{1 + \frac{1-D}{D} \cdot \frac{P_{loss,\min}}{P_{in,\max}} + E_{TVC} \cdot f} \tag{3.38}$$

Where E_{TVC} is the energy absorbed by TVC during each load transient and f is the load transient frequency.

By plugging in the data acquired in Fig 3.20 and E_{TVC} into Eq. (3.38), a 3-D curve can be generated as shown in Fig. 3.21. It seems that if load transient frequency is lower than 10 kHz, the total efficiency almost keeps constant which means at low transient frequency the power loss added by TVC is negligible as compared with the other losses. Fig 3.22 gives us a clearer picture how the TVC power loss affects total efficiency. We should also be noticed that if load transient frequency keeps increasing, finally the TVC solution is unacceptable because of the extremely high added power loss.

However this statement is quite questionable. Recalling from the equivalent impedance concept, the dynamic currents distribution during load transient between different impedance branches are different. The higher the impedance, the smaller the current will be. According to Intel proposed VR output impedance (See Fig 3.2), a simplified AC impedance circuit was constructed in Saber.

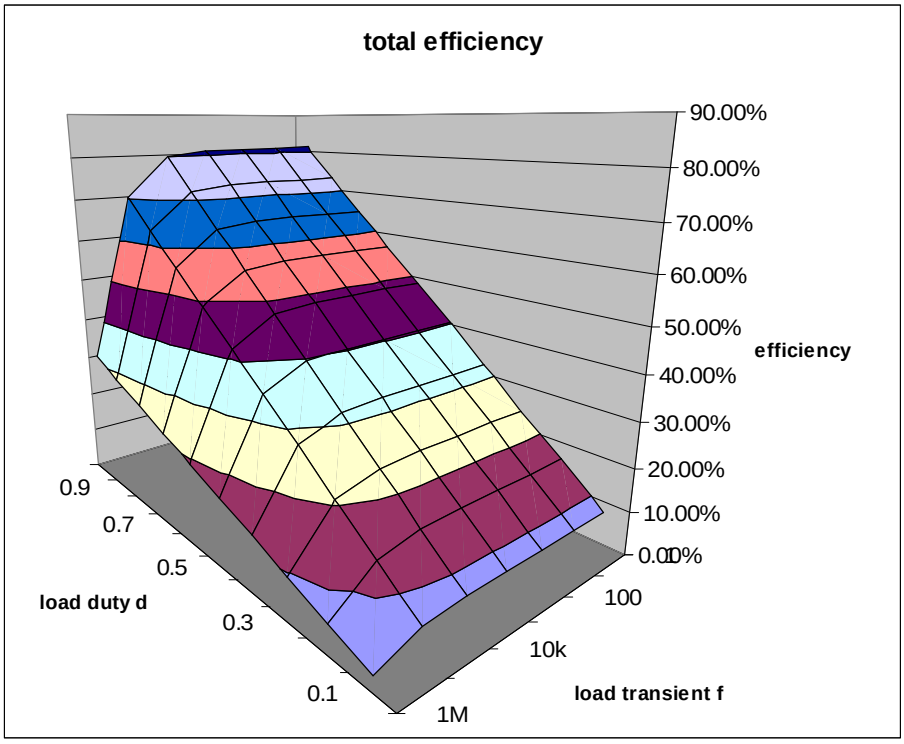

Fig 3.21 Total efficiency vs. load transient duty and frequency

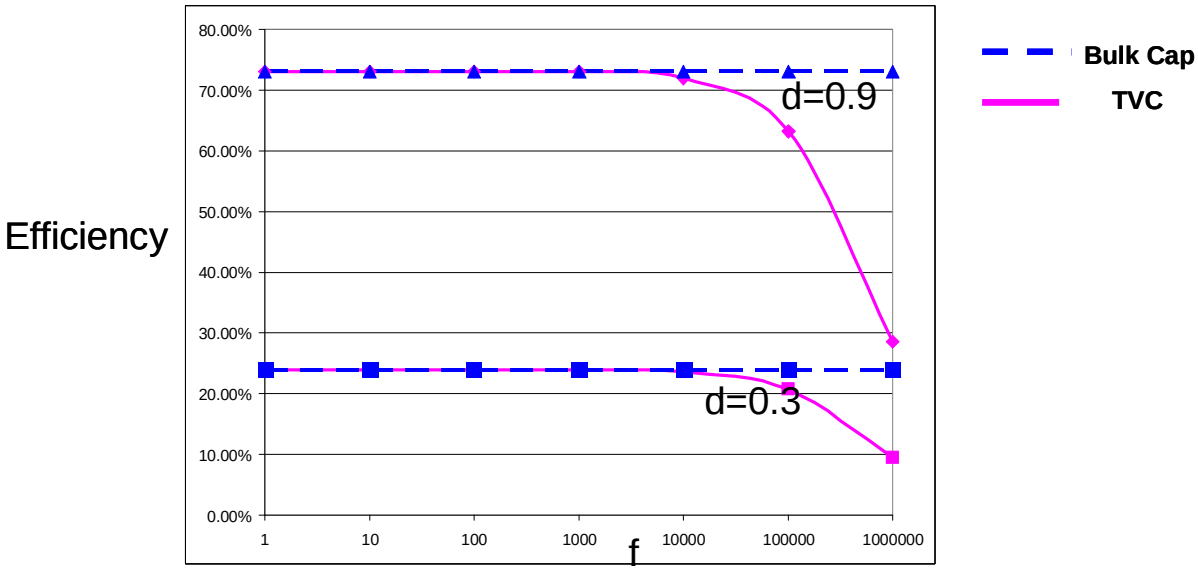

Fig 3.22 Efficiency comparison between bulk cap and TVC solution

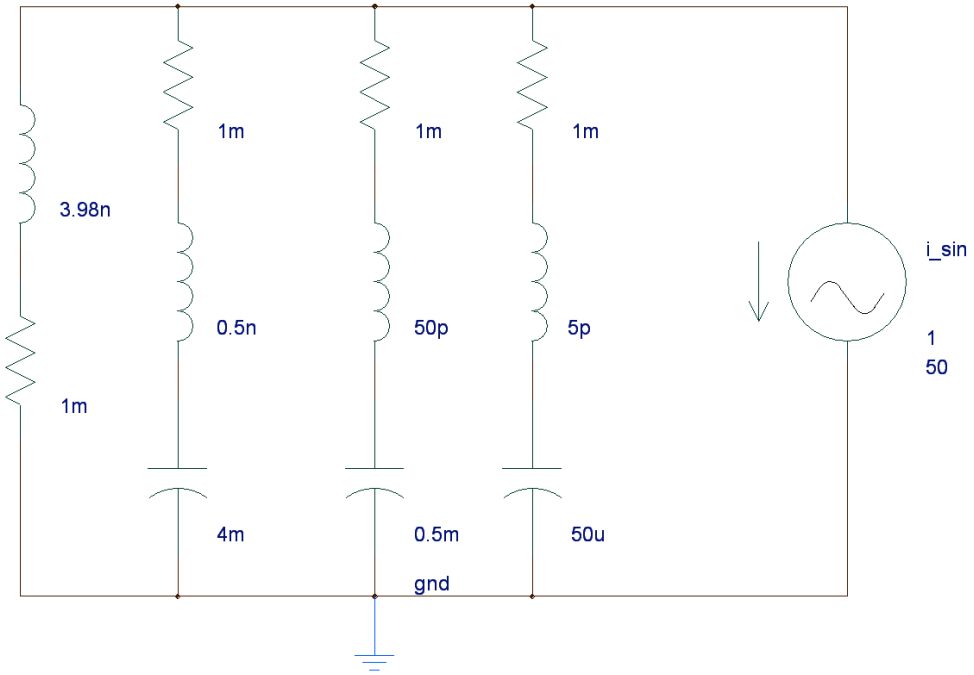

Fig 3.23 Simplified AC equivalent circuit of CPU power delivery path

Fig 3.23 shows how the simplified microprocessor's power delivery path looks like. The branches from left to right stand for VR, bulk capacitors, decoupling capacitors (MLCC) and cavity capacitors respectively. By doing a small signal analysis, one can get the frequency response of each branch's current as shown in Fig 3.24. This graph clearly shows that even if the load transient frequency is as high as several MHz, owing to the impedance relationship, the bulk capacitors or TVC branch only takes very low current. As the slope of current's frequency response is -20 dB per decade, the current magnitude is reversely proportional to excitation frequency. Therefore, the second "pole" of TVC current frequency response curve, which is also the second "zero" of TVC impedance, will determine the product of current excitation magnitude and frequency.

To further verify the above thinking, similar analysis approach is carried out as when we study the current distribution between VR inductor and TVC during load step change. Fig 3.25 is same as Fig 3.14 but has different meaning. L1 and R1 stands for TVC's equivalent

bandwidth which is the second impedance “zero” and R2, C2 is now the equivalent branch of decoupling capacitors. Following the same rule, we know that the slope of TVC current rising edge is determined by its “bandwidth”. Imagine that the load excitation is a square wave with an extremely high frequency, since TVC current cannot follow, it will have a much smaller magnitude. Fig 3.26 is the simulation results.

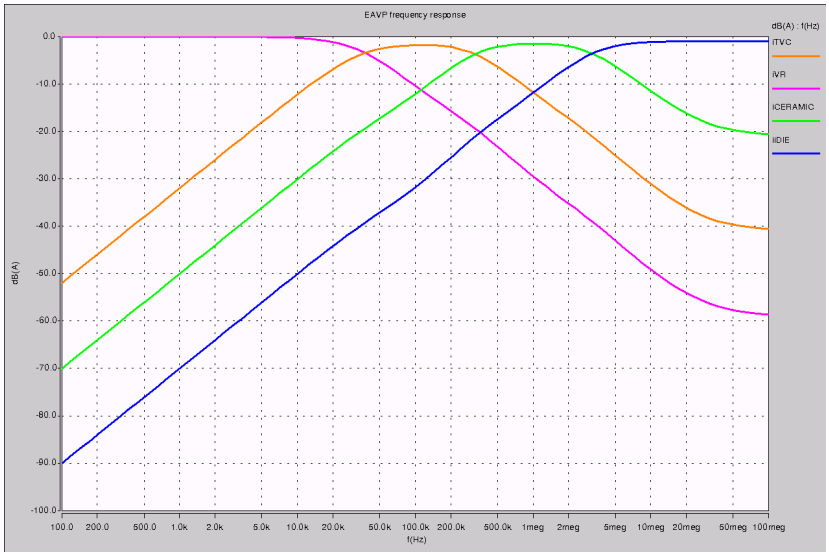

Fig 3.24 Frequency response of branch currents in CPU power delivery path

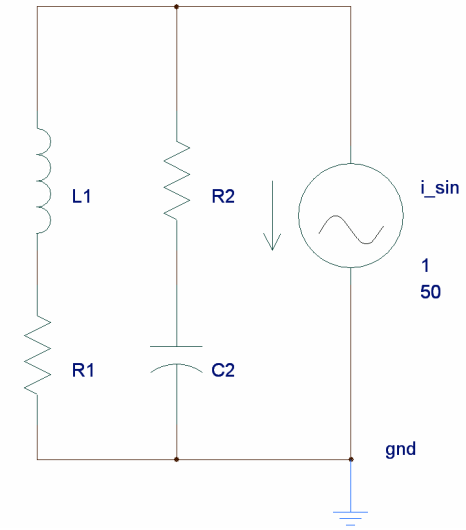

Fig 3.25 Simplified AC equivalent impedance of TVC and decoupling caps

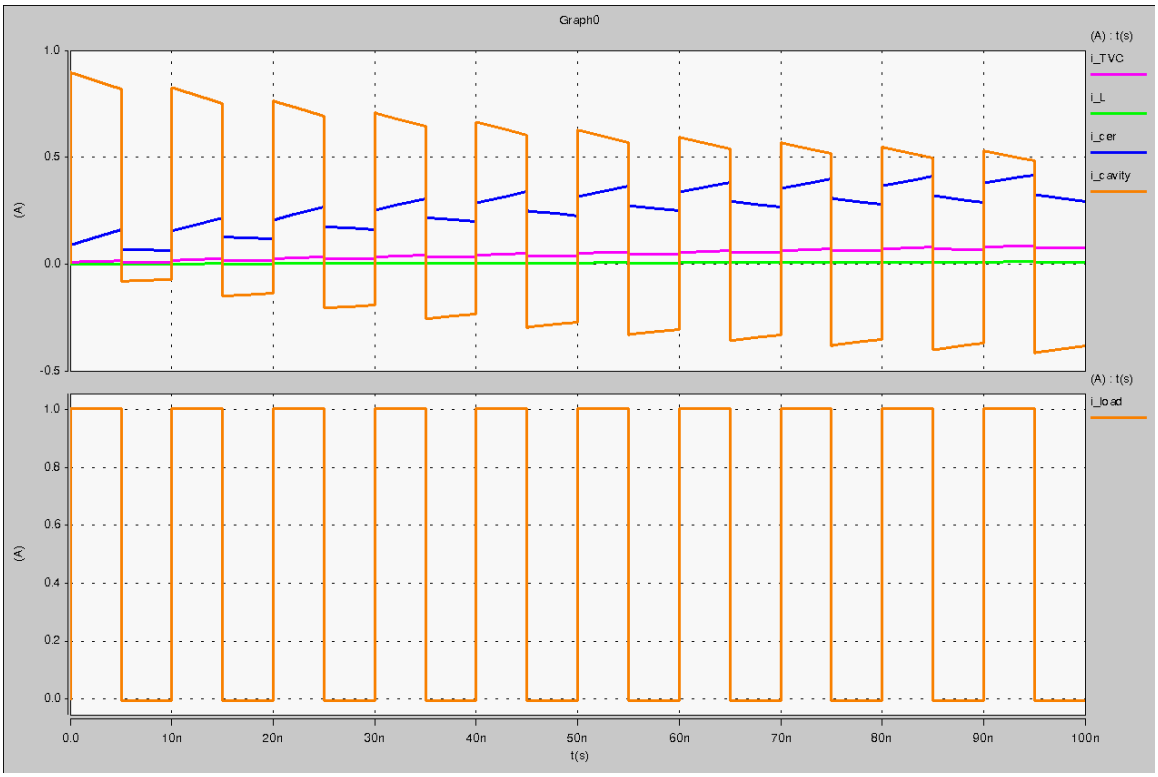

Fig 3.26 Simulated high-frequency load current and branch currents

Fig 3.24 gave us the idea how to reduce load-transient related TVC loss: if TVC impedance second “zero” can be moved to lower frequency, the loss will be reduced. In order to keep the same constant output impedance, other types of capacitors with lower ESR zero frequency than ceramic capacitors can be inserted. For example, tantalum capacitors have an ESR zero which is between the Oscon capacitors and ceramic capacitors. This will help to reduce TVC power loss and make TVC design achievable.

CHAPTER 4 Experimental Verifications

4. 1 Benchmark Design Using Traditional Bulk Capacitors

To verify the TVC design concept and evaluate its performance in terms of load transient response and power loss, hardware based evaluation boards were built. Base on the same PCB layout, two solutions between traditional bulk capacitors and TVC as output filters were compared. Since the inductor value and switching frequency are the same for both cases, the expected converter efficiency of steady state operation are also the same.

A reference design of 2-channel interleaving synchronous buck converter was implemented. The design specifications are: Vin = 12V, Vout = 1.5V, Iout,max = 40A (20A per channel), Rdroop = 1.7mΩ, switching frequency fsw = 300 kHz, inductance per channel = 400 nH, output capacitors are 10 pieces of 560uF*7mΩ Oscon capacitor in parallel with 20 pieces 22uF MLCC. The VR controller is ISL6565ACB from Intersil. The gate driver is LM2726 and the power MOSFETs are IRF7811 and IRF7822 for control FET and synchronous FET respectively. A dynamic load transient circuit was utilized to generate a load step change from 0 to 23A with a current slew rate of 100A/uS approximately. This design is considered the benchmark design and will be compared with the TVC solution.

Fig 4.1 shows the output voltage and each phase switching node waveforms of the benchmark design during load step change from 23A to 0. The output voltage waveform was measured on the pads of one decoupling capacitor. We can easily see that the duty cycles were saturated during load step down. This is due to the high control bandwidth design whose control bandwidth exceeds the critical control bandwidth. The DC Rdroop was strictly followed since 23A*1.7mΩ ≈ 40mV. However, because of the parasitic inductance between

the bulk capacitors and decoupling ceramic capacitors, output voltage has an overshoot. The total peak to peak voltage difference ΔV between full-load and zero-load is around 80 mV.

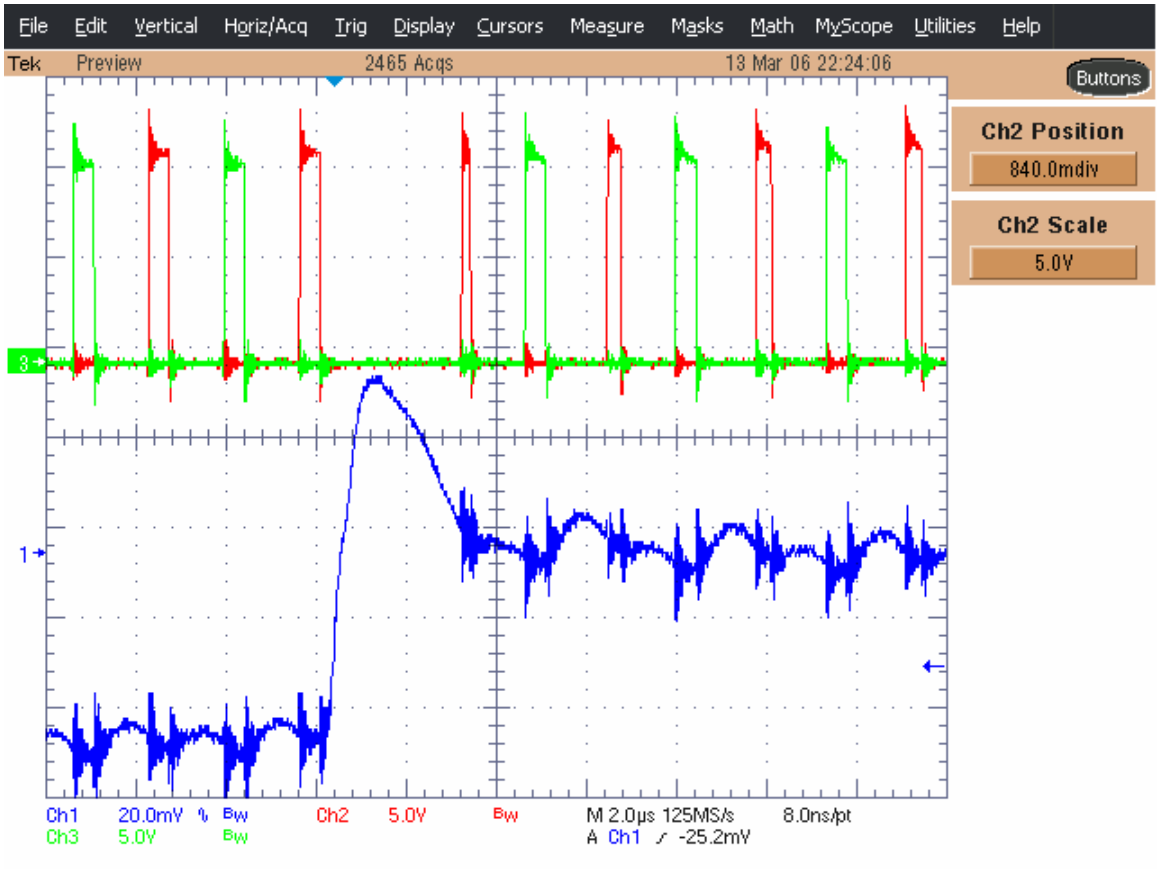

Fig 4.1 Waveforms during Load step down of benchmark design

4. 2 TVC Circuits Design Verification

With the same PCB board and simply removing all the Oscon capacitors, the VR compensator needs to be redesigned due to the modified power stage parameters. Before adding TVC, efforts need to be made to guarantee that main VR is still stable. However, even with stably switching, VR output voltage suffered from high spike during load transient due to very limited output capacitance. Since the total capacitance is less than one tenth of the

benchmark design, with the same inductor energy dumping into it, ΔV is now 173mV. (See Fig. 4.3)

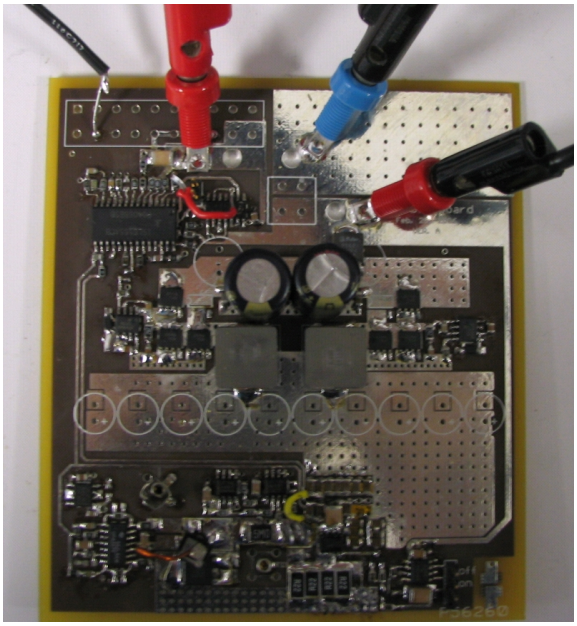

Fig 4.2 Top view of TVC demo board: All bulk caps are removed

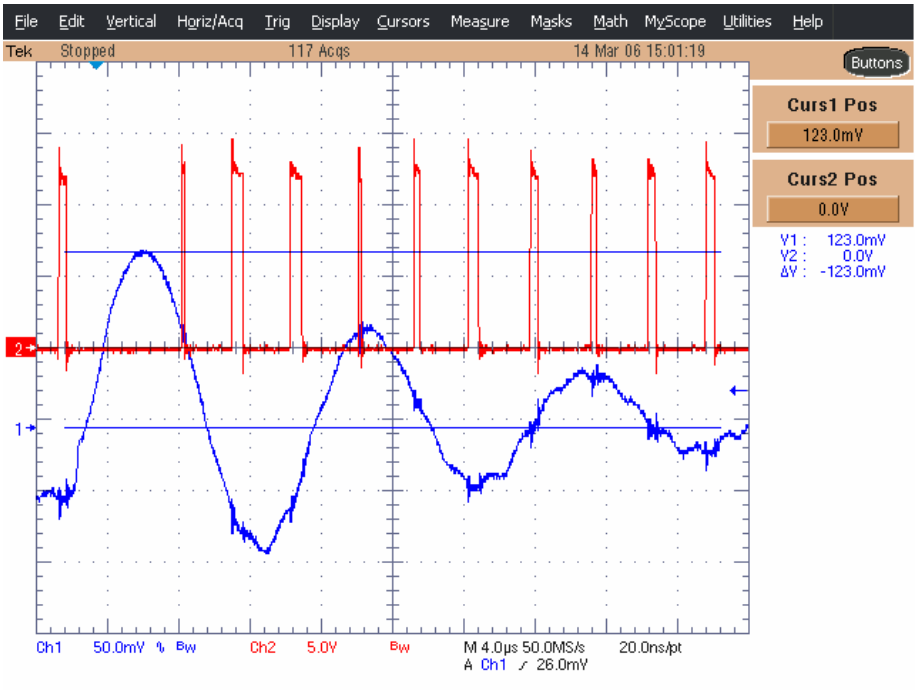

Fig 4.3 Waveforms during Load step down after removing all bulk caps

A TVC circuit thus kicked in to help with load transients. The class AB amplifier includes ZETEX 849X/951X BJT pair who has a peak current rating of 20A. A current-feedback Op Amp OPA2674 was used to set up the TVC compensator. Since it has the driving capability of 500 mA peak current, no extra buffer stage is needed to drive the class AB amplifier.

The TVC compensator was designed according to the impedance matching guide line. It was debugged and measured as a single building block. TVC input signal is delivered by the signal generator. By varying the input sinusoidal signal frequency and recording the output magnitude, one can sketch the Bode plot of the input output transfer function. Fig 4.4 and Fig 4.5 showed how this approach was taken.

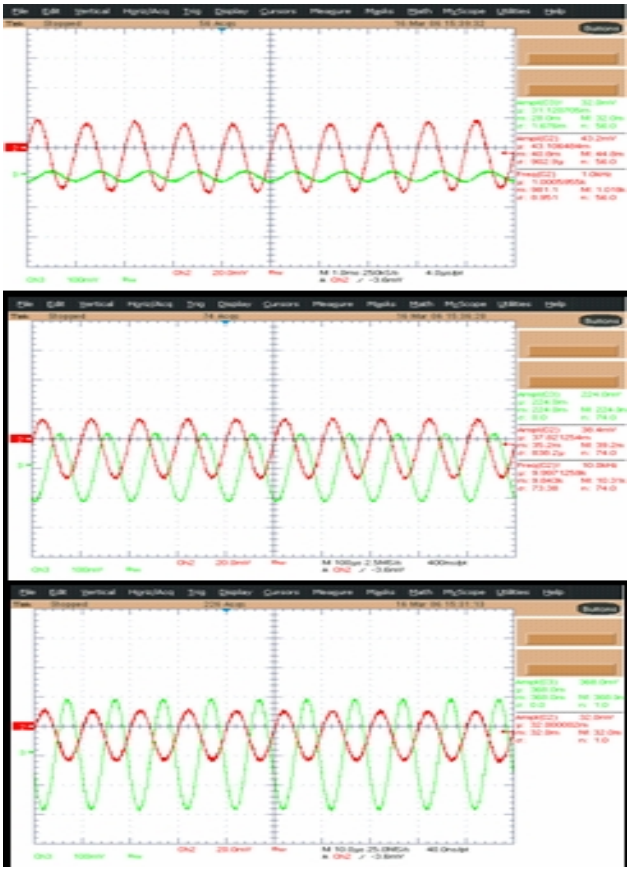

Fig 4.4 Measured TVC input output with varying frequency

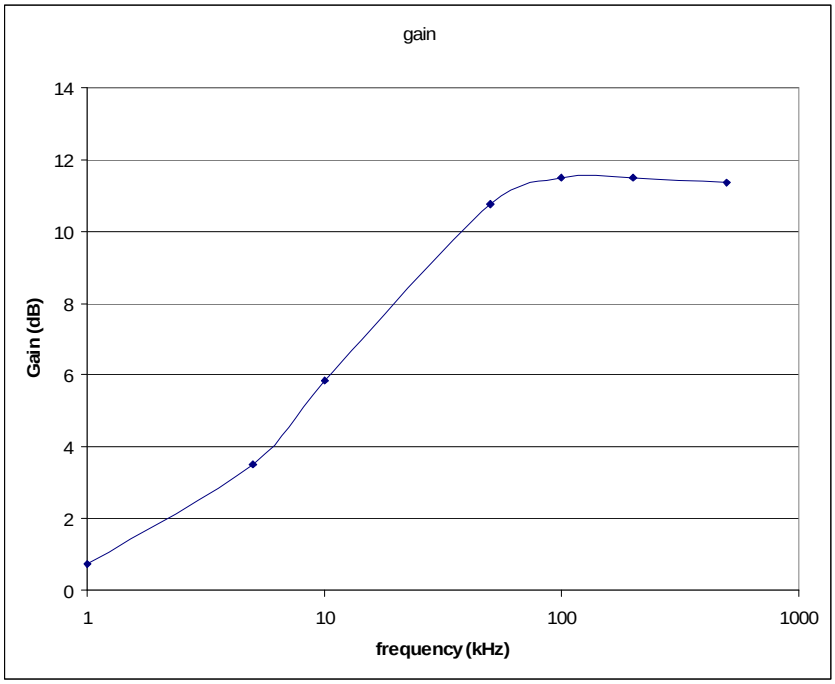

Fig 4.5 Recorded TVC compensator frequency response

4.3 Parallel Impedance Idea Verification

As mentioned in Chapter 3, changing the TVC compensator poles position will affect the dynamic currents distribution between VR and TVC. Two cases were compared to justify this concept. In case 1, TVC compensator was intentionally given a lower frequency pole which is overlapped with VR control bandwidth. In case 2, such overlapping is largely reduced. From Fig 4.6 (Case 1) and Fig 4.7 (Case 2) we can tell the TVC current difference. This phenomenon convinced us that the parallel impedance concept is applicable when we are optimizing the TVC compensator design.

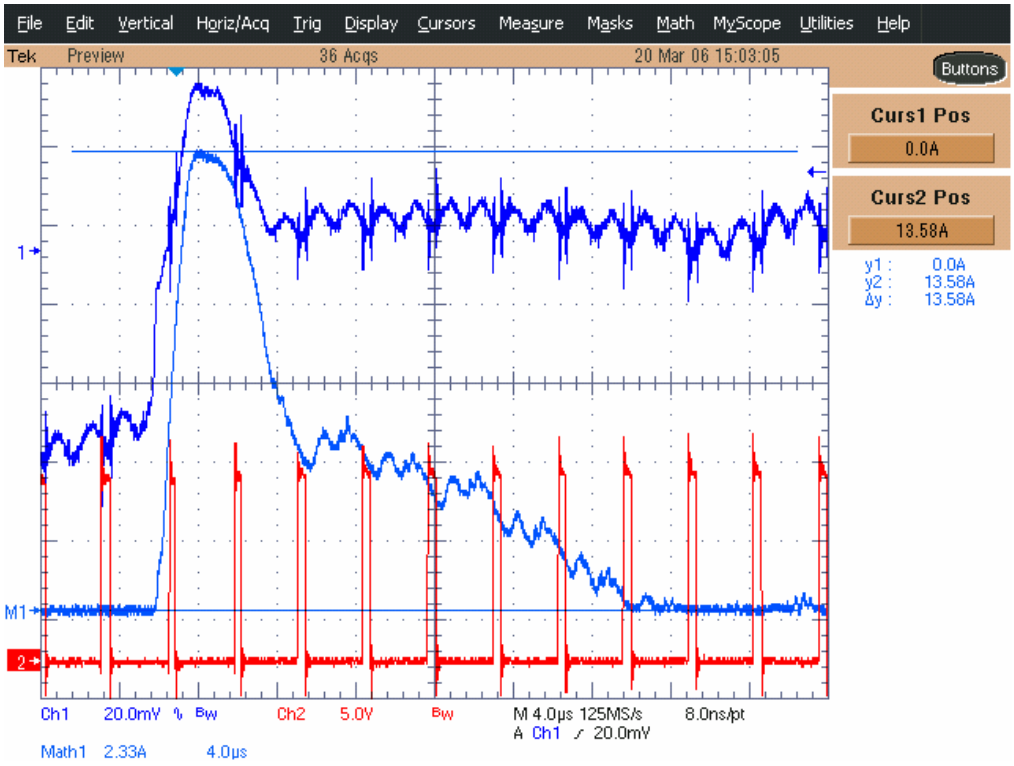

Fig 4.6 TVC current during load step down with lower compensator pole

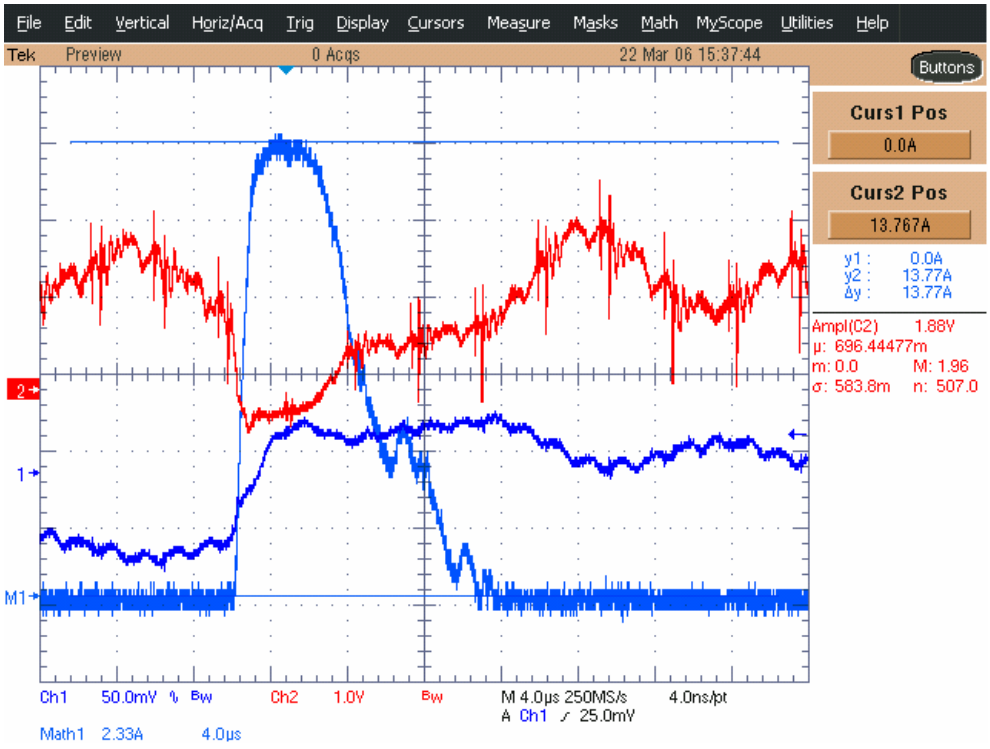

Fig 4.7 TVC current during load step down with higher compensator pole

4.4 Non-linear TVC Performance

To further reduce TVC current tail, non-linear approach was carried out. Basically there are two parts added to the original TVC: TVC current detector and duty cycle saturation logic.

The TVC current is sensed by a 5mΩ resistor. A differential signal with the maximum magnitude of about 100mV (5mΩ*20A) is then inputted to the Schmitt trigger, which is composed of TL3116 comparator and resistors. The generated pulse output goes to the NOR gates (74HC02) combining with original VR PWM output and gives out new PWM signals.

Fig 4.8 shows the input output waveforms of the Schmitt trigger. And it is shown that when input exceeds -64mV (TVC sinking current greater than 13A) an output “high” is generated and input falls to nearly zero, output resumes to “low”.

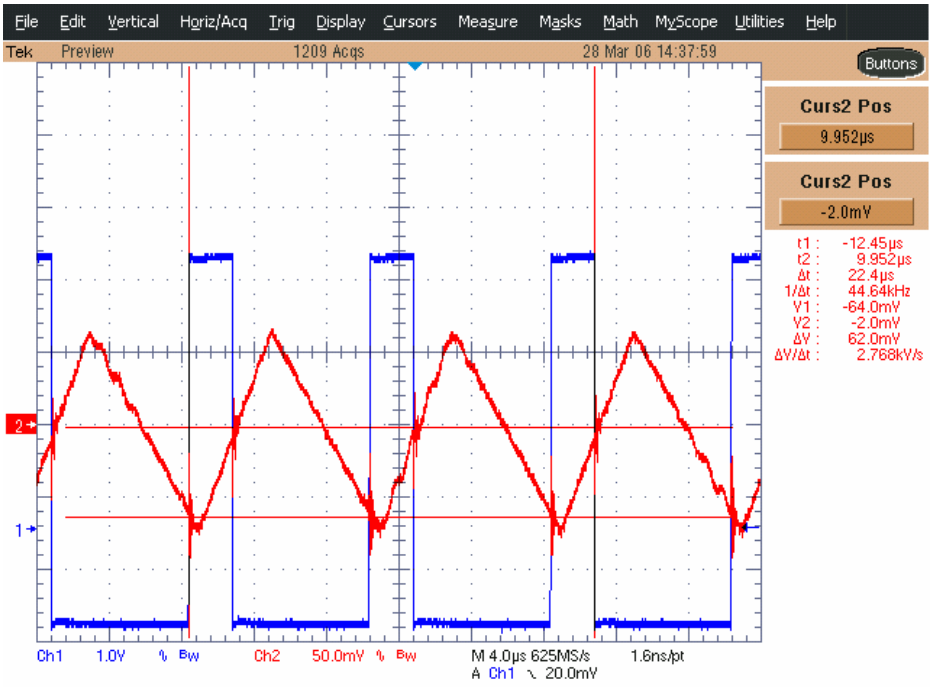

Fig 4.8 Input output waveforms of Schmitt trigger

With the non-linear TVC control scheme, a much better load transient response was achieved in terms of TVC power loss. The waveforms shown in Fig 4.9 from top to bottom are load current, output voltage and switching node voltage of one phase respectively. ΔV is 74mV now, which is even smaller than the bulk capacitor case. It is clearly shown that the duty was saturated and the effective VR control bandwidth was pushed higher.

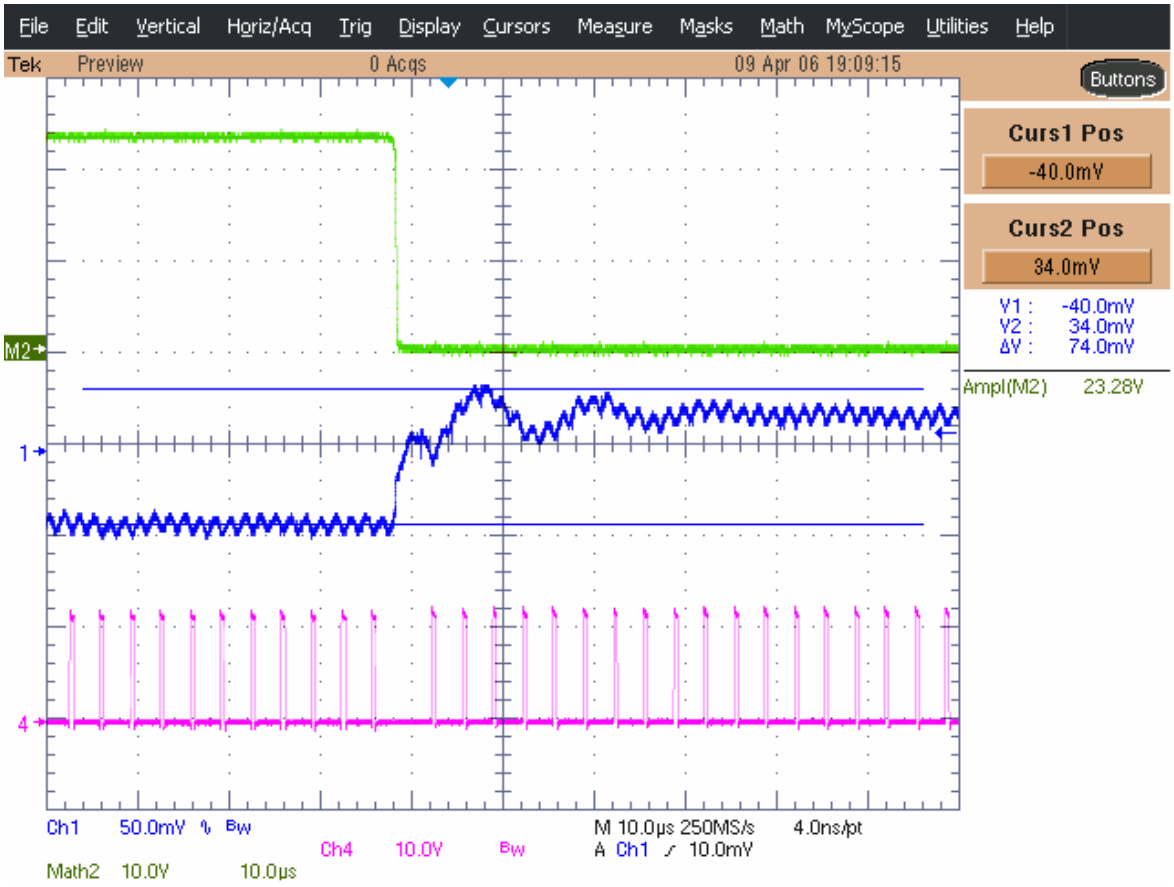

Fig 4.9 Load step down waveforms of non-linear TVC

In order to have an idea how much power loss TVC will add to the whole circuits, the TVC current and output voltage were measured and the product of them was integrated in a load step down transient. Fig 4.10 tells us that with a load changing from 23A to 0, total energy dissipated in TVC is 40uJ. Provided that each TVC can handle up to 2W power loss,

the highest load transient frequency the system can endure is then given by 2W/40uJ = 50 kHz.

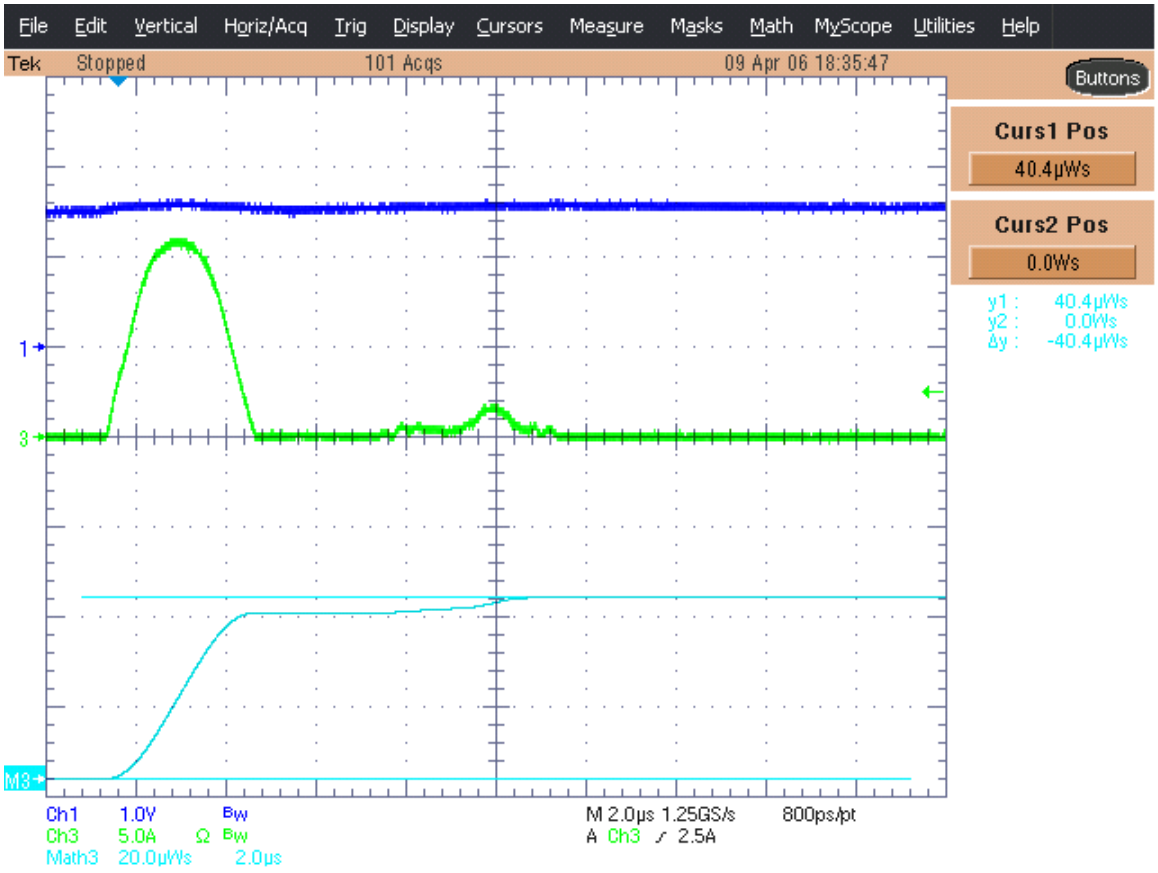

Fig 4.10 Energy dissipated in TVC during load step down

CHAPTER 5 Summary and Future Work

5.1 Summary

The main contribution of this work is the proposed design methodology of a Transient Voltage Clamp circuit. With the aid of output impedance analysis, such a TVC circuit as the silicon substitute was proposed to replace the traditional bulk capacitors.

The TVC compensator design guideline was introduced based on the output impedance requirement. With such a design, AVP performance is achieved. Dynamic currents distribution during load transients was also analyzed. A 1^{st} order approximation was concluded to model the branch current step response.

Due to the control bandwidth limitation of main VR, TVC will suffer from high power loss during load transient. A non-linear TVC control scheme was proposed and an effective VR control bandwidth based on the inductor slew rate was derived. By such a way, TVC power loss during load transient was reduced.

Further discussion on converter total efficiency was carried out. With traditional bulk capacitor solution, total efficiency is only related to load transient duty. With replaced TVC, total efficiency is also related to load transient frequency. Based on measured TVC power loss, a series of efficiency curves were generated. Below a specific load transient frequency, TVC loss has little impact on the total efficiency degradation.

As the load transient frequency goes higher and higher, the TVC current will not response accordingly. This is based on the simplified microprocessor power delivery parallel impedance model. This conclusion convinced people that TVC could be a good candidate even in the strict application such as the microprocessor power delivery.

A discrete version of TVC was built and the experimental results verified the aforementioned concepts and ideas. Non-linear TVC showed very good performance in terms of transient performance and low power loss.

5.2 Limitations

The linear type transient voltage clamp dissipates energy during load transients and it is a net power loss. This power loss is directly proportional to load transient frequency.

To design such a transient voltage clamp, frequency domain information is required such as poles and zeros placement. The design methodology is not as straightforward as calculating the inductor or output voltage ripple.

The non-linear control scheme combining with linearly compensated VR may cause some problem such as oscillation. Special concern is necessary when doing such design.

5.3 Future Work

Base on the successful discrete TVC experiment results, an integrated TVC is then proposed in order to save space and cost. The tentative pin definition is as shown below:

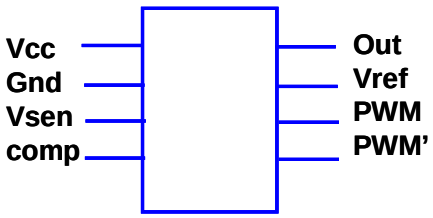

Fig 5.1 proposed TVC pin definition

Since TVC only deals with peak current, the integrated TVC chip does not need to be a powerful device. Standard CMOS technology is more than enough to implement it. In fact, in [9], a similar chip with successful experiment results was already reported.

In future VR design, output current rating is as high as more than 100A. Single TVC cannot handle such huge current. The paralleling and current sharing problem existing in the multi-phase buck converter also exists in the TVC design.

More work need to be done to further reduce TVC power loss during load transients. The supply rail voltage can be reduced; other types of capacitors can be inserted to lower TVC impedance second zero; main VR can be other high bandwidth non-linear control so that duty-cycle saturation logic is no longer required; even the pull-up network of TVC can be removed because of the asymmetric inductor current slew rates during load step up and step down.

Also in this work, dynamic VID in VR design is not considered. To put TVC into real industry practice, this is mandatory.

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