ABSTRACT

LUO, LEI. Capacitively Coupled Chip-to-Chip Interconnect Design. (under the direction of Dr. Paul D. Franzon)

In modern high performance VLSI chips high-bandwidth and high-throughput are becoming increasingly important. I/O bandwidth in the Multi-Tb/s range is required for current and future high performance VLSI chips. This trend demands high-speed, high-density and low power I/Os.

AC coupled interconnect (ACCI) has been demonstrated as a systematic solution for providing higher pin density, smaller transceiver design and lower power dissipation for high speed chip-to-chip communications. ACCI utilizes non-contact capacitor plates as signal I/O which yields a much higher pin density than traditional solder bump I/O. The coupling capacitors provide passive equalization, thus eliminating the need for costly traditional active equalization. This saves both power and area associated with the equalization circuitry used in a traditional transceiver. ACCI also saves significant power on the transmitter by using pulse signaling instead of traditional non-return-to-zero (NRZ) signaling.

The pulse receiver is one of the most important designs in ACCI. The pulse receiver is used at the receiver front end to recover the NRZ signal from the small pulse signal. A complementary low-swing pulse receiver was designed to accommodate the increased attenuation and to enable the use of smaller coupling capacitors and longer transmission lines (T-Lines). A test chip with a complete capacitively coupled serial link was designed including: a random data generator, multi-phase DLL, serializer, transmitter, pulse receiver,

clock and data recovery (CDR), deserializer and bit error rate (BER) tester. ACCI chip-to-chip communication was demonstrated through two 150fF coupling capacitors and a single end terminated 15 cm microstrip line on a FR4 board at 3Gb/s.

A fully differential pulse receiver was also designed for capacitive ACCI. The fully differential receiver was implemented in a 6-bit bus and measurements are reported for an aggregate bandwidth of 36Gb/s. Signal integrity issues associated with the ACCI bus, such as crosstalk and switching noise, are discussed. Simulation results demonstrate that higher data rates over ACCI channels can be achieved with more advanced CMOS technologies.

CAPACITIVELY COUPLED CHIP-TO-CHIP INTERCONNECT DESIGN

By

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DEDICATION

To my wife Yang, my parents Zhengbang and Juying

BIOGRAPHY

Lei Luo was born in Suzhou, China. He received the B.S. and M.S. degrees in radio engineering from Southeast University, Nanjing, China, in 1998 and 2001, respectively. From 1998 to 2001, he was also with National Mobile Communication Research Lab and Southeast Communication Inc., working on CDMA2000 base station signal processing chip design, in Nanjing, China. He started the PhD program in electrical and computer engineering at North Carolina State University, Raleigh in 2001. During the summers of 2004 and 2005, he worked for ARM and Rambus, respectively, designing high-speed serial link PHY IP. His research interests include: mixed-signal circuit design for high-speed chip-to-chip communications, inter-chip interconnect, signal integrity issues, and signal processing techniques for communications.

ACKNOWLEDGEMENTS

First of all, I would like to thank Dr. Franzon for offering me this great opportunity to work on the ACCI project. Dr. Franzon always trusted me from the time I joined his group. Without his support, encouragement and referrals, I would not have had the resources to use expensive silicon processes to test my designs and I would not have had the opportunities to work with ARM and Rambus for summer internships, where I further elevated my knowledge and skill. Although he is very busy, Dr. Franzon always has time ready to guide and discuss issues with me. His optimism along with many insights influenced me and drove this project, which were very important and valuable.

I want to thank Dr. Wilson for the many times he provided detailed technical guidance and discussions. Without his help, encouragement and patience, I would not have been able to achieve the results I have today. I also appreciate many late nights Dr. Wilson spent with me in the lab doing measurements. Those exciting moments in the lab will be always be remembered.

I want to thank Dr. Steer, Dr. Davis and Dr. Maria for their knowledgeable and valuable guidance, comments and suggestions to this work. I also learned a lot from the courses taught by Dr. Steer and Dr. Davis.

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I learned a lot from my internship experiences with ARM and Rambus. Many skills I learned from them were applied in this thesis. I would like thank Dr. Perkinson, Dr. Gray, Steve, Jason and the others at ARM, and thanks to Fred, Dr. Poulton, Teva, Dr. John Eble, Dr. Palmer, Trey, Jade, Dr. Dettloff and the others at Rambus for all the help and discussions.

I also appreciate the discussions and feedback from industry and academia through other channels. This valuable feedback helped us to develop ACCI in a more systematic and detailed manner. I would like thank Dr. Henning and Dr. Banerjee from Intel; Dr. Gerald from AMD, Dr. Bob Evans from Cisco, Dr. Clay Cranford from IBM, Dr. Tom Knight from MIT, and Dr. Angus Kingon from NCSU MSE.

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Chapter 1 Introduction

1.1 Motivation

Advances in both IC fabrication technology and circuit design have led to exponential growth of IC speed and integration levels [1]. Performance bottlenecks have gradually moved from the processing portion of the systems to the I/O section. Multi-Tb/s throughput is now required for high performance VLSI chips. This trend demands for high speed, high density and low power I/Os. Figure 1.1 (a) shows the trend of the pad count and pitch for high performance VLSI chips; (b) shows the trend of power dissipation for one chip and for each I/O for high performance chips; both predicted by ITRS [2].

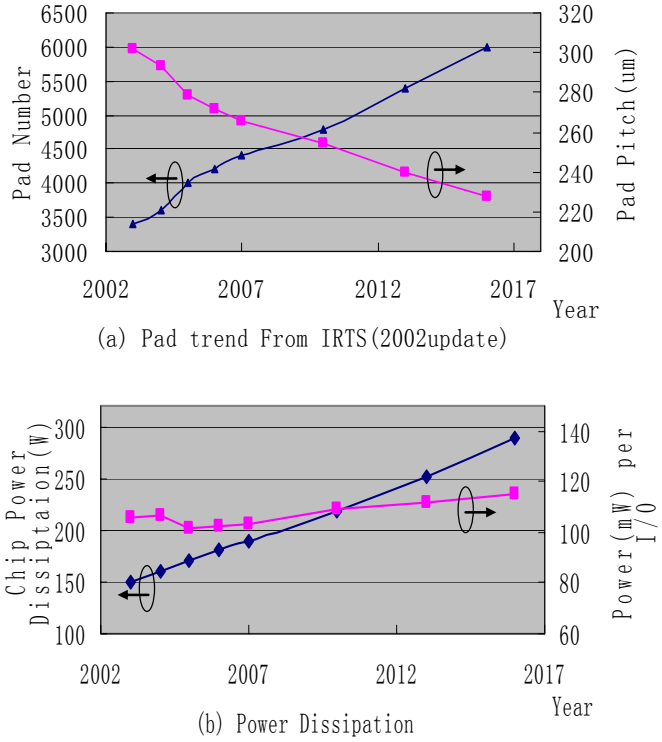

Figure 1.1 Pad and power requirements from IRTS [1]

Traditional high speed serial link I/Os use current-mode NRZ signaling. A lot of power is dissipated by the differential current-mode driver. Equalization is necessary to compensate the high frequency loss on the transmission line (T-Line) [3]. Moreover, complicated adaptive equalization is needed to accommodate the variation of high frequency channel loss [4][5].

AC Coupled Interconnect (ACCI) proposed in [6] enables much higher pin density than traditional pin or solder bump technologies. The I/O density that ACCI can provide meets the density requirement predicted by IRTS for year 2017.

[1] Assume 25% of the pins are high speed I/Os, and all of the high speed I/Os are differential.

ACCI can be applied to high speed serial link applications. Low power, low area and simple implementation can be achieved due to pulse signaling and equalization-free design. This enables even more integration of high speed I/Os [7].

1.2 Dissertation overview

Chapter 2 is a literature review. The trends of serial link design are illustrated and current commercial standards are summarized. A typical serial link transceiver design is described in the architecture level. Applications of previous capacitively coupled I/O designs are reviewed. Both physical structures and circuit designs are discussed.

Pulse signaling with capacitive coupling is proposed in chapter 3 to design low power serial links with passive equalization. Based on the channel response, it is proved that active equalization for high frequency compensation is no longer necessary in ACCI. Instead, a latch based receiver is designed to compensate the low frequency loss. A complementary low swing pulse receiver is designed to allow greater attenuation and to enable smaller coupling capacitors and longer transmission lines (T-Lines). Simulation and analysis on variations of coupling capacitors and T-Line lengths are given.

A complete ACCI serial link test chip is presented in chapter 4. A test chip is designed based on the proposed pulse receiver. The test chip includes random data generator, multi-phase DLL, serializer, driver, pulse receiver, clock and data generator, deserializer and bit error tester. Architecture and circuit details are presented for both the transmitter path and receiver path. ACCI chip-to-chip communication is demonstrated through two 150fF coupling capacitors and a single end terminated 15 cm microstrip line on FR4 at 3Gb/s.

In chapter 5, a differential pulse receiver is designed for higher bandwidth operation. Signal integrity issues associated with ACCI bus, such as crosstalk, switching noise are analyzed. Higher data rate chip-to-chip communications over ACCI channel with more advanced CMOS technologies are investigated through simulations. Measurements of 36Gb/s operation over 6 bit wide ACCI bus are reported.

In chapter 6, contributions of this work are stated. Future work is proposed as well.

1.3 Publications during the Ph.D work

1.3.1 Journal papers

1. Luo, L.; Wilson, J.; Mick, S.; Xu, J.; Zhang, L. and Franzon, P., "3Gb/s AC Coupled Chip-to-Chip Communication using a Low Swing Pulse Receiver," to be appeared in *Journal of Solid-state circuits*, a special issue for *ISSCC05*, Jan. 2006.

2. Mick, S.; Luo, L.; Wilson, J. and Franzon, P.; "Buried Bump and AC Coupled Interconnection Technology," *IEEE Transactions on Advanced Packaging*, vol. 27, pp. 121–125, Feb. 2004.

3. Xu, J.; Mick, S.; Wilson, J.; Luo, L.; Chandrasekar, K.; Erickson, E.; and Franzon, P. "AC Coupled Interconnect for Dense 3-D ICs," *IEEE Transactions on Nuclear Science,* pp. 2156-2160, Oct. 2004.

1.3.2 Conference papers

1. Luo, L.; Wilson, J.; Mick, S.; Xu, J.; Zhang, L.; and Franzon, P. “A 3Gb/s AC Coupled Chip-to-Chip Communication using a Low Swing Pulse Receiver,” *ISSCC Dig. Tech. Papers,* 2005, pp. 522-523.

2. Luo, L.; Wilson, J., Xu, J.; Mick, S.; and Franzon, P. "Signal Integrity and Robustness of ACCI packaged systems,” *Electric Performance on Electronic Packaging*, Oct 2005.

3. Xu, J.; Mick, S.; Wilson, J.; Luo, L; and Franzon, P.; “2.8Gb/s Inductively Coupled Interconnect for 3-D ICs,” in *Proc. Symp. VLSI Circuits,* 2005.

4. L. Zhang, J. Wilson, R. Bashirullah, L. Luo, J. Xu, and P. Franzon, “Driver Pre-emphasis Techniques for On-Chip Global Buses,” *International Symposium on Low Power Electronics and Design, Aug. 2005.*

5. Wilson, J., Xu, J.; Mick, S.; Luo, L.; Salvatore Bonafede, Alan Huffman, Richard LaBennett and Franzon, P. " Fully Integrated AC Coupled Interconnect using Buried Bumps,” *Electric Performance on Electronic Packaging,* Oct. 2005.

6. Xu, J.; Mick, S.; Wilson, J.; Luo, L; Chandrasekar, K.; Enckson, E.; Franzon, P.; "AC Coupled Interconnect for Dense 3-D ICs,” *IEEE Nuclear Science Symposium Conference Record*, 2003, vol. 1, pp. 125–129.

7. Franzon, P.; Mick, S.; Wilson, J.; Luo, L. and Chandrasakhar K.; Invited Paper, “AC Coupled Interconnect for High-Density High-Bandwidth Packaging” *Proc. SPIE*, *Microelectronics: Design, Technology and Packaging*, Perth , Australia , December 2003. pp 67-69.

8. Franzon, P.; Mick, S.; Wilson, J.; Luo, L. and Chandrasekar, K.; "AC Coupled Interconnect for High-Density High-Bandwidth Packaging," *International Conference on Solid State Devices and Materials*, Tokyo, Japan, Sep. 2003.

9. Franzon, P.; Kingon, A.; Mick, S.; Wilson, J.; Luo, L.; Chandrasekar, K.; Bonafede, S., Statler; and C., LaBennett, R.; "High Frequency, High Density Interconnect Using AC Coupling," *Materials Research Symposium*, Invited Paper, Session B6.1, Boston, Massachusetts, Dec. 2003.

10. Mick, S.; Luo L.; Wilson, J. and Franzon, P.; "Buried solder bump connections for high-density capacitive coupling," *IEEE Electrical Performance of Electronic Packaging*, Oct. 2002, pp. 205-208.

1.4 Technical Honors Received During the Ph.D Work

1. Intel Best Student Paper Award at the *14th IEEE Electrical Performance of Electronic Packaging Conference* held in Austin, TX, Oct. 2005, for the paper titled "Signal Integrity and Robustness of ACCI Packaged Systems".

2. The *ISSCC05* paper "A 3Gb/s AC Coupled Chip-to-Chip Communication using a Low Swing Pulse Receiver" is invited to a *Journal of Solid-state Circuit* special issue in Jan. 2006.

3. Won 1st place in NC State University ECE Graduate seminar competition, Aug. 2004, Raleigh, NC

1.5 Abbreviations

ACCI	AC Coupled Interconnect
b/s	Bit per Second

BER	Bit Error Rate
C3MOS	Capacitve Coupled CMOS
CDR	Clock and Data Recovery
CMFB	Common-Mode Feed Back
DAC	Digital to Analog Converter
DLL	Delay Locked Loop
DFE	Decision Feedback Equalization
FF	Flip Flop
FFE	Feed Forward Equalization
FIR	Finite Impulse Response
FSM	Finite State Machines
PYH	Physical layer
IIR	Infinite Impulse Response
IP	Intellectual property
ISI	Inter-Symbol-Interference
ITRS	International Technology Roadmap of Semiconductor
LFSR	Linear Feedback Shift Registers
LMS	Least Mean Square
LVDS	Low Voltage Differential Signaling
MCM	Multi-Chip Module
NRZ	Non-Return-to-Zero
QF	Quantized feedback
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
SNR	Signal-to-Noise Ratio
SSN	Synchronous Switching Noise
T-Line	Transmission Line
TX	Transmitter
TRX	Transceiver
UI	Unit Interval

VCO	Voltage Controlled Oscillators
V_{PPD}	Voltage Peak-to-Peak Differential
V_{SEPP}	Voltage Single-Ended Peak-to-Peak
Xtalk	Cross Talk

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Chapter 2 Chip-to-Chip Interconnect

For many digital systems, the major performance-limiting factor is the interconnect bandwidth between chips, boards and cabinets. Examples of the applications include Gigabit Ethernet, Xaui, 10GE, Fiber Channel, backplane transceivers, network switches, multi-processor networks and CPU-to-memory links.

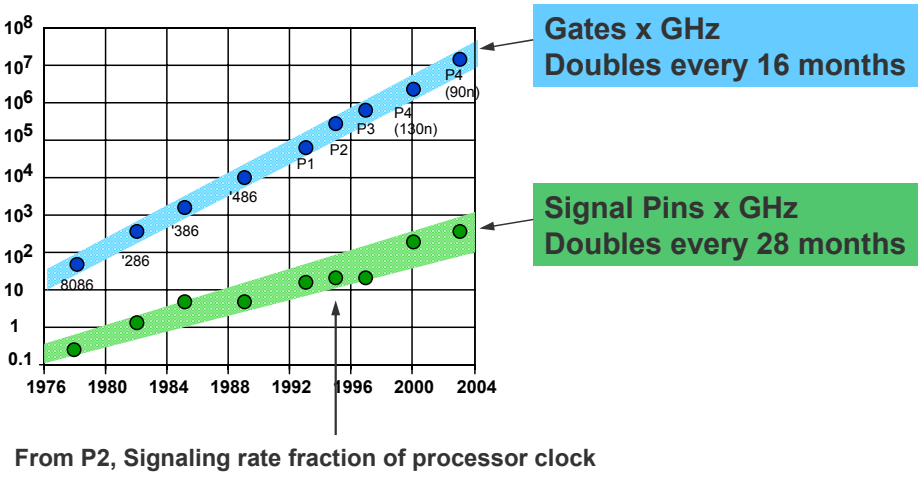


Figure 2.1 Off-chip bandwidth Vs On-chip bandwidth

As VLSI technology continues to scale, system bandwidth will become an even more significant bottleneck. This is because the number of I/Os will scale more slowly than the bandwidth demands of chip logic. Also, off-chip signaling rates have historically scaled more slowly than on-chip clock rates [3], as shown in Figure 2.1.[17]

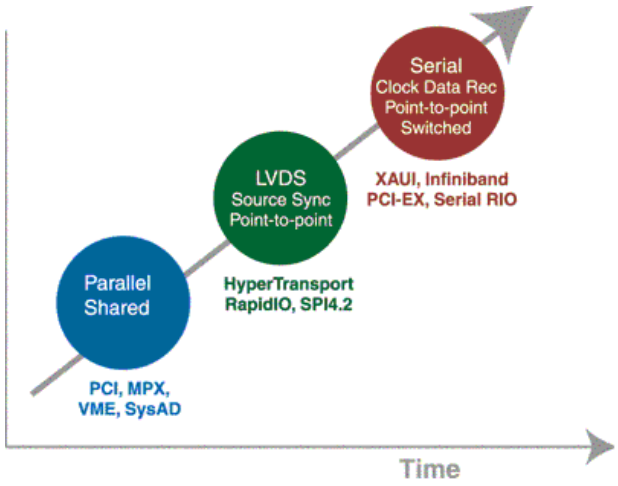


Figure 2.2 Off-chip Interconnection revolution for medium and long links [8]

Figure 2.2 shows the evolution of off-chip interconnects. For shared parallel interconnect, the data lines and clock of the bus must have traces carefully matched in length to minimize any skew, which is not feasible for high speed communication. LVDS source synchronous point to point offers smaller skew and higher speed communication, but it needs an extra clock path to go along with each signal path, which means more pins and interconnects. A serial link approach offers fewer pins and reduced skew sensitivity and thus is suitable for high speed interconnect with smallest pins. This work is focused on serial link applications.

This chapter is a literature review on both serial links and capacitive coupling I/Os. Current commercial high speed link standards and major trends are summarized. A typical serial link

transceiver design will then be described at the architecture level. Previous capacitive coupling I/O designs will be presented on both physical structures and circuit levels.

2.1 Current commerical high speed links

Standards	Lanes	Gb/s	Channel coding	Media [1]	applications	Companies	Misc.
SONET OC-192	1	9.95	FEC	O	Data comm. WAN	ATT,Verizon, Cisco,Nortel…	OC-3-12-48 & OC-768
Infiniband	1,4,8, 12	2.5, 5, 10	8/10	O/E	System/WAN	Intel, Agilent IBM, Sun…	
Serial RapidIO	1,4	1.25, 2.5, 3.125	8/10	E	System	Motorola, Lucent, AD, TI, AMCC…	
Hyper Transport	2,4,… 32	Up to 2.8	N/A	E	System, chip to chip	AMD,Sun, Apple, Cisco, Broadcom…	Parallel links, share clock per 8 lines, low latency;
10Gb Ethernet	1	10	8/10 64/66	O	Data comm. LAN	3Com Cisco Intel…	Finished on 2002
10Gethernet XAUI	4	3.125	8/10	E	Data comm.	3Com Cisco Intel…	Finished on 2002
Fibre Channel	1,4,12	1.06, 2.12, 3.1875, 10.519	8/10	E	Storage, SAN	Agilent, Agere, IBM, Cisco…	
SAS	1	1.5, 3	8/10	E	Storage, SAN	HP, Intel, LSI logic…	
PCI Express	1,2,4.. .32	2.5	8/10	E	System, chip to chip	AMD, Cadence, Agilent…	Turbo PCI Express goes to 6Gb/s
Aurora	1 to 16	3.125			System, chip	Xilinx	
RocketIO	Up to 20	2.5 to 10	8/10 or 64/66	E	Server, SAN	Xilinx	

Table 2.1 Summary of typical commercial high speed links [54] - [65]

[1] E is electrical media such as cable, copper traces and etc. O is optical media.

Industry is putting a great deal of effort in designing high speed links, as shown in Table 2.1. Several standards are established. Some of them already have lead to successful products; some of them are at the test stages. Most of these standards are still moving forward to squeeze more bandwidth from the Shannon channel capacitance. Below are some of the trends from this summary table:

1. Most of these high speed links are serial links, which means individual clock and data recovery per line. Hyper Transport is the only exception, where a source synchronous architecture is used and eight channels share one clock. This is used to reduce power and latency for chip to chip applications.

2. Most of the applications employ 8B/10B coding in physical layer. This channel coding is used to balance the number of '1's and '0's, to add activities for clock recovery, to enable error detection and to provide some special characters.

3. No error-correction coding is used in high speed links because the channel response in high frequency region is so bad. The bandwidth penalty due to the error-correction coding overhead will be large especially for high speed links.

4. Most of the optical link designs are at 10Gb/s and are moving forward to 40Gb/s in OC-768. Most of the electrical link designs are at 3Gb/s and are moving forward to 6-10Gb/s in Rocket IO, Turbo PCI Express and Fibre Channel. Electrical cable is cheap and can be high density, but the channel response at high frequency (more than 5GHz) is terrible.

5. Typical throughput is 1Gb/s to 200Gb/s, which is achieved by both squeezing high speed and using multi-lanes.

2.2 A typical Chip-to-Chip serial link I/O design

Figure 2.3 shows a traditional current-mode differential serial link [1][3][13][14][15]. A strong transmitter drives differential current over the T-Line. Receiver side termination resistors convert the differential current into voltage swing and feed to one or more sense amplifiers. The clock and data recovery is realized at the receiver side. Data is regenerated by the sense-amplifier based samplers. In the following sections, the architecture and circuit design will be reviewed for transmitter, receiver, timing circuits and equalization schemes.

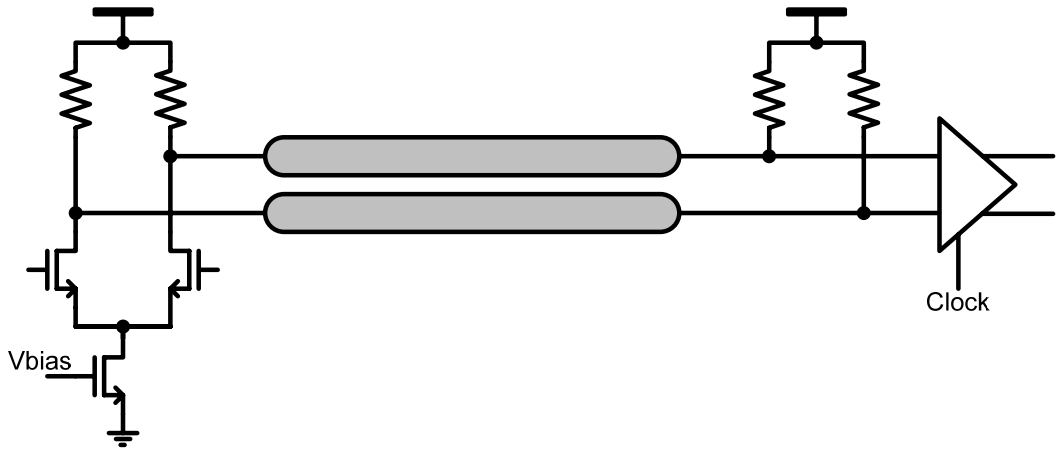


Figure 2.3 Traditional current-mode serial link: terminated at both ends to limit reflections; with source coupled current driver and regenerative sense amplifier receiver.

2.2.1 Transmitter design

As show in Figure 2.4, the low speed digital signals are multiplied. A driver with transmitter side equalization is applied to compensate the high frequency loss due to the T-Line.

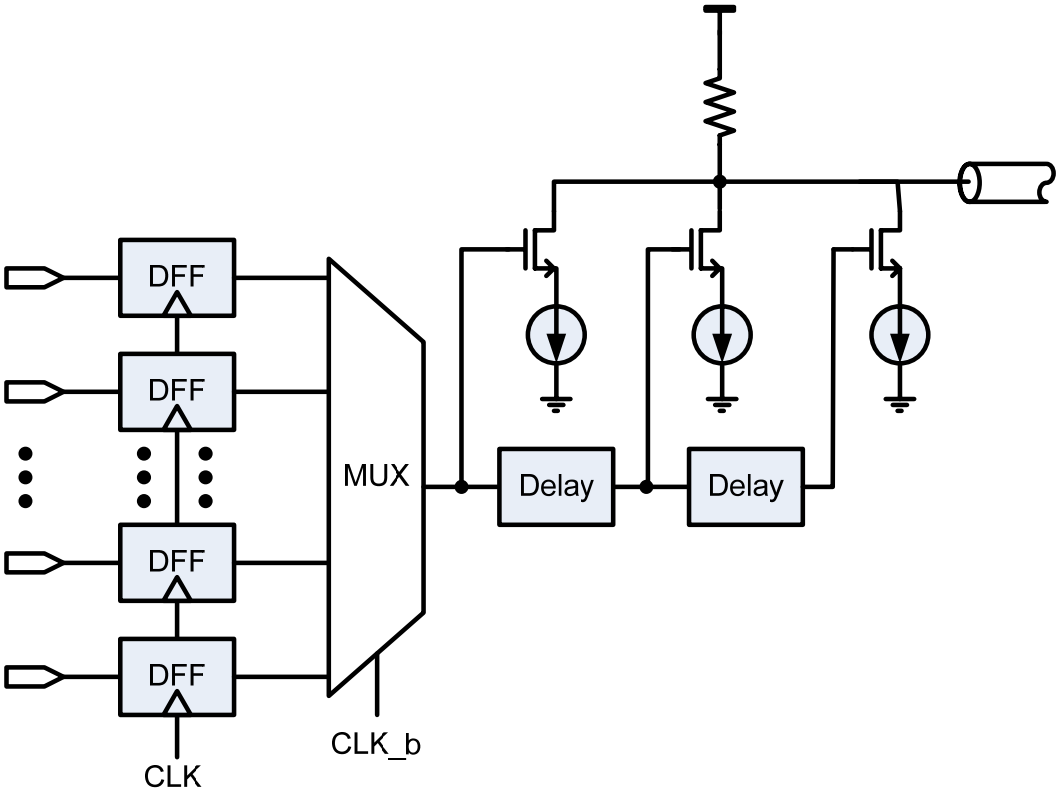


Figure 2.4 Traditional serial link transmitter design: MUX, Equalization and driver

A Multiplexer is necessary to save expensive off-chip I/Os by sharing slow data paths from the logic chip. The shortest achievable clock period in a logic chip in a given technology is limited to be no less than $8\tau_4$[2] (about 0.8ns in 0.18um technology)[14][16], while the MUX, driver and the channel can support a much higher data rate with bit period less than τ_4. A 4:1 or even 8:1 MUX can be applied to generate a high speed serialized data.

Active equalization is also necessary to extend the data rate and the distances by compensating for the frequency-dependent attenuation of the transmission line mainly due to skin effect and dielectric loss, as shown in Figure 2.5. A digital equalization scheme at the

[2] τ_4 is FO4 inverter delay, which can be estimated by 500*ps*L, where L is min channel length. [16]

transmitter path is proposed in [3]. The analog current summing transmitter FIR filter shown in Figure 2.4 is widely used in serial link designs. Comparing with receiver side equalization, transmitter side equalization is simple to design and implement. But transmitter side equalization is less flexible to channel variation since the tap coefficients are fixed unless adaptive equalization [18][19] is applied.

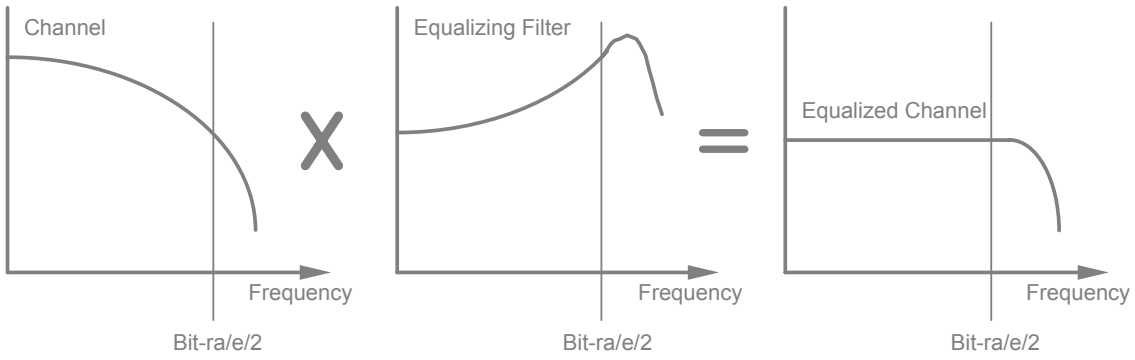


Figure 2.5 Equalization for serial links, can be at either TX side or RX side [17]

2.2.2 Receiver design

Figure 2.6 shows a typical serial link receiver. The data is 2X over-sampled and then fed into a semi-digital clock and data recovery circuitry. The receiver side equalization can further reduce ISI. Serial link protocols usually set requirements on both the eye opening at transmitter output and the tolerance of eye opening at receiver input. To reach the later requirement, the receiver needs to use equalization to improve the worst required eye opening. Comparing with transmitter side pre-emphasis, receiver side equalization is usually more complex, but offers adaptive equalization capability to meet variations of link and process-voltage-temperature (PVT). Recent designs with adaptive receiver side equalizer are reported in [22][27][28].

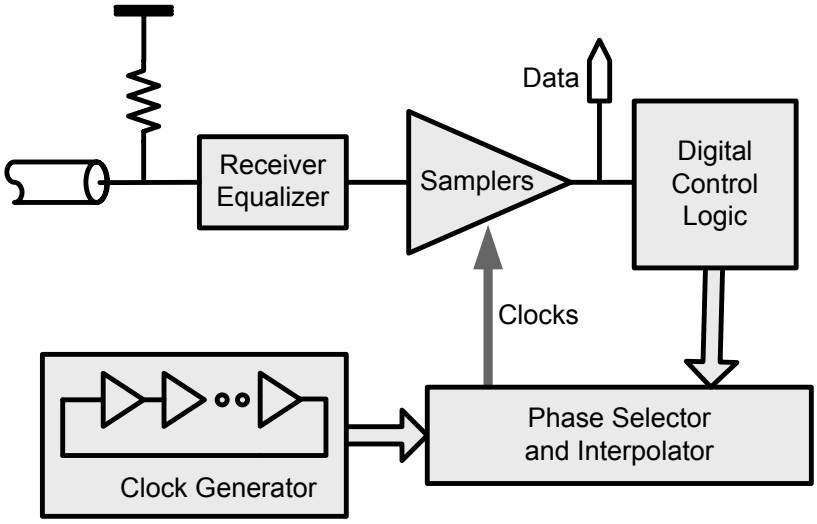


Figure 2.6 Traditional serial link receiver design, including sampler and a semi-digital clock and data recovery circuit

The sampler is usually implemented by clock triggered regenerative sense amplifier, for example, the strong-arm sense amplifier in [20]. A semi-digital clock and data recovery circuit [21] is widely used because of its unlimited phase capture range crossing variations of data rates and link delays.

2.2.3 Equalization

For a copper trace channel, the high frequency attenuation becomes more severe at higher data rates. Thus, equalization [23]-[26] has become a crucial part of serial link design to reduce inter-symbol-interference (ISI). Both the self-generated noise and noise rejection performance are important when implementing the equalization.

There are many ways to categorize equalization schemes. In the following, three aspects of equalization schemes are described.

2.2.3.1 Forward and Backward Equalization

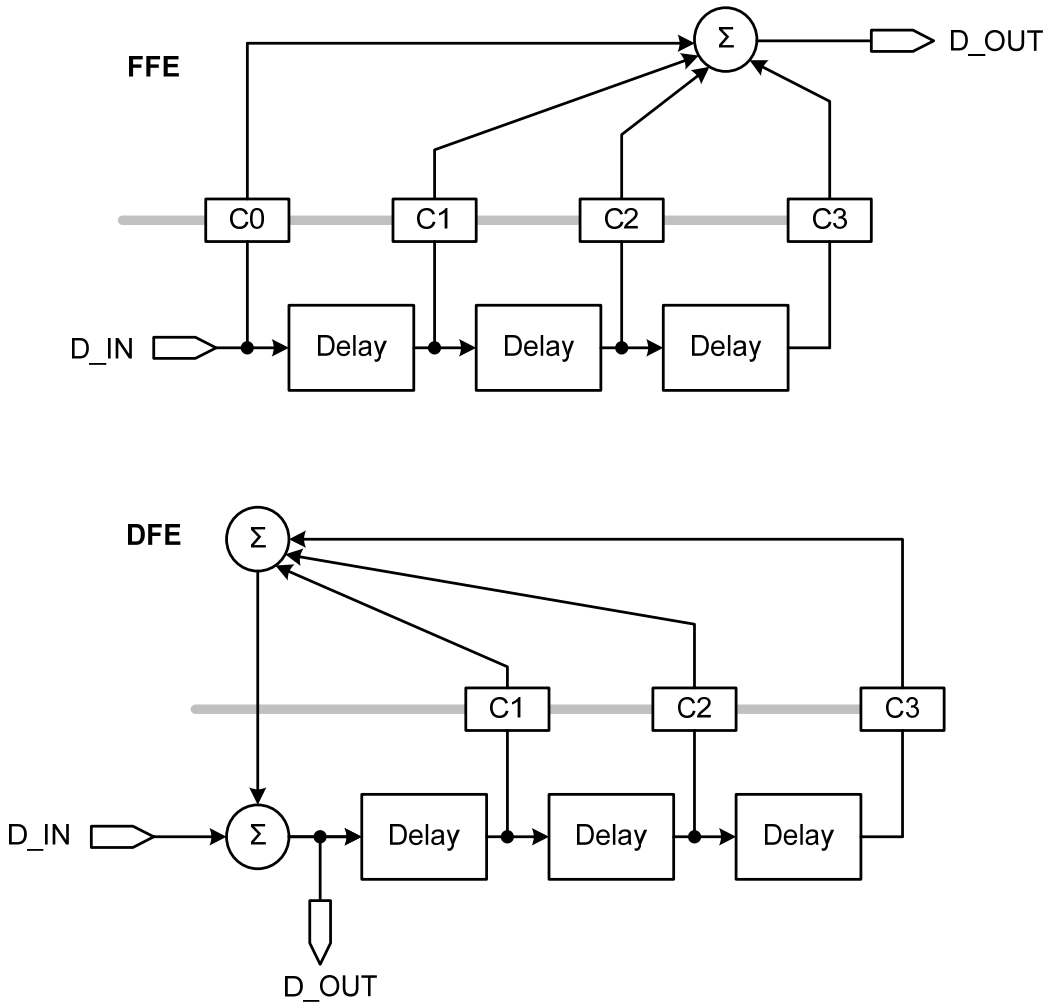


Figure 2.7 (a) FFE and (b) DFE

Equalization can be implemented as either forward or backward. Figure 2.7 (a) shows a feed forward equalization (FFE). There are four taps in this structure. C0 is the coefficient for the main tap, while C1, C2 and C3 are equalization tap coefficients. These taps are used to de-emphasis or to remove the residual of previous bits which could otherwise cause ISI. The coefficients and the delay time are optimized based on the characteristics of the ISI. The delay cell can insert either a continuous delay or a discrete-time delay, for example a bit

period delay. FFE can be used at either transmitter side as pre-emphasis or at receiver side as high frequency booster.

Figure 2.7 (b) is a decision feedback equalization (DFE). The delay cell here is usually implemented to provide one bit period delay. DFE is usually used at receiver side to remove the ISI. The feedback loop introduces a potential error propagation issue, which is not a problem in FFE.

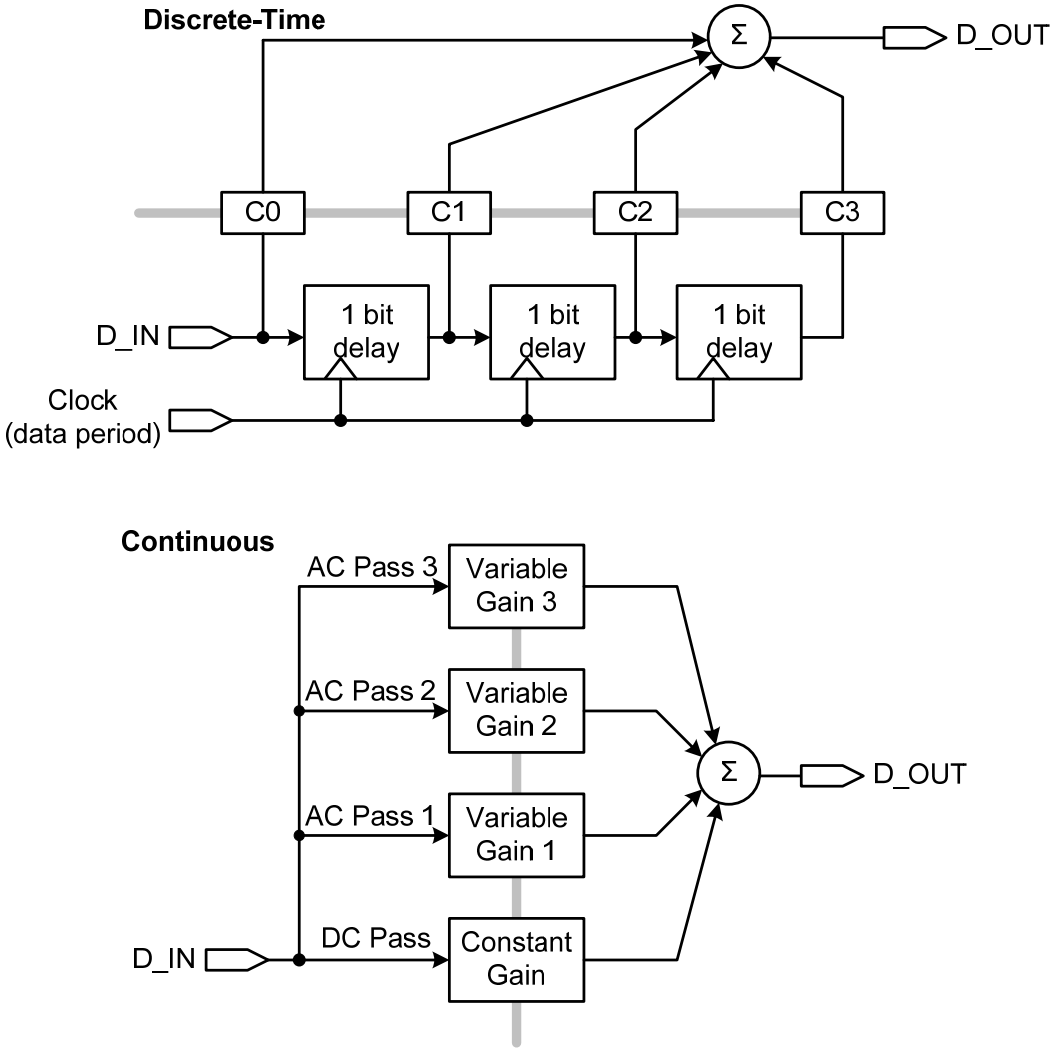


Figure 2.8 (a) Discrete-Time and (b) Continuous Equalization Schemes

2.2.3.2 Continuous or Discrete-time Equalization

Equalization can be implemented in either continuous-time or discrete-time. A discrete-time FFE implementation, usually called finite impulse response (FIR) filter, is shown in Figure 2.8 (a). An FIR filter is usually used at the last stage of transmitter to do pre-emphasis or de-emphasis. It can be easily implemented by using digital-analog converter (DAC) tail currents. The side product of pre-emphasis is that it introduces more high frequency signal onto the channel, which could cause more crosstalk noise and switching noise.

A continuous-time implementation, usually called infinite impulse response (IIR) or analog FIR (AFIR) or continuous FFE or "high frequency boost", is shown in Figure 2.8 (b). It is used at receiver front end to compensate the high frequency loss in the channel. One of the drawbacks of this continuous FFE is that it linearly amplifies both signal and noise at receiver input. The noise comes from crosstalk noise, reflection noise, switching noise, etc.

2.2.3.3 Adaptive Equalization

Equalization tap coefficients can be implemented as constant values or can be dynamic controlled. The copper trace channel with via connectors can have various possible channel responses for different applications. It is desirable to have a dynamic control function on the tap coefficients. Figure 2.9 shows the transmitter side tap coefficients controlled by the least mean square (LMS) algorithm through an up-link channel from receiver to transmitter.

Figure 2.10 shows a typical IIR at front-end receiver with its tap coefficients and analog delay being dynamically adjusted.

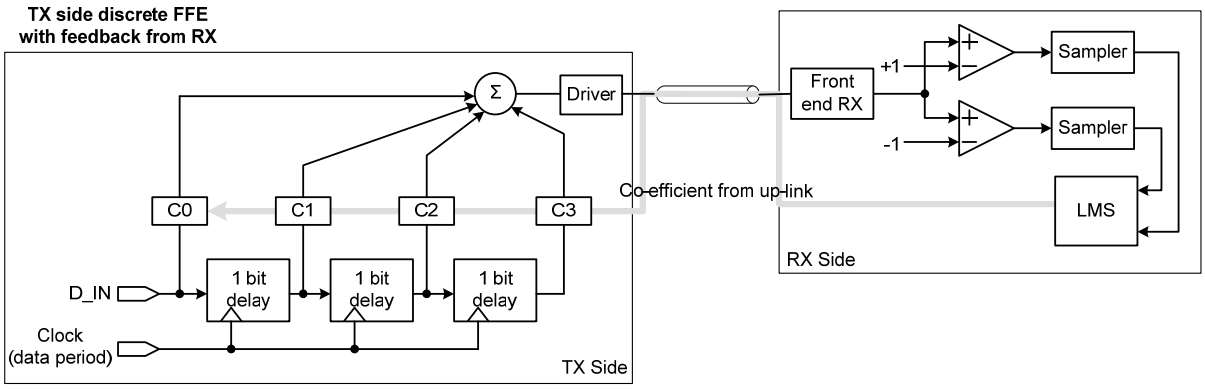


Figure 2.9 Feedback to TX side FIR

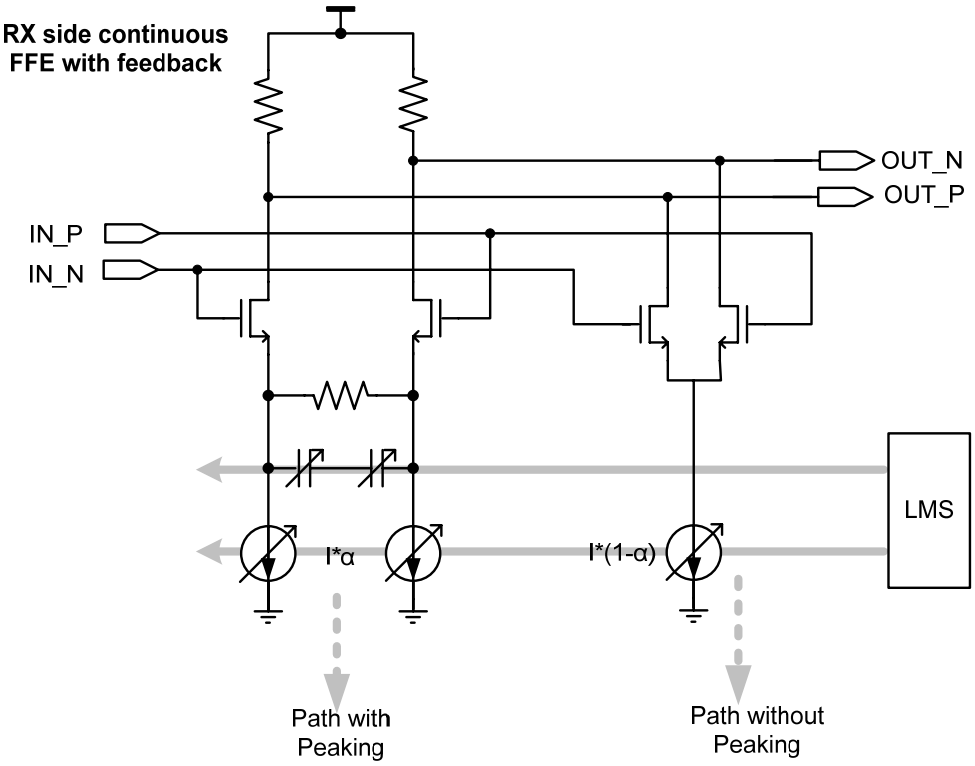


Figure 2.10 Feedback to RX side Continuous FFE

2.2.3.4 Decision Feedback Equalization

DFE is an alternative to analog FFE, used at the receiver side. Figure 2.11 shows a typical DFE at the receiver side with its tap coefficients being dynamically adjusted through the LMS algorithm. In contrast to continuous FFE, where both the signal and the noise are

peaked at high frequency range, DFE only amplifies the signal. This is because DFE is non-linear and it only feeds back the digitized signal. This feature makes DFE suitable for equalization of a noisy channel.

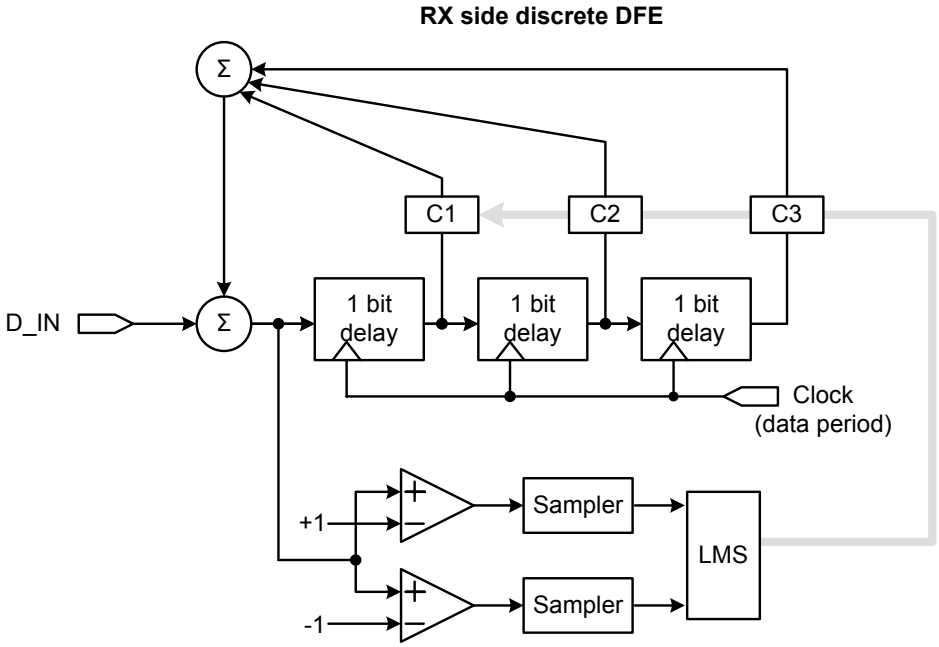


Figure 2.11 decision feedback equalization (DFE)

However, there are drawbacks in DFE:

1. DFE is usually implemented in discrete-time, which means the clock and data recovery (CDR) needs to perform correctly even before the DFE functions. This requires a preliminary eye diagram opening before DFE functions.

2. DFE has error propagation issue due to its feedback structure, which is not a problem in FFE.

3. Due to its architecture, the pre-curser can't be equalized by the DFE. Instead, FFE can equalize the pre-curser.

2.2.3.5 Equalization Implementations

Based on the characteristics presented in all these equalization schemes, the most feasible and noise robust serial link would have those three equalization schemes combined together.

1. At transmitter side, use an FIR (discrete FFE) at transmitter side to provide moderate pre-emphasis. Too much transmitter side equalization will cause more noise, such as crosstalk and switching noise.

2. At receiver front end, use an IIR (continuous FFE) to boost high frequency signal and open the signal eye diagram for CDR to operate.

3. Then use a DFE to further reduce ISI and open the eye diagram. DFE is essential to get fine equalization and good BER for noisy channels without amplifying the noise.

2.2.4 Timing circuits

Timing circuits in a serial link include the multi-phase clock generator and the phase recovery circuits.

2.2.4.1 Multi-phase clock generator

There are three decisions to make when designing the clock generator:

1. Full speed clock versus multiplying clock as shown in Figure 2.12.

A full rate clock architecture requires higher circuit speed but has inherently better jitter performance and simple design using voltage controlled oscillators (VCO). An additional high speed clock needs to be generated separately since the logic clock has the same rate as the input parallel data. Generating and on-chip routing of such a high frequency clock may

bring high frequency noise to its neighbor signal lines. Full rate clocks are usually used in high performance optical transceivers [29][30] where jitter performance is critical.

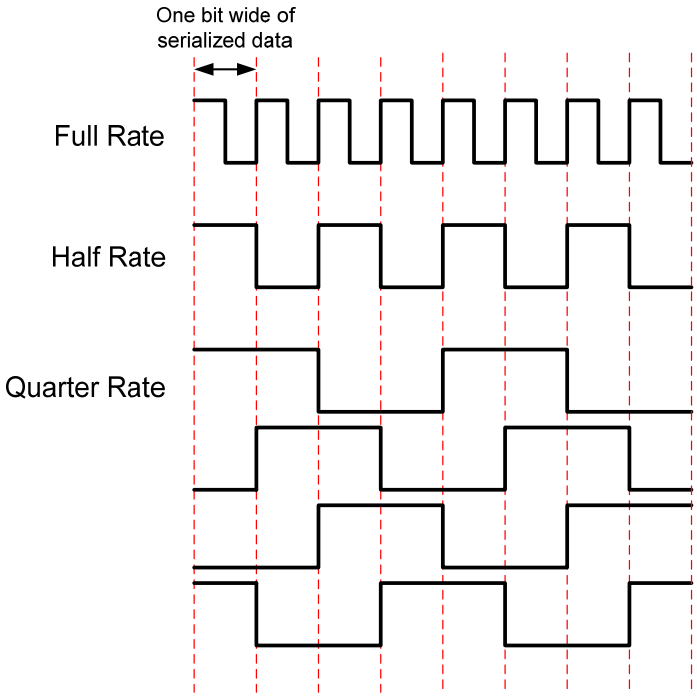


Figure 2.12 Clock speed: full rate or half rate or quarter rate of serialized data rate

A half rate architecture [31] samples at both the rising and falling edge of the clock. It eases the speed requirement of the VCO, but suffers from the deviation of clock duty cycle.

A multiplying clock can have the same low frequency as the logic clock and they can be shared. It can be quarter rate or even slower. For example, quarter rate clocks [14][15] provide bit period by combination of the four clocks. It eases the clock speed but brings unavoidable deviation of phase offset between neighboring clocks due to uneven matching. Even with a carefully laid out DLL structure, exact quarter phase offset is very difficult to achieve.

In this section, we will focus on multi-phase clock scheme for low power and simple design.

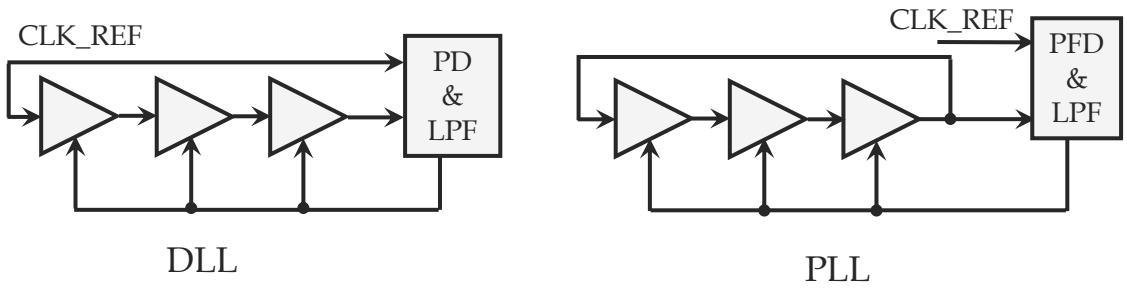


Figure 2.13 Basic schematic for DLL and PLL loop

2. PLL or DLL

A DLL can only recover clock phase while not frequency. Thus, for the cases where clock synthesis is needed, A PLL is preferred. However, A PLL has a jitter accumulation effect, which makes it more susceptible to power-supply and substrate noise [33]. On the other hand, a DLL is easy to design and is inherently stable. A DLL is used based on the assumption that the capacitively coupled serial link is short and that the TX chip and RX chip can share the same clock source.

3. LC oscillator or ring oscillator

A clock multiplication unit can be implemented as an LC oscillator or a ring oscillator PLL. LC oscillators generate high quality clocks with low power consumption, but the inductor used in this scheme occupies a large area on chip. A ring oscillator PLL occupies moderate area, but the tradeoff between jitter and power results in relatively high power for low jitter generation.[32]

Ring oscillator design was focused on to achieve a small area design.

2.2.4.2 Semi-digital DLL

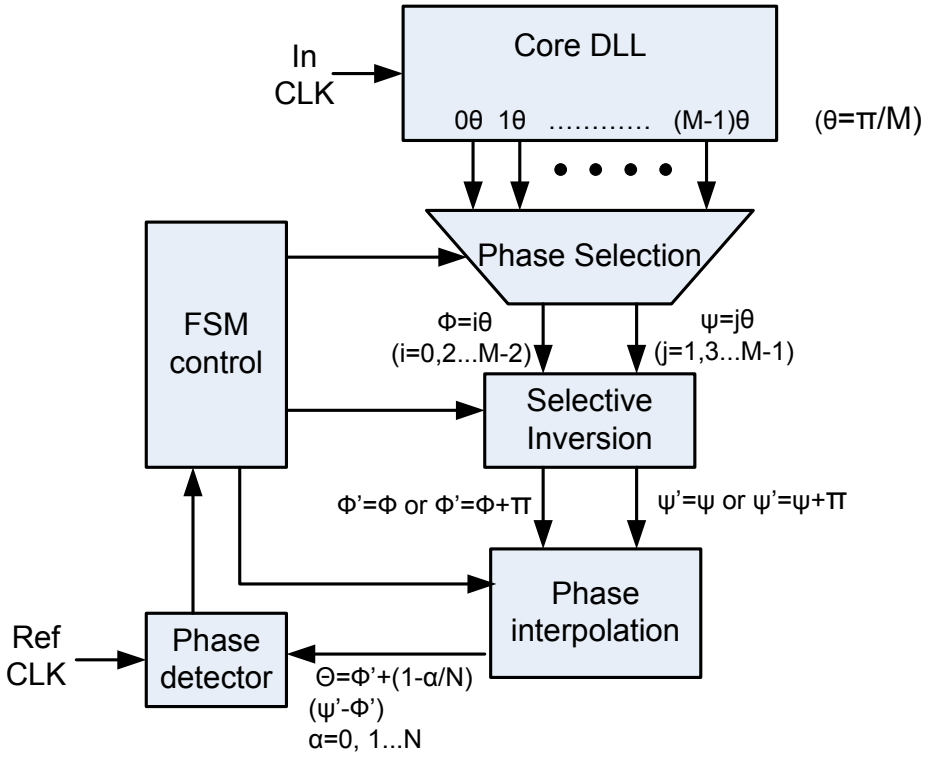


Figure 2.14 Semi-digital Dual Delay-locked loop

The insertion delay from transmitter to receiver includes the delay in circuits and delay on the T-Line. This delay is unpredictable for high speed links with a wide range of data rate variation. A semi-digital DLL presented in [21] can recover unlimited clock phases with various insertion delays and data rates. It is widely used in serial link applications [14][34][35][36]. This clock recovery architecture is shown in Figure 2.14. A core DLL generates M-phase clocks. Two neighboring clocks are selected and selectively inversed depending on the control lines from the finite state machines (FSM). A phase interpolation is operated on these two neighbor clocks based on the weight α from the FSM. The interpolated clock is compared with a reference clock and early/late information is used by the FSM

control unit to generate phase selection and interpolation weight. Phase selection combined with selective inversion covers a seamless 0 to 2π phase range with a phase step of π/M, where M is the multi-phase stages. This π/M phase step is further divided into N stages, which is covered by the phase interpolator, resulting in a final phase step of $\pi/(MN)$.

2.3 Capacitively coupled I/O design

Capacitive coupling has been used extensively in circuit design. It has been used to isolate different common-mode levels [38][40]; to provide frequency compensation [39], etc.

In chip-to-chip links, capacitive coupling is extensively used in the following three applications:

1. To isolate the common mode voltage difference between transmitter and receiver [37][49][54][55].

2. To reject high range of common mode noise at receiver input [50][51].

3. A high density contact-less AC paths instead of physical solder bumps [41]-[47].

Capacitively coupled interconnects have a number of advantages over conventional conductive interconnects [41]-[44], [53]. The main advantages are high pin density, low power, and passive equalization. Previously reported capacitive coupling interconnect schemes and pulse receivers are reviewed in this section.

2.3.1 Capacitively coupled chip-to-chip interconnect scheme

Currently, there are three kinds of applications in capacitive coupling interconnect: 3D-IC, proximity communication and AC coupled interconnect.

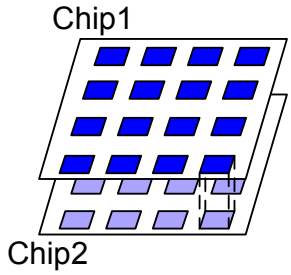


Figure 2.15 capacitive coupling chip-to-chip interconnect scheme 1: 3D-IC

1) Figure 2.15 shows the 3D-IC vertical signal transmission reported in [48] and [45]. Low propagation delay and low power dissipation are achieved by this 3D-IC scheme. In [48], 500MHz data rate is achieved in simulation and 15MHz date rate communication is demonstrated between two vertical chips through a 20um by 20um coupling capacitor (5fF).

In [45], a wireless superconnect with a similar physical structure is demonstrated. An 1.27Gb/s/pin and 3mW/pin vertical chip to chip communication is demonstrated through 20um by 20um coupling capacitor. Low power is achieved in design by using a sense amplifier with receiver side clock, as shown in Figure 2.27**.**

2) Proximity communication [46] is shown in Figure 2.16. In contrast to traditional 3D-IC, chips are only overlapped at the edge in proximity communication system. Given the fact that the capacitive coupling I/O can be built in a 50μm pitch, overlapping only at one edge will bring 200 such I/Os for an 1cm by 1cm chip. With a 1.35Gb/s per I/O speed, that's a 270Gb/s off-chip throughput. The center area of the chip can be used to route the DC signals, including the power supply and some low frequency control signals. A mechanically coarse alignment and an electronic alignment method were used to reduce the residual misalignment to less than 1/8 of the pitch of capacitor plates [47].

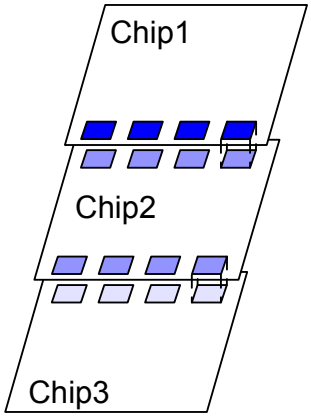


Figure 2.16 Capacitively coupled chip-to-chip interconnect scheme 2: Proximity Communication

3) Multi-chip module (MCM) and ACCI [41][44] are shown in Figure 2.17. In contrast to 3D-IC and proximity communications, the chips in MCM or ACCI don't communicate with other chips directly. In MCM and ACCI, routing on substrate is available and more chips can communicate with each other. Moreover, the pad distribution on the chip surface can be much more flexible.

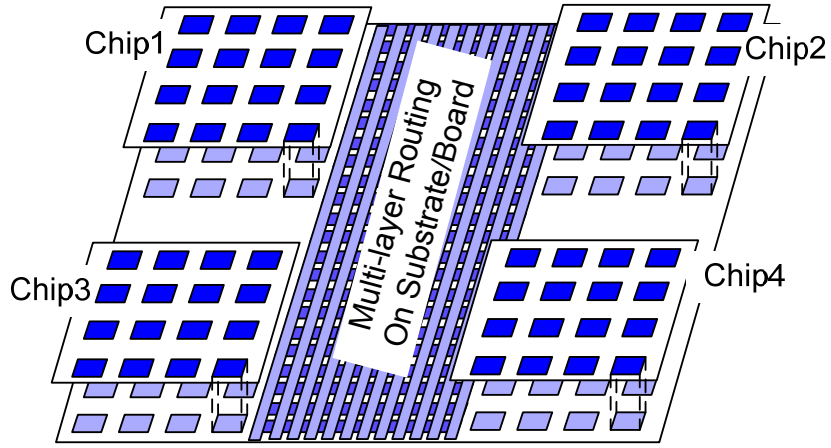


Figure 2.17 Capacitively coupled chip-to-chip interconnect scheme 3: AC coupled interconnect:

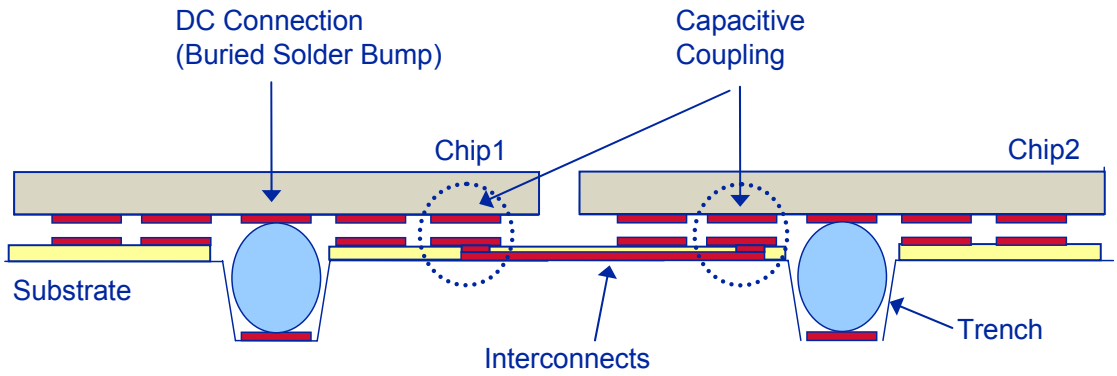


Figure 2.18 AC coupled interconnect with buried solder bumps

A buried solder bump structure for ACCI is further proposed in [41] and shown in Figure 2.18. The buried solder bumps provide DC paths while the coupling capacitors provide AC paths from chips to substrate. The buried structure enables a smaller gap between the substrate and the chips, which is reverse proportional to the coupling capacitance. The buried solder bumps also provide mechanical support and self-alignment [7].

2.3.2 Pulse receivers

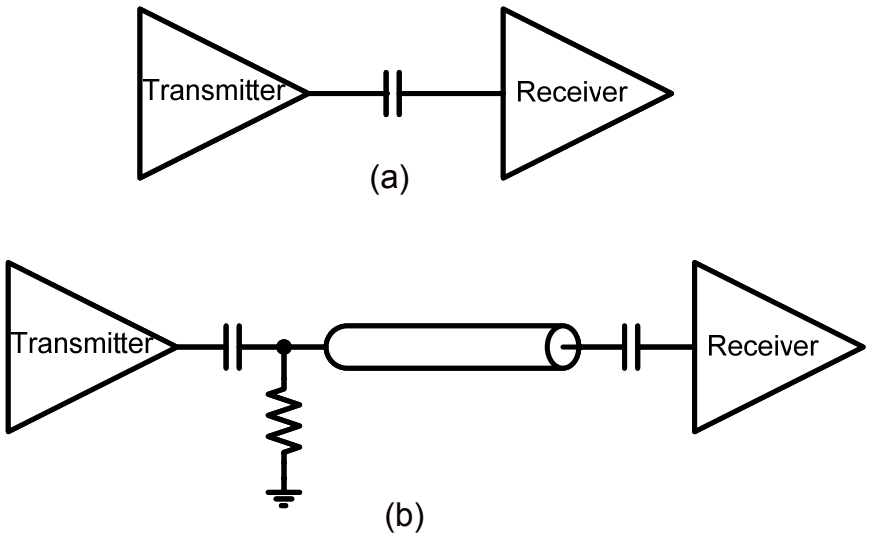


Figure 2.19 Circuit view of capacitive coupling interconnect (a) for 3D-IC and proximity communication in Figure 2.15 and Figure 2.16. (b) for ACCI in Figure 2.17

From a circuit view, 3D-IC and proximity communication are structured as shown in Figure 2.19 (a); while MCM and ACCI share the structure shown in Figure 2.19 (b). Scheme b has much more attenuation than scheme a. For scheme b, a termination resistor is needed at either transmitter side or receiver side or both. Transmitters for both schemes are similar, such as an inverter chain to drive NRZ data. After the coupling capacitor, NRZ data is translated into pulse signals shown as Figure 2.20. The receiver needs to recover the pulses back into NRZ data. Since there is much more attenuation in scheme b, the receiver for scheme b requires better input sensitivity than that of scheme a.

Since the receiver input is isolated by the coupling capacitor, controlling DC wander is one of the challenges faced when designing pulse receivers. Some designs use coding to add data activity to minimize DC wander [37], some circuits can totally remove the DC wander. This section will describe some of the typical pulse receivers reported recently.

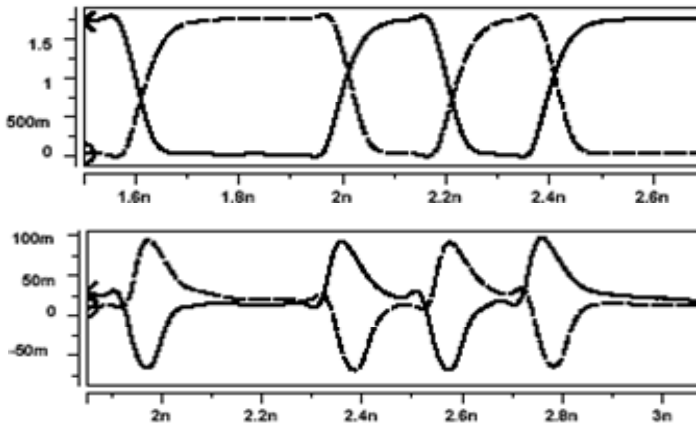


Figure 2.20 Pulse signaling of capactively coupled I/Os

2.3.2.1 Kühn's receiver

Kühn's receiver [48] shown in Figure 2.21 is a typical single ended pulse receiver. The first stage is an inverter with diode-connected feedback to bias the local DC voltage to nearly Vdd/2. The second stage is a latch to recover the pulse signal to NRZ data. An inverter isolates two stages and offers some voltage gain. A similar pulse receiver shown in Figure 2.22 is used in proximity communications [46]. This simplified receiver has a similar structure as Kühn's receiver's latch, but doesn't have the input bias stage. To address this problem, the feedback inverter output was clamped within a range of V_H to V_L, which is set to be about 100mV above and below the switch threshold respectively.

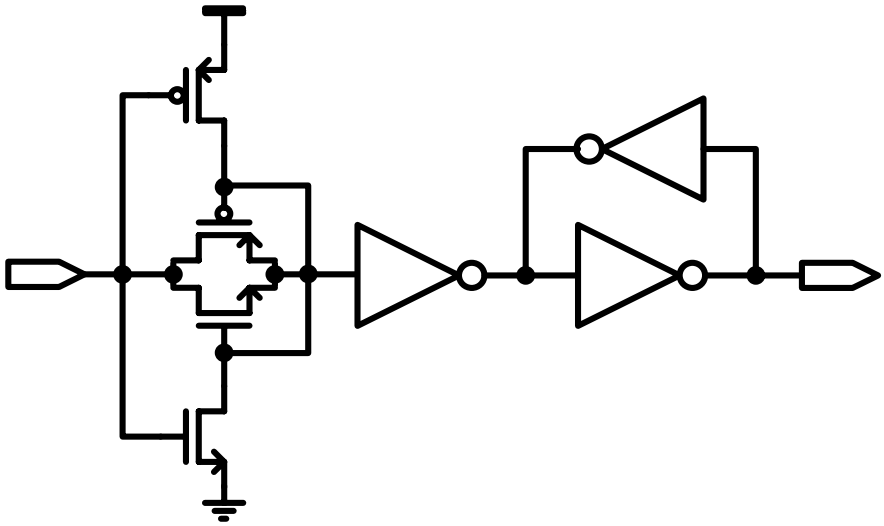


Figure 2.21 Kühn's receiver 1: a self-biased gain stage and a latch structure

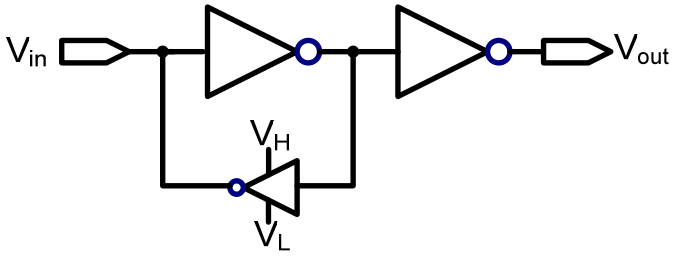


Figure 2.22 Simplified pulse receiver for proximity communications

A comparator with hysteresis [48] is shown in Figure 2.23. MN0, MN1, MN3 and MP0, MP1 are current sources and mirrors. V_{in} is DC biased at V_{ref} through diode-connected MN6 and MN7. A positive/negative pulse will decrease/increase V_p , then turned off/on MN2, thus turn off/on current source MN1, that is decreasing/increasing I_1, then decrease/increase V_p, giving a positive feedback at V_p, so that the output can remain high or low.

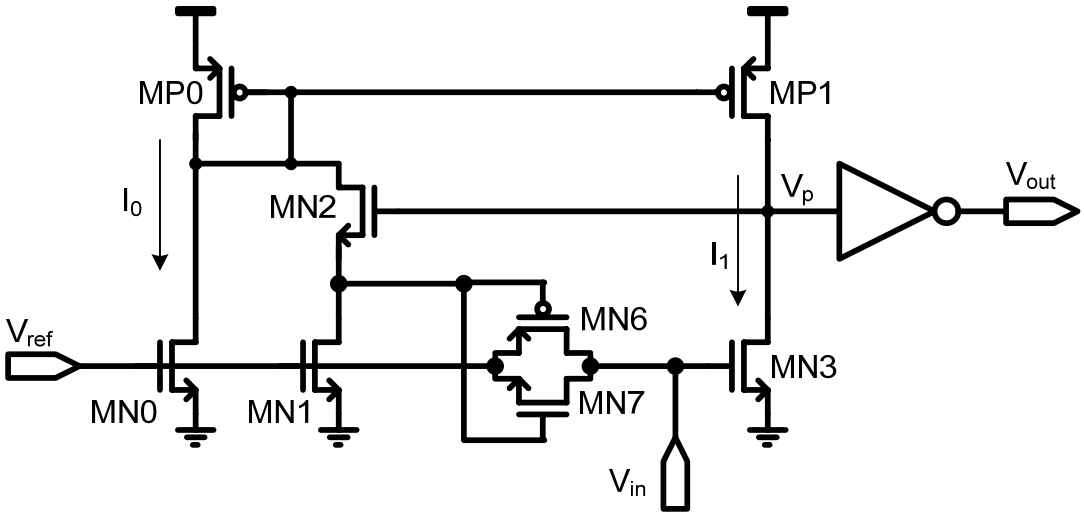


Figure 2.23 Kühn's receiver 2: Comparator with hysteresis

2.3.2.2 Quantized feedback (QF) receiver

The Quantized Feedback (QF) receiver is a differential pulse receiver [49]. As shown in Figure 2.24, input signals "in" and "inb" are differential NRZ data. After the coupling

capacitors, the signals have lost most of their DC components. The two inverters are the positive feedback path, which gives QF to compensate the low frequency insertion loss due to C_1 and C_2. MN_3 and MN_4 are clamping devices to make sure the voltage swing between Vout and V_2 remains within a desired range. Cross coupled PMOS (MP_1 and MP_2) are latch load, which further latches the detected edge of the signal at V_1 and V_2. The input pulse swing requirement is $1V_{pp}$.

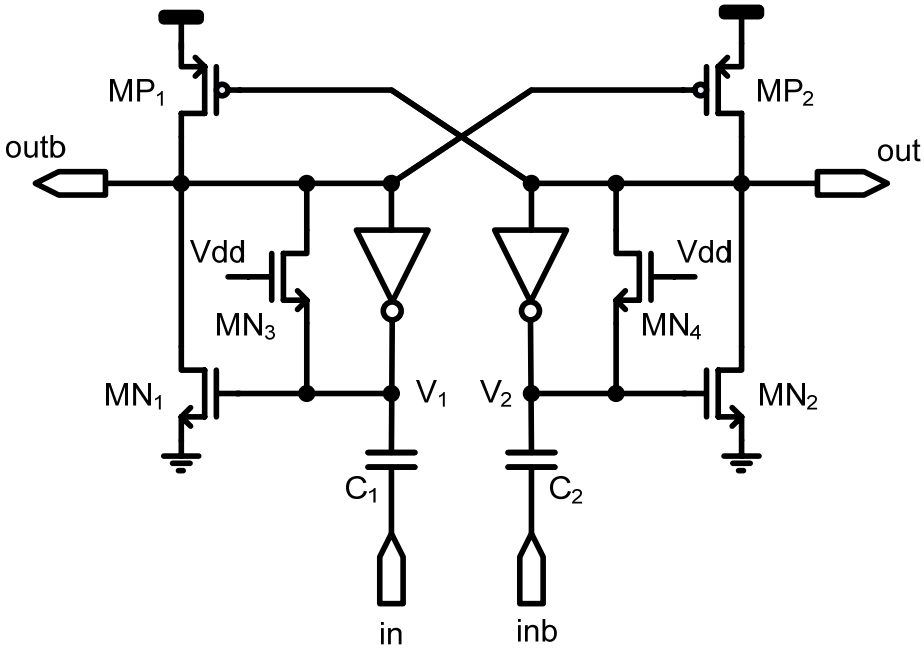


Figure 2.24 Balanced self-clocked CMOS quantized feedback circuit

2.3.2.3 Maillard's pulse receiver

Maillard's pulse receiver [50] is shown in Figure 2.25. Combined with capacitive coupling and common-mode (CM) dimmer, the QF receiver is able to recover 125Mb/s differential pulse signals with 100V/μs CM noise. The first stage is a CM dimmer, equal i_{cmc} currents are provided by current mirrors which reject the rising/falling CM edges and hold Vp and Vn

within the good input range of QF circuit. The second stage is a QF circuit similar to [49]. A similar pulse receiver in BiCMOS process [51] presents an 8Gb/s RX with DC input range of $\pm 690V$ and CM edge rejection with up to 4V/ns steepness.

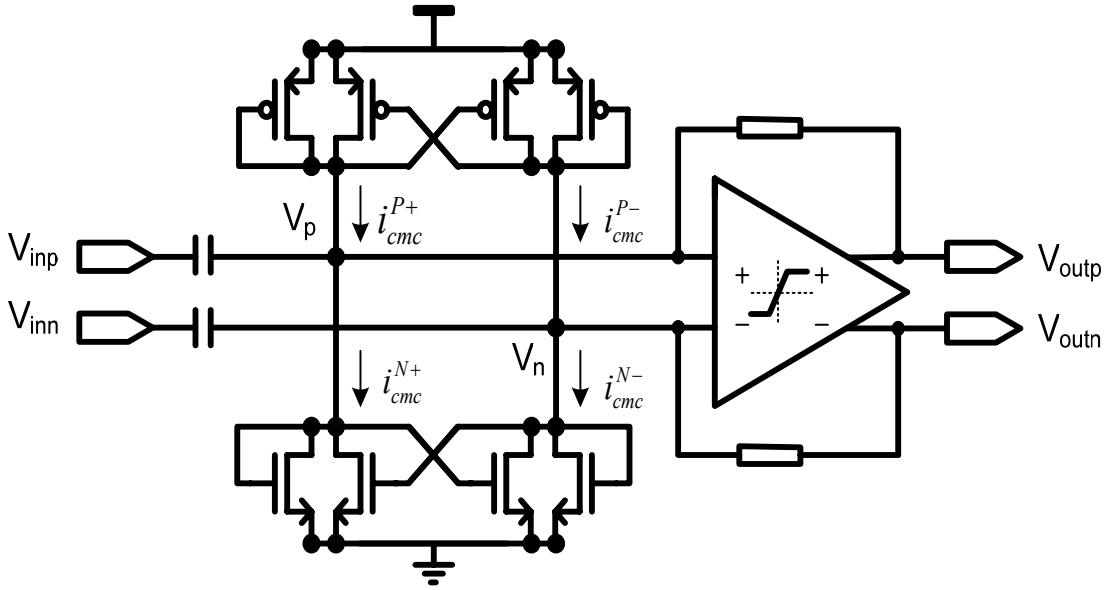


Figure 2.25 Mailland pulse receiver: CM dimmer followed by QF

2.3.2.4 Knight's pulse receiver

A differential pulse receiver [42] is shown in Figure 2.26. This is a push/pull circuit using a set of four identical inverters. Two inverters were used in a flip flop configuration, with opposite sides driven by the two AC coupled inputs. Each output also drove identical inverters as loads. The two inputs were resistively shorted with a turned-on N device "resistor" whose size was adjusted to set the maximum swing of the flip flop nodes. Since all inverters were identical, the small swings were accurately sensed by the output inverters, even under high power supply variation.

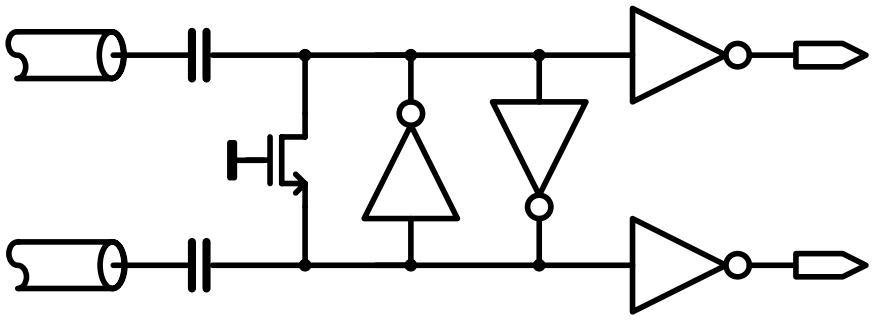


Figure 2.26 Knight's differential pulse receiver

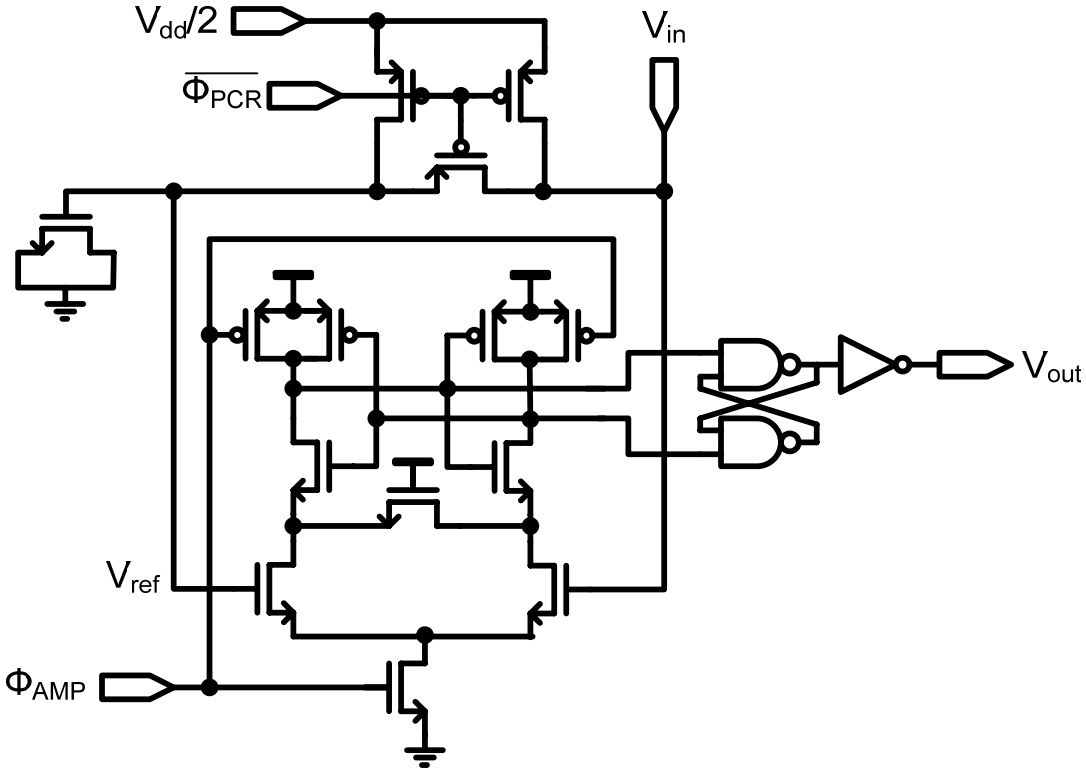


Figure 2.27 Superconnect pulse receiver: sense amplifier with manually adjusted receiver side clock to achieve low power

2.3.2.5 Superconnect pulse receiver

Unlike previous pulse receivers, the receiver [45] in Figure 2.27 needs several manually adjusted clocks for the sense amplifier. V_{ref} and V_{in} are pre-charged to $V_{dd}/2$ at $\overline{\Phi_{PCR}}$ and evaluated at Φ_{AMP}. The latch load of sense amplifier and the F/F output stage samples the pulse signal and recovered into NRZ data. Power consumption is saved by removing the auto bias circuit and taking advantage of externally adjustable clocks.

2.3.3 Other capacitively coupled I/O applications

A capacitively coupled CMOS (C^3MOS) [53] is shown in Figure 2.28. In contrast to previous capacitive coupling I/O, C^3MOS has a transmission line but only one coupling capacitor at the transmitter side. The goal of C^3MOS is to generate pulse signals using this coupling capacitor to reduce power dissipation on the transmission line. Instead of charging the entire line, small pulses associated with small current packages are launched on the line. The total charge or power dissipation is much smaller than that required to charge the entire line in the traditional NRZ signaling.

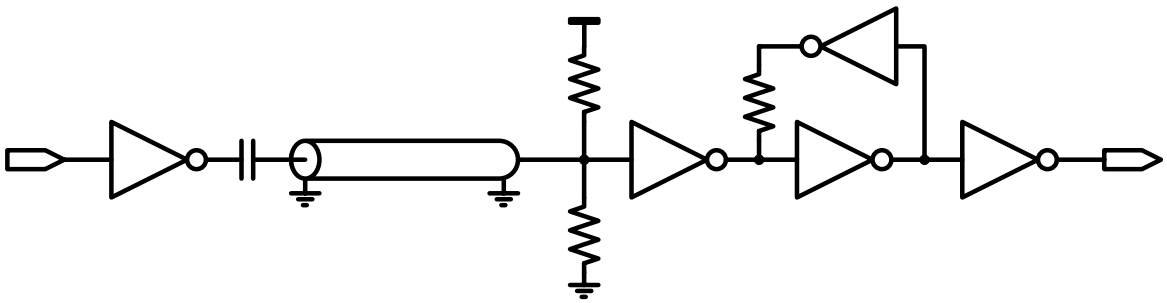


Figure 2.28 Capacitively coupled CMOS(C^3MOS) line driver/receiver configuration

2.3.4 Summary of capacitive coupling I/Os

The following is an explanation of different capacitive coupling schemes. 3D-IC and proximity communication use one coupling capacitor to achieve direct chip to chip communication, which has low latency and is applicable for CPU and memory communication. The two overlapped chips need to have exactly the same pad distribution to achieve vertical communication, which is sometimes difficult to achieve. ACCI and MCM have two coupling capacitors and allow routing between dozens of chips. This is applicable for high speed communications among more chips, and pad distribution on the chips are much more flexible. Table 2.2 gives a brief summary of capacitive coupling schemes.

Technique	References	Objectives	Comments	Applications
3D-IC	[45][48]	High density, low latency	Limited to two chips	Processor to memory bus
Proximity Communication	[46]	High density, low latency	Fixed chip pad distribution, communicates up to 4 chips	Processor to memory bus, multi-CPU communication
ACCI on MCM	[41][44]	High density I/O with short range routing	Enables dozens of chips with flexible pad distribution	multi-CPU communication
C^3MOS	[53]	Generate impulse signals	Reduce power dissipation on lines	Low power interconnect

Table 2.2 Summary of Capacitively coupled I/O scheme

Most of the pulse receivers can be used with the capacitive coupling schemes. The performance matrix to evaluate these pulse receivers are power supply, input sensitivity, jitter performance and sensitivity to power supply noise and PVT corners. Table 2.3 gives a brief summary on these pulse receivers.

Pulse RX	References	Description	Comments
Kühn's receiver 1	[41][48]	a self-biased gain stage and a latch structure	High speed
Simple latch	[46]	Two inverters in a flip-flop configuration	Simple but require careful design on feedback inv to get proper DC bias
Kühn's receiver 2	[48]	Resistive bias and current switching latch	Lower power without self-bias
Quantized Feedback	[49]	A differential scheme using quantized feedback to compensate DC loss	Low input swing requirement
Maillard's receiver	[50][51]	Current mirrors followed by quantized feedback	Good Common-mode rejection
Knight's 4-INV	[52]	Four-inverter scheme, two as latch, two as buffers	Simple and easy match
Clocked sense amp	[45]	Pre-charge to bias and evaluate with help of clock	Low power, need precisely aligned clocks

Table 2.3 Summary of pulse receiver

Chapter 3 ACCI Pulse Signaling

3.1 Introduction

Technology scaling demands high density and low power off-chip input/output (I/O). The ITRS predicts the need for 110μm pad pitch for cost-performance area array flip-chip applications for year 2008 [66]. This pitch requirement is difficult to achieve with available technologies. Recently, several technologies have been reported using capacitive coupling to replace physical pin/solder bumps for high density, low power chip-to-chip communications [48][49][67][68]. This is based on the fact that non-contacting AC connections can be built more densely than DC connections and the AC component actually carries all the information of a digital signal. Instead of using traditional bonding wires as the DC connections at edge of chips, in ACCI, the buried solder bump technology provides a solution for both high-density signal I/O and power/ground pin distribution [6].

In contrast to most of the recent results focusing on stacked ICs [45][46][48], the work presented here, ACCI, is optimized for lossy, board-level, capacitively-coupled interconnect. This work enables long distance communication among multiple chips, while retaining the high-density and low-power properties of capacitive coupling. ACCI can not only satisfy the increasing demand for high-density signal I/Os, but also saves precious chip area for more Vdd/Gnd pins to improve power system signal integrity.

In this chapter, the unique band-pass channel response and equalization scheme of the ACCI channel are discussed and compared with traditional low pass response of a T-Line channel. Coupling capacitor and T-Line design rules and design margins are discussed. A voltage mode driver is used for the ACCI channel and saves more than 70% power, when compared to a traditional current-mode driver with conductive signaling. Interconnect power dissipation is minimized by using low swing pulse signaling. For receiver design, previous CMOS single-ended [6][45][67] and differential [49] pulse receivers are reported with more than 200mV$_{pp}$ input swing when scaled to 0.18μm technology, as shown in Figure 3.1. In this work, a 3Gb/s differential pulse receiver requiring only 120mV$_{pp}$ input swing is proposed. The three times reduction of input swing made possible by this receiver enables ACCI with five times smaller coupling capacitance which translates to five times higher I/O density, and signal across longer T-Lines than previous work [6].

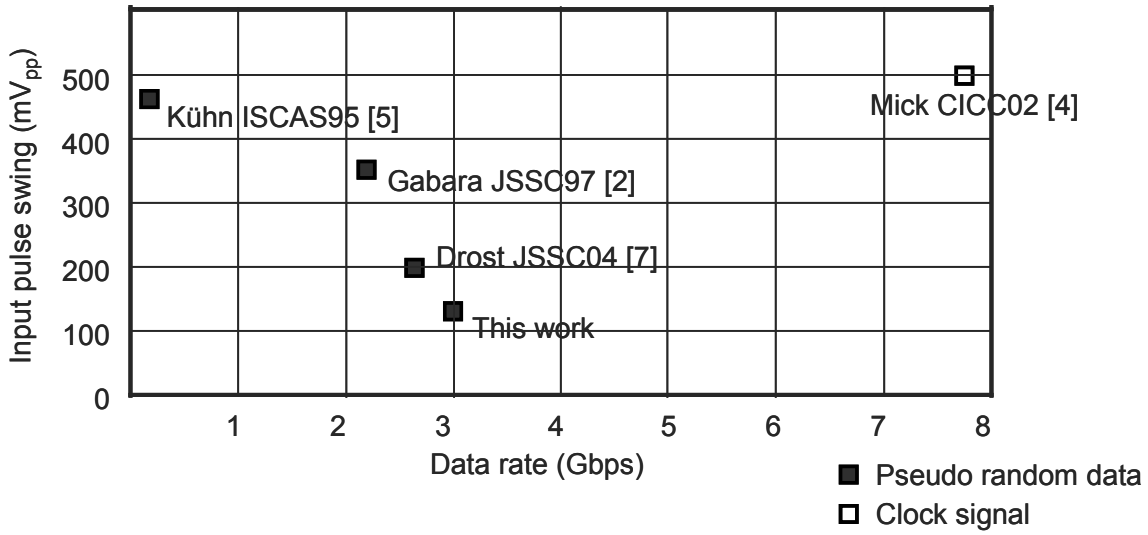


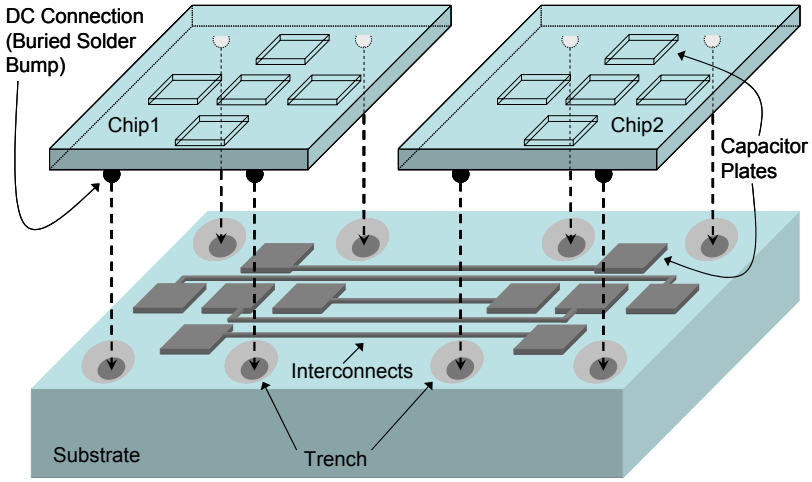
Figure 3.1: Comparison with previous CMOS high speed pulse receivers. (All scaled to 0.18μm. To be on the same base line, single ended Vpp is used for single ended pulse receivers in [6][45][67]; differential Vppd is used for differential pulse receivers in [49] and in this work.).

Chip-to-chip communication at 3Gb/s is demonstrated through two 150fF coupling capacitors across a 15 cm FR4 microstrip line. On the test chip, the pulse receiver converts pulses into non-return-to-zero (NRZ) data without a clock signal; then a semidigital dual DLL successfully recovers receiver side clock phase from the recovered NRZ data. An on-chip BER tester indicates a BER less than 10^{-12} through one ACCI channel at 3Gb/s. Given the density made possible by ACCI with this pulse receiver, the ITRS milestone of 110μm pad pitch can be achieved.

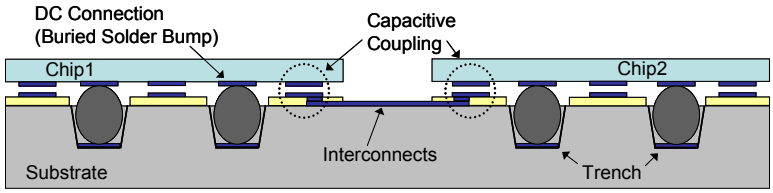
Section2 describes the ACCI physical structure and the corresponding channel response. Section3 discusses pulse signaling in ACCI and its equalization scheme. Section4 presents the ACCI transceiver circuit details. Section5 gives noise simulation and analysis.

3.2 AC Coupled Interconnect

3.2.1 Physical Structure



(a)



(b)

Figure 3.2: ACCI physical structure (a) top-down view, (b) cross-section view

The top-down and cross-section view of ACCI are shown in Figure 3.2. The key concept here is that DC connections are not needed to convey the high frequency content of AC signals. Instead, the information in these signals can be transported by AC connections, such as a series capacitor. The advantage of AC connections is that circuit design considerations can be made the limiting factor to achieving high I/O density rather than physical limitations such as the manufacturability of dense arrays of sub-100μm solder bumps [71].

The buried solder bump has two purposes. First, the solder bumps provide evenly distributed DC connections (e.g. for power, ground and bias signals) across the interface with normal size solder bumps. Second, the buried solder bumps provide a means to self-align the chip and package surfaces while maintaining a close, controlled proximity between corresponding capacitor plates [6]. In this way, evenly distributed AC and DC paths are simultaneously created across the same interface between chip and package (though a MCM is shown, it can be used for conventional packaging). Although capacitive coupling is demonstrated here, inductive coupling is an alternative implementation for ACCI.

3.2.2 Channel Response

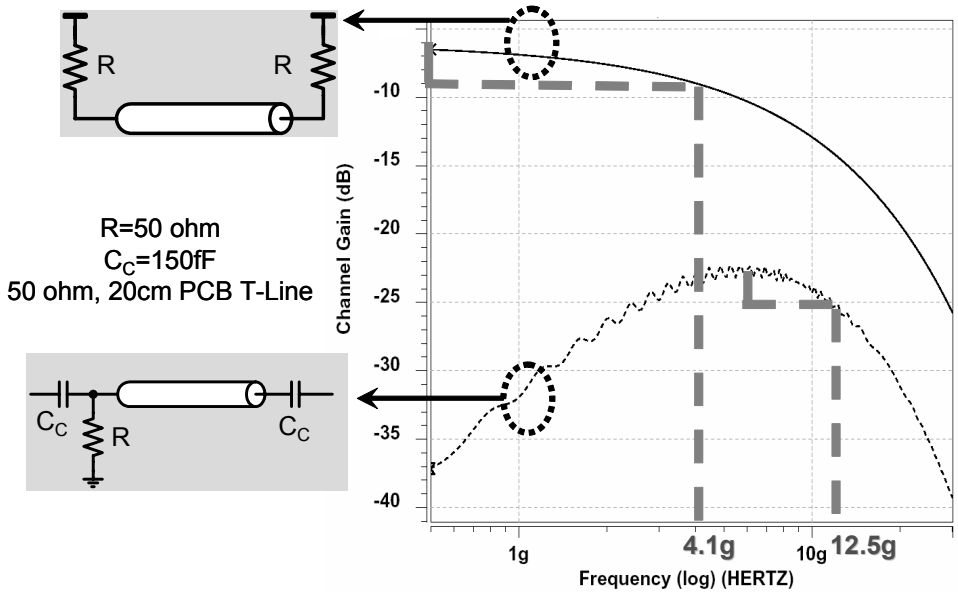


Figure 3.3: Channel response of a T-Line channel (solid curve) and an ACCI channel (dotted curve)

As shown in Figure 3.3, instead of the low pass channel response of a traditional T-Line, in ACCI, the combination of serial coupling capacitors, parasitic capacitors and the T-Line create a channel from transmitter (TX) to receiver (RX) with a band-pass response. The T-

Line and parasitic capacitors define the low-pass characteristics while the coupling capacitors define the high-pass characteristics of the ACCI channel response. The series coupling capacitors filter out the low frequency components of transmitted data, thereby, reducing ISI and effectively extend channel bandwidth to higher frequencies. For example, the 3dB bandwidth of the ACCI circuit shown in Figure 3.3 is three times larger (12.5GHz versus 4.1GHz) when compared with a traditional channel having the same T-Line length. However, low frequency attenuation needs to be compensated through equalization and this will be addressed in section 3. It should be noted that there is a need to increase sensitivity of the receivers due to the broad approximate 20dB loss for the ACCI channel compared to the conventional conductive channel.

3.2.3 Impedance match at transmitter side

To minimize reflections, either or both sides of the transmission line should be impedance matched. Terminating at the transmitter side reduces reflections and allows the receiver side to remain high impedance which in turn provides for voltage doubling as a transmitted pulse encounters the high impedance receiver. As shown in Figure 3.6(b), although there is about 6db attenuation on T-Line, the signal swing at far end T-Line is about same as that at near end T-Line due to this voltage doubling. When compared with terminating only at the receiver side, transmitter side termination will lead to a smaller pulse swing on the T-Line, which causes less crosstalk noise to neighboring lines.

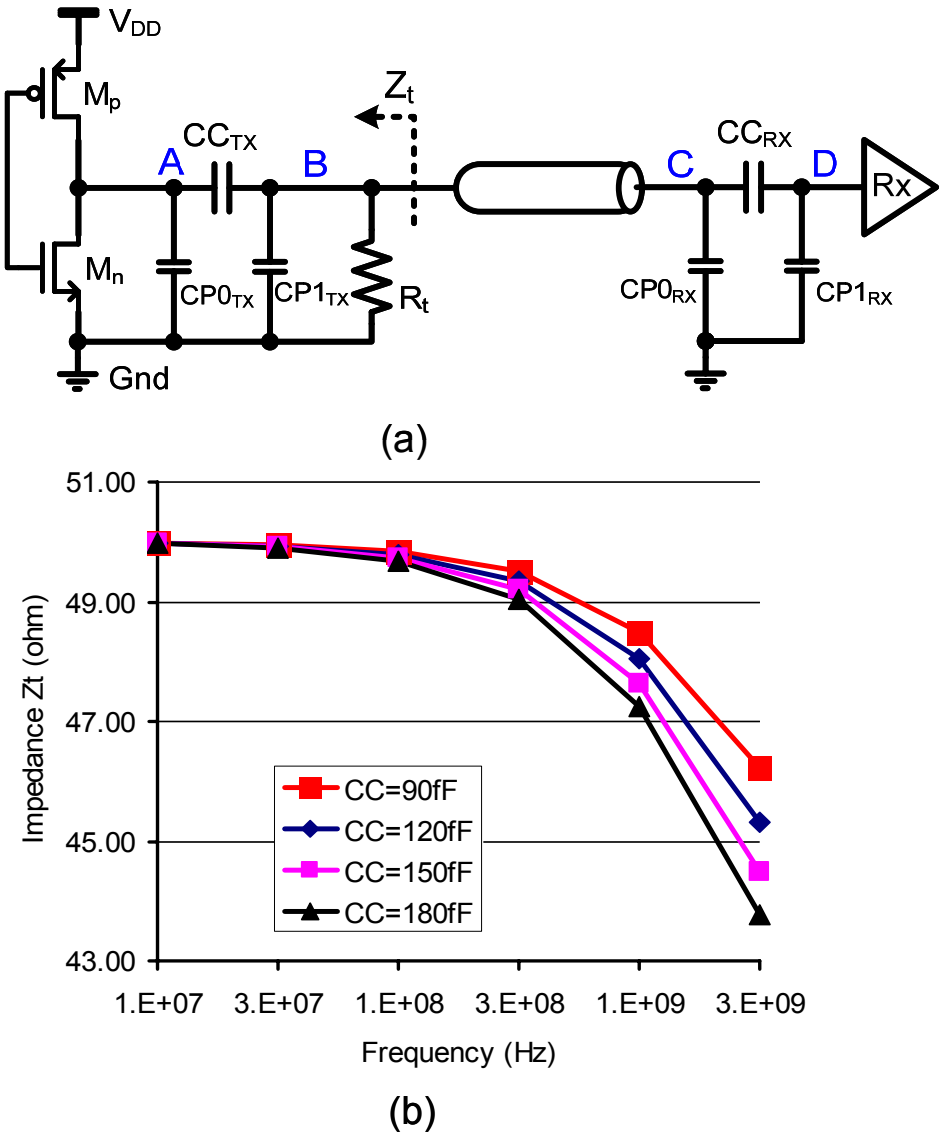


Figure 3.4: (a) Transmitter side termination scheme. (b) Impedance looking back from T-Line to coupling capacitor and transmitter

Figure 3.4 (a) shows the termination scheme, where M_p and M_n form the output stage of the transmitter, CC is the coupling capacitor, CP0 and CP1 are the parasitic capacitance and R_t is the 50 Ω termination resistor. Figure 3.4 (b) shows Z_t, the impedance looking back from transmission line to coupling capacitor and transmitter. As long as Z_t equals 50 Ω, the

backward wave reflected from receiver side is terminated at the driver side and thus no further reflections are generated. This is proved in the simulation waveforms in Figure 3.6 (b). There is reflection noise at near end T-Line due to the backward reflection at un-terminated far end T-Line. This backward reflection noise is absorbed by the near end termination resistor and thus no further forward reflection noise shown at far end T-Line. The driver output impedance is isolated by the coupling capacitor and thus does not have to be 50 Ω. Z_t is equal to R_t at low frequencies. Though at higher frequencies, the parasitic and coupling capacitors reduce Z_t, the impedance still matches well across a wide range of coupling capacitor values.

3.2.4 Pulse swing

Larger pulse signal swing at receiver input is preferred for higher signal-to-noise ratio (SNR) and lower BER. It is the driver side coupling capacitor that translates the NRZ signals into RZ pulse signals. The swing of pulse signal is largely related to edge rate of the NRZ signal. Figure 3.5 shows the simulated waveforms based on the setup in Figure 3.4 (a), with a lossless T-Line. The four series of waveforms represent the signals at node A, B, C and D, as noted in Figure 3.4. Four kinds of NRZ signals are simulated, as noted as 1, 2, 3 and 4 on each individual waveform. Signal1 has the fastest NRZ edge rate and thus largest pulse swing at receiver input. Although signal2 has twice of NRZ swing than that of signal3, they generate similar pulse swings. This is because signal2 and signal3 have the same edge rate. This clearly shows the NRZ edge rate is much more important than NRZ pulse swing to generate a larger pulse swing. Larger NRZ swing actually results in longer NRZ transition

time and thus longer pulse width, which could bring ISI. Signal4 has the slowest edge rate and thus smallest pulse swing at receiver side.

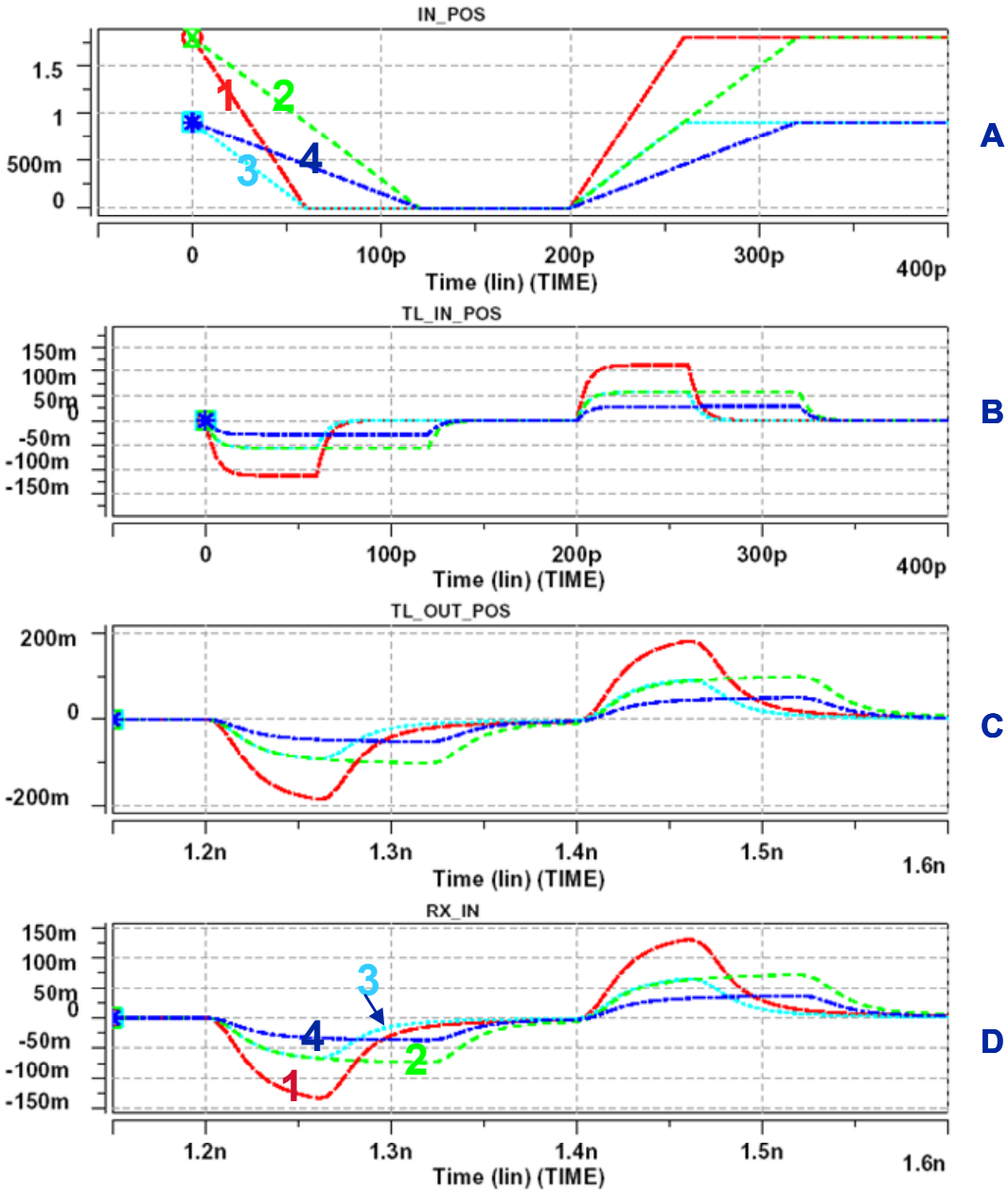


Figure 3.5: Pulse swing depends on edge rate of NRZ signal at driver output

To summarize, the edge rate of the driver output NRZ signal determines the pulse swing while the transition time of the NRZ signal determines the pulse width (neglect the low pass effect of T-Line at this point). Fast edge rate and short NRZ transition time are preferred. This helps to define the best driver for ACCI. Note that infinite edge rate is not preferred due to the switching noise it will cause. So the design trade-off here is among pulse swing, ISI and switching noise.

3.3 Pulse Signaling

3.3.1 Pulse Signaling on ACCI

In contrast to NRZ signaling, pulse signaling has been used to reduce power consumption on interconnect by only dissipating dynamic power [6][53][68]. The band-pass characteristic of the ACCI channel produces return-to-zero pulse signaling, which minimize the power dissipation in the ACCI channel. Figure 3.6 shows the ACCI circuit overview and the transient waveforms at the nodes associated with pulse signaling and pulse receiver.

In Figure 3.6, CC are the coupling capacitors and CP are the parasitic capacitors. Driver side termination is used here, although receiver side termination is another option. The first two waveforms are time shifted 1ns to compensate part of the delay on T-Line. A pseudo-differential driver outputs full-swing, high edge rate NRZ data; the first coupling capacitor with T-Line load acts like a differentiator, converting the data into return-to-zero (RZ) pulses at the data transitions. With the two coupling capacitors isolating the DC levels, the RZ pulses on T-Line have a DC level of zero. The pulse receiver auto-generates the DC level at RX input, amplifies the incoming small pulses and converts them back into NRZ data.

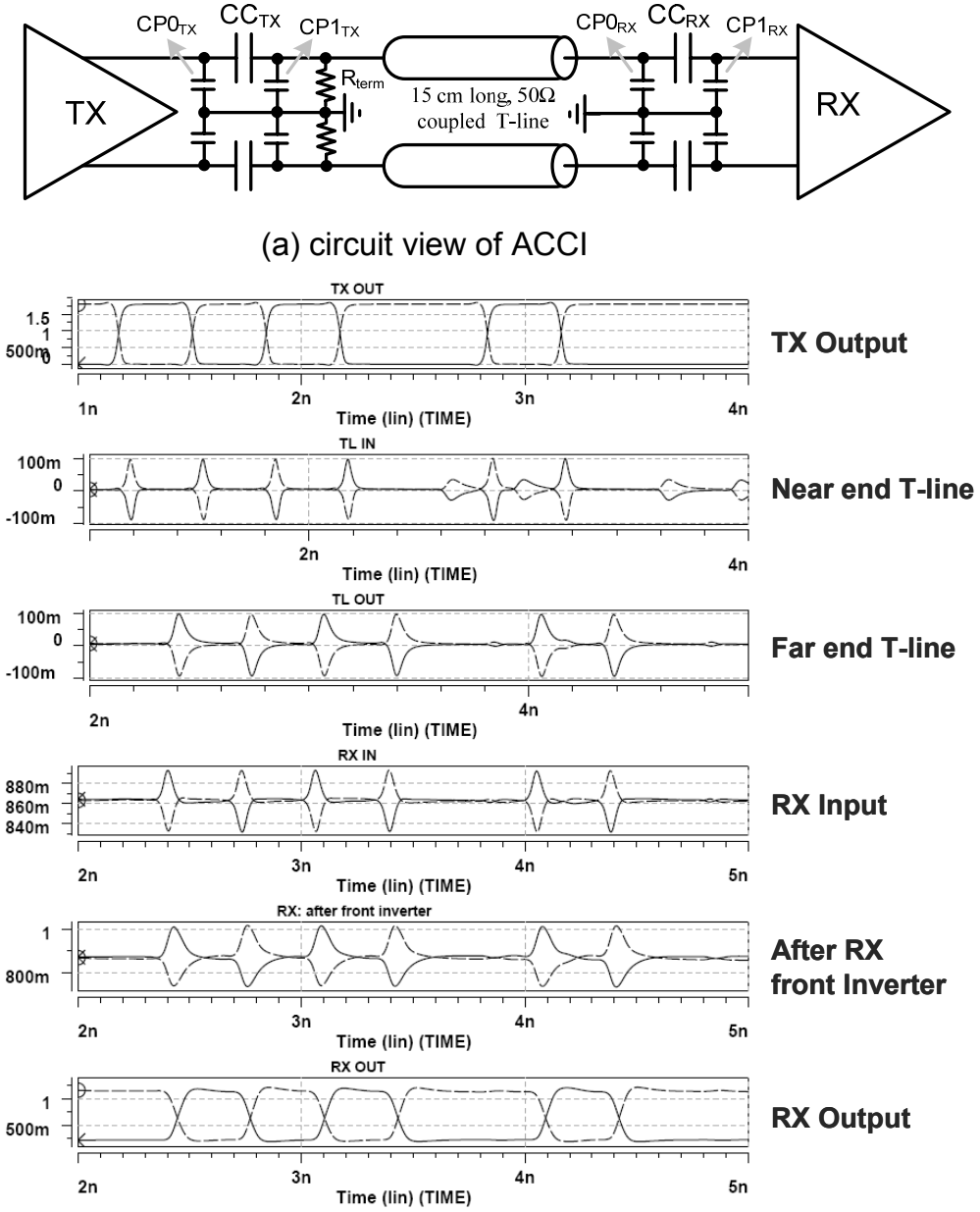


Figure 3.6: Circuit view and transient waveforms of ACCI

When compared with stacked ICs [45][48][67], ACCI has a long T-Line and an additional serial coupling capacitor which produces both broad-band and high-frequency channel loss. These additional elements allow the benefits of capacitive coupling to be extended to

scenarios requiring long-range chip-to-chip communication, but it introduces the need for a more sensitive pulse receiver for ACCI.

3.3.2 Equalization for pulse signaling in ACCI

The band-pass characteristic of an ACCI channel uses a different equalization scheme than that used with traditional T-Line channels. High frequency compensation used in traditional T-Line channels is not required in ACCI because the 3dB bandwidth is already extended by three times, as shown in Figure 3.3. However, low frequency compensation is necessary.

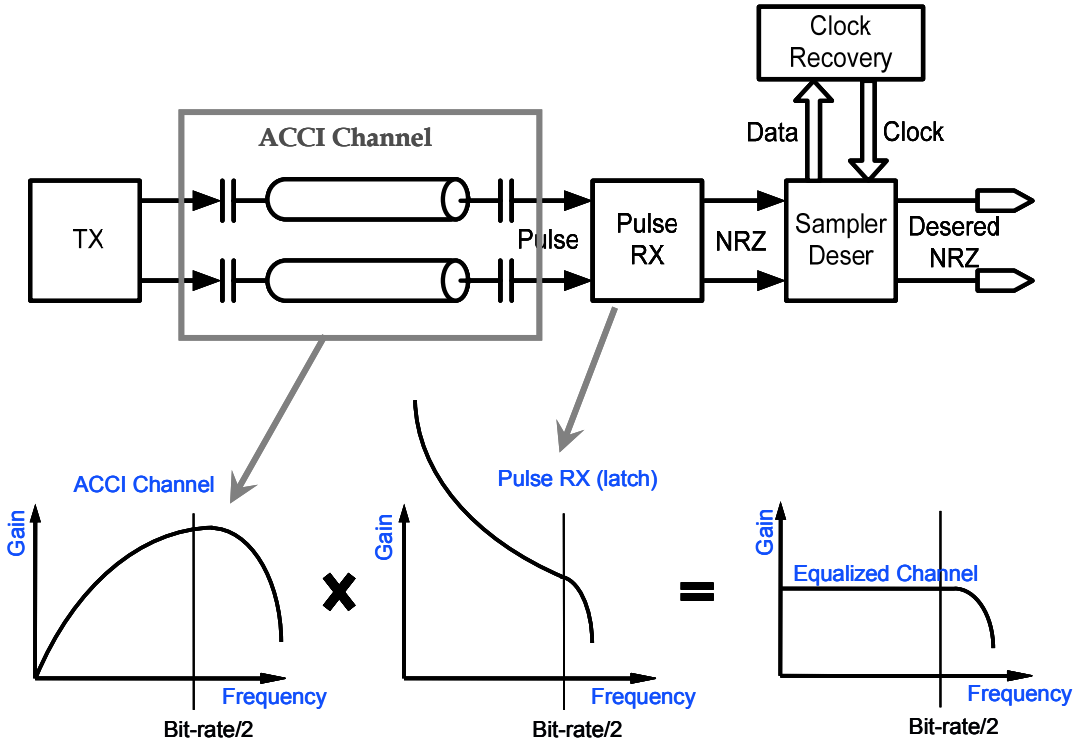


Figure 3.7: Frequency domain equalization scheme for pulse signaling in ACCI

In the frequency domain, as shown in Figure 3.7, the pulse receiver is essentially a latch or edge detector, and is used to compensate for the low frequency loss and ensures a near flat channel response before the sampler. The latch detects and captures pulses, and then remains

stable until it detects the next opposite polarity pulse regardless of the bit period, thereby, implementing an adaptive low frequency compensator.

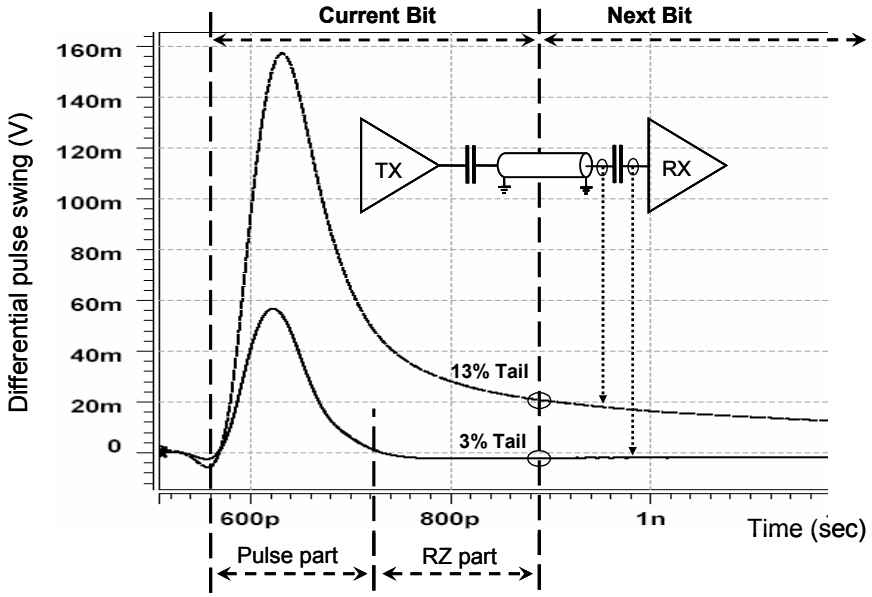


Figure 3.8: Coupling capacitors provide passive high frequency compensation in time domain. The ISI is 3% at the RX input.

The receiver is able to restore the attenuated low frequency information as long as the pulse data rate is less than the latch bandwidth. The low frequency compensation dynamically adapts to the changes in pulse width caused by the T-Line and coupling capacitor variations, since the information is stored in the edge and its polarity. Furthermore, as long as the NRZ signal edge rate fits in the pass band of the ACCI channel, any digital signal can pass the ACCI channel and be recovered by the pulse receiver. Theoretically, this corresponds to a digital signal with a data rate approaching DC. This also explains how the latch-based pulse receiver can recover long sequences of consecutive “1”s or “0”s.

Figure 3.8 shows, in the time domain, how ACCI extends the bandwidth in the high frequency range. A step input to the channel results in a pulse signal on the T-Line, and at the receiver input. The T-Line has a low-pass response due to the skin effect and dielectric loss, resulting in a long tail on the pulse signal. Without equalization, this tail would cause inter-symbol-interference (ISI) and reduce the timing margin at the receiver. The second coupling capacitor de-emphasizes the low frequency components by filtering the long pulse tail, thereby, reducing energy that interferes with adjacent pulses. This inherent passive behavior allows ACCI to save chip area and power dissipation typically associated with active high frequency compensation.

3.3.3 Valid range of coupling capacitor sizes and T-Line Lengths

The coupling capacitors and T-Line parameters define the ACCI channel response and thus the pulse swing and width at the receiver. For a given data rate and pulse receiver input sensitivity, there are a range of coupling capacitor sizes and T-Line lengths, within which a pulse receiver is able to recover the NRZ data.

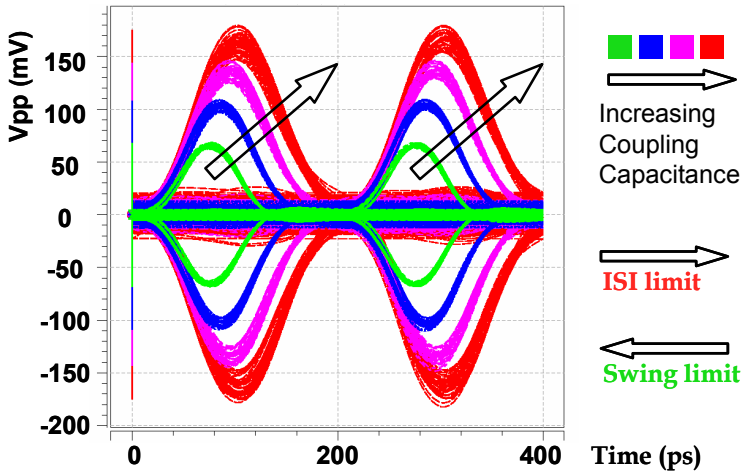


Figure 3.9: Differential pulse eye diagrams with increasing coupling capacitances

Figure 3.9 shows the differential pulse eye diagram after the second coupling capacitance (i.e. at the input of the receiver). The arrows show the trend resulting from increasing the coupling capacitor size. Larger coupling capacitors will increase the peak-to-peak pulse swing and overall pulse duration. The increased swing relaxes the constraint on the receiver input sensitivity, but the increased pulse width may introduce ISI. The use of a smaller coupling capacitance provides more efficient filtering of the pulse signal tail and reduces ISI, but the corresponding reduction in signal swing increases the input sensitivity requirement for the pulse receiver. Therefore, the maximum coupling capacitance is constrained by the ISI limit, or the data period limit; while the minimum coupling capacitance is constrained by the swing limit, or pulse receiver input sensitivity. (This simple explanation ignores noise in the system. A discussion of noise related issues is covered in a later section.)

Similarly, the T-Line also affects channel response and pulse shape. Longer T-Lines result in more attenuation, especially high frequency attenuation. This not only extends pulse width (increasing ISI) but also limits pulse swing. Thus, the maximum T-Line length is constrained by both the ISI limit and swing limit.

As long as signal-to-noise ratio (SNR) allows, it is desirable to have a low-swing pulse receiver. This enables performance increases in following ways: higher I/O density (from the use of smaller coupling capacitors), longer T-Lines lengths, the relaxation of the ISI constraint, and an increase in the data rate.

3.4 Implementation

3.4.1 Driver design

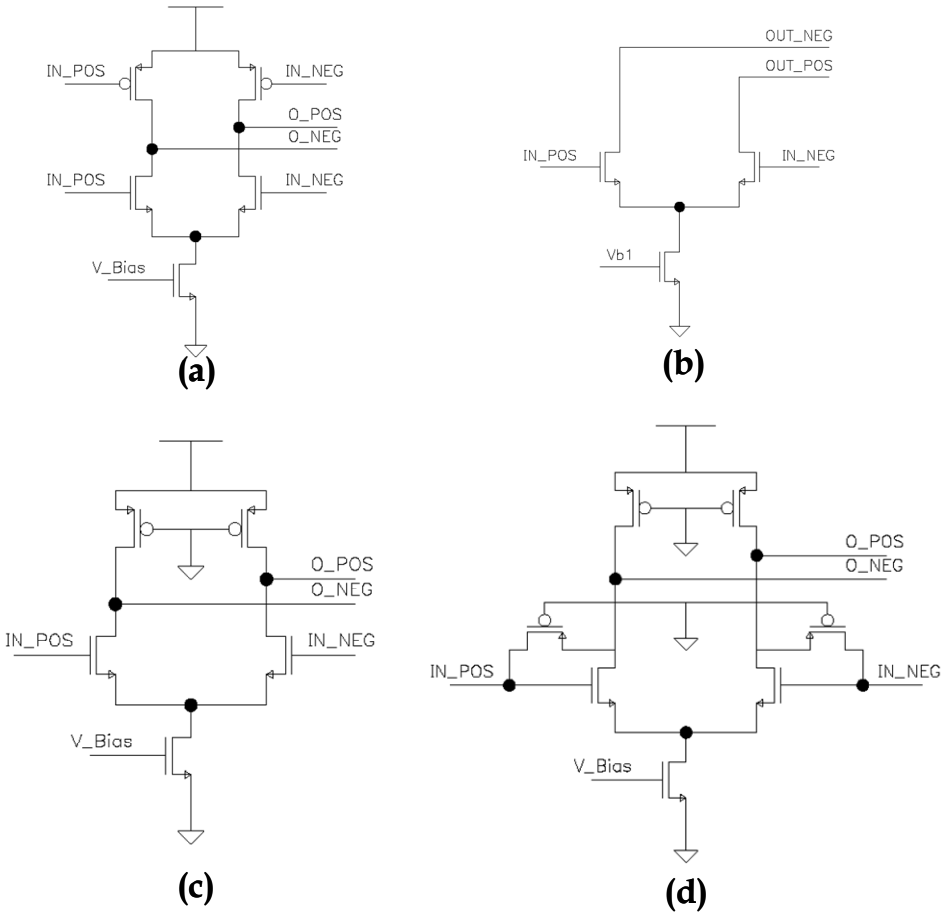


Figure 3.10: Candidates for high speed output drivers: (a) H-bridge with tail current; (b) Current-mode driver; (c) MOS Current-mode Logic (MCML) Inverters [69]; (d) MCML Inverters with feedback to compensate V_{th} variations [70]

The driver needs to generate high edge rate to signal through the ACCI channel. Balanced rising/falling edges are also required so that the positive and negative pulses are symmetric. Figure 3.10 shows a few candidate differential drivers. When driving an ACCI channel, differential current-mode drivers have the disadvantages of slower edge rates and higher

power dissipation. The ACCI channel has high input impedance and making it more appropriate to use a voltage mode driver.

3.4.2 Voltage Mode Driver

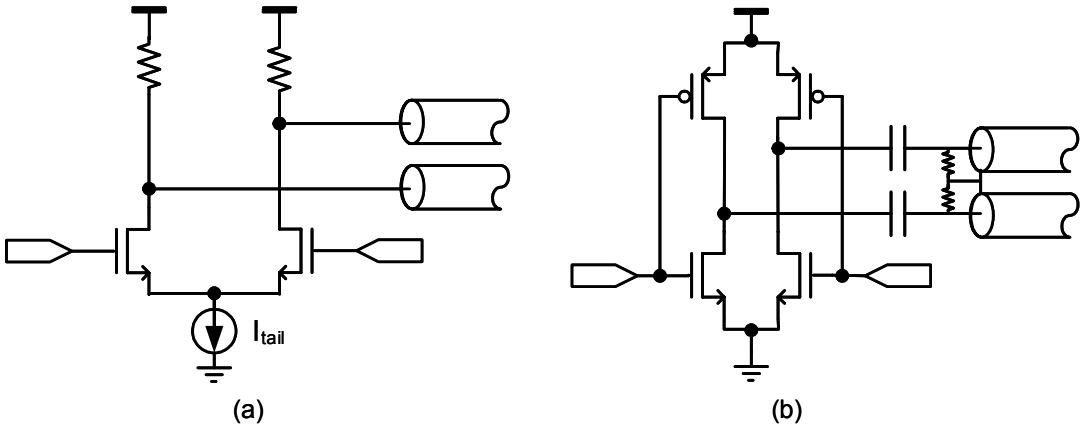


Figure 3.11: (a) Current-mode driver, (b) voltage mode driver

High-speed serial-link transceiver circuits typically use a current-mode driver as shown in Figure 3.11 (a) [1], but ACCI enables the use of a voltage mode driver as shown in Figure 3.11(b). There are three reasons why a voltage-mode driver, such as a complementary inverter pair, is the best choice for ACCI. First, as show in Figure 3.4(a), return impedance matching at the driver side is already provided by the parallel termination, and since the driver is isolated by the driver-side coupling capacitor it is not necessary to use a 50 Ω driver to match the T-Line impedance. Secondly, the input impedance of the ACCI channel is high and more easily driven by a voltage mode driver. Finally, severe channel loss and the high frequency pass-band channel characteristic requires a full swing and high edge rate driver output, which is only possible by using a voltage mode driver.

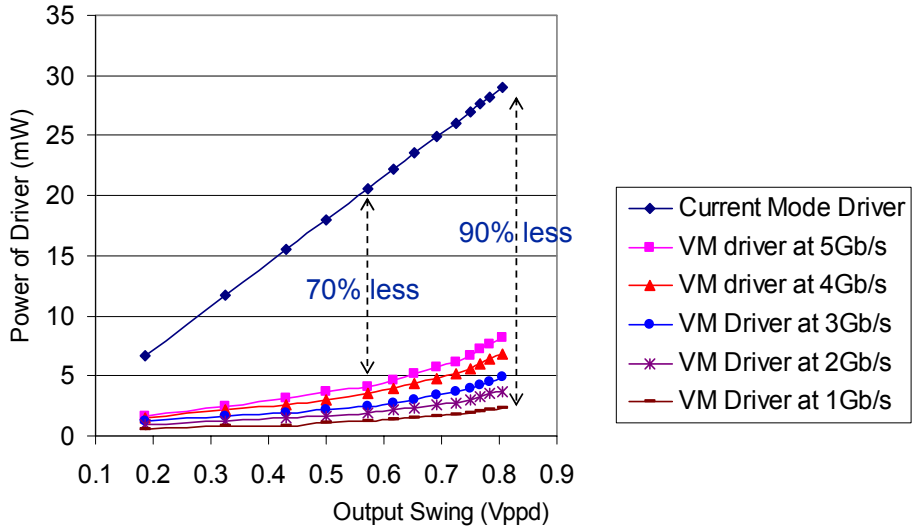


Figure 3.12: Power savings from voltage mode driver, with a data activity of 0.5, for 1G-5Gb/s data rates, with 0.18um CMOS driver

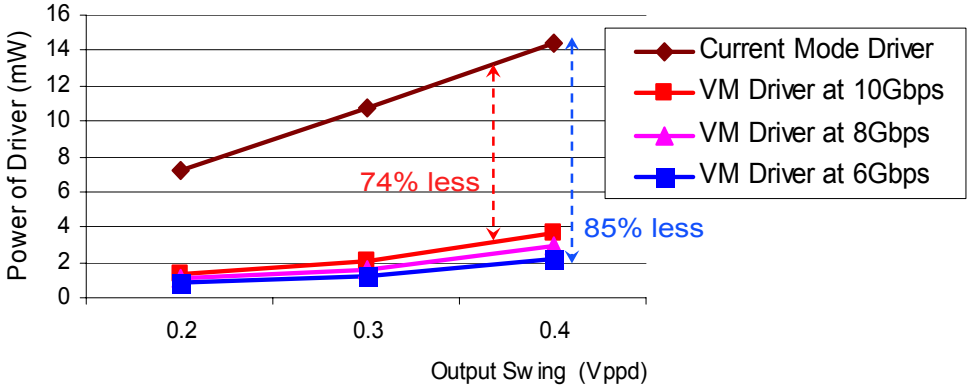


Figure 3.13: Power savings from voltage mode driver, with a data activity of 0.5, for 6G-10Gb/s data rates, with 90nm CMOS driver

The voltage-mode driver only draws dynamic current and thus consumes much less power than a current-mode driver. Figure 3.12 compares simulated 0.18 μm current-mode and voltage-mode driver power for data rates from 1Gb/s to 5Gb/s, with a data activity of 0.5, both include appropriate parasitics for a MCM implementation. To get the same output swing (either a NRZ or return-to-zero pulse), the voltage mode driver saves 70% to 90% power,

depending on data rate. Figure 3.13 shows similar power savings for higher data rates with a 90nm CMOS driver.

Above all, we use complementary inverters for their fast edge rates, low dynamic power dissipation, simple design and smaller circuit area. The disadvantage of the inverter is that dynamic supply current will introduce synchronous switching noise (SSN). This SSN could be reduced by adding slew rate control for low data rate communications and adequate power supply filtering/decoupling. Techniques to reduce this SSN will be discussed in chapter 5.

3.4.3 Basic Low-Swing Pulse Receiver

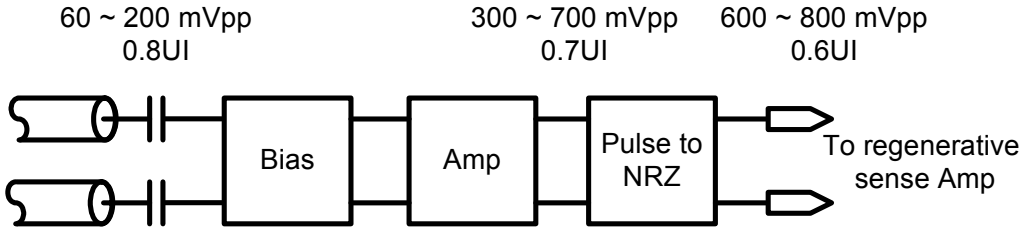


Figure 3.14: Block view of a basic low-swing pulse receiver with timing/voltage margin

Figure 3.14 shows the basic functional blocks of the low-swing complementary pulse receiver, with voltage and timing margin noted at each node. In ACCI, since the coupling capacitors block the DC signal, the RX needs to self-bias, then amplify and convert the pulse signals into NRZ data.

To accommodate combinations of coupling capacitors' size, gap, overlap, tilting and T-Line length, the input sensitivity range is set to be from 60 to 200mV$_{pp}$. A sense amplifier is needed to increase pulse swing to be more than 300mV$_{pp}$, which is the minimum input swing requirement for the edge detector circuit. The output of the edge detector is 600mV$_{pp}$ NRZ

data, which is ready to be sampled by the regenerative sense amplifier. A 600mVpp swing is chosen with tradeoffs among voltage margin, latch bandwidth and timing margin.

Minimum timing margin at output is set as 0.6UI to insure correct clock recovery operation and good jitter performance in the recovered clock. Input timing margin is set to 0.8UI, considering 0.1UI jitter loss at the transmitter output and another 0.1UI loss on T-Line. The deterministic jitter from ISI is not included since the coupling capacitors provide passive equalization. The "Bias", "Amplifier" and "Edge Detector" will consume the remaining timing margin up to 0.2UI.

3.4.4 Low-Swing Pulse Receiver

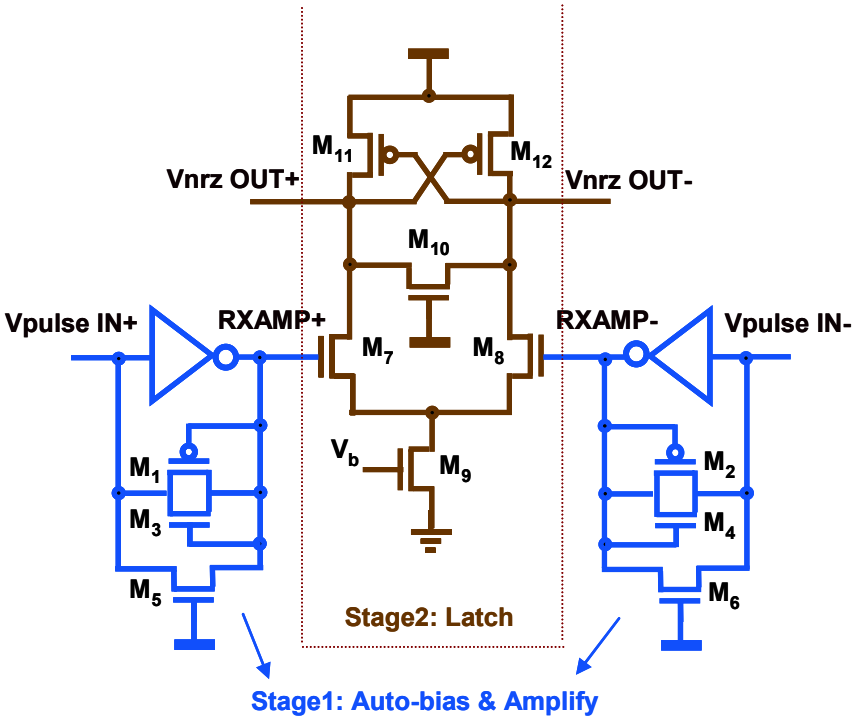


Figure 3.15: Low-swing, high-speed pulse receiver

A pulse receiver is used to recover NRZ data from the ACCI channel. In ACCI, since the coupling capacitors block the DC signal, the receiver needs to self-bias, then amplify and

convert the pulse signal back into NRZ data. Figure 3.15 illustrates the low-swing pulse receiver. Two inverters, with negative feedback (M_1-M_6), self-bias and amplify the differential pulse signal at the receiver input. The feedback structure not only sets up the bias level but also helps to hold the inverter in the high gain region. There are two feedback mechanisms employed here to achieve both adaptive swing control and a stable bias level to accommodate variations in coupling capacitor size and T-Line length. The diode connected feedback (M_1-M_4) limits the swing at the output of the inverters by adaptively controlling the feedback strength. It also sets up a coarse bias voltage, which is sensitive to the data pattern and both the width and swing of the incoming pulses. To mitigate this problem, the NMOS devices (M_5 and M_6) tied to V_{dd}, provide a weak but constant feedback to stabilize the bias voltage, making it less sensitive to the input pulses.

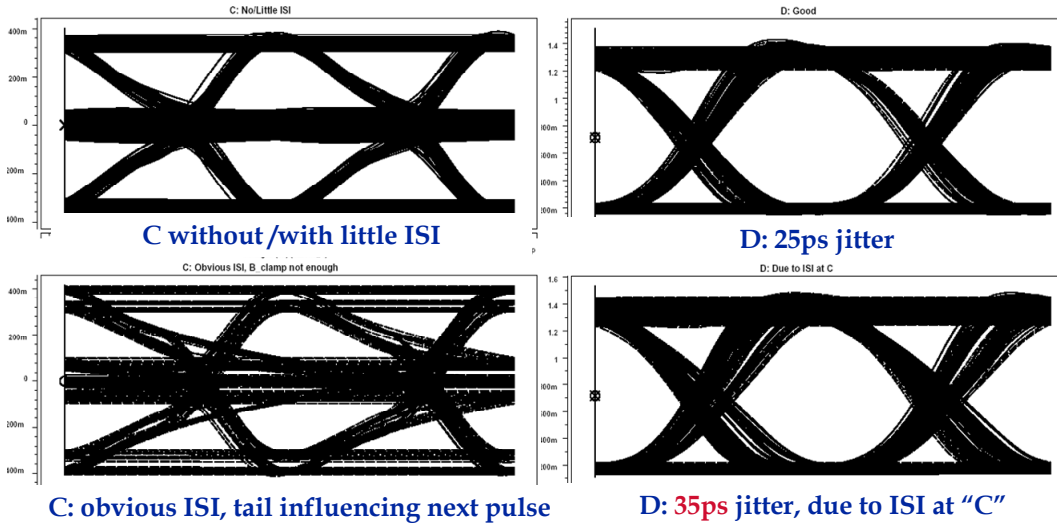


Figure 3.16: Jitter at pulses influence the latch operation and lead to jitter at NRZ data

Note that the pulse width is extended due to limited bandwidth of the bias stage. The design trade-off is between gain and bandwidth. Strong feedback is preferred to get higher bandwidth while weak feedback is preferred to get higher gain. An optimized design

procedure is to get higher gain up to the point that the pulse width reaches the bit width, as shown in the top two waveforms in Figure 3.16. In contrast, the bottom two waveforms show the pulses exceeding one bit period, producing ISI in the pulse signals, leading to more jitter at the recovered NRZ data.

The source coupled logic (M_7-M_9) further amplifies the pulses, while the cross-coupled PMOS load (M_{11} and M_{12}) serves as a clock-free latch to recover NRZ data. A clamping NMOS device (M_{10}) limits the swing of long "1s" or "0s" and enables latch operation for a single "1" or "0". The recovered NRZ data is then fed to a traditional clock and data recovery circuit for receiver clock phase recovery and data re-sampling. Figure 3.17 shows the recovered NRZ data without and with the clamping NMOS device (M_{10}). The clamping NMOS transistor enables higher speed latch operation. The consecutive "1" and "0" are swing limited due to the clamping transistor, which enables a single "1" and "0" transition to have same swing as a long series of "1s" or "0s". This is especially important design feature of this latch structure because as long as the output is deeply latched when consecutive "1" and "0" occurs, it's very difficult for single "1" and "0" to toggle.

The trade-off of this latch design is between high bandwidth and robust latch operation. M_7, M_8 and M_{10} help increasing bandwidth while M_{11} and M_{12} help to insure robust latch operation. The design procedure is to guarantee robust latch operation and then maximize the bandwidth. If the latch doesn't work properly, it will not work at any data rate. However, if the bandwidth is not enough, it can still work for lower data rates. So, it is important to leave some margin to insure that latch design is robust across voltage, transistor and temperature variations.

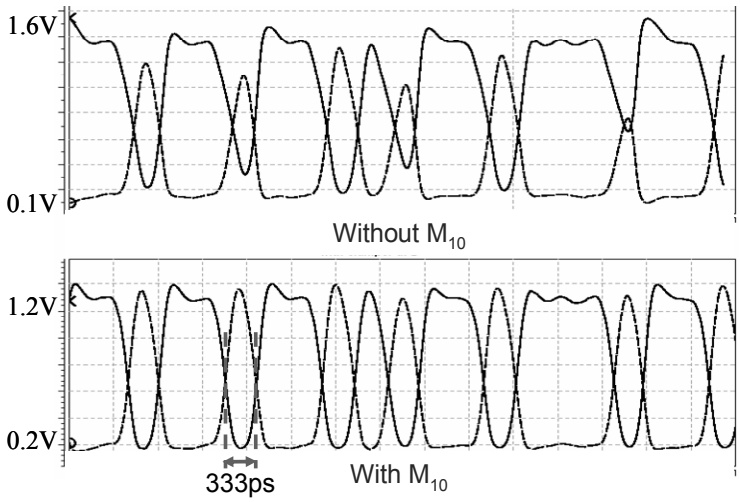


Figure 3.17: Output clamping for high speed latch operation

3.4.5 Receiver Input Common-Mode Offset

Receiver side offset is established by the use of feedback transistors. The top two curves in Figure 3.18 show how the auto-biased offset voltage tracks well with the ideal inverter switching threshold voltage. This ensures the front-end inverter is always biased at the switching threshold point across all transistor process corners. The bias voltage will deviate around the offset due to data activity, as shown in the bottom curve in Figure 3.18. Simulations show that the peak-to-peak deviation of this bias voltage is controlled to within 10% of the total pulse swing across all process corners. This low deviation in the bias voltage is provided by the turned-on NMOS M_5 and M_6 in Figure 3.15. M5 and M6 provide a weak but constant feedback to stabilize the bias voltage, making it less sensitive to the input pulses. In contrast, Kühn's receiver [48] has a similar structure but without M_5 and M_6. The bias voltage is thus very sensitive to the pulse width, pulse swing and data activity of the signal. Large bias voltage deviation across process corners is observed in simulation with Kühn's receiver.

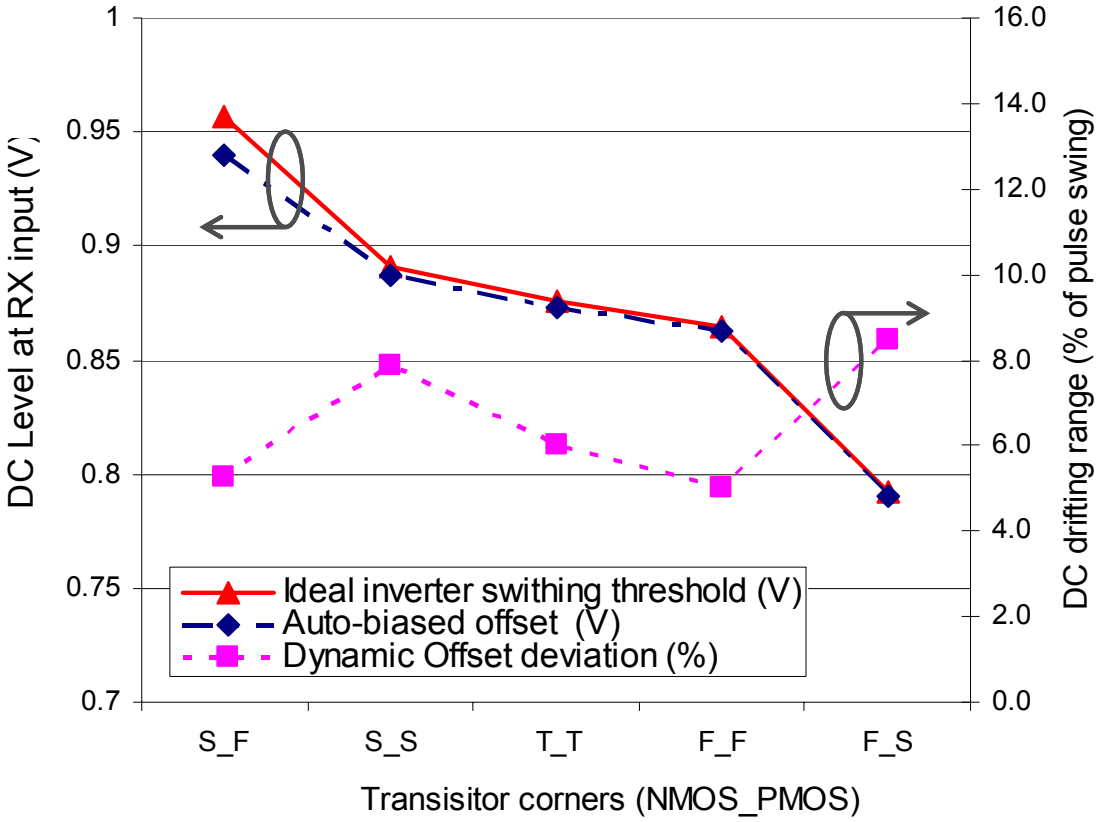


Figure 3.18: RX input offset and deviation

3.4.6 Receiver Input Noise Margin

There are two kinds of noise margin associated with a RZ-pulse signal. An RZ-pulse signal eye diagram, as shown in Figure 3.19, can be divided into two portions in one data period. One is the pulse, and the other is the return-to-zero (RZ) portion or tail. In the pulse, the noise margin NM_P is the difference between the pulse swing and the receiver threshold. In the RZ portion, the noise margin is the receiver threshold, which prevents the mis-detecting of noise as a valid pulse. To maximize the noise margins, it is desirable to make the receiver threshold voltage equal to half of the signal swing.

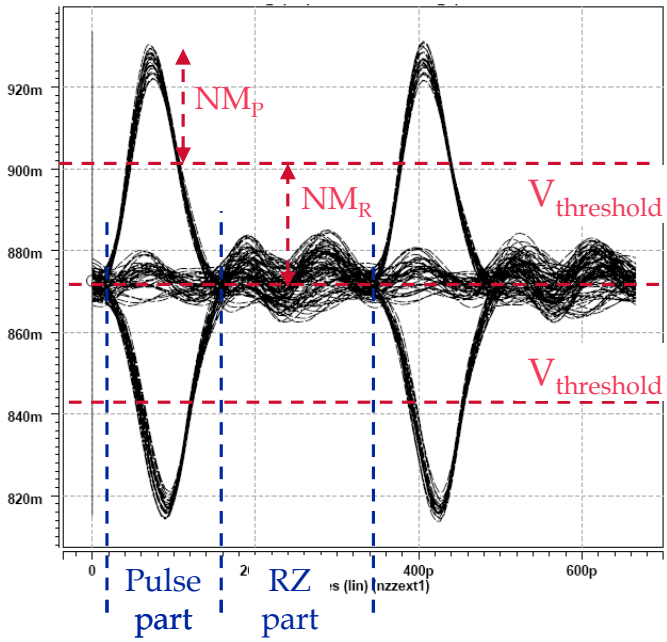


Figure 3.19: Noise margin of RZ pulse signal at receiver input

3.4.7 Simulated Shmoo Plot

Simulations were performed with the voltage mode driver, the ACCI channel and the pulse receiver. Figure 3.20 shows the shmoo plot based on the simulation results. Various simulations of 3Gb/s chip-to-chip communication over an ACCI channel are shown for TX side and RX side coupling capacitors simultaneously varying from 85fF to 175fF verses T-Line length varying from 0cm to 20cm. The transistor level parasitic capacitors at the driver output and pulse receiver input are modeled using Spice. Additional parasitic capacitors (CP) shown in Figure 3.6(a) are also included in the simulations. $CP0_{TX}$ and $CP1_{RX}$ are the parasitic capacitance associated with the MIM capacitor size, which is estimated as 30% of the CC value. Since the test chip is not packaged in the wirebond test, $CP1_{TX}$ and $CP0_{RX}$ are estimated as 200fF to represent the parasitic capacitance associated with 0.025mm diameter and 2mm long bonding wire. The parasitic resistance and inductance associated with the

bonding wires (not shown in the figure) are estimated as 0.1Ω and 2nH respectively. We assume the transistor layout is symmetrical and close enough so transistor mismatch is not included in this simulation. As discussed before, minimum coupling capacitance is constrained by the input pulse swing requirement of the receiver, which needs to be more than $120mV_{ppd}$. Maximum coupling capacitance is constrained by ISI in neighboring pulses, which requires pulse width to be less than the 330ps bit period for 3Gb/s operation. Maximum T-Line length is constrained by either swing (in lower right area) or ISI limit (in upper right area). The valid operating range, for variation in one or both of the coupling capacitors, allows a $\pm 35\%$ tolerance to capacitance value, which could come from the six degrees of misalignment [67]. The valid operating range of T-Line lengths enables chip-to-chip communication over distance variations from 0cm to 20cm using the same transceiver cell, even with the $\pm 35\%$ change in one or both of the coupling capacitors.

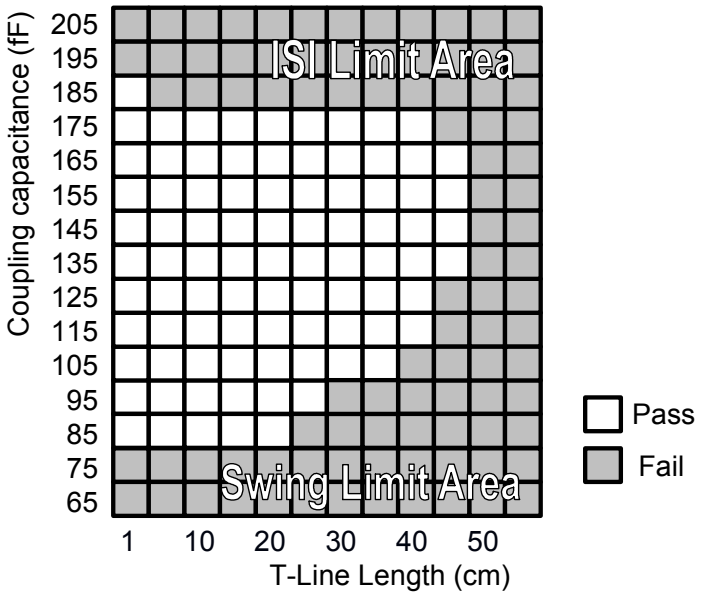


Figure 3.20: Simulated shmoo plot with coupling capacitance and T-Line length variations, pass criteria is 0.8UI time opening at the eye diagram of the recovered NRZ data

3.5 Noise analysis

Simulations have been performed to quantify the effects of additional power supply noise and signal common-mode noise on the T-Line, and are shown in Figure 3.21. Differential noise at the receiver input will be considered as part of the signal and needs to be directly subtracted from the input noise margin. Therefore, only common-mode noise is analyzed in this section. Both of the noise sources are frequency swept and simulated across all transistor corners (SS, SF, FS and FF).

3.5.1 Common-mode noise at the receiver input

A sinusoidal noise source is swept from 10MHz to 11GHz and its signal is injected to the T-Line to simulate the common-mode crosstalk noise from neighboring lines or vias, and coupling noise from reference plane.

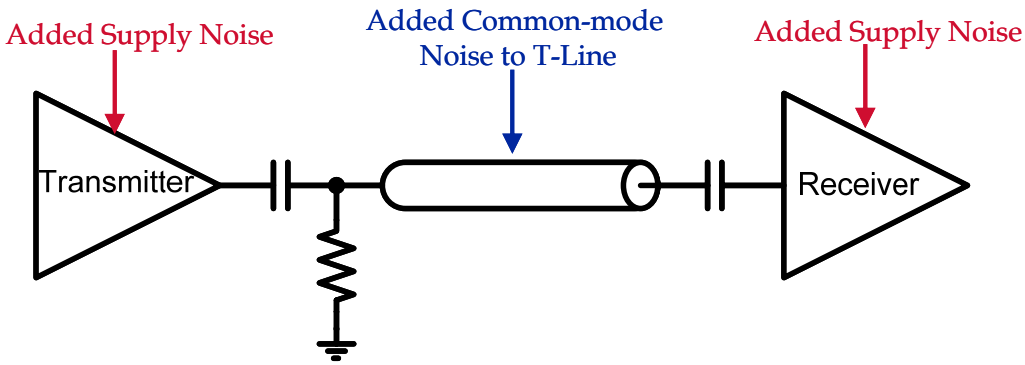


Figure 3.21: Simulation of common-mode noise on the T-Line and supply noise on transceiver

A comprehensive transient simulation including added T-Line noise, added supply noise and self-generated SSN (refer to Figure 5.7 (a)) are performed. A $10mV_{pp}$ SSN (from 4nH power supply pin inductance with 200pF power supply bypass capacitance) and $30mV_{pp}$ at 3GHz (worst case) added supply noise is included. At each frequency point, we apply additive AC

noise on T-Line until the NRZ output falls into the eye opening mask (0.75UI eye opening and 500mV voltage opening).

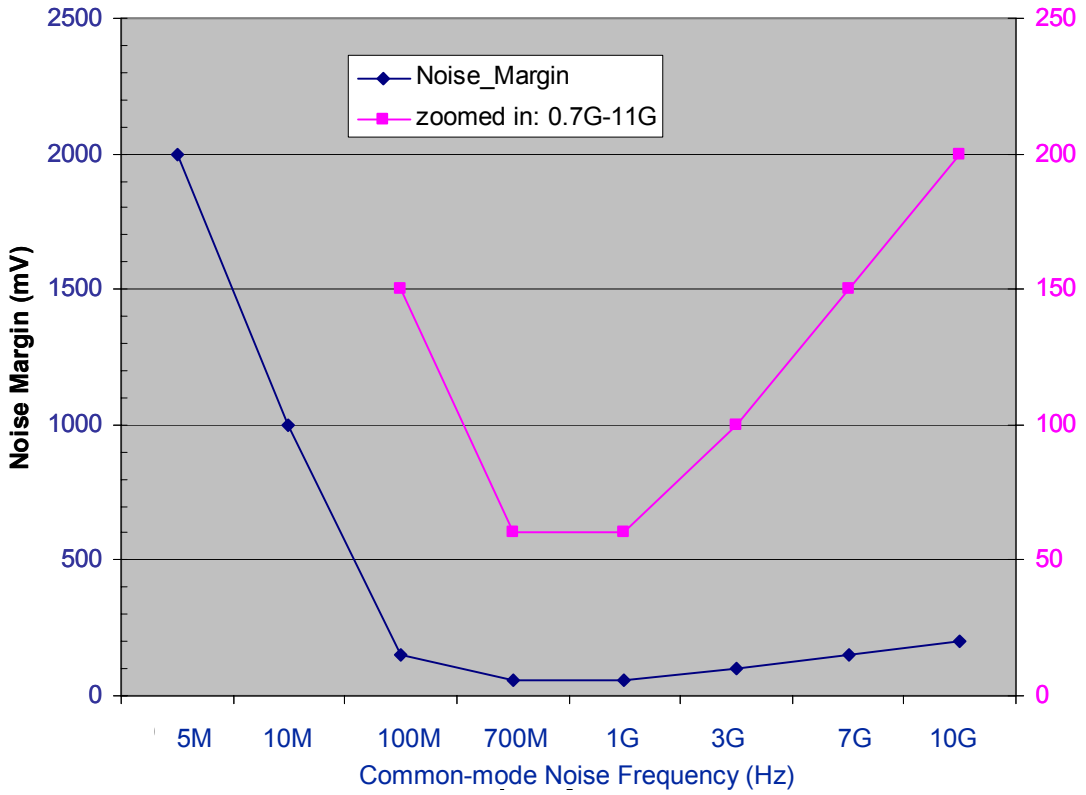


Figure 3.22 Surviving Noise margin for all 4 variation corners

The final surviving noise margin for all four transistor process corners is shown in Figure 3.22. Below are the two major observations:

1. Any T-Line noise lower than 5MHz can be as large as 2Vpp, including DC level. This indicates ACCI links can reject low frequency common-mode noise very well. It can also be used between two systems with different power supply voltages or I/O DC operating levels.

2. Noise from 0.7~1GHz is in the high sensitivity range and the noise margin in this range is 60mV$_{pp}$. The main reason for this is because the latch operation is sensitive to the common-mode noise in this frequency range. To increase this noise margin, a stronger latch is desired

in Figure 3.15, but this will reduce the bandwidth of the pulse receiver, as discussed in the latch design trade-offs.

3.5.2 Power supply noise sensitivity

To quantify the power supply noise rejection ratio, simulations using a supply noise model from IBM (located at RTP, NC) were performed, as shown in Figure 3.23 and Figure 3.24, for 150fF coupling capacitors and for 90fF coupling capacitors, respectively. Both simulations were at 3Gb/s and with 20cm micro-strip T-Line. The supply noise sensitivity is defined as $\frac{\Delta Jitter\,(ps)}{\Delta Supply\ Noise\,(mV)}$, where jitter is measured at the recovered NRZ eye diagram (1 UI equals to 333ps at 3Gbps) and supply noise here is 100mV. For the 150fF coupling capacitor case, the supply noise sensitivity is *0.1ps/mV*. For the 90fF coupling capacitor case, it is *0.13ps/mV*. The reason for higher supply noise sensitivity for 90fF case is due to the lower signal swing at receiver input. The pulse swing at receiver input is 60mV for 90fF case and 120mV for 150fF case, as shown in the figure. As expected, this suggests avoiding having small a pulse swing at the receiver input. Again, this comes from the design trade-offs between pulse swing and ISI, as we discussed in previous section.

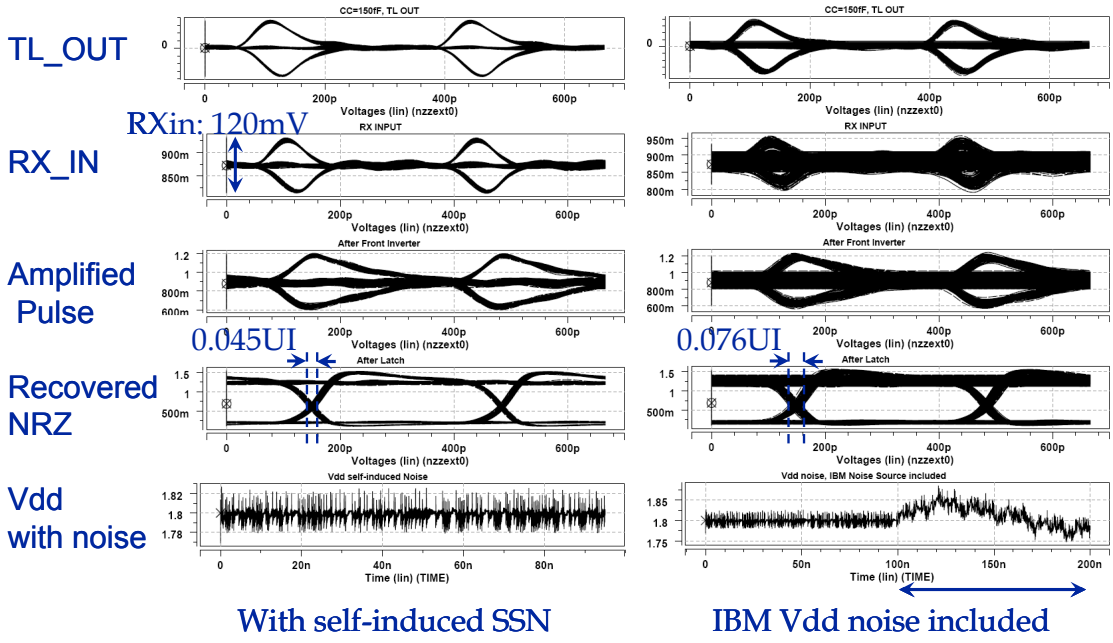


Figure 3.23: Transient simulation with power supply noise model from IBM, with 150fF coupling capacitors and a 20cm T-Line

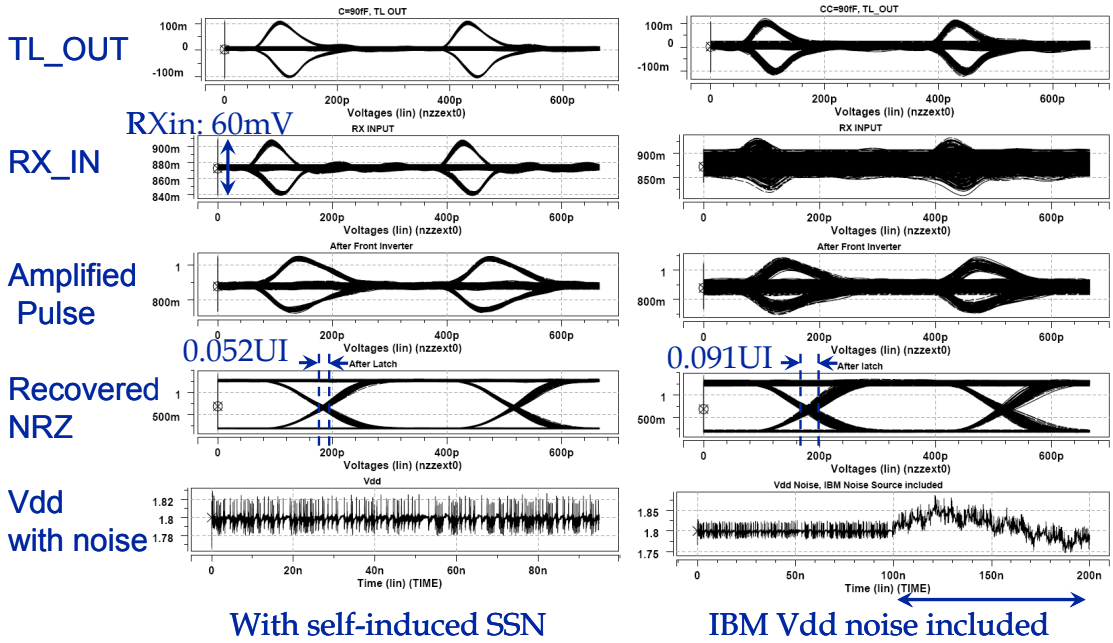


Figure 3.24: Transient simulations with power supply noise model from IBM, with 90fF coupling capacitors and a 20cm T-Line

3.6 ACCI design procedure

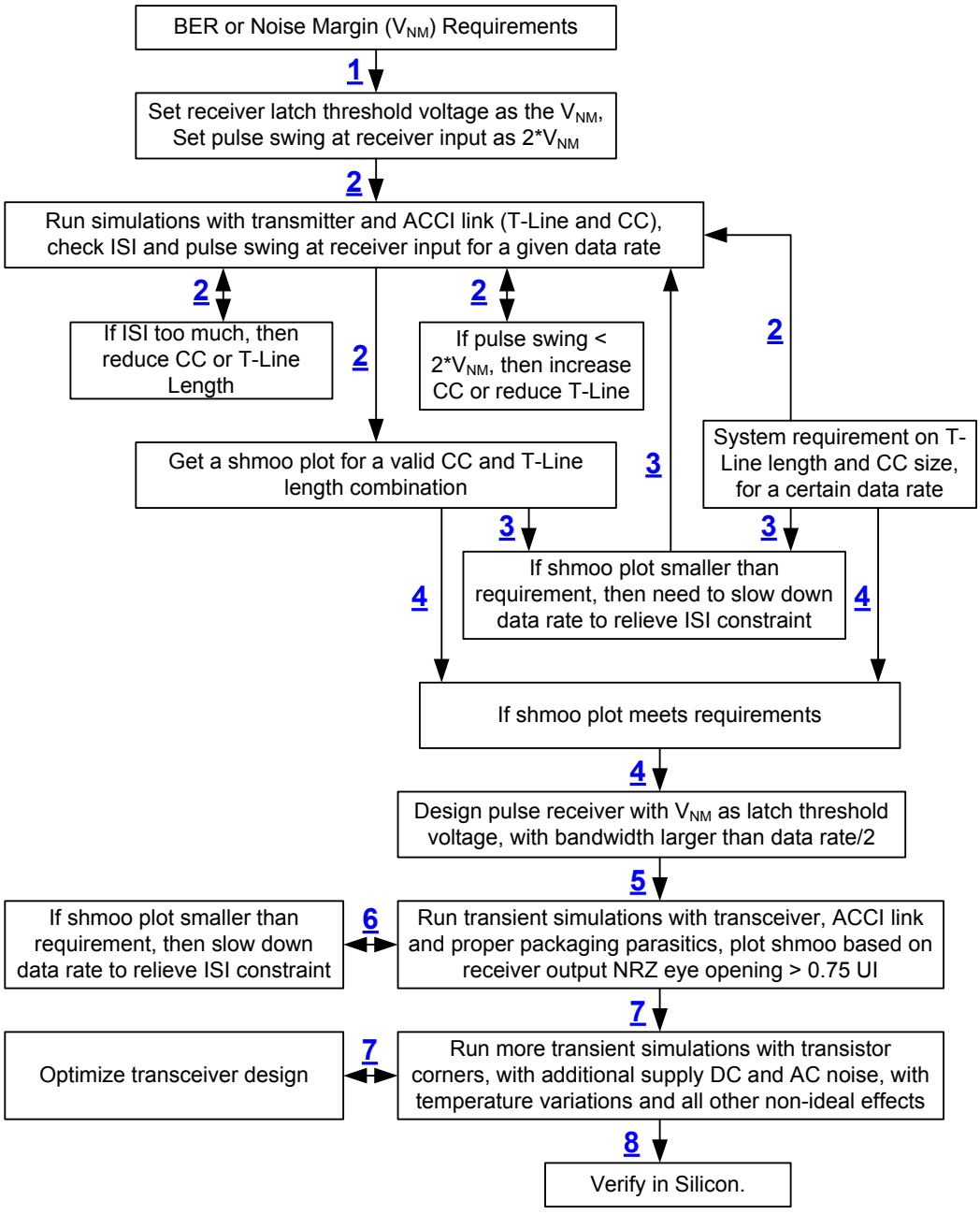


Figure 3.25: Basic design flow for capacitively coupled interconnect

To summarize, an ACCI design procedure is suggested in Figure 3.25.

1. Based on the BER requirements, the noise margin requirement V_{NM} is estimated for receiver input RZ pulse. Based on Figure 3.19, the receiver latch threshold voltage is set as V_{NM} and the pulse swing at the receiver input is set to $2*V_{NM}$.

2. Perform simulations for a simple ACCI channel. The system requirements give the initial settings for T-Line length, coupling capacitor size and the operating data rate. Typical range of these requirements is 0 to 40cm T-Line length, 80fF to 200fF coupling capacitor size and 0 to 10Gbps data rate. Note the T-Line length and data rate variation is due to the application requirements while the coupling capacitor size variation is to accommodate the packaging and assembling variations. Based on these parameter, simulations are performed with a voltage mode driver, ACCI link, single side or double side parallel termination for a given data rate. The pulse signal eye diagram is observed at receiver input (refer to Figure 3.9). If there is ISI, then reduce the coupling capacitor or T-Line length. If the pulse swing is less than $2*V_{NM}$, then increase the coupling capacitor or reduce the T-Line length. After iterations, an initial shmoo plot is generated with a valid CC and T-Line length combination. The pass criterion here is whether there is observable ISI or not.

3. If the simulated shmoo plot pass area is smaller than that of the system requirements, we need to negotiate with system level requirements to either reduce the shmoo plot pass area or reduce the data rate. Otherwise, simple receiver side equalization is needed to remove the ISI. Suppose the data rate requirements can be reduced, we then perform shmoo simulation again.

4. If the simulated shmoo plot meets the requirements, the pulse receiver needs to be designed with V_{NM} as the latch threshold voltage. The pulse receiver also needs to have an

operating bandwidth greater than half of the data rate. For example, if the data rates are 3Gbps, the pulse receiver needs to have a bandwidth of at least 1.5GHz.

5. A more realistic transient simulation is needed to estimate the ACCI channel with transmitter circuit, ACCI channel, pulse receiver circuitry and all packaging parasitics. The parasitics include the power supply pin inductances, decoupling capacitors, bonding wire parasitics, through hole via stubs, termination resistor variations, T-Line impedance mismatch and discontinuities, parasitic capacitance of the coupling capacitors and other physical imperfections. We sweep the T-Line length and coupling capacitor size and get a preliminary shmoo plot. This time, the pass criterion is whether the recovered NRZ eye diagram opening is larger than 0.75UI.

6. If the preliminary shmoo plot doesn't meet the system requirements, the data rate needs to be reduced and then repeat step 6.

7. If the preliminary shmoo plot meets the system requirements, then run simulations with more non-ideal effects, such as transistor process corners, power supply DC variation and AC noise, temperature variations, transistor mismatches and other variations. A final shmoo plot is generated after these simulations. Transceiver optimization is needed to expand the shmoo plot pass area, to increase the data rate and to function more robustly cross all the non-ideal factors.

To optimize the transmitter design, the rising edge and falling edge need to have same edge rate to generate same amount of swing on both positive and negative pulses in ACCI channel. The data rate requirement defines the maximum pulse width and thus maximum transmitter output NRZ rising/fall edge rate, which is related to the strength of the transmitter. There is a

design trade-off for how strong the transmitter should be. A strong transmitter will generate fast edge rate and thus short pulses, which reduces ISI but dissipates more power, occupies more circuit area and generates more switching noise. The design rule here is to guarantee low ISI and then find the smallest transmitter. Thus, we get smallest transmitter design, lowest power dissipation and lowest SSN while maintaining low-ISI operation.

To optimize the receiver design, the key is to balance the design trade-off between the bandwidth and the robust latch operation. The design rule is to guarantee a robust latch operation and then maximize the bandwidth. If the latch doesn't work properly, it will not work at any data rate. However, if the bandwidth is not enough, it can still work for lower data rates. So, it is important to leave some margin to make insure a robust latch design. (The latch operation in the pulse receiver design is similar the race problem in a sequential logic.)

8. After the transceiver design is optimized, we then design the chip and verify the design in silicon, package and interconnect.

Chapter 4 Capacitively coupled serial link

The pulse receiver developed in Chapter 3 is the front-end receiver (RX in Figure 4.1) for capacitively coupled serial links. In this chapter, a test chip with a complete capacitively coupled serial link design is presented. The test chip includes a random data generator, multi-phase DLL, serializer, driver, pulse receiver, clock and data recovery, deserializer and bit error rate tester.

4.1 Architecture

We will first illustrate the architecture of the whole transceiver, followed by circuit details in the transmitter path and receiver path. The block level layout of the test chip is shown in Figure 4.1. TX is the voltage mode driver and RX is the pulse receiver. Four pseudo-random bit sequences (PRBS) with a pattern length of 2^7-1 are generated with spread seeds and multiplexed by four into a 3Gb/s data stream based on 4-phase DLL generated clocks. The driver outputs full-swing NRZ data into the ACCI channel. To reduce reflections, a 50 Ω shunt termination is used. The pulse receiver recovers the NRZ data from the low-swing

pulses and sends this data to a semi-digital dual-edge DLL. The clock phase at the receiver is recovered and the data are deserialized by four and analyzed for BER.

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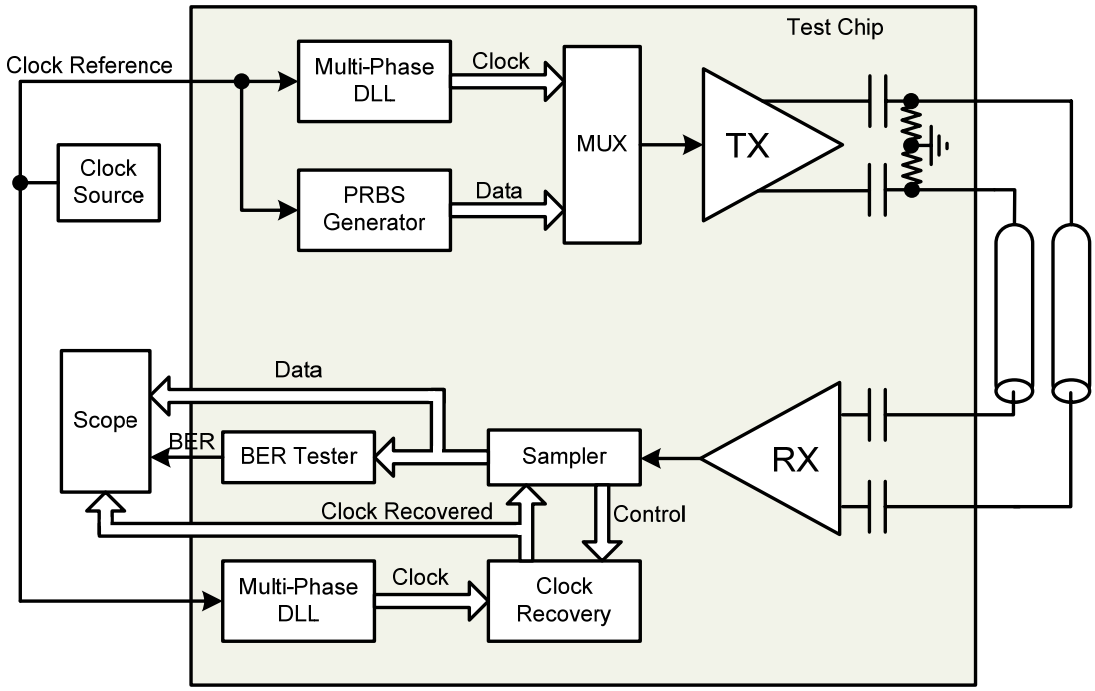


Figure 4.1: Block diagram of the test chip

4.2 Transmitter path

The transmitter path includes a multi-phase DLL clock generator, a multiplexer and a driver. The DLL is the key part of the transmitter path since it directly determines the jitter performance of the driver output and further determines the jitter budget of the whole serial link. So we also present some simulation results on the multi-phase DLL. The multiplexer is also a key part, where we expect the output data to have the same jitter performance as the clock.

4.2.1 Dual loop multi-phase DLL

A multi-phase DLL clock generator is used by the multiplexer (MUX) in the transmitter path and also used by the clock phase recovery block in the receiver path. The MUX serializes data based on combinations of the multi-phase clocks; therefore, both edges of the multi-phase clocks are important and will directly influence the jitter performance of the output data. It is required that all the rising/falling edges are spaced by exactly a quarter of a period so that the serialized data jitter is equal to the clock jitter. Otherwise, any inter-clock phase offset, on both edges, will transfer to output jitter in addition to the single clock jitter.

To minimize inter-clock phase offset, the delay cell employs a dual-edge control mechanism [76]. Shown in Figure 4.2, both the rising and falling edge are detected and controlled by the delay cell. “VCN” & “VCP” control the rising edge of the clock line and “VCN2” & “VCP2” control falling edge of the clock line, as shown in the delay cell. To help the phase detector minimize phase errors, it is also necessary to maintain the same rise/fall time and duty cycle for Clk_ref and Clk3. To achieve this, the drive force (output impedance) and capacitive load for each node between neighboring delay cells needs to be well balanced. Dummy delay cells are placed at the beginning and end of the delay loop, and additional dummy capacitive loads are carefully inserted after post-layout RC extraction. This also helps to minimize delay variation between the delay cells.

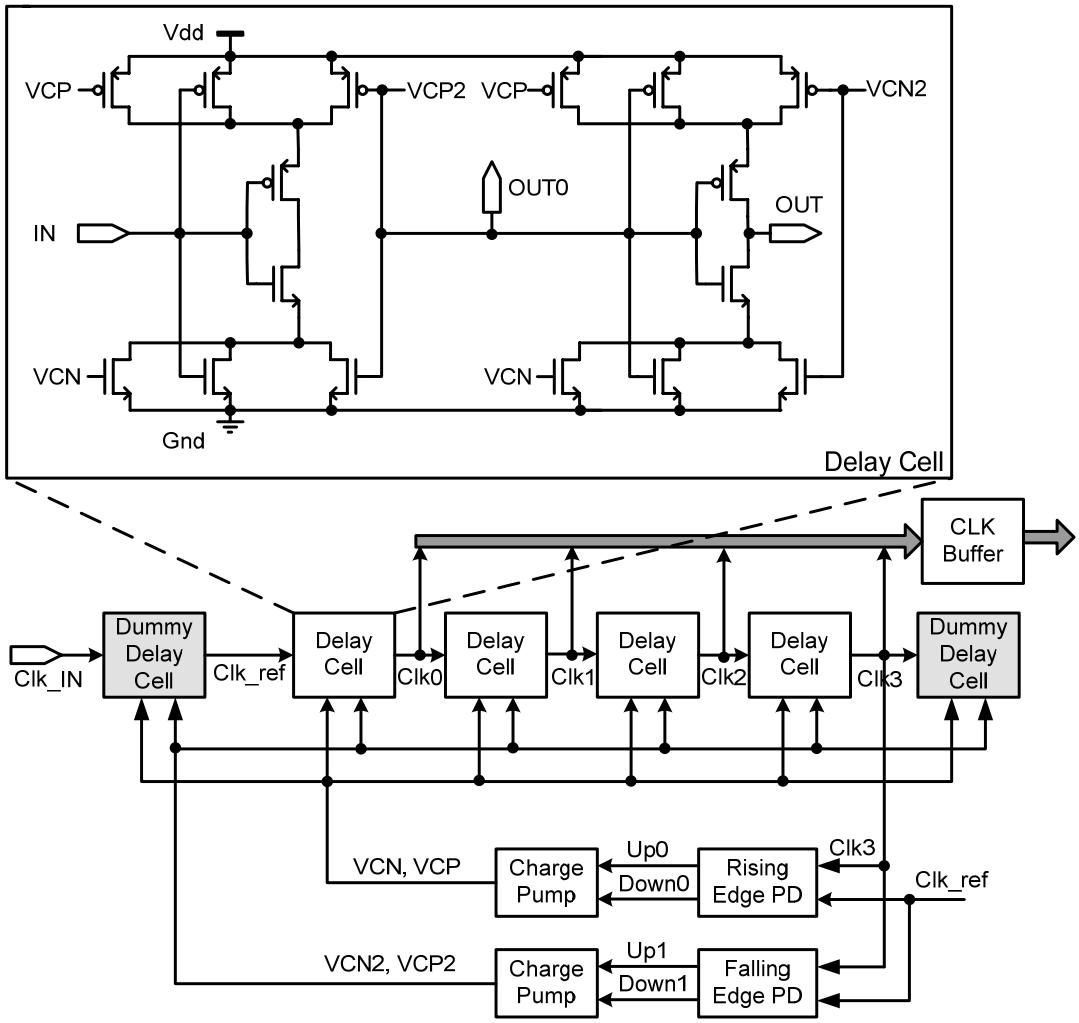


Figure 4.2: Dual-edge controlled Multi-phase DLL

Following is a discussion of the circuit details for all the blocks used in the dual loop multi-phase DLL.

4.2.1.1 Dynamic phase detector

The phase only detector used here was proposed in [76] and is shown in Figure 4.3. The operation is show on the right side of Figure 4.3. Only when “clock_in” is low and “clock_ref” changes from low to high, will “up” be high until “clock_in” changes to high

(complementary levels with the “down” operation). The “up” and “down” pulse width at locked status can be modified by adjusting M1. Smaller pulse width helps relieving mismatch between I_{up} and I_{down} for charge pump circuit. Equal and short up/down pulses during the locked state will help to reduce static phase offset.

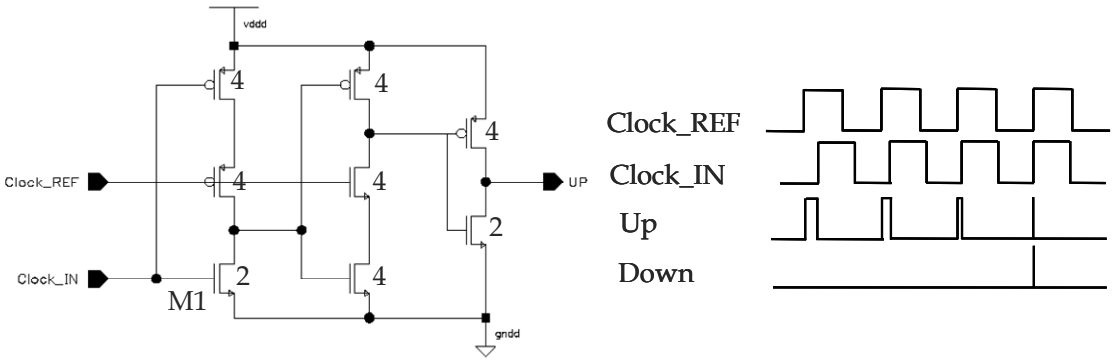


Figure 4.3: A dynamic phase only detector for multi-phase DLL

4.2.1.2 Charge pump circuit

The charge pump circuit serves as a low-pass filter, by removing high frequency phase input while low frequency or constant phase differences are integrated and control signals are generated. The circuit to do this is shown in Figure 4.4. The net charging/discharging current is I_4-I_2. In the locked state, I_1=I_2 = I_3=I_4. The charge sharing effect on M_1 and M_2 will introduce pulse noise on CP_Vbias and thus ripple on the control signal and finally cause the jitter on generated clock. This can be relieved by adding a filter capacitor on CP_Vbias. The short channel effect will cause unbalanced V_{d3} and V_{d4}, thus unbalanced I_3 and I_4. To accommodate this, we use transistors at four times the minimum length for the current mirrors.

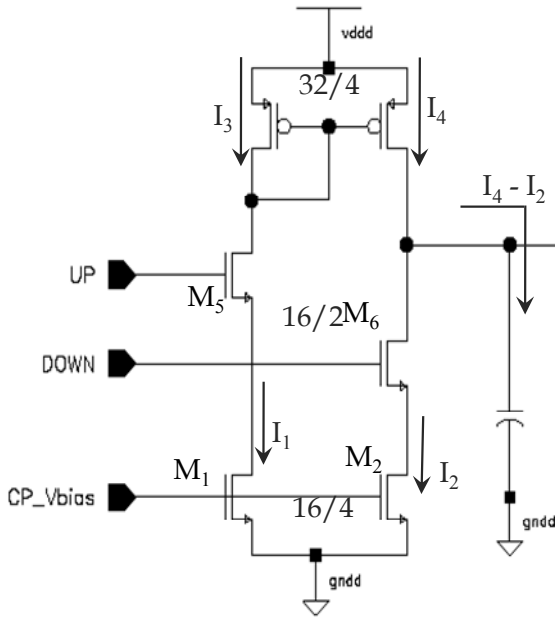


Figure 4.4: Charge pump circuit for multi-phase DLL

4.2.1.3 Clock output buffer

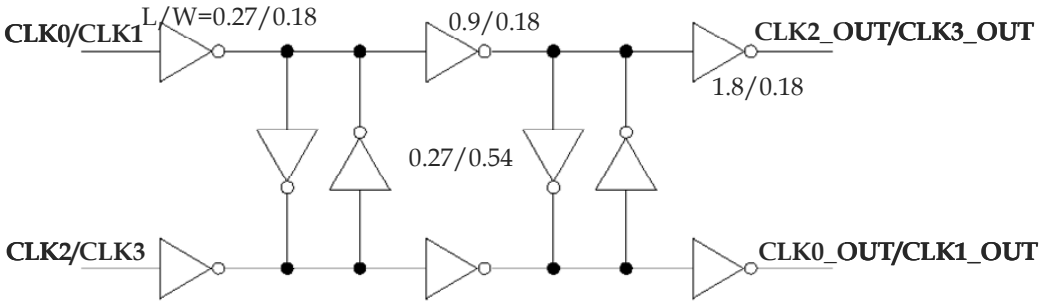


Figure 4.5: Clock outpt buffer for multi-phase DLL

The clock output buffer is shown in Figure 4.5. With the clock output buffer, the DLL is isolated from the clock sinks and the output clock jitter will be decreased due to a faster edge rate. After the output buffer, ring/falling edge of opposite clock phases will be aligned. In addition, this output buffer also auto-adjusts duty-cycle to 50%, with a 40%-60% input duty-

cycle tolerance. To ensure full swing and enough bandwidth, the coupling inverters need to be 1/3 the strength of the buffer inverters.

4.2.1.4 Multi-phase DLL simulation

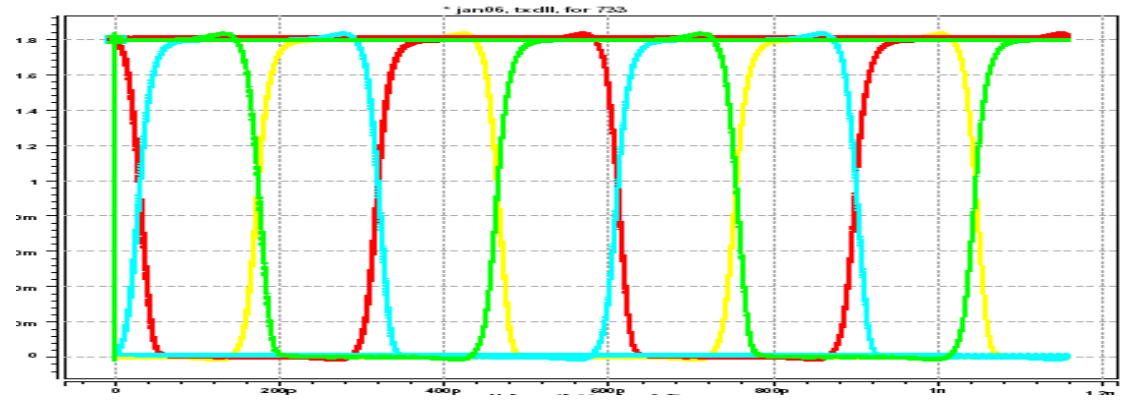


Figure 4.6: Overlapped eye diagram of 4-phase clocks, with 15mV$_{pp}$ supply noise

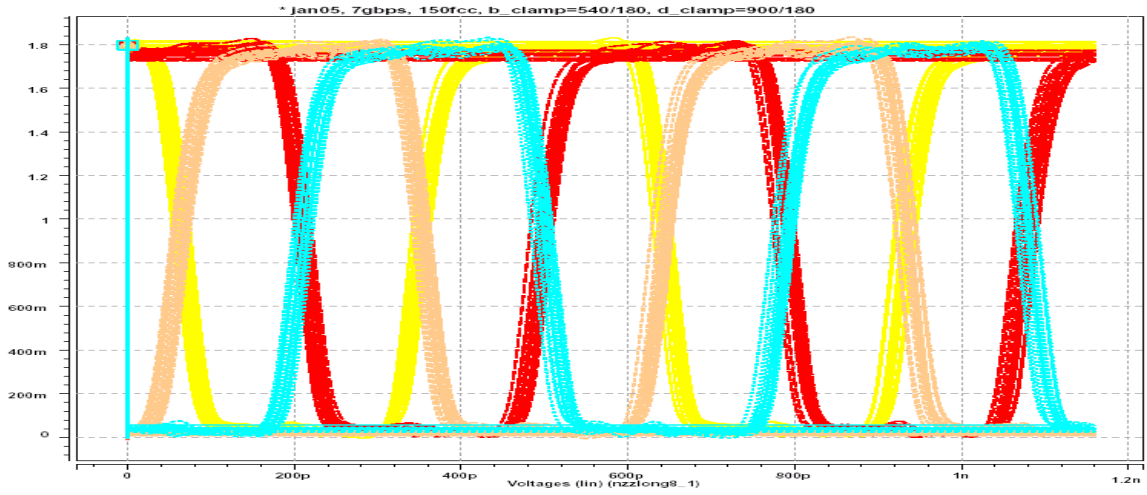


Figure 4.7: Overlapped eye diagram of 4-phase clocks, with 90mV$_{pp}$ supply noise

Simulations were performed on the multi-phase DLL circuits using the TSMC 180nm CMOS technology. Figure 4.6 and Figure 4.7 show the overlapped 4-phase clock eye diagrams with supply noise of 15mV$_{pp}$ and 90mV$_{pp}$, respectively. The measured noise and jitter performance is summarized in Table 4.1.

For the low supply noise case (Figure 4.6), the static phase error is lower than 1ps due to the dual-loop controlled structure. Without dual loop control, the static phase error could be more than 4ps (not shown in this simulation).

For the high supply noise case (Figure 4.7), $jitter_{pp}$ increased a lot mostly because of the noise on the control signal, which is coupled from the power supply noise. The jitter noise sensitivity is approximately 0.5ps/mV.

Performance and parameters	Low supply noise	High supply noise
Static phase error	1ps	3ps
Peak to Peak Jitter	1ps	30ps
Acqusition time	30ns	30ns
Noise on control signal	$20mV_{pp}$	$90mV_{pp}$
Power dissipation	4mW@2GHz	4mW@2GHz
Gnd/Vdd noise	$15mV_{pp}$	$80/90mV_{pp}$
Power supply loop Inductance	1.4nH	1.4nH
On chip Bypass capacitor	200pF	200pF

Table 4.1: Simulation results of the multi-phase DLL, with low and high supply noise

4.2.2 Multiplexer

The multiplexer is based on the combination of the 4-phase clocks, as shown in Figure 4.8. A PMOS with its gate tied to gnd serves as a resistive load, which sacrifices bandwidth when compared to a resistive load. Since the multiplexer bandwidth here is not the limiting factor, this structure was used to save area. The device used to create the tail current in the multiplexer is removed to get rail-to-rail output swing. The multiplexed data is then feed into a differential buffer to provide 3Gb/s data for the ACCI voltage mode driver.

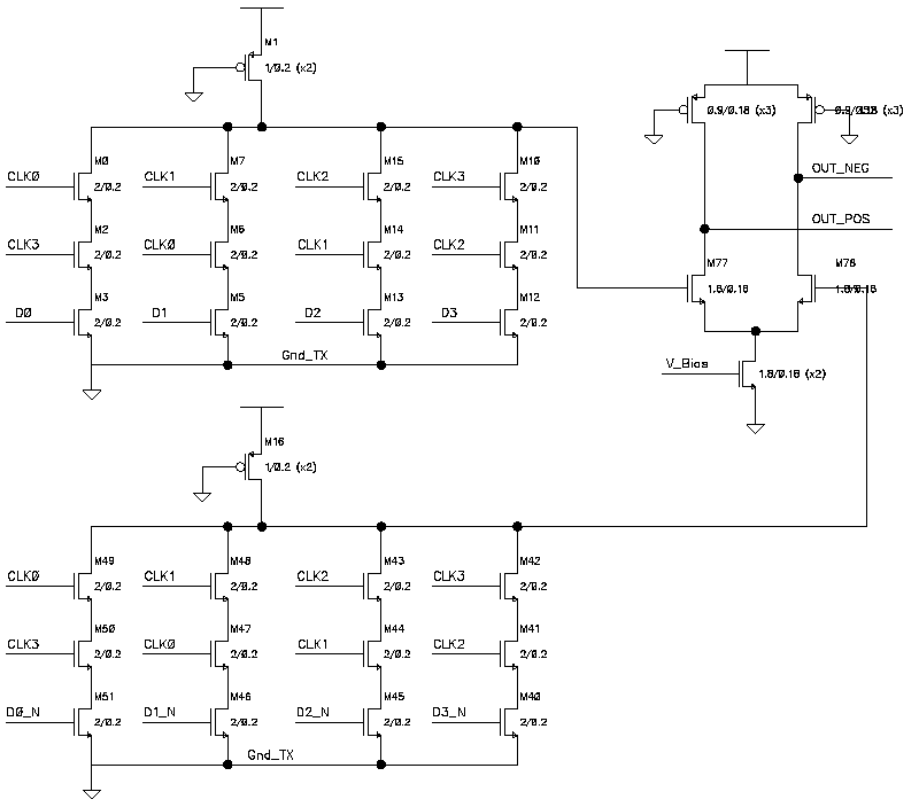


Figure 4.8: Current steering multiplex based on combinations of multi-phase clocks

4.3 Receiver path

Figure 4.9 shows the basic blocks of a pulse receiver with clock and data recovery. In scheme (a), pulse signals are converted into NRZ data by the self-triggered pulse receiver. A conventional clock and data recovery circuit over-samples the NRZ data and generates the receiver side local clock. An alternate for this scheme is (b), where pulses are directly sampled by a "pulse sampler" and the clock is recovered from the sampling results based on the information of whether the receiver side clock is leading or lagging the pulse. Both the sampler and the control path in clock recovery circuit need to be modified. The advantage of scheme (b) is that we can bypass the pulse receiver and thus improve the timing budget.

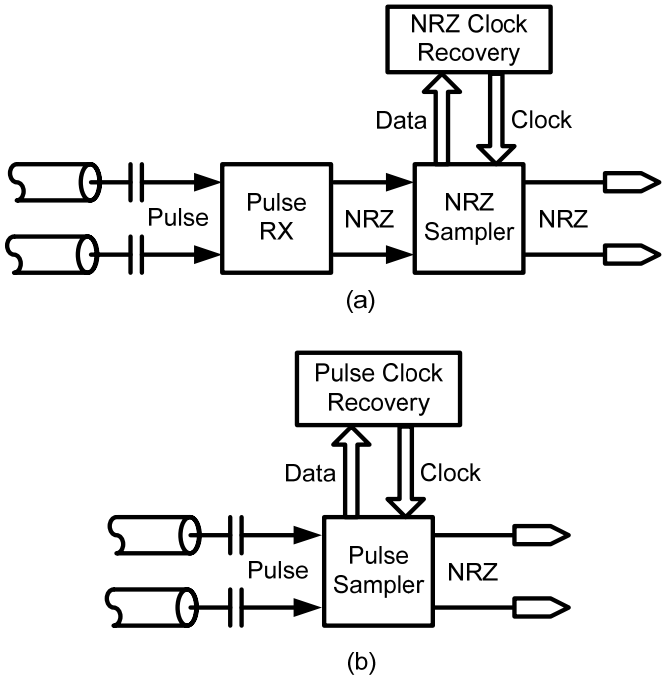


Figure 4.9: Overview of receiver circuits

However, scheme (b) requires a high resolution pulse sampler. Considering a pulse width of only 100ps, the timing budget for the sampler is very tight. Also, the pulse signal has 3 states: positive, negative and zero. The over-sampler needs to have two threshold voltages to do sampling on this pulse signal. To keep this design simple, it was decided to focus on scheme (a). Thus we can reuse the traditional clock and data recovery circuitry after the pulse receiver. In the receiver path, we will present the regenerative sense amplifier, the semi-digital dual-loop clock recovery circuit, PRBS generator and BERT.

4.3.1 Regenerative sense sampler

Suppose we already have the NRZ data from the pulse receiver. This NRZ data will have low jitter performance due to the noisy serial link channel and also due to the added noise after

the self-triggered pulse receiver. A clean receiver side clock is needed to resample, and deserialize the noisy data and get a clean recovered NRZ data.

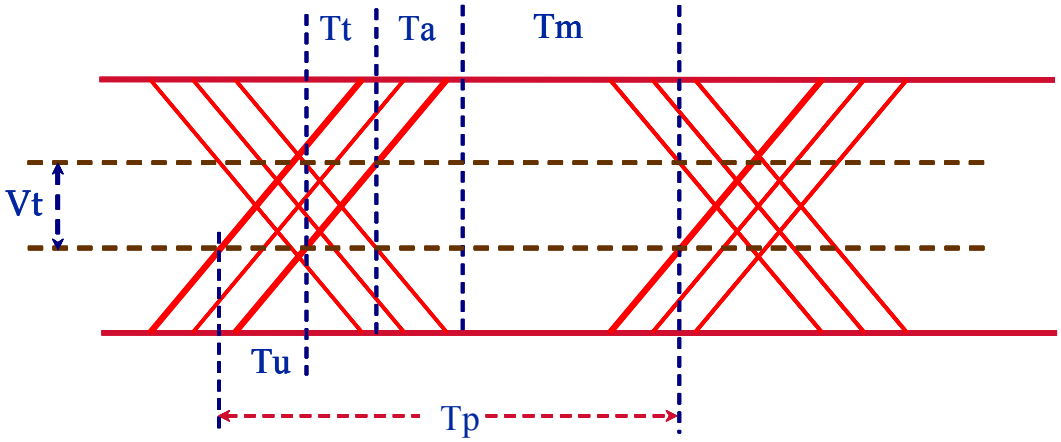


Figure 4.10: Timing budget at input of sense sampler

Figure 4.10 shows the timing budget of a NRZ signal, at the input of the sense sampler, where T_p is the period of NRZ, T_u is the uncertainty jitter (including both deterministic jitter and random jitter), T_t is the transition time corresponding to the sense level of the sampler, T_a is the aperture time of sampler, T_m is the time margin, and V_t is the sense level of sampler. As we can see, $T_m=T_p-T_u-T_t-T_a$. The greater T_m, the more timing margin and the lower BER. T_t is proportional to V_t. A good sampler needs to have smaller V_t and T_a.

The sense sampler in Figure 4.11 is the strongarm latch proposed by Montanaro in [77], which is used extensively as a high-speed sense sampler due to its small load and short aperture time. Coupled PMOS, NMOS and a RS latch load are all used to form a latch to maintain current status. The clamping NMOS structure increases the sensitivity and leads to a smaller sense level. Small differential NMOS transistors are designed to keep the load of

previous stage as small as possible. Smaller aperture time is also achieved by reducing the load of "Va" and "Vb", which enables almost full swing signaling at these two nodes.

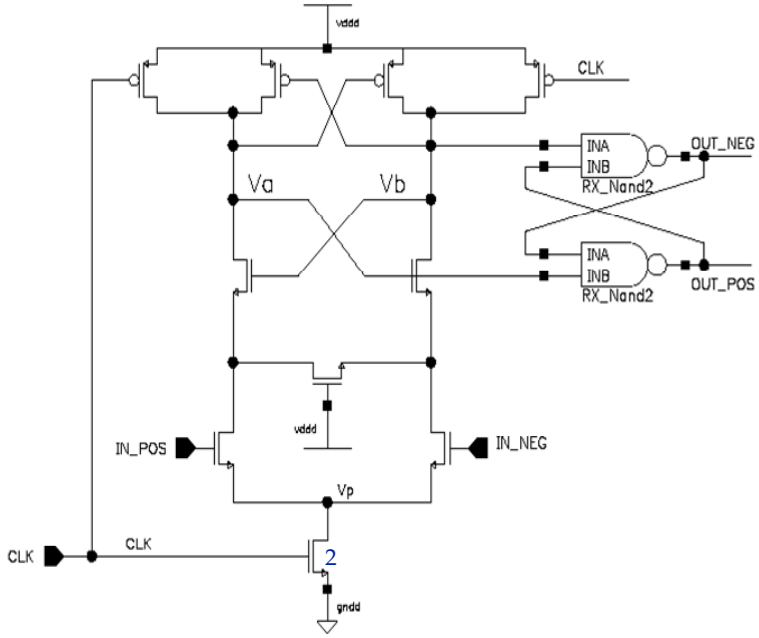


Figure 4.11: Strongarm sense amplifier

Simulation is performed to test the sense level and aperture time. The waveforms are shown in Figure 4.12. A 7Gb/s, 640mV to 700mV NRZ is the input to the sense sampler. The $60mV_{pp}$ sense level corresponds to a 5ps transition time. These parameters are from the output of the pulse receiver designed in Chapter 3. The clock input is 1.75GHz NRZ data with a 70ps edge rate. In Figure 4.12, there are two sets of simulation waveforms. The NRZ input is same for both sets, while CLK is offset by 16ps. In (a), the sampler always correctly samples the D0 bit as shown in Figure 4.13, while in (b), the sampler always correctly samples the D1 bit. From this, we get the aperture time of this strongarm sampler is 16ps $-T_r$ =11ps, at a sense level of 60mV. If the jitter is assumed to be 60ps, then the timing margin is (1000/7)-70-11-5=67ps.

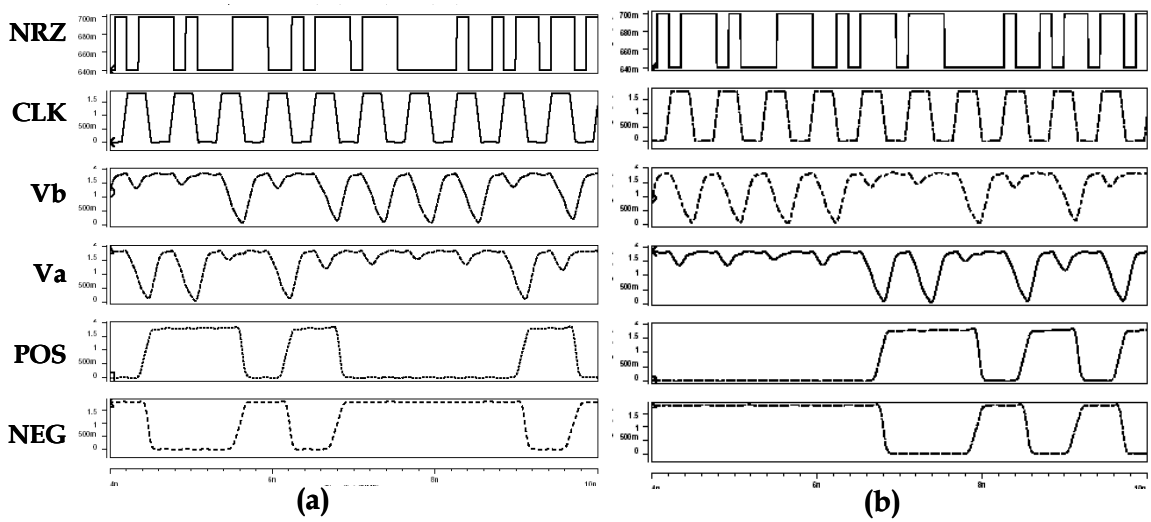


Figure 4.12: Measured aperture time on a 60mV$_{pp}$ sense level

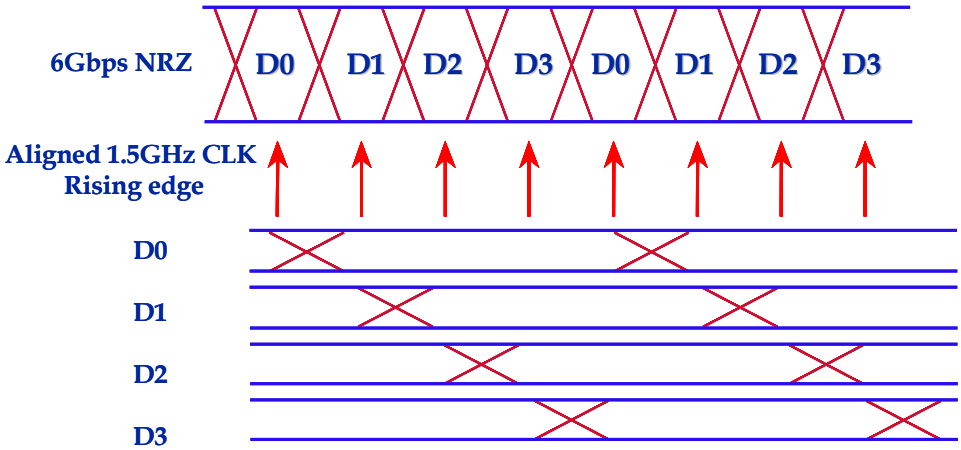


Figure 4.13: Deserialization by 2X oversmapling

Figure 4.13 shows how the implementation of the deserializer in the sense sampler. Four parallel sense samplers sample the NRZ data at the rising edge of each clock phase. The sampling result of each sampler represents the deserialized data, which is now at a lower frequency comparable to $8\tau_4$ and ready to feed into a logic circuitry. Moreover, the data is much cleaner after the re-sampling. The jitter of the deserialized data is reset to the clock jitter.

4.3.2 Clock phase recovery

In designing the deserializer, it is assumed that there are multi-phase clocks with transition edges at the exact center of each bit period. This is realized by a semi-digital dual loop DLL phase recovery circuit. The original method was proposed by Sidiropoulos in [21] and then extensively used in serial link clock and data recovery designs.

As shown in Figure 4.14, 8-phase clocks are generated by a similar multi-phase DLL structure as used at TX side. The NRZ data is sampled by the 8 sense samplers based on each of the 8 evenly distributed clock phases. We define the eight clock phases into two sets, the edge clocks and the data clocks. The edge clocks sample at the data transition edges and the data clocks sample at the data periods. We define the sampling result of the data clock as "data" and the sampling result of the edge clock as "edge". Based on the relative phase offset between the data and clocks there are three statuses:

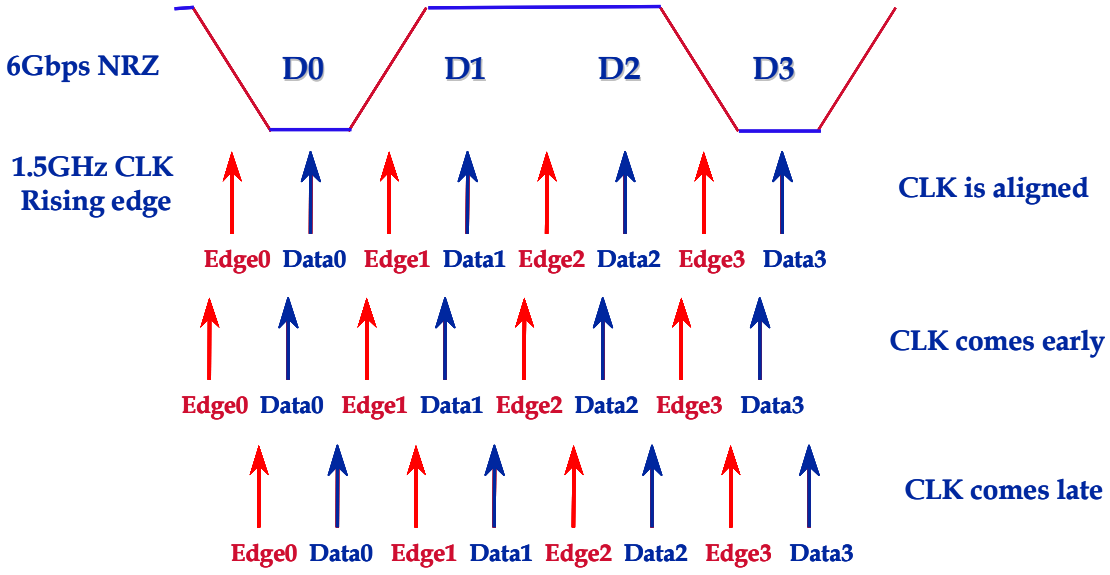


Figure 4.14: 2X oversampling for clock phase recovery

1. Clock is aligned with the data:

Data clocks sample at the center of the bit period, edge clocks sample at the centre of the transition edges. The “data” signal is the deserialized data. When the “edge” signal is equal to either previous or next “data”, this is the ideal clock phase we want to achieve. So, if we observe that half of the “edge” is equal to previous “data” and the other half is equal to next “data”, we then assume the clocks are aligned with data. We also call this “No information”.

2. Clock leads the data:

Both the data clocks and the edge clocks sample before the center points. The “data” signal is the deserialized data, similar to the previous state. But the “edge” always equals to the previous “data”. So, if we observe the “edge” being equal to the previous “data” while not equal to the next “data”, we assume the clock is leadings the data. We call this “Early”. If the previous “data” and next “data” have the same value, we assume there is no timing information we can extract from this “edge” information. We call this “No information”.

3. Clock lags the data:

Both the data clocks and the edge clocks sample after the center points. “Data” is the deserialized data, similar to the previous state. But “edge” always equals to the next “data”. So, if we observe the “edge” being equal to next “data” while not equal to the previous “data”, we assume clock lags data. We call this “Late”. If the previous “data” and next “data” have the same value, we assume there is no timing information we can extract from this “edge” information. We call this “No information”.

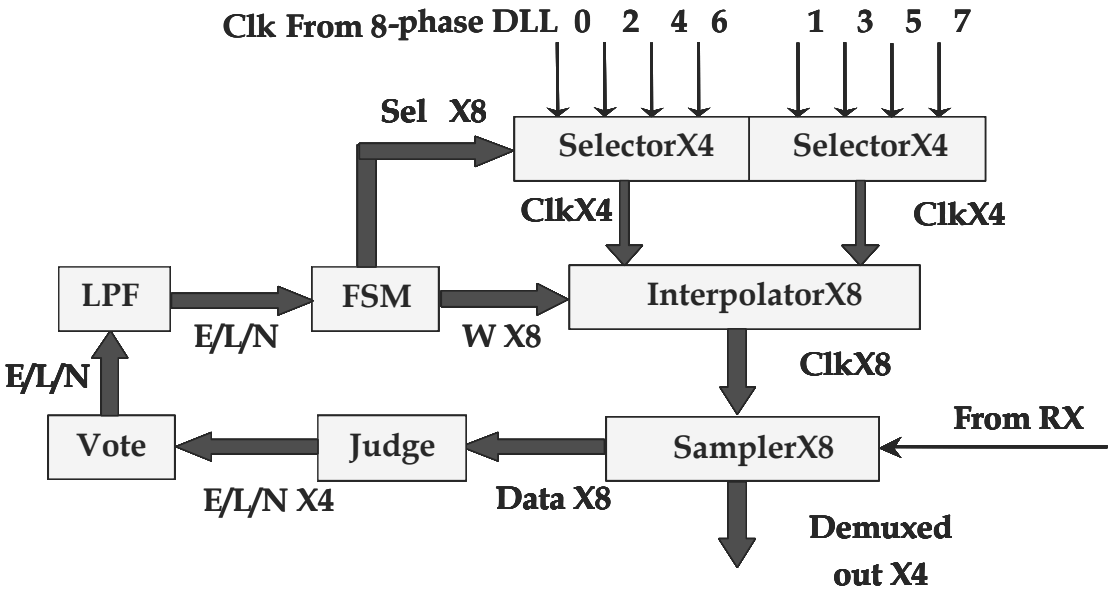


Figure 4.15: Clock phase recovery block diagram

Now, based on the comparison between "edge" and its neighboring "data", we get "Early" or "Late" or "No information" (E/L/N). Based on this, the clocks are adjusted in the correct direction and finally the clock will be aligned with the NRZ data.

The detailed phase recovery process is shown in Figure 4.15. For each 8-phase clock period, there are four "edge" signals, as shown in Figure 4.14, "Edge0", "Edge1", "Edge2" and "Edge3". Each of these "Edge" signals will give us an E/L/N. We do majority voting on these four E/L/N and get a final judgment. Then the E/L/N information is low pass filtered to allow enough cycles for the clock phase to be adjusted. Then a finite state machine generates the control signals based on the E/L/N information and controls the "clock phase adjust circuits", which includes selectors and interpolators. The selector circuit selects two neighbor phases and then the phase interpolator generates even and precise phase steps based on the control signals. The phase resolution by the selector is 1/2 of the clock period. The 8-bit

controlling phase interpolator further increases the resolution into 1/16 of the bit period. For a 5Gb/s data rate, this corresponds to a 12ps phase step or resolution.

4.3.3 Pseudo-random bit sequence (PRBS) data generator and BERT

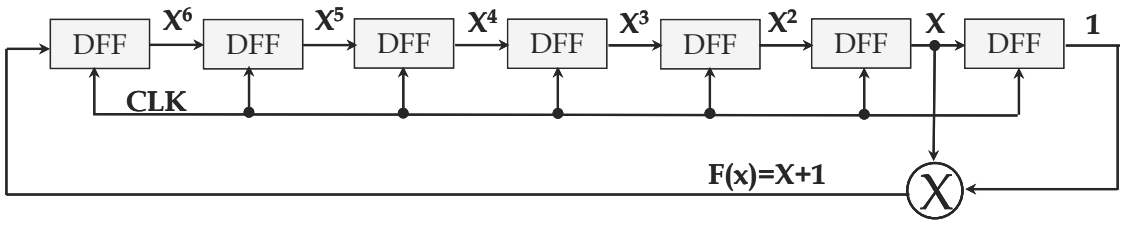


Figure 4.16: 2^7-1 Pseudo-Random Bit sequence generator

A 2^7-1PRBS signal is generated by the linear feedback shift register (LFSR) circuit shown in Figure 4.16. The maximum consecutive '1' is seven while maximum consecutive '0' is six. Comparing with 10b/8b or 5b/4b, where maximum consecutive '0/1' is 5, this PRBS is more random. In designing this LFSR, we need to avoid the all '0' sequence, else this all '0' sequence will remain forever. To eliminate this all zero state, an initial reset is needed. Moreover, the initial reset determines the seeds of the PRBS. In our design, we artificially set different seeds to spread the 4 parallel data paths.

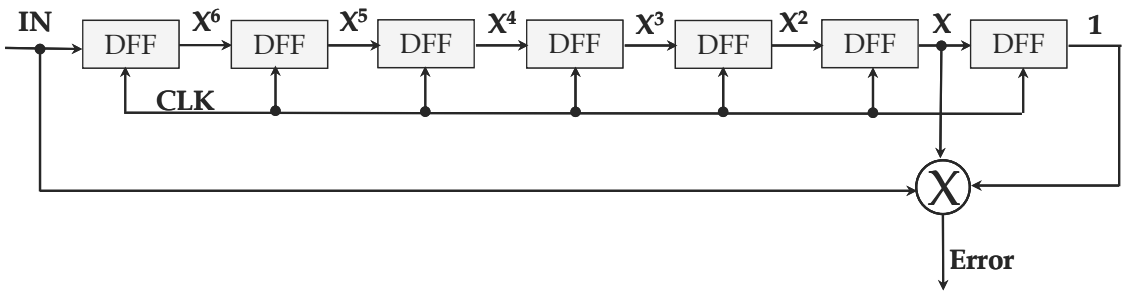


Figure 4.17: Bit error judger

Similar to the PRBS generator, Figure 4.17 shows the bit error tester. It's obvious that as long as the bit sequence satisfy the linear feedback equation at TX side, the error bit will be '0', otherwise the error bit will be '1'.

4.4 Measurement Results

4.4.1 Test Chip

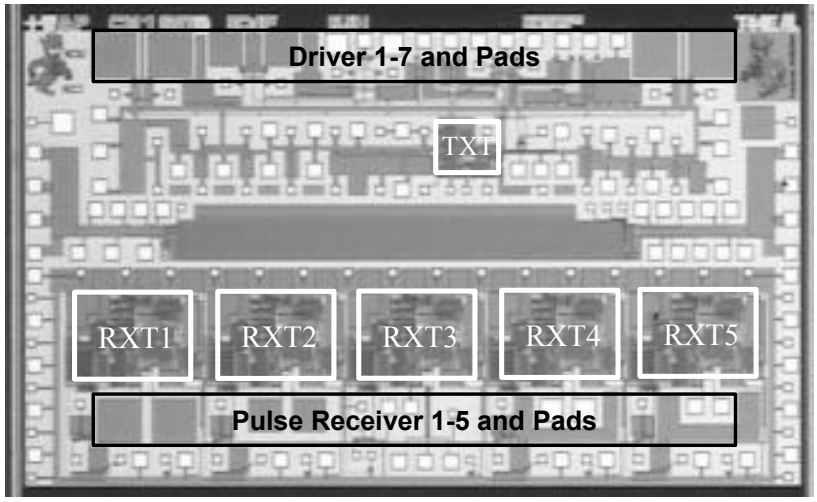


Figure 4.18: Die photo of TSMC 0.18µm CMOS test chip (2mm × 3.5mm)

A 2mm×3.5mm test chip [72] with seven drivers and five pulse receivers was fabricated in the TSMC 0.18µm CMOS technology (Figure 4.18). Each driver and pulse receiver circuit occupies an area of 40µm×20µm and 45µm×15µm, respectively. In this measurement, the AC pads at both transmitter side and receiver side are 60µm×60µm, with 150fF metal-insulator-metal (MIM) capacitors beneath it. The seven drivers share the TX test (TXT) circuitry, including the pseudo-random data generator, multi-phase DLL and multiplexer. Each of the five pulse receivers has its individual RX test (RXT) circuitry, including the clock and data recovery, deserializer and bit error rate tester

4.4.2 Experimental Results

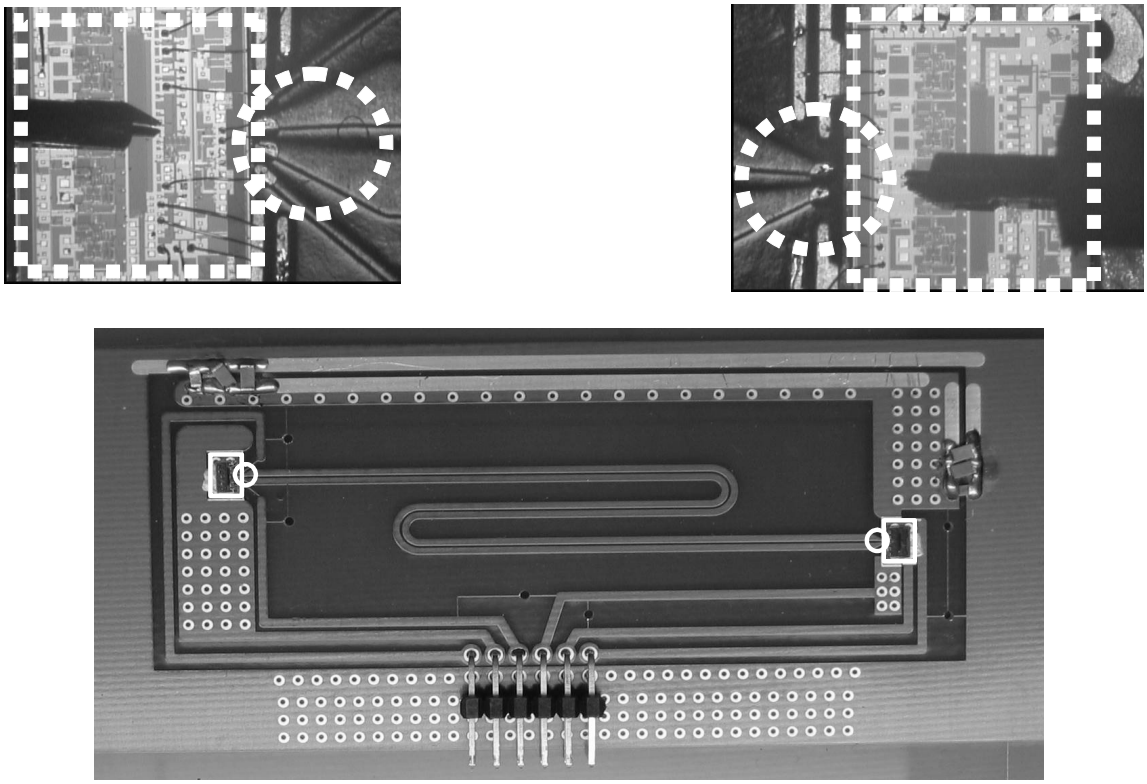


Figure 4.19: Test setup on PCB

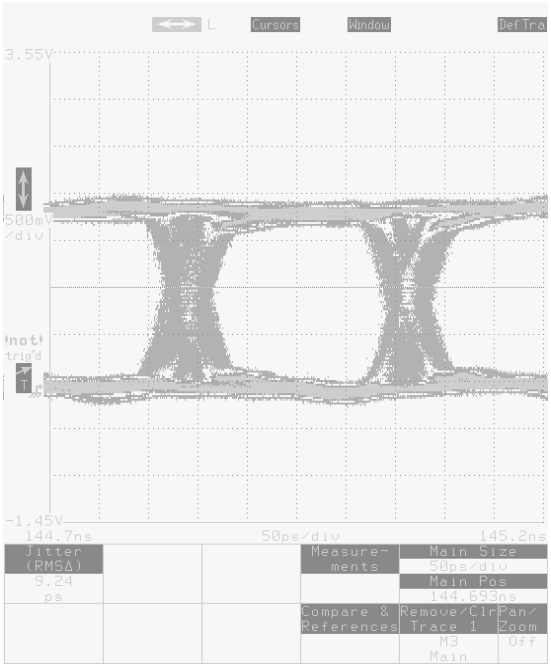
Table 4.2 Chip Summary and Measured Data

Process		TSMC 0.18µm CMOS 1P 6M
Supply Voltage		1.8V
Data Rate		3Gb/s/channel
BER		$< 10^{-12}$
Coupling Caps		60µm × $^{60\mu m}$ on-chip (150fF)
Link		15 cm and ^{50} Ω micro-strip line
Jitter of recover data		7ps RMS
Power (mW)	Pre-Driver and Driver	5
	Pulse RX	10
	Clock, test circuit and buffers	117
	Total	132

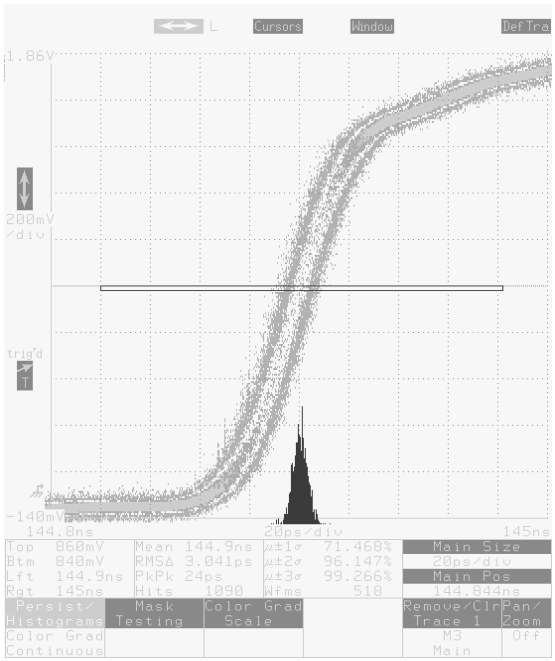
The test chips are measured over an ACCI channel consisting of two 150fF coupling capacitors and a 15 cm long 50Ω copper T-Line on FR4, as shown in Figure 4.19. Power supply and signals are wire-bonded out from the chips. A 0.75GHz clock is generated by an HP8133A Pattern Generator and fed into the chip using a GGB Model 40A probe. Recovered clock, recovered and deserialized NRZ data, and bit error report signals are probed at the receiver chip and monitored using Tektronix 11801B Digital Sampling Oscilloscope.

For a 3Gb/s data rate on each channel, the driver and pulse receiver consume 5mW and 10mW, respectively. All other test circuits in Figure 4.1 except for TX and RX, consume 117mW of power. These test circuits includes the PRBS generator, the multi-phase DLL and the 4:1 multiplexer on transmitter chip. It also includes the samplers, the multi-phase DLL, the clock recovery circuit and the BER test circuit on the receiver chip. Table I shows the chip summary and measured data. BER is estimated to be below 10^{-12} based on an error-free 3Gb/s operation over 10 minutes.

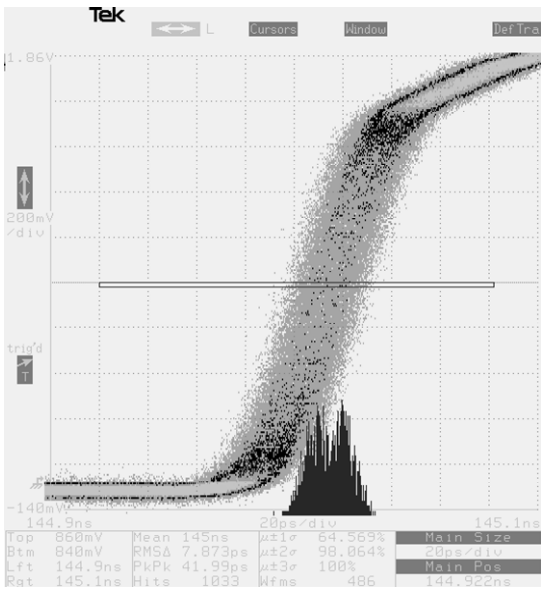
Figure 4.20 shows the measured results: (a) shows the random sequence eye diagram at driver output, (b) shows a quite receiver side clock when clock and data recovery circuitry are turned off, (c) shows the clock recovered by the semidigital dual DLL with a phase interpolation step of 16ps, and (d) shows the recovered and 1:4 deserialized NRZ data with 7ps root mean squared (RMS) jitter.



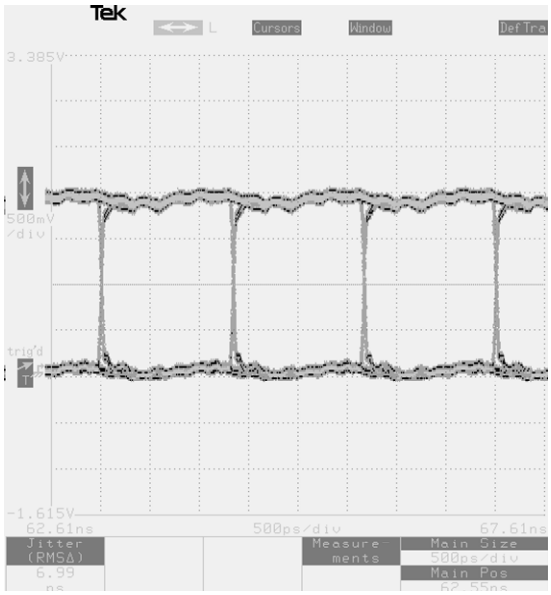
(a) Transmitter output



(b) Receiver side quite clock jitter



(c) Recovered clock jitter



(d) Recovered and deserialized data

Figure 4.20: Measured eye diagram and jitter performance for data and clock

4.5 Conclusion

The key components in the traditional serial link applications are implemented with this ACCI link, including serialization, deserialization, clock generation and clock phase recovery. These traditional circuit blocks, along with the voltage mode driver and the low swing pulse receiver we presented in Chapter 3 are tested in an integrated ACCI serial link system. 3Gb/s/channel communication is demonstrated through this wire-bonded ACCI serial link with two 150fF coupling capacitors and 15 cm long 50 Ω copper T-Line on FR4. BER is measured to be less than 10^{-12} from the on-chip BER tester.

A 150fF on-chip coupling capacitor in wire-bonded ACCI is equivalent to a 93μm×93μm AC pad or a 110μm pitch in flip-chip ACCI, assuming a SiO_2 gap of 2μm. Given the density made possible by ACCI using this pulse receiver, the ITRS milestone in the year 2008 of 110μm pad pitch can be attained in the area array flip chip application.

Chapter 5 High Speed ACCI Bus

5.1 Motivation

Board level capacitively coupled interconnect [6][35][72] and stacked ICs [45][46][48] have been reported as alternatives to physical pin/solder bumps for high density, low power chip-to-chip communications. Although transceiver design of capacitive coupling have been reported extensively, the data rate of capacitive coupled links are still lower than traditional links and the potential crosstalk associated with its return-to-zero (RZ) pulse signaling have not been reported. There are three significant contributions reported in this chapter. First, a fully differential pulse receiver is proposed. This receiver doubles the data rate to 6Gb/s/channel, doubles interconnect length to 30cm, and reduces the power dissipation by 60% to 2mW/Gb/s, when compared to the most recent work [35][72]. Second, the signal integrity aspects and robustness of capacitively coupled links are analyzed. Guidelines on bus design for return-to-zero signaling in ACCI systems are given [78]. Third, a 6-bit wide

differential ACCI bus is demonstrated at 6Gb/s/channel while subject to crosstalk from both its neighboring lines.

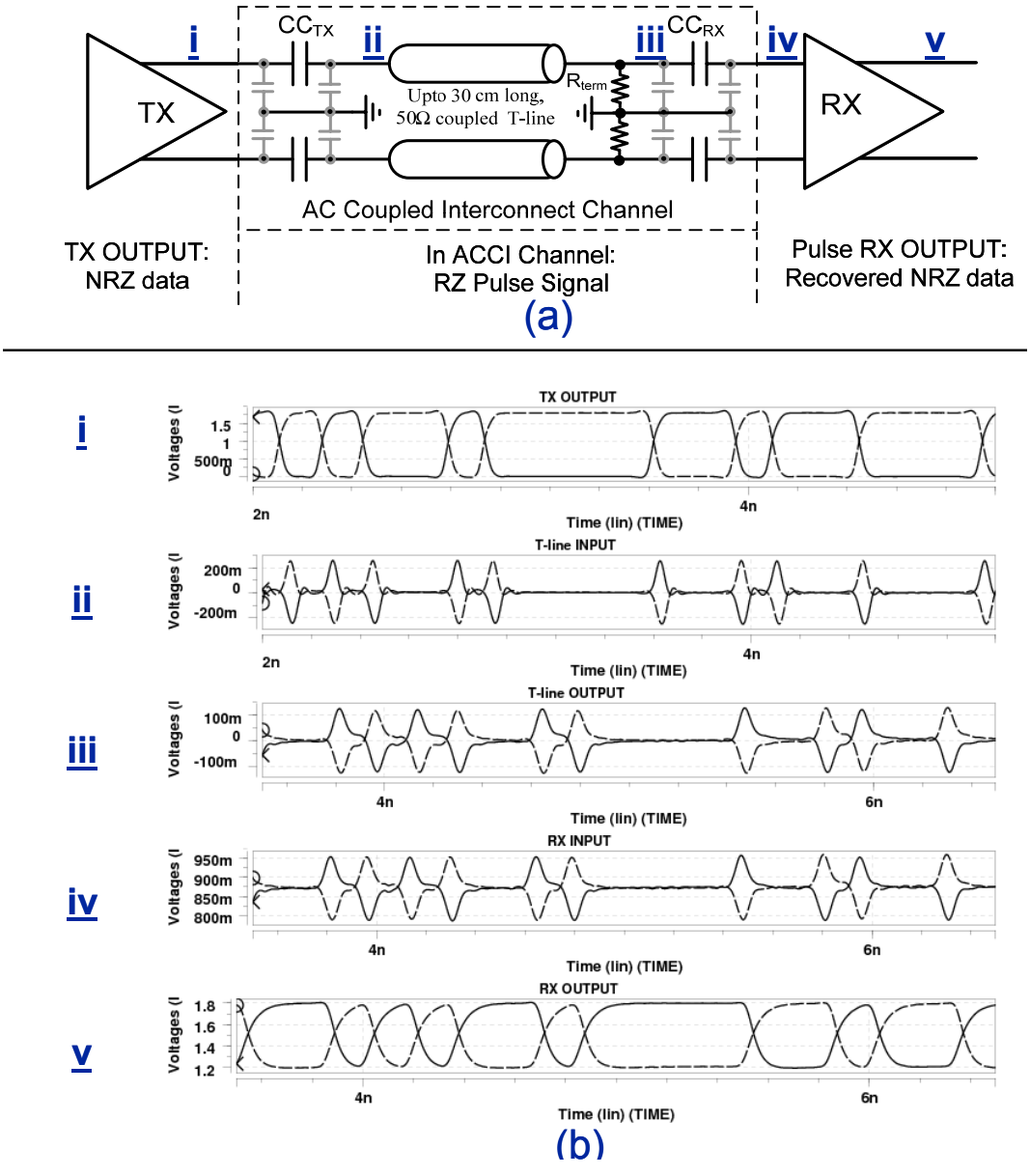


Figure 5.1: (a) ACCI circuit view and (b) Simulated waveforms

Figure 5.1 shows the schematic view of an ACCI link, the waveforms at TX output, T-Line input, T-Line output, RX input and RX output. An ACCI link has a bandpass response and it converts NRZ data into RZ-pulses. Smaller coupling capacitors (CC) are preferred, in order to get higher density AC pads. High data rates and longer T-Lines are preferred to accommodate more applications.

The work in this chapter is to design a higher speed ACCI bus over longer interconnect and smaller coupling capacitors. The key challenge here is to design a pulse receiver to recover NRZ data from the high speed and low swing RZ-pulses.

5.2 Circuit Implementation

5.2.1 Differential pulse receiver

A 120mV$_{ppd}$ low swing pulse receiver (Figure 3.15) was demonstrated in [72] and discussed in chapter 3. However, this pulse receiver has a complementary input stage and is not good at rejecting common-mode noise. The inverter used in this design has a very high gain-bandwidth product at its deep saturation region. It is usually not used as a sense amplifier because of its single ended structure, highly non-linearity and supply noise sensitivity. Figure 5.2 shows the gain of an inverter vs. the DC operation point in 0.18μm CMOS technology with a PMOS to NMOS width ratio of 3/1. As we can see, the gain is highly dependant on the input DC bias. Moreover, the inverter will non-linearly amplify the common mode noise and results in a non-rejectable differential noise at input of the latch. This is one of the reasons why this complementary pulse receiver has low common-mode noise margin, as shown in Figure 3.22. Examples of such common mode noise at receiver input could be

coupled noise from reference plane, crosstalk noise from neighboring lines or vias, and power supply noise.

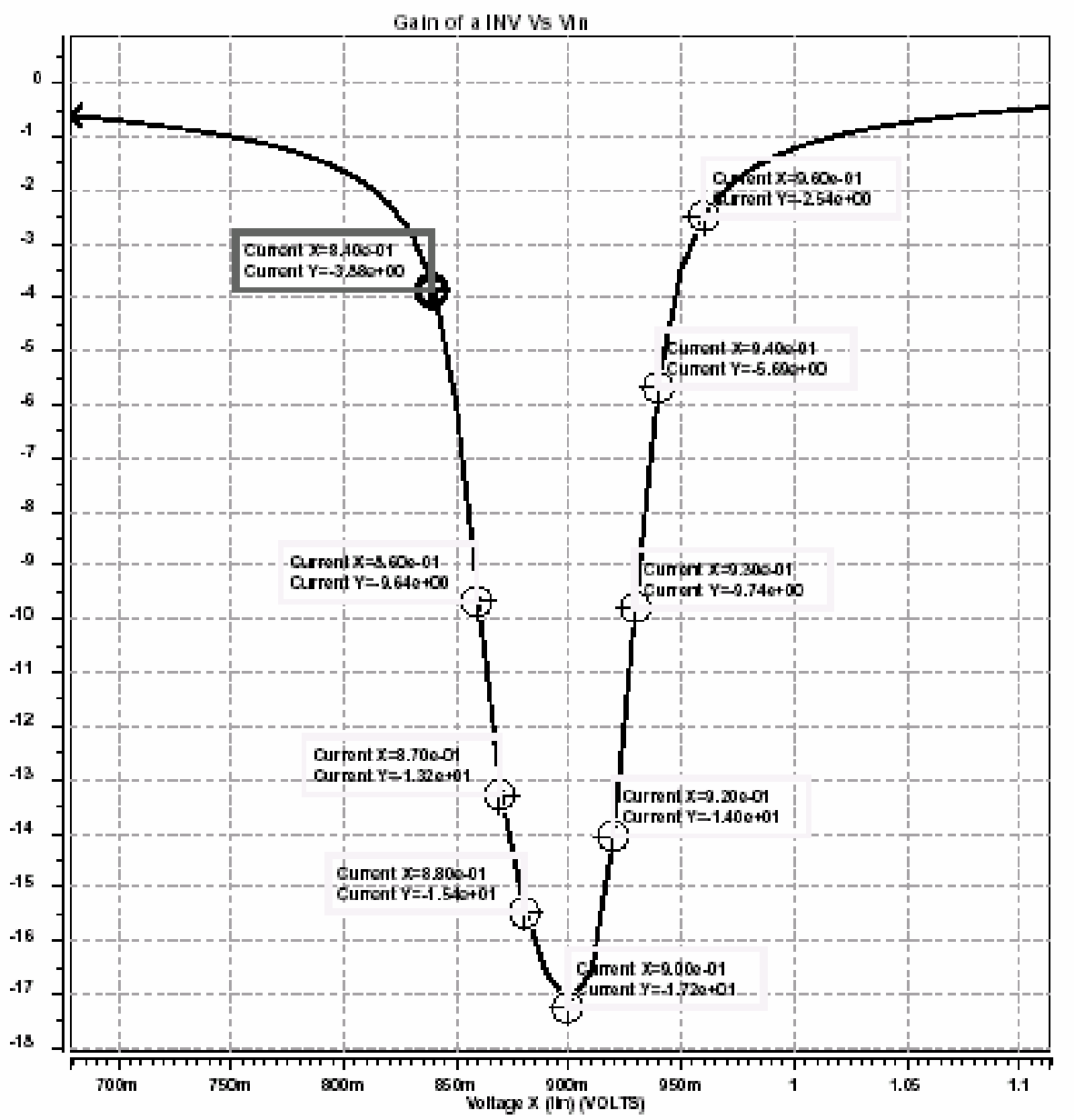


Figure 5.2: INV gain

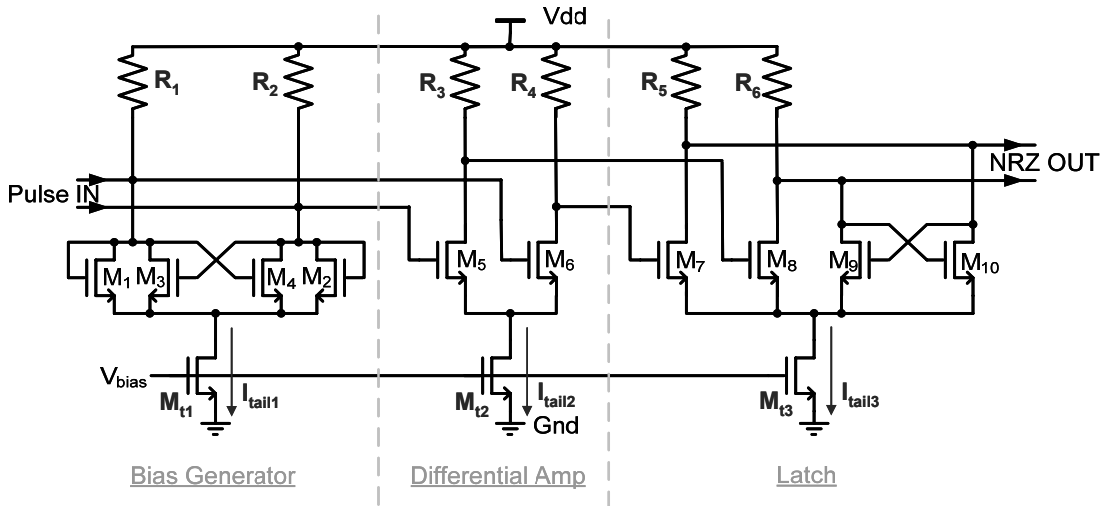


Figure 5.3: Fully differential pulse receiver for AC Coupled Interconnect Bus

The focus of this work is on the ACCI bus, which needs to work in a more realistic (i.e. noisy) environment. As shown in Figure 5.3, the differential pulse receiver proposed here includes three stages: a bias generator that sets up the RX input DC level, which is otherwise not available since the coupling capacitors block the DC level from the T-Line side. Then a simple source coupled inverter amplifies the pulse and feeds it to the latch. Finally, a source coupled latch recovers the NRZ data from the pulse signal. The input sensitivity (input pulse swing requirement) of this differential pulse receiver is $200mV_{ppd.}$

The source coupled logic is used here to provide purely differential signaling to reject common-mode noise in both the signal path and from the power supply. Instead of a PMOS load, pull up resistors are used here to provide more linear gain and higher bandwidth operation.

Bandwidth, output signal swing, and power dissipation need to be considered in designing this source coupled logic circuitry. The bandwidth is mainly determined by the output pole at

$\frac{1}{R \cdot C}$, where C is the parasitic capacitance at the output node and R is the pull-up resistance. The output voltage range is from V_{dd} to $(V_{dd} - R \cdot I_{tail})$, with a swing of $R \cdot I_{tail}$. The power dissipation is determined by the tail current I_{tail}.

The design trade-offs are between the bandwidth, signal swing and power dissipation. For example, to increase the bandwidth while maintaining the output swing, R needs to be reduced and thus I_{tail} needs to be increased. This increases power dissipation. There is not a method to improve one of these three parameters without sacrificing one of the other two. Based on the bandwidth requirement and the signal swing requirement, the power dissipation is determined.

In the bias generator, a bias level is set up through the pull-up resistors R_1 and R_2 (R_1=R_2), and the diode-connected NMOS transistors M_1 and M_2. The two paths share the tail current I_{tail1} and thus the bias level is $(V_{dd} - 0.5 \cdot R_1 \cdot I_{tail1})$. The two cross-coupled NMOS transistors M_3 and M_4 provide positive feedback and thus amplify the differential input voltage.

The differential amplifier is the simplest source coupled logic circuit. The gain is determined by the tail current I_{tail2} and the bandwidth is determined by the pull-up resistance R_3 and R_4 (R_3=R_4) and the parasitic capacitance on output nodes. The parasitic capacitors come mainly from the gate capacitance of the next input stage M_7 and M_8. Based on the bandwidth requirement and the parasitic capacitance, the pull-up resistance value can be determined. Based on the gain requirement, the tail current I_{tail2} can be determined.

In the latch structure, M_7 and M_8 serve as edge detectors. M_9 and M_{10} maintain the previous state until the next pulse edge is detected by M_7 and M_8. The design trade-off here is between

the bandwidth and robust latch operation. Strong M7 and M8 help improve the robustness of latch operation. The design rule is to first ensure the robustness of latch operation and then increase the bandwidth. Typically, M_9 and M_{10} are two times wider than M_7 and M_8 to ensure the latch operation.

Similar as the simulations done in chapter 3, the common-mode noise margin for this fully differential pulse receiver are shown in Figure 5.4. The worst common-mode noise margin is 140mV for the fully differential pulse receiver and 60mV for the complementary pulse receiver. The better common-mode noise rejection performance makes this differential pulse receiver suitable for a noisy ACCI channel.

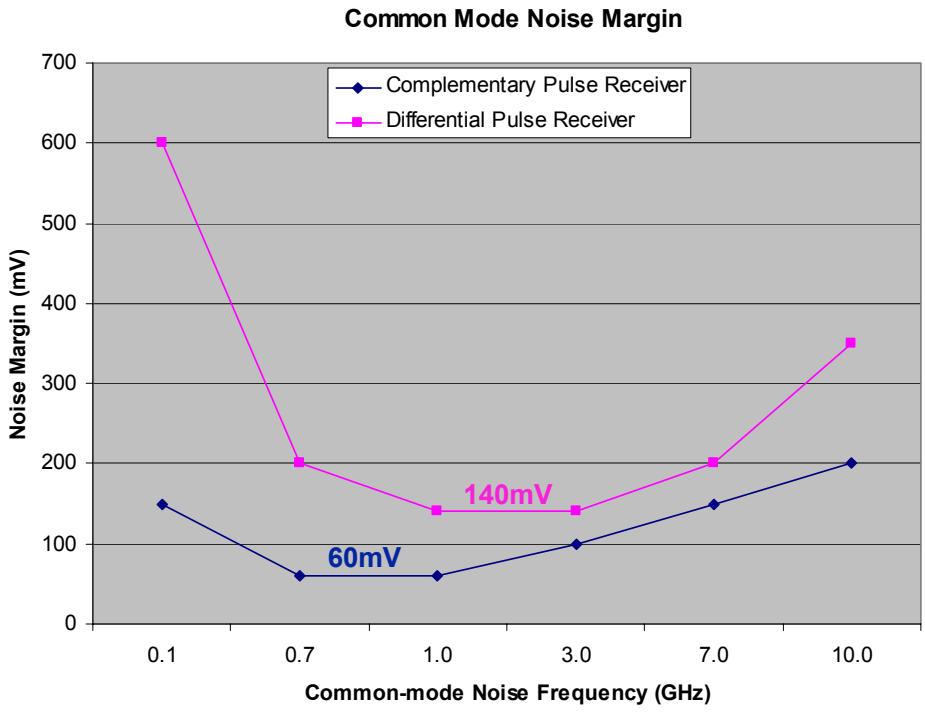


Figure 5.4: Common-mode noise margin comparison: complementary pulse receiver versus differential pulse receiver

5.2.2 Bias Voltage Generator

The pull-up resistors are implemented using poly resistors. In this CMOS process, the poly resistors used here have large process variations on the resistance value (0.8X to 1.2X). To accommodate the resistor process variation corners, a simple feedback circuit is used to track the resistor process variations, as shown in Figure 5.5. V_{ref} is the reference voltage generated by a bandgap reference circuit. R_S is implemented using the same poly resistor as the pull up resistors R_L. Assume R_S and R_L will vary linearly at same direction, the operational amplifier at the left side will force $R_S \cdot I_0 = V_{ref}$. After the current mirrors, $R_L \cdot I_2$ will be a constant value, which is independent of the resistor variations. Thus the output swing of the source coupled logic will remain same regardless of the resistance variations.

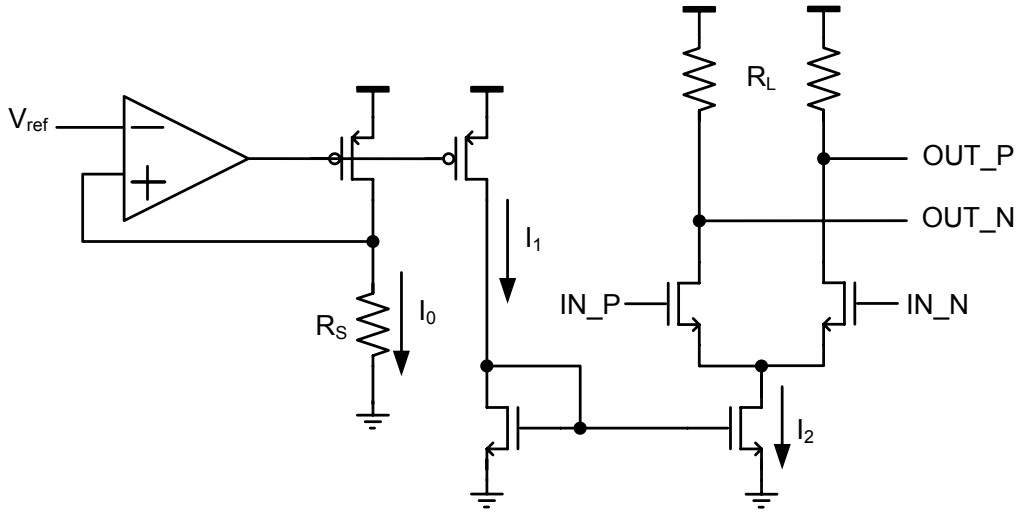


Figure 5.5: Adaptive bias voltage generator to track the resistance variation

5.3 Signal Integrity on ACCI Bus

5.3.1 Cross talk of ACCI Bus

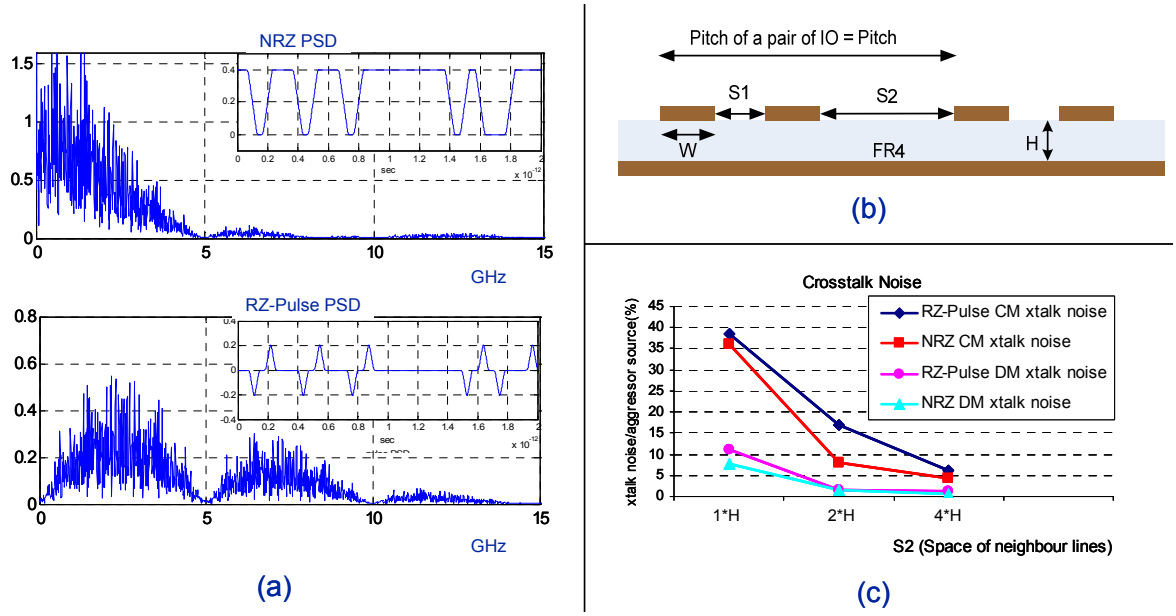


Figure 5.6: (a) Power spectrum density of NRZ and RZ pulses, (b) Cross-section view of coupled micro-strip line, (c) Cross Talk Noise of NRZ and RZ-Pulse signal

RZ pulses have higher bandwidth components than NRZ signals, as shown in Figure 5.6(a). This could increase crosstalk effects relative to NRZ. To analysis this, a group of coupled microstrip lines are modeled using a 2D field-solver to extract the line-to-line coupling capacitance and inductance. Line width W, coupled line space W, and dielectric thickness H are all set to 5mil. The neighboring line spacing, S2 is set to 1*H, 2*H and 4*H (H=5mil). Spice simulations are performed to compare the crosstalk effect of RZ-pulses to NRZ signals, as shown in Figure 5.6 (b). The top two curves show the common-mode (CM) xtalk noise generated by RZ pulses and by traditional NRZ signals. The bottom two curves show the differential-mode (DM) xtalk noise generated. From the simulations, the xtalk noise

generated by RZ-pulse signals and by traditional NRZ signals are similar as long as the space between two coupled lines is greater than 2*H (10mils).

The receiver can reject most of the common-mode noise. But the differential noise is more critical because it will directly reduce the noise margin at the input of the receiver. Fig. 3(c) shows that as long as the neighboring T-Lines are spaced more than 2*H (10mil), the differential xtalk noise will be controlled to within 3% of the aggressor's swing. To get good isolation from the xtalk generated by RZ-pulse signals, 4*H (20mil) of space is needed.

5.3.2 Switching noise

The effects of power supply switching noise on signal integrity limit the level of system integration. In ACCI systems, it is important to reduce the self-generated switching noise at the transmitter side, and improve noise immunity at the receiver side.

Due to its high input impedance, ACCI channels allow the use and also require a voltage mode driver. Voltage mode drivers save significant power (Figure 3.11) but also generate more switching noise than traditional current-mode drivers. Figure 5.7 (a) shows the switching noise that is generated due from the inductance in power supply network. The more inductance, the higher di/dt, and the more switching noise will be generated on the on-chip power supply network. Voltage mode drivers consume power supply current only at data transition edge. This means that voltage mode drivers generate high di/dt and thus high switching noise. The higher output edge rate, the more switching noise a voltage mode driver will generate. However, the traditional current-mode driver consumes constant power supply current over the whole bit period because it steers the tail current from one side to the other,

thereby, generating significantly less switching noise. Figure 5.7 (c) shows the switching noise generated by a complementary voltage mode driver use in ACCI, and a differential mode current-mode driver for traditional channel, respectively. The complementary voltage mode driver with capacitive loading generates five times the switching noise on the power supply than the current-mode driver.

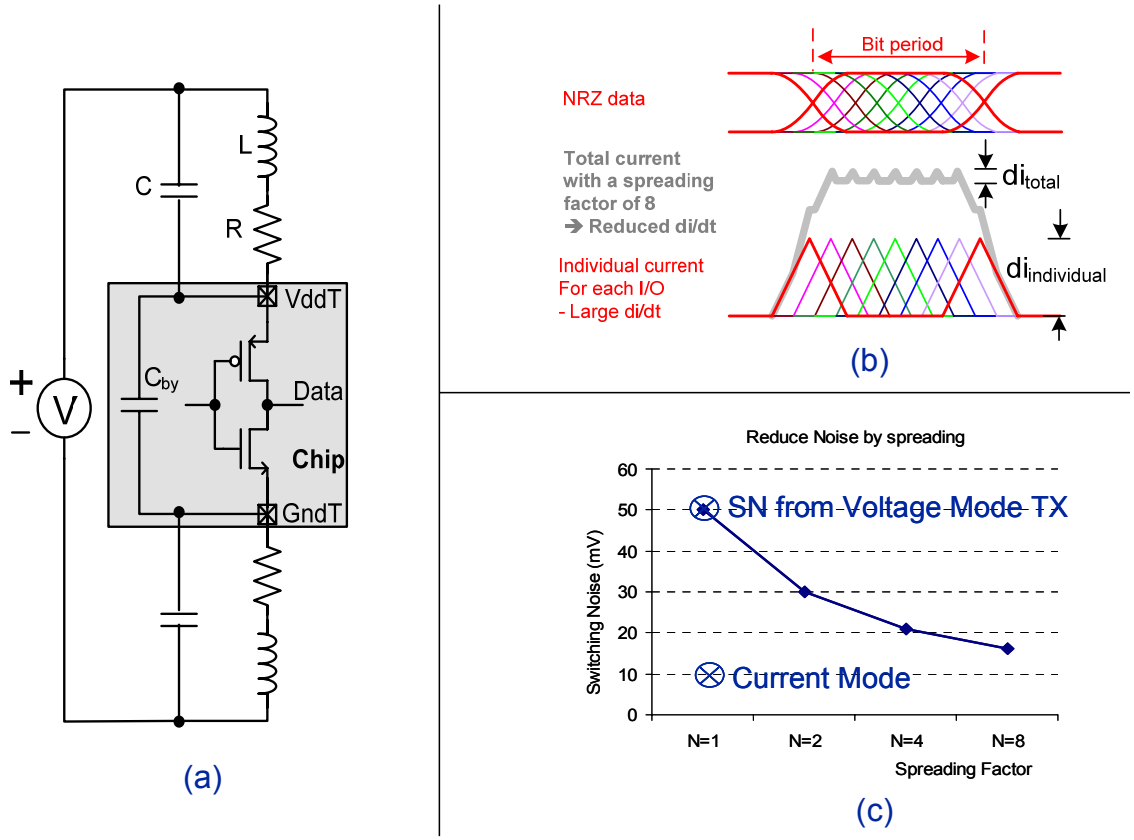


Figure 5.7: (a) Voltage mode driver cause switching noise, (b) Reduce switching noise by spreading transition edges, (c) Switching noise largely reduced by spreading I/O edges, according to simulations

This self-generated switching noise in voltage mode driver can be reduced in several ways. Sufficient use of on-chip and off-chip bypass capacitors and large numbers of low inductance power supply pins are preferred, which is actually available in ACCI systems. AC signal pins are built with very high density so that most of the chip surface area is available for power

supply pins. In addition, slew control can be used at transmitter side to slow down the signal edge rate and thus reduce the switching noise. This is feasible for lower signaling rates or for shorter link length communication.

Another more efficient and low cost way, proposed here, is to spread the transition edges among all I/Os. Since the switching noise only happens at data transition edge for all the channels, it is possible to average the din/dt (n is the number of channels associated with edge spreading) by spreading the transition edges of the data. Simulations show that power supply switching noise is reduced significantly by using this edge spreading method as shown in Figure 5.7 (c). When a spreading factor of eight is used, the switching noise generated by the voltage mode driver will be similar to that generated by the current-mode driver. This method is especially efficient when the data of the channels are independent. In serial link applications, spreading of edges will not affect the timing constraint since at receiver side; each channel will be individually recovered from RZ-pulse signals to NRZ data by the asynchronous pulse receiver and then sent to individual clock and data recovery circuits.

Switching noise can also come from other parts of the chip/system. Common-mode noise coupled from transmission lines at board level or multi-chip module (MCM) level could be larger than the actual signal itself, which means a SNR less than 1. Fortunately, the noise is usually common mode and can be rejected by a differential receiver. This requires good noise rejection circuit at receiver side.

5.4 Test and Measurement

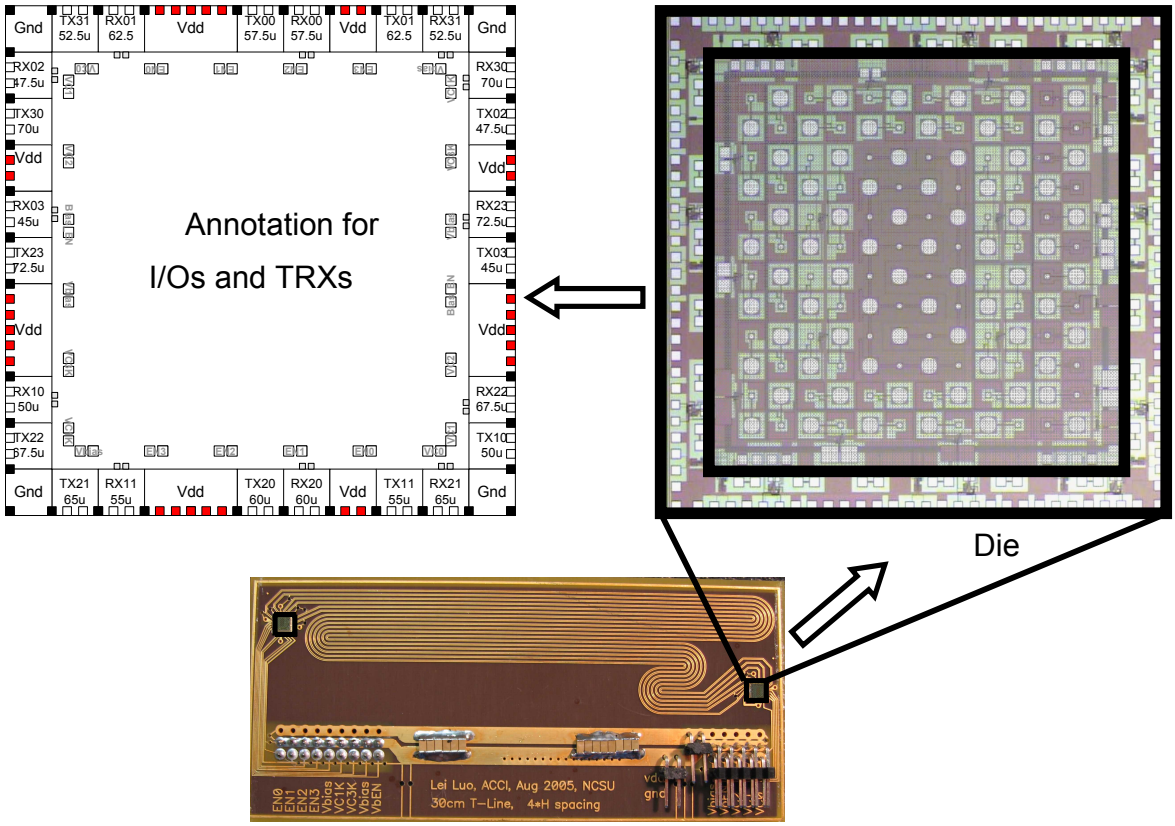


Figure 5.8: Test PCB with 6 pairs of meandered 30cm ACCI channels; the Die photo of CMOS 0.18µm test chip (3.3mm by 3.3mm)

A 3.3mm×3.3mm test chip with twelve TX and RX circuits was fabricated in TSMC 0.18µm CMOS (Figure 5.8). Each TX and RX layout occupies an area of 40µm×20µm and 60µm×60µm, respectively. All the TX, RX, coupling capacitor landing pads and power supply pads are located around the periphery of the chip. The coupling capacitors' vary from 85 - 175fF to determine the range for valid operation. The inner chip area is for the flip chip test of capacitive coupling links.

Two chips were wire-bonded to a FR4 PCB. The ACCI link was composed of a MIM capacitor and the coupled micro-strip T-Line on FR4. Two boards were tested, one with 6-bit wide, 30cm long T-Lines (Figure 5.8), with a S2 (neighbor space) of 4*H. The other board had 6-bit wide, 20cm long T-Lines, with S2 equal to 3*H. For both boards, the 6 channels worked simultaneously for 36Gb/s, while all were subject to crosstalk noise and switching noise.

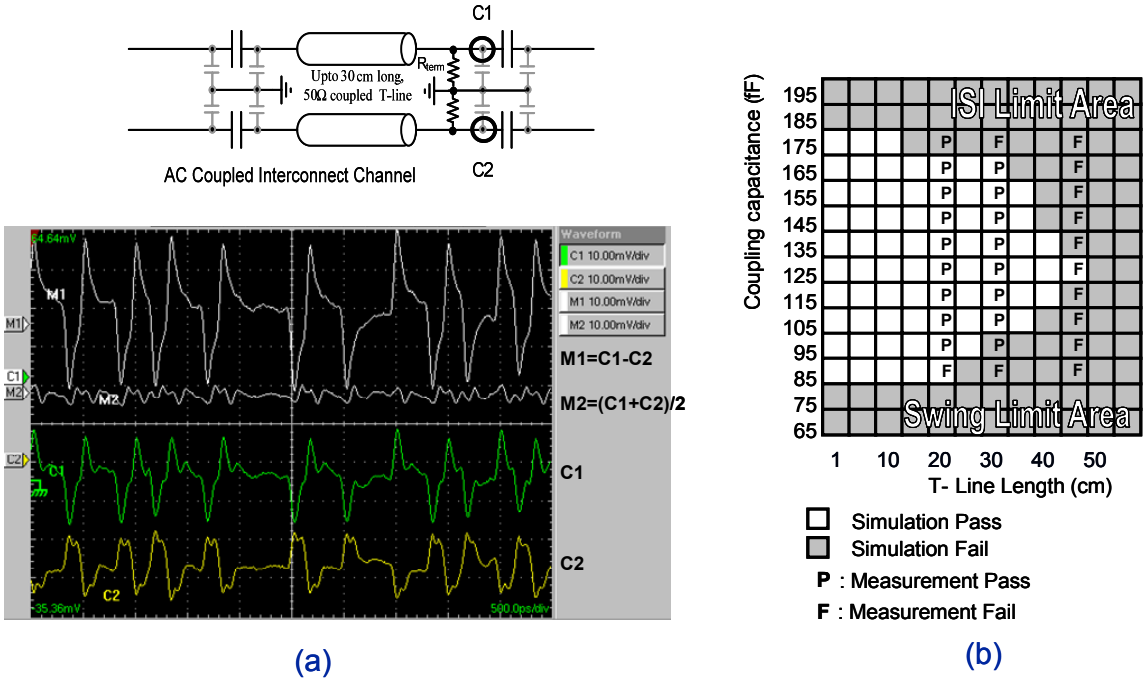


Figure 5.9: (a) Measured 6Gb/s/Channel RZ-Pulse signal after transmission line
(b) Simulated and Measured Shmoo Plot

Figure 5.9 (a) shows the measured RZ pulse signals (C1, C2) just before the RX side coupling capacitor. It also shows the differential mode (M1) and common mode (M2) of the two pulse signals. The swing and width of the pulse depends on the size of the coupling capacitors and T-Line length. Fig. 4(b) shows a shmoo plot, where the grey and white block

indicate simulated pass and fail for a range of CC and T-Line values. The "P/F" shows the actual measured pass/fail values. The measurement results agree with the simulation results, showing two possible failure regimes. One is the ISI limited area, which is limited by large coupling capacitors or a longer T-Line. The other is the swing limited area, which is limited by small coupling capacitors or a longer T-Line. For the test case with 45cm T-Line, the pulse swing at receiver input was not enough in both simulation and measurement.

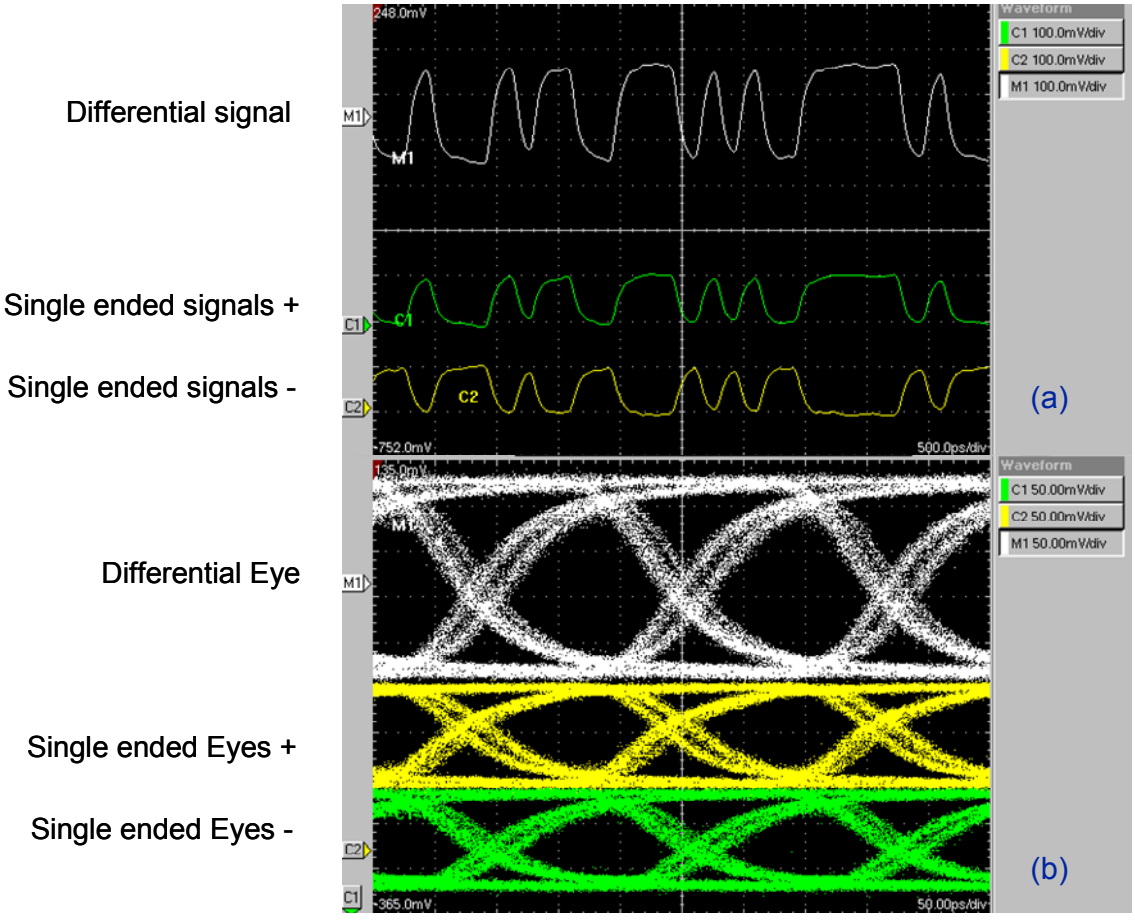


Figure 5.10: Measured 6Gb/s/Channel Recovered NRZ data (a) transient waveform of a repeated pattern; (b) Recovered Eye diagram of a 2^7-1 Pseudo-Random Bit Sequence

Figure 5.10 shows the differential signal and single ended signal of the measured data pattern at the pulse receiver output and also the eye diagram based on a PRBS-127, all running at 6Gb/s/channel with no detectable errors.

36Gb/s chip-to-chip communication is achieved over a 6-bit wide ACCI bus, with coupling capacitors as small as 95fF, using a 30cm microstrip line on FR4, while subject to crosstalk and switching noise. The total transceiver power consumption is only 12mW per I/O at 6Gb/s/channel (PRBS-127). This work shows that capacitively coupled links can achieve the same data rates as conductive links with low power dissipation and with similar crosstalk and switching noise effects.

Technology		TSMC 0.18um CMOS
Area		3.3mm by 3.3mm
Power Dissipation	TX	5mw
	RX	6.8mw
	12 TRX for 72Gb/s	141.6mw
	TRX Per Gb/s	1.97mw/Gb/s
AC signal I/Os (with TRX)	Wirebond test	12
	MCNC Flip chip test	7
	Endicott Flip chip test	7
	Total	26
Max Bandwidth	Wirebond test	72Gb/s (partially measured: 36Gb/s)
	Flip-chip	84Gb/s
	Total	156Gb/s
Max data Rate per channel		6Gb/s
Min data Rate		DC (50MHZ measured, limited by signal source)

Table 5.1: Performance matrix of 12 bit wide, 36Gb/s ACCI bus

5.5 Higher speed pulse signaling over ACCI

To push ACCI links into even higher data rates with more advanced CMOS technologies, simulations are performed to show the feasibility. The main concerns for scaling are data rate

scaling, power supply scaling, power consumption scaling and area scaling. An ACCI link is demonstrated at 12.5Gb/s date rate with 90nm CMOS technology. The simulations also shows a scalable power supply voltage, scalable power consumption, scalable circuit area, with low BER and robust operation.

5.5.1 12.5Gb/s pulse signaling with 90nm CMOS

To investigate ACCI with higher data rate communication, simulations are performed with the same transceiver circuitry but with 90nm CMOS technology. Except the transistor size change, some other parameters need to be taken care of. These parameters include coupling capacitor size, pulse swing, T-Line length, data rate and power dissipation.

To get a low BER target, SNR needs to be maintained as that in 180nm design. This requires coupling capacitance to maintain a similar value as that used in the 180nm design. The coupling capacitor size is not scaling with technology, just like the I/O pads is not scaling down in traditional design.

For 90nm CMOS, power supply voltage drops to 1V. However, the edge rate at driver's output is much higher than that of 0.18um CMOS. This high edge rate directly converts into more pulse swing after the first coupling capacitor, which acts as a differentiator. This means that the power supply voltage scaling will not affect the ACCI link. While in traditional conductive links, the transmitter output signal swing is largely dependant on the I/O power supply voltage since the devices in the output buffer need to stay in the saturation region. For example, with 90nm CMOS, the traditional current-mode driver already runs out of voltage headroom. The common solution in industry is to use another higher power supply dedicated

for the I/O buffer. ACCI can tolerant lower supply voltage operation and thus save this dedicated high voltage power supply. This benefit of ACCI was demonstrated in Figure 3.5.

The high edge rate provided by 90nm CMOS enables a 12.5Gb/s data rate communication over ACCI, according to simulation. The key point here is that the pulse width is directly related to the edge rate at driver output. And it is the pulse width which determines the highest data rate with a certain tolerable ISI. The bottom three eye diagrams in Figure 5.11 shows the NRZ data recovered by the pulse receiver. As we can see, for small coupling capacitor size and short T-Line, the eye diagram is wide opened as long as the swing is enough. For large coupling capacitor size and long T-Line, ISI can be observed. Simulation shows the power dissipation drops to 7mW/12.5Gb/s/channel or 0.56mW/Gb/s. This power/Gb/s number is less than one third of that in 0.18um CMOS technology. The power saving comes mainly from Vdd scaling for both transmitter and receiver circuitry. For the differential receiver design, the power consumption is independent with the data rate. Thus the 12.5Gb/s operation also helps to reduce the power/Gb/s for receiver.

Figure 5.12 shows the shmoo plot for 12.5Gb/s operation. Comparing with the shmoo plot in Figure 5.9, this one has similar coupling capacitor size range but shorter T-Line length. The main reason is because of the high data rate and thus more ISI. Higher data rates means less bit period and thus less ISI margin for RZ pulse signaling. This is the main reason the T-Line length being limited comparing with 6Gb/s operation in 0.18um CMOS. For lower data rate operation, this shmoo plot pass region can be extended.

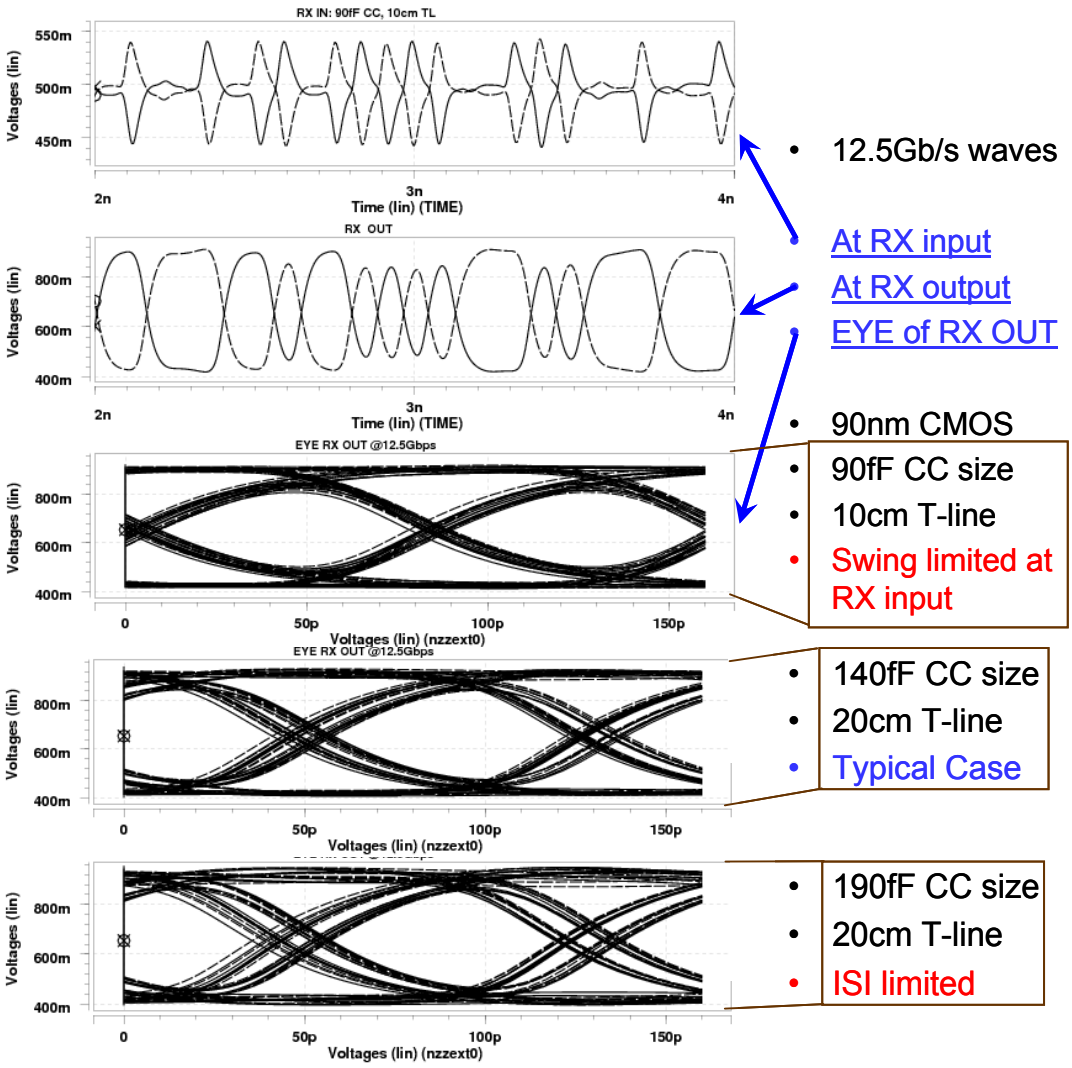


Figure 5.11: Simulated waveforms and Eye diagrams at RX output

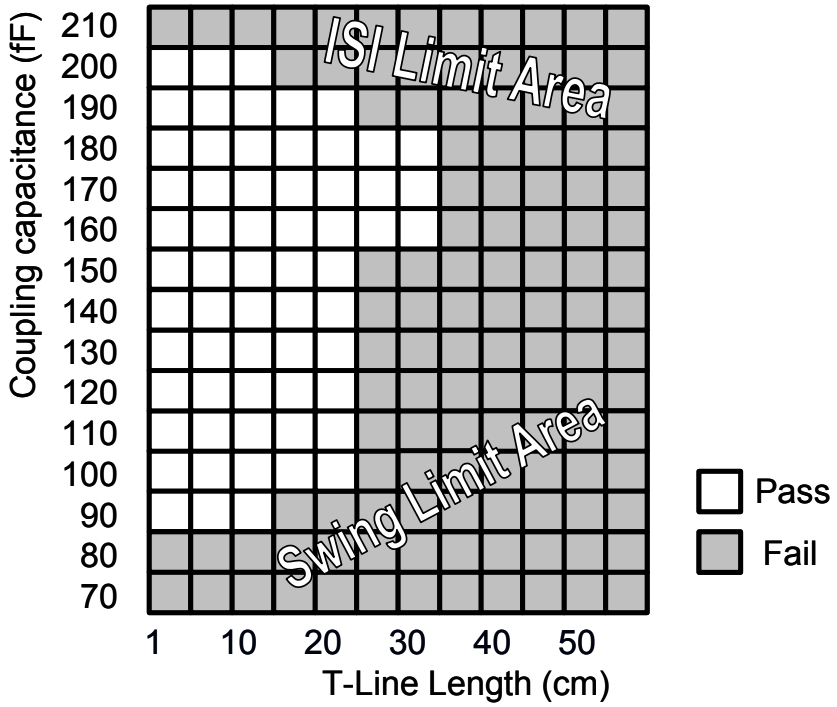


Figure 5.12 Simulated Shmoo for 0.75UI opening @ RX OUTPUT @ 12.5Gb/s with 90nm CMOS

5.5.2 20Gb/s pulse signaling is expected with 65nm CMOS

To explore even higher data rates, the 65nm CMOS technology is emulated by assuming 0.7V Vdd and 30ps rising/falling edge at transmitter output. Based on the receiver threshold voltage in 180nm and 90nm CMOS circuits, the pulse receiver input threshold is also estimated as 80mV. Since the transistor models are not available, the ACCI channel is simulated without the transceiver circuitry, at 20Gb/s data rate, as shown in Figure 5.13. The corresponding waveforms are shown in Figure 5.14. From the waveform at the receiver input, there is no obvious ISI and it is assumed that the pulse receiver can recover the NRZ as long as the pulse swing is larger than the input threshold level, which is estimated as 80mV.

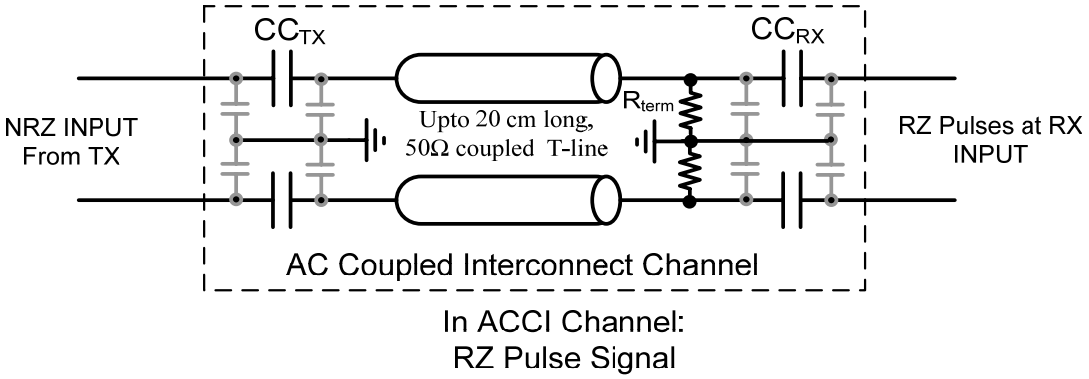


Figure 5.13: Simulation setup for 20Gb/s operation

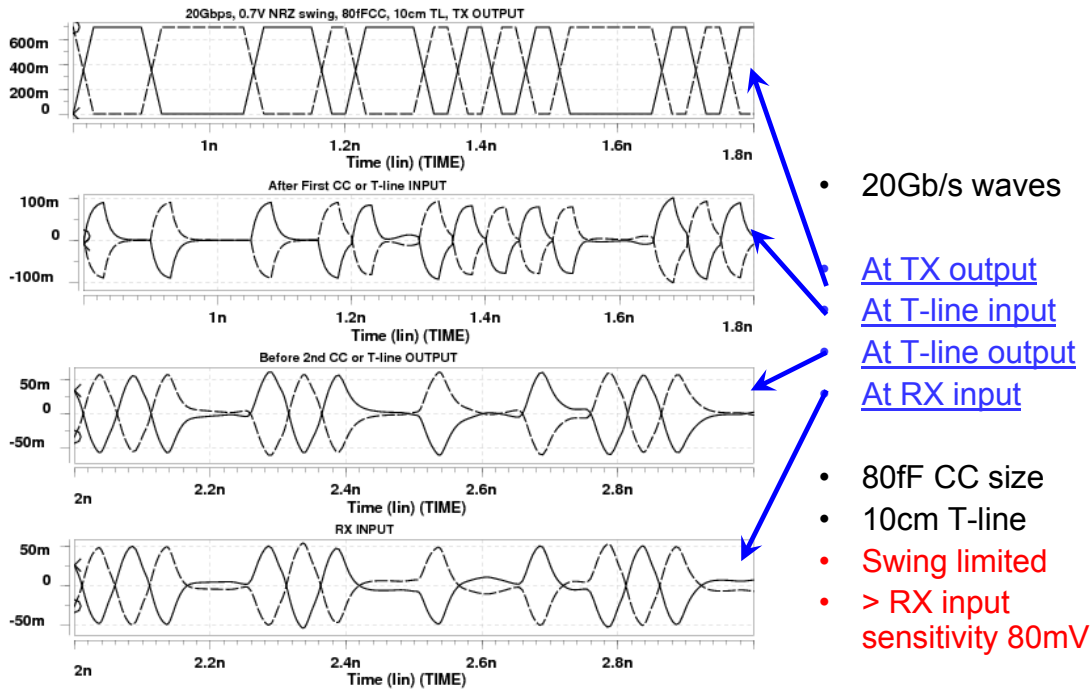


Figure 5.14: Waveforms for 20Gb/s operation

At 20Gb/s, the ISI becomes more critical, as shown in the eye diagrams in Figure 5.15. The first three eye diagrams are with an ACCI channel with 80fF coupling capacitance and 10cm T-Line. The first three eye diagrams show the signal at T-Line input, T-Line output and receiver input, individually. There is negligible ISI at receiver input and the pulse swing is

100mV. The last three eye diagrams are with 140fF coupling capacitance and 20cm T-Line. The eye diagram at T-Line output shows large ISI. Part of this ISI is filtered by the second coupling capacitor, but the receiver input still has significant ISI, which will directly transfer to jitter at recovered NRZ.

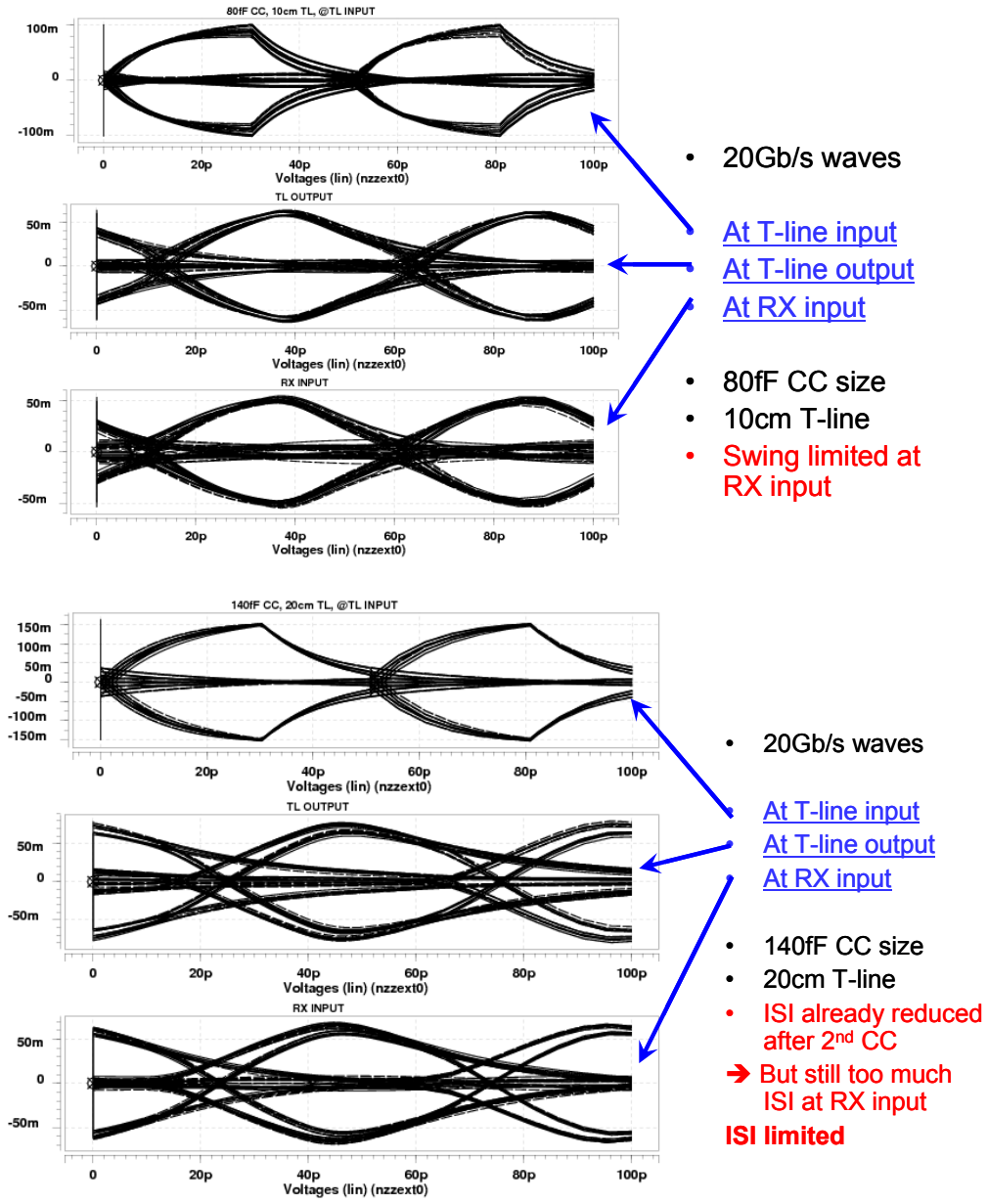


Figure 5.15: Eye Diagrams for 20Gb/s operation

Based on the simulations, a shmoo plot for 20Gb/s operation over ACCI is shown in Figure 5.16. The ISI limit pushes the coupling capacitor size to be smaller and thus limits the pulse swing at receiver input, which limits the T-Line length. If a simple FFE is implemented before the pulse receiver to filter the ISI, the pass area is expected to expand to the "ISI limited area". This suggests using simple equalization at receiver front end for 20Gb/s data rate over ACCI.

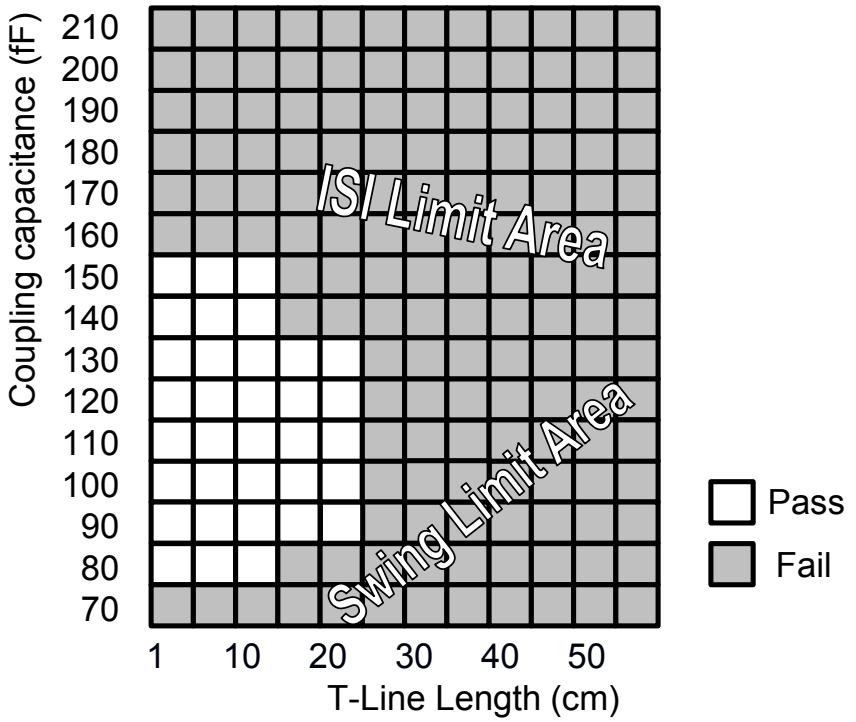


Figure 5.16: Simulated Shmoo for 0.75UI opening @ RX output @ 20Gb/s

5.5.3 Summary of technology scaling

The ACCI channel provides enough bandwidth to enable 20Gb/s data rate communication. The bandwidth and attenuation is defined by the coupling capacitor size and T-Line length. To tolerant a wide range of coupling capacitor size and T-Line length, simple equalization at receiver side front end is needed for 20Gb/s data rate.

Coupling capacitors are used as passive equalization in ACCI pulse signaling. By using simple FFE equalization to provide part of the equalization, the coupling capacitor can be designed to be larger and thus provide less signal attenuation. This means the T-Line can be longer. So, by using simple FFE, both the capacitor range and the T-Line length range can be extended.

Chapter 6 Conclusions

6.1 Conclusions

1. ACCI provides high density and reliable signal pads for the chip-package interface. (Ch3)

2. In ACCI, passive equalization replaces traditional equalization circuitry. This saves design effort, circuit area and power consumption associated with traditional active equalization. (Ch3)

3. ACCI uses a voltage mode driver, which provides higher edge rate output and consumes less power , when compared with traditional current-mode drivers. (Ch3)

4. The complementary pulse receiver achieves highest data rate (3Gb/s) and lowest pulse swing requirement (120mV_{PPD}), when compared with previously reported capacitively coupled systems. This low-swing pulse receiver enables ACCI with smaller coupling capacitance which translates to higher I/O density. It also enables ACCI over longer T-Line lengths than previous works. (Ch3)

5. 3Gb/s/channel communication was demonstrated through the wire-bonded ACCI serial link with two 150fF coupling capacitors and 15 cm long 50 Ω copper T-Line on FR4. This 150fF on-chip coupling capacitor in wire-bonded ACCI is equvialent to a 93 μm × 93 μm AC pad or 110 μm pitch in flip-chip ACCI, assuming a SiO_2 gap of 2 μm. (Ch4)

6. Signal integrity in ACCI systems is controllable. The self-generated switching noise can be controlled by on-chip decoupling capacitors, by slew rate control and by spreading transition edges across I/Os. The crosstalk noise of RZ-pulses can be reduced by proper design of the T-Line. (Ch5) The power supply noise rejection ratio is 0.1ps/mV for 60mV pusle swing, and 0.13ps/mV for 120mV pusle swing at receiver input node. Larger pulse swings are prefered to get better supply noise rejection ratio. (Ch3)

7. A 6-bit wide differential ACCI bus was demonstrated at 6Gb/s/channel. A fully differential pulse receiver was designed to achieve better common-mode noise rejection and higher bandwidth. (Ch5)

8. Two pulse receivers are designed and tested in this work, the complementary pulse receiver and the differential pulse receiver. The complementary pulse receiver requires less pulse swing at its input. The differential pulse has better common-mode noise rejection performance and dissipates less power. (Ch3 and Ch5)

9. For a long channel (20cm to 30cm) ACCI, single side termination is preferred because the swing is the limiting factor. For a short channel (15cm or less) ACCI, double side termination is preferred as long as the pulse swing at receiver input is enough. Short ACCI channels are more sensitive to reflection noise because the reflection noise is not attenuated

as in long ACCI channel. Double side termination also helps reduce the reflection noise due to impedance discontinuity due to vias, connectors and copper trace discontinuities. (Ch5)

10. The ACCI channel provides enough bandwidth to enable 20Gb/s data rate communication. The bandwidth and attenuation is defined by the coupling capacitor size and T-Line length. To tolerate a wide range of coupling capacitor size and T-Line length, simple equalization at receiver side front end is needed for 20Gb/s data rate. Coupling capacitors are used to provide passive equalization in ACCI pulse signaling. By using simple FFE equalization to provide part of the equalization, the coupling capacitor can be designed to be larger and thus less signal attenuation across the coupling capacitors. This means the T-Line can be longer. So, by using simple FFE, both the capacitor range and the T-Line length range can be extended. (Ch5)

6.2 Contributions

1. The ACCI channel was analyzed in three aspects: frequency domain, time domain and pulse eye diagram plot. The equalization concept for ACCI pulse signaling was proposed as well. This helps in designing a robust ACCI link in the initial stage.

2. A complementary low-swing pulse receiver was designed and tested. The lowest input swing requirement was achieved at a 3Gb/s data rate.

3. Design procedures and design rules were proposed for designing capacitively coupled interconnect.

4. A complete 3Gb/s ACCI serial link was design and tested, with multi-phase DLL, clock and data recovery, deserializer and BERT.

5. A 6Gb/s fully differential pulse receiver was designed for a 6-bit wide ACCI bus over 30cm long T-Line, with 2mW/Gb/s power dissipation.

6. The feasibility of 10Gb/s to 20Gb/s operation was demonstrated on ACCI links with more advanced CMOS technology. Design rules for higher data rates were given.

7. Signal integrity issues for ACCI were investigated, including ISI, switching noise, reflections, and crosstalk noise. Techniques and design rules were proposed to improve the ACCI pulse signal integrity.

6.3 Future work

The capactively coupled interconnect research can be extended in many directions, such as noise, partial equalization and CDR for pulse signaling.

6.3.1 Noise

Noise probably has the first priority to be explored in future work. In order to be commercialized, high yield and robust ACCI with 10^{-15} BER need to be demonstrated in real world systems. In addition to the simulation and measurement performed in this work, other factors need to be considered, such as the reflection noise due to vias, connectors and T-Line discontinuities. The power supply noise sensitivity need to be quantified. Technologies like spreading edges and crosstalk noise cancellation need to be designed and verified in silicon.

6.3.1.1 Reflection noise

Vias, connectors and T-Line impedance discontinuities can also cause reflections. The reflection noises associated with these factors need to be investigated. Measurement with

these effects needs to be performed. A decision needs to be made as to whether double side termination is required to reduce the reflection noise. The trade-off between single side termination and double side termination is signal swing versus reflection noise.

It is desirable to measure the S-parameters of ACCI channels with vias, connectors and termination resistors (at either side and at both sides). Then use the measured S-parameters into simulation.

6.3.1.2 Spreading edges for switching noise

The spreading edge technology is proposed and simulated but hasn't been tested in measurement. It is desirable to test this method in silicon and quantify how much it can reduce switching noise. Note the spreading edge method functions best if all I/O data patterns are independent with each other. So it is desirable to test different cases, where the data patterns of I/Os have different correlation co-efficients.

6.3.1.3 Noise sensitivity and Jitter transfer

The jitter transfer analysis from both power supply noise and transmitter output jitter need to be measured. On-chip power supply and substrate noise generator need to be designed on chip to measure the power supply noise rejection of the pulse receiver.

6.3.1.4 Crosstalk cancellation for pulse signaling

For pulse signal, the crosstalk is larger than traditional NRZ data due to its higher frequency components. Crosstalk cancellation schemes integrated with pulse signaling is preferred to reduce crosstalk and further increase the routing density of T-Lines. To be simple, the crosstalk cancellation is preferred to be at transmitter side.

6.3.2 Simple equalization

Coupling capacitors are used as passive equalizers in ACCI pulse signaling. For very high data rates, such as 20Gb/s, the coupling capacitors need to be very small to provide equalization and remove ISI. These small coupling capacitors limit the signal swing at receiver input. By using simple FFE equalization to provide part of the equalization, the coupling capacitor can be designed to be larger and thus relieve the swing limit. This also allows the T-Line to be longer. So, by using simple FFE, both the capacitor range and the T-Line length range can be extended.

We can use only passive equalization or use only active equalization or use both. The trade-offs among these three schemes are data rate, power dissipation, design effort, circuit area, crosstalk noise, coupling capacitor size range, and T-Line length range.

6.3.3 Clock recovery based on pulse signaling

Traditional clock recovery is based on NRZ signaling. A multi-phase clock recovery based on recovered NRZ data after the pulse receiver is shown in Chapter 3. It is desired to have a novel clock and data recovery design dedicated for pulse signaling, as shown in Figure 4.9 (b). This not only simplifies the procedure for front-end pulse receiver design, but also removes the jitter added by the front-end receiver. The challenge is that the pulse width is narrower than that of NRZ data, which reduces timing margin for the sampler.

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