ABSTRACT

XU, JIAN. AC Coupled Interconnect for Inter-chip Communications. (Under the direction of Prof. Paul D. Franzon.)

The scaling of integrated circuit (IC) technology demands high-speed, high-density and low-power input/output (I/O) for inter-chip communications. As an alternative scheme for conductive interconnects, AC coupled interconnect (ACCI) was proposed previously to meet these increasing I/O requirements. ACCI includes AC coupling elements into a signal channel; it has contactless physical structure and band-pass channel characteristic. ACCI can be classified into two categories: capacitively coupled interconnect (CCI) that includes series capacitors, and inductively coupled interconnect (LCI) that includes spiral transformers. This dissertation addressed research progresses on both CCI and LCI for multi-Gb/s inter-chip communications.

System analysis and transceiver circuit design for CCI chip-to-chip communications are presented. In a demonstration for CCI on multi-chip module (MCM), two flip chips communicated pseudo random bit sequence (PRBS) signals at 2.5Gb/s data rate through chip-substrate interface capacitors. In a demonstration for CCI on print circuit board (PCB), two bare chips communicated data at 2.0Gb/s through on-chip capacitors. Potential applications of high-permittivity materials and embedded capacitors for CCI interfaces were also investigated.

This work explored LCI vertical connections in three-dimensional (3D) ICs. A novel current-mode LCI transceiver circuit is presented. In measurements, two test chips stacked and communicated data at 2.8Gb/s through an inter-chip transformer. Misalignment and crosstalk issues in LCI are also addressed. A unique power delivery scheme, which provides

AC connections through LCI interfaces and DC connections at chip edges, is proposed. A novel 3D-ICs structure, which combines LCI vertical connections and 3D vertical vias, is also presented. In measurements, eight LCI vertical channels operated simultaneously at 1.25Gb/s data rate.

This work also explored LCI interfaces in package-board sockets and board-board connectors. Analysis and electromagnetic (E-M) modeling for interface transformers are addressed. MCM test vehicles were designed to demonstrate chip-to-chip communications over LCI. Simulations indicated a LCI transceiver system could communicate data at 2.0Gb/s through a pair of coupled spiral inductors.

In conclusion, ACCI can provide feasible high-density high-speed and low-power I/O at L1~L3 packaging levels for inter-chip communications.

AC COUPLED INTERCONNECT
FOR INTER-CHIP COMMUNICATIONS

by

JIAN XU

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APPROVED BY:

PAUL D. FRANZON
(Chair of Advisor Committee)

JOHN M. WILSON
(Co-chair of Advisor Committee)

EDWARD GRANT

W. RHETT DAVIS

JON-PAUL MARIA

DEDICATION

To my wife, Zhengmin

my parents, Tingkui and Changying

BIOGRAPHY

Jian Xu was born in Jiangxi Province, China, in 1972. He earned a B.S. degree in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China, in 1993, and then worked on process automation with Beijing General Research Institute of Mining & Metallurgy, Beijing, China. He started the Ph.D program in Electrical and Computer Engineering at North Carolina State University (NCSU), in Fall 2001. He did internships with Motorola Labs, IBM T.J. Watson Research Center and Rambus during the summer of 2002, 2005 and 2006, respectively. His research topics included: AC coupled interconnect, high-speed I/O transceiver, three-dimensional ICs integration, signal integrity analysis, and power electronics for piezoelectric micro-actuators.

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LIST OF ABBREVIATIONS

3D-ICs, 3-D ICs	Three-dimensional Integrated Circuits
ACCI	AC Coupled Interconnect
BER	Bit Error Rate
CCI	Capacitively Coupled Interconnect
E-M	Electromagnetic
ESD	Electrostatic discharge
FD-SOI	Fully-depleted Silicon on Insulator
Gb/s, Gbps	Gigabit per Second
I/O	Input Output
ISI	Inter-Symbol-Interference
ITRS	International Technology Roadmap of Semiconductor
LCI	Inductively Coupled Interconnect
MIM	Metal-Insulator-Metal
MCM	Multi-Chip Module
NRZ	Non-Return-to-Zero
PCB	Print Circuit Board
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
RZ	Return-to-Zero
SAFF	Sense Amplifier Flip Flop
SNR	Signal-to-Noise Ratio

SSN	Simultaneous Switching Noise
T-Line	Transmission Line
TX	Transmitter / Driver
TRX	Transceiver
UI	Unit Interval
XMFR	Transformer
Xtalk	Cross Talk

Chapter 1. Introduction

1.1. Motivations and Objectives

1.1.1. Research Motivations

The scaling of integrated circuit (IC) technology demands high-speed, high-density and low-power input/output (I/O) to provide Terabit/sec aggregate bandwidth for inter-chip communications. The International Technology Roadmap for Semiconductors (ITRS) website [57] predicts that in year 2013 the maximum pin-count in a high-performance single chip package will be 4736 and the data speed of chip-to-board peripheral buses will be 18.625GHz. AC coupled interconnect (ACCI) scheme uses contactless signal channels and transmits information on the transition edges of digital signals. ACCI is an alternative for conventional conductive interconnects and provides a solution to meet increasing I/O requirements. There are two types of ACCI: capacitively coupled interconnect (CCI) where coupling elements are formed using metal plate pairs, and inductively coupled interconnect (LCI) where coupling elements are formed using spiral inductor pairs.

For a binary digital signal, its transition edges (i.e. rising/falling edges) carry the digital information and its DC component is not necessary for the transmission of digital information. ACCI includes AC coupling elements, such as: a series capacitor or a spiral transformer, into a signal I/O channel. It blocks DC and low-frequency components of digital signals, and only transmits transition edges of digital signals. The magnitude of the AC coupled signal is proportional to the edge rate of digital signals instead of data rate, though

high data rates require fast edge rates. While the data rates and edge rates continue to scale up with IC technologies, ACCI channels will more easily support high speed signaling.

For high-density package technologies, e.g. controlled-collapse-chip connections (C4) [52] in flip-chip packages, mechanical stress and thermal issues are one of the major limitations to achieving higher I/O density. ACCI interface has a non-contacting physical structure. It has the potential to overcome some of the mechanical and thermal constraints in building high-density I/O interfaces.

1.1.2. Research Objectives

The purpose of this work is to develop high-speed, high-density, low-power, low-cost and robust ACCI transceiver systems for chip-to-chip communications as well as vertical signaling in three-dimensional (3D) ICs.

1.2. Original Contributions

1.2.1. Capacitively Coupled Interconnect

This dissertation describes the theoretical analysis for CCI in both time domain and frequency domain. It also addresses characterizations for CCI channels and circuit design for CCI transceiver systems. This dissertation presents two successful demonstration systems for CCI chip-to-chip communications on a multi-chip module (MCM) and a printed circuit board (PCB):

A MCM assembly was built to demonstrate 2.5Gb/s capacitive coupling communications between two flip-chips, where transceiver test chips were fabricated in 0.35μm CMOS technology and coupling capacitors were formed at the interface between the flipped chips and the MCM.

A test vehicle on a PCB was built to demonstrate 2.0Gb/s capacitive coupling communications between two surface-mounted bare chips, where transceiver test chips were fabricated in 0.18μm fully-depleted silicon-on-insulator (SOI) technology and coupling capacitors were on-chip metal-insulator-metal (MIM) capacitors.

This work explored the potential applications of high-permittivity under-fill materials and on-board embedded capacitors for CCI chip-to-chip communications, as well.

1.2.2. Inductively Coupled Interconnect

This dissertation describes theoretic analysis for LCI in both time domain and frequency domain. It also addresses characterizations for LCI channels and circuits design for LCI transceiver systems.

This dissertation presents a successful demonstration system for LCI vertical signaling in a three-dimensional (3D) IC. Two chips were stacked to demonstrate 2.8Gb/s inductively coupled vertical signaling in a 3D-ICs, where transceiver test chips were fabricated in 0.35μm CMOS technology and coupled spiral inductors formed an inter-chip transformer.

This dissertation proposes a new power delivery scheme for LCI in 3D-ICs, which provides AC connections via LCI interfaces and DC connections at chip edges. It also

presented an integrated 3D-ICs structure that combines LCI interfaces and 3D vertical via technologies. In demonstration, 8 LCI vertical channels operated simultaneously at 1.25Gb/s.

This work also explored LCI schemes for package-to-board socket and board-to-board connector interfaces to improve I/O pin density and create a reliable interface. Analysis and electromagnetic (E-M) modeling for interface transformers are addressed. MCM test vehicles were designed to demonstrate chip-to-chip communications over LCI.

1.3. Dissertation Overview

Chapter 1 introduces the research motivation and objectives of ACCI for inter-chip communications. Chapter 2 reviews the previous publications relevant to ACCI approaches in academia and industry research. Chapter 3 presents CCI chip-to-chip communications on MCMs and PCBs. Chapter 4 presents LCI vertical connections in three-dimensional (3D) ICs. Chapter 5 addresses LCI schemes for package-board socket and board-board connector interfaces. Chapter 6 provides conclusions and proposes ACCI future work. The appendices describe some additional topics relevant to ACCI.

1.4. Publications List

1.4.1. Journal Papers

1. J. Xu, S. Mick, J. Wilson, L. Luo, K. Chandrasekar, E. Erickson, and P. Franzon, "AC coupled interconnect for dense 3-D ICs", *IEEE Trans. on Nucl. Sci.,* vol. 51, no. 5, Oct. 2004, pp. 2156-2160.
2. W. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. Sule, M. Steer, P. Franzon, "Demystifying 3D ICs: The pros and cons of going vertical", *IEEE Design & Test of Computers,* vol. 22, no. 6, Nov. 2005, pp. 498-510.
3. L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, and P. Franzon, "3Gb/s AC coupled chip-to-chip communication using a low swing pulse receiver", *IEEE J. of Solid State Circuits,* vol. 41, no. 1, Jan. 2006, pp. 287-296.
4. L. Zhang, J. Wilson, R. Bashirullah, L. Luo, J. Xu, P. Franzon, "Voltage-mode driver pre-emphasis technique for on-chip global buses", *IEEE Trans. on VLSI,* (accepted)
5. J. Wilson, S. Mick, J. Xu, L. Luo, S. Bonafede, A. Huffman, R. LaBennett, P. Franzon, "Fully integrated AC coupled interconnect using buried bumps*", IEEE Trans. on Advanced Packaging,* (accepted)

1.4.2. Conference Papers

1. J. Xu, J. Wilson, S. Mick, L. Luo, and P. Franzon, "2.8Gb/s inductively coupled interconnect for 3-D ICs", *Symp. on VLSI Circuits,* Jun. 2005, paper 22.4, pp. 352-355.

2. J. Xu, S. Mick, J. Wilson, L. Luo, K. Chandrasekar, E. Erickson, and P. Franzon, "AC coupled interconnect for dense 3-D ICs", *IEEE Nucl. Sci. Symp.,* Oct. 2003, pp. 125-129.
3. J. Xu, J. Wilson, E. Erickson and P. Franzon, "Pulse signaling in inductively coupled sockets and connectors", *Semiconductor Research Corp. Student Symposium*, Oct. 2006, paper 13.2
4. L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, and P. Franzon, "A 3Gb/s AC coupled chip-to-chip communication with a low swing pulse receiver", *IEEE Int'l Solid-State Circuits Conf.,* Feb. 2005, paper 28.7, pp. 522-523.
5. L. Luo, J. Wilson, J. Xu, S. Mick and P. Franzon, "Signal integrity and robustness of ACCI packaged systems", *IEEE Topic Meeting on Electrical Performance of Electronic Packaging,* Oct. 2005, pp. 11-14.
6. L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, E. Erickson and P. Franzon, "A 36Gb/s ACCI multi-channel bus using a fully differential pulse receiver," *IEEE Custom Integrated Circuits Conf. (CICC),* Sept. 2006, paper 26.3.
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9. J. Wilson, S. Mick, J. Xu, L. Luo, S. Bonafede, A. Huffman, R. LaBennett, P. Franzon, "Fully integrated AC coupled interconnect using buried bumps*", IEEE Topic Meeting on Electrical Performance of Electronic Packaging,* Oct. 2005, pp. 7-10.

10. J. Wilson, P. Franzon, L. Luo, J. Xu, S. Mick, B. Chan and H. Lin, "AC coupled interconnect using buried bumps for laminated organic packages," *Electronic Components and Technology Conf.,* May 2006, paper 1.7.
11. J. Wilson, S. Mick, J. Xu, L. Luo, E. Erickson, and P. Franzon,, "Consideration for transmission line design on MCMs using AC coupled interconnect with buried solder bumps," *10th IEEE Workshop on Signal Propagation on Interconnects,* May 2006.
12. K. Chandrasekar, J. Wilson, E. Erickson, Z. Feng, J. Xu, S. Mick and P. Franzon, "Fine pitch inductively coupled connectors for multi-Gbps pulse signaling," *IEEE Topic Meeting on Electrical Performance of Electronic Packaging,* Oct. 2006, paper 2.3.
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1.4.3. Presentations

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2. J. Xu, J. Wilson and P. Franzon, "Development of AC coupled interconnects for multi-gigabit/sec inter-chip communications," *1st Annual NC State Graduate Student Research Symposium (Poster),* Raleigh, NC, Mar. 2006
3. J. Xu, J. Wilson, and P. Franzon, "Development of multi-Gb/s AC coupled interconnects", *IMAPS Carolina Scientific Symp,* RTP, NC, Mar. 2006
4. J. Xu, J. Wilson, and P. Franzon, "A power delivery scheme for inductively coupled 3D-ICs," *IMAPS Carolina Scientific Symp* (Poster), RTP, NC, Mar. 2006
5. J. Xu, J. Wilson, S. Mick and P. Franzon, "Development of multi-Gb/s AC coupled interconnects," *Semiconductor Research Corp. Contract Review (Poster),* Palo Alto, CA, Aug. 2005.
6. J. Xu, J. Wilson and P. Franzon, "Development of AC coupled interconnects for multi-Gb/s inter-chip communication", *ECE Department Graduate Student Association Seminar*, Raleigh, NC, Aug. 2005
7. J. Xu, J. Wilson and P. Franzon, "Development of multi-Gb/s AC coupled interconnects," *IBM T.J. Watson Research Center Seminar,* Yorktown Heights, NY, Aug. 2005.
8. J. Xu, J. Wilson and P. Franzon, "AC coupled interconnects with fully-depleted SOI technology," *Air Force Research Lab Contract Review*, Raleigh, NC, Sept. 2003

Chapter 2. Literature Review

2.1. Overview

This chapter introduces the concept of AC coupled interconnect (ACCI), which includes capacitively coupled interconnect (CCI) and inductively coupled interconnect (LCI). It also summarizes the up-to-date publications on ACCI and similar technologies in chip-to-chip communications and vertical signaling in three-dimensional ICs.

2.2. IC Packaging Hierarchy

In the semiconductor and electronics manufacture chain, IC packaging process includes multiple levels such as: chip-to-package *L1* level, package-to-board *L2* level and board-to-board *L3* level. An overview of IC packaging hierarchy is illustrated in Figure 2.1. In the first level (*L1*) packaging, a bare chip is mounted onto a chip carrier or an interposer through wire-bonding or flip-chip techniques [52], and the interconnections in *L1* packaging are at chip-to-package interfaces. A special type of *L1* packaging is a multi-chip module (MCM) [47], where multiple chips are mounted on a common substrate. The interconnections in a MCM include chip-to-substrate connections and chip-to-chip connections. Another special type of *L1* packaging is a three-dimensional (3D) IC [38],

where multiple chips are stacked on a base chip and encapsulated into a package. The interconnections in 3D-ICs include chip-to-chip vertical connections and the base chip to package connections.

In the second level (*L2*) packaging, a ceramic or organic package such as a pin-grid array (PGA) or ball-grid array (BGA) is mounted onto a printed circuit board (PCB). The interconnections in *L2* packaging are at package-to-board interfaces. A special type of *L2* packaging is a package-board adapter or socket that introduces more flexibility for manufacture/assembly. In the third level (*L3*) packaging, daughter cards are mounted onto a motherboard or backplane. The interconnections in *L3* packaging are at board-to-board connector interfaces.

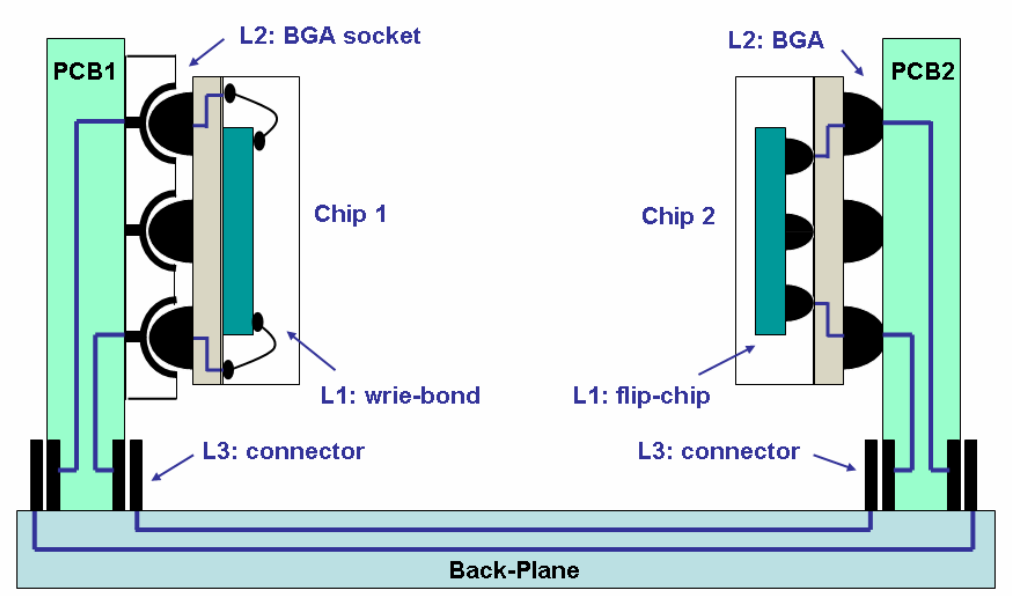


Figure 2.1. Overview of packaging hierarchy

2.3. AC Coupled Interconnect

AC coupled interconnect (ACCI) inserts AC coupling elements such as series capacitors and spiral transformers for inter-chip connections at L1~L3 packaging levels. It has a non-contacting structure and is an alternative scheme for conventional conductive interconnections to achieve multi-Gb/s communication data rate between ICs. Mick et al. (2002) presented the concept of ACCI [7], which includes two types: capacitively coupled interconnect (CCI) where the coupling elements are series capacitors formed by metal plate pairs, and inductively coupled interconnect (LCI) where the coupling elements are transformers formed by spiral inductor pairs.

(a) A capacitively coupled interconnect (CCI) transceiver system

(b) An inductively coupled interconnect (LCI) transceiver system

Figure 2.2. Concept of AC coupled interconnect

Figure 2.2(a) shows a CCI chip-to-chip transceiver system. A voltage mode transmitter (TX) circuit drives the first series capacitor and converts non-return-to-zero (NRZ) digital signals into return-to-zero (RZ) pulses. These pulses propagate over a transmission

line (T-line) and pass through the second series capacitor with some attenuation and distortion. A voltage mode receiver (RX) circuit senses the voltage pulses and restores them back to full-swing NRZ voltage signals. Although the transceiver system shown in Figure 2.2(a) has a single-ended structure, it can be a differential as well.

Figure 2.2(b) shows a LCI chip-to-chip transceiver system. A current mode TX circuit converts NRZ voltage signals into bipolar current swings. At the first transformer, the current swings excite the primary inductor and induce current pulses at the secondary inductor. These current pulses flow in the T-line and pass the second transformer with additional attenuation and distortion. A current mode RX circuit senses the current pulses and regenerates NRZ voltage signals.

Franzon et al. (2001) filed a patent on "inductively coupled electrical connectors" [53]. They also filed a patent on "Buried solder bumps for AC-coupled microelectronic interconnects" [54].

Mick et al. (2004) proposed a novel physical structure to allow both ACCI and DC connections across the chip-to-substrate interfaces in a multi-chip module (MCM) [7][8]. A cross section of this structure is shown in Figure 2.3, which consists of multiple flip chips and a common substrate. Buried solder bumps are landed into trenches in the substrate to provide DC connections between chips and substrate. AC coupling elements, either metal plates or spiral inductors, are created on both chips and the substrate to provide AC signal connections across the chip-to-substrate interfaces. Routing layers are created on the substrate to bring DC voltages to solder bumps and allow interconnections between chips via the AC coupling elements.

Mick et al. demonstrated a CCI transceiver system that transmitted 2GHz clock signals. Test chips were fabricated in 0.25μm CMOS technology, and the coupling elements were 0.8pF on-chip metal-insulator-metal (MIM) capacitors. In Mick's Ph.D dissertation (2004) [1], he included detailed analysis of CCI and LCI interface models.

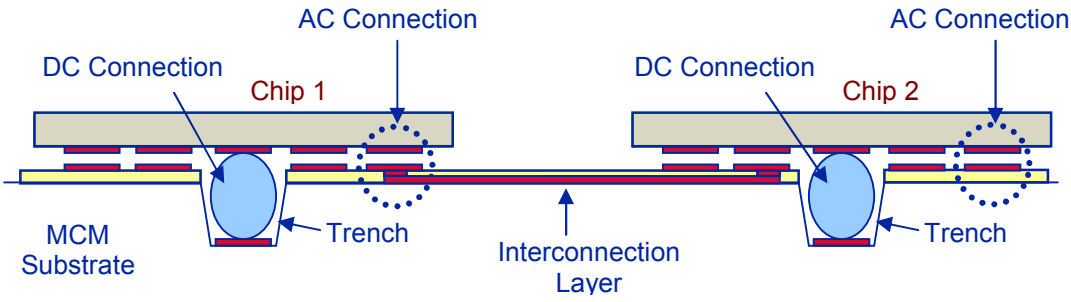


Figure 2.3. A physical structure of ACCI on MCM

Luo et al. (2005) presented capacitively coupled chip-to-chip communication using a low-swing pulse receiver [9][10][11]. They demonstrated two chips communicating across a 15cm PCB micro-strip line that connected 150fF on-chip coupling capacitors on each end through bonding wires. The novel low-swing differential pulse receiver was able to detect 60mV pulse signals and recover non-return-to-zero (NRZ) signals at the data rate of 3Gb/s. For 0.18μm CMOS test chips, each transceiver channel dissipates 15mW. They also discussed signal integrity and robustness issues in CCI packaged systems [11]. Luo presented timing circuits that include a delay-lock-loop (DLL) and clock-data-recovery (CDR) for CCI transceiver system in his Ph.D dissertation [2].

Chandrasekar et al. (2005) introduced inductively coupled board-to-board connectors [14][15]. They proposed to replace conventional connectors with coupled spiral inductors to increase I/O pin density, and reported simulation and measurement results for LCI interfaces

Chandrasekar also described LCI channel modeling and system design tradeoffs in his Ph.D dissertation [3].

2.4. Chip-to-Chip Communications

2.4.1. Conductive Chip-to-Chip Communications

Signal channels for conductive chip-to-chip communications on MCM, PCB and Backplane are described in Table 2.1.

Table 2.1. Signal channels for conductive chip-to-chip communications

	MCM	PCB	Backplane
Package	Bare chip wire-bond or flip-chip	Packaged chip PGA, BGA or LGA	Packaged chip PGA, BGA or LGA
T- lines	Short lossy T-line on carrier (e.g. 1 inch)	T-line on board (e.g. 10 inch)	Two T-lines on cards, one long T-line on backplane (e.g. 25 inch)
Parasitic components	Bonding wires or solder bumps	Package leads, board vias, sockets	Package leads, board vias, connectors

In a multi-chip module (MCM), multiple bare chips are mounted onto a common carrier or substrate via wire-bonding or flip-chip technologies. A signal channel for chip-to-chip communication in a MCM includes a short but lossy transmission line on the substrate and lumped parasitics for bonding wires or solder bumps.

In a PCB, multiple packaged chips are assembled onto a laminated FR4 board via surface-mount or through-hole technologies. A signal channel on a PCB includes traces on the board and parasitic lumped components such as: bonding wires or solder bumps for die,

trace stubs in packages, leads or balls of package pins, and via stubs on the board. A package-to-board adaptor or socket may also be included into the signal channels.

In a backplane system, multiple line cards are inserted into connectors or slots on a backplane. Signal channels for chip-to-chip communications in a backplane include traces and parasitic components on daughter cards, board-to-board connectors, long traces and via stubs on the backplane.

2.4.2. Non-contacting Chip-to-Chip Communications

Salzman et al. (1994) introduced capacitively coupled interconnect for chip-to-substrate interfaces in a multi-chip module [32][33]. Knight et al. filed two patents on capacitive coupling interfaces in 1994 [55] and in 1999 [56]. Hayden et al. (1994) introduced pulse-mode signaling for a capacitively coupled interconnect [37].

Gabara et al. (1996) described a technique of quantized feedback that eliminates the "zero wander" effect in capacitive coupling channel with an on-chip capacitor [35][36]. For 0.5μm CMOS test chips, this receiver circuit can detect PRBS data up to 800Mb/s and down to 2kHz.

Chang et al. (2001) introduced a concept of RF/wireless interconnect for inter-chip and intra-chip communications [18]. Unlike the conventional conductive interconnect, the novel RF/wireless interconnect is based on capacitive coupling onto a coplanar waveguide (CPW).

Kim et al. (2004) presented a capacitively coupled bus interface based on synchronous pulse signaling [21][22]. For test chips in 0.1μm CMOS DRAM process, they

demonstrated 1.0Gb/s differential pulsed signaling over 10cm PCB lines. This system dissipates 1.92mW power per transmitter and 2.7mW power per receiver.

2.5. Inter-chip Communications in Three-dimensional ICs

2.5.1. Three-dimensional ICs Overview

Three-dimensional (3D) ICs is a new chip/package architecture where multiple chips are stacked vertically. Banerjee et al. (2001) gave an overview on 3D-ICs technology [38]. It was shown that 3D-ICs can improve the availability of interconnect resources and significantly reduce interconnect delay. 3D-ICs can also facilitate integration of heterogeneous technologies in a single chip.

Figure 2.4 illustrates multiple planar chips, which includes a microprocessor chip, a memory chip, a digital signal processor (DSP) chip and a radio frequency (RF) module chip, integrated into a 3D-ICs stack.

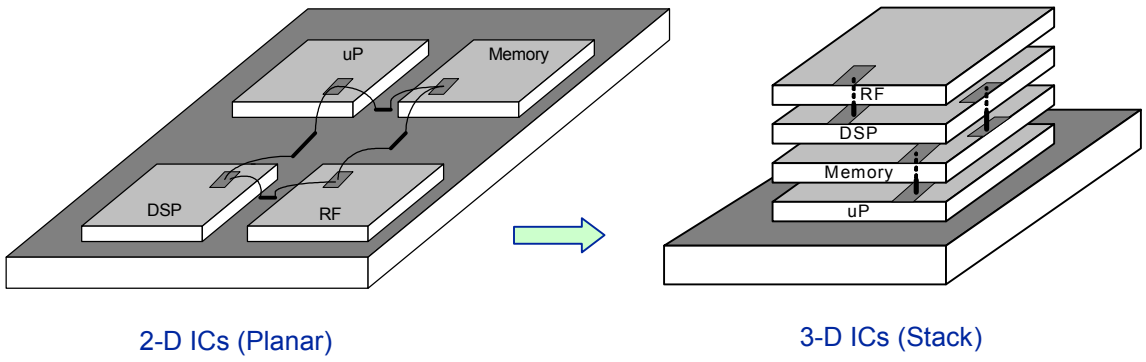


Figure 2.4. Integrating 2-D ICs to 3-D ICs

However, 3D-ICs technology dramatically increases internal heat density [16]. The thermal management capability for 3D interconnects is a critical challenge predicted by the International Technology Roadmap for Semiconductors (ITRS) [57].

2.5.2. Conductive Vertical Interconnections

Al-Sarawi et al. (1998) gave a review of 3-D packaging technologies [45]. Brown (2004) gave an overview on system-in-package (SiP) technologies [41], he presented multiple thin chips that were stacked and connected through wire-bonding. Ezaki et al. (2004) reported a CPU-DRAM 3D chip stack [42], where the vertical connections between chips consist of micro-bumps in 30μm diameter and 60μm pitch.

Black et al. (2004) demonstrated a 3-D implementation of an x86 microprocessor [39]. Two chips stacked face-to-face and connected through die-to-die vias. Compared to a 2-D planar implementation, the 3-D architecture could improve performance by 15% while decreasing power by 15%.

Suntharalingam et al. (2005) presented a mega-pixel image sensor fabricated in wafer level 3D-ICs technologies [40]. Two fully-depleted SOI dies and one photodiode die were thinned and stacked. Two bonded dies were connected by 3-D vias that used tungsten (W) plugs with ~2μm square size and ~7.5μm depth.

Figure 2.5 illustrates various conductive vertical connections in a 3-D stack; it includes a 3-D package (SiP) with wire-bonding, a face-to-face chip stack with micro-bumps and a 3D-ICs with vertical through-vias technologies.

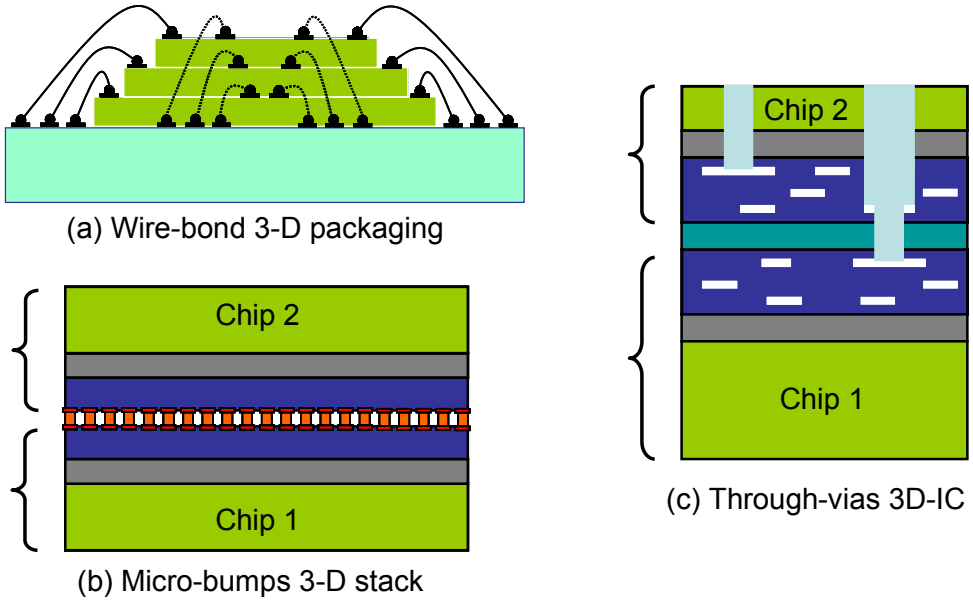


Figure 2.5. Conductive vertical interconnections

2.5.3. Capacitively Coupled Vertical Signaling

Kuhn et al. (1995) proposed a signaling method for direct vertical transmission of digital signals between adjacent chip-layers in 3D-ICs by capacitive coupling [34]. The scheme of a capacitive coupling interface is shown in Figure 2.6, where the coupling pads occupied 20x20μm^2 area and separated vertically with a 2.5μm dielectric layer. They chose an inverter chain as the driver and proposed novel circuitry for pulse receiving. For 0.5μm CMOS test chips, the RX circuit recovered clock signals at 25MHz.

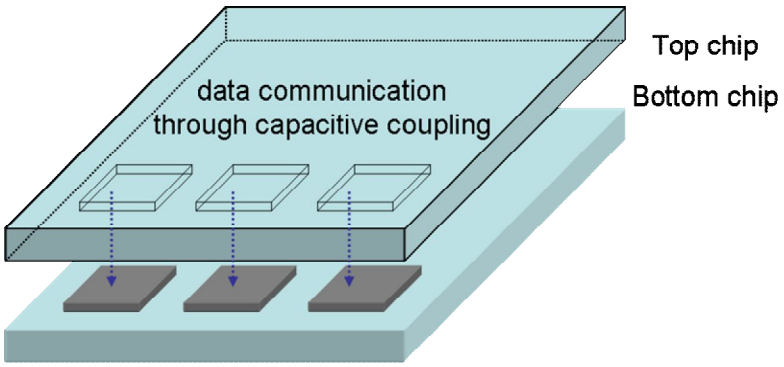


Figure 2.6. An interface for capacitively coupled vertical signal transmission

Kanda et al. (2003) presented a wireless superconnect (WSC) interface scheme for vertical signaling in 3D-ICs [26]. This scheme also utilizes capacitively coupled contactless mini-pads as chip-to-chip connection interfaces. The transmitter converts NRZ signals to return-to-half-Vdd signals and the receiver is based on a sense-amplifier flip-flop. They demonstrated WSC using 0.35μm CMOS test chips, where each mini-pad was 20μm per side and the vertical distance between two mini-pads was 1~2μm, and each capacitive WSC I/O consumed 3mW power at 1.27Gb/s data rate.

Drost et al. (2003) proposed a proximity communication structure, shown in Figure 2.7, where chips overlap face-to-face and communicate via capacitive coupling interfaces on chip edges [23][24][25]. For 0.35μm CMOS test chips, they demonstrate 16 capacitive coupling channels, placed in 50μm pitch and operated simultaneously. Each channel communicated PRBS signals at a data rate of 1.35Gb/s, and 16 channels achieved an aggregate bandwidth of 21.6Gb/s.

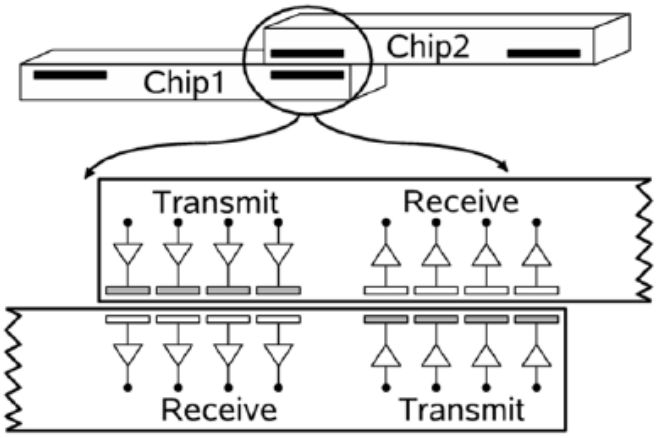


Figure 2.7. Cross-section of a proximity communication structure [25]
(Courtesy of Robert Drost, Sun Microsystems)

Gu et al. (2004) presented a RF-interconnect (RFI) technology based on capacitive coupling and peak signal detection [19][20]. For 0.18μm CMOS test chips with 60fF coupling capacitors, they demonstrated an amplitude-shift keying (ASK) transceiver system in 3D-ICs. The RF-interconnect transceiver communicated PRBS at 3Gb/s data rate, consumed 4mW power and maintained a bit error rate (BER) less than 10^{-10}.

Fazzi et al. (2005) reported a synchronous 3D interconnection based on capacitive coupling [48]. They presented a capacitively coupled link consumed 0.128mW/pin power at 975Mb/s data rate, and the capacitive pad area was down to $8x8\mu m^2$.

2.5.4. Inductively Coupled Vertical Signaling

Mizoguchi et al. (2004) presented an inductive coupling wireless superconnect (WSC) in stacked chips, shown in Figure 2.8, where data paths used coupled spiral inductors, power/ground and clock used wire-bonded connections [27][30]. Test chips in 0.35μm

CMOS technology were stacked at a distance of 300μm. Transceiver circuits communicated NRZ signals at a data rate of up to 1.2Gb/s per pin, while the TX circuit consumed 43mW power and the RX circuit consumed 2.5mW power.

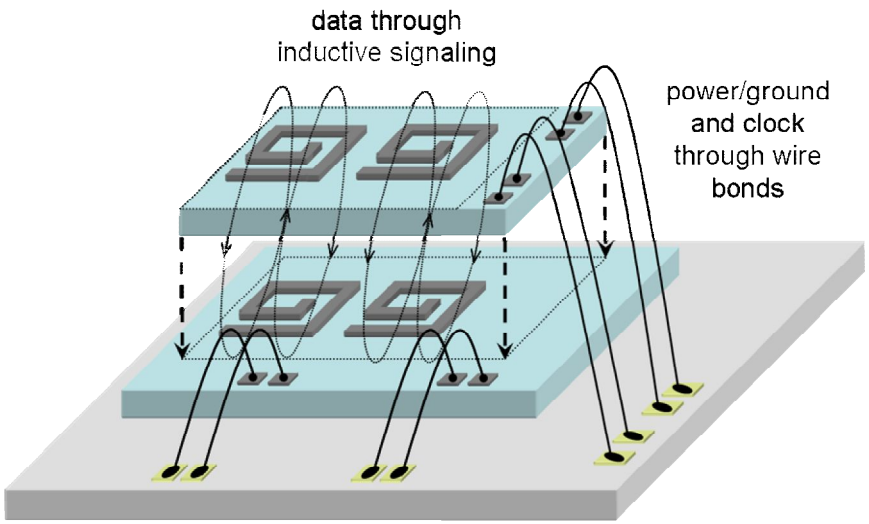


Figure 2.8. Wireless superconnect (WSC) based on inductive inter-chip signaling

Miura et al. (2005) reported inductively coupled wireless interface, which achieved an aggregated data rate of 195Gb/s by arranging 195 transceivers in 50μm pitch with total power dissipation of 1.2W [28][31]. The chip thickness was thinned down to 10μm and the communication distance was 15μm, including the glue thickness. The TX circuit used a single-end structure and included a series compensation capacitor for reducing its DC power dissipation.

Miura et al. (2006) presented a 1024 transceiver array for inductive-coupling inter-chip communication in a two-chip stack [29]. The chip thickness was also thinned down to 10μm and the inductor pitch was 30μm. Each data channel operated at 1Gb/s and consumes 3mW. For every 64 data channels, a clock channel was included for synchronization.

2.6. Summary

Recently, ACCI attracts growing research interests in both academia and industry. CCI was proposed to apply on various areas such as vertical connections in 3D-ICs [26], edge-to-edge proximity communication [25], and multi-drop memory bus [22]. LCI was reported to apply on vertical connections in 3D-ICs [31].

In NC State University, Mick proposed a novel ACCI physical structure on MCM [1]; Luo reported differential transceiver systems for CCI on PCB, he also presented timing circuitry and signal integrity for CCI [2]; Chandrasekar described analysis and modeling for LCI interfaces [3].

This work explored ACCI in an integrated view; it includes channel characterization, system analysis, transceiver circuit design and I/O demonstrations for CCI as well as LCI.

Chapter 3. Capacitively Coupled Interconnect (CCI) in Chip-to-Chip Communications

3.1. Overview

This chapter addresses the analysis for capacitive coupling channels and the characterizations for capacitive coupling interfaces. It describes pulse-mode signaling circuit design for capacitive coupling transceiver systems. It also presents capacitive coupling demonstration systems for chip-to-chip communications on MCM and PCB.

3.2. Analysis for Capacitive Coupling Channels

3.2.1. Frequency Domain Analysis

By ignoring parasitic capacitances of coupling capacitors, a simplified capacitive coupling channel for chip-to-chip communications is shown in Figure 3.1. It includes a transmission line (T-line), a termination resistor (R_T), a coupling capacitor (C_1) at the TX side and another coupling capacitor (C_2) at the RX side.

A lossy T-line presents low-pass characteristic. For instance, a 10cm 50ohm micro-strip line, which has 6.3mil trace width, 1oz (35μm) copper thickness and 4mil FR4 dielectric thickness, has a low-pass corner (-3dB) frequency at 13.95GHz.

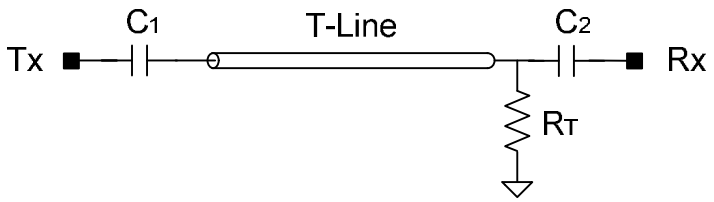


Figure 3.1. A simplified capacitive coupling channel

By adding a 50ohm termination resistor and two coupling capacitors which have capacitance variable in 200fF~1nF, AC analysis was performed and frequency responses (S_{21}) for the capacitive coupling channel are shown in Figure 3.2. It can be observed that a capacitive coupling channel presents band-pass characteristic, where the coupling capacitance (C_C) defines the high-pass corner frequency (f_{hp}) and the lossy T-line defines the low-pass corner frequency (f_{lp}).

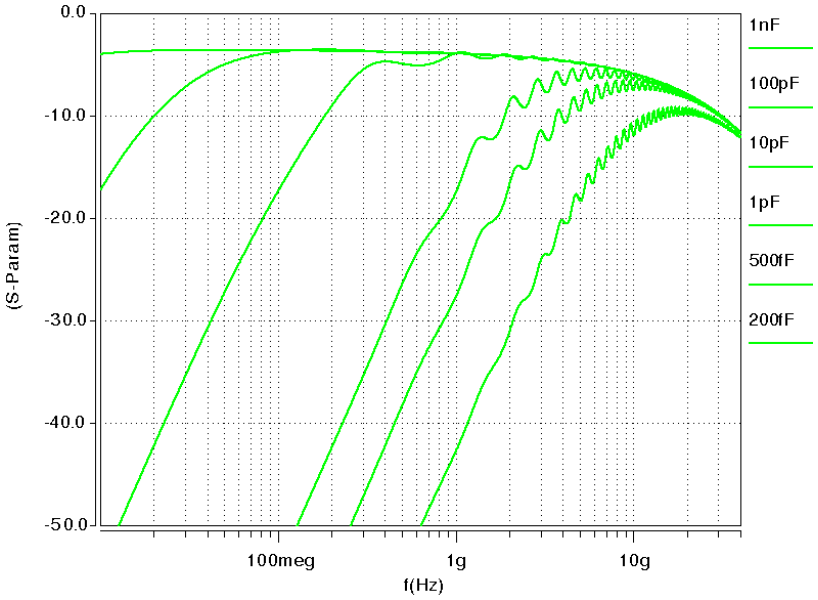


Figure 3.2. Frequency responses for various capacitive coupling channels

For various values of coupling capacitance, the corresponding bandwidths of the capacitive coupling channel are shown in Table 3.1. A channel with larger coupling capacitance, e.g. 1nF, has a lower f_{hp}, e.g. 3.6MHz, and can passes most low-frequency components of digital signals. Its band covers most of NRZ signal spectrum that is shown in Appendix F and it can support NRZ signaling with some coding scheme such as 8b/10b [4]. A channel with smaller coupling capacitance, e.g. 200fF, has a higher f_{hp}, e.g. 7.83GHz, and can only pass high-frequency components of digital signals. Its band covers RZ pulse signal spectrum that is also shown in Appendix F and it is suitable for pulse-mode signaling. If the coupling capacitance is in a range 5pF~100pF, the channel could support neither NRZ signaling nor RZ pulse signaling at multi-Gb/s data rate.

Table 3.1. Bandwidth of capacitive coupling channel

Coupling capacitance	High-pass corner frequency	Low-pass corner frequency	Signaling method
1 nF	3.6 MHz	11.20 GHz	NRZ
100 pF	38.4 MHz	11.20 GHz	NRZ
10 pF	271.5 MHz	11.20 GHz	None
1 pF	2.03 GHz	21.58 GHz	RZ pulse
500 fF	3.67 GHz	29.86 GHz	RZ pulse
200 fF	7.83 GHz	48.26 GHz	RZ pulse

3.2.2. Time Domain Analysis

A simplified model for a capacitive coupling transmitter is shown in Figure 3.3, where R_s, C_c and Z_0 represent the output impendence of drive circuit, the coupling

capacitance and the characteristic impendence of T-line, respectively. A 0→V_i step function is added as the source.

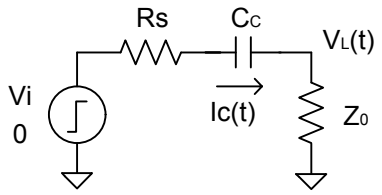


Figure 3.3. A simplified model for a capacitive coupling transmitter

This circuitry has differential equations:

$$V_i = R_s i_c(t) + v_c(t) + i_c(t) Z_o$$

$$\text{and} \quad i_c(t) = C_c \frac{dv_c(t)}{dt}$$

and an initial condition: $i_c(0) = \frac{Vi}{R_s + Z_0}$

There are solutions for the current in capacitor:

$$i_c(t) = \frac{Vi}{R_s + Z_0} \exp(\frac{-t}{(R_s + Z_0)C_c})$$

and the voltage on T-line:

$$V_L(t) = i_c(t) Z_o = \frac{Z_0 Vi}{R_s + Z_0} \exp(\frac{-t}{(R_s + Z_0)C_c})$$

This is the step response of the transmitter and has an decaying exponential waveform, where the time constant $(R_s+Z_0)C_c$ represents the decay time and the initial value $\frac{Z_0 Vi}{R_s + Z_0}$ represents the maximum amplitude. For a capacitive coupling transmitter with R_s=50ohm, Z_0=50ohm, and C_c= 0.2pF~100pF, the step response waveforms are shown in

Figure 3.4. If C_c is smaller than 1pF, the decay time is short than 500ps, which means a 2Gb/s NRZ signal will be converted into RZ pulses. If C_c is larger than 100pF, the decay time is much longer than 1ns, which means a 2Gb/s NRZ signal will pass the coupling capacitor and keep the NRZ shape.

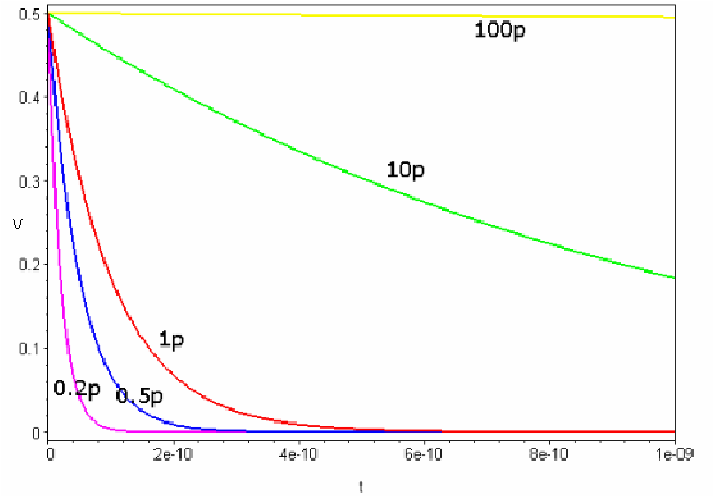


Figure 3.4. Step responses for a capacitive coupling transmitter

A simplified model for capacitive coupling receiver is shown in Figure 3.5, where R_T and R_L represent the termination resistance and the input impedance of receiver. Assuming the T-line is an ideal transmission line without any attenuation, the source for this receiver model equals the voltage on T-line $V_L(t)$, which is given by the previous solutions.

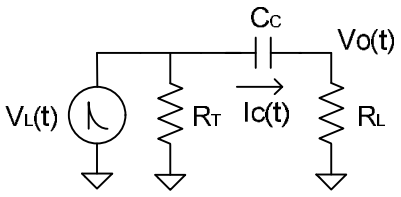


Figure 3.5. A simplified model for a capacitive coupling receiver

This circuitry has differential equations:

$$V_L(t) = v_c(t) + i_c(t)R_L$$

$$\text{and} \quad i_c(t) = C_c \frac{dv_c(t)}{dt}$$

and an initial condition: $i_c(0) = \dfrac{Z_0 Vi}{(R_s + Z_0)R_L}$

There is a solution for the voltage at the receiver input:

$$\mathrm{Vo}(t) := Rl\ \mathrm{ic}(t) = Rl \left(\frac{Vi\ Zo\ \mathbf{e}^{\left(-\frac{t\,(Rl - Rs - Zo)}{(Rs + Zo)\,Cc\,Rl}\right)}}{(Rs + Zo)\,(Rl - Rs - Zo)} - \frac{Vi\ Zo}{Rl\,(Rl - Rs - Zo)} \right) \mathbf{e}^{\left(-\frac{t}{Rl\,Cc}\right)}$$

A capacitive coupling transceiver system includes two differentiation elements, it has a second-order transfer function and its step response is a combination of two exponential waveforms. For R_S=50ohm, Z_0=50ohm, C_C=0.2pF, R_T=50ohm, and R_L=50~1000ohm, step responses at receiver input are shown in Figure 3.6. If R_L equals 50ohm, the voltage waveform at the receiver input will have large overshoot, also referred to as a double pulse. If R_L is larger, e.g. 500ohm, the overshoot will be much smaller. A high input impedance of receiver R_L increases the damping factor of the system transfer function and limits the overshoot to avoid double pulses.

Actually, in circuit simulations for a capacitive coupling transceiver system, the overshoot or double pulse at the second coupling capacitor was not significant because the input impedance of receiver R_L is typically much larger than 50ohm. It can also be explained in terms of bandwidth of high-pass filters. For the first coupling capacitor, its corner

frequency (f_1) is defined by $1/((R_S+Z_0)*C_C)$, where R_S is typically around 50ohm. For the second coupling capacitor, its corner frequency (f_2) is defined by $1/(R_L*C_C)$, where R_L is typically around 500ohm. As $(R_S+Z_0) << R_L$, then $f_1 >> f_2$, the second coupling capacitor has a lower high-pass corner frequency and a wider bandwidth than the first coupling capacitor. A pulse generated by the first coupling capacitor can pass the second coupling capacitor without creating a significant double pulse.

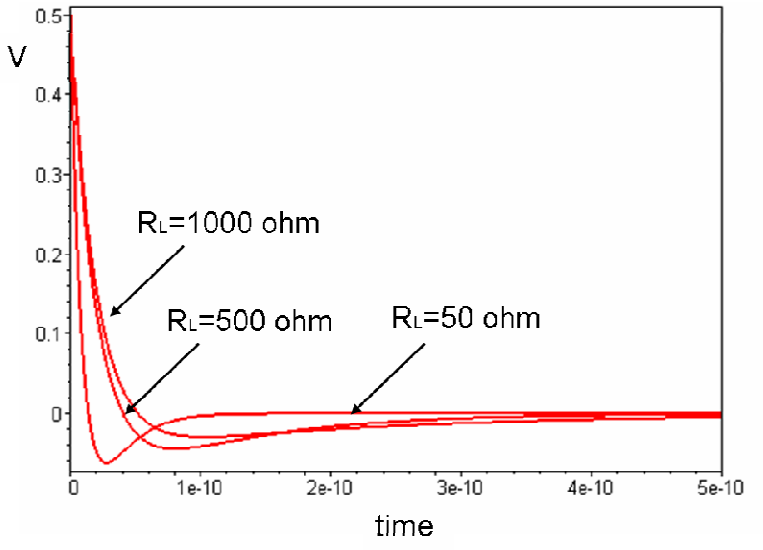


Figure 3.6. Step responses for capacitive coupling channels

3.3. Characterization for Capacitive Coupling Interfaces on MCM

3.3.1. Coupling Capacitance of Metal Plate Pair with Air Gap

A cross-section of capacitive coupling interface with air gap on a MCM is shown in Figure 3.7. Metal plates on chips and substrate are aligned to form coupling capacitors. Solder bumps not only provide DC connections between chips and substrate but also

maintain an air gap between them. A process overview of MCM with buried solder bumps is described in Appendix C.

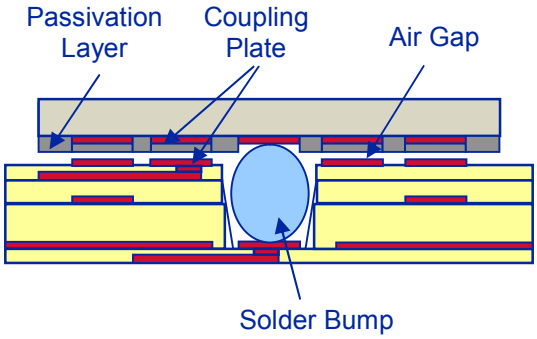


Figure 3.7. Cross-section of a capacitive coupling interface with air gap

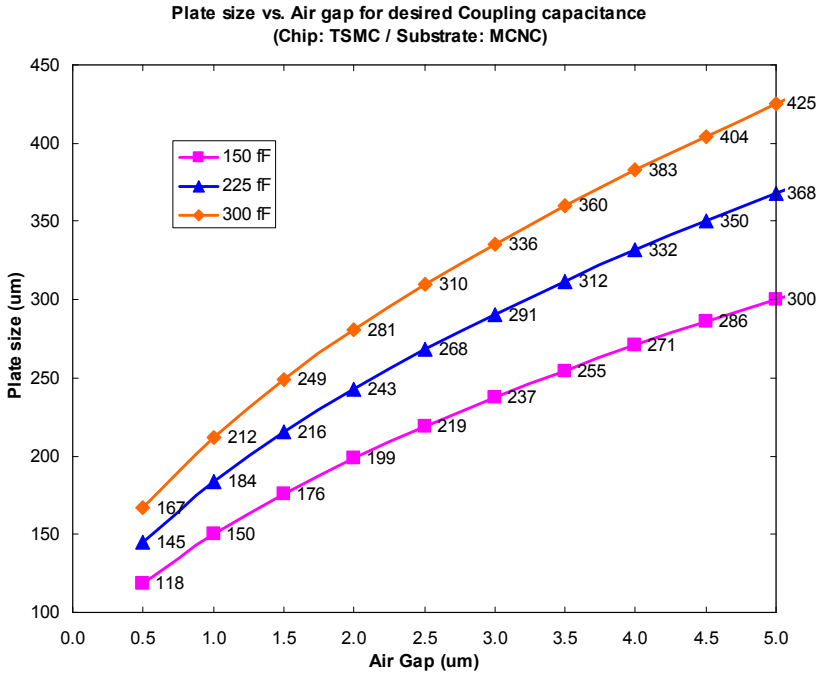


Figure 3.8. Requirements of plate size for various air gaps

For desired coupling capacitances such as 150fF, 225fF and 300fF, curves for the requirement of plate size in various air gap (0.5μm~5μm) are shown in Figure 3.8. The passivation layer on top of metal plates, e.g. 1.7μm dielectric with a 0.3μm equivalent air gap, is preferably kept for isolation. For a given coupling capacitance, the minimum size of coupling plates strongly depends on the air gap. For instance, at 2μm air gap, a 200x200μm^2 coupling plate pair is required to achieve a desired 150fF coupling capacitance. Such large size for a metal plate limits the density of coupling elements.

In the MCM assembly process, to achieve a 1~2μm air gap is feasible by controlling the volume of solder bumps. However, it is very difficult to maintain such a small gap evenly and constantly, due to the process variation and thermal expansion.

3.3.2. Coupling Capacitance of Metal Plate Pair with Epoxy Under-fill

Epoxy under-fill materials are commonly used in flip-chip processes to reduce the stress of solder bumps due to thermal mismatch between chips and substrate. A cross-section of capacitive coupling interface with epoxy under-fill on MCM is shown in Figure 3.9. Curves for the requirement of plate size in various epoxy under-fill thickness are shown in Figure 3.10.

Compared to the air gap capacitive coupling interfaces, plates sizes in the case of epoxy under-fill are reduced because the permittivity of epoxy material is higher than air gap, e.g. ε_r=5. For 5μm epoxy filling, to achieve the desired 150fF coupling capacitance, coupling plates could be 150x150μm^2.

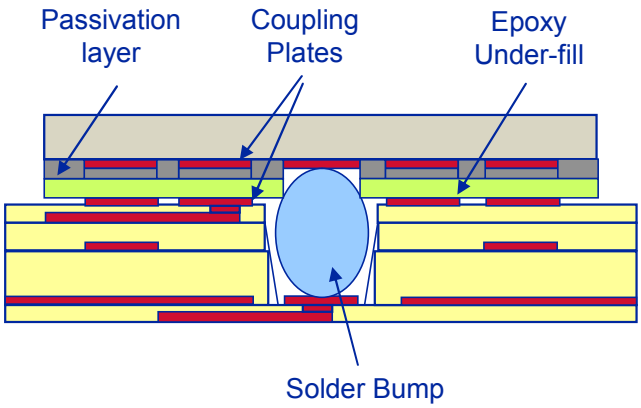


Figure 3.9. Cross-section of a capacitive coupling interface with epoxy under-fill

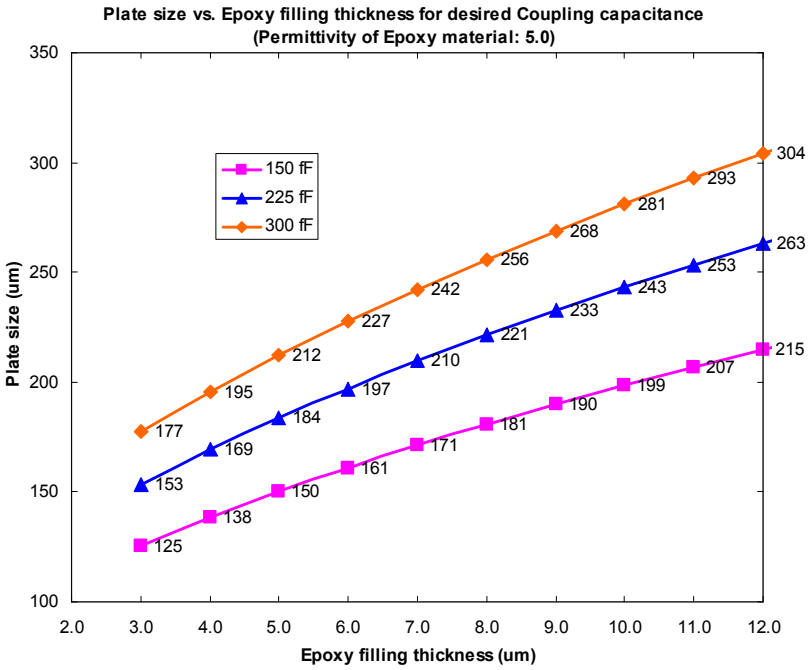


Figure 3.10. Requirements of plate size for various epoxy filling thickness

3.3.3. Coupling Capacitance of Metal Plate Pair with High-k Under-fill

The implementation of air gap capacitive coupling interfaces on MCM requires the chips and the substrate be brought into a very close proximity (1μm~2μm) to achieve the

desired capacitance for effective coupling due to the low permittivity of air gap (ε_r=1). This proximity requirement brings significant manufacturing challenges due to tolerance issues associated with such small dimensions.

Replacing the air gap with a high permittivity material can achieve higher capacitance density and thereby relax the proximity requirement between the chip and the substrate. Such a material can also provides stress relief by acting as an under-fill material and thus improves the overall reliability of capacitively coupled interconnect (CCI). Kim et al. developed a Barium Titanate (BaTiO3) and epoxy nano-composite, which has a permittivity up to 20 at multi-GHz and is a promising candidate for under-fill material in CCI [17].

A cross-section of capacitive coupling interface with high-k filling on MCM is shown in Figure 3.11. If the passivation layer on top of metal plates is removed, a high-k material is then used to fill the gap between coupling plate pairs. To reduce the un-wanted crosstalk between neighboring plates, the high-k under-fill layer needs be deposited with pattern rather than processed evenly.

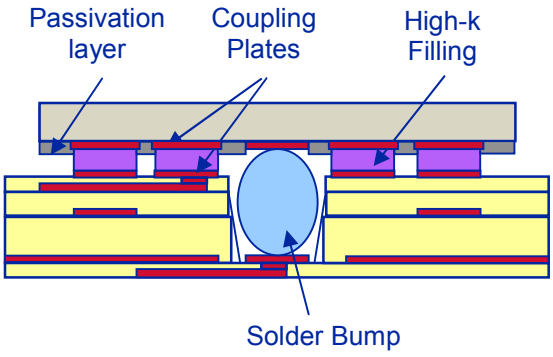


Figure 3.11. Cross-section of a capacitive coupling interface with high-k under-fill

For specified coupling capacitances, three curves of the requirement of plate size versus various high-k filling thickness (ε_r=20, 3~12μm) are shown in Figure 3.12. Compared to the capacitive coupling interfaces with air gap, the required minimum size of coupling plates in the capacitive coupling interfaces with high-k filling is reduced significantly due to the high capacitance density. For instance, at 3μm high-k underfill, the glass opening on top of metal plates could be as small as 54x54μm^2 to achieve the desired 150fF coupling capacitance. Considering the glass-metal overlap, typically 10μm, coupling plates could be 64x64μm^2. This would make a possible high-density capacitive coupling plates array with a pitch less than 75μm.

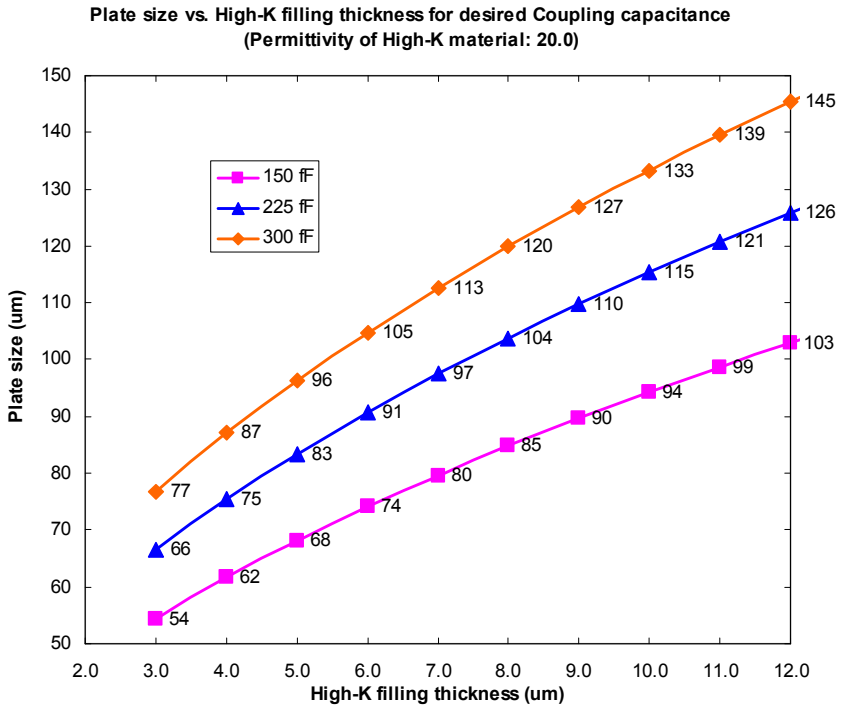


Figure 3.12. Requirements of plate size for various high-k filling thickness

3.3.4. Parasitic Capacitance of Metal Plate Pair

Beside the coupling capacitance, the parasitic capacitances of coupling plates need also be included in circuit simulations. Figure 3.13 shows a "pi" model of coupling plates, where C_c represents the coupling capacitance; C_{p1} represents the parasitic capacitance of plate on chip and C_{p2} represents the parasitic capacitance of plate on substrate.

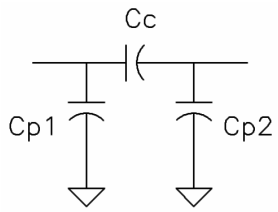


Figure 3.13. A "π" model for a coupling plate pair

For TSMC 0.18μm, 0.25μm and 0.35μm CMOS technologies, the unit area parasitic capacitance of top layer metal is 3.0aF/μm^2, 4.0aF/μm^2 and 6.3aF/μm^2, respectively. For the MCNC (RTI) MCM process, the unit area parasitic capacitance is only 0.87aF/μm^2. Ignoring the fringe parasitic capacitances because of the relatively big plates, the relationships between parasitic capacitances and the size of coupling plates are shown in Figure 3.14.

As the coupling plates are placed on the top layer metal of chip, an older CMOS technology has less metal layers and thus a larger parasitic capacitance of coupling plates. For a 200x200μm^2 metal plate, the on-chip parasitic capacitance is 120fF, 160fF and 252fF for 0.18μm, 0.25μm and 0.35μm technology, respectively. In the case of capacitive coupling with an air gap, the on-chip parasitic capacitances are comparable or even larger than the

coupling capacitance. It will bypass a large amount of signal energy and reduce the effective signal strength especially at the input of RX circuit.

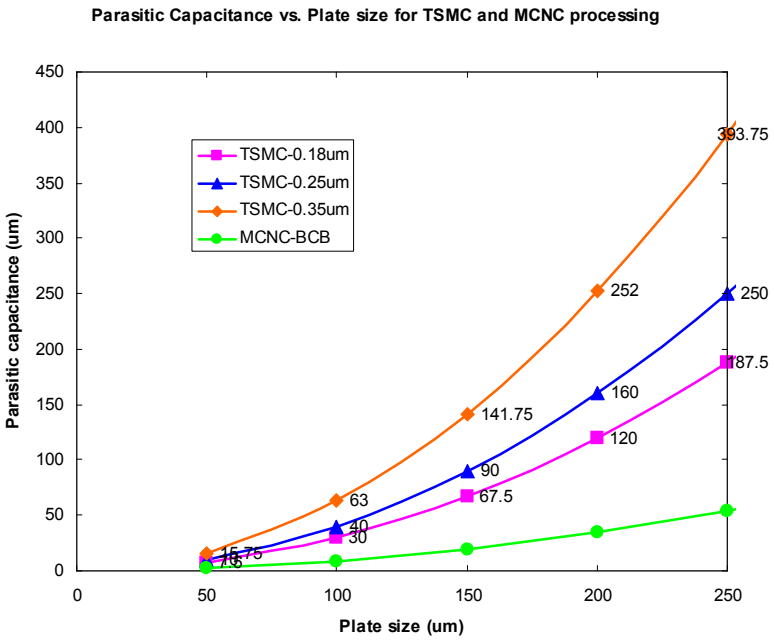


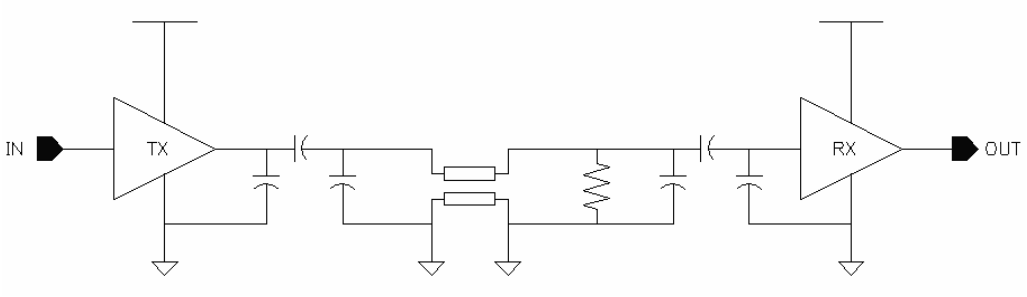
Figure 3.14. Parasitic capacitances for various coupling plate size

3.4. Capacitive Coupling Transceiver Circuit Design

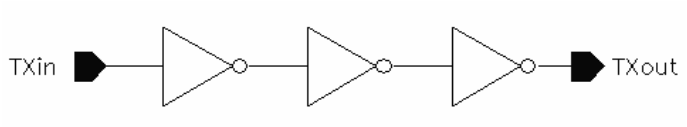
3.4.1. Single-ended Transceiver Circuit

A single-ended transceiver system for CCI, shown in Figure 3.15a, includes a transmitter (TX), two coupling capacitors, a transmission line, a termination resistor and a receiver (RX). The TX circuit, shown in Figure 3.15b, is a three-stage inverter chain. The last stage inverter is relatively large to drive the coupling capacitance of the series capacitor as

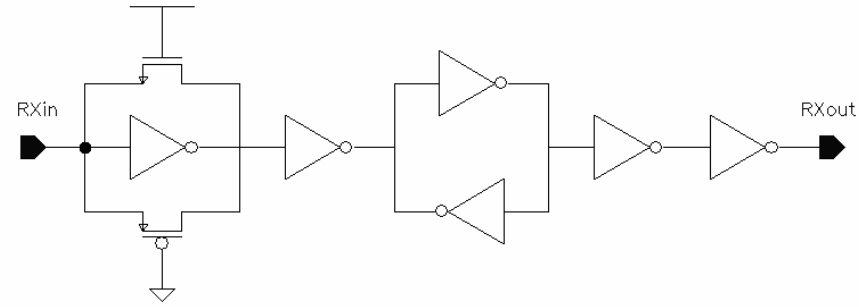
well as its parasitic capacitances. The first two inverters are sized to maintain a fast edge rates for the last inverter stage.



(a) Transceiver system



(b) Transmitter circuit



(c) Receiver circuit

Figure 3.15. Schematics of single-ended transceiver circuit for CCI

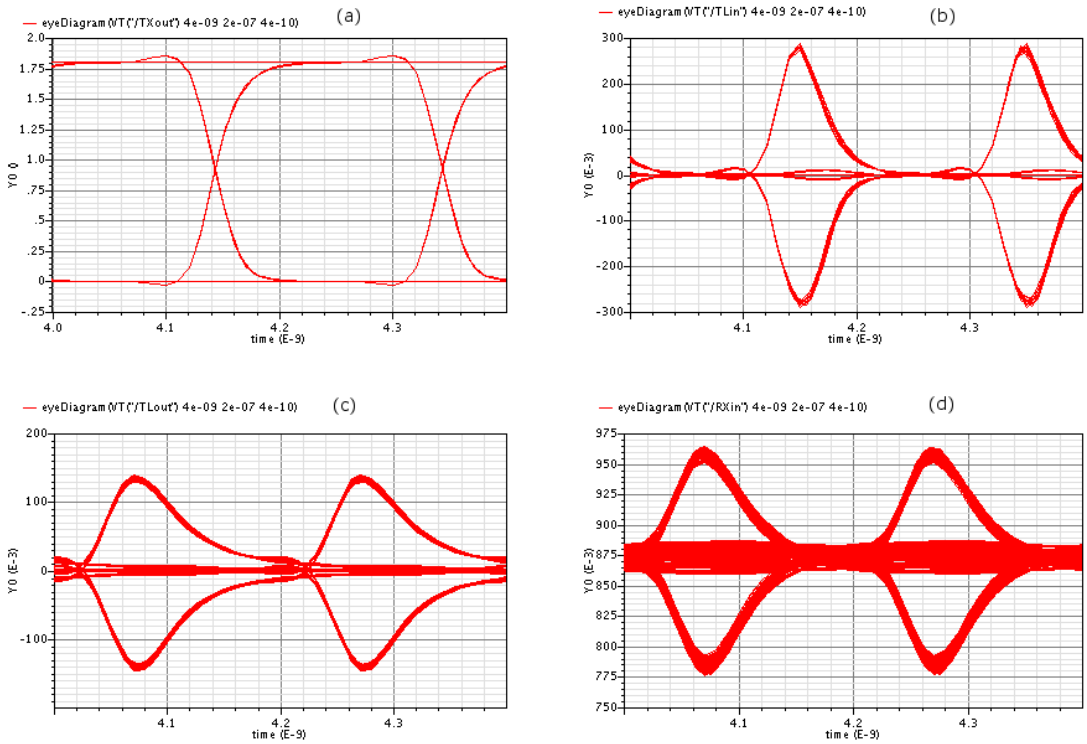
By passing through the first series capacitor, which has a high-pass characteristic and blocks DC components, the rising edges of NRZ signal are converted into positive voltage pulses, and the falling edges of NRZ signals converter into negative voltage pulses. As a lossy T-line has the properties of a low-pass filter, the voltage pulses transmitting over the T-

line will be degraded. Because the input impedance of RX circuit is much lager than the T-line characteristic impedance, the second series capacitor has a wider bandwidth than the first one. Those voltage pulses can pass the second series capacitor with some additional attenuation but little overshoot.

The function of a RX circuit is to sense the incident voltage pulses and restore them to full swing signals. A modified Kuhn receiver [34], shown in Figure 3.15c, was proposed to accomplish this function. Two feedback transistors, operating in the linear region, create a DC bias at half of the supply voltage (Vdd/2) for the first stage inverter and maintain that inverter amplifier to operate in the high gain region. Moreover, the feedback mechanism trades some inverter gain to expand the bandwidth of the inverter amplifier. The voltage pulses can be amplified with little distortion and it is very beneficial for jitter control. An inverter isolates the feedback from the rest of circuit and continues to amplify voltage pulses; a cross-coupled inverter pair forms a bi-stable latch to restore voltages pulses to NRZ signals; and the last two inverters are buffers to drive the output load.

For instance, a CCI channel includes two 150fF coupling capacitors and a 25cm 50ohm T-line, and transceiver circuits were designed in the TSMC-0.18μm CMOS technology. In simulation, source signals at the TX input are 5Gb/s PRBS data. Simulated eye-diagrams of signals along the CCI channel are shown in Figure 3.16.

Figure 3.16(a) shows waveforms at the TX output, which is in front of the first series capacitor. They are NRZ signals with a 1.8V swing, 200ps unit interval (UI) and 80ps transition time. Figure 3.16(b) shows waveforms at the T-line input, which is behind the first series capacitor. They are RZ bipolar pulses with a 280mV amplitude and 110ps width. The NRZ to RZ conversion is due to the high-pass characteristic of a small series capacitor.



(a) NRZ signals at TX output, (b) RZ pulses at T-line input, (c) Attenuated RZ pulses at T-line output, (d) Biased pulses at RX input

Figure 3.16. Simulated eye-diagrams of signals over a CCI channel

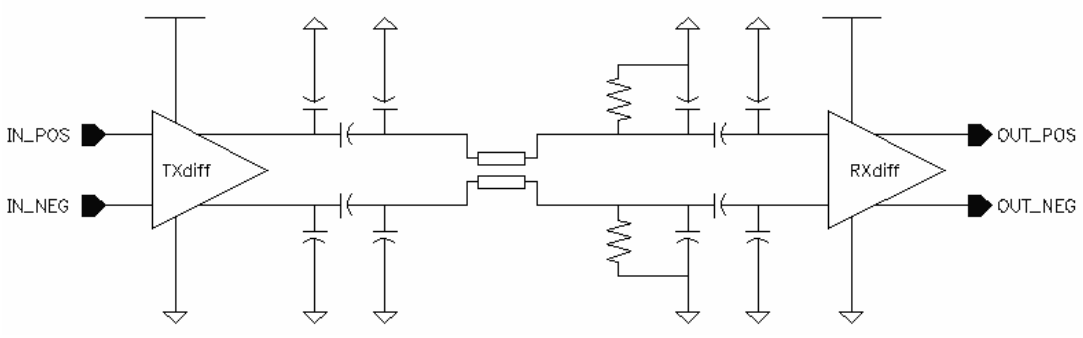
Figure 3.16(c) shows waveforms at the T-line output, which is in front of the second series capacitor. They are bipolar pulses with 140mV amplitude and 210ps width. The attenuation of pulse width and extension of pulse tail are due to the low-pass characteristic of a lossy T-line. Figure 3.16(d) shows waveforms at the RX input, which is after the second series capacitor. They are bipolar pulses biased at 870mV, which is approximately equal to Vdd/2. The pulse amplitude was attenuated to 80mV and pulse width was decreased to 120ps due to the high-pass characteristic of second series capacitor.

It can be observed that the pulses at the RX input have some overshoot, which is due to the differentiation property of the series capacitor. Because of the relatively high input impedance of the RX, e.g. 570ohm, the overshoot is damped to acceptable amplitude. The pulse width at the RX input is less than one UI. It will leave some margin for inter-symbol interference (ISI) at the RX circuit. The pulse shape is independent of the data pattern; it depends on the edge rate of NRZ data and is regulated by the CCI channel. The regulated narrow pulses are equalized signals to the RX circuit, so a CCI channel provides passive equalization and relieves the requirements of equalization in TX or RX circuits.

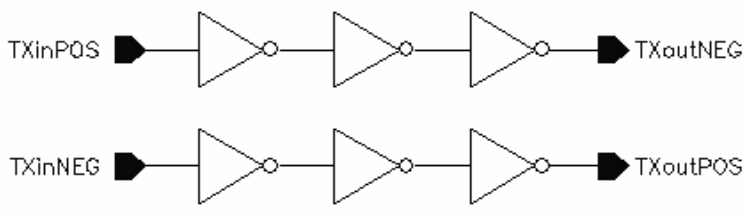
3.4.2. Differential Transceiver Circuit

A differential transceiver system for CCI is shown in Figure 3.17a, which includes a differential TX, a pair of coupled T-lines, two pairs of series capacitors, two terminators and a differential RX. A schematic of a differential TX, which includes two inverter chains operating complementary, is shown in Figure 3.17b.

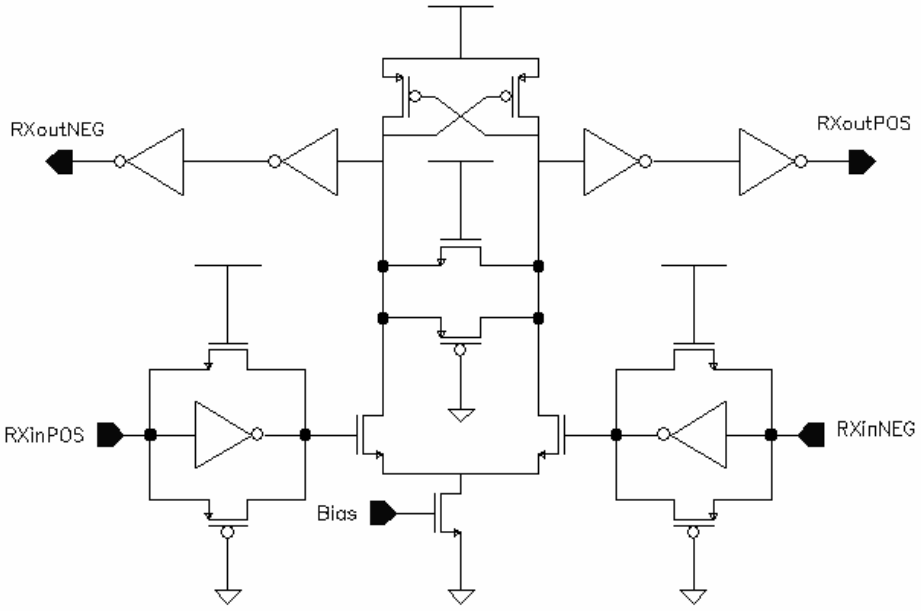
The reason to apply differential structure is to improve common-mode noise rejection and the detection sensitivity of RX. A differential RX, shown in Figure 3.17c, includes a sensing stage that composed by two inverters with feedbacks, a latch stage that is a cross-coupled differential amplifier and a buffer stage that uses two inverters.



(a) Differential transceiver (TRX) system



(b) Differential transmitter (TX) circuit



(c) Differential receiver (RX) circuit

Figure 3.17. Schematics of differential transceiver circuit for CCI

In the sensing stage, feedback transistors build DC bias voltages for the inputs of RX and maintain the inverter amplifier to operate in a high gain region. In the latch stage, two cross-coupled transistors create a positive feedback mechanism that can accelerate transitions of the amplifier; two spanning transistors compensate the cross-coupled transistors and improve the stability of amplifier. The latch stage converters differential voltage pulses into large swing complementary signals, and the voltage buffers restore them to full swing complementary NRZ signals.

3.5. Demonstration of Capacitively Coupled Interconnect on MCM

3.5.1. Overview

A demonstration system for CCI chip-to-chip communications on MCM was built and tested. Figure 3.18 shows a schematic for a CCI transceiver system on a MCM. Transceiver test chips were fabricated in TSMC-0.35μm CMOS technology. A MCM silicon substrate was fabricated by MCNC (RTI) with copper deposition and BCB spin-on technology. Test chips were flipped and assembled on the common substrate. Coupling capacitors were formed at the interfaces between the chips and the substrate; the coupling plate size was 200x200μm^2 and the gap between two plates was approximately 1μm. A 5.6cm 50ohm micro-strip copper trace was placed in the BCB layers of the substrate to connect two series capacitors. Figure 3.19 depicts the physical structure for CCI in MCM, which include a 3-D view and a cross-section view.

In measurements, two single-ended transceiver channels operated simultaneously at 2.5Gb/s data rate.

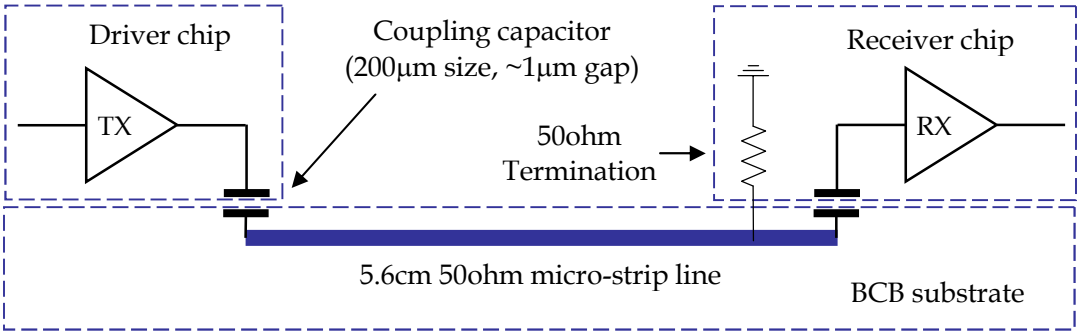
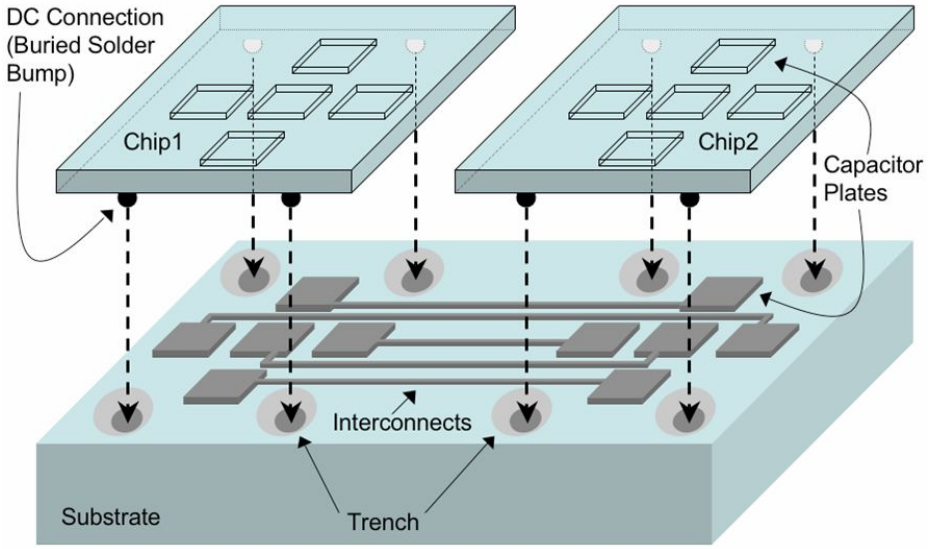
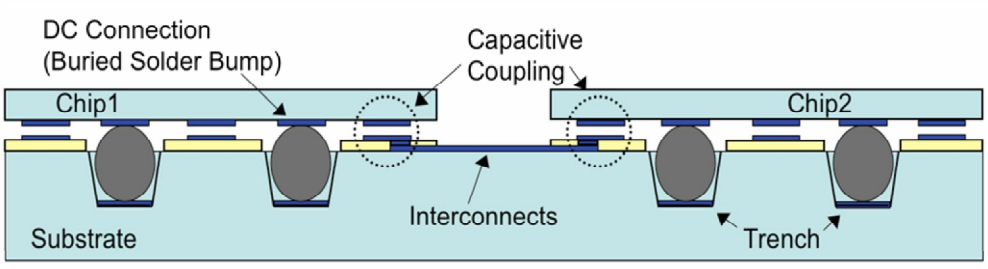


Figure 3.18. Schematic for CCI transceiver system on MCM



(a) 3-D view for CCI on MCM

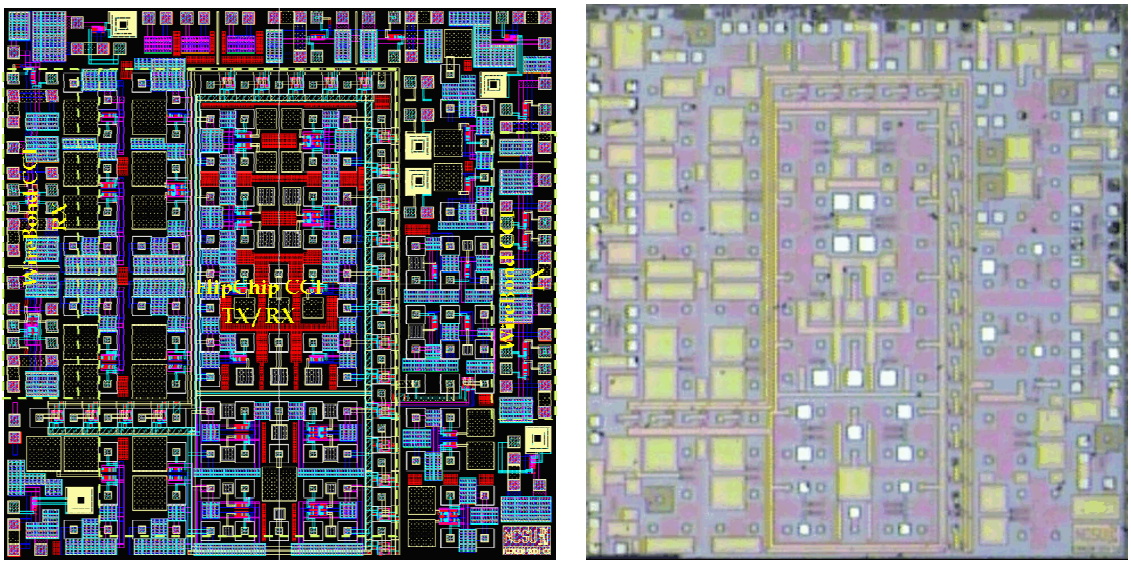


(b) Cross-section view for CCI on MCM

Figure 3.19. Physical structures of CCI on MCM

3.5.2. Test Chip and MCM Design

A CCI transceiver test chip (3.2x3.2mm^2), shown in Figure 3.20, was fabricated in 0.35μm CMOS technologies. It includes single-ended circuits as well as differential circuit with various coupling capacitances.



(a) Layout (b) Micrographic

Figure 3.20. Layout and micrographic of a TSMC-0.35μm test chip for CCI

A MCM (1.0x0.5inch^2), shown in Figure 3.21, was fabricated by MCNC (now RTI) with BCB deposition technology. Two transceiver test chips were flipped and assembled on a common substrate; the left one acted as a TX chip and the right one acted as a RX chip. Termination resistors were created on test chips by using poly-silicon; and flip-chip style decoupling capacitor array were mounted on the substrate.

Figure 3.22 depicts a cross-section view for chip-substrate interfaces. Solder bumps were buried into trenches in the substrate. They provide mechanical support as well as electrical DC connections to the flip-chip. Metal plate pair at the chip-substrate interfaces forms coupling capacitors.

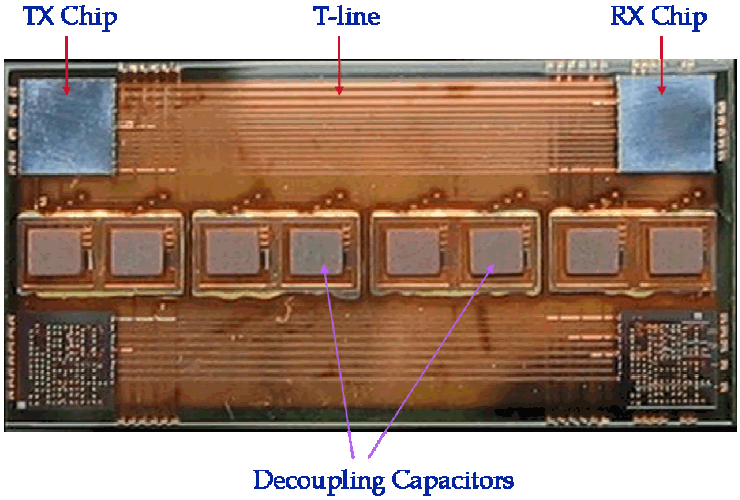


Figure 3.21. Picture of a MCM under test (1.0”x0.5”)

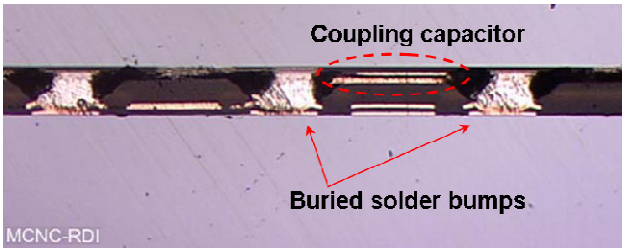


Figure 3.22. Cross-section view for chip-substrate interfaces in a MCM

3.5.3. Test Structures

A test structure of a CCI transceiver system for on MCM is shown in Figure 3.23. The input signals at the TX were delivered through a RF probe (GGB model 40A, 50ohm); the output signals at the RX were sensed through a high-impedance probe (GGB model 35, 50fF, 1.25Mohm). A demonstration system for CCI on MCM with input/output probes in place is shown in Figure 3.24.

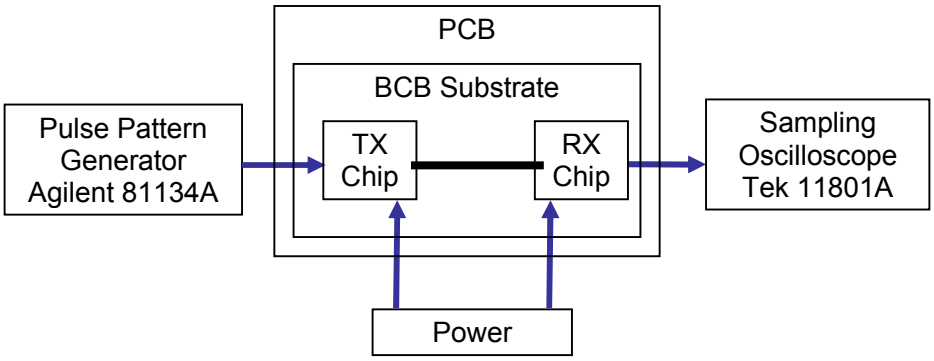


Figure 3.23. A test structure of a CCI transceiver system on MCM

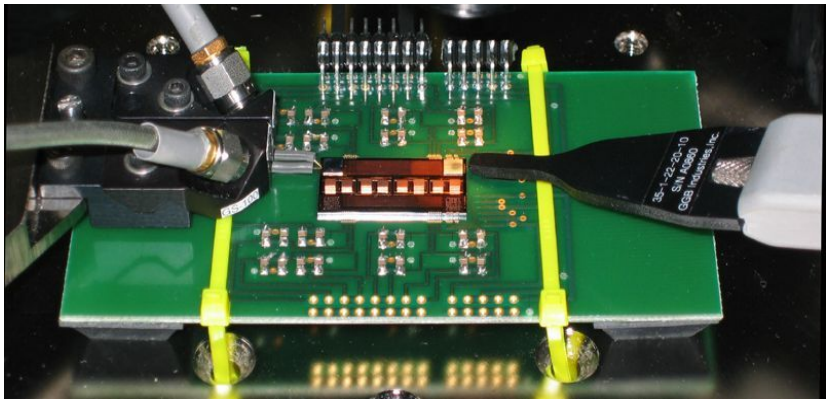


Figure 3.24. A demonstration system for CCI on MCM with probes setting-up

3.5.4. Measurement Results

Two CCI channels operated simultaneously. One channel was fed by a 2.5Gb/s 32bit arbitrary pattern data, and the other channel was fed by a 2.5Gb/s PRBS data. The measured waveform at the RX output of the first channel is shown in Figure 3.25.

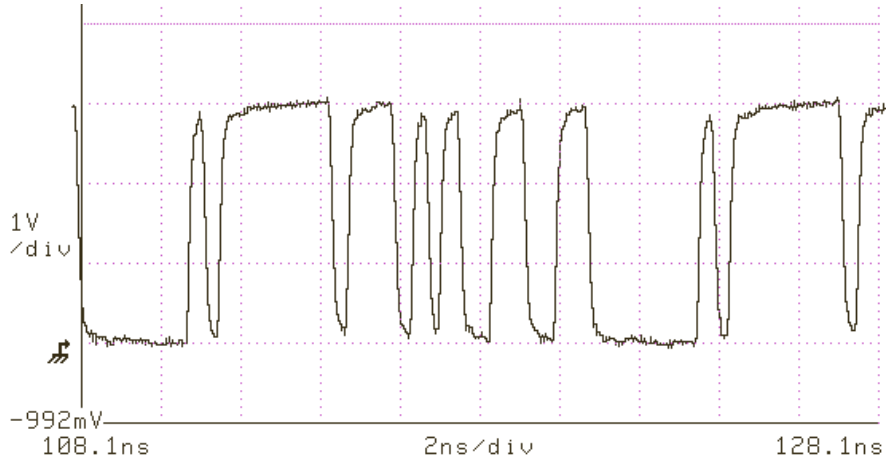


Figure 3.25. Measured output waveform in CCI on MCM for 2.5Gb/s arbitrary data

When both CCI channels were fed by 2.5Gb/s 2^7-1 PRBS data, a measured eye-diagram at the RX output of the first channel is shown in Figure 3.26, where the peak-to-peak jitter is less than 120ps. In BER measurements, this transceiver system transmitted 4 trillion bits without error at 2.5Gb/s data rate; it achieved a BER less than 10^{-12}. A CCI transceiver channel consumes 25.3mW power, in which the TX and the RX consume 10.3mW and 15.0mW, respectively. Table 3.2 summarizes the performance of CCI demonstration in MCM.

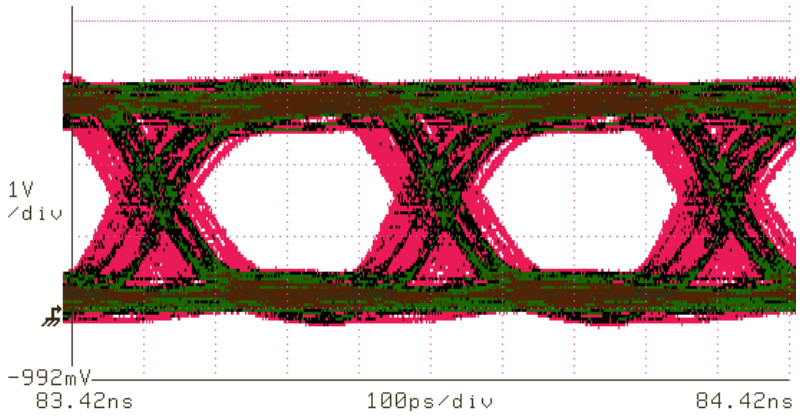


Figure 3.26. Measured eye-diagram in CCI on MCM for 2.5Gb/s PRBS

Table 3.2. Performance summary for CCI on MCM

Chip technology	TSMC-0.35μm CMOS
MCM technology	MCM-D with BCB
Supply voltage	3.3V
T-line length	5.6cm micro-strip line
Coupling plate size	200x200 μm^2
Data rate (PRBS)	2.5Gb/s per channel
Power per channel	TX: 10.3mW, RX: 15.0mW
Bit error rate (BER)	$< 10^{-12}$
Jitter at RX out	< 120ps peak-to-peak

3.6. Demonstration of Capacitively Coupled Interconnect on PCB

3.6.1. Overview

A demonstration system for CCI chip-to-chip communications on PCB was built and tested. Figure 3.27 illustrates a transceiver system for CCI on PCB. Transceiver test chips

were fabricated by MIT Lincoln lab in 0.18μm fully-depleted SOI technology, which is described in Appendix A; coupling capacitors were embedded in the test chips; bare chips were mounted on a PCB directly; a 17cm 50ohm micro-strip copper trace on the PCB connected two test chips via wire bonding.

For square-wave clock inputs, this transceiver system operates at a frequency up to 3.0GHz and consumes 9.90mW power. For arbitrary pattern data inputs, this transceiver system works at 2.0Gb/s data rate with 35% data activity and consumes 6.98mW power. For PRBS data inputs, this transceiver system consumes 7.35mW power at 2.0Gb/s data rate and maintains a jitter less than 80ps on the eye-diagram at RX output.

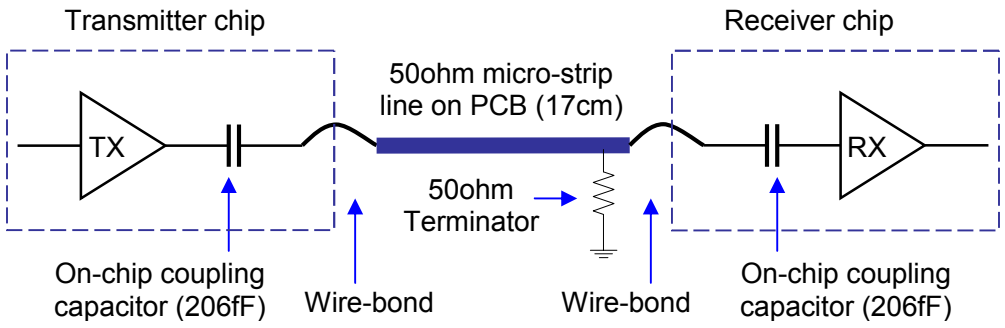
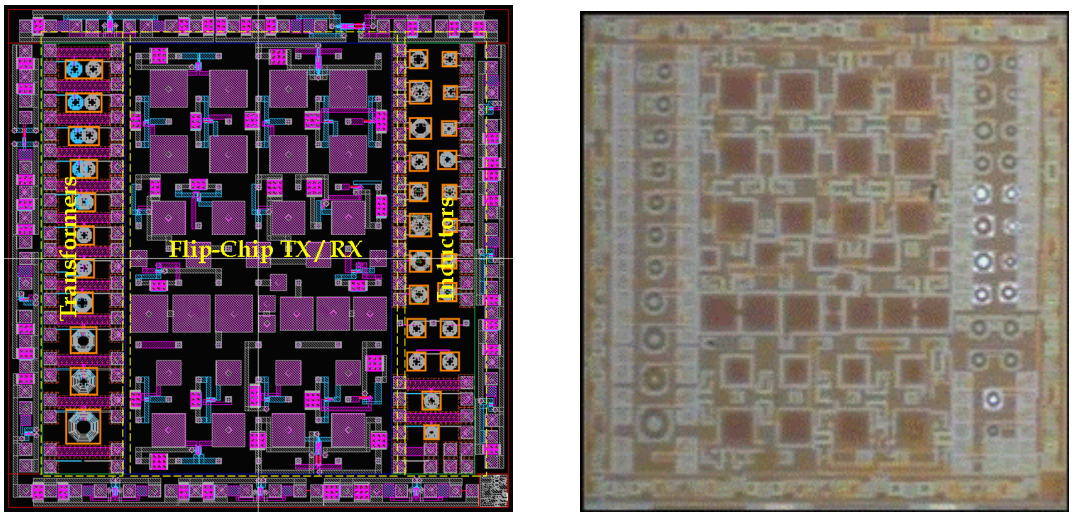


Figure 3.27. Schematic of a CCI transceiver system on PCB

3.6.2. Test Chip and PCB Design

A CCI transceiver test chip (3.0x3.0mm^2), shown in Figure 3.28, was fabricated in 0.18μm fully-depleted SOI technology. It includes single-ended circuit as well as differential circuit with various coupling capacitances. It also includes transceiver circuits for CCI flip-

chip experiments and some passive test structures for on-chip inductor and transformers, which are not reported in this dissertation.



(a) Layout (b) Micrographic

Figure 3.28. Layout and micrograph of a 0.18μm fully-depleted SOI test chip for CCI

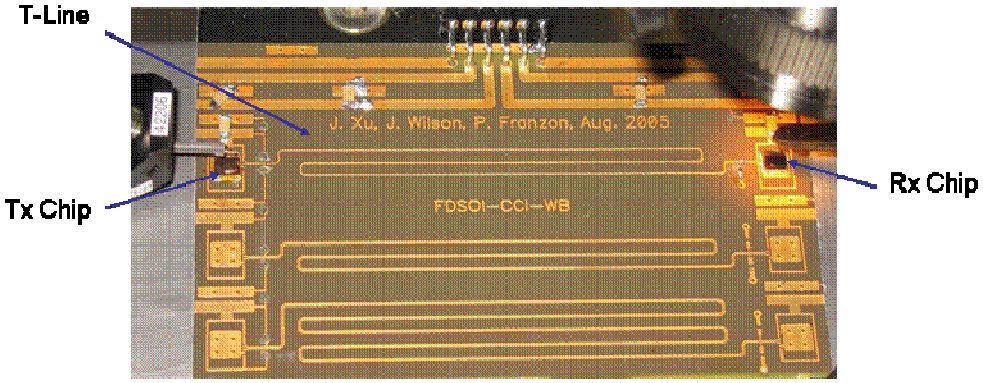


Figure 3.29. A test vehicle to demonstrate CCI on PCB

A test vehicle for CCI chip-to-chip communication on PCB is shown in Figure 3.29. Two transceiver chips were glued on the PCB directly, where the left one acted as a TX chip

and the right one acted as a RX chip; Termination resistors and decoupling capacitors were soldered on the PCB. The top of PCB pads were coated with a gold layer; and bonding wires connected chips and the PCB.

3.6.3. Measurement Results

A test structure of a transceiver system for CCI on PCB is shown in Figure 3.30. Both TX chip and RX chip were supplied with 1.5V voltage. Input signals at the TX were delivered through a RF microprobe (50ohm); output signals at the RX were picked up through a high-impedance microprobe (50fF, 1.25Mohm).

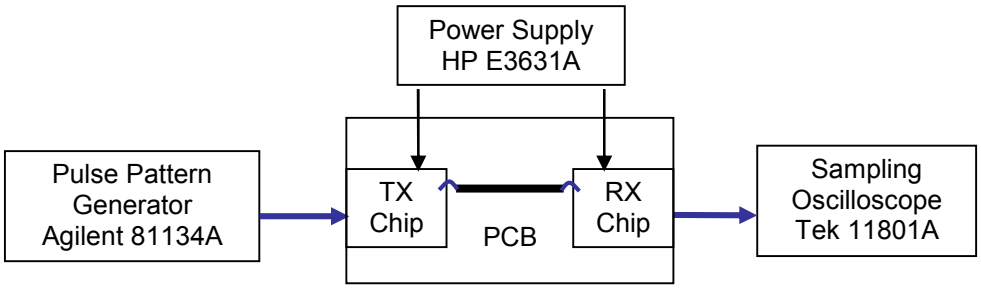


Figure 3.30. A test structure of a CCI transceiver system on PCB

For 3.0GHz square wave clock inputs, the measured waveform at the RX output is shown in Figure 3.31. A single-ended CCI transceiver consumes 9.9mW power, where the TX and the RX consume 2.4mW and 7.5mW, respectively.

For 2.0Gb/s arbitrary pattern data inputs, the measured waveform at the RX output is shown in Figure 3.32, where the 40bits pattern, 0000,0001,0000,1111,1111,0111,1010,0010,

1000,0110 has a 35% data activity. A CCI transceiver consumes 7.0mW power, where the TX and the RX consume 0.4mW and 6.6mW, respectively.

Figure 3.31. Measured 3.0GHz clock waveform at RX output in CCI on PCB

Figure 3.32. Measured 2.0Gb/s pattern waveform at RX output in CCI on PCB

For 2.0Gb/s 2^7-1 PRBS data, the measured eye-diagram at the RX output is shown in Figure 3.33, where the peak-to-peak jitter is less than 80ps. A CCI transceiver channel consumes 7.35mW power, where the TX and the RX consume 0.57mW and 6.78mW, respectively.

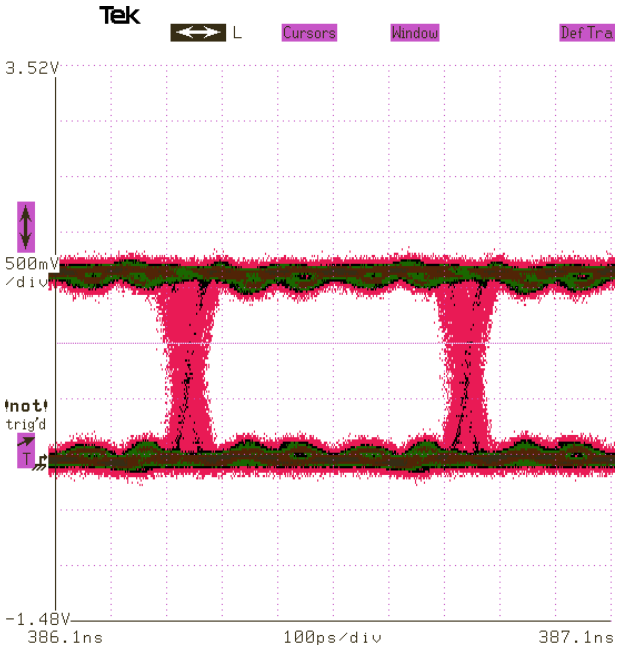


Figure 3.33. Measured eye-diagram at RX output in CCI on PCB for 2.0Gb/s PRBS

The data rate of the CCI on PCB transceiver system was limited by the switching noise excited by the bonding wires of power/ground connections. The switching noise can be estimated by *L*di/dt*, where *L* represents the inductance of off-chip connections such as bonding wires or solder bumps, *di/dt* represents the transition rate of supply current which is associated with data rate and drive/load impedance. For instance, a 2mm bonding wires has a parasitic inductance around 2nH; if a current rises from 0 to 1mA in 100ps, the excited

switching noise could be around 20mV. There are some on-chip decoupling capacitors for each power/ground pair. However, they may not be large enough to compensate for all the switching noise. At a higher data rate, the switching noise disturbed the sense and latch stages of the RX circuit and then introduced uncertainty and errors in pulse recovery.

It was observed that the power consumption of the RX circuit was not proportional to the communication data rate. The reason is the first stage of RX circuit is biased at Vdd/2, it consumes a large amount of static power which is about 5.5mW and independent with the data rate or data activity.

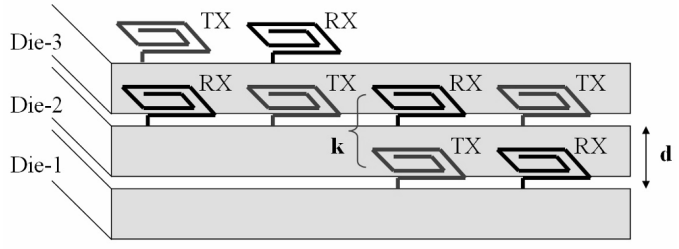
Chapter 4. Inductively Coupled Interconnect (LCI) for Vertical Connections in 3D-ICs

4.1. Overview

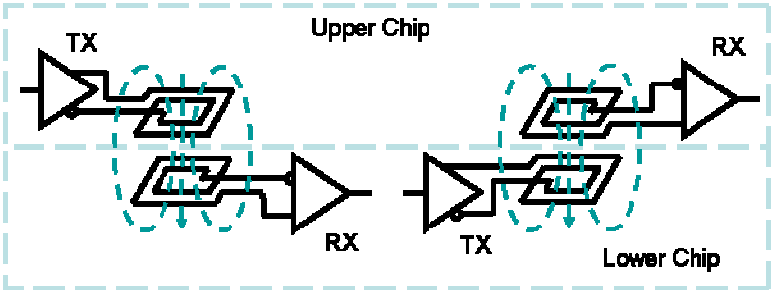
ACCI has a non-contacting structure; it is an attractive alternative to vertical connections such as through-vias or micro-bumps in three-dimensional ICs. This chapter addresses the characterizations for inductive coupling interfaces in 3D-ICs. It presents an inductive coupling demonstration system in a two-chip stack. This chapter presents a new power delivery scheme for LCI in 3D-ICs, which provides AC connections via LCI interfaces and DC connections at polished chip edges. It also presents an integrated 3D-ICs structure that combines LCI and 3D vertical via technologies.

4.2. Characterization for LCI interface in 3D-ICs

The concept of inductively coupled interconnects for 3D-ICs is illustrated in Figure 4.1, where multiple chips are thinned and stacked face-to-back. The two spiral inductors in neighboring chips overlap and form an inter-chip transformer that communicates digital signals between a TX and a RX.



(a) 3-D view of a physical structure for LCI in 3D-ICs



(b) Schematic of LCI vertical signaling in 3D-ICs

Figure 4.1. Concept of inductively coupled interconnect (LCI) in 3D-ICs.

The inter-chip transformer used in the inductively coupled interconnect must be modeled accurately. The magnetic coupling coefficient (k) depends strongly on the separation distance (d) between the primary and secondary inductors. In 3D-ICs, the separation distance proximately equals to the thickness of the chips in the stack while ignoring any gap between the chips. For 150μm and 100μm double-layer inductors, the relationship between the coupling coefficient and the chip thickness, which was simulated using ASITIC [58], is plotted in Figure 4.2. For a 90μm thick chip, the coupling coefficient between two 150μm inductors is only around 0.05.

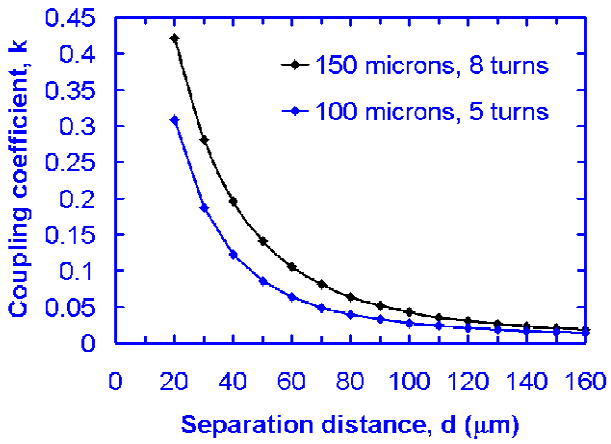


Figure 4.2. Dependence of coupling coefficient on separation distance

A lumped differential model for the inter-chip transformer was extracted from simulation results and is shown in Figure 4.3. Where *L1* and *L2* represent the self-inductances, *k* represents the coupling coefficient, *R1* and *R2* represent the winding resistances, *C12* and C21 represent the coupling capacitances between two overlapping inductors, *Rs* and *Cs* represent the parasitic resistances and capacitances of inductor windings.

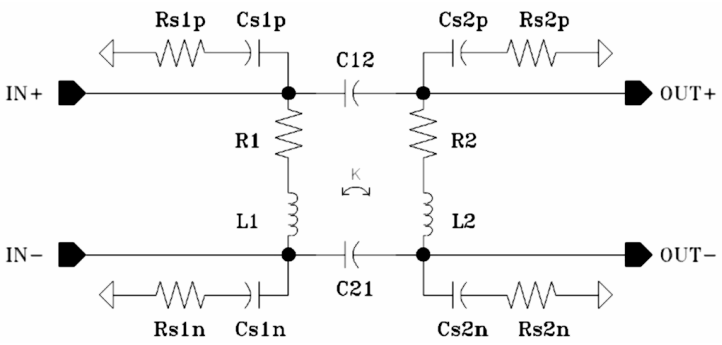


Figure 4.3. A differential inter-chip transformer model

4.3. Inductively Coupled Interconnect in a Two-Chip Stack

4.3.1. Overview

An inductively coupled interconnect scheme for vertical signaling in 3D-ICs is demonstrated. Test chips were fabricated in TSMC 0.35µm CMOS technology, then thinned and stacked. For 90µm thick chips using 150µm inductors, the transceiver communicates NRZ signals at 2.8Gb/s, and tolerates up to 50µm misalignment. TX and RX power dissipation are 10.0mW and 37.6mW, respectively. The transceiver circuit does not require a clock to recover the data and is able to maintain less than 100ps jitter at the RX output. The measured BER at 2.5Gb/s data rate is $<10^{-13}$.

4.3.2. Transceiver Circuit Design

A schematic of the current-mode transceiver circuit used for inductively coupled interconnects is shown in Figure 4.4. The TX circuit is implemented using an H-bridge current steering structure. A non-return-to-zero (NRZ) input signal and its complementary signal are used to switch the H-bridge and steer the current directions in the primary inductor of the inter-chip transformer. The alternating current generates an alternating magnetic field and induces current pulses in the secondary inductor.

The RX circuit can be divided into a sensing stage, an amplifying stage and a latching stage. The sensing stage of the RX, which forms a structure with low input impedance, detects current pulses from the secondary inductor and converts them into voltage pulses.

The amplifying stage amplifies those voltage pulses. The latching stage converts them into NRZ signals.

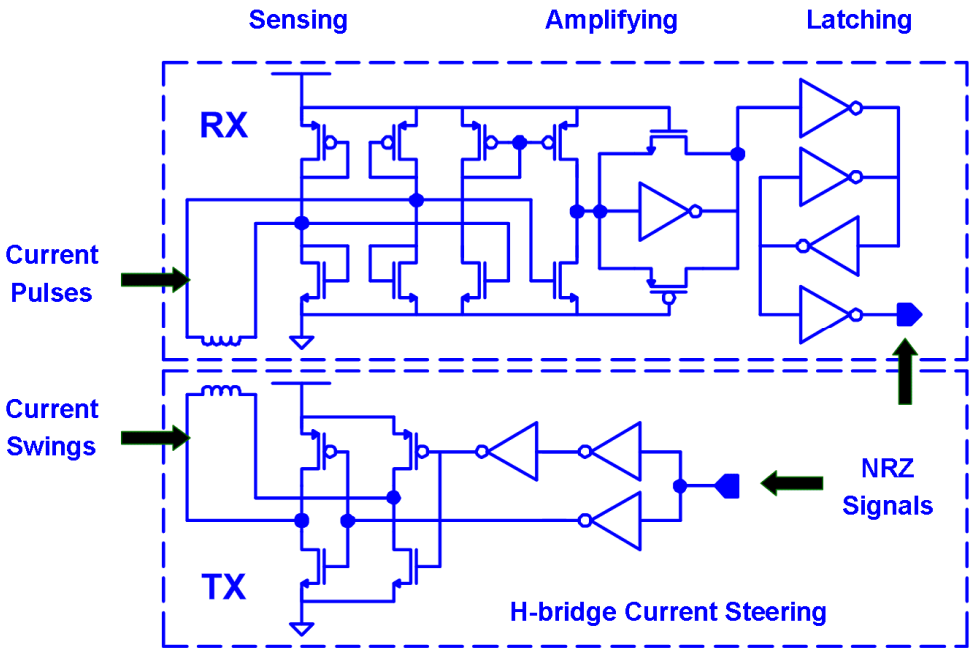
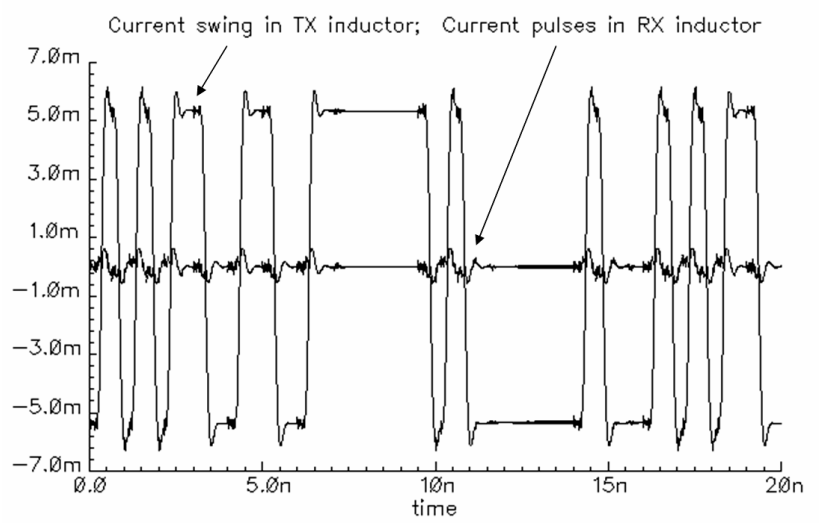
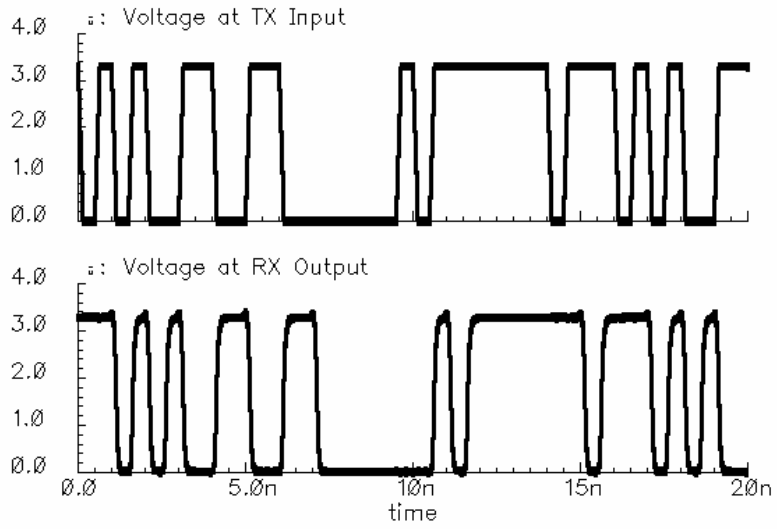


Figure 4.4. A transceiver circuit for LCI in 3D-ICs

Simulation results of the transceiver system are shown in Figure 4.5. The current signal in the TX inductor is bipolar swings and the current signal in the RX inductor is bipolar pulses, in which positive or negative pulse correspond the rising or falling edge of current swing in the TX inductor. The RX output signal is logically identical to the TX input signal except for some delay.



(a) Current in the inter-chip transformer



(b) Voltage at TX input and RX output

Figure 4.5. Simulation results of a transceiver for LCI in 3D-ICs

4.3.3. Experiment Scheme

A test chip, shown in Figure 4.6, for demonstrating the inductively coupled interconnect scheme was fabricated in the TSMC 0.35μm CMOS technology. A two-chip

stack demonstration system is shown in Figure 4.7. The bottom chip was used as the TX and was mounted on a PCB. The top chip was used as the RX and was thinned to the desired thickness, then rotated 90^{o}, aligned and stacked on the bottom chip. The top chip was glued onto a micromanipulator, which was used to provide precise positioning in X and Y directions. The top chip was pushed onto the bottom chip to close the gap between them.

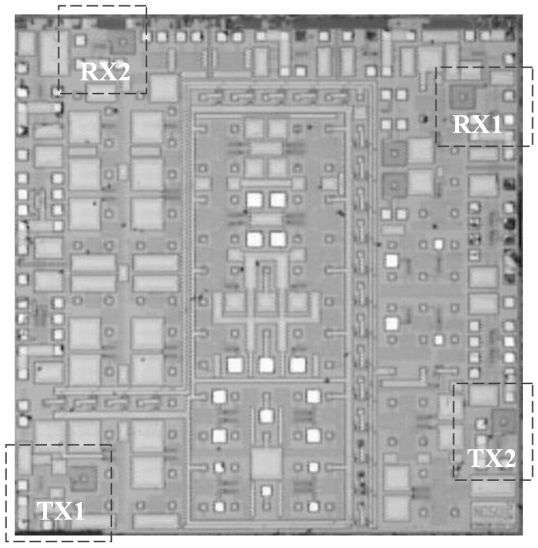


Figure 4.6. Microphotograph of test chip for LCI in 3D-ICs (3.2x3.2mm^2)

Alignment marks were included in the layout of the chip, and are visible for both top and bottom chips. By referring to the alignment marks and adjusting the micromanipulator, it is possible to achieve perfect overlap of the coupled inductors. It also allows for arbitrary offsets of the inductors, making it possible to explore the tolerance of the transceiver system to misalignment in the 3-D assembly. Figure 4.8 shows a 3-D test structure under measurement.

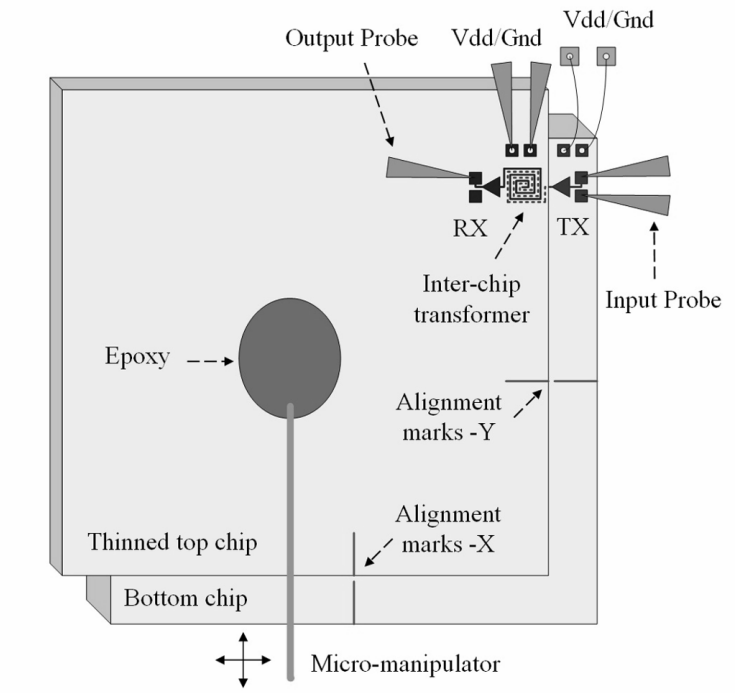
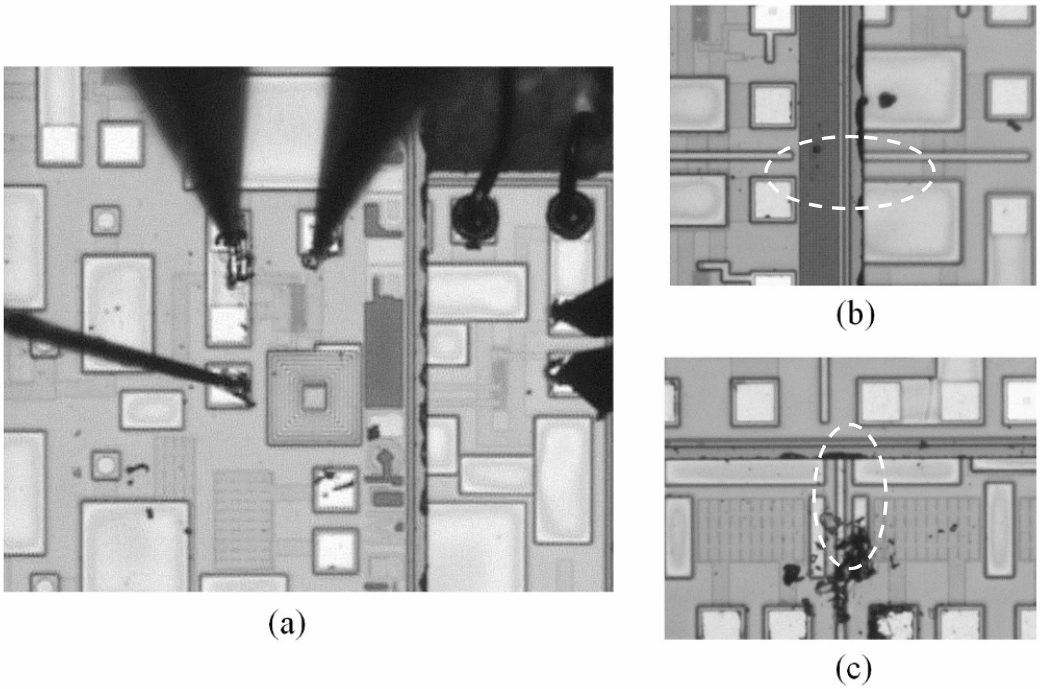


Figure 4.7. A demonstration system of LCI in a two-chip stack

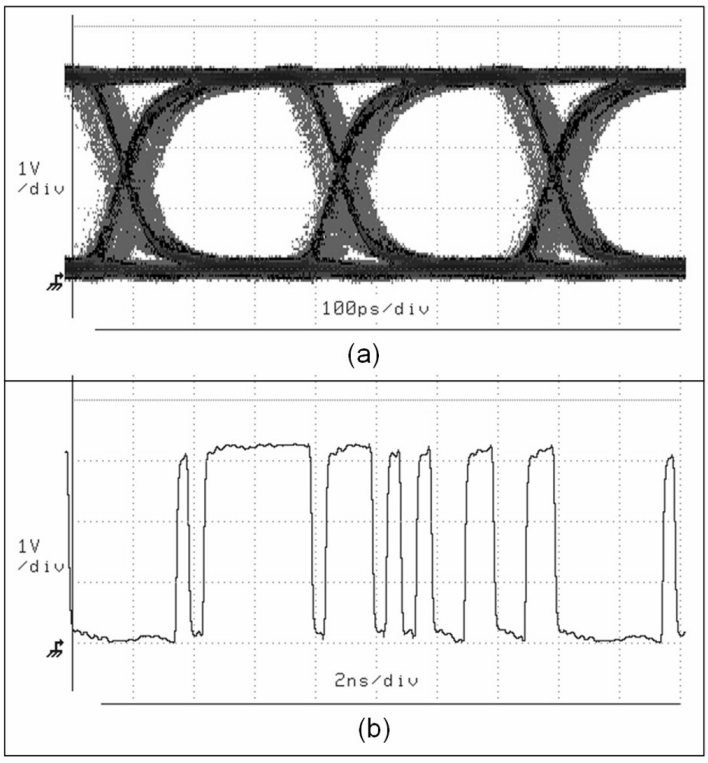


(a) Two chips stack with probes setting-up, (b) Alignment marks in Y direction with 0 offset, (c) Alignment marks in X direction with 20μm offset.

Figure 4.8. Test structure for emulating 3D-ICs assembly

4.3.4. Experiment Results

For a double layer 150x150μm^2 spiral inductor with eight turns per layer, the measured self-inductance is ~27nH. An inter-chip transformer was formed by overlapping such two inductors. Measurements of this inductively coupled transceiver channel produced a maximum signaling rate of 2.8Gb/s for a 2^7-1 pseudorandom binary sequence (PRBS) when the top chip was thinned to 90μm. The accumulated eye diagram at the RX output is shown in Figure 4.9 (a). A transient waveform at the RX output for a 2.0Gb/s arbitrary data pattern is also shown in Figure 4.9 (b).



(a) Eye diagram at RX output for 2.8Gb/s PRBS, (b) Waveform at RX output for 2.0Gb/s arbitrary pattern.

Figure 4.9. Measurement results for 90μm thick LCI test chip in 3D-ICs.

To study the dependence of the coupling coefficient on the chip thickness in 3D-ICs, the top chips were thinned to 90μm, 105μm and 120μm, and each was then stacked on the bottom chip for measurement. In the case of perfect alignment at the same data rate (2.0Gb/s), the thinner the chip, the less jitter was observed in the eye diagram at the RX output.

The power dissipation for one pair of TX/RX is 47.6mW, in which the TX consumes 10.0mW and the RX consumes 37.6mW. The transceiver circuit does not require external support circuitry or a clock to recover the data and is able to maintain less than 100ps peak-to-peak jitter in the eye diagram at the RX output.

4.3.5. Misalignment Tolerance

The coupling coefficient determinates the strength of receiving signal at the RX input; it is not only sensitive to the vertical separation distance between two coupled inductors, but also sensitive to the horizontal offset between them. Figure 4.10 illustrates the relationship between the coupling coefficient and the horizontal offset, or misalignment, for chip thickness equal to 90μm, 105μm and 120μm, based on ASITIC simulations.

To investigate the tolerance of an inductively coupled transceiver system to the horizontal misalignment in a 3-D assembly process, measurements at arbitrary offsets between two coupled inductors in X and/or Y direction were performed. Figure 4.11 illustrates a shmoo plot for measured misalignment tolerances at 2.0Gb/s data rate, where a

dot point indicates a valid operation; and a triangle point indicates an invalid operation. The criteria for pass/fail are 0.7UI eye-opening at RX output.

To operate the transceiver system at a data rate of 2.0Gb/s with the top chip thinned to 90μm, 105μm and 120μm, the inter-chip transformer can tolerate 50μm, 20μm and 5μm misalignment in both X and Y directions, respectively.

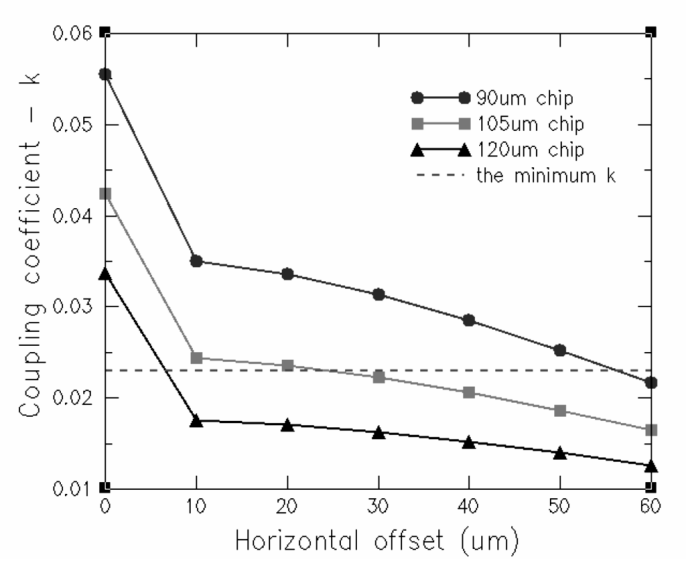


Figure 4.10. Coupling coefficient sensitivity to horizontal offset

The measurement results correlate well with the simulation results. The required minimum coupling coefficient defines a boundary between the regions of valid operation and invalid operation, for this work the minimum coupling coefficient is approximately 0.023. For instance, with 90μm chip thickness and 40μm offset, the simulated coupling coefficient is 0.028.

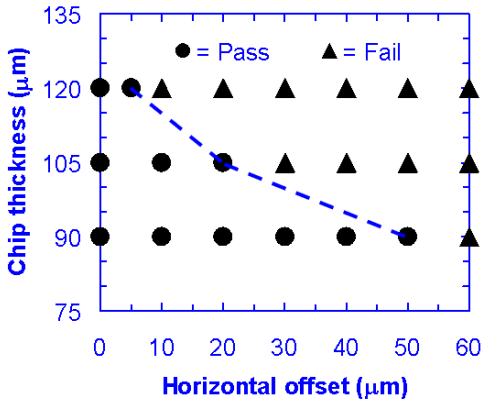


Figure 4.11. Shmoo plot for measured misalignment tolerances at 2.0Gb/s data rate

4.3.6. Crosstalk

To explore the density or pitch of coupling elements, the crosstalk between neighboring inductors was measured. A crosstalk test structure is shown in Figure 4.12 and the measured isolation, S_{21}, between two neighboring inductors is plotted in Figure 4.13. For frequencies up to 5GHz, there is at least 40dB of isolation with 50μm of spacing between inductors, which is 1/3 of the inductor diameter. The scattering parameter S21 represents the forward transmission coefficient.

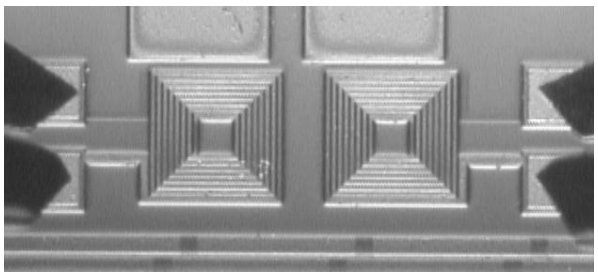


Figure 4.12. Test structure for measuring the crosstalk between neighboring inductors.

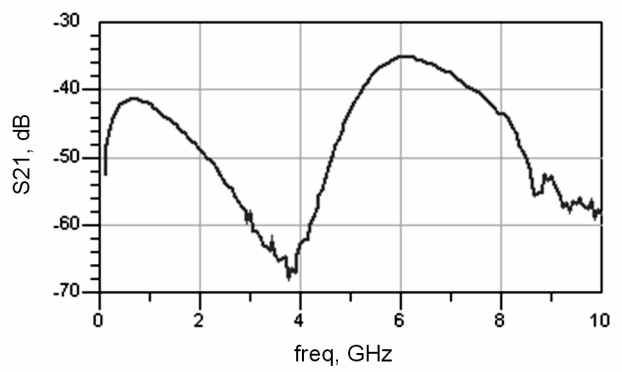


Figure 4.13. Measured isolation between two neighboring inductors

4.3.7. Summary

A demonstration system for inductively coupled interconnects in 3D-ICs was built and tested. The inductive coupling behavior as a function of vertical separation and horizontal offset was also explored. For a 90µm thinned chip with a 150µm spiral inductor, the transceiver communicated PRBS signals at a data rate of 2.8Gb/s and tolerates up to 50µm misalignment. The transceiver circuit does not require any external support circuitry or a clock to recover the data and is able to maintain peak-to-peak jitter less than 100ps in the eye diagram at the RX output. Performance summary for LCI vertical signaling in 3D-ICs is illustrated in Table 4.1.

Table 4.1. Performance summary for LCI in 3D-ICs

Chip technology	TSMC-0.35µm CMOS
Data rate (PRBS)	2.8Gb/s
Power dissipation	TX: 10.0mW, RX: 37.6mW
Bit error rate (BER)	$< 10^{-13}$ (measured at 2.5Gb/s)

4.4. LCI in a Two-Chip Stack with Edge DC Connections

4.4.1. Physical Structure

Vertical connections between stacking dies in 3D-ICs include both AC connections such as data/clock signals and DC connections such as power/ground distributions. LCI have been demonstrated previously for high-speed vertical signaling in 3D-ICs. A vertical inter-connection scheme that provides AC connections via LCI interfaces and DC connection via wire-bonding is shown in Figure 4.14. In this scheme, the dimension of an upper die must be smaller than the lower one to expose wire-bonding pads. This indentation structure limits the total number of stacked dies.

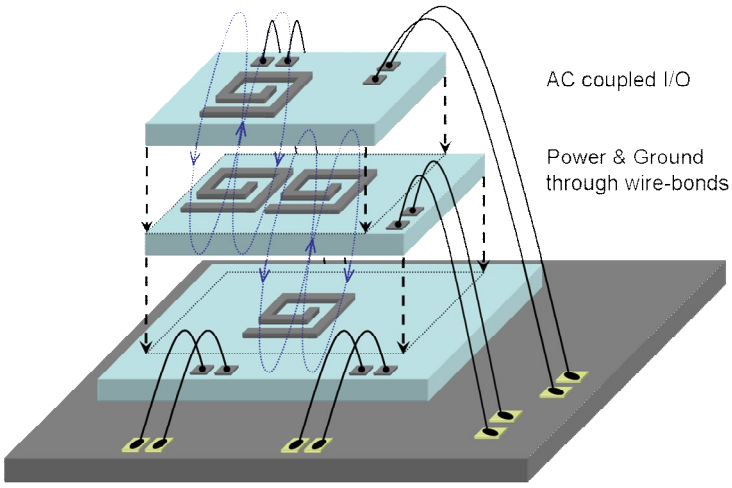


Figure 4.14. A combination of LCI interfaces and wire-bonding DC connections

This section presents a new power delivery scheme for inductive coupling 3D-ICs, which enables multiple dies with the same dimensions to be stacked, without blocking the ability of internal dies to power and ground connections. A combination of LCI and edge DC

connections is shown in Figure 4.15. It is accomplished by placing array of vias and metal layers on each die at opposite edges for inter-chip power/ground connections; these dies are polished or etched to expose the on-chip power/ground vias and metal layers; and vertical DC connections can be introduced by applying conductive epoxy or solder onto exposed and aligned power/ground conductors. These edge DC connections provide large external connecting points for power and ground as well as thermal paths.

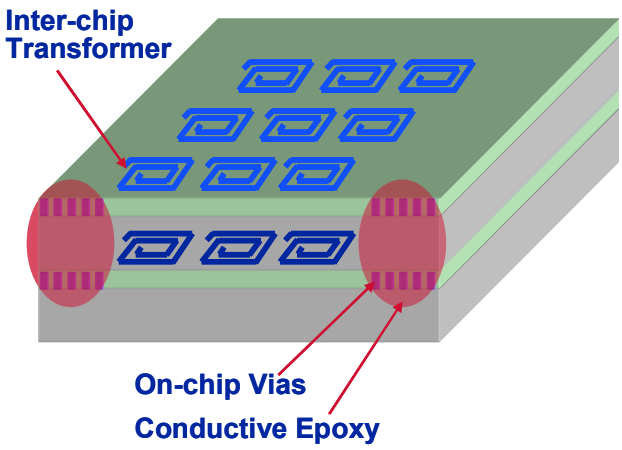


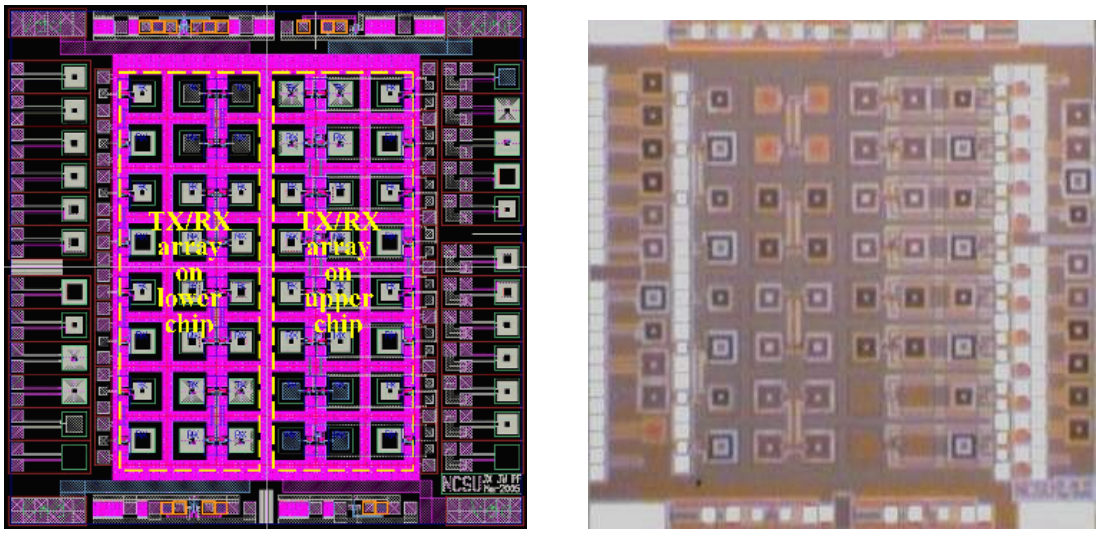
Figure 4.15. A combination of LCI interfaces and edge DC connections

This method, a combination of LCI AC connections and edge DC connections, has the advantage of not requiring processing to construct through-wafer vias for power/ground delivery and data/clock transmission between chips in a 3D chip stack. Since the power and ground connections are on the periphery of the chip, only coarse attachment for power/ground at the edge of the die stack is necessary. The top chip in the stack can be designed with a solder bump array to provide I/O to the assembled 3D-ICs. Chips in the stack can be built in different technologies, and then assembled together through this method. Because a regular low resistive wafer substrate can not avoid bypass current between power

and ground connections. To build multiple vertical DC connections with isolation, a high resistivity substrate for chip fabrication is required, and a SOI process is preferred.

4.4.2. Transceiver Test Chip

A test chip, shown in Figure 4.16, was fabricated by MIT Lincoln Lab in 0.18μm fully-depleted SOI technology. The layout of the test chip occupies 3.1x3.1mm^2 and includes a 3x6 TX-inductor array and a 3x6 RX-inductor array for demonstrating the inductively coupled vertical inter-chip communications. The coupling inductors vary in dimensions from 100μm to 150μm. The layout also includes some passive test structures for characterizing inter-chip transformers.



(a) Layout (b) Micrographic

Figure 4.16. Layout and micrographic of a 0.18μm fully-depleted SOI test chip for LCI

4.4.3. Transceiver Circuit Design

An asynchronous LCI transceiver system is shown in Figure 4.17, which has similar structures as shown in Figure 4.4. The TX converts NRZ signals into current signals; through magnetic coupling, current swings in the primary inductor induce current pulses in the secondary inductor; and the RX senses current pulses and converts them into voltage pulses, the voltage pulses are amplified and latched to restore NRZ signals.

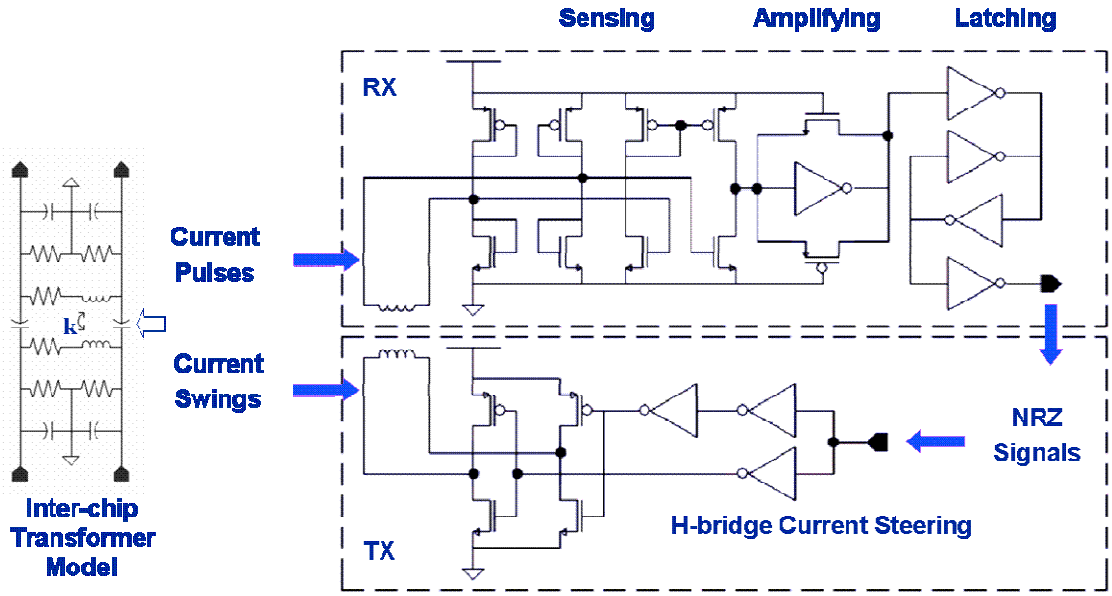


Figure 4.17. An asynchronous LCI transceiver circuit in 3D-ICs

In simulation, at data rate of 4Gb/s, an asynchronous transceiver circuit consumes 6.3mW power, in which the driver and receiver consume 3.6mW and 2.7mW, respectively. Figure 4.18 shows an eye-diagram at the RX output for LCI with edge DC connections. A test vehicle was designed for demonstrating a face-to-back two-chip stack with combinations of 3x6 LCI AC connections and 2 pairs edge DC connections.

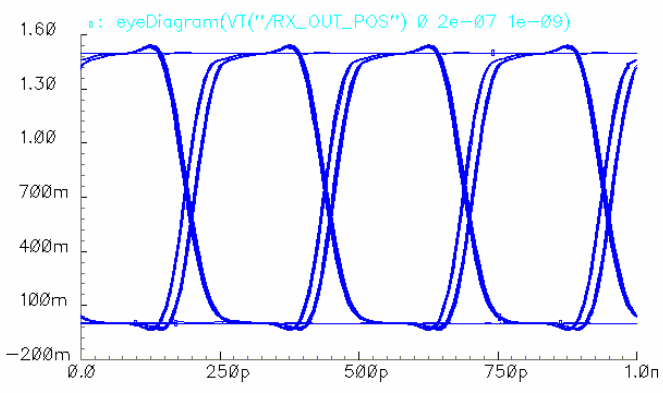


Figure 4.18. Simulated eye-diagram at RX output for LCI with edge DC connections

4.5. LCI in Multi-Chip Three-dimensional ICs

4.5.1. Physical Structure

For multi-chip 3D-ICs with through-wafer vertical vias technology, the yield for 3D-ICs is strongly depends on the process of vertical vias. By combining ACCI and 3D vertical vias, the overall 3D-ICs yield can be increased. The combination of ACCI and 3D vias is shown in Figure 4.19. LCI can be used for signaling between far-neighboring dies; CCI can be used for signaling between close-neighboring dies. Redundant DC vertical vias can tolerant process failures.

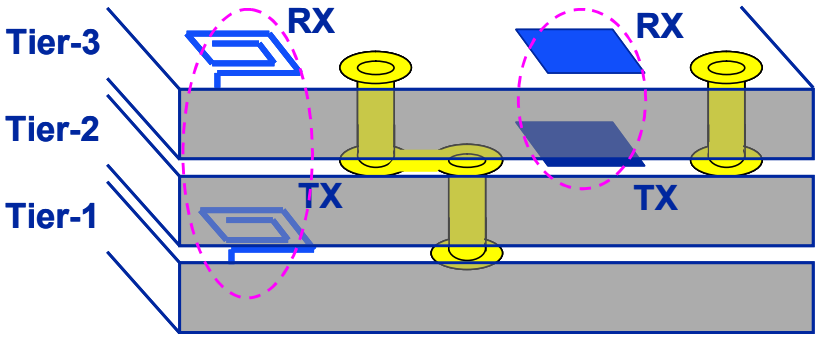


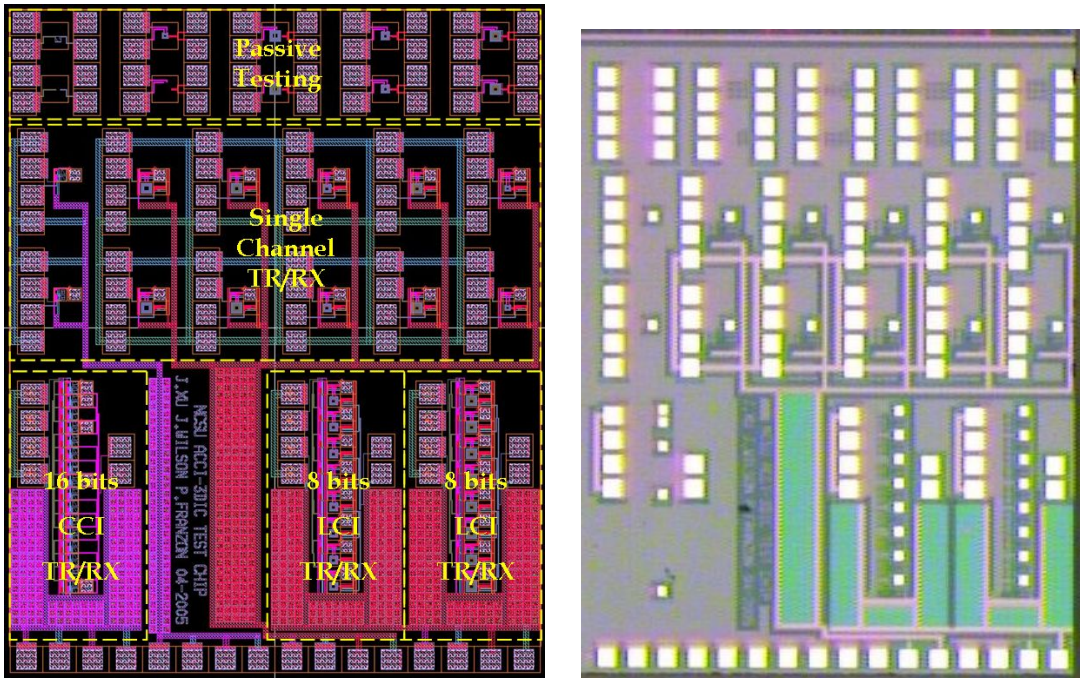
Figure 4.19. Combinations for ACCI interfaces and 3D vias

4.5.2. Transceiver Test Chip

A 3-layer 2.0X2.5 mm^2 3D-ICs test chip was fabricated at MIT Lincoln Lab with 0.18μm Fully-Depleted SOI 3-D integration process that is described in Appendix B. The layout of this test chip, shown in Figure 4.20, includes two 8-bit parallel inductive coupling transceiver arrays for demonstrating inter-chip communications between far neighboring chips. The coupling inductors vary in dimensions from 20μm to 40μm. In simulation, a synchronized inductive coupling transceiver circuit operated at 2.5Gb/s data rate.

The layout also included a 16-bit parallel capacitive coupling transceiver array for demonstrating inter-chip communications between close neighboring chips. Each capacitive coupling channel includes two 20μmX20μm plates in differential. In simulation at 2.5Gb/s data rate, a synchronized capacitive coupling transceiver circuit consumes 0.7mW power, in which transmitter and receiver consumes 0.2mW and 0.5mW respectively.

Moreover, the layout also includes some single-channel transceiver and some passive test structures for channel characterization.



(a) Layout (b) Micrographic

Figure 4.20. Layout and micrographic of a 3D-ICs test chip for ACCI

4.5.3. Transceiver Circuit Design

LCI or CCI transceiver circuits presented in previous chapters have asynchronous structures, which do not require a clock signal to sample the pulses. However, in practice a digital signaling system usually requires synchronization. A receiver circuit based on sense amplify flip-flop structure was proposed to sample the received pulse signals. A schematic of synchronized transceiver circuit is shown in Figure 4.21.

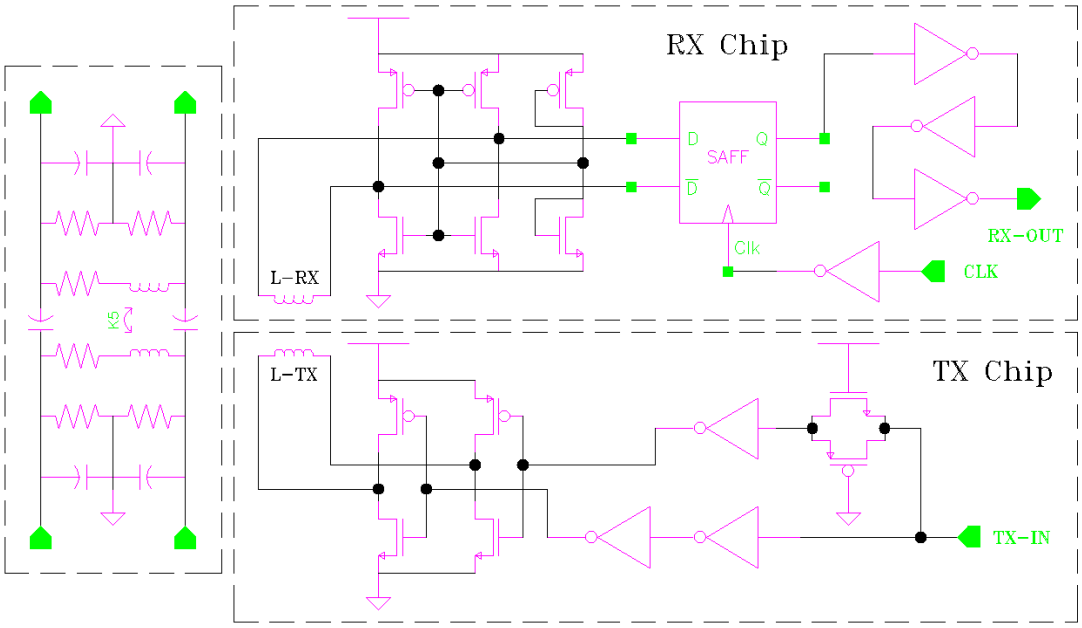


Figure 4.21. An synchronized LCI transceiver circuit

4.5.4. Transceiver Measurement Results

A test structure for 8 channels LCI in multi-tier 3D-ICs is depicted in Figure 4.22, where TX and RX are placed on tier 1 and tier 3, respectively. The primary inductor has a 30μm diameter and 3.3nH inductance; the secondary inductor has a 40μm diameter and 3.5nH inductance; two inductors has a 10μm separation and 0.4nH mutual inductance. Power and ground connections are through bonding wires; input/output signals connections such as data and clock are through micro-probes.

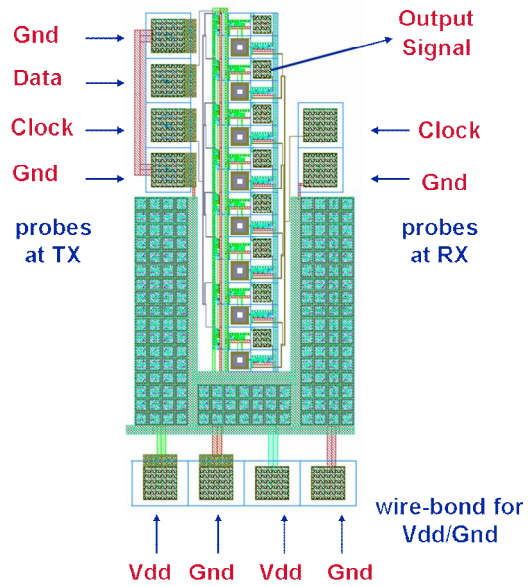


Figure 4.22. Test structure for LCI in multi-tier 3D-ICs

In measurement, at data rate of 1.25Gb/s, each synchronous transceiver circuit consumed 3.5mW power, where TX and RX consumed 2.4mW and 1.1mW, respectively. Figure 4.23 shows an eye-diagram at RX output for a synchronized LCI transceiver system.

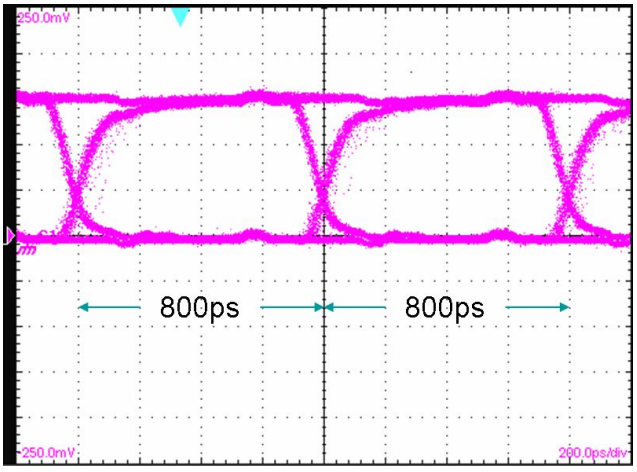


Figure 4.23. Eye-diagram at RX output for a synchronized LCI transceiver

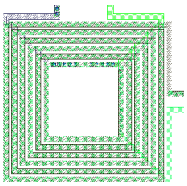
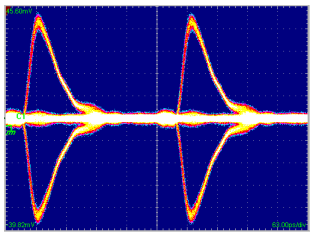
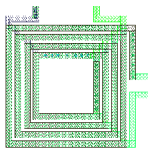
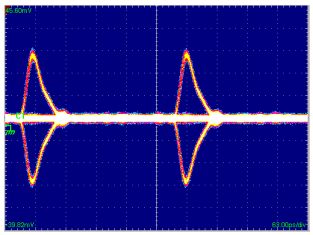
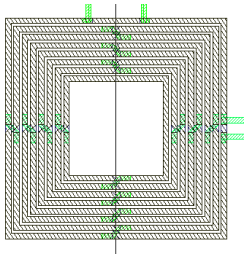
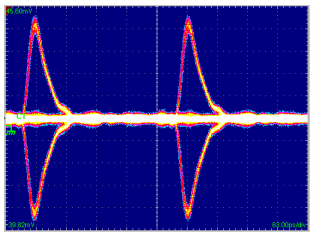
4.5.5. Transformer Measurement Results

In a 3D-ICs test chip fabricated using fully-depleted SOI technology, for inter-tier transformers with various spiral inductor size and structure, inductive coupling pulses are illustrated in Table 4.2. For two transformers with similar spiral structure, e.g. in case 1 and case 2, the amplitude of pulses are strongly depends on the magnetic coupling coefficient *k* instead of self-inductance. For two transformers with different spiral structures, e.g. in case 1 and case 3, the amplitude of coupling pulses depends on the spiral structures, which affect all parameters such as self-inductance, winding resistance, and coupling coefficient. In terms of area, a transformer with double-layer spiral inductor has a higher efficiency to induce the same pulse than a transformer with single-layer spiral inductor.

Table 4.2 shows coupling pulses for asymmetric transformers where primary inductor and secondary are in different sizes. In case 1 and case 2, the inner diameter of a balanced single-layer inductor approximately equals the outer diameter of another balanced single-layer inductor; and the capacitive coupling between two spiral windings are ignorable. The coupling pulses in these two cases are very similar regardless the excitation source is added at the bigger inductor or at the smaller inductor. In case 3 and case 4, a bigger un-balanced double-layer inductor is placed on top of a smaller un-balanced double-layer inductor. The coupling pulses in case 4, where the primary inductor is bigger than the secondary inductor, are larger than the coupling pulses in case 3, where the primary inductor is smaller than the secondary inductor. As magnetic flux in a double-layer inductor is concentrated in the center of the spiral. If an excitation source is added onto a bigger primary inductor, the smaller secondary inductor is exposed to the concentrated flux and to induce large pulses. In contrast,

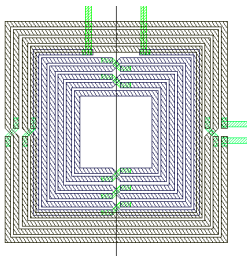
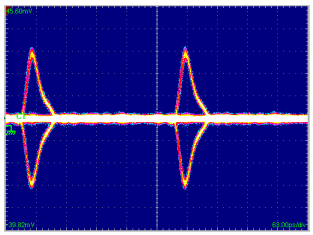
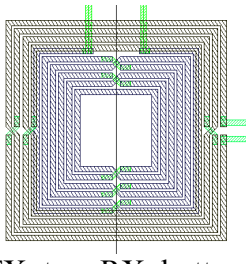
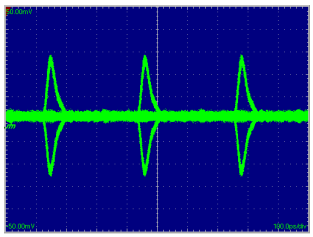
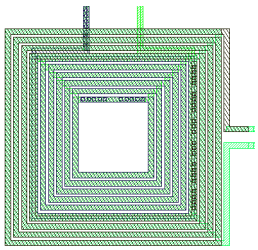
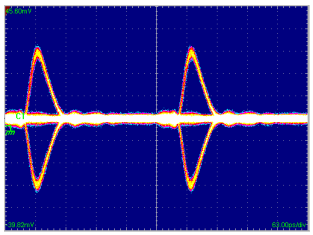
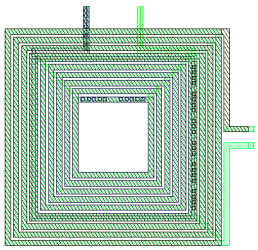
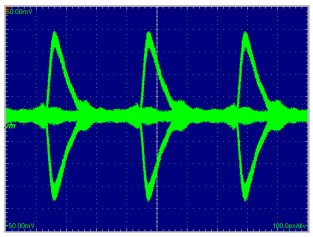
if an excitation source is added onto a smaller primary inductor, the bigger secondary spiral inductor is exposed to a partial of the flux and to induce small pulses.

Table 4.2. Coupling pulses for various transformers

1	*Spiral 1 (bottom)*	*Spiral 2 (top)*	*Transformer (inter-tier)*	*Layout*	*Pulses at RX (3.125Gb/s, 1V, at TX)*
	double-layer square	double-layer square	separation in oxide	 TX: bottom, RX: top	 peak-peak: 79mV
	d: 30um w: 1um s: 0.5um turns: 6	d: 30um w: 1um s: 0.5um turns: 6	g: 10.9um		
	L: 3.3nH R: 103ohm	L: 3.3nH R: 103ohm	k: 0.124 M: 0.41nH		
2	*Spiral 1 (bottom)*	*Spiral 2 (top)*	*Transformer (inter-tier)*	*Layout*	*Pulses at RX (3.125Gb/s, 1V, at TX)*
	double-layer square	double-layer square	separation in oxide	 TX: bottom, RX: top	 peak-peak: 50mV
	d: 20um w: 1um s: 0.5um turns: 4	d: 20um w: 1um s: 0.5um turns: 4	g: 10.9um		
	L: 0.9nH R: 46ohm	L: 0.9nH R: 46ohm	k: 0.078 M: 0.07nH		
3	*Spiral 1 (bottom)*	*Spiral 2 (top)*	*Transformer (inter-tier)*	*Layout*	*Pulses at RX (3.125Gb/s, 1V, at TX)*
	single-layer symmetric	single-layer symmetric	separation in oxide	 TX: bottom, RX: top	 peak-peak: 75mV
	d: 40um w: 1um s: 0.5um turns: 8	d: 40um w: 1um s: 0.5um turns: 8	g: 10.9um		
	L: 2.4nH R: 74ohm	L: 2.4nH R: 74ohm	k: 0.167 M: 0.40nH		

"d", "w", "s" and "g" represents spiral diameter, line width, line spacing and winding separation, respectively.

Table 4.3. Coupling pulses for asymmetric transformer

	Spiral 1 (bottom)	*Spiral 2 (top)*	*Transformer (inter-tier)*	*Layout*	*Pulses at RX (3.125Gb/s, 1V, at TX)*
1	single-layer symmetric	single-layer symmetric	separation in oxide	 TX: bottom, RX: top	 peak-peak: 51mV
	d: 30um w: 1um s: 0.5um turns: 6	d: 40um w: 1um s: 0.5um turns: 4	g: 10.9um		
	L: 1.0nH R: 42ohm	L: 1.0nH R: 66ohm	k: 0.100 M: 0.10nH		
2	single-layer symmetric	single-layer symmetric	separation in oxide	 TX: top, RX: bottom	 peak-peak: 50mV
	d: 30um w: 1um s: 0.5um turns: 6	d: 40um w: 1um s: 0.5um turns: 4	g: 10.9um		
	L: 1.0nH R: 42ohm	L: 1.0nH R: 66ohm	k: 0.100 M: 0.10nH		
3	double-layer square	double-layer square	separation in oxide	 TX: bottom, RX: top	 peak-peak: 53mV
	d: 30um w: 1um s: 0.5um turns: 6	d: 40um w: 1um s: 0.5um turns: 4	g: 10.9um		
	L: 3.3nH R: 103ohm	L: 3.5nH R: 110ohm	k: 0.115 M: 0.39nH		
4	double-layer square	double-layer square	separation in oxide	 TX: top, RX: bottom	 peak-peak: 71mV
	d: 30um w: 1um s: 0.5um turns: 6	d: 40um w: 1um s: 0.5um turns: 4	g: 10.9um		
	L: 3.3nH R: 103ohm	L: 3.5nH R: 110ohm	k: 0.115 M: 0.39nH		

Chapter 5. Inductively Coupled Interconnect (LCI) in Chip-to-Chip Communications

5.1. Overview

This chapter explores the LCI scheme at package-to-board socket and board-to-board connector interfaces to improve I/O pin density. Two MCM, which include transceiver chips and spiral inductors, are overlapped at edges to demonstrate the chip-to-chip communications over LCI interfaces. The extraction for equivalent circuits of interface transformers and the characterization for LCI channels are described. A novel synchronization circuit for LCI transceiver is also presented. Simulation results indicate that a LCI transceiver system communicated PRBS data at 2.0Gb/s via 400x400 μm^2 spiral inductor pair.

5.2. LCI Potential Applications in Chip-to-Chip Communications

LCI for vertical connections in 3D-ICs has been addressed in the previous chapter. LCI can provide unique non-contacting signal channels and tolerate a large separation and misalignment between coupled spiral inductors. It has potential applications in high-speed chip-to-chip communications to replace conventional contacting interfaces such as chip-to-package interfaces, package-to-board socket interfaces and board-to-board connector interfaces. It is also proposed to apply LCI at cube-to-cube lateral interfaces in 3D-ICs.

5.2.1. LCI at Package-Board Socket Interfaces

A package-board socket or adapter is used to mount a chip package onto a PCB with more flexibility. A typical pin pitch in a ball grid array (BGA) or land grid array (LGA) package is 0.5~1.27mm. Packaging manufacturers are working to reduce the pin pitch and cost, and improve signaling performance and reliability. For high-speed signal pins, LCI can take places of BGA bumps or LGA springs at package-board socket interfaces. A scheme for LCI at package-board socket interfaces is shown in Figure 5.1.

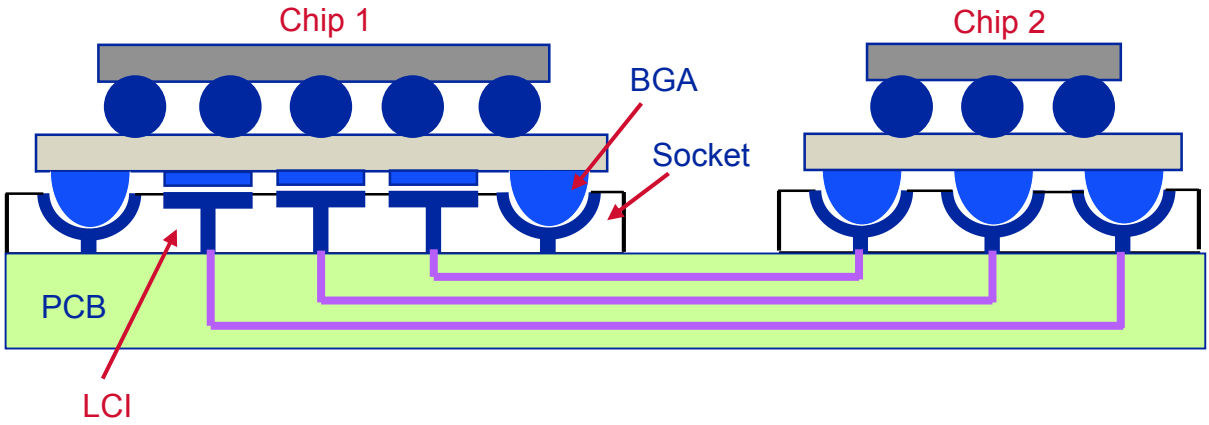


Figure 5.1. Scheme for LCI at package-board socket interfaces

Chip 1 has a large I/O pin count and requires a high density package, where signal connections use LCI and power/ground connections use regular BGA/LGA socket. Chip 2 has a small I/O pin count and only need a low density I/O package, where all signal and power/ground connections use regular BGA/LGA sockets. The research goal for applying

LCI in socket interfaces is to develop a new non-contacting I/O scheme and achieve less than 0.5mm pin pitch and 2+Gb/s data rate.

5.2.2. LCI at Board-Board Connector Interfaces

For board-to-board edge connections, e.g. a PCI-express slot on a motherboard for daughter-card insertion, perpendicular connectors are usually used. A typical pin pitch in connector is in a range of 0.4~2.0mm. Connector vendors are working to improve pin bandwidth and density, and reduce manufacture cost as well. For high-speed signal I/O, the conventional connector pin can be replaced by LCI. A scheme for LCI at board-to-board connector interfaces is shown in Figure 5.2.

For instance, chip 1 is a graphics processing unit (GPU) chip, which is on a daughter-card, and chip 2 is a north bridge (NB) chip which is on the motherboard. The signal pins are using LCI and the power/ground pins are using regular connectors. The non-contacting LCI interfaces does not require any insertion force to ensure the contacting and could be feasible using zero-insertion-force (ZIF) connectors. At LCI connector interfaces, the signal paths are inductively coupled but the return paths for TX and RX could be isolated; the ground pins could be much less than signal pins and still maintain good signal integrity. A research goal for applying LCI at connector interfaces is to achieve non-contacting I/O with pitch less than 0.5mm and bandwidth faster than 2Gb/s.

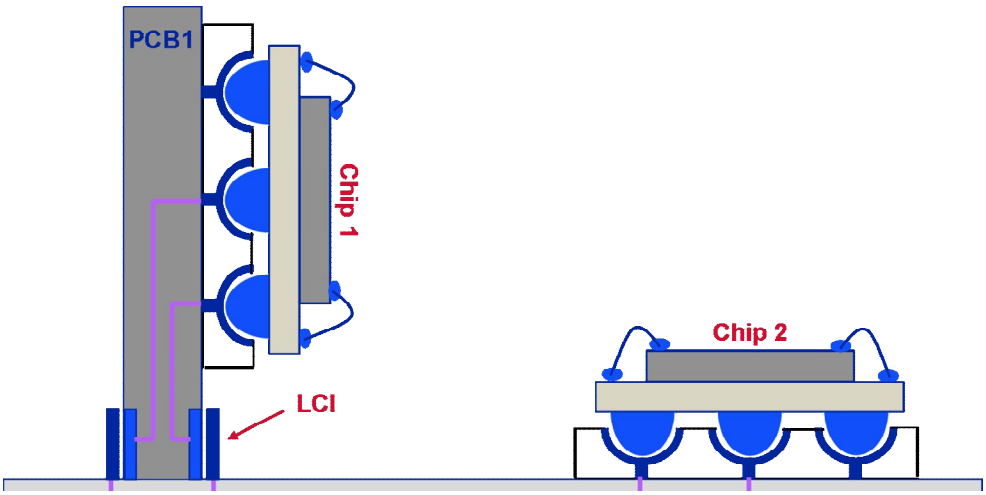


Figure 5.2. Scheme for LCI at board-board connector interfaces

5.2.3. LCI at 3D-ICs Cube-to-Cube Interfaces

For a massively stacked 3D-ICs system, where multiple 3D-ICs cubes are integrated onto a common substrate such as a BGA carrier, there are I/O demands for cube-to-cube lateral communications. Because direct contacting lateral connections between cubes are difficult to build, a conventional lateral signal path includes vertical connections in TX cube, interfaces for TX cube and the substrate, horizontal connections on the substrate, interfaces for RX cube and the substrate, and vertical connections in RX cube. The multiple interconnection stages for a conventional lateral signal path will limit signaling speed and cost a large amount of routing area. LCI may provide non-contacting signal paths for high-speed lateral communications between neighboring chip-cubes.

A scheme for LCI at 3D-ICs cube-to-cube interfaces is shown in Figure 5.1, where spiral inductors are created on the sidewall of chip stacks and two aligned spiral inductors on

neighboring cubes couple to form a transformer. The main advantage of this scheme is it provides a feasible high-speed lateral I/O without much mechanical complexity.

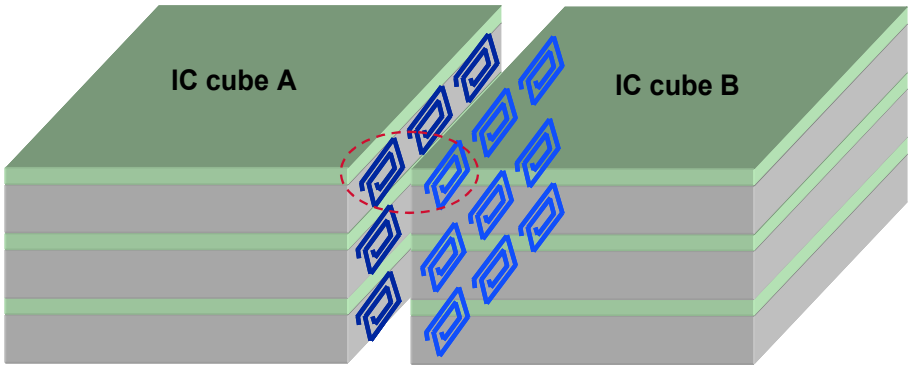


Figure 5.3. Scheme for LCI at 3D-ICs cube-to-cube interfaces

5.3. Channel Characterization for LCI Chip-to-Chip Communications

5.3.1. LCI Transceiver System for Chip-to-Chip Communications

A differential LCI transceiver system for chip-to-chip communication is shown in Figure 5.4. It includes a driver (TX) circuit, a receiver (RX) circuit, two spiral inductors that are placed at the package-board or board-board interfaces to form an interfacing transformer, and two differential transmission lines or stubs that connect driver/receiver to the coupling inductors.

Figure 5.4. A transceiver system for LCI chip-to-chip communications

5.3.2. Transformer Analysis

A conventional "T" model for transformer is shown in Figure 5.5, where M represents the mutual inductance ($M = k * \sqrt{L_1 * L_2}$), L_1-M and L_2-M represent leakage inductances, R_1 and R_2 represents winding resistances, R_S and R_O represents source and load resistances, respectively.

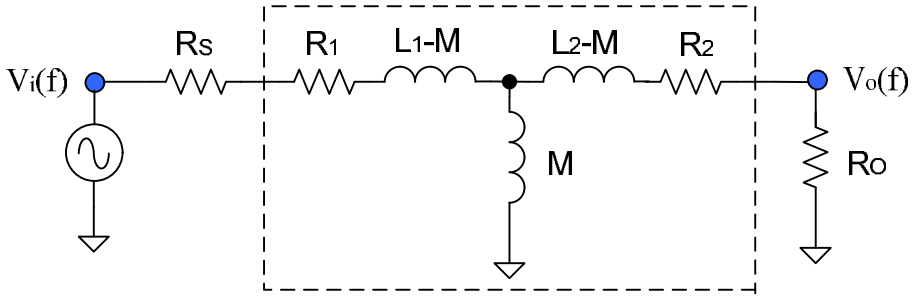


Figure 5.5. A "T" model for transformer analysis

Assume the two inductors are identical, then $L_1=L_2=L$, $R_1=R_2=R$, a transfer function of transformer in frequency domain, $G(f)=Vo(f)/Vi(f)$, can be expressed as:

$$G(f) := 2\,Ro\,\pi f k L \Big/ \left(\left(Rs + R + 2\,\pi f (L - k L) + \frac{2\,(2\,\pi f (L - k L) + R + Ro)\,\pi f k L}{2\,\pi f (L - k L) + R + Ro + 2\,\pi f k L} \right) (2\,\pi f (L - k L) + R + Ro + 2\,\pi f k L) \right)$$

For instance, $L_1=L_2=1$nH, $R_1=R_2=1\Omega$, Rs=Ro= 50Ω, the dependence of frequency response on the coupling coefficient k is shown in Figure 5.6. A large k, which means tight

coupling, results in a larger signal transferring and wider bandwidth. In an ideal case, k=1, there would be no leakage inductance but only mutual inductance, the transformer presents a high-pass filter. In the LCI system, *k* is usually less than 0.8, which introduce significant leakage inductances. The leakage inductance presents low-pass characteristic and limits the bandwidth of transformer.

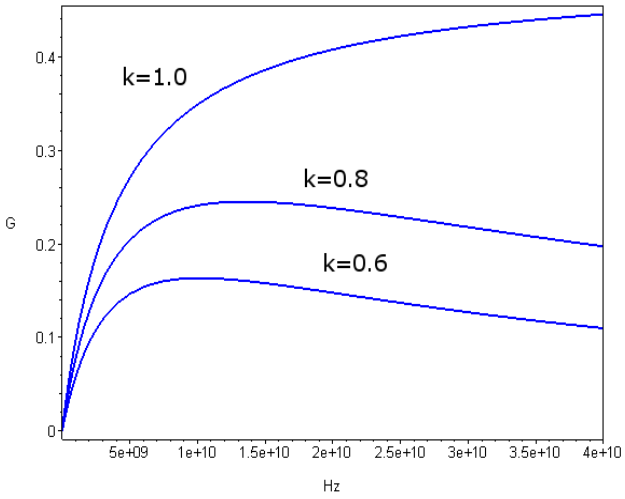


Figure 5.6. Frequency responses for various coupling coefficient

Given k=0.8, R_1=R_2=1Ω, Rs=Ro=50Ω, the dependence of frequency response on the self-inductance *L* is shown in Figure 5.7. A large *L* results in a larger mutual inductance and a lower high-pass corner frequency. However, a larger *L* also introduces larger leakage inductances and a lower low-pass corner frequency. Its bandwidth is narrower and it can pass more low-frequency components that may introduce inter-symbol-interference (ISI) in signaling. There is an optimized inductance range for pulse mode signaling, e.g. 2~5nH, to match LCI channel characteristic to the RZ pulse spectrum.

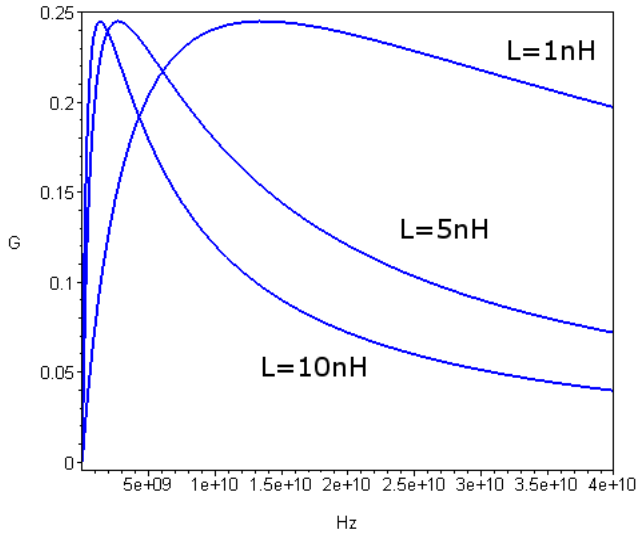


Figure 5.7. Frequency responses for various self-inductances

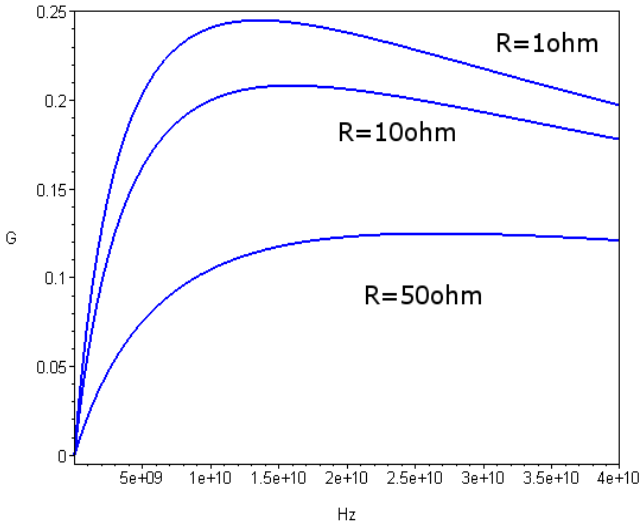


Figure 5.8. Frequency responses for various DC resistances

It is observed that the performance of the transformer also depends on its DC winding resistance. For k=0.8, L_1=L_2=1nH, Rs=Ro=50Ω, the frequency response dependence on *R* is shown in Figure 5.8. An on-chip spiral inductor has a large *R* due to the narrow metal width and thin metal thickness. It introduces a larger internal voltage drop and an increased high-

pass corner frequency. An in-package or on-board spiral inductor has a lower *R* due to its wider and thicker metal winding. It results in more energy transfer and passes more of the low-frequency spectrum. However, a low DC resistance will cause problems with the impedance matching and reflection elimination.

5.3.3. Inductor and Transformer Modeling

Figure 5.9 shows a spiral inductor on a MCM substrate. It has 400μm in size, 3 turns, 25μm line width and 25μm line spacing. These two spiral inductors with 25μm air-gap separation couple to form an interface transformer.

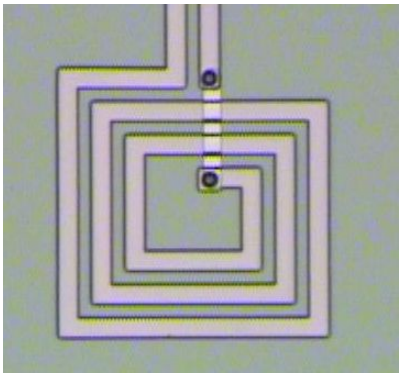


Figure 5.9. Micrographic of a spiral inductor on a MCM substrate

Figure 5.10 shows a 3D view for that interface transformer in an electromagnetic (E-M) field solver, e.g. Ansoft/Q3D [61]. Layouts of spiral inductors were drawn in Cadence/Virtuoso and then imported into Ansoft/Q3D. By customizing the process parameters such as dielectric layer thickness and metal layer height, Q3D can build 3D structure from Cadence 2D layout and run finite element mesh analysis.

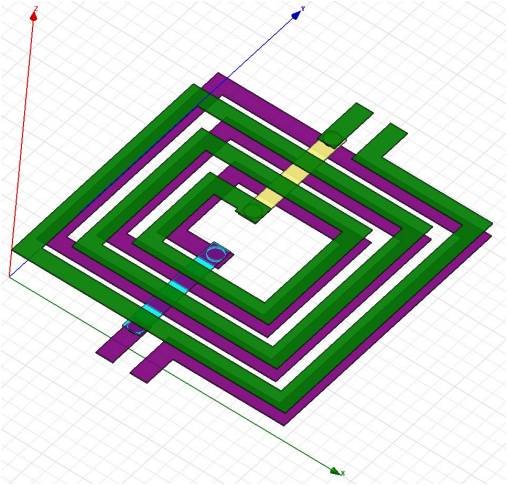


Figure 5.10. An interface transformer in a 3D E-M field solver

Equivalent circuits for spiral inductors and interface transformers can be extracted by using Ansoft/Q3D extractor, which provides an E-M based synthesis solution for passive elements. Figure 5.11 shows an extracted equivalent circuit for the interface transformer depicted in Figure 5.10. This model is a Q3D ladder model, which includes two identical serial blocks and one parallel block. Each serial block includes two self-inductances, two parasitic resistances and a mutual inductance. The parallel block includes two shunt parasitic capacitances of inductor windings and a crossover capacitance between windings. Additional details on inductor and transformer modeling are described in Appendix E.

Compared to the ASITIC transformer model, which was discussed in the previous chapter, the Q3D ladder-type model includes two identical half circuits and has less intuitive meaning than the ASITIC model does. However, the ASITIC model is based on linear Green's functions for Maxwell's E-M equations, and it can fit narrow-band applications such as RF communications. Q3D model is based on finite-element methods and S-parameter

responses, and it can fit wide-band applications such as LCI chip-to-chip data communications, as well as narrow band applications.

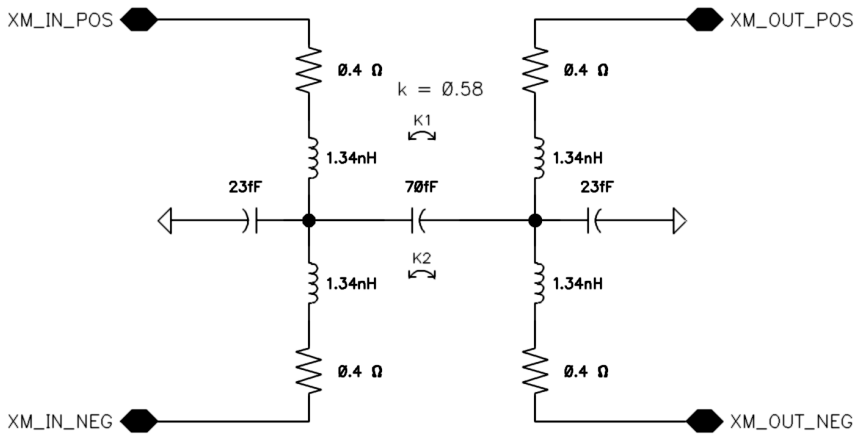
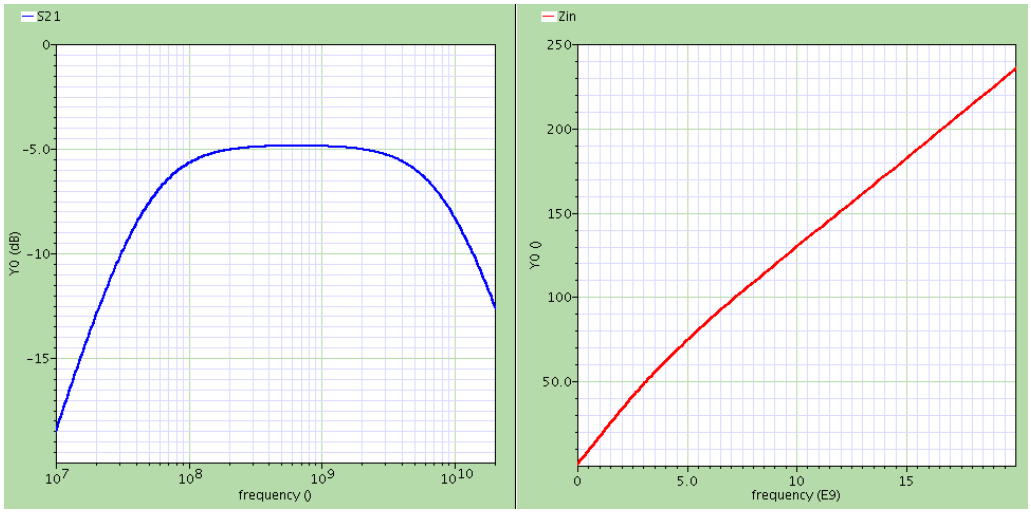


Figure 5.11. An equivalent circuit for an interface transformer

Differential AC analysis for such a transformer was performed, and its frequency response is shown in the left side of Figure 5.12, which has a band-pass characteristic. The mutual inductance ($M = k * \sqrt{L_1 * L_2}$) and self-resistances define a high-pass corner frequency; leakage inductances (L_1-M and L_2-M) and self-resistances define a low-pass corner frequency. For a transformer with large self-inductances and a large mutual inductance, its high-pass corner frequency is very low and it could support NRZ signaling. For a transformer with large parasitic resistance, e.g. an on-chip spiral inductors with narrow line and many turns, its high-pass corner frequency will be high. It blocks a lot of low-frequency components of NRZ spectrum and is suitable for pulse signaling. For a tightly coupled transformer, i.e. its coupling coefficient k is close to 1, there will be tiny leakage inductance and the transformer presents a high-pass characteristic. In LCI practice, there are some separation between spiral inductors and k is in a 0.5~0.8 range, which results in a

limitation for the higher band. The input impedance of a transformer shown in the right side of Figure 5.12 is approximately proportional to frequency. e.g. this transformer presents a 50Ω input impedance at 3GHz.



(a) Frequency response (b) Input impedance

Figure 5.12. Frequency response and input impedance of an interface transformer

A work flow for inductor or transformer design and modeling is showing in Figure 5.13. ASITIC is used to design spiral inductor geometrics, estimate inductance and export inductor layout in "cif" format. Cadence/Virtuoso is used to import inductor layout, then modify it to be a transformer layout and export the transformer layout in "cif" format. By using a Perl script and referring to a customized technology file, the transformer layout are imported into Ansoft/Q3D and converted to be 3D transformer structures. After running simulations for E-M field solver, an equivalent circuit model can be extracted in "netlist" format. That netlist can be included directly as a sub-circuit or represented by a RLC schematic block.

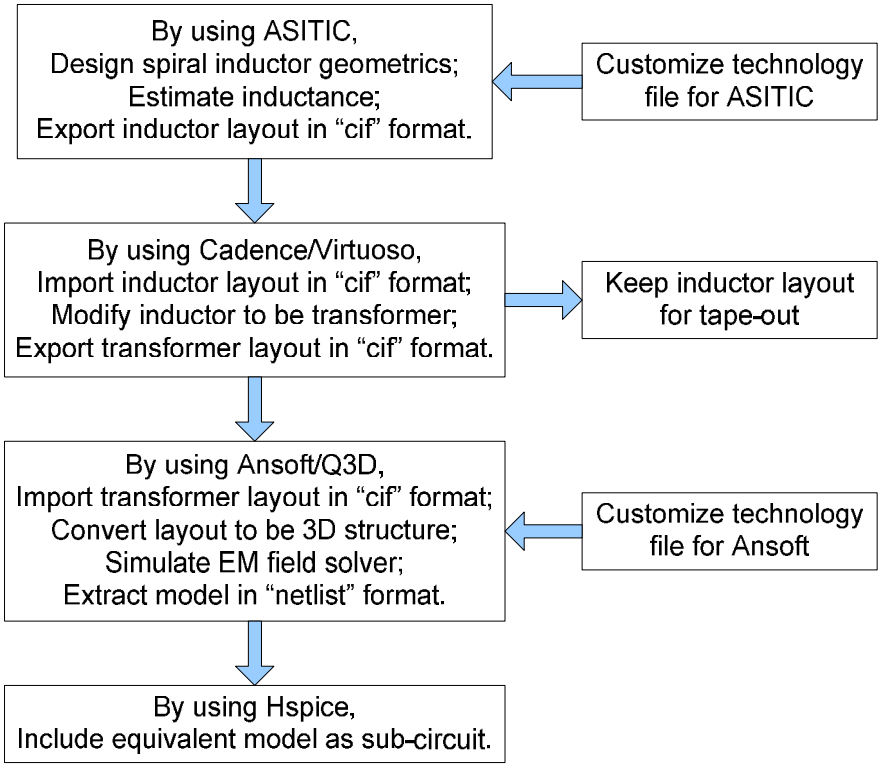


Figure 5.13. Work flows for inductor/transformer design and modeling

5.3.4. Transmission Line Modeling

Lossy transmission lines on PCB or stubs in package can be modeled by using "W-element" in Hspice that is described in Appendix D. A cross section for two coupled micro-strip lines is shown in Figure 5.14, where "H" represents the dielectric layer thickness, "W", "S" and "T" represents the metal trace width, spacing and thickness, respectively. For instance, two copper stubs which have 25μm "W", 25μm "S" and 1.8μm "T" are placed on top of a Benzocyclobutene (BCB) layer which has 11μm "H" and 2.65 in dielectric permittivity. Calculated by using a transmission line calculator [60], these two coupled

micro-strip lines have 50ohm odd mode characteristic impedances Z_{odd} and 52ohm even mode characteristic impedances Z_{even}. "W-element" RLGC parameters in unit length were generated by using Hspice 2-D field solver [62] and are shown in Table 5.1, which is a 6x3 matrix and includes self and mutual parameters for resistance, inductance, conductance, capacitance, skin effect and dielectric loss.

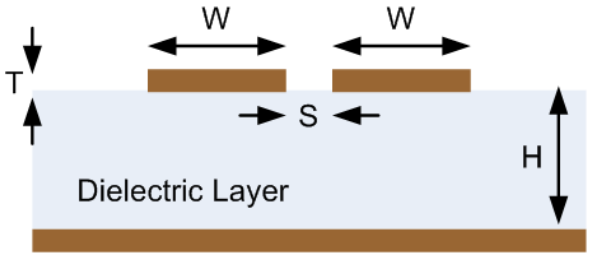


Figure 5.14. A cross-section of two coupled micro-strip lines

Table 5.1. W-element model for a pair of coupled transmission lines

Unit parameters		Self (line 1)	Mutual	Self (line 2)
DC inductance	Lo (H/m)	2.773078e-07	2.641844e-08	2.773078e-07
DC capacitance	Co (F/m)	9.431704e-11	-6.103344e-12	9.431704e-11
DC resistance	Ro (Ω/m)	4.629627e+02	0.000000e+00	4.629627e+02
DC conductance	Go (S/m)	0.000000e+00	0.000000e+00	0.000000e+00
Skin effect resistance	Rs (Ω/m)	8.252813e-03	5.717809e-04	8.252813e-03
Dielectric loss conductance	Gd (S/m)	7.901486e-13	-5.113126e-14	7.901486e-13

5.3.5. Frequency Response for a LCI Transceiver System

AC analysis was performed for a LCI signaling channel, which includes a 2cm coupled micro-strip stub at TX, a differential transformer model shown in Figure 5.11 and another 2cm coupled micro-strip stub at RX. Frequency responses at the secondary side of transformer and the end of second T-line are shown in Figure 5.15. A lossy T-line or stub has a low-pass characteristic; however, a transformer has a band-pass characteristic. The combination of T-lines and a transformer also has a band-pass characteristic, where the high-pass corner (-3dB) frequency f_{hp} is defined by transformer and the low-pass (-3dB) corner frequency f_{lp} is mostly defined by T-line. In this example, the maximum response occurs at 7.25GHz, and its bandwidth between the two corner frequencies is 2.27~15.26GHz, which is suitable range for pulse signaling.

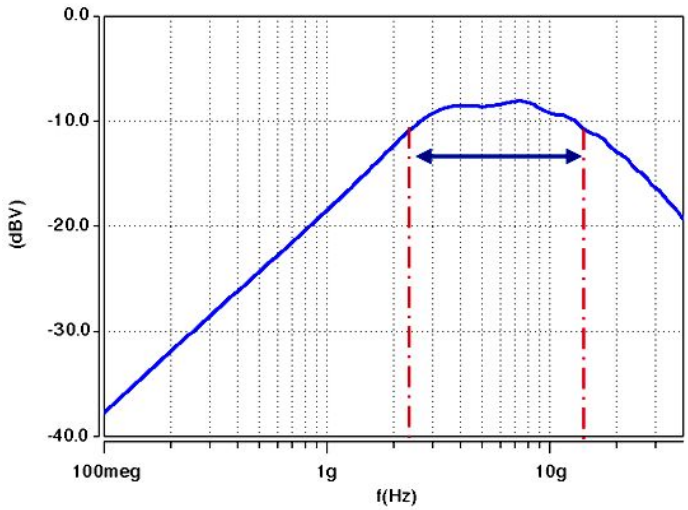


Figure 5.15. Frequency response for a LCI signaling channel

5.4. Pulse Signaling in LCI Chip-to-Chip Communications

5.4.1. LCI Transceiver System

A LCI transceiver system, shown in Figure 5.4, utilizes current-mode pulse signaling. Upon the input NRZ data, a differential drive (TX) circuit controls the directions of current swing in the primary inductor, and creates an alternating magnetic field that induces current pulses in the secondary inductor. A differential receiver (RX) circuit converts the current pulses into voltage pulses, then amplifies these voltage pulses and latches them to binary digital signals. Two coupled inductors form an interface transformer that provides passive equalization to reduce the inter-symbol interference (ISI).

5.4.2. LCI Transmitter Circuit

A drive circuit in LCI inter-chip communication is shown in Figure 5.16. A single-ended digital signal is converted into two complementary signals by using an inverter and a transmission-gate (T-gate). By adjusting the ratio of size for the inverter and the T-gate, skews between two complementary signals are reduced and they can be treated as a pair of differential signals. The differential signals switch two output NMOS transistors and steer the direction of current in the T-line and the primary inductor. On-chip termination resistors are included at the TX output to match the impendence of the T-line and reduce reflections.

The last stage of TX is a source follower circuit, which has low output impedance and is suitable to drive a 50ohm transmission line or stub. An expression for the turn-on

resistance of output NMOS is $R_{on} = \frac{1}{g_m + g_{mb}}$, where $g_m = \frac{\partial I_D}{\partial V_{GS}}$ represents the trans-conductance of FET and $g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$ represents the substrate trans-conductance. In the output stage of TX circuit shown in Figure 5.16, a 6μm NMOS in TSMC-0.25μm technology has a turn-on resistance 286Ω. When placing in parallel with a 60Ω termination resistance, the output impedance of the source follower stage is around 50Ω which matches the characteristic impedance of T-line.

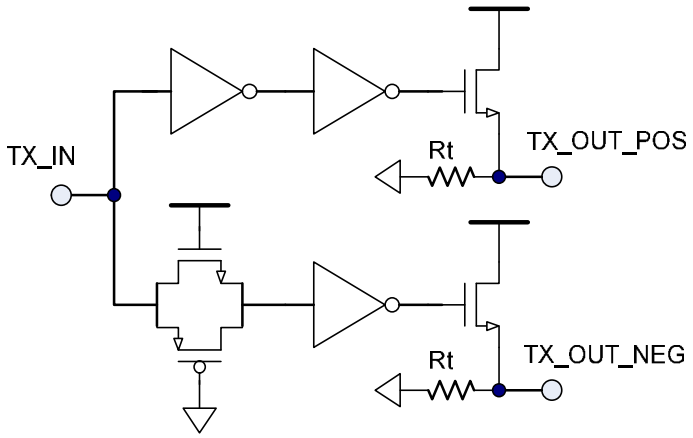
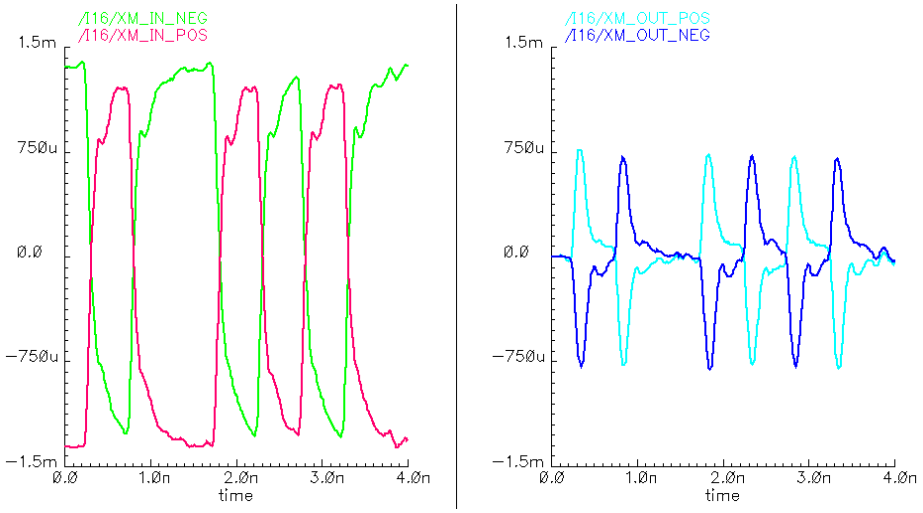


Figure 5.16. A transmitter circuit in LCI chip-to-chip communications

5.4.3. LCI Coupling Interface

At a LCI transformer coupling interface, bipolar current swings excite an alternating magnetic field at the primary side of transformer and then induce current pulses at the secondary side of transformer. Figure 5.17 shows currents waveform in both sides of a transformer described in previous sections. If the winding configurations in a transformer are

in-phase, a positive pulse in the right side figure represents a current transition from negative to positive in the left side figure; a negative pulse represents a current transition from positive to negative. If no transition occurs at the primary spiral inductor, the output at the secondary spiral inductor would be “zero”. This transformer has small values for self-inductance (e.g. 2.68nH and loosely inductive coupling k=0.58). It has a band-pass characteristic and blocks most low-frequency components. That is the principal for pulse generation.



(a) Current swings in the primary inductor (b) Current pulses in the secondary inductor

Figure 5.17. Current waveform in a coupling transformer

5.4.4. LCI Receiver Circuit

As shown in Figure 5.18, a receiver circuit includes three stages: sensing, amplifying and sampling. On-chip termination resistors are placed at the RX input to match the impendence of the T-line and reduce reflections.

The RX sensing stage is based on a common gate trans-impedance amplifier, which has low input impedance, and converters the current pulses on the termination resistors into voltage pulses. The RX amplifying stage includes a pair of self-biasing, source-coupled amplifiers and a symmetric Chappell amplifier [4]. There are tradeoffs between bandwidth and gain in an amplifier design. To amplify pulse signals and keep pulse shapes, an amplifier with high bandwidth but low gain is desired. That amplifier-chain boosts the amplitude of voltage pulses with little distortions. To eliminate a DC wandering between two differential pulses, clamping transistors are also included at each amplifier output stage.

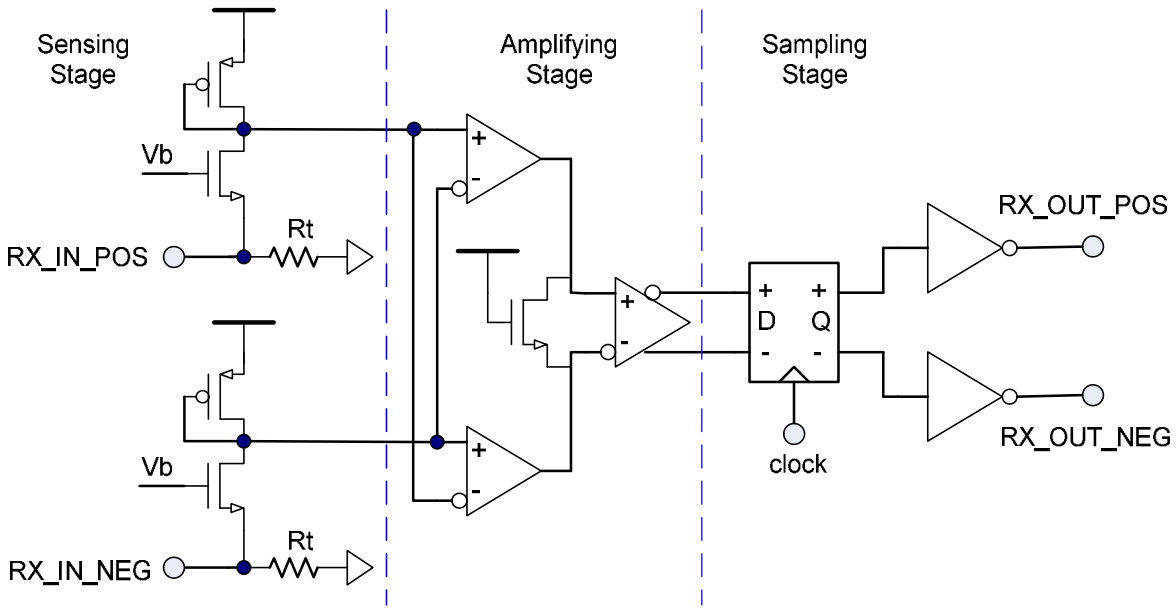
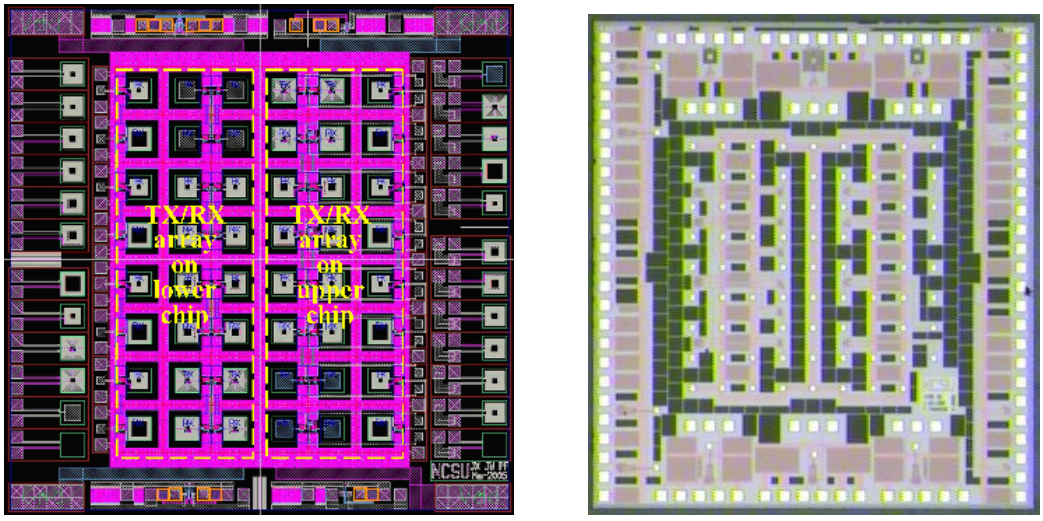


Figure 5.18. A receiver circuit in LCI chip-to-chip communications

The RX sampling stage is based on a differential edge-triggered flip-flop [4] (strong-ARM flip-flop), which has a very good sensitivity is suitable for low-swing signals detection. By combining a gate-isolated clocked sense amplifier and an R-S flip-flop, it converters the low-swing voltage pulses into binary digital signals.

5.4.5. LCI Transceiver Test Chip

Spiral inductors of various sizes and structures were placed on two alumina MCM substrates. Short differential micro-strip T-lines (stubs), e.g. 1~2cm, were also placed on the substrates to connect transceiver chips and inductors. A transceiver test chip including various driver/receiver circuits was designed and fabricated in TSMC 0.25-μm CMOS technology. Figure 5.19 shows a layout and a die-photo of the test chip, which has 2.8x3.1mm^2 in die size.



(a) Layout (b) Micrographic

Figure 5.19. Layout and micrographic of a TSMC-0.25μm test chip for LCI

Transceiver chips are mounted on the MCM substrates via flip-chip or wire-bond techniques. The two MCMs are stacked face-to-face or face-to-back and partially overlapped. The coupled inductors form transformers to emulate the LCI at the package-to-board socket,

board-to-board connector and 3D-ICs cube-to-cube lateral interfaces. Figure 5.20 shows a test structure for LCI in two MCMs stack, where TX and RX chips are mounted onto MCM via flip-chip technique; and two MCMs are stacked face-to-face.

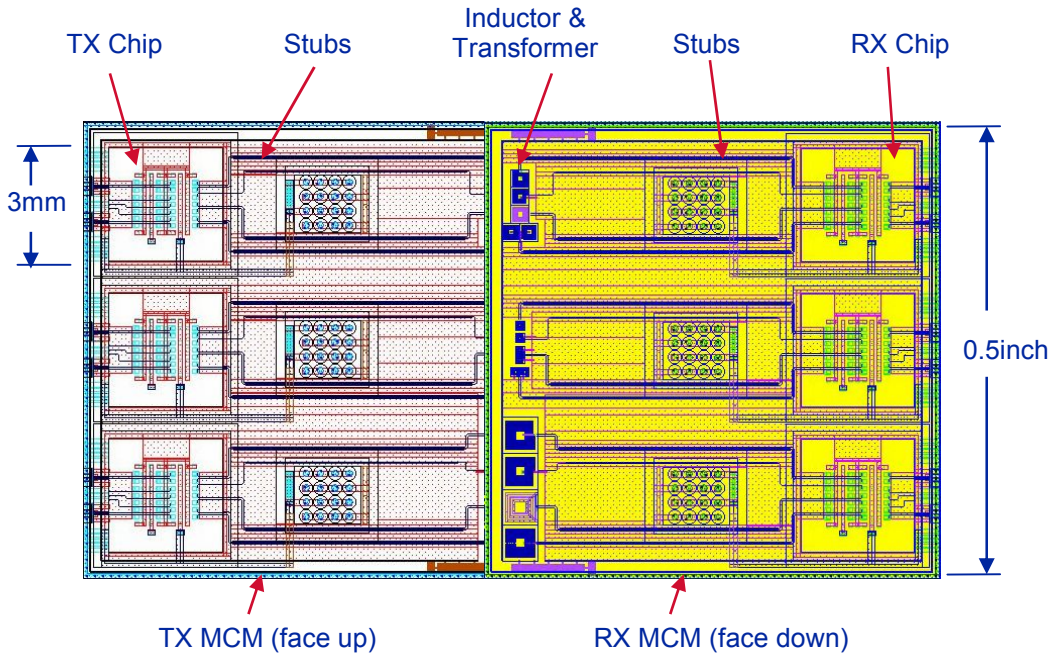


Figure 5.20. A test structure for LCI in a two-MCM stack

5.4.6. Simulation Results

For instance, a copper spiral inductor on a MCM substrate has geometries as 400μm square shape, 3 turns, 25μm line width, 25μm line spacing and 1.5μm copper thickness. For a transformer including such two spiral inductors at 25μm separation, its extracted model parameters by using Q3D are 2.68nH self-inductance, 0.8Ω DC resistance and 0.58 coupling coefficient, which represents 1.57nH mutual inductance. A differential LCI transceiver system communicates pseudo random bit sequence (PRBS) data at 2.0Gb/s and each I/O

consumes 13.0mW power, with the TX and RX consuming 6.5mW each. Figure 5.21 shows an eye-diagram at RX output in a LCI transceiver system for chip-to-chip communications over stacked MCMs interfaces. Table 5.2 summarizes the performance for this LCI test chip.

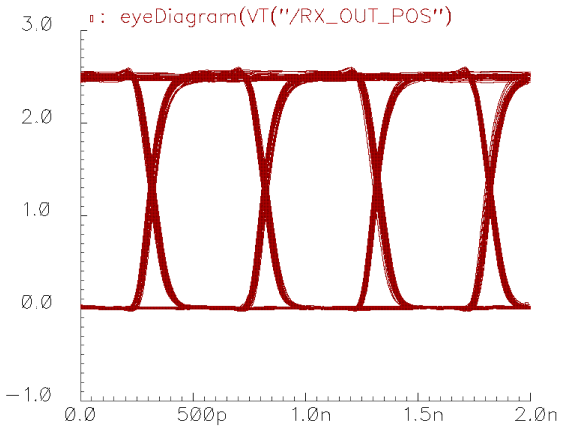


Figure 5.21. Eye-diagram at RX output in a LCI transceiver system

Table 5.2. Summary for LCI test chip with TSMC-0.25µm technology

Test chip	TSMC-0.25µm CMOS, 2.8x3.1mm^2
Substrate	MCNC/RTI MCM-D process
Data rate	2.0Gb/s PRBS
Power	TX: 6.5mW, RX: 6.5mW
Area	TX: 30x30µm^2, RX: 60x30µm^2

Chapter 6. Conclusions and Future Work

6.1. Conclusions

6.1.1. Capacitively Coupled Interconnect (CCI)

The non-contacting structure of CCI relieves mechanical and thermal stresses to I/O pins. Combining a redundant design for DC connections, CCI can provide reliable high-density I/O for chip-to-chip communications. The band-pass CCI channel characteristic does passive equalization for high-speed signaling. It relieves the requirements for coding and equalization circuits. The relatively high input impedance of CCI channel reduces the load for drive circuit and saves significant power.

This dissertation presents the developments of CCI transceiver systems for chip-to-chip communication on MCM and PCB. In the CCI on MCM experiments, two flip chips fabricated in 0.35μm CMOS technology communicated PRBS data at 2.5Gb/s with $< 10^{-12}$ BER via 200μm chip-substrate interface capacitors. In the CCI on PCB experiments, two bare chips fabricated in 0.18μm fully-depleted SOI technology communicated PRBS data at 2.0Gb/s and clock signals at 3.0GHz via 60μm on-chip MIM capacitors.

This dissertation describes pulse-mode signaling circuit design for CCI transceiver systems. It also presents the application of high-k under-fill on CCI coupling elements for improving I/O pad density. Combining with high-k under-fill technology (e.g. 5μm, k=20

material), CCI can provide feasible multi-Gb/s I/O in less than 75μm pad pitch at the chip-package interfaces.

6.1.2. Inductively Coupled Interconnect (LCI)

LCI also has non-contacting structure and band-pass channel characteristic. Moreover, it can communicate at a relatively large separation between coupling elements while tolerating some misalignment. LCI is suitable for proximity interfaces, such as vertical connections in 3D-ICs and chip-package socket and board-board connector interfaces.

This work explored LCI vertical connections in 3D-ICs to take the place of vertical vias. Two stacked chips fabricated in 0.35μm CMOS technology communicated PRBS data at 2.8Gb/s through a pair of 150μm coupling inductors. A novel current-mode pulse signaling circuit for LCI transceiver system in 3D-ICs is presented. The electromagnetic (E-M) modeling for inter-chip transformer and the misalignment tolerance for transceiver system are also addressed.

This dissertation describes a unique power delivery scheme for LCI in 3D-ICs, which provides AC connections through LCI interfaces and DC connections through exposed vias at chip edges. In simulations, two stacked transceiver chips in 0.18μm full-depleted SOI technology communicated PRBS data at 4Gb/s through a pair of 100μm coupling spiral inductors.

This dissertation also proposed a novel 3D-ICs structure that combines LCI interfaces and 3D vertical vias technologies. In measurements, 8 LCI vertical channels operated simultaneously at 1.25Gb/s through inter-chip transformers in 30μm/40μm diameter.

This work also explored LCI scheme on package-to-board socket and board-to-board connector interfaces to increase the I/O pin density. Two MCMs that include transceiver test chips fabricated in 0.25μm CMOS technology and on-substrate spiral inductors are designed to emulate the interfaces of sockets and connectors. Simulation results indicate that the LCI transceiver system can communicate PRBS data at 2.0Gb/s through 400μm spiral inductor pair. The extraction for equivalent circuits of interface transformers and the characterization for LCI channels are addressed. A novel synchronization circuit for LCI transceiver is also addressed.

6.1.3. Comparisons for CCI and LCI

Table 6.1 describes the comparisons between CCI and LCI in physical structures, interface models and signaling methods. CCI coupling elements are easy for manufacturing and modeling; CCI channels are simple for characterization and CCI signaling circuit consumes low power. However, CCI can only communicate over a small separation; it is suitable for close proximity interfaces such as chip-package *L1* level packaging.

In the contrast, LCI coupling elements are difficult for manufacturing and modeling; LCI channels are complex for characterization and LCI signaling circuit consumes more power. However, LCI can communicate over a relatively large separation; it is suitable for large dimension interfaces such as package-board *L2* level packaging or even board-board *L3* level packaging.

Table 6.1. Comparisons of CCI and LCI

	Capacitive coupling (CCI)	Inductive coupling (LCI)
Coupling elements	Series capacitor, Metal plate pair, Capacitance: 100~500 fF, Dimension: 75~300 μm	Interface transformer, Spiral inductor pair, Inductance: 1~5 nH, Dimension: 30~500 μm
Coupling range	1μm ~ 5μm	5μm ~ 25μm
Manufacturability	Simple metal plate	Multiple turns winding, need at least two metal layers, depends on feature width and via size
Interface modeling	Simple, calculation	Complex, need E-M field solver
Channel characterization	Band-pass, relatively wider	Band-pass, relatively narrower
Pulse signaling	voltage mode	current mode
Power dissipation	low power	relatively high power
Design challenges	Parasitic capacitance of plate, SSN noise, Sensitivity to separation	Low impedance elements, Poor termination for reflections, Double pulses, Modeling accuracy
Applications	Chip-substrate in MCM, Chip-package interfaces, Embedded capacitor on board	Vertical connections in 3D-ICs, Package-board socket, Board-board connector

6.2. Future Work

6.2.1. CCI with Embedded Capacitors

As discussed in previous chapters, a CCI with chip-package interface capacitors provides a feasible high-density and high-speed off-chip I/O, and a CCI with on-chip MIM capacitors provides low-power and high-speed off-chip I/O. Recently, on-package or on-board embedded capacitors are proposed to replace surface mounted (SMT) capacitors to improve signal integrity and power integrity [50][51]. It is attractive to investigate the applications of embedded capacitors on CCI.

In an advanced ultra-thin PCB process, multiple 8~16μm dielectric layers with 4~30 permittivity are laminated. Two metal plates that isolated by such a dielectric layer would form a sandwich style on-board embedded capacitor. For various dielectric properties such as thickness and permittivity, coupling capacitances of embedded capacitors in various pad sizes are shown in Figure 6.1. To achieve high-density placement for embedded capacitors, the pad size is desired to be smaller than 20x20 mil^2. Its coupling capacitance is in a range of 0.1pF~4pF, which is suitable for pulse-mode signaling. For instance, two 10x10 mil^2 metal plates, which are isolated by a 16μm high-k (k=30) dielectric layer, have a ~1pF coupling capacitance.

A schematic of CCI transceiver system with an on-board embedded capacitor is shown in Figure 6.2, where a CCI channel includes a stub in TX chip package, an embedded capacitor, a T-line on PCB, and another stub in the RX chip package. There are also on-die termination resistors at both TX and RX chips to eliminate reflections. The pulse amplitude after an embedded capacitor can be estimated by $Zo*Cc*dVc/dt$, where Zo represents the T-

line characteristic impedance, *Cc* represents the coupling capacitance, *dVc/dt* represents the voltage differentiation over time that depends on the edge rate of NRZ signals. The first stub reduces the edge rate of NRZ signals and results in lower pulse amplitude; it requires a strong TX to provide a fast edge rate. The termination resistor at RX pulls down DC level; it brings some challenges in the RX circuit design.

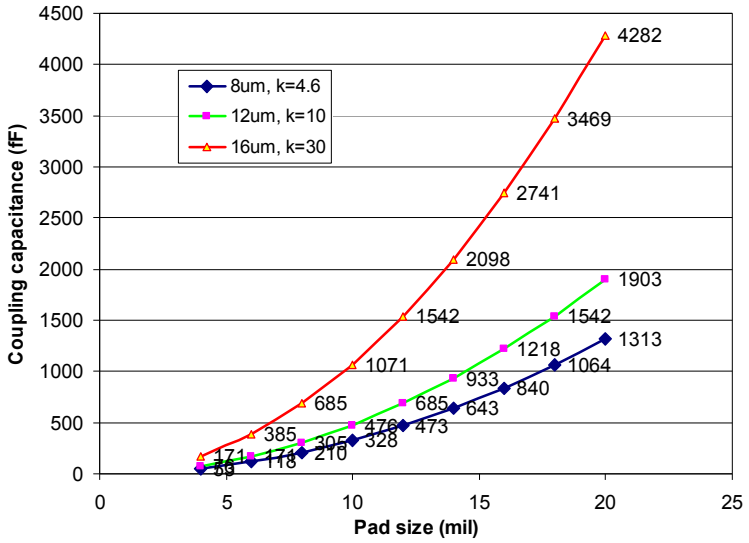


Figure 6.1. Capacitance of embedded capacitor on an ultra-thin PCB

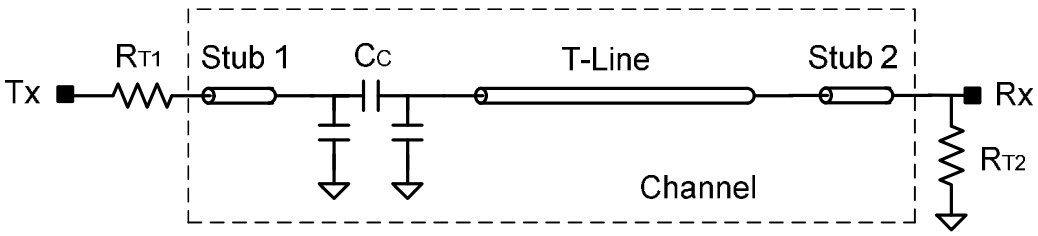


Figure 6.2. Schematic of CCI with an embedded capacitor

For coupling capacitance varying from 0.5~2pF, pulse waveforms are shown in Figure 6.3. A larger capacitor can couple a larger amplitude pulse; however, that pulse has a

longer tail and introduces inter-symbols interference (ISI). The T-line and the second stub attenuate pulse amplitude, extend pulse tail and create more ISI. Considering the ISI, there is an optimal value for coupling capacitance to meet a specific data rate. For instance, to achieve 2.5Gb/s data rate (400ps per unit interval) and less than 10% ISI, a coupling capacitor should be less than 1pF, without additional equalization.

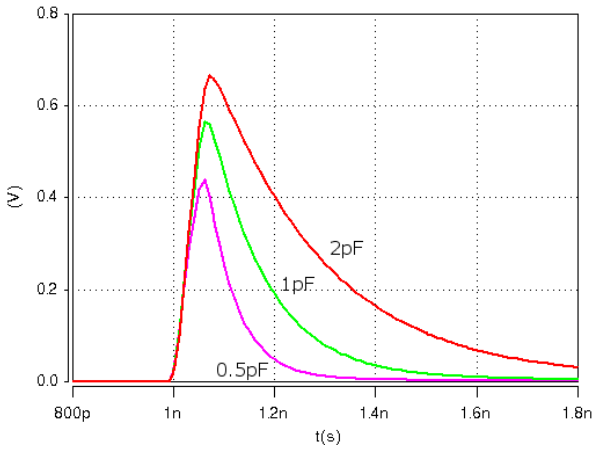


Figure 6.3. Pulse waveforms for various embedded capacitors

To eliminate the ISI in a CCI channel with an embedded capacitor, a passive equalization structure is proposed and shown in Figure 6.4. The passive equalizer includes an on-chip poly-silicon resistor (e.g. 1k~3k Ω), and an on-chip MIM capacitor (e.g. 0.3p~0.5p F); it works as a high-pass filter to compensate the high-frequency loss in the T-line. At the cost of some additional attenuation for pulse amplitude, the passive equalizer cuts the tail of pulse and limits the pulse width to be less than one UI. Another benefit of this passive equalizer is that it isolates the receiver circuit with the termination resistor; and the pulses can be biased to a DC level and be suitable for pulse amplifier operations.

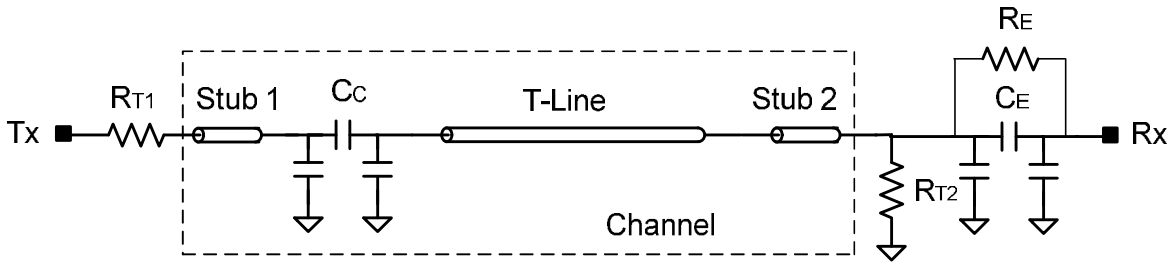
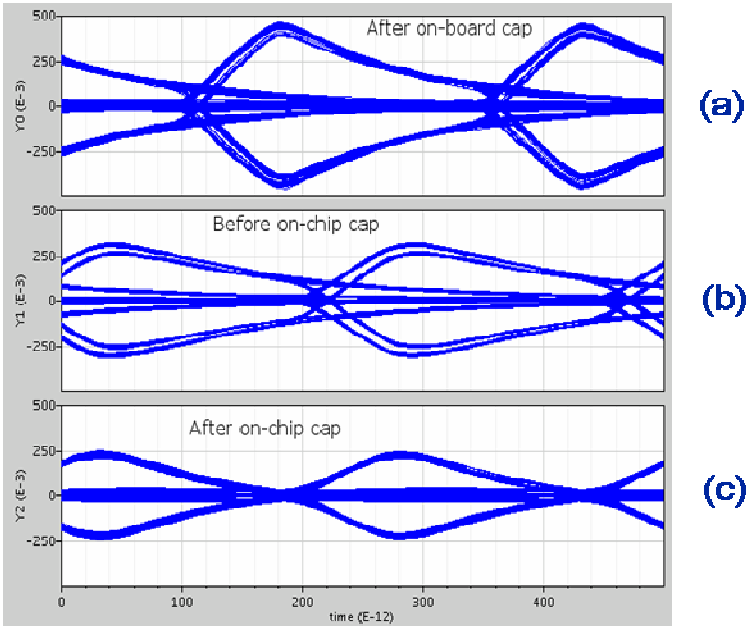


Figure 6.4. CCI with an embedded capacitor and a passive equalizer

For a CCI channel including a 1pF embedded capacitor, a 25cm T-line and two 2cm stubs, to achieve 4Gb/s data rate (250ps per UI), the parameters of the equalizer are tuned to be C_E=0.3pF and R_E=3kΩ. The simulated eye-diagrams after the embedded capacitor, before the equalizer and after the equalizer are shown in Figure 6.5.



(a) Pulses generated by the embedded capacitor, (b) Pulses attenuated by the T-line,
(c) Pulses after passing the passive equalizer

Figure 6.5. Eye-diagrams for CCI with embedded capacitor and passive equalizer

6.2.2. CCI at Package-to-Board Socket Interfaces

Conventional conductive socket pins can be replaced by non-contacting capacitive coupling elements, such as a pair of metal pads coating by high permittivity material. A scheme for CCI at a socket interface is shown in Figure 6.6, where two stubs on packages connect TX and RX circuits to coupling capacitors at package-board interfaces.

In the CCI chip-to-chip communication system discussed in Chapter 3, coupling capacitors are placed very close to transceiver circuitry, e.g. <1cm and the connections between transceiver circuitry and coupling capacitors are considered as lumped RC parasitic. However, if the coupling capacitors are placed at socket interface, there are stubs usually longer than 1cm. The velocity of signal propagation on a FR4 board is 14cm/ns, given by $v = c/\sqrt{\varepsilon_r}$, where c =30cm/ns is the speed of light, and ε_r=4.6 is the permittivity of FR4. For multi-GHz signal propagation, the transition time is less than 100ps. Because the flight time for a 1cm stub is around 70ps, which is comparable to the transition time, the stubs need be treated as transmission lines instead of lumped elements.

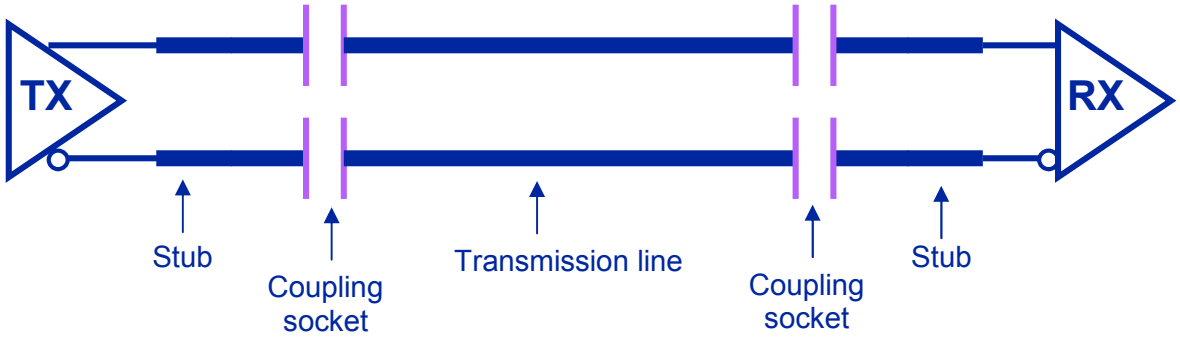


Figure 6.6. CCI application on package-board socket interface

The stubs on the package create many challenges in transceiver system design as well as circuit design. The first stub degrades the edge rate of NRZ signals and results in smaller pulses at the first capacitive coupling socket. The second stub presents a low impedance load to the second capacitive coupling socket. It cannot provide enough damping for the second order transfer system and introduces overshoot, which is also referred to a double pulse. Because the coupling capacitors introduce an impedance discontinuity, it forces the placements of on-board terminations at both sides of the T-line and on-chip terminations at both TX and RX.

6.2.3. LCI Application on Chip-to-Chip Communications

Single LCI interface applications for chip-to-chip communication were presented in the previous chapter. Figure 6.7 illustrates a LCI chip-to-chip communication system with two transformers. Because a transformer usually has low input impedance, series termination resistors are needed at the end of T-line to reduce reflections.

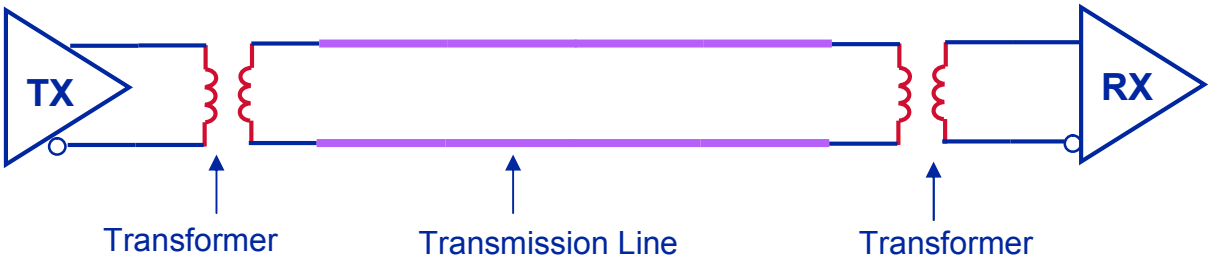


Figure 6.7. LCI application on chip-to-chip communications with two transformers

A single transformer can be represented by a "T" model, which includes a mutual inductance *M*, two leakage inductances *(L-M)* and two parasitic resistances *R*. Assume the T-line is an ideal transmission line, then a two transformers LCI channel can be represented by cascading two "T" models, which is shown in Figure 6.8.

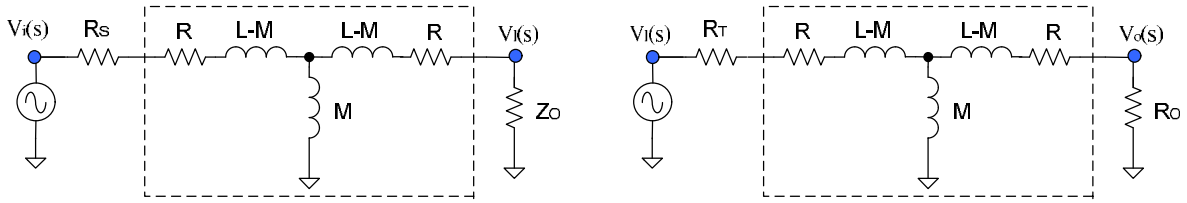


Figure 6.8. A cascaded "T" model for a LCI system with two transformers

Transfer functions for the first and the second transformers are expressed by

$$\frac{Zo\ s\ M}{\left(Rs + R + s\,(L - M) + \frac{(s\,(L - M) + R + Zo)\ s\ M}{s\,(L - M) + R + Zo + s\ M}\right)(s\,(L - M) + R + Zo + s\ M)},$$

and

$$\frac{Ro\ s\ M}{\left(Rt + R + s\,(L - M) + \frac{(s\,(L - M) + R + Ro)\ s\ M}{s\,(L - M) + R + Ro + s\ M}\right)(s\,(L - M) + R + Ro + s\ M)},$$

where *s* represents angular frequency, (j2πf). *Rs, Zo, Rt* and *Ro* represent TX output impedance, T-line characteristic impedance, series termination resistance and RX input impedance, respectively. For instance, a LCI system with two transformers has following parameters: L=1nH, R=10Ω, Rs=Zo=Ro=50Ω and Rt=40Ω, its frequency responses are shown in Figure 6.9. The second transformer would attenuate signal amplitude significantly.

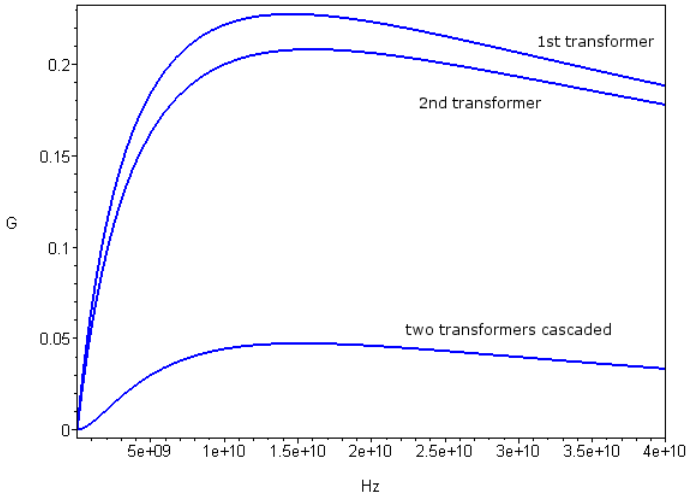
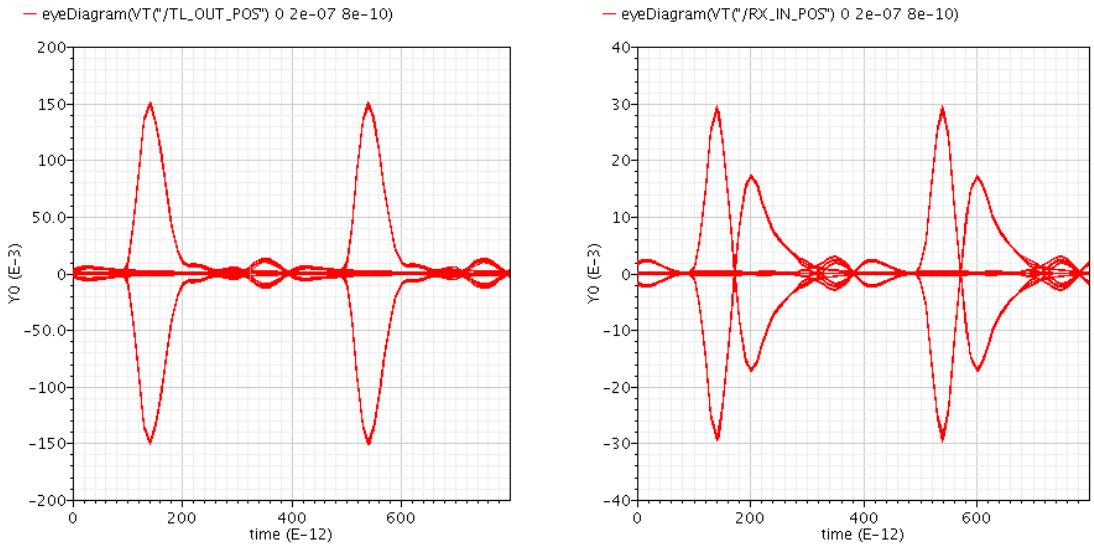


Figure 6.9. Frequency responses for a LCI system with two transformers

The first transformer has a band-pass characteristic; it differentiates NRZ signals into RZ pulses. By adding a series termination resistor at the front of the second transformer, the termination resistance plus the input impedance of the transformer can match the T-line impedance and eliminate reflections at a specific frequency. However, the input impedance of transformer depends on frequency and is comparable to the T-line impedance. It is impossible to match the T-line impedance in the frequency range of the whole pulse spectrum; and it causes reflections at the end of T-line.

The second transformer has the same band-pass characteristic as the first one; it differentiates the pulses and creates double pulses. For instance, simulated eye-diagrams for the single pulse at the end of T-line and the double pulses at the input of RX are shows in Figure 6.10. Due to the double pulses, the RX circuit cannot recover the NRZ signals. Limiting or avoiding double pulses is one of the major design challenges in a LCI system with two transformers.



(a) Single pulse at the end of T-line (b) Double pulses at the input of RX

Figure 6.10. Eye-diagrams in a LCI system with two transformers

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APPENDICES

Appendix A. Fully-depleted SOI Technology

Silicon-on-insulator (SOI) technology refers to placing a thin silicon layer on top of a buried insulator layer, such as a silicon oxide layer. Devices such as a transistor are then built on the thin silicon layer. A cross-section of n-channel MOSFET on SOI technology is shown in Figure A.1. By dielectrically isolating the devices, SOI technology significantly reduces junction capacitances, allowing circuits to operate at higher speed or substantially lower power at the same speed. The island-style device structure also eliminates latch-up failure in bulk CMOS technology [43].

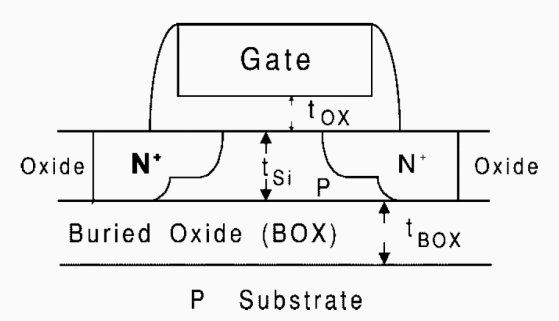


Figure A.1. Cross-section of a N-channel SOI transistor [43]

In a fully-depleted SOI device, an ultra-thin (50nm or so) silicon film is used so the depletion layer extends through the entire film. Its advantages include the elimination of the floating-body effect and better short-channel behavior. However, the ultra-thin silicon film dictates a low device threshold voltage with high sensitivity to film thickness variations.

Stringent control of the film thickness imposes severe limitations on the manufacturability of the fully-depleted SOI devices [43][5].

A partially-depleted SOI device, with film thickness around 150nm, alleviates the constraint on film thickness, thus eases the manufacturing problem. The major issue of the partially depleted SOI device is the "floating-body effect" and the resulting parasitic bipolar effect [43][5].

Appendix B. Three-dimensional ICs Technology

MIT Lincoln Lab has developed a three-dimensional integrated circuits (3D-ICs) technology where three device layers in fully-depleted SOI technology are integrated at wafer process level [40]. Beside the fully-depleted SOI fabrication, Lincoln Lab 3D-ICs technology includes low-temperature wafer-wafer oxide bonding, precision wafer-wafer alignment, and dense vertical interconnections. Compared to a micro bump 3D-ICs technology where bump size is 30μm at a pitch of 60μm [42], Lincoln Lab 3D-ICs technology offers higher density vertical interconnections where vertical via is 1.75μm square at a pitch of 5.5μm.

The 3D circuit integration process begins with the fabrication of three fully-depleted SOI active sections that are called tiers. Then wafer 2 is flipped, aligned, and bonded to wafer 1. The handle silicon substrate of wafer 2 is removed, 3D vias are etched through the oxides of tier 2 and tier 1 and stop on metal pads in tier 1, and tungsten is deposited and planarized. Tier 3 is transferred to the tiers 1-2 assembly using the same processes except that

the 3D vias connect the top-level metal of tier 3 to the first metal level of tier 2. A completed 3D assembly is shown in Figure B.1, after bond pads are etched to expose the back of the first level metal of tier 3 for probing and wire bonding [44].

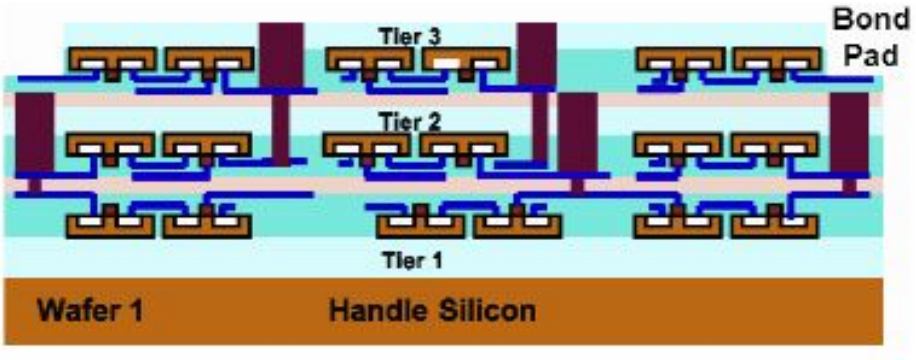


Figure B.1. Cross-section of a 3D-ICs in FD-SOI technology [44]

Appendix C. Multi-Chip Module with Buried Bumps

In a multi-chip module (MCM) [47], multiple bare chips are mounted onto a common carrier or substrate via wire-bonding or flip-chip technologies. There are different types of MCM substrates available such as: co-fired ceramics (MCM-C), organic laminates (MCM-L) and deposited dielectric (MCM-D). To demonstrate ACCI with buried bumps, a MCM-D substrate was fabricated at MCNC (now RTI) [12][13]. The substrate was manufactured using silicon or alumina wafer with four benzocyclobutene (BCB) dielectric layers and five copper interconnect layers, each 2μm thick. An illustration for the substrate layer stack-up is shown in Figure C.1.

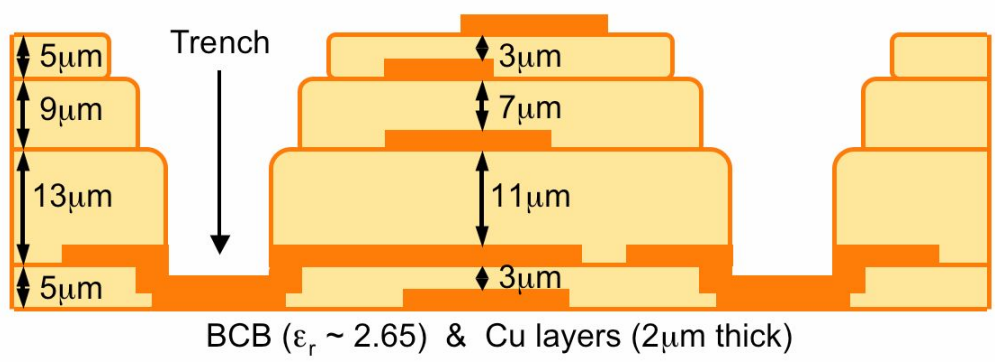


Figure C.1. Cross-section of a MCM substrate for buried bumps

The two lower metal layers (M1 & M2) were used for power/ground distributions and reference planes, and to form landing layers for the buried bumps. The two inner metal layers (M3 & M4) were used for the routing of T-lines, and the top metal layer (M5) was mainly used to form the ACCI passive structures.

Figure C.2 shows a cross section of an assembled substrate and chip. Coupling capacitors formed at chip-substrate interfaces between the buried bumps which have a 250μm pitch. This intimate proximity resulted in a separation between the chip and substrate coupling plates of approximately 1μm. By controlling the solder ball volume and re-flow parameters, a specific gap distance can be achieved.

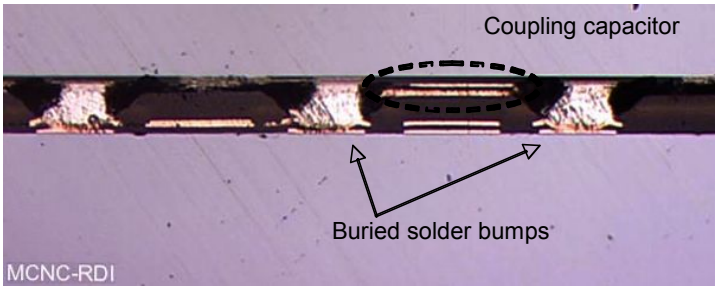
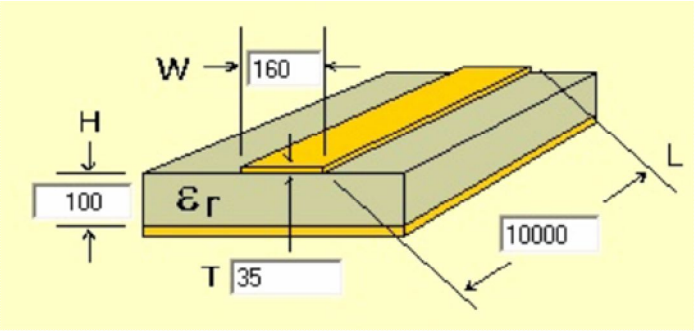


Figure C.2. Micrographic for a CCI interface in MCM

Appendix D. Transmission Line Modeling

In chip-to-chip communication channels, a transmission line is either a micro-strip line which is routed on an outside metal layer and has a reference plane, or a strip line which is routed on an inside metal layer and has two reference planes. A transmission line can be a single-ended line or a coupled line which is commonly called a differential line. For a transmission line with given geometries and dielectric structures, its characteristic impedance can be estimated by using formulas [6] or design tools such as AppCAD [59]. Figure D.1 shows a 3D view for a 50ohm single-ended micro-strip line on FR4 board, where "W", "L", "T", "H" represents the trace width, trace length, metal thickness, and dielectric thickness, respectively.



(unit: μm)

Figure D.1. 3D view of a 50ohm micro-strip line on FR4 board

In Hspice simulation, a transmission line can be modeled by a "W element", which includes unit length parameter matrixes such as R_0, L_0, G_0, C_0, R_s and G_d. Where R_0, L_0, G_0, C_0, R_s and G_d represents DC resistance, DC inductance, DC conductance, DC capacitance, skin effect resistance and dielectric loss conductance. For a given geometries and dielectric

properties, Hspice provides a 2D field solver to calculate those RLGC parameters [62]. For a single-ended micro-strip line shown in Figure D.1, the calculated RLGC parameters are:

Lo = 2.997130e-07 (H/m), Co = 1.180495e-10 (F/m),

Ro = 3.100174e+00 (Ohm/m), Go = 0.000000e+00 (S/m),

Rs = 7.738046e-04 (Ohm/(m*sqrt(Hz)), Gd = 7.788135e-12 (S/(m*Hz)).

Its frequency responses in terms of S_{21} and S_{11} are shown in Figure D.2. Generally, a transmission line presents a low-pass characteristic due to the frequency dependent losses, e.g. this 10cm micro-strip line has a -3dB corner frequency at 12.95GHz.

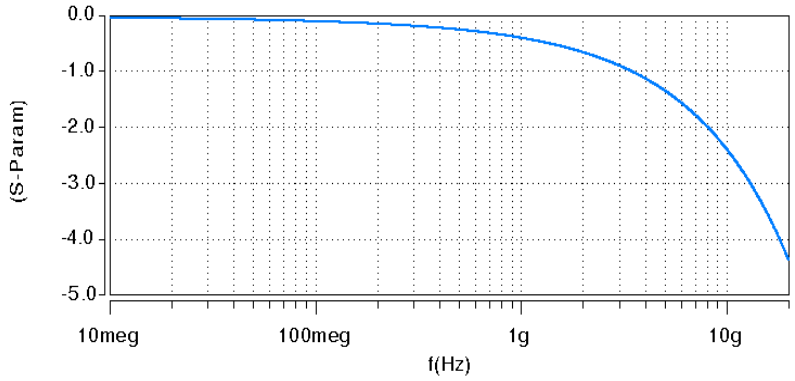


Figure D.2. Frequency responses for a 10cm micro-strip line

In Spectre simulations, a transmission line can be modeled by a “mtline” cell which is either a lumped macro-model or a RLGC matrix in unit length. For a given transmission line geometries and dielectric properties, Spectre provides a line model generator (LMG) to create both lumped sub-circuit and unit length RLGC parameters [63]. A wideband “mtline” RLGC model file includes parameter sets for multiple frequency points. For a single-ended micro-strip line shown in Figure D.1, the calculated RLGC parameters at 1GHz are:

Lo = 3.049990e-07 (H/m), Co = 1.129000e-10 (F/m),

Ro = 4.119558e+01 (Ohm/m), Go = 0.000000e+00 (S/m),

Appendix E. Inductor and Transformer Modeling

In simulations for an inductively coupled transceiver system, AC coupling passive elements such as spiral inductors and transformers need be modeled with either equivalent circuits or S-parameter matrixes. Figure E.1 shows the layout of a 6 turns spiral inductor that has 30X30 μm^2 size, 1μm line width and 0.5μm line spacing. A spiral inductor can be modeled by a "pi" sub-circuit shown in Figure E.2, where L and R represent self inductance and winding resistance, R_1, C_1, R_2 and C_2 represent parasitic shunt resistance and capacitance to substrate.

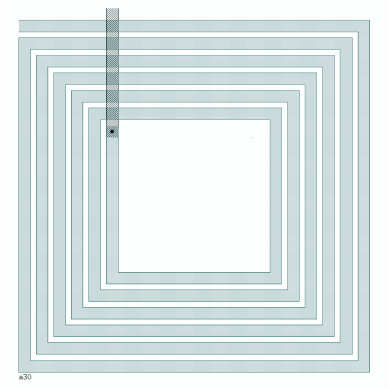


Figure E.1. Layout for an on-chip spiral inductor

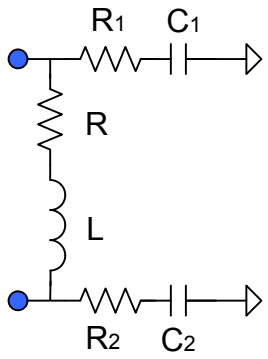


Figure E.2. A "π" model for a spiral inductor

ASITIC, a free CAD tool from U.C. Berkeley [45], can be used for modeling spiral inductors. It provides convenient geometric design and fair accurate numerical analysis. For a simple inductor shown in Figure E.1, its calculated parameter set at 1GHz in "pi" model are:

$$L = 1.038 \text{ nH}, R = 42.56 \text{ ohm}$$

$$C_1 = 6.502 \text{ fF}, R_1 = 2.923 \text{ kohm}$$

$$C_2 = 4.604 \text{ fF}, R_2 = 4.426 \text{ kohm}$$

ASITIC can be also used to analysis stack transformers. It can calculate the magnetic coupling coefficient k between two coupled inductors. However it can not model the capacitive coupling between two inductor windings. Ansoft Q3D Extractor is a 3D electromagnetic (E-M) field solver and can create a more accurate equivalent circuit for a transformer. Figure E.3 shows a 3D view of a transformer in the Q3D filed solver, where two spiral inductors separate 12.5μm and each inductor has 400μm size, 3 turns, 25μm line width and 25μm line spacing. An equivalent circuit for a transformer is shown in Figure E.4, where each inductor is represented by a "T" model which includes two identical series resistance-inductance portions and a shunt capacitance portion, the inductive coupling is represented by

mutual inductances $M_{12}=k_{12}*\sqrt{L_1*L_2}$ and $M_{34}=k_{34}*\sqrt{L_3*L_4}$, the capacitive coupling is represented by a cross capacitance C_{12}.

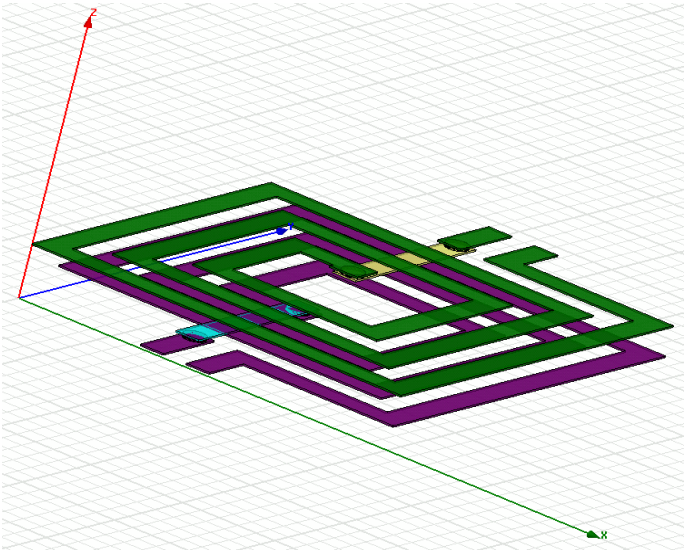


Figure E.3. 3D view of a transformer in Q3D field solver

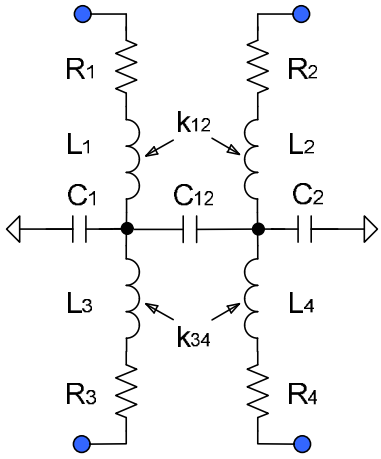


Figure E.4. An equivalent circuit for a spiral transformer

For a transformer shown in Figure E.3, the extracted circuit parameters are:

$L_1 = L_3 = 1.33$ nH, $R_1 = R_3 = 1.05$ ohm, $L_2 = L_4 = 1.33$ nH, $R_2 = R_4 = 1.05$ ohm,

$k_{12} = 0.66$, $k_{34} = 0.66$, $C_1 = 21.7$ fF, $C_2 = 21.7$ fF, $C_{12} = 102.6$ fF.

The winding directions of two coupled inductors determine the sign of coupling coefficient *k*. If two spiral windings are at the same direction, *k* has a positive sign; otherwise *k* has a negative sign. The inductive coupling between the primary and secondary inductors could be in-phase or out-of-phase regarding the sign of *k*. There is also a crossover capacitance between two windings represents the capacitive coupling that is always in-phase.

For a transformer shown in Figure E.3, its frequency responses in terms of transmission coefficient S_{21} are shown in Figure E.5, where the dash-line represents the case for in-phase inductive coupling; the dot-line represents the case for out-of-phase inductive coupling; the solid-line represents a virtual case for ignoring crossover capacitance. In case of in-phase coupling, the crossover capacitance introduces resonate "zero" point and limits the bandwidth of transformer. In case of out-of-phase coupling, it brings an anti-resonate "pole" point to extent the bandwidth of transformer.

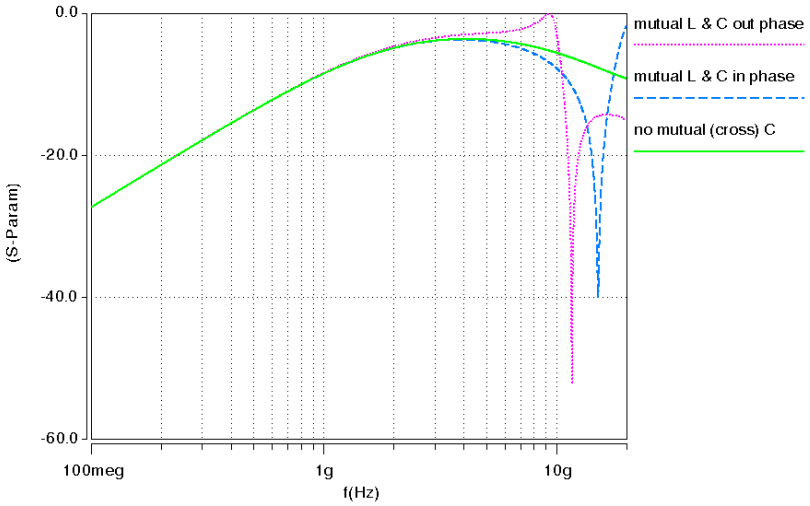


Figure E.5. Frequency response (S_{21}) of a spiral transformer

Appendix F. Signal Spectrum Analysis

A non-return-to-zero (NRZ) binary signal stream is shown in Figure F.1, which includes 10 symbols “0001110111” at 2.5G baud rate as well as 2.5Gb/s data rate. A unipolar return-to-zero (RZ) signal can be converted from a NRZ signal by Manchester binary phase-shift keying (BPSK) modulation, e.g. using “01” RZ transition symbols to represent “1” NRZ symbol and using “10” RZ transition symbols to represent “0” NRZ symbol. A RZ signal stream is also shown in Figure F.1, which includes 20 symbols “10101001010110010101” at 5.0G baud rate but 2.5Gb/s data rate. In CMOS circuit design, a NRZ-RZ converter can be built by using a NRZ signal at xGb/s to select a pair of differential clocks at xGHz, e.g. a “0” NRZ data selects a positive phase clock and a “1” NRZ data selects a negative phase clock.

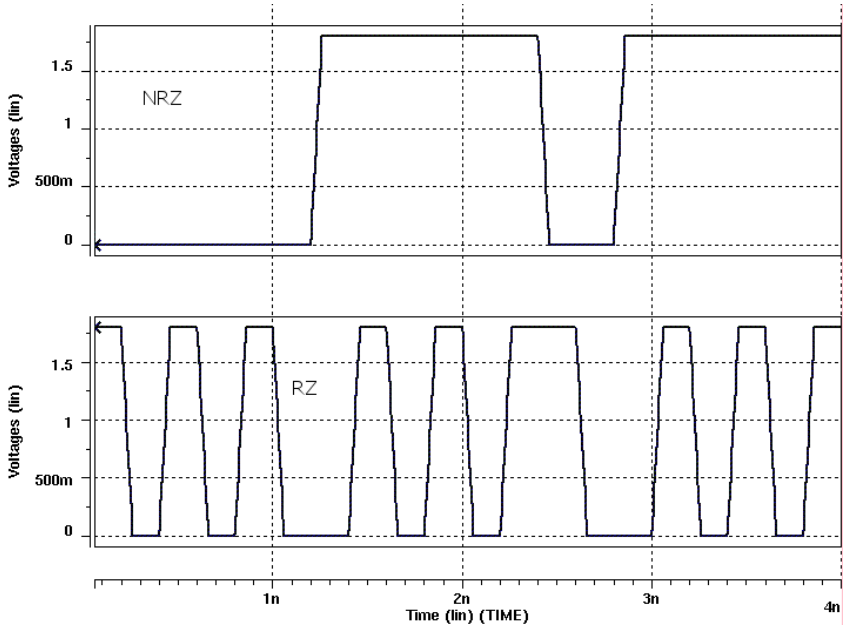


Figure F.1. Waveform of 2.5Gb/s NRZ and RZ signals

FFT spectrum analysis results for 1k bits NRZ and RZ signals are shown in Figure F.2. A 2.5Gb/s NRZ signal has a fundamental frequency at 1.25GHz and a third order harmonic frequency at 3.75GHz. However, a 2.5Gb/s RZ signal has a fundamental frequency at 2.5GHz and a third order harmonic frequency at 7.5GHz. The RZ signal spectrum has more high-frequency components than NRZ signal spectrum, and the bandwidth requirement of RZ signaling is double of NRZ signaling. RZ signal is a DC balanced code and introduces less inter-symbol-interference (ISI) than NRZ signal does. Another benefit of such RZ Manchester code is the clock information is carried by the signals, and make clock data recover (CDR) circuit design to be simpler. For AC coupling pulse-model I/O, the pulse width depends on the edge rate of source signal instead of baud rate. AC coupled transceiver system can apply RZ binary signal as a source and take its advantages.

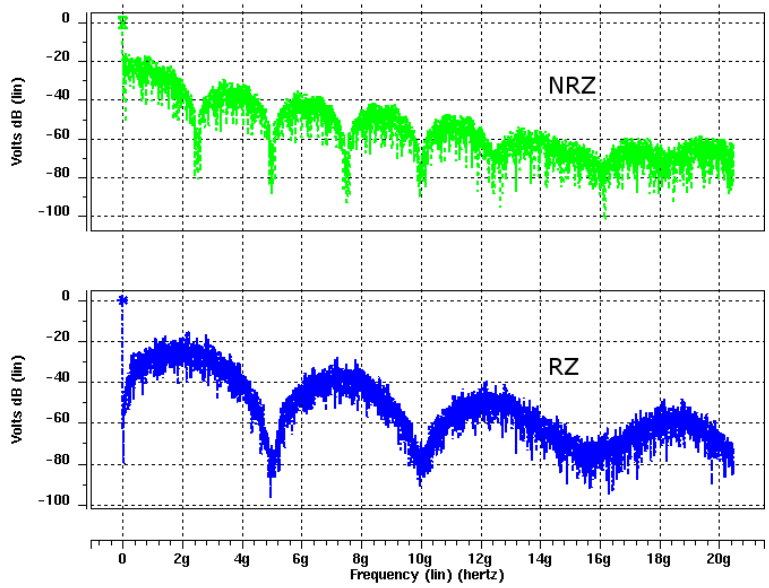


Figure F.2. Spectrum of 2.5Gb/s NRZ and RZ signals

NRZ signals can also be converted into bipolar RZ pulses, e.g. a positive pulse represents a rising edge of NRZ signal; a negative pulse represents a falling edge of NRZ signal; and a "zero" DC level represents a non-transition status for NRZ signal. Figure F.3 shows a waveform and spectrum for 2.5Gb/s pulses. Compared with the spectrum of NRZ signals, bipolar RZ pulses have a same fundamental frequency, e.g. 1.25GHz. It also can be observed that both unipolar and bipolar RZ signals include few low frequency components. However, they have different spectrum envelopes for fundamental frequency and harmonics.

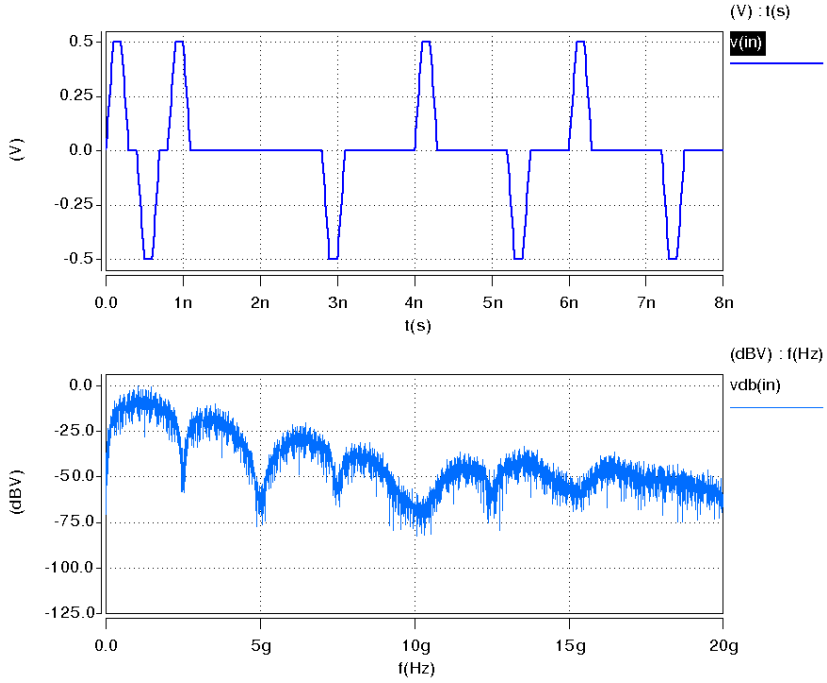


Figure F.3. Waveform and spectrum of 2.5GHz bipolar RZ Pulses

Appendix G. Schematics of Transceiver Circuit

G.1. TSMC-0.35μm Test Chip for LCI in 3D-ICs

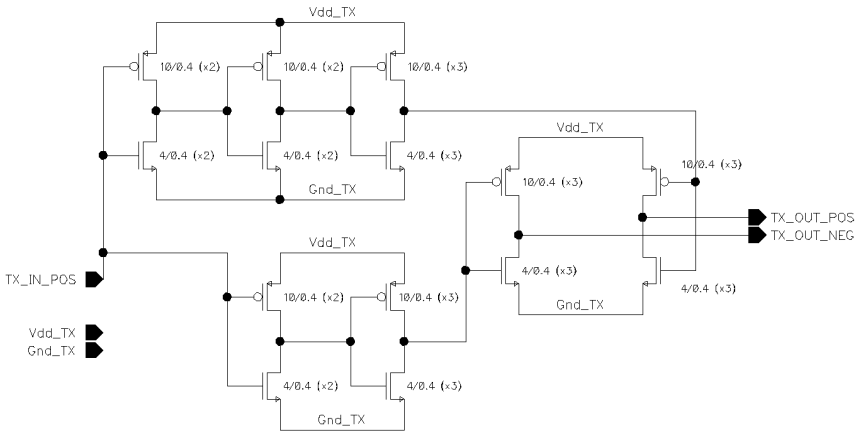


Figure G.1. TX circuit for LCI in 3D-ICs with TSMC-0.35μm technology

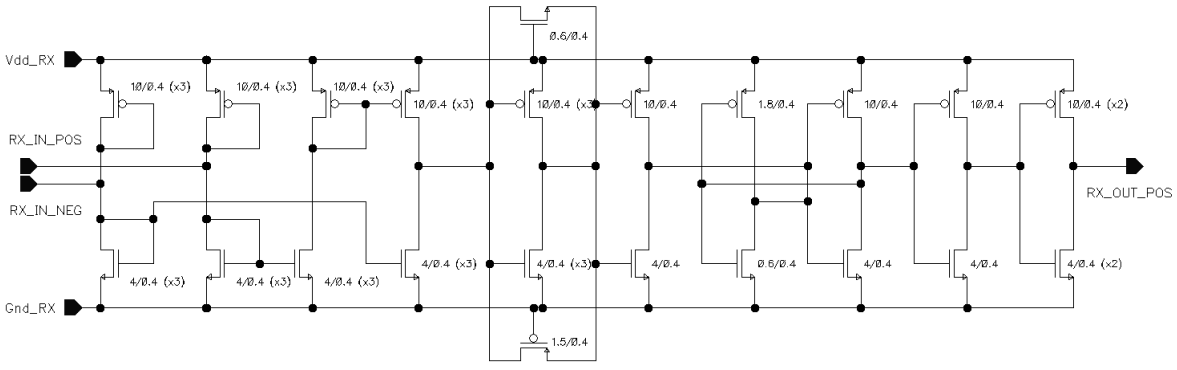


Figure G.2. RX circuit for LCI in 3D-ICs with TSMC-0.35μm technology

G.2. TSMC-0.25μm Test Chip for LCI in Chip-to-Chip Communications

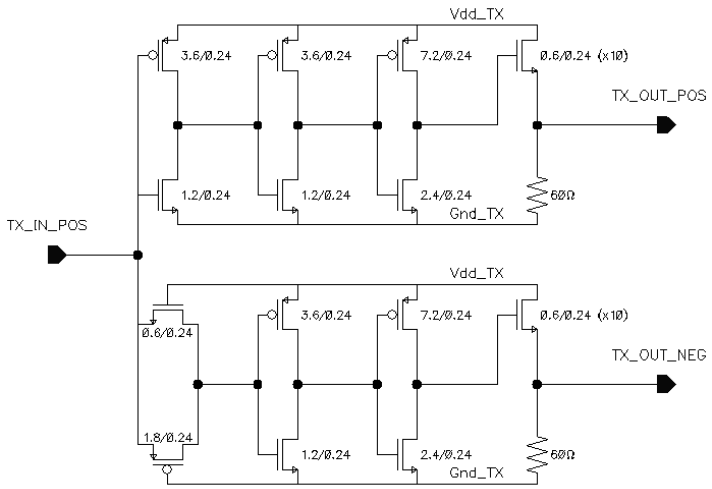
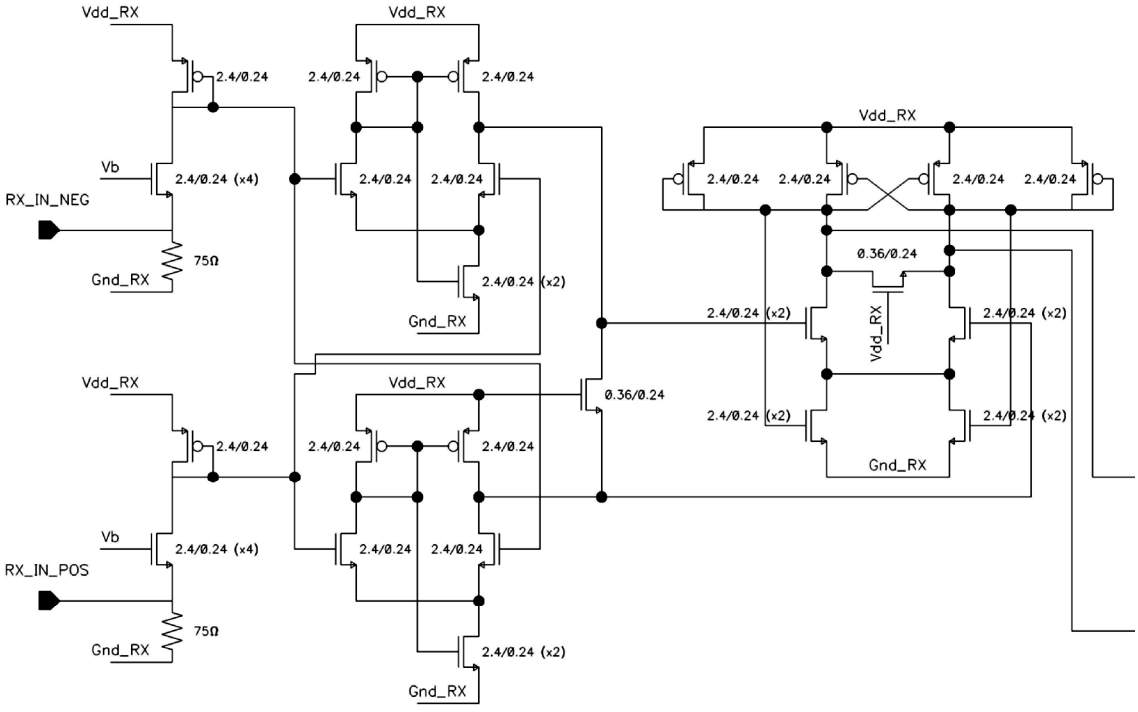
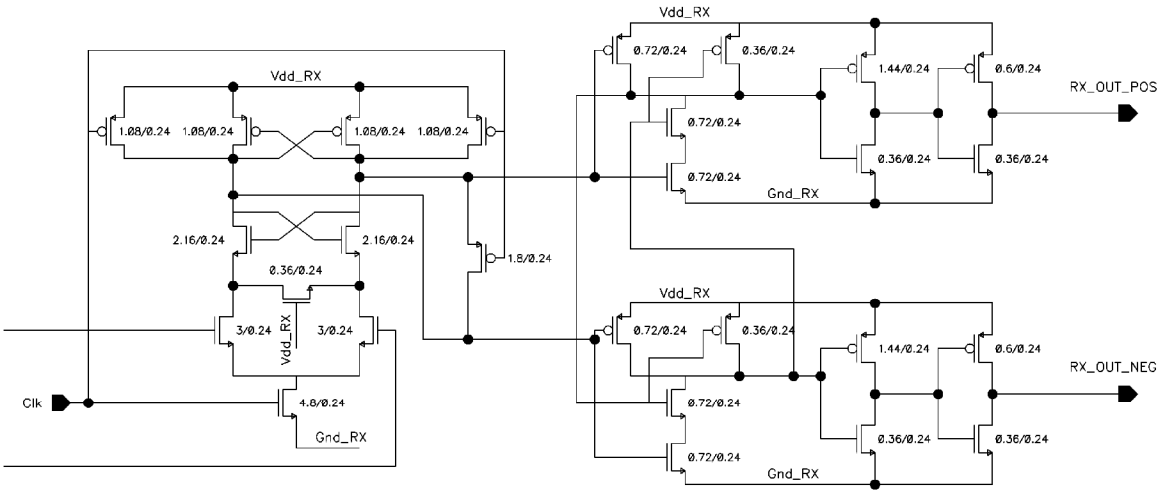


Figure G.3. TX circuit in a LCI link with TSMC-0.25μm technology



(a) Sensing and amplifying stages



(b) Sampling and latching stages

Figure G.4. RX circuit in a LCI link with TSMC-0.25µm technology

G.3. FDSOI-0.18µm Test Chip for LCI in Multi-Tier 3D-ICs

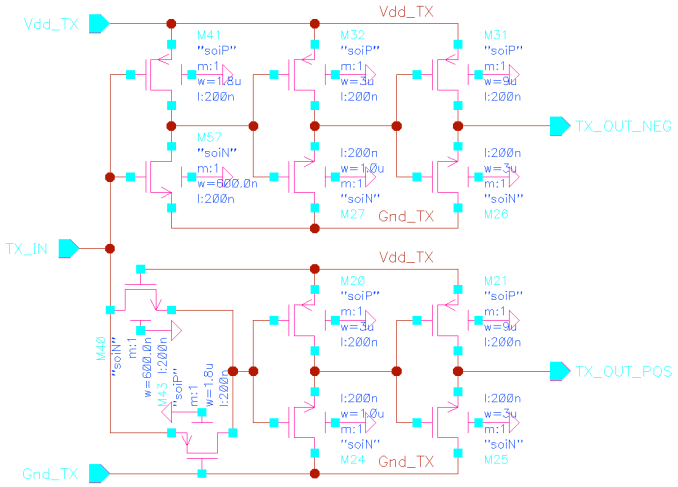
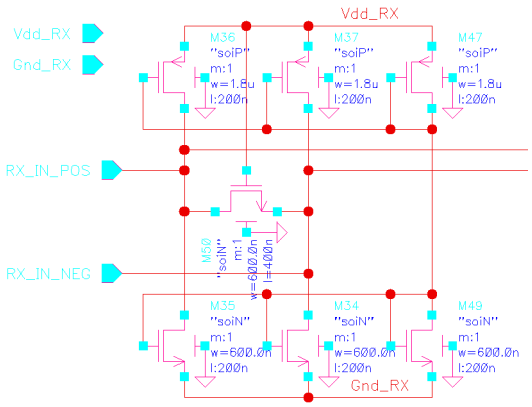
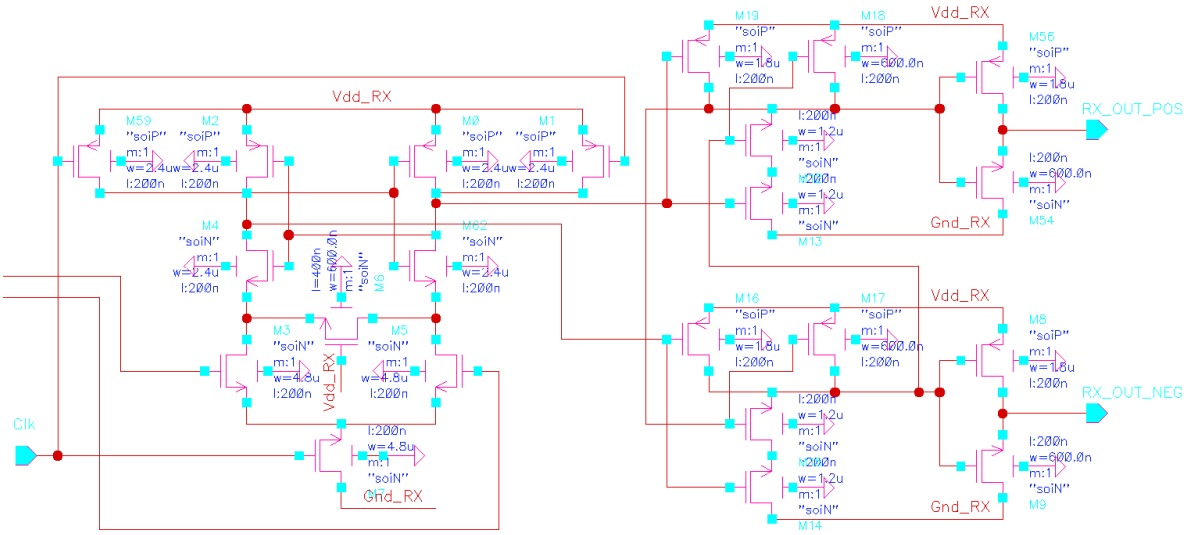


Figure G.5. TX circuit for LCI in 3D-ICs with FDSOI-0.18µm technology



(a) Sensing stage



(b) Sampling and latching stage

Figure G.6. RX circuit for LCI in 3D-ICs with FDSOI-0.18µm technology