ABSTRACT

SURESH, ARUN. Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors, Non-volatile Memory and Circuits for Transparent Electronics. (Under the direction of Dr. John F. Muth).

The ability to make electronic devices, that are transparent to visible and near infrared wavelength, is a relatively new field of research in the development of the next generation of optoelectronic devices. A new class of inorganic thin-film transistor (TFT) channel material based on amorphous oxide semiconductors, that show high carrier mobility and high visual transparency, is being researched actively. The purpose of this dissertation is to develop amorphous oxide semiconductors by pulsed laser deposition, show their suitability for TFT applications and demonstrate other classes of devices such as non-volatile memory elements and integrated circuits such as ring oscillators and active matrix pixel elements.

Indium gallium zinc oxide (IGZO) is discussed extensively in this dissertation. The influence of several deposition parameters is explored and oxygen partial pressure during deposition is found to have a profound effect on the electrical and optical characteristics of the IGZO films. By optimizing the deposition conditions, IGZO TFTs exhibit excellent electrical properties, even without any intentional annealing. This attribute along with the amorphous nature of the material also makes IGZO TFTs compatible with flexible substrates opening up various applications.

IGZO TFTs with saturation field effect mobility of 12 – 16 $cm^2 V^{-1} s^{-1}$ and subthreshold voltage swing of < 200 mV $decade^{-1}$ have been fabricated. By varying the oxygen partial pressure during deposition the conductivity of the channel was controlled to give a low off-state current ~ 10 pA and a drain current on/off ratio of $> 1 \times 10^8$. Additionally, the effects of the oxygen partial pressure and the thickness of the semiconductor layer, the choice of the gate dielectric material and the device channel length on the electrical characteristics of the TFTs are explored.

To evaluate IGZO TFT electrical stability, constant voltage bias stress measurements were carried out. The observed logarithmic dependence of the threshold voltage shift to the stress duration was modeled using a charge trapping/tunneling mechanism at the semiconductor/dielectric interface. By incorporating platinum nanoparticles in the dielectric

layer of the TFT, non-volatile memory characteristics were achieved. The devices exhibited good memory behavior and up to 10 % charge retention extrapolated over 10 years.

The potential application for IGZO TFTs is examined by fabricating and characterizing 5- and 7-stage ring oscillators. The 5-stage ring oscillators operate at more than 2 MHz and have a sub 50 ns propagation delay at a supply voltage of 25 V. To the best of our knowledge these are the fastest all-transparent ring oscillators reported to date. As a practical demonstration, we integrated IGZO TFTs with a novel thin film electroluminescent phosphor to form an active matrix pixel element. The output intensity of the phosphor was successfully modulated by the TFT. These results demonstrate that IGZO TFTs are viable candidates for transparent circuits and display applications.

Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors, Non-volatile Memory and Circuits for Transparent Electronics

by
Arun Suresh

A dissertation submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Electrical Engineering

Raleigh, North Carolina

Summer 2009

APPROVED BY:

_____	_____
Dr. John F. Muth Committee Chair	Dr. Leda M. Lunardi
_____	_____
Dr. Veena Misra	Dr. Mark Johnson

BIOGRAPHY

Arun Suresh was born in Madras, the capital city of the temple state of Tamil Nadu (located in Southern India). He graduated from Padma Seshadri Bala Bhavan and went on to get his Bachelors in Metallurgy and Materials Engineering at IIT Kharagpur in West Bengal. Not being too happy with being in a small pond in India he applied to universities in the United States for his Masters degree – only to find himself in another small pond: at Happy Valley in Pennsylvania State University. He "sailed" through his Masters degree and went on to work for Analog Devices Inc. at Boston, MA. After working for 4 years he succumbed to another calling to get back to research. In Fall 2005 he gained admission to the Electrical Engineering department at North Carolina State University for his Doctoral work. Since then he has worked under the guidance of Dr. John Muth on thin-film transistors for transparent electronic applications.

ACKNOWLEDGEMENTS

Quite a few people have been instrumental in shaping the 4 years I spent at North Carolina State University,

Preethika My support – solid, like a rock. The only reason why I ventured on this endeavor. My source of constant love, encouragement, inspiration and my loving wife.

Mummy & Daddy For their unrelenting efforts to provide for me the best life possible. I won't be the person I am without their love and understanding.

Amma & Appa For their useful insights on life and prayers.

Dr. Muth For being an invaluable resource and for his support, guidance and his ability to make me look for answers.

Dr. Lunardi **Dr. Misra** **Dr. Johnson** For acting as my committee members. Dr. Lunardi for being as excited about my work as I was and being a "surrogate mother" for the group when Dr. Muth was serving in Iraq. Dr. Misra for letting me use the facilities in her lab, I spent half my time here using her stuff.

Joe For training me to be independent in the clean room and not getting too mad when I messed things up.

Patrick For discussions and an excellent bouncing board for ideas. I don't know if he benefited from our discussions but I sure did. A good friend to boot.

Smita & Akash Like family. Preethika and I enjoyed the time we spent together. Smita, with her expressive eyes and Akash with his "white heart" will be missed wherever we go.

And all the past and present students in Dr. Muth's and Dr. Misra's group and office mates in 112 MRC, thanks for making my stint here comfortable and productive and letting me be the goofball that I am at times.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Overview

Anybody who has watched the movie Minority Report would have been struck by the futuristic nature of the displays that are shown. The images are formed on a transparent display and respond to a user's every touch and movement [1]. To arrive at such displays two critical components are required – a transparent light source and a transparent circuitry to control the pixel elements of the display. This monolithic integration of display driver circuits as well as other peripheral functions on the active matrix substrate leads to system-on-panel displays as portrayed in the movie. Such a display can be deployed virtually anywhere a sheet a glass is present, such as the windscreen of a car. With the recent advent of transparent oxide semiconductors this futuristic idea is one step closer to being realized.

Oxide thin films, with degenerate doping, have been utilized as passive elements with high conductivity and transparency for over half a century [2]. However, with the demonstration of the transparent thin-film transistor (TTFT) in 2003 using ZnO as the active layer [3-5], there has been a paradigm shift and this marked the inception of transparent electronics. Several metal oxides have started to be considered for their semiconducting properties and are identified as transparent oxide semiconductors (TOS) [6]. In 1996, Hosono *et al.* [7] reported on a new class of inorganic oxides based on multi-component combinations of heavy-metal cations with an outside shell electronic configuration of $(n-1)d^{10}ns^{0}$ $(n > 4)$. Apart from their visible transparency, the most attractive characteristic of these oxides is their relatively high mobility even in their amorphous state. A unique feature of TOSs is that the mobility is immune to structural disorder and amorphous TOSs still display considerable carrier mobility comparable to their crystalline counterparts. For instance, the mobility of single crystal silicon is ~ 2-3 orders of magnitude higher than that of

amorphous silicon (a-Si:H). Hence these TOSs, in their amorphous form, are referred to amorphous oxide semiconductors (AOS). Typically AOSs mobilities are an order of magnitude larger than that of a-Si:H.

Currently for large area applications such as the displays mentioned before, hydrogenated amorphous silicon (a-Si:H) introduced by Spear and LeComber is the material of choice to create circuit functionality [8]. However, a-Si:H inherently possess several drawbacks, such as low carrier mobility ~ 1 $cm^2 V^{-1} s^{-1}$, relatively poor stability, opacity, sensitivity to light, etc. The low mobility degrades the drive current capability and the frequency performance of the a-Si:H thin film transistor (TFT). Nevertheless, a-Si:H TFTs are widely used as high dynamic range voltage-controlled switches in active-matrix liquid-crystal displays (AMLCDs) and have been researched over the past three decades. AOS-based TTFTs have the potential to replace a-Si:H TFTs. Compared with their silicon and organic counterparts, AOS TFTs have much higher field-effect mobility, leading to a higher drain current density. Furthermore, low temperature process and the amorphous nature render AOS TFTs compatible with future generation of large area electronics that require flexible substrates.

Current research focuses on material development, exploring both HMC's and amorphous multicomponent heavy metal cation (a-MHMC) oxides for transparent channel material applications [9]. Research within this area of oxide electronics has burgeoned in recent years, and several companies have started the commercialization of oxide-based electronics for use in display technology [10,11]. The primary focus of these reports is the process optimization of the oxide semiconductor for use in TFTs [12]. Additionally, there are a few reports, which have used oxide-based electronics as switches for organic light emitting diode (OLED) and E-ink displays [13]. Functional TFTs have also been fabricated on plastic substrates for flexible electronic applications [14]. Furthermore, issues such as contact resistance, light sensitivity, short channel effects, and bias stress stability have been investigated [14, 15-17].

Apart from applications as display switching elements, other applications for oxide TFTs have been suggested. The higher current density provided by AOS TFTs make them well suited for driver transistors in current-driven OLED displays [18]. Oxide semiconductors can

show sensitivity to specific gases or humidity, which can open up new sensor based applications [19,20]. There have been claims about the suitability of oxide-based TFTs for sense and control elements for high-density memory applications [16].

1.2 Research objective and Dissertation organization

Though there has been a strong interest in amorphous oxide semiconductors, AOS based technology is still in the nascent stage. Like any new field, the advancement and successful implementation of transparent electronic applications would largely depend on the comprehensive understanding of AOS physics and chemistry, material and device processing issues and device physics. The primary goal of this dissertation is to develop indium gallium zinc oxide (IGZO) AOS thin films by the pulsed laser deposition process and to identify the dominant process and device parameters, which affect the IGZO TFT performance. Other important criteria such as device stability and dynamic characteristics have not been well addressed for AOS TFTs. In this dissertation electrical device stability and the dynamic behavior of IGZO TFTs are determined by fabricating ring oscillators and active matrix switching elements. Additionally, a non-volatile memory element for system-on-panel applications has been developed using the IGZO TFTs.

The structure of the dissertation is as follows. Chapter 2 gives a brief review of the pertinent literature related to amorphous oxide semiconductors. Description of thin film transistor device physics and device operation is discussed to provide the background for the experimental work presented in this dissertation. Chapter 3 provides a description of the various fabrication (and characterization) tools and techniques employed, followed by a discussion on the relevant electrical TFT characterization methodology and figures-of-merit. Chapter 4 presents the influence of several deposition parameters for IGZO thin films in addition to TFT device development, fabrication, and characterization. The effects of process parameters, such as the oxygen partial pressure and the thickness of the semiconductor layer, the choice of the gate dielectric material and the device channel length on the electrical characteristics of the TFTs are explored. Chapter 5 describes the evaluation of IGZO TFT electrical stability under a constant gate voltage stress. The behavior is modeled using a

charge trapping/tunneling mechanism at the semiconductor/dielectric interface. Chapter 6 describes the development of a non-volatile memory element based on the IGZO TFT. Memory characterization such as, programming, erasing and charge retention are elaborated as well. Chapter 7 reports preliminary results for IGZO based integrated circuits. Fabrication and characterization of inverters, ring oscillators and switching transistors for an active matrix pixel element are presented. Finally, Chapter 8 concludes by highlighting the salient results of the research presented in the dissertation and points out suggestions for future work..

CHAPTER 2

OXIDE SEMICONDUCTORS AND THIN-FILM TRANSISTORS

This chapter introduces the application of oxides in electronics followed by a brief discussion of transparent conducting oxides. Amorphous oxide semiconductors (AOS) are explored with the morphology and properties of indium gallium zinc oxide (IGZO) discussed in more detail since they are extensively used in this work. An introduction to thin film transistor structure and behavior is given. An overview of the research carried out on oxide semiconductor based thin film transistors is briefly reviewed, given that the thrust of this work is on devices.

2.1 Oxides in Electronics

Oxides are thermodynamic stable form of materials in standard ambient conditions. Metal oxides have traditionally been and still are used as heat resistant structural materials in addition to being used as raw materials for extraction of metals. The ancient knowledge about the transparency in silica and magnetism in magnetite has been augmented with a growing interest in the functional properties of oxides since mid-20^{th} century. Recent advances in understanding the chemistry and the physics of the metal oxide systems has led to the exploitation of new electronic and chemical properties present in these oxides [21]. Applications that oxides have been studied for include, semiconducting sensors, ferroelectrics, superconductors, micro and optoelectronic devices, transparent conductors, magneto-optics and spintronics [22].

Oxides are a ubiquitous part of electronics. The major advances in microelectronics in the 20^{th} century have been primarily due to silicon and its innate oxide, SiO_2. The desire to make smaller and faster devices (Moore's law) for nanoscale logic and memory devices, led to high-*k* dielectrics (such as HfO_2, ZrO_2 etc.) being investigated as a replacement for the SiO_2

insulator [23]. Oxides have also been considered for active electronic materials. At present there is considerable interest in ferroelectric thin films based on $PbZrTiO_3$ and $BaSrTiO_3$ for applications in non-volatile data storage [24]. Magneto-optic and spin electronic devices have been reported in Mn, Co doped ZnO, TiO_2 and SnO_2 [25]. Oxide-based thin-films and hetero-structures are attractive for optoelectronic devices. ZnO and ZnMgO heterostructures have been utilized as UV photodetectors [26,27]. ZnO-based light emitting diodes (LED) have been studied. P-type oxide semiconductors have been used to obtain current-injection excitonic blue emission from an all-oxide LED structure [28].

The wide band gap of oxides makes them transparent to visible light, but transparent conducting oxides (TCO) provide additional functionality. TCOs have been used in electronic devices and their applications have been limited to passive components such as window electrodes and electrical interconnections in solar cells and flat-panel displays [29]. Lack of active devices such as p-n junction diodes had been due to the absence of p-type TCO. But recently Cu^+-bearing oxides such as $CuGaO_2$ and $SrCu_2O_2$ have led to the development of p-n diodes [30]. In this dissertation the focus will be on unipolar devices based on n-type transparent conducting oxides.

2.2 Transparent conducting oxides

Transparent conducting oxides (TCO) belong to a class of oxides that exhibit high conductivity as well as a large band gap ($E_{GAP} > 3.1$ eV) due to the large electronegativity of oxygen, making them highly transparent in the optical portion of the electromagnetic spectrum. TCO characteristics were first observed in 1907 with cadmium oxide and since then several other TCOs have been used for their optical and electrical properties, such as tin oxide (SnO_2), indium oxide (In_2O_3) and zinc oxide (ZnO).

TCOs are degenerately doped to achieve high conductivity. In these materials, n-type conduction can be achieved from two sources: extrinsic substitutional doping (typically on the cation site) or the creation of point defects (such as oxygen vacancies and/or metal interstitials). In indium oxide, the point defects are due to either oxygen vacancies or indium

interstitials. Generation of free electrons, by the creation of oxygen vacancies is described as follows [31],

$$2In_{In} + 3O_O \rightarrow 2In_{In} + 3V_O^{\bullet\bullet} + 6e^- + 3/2O_2 \qquad (2.1)$$

where In_{In} and O_O denote neutral indium and oxygen atoms at the fixed positions, respectively, $V_O^{\bullet\bullet}$ represents an oxygen vacancy with positive divalent charge, e^- an electron with a negative univalent charge, and O_2 denotes gaseous oxygen. An excess of indium atoms at an interstitial site in In_2O_3 can also contribute to the generation of conduction electrons and can be described as,

$$2In_{In} + 3O_O \rightarrow 2In_i^{+x} + 2xe^| + 3O_O \qquad (2.2)$$

where In_i^{+x} denotes interstitial indium, In_i, with positive charge of *x*. Ovadyahu *et al*. also describe the existence of indium atoms with different valences [32]. Indium oxide can also be extrinsically doped, typically with a tin ion on an indium site (In_2O_3:Sn). In this case, a 4^+ tin sits on a 3^+ site, resulting in one additional electron in the conduction band and a localized 1^+ site. A similar behavior is seen in aluminum-doped zinc oxide [33]. Point defect concentrations can also be modified during the deposition process by appropriate selection of processing parameters or by subjecting the sample to an oxidizing or reducing post-deposition anneal.

Bellingham *et al*. have estimated the minimum theoretical resistivity limit for n-type TCOs as 4 x 10^{-5} Ω cm [34]. They arrive at this limit by taking into account the carrier transport in the film, which is constrained by ionized impurity scattering (μ < 90 $cm^2 V^{-1} s^{-1}$) and the carrier concentration limitations due to increasing optical reflection with increasing carrier concentration (n < 2 x 10^{21} cm^{-3} for > 90% optical transmission). Experimental results for single crystal tin doped indium oxide (In_2O_3:Sn) – minimum resistivity of ~ 7.7 x 10^{-5} Ω cm (μ = 42 $cm^2V^{-1}s^{-1}$, n = 1.9 x 10^{21} cm^{-3}) indicate that the predicted theoretical resistivity limit is fairly accurate.

TCOs are currently utilized in a number of passive applications, including thin-film solar cells and flat-panel displays. Of the commercially available TCOs, In_2O_3:Sn is the most conductive. But due to the limited availability and high cost of indium other TCOs are being

investigated [35]. Among the materials being explored is ZnO:Al, which is attractive for its ease of etchability, stability in a hydrogen plasma, and low process temperature requirement [36].

2.3 Amorphous oxide semiconductors

Since the pioneering work of Denton *et al*. in 1954, the electrical properties of amorphous and semiconductive oxide materials based on transition metals have been known [37]. Of this family, V_2O_5-based amorphous materials have been most extensively studied [38]. The mobility of electrons in these amorphous oxide semiconductors is of the order of 10^{-4} cm^2 V^{-1} s^{-1} at room temperature. Such a low mobility and intense coloring due to *d-d* absorptions of transition metal ions makes it unsuitable as a transparent semiconducting oxide.

In 1995, Yasukawa *et al*. reported on a novel transparent and conductive, n-type amorphous $AgSbO_3$ thin film [39]. The electrical conductivity of the sputter-deposited film at ~ 300 K was increased by four orders of magnitude from ~ 10^{-5} S cm^{-2} to ~ 10^{-1} S cm^{-2} when the as-deposited films were heated at 500 °C. Upon heating, the film remained amorphous and carrier electrons were generated through the formation of oxygen vacancies and the mobility observed went up to ~ 7 cm^2 V^{-1} s^{-1} at room temperature. Another interesting observation was that the mobility is almost the same as that in polycrystalline $AgSbO_3$, obtained by crystallization of the amorphous film. Similar results with other material systems Cd_2GeO_4, $CdPbO_5$, and $MgIn_20_7$ led to new classification of the high mobility amorphous oxides called amorphous oxide semiconductors (AOS) [40-42].

Hosono *et al*. propose a theory to explain the dramatic differences seen in the electronic and optical properties of traditional amorphous semiconductors and AOS [43,5]. In contrast to covalent semiconductors, oxide semiconductors are ionic in nature and the conduction band minimum (CBM) and the valence band maximum (VBM) are formed by different ionic species. When metal atoms and oxygen atoms come close, due to the large differences in the electron affinity and ionization potential, charge transfer takes place ionizing the atoms and leading to electrostatic separation of the anionic and cationic sites. This leads to the CBMs

being primarily composed of metal cations and the VBMs composed of oxygen *2p* orbitals in most oxides although this does not hold for lanthanide and actinides and transition metal oxides. A large bandgap in oxides is attained by the low energy of the oxygen *2p* orbitals leading to transparency.

It has been proposed [43] that metal oxides composed of heavy metal cations (HMC) with an electronic configuration $(n\text{-}l)d^{10}ns^{0}$ where $4 \leq n \leq 6$ would lead to realizing high mobility in amorphous oxides. To achieve high mobility a continuous conduction path is required and hence a large overlap between relevant orbitals is essential. Moreover the magnitude of the overlap needs to be insensitive to the structural randomness, which is intrinsic to the amorphous state and HMCs satisfy both these requirements. The bottom part of the conduction band in these oxides is primarily composed of *ns* orbitals of the HMCs. Given the spatial spread of the *s* orbital is large than the inter-cationic distance (by selecting a suitable value of *n*), and owing to the spherical symmetry of the *s*-orbital, large overlap and insensitivity to the amorphous state is achieved.

As schematically shown in Figure 2-1(b), the spatial spreading of the *s*-orbital is considerable and the overlap between these *ns* orbitals with spherical symmetry is large and insensitive to any angular variation in the bonding angles compared with the cases of *p-p* or *d-p* orbitals having high spatial anisotropy. Figure 2-1(a) shows the spatial directivity of a typical covalent semiconductor having sp^3 orbitals. Owing to this arrangement, the amorphous state leads to highly strained chemical bonds, which leads to rather deep and high-density localized states below the CBM and above VBM, causing carrier trapping. This would also explain why amorphous semiconductors typically exhibit much deteriorated carrier transport properties compared to their crystalline counterparts as shown in a-Si:H and chalcogenides whereas the electron mobility of AOS is comparable to their corresponding crystalline counterparts.

The above electronic structure of AOS explains their peculiar properties not observed in conventional amorphous semiconductors. First, the electron mobilities ($10 – 40$ $cm^2 V^{-1} s^{-1}$) in AOS devices are relatively high, greater than a-Si:H by a factor > 10 and most organic semiconductors by a factor > 10^2. Second, a Hall sign anomaly is seen in conventional

amorphous semiconductors in which the sign of the Hall coefficient is different from that of the Seebeck coefficient [44]. This is presumably due to the short carrier mean free paths, which invalidates assumptions made in the Boltzmann transport equations [45]. In AOS, the Hall coefficient matches that of the Seebeck coefficient, which indicates that the length of the electron mean free path is longer translating to larger mobilities. Third, it is possible to dope AOS degenerately whereas this is not possible in conventional amorphous semiconductors.

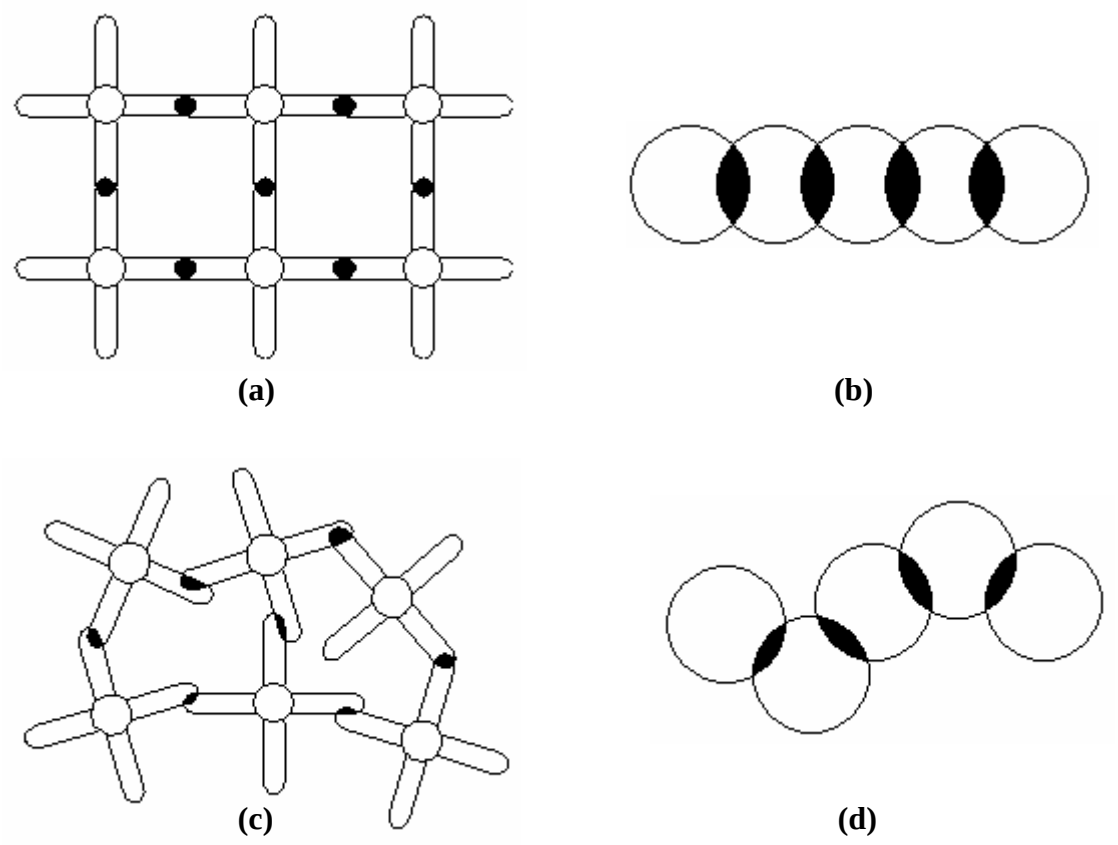

Figure 2-1: Comparison of atomic orbital overlap for covalent semiconductors (a, c) and oxide semiconductors (b, d) in both crystalline and amorphous configurations. The conduction band of covalent semiconductors consists of highly directional sp^3 hybrid orbitals while the conduction band in oxide semiconductors is composed of large isotropic s orbitals. The direct measure of the mobility is the amount of overlap between neighboring atomic orbitals. Hence, when a covalent semiconductor is in an amorphous state (c) there is a substantial decrease in carrier mobility when compared to its crystalline counterpart (a) and in oxide semiconductors, the overlap is relatively unchanged between the crystalline (b) and amorphous (d) configurations. Schematic based on [43].

Carrier conduction is conventional amorphous semiconductors takes place by hopping between tail states within the band gap of the semiconductor where the Fermi level is pinned leading to lower mobilities [44]. In contrast, with appropriate doping or via application of a gate bias in a thin film transistor structure, the Fermi level of AOS can be moved into the conduction band, resulting in degenerate or band conduction. Table 2-1 lists some of the properties that differentiate the two classes of amorphous semiconductors.

Table 2-1: Comparison of the characteristics of conventional amorphous semiconductor and AOSs.

	Conventional Amorphous Semiconductors (e.g. a:Si-H)	**Amorphous Oxide Semiconductors**
Mobililty	1-2 $cm^2 V^{-1} sec^{-1}$	10-60 $cm^2 V^{-1} sec^{-1}$
Chemical Bonding	Covalent	Ionic
Conduction Mechanism	Hopping	Band Conduction
Doping degenerately	Not possible	Possible

Primarily TCO are based on heavy metal cations similar to AOS but are degenerately doped to achieve high conductivity. By achieving well-controlled and low carrier concentration active transparent devices, namely transistors, can be made using oxide semiconductors. Several AOS including, indium gallium zinc oxide (IGZO), have been proposed for application as the channel material for thin film transistors [46-55].

2.3.1 Indium gallium zinc oxide

Indium gallium zinc oxide (IGZO) is a wide band gap (~ 3.5 eV), n-type semiconductor containing three component oxides, In_2O_3, Ga_2O_3 and ZnO whose stoichiometry can be generally described as $In_{2x}Ga_{2-2x}Zn_kO_{k+3}$, where $0 < x < 1$ and k is an integer greater than 0. Bulk samples with different stoichiometry (both x and k) of IGZO have been synthesized to study the solubility limits of the components [56,57]. Interestingly, it is seen that regardless

of k, when $x = 0.5$, i.e. equal proportions of In and Ga, the structure of the compound is preserved. Single crystal indium gallium zinc oxide is composed of alternating layers of InO_2^- and $GaZnO_4^+$; the In^{3+} ion has octahedral coordination, the Ga^{3+} ion has pentagonal coordination, and the Zn^{2+} has tetragonal coordination.

For $k \leq 3$ the conductivity decreases as k increases which is observed in both thin film [57] and bulk samples [58]. This trend indicates that the conductivity of indium gallium zinc oxide is primarily associated with the In *5s* states. However, for $k \geq 4$, the fraction of Zn becomes increasingly large and Zn begins to contribute to conduction [58]. The ionic radii of Ga, In, and Zn are 1.27, 1.49, and 1.54 Å, respectively. If orbital overlap interaction is considered, and since the ionic radii of In and Zn are similar, the shift in conduction path as the fraction of Zn becomes large is evident. Indium contributes to the large spreading of the CBM. Another way to form greatly dispersed CBM is found in ZnO: a small Zn–Zn distance, due to fourfold coordination, increases CBM dispersion and results in high electron mobility [59]. Gallium oxide, which has a strong metal–oxygen bond is used to suppress the generation of free carriers via the formation of oxygen vacancies. In fact Ga^{3+} has two effects, first the introduction of aliovalent different-sized cations enhances amorphization and second, owing to the stronger Ga-O chemical bonds, compared to Zn-O and In-O, the generation of free carriers is suppressed [59].

Extended x-ray absorption fine structure (EXAFS), which is commonly employed to evaluate short-range order in materials, was used to examine the structure of both single crystal and amorphous IGZO thin films [60]. The nearest-neighbor distances for In-O, Ga-O, and Zn-O in the amorphous film are 0.211, 0.200, and 0.195 nm, respectively. This short range ordering is similar to that of the single crystal structure (0.218, 0.193, and 0.193, respectively). However, it appears that medium range ordering (second nearest-neighbor distances) near the Ga and Zn ions is lost in the amorphous films. *Ab initio* calculations were performed and are in good agreement with the EXAFS results. From the experimental and calculated results, the coordination numbers of In-O, Ga-O, and Zn-O are deduced to be 5, 5, and 4, respectively. Also, pseudoband calculations show that the conduction band minimum is composed of In *5s* [60].

Nomura *et al*. also calculate the amorphous IGZO band structure and found that the effective mass is small, about 0.2 m_e accounting for the high mobility and they conclude that no localized states exist near the conduction band, unlike a-Si:H. Hence the dominant conduction mechanism in IGZO is not variable range hopping (VRH), i.e. quantum mechanical hopping via band-tail states. However, the $T^{-1/4}$ temperature dependence of the conductivity seen in IGZO for non-degenerate doping is the same relationship seen in VRH. Nomura *et al*. explained the similarity by employing a percolation mechanism, which also has a $T^{-1/4}$ temperature dependence of conductivity [61].

2.4 Thin film transistors (TFT)

Thin film transistors (TFT) are a class of field effect devices in which the current through the device is modulated on the same basic principle as the MOS transistor. But unlike the MOS transistor where the substrate material is typically the semiconductor, thin films of the semiconductor material are deposited on a substrate to fabricate TFTs [62]. Though J. E. Lilienfeld is often credited for the invention of the TFT [63], the development of the first TFT as it is known today has been credited to P. K. Weimer [64]. Since Weimer's initial work, which involved CdS as the channel material, the TFT structure, fabrication, integration and material systems employed have undergone extensive evolution, development and refinement. TFTs have been made using CdS, CdSe, hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) as the channel material. The most widely used application of TFTs is as switching transistors for active matrix liquid crystal displays (AMLCD) and the channel material of choice is a-Si:H followed by poly-Si. The typical characteristics of these technologies are mobilities in the range for 0.5 – 1.0 $cm^2 V^{-1} s^{-1}$ and 10 – 80 $cm^2 V^{-1} s^{-1}$ for a-Si:H, and poly-Si with maximum processing temperatures around 300 °C and 500 – 600 °C, respectively [65].

In addition to silicon or inorganic TFTs another class of TFTs consists of those which employ organic materials as the channel layer [66]. Though these materials exhibit relatively low mobilities ~ 10^{-3} – 1 $cm^2 V^{-1} s^{-1}$, it is offset by the low cost of fabrication, such as spin

coating and printing. Moreover, the processing temperature of these devices is typically below 300 °C, allowing for deposition onto plastic substrates. A large number of these organic channel materials are p-type. However, n-type and recently ambipolar TFT have been demonstrated using organic channel layers [67]. In the following subsections, a brief description of the TFT device structures and basic device operation is given.

2.4.1 Device structures

Thin film transistor structures are usually categorized as co-planar or staggered. They can further be classified as either as bottom-gate or top-gate devices. Figure 2-2 shows the four possible device structures. The basic differences are in the relative position of the gate, source/drain, the semiconductor and the insulator. A staggered TFT structure has the gate and source/drain contacts on opposite sides of the semiconductor and hence there is no direct connection with the induced channel in the semiconductor. This arrangement provides a large contact area for the source/drain contacts for charge injection. On the other hand, the co-planar TFT structure has the gate and source/drain contacts on the same side of the semiconductor. This configuration leads to the source/drain contacts to be in direct contact with the induced channel.

In bottom-gate or inverted TFT structure the gate electrode and the gate insulator are present beneath the semiconductor, which leads to the top surface of the semiconductor to be exposed to atmosphere. In a top-gate TFT structure the gate electrode and the insulator are present on top of the semiconductor. In this configuration the semiconductor is covered by the insulator and hence the surface is inherently passivated.

Process flow and process integration related issues can also determine the right kind of TFT structure for the application. In the co-planar top-gate structure, the semiconductor is deposited first. Therefore, the maximum semiconductor processing temperature is limited only by the semiconductor and the substrate. Also, in both the top-gate structures the insulator is deposited after the semiconductor layer. This implies that during the insulator deposition care must be taken to avoid damage of the semiconductor close to the interface

where the channel will be formed. A bottom-gate structure would possibly reduce such issues where the insulator is deposited before the semiconductor. The co-planar structure is difficult to realize in some technologies, such as a-Si:H. Typically staggered structure is usually adopted in the fabrication of amorphous silicon TFT while co-planar structure is usually adopted in the polycrystalline silicon TFT [62]. The staggered bottom-gate TFT is widely used in the manufacturing of active-matrix LCD back panes [62]. Various factors including processing temperature and sequence plays a role in determining the final TFT structure utilized.

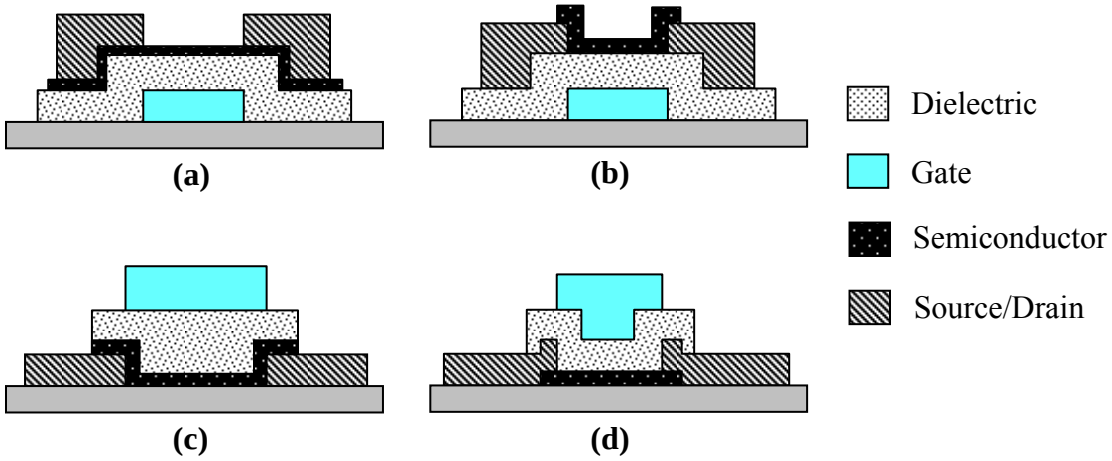

Figure 2-2: The four basic TFT structures: (a) staggered bottom-gate, (b) co-planar bottom-gate, (c) staggered top-gate, and (d) co-planar top-gate.

2.4.2 Basic device operation

In this discussion an *n*-channel accumulation mode TFT is assumed. A similar treatment can be extended to *p*-channel TFT. Figure 2-3 represents the structure and the energy band diagram of the *n*-channel TFT. Note that the semiconductor layer is slightly *n*-type. Figure 2-3(b) is the idealized case with the semiconductor and gate electrode having the same work function. Now let us consider two biasing conditions, $V_{GS} > 0$ and $V_{GS} < 0$. When a positive bias ($V_{GS} > 0$) is applied to the gate, the voltage is dropped across the insulator and the semiconductor causing the bands to bend downwards, as in Figure 2-3(c), and delocalized electrons to accumulate, forming the channel near the semiconductor/dielectric interface. If a

positive voltage is applied to the drain electrode ($V_{DS} > 0$) electrons are injected from the source electrode into the channel and a current flows between the drain and the source electrode. This current can be modulated by changing the gate voltage, which modulates the conductivity of the channel by increasing the degree of band bending in the semiconductor.

On the other hand, when a negative bias ($V_{GS} < 0$) is applied to the gate, the opposite band bending in the semiconductor occurs, leading to depletion of carriers at the insulator/semiconductor interface. As the magnitude of the negative gate bias increases the depletion region grows further into the semiconductor layer until eventually the entire thickness of the semiconductor can be depleted. In this condition, the channel is not formed and even a potential across the source and drain does not induce a current as in Figure 2-3(d).

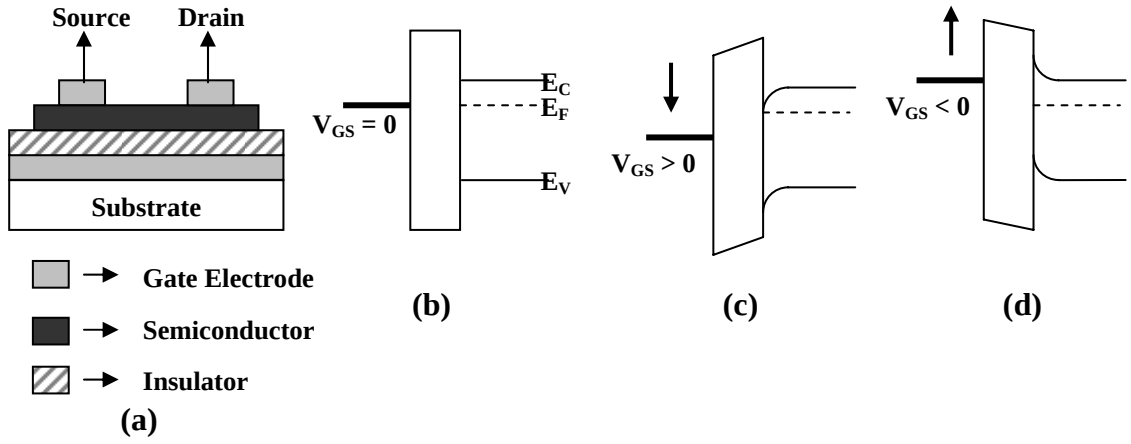

Figure 2-3: (a) Staggered bottom-gate TFT structure (b) the idealized energy band diagrams of the gate, insulator and n-type semiconductor in equilibrium ($V_{GS} = 0$), (c) a positive bias applied to the gate electrode ($V_{GS} > 0$) (d) a negative bias applied to the gate electrode ($V_{GS} < 0$).

As mentioned earlier a positive drain bias (V_{DS}) produces current when $V_{GS} > 0$. Two bias conditions are depicted in Figure 2-4. Figure 2-4(b) depicts a device when biased with a low V_{DS}. This is called the 'linear' regime of device operation where the drain current increases linearly with respect to V_{DS} (for a given V_{GS}), i.e. the channel acts like a resistor. The channel charge density is fairly uniform from the source to the drain as seen in Figure 2-4(b). The channel resistance depends on the accumulation channel sheet charge density, which is a function of the bias applied on the gate (V_{GS}).

When a significantly high V_{DS} is applied, the device enters the 'saturation' regime of operation. In this regime the drain current remains constant with further increases in V_{DS}. The large drain voltage causes the channel to be fully depleted near the drain as shown in Figure 2-4(c). This is called the pinch-off condition and the drain voltage at which this occurs is called the pinch-off voltage, $V_{pinch\text{-}off}$.

A quantitative formulation of the ideal TFT operation has been derived using the square-law theory and summarized below [68]. The equations for both the linear and saturation regions of operation are given as,

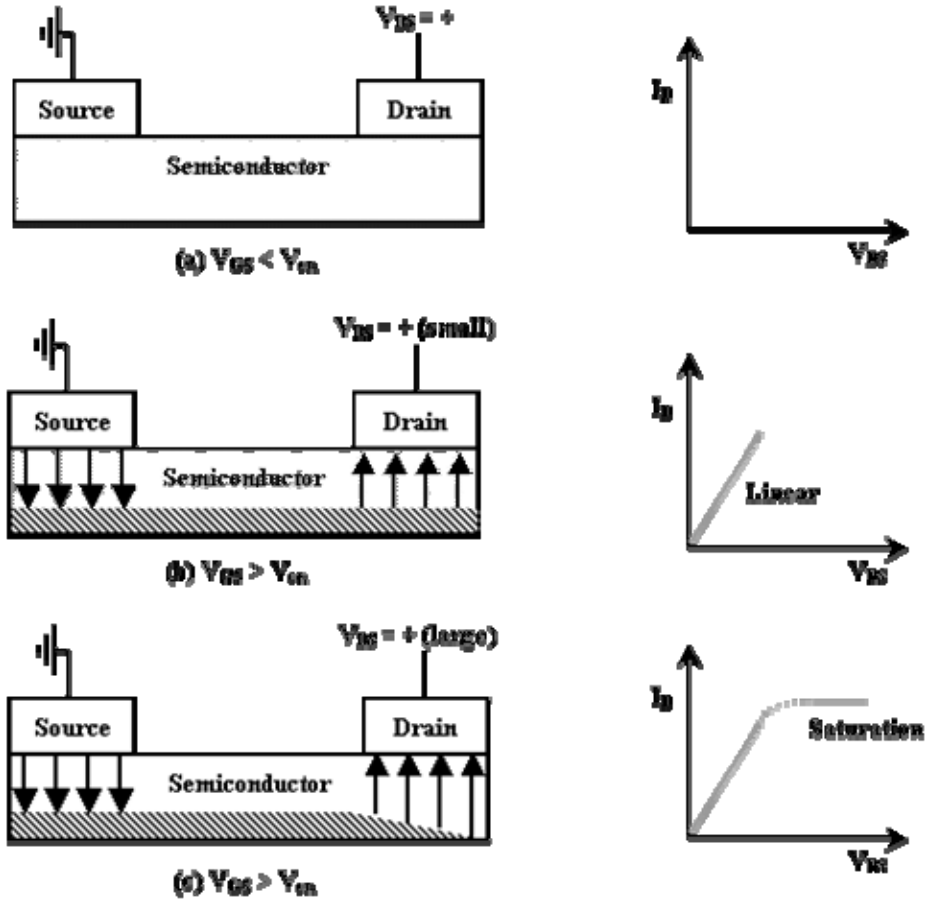

Figure 2-4: Ideal n-channel thin-film transistor operation. The shaded region is the channel layer due to electron accumulation, which is not formed below cut-off, i.e. $V_{GS} < V_{on}$ (a). At low V_{DS} ($V_{DS} << V_{GS} - V_{on}$) the channel formed at the semiconductor/dielectric interface is uniform from the source to drain and the drain current varies linearly with V_{DS} – linear regime (b). When $V_{DS} \geq V_{GS} - V_{on}$ the channel is 'pinched off' leading to I_D being saturated with respect to V_{DS} – saturation regime. Schematic based on [68].

$$I_D = \frac{W}{L}\mu C_{di}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \rightarrow \quad \text{linear} : V_{DS} \le V_{GS} - V_T \qquad (2.3)$$

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{di}(V_{GS} - V_T)^2 \quad \rightarrow \quad \text{saturation} : V_{DS} > V_{GS} - V_T \qquad (2.4)$$

It has been argued that [69] Eqns. (2.3) and (2.4) are more suitable for field effect devices such as MOSFETs, while the equations below are more apt for TFTs due to its characteristics.

$$I_D = \frac{W}{L}\mu(V_{GS})C_{di}\left[(V_{GS} - V_{on})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \rightarrow \quad \text{linear} : V_{DS} \le V_{GS} - V_{on} \qquad (2.5)$$

$$I_D = \frac{1}{2}\frac{W}{L}\mu(V_{GS})C_{di}(V_{GS} - V_{on})^2 \quad \rightarrow \quad \text{saturation} : V_{DS} > V_{GS} - V_{on} \qquad (2.6)$$

the differences between Eqns. (2.3), (2.4) and Eqns. (2.5), (2.6) are the replacement of V_T with V_{on} and that the gate bias dependence of channel mobility has been introduced. These features will be further discussed in detail in Section 3.7.3.2.

As previously mentioned, by applying a negative bias the channel can be depleted of carriers. The depletion width is the function of the applied gate bias and is given by [70],

$$W = \frac{\varepsilon_s}{C_{di}}\left[\left(1 + \frac{2C_{di}^2 V_G}{qN_D\varepsilon_s}\right)^{1/2} - 1\right] \qquad (2.7)$$

where ε_s is the semiconductor permittivity, N_D is the intrinsic semiconductor carrier density. The intrinsic carrier density is responsible for any background current condition and to minimize this the semiconductor needs to be fully depleted. This implies that the carrier density in the semiconductor needs to be minimized or for a given N_D the thickness of the semiconductor can be varied to bring about full depletion of the channel.

The discussion so far has been pertaining to an ideal TFT behavior, while several non-idealities might be present and need to be suitably accounted for to model the TFT behavior accurately. These include, but are not limited to, traps (acceptor or donor type) at the semiconductor/insulator interface or in the semiconductor, subthreshold conduction, interface

roughness, series resistance of contacts, conductive channel, channel length modulation, gate leakage etc.

2.5 Oxide semiconductor based thin film transistors and applications

Since zinc oxide based thin film transistors were first demonstrated in 2003 [3-5], a large variety of n-type oxide semiconductors have been utilized as channel materials. Channel materials based on single component oxides, such as ZnO, In_2O_3, SnO_2, and Ga_2O_3 and multi-component oxides, such as zinc tin oxide (ZTO) [46-48], indium gallium oxide (IGO) [51,52], zinc indium oxide (ZIO) [49,50], and indium gallium zinc oxide (IGZO) [52-55] have been reported. The majority of the research is on discrete TFT performance but there are few reports on oxide semiconductor based circuits and integration with several display applications as well. The techniques to form the semiconducting channels range from, RF sputtering [5], ion beam sputtering [4], solution-based deposition [71], atomic layer deposition (ALD) [72], metal-organic chemical vapor deposition (MOCVD) [73], and pulsed laser deposition (PLD) [3,74]. In the next section, single component oxides, and IGZO have been emphasized. A brief description of some of the circuit applications is discussed as well. References are provided for the rest of the oxide semiconductor based research for additional information.

2.5.1 TFTs with single component oxide channel: ZnO

The first reports on oxide semiconductor TFTs were based on zinc oxide (ZnO). Demonstration of ZnO-based TFTs by Masuda *et al*. [3], Hoffman *et al*. [4] and Carcia *et al*. [5] in 2003 started the currently expanding research on oxide based transparent TFTs. Before the multi-component oxides were introduced as viable candidates for TFT channel application, ZnO was the most widely researched oxide semiconductor.

Masuda *et al*. used PLD ZnO to fabricate bottom-gate TFTs. The ZnO layer was deposited at 450 °C with a double layer gate insulator consisting of SiO_2 and SiN_x used to

suppress leakage current. The I_{on}/I_{off} ratio was 10^5 with a threshold voltage of 2.5 V and a field effect mobility of 0.03 $cm^2 V^{-1} s^{-1}$. Hoffman *et al*. fabricated ZnO TFTs using ion beam sputtering. The resistivity of the channel was increased by a rapid thermal annealing step, 600 – 800 °C in O_2. Enhancement-mode TFT operation with an I_{on}/I_{off} ratio of ~ 10^7 was achieved. Threshold voltages and channel mobilities of devices were10 to 20 V and 0.3 to 2.5 $cm^2 V^{-1} s^{-1}$, respectively. Carcia *et al*. reported on a room temperature process to fabricate rf magnetron sputtered ZnO TFTs on glass substrates.

More recently, several other authors have explored ZnO-based TFTs with RF sputtering that do not require intentional post-deposition annealing treatments. Fortunato *et al*. [75] and Carcia *et al*. [76] use different deposition parameters of pressure and power to achieve high performance ZnO TFTs. The electrical properties of ZnO-based TFTs are shown to be strongly influenced by the O_2 partial pressure in the deposition ambient. TFTs with mobilities approaching 25 $cm^2 V^{-1} s^{-1}$ were demonstrated. Additionally, ZnO-based TFTs on flexible polyimide substrates were also demonstrated [76].

Solution-based deposition techniques, such as spin coating and chemical bath deposition have been used to fabricate ZnO-based TFTs [77-79]. A high temperature post-deposition anneal is usually employed to achieve adequate crystallization and to drive away volatile components in spin-coated samples. This also enhances the device performance of the TFTs. Norris *et al*. spin a zinc nitrate and glycine precursor solution and anneal at 700 °C. The channel mobility and I_{on}/I_{off} of these devices are 0.2 $cm^2 V^{-1} s^{-1}$ and 10^7, respectively [77]. Li *et al*. use a precursor solution with zinc acetate dihydrate, 2-ethanolamine and methoxyethanol and optimize the respective ratios to get high performance ZnO TFTs. TFTs annealed at 400 – 500 °C exhibited channel mobilities, threshold voltages, and I_{on}/I_{off} ratios of 5-6 $cm^2V^{-1}s^{-1}$, 20 V, and 10^5, respectively [78]. Cheng *et al*. utilize a chemical bath containing zinc nitrate and dimethylamineborane at 60 °C to grow ZnO films. TFTs fabricated with these films exhibited channel mobilities and and I_{on}/I_{off} ratios 0.25 $cm^2 V^{-1} s^{-1}$ and 10^5, respectively [79].

MOCVD has been recently used to deposit ZnO for TFT applications. Zhu *et al*. grew ZnO at 400 – 500 °C using MOCVD, SiO_2 was used as the gate dielectric and achieved

depletion mode devices. ZnO grown on glass has an $I_{on}/I_{off} \sim 10^4$ and a field effect mobility of 4.0 $cm^2 V^{-1} s^{-1}$. ZnO grown epitaxially on r-Al_2O_3 substrate yielded TFTs with field effect mobility ~ 35 $cm^2 V^{-1} s^{-1}$ and I_{on}/I_{off} ratio of 10^8 [80]. Jo *et al*. fabricated ZnO TFTs, which were depletion mode and attributed it to the oxygen deficiencies during the deposition process [81]. By allowing sufficient oxidation time during growth, enhancement mode devices with 15 $cm^2 V^{-1} s^{-1}$ mobility and $I_{on}/I_{off} \sim 10^7$, and a 5 V threshold voltage were realized. Levy *et al*. report on the fabrication of the gate dielectric and semiconductor layer via ALD [82]. Zinc oxide TFTs are fabricated with temperatures below 200 °C, exhibiting mobilities as high as 20 $cm^2 V^{-1} s^{-1}$ and no visible hysteresis.

Hossain *et al.* [83] and Hoffman [69] have made contributions towards enhancing the understanding of oxide-based TFT operation. Hossain *et al.* analyze grain boundary effects for polycrystalline ZnO TFTs. The simulations that are carried out show a decrease in grain boundary barrier height with increasing free carrier concentration and a decrease in channel mobility with an increase in the number of grain boundaries in the channel. Hoffman uses basic semiconductor physics to formulate mobility extraction methodologies suitable for TFTs and discusses mobility characteristics of ZnO TFTs. These mobility extraction methods are discussed in further detail in Section 3.7.3.3.

2.5.2 TFTs with single component oxide channel: In_2O_3, Ga_2O_3, SnO_2

In_2O_3 is not commonly employed as the TFT semiconductor layer due to the difficulty in controlling and reducing indium interstitials/oxygen vacancy formation in the films [84]. The propensity to form these defects leads to large carrier concentrations in the film, leading devices with highly negative threshold voltages (depletion mode). Wang *et al*. tackle this issue by utilizing an ion-assisted deposition process, and control the carrier concentration to 10^{17} to 10^{20} cm^{-3} in In_2O_3 films by adjusting the O_2 partial pressure and ion beam power. Using this technique, inorganic-organic hybrid In_2O_3-based TFTs with organic self-assembled dielectrics were fabricated. These hybrid TFTs show very large field effect mobility (~ 120 $cm^2 V^{-1} s^{-1}$), and a near-zero threshold voltage [84]. Other reports on ion-

assisted and reactive thermal evaporated In_2O_3 TFTs do not show promising device characteristics [85]. In_2O_3 nanowire (NW) TFTs have also been reported and will be discussed in Section 2.5.4.2.

Like In_2O_3, Ga_2O_3 is not commonly employed as a TFT semiconductor layer due to its low mobility values. Matsuzaki *et al*. report on polycrystalline PLD Ga_2O_3-based TFTs processed at 550 °C with field-effect mobilities of 0.05 $cm^2 V^{-1} s^{-1}$ with $I_{on}/I_{off} \sim 20$ and a threshold voltage ~ -6.7 V [86]. At higher processing temperatures, the field effect induced conduction of Ga_2O_3-based TFTs was lost indicating a high trap concentration. The small field-effect mobility is attributed to the granular structures of the film surface.

Tin oxide is unique, since both n-channel (SnO_2) [87] and p-channel (SnO) [88] TFTs have been reported. Presley *et al*. utilize extremely thin semiconductor layers (10-20 nm) to control the threshold voltage of SnO_2-based TFTs. The semiconducting layer was deposited using RF magnetron sputtering and rapid thermal annealed in O_2 at 600 °C to yield a field effect mobility ~ 2 $cm^2 V^{-1} s^{-1}$. Fully transparent SnO_2 NW TFTs have been reported by Dattoli *et al*. [89] and Ju *et al*. [90]. Field effect mobilities ~ 120 – 170 $cm^2 V^{-1} s^{-1}$ have been extracted. Recently Ogo *et al*. reported on a p-channel TFT based on PLD SnO [88]. Top-gated TFTs, using SnO channels grown epitaxially on yttria-stabilized zirconia substrates at 575 °C, exhibited field-effect mobilities of 1.3 $cm^2 V^{-1} s^{-1}$, I_{on}/I_{off} of 10^2, and a depletion mode device with threshold voltages of 4.8 V.

2.5.3 TFTs with multi component oxide channel: IGZO

Currently indium gallium zinc oxide (IGZO) is probably the most widely used channel material for oxide-semiconductor based TFT applications with a large number of reports in the literature. The very first report was in 2003 when Nomura *et al*. fabricated a transparent TFT based on a single crystal superlattice of $InGaO_3(ZnO)_5$ [91]. The IGZO channel was deposited by PLD on a single-crystal yttria stabilized zirconia substrate and annealed at 1400 °C to undergo a reactive solid-phase epitaxy process. These TFTs employ a coplanar top-gate structure with an 80 nm thick HfO_2 gate insulator. The TFTs exhibited a field-effect mobility

(μ_{FE}), a threshold voltage (V_T) and an I_{on}/I_{off} of 80 $cm^2 V^{-1} s^{-1}$, 3 V and 10^6, respectively. Following this report, in 2004, Nomura et al. demonstrated a flexible transparent TFT employing amorphous IGZO (a-IGZO) (with composition, In : Ga : Zn = 1 : 1 : 1 atomic ratio) as the channel material [43]. The TFT channel was deposited via PLD at room temperature onto polyethylene terephthalate substrates and the gate insulator was yttrium oxide. The TFTs showed a μ_{FE}, an I_{on}/I_{off} and a V_T of 6-9 $cm^2 V^{-1} s^{-1}$, 10^3 and 1.6 V, respectively. The device characteristics were found to be stable during repetitive bending of the substrate sheet. A follow up report on a similar structure showed improved mobilities and I_{on}/I_{off}, >10 $cm^2 V^{-1} s^{-1}$ and ~ 10^6, respectively [59].

Yabuta *et al*. explored amorphous IGZO-based ($InGaZnO_4$) TFTs with a staggered top-gate structure [53]. RF sputtering is used for deposition of the semiconductor and insulator (Y_2O_3) layers. While no intentional substrate heating is used, the maximum processing temperature is 140 °C due to heating from the sputtering process during insulator deposition. The channel mobility, V_T, and I_{on}/I_{off} are 12 $cm^2 V^{-1} s^{-1}$, 1 V, and 10^8, respectively.

Iwasaki *et al*. explored the compositional optimization of IGZO channel using a combinatorial approach with rf co-sputtering from three individual sources, ZnO, Ga_2O_3, and In_2O_3 [92]. A staggered bottom-gate structure was used and the range of compositional variation was 10 – 70% for each component. Iwasaki *et al*. indicate that the optimal O_2 partial pressure employed during deposition changes for different stoichiometries. Higher Ga content required a lower O_2 partial pressure; while higher In content required a higher O_2 partial pressure to produce functioning TFTs. Mobility is observed to be strongly related to the indium content of the film. The best TFT performance was achieved with a compositional ratio of In : Ga : Zn = 37 : 13 : 50. This ratio corresponds to a saturation mobility of 12 $cm^2 V^{-1} s^{-1}$, a V_T of 3 V, and an I_{on}/I_{off} ~ $7x10^7$. It is noted that the optimum composition for a specific application should be chosen after further study of long-term stability, process margins, and device specifications.

In 2007 Hayashi *et al.* reported on the fabrication of 96 TFTs in a 1x1 square inch with a pitch of 1 millimeter between transistors to investigate uniformity [93]. The TFT array is fabricated on thermally oxidized silicon by RF magnetron sputtering the IGZO layer and

patterning it with photolithography and wet etching. All the devices exhibited virtually identical transfer curves. Electrical performance includes an average saturation mobility of 14.55 ± 0.11 cm^2 V^{-1} s^{-1}, a V_T of 2.25 ± 0.13 V with an average subthreshold swing of 0.197 ± 0.006 V decade^{-1}, and an average V_{on} of -0.37 ± 0.13 V. They point out that the demonstration of uniformity is critical for the consideration of using AOS based TFTs in display applications.

Kumomi *et al.* explored the impact of several variables on TFT performance including the structure, oxygen partial pressure during deposition, and choice of materials for the gate insulator [10]. In every case, the IGZO layer is sputtered at room temperature in an Ar/O_2 atmosphere. The electrical conductivity of the sputtered film is controlled by varying the oxygen partial pressure – the conductivity decreases monotonically with increasing oxygen partial pressure. The choice of Y_2O_3 as a gate insulator lends itself to a top-gated transistor structure while thermal oxide is more suited for a bottom-gated structure owing to the roughness of each layer.

IGZO based TFT have been heavily researched by the corporate R&D department in Samsung SDI Company. They use a staggered bottom gate structure with patterned Mo metal as the gate electrode followed by a PECVD processed SiN_x, which acts as the gate insulator. The channel is RF sputtered in an Ar/O_2 atmosphere and the finished structures are annealed in nitrogen ~ 300 °C for 1 hr. Park *et al*. report on the effect of Ar plasma treatment on IGZO TFTs [94]. Before the source/drain metal (Pt/Ti) is deposited, the channel is subject to an Ar plasma for 30 s. This reduces the contact resistance between the Pt/Ti and IGZO channel. Without the treatment, TFTs exhibited a moderate μ_{FE} of 3.3 cm^2 V^{-1} s^{-1}, subthreshold swing, S, of 0.25 V decade^{-1}, and $I_{on}/I_{off} \sim 4\text{x}10^7$. After the Ar plasma treatment the device performance significantly improved, an S value of 0.19 V decade^{-1}, $I_{on}/I_{off} \sim 10^8$, as well as a μ_{FE} of 9.1 cm^{2}V^{-1}s^{-1}, were recorded. Kim *et al*. have demonstrated a passivated IGZO TFT utilizing a CVD SiO_2 as the passivation layer [95]. Devices with the passivation layer exhibited a μ_{FE} of 36 cm^2 V^{-1} s^{-1} and a V_{on} of 0 V, however devices without the passivation layer showed reduced performance due to damage during the source and drain patterning. The μ_{FE} reduced from 35.8 to 14.8 cm^2 V^{-1} s^{-1} with decreasing channel length. The drop of

the apparent field-effect mobility in the short channel device (10 μm) was due to the existence of parasitic source/drain resistance.

The effect of adsorbed oxygen on IGZO TFTs is explored by Kang *et al*. [96]. Transfer curves are measured and V_{on} monitored at atmosphere and as a vacuum is pulled in a chamber (as low as 8.5×10^{-6} Torr). After reaching the lowest pressure, oxygen is then introduced into the chamber with measurements being made at varying intervals. In ambient air, V_{on} is approximately −7 V. However, at a pressure of 8×10^{-6} Torr, V_{on} dramatically shifts to nearly −47 V. When the oxygen is introduced in the chamber, the turn-on voltage returns to the normal value (V_{on} in air). It is believed that the adsorbed oxygen forms a depletion layer below the surface, resulting in V_{on} shifts. Song *et al*. examine the short-channel effects of IGZO based TFTs. TFTs with source-to-drain separation of 50 nm are fabricated utilizing e-beam lithography [15]. These devices showed a μ_{FE} of 8.2 $cm^2 V^{-1} s^{-1}$ and V_{on} of -2 V. Varying the source-to-drain separation from 50 nm to 500 nm had minimal effects on the subthreshold swing and turn-on voltage. The drain current however did not scale linearly with source-to-drain separation, and is attributed to the effect of contact resistance.

Jeong *et al*. examined the effect of channel deposition pressure when fabricating IGZO TFTs [97]. The performance of the transistors improved monotonically with decreasing chamber pressure. At a pressure of 1 mTorr, μ_{FE} and S of the TFTs were dramatically improved to 21.8 $cm^2 V^{-1} s^{-1}$ and 0.17 V $decade^{-1}$, respectively, compared to those (11.4 $cm^2 V^{-1} s^{-1}$ and 0.87 V $decade^{-1}$) transistors prepared at 5 mTorr. The enhancement in the subthreshold characteristics was attributed to the reduction of the bulk defects of the IGZO channel, which might result from the greater densification of the IGZO films at the lower deposition pressure. Park *et al*. have also studied the effects of water on IGZO-based TFTs [98]. Two competing effects are analyzed, for films thicker than 100 nm, water appears to act as an electron donor, manifesting as a large negative threshold voltage shift. For films thinner than 70 nm, water appears to act as an acceptor-like trap, manifesting as a large increase in subthreshold swing characteristics. The mechanism for both electron donor- and acceptor-like trap appears to be reversible. Recently Park *et al*. have formed IGZO TFTs with a self-aligned process [99]. In a top gate device structure after patterning the gate electrode and gate

dielectric (100 nm of CVD SiO_2) the device is exposed to an argon plasma, which dopes the exposed semiconductor region with oxygen vacancies, rendering them conductive and constitute the source and drain. Double-gated IGZO TFTs have also been reported [100].

Chiang *et al*. reported on the processing effects on IGZO TFT performance [101]. Transistors are bottom-gate inverted structures fabricated on thermally grown silicon dioxide/silicon substrates with the IGZO being deposited by RF magnetron sputtering. Oxygen partial pressure, sputtering power, anneal temperature, and deposition time (channel thickness) are all varied. In general, experimental variables (such as RF power and O_2 partial pressure) have the greatest influence at lower post-deposition anneal temperatures (< 400 °C). At higher temperatures (> 400 °C), the annealing treatment dominates device performance and minimizes the effect of deposition process variables. Solution-processed IGZO thin films have been used as TFT channel layer by Kim *et al*. [102]. A spin-coating method using acetate- and nitrate-based indium, gallium and zinc precursors was used. The IGZO film annealed at 450 °C had smooth morphology and fine grains with an average size of ~ 15 nm. I_{on}/I_{off}, μ_{FE}, and S were ~ 10^6, 0.96 $cm^2 V^{-1} s^{-1}$, and 1.39 V $decade^{-1}$, respectively.

2.5.4 Oxide semiconductor based circuits

The majority of the research reported on oxide semiconductor based devices has been focused on the development of discrete TFTs. While a large number of these reports describe the optimization of the DC characteristics of these TFTs, over the past couple of years there has been some interest in creating integrated circuits and studying the dynamic characteristics of oxide semiconductor TFTs. Basic structures such as inverters and ring oscillators have been reported. Oxide semiconductor based TFTs have been used as switching devices for liquid crystal displays (LCDs) and driving transistors for organic light emitting diodes (OLEDs). A brief description of some of these applications is given below.

2.5.4.1 Inverters and Ring oscillators

The basic building block of digital circuits is an inverter. Its function is to provide an output that is the opposite of the input signal, i.e. if the signal is high the output will be low and vice versa. In standard complementary metal oxide semiconductor (CMOS) technology two transistors of opposite polarity (PMOS and NMOS) are used to achieve an inverter behavior. Whereas, oxide semiconductor based TFTs are unipolar in nature and hence two enhancement-mode transistors (load and control) are connected in series as shown in Figure 2-5(a) to produce an inverter action. The load transistor is diode driven (in saturation) and this configuration is widely used in unipolar TFT technology [103].

The dynamic performance of TFTs is an important property for circuit and display applications. Ring oscillators (ROs) are used to evaluate how fast the TFTs operate. A RO is formed by connecting an odd number of inverters in series and tying the output of the final inverter back to the input of the first inverter as shown in Figure 2-5(c). Since there are an odd number of inverters the output of the final stage is opposite to that of the input of the first stage and leads to an indefinite oscillation (provided the gain of each inverter stage is greater than 1). ROs are used to determine the propagation delay, t_p, of each inverter stage.

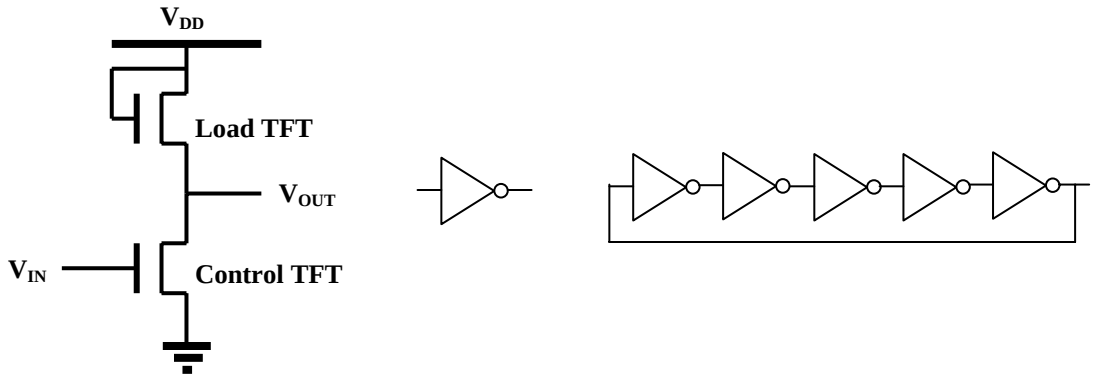

Figure 2-5: (a) Inverter structure for an n-type transistor technology. The active load is an enhancement-mode TFT operating in saturation. (b) Representation of an inverter with gain. (c) A five-stage ring oscillator structure in which five inverters are connected in tandem.

Presley *et al*. reported on the first transparent five-stage ring oscillator based on IGO TFTs [52]. The channel was deposited by RF magnetron sputtering; SiN_x and ITO act as the gate insulator and the source/drain electrode, respectively. The gain of an inverter stage is measured to be ~ 1.5 and the oscillation frequency of the RO is found to vary approximately linearly with increasing supply voltage, V_{DD}. The maximum frequency was determined to be ~ 9.5 kHz at an applied bias of 80 V. Large gate-source/gate-drain overlaps of 200 µm and large channel lengths of 60 µm are attributed to the low oscillation frequency of this device.

Ofugi *et al*. [104] and Hayashi *et al*. [93] have reported on the performance of a five-stage RO based on IGZO TFTs. Au/Ti metal was used as the gate and source/drain electrodes and patterned by lift-off. SiO_x (gate insulator) and IGZO (channel) were deposited by RF magnetron sputtering and patterned by photolithography and wet etching. The structures are annealed at 300 °C for 20 min in air. Channel lengths are 10 µm with a gate-source/gate-drain overlap of 5 µm. The RO starts to oscillate even at a low supply voltage of 1 V, and as the supply voltage increases the propagation delay per stage decreases. With a supply voltage of V_{DD} = 18 V, the oscillation frequency is 410 kHz corresponding to a propagation delay of 240 ns per stage.

RO based on plasma enhanced chemical vapor deposition (PECVD) processed ZnO have been reported by Sun *et al*. [105]. PECVD Al_2O_3 acts as the gate insulator, Al and Cr metal act as the source/drain and gate respectively. The individual TFTs exhibited a μ_{FE} ~ 0.05 $cm^2 V^{-1} s^{-1}$. Five-stage RO oscillated at 1.2 kHz at a V_{DD} = 60 V corresponding to a propagation delay of 100 µs. A rather marked improvement in ZnO based RO device performance was achieved by Sun *et al*. [106]. For this study a seven-stage RO was fabricated with ZnO and Al_2O_3 deposited using a spatial ALD process at 200 °C. A much improved μ_{FE} of ~ 13 $cm^2 V^{-1} s^{-1}$ was extracted. For V_{DD} = 25 V, the circuit operated at a frequency of 2.3 MHz corresponding to a propagation delay of 31 ns per stage.

Even faster RO based on IGZO TFTs has been very recently revealed by Yin *et al*. [107]. Five-stage RO with propagation delay times of 0.94 ns per stage for a supply voltage of 9 V is achieved. The reason for this superior performance is the small channel length and gate-source/gate-drain overlaps each being 0.5 µm. Also a more complicated inverter structure

called bootstrapped inverter involving three TFTs was used. These reports show the capability of oxide semiconductors for circuit applications.

2.5.4.2 Oxide semiconductor TFTs for display applications

As mentioned earlier recently, oxide semiconductor based TFTs have been used as switching transistors for LCD and driver transistors for OLED applications. In 2006, Gorrn *et al*. reported the application of a ZTO TFT in combination with an OLED to create a transparent pixel [18]. The OLED is built vertically on top of the TFT structure and uses the drain electrode of the transistor as the cathode for the diode. The ZTO channel layer is deposited via oxygen plasma assisted pulsed laser deposition (PAPLD). The radical oxygen species in this technique prevent the formation of oxygen vacancies and hence reduces unintentional doping. No post-deposition anneal is employed, and the maximum processing temperature was 150 °C. The pixel has an average transmittance of greater than 70% in the optical portion of the spectrum. Threshold voltages of the ZTO TFT are reported to vary between -1 V and 1 V. A saturated μ_{FE} of 11 $cm^2 V^{-1} s^{-1}$ and an $I_{on}/I_{off} \sim 10^5$ are also observed. The OLED had a luminance of 500 cd m^{-2} at a gate and anode bias of 5 V and 25 V respectively.

Jeong *et al*. [108] of Samsung SDI have reported a full-color display driven by an IGZO backplane using two-transistors one-capacitor (2Tr-1C) circuitry. The discrete TFT fabrication is previously discussed in Section 2.5.3. The display is a full-color 12.1-inch WXGA (1280 x 768 pixels) active matrix OLED (AMOLED) display. There are 123 pixels per inch (ppi) and this is the largest AMOLED display driven by an amorphous oxide TFT backplane to date. Hayashi *et al*. [93] also briefly report on OLED cells driven by a 2Tr-1C circuit, which is illustrated in Figure 2.6. The OLED cell is monolithically integrated with the backplane circuit. The authors report successful illumination of the OLED while no discrete device performance is provided.

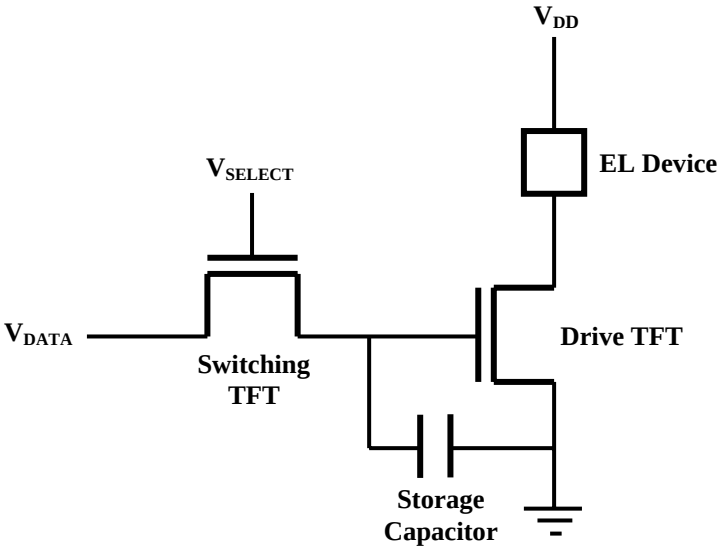

Figure 2-6: A commonly used two-transistor, one-capacitor (2Tr-1C) pixel circuit. The electroluminescent (EL) device, e.g. OLED, is made operational by turning 'on' the drive TFT by the right combination V_{SELECT} and V_{DATA} signals.

Ito *et al*. have demonstrated the application of IGZO TFTs to electronic paper [13]. A 4" bottom gated IGZO TFT array was integrated with an electrophoretic frontplane. Both the channel (IGZO) and the gate insulator (SiON) were RF sputtered while the source and drain (Ag) was screen-printed. The TFTs show a high $I_{on}/I_{off} \sim 10^7$ and the extracted μ_{FE} was ~ 2.8 $cm^2 V^{-1} s^{-1}$. The resolution of the display is 200 ppi and the number of the pixel is 640 x 480 (QVGA). Ju *et al*. have reported on a transparent AMOLED display driven by an In_2O_3 nanowire circuitry [109]. They describe the fabrication of the In_2O_3 TFT and its integration with the OLED structure. InO NWs were synthesized by pulsed laser ablation; the gate dielectric was a self-assembled nano dielectric (SAND) with ITO being the source and drain. Mobilities ~ 258 $cm^2 V^{-1} s^{-1}$ were reported. A single pixel consisted of one switching and two driving transistors. A major advantage is the transparency, which enhances the aperture ratios and the room temperature processing.

2.6 Bias stability in thin film transistors

Long-term reliability is an important factor that needs to be addressed before any material system can be adopted for large-scale manufacturing. Instabilities in the device behavior can be classified as environmental or electrically induced. Instabilities have been explored for MOSFET, a-Si:H, organic TFTs (OTFT) and oxide semiconductor based TFTs. The instability is usually characterized by the presence of hysteresis or a threshold voltage shift but in essence instability manifests as an alteration of the current–voltage (*I-V*) characteristics of the TFT. This might include changes in the magnitude of the drain current, the mobility or the subthreshold slope. In the following section a brief description of the two major mechanisms that have been attributed for electrical instability in TFTs is discussed.

Most types of electrical instabilities in TFTs arise from some form of charge rearrangement or generation in the semiconductor or the dielectric or at the semiconductor/dielectric interface. a-Si:H based TFTs exhibit both these forms of instabilities. As bias voltages are applied to a-Si:H TFTs, the band bending in the channel leads to the silicon atom having an unstable configuration. This unstable situation is resolved by the breaking of the weak Si-Si bonds and the formation of dangling bond defects [110],

$$2Si_4^0 + e^- \rightarrow Si_3^- + Si_3^0 \tag{2.8}$$

these dangling bonds create deep-gap states in the a-Si:H and alter the current–voltage behavior of the TFTs. The defect creation in a-Si:H channel occurs at lower positive gate voltages (e.g., $V_G < 25$ V). It has been proposed that deep-state defect creation is characterized by a power law time dependence and is strongly affected by temperature and the threshold voltage shift seen due to bias stressing is given by [111],

$$\Delta V_T(t) = A(V_G - V_{Ti})t^{\beta} \tag{2.9}$$

where A and β are temperature-dependent parameters, V_G is the gate bias stress voltage, V_{Ti} is the threshold voltage of the TFT before bias stress is applied, and t is the bias stress time duration.

The other mechanism, charge trapping, is considered to be due to the tunneling of carriers from the semiconductor into shallow traps at the insulator-semiconductor interface or into defects in the insulator due to the lowering of the energy barrier between the semiconductor and insulator during stress. A number of possible electron injection mechanisms leading to TFT instability were proposed by Powell [112], including (a) Fowler- Nordheim injection, (b) trap-assisted injection, (c) constant energy tunneling from the conduction band, (d) tunneling from conduction band to E_F, (e) hopping at the Fermi level. While mechanics (a) and (b) occur at a relatively high electric fields, mechanism (d) and (e) have been used to account for charge trapping in CdSe TFTs and the time dependence of the threshold voltage shift is modeled as,

$$\Delta V_T(t) = r_d \log\left(1 + \frac{t}{t_0}\right) \tag{2.10}$$

where r_d is a constant which contains the density of traps N_t [cm^{-3}] and a tunneling constant λ [cm] and t_o is the supply function dependent on the biasing temperature and state. A theory was proposed to explain the strong temperature dependence observed in the threshold voltage shift (ΔV_T) seen in a-Si:H TFTs. A redistribution of the tunneled electrons in the insulator by hopping i.e., the electrons initially tunnel to states in the nitride but after certain time as the states get filled up to a depth x_o, it becomes more favorable for electrons to hop from these filled states to states deeper in the insulator (i.e. $x > x_o$) rather than deeper states ($x > x_o$) getting filled directly by tunneling of electrons from the silicon channel. Libsch and Kanicki found that they could adequately model their bias temperature stress (BTS) data using the following standard exponential equation,

$$\left|\Delta V_T\right| = \left|V_G - V_{T0}\right|\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{2.11}$$

where β is a constant, τ is expressed as $\tau = \tau_0 \exp(E_\tau / kT)$, E_τ is the effective potential barrier for carriers to enter the insulator and V_{T0} is the initial threshold voltage [113]. This behavior is especially seen in PECVD a-SiN_x gate insulator TFTs due to the high defect density of SiN_x, which leads to a charge trapping when the TFT undergoes bias stress.

Few bias stress studies have been carried out on oxide semiconductor based TFTs. Navamathavan *et al*. report on the bias stress stability of DC magnetron spluttered ZnO TFTs using PECVD SiN_x as the gate insulator [114]. After applying a modest bias of $V_{GS} = V_{DS} =$ 10 V for 200 s the *I-V* characteristics is severely degraded with an increase in off-state current (about 3 decades) and an increase in the subthreshold slope. They attribute the degradation of device behavior to charge trapping at the SiN_x/ZnO interface and the breaking of Zn-O bonding. Cross *et al*. studied the bias stability of RF magnetron sputtered ZnO/thermal SiO_2 TFTs [115]. Positive gate bias stress leads to a positive ΔV_T while negative stresses lead to negative shifts. At low bias levels the subthreshold characteristics do not change. This instability is attributed to charge trapping at/near the channel/insulator interface. Higher biases ($V_G > 30$ V) cause a deterioration of the subthreshold shape and this is attributed to an increase in the defect state creation within the ZnO channel material. Another aspect of this study is that after the stress measurements, when the devices are left unbiased at room temperature, the original characteristics are recovered and without any necessity of annealing

The effect of composition and processing temperature on zinc tin oxide (ZTO) TFT bias stress stability was studied by Gorrn *et al*. [17]. Pulsed laser deposition (PLD) was used to deposit the ZTO layer and the gate insulator used was an AlO_x/TiO_x nanolaminate (ATO). Highly stable transistors with the ZTO composition of [Zn]:[Sn] = 36:64 were fabricated with $\Delta V_T \sim 30$ mV after 1000 minutes of operation. A clear correlation between processing temperature and bias stability were ascertained. Both positive and negative threshold voltage shifts were observed and attributed to charge trapping and defect state creation in the semiconductor layer respectively.

Various other reports on the oxide semiconductor TFT stability have been reported recently. Levy *et al*. report on atomic layer deposited ZnO TFTs and note that the bias stability improves markedly by passivating the device using ALD Al_2O_3 [82]. Park *et al.* have reported on the bias stability of TFT fabricated using a novel channel material ZrInZnO [116]. They compare the bias stability to IGZO TFTs and attribute the improved stability of ZrInZnO TFTs to the role of Zn ions as oxygen binders or structural stabilizers in the

ZrInZnO material system. Solution processed ZTO were examined by Seo *et al*. [117]. Cho *et al*. report on the charge trapping and detrapping as a mechanism of V_T shifts in IGZO TFTs under static and dynamic stresses [118]. Jeong *et al*. attribute the bias stress instability of IGZO TFTs to the interaction between the exposed IGZO back surface and oxygen and/or water in the ambient atmosphere during the gate voltage stress [119]. Chiang *et al*. propose the trapping of charges as a mechanism for V_T shift in IGZO TFTs under bias tress [101]. They achieve stable TFTs by minimizing the charges present in the channel (to minimize the trapping) by controlling the processing of the IGZO channel.

CHAPTER 3

EXPERIMENTAL METHODS AND DEVICE CHARACTERIZATION

This chapter presents information regarding the fabrication and characterization of IGZO based thin films and devices. Thin-film processing techniques used in this work including, pulsed laser deposition, plasma enhanced chemical vapor deposition and atomic layer deposition, are briefly discussed and thin film pattering techniques are explored. Thin-film characterization techniques are discussed including, Hall and optical transmission measurements. Finally, IGZO TFT characterization including, threshold voltage and channel mobility extraction from DC $I-V$ measurements is discussed.

3.1 Pulsed laser deposition

A major part of the work in this dissertation involves the synthesis of thin films by pulsed laser deposition (PLD) the technique used to deposit indium gallium zinc oxide (IGZO) and indium tin oxide (ITO) thin films. In this subsection a brief description of the process along with the characteristics of our system and methods is given. PLD is a versatile thin film deposition technique in which short and high-energy laser pulses are used to ablate a solid target in a high vacuum chamber. Typically, a ceramic target is placed in a vacuum chamber and a pulsed laser beam is used to vaporize the surface of the target and the vapor condenses on a substrate producing a thin film of the target material.

There are a few basic characteristics of the PLD technique that make it unique. Owing to the high power density of the system and the narrow bandwidth of the laser the radiation energy is enough to vaporize even the hardest and most heat resistant materials. Also the stoichiometry of the target is faithfully retained in the deposited films, since the extremely high heating rate of the target surface due to high energy laser pulses leads to congruent evaporation of the target irrespective of the evaporating point of the constituent elements or compounds of the

target. Another feature of PLD is the high energy (10 eV – 100 eV) of the ablated species in the plasma. As a comparison, the average energy of the impinging species in MBE is ~ 0.1 eV and in sputtering is of the order of few eV. The higher kinetic energies lead to enhanced adatom mobility and increased surface diffusivity.

PLD also provides us with a high deposition rate owing to the forward directed nature of the plume. This also ensures minimum contamination and preserves the stoichiometry in case of multi-component targets, as in our case with IGZO and ITO. The major disadvantage of the PLD process is its non – uniformity due to the narrow angular distribution of the ablated species. The other issue is the splashing or deposition of particulates on the film due to surface boiling or exfoliation of the target. The size of particulates may be as large as a few microns. These features limit the use of PLD in producing a large area uniform thin film. Most of the samples used in the present work were of the size ~15 mm x 15 mm and fairly uniform film growth can be achieved by controlling the deposition parameters and rotating the substrates. To reduce particulate issues low laser fluence ~ 150-160 mJ was used.

A basic PLD system consists of primarily three components: 1) High power laser source, 2) A vacuum chamber containing both the target and the substrate holder and, 3) Laser optics consisting of a set of lenses, apertures, and mirrors needed to guide the laser beam onto the target through a UV laser window. A schematic of a PLD set-up used in the present work is shown in Figure 3-1. The primary choice for the PLD radiation has been excimer lasers, since they emit radiation in the 200 – 400 nm wavelength range [120]. This is ideal since most materials show strong absorption in this wavelength range. Repetition rates as high as several hundred hertz and energies over 500 mJ/pulse can be easily achieved using excimer lasers. The wavelength at which the laser emits depends on the gases used. In the present work the KrF excimer laser was used as the laser source.

The ITO thin films in this study were grown from a commercial target (91 mol% In_2O_3-9 mol% SnO_2). For IGZO films the target was made in-house. High purity In_2O_3, Ga_2O_3, ZnO powders were used. Powders were weighed to give the required composition of the IGZO target and mixed in a beaker with ethyl alcohol. The suspension was stirred and left to dry in a chemical hood. The dried out powder was then ground using a mortar and pestle. This

powder was transferred to an alumina crucible with a lid and calcined at 1000 ºC for 2 hrs in a box furnace. Next the powder was ground once again and is now ready to be pressed. A 1" die was used and lubricated with a small amount of oleic acid. About 5 to 6 grams of powder are transferred into the die and pressed. The amount of pressure is typically around 5000 psi. Next the pressed pellet is transferred into a clean alumina crucible and sintered in a tube furnace. Temperatures for sintering IGZO is usually from ~ 1200 ºC to ~ 1400 ºC, for about 3 to 6 hours.

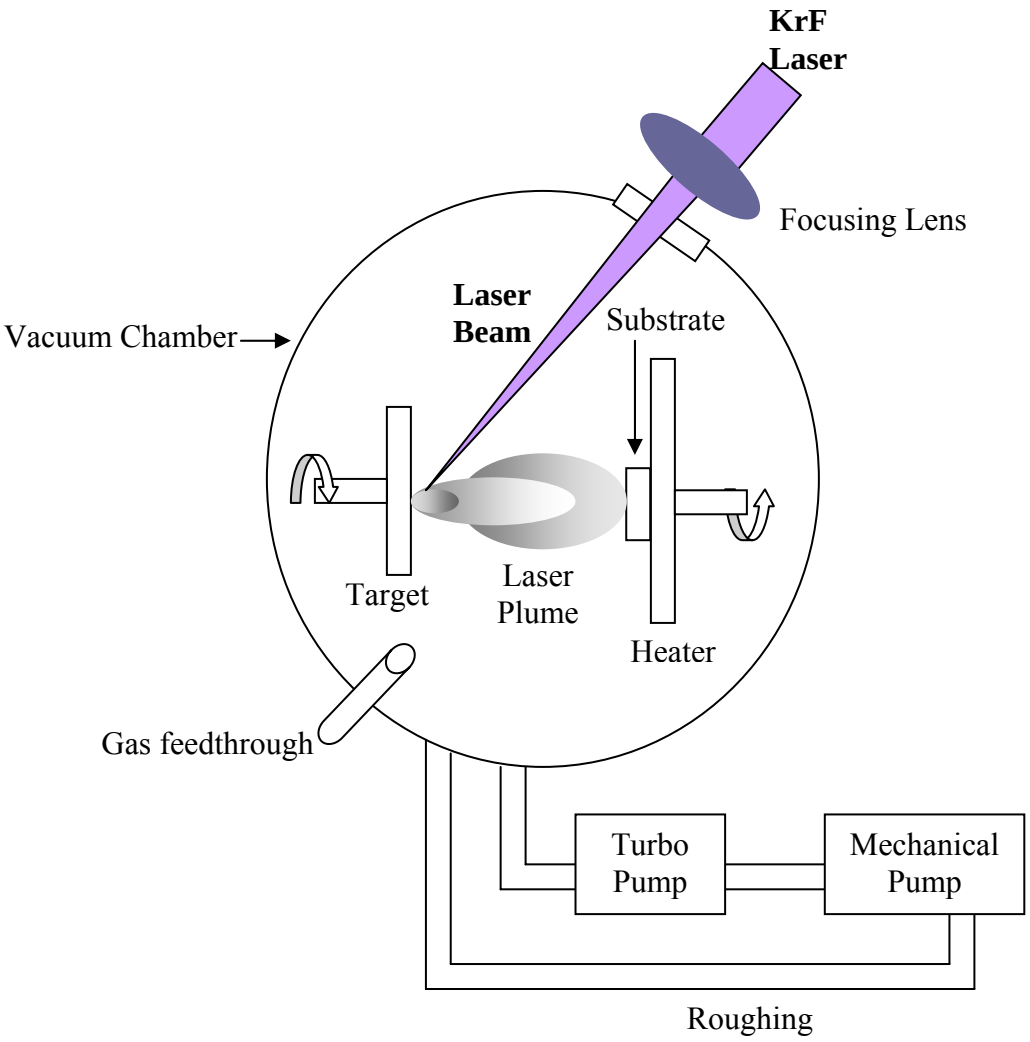

Figure 3-1: A schematic of a pulsed laser deposition chamber.

Samples and target are loaded into the PLD chamber which is then pumped down to a base pressure of ~ 1-2 x 10^{-7} Torr. Before the deposition the target was pre-cleaned with 500 pulses at 5 Hz and 500 pulses at 10 Hz repetition rate with the sample covered with a shutter. The repetition rate and energy level of laser pulses are kept at 10 Hz and 150 ~ 160 mJ in this study. During the depositions, the target is rotated and rastered to avoid target pitting. The substrate holder is also rotated during the growth for film uniformity. The oxygen partial pressure during deposition was actively controlled using a gate valve and varied between 5 mTorr and 100 mTorr and the number of pulses was varied to give the required film thickness. The PLD depositions were all carried out at room temperature with no intentional heating of the substrates.

3.2 Plasma-enhanced chemical vapor deposition

Chemical vapor deposition (CVD) is a thin film deposition technique in which gas-phase sources are employed. In a thermal CVD method the introduced gas-phase precursors are transported by diffusion to the substrate where chemical reactions (driven by thermal energy) results in the formation of a thin film [121]. As a modification of the simple thermal CVD, alternate energy sources, such as plasmas and optical excitation can be used to drive the chemical reactions, allowing the deposition to occur at low temperature.

Plasma-enhanced chemical vapor deposition (PECVD) techniques use RF energy to generate a glow discharge (plasma) and this transforms the gas mixture into reactive radicals, ions, neutral atoms and molecules, and other highly excited species. These atomic and molecular fragments interact with the substrate to complete the CVD reactions without a requirement of high substrate temperatures. Some of the desirable properties of PECVD films, apart from relatively low process temperatures, are good adhesion, good step coverage, and uniformity. In this work, an Oxford Plasmalab 80^{Plus} parallel plate PECVD system is utilized is utilized to deposit both SiN_x and SiO_x for use as a gate dielectric.

3.3 Atomic layer deposition

Atomic layer deposition (ALD) is a process for synthesizing thin solid films from alternating exposures of molecular precursors to a substrate. The main attribute of the ALD process, that differentiates it from other thin film depositions techniques, is its self-limiting nature. The process is such that the entire sample surface is reacted to completion, disallowing further reactions to take place. The self-limiting film growth mechanism in ALD ensures excellent film conformality and uniformity over large areas, and atomic level composition and thickness control. The one major limitation of the ALD process is its slowness since around one monolayer of the film is deposited during each cycle.

In ALD the film growth takes place in a cyclical manner. An ALD growth cycle typically consists of four steps, as illustrated in Figure 3-2 for an ALD process employing trimethyl aluminum (TMA) and water as precursors.

First TMA is pulsed into the reaction chamber and reacts with the surface hydroxyl groups in a saturating manner until a monolayer has been chemisorbed on the substrate. Next the excess of the precursor is purged away with an inert gas. The second precursor H_2O is pulsed into the reactor and reacts with the chemisorbed TMA forming an AlO_x layer on the substrate and CH_4 gas as a byproduct. The CH_4 gas and excess H_2O are then purged with an inert carrier gas. The second purge completes one deposition cycle. The desired film thickness is obtained by repeating the deposition cycle an appropriate number of times. In the ideal case, a complete monolayer is formed in every deposition cycle and no impurities are introduced to the film. In practice, only a fraction of a monolayer may be deposited in each cycle due steric hindrances between bulky ligands in the chemisorption layer or lack of reactive surface sites [122].

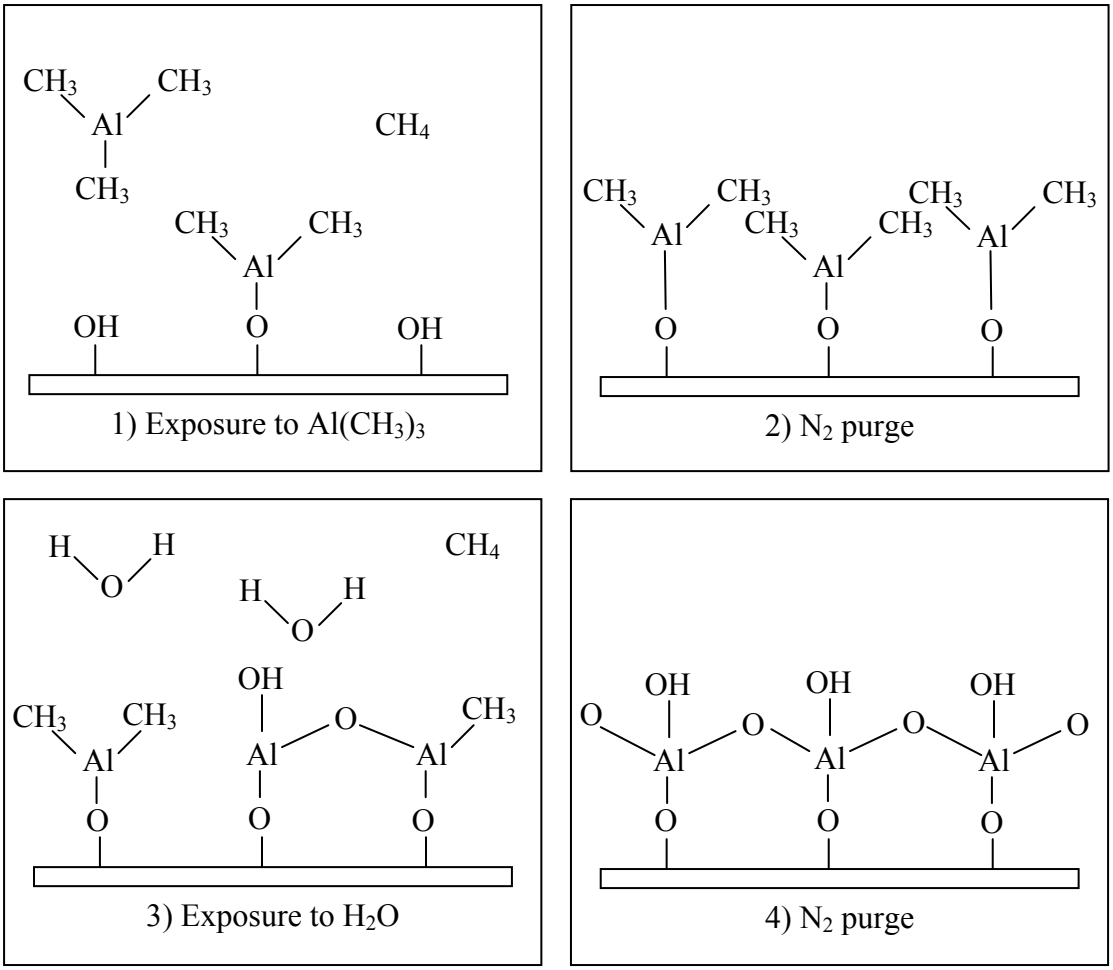

Figure 3-2: Schematic of aluminum oxide ALD using trimethylaluminum and water.

When the deposition conditions in ALD are optimal, the film growth proceeds through saturative, self-limiting surface reactions. Processing temperature is a key parameter for controlling the saturation mechanism of the ALD process. The temperature range where this ALD-type self-terminating growth takes place often leading to a constant growth rate, is known as the ALD window. Figure 3-3 illustrates a graph of growth rate vs. temperatures with the ALD window identified.

At low deposition temperatures the deposition rates could be high due to condensation, so instead of chemisorption, the precursor is physically absorbed on the sample surface.

Alternatively, the growth rate can be low if the reaction of the precursors with the surface is retarded due to the low temperature. At high deposition temperatures, the precursor can decompose leading to a CVD type deposition process and an increase in growth rate. On the other hand, at high deposition temperatures, the precursor can chemically desorb from the sample surface lowering the growth rate.

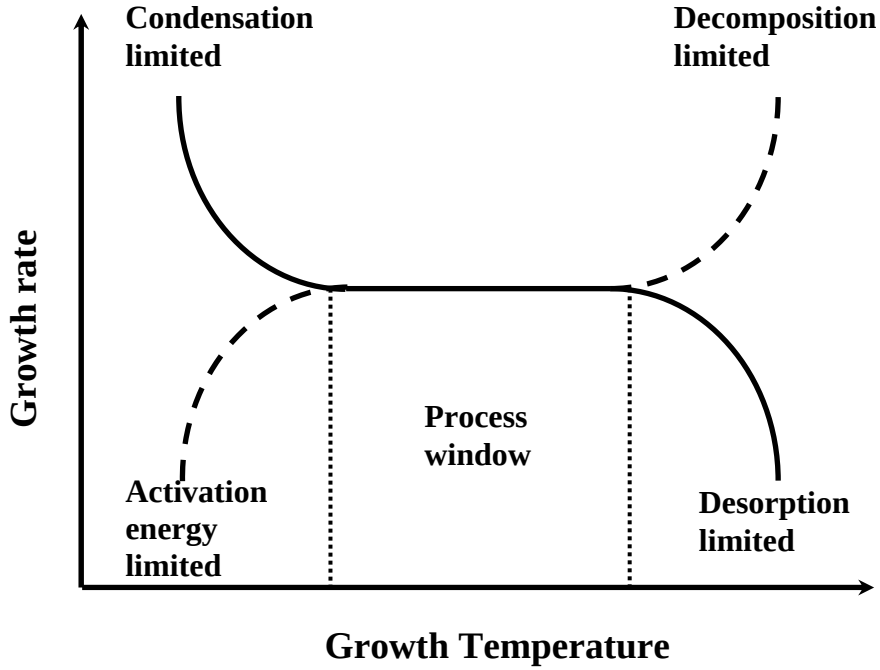

Figure 3-3: ALD process window.

In this work, a Savannah 100, Cambridge Nanotech ALD system was used to deposit, aluminum oxide (AlO_x) and platinum nanoparticles (Pt-NPs) as a dielectric and a charge-trapping layer, respectively. The precursors used and other pertinent process parameters have been listed in Table 3-1. The individual half cycle reactions for AlO_x, and Pt are listed below, where * represents the surface species.

Aluminum oxide [123]

$$*OH\ (s) + Al(CH_3)_3\ (g) \rightarrow *OAl(CH_3)_2\ (s) + CH_4\ (g)$$

$$*OAl(CH_3)_2\ (s) + 2H_2O\ (g) \rightarrow *OAl(OH)_2\ (s) + 2CH_4\ (g)$$

Platinum metal [124]

$$*Pt\ (s) + O_2\ (g) \rightarrow *PtO_x\ (s)$$

$$CH_3C_5H_4Pt(CH_3)_3\ (g) + *PtO_x\ (s) \rightarrow *Pt\ (s) + CO_2\ (g) + H_2O\ (g) + \text{other by-products}\ (g)$$

Table 3-1: ALD growth conditions for AlO_x, and Pt used in this work.

Layer	Temperature (^oC)	Precursors	Pulse time (s)	Purge time (s)	Exposure (s)
AlO_x	200	Trimethyl Amuminum (TMA)	0.15	8	0-1
		Water (H_2O)	0.15	8	0-1
Pt	270	(methylcyclopentadienyl)trimethylplatinum ($(MeCpPtMe_3)$)	0.25	3	none
		Oxygen (O_2)	1	3	none

3.4 Thin film patterning

Patterning of thin films is essential for device fabrication and integration. The films can be patterned either by photolithographic techniques or by using a shadow mask. Shadow mask patterning is the simplest, in which a physical mask is placed in the path of the incoming plume during pulsed laser deposition to create a pattern. This technique is widely used in applications in which the underlying layers are not compatible with photolithographic techniques or when the resolution is not critical for device fabrication. In this work photolithographic techniques were exclusively used. There are two routes for pattering films – additive, which involves photolithography and liftoff, or subtractive, which involves photolithography and etching. Both these techniques are described below.

3.4.1 Photolithography

Lithography is the most important step for fabricating microscale structures. Photolithography, in which the energy source is ultraviolet (UV) light can be used to transfers a pattern onto another surface. The basic steps employed in photolithography are as follows. First, photoresist (a light sensitive material used to form the pattern) is coated on top of a thin film or substrate. The resist is then exposed to UV light through a mask, which contains transparent and opaque regions. The photoresist is then submerged in a developer to define the pattern, which selectively removes photoresist. Now post processing (etching, deposition, etc.) can be applied to regions without photoresist. Usually after the photoresist is coated on the substrate a soft bake is employed to drive out solvents and dehydrate the film. Other bake steps may be employed depending on the photoresist and the process involved.

Photoresists are polymers that consist of three major components: resin, a photoactive component (PAC), and solvent. The type of PAC and its operation determines the photoresist type: negative or positive. The major difference lies in the solubility difference between the exposed and the unexposed portions of the resist. In a positive photoresist, the photoactive component decomposes when exposed to UV light; areas exposed to UV light become soluble in developer. In a negative photoresist, the photoactive component crosslinks when exposed to UV light and hence areas exposed to UV light become insoluble in developer.

In this work an MJB 360 mask aligner with a 365 nm (i-line) UV light source with exposure energy of 275 mJ/cm^2 was used. AZ5214E photoresist was used as both a positive and negative photoresist. In the positive mode the samples were developed directly after exposure. In the negative mode after exposure the samples were baked at 115 ^{o}C for 90 sec followed by a flood exposure (no mask required) for 90 sec before the samples were developed.

3.4.2 Lift-off patterning

Lift-off patterning is the common additive technique to transfer a pattern from a mask on to the substrate. The lift-off process involves spinning and patterning the photoresist, and then the thin film is deposited directly on the patterned photoresist layer and the substrate. The substrate is then submerged in a solvent (usually acetone) to remove the photoresist, this also removes the film on top of the photoresist leaving the desired pattern of the thin film on the substrate. The presence of photoresist keeps the temperature limit of the subsequent deposition process below ~ 300 ^{o}C. In this work, the thin films deposited using PLD were patterned using the lift-off technique.

3.4.3 Etching

In this subtractive process, after photolithography is first used to define the pattern, the etching process is then used to selectively remove the exposed surface and form the desired patterns. Broadly there are three types of etching: (a) wet chemical etching, (b) physical etching, and (c) reactive ion etching (RIE), a combination of chemical and physical etching. In this work RIE was used exclusively as the etching process and is discussed further.

RIE, or plasma etching, is carried out in a plasma chamber and is technically the reverse process of plasma-enhanced deposition described in Section 3.2. In RIE reacting gases dissociate through electron impacts into radicals, which then transport to the underlying substrate surface and react with it to form volatile products. Etching in a plasma environment combines the selectivity of purely chemical etching and the anisotropy of physical etching [121]. Also a wide range of etch processes are available with differing amounts of physical and chemical attack. In a typical plasma etch process, the surface of the film to be etched is subjected to an incident flux of ions, radicals, electrons, and neutrals. Generally the physical etching is related to the ion flux and the chemical etching is related to the radical flux, but in some cases the ion energy is required to stimulate the chemical reaction.

In this work, two RIE etch tools were used. SiN_x and SiO_x layers were etched in an Oxford Plasmalab 80^{Plus} parallel plate RIE system and ITO layers were etched in a Plasmatherm batchtop RIE tool.

3.5 Thin film characterization

IGZO thin films were characterized for their optical and electrical properties. Optical transmission measurements provide information about the band gap energy and transition type of the films. Hall measurements can be used to determine the Hall mobility, carrier type and concentration. Four-point probe resistivity measurements are used to measure the conductivity of the thin films.

3.5.1 Optical transmission

IGZO films deposited on double side polished sapphire wafers were used for optical transmission measurements. The measurements in this study were performed on a dual-beam and double monochromator Perkin-Elmer Lambda 9 (UV-VIS-NIR) absorption spectrophotometer. The spectrophotometer has two light sources: a tungsten-halogen lamp and a deuterium lamp, and for NIR range optical detection it has a PbS detector. The two monochromator with UV/VIS gratings of 1440 line/mm and NIR gratings of 360 lines/mm are capable of operating at wavelengths from 185 to 3200 nm. To get the required spectral resolution, the slit width and the scan speed of the instrument are set as 1 nm and 120 nm/min or 0.5 nm and 7.5 nm/min.

3.5.2 Four-point probe resistivity measurements

The four-point probe resistivity measurement technique is used to eliminate the effects of contact resistance while measuring low resistivity samples. The technique is relatively simple with four probes are placed on the test sample in a linear fashion as shown in Figure 3-4. A

constant current is forced through the outer probes while the potential drop across the inner probes is measured. The high impedance of the voltmeter minimizes the current flow through the inner probes. Thus, since there is no potential drop across the contact resistance associated with the inner probes, only the resistance associated with the sample is measured. If probes with uniform spacing *s* are placed on an infinite slab material, then the resistivity, ρ, is given by

$$\rho = 2\pi s \frac{V}{I} \text{ for t >> s} \tag{3.1}$$

and

$$\rho = \frac{\pi t}{\ln 2} \frac{V}{I} \text{ for s >> t} \tag{3.2}$$

with *t* representing the thickness of the thin film. Errors might be introduced in the measurements due to proximity of the probes to the edge of the sample or limitations in the lateral dimension of the sample, which need to be corrected accordingly. The apparatus used in the set up for this study consisted of a Keithley 6517A electrometer, Keithley 220 programmable current source and a Lucas 302 four-point probe stand. The measurement head was made of four tungsten carbide probes with osmium tips, spaced .040" (~1 mm) apart.

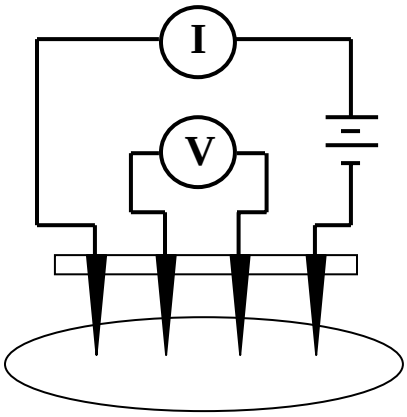

Figure 3-4: Schematic of the four-point resistivity measurement system.

3.5.3 Hall measurements

The Hall effect can be used to determine the carrier type and concentration, and mobility of a semiconductor sample [125]. The Hall effect is based on the Lorentz force seen by the carriers in a current carrying semiconductor when placed in a magnetic field. The charge carriers of the semiconductor experience a force in a direction perpendicular to the magnetic field and current. At equilibrium, the deflection experienced by the carriers (the direction depends on the carrier type) to the sample edges creating a potential known as Hall voltage, V_H and is given by,

$$V_H = \frac{BI}{qtn} \tag{3.3}$$

where q denotes the charge of the particle, B the magnetic field, I is the current, t is the thickness of the sample and n is the carrier concentration. We can also define the Hall coefficient, R_H,

$$R_H = \frac{tV_H}{BI} \tag{3.4}$$

and the sign of the Hall coefficient indicates the dominant carrier type – a negative Hall coefficient indicates that electrons are the dominant carriers. The carrier concentration, n, can be calculated by,

$$n = -\frac{1}{qR_H} \tag{3.5}$$

Without the presence of the magnetic field the sheet resistance, R_s, of the sample is assessed by measuring the film resistivity, ρ. Finally, the Hall mobility, μ_H, is determined by,

$$\mu_H = \frac{R_H}{\rho} \tag{3.6}$$

A typical Hall measurement involves soldering of gold wires using indium to the four corners of the samples. The potentials across two terminals are determined while passing current through the other two terminals to determine the resistivity of the films using the Van der Pauw technique. Following the determination of the resistivity of the films, positive and

negative magnetic fields are applied and Hall measurements are carried out. The measurement sequence and the Hall calculations to determine Hall mobility are detailed in Reference [126].

3.6 Thin-film transistor structures

In this dissertation two configurations of the bottom-gate staggered thin-film transistor structure – a fully transparent and a non-transparent TFT, are fabricated. The cross-section of both the devices are shown in Figure 3-5. The fully transparent TFT (TTFT) is fabricated using either ATO, or SiN_x as the gate dielectric. TFTs using ATO as the insulator are constructed on commercially available substrates from Planar Systems Inc. that are OA-2 borosilicate glass coated with a 250 nm (8 Ω/□) sputtered indium tin oxide (ITO) and a 220 nm atomic layer deposited AlO_x and TiO_x (ATO) superlattice with AlO_x capped on both sides. TFTs using SiN_x as the insulator are built on substrates from Delta Technologies Ltd. that are polished float glass passivated with SiO_2 coated with a 60 nm (60 Ω/□) sputtered ITO. The SiN_x layer is deposited using PECVD at 300 °C. The ITO and ATO or SiN_x layers constitute the gate electrode and gate dielectric, respectively, of a bottom-gate TTFT.

The non-transparent TFT is fabricated on heavily doped (0.01-0.03 Ω/□) p-type silicon substrates. The native oxide is etched using a 1 % HF solution and AlO_x is deposited using ALD. A Cr/Au (5 nm/300 nm) layer is e-beam evaporated on the backside of the silicon substrate. In this case, the silicon acts as both as the substrate and the gate electrode while the AlO_x acts as the gate dielectric. The IGZO channel and ITO source and the drain electrodes, are then deposited at room temperature by PLD. The channel and the source/drain electrode layers were patterned using standard photolithography and liftoff techniques. TFTs with various length and width dimensions were fabricated.

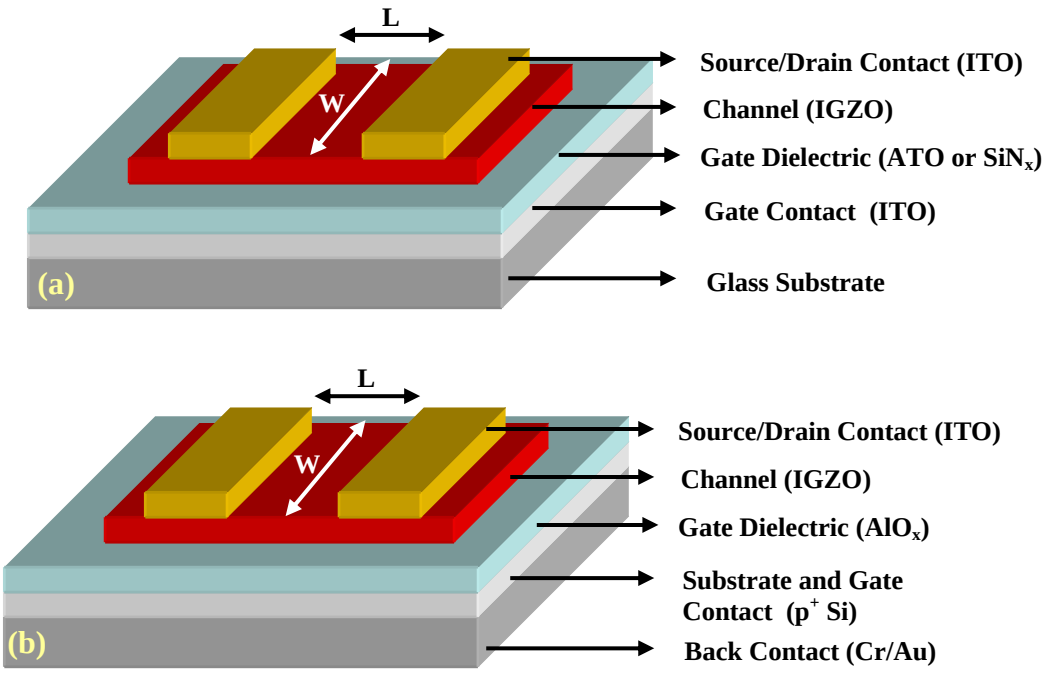

Figure 3.5: TFT structures used for the research discussed in this thesis, including (a) fully-transparent thin-film transistor and (b) non-transparent thin-film transistor.

3.7 Electrical Characterization of Devices

This section defines the various figures-of-merit used to characterize TFT performance and discusses the methodology involved in extracting them from experimental data. These include the subthreshold voltage swing, drain current on/off ratio, threshold voltage, turn-on voltage, and channel mobility. This section also sets up the framework under which behavior of IGZO based memory transistors and pixel circuit can be described.

3.7.1 Current-voltage characteristics

Current-voltage (*I-V*) characterization of the IGZO based TFTs and devices were carried out on a Cascade probe station using 3 micromanipulator probes. The electrical potential of

the metal vacuum chuck is floating. *I-V* characteristics throughout this work are obtained using a Hewlett Packard 4155B Precision Semiconductor Parameter Analyzer. All measurements are performed in the dark unless stated otherwise. A "Medium" integration time was used for all measurements. The two most common measurements used to describe TFT performance are the transfer characteristics (log [I_{DS}] *vs.* V_{GS}) and the output characteristics (I_{DS} *vs.* V_{DS}). These are discussed below.

3.7.2 DC I-V measurements: Output Characteristics

I_{DS}-V_{DS} or output characteristics are obtained by measuring drain current as a function of drain voltage for several different gate voltages. This produces a "family of curves" as shown in Figure 3-6. This measurement provides qualitative information about the device under test. Saturation, as seen in Figure 3-6, in these characteristics indicate the ability to completely deplete the channel of carriers using the applied bias voltages. Also, significant deviations from linearity in the low-V_{DS} region would indicate considerable contact resistance in the TFTs.

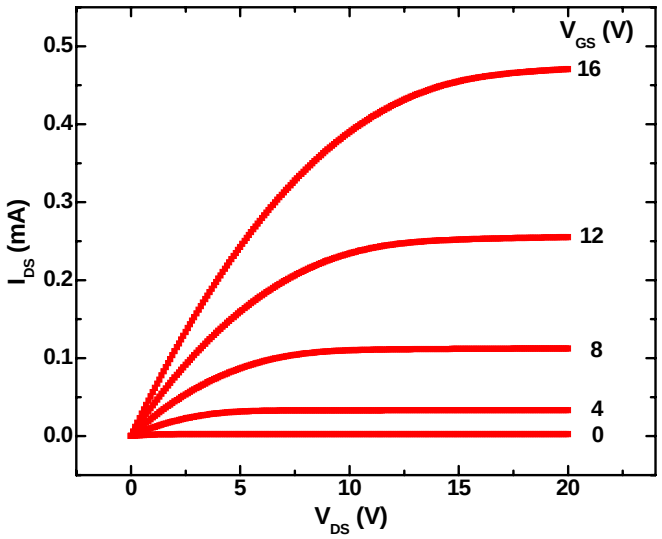

Figure 3-6: Output characteristics of an ATO gated IGZO TFT. Drain current (linear scale) is plotted against drain voltage for gate voltages 0-16 V in 4 V steps. 35 nm IGZO grown at an oxygen partial pressure of 25 mTorr. TFT dimensions, L = 100 μm and W = 400 μm.

3.7.3 DC I-V measurements: Transfer Characteristics

Log [I_{DS}]-V_{GS} or transfer characteristics is obtained by measuring drain current as a function of gate voltage typically at a low and a high V_{DS} value and is presented in a semi-log plot as shown in Figure 3-7. This measurement generally provides more quantitative information regarding the device under test. Several of the TFT parameters extraction are possible and are discussed below.

3.7.3.1 Subthreshold voltage swing and drain current on/off ratio

The subthreshold voltage swing, S, and the drain current on/off ratio (I_{on}/I_{off}) can be estimated from the transfer characteristics measured at a high V_{DS}. S is the inverse of the maximum slope in the transfer characteristics,

$$S = \left(\left. \frac{\partial \log(I_D)}{\partial V_{GS}} \right|_{\max} \right)^{-1} \tag{3.7}$$

S gives a measure of the increase in gate voltage required to switch the transistor from an off-state to an on-state. A small value of S is desirable because it corresponds to a fast transition from an off to on state. For the device shown in Figure 3-7, $S \sim 250$ mV decade^{-1}.

Drain current on/off ratio is another measure of the switching behavior of the TFT. It is simply the ratio between highest measured current (the on-state current, I_{on}) to the lowest measured current (the off-state current, I_{off}) as shown in Figure 3-7. I_{off} is also a measure of the gate leakage present in the device. For the device shown in Figure 3-7, the drain current on/off ratio is > 10^8.

3.7.3.2 Threshold voltage and turn on voltage

Threshold voltage, V_{TH}, is an important TFT parameter, which indicates the onset of drain current in the device. In this work V_{TH} was experimentally determined by biasing the TFT in

saturation, i.e. $V_{DS} \geq V_{GS} - V_T$. Using the square law model of a TFT, I_{DS} in saturation is given by,

$$I_D = \frac{1}{2}\mu C_{di}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \tag{3.8}$$

and

$$\sqrt{I_D} = \sqrt{\frac{\mu C_{di} W}{2L}}\left(V_{GS} - V_{TH}\right) \tag{3.9}$$

plotting $\sqrt{I_{DS}}$ *vs.* V_{GS} as shown in Figure 3-8 and by extrapolating down to the x-axis, the threshold voltage can be determined. Though V_{TH} is widely used in literature to describe TFTs, it is not a unique device parameter since there are several methods to extract V_{TH} including extrapolating I_{DS} *vs.* V_{GS} curves when the device is biased in the triode region.

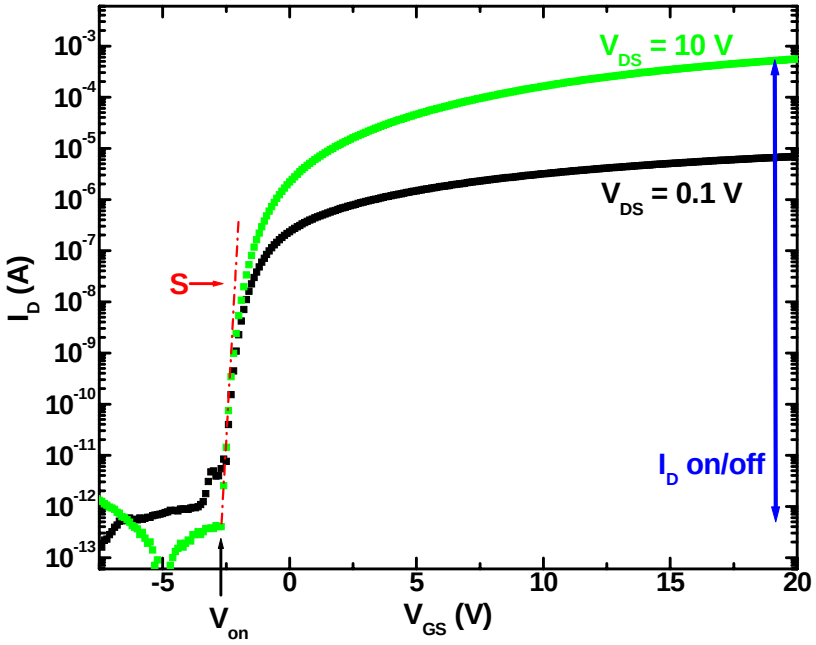

Figure 3-7: Transfer characteristics of an ATO gated IGZO TFT for 2 different V_{DS} values, 0.1 and 10 V. subthreshold voltage swing, drain current on/off ratio, and turn-on voltage are indicted. 35 nm IGZO grown at an oxygen partial pressure of 25 mTorr. TFT dimensions, L = 100 µm and W = 400 µm.

Moreover there is a genuine concern over the extrapolation techniques, which might be relatively subjective in nature. With this factor in consideration another parameter, the turn-

on voltage, V_{on}, has been used to evaluate the TFTs. V_{on} has been identified in the transfer characteristic in Figure 3-7 and is defined as the gate voltage at which there is a sharp increase in the channel conduction. Alternatively the turn-on voltage corresponds to the applied gate bias at which an appreciable density of mobile carriers is present in the channel. V_{on} is an easier parameter to handle especially in device analysis in which a shift in the onset of current conduction is observed such as during bias stress and memory transistor studies. In this work both V_{TH} and V_{on} are reported for the device tested.

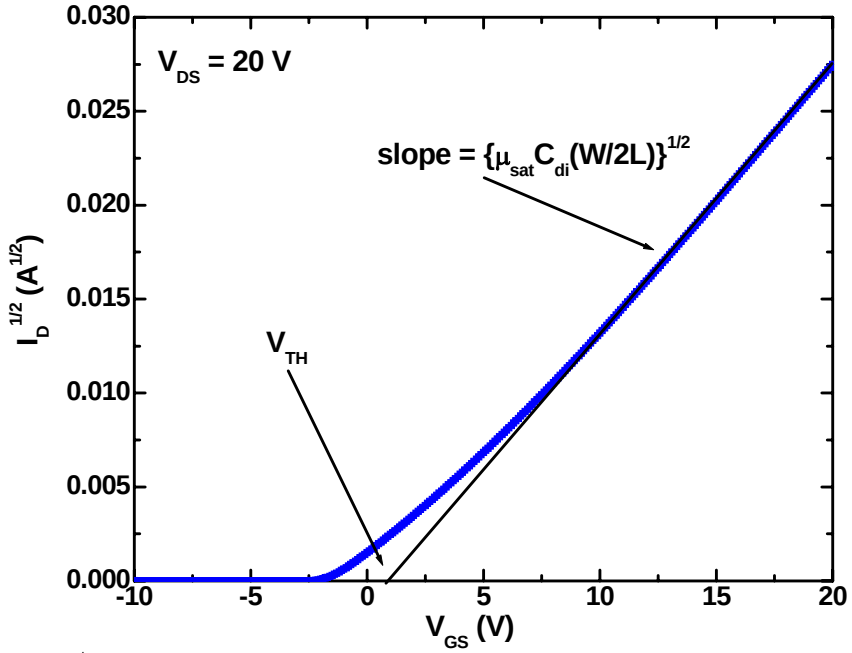

Figure 3-8: $\sqrt{I_{DS}}$ *vs.* V_{GS} characteristic of an ATO gated IGZO TFT when biased in the saturation regime with V_{DS} = 20 V. Threshold voltage, V_{TH}, and saturation mobility, μ_{sat}, can be extracted from this plot. 35 nm IGZO grown at an oxygen partial pressure of 25 mTorr. TFT dimensions, L = 100 μm and W = 400 μm.

3.7.3.3 Mobility extraction

The channel mobility is a key figure-of-merit for TFTs. It is the average mobility of carrier transported in the semiconductor channel and is a measure of the ease with which free carriers flow between the source and the drain when the TFT is biased appropriately. The channel mobility quantifies the current drive capability and a higher mobility corresponds to a higher current drive.

Similar to V_{TH} estimation, there are multiple techniques to extract the channel mobility, each resulting in slightly different values owing to the respective approximations involved. The most commonly encountered technique for determining the channel mobility employs MOSFET drain current equations. The effective mobility, μ_{eff}, and the field-effect mobility, μ_{FE}, are both determined from the linear portion of the triode region and the saturation mobility, μ_{sat}, is determined from the saturation region.

Classic mobility estimation techniques are extensively employed in literature as estimators of TFT channel mobility with an assumption that the channel mobility of TFTs is a constant independent of V_{GS}. This assumption would be valid for an ideal device, whereas TFTs may have several non-idealities including, carrier trapping, interface roughness scattering, velocity saturation, to name a few. Hoffman introduced two new mobility metrics, average mobility, μ_{avg}, and incremental mobility, μ_{inc}, which do not involve classic MOSFET equation manipulations and assumptions [69]. Hence these metrics are better suited to handle TFT non-idealities and provide us with a more physically meaningful and quantitatively representative metric of device performance. The physical significance of, μ_{avg} and μ_{inc} along with a short description of all five mobility estimates are discussed below.

3.7.3.3.1 μ_{eff}, μ_{FE}, and μ_{sat}

Consider the triode region of TFT operation. The drain current is given as,

$$I_D = \mu C_{di} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{3.10}$$

Note the use of V_{TH} to follow classical formulation of μ_{eff} and μ_{FE}. In the linear regime if V_{DS} is very small,

$$I_D \approx \mu C_{di} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS}\right] \tag{3.11}$$

Differentiating Eqn. (3.11) with respect to V_{DS} and V_{GS} yields the channel conductance, g_d, and the transconductance, g_m, respectively,

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{di} \frac{W}{L}\left[\left(V_{GS} - V_{TH}\right)\right] \tag{3.12}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{di} \frac{W}{L} V_{DS} \tag{3.13}$$

the effective mobility, $\mu_{eff,}$ and the field effect mobility, μ_{FE}, is then given by,

$$\mu_{eff} = \frac{g_d}{C_{di} \frac{W}{L}\left(V_{GS} - V_{TH}\right)} \tag{3.14}$$

$$\mu_{FE} = \frac{g_m}{C_{di} \frac{W}{L} V_{DS}} \tag{3.15}$$

from Eqn. (3.14) it can be seen that μ_{eff} is explicitly dependent on V_{GS}. Now consider the TFT operation in the saturation regime. Square law theory states,

$$I_D = \frac{1}{2} \mu C_{di} \frac{W}{L}\left[\left(V_{GS} - V_{TH}\right)^2\right] \tag{3.16}$$

μ_{sat} is extracted by taking the square root of Eqn. (3.16) and differentiating with respect to V_{GS}, and is given by,

$$\mu_{sat} = \left(\frac{d\sqrt{I_D}}{dV_{GS}} \frac{1}{\sqrt{C_{di} \frac{W}{2L}}} \right)^2 \tag{3.17}$$

in essence μ_{sat} is determined from the slope of the $\sqrt{I_{DS}}$ *vs.* V_{GS} graph shown in Figure 3-8. μ_{eff} is the preferred way of mobility extraction since μ_{sat} is inaccurate as it gives an average of the mobility in the channel and the pinched-off region whereas μ_{FE} is considered unreliable due to the exclusion of gate voltage dependence in the determination of μ_{FE}.

3.7.3.3.2 μ_{avg}, and μ_{inc}

Hoffman's method of mobility extraction uses basic charge transport theory assuming drift-dominated transport [69]. It also includes the gate voltage dependence of mobility.

Average mobility, μ_{avg} as the name suggests, takes into account the mobilities of all the carriers in the channel. To determine μ_{avg} the channel conductance of the TFT is considered and is given by,

$$G_d(V_{GS}) = \mu_{avg}(V_{GS})\frac{W}{L}Q_{ind}(V_{GS}) \tag{3.18}$$

where $Q_{ind}(V_{GS})$ is the cumulative charge per unit area induced in the channel by the applied gate voltage in excess of V_{on}. $Q_{ind}(V_{GS})$ can be approximated using simple electrostatics as,

$$Q_{ind}(V_{GS}) = C_{di}[V_{GS} - V_{on}] \tag{3.19}$$

Combining Eqn. (3.18) and Eqn. (3.19) and rearranging the terms we get,

$$\mu_{avg}(V_{GS}) = \frac{G_d(V_{GS})}{C_{di}\frac{W}{L}(V_{GS} - V_{on})} \tag{3.20}$$

The expression for μ_{avg}, is very similar to one for μ_{eff} except for the dependence of the channel conductance on the applied gate voltage and that V_{TH} is replaced with V_{on}. μ_{avg} is a good indicator of TFT performance for circuit applications because it takes into account all the carriers in the channel. Incremental mobility, μ_{inc}, corresponds to the incremental mobility of carriers added to the channel as the gate voltage increases. To estimate μ_{inc} the differential channel conductance is determined and is given by,

$$\Delta G_d(V_{GS}) = \mu_{inc}(V_{GS})\frac{W}{L}\Delta Q_{ind}(V_{GS}) \tag{3.21}$$

Differentiating Eqn. (3.19) substituting in Eqn. (3.21) we get

$$\mu_{inc}(V_{GS}) = \frac{\frac{\Delta G_d(V_{GS})}{\Delta V_{GS}}}{C_{di}\frac{W}{L}} = \frac{G_d'(V_{GS})}{C_{di}\frac{W}{L}} \tag{3.22}$$

Eqn. (3.22) is valid under the assumption that the mobility of the carriers already present does not change as additional charges are induced. μ_{inc} is a useful measure to study the transport properties of carriers in the channel. Both μ_{avg} and μ_{inc} are extracted at low V_{DS} values i.e. $V_{DS} \rightarrow 0$ since drift, rather than diffusion, is the dominant carrier transport mechanism in the linear regime.

In this work μ_{sat}, and μ_{avg} are used extensively to characterize IGZO TFTs. Figure 3-9 shows the comparison of μ_{sat} and μ_{avg} for the same IGZO TFT.

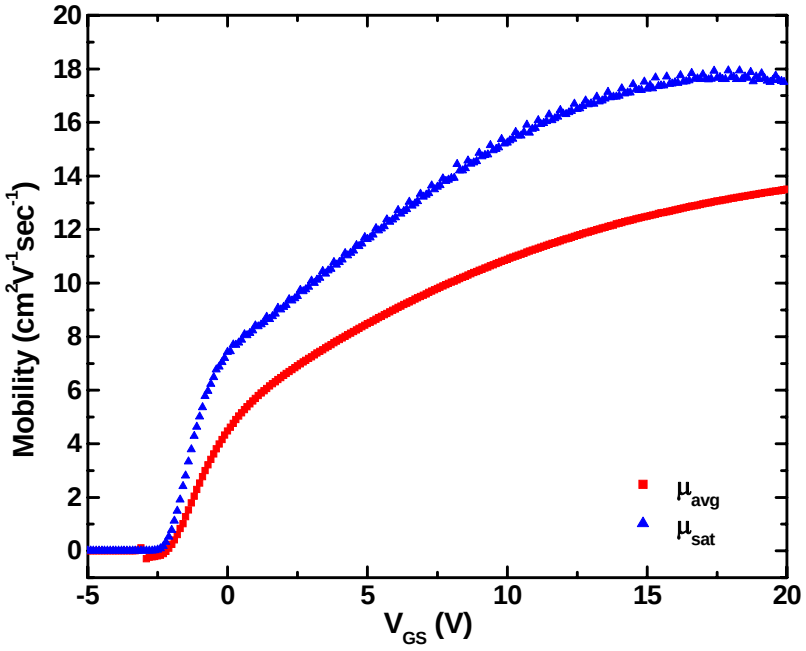

Figure 3-9: Comparison of mobility determination methods for an ATO gated IGZO TFT-channel. For this device, V_{on} and V_{TH} are –3 and 1 V, respectively. μ_{sat} is determined using V_{DS} = 20 V and Eqn. 3.17. μ_{avg} is determined using V_{DS} = 0.1 V and Eqn. 3.20. 35 nm IGZO grown at an oxygen partial pressure of 25 mTorr. TFT dimensions, L = 100 μm and W = 400 μm.

CHAPTER 4

INDIUM GALLIUM ZINC OXIDE THIN FILMS AND THIN-FILM TRANSISTORS BY PULSED LASER DEPOSITION

Based on manuscripts:

Transparent, high mobility of InGaZnO thin films deposited by PLD
A. Suresh, P. Gollakota, P.Wellenius, A. Dhawan, and J. F. Muth
Thin Solid Films, **516**, 1326 (2008).

Room temperature pulsed laser deposited indium gallium zinc oxide channel based transparent thin film transistors
A. Suresh, P.Wellenius, A. Dhawan, and J. F. Muth
Applied Physics Letters, **90**, 123512 (2007).

4.1 Abstract

Transparent amorphous oxide semiconductor thin films based on indium gallium zinc oxide (IGZO) were prepared by pulsed laser deposition (PLD) at room temperature. The oxygen partial pressure during deposition can be used to vary the carrier concentration by several orders of magnitude from insulating to 10^{19} carriers/cm^3. Hall mobilities as high as 16 cm^2 V^{-1} sec^{-1} were observed. This is approximately an order of magnitude higher than the mobility of amorphous silicon. IGZO thin films deposited by PLD at room temperature was used as a channel layer to fabricate transparent thin film transistors (TFTs) with good electrical characteristics; saturation field effect mobility of 12-14 cm^2 V^{-1} s^{-1} and subthreshold voltage swing of 200 mV decade^{-1}. By varying the oxygen partial pressure during deposition the conductivity of the channel was controlled to give a low off-state current ~ 10 pA and a

drain current on/off ratio of $> 1 \times 10^8$. Changing the channel layer thickness was a viable way to vary the threshold voltage. The effect of the gate dielectric on the electrical behavior is also studied. By measuring the electrical characteristics of TFTs of varying device dimensions the parasitic effects in the devices were evaluated.

4.2 IGZO thin films by PLD

4.2.1 Experimental Approach

The IGZO target of the composition, In:Ga:Zn :: 1:1:5 atomic ratio were prepared and pulsed laser deposition was used to deposit uniform IGZO films on sapphire and glass substrates at room temperature in an oxygen ambient. The oxygen partial pressure was varied between vacuum and 80 mTorr. A mass flow controller regulates oxygen gas flow while a variable position gate valve maintains the desired chamber pressure. The structure of the films was studied by θ–2θ and transmission electron microscopy (TEM). The film composition was studied using the XPS technique. Hall mobility and carrier concentration were measured at room temperature using the Van der Pauw configuration at magnetic fields of 0.5 T. Conductivity measurements were carried out using a four-point probe stand, equipped with rounded osmium tips, spaced 1 mm apart.

4.2.2 Discussion

The room temperature deposited $InGaO_3(ZnO)_5$ films when studied using the θ-2θ x-ray showed only the peaks corresponding to the (0006) and (00012) crystal planes from the sapphire substrate. To remove the influence of the substrate, $InGaO_3(ZnO)_5$ were deposited on a glass substrate. Figure 4-1(a) shows the x-ray diffraction pattern of an IGZO film deposited at room temperature and used in this study. The film is amorphous with no obvious crystalline structure. The broad peaks seen are from the glass substrate. In Figure 4-1(b), a cross-sectional high-resolution transmission electron microscopy (HRTEM) image of a TFT

with the IGZO channel shows smooth films and the inset confirms that the IGZO film is essentially amorphous.

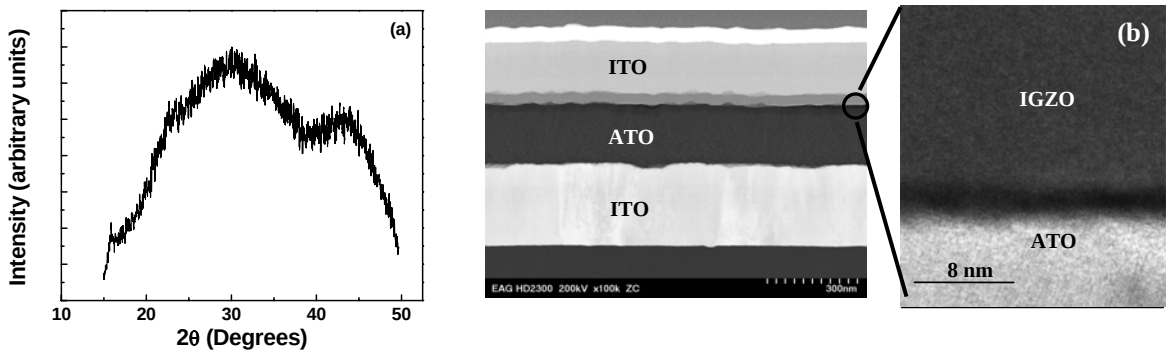

Figure 4-1: (a) Typical XRD pattern of IGZO films. The film is amorphous and the broad peaks are from the glass substrate. (b) Cross-sectional HRTEM micrograph of the TFT layer structure and the magnified image of the ATO/amorphous IGZO interface.

One potential complication of the pulsed laser deposition in the reactive oxygen atmosphere is that the fluctuations in the composition of the films can be influenced by the partial pressure. A set of XPS studies on the films deposited at various oxygen partial pressures showed the films indium to gallium ratio was closer to 1:1.5 than to 1:1 and the indium to gallium ratio decreased slightly with increased oxygen partial pressure. Due to the low melting point of indium the target preparation process likely produced an indium deficient target.

The optical quality of the films was high, with optical transmission for films deposited on double side polished substrates greater than 80 percent throughout the visible spectrum. As shown in the transmission spectra presented in Figure 4-2(a), distinct interference fringes were also observed indicating smooth films with little scatter and a relatively sharp optical absorption edge near 345 nm for the film grown at 20 mTorr. The positions of the optical edges of all of the films grown were blue shifted with respect to the optical edge of single crystal ZnO as shown in Figure 4-2(b) due to the presence of Ga_2O_3 which has a higher bandgap of 4.7 eV [127]. The optical quality and conductivity of the films correlates with the oxygen partial pressure of deposition, with more conductive films having more near infrared absorption (5 mTorr).

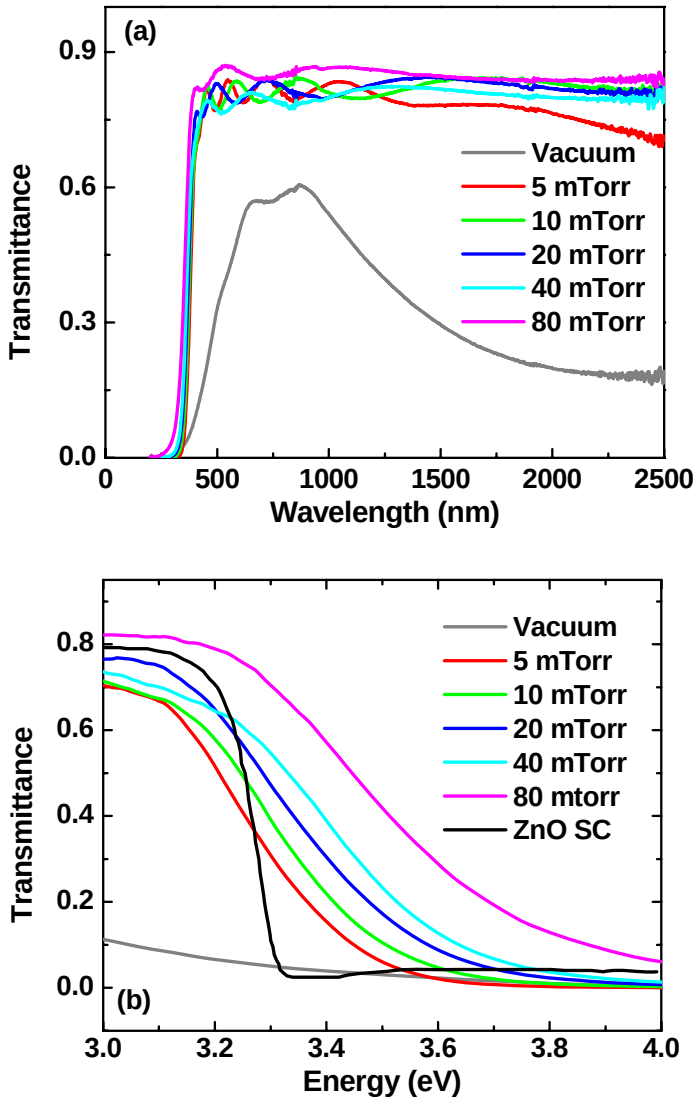

Figure 4-2: (a) Optical transmission spectrum of $InGaO_3(ZnO)_5$ amorphous films deposited at various oxygen partial pressures. **(b)** Comparison of the optical band edge of amorphous $InGa_3(ZnO)_5$ semiconducting films with that of single crystal ZnO.

The optical band edge or Tauc gap of the films also shifted to the red with films deposited at lower oxygen partial pressures. However it is interesting to note that with the exception of the film deposited in vacuum, the optical band edge remains relatively sharp. The increase of the absorption edge energy with increasing oxygen partial pressure may partially be due the decreasing indium to gallium ratio that was observed by XPS. However

the filling of absorptive defect states with oxygen under increased oxygen partial pressure may also have an influence.

The carrier concentration and the Hall mobility of the films, shown in Figure 4-3(a) was found to vary strongly with the oxygen partial pressure of deposition and were found to be n-type in agreement with Takagi *et al*. [128]. The film grown in vacuum was found to be metallic in nature with a carrier concentration of ~ 10^{20} but with lower mobilities (3-4 $cm^2 V^{-1} sec^{-1}$) than films grown in an oxygen partial pressure. The mobility tends to decrease with the carrier concentration in the films. The Hall mobility and carrier concentration of films deposited at pressures greater than 20 mTorr were hard to measure accurately due to the limitations of our Hall measurement system with respect to high resistivity materials.

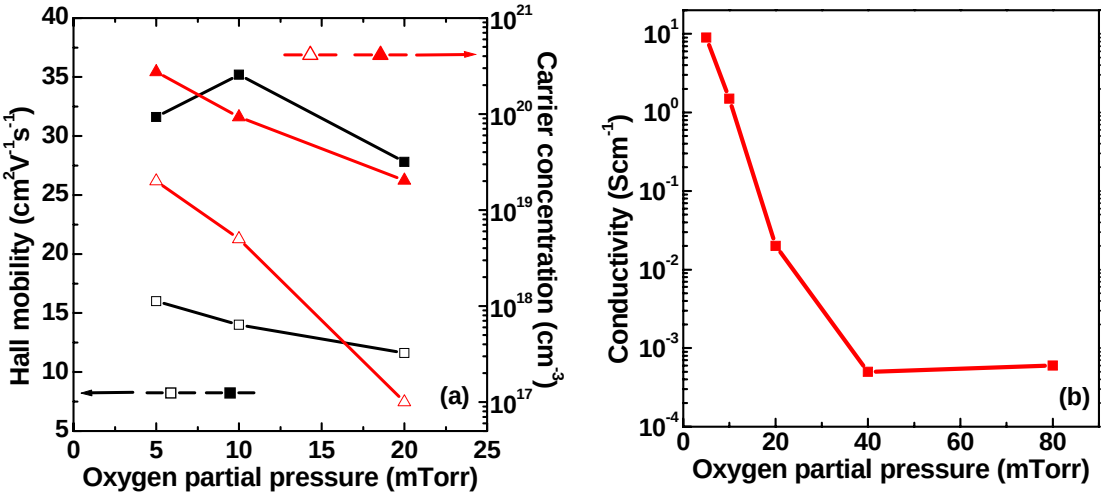

Figure 4-3: (a) Carrier concentration and Hall mobility as a function of oxygen partial pressure during film growth. IGZO film with higher indium concentration (solid) and IGZO composition used in this work (open). (b) Conductivity of IGZO films as a function of oxygen partial pressure during film growth.

The carrier concentration and Hall mobility of an IGZO film with a higher concentration if indium oxide (In_2O_3: Ga_2O_3: ZnO = 1:1:1) is also plotted in Figure 4-3(a) and as expected the Hall mobility was higher. Irrespective of the concentration of the constituent oxides the carrier concentration decreased monotonically as the oxygen partial pressure during deposition increased. By extrapolation, it is assumed that the carrier concentration for the

insulating films was in the 10^{14}-10^{15} carriers/cm^3 range. For semiconducting films grown between 5 and 80 mTorr the conductivity decreased consistently with increasing partial pressure of oxygen as shown in Figure 4-3(b) due to both reductions in the carrier concentration and mobility of the films.

4.3 IGZO thin-film transistors

4.3.1 Experimental Approach

The TFTs fabricated for this study were a bottom-gated structure with the IGZO channel deposited at room temperature by PLD. Two IGZO TFT configurations were studied – transparent TFTs (TTFTs) were fabricated on glass substrates and opaque TFTs were built on Si substrates. The fabrication process and the different TFT components are described in Section 3.6. The growth conditions for the channel layer (IGZO), especially the oxygen partial pressure during deposition and the number of pulses were varied and optimized to give the required carrier concentration and thickness of the film. Three dielectrics were evaluated, ALD ATO, and PECVD SiN_x for TTFTs and ALD AlO_x for IGZO TFTs on Si substrates. TFTs with a series of device dimensions – length (L) and width (W) were fabricated and measured. The capacitance of the gate dielectric (ATO, SiN_x, and AlO_x) was measured using a standard *C-V* meter and a HP4145 parameter analyzer was used to measure the DC *I-V* characteristics of the TFTs. All measurements were carried out in the dark in a double-sweep mode; the gate voltage was swept up and then back down for each drain voltage.

4.3.2 Discussion

Figure 4-4(a) shows the optical transmittance spectrum versus wavelength of the entire IGZO-TTFT stack, (glass/ITO/ATO/IGZO/ITO), and compares it to the substrate, (glass/ITO/ATO). The data represents raw transmission through the entire structure, i.e. the

measured transmission is not corrected for either reflection or absorption. The entire stack was highly transparent at visible wavelengths and the majority of the absorption coming from the ITO contact layer, which was deposited at room temperature. Depositing this layer at elevated temperatures would further improve the transparency, but was not done since the desire was for a room temperature process. Using conducting IGZO source/drain contacts further improved the transparency. The transparency of working transistor chips with different source/drain material is shown in Figure 4-4(b).

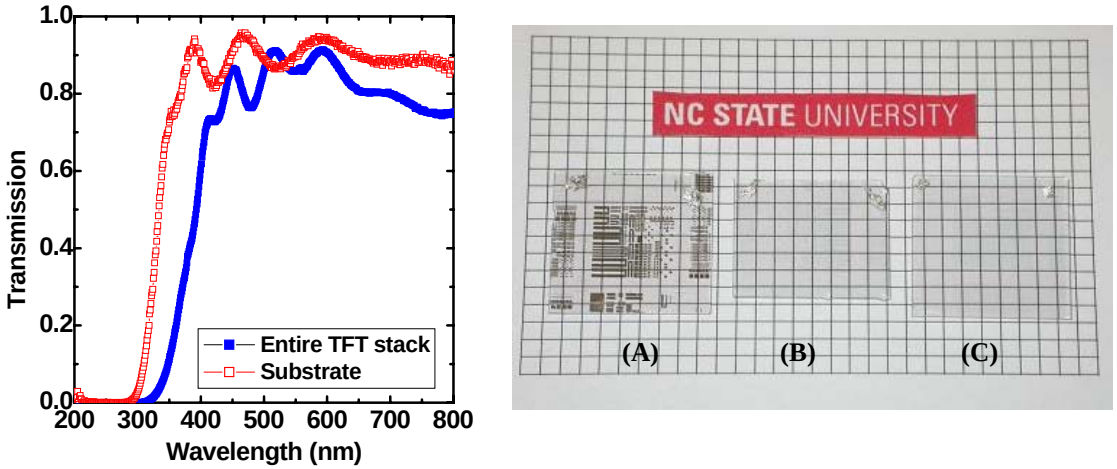

Figure 4-4: (a) Optical transmission spectrum for the complete IGZO TFT stack (solid) and the substrate alone (open). The PLD IGZO and ITO layers do not significantly reduce the transmission in the visible range. (b) The high transmission throughout the visible spectrum can be seen with the chips having functional transistors. The three chips shown have different source/drain material – (A) opaque metal (B) transparent ITO and (C) transparent IGZO.

Figure 4-5(a) illustrates typical DC drain current – drain voltage [$I_{DS} - V_{DS}$] curves for an IGZO TTFT with the channel deposited at an oxygen partial pressure of 25 mTorr and 40 nm in thickness. It can be seen that the drain current exhibits pinch-off and current saturation indicating that the TFT follows standard field effect transistor characteristics. The IGZO TTFT is shown to be an n-type enhancement mode device and hard saturation is achieved, which means that the entire thickness of the IGZO channel layer is depleted of carriers.

A typical DC transfer characteristic [$\log(I_{DS}) - V_{GS}$] and gate leakage current [$\log(|I_G|) - V_{GS}$] of a TTFT with IGZO channel thickness of 40 nm and grown at a oxygen partial pressure of 25 mTorr is shown in Figure 4-5(b). The curves indicate a low off state current of

1 x 10^{-11} A and a drain current on/off ratio of 5 x 10^{7} was obtained. The off-state current matches well with the gate leakage current as seen in Figure 4-5(b). The subthreshold gate voltage swing, S, is given by the maximum slope in the transfer curve and was determined to be 200 mV $decade^{-1}$. The average capacitance of the ATO gate dielectric was measured to be 60 nF cm^{-2}. We extracted a threshold voltage of 2 V and a saturation field effect mobility, μ_{sat} of 11 $cm^2\ V^{-1}\ s^{-1}$. This is comparable to the mobility reported for other oxide based TFTs [52,53,129].

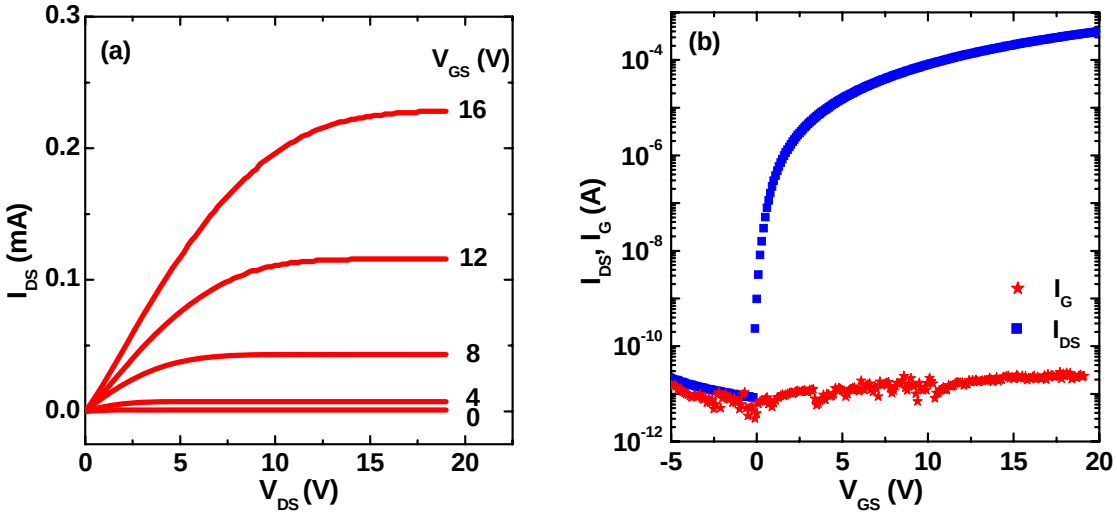

Figure 4-5: (a) Drain current – drain voltage [$I_{DS} - V_{DS}$] characteristics for an IGZO TFT. (b) Log(I_{DS}) – V_{GS} and log(I_G) – V_{GS} at V_{DS} = 20 V for IGZO TFTs. The plot also has the gate leakage, I_G, as a function of the gate bias. IGZO channel has a thickness of 40 nm. The TFT have ATO as the gate dielectric and the IGZO channel is deposited at oxygen partial pressure of 25 mTorr. TFT dimensions, L = 100 µm and W = 400 µm.

The effect of semiconductor layer thickness, t_s, on IGZO TFT performance was carried out. By changing the number of PLD pulses during IGZO deposition, the semiconductor layer thickness was varied and devices with t_s ~ 35 nm, 70 nm, and 130 nm deposited at 25 mTorr oxygen partial pressure were evaluated. The transfer characteristics [log(I_{DS}) – V_{GS}] curves and the average mobility, μ_{avg}, are plotted in Figure 4-6. In general, μ_{avg} does not vary significantly with t_s (~ 10% variation). This is different from a-Si:H and ZIO based TFTs, in which the mobility could vary up to 3 times with t_s [50,130]. In ZIO TFTs, the channel mobility decreases with an increase in t_s and this is attributed to increased source-drain path

length with thicker channels. There is very likely an optimal semiconductor layer thickness below which the mobility would start to decrease, as the carrier flow would tend to get constrained by the thinner channel.

The device parameters extracted from the transfer characteristics are summarized in Table 4-1. The most systematic effect of t_s is on V_{TH} and V_{on} – both V_{TH} and V_{on} decrease with increasing semiconductor layer thickness. V_{on} is a measure of filled and unfilled traps in the device structure [68]. A positive V_{on} indicates that there are unfilled traps and a gate voltage = V_{on} is required to fill the defect states. While a negative V_{on} indicates, carriers are present in the semiconductor before the application of a gate voltage. This would imply a negative gate voltage would be required to completely deplete the channel. It is evident that the TFT with t_s = 130 nm works as a depletion mode device and there is considerable drain current even when the gate voltage is zero. This also shows that changing the channel thickness would be an effective way to engineer the threshold voltage of the TFTs [50,130].

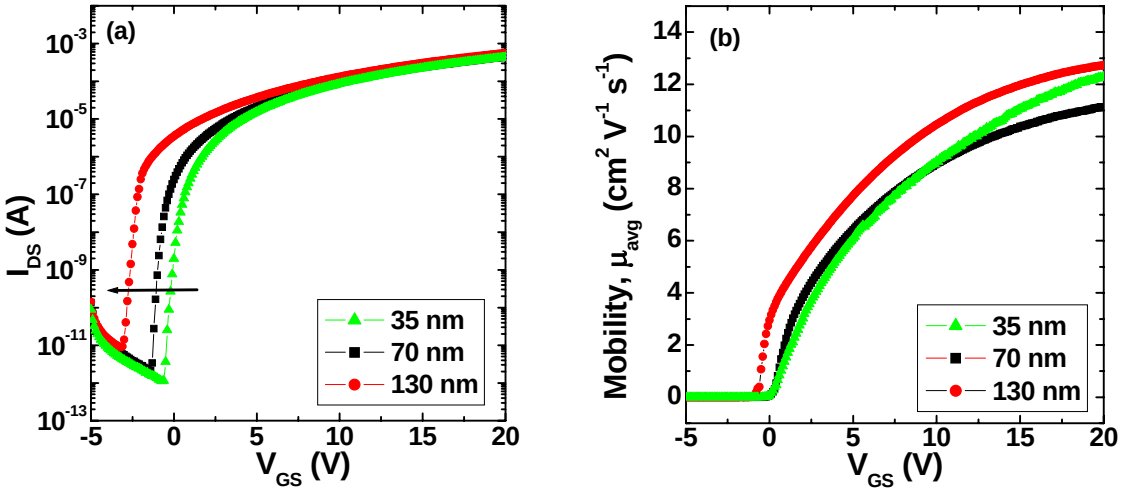

Figure 4-6: (a) Transfer characteristics at V_{DS} = 20 V for IGZO TFTs with varying semiconductor layer thickness, t_s. The arrow indicates the progression of the transfer curves as t_s increases. (b) The extracted average mobility as a function of t_s. The TFT have ATO as the gate dielectric and the IGZO channel is deposited at an oxygen partial pressure of 25 mTorr. TFT dimensions, L = 100 µm and W = 400 µm.

Table 4-1: Device parameters extracted for IGZO TFTs with varying semiconductor layer thickness.

	Channel Thickness (nm)		
	35	70	130
V_{on} (V)	-0.6	-1.4	-3.1
V_{TH} (V)	1.7	1.5	0.35
Subthreshold slope (mV decade^{-1})	180	170	220
Saturation mobility (cm^2 V^{-1} sec^{-1})	11.8	11.7	13
I_{on}/I_{off}	3 x 10^8	2 x 10^8	6 x 10^7

If we model the TFT gate structure as a simple MOS capacitor, the free carrier concentration of the uniformly doped TFT can be estimated by assuming that the turn-on voltage would be the gate voltage when the semiconductor layer is fully depleted. This implies,

$$N_D = \frac{C_{di} V_{on}}{q t_s} \tag{4.1}$$

where C_{di}, is the capacitance per unit area of the gate dielectric, q is the fundamental electron charge, N_D is the channel doping concentration, and t_s is the semiconductor layer thickness. Using data from Table 4-1, N_D is estimated to be ~ 6 – 8 x 10^{16} cm^{-3} which is very similar to the extrapolated values from the Hall measurements shown in Figure 4-3(a).

The effect of the oxygen partial pressure at which the IGZO channel layer is deposited was studied. Figure 4-7(a) compares transistors with AlO_x gate dielectric with IGZO grown at 25 mTorr and 40 mTorr oxygen partial pressure. Few observations can be made from the log(I_{DS}) – V_{GS} curves. First, the turn-on voltages are not very different between the two transistors, V_{on}(25 mTorr) ~ -0.2 V and V_{on}(40 mTorr) ~ 0 V but the subthreshold gate swing is deteriorated for the TFT with the 40 mTorr channel, S(25 mTorr) ~ 175 mV decade^{-1} and S(40 mTorr) ~ 250 mV decade^{-1}. Moreover, a large clockwise hysteresis is seen in the transfer curve of the 40 mTorr channel TFT while the 25 mTorr channel showed negligible hysteresis. This along with the poor subthreshold slope indicates that the defect or trap

density at the gate dielectric/IGZO channel interface is larger for the 40 mTorr compared to the 25 mTorr TFT. The drain current for the 40 mTorr IGZO TFTs is considerably lower compared to the 25 mTorr IGZO TFTs. The extracted average mobility of the TFTs is plotted in Figure 4-7(b). It is clearly evident that the 25 mTorr TFT has a superior mobility. We have earlier showed a monotonically decreasing Hall mobility of the IGZO films with an increase in the deposition oxygen partial pressure and the extracted mobility scales well with the data from Figure 4-3(a). A similar *I-V* behavior was observed in TFTs with ATO and SiN_x gate dielectrics as well.

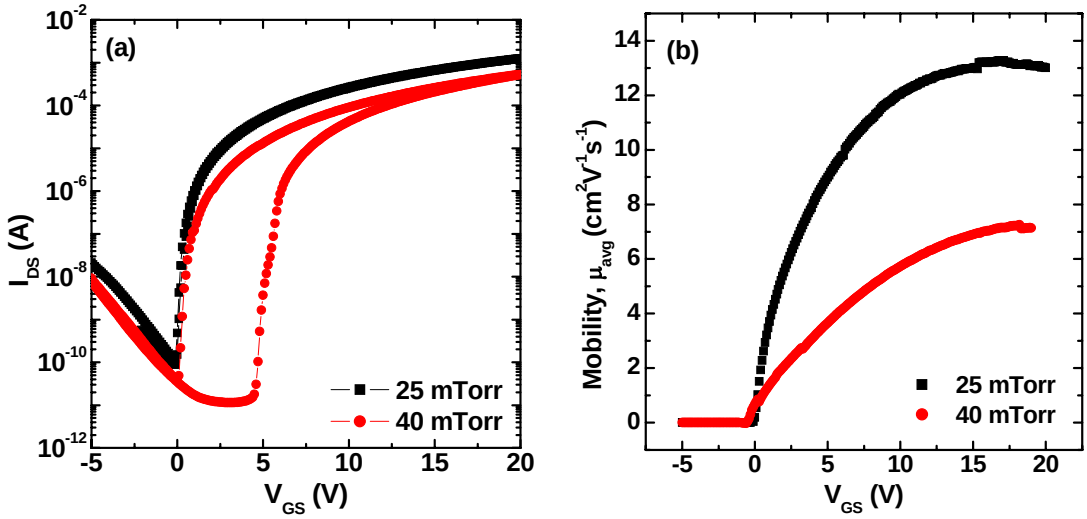

Figure 4-7: (a) Transfer characteristics at V_{DS} = 20 V for IGZO TFTs with AlO_x gate dielectric both in the forward and reverse V_{GS} sweeps. IGZO channel deposited at oxygen partial pressure of 25 mTorr and 40 mTorr. The TFT with the 40 mTorr IGZO layer shows a clockwise hysteresis. (b) The extracted average mobility for the 25 mTorr and 40 mTorr channel TFTs. Semiconductor layer thickness of 40 nm and TFT dimensions of L = 100 μm and W = 400 μm.

In general, TFT electrical behavior and hence the field effect mobility strongly depend on the gate dielectric material and thereby the dielectric/semiconductor layer interface. To evaluate the effect of the gate dielectric, three dielectrics were studied ATO, PECVD SiN_x and ALD AlO_x. For the channel layer IGZO films, 40 nm thick were grown at an oxygen partial pressure of 25 mTorr. The $\log(I_{DS}) - V_{GS}$ characteristics for SiN_x and the ATO gate dielectric transistors are compared in Figure 4-8. We observe that for the SiN_x TFT the

threshold voltage was lower compared to the ATO TFT. The saturation field effect mobility for the SiNx transistors, with a capacitance per unit area 22 nF cm^{-2}, was 4 $cm^2 V^{-1} s^{-1}$ and the inverse subthreshold voltage slope was 400 mV $decade^{-1}$ and inferior to the ATO transistors. We also observed a hysteresis in the forward and reverse voltage sweeps for the $V_{GS} - I_{DS}$ measurement for SiN_x gated transistors while no significant hysteresis was observed in the ATO gated TFTs. Similar gate dielectric dependent observations have been reported in TFTs based on other material systems [52,131]. The device parameters extracted for the IGZO TFTs with ATO, SiN_x and AlO_x gate dielectric are summarized in Table 4-2.

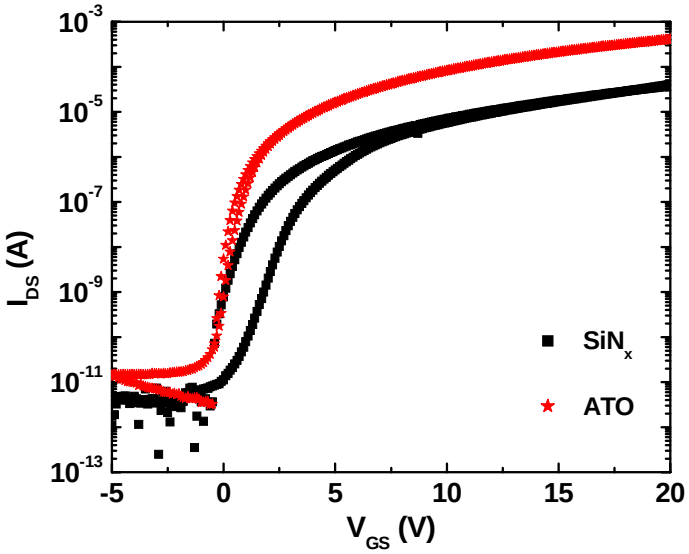

Figure 4-8: Comparing transfer characteristics at V_{DS} = 20 V for IGZO TFTs with ATO and SiN_x gate dielectrics both in the forward and reverse V_{GS} sweeps. IGZO channel deposited at oxygen partial pressure of 25 mTorr. The TFT with the SiN_x gate dielectric shows a significant clockwise hysteresis. Semiconductor layer thickness of 40 nm and TFT dimensions of L = 100 μm and W = 400 μm.

Another reason for the importance of the gate dielectric is that these TFTs are essentially surface channel devices whose action depends on the formation of an electron channel at the gate interface between the gate dielectric and the active layer. In the output characteristics measurements in ATO gated IGZO TFTs, it was observed that at higher gate bias, for example greater than 24 volts, that for a given step change in gate voltage the separation in saturation current I_{DS} curves decreased. This non-ideality in the I_{DS}-V_{DS} characteristics

implies a lower effective mobility at higher gate biases. This is consistent with carrier scattering at the interface as the electron channel narrows at a higher gate bias [49].

A straightforward way to improve TFT performance is to increase the gate capacitance density. This leads to a higher drive current, a decrease in the subthreshold swing and possibility of making the turn-on voltage very close to zero volts. An ALD AlO_x gate dielectric with a capacitance per unit area of 120 nF cm^{-2} was used and the transistor characteristics are tabulated in Table 4-2. Developing dielectrics with such large capacitance densities along with the high mobility of IGZO should result in lowering of the operating voltages of IGZO TFTs. Figure 4-9 shows the output characteristics and hysteresis transfer characteristics of AlO_x gated IGZO TFTs at low operating voltages.

Table 4-2: Device parameters extracted for IGZO TFTs with different gate dielectrics.

	Gate Dielectric		
	ATO	SiN_x	AlO_x
V_{on} (V)	-0.5	-0.7	-0.2
V_{TH} (V)	1.7	2.9	1.2
Subthreshold slope (mV decade^{-1})	190	375	175
Saturation Mobility (cm^2 V^{-1} sec^{-1})	11.2	4	14.7
I_{on}/I_{off}	2×10^8	1×10^7	1×10^7
Hysteresis window (V)	0.2	1.7	0.07

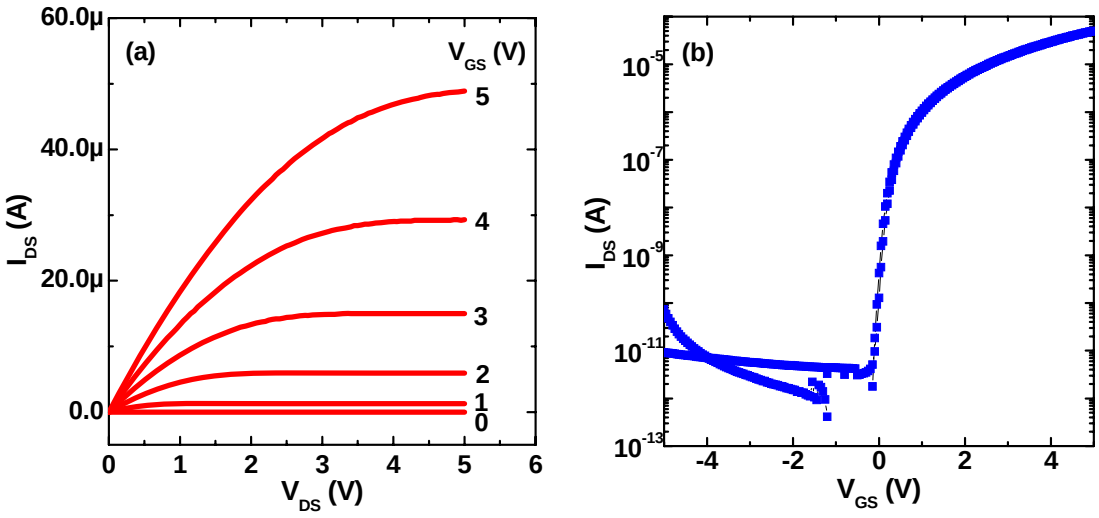

Figure 4-9: (a) Output characteristics and (b) Transfer characteristics at V_{DS} = 5 V of AlO_x gated IGZO TFTs both in the forward and reverse V_{GS} sweeps. Plots indicate the capability of IGZO TFTs to be operated at low voltages. IGZO deposited at an oxygen partial pressure of 25 mTorr and a thickness of 40 nm. TFT dimensions of L=100 µm and W=400 µm.

Hard saturation is evident and a enhancement mode device with a V_{on} close to 0 V and a low off-state current of 1 x 10^{-11} A which is essentially the gate leakage current and a drain current on/off ratio ~ 3 x 10^{7} was obtained. The subthreshold gate voltage swing, S, was determined to be 90 mVdecade^{-1}. We extracted a threshold voltage of 0.6 V and a saturation field effect mobility of 12 cm^2 V^{-1} s^{-1}. A small clockwise hysteresis window of ~ 0.03 V is observed when the gate voltage was swept in the forward and reverse directions. This is a sign of low trap densities at the semiconductor/dielectric interface.

In ideal thin-film transistors, the source and drain (*S/D*) contacts are assumed to be Ohmic, but in reality some parasitic resistance is always present at the *S/D* contacts and the semiconductor layer. In long-channel devices this parasitic resistance could be a small fraction of the total resistance, R_T, of the TFT, but it may become significant as the channel length of the devices shrink. The channel resistance method [132] was utilized to evaluate the parasitic resistances present in IGZO TFTs grown at 25 mTorr and a channel thickness of ~ 35 nm. The parasitic source-to-drain resistance, R_{SD}, and the effective channel length, L_{eff}, were evaluated with TFTs having different designed channel lengths, L_d. Figure 4-10 shows

the transfer characteristics of TFTs with W = 100 μm and different L_d (L_d = 4 – 50 μm) measured in the linear regime at V_{DS} = 0.1 V.

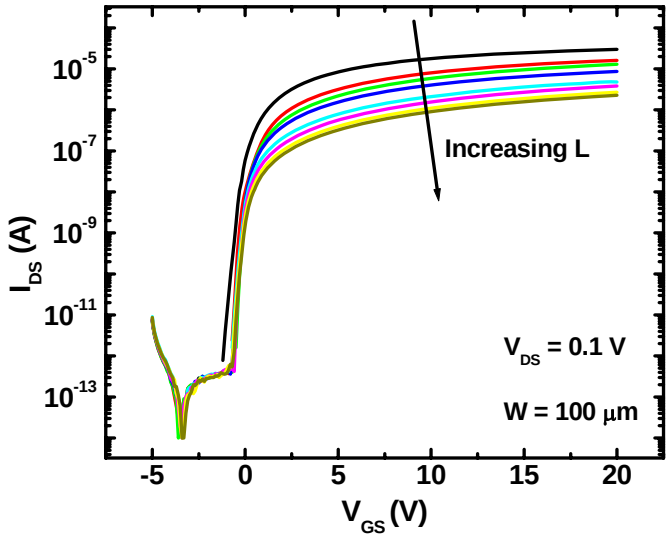

Figure 4-10: Transfer characteristics of ATO gated IGZO TFTs with various designed channel lengths, L_d, and W = 100 μm at V_{DS} = 0.1 V. The IGZO channel is grown at 25 mTorr and with a thickness of ~ 35 nm. The arrow indicates the direction of increasing channel length, L.

Using the curves in Figure 4-10 at $V_{GS} >> V_{DS}$, the total device resistance, R_T, of the TFTs and L_{eff} are given by,

$$R_T = \frac{V_{DS}}{I_{DS}} = R_{SD} + \frac{L_d - \Delta L}{\mu_{eff} C_{di} W (V_{GS} - V_{TH})} \qquad (4.2)$$

where ΔL is defined as L_d - L_{eff}, μ_{eff} is the effective mobility and C_{di} is the capacitance per unit area of the gate dielectric. Figure 4-11(a) shows the dependence of R_T on L_d at different values of V_{GS}. Using Eqn. 4.2, R_{SD} and ΔL values were extracted from the intersection point of the straight lines shown in Figure 4-11(b). A value of 2300 Ω was extracted, which when normalized for the width of the TFTs ($R_{SD}W$) gave a resistance of 23 Ω cm. This value is similar to the ones reported by Sato *et al*. (34 Ω cm) [133] and Jeong *et al*. (25 Ω cm) [134] but it is much lower than those reported by Kim *et al*. (113 Ω cm) [95] and Park *et al*. (330 Ω cm) [94]. This indicates that the ITO forms good Ohmic contacts with very low parasitic resistance with the IGZO channel in our TFTs. The major contribution to the contact

resistance is due to the resistance to access the IGZO channel layer rather than S/D – IGZO interface resistance. A ΔL value of ~ 1 μm was also recorded which is the shrinkage of the channel and can be attributed to the loss of critical-dimension (designed channel length) during pattering using the lift-off process.

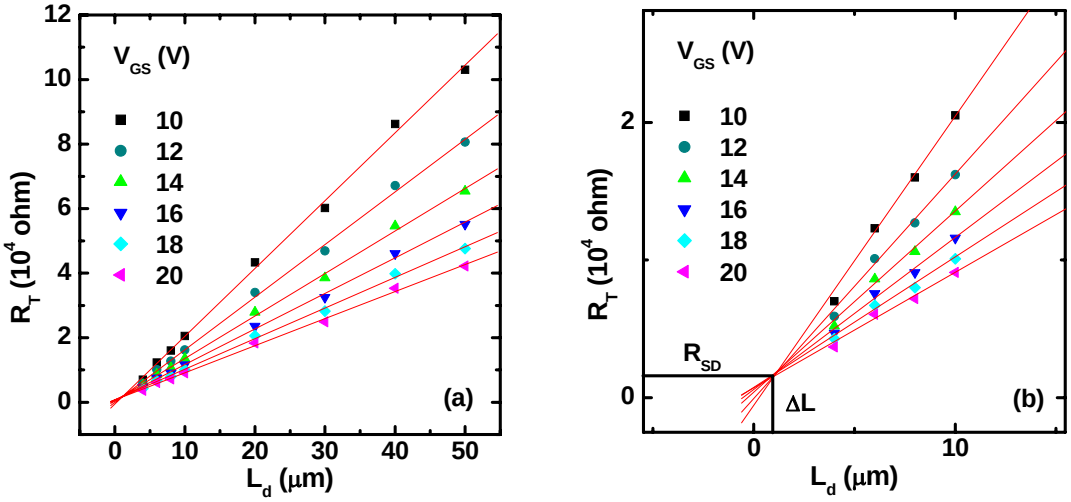

Figure 4-11: (a) Total device resistance, R_T, as a function of TFT channel length, L, and V_{GS}. (b) Magnified view of (a) in the small L region. The point of intersection of the lines gives R_{SD} and ΔL. Data extracted from curves in Figure 4-10.

Figure 4-12 plots the transconductance $g_m = \partial I_{DS}/\partial V_{GS}$ as a function of the inverse channel length, L^{-1}, and the field-effect mobility $\mu_{FE} = g_m/((W/L)C_{di}V_{DS})$ as a function of L. It can be seen that g_m is linearly dependent on L^{-1} implying that the g_m is maximized; this is another consequence of achieving small values of $R_{SD}W$. The field-effect mobility shows a channel-length independent behavior for long-channel TFTs and for short-channel TFTs the mobility shows a trend to decrease slightly with decreasing L, which can be attributed to the influence of R_{SD}. The mobility changes ~ 10% as the TFT channel length varies between 50 μm to 4 μm.

It should be pointed out that so far in this study all the PLD depositions to fabricate IGZO TFTs have been at room temperature with no post-deposition annealing. Owing to the relatively low temperature of processing, TFTs based on the IGZO system can be fabricated on flexible substrates such as polyethylene theraphthalate (PET). A PET substrate coated

with ITO from Sigma Aldrich was used and mounted on a piece of silicon to improve handling of the sample. PECVD SiN_x deposited at 175 ^oC was used as

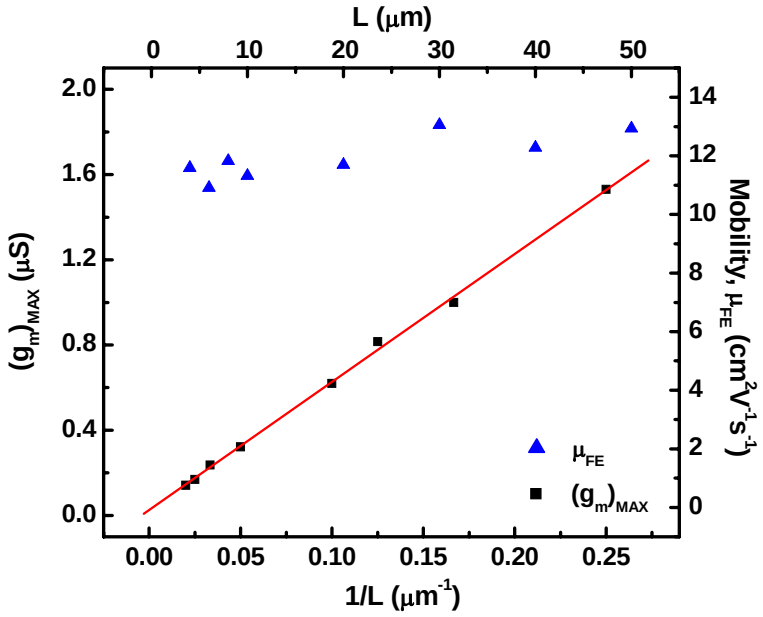

Figure 4-12: Transconductance, g_m, versus the inverse channel length, L^{-1}, (lover abscissa) and the filed-effect mobility, μ_{FE}, versus the channel length, L, (upper abscissa). The linear trend between g_m and L^{-1} is observed.

the gate dielectric. The channel layer and the source and drain electrodes were processed using a lift-off process similar to the IGZO TFTs made on glass substrates. A picture of the fabricated chip with working IGZO transistors on a PET substrate is shown in Figure 4-13.

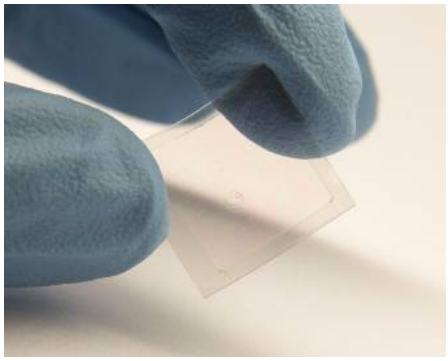

Figure 4-13: Transparent IGZO TFTs fabricated on a flexible PET substrate. A bottom gated structure similar to TFTs fabricated on glass substrates was used. A low temperature PECVD SiN_x deposited at 175 ^{o}C was used as the gate dielectric.

Figure 4-14 shows the output characteristics and hysteresis transfer characteristics of IGZO TFTs on flexible PET substrates. The following electrical parameters were extracted – V_{on} ~ -2.6 V, V_{TH} ~ -0.5, S ~ 430 mV decade^{-1}, I_{on}/I_{off} ~ 1 x10^{7} and μ_{sat} ~ 7 cm^{2} V^{-1} s^{-1}. The transistors show good electrical characteristics with low leakage currents, high on/off ratios and good saturation behavior. This shows that the process is compatible with flexible substrates as well.

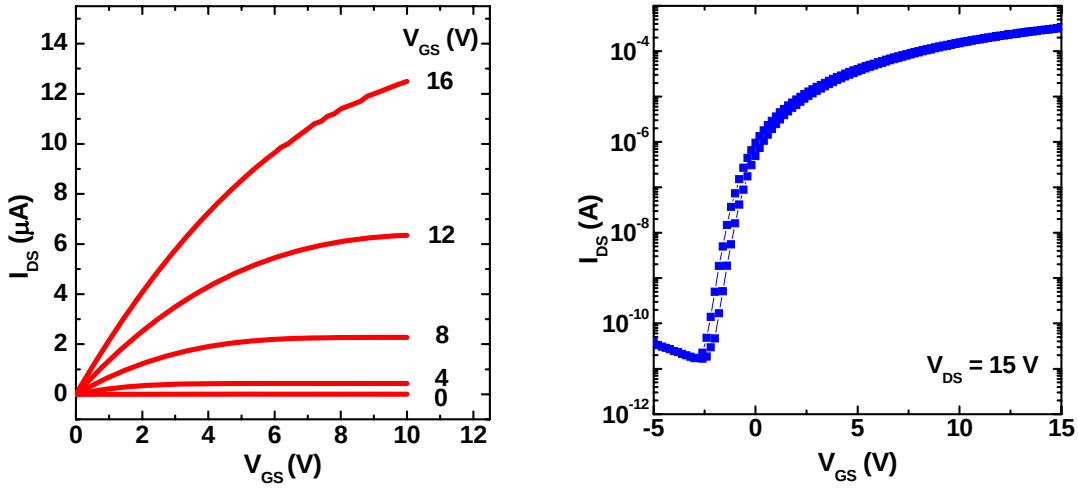

Figure 4-14: (a) Output characteristics and (b) Transfer characteristics at V_{DS} = 15 V of IGZO TFTs on a PET substrate with a SiN_x dielectric both in the forward and reverse V_{GS} sweeps. IGZO deposited at an oxygen partial pressure of 25 mTorr and a thickness of 40 nm. TFT dimensions of L=100 μm and W=400 μm.

4.4 Conclusions

Highly optical quality, high mobility, $InGaO_3(ZnO)_5$ films have been deposited by PLD at room temperature. The electronic properties of the films were found to be controllable by varying the partial pressure of oxygen in the deposition chamber. The mobility demonstrated by these films is over an order of magnitude higher than that of amorphous silicon. Optically, the deposited films were all highly transparent throughout the visible region and into the near-infrared. Optimized IGZO films are used as a channel to construct transparent TFTs. The devices exhibit good electrical characteristics. The effect of deposition and device parameters along with the effect of the gate dielectric on the TFT behavior was studied.

CHAPTER 5

BIAS STRESS STABILITY OF TRANSPARENT INDIUM GALLIUM ZINC OXIDE THIN-FILM TRANSISTORS

Based on the manuscript:

Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors

A. Suresh, and J. F. Muth

Applied Physics Letters, **92**, 033502 (2008).

5.1 Abstract

The effects of bias stress on transistor performance are important when considering new channel materials for thin film transistors. In this chapter, the bias stress stability of indium gallium zinc oxide (IGZO) TFTs are evaluated. This study reveals that the effects of a constant gate bias stress and the resulting shifts in threshold voltage can be explained using a simple charge-trapping model. Applying a positive gate bias stress was found to induce a parallel threshold voltage shift without changing the field effect mobility or the subthreshold gate voltage swing. The threshold voltage change is logarithmically dependent on the duration of the bias stress implying a charge tunneling mechanism resulting in trapped negative charge screening the applied gate voltage. This time dependence was verified for both short and long stress durations. When the bias stress is removed, the voltage threshold recovers to its original value.

5.2 Experimental Approach

Transparent IGZO (In_2O_3:Ga_2O_3:ZnO = 1:1:10 mol%) thin film transistors (TFTs) were fabricated using a bottom gated configuration with the following elements – indium tin oxide, ITO (gate electrode ~ 250 nm), AlO_x and TiO_x superlattice, ATO (gate dielectric, C_{di} – 60 nF cm^{-2}, ~ 220 nm), IGZO (channel ~ 40 nm) and ITO (source and drain electrodes ~ 175 nm). The fabrication details are discussed in Section 3-1. The IGZO channel and the ITO source and drain were deposited using pulsed laser deposition (PLD) at room temperature. Good transistor characteristics were obtained without any annealing of the films, although as discussed later improvements in reducing the threshold voltage shift due to applied bias stress were obtained by post annealing the transistors. To obtain optimal TFT characteristics the oxygen pressure used during the IGZO deposition was set at 25 mTorr. Transistors used in the study operate as an n-channel enhancement mode device and exhibit good characteristics, with an extracted field effect mobility of ~ 14 $cm^2 V^{-1} s^{-1}$, drain current on/off ratios > 10^7, low off-state currents and good saturation. The TFT dimensions used for the bias stress study was100x400 μm^2 *(LxW)*. All the stress bias measurements were carried out at room temperature, in air and in the dark and a "virgin" device was used for each stressing condition. Gate bias stress was carried out for a predetermined time with the bias stress voltage in the linear regime using a V_{DS} of 1 V. The linear regime was chosen instead of the saturation regime because the effect of bias stress on the threshold voltage shift is smaller in the saturation regime [135]. The transfer characteristics were measured before and after applying the stress in a dual sweep mode. The threshold voltage V_{TH}, was extracted from the $\sqrt{I_{DS}}$ vs. V_{GS} plots. *I-V* characteristics of the transistors were measured on a semiconductor parameter analyzer, Keithley 4200 and the *C-V* measurements were carried out on a LCR meter, HP 4284A.

5.3 Discussion

Figure 5-1(a) shows two transfer characteristics of the same TFT device. After the first gate voltage sweep, the gate electrode was stressed at 30 V for 500 s. Following this the second gate voltage sweep was performed. It can be seen that the transfer characteristics [log (I_{DS}) – V_{GS}] of the device before and after the bias stress have a similar shape except for a parallel shift along the gate voltage axis in the positive direction, this is the typical threshold voltage shift seen in TFTs after bias stressing. Figure 5-1(a) also shows that the sub-threshold slope of the device (~ 250 mV decade^{-1}) does not change even after the device has undergone bias stressing. This indicates that no new defect states are created at the channel/dielectric interface after the device was stressed [136]. This is important since the issue of defect state creation in a-Si:H devices leads to poor bias stress stability and indicates the suitability of oxide semiconductors for TFT applications.

Figure 5-1(b) shows the plot of the square root of the drain current as a function of the applied gate bias. From the plot it is clear that the slope of the linear part of the curve, which is proportional to the field-effect mobility in the saturation regime, is similar for both curves. The extracted saturation field-effect mobility (~ 14 cm^2 V^{-1} sec^{-1}) seems to remain unaltered even after the application of gate bias stress. The phenomenon of a positive threshold voltage shift with an applied positive gate bias results from negative charge being trapped at the semiconductor channel/dielectric interface or getting injected into the gate dielectric. The positive threshold voltage shift is then explained by the negative charge screening the applied gate voltage. The lower effective gate bias results in a smaller current flowing through the channel, thus a larger positive voltage is required for the device to turn on and reach saturation.

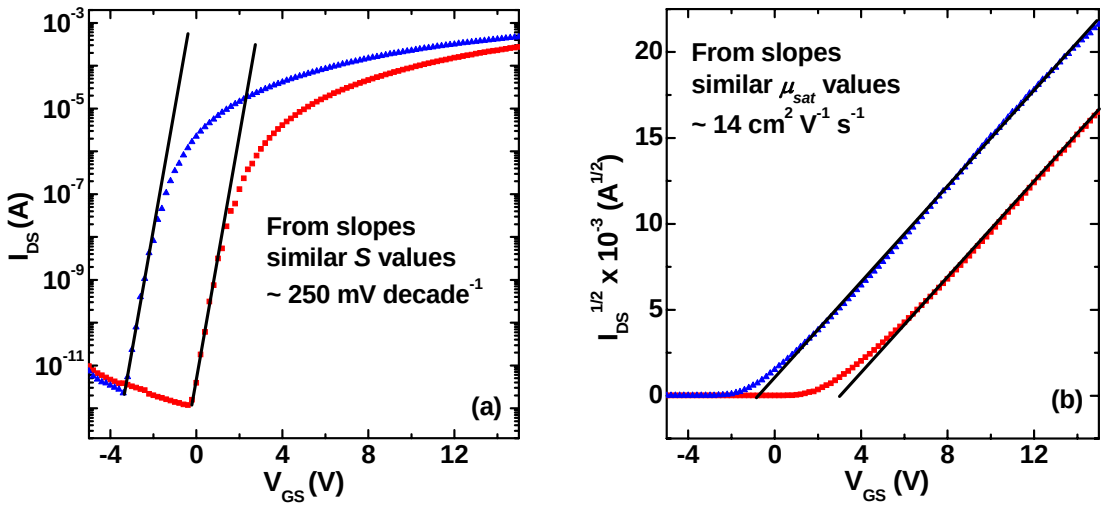

Figure 5-1: Effect of bias stress on the drain current, the field effect mobility and the sub-threshold voltage swing of the TFT. 30 V bias stress was applied on the gate electrode for 500 s, while the V_{DS} was kept at 1 V. The log(I_{DS}) - V_{GS} sweep was done at V_{DS} = 15 V. (▲ – pre stress, and ■ – post stress). Only the forward sweep has been plotted.

Figure 5-2 shows the room temperature C-V measurement of the ITO/ATO/IGZO/ITO capacitor structure. The capacitor was subjected to three back-to-back hysteresis loop sweeps of V_G = -10 to 10 V, -20 to 20 V, and -30 to 30 V. From Figure 5-2 we observe that the flat band voltage, V_{FB}, shifts successively to more positive voltage for each hysteresis loop during the return sweep. This is additional evidence that negative carriers are trapped at the channel/dielectric interface or injected into the dielectric from the IGZO channel. Also note that the forward sweep of curves, -20 to 20 V, and -30 to 30 V fall on the previous curves reverse sweep (i.e., -10 to 10 V, and -20 to 20 V respectively). This indicates that when a negative bias is applied to the gate no positive charges are injected from the IGZO channel into the gate dielectric and the capacitor maintains its characteristics from the positive part of the previous hysteresis loop. The slope of the curves in the transition region from accumulation to depletion is the same as that from depletion to accumulation, indicating that the bias stress does not change the trap density at the channel/dielectric interface.

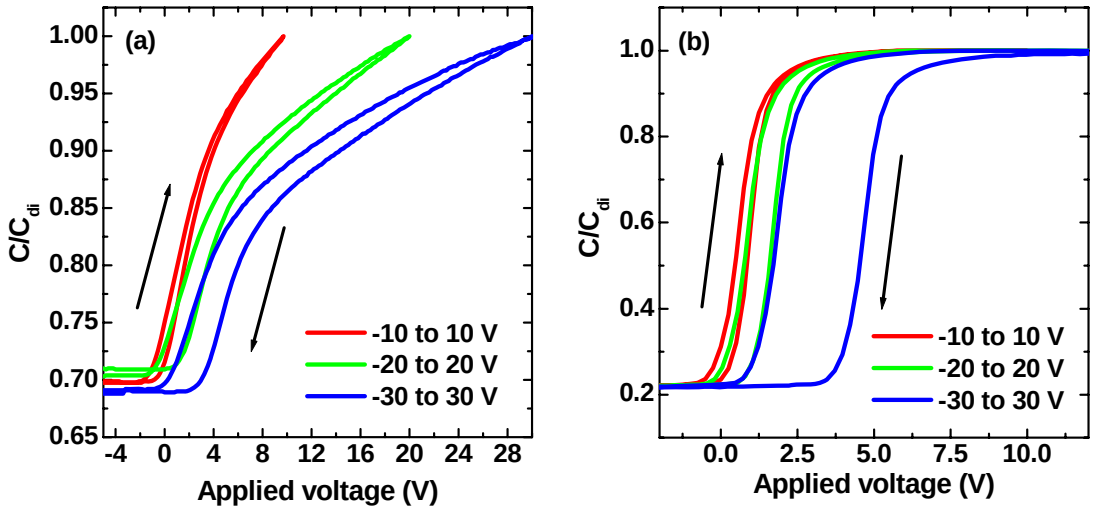

Figure 5-2: Hysteresis behavior of ITO/ATO/IGZO/ITO capacitor structure. Hysteresis sweeps -10 to 10 V, -20 to 20 V and -30 to 30 V were made consecutively. The size of the capacitor pad is 200x1600 μm^2. The directions of the forward and reverse sweeps are indicated. Measurements were carried out at (a) 1 MHz and (b) 1 KHz. Note the expanded scale in (b).

This was further verified by applying negative voltages as a bias stress. Figure 5-3 compares two TFTs, one having been subjected to a positive gate bias stress while the other undergoes a negative gate bias stress. It can be seen that as expected the positive bias stress causes a positive threshold voltage shift ΔV_{TH}, where $\Delta V_{TH} = V_{TH}(t) - V_{TH}(t=0)$ while the negative gate bias stress doesn't change the threshold voltage and the transfer curve of the stressed TFT overlaps that of the unstressed TFT. This is an indication that when a negative bias is applied to the gate, the transistor channel is depleted of electrons at the channel/dielectric interface and no mobile charges are available for the charge trapping and tunneling process.

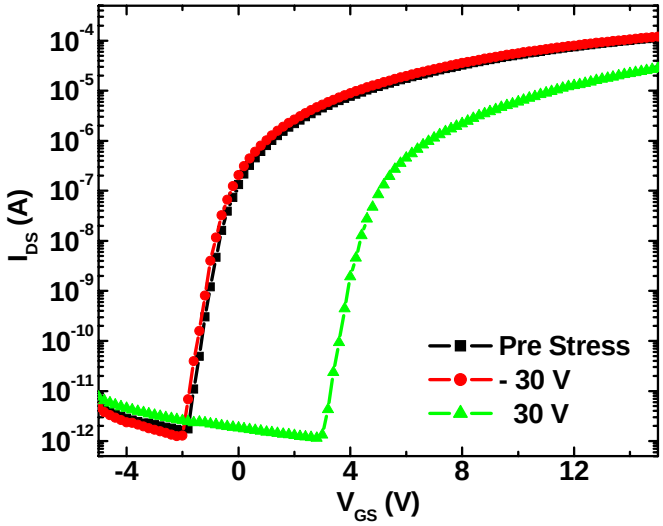

Figure 5-3: Comparison of the effect of positive and a negative gate bias stress on the transfer characteristics. Stress duration was 1000 s, V_{DS} = 1 V. The log(I_{DS}) - V_{GS} sweep was done at V_{DS} = 15 V. (■ – pre stress, ▲ – after +30 V stress, and ● – after -30 V stress).

The dependence of the threshold voltage shift on the duration of the applied gate bias is plotted in Figure 5-4 for different gate stress voltages. From the plot a linear relationship between ΔV_{TH} and logarithmic time can be seen. Figure 5-4(b) shows a similar trend even for longer stress durations for the sample stress biased at 10 V. This dependence is indicative of charge trapping phenomenon [115]. The relationship can be modeled by quantifying the total charge that get trapped at the channel/dielectric interface or in the dielectric for any given time *t*. Given the material parameters (work function, capacitance etc.) are invariant during biasing, the ΔV_{TH} can be expressed as,

$$\Delta V_{TH}(t) = Q(t)/C_{di} \tag{5.1}$$

where *Q(t)* is the total charge trapped and C_{di} is the capacitance per unit area of the gate dielectric. By assuming a uniform distribution of traps in the dielectric, an expression for the total trapped charge is obtained by integrating over time and thickness of the gate dielectric in which traps are present [137],

$$Q(t) = \int_0^t dt' \int_0^x dx' N_{tr} \varpi(x') \exp[-\varpi(x')t'] \tag{5.2}$$

N_{tr} is the density of traps in the dielectric and $\varpi(x) = \varpi_0 \exp(-x/\lambda)$ is the time independent tunneling probability, where the tunneling constant λ is the product of the applied gate voltage and dielectric material parameters. The solution of the above equation leads to the ΔV_{TH} expression given below,

$$\Delta V_{TH} = r_o \log\left(\frac{t}{t_0}\right) \tag{5.3}$$

where r_o is a decay rate constant which is proportional to the product of N_{tr} (cm^{-3}) and λ (cm). Since λ is dependent on the applied gate voltage, higher bias stresses will result in more charge trapping, larger decay rate constants and larger voltage shifts.

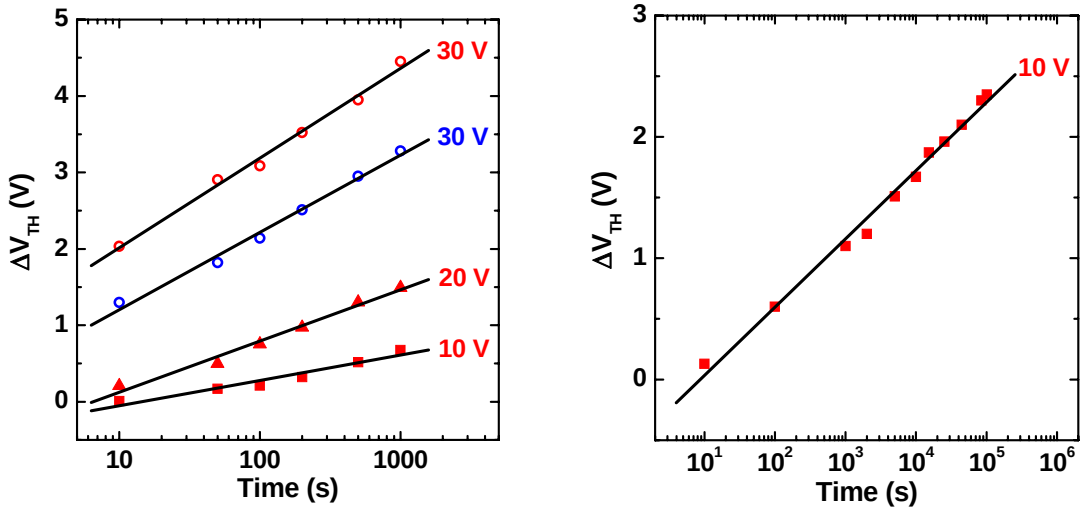

Figure 5-4: (a) Logarithmic dependence of the threshold voltage shift, ΔV_{TH} with the bias stress duration. The effect of the gate voltage is seen as well (■ – 10V, ● – 20V and ○ – 30V). ΔV_{TH} for TFTs bias stressed at 30 V based on an IGZO channel grown at (○) 40 mTorr is plotted as well. (b) Logarithmic dependence seen for a 10 V gate bias for longer stress durations.

One-way to reduce the threshold voltage shift during bias stressing would be to reduce the mobile carriers in the channel. We have previously discussed the effect of oxygen partial pressure during the PLD deposition of IGZO on the carrier concentration and mobility of the films in Chapter 4. Films grown at a higher oxygen partial pressure tend to have lower carrier concentration. The effect of IGZO growth conditions on ΔV_{TH} is also shown in Figure 5-4(a).

We can clearly see that the TFT fabricated with a 40 mTorr channel is less sensitive to gate bias stress with lower threshold voltage shifts. Varying the oxygen partial pressure during deposition of the channel slightly changes the composition of the film, this in itself could very well affect the channel/dielectric interface by changing the density of the interface states and thereby bringing about a reduction in the threshold voltage shifts. It should be noted that the decay rate constant appears to be a strong function of the applied gate bias.

Annealing the IGZO films at temperatures as low as 200 ^{o}C in atmosphere for a few minutes leads to a drop in the carrier concentration. The highest temperature the as fabricated transistors were exposed to during processing is a 95 ^{0}C photoresist bake step. To investigate the effect of post deposition annealing, TFTs fabricated with a 25 mTorr channel were annealed at 200 ^{o}C for 10 min in atmosphere. Bias stress data was measured before and after anneal. It was found that the ΔV_{TH} reduced from 4.6 V to 3 V for a bias stress of 30V and duration of 1000 s. This suggests that improvements in the channel/dielectric interface can be obtained, via reduction in charge trapping defects, with some improvement also resulting from a reduction in carrier concentration. A vast majority of the reports on oxide semiconductor based TFTs involve some form of post-deposition/fabrication anneal which shows a large improvement in the TFT characteristics [101,16,118].

The threshold voltage, V_{TH} can be recovered to the original value if the device is left unbiased. Also, charge trapped at the channel/dielectric interface appears to have the same effect as charge injected into the dielectric on the electrical characteristics of the TFT. This suggests that temperature dependent studies to determine the kinetics of the charge trapping would help in understanding the details of the threshold voltage shift and recovery.

5.4 Conclusions

In conclusion, we have investigated the effects of gate bias stress on IGZO thin film transistors. A threshold voltage shift (ΔV_{TH}) was observed as a result of bias stress, and this shift was quantified as a function of bias stress voltage and duration. Both *I-V* and *C-V* measurements were used to determine that the voltage instability arises due to the process of

charge trapping in the channel/dielectric interface or in the dielectric due to bias stressing. The ΔV_{TH} as a function of the stress duration was modeled using basic electrostatic considerations.

CHAPTER 6

INDIUM GALLIUM ZINC OXIDE TRANSISTOR BASED FLOATING GATE MEMORY

Based on manuscripts:

Transparent Indium Gallium Zinc Oxide Transistor based Floating Gate Memory with Platinum Nano-particles in the Gate Dielectric

A. Suresh, S. Novak, P. Wellenius, V. Misra, and J. F. Muth

Applied Physics Letters, **94**, 123501 (2009).

Transparent Non-volatile Memory using Pt Nano-particles embedded in an Amorphous Indium Gallium Zinc Oxide Thin Film Transistor

A. Suresh, S. Novak, P. Wellenius, V. Misra, L. M. Lunardi, and J. F. Muth

Presented at *MRS Fall 2008*, Manuscript under review.

6.1 Abstract

This chapter deals with the development of a transparent memory element based on an indium gallium zinc oxide thin-film transistor. Atomic layer deposited platinum nano-particles are incorporated in the gate dielectric stack of the transistor, which acts as a floating gate and a charge storage medium. The transfer characteristics of the device show a large clockwise hysteresis due to electron trapping and are attributed to the platinum nano-particles. The presence of the platinum nano-particles is characterized by various techniques. The effect of the gate bias stress (program voltage) magnitude, duration and polarity on the memory window characteristics has been studied. Charge retention measurements were carried out and a loss of less than 25% of the trapped electrons was observed over 10^4 s

indicating promising application as non-volatile memory. One of the characteristics of the device is that it cannot be completely erased using a Fowler-Nordheim biasing scheme. This asymmetric program/erase characteristic has been explained taking into account the relative band offsets of the various components of the device. The use of ultraviolet light is shown to erase the memory.

6.2 Experimental approach

Two device structures were studied, (a) completely transparent memory based on the ATO TTFT, and an opaque TFT memory fabricated on a silicon substrate, based on the device structures described in Section 3.6. The ATO (220 nm) and the AlO_x (50 nm) layers act as the blocking oxide of the devices, respectively. Before the IGZO channel is deposited, Pt-NPs were formed on the blocking oxide (ATO or AlO_x) at 270 ^oC using the precursor $MeCpPtMe_3$ and high purity oxygen [138]. The initial nucleation of the Pt film produces small, disbursed crystals, which can be grown further with subsequent ALD cycles. Next a thin layer, ~ 7 nm, of AlO_x was deposited at 200 ^oC by ALD, which acts as the tunneling oxide. This was followed by the deposition and patterning of IGZO (channel) and ITO (source/drain) by pulsed laser deposition (PLD) at room temperature using standard photolithography and liftoff. The IGZO and ITO layers were grown at 25 mTorr (~ 40 nm) and 10 mTorr (~ 200 nm) respectively. Control samples without the Pt-NPs (ITO/ATO/AlO_x/IGZO/ITO) and (p^+ Si/AlO_x/AlO_x/IGZO/ITO) were also fabricated for comparison purposes. The fabricated devices were post-annealed at 250 ^oC in air for 1 hr. The TFT dimensions are L = 100 μm and W = 400 μm. Transmission spectra were obtained using a Perkin Elmer Lambda 9 UV/Vis/NIR dual beam spectrophotometer. Plan view images of the Pt-NPs grown on ALD AlO_x layer were obtained using an analytical SU-70 FESEM at 1 kV. A Hitachi HF2000 transmission electron microscope was used to image the Pt-NPs in plan view and in the cross-section of the device samples prepared by focused ion beam milling. X-ray photoelectron spectroscopy (XPS) was carried out using a Riber XPS

with dual Mg/Al anode source. The IGZO memory device characteristics were measured with an HP 4155B semiconductor parameter analyzer.

6.3 Discussion

The schematic cross-section of the TTFT IGZO memory device is shown in Figure 6-1(a), which is similar to a bottom-gated TFT structure. To verify that the proposed device is transparent, optical transmission experiments using a spectrophotometer were carried out. The raw optical transmission versus the wavelength of the substrate and the entire IGZO memory device stack is shown in Figure 6-1(b), (A) represents the substrate (glass/ITO/ATO) and (B) represents the entire stack of the memory device (glass/ITO/ATO/Pt-NPs/AlO_x/IGZO/ITO). At visible wavelengths the entire stack was still highly transparent throughout the visible spectrum. The addition of subsequent layers to the substrate did not cause an appreciable reduction in the transparency of the device and at visible wavelengths the entire stack was still highly transparent.

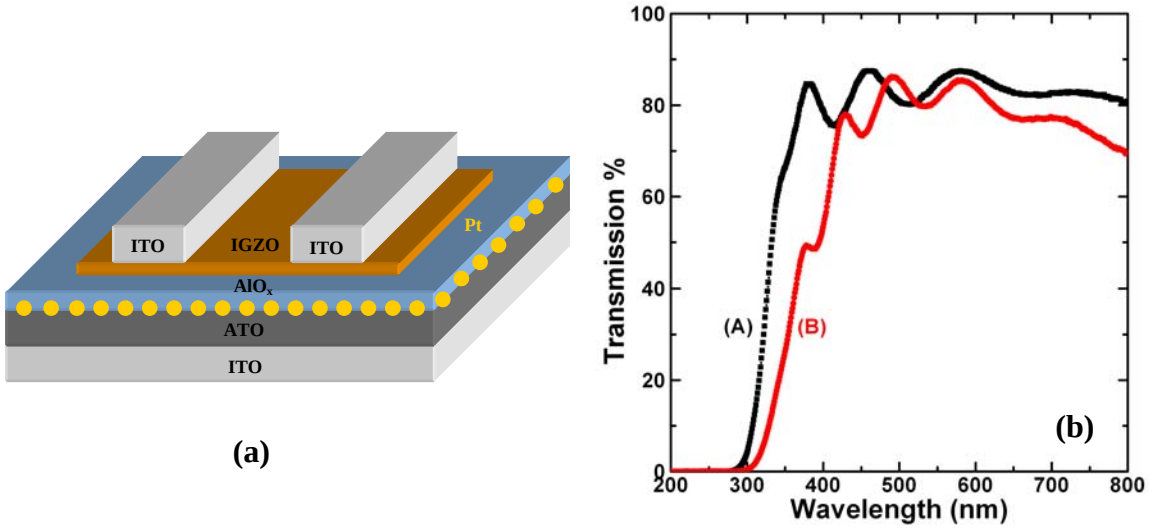

Figure 6-1: (a) A schematic representation of the transparent IGZO memory device, (b) Transmission spectrum of the substrate (A) and the entire device stack (B).

The schematic cross-section of the opaque IGZO memory device is shown in Figure 6-2(a), which is again similar to a bottom-gated TFT structure. To verify the presence of Pt-

NPs on the substrate several analytical techniques were utilized. Field emission scanning electron microscope (FESEM) was used to image the Pt-NPs grown on ALD AlO_x. The Pt was grown for 30 cycles and Figure 6-2(b) shows disbursed Pt-NPs in the 4-5 nm size range.

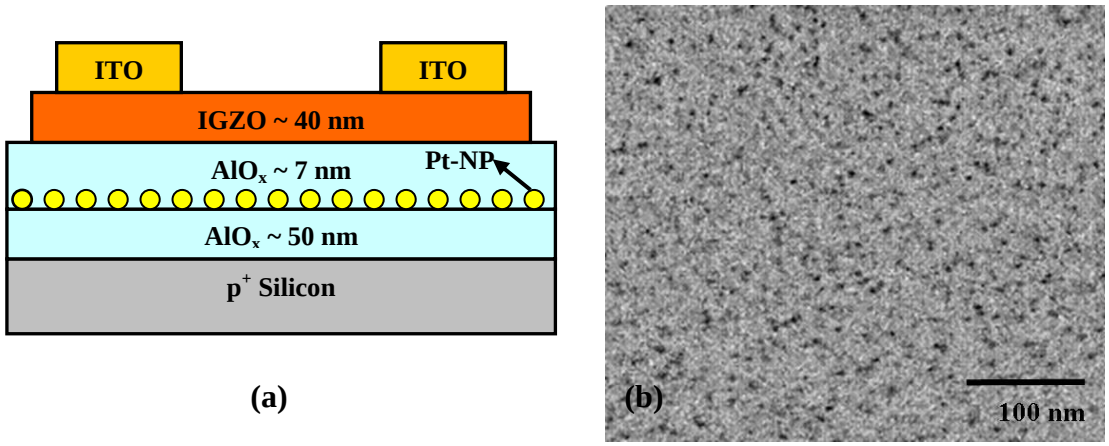

Figure 6-2: (a) A schematic representation of the opaque IGZO memory device. The ITO layer thickness was ~ 200 nm. (b) A FESEM image of the Pt-NPs grown for 30 cycles on ALD AlO_x shows disbursed Pt-NPs in the 4-5 nm size range.

To get a measure of the density of the Pt-NPs, a plan view transmission electron micrograph was used. A 5 nm AlO_x layer was grown on a thin SiN_x membrane obtained from Protochips Inc., following which Pt was grown for 30 cycles. The TEM image is shown in Figure 6-3. Finely disbursed Pt particles in the size range 3 – 5 nm is observed with few cases of neighboring particles coalescing.

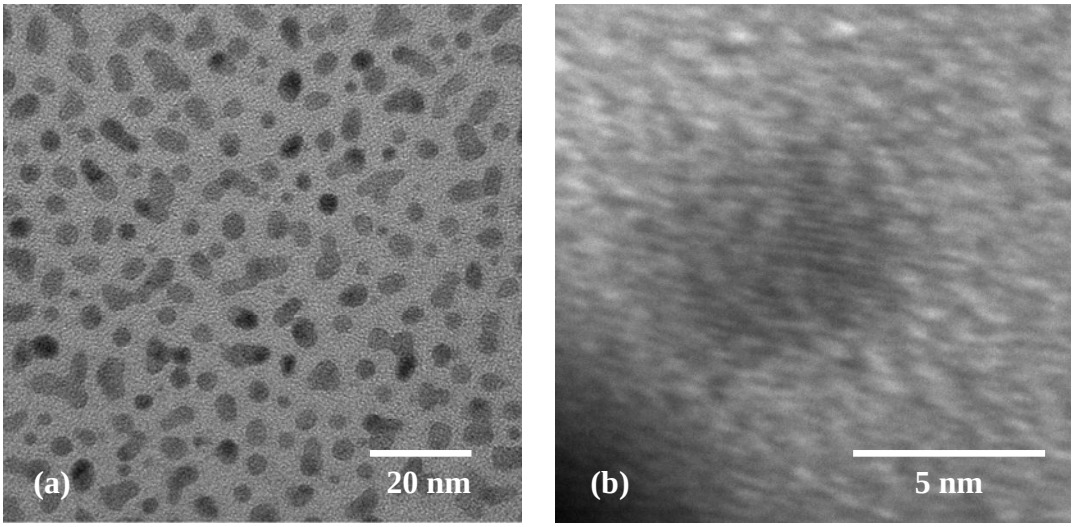

Figure 6-3: (a) TEM image of Pt-NPs grown on an AlO_x layer. Pt was grown for 30 cycles. A rather uniform distribution of particles ranging from 3 – 5 nm in size is observed. (b) High resolution TEM image shows the lattice planes and the crystalline nature of the Pt-NPs.

From Figure 6-3(a) the Pt-NP density was determined to be ~ 2.3 x 10^{12} cm^{-2}. By increasing the number of Pt growth cycles Pt-NP density increases but brings about more variation in the particles size distribution due to nucleation of new particles. In Figure 6-3(b), the high resolution TEM image indicates that the Pt-NPs are essentially crystalline with distinct lattice planes. To analyze Pt-NPs grown on an ATO substrate XPS analysis was carried out. Figure 6-4 shows the XPS data for the platinum 4f and 4d signals after 25 and 35 cycles of ALD Pt on ATO substrates. The signal intensity increases as a function of the cycle count. The increase is attributed to the increase in the number of Pt nuclei and the increasing size of the Pt nuclei. The Pt 4f peak overlaps with the Al 2p peak (~ 74 eV) but the Pt 4f doublet (~ 71 eV) becomes more apparent as the cycle count increases. We also use the weaker Pt 4d peak to confirm the presence of Pt after 25 cycles. Similar results were seen for Pt-NP grown on ALD AlO_x samples [138].

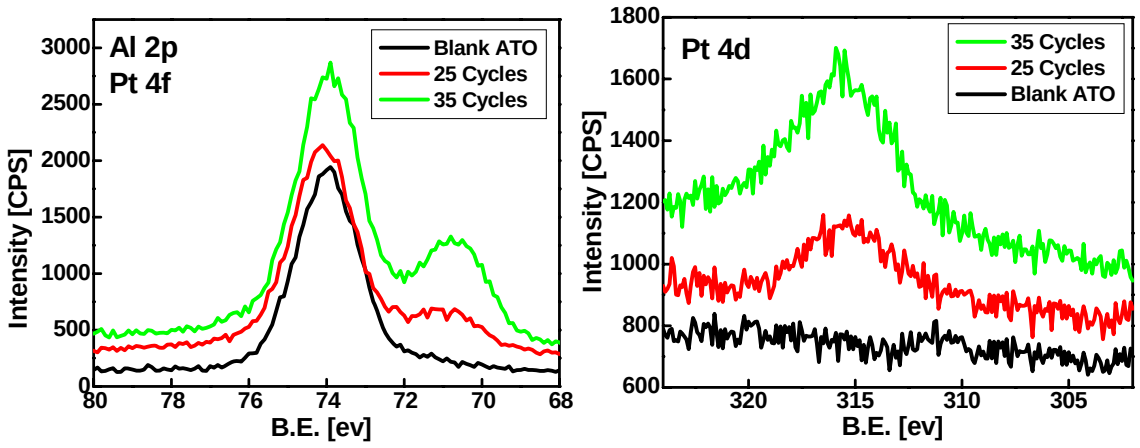

Figure 6-4: XPS data showing an increase in signal intensity of Pt 4f and Pt 4d peaks with ALD Pt cycle count corresponding to the increase in Pt on the ATO sample surface.

A cross-sectional transmission electron micrograph (TEM) of the TTFT IGZO memory device with Pt grown at 25 cycles is shown in Figure 6-5(a), and the various layers are indicated. Figure 6-5(b) is a micrograph at a higher magnification and clearly shows the presence of Pt-NPs. The particles appear spherical in nature and are about 3 nm in size.

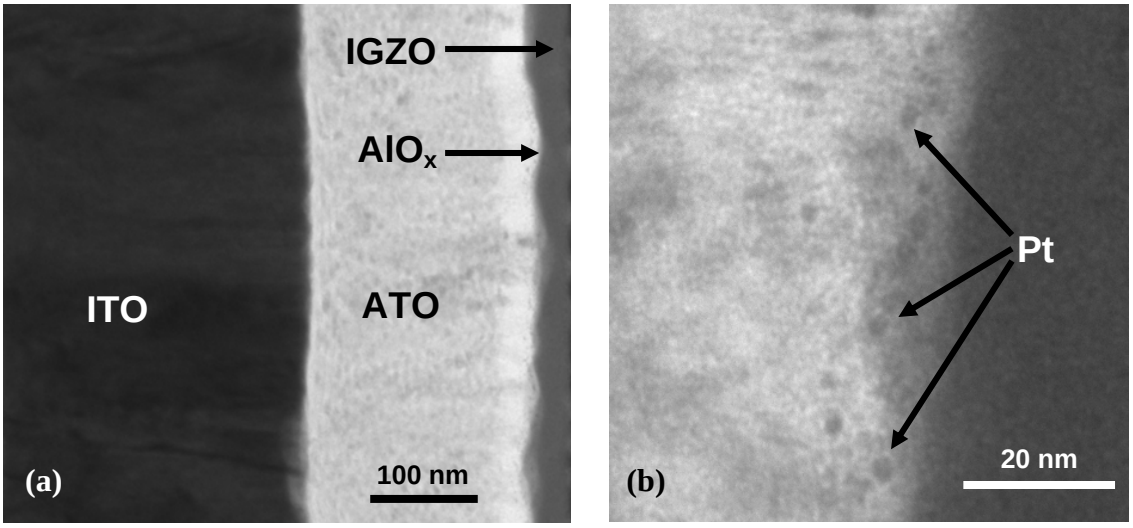

Figure 6-5: (a) Cross-section TEM micrograph of a TTFT IGZO memory device stack. (b) Embedded Pt-NPs are evident at a higher magnification and appear spherical and about 3 nm in size.

The transfer characteristics [$\log(I_{DS})$–V_{GS}] of the IGZO TTFTs both with (grown at 35 cycles) and without Pt-NPs are shown in Figure 6-6(a) and (b). The gate voltage, V_G, was swept in 0.2 V increments from a negative value to a positive value and back to the starting negative value (e.g. -10 to 10 to -10 V) while the source/drain voltage, V_{DS}, was fixed at 10 V. We define the TFT on-voltage, V_o, as the gate voltage where the drain current reaches 100 pA. We can see in Figure 6-6(a) that the control transistors (without the Pt-NPs) show negligible hysteresis with the ΔV_o [V_o (reverse sweep) – V_o (forward sweep)] ~ 0.35 V when the device was swept from -30 to 30 V and back. The following TFT characteristics were extracted for the control devices, V_{TH} = -0.25 V, μ_{eff} = 14 $cm^2 V^{-1}sec^{-1}$, $I_{on}/I_{off} > 10^7$, and S = 0.2 $Vdecade^{-1}$.

In contrast a significant hysteresis phenomenon can be seen in the devices with embedded Pt-NPs as shown in Figure 6-6(b). We see a clockwise hysteresis of the transfer curves. IGZO TFTs are basically n-type devices and a positive bias generates an accumulation layer of electrons in the channel close to the channel/dielectric interface. These electrons tunnel through the AlO_x (tunneling oxide) and get trapped in the Pt-NPs when $V_G >$ 0 during the forward sweep. During the reverse sweep the trapped electrons screen the applied gate voltage leading to a lower current and the observed clockwise hysteresis in the transfer characteristics. For the same reason the maximum current seen in the devices with Pt-NPs is about an order of magnitude lower than the control devices due to the electrons trapped in the Pt-NPs. We can also notice that the subthreshold slopes of both the forward and the reverse sweeps are similar indicating no defect creation at the semiconductor/dielectric interface due to the charging process. We also observed that the slope of the $\sqrt{I_{DS}}$ vs. V_G characteristics does not change appreciably when the device was charged showing that the charging process has a minimal influence on the carrier mobility.

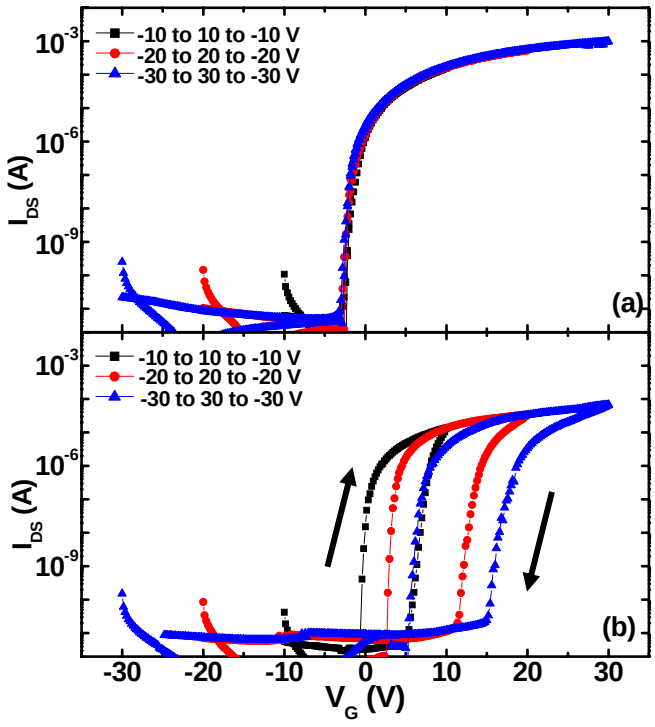

Figure 6-6: log(I_{DS})-V_{GS} sweeps of (a) control TTFT (no Pt-NPs) and (b) memory TTFT (with Pt-NPs grown for 35 ALD cycles). Hysteresis sweeps (■) –10 to 10 to -10 V, (●) –20 to 20 to -20 V, and (▲) –30 to 30 to -30 V were made consecutively. The directions of the forward and reverse sweeps are indicated. V_{DS} = 10 V and TFT dimensions: L = 100 μm and W = 400 μm.

From Figure 6-6(b) we can see that ΔV_o increases by 5.1, 8.9, and 9.8 V as the V_G sweep range increases from (-10 to 10 to -10 V), (-20 to 20 to -20 V), and (-30 to 30 to -30 V) respectively showing that the trapping sites are not completely saturated. The I_{off} of the reversely swept curves are higher than that of the forward swept curves indicating that the trapped electrons are not released in the reverse sweep [139]. We observe that the V_o of the forward sweep for the three consecutive sweeps, (-10 to 10 to -10 V), (-20 to 20 to -20 V), and (-30 to 30 -30 V), increases also indicating the trapped electrons are not completely released during the reverse sweep. This is the result of the device being in a depletion mode when a negative gate bias is applied ($V_G < 0$), hence the device would require a much larger time and/or negative potential to completely remove the trapped electrons [140].

The charging efficiency of the Pt-NPs was verified by stressing the memory devices with a gate bias. Both positive and negative bias (program voltage) for a predetermined time (0.1, 1, 2.5, and 10 s) was applied to the gate electrode while grounding the source and drain electrodes. The V_o was measured before and after the application of the stress and the shift in V_o is plotted in Figure 6-7. A positive gate bias induces a positive V_o shift as expected due to the electron injection into the charge-trapping layer. The hysteresis memory window [ΔV_o = V_o (post) – V_o (pre)] increases with an increase in the applied gate bias and the stress duration. The shift in V_o tends to saturate for stress times above 3 s indicating that the number of electrons the nano-particle can store is saturating [141].

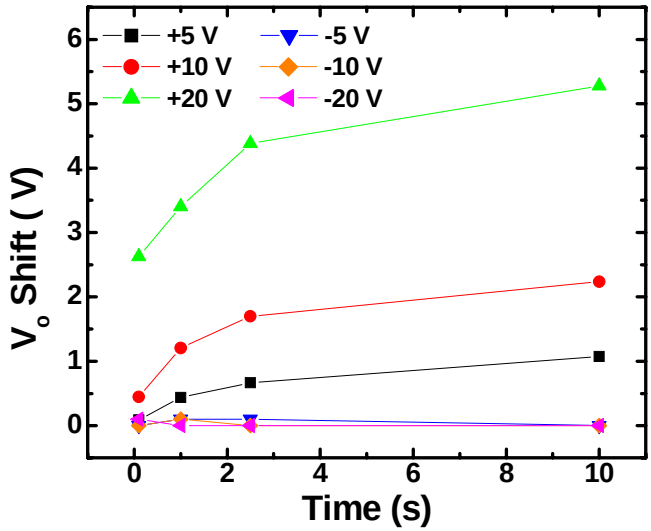

Figure 6-7: Shift in V_o for a TTFT IGZO memory device with Pt-NPs grown for 35 cycles as a function of gate bias and the stress duration for both positive and negative gate bias. Source and drain electrodes were grounded while stressing the gate. V_{DS} = 10 V while reading the device. The curves are for visual aid.

On the other hand a negative gate bias does not introduce a shift in V_o. The invariability of V_o with a negative bias on the gate can be explained by the lack of electrons in the channel due to the creation of the depletion layer and lack of holes, which are not generated in the semiconductor. This shows that in this device programming is done by electron trapping while programming with holes is not possible [6,142]. The control TFTs (without the Pt NPs) showed minimal (~0.2 V for +20 V bias for 10 s) variation in V_o with a positive gate bias and

no shift in V_o for a negative gate bias confirming that the observed behaviors of the IGZO memory devices are due to trapping of electrons in the Pt-NPs.

To study the effect of number of Pt-NP growth cycles on the memory effect, TTFT memory devices with two different cycle counts (25 and 35) were fabricated. Increasing the number of growth cycles has two effects. It increases the size of the existing Pt-NPs and also induces nucleation of new Pt-NPs. Though Novak *et al*. pointed out that subsequent grown cycles predominantly grows the existing particle size [138], nevertheless both these effects increase the number of trapping sites for the electrons and which in turn increases the tunneling probability for the electrons. In Figure 6-8, the IGZO memory device with Pt-NPs grown for 35 cycles shows a higher V_o shift compared to the one with 25 cycles as expected. Similar to data shown in Figure 6-7 we can see that the V_o shift starts to saturate above 3 s.

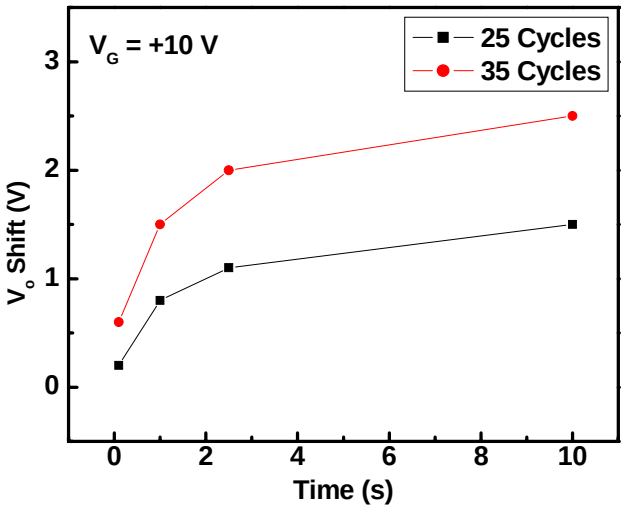

Figure 6-8: The effect of the Pt growth cycles on the IGZO TTFT memory window. The stressing voltage is $V_G = +10$ V. Source and drain electrodes were grounded while stressing the gate. Legend indicates the Pt ALD growth cycles. $V_{DS} = 10$ V while reading the device. The curves are for visual aid.

The charge retention characteristics of the IGZO TTFT memory device were evaluated. The stored electron charge loss (measured as shift in V_o) was assessed at room temperature after stressing the device at $V_G = 20$ V for 2 s while the source and the drain electrodes were grounded. The V_o was measured periodically by sweeping V_G over 5 V around the point when the TFT turns on to limit the charging effect during the read measurements. ΔV_o as a

function of time is shown in Figure 6-9. Immediately after the stressing ΔV_o is 3.45 V and within the first 500 s it drops down to ~ 3 V and then slowly reduces to 2.65 V after 10^4 s which amounts to less than 25% charge loss. The initial loss corresponds to electrons trapped in shallow interface states created during the Pt-NPs incorporation in the TFT dielectric while the majority of the electrons are strongly trapped at the Pt-NP sites. Further improvements in the device behavior are expected if the blocking oxide, ATO, thickness is reduced; this would lower the voltage requirements of the device leading to further optimization of the device structure.

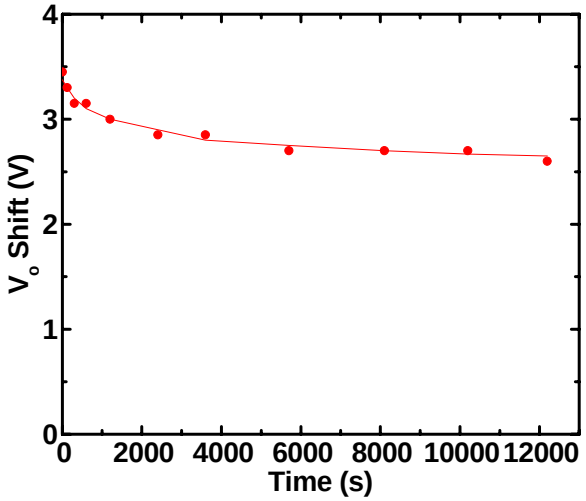

Figure 6-9: Charge retention characteristics of the IGZO TTFT memory with with Pt-NPs grown for 35 cycles after stressing at V_G = 20 V for 2 s. Less than 25% loss in stored charge seen after 10^4 s.

Programming and charge retention experiments carried out on opaque IGZO memory devices samples showed similar behavior. Figure 6-10 shows the effect of programming time on the memory window for the memory device with Pt-NPs grown for 30 cycles. As expected the control sample show minimal V_{on} shift on programming and a negative programming voltage on a memory device does not produce a memory window.

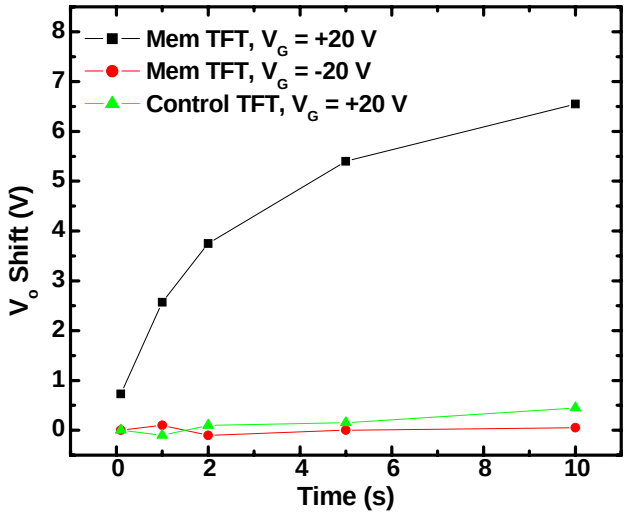

Figure 6-10: Shift in V_o for an opaque IGZO memory device with Pt-NPs grown for 30 cycles as a function of the gate stress duration for both positive and negative gate bias. The control sample (without Pt-NPs) does not show a V_o shift. Source and drain electrodes were grounded while stressing the gate. V_{DS} = 10 V while reading the device. The curves are for visual aid.

The higher V_o shifts seen in this sample compared to the TTFT memory device is due to the relatively higher coupling factor, ~ 0.06 for TTFT and ~ 0.12 for the opaque IGZO memory device, or due to the change in the Pt-NP size and distribution between the two variants of the memory device. As seen earlier, the density of the Pt-NP grown on AlO_x for 30 cycles is ~ 2.3 x 10^{12} cm^{-2} and from Figure 6-10, a V_o shift of 2.5 V is observed when the device is programmed at 20 V for 1 s. A measure of the trapped charge density is given by,

$$N = \frac{C_{BO}}{q}\Delta V_{on} \qquad (6.1)$$

where C_{BO} (capacitance per unit area of the blocking oxide) and q have values of 149 nF cm^{-2} and 1.6 x 10^{-19} C, respectively. Thus, the number of electrons stored in the Pt-NPs is estimated to be ~ 2.3 x 10^{12}. This indicates that roughly 1 electron is stored per Pt-NP. When the same analysis is extended to the V_o shift seen when the memory device is programmed for 10 s (~ 6.5 V), it accounts for about 3 electrons stored per Pt-NP [140].

The charge retention characteristic of the opaque IGZO memory device was carried out at room temperature. The shift in V_o was assessed after stressing the device at V_G = 20 V for

5 s while the source and the drain electrodes were grounded. The measurement settings were similar to the TTFT memory device case. ΔV_o as a function of time is shown in Figure 6-11. The charge retention is relatively enhanced compared to the TTFT memory case, which may be due to the smoother nature of the AlO_x compared to ATO. A memory window loss of 50 % was estimated to occur at ~ 1 x 10^6 s and ~ 10 % of the window was still preserved over 10 years.

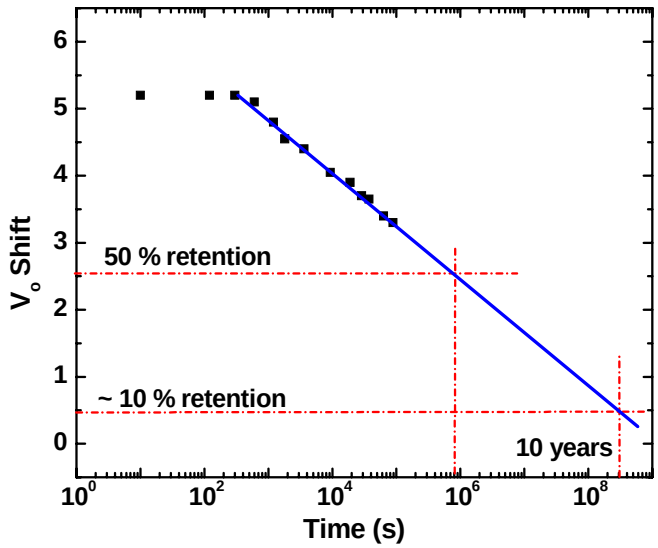

Figure 6-11: Charge retention characteristics of the opaque IGZO memory TFT with Pt-NPs grown for 30 cycles after stressing at V_G = 20 V for 5 s. The linear extrapolation of the memory window loss with log time indicates a 50% charge retention at ~ 10^6 s and ~ 10% charge retention over 10 years.

To understand the erase characteristics of the memory device a V_G = -10 V was applied after the device was programmed with V_G = 20 V for 2 s. But unlike the charge retention experiment, the gate bias was maintained at -10V and the source and drain electrodes were grounded when the device was idle and not being read. The change in V_o from the initially programmed state is converted as the stored electron charge loss with time, charge loss % = $\{[V_o(t = 0) - V_o(t)]/V_o(t = 0)\}$ and plotted in Figure 6-12. The data presented in Figure 6-9 is also plotted in Figure 6-12 as a comparison. We can see that the charge loss behavior of the stressed device (V_G = -10 V) is similar to the unstressed device (gate floating) with a fast

component and a slow gradual component and that the negative gate bias is not effective in completely erasing the device showing us the strong trapping of the electrons in the PT-NPs. In fact the charge loss difference between the stressed and unstressed devices (~ 5% over10^4 s) is the amount of erasing induced by the negative gate bias. The IGZO memory devices are easy to program but difficult to erase and this can be understood by looking at the program/erase mechanisms using simple energy band diagrams shown in Figure 6-13.

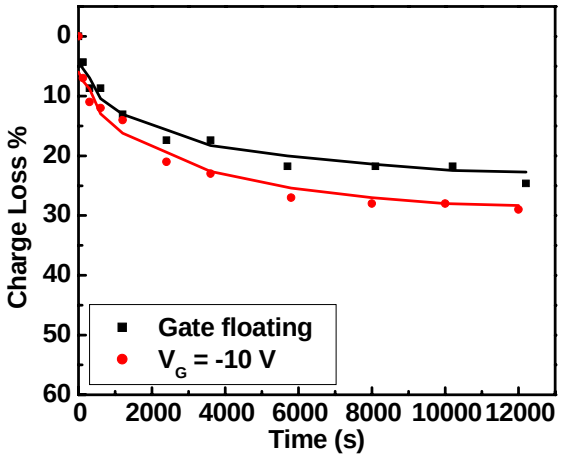

Figure 6-12: Effect of erasing the device with a $V_G = -10$ V bias as measured as charge loss %. Data presented in Figure 6-9 is plotted as a comparison. The curves are for visual aid.

In all the program/erase experiments, a Fowler-Nordheim (F-N) tunneling method was used, in which a positive (program) or a negative (erase) gate bias was applied while the source and drain electrodes were grounded. The number of charges tunneling through the thin AlO_x dielectric, as expressed as a tunneling current density (J), which is also a measure of the V_o shift is given by [143],

$$J = \frac{A}{4\Phi_b} E_{inj}^2 \exp\left[-\frac{2B\Phi_b^{3/2}}{3E_{inj}}\right] \qquad (6.1)$$

where A and B are constants, E_{inj} and Φ_b are the electric field and the energy barrier at the charge injection interface respectively. We can see from Figure 6.13 that Φ_b for electron injection during programming from the IGZO channel is about 3.1 eV. Owing to the large work function of the Pt (~5.6 eV), the Φ_b for electron injection during erasing from the Pt-

NPs is about 4.6 eV. This large discrepancy between the electron barriers leads to the asymmetry in the program/erase characteristics of the IGZO memory devices.

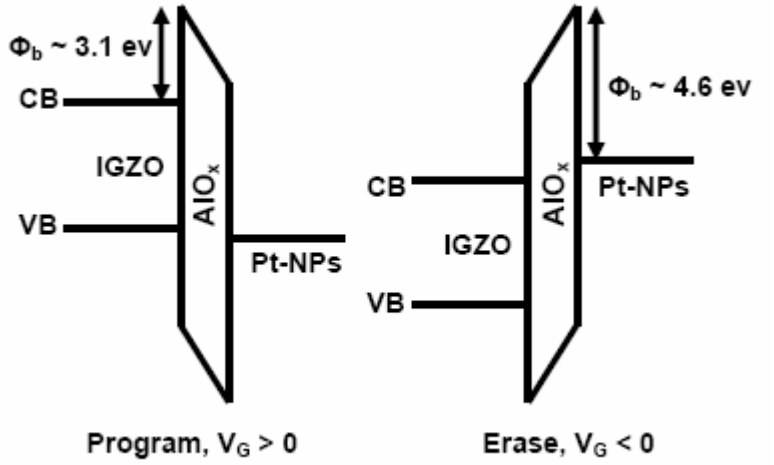

Figure 6-13: F-N tunneling program/erase mechanisms for IGZO TFT memory devices. The tunneling barrier seen by electrons while programming and erasing is 3.1 eV and 4.6 eV respectively.

Erasable programmable read only memory is a class of non-volatile memory that can be electrically programmed but erased using an ultraviolet (UV) light [144]. The UV light provides sufficient energy for the trapped electrons to overcome the barrier resulting in memory erasure. A similar technique was used to erase the IGZO memory devices. After the devices were programmed at 20 V for 10 s, a UV light with a wavelength centered at 350 nm illuminated the sample for ~ 1 s which accounted for erasing the device. Five program/erase (P/E) cycles were carried out and the turn-on voltage, V_o of the device was recorded after each step (program and erase). Figure 6-14 complies the results from the P/E cycles. The memory window after the first program step is ~ 6.5 V and with the subsequent erase and program cycles the memory window shrinks. It can be noted that the memory window starts to saturate to a value close to 3.5 – 4 V as the number of P/E cycles increases. This may be due the interaction of the UV light with the layers of the device, which may create or reduce defect states leading to a reduction in the tunneling of carriers. The UV erase step seems to be sufficient enough to remove all the carriers trapped in the Pt-NPs as evidenced by the V_o of erased device being similar to that of the virgin device. There is also a tendency for the

device to be over-erased. This set of experiments was carried out to show that the IGZO memory TFTs could not only be programmed but erased as well. More studies with appropriate automation needs to be carried out to completely understand the physics behind the UV erase behavior of these devices.

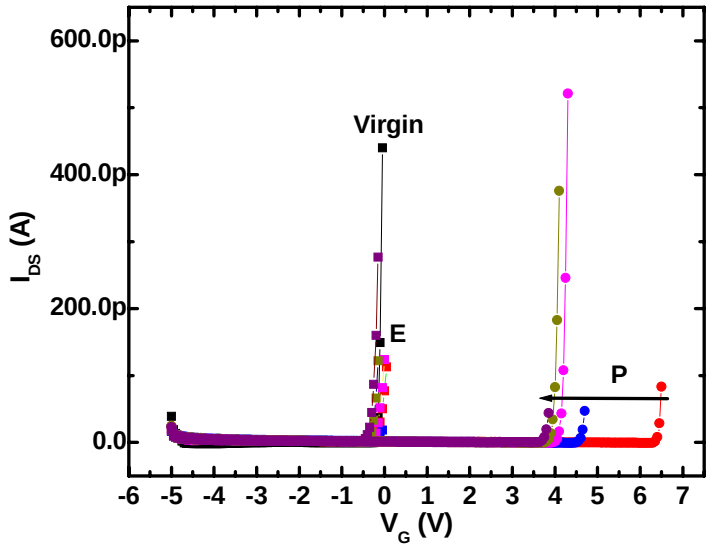

Figure 6-14: Program/Erase (P/E) behavior of IGZO memory TFTs. Devices were programmed at 20 V for 10 s. The erase was carried out by shining a 350 nm wavelength ultraviolet lamp for ~ 1 s on the device. The read measurements to determine V_o were carried out by sweeping V_G with V_{DS} = 10 V. (●) – program (P) and (■) – erase (E). The arrow indicates the evolution of the memory window as the number of P/E cycle increases.

6.4 Conclusions

In summary a transparent memory device utilizing Pt nano-particles and an amorphous oxide semiconductor TFT based on IGZO has been demonstrated. The charge trapping can be attributed to the presence of Pt-NPs and verified from the turn-on voltage shifts seen during positive gate voltage stress. Charge retention measurements show that the charges are strongly trapped in the Pt nano-particles and the non-volatility of the device was ascertained with only a 25% loss of the stored charge even after 10^4 s. An asymmetric response was observed between the programming and erasing nature of the IGZO memory TFT and was explained using the difference between the energy barriers that the electron encounters

during program/erase. Memory erasure was accomplished by illuminating a UV light source on the sample.

CHAPTER 7

TRANSPARENT CIRCUITS BASED ON INDIUM GALLIUM ZINC OXIDE THIN-FILM TRANSISTORS

Based on manuscripts:

Transparent, high-speed ring oscillators based on indium gallium zinc oxide
A. Suresh, P.Wellenius, H. Luo, L. M. Lunardi, and J. F. Muth
To be submitted.

An amorphous indium gallium zinc oxide active matrix electroluminescent pixel
P.Wellenius, A. Suresh, H. Luo, L. M. Lunardi, and J. F. Muth
Accepted in Journal of Display Technology, to be published in the special issue on transparent electronics.

7.1 Abstract

In this chapter transparent integrated devices and circuits using indium gallium zinc oxide (IGZO) thin film transistors (TFT) are fabricated and characterized. First, inverter circuits using two enhancement-mode transistors were designed and fabricated. The inverters show peak gain magnitude (dV_{OUT}/dV_{IN}) ~ 3. Using these inverters, five- and seven-stage ring oscillator (RO) circuits were fabricated. Five-stage ROs operated at a frequency as high as 2 MHz for a supply voltage of 25 V, which corresponds to a propagation delay of 50 ns/stage. The effect of the individual device size and the design criteria used in fabricating the ROs on the oscillation frequency and propagation delay are explored. Second, an active matrix pixel was fabricated and characterized using IGZO thin film transistors and a novel electroluminescent Eu:IGZO thin film phosphor. The results show that even large and

unoptimized IGZO devices are capable of modulating at the frequencies necessary for modern display technology. The effect of the device sizes on the modulating efficiency of IGZO TFTs is evaluated. Furthermore, a rare-earth doped amorphous oxide semiconductor (AOS) electroluminescent phosphor integrated with a TFT to form a transistor controlled pixel element was demonstrated.

7.2 Transparent IGZO inverters and ring oscillators

7.2.1 Experimental Approach

The circuits were fabricated on glass substrates coated with ~ 60 nm of sputtered indium tin oxide (ITO) from Delta Technologies Inc. The entire process employs four mask levels. The first step is patterning and reactive ion etching (RIE) the ITO layer to form gate electrodes. Next a 120 nm thick AlO_x gate insulator is put down using atomic layer deposition (ALD) at 200 °C. The next step is the opening of contact holes to the gate electrode, which is carried out using photolithography and RIE. The next two mask levels involve a standard photolithography and liftoff process in which the IGZO (semiconductor) and ITO (source/drain and interconnect) are deposited at room temperature using pulsed laser deposition (PLD) at an oxygen partial pressure of 25 mTorr and 10 mTorr respectively.

A plan view image of a processed chip with thirteen ring oscillators, twenty inverters and several discrete transistors is shown in Figure 7-1. The circuits are evidently highly transparent owing to the wide bandgap of the constituent layers. Individual TFTs and inverters were electronically characterized using a Hewlett Packard 4155B parameter analyzer. The transient response of the inverters was measured using an Agilent 20 MHz waveform generator to apply a square pulse train to the input terminal of the inverter. The transient response was observed by measuring the output voltage drain current using a Tektronix DPO4104 1 GHz oscilloscope. The oscilloscope was used to capture the output waveform of the ring oscillators, while a constant positive voltage in the 0 to 30 V range was applied to gate and the drain of the load transistors using a DC power supply. The voltage

supplied to the gates (V_G) of the load TFTs was always set the same as that to the drains (V_{DD}).

Figure 7-1: Glass substrate containing several ring oscillators, inverters, and discrete transistors. Note the highly transparent nature of the circuits where the label below is clearly visible.

7.2.2 Discussion

Transistor characteristics of a TFT with W = 100 μm and L = 20 μm were extracted from $\log(I_{DS}) - V_{GS}$ and $\sqrt{I_{DS}}$ versus V_{GS} curves, as shown in Figure 7-2(a). At a V_{DS} = 20 V, a saturation field effect mobility of ~ 15 $cm^2 V^{-1} s^{-1}$, a threshold voltage of 3.75 V, a subthreshold slope of ~ 130 mV $decade^{-1}$, and an I_{on}/I_{off} ratio > 10^8 were measured. The maximum off-state current was < 1 pA, which is limited by the gate current. Figure 7-2(b) shows the output characteristics (I_{DS} versus V_{DS}) for several values of V_{GS} for the same device.

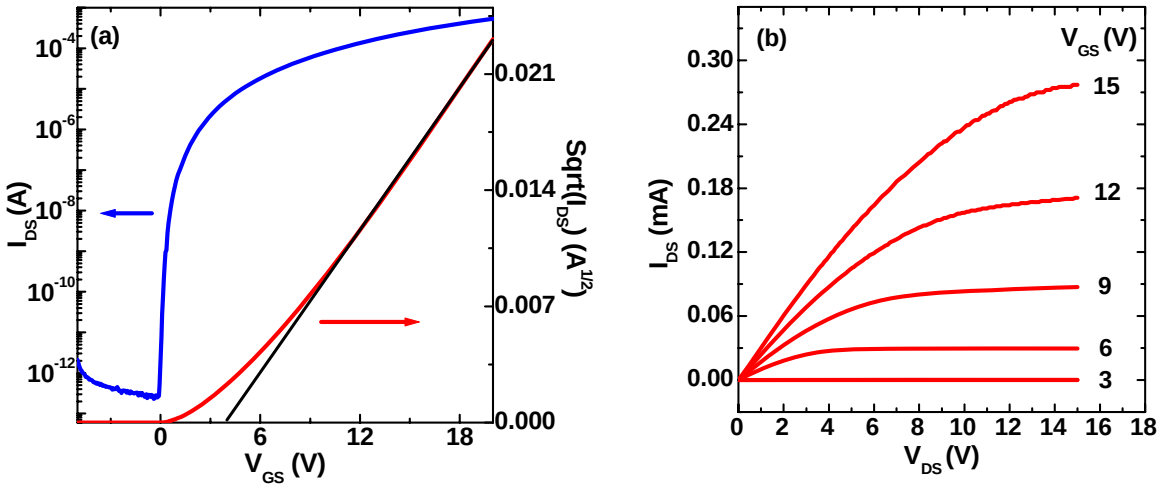

Figure 7-2: (a) IGZO TFT log(I_{DS}) – V_{GS} and $\sqrt{I_{DS}}$ versus V_{GS} characteristics for V_{DS} = 20 V. (b) I_{DS} – V_{DS} characteristics of the same device. W/L = 100 µm/20 µm and C_{di} ~ 60 nF cm^{-2}.

The most basic digital integrated circuit is a voltage inverter, which is shown schematically in Figure 7-3(a). Unlike CMOS inverters, in an n-type transistor based inverter, two transistors are connected such that one of them acts as a voltage-controlled switch (or driver) while the other acts as an active load (diode type). An optical micrograph of the fabricated IGZO inverter is shown in Figure 7-3(b) and the different components are indicated.

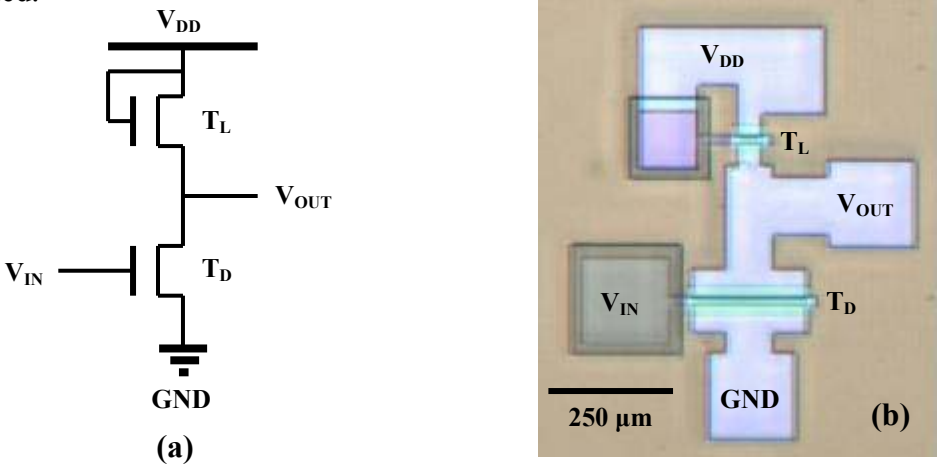

Figure 7-3: (a) Schematic representation of a voltage inverter with an enhancement load. T_L and T_D represent the load and drive transistors, respectively. (b) Optical micrograph of an IGZO TFT inverter with a beta ratio = 5 (L_{drive} = 10 µm, W_{drive} = 200 µm, L_{load} = 10 µm, W_{load} = 40 µm).

An important attribute of the inverter is its geometry or device sizes. The beta ratio, β, is given by ratio of the size of the drive transistor to that of the load transistor, i.e. $\beta = (W_{drive}/L_{drive})/(W_{load}/L_{load})$. The DC characteristics of the inverter was evaluated by applying a supply voltage, V_{DD} on the load TFT and sweeping the input voltage, V_{IN} while measuring the output voltage, V_{OUT}. Figure 7-4(a) represents the evolution of V_{OUT} as a function of V_{IN} and V_{DD} for an IGZO inverter with, $L_{drive} = 20$ µm, $W_{drive} = 400$ µm, $L_{load} = 20$ µm, $W_{load} = 40$ µm (a beta ratio of 10) and a source/gate and source/drain overlap of 2.5 µm. Figure 7-4(a) indicates that the output voltage decreases with increasing input voltage (toward positive voltage). It shows that the transfer characteristic of the inverter shows good logic level conversion. A near zero input voltage (corresponding to a binary value "0"), still results in a large positive output voltage (corresponding to a binary value "1"). The switching voltage (the input voltage at which the output voltage begins to decrease) occurs close to $V_{IN} = 0$, which corresponds to the near zero V_{on} of the TFTs. These inverter characteristics make them suitable to be used in ring oscillator (RO) circuits without the necessity of additional compensated circuits such as level shifters [52].

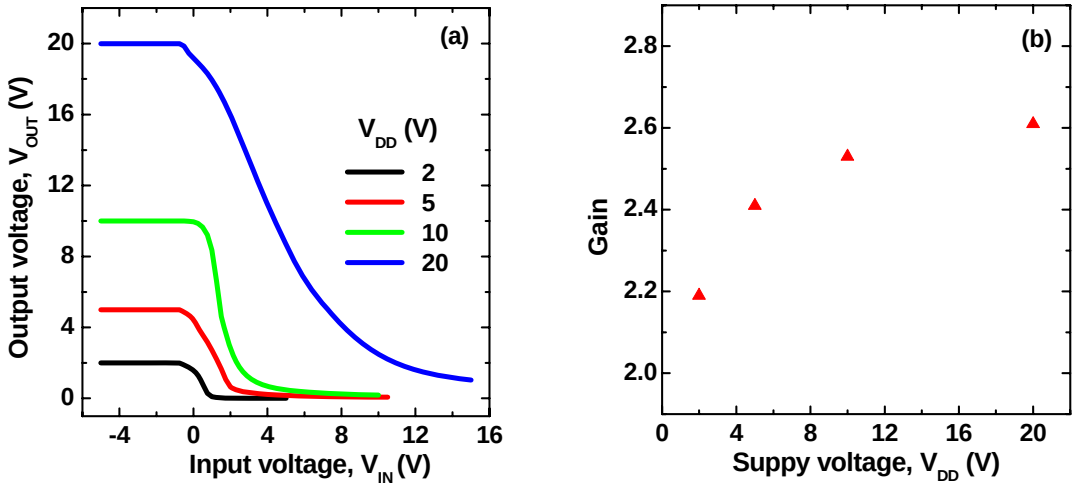

Figure 7-4: (a) Transfer curve for a transparent inverter fabricated using IGZO TFTs for different values of V_{DD}. (b) The change in the inverter gain magnitude as a function of V_{DD}. The inverter beta ratio = 10 ($L_{drive} = 20$ µm, $W_{drive} = 400$ µm, $L_{load} = 20$ µm, $W_{load} = 40$ µm) and a source/gate and source/drain overlap of 2.5 µm.

Another requirement for the inverters to be applied to RO circuits is a gain magnitude greater than 1 for sustained signal propagation. The peak gain magnitude of an inverter is obtained from its transfer curve and is given by, gain = dV_{OUT}/dV_{IN}. The gain is affected by the ratio between the drive TFT and load TFT impedances and ideally equals $\sqrt{\beta}$ [103]. The impedance of the TFTs and hence the gain of the inverter are affected by the channel mobility, device geometry and biasing conditions. Figure 7-4(b) shows the inverter gain as a function of the supply voltage, V_{DD}. We see that the inverter gain increases and flattens as V_{DD} increases from 2 to 20 V. With the designed β of 10 for the inverter the gain approaches the theoretical value of 3.16. The difference between the theoretical value and the extracted value of the inverter gain may be due to the variation between the designed and the actual sizes of the TFTs. To further analyze the performance of the IGZO inverter a square pulse at different frequencies was applied to the drive TFT while a constant V_{DD} was applied to the load TFT. Figure 7-5 represents the input and output waveforms and it can be seen that the inverter functionality is achieved. At a higher frequency (1 kHz), the response of the inverter

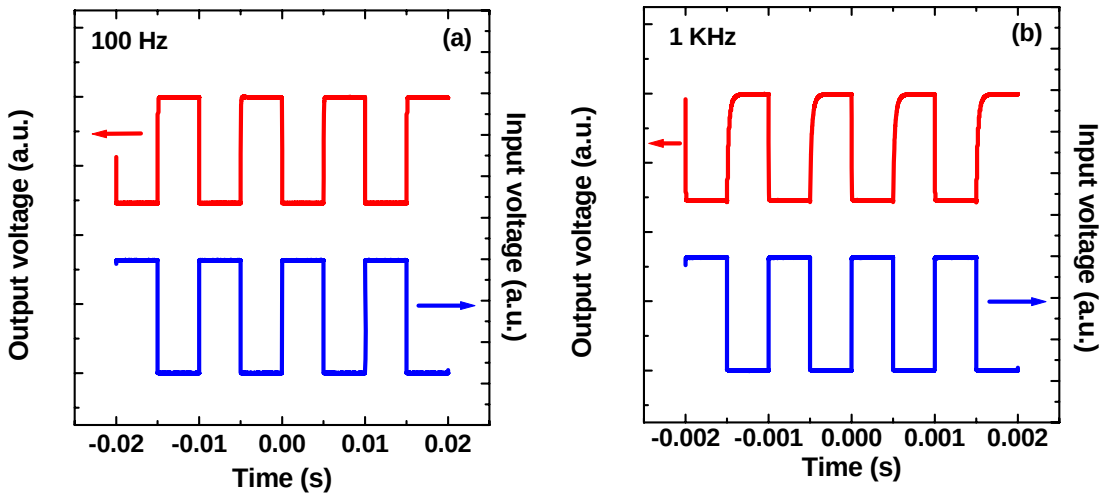

Figure 7-5: IGZO inverter response to a pulse input at different frequencies (a) 100 Hz and (b) 1 kHz. The inverter beta ratio = 10 ($L_{drive} = L_{load} = 20$ µm, $W_{drive} = 400$ µm, $W_{load} = 40$ µm) and a gate source/drain overlap of 2.5 µm. The amplitude of V_{IN} and V_{OUT} was 5.1 V and 3.1 V respectively.

when the input signal goes from low to high is faster than when the input signal goes from high to low. This is due to the large capacitance of the drive transistor ($L = 20$ µm, $W = 400$

μm) and shows that it is faster to charge the capacitor than to discharge it possibly due to residual trapped charges.

A ring oscillator consists of any odd number of inverters connected in series. In this study both 5- and 7-stage ROs were fabricated and characterized. Figure 7-6(a) shows the cross-section of the fabricated RO and Figure 7-6(b) is the optical micrograph of a 7-stage IGZO RO. No level shifter circuitry or an output buffer was used in the RO design.

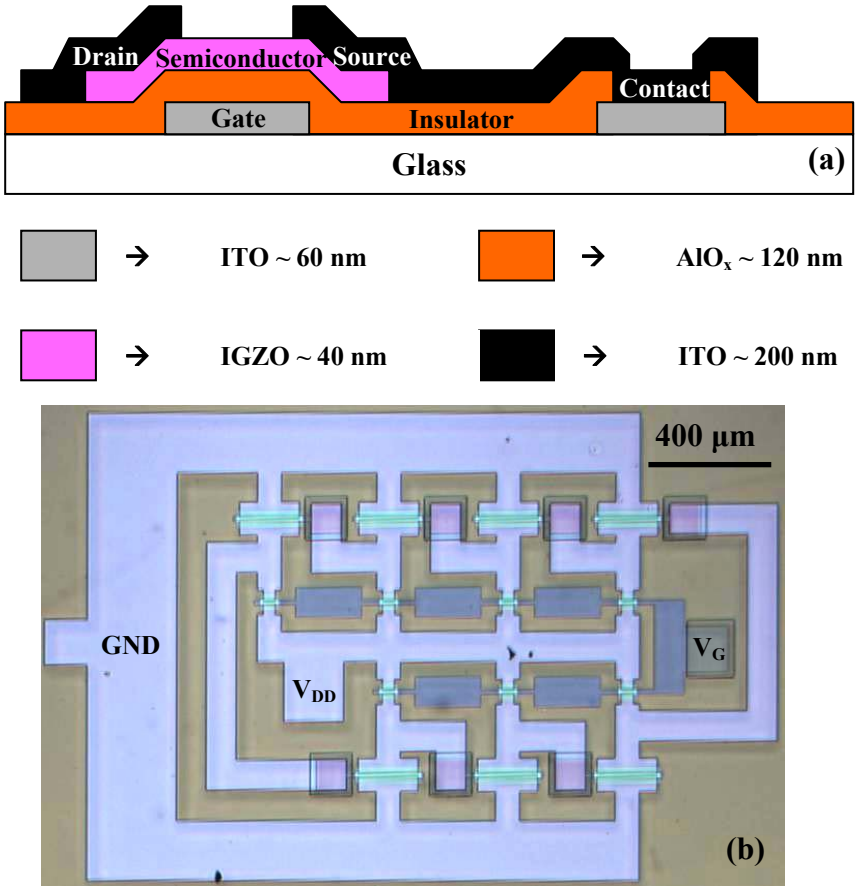

Figure 7-6: (a) Cross-sectional schematic of a RO. (b) Plan-view photograph of a seven-stage IGZO RO as fabricated (L_{drive} = 10 μm, W_{drive} = 200 μm, L_{load} = 10 μm, W_{load} = 40 μm, beta ratio = 5, and 2.5-μm source/gate and drain/gate overlap).

Figure 7-7(a) shows the output waveform of a 5-stage IGZO ring oscillator. The devices used in this ring oscillator had a minimum channel length of 10 μm and an overlap between the gate and source-drain electrodes of 2.5 μm. The width of the drive and load transistors

were 200 µm and 40 µm respectively giving a beta ratio of 5. The RO starts to oscillate at a supply voltage of 6 V. The DC offset voltage is ~ 0 V and the peak-to-peak voltage swing and frequency of oscillation at V_{DD} = 25 V are 110 mV and 2 MHz respectively. Figure 7-7(b) shows the oscillation frequency and the propagation delay per stage as a function of V_{DD}. As expected, the oscillation frequency increases as V_{DD} increases due to the reduction in the impedance of the load as well as drive transistors and this dependence is rather linear.

The propagation delay per stage, t_p is from the time period or frequency of the oscillation and is given by,

$$t_p = \frac{1}{2fN} \tag{7.1}$$

where, f is the frequency of propagation and N is the number of stages in the RO. The factor 2 arises from the fact that a full cycle requires both a low-to-high and high-to-low transition. A propagation delay of 50 ns per stage is recorded for V_{DD} = 25 V.

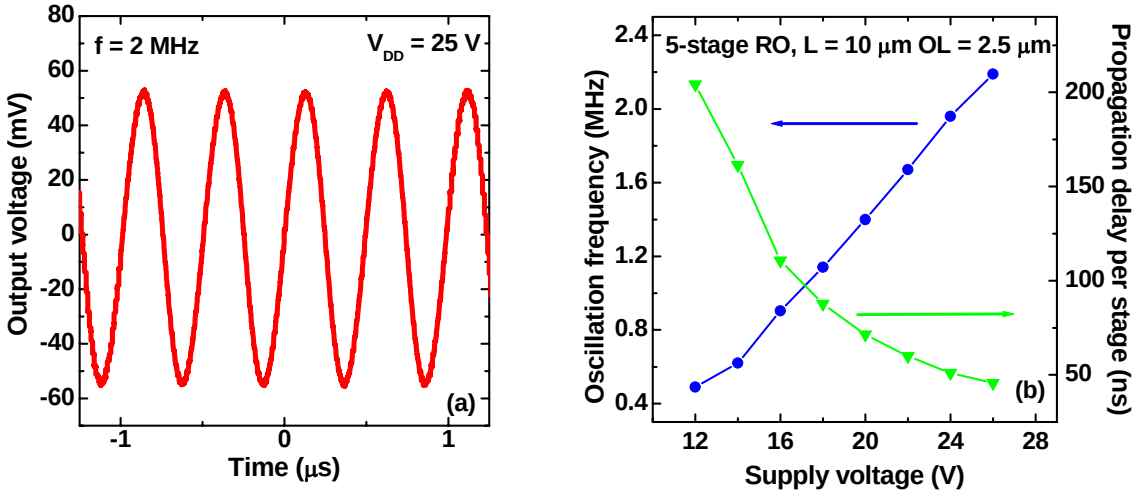

Figure 7-7: (a) Output waveform of a five-stage RO with a supply voltage, V_{DD} = 25 V operating at 2 MHz (the propagation delay of 50 ns/stage) and an output voltage swing ~ 110 mV $V_{p\text{-}p}$. (b) Oscillation frequency and propagation delay as a function of V_{DD}. (L_{drive} = 10 µm, W_{drive} = 200 µm, L_{load} = 10 µm, W_{load} = 40 µm, beta ratio = 5, and 2.5-µm source/gate and drain/gate overlap).

A similar analysis of a 5-stage RO circuit with a minimum channel length of 20 µm is shown in Figure 7-8. The DC offset voltage is ~ -0.1 V and the peak-to-peak voltage swing and frequency of oscillation at V_{DD} = 25 V are 1.7 V and 640 kHz respectively.

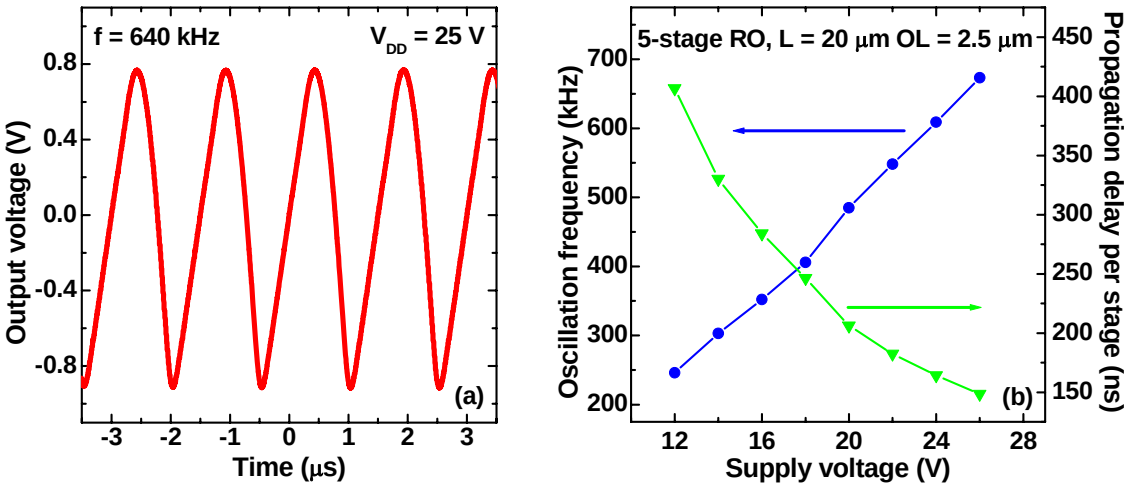

Figure 7-8: (a) Output waveform of a five-stage RO with a supply voltage, V_{DD} = 25 V operating at 640 kHz (the propagation delay of 156 ns/stage) and an output voltage swing ~ 1.7 V $V_{p\text{-}p}$. (b) Oscillation frequency and propagation delay as a function of V_{DD}. (L_{drive} = 20 μm, W_{drive} = 400 μm, L_{load} = 20 μm, W_{load} = 80 μm, beta ratio = 5, and 2.5-μm source/gate and drain/gate overlap).

It is evident that the geometry of the TFTs in the inverters of the RO governs the characteristics of the RO. In the next few plots the effect of channel length, the beta ratio and source/gate and source drain overlap in the inverters on the propagation delay and the oscillation frequency are studied. Figure 7-9 shows the effect of channel length on the RO performance. ROs with two different channel lengths, 10 μm and 20 μm are compared while the rest of the RO features are similar. As expected the RO composed of the smaller devices is faster with the oscillation frequency about 3 times higher.

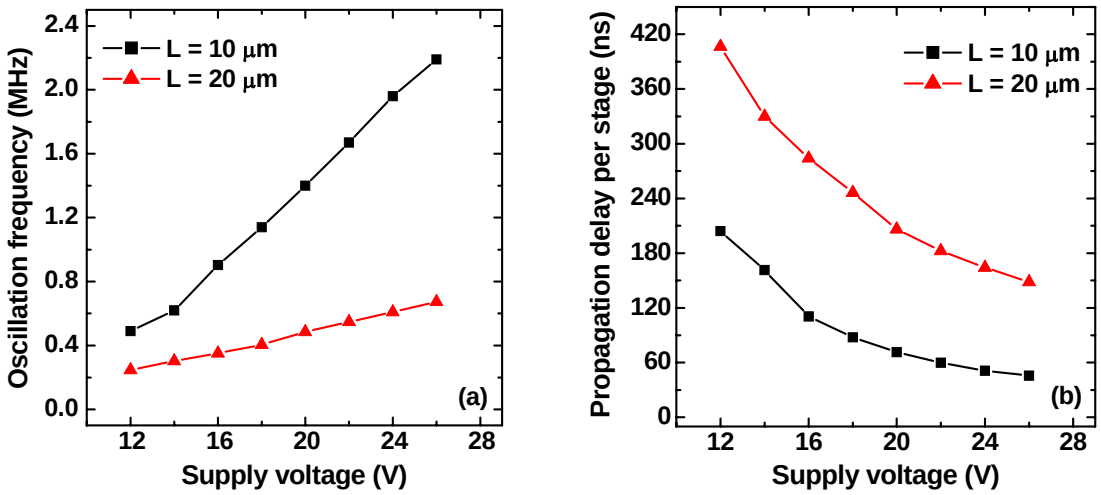

Figure 7-9: Oscillation frequency (a) and propagation delay per stage (b) as a function of supply bias and channel length (10 μm and 20 μm) of a 5-stage IGZO ring oscillator (L_{drive}/W_{drive} = 20, and L_{load}/W_{load} = 4, beta ratio = 5, and 2.5-μm source/gate and drain/gate overlap).

Figure 7-10 shows the oscillation frequency and propagation delay per stage as a function of supply bias for 5-stage ring oscillators with 2.5 μm and 5 μm gate to source and gate to drain electrode overlap. As expected, the propagation delay decreases with increasing supply voltage and with decreasing gate to source-drain electrode overlap. The smaller the electrode overlap the smaller is the parasitic capacitance of the circuit leading to faster circuits. Also since the IGZO TFTs have low subthreshold slopes high mobility and near zero turn-on voltages it is possible to operate these transparent RO circuits at relatively low voltages. RO circuits based on organic TFTs are usually operated at much higher voltages, 60 – 80 V [145,146].

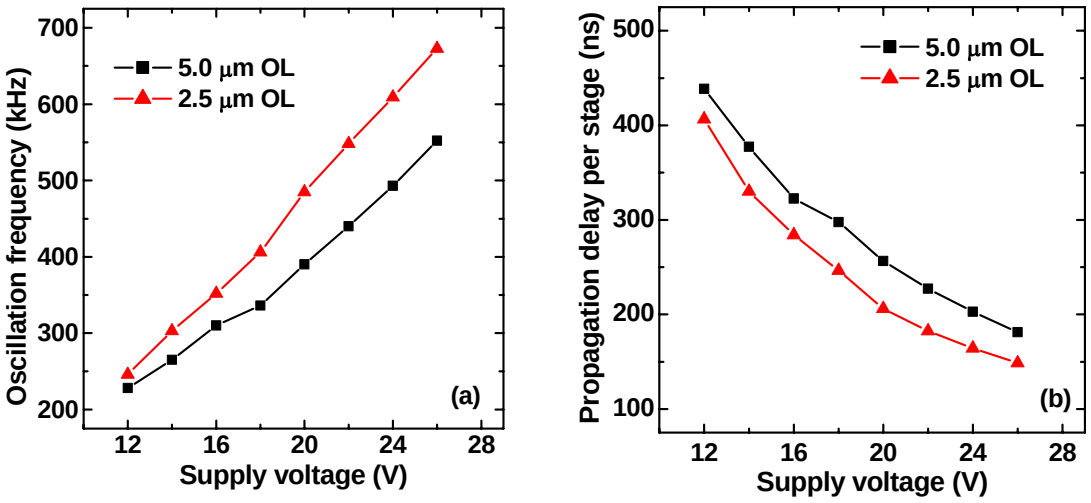

Figure 7-10: Oscillation frequency (a) and propagation delay per stage (b) as a function of supply bias and gate to source-drain electrode overlap (2.5 µm and 5.0 µm) of a 5-stage IGZO ring oscillator (L_{drive} = 20 µm, W_{drive} = 400 µm, L_{load} = 20 µm, W_{load} = 80 µm, beta ratio = 5).

To average out the propagation delay involved in a RO several stages are required. The intrinsic resistance and capacitance of the circuit have a larger effect on the circuit when the number of the RO stages increases giving a more accurate representation of the circuit performance. Figure 7-11 compares 5-stage and 7-stage ROs with 10 µm and 20 µm channel lengths. The oscillation frequency and the propagation delay scale very well as the number of stages increases. The 20 µm channel length 7-stage RO shows a slightly higher propagation delay compared to its 5-stage counterpart whereas in the 10 µm channel length RO the propagation delays are virtually identical especially at higher supply voltages.

There are several features of the IGZO ring oscillator that warrant a discussion. It is observed that even though the oscillation frequencies achieved in IGZO ROs are excellent for an all-oxide transparent circuit, the maximum voltage swing achieved is quite low for the applied voltage compared to RO circuits in [52] and [104]. Threshold voltage does not have a large effect on circuit speed, but can be one of the dominant factors determining output voltage swing [147]. From the transfer characteristics of the IGZO TFT it is observed that the devices have positive threshold voltages with near-zero V_{on} and a sharp device turn on. And

from the inverter behavior it is observed that the TFT characteristics are adequate to realize enhancement-enhancement inverters.

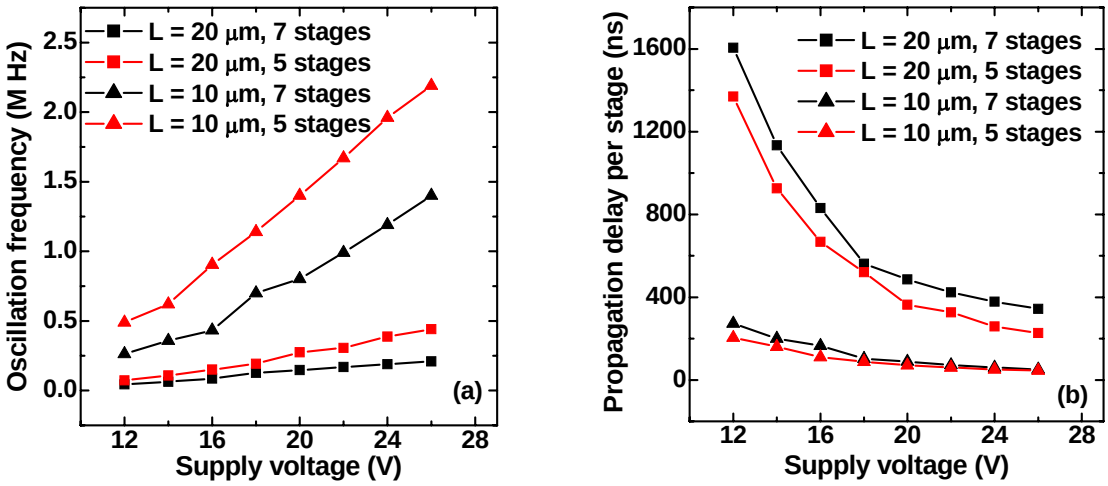

Figure 7-11: Oscillation frequency (a) and propagation delay per stage (b) as a function of supply bias, channel length (10 μm and 20 μm) and number of stages (5- and 7-stage) of a IGZO ring oscillator (L_{drive}/W_{drive} = 20, and L_{load}/W_{load} = 4, beta ratio = 5, and 2.5-μm source/gate and drain/gate overlap).

Another possibility is the lack of a buffer inverter stage at the output. The resistance offered by the oscilloscope might not be high enough when the signal is tapped within the ring oscillator leading to a voltage divider effect and loss of voltage swing of the ring oscillator. Uniform performance in the unit TFTs is required to achieve good operational speed and output swing. While the IGZO and ITO depositions within the dimensions of the circuit are definitely uniform, there might be issues with alignment of the various levels of the transparent circuit, which might lead to mismatch of device sizes and geometry. It is observed that the voltage swing in ROs made of TFTs with L =20 μm is ~ 20 times that of the ROs made of TFTs with L = 10 μm (2 V compared to 0.1 V). The misalignment, if any, would have a larger impact on a smaller device compared to a larger device. Further simulation and analysis is required to clarify the cause of low voltage swing see in these circuits.

7.3 Amorphous IGZO active matrix electroluminescent pixel

7.3.1 Experimental Approach

An addressable two-TFT active matrix pixel as shown by the circuit diagram in Figure 7-12(a) is fabricated. Here, one TFT (labeled *T1*) has as inputs a row (drain) and column (gate) voltage signal. The gate of the other TFT (*T2*) is connected to the source of *T1*, and the source of *T2* is grounded. When both the row and column are "high", *T1* applies a voltage to the gate of *T2* and is biased into saturation, providing a low resistance path to ground for one terminal of the TFEL device. The other terminal of the TFEL is connected to a high AC voltage source. In this scheme, a "high" signal is required on the row and column inputs to produce electroluminescence, while all other combinations of inputs result in no EL output. High AC voltages are needed to operate TFEL devices, which cannot be properly modulated by the TFTs themselves, as negative potentials cannot be applied to the source or drain of n-type TFTs. Thus, the TFEL output is modulated by creating a ground path via *T2*, which is effectively controlled via *T1*.

Fabrication of the pixel involves six mask levels and was built on a Corning 7059 glass substrate with 250 nm ITO and 220 nm ATO films obtained from Planar Systems Inc. The first two process steps consist of plasma etching of the ITO and ATO layer to allow fabrication of interconnected bottom-gated TFTs. The ITO layer is significantly thinned during plasma etching to reduce the step height and off-state leakage current through the TFT. The ITO acts as the gate electrode of the TFTs as well as the bottom contact for the TFEL device. The ATO dielectric is only used for the TFEL device where a high breakdown voltage and high-k dielectric is critical to device performance. The cross section illustrating the integration of a TFEL device with a single TFT is shown in Figure 7-12(b).

After substrate etching, a 200 nm thick SiN_x dielectric layer is deposited by PECVD at 300 ^{o}C. This conformal layer acts as the gate dielectric for the bottom gated TFTs. The SiN_x layer is lithographically defined and plasma etched using standard techniques. The 50 nm IGZO channel layer, 200 nm Eu:IGZO phosphor layer and 200 nm thick ITO contact layers

were put down by PLD in oxygen ambient at room temperature. PLD layers were individually patterned using standard lift-off lithography techniques. A plan view image of a processed chip with four pixels is shown in Figure 7-12(c). The final pixel is highly transparent, owing to the wide bandgap of the constituent layers. The light emitting area of the TFEL device is 2 mm x 2 mm. Three different channel lengths for TFT *T2* i.e., 100, 200 and 400 μm, were fabricated to investigate the effect of channel size on the transient characteristics of the TFT as well as the ability to modulate the TFEL device. The channel width for all TFTs was 800 μm and a single geometry was used for *T1* (*W/L* = 800/200).

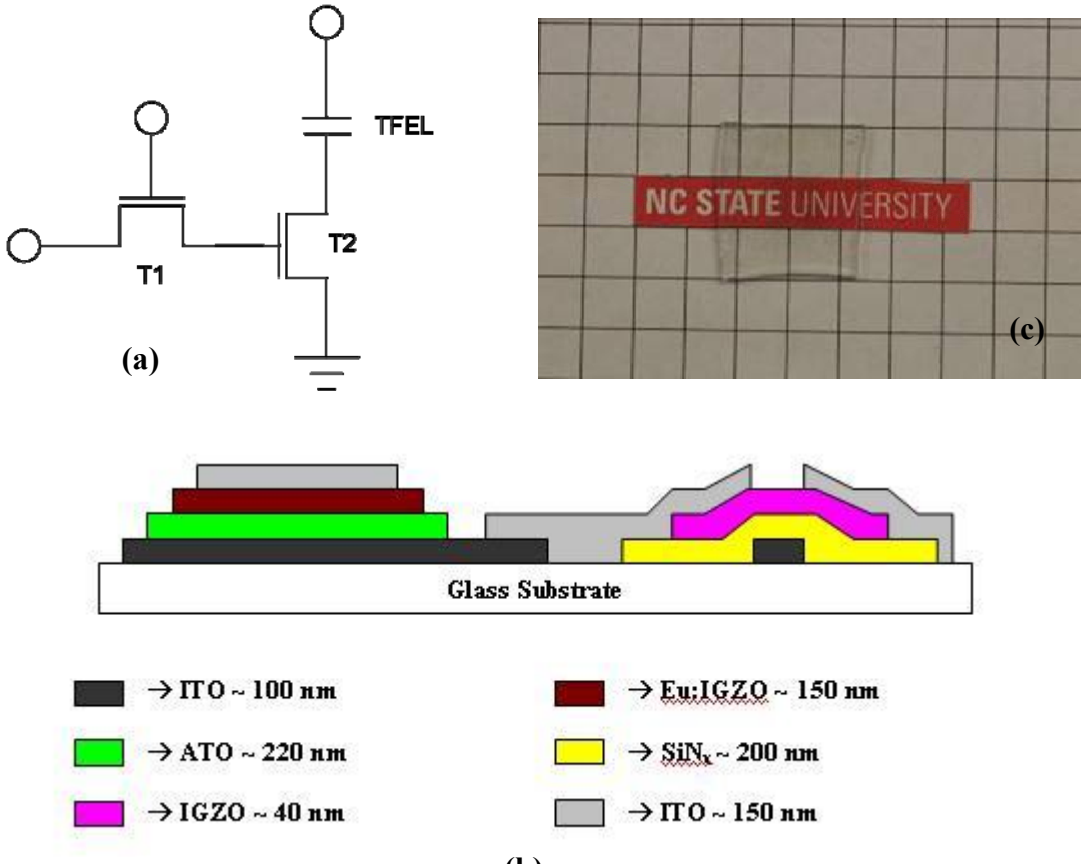

Figure 7-12: (a) Two-TFT pixel circuit for modulating a TFEL device. (b) Schematic illustration of the TFEL device incorporated with a single TFT. (c) The image of the finished active matrix pixel. The grid is 0.25" square. Note the highly transparent nature of the finished pixel.

Individual TFTs were electronically characterized using a Hewlett Packard 4155B parameter analyzer. The transient response of individual TFTs was measured using an Agilent 20 MHz waveform generator to apply a square pulse train to the gate or drain contacts. The transient response was observed by measuring the drain current using an EG&G model 181 preamplifier connected to a Tektronix DPO4104 1 GHz oscilloscope. Measurement of the transient characteristics of two interconnected devices was accomplished in a similar way. TFEL devices were biased using an Agilent 20 MHz waveform generator with an inverting amplifier to achieve the necessary biasing. The optical intensity of the TFEL device was measured using a calibrated, large area Si photodiode whose output was measured using a Keithley picoammeter.

7.3.2 Discussion

The static characteristics of individual TFTs, including I_{DS} vs. V_{DS} and $\sqrt{I_{DS}}$ vs. V_{GS} curves were measured. It was determined that the TFTs are of high quality and demonstrate hard saturation, as shown in Figure 7-13(a). An I_{on}/I_{off} ratio greater than 10^8 and an-off state leakage current on the order of 1 pA is achieved as demonstrated in Figure 7-13(b). The subthreshold swing of 400 mV decade^{-1} was extracted from the transfer characteristics displayed in Figure 7-13(b), indicating linearity that meets requirements for fast transient response of TFTs.

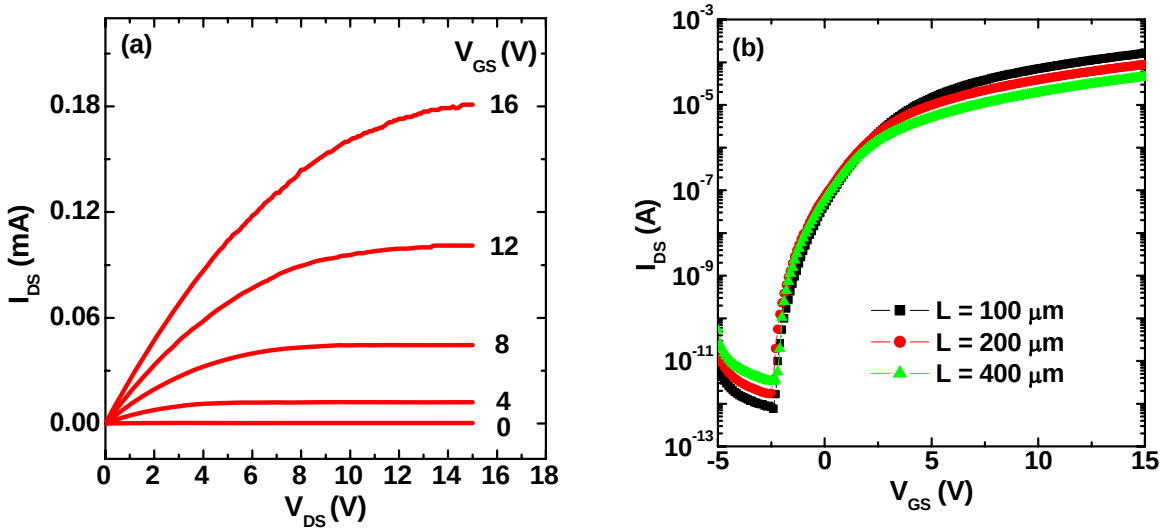

Figure 7-13: (a) DC I_{DS}-V_{DS} curves for V_{GS} from 0 to +16V. W/L = 800 µm/200 µm. (b) log(I_{DS})-V_{GS} transfer curves for three IGZO TFTs with different channel lengths, given in microns. All TFT channel widths are 800 µm.

The threshold voltage (~1 V) was determined by extrapolating the linear portion of the $\sqrt{I_{DS}}$-V_{GS} curve to zero as shown in Figure 7-14(a) and a saturation field effect mobility, μ_{sat}, of 7 $cm^2\ V^{-1}\ s^{-1}$ was extracted. The dependence of the average mobility, μ_{avg}, on V_{GS} in the linear regime is plotted in Figure 7-14(b). Both measures of carrier mobility are in good agreement.

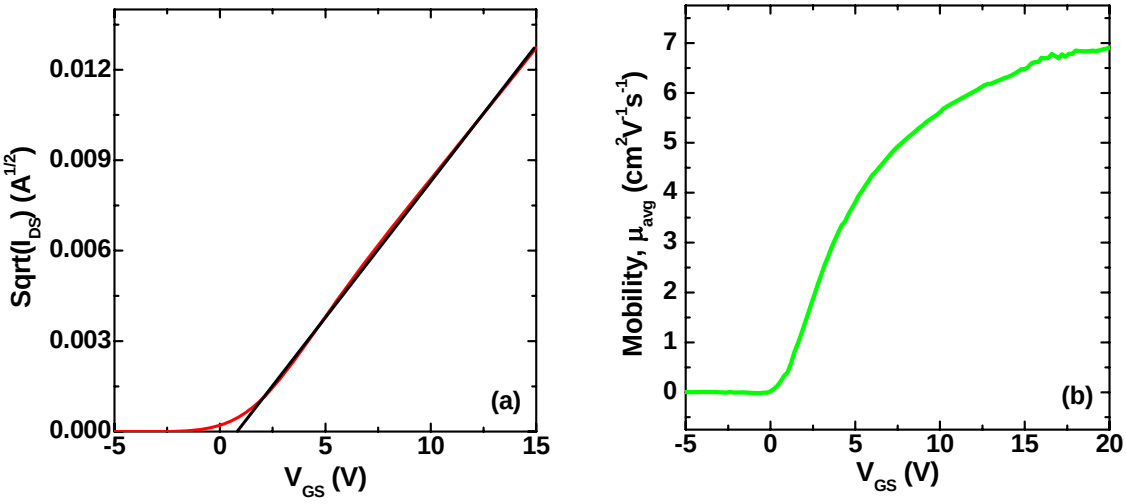

Figure 7-14: (a) A $\sqrt{I_{DS}}$-V_{GS} plot where the linear portion has been extrapolated to zero to determine the threshold voltage. (b) Carrier mobility is plotted as a function of gate voltage for an IGZO TFT in the linear regime, (W/L = 800 µm/200 µm).

The individual transient behavior of a single TFT (W/L = 800/100) was characterized using a waveform generator to individually pulse either V_{DS} or V_{GS}. To measure the response to a changing V_{GS}, the gate voltage was pulsed from 0 – 10 V with a 50% duty cycle while applying 10 V_{DC} to the drain. Subsequently, V_{DS} was pulsed from 0 – 5 V with a 50% duty cycle while 10 V_{DC} was applied to the gate contact. As shown in Figure 7-15, the response of the TFT to a change in V_{DS} is faster than to a change in V_{GS}. The slow response to a pulsed V_{GS} is mostly due to the large area of the TFTs. The response to a pulsed V_{DS} is quicker because the TFT channel is already formed as V_{DS} is pulsed. These devices have not been optimized for high-speed operation, but seem capable of operating at the frequencies required by modern displays. The frequency response could be substantially improved through the use of a gate insulator with a higher relative dielectric constant, or by reducing the TFT active area.

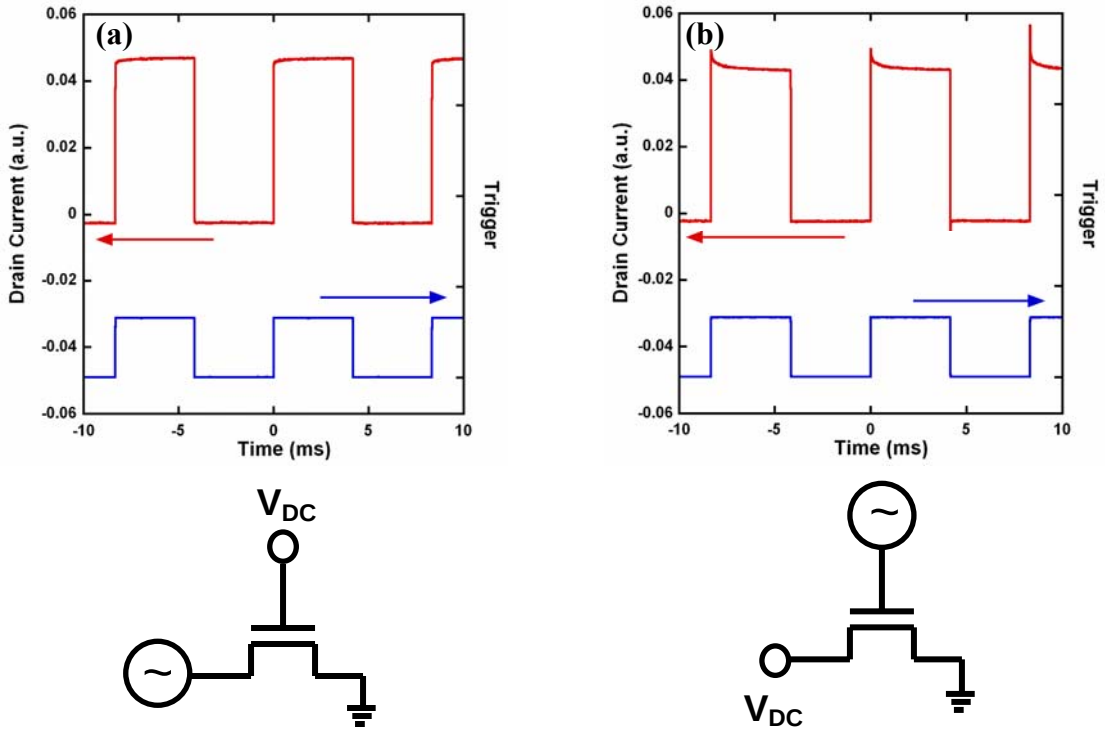

Figure 7-15: Single TFT switching characteristics, (a) V_{DS} is pulsed 0-10 V and (b) V_{GS} is pulsed 0-5 V. The trigger waveform represents a TTL output from the waveform generator. The biasing scheme of the TFT is also shown.

More important for pixel operation is the transient response of the interconnected TFTs, *T1* and *T2*. The results shown in 7-16 demonstrate that these large devices are capable of operating at 120 Hz, which is a common operating frequency for modern LCD displays. However, the devices can be optimized to further improve upon the transient characteristics. Features of the TFT design that can be addressed to improve the transient response include reducing the channel area, reducing the overlap between the source or drain and the channel and increasing the dielectric constant of the gate insulator.

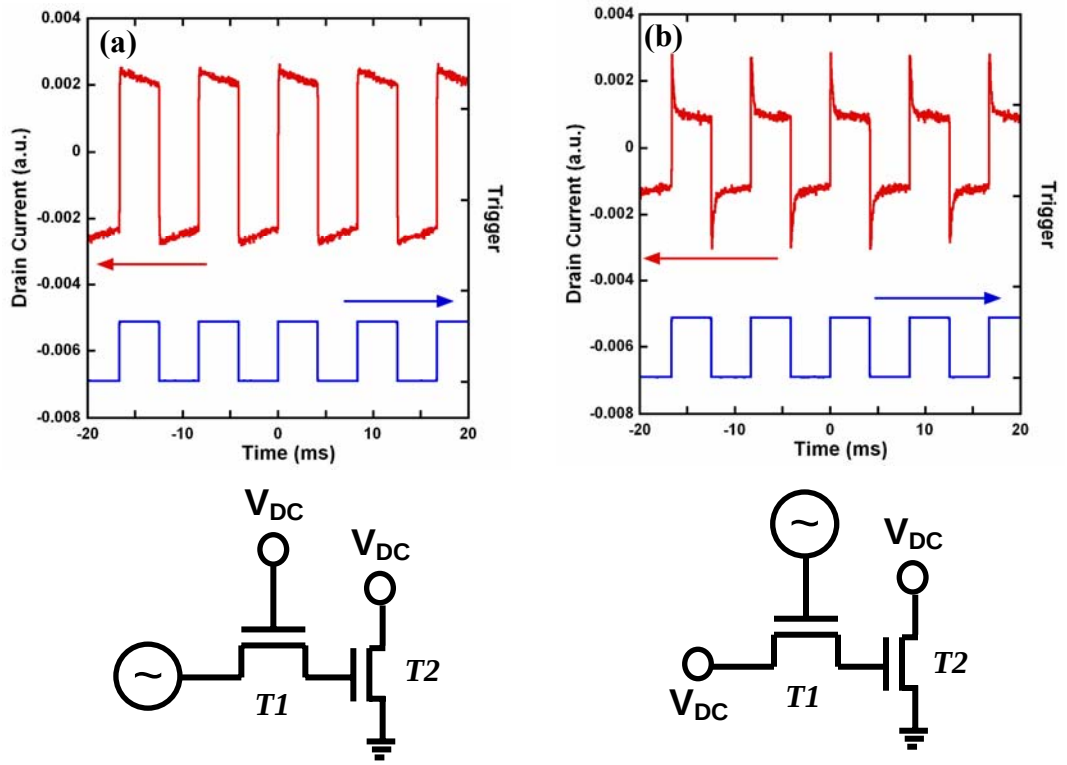

Figure 7-16: Transient response for two interconnected TFTs where the drain current from *T2* is plotted as a function of time. (a) The drain bias on *T1* is modulated from 0 – 10 V at 120 Hz with a gate voltage of 10 V. (b) The gate bias on *T1* is modulated from 0 – 5 V at 120 Hz with a drain bias of 10 V. In both tests, the *T2* drain bias is 10 V. The biasing scheme of the interconnected TFTs is also shown.

Eu doped gallium oxide and IGZO electroluminescent (EL) devices have been processed and characterized by Wellenius *et al*. [148]. The electroluminescence seen in these devices is due to the characteristic of the emission of the Eu^{3+} dopant where the most intense emission

results from transitions from the $^5D_0$ state to the ^7F_J manifold. The main emission peak is at 615 nm, due to the $^5D_0$ to $^7F_2$ transition in the rare earth ion. The narrow emission peaks can be useful for display devices as the result is a color with high spectral purity and the lack of emission from the IGZO host preserves the spectral purity of the Eu dopant. CIE color coordinates based on the EL emission were found to be (0.621, 0.362), which agree well with previous successful red TFEL devices [149].

Figure 7-17 shows the cathodoluminescence (CL) and electroluminescence (EL) spectra of Eu:IGZO films and TFEL devices. The spectral features are identical for both experiments and the CL emission intensity was shown to increase with increasing oxygen pressure. Figure 7-17 also shows the TFEL device in an on and off state.

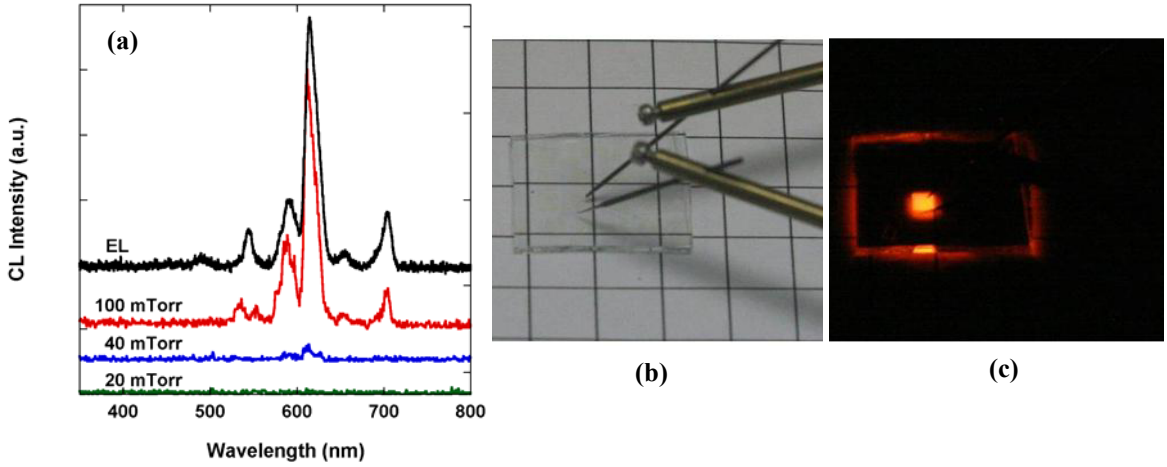

Figure 7-17: (a) Cathodoluminescence and electroluminescence spectra of Eu:IGZO doped films and a TFEL device. Photographs of the TFEL device off (b) and on (c) [148].

The output intensity of an individual TFEL device was characterized as a function of the applied AC voltage. In Figure 7-18(a), the device was driven by a 300 Hz sinusoid with a peak voltage from 40 to 100 V. The device threshold is near 40 V, but EL intensity increases rapidly beyond 40 V until it saturates near 65 V. From 65 V to 100 V, less than 10 % change in EL intensity is observed. The largest recorded photodiode current corresponds to approximately 2.5 cd/m^2, which can be seen by eye in a dark room.

Though the pixel was designed to be switched on/off by controlling the inputs of the two control transistors, the EL intensity could still be modulated, or turned off altogether, using

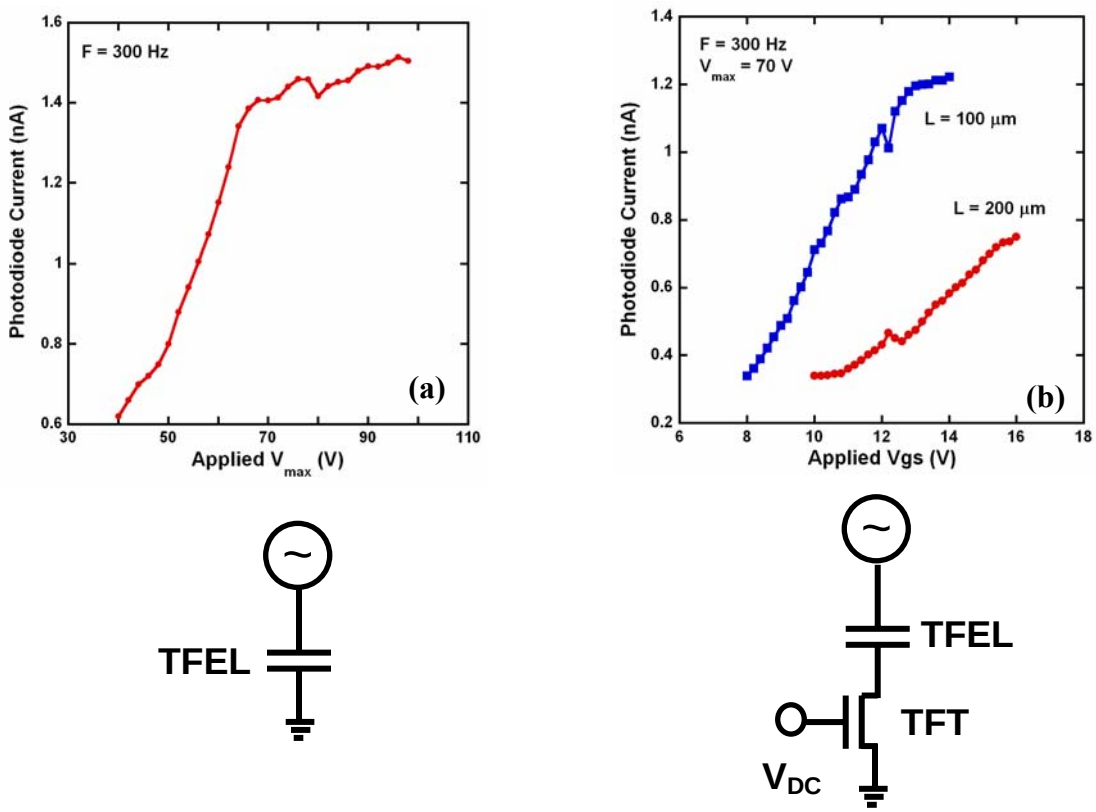

Figure 7-18: (a) EL intensity as a function of excitation voltage for an individual Eu:IGZO TFEL device, excited by a sinusoid waveform. The peak EL intensity corresponds to approximately 2.5 cd/m^2. (b) EL intensity for a TFT-modulated TFEL device with a peak applied voltage of 70 V at 300 Hz. The channel length of the modulating TFT are shown in the figure next to the corresponding data. The biasing scheme of the TFEL and the pixel element is also shown.

just the gate input to TFT *T2*. Here, the driving waveform is the same 300 Hz sinusoid, but the peak voltage is set to 70 V and V_{GS2} is varied from 8 to 16 V_{DC} for two TFT sizes (W/L = 800/200 and 800/100). As shown in Figure 7-18(b), both TFTs were capable of modulating the output of the TFEL device over a wide range of optical intensity and with a clear threshold for luminance. Three important features are observed to depend on the TFT channel length: 1) the EL luminance threshold, 2) the sensitivity of the TFEL device to the applied gate bias and 3) the maximum observed TFEL luminance. Another interesting observation is that the EL intensity saturates at high V_{GS}, with intensity well below which the TFEL device emits at the same applied AC voltage. As a simplification, this may be

explained by discussing the TFT as a variable current-limiting device in series with the TFEL. The instantaneous current through a TFEL device can be quite large as the polarity of the applied electric field is reversed. In this scenario, the instantaneous current flowing through the TFEL is modulated by the TFT. A reduction in current through TFT *T2* results in a proportional reduction in TFEL emission. The effect of the channel length is then approximately consistent with TFT device theory. An increased channel length reduces the drain current in both saturation and linear regions of operation and is a likely factor in effects 1) and 3). Furthermore, in the linear region of operation, an increased channel length negatively affects the transconductance of the device, which may impact 2). This is a complex system and requires further investigation to fully understand the mechanisms at work in TFEL device modulation.

7.4 Conclusions

Using room temperature processed transparent IGZO TFTs basic digital circuits such as inverters and ring oscillators were fabricated. A 5-stage ring oscillator with a minimum channel length of 10 and a gate and source drain overlap of 2.5 operates at more than 2 MHz, corresponding to a propagation delay of 50 ns per stage at a supply bias of 25 V. Effect of TFT channel length and gate and source-drain electrodes overlap or the circuit performance was evaluated. IGZO TFTs were used as switching transistors to fabricate an active matrix pixel featuring a Eu:IGZO TFEL phosphor layer. This TFEL device was successfully integrated with and modulated by a TFT by applying a gate voltage in the range of 8 to 16 V_{DC}, using the TFT channel as a ground path for the TFEL. IGZO TFTs were pulsed at 120 Hz with good transient response, demonstrating IGZO as a viable material for active matrix backplanes.

CHAPTER 8

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

8.1 Conclusions

The focus of the research presented in this dissertation is to develop indium gallium zinc oxide (IGZO) AOS thin films by the pulsed laser deposition process for thin film transistor applications and to identify the experimental as well as design parameters that influence TFT performance. Before IGZO can be extensively used its electrical stability and dynamic characteristics needs to be ascertained. This is the other area of research that has been described in this document.

High mobility indium gallium zinc oxide (IGZO) thin films were deposited using pulsed laser deposition at room temperature. The deposited films were amorphous in nature and highly transparent and have a relatively sharp optical absorption edge near 345 nm for the film grown at 20 mTorr. Hall mobilities as high as 35 $cm^2\ V^{-1}\ s^{-1}$ were observed. Oxygen partial pressure during deposition was found to have a profound effect on the electrical characteristics of the IGZO films. The carrier concentration and the Hall mobility of the films decrease monotonically as the oxygen partial pressure during deposition increased. By varying the oxygen partial pressure during deposition from 5 to 80 mTorr, the conductivity of the IGZO films can be varied over several orders of magnitude – from conducting to insulating.

With the ability to control the carrier concentration in the IGZO films, transparent thin film transistors (TFT) were fabricated. IGZO ($InGaZn_5O_8$) TFTs showed an n-type enhancement mode behavior. Typical IGZO TFT characteristics with an ATO insulator were – V_{TH}, μ_{sat}, I_{on}/I_{off}, and subthreshold voltage swing, ~ 2 V, ~14 $cm^2\ V^{-1}\ s^{-1}$, > 10^7, and 200 mV $decade^{-1}$, respectively. The oxygen partial pressure during IGZO deposition was found to

have a profound effect on TFT characteristics. TFTs with 25 mTorr channel layer showed ideal behavior with double (~ 14 $cm^2 V^{-1} s^{-1}$) the mobility compared to a 40 mTorr channel. A large hysteresis is observed in the 40 mTorr film due to the higher interface traps present. The influence of the semiconductor thickness, t_s, was investigated. The variation in μ_{avg} with t_s is minimal (< 15% variation), while V_{on} decreases as t_s increases. TFT characteristics are shown to be dominated by the semiconductor-insulator interface. ATO and AlO_x seem to be relatively optimal candidates for gate insulator while silicon nitride appears to be a poor choice. By utilizing AlO_x with high gate capacitance density, TFTs with low operating voltages (< 5 V) were achieved with good characteristics. Using the channel resistance method the parasitic source-to-drain resistance (normalized for the width of the TFT) was determined to be 23 Ω cm, which indicates a low resistance contact between the ITO and the semiconductor. The mobility shows an almost channel-length independent behavior with mobility decreasing slightly (< 15%) as the channel length varied from 50 μm to 4 μm. Taking advantage of the room temperature process, IGZO TFTs with good characteristics were demonstrated on flexible substrates (PET).

The bias stress stability of IGZO TFTs was evaluated. When a constant positive gate bias stress was applied, a positive threshold shift in the transfer characteristics was observed. The mobility and the sub-threshold voltage swing remain unchanged after the stress indicting that no new defect states were created at the channel/insulator interface after the device was stressed. The threshold voltage shift was observed to be logarithmically dependent on the duration of the bias stress. The logarithmic dependence of the threshold voltage shift on the duration of the bias stress was modeled using simple electrostatic considerations. The validity of the model was verified for both short (10^3 s) and long (10^5 s) stress durations. This logarithmic relationship is representative of charge trapping at the semiconductor/insulator interface. A negative bias stress does not induce a threshold voltage shift due to the unavailability of electrons for the trapping and tunneling process.

A transparent IGZO TFT with non-volatile memory characteristics was developed. Atomic layer deposited platinum nano-particles were incorporated in the gate dielectric stack of the transistor. The Pt-NPs act as a floating gate and charge-trapping layer. The Pt-NPs were in the 2 – 5 nm range and were imaged using several techniques such as FESEM and TEM. The Pt-NP density was determined to be ~ 2 x 10^{12} cm^{-2} and capable to storing 1 to 3 electrons per particle depending on the programming voltage and duration. By applying a positive gate bias the memory device was programmed showing a positive V_{on} shift. The memory window increases with programming duration and which tends to saturate after 3 s. 50% charge retention after 10^6 s and 10% charge retention over 10 years was determined for the memory TFT. A negative bias was unable to erase the device completely and this was explained by the large energy barrier offset for the erase process. Using a UV light source the memory device could be erased showing that the photon energy from the UV illumination was needed to effectively overcome the barrier.

Using room temperature processed transparent IGZO TFTs basic digital circuits such as inverters and ring oscillators were fabricated. The voltage gain of a simple inverter circuit was about 2.5 – 3 and the positive TFT threshold voltage permits the design of circuits without level shifting. 5- and 7-stage ring oscillators were fabricated with different channel lengths (10 μm and 20 μm) and gate and source-drain electrodes overlap (2.5 μm and 5 μm). A 5-stage ring oscillator with a minimum channel length of 10 and a gate and source drain overlap of 2.5 operates at more than 2 MHz, corresponding to a propagation delay of 50 ns per stage at a supply bias of 25 V. The circuits also operate at low voltages with oscillation beginning at a supply voltage of about 6 V. These results demonstrate that an all-transparent and fast circuit can be fabricated with IGZO films at relatively low temperatures.

To explore the suitability of IGZO TFTs as switching transistors an active matrix pixel was fabricated featuring IGZO TFTs and europium doped IGZO as a TFEL phosphor layer. The phosphor demonstrates electroluminescence characteristic of the Eu^{3+} dopant, resulting in emission comparable to that of earlier red TFEL devices. This TFEL device was successfully integrated with and modulated by a TFT by applying a gate voltage in the range

of 8 to 16 V_{DC}, using the TFT channel as a ground path for the TFEL. IGZO TFTs were pulsed at 120 Hz with good transient response, demonstrating IGZO as a viable material for active matrix backplanes. TFT channel geometry is an important consideration for TFEL modulation as the length was observed to affect many facets of the TFEL luminance. These results indicate the viability of IGZO TFTs for active matrix display applications.

8.1 Suggestions for future work

1. Channel material – Multicomponent oxide semiconductors offer an opportunity to vary the ratio of the constituent oxides to effectively give flexibility in the stoichiometry of the oxide used. A systematic method using a combinatorial approach can be used to identify the optimal composition of the oxide for TFT application. While picking a particular composition the entire spectrum of TFT figures-of-merit including, V_{on}, V_{TH}, I_{on}/I_{off}, subthreshold swing and the long-term device stability need to be evaluated.

2. Annealing of thin films and devices – In this dissertation all the pulsed laser depositions were carried out at room temperature with no intentional heating of the layers. Predominantly, the majority of the research on amorphous oxide semiconductor based TFT involves some form of post deposition or post fabrication annealing. Fundamental changes in the semiconducting oxide thin films and the interfaces due to annealing would dictate the properties of the TFTs. Preliminary annealing studies in our group show that annealing at modest temperatures brings about a reduction in the carrier concentration leaving the mobility largely unchanged [150] – Figure 8-1(a). We also observe that the bias stress stability improves with annealing – Figure 8-1(b). This shows that annealing studies on oxide semiconductors is critical.

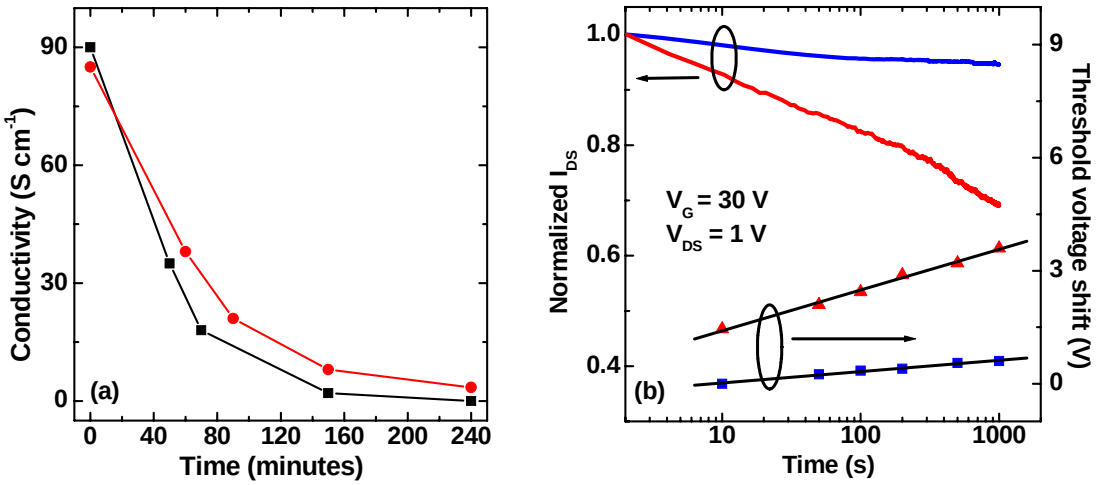

Figure 8-1: (a) Effect of post-deposition annealing in air on electrical conductivity as a function of time for two different temperatures, (●) 175 °C and (■) 200 °C. (b) Evolution of normalized current and threshold voltage shift with bias stressing for an as-processed TFT and a TFT with a post deposition anneal (300 °C for 1 hr in air).

3. Device passivation – Passivation is an integral part of circuit fabrication and integration for the mechanical/chemical protection of devices. Passivation especially on bottom-gated structures, where the back surface is exposed, would modify the entire electrostatics of the TFT. The back surface, which is usually depleted when exposed to air due to oxygen/water vapor being chemisorbed might not be completely depleted or in some cases form an accumulation layer and hence change the V_{on}/V_{TH} of the TFT. Depending on the passivation layer and the method of application the back surface of the semiconductor layer might get damaged. To factor in the changes due to device passivation, the semiconductor layer deposition conditions such as oxygen partial pressure and thickness would need to be optimized and/or post deposition anneals would be necessary. It has been also been reported that passivated TFTs show better bias stress stability compared to unpassivated TFTs making the study of TFT passivation important.

4. Exploration of p-type material – In this dissertation some basic devices such as TFTs and memory elements were demonstrated. A p-n diode was not attempted due to the paucity in p-type oxide semiconductors. Probably the first step would be to develop a p-type

degenerate semiconductor, which might lead to the realization of a p-type oxide semiconductor TFT. P-channel TFTs would in turn lead to a complementary circuit technology. Several potential candidates have been proposed such as NiO, CuO, and SnO. P-type oxides suffer due to low mobility and require a high temperature annealing treatment to improve their performance and also hole injection might be difficult in these films.

5. Gate insulator – Apart from the channel material, the most important component of the TFT is the gate insulator since the carrier flow is at the semiconductor/insulator interface. The insulator dictates the characteristics of the TFTs as shown in this dissertation. Developing a low-temperature insulator with reasonable gate leakage and high capacitance per unit area to minimize device-operating voltages would be of great value. Atomic layer deposition seems to be an attractive method to achieve these characteristics. The compatibility of the insulator with the semiconductor, leading to low interface states and improved device stability, is another critical factor.

6. Devices on flexible substrates – The compatibility of the TFT processing used in this study with flexible substrates was established. Further research is required to completely characterize the TFTs on flexible substrate and to make functional circuits and move towards flexible electronic applications. Especially the stresses involved during flexure and its effect on the TFT characteristics need to be determined.

7. Kinetics of charge trapping – In Chapter 5 it was briefly mentioned that the threshold voltage shift seen after stress biasing recovered when the TFT was left unbiased. Figure 8-2 shows the effect the bias voltage magnitude on V_{TH} recovery. The device stressed at 30 V does not completely recover even after 6 hr. The evaluation of the kinetics of this recovery mechanism would shed more light on the energy levels of the defect states involved in the charge trapping process. Testing the TFTs at different temperatures could be used to extract the activation energy related to this process.

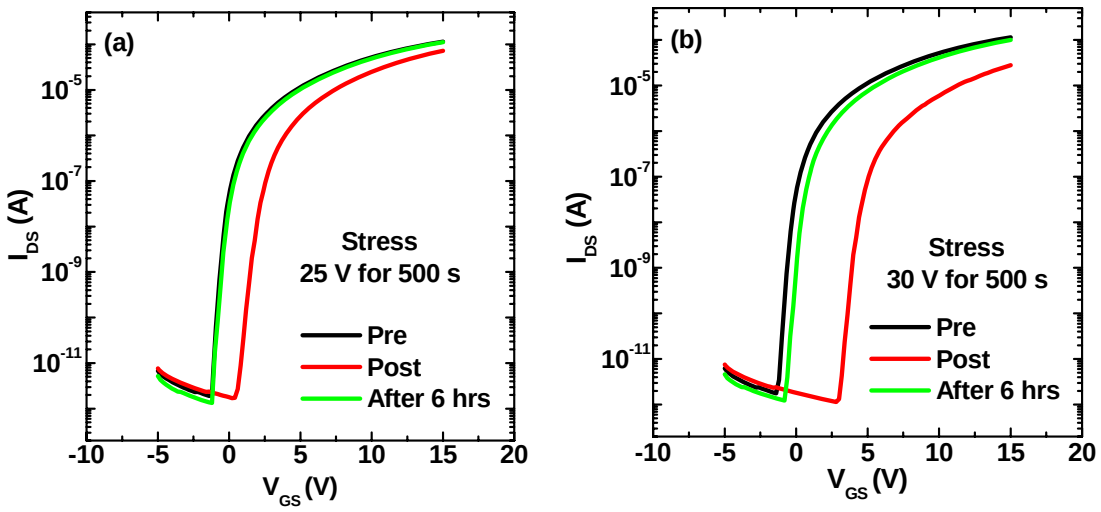

Figure 8-2: The V_{TH} is recovered when the TFT is left unstressed, completely for a TFT stressed at 25 V (a) and partially for a TFT stressed at 30 V (b). Initial stress duration is 500 s.

8. Transistor structure – In this study and predominantly in literature, bottom gated TFT structures are used to evaluate oxide semiconductor TFTs. Design and characterization of top gated TFT structures would be desirable giving more flexibility in integrating these devices. Also the top gated structure could be used to determine the work function values of the various degenerately doped amorphous oxide semiconductors that are available. The top gated structure provides a natural passivation to the semiconductor layer as well.

9. Device integration – Though in this study inverters and ring oscillators using IGZO TFTs were successfully demonstrated, it would be worthwhile to attempt other circuits such as logic gates, current mirrors. Additional requirements or constrains placed by these circuits would be helpful in ascertaining the limits of amorphous oxide semiconductor based devices. The pattering of the active layer (IGZO) in the ROs and pixel structure in this study was by a lift-off process. By developing an etch recipe for IGZO and other layers, smaller devices can be fabricated which potentially would lead to faster circuits and would be helpful to determine the full potential of oxide semiconductors.

REFERENCES

[1] http://www.imdb.com/title/tt0181689/

[2] R. G. Gordon, "Criteria for choosing transparent conductors", MRS Bulletin, vol.25, no.8, pp. 52-57, Aug 2000.

[3] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata and T. Kawai, "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties", Journal of Applied Physics, vol.93, no.3, pp. 1624-1630, Feb 2003.

[4] R. L. Hoffman, B. J. Norris and J. F. Wager, "ZnO-based transparent thin-film transistors", Applied Physics Letters, vol.82, no.5, pp. 733-735, Feb 2003.

[5] P. F. Carcia, R. S. McLean, M. H. Reilly and G. Nunes, "Transparent ZnO thin-film transistor fabricated by RF magnetron sputtering", Applied Physics Letters, vol.82, no.7, pp. 1117-1119, Feb 2003.

[6] H. Hosono, "Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application", Journal of Non-Crystalline Solids, vol.352, pp. 851-858, 2006.

[7] H. Hosono, M. Yasukawa and H. Kawazoe, "Novel oxide amorphous semiconductors: Transparent conducting amorphous oxides", Journal of Non-Crystalline Solids, vol.203, pp. 334-344, 1996.

[8] W. E. Spear and P. G. Lecomber, "Substitutional doping of amorphous silicon", Solid State Communications, vol.17, no.9, pp. 1193-1196, 1975.

[9] H. Hosono, N. Kikuchi, N. Ueda and H. Kawazoe, "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples", Journal of Non-Crystalline Solids, vol.198-200, pp. 165-169, 1996.

[10] H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "Amorphous oxide channel TFTs", Thin Solid Films, vol.516, no.7, pp. 1516-1522, 2008.

[11] J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee and J. M. Kim, "Bottom-gate gallium indium zinc oxide thin-film transistor array for high-resolution AMOLED display", IEEE Electron Device Letters, vol.29, no.12, pp. 1309-1311, Dec 2008.

[12] P. Barquinha, A. M. Vila, G. Goncalves, R. Martins, J. R. Morante, E. Fortunato and L. Pereira, "Gallium-indium-zinc-oxide-based thin-film transistors: Influence of the source/drain material", IEEE Transactions on Electron Devices, vol.55, no.4, pp. 954-960, Apr 2008.

[13] M. Ito, C. Miyazaki, M. Ishizaki, M. Kon, N. Ikeda, T. Okubo, R. Matsubara, K. Hatta, Y. Ugajin and N. Sekine, "Application of amorphous oxide TFT to electrophoretic display", Journal of Non-Crystalline Solids, vol.354 pp. 2777-2782, 2008.

[14] W. B. Jackson, R. L. Hoffman and G. S. Herman, "High-performance flexible zinc tin oxide field-effect transistors", Applied Physics Letters, vol.87, no.19, Nov 2005.

[15] P. Gorrn, M. Lehnhardt, T. Riedl and W. Kowalsky, "The influence of visible light on transparent zinc tin oxide thin film transistors", Applied Physics Letters, vol.91, no.19, Nov 2007.

[16] I. Song, S. Kim, H. X. Yin, C. J. Kim, J. Park, H. S. Choi, E. Lee and Y. Park, "Short channel characteristics of gallium-indium-zinc-oxide thin film transistors for three-dimensional stacking memory", IEEE Electron Device Letters, vol.29, no.6, pp. 549-552, Jun 2008.

[17] P. Gorrn, P. Holzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze and S. Kipp, "Stability of transparent zinc tin oxide transistors under bias stress", Applied Physics Letters, vol.90, no.6, Feb 2007.

[18] P. Gorrn, M. Sander, J. Meyer, M. Kroger, E. Becker, H. H. Johannes, W. Kowalsky and T. Riedl, "Towards see-through displays: Fully transparent thin-film transistors driving transparent organic light-emitting diodes", Advanced Materials, vol.18, no.6, pp. 738-+, Mar 2006.

[19] N. Hiratsuka, A. Hosoi, H. Kobayashi and K. Kakizaki, "Isobutane gas sensing characteristics of zinc-tin complex oxide system", Journal of the Ceramic Society of Japan, vol.104, no.12, pp. 1158-1159, Dec 1996.

[20] G. Eranna, B. C. Joshi, D. P. Runthala and R. P. Gupta, "Oxide materials for development of integrated gas sensors - a comprehensive review", Critical Reviews in Solid State and Materials Sciences, vol.29, no.3-4, pp. 111-188 2004.

[21] H. Koinuma, "Chemistry and electronics of oxides from carbon dioxide to perovskite", Thin Solid Films, vol.486, pp. 2-10, 2005.

[22] "*Thin films and heterostructures for oxide electronics*" Ed. S. B. Ogale, Springer

(New york), 2005.

[23] J. P. Locquet, C. Marchiori, M. Sousa, J. Fompeyrine and J. W. Seo, "High-k dielectrics for the gate stack", Journal of Applied Physics, vol.100, no.5, Sep 2006.

[24] R. E. Jones, P. Zurcher, P. Chu, D. J. Taylor, Y. T. Lii, B. Jiang, P. D. Maniar and S. J. Gillespie, "Memory applications based on ferroelectric and high-permittivity dielectric thin films", Microelectronic Engineering, vol.29, no.1-4, pp. 3-10, 1995.

[25] M. Bibes and A. Barthelemy, “Oxide spintronics”, IEEE Transactions on Electron Devices, vol. 54, no. 5, pp. 1003-1023, May 2007.

[26] S. Liang, H. Sheng, Y. Liu, Z. Huo, Y. Lu and H. Shen, "ZnO schottky ultraviolet photodetectors", Journal of Crystal Growth, vol.225, no.2-4, pp. 110-113, 2001.

[27] K. Koike, K. Hama, I. Nakashima, G. Takada, K. Ogata, S. Sasa, M. Inoue and M. Yano, "Molecular beam epitaxial growth of wide bandgap ZnMgo alloy films on (111)-oriented Si substrate toward UV-detector applications", Journal of Crystal Growth, vol.278, no.1-4, pp. 288-292, 2005.

[28] T. Kamiya and H. Hosono, "Creation of new functions in transparent oxides utilizing nanostructures embedded in crystal and artificially encoded by laser pulses", Semiconductor Science and Technology, vol.20, no.4, pp. S92-S102, Apr 2005.

[29] T. Minami, "Transparent conducting oxide semiconductors for transparent electrodes", Semiconductor Science and Technology, vol.20, no.4, pp. S35-S44, Apr 2005.

[30] H. Hosono, H. Ohta, M. Orita, K. Ueda and M. Hirano, "Frontier of transparent conductive oxide thin films", Vacuum, vol.66, pp. 419-425, 2002.

[31] T. Tomita, K. Yamashita, Y. Hayafuji and H. Adachi, "The origin of n-type conductivity in undoped In_2O_3", Applied Physics Letters, vol.87, no.5, Aug 2005.

[32] Z. Ovadyahu, B. Ovryn and H. W. Kraner, "Microstructure and electro-optical properties of evaporated indium-oxide films", Journal of the Electrochemical Society, vol.130, no.4, pp. 917-921 1983.

[33] C. P. Liu and G. R. Jeng, "Properties of aluminum doped zinc oxide materials and sputtering thin films", Journal of Alloys and Compounds, vol.468, no.1-2, pp. 343-349, Jan 2009.

[34] J. R. Bellingham, W. A. Phillips and C. J. Adkins, "Intrinsic performance limits in

transparent conducting oxides", Journal of Materials Science Letters, vol.11, no.5, pp. 263-265, Mar 1992.

[35] T. J. Coutts, D. L. Young, X. Li, W. P. Mulligan and X. Wu, "Search for improved transparent conducting oxides: A fundamental investigation of CdO, Cd_2SnO_4, and Zn_2SnO_4", Journal of Vacuum Science & Technology a-Vacuum Surfaces and Films, vol.18, no.6, pp. 2646-2660, Nov-Dec 2000.

[36] B. Szyszka, V. Sittinger, X. Jiang, R. J. Hong, W. Werner, A. Pflug, M. Ruske and A. Lopp, "Transparent and conductive ZnO:Al films deposited by large area reactive magnetron sputtering", Thin Solid Films, vol.442, pp. 179-183, 2003.

[37] E. P. Denton, H. Rawson and J. E. Stanworth, "Vanadate glasses", Nature, vol.173, no.4413, pp. 1030-1032 1954.

[38] H. Mori, H. Matsuno and H. Sakata, "Small polaron hopping conduction in V_2O_5-TeO_2 glasses", Journal of Non-Crystalline Solids, vol.276, no.1-3, pp. 78-94, Oct 2000.

[39] M. Yasukawa, H. Hosono, N. Ueda and H. Kawazoe, "Preparation of electroconductive and transparent thin-films of $AgSbO_3$", Journal of the Ceramic Society of Japan, vol.103, no.5, pp. 455-459, May 1995.

[40] H. Hosono, N. Kikuchi, N. Ueda, H. Kawazoe and K. Shimidzu, "Amorphous transparent electroconductor $2CdO.GeO_2$ - conversion of amorphous insulating cadmium germanate by ion-implantation", Applied Physics Letters, vol.67, no.18, pp. 2663-2665, Oct 1995.

[41] H. Hosono, Y. Yamashita, N. Ueda, H. Kawazoe and K. Shimidzu, "New amorphous semiconductor: $2CdO.PbO_x$", Applied Physics Letters, vol.68, no.5, pp. 661-663, Jan 1996.

[42] H. Hosono, H. Unno, N. Ueda, H. Kawazoe, N. Matsunami and H. Tanoue, "Conversion of insulating thin films of $MgIn_2O_4$ into transparent conductors by ion implantation", Nuclear Instruments and Methods in Physics Research B, vol.106, pp. 517-521, 1995.

[43] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", Nature, vol.432, no.7016, pp. 488-492, Nov 2004.

[44] Elliott, S. R., *Physics of Amorphous Materials,* second edition (London: Longman), 1990.

[45] K. Shimakawa, S. Narushima, H. Hosono and H. Kawazoe, "Electronic transport in degenerate amorphous oxide semiconductors", Philosophical Magazine Letters, vol.79, no.9, pp. 755-761, Sep 1999.

[46] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong and D. A. Keszler, "High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer", Applied Physics Letters, vol.86, no.1, Jan 2005.

[47] R. L. Hoffman, "Effects of channel stoichiometry and processing temperature on the electrical characteristics of zinc tin oxide thin-film transistors", Solid-State Electronics, vol.50, no.5, pp. 784-787, May 2006.

[48] M. K. Jayaraj, K. J. Saji, K. Nomura, T. Kamiya and H. Hosono, "Optical and electrical properties of amorphous zinc tin oxide thin films examined for thin film transistor application", Journal of Vacuum Science & Technology B, vol.26, no.2, pp. 495-501, Mar-Apr 2008.

[49] N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, C. H. Park and D. A. Keszler, "Transparent thin-film transistors with zinc indium oxide channel layer", Journal of Applied Physics, vol.97, no.6, Mar 2005.

[50] P. Barquinha, A. Pimentel, A. Marques, L. Pereira, R. Martins and E. Fortunato, "Influence of the semiconductor thickness on the electrical properties of transparent TFTs based on indium zinc oxide", Journal of Non-Crystalline Solids, vol.352, pp. 1749-1752, 2006.

[51] H. Q. Chiang, D. Hong, C. M. Hung, R. E. Presley, J. F. Wager, C. H. Park, D. A. Keszler and G. S. Herman, "Thin-film transistors with amorphous indium gallium oxide channel layers", Journal of Vacuum Science & Technology B, vol.24, no.6, pp. 2702-2705, Nov-Dec 2006.

[52] R. E. Presley, D. Hong, H. Q. Chiang, C. M. Hung, R. L. Hoffman and J. F. Wager, "Transparent ring oscillator based on indium gallium oxide thin-film transistors", Solid-State Electronics, vol.50, no.3, pp. 500-503, Mar 2006.

[53] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature RF-magnetron sputtering", Applied Physics Letters, vol.89, no.11, Sep 2006.

[54] J. H. Noh, C. S. Kim, S. Y. Ryu and S. J. Jo, "Low-voltage-driven bottom-gate amorphous indium-gallium-zinc-oxide thin-film transistors with high dielectric

constant oxide/polymer double-layer dielectric", Japanese Journal of Applied Physics Part 1-Regular Papers Brief Communications & Review Papers, vol.46, no.7A, pp. 4096-4098, Jul 2007.

[55] W. T. Lim, J. H. Jang, S. H. Kim, D. P. Norton, V. Craciun, S. J. Pearton, F. Ren and H. Shen, "High performance indium gallium zinc oxide thin film transistors fabricated on polyethylene terephthalate substrates", Applied Physics Letters, vol.93, no.8, Aug 2008.

[56] M. Nakamura, N. Kimizuka and T. Mohri, "The phase-relations in the In_2O_3-Ga_2ZnO_4-ZnO system at 1350 ºC", Journal of Solid State Chemistry, vol.93, no.2, pp. 298-315, Aug 1991.

[57] T. Moriga, D. R. Kammler, T. O. Mason, G. B. Palmer and K. R. Poeppelmeier, "Electrical and optical properties of transparent conducting homologous compounds in the indium-gallium-zinc oxide system", Journal of the American Ceramic Society, vol.82, no.10, pp. 2705-2710, Oct 1999.

[58] M. Orita, H. Ohta, H. Hosono, K.Morita, H. Tanji, and H. Kawazoe, “Properties of a novel amorphous transparent conductive oxide, $InGaO_3(ZnO)_m$,” Materials Research Society Symposium, vol. 623, pp. 291–296, 2000.

[59] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors", Japanese Journal of Applied Physics, vol.45, no.5B, pp. 4303-4308, 2006.

[60] K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano and H. Hosono, "Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-o: Experiment and ab initio calculations", Physical Review B, vol.75, no.3, Jan 2007.

[61] K. Nomura, T. Kamiya, H. Ohta, K. Ueda, M. Hirano and H. Hosono, "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline $InGaO_3(ZnO)_5$ films", Applied Physics Letters, vol.85, no.11, pp. 1993-1995, Sep 2004.

[62] A. C. Tickle, *Thin-film transistors a new approach to microelectronics*, John Wiley & Sons Inc., 1969.

[63] J. E. Lilienfeld, “Device for controlling electric current.” US Pat. 1,900,018, 1933.

[64] P. K. Weimer, "TFT - new thin-film transistor", Proceedings of the Institute of Radio Engineers, vol.50, no.6, pp. 1462-& 1962.

[65] C. R. Kagan and P. Andry, *Thin-film transistors*. New York: Marcel Dekker, Inc., 2003.

[66] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances", IBM Journal of Research and Development, vol.45, no.1, pp. 11-27, Jan 2001.

[67] R. J. Chesterfield, C. R. Newman, T. M. Pappenfus, P. C. Ewbank, M. H. Haukaas, K. R. Mann, L. L. Miller and C. D. Frisbie, "High electron mobility and ambipolar transport in organic thin-film transistors based on a pi-stacking quinoidal terthiophene", Advanced Materials, vol.15, no.15, pp. 1278-+, Aug 2003.

[68] J. F. Wager, D. A. Keszler, and R. E. Presley, *Transparent Electronics*. New York: Springer, 2008.

[69] R. L. Hoffman, "ZnO-channel thin-film transistors: Channel mobility", Journal of Applied Physics, vol.95, no.10, pp. 5813-5819, May 2004.

[70] S. Sze, *Physics of Semiconductor Devices*. New York: John Wiley & Sons, 1981.

[71] C. G. Choi, S. J. Seo and B. S. Bae, "Solution-processed indium-zinc oxide transparent thin-film transistors", Electrochemical and Solid State Letters, vol.11, no.1, pp. H7-H9 2008.

[72] S. J. Lim, S. J. Kwon, H. Kim and J. S. Park, "High performance thin film transistor with low temperature atomic layer deposition nitrogen-doped ZnO", Applied Physics Letters, vol.91, no.18, Oct 2007.

[73] J. Jo, O. Seo, E. Jeong, H. Seo, B. Lee and Y. I. Choi, "Effect of hydrogen in zinc oxide thin-film transistor grown by metal organic chemical vapor deposition", Japanese Journal of Applied Physics, vol.46, no.4B, pp. 2493-2495, 2007.

[74] P. K. Shin, Y. Aya, T. Ikegami and K. Ebihara, "Application of pulsed laser deposited zinc oxide films to thin film transistor device", Thin Solid Films, vol.516, no.12, pp. 3767-3771, Apr 2008.

[75] E. M. C. Fortunato, P. M. C. Barquinha, A. Pimentel, A. M. F. Goncalves, A. J. S. Marques, L. M. N. Pereira and R. F. P. Martins, "Fully transparent ZnO thin-film transistor produced at room temperature", Advanced Materials, vol.17, no.5, pp. 590-+, Mar 2005.

[76] P. F. Carcia, R. S. McLean and M. H. Reilly, "Oxide engineering of ZnO thin-film transistors for flexible electronics", Journal of the Society for Information Display,

vol.13, no.7, pp. 547-554, Jul 2005.

[77] B. J. Norris, J. Anderson, J. F. Wager and D. A. Keszler, "Spin-coated zinc oxide transparent transistors", Journal of Physics D-Applied Physics, vol.36, no.20, pp. L105-L107, Oct 2003.

[78] C. S. Li, Y. N. Li, Y. L. Wu, B. S. Ong and R. O. Loutfy, "Performance improvement for solution-processed high-mobility ZnO thin-film transistors", Journal of Physics D-Applied Physics, vol.41, no.12, Jun 2008.

[79] H. C. Cheng, C. F. Chen and C. C. Lee, "Thin-film transistors with active layers of zinc oxide (ZnO) fabricated by low-temperature chemical bath method", Thin Solid Films, vol.498, pp. 142-145, 2006.

[80] J. Zhu, H. Chen, G. Saraf, Z. Duan, Y. Lu and S. T. Hsu, "ZnO TFT devices built on glass substrates", Journal of Electronic Materials, vol.37, no.9, pp. 1237-1240, 2008.

[81] J. Jo, O. Seo, H. Choi and B. Lee, "Enhancement-mode ZnO thin-film transistor grown by metal organic chemical vapor deposition", Applied Physics Express, vol.1, no.4, Apr 2008.

[82] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan and L. M. Irving, "Stable ZnO thin film transistors by fast open air atomic layer deposition", Applied Physics Letters, vol.92, no.19, May 2008.

[83] F. M. Hossain, J. Nishii, S. Takagi, A. Ohtomo, T. Fukumura, H. Fujioka, H. Ohno, H. Koinuma and M. Kawasaki, "Modeling and simulation of polycrystalline ZnO thin-film transistors", Journal of Applied Physics, vol.94, no.12, pp. 7768-7777, Dec 2003.

[84] L. Wang, M. H. Yoon, G. Lu, Y. Yang, A. Facchetti and T. J. Marks, "High-performance transparent inorganic-organic hybrid thin-film n-type transistors", Nature Materials, vol.5, no.11, pp. 893-900, Nov 2006.

[85] Y. Vygranenko, K. Wang, M. Vieira and A. Nathan, "Indium oxide thin-film transistor by reactive ion beam assisted deposition", Physica Status Solidi A, vol.205, no.8, pp. 1925-1928, 2008.

[86] K. Matsuzaki, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, "Growth, structure and carrier transport properties of Ga_2O_3 epitaxial film examined for transparent field-effect transistor", Thin Solid Films, vol.496, no.1, pp. 37-41, 2006.

[87] R. E. Presley, C. L. Munsee, C. H. Park, D. Hong, J. F. Wager and D. A. Keszler, "Tin oxide transparent thin-film transistors", Journal of Physics D-Applied Physics, vol.37, no.20, pp. 2810-2813, Oct 2004.

[88] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, "P-channel thin-film transistor using p-type oxide semiconductor, SnO", Applied Physics Letters, vol.93, no.3, Jul 2008.

[89] E. N. Dattoli, Q. Wan, W. Guo, Y. B. Chen, X. Q. Pan and W. Lu, "Fully transparent thin-film transistor devices based on SnO_2 nanowires", Nano Letters, vol.7, no.8, pp. 2463-2469, Aug 2007.

[90] S. Y. Ju, P. C. Chen, C. W. Zhou, Y. G. Ha, A. Facchetti, T. J. Marks, S. K. Kim, S. Mohammadi and D. B. Janes, "1/f noise of SnO_2 nanowire transistors", Applied Physics Letters, vol.92, no.24, Jun 2008.

[91] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor", Science, vol.300, no.5623, pp. 1269-1272, May 2003.

[92] T. Iwasaki, N. Itagaki, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "Combinatorial approach to thin-film transistors using multicomponent semiconductor channels: An application to amorphous oxide semiconductors in In-Ga-Zn-O system", Applied Physics Letters, vol.90, no.24, Jun 2007.

[93] R. Hayashi, M. Ofuji, N. Kaji, K. Takahashi, K. Abe, H. Yabuta, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano and H. Hosono, "Circuits using uniform TFTs based on amorphous In-Ga-Zn-O", Journal of the Society for Information Display, vol.15, no.11, pp. 915-921, 2007.

[94] J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim and S. I. Kim, "Improvements in the device characteristics of amorphous indium gallium zinc oxide thin-film transistors by Ar plasma treatment", Applied Physics Letters, vol.90, no.26, Jun 2007.

[95] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. S. Park, J. K. Jeong, Y. G. Mo and H. D. Kim, "High mobility bottom gate InGaZnO thin film transistors with SiO_x etch stopper", Applied Physics Letters, vol.90, no.21, May 2007.

[96] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park and J. Chung, "Amorphous gallium indium zinc oxide thin film transistors: Sensitive to oxygen molecules", Applied Physics Letters, vol.90, no.19, May 2007.

[97] J. H. Jeong, H. W. Yang, J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim, J. Song and C.

S. Hwang, "Origin of subthreshold swing improvement in amorphous indium gallium zinc oxide transistors", Electrochemical and Solid State Letters, vol.11, no.6, pp. H157-H159 2008.

[98] J. S. Park, J. K. Jeong, H. J. Chung, Y. G. Mo and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water", Applied Physics Letters, vol.92, no.7, Feb 2008.

[99] J. Park, I. Song, S. Kim, C. Kim, J. Lee, H. Lee, E. Lee, H. Yin, K. K. Kim, K. W. Kwon and Y. Park, "Self-aligned top-gate amorphous gallium indium zinc oxide thin film transistors", Applied Physics Letters, vol.93, no.5, Aug 2008.

[100] H. Lim, H. Yin, J. S. Park, I. Song, C. Kim, J. Park, S. Kim, S. W. Kim, C. B. Lee, Y. C. Kim, Y. S. Park and D. Kang, "Double gate GaInZnO thin film transistors", Applied Physics Letters, vol.93, no.6, Aug 2008.

[101] H. Q. Chiang, B. R. McFarlane, D. Hong, R. E. Presley and J. F. Wager, "Processing effects on the stability of amorphous indium gallium zinc oxide thin-film transistors", Journal of Non-Crystalline Solids, vol.354, no.19-25, pp. 2826-2830, 2008.

[102] G. H. Kim, H. S. Shin, B. D. Ahn, K. H. Kim, W. J. Park and H. J. Kim, "Formation mechanism of solution-processed nanocrystalline InGaZnO thin film as active channel layer in thin-film transistor", Journal of the Electrochemical Society, vol.156, no.1, pp. H7-H9 2009.

[103] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, New York: Oxford University Press, fourth edition, 1998.

[104] M. Ofuji, K. Abe, H. Shimizu, N. Kaji, R. Hayashi, M. Sano, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "Fast thin-film transistor circuits based on amorphous oxide semiconductor", IEEE Electron Device Letters, vol.28, no.4, pp. 273-275, Apr 2007.

[105] J. Sun, D. A. Mourey, D. L. Zhao and T. N. Jackson, "ZnO thin film, device, and circuit fabrication using low-temperature PECVD processes", Journal of Electronic Materials, vol.37, no.5, pp. 755-759, May 2008.

[106] J. Sun, D. A. Mourey, D. L. Zhao, S. K. Park, S. F. Nelson, D. H. Levy, D. Freeman, P. Cowdery-Corvan, L. Tutt and T. N. Jackson, "ZnO thin-film transistor ring oscillators with 31-ns propagation delay", IEEE Electron Device Letters, vol.29, no.7, pp. 721-723, Jul 2008.

[107] H. Yin, S. Kim, C. J. Kim, J. C. Park, I. Song, S.-W. Kim, S.-H. Lee and Y. Park, “Bootstrapped ring oscillator with propagation delay time below 1.0 nsec/stage by standard 0.5μm bottom-gate amorphous Ga_2O_3-In_2O_3-ZnO TFT technology”, IEEE International Electron Devices Meeting, pp. 1-4, Dec 2008.

[108] J. K. Jeong, J. H. Jeong, H. W. Yang, T. K. Ahn, M. Kim, K. S. Kim, B. S. Gu, H. J. Chung, J. S. Park, Y. G. Mo, H. D. Kim and H. K. Chung, "12.1-in. WXGA AMOLED display driven by InGaZnO thin-film transistors", Journal of the Society for Information Display, vol.17, no.2, pp. 95-100, 2009.

[109] S. Ju, J. F. Li, J. Liu, P. C. Chen, Y. G. Ha, F. Ishikawa, H. Chang, C. W. Zhou, A. Facchetti, D. B. Janes and T. J. Marks, "Transparent active matrix organic light-emitting diode displays driven by nanowire transistor circuitry", Nano Letters, vol.8, no.4, pp. 997-1004, Apr 2008.

[110] M. J. Powell, C. Vanberkel, I. D. French and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous-silicon thin-film transistors", Applied Physics Letters, vol.51, no.16, pp. 1242-1244, Oct 1987.

[111] M. J. Powell, C. Vanberkel and J. R. Hughes, "Time and temperature-dependence of instability mechanisms in amorphous-silicon thin-film transistors", Applied Physics Letters, vol.54, no.14, pp. 1323-1325, Apr 1989.

[112] M. J. Powell, "Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors", Applied Physics Letters, vol.43, no.6, pp. 597-599 1983.

[113] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time-dependence of charge injection and trapping in amorphous thin-film transistors", Applied Physics Letters, vol.62, no.11, pp. 1286-1288, Mar 1993.

[114] R. Navamathavan, E. J. Yang, J. H. Lim, D. K. Hwang, J. Y. Oh, J. H. Yang, J. H. Jang and S. J. Park, "Effects of electrical bias stress on the performance of ZnO-based TFTs fabricated by RF magnetron sputtering", Journal of the Electrochemical Society, vol.153, no.5, pp. G385-G388 2006.

[115] R. B. M. Cross and M. M. De Souza, "Investigating the stability of zinc oxide thin film transistors", Applied Physics Letters, vol.89, no.26, Dec 2006.

[116] J. S. Park, K. Kim, Y. G. Park, Y. G. Mo, H. D. Kim and J. K. Jeong, "Novel ZrInZnO thin-film transistor with excellent stability", Advanced Materials, vol.21, no.3, pp. 329-333, Jan 2009.

[117] S. J. Seo, C. G. Choi, Y. H. Hwang and B. S. Bae, "High performance solution-

processed amorphous zinc tin oxide thin film transistor", Journal of Physics D-Applied Physics, vol.42, no.3, Feb 2009.

[118] I. T. Cho, J. M. Lee, J. H. Lee and H. I. Kwon, "Charge trapping and detrapping characteristics in amorphous InGaZnO TFTs under static and dynamic stresses", Semiconductor Science and Technology, vol.24, no.1, Jan 2009.

[119] J. K. Jeong, H. W. Yang, J. H. Jeong, Y. G. Mo and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors", Applied Physics Letters, vol.93, no.12, Sep 2008.

[120] S.M. Green, A. Piqué and K.S. Harshavardhan, in *Pulsed Laser Deposition of Thin Films*, edited by D.B. Chrisey and G.K. Hubler (Wiley, New York), pp. 23-54 (1994).

[121] Stephen A. Campbell, *Fabrication Engineering at the Micro- and Nanoscale*, New York Oxford University Press 2008.

[122] Jill Svenja Becker, *Atomic layer deposition of metal oxide and nitride thin films*, PhD thesis, Harvard University, 2002.

[123] http://www.cambridgenanotech.com/cnpruploads/ALD_Tutorial_optfinal_2008.pdf

[124] T. Aaltonen, M. Ritala, T. Sajavaara, J. Keinonen and M. Leskela, "Atomic layer deposition of platinum thin films", Chemistry of Materials, vol.15, no.9, pp. 1924-1928, May 2003.

[125] D. K. Schroeder, *Semiconductor Material and Device Characterization*. New York: John Wiley & Sons, Inc., 1998.

[126] NIST Electronics and Electrical Engineering Laboratory Hall effect measurements website - http://www.eeel.nist.gov/812/hall.html

[127] N. Ueda, H. Hosono, R. Waseda and H. Kawazoe, "Anisotropy of electrical and optical properties in beta-Ga_2O_3 single crystals", Applied Physics Letters, vol.71, no.7, pp. 933-935, Aug 1997.

[128] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-$InGaZnO_4$", pp. 38-41, 2005.

[129] P. Barquinha, E. Fortunato, A. Goncalves, A. Pimentel, A. Marques, L. Pereira and R. Martins, "Influence of time, light and temperature on the electrical properties of zinc oxide TFTs", Superlattices and Microstructures, vol.39, no.1-4, pp. 319-327, 2006.

[130] S. Martin, C. S. Chiang, J. Y. Nahm, T. Li, J. Kanicki and Y. Ugai, "Influence of the amorphous silicon thickness on top gate thin-film transistor electrical performances", Japanese Journal of Applied Physics Part 1, vol.40, no.2A, pp. 530-537, Feb 2001.

[131] S. Yaginuma, J. Yamaguchi, K. Itaka and H. Koinuma, "Pulsed laser deposition of oxide gate dielectrics for pentacene organic field-effect transistors", Thin Solid Films, vol.486, pp. 218-221, 2005.

[132] J. G. J. Chern, P. Chang, R. F. Motta and N. Godinho, "A new method to determine MOSFET channel length", Electron Device Letters, vol.1, no.9, pp. 170-173 1980.

[133] A. Sato, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano and H. Hosono, "Amorphous In-Ga-Zn-O coplanar homojunction thin-film transistor", Applied Physics Letters, vol.94, no.13, Mar 2009.

[134] J. K. Jeong, H. J. Chung, Y. G. Mo and H. D. Kim, "Comprehensive study on the transport mechanism of amorphous indium-gallium-zinc oxide transistors", Journal of the Electrochemical Society, vol.155, no.11, pp. H873-H877 2008.

[135] K. S. Karim, A. Nathan, M. Hack and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs", IEEE Electron Device Letters, vol.25, no.4, pp. 188-190, Apr 2004.

[136] J. F. Yuan, J. D. Zhang, J. Wang, D. H. Yan and W. Xu, "Study on the instability of organic field-effect transistors based on fluorinated copper phthalocyanine", Thin Solid Films, vol.450, no.2, pp. 316-319, Mar 2004.

[137] A. V. Ferrisprabhu, "Charge-transfer by direct tunneling in thin-oxide memory transistors", IEEE Transactions on Electron Devices, vol.24, no.5, pp. 524-530 1977.

[138] S. Novak, B. Lee, and V. Misra, “Platinum nano-particles grown by atomic layer deposition for non-volatile charge storage memory applications” (unpublished).

[139] Y. Kuo and H. Nominanda, "Nonvolatile hydrogenated-amorphous-silicon thin-film-transistor memory devices", Applied Physics Letters, vol.89, no.17, Oct 2006.

[140] C. Novembre, D. Guerin, K. Lmimouni, C. Gamrat and D. Vuillaume, "Gold nanoparticle-pentacene memory transistors", Applied Physics Letters, vol.92, no.10, Mar 2008.

[141] J. H. Kim, K. H. Baek, C. K. Kim, Y. B. Kim and C. S. Yoon, "Formation of gold

nanoparticles embedded in a polyimide film for nanofloating gate memory", Applied Physics Letters, vol.90, no.12, Mar 2007.

[142] W. R. Chen, T. C. Chang, P. T. Liu, C. H. Tu, J. L. Yeh, Y. T. Hsieh, R. Y. Wang and C. Y. Chang, "Formation of germanium nanocrystals by rapid thermal oxidizing SiGeO layer for nonvolatile memory application", Surface and Coatings Technology, vol.202, pp. 1333-1337, 2007.

[143] Lenzling.M and E. H. Snow, "Fowler-nordheim tunneling into thermally grown SiO_2", Journal of Applied Physics, vol.40, no.1, pp. 278-& 1969.

[144] H. T. Lin, Z. W. Pei, J. R. Chen and Y. J. Chan, "A UV-erasable stacked diode-switch organic nonvolatile bistable memory on plastic substrates", IEEE Electron Device Letters, vol.30, no.1, pp. 18-20, Jan 2009.

[145] S. K. Park, D. A. Mourey, S. Subramanian, J. E. Anthony and T. N. Jackson, "Polymeric substrate spin-cast diF-TESADT OTFT circuits", IEEE Electron Device Letters, vol.29, no.9, pp. 1004-1006, Sep 2008.

[146] T. D. Anthopoulos, B. Singh, N. Marjanovic, N. S. Sariciftci, A. M. Ramil, H. Sitter, M. Colle and D. M. de Leeuw, "High performance n-channel organic field-effect transistors and ring oscillators based on C60 fullerene films", Applied Physics Letters, vol.89, no.21, Nov 2006.

[147] Sung Kyu Park, *High mobility solution processed organic thin film transistors*, PhD thesis, Pennsylvania State University, 2007.

[148] P. Wellenius, A. Suresh, and J. F. Muth, “An Amorphous IGZO Rare Earth Doped Luminescent Phosphor”, Materials Research Society Symposium Proceedings, Vol. 1111**,** 1111-D08-03 (2009).

[149] P.D. Rack, and P.H. Holloway, “The structure, device physics, and material properties of thin film electroluminescent displays,” Materials Science and Engineering, R21, pp. 171-219, 1997.

[150] Praveen Gollakota, *Investigation of europium doped wide band gap oxides and an annealing study of the amorphous oxide semiconductor – indium gallium zinc oxide*, Masters thesis, North Carolina State University, 2007.