ABSTRACT

JUNG, JEESUNG. Integrated Single Pole Double Throw (SPDT) Vertical Power MOSFETs for High Current and Fast Frequency Monolithic Synchronous Converters. (Under the direction of Dr. Alex Q. Huang.)

The SPDT switch is implemented by two integrated vertical-structure power MOSFETs for the first time. In other words, a high current handling monolithic synchronous converter, based on both a control and a synchronous vertical MOSFET structure is proposed. The power switches are designed as combining the advantages of both conventional lateral- and vertical-type MOSFETs. Therefore, the lowest FOMs among the same voltage-rating devices as well as the high operating current handling capability have been achieved. Besides, various integrated devices such as analog/digital Complementary Metal Oxide Semiconductor (CMOS) Devices and Bipolar Junction Transistor (BJT)s show good performances as power stage driver and controller ones at the same time. In addition, the new monolithic design challenges such as isolations and parasitic devices are addressed and possible solutions are verified not only by state of the art device/circuit simulations but also by experiments. The new concept of the controlled CMOS p-body voltage which can subdue the parasitic effects dramatically and increase the reliability providing full flexibility of integration is explained, also. Eventually, novel BCD (Bipolar-CMOS-DMOS) process which is optimized to achieve all goals above is developed. And the most challengeable non-standard CMOS process of the current path-trench fabrication is investigated in details and tested physically and electrically. Though the buck converter is selected and analyzed in details in this dissertation due to its popularity, the proposed SPDT switch can be used for other SMPS (Switch Mode Power Supply) converters such as a boost or a buck-boost converter, also. Therefore, this dissertation should build a strong motivation for the practical implementation of the new SOC (System On a Chip)-high current and fast frequency handling power converter design for the first time.
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Integrated Single Pole Double Throw (SPDT) Vertical Power MOSFETs for High Current and Fast Frequency Monolithic Synchronous Converters

by
Jeeseung Jung

A dissertation submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the Degree of Doctor of Philosophy

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APPROVED BY:

Dr. Subhashish Bhattacharya
Dr. Veena Misra

Dr. Alex Q. Huang
Chair of Advisory Committee
Dr. Kevin G. Gard
DEDICATION

To my LORD and FAMILY with my sincere LOVE

• To my extra-ordinary Wife, Bokyung Choi

• To my extra-lovely Children, Daniel and Christopher Jung

• To my extra-reliable Parents and Parents-in-law

• To my extra-admirable Sisters and Brothers-in-law
BIOGRAPHY

The author, Jeesung Jung, received B.S. degree in electrical engineering from Korea University, Seoul, Korea, in 2002, and M.S. degree in electrical and computer engineering from North Carolina State University, Raleigh, in 2005. He worked for SAMSUNG Electronics, Korea as a Low-Power Portable System Design Research Engineer and has been qualified as a 6-sigma green belt engineer from the same company in 2003. He started his Master graduate program study as a recipient of Engineering Foundation Graduate Study Abroad Scholarship awarded by Korea Government from 2003. And he has been selected as a Honor Society of Phi Kappa Phi member in the following year of 2004. He joined Semiconductor Power Electronics Center, North Carolina State University, Raleigh, from 2004 as a Research Assistant with his advisor Dr. Alex Q. Huang during his Master program. And he has continued his research at the same center as pursuing Ph.D. degree from 2005. His current research interests include Power Semiconductor Devices Design, BCD fabrication Process Developments and power Integrated Circuits design for SMART Power IC and Power Management Microsystems.
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Chapter 1

Introduction

1.1 Motivation

In the current power architecture for computer systems, the large operating current and the low input voltage are required for several major blocks such as CPU, I/O power, graphics, memories (DDR) etc., shown in Fig. 1.1 [13] [14] [15]. Therefore, voltage regulator (VR)s in the system need to not only convert the main bus voltage coming from the AC/DC adapter to the low voltage but also supply high current into the blocks [16]. Fig. 1.2 (a) shows the current power MOSFET application map [2]. The low voltage power MOSFETs used in a DC-DC converter VRMs require more than 10A drain current, which is quite challengeable for modern SOC (System On a Chip) technology. Fig. 1.2 (b) shows the kind of operating conditions in which power MOSFET applications are used, with load inductance and operating frequency as parameters [3]. The DC-DC converters in the red-rectangle are our main target and these are operated in between 100K (hz) and 1M (hz) frequency range and need several tens micro-capacitance which consumes large area. And the high operating frequency is another VR required-trend to reduce passive components consumed area [17] [18]. It means that the VRs which are operated in above ~ Mhz range switching frequency are essential in the near future. In addition, because the high-operating current is required at the same time, the $di/dt$ will become very high and the parasitic inductors-effect may cause severe problems. Therefore, the monolithic power converter design has become more and more important.

As the device technology is progressed, higher current and lower output voltage
Figure 1.1: The current power architecture for a laptop system: A blue rectangle indicates the VR bus input voltage and red ones do the components which require the high operating current and VRs. [2]

VRs become essential shown in Fig.1.3 [3] [4]. In addition, because the VR output voltage is lower, its accuracy becomes critical, also. The inductor current ripple for a buck converter is expressed:

\[ \Delta i_L = \frac{1}{f_s} \cdot \frac{(1 - D) \cdot v_{out}}{2 \cdot L_{out}} \quad (1.1) \]

\( i_L \): inductor current, \( f_s \): switching frequency, \( D \): duty cycle, \( v_{out} \): output voltage and \( L_{out} \): load inductance.

And the output voltage ripple for a buck converter is expressed:

\[ \Delta v_{out} = \frac{1}{f_s} \cdot \frac{\Delta i_L}{8 \cdot C_{out}} \quad (1.2) \]

\( C_{out} \): output capacitance.

Combining Equ.1.1 and Equ.1.2, we obtain:

\[ \Delta v_{out} = \frac{1}{f_s^2} \cdot \frac{(1 - D) \cdot v_{out}}{16 \cdot L_{out} \cdot C_{out}} \quad (1.3) \]

As it is shown in Equ.1.3, smaller output voltage ripple (i.e. accurate output voltage) requires large inductances, capacitances values and large consumed area. However,
Figure 1.2: Power MOSFET application maps for (a) $V_{DSS}$ and $I_D$ (b) $L_{out}$ and $f_s$ [2] [3]
if the switching switch ($f_s$) is increased, not only small passive components but also the high output voltage accuracy can be achieved.

In today’s industry, most high current converters are designed based on multi-channel [19] or SIP (System In a Package) technology [20]. However, the former asks not only large areas but also complicated circuit design due to the increased number of transistors and controllers. Though the latter does not suffer from these problems, it has drawbacks compared to SOC(System On a Chip) design [21]. SIP and SOC approaches shown in Fig.1.4 provide different advantages for different end-market applications [5], [6]. SIP allows for relatively easy hetero-integration of power devices, analog and digital devices, with possible cost and performance benefits. In other words, it has short development TAT(Turn Around Time), low cost for NRE(Non Recurring Engineering), and low potential of design failure because of relatively easy design between well-known chips. However, proper system partitioning at the design stage is the key to obtaining the maximum value from SIP. In short, its performances are generally poorer than SOC’s ones. Meanwhile, SOC provides the lowest manufacturing cost, high integration with advanced process technology and high performance including low power consumption and high-speed operation, but design costs are often higher and time-to-market is generally slower. However, if the SOC design is

![Figure 1.3: VRM Requirement Trends][3] [4]
accomplished based on the previous existing process technology, these problems can be avoided. And our novel buck-converter is designed based on it and does not suffer from the potential matters. Because all types of transistors are fabricated through a process in SOC design, different function blocks in a converter do not need to be connected externally through additional wires and bonds. In addition, SOC technology reduces parasite LC components which can cause considerable transient effects resulting in electromagnetic interference (EMI) problems and increases the high frequency performance reliability. Owing to the higher operating frequency, small passive components, chip area and high accurate output voltage can be achieved [22]. Besides, market cost power thanks to the single batch fabrication process and lower cost are fortified and the slow growth rate of PIC (Power Integrated Circuit) can be boosted up comparable to VLSI (Very Large Signal Integrated circuit) eventually with SOC design [23].
Table 1.1: State of art high current and low voltage synchronous buck converter comparisons

<table>
<thead>
<tr>
<th>Company</th>
<th>Breakdown Voltage(V)</th>
<th>MOSFET Structure</th>
<th>Integration method</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thoshiba</td>
<td>30</td>
<td>UMOS</td>
<td>System In a Package (SIP)</td>
<td>2008</td>
</tr>
<tr>
<td>IR</td>
<td>33</td>
<td>UMOS</td>
<td>System In a Package (SIP)</td>
<td>2005</td>
</tr>
<tr>
<td>Intersil</td>
<td>35</td>
<td>Highdensity UMOS</td>
<td>System In a Package (SIP)</td>
<td>2001</td>
</tr>
<tr>
<td>Vishay</td>
<td>35</td>
<td>WMOS</td>
<td>System In a Package (SIP)</td>
<td>2005</td>
</tr>
<tr>
<td>Philips</td>
<td>27</td>
<td>Ultra narrow UMOS</td>
<td>System In a Package (SIP)</td>
<td>2002</td>
</tr>
<tr>
<td>Renesas</td>
<td>30</td>
<td>UMOS</td>
<td>System In a Package (SIP)</td>
<td>2005</td>
</tr>
<tr>
<td>Maxim</td>
<td>30</td>
<td>-</td>
<td>System In a Package (SIP)</td>
<td>2008</td>
</tr>
<tr>
<td>MPS</td>
<td>30</td>
<td>-</td>
<td>System On a Chip (SOC)</td>
<td>2008</td>
</tr>
</tbody>
</table>

### 1.2 The SOC high current power converter challenges and proposed solutions

The current literature reviews about the state of art high current and low voltage synchronous buck converter of power semiconductor industries are summarized in the Table 1.1 which is explained in details in the chapter 2 [20], [21], [5], [6], [24], [25], [26], [27], [28].

As it is mentioned above, most of companies choose SIP technology as a high current handling capability power converter. Though the MPS(Monolithic Power System : www.monolithicpower.com) provides SOC solutions, its maximum handling current is limited to 6(A) so far.

It should be noted that UMOS(U-shape MOS) which is a vertical device MOSFET
Table 1.2: Summary of Advantages and Disadvantages of Power Devices structures

<table>
<thead>
<tr>
<th></th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral</td>
<td>Easy to integration</td>
<td>Metal de-biasing</td>
</tr>
<tr>
<td></td>
<td>No Epitaxial Layer</td>
<td>Low current capability</td>
</tr>
<tr>
<td>Power</td>
<td>Low fabrication cost</td>
<td>Complicated metal layout</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Short gate-drain overlap and small $C_{gd}$</td>
<td>Lateral drift region and large area consumption</td>
</tr>
<tr>
<td></td>
<td>Low metal de-biasing</td>
<td>Hard to integration</td>
</tr>
<tr>
<td>Vertical</td>
<td>High current capability</td>
<td>Thick Epitaxial Layer</td>
</tr>
<tr>
<td>Power</td>
<td>No fine metal lithography</td>
<td>High fabrication Cost</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Vertical drift region and small area consumption</td>
<td>Long gate-drain overlap and large $C_{gd}$</td>
</tr>
</tbody>
</table>

structure is selected for most SIP design in Table.1.1. In other words, there are several reasons related to the power device structures why it is hard to achieve SOC design and high-operating current capability at the same time [29].

The major differences between Lateral devices and Vertical devices are summarized in Table. 1.2.

While LMOS(Lateral power MOSFET structure) shown in Fig.1.7 and Fig.1.8 can be integrated with other types of devices because of its lateral current flowing direction and shared substrate, it can not handle the high current because of the small drain and source metal areas. Because drain and source contacts are put on the same top substrate surface, inter-digit fingers shape metal layout is general shown in Fig.1.5 [7]. And each contact metal area should be reduced not only because of another metal area itself but also because of the physical alignment and tolerance considerations decided by the fabrication technology, design-rule and undesirable cross-talks. If the large current is flowing through each small
width metal, metal-de-biasing effects become severe due to the high metal resistance and
electro-migration failure damages the device [30]. In addition, the device on-resistance and
total power dissipation can be increased and the maximum handling current related to SOA (Safe
Operating Area) is decreased. In the industry, very thick copper is usually used as the top
metal to reduce the resistance shown in Fig.1.6 (a) [8] but it asks special deposit and etch
processes at an expense of higher cost [8] [31]. Another popular way is to use the multi-layer
metals shown in Fig.1.6 (b) [9] but it increases the process complexity, cost, and parasitic
capacitances.

On the other hands, VMOS (Vertical power MOSFET structure) shown in Fig.1.9
and Fig.1.10 can handle higher current because its drain and source metals are usually put
on the backside and frontside of the substrate separately. Therefore, each metal can cover
large area and high current can flow through it without suffering from the metal-debiasing
and electro-migration failure problems. However, it is not easy to integrate VMOS with
other types of devices because its entire substrate is the drain. And the power converter
including power switches and analog / digital circuits can not be fabricated on the same
substrate as a SOC solution with VMOS.
Figure 1.6: The popular ways for high current handling capability devices in the current industry (a) Thick copper layer on top of power MOSFETs [8] (b) Multi-layer metals of lateral power MOSFETs [9]

Figure 1.7: The LDMOSFET (Lateral Diffused MOSFET) structure
Figure 1.8: The LRESURF (Lateral REDUCED SURFACE) MOSFET structure

Figure 1.9: The VDMOSFET (Vertical Diffused MOSFET) structure
Therefore, many companies choose the vertical MOSFET structure, especially UMOS, as a high current handling power switch and connect it with drivers and controllers externally as a SIP at an expense of lower performances such as high power consumption and low-speed operation compared to the SOC [25] [32].

Because of the reasons above, no fully integrated vertical-type, high-current handling power converter is reported, yet. In this dissertation, novel ideas to achieve the goal above will be proposed which cover novel and high performance power switch and analog/digital devices, monolithic converter design challenges / solutions and fabrication processes.

The novel monolithic buck-converter brings obvious benefits below:

- Reduced metal de-biasing effect due to reduced number of external nodes
- High current handling capability due to large metal areas without electro-migration failure
- Integration convenience of power switches and other types of driver and controller
devices

- No fine metal lithography and much simplified and small area consumption layout
due to the reduced numbers of contacts and no drain/source inter-digit metal finger
- Smaller capacitance structure and metal cross-talk
- Integrated Power MOS, analog and digital CMOS and BJT's on the same wafer
- **SOC + High current handling Design**

Eventually, proposed devices would combine many advantages of both VMOS/LMOS
and a SOC-High current handling power convert has been achieved for the first time.
Chapter 2

Fundamentals and Challenges of Power MOSFETs and a Buck Converter

2.1 The Power MOSFET

The power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is widely used device in low and middle range power applications. And there are several reasons it is selected as a primary switch in lots of areas. First, it is a unipolar device. Bipolar devices such as BJT (Bipolar Junction Transistor), Thyristor, GTO (Gate Turn-Off transistor) or IGBT (Insulated Gate Bipolar Transistor) operation needs both types of electrons and holes flowing for their forward conduction. This would increase the switching time and losses and degrade the operation speed, for example, due to the extra switching delay of storage and recombination tail time of minority carriers during turn-off. The unipolar MOSFET can be turned on and off very fast by only applying the appropriate gate voltage and its switching speed is orders of magnitude faster than for bipolar devices [29]. Second, it is a voltage controlled device. Thanks to the matured silicon dioxide technology which shows almost perfect matching to silicon properties, the static gate current is very low. This causes its low complexity gate driver design as well as high input impedance. Some of bipolar-type devices need current driver circuits which ask more supplement peripheral circuits and the entire driver circuits become complex and expensive. And the gain which is
especially important for power amplifiers becomes poor for the current controlled devices. Simple inverter types of chain drivers are enough for most power MOSFET applications [29]. Third, it has excellent SOA (Safe Operation Area) property. At the high current and the high voltage operation condition, SOA is limited by either a thermal runaway or a second break-down. Some of bipolar devices show poor SOA property due to the forward biased or reverse biased second breakdown in an inductive load power circuit. Though, MOSFET still has the bipolar second-breakdown or the MOS second-breakdown phenomena, its SOA is larger than Bipolar device’s one [29]. Fourth, its thermal reliability is better. In many applications, large width devices are usually laid out in parallel. Because bipolar devices’ forward voltage drops have negative temperature coefficients, it is hard to put them in parallel. As the temperature is increased, the forward voltage drop of a specific device may be reduced when they are put in parallel. And the current for the device is increased due to the reduced forward voltage drop and the temperature is increased further. Eventually, thermal-runaway may happen due to the positive feedback. However, MOSFET’s forward voltage drop has a positive temperature coefficient. As the temperature is increased, the forward voltage drop is increased and the current for the device is reduced. In other words, paralleled MOSFETs are willing to share the current. And its temperature is lowered. Therefore, the thermal reliability is higher due to the negative feedback [29]. Owing to all the advantages of MOSFET properties above, it has been regarded as a first candidate for high frequency power converter applications.

Two major types of Power MOSFETs are introduced in details at the following sections. And these will guide the expected novel device and process development directions.

2.1.1 A Vertical Power MOSFET

Typical vertical power MOSFET structures are shown in Fig.1.9 and Fig.1.10. The drain and source contacts are located on the different side of a wafer for vertical power MOSFETs. Fig.1.9 is called as VDMOSFET which names after the vertical double-diffusion processes. Its channel is formed by double lateral diffusion difference between p-base and source dopant during the annealing process. The double-diffusion process has unique channel process property for the channel length of the device is not decided by a lithography technology but lateral diffusion differences. In other words, the minimum feature size decided by the lithography facilities is not small, the small channel length can be
achieved. The brief VDMOSFET fabrication process is shown in Fig.2.1.

In the forward conduction mode, its specific on-resistance ($R_{onsp}$) which is one of the most important parameters of the POWER devices is comprised of several factors of Source Contact Resistance ($R_{cs}$), Source Resistance ($R_s$), Channel Resistance ($R_{ch}$), Accumulation Resistance ($R_a$), JFET Resistance ($R_j$), Drift Resistance ($R_d$), Substrate Resistance ($R_{sub}$) and Drain Contact Resistance ($R_{cd}$). When the device is optimized, there is a lowest $R_{onsp}$ point with a cell-pitch variable. In other words, the cell pitch should be reduced to achieve the higher cell density but the JFET resistance caused by the P-base regions becomes larger. If the extra n-type dopant is implanted into the JFET region, low $R_{onsp}$ as well as the higher cell density can be achieved.

Fig.1.10 is called as a UMOSFET which names after from the U-shape of the Gate groove. The brief UMOSFET fabrication process is shown in Fig.2.2. In the forward conduction mode, the channel is formed on the sidewall of the gate trench vertically and the channel density becomes higher and its $R_{onsp}$ is low. Its $R_{onsp}$ is comprised of several factors similar to the one of VDMOSFET of Source Contact Resistance($R_{cs}$), Source Resistance($R_s$), Channel Resistance($R_{ch}$), Drift Resistance($R_d$), Substrate Resistance($R_{sub}$) and Drain Contact Resistance($R_{cd}$). Unlike VDMOSFET, UMOSFET does not have the accumulation and JFET resistances and its $R_{onsp}$ is reduced further in addition to its smaller cell pitch. Eventually, low $R_{onsp}$ and power consumptions can be achieved with UMOSFET switches.

For both types vertical MOSFETs above, in the voltage blocking mode when higher voltage is applied to the drain than the source, p-base and n' drift junctions sustain the high voltage through the vertical depletion area. The breakdown-voltage of these devices can be increased as the n' drift region doping concentration is reduced and/or its thickness is increased. However, there is a trade-off between higher blocking ability and the increased specific resistance. Typically, the maximum power dissipation is decided by the junction temperature and the thermal impedance of the device system including packages. For normal package of power devices, around 100(W/cm²) range is the maximum allowable power dissipation. If higher operating voltage which exceeds the power ability of MOSFETs is required, other types of devices such as IGBT, GTO, thyristor and so on. should be considered at the expense of other properties. Or the super-junction MOSFETs can be used at the expense of higher cost [33].
Figure 2.1: The brief VDMOS Fabrication Process including required masks.
Figure 2.2: The brief UMOS Fabrication Process including required masks.
The vertical power MOSFET has several advantages over the lateral one. First, the metal de-biasing effect is small. The metal de-biasing effect is a serious problem because it is related not only to power losses but also to the device current handling capability. If the current which is flowing through the metal is large but its area is small, the voltage drop across the metal exists and severe de-biasing effects happen. At the same time, it makes the current density and power dissipation increased and thermal runaway and/or physical electro-migration failures happen, eventually. Though there are several ways to relieve these problems such as the substitution of the high sheet resistance metal with the low sheet resistance material like copper or thick top metal deposition or multi-thin metal depositions, all of these techniques increase the process complexities and cost and lower the device operation reliability including inter-connections [7]. Due to its large drain and source metal areas, vertical power MOSFET does not suffer from the severe metal de-biasing effect. Second, it has the high current handling capability. As the technology is progressed, microprocessors, graphic and memory cards ask more than 15(A) operating current. VRM(Voltage Regulator Module) which is comprised of main power switches and peripheral controllers should satisfy this specification. The vertical power MOSFET can handle such high current as a discrete device. Third, it consumes relatively small silicon area because of its vertical directional drift region and channel. No matter how the power converter is integrated monolithically, co-packaged or discrete, consumed silicon area is directly related to the cost. A UMOSFET shown in Fig.1.10 consumes small area and the fabrication cost is reduced. Fourth, less complicated layout technique is required. As higher performances and safety criteria are required, more and more circuit blocks such as over voltage and current protection, dead time controller, sophisticated gate driver should be put together. For the power converter, the layout location of the active and passive components affect the performances of the circuits directly. And the complex layout can cause reliability problems and increase the time to market. The vertical power MOSFET has a straight-forward layout structure for the top layout of the device is relatively simple.

Meanwhile, the vertical power MOSFET has several disadvantages over the lateral one also. First, it is hard to integrate the vertical MOSFET with other devices. Because the whole substrate of the vertical MOSFET is used as a drain terminal to where high voltage is applied. When many types of devices are integrated together, there are several issues which will be discussed in details in the chapter 6. Especially, the operating of one
device should not affect others and very careful design is essential for device-integrations. In this point, the vertical power MOSFET is not preferred and no integrated vertical type of power converter is reported, yet. Second, its gate to drain capacitance ($C_{gd}$) is large. As shown in Fig.1.9 and Fig.1.10, there are long overlap between gate and $n^-$ drain area and it increases its overlap capacitance. Thick silicon dioxide under the gate can be a possible solution at the cost of complicated processes and cost. And the vertical power MOSFET structure is not usually selected for the high switching applications like high frequency DC-DC converters. Third, epitaxial layer growth is needed whose function is the low doped drain area as a voltage sustaining region for power devices. Due to the highly doped substrate to reduce its resistance, epitaxial growth is the easiest way to implement low doping area on top of the highly doped substrate. Not only is the epitaxial growth cost expensive but also there is only limited number of manufactures which can do this process owing to the highly controlled technology. Though this growth technology is matured, it still increases the total power devices cost beyond the VLSI devices’ one.

### 2.1.2 A Lateral Power MOSFET

Typical lateral power MOSFET structures are shown in Fig.1.7 and Fig.1.8. The drain and source contacts are located on the same side of a wafer for lateral power MOSFETs. Fig.1.7 is called as LDMOSFET which names after the lateral double-diffusion processes similar to the previous VDMOSFET. Unlike the vertical one, this has low doping $p^-$ substrate and the drift area can be formed by ion-implantation and annealing easily instead of the expensive epitaxial growth, though the later is still valid for the lateral one, also. The brief fabrication process is shown in Fig.2.3. In the forward conduction mode, its specific on-resistance($R_{onsp}$) is comprised of several factors of Source Contact Resistance($R_{cs}$), Source Resistance($R_s$), Channel Resistance($R_{ch}$), Drift Resistance($R_d$), Drain Resistance($R_d$) and Drain Contact Resistance($R_{cd}$).

Fig.1.8 is another type of the Lateral RESURF DMOSFET whose structures is similar to the LDMOSFET. Unlike LDMOSFET, this has shallow $n^-$ drift area which can be formed by the ion-implantation without asking high thermal budget. Because the p-base, p-epitaxial layer(optional) and p-substrate have the same types of dopant, some of these processes can be skipped as long as other properties such as its threshold voltage, leakage current, and breakdown voltage are in specifications. The brief fabrication pro-
Figure 2.3: The brief LDMOS Fabrication Process including required masks.
cess is shown in Fig.2.4. In the forward conduction mode, its specific on-resistance ($R_{onsp}$) is comprised of several factors of Source Contact Resistance ($R_{cs}$), Source Resistance ($R_s$), Channel Resistance ($R_{ch}$), Drift Resistance ($R_d$), Drain Resistance ($R_d$) and Drain Contact Resistance ($R_{cd}$).

For both lateral MOSFETs above, in the voltage blocking mode when higher voltage is applied to the drain than the source, p-base and n– drift junctions sustain the high voltage through the lateral depletion area. The breakdown-voltage of these devices can be increased as the n– drift region doping concentration is reduced and/or its length is increased. However, there is a trade-off between higher blocking ability and the increased specific resistance. In these structures, the high voltage is sustained by the well-known RESURF effect [34]. This effect makes the on-resistance smaller at the same break-down voltage and causes smaller power dissipation.

The lateral power MOSFET has several advantages over the vertical one. First, devices integration is easy. Because the common substrate is not used as a specific node unlike the vertical one, all integrated devices can be built on the same substrate. In most applications, the p-substrate and n junction is reverse-biased and the minority carriers are seldom generated. Therefore, the possibility of the mal-function of a device which is caused by the operation of another type of device is low and the reliability of the entire circuit is improved. Second, its gate to drain capacitance ($C_{gd}$) is small. Unlike the long overlap between gate and n– drain area shown in Fig.1.9 and 1.10, it has only small overlap area. And its small capacitance can be achieved without a complicated process like thick silicon dioxide under the gate edge. Therefore, the lateral power MOSFET is widely used for high frequency applications. Third, expensive epitaxial layer growth can be substituted by the ion-implantation. The low doped drain area is required as a voltage sustaining region as mentioned above. Due to the low doped substrate, the drain area can be implemented by the ion-implantation instead of the expensive epitaxial growth. The relatively deep n– in Fig.1.7 needs not only the ion-implantation but also the high-temperature annealing. The latter can increase the process thermal budget. Therefore, this process should be done at the early stage of the entire processes not to cause thermal diffusions of other dopants much. On the other hands, n– in Fig.1.8 does not need the high thermal annealing thanks to its shallow depth. Therefore, this device structure is preferred for relatively low voltage operating conditions.
Figure 2.4: The brief LRESURF-DMOS Fabrication Process including required masks.
Meanwhile, the lateral power MOSFET has several disadvantages over the vertical one, also. First, its metal de-biasing effect is severe. Because the drain and source are located on the same surface of a wafer, each metal area should be reduced. And the usual multi-finger metal layout which is discusses below makes this worse. Second, its current handling capability is poor. As it is mentioned above, most of VRMs for the next generation ask the high operating current for its high system performance. This poor current handling capability is a major problem of a monolithic power integrated circuit design with the lateral power MOSFETs. Third, it consumes relatively large silicon area. Because the high voltage is sustained by the lateral low doped drain region, the cell pitch of a lateral MOSFET should be wider as the required breakdown voltage is increased. And the inter-digitized layout is another factor to increase the area discussed below. Fourth, careful layout technique is required. For instance, folded layout structure is widely used when the long MOSFET width is needed for its capacitances and gate resistances can be reduced [35]. In this structure, drain and source should be layouted in the inter-digit finger shape. It increases not only the complexity of the layout but also the consumed silicon area because there is minimum required gap between metals to minimize coupling effects and to avoid the process misalignment. As a number of integrated circuit blocks are increased, metal connections layout becomes critical and it affects the performance and reliability a lot.

Either type of vertical or lateral device has its own trade-off as explained so far. The choice of a power electronics designer depends on the application of the device. However, mixed advantages from both types are very attractive in some applications. For switch mode power converter, high current and fast frequency VRM is required especially for portable devices. Therefore, new structure and processes should be investigated for this special requirement. In next chapters, these are discussed in details and novel devices and their fabrication processes are proposed.

### 2.2 A Buck Converter

Power Electronics is a field of electric power processing with electric devices. It incorporates a diverse set of research area such as analog circuits, electronic devices, control systems, power systems, magnetics, electric machines and numerical simulation [22]. And power convert is a key element. As the heat problems become worse and worse, efficiency
which has not been the primary concern in conventional signal processing applications has become one of the most important factors in power converter design. Among three main types of converters of Linear Regulator, Capacitor Charge Pump and Switching Regulator, switching regulator shows the highest efficiency. While the linear regulator has poor efficiency for high drop voltage and the capacitor charge pump can not maintain high efficiency for a wide range of ratios of input to output voltages, switching regulator shows stable high efficiency. In a current single-stage power architecture for laptop, most of components such as main power stage, I/O power stage, CPU, graphic cards and memory cards require voltage drop from the main voltage bus [13]. Therefore, a buck converter which converters its high input voltage to the low output voltage is selected and studied below in details.

2.2.1 A Topology and Fundamental operations

The simple form of a buck regulator is shown in Fig.2.5. The main power stage is comprised of several components of power device switches (sw1, sw2), capacitor(C) and inductor(L). In the typical controller, voltage and current sensor, reference, compensator, pulse-width modulator, gate-driver and protection circuits are included. And it is generally hard to integrate the inductor due to its large size but a switching converter and a controller are usually integrated together in a power integrated circuit.
Figure 2.6: A buck regulator for sw1 on ans sw2 off

At this section, only the main power stage operation is discussed to concentrate on the basic functions and challenges of a buck converter. The controller design can be found in details in the book of [22].

The goal of a buck converter is to converter voltage without spending much power. Two switches of power devices in Fig.2.5 (sw1,sw2) turns on alternatively. And the output filter comprised of a inductor and a capacitor filters out $V_s$. Finally, the reduced stable output voltage is acquired at the output stage and its value depends on the duty(D). The fundamentals of a buck converter operations are explained below.

- For sw1 turns on and sw turns off, Fig.2.6 is an equivalent buck converter circuit. In this circuit, inductor voltage is

$$v_L(t) = V_{in} - v_o(t)$$

With small ripple approximation,

$$v_L(t) = V_{in} - V_o \quad (2.1)$$

With well known inductor voltage and current equation below and Equ.2.1,

$$v_L(t) = L \frac{di_L(t)}{dt} \quad (2.2)$$

$$v_L(t) = L \frac{di_L(t)}{dt} = V_{in} - V_o$$

$$\frac{di_L(t)}{dt} = \frac{V_{in} - V_o}{L} \quad (2.3)$$
Figure 2.7: A buck regulator for sw1 off ans sw2 on

- For sw1 turns off and sw2 turns on, Fig.2.7 is an equivalent buck converter circuit. In this circuit, inductor voltage is

\[ v_L(t) = -v_o(t) \]

With small ripple approximation,

\[ v_L(t) = -V_o \] (2.4)

With Equ.2.2 and Equ.2.4,

\[ v_L(t) = L \frac{di_L(t)}{dt} = -V_o \]

\[ \frac{di_L(t)}{dt} = -\frac{V_o}{L} \] (2.5)

From Equ.2.1, Equ.2.4 and Equ.2.3, Equ.2.5, inductor voltage and current waveforms for one switching period\( (T_s) \) are drawn in Fig.2.8 each. Based on these waveforms, input and output voltage equation and inductor ripple voltage equation can be found.

If Equ.2.2 is integrated over one switching period,

\[ i_L(T_s) - i_L(0) = \frac{1}{L} \int_0^{T_s} v_L(t) dt \] (2.6)

Because the net change in inductor current is zero in a steady state condition, Equ.2.6 becomes,

\[ 0 = \frac{1}{L} \int_0^{T_s} v_L(t) dt \] (2.7)
Figure 2.8: Inductor Voltage and Current for one switching period
If the frequency is multiplied to the right side of Equ.2.7, it becomes the average voltage. This means that the average inductor voltage is zero in a steady state condition. And this principle is called as *volt-second balance*.

From Fig.2.8, average inductor voltage is,

\[ <v_L> = D(V_{in} - V_o) + D'(-V_o) = 0 \] (2.8)

Therefore, the equation for input and output voltage is,

\[ V_o = D V_{in} \] (2.9)

From Fig.2.8, the inductor ripple equation can be found, also. The slope during DT_s period should be the same as change in the inductor current over length of subinterval,

\[ \Delta i_L = \left( \frac{V_{in} - V_o}{2L} \right) (DT_s) \] (2.10)

\[ L = \left( \frac{V_{in} - V_o}{2\Delta i_L} \right) (DT_s) \] (2.11)

As the inductance is increased, the inductor ripple becomes smaller, also.

In a similar way above, the *capacitor charge balance* principle which is the average capacitor current is zero in a steady state condition. And the capacitor ripple equation is,

\[ \Delta v_o = \left( \frac{\Delta i_L}{8C} \right) T_s \]

\[ C = \left( \frac{\Delta i_L}{8\Delta v_o} \right) T_s \] (2.12)

As the capacitance is increased, the capacitor ripple becomes smaller.

### 2.2.2 Power Losses

The power loss is one of the most important parameters in a power converter design because it decides the power efficiency and the reliability. If the exact power losses can be expected and calculated, a very high efficiency power converter can be achieved ideally. Unfortunately, it is impossible to expect all losses exactly for these are combinations of many complicated factors. However, theoretically, its loss can be breakdowned into several expected elements discussed in the following section. And the real power dissipation is not so much different from this.
Non-synchronous buck converter losses

Non-synchronous buck converter is shown in Fig.2.9. The sw1 and sw2 in Fig.2.5 is substituted by power MOSFET(M) and Diode(D) each. Unlike the synchronous buck converter, only MOSFET is controlled by the controller circuit and the diode status is decided by the status of the MOSFET passively.

Power losses for non-synchronous buck regulator are comprised of several factors below:

- MOSFET Conduction loss
- Diode Conduction loss
- Turn on and Turn off Switching loss
- Diode Reverse Recovery loss
- Gate Driver loss
- Inductor ESR(Equivalent Series Resistance) loss
- Capacitor ESR loss
- Controller loss

Fig.2.10 shows the inductor, MOSFET and diode current waveforms for one duty cycle.

**MOSFET Conduction loss**: MOSFET(M) in Fig.2.9 turns on during DT_s shown in Fig.2.10 and RMS(Root Mean Square) current can be calculated based on the
Figure 2.10: Inductor, MOSFET and Diode Current waveforms
I_M(t) waveform.

\[ I_{MOSrms} = \sqrt{D I_L} \sqrt{1 + \frac{\Delta i_L^2}{3 I_L^2}} \]  \hspace{1cm} (2.13)

And the MOSFET conduction loss is

\[ P_{MOSCon} = I_{MOSrms}^2 R_{MOSon} \]
\[ = DI_L^2 \left(1 + \frac{\Delta i_L^2}{3 I_L^2}\right) R_{MOSon} \]  \hspace{1cm} (2.14)

Substituting Equ.2.10 into \( \Delta i_L \) of Equ.2.14,

\[ P_{MOSCon} = DI_L^2 \left\{ 1 + \left(\frac{V_{in} - V_o}{2L}\right)^2 \left(\frac{D T_s}{I_L}\right)^2 \right\} R_{MOSon} \]
\[ = DI_L^2 \left[ 1 + \frac{1}{3} \left(\frac{V_{in} - V_o}{2L}\right) \left(\frac{D T_s}{I_L}\right)^2 \right] R_{MOSon} \]  \hspace{1cm} (2.15)

**Diode Conduction loss:** Diode(D) in Fig.2.9 turns on during D’T_s shown in Fig.2.10 and RMS current can be calculated based on the I_D(t) waveform. And the diode resistance power loss can be calculated in a similar way above.

\[ P_{DiodeR} = D'I_L^2 \left\{ 1 + \left(\frac{V_o - V_{a}}{2L}\right)^2 \left(\frac{D T_s}{I_L}\right)^2 \right\} R_{DiodeR} \]
\[ = D'I_L^2 \left[ 1 + \frac{1}{3} \left(\frac{V_{in} - V_o}{2L}\right) \left(\frac{D T_s}{I_L}\right)^2 \right] R_{DiodeR} \]  \hspace{1cm} (2.16)

In addition to the power loss of Equ.2.16, diode turns on voltage loss should be considered.

\[ P_{DiodeOn} = I_{av} V_{on} \]
\[ = D'I_L V_{on} \]  \hspace{1cm} (2.17)

From Equ.2.16 and Equ.2.17,

\[ P_{DiodeCon} = D'I_L V_{on} + D'I_L^2 \left[ 1 + \frac{1}{3} \left(\frac{V_{in} - V_o}{2L}\right) \left(\frac{D T_s}{I_L}\right)^2 \right] R_{DiodeR} \]  \hspace{1cm} (2.18)

**Turn on and Turn off Switching loss:** Practically, Power devices can not be turn-on and off abruptly but have delay time which causes switching losses. Fig.2.11 shows
simplified turn-on(a) and off(b) losses for the control(High-Side) power MOSFET. For the drain source voltage, the solid line represents the non-synchronous $v_{ds}(t)$. As it is well known, the constant $V_g$ during $t_2 \sim t_3$ (or $t_1' \sim t_2'$) time interval is caused by the Miller Effect Capacitance ($C_{gd}$) which contributes the switching power loss mainly. Therefore, much efforts are spent to make this capacitance small and switching losses for high-frequency application.

The turn on power loss is expressed roughly,

$$P_{MOS\text{swon}} = \frac{(t_3 - t_1)(V_{in} + V_{don})(I_L - \Delta i_L)}{2} f$$  \hspace{1cm} (2.19)$$

In a usual power MOSFET datasheet, charge data for gate turn on and off is given instead of time. And the average driving current from the gate driver during $t_1 - t_3$ is expressed,

$$I_{Gav} = \frac{V_G - V_{GP}}{R_{\text{driveron}}}$$  \hspace{1cm} (2.20)$$

And based on the current definition,

$$t_2 - t_1 = \frac{Q_{GS} - Q_{th}}{I_{Gav}}$$  \hspace{1cm} (2.21)$$

$$t_3 - t_2 = \frac{Q_{GD}}{I_{Gav}}$$  \hspace{1cm} (2.22)$$

Adding Equ.2.21 and Equ.2.22,

$$t_3 - t_1 = \frac{Q_{GD} + Q_{GS} - Q_{th}}{I_{Gav}}$$  \hspace{1cm} (2.23)$$

Substituting Equ.2.23 into Equ.2.20 and Equ.2.10 and Equ.2.20 into Equ.2.19,

$$P_{MOS\text{swon}} = \frac{R_{\text{driveron}}}{2} (Q_{GD} + Q_{GS} - Q_{th}) \left( \frac{V_{in} + V_{don}}{V_{in} - V_{GP}} \right) \left\{ I_L - \left( \frac{V_{in} - V_{o}}{2L} \right) (DT_s) \right\} f$$ \hspace{1cm} (2.24)$$

In a similar way, turn off power loss is,

$$P_{MOS\text{swoff}} = \frac{R_{\text{driveroff}}}{2} (Q_{GD} + Q_{GP} - Q_{th}) \left( \frac{V_{in} + V_{don}}{V_{GP}} \right) \left\{ I_L + \left( \frac{V_{in} - V_{o}}{2L} \right) (DT_s) \right\} f$$ \hspace{1cm} (2.25)$$

**Diode Reverse Recovery loss**: Another mechanism is the loss due to the body diode reverse recovery. This is due to the fact that the HS MOSFET turns on into the body diode. The body diode takes a finite time to turn off during which time there are losses
Figure 2.11: A control MOSFET (a) turn on and (b) turn off waveforms for (non) synchronous buck converter
in the HS MOSFET. One method of estimating the losses in the diode due to this reverse recovery current is

$$P_{DIODE\_recovery} = V_{in}Q_{rr}f$$  \hspace{1cm} (2.26)

$Q_{rr}$ is reverse recovery charge which must be discharged from the diode during reverse recovery process.

**Gate Driver loss:** When the device turns on and off, gate driver itself generates the loss and it is express,

$$P_{driver} = f \int_{0}^{t_{on}} iV_G dt = fV_G \int_{0}^{t_{on}} C_G \frac{dV_G}{dt} dt$$

$$= fV_G \int_{0}^{V_G} C_G dV_G = fV_GQ_G$$  \hspace{1cm} (2.27)

**Other losses:** A controller is another power loss factor which becomes large as more accurate power stages and feedback circuits are required. And the passive devices such as input and output filters and parasitic inductors and capacitors consume power due to their ESRs. All of these should be included in loss calculations, especially for low power applications. These power losses are express,

$$P_{Inductor\_ESR} = I_{Inductor\_ESR}^2 R_{Inductor\_ESR}$$

$$= I_L^2 \left[ 1 + \frac{1}{3} \left( \frac{V_{in} - V_o}{2L} \right) \frac{DT_s}{I_L} \right]^2 R_{Inductor\_ESR}$$  \hspace{1cm} (2.28)

$$P_{Capacitor\_ESR} = I_{Capacitor\_ESR}^2 R_{Capacitor\_ESR}$$

$$= \frac{\Delta i_L^2}{3} R_{Capacitor\_ESR}$$

Substituting Equ.2.10 into $\Delta i_L$,

$$= \left\{ \left( \frac{V_{in} - V_o}{2L} \right) (DT_s) \right\}^2 R_{Capacitor\_ESR}$$  \hspace{1cm} (2.29)

$$P_{Controller} = I_{Controller} V_{in}$$  \hspace{1cm} (2.30)
From Equ.2.15, Equ.2.18,Equ.2.24,Equ.2.25 ,Equ.2.26,Equ.2.27,Equ.2.28,Equ.2.29 and Equ.2.30, total power loss ($P_{T\text{lossNONSYN}}$) for non-synchronous buck converter is summarized,

$$P_{T\text{lossNONSYN}} = P_{\text{MOSCon}} + P_{\text{DiodeCon}} + P_{\text{MOSswon}} + P_{\text{MOSswoff}} + P_{\text{DIODErecovery}} + P_{\text{driver}} + P_{\text{inductorESR}} + P_{\text{capacitorESR}} + P_{\text{Controller}}$$

(2.31)

And the efficiency is expressed below with Equ.2.31,

$$\text{Efficiency}(\eta)(\%) = \frac{P_{out}}{P_{in}} \times 100 = \frac{P_{out}}{P_{out} + P_{T\text{lossNONSYN}}} \times 100$$

(2.32)

**Synchronous buck converter losses**

A synchronous buck converter is shown in Fig.2.12. The sw1 and sw2 in Fig.2.5 is substituted by power MOSFETs of M1(Highside) and M2(Lowside) each. Unlike the non-synchronous buck converter, both MOSFETs are controlled by the controller circuit.

Power losses for synchronous buck regulator are comprised of several factors below:

- Highside MOSFET Conduction loss
- Lowside MOSFET Conduction loss
- Lowside Body Diode Conduction loss
• Diode Reverse Recovery loss
• Highside MOSFET Turn on and Turn off Switching loss
• Gate Driver loss
• Inductor ESR loss
• Capacitor ESR loss
• Controller loss

Fig.2.13 shows the inductor, highside and lowside MOSFET current and body-diode waveforms for one duty cycle.

Highside MOSFET Conduction loss: Highside MOSFET (M1) in Fig.2.12 turns on during DT_s shown in Fig.2.13. In a similar way of non-synchronous MOSFET conduction loss calculation, Highside MOSFET Conduction loss is found,

\[ P_{HSCon} = I_{HSrms}^2 R_{HSon} = DI_L^2 \left(1 + \frac{\Delta I_L^2}{3I_L^2}\right) R_{HSon} = DI_L^2 \left[1 + \frac{1}{3} \left(\frac{V_{in} - V_o}{2L} \frac{DT_s}{I_L}\right)^2\right] R_{HSon} \tag{2.33} \]

Lowside MOSFET Conduction loss: Lowside MOSFET (M2) in Fig.2.12 turns on during D’T_s shown in Fig.2.13. And the Lowside MOSFET conduction power loss can be calculated in the similar way above. While a diode has additional turns on voltage loss, MOSFET doesn’t and the conduction loss is smaller.

\[ P_{LSCon} = I_{LSrms}^2 R_{LSon} = D' I_L^2 \left(1 + \frac{\Delta I_L^2}{3I_L^2}\right) R_{LSon} = D' I_L^2 \left[1 + \frac{1}{3} \left(\frac{V_{in} - V_o}{2L} \frac{DT_s}{I_L}\right)^2\right] R_{LSon} \tag{2.34} \]

Lowside Body Diode Conduction loss: While the diode status is decided by the control MOSFET for non-synchronous converter, a control MOSFET (M1) and a synchronous MOSFET (M2) status are controlled by the controller individually. Because delay, rising, falling times exist in a real circuit, the shoot-through which causes a lot power
Figure 2.13: Inductor, Highside and Lowside MOSFET and Body-diode Current waveforms
consumptions and failure of devices can happen. To prevent this disaster, the proper turn off time for both M1 and M2 at the same time is added. And it is called as *dead-time*. During the dead-time, the body-diode of M2 flows the inductor current and causes loss. Its current waveform is shown in Fig.2.13 and power loss is calculated,

\[
P_{BDCon} = \left\{ V_{DiodeCon}(I_L + \Delta i)t_{d1} + V_{DiodeCon}(I_L - \Delta i)t_{d2} \right\}f
\]

\[
= V_{DiodeCon}I_L \frac{t_{d1} + t_{d2}}{T}
\]

\[
= (V_{on} + I_LR_{DiodeR})I_L(t_{d1} + t_{d2})f
\]

(2.35)

**Diode Reverse Recovery loss:** After the dead-time is just over, the body diode is about to block the voltage. At this time, there is a well-known reverse recovery process which causes additional power loss. Though the time is not too long, the reverse recovery current is quite high and its power loss is important especially for low power applications. And its loss is expressed,

\[
P_{RR} = V_{in}Q_{rr}f
\]

(2.36)

**Highside MOSFET Turn on and Turn off Switching loss:** The dash line in Fig.2.11 represents the synchronous \( v_{ds}(t) \). In a similar way of non-synchronous MOSFET on, off losses calculation, highside MOSFET on, off losses are found,

\[
P_{HSswon} = \frac{R_{driveron}}{2}(Q_{GD} + Q_{GP} - Q_{th})\left(\frac{V_{in} + V_{dom}}{V_{in} - V_{GP}}\right)\left\{ I_L - \left(\frac{V_{in} - V_o}{2L}\right)(DT_s) \right\}^2
\]

(2.37)

\[
P_{HSswoff} = \frac{R_{driveroff}}{2}(Q_{GD} + Q_{GP} - Q_{th})\left(\frac{V_{in} + V_{dom}}{V_{GP}}\right)\left\{ I_L + \left(\frac{V_{in} - V_o}{2L}\right)(DT_s) \right\}^2
\]

(2.38)

Lowside MOSFET usually has trivial switching losses.

**Gate Driver loss:** In a similar way of non-synchronous MOSFET gate driver loss calculation, MOSFET gate driver loss is found,

\[
P_{HSdriver} = fV_GQ_{HSG}
\]

(2.39)

\[
P_{LSdriver} = fV_GQ_{LSG}
\]

(2.40)

**Other losses:** Other losses for synchronous are the same as ones for non-synchronous.
From Equ.2.33, Equ.2.34, Equ.2.35, Equ.2.36, Equ.2.37, Equ.2.38, Equ.2.39, Equ.2.40, Equ.2.28, Equ.2.29 and Equ.2.30, total power loss ($P_{TlossSYN}$) for synchronous buck converter is summarized,

\[
P_{TlossSYN} = P_{HSCon} + P_{LSCon} + P_{BDCon} + P_{HSwn} + P_{HSwoff} + P_{HSdriver} + P_{LSdriver} + P_{InductorESR} + P_{CapacitorESR} + P_{Controller}
\]

(2.41)

And the efficiency is expressed below from Equ.2.41,

\[
Efficiency(\eta)(\%) = \frac{P_{out}}{P_{in}} \times 100 = \frac{P_{out}}{P_{out} + P_{TlossSYN}} \times 100
\]

(2.42)

The estimated power losses and efficiencies for both synchronous and nonsynchronous buck converter have been derived. And the following challenges for a buck converter design related to these are addressed, also. The efficiency is one of the main design factors when the power device and circuit are designed in the chapter 6. A nonsynchronous buck regulator usually has higher power consumption than a synchronous one due to the relatively high diode on voltage compared to the one of synchronous MOSFET. Therefore, synchronous buck converter is selected for a high efficiency converter design in this dissertation. In addition, to further reduce the power loss and improve the reliability, monolithic synchronous buck converter design is proposed, also.
Chapter 3

Smart Power Integrated Circuit (SPIC)

The demands of developing high voltage (HV) devices integration with low voltage (LV) digital and analog ones have been grown continuously [36] [37] [38] [39] [40]. That is because the Smart Power Integrated Circuit (SPIC) technology has wide range of applications such as motor controls, telecommunications, VRMs, automobiles, aircraft, medical instruments and so on. Though this technology brings obvious advantages of the compact chip size and subduing parasitic effects which degrade devices and overall circuits performances a lot [41], there are still limited number of fabrication manufactures which can proceed the SPIC because of the uniqueness of high voltage device processes.

Alternatively, considerable amounts of research have been carried out for the high voltage device integration in a well-established VLSI process to overcome the high voltage device fabrication complexity. By the high voltage VLSI integration technology, not only can the low fabrication cost and better reliability be achieved but the development time to market can be reduced [41] [42] [43].

However, some of these HV-devices ask extra masks and processes in addition to the conventional CMOS process and the total fabrication cost and the design complexity are increased [44] [45]. Though the devices which can be fabricated in the conventional CMOS process without extra processes for RF applications have been reported [46] [47], power-management application investigations are still lack and need to be studied further. For example, FOM (Figure Of Merit) which is an important specification for high-frequency
and low power consumption power electronics areas for device- and circuit- performances comparisons should be considered and evaluated for SMPS (Switch Mode Power Supply) applications. And a p-channel improved-BV MOSFET as well as an n-channel should be suggested for power converters such as buck, boost and buck-boost which are core blocks in power management applications, at the same time. Complementary control and synchronous switches are essential for fully integrated power stages with drivers and controllers on the same substrate unless extra isolations which may cause device failures exist [48].

In this chapter, prior high and low voltage devices integration research is introduced briefly. And new improved breakdown-voltage complementary devices for power converter applications are introduced considering all of fabrication process tolerances in a state-of-art 0.18μm VLSI process without any additional processes. And small on-resistances shown in Table.3.1, Table.3.2 and FOMs shown in Fig.3.6 are acquired for high-frequency applications. Furthermore, the merged-charge effect through STI is introduced and helps to increase the breakdown voltage. It should be noted that new improved BV-CMOS properties should not affect or degrade other important parameters.

At the last section of this chapter, limitations for HV power MOSFET design in a standard CMOS process are explained, also. Eventually, needs for novel vertical power MOSFETs development is introduced.

3.1 Prior High- and Low- Voltage Devices Integration Technology

There have been many previous proposed approaches for high voltage power devices and low voltage analog and digital ones integration in various research areas [45] [46] [49] [50] [51] [52] [53] [54] [55] [56] [12] [57] [58] [42]. In this section, previous research are reviewed briefly and the related issues are addressed for high and low voltage devices integration.

3.1.1 Integrated High Voltage Devices in a Low Voltage CMOS process with Additional Masks and Steps

Some of previously proposed power devices showed high performances such as the high power gain at high frequency and high power efficiency for RF power applications by
adding several masks and process steps [44] [45]. Though a high voltage device is developed in a CMOS process, there is a major drawback of increased number of additional processes and masks. For example, its higher breakdown voltage is achieved by the additional n-implantation [45] which requires not only one more mask but also several extra fabrication steps and cost. And this structure does not fully take the advantage of a CMOS process with STI explained later. Moreover, a high voltage PMOS device is not suggested, also. Another structure suggested high voltage complementary MOSFETs in a CMOS process which is desirable for integrated half-bridge synchronous buck converter applications at the expense of extra masks and processes [45]. Fully compatible power MOSFETs with existing CMOS fabrication processes without extra steps are required to reduce the market time and cost.

3.1.2 Integrated High Voltage Devices in a Low Voltage CMOS process without Additional Masks and Steps

Another research effort for PIC fabrication is to follow the pre-established VLSI CMOS process exactly. Z. Parpia developed high breakdown-voltage complementary devices in a CMOS process without any additional processes and masks [42]. However, there are still some drawbacks. First of all, n-guard doping which is used as a drift region may not be low enough in a specific process technology because of its original function and required dose. For example, if it is too low to endure high voltage, it can not prevent the unexpected parasitic device turn-on. Meanwhile if it is too high, it can not endure the drain high voltage. Second, STI instead of LOCOS used in [42] can increase the breakdown voltage further explained later. Third, while thick LOCOS causes the bird’s beak and high hill on the silicon surface, STI devices have very smooth surfaces and small silicon consumed area and increase device reliabilities much. J. Ramos suggested high voltage devices in a CMOS process without any additional processes and masks, also [46]. However, the power device structures can be improved further. There is \( n^+ \) implant in [46] on the right side of the self-aligned gate which is necessary for the low poly silicon gate resistance. This increases the consumed silicon area. And the poly over the n-well is used to create a low doping drift region by blocking the \( n^+ \) implant over all the n-well. However, this increases the cell pitch and consumes silicon area, also. The better way to avoid these problems are proposed in the following sections. In addition, no high voltage PMOS is suggested in [46].
3.2 Novel High Voltage Device Embodiment in a Standard CMOS process [1]

3.2.1 Improved Breakdown-Voltage Device Structures

The improved breakdown-voltage transistors are designed in a standard 1-Poly 6-Metal twin-well silicide 0.18μm CMOS process.

Improved Breakdown-Voltage N-type MOSFET

The brief cross-section of the n-type power MOSFET is shown in Fig.3.1.

The relatively low doped n-well is used as a drift region to sustain the drain voltage and increases the breakdown voltage. This n-well prevents not only the premature well-known gate-edge breakdown but also the reach-through which usually happens in a narrow effective gate length MOSFET structure and degrades its breakdown. Because the depletion region extends into the low-doped n-well instead of into the channel in Fig.3.1, higher voltage

---

Figure 3.1: A Cross-Section of the Improved Breakdown-Voltage NMOS(not-scaled)
Figure 3.2: A Cross-Section of the Improved Breakdown-Voltage PMOS (not-scaled)

can be applied to its drain contact without causing the reach-through problem.

And the STI next to $n^+$ drain in the n-well contributes to the high breakdown voltage, also. First, it can lengthen the effective drift region at the same silicon area. Second, it causes the merged-charge effect (charge-coupling) as long as the distance between p,n-well junction and STI distance ($d_1$ in Fig.3.1) is short enough. These will be discussed in details later.

For a conventional CMOS process, wells are ion-implanted after STI is formed. And lateral diffusion of the n-well dopant during its annealing process is necessary to form the n-well below STI in Fig.3.1. Therefore, the STI width ($d_2$) in Fig.3.1 is limited by its lateral diffusivity. Both STI width ($d_2$) and depth of 0.3$\mu$m are selected based on the design and process rules (alignment tolerances, minimum feature sizes etc.).

**Improved Breakdown-Voltage P-type MOSFET**

The brief cross-section of the p-type power MOSFET is shown in Fig.3.2. The reason the HV-PMOS structure is different from the HV-NMOS one in Fig.3.1 is that the
p-well connected to the common p-type substrate inherently can not work as a drift region without extra isolations if the similar structure is selected. For a conventional silicon CMOS process, the PMOS is usually formed in a n-well because of the preferred p-type substrate. If the p-well is used as a drain region, additional deep n-well is required to isolate this PMOS drain from the substrate but the number of masks, process steps and cost are increased. Furthermore, the high voltage can not be applied to the p-drain because the p-substrate is already connected to the ground as a common substrate without additional deep n-well structure. Therefore, the new structure which is different from the novel NMOS concept should be suggested shown in Fig.3.2.

In the proposed PMOS structure, the n-well is counter-doped by the p-well ion-implantation and the effective doping concentration is reduced to endure higher voltage. However, the high electric field at the gate edge still exists and limits the amount of the increased breakdown voltage. Therefore, the doping at the edge of a PMOS gate should be decreased without adding any additional mask and process. The low doping p-channel ion-implantation can be used for this purpose and this function is similar to a LDD (Lightly Doped Drain) concept shown in Fig.3.2. It should be paid attention that the counter-doping and modified p-channel layout should not affect the threshold voltage. This problem can be solved by adjusting the gate-drain overlap length (\(d_{ov}\) shown in Fig.3.2) easily considering the counter-doped n-well doping concentration. Eventually, there are no other severe PMOS performance degradations. And the breakdown voltage has been increased by almost twice. A potential disadvantage of this structure is caused by the conventional CMOS fabrication process sequences. Because the channel-doping should be ion-implanted before the gate is formed in a standard CMOS process, the lightly doped drain formation using channel doping is a non self-aligned process. The proper process alignment tolerance (\(d_{ov}\)) should be added to prevent the serious device malfunction caused by the drain and gate disconnection. This may increase the gate-drain capacitance (\(C_{gd}\)) and degrade FOM but its FOM is still very small among the same voltage level devices shown in Fig.3.6.
3.2.2 Devices Performances

NMOS Performances for SMPS Applications

Possible layout variables to control the NMOS breakdown voltage shown in Fig.3.1 are d1 and d2. It is found that the breakdown voltage is a strong function of d1 shown in Fig.3.3 but not of d2.

As d1 is reduced, the breakdown voltage is increased and this can be explained by the merged-charge effect. As d1 is reduced, the depletion areas next to STI in the n-well which are comprised of one from the left due to the positive charges of p,n-well junction, another from the gate, and the other from the right through the STI [59] [60] are merged together. Therefore, the vertical depletion depth from the gate oxide becomes larger. In other words, the positive charges next to STI in the n-well is increased due to the merged-charge effect at the same voltage shown in Fig.3.4. The electric field is more uniformly distributed as d1 is reduced and maximum electric field is relieved.

Therefore, not only does the STI in the n-well lengthen the drift region at the same silicon area, but it invokes the merged-charge effect of increased positive charges in

Figure 3.3: NMOS Breakdown Voltage as a function of d1
the n-well and increases the breakdown voltage. In addition, the on-resistance and FOM are reduced at the same breakdown voltage. However, due to the current fabrication process tolerance limits, d1 can not become too small. 0.4\( \mu \text{m} \) is selected considering 0.18\( \mu \text{m} \) CMOS process and the achieved maximum breakdown voltage is 22.6V which is 3.5-times larger than 6.6V of low voltage VLSI NMOS shown in Fig.3.5. It should be noted that if the right edge of the gate is put somewhere between p,n-well junction and STI, the breakdown improvement is lower (11.6V) [47] due to the well-known gate edge electric field crowding effects and this is shown as a blue dot line (STI Offset: the distance between edge of the gate and STI) in Fig.3.5. By putting its edge on the thick oxide (STI), this can be prevented. Though this may increase the \( C_{gd} \) a little bit, its FOM is still lower than other devices shown in Fig.3.6.

Therefore, NMOS breakdown voltage is improved 3.5-times (22.6V) and on-resistance (10m\( \Omega \cdot \text{mm}^2 \)) and FOM (11m\( \Omega \cdot \text{nC} \)) are small among the same voltage level devices. The results are summarized in Table.3.1 and in Fig.3.6 each.
Figure 3.5: Breakdown-Voltage Comparison among conventional, STI offset and No STI Offset NMOS

Table 3.1: Summary of Conventional LV-NMOS and Improved-BV NMOS

<table>
<thead>
<tr>
<th></th>
<th>BV (V)</th>
<th>$R_{on}$ (m$\Omega$*mm$^2$)$^{1)}$</th>
<th>$V_{th}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HVN$^{2)}$</td>
<td>22.6</td>
<td>10.0</td>
<td>0.8</td>
</tr>
<tr>
<td>LVN$^{3)}$</td>
<td>6.6</td>
<td>4.4</td>
<td>0.8</td>
</tr>
</tbody>
</table>

$^{1)}$ For $V_{gs}=3$(V), $^{2)}$ High Voltage NMOS, $^{3)}$ Low Voltage NMOS
PMOS Performances for SMPS Applications

A layout variable to control the PMOS breakdown voltage in Fig.3.2 is the low doped p' drain length (\(d_3\) or \(d_{ov}\)). It is found that the breakdown voltage is a weak function of \(d_3\) shown in Fig.3.7. Therefore, \(d_3\) should be decided by considering its threshold voltage, reach-through, gate-drain capacitance, process tolerances and consumed area. \(d_3\) of 0.3 \(\mu\)m is selected as an optimum value.

Therefore, PMOS breakdown voltage is improved 2-times (13.2V) and on-resistance (23.1m\(\Omega\cdot\text{mm}^2\)) and FOM (5.3m\(\Omega\cdot\text{nC}\)) are small among the same voltage level devices. The results are summarized in Table.3.2 and in Fig.3.6 each.

3.3 Monolithic Synchronous DC-DC Converter Design

New proposed PMOS and NMOS can be used as a control and a synchronous power switch each in a monolithic synchronous buck converter. Because there is no special isolation structures among different types of devices in a conventional CMOS process.
Figure 3.7: PMOS breakdown voltage as a function of p-drain length

Table 3.2: Summary of Conventional LV-PMOS and Improved-BV PMOS

<table>
<thead>
<tr>
<th></th>
<th>BV(V)</th>
<th>$R_{on}$(mΩ*mm$^2$)$^1$</th>
<th>$V_{th}$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HVP$^2$</td>
<td>13.2</td>
<td>23.1</td>
<td>-1.0</td>
</tr>
<tr>
<td>LVP$^3$</td>
<td>7.6</td>
<td>5.7</td>
<td>-0.8</td>
</tr>
</tbody>
</table>

$^1$ For $V_{gs}=3$(V),$^2$ High Voltage PMOS,$^3$ Low Voltage PMOS
except the STI and self-isolations (SI), the PMOS should be selected as a high side switch for power switches and drivers/controllers integration. And PMOS gate driver and controller circuits including voltage level-shifters, voltage clamps or the AC-coupled topology should be designed carefully because of its high gate input voltage swing and limited gate oxide breakdown voltage. A monolithic buck converter is designed based on the HV-Complementary MOSFET above as power switches with integrated LV-CMOS drivers and controllers together without adding any additional processes shown in Fig.3.8.

As the required operation frequency for power converters are faster, the performance degradations by parasitic components become critical. As shown in Fig.3.8, a monolithic solution reduces the number of package and parasitic component. Therefore, power losses and power converter function reliabilities are improved. The designed monolithic buck converter for high frequency applications has less parasites components and ISE-TCAD and Cadence-SPICE simulations show high efficiency (88%) as shown in Fig.3.9. The operating specifications are shown in the table in Fig.3.9. It is shown that the new improved breakdown voltage CMOS is proper for SMPS applications.

![Figure 3.8: Discrete vs. Monolithic Half-bridge converter](image-url)
Figure 3.9: High Frequency Monolithic synchronous Buck Converter Loss Breakdown and Efficiency

3.4 Brief Summary

The novel complementary high voltage MOSFET is designed in a state-of-art 0.18μm VLSI technology. The improved BV-NMOS achieves 22.6V breakdown voltage thanks to the merged-charge effect through STI as well as the low-doped n-well and 10mΩ·mm² specific resistance. And the improved BV-PMOS achieves 13.2 V breakdown voltage thanks to the counter-doping as well as the low doping concentration at the gate-drain edge and 23.1mΩ·mm² specific resistance. Finally, these show the lowest FOMs among the same voltage rate devices which are proper for high-frequency and low power applications. And high voltage power devices and analog / digital circuits for the high-frequency monolithic DC-DC converter have been integrated and 88% high-efficiency is achieved. Therefore, the novel improved BV-devices design has been optimized for power convert applications.
3.5 Limitations for HV Switches in a standard CMOS process and Further Requirements

Limitations for HV power MOSFETs in a standard CMOS process

As it is shown above, high voltage devices development method by only adjusting layouts is simple and attractive. However, there are still limitations. In the application point of view, DC-DC converters, VRM for Desktop PCs, notebook, network servers, work stations, cell phone and telecommunication equipments ask higher operating frequency and current as the technology is proceeded. Because the conventional CMOS process is developed only for VLSI for which all of its process parameters are optimized, the layout adjustment technology has its maximum voltage limit beyond which device breakdown voltages can not be improved further. In other words, breakdown-voltages can not be increased much without changing the processes. In addition, the existing low doping areas in the conventional CMOS process are not optimized for power devices. If these are used as high-voltage sustaining regions, the SMPS can not satisfy high performance required systems because of their unoptimized poor characteristics. Furthermore, most of the devices are lateral ones which can not flow the high current due to the metal de-biasing effect and severe heat density. And the isolation is another big concern for it is directly related to the entire circuit reliability which becomes more and more important as the chip densities are increased.

Needs for Novel vertical power MOSFETs development

Considering all of the problems above, new power devices which would satisfy the next generation high operating specifications need to be developed. At the same time, the process complexity should be minimized. The developed novel vertical power MOSFETs in this dissertation can satisfy these requirements with only one additional mask and next chapters would explain the details.
Chapter 4

Integrated Single Pole Double Throw Vertical Power Devices

4.1 Integrated Switches

Novel a control (High-Side:HS) and a synchronous (Low-Side:LS) power devices structures which combine many advantages of both vertical MOSFETs and lateral MOSFETs are shown in Fig.4.1. The details of each structure are explained in the following sections but the ways how to integrate two different vertical MOSFETs on the same substrate as the integrated SPDT switch and how to increase the current handling capability are discussed here.

In a synchronous buck-converter topology shown in Fig.4.2, the high-side switch source (S1) is connected to the low-side switch drain (D2) as a switching node (SW) which equals to $V_{in}$ during the duty cycle or ground else ideally. Because the SW node (Single Pole) is connected to $V_{in}$ or ground through HS device or LS device (Double Throw) each, these are called as SPDT switches. And the two nodes (S1 and D2) are usually connected each other externally through each pad or internally through each metal. However, the former increases the number of pads and external pins which are not desirable because of the increased parasitic components and more complicated system (PCB) level optimization requirements. And the latter makes the layout complicated and the handling current reduced. Meanwhile, as it is shown in Fig.4.1, HS top-surface source (S1) is connected to the common substrate through its own highly doped trench and LS top-surface drain (D2) is connected to the
common substrate through its own highly doped trench, also. Therefore, S1 and D2 are
connected internally through the common substrate which is the switching node.

The vertically shared switching node structure brings lots of advantages. It is
common that the source contact(S1) of high-side and the drain contact(D1) of low-side
switches in a monolithic design are located on the same top-surface. However, these two
contacts can be put on the bottom surface of the substrate instead of the shared top-surface
as a unified contact in the novel structure. In addition, in the each device design point of
view, only one type of contacts between its source and drain contact (metal) can be put on
its top-surface shown in Fig.4.1. In other words, each HS drain (D1) metal for high-side
switch and LS source (S2) metal for low-side switch can cover its most top-surface area and
each metal coverage area is increased. Besides, the shared bottom S1 and D2 metal cover
large substrate area at the same time. Therefore, high operating current can flow through
each device with much reduced metal debiasing effects owing to the large metal widths for
all contact metals without suffering from the electro-migration failures. The thick metal
like copper technology is not required to go with it. And in the fabrication and layout point
of view, no high cost fine metal lithography is required and the physical layout has been
simplified due to the reduced numbers of contacts and external nodes and no drain/source
inter-digit metal finger structure requirement. Of course, the cell pitch, consumed chip
areas and metal cross-talks are reduced at the same time. Moreover, the inherent lateral
device structure on the top surface lowers the capacitances, especially $C_{gd}$ which is one
of the most important FOM (Figure Of Merit) factors. And other analog/digital signal-
processing devices which show high performances in our design can be integrated with the
vertical power switches on the same wafer easily. Eventually, a SOC - high current handling
power devices have been proposed for the first time.

4.2 A High-side(control) and A Low-side(synchronous) Power
MOSFET

4.2.1 Optimized Structures

The HS and LS MOSFET structures in Fig.4.1 have been optimized not only for
high-current handling capabilities but also for high-performances for SMPS applications
Figure 4.1: Cross-Sections of Novel POWER MOSFETs (process-simulated with ISE-TCAD FLOOPS)
The high drain voltage is supported by the well-known optimized dose RESURF area [34]. If the RESURF doping concentration is increased, the drain resistance can be reduced but it is hard to make its area depleted and RESURF effect can not be invoked. Furthermore, because the electric field at the gate-drain edge is increased at the same time, high impact ionization rate may occur at the region and its breakdown voltage is decreased. Therefore, the dose should be optimized considering its breakdown voltage and specific on-resistance trade-off. Based on the state of art ISE-TCAD device and process simulations, $3 \cdot 10^{12} \text{cm}^{-2}$ RESURF dose is selected for $\sim 30V$ breakdown voltage devices in our design.

Each HS source and LS drain is comprised of three regions of its top surface, side-wall doped trench and common substrate. The trench which is highly doped to reduce its resistance can be implemented by the tilt-angle and multi-rotation ion-implantations technology after silicon trench etching process following insulator filling. Because it is the only process which is not involved in the conventional power device and VLSI CMOS fabrication processes in the novel BCD process, it is one of the most important structures.
and processes for the entire power converter design. Therefore, electrical characterizations as well as physical properties should be verified intensively by numerical simulations and experimentations. This will be discussed more details in the chapter 7. Because HS source contact and metal are located on the bottom substrate thanks to the trench, its drain metal can cover the most HS top surface area except island body-metal region shown in Fig. 4.9. In a similar reason, LS source metal can cover the most LS top surface area. It should be noted that though both HS and LS devices use RESURF effect to sustain their high drain voltage, there is a difference. In the HS structure in Fig. 4.1 (a), its p-body and source comprised of $n^+$ top-surface, $n^+$ trench, and $n^+$ substrate are shorted and have the same voltage. However, in the LS structure in Fig. 4.1 (b), its p-body connected to its source and drain comprised of $n^-$ RESURF, $n^+$ trench and $n^+$ substrate are not shorted. In other words, there is not only $n^-$ RESURF-pbody(pbase) junction but also $n^+$ trench-pbody(pbase) and $n^+$ substrate-pbody(pbase) junctions. Therefore $n^+$ trench and $n^+$ substrate doping concentrations can not be too high, otherwise the breakdown happens at one of these junctions. Fortunately, there are merged charge effect explained in the section 4.3 and graded junction effect and their doping concentrations can be higher.

In a sub-micron channel device, the drain and source punch-through is a serious problem especially for power devices due to their high drain voltage. However, this can be prevented by adding highly doped p-base regions shown in Fig. 4.1 which makes the depletion area extended into the drain area further instead of into the narrow channel region. Furthermore, the p-base doping concentration and its depth should be optimized for achieving not only its target threshold voltage but also better $dV/dt$ capability and safe-operating-area (SOA) by subduing the second breakdown phenomena [29]. Lastly because bipolar junction transistor(BJT)s should be integrated with the power MOSFETs without extra masks and processes, the p-base design should consider BJT performances explained in the chapter 5 at the same time.

### 4.2.2 Performances

As the required operating frequency for a power converter is increased, the gate charge as well as the specific on-resistance becomes important. And the on-resistance and the gate-charge are shown in Fig. 4.3 and Fig. 4.5 for a high-side MOSFET and Fig. 4.4 and Fig. 4.6 for a low-side MOSFET. And major properties of the novel vertical MOSFETs are
Figure 4.3: High-side switch $I_{ds}$ vs. $V_{ds}$ curves and $R_{on}$ for different gate voltages

summarized in Table 4.1. In addition these can handle high operating current as integrated vertical switches for the first time, their on-resistances ($R_{on}$) and gate-drain capacitances ($Q_{gd}$) are low compared to other reported devices at the same voltage rating shown in Fig. 4.7. Eventually these have the lowest FOM for the same reported 30V-rating power devices shown in Fig. 4.8. It should be noted that Thoshiba’s 2003 LDMOS has almost the same FOM as ours but it can not handle the high operating current.

### 4.2.3 Layout Considerations

Due to the vertical $n^+$-doped trench shown in Fig. 4.1 (a), HS body contact should be located in the 3-D direction (remote body-contact) shown in Fig. 4.9. Highly doped $p^+$ region are exposed between two discontinued trenches and the island metal connects it to the $n^+$source region and HS p-body and source are shorted together. Because this body-metal is an island which is not connected to the external pad, most of high-side MOSFET areas can be covered by the drain metal without losing much area. The high-side switch
Figure 4.4: Low-side switch $I_{ds}$ vs. $V_{ds}$ curves and $R_{on}$ for different gate voltages

Table 4.1: Major properties of Integrated Vertical Power MOSFETs

<table>
<thead>
<tr>
<th></th>
<th>BV</th>
<th>$V_{th}$</th>
<th>$R_{on}$</th>
<th>$Q_{gd}$</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side</td>
<td>33</td>
<td>2.0</td>
<td>28.4</td>
<td>0.3</td>
<td>9.8</td>
</tr>
<tr>
<td>Low-side</td>
<td>33</td>
<td>2.1</td>
<td>29.0</td>
<td>0.3</td>
<td>10.1</td>
</tr>
</tbody>
</table>
cross-sections which are cut at A-A’ and B-B’ in the HS top-view layout in Fig.4.9 (b) are shown in Fig.4.9 (a) and (c) each. As it is shown in (a), the island body metal builds the connection between source and p-body as explained above. And there is no trench exists in the specific area. (c) shows another cross-section which includes the trench structure without the island body metal. And the entire surface is covered by the drain metal. In addition, the body contact is usually not required for every cell and the island metal area becomes much smaller than the drain one.

Meanwhile, LS does not need additional body metal because its source metal covers the body area shown in Fig.4.10. However, the remote body-contact layout can be used for LS to reduce its cell-pitch and on-resistance shown in Fig.4.11. It should be noted that the periodicity of the body-contacts depends on the device/circuit reliability-requirements such as latch-up and voltage deviation due to the parasitic body resistance.

In some applications, high channel-density power MOSFETs whose on-resistances are reduced further as increasing the number of gate channel on the same area and their current-density are required. And the closed cells such as squares, offset-squares, trian-
Figure 4.6: Low-side switch $V_{gs}$ vs. $Q_g$ curves: $Q_{gs1}$ is the charge before $V_{gs}$ reaches to $V_{th}$, $Q_{gs2}$ is the gate-source capacitor charge except $Q_{gs1}$ and $Q_{gd}$ is the gate-drain capacitor charge.

Gles, hexagonals, circles and atomic lattice are popular for the purpose \cite{29}, \cite{61} instead of the linear (stripe) one. Both stripe-layout and square-layout power devices are shown and compared in Fig. 4.12. The poly-silicon gates are put in cross-shapes in the high-density (square-layout; (b) and (d)) design and the channel density has become increased. And the operating current is flowing through 4-directions in (b) and (d) shown in Fig. 4.13 instead of 2-directions in (a) and (c). Therefore, the on-resistance and FOM of each power MOSFET are reduced. However, high-density devices should be designed carefully not to reduce their breakdown voltages. Because the spherical junctions exist in the high-density cell layouts instead of the cylindrical ones in the stripe layouts shown in Fig. 4.12, their corner breakdown voltages can be reduced \cite{29}. Therefore the sharp corner should be avoided and the round corners are added shown in Fig. 4.12 (b) and (d). And the breakdown voltages for both devices are not affected by the layout much.
Figure 4.7: $Q_{gd}$ and $R_{on}$ Comparisons for 30V MOSFETs

Figure 4.8: FOM comparisons for 30V MOSFETs
Figure 4.9: Top-view and cross-sections of the high-side MOSFET including island body-metal (not-scaled): (a) The cross-section cut at A-A' in (b) (b) The top-view of HHS switch (c) The cross-section cut at B-B' in (b)
Figure 4.10: (a)Top-view and (b)cross-section of the low-side MOSFET
Figure 4.11: Top-view and cross-sections of the low-side MOSFET with the remote contact:
(a) The cross-section cut at A-A' in (b) (b) The top-view of LS switch (c) The cross-section cut at B-B' in (b)
Figure 4.12: Low- and High- density Layouts for (a),(b) HS MOSFET and (c),(d) LS MOSFET
4.3 Higher voltage-rating power devices

Though most VRs for portable systems like a laptop require less than 30(V) breakdown voltage switches considering SOA and reasonable voltage margin shown in Fig.1.1, there are still applications which ask higher voltage-rating and high current devices. As it is shown in Fig.1.2, the power switches for desktop PCs, notebook PCs, servers, and other portable devices such as cell phone and PDA require ~50(V) voltage-rating devices. Therefore, the novel vertical power MOSFETs which can endure more than 50(V) are suggested here in addition to the 30(V) ones.

4.3.1 Optimized Structures

50(V) voltage rating HS and LS MOSFETs are shown in Fig.4.14. Though most of structures are similar to the 30(V) power devices, there are several major differences below.

1. The FOX (Field OXidation) exists under the poly-silicon gate edge in the drift region. As the drain voltage is increased, the poly-silicon edge toward the drain side voltage and its electric field are increased. To avoid the premature breakdown voltage because of this edge crowding effect, the drift doping concentration should be lowered at
the cost of the increased on-resistance. Alternatively, the edge electric field can be lowered by putting the thick field oxide under the gate edge without sacrificing the on-resistance. In addition, FOX can lower the gate-drain capacitance due to the increased effective dielectric thickness.

2. Deeper n-RESURF (n-well) drain is used to sustains higher voltage instead of the shallow one for 30(V) device. As it is explained in the chapter 3 , the doping profile under the FOX is the same as other n-well regions because of the lateral diffusion during the n-well annealing process. Therefore, on-resistance can be kept small.

3. The poly-silicon gate is extended over the drain region. The poly-edge should be put on top of FOX to prevent the premature breakdown voltage but the distance between FOX and channel is limited by the active and n-well masks alignment tolerance, bird’s beak, and thermal budget(lateral diffusion). And the gate-drain capacitance can not help being increased. However, its FOM is still low compared to others shown in Fig.4.18.
4.3.2 The breakdown voltages and on-resistances

The electro-potential contour at each device’s breakdown point is shown in Fig. 4.15. The RESURF effects are well-shown in the n-well drain region for both devices. The highest electric field exists around the poly-silicon gate edge at the relatively thin bird’s beak portion of FOX. This thin portion can be smaller as increasing the $Si_3N_4$ thickness used as the active region hard mask but the silicon surface stress is higher at the same time. The breakdown voltages of $n^+$ trench and pbody junction and $n^+$ substrate and pbody junction in the Fig. 4.1 (b) are around 35(V). However, the low-side MOSFET breakdown voltage in Fig. 4.14 can be increased to 56(V) without suffering from the 35(V) breakdowned junctions because of the merged-charge effects explained in the chapter 3. As it is shown in

Figure 4.15: The electro-potential contour at the breakdown point for (a) High-side MOSFET (b) Low-side MOSFET
Fig. 4.15 (b), the negative charges in the pbody are generated by three regions: One from the n-well positive charge, another from the n<sup>+</sup>-trench one, and the other from the n<sup>+</sup>-substrate one. Therefore, the lateral depletion width at the n<sup>+</sup>-trench and pbody junction and upward depletion width at the n<sup>+</sup>-substrate and pbody junction are increased and the device breakdown voltage is not limited by these portions. This is similar to the RESURF or super-junction effects. Eventually, highly doped n<sup>+</sup>-trench drain of Low-side switch can still be used for its low on-resistance without reducing its breakdown voltage.

The low-side on-resistance is 20% higher than the high-side one shown in Table 4.2 unlike the 30V devices cases at which both HS and LS show almost the same on-resistances. The details of their on-resistances are breakdowned into several components in Fig. 4.16. The n-well resistance portion of total LS on-resistance is larger than the one of total HS one. This is caused by the contact and the n<sup>+</sup>-trench location differences of each power switch. HS drain contact is located in the n-well on the substrate top surface and highly doped n<sup>+</sup>-region exist under the contact to form the ohmic contact and reduce its contact resistance shown in Fig. 4.14 (a). However, LS drain contact is located on the substrate bottom surface and there is no highly doped n<sup>+</sup>-region in the n-well except its trench shown in Fig. 4.14 (b). Therefore, the latter has larger n-well resistance laterally. Another reason is related to the n<sup>+</sup>-trench location and the current flowing direction. As it is shown in Fig. 4.17, the high current-densities during on-states are observed at the top surfaces because of the high doping concentration and low resistance on the surfaces in the n-well. While the HS drain current is coming from the top surface drain contact and flowing through the surface mostly to its channel, the LS one is coming up from the bottom surface drain contact and flowing through the n<sup>+</sup>-trench. Because the LS current which is coming through the n<sup>+</sup>-trench is spread when it reaches to its n-well from the substrate and the current is flowing more uniformly shown in Fig. 4.17 (b) and (c). Therefore, the LS n-well and total on-resistances are larger than HS ones.

4.3.3 Performances

Major properties of the novel vertical 50V voltage-rating MOSFETs are summarized in Table 4.2.

In addition, these can handle high operating current as integrated vertical switches for the first time, their on-resistances (R<sub>on</sub>) and gate-drain capacitances (Q<sub>gd</sub>) are low
Figure 4.16: The breakdown of specific on-resistances of 50V-rating power switches
Figure 4.17: The on-state current densities (a) HS current density (b) LS current density (c) current densities at the cut of AA’ (black dashed) for HS and BB’ (blue solid) for LS.
Table 4.2: Major properties of 50(V) voltage-rating Integrated Vertical Power MOSFETs

<table>
<thead>
<tr>
<th></th>
<th>BV(V)</th>
<th>$V_{th}$ (V)</th>
<th>$R_{on}$ ($m\Omega \cdot mm^2$)</th>
<th>$Q_{gd}$ ($nC/mm^2$)</th>
<th>FOM ($m\Omega \cdot nC$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side</td>
<td>53</td>
<td>1.9</td>
<td>48.3</td>
<td>1.6</td>
<td>75</td>
</tr>
<tr>
<td>Low-side</td>
<td>56</td>
<td>1.9</td>
<td>58.9</td>
<td>1.1</td>
<td>63</td>
</tr>
</tbody>
</table>

Figure 4.18: FOM comparisons for 50V MOSFETs

compared to other reported devices at the same voltage rating. Eventually these have the lowest FOM for the same 50V-rating power devices shown in Fig.4.18.

The HS and LS on-resistances for both 30V and 50V are compared to other companies’ BCD processed power devices ones in Fig.4.19. The proposed ones have low resistance-values even though some competitors’ devices are developed in the more advanced technology with high cost and even can not handle the high operating current.

Therefore, the novel devices show great performances not only in the high-frequency applications at which small FOM is required but also in the medium and low frequency ones at which small $R_{on}$ is preferred.
Figure 4.19: Breakdown voltages vs. On-resistances comparisons
Chapter 5

Integrated Analog/Digital CMOS and BJT Devices

Drivers and controllers as well as power stages should be integrated on the same substrate for the monolithic power converter design. These are comprised of different types of devices such as N- and P-channel analog/digital CMOS and NPN/PNP BJT because of their own unique superior characteristics [62]. For example, CMOS provides superior chip density, high noise threshold, and low power dissipation that is well suited to the demands of analog, logic and memory circuits. And BJT is often used in the analog circuit design because it has higher and more lithography independent transconductance, higher current and fast charging of loads, better transistor matching, low $l/f$ noise, and $V_{be}$ which can be matched with precision. Therefore, the combination of Bipolar and CMOS (BiCOMS) technology brings a lot of benefits and becomes more and more on demand [63]. And this technology and related devices should be optimized for the high performances of power converter circuits in our applications. The structures and major performances of the integrated devices would be discussed here.

5.1 Integrated Complementary Metal Oxide Semiconductor Field Effect Device (CMOS)

The integrated NMOS and PMOS structures are shown in Fig.5.1. Both have the 0.5$\mu m$ minimum physical gate length ($L_g$) and 20nm silicon dioxide thickness ($t_{ox}$). There
Figure 5.1: Cross-Sections of CMOS (process-simulated with FLOOPS in ISE-TCAD)
are many important parameters which have been considered for higher performance CMOS
device design below.

1. Transconductance \( (g_m) \) : The transconductance is defined as the change of drain
current over the change of the gate-source voltage \( (dI_d/dV_{gs}) \) expressed in Equ.5.1
and Equ.5.2. Small gate length \( (L_g) \), high channel mobility\( (\mu_{ch}) \), thin gate oxide \( (t_{ox}) \)
and low threshold voltage \( (V_{th}) \) are required to increase it.

\[
\begin{align*}
g_{mlin} & = \frac{W}{L_g} \mu_{ch} C_{ox} (V_{ds}) \quad \text{for linear region} \\
g_{msat} & = \frac{W}{L_g} \mu_{ch} C_{ox} (V_{gs} - V_{th}) \quad \text{for saturation region}
\end{align*}
\]

2. Saturation current \( (I_{dsat}) \) : The saturation current is the drain-source current for
\( V_{ds} \geq V_{gs} - V_{th} \) expressed in Equ.5.3. Its physical meaning of a device status is that
the inversion channel is pinched-off at the drain side and the electron(or hole) for
NMOS (or PMOS) is swept by the electric field at the drain side. Because it decides
the maximum drive current which supply the charges into the load capacitances, it
should be high enough not to cause power devices’ switching and driver losses much.
Again, it is required that small gate length, high channel mobility, thin gate oxide
and low threshold voltage to increase it.

\[
I_{dsat} = \frac{1}{2} \cdot \frac{W}{L_g} \mu_{ch} C_{ox} (V_{gs} - V_{th})^2 \quad \text{for saturation region}
\]

3. Substrate sensitivity \( (\gamma) \) : Because most CMOS are four-terminals (gate,drain,source
and substrate) devices, the substrate terminal(back-gate) can affect their threshold
voltage and performances. In other words, the threshold voltage varies with the
substrate voltage expressed in Equ.5.4. In the monolithic design, the substrate is
vulnerable to minority carrier injections which can change its voltage unless there are
firm isolations and/or special prevention techniques which are discussed in details in
the chapter 6. Therefore, \( \gamma \) is an important parameter which should be considered
carefully in our design. As it is shown in Equ.5.4, the body effect can be reduced with
thin gate oxide and low channel doping concentration.
\[ V_{th} = V_{th0} + \gamma \left( \sqrt{|V_{sub} - 2\Phi_F|} - \sqrt{2\Phi_F} \right) \]
\[ \text{for } \gamma = \frac{\sqrt{2q\varepsilon_{Si}N_{ch}}}{C_{ox}} \]

(5.4)

4. Leakage current \((I_{off})\) and Sub-threshold current \((I_{sub})\): A variety of leakage currents draw current away from the main logic path because of many reasons below:

- Weak inversion current (sub-threshold current)
- Reverse-biased pn junctions
- Drain-induced barrier lowering (DIBL)
- Gate-induced drain leakage (GIDL)
- Punch-through currents
- Gate oxide tunneling
- Hot carriers

Among these, the subthreshold current has been one particularly important type of leakage current. The sub-threshold current flows during the gate to source voltage is lesser than the threshold voltage of the device. This happens due to the carrier diffusion between the source and drain regions of the CMOS transistor in weak inversion. When gate to source voltage is smaller than but very close to threshold voltage of the device, the sub-threshold current becomes significant. As observed by [64] currently, the sub-threshold leakage is still playing the main part among the leakage currents above. \(I_{sub}\) depends on different effects and voltages which is expressed in Equ.5.5.

\[ I_{sub} = I_0 \cdot \exp \left\{ \frac{ln10 \cdot (V_{gs} - V_{th})}{S} \right\} \cdot \left( 1 - e^{-\frac{qV_{ds}}{kT}} \right) \] \( I_0 \) is a constant \( (5.5) \)

The subthreshold slope \((S = \partial V_g/\partial \log I_d)\) characterizes weak inversion current. The increase in the threshold voltage of the device keeps the \(V_{gs}\) of the NMOS transistor safely below its \(V_{th}\). This is the case for logic zero input. For the logic one input, the
increase in the threshold voltage of the device keeps the $V_{sg}$ of the PMOS transistor safely below its $V_{th}$. And the subthreshold leakage current is reduced.

However, researchers believe that gate leakage and reverse-biased junction Band To Band Tunneling (BTBT) will be as important as sub threshold from 45 nm process downwards. In addition, with technology scaling, the gate oxide thickness will be reduced and the substrate doping densities will be increased. As a result other factors such as gate-induced drain leakage (GIDL) and drain-induced barrier lowering (DIBL) will also become more and more evident. Therefore, future effective low leakage design will need to target at several components since all of them play important roles in the total leakage consumption. Various techniques at process and circuit level exist to reduce leakage consumption, including modifying doping profile, oxide thickness and channel length. Forward or inverse body biasing is also one of them, which is a technique resulting in variable threshold CMOS and discussed in the chapter 6.

5. Junction Breakdown: As it is similar to the power MOSFET structures, there are many p-n junctions in the CMOS. Though its logic supply voltage is low, the breakdown can be caused without special cautions. The breakdown voltage can be increased by reducing the substrate doping concentration. In addition, the junction capacitances can be reduced at the same time. However, if it is too low, the threshold voltage can be reduced and punch-through problem can be occurred also.

6. Drain voltage effects: High drain voltage causes depletion regions to merge and source barrier to drop. And the surface and bulk leakage path are created which are usually called as DIBL (Drain Induced Barrier Lowering) effect. DIBL increases subthreshold leakage and subthreshold swing and is responsible for the short channel effect which affects the threshold voltage, also. Additional short channel effects are the modulated channel length by the drain voltage and degraded channel mobility by high channel doping concentration, high electric field and velocity saturation.

All of these effects should be considered whenever new CMOS is developed in the FEOL (Front End Of Line) design stage. As it is explained, there are many obvious design trade-off which should be optimized. For example, the best NMOS threshold voltage and short channel behavior can be obtained at high substrate doping concentration. But
the best breakdown voltage and substrate sensitivity are obtained at low substrate doping concentration. Therefore, non-uniform doping profile (drain-engineering) techniques which are done by ion-implantations are used to overcome the trade-off. In our design, high doping concentration at the surface of the channel is to control threshold-voltages as shown in Equ.5.6, to prevent punch through and short channel effect and so on. Especially, the depth and dose should be sufficiently high to restrict lateral depletion of junctions for a sub-micron technology CMOS. Because our poly-silicon is doped by $n^+$ dopant, there is relatively large work function differences between $n^+$ poly-silicon and PMOS n-well. This makes PMOS threshold voltage too large a negative value. Thus boron is implanted into the channel region (counter doping) to raise it to an acceptable value. Meanwhile, low doping concentration at the bulk is to reduce the junction capacitance and to increase the breakdown voltage and so on.

$$V_{th0} = \phi_{ms} + 2\phi_F \pm \frac{\sqrt{4q\varepsilon_{si}(N_b + N_{implanted})}}{C_{ox}}$$  \hspace{1cm} (5.6)

For the low-voltage devices, the back-end processes (BEOL) are important to improve the metal resistances as well as reliabilities. Aluminum (Al), Copper (Cu), Tungsten (W) and Titanium (Ti) which forms low resistance silicide ($TiSi_2$) are used as multiple metal layers and several BPSG / ph-doped $SiO_2$ and $Si_3N_4$ layers are processed in the optimized temperature, time and gas. Though the details are explained in the chapter 7, major back-end processes and their functions are summarized in the Table5.1.

Owing to all of these optimized structures and design considerations, integrated CMOS show great performances shown in Table.5.2, Table.5.3, Fig.5.4 and Fig.5.5. AMI 0.5$\mu$m CMOS performances data are shown for comparison, also. Though breakdown voltages for proposed CMOS(BV$\sim$10V) are lower than AMI CMOS ones(BV$\sim$14V), these are enough to endure CMOS controller 5(V) power supply voltage. Good device design calls for 0.1~0.3x$V_{dd}$ as a device threshold voltage and 0.7V for NMOS and -1.3V for PMOS are achieved in the desirable ranges. Several important device performances such as saturation current(or drive current :$I_{drive}$), leakage current(off current:$I_{off}$), subthreshold slope, transconductance and output resistance are compared in Fig.5.4 for NMOS and Fig.5.5 for PMOS.
Table 5.1: Major back-end materials, annealing conditions and functions

<table>
<thead>
<tr>
<th>Material</th>
<th>Annealing Temperature(°C)</th>
<th>Annealing Time(sec)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>600</td>
<td>15~60 (RTA)</td>
<td>First annealing to form TiSi₂</td>
</tr>
<tr>
<td>Ti</td>
<td>800</td>
<td>30~60 (RTA)</td>
<td>Second annealing to reduce TiSi₂ and TiN to its final resistance</td>
</tr>
<tr>
<td>BPSG SiO₂</td>
<td>800~1000 (BPSG-PSG)</td>
<td></td>
<td>Ion protection, better flow at low temperature and to smooth the surface topography</td>
</tr>
<tr>
<td>TiN</td>
<td>400~500</td>
<td>1800</td>
<td>Adhesion/barrier layer, to reduce electrical resistance to the underlying metal, to protect it from the corrosive W CVD chemistry and to improve its barrier properties</td>
</tr>
<tr>
<td>W</td>
<td></td>
<td></td>
<td>Contact filling to avoid Al step</td>
</tr>
<tr>
<td>Al+Si(1%)+Cu(4%)</td>
<td></td>
<td></td>
<td>Metal</td>
</tr>
<tr>
<td>SiO₂</td>
<td>400</td>
<td></td>
<td>IMD</td>
</tr>
<tr>
<td>ph-doped SiO₂ and Si₃N₄</td>
<td>400</td>
<td></td>
<td>Protection from contaminations</td>
</tr>
<tr>
<td></td>
<td>400~450</td>
<td>1800</td>
<td>Final heating to alloy the metal contacts and to reduce charges associated with Si/SiO₂ interface</td>
</tr>
</tbody>
</table>
Table 5.2: NMOS Major properties Comparisons

<table>
<thead>
<tr>
<th></th>
<th>Min.feature(μm)</th>
<th>$t_{ox}$(nm)</th>
<th>$BV$($V$)</th>
<th>$V_{th}$($V$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.5</td>
<td>20</td>
<td>10</td>
<td>0.7</td>
</tr>
<tr>
<td>AMI NMOS</td>
<td>0.5</td>
<td>14</td>
<td>14</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Unlike the conventional CMOS structure, there is a highly doped $n^+$ substrate and additional junction which consists of this and p-body in Fig.5.1. This additional junction may create parasitic devices which can cause unwanted effects. All of the matters related to this are discussed in the chapter 6 in details. However, the design challenges for PMOS are discussed here to verify the reliability of PMOS performances.

As it is shown in Fig.5.2 (a), there is the internal NPN-BJT($PMOS_{NPN}$) comprised of the n-well, p-body and $n^+$-substrate. During the dead-time, $n^+$-substrate voltage becomes (-)diode turn-on($-V_{dom}$) voltage shown in Fig.5.2 (b) because the LS internal body-diode turns on. Because the base-emitter junction in PMOS turns on at the same time, the large current is flowing through the NPN BJT. Therefore, special strategy is proposed to prevent this situation in the chapter 6 and the problem can be prevented successfully.

Another concern happens when the HS switch turns on. For the PMOS, when the HS is conducting the operating current, the switching node voltage in Fig.5.2 (a) equals to the buck-converter input voltage ($V_{in}$) and the depletion region extends into the p-body due to the reverse-biased p-body and $n^+$-substrate junction in addition to another depletion region due to the n-well and p-body reverse-biased junction. If $d_1$ in Fig.5.2 (a) is small, punch-through happens and huge current is flowing through the BJT. Therefore, $d_2$ in Fig.5.2 (a) should be decided carefully considering n-well depth as well as $d_1$ related to the punch-through problem. Because $d_2$ decides the etched trench depth for power switches and isolations, it affects the key BCD fabrication process, also. Besides, $d_1$ distance is affected not only by the n-well depth and the epitaxial layer thickness but also by the substrate wafer dopant upward diffusion($d_3$) shown in Fig.5.3. The arsenic is selected as a substrate dopant due to its low diffusivity and small $d_3$. Eventually, the punch-through voltage for a designed PMOS is designed larger than power MOSFET breakdown voltages.
Figure 5.2: (a) Parasitic BJT in the PMOS structure (b) The BJT schematic during the dead-times (c) The BJT schematic during the HS switch on
Figure 5.3: PMOS vertical doping profile cut below the channel region: Y is the vertical axis.

Figure 5.4: NMOS Performance Comparisons
Table 5.3: PMOS Major properties Comparisons

<table>
<thead>
<tr>
<th></th>
<th>Min.feature(μm)</th>
<th>$t_{ox}$(nm)</th>
<th>BV(V)</th>
<th>$V_{th}$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>0.5</td>
<td>20</td>
<td>10</td>
<td>-1.3</td>
</tr>
<tr>
<td>AMI PMOS</td>
<td>0.5</td>
<td>14</td>
<td>14</td>
<td>-1.0</td>
</tr>
</tbody>
</table>

Figure 5.5: PMOS Performance Comparisons
5.2 Integrated Bipolar Junction Transistor (BJT)

The BJT collector current and its transconductance are expressed:

\[ I_c = I_0 \cdot e^{\frac{qV_{be}}{kT}} \]  
\[ g_m = \frac{\partial I_c}{\partial V_{be}} = \frac{qI_c}{kT} \]  

While the MOS transconductances in Equ.5.1 and Equ.5.2 are process, geometry dependent and functions of \( \sqrt{I_d} \), the BJT one in Equ.5.8 is process, geometry independent and a function of \( I_c \). Therefore, as it is explained before, bipolar devices have larger transconductance and provide more drive current to charge capacitance load. Because analog and RF applications typically require precision passive components such as resistors, capacitors, and inductors, BJT has been one of the most popular devices in these areas. When the novel BJT structure and process are designed, several trade-off below are considered for its high performances:

1. Collector
   - High doping concentration to reduce collector resistance
   - High doping concentration to enhance diffusion in base
   - High doping concentration to reduce collector-base depletion region width and transit time
   - Low doping concentration to reduce basecollector capacitance
   - Wide collector effective area to collect large number of electron for NPN (or hole for PNP)

2. Base
   - High doping concentration to reduce collector punch-through
   - Low doping concentration (Gummel Number) to increase gain
   - Narrow width to increase gain
3. Emitter

- High doping concentration at solubility limit to increase gain
- High doping concentration to reduce emitter resistance
- Low doping concentration to avoid bandgap narrowing
- Abrupt profiles to control junction depth
- Phosphorous as a dopant for NPN instead of Arsenic to reduce thermal cycle and increase activation

The integrated NPN and PNP BJT structures are shown in Fig.5.6. P-base implantation for POWER MOSFETs is used to form the NPN base and PNP emitter area. And n-well implantation for CMOS builds NPN collector and PNP base regions at the same time. The BJT doping profiles cut in the vertical direction are shown in Fig.5.7.

Due to the relatively high doping concentration of NPN base region shown in Fig.5.7 (a), its emitter injection efficiency and gain($\text{beta}$) are low. Though PNP base width is larger than NPN one in Fig.5.7 (b) which makes the base transfer factor small and its emitter doping concentration is low which makes the emitter injection efficiency low, its
gain is relatively high because of the low base doping concentration which increases the emitter injection efficiency. There are two possible BJT operating current flowing paths in the given structure in Fig.5.6. One possible path is through the silicon surface and the other is through the bulk. As it is shown in Fig.5.8, large portion of currents is flowing through the bulk instead of the surface. The major current path is affected by its gain which is decided by the base transfer factor and the emitter injection efficiency. While the lateral surface base width is limited by the lithography technology and the dopant lateral diffusion, the vertical base width is decided by the vertical diffusion which can be controlled by the annealing time and temperature. Because NPN surface base width is larger than vertical one, the former base transfer factor and gain are lower than the latter ones. However, there is not so much difference between the surface base width and the vertical one for PNP and both transfer factors should be almost the same. As it is shown in Fig.5.7, the BJT base regions have the Gaussian doping profiles which have the maximum values at the surfaces. And the vertical base region which is far from the surface has lower doping concentration. Therefore, the emitter injection efficiency and gain in the bulk should be higher than the surface ones. In other words, NPN vertical current path has not only high base transfer

Figure 5.7: (a)NPN doping profiles cut in the vertical direction (b)PNP doping profiles cut in the vertical direction
Figure 5.8: (a)NPN current flowing path in the forward active operating region (B)PNP current flowing path in the forward active operating region

factor but also high emitter injection efficiency and most currents flow through this path shown in Fig.5.8 (a). Meanwhile, PNP vertical current path has high emitter injection efficiency and most currents flow through this path shown in Fig.5.8 (b). It should be noted that because there is not so much difference between the surface base width and the vertical one for PNP as mentioned before, PNP current is more spread compared to the NPN one shown in Fig.5.8 (b).

The bipolar transistor blocking characteristics are categorized into three [29]. First one is the open emitter breakdown voltage ($BV_{CB0}$) in Fig.5.9. In this case, the bipolar transistor behaves like a p-n junction diode and $BV_{CB0}$ is determined by the doping concentration and thickness of the low doping region. Second one is the open base breakdown voltage ($BV_{CE0}$) in Fig.5.9. $BV_{CE0}$ is decided by the BJT current gain especially the multiplication factor ($M$). $M$ and $BV_{CE0}$ are expressed:

$$M = \frac{1}{1 - \left(\frac{V_C}{BV_{CB0}}\right)^6} \quad (5.9)$$
$$BV_{CE0} = \frac{1}{(1 + \beta)^\frac{1}{n}} \quad n \text{ is a constant} \quad (5.10)$$

It should be noted that there is a trade-off between BJT gain and breakdown voltage shown in Equ.5.10.
The last one is the shorted base case which is the normal circuit configuration for a BJT reverse-blocking mode. The BJT base is shorted to its emitter via the drive circuit to turn off itself and it endures high voltage across the collector and emitter. As the $V_{CE}$ approaches to $BV_{CBO}$, the impact ionization current is getting amplified by the current gain of the BJT and its breakdown voltage is collapsed to $BV_{CEO}$ shown in Fig.5.9. Therefore, maximum operating voltage for the bipolar transistor is limited to the open-base breakdown voltage ($BV_{CEO}$).

Good performances NPN and PNP BJT, compared with ST BCD BJTs’ ones shown in Table.5.4 and Table.5.5 each, can be integrated with CMOS and Power MOSFETs in a monolithic process. And NPN and PNP open-base breakdown voltage ($BV_{CEO}$) is 16V and 17V each enough considering 5V BJT supply voltage. It should be noted that there are several parasitic structures in the cross-section of BJTs shown in Fig.5.6. All of these undesirable devices operations should be subdued by the careful design. And the proposed BJT operations should not be affected not only by these parasitics but also by the main buck-converter stage operations. All of these are discussed in the chapter 6 in details. Eventually, the performances and reliabilities of BJTs are verified considering all the related cases and the novel BJTs do not suffer from these problems.
Table 5.4: NPN Major properties Comparisons

<table>
<thead>
<tr>
<th></th>
<th>Min.feature($\mu$m)</th>
<th>Gain($\beta$)</th>
<th>$BV_{ceo}(V)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPN</td>
<td>0.5</td>
<td>23</td>
<td>16</td>
</tr>
<tr>
<td>ST BCD NPN</td>
<td>0.5</td>
<td>70</td>
<td>15</td>
</tr>
</tbody>
</table>

Table 5.5: PNP Major properties Comparisons

<table>
<thead>
<tr>
<th></th>
<th>Min.feature($\mu$m)</th>
<th>Gain($\beta$)</th>
<th>$BV_{ceo}(V)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PNP</td>
<td>0.5</td>
<td>52</td>
<td>17</td>
</tr>
<tr>
<td>ST BCD PNP</td>
<td>0.5</td>
<td>40</td>
<td>13</td>
</tr>
</tbody>
</table>
Chapter 6

Monolithic Buck Convert Design Challenges, Proposed Solutions and Performances

In this section, different types of devices integration challenges for a monolithic buck converter design are addressed. And possible solutions are suggested and verified by ISE-TCAD Mixed-Mode/H-spice simulations and experiments. At the last section of this chapter, the monolithic buck converter performances in which the solutions are included are optimized.

6.1 Isolations

In a smart power IC technology, the interferences among various functions of devices have been one of the hardest problems to be solved [48]. Junction-Isolation (JI), Dielectric-Isolations (DI), and Self-Isolation (SI) are widely used well-known isolation techniques [65]. In our PIC structure, all of these isolation techniques would be incorporated to minimize devices and circuits malfunction caused by the poor isolations.

6.1.1 Lateral Isolations

For lateral isolation((L) in FIG.6.1)s among different types of devices, not only DI by TEOS filled trench but also JI by $n^+$-doped Trench and p junction is used shown in
6.1.2 Vertical Isolations

For vertical isolation ((V) in FIG.6.1)s, not only JI but also the Controlled p-body voltage strategy explained later is used shown in Fig.6.1. Both provide the electrical isolation functions by adjusting the applied voltages properly without adding complicated extra circuits.

6.1.3 Self-Isolations and FOX

Self-isolation is used mostly in MOS technology. Source and Drain junctions isolate themselves from each other under reverse bias for all devices. And FOX (Field Oxidation) is added in CMOS area as usual shown in Fig.6.1. In addition, the low doped RESURF is added to the CMOS area to prevent premature surface breakdown in the CMOS region which can be caused by the integrated high-voltage switches.

Because each type of device has its own p-body voltage, isolations among these devices such as highside-lowside, highside-highside circuits, lowside-lowside circuits, highside circuits-lowside circuits and so on. are very important. And these should be designed and included carefully as shown in Fig.6.23 and Fig.6.24. Otherwise, parasitic devices are working and the original devices functions are failed.
6.2 Parasitic devices On Prevention

The shoot-through which happens when both HS and LS turn on at the same time can damage the devices and make the power stage failed. Therefore, after one device turns off, another device does not turn on immediately but both devices remain off for a while. This additional time is called as *dead-time*. In one switching period, two dead-times are usually added intentionally. One is after the HS turns off and before LS turns on. The other is after the LS turns off and before HS turns on. During these times, the switching node (SW in Fig.4.2) becomes negative voltage because the LS internal (p-body and n$^+$-substrate in Fig.4.1) body-diode conducts the operating current. However, the negative SW voltage can affect other devices if there are no proper solutions. Therefore, the related problems and solutions are addressed in the following sections.

6.2.1 Grounded CMOS p-body effects

If the CMOS p-body contact is grounded as usual CMOS configuration, parasitic p-body n$^+$-substrate diode ($D_1$) in Fig.6.2 turns on during the dead-time and parasitic BJTs in Fig.6.2 conduct multiplied unexpected current due to their gains. This may increase the power consumption and affect the analog/digital circuit performances intensively.

6.2.2 Floated CMOS p-body effects

In SOI (Silicon On Insulator) technology, MOSFET body is usually floated [66] though it may cause several problems such as the kink effect, un-stable voltage and current bias points and output resistances [67].

The floated CMOS p-body voltage waveform is shown in Fig.6.7 for a buck-converter operation switching period. The waveform is simulated by the *ISE-TCAD* Mixed-Mode simulator including not only *TCAD Floops* process simulated HS/LS power switches and high- and low-side CMOS inverter drivers but also passive and parasitic inductors, capacitors and resistors which make the simulation results very close to the real conditions. This shows that though the floated p-body strategy can prevent the $D_1$ turning on during dead-times because the CMOS p-body voltage becomes negative following the SW voltage, other parasitic diodes and BJTs turning on can not be avoided during other operating periods except the dead-times.
Performance Degradations

It should be noted that the p-body potential is larger than 0.6(V) all the time except dead-times with floated CMOS p-body in Fig.6.7. During the HS on period \((D \cdot T_s)\), diode \(D_2\) turns on and BJT \(B_1\) conducts large current. While during the LS on period \((D' \cdot T_s)\), diode \(D_1\) turns on and both BJTs \(B_1\) and \(B_2\) conduct large currents shown in Fig.6.3. The Mixed-Mode simulation shows about 1.4(W) extra power dissipation is caused due to the parasitic BJT currents and power conversion efficiency is degraded by more than 10(\%).

Furthermore, the digital and analog circuit performances can be affected by the floated p-body voltage. The threshold voltage is a function of the total charge in the depletion region because the gate charge must mirror this before an inversion layer is formed. Thus, as p-body voltage \((V_{b})\) increases, the threshold voltage \((V_{th})\) also drops called as the *body effect* or the *back-gate effect* explained in the chapter 5 shown in Fig.6.4. As it is mentioned above, the p-body voltage is larger than 0.6(V) except the short dead-times.
Figure 6.3: Unexpected parasitic currents flowing due to the floated CMOS p-body in a buck converter topology

and the NMOS $V_{th}$ becomes small value and even negative one. This makes the inverter transfer curves left-shifted and increases the drain-source current and the dynamic power dissipation shown in Fig.6.5 for a given design. The left-shifted inverter switch voltage ($V_m$) can degrade the gate-driver performances when the inverter chains are chosen as a driver topology. In addition, the noise-margin low (NML) which represents the voltage ranges of logic 0 is degraded while the noise-margin high (NMH) which represents the voltage ranges of logic 1 is improved shown in Fig.6.6. Another well-known floated-body potential problem is a kink effect caused by the varied $V_b$ and $V_{th}$ [68]. This causes the abruptly increased device saturation current and degrades analog circuit performances such as voltage/current bias points, output resistances and transconductances. In addition, both analog and digital device- and circuit- performances are degraded by the uncontrolled floated p-body voltage.

Floated CMOS p-body voltage waveform explanation

The floated CMOS p-body potential ($V_b$) for a buck-converter operation is decided by the stored charges in the p-body itself. In other words, the ratio between $C_{bs}(pbody-$
Figure 6.4: An integrated NMOS threshold-voltage ($V_{th}$) as a function of p-body voltage ($V_b$).

Figure 6.5: An integrated Inverter Transfer Functions and Currents at different p-body voltages.
Figure 6.6: An integrated Inverter Noise margins at different p-body voltages

NMOS source capacitance) and $C_{bsw}$ (pbody-switching node capacitance) shown in Fig.6.2 decides the p-body voltage described in Eqn.6.1. As it is shown in Eqn.6.1, both capacitances in the coefficient of $dV_{sw}/dt$ are junction capacitances and functions of two junction-voltages ($V_{sw}$ and $V_b$). As the $V_{sw}$ is changed by power switches on/off, $V_b$ is following also. Therefore, both capacitances are changed following their junction voltages at the same time. Therefore, it is complex to derive the exact $V_b$ transient equation for the buck-converter operation. However, it is still possible to explain and predict $V_b$ in Fig.6.7 with the help of C-V graphs. Based on this analysis, new methodology preventing parasitic devices turning on will be proposed.

$$\frac{dV_b}{dt} = \left\{ \frac{C_{bsw}(V_{sw},V_b)}{C_{bsw}(V_{sw},V_b) + C_{bs}(V_{sw},V_b)} \right\} \cdot \frac{dV_{sw}}{dt}$$ (6.1)

A circuit model which is comprised of inherit capacitances of a NMOS in Fig.6.2 and a transient switching node voltage source is shown in Fig.6.8. And both junction capacitances as functions of their junction voltages are shown in Fig.6.9, also. It should be noted that the capacitances are increased abruptly when their p-n diodes turn on [69]. As
Figure 6.7: CMOS p-body voltage waveforms vs. time (TCAD Mixed-Mode simulations with process simulated integrated devices)
these capacitances graphs are shifted following the switching node voltage, the ratio of $C_{bs}$, $C_{bsw}$ and $V_b$ are decided explained below in details.

The pbody-source capacitance from Fig.6.9 can be re-drawn simply in C vs. $V_{b0}$ (pbody-ground voltage) axis shown in Fig.6.10 (a). In the same way, the pbody-switching capacitance can be re-drawn simply in C vs. $V_{bsw}$ (pbody-switching voltage) axis shown in Fig.6.10 (b) but it should be axis-transformed to be drawn in the same axis as the pbody-source capacitance (a). The axis transformed $C_{bsw}$ is shown in Fig.6.10 (c) and two capacitances can be drawn on the same axis. $C_{bsw}$ in Fig.6.10 (c) is a function of $V_{sw}$ and three $C_{bsw}$ curves based to the buck converter’s three major status related to switches on/off shown in Fig.6.11 and $C_{bs}$ are drawn in Fig.6.10 (d). In other words, the $C_{bsw}$ curve is shifted horizontally as the $V_{sw}$ is changed in a time-domain shown in Fig.6.11.

The $V_b$ is analyzed during the transient variation of $V_{sw}$ such as A,B,C and D shown in Fig.6.11 in details below.

1) During A : Let’s assume the initial $V_{b1}$ as 0(V). Eventually, it will be shown that the steady-state $V_b$ waveform is not affected by the initial $V_{b1}$ value assumption itself. As $V_{sw}$ is changed from 0(V) (ignoring switches’ on-resistances) to $-V_{don}(V)$ in the time axis shown in Fig.6.11, its corresponding $C_{bsw}$ is shifted from the blue-line to the pink-line in
Figure 6.9: Parasitic Capacitances of NMOS pbody-source ($C_{bs}$) and pbody-switching node ($C_{bsw}$) shown in Fig.6.2 as functions of applied voltages.
Figure 6.10: $C_{bs}$ and $C_{bsw}$ as functions of applied voltages: (a) $C_{bs}$ vs. body-ground Voltage ($V_{b0}$) (b) $C_{bsw}$ vs. body-switching Voltage ($V_{bsw}$) (c) $C_{bsw}$ vs. body-ground Voltage ($V_{b0}$) (d) $C_{bs}$ and $C_{bsw}$ at various switching voltages ($V_{sw}$) => pink-line: for dead-times, blue-line: for $D'T$, black-line: for $DT$
Figure 6.11: The buck converter switching node voltage ($V_{sw}$) including dead-times

the $V_{b0}$ axis shown in Fig.6.12. Because $V_b$ changes from $V_{b1}$ to $V_{b2}$ and $C_{bs}$ and $C_{bsw}$ are the same for this voltage range, Equ.(6.1) during this period becomes:

\[
\frac{dV_b}{dt} = \left\{ \frac{1}{2} \right\} \cdot \frac{dV_{sw}}{dt}
\]

And the final $V_b$ is:

\[
V_{b2} = \left\{ \frac{1}{2} \right\} \cdot -V_{don}
\]

which is around $-0.35(V)$ for $0.7(V)$ diode on voltage.

2) During B: As $V_{sw}$ is changed from $-V_{don}$ to $V_{in}(V)$ (ignoring switches’ on-resistances) in the time axis shown in Fig.6.11, its corresponding $C_{bsw}$ is shifted from the pink-line to the green-line in the $V_{b0}$ axis shown in Fig.6.13. $C_{bs}$ and $C_{bsw}$ are the same until $V_b$ reaches to $V_{don}$ and Equ.(6.1) becomes during this time:

\[
\frac{dV_b}{dt} = \left\{ \frac{1}{2} \right\} \cdot \frac{dV_{sw}}{dt}
\]

$C_{bs}$ is increased abruptly after this point and Equ.(6.1) becomes:

\[
\frac{dV_b}{dt} = 0 \cdot \frac{dV_{sw}}{dt}
\]
Figure 6.12: $C_{bs}$ and $C_{bsw}$ as functions of applied voltages: The solid arrow indicates $C_{bsw}$ shift during A and the dashed arrow does $V_b$ change at the same time.

In other words, there is no more $V_b$ increase after it reaches to $V_{don}$. It is identical to the physical meaning of $D_2$ diode turning on in Fig.6.2, also. Due to the conduction of this diode, $V_b$ is clamped to $V_{don}$. Therefore, the final $V_b(=V_{b3})$ is the same as $V_{don}$ which is around 0.7(V).

3) During C: As $V_{sw}$ is changed from $V_{in}$ to $-V_{don}(V)$ (ignoring switches’ on-resistances) in the time axis shown in Fig.6.11, its corresponding $C_{bsw}$ is shifted from the green-line to the pink-line in the $V_{b0}$ axis shown in Fig.6.14.

$C_{bs}$ is much larger than $C_{bsw}$ until $C_{bsw}$ reaches to the blue-line and Equ.(6.1) becomes during this time:

$$\frac{dV_b}{dt} = 0 \cdot \frac{dV_{sw}}{dt}$$

In other words, there is no $V_b$ change during this period. As $C_{bsw}$ is shifted from the blue-line to the pink-line, $C_{bsw}$ is much larger than $C_{bs}$ and Equ.(6.1) becomes:

$$\frac{dV_b}{dt} = 1 \cdot \frac{dV_{sw}}{dt}$$
Figure 6.13: $C_{bs}$ and $C_{bsw}$ as functions of applied voltages: The solid arrow indicates $C_{bsw}$ shift during B and the dashed arrow does $V_b$ change at the same time.

Therefore, the $V_b$ change is the same as $V_{sw}$ change during this period which is $-V_{don}$ and the final $V_b(=V_{b4})$ is $V_{b3} - V_{don}(=V_{don} - V_{don})$ which is around 0(V).

4) During D: As $V_{sw}$ is changed from $-V_{don}$ to 0(V) (ignoring switches’ on-resistances) in the time axis shown in Fig.6.11, its corresponding $C_{bsw}$ is shifted from the pink-line to the blue-line in the $V_b$ axis shown in Fig.6.15.

$C_{bsw}$ is much larger than $C_{bs}$ during this period and Equ.(6.1) becomes during this time:

$$\frac{dV_b}{dt} = 1 \cdot \frac{dV_{sw}}{dt}$$

Therefore, the $V_b$ change is the same as $V_{sw}$ change ($=V_{don}$) during this period and the final $V_b(=V_{b5})$ is $V_{b4} + V_{don}(=0+V_{don})$ which is around 0.7(V).

5) During the second A: Unlike the previous 1)During A case at which the initial $V_b$ was 0(V)($=V_{b1}$), the $V_b$ is $V_{don}(=V_{b5})$ at the beginning of the second A period. And it is shown that the final $V_b$ waveform is not affected by the initial $V_b$ value itself.

As $V_{sw}$ is changed from 0(V) to $-V_{don}$ (ignoring switches’ on-resistances) in the
Figure 6.14: $C_{bs}$ and $C_{bsw}$ as functions of applied voltages: The solid arrow indicates $C_{bsw}$ shift during C and the dashed arrow does $V_b$ change at the same time.

Figure 6.15: $C_{bs}$ and $C_{bsw}$ as functions of applied voltages: The solid arrow indicates $C_{bsw}$ shift during D and the dashed arrow does $V_b$ change at the same time.
Figure 6.16: $C_{bs}$ and $C_{bsw}$ as functions of applied voltages: The solid arrow indicates $C_{bsw}$ shift during the second A and the dashed arrow does $V_b$ change at the same time.

In the time axis shown in Fig.6.11, its corresponding $C_{bsw}$ is shifted from the blue-line to the pink-line in the $V_{b0}$ axis shown in Fig.6.16. $C_{bsw}$ is much larger than $C_{bs}$ during this period and Equ.(6.1) becomes during this time:

$$\frac{dV_b}{dt} = 1 \cdot \frac{dV_{sw}}{dt}$$

Therefore, the $V_b$ change is the same as $V_{sw}$ change ($=V_{don}$) during this period and the final $V_b(=V_{b6})$ is $V_{b5} - V_{don}(=V_{don} - V_{don})$ which is around $0(V)$.

6) During the second B: As $V_{sw}$ is changed from $-V_{don}$ to $V_{in}(V)$ (ignoring switches’ on-resistances) in the time axis shown in Fig.6.11, its corresponding $C_{bsw}$ is shifted from the pink-line to the green-line in the $V_{b0}$ axis shown in Fig.6.17. $C_{bs}$ and $C_{bsw}$ are the same until $V_b$ reaches to $V_{don}$ and Equ.(6.1) becomes during this time:

$$\frac{dV_b}{dt} = \left\{ \frac{1}{2} \right\} \cdot \frac{dV_{sw}}{dt}$$
$C_{bs}$ is increased abruptly after this point and Equ.(6.1) becomes:

$$\frac{dV_b}{dt} = 0 \cdot \frac{dV_{sw}}{dt}$$

In other words, there is no more $V_b$ increase after it reaches to $V_{don}$. It is identical to the physical meaning of $D_2$ diode turning on in Fig.6.2, also. Due to the conduction of this diode, $V_b$ is clamped to $V_{don}$. Therefore, the final $V_b(= V_{b7})$ is the same as $V_{don}$ which is around 0.7(V). This is similar to the 2)During B case.

Because final $V_b$ during the second B period is the same as the one during the first B, the remain waveform pieces are repeated from now and the $V_b$ waveform reaches to its steady-state.

Eventually, the floated body-voltage of $V_b$ in Fig.6.7 is explained with the help of C-V graphs and equations easily. Based on the analysis, novel idea preventing parasitic devices turning on is proposed and verified in the following section.
6.2.3 Controlled CMOS p-body voltage strategy and experimentation

If the CMOS p-body potential \( V_b \) can be controlled for power-converter operations and it becomes a proper negative value following the negative switching node voltage \( V_{sw} \) during the dead-times and stays almost zero elsewhere, the parasitic devices remain off all the time. This is possible by just substituting the voltage variable \( C_{bs}(V_{sw}, V_b) \) in Equ.6.1 with the proper fixed-capacitance capacitor \( C_{fix} \) shown in Equ.6.3 without adding the complicated active pull-down voltage controlled circuits [70].

\[
\frac{dV_b}{dt} = \frac{C_{bsw}(V_{sw}, V_b)}{C_{bsw}(V_{sw}, V_b) + C_{fix}} \cdot \frac{dV_{sw}}{dt} \quad (6.3)
\]

Because \( C_{bsw}(V_{sw}, V_b) \) becomes large under the forward-bias condition, the coefficient of \( dV_{sw}/dt \) becomes almost one and \( dV_b/dt \) follows \( dV_{sw}/dt \) in Equ.6.3 and this is the case of dead-time period. Meanwhile, because \( C_{bsw}(V_{sw}, V_b) \) becomes small under the reverse-bias condition, the coefficient of \( dV_{sw}/dt \) becomes small and \( dV_b/dt \) does not follow \( dV_{sw}/dt \) much in Equ.6.3 during this time. This is the other periods except dead-times. Eventually, the CMOS p-body potential can be controlled as it is desired above by just connecting proper fixed-value capacitor to the CMOS p-body shown as a rectangular red line in Fig.6.7.

Because \( V_b \) follows \( V_{sw} \) well during the dead-time, it reaches to around -0.4(V) and the voltage across the \( D_1 \) diode is only \( \sim 0.3(V) \) which is smaller than the diode turn on voltage. Therefore, the parasitic diodes and BJTs remain off all the times.

This novel parasitic components subduing strategy is verified by ISE-TCAD Mixed-Mode simulation with a monolithic synchronous buck-converter including all parasitics and experiments.

The simulated monolithic buck is shown in Fig.6.22 including \( C_{fix} \). Both \( B_2 \) and \( B_1 \) collector currents in Fig.6.2 are shown in Fig.6.18 without \( C_{fix} \) (solid lines) and with \( C_{fix} \) (dash lines). And the most serious problem maker of n-well p-body \( n^+ \)-substrate BJT \( (B_2) \) current is reduced more than \( 1 \cdot 10^{-6} \) times which is very negligible during the dead-time.

The NPN BJT current as a function of the \( C_{fix} \) is measured with the transient signal voltage source connected to the \( B_2 \) emitter which represents the switching node voltage by Agilent 4155C. Because the NPN collector current depends on its emitter voltage,
Figure 6.18: $B_2$ and $B_1$ collector currents: Solid lines are with $C_{fix}$ and dash lines are without $C_{fix}$.
the minimum emitter voltage during the transient sweep decides its collector current shown in Fig.6.19. As the minimum emitter voltage is increased negatively, the collector current is increased. Due to the safety limit of the equipment, the maximum measured current is 0.1(A). However, the current can be reduced dramatically with the proper size of $C_{fix}$ shown in Fig.6.19. Eventually, the BJT current is reduced $3 \cdot 10^{-6}$ times with 54pF $C_{fix}$ at the minimum emitter voltage of -0.7(V) which is the LS body-diode turn on voltage. As it is mentioned before, the proper size of $C_{fix}$ is decided by the Equ.6.3. In other words, the coefficient of $\frac{dV_{sw}}{dt}$ should be closed to 1 during the dead-time but very small else. And $V_b$ can stay almost 0 voltage except the dead-times. If it is too large, $V_b$ can not follow $V_{sw}$ change during the dead-time and parasitic devices turn on. If it is too small, $V_b$ follows $V_{sw}$ change during $DT_s$ and $D_2$ diode turns on which causes extra power consumption. Therefore, the proper size of the capacitor should be decided. Based on the experiments and simulations, $4 \sim 8fF/um^2$ is the proper capacitance for our design. This capacitor can become either of the external or internal one. The poly gate capacitor with highly doped p-body capacitor can be used for this function due to its low dependence on the bias voltage.
across it. The capacitance deviation for voltage changes is less than 10% which is still in the reasonable required capacitance range from 0(V) to -1(V) $V_b$ voltage. The actual consumed capacitor area is decided after the optimized converter design but it is small enough to be integrated on the same substrate with other devices. The optimization and area would be discussed in the following section.

It should be noted that though the p-body voltage is changed over the period (0.1(V) or -0.03(V) for either switches on and -0.4(V) for dead-times), the variable p-body voltage technique ($V_{th}$ scaling Techniques) is the most widely employed technique for enhancing the performances of VLSI circuits such as boosting switching speed and reducing power dissipation. And its reliability has been proved by many related research so far. In other words, Controlled CMOS p-body voltage strategy does not cause severe performances degradation not only for devices but also circuits verified by TCAD/Cadence simulations and experiments. In addition, parasitic BJT gain sensitivity which depends on the fabrication process tolerance is tested by the life-time control method and its result is not changed. And it is claimed that $C_{fix}$ strategy is in-sensitive to the gain and fabrication variation, also.

### 6.3 Optimized Buck converter performances

It is very hard to predict the exact power losses for a power converter as mentioned before. Fortunately, there is usually not so much difference between the rough calculation and real values for power losses. Therefore, power stages and drivers power consumption are calculated based on several equations and the buck converter is optimized. It is noted that the small ripple approximation is used for power losses calculations here.

The operating conditions for the buck converter and abbreviation explanation for power losses equations are shown in Table.6.1 and Table.6.2 each.

#### 6.3.1 Lowside (synchronous) power MOSFET optimization

The major predicted power losses for lowside switch are expressed below:

$$P_{CON,LS}(A_{LS}) = (1 - D) \cdot I_{out}^2 \cdot \left( \frac{R_{on,sp,LS}}{A_{LS}} \right)$$

(6.4)
Table 6.1: Integrated synchronous buck converter operating conditions

<table>
<thead>
<tr>
<th>$V_{in}(V)$</th>
<th>$V_{out}(V)$</th>
<th>$V_{dd}(V)$</th>
<th>$I_{out}(A)$</th>
<th>Duty(D)</th>
<th>frequency($f_s$)(hz)</th>
<th>$t_{deadtime}(sec)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>1.2</td>
<td>5</td>
<td>10</td>
<td>0.1</td>
<td>1M</td>
<td>20n</td>
</tr>
</tbody>
</table>

Table 6.2: Abbreviation explanation for power losses equations

<table>
<thead>
<tr>
<th>$P_{CON}$</th>
<th>$P_{OSS}$</th>
<th>$P_{DIODE,ON}$</th>
<th>$P_{DRIVER}$</th>
<th>$P_T$</th>
<th>$P_{SW}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction Loss</td>
<td>Output Charge Loss</td>
<td>Diode on Loss</td>
<td>Driver Loss</td>
<td>Total Loss</td>
<td>Switching Loss</td>
</tr>
<tr>
<td>$Q_{oss,sp}$</td>
<td>$Q_{g,sp}$</td>
<td>$I_{G,DRIVER,P}$</td>
<td>$I_{G,DRIVER,N}$</td>
<td>$Q_{gs2,sp}$</td>
<td>$Q_{gd,sp}$</td>
</tr>
<tr>
<td>Output charge</td>
<td>gate charge</td>
<td>PMOS gate driver I</td>
<td>NMOS gate driver I</td>
<td>gate-source charge after $V_{th}$</td>
<td>gate-drain charge</td>
</tr>
</tbody>
</table>
\[ P_{\text{OSS,LS}}(A_{\text{LS}}) = \left( \frac{Q_{\text{oss,sp,LS}} \cdot A_{\text{LS}}}{2} \right) \cdot V_{\text{in}} \cdot f_s \quad (6.5) \]

\[ P_{\text{DIODE,ON,LS}} = V_D \cdot I_{\text{out}} \cdot (2 \cdot t_{\text{deadtime}}) \cdot f_s \quad (6.6) \]

\[ P_{\text{DRIVER,LS}}(A_{\text{LS}}) = V_{dd} \cdot (Q_{g,sp,LS} \cdot A_{\text{LS}}) \cdot f_s \quad (6.7) \]

And the total lowside switch power loss is:

\[ P_{T,LS}(A_{\text{LS}}) = P_{\text{CON,LS}}(A_{\text{LS}}) + P_{\text{OSS,LS}}(A_{\text{LS}}) + P_{\text{DIODE,ON,LS}} + P_{\text{DRIVER,LS}}(A_{\text{LS}}) \quad (6.8) \]

Because the low-side on-resistance is reduced as the area is increased, the conduction loss is decreased shown in Equ.6.4. However, other losses such as the output charge loss and the gate driver loss are proportional to the consumed area shown in Equ.6.5 and Equ.6.7 each. Therefore, there is an optimized area for low-side power switch shown in Fig.6.20. Though the lowest total power loss point is around 10mm\(^2\), 5mm\(^2\) is selected considering silicon area consumption, cost, and the power loss.

### 6.3.2 Highside (control) power MOSFET optimization

The major predicted power losses for highside switch are expressed below:

\[ P_{\text{CON,HS}}(A_{\text{HS}}) = D \cdot I_{\text{out}}^2 \cdot \left( \frac{R_{\text{on,sp,HS}}}{A_{\text{HS}}} \right) \quad (6.9) \]

\[ P_{\text{OSS,HS}}(A_{\text{HS}}) = \left( \frac{Q_{\text{oss,sp,HS}} \cdot A_{\text{HS}}}{2} \right) \cdot V_{\text{in}} \cdot f_s \quad (6.10) \]

\[ P_{\text{SW,HS}}(A_{\text{HS}}) = \left( \frac{I}{I_{G_\text{HS,DRIVER,P}}} + \frac{I}{I_{G_\text{HS,DRIVER,N}}} \right) \cdot V_{\text{in}} \cdot \left\{ (Q_{g_{s2,sp,HS}} \cdot A_{\text{HS}}) + (Q_{g_{d,sp,HS}} \cdot A_{\text{HS}}) \right\} \cdot f_s \quad (6.11) \]
Figure 6.20: Power losses vs. area for low-side switch

\[ P_{\text{DRIVER\_HS}}(A_{\text{HS}}) = V_{dd} \cdot (Q_{gsp\_HS} \cdot A_{\text{HS}}) \cdot f_s \]  

(6.12)

And the total high-side switch power loss is:

\[ P_{T\_HS}(A_{\text{HS}}) = P_{\text{CON\_HS}}(A_{\text{HS}}) + P_{\text{OSS\_HS}}(A_{\text{HS}}) + P_{\text{SW\_HS}}(A_{\text{HS}}) + P_{\text{DRIVER\_HS}}(A_{\text{HS}}) \]  

(6.13)

Because the high-side on-resistance is reduced as the area is increased, the conduction loss is decreased shown in Equ.6.9. However, other losses such as the output charge loss, the gate driver loss and the switching loss are proportional to the consumed area shown in Equ.6.10, Equ.6.12 and Equ.6.11 each. Therefore, there is an optimized area for high-side power switch shown in Fig.6.21. 0.5mm² is selected considering silicon area consumption, cost and power loss.

In addition, chain gate drivers are designed to achieve not only low switching losses but also desired both high- and low-side power switches turning on/off speed which is around 10nsec.
In the circuit simulations, the 1st and 2nd shoot-through protection logic-gates, level shifters and PWM signal generators are optimized, also.

6.3.3 Monolithic synchronous buck converter performances

The high current, fast frequency optimized monolithic synchronous buck converter including gate drivers is designed and simulated with ISE-TCAD mixed mode simulators shown in Fig.6.22. All power and analog/digital devices used for the simulations are process-simulated based on the developed BCD recipe in the chapter 7. As it is expected section 6.1 and 6.2 above, no parasitic devices turn on during entire switching period and power losses can be kept small thanks to the $C_{fix}$. And the entire converter layouts are shown in Fig.6.23 and Fig.6.24 with the emphasize of isolations.

In addition, all the parasitic components such as package inductors and inductor- and capacitor- ESR(Equivalent series resistance)s are added in the mixed-mode simulations based on the required inductor current and output voltage ripple specifications and real
Figure 6.22: Mixed-Mode simulated Buck-Converter including all parasitics

data from several component-making companies (JW miller, Taiyo Yuden etc.) to make the simulation results close to the experiment ones.

Eventually, ISE-TCAD mixed mode simulations including all the monolithic solutions above show the buck converter loss breakdowns at high frequency (1Mhz) and middle frequency (300Khz) shown in Fig.6.25 and Fig.6.26 each. And its high-efficiency curve at high switching frequency as varying its load current is drawn in Fig.6.27.
Figure 6.23: Monolithic synchronous buck converter layout drawing

(a) Monolithic synchronous buck converter layout (not scaled)

(b) Equivalent monolithic synchronous buck converter schematic

Figure 6.23: Monolithic synchronous buck converter layout drawing
Figure 6.24: Monolithic synchronous buck converter layout
Figure 6.25: Loss Breakdown at 1Mhz ($V_{in} = 12V, V_{out} = 1.3V, I_{out} = 10A, P_{loss} = 2.85W$, Efficiency = 82%)

Figure 6.26: Loss Breakdown at 300Khz ($V_{in} = 12V, V_{out} = 1.3V, I_{out} = 10A, P_{loss} = 1.28W$, Efficiency = 91%)
Figure 6.27: Efficiency vs. Load Current ($V_{in} = 12V, V_{out} = 1.3V, f_{sw} = 1MHz$)
Chapter 7

Novel Bipolar-CMOS-DMOS (BCD) Processes

It is not simple to develop the monolithic processes through which various types of devices are fabricated on a substrate at the same time. All of three major design areas of electrical dimension (device/circuit engineering: electrical performances, performances degradation affection by other devices, thermal budget), mask dimension (layout engineering: mask design rule, tolerance, misalignment), and wafer dimension (process engineering: technology / facility availability and cost) need to be investigated to achieve one fully integrated BCD process shown in Fig.7.1.

In this chapter, the novel BCD fabrication process which is optimized for a high-current and fast-frequency converter is developed compatible to the conventional CMOS process with only one additional mask.

7.1 The developed BCD Fabrication Processes

In this proposed fabrication processes, a lot of parameters below are considered to fulfill the three major design area requirements above.

1) Electrical Requirements: Breakdown Voltage, on-resistance, FOM, capacitance, maximum current handling capability, thermal capability (thermal resistance or impedance),
Figure 7.1: Three major required design areas for monolithic fabrication process development.

switching transition, $dV/dt$ capability, $dI/dt$ capability, punch-through, threshold voltage, leakage current, latch-up, reliability (UIS: Unclamped Inductor Switch Energy, hot-carrier effect), oxide breakdown voltage, subthreshold slope, output resistance, saturation current, SOA, body-effect, DIBL (Drain Induced Barrier Lowering), GIDL (Gate Induced Drain Lowering), isolation, gain, transconductance, parasite effects and so on.

2) Process Requirements: Species, dose, temperature, time, gas, pressure, thickness, dopant, energy, tilt, rotation, mask, photo-resist selections, step coverage, material, polarity, under/over-etch, surface roughness, unwanted impurity and so on.

3) Layout Requirements: Alignment, tolerance, cross-talk, minimum feature size, consumed area, latch-up, inter-connection, parasite effects, isolation and so on.

And ~250 steps are proceeded including 12 mask levels, 15 film layers, 9 ion-implants and 15 high temperature processes. The major process conditions and cross-sections of devices are shown in Fig7.2, Fig7.3, Fig7.4, Fig7.5, and Fig7.6.

Based on this novel BCD process, high-current handling power switches, low voltage CMOS and BJT can be fabricated shown in Fig.4.1, Fig.5.1 and Fig.5.6 each.
1) Substrate: Low resistivity ($10^8$ Ohm cm) n$^{-}$<100> silicon substrate
2) P-body: (1) p-Epi. layer (Sum) or (2) n-Epi. layer and ion-implantation / drive-in (Sum)

<table>
<thead>
<tr>
<th>High-Side Switch</th>
<th>Low-Side Switch</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NPN BJT</th>
<th>PNP BJT</th>
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</tbody>
</table>

3) Thermally grown SiO$_2$(40nm) and deposited Si$_3$N$_4$(80nm)
4) Mask #1 (Active): Patterning and Etched Si$_3$N$_4$
5) Thermally grown FOX (Not shown here): T=30min, Temp=100°C and Stipped Si$_3$N$_4$

<table>
<thead>
<tr>
<th>High-Side Switch</th>
<th>Low-Side Switch</th>
<th>NMOS</th>
<th>PMOS</th>
<th>NPN BJT</th>
<th>PNP BJT</th>
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</table>

6) Mask #2 (N-WELL): Patterning
7) Phosphorous Ion-Implantation: Dose=$10^{15}$ cm$^{-2}$, Energy=400keV
8) N-WELL Drive-in: T=4hour, Temp=110°C

Figure 7.2: Proposed monolithic fabrication processes 1
Figure 7.3: Proposed monolithic fabrication processes 2(continued)
Figure 7.4: Proposed monolithic fabrication processes 3(continued)
24) Mask #8 (N+): Patterning
25) Phosphorus Ion-Implantation: Dose=4×10^16 cm^-2, Energy=50 keV, 

26) Deposited SiO₂ (1um) + Silicon Etching Hard Mask
27) Mask #9 (TRENCH): Patterning and Etched Hard Mask SiO₂ and Silicon(3.5um)
28) Phosphorus Ion-Implantation (Trench doping): Dose=4×10^16 cm^-2, Energy=50 keV, Tilt=7°C and 4-Rotation (0°, 90°, 180°, 270°)
29) RTA (Rapid Thermal Annealing): T=10sec., Tempe=1050°C (hold time)
30) Thermally Grown Oxide Liner (10um)
31) Deposited TEOS (40um): Filling the Trench
32) SiO₂-CMP
33) Mask #10 (CONTACT): Patterning and Etched SiO₂

Figure 7.5: Proposed monolithic fabrication processes (continued)
Figure 7.6: Proposed monolithic fabrication processes 5(continued)
In brief, the entire process is comprised of two major parts of normal CMOS processes and one additional trench process shown in Fig. 7.5. In the fabrication point of view, CMOS processes are already well matured technology which do not have major fabrication challenges but the additional trench step is not involved in the conventional process and should be verified intensively and experimentally in the following section.

7.2 Side-wall doped Trench Current Path

7.2.1 Trench Fabrication

When the trench is fabricated, there are three important considerations of surface roughness, thermal budget and tilt/rotation ion-implantation methodology. As it is shown in Fig. 7.5, the trench is fabricated at the end of the FEOL (Front End Of the Line) process. If this step asks high thermal budget process, other previous formed junctions would be affected.

The fabricated side-wall doped trench processes are shown in Fig. 7.7 and Fig. 7.8 in details. Unlike the previous similar structure [71] in which the current is flowing through the bulk silicon, the proposed switches current should flow through the etched-wall surface. And the surface roughness can increase the on-resistance directly.

Therefore, different silicon trench etching processes which affect surface roughness and process simplicity and thin screen oxide growing before the ion-implantation which affect the thermal budget are tested on several different wafers shown in the Table. 7.1.

Though it is known that Bosch etched trench has a scallop-shaped rough surface wall due to its process nature, it is fabricated and tested also because of its process simplicity. The 10nm thin $SiO_2$ is added as a screen oxide before the trench wall is ion-implanted to minimize the surface damage and channeling in two different methods of RTO (Rapid Thermal Oxidation) and dry thermal oxidation which causes moderate and high thermal budget each. However, no screen oxide grown trench has shown almost the same measured trench-resistance as others. This is because the tilt angle is large of $83^\circ$ ($=90^\circ - 7^\circ$ tilt for substrate surface) based on the vertical wall direction and the damage and channelling effect are negligible. Therefore, no screen oxidation is needed for trench ion-implantation and the thermal budget can be minimized not to jeopardize previous existing junctions. And the trench walls are supposed to be highly doped by the ion-implantation. The tilt angle
Table 7.1: Two major difference processes and number of tested wafers

<table>
<thead>
<tr>
<th>Etch Process</th>
<th>Process complexity</th>
<th>Oxidation Process</th>
<th>Thermal Budget</th>
<th># of wafers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bosch</td>
<td>simple</td>
<td>No Oxidation</td>
<td>no</td>
<td>1</td>
</tr>
<tr>
<td>Bosch</td>
<td>simple</td>
<td>Rapid Thermal Oxidation</td>
<td>moderate</td>
<td>1</td>
</tr>
<tr>
<td>Bosch</td>
<td>simple</td>
<td>Thermal Oxidation</td>
<td>high</td>
<td>2</td>
</tr>
<tr>
<td>Plasma Thermal</td>
<td>moderate</td>
<td>No Oxidation</td>
<td>no</td>
<td>1</td>
</tr>
<tr>
<td>Plasma Thermal</td>
<td>moderate</td>
<td>Rapid Thermal Oxidation</td>
<td>moderate</td>
<td>1</td>
</tr>
<tr>
<td>Plasma Thermal</td>
<td>moderate</td>
<td>Thermal Oxidation</td>
<td>high</td>
<td>2</td>
</tr>
<tr>
<td>Total # of wafers</td>
<td></td>
<td></td>
<td></td>
<td>8</td>
</tr>
</tbody>
</table>
ion-implantation makes it possible for each wall to be doped and rotated ion-implantations would dope all walls. Because the high channel density trench has rectangular shape in the top view and 4 current flowing path walls shown in Fig.4.13 and Fig.7.9 needed to be doped. However, only 2-rotations are done for the fabricated trench to make it simple to measure the trench resistance. The rapid thermal annealing(RTA) is done as an annealing process after the ion-implantation to reduce the thermal budget. Because this RTA makes $n^+$ NMOS source, NMOS drain and PMOS body dopants which are ion-implanted at 25) step in Fig.7.5 activated at the same time, the trench fabrication steps would not affect the conventional CMOS properties such as doping profile, junction depth, lateral diffusion and threshold voltage at all. Eventually, the trench-resistance is measured to verify all the processes validness.
Figure 7.8: The processes for fabricated side-wall doped trenches (continued)
Figure 7.9: Various shapes of etched trench in a buck-converter layout
7.2.2 Trench Characteristics

In the high channel density power MOSFET shown in Fig.4.12 (b), (d) and Fig.7.9, several types of sub-micron trenches such as rectangular, donut, circle and U-shape trenches exist. All these new types of doped silicon etched trenches and process design rules test patterns are fabricated shown in Fig.7.10 and those dimensions are summarized in Table.7.2.

The fabricated $n^+$-doped trench cross-sections captured by SEM (Scanning Electron Microscope) are shown in Fig.7.11. Each of plasma thermal (a) and bosch (b) etched trench has its own advantages and disadvantages. Firstly, while the trench width of (a) can be controlled accurately, one of (b) shows maximum 30% deviation from the target width.
Table 7.2: Process design rule test and Resistance measurement sites dimensions

<table>
<thead>
<tr>
<th>Process design rule test site</th>
<th>Resistance measurement site</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectangle, U-shape</td>
<td>Circle</td>
</tr>
<tr>
<td>Width(um)</td>
<td>0.8~2.2</td>
</tr>
<tr>
<td>Length(um)</td>
<td>5~35</td>
</tr>
<tr>
<td></td>
<td></td>
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</tbody>
</table>

due to the existing hill-valley height of the scallop walls. Secondly, while the depth of (a)
can be decided exactly by the initial target depth program, it is hard to control the depth of
(b). Because the depth of bosch etched trench depends on the ARDE(Aspect Ratio Depen-
dent Etch), whenever the width is changed, the depth should be checked. Unfortunately, it
is hard to check the depth without breaking the wafer which wastes the silicon wafer and
time. Thirdly, while the wall of (a) is anisotropic vertically smooth, one of (b) has scallops
due to the nature of bosch process. It causes not only the trench resistance to be increased
but also the reliability problems related to the trench filling. Lastly, while trenching and
side-wall inhibitor deposition happen for (a), (b) does not have this phenomena. However,
fortunately, these do not increase the trench resistance because the doping concentration at
the trench bottom is very high and even current is flowing vertically through the substrate
for both of high- and low-side power MOSFETs. Therefore, the plasm thermal etched trench
process is superior to the bosch one in the SEM experimental point of view. In addition,
the several important measured trench resistances are shown in Table.7.3 electrically. As
it is expected from the SEM test, the rough wall-surface shown (b) in Fig.7.11 shows twice
large resistance for the current is flowing through the surface instead of the bulk. And the
non-screen oxide trench (lowest thermal budget) has almost the same resistance as RTO
and Thermal Oxidation(not shown) ones due to the explained reasons above. Furthermore,
all the resistance values are well matched to the 2D/3D process simulated FLOOPS ISE-
TCAD simulation, also. Each of simulated and measured one shows 3.7mΩ · mm² and
3.8mΩ · mm² which is 12% of the total specific resistance for 3.8um-depth silicon trench.
Eventually, the only challengeable non-CMOS process step in the proposed BCD process
is proved by experiments as well as simulations and setup (hard mask, thermal budget, damage, tilt/rotation ion-implantation etc.).

### 7.2.3 Cost Effective Side-wall doped Trench Resistance Measurement Methodology

When the resistance is measured experimentally, contact, spreading and probe resistances as well as ohmic contact should be considered [72]. The metal is usually put on the probe pads to prevent any problems caused by all of these above. Though the metal sputtering process is a matured technology, the additionally required metal mask and steps can increase the fabrication cost which must be low enough especially for a prototype structure. If the metal lift-off technique is used, no extra mask is needed but accurate alignment and small tolerance control techniques are required. Therefore, only 1-mask required cost-effective side-wall doped trench resistance measurement methodology in which none metal processes are included is proposed here and verified by not only 2D/3D simulations but also by experiments. The top-view of rectangular trenches layout and dimensions are shown in Fig.7.12 (a). The black trenches are located periodically by 2W from the center of one trench to another. And the red and black lines represent the $n^+$
Table 7.3: Measured trench specific resistances and comparisons

<table>
<thead>
<tr>
<th>Etch Method</th>
<th>Screen</th>
<th>Trench Depth (μm):SEM</th>
<th>Measured $R_{trench}$ (mΩ·mm$^2$)</th>
<th>$R_{trench}$ Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plasma Thermal</td>
<td>None</td>
<td>3.5</td>
<td>3.42</td>
<td>1.0</td>
</tr>
<tr>
<td>Plasma Thermal</td>
<td>RTO</td>
<td>3.5</td>
<td>3.37</td>
<td>0.99</td>
</tr>
<tr>
<td>Bosch</td>
<td>None</td>
<td>3.5</td>
<td>7.09</td>
<td>2.07</td>
</tr>
</tbody>
</table>

doped wall by the ion-implantation and undoped wall each. The microscopic pictured sidewall doped rectangular trenches are shown in Fig.7.12 (b), also. Because the left and right trench walls are not ion-implanted due to the only 2-rotation (7°tilt) ion-implantations in the process explained before, the current can only flow through the red $n^+$-doped wall and the very large resistance for undoped walls can be ignored when two probes are put on $\alpha/\alpha'$ and $\beta/\beta'$ separately. The equivalent resistances of $R_{eq1}$ and $R_{eq2}$ can be modeled as the combinations of $R_T$ (lumped trench wall resistance) and $R_B$ (lumped other resistance) in each cell (AC and BC each). It should be noted that these are lumped resistances. In other words, it does not mean the current is only flowing through the marked resistances on the layout shown in Fig.7.12 (c). In conclusion, trench resistance can be measured by only measuring two $R_{eq1}$ and $R_{eq2}$ for large $W$ ($\frac{R_T}{R_B} << 1$) area verified below.

$$R_{eq1} = \frac{(2R_T + R_B)/(2R_T + 5R_B)}{(2R_T + R_B) \cdot (\frac{2R_T}{R_B} + 5)}$$

$$= \frac{10R_T + 5R_B}{6} \quad (for \quad \frac{R_T}{R_B} << 1) \quad (7.1)$$

$$R_{eq2} = \frac{(4R_T + 5R_B)/R_B}{(\frac{4R_T}{R_B} + 6)}$$

$$= \frac{(4R_T + 5R_B)}{6} \quad (for \quad \frac{R_T}{R_B} << 1) \quad (7.2)$$
Figure 7.12: Top-view and resistor models of fabricated rectangular trenches
Subtracting Equ. 7.2 from Equ. 7.1,

\[ R_{eq1} - R_{eq2} = \frac{(10R_T + 5R_B) - (4R_T + 5R_B)}{6} = R_T \quad (for \ R_T \frac{R_T}{R_B} << 1) \] (7.3)

The 2D, 3D simulated and measured structures and their resistances are shown in Fig.7.13. And all trench resistances are well-matched each other as \( W \) is increased as predicted in Equ.7.3. Eventually, simple and novel \( n^+ \)-doped trench wall resistance measurement methodology has been proposed and \( R_T \) has been successfully measured with only one mask without metal lift-off process at all which asks the alignment accuracy and extra cost.
Figure 7.13: 2D, 3D simulation and measurement $n^+$-doped Trench Resistance ($R_T$) and each structure for $W=50,100,200\mu m$
Chapter 8

Conclusions and Future Works

8.1 Conclusions

The novel fast frequency monolithic synchronous buck-converter which can handle the high operation current without suffering from the metal-debiasing effects is proposed for the first time. This is achieved owing to the new power MOSFET structures for both high- and low-side switches which have the vertical current flowing capability as SPDT switches. In other words, both control and synchronous power switches are integrated as vertical-type MOSFETs on the same substrate without affecting other peripheral devices. And the key characteristics of other essential integrated devices such as CMOS and BJTs as well as the power MOSFETs have been investigated extensively for monolithic SMPS (Switch Mode Power Supply) applications. In addition, the high-performance and reliability layout considerations for the entire buck-converter as well as for power switches are explained in details. And high-density, closed-cell monolithic layout is proposed, also. All of these show great performances (breakdown voltage, on-resistance, gate-charge, FOM, transconductance, output-resistance, saturation and leakage current, beta-gain and so on) compared to previous research and commercial products for high-frequency required voltage regulators. Especially, the vertical power MOSFET FOMs are smaller than reported state-of-art power MOSFETs ones. Therefore, these low FOMs and monolithic vertical integration (SOC) design reduce impacts of the parasitic components and total power losses. One of the most important and challengeable issue for a monolithic design is the operation reliability related to the isolations and parasitic devices. In this dissertation, the
conventional and new monolithic design challenges have been addressed and solutions are experimentally demonstrated. The unexpected parasitic effects by inherit diodes and BJTs due to the unique new structures can be prevented by the controlled CMOS p-body voltage strategy explained in the chapter 6. Based on all these simulations and experiments, novel cost-effective monolithic BCD fabrication process has been developed in details and the most challengeable side-wall doped trench fabrication process is setup experimentally. In addition, the easiest way to test it and the related equations are developed theoretically and experimentally. The designed monolithic buck-converter shows 82% high efficiency at 1Mhz switching frequency with 10A operating current. Eventually, all of these make it possible to achieve the high frequency and high current handling capability synchronous converters required for the next generation voltage regulator.

8.2 Further Research Directions

In this dissertation, the research has focused on the 30~50(V) voltage-rating, high current and high frequency buck converter design. And this lays the groundwork for a number of future works. Therefore, this technique can be extended to other research areas as the follows.

- Evaluation of different SMPS topologies: The buck converter is one of many popular switching converters. There are two other commonly used converters which perform different voltage conversion functions. One is the booster converter which steps the voltage up. The other is the buck-boost converter which can increase or decrease the magnitude of the voltage. Because the SPDT(Single Pole Double Throw) can be used for all of these converters, our proposed integrated power MOSFETs can be incorporated into these topologies, also.

- Evaluation of high voltage applications: More than 600(V) voltage-rating is required for some switch power supply applications shown in Fig.1.2 in the chapter 1. Though these applications ask several tens kilo-hertz switching frequency currently, it will be increased quickly as the more and more SOC technology is required [73]. 600(V) rating power MOSFETs which have low on-resistance may be developed based on our proposed structure. As the trench doping concentration is adjusted, the super-
junction (SJ) effects can be expected and total resistance will be small enough with higher breakdown voltages.

- Evaluation of system level design: The system level design is essential whenever the operation conditions are changed. However, the TCAD mixed-mode simulation which solves a lot of physical equations takes too long time to be used for this purpose. Therefore, the spice model extraction and modeling are needed which can be used in the circuit simulator such as H-spice, spectre or saber. With these parameters from our proposed power switches and other devices, the system level optimization can be done more accurately in a short simulation time.
Bibliography


