

## ABSTRACT

LEE, BONGMOOK. A Study of Group III Elements (La, Gd, Eu, and Al) Incorporation on Metal Gate / High- $k$  Stacks for Advanced CMOS Applications. (Under the direction of Dr. Veena Misra).

The goal of this research is to evaluate the effect of group III elements incorporation into advanced metal gate / high- $k$  dielectric stacks to achieve the desired gate stack work function without degrading electrical performance. The physical origins and possible mechanisms are provided in order to explain the experimental results. By incorporating group III elements into the gate stack, device  $V_{FB}/V_T$  can be modulated to the desired value for both NMOS (by using Rare Earth metals and oxide) and PMOS (by using an Al-based alloy) while maintaining key device properties. Based on these studies, an alternative route to achieve dual CMOS metal gate / high- $k$  dielectric stacks for the next generation technology is demonstrated and supported with encouraging experimental results.

The first part of this work focused on the impact of Rare-Earth metal incorporation on the effective work function of the gate stack by using Fully Silicided (FUSI) Gate approach. Rare-Earth metal incorporated Ni-FUSI gate on  $HfSiO_x$  dielectric provides 0.3~0.4 V of effective work function shift depending on composition and metal. It was found that the structural properties with Gadolinium (Gd) and Europium (Eu) incorporation into Nickel (Ni) Fully Silicided (FUSI) gate electrodes are markedly different and resulted in different degrees of effective work function modulation. It was also found that the incorporation of Gd and Eu metals into Ni-FUSI gate can remotely scavenge the interfacial oxide layer resulting in lower EOT of the device.

The second part of this work focused on the impact of Rare-Earth oxide capping on the electrical properties of NMOS devices. The presence of La atoms at high- $k$ /SiO<sub>2</sub> interface formed a dipole layer creating a band offset so that the effective work function of the gate stack is modulated toward NMOS band edge. It was found that the La concentration at high- $k$ /SiO<sub>2</sub> interface is the key factor for the  $V_{FB}$  modulation whereas the host high- $k$  materials and gate electrode on  $V_{FB}$  shift have a minimal impact. In reliability, the incorporation of La<sub>2</sub>O<sub>3</sub> can enhance both breakdown and PBTI characteristics since the La-induced dipole layer can effectively increase barrier height for electron injection as well as passivate some level of bulk defects in the HfO<sub>2</sub> layer.

The last part of this work addressed the impact of Al-based dielectric capping approach for PMOS devices. The addition of Ta in AlTaO<sub>x</sub> structure produces charges resulting in desired  $V_T$  for PMOS devices as well as retarding Al diffusion through the HfO<sub>2</sub> layer preventing Al-caused mobility degradation. Furthermore, the reliability characteristics such as breakdown and negative bias temperature instability (NBTI) were studied. The incorporation of an AlTaO capping layer improves device reliability characteristics by suppressing the hydrogen release as well as trap generation during the negative bias stress.

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A Study of Group III Elements (La, Gd, Eu, and Al) Incorporation on Metal Gate / High-*k*  
Stacks for Advanced CMOS Applications

by  
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## **DEDICATION**

**To my parents**

*Jung-Oh Lee*

*Ok-Hee Kim*

**and my wife**

*Hyeseon Youm*

## **BIOGRAPHY**

Bongmook Lee received Bachelor of Science in Electronic Materials Engineering from Kwangwoon University (Seoul, South Korea) in 2002. He obtained Master of Science degree in Electrical Engineering from North Carolina State University in 2005 and continued to work towards Ph. D degree in the area of developments of metal gate / high-k dielectric stack for advanced CMOS devices gate stack. During his doctoral study he has been the recipient of the Student Travel Grant at Electrochemical Society meeting in 2008 and Applied Materials Inc. fellowship since 2007.

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## TABLE OF CONTENTS

LIST OF TABLES .....	viii
LIST OF FIGURES .....	ix
Chapter 1 <i>Introduction</i> .....	1
1.1 Historic Evolution and CMOS technology scaling.....	1
1.2 High-k Gate Dielectrics.....	3
1.3 Metal Gate Electrodes.....	7
1.4 Property of Group III Elements .....	12
1.5 Objectives .....	13
1.6 Overview of dissertation .....	13
Chapter 2 <i>Experimental Description and Characterization Methodology</i> .....	16
2.1 Deposition techniques for advanced gate stack .....	16
2.1.1 Atomic Layer Deposition.....	16
2.1.2 Molecular Beam Deposition (MBE).....	21
2.1.3 RF-sputtering for gate electrode .....	22
2.2 Process flow .....	23
2.3 Electrical Characterization Methodology .....	26
2.3.1 Two Terminal Electrical Characterization.....	27
2.3.2 Four Terminal Basic Electrical Characterization.....	34
2.3.3 Four Terminal Advanced Electrical Characterization .....	39
2.4 Analytical Characterization .....	55
2.4.1 X-Ray Photoelectron Spectroscopy (XPS) .....	55
2.4.2 X-Ray Diffraction (XRD) Analysis .....	57
2.4.3 Backside SIMS.....	57
2.4.4 Transmission Electron Microscopy (TEM) .....	58
2.5 Summary .....	60

Chapter 3 <i>The role of Rare Earth Metal (RE=Gadolinium and Europium) on Effective Work function modulation of Ni-FUSI / High-k dielectric stacks</i> .....	61
Abstract .....	61
3.1 Introduction .....	62
3.2 Experiments .....	63
3.3 Results and Discussion .....	65
3.3.1 Impact of Gd incorporation on effective work function .....	65
3.3.2 Impact of Eu incorporation on Effective work function .....	75
3.3.4 Mechanism for Gd and Eu incorporation into Ni-FUSI .....	82
3.4 Summary .....	87
 Chapter 4 <i>Investigation of the origin of <math>V_T/V_{FB}</math> modulation by <math>La_2O_3</math> capping layer approaches for NMOS application</i> .....	88
4.1 Introduction .....	88
4.2 Experiments .....	89
4.3 Literature Review of proposed mechanism on $V_T/V_{FB}$ modulation by Rare-Earth capping Incorporation .....	90
4.4 Results and Discussion .....	93
4.4.1 Effect of host high- $k$ dielectrics on $V_{FB}$ (aliovalent substitution) .....	93
4.4.2 Effect of $La_2O_3$ location on $V_{FB}$ shift (Dipole and charge) .....	101
4.4.3 Transistor Results .....	110
4.5 Summary .....	130
 Chapter 5 <i>Impact of <math>AlTaO</math> capping layer on device performance and reliability for PMOS application</i> .....	131
5.1 Introduction .....	131
5.2 Experiments .....	132
5.3 Results and discussion .....	134
5.3.1 C-V Result of capping layer with W gate electrode .....	134

5.3.2 Material Analysis .....	136
5.3.3 Dielectric-gate reaction (TaN gate electrode).....	141
5.3.4 Electrical Characterization of Al-based capping MOSFET.....	147
5.4 Summary .....	170
 Chapter 6 <i>Conclusion and Future Outlook</i> .....	 171
6.1 Conclusion .....	171
6.2 Future Outlook .....	174
 References .....	 176
 Appendix .....	 193
Appendix: MOSFET Fabrication Process (4 level GEM Masks).....	194

## LIST OF TABLES

Table 1.1	Key factors for high performance application (MPU) and low power application (cell phone) device from ITRS 2007 [8].....	3
Table 1.2	Dielectric Properties of HfO <sub>2</sub> and SiO <sub>2</sub> .....	7
Table 2.1	Summary of deposition condition for ALD Al <sub>2</sub> O <sub>3</sub> and HfO <sub>2</sub> process.....	20
Table 2.2	Self-align MOSFET process.....	25
Table 3.1	Summary of effective work function and EOT.....	72
Table 3.2	Summary of effective work function and EOT.....	80
Table 4.1	Key parameters extracted from C–V and I–V measurements.....	114
Table 4.2	Summary of mobility value and interface state density.....	116
Table 5.1	Key parameters extracted from C–V and I–V measurements.....	151
Table 5.2	Summary of peak mobility and high field (E <sub>eff</sub> =0.9MV/cm) mobility.	156

## LIST OF FIGURES

Figure 1.1	Number of Transistors and cost per transistor in Intel processors over generations (reproduced from Intel website).....	2
Figure 1.2.	Gate leakage current for various thickness of SiO <sub>2</sub> dielectric. Leakage current increases exponentially due to the direct tunneling [10].....	4
Figure 1.3	Relation between bandgap and dielectric constant for various high <i>k</i> dielectric materials. Data were taken from [14].....	6
Figure 1.4	(a) Fermi level pinning of n <sup>+</sup> and p <sup>+</sup> poly-silicon gate on HfO <sub>2</sub> dielectric after C. Hobbs [27] and (b) effective mobility degradation of poly-silicon/high- <i>k</i> dielectric stack after R. Chau [29]. The inset of (b) shows the effect of scattering on HfO <sub>2</sub> dielectric.....	9
Figure 1.5	Candidate elemental metals for NMOS and PMOS devices based on vacuum work function.....	11
Figure 1.6	Schematic representation for proposed Approaches.....	14
Figure 2.1	Typical ALD Al <sub>2</sub> O <sub>3</sub> process illustrations from Cambridge Nanotech ( <a href="http://www.cambridenanotech.com">www.cambridenanotech.com</a> ), (a) TMA pulse, (b) un-reacted TMA precursor and byproduct are purged out, (c) H <sub>2</sub> O precursor is pulsed to create O-H terminated surface followed by purging process of reaction product and (d) as a result one layer of desired film is deposited. After two sequential pulse and purge cycle's one monolayer of desired film is deposited. With our system the deposition rate is ~ 1.1 Å/cycle.....	17
Figure 2.2	Illustration of ALD acceptable temperature ranges.....	18
Figure 2.3	Schematic of ALD system used for HfO <sub>2</sub> and Al <sub>2</sub> O <sub>3</sub> deposition.....	19
Figure 2.4	(a) Schematic and (b) photograph of MBE system used for La <sub>2</sub> O <sub>3</sub> and TaO <sub>x</sub> deposition [45].....	21
Figure 2.5	Schematic illustration of UHV-PVD (RF-magnetron sputtering) system.....	23
Figure 2.6	Schematic of typical MOSFET process steps (a) active, (b) gate stack formation, (c) source/drain implant, and (d) contact pad with isolation oxide layers.....	24
Figure 2.7	(a) Typical low and high frequency C–V curves and (b) equivalent circuit of the MOS capacitor structure.....	28
Figure 2.8	V <sub>FB</sub> vs. EOT plot extracted from C–V. Y-intercept represents φ <sub>MS</sub> and the slope is related to the fixed charge. Since φ <sub>S</sub> is known, the effective work function can be determined from the φ <sub>MS</sub> .....	30
Figure 2.9	Band diagram of (a) Fowler–Nordheim (FN) Tunneling process and (b) Direct Tunneling (DT) process through gate dielectric.....	33

Figure 2.10	Typical FN plot of metal gate / SiO <sub>2</sub> stack taken from J <sub>g</sub> -V <sub>g</sub> curve. Linear behavior confirms the current conduction is dominated by FN tunneling. The slope is related to the barrier height.....	34
Figure 2.11	Threshold voltage determination by the linear extrapolation technique. NMOSFET with V <sub>ds</sub> = 50mV, EOT = 2.2 nm and W/L = 50um/10um.....	36
Figure 2.12	Method to determine subthreshold swing from log (I <sub>ds</sub> )-V <sub>gs</sub> curve.....	38
Figure 2.13	Universal mobility characteristics vs. effective field showing the impact of coulomb, phonon, and surface roughness scattering.....	40
Figure 2.14	Extrinsic mobility degradation mechanisms for poly-si/high- <i>k</i> stack	41
Figure 2.15	Measurement setups of Split C-V technique for (a) gate-to-channel capacitance (C <sub>gc</sub> ), (b) Gate-to-bulk capacitance (C <sub>gb</sub> ), (c) examples of measured C <sub>gc</sub> and extracted Q <sub>inv</sub> , and (d) example of C <sub>gb</sub> measurement.....	44
Figure 2.16	I <sub>ds</sub> -V <sub>gs</sub> characteristics with measured and leakage current corrected curve.....	45
Figure 2.17	Schematic illustration of charge pumping method for (a) fixed amplitude with base level sweep charge pumping, (b) fixed base level with various amplitude sweep, (c) typical base level charge pumping curve, and (d) various amplitude charge pumping curve with SiO <sub>2</sub> and HfO <sub>2</sub> dielectrics.....	48
Figure 2.18	Schematic of Si/SiO <sub>2</sub> interface after FGA. Si dangling bonds created by the mismatch between crystalline Si and amorphous oxide are passivated by hydrogen.....	50
Figure 2.19	Schematic of time evolution of the R-D model. Regions (i) generation limited, (ii) dynamic equilibrium, (iii) diffusion limited, and (iv) saturation after [85]. Typical NBTI time evolution follows power law in region (iii).....	52
Figure 2.20	Measurement setup for NBTI test.....	54
Figure 2.21	Schematic of photoelectron emission process and XPS measurement setup taken from [56].....	56
Figure 3.1	Vacuum work function values for Rare-Earth Metals. It also indicates the valency of the metals. Eu and Yb are divalent metals and hence show the lowest work function.....	63
Figure 3.2	Flatband (V <sub>FB</sub> ) voltage versus EOT plot for 500Å W/300Å Ni <sub>1-x</sub> Gd <sub>x</sub> /300Å Si on HfSiO <sub>x</sub> /SiO <sub>2</sub> dielectrics (x varies from 0 to 30) after 450 °C RTA annealing.....	65
Figure 3.3	(a) C- V curve with frequencies for NiSi and 30% Gd incorporated NiSi. V <sub>FB</sub> modulation is clearly obtained with Gd incorporation with similar level of D <sub>it</sub> response. (b) Variation of accumulation capacitance for 400 °C and 450 °C silicidation annealing. Larger variation in C <sub>acc</sub> indicates incomplete silicidation of Si. Un-doped Si	

	layer act like semi-insulating material resulting in dependence in applying frequency, and (b) C–V curves with frequencies.....	66
Figure 3.4	EOT vs. physical thickness of HfSiO <sub>x</sub> dielectric for NiSi control and 30% Gd incorporated NiSi gate. Y-intercept corresponds to the interfacial layer thickness and the slope is related to the charge profile. Interfacial layer is decreased with Gd presence whereas the slope is stayed.....	67
Figure 3.5	High resolution cross-sectional TEM images of (a) Control Ni-FUSI on HfSiO <sub>x</sub> gate stack and (b) 30% Gd incorporated FUSI gate stacks after 450°C 1min RTA. Both low- <i>k</i> interfacial layer and high- <i>k</i> layer is reduced for Gd incorporated FUSI sample.....	69
Figure 3.6	Backside SIMS for Ni <sub>70</sub> Gd <sub>30</sub> / Si gate stack on HfSiO <sub>x</sub> gate dielectric after 450°C 1min annealing, measured with O <sub>2</sub> <sup>+</sup> beam. No indication of Gadolinium diffusion into the dielectric was observed.....	70
Figure 3.7	Leakage current for NiSi and Gd incorporated NiSi. Higher leakage with 30% Gd incorporation indicates the decomposition of oxide by Gd.....	71
Figure 3.8	Extracted effective work function and EOT as a function of Gd percentage in Ni layer from V <sub>FB</sub> vs. EOT plot.....	72
Figure 3.9	XRD patterns of NiSi and Gd incorporated NiSi gate electrodes for 10 to 30 percent Gd after one step silicidation annealing at 450°C for 1min. As percentage of Gd increases the peak intensity is reduced and broadened.....	73
Figure 3.10	AES depth profile for (a) NiSi and (b) 30% Gd incorporated NiSi.....	74
Figure 3.11	V <sub>FB</sub> vs. EOT with NiSi, 10% Eu incorporated Ni-FUSI, and 30% Eu incorporated Ni-FUSI after 450 °C 1min silicidation annealing in Ar ambient.....	76
Figure 3.12	Frequency dispersion of 30% Eu incorporated Ni FUSI. Minimal dispersion the accumulation region confirmed full silicidation.....	77
Figure 3.13	J <sub>G</sub> at 1V beyond flatband with NiSi, 10% Eu incorporated Ni FUSI, and 30% Eu incorporated Ni-FUSI gate. 2 order of magnitude reduction in leakage current with 30% Eu incorporated Ni-FUSI was observed.....	78
Figure 3.14	EOT vs. physical thickness of dielectric. Clearly shows reduction of interfacial layer with Eu incorporation. But the slope did not change indicating charge profile is similar.....	79
Figure 3.15	Effective work function and EOT as a function of Eu percentage of Ni-FUSI gate extracted from V <sub>FB</sub> vs. EOT plot.....	80
Figure 3.16	AES depth profile for 30% Eu incorporated Ni FUSI after 450 °C 1min silicidation annealing. Similar structure to NiSi near the high – <i>k</i> layer was observed.....	81
Figure 3.17	Baskside SIMS with 30% Eu incorporated Ni-FUSI after 450 °C 1min silicidation annealing. Pile-up at FUSI/high- <i>k</i> interface was	

	clearly observed.....	82
Figure 3.18	Comparison of Gd and Eu incorporation into Ni-FUSI for (a) Effective work function as a function of RE percentage in Ni and (b) corresponding EOT and leakage values.....	83
Figure 3.19	Binary Phase Diagram for (a) Ni-Gd alloy and (b) Ni-Eu alloy.....	84
Figure 3.20	Schematic illustration of Gd and Eu incorporation into Ni-FUSI gate. (a) NiSi control gate, (b) 30% Gd incorporated Ni-FUSI, and (c) 30% Eu incorporated Ni-FUSI. The incorporation of Gd and Eu can change NiSi structure.....	86
Figure 4.1	Process flows for gate first self-align nMOSFET process and schematic of dielectric stacks used in this study.....	90
Figure 4.2	C–V curves with and without La <sub>2</sub> O <sub>3</sub> capping on Al <sub>2</sub> O <sub>3</sub> dielectrics. Larger V <sub>FB</sub> shift was obtained after 1065 °C annealing.....	92
Figure 4.3	C–V curves with and without La <sub>2</sub> O <sub>3</sub> capping on Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectric after 1065 °C annealing. Negative shift in V <sub>FB</sub> is also observed but the degree of shift is less than capping on Al <sub>2</sub> O <sub>3</sub> dielectric.....	94
Figure 4.4	ΔV <sub>FB</sub> shifts as a function of temperature with La <sub>2</sub> O <sub>3</sub> incorporation on Al <sub>2</sub> O <sub>3</sub> and Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectrics. Amount of shift depends on temperature and 600mV of V <sub>FB</sub> was modulated with Al <sub>2</sub> O <sub>3</sub> dielectric after 1065 °C annealing.....	95
Figure 4.5	Extracted EOT and J <sub>G</sub> at V <sub>G</sub> -V <sub>FB</sub> =1V for Al <sub>2</sub> O <sub>3</sub> and La <sub>2</sub> O <sub>3</sub> /Al <sub>2</sub> O <sub>3</sub> dielectric. Low EOT and leakage value were obtained with La <sub>2</sub> O <sub>3</sub> addition due to the higher <i>k</i> layer formation.....	96
Figure 4.6	Si 2s XPS spectra with and without La <sub>2</sub> O <sub>3</sub> layer on Al <sub>2</sub> O <sub>3</sub> dielectric. The peak at near 152eV is observed with La <sub>2</sub> O <sub>3</sub> capping layer and increased after 900 °C annealing indicating presence of silicate formation.....	97
Figure 4.7	Corresponding (a) La 3d and (b) Al 2p spectra on Al <sub>2</sub> O <sub>3</sub> dielectric with two different angles. La-silicate formation was confirmed after 900 °C annealing.....	98
Figure 4.8	Si 2s XPS spectra with and without La <sub>2</sub> O <sub>3</sub> layer on Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectric. Similar result was obtained with Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectric with La <sub>2</sub> O <sub>3</sub> incorporation.....	99
Figure 4.9	Corresponding La 3d and Hf 4f spectra on Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectric with two different take off angles. La-silicate formation was confirmed after 900 °C annealing but the La 3d peak position with Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> is lower than with Al <sub>2</sub> O <sub>3</sub> dielectric. This less silicate formation can explain the less V <sub>FB</sub> shift on Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> stack in Figure 4.3.....	101
Figure 4.10	(a) C–V characteristics and (b) extracted V <sub>FB</sub> and hysteresis (ΔV <sub>FB</sub> ) over temperature for TaN/La <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>2</sub> /Si capacitor (Latop).....	102

Figure 4.11	(a) C–V characteristics and (b) extracted $V_{FB}$ and hysteresis ( $\Delta V_{FB}$ ) over temperature for TaN/HfO <sub>2</sub> /La <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub> /Si capacitor (Labot).....	104
Figure 4.12	Comparison of samples for (a) extracted $V_{FB}$ vs. temperature and (b) EOT vs. temperature. It is confirmed that the presence of La shifted $V_{FB}$ of the gate stack.....	105
Figure 4.13	Normalized Si 2s XPS spectra after low (500°C) and high temperature (1000°C) annealing for (a) TaN/La <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>2</sub> /Si capacitor and (b) TaN/HfO <sub>2</sub> /La <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub> /Si capacitor. The location of La <sub>2</sub> O <sub>3</sub> layer can significantly change interface SiO <sub>2</sub> layer.....	107
Figure 4.14	XPS spectra of La 3d. It clearly indicates La diffusion through HfO <sub>2</sub> after 1000°C.....	108
Figure 4.15	Schematic representations of dielectric stack with (a) La <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>2</sub> stack and (b) HfO <sub>2</sub> /La <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub> stack with temperature.....	110
Figure 4.16	Capacitance–Voltage Curves for transistors.....	111
Figure 4.17	(a) Linear $I_{ds}$ – $V_{gs}$ curve and (b) log ( $I_{ds}$ )– $V_{gs}$ curve for transistors. $V_T$ is shifted with La <sub>2</sub> O <sub>3</sub> insertion from HfO <sub>2</sub> as expected and large shift in $V_T$ is obtained when La <sub>2</sub> O <sub>3</sub> is placed between HfO <sub>2</sub> and SiO <sub>2</sub> layer. Plot (c) is corresponding transconductance.....	112
Figure 4.18	$I_{ds}$ – $V_{ds}$ characteristics with $V_{gs}$ – $V_T$ =1V and 2V.....	114
Figure 4.19	Effective mobility of transistors at room temperature (25°C).....	115
Figure 4.20	Base level charge pumping results.....	116
Figure 4.21	Coulomb components of Mobility extracted from Matthiesen’s rule for different $N_{it}$ ’s. Charge pumping result shows similar level of $N_{it}$ values.....	118
Figure 4.22	Effective mobility vs. temperatures for nMOSFET device with various dielectrics. Least temperature dependency with TaN/La <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>2</sub> /Si stack due to the larger interface state.....	119
Figure 4.23	Peak mobility comparisons over temperature. TaN/La <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> stack shows less dependency of mobility in temperature suggesting that the mobility degradation mechanism is different from other samples.	120
Figure 4.24	Mobility sensitivity factor. TaN/HfO <sub>2</sub> /La <sub>2</sub> O <sub>3</sub> gate stack shows higher sensitivity.....	121
Figure 4.25	High-resolution TEM (HRTEM) and z-contrast STEM images for TaN/HfO <sub>2</sub> /SiO <sub>2</sub> , TaN/HfO <sub>2</sub> /La <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub> , and TaN/La <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>2</sub> samples after 1000°C annealing. The incorporation of La in the gate dielectric causes rough and thin interfacial layer.....	122
Figure 4.26	Gate Leakage characteristics of MOSFET devices for substrate injection. Presence of La in SiO <sub>2</sub> can create band offset resulting in retardation of electron tunneling [136].....	124
Figure 4.27	XRD of the samples after 1000°C annealing. Incorporation of La retards crystallization of HfO <sub>2</sub> .....	125

Figure 4.28	Weibull distribution plots for breakdown field. TaN/HfO <sub>2</sub> /La <sub>2</sub> O <sub>3</sub> gate stack provides tight and dense distribution.....	126
Figure 4.29	I <sub>ds</sub> and g <sub>m</sub> variation over time.....	127
Figure 4.30	N <sub>it</sub> variations over time measured by charge pumping.....	128
Figure 4.31	Positive Bias Temperature Instability (PBTI) results for two different stress fields at 125°C. Similar V <sub>T</sub> shift behavior with and without capping indicating the incorporation of La <sub>2</sub> O <sub>3</sub> layer does not degrade dielectric quality.....	129
Figure 5.1	Process flows for gate first self-align pMOSFET process and schematics of dielectric stack used in this study.....	133
Figure 5.2	C–V characteristic of W/Al <sub>2</sub> O <sub>3</sub> /SiO <sub>x</sub> /Si capacitors with and without TaO capping layer after low and high temperature annealing. The incorporation of TaO capping can modulate device V <sub>FB</sub> toward positive direction.....	135
Figure 5.3	C–V characteristic of W/Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>x</sub> /Si capacitors with and without TaO capping layer. The incorporation of TaO capping can also modulate device V <sub>FB</sub> with Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectric.....	136
Figure 5.4	XPS for Si 2s, O 1s spectra for Al <sub>2</sub> O <sub>3</sub> after 900 °C, TaO/Al <sub>2</sub> O <sub>3</sub> after 400 °C, and TaO/Al <sub>2</sub> O <sub>3</sub> after 900 °C annealing.....	137
Figure 5.5	XPS for Ta 4f and Al 2p on Al <sub>2</sub> O <sub>3</sub> and TaO/Al <sub>2</sub> O <sub>3</sub> dielectric with two different take off angles (60° and 90°). Minimal structural change is observed at a given temperature range.....	138
Figure 5.6	AR-XPS spectra for Si 2p, O1s, Ta 4p, and Hf 4f with 90° take-off angle. Small degree of intermixing between dielectrics was observed after 900°C.....	139
Figure 5.7	Backside SIMS depth profiles for TaN/Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>2</sub> /Si stack after 950°C 10s annealing. Most of Al stays on top of the HfO <sub>2</sub> dielectric.....	141
Figure 5.8	C –V plots for TaN/Al <sub>2</sub> O <sub>3</sub> /SiO <sub>x</sub> /Si capacitor, W/Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>x</sub> /Si capacitor, and W/TaO/Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>x</sub> /Si capacitor after 900°C anneal. The presence of Ta enhances V <sub>FB</sub> due to the Ta (gate) and AlO (dielectric) reaction at the top of the interface.....	142
Figure 5.9	V <sub>FB</sub> vs. temperature for Al <sub>2</sub> O <sub>3</sub> and Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectrics with TaN gate electrode. V <sub>FB</sub> is modulated towards positive direction as temperature indicating more reaction between TaO-Al <sub>2</sub> O <sub>3</sub> and/or presence of Al at the bottom interface.....	143
Figure 5.10	Summary of V <sub>FB</sub> for various dielectrics (a) with W gate electrode after 900°C and (b) with TaN gate electrode after 900°C. 200mV shift was obtained with TaO layer between Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> dielectric and W gate electrode. However, same 200mV shift in V <sub>FB</sub> was obtained with TaN/Al <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> stack confirming Ta and Al <sub>2</sub> O <sub>3</sub> reaction is the main responsible mechanism for additional V <sub>FB</sub> shift...	144

Figure 5.11	Proposed models to explain the $V_{FB}$ shift mechanism caused by AlTaO capping on a) $HfO_2$ dielectrics and b) $Al_2O_3$ dielectrics. The TaO-AlO reaction creates Ta d states in $Al_2O_3$ matrix (electron traps) resulting in enhancement of $V_{FB}$ . $Al_2O_3$ dielectric shows larger $V_{FB}$ modulation due the $Al_2O_3/SiO_x$ interface dipole effect.....	146
Figure 5.12	C-V curves for pMOSFET with various dielectric stacks. The addition of $Al_2O_3$ or TaO can modulate device threshold voltage.....	148
Figure 5.13	Extracted $V_{FB}$ as a function of Ta composition in $Al_{1-x}Ta_xO$ layer. $V_{FB}$ starts to decrease when Ta composition in $Al_{1-x}Ta_xO$ is more than 60%.....	149
Figure 5.14	Linear $I_{ds}-V_{gs}$ and corresponding transconductance for (a) $HfO_2$ based dielectrics and (b) $Al_2O_3$ based dielectrics.....	150
Figure 5.15	$V_T$ distributions with $HfO_2$ , TaO/ $Al_2O_3$ / $HfO_2$ , and $Al_2O_3$ / $HfO_2$ dielectrics.....	151
Figure 5.16	$I_{ds}-V_{ds}$ curves for two different overdrive voltage, $V_{gs}-V_T$ , (-1V and -2V). Higher drive current is obtained with $Al_2O_3$ / $HfO_2$ dielectric.....	152
Figure 5.17	$J_G$ characteristics for both gate and substrate injection. Incorporation of capping does not degrade dielectric property.....	153
Figure 5.18	Effective mobility curves extracted from split C-V method for (a) $HfO_2$ based dielectric and (b) $Al_2O_3$ based dielectrics.....	155
Figure 5.19	Base level sweep charge pumping data for (a) $HfO_2$ based dielectric and (b) $Al_2O_3$ based dielectric. Measured $N_{it}$ corresponds to the mobility data.....	158
Figure 5.20	Amplitude sweep charge pumping results with various charging times. TaN/ $HfO_2$ stack shows more dependence on frequency than $Al_2O_3$ / $HfO_2$ .....	159
Figure 5.21	$N_{CP}$ vs. charging time for $HfO_2$ based dielectric. $Al_2O_3$ / $HfO_2$ stack shows less dependence on charging time indicating less bulk traps near the interface than $HfO_2$ stack.....	160
Figure 5.22	Stress and sense measurement setup for the NBTI testing. During stress cycle voltage is applied to the gate while source, drain, and body are connected to the ground. During the sense cycle, typical $I_{ds}-V_{gs}$ and charge pumping are sensed. Stress and sense cycle are controlled through the switching matrix with Keithley 4200 system...	161
Figure 5.23	$I_{ds} - V_{gs}$ results as a function of stress time at 125 °C for TaN/ $HfO_2$ gate stack. Large $V_T$ shift as well as drain current reduction is obtained.....	162
Figure 5.24	$V_T$ shifts over time evolution with TaN/ $HfO_2$ stack in (a) linear and (b) log time scale. Most of $V_T$ shifts occur at the beginning of stress time indicating typical NBTI degradation behavior. The power law fitted time exponent is similar to $SiO_2$ .....	163
Figure 5.25	$V_T$ vs. $E_{ox}$ with TaN/ $HfO_2$ stack. $V_T$ shifts obey power law with exponent $\sim 3$ .....	164

Figure 5.26	(a) $\Delta V_T$ shifts over time and (b) corresponding $G_m$ degradation with two different stress conditions at 125 °C.....	165
Figure 5.27	(a) $N_{it}$ generation over time from the charge pumping measurement and (b) Subthreshold swing degradation over time. Higher generation rate was observed with $HfO_2$ dielectric.....	167
Figure 5.28	10 year lifetime projection for $HfO_2$ based dielectric. $Al_2O_3/HfO_2$ dielectric shows better lifetime.....	169

# Chapter 1

## Introduction

### 1.1 Historic Evolution and CMOS technology scaling

Metal-oxide-semiconductor field effect transistors (MOSFETs) have been used as a basic structure of integrated circuits for more than four decades in the semiconductor industry. The basic concept of field effect transistor was initially proposed in 1930's by J. E. Lilienfeld [1-2]. However, the practical and reliable MOSFET device was demonstrated almost 30 years later based on Si substrate with SiO<sub>2</sub> dielectric by D. Kahng and M. Attala [3-4], and has since become the most important electronic component in integrated circuits. In 1965, G. Moore predicted the future of semiconductor technology, which is now popularly called Moore's Law [5]. This implies that the transistor density per area is doubled every two years, leading to device performance improvement with lower cost per function, increased chip functionality, and hence business financials through die size reduction as illustrated in Fig. 1.1. The physical device dimension has been scaled down from ~ 10  $\mu\text{m}$  in 1960's to below 100 nm in 2000's. The gate dielectric thickness and operating voltage have also been reduced in order to keep improving device electrical characteristics. However, as gate length of the transistor is scaled down below the sub-micron regime, the electric field from the source/drain junctions affects the channel resulting in degradation of transistor

electrical performance. One way to overcome this issue is to increase the gate to channel capacitance by reducing the gate oxide thickness.

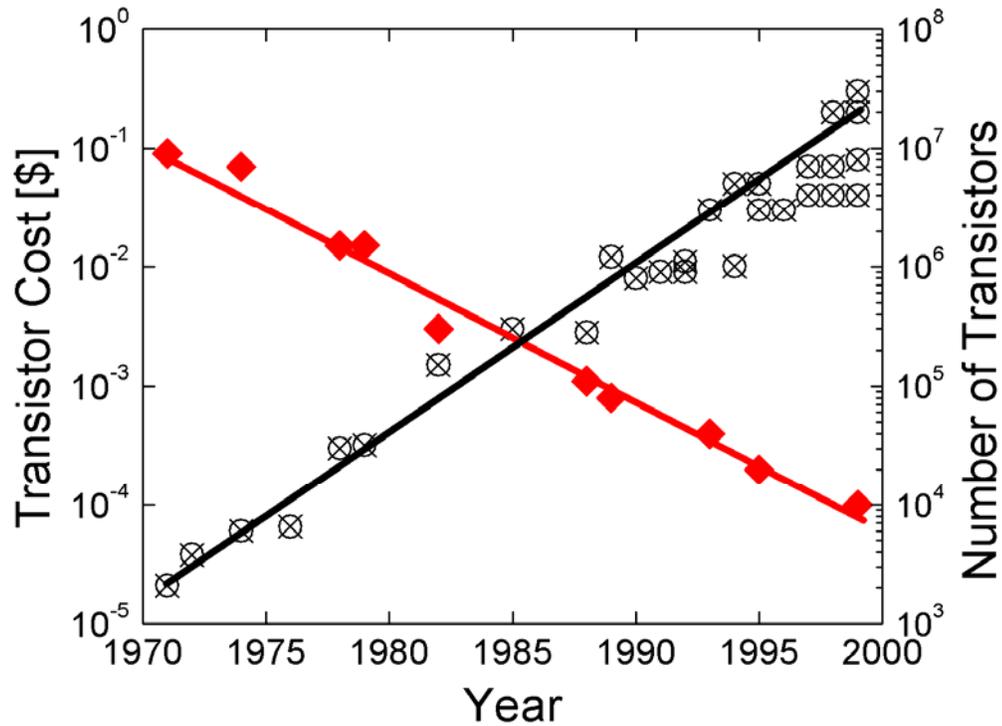


Figure 1.1 Number of Transistors and cost per transistor in Intel processors over generations (reproduced from Intel website)

However, scaling of conventional SiO<sub>2</sub> gate dielectrics for the sub-micron regime causes severe problems. Since the full bandgap of SiO<sub>2</sub> on Si can be realized only if at least two-monolayers of SiO<sub>2</sub> are present, SiO<sub>2</sub> gate dielectrics can not be scaled down below 1 nm. Even though transistors with 1.3~1.5 nm thick gate oxides are still candidates for high performance applications, their high gate leakage current density (1-10A/cm<sup>2</sup>) may not be suitable for low power applications [6-7]. Also, transistors with gate dielectrics thinner than

1.2 nm do not exhibit any improvement in drive current [8-9]. High gate tunneling currents is thus a major problem for the scaled CMOS devices. As the oxide thickness is scaled down, the direct tunneling of gate-to-channel leakage for SiO<sub>2</sub> increases exponentially [10]. Figure 1.2 shows measured gate oxide tunneling currents for oxide thicknesses varying from 3.5 nm to 1.4 nm over a voltage range where direct tunneling dominates.

Table 1.1 Key factors for high performance application (MPU) and low power application (cell phone) device from ITRS 2007 [8]

		<b>2007</b>	<b>2008</b>	<b>2009</b>	<b>2010</b>	<b>2011</b>	<b>2012</b>
<b>Technology (nm)</b>		65	57	50	45	40	36
<b>EOT (nm)</b>	<b>HP</b>	<b>1.2</b>	<b>0.9</b>	<b>0.75</b>	<b>0.65</b>	<b>0.55</b>	<b>0.5</b>
	<b>LSTP</b>	1.9	1.6	1.5	1.4	1.3	1.2
<b>V<sub>dd</sub> (HP)</b>		1.1	1.0	1.0	1.0	0.95	0.9
<b>Gate Leakage (A/cm<sup>2</sup>)</b>	<b>HP</b>	80	87	100	110	130	140
	<b>LOP</b>	0.067	0.081	0.094	0.11	0.12	0.13

## 1.2 High-*k* Gate Dielectrics

As mentioned earlier silicon dioxide (SiO<sub>2</sub>) has been used as a gate dielectric for VLSI applications for more than 40 years. There are some primary reasons for this success including 1) passivation of the Si surface with low surface state density ( $\sim 1-3 \times 10^{10}$  (eV-cm<sup>2</sup>)<sup>-1</sup>), 2) presence of a large insulator band gap ( $\sim 9$  eV) and 3) very few bulk traps. In order

to achieve high transistor performances such as fast circuit speed, reduced power and increased packing density, the gate oxide thickness must undergo continued downscaling to maintain the control of the gate over the channel [11-12].

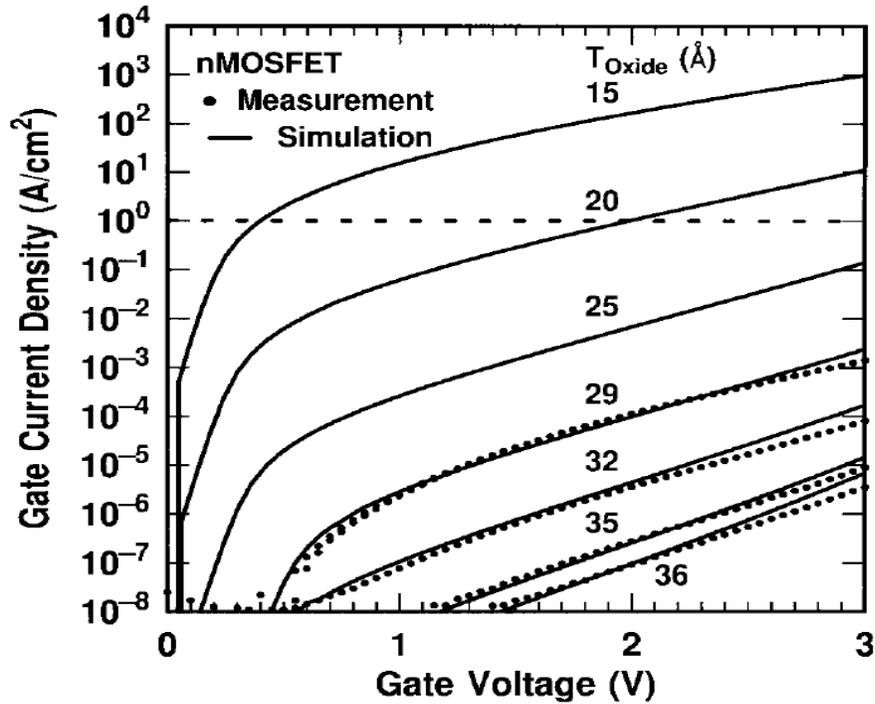


Figure 1.2 Gate leakage current for various thickness of SiO<sub>2</sub> dielectric. Leakage current increases exponentially due to the direct tunneling [10].

According to the 2007 International Technology Roadmap for Semiconductor (ITRS) [13], an equivalent oxide thickness (EOT) less than 1 nm is necessary beyond 65nm generation as summarized in Table 1.1. Therefore, higher dielectric constant gate insulators are being considered to solve problems facing conventional SiO<sub>2</sub> gate insulators as well as to keep continuing scaling. The gate dielectric capacitance is inversely related to the thickness

$$C = \frac{k_{ox} \epsilon_0}{t_{ox}} \quad (1.1)$$

where  $k_{ox}$  is the dielectric constant of oxide,  $\epsilon_0$  is the permittivity of free space, and  $t_{ox}$  is the thickness of the oxide. This expression can be written in terms of the equivalent oxide thickness (EOT), which represents the theoretical SiO<sub>2</sub> thickness that is required to achieve the same capacitance with high- $k$  dielectric

$$EOT_{high-k} = \left( \frac{k_{SiO_2}}{k_{high-k}} \right) t_{high-k} \quad (1.2)$$

Thus, physically thicker dielectric materials having higher  $k$  value than SiO<sub>2</sub> ( $k=3.9$ ) can be maintained at the same level of EOT and corresponding inversion charges. This thick high- $k$  layer also reduces the probability of electrons and holes tunneling through the dielectric and hence the leakage problem mentioned above can be hindered. Provided that band offsets are sufficiently large, the use of thicker dielectric layers result in less gate leakage current, thereby permitting further scaling of the dielectric thickness. In order to be used as gate dielectrics, alternative high- $k$  materials must satisfy some key requirements such as having appropriate barrier heights, high dielectric constants, ability to form a stable interface with Si as well as gate electrode materials, and good interface quality at dielectric-silicon interface to achieve high channel mobility [14]. Higher band offset means that carriers are less likely to be injected into insulator. It is reported that the gate leakage current is unacceptably large when the band offset is less than 1.0 eV [15]. Figure 1.3 illustrates the relationship between band gap and dielectric constant for several high- $k$  dielectric materials. It clearly shows the trade-off between band gap and dielectric constant which limits the selection of candidate materials. Based on the selection criteria, several high- $k$  materials such as Al<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>,

ZrO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, and HfO<sub>2</sub> have been proposed as possible candidates for replacing SiO<sub>2</sub> dielectric [14-19]. Al<sub>2</sub>O<sub>3</sub> is the only high-*k* dielectric material having a large bandgap similar to SiO<sub>2</sub> but the *k* value is only 2 ~ 2.5 times larger than SiO<sub>2</sub>. Moreover, it has been shown that the presence of Al<sub>2</sub>O<sub>3</sub> in the gate stack can degrade channel properties due to interfacial fixed charge [18]. It has also reported that Ta<sub>2</sub>O<sub>5</sub> and ZrO<sub>2</sub> are not stable with Si as well as poly Si although they have desired *k* value [19-20]. After numerous studies, Hf-based metal oxide and their silicates (HfO<sub>2</sub> and HfSiO<sub>x</sub>) have been leading candidates as alternative gate dielectrics due to their physical and chemical properties such as thermodynamic stability on Si, acceptable barrier heights, ease of deposition, higher mobility than other high-*k* dielectrics [22-24]. Table 1.2 summarizes the properties of HfO<sub>2</sub> compared to SiO<sub>2</sub>.

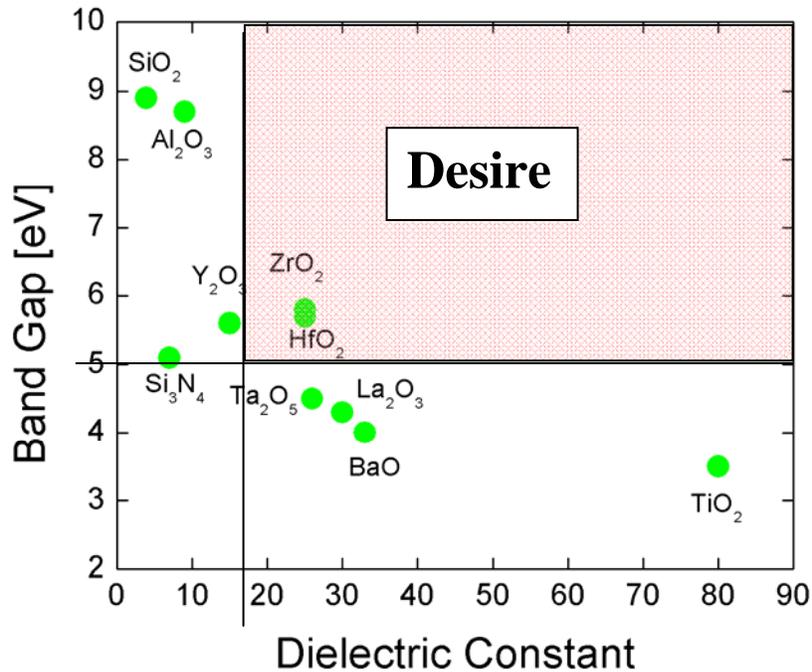


Figure 1.3 Relation between bandgap and dielectric constant for various high *k* dielectric materials. Data were taken from [14]

Table 1.2 Dielectric Properties of HfO<sub>2</sub> and SiO<sub>2</sub>

<b>Material Properties</b>	<b>HfO<sub>2</sub></b>	<b>SiO<sub>2</sub></b>
<b>Dielectric Constant</b>	17 ~ 25	3.9
<b>Bandgap [eV]</b>	5.7	9
<b>Barrier Height at CB [eV]</b>	1.5	3.5
<b>Barrier Height at VB [eV]</b>	3.4	4.4
<b>Refractive Index</b>	2.2	1.47
<b>Density [g/cm<sup>3</sup>]</b>	9.68	2.27
<b>Interface State [cm<sup>-2</sup>eV<sup>-1</sup>]</b>	>10 <sup>11</sup>	< 5X10 <sup>10</sup>

### 1.3 Metal Gate Electrodes

Doped poly-silicon gate has also been used as the gate electrode on SiO<sub>2</sub> dielectrics due to ease of integration. However, the use of poly-silicon with ultrathin gate dielectrics is becoming a major problem for submicron devices [25-26]. The major challenges with poly-silicon gate on top of thin gate dielectrics includes 1) the formation of a poly depletion layer at gate/dielectric interface, 2) dopant penetration during the activation annealing, and 3) increase in gate sheet resistance. A poly-silicon depletion layer is formed at the poly-silicon/gate oxide interface where the active poly-silicon dopant concentration is relatively

low as compared to bulk of the electrode. Conventional CMOS process requires the use of n+ poly-silicon gate for NMOS and p+ poly-silicon gate for PMOS which accomplished by ion implantation and subsequent annealing. However, since shallow junctions are needed for sub-micron devices, the energy of implantation and dopant activation temperatures are substantially constrained resulting in less active dopant concentration in the poly-silicon gate, especially at the oxide interface. This reduction of the dopant concentration at poly-silicon/oxide interface can form a depletion layer resulting in increase an effective oxide thickness. Therefore device threshold voltage increases and transconductance decreases and as a result drive current decreases [26]. Even in the absence of dopant depletion, as poly-silicon thicknesses are scaled down in the sub-micron regime, the poly-silicon sheet resistance gets larger and hence limits the MOSFET circuit's speed. Dopant penetration is another problem. Increases in active dopant concentration in poly-silicon gate can reduce sheet resistance but the limitation of poly-silicon doping is  $\sim 10^{21} \text{cm}^{-3}$  which may not be enough to prevent depletion effect. During the dopant activation thermal cycle, some of the boron dopant penetrates through the thin gate oxide into the channel and shifts the device threshold voltage. Replacing thin  $\text{SiO}_2$  gate dielectrics with high- $k$  dielectrics can overcome some of problems associated with poly-silicon gate electrode such as dopant penetration or minimize poly depletion effect because of physically thicker dielectric. However integration of poly-silicon gate with high- $k$  dielectric can cause alternate problems. It has been reported that the Fermi level of poly-silicon gate is pinned to the high- $k$  dielectric so that the device threshold voltage cannot be adjusted as shown in Fig. 1.4 [27-28].

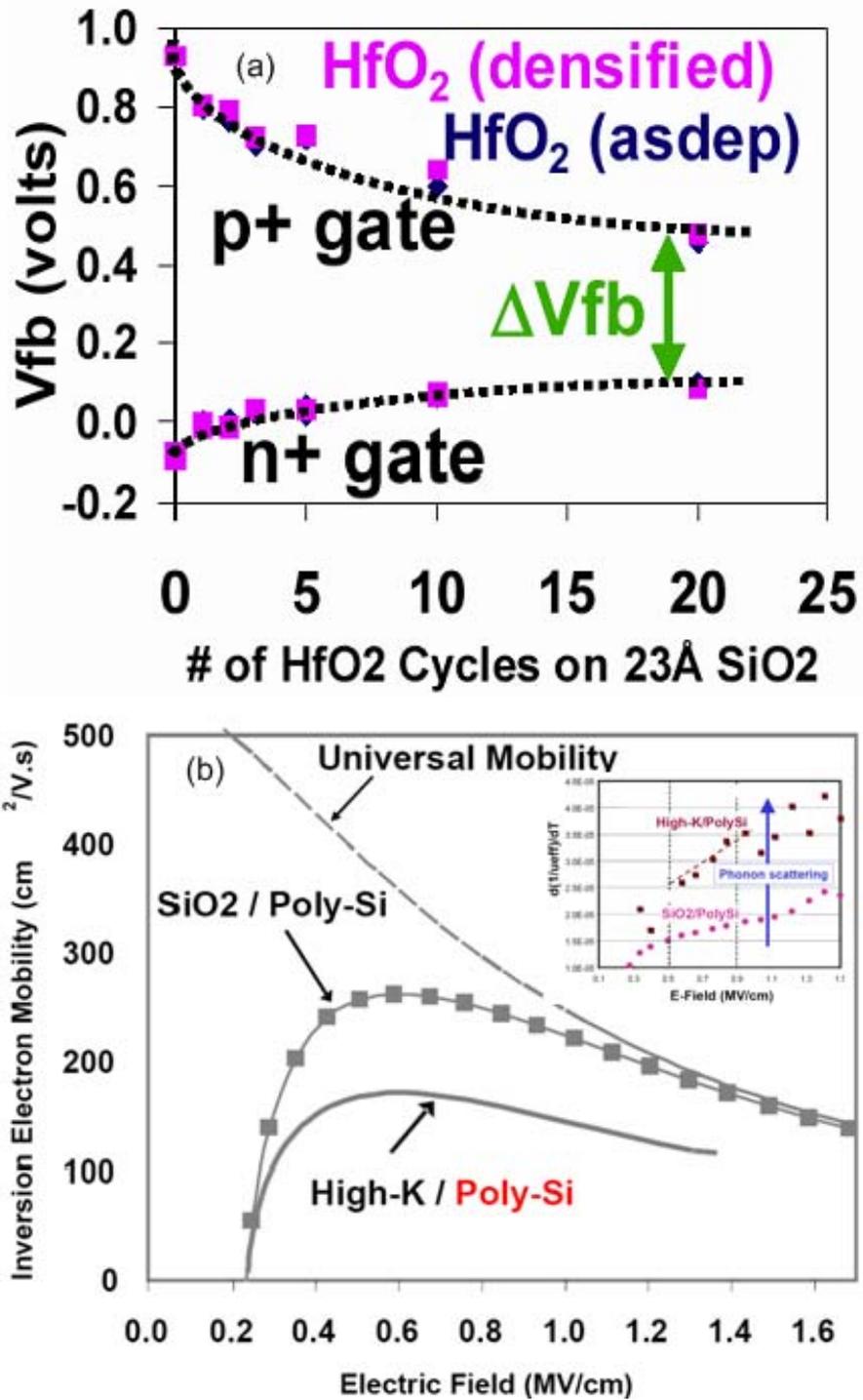


Figure 1.4 (a) Fermi level pinning of  $n^+$  and  $p^+$  poly-silicon gates on  $HfO_2$  dielectric after C. Hobbs [27] and (b) effective mobility degradation of poly-silicon/high- $k$  stack after R. Chau [29]. The inset of (b) shows the effect of scattering on  $HfO_2$  dielectric.

Furthermore, it also reported that the mobility of poly-silicon/high- $k$  gate stack is degraded since the charges presented in the high- $k$  dielectric cannot be screened by the poly-silicon gate [29].

Using a metal as a gate electrode can potentially eliminate these limitations of poly-silicon gates. However, replacing the poly-silicon gate electrode with metal gate electrodes imposes serious manufacturing and reliability challenges. Metal gate electrodes need to have thermal/chemical stability and process compatibility with high- $k$  dielectrics and also be able to withstand the entire CMOS processing sequence. In order to be integrated as n-channel and p-channel devices, dual gate work functions ( $\phi_m$ ) are needed. As summarized in Fig. 1.5, it has been found that the work function of Al, Ta, Ti, Hf, and Zr metal were near the conduction band edge of Si, while Ru, Rh, Co, Pt, Pd, and RuO<sub>2</sub> were near the valance band edges so that these metals appear to be the potential candidates for NMOS and PMOS gate electrodes, respectively. However, the former metals are suffering from the high temperature stability issues resulting in higher gate work functions than desired values whereas the latter metals have interfacial layer growth by oxygen diffusion and adhesion problems [30-32]. There has also been the introduction of conducting metal nitrides such as TaN, TiN, and TaSi<sub>x</sub>N<sub>y</sub>, which also act as good gate electrode candidates [33-35]. These metal electrodes can be easily introduced to the fabrication processes and solve the issues associated with elemental metal gates. However, the work functions of metal nitrides are typically near the midgap resulting in difficulty to control both  $V_T$  and short channel effects.

As an alternate route, several groups have investigated Fully-Silicided (FUSI) gate

electrode due to the compatibility of conventional processing. FUSI gate electrode can provide drive current improvement and significant gate leakage reduction due to the elimination of poly depletion effect and improvement of the effective mobility [37]. Threshold voltage can be further modulated with pre-doping with dopants (As and Sb for NMOS and B for PMOS) or controlling of  $Ni_xSi_y$  phases [37-38]. Although these approaches demonstrated improved electrical characteristics over poly-silicon gate, it has not demonstrated the effective work function values of 4.35 eV or less especially with Hf based dielectrics yet.

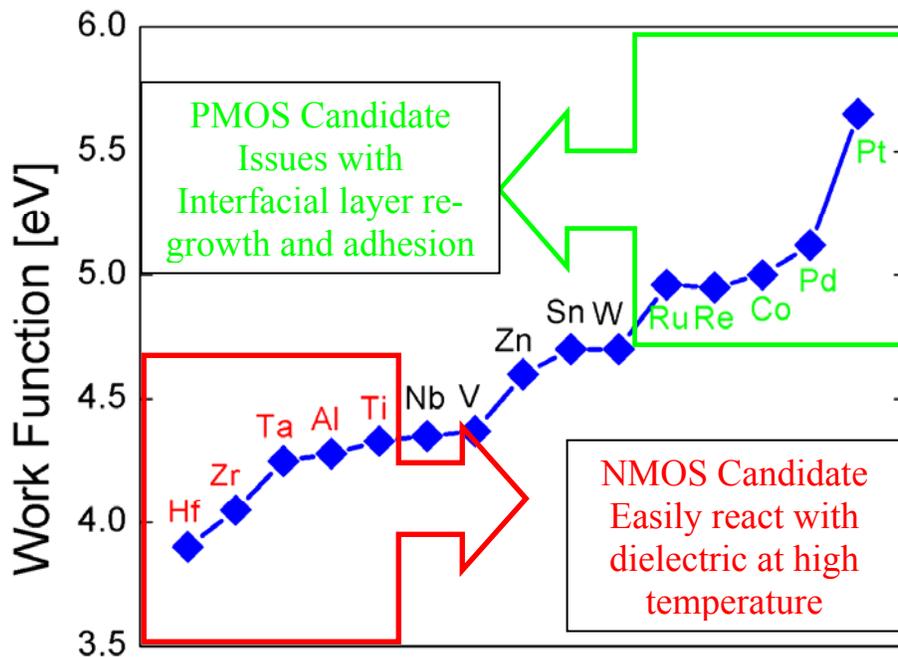


Figure 1.5 Candidate Elemental metals for NMOS and PMOS based on vacuum work function.

## 1.4 Property of Group III Elements

Group III elements such as rare-earth metals have been of interest for advanced CMOS devices since they provide the lowest vacuum work function (from 2.6 eV to 3.4 eV) among metals [39]. Their silicides have also been widely studied for nMOS contact application owing to the low barrier height [40]. However, since Si is a diffusion species during silicidation there is a potential issue associated with void formation [41]. One way to obtain a low work function with minimizing voiding issue is to form silicides from binary alloys of Ni and rare earth metals since the presence of both Ni and rare earth metal is expected to significantly impact the diffusion kinetics of the moving species.

Rare-Earth oxides and their silicates have been explored for their high dielectric constant and wide energy band gap [42-43]. Although Rare-Earth oxides are attractive, it is not feasible to use as them as gate dielectrics because they tend to have low crystalline temperature and are not thermally stable on Si [44]. To avoid this, recent studies have utilized gate dielectric capping approaches ( $\text{La}_2\text{O}_3$  for nMOS and  $\text{Al}_2\text{O}_3$  for pMOS) on  $\text{HfO}_2$  dielectric to obtain the desired threshold voltage ( $V_T$ ) while maintaining low EOT with good electrical and reliability properties [45-46]. While the above mechanisms look promising, fundamental understanding of how rare-earth modulates the  $V_T$  and what impact it has on the device mobility and reliability is still lacking.

$\text{Al}_2\text{O}_3$  was initially considered as a potential replacement of  $\text{SiO}_2$  due to comparable band gap to  $\text{SiO}_2$ , large band offset, and good thermal stability [14]. Moreover, the presence of Al near the channel can provide negative charges suitable for pMOS application at a cost

of mobility [47]. Despite its several advantages, it is only considered as a short term solution because of its relative small dielectric constant.

## 1.5 Objectives

The purpose of this work is to understand the effect of group III elements incorporation into advanced metal gate / high- $k$  dielectric stacks to achieve the desired gate stack work function without degrading electrical performance. The physical origins and possible mechanisms are provided in order to explain the experimental results. By incorporating group III elements into the gate stack, device  $V_{FB}/V_T$  can be modulated to the desired value for both NMOS (by using Rare Earth metals and oxides) and PMOS (by using Al-based dielectric capping) while maintaining key device properties. Based on these studies, an alternative route to achieve dual CMOS metal gate / high- $k$  dielectric stacks for the next generation technology is demonstrated and supported with encouraging experimental results.

## 1.6 Overview of dissertation

This dissertation will correlate electrical characterization results with analytical characterization. This work will provide evaluation of Rare-Earth metal incorporation into advanced gate stack by engineering to the gate (using Rare-Earth metals) associated with Ni-FUSI approach or by engineering to the high- $k$  dielectric (using ultrathin oxide capping approaches) with stable nitride metal gate as shown in Fig. 1.6.

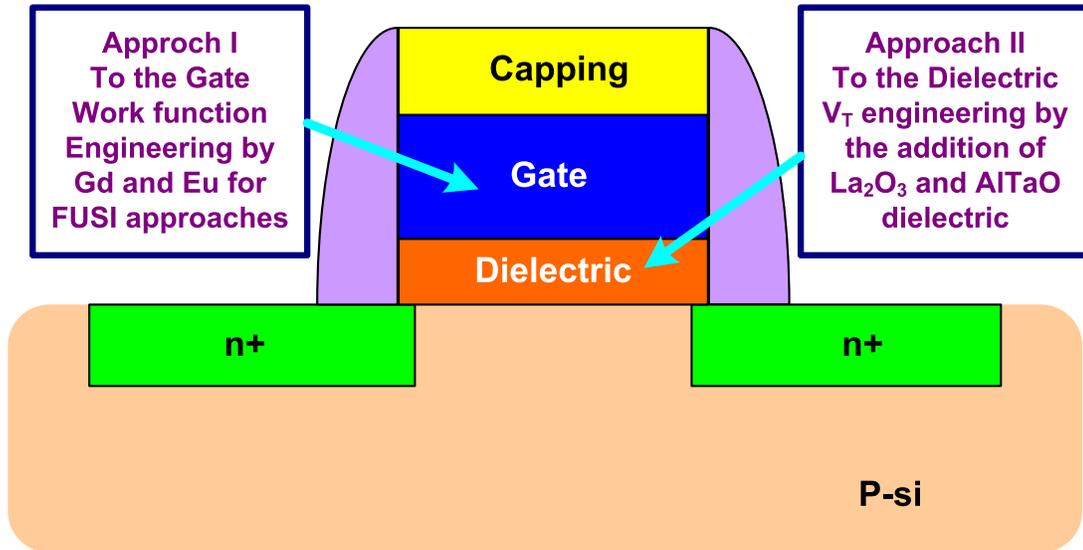


Figure 1.6 Schematic representation for proposed Approaches.

Following the introduction chapter, chapter 2 provides a novel deposition and fabrication process and detailed basic and advanced electrical characterization technique. Relative theory and background are also discussed.

Chapter 3 discusses the impact of Rare Earth metal (RE = Gd and Eu) incorporation into Ni-based FUSI gate on  $\text{HfSiO}_x$  dielectrics in terms of effective work function modulation and device characteristics.

Chapter 4 investigates the impact of Rare Earth oxide capping on  $V_{\text{FB}}/V_{\text{T}}$  modulation. The effect of  $\text{La}_2\text{O}_3$  capping on device performance focused on threshold voltage modulation and mobility is evaluated. Based on experimental data the mechanism explaining electrical results is also proposed.

Chapter 5 presents an analysis of oxide capping approach for PMOS devices. The impact of  $\text{Al}_2\text{O}_3$  and  $\text{AlTaO}_x$  incorporation on electrical performance of TaN/ $\text{HfO}_2$  stack is

provided. The effect of the incorporation of oxide capping layer on device reliability is also shown with explanation.

Finally chapter 6 summarizes the dissertation research and suggests the future works in this area.

## **Chapter 2**

### **Experimental Description and Characterization**

#### **Methodology**

This chapter will provide experimental and characterization techniques used in this dissertation. Description of the process flows and various deposition techniques for metal gates and high- $k$  dielectrics are discussed. Detailed basic and advanced electrical and material characterization for MOSCAPs and MOSFETs are also addressed.

#### **2.1 Deposition techniques for advanced gate stack**

This section provides detailed gate stack deposition methods used in this dissertation. Atomic Layer Deposition (ALD) method was used to deposit  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  high- $k$  dielectric materials. A Molecular Beam Epitaxy (MBE) tool was used to deposit  $\text{La}_2\text{O}_3$  and  $\text{TaO}_x$  dielectrics. Radio-frequency (RF) magnetron sputtering system was used to deposit metal gate electrodes.

##### **2.1.1 Atomic Layer Deposition**

Atomic Layer Deposition (ALD) is a film deposition method based on the principle of self-limiting growth by chemisorption of reactant gases. The concept of ALD was proposed by T. Santona and co-workers in 1970's in order to deposit epitaxial  $\text{ZnS}$  and  $\text{SnO}_2$

[48-49]. ALD technology has grown rapidly and become popular since late 1990's due to the fact that microelectronic industry has started to consider ALD technology for the ultrathin high-*k* gate dielectric and high aspect ratio deposition.

Figure 2.1 shows the typical ALD  $\text{Al}_2\text{O}_3$  formation process using Trimethyl Aluminum (TMA) and water as a precursor as described in [50]. When Al precursor is pulsed into the reaction chamber, TMA reacts with the adsorbed hydroxyl (O-H) groups at surface producing methane ( $\text{CH}_4$ ) as the reaction product. Since TMA does not react with itself, excess TMA precursor as well as methane is then purged out during the purge cycle.

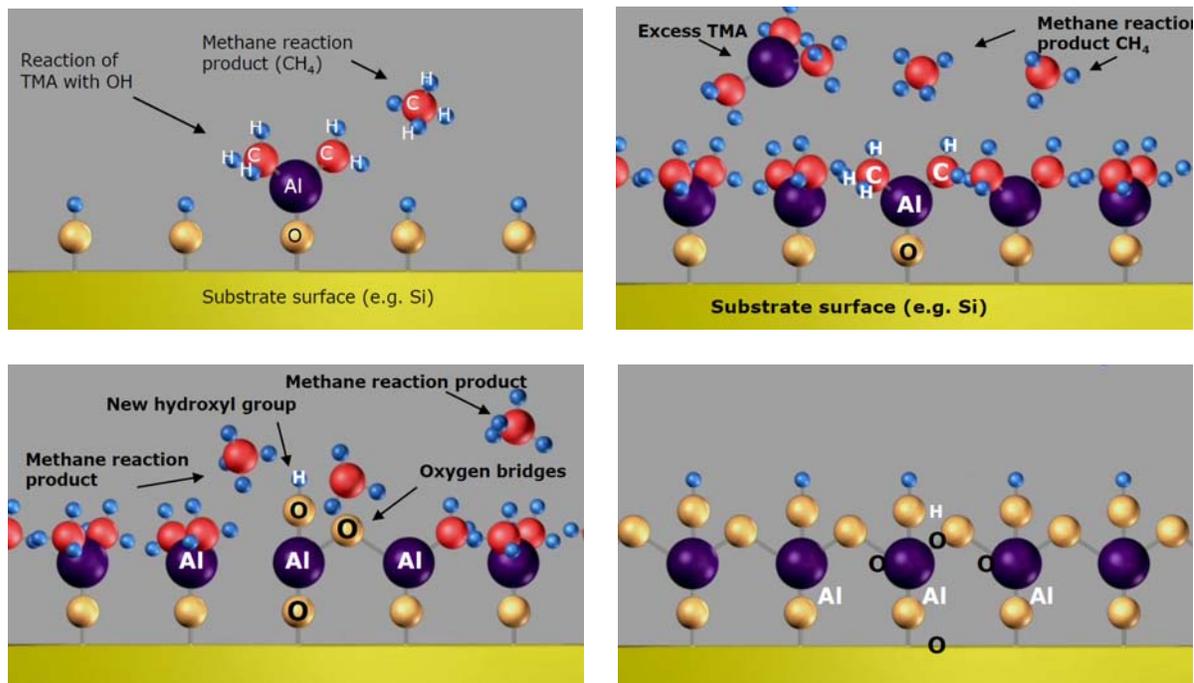


Figure 2.1 Typical ALD  $\text{Al}_2\text{O}_3$  process illustrations from Cambridge Nanotech ([www.cambridgenanotech.com](http://www.cambridgenanotech.com)), (a) TMA pulse, (b) un-reacted TMA precursor and byproduct are purged out, (c)  $\text{H}_2\text{O}$  precursor is pulsed to create O-H terminated surface followed by purging process of reaction product and (d) as a result one layer of desired film is deposited. After two sequential pulse and purge cycle's one monolayer of desired film is deposited. With our system the deposition rate is  $\sim 1.1 \text{ \AA/cycle}$

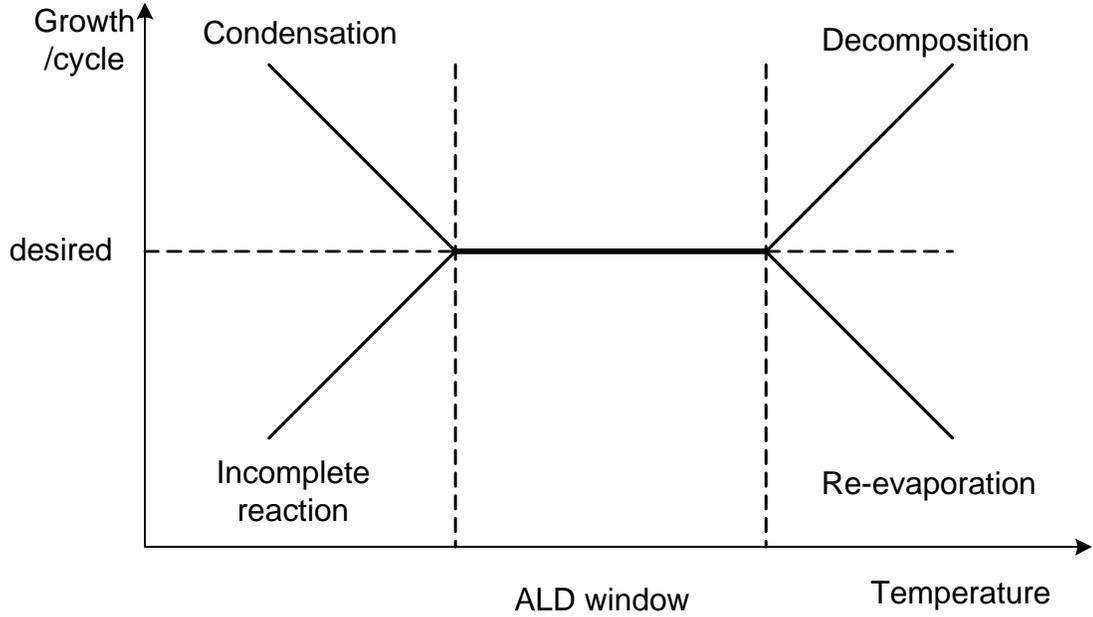
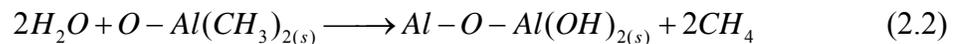
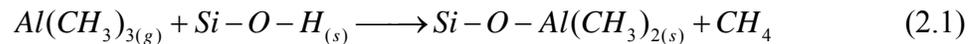


Figure 2.2 Illustration of ALD acceptable temperature range.

After the un-reacted TMA and  $\text{CH}_4$  are pumped out, water vapor ( $\text{H}_2\text{O}$ ) is then pulsed into the reaction chamber so that  $\text{H}_2\text{O}$  molecules react with the dangling methyl group on the surface forming Al-O bridges with hydroxyl terminated surface for the next TMA pulse. Since excess water vapor also does not react with the hydroxyl surface group, one mono layer of the desired film can be deposited. The two reactions are expressed as



This self-limiting chemisorption of each layer and passivation in each cycle enables the precise thickness and uniformity control of film growth which is required for ultrathin dielectric films and high aspect ratio structures. In addition, low temperature deposition process of ALD provides another advantage of using the ALD method. However, the

deposition temperature should be high enough for the reaction to occur on the surface. If the deposition temperature is too low, then 1) thermally activated chemisorption as well as film forming reaction rates can reduce resulting in a decrease in the deposition rate or 2) pulsed precursors on the surface can react with each other resulting in an increase in deposition rate [51]. In contrast, if the deposition temperature is too high, chemical bonding cannot be sustained or the density of chemically reactive sites is reduced [51]. Figure 2.2 depicts the allowable temperature window for ALD process.

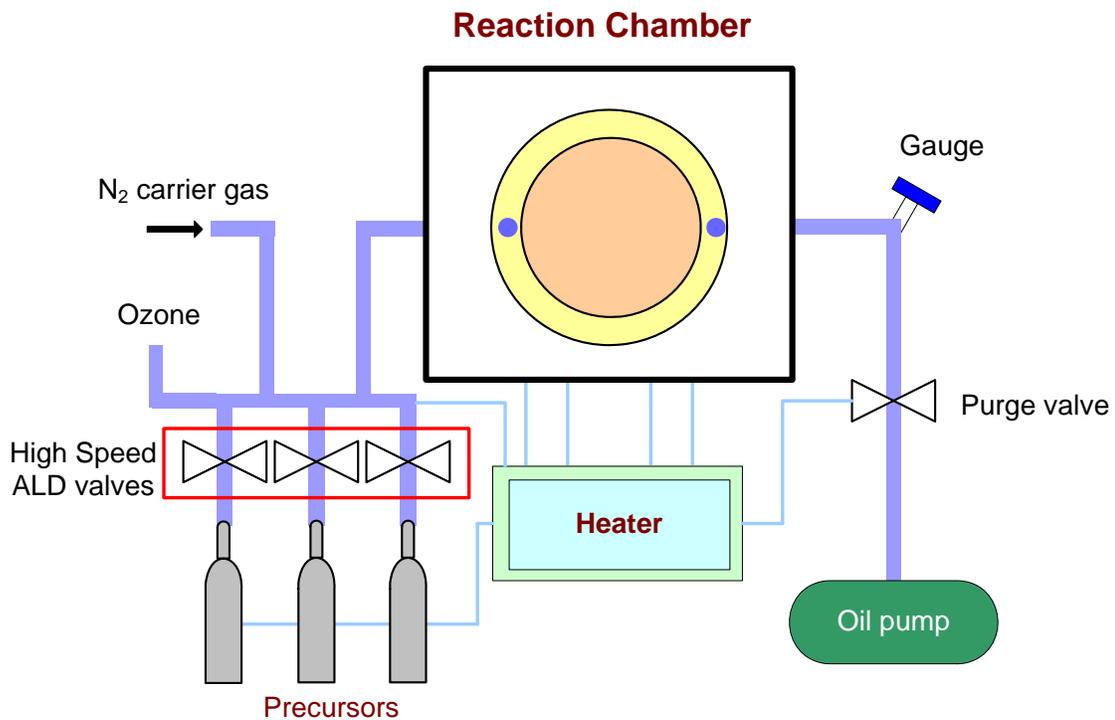


Figure 2.3 Schematic of ALD system used for HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> deposition.

The ALD process used in this work was performed on a Savannah S100 system from Cambridge Nanotech as illustrated in Fig. 2.3. The base pressure was 200 mTorr with constantly flowing N<sub>2</sub> carrier gas. The tool is equipped with high speed pneumatic valves in

order to precisely control the pulse time (in a range of ms) of precursors. Two heater lines were connected to the substrate holder supporting temperature range up to 400 °C. Table 2.1 summarizes ALD deposition conditions for Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> process used in this work.

For HfO<sub>2</sub> deposition Tetrakis, dimethylamido-hafnium (TDMHA), and H<sub>2</sub>O were used as reaction precursors. Since TDMHA is solid at room temperature Hf precursor (TDMHA) was heated at 75 °C. For Al<sub>2</sub>O<sub>3</sub> deposition TMA and H<sub>2</sub>O were used as precursor gases without heating. All dielectric depositions were done at a substrate temperature of 200 °C with no exposure time.

Table 2.1 Summary of deposition condition for ALD Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> process

		HfO <sub>2</sub>	Al <sub>2</sub> O <sub>3</sub>
Precursor		TDMAH	TMA
Reactant		water (H <sub>2</sub> O)	water (H <sub>2</sub> O)
Substrate Temperature		200 °C	200 °C
Precursor temperature		Hf: 75 °C	Al: RT
		H <sub>2</sub> O: RT	H <sub>2</sub> O: RT
Pulse	Precursor	0.2 s	0.015 s
	Reactant	0.3 s	0.015 s
Exposure	Precursor	0 s	0 s
	Reactant	0 s	0 s
Purge	Precursor	8 s	8 s
	Reactant	8 s	8 s
Deposition Rate		0.9 Å/cycle	1.1 Å/cycle

## 2.1.2 Molecular Beam Deposition (MBE)

TaO<sub>x</sub> and La<sub>2</sub>O<sub>3</sub> high-*k* dielectrics were deposited using evaporation in the ultrahigh vacuum (< 1 x 10<sup>-9</sup> Torr) molecular beam epitaxy (MBE) system shown in Fig 2.4 [45]. Lanthanum oxide was grown using lanthanum source evaporated using an effusion cell at a temperature of 1700 °C and high purity oxygen gas. Deposition pressure was maintained at 1 x 10<sup>-6</sup> Torr by oxygen flow and the substrate temperature was set at 350 °C. Moderate in-situ post deposition annealing was done at 400 °C for 10min in order to remove defects in oxide film and improve film quality. TaO<sub>x</sub> was grown at a substrate temperature of 300 °C with the chamber pressure < 1 X 10<sup>-8</sup> Torr. Ta was evaporated from Ta source with 8KV beam energy followed by in-situ post oxidation anneal using high purity O<sub>2</sub> gas at 450 °C for 10 min to completely oxidize evaporated Ta film. The growth rate is monitored by quartz crystal monitoring system.

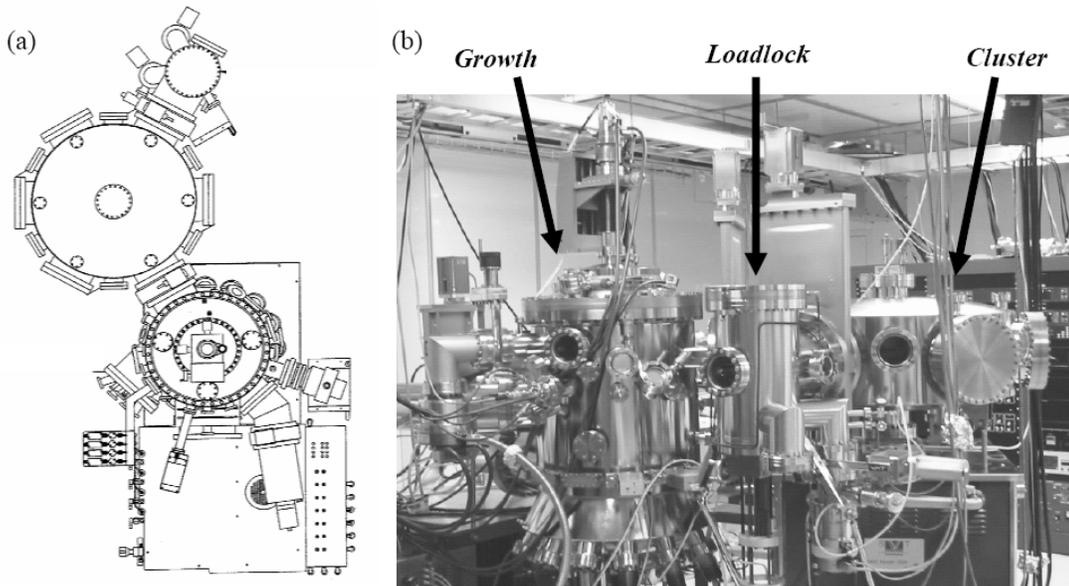


Figure 2.4 (a) Schematic and (b) photograph of MBE system used for La<sub>2</sub>O<sub>3</sub> and TaO<sub>x</sub> deposition [45].

### 2.1.3 RF-sputtering for gate electrode

Sputtering is widely used film deposition method for metals and ceramic thin films [52-54]. The sputtering process is based on the nature of momentum transfer of atoms. When inert gas (typically Ar) is introduced in the chamber, it collides with electron producing positively charged Ar ions and then accelerates to the negatively charged target material. Since these positively charged ions are energetic, they can eject target atoms through the energy transfer.

A magnetic field can be applied by using a magnetron behind the target material to enhance sputtering yield. The magnetron creates a magnetic field to increase density of plasma near the target resulting in higher deposition rate at a lower power. Radio-Frequency (RF) sputtering is also used for dielectric material deposition because of electron oscillation with ac field resulting in no charge accumulation at the target surface [53]. Therefore, RF magnetron sputtering provides several advantages such as 1) high deposition rate, 2) the capability to deposit and maintain complex alloy, and 3) deposition of most metals as well as insulators.

All the metal gate electrodes used in this work were deposited using UHV RF-magnetron sputtering system. The system consists of two chambers (main chamber and loadlock chamber) as illustrated in Figure 2.5. The base pressure of main chamber was kept lower than  $1 \times 10^{-8}$  Torr (typically  $7 \times 10^{-9}$  Torr) in order to minimize the level of impurities in the chamber. Three RF-magnetron guns are attached on top of the main chamber and thus three different materials or metal alloys can be easily deposited without breaking vacuum.

Alloy metal films such as  $\text{Ni}_x\text{Gd}_y$  and  $\text{Ni}_x\text{Eu}_y$  were deposited using co-sputtering of two targets and the composition and deposition rate are controlled by the RF power as

$$\left( \frac{\text{sputtering power of metal 1}}{\text{sputtering power of metal 1} + \text{sputtering power of metal 2}} \right)$$

Reactive sputtering such as TaN deposition was done by flowing Ar and  $\text{N}_2$  together. The deposition pressure was set to 5mTorr in order to prevent gas-phase collision and optimized deposition rate. In most cases tungsten (W) metal was used for the capping layer in order to prevent oxidation of metal gate as well as ensure good electrical contacts.

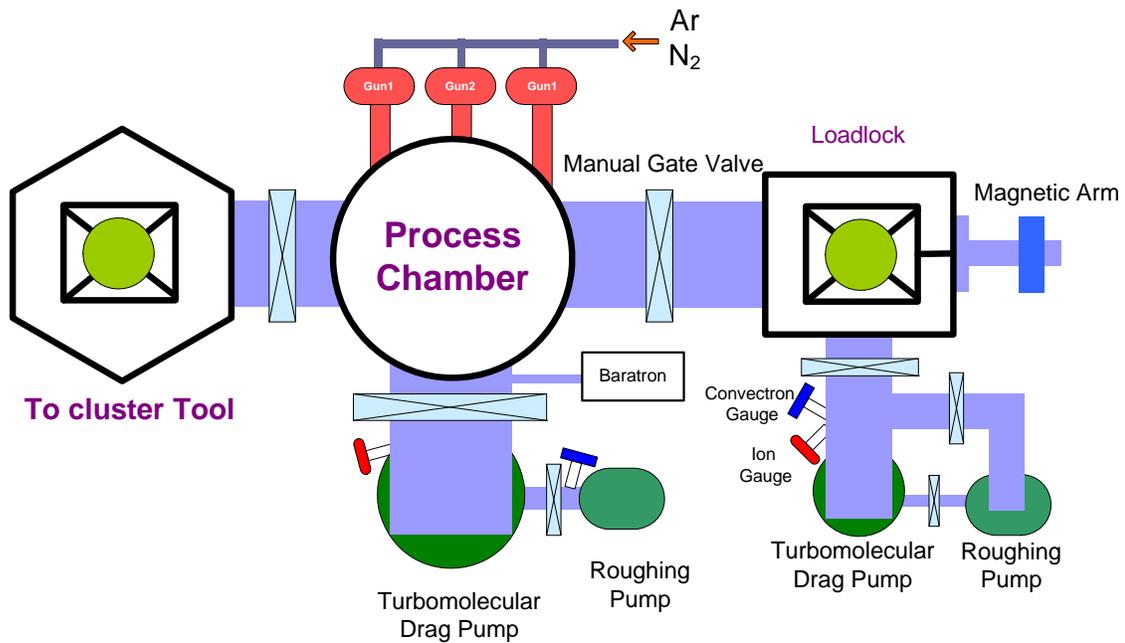


Figure 2.5 Schematic illustration of UHV-PVD (RF-magnetron sputtering) system.

## 2.2 Process flow

The standard gate first MOSFET processes are illustrated in Fig 2.6 and summarized key process steps in table 2.2. A detailed MOSFET process steps can be found in the appendix. The 4 level GEM masks set developed in our research group was used to fabricate various channel length and width FETs as well as overlap and non-overlap capacitors in order to perform charge pumping, compare device threshold voltage vs. channel length, and extract key device parameters. The junction activation temperatures were 950 °C for 10s and 1000 °C for 5s for PMOS and NMOS, respectively, in RTA system. All transistor and capacitor structures were conventionally defined by photo lithography and subsequent wet/dry etching techniques. Forming Gas Anneal (FGA) with Hydrogen was performed as a final processing step.

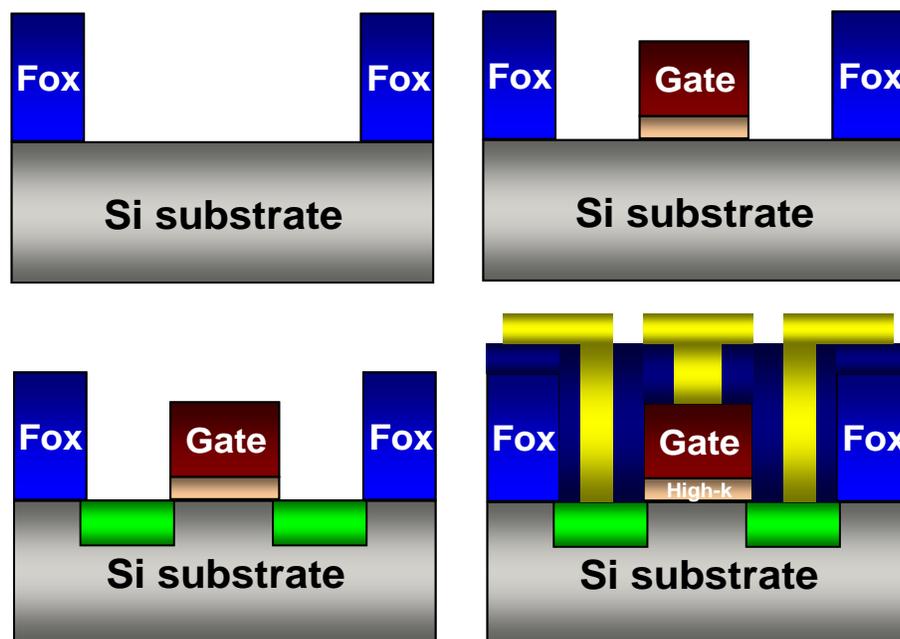


Figure 2.6 Schematic of typical MOSFET process steps (a) active, (b) gate stack formation, (c) source/drain implant, and (d) contact pad with isolation oxide layers

Table 2.2 Self-align MOSFET process

Step	Process	Detail	Note
1	JTB clean	JTB 111 solution for 10min	
2	Field Oxidation ( $f_{ox}$ )	1000 °C	2700 Å
3	Active Photolithography	GEM active mask	DF
4	Etch $f_{ox}$	Buffered Oxide Etch (BOE)	7min
5	RCA Clean	SC1 and SC2	10min each
6	Sacrificial oxidation	Dry oxidation	800 °C
7	Oxide etch	1% HF solution	
8	RCA Clean	SC1 and SC2	10min each
9	Gate Oxidation	Dry oxidation for SiO <sub>2</sub>	800 °C
10	Gate Dielectric deposition	ALD or MBE	
11	Gate Electrode deposition	PVD	TaN/W
12	Gate Photolithography	GEM Gate Mask	BF
13	Etch W capping layer	TFW solution	
14	Etch TaN/high-k layer	BCl <sub>3</sub> Dry etching	RIE
15	Low temperature Oxide	LPCVD or PECVD	410°C/250°C
16	Ion Implantation	BF <sub>2</sub> , 2X10 <sup>15</sup> cm <sup>-2</sup> , 15KeV	PMOS
		As, 5 X 10 <sup>15</sup> cm <sup>-2</sup> 20KeV	NMOS
17	Activation Anneal	950 °C to 1000 °C in N <sub>2</sub>	RTA
18	Etch LTO	BOE solution	7sec
19	Deposit thick LTO	PECVD	250 °C

Table 2.2 Self-align MOSFET process (continue)

20	Contact hole Photolithography	GEM contact	BF
21	Etch LTO	BOE solution	4min
22	Contact metal Phothlithography	GEM metal	DF
23	Contact metal evaporation	Ti/Al	50nm/200nm
24	Contact metal lift-off	NMP solution	
25	Forming Gas Anneal	400 ~ 500 °C	Furnace
26	Back side Oxide Etch		

### 2.3 Electrical Characterization Methodology

This section provides basic and advanced electrical characterization techniques commonly used in MOS technology in order to determine device properties. MOS capacitance–voltage (C–V) and current–voltage (I–V) techniques are used to extract and monitor parameters such as oxide capacitance, substrate doping, oxide charge, breakdown characteristics, and barrier height. Conventional MOSFET I–V curves are used to determine device performance and parameter extraction like  $V_T$ , subthreshold swing, drive current, and mobility. The advanced electrical characterization methods such as charge pumping are mainly used for high- $k$  dielectric based gate stacks since basic DC based MOSFET techniques suffer from charges (interfacial as well as fixed) caused by high- $k$  dielectrics. Bias temperature instability (BTI) is used to evaluate the device reliability paramters such as  $V_T$  shift,  $g_m$  degradation, and lifetime projection.

## 2.3.1 Two Terminal Electrical Characterization

### 2.3.1.1 Capacitance–Voltage (C–V) Characterization and effective work function extraction

The capacitance–voltage (C–V) method is known to be the most popular MOS characterization method since this can determine many important parameters of CMOS devices. The C–V measurement in this work was done using HP4284 LCR meters where L is an inductance, C is capacitance, and R is a resistance. When DC bias with ac signal was applied to the two terminals of the MOS structure the capacitance and the conductance can be measured simultaneously. It is noted that the superimposed ac signal should be as small as possible so that the measurement is not affected or altered by the ac signal [55]. Figure 2.7 (a) shows the typical MOS capacitor C–V curve at high and low frequencies and Figure 2.7 (b) shows equivalent circuit of the MOS capacitor where  $C_{ox}$  is the oxide capacitance,  $R_s$  the series resistance, and  $G_p$  is parallel conductance. It is assumed that metal gate and p-type Si substrate are used for the discussion. By sweeping gate bias the capacitance of the MOS capacitor varies since the capacitance is defined as

$$C = \frac{dQ}{dV} \quad (2.3)$$

If gate bias is more negative than flatband, the semiconductor side is accumulated with majority carriers (holes for p-type semiconductor) so the semiconductor accumulation capacitance ( $C_{acc}$ ) is very high thus shorting out the other parallel capacitances. Therefore the measured total capacitance is the gate oxide capacitance as shown in Fig. 2.7, region (a).

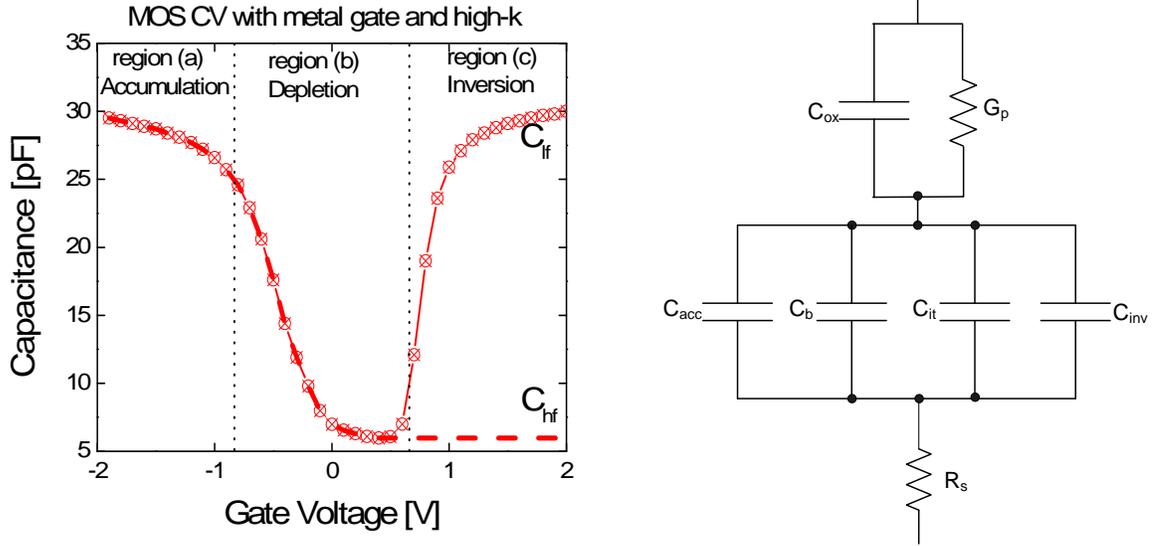


Figure 2.7 (a) Typical low and high frequency C–V curves and (b) equivalent circuit of the MOS capacitor structure.

The dielectric thickness can be determined using Equation 1.1 assuming the dielectric constant is known. When gate bias is between accumulation and inversion (region (b)), the semiconductor surface is depleted and thus the measured capacitance is the combination of  $C_{ox}$  in series with depletion capacitance ( $C_b$ ) resulting in decrease in total capacitance. Figure 2.7 region (c) represents the condition where the gate bias is in the inversion for both low and high frequency. If the applied frequency is low, then the inversion capacitance is dominant since inversion carriers can response the slowly varying signal, so the total measured capacitance is same as  $C_{ox}$ . If the frequency is high, the inversion carriers cannot follow the applied ac signal and the semiconductor capacitance becomes the depletion capacitance ( $C_b$ ) associated with a maximum depletion layer. Thus high frequency inversion capacitance ( $C_{min}$ ) is the combination of  $C_{ox}$  in series with the depletion capacitance in inversion ( $C_{b,inv}$ ). The substrate doping density can then be calculated from the  $C_{min}$  since  $C_{b,inv}$  is proportional

to the substrate doping. Once the oxide thickness and the substrate doping density are determined, the flatband voltage and corresponding fixed charge can be calculated. The relationship of  $V_{FB}$  to the gate dielectric charge distribution and the equivalent oxide thickness can be expressed as [56]

$$V_{FB} = \phi_{ms} - \frac{1}{\epsilon_{ox}} \left[ \int_0^{EOT} x \rho(x) dx \right] \quad (2.4)$$

where  $\epsilon_{ox}$  is the permittivity of SiO<sub>2</sub> and  $\phi_{ms}$  is the effective work function difference between gate and substrate. With the assumptions that (i) the density of interface states as well as bulk traps are negligible, (ii) a fixed charges are considered as sheet charge located at the interface, and (iii) a uniform distribution of fixed bulk charge  $\rho$  per unit volume exists in the gate dielectric, the equation (2.4) can be simplified as

$$V_{FB} = \phi_{ms} - \frac{1}{\epsilon_{ox}} Q_f EOT - \frac{1}{\epsilon_{ox}} \rho \frac{EOT^2}{2} \quad (2.5)$$

If the magnitude of the fixed charges at the interface is much higher than the bulk charges ( $Q_f \gg \rho EOT$ ), then the equation can be written as

$$V_{FB} = \phi_{ms} - \frac{1}{\epsilon_{ox}} Q_f EOT \quad (2.6)$$

indicating that  $V_{FB}$  is linearly related to the EOT. Thus, as shown in Fig. 2.8 by plotting extracted  $V_{FB}$  for several thicknesses of EOT,  $\phi_{ms}$  and the fixed charge at Si/SiO<sub>2</sub> interface can be extracted from the y-intercept and the slope respectively. Therefore, effective work function of the gate electrode can be determined from the relationship

$$\phi_{m,eff} = \phi_{ms} + \phi_s \quad (2.7)$$

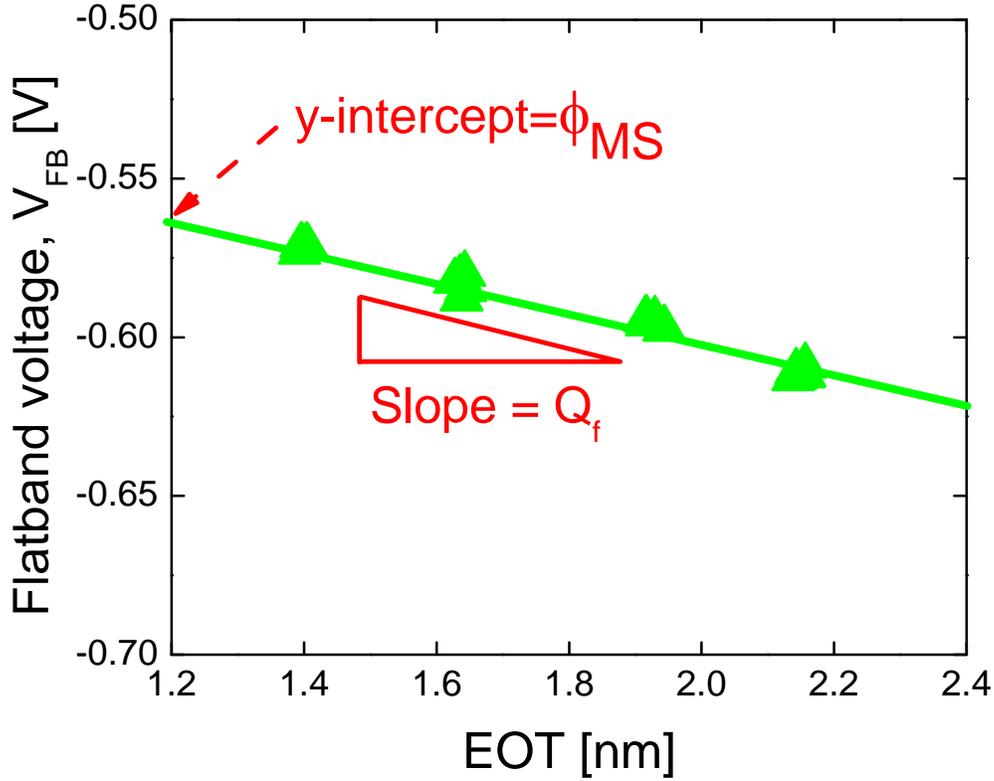


Figure 2.8  $V_{FB}$  vs. EOT plot extracted from C-V. Y-intercept represents  $\phi_{MS}$  and the slope is related to the fixed charge. Since  $\phi_S$  is known, the effective work function can be determined from the  $\phi_{MS}$ .

In addition, it is known that species with different electronegativity bonds across the each interfaces resulting in the partial charge transfer at the interface [57]. This uniformly formed charge layer is called as dipole layer which also contributes the device effective work function caused by the creation of voltage drops. Therefore the equation 2.6 can be modified

as

$$V_{FB} = \phi_{ms} - \frac{1}{\epsilon_{ox}} Q_f EOT + (\Delta V_{interface1} + \Delta V_{interface2} + \dots) \quad (2.8)$$

where  $\Delta V$  represents voltage drops due to the dipole formation at each interface. Therefore the effective work function of the gate stack can be extracted from

$$\phi_{m,eff} = \phi_m + \Delta V - \frac{1}{\epsilon_{ox}} Q_f EOT \quad (2.9)$$

which deviates from the vacuum work function value caused by the fixed charge and/or dipole layer.

### 2.3.1.2 Current – Voltage (I – V) Characterization

The current–voltage (I–V) characteristics are also commonly used method in electrical measurement techniques in order to analyze the quality of dielectric film such as breakdown characteristics and reliability. The current conduction through dielectric is a quantum mechanical process and is called tunneling. There are two types of well known tunneling processes for single SiO<sub>2</sub> dielectric, which are called Fowler–Nordheim (FN) tunneling [58] and direct tunneling (DT) [59] as depicted in Fig. 2.9. If carriers are tunneling through the triangular potential barrier, then FN tunneling process is dominant and the relationship is given by:

$$J_{FN} = A_G E_{ox}^2 \exp\left(\frac{-B}{E_{ox}}\right) \quad (2.10)$$

Where

$$\begin{aligned}
A &= \frac{q^3 (m / m_{ox})}{8\pi h \Phi_B} \\
B &= \frac{8\pi \sqrt{2m_{ox} \Phi_B^3}}{3qh}
\end{aligned}
\tag{2.11}$$

The plot of  $\ln(J_{FN} / E_{ox}^2)$  versus  $1/E_{ox}$  should be a straight line if the current conduction through the oxide is pure FN process as seen in Fig 2.10. The FN tunneling current increases exponentially with applied field as seen in Equation 2.10. If current conduction is through the trapezoidal barrier, then the direct tunneling process is dominant where the current increases exponentially as the dielectric thickness and the relationship is given by

$$J_{DT} = A_G E_{ox}^2 \exp\left(\frac{-B[1 - (1 - qV_{ox} / \Phi_B)]^{1.5}}{E_{ox}}\right)
\tag{2.12}$$

The current conduction is very complicated with high- $k$  based dielectrics since deposited high- $k$  layers typically have traps and defects which also contribute carrier conduction through the dielectric. It has been reported that there are several carrier conduction mechanisms with high- $k$  dielectrics such as Frenkel-Poole (FP) emission and trap assisted tunneling resulting in increase in the total current [39, 60]. FP currents are due to the field enhanced excitation of electrons through trapping sites in the dielectric. In order to distinguish stated current conduction mechanism from the quantum-mechanical tunneling process, I-V measurements as a function of temperature with detailed modeling are required since these types of conduction have stronger temperature dependency than quantum mechanical tunneling processes [39].

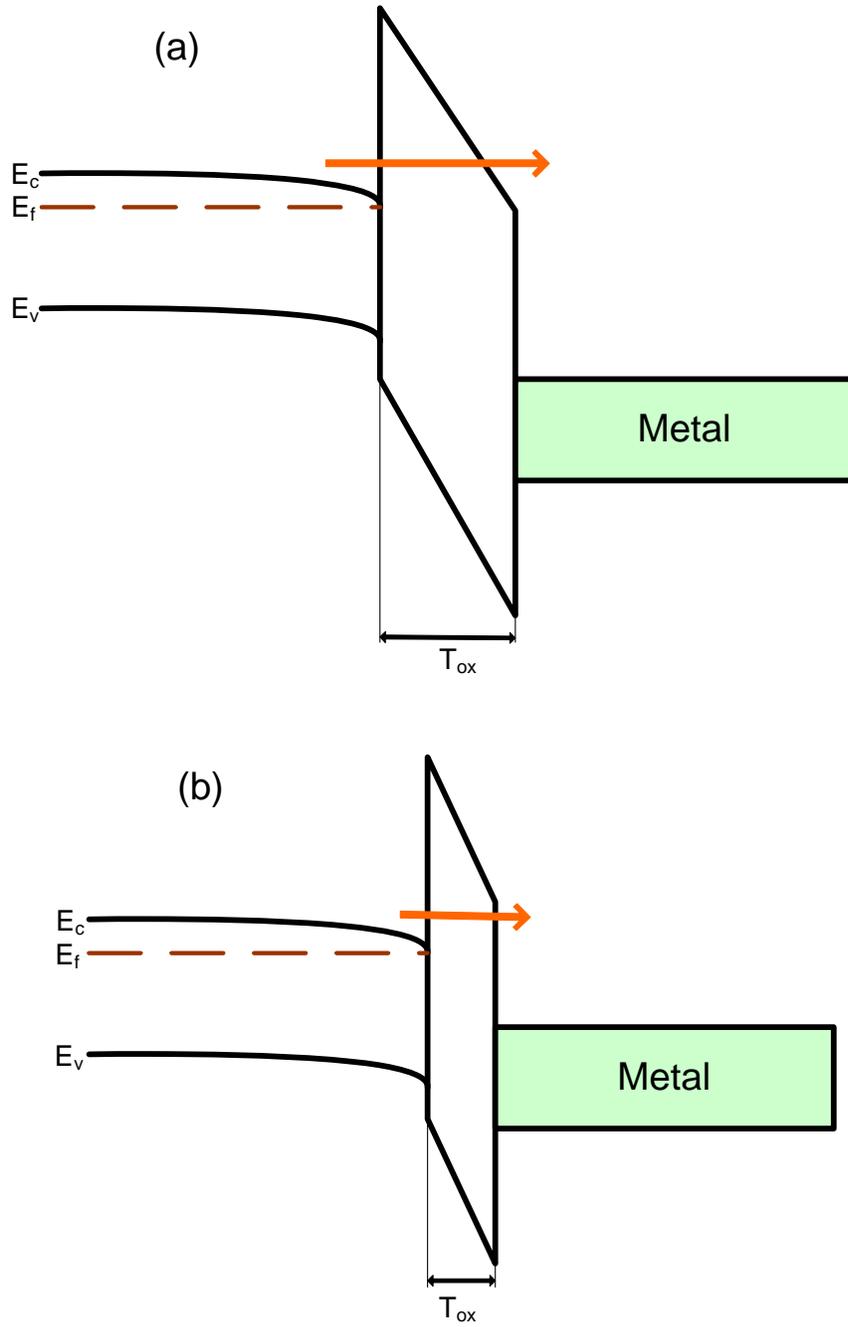


Figure 2.9 Band diagram of (a) Fowler–Nordheim (FN) Tunneling process and (b) Direct Tunneling (DT) process through gate dielectric

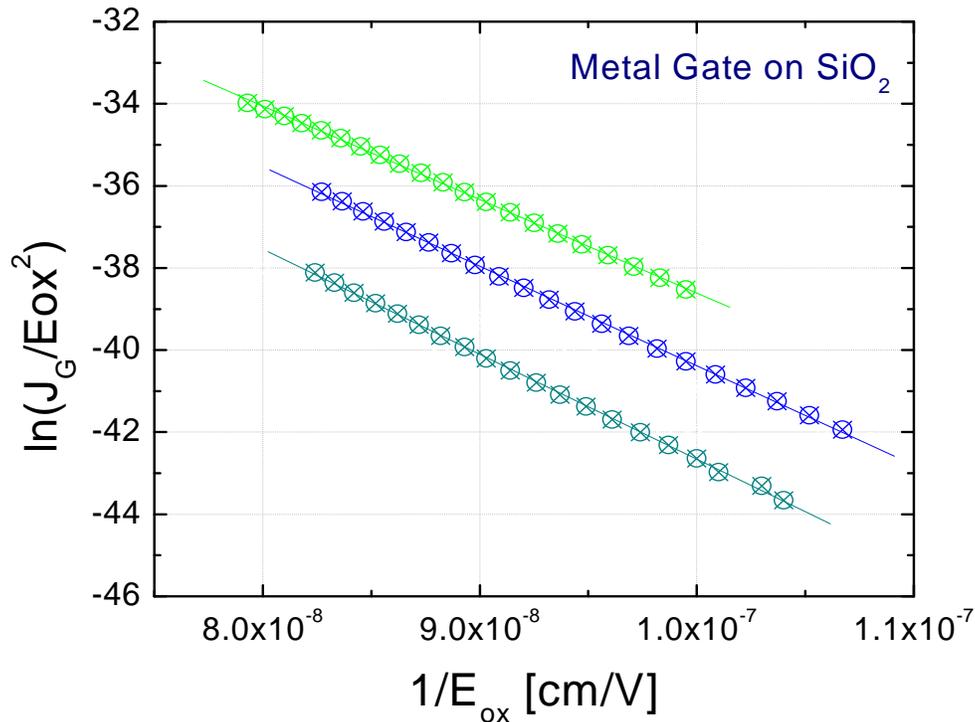


Figure 2.10 Typical FN plot of metal gate / SiO<sub>2</sub> stack taken from  $J_g - V_g$  curve. Linear behavior confirms the current conduction is dominated by FN tunneling. The slope is related to the barrier height.

## 2.3.2 Four Terminal Basic Electrical Characterization

### 2.3.2.1 MOSFET $I_{ds} - V_{gs}$ and $I_{ds} - V_{ds}$

In MOSFET devices  $I_{ds} - V_{ds}$  and  $I_{ds} - V_{gs}$  characteristics are important since these are directly related to the device performances. In  $I_{ds} - V_{ds}$  characteristics drain current is monitored while drain voltage is swept from 0V to operating voltage ( $V_{dd}$ ). This gives saturation drain current ( $I_{dsat}$ ) providing device output current under typical operating condition.  $I_{ds} - V_{gs}$  characteristics vary as drain voltage changes and can be divided into two

regions of operation: linear region and saturation region. In the linear region the MOSFET acts as resistor where the drain current (or channel resistance) is controlled by the gate voltage. When the drain voltage is equal to or larger than the gate over drive voltage ( $V_{gs} - V_T$ ) the drain current starts to saturate and is no longer function of the gate voltage. The relationships for two operating regions are expressed as:

$$I_d \cong \mu C_{ox} \frac{W}{L} (V_g - V_T) V_d \quad : \text{linear operation when } V_{ds} < V_{gs} - V_T \quad (2.13)$$

$$I_d \cong \mu C_{ox} \frac{W}{L} (V_g - V_T) V_d^2 \quad : \text{saturation operation when } V_{ds} > V_{gs} - V_T \quad (2.14)$$

where  $\mu$  is effective mobility of the device,  $C_{ox}$  is oxide capacitance, and  $W$  and  $L$  are channel width and length respectively. Linear  $I_{ds} - V_{gs}$  curves obtained at low drain voltage (<100mV) are typically used to extract parameters like threshold voltage, mobility, and effective channel length.

$V_T$  is called as the channel threshold voltage and expressed as

$$V_T = V_{fb} + 2\phi_b + \frac{\sqrt{2qN_a \epsilon_{si} \phi_b}}{C_{ox}} \quad (2.15)$$

### 2.3.2.2 Threshold voltage extraction

Threshold voltage is one of the most important parameter in CMOS devices. This is basically a turn on voltage of the device and separation voltage of the subthreshold region from the strong inversion region. One of the most common measurement techniques for the

threshold voltage is known as linear extrapolation method determined from the linear  $I_{ds} - V_{gs}$  curve at a low drain voltage. The device transconductance,  $g_m$ , is defined as

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}=\text{constant}} \quad (2.16)$$

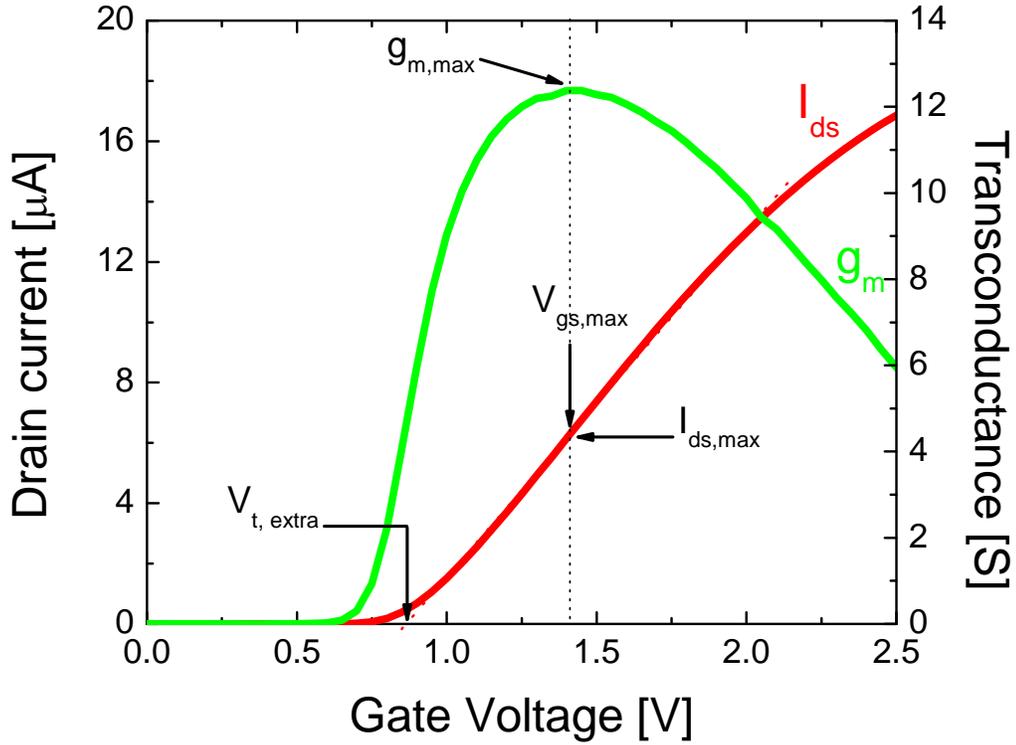


Figure 2.11 Threshold voltage determination by the linear extrapolation technique. NMOSFET with  $V_{ds} = 50\text{mV}$ ,  $EOT = 2.2\text{ nm}$ , and  $W/L = 50\mu\text{m}/10\mu\text{m}$ .

$I_{ds} - V_{gs}$  curve is then extrapolated to  $I_{ds} = 0$  from the maximum transconductance value as seen in Fig. 2.11. The ideal drain current in the linear region is expressed by

$$I_d = \mu C_{ox} \frac{W}{L} \left( V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds} \quad (2.17)$$

From this expression, the x-intercept  $V_{T,extrapolated}$  is equal to  $V_T + V_{ds}/2$ . Therefore the threshold voltage can be calculated from

$$V_T = V_{T,extrapolated} - \frac{V_{ds}}{2} \quad (2.18)$$

Equation 2.18 is valid only for negligible series resistance which is usually valid at low drain voltage (typically 20 to 50 mV) [61]. All threshold voltages reported in this work are extracted through this linear extrapolation technique.

### 2.3.2.3 Subthreshold slope measurement

The subthreshold current characteristics have become important as device dimension scale down. The drain current of a MOSFET operated at gate voltages below the threshold voltage is called subthreshold current. In this region the current varies exponentially with gate voltage expressed as [62]

$$I_{ds} = I_{d1} \exp\left(\frac{q(V_{gs} - V_T)}{nkT}\right) \left(1 - \exp\left(\frac{-qV_{ds}}{kT}\right)\right) \quad (2.19)$$

where  $I_{d1}$  is a constant depends on temperature, doping, and device dimension.

The parameter  $n$  is given by

$$n = 1 + \frac{C_d + C_{it}}{C_{ox}} \quad (2.20)$$

where  $C_d$ ,  $C_{it}$ , and  $C_{ox}$  are the depletion, interface state, and oxide capacitance respectively.

As doping density and/or interface state density increases the parameter  $n$  increases.

The inverse of the slope of the  $\log(I_{ds})$  vs.  $V_{gs}$  curve which is defined as subthreshold swing (S) is the critical parameter since this provides the amount of voltage required to switch from ‘off’ state to ‘on state. Therefore it is desirable to achieve S as small as possible. The subthreshold swing (S) is given by

$$S = \ln 10 \frac{dV_g}{d(\ln I_d)} \quad (2.21)$$

where the value is typically 70 ~ 100mV/decade in modern CMOS technology. Figure 2.12 illustrates the determination technique for subthreshold swing from the  $\log(I_{ds})$  versus  $V_{gs}$  plot.

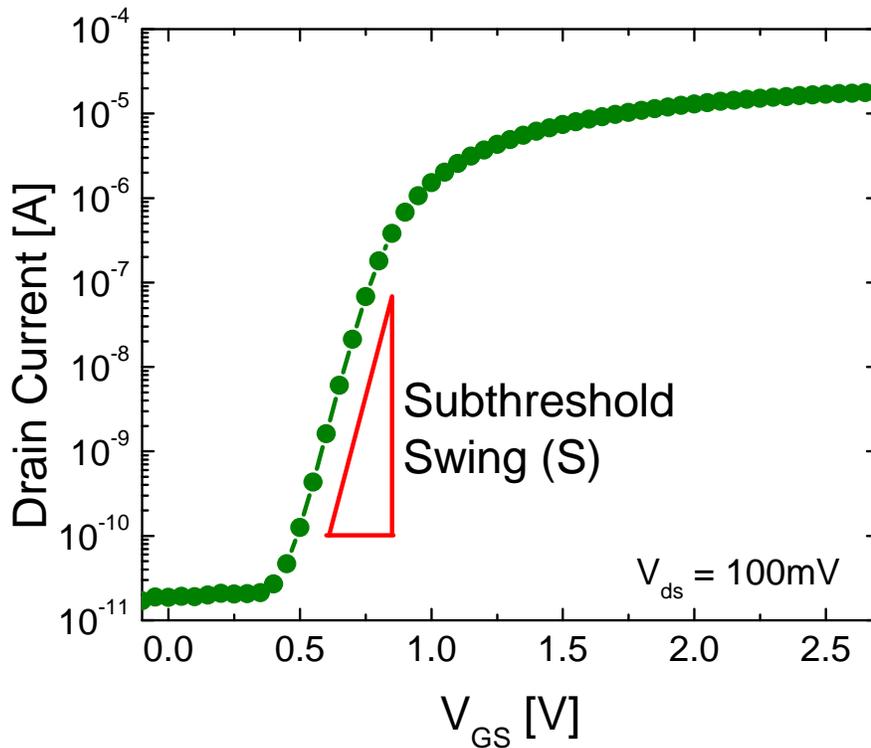


Figure 2.12 Method to determine subthreshold swing from  $\log(I_{ds})$ – $V_{gs}$  curve

## 2.3.3 Four Terminal Advanced Electrical Characterization

### 2.3.3.1 Mobility

Mobility in the inversion channel is also one of the key parameters for MOSFET devices. The actual channel mobility is deviated from the theoretical value due to the imperfect nature of the actual device which is generally called scattering. It is believed that the dominant scattering mechanisms are caused by interface charges, ionized impurities, phonons, and surface roughness. The total mobility is assumed to be dependent upon the individual component by Matthiessens's rule

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{Coul}} + \frac{1}{\mu_{Ph}} + \frac{1}{\mu_{SR}} \dots \quad (2.22)$$

and the lowest mobility dominates as shown in Fig. 2.13.

Coulomb scattering originates from various charges (fixed charge, and interface states) in gate dielectrics and ionized impurities in the depletion layer, and is mainly dominant at lower field due to the small inversion carrier densities [63]. Phonon scattering is based on the acoustic and optical mode vibrations of the lattice and has a strong impact on mobility at higher temperature and lower/moderate field [64]. Phonon scattering components in high- $k$  materials has a strong impact on mobility degradation due to the nature of highly polarized metal-oxygen bonding [65]. Surface roughness scattering originates from imperfect Si/dielectric interface. At high field the inversion carriers are pulled to the surface and mobility is limited due to the roughness of the surface [66].

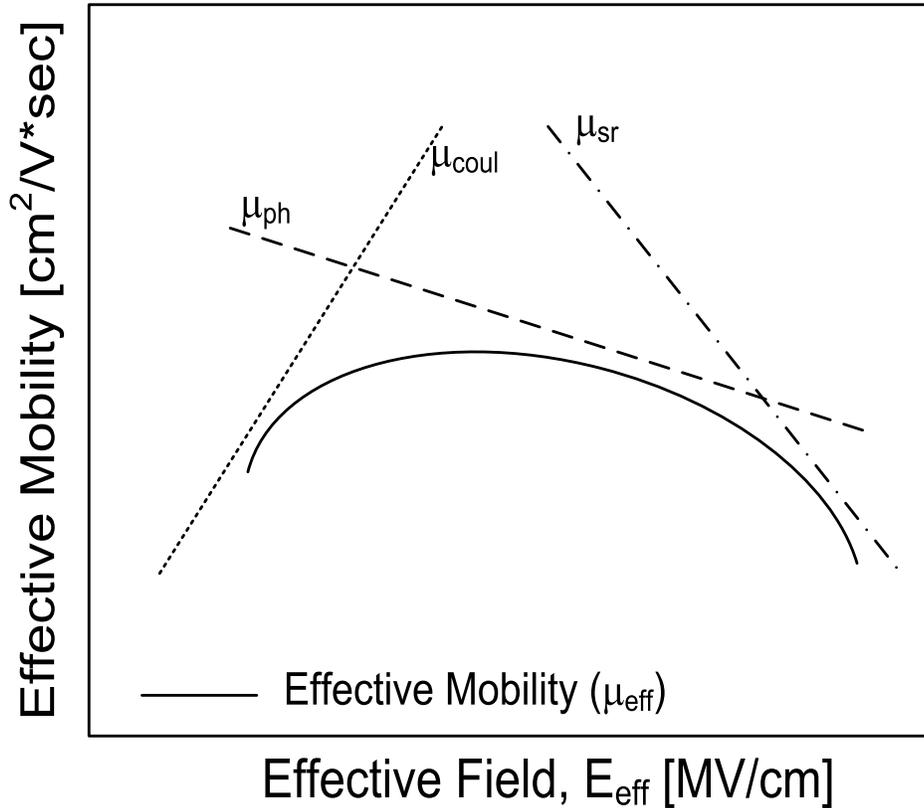


Figure 2.13 Universal mobility characteristics vs. effective field showing the impact of coulomb, phonon, and surface roughness scattering

In addition to the conventional scattering mechanisms the mobility of poly-silicon /high- $k$  dielectric stack may be degraded further by extrinsic mechanisms such as fixed charges, roughness, crystallization (and/or phase separation), and/or the presence of a dipole layer as depicted in Fig. 2.14. The scattering of the inversion charges with charges inside the high- $k$  dielectric is called remote charge scattering [67-69] since inversion carriers do not directly collide with charges in the high- $k$  layer. Nevertheless the inversion carriers can be affected by the potential disturbances created by the charge in the high- $k$  layer and hence the effective mobility degrades.

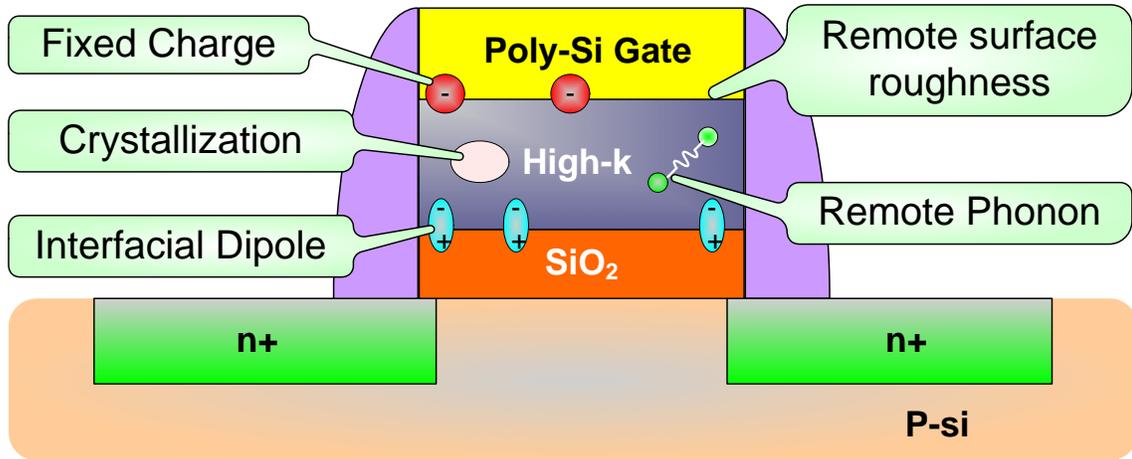


Figure 2.14 Extrinsic mobility degradation mechanisms for poly-si/high- $k$  stack

Since the channel mobility is suffered from various scattering mechanisms, it is highly desired to perform an accurate measurement to determine inversion charges precisely. As seen in Equation 2.13 the effective mobility can be determined from linear  $I_{ds}-V_{gs}$  curve as

$$\mu_{eff} = \frac{L}{W} \frac{I_d(V_g)}{V_d Q_{inv}(V_g)} = \frac{L}{W} \frac{g_d}{Q_{inv}} \quad (2.23)$$

where drain conductance is defined by

$$g_d = \left. \frac{\partial I_d}{\partial V_d} \right|_{V_{gs}=\text{constant}} \quad (2.24)$$

Therefore it is critical to measure effective channel length and width, and inversion charge of the device. It is noted that the drain voltage is kept as low as possible (typically 20 to 50mV) in order to minimize the variation of  $Q_{inv}$  near the  $V_T$ . There are several ways to determine inversion charge. One simple way to extract  $Q_{inv}$  is to use the following relationship

$$Q_{inv} = C_{ox} (V_g - V_T) \quad (2.25)$$

where  $C_{ox}$  is the oxide capacitance and  $V_T$  is the device threshold voltage. This approximation works well for large gate voltages but becomes inaccurate for gate voltages near the threshold voltage, since  $V_T$  cannot be determined exactly, resulting in inadequate estimation of true inversion charge. Traps or interface charges can also affect Equation 2.25 resulting in potential errors in inversion charge estimation. A Split C–V technique was then developed in order to directly determine the inversion charge from the inversion capacitance [69-70]. Figure 2.15 shows a typical characterization setup for the inversion charge and the depletion charge measurement. For the inversion charge measurement (Fig. 2.15 (a)), gate terminal and source/drain terminals are connected to the LCR meter while substrate terminal is grounded. The inversion charge is then extracted from the gate-to-channel capacitance ( $C_{GC}$ ) as

$$Q_{inv} = \int_{-\infty}^{V_{gs}} C_{gc} dV_{gs} \quad (2.25)$$

When  $V_{gs}$  is less than  $V_T$ , the measured capacitance is the overlap capacitance (gate-to-source and gate-to-drain). If the  $V_{gs}$  is larger than  $V_T$ , the channel is inverted and the measured capacitance is the combination of  $C_{gc}$  with  $2C_{ov}$ . Therefore subtracting  $2C_{ov}$  from the measured capacitance with integration will provide inversion charge as a function of  $V_{gs}$  as shown in Fig. 2.15 (c). Since effective mobility is usually plotted as a function of the effective transverse field at the surface, it is also necessary to determine the depletion charge along with inversion charge since the effective field is expressed as [71]

$$E_{eff} = \frac{1}{\epsilon_{Si}} (\eta Q_{inv} + Q_b) \quad (2.26)$$

where  $\epsilon_{Si}$  is the silicon permittivity and  $\eta$  is the averaging of the electric field over the electron distribution in the inversion layer. The parameter  $\eta$  is usually taken as  $\eta=1/2$  for electron mobility and  $1/3$  for the hole mobility [71-72]. For the depletion capacitance measurement, gate terminal and substrate terminal are connected to the capacitance meter while source and drain terminals are grounded as illustrated in Fig. 2.15 (b). Although  $Q_{inv}$  is accurately determined by the split C-V technique, there can be an error for mobility extraction when an ultrathin dielectric is used. Figure 2.16 shows the contribution of gate leakage current on drain current for metal gate/high- $k$  dielectric stack. As gate leakage current increases, carriers across the channel are leaking through the gate stack and as a result the drain current deviates from the saturation value at high  $V_{gs}$ . Therefore the drain current should be corrected for accurate mobility extraction by using physical based approach [73]. In this model, the substrate current is negligible since substrate current is typically small during normal operating condition. Thus it can be simply assumed that the source of gate leakage comes from the source and the drain. Since most of devices are symmetrically processed [74], gate leakage current can be expressed as the sum of the gate to source ( $I_{gs}$ ) and gate to drain ( $I_{gd}$ ) current.

$$I_g = I_{gs} + I_{gd} \quad (2.27)$$

and also

$$I_{gs} = I_{gd} = \frac{I_g}{2} \quad (2.28)$$

Therefore, the gate leakage current corrected drain current can be represented as

$$I_{d,corrected} = I_{d,measured} + \frac{I_g}{2} \quad (2.29)$$

And the result is plotted in Fig. 2.16.

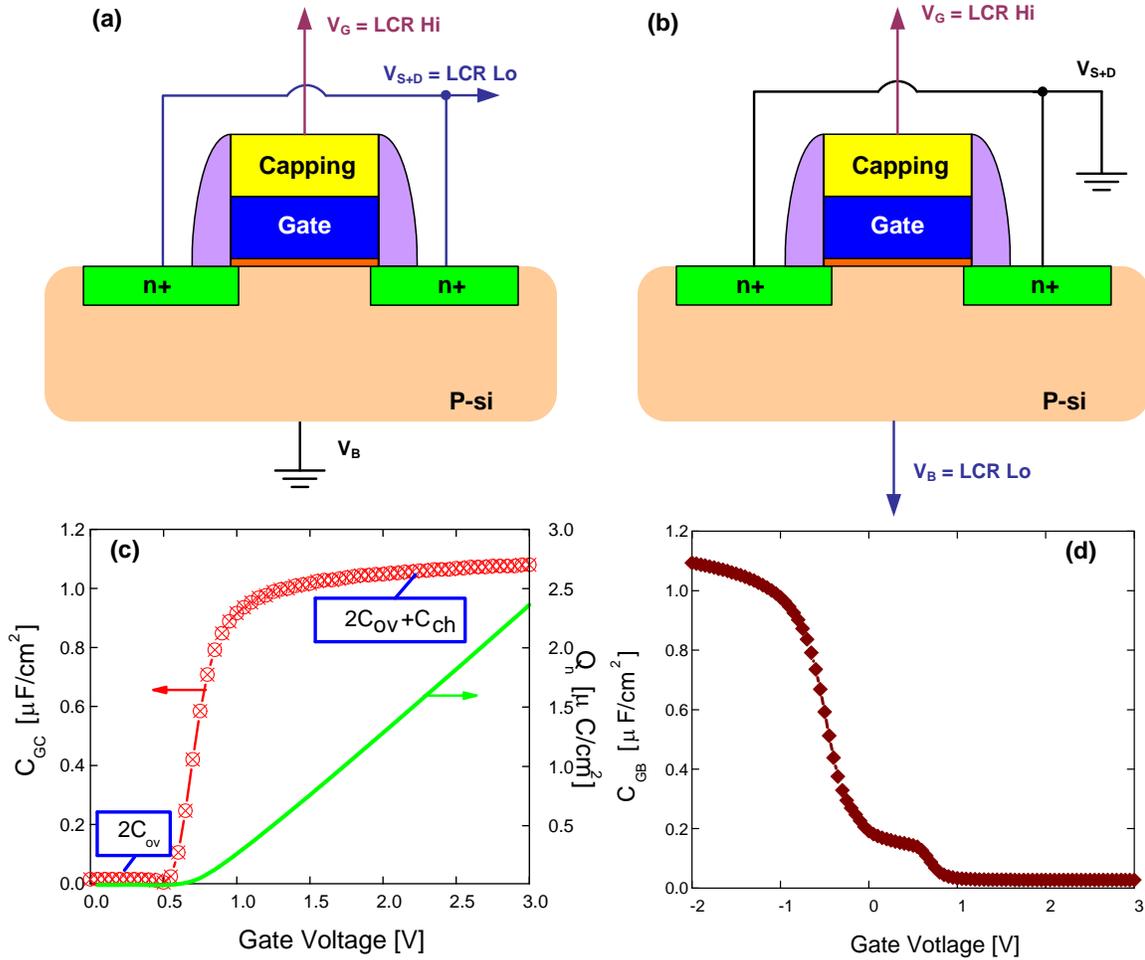


Figure 2.15 Measurement setups of Split C–V technique for (a) gate-to-channel capacitance ( $C_{gc}$ ), (b) Gate-to-bulk capacitance ( $C_{gb}$ ), (c) examples of measured  $C_{gc}$  and extracted  $Q_{inv}$ , and (d) example of  $C_{gb}$  measurement.

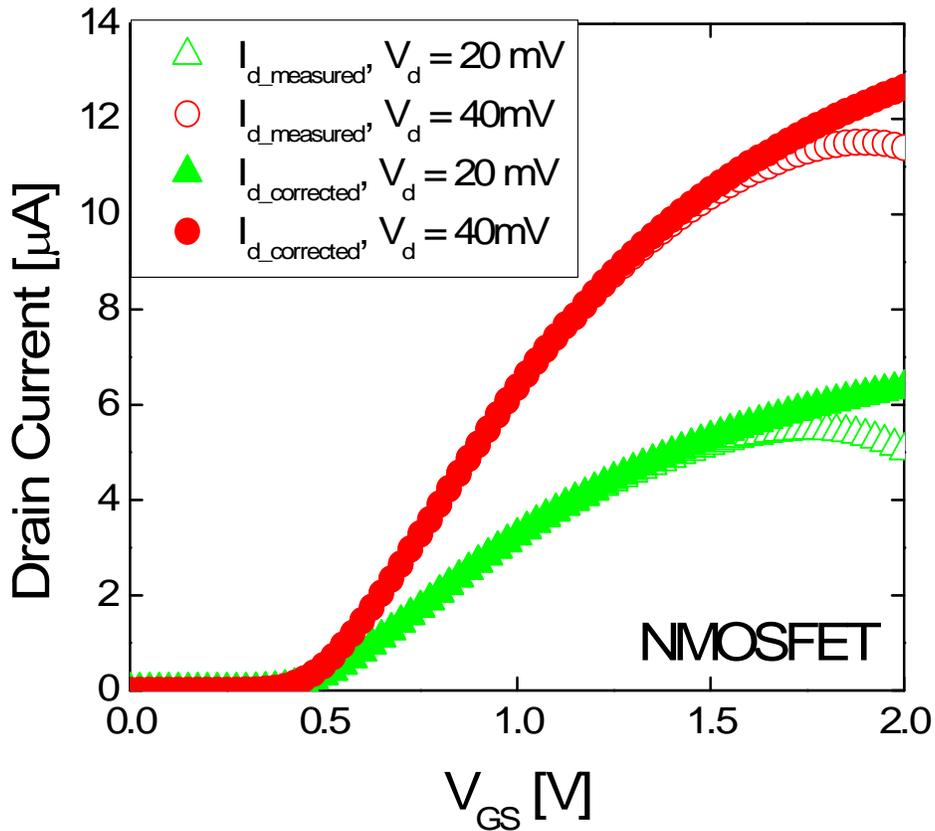


Figure 2.16  $I_{ds} - V_{gs}$  characteristics with measured and leakage current corrected curve.

### 2.3.3.2 Charge pumping (basic sweep and amplitude sweep)

The charge pumping (CP) measurement technique was developed in the late 1960's [75] but it was not popular until practical and reliable interpretation was introduced [76]. The charge pumping measurement can provide very detailed and accurate information about Si/dielectric interface in terms of trap density and distribution. Moreover, it has become a powerful characterization technique with high- $k$  based dielectrics since it provides not only the interface trap information but also response from the bulk traps in the high- $k$  layer.

Figure 2.17 (a) and (c) show basic measurement setup for the two-level base level sweep charge pumping method and the corresponding plots. A pulse train can be applied to the gate of the MOS transistor while source/drain can be grounded or slightly reverse biased. The substrate current is then monitored as function of voltage from inversion (accumulation) to accumulation (inversion). The amplitude of the pulse can be chosen such that the device can be driven from inversion to accumulation or vice versa. The charge pumping characteristic is based on the Shockley Reed Hall (S-R-H) statistics of recombination process [75]. When transistor is pulsed into the inversion region, the minority carriers flow from source to drain over the channel but some of the minority carriers are captured by pre-existing interface traps. Some of captured minority carriers in interface states near the band edge can emit into conduction band (in case of electron) or valence band (in case of hole). Emitted carriers then become free carriers, but the minority carriers captured deeper in the bandgap do not have sufficient time to escape the traps and hence remain captured. A pulse is then applied to the gate in order to drive channel into the accumulation region, and the minority carriers in the channel drift back to the source and drain. However, the carriers that are captured in the interface traps will recombine with the majority carrier from the substrate. This process can generate a net flow of the charges into substrate and the expression is given by

$$Q_{cp} = qA \int_{E_{f,acc}}^{E_{f,inv}} D_{it}(E)dE \quad (2.30)$$

where  $q$  is the electron charge,  $A$  is the gate area,  $D_{it}$  is the interface state density, and  $E_{f,inv}$  and  $E_{f,acc}$  are the Fermi level in the inversion and the accumulation respectively. When

applying repetitive pulses with frequency  $f$ ,  $Q_{cp}$  will give rise to a net dc current in the substrate written as

$$I_{cp} = fQ_{cp} = fqA\overline{D_{it}}\Delta E \quad (2.31)$$

Where  $\overline{D_{it}}$  is the average interface trap density over energy range  $\Delta E = E_{f,inv} - E_{f,acc}$ .

It is noted that this substrate current can be affected by the amplitude, rise/fall time, frequency, and duty cycle of the applied pulse. When the pulse is in accumulation or inversion, there is no recombination resulting in very low charge pumping current. When gate pulse starts to swing into the bandgap, the recombination process starts and hence results in increase of charge pumping current. When the pulse sweeps between  $V_T$  and  $V_{FB}$  the maximum recombination takes place providing saturation charge pumping current. By plotting charge pumping current as a function of base level (shown in Fig. 2.17 (c)), a hat shape of curve is obtained where the one edge of the curve occurs at  $V_T - \Delta V_{peak}$  and the other edge of the curve occurs at  $V_{FB}$ . Therefore, the average interface state density can be extracted from the saturated maximum charge pumping current based on Equation 2.31.

Another two level charge pumping method is called variable amplitude (VA) sweep with fixed base level as shown in Fig. 2.17 (b) and (d). With the VA technique the charge pumping current strongly depends on the frequency especially for high- $k$  dielectrics due to the pre-existing traps as shown in Fig. 2.17 (d). It is noted that as frequency decreases the electrons have more time to be injected further into bulk trap sites as well as to be released from the bulk traps and contribute the recombination current. Since this frequency dependency of charge pumping current is observed only with high- $k$  dielectrics, the charge

pumping has become the essential characterization method for MOSFETs with advanced gate stacks.

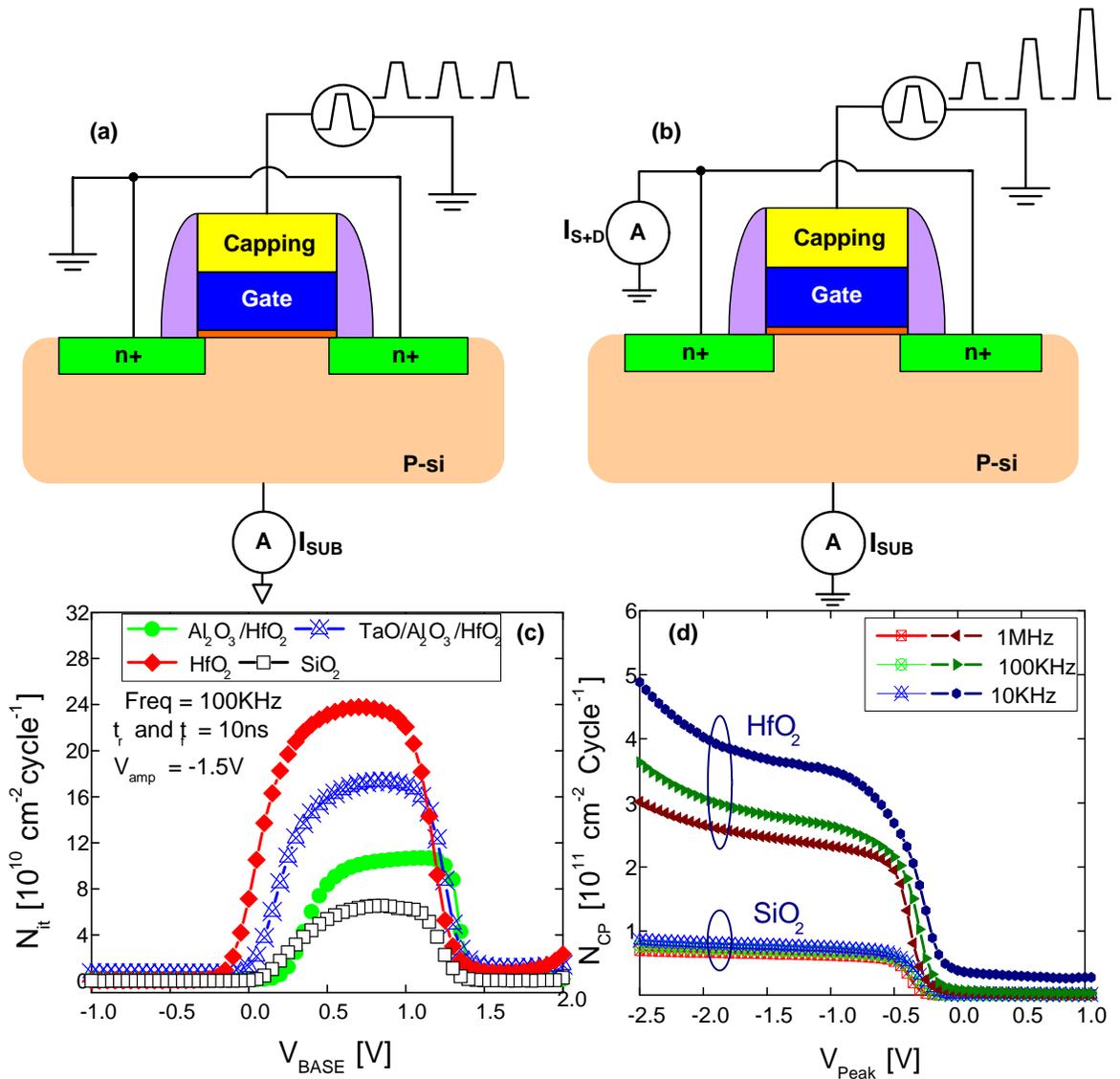
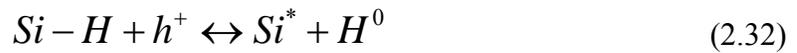


Figure 2.17 Schematic illustration of charge pumping method for (a) fixed amplitude with base level sweep charge pumping, (b) fixed base level with various amplitude sweep, (c) typical base level charge pumping curve, and (d) various amplitude charge pumping curve with  $\text{SiO}_2$  and  $\text{HfO}_2$  dielectrics.

### 2.3.3.3 Bias Temperature Instability

Reliability of the MOSFET devices are also very important since key parameters such as  $V_T$ ,  $I_{d,sat}$ , and  $g_m$  have to be stable for a certain amount of time. High- $k$  dielectrics have inherent defect states and these defects can significantly affect device reliability for both nMOS and pMOS.

Negative Bias Temperature Instability (NBTI) is a significant reliability concern for current CMOS based technology. NBTI occurs in negatively biased pMOSFET due to the generation of the interface traps at the Si/oxide interface at elevated temperatures. As a result the  $V_T$  of the device is shifted towards higher values over time causing transconductance reduction and corresponding drive current degradation. Several models have been proposed to explain NBTI degradation behavior. Among them the reaction-diffusion (R-D) model is widely accepted NBTI model based on the reaction of Si-H bonds with holes at Si/SiO<sub>2</sub> interface [77-85]. In a conventional Si/SiO<sub>2</sub> MOSFET, Si atoms are bonded to either oxygen (from SiO<sub>2</sub>) or Hydrogen (from forming gas annealing) at the Si/oxide interface as shown in Fig 2.18. In the R-D model, the interface trap generation at the Si-SiO<sub>2</sub> interface is expressed as a chemical reaction



Under the higher field and/or at elevated temperature, inversion carriers (hole,  $h^+$ ) of pMOS devices interact with interface bonds resulting in weakening or broken of Si-H bonds. When the Si-H bonds are broken, detached hydrogen can diffuse into the oxide layer or anneal existing traps, and interface silicon atoms become dangling due to the unsaturated

electron resulting in interface charges. The interface trap density,  $N_{it}$ , increases with the net rate of the reaction given in equation (2.32), so

$$\frac{dN_{it}}{dt} = k_f (N_0 - N_{it}) - k_r N_H^0 N_{it} \quad (2.33)$$

where  $k_f$ ,  $k_r$ ,  $N_0$ , and  $N_H^0$  are Si-H bonds breaking rate, Si-H bonds annealing rate, the initial Si-H bond density at the interface, and Si-H bond density after stressing.

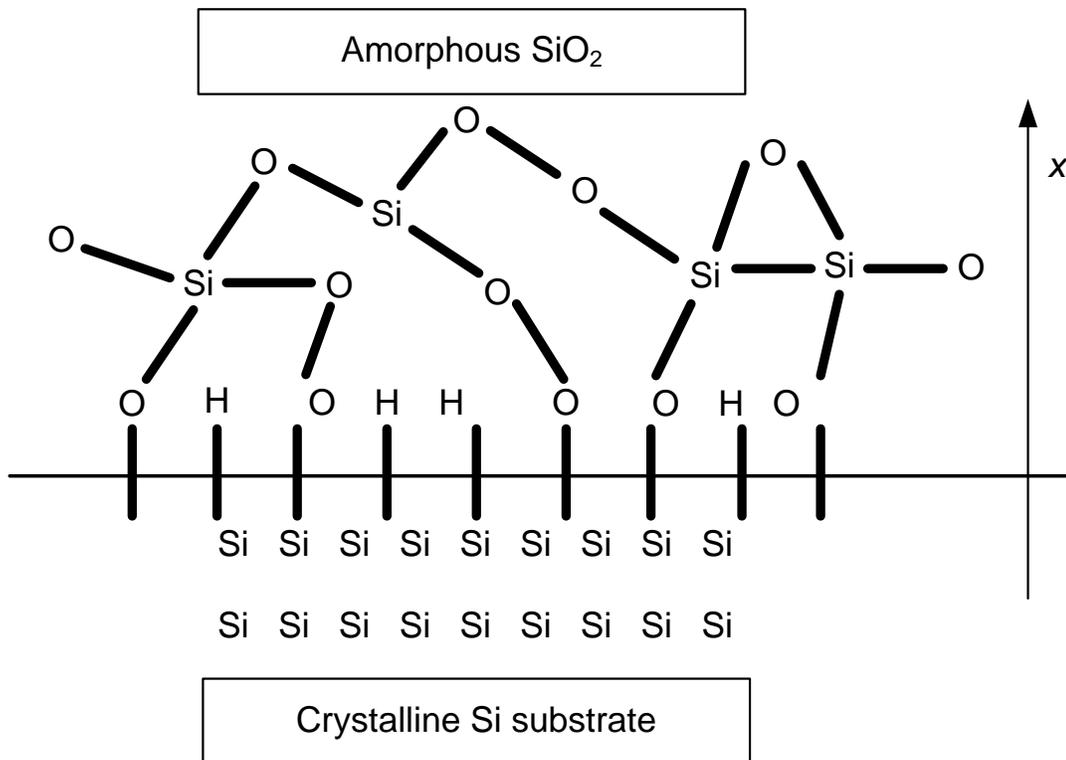


Figure 2.18 Schematic of Si/SiO<sub>2</sub> interface after FGA. Si dangling bonds created by the mismatch between crystalline Si and amorphous oxide are passivated by hydrogen.

When a device is stressed, both  $N_{it}$  and  $N_H^0$  are negligible as compared to  $N_0$ . Therefore the increase in  $N_{it}$  is generation limited. When sufficient hydrogen is built up at

the interface, hydrogen starts to diffuse from the interface and hence the interface trap generation rate is limited by the diffusion of hydrogen. For this period, the diffusion of hydrogen obeys

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} \quad (2.34)$$

where  $D_H$  is the diffusion coefficient of hydrogen and  $x$  is the distance into the dielectric. If all the Si-H bonds are broken (in case of  $N_{it} \approx N_0$ ), then the interface trap generation rate is slowed down and eventually saturated. The general interface trap generation characteristic over time is shown in Fig 2.19 taken from [83]. It is noted that the  $N_{it}$  generation in region (i) and (ii) is very quick and not observed in typical experimental measurements. It is also noted that the oxide field dependence of NBTI is incorporated in factor  $k_r$  and the temperature dependence is included through activation energies of  $k_f$ ,  $k_r$ , and  $D_H$  [81]. During the diffusion dominated period,  $N_{it}$  generation as a function of time can be derived from the triangle approximation and expressed as

$$N_{it}(t) = \sqrt{\frac{k_f N_0}{2k_r}} (D_H t)^{\frac{1}{4}} \quad (2.35)$$

which gives the time exponent ( $n=0.25$ ) of NBTI when only H diffusion is taken into account. However, this result is not fitted well with experimental data since atomic hydrogen is unstable and thus atomic hydrogen should be converted to molecular  $H_2$  after releasing from the interface [81-82, 84]. It has also reported that the activation energy extracted from NBTI measurements supports the dominant diffusion species is  $H_2$  [85-86]. Although  $H_2$  is

dominant species rather than H, it still follows R – D model. Therefore the interface generation over time can be represented as

$$N_{it}(t) \propto \left( \frac{k_f N_0}{k_r} \right)^{\frac{2}{3}} (D_{H_2} t)^{\frac{1}{6}} \quad (2.36)$$

which the time exponent ( n=0.17) is consistent with experimental data.

It is shown that the NBTI degradation behavior with high-*k* dielectrics is similar to SiO<sub>2</sub> based dielectrics and hence the degradation behavior over time with high-*k*/metal gate stacks can be explained by the reaction-diffusion model. [87]. However, the effect of bulk charges should also be considered when dealing with thick high-*k* layer (more than 2nm) [88-89].

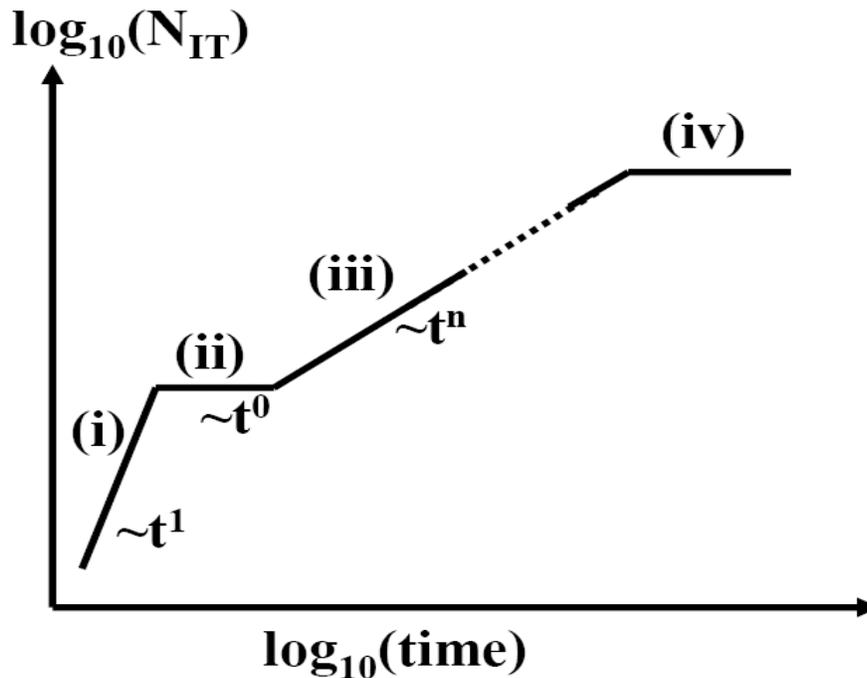


Figure 2.19 Schematic of time evolution of the R – D model. Regions (i) generation limited, (ii) dynamic equilibrium, (iii) diffusion limited, and (iv) saturation after [85]. Typical NBTI time evolution follows power law in region (iii).

The NBTI test in this work was done using Keithley SCS-4200 system with switching matrix at elevated temperatures as shown in Fig. 2.20. Conventional stress and sense techniques were used where linear  $I_{ds}-V_{gs}$  curves along with charge pumping are measured after stressing. It is important to note that the delay between switching has been minimized in order to avoid recovery effects. Due to the limitation of characterization system the delay time was about 0.7 s between stress and sensing expecting that there is some recovery effect of interface state. Therefore subthreshold characteristics were also used as an alternate method for obtaining the interface state generation characteristics. The subthreshold swing (S) was defined in section 2.3.2 and the parameter  $n$  is related to an interface state capacitance which can be expressed as  $qN_{it}$ .

$$S = 2.3 \frac{nkT}{q} = 2.3 \frac{kT}{q} \left( 1 + \frac{C_d + C_{it}}{C_{ox}} \right) \quad (2.37)$$

The change in subthreshold swing due to the change in interface state density is then expressed as

$$\delta S = 2.3 \frac{kT}{q} \frac{\delta N_{it}}{C_{ox}} \quad (2.38)$$

assuming the depletion layer capacitance is constant. During the  $I_{ds}-V_{gs}$  measurement, the subthreshold swing changes with gate bias if interface traps are present. Therefore if the change of interface state density after certain stress time is monitored, one can expect a linear relation between the change in subthreshold swing log (dS) and the log of stress time. The longer the MOSFET is stressed, the more silicon hydrogen bonds are broken by inversion charges resulting in higher interface state density, hence increasing dS.

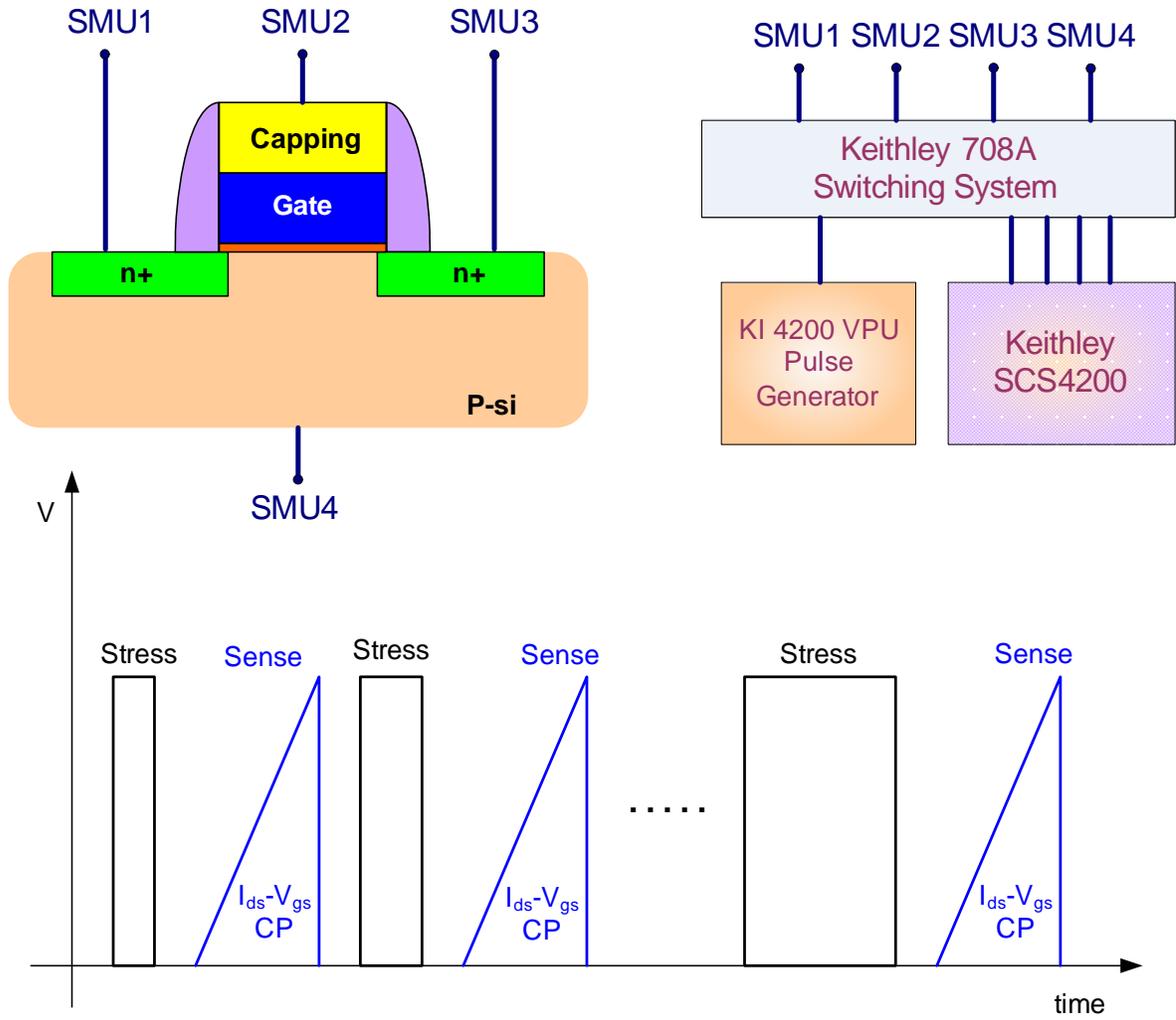


Figure 2.20 Measurement setup for NBTI test.

## 2.4 Analytical Characterization

### 2.4.1 X-Ray Photoelectron Spectroscopy (XPS)

X-Ray Photoelectron Spectroscopy (XPS) or Electron Spectroscopy for Chemical Analysis (ESCA) is known to be one of the most powerful techniques to analyze chemical information in ultrathin high- $k$  oxides or at the surface [90-91]. Figure 2.21 demonstrates the electron emission process and the typical measurement system. While sample is irradiated with monochromatic Mg or Al X-ray, the kinetic energy (KE) of electrons ejected from the sample is simultaneously measured. The total energy is express by

$$BE = h\nu - KE - \phi_s \quad (2.39)$$

where  $h\nu$  is the photon energy, BE is the binding energy of the sample which is the minimum energy required for breaking the chemical bonds of molecule, and  $\phi_s$  is the spectrometer work function. Since the measured kinetic energy of the collected electrons is based on the Fermi level of a spectrometer, the work function of the spectrometer should be considered to obtain proper binding energy. The acquired energy spectrum provides chemical state information because different bonding varies the valence electron charge distribution which affects the core level potentials. This change in core level potentials results in the kinetic energy needed for valence electron to be emitted. Therefore the chemical state information can be obtained by comparing obtained binding energy (or kinetic energy) of the atom to the reference. Angle dependent photoemission (angle-resolve XPS) uses sample tilting to vary the take-off angle at which the electrons are collected by the detector relative

to sample surface normal. Non-destructive depth profiling can be obtained by using AR-XPS technique. However, XPS on insulating materials can create charging effect at the surface resulting in relative BE shift. Therefore this should be compensated before or after data acquisition by using charge neutralizer or known reference peak such as surface carbon or Si substrate.

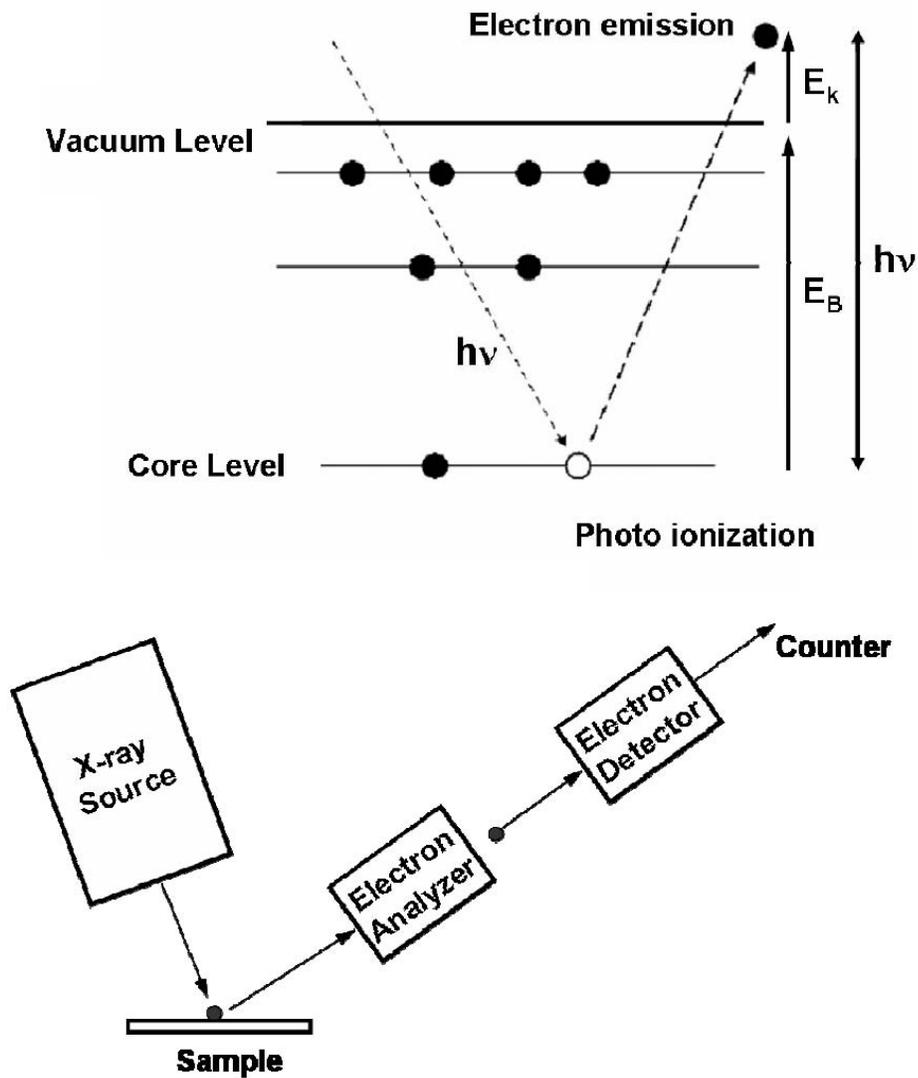


Figure 2.21 Schematic of photoelectron emission process and XPS measurement setup taken from [56]

### 2.4.2 X-Ray Diffraction (XRD) Analysis

The X-ray diffraction technique is used to determine material structures such as crystalline, poly-crystalline, or amorphous. Incident x-ray beam is diffracted from the atomic planes at a certain angle satisfying Bragg's formula as

$$2d \sin \theta = n\lambda \quad (2.40)$$

where  $d$  is atomic distance,  $\theta$  is the angle, and  $\lambda$  is the wave length. Since each atomic plane has a unique  $\theta$  value, it allows us to determine crystal structure as well as phases. X-ray diffraction peaks are obtained if constructive interference is formed between two reflected X-rays by the parallel crystal planes.

X-ray Diffraction used in this work was conducted with a Bruker D-5000 diffractometer equipped with HighStar wide area detector. Cu-K $\alpha$  radiation was used for X-ray source generated at 40 kV and 30 mA. The area detector enables the scattered X-rays to be collected over approximately  $35^\circ 2\theta$  and  $45^\circ \chi$  simultaneously.

### 2.4.3 Backside SIMS

The Secondary Ion Mass Spectrometry (SIMS) technique is used to determine chemical composition of the sample by using primary ion beam (typically Cs<sup>+</sup> or O<sup>-</sup>) to sputter materials [56, 92]. When energetic primary ion bombards a sample surface, various atoms and molecules escape from the surface. A small portion of the escaped species are ionized and extracted by an electric field. These secondary ions are then separated and are detected by a mass spectrometer providing useful information about the sample. The main

advantage of SIMS is quantitative depth profiling with lower detection limits on the order of  $10^{14} \sim 10^{15} \text{ cm}^{-3}$ . However, the data acquired from conventional front-side SIMS technique with advanced gate stacks (metal gate and ultrathin high- $k$ ) can be altered by matrix effects from different elements in new material, surface roughness of the sample, and decrease in resolution, which makes the analysis of new materials difficult.

In order to minimize issues associated with front-side SIMS technique, backside SIMS technique was introduced. For backside SIMS, sample preparation included mechanical polishing from the Si substrate to 200nm of Si/oxide interface. Backside SIMS technique can provide useful information such as Si-high- $k$  reaction, intermixing of high- $k$ , and metal penetration from the gate electrode.

#### **2.4.4 Transmission Electron Microscopy (TEM)**

The Transmission Electron Microscopy (TEM) technique was used to examine the cross section of the metal gate / high- $k$  dielectric stack. In TEM technique, electron beams are focused on the sample by electromagnetic lenses. Since the wavelength of electron beam is less than that of visible ray, the resolution of TEM is higher than optical microscope [56]. The sample thickness should be thin enough so that the electron beam is transmitted through the sample and hence the special sample preparation is required.

Generally, High Resolution TEM (HR-TRM) combines phase contrast from elastic scattering events and mass-thickness contrast from inelastic scattering. A TEM equipped with the image filter can filter out inelastic scattered electrons for high resolution (HR)

images. Therefore, image-filtered HRTEM provides almost pure phase contrast, which shows better crystallographic structures, planar defects and strain fields information at the atomic scale. However, for samples with multiple amorphous layers, where the contrast can only come from mass-thickness contrast, HRTEM is not sufficient to investigate those layers and image-filtered HRTEM is even worse.

Z-contrast in Scanning TEM (STEM) mode can overcome the issues with phase contrast HRTEM imaging since a fine beam is scanned across the sample in a raster manner similar to conventional scanning electron microscopy (SEM). During the scan scattered high angle, low angle, and surface secondary electron signals are collected using high angle angular dark field (HAADF), low angle ADF (LAADF), and Everhart-Thorley detectors. In HAADF mode the elastic Bragg scattering is reduced so the image strongly depends on the sample mass ( $\sim Z^2$ ) providing good compositional and chemical contrasts in atomic scale. HAADF images are called Z-contrast images.

Samples were prepared by using FEI Quanta 200 3D Focused Ion Beam (FIB) system. Both HR-TEM and z-contrast STEM imaging were performed using a field-emission TEM equipped with a Gatan imaging filter (GIF) and at 200 kV of accelerating voltage. Prior to load sample to the TEM, samples were treated and cleaned in oxygen plasma to remove the contamination like carbon.

## **2.5 Summary**

This chapter reviewed the deposition techniques for metal gates and high-k dielectrics, sample fabrication process, and characterization method used in this dissertation.

## Chapter 3

# The role of Rare Earth Metal (RE=Gadolinium and Europium) on Effective Work function modulation of Ni-FUSI / High- $k$ dielectric stacks

### *Abstract*

It was found that the structural properties with Gadolinium (Gd) and Europium (Eu) incorporation into Nickel (Ni) Fully Silicided (FUSI) gate electrodes are markedly different and resulted in different degrees of effective work function modulation. It was found that Ni-Gd alloys tend to form stable compounds during silicidation and produced a Si-rich layer with amorphous/nanocrystalline structure near the FUSI gate/high- $k$  dielectric interface. This compositional and structural change is the main mechanism responsible for effective work function modulation with Gd incorporation. However, in the case of Europium, Eu atoms tend to segregate outside the Ni-FUSI layer during silicidation and resulted in a uniform  $\text{Ni}_x\text{Si}_y$  layer with Eu pile-up layer at the FUSI gate electrode / high- $k$  dielectric interface. This pile-up is believed to be the main cause of effective work function modulation with Eu incorporation. It was also found that the incorporation of Gd and Eu metals in Ni-FUSI gate remotely scavenge the interfacial oxide layer resulting in lower EOT of the device.

### 3.1 Introduction

Fully silicided (FUSI) metal gate electrodes for dual gate CMOS application have been the focus of many research groups [93-96]. The major advantage of FUSI gate approach is the fabrication process compatibility with current CMOS technology. Over the years, research on FUSI gates has focused on achieving a large range of effective work function ( $\phi_{m, \text{eff}}$ ) tuning on various dielectrics. Nickel based FUSI gate electrodes with various dopants (As, Sb, and B) were initially introduced on SiO<sub>2</sub> based dielectrics to modulate effective work function from the undoped NiSi gate work function (near midgap) [94]. However, it was reported that the degree of effective work function modulation is decreased on hafnium based dielectrics with the same FUSI gate electrode [97]. Rare-earth metals typically have low vacuum work functions ranging from 2.5 eV to 3.4 eV and their silicides can be formed at lower temperatures as compared to NiSi [40, 98]. However, unlike NiSi, most rare-earth silicides involve Si as the dominant moving species which can result in void formation at the dielectric-electrode interface. One way to obtain both a low work function and minimize voiding issue is to form silicides from binary alloys of Ni and rare earth metals since the presence of both Ni and rare earth metal is expected to significantly impact the diffusion kinetics of the moving species.

We have chosen Gd and Eu since they provide both similarities and differences in their physical properties such as vacuum work function, valency, atomic radii, and different rates of reactions with Ni as shown in Fig 3.1. Hence, comparing these two RE elements can lead insight into the structure-property relationship of RE incorporation approach. In this

chapter, we have investigated not only the role of RE metals in Ni-based FUSI but also the physical mechanism on effective work function modulation as a potential candidate for N-channel MOS devices on  $\text{HfSiO}_x$  dielectrics.

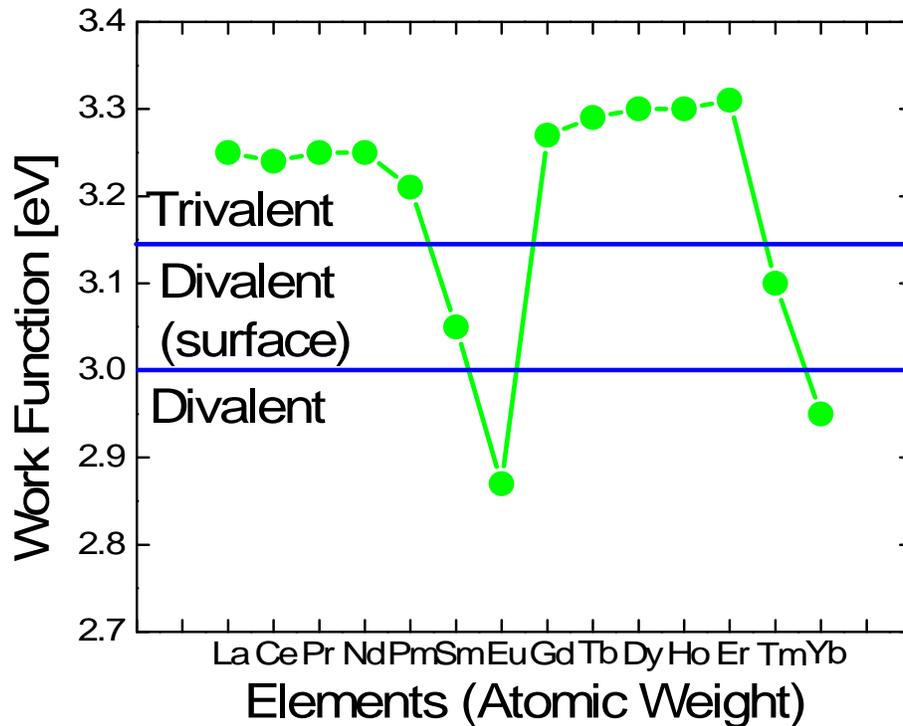


Figure 3.1 Vacuum work function values for Rare-Earth Metals. It also indicates the valency of the metals. Eu and Yb are divalent metals and hence show the lowest work function.

### 3.2 Experiments

$\text{HfSiO}_x$  with 30%  $\text{SiO}_2$  dielectrics deposited by atomic layer deposition (ALD) on p-type Si (001) substrates were received from Texas Instruments. Un-doped Si was deposited using CVD methods. Prior to loading the samples into the deposition tool, a 1 % HF dip was

done to remove the native oxide at the Si surface. NiGd and NiEu alloy metals were deposited in-situ by RF magnetron sputtering system from 2 in. diameter targets in an Ar ambient. The base pressure of the chamber was  $7 \times 10^{-9}$  Torr and the deposition pressure was 5.5mTorr. The composition of the alloys was controlled by sputter power of the Ni and RE based on the deposition rate of each metal and three different alloy compositions were used as Ni (90%) – RE (10%), Ni (80%) – RE (20%) and Ni (70%) – RE (30%). The metal sputtering rates were also controlled so that the total metal thickness was to be 30 nm. The ratio of the metal layer to undoped Si layer was chosen to ensure that the underlying Si would be fully consumed. Following the NiRE deposition, in-situ tungsten (W) capping layer was deposited to prevent oxidation during to silicidation process and also to ensure good electrical contact. Pure Ni films were also sputtered on undoped Si layers as controls. After gate patterning via photolithography, silicidation was achieved by rapid thermal annealing (RTA) at 450°C in an Ar ambient for 1min. Capacitance–voltage (C–V) and current–voltage (I–V) characteristics were measured using HP 4284 LCR meter and HP 4155 meter respectively. Flatband voltages ( $V_{FB}$ ) and equivalent oxide thickness (EOT) values were extracted using NCSU C–V program [99]. Systematic material characterization techniques such as X-Ray Diffraction (XRD), Auger Electron Spectroscopy (AES) depth profiling, and Backside Secondary Ion Mass Spectroscopy (SIMS) analysis were used to analyze the material properties of the gate electrodes.

### 3.3 Results and Discussion

#### 3.3.1 Impact of Gd incorporation on effective work function

Figure 3.2 shows the  $V_{FB}$  vs. EOT plots obtained from typical capacitance–voltage (C-V) curves at high frequency for NiGd/Si/HfSiO<sub>x</sub>/Si capacitors. An estimate of the effective work function values was obtained from the y-intercept of the  $V_{FB}$  vs. EOT plots.

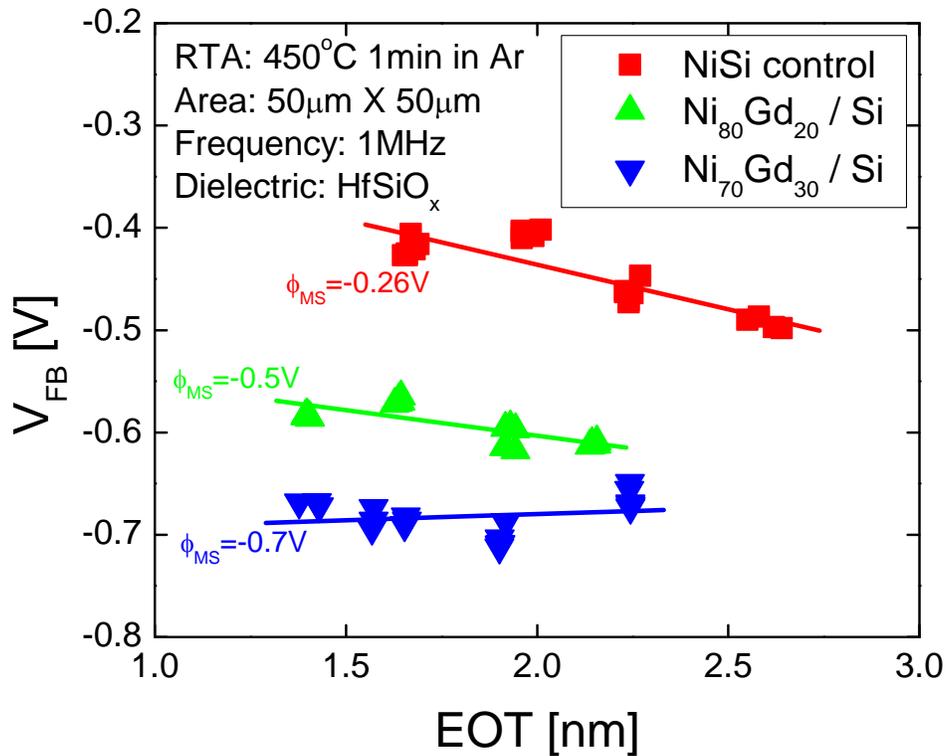


Figure 3.2 Flatband ( $V_{FB}$ ) voltage versus EOT plot for 500Å W / 300Å Ni<sub>1-x</sub>Gd<sub>x</sub> / 300Å Si on HfSiO<sub>x</sub>/SiO<sub>2</sub> dielectrics (x varies from 0 to 30) after 450 °C RTA annealing.

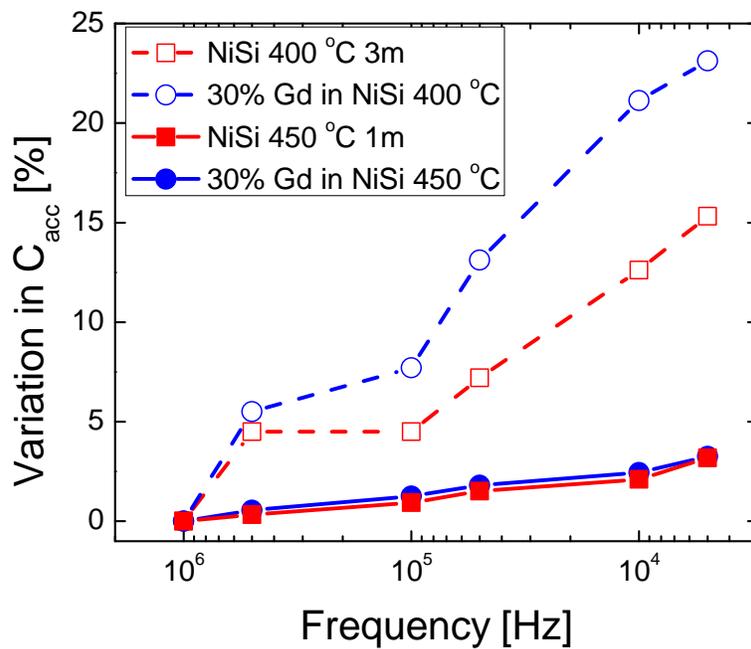
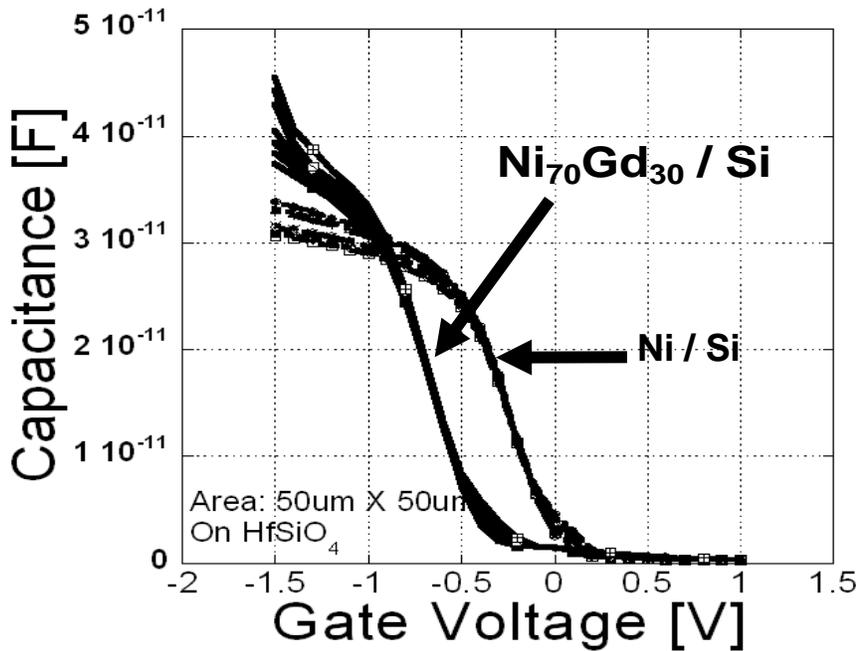


Figure 3.3 (a) C–V curve with frequencies for NiSi and 30% Gd incorporated NiSi.  $V_{\text{FB}}$  modulation is clearly obtained with Gd incorporation with similar level of  $D_{\text{it}}$  response. (b) Variation of accumulation capacitance for 400 °C and 450 °C silicidation annealing. Larger variation in  $C_{\text{acc}}$  indicates incomplete silicidation of Si. Un-doped Si layer act like semi-insulating material resulting in dependence in applying frequency, and (b) C – V curves with frequencies.

No correction for charges that maybe present at the various interfaces was applied since the error associated with these is minimal due to the low EOTs involved. The variation of frequency dispersion taken from the accumulation capacitance of the C–V curve was negligible as seen in Fig. 3.3 and suggested that full silicidation was indeed occurring at the RTA conditions used for the samples. It also indicates that the Si–dielectric interface has a low density of states suggesting that Gd does not diffuse through to the SiO<sub>2</sub>/Si interface.

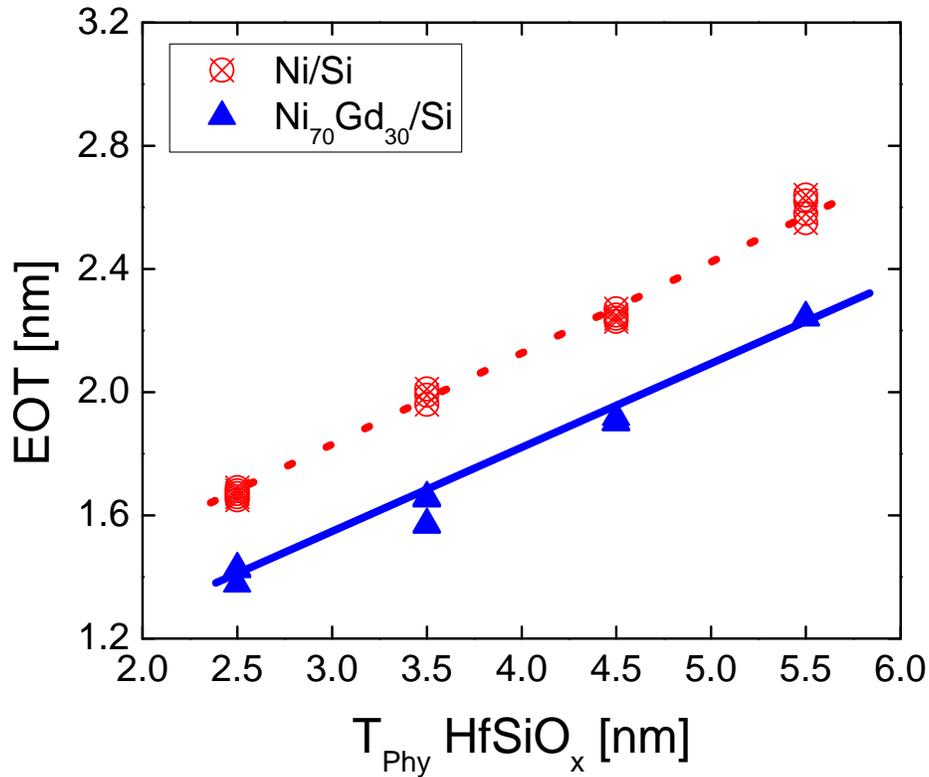


Figure 3.4 EOT vs. physical thickness of HfSiO<sub>x</sub> dielectric for NiSi control and 30% Gd incorporated NiSi gate. Y-intercept corresponds to the interfacial layer thickness and the slope is related to the charge profile. Interfacial layer is decreased with Gd presence whereas the slope is stayed.

As evident from Figure 3.2, a decrease in EOT was observed as the Gd percentage increased suggesting potential reactions between the gate electrode and dielectric. In order to evaluate the cause of reduction in EOT, the extracted EOT of  $\text{HfSiO}_x$  was plotted vs. physical thickness of the  $\text{HfSiO}_x$  for NiSi control and 30% Gd incorporated NiSi gate. As shown in Figure 3.4, the y-intercept of this plot leads to the interfacial layer thickness and the slope of this plot is related to the dielectric constant of the film. As Gd is presented, only the intercept changes while minimal impact on the slope indicating that the Gd is scavenging the  $\text{SiO}_2$  rich interfacial layer. The extracted interfacial layer thickness decreased from 11 Å to 7 Å as Gd percentage increased from 0 percent to 30 percent. The difference in interfacial layer thickness corresponds well to the decrease observed in EOT. To gain further insight into the cause of reduction in EOT, high resolution TEM (HRTEM) was performed. The HRTEM image for the control Ni-Si sample as shown in Figure 3.5 (a) shows the presence of an interfacial layer both underneath and on top of the high- $k$  dielectric. Although the origin of this interfacial layer is not fully understood, it is believed to be related to the presence of Si which may get oxidized during the FUSI process. In contrast to the control Ni-FUSI, the Ni-Gd FUSI sample with 30% Gd, shown in Figure 3.5 (b), depicts a marked reduction in the thickness of the top and bottom interfacial layers and also in the thickness of the high- $k$  layer itself. Backside SIMS analysis (Figure 3.6) was also performed on 30% Gd Ni-FUSI sample in order to monitor the profile of Gd, Ni, and Si after annealing. It is clearly shown that no evidence of Gd diffusion into the bottom interfacial layer or Si substrate was observed. Furthermore, the Ni signal precedes the Gd signal indicating that Gd does not accumulate at the dielectric-gate electrode interface.

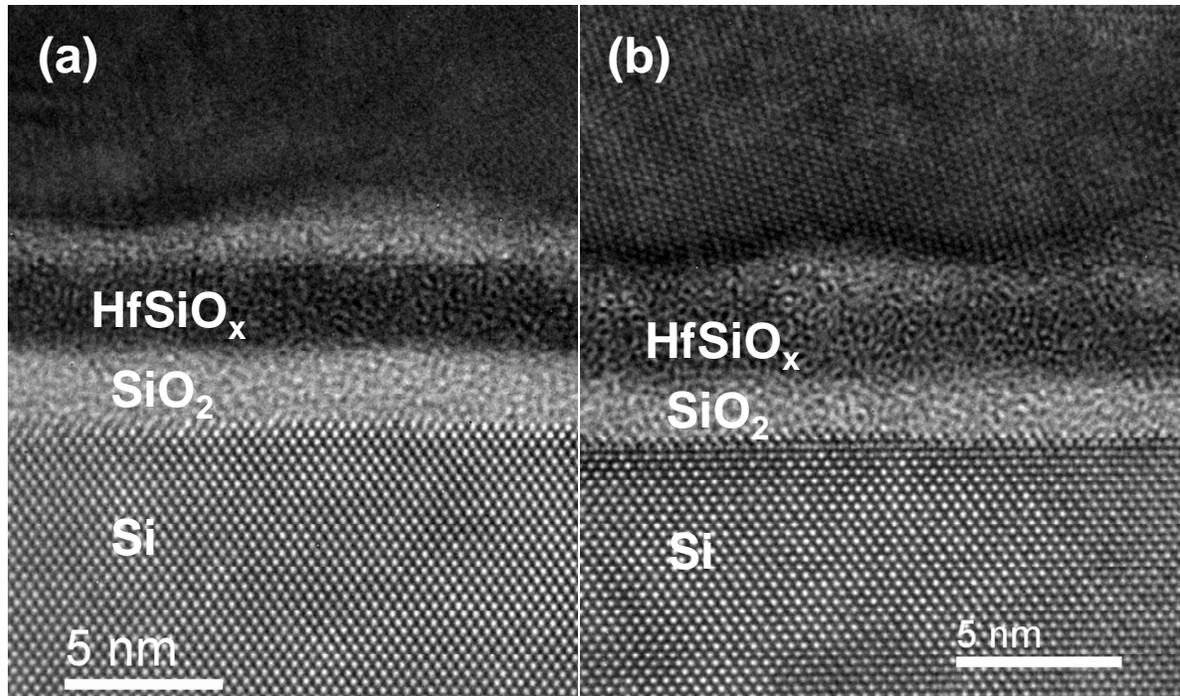


Figure 3.5 High resolution cross-sectional TEM images of (a) Control Ni-FUSI on  $\text{HfSiO}_x$  gate stack and (b) 30% Gd incorporated FUSI gate stacks after 450°C 1min RTA. Both low- $k$  interfacial layers and high- $k$  layer is reduced for Gd incorporated FUSI sample.

This is not surprising since silicidation kinetics of Gd involves Si diffusion. This above TEM and SIMS suggests that the reduction of the interfacial and high- $k$  layers occurs even though the Gd is not observed to be accumulating at the dielectric-electrode interface. Therefore, the reduction of the interfacial layer is attributed to an oxygen scavenging reaction by the Gd similar to what has been reported with Ti layers [100]. However, the scavenging effect of Gd is expected to be more severe than Ti due to its higher oxygen affinity. This physical thinning of EOT by decomposing the bottom interfacial layer is attributed to the thermodynamic nature of Gd-O and Si-O bonds. The Gibbs free energy of formation for Gd-O is -1739KJ/mol at 298K is much more negative than Si-O (-805KJ/mol) and even Hf-

O (-1084KJ/mol). This means that Gd–O reaction is the most favored reaction at a given thermal budget provided that enough kinetic energy is available for diffusion [101-102]. The Si remaining from this reaction can be assumed to be incorporated into the underlying substrate [100]. The decomposition of SiO<sub>2</sub> by Gd incorporated NiSi gates is clearly observed with single SiO<sub>2</sub> gate dielectric. 30 percent Gd incorporated in a NiSi gate on SiO<sub>2</sub> dielectric showed higher leakage current based on I-V measurements as shown in Figure 3.7.

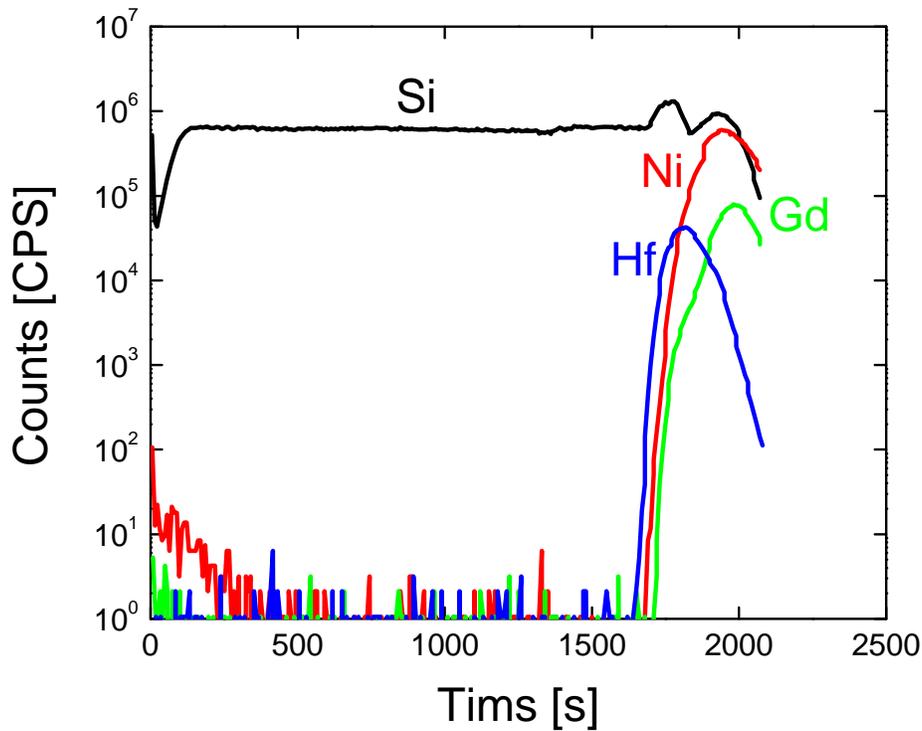


Figure 3.6 Backside SIMS for Ni<sub>70</sub>Gd<sub>30</sub>/ Si gate stack on HfSiO<sub>x</sub> gate dielectric after 450°C 1min annealing, measured with O<sub>2</sub><sup>+</sup> beam. No indication of Gadolinium diffusion into the dielectric was observed.

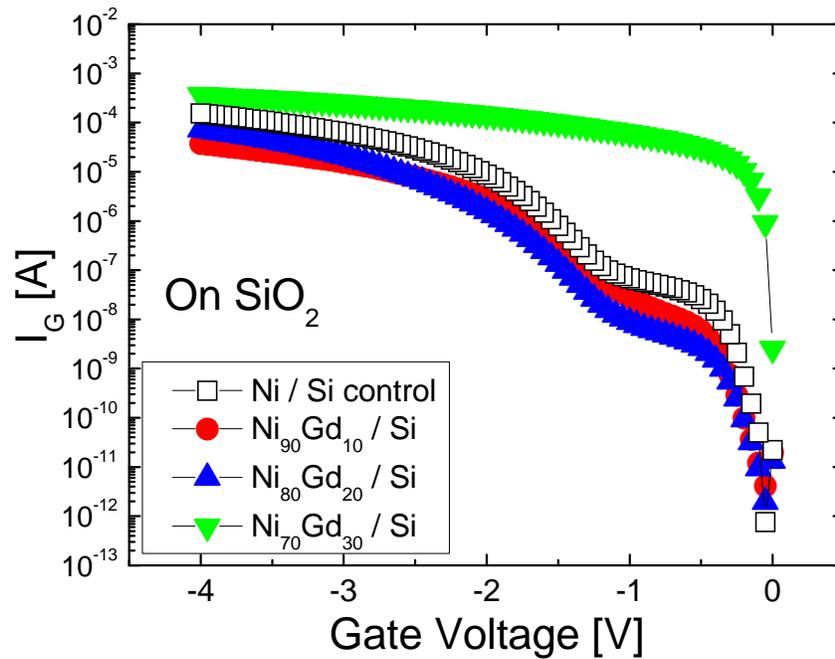


Figure 3.7 Leakage current for NiSi and Gd incorporated NiSi. Higher leakage with 30% Gd incorporation indicates the decomposition of oxide by Gd

Figure 3.8 shows extracted effective work function values as well as EOT of Ni – FUSI gate electrodes as a function of Gd percentage in the NiGd alloy film. As shown in Table 3.1, with 10 percent to 20 percent Gd, the shift in effective work function is about 0.2 eV compared to the control sample. With 30 percent Gd, 0.45 eV of effective work function value modulation from the control is achieved. The reduction in  $\phi_{m, \text{eff}}$  can be explained by several mechanisms. Firstly, as shown in Figure 3.9, Ni–Gd FUSI films are amorphous / nanocrystalline in their microstructure which is associated with the competing silidication mechanisms of Ni and Gd. This lack of crystallinity could affect the  $\phi_{m, \text{eff}}$  as already reported in the literature [103-104]. Secondly, it can be explained by the diffusion of GdNi alloy to the

silicide/dielectric interface where the low vacuum work function value of Gd could be responsible for lowering the effective work function from the typical NiSi gate value of 4.75 eV

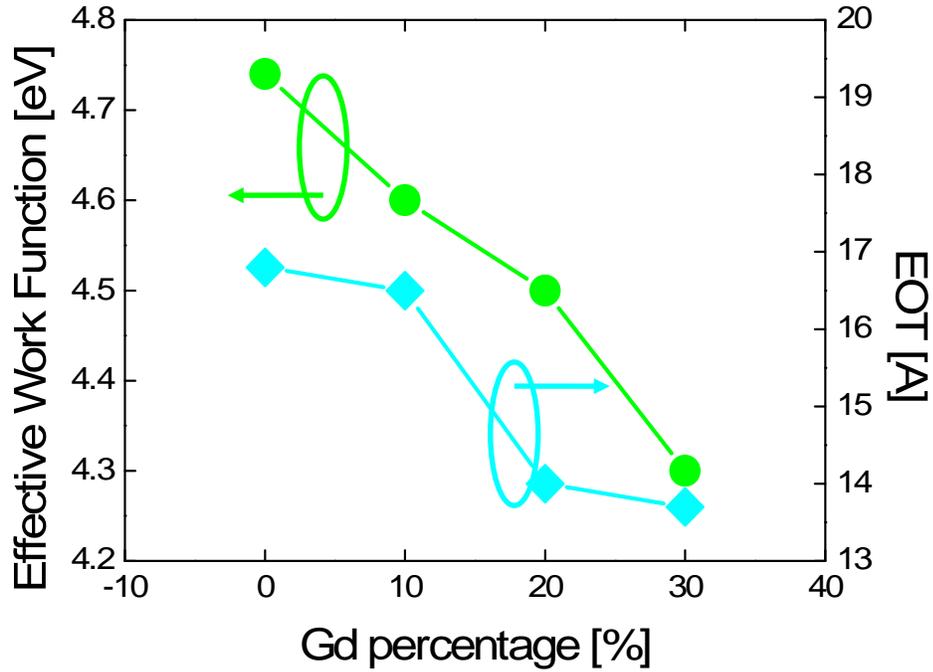


Figure 3.8 Extracted effective work function and EOT as a function of Gd percentage in Ni layer from  $V_{FB}$  vs. EOT plot.

Table 3.1 Summary of effective work function and EOT

<b>% of Gd in Ni</b>	<b>EWf [eV]</b>	<b>EOT [Å]</b>
<b>0</b>	<b>4.75</b>	<b>17</b>
<b>10</b>	<b>4.6</b>	<b>16.8</b>
<b>20</b>	<b>4.5</b>	<b>14</b>
<b>30</b>	<b>4.3</b>	<b>13.8</b>

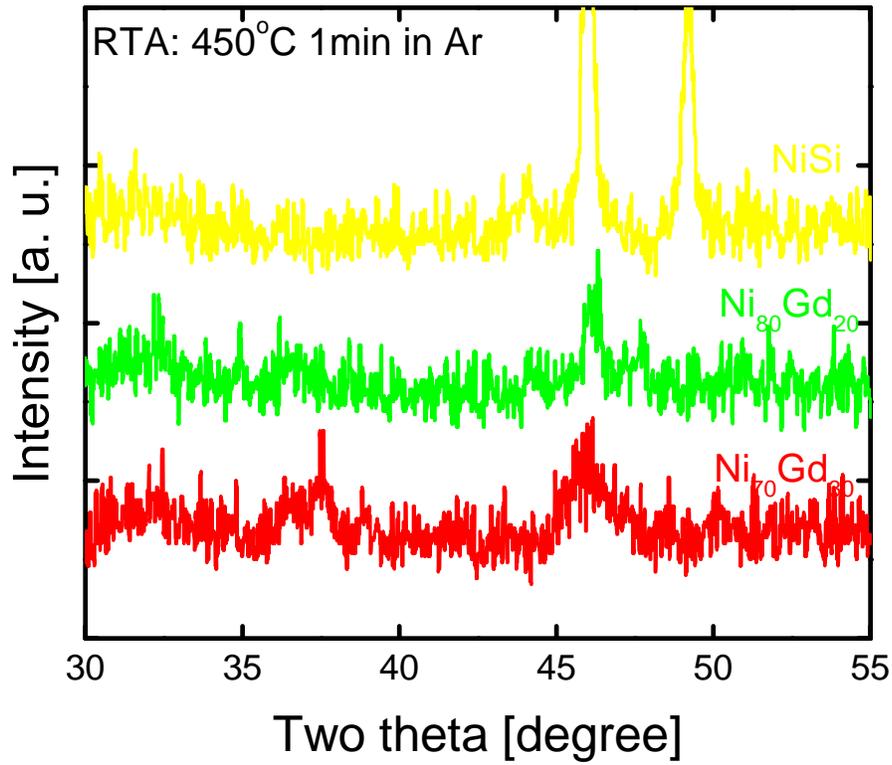


Figure 3.9 XRD patterns of NiSi and Gd incorporated NiSi gate electrodes for 10 to 30 percent Gd after one step silicidation annealing at 450°C for 1min. As percentage of Gd increases the peak intensity is reduced and broadened.

AES depth profiling has been performed in order to understand the effect of the incorporation of Gd metals on effective work function modulation. It should be noted that atomic concentration and sputter depth indicated in Fig. 3.10 is determined by the sputter rate and sensitivity factor relative to SiO<sub>2</sub>; therefore the actual thickness and concentration of each layer scales as the ratio of the sputter yield of the layer to the sputter yield of SiO<sub>2</sub>. In the case of the NiSi control, Ni and Si are uniformly distributed over the gate electrode layer up to the FUSI / high-*k* interface indicating the formation of a uniform Ni<sub>x</sub>Si<sub>y</sub> layer.

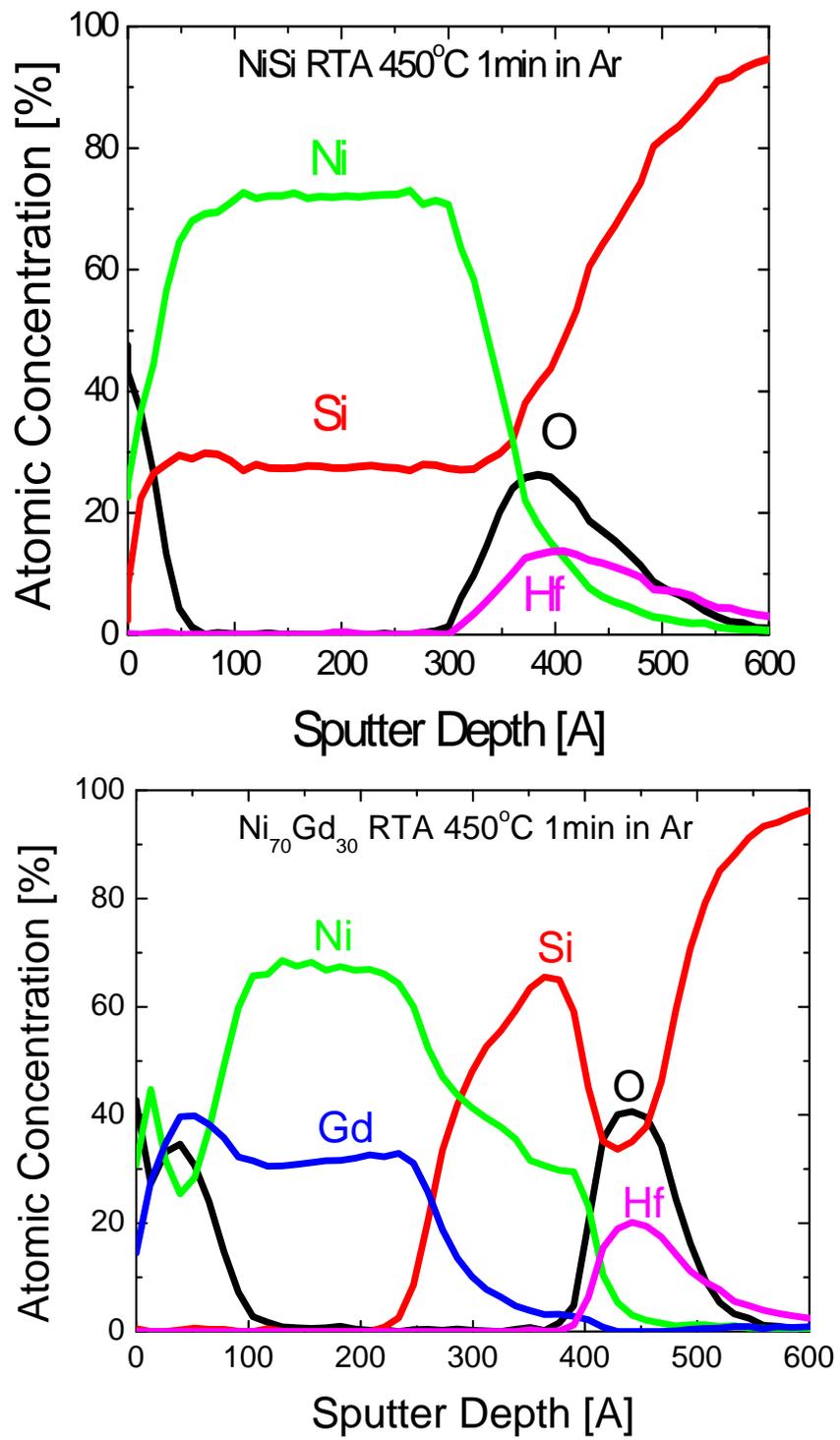


Figure 3.10 AES depth profile for (a) NiSi and (b) 30% Gd incorporated NiSi

On the other hand, the presence of Gd in the stack resulted in significant changes in the silicidation reactions as shown in Fig. 3.10 (b). Firstly, two distinct layers namely Ni–Gd layer on the top and Ni–Si–Gd (Si rich) intermixed layer on the bottom were observed. It is also noticed that Si up–diffusion into Ni–Gd layers was minimal and no Si was observed on the surface. This clearly suggests that the incorporation of Gd into a Ni-FUSI gate changes not only the relative composition of Ni and Si but also the structure of silicided layer. Another possible mechanism responsible for the lower  $\phi_{m, \text{eff}}$  could be the formation of positively charged oxygen vacancies within the high- $k$  dielectric. In order to understand this, the charge profile in the dielectric fixed charge density ( $N_f$ ) was calculated by taking the slope of  $V_{\text{FB}}$  versus EOT plot. The calculated fixed charge density values are  $3.434 \times 10^{11} / \text{cm}^2$  and  $1.383 \times 10^{11} / \text{cm}^2$  for NiSi and 30 percent Gd-NiSi gate respectively, indicating that the presence of oxygen scavenging of Gd layer does not increase fixed charge in the dielectric layer and hence the negative shift of  $V_{\text{FB}}$  by positive charge is not due to induced positive fixed charges of oxygen or Gd atoms in the dielectric layer. Therefore the shift in effective work function is attributed to compositional and structural changes in the presence of Gd incorporation in Ni-FUSI gate electrode.

### **3.3.2 Impact of Eu incorporation on Effective work function**

Figure 3.11 shows extracted  $V_{\text{FB}}$  vs. EOT plots for NiEu/Si/HfSiO<sub>x</sub>/Si capacitors from the C–V curve taken at 1MHz. It is observed that effective work function decreases as increase Eu fraction in FUSI gate as similar to Gd incorporation. Frequency dispersion

characteristics confirmed that Si layer is fully converted to silicide layer as shown in Fig. 3.12. It is also noticed that a 3 ~ 5 Å of EOT reduction was obtained with 30% Eu incorporation from the control without any degradation of dielectric leakage characteristics as shown in Fig 3.13. At least 2 order of magnitude of leakage reduction was observed with Eu-incorporated FUSI / HfSiO<sub>x</sub> dielectric stacks at 1V beyond flatband. High leakage with NiSi control on HfSiO<sub>x</sub> stack can be attributed to the formation of interfacial layer as shown in Fig 3.5 (a).

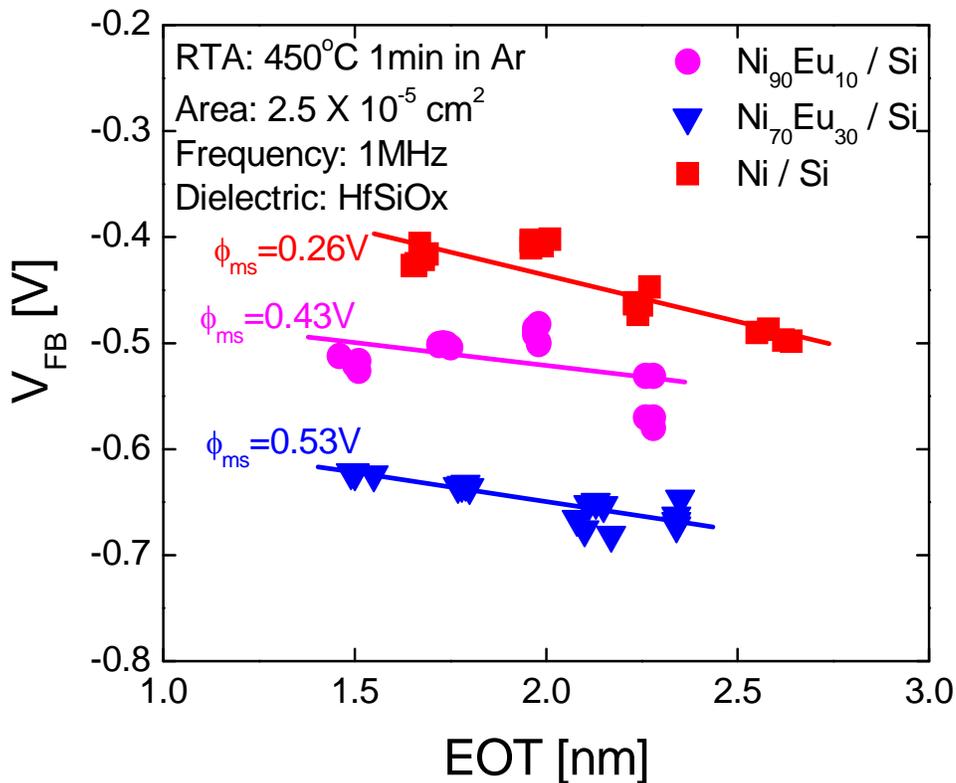


Figure 3.11  $V_{FB}$  vs. EOT with NiSi, 10% Eu incorporated Ni-FUSI, and 30% Eu incorporated Ni-FUSI after 450 °C 1min silicidation annealing in Ar ambient

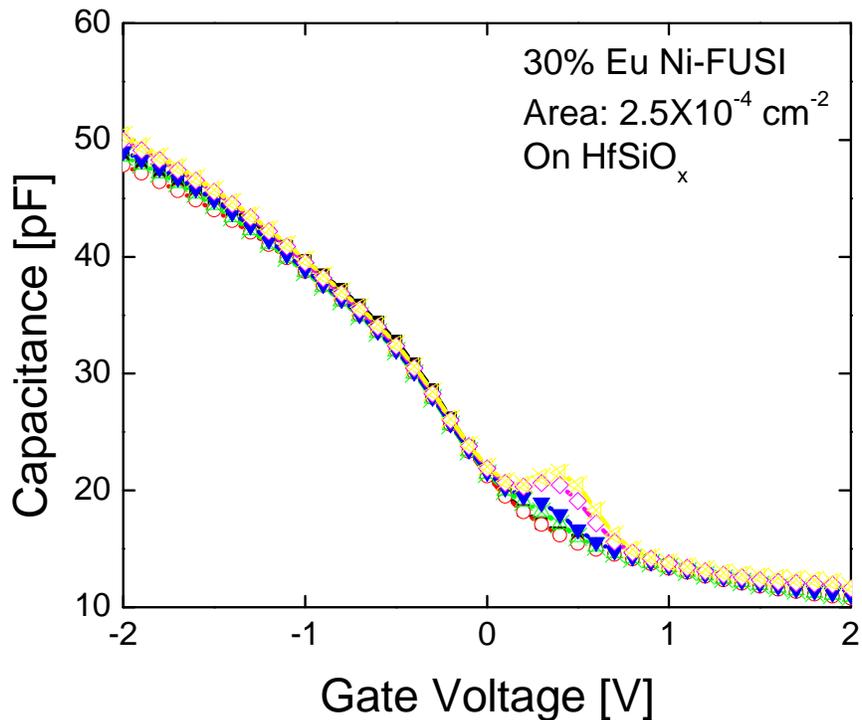


Figure 3.12 Frequency dispersion of 30% Eu incorporated Ni FUSI. Minimal dispersion at accumulation confirmed full silicidation.

Figure 3.14 shows EOT vs. high- $k$  physical thickness plot with NiSi control and 30% Eu incorporated Ni-FUSI gate. The interfacial layer thickness decreased from  $11 \text{ \AA}$  to  $8 \text{ \AA}$  as Eu percentage increased from 0 percent to 30 percent. The difference in interfacial layer thickness corresponds well to the decrease observed in EOT. Therefore the EOT reduction with Eu incorporation is also attributed to the decomposition of interfacial layer by the presence of high oxygen affinity Eu atoms similar to Gd incorporation. In addition, the change in EOT due to changes in the dielectric constant of the high- $k$  material is not

expected to be the dominant mechanism since the slope of the EOT vs. physical thickness is not changed with 30% Eu incorporation compared to NiSi control as seen in Fig. 3.14.

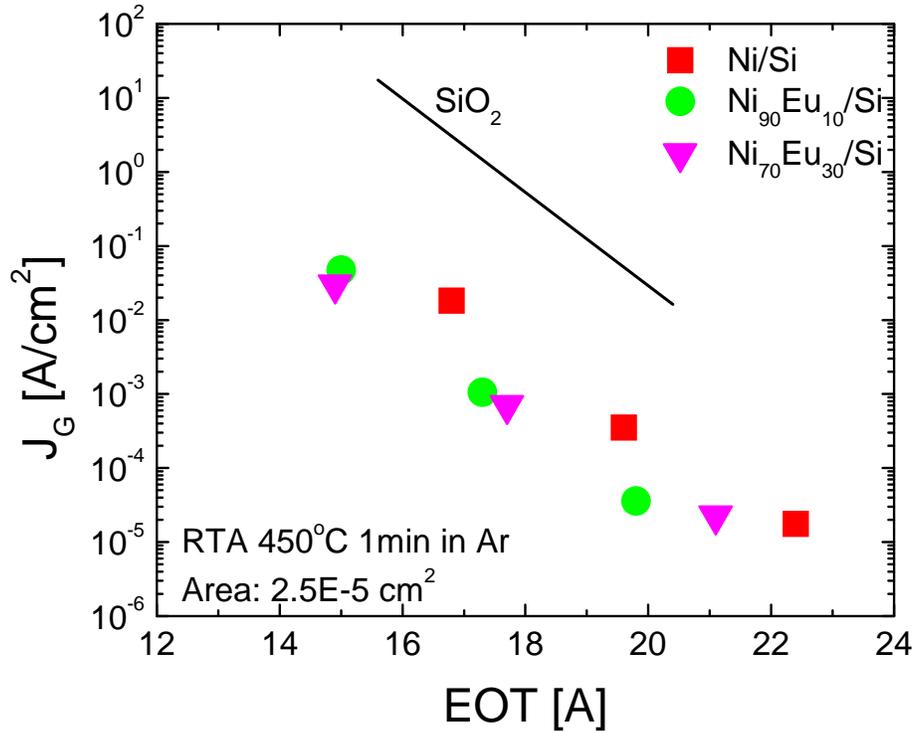


Figure 3.13  $J_G$  at 1V beyond flatband with NiSi, 10% Eu incorporated Ni FUSI, and 30% Eu incorporated Ni–FUSI gate. 2 order of magnitude reduction in leakage current with 30% Eu incorporated Ni–FUSI was observed.

Figure 3.15 and Table 3.2 summarized the impact of Eu incorporation into Ni based FUSI gate. As shown in Table 3.2, with 10 percent to 20 percent Gd, the shift in effective work function is about 0.2 eV compared to the control sample. With 30 percent Gd, 0.3 eV shift of effective work function value from the control is achieved which is 0.1 eV less than with 30 % Gd incorporation as shown in previous section. In order to understand the impact

of Eu incorporation on effective work function modulation of the gate stack, systematic material analyses were carried on.

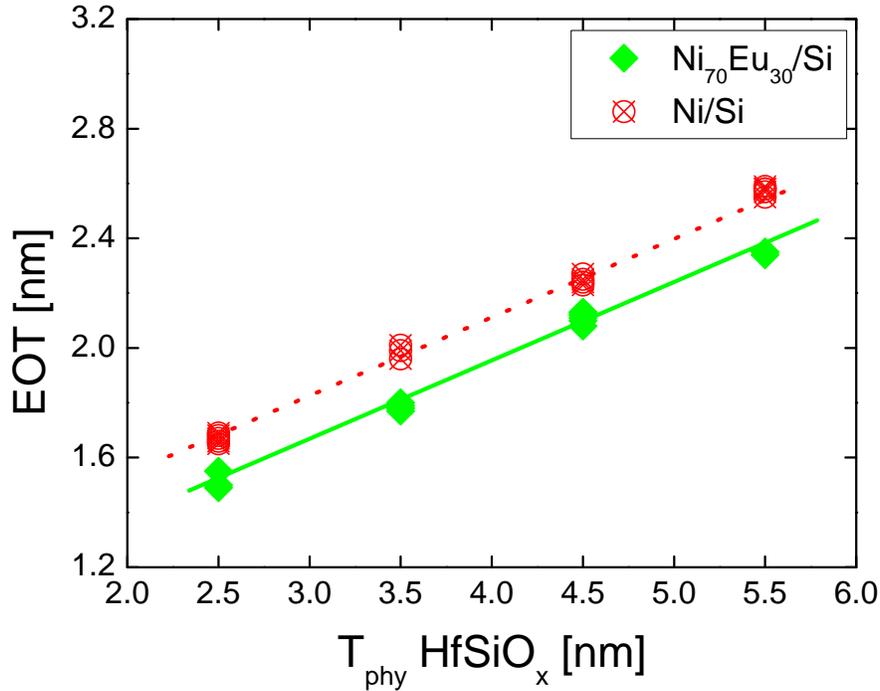


Figure 3.14 EOT vs. physical thickness of dielectric. Clearly shows reduction of interfacial layer with Eu incorporation. But the slope did not change indicating charge profile is similar.

Figure 3.16 shows AES depth profiling of the 30% Eu incorporated Ni-FUSI gate. AES data shows that three distinct layers with this gate stack which are Eu–Si–O alloy layer, a Ni–Si–Eu intermixed layer, and a Ni–Si layer from the top to the bottom (high- $k$  dielectric side). It is noted that, unlike the samples with Gd incorporation, Si is present on the surface indicating Si up-diffusion through the stack. It was also observed that the silicided layer near the  $\text{HfSiO}_x$  dielectric only consists of Si and Ni resulting in  $\text{Ni}_x\text{Si}_y$  layer similar to the control  $\text{Ni}_x\text{Si}_y$  (Fig. 3.10 (a)). The incorporation of Eu is not the same as Gd incorporation and hence

the effect of Eu on work function modulation of Ni-FUSI gate cannot be explained by structural change since the structure near the  $\text{HfSiO}_x$  dielectric layer is similar to the control Ni-FUSI gate.

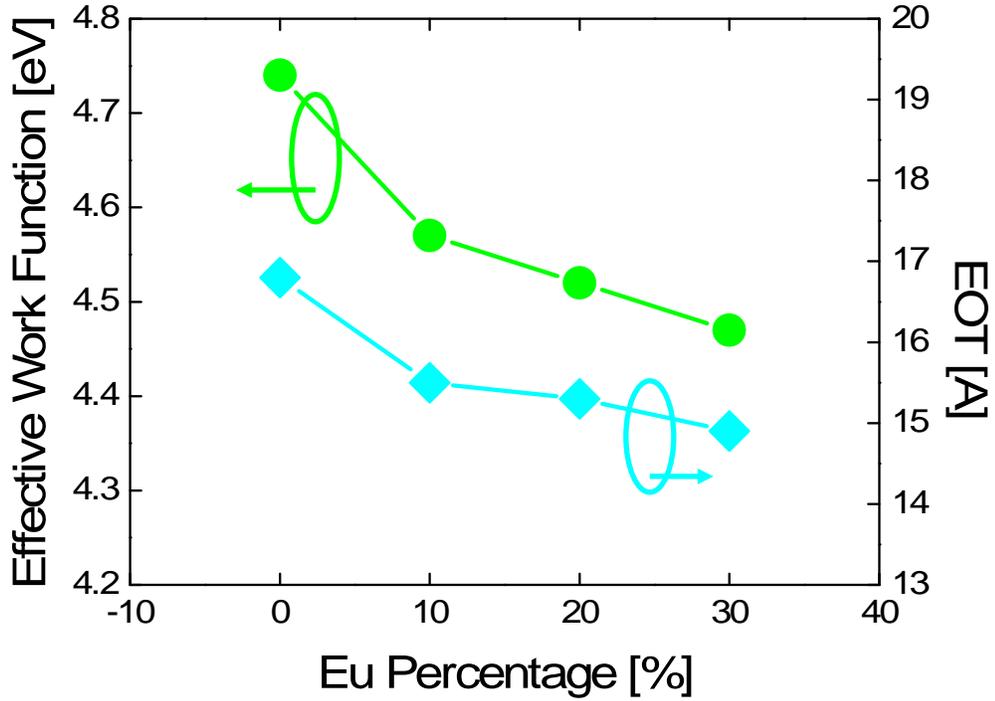


Figure 3.15 Effective work function and EOT as a function of Eu percentage of Ni-FUSI gate extracted from  $V_{FB}$  vs. EOT plot.

Table 3.2 Summary of effective work function and EOT

% of Eu in Ni	EWf [eV]	EOT [Å]
<b>0</b>	<b>4.75</b>	<b>17</b>
<b>10</b>	<b>4.6</b>	<b>15.5</b>
<b>20</b>	<b>4.54</b>	<b>15.3</b>
<b>30</b>	<b>4.45</b>	<b>14.9</b>

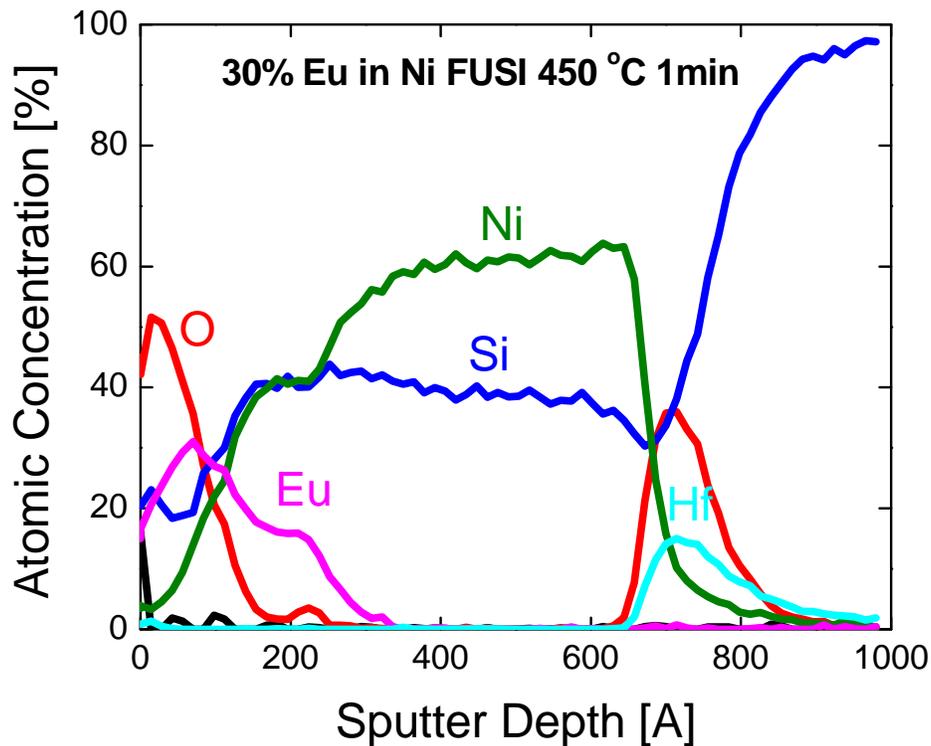


Figure 3.16 AES depth profile for 30% Eu incorporated Ni FUSI after 450 °C 1min silicidation annealing. Similar structure to NiSi near the high- $k$  layer was observed.

It is known that gate/high- $k$  interface is critical in determining effective work function of the gate stack. Therefore it is worthwhile to closely look at the profile of each element at this interface. Figure 3.17 shows the backside SIMS results for 30% Eu incorporated Ni-FUSI gate after silicidation annealing. It is clearly observed that Eu atoms are segregated at the gate / high- $k$  dielectric interface. This pile-up is a well known phenomenon in which dopants are redistributed when Ni-silicidation occurs due to lower solubility of the dopant in the silicide [94]. It should also be noted that backside SIMS data confirmed that Eu atoms are not present in the Si channel or bottom interface since the Hf

signal precedes Eu signal. However, it is shown that Ni diffuses into the high- $k$  dielectric layer and as a result the interface state increased as shown in Fig 3. 12.

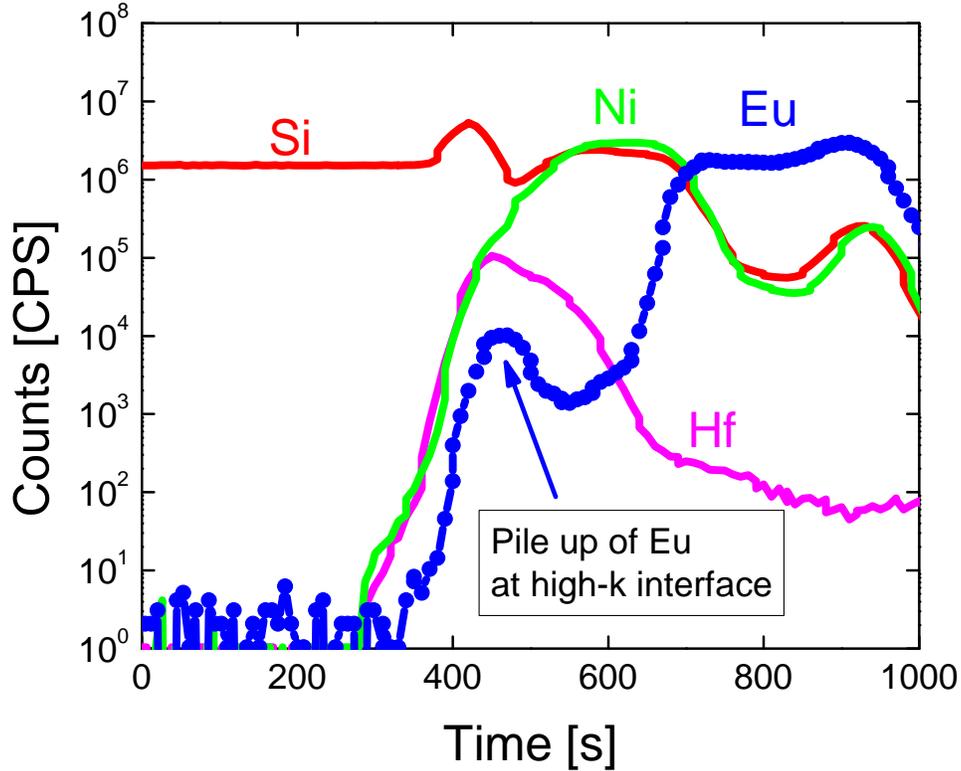


Figure 3.17 Baskside SIMS with 30% Eu incorporated Ni-FUSI after 450 °C 1min silicidation annealing. Pile-up at FUSI/high- $k$  interface was clearly observed.

### 3.3.4 Mechanism for Gd and Eu incorporation into Ni-FUSI

As shown above, incorporation of Eu and Gd in Ni-FUSI gate has provided different level of effective work function modulation compared to the control NiSi FUSI gate. Figure 3.18 summarizes effective work function, and corresponding EOT as well as gate leakage density ( $J_G$ ) plot taken from C-V and I-V measurement for  $Ni_xSi_y$  control gates, 30% Gd

incorporated Ni-FUSI gates, and 30% Eu incorporated Ni-FUSI gates respectively after silicidation annealing.

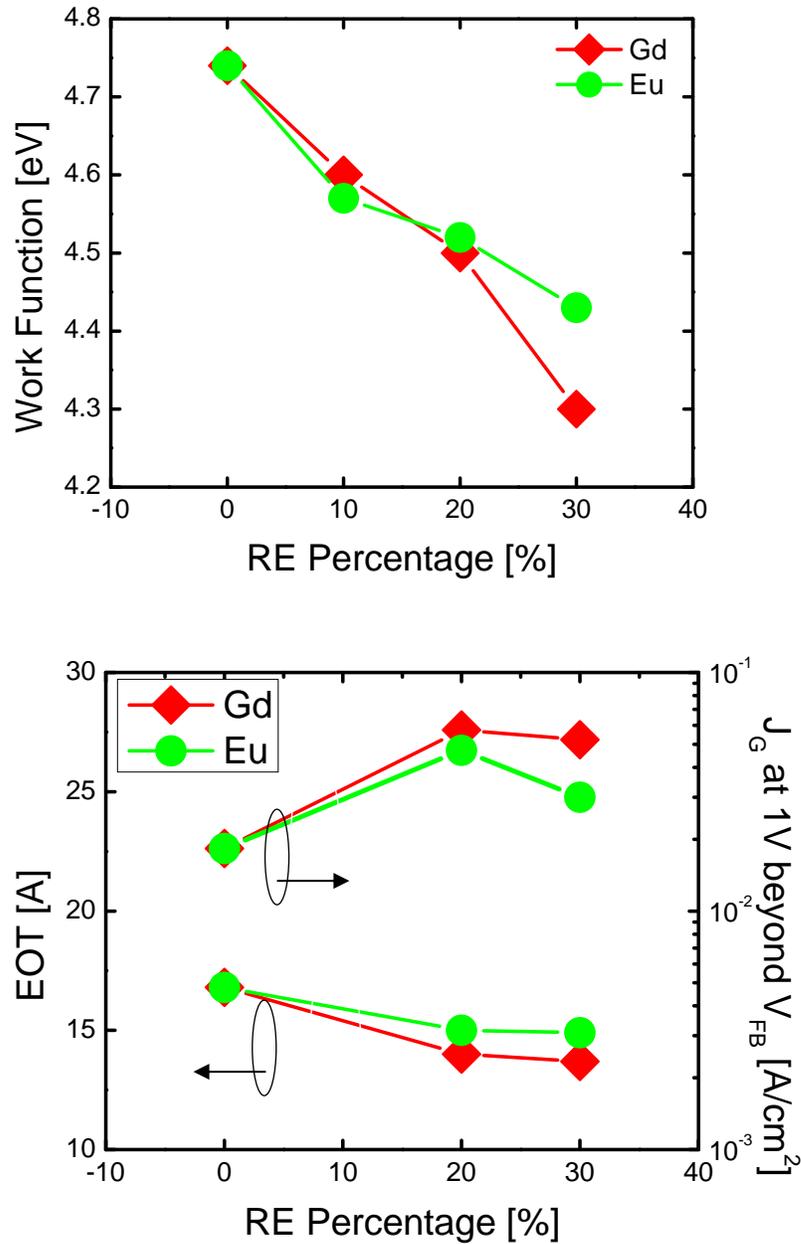


Figure 3.18 Comparison of Gd and Eu incorporation into Ni-FUSI for (a) Effective work function as a function of RE percentage in Ni and (b) corresponding EOT and leakage values

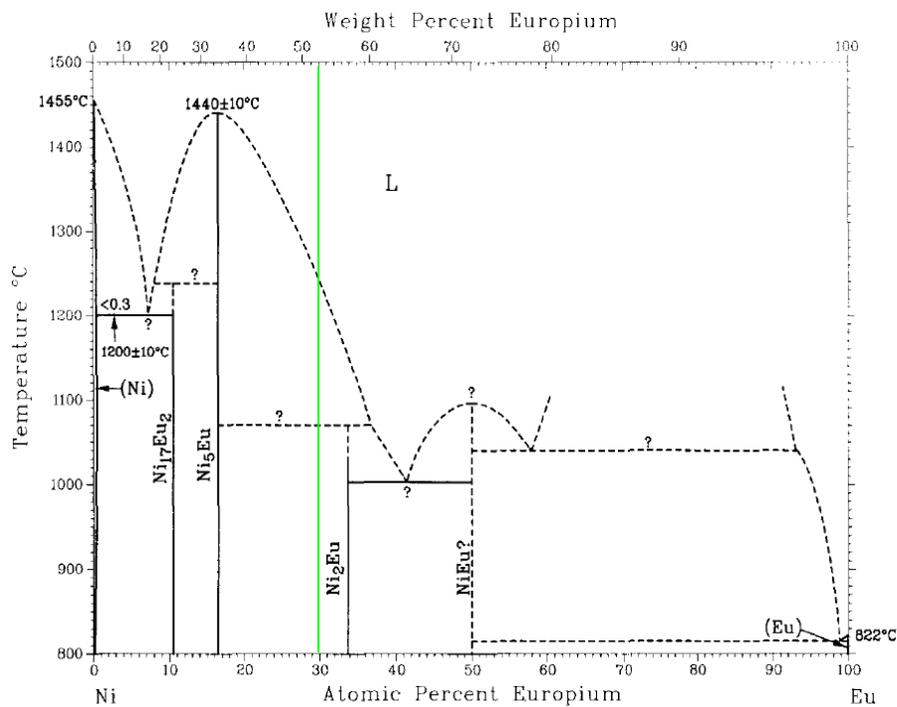
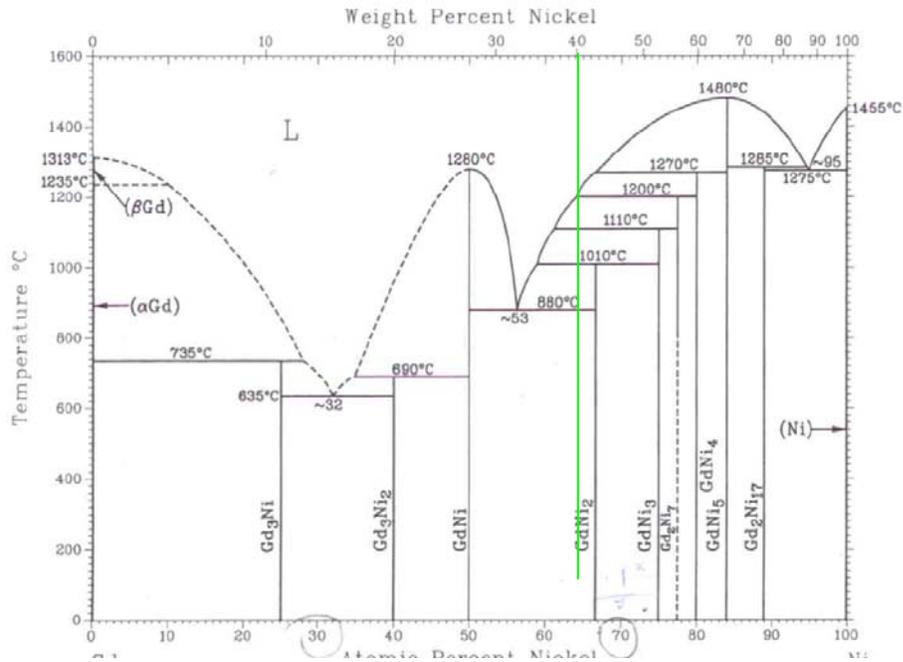


Figure 3.19 Binary Phase Diagram for (a) Ni-Gd alloy and (b) Ni-Eu alloy.

Eu incorporation shows slightly less EOT reduction from the control (0 %) and hence the corresponding leakage current is low. In case of work function value, with 30% Gd incorporation, a 0.45 eV shift of effective work function from the control  $\text{Ni}_x\text{Si}_y$  value (around midgap) was obtained, whereas only a 0.3 eV shift was obtained with 30% Eu incorporation.

In order to explain the different impact on effective work function modulation by Eu or Gd incorporation, it is carefully considered and examined both silicidation kinetics and thermodynamics for both RE silicide and Ni silicide. Since Ni is the dominant moving species for Ni-Si reaction whereas Si is the moving species for RE-Si reaction, based on silicidation kinetics, it is expected that Gd and Eu would behave similarly during the silicidation and the result would be similar if other conditions are the same. However, above experimental data shows that the roles of Gd and Eu in the silicidation process are not the same, and thus we cannot explain the role of Gd and Eu on effective work function modulation in terms of silicidation kinetics only. Based on AES and backside SIMS data, it is clearly shown that Gd atoms do not segregate out during the silicidation whereas Eu atoms easily segregate out from the Eu-Ni compound. This difference of segregation between Gd and Eu incorporation into Ni-FUSI gates can be explained by the formation of RE-Ni alloy based on thermodynamics. According to binary alloy phase diagram, Gd-Ni can easily form intermetallic compounds having many phases (> 5 phases) whereas Eu-Ni can only form only 2-3 phases as shown in Fig. 3.19 [105]. It is also reported that when 30% Gd is incorporated into a Ni layer, the heat of formation of Gd-Ni is more negative than Eu-Ni with 30% Eu [106-107]. This suggests that the bonding between Ni and RE metal reaction is

important when RE–Ni alloy forms a silicided layer. Therefore, when a Eu–Ni alloy reacts with Si, Ni is likely to react with Si by breaking the bonds with Eu resulting in a uniform  $\text{Ni}_x\text{Si}_y$  layer, since the Eu–Ni bonding is not as favorable as the Ni–Si or Eu–Si bonding. Therefore Eu atoms will segregate out of the Ni film resulting in Eu–Si layer on the top and Ni–Si layer near the high- $k$  dielectric interface with Eu segregation at the interface as can be seen in AES and backside SIMS (Fig. 3.16, and 3.17). In the case of Gd incorporation in Ni, however, most of Gd atoms are strongly bonded to Ni prior to or during silicidation resulting in the retardation of Ni diffusion, and hence this can cause compositional and structural changes in the  $\text{Ni}_x\text{Si}_y$  layer resulting in Si rich silicided layer with an amorphous/nanocrystalline structure (Fig. 3.6, 3.9, and 3.10). Figure 3.20 illustrates the schematic representation explaining the experimental data by the incorporation of RE metals in Ni-FUSI gate.

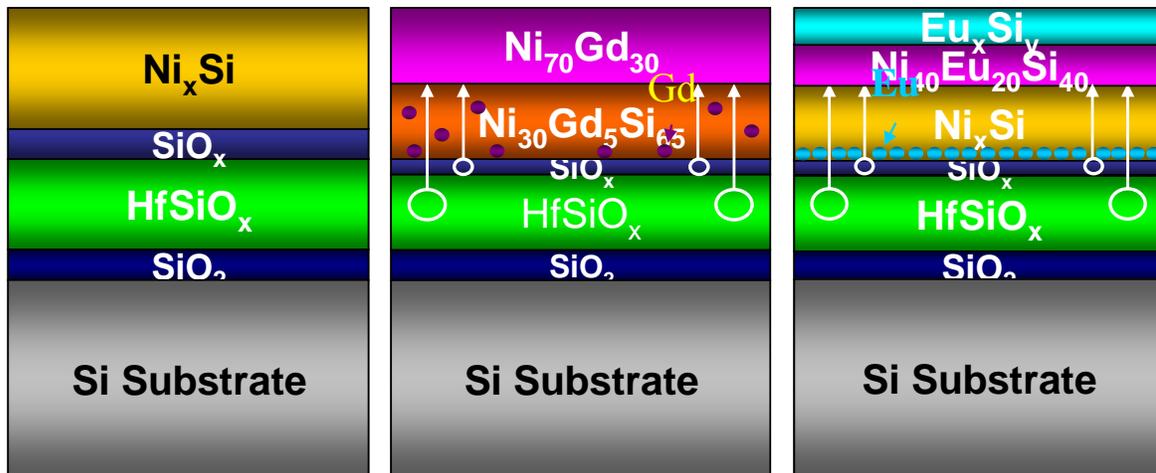


Figure 3.20 Schematic illustration of Gd and Eu incorporation into Ni-FUSI gate. (a) NiSi control gate, (b) 30% Gd incorporated Ni–FUSI, and (c) 30% Eu incorporated Ni–FUSI. The incorporation of Gd and Eu can change NiSi structure.

### 3.4 Summary

In conclusion, the role of Gd and Eu incorporation in Ni-FUSI gates on HfSiO<sub>x</sub> dielectric was analyzed by electrical and material characterization methods. A larger degree of effective work function modulation was achieved with 30% Gd incorporated Ni-FUSI gate than with 30% Eu incorporated Ni-FUSI gate. The primary reason for this difference is attributed to the difference between initial Gd-Ni and Eu-Ni formation based on their material properties prior to or during the silicidation reaction. Gd atoms retard Ni diffusion into a Si layer resulting in a Si rich silicided layer which is an amorphous/nanocrystalline in nature, whereas Eu atoms are believed to be pushed out by NiSi silicidation resulting in an uniform Ni<sub>x</sub>Si<sub>y</sub> layer with Eu pile-up at the FUSI/high-*k* interface. Furthermore, both Gd and Eu incorporation can also scavenge the oxygen remotely from SiO<sub>2</sub> dielectric leading to a desirable EOT reduction with acceptable leakage current.

## Chapter 4

# Investigation of the origin of $V_T/V_{FB}$ modulation by $\text{La}_2\text{O}_3$ capping layer approaches for NMOS application

### 4.1 Introduction

Recently gate dielectric capping approaches have been introduced in CMOS logic technologies since this technique can provide the desired threshold voltage ( $V_T$ ) while maintaining low EOT with good electrical and reliability properties [46-47, 108]. Rare-Earth (RE) based capping layers are used as NMOS capping materials due to their intrinsic properties [46-47]. Several mechanisms were introduced to explain the origin of  $V_T/V_{FB}$  modulation, yet the main mechanism for  $V_T/V_{FB}$  tuning caused by RE capping layers with high- $k$  dielectrics is still under investigation. In this chapter, the main mechanism on  $V_T/V_{FB}$  shift caused by  $\text{La}_2\text{O}_3$  capping incorporation is analyzed in terms of electrical and analytical characterization methods. The possible reaction mechanisms causing the  $V_T/V_{FB}$  modulation seen in NMOS gate stack is then proposed based on experimental results. Transistors with  $\text{La}_2\text{O}_3$  capping were then fabricated to evaluate the impact of capping layers on device performance and reliability.

## 4.2 Experiments

The conventional gate first n-channel MOSFETs and MOSCAPs were fabricated on p-type substrate. Three different high- $k$  dielectrics ( $\text{Al}_2\text{O}_3$ ,  $\text{Al}_2\text{O}_3/\text{HfO}_2$ , and  $\text{HfO}_2$ ) were used as host dielectrics in this study.  $\text{HfO}_2$  was deposited by atomic layer deposition (ALD) and  $\text{Al}_2\text{O}_3$  layer was deposited by RF-PVD or ALD method. Then ultrathin ( $5\text{\AA}$  or  $10\text{\AA}$ )  $\text{La}_2\text{O}_3$  cap layer was deposited on these dielectrics in a UHV-MBE system by using reactive evaporation of lanthanum in oxygen ambient, and then were annealed in-situ at  $475^\circ\text{C}$  in  $1\times 10^{-6}$  Torr  $\text{O}_2$ , followed by an ex-situ TaN/W metal gates deposition using an UHV RF-sputtering system. Figure 4.1 illustrates dielectric stacks used in this work and summarizes processing steps. After patterning and selective etch, the capacitor samples were subjected to Rapid Thermal Annealing (RTA) for various temperature ranges in Ar ambient to investigate the effect of temperature on the device characteristics. The dopant activation anneal was done at  $1000^\circ\text{C}$  5s in RTA system for the transistor samples. Forming Gas Annealing (FGA) was done for all samples before measurements. Capacitance-Voltage (C-V) and Current-Voltage (I-V) characteristics were measured using HP4278 LCR meter and Keithley 4200SCS system respectively. Electrical equivalent oxide thickness (EOT) and flatband voltage ( $V_{\text{FB}}$ ) were extracted using NCSU CVC program [99]. Split C-V and charge pumping measurement were used for transistors in order to extract mobility and interface state density respectively. Angle-resolved X-Ray Photoelectron Spectroscopy (AR-XPS), X-ray diffraction (XRD), and Transmission Electron Microscopy (both high resolution and z-contrast) were used to examine the chemical and physical properties of the dielectric stacks.

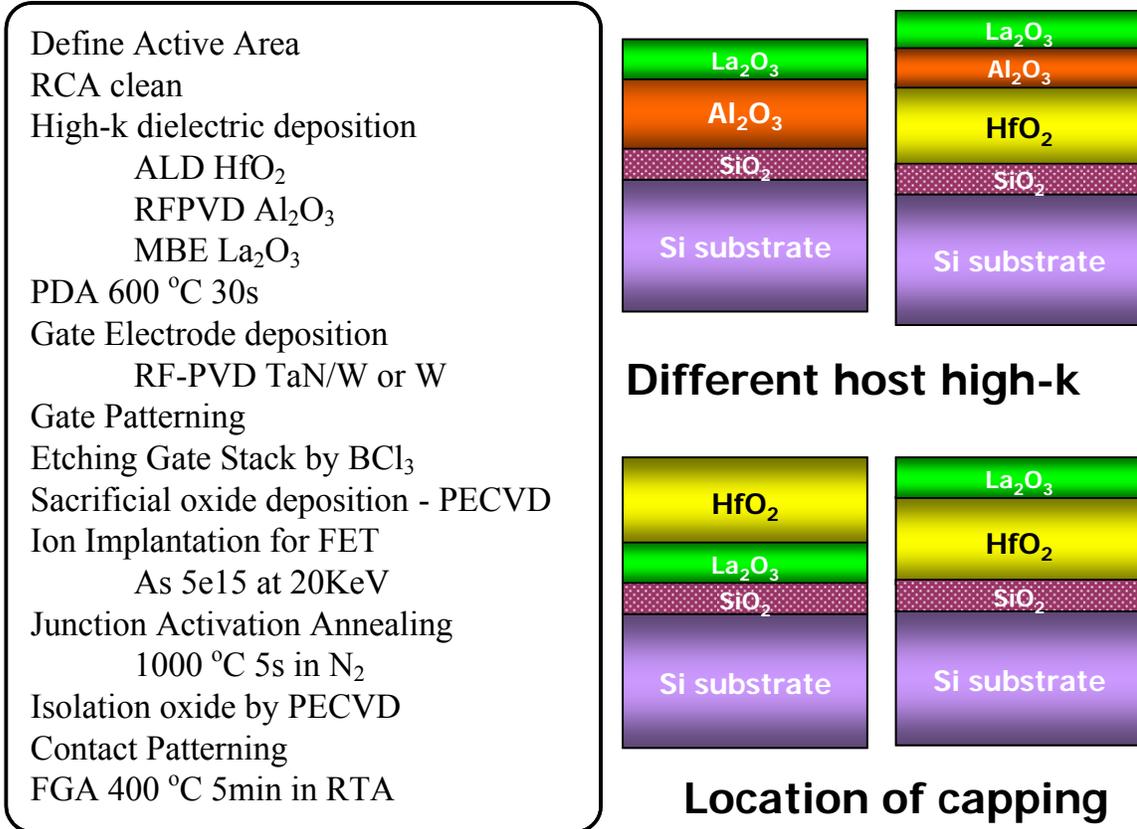


Figure 4.1 Process flows for gate first self-align nMOSFET process and schematic of dielectric stacks used in this study.

### 4.3 Literature Review of proposed mechanism on $V_T/V_{FB}$ modulation by Rare-Earth capping Incorporation

As discussed in chapter 1 and 2, it is desired to have low  $V_T$  value to achieve better performances. When Rare-Earth oxide or nitride is incorporated into nitride metal gate (TaN or TiN) / Hf-based dielectric stack, the device  $V_T/V_{FB}$  is shifted toward Si conduction band edge resulting in desired  $V_T$  value for NMOS device. Several mechanisms based on valencies, dipoles and charges have been introduced to explain the experimental  $V_T/V_{FB}$  shift [109-111].

S. Guha et al., proposed a mechanism explaining  $V_{FB}$  shifts in  $La_2O_3/HfO_2$  stack using a vacancy model [109]. It is said that the substitution of La in Hf after high temperature annealing can create positively charged vacancies resulting in a shift in  $V_{FB}$  towards the negative direction expressed as



When a La ion with +3 valence substitutes into Hf sites, a negatively charged defect ( $La'_{Hf}$ ) and compensating positively charged oxygen vacancy ( $V_o^{\cdot\cdot}$ ) defect is generated to ensure charge neutrality and site conservation. In similar way it is expected to have larger impact of group IIA elements on  $V_T/V_{FB}$  is larger than group IIIB elements.

P. D. Kirsch et al., proposed another mechanism explaining  $V_{FB}$  shift by interface dipole model between RE–O–Hf [110]. After high temperature annealing RE atoms diffuse through the  $HfO_2$  layer and are present at the  $HfO_2/SiO_2$  interface. At this interface RE–O–Hf configuration can be formed resulting in charge transfer and as a result the device  $V_{FB}/V_T$  is shifted. The amount of charge transfer determines the magnitude of the dipole,  $\mu$ , which is determined by positive pole (+Q) and negative pole (–Q) separated by distance  $d$  represented as

$$\mu = Q \cdot d \quad (4.2)$$

This dipole vector shifts the effective gate work function of a variable amount  $\Delta$  depending on electronegativity of dopants.

J. M. LeBeau et al., proposed an alternate mechanism to explain  $V_T/V_{FB}$  shift of  $DyO_x$  and  $HoO_x$  capping on  $HfSiON$  dielectric [111]. They claimed that the microstructure change

in interfacial oxide ( $\text{SiO}_x$ ) could give rise to negative flatband shift. It was observed that there was minimal diffusion of Dy or Ho through the HfSiON by STEM but the negative  $V_{\text{FB}}$  shift was still observed. They found that the interfacial  $\text{SiO}_2$  thickness was reduced as RE oxide was introduced. The reduction of interfacial  $\text{SiO}_2$  can lead to either an oxygen deficient  $\text{SiO}_x$  layer or a HfSiON layer close to the Si channel resulting in increased amount of positive fixed charge and hence the negative  $V_{\text{FB}}$  shift.

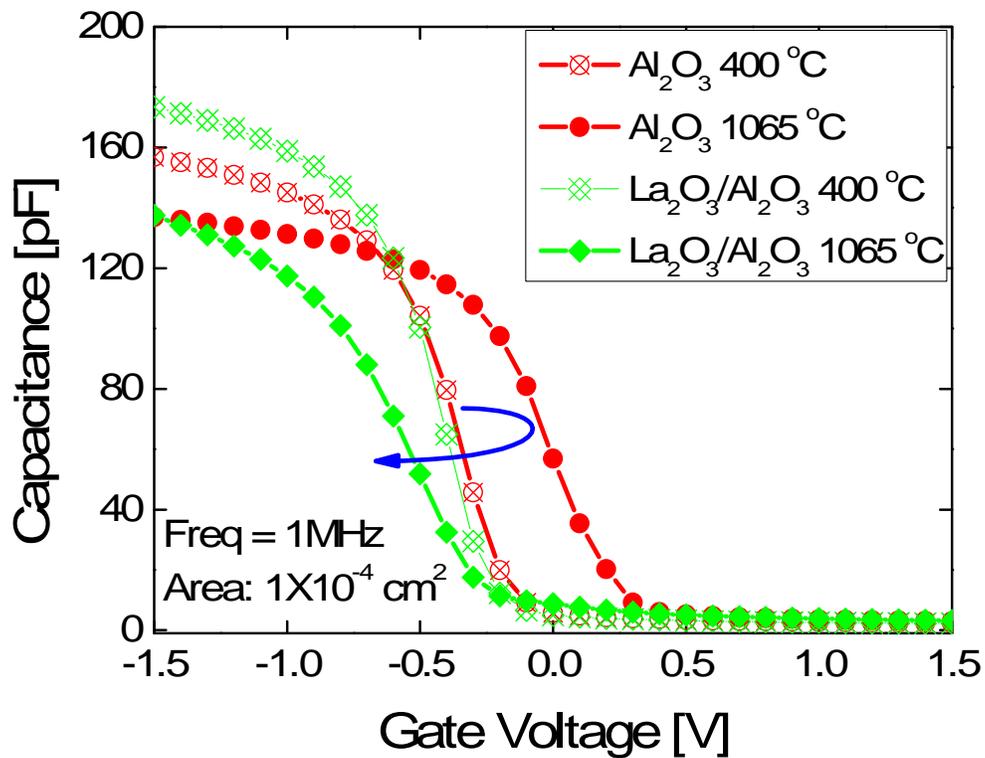


Figure 4.2 C–V curves with and without  $\text{La}_2\text{O}_3$  capping on  $\text{Al}_2\text{O}_3$  dielectrics. Larger  $V_{\text{FB}}$  shift was obtained after 1065 °C annealing.

## 4.4 Results and Discussion

### 4.4.1 Effect of host high- $k$ dielectrics on $V_{FB}$ (aliovalent substitution)

In order to clarify the origin of  $V_T/V_{FB}$  shift mechanism caused by  $\text{La}_2\text{O}_3$  incorporation, systematic experiments were designed. Aluminum oxide ( $\text{Al}_2\text{O}_3$ ) is a good dielectric material to study in terms of the impact of aliovalent substitution since the valency of Al is the same as La (+3). It is also known that  $\text{Al}_2\text{O}_3$  dielectrics provides pMOS like  $V_{FB}$ , lower oxygen vacancy levels than  $\text{HfO}_2$ , and a good interface to  $\text{SiO}_2$  [14, 112]. Figure 4.2 shows C-V characteristics with and without 10Å  $\text{La}_2\text{O}_3$  layer on 20Å  $\text{Al}_2\text{O}_3$  dielectric. In the case of control  $\text{Al}_2\text{O}_3$  samples, the capacitor  $V_{FB}$  is shifted toward positive direction after 1065°C annealing from the 400°C annealing and this is attributed to the large (or strong) dipole bonding at the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  interface [113]. When a thin layer of  $\text{La}_2\text{O}_3$  is incorporated in the dielectric followed by subsequent 1065°C annealing, the  $V_{FB}$  is shifted back towards the negative direction and even further modulated than the control  $\text{Al}_2\text{O}_3$  annealed at 400°C. Figure 4.3 shows C-V curves with and without the  $\text{La}_2\text{O}_3$  capping layer on 10Å  $\text{Al}_2\text{O}_3/20\text{Å}$   $\text{HfO}_2$  dielectric after 1065°C annealing. It is shown that a negative shift in  $V_{FB}$  is also observed in the presence of the  $\text{La}_2\text{O}_3$  capping layer but the degree of  $V_{FB}$  shift is less than with the single  $\text{Al}_2\text{O}_3$  dielectric. Figure 4.4 compares  $\Delta V_{FB}$  ( $V_{FB, \text{without capping}} - V_{FB, \text{with capping}}$ ) as a function of temperatures for both  $\text{Al}_2\text{O}_3$  and  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectrics. It is clearly shown that the  $V_{FB}$  is shifted toward negative direction only when  $\text{La}_2\text{O}_3$  capping layer is incorporated and depends only on the anneal temperature regardless of host high- $k$  dielectric. It is noted that the  $\Delta V_{FB}$  is less with  $\text{Al}_2\text{O}_3/\text{HfO}_2$  than  $\text{Al}_2\text{O}_3$  and this is attributed to 1) the use

of thicker dielectric of 10Å Al<sub>2</sub>O<sub>3</sub> / 20Å HfO<sub>2</sub> layer than 20Å Al<sub>2</sub>O<sub>3</sub> layer and 2) easier reaction of La<sub>2</sub>O<sub>3</sub>–Al<sub>2</sub>O<sub>3</sub> than La<sub>2</sub>O<sub>3</sub>-HfO<sub>2</sub> based on thermodynamics[114-115].

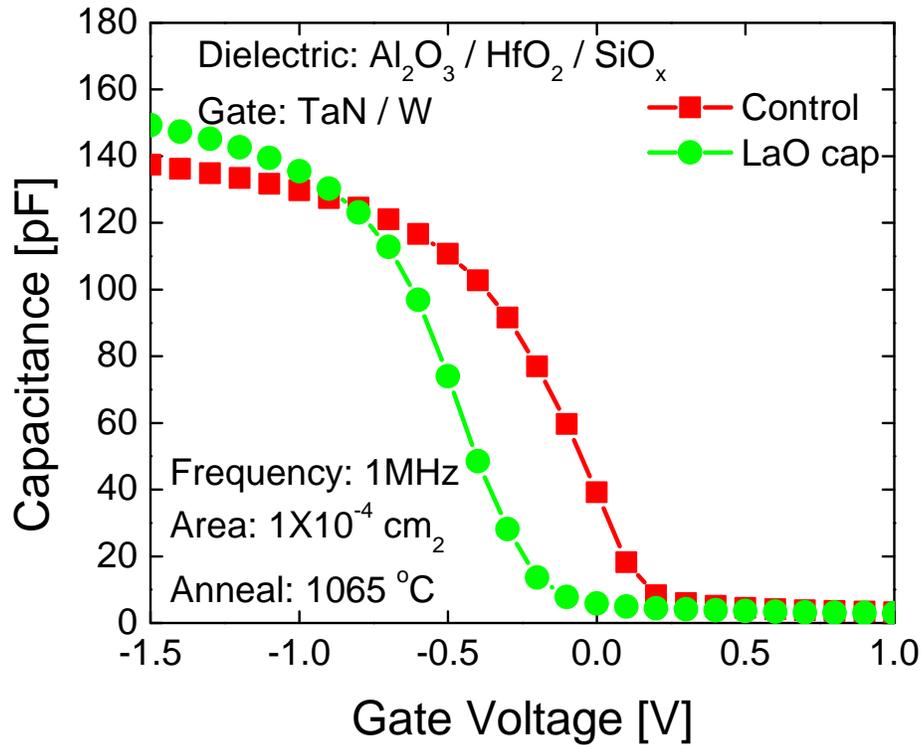


Figure 4.3 C-V curves with and without La<sub>2</sub>O<sub>3</sub> capping on Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> dielectric after 1065°C annealing. Negative shift in V<sub>FB</sub> is also observed but the degree of shift is less than capping on Al<sub>2</sub>O<sub>3</sub> dielectric.

If the negative V<sub>FB</sub> shift is due to the oxygen vacancy caused by the La–Hf reaction during the annealing, then Al<sub>2</sub>O<sub>3</sub> dielectric should provide less or minimal negative shift since La and Al have same valency (+3). However, our experimental data clearly demonstrates that the V<sub>FB</sub> shift behavior is observed only with La<sub>2</sub>O<sub>3</sub> incorporation and is indeed larger with Al<sub>2</sub>O<sub>3</sub> dielectric than Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>. Moreover it is reported that La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>

dielectric provides negative  $V_{FB}$  without the  $HfO_2$  layer [116]. Therefore it is concluded that the  $V_{FB}$  modulation is related to the nature of  $La_2O_3$  and independent of host high- $k$  layer or the valency. Figure 4.5 summarizes EOT and leakage current density with and without  $La_2O_3$  capping on  $Al_2O_3$  dielectric as a function of temperature. It is shown that about 3 ~ 4 Å of EOT are gained after 1065°C annealing for both samples and this is attributed to the interfacial  $SiO_2$  layer growth. The leakage current characteristics with  $La_2O_3$  incorporation are slightly better than controls and this can be explained by the formation of higher  $k$  ( $LaAlO_x$ ) material or physically thicker  $La_2O_3/Al_2O_3$  dielectric compared to  $Al_2O_3$  dielectric.

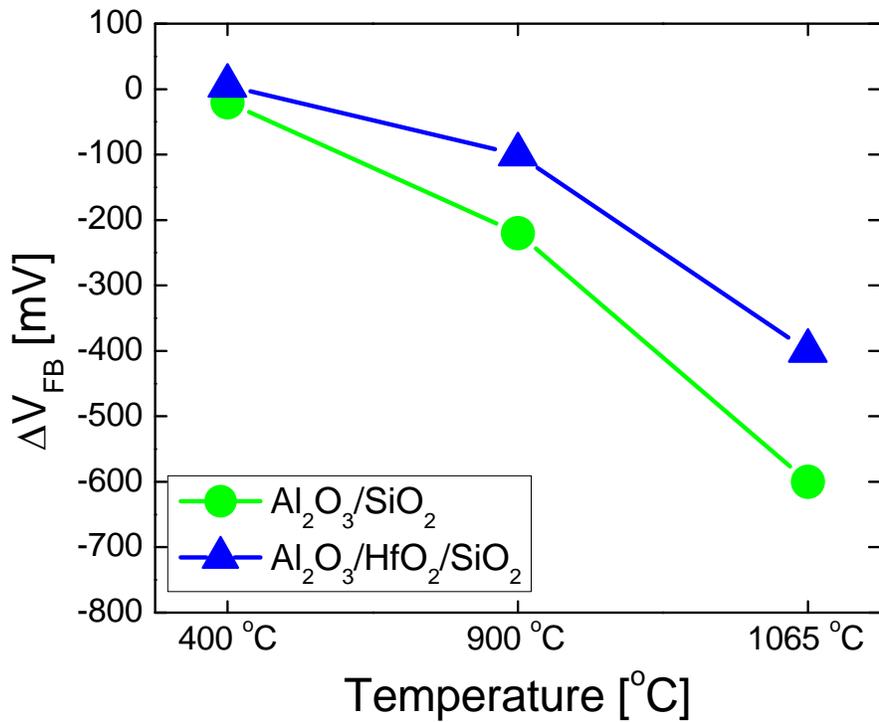


Figure 4.4  $\Delta V_{FB}$  shifts as a function of temperature with  $La_2O_3$  incorporation on  $Al_2O_3$  and  $Al_2O_3/HfO_2$  dielectrics. Amount of shift depends on temperature and 600mV of  $V_{FB}$  was modulated with  $Al_2O_3$  dielectric after 1065°C annealing.

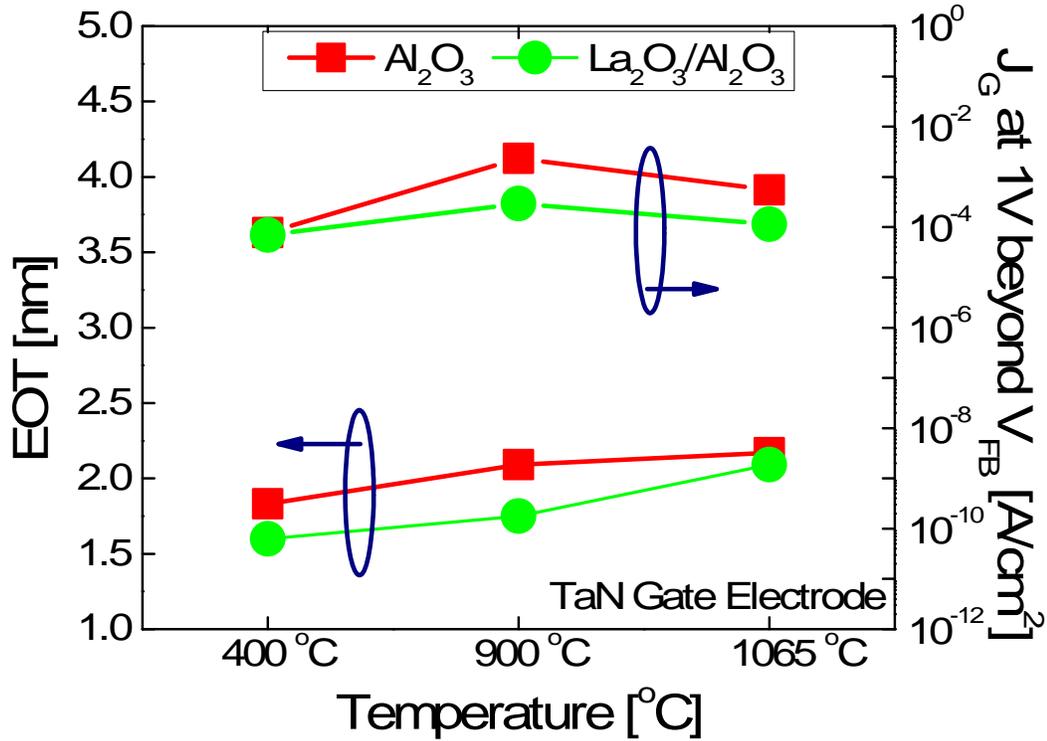


Figure 4.5 Extracted EOT and  $J_G$  at  $V_G - V_{FB} = 1V$  for  $Al_2O_3$  and  $La_2O_3/Al_2O_3$  dielectric. Low EOT and leakage value were obtained with  $La_2O_3$  addition due to the higher  $k$  layer formation.

Angle resolved XPS was performed to evaluate the diffusion, chemical change, and intermixing of the above dielectric stacks with  $La_2O_3$  cap incorporation. It is noted that all peaks were referenced to the Si 2s substrate peak at a binding energy of 150.7 eV [117]. As shown in Fig. 4.6, Si 2s spectra consists of two main peaks of which the major peak is Si–Si bonding from the Si substrate and the broad second peak, near 154.0 eV, represents Si–O bonding for the control  $Al_2O_3/SiO_x$  dielectric. With a  $La_2O_3$  capping layer subjected to a 400°C anneal, the second peak can be fit by two peaks at 153.5 eV and 152.0 eV noting that

the higher peak is indicative of  $\text{SiO}_x$  formation and the lower peak is indicative of silicate like formation [118].

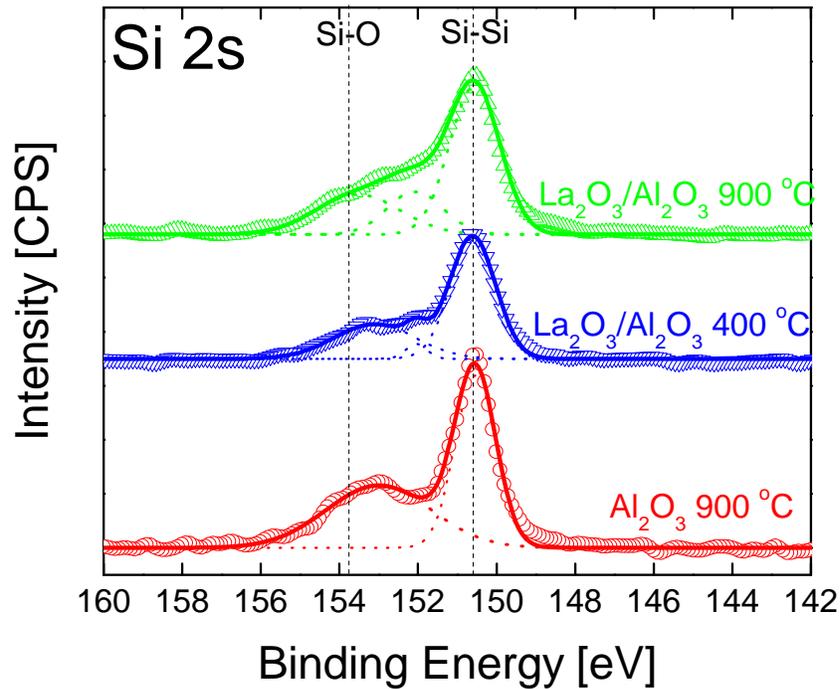


Figure 4.6 Si 2s XPS spectra with and without  $\text{La}_2\text{O}_3$  layer on  $\text{Al}_2\text{O}_3$  dielectric. The peak at near 152eV is observed with  $\text{La}_2\text{O}_3$  capping layer and increased after 900°C annealing indicating presence of silicate formation.

After 900°C annealing, the peak around 152.0eV increases indicating more silicate formation caused by intermixing of Si and La. Figures 4.7 (a) and (b) show the La 3d and Al 2p spectra for low and high T annealing with different take-off angles. The Al 2p peaks for the control sample were at 74.1 eV with 90° and did not change with 60° take-off angle, whereas the Al 2p peak with  $\text{La}_2\text{O}_3$  capped samples after a 400°C anneal showed a shift towards lower binding energy (BE) (73.5 eV) which is indicative of  $\text{LaAlO}$  formation [119].

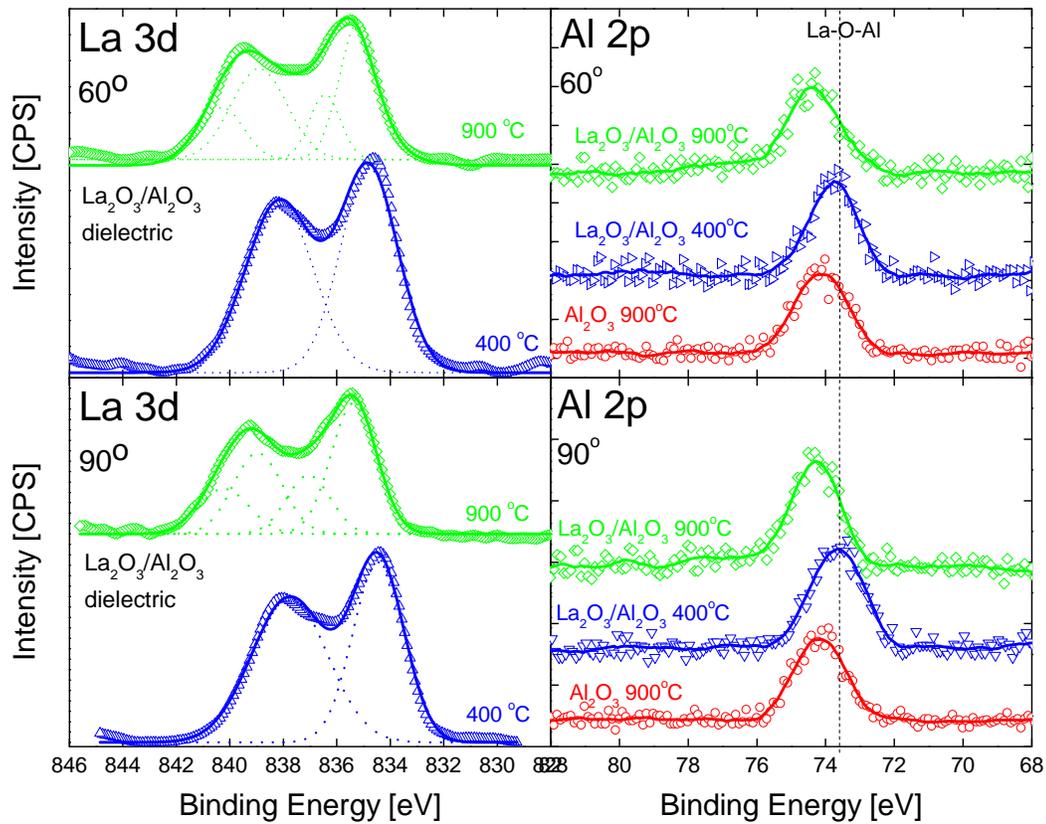


Figure 4.7 corresponding (a) La 3d and (b) Al 2p spectra on Al<sub>2</sub>O<sub>3</sub> dielectric with two different angles. La-silicate formation was confirmed after 900°C annealing.

Furthermore, the La 3d peak position is close to the La–O position. Since the binding energies of La–O and La–O–Al are very similar [119], it is hard to ascertain whether either a mixture of La–O and La–O–Al is formed or homogenous La–O–Al is formed at this temperature. However, after a high T anneal at 900°C, the Al 2p peaks shift back to the Al–O position and La 3d peak shifts to high binding energy (e.g., silicate like position) indicating that the chemical states of Al–O and La–O have been altered. Based on La, Al, and Si spectra we conclude that significant La–O–Si bonds at the Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> interface were formed during the high T annealing. It is known that La atoms tend to react with Si atoms, and thus La–

atoms leave LaAlO in order to form La–O–Si inside the Al<sub>2</sub>O<sub>3</sub> dielectric and/or near the bottom SiO<sub>2</sub> interface, leaving behind Al<sub>2</sub>O<sub>3</sub> near the top surface as observed from XPS. The formation of La–O–Si over LaAlO can also be explained by the more favorable free energy of formation of La–O–Si compared to that of La–O–Al, Al–O–Si, La–O or Si–O [119-120].

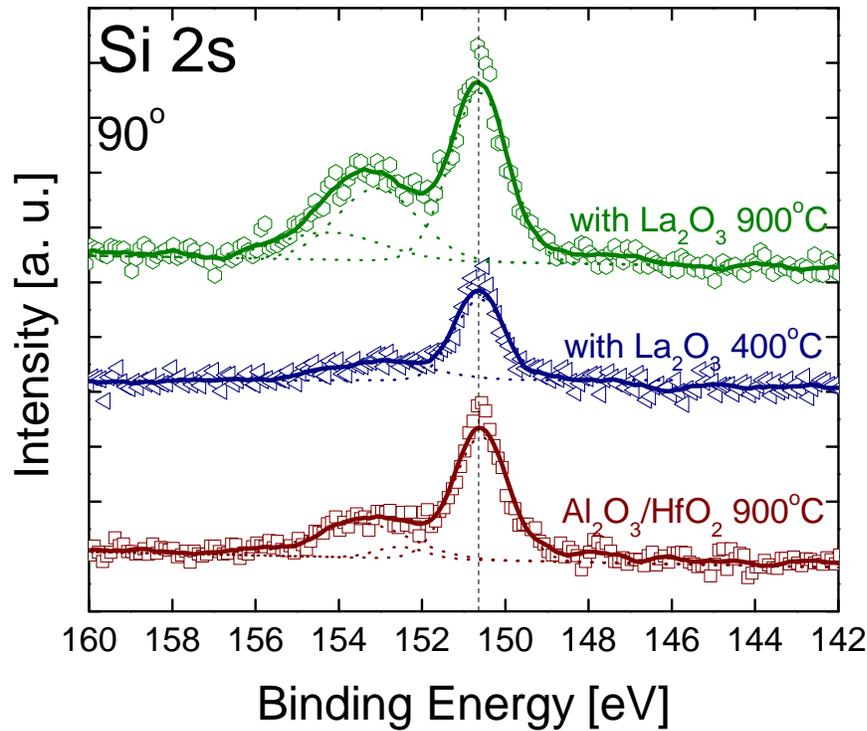


Figure 4.8 Si 2s XPS spectra with and without La<sub>2</sub>O<sub>3</sub> layer on Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> dielectric. Similar result was obtained with Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> dielectric with La<sub>2</sub>O<sub>3</sub> incorporation.

In case of Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> dielectric, only two Si 2s peaks at 150.7 eV (Si substrate) and 153.7 eV (Si–O) with La<sub>2</sub>O<sub>3</sub>/Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack were detected after 400°C annealing unlike La<sub>2</sub>O<sub>3</sub>/Al<sub>2</sub>O<sub>3</sub>/SiO<sub>x</sub> dielectrics, indicating no silicate formation and suggesting that 1) the HfO<sub>2</sub> serves as a diffusion barrier at these temperatures and/or 2) the thermal budget is not

enough for La to diffuse through the  $\text{HfO}_2$  layer. After high-T annealing, two peaks were observed located at 153.7eV (Si-O) and 152eV (Si-O-Hf or Si-O-La) suggesting the increase in interfacial layer as well as formation of silicate as compared to sample without  $\text{La}_2\text{O}_3$  capping as shown in Fig. 4.8. Figure 4.9 shows the La 3d and Hf 4f spectra on  $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{SiO}_x$  dielectric after low and high T annealing with different take-off angles. The La 3d peak shifts to higher binding energies after high temperature anneal suggesting either La-O-Hf and/or La-O-Si bonding whereas the Hf 4f peaks are shifted to lower binding energies than the control ( $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{SiO}_2$ ) sample. Since Hf-O-Si formation (representing Hf-silicate) is located 1 eV higher in B.E. than pure  $\text{HfO}_2$  [121], the lower B.E. could be attributed to the formation of vacancies in the  $\text{HfO}_2$  layer [122-123] or the reaction between La and Hf [116, 123], since La is a more ionic cation than Hf, based on the calculated bond ionicities of 0.75 and 0.68, respectively. However, the peak shift in La 3d peak after high T annealing is more than 1.0 eV suggesting that La atoms not only react with Hf or Al atoms, but also react with Si atoms as well.

XPS results clearly show that there is more reaction in the bottom interface for  $\text{La}_2\text{O}_3$  with  $\text{Al}_2\text{O}_3$  layer than  $\text{La}_2\text{O}_3$  with  $\text{Al}_2\text{O}_3/\text{HfO}_2$  layer and are correlated to the electrical results implying that this La-induced silicate formation is important for  $V_{\text{FB}}$  shift.

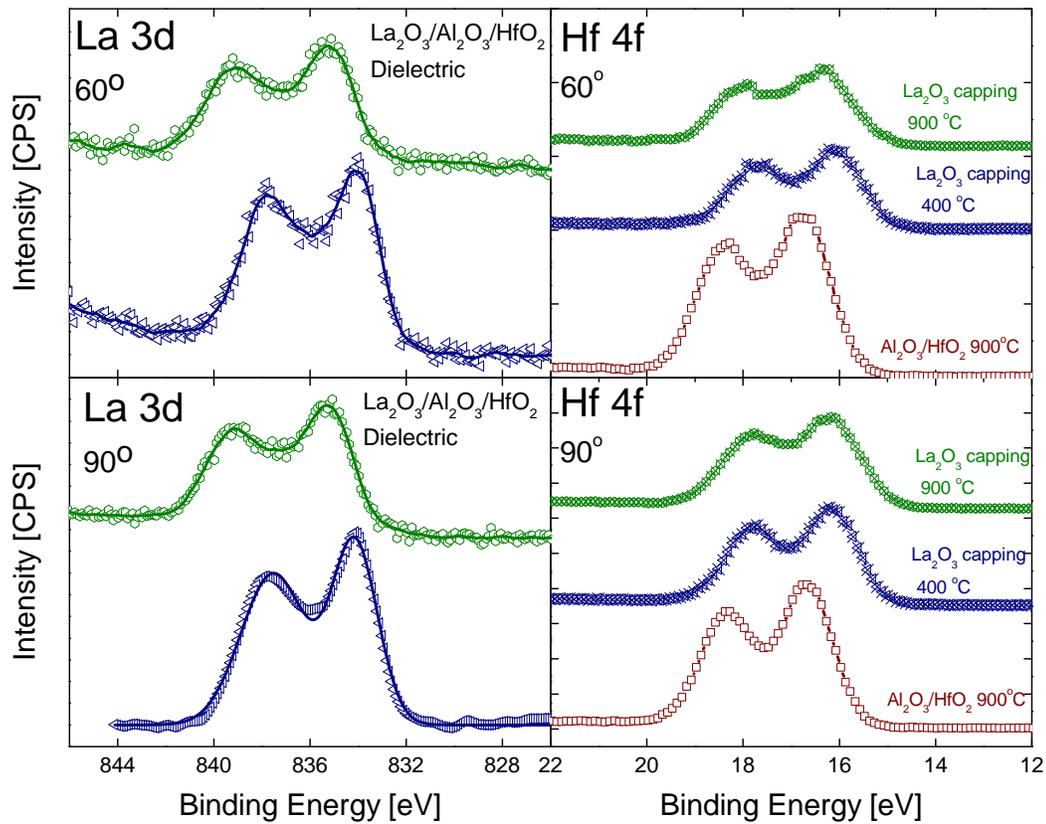


Figure 4.9 corresponding La 3d and Hf 4f spectra on  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric with two different take off angles. La-silicate formation was confirmed after  $900^\circ\text{C}$  annealing but the La 3d peak position with  $\text{Al}_2\text{O}_3/\text{HfO}_2$  is lower than with  $\text{Al}_2\text{O}_3$  dielectric. This less silicate formation can explain the less  $V_{\text{FB}}$  shift on  $\text{Al}_2\text{O}_3/\text{HfO}_2$  stack in Fig. 4.3.

#### 4.4.2 Effect of $\text{La}_2\text{O}_3$ location on $V_{\text{FB}}$ shift (Dipole and charge)

So far, it has been shown that the negative  $V_{\text{FB}}$  shift depends on the presence of La in the dielectric and La-induced silicate formation is suspected. To investigate the role of silicate on  $V_{\text{FB}}$  as well as to clarify the main mechanism responsible for the  $V_{\text{FB}}$  shift, a new set of experiments was designed. As already shown in Figure 4.1, an ultrathin layer of  $\text{La}_2\text{O}_3$  ( $5\text{\AA}$ ) dielectric was deposited either before or after  $\text{HfO}_2$  dielectric deposition.

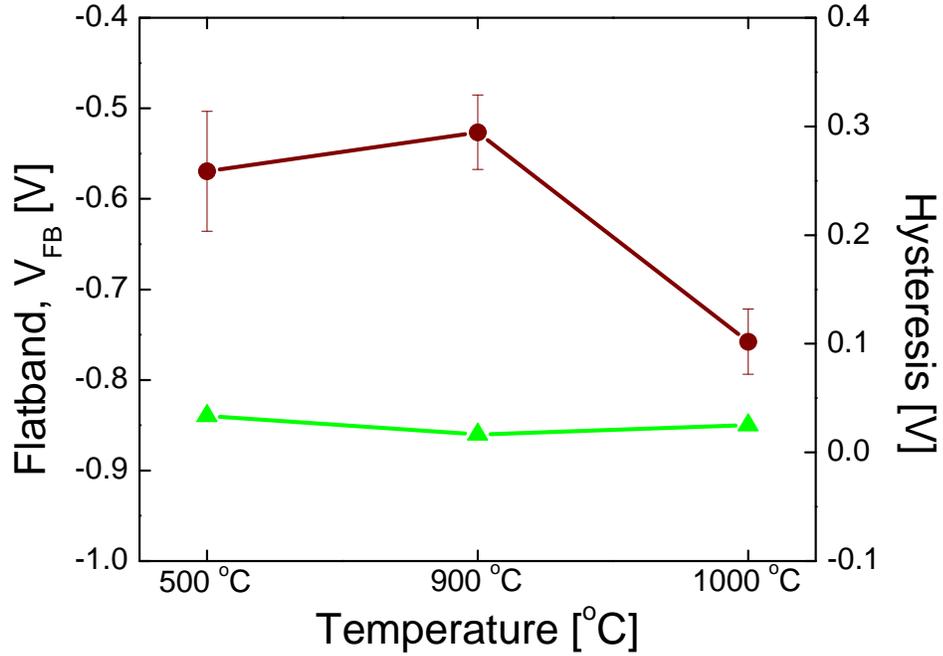
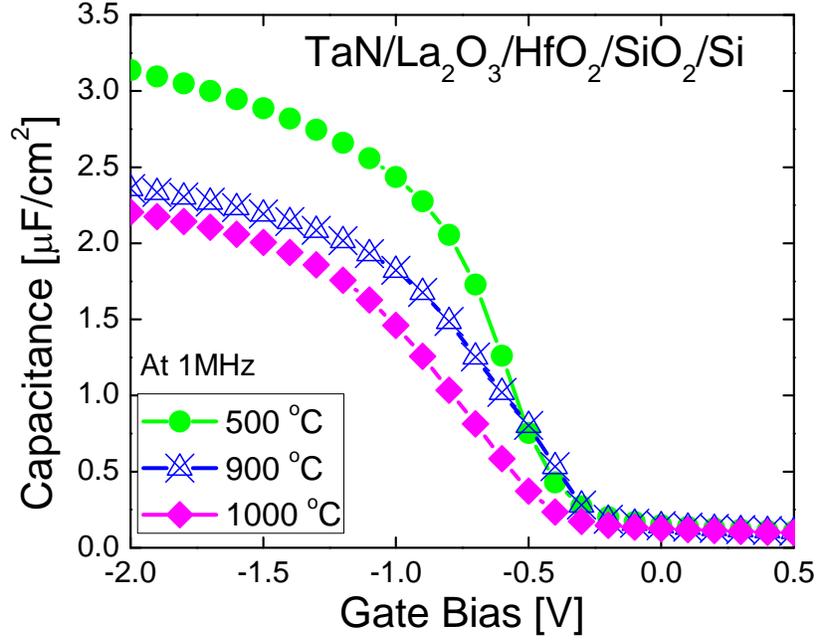


Figure 4.10 (a) C – V characteristics and (b) extracted  $V_{\text{FB}}$  and hysteresis ( $\Delta V_{\text{FB}}$ ) over temperature for TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub>/Si capacitor (Latop).

Figure 4.10 (a) shows C–V curves for TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub>/Si capacitor (called La–top hereafter) with 3 different temperature ranges. Device flatband voltage stays nearly constant up to 900°C then decreased after 1000°C implying that the presence of La<sub>2</sub>O<sub>3</sub> on top of HfO<sub>2</sub> has a minimal impact on V<sub>FB</sub> shift for temperature range less than 1000°C and La<sub>2</sub>O<sub>3</sub> must diffuse in or through the HfO<sub>2</sub> layer in order to modulate device V<sub>FB</sub>. Accumulation capacitance reduced as temperature increases due to the interfacial layer growth. Figure 4.10 (b) plots extracted V<sub>FB</sub> and hysteresis as a function of temperature. Extracted flatband voltages are -0.58V, -0.56V, and -0.75V for 500°C, 900°C, and 1000°C respectively whereas hysteresis remained the same over the entire temperature range. Therefore the V<sub>FB</sub> shift is not originated from the trapped charge since HfO<sub>2</sub>/SiO<sub>2</sub> controls shows similar level of hysteresis with temperature. This also confirms that V<sub>FB</sub> shift is attributed to the La diffusion through the high-*k* layer or the intermixing of La atoms with high-*k* since only high temperature data shows modulation of V<sub>FB</sub>. Figure 4.11 (a) shows C–V curves for TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>/Si capacitor (called La–bot hereafter) with temperatures. It is clearly observed that the C–V curves are shifted further negative to begin even after low temperature annealing (400°C and 500°C) and move toward positive flatband voltages after high-T annealing (900°C and 1000°C) unlike the Latop sample. It is also noticed that the EOT change with temperatures is less as compared to Latop sample. Figure 4.11 (b) shows the extracted V<sub>FB</sub> and hysteresis as a function of temperature. Almost 1 V more negative shift in V<sub>FB</sub> than the control sample was observed in the presence of La<sub>2</sub>O<sub>3</sub> between the HfO<sub>2</sub> and SiO<sub>2</sub> layers with large hysteresis for temperatures up to 500°C indicating the intrinsic trapped charges are also contributed to the V<sub>FB</sub> shift [124].

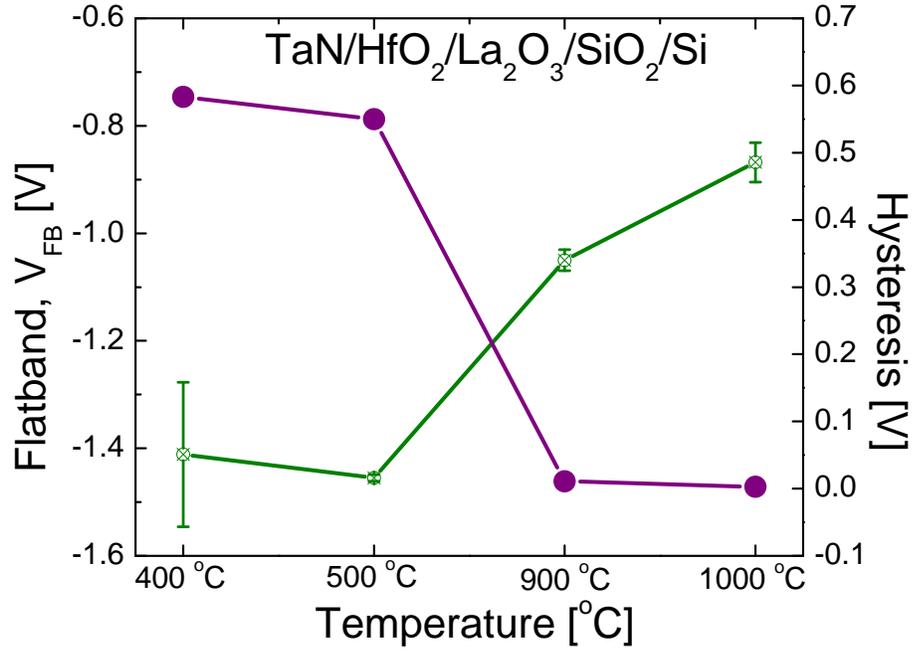
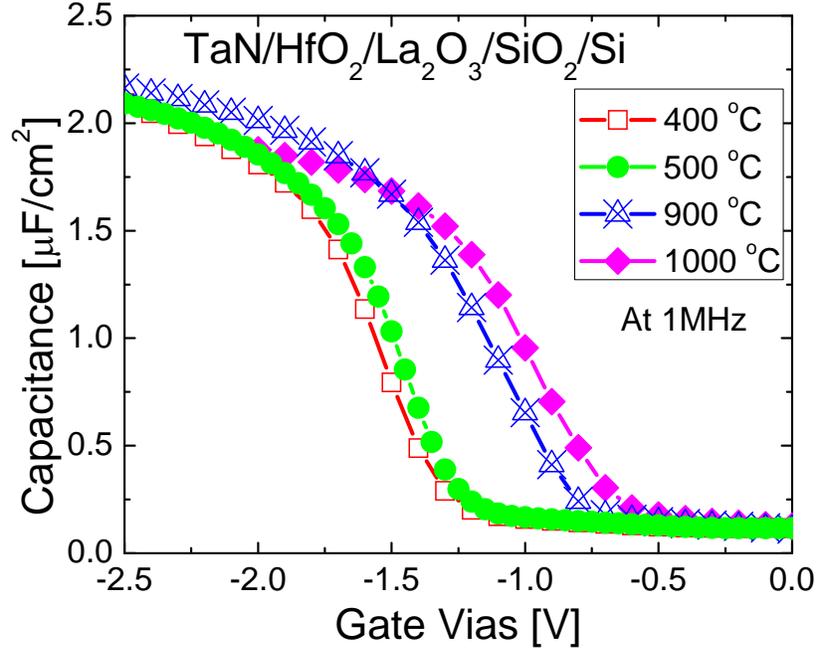


Figure 4.11 (a) C–V characteristics and (b) extracted  $V_{\text{FB}}$  and hysteresis ( $\Delta V_{\text{FB}}$ ) over temperature for TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>/Si capacitor (Labot).

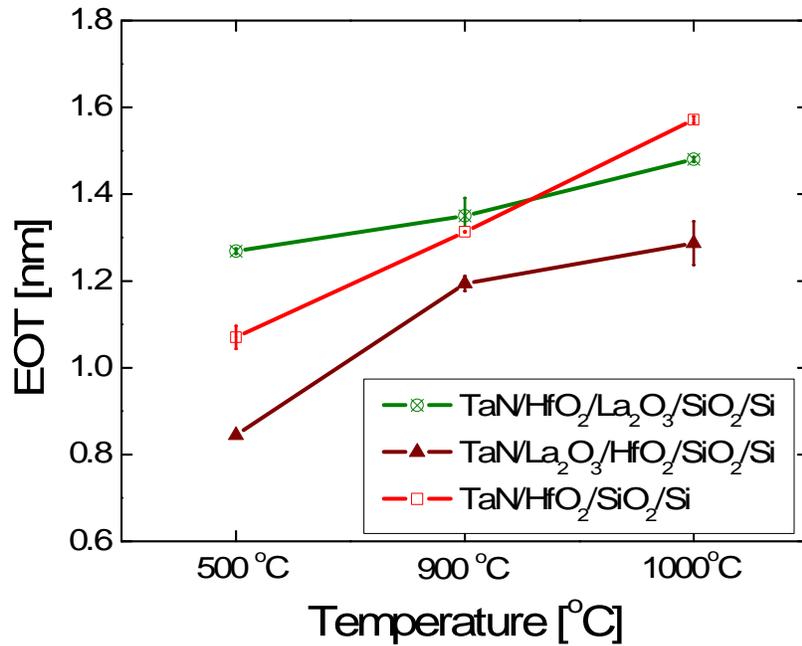
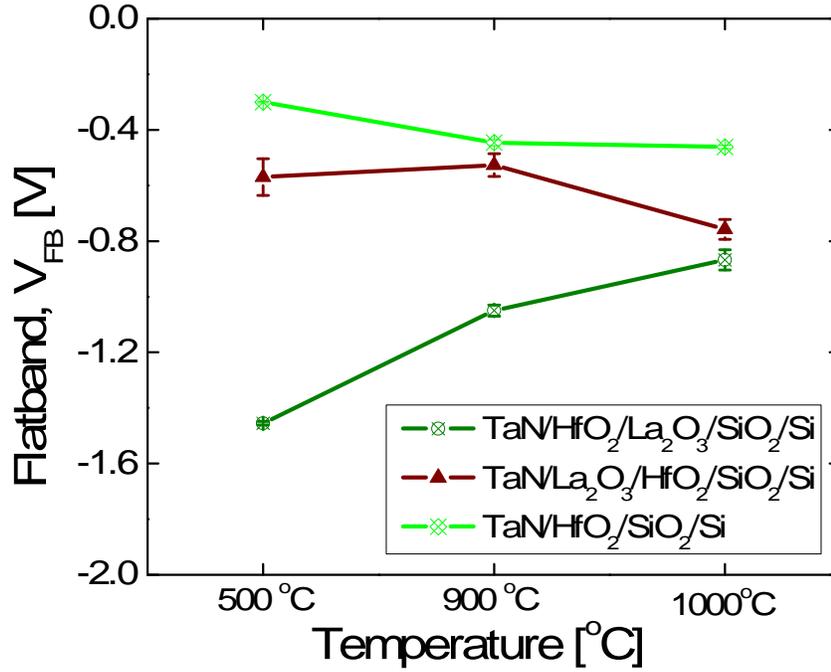


Figure 4.12 Comparison of samples for (a) extracted  $V_{FB}$  vs. temperature and (b) EOT vs. temperature. It is confirmed that the presence of La shifted  $V_{FB}$  of the gate stack.

However, after 900°C the amount of hysteresis is greatly reduced similar to the Latop sample whereas  $V_{FB}$  is still more negative than Latop sample. This clearly suggests that the  $V_{FB}$  shift by the presence of  $La_2O_3$  originates from the  $HfO_2/SiO_2$  interface and depends on the amount of La at the bottom interface since the main difference between Latop and Labot samples is the availability of La atoms (or concentration) at the  $HfO_2/SiO_2$  interface. Figure 4.12 compares extracted  $V_{FB}$  and EOT for all sample conditions in the temperature range from 500°C to 1000°C. After 1000°C annealing,  $V_{FB}$  with Labot sample is at least 100mV more negative than Latop sample. The EOT behavior over temperature is quite different and depends on the location of  $La_2O_3$  layer. Both  $HfO_2$  and Latop samples gain about 5 or 6 Å of EOT whereas Labot sample is only increased 2 or 3 Å after 1000 °C annealing.

In order to investigate the chemical information at the bottom interface, a XPS study was carried out. XPS spectra were collected using an Al ka monochromatic X-ray source with electron energy analyzer in a 20eV of constant pass energy. Substrate Si-Si peak was used to calibrate peak positions as stated before. Figure 4.13 shows the Si 2s spectra for both Latop and Labot samples after low (500°C) and high (1000°C) temperature annealing. It is noted that the spectra are normalized with respect to Si-Si peak from the substrate for comparing the relative peak intensity and position. When La atoms are present at the bottom interface to begin with, the oxide layer is converted to a silicate layer due to the more favorable reaction of silicate formation than oxide [125]. This silicate formation is clearly observed from the XPS spectra from the 500°C data. After 1000°C annealing second peak at 153.3eV in Si 2s spectra increased and shifted slightly toward higher binding resulting in the growth of interfacial  $SiO_2$  at the expense of La-silicate.

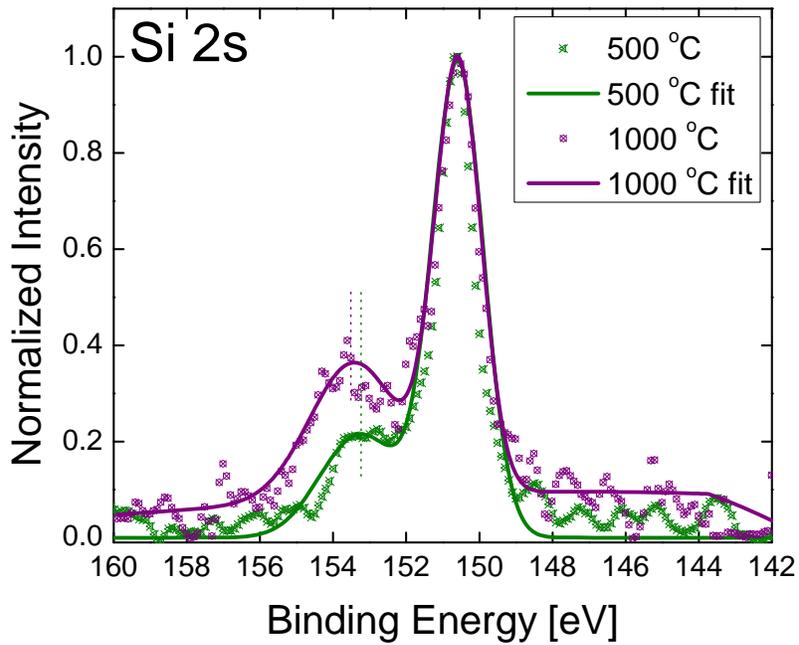
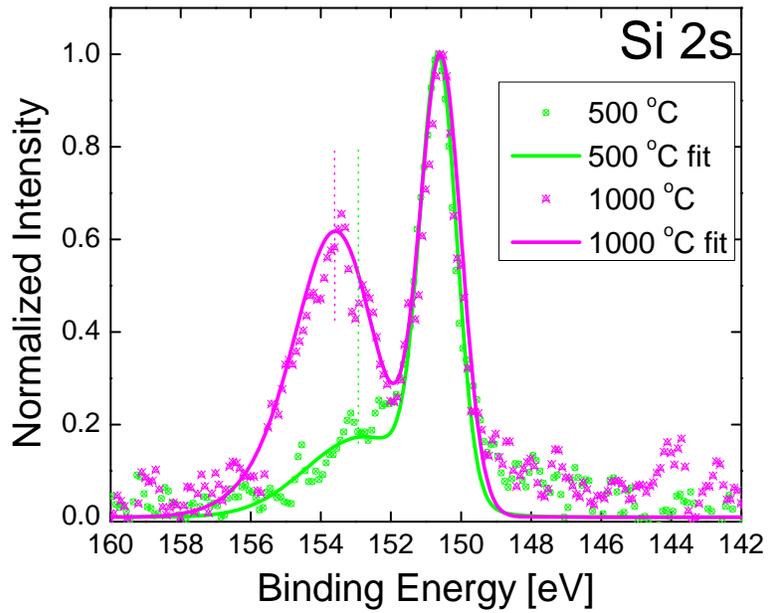


Figure 4.13 Normalized Si 2s XPS spectra after low (500°C) and high temperature (1000°C) annealing for (a) TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub>/Si capacitor and (b) TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>/Si capacitor. The location of La<sub>2</sub>O<sub>3</sub> layer can significantly change interface SiO<sub>2</sub> layer.

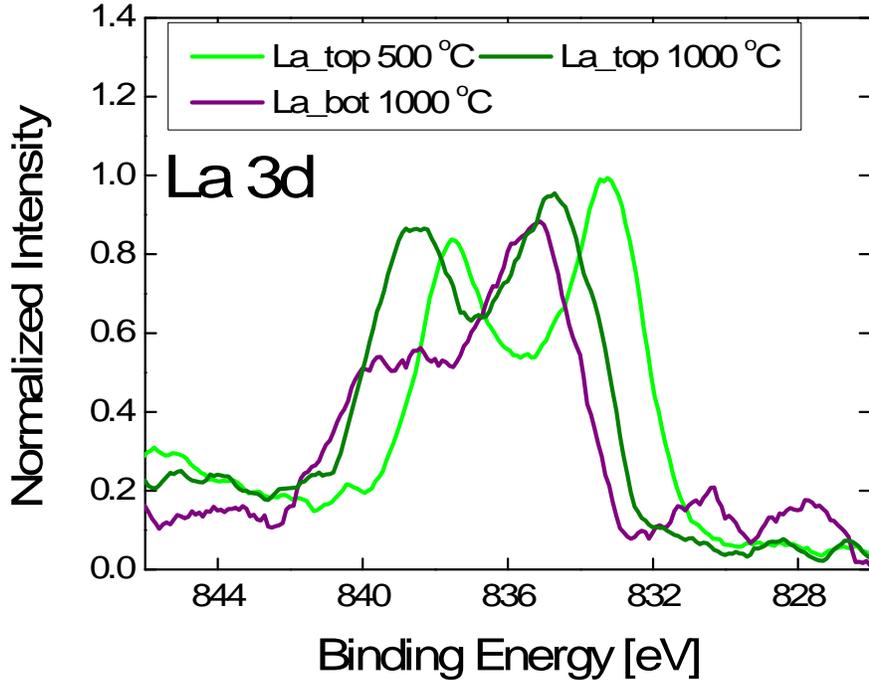


Figure 4.14 XPS spectra of La 3d indicating La diffusion through HfO<sub>2</sub> after 1000°C.

When La<sub>2</sub>O<sub>3</sub> layer is present at the top of the HfO<sub>2</sub> layer, the bottom interface configuration is quite different. After 500°C only Si–Si peak and Si–O peak are detected. When the sample is annealed at 1000°C, intensity from Si–O bonding increases with small indication of silicate formation. The growth of an interfacial layer is typically observed with HfO<sub>2</sub>/SiO<sub>2</sub> stack and the presence of La<sub>2</sub>O<sub>3</sub> on top of HfO<sub>2</sub> is expected to be similar to HfO<sub>2</sub> whereas the presence of La<sub>2</sub>O<sub>3</sub> below the HfO<sub>2</sub> layer can suppress interfacial layer growth caused by the silicate formation. This XPS result is consistent with EOT data extracted from C–V curve and it is concluded that the EOT gain with TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub>/Si stack is mainly attributed to the interfacial layer growth whereas EOT increase with TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>/Si stack consists of interfacial layer growth as well as low-*k* silicate

formation. The evidence of silicate formation is also confirmed by La 3d spectra as shown in Fig. 4.14. The peak position for the Latop sample after 500°C indicates La–O bonding. This peak is shifted toward a higher binding energy state indicating La–O–Si like formation. However, the peak position is slightly less than La 3d from Labot sample suggesting that the silicate formation plays a critical role in the  $V_{FB}$  shift.

As mentioned earlier the distance between Si channel and high- $k$  layer is critical for flatband voltage modulation as proposed by J. M. LeBeau et al., [111]. Our experimental results suggest that the  $V_{FB}$  with Labot samples is more negative than Latop samples. Therefore it can be concluded that the La induced  $V_{FB}$  shift is more pronounced than the interfacial thickness effect (proximity) on  $V_{FB}$ . According to the dipole model proposed by Sivasubramani et al., a magnitude of  $V_{FB}$  shift can be determined by the difference in electronegativity between RE atoms and Hf atoms [126]. However, a recent study has shown that some RE oxides do not follow the relation [127]. Therefore  $V_{FB}$  shift caused by  $La_2O_3$  cannot be simply explained by the electronegativity concept but should be carefully examined in terms of deposition conditions, the quality of the host high- $k$  layer, and/or annealing condition. Based on our experimental data, it is confirmed that the La atoms must be present at the bottom interface near the channel to provide desired  $V_T/V_{FB}$  value.

Figure 4.15 demonstrates the proposed mechanism explaining the  $V_{FB}$  shift caused by  $La_2O_3$  incorporation observed from capacitance measurements. As shown in Fig. 4.15 (a) the presence of  $La_2O_3$  on top of  $HfO_2$  layer requires high temperature (at least 900°C but higher temperatures are better for obtaining large shifts) in order for La atoms to diffuse through  $HfO_2$  layer. Once La atoms reach at the  $HfO_2/SiO_2$  interface, they are converted to silicate

and form the dipole layer. In case with  $\text{La}_2\text{O}_3$  on the bottom of the  $\text{HfO}_2$  dielectric, La atoms consumes  $\text{SiO}_2$  layer to form silicate with maximum concentration at low temperature, then the interfacial layer starts to grow with high temperature annealing since the availability of La atoms are limited.

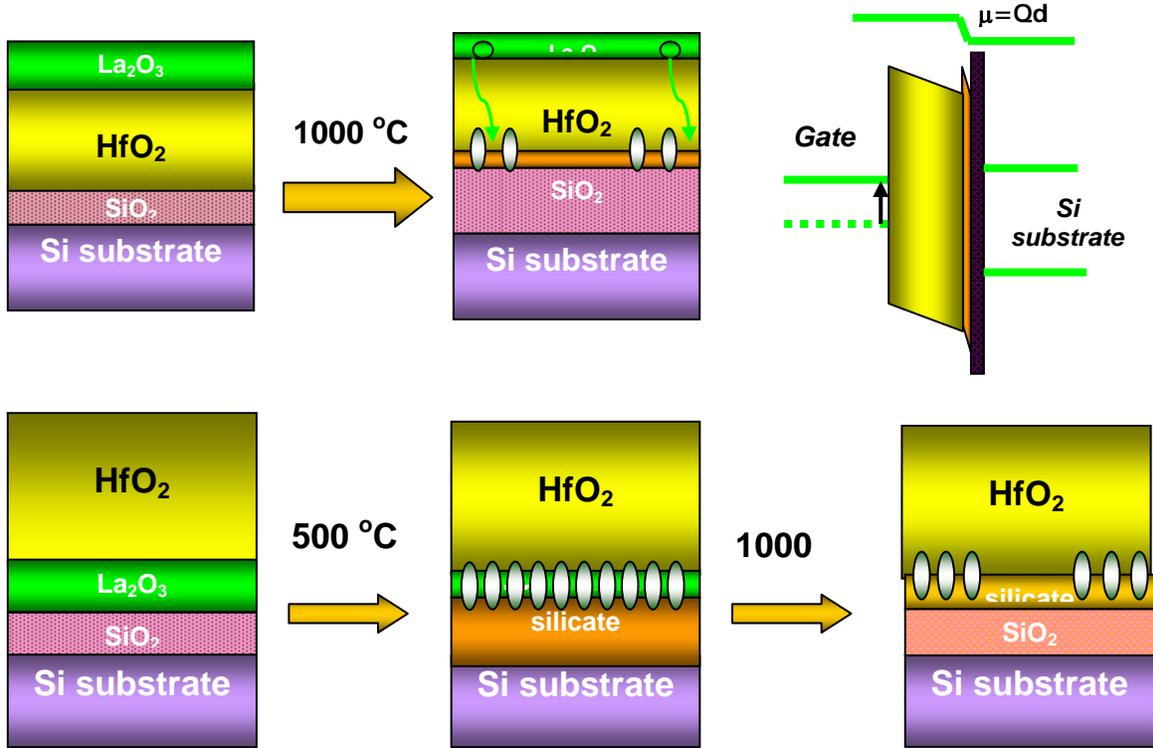


Figure 4.15 Schematic representations of dielectric stack with (a)  $\text{La}_2\text{O}_3/\text{HfO}_2/\text{SiO}_2$  stack and (b)  $\text{HfO}_2/\text{La}_2\text{O}_3/\text{SiO}_2$  stack with temperature.

### 4.4.3 Transistor Results

In the previous section, it was clarified that the main mechanism responsible for  $V_T/V_{FB}$  shifts with  $\text{La}_2\text{O}_3$  capping is attributed to the dipole formation and/or fixed charge caused by the presence of La atoms at the high- $k/\text{SiO}_2$  interface. In this section, the electrical characteristics such as mobility as well as reliability of the transistor with capping layer are evaluated.

#### 4.4.3.1 Basic Electrical Results

The nMOSFET devices with and without capping layers on  $\text{HfO}_2$  dielectrics and control  $\text{SiO}_2$  dielectrics without capping were fabricated as outlined in Chapter 2.

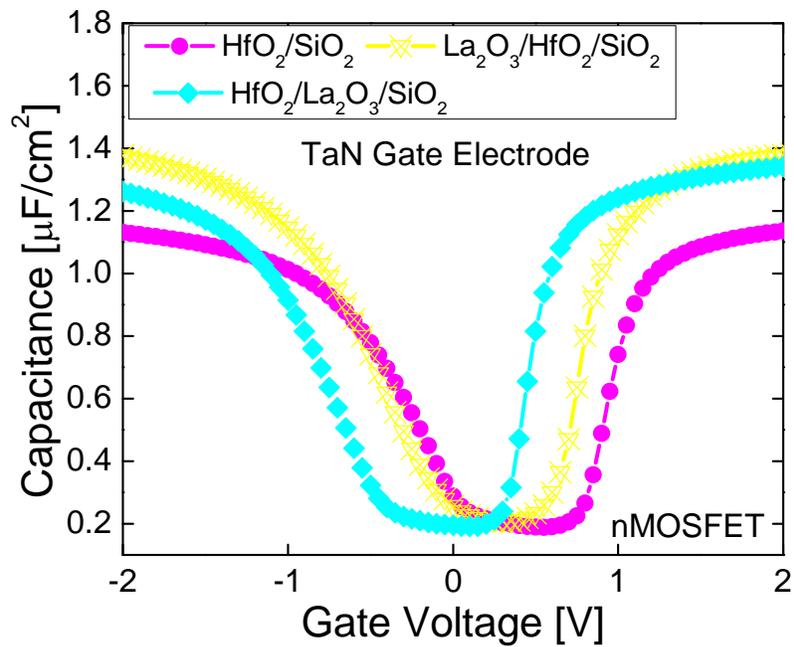


Figure 4.16 Capacitance–Voltage Curves for transistors

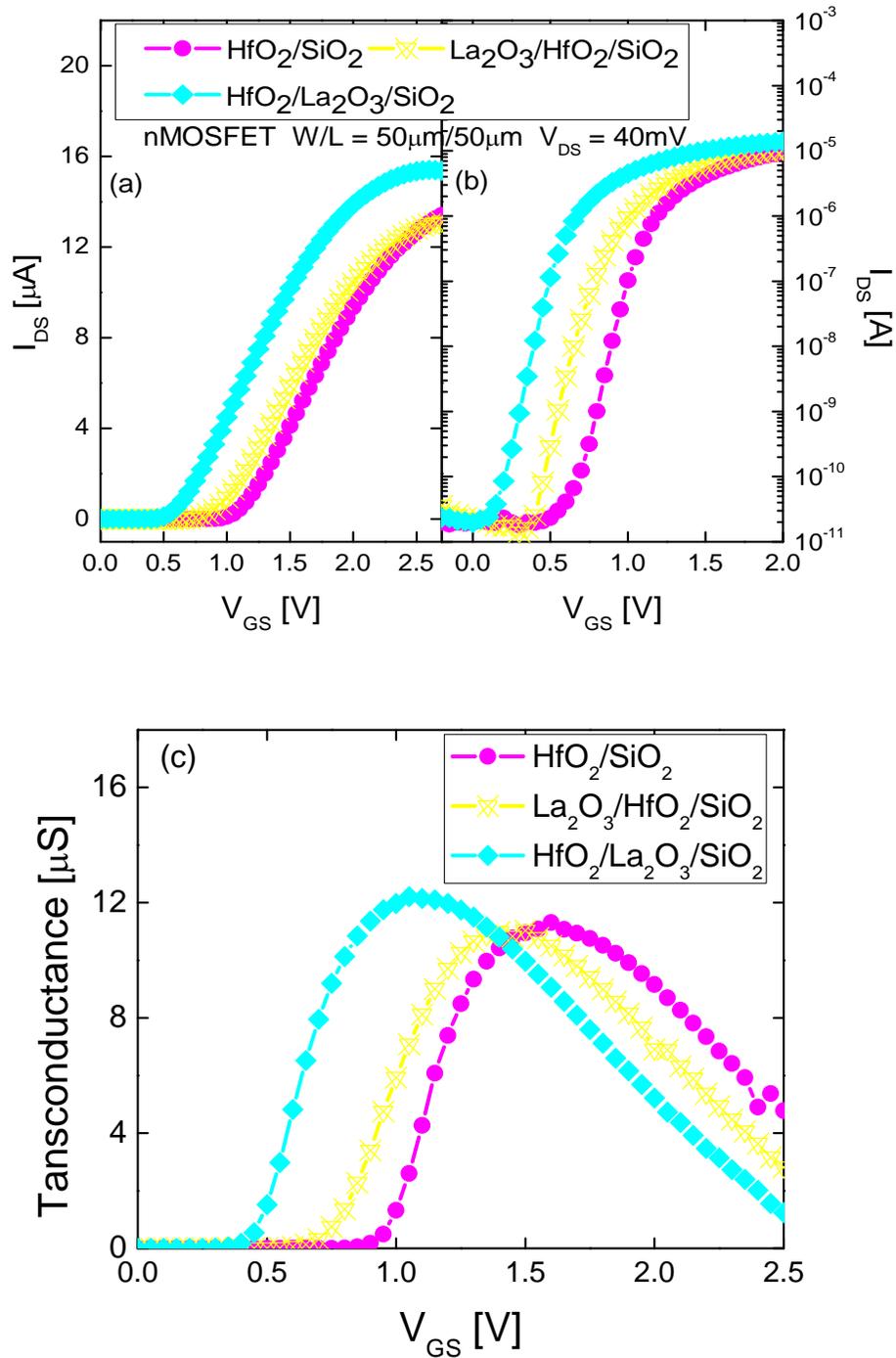


Figure 4.17 (a) Linear  $I_{ds} - V_{gs}$  curve and (b)  $\log(I_{ds}) - V_{gs}$  curve for transistors.  $V_T$  is shifted with  $\text{La}_2\text{O}_3$  insertion from  $\text{HfO}_2$  as expected and large shift in  $V_T$  is obtained when  $\text{La}_2\text{O}_3$  is placed between  $\text{HfO}_2$  and  $\text{SiO}_2$  layer. Plot (c) is corresponding transconductance.

Figure 4.16 shows the high frequency C–V curves with TaN gate electrodes for 35Å HfO<sub>2</sub>/SiO<sub>2</sub> control, Latop (5Å La<sub>2</sub>O<sub>3</sub>/30Å HfO<sub>2</sub>/SiO<sub>2</sub>), and Labot (30Å HfO<sub>2</sub>/5Å La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>) samples respectively. It is observed that all devices show good device characteristics. The incorporation of a capping layer modulates device  $V_T/V_{FB}$  from the HfO<sub>2</sub> control values and the TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> (Labot) stack shows larger  $V_T/V_{FB}$  modulation than TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> (Latop) stack, agreed with the capacitor results from the previous section. The incorporation of La<sub>2</sub>O<sub>3</sub> layer can also increase the inversion capacitance due to the higher  $k$  formation by the reaction of HfO<sub>2</sub> and La<sub>2</sub>O<sub>3</sub>. Figure 4.17 plots  $I_{ds}-V_{gs}$  characteristics with transistors after 1000°C annealing for both linear and log scale and clearly demonstrates the  $V_T$  tuning effect by La<sub>2</sub>O<sub>3</sub> capping incorporation corresponding well with the capacitance results. The extracted  $V_T$  for HfO<sub>2</sub>, Latop, and Labot samples are 1.05V, 0.95V, and 0.55V respectively. It is noted that the high  $V_T$  value is attributed to the higher doping of the p–type substrate ( $6 \times 10^{17} / \text{cm}^3$ ). It is also noted that less shift in  $V_T$  is seen with Latop samples than with Labot samples, which is attributed to incomplete diffusion of La atoms through the thick HfO<sub>2</sub> layer (3.5nm based on TEM measurement) at the given thermal budget. The subthreshold slope is slightly high ( $> 85$  mV/decade) for all samples compared to SiO<sub>2</sub> control and this is attributed to the high interface states density which was confirmed with charge pumping measurements (discussed later). The corresponding transconductance characteristics are also shown in Fig. 4.17 (b). Well behaved drive current characteristics were obtained for two different over drive voltages ( $V_{gs}-V_T$ ) as shown in Fig. 4.18. Table 4.1 summarizes the key parameters such as EOT,  $V_T/V_{FB}$ , subthreshold swing (S), and  $G_m$  extracted from C–V and I–V curves of the transistors.

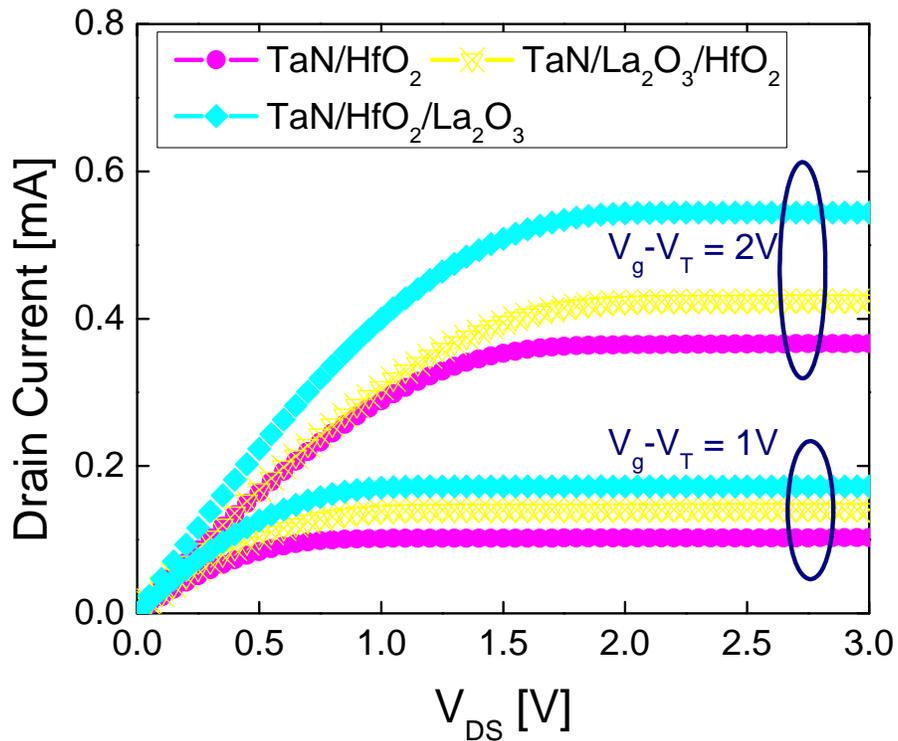


Figure 4.18  $I_{ds}$ - $V_{ds}$  characteristics with  $V_{gs}-V_T=1V$  and  $2V$ .

Table 4.1 Key parameters extracted from C-V and I-V measurements

	HfO <sub>2</sub>	La <sub>2</sub> O <sub>3</sub> /HfO <sub>2</sub> /SiO <sub>2</sub>	HfO <sub>2</sub> /La <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub>
EOT (nm)	<b>2.6</b>	<b>2.127</b>	<b>2.24</b>
$V_{FB}$ (V)	<b>-0.316</b>	<b>-0.587</b>	<b>-0.811</b>
$V_T$ (V)	<b>1.05</b>	<b>0.95</b>	<b>0.55</b>
$G_{m, peak}$ (uS)	<b>10.5</b>	<b>10</b>	<b>12.5</b>
Subthreshold Swing	<b>91</b>	<b>105</b>	<b>85</b>

### 4.4.3.2 Mobility

Figure 4.19 shows the effective electron mobility of the samples as a function of effective electric field extracted using the split C–V method. Device areas of  $50\mu\text{m} \times 50\mu\text{m}$  were chosen for mobility extraction to avoid the geometric effects and series resistance issues. A correction for gate leakage was also employed for  $I_{\text{ds}}-V_{\text{gs}}$  curves in order to determine accurate mobility values. As seen in Fig. 4.19 peak mobility value is reduced from the universal mobility curve not only with high- $k$  dielectrics but also with  $\text{SiO}_2$  control samples. It is well known that effective mobility at low effective field can be degraded as interface state density increases since the coulomb scattering component is dominant if interface state densities are high as mentioned in chapter 2.

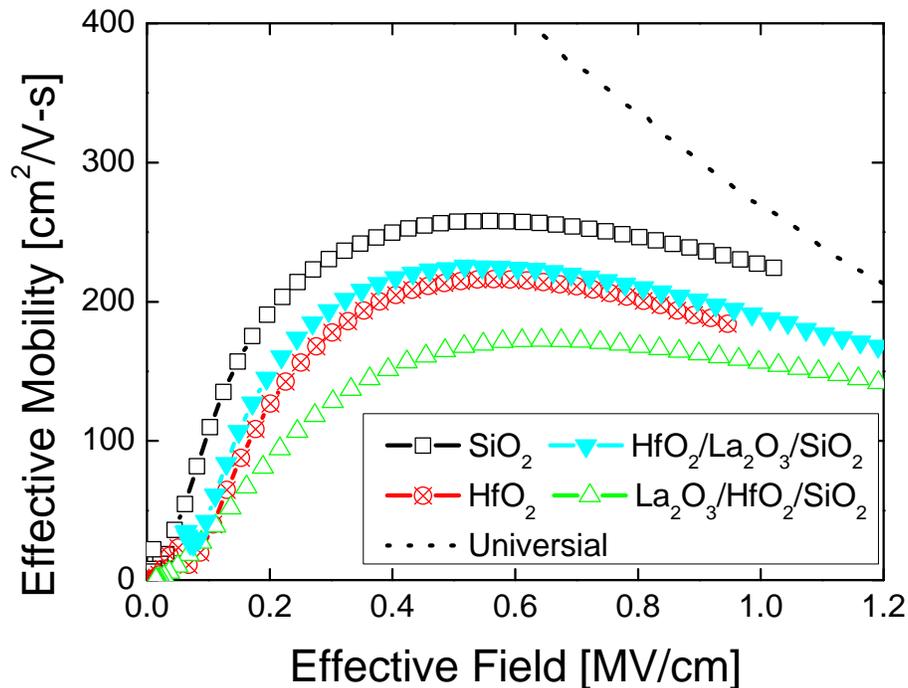


Figure 4.19 Effective mobility of transistors at room temperature ( $25^\circ\text{C}$ )

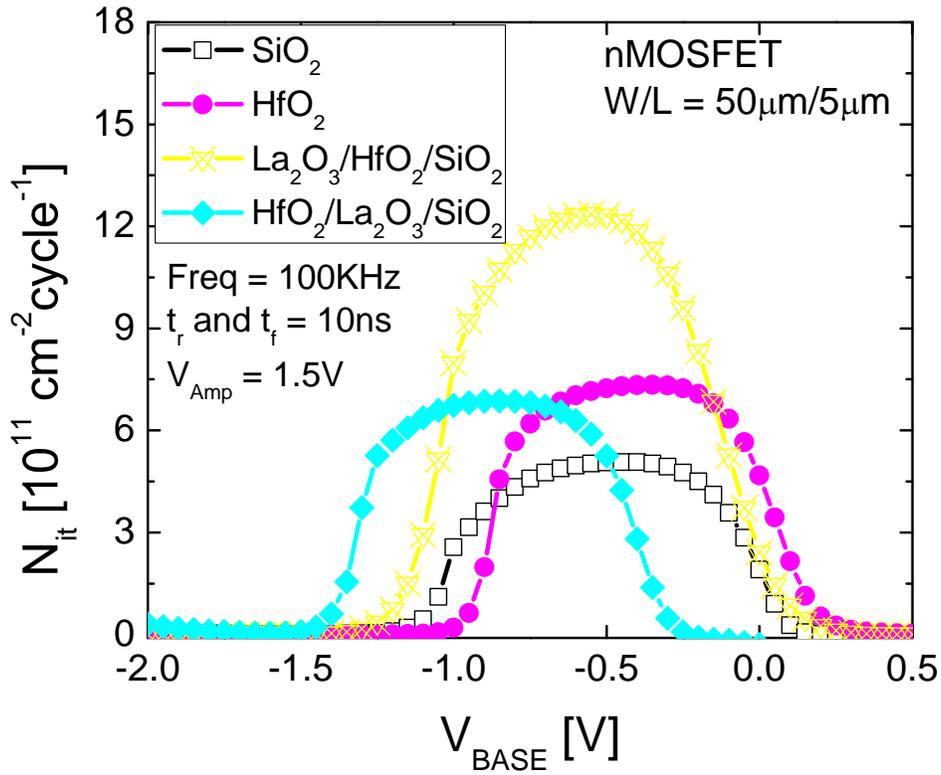


Figure 4.20 Base level charge pumping results

Table 4.2 Summary of mobility value and interface state density

	<b>HfO<sub>2</sub></b>	<b>La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub></b>	<b>HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub></b>
<b>μ<sub>eff, peak</sub> (cm<sup>2</sup>/V-s)</b>	220	178	240
<b>μ<sub>eff</sub> at E<sub>eff</sub>=1MV/cm</b>	177	156	192
<b>N<sub>it</sub> (cm<sup>-2</sup> cycle<sup>-1</sup>)</b>	7.4 X 10 <sup>11</sup>	1.23 X 10 <sup>12</sup>	7.2 X 10 <sup>11</sup>

In order to extract average interface state density, the two level charge pumping measurement with base level sweep was performed on transistors with area of 50 $\mu\text{m}$  X 5 $\mu\text{m}$ . Figure 4.20 shows charge pumping characteristics taken at 100 KHz with 10ns of rise/fall time. The extracted  $N_{it}$  value is 4X10<sup>11</sup>/cm<sup>2</sup> for SiO<sub>2</sub> which is one order of magnitude higher than typical thermally grown SiO<sub>2</sub> (< 5X10<sup>10</sup> /cm<sup>2</sup>). Moreover, the extracted  $N_{it}$  values for high- $k$  dielectrics are even higher (> 6X10<sup>11</sup>/cm<sup>2</sup>). This high interface state is attributed to the insufficient FGA after transistor device fabrication (400°C 5 min in RTA). Table 4.2 summarizes the peak mobility, high field mobility and average interface state density suggesting that the peak mobility degradation is related to extracted interface state density. It is noted that the coulomb scattered mobility is inversely proportional to the doping density and interface charge as modeled by S. Villas et al., [128] and expressed as

$$\mu_{Coulomb} = \frac{\gamma N_{inv}}{\alpha N_A + \beta N_{it}} \quad (4.3)$$

where  $\gamma$  is  $N_{it}$  scattering factor,  $\beta$  is obtained from non-linear regression analysis, and  $\alpha$  is a fitting parameter. Figure 4.21 compares the theoretical coulomb component of mobility calculated from Equation 4.3 and experimental data taken from split C-V technique showing that the experimental data agree well with the theoretical calculation. It has been reported that the coulomb component of mobility is solely limited by scattering from the interface states when  $N_{it}$  is larger than 6X10<sup>11</sup> cm<sup>-2</sup> [129] and therefore the reduction in mobility with high- $k$  dielectric shown in Figure 4.19 is possibly attributed to the scattering from the high interface states.

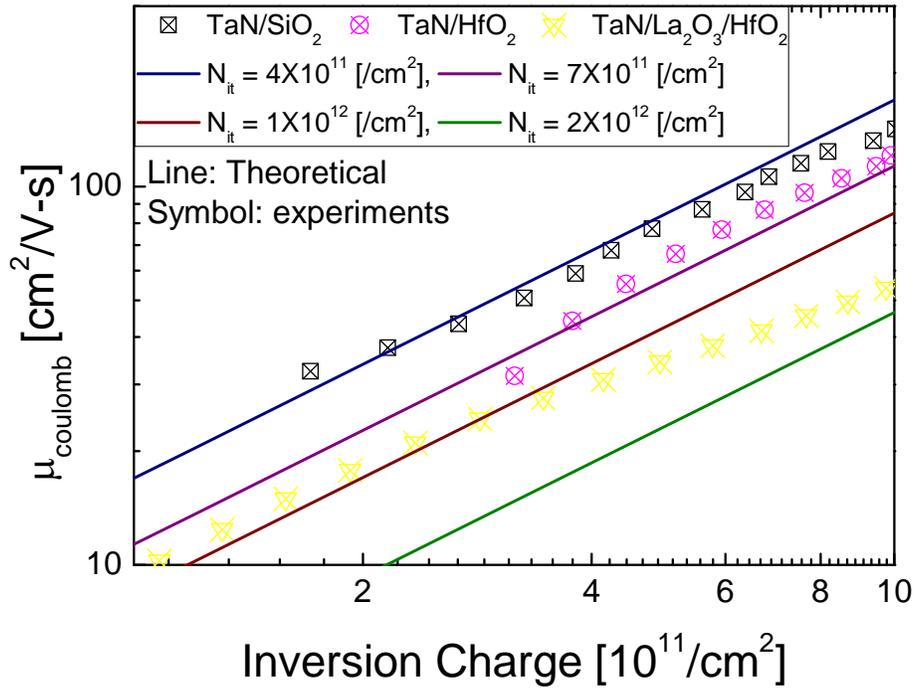


Figure 4.21 Coulomb components of Mobility extracted from Matthiesen’s rule for different  $N_{it}$ ’s. Charge pumping result shows similar level of  $N_{it}$  values.

In order to further evaluate the impact of additional scattering components on the mobility degradation with high- $k$  dielectrics, a temperature study was carried out. It is well known that phonon scattering with high- $k$  dielectrics is also key factor for mobility degradation. Phonon scattering dominates at high temperatures and as a result the effective channel mobility decreases. Figure 4.22 shows mobility curves for the temperature range from 25°C to 125°C extracted by the split C-V method. The mobility values for all samples were reduced as temperature increased due to an increase in the phonon scattering component. It is interesting to see that the temperature dependency of mobility degradation is inversely proportional to the interface state density. In other words, TaN/SiO<sub>2</sub> sample shows a large

temperature dependency of the mobility, whereas the least changes in mobility with temperature occurs for the TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> sample which is attributed to the fact that the mobility is already influenced by high interface states and thus less sensitive to the phonon scattering.

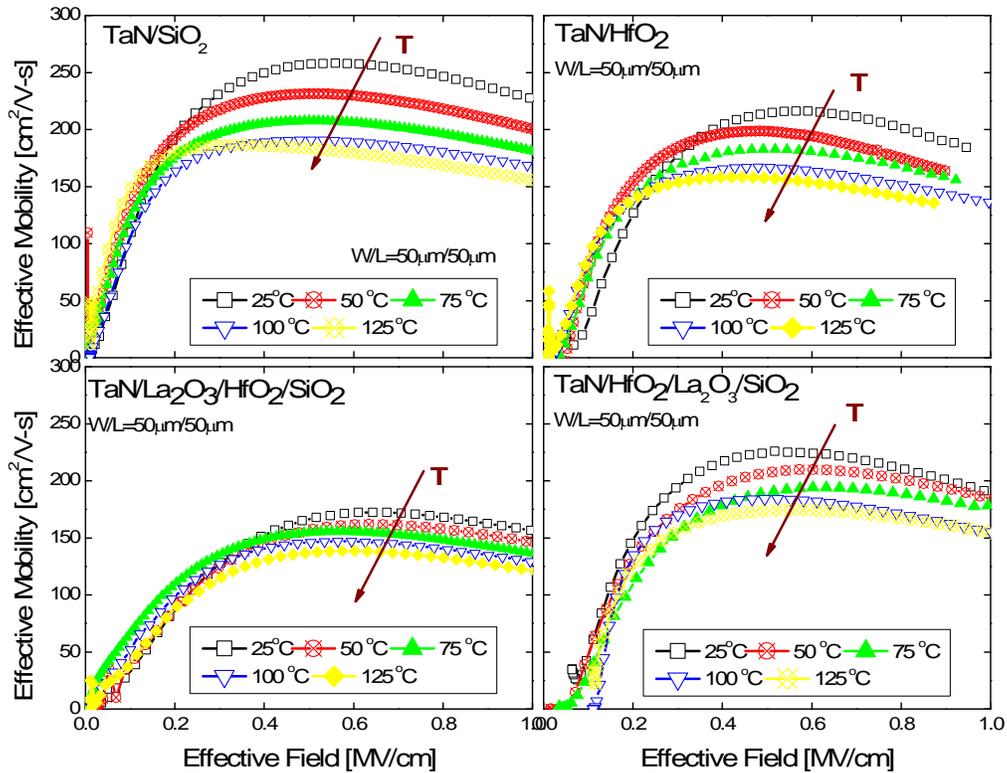


Figure 4.22 Effective mobility vs. temperatures for nMOSFET device with various dielectrics. Least temperature dependency with TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub>/Si stack due to the larger interface state.

Figure 4.23 shows peak mobility variation over temperature ranges where the solid line shows a polynomial fit to the extracted data points. It is clearly shown that the slope of

TaN/HfO<sub>2</sub> and TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> stacks is similar to SiO<sub>2</sub> whereas the slope of TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack clearly shows less dependence over temperature ranges.

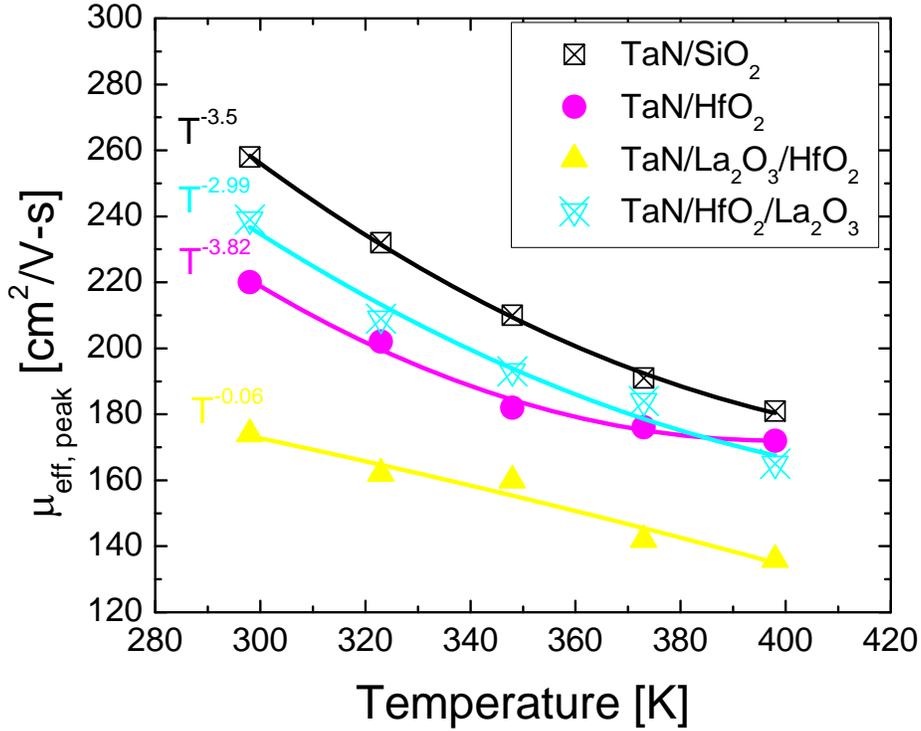


Figure 4.23 Peak mobility comparisons over temperature. TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack shows less dependency of mobility in temperature suggesting that the mobility degradation mechanism is different from other samples.

In order to decouple the coulomb scattering component from the phonon component, the temperature sensitivity factor (the rate of change of the reciprocal of effective mobility with respect to temperature,  $d(1/\mu_{\text{eff}})/dT$ ) has been introduced [29]. By taking reciprocal effective mobility with temperature, the net value of the temperature sensitivity factor is negative for the range where coulomb scattering is dominant, whereas the net value of this factor is positive for the effective field ranges where phonon scattering is dominant.

Therefore sensitivity factor plotted over effective field can provide information of the mobility dependency on the phonon component of the dielectric layer. It is shown that TaN/HfO<sub>2</sub> and TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack show similar temperature dependency as SiO<sub>2</sub> indicating the additional phonon scattering from the high-*k* layer has minimal impact on mobility. However, there is a larger temperature dependency with the TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> stack, indicating the additional phonon scattering effect from the high-*k* layer contributes to the mobility degradation although the overall dependency is less than reported HfO<sub>2</sub>/SiO<sub>2</sub> dielectric stack.

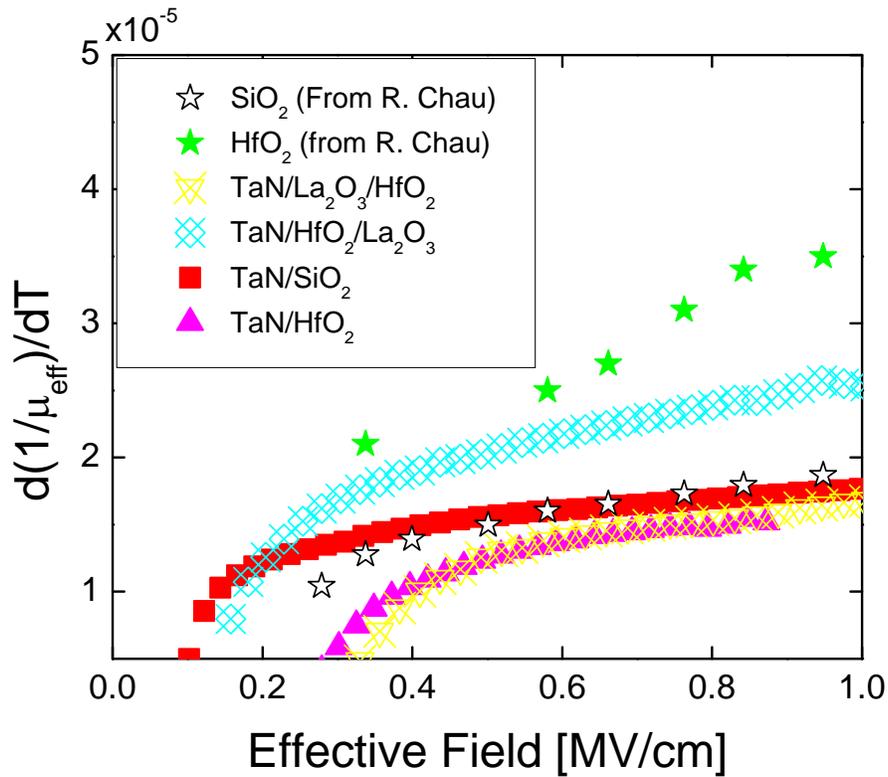


Figure 4.24 Mobility sensitivity factor. TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> gate stack shows higher sensitivity.

In order to confirm the interfacial layer quality and thickness as well as crystalline structure of the dielectric stack, Transmission Electron Microscopy (TEM) study was carried out. Figure 4.25 shows both high-resolution TEM (HR-TEM) and Z-contrast scanning TEM (STEM) images for TaN/HfO<sub>2</sub>/SiO<sub>2</sub>, TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub>, and TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> samples respectively. It is noted that control TaN/HfO<sub>2</sub>/SiO<sub>2</sub> sample (Fig. 4.25 (a) and (d)) has thick interfacial layer (2.2~2.4nm) with smooth interfaces to both the high-*k* and substrate. The presence of La in the dielectric stack reduced the interfacial layer thickness. About 3Å ~ 5Å of interfacial layer is reduced depending on the initial location of La atoms.

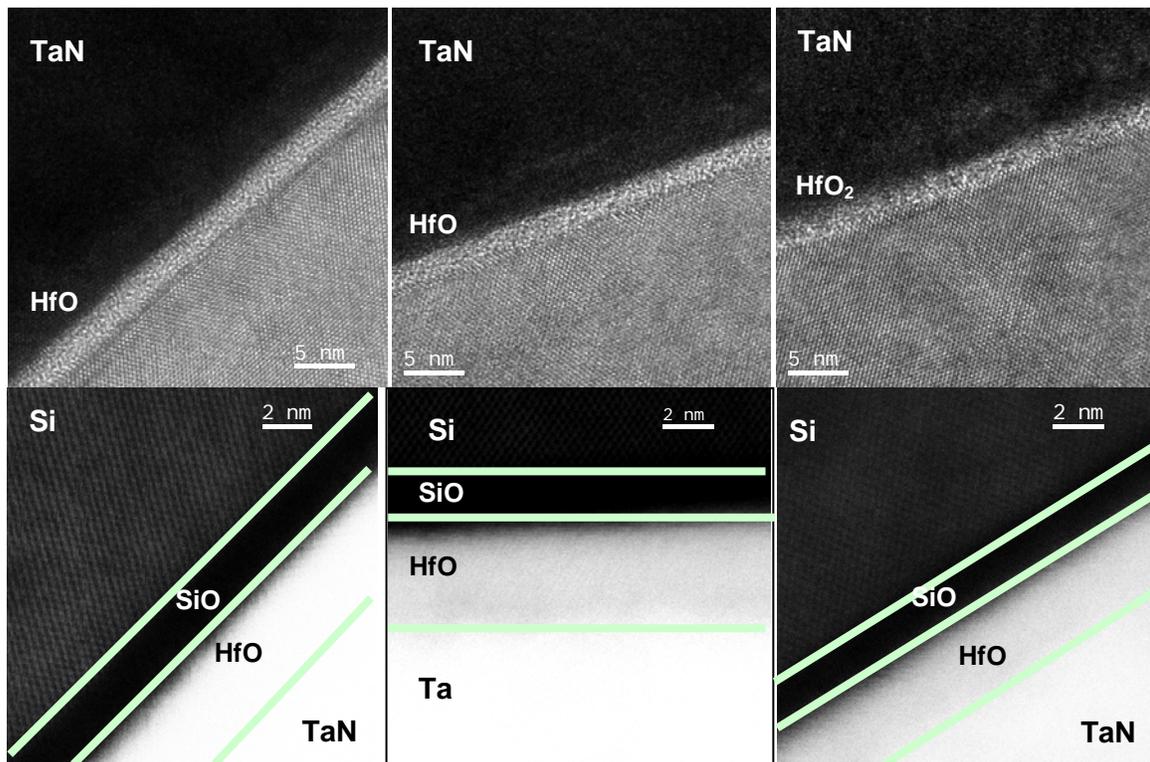


Figure 4.25 High-resolution TEM (HRTEM) and z-contrast STEM images for TaN/HfO<sub>2</sub>/SiO<sub>2</sub>, TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>, and TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub> samples after 1000°C annealing. The incorporation of La in the gate dielectric causes rough and thin interfacial layer.

This initial location of La atoms can significantly influence the quality of interfacial layer during or after high temperature annealing. When La atoms are present at the bottom of the HfO<sub>2</sub> layer to begin with, the interfacial layer is initially converted to a silicate during the post deposition annealing followed by re-growth of interfacial oxide layer after 1000°C [124] which has already been seen with the XPS study. When La atoms are present on top of the HfO<sub>2</sub> followed by subsequent annealing not only is the SiO<sub>2</sub> thickness reduced, but also decomposition of the SiO<sub>2</sub> layer occurs. This is attributed to the scavenging of low *k* material by Rare-earth materials as discussed in chapter 3. Z-contrast STEM imaging techniques were used to measure the thickness of HfO<sub>2</sub> as well as interfacial layer thickness accurately since HR-TEM images cannot distinguish the HfO<sub>2</sub> layer from the TaN gate electrode due to the measurement limit discussed in chapter 2. It is observed that the dielectric layer has two distinct layers for all three samples which correspond to a SiO<sub>2</sub> like (dark region) and HfO<sub>2</sub> layer (gray region). It is noted that the HfO<sub>2</sub> (gray region) layer between SiO<sub>2</sub> and TaN with La<sub>2</sub>O<sub>3</sub> incorporation is distinct on STEM images whereas it is still not clear even on STEM with TaN/HfO<sub>2</sub> sample. This is attributed to the presence of La in HfO<sub>2</sub> layer providing better contrast between TaN and HfO<sub>2</sub> since z-contrast scan strongly depends on the mass of the atoms. While the SiO<sub>2</sub> and HfO<sub>2</sub> layers are apparent, however, STEM results did not confirm the distinct La-oxide or silicate layer since only 5Å of La<sub>2</sub>O<sub>3</sub> was deposited and subsequently annealed at 1000°C. Although it is difficult to distinguish the location of La atoms, the XPS data confirmed the presence of La at the HfO<sub>2</sub>/SiO<sub>2</sub> interface.

The TEM images in Fig 4.25 reveal that the interfacial SiO<sub>2</sub> thickness is about 1.5nm to 2.2nm depending on the sample and hence the high-*k* phonon induced mobility

degradation mechanism can have minimal impact on the mobility degradation [129]. However, some of La atoms in the TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> stack might have diffused into the SiO<sub>2</sub> layer acting as the source of phonon scattering, which can explain the higher slope for TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> stack than other devices in the temperature sensitivity plot in Fig. 4.24. Therefore, it is concluded that the reduction in mobility for TaN/HfO<sub>2</sub> and TaN/La<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack is mainly attributed to the insufficient screening of Coulomb potential caused by large interface state density whereas both coulomb and phonon scatterings can affect the mobility for the TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> stack.

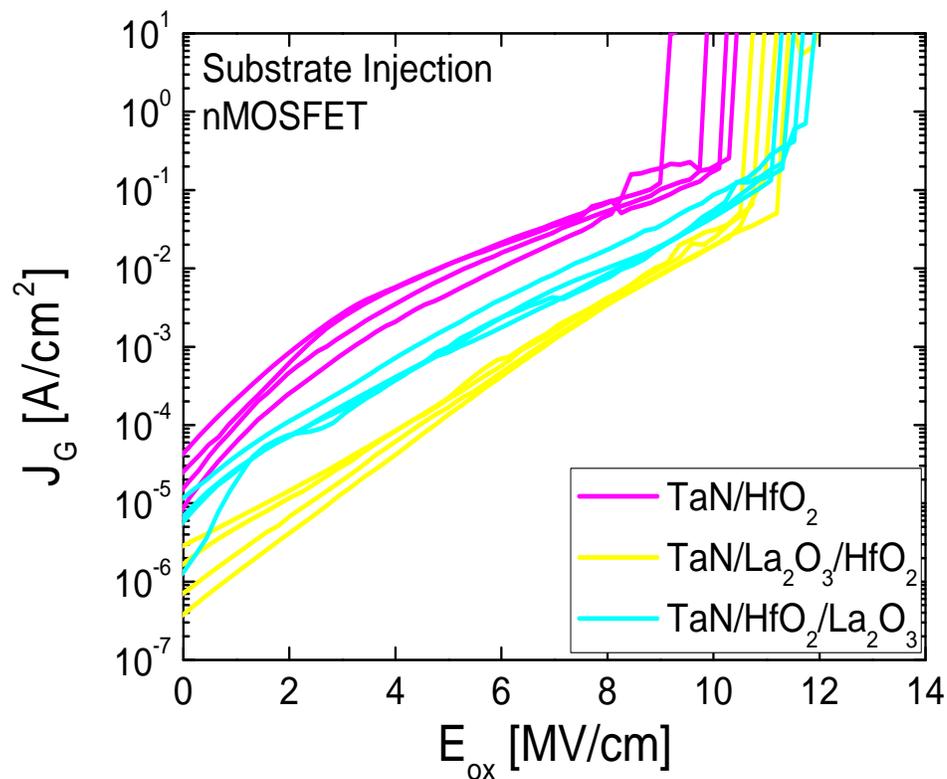


Figure 4.26 Gate Leakage characteristics of MOSFET devices for substrate injection. Presence of La in SiO<sub>2</sub> can create band offset resulting in retardation of electron tunneling [136].

#### 4.4.3.3 Impact of $\text{La}_2\text{O}_3$ capping on Reliability

The impact of  $\text{La}_2\text{O}_3$  incorporation on reliability was also evaluated by the gate leakage characteristics of the MOSFET as well as positive bias temperature instability (PBTI) techniques through the stress and sense measurement technique. Figure 4.26 shows gate leakage current density ( $J_G$ ) in the inversion condition as a function of the effective field across the gate oxide. It is observed that the incorporation of a  $\text{La}_2\text{O}_3$  dielectric reduces gate leakage current and improves dielectric breakdown characteristics as compared to control  $\text{HfO}_2$  sample. As discussed earlier the presence of La at the  $\text{HfO}_2/\text{SiO}_2$  interface creates dipole layer and this dipole layer effectively increases the barrier offset from the Si conduction band [130]. As a result of this barrier caused by dipole, electron tunneling from the Si channel is retarded resulting in gate leakage current reduction under the same field.

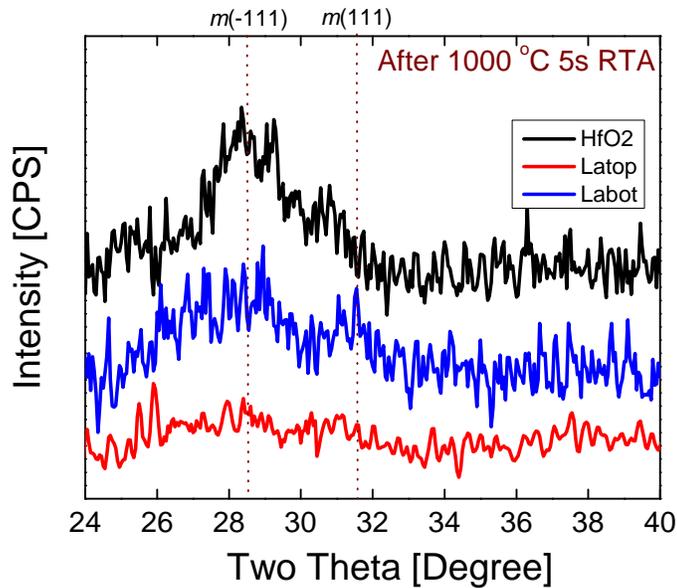


Figure 4.27 XRD of the samples after  $1000^\circ\text{C}$  annealing. Incorporation of La retards crystallization of  $\text{HfO}_2$ .

Moreover, crystalline HfO<sub>2</sub> dielectric itself also tends to have higher leakage current than amorphous dielectric due to presence of intrinsic defect sites. Figure 4.27 shows X-Ray Diffraction pattern (XRD) with and without La<sub>2</sub>O<sub>3</sub> capping layer on HfO<sub>2</sub> dielectric confirming that the incorporation of La<sub>2</sub>O<sub>3</sub> on HfO<sub>2</sub> mitigates the crystallization of HfO<sub>2</sub>. Therefore, the improvement in the leakage characteristics by the incorporation of La<sub>2</sub>O<sub>3</sub> is attributed to 1) the suppression of the trap generation caused by retardation of HfO<sub>2</sub> dielectric crystallization, 2) the passivation of existing bulk traps, and 3) an effective increase in the barrier height for electrons.

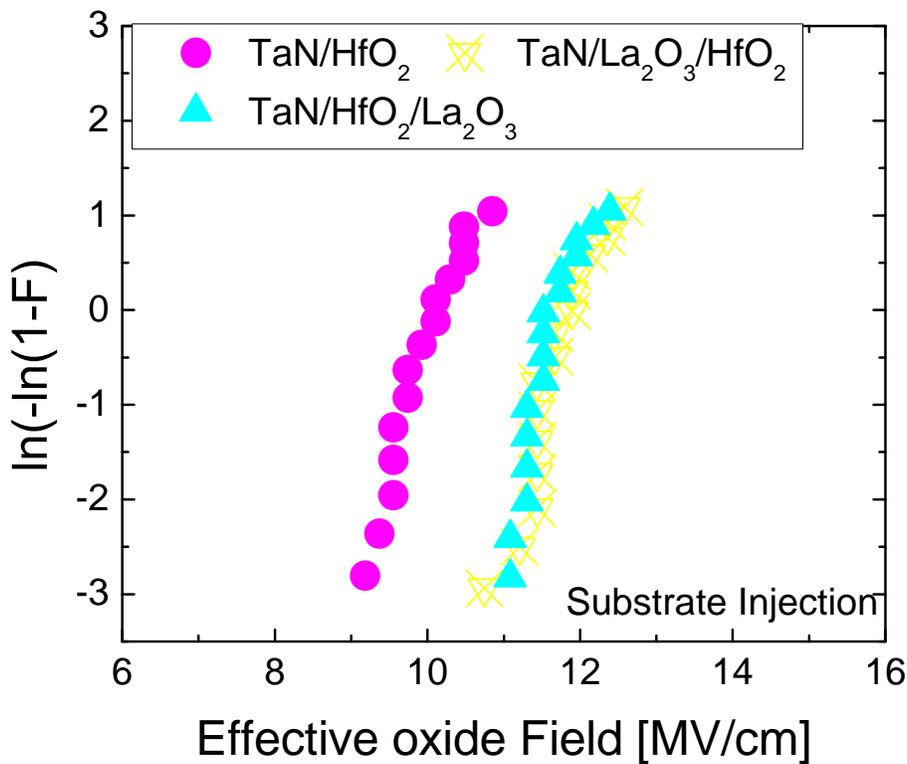


Figure 4.28 Weibull distribution plots for breakdown field. TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> gate stack provides tight and dense distribution.

Figure 4.28 represents Weibull distribution plot for the breakdown voltage. It is clearly observed that breakdown voltage is enhanced by the incorporation of  $\text{La}_2\text{O}_3$  in the dielectric stack. It is interesting to note that the breakdown characteristics are similar for Latop and Labot sample although the overall gate leakage characteristic is order of magnitude lower with Latop sample than Labot sample. This can be explained by the locally defective interfacial oxide in  $\text{TaN}/\text{HfO}_2/\text{La}_2\text{O}_3$  samples caused by the presence of La. This local defective interfacial layer might act as a trapping sites resulting in trap-assisted tunneling.

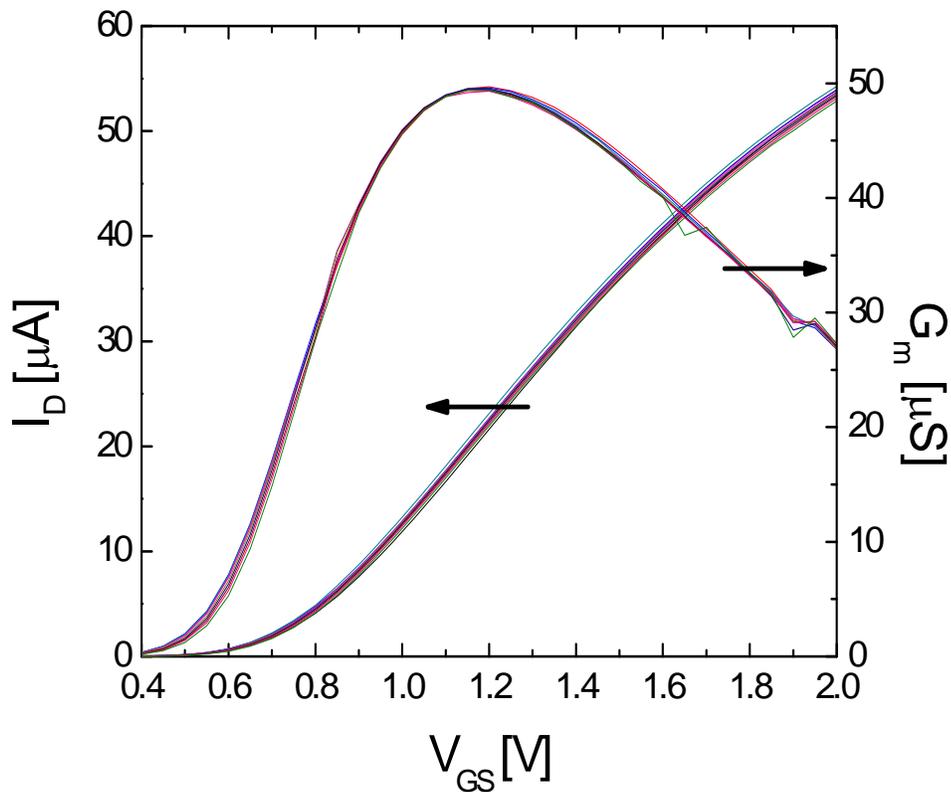


Figure 4.29  $I_{ds}$  and  $g_m$  variation over time

For the PBTI measurement constant voltage at elevated temperature was applied to the gate while source, drain, and bulk terminals were grounded. The  $I_{ds}-V_{gs}$  as well as  $N_{it}$  were monitored periodically during the stress. It is noted that this method cannot detect the fast trap/detrapping characteristics since the response time is about 0.7s to 1s between stress and sense whereas microsecond time is needed for the fast transient charge trapping. Figure 4.29 shows  $I_{ds}-V_{gs}$  and corresponding transconductance curves over time evolution. It is shown that slight  $V_T$  shift toward positive direction was observed with minimal transconductance degradation. This is typical for PBTI characteristics since electrons do not generate interface states unlike pMOS device (known as NBTI) [130].

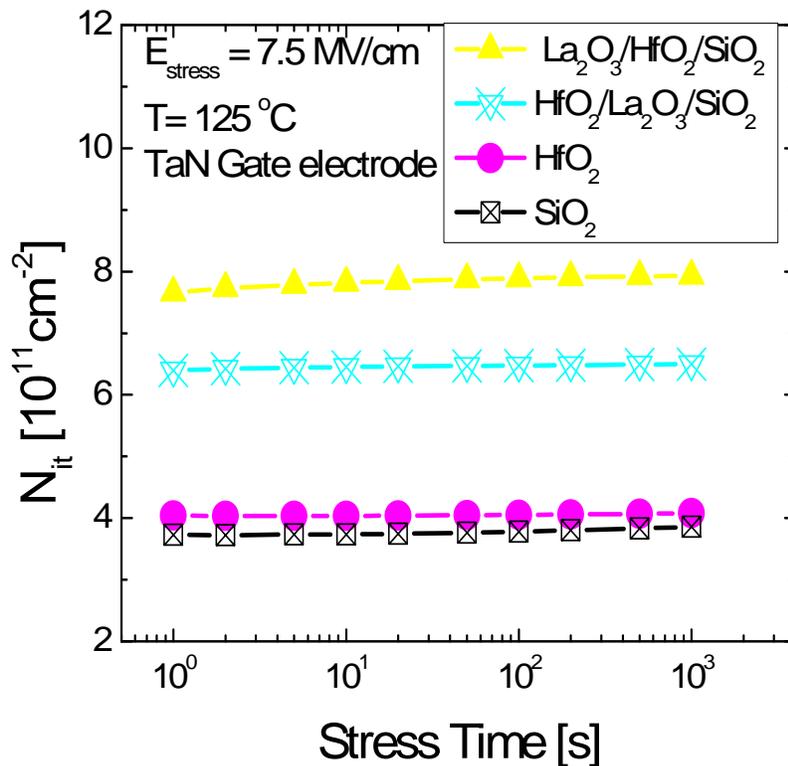


Figure 4.30  $N_{it}$  variations over time measured by charge pumping

Figure 4.30 shows the extracted  $N_{it}$  from charge pumping as a function of stress time. It confirms that the constant stressing at elevated temperature does not create new interface states and thus the  $V_T$  shift from the measurement is originated from either charge trapping of existing traps or creation of new traps near the interfacial  $\text{SiO}_2$  layer.

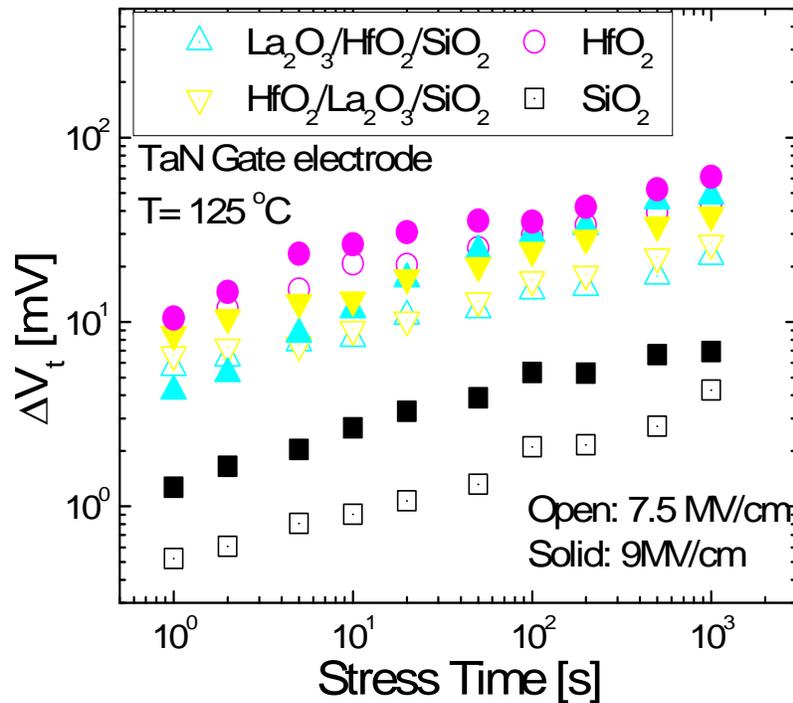


Figure 4.31 Positive Bias Temperature Instability (PBTI) results for two different stress fields at  $125^\circ\text{C}$ . Similar  $V_T$  shift behavior with and without capping indicating the incorporation of  $\text{La}_2\text{O}_3$  layer does not degrade dielectric quality.

Figure 4.31 shows the threshold voltage shift ( $\Delta V_T$ ) over time for two different stress fields to the gate. It is noted that equivalent oxide field ( $E_{ox} = (V_{gs} - V_T)/EOT$ ) was applied to stress the devices since the EOT of the devices is different. It is clearly shown that the  $V_T$  shift with high- $k$  dielectrics is higher than with  $\text{SiO}_2$  due to the inherent bulk traps of the

high- $k$  layer. The incorporation of an ultrathin  $\text{La}_2\text{O}_3$  layer shows slightly less  $V_T$  shift over time than  $\text{HfO}_2$  at  $E_{\text{stress}}=7.5\text{MV}$ . This is attributed to the fact that the incorporation of La can passivate the defect sites in the  $\text{HfO}_2$  after high temperature annealing [130] and/or retard crystallization of  $\text{HfO}_2$  after annealing. At  $E_{\text{stress}}=9\text{MV/cm}$  the slope of  $\text{TaN}/\text{HfO}_2/\text{La}_2\text{O}_3$  stack is higher than  $\text{TaN}/\text{La}_2\text{O}_3/\text{HfO}_2$  stack but still comparable with  $\text{TaN}/\text{HfO}_2$  stack suggesting the incorporation of  $\text{La}_2\text{O}_3$  capping in  $\text{TaN}/\text{HfO}_2$  stack does not degrade device reliability.

## 4.5 Summary

The role of  $\text{La}_2\text{O}_3$  capping in the  $V_T/V_{\text{FB}}$  shift with various high- $k$  and metal gate electrodes was investigated. The presence of La atoms at the high- $k$ /SiO<sub>2</sub> interface forms a dipole layer altering the effective band offset so that the effective work function of the gate is modulated toward nMOS band edge. It was found that the La concentration at the high- $k$ /SiO<sub>2</sub> interface is the key factor for the  $V_T/V_{\text{FB}}$  modulation and the effects of host high- $k$  materials on  $V_T/V_{\text{FB}}$  shift were minimal. The device with  $\text{TaN}/\text{HfO}_2/\text{La}_2\text{O}_3$  gate stack provided 0.4V shift in  $V_T$  from the control  $\text{HfO}_2$  and minimal degradation in mobility whereas the device with  $\text{TaN}/\text{La}_2\text{O}_3/\text{HfO}_2$  gate stack has severe mobility degradation caused by high interface state density. For device reliability, the incorporation of  $\text{La}_2\text{O}_3$  can enhance both breakdown and PBTI characteristics since the La-induced dipole layer can effectively increase barrier height for electron injection as well as passivate bulk charges in the  $\text{HfO}_2$  layer.

## Chapter 5

# Impact of AlTaO capping layer on device performance and reliability for PMOS application

### 5.1 Introduction

Recent studies have shown that many high work function elemental metal gates have an effective flatband voltage ( $V_{FB}$ ) shift ( $V_{FB}$  roll-off) after annealing when deposited on  $HfO_2$  dielectrics, due to the generation of oxygen vacancy in  $HfO_2$  [131-134]. Furthermore, this PMOS gate stack can cause challenges in device scaling due to unwanted EOT gain caused by interfacial layer ( $SiO_2$ ) re-growth [133-134]. In order to overcome the stated problems, a stable metal nitride gate electrode (TaN or TiN) with Al (metal or oxide) incorporation approach for  $V_{FB}$  tuning has been extensively studied as a potential candidate [108, 135-138]. Although nitride metal gates on  $HfO_2$  dielectric have shown promising results such as device scalability, thermal stability, and process compatibility, they have not yet provided PMOS band-edge gate work function for controlling the device threshold voltage ( $V_T$ ) precisely. Therefore the Al based layer should be implemented in order to control  $V_T$  of the PMOS device when midgap nitride metal gates are used. However, even though devices with Al-based capping show some level of  $V_T$  tuning towards PMOS compatible values, it is reported that the mobility of the device is degraded due to the

presence of Al near the channel [135-136]. As an alternate route, it has reported that the work function of  $\text{Al}_x\text{Ta}_{1-x}\text{N}$  metal gate provides PMOS compatible effective work function values on  $\text{SiO}_2$  but decreases with  $\text{HfO}_2$  dielectric due to the reduction of Al–O bonding [138]. In this chapter, we propose and explain an alternate capping layer approach that provides a similar PMOS  $V_T$  tuning effect but which does not degrade mobility or reliability.

## 5.2 Experiments

The conventional gate first p–channel transistors were fabricated on 4” n–type (100) Si substrate. After standard RCA clean, atomic layer deposition (ALD) was used to deposit  $\text{HfO}_2$  high– $k$  layer using TDMAH and  $\text{H}_2\text{O}$  precursors followed by in-situ thin  $\text{Al}_2\text{O}_3$  capping layer using TMA and  $\text{H}_2\text{O}$  precursors. Control  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  were also included to further elucidate the role of capping on the  $V_T$  shift. Another set of  $\text{Al}_2\text{O}_3$  and  $\text{Al}_2\text{O}_3/\text{HfO}_2$  high– $k$  dielectrics deposited on p–type substrate by Applied Materials were also used to fabricate capacitors to examine the effect of temperature on  $V_{\text{FB}}$  modulation. The AlTaO capping layer was formed by 1) the reaction between Ta from gate electrode and  $\text{Al}_2\text{O}_3$  dielectric during the high temperature annealing and 2) depositing an ultrathin TaO layer via UHV–MBE on top of host dielectrics ( $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$ , and  $\text{Al}_2\text{O}_3/\text{HfO}_2$ ) followed by a high–temperature anneal. All samples received an ex–situ PVD TaN or W deposition as a gate electrodes followed by in–situ W capping layer to prevent oxidation of TaN layer as well as to ensure good electrical contact. After gate patterning, source and drain junctions were formed by ion implantation followed by activation anneal at  $950^\circ\text{C}$  for 10s in rapid thermal

anneal (RTA). Several high temperature annealing with capacitors were also carried on to investigate temperature effects on  $V_{FB}$ . After Ti/Al metallization, a forming gas anneal (FGA) was performed at 500°C for 30 min in 10% H<sub>2</sub> in N<sub>2</sub> to passivate interface states. Figure 1 summarizes the fabrication process flow and schematics of dielectric stack used in this study. The samples were characterized in terms of C–V (HP4284 LCR) and I–V (HP4155B).

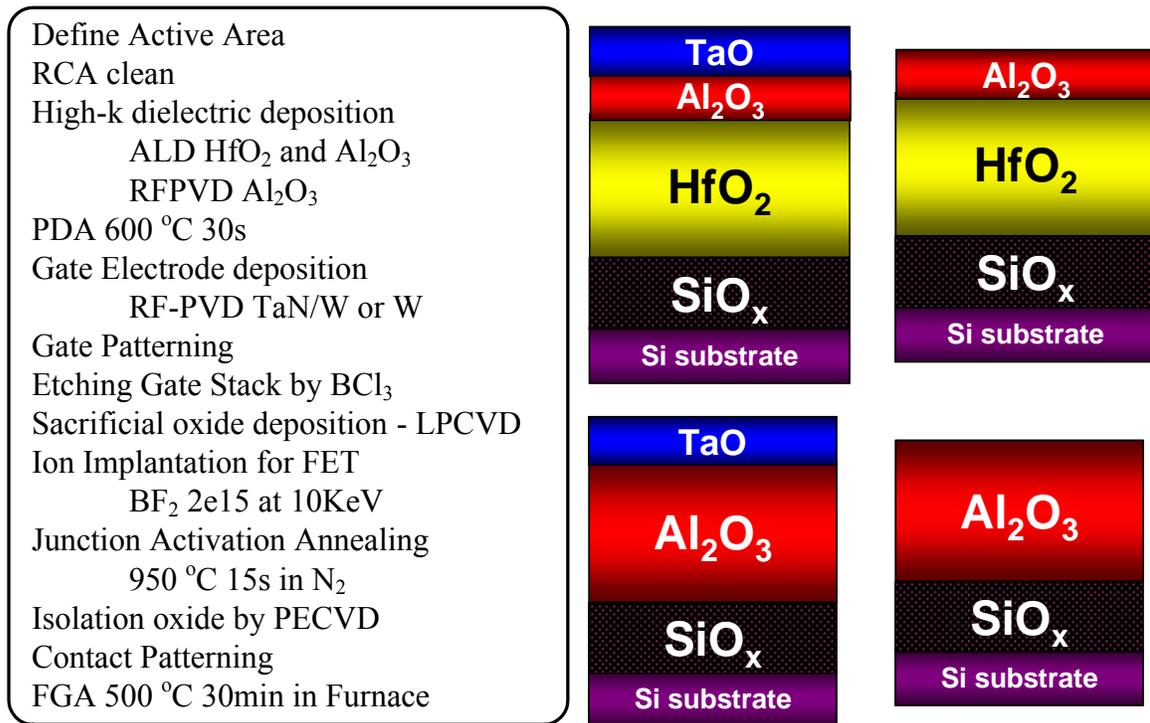


Figure 5.1 Process flows for gate first self-align pMOSFET process and schematics of dielectric stack used in this study

The key parameters such as equivalent oxide thickness (EOT) and flatband voltage ( $V_{FB}$ ) were extracted using NCSU's CVC program [99], and split C–V technique was used to calculate effective mobility. Negative Bias Temperature Instability (NBTI) at elevated temperature (125°C) and charge pumping (CP) measurements were also performed to

evaluate device reliability and charge trapping characteristics. Backside Secondary Ion Mass Spectrometry (SIMS) and Angle-Resolved X-Ray Photoelectron Spectroscopy (AR-XPS) were used to for the physical analysis.

## 5.3 Results and discussion

### 5.3.1 C–V Result of capping layer with W gate electrode

As discussed in chapter 2, the flatband voltage ( $V_{FB}$ ) depends not only on the gate work function but also on charges within the dielectric. Thus, if these parameters can be modulated by the new materials or engineering dielectrics then it is possible to achieve the desired  $V_{FB}$ . Figure 5.2 shows C–V curves for 10Å TaO / 20Å Al<sub>2</sub>O<sub>3</sub> and 20Å Al<sub>2</sub>O<sub>3</sub> high- $k$  dielectrics with W gate electrode after 400°C and 900°C RTA anneal. It is noted that the  $V_{FB}$  with both the TaO/Al<sub>2</sub>O<sub>3</sub>/SiO<sub>x</sub> sample and the Al<sub>2</sub>O<sub>3</sub>/SiO<sub>x</sub> dielectric sample are shifted to positive value after 900°C anneal as compared to 400°C anneal. It is known that the Al–O and Si–O reaction create dipole layers after high temperature annealing resulting in  $V_{FB}$  shift toward positive direction [136-137]. When TaO layer is incorporated between the gate and the Al<sub>2</sub>O<sub>3</sub> dielectric, it is observed that the  $V_{FB}$  is increased towards more positive values as compared to the control Al<sub>2</sub>O<sub>3</sub> dielectric after low temperature annealing (open symbol in Fig. 5.2) but more or less similar after high temperature annealing. It is also interesting to note that the EOT of samples with TaO capping layers was lower than the control Al<sub>2</sub>O<sub>3</sub> dielectric. This can be attributed to 1) the formation of higher  $k$  TaAlO<sub>x</sub> dielectric from the reaction

between TaO and Al<sub>2</sub>O<sub>3</sub>, and 2) that the presence of a TaO layer may scavenge the bottom interface layer as seen in C–V [100]. In order to further investigate the origin of V<sub>FB</sub> modulation, an alternative bi-layer Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack is examined that minimizes the effect of AlO–SiO dipoles on V<sub>FB</sub> at the bottom interface. Figure 5.3 shows the C–V curve illustrating the effect of TaO capping on 10Å Al<sub>2</sub>O<sub>3</sub> / 20Å HfO<sub>2</sub> dielectric with W gate electrode after low and high T treatment. It is shown that the V<sub>FB</sub> with TaO capping sample is clearly more positive than the control Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> sample for both low and high temperature annealing. The amount of extracted V<sub>FB</sub> shift by the incorporation of TaO capping is similar for both dielectrics (about 50~60mV).

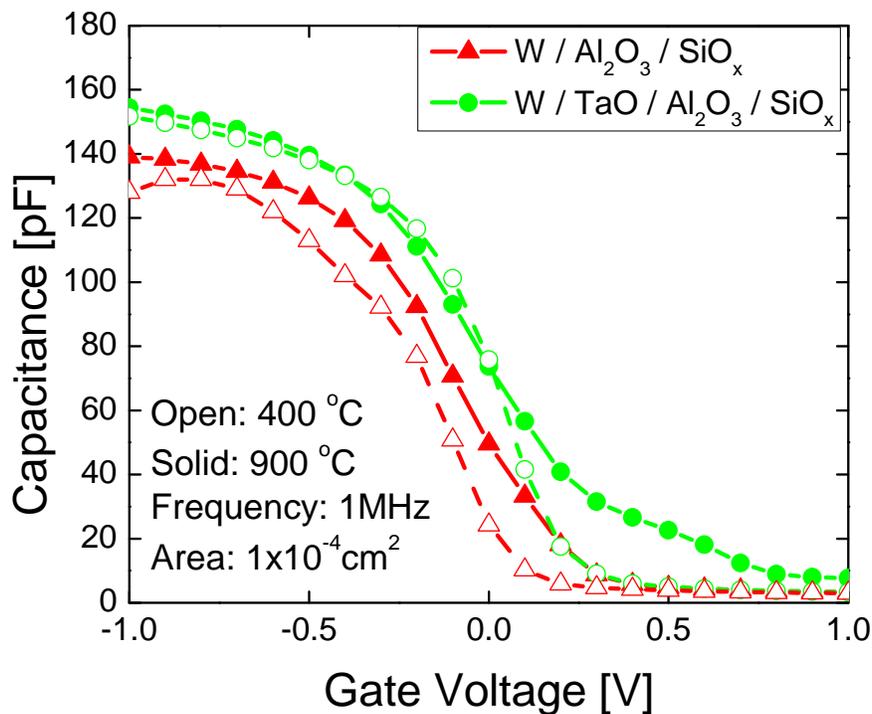


Figure 5.2 C–V characteristic of W/Al<sub>2</sub>O<sub>3</sub>/SiO<sub>x</sub>/Si capacitors with and without TaO capping layer after low and high temperature annealing. The incorporation of TaO capping can modulate device V<sub>FB</sub> toward positive direction.

This result supports that the origin of  $V_{FB}$  shift is attributed to the reaction associated with the TaO–AlO bonding effect [137-138] rather than interaction with bottom interface layer since both  $Al_2O_3$  and  $Al_2O_3/HfO_2$  dielectrics provide similar  $V_{FB}$  shift.

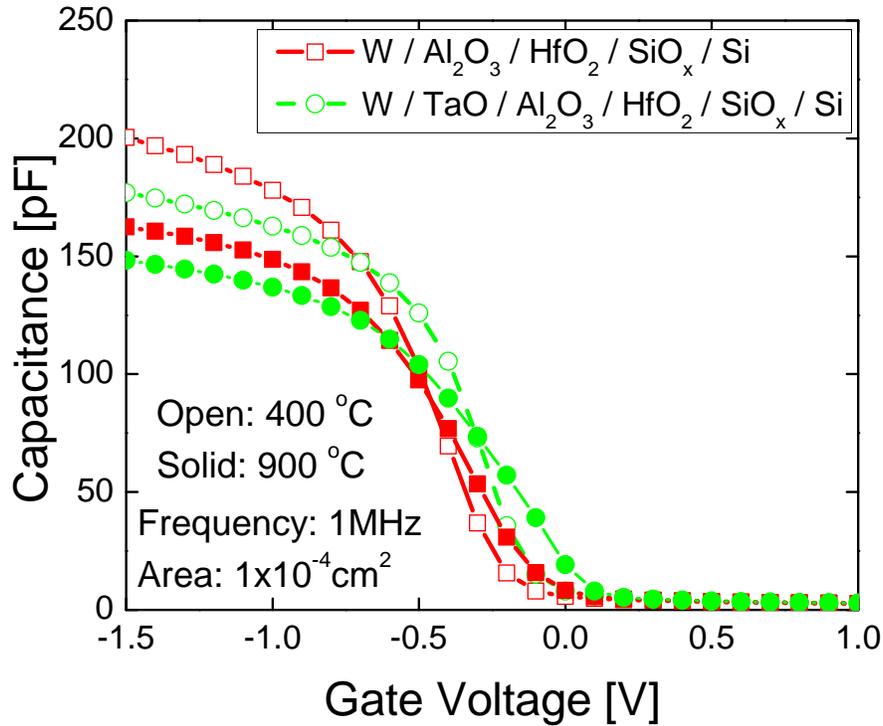


Figure 5.3 C–V characteristic of W/ $Al_2O_3$ / $HfO_2$ / $SiO_x$ /Si capacitors with and without TaO capping layer. The incorporation of TaO capping can also modulate device  $V_{FB}$  with  $Al_2O_3/HfO_2$  dielectric.

### 5.3.2 Material Analysis

To gain further insight into the cause of  $V_{FB}$  shift with AlTaO capping layer on  $HfO_2$  dielectric, systematic material analyses were performed. Angle-Resolve XPS (AR-XPS)

analysis was used to determine 1) chemical bonding states of Hf, Al, and Ta atoms, and 2) diffusion profile of each element at a given temperature. It is noted that all spectra were corrected using charge neutralizer as well as reference peaks. Figure 5.4 shows XPS spectra for Si 2s and O 1s with TaO/Al<sub>2</sub>O<sub>3</sub> stack after low (400°C) and high (900°C) temperature annealing. Two peaks were observed for Si 2p spectra where one peak is for the substrate at 150.7 eV and the other peak is for Si-O bonds. Unlike La<sub>2</sub>O<sub>3</sub> capping shown in chapter 4, these two peak positions did not change even after a high T anneal suggesting that SiO<sub>2</sub> interface is not involved in the reaction over the given temperature range. Corresponding O 1s spectra also support that there is less intermixing in the dielectric with the addition of TaO and no silicate like formation.

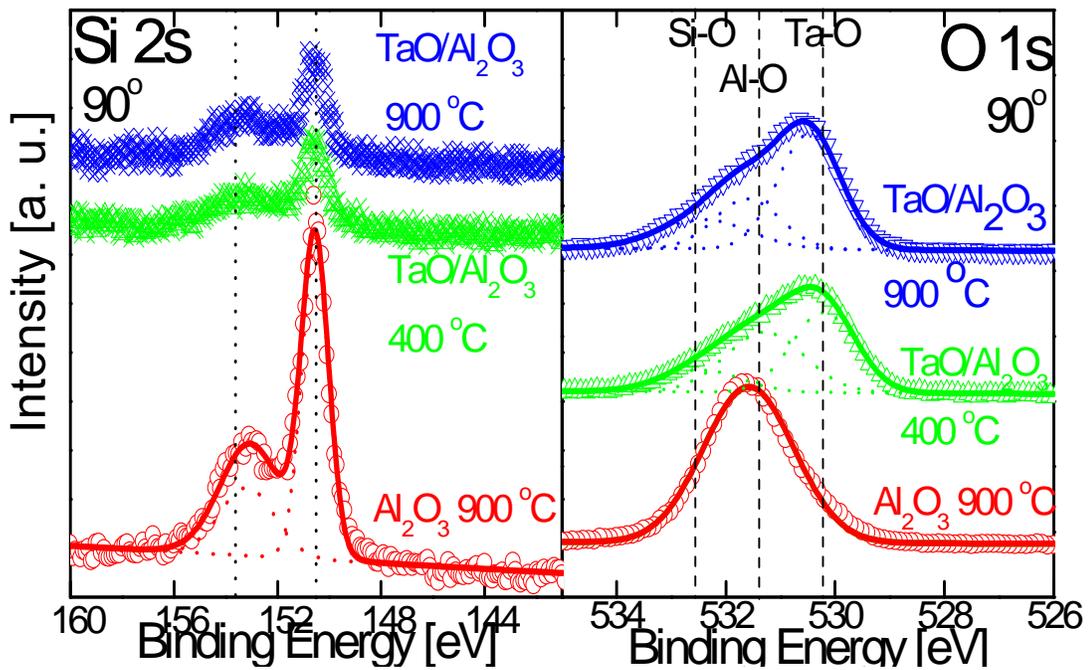


Figure 5.4 XPS for Si 2s, O 1s spectra for Al<sub>2</sub>O<sub>3</sub> after 900°C, TaO/Al<sub>2</sub>O<sub>3</sub> after 400°C, and TaO/Al<sub>2</sub>O<sub>3</sub> after 900°C annealing.

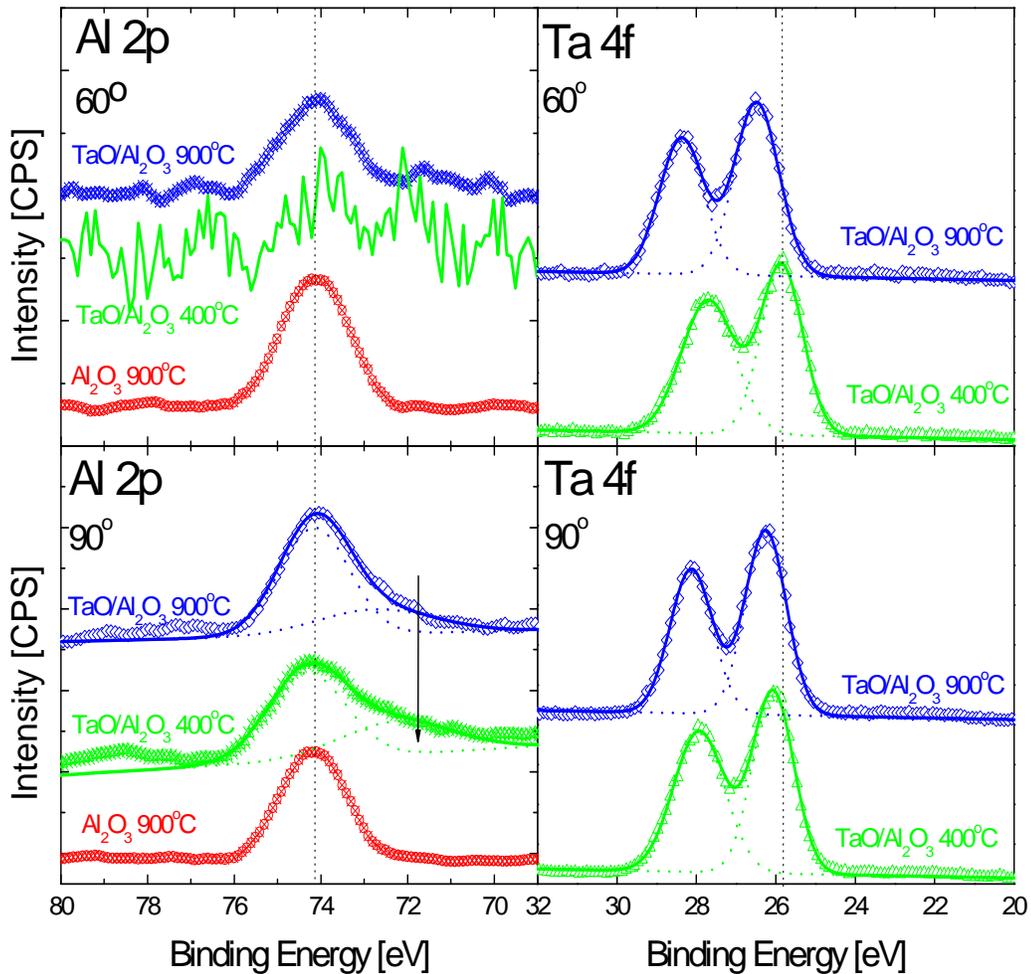


Figure 5.5 XPS for Ta 4f and Al 2p on Al<sub>2</sub>O<sub>3</sub> and TaO/Al<sub>2</sub>O<sub>3</sub> dielectric with two different take off angles (60° and 90°). Minimal structural change is observed at a given temperature range.

Figure 5.5 shows the Ta 4f and Al 2p spectra with 60° and 90° take off angles. Al 2p peak position does not change as temperature increases, whereas slight peak shifts are observed after 900°C for Ta 4f spectra indicating intermixing between TaO and Al<sub>2</sub>O<sub>3</sub> dielectrics is localized at or near the TaO/Al<sub>2</sub>O<sub>3</sub> interface. It is also noted that the Al 2p intensity after 400°C anneal is decreased as compared to the 900°C annealed sample

indicating less intermixing or inter-diffusion of TaO and Al<sub>2</sub>O<sub>3</sub> layers. The Ta 4f peak shifts slightly toward higher binding energy (B.E) where as the Al 2p peak does not move, also suggesting Al-rich AlTaO layer formation [139]. It is also noted that metallic Al like bonding is found as a result of TaO incorporation and this is attributed to the fact that presence of Ta atoms can scavenge oxygen from the Al<sub>2</sub>O<sub>3</sub> layer. It is expected that TaO layer on Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> dielectric shows similar behavior from the electrical data, if the reaction is constrained to the top of the dielectric.

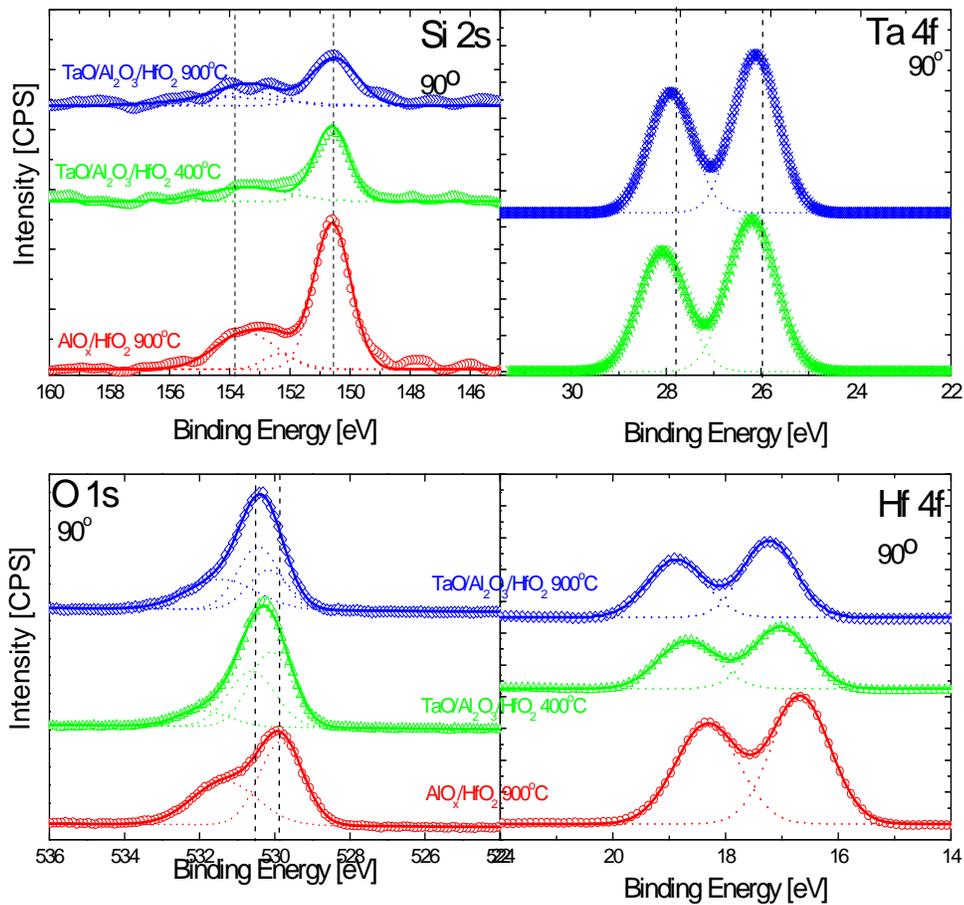


Figure 5.6 AR-XPS spectra for Si 2p, O1s, Ta 4p, and Hf 4f with 90° take-off angle. Small degree of intermixing between dielectrics was observed after 900°C.

As shown in Fig. 5.6 XPS results suggest that the addition of Ta did not change the  $\text{HfO}_2/\text{SiO}_x$  interface property or the bulk properties. Ta 4f and Hf 4f spectra also support that the TaO layer does not fully intermix with the underlying dielectrics. The Hf peaks shift towards higher B.E. after high T annealing indicating either Hf–Al–O reactions or Hf–Al–Ta–O reactions are preferred over Hf–Si–O formation. Si 2s and O1s spectra also do not show any evidence of Si diffusion or silicate formation [140]. Therefore, it is concluded that the  $\text{HfO}_2/\text{SiO}_2$  interface is preserved and the reaction happens only at the top of the dielectric and involves TaO,  $\text{Al}_2\text{O}_3$ , and/or  $\text{HfO}_2$  layers. Since we have a TaO/Ta–Al–O/ $\text{Al}_2\text{O}_3$  stack based on XPS study, a small shift in  $V_{\text{FB}}$  can be attributed to the 1) less degree of intermixing between TaO and  $\text{Al}_2\text{O}_3$  at a given annealing condition or 2) rich TaO in Ta–O–Al formation.

The backside SIMS analysis of TaN/10Å  $\text{Al}_2\text{O}_3$ / 30Å  $\text{HfO}_2/\text{SiO}_2/\text{Si}$  stack after 950°C 10s RTA annealing confirms most of the Al stays on top of the  $\text{HfO}_2$  layer since Hf signal proceeds Al and Ta signals as shown in Fig. 5.7. It also noted that there is slight concentration gradient at low portions of Al concentration indicating some degree of the Al diffused into  $\text{HfO}_2$  layer but not into the  $\text{HfO}_2/\text{SiO}_2$  interface or the Si channel. Therefore, the main mechanism responsible for the  $V_{\text{FB}}$  shift at a given thermal budget is attributed to the reaction of  $\text{Al}_2\text{O}_3$  layer with TaO at the gate/high- $k$  interface where creates localized d-states (charges) of Ta in  $\text{Al}_2\text{O}_3$  dielectric [141].

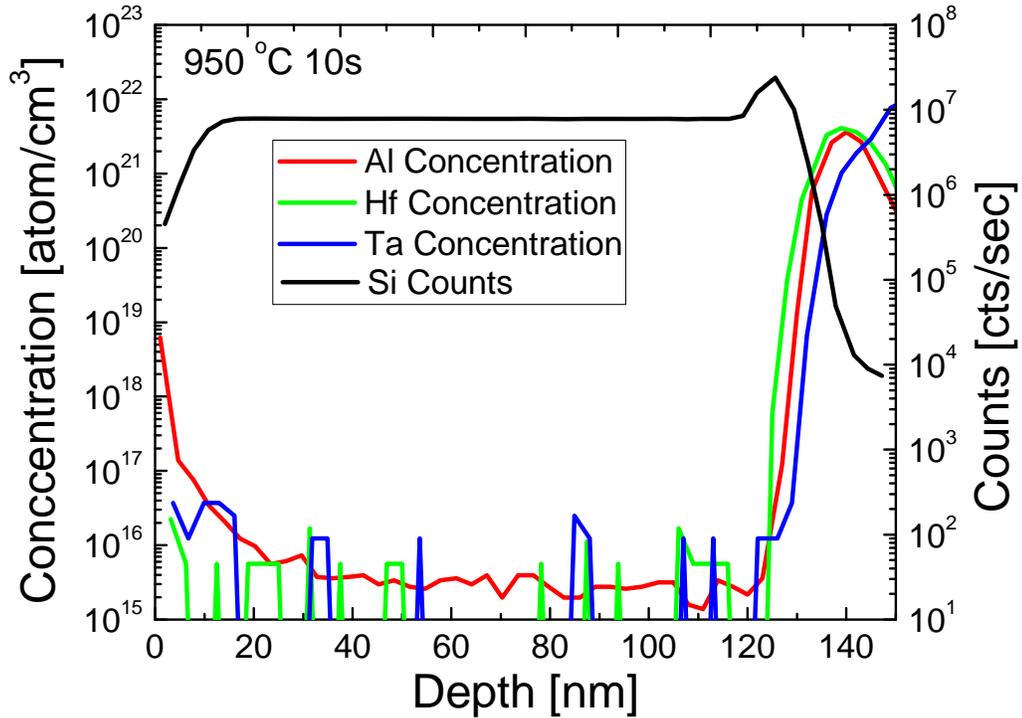


Figure 5.7 Backside SIMS depth profiles for TaN/Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>/SiO<sub>2</sub>/Si stack after 950°C 10s annealing. Most of Al stays on top of the HfO<sub>2</sub> dielectric.

### 5.3.3 Dielectric-gate reaction (TaN gate electrode)

In the previous section, it is shown that Al–Ta–O formation on top of the dielectric is the responsible mechanism for  $V_{FB}$  modulation of the devices. However, double capping approach is not attractive in CMOS integration schemes due to the additional processing step. Thus, it is desired to develop a gate stack having similar electrical characteristic with integration friendly approach. As stated earlier it is reported that TaAlN gate on HfO<sub>2</sub> provides PMOS like  $V_{FB}$  after 1000°C annealing [138]. In this section we evaluate  $V_{FB}$  shift behavior caused by Ta–Al–O formation which is formed by the reaction between Ta–

containing gate and  $\text{Al}_2\text{O}_3$  dielectric. The C–V characteristics of  $\text{Al}_2\text{O}_3/\text{HfO}_2$  with TaN gate electrode after  $900^\circ\text{C}$  annealing are shown in Fig. 5.8. The C–V curves with W gate electrode on both  $\text{Al}_2\text{O}_3/\text{HfO}_2$  and  $\text{TaO}/\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric are also shown as a comparison. It is clearly shown that the  $V_{\text{FB}}$  of the TaN/ $\text{Al}_2\text{O}_3/\text{HfO}_2$  capacitor is shifted toward positive direction from the W/ $\text{Al}_2\text{O}_3/\text{HfO}_2$  sample and to similar value to the W/ $\text{TaO}/\text{Al}_2\text{O}_3/\text{HfO}_2$  sample, confirming that the  $V_{\text{FB}}$  shift is caused by the Ta–Al–O formation. Since thermally stable TaN gate electrode was used, the temperature effect on  $V_{\text{FB}}$  with dielectrics can be studied.

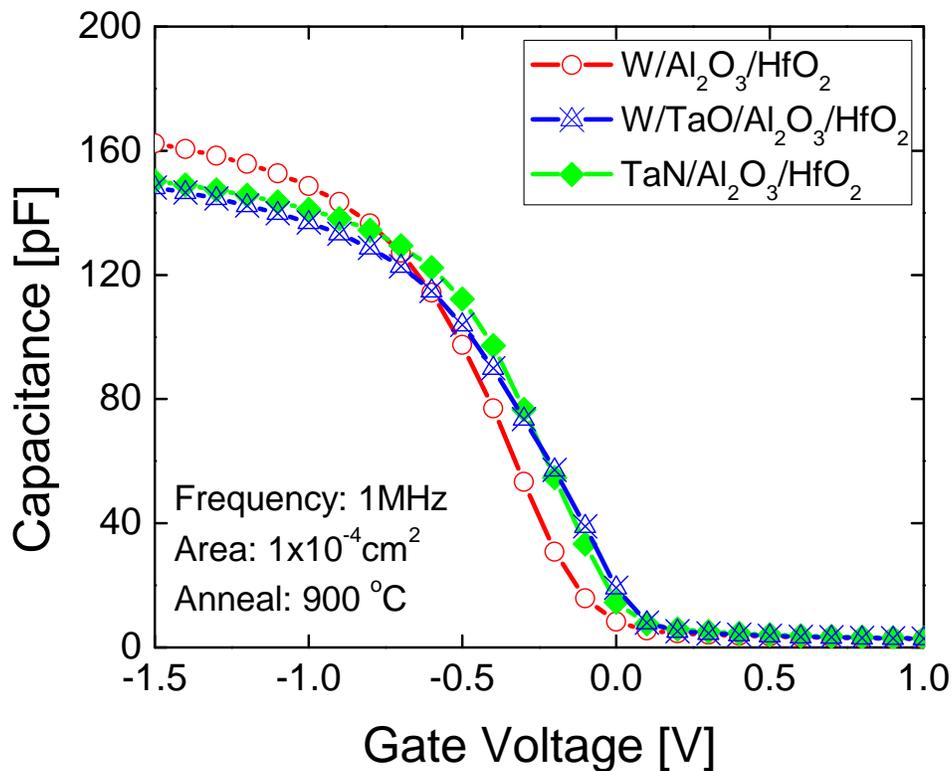


Figure 5.8 C–V plots for TaN/ $\text{Al}_2\text{O}_3/\text{SiO}_x/\text{Si}$  capacitor, W/ $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{SiO}_x/\text{Si}$  capacitor, and W/ $\text{TaO}/\text{Al}_2\text{O}_3/\text{HfO}_2/\text{SiO}_x/\text{Si}$  capacitor after  $900^\circ\text{C}$  anneal. The presence of Ta enhances  $V_{\text{FB}}$  due to the Ta (gate) and  $\text{Al}_2\text{O}_3$  (dielectric) reaction at the top of the interface.

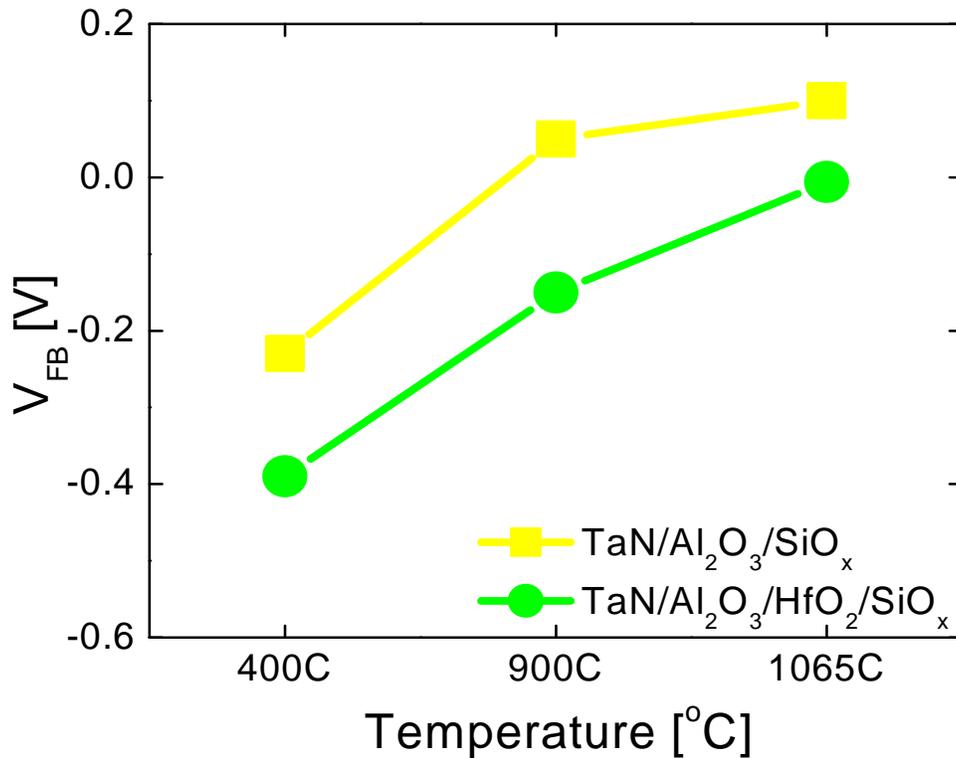


Figure 5.9  $V_{FB}$  vs. temperature for  $Al_2O_3$  and  $Al_2O_3/HfO_2$  dielectrics with TaN gate electrode.  $V_{FB}$  is modulated towards positive direction as temperature indicating more reaction between TaO– $Al_2O_3$  and/or presence of Al at the bottom interface.

The magnitude of  $V_{FB}$  is increased with temperatures as shown in Fig. 5.9 indicating further reaction or diffusion of Al to the bottom interface. It should be noted that an additional 200mV shift for control  $Al_2O_3$  samples over  $Al_2O_3/HfO_2$  stacks is obtained due to the large/strong Al–O bonding available at the bottom interface which causes  $SiO_2$ – $Al_2O_3$  dipole formation as mentioned before. Figure 5.10 summarizes the extracted  $V_{FB}$  for the different dielectrics with W and TaN gate electrodes.

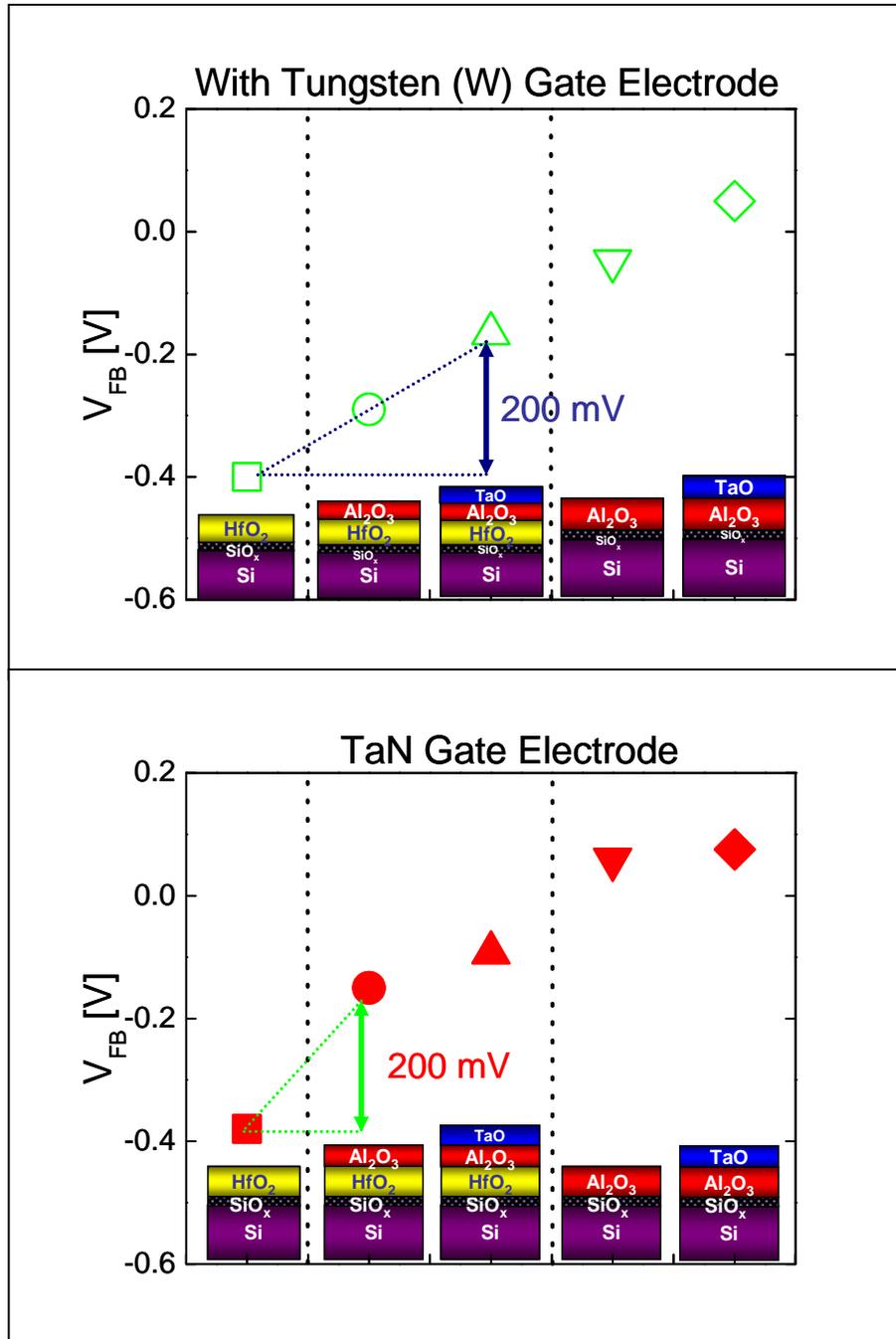


Figure 5.10 Summary of  $V_{FB}$  for various dielectrics (a) with W gate electrode after 900°C and (b) with TaN gate electrode after 900°C. 200mV shift was obtained with TaO layer between Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> dielectric and W gate electrode. However, same 200mV shift in  $V_{FB}$  was obtained with TaN/Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack confirming Ta and Al<sub>2</sub>O<sub>3</sub> reaction is the main responsible mechanism for additional  $V_{FB}$  shift.

The extracted  $V_{FB}$  on single  $HfO_2$  dielectric is about -0.4V with W and TaN gate electrodes indicating the effective work function of W and TaN on  $HfO_2$  is similar. It is observed that 200mV of  $V_{FB}$  is shifted from the control ( $HfO_2$ ) when double capping TaO/ $Al_2O_3$  layer is incorporated between W gate electrode and  $HfO_2$  dielectric after 900°C annealing. However same amount (200 mV) of  $V_{FB}$  shift is obtained with single  $Al_2O_3$  capping incorporation on  $HfO_2$  dielectric with TaN gate electrode. A similar result is observed on  $Al_2O_3$  dielectric as shown in Fig. 5.10. This result confirms that the TaN gate electrode can also be used for Ta–Al–O formation for an additional  $V_{FB}$  modulation and reduction of process steps. Figure 5.11 illustrates the proposed models for our experimental results explaining the  $V_{FB}$  shift for  $Al_2O_3/HfO_2$  and  $Al_2O_3$  dielectrics.

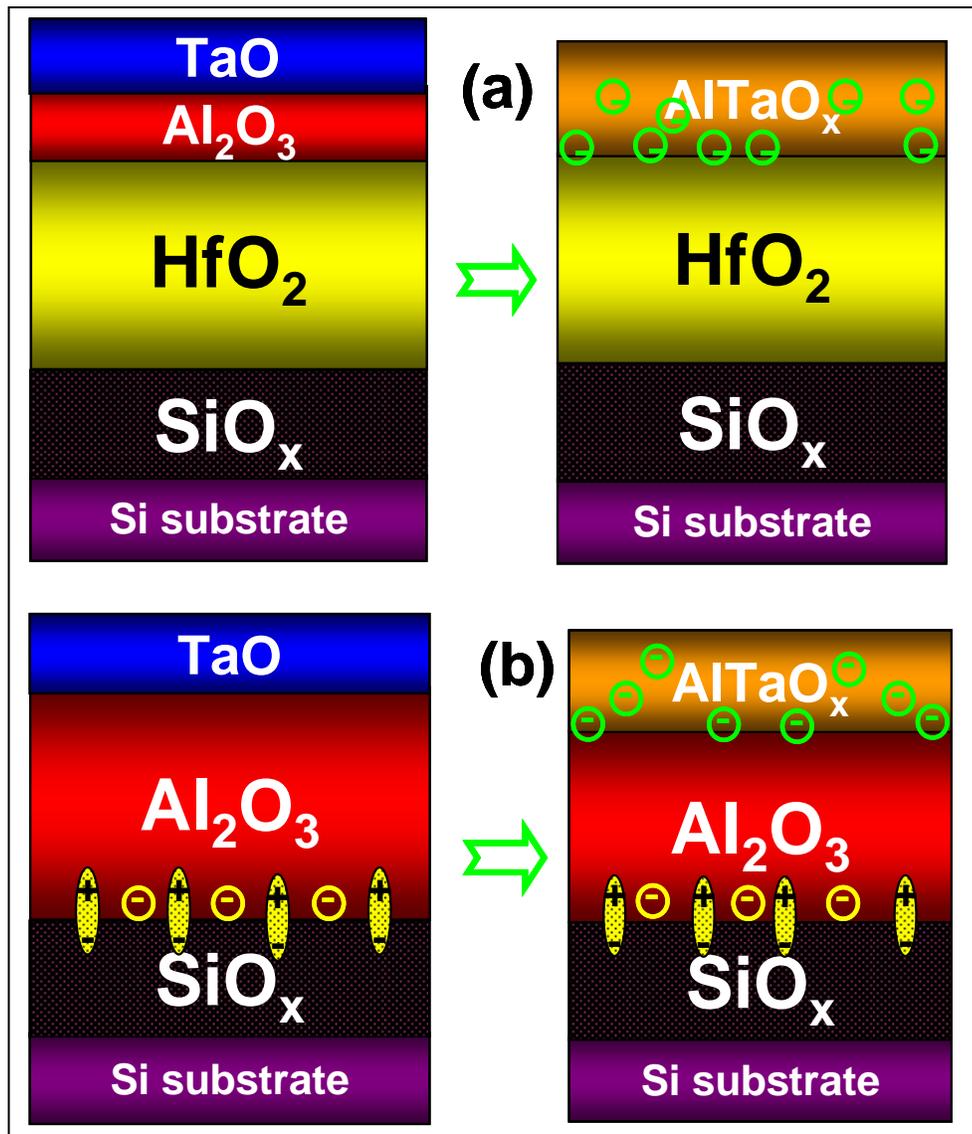


Figure 5.11 Proposed models to explain the  $V_{FB}$  shift mechanism caused by AlTaO capping on a) HfO<sub>2</sub> dielectrics and b) Al<sub>2</sub>O<sub>3</sub> dielectrics. The TaO–Al<sub>2</sub>O<sub>3</sub> reaction creates Ta d states in Al<sub>2</sub>O<sub>3</sub> matrix (electron traps) resulting in enhancement of  $V_{FB}$ . Al<sub>2</sub>O<sub>3</sub> dielectric shows larger  $V_{FB}$  modulation due the Al<sub>2</sub>O<sub>3</sub>/SiO<sub>x</sub> interface dipole effect.

### 5.3.4 Electrical Characterization of Al-based capping MOSFET

It was shown that the TaN gate with Al<sub>2</sub>O<sub>3</sub> capping on HfO<sub>2</sub> dielectric can provide desired PMOS like effective work function based on capacitor result. In this section the electrical performances and reliable characteristics of pMOSFET fabricated using same capping layers on high-*k* dielectric are evaluated.

#### 5.3.4.1 MOSFET C-V and I-V

Figure 5.12 shows high frequency (100 KHz) C-V characteristic of transistors with and without capping on both HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> dielectrics. It is clearly revealed that the addition of dielectric capping layer can modulate  $V_T/V_{FB}$  of the device to the positive direction relative to the control sample (HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> dielectric), similar to the capacitor results. It is also noticed that the degree of the C-V shift is lower with TaO/Al<sub>2</sub>O<sub>3</sub> capping compared to just Al<sub>2</sub>O<sub>3</sub> capping on HfO<sub>2</sub> dielectric whereas shift in  $V_T/V_{FB}$  with a TaO/Al<sub>2</sub>O<sub>3</sub> dielectric is larger than with Al<sub>2</sub>O<sub>3</sub> only dielectric. This difference is attributed to the limited availability of Al to react with Ta for the case with the HfO<sub>2</sub> dielectric, whereas there is a larger availability of Al to react with Ta for the case with only the Al<sub>2</sub>O<sub>3</sub> dielectric (this Al<sub>2</sub>O<sub>3</sub> only layer is physically thicker (40Å) than Al<sub>2</sub>O<sub>3</sub> capping (10Å) on HfO<sub>2</sub>). To support the compositional effect of Ta in Al<sub>2</sub>O<sub>3</sub> separate experiments performed by co-sputtering Al<sub>x</sub>Ta<sub>1-x</sub>O showing that the  $V_{FB}$  shift is maximized only when the Ta concentration is below 60% indicating that Ta rich films do not result in an additional  $V_{FB}$  shift as shown figure 5.13. Therefore it is critical to control the ratio of Al to Ta precisely to maximize  $V_{FB}$  modulation

while minimizing EOT growth. Furthermore, it is clearly seen that the  $\text{Al}_2\text{O}_3$  based dielectrics show larger modulation in  $V_T$  as compared to  $\text{HfO}_2$  based dielectrics, which is explained by the Al-induced dipole layer at the bottom interface as already discussed in previous section. Figure 5.12 also indicates that about 4 Å of EOT is gained for both  $\text{Al}_2\text{O}_3$  capping and  $\text{TaO}/\text{Al}_2\text{O}_3$  capping on  $\text{HfO}_2$  dielectric samples due to the physical thickening of the dielectric stack. The reason why  $\text{TaO}/\text{Al}_2\text{O}_3$  capping shows similar EOT gain even though the stack is physically thicker than  $\text{Al}_2\text{O}_3$  capping can be attributed to 1) the effect of higher  $k$  Ta-oxide incorporation and 2) Ta induced interfacial layer decomposition.

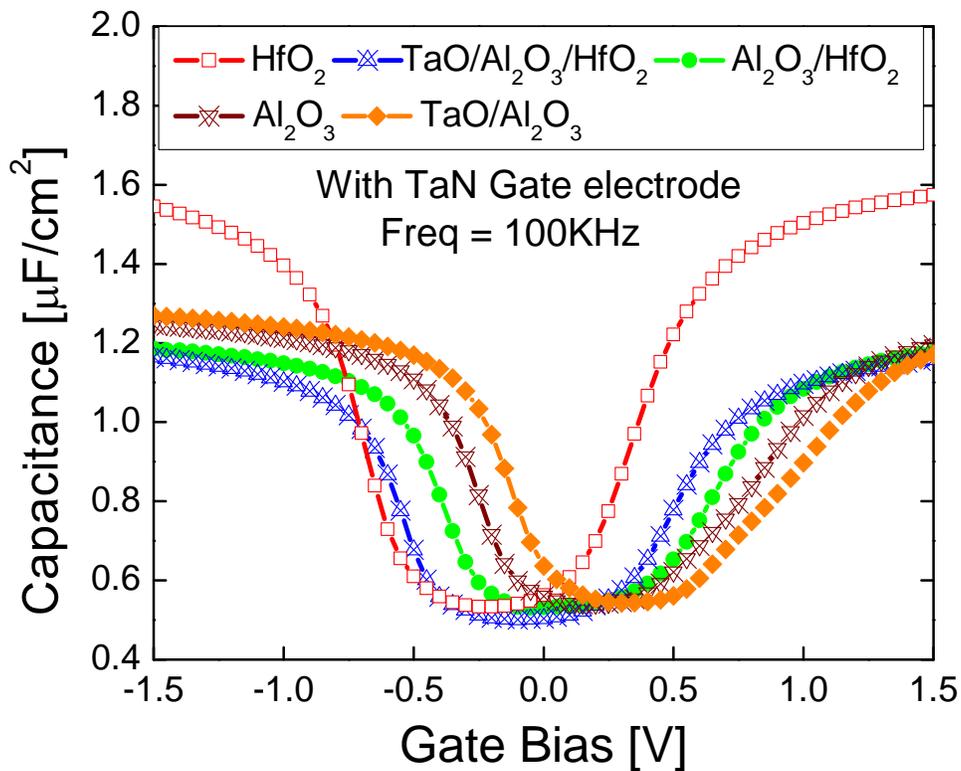


Figure 5.12 C–V curves for pMOSFET with various dielectric stacks. The addition of  $\text{Al}_2\text{O}_3$  or TaO can modulate device threshold voltage.

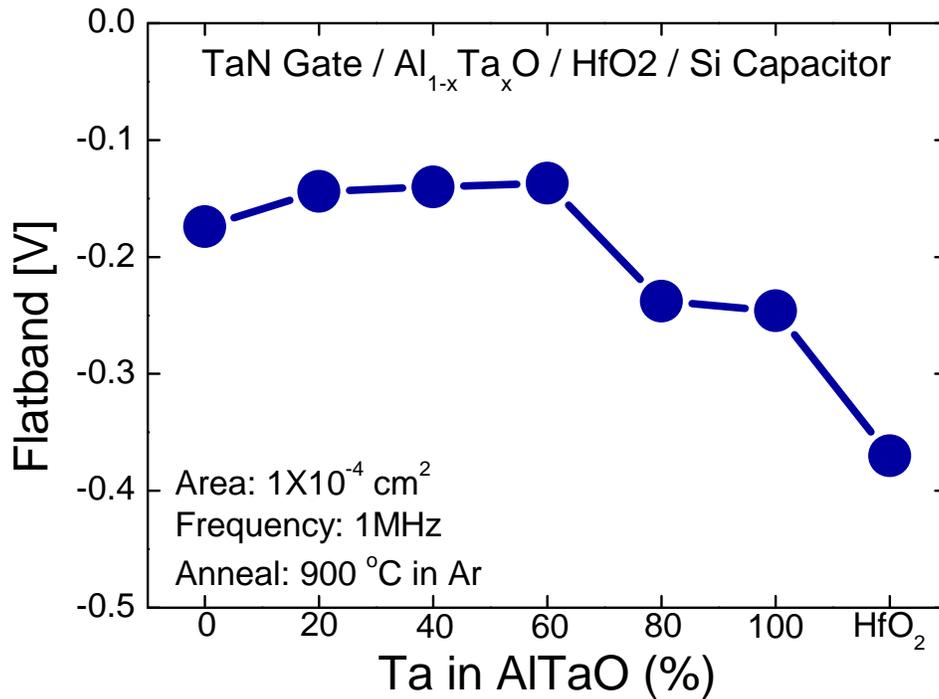


Figure 5.13 Extracted  $V_{FB}$  as a function of Ta composition in  $Al_{1-x}Ta_xO$  layer.  $V_{FB}$  starts to decrease when Ta composition in  $Al_{1-x}Ta_xO$  is more than 60%.

Figure 5.14 shows  $I_{ds}-V_{gs}$  characteristics of the transistor for all sample condition. The impact of the capping layer on  $V_T$  is also seen in device transfer characteristics with improved transconductance. It is worthwhile to note that the TaN/ $Al_2O_3$ /HfO<sub>2</sub> stack shows higher drain current and transconductance than the TaN/HfO<sub>2</sub> stack, despite having thicker EOT. This will be addressed in the mobility analysis section. The extracted  $V_T$  for the HfO<sub>2</sub> control, TaO/ $Al_2O_3$ /HfO<sub>2</sub>, and  $Al_2O_3$ /HfO<sub>2</sub> dielectrics are -0.8V, -0.6V, and -0.4V respectively.

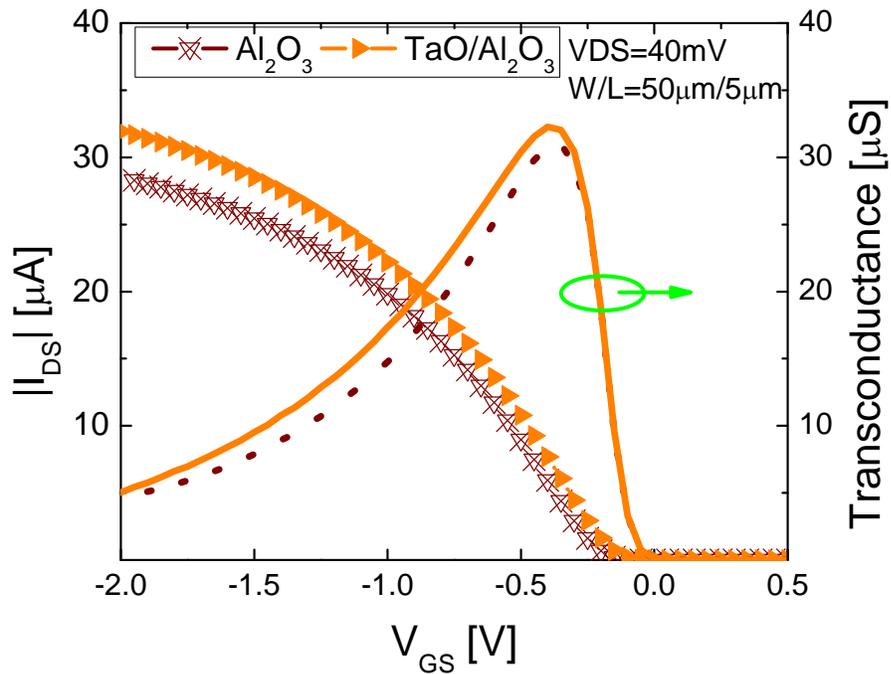
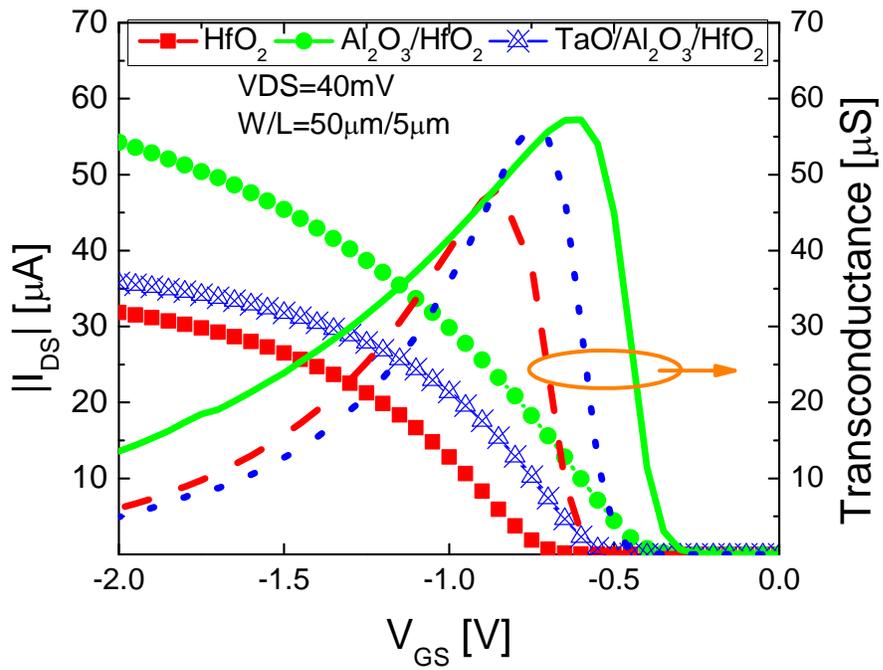


Figure 5.14 Linear  $I_{ds}$ - $V_{gs}$  and corresponding transconductance for (a) HfO<sub>2</sub> based dielectrics and (b) Al<sub>2</sub>O<sub>3</sub> based dielectrics.

Table 5.1 Key parameters extracted from C–V and I–V measurements

Dielectric	EOT (nm)	$V_{FB}$ (V)	$V_T$ (V)	$G_{m, peak}$ (uS)	Subthreshold swing (S) (mV/decade)
<b>HfO<sub>2</sub></b>	1.78	0.464	-0.706	57	75
<b>TaO/Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub></b>	2.40	0.603	-0.554	56	72
<b>Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub></b>	2.35	0.797	-0.418	48	70
<b>Al<sub>2</sub>O<sub>3</sub></b>	2.27	0.992	-0.204	31	85
<b>TaO/Al<sub>2</sub>O<sub>3</sub></b>	2.26	1.099	-0.15	32	82

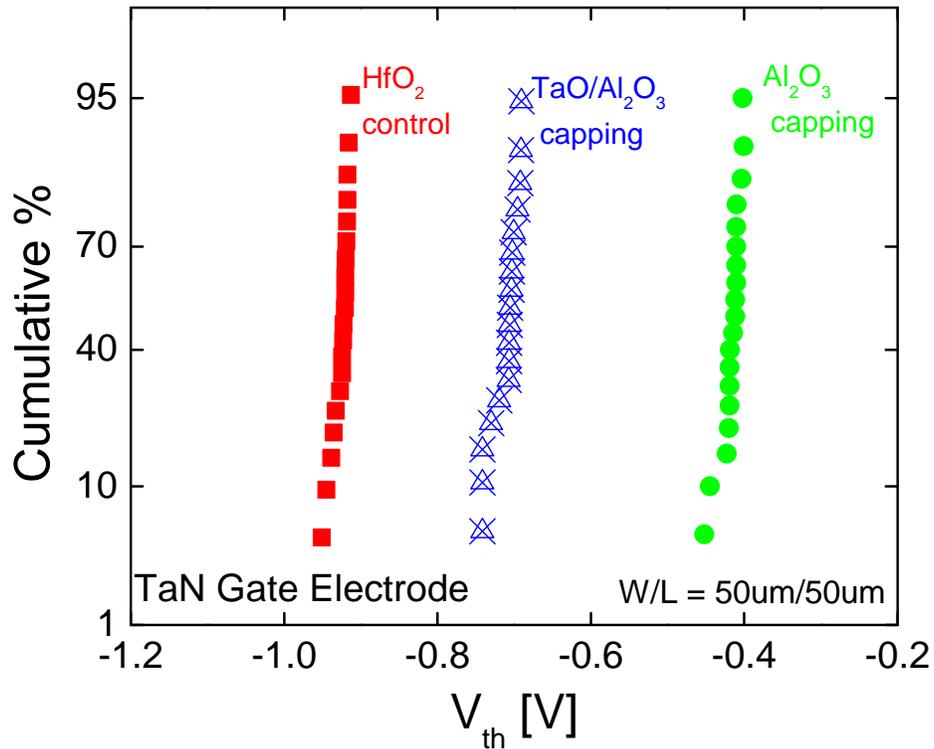


Figure 5.15  $V_T$  distributions with HfO<sub>2</sub>, TaO/Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>, and Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> dielectrics.

It is noted that relative high  $V_T$  values for the device are attributed to the high doping concentration of the n-substrate. Almost 60mV enhancement in the  $V_T$  is observed by the addition of TaO capping from  $\text{Al}_2\text{O}_3$  dielectric.  $I_{ds}-V_{gs}$  characteristics for Al-based dielectrics support that the addition of TaO capping on single  $\text{Al}_2\text{O}_3$  dielectric modulates  $V_T$  further since bottom the  $\text{Al}_2\text{O}_3-\text{SiO}_2$  reaction also contributes to the additional modulation of  $V_T$  as well as the top TaO- $\text{Al}_2\text{O}_3$  reaction. Table 5.1 summarizes the key parameters of the pMOSFET devices for all gate stack samples.

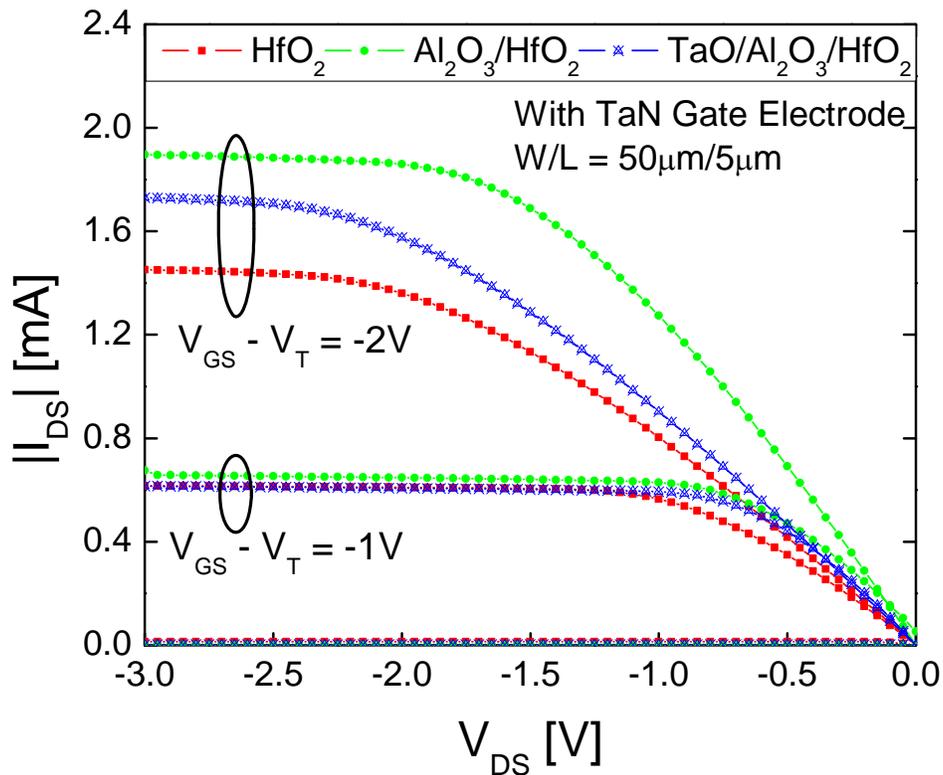


Figure 5.16  $I_{ds}-V_{ds}$  curves for two different overdrive voltage ( $V_{gs}-V_T = -1\text{V}$  and  $-2\text{V}$ ). Higher drive current is obtained with  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric.

Figure 5.15 shows  $V_T$  distributions through the wafer with and without capping on  $\text{HfO}_2$  dielectrics. The device to device variation is similar with and without capping indicating uniform distribution of the  $V_T$ . Figure 5.16 shows  $I_{ds}-V_{ds}$  characteristics with two different overdrive conditions ( $V_{gs}-V_T = -1$  and  $-2$  V). Incorporation of capping layer can enhance drive current characteristic of TaN/ $\text{HfO}_2$  stack even though the control  $\text{HfO}_2$  stack has thinner EOT than the capping samples. Finally gate leakage current characteristics on  $\text{HfO}_2$  based dielectric were evaluated and plotted in Fig. 5.17. The incorporation of  $\text{Al}_2\text{O}_3$  capping can reduce the electron injection probability from the gate due to the additional barrier of  $\text{Al}_2\text{O}_3$  whereas the leakage current from substrate injection is similar with and without  $\text{Al}_2\text{O}_3$  capping due to the presence of  $\text{HfO}_2$  barrier. This confirms that most of  $\text{Al}_2\text{O}_3$  stays on top of the  $\text{HfO}_2$  or inside  $\text{HfO}_2$  as confirmed by backside SIMS analysis.

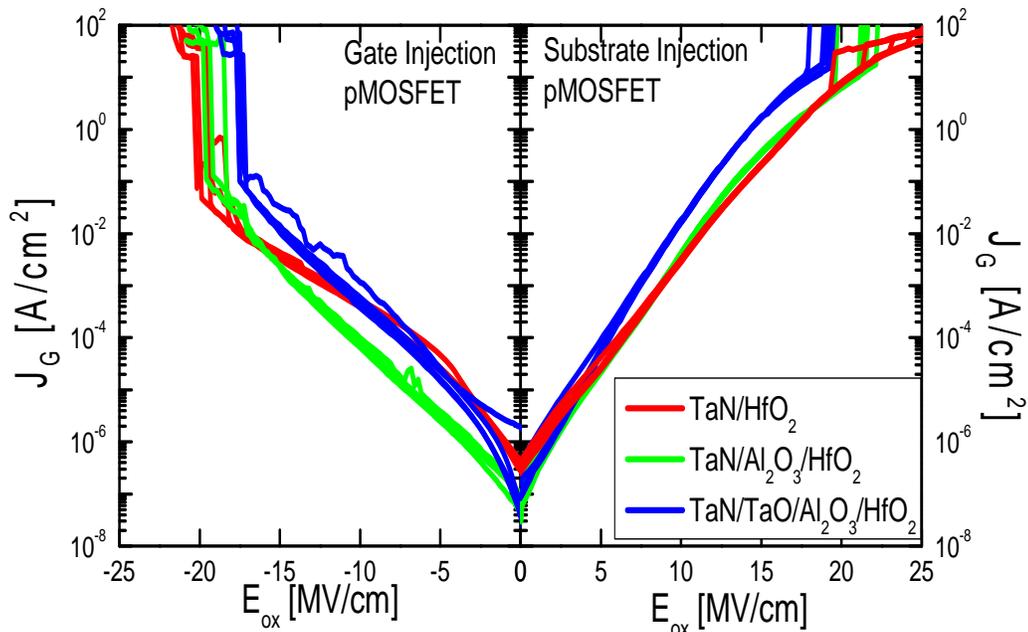


Figure 5.17  $J_G$  characteristics for both gate and substrate injection. Incorporation of capping does not degrade dielectric property.

### 5.3.4.2 Mobility Analysis

Figure 5.18 shows effective hole mobility ( $\mu_{\text{eff}}$ ) of pMOSFET with and without capping on HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> dielectrics extracted by split C–V method with leakage current correction as discussed in chapter 2. It is clearly shown that both Al<sub>2</sub>O<sub>3</sub> and TaO/Al<sub>2</sub>O<sub>3</sub> capping improve peak mobility as well as high field mobility compared to HfO<sub>2</sub> control. Table 5.2 summarizes the peak mobility values as well as high field mobility at  $E_{\text{eff}}=0.9\text{MV/cm}$ . Only 2% of effective mobility at high field is degraded with the Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack from the universal curve whereas 20% of effective mobility is degraded from the universal curve with HfO<sub>2</sub> dielectric. The extracted effective mobility with Al<sub>2</sub>O<sub>3</sub> only dielectric shows much lower values than other samples due to the presence of Al near the channel. However, the addition of TaO layer on Al<sub>2</sub>O<sub>3</sub> dielectric can improve mobility and this can be explained by the reduction of i) interface state density (from charge pumping data in Fig. 5. 19 (b) and/or ii) the reduction of free Al near the Si channel since the presence of Al near the Si channel is known to degrade the effective mobility of the device [136]. Our experimental data demonstrates that the mobility is not degraded by the addition of Al<sub>2</sub>O<sub>3</sub> capping layer due to the retardation of Al diffusion into the bottom interface.

To gain further insight for causing the mobility degradation with HfO<sub>2</sub> dielectric, charge pumping measurement was carried on. The base sweep charge pumping data (Fig. 5.19 (a)) shows the Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> sample has  $1 \times 10^{11}$  (cm<sup>-2</sup>) of  $N_{\text{it}}$  as compared to  $2.6 \times 10^{11}$  (cm<sup>-2</sup>) of control HfO<sub>2</sub> sample. This high  $N_{\text{it}}$  value for HfO<sub>2</sub> dielectric can be one of reasons for mobility degradation since the degradation trend in extracted motilities corresponds well with charge pumping data.

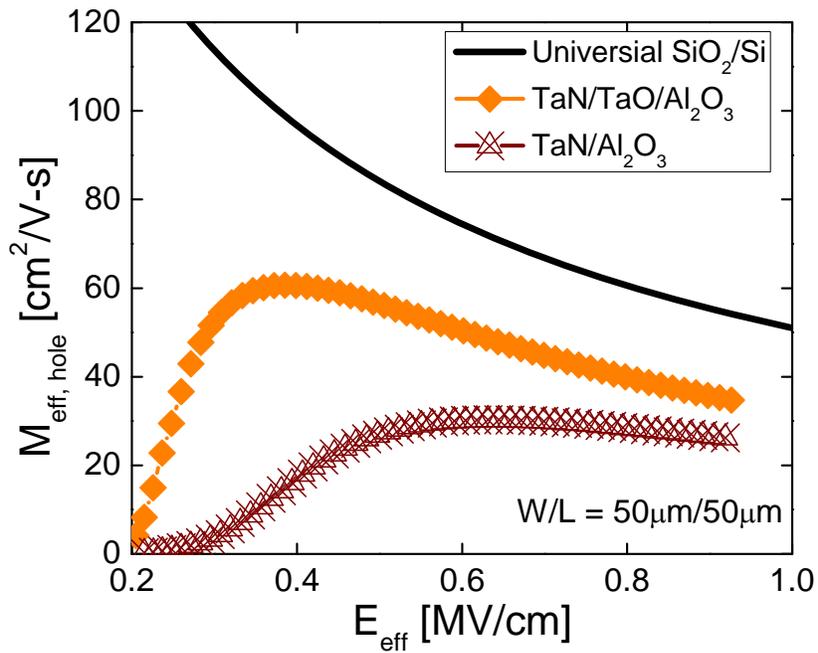
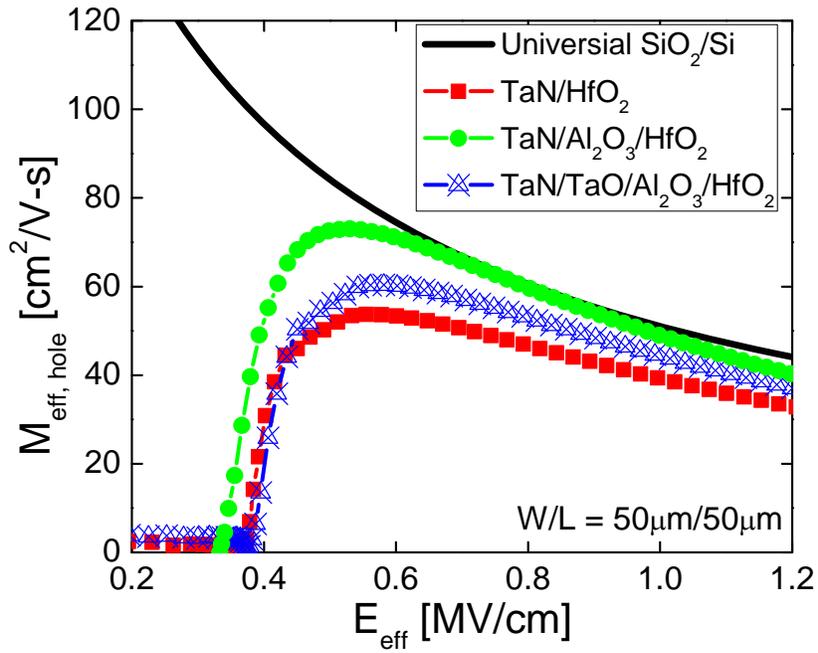


Figure 5.18 Effective mobility curves extracted from split C–V method for (a) HfO<sub>2</sub> based dielectric and (b) Al<sub>2</sub>O<sub>3</sub> based dielectrics.

Table 5.2 Summary of peak mobility and high field ( $E_{\text{eff}}=0.9 \text{ MV/cm}$ ) mobility

<b>Dielectric</b>	$\mu_{\text{eff, peak}}$ ( $\text{cm}^2/\text{V-s}$ )	$\mu_{\text{eff}}$ ( $\text{cm}^2/\text{V-s}$ ) at <b>0.9MV/cm</b>	<b>% of <math>\mu_{\text{eff}}</math> degradation</b>
<b>HfO<sub>2</sub></b>	55	43.5	20
<b>TaO/Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub></b>	60	48.2	12
<b>Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub></b>	76	53.6	2
<b>Al<sub>2</sub>O<sub>3</sub></b>	31	26.5	50
<b>TaO/Al<sub>2</sub>O<sub>3</sub></b>	63	35.7	34

Furthermore, it has reported that the mobility of the HfO<sub>2</sub> dielectric is suffered from not only interface state charges but also oxide charges in crystalline HfO<sub>2</sub> [142-143]. It is reported that the incorporation of elements such as Al, Si and Ta into HfO<sub>2</sub> layer can improve mobility by suppressing crystallization of HfO<sub>2</sub> dielectric as well as bulk trap generation in HfO<sub>2</sub> layer [143-144]. It is also reported that the mobility of TaN (or TiN) gate / HfO<sub>2</sub> dielectric stack can be degraded due to the nitrogen diffusion from the gate electrode after high T annealing [145]. If Al<sub>2</sub>O<sub>3</sub> capping layer is inserted between HfO<sub>2</sub> dielectric and TaN gate electrode, the diffusion of nitrogen from the gate can be minimized and thus the mobility characteristic is improved. Therefore the mobility enhancement caused by Al-based capping layer incorporation is attributed to i) minimized Al diffusion to the bottom interface by the Al-Ta reaction, ii) the reduction of trap generation in HfO<sub>2</sub> dielectric by preventing dielectric crystallization, and iii) minimized nitrogen diffusion from the TaN gate. It is also noticed that TaO/Al<sub>2</sub>O<sub>3</sub> capping shows lower  $\mu_{\text{eff}}$  than Al<sub>2</sub>O<sub>3</sub> capping and this can be explained by i) less

quality of the interfacial oxide formed by the incorporation of a non-stoichiometric TaO layer (from the XPS results) in the dielectric stack which can remotely decompose the interfacial layer as mentioned in chapter 3, and ii) inherent bulk traps from the TaO layer.

In order to investigate the bulk trap response from the high- $k$  dielectrics near the Si channel, amplitude sweep charge pumping technique has been applied and the result is shown in Fig 5.20. When charging time is long enough with sufficient rise/fall times, then some of bulk traps near the interface can contribute to the recombination process and hence increases charge pumping current. Figure 5.20 also includes the current measured at the source/drain ( $N_{S+D}$ ) terminal simultaneously with substrate current ( $N_{CP}$ ) for three different charging times. With  $Al_2O_3$  capping, the  $N_{CP}$  variation with charging time is less than with  $HfO_2$  and this is direct evidence for the suppression of bulk traps by intermixing of  $HfO_2$  and  $Al_2O_3$ . It is also noted that  $N_{S+D}$  indicates larger variation than  $N_{CP}$  for both samples over frequency ranges. It is believed that the increase in  $N_{S+D}$  over  $N_{CP}$  is attributed to the tunneling current from inversion layer to the gate electrode or detrapping of trapped charge to the gate electrode [146]. Since TaN/ $HfO_2$  stack is physically thinner and imperfect dielectric, it is obvious to observe larger deviation in  $N_{S+D}$  or charging time dependence. Figure 5.21 summarizes  $N_{CP}$  variation taken at  $V_{peak} = V_T + 1.5V$  as a function of charging time. It is clearly shown that the incorporation of Al into  $HfO_2$  can reduce some of the bulk charge generation. Furthermore,  $N_{CP}$  of TaO/ $Al_2O_3$  capping shows large dependency in charging time indicating more bulk traps near the interface. These traps and charges can communicate with inversion charges and hence mobility is degraded as shown in mobility curve.

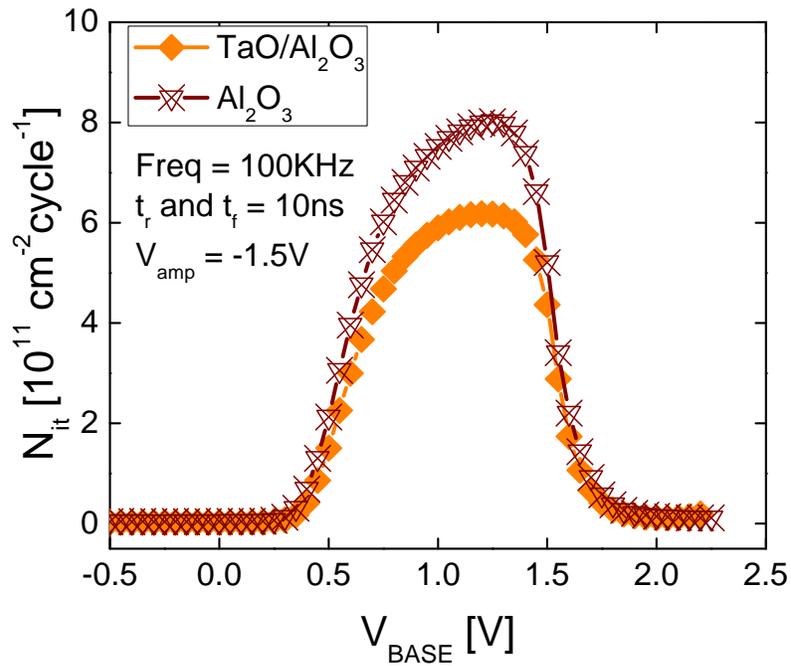
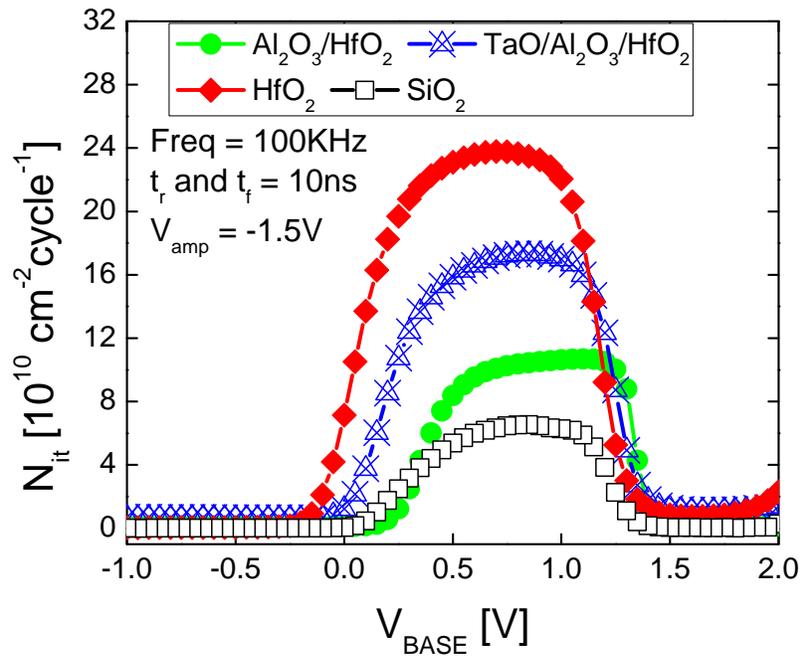


Figure 5.19 Base level sweep charge pumping data for (a)  $\text{HfO}_2$  based dielectric and (b)  $\text{Al}_2\text{O}_3$  based dielectric. Measured  $N_{it}$  corresponds to the mobility data.

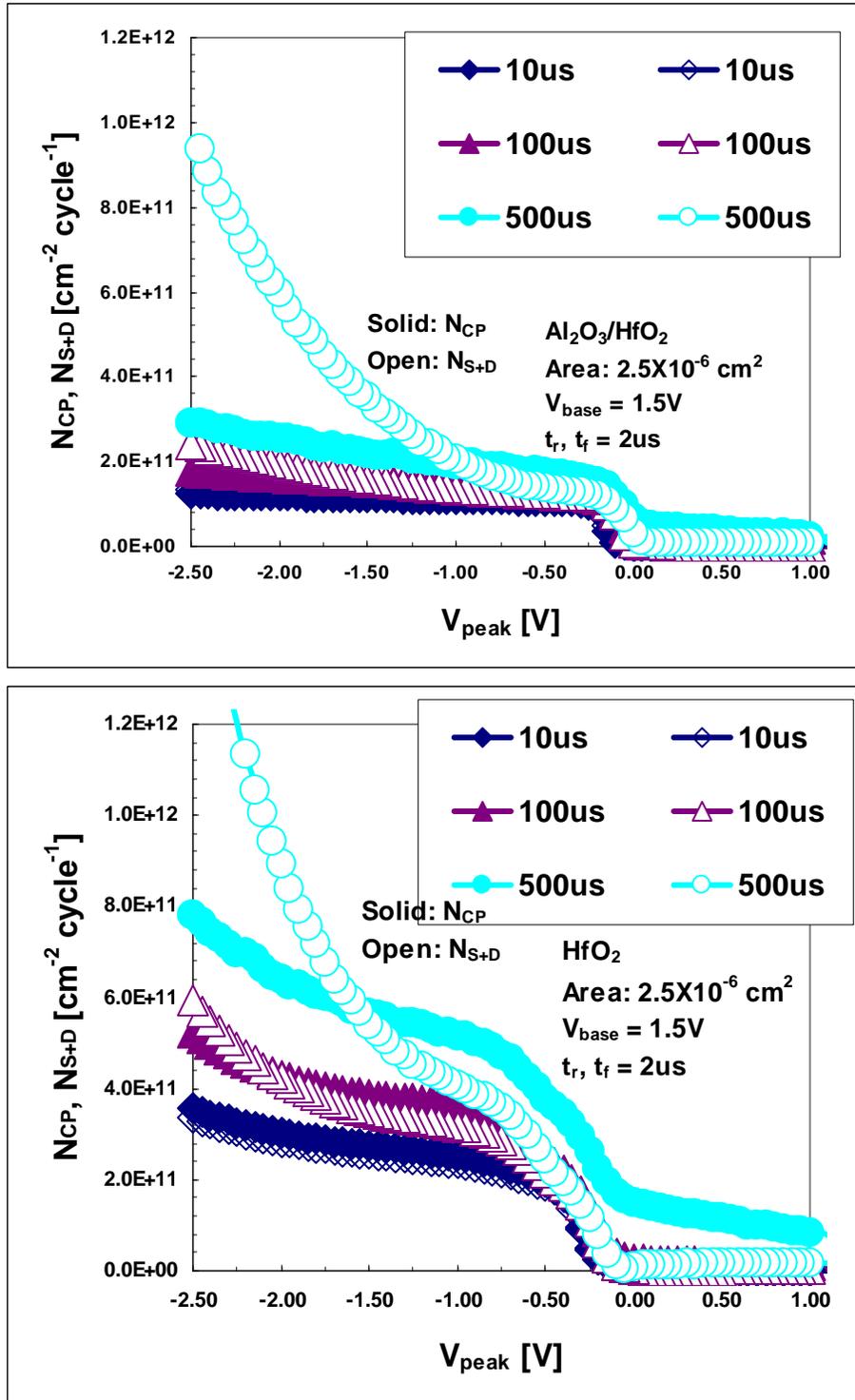


Figure 5.20 Amplitude sweep charge pumping results with various charging times. TaN/HfO<sub>2</sub> stack shows more dependence on frequency than Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub>.

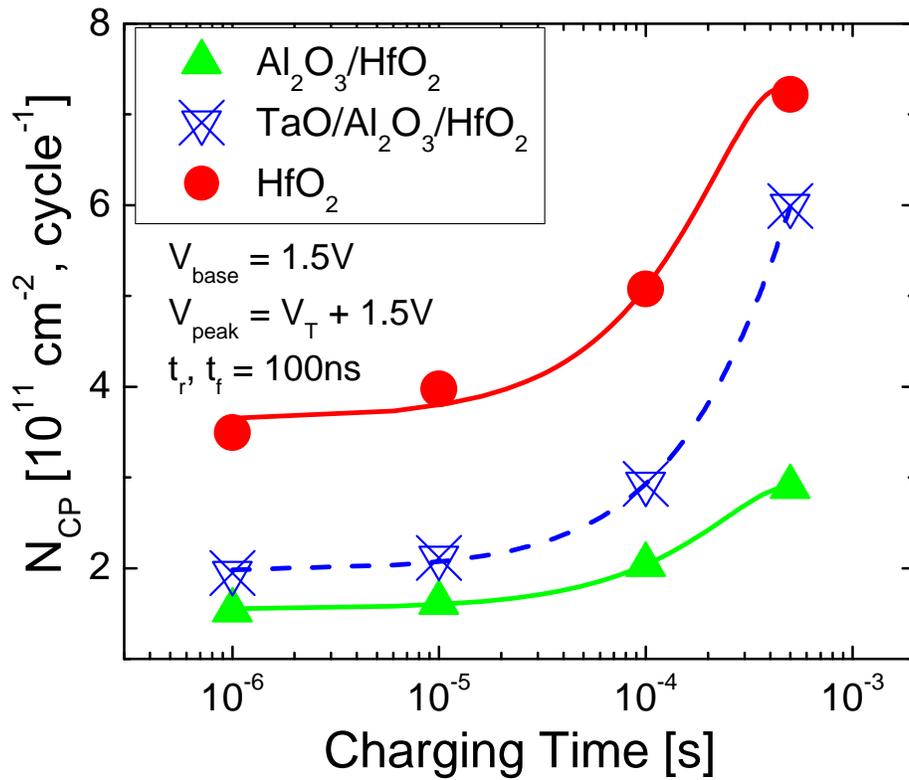


Figure 5.21  $N_{CP}$  vs. charging time for HfO<sub>2</sub> based dielectric. Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack shows less dependence on charging time indicating less bulk traps near the interface than HfO<sub>2</sub> stack.

### 5.3.4.3 Impact on Reliability caused by capping layer

Negative Bias Temperature Instability (NBTI) is a good way to evaluate device reliability of a pMOSFET. NBTI causes p-channel threshold voltage shift toward higher value resulting in reduction of drive current and transconductance at the operating voltage. NBTI measurements were done using stress and sense technique as illustrated in Fig 5.22. Different levels of voltage were applied to the gate in order to stress the device while source, drain, and body terminals of pMOSFET were grounded. The  $I_{ds}-V_{gs}$  characteristics as well as

base level charge pumping were monitored periodically during the stress. The key parameters such as  $V_T$ , subthreshold swing (S), transconductance ( $G_m$ ), and average interface state density ( $N_{it}$ ) were extracted from the measurements. It is noted that some degree of  $V_T$  can be recovered due to the measurement delay between stress and sense cycle.

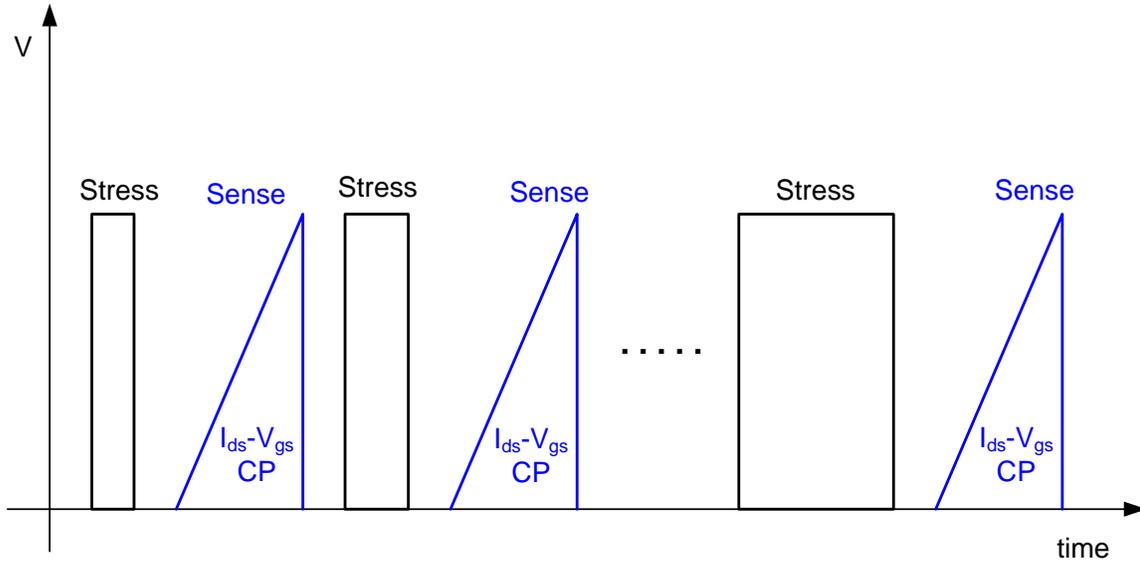


Figure 5.22 Stress and sense measurement setup for the NBTI testing. During stress cycle voltage is applied to the gate while source, drain, and body are connected to the ground. During the sense cycle, typical  $I_{ds}-V_{gs}$  and charge pumping are sensed. Stress and sense cycle are controlled through the switching matrix with Keithley 4200 system.

Figure 5.23 demonstrates  $I_{ds}-V_{gs}$  characteristics over time for TaN/HfO<sub>2</sub> gate stack under the stress level of  $V_{ox} = -1.75V$ . It is clearly observed that  $V_T$  is shifted to the negative direction (increasing pMOSFET  $V_T$ ) as time and corresponding drain current at a given  $V_{gs}$  is degraded. Extracted  $\Delta V_T$  ( $V_{T, stress} - V_{T, initial}$ ) is then plotted for different  $V_{ox}$  and the result is shown in Fig. 5.24. It is observed that most of the  $V_T$  shifts occur in the beginning of the

stress and then saturates thereafter indicating typical NBTI characteristics as already discussed in chapter 2.

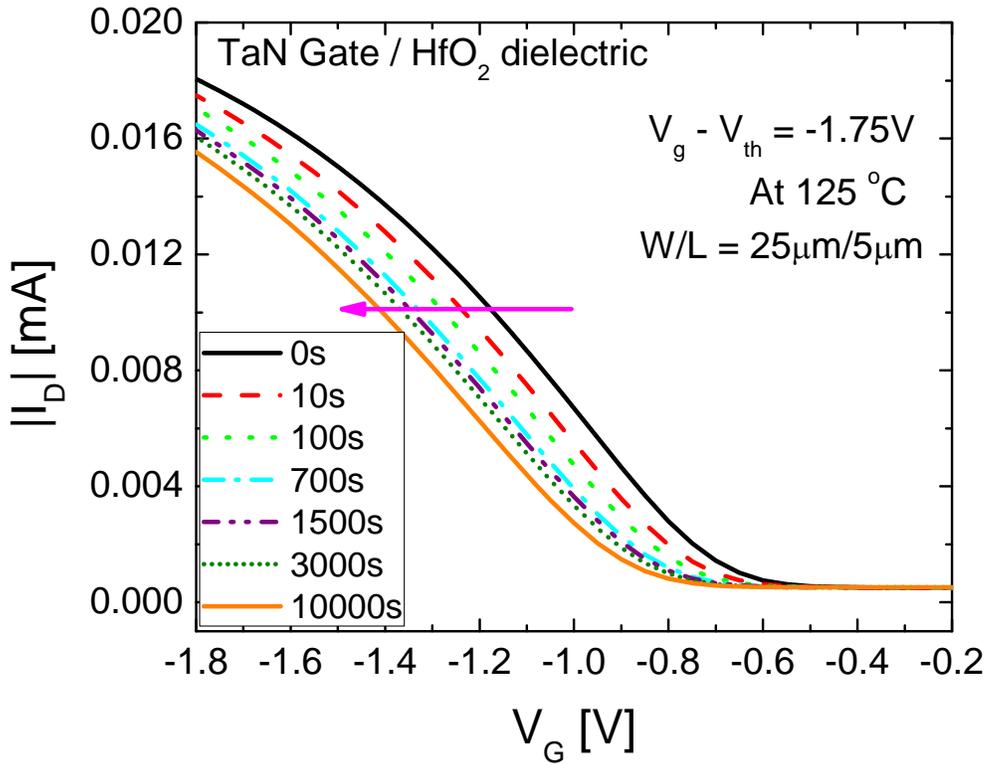


Figure 5.23  $I_{ds} - V_{gs}$  results as a function of stress time at  $125^\circ\text{C}$  for TaN/ $\text{HfO}_2$  gate stack. Large  $V_T$  shift as well as drain current reduction is obtained.

When device is under  $V_{ox} = -1.75\text{V}$  stress,  $\Delta V_T$  value is not saturated and keeps increasing indicating that generation of bulk traps also contributes the  $V_T$  shift at high field stress.

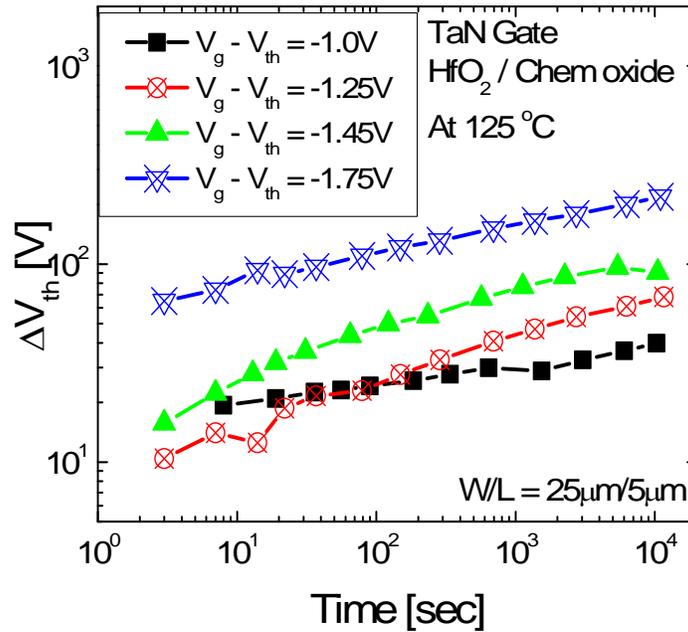
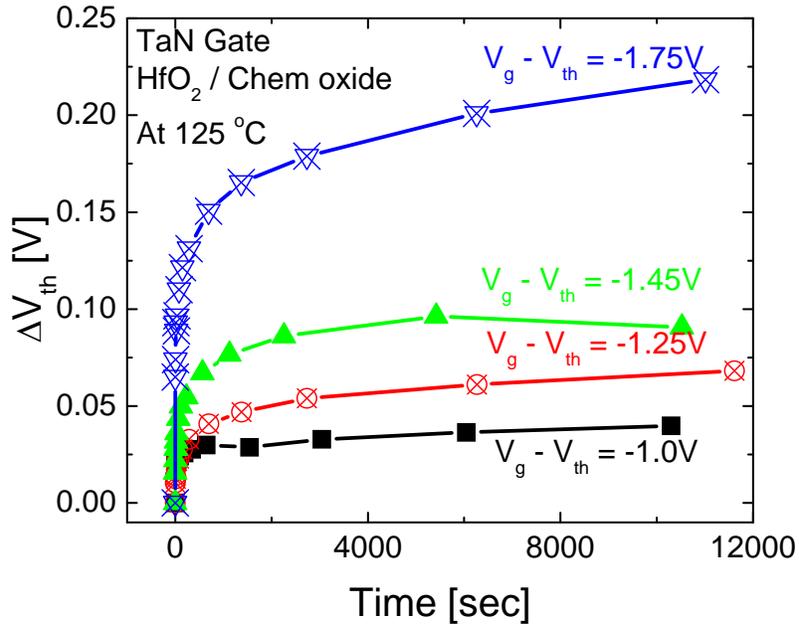


Figure 5.24  $V_T$  shifts over time evolution with TaN/HfO<sub>2</sub> stack in (a) linear and (b) log time scale. Most of  $V_T$  shifts occur at the beginning of stress time indicating typical NBTI degradation behavior. The power law fitted time exponent is similar to SiO<sub>2</sub>.

The time, temperature, and oxide field dependence of  $V_T$  shift in  $\text{SiO}_2$  devices under negative bias temperature stress can be described by the empirical relationship [147]

$$\Delta V_t = CE_{ox}^m \left( \frac{-E_a}{k_B T} \right) t^\alpha \quad (5.1)$$

where  $C$  is a constant,  $E_a$  is an activation energy,  $m$  is a power exponent with a range of 3~4, and  $\alpha$  is a time exponent with a range of 0.2~0.25. Figure 5.24 (b) shows the  $\Delta V_T$  over time in log scale with the extracted exponents of 0.18~0.24 which is similar value as  $\text{SiO}_2$  dielectric. Figure 5.25 shows  $\Delta V_T$  as a function of applied field for TaN/ $\text{HfO}_2$  stack at  $125^\circ\text{C}$  after 3000s stress. Solid line represents a power-law fit to the data with exponent  $\sim 3$  (also similar to  $\text{SiO}_2$ ).

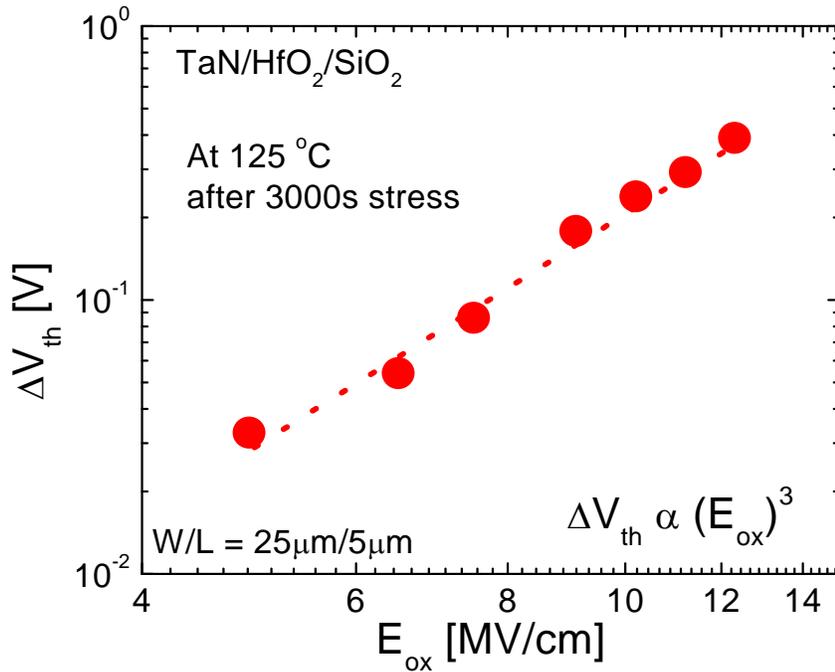


Figure 5.25  $V_T$  vs.  $E_{ox}$  with TaN/ $\text{HfO}_2$  stack.  $V_T$  shifts obey power law with exponent  $\sim 3$ .

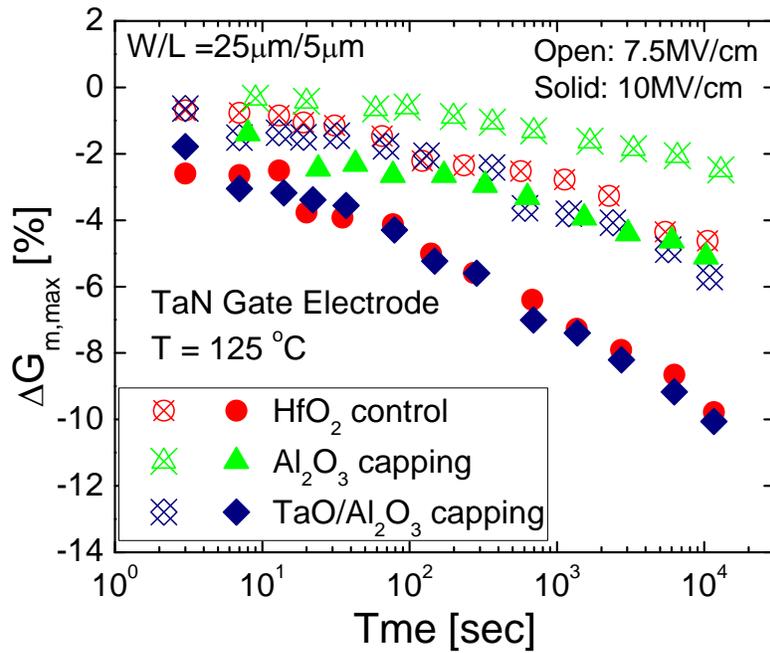
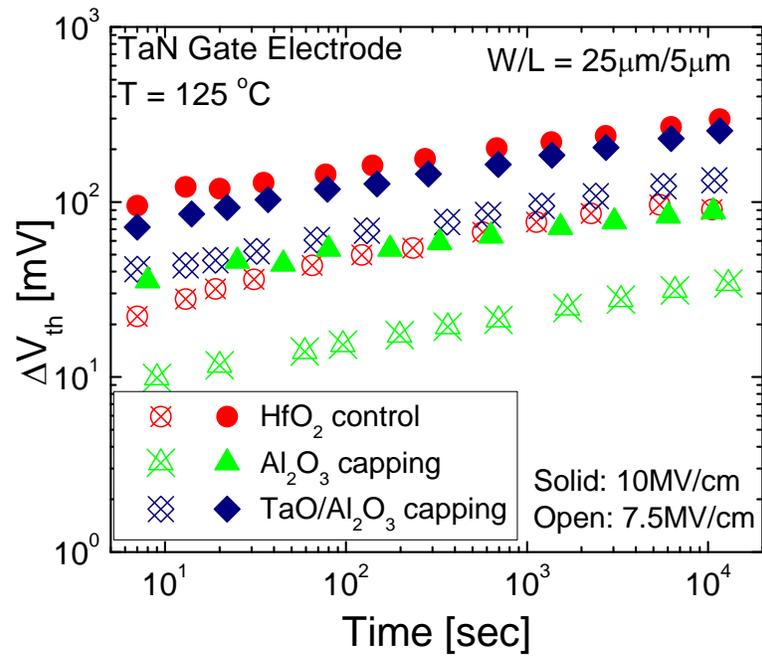


Figure 5.26 (a)  $\Delta V_T$  shifts over time and (b) corresponding  $G_m$  degradation with two different stress conditions at  $125^{\circ}\text{C}$ .

It is therefore confirmed that the  $V_T$  shift behavior is similar to the  $\text{SiO}_2$  based dielectric suggesting that the NBTI degradation mechanism with Hf-based dielectrics can be explained by well known reaction-diffusion model [148]. Thus, the  $V_T$  shift over time is mainly caused by the reaction of a hole with hydrogen atom at the interface followed by the hydrogen diffusion into the oxide. Figure 5.26 shows the impact of device reliability by the incorporation of capping on TaN/HfO<sub>2</sub> stack. It is noted that since the EOT for samples is different, the same effective field (gate overdrive over EOT) through the dielectric stacks was applied rather than same overdrive voltage. Two different effective fields (7.5MV/cm and 10MV/cm) were applied to the gate in order to stress the device at 125°C. The  $V_T$  shift behavior over time follows the power law dependence with the exponents of 0.17 ~ 0.21 for all samples. It is noted that the slope is independent of the applied field suggesting that interface state generation ( $\Delta N_{it}$ ) is the main mechanism responsible for the  $V_T$  shift rather than the bulk trap generation or charge trapping effect. If the charge trapping associated with defects or bulk traps in the high- $k$  layer causes the  $V_T$  shift, then the interface state and transconductance do not change over time as already seen in PBTI characteristics in Chapter 4. However, extracted  $G_m$  clearly shows large reduction after stressing confirming the  $V_T$  shift of the PMOS device is indeed attributed to the interface state generation. Both charge pumping and subthreshold swing were used to monitor interface state variation over time as shown in Fig. 5.27. The longer the device is stressed, the more silicon hydrogen bonds are broken by inversion charges (holes) resulting in higher interface state density, hence increasing charge pumping current ( $I_{CP}$ ) as well as subthreshold swing (S).

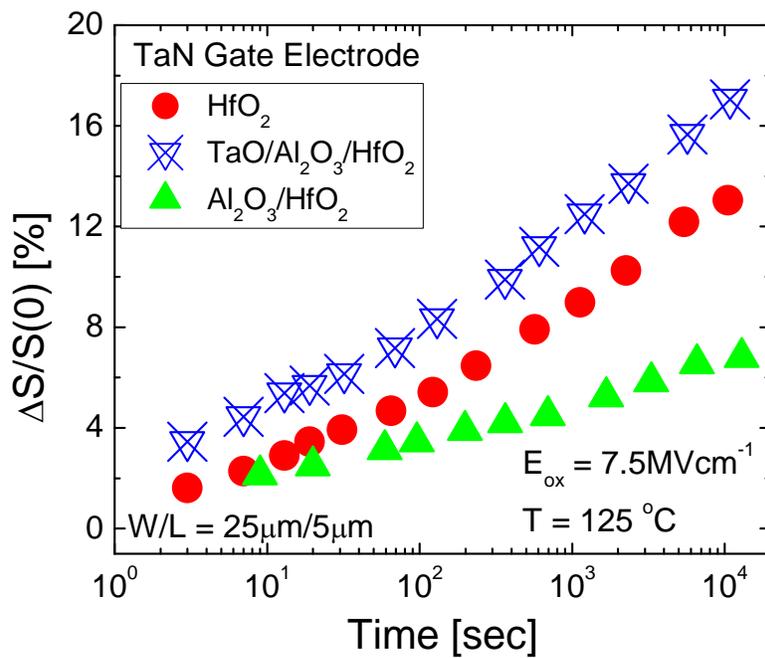
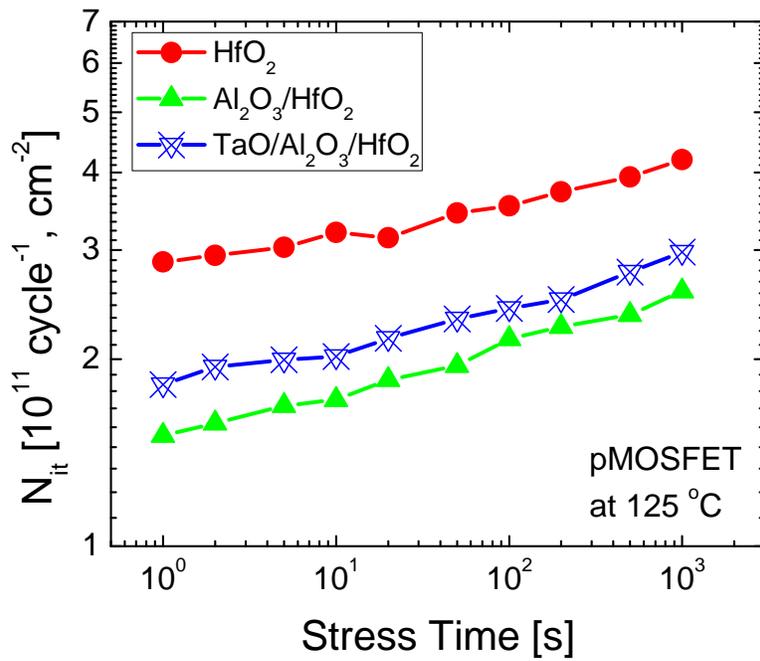


Figure 5.27 (a)  $N_{it}$  generation over time from the charge pumping measurement and (b) Subthreshold swing degradation over time. Higher generation rate was observed with  $\text{HfO}_2$  dielectric.

Charge pumping measurement provides direct information for the interface state. However, since there is about 1.3s of delay time between stress and sense cycle due to the switching some of the generated interface states are potentially recovered or passivated by released hydrogen. Therefore subthreshold characteristics were also monitored to compare with charge pumping data. As discussed in chapter 2 subthreshold swing is related to the interface state as

$$S = 2.3 \frac{nkT}{q} = 2.3 \frac{kT}{q} \left( 1 + \frac{C_d + C_{it}}{C_{ox}} \right) \quad (5.2)$$

The change in subthreshold swing due to the change in interface state density is related to

$$\delta S = 2.3 \frac{kT}{q} \frac{\delta N_{it}}{C_{ox}} \quad (5.3)$$

assuming the depletion layer capacitance is constant. During the  $I_{ds}-V_{gs}$  measurement, the subthreshold swing is changing with gate bias if interface traps are generated. The charge pumping and subthreshold swing characteristics over time, as shown in Fig. 5.27, confirm that the incorporation of  $Al_2O_3$  capping into the TaN/HfO<sub>2</sub> stack can suppress the generation of the interface states. However the TaO/ $Al_2O_3$  capping generates more interface states than  $Al_2O_3$  capping as obtained from the subthreshold swing characteristics, and is attributed to having worse interfacial oxide quality as discussed before. Therefore, it is concluded that  $Al_2O_3$  incorporation into HfO<sub>2</sub> provides good reliability characteristics having less  $V_T$  shift and less  $G_m$  degradation and this is attributed to the creation of strong Hf-Al bonding inside HfO<sub>2</sub> resulting in suppression of hydrogen diffusion into the bulk HfO<sub>2</sub> dielectric [149-150]. Another possible explanation for having better NBTI characteristics with capping layer as

compared to  $\text{HfO}_2$  layer is attributed to the suppression of nitrogen diffusion from the gate. Nitrogen is known to accelerate NBTI degradation of pMOSFET due to the i) lowering the dielectric barrier and ii) increase in hole trapping sites [150]. The incorporation of a capping layer between TaN gate and host high- $k$  can act as a diffusion barrier for nitrogen and hence minimizes nitrogen induced NBTI reliability concerns. Based on NBTI characteristics it is expected that the lifetime of the device with capping layer also better than single dielectric. The 10 year projection for various stress fields based on  $\Delta V_T=50\text{mV}$  as failure criterion is shown in Fig. 5.28. The incorporation of capping slightly improves lifetime as expected.

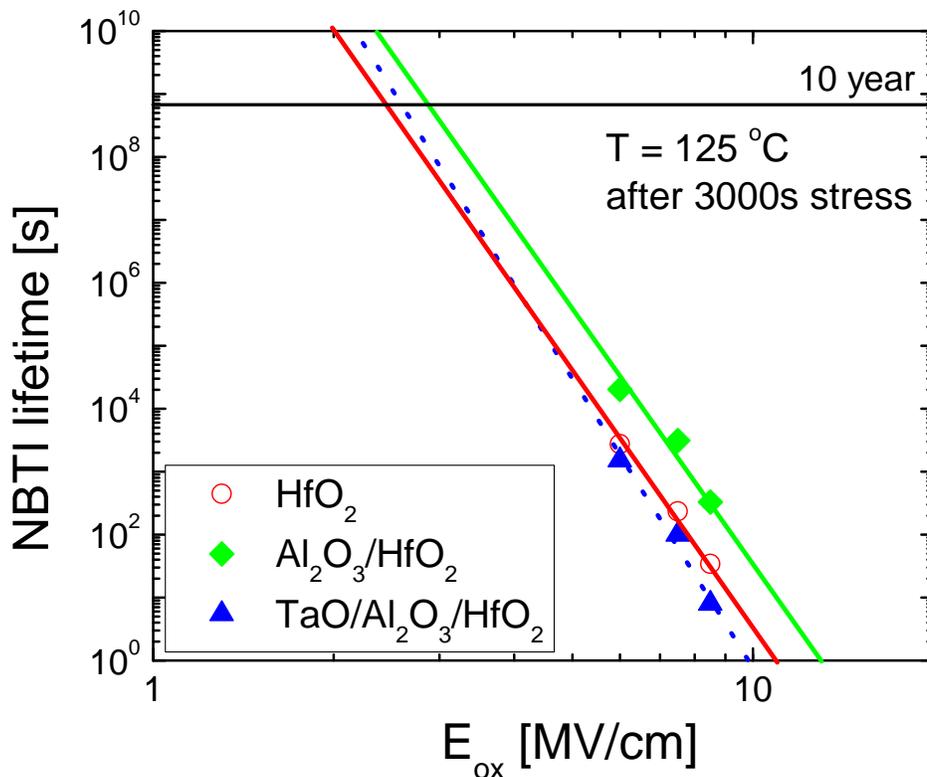


Figure 5.28 10 year lifetime projection for  $\text{HfO}_2$  based dielectric.  $\text{Al}_2\text{O}_3/\text{HfO}_2$  dielectric shows better lifetime.

## 5.4 Summary

It was found that AlTaO capping layers can effectively modulate  $V_T$  further for pMOS devices without degrading dielectric properties, and maintain excellent mobility. The reaction between Ta and Al not only creates d-states in the  $Al_2O_3$  matrix to enhance  $V_T$  further than  $Al_2O_3$  capping but also prevents Al diffusion to the bottom interface which minimizes Al-induced mobility degradation. Furthermore, the incorporation of capping layer in  $HfO_2$  dielectrics can change the structure of  $HfO_2$  dielectrics such that 1) mobility degradation caused by crystallization of the  $HfO_2$  layer is avoided by the capping layer retarding  $HfO_2$  crystallization and 2) device reliability characteristics (NBTI) are improved by suppression of hydrogen diffusion. The presence of an  $Al_2O_3$  layer between the TaN gate and  $HfO_2$  dielectric can also suppress nitrogen diffusion from the TaN gate resulting in better NBTI characteristics. However, if the composition of Ta is high (>60%) in AlTaO layer, then the degree of  $V_T/V_{FB}$  modulation is reduced and therefore it is critical to control the composition of Al and Ta in order to maximize the  $V_T$  modulation.

## Chapter 6

### Conclusion and Future Outlook

In this work, the effect of group III elements incorporated into advanced metal gate / high- $k$  dielectric stacks was investigated to achieve the desired gate stack work function providing suitable device threshold voltage ( $V_T$ ) without degrading electrical performance. The physical origins and possible mechanisms were provided in order to explain the experimental results. By incorporating group III elements into the gate stack, device  $V_{FB}/V_T$  was modulated to the desired value for both NMOS (by using Lanthanide) and PMOS (by using Al-based dielectric capping) while maintaining key device properties. Based on these studies, an alternative route to achieve dual CMOS metal gate/high- $k$  dielectric stacks for the next generation technology was demonstrated and supported with encouraging experimental results.

#### 6.1 Conclusion

The following is a summary of the conclusions of this dissertation:

- (i) The impact of Rare Earth metal (RE = Gd and Eu) incorporation into Ni-based FUSI gate on  $HfSiO_x$  dielectrics was investigated in terms of effective work function modulation and device characteristics. It was found that the structural properties with Gadolinium (Gd) and Europium (Eu) incorporation into Nickel

(Ni) Fully Silicided (FUSI) gate electrodes are markedly different and resulted in different degrees of effective work function modulation. It was found that Ni–Gd alloys tend to form stable compounds during silicidation and produce a Si–rich layer with amorphous / nanocrystalline structure near the FUSI gate electrode / high– $k$  dielectric interface. This compositional and structural change is the main mechanism responsible for effective work function modulation with Gd incorporation. However, in the case of Europium, Eu atoms tend to segregate outside the Ni–FUSI layer during silicidation and resulted in a uniform  $\text{Ni}_x\text{Si}_y$  layer with Eu pile–up layer at the FUSI gate electrode / high– $k$  dielectric interface. This pile-up is believed to be the main cause of effective work function modulation with Eu incorporation. It was also found that the incorporation of Gd and Eu metals into Ni–FUSI gate can remotely scavenge the interfacial oxide layer resulting in lower EOT of the device.

- (ii) Second, the role of Rare Earth metal incorporation was studied as an oxide capping approach on  $V_{\text{FB}}/V_{\text{T}}$  modulation. It was found that the La concentration at high– $k$ /SiO<sub>2</sub> interface is the key factor for the  $V_{\text{FB}}$  modulation and the effects of host high– $k$  materials as well as gate electrode on  $V_{\text{FB}}$  shift were minimal. Presence of La at the high– $k$ /SiO<sub>2</sub> interface forms a dipole layer creating band offset and hence the gate work function is modulated. The effect of La<sub>2</sub>O<sub>3</sub> capping on device performance with a focus on threshold voltage modulation and mobility is also evaluated. The device with TaN/HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> gate stack provided a 400mV

shift in  $V_T$  from the control  $\text{HfO}_2$  with minimal degradation in mobility. In the case of  $\text{TaN}/\text{La}_2\text{O}_3/\text{HfO}_2$  gate stack, only 100mV shift in  $V_T$  was observed with large degradation in mobility. This is attributed to the fact that the La atoms decompose the interfacial  $\text{SiO}_2$  during the annealing causing the creation of large interface states and thereby degrading the mobility. For device reliability, the incorporation of  $\text{La}_2\text{O}_3$  improves both breakdown and PBTI characteristics since the La-induced dipole layer can effectively increase barrier height for electron injection as well as passivate some level of bulk charges in the  $\text{HfO}_2$  layer. Based on experimental data, a mechanism explaining the electrical results was also proposed.

- (iii) Finally, an analysis of the oxide capping approach for PMOS devices was investigated using group III elements and their alloys. The impact of  $\text{Al}_2\text{O}_3$  and  $\text{AlTaO}_x$  incorporation on electrical performance of  $\text{TaN}/\text{HfO}_2$  stack is provided. 400mV modulation in threshold voltage and significantly improved mobility were observed with  $\text{AlTaO}_x$  capping incorporation without degrading dielectric properties. The addition of Ta in  $\text{AlTaO}_x$  structure produces d-states in the  $\text{Al}_2\text{O}_3$  matrix resulting in additional  $V_T$  shift toward PMOS band-edge. This  $\text{Al}_2\text{O}_3$ -TaO reaction not only modulates the device  $V_T$  towards values suitable for PMOS but also retards Al diffusion through the  $\text{HfO}_2$  layer preventing Al-caused mobility degradation as shown in XPS and backside SIMS analysis. Furthermore, the incorporation of these capping layers can improve device NBTI characteristics by

suppressing the hydrogen release during the negative bias stress at elevated temperature.

## **6.2 Future Outlook**

Based on the findings in this work, the following is a list of future research that can provide more insight into this field.

### **6.2.1 Optimization of dielectric stacks**

This dissertation suggests that the La induced silicate formation should be constrained only to the high- $k$ /SiO<sub>2</sub> interface in order to provide good electrical characteristics in case of NMOS devices and the prevention of the Al diffusion is the key to maintain good electrical characteristics in case of PMOS devices. The continuation of this work needs to be focused on the optimization of the device structure in terms of the fabrication process such as the growth of good quality of interfacial SiO<sub>2</sub>, the thickness ratio of the capping and high- $k$  dielectrics, post deposition annealing (PDA) conditions (time, temperature, and environment), and thickness of metal gate electrode.

### **6.2.2 Validation of proposed model**

This work clearly demonstrates that the bottom interface is critical with La diffusion for NMOS devices whereas the reaction between Al and Ta is the primary factor for PMOS

in order to achieve the desired  $V_T$  value of metal gate/high- $k$  dielectric stack. Although the empirical model was proposed based on the experimental results, the future work needs to be focused on the atomic level calculation or modeling to validate proposed model.

### **6.2.2 Reliability of capping layer incorporation**

The reliability of scaled devices is one of the major concerns and even more so when high- $k$ /metal gate stack is incorporated due to its nature. The key point of the reliability of the device is to have a good interfacial oxide as well as to minimize charges in the high- $k$  layer. Although the dielectric capping incorporation improved the reliability characteristics as compared to single high- $k$  layer, it can be improved further by using good quality of interfacial  $\text{SiO}_2$  with optimized post deposition annealing.

### **6.2.3 Dielectric capping approach for non-Si substrate**

The creation of negative charges due to the reaction between Ta and Al can be applied to alternate substrates which require high threshold voltages, such as SiC based MOSFETs and GaN high electron mobility transistors for power and RF applications. The most common fabrication technique for SiC power MOSFET uses thermally grown  $\text{SiO}_2$  followed by very high temperature annealing in nitrogen ambient. This results in mobility enhancement but device  $V_T$  typically becomes negative. By using Al-Ta based gate stack it would be possible to achieve positive  $V_T$  shift while maintaining high mobility values.

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## APPENDIX

# Appendix

## MOSFET Fabrication Process (4 level GEM Masks)

**Always do the control experiment first for all processing steps**

1. Baker Clean
  - a. JTB 111 solution (JTB111 965ml + Hydrogen Peroxide 212ml + DI water 4823ml) for 10min
  - b. DI water rinse
  - c. Spin Dry (RCA only use)
2. Field Oxidation (wet oxidation)
  - a. 2500Å to 3500Å
  - b. Measured by Nanometrics
3. Active Photo-lithography
  - a. N2 blow wafer
  - b. Spin coat 1813 photoresist
    - i. 40sec at 4000 rpm
    - ii. Apply P-20 HMDS (improve adhesion)
    - iii. Apply Shipley 1813
  - c. Soft bake 1 min at 115°C
  - d. Align and Exposure (MA6)
    - i. 12sec
  - e. Develop
    - i. MF319 (PH 13) solution for 50 to 70sec
  - f. Spin Dry
  - g. Post bake 5min at 115°C

4. Plasma Descum
  - a. 600mTorr at 300W + 80sccm O<sub>2</sub> for 300sec (in case of 2500Å Fox)
5. Etch Field Oxide (in Buffered Oxide Etch solution)
  - a. Etch rate: normally 500 Å/min
    - i. For 2500Å: 5min 8sec
6. Strip photoresist (Nanostrip)
  - a. 10min in dirty(right) followed by 12min in clean(left)
  - b. DI water rinse + spin dry
7. RCA clean
  - a. SC1(NH<sub>4</sub>OH: H<sub>2</sub>O<sub>2</sub>: H<sub>2</sub>O=1100:1100:5500ml) for 10min at 75°C
  - b. DI rinse
  - c. SC2(HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O=1100:1100:5500ml) for 10min at 75°C
  - d. DI rinse + Spin dry
8. Sacrificial Oxidation
  - a. Dry oxidation at 850°C (thickness about 100 Å)
  - b. Measure by Ellipsometry
  - c. Etching oxide using 1% HF solution
9. RCA clean
  - a. SC1(NH<sub>4</sub>OH: H<sub>2</sub>O<sub>2</sub>: H<sub>2</sub>O=1100:1100:5500ml) for 10min at 75°C
  - b. DI rinse
  - c. SC2(HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O=1100:1100:5500ml) for 10min at 75°C
  - d. DI rinse + Spin dry
10. Gate Dielectric Deposition
  - a. SiO<sub>2</sub>: furnace (dry oxidation) at 800 to 900 °C
  - b. ALD: HfO<sub>2</sub> and/or Al<sub>2</sub>O<sub>3</sub>
    - i. HfO<sub>2</sub>: using TDMAH and water at 200°C without exposure
    - ii. Al<sub>2</sub>O<sub>3</sub>: using TMA and water at 200°C without exposure
11. Gate Electrode Deposition (Metal)
  - a. UHV-PVD tool

## 12. Gate Electrode Pattern

- a. Metal gate (typical)
  - i. PVD metal gate deposition
  - ii. Spin HMDS and Shipley1813
  - iii. Soft bake
  - iv. Align and exposure (light field mask)
  - v. Develop and spin dry
  - vi. Hard bake
- b. Metal gate (if using lift-off)
  - i. Spin HMDS and Shipley1813
  - ii. Soft bake
  - iii. Align and exposure (dark field mask)
  - iv. Develop and spin dry
  - v. Hard bake
  - vi. Metal gate deposition by PVD
- c. Poly-Si
  - i. LPCVD poly-Si(630°C) or a-Si (550°C) deposition or PVD si
  - ii. Spin HMDS and Shipley1813
  - iii. Soft bake
  - iv. Align and exposure (light field mask)
  - v. Develop and spin dry
  - vi. Hard bake

## 13. Etching Gate electrode

- a. Metal gate: use proper wet and dry etching recipe for metal
  - i. For W: use W etchant (KOH hood)
  - ii. For TaN/TiN: BCl<sub>3</sub> dry etching
- b. Lift-off metal gate
  - i. NMP solution on sonicator ~30min
  - ii. DI water rinse and dry

- c. Poly-Si gate
  - i. Dry etching
    - 1. Plasma-Therm
    - 2. Two step  $\text{Cl}_2$  etching (recipe name: bongmook)
  - ii. Wet etching
    - 1.  $\text{HNO}_3:\text{NH}_4\text{F}:\text{H}_2\text{O}=21:1:11$
    - 2. DI water rinse and dry
- 14. Strip PR using Nanostrip (make sure all PR are removed)
- 15. LTO deposition  $\sim 100\text{\AA}$  (sacrificial oxide)
  - a. 410C less than 5min
  - b. PECVD at Duke
- 16. Ion implantation (should calculate dose and energy for your target from the simulation)
  - a. As(NMOS) Dose/Energy= $5\text{e}15/20\text{KeV}$
  - b.  $\text{BF}_2$ (PMOS) Dose/Energy= $2\text{e}15/10\text{KeV}$
- 17. Etching LTO (you can etch this sacrificial LTO after activation annealing)
  - a. BOE (LTO etch is faster than thermal  $\text{SiO}_2$ )
- 18. S/D activation
  - a. 950°C 10s for  $\text{BF}_2$  (pMOS)
  - b. 1000°C 5s for As (nMOS)
- 19. LTO deposition (2000Å to 3000Å) by LPCVD
  - a. Isolation oxide
- 20. Pattern LTO for contact hole
  - a.  $\text{N}_2$  blow wafer
  - b. Spin coat 1813 photoresist
    - i. 40sec at 4000 rpm
    - ii. Apply P-20 HMDS (improve adhesion)
    - iii. Apply Shipley 1813
  - c. Soft bake 1 min at 115°C

- d. Align and Exposure (dark field)
    - i. 12sec
  - e. Develop
    - i. MF319 (PH 13) 50 to 70sec
  - f. Spin Dry
  - g. Post bake 5min at 115°C
  - h. Descum for 3min 30s at 300W for 1700A LTO (optional)
21. Etching LTO (**the most critical step**)
- a. BOE and/or HF solution
  - b. DI water rinse and dry
22. Etching high-K (**the most critical step**)
- a. Dry or wet etch (be sure high-k etched completely)
  - b.  $\text{HfO}_2$  or  $\text{Al}_2\text{O}_3$  can be etched by  $\text{BCl}_3$
  - c. HF dip to remove interfacial  $\text{SiO}_2$
  - d. DI water rinse and Dry
23. Pattern contact metal (lift-off)
- i. Spin HMDS and Shipley1813
  - ii. Soft bake
  - iii. Align and exposure (dark field mask)
  - iv. Develop and spin dry
  - v. Hard bake
24. Evaporate metals (**do not use the rotation in thermal evaporator**)
- a. Ti/Al (50nm/200nm)
25. Lift-off metal by NMP solution (may need heat up)
26. Backside oxide etching
- a. Use cotton swab to apply BOE to backside
27. Backside Al evaporation (optional)
28. Forming Gas Anneal
- a. Using Furnace: 400°C 30min / 500°C 30min

b. Using RTA: 400°C 5min

Note:

If you like to use 5 level masks, please see H. Lazar's Thesis for detailed process flow.