

ABSTRACT

VICTOR, ALAN M. Microwave Power Oscillator utilizing Thin-Film Ferroelectric Varactors. (Under the direction of Dr. Michael B. Steer.)

Microwave communication systems demand simplified and efficient point-to-point and point-to-multi-point links. This research focuses on direct RF (radio frequency) carrier generation and architectures to support microwave systems utilizing this technique. Direct carrier frequency generation relies on the synthesis of power oscillators operating efficiently at the final output frequency. Power oscillators in this work permit a stable tunable frequency source with output power greater than 1 watt with modulation capability. Improvement in operating efficiency or the conversion of DC input power into RF microwave signals requires devices operating with high breakdown voltage. The high breakdown voltage feature removes the need for wasteful conversion of available high DC input supply voltages to lower operating voltages via voltage regulation or DC-to-DC conversion. The combination of appropriate RF architecture, analysis techniques, and device technology are investigated to maximize operating efficiency. In this work, the effort is focused on the capabilities of Gallium Nitride on Silicon (Si-GaN) HFET coupled with Barium Strontium Titanate (BST) thin-film varactors.

Studies are confined to an operating frequency range of 1–6 GHz. Oscillator design is implemented via a synthesis technique and is achieved by combining the procedure of active device mapping with large signal circuit analysis. The outcome of a portion of this work identifies a routine of “tuning” the active device reflection coefficient to effectively absorb parasitics associated with hybrid oscillator implementation. Emphasis is primarily on output power, RF conversion and load efficiencies, and tuning bandwidth. Oscillator load efficiency is approached via the application of describing functions for non linear operation. Nonlinear descriptions are general so both the FET and the bipolar device share similar expressions for load efficiency. Conversion efficiency must contend with thin-film varactor Q , which is also addressed. The development of high power sources with wide tuning bandwidth while maintaining adequate

phase noise also requires technology with high breakdown voltage. In this work, phase noise and tuning bandwidth are related to physical factors which describe the varactor. Networks which permit favorable tradeoff in tunability and power efficiency are discussed. The characteristics of GaN on Silicon and of BST varactors, components that both have demonstrated high breakdown voltage, are investigated. The tracking phase lock characteristic of an oscillator using a BST varactor is unique and revealed in this study. Distinguishing the noise mechanism in oscillators incorporating BST varactors is addressed. The study of noise in BST is investigated at baseband and then applied to power oscillator design. Studies of small signal oscillators with output power less than 100 mW and operation below 1 GHz provides important design insight. These studies assess the impact that a varactor with large breakdown voltage has on noise, on linearity of the oscillator tuning frequency characteristics, without the aberrations caused by having a large RF signal. Furthermore, oscillator operation at lower frequencies also permits the study of large RF excitation voltages when present and impressed across the varactor. The alteration of oscillator performance is readily observed, as the affect of circuit parasitics are less.

Although circuit function and device characteristics are the central part of this work, it is essential that the integration of a system perspective be included. Power oscillators are part of an RF system and a new radio architecture design resulting in improved RF power conversion efficiency which is presented. In this work a phase lock methodology is used to implement a power oscillator directly operating at the carrier frequency. This direct carrier launch method is contrasted with the traditional heterodyne architecture. For both cases, a methodology for optimizing the signal-to-noise ratio of a cascade transmitter system using what is called an equal contribution methodology is presented. This method is also applied to receive systems. The approach readily determines the offending network or networks in the RF system and also provides an approach for optimization of system dynamic range.

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Microwave Power Oscillator utilizing Thin-Film Ferroelectric Varactors

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DEDICATION

First and foremost, I want to dedicate this work to my family. Particularly my wife and her kitchen table, which I monopolized for many years in completing this work. Thank you, Phyllis, for forcing me to continue to work towards this goal. I want to thank my family, my son Todd, my daughter Lynda, my daughter-in-law, Heather, and our newest member, my grand-daughter Madeline, for their patience. There were many hours spent away from them, working on this project. However, I knew quite early on, this dissertation was not going to write itself. If there were a way to place it on auto pilot, I would have!

BIOGRAPHY

Alan Victor received the B.S.E.E. degree from the University of Florida, Gainesville and the M.S.E. degree from Florida Atlantic University, Boca Raton. After graduation he joined the Motorola Communications Group working in research and development, and was a senior staff engineer. He received several patents in circuits and systems relating to the two-way radio industry. Following Motorola he co-founded a wireless radio LAN company providing data communications equipment to the auto ID industry. Subsequently he was at IBM, and then the Nitronex corporation investigating Silicon Germanium and Gallium Nitride on Silicon circuits for radio systems targeting the personnel communications industry. While at IBM, he began work towards the Ph.D. degree at North Carolina State University, Raleigh. During that same period, he joined Harris Microwave Division as a Senior Scientist where he was involved with microwave transceiver design. His main interests are low noise circuits, power oscillators, and the application of ferroelectric materials. Mr. Victor is a member of Eta Kappa Nu and a senior member of the IEEE.

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Chapter 1

Introduction and Motivation

In this chapter we lay the ground work for the analysis of transceiver systems with emphasis on the transmit function. The case for simplifying the conversion from baseband modulation to carrier is presented and the analytic tools necessary for judging performance introduced. Measurements of circuits which comprise these systems are also addressed and subsequent sections will discuss some novel techniques for treating the measurements of noise in amplifiers and oscillators. Both of these network elements are fundamental to this work. The premise behind the idea of direct carrier launch is discussed as well as the initial work for proof of concept. This dissertation deals with the synthesis and methods for power oscillator design and their tuning ability is carried forward in subsequent chapters.

Reliable communication links require robust systems. Quality of Service (QoS) of competitive wireless links demand packet error rates that do not exceed 10^{-9} [1]. These links, wired or wireless, employ some form of error correction. Nevertheless not all of the required correction can be assigned to the communication protocol as the additional overhead reduces system data packet throughput. Therefore the system is required to maintain a minimum link margin. Link margin is a measure of the signal-to-noise ratio of the received signal presented to a decoder relative to the required transmitter output power to achieve a specific uncorrected packet error rate. A typical microwave link maintains a link margin of 30 dB or greater to alleviate cor-

rection requirements in fades or signal loss due to path degradation, for example changes in weather and seasonal variations. The link value consists of the sum of transmitter output power, receiver sensitivity including any coding gain, and total antenna gain [2]. Transmitter output power is on the order of 30 dBm and the receiver sensitivity for uncorrected code is typically -85dBm for a 128 QAM (quadrature amplitude modulation) system. Therefore, at this point, a system link gain of 115 dB not including antenna gains is available. At 6 GHz, the free space path loss over a 20 mile distance is approximately 138 dB. Therefore, the additional 50 dB system gain plus margin must be found from a combination of the error correction supported by the protocol and antenna gain; both receive and transmit. However, higher antenna gain will add size and cost to the system. In addition, in digital radio systems, noise, jitter, and non-linearity will introduce errors in the complex signal. These errors manifest themselves in both amplitude and phase. Two major components in the system transmitter hardware affect these errors the most and command significant attention. These are the power amplifier and the local oscillator. These two components are always present, irrespective of the system or transmitter architecture. The need to provide synchronization and timing in addition to agile frequency of operation falls squarely on the oscillator design. Establishing a specific signal-to-noise ratio of the link at a designated distance requires appropriate RF transmit power, sufficient stage linearity to process complex modulation without adverse distortion, and adequate receiver decode sensitivity. Some of these requirements are controlled by power amplification and design of the power amplifier (PA) system. Power amplifiers are treated as systems in the sense that additional feedback, feed-forward, and gain control networks are involved with the design of the PA, not just the PA itself. In this work both functions are incorporated into one network, the power oscillator. The design goal is to achieve operation directly at the required carrier frequency, achieve adequate power to meet the link margin, suppress noise and jitter, and enable modulation to support a high throughput communication system. The conservation of DC power consumption by minimizing the direct current at any supply voltage, and maximizing efficiency while minimizing distortion is the essential challenge. Minimization of operating DC

power consumption reduces the heat produced, improves reliability, and simplifies mechanical constraints. For example, permitting the use of compact heat-sinks and the elimination of forced air cooling, reduces weight and size while improving reliability through the elimination of moving components. Therefore, obtaining highly efficient conversion of DC input power to RF signal output power is a primary challenge. Current architectures readily consume 100 W of DC power for 1–2 W of output power for microwave links using complex modulation. Rarely however do the efficiencies obtained in RF transmit point-to-point systems rise above 5%.

1.1 Architecture overview

Design of wireless communication links begin with the development of system specifications. These specifications dictate electrical requirements, and indirectly affect the cost, size and scope of the product and the mechanical aspects of the products. The system specifications, of course, are driven by market demands, customer requirements, and competitive pressure. Designs can be evolutionary or revolutionary, and usually a hybrid of both to achieve risk mitigation while providing competitive advancement. Designs which are evolutionary tend to be based on some form of heterodyne architecture, Figure 1.1. In the heterodyne transmitter architecture a modulated signal is produced at a low frequency. Then the signal is converted up in frequency using a mixer and then the signal is amplified to the required level. In a heterodyne receiver architecture, the continuation of Figure 1.1, a low noise amplifier amplifies the received RF signal which is mixed down using one or mixing stages to a frequency that can be readily sampled, shown in Figure 1.2. Variations of this translation theme are possible. It is not uncommon to see upconversion first applied in the receive function, then followed by down conversion, to improve spurious performance. As the market drives the need for greater capabilities, usually new network blocks are added to an established architecture, or the network blocks themselves are improved.

The most common architecture used in communications systems architecture is the heterodyne architecture. This system relies on the use of small-signal networks to develop complex

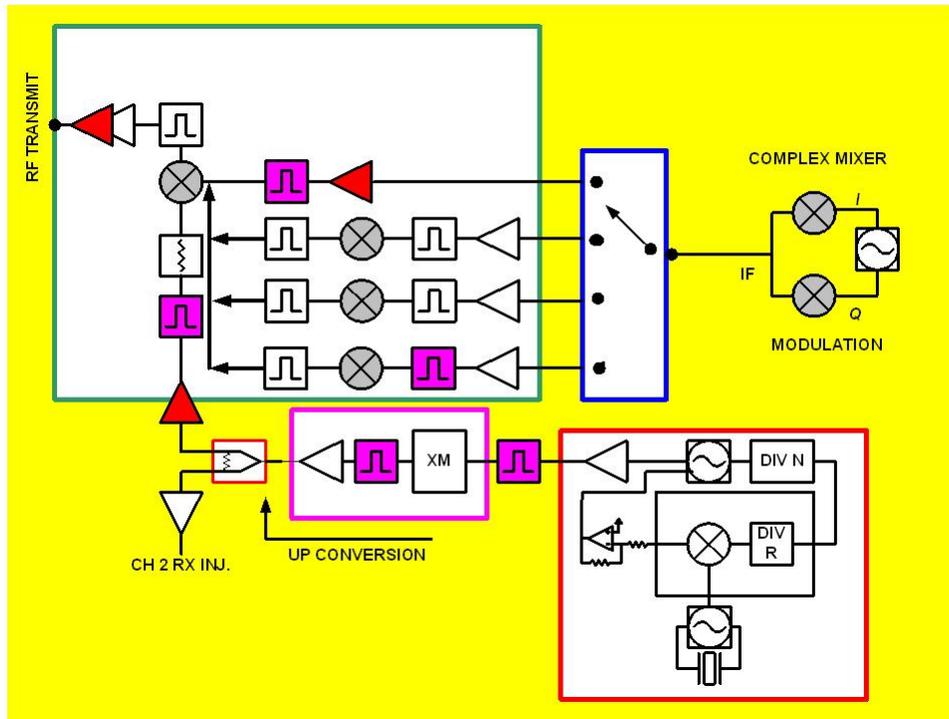


Figure 1.1: Microwave heterodyne up-down converter block diagram, the transmit up conversion portion only.

signals which are translated in frequency. Many of the system performance parameters are driven by both local oscillators and mixers that implement frequency translation. The translation process is followed by a subsystem that consists of a cascade of networks which provides signal conditioning; including filtering and amplification. Systems based on the heterodyne architecture can be bulky, expensive and difficult to apply in frequency agile systems. Also, since multiple sources are involved, frequency plans and mitigation of spurious tones is a constant challenge and this is a significant driver of design costs and per unit cost.

Recently simplifications of the heterodyne system have evolved which blend digital implementations of some networks with the appropriate analog subsystem. These architectures place much of the system functionality into software and firmware applications, e.g. software defined radio systems. Other architecture simplifications resort to low frequency networks which are converted in one step of frequency translation, so called zero IF or low IF heterodyne architec-

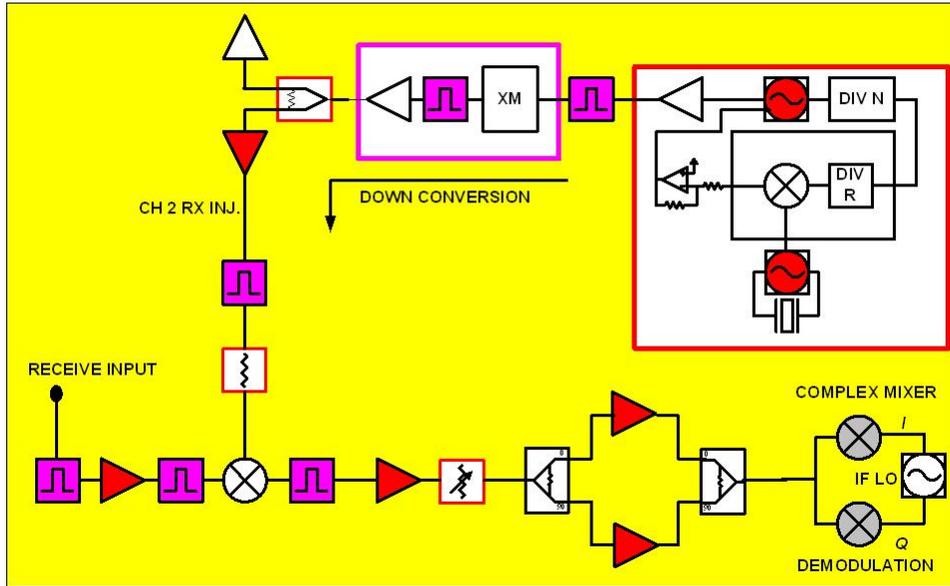


Figure 1.2: Microwave heterodyne down-converter block diagram, the receive down conversion portion only. High dynamic range is required in the receive function and as well requires attention to circuit linearity.

tures. Both systems still require at least one or more frequency translation and filter networks, and lead quickly to complexity for multiple frequency operation [3].

The system architecture considered in this work in this dissertation does not contain mixing stages. In this work the operation of the transmitter is directly at carrier frequency. No frequency translation networks are required other than those for baseband modulation and demodulation. If the method of modulation and demodulation is accomplished through a phase lock system, then the operation of up conversion (transmitting) and down conversion (receiving) is accomplished directly through the loop. The so called direct carrier launch system dispenses with traditional mixer down conversion or up conversion as operation is at the desired final RF carrier frequency.

1.2 System analysis tools

Fundamental to all radio front-end architectures is maintaining performance objectives by a careful balance of network gain, noise, linearity and frequency management. Our work presented in this dissertation provides a basis for optimizing the complex trade-offs, particularly in cascade systems. The approach is unique as we identify a different perspective towards assessing these trade-offs and it is based on an equal stage contribution methodology. We lay the ground work here and further develop the approach in subsequent sections.

One prior methodology is based on cascaded system analysis and application of the Friss formula [4]. Spreadsheets in Excel format, Figure 1.2, are commonly utilized in the design process to establish stage by stage parameters to meet system requirements. This technique is further improved by adding tunable parameters to elements such as gain, temperature, and bandwidth adjustment. In the development of these sheets there are a number of short comings, some of which are addressed in this work. First there is no clear method of synthesis to meet system goals and second no clear rendering of the offensive stage or stages. Translation networks (mixers) must be handled carefully. As mixers are dual response networks, the assignment of system bandwidth must be understood in the context of mixer operation [5]. The budget analysis method and the cascade formulation should not be limited to small signal analysis. Moderate stage compression and the treatment of noise partitioned into amplitude and phase components or the quadrature representation of noise is desired. Cascade noise analysis usually treats pure noise only. System budget diagrams tend to be static, while in fact they need to be dynamic. One function, often overlooked, is the need to apply a moderate compression factor or gain reduction value to the budget analysis sheet. This factor would be a function of each stage power output and subsequent stage power input with an associated compression factor. An empirical method applicable to a large number of amplifiers is based on the dependence of the power gain, G_p as a function of the input signal power, P_s [6]

$$G_p = \frac{P_{sat}}{P_s} \left(1 - \exp \left(\frac{-G_{ss} P_s}{P_{sat}} \right) \right). \quad (1.1)$$

Description	Sym	Gain	Noise Figure	IP3	P1dB	Input	Output	Cum Gain	Cum IP3	Cum IMD	Cum NF	In Band Cum Noise	SNR
		dB	dB	dBm	dBm	dBm	dBm	dB	dBm	dBc	dB	dBm	dB
Quad Mixer AD8345	⊗	0.0	19.0	18.5	2.5	-11.0	-11.0	0.0	18.50	-65.00	19.00	-79.80	68.80
3 dB Pad	⊞	-1.0	1.0	100.0	100.0	-11.0	-12.0	-1.0	17.50	-65.00	19.01	-80.78	68.78
Amplifier GALI-1	▽	15.5	3.5	40.0	23.0	-12.0	3.5	14.5	32.21	-63.42	19.10	-65.20	68.70
3 dB Pad	⊞	-8.5	8.5	100.0	100.0	3.5	-5.0	6.0	23.71	-63.42	19.11	-73.69	68.69
BP Filter	⊞	-1.0	1.0	100.0	100.0	-5.0	-6.0	5.0	22.71	-63.42	19.11	-74.68	68.68
3 dB Pad	⊞	-4.0	4.0	100.0	100.0	-6.0	-10.0	1.0	18.71	-63.42	19.14	-78.66	68.66
Amplifier AH2 (WJ)	▽	15.5	3.5	40.0	23.0	-10.0	5.5	16.5	33.19	-61.39	19.19	-63.11	68.61
3 dB Pad	⊞	-2.0	2.0	100.0	100.0	5.5	3.5	14.5	31.19	-61.39	19.19	-65.11	68.61
Combiner ADP-2-1W	⊞	-3.0	3.0	100.0	100.0	3.5	0.5	11.5	28.19	-61.39	19.19	-68.10	68.60
0 ft IDU-ODU Cable	⊞	0.0	0.0	100.0	100.0	0.5	0.5	11.5	28.19	-61.39	19.19	-68.10	68.60
Cable Interface	⊞	-3.0	3.0	100.0	100.0	0.5	-2.5	8.5	25.19	-61.39	19.20	-71.10	68.60
Switch	⊞	-1.0	1.0	100.0	100.0	-2.5	-3.5	7.5	24.19	-61.39	19.20	-72.10	68.60
Amplifier#1 (bypassable)	▽	0.0	0.0	100.0	100.0	-3.5	-3.5	7.5	24.19	-61.39	19.20	-72.10	68.60
Attenuator 1 (Cable AGC)	⊞	-14.0	14.0	26.0	16.0	-3.5	-17.5	-6.5	10.08	-61.16	19.42	-85.88	68.38
Amplifier#2	▽	10.0	2.0	29.0	19.0	-17.5	-7.5	3.5	19.56	-60.11	19.54	-75.75	68.25
BPF+Pad	⊞	-8.0	8.0	100.0	100.0	-7.5	-15.5	-4.5	11.56	-60.11	19.66	-83.64	68.14
Mixer	⊗	-9.0	9.0	11.0	1.0	-15.5	-24.5	-13.5	1.98	-58.95	20.49	-91.81	67.31
Amplifier#3	▽	16.0	4.5	30.0	20.0	-24.5	-8.5	2.5	17.71	-58.42	21.84	-74.46	65.96
BPF 1 (TxIF)	⊞	-3.0	3.0	100.0	100.0	-8.5	-11.5	-0.5	20.71	-70.42	21.85	-77.44	65.94
Pad	⊞	0.0	0.0	100.0	100.0	-11.5	-11.5	-0.5	20.71	-70.42	21.85	-77.44	65.94
Variable Attenuator#2	⊞	-13.0	13.0	7.0	-3.0	-11.5	-24.5	-13.5	4.33	-63.66	22.42	-89.88	65.38
Amplifier#4	▽	11.0	5.0	30.0	20.0	-24.5	-13.5	-2.5	15.19	-63.37	23.48	-77.82	64.32
Pad	⊞	-2.0	2.0	100.0	100.0	-13.5	-15.5	-4.5	13.19	-63.37	23.50	-79.80	64.30
Variable Attenuator #3	⊞	-5.0	5.0	15.0	5.0	-15.5	-20.5	-9.5	7.36	-61.73	23.62	-84.68	64.18
Amplifier#5	▽	11.0	5.0	30.0	20.0	-20.5	-9.5	1.5	18.08	-61.15	23.97	-73.33	63.83
Pad	⊞	-5.0	5.0	100.0	100.0	-9.5	-14.5	-3.5	13.08	-61.15	23.99	-78.30	63.80
Variable Attenuator #4	⊞	-5.0	5.0	15.0	5.0	-14.5	-19.5	-8.5	7.27	-59.55	24.08	-83.22	63.72
Amplifier# 6	▽	8.0	5.0	30.0	20.0	-19.5	-11.5	-0.5	15.13	-59.26	24.33	-74.97	63.47

Figure 1.3: Excel spreadsheet of a microwave transmitter system. This includes baseband and modulation blocks through selectable gain amplifiers, filters and mixers. The cascade may also include cable and antenna losses.

Here G_{ss} is the linear small signal gain and P_{sat} the saturation value of the output power. Note that (1.1) provides one of the key elements of a describing function for large signal power amplifiers and oscillators, namely compression.

Further discussions are devoted to power compression and the treatment of noise separated into quadrature components. An overview analysis of an up converter is considered next and in Section 2.3 cascade and cascade-feedback systems specific to the up converter are discussed in more detail. The motivation for spurious reduction and the issues created in the heterodyne architectures are presented in Section 2.2.

Both synthesis and flagging of stage limiting metrics are addressed by a contribution method

of identification and developed in a Mathcad© script discussed in this work. Detailed development is discussed in Section 6.3. An example of the technique is illustrated by utilizing the

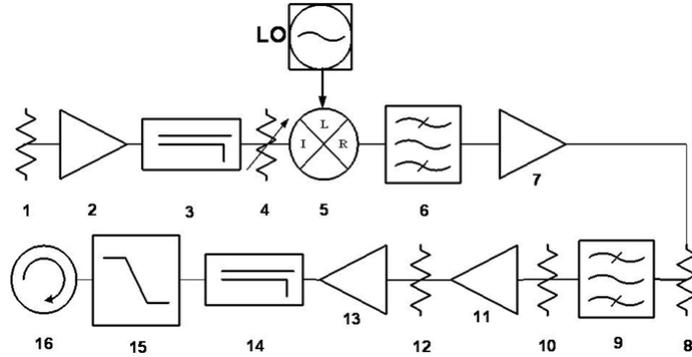


Figure 1.4: Block diagram of a 16 stage up-converter cascade.

block diagram of Figure 1.3. In this figure a 16 stage up-conversion transmitter cascade is presented. Each of the elements of the system cascade are defined in a single column 16 row vector described in Table 1.1. The local oscillator source (LO) is not part of the vector table in this analysis nor is the LO noise. However, it is shown in Figure 1.3 for clarity with connection to the up-conversion mixer, mixer-5. The cascade consists of both active and passive networks which are characterized in terms of their noise factor (noise figure in dB), gain and distortion. Distortion level is gauged in terms of the ratio of fundamental to third-order distortion power level for each stage, therefore the measurement units are dBm. These values are entered into a vector table and each block distortion value is described by either an input or output intercept value, $IP3_i$ or $IP3_o$ respectfully [7]. This method of characterization and the methodology of intercepts is discussed in a latter section. In turn each cascade element is recast into the cascade formula in terms of a contribution value. As displayed in Figure 1.4, it is readily apparent for example that noise power contribution from stage 7 is dominant. A similar arrangement for distortion using individual stage intermodulation is calculated. Typically the worse case addition of intermodulation components is used [8]. In combination, the noise contribution

Table 1.1: 16 stage up-converter cascade

System Cascade Parameters				
stage n	description	gain (dB)	noise figure (dB)	distortion (dBm)
1	IF attenuator	-6	6	51
2	IF preamp	11	4	15
3	IF coupler	-4	4	49
4	IF attenuator	-2	2	47
5	up-converter mixer	-11	10	22
6	bandpass filter	-2	-2	47
7	buffer amplifier	12	5	15
8	variable attenuator	-3	3	28
9	bandpass filter	-1	1	46
10	variable attenuator	-1	1	46
11	driver amplifier	12	5	15
12	attenuator	-1	11	46
13	power amplifier	23	7	21
14	RF detector coupler	-0.4	0.4	60.4
15	low pass filter	-0.5	0.5	60.5
16	circulator	-0.3	0.3	50

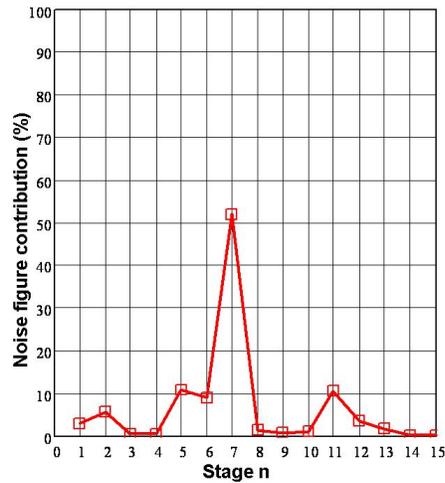


Figure 1.5: Noise contribution of each stage to the total noise factor

and the distortion contribution permit dynamic range through the cascade to be charted. This coupling of noise power contribution and distortion power distribution readily provides system spurious dynamic range. Portraying the dynamic range in this manner clearly demonstrates

how the first few initial stages in the cascade can dominate. For example, a rapid reduction in signal-to-noise ratio would be difficult to recover if the first stage of the cascade had excessive output noise power. The 2nd stage in this cascade example sets the limit as the reduction in the system dynamic range is rapid, producing over 20 dB change, see Figure 1.5. Thereafter further reduction is gradual. Interesting to note, that although stage 7 leads in noise contribution, stage 2 results in a dramatic reduction in dynamic range. Location of the offensive stage and the numeric contributions are equally important. In latter sections we will see that this is particularly poignant when stage nonlinearity is considered. In the case of receiver cascade the available gain, G_{av} (*Power available from the network/Power available from the source*) and in the transmit cascade the power gain, (*Power delivered to the load/Power into the network*)[21] will compress at sufficiently high input signal levels. Usually the situation directed in receiver design is not as severe as in transmit design because of the presence of interstage selectivity. However in transmitter architectures where complex modulation is present the amplitude component must be closely monitored to maintain the constellation fidelity. In the n-QAM system with the signal power confined to the average carrier frequency, the magnitude and phase of the carrier vector are equally important. Careful application of automatic gain control (AGC)

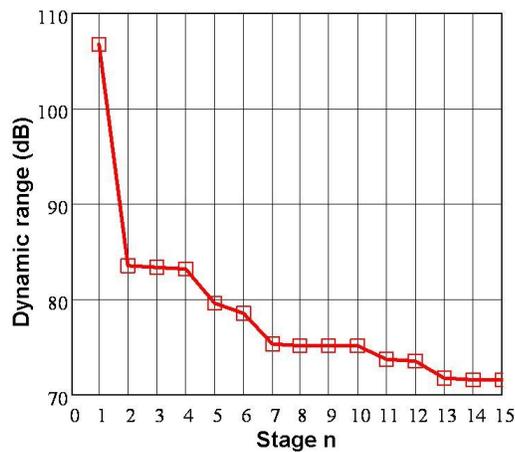


Figure 1.6: Dynamic range line segment plot for the 16 stage cascade

implemented with variable gain attenuators (VGA) in conjunction with fixed attenuation are necessary elements in design. For example, as displayed in Figure 1.6, the increase in front-end attenuation (attenuator 4 in Figure 1.3) in a transmitter cascade has actually resulted in an increase in output power and a decrease in noise power. Although the power gain shows an increased slope, the output intercept remains flat and actually decreases. At first glance, this appears to be counter intuitive. This is the result of stage(s) operating under power compression as mentioned earlier and the location of the variable attenuation. The first result as the attenuator is significantly increased in attenuation is a decrease in output intercept point. This is a direct consequence of decreased mixer output intercept despite the overall power gain increasing. As a stage output intercept is a function of the stage associated power gain, we have $OIP_3 = IIP_3 + G_p$, where OIP_3 and IIP_3 are the output and input third-order intercept respectively and G_p is the stage power gain. Consequently increased mixer and attenuator 4 loss lead to decreased output intercept of the mixer stage and consequently decreased output intercept to the cascade. The decrease of intercept point occurs despite the power gain of the network increasing and is a consequence of stages operating into compression. That is, these actions are the ramifications of a system network operating at large input signal levels; large relative to the compression factor of each stage. Furthermore, the compression factor is a function of this specific attenuator setting as well as a function of the location of the attenuator and the gain distribution. The particular response demonstrated here is a consequence of earlier stages which are removed from compression.

Finally, the noise figure is not independent of the affect of large signal input levels. The noise figure improves as attenuation increases and the affects of large signal compression are removed [22, 23]. These techniques, when applied in analysis, are also applicable in system synthesis. The concept here is to permit an equal contribution methodology for the system cascade. As an example, by doing so, no single stage dominates the total system noise power. If this approach is applied to intermodulation, whereby all stages contribute to intermodulation, then a system cascade which just meets the dynamic range target is possible with potentially

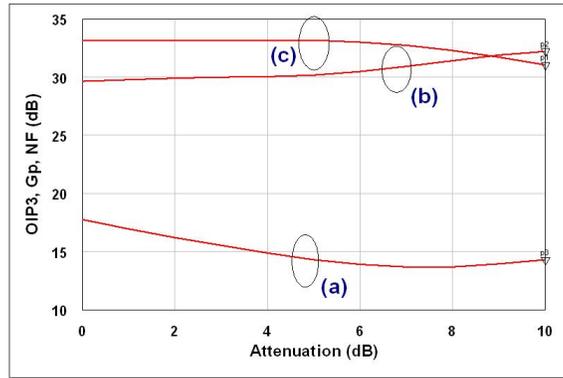


Figure 1.7: The transmitter cascade of Figure 1.3 demonstrating power gain compression, (a) noise figure, (b) power gain, (c) OIP3 vs. variable attenuator-4 setting in dB

lower power expenditure. This is in contrast to the condition where only the first few stages dominant the noise power. Permitting the first stage to have higher gain shifts intermodulation distortion requirements to latter stages in the cascade; the consequence of this is increased power dissipation. The equations necessary to synthesize such a cascade are closed form and dependent on the topology of the cascade. In certain cascade topologies, the interrelationship between stage gain and loss is defined from stage to stage. In other cases, a requirement for a trade-off table is necessary as no such straight forward “closed form” coupling condition of stage parameters exists between the stages. Of course, the realization of networks with such prescribed noise, gain, and distortion for an equal contribution system is not straightforward. Most important though, such a technique leads to a system budget cascade that is initially set to minimize power requirements. In addition, trade-off tables created in the process clearly evolve. They are not assigned in an ad hoc manner [24].

1.3 Direct carrier launch system

The desire to minimize size, power consumption, and cost motivates the designer to consider simplified architectures. Minimizing the number of conversion stages in a transmitter cascade is one architecture that achieves these goals. Frequency generation is still required as well as complex modulation. A power oscillator or a lower power oscillator followed by a power amplifier (MOPA) is another technique. Frequency agility while preserving modulation capability is provided by a phase lock loop (PLL) system. Phase modulation is introduced without the influence of the loop bandwidth, while amplitude modulation is normally introduced outside the loop. Under all types of modulation adequate carrier-to-noise ratio must be maintained. Consequently, oscillator phase noise reduction and loop tracking dynamics require analysis of the PLL system. In this dissertation the case whereby the tunable oscillator is BST varactor based is considered.

The generation of high power in an oscillator while maintaining high efficiency requires an appropriate set of technologies. Gallium nitride (GaN) coupled with a ferroelectric component such as Barium Strontium Titanate is studied in this work. Both technologies are comple-

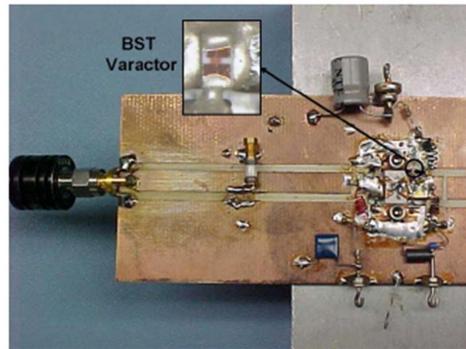


Figure 1.8: Power GaN oscillator coupled to BST tuning varactor

mentary as they possess high breakdown voltage necessary to sustain the required performance in a power oscillator application. The C-V curve of a BST varactor is unique. Consequently

the tuning capability of the BST varactor in oscillators is investigated. A study in Section 2.5.2 addresses the fundamental tuning range of a varactor network and the resonator, while minimizing phase noise. There is an inherent trade-off in designing the oscillator for minimum phase noise while obtaining sufficient tunability. The problem here is to identify the correlation in the varactor device Q and the required tuning bandwidth of the resonator in conjunction with the active device.

In addition, the presence of circuit parasitics in the resonator will limit tuning range. It is demonstrated in this dissertation that proper embedding of the active device, while considering the nonlinear limiting of the oscillator, successfully permits resonator parasitics to be absorbed. The trajectory of the device negative reflection coefficient and the resonator impedance vs. frequency is required. Prior to and during self limiting in the active device, modification of the device impedance is possible to successfully absorb the parasitic elements of the resonator. This is essential in preventing multiple frequency oscillation. Both oscillator tunability and meeting the criterion for oscillation are analyzed through mapping techniques. These techniques are particularly important as the configuration of the active device, a Gallium Nitride on Silicon FET here, is in common source configuration. Although the grounded source arrangement assists in removing heat from the device, via the substrate connected source contact, it is not amenable to a broadband oscillator design. An example of the network studied in Chapter 5 is illustrated in Figure 1.7. Configurations based on both the negative resistance approach and the classical open loop amplifier are discussed. The case of an open loop stable amplifier is purposed whereby specific gain and phase relationships are required to synthesize a stable oscillator. All of the oscillators studied in this dissertation are self-limiting as opposed to using external leveling or gain control loops. Finally, in addressing oscillator tunability, electromagnetic (EM) and circuit co-simulation (*EM Co-Simulation*) is required. Co-simulation is particularly important in high frequency hybrid designs where parasitic metal interconnects must be considered. In oscillator circuits exact tuning frequency vs. voltage must meet predictable values. There is no pre or post manufacturing trimming allowed, as this would add unnecessary cost. Finally,

the temperament of the tuning curve eventually effects in-band oscillator noise and the carrier-to-noise ratio. Therefore, the tuning curve of the oscillator must be reasonably insensitive to component tolerance and temperature.

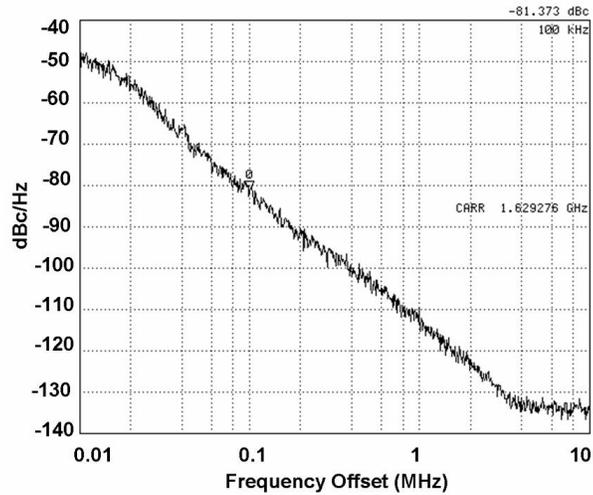


Figure 1.9: Power GaN oscillator-BST varactor carrier-to-noise via phase noise measurement

Analogous to noise factor in a receiver cascade, the noise distribution in a transmitter system utilizing a phase locked power oscillator is important. In this work, the excess additive noise of the power GaN FET and the BST varactor is observed through phase noise measurements and through independent noise studies of the devices. Phase noise data is invaluable as it permits the collaboration of the individual noise sources associated with the devices measured at base-band frequencies with actual in circuit operation. For example, excess noise of an individual component, a resistor, may be measured at audio frequencies with the ease of measurement of low frequency spectra. Then the same resistor component can be embedded in an oscillator system for measurements at carrier frequencies. In our case studies, the system is the power oscillator embedded in a phase locked loop (PLL). Use of the power oscillator permits application of high RF voltage to the varactor and the consequent modification of the noise parameters. These noise parameters are compared to DC measurements of the BST varactor and differences

noted. Oscillator signal-to-noise noise measurements are employed via a signal source analyzer system. In addition, a carrier desensitization method is also used, and detailed in Section 7.2. The data is presented as a measure of the single sided noise power spectral density and is shown in Figure 1.9. Where possible these large signal RF carrier noise measurements are correlated with low frequency baseband noise measurements and also include measurements of DC leakage current, small signal capacitance, and varactor unloaded Q .

Frequency control of the power oscillator is essential. If complex modulation is desired then both phase and amplitude signals must be introduced to the oscillator without adversely impacting the average frequency. A PLL is required. In this work a phase lock multiplier (PLM) is utilized. The noise characteristics of the PLM are known in the context of the power oscillator noise and other noise sources which contribute within the control loop. The final output power to carrier noise ratio of a locked power oscillator is a function of the PLL bandwidth and in turn the oscillator tuning gain. Since the oscillator tuning gain depends partly on the varactor capacitance vs control voltage, we might expect the carrier-to-noise of the oscillator would depend on the varactor type. Indeed BST varactors possesses a unique C-V curve which alters the open loop gain characteristic of the PLM. Therefore the noise tracking properties of the loop are modified. The operation of the PLL is drastically modified as compared to that using a conventional junction varactor VCO (voltage controlled oscillator). Methods of dealing with these differences are presented.

In this dissertation the design of phase locked oscillators operating in a PLM through 6 GHz are reported. The oscillators are hybrid in construction. As part of this study to improve tuning bandwidth, particularly with the BST varactor, a multitude of power oscillators on a single hybrid each covering a smaller percentage tuning bandwidth were considered. Other possibilities included transmission line varactor networks which multiply the reactance shift of the varactor and switched reactance resonators. Potentially these circuit modifications are more efficient and more cost effective than single broadband oscillator sources.

1.4 Publications

There are a number of publications that are derived from the work presented in this dissertation. The list of publications and works accepted for publication are as follows:

A. Victor and M.B. Steer, "Transceiver cascade system analysis and design via a contribution method," *International Journal of RF and Microwave Computer-Aided Engineering*, May 2006, pp.338-345.

A. Victor, J. Nath, K.G. Gard, J.-P. Maria, A.I. Kingon, and M.B. Steer, "Tracking phase-locked loop characteristics with a VCO using a barium strontium titanate (BST) thin-film varactor," *IEEE Radio and Wireless Symposium Rawcon 2007*, Jan 9-11, pp. 289-292.

Alan Victor, Jayesh Nath, Dipankar Ghosh, Brian Boyette, Jon-Paul Maria, Michael Steer, Angus I. Kingon, and Gregory Stauff, "A voltage controlled oscillator using Barium Strontium Titanate (BST) thin-film varactor," *IEEE Proceedings 2004 Radio and Wireless Conference*, Sept. 19-22, 2004, pp. 91-94.

Alan Victor, Jayesh Nath, Dipankar Ghosh, Seymen Aygun, Walter Nagy, Jon-Paul Maria, Angus Kingon, and Michael Steer, "Voltage controlled GaN-on-Si HFET power oscillator using thin-film ferroelectric varactor tuning," *European Microwave Conference 2006*, Sept 2006, pp. 87-90.

Alan Victor, Jayesh Nath, D. Ghosh, B. Boyette, J.P. Maria, M.B. Steer, A.I. Kingon, and G.T. Stauff, "Noise characteristics of an oscillator with a barium strontium titanate (BST) varactor," *IEEE Proceedings Microwaves, Antennas and Propagation*, Feb 6, 2006, pp. 96-102.

Alan M. Victor, and M.B. Steer, "Improved Y factor measurement using the second stage contribution to advantage," *IEEE 65th ARFTG Conference Digest 2005*, Spring 2005.

A. Victor, and M.B. Steer, "Reflection coefficient shaping of a 5-GHz voltage-tuned oscillator for improved tuning," *IEEE Transactions on Microwave Theory and Techniques*, December 2007, pp. 2488-2494.

A. Victor, and J. Nath, "Design of a C-Band microstrip voltage controlled oscillator using an electromagnetic-harmonic balance co-design Technique," *Asia-Pacific Microwave Conference*,

2007, Session FR-A2-F5, Dec. 14, 2007.

A. Victor, and J. Nath, “Circuit co-simulation and measurement techniques applied to voltage-controlled oscillator design,” *IET Microw. Antennas Propag.*, Vol.2, No.8, 2008, pp.922-928.

Alan Victor, Jayesh Nath, “An analytic technique for trade-off of noise measure and mismatch loss for low noise amplifier design”, *IEEE WAMICON 2010 Conference*, Melbourne, FL., April 2010, accepted for publication.

1.5 Original Contributions

There are a number of distinct contributions in this dissertation. Several of these contributions are enumerated here with an overview. Details of further contributions will follow in subsequent sections. The original contributions are as follows:

1. Sections 1.2, 4.3.1 and 6.3

A brief introduction to this work was just touched upon in Section 1.2. The central point is an approach that permits maximizing the dynamic range of a cascade transceiver system while minimizing power consumption. In addition, the core methodology permits an initial stage assessment which eliminates the ad hoc method for assigning stage gain, loss, noise factor, and linearity to cascade blocks in an RF system. The central theme is the introduction of an equal contribution method as the initial starting point. A detailed example is discussed in Section 4.3.1.

2. Sections 4.6.1, and 5.1.4

The unique C-V characteristic curve of the BST varactor is investigated when the control element is a phase lock loop. Issues which arise and the potential problem introduced are not addressed in the literature. In a control system where the BST varactor is employed, designs must be cognizant of a system which will present sign reversal and eventually control system “hang and latch-up.” This property is unique to the BST transfer function when employed in

phase lock systems. This is dealt with in detail in Section 4.6.1.

3. Sections 4.6.2, and 4.6.7

The properties of the voltage controlled oscillator (VCO) are unique with the BST varactor employed. In this and subsequent work we identify noise, control, and distortion characteristics of the BST varactor based VCO. Emphasis on large signal coupling to the varactor and operational differences when compared to the junction varactor are noted. The investigation here is different to those where the central theme is filter and intermodulation distortion of multiple input signals. The impedance level in oscillator applications is significantly larger and the RF voltage impressed across the varactor potentially greater. Contrasting the junction varactor with the BST varactor is key.

4. Sections 2.5, 5.1.1, 6.1.1 and 6.1.2

The power oscillator is fundamental to direct carrier generation. While power amplifiers for complex modulation systems average 2–5% efficiency; power oscillators demonstrate 20–25% and provide additional benefit by reducing translation networks and minimizing filters. In this work, a technique of combining high voltage GaN and BST is demonstrated. A stable amplifier configuration is selectively regenerated by introducing L-C series feedback in the common source lead. This connection also permits heat to be extracted from the power FET via direct connections to the source. Mapping is used to find an appropriate series feedback network in the source lead for a combination of load and resonator port impedances at the drain and gate of the GaN FET. The design provided over 20% load conversion efficiency with 1.6 watt power output at 1.6 GHz and linear tuning provided by a BST varactor with over 100 V breakdown. No spurious modes or nonmonotonic tuning characteristics occur despite the tight coupling of the varactor to the resonator network.

5. Section 2.5.2

This work characterized the relation between the varactor Q and the required resonator Q to meet a specified oscillator phase noise and degree of oscillator tunability. We show that there is a clear trade-off in meeting these objectives for a specific varactor and contrast the junction varactor and the BST varactor in the analysis. Both varactor types have a pair of voltage limiting boundary values. One boundary value is the reverse voltage breakdown and avalanche breakdown. The other boundary case is the forward conduction in the junction varactor and an increase in shot noise of current. While the BST varactor does not suffer from a forward bias condition, it does suffer loss of tunability at one extreme boundary value and a rapid rise in noise voltage and phase noise degradation at the other extreme boundary value, near breakdown. Oscillator phase noise measurements indicate both varactor types demonstrate a rapid rise in phase noise as breakdown voltage is approached. Although, the BST varactor based oscillator demonstrated a more rapid rise in phase noise power than the junction varactor near voltage breakdown. Correlation of phase noise measurements, baseband-to-RF, and the influence of leakage current are presented in Section 4.6.2.

6. Section 7.2

The ability to measure noise figure and noise power accurately is key to RF system development and optimization. At microwave frequencies automatic noise figure measurements are limited in frequency range without resorting to frequency translation or down conversion techniques. The Y factor technique relies on an accurate known noise power and the change in the noise power as measured on a power meter or spectrum analyzer. Unfortunately, the level of noise power, although accurately known, is small. Therefore, additional gain is required for measurements. In this paper a technique is outlined which provides this capability by utilizing the actual device under test in a pair of cascade arrangements. The required gain is provided by the devices under test taken in pairs and cascaded in two sequences. Then application of the cascade formulation of noise power permits deembedding the devices noise under test and obtaining the noise factor of each.

7. Sections 4.4.2 and 5.1.3

Stable tuning of oscillators over a broad frequency range while contending with circuit parasitics is addressed in this work. We recognize prior to device limiting, that the input reflection coefficient of the active device may be modified and directed on the reflection plane in an appropriate manner. This form of active device modification permits successful absorption of circuit parasitics. Additional development is addressed in Section 4.4.2.

8. Section 4.4.7

This section emphasizes the need for electromagnetic (EM) and harmonic balance (HB) co-simulation methodology. A design flow presented integrates both techniques. The tie between simulation and measurement, particularly the tuning characteristics as influenced by the unintentional EM consequence of coupled lines and pads, is emphasized. In addition, the unloaded and loaded oscillator Q measurement and the inference of their measurement via oscillator phase noise is detailed in Section 4.4.8.

1.6 Summary

In this chapter we presented the groundwork and the argument for pursuing an alternative approach to the microwave transmit function. The core of the motivation is two fold: one, reduced circuit function complexity; and two, improved efficiency. Chapters 2 through 4 and the appendix focus on the tools necessary to evaluate various architectures. In addition, the ideas of direct carrier launch will be analyzed and contrasted against other system solutions. Our focus is to permit the realization of a direct carrier launch system and compare performance attributes with those of a heterodyne system as an example. Therefore to this end, discussion of the design and analysis of power amplifiers and power oscillators is developed. In the last half of the dissertation, Chapters 5-7, we discuss details of several circuit implementations and case studies which apply methods of synthesis for FET power oscillators developed in this

dissertation. The power oscillator including BST varactor, Si-GaN FET, and implementation in a phase locked multiplier architecture are highlighted.

Circuit synthesis concentrates on the power oscillator design with emphasis on efficiency and the ability to realize an acceptable tuning frequency range. Our primary focus is in the application of high voltage components. The ability to realize acceptable performance for a microwave transmit function whereby peak RF voltages are substantial is key. The application of the phase lock technique is key to the direct RF carrier launch mechanics. In this dissertation we will present a number of unique aspects to the high breakdown voltage components used and in particular their operation in the phase lock system.

Chapter 2

Investigation of Architectural and Specific Circuit Functions

2.1 The problem definition

The focus of the design effort in microwave transceivers is to cost effectively and efficiently meet target RF specifications for link range and data throughput. As highlighted in Chapter 1, several aspects of the design phase continue to challenge first time design success. The motivation in this section is to contrast the direct carrier launch technique applied in an open loop cascade scenario vs. one with both cascade plus feedback as applied in the phase lock loop and specifically a phase lock multiplier (PLM). Direct carrier launch which minimizes the number of translation stages with filters, gain, and sources is accomplished with two or more sources and a single mixer. Obtaining sufficient output power would then require a power amplifier with appropriate linearity. One issue with this approach is restricted agility due to mixer spurious and subsequent filters to meet the required bandwidth at microwave frequencies. Another less obvious issue is the ability to meet the required signal-to-noise ratio (C/N_o) including spurious signals. Therefore, the cascade network design challenge in transmitter design, and specific to a direct carrier launch technique, is the dual to receiver design. We

find that the design challenges experienced in the development of receiver architecture are very similar to those seen in transmitter architectures. This is particularly true in meeting a specified dynamic range. In this chapter we investigate various noise processes in the heterodyne architecture and contrast this to a feedback arrangement as used in the PLM which is more fully developed. Considerations of spurious tones, modulation of the loop, microphonics, power oscillators, which are phase locked, and the fundamentals of resonator design for oscillators are addressed.

Again, measurements are key to developing validation against theory. Details of the measurement of the BST varactor capacitance, Q , and noise, are provided. In order to handle high operating voltages which are applied to the BST varactor, a special purpose bias tee is developed. Since the bias tee is an in-circuit network which is part of a calibration sequence, it is assumed that this bias tee remains impedance stable with the application of high voltage. Impedance stability of the bias tee is not necessarily the case and this is focused on Section 7.1.

2.2 Heterodyne and homodyne approaches and concerns

In this section we review some of the fundamental system design problems associated with both the heterodyne and the homodyne architectures. Management of carrier signal level, noise level and the processing of signal and noise are addressed. Then the details of the distinctive types of noise are discussed. These various types of noise include AM, PM and their composite, or pure noise which propagates through the system blocks. Depending on the circuit function and operation, each type of noise must be managed differently. Similarly, the action of each system block with single and multiple signals at the input is considered. The overall performance of the system is then monitored in terms of the signal-to-noise ratio and the influences of the chosen system architecture.

Multiple conversion systems applied in the heterodyne approach which shifts higher performance functions to lower frequencies are considered. The aim is to find an architecture that lowers power consumption, cost, and complexity. Unfortunately in the process of heterodyning,

problems arise from the mixing of multiple clock sources. In addition to the mixing problem, linear networks may eventually operate in a nonlinear region. Increased signal levels, relative to the DC quiescent values, partly determine the likelihood of nonlinear operation. Thus complex modulation systems require the addition of automatic gain control (AGC) to be applied to small signal networks to maintain the necessary degree of linearity and meet the distortion requirements. The problem of spurious signals and crosstalk is firstly a linear algebra problem [55]. As the number of sources (n, p, \dots) increase, the ability to eliminate unwanted signals in the channel f_o and the potential for a viable frequency plan, decrease. Given multiple sources, the problem is to minimize, below an acceptable level, all signals that satisfy $j \cdot f_n \pm k \cdot f_p \pm \dots = f_o$ where j and k are integer harmonic components of the signals f_n and f_p . In addition to extraneous signals not occupying the channel frequency f_o , they must not occur within an operating channel bandwidth, given by $j \cdot f_n \pm k \cdot f_p \pm \dots = f_o \pm (\Delta \cdot f_o)$, where $\text{BW} = \Delta \cdot f_o$ and Δ is given as a fraction of the operating frequency, f_o . For point-to-point communications at microwave frequencies a Δ of 0.1, or a BW of 10% of f_o , is typical. Each of the occurrences of an unwanted signal at or near f_o has a unique set of associated coefficients j, k, \dots . In addition, the “sign” of the coefficient term defines the direction that the unwanted signal will move with respect to the corresponding source frequency in the frequency domain, while the magnitude of the coefficient determines the rate, $j \cdot \text{Hz/Hz}$. Consequently, these undesired or false signals, or spurious signals, have specific identities and associated terminology such as $\frac{1}{2}$ IF, image, $m \cdot n$ order, intermodulation, and cross modulation [56]. The source of a given spurious signal and its interference is not restricted to a single circuit function. For example, in a transmit only function whereby a local oscillator is applied to an up-conversion mixer and mixes with a multiple of the same oscillator there is crosstalk among several different circuit functions. It is not unusual for lower frequency baseband sources and microprocessor system clocks to up convert to the RF carrier frequency. Also digital counters, which operate as sampling systems, create low frequency components from a set of high frequency clocks. The design solution to mitigating these false signals is both electrical and mechanical. The process of chartering

a frequency plan is analogous to noise and distortion analysis in cascaded systems. Existing graphical and analytic tools are available to the designer, however, appropriate trade-offs in the design of each architectural approach are driven largely by experience.

Discrete spurious signal interference is one troublesome element. Noise is a second cumbrance. Amplitude and phase noise degradation in a multi-cascade system is both bandwidth limited and signal level dependent [57]. In addition, noise in cascade systems is both additive and multiplicative. Early work on noise in systems treats the modification of noise power by amplifiers and frequency translation circuits, i.e. mixers [25]. The treatment of noise in mixers is somewhat more complicated compared to amplifiers where noise power is additive. In mixer operation we require the multiplication of two input signals to produce an output. Consequently, we must process two noise voltages to observe the signal-to-noise power of the final composite signal; one noise voltage associated with the RF carrier, and a second from the LO. In this chapter we treat the signal and noise properties of amplifiers first, then we consider mixers, followed by the discussion of frequency multipliers and counters. All these active elements are major parts of either an RF cascade or a cascade-feedback system. Fundamental to this discussion is the need for signal and noise values to be expressed in terms of a set of quadrature components and in the presence of signal levels or RF excitation at varying input power level. The motivation here is driven by the manner in which active networks process signals and noise under both small and large signal regimes. For example, if a limiting function is present or an amplifier is overdriven, amplitude variations are suppressed. Mixers, depending on the nature of the input signals, will have the output signal level sensitive to amplitude, phase, or possibly both of the variations of the input signals. Frequency multipliers are insensitive (for the most part) to amplitude change above a threshold point [59]. Mixer networks must consider signal leakage terms or port-to-port isolation in addition to noise voltages. Since two signals are present at two of the three ports of a mixer, signal cross coupling occurs. The LO-RF tone, present in transmitter up conversion and the LO-IF tone, applicable in a receiver down converter, result in spurious coupling, and are the most problematic in generating additional

spurious mixing products. The convention in an up-conversion system, the focus in this work, applies the input signal $x(t)$ to the IF port and the LO signal, $LO(t)$, to the LO port. The output signal $y(t)$ is available at the RF port. Leakage of the LO signal to the IF and RF ports exists. At the RF port this leakage contributes to an undesired spectrum at the output and is characterized by LO-to-RF port isolation [63, 64]. Now in addition to the desired up-conversion signal, the post amplification processes multi-tone inputs, and is particularly an acute problem in wideband systems. The power compression characteristics of the amplifiers which follow, therefore, must be designed accordingly if used in a wideband system, otherwise narrow bandwidth tracking filters must be employed. A summary of functional blocks to be

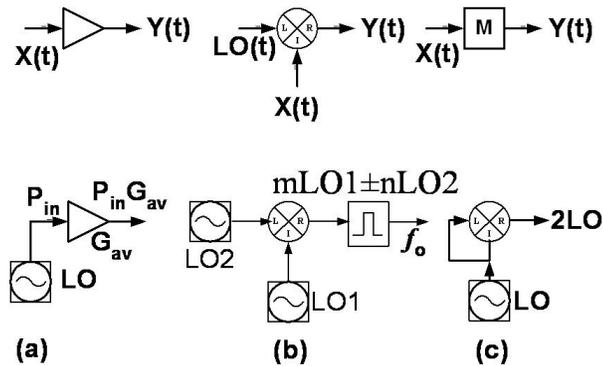


Figure 2.1: Functional blocks in an RF front end system: (a) amplifier, (b) mixer and (c) multiplier functions.

investigated is given in Figure 2.1.

This section discussed several of the requirements of cascade system blocks to meet the technical objectives of an up-conversion transmitter function. The specific up-conversion architecture that was addressed was the heterodyne architecture. Therefore, the complication of spurious signal generation, by multiple terms of signals via mixing, both desired harmonics and

undesired by cross signal terms and by unintentional coupling and signal leakage were highlighted. The processing of noise and noise in the presence of signals was just touched upon and is the main topic of the next section.

2.3 Network noise analysis: introduction to AM, PM and pure noise

The focus of this section is the processing of signals and noise in a cascade system consisting of amplifiers and mixers. This is followed by considering the similarities and differences of noise power in systems employing feedback, such as in the phase lock multiplier architecture. The management of the signal-to-noise ratio and the desire to maintain a minimum required dynamic range is central to the discussion, before embarking on the exploration of other architectures. In this section, we find it is advantageous to distinguish the so called pure form of noise. The pure form of noise is defined here as a random process, perhaps RF noise, whereby the distribution is equally partitioned between processes which are both amplitude modulated (AM) and phase modulated (PM) in origin.

The noise power associated with a specific circuit is a function of both signal level and circuit topology. The no-signal noise figure description of cascaded system blocks is insufficient to describe noise performance. Network system analysis of cascaded systems must permit the calculation and description of the noise power in terms of operating signal level and the composition of the noise. We must distinguish the makeup of noise from origins which are either the result of random fluctuations of amplitude, or random fluctuations of frequency or phase.

2.3.1 The amplifier noise model

First consider an amplifier. The time domain expression $x(t)$ for a single signal plus noise is

$$x(t) = A \cdot \sin(\omega_o t) + n(t), \quad (2.1)$$

where A is the peak amplitude of the signal voltage, ω_o is the RF carrier frequency, and $n(t)$ the noise voltage amplitude. The noise bandwidth and frequency are assumed to be much less than the RF carrier frequency, and the input noise amplitude $n(t)$ is much less than the carrier amplitude A . A more precise definition of this somewhat “generic” form for a single signal plus noise should include a description of both the amplitude and phase perturbations of the carrier explicitly. Therefore, a more precise definition of a carrier signal with noise needs to incorporate carrier amplitude and frequency (or phase) perturbations. In general, the noise signal $n(t)$, includes small spurious coherent signals. The same would apply to the amplitude and phase term of the signal. Finally, we will consider the amplitude of the carrier signal to be *small* relative to the device’s quiescent operating point. Then a time domain signal plus noise description becomes

$$x(t) = A_o \cdot \sin(\Omega_o t + \phi(t)) + n(t) . \quad (2.2)$$

Recognizing the perturbation of amplitude and phase due to the noise term $n(t)$, this becomes

$$x(t) = [A_o + \Delta x(t)] \cos(\Omega_o t + \phi_o(t) + \Delta\phi(t)) . \quad (2.3)$$

Hence the corruption of the carrier signal by noise is described by a random fluctuation of the amplitude and phase. The long-term mean value of the amplitude and phase fluctuations of the carrier are zero, therefore, $\overline{\Delta x(t)} = \overline{\Delta\phi(t)} = 0$. With the amplitude and phase fluctuations normally small with respect to the carrier, (2.3) is approximated as a complex phasor given by

$$x(t) = \text{Re} \left(A_o e^{j[\phi_o(t) + \Delta\phi(t) + \Omega_o(t)]} \right) . \quad (2.4)$$

Here $A_o e^{j[\phi_o(t)]}$ is the complex phasor of the carrier with carrier frequency $\Omega_o(t)$. The noise band about the carrier frequency is small. If the noise band is translated to baseband by a noiseless linear frequency translation, then this band of noise is observed on a low frequency spectrum analyzer, i.e. at an intermediate or IF channel. We will assign the translated frequency band of noise a designation given by $\omega_o(t)$. The noise term is conveniently written as a set of components

that describe the amplitude and phase disturbances of the original carrier term as

$$n(t) = n_x(t) \cdot \cos(\omega_o t) + n_y(t) \cdot \sin(\omega_o t). \quad (2.5)$$

The noise voltage is expressed as a sum of orthogonal terms and is a representation of a random process $n(t)$. This is also expressed as a noise power in the frequency domain and is the sum of the orthogonal components given as

$$N(\omega) = N_x(\omega) + N_y(\omega). \quad (2.6)$$

Substitution of (2.5) into (2.1), collecting terms, using trigonometric identity and the small angle rule for sin and cos functions yields $x(t)$ in a form that is amenable to analysis of linear systems with noise given as

$$x(t) \approx A \cdot \sin\left(\omega_o t + \frac{n_x(t)}{A}\right) + n_y(t) \cdot \sin(\omega_o t). \quad (2.7)$$

Again, application of a trigonometric identity to (2.7), and using the amplitude relation of $\sin(\omega_o t)$ and $\cos(\omega_o t)$ for $\omega_o t$ bounded between 0 and 1, permits $x(t)$ to be written as

$$x(t) \approx A \cdot \left(1 + \frac{n_y(t)}{A}\right) + \sin\left(\omega_o t + \frac{n_x(t)}{A}\right). \quad (2.8)$$

In (2.8) the amplitude and phase noise terms are distinct. The quadrature components responsible for AM and PM noise are separable and operate distinctly in cascade block analysis. Through separation of the noise contributions, a more appropriate expression for noise figure would consist of an AM and a PM component. We contrast this to pure noise where no distinction between AM and PM noise is made. Unlike pure noise measurements, AM and PM noise are conveniently measured by frequency translation of the noise spectra to baseband. In the translation to baseband frequency, the carrier term is eliminated and the noise terms which remain are those which modulated the carrier in amplitude and phase at the carrier frequency.

Therefore, the measurement at baseband is a view of the Fourier line spectra, termed the Fourier frequency, and is composed of the carrier term plus modulation. The Fourier frequency or radian frequency, (ω_m), is also called the offset frequency, sideband frequency, modulation frequency, and finally baseband frequency. At baseband, the noise power measurement is referred to in the *Fourier frequency domain* and may be expressed as either a signal-to-noise power ratio or as is customary, the inverse, a noise-to-carrier power ratio value with units, dBc/Hz, a negative quantity. Phase noise is the term most widely used to describe the characteristic randomness of frequency stability, and as such, the purity of the signal is a measure of the carrier signal power to the power generated in adjacent sidebands. Measurements of phase noise and AM noise are performed in the frequency domain using a spectrum analyzer that provides a window following the detector, a mixer. Frequency stability can also be measured in the time domain with a gated counter that provides a time window providing fluctuations of the carrier period. Because time-frequency relations are tied via a Fourier transform pair, we address the frequency domain measurements of fluctuations of phase and frequency in relation to a particular Fourier frequency. These Fourier frequency or sideband frequencies relative to the carrier, will be uniquely tagged to the corresponding fluctuations of the carrier signal as observed in the time domain. The representation of these fluctuations in the frequency domain is called a spectral density graph, whereby the graph is a distribution of power variance versus frequency.

In particular, when addressing the phase noise of a carrier signal, due to the introduction of random phase modulation of the carrier, reference is made to the single sided noise spectral density. This is the value of noise power, either at the carrier frequency or after frequency translation to baseband, at an offset frequency, f_m , relative to the power at the carrier frequency. Inspection of the noise power in a 1 Hz bandwidth, taking just one side of the carrier, in relation to the carrier power, leads to the definition of $L(f_m)$. Although the noise power after frequency translation is double sided, corrections are applied to the measured value, so as to obtain a single sided value. This noise power as provided by a measure of $L(f_m)$, when measured in

the frequency domain, is a measure of phase fluctuations of the carrier signal. As such, these measurements are again referred to as measurements in the Fourier frequency domain, to stress that these measurements are either single sided frequency, or measured at baseband frequency, at an offset frequency from the carrier of f_m Hz. Additional details in the application and origin of $L(f_m)$, abbreviated herein as $L(f)$, are reserved for Appendix F.

The phase noise measurements, also permit the ratio of noise power to carrier power, to be converted to an equivalent PM or AM noise factor. The phase modulation noise figure term is,

$$\text{NF}_{\text{PM}} = L_{\text{flat}} - (-177) + (P_{\text{IN}})_{\text{dBm}} \quad (2.9)$$

where L_{flat} is the PM noise level in the flat region of noise spectra as measured in the Fourier frequency domain. It is the noise floor of the device measured in units of dBc/Hz where P_{IN} is the device input power in units of dBm, NF is the noise figure in units of dB, and -177 is the room temperature thermal noise in a single-sided noise band with units of dBm. The trend line for this relationship is an increase of the measured spectral density of phase noise is accommodated by a reduction in the input power. The net result of this measurement is a decrease in PM noise figure which approaches the small signal noise figure or the zero signal noise figure. Conversely, a decrease in the measured PM noise figure would require an amplifier that would tolerate a larger signal input with no significant shift in the $L(f)$ value. This shift in $L(f)$ is a consequence of nonlinear intermodulation within the amplifier, either the noise sources mixing with the signal drive, or cyclostationary time variance of noise sources with signal excitation [72, 73]. Conversely, with zero signal input, and with the amplifier input terminated, and with equal noise contribution of both AM and PM noise; the amplifier total output noise power in the frequency domain is given by:

$$N_{\text{out, AMP}}(\omega) = F \cdot G_{\text{av}} \cdot k \cdot T \quad (2.10)$$

where k is the Boltzmann constant $k = 1.38 \cdot 10^{-23}$ J/K, G_{av} is the amplifier available power

gain, T is the noise temperature, and F is the numeric noise factor of the amplifier obtained from the small signal noise figure of the amplifier. From (2.6) the total output noise power is expressed as the sum of the power of its orthogonal components. Each of these orthogonal components, expressed in the time domain, permits the total amplifier output noise power to be expressed in the time domain. Therefore, we have,

$$N_{\text{out, AMP}}(t) = N_{y,\text{AMP}}(t) \cdot \sin(\omega_o t) + N_{x,\text{AMP}}(t) \cdot \cos(\omega_o t) \quad (2.11)$$

with AM and PM components $N_{y,\text{AMP}}(t) \cdot \sin(\omega_o t)$ and $N_{x,\text{AMP}}(t) \cdot \cos(\omega_o t)$. Referring to (2.10) and the desire to separate the AM and PM noise power terms into equal components, we have the output noise of the amplifier alone as

$$N_{y,\text{OUTAMP}}(\omega_o) = N_{x,\text{OUTAMP}}(\omega_o) = \frac{1}{2} \cdot F \cdot G_{\text{av}} \cdot kT. \quad (2.12)$$

Hence, half the total noise power is contributed by fluctuations in signal amplitude, and half by fluctuations in phase. Therefore, in the treatment of the noise figure of cascaded stages, it is prudent to classify the noise type since the reference noise level of the cascade must be adjusted accordingly. The case of equal types of noise power contributions would utilize -174 dBm as the reference noise level.

The input signal plus noise voltage from (2.7) is added to the noise voltage of the amplifier using (2.11) and applied to the input of the amplifier. Using the condition for the noise output power from (2.12), the signal plus noise output voltage is found and put into the form of (2.8) after using the same approximations and gives

$$N_{\text{AMP_OUT}}(t) \approx \sqrt{G_{\text{av}}} \cdot A \cdot \left(1 + \frac{N_y(t) + N_{y\text{AMP}}(t)}{A} \right) \cdot \sin \left(\omega_o t + \frac{N_x(t) + N_{x\text{AMP}}(t)}{A} \right). \quad (2.13)$$

As an example, consider an amplifier with a noise equivalent bandwidth of 100 MHz processing a signal at an input power of 0 dBm with noise figure of 7 dB. Normalized to a 1 Hz bandwidth,

the amplifier will provide an output signal-to-noise ratio of 167 dBc/Hz. If the source is limited in amplitude such that no AM noise is present (e.g. the amplifier is a limiter network removing amplitude noise variations), then the noise floor is appropriately modified to -177 dBm/Hz and the signal-to-noise ratio is 170 dBc/Hz. If the expression instead is referred to as the noise-to-carrier ratio, the values are accordingly negated. In (2.13) we note that the noise power output increases with amplifier available gain, and increasing amplifier noise figure. Therefore, a minimal amplifier noise power contribution is achievable at high gain so long as the noise figure is maintained. Conversely, one would like to achieve this gain without the affects of saturation. Large power gain, small noise contribution, and no compression translate into amplifier design requirements for high dynamic range. If an approach to realizing high power oscillator were to simply add a high power amplifier after the oscillator, this issue of amplifier dynamic range in the context of noise power and maximum achievable compression power is different. Now there is a need to consider the large signal noise figure and the required trade-off of oscillator noise, signal power, and coupling factor, between the oscillator and the amplifier for a specified total noise-to-carrier ratio. A term introduced earlier and again in latter sections is the spectral density of phase noise. The terminology is particular to oscillators but certainly appropriate for all networks in treating the signal-to-noise ratio. One form of definition for the spectral density of phase noise is

$$S_{\Delta\theta} = FkT/P_{s, av} . \quad (2.14)$$

This expression is directly related to $L(f)$ as the spectral density of phase noise is a function of random phase modulation, $\Delta\theta$, which is limited to the device noise floor, kT , plus the device noise factor, F . Relative to the available carrier signal power, $P_{s, av}$, this is the noise-to-carrier ratio. Here, k is Boltzman's constant, T device temperature in degrees Kelvin, and the carrier power, P_s , is expressed in watts.

2.3.2 Frequency translator noise model, mixer and variations

Mixer analysis needs to go beyond the signal and noise terms expressed in (2.1) and (2.5) which were developed for the amplifier model. The mixer model description must extend beyond the two-port model of the amplifier as multi-signal operation is inherent. The model must handle leakage and cross talk terms which exist among three signals. These terms will be expressed in the same form as (2.1) and (2.5) however, in addition, correlation exists among the sources of noise. In an ideal situation, a shift in the carrier frequency with small phase or amplitude fluctuations is simple. If we assume that the mixer is quasi-linear and the local oscillator (LO) is ideal and noise free, then the noise spectra of the input signal is shifted in frequency. We also assume that the mixer is noise free and provides no noise contribution. It follows that the output phase noise of the mixer would be equal to the input phase noise as a function of time and would be independent of frequency. From this we would conclude that the corresponding power spectra are also equal. Under the assumption of quasi-linearity of the mixer, any amplitude fluctuations will also be linearly transposed in frequency. Now consider the case where the contribution of noise from the LO is present. AM LO noise is not considered in this discussion. As we shall see, this is a reasonable assumption for the self-limiting class of oscillators. Furthermore, assume that the phase noise of the LO is *not* correlated with other signals. Then the phase noise of the output converted signal at the RF channel is the sum of the oscillator phase noise and the IF input phase noise or, $PM_{\text{mixer}}(f_{\text{RF}}) \approx PM(f_{\text{IF}}) + PM(f_{\text{LO}})$. In a real mixer however, noise is replicated and translated by each harmonic of the LO and the LO leakage, resulting in correlations at frequencies separated by $k \cdot f_{\text{LO}}$ [74, 75, 76, 77]. The LO leakage signal is expressed as

$$LO_{\text{leakage}}(t) = \sqrt{LO_{\text{leakage}}} A_{\text{LO}} \sin \left(\omega_{\text{LO}}(t) + \theta_{\text{LO}}(t) + \frac{n_{x\text{LO}}(t)}{A_{\text{IF}}} \right) \quad (2.15)$$

where LO_{leakage} is the mixer LO to RF output port leakage factor. The context is no different than (2.13). That is to say, the relative signal leakage or output noise level is proportional to

a ratio of signal amplitudes. In the case of an up-conversion mixer, the relative ratio is the level of the LO signal to that of the IF signal. The loss or isolation of the LO voltage to RF port output is proportional to $\sqrt{LO_{leakage}}A_{LO}$. Finally, the noise-to-carrier ratio of the mixer output port is directly proportional to the ratio of the LO PM noise level to the LO signal power. The translation mixer is unique, in the sense that the LO signal level and spectral content establishes the carrier-to-noise ratio at the up-converted RF port. However, at the same time, the LO signal represents a corruptive component and a spurious signal in the final context of the intended architecture.

In cascade and feedback analysis it is convenient for the total output signal plus noise voltage to be referred back to the amplifier input. Again, frequency domain descriptions of noise power can be expressed in the time domain and visa-versa. From (2.6) and (2.12) the AM and PM noise power terms are distinct. Then using (2.13) the noise powers in the frequency domain with Fourier offset frequency f are written as

$$AM_{amp}(f) \approx \left(\frac{1}{A^2}\right) \cdot \left(N_y(f) + \frac{1}{2} \cdot NF \cdot k \cdot T\right) \quad (2.16)$$

and

$$PM_{amp}(f) \approx \left(\frac{1}{A^2}\right) \cdot \left(N_x(f) + \frac{1}{2} \cdot NF \cdot k \cdot T\right) \quad (2.17)$$

respectively. The up-converting mixer analysis requires the product of the LO voltage, $LO(t)$, and the signal voltage, $x(t)$, which is the IF signal. Products are identified in the time domain at the output, $y(t)$ at the RF port. First the LO signal is defined as

$$LO(t) \approx A_{LO} \cdot (1 + n_{y,LO}(t)/A_{LO}) \cdot \sin(\omega_{LO}t + \theta_{LO}(t) + n_{x,LO}(t)/A_{LO}) \quad (2.18)$$

and the IF signal as

$$x(t)_{IF} \approx A_{IF} \cdot (1 + n_{y,IF}(t)/A_{IF}) \cdot \sin(k \sin \omega_{LO}t + k\theta_{LO}(t) + n_{x,IF}(t)/A_{IF}) . \quad (2.19)$$

The voltage amplitude of the signals are designated by A and A_{CG} where A_{CG} is defined as the mixer conversion gain and A_{CG} may be less than unity. Following the amplifier study, subscripts x and y refer to the phase and amplitude noise terms. In actual mixers, the IF signal and the LO signal are correlated provided the LO signal is free of amplitude or phase modulation introduced by other signals. The IF input signal frequency and the phase term carry a k multiplier term to identify that the IF input and the LO signals are k multiples of each other. The up-converted RF port signal voltage is obtained after multiplication of (2.18) with (2.19). The output signal $y(t)$ at the RF port will carry this same set of correlation terms due to the relationship of the LO PM noise and the LO signal frequency. The conversion gain provides a measure of the ratio of the up-conversion signal voltage at the RF port referenced to the IF port, A_{CG} . This conversion gain or loss is a function of the LO amplitude A_{LO} . Multiplication, collection of terms, simplification for small quadratic values, and use of the small angle rule gives the up converted output RF signal voltage as,

$$y_{\text{mixer}}(t) \approx \sqrt{A_{CG}} \cdot A_{\text{IF}} \cdot ((1 + n_{y,\text{IF}}(t)/A_{\text{IF}})) \cdot \cos(\gamma) \quad (2.20)$$

with $\gamma = ((1 + k)\omega_{\text{LO}}(t) + (1 + k)\theta_{\text{LO}}(t) + n_{x\text{LO}}(t)/A_{\text{LO}} + n_{x\text{IF}}(t)/A_{\text{IF}})$. Several observations are in order. With large amplitude LO voltage, the up-converted noise is reduced. The same is true of the IF signal. This assumes the noise factor of the mixer does not degrade with increased LO voltage. There is multiplication of the frequency and phase noise terms as a function of the value of k , and noise voltage will increase in the up-conversion case. The $(n_{y\text{LO}}(t)/A_{\text{LO}})$ AM noise term is dropped from (2.18) as the mixer will compress the LO signal at large LO levels. Although as the LO level increases, the benefits of increased LO voltage are offset as the LO leakage term becomes a limiting factor. In many cases it is the LO leakage level that is dominant over the noise power or distortion introduced by the mixer. A reference to a few RF network systems demonstrate the condition where the impact of leakage is a concern including transmit and PLL architectures, see Figure 2.2. Using the description of the mixer signal and noise model in the time domain and including the LO leakage, the frequency-domain power will

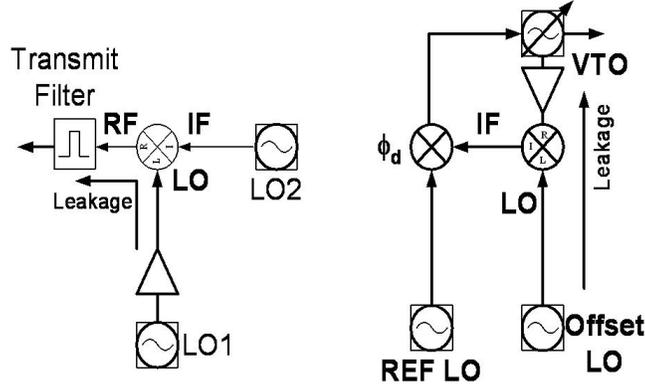


Figure 2.2: LO leakage in mixer based architectures, direct carrier and offset PLL transmit

include three terms: AM noise, PM noise associated with the IF, and PM noise associated with the LO and the LO leakage. From (2.15) we find that the phase noise at the RF output port, PM noise, is partly due to the LO leakage of the mixer given by

$$PM_{LO_LEAKAGE}(f) \approx \left(\frac{LO_{leakage}}{A_{GC}} \right) \left[\frac{A_{LO}^2}{A_{IF}^2} (\theta_{LO}(f)) + \frac{N_{xLO}(f)}{A_{IF}^2} \right]. \quad (2.21)$$

The contribution of the LO leakage to the output phase noise as well as to the spurious power of the signals is reduced as the conversion gain is increased (loss reduced) and as the IF signal level increases. However, this comes at a cost in mixer linearity and potentially greater ($m \cdot n$) spurious signals. In addition to the LO leakage and the PM noise associated with it, there are three other noise power terms at the output: the AM and PM noise of the IF signal, multiplication of the LO phase deviation correlated with the IF noise, and the PM noise of the LO that is not correlated. The total up-converted noise power at the RF port is the sum of all terms. The noise power is displayed in the frequency domain and measured at a Fourier offset from the LO carrier. In a practical sense, at RF offsets equal to or greater than the LO offset, the noise power is flattened at the mixer RF output. The noise power that remains is the thermal noise of the LO. Normalizing each of the noise terms to their signal amplitudes

gives the following:

AM and PM noise at the mixer RF port due to IF noise are

$$\text{AM}_{\text{mixer}}(f) = N_{y,\text{IF}}(f) / A_{\text{IF}}^2 \quad (2.22)$$

$$\text{PM}_{\text{mixer}}(f) = N_{x,\text{IF}}(f) / A_{\text{IF}}^2. \quad (2.23)$$

The PM noise at the mixer RF port due to LO noise is

$$\text{PM}_{\text{mixer}}(f) = N_{x,\text{IF}}(f) / A_{\text{IF}}^2 \quad (2.24)$$

and the PM noise at the mixer RF port due to LO leakage noise, (2.21) is repeated here for convenience,

$$\text{PM}_{\text{mixer}}(f) = \left(\frac{LO_{\text{leakage}}(f)}{A_{\text{GC}}} \right) \left[\frac{A_{\text{LO}}^2}{A_{\text{IF}}^2} (\theta_{\text{LO}}(f)) + \frac{N_{x\text{LO}}(f)}{A_{\text{IF}}^2} \right]. \quad (2.25)$$

The mixer power output noise spectrum consists of multiplied phase noise of the LO and of the LO leakage signal. Reference to (2.24) shows correlated LO noise power increasing with $(1+k)^2$ in an up-conversion mixer while other uncorrelated PM noise terms are additive. A frequency multiplier is configured from a mixer where both the LO and IF ports are driven in parallel. The up-converted signal at the RF port is a doubled version of the input. For $k=1$, the output signal is obtained from (2.20) with γ evaluated for $k=1$. We have

$$y_{\text{mult}}(t) \approx \sqrt{A_{\text{CG}}} \cdot A_{\text{IF}} \cdot [1 + n_{y,\text{IF}}(t) / A_{\text{IF}}] \cdot \cos \{ 2 [\omega_{\text{LO}}(t) \theta_{\text{LO}}(t) + n_{x,\text{LO}}(t) / A_{\text{LO}} + n_{x,\text{IF}}(t) / A_{\text{IF}}] \} \quad (2.26)$$

and frequency and phase noise are doubled while AM components remain the same. The PM noise rises by the square of the multiplier factor since the phase noise multiplier factor appears inside the argument of the sinusoidal time domain signal. The power spectrum in

the frequency domain results in the PM noise power rising by the square of the multiplication factor, resulting in the $20\log_{10}N$ relation while the AM noise power remains the same, as ideal frequency multiplication maintains a constant modulation index.

The frequency translation process can occur by at least two different methods. The application of the mixer is one, the frequency multiplier another. Both approaches must contend with the potential degradation of noise and the introduction of signal spurious. While the frequency multiplier is a subset of the mixer translator and the main attention is phase noise degradation, a real frequency multiplier is a nonlinear device and may multiply AM sidebands. However, if the multiplier is permitted to saturate, the multiplier can suppress AM affects. This is acceptable, as long as harmonic content of the output signal does not increase. Upon normalizing the signal power to the noise power as before, and with the LO port signal much larger in amplitude than any of the LO harmonics, and upon application of the LO signal to both the LO port and the IF port, we yield the PM noise of the multiplier as

$$\text{PM}_{\text{mult}}(f) \approx N^2 \cdot N_{x,\text{IF}}(f) / A_{\text{IF}}^2(f) \quad (2.27)$$

while the AM noise is

$$\text{AM}_{\text{mult}}(f) \approx N_y(f) / A_{\text{IF}}^2(f) . \quad (2.28)$$

Therefore, as the multiplication factor N increases, so does the degradation in phase noise. A reasonable argument which invariably surfaces is centered on the discussion of how to arrive at the final carrier frequency with the required signal-to-noise ratio, and with minimized spurious signals. The analysis must consider the phase noise of the source, the required multiplication factor, the N and M values as required in the multiplication cascade to arrive at the final carrier frequency, and the cost and complexity of additive filtering functions as they are required. The pure multiplication architectural approach may then be used as baseline to judge a mixer and multiple source approach, and then finally, the direct operation at carrier frequency architecture might be considered. Our approach in this dissertation will focus on the

last. Some key questions, whose answers are partially driven by the technology, are: “What is the comparative signal-to-noise ratio at the final carrier frequency provided by these different techniques?” and, “What is the level of complexity, efficiency, and the cost?”

2.3.3 Noise analysis in systems

AM and PM noise analysis of a cascaded or PLL feedback system is treated in a similar manner to the simpler open system cascade, for example a frequency multiplier. The analysis is not unlike the noise and distortion analysis of the cascade of Figure 1.4, however, the noise factor at large input signal level and signal compression must now be treated. The additive and multiplicative level of noise power, signal output, and compression must all be accounted for in the analysis. A case study of the multiplication of cascaded noise effects in [58, 65, 66] demonstrated that the difference in multiplicative phase noise in an ideal mixer-multiplier configuration was negligible from the prediction for the cascade studied. That is, the multiplicative effect, ($PM_{\text{mult}}(f) = 20 \cdot \log N$), dominated the noise degradation compared to the additive noise effects. However, large signal conditions will alter this result. For example, as previously discussed, the noise figure of amplifiers will increase significantly as the amplifiers are driven into compression. The noise performance is potentially different and dependent on the architecture of the system. While the PM noise in dB of an ideal frequency multiplier is $20 \cdot \log_{10} N$ where N is the frequency multiplier factor, the noise power in a PLL system is found to be a strong function of both additive and multiplicative noise sources. When applied to a transmit up-converter, there are a number of benefits for the selection of a PLM as compared to a cascaded multiply and translation system. A key to PLM operation is the frequency counter. The counter operation as a frequency divider provides signal compression and limiting. Thus AM noise is minimized. In addition, the PM noise is reduced as the modulation index is divided. Again, reference to the PM noise component of (2.8) with an arbitrary input phase is passed through a frequency counter. The arbitrary phase noise term is associated with the additive noise of the counter that is not correlated with the input noise. This analysis gives the time

domain output noise as

$$y_{\text{counter}}(t) = A \cdot \sin(\omega_o t/N + (n_x(t)/N \cdot A_{\text{IF}}) + \theta_o(t)). \quad (2.29)$$

The output phase noise power spectrum is accordingly reduced by the counter value N^2 and is

$$\text{PM}_{\text{counter}}(f) \approx N_x(f)/(N \cdot A_{\text{IF}})^2 + \theta_o(f). \quad (2.30)$$

Consider the subtleties of the signal-to-noise distribution and the cumulative effects in the cascade that are captured in reduction in dynamic range as illustrated in Figure 1.6, and indicated in (2.26) and (2.30). In these specific cases, reduction in dynamic range happens firstly due to amplifier distortion, while if a frequency multiplier were used secondly, reduction in dynamic range would occur due to noise multiplication.

The problem of noise multiplication previously addressed is germane to receiver and transmitter local oscillator cascades and manifests itself in clock distribution systems, in analog-to-digital converters (ADC), and digital-to-analog (DAC) converters in the form of clock jitter. To appreciate the problem, we need to reconsider the cascade of Figure 1.3, this time adding the local oscillator noise power contribution to the cascade. Prior analysis, assumed the oscillator injection source was free of any noise perturbations. In general, noise analysis of cascade systems should state if frequency sources are considered in the noise contribution to the output signal. Mismanagement of this network has consequences in receiver and transmitter opera-

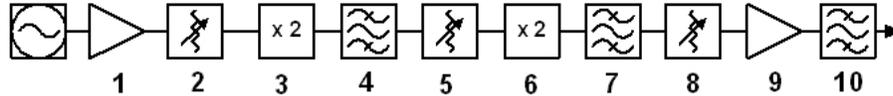


Figure 2.3: Cascade LO and frequency multiply network

tion. The LO chain contains sources, amplifiers and frequency multipliers. Careful distribution

of loss, deliberately distributed in the cascade is necessary to manage gain and severe stage compression. If attenuation is not added appropriately, an increase in noise-to-carrier (N_o/C) occurs. For example, in Figure 1.6, switching stages 1 and 2 and adjusting the attenuator for the same net gain, causes a 3 dB increase in the noise-to-carrier ratio. The consequence of this increased noise in receivers is loss of decode sensitivity, and in transmitters phase noise modulation is added to carrier symbols. An LO chain as described in Figure 2.3, and a breakout of the noise factor, gain, and linearity of each stage is required to assess the placement and value of attenuators. Analysis of the cascade must also consider nonlinearity. Utilization of the intercept method is a convenient and fast methodology for the distortion analysis of cascades. Although it is common to use the third-order output intercept (OIP3) only in analyzing nonlinear performance, however this approach has limited accuracy. There are several issues that introduce error. Specifically OIP3 is normally extrapolated from a set of quite small discrete tone signal measurements and assumes a linear logarithm dependence of third-order distortion on input power. First, characterization is usually accomplished with just two-tones at signal levels far below where the device will operate in an actual system environment. Therefore, the extrapolation accuracy of finding the intersection of the distortion tones with the fundamental tone is limited. Second, the actual modulation is complex, and therefore the degree of circuit function saturation is a better metric. Therefore, the output power compression point or P_{-1dB} is potentially more meaningful and is used here in cascade noise-to-carrier calculations. For the system shown in Figure 2.3, typical of an X-band LO-multiplier cascade, we have the parameters listed in Table 2.1.

This cascade provides a $\times 4$ multiplication with a cascade of two frequency doublers providing nonlinear frequency multiplication. Therefore, these devices are deliberately over driven with sufficient input signal power to permit efficient frequency multiplication. Consequently, post filters are required here, stages 4 and 7. Attenuators are required firstly to assist in maximizing system dynamic range by properly balancing gain and noise power distribution, and secondly to serve as output power control. The gain listed is the available gain, G_{av} , where the available

Table 2.1: 10 stage cascade LO and frequency multiply network of Figure 2.3

Local oscillator frequency multiplier parameters						
stage n	function	gain (dB)	NF (dB)	P_{-1dB} (dBm)	P_{out} (dBm) (dBm)	Compr (dB)
1	amplifier	16	4.5	14	14.4	1.6
2	attenuator	-20	20	20	99	
3	multiplier x2	19	4.5	16	13.3	0.1
4	bandpass filter	-3	3	99	10.3	
5	attenuator	-15	15	99	-4.7	
6	multiplier x2	28	4.5	18	18.7	4.6
7	bandpass filter	-3	3	99	15.7	
8	attenuator	-9	9	99	6.7	
9	driver amplifier	18	4.5	18	18.6	6.1
10	bandpass filter	-3	3	99	15.6	

Note: $P_{in}=0$ dBm, source signal-to-noise ratio = -155 dBm/Hz

gain is defined as the ratio of the available power from the output of a two port to the available power from the source. The available gain is a function of the source impedance. As well, the noise factor of the two port is also a function of the source impedance. Therefore, the available gain covers both facets of key parameters in the system cascade and is the preferred quantity for amplifier characterization [67]. The noise figure includes both components of AM and PM noise, and the compression factor in dB (Compr-dB) is the reduction in dB of the fundamental signal power due to the finite 1 dB compression point of each stage. Therefore, P_{out} represents the cumulative power at each point in the cascade.

The source input power is 0 dBm and the signal-to-noise ratio established by the local oscillator source, the input to stage 1, is -155 dBm/Hz. All stages other than the multipliers and driver amplifiers exhibit little compression. Some compression is desired, however, to the extent that carrier output power remains constant, as this minimizes output power fluctuation with frequency, temperature and input power variations. Careful setting and positioning of attenuators is required. For one, power input to multipliers might be confined to an input power window variation as small as 6 dB, or as much as 20 dB, dependent on the design and topology of the cascade. In the analysis presented, the noise figure and gain are considered

to be constant over the bandwidth of the modulated carrier and any image frequency. This distinction is particularly important to state if there is a mixer present. For simplification, unless there is sufficiently narrow band selectivity, the desired channel gain and image channel gain are assumed to be the same. Although bandpass filters are included in the analysis, the rejection limits are limited to spurious signals of the multipliers as the M^{th} doubler with a multiplication factor of N creates spurious signals at frequencies of $N + 1$ and $N - 1$ times the fundamental. As an example, if the multiplier is a doubler, the fundamental and the third harmonic of the multiplier input are spurious signals at the output of the doubler.

The calculated noise figure of the multiplier cascade described in Table 2.2 is 20.06 dB and is dominated by the noise of the attenuators. However, use of a low noise amplifier (stage 1) at the beginning of the cascade, reduces the change in total cascaded noise figure with changes in attenuator settings. This is key to maintaining a reasonably constant noise-to-carrier ratio with variations in subsequent stage losses. Therefore, in this particular cascade shown in Figure 2.3, the noise power output obtained from the factor $(F - 1)G_{av}$ and including all gain compression is 35.6 dB above the constant white noise level. Consider the gain compression present and the limiting function provided by frequency multipliers. As an example, with the cascade input power set at 0 dBm, the input power to each of the successive multipliers in Figure 2.3, is in excess of 13 and 18 dBm respectfully. This is in fact the required input power for these frequency multiplier blocks, if there is to be no change in harmonic output power and the signal-to-noise ratio is to be maintained in the cascade. This is clear, as Table 2.1 demonstrates the second multiplier is 4.6 dB into compression. These calculations are provided by writing a Mathcad script.

In this cascade, the noise power is dominated by the phase noise power spectrum and should be referenced to a PM noise floor of $kTB/2$. Analysis at lower signal levels would consider both AM and PM noise power or the composite or so called pure noise, in which case the reference is kTB . Consequently the output noise power is -141 dBm/Hz at the stage 10 output.

Consider a complex modulation system supporting a 128 QAM-encoded data packet. Sys-

tems are required to adhere to specific channel operating bandwidths, for example in the range of 14 – 56 MHz. Such a system would dictate a noise equivalent bandwidth of 56 MHz to support an error free data link after decoding when operating at 10 dB carrier-to-noise ratio. If the LO multiplier cascade of Figure 2.4 is noise free and applied to a receiver down-converting mixer operating with 56 MHz IF bandwidth, then the signal level at 10 dB above the minimum sensitivity required for error free decoding is -82.5 dBm for a 4.5 dB receiver system noise figure. However, the noise power associated with the LO applied to the receiver mixer is -64.4 dBm in a 56 MHz bandwidth. Without a reduction of the LO multiplier noise power there is significant sensitivity degradation. As a minimum, an additional noise reduction of 28 dB is required to increase sensitivity by 0.4 dB. An 18 dB reduction in noise power of the LO source would provide an uncorrelated source of noise just equal to the sensitivity noise power level. Then an additional 10 dB is required so as to limit the contribution of noise power from the LO source to just 0.4 dB. This calculation is obtained from the sum of log powers given by $dB_{\text{sum}} = 10\log_{10} \frac{1}{1+x}$ for $x \leq 1$, with $x = 0.1$.

A substantial portion of this noise power reduction typically comes from mixer LO port-to-IF port balance for the case of AM noise reduction and subsequently port-to-port isolation in a balanced mixer. However, additional rejection must come from LO filter selectivity [68]. It should be noted that balanced mixers provide no suppression of phase noise. Furthermore, consider the same LO multiplier cascade applied to a transmitter up-converter and power amplifier as shown in Figure 2.4. A power amplifier is characterized for noise figure at rated

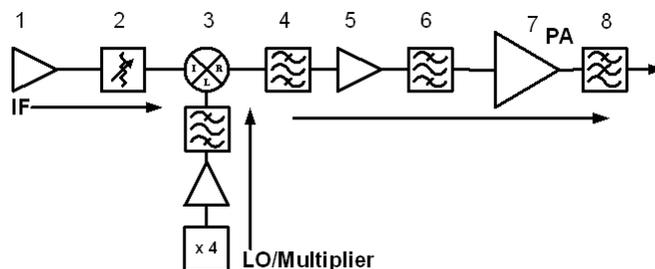


Figure 2.4: Cascade transmitter up converter with LO multiplier of Figure 2.3

output power. Both the up-conversion mixer and driver amplifier are characterized at small signal levels. The system studied provides output at 15 GHz with an LO at 11 GHz and an IF at 4 GHz. The final output noise-to-carrier ratio is contingent on establishing adequate carrier-to-noise ratio at the IF channel. This condition is met by using a low noise IF amplifier utilizing a P-HEMT transistor at 4 GHz. A variable attenuator to control gain follows the IF amplifier so that noise figure and distortion are largely independent of the attenuator settings. The cascade table for this 8 stage system is shown in Table 2.2. Assuming that the broadband LO noise is confined to a carrier offset frequency equal to the IF channel frequency, then the noise-to-carrier ratio is -155 dBm/Hz. If no noise is added by the multiplier cascade, then the transmitter signal-to-noise ratio is -53 dBm/1MHz bandwidth. Conversely, as shown earlier, the LO multiplier cascade adds excess noise of -141 dBm/Hz. Therefore, using this LO-multiplier cascade raises the noise power such that the transmit noise-to-carrier ratio is -45 dBm/1 MHz. An additional 8 dB of either mixer AM LO noise rejection, port-to-port balance, or port isolation is required. Otherwise, LO-multiplier selectivity is needed to reduce PM noise modulation. Any of these approaches are valid solutions and are required prior to frequency up-conversion.

2.3.4 Summary

In this section, the processing of signals, noise, and noise in the presence of large signals was addressed. One focus of this section was to address the impact of multiplication and translation of noise on the noise performance of a cascade architecture. The primary architecture considered used the heterodyne principle and we found that careful control of gain, loss, and noise distribution, is required to meet design objectives. Processing of noise power in the mixer is uniquely differentiated from that of an amplifier. As the mixer is fundamentally a dual signal, dual channel device, there are a number of additional constraints when the mixer is utilized in a system targeted for a single channel application. To treat these devices in a straight-forward manner, representation of the noise by in-phase and quadrature terms was introduced.

Table 2.2: 8 stage up-converter transmitter-PA using the LO multiplier cascade of Figure 2.3.

Up-converter transmitter-PA with LO-multiplier					
stage n	function	gain (dB)	NF (dB)(*)	P-1dB (dBm)	Pout (dBm)
1	IF amplifier	17	1	20	11
2	attenuator	-10	10	99	1
3	up-converter mixer	-9	9	99	-8
4	bandpass filter	-3	3	99	-10
5	PA driver	21	8	25	11
6	bandpass filter	-2	2	99	9
7	power amplifier	21.5	15	30	29.7
8	low pass filter	-0.5	0.5	99	29.2

*noiseless LO multiplier cascade

The need for the careful balance of gain, noise power, linearity and losses, coupled with frequency planning, proper distribution of selectivity, and judicious placement of losses complicates transmitter design. This prompts the designer to consider alternative architectures. The design motivation is to simplify the architecture, provide for the introduction of complex modulation, and prepare for increasing the carrier frequency through up-conversion for microwave transmission. With this simplification a reduction in spurious products and improved efficiency should be possible. An approach which permits integration of the modulation into the same circuit function as the up-conversion process will also lead to further reduction in circuit complexity and power drain. Finally, the application of feedback can lead to improved carrier-to-noise ratio if circuit performance and stage assignments are partitioned properly just as in cascade architectures.

2.3.5 Phase lock multiplier introduction

The cascade transmit architecture, in heterodyne form, typically consists of one principle forward path. Feedback is not always used and if used is usually confined to a local single cascade stage. In this section an alternative architecture is considered which is feedback based. The phase lock system is operated as a frequency translator and the issues of this architecture are contrasted with those of the cascaded heterodyne implementation. Several problematic aspects

of both systems share similarities. For example, spurious signals and noise are present. The use of feedback to reduce their affect on performance is highlighted. In addition, new problems are introduced, which are unique to the phase lock multiplier operation including mechanical vibration induced noise, and these are also addressed. Finally, introduction of unintentional modulation, microphonics, and the reduction of extraneous spurious signals are detailed.

2.3.6 Phase lock multiplier architecture

The new phase-locked multiplier PLM architecture is shown in Figure 2.5. Emphasis is on frequency translation-multiplication, and power amplification via a cascade of phase lock systems. Shown in Figure 2.6, is an N -divider and M -blocks multiplier with mixer, amplifiers, and controlled sources. Remaining elements of the phase lock loop include phase detector K_ϕ , a balanced mixer and a loop compensator $F(j\omega)$. The operating frequency, f_o , is at the final carrier frequency. The architecture employs a self-contained power oscillator or the use of an oscillator power amplifier combination implemented as a master oscillator power amplifier or MOPA. However, while a MOPA is possible, in this dissertation the emphasis is on a single self-contained circuit implementation of a high efficiency power oscillator. Through the successful circuit topology of a power oscillator, the potential system integration of frequency generation, power amplification, frequency translation, and modulation into an integrated system approach is possible. This system approach is emphasized in Figure 2.5. The power oscillator operates in a phase lock condition with feedback controlled by the filter compensator and the phase detector/comparator shown in Figure 2.6. The condition of phase lock requires that the frequency inputs to the phase comparator are identical, and so the power oscillator carrier frequency must be $(N/M) \cdot f_x$. In general for the network shown, an offset and multiply loop is used, therefore $f_o = (N/M) \cdot f_x \pm f_m$. This work focuses mainly on the application of the loop as a frequency multiplier. The addition of the offset loop provides a number of advantages including further improvement in the (C/N_o) ratio, however care in frequency planning is required as frequency translation is introduced via the mixer. The offset portion of the loop represents an example of

a cascade block embedded in a feedback system. The advantages of this additional architecture will be considered as the impact to (C/N_o) is discussed. Noise analysis leading to carrier-to-noise ratio of PLLs is well documented [69], however it is revised in this dissertation to address unique issues to the PLM architecture.

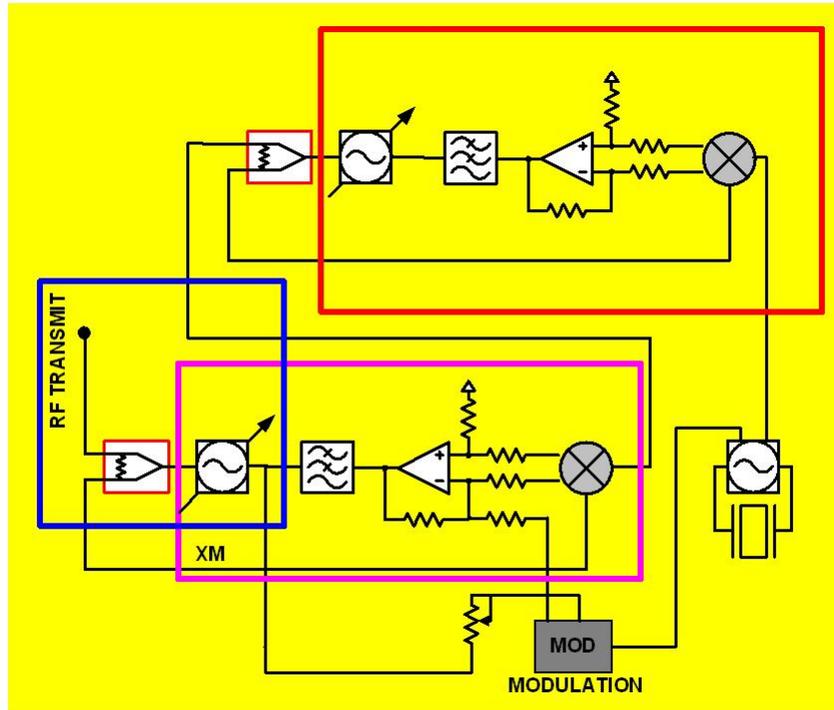


Figure 2.5: The phase locked power oscillator integrates multiple up-conversion transmitter functions.

A significant attribute of the PLM architecture is the placement of cascaded system blocks within a feedback loop. Such flexibility in the arrangement of network blocks permits the possible improvement in operation with respect to spurious signal generation and noise. For example, the phase lock loop implements a lowpass transfer function for a signal input to the phase comparator. However, care is still required in implementation of the architecture and in network block placement. For example, the counter block is able to reduce phase noise for input signals if the counter location is outside the feedback loop. Conversely, one impact of

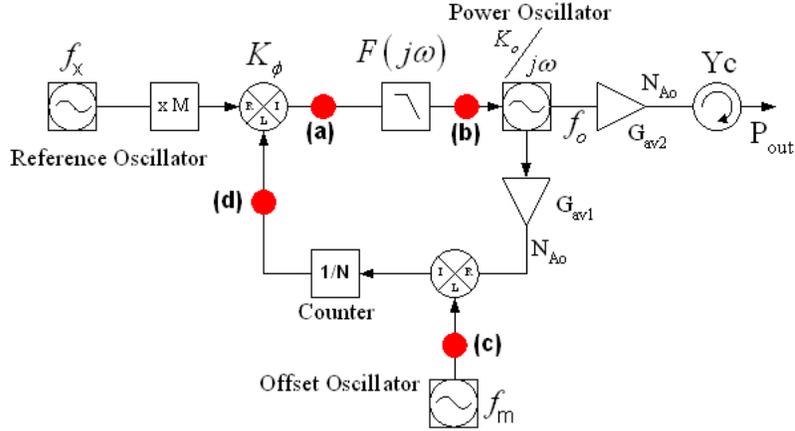


Figure 2.6: A generic PLM architecture including an offset PLL. Points of noise entry (a)–(d) are addressed in text.

the counter while being inside the loop is the multiplication of phase noise. Evidence of this is obtained readily by writing the appropriate phase transfer functions within the loop. Reference to Figure 2.6 demonstrates that if the reference point for measurement of C/N_o is at the output indicated by the carrier frequency f_o , then a noise voltage injected at point (a) will be subject to a lowpass transfer function while noise injected at point (b) will be subject to a highpass response. Several key points of noise injection at locations (a)–(d) are highlighted in Figure 2.6. Each block’s contribution to noise power is assumed to be a small-signal perturbation and the loop remains phase locked. Therefore, the various transfer functions of the loop are found by applying superposition. A generic representation of the PLM architecture will include mixers, frequency counters, and multipliers. In addition, the power oscillator serving the dual role as power amplifier will provide direct carrier launch. Therefore, this architecture bypasses the conventional up-conversion arrangement with frequency sources and power amplifier to accomplish the transmitter function. For direct complex modulation, a means of varying the oscillator amplitude and phase is required. Phase or frequency modulation is introduced within the loop and is compensated to account for impairments caused by loop dynamics. Consequently, the modulation bandwidth of the loop is de-coupled from the loop dynamics so far as the oscillators have sufficient modulation response. Envelope modulation however, must not

appreciably affect the source frequency as the nominal frequency and phase lock are compromised. Therefore, appreciable AM is introduced outside the loop. The use of an isolator after the phase locked oscillator is one method to address the issue of oscillator frequency shift while introducing amplitude modulation. Another, is to constrain the envelope modulation rate less than the loop bandwidth. In this manner, frequency perturbations created by impedance fluctuation from the envelope modulator would be suppressed. Furthermore, if the loop bandwidth is sufficiently wide, and the impedance state of the envelope modulator is constant, this will further reduce perturbations of the oscillator frequency. Introduction of AM outside the loop is not treated in this dissertation and is left for future work.

As mentioned earlier, an important benefit of the loop is the inherent presence of an intrinsic lowpass filter transfer function. The phase lock loop bandwidth is a baseband equivalent of the RF carrier center frequency bandwidth. This bandwidth is under designer control and is shaped as required by the phase lock loop compensator. This is easily seen from the loop transfer function which can be written either in terms of the phase deviation of the signal at points to the left of (a) or in terms of the signal output associated with the VCO (function $K_o/j\omega$). In terms of the phase deviation at point (a),

$$\frac{\Delta\theta_o}{\Delta\theta_i} = \frac{K_\phi F(j\omega) K_o}{j\omega + (K_\phi F(j\omega) K_o)/N}. \quad (2.31)$$

This phase transfer function is valid for small signal perturbations, small enough such that the loop remains phase locked. The oscillator output phase deviation, $\Delta\theta_o$, is a function of the reference source phase deviation, $\Delta\theta_i$. The shape of the frequency response is controlled by the loop open-loop gain of the loop controlled by oscillator function or tuning gain, K_o ; and the counter value, N , and loop compensator, $F(j\omega)$.

Since the transfer function is lowpass in the forward path of the loop, loop rejection of spurious signals is quite good with one caveat: signals and noise within the loop bandwidth will be troublesome and care must be exercised to minimize spurious tones and noise that either mix or alias to baseband frequencies. Using (2.31), it can be seen that low frequency signals

which are within the loop bandwidth are multiplied by N , the division factor of the counter, while the bandwidth of the system is controlled by the open loop gain, A_{OL} .

$$A_{OL} = \frac{K_\phi F(j\omega) K_o}{j\omega N} . \quad (2.32)$$

The open loop gain controls the magnitude of the error signal and eventually the tracking error of the controlled oscillator with that of the reference. Thus large open loop gain of a feedback system is desirable. In addition, large phase detector gain is also desirable. The noise situation in the forward path of the loop is not unlike cascaded noise accumulation in the forward path of a receiver or transmitter. That is to say, large gain prior to the point of noise entry minimizes the impact of additional noise at latter stages. However, the designer has little flexibility to increase phase comparator gain K_ϕ without introducing excessive noise in the process. The phase detector is often implemented as a ring diode mixer or as an Exclusive Or digital detector operating as sinusoidal and edge-triggered detectors respectfully. Both types of detectors have very low noise performance. Detector voltage ranges are limited with voltage gain set by diode ring operation in one case, and supply voltage and digital threshold limits in the other. Phase detector gains typically range from 0.5 V/radian to 1 V/radian. N is usually in the range $2 \leq N \leq 6$. Lower values of N are desirable as we minimize the noise multiplication of the reference source. Conversely, small values of N raise the phase comparison and reference frequency and increase the risk of noise degradation. Noise degradation is partly contributed by the reference source which is now operating at a higher frequency as well as the phase detector. Both circuit functions suffer potential noise degradation if their associated internal signal jitter is not reduced relative to their operating frequency. Larger values of N increase the multiplication of reference noise and the acceptance of this approach is largely based on the noise performance achievable in the reference source. The implementation of the PLM architecture described in this dissertation uses $N = 4$. For example with $N = 6$ and 40 GHz operation, the phase detector must function at 7 GHz which is acceptable for a diode ring phase comparator. Although a lower N value would reduce the noise multiplication factor, this

is offset by the higher operating frequency of the phase comparator, f_x , and increased noise power within the bandwidth of the loop.

Additive phase noise from the counter is also of concern. Synchronous high speed binary counters are preferred to asynchronous counters. This is because clock jitter is not cumulative in synchronous clocked topologies but is for asynchronous counters. Small counter N values of 2, 4, 8, result in low excess phase noise as compared to larger and more complex counter structures such as master slave counters, Johnson counters, and ripple counters, see [70]. The use of analog dividers is an attractive option as it contributes very little added phase noise [71]. The design of the compensator, $F(j\omega)$, must first address feedback stability and loop compensation and second increase loop bandwidth. Finally, since the VCO utilizing a BST varactor requires a high tuning voltage, a charge pump voltage multiplier is required to supplement the loop compensator.

The VCO lends itself readily to tailoring the operating bandwidth of the multiplier loop through adjustment of the VCO gain K_o . Optimized loop bandwidth represents a trade-off analogous to balancing gain and loss in a cascade system. First, on the pro side, a wide loop bandwidth is desirable. VCO induced modulation from temperature cycling will induce mechanical stress, phase transients, and microphonics, all causes of loss of phase lock and communication link synchronization. These perturbations are suppressed in a wide loop. Therefore, a wideband loop via feedback forces these transient events to be reduced through high open loop gain and corrective feedback. It is instructive to calculate the potentially maximum bandwidth of the loop. Under the assumption that the minimum value of N is 1, and the loop compensator filter is unity, the loop bandwidth is limited to the product of $K_o K_\phi / j\omega$. Under this condition, the phase lock loop is a first-order control system. The oscillator as viewed by the phase comparator, is a perfect integrator. Therefore, closed loop gain approaches the open loop gain at low frequencies. Oscillator tuning gain of 400 MHz/Volt is typical. Although a benefit is achieving a wide loop, the large oscillator tuning gain is susceptible to extraneous noise modulation introduced at points (a) and (b) in Figure 2.5. Nevertheless, we will use this

value as a baseline. Then the loop bandwidth is $(0.64\text{V/radian}) \cdot (400\text{MHz/V}) \cdot 2\pi$, or 250 MHz.

Achieving wide loop bandwidth requires attention to nondominant poles, poles which are not part of the compensator $F(j\omega)$. These would include the tuning oscillator response time and any tuning line decoupling networks with their associated time constants, phase detector limiting bandwidth, R-C decoupling associated with the oscillator varactor input, and the loop amplifier if designed as part of the compensator network. The occurrence of all high frequency poles adds additional phase contribution. The total accumulation of additional phase shift must be calculated as it impacts the unity crossover frequency of the loop. Any additional phase shift which does occur near the unity gain crossover frequency of the loop, will cause undesirable noise peaking of the loop. This includes phase shift induced by sampler delay in the counter. The sum of the total phase shift of all the dominant poles which are located at radian frequencies $\omega = \omega_x$, are evaluated in relation to the loop unity gain crossing frequency, ω_{UG} . As a function of radian frequency this is given as,

$$\phi_T = \phi_{\text{OL}}(\omega) + \sum_x \tan^{-1} \left[\frac{\omega}{\omega_x} \right]_{\omega=\omega_{\text{UG}}} \quad (2.33)$$

with the accumulated phase shift evaluated at the unity gain crossing frequency, $\omega = \omega_{\text{UG}}$. The existing open loop phase shift, exclusive of the additional poles, is $\phi_{\text{OL}}(\omega)$. The ramifications of excessive additive phase shift is the consequence of excessive loop peaking and distortion of phase modulation introduced into the loop. Both of the aberrations are difficult to correct and compensate. This is addressed in Section 2.4. A measure of the phase modulation distortion effect comes from the deviation of the modulation linearity of the oscillator. The deviation from linear modulation results from the oscillator tuning varactor and associated varactor decoupling network and this is discussed in Section 4.6.5. In this discussion, the important considerations are tailoring of the VCO gain, meeting gain linearity objectives with non-optimum C-V varactor characteristics, and finding suitable resonator topologies to maintain these characteristics at high resonator power. One of the primary benefits of the PLM, aside from low spurious content is the potentially larger operating bandwidth. However, along with this benefit comes a noise

power increase resulting from frequency multiplication. Although the $20 \log(N)$ phase noise multiplication factor of the noise spectra of the source at f_x , exists as in the cascade multiplier case, the ability to provide “shaped” noise filtering after multiplication via a baseband loop compensator is far more straightforward.

With respect to the open loop cascaded heterodyne system, a PLM architecture has a number of distinct advantages. The function of filtering is now shifted from RF to baseband and although the same care in frequency planning is required, the number of sources in contention is low.

2.3.7 Reduction of spurious signals in a wide band loop

In this section we investigate the trade-offs involved in maximizing the loop bandwidth. We consider the need to accommodate the highest modulation frequency, while minimizing the introduction of spurious signals and suppressing mechanically induced modulation. Other forms of spurious modulation such as digital counter noise, phase modulation of the VCO induced via load impedance fluctuations, voltage pushing of the oscillator introduced via the phase detector, and conversion of the power supply noise by way of the VCO are particular to the PLM architecture. These additional modulation components are treated in the same manner as other discrete spectral noise components since their origin, although perhaps different, occur through similar mechanisms. These unique components of noise modulation will be considered here.

Loop modulation induced by mechanical vibration or microphonics, is discussed in Section 5.1.5. In addition, modulation induced through power supply and tuning supply voltage is also addressed. A noise equivalent model of the oscillator is developed. In addition, we address the microphonics of a GaN power FET oscillators.

If large oscillator tuning gain is used, there is the risk of signal crosstalk between digital control circuits and the analog components. In this case, phase noise modulation is induced through the oscillator control line as well as via the supply line and ground return paths. First,

consider the oscillator alone. The oscillator is modeled as a noise free integrator since the phase shift of the oscillator is proportional to the integral of the tuning voltage. All noise sources associated with the oscillator are placed at the tuning line input and are summed on a RMS basis assuming no correlation among these sources of noise. Since the modulation frequency and level are assumed small in comparison to the carrier frequency, the small angle rule for sinusoidal FM sources is permitted. The narrow band frequency modulation (NBFM) approximation is applied to calculate the level of spurious signal produced by the oscillator in the frequency domain. This level of noise modulation in the frequency domain, or the phase domain, is directly a function of the noise voltage input to the oscillator modulation port in the time domain. The oscillator is a voltage-to-frequency converter. Furthermore the oscillator is an integrator, as stated earlier, if we consider the oscillator output in the phase domain, which is precisely how the oscillator output is interpreted by the phase comparator. Then the voltage tuned oscillator is represented as shown in Figure 2.7.

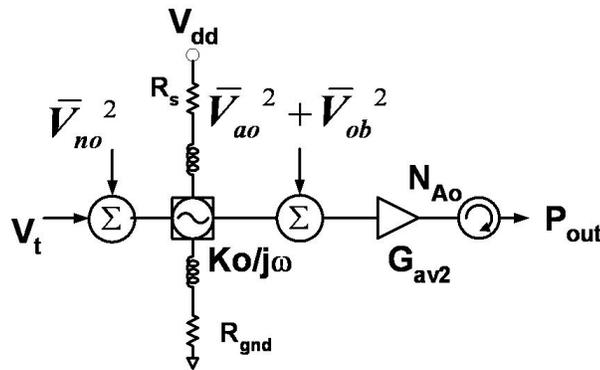


Figure 2.7: A simple noise equivalent model of the VCO

Describing the noise equivalent model of the oscillator and amplifier interface via superposition is possible since the noise voltages are uncorrelated. The oscillator noise modulation

is viewed readily in the frequency domain. It may be also viewed in the phase domain, see appendix. Several points of summation are provided at the oscillator and amplifier input. If no external additive noise modulation is present, then the intrinsic noise free oscillator is described conveniently. For this specific case, the signal-to-noise ratio at a specified frequency offset has an associated noise voltage level directly proportional to the oscillator tuning gain, given by K_o . The oscillator is modeled as noise free, and the necessary noise voltage required for a given signal-to-noise ratio power is obtained from the narrow band FM approximation. Since the noise modulation is small, the frequency deviation is small, and the level of the associated noise voltage is directly proportional to the modulation index given by β where $\beta = \Delta f / f_m$ where Δf is the deviation and f_m the modulation or offset frequency. Therefore, the corresponding noise power level is directly proportional to the V_n^2 . The level of these noise voltages are correspondingly reduced by the oscillator tuning gain at the corresponding point of noise entry. The dominant noise point of entry, and therefore highlighted in Figure 2.7, is the tuning line port. Hence we have,

$$V_n = 10 \log_{10} \left(\frac{N_o}{C} \right)_{f_{\text{offset}}} - 20 \log_{10} K_o + 20 \log_{10} (f_{\text{offset}}) \quad . \quad (2.34)$$

This expression is for the signal-to-noise spectrum of the VCO, and expressed as a single-sided carrier-to-phase noise value as measured on a signal analyzer [78]. Note, for the oscillator signal-to-noise cases studied in this work, this is the form of measurement; i.e. single-sided phase noise-to-carrier power ratio and if required, +3 dB is added if the double-sided carrier-to-phase noise value is desired.

The model shown in Figure 2.7 includes series resistance and reactance in combination with noise induced voltages applied to the tuning line at V_t . The elements R_{gnd} and R_s along with series inductance imply the inability to fully decouple the oscillator from noise-induced potential changes in the ground and the power supply line voltage and resistance. In other words, for a given oscillator current these variations will force modulation of the supply line voltage. The process is the same as modeling total equivalent noise at the tuning line as the mechanism is

additive phase modulation via the supply line. Such modulation, known as voltage pushing [80], usually has a reduced K_o as compared to the tuning line port and this would be modified in (2.34). The magnitude of these voltage sensitivity levels is striking, see Figure 2.7 and 2.34. The impact of these calculations are potentially a major concern in power oscillators as the peak supply currents are large.

As an example, consider an oscillator with 25% conversion efficiency operating at a supply voltage of 28 volts and 1 W output power. Assume the voltage and current supporting oscillation are sinusoidal. Then based on the load efficiency and DC operation at 28 volts, the required DC current is approximately 140 mA. Therefore, modulation of the ground return resistance due to shock and vibration is 140 mV/ Ω . Consider an offset frequency of 10 kHz and a desired single sided C/N_o ratio of 100 dB. Utilizing Figure 2.7 and (2.34) with Figure 2.8 scaled for the pushing value, we can make the following calculations. Consider an oscillator voltage pushing value which is 1% of the oscillator tuning sensitivity. Then a loop corrective gain of nearly 140 dB per a fluctuation of 1 ohm of contact resistance is required at an offset frequency of 10 kHz to meet this signal-to-noise ratio of 100 dB. Clearly, the DC return resistance needs to be either near zero, or held constant, or the oscillator and mechanics must be designed to be resistant to shock and vibration and hence reduce the oscillator pushing value. A similar set of calculations involve the spurious coupling of the sampling frequency, f_x , via the supply line and ground inductance paths. If the sampling frequency of the controlled oscillator is 1.5 GHz and the DC return inductance is 1 nH, then modulation current must be reduced in the supply and ground return paths below 100 pA. This calculation is driven based on the reactance of the ground and supply inductance. Fortunately, this problem is somewhat easier as conduction paths with 80 dB or more isolation are possible, permitting raising this level to a manageable 1 μ A. However, radiation paths are other coupling mechanisms and induction of RF currents are possible. Therefore, the use of electrostatic shielding is common in these architectures. A refined analysis of this problem is discussed when oscillator efficiency is presented in Section 4.5.

Several of these effects described above are captured in Figure 2.7. The noise voltages of the oscillator and all noise voltages associated with subsequent stages are assumed uncorrelated and statistically independent events. Therefore, the noise voltages of amplifiers, filters, and attenuators, can all be referred back to their respective inputs by replacing their noise voltage by an equivalent value offset by their stage respective gain or loss. Here, \bar{V}_{no}^2 and \bar{V}_{ao}^2 are from the referred oscillator signal-to-noise ratio and the use of (2.34) as this captures the effective gain of the oscillator. An amplifier noise factor would be handled in a similar manner, by offsetting noise voltage by the available gain. Finally, \bar{V}_{ob}^2 could be a noisy voltage uniquely associated with an oscillator output component, for example, a lossy attenuator, again referred back to a common point of noise entry after suitable loss scaling. Therefore, a noisy stage may be replaced by a noise free stage whose equivalent input noise voltage is scaled by the appropriate gain or loss of that stage. This central concept is key in deriving the cascade noise figure formulation of Friss [4]

The phase lock multiplier, configured as a wide bandwidth loop, will require the sampling rate of the loop to be high. The filtering of direct reference path clock spurious signals is easy if their point of entry is subsequent to the loop compensator. Although the loop compensator gain bandwidth product limits the upper frequency limit for attenuation of very wide loops, loops with bandwidths of 10 MHz can provide effective filtering when using current feedback amplifiers or high speed voltage feedback designs with the requisite gain-bandwidth product. Substantially higher frequencies will require appropriate higher frequency filtering in the forward path of the loop which is to the right of point (a) in Figure 2.6. This is best accomplished with additional $L - C$ networks. Preserving the $L - C$ filter transfer function while the terminations are complex, and not necessarily a constant real impedance (e.g 50 ohms), requires care. High frequency modeling of the phase detector as the source and the VCO varactor tuning line as the termination are required. A filter design which is based on a single termination, whereby the filter is either current or voltage driven is one approach.

The forward path of the loop is one entry path for spurious signals, and a number of

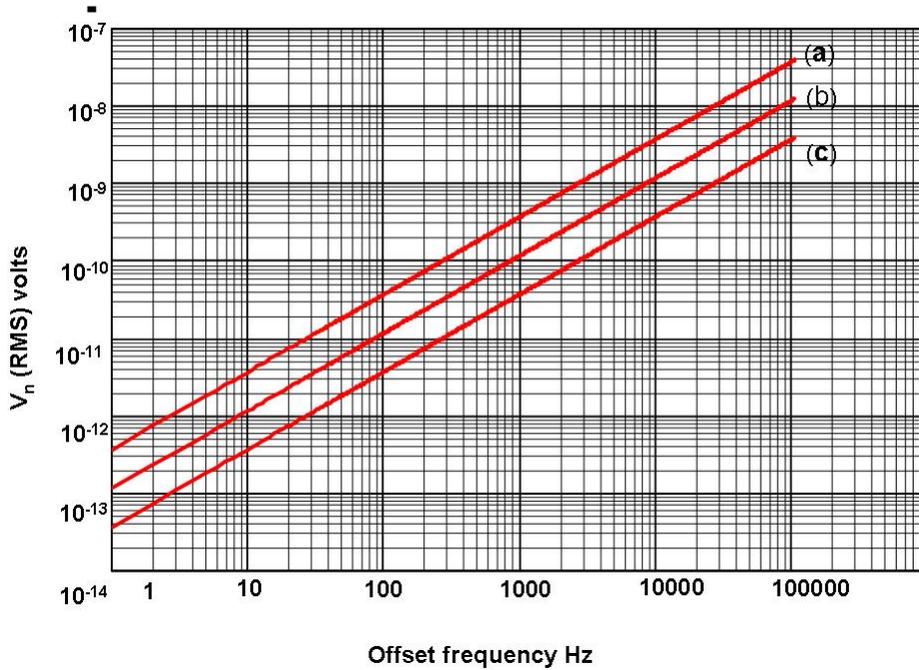


Figure 2.8: Double sided VCO equivalent input noise voltage, V_n vs. offset frequency for $2C/N_o$ of a) 80 dBc/Hz, b) 90 dBc/Hz, c) 100 dBc/Hz, $K_o = 400$ MHz/volt

secondary paths exist in the form of reverse paths from points (c) and (d), see Figure 5.29. Here, point (d) is referred back to the counter input as an equivalent input noise and spurious signal level voltage. These additional spurious paths exist as re-modulation of the VCO frequency through oscillator variation in termination impedance, also referred to as load pull, will occur. This occurrence of modulation is created by dithering the counter input impedance with the oscillator signal drive level at a modulation rate of f_m . Both paths (c) and (d) are subject to the injection of signal spurious. These spurious levels are reduced by the application of active isolation which is broadband. In addition, the use of small signal amplifiers which small high reverse gain and power splitters which provide port-to-port isolation are used. In addition, the balance of the ring-diode mixer provides isolation from the IF-to-RF and LO-to-RF ports by virtue of the balanced nature of the hybrid coupler which is germane to this class of mixers.

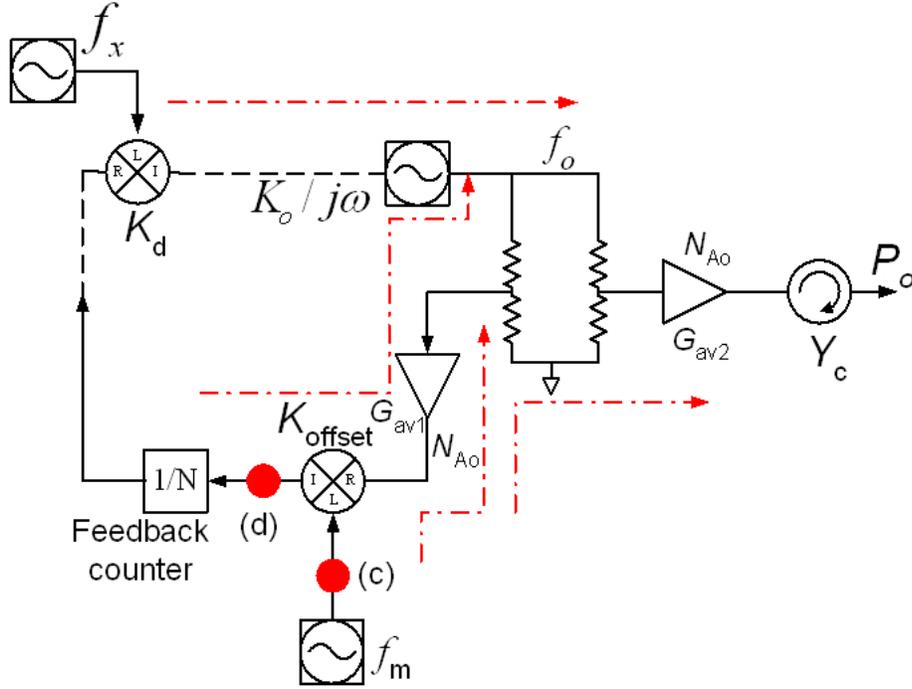


Figure 2.9: PLM signal spurious paths and isolation

2.4 Phase lock multiplier operation with modulation

In the cascade systems using heterodyne architectures, modulation is introduced into low frequency stages either through I-Q complex mixers, or through local oscillators. Eventually these signals are multiplied in frequency or translated by external mixers to the final carrier frequency. In the phase lock multiplier architecture discussed in this section, the base band and carrier frequency share a common port or node in the feedback path; the phase detector. Therefore, it is possible to introduce modulation into a single port and provide frequency translation in a single step. In this section we review the properties of introducing modulation into the loop and operation of compensation of the modulation to maintain a uniform frequency response. Complex modulation could than be accomplished by simultaneous modulation within the loop and outside the loop.

The PLM loop bandwidth needs are tailored to system requirements and are not necessarily

freely chosen, in order to accommodate wideband complex modulation. Auspiciously, the modulation bandwidth is supported independent of the PLM bandwidth through a compensation or pre-distortion method freely provided by the loop itself. Since the phase transfer function from point (b) of Figure 2.6 is high pass, the phase modulation which is deemphasized with increased modulation frequency will be automatically compensated. Conversely, modulation introduced at point (a) will be properly deemphasized, or low pass filtered, courteous of the loop compensator. Hence, perfect compensation is obtained if the loop is properly dampened near the unity gain crossover frequency of the system. Therefore, we are motivated to constrain loop peaking. First we desire to minimize the peaking of jitter and second reduce modulation distortion. Other locations where modulation may be introduced with the same compensation affect are pairs (c) and (b), and at f_x and (b) of Figure 2.6. There is yet another important advantage of placing modulation directly into the loop at two locations and not depending on outside “open loop” compensation. Since the phase detector inputs are from a set of complementary functions, the detector correction voltage due to modulation will sum to zero. No spurious signals are generated via the modulation. One challenge to this dual port modulation technique is the need to match the amplitude and phase deviation of each of the ports to modulation. In a practical sense the two deviations are not necessarily matched. Consider modulation introduced via f_x and at point (b) in Figure 2.6. The oscillator and phase comparator will have the same constants as used earlier, $K_\phi = (0.64\text{V/radian})$ and $K_o = (400\text{ MHz/volt}) \cdot 2\pi\text{ radians/volt-sec}$. Then

$$\Delta f_{o\text{LO frequency}} = N\Delta f_x \quad (2.35)$$

and

$$\Delta f_{o\text{HI frequency}} = K_o V_b. \quad (2.36)$$

The output frequency deviation Δf_o , with respect to the modulation introduced, is only flat with modulation frequency if $K_o \cdot V_b = N \cdot \Delta f_x$. Consider the modulation output frequency under the influence of the PLM parameters. Steady state transfer functions for modulation

introduced at f_x and at point (b) at the VCO input give

$$\Delta f_o(s) = \frac{\Delta f_x}{s} \cdot \frac{K_o K_\phi F(s)}{1 + \frac{K_o K_\phi F(s)}{sN}} + V_b \cdot \frac{K_o}{1 + \frac{K_o K_\phi F(s)}{sN}} \quad (2.37)$$

where $s = j\omega$ is the complex modulation frequency, and here where f_{mod} is the modulation frequency, $\omega = 2\pi f_{mod}$. Using the relations of (2.35) and (2.36) in (2.37) and setting these equal to the required modulation response, Δf_{req} yields

$$\Delta f_o(s) = \frac{\Delta f_{req}(s)}{sN} \cdot \frac{K_o K_\phi F(s)}{1 + \frac{K_o K_\phi F(s)}{sN}} + \frac{\Delta f_{req}(s)}{1 + \frac{K_o K_\phi F(s)}{sN}} \rightarrow \Delta f_{req}(s). \quad (2.38)$$

We see that the required modulation response, $\Delta f_{req}(s)$, will be constant with respect to the modulation frequency as the modulation frequency varies from below and above the loop natural frequency, f_n given by $K_o K_d F(s)/N$, where N takes on discrete values equal to or larger than unity. Now the incremental error in the modulation frequency response of the PLM is represented by an error in the magnitude and phase match between any two points of modulation entry. Let $\frac{\Delta f_{oHI \text{ frequency}}}{\Delta f_{oLO \text{ frequency}}} = (1 + \varepsilon) \exp(-j\theta)$. Then

$$\frac{\Delta f_{oHI \text{ frequency}}}{\Delta f_{oLO \text{ frequency}}} = (1 + \varepsilon) \cos(\theta) - j(1 + \varepsilon) \sin(\theta) \quad (2.39)$$

where the amplitude mismatch is given by ε and the phase mismatch by θ . Using (2.38) and rewriting $\Delta f_{oreq}(s) = \frac{\Delta f_{oHI \text{ frequency}}}{\Delta f_{oLO \text{ frequency}}}$ gives,

$$\Delta f_o(s) = \Delta f_{oLO \text{ frequency}} \left(\frac{\frac{K_\phi K_o F(s)}{sN} + \frac{\Delta f_{oHI}}{\Delta f_{oLO}}}{\frac{K_\phi K_o F(s)}{sN} + 1} \right). \quad (2.40)$$

Various forms of compensator and phase detector are available. The infinite gain, zero static phase error loop is considered most appropriate for low noise and minimum spurious feed-

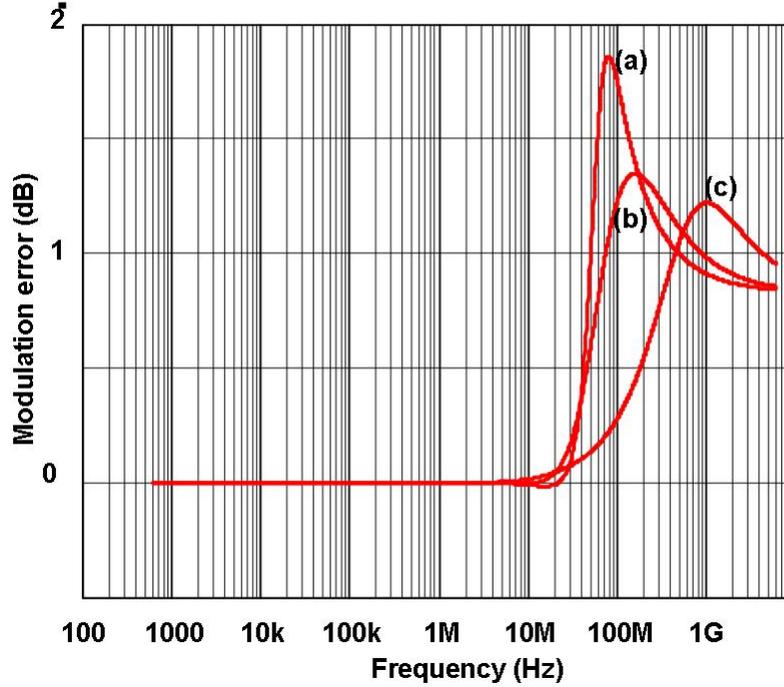


Figure 2.10: Wide band modulation response for 10% amplitude mismatch and 10 degree phase mismatch: (a) $\delta = 0.5$; b) $\delta = 1$; and (c) $\delta = 5$

through. The digital phase detector is implemented as a tri-state charge pump configuration. The ring diode modulator operating as phase detector with an active loop filter compensator closely approximates the same type detector. For this case the compensator transfer function is given by $F(s) = R \cdot (s + 1/RC)/s$. Substituting for $F(s)$ and, $\frac{\Delta f_{oHI}}{\Delta f_{oLO}}$ using (2.39) and with $s = j\omega$ results in (2.40) becomes,

$$\frac{\Delta f_o}{\Delta f_{LO}} = \frac{(f_n^2 - f^2 (1 + \varepsilon) \cos(\theta)) + j (2\delta f_n f + (1 + \varepsilon) f^2 \sin(\theta))}{(f_n^2 - f^2) + j f (2\delta f_n)}, \quad (2.41)$$

where the modulation frequency is f and the output deviation frequency is normalized to the low end of the modulation frequency, $\Delta f_o/\Delta(f_{LO})$. Expression (2.41) is a function of the loop natural frequency, f_n , dampening factor δ , and amplitude and phase mismatch factor, ε and θ .

All terms are available as design elements of the PLM. Finding the magnitude gives,

$$\left| \frac{\Delta f_o}{\Delta f_{LO}} \right| = \sqrt{\frac{(f_n^2 - f^2(1 + \varepsilon) \cos(\theta))^2 + (2\delta f_n f + (1 + \varepsilon) f^2 \sin(\theta))^2}{(f_n^2 - f^2)^2 + f(2\delta f)^2}}. \quad (2.42)$$

Note for zero amplitude and phase mismatch, the magnitude of (2.42) is unity and the modulation response is flat. The fidelity of the modulation response as a function of amplitude and phase mismatch is shown in Figures 2.10 and 2.11. The loop modulation response vs. modula-

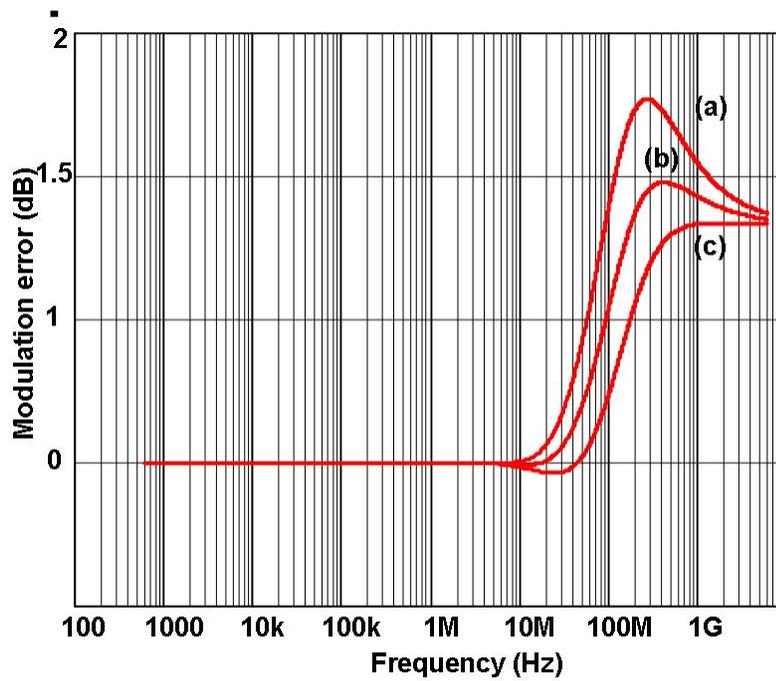


Figure 2.11: Wide band modulation response for constant δ of 1.5 and amplitude mismatch of 10% but various phase mismatch: a) 10° , b) 5° , c) 1° .

tion frequency is normalized to the natural loop frequency, f_n . The graph provides normalized frequency response curves for both amplitude and phase mismatch and dampening variation.

Peaking near the natural frequency of the loop, 10 MHz, occurs for small damping and is aggravated by larger amplitude and phase mismatch. For damping slightly larger than unity,

the loop modulation error is confined to about 1 dB.

In this section, modulation and distortion of the PLM was addressed. Parameters of the loop were derived which influence the degree of fidelity of the modulation. The loop provides frequency response self compensation to the modulation band over a wide frequency range, and if properly designed, the loop bandwidth can be designed to meet other objectives. These objectives include spurious signal reduction and the reduction of noise power spectral density over a specified offset frequency range relative to the carrier frequency.

2.4.1 Power transfer oscillator

In the cascade approach to achieving high output power, small signal amplifiers are concatenated with impedance matching between stages, the signal attenuated to the appropriate input power levels, and signal finally filtered if required. Additional stages are added to increase the power if required, and this sequence, with added gain control stages is repeated. This approach although successful, is not particularly efficient and suffers from the classic trade-off of gain, noise, and distortion. In this section we discuss how the PLM architecture is used to more successfully implement the trade-offs.

An interesting variation of the PLM is one that permits an architecture whereby the loop counter takes on the value of unity, thus the output oscillator is operated at the same frequency as the comparison or reference oscillator frequency. Therefore, there is no noise multiplication

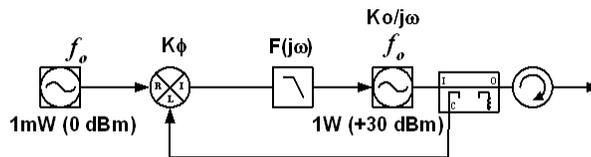


Figure 2.12: A power transfer oscillator, a PLM with $N=1$, permits a high power oscillator to track the favorable characteristics of a lower power source. In the process, the power gain achieved here is 30dB.

since the counter N is unity. Another approach, uses a frequency multiplier in lieu of a counter in the feedback path of the loop. The consequence of eliminating the counter N is that the in-band phase noise and loop bandwidth are significantly reduced and potentially widened respectfully. This configuration is best termed a power transfer oscillator with an intrinsic low pass filter (LPF) function. The phase lock loop (PLL) serves as a gain block, transferring the signal qualities of a low power source to a **high power** source subjected to a LPF transfer function in the forward path of the loop. In effect, the PLL is a gain block with the its gain being the ratio of the locked oscillator output power relative to the reference source power. The block diagram of the system is shown in Figure 2.12 and such an approach is extendable as illustrated in Figure 2.13. A single reference oscillator serves to synchronize all sources and mitigates the propagation of phase noise accumulative jitter from each loop. The cascaded oscillator loops do not result in intermodulation distortion. However, noise propagation and the cascade effect of cumulative phase noise is potentially an issue. Thus care in setting each successive loop bandwidth is required to mitigate noise.

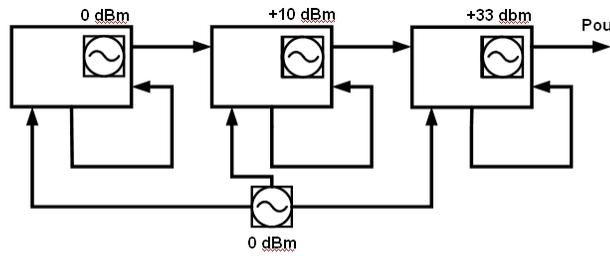


Figure 2.13: The power transfer technique is extendable. Each loop in effect a LPF and without the problems of cascaded intermodulation distortion.

2.5 Power oscillator development

In this section we put forward the ground work and lay down a foundation for power oscillator synthesis. Subsequent sections will focus on contributions to designing the resonator for proper

active device interface with the primary aim to address tuning stability. We address efficiency and the ability to operate the active device in a role not customary for an oscillator configuration. The goal is minimizing thermal resistance and maximizing heat transfer for reliability and performance.

This section provides an overview of the critical aspects of power oscillator design. A review of small signal oscillators provides a good introduction into oscillator synthesis, especially tunability and stability. This review discusses the oscillator noise profile, and for simplicity we will use the LTI (linear time invariant) approach. This provides fundamental understanding of noise when the active device is operated in the oscillator regime, and the impact on noise resulting from the interaction of the active device with the resonator. The main motivation in this section is highlighting the design issues and problems that arise in power oscillator design.

2.5.1 Oscillator-power amplifier, a review of the interface

Fundamentally, one approach to power oscillator design as applied to direct carrier launch is to utilize a small signal oscillator operating at carrier frequency followed by a power amplifier in cascade. The desired output power is 1 W. Consider a small signal oscillator operating at a nominal output power of 1 mW (0 dBm) which would require a minimum of 30 dB power gain to achieve a desired 1 W output power. Once again the issue of cascaded noise and distortion must be addressed. Noise power and the ability to minimize extraneous cross coupling of unintentional signals is a challenge, especially with the 30 dB power gain required.

The first problem addressed is the design of the amplifier and oscillator resonator parameters to meet a specified output carrier signal-to-noise, (C/N_o) , ratio. If the loop gain is too high there is a potential for spurious signal generation and possibly loop instability. Since the loop is a feedback system, noise suppression will be inversely proportional to the open loop gain at a particular offset frequency from the carrier. To see this, we can model the output oscillator noise resulting when noise is injected at point (b) in Figure 2.5. The transfer function for the output oscillator frequency deviation with respect to the noise voltage $\overline{V_{no}^2}$, and considering the

oscillator noise model of Figure 2.7, is

$$H_{V^2_{no}}(s) = \frac{K_o/s}{1 + K_o K_\phi (s\tau + 1) / (Ns^2)}. \quad (2.43)$$

The transfer function is high pass and frequency excursions of the oscillator are reduced by the open loop gain, in this case $K_o K_\phi (s\tau + 1) / (Ns^2)$. The value of τ which provides a transmission zero, forms lead compensation and therefore phase lag compensation. The value of τ is chosen to provide appropriate stability and damping control of the loop.

It can be seen that, the oscillator phase transfer function and hence the phase noise of the oscillator will be reduced by the value of the loop gain. Correction of a phase disturbance will occur if the rate of change of the phase disturbance is much less than the loop unity gain frequency of the loop. A plot of a typical open loop gain characteristic is shown in Figure 2.14. Here the oscillator gain is 400 MHz/V and the phase detector gain is 1 V/radian. The loop must be phase compensated for stability by the addition of a zero. In this case the time constant of the zero, τ is set to approximately $\frac{1}{60}$ th of the inverse of the maximum frequency where loop correction needs to be applied, or 10 kHz. There will be negligible suppression of the noise resulting from disturbances with rate of change above 100 kHz. Assuming no other sources of noise, at 10 kHz the corrective gain is 32 dB and therefore the phase noise modulation is suppressed by a factor of 40. Thus, this forces the oscillator to adhere to the noise properties of stages prior to the point of noise entry. For example, if the (C/N_o) value at an offset frequency of 10 kHz from the carrier is -70 dBc/Hz, then this value would be improved by 32 dB to -102 dBc/Hz. This improvement again assumes that no other noise contributors are present near or above this level. Superposition of all noise sources that contribute to the oscillator output is possible assuming that there is no correlation among the sources of noise. The net total signal-to-noise ratio is a result of applying superposition to all points of noise entry shown in Figure 2.5 [79].

It is more convenient to use the oscillator signal-to-noise ratio rather than the carrier-to-noise in the analysis that follows. From [87] the signal-to-noise ratio is a function of the singly

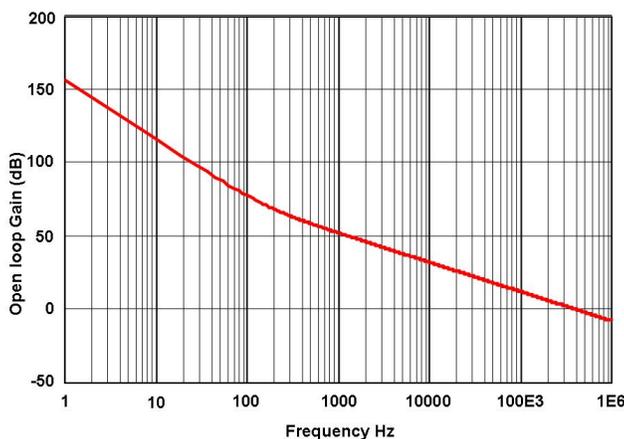


Figure 2.14: Open loop gain of PLM with $N=4$, correction gain at 10 kHz is 32 dB

loaded Q , Q_L , and the carrier signal power, P_s . If no additional power is removed from the network, then the carrier signal power is the total power available to the resonator. In the ideal case, very little power needs to be removed from the resonator and delivered to the active device to sustain sufficient loop gain and satisfy the condition of oscillation. An expression for the signal-to-noise ratio that considers LTI operation and only two sources of noise, white phase noise of the active device and the thermal noise contribution of the finite Q resonator only, Q_L , is [89] and [90]

$$\frac{S}{N} = \left(\frac{\omega_m}{\omega_o} \right)^2 \frac{P_s Q_L^2}{FkT}. \quad (2.44)$$

The radian carrier frequency and the offset radian frequency are ω_o and ω_m respectfully. A simplified representation of an oscillator consists of an output network configured as a resonator providing a feedback voltage. The feedback voltage in turn controls a voltage controlled current generator with an initial transconductance G_m driving the resonator. The voltage gain of this loop needs to approach unity from an initial gain larger than unity and with a total phase shift of 360° to satisfy the condition of oscillation. The elements of the network are shown in Figure 2.15. The $g_m \cdot V_{in}$ term is associated with the active device and g_m is dynamic; beginning with a large signal of amplitude G_m and compressing with the large input signal until the

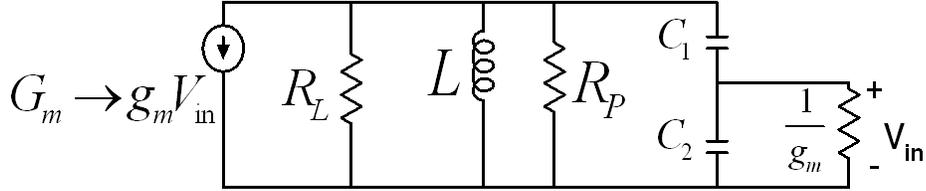


Figure 2.15: Basic oscillator with L-C resonator, feedback and load

voltage gain is unity. If there is no power removed from the network, the initial assumption, then R_L is infinite and R_p is just the real loss of the finite Q of the resonator, (Q_{UL}), and the transformed device input impedance with feedback. Although this is a very heuristic approach, it is sufficient at this level for our analysis. The problem to address is to find the resonator power for a given signal-to-noise ratio while delivering sufficient power to an external load, for example an amplifier. Power must be removed from the resonator, a portion of which provides feedback to the active device while the remaining resonator power is delivered to an external load. The carrier signal-to-noise ratio must be sufficient to satisfy the requirements of the cascaded oscillator-amplifier combination.

The total required resonator power, P_T , is a function of the RMS resonator voltage, the resonator impedance, and the external load impedance. The total resonator impedance is assumed real as any reactive portion is absorbed by adjustment in the resonator design. The total power delivered to the resonator is proportional to the supply voltage, the specific embedment of the active network, and the connection to the resonator and is defined as P_T . Assuming a sufficient resonator operating Q_L , the RMS resonator voltage of the resonator gives a resonator total power of,

$$P_T = \frac{V_T^2 (R_L + R_P)}{R_L R_P} \quad (2.45)$$

while the power available to the load is, is

$$P_L = V_T^2 / R_L. \quad (2.46)$$

Again, reiterating, while R_L is the external load, R_P will include the finite lossy R of the resonator and the transformed dynamic input resistance ($1/g_m$) of the device. The loaded and unloaded Q of the resonator are defined in terms of all of the resistances, internal and external, and reactance of the resonator, X_L . Then $Q_L = (R_L // R_P) / X_L$ and $Q_{UL} = R_P / X_L$ where $//$ implies parallel combination. Using the definitions of Q , we form the Q ratios given by,

$$\frac{Q_{UL}}{Q_L} = \frac{R_p + R_L}{R_L}. \quad (2.47)$$

The ratio of the total power to the load power is given by,

$$\frac{P_L}{P_T} = \frac{R_p}{R_P + R_L}. \quad (2.48)$$

The resonator loaded Q , Q_L , is assumed large enough to sustain nearly sinusoidal voltage, then a reasonable assumption is $Q_{UL} \gg Q_L$. Therefore, using (2.47) and (2.48) we can write the ratio of the power delivered to the load, to the total power available as,

$$\frac{Q_L}{Q_{UL}} = \frac{P_T - P_L}{P_L}. \quad (2.49)$$

The total signal power, P_s , required by the oscillator-resonator combination to meet a specified signal-to-noise ratio, must be provided by P_T . Therefore, rewrite (2.44) as,

$$\frac{S}{N} = \tilde{k} \left(\frac{\omega_m}{\omega_o} \right)^2 P_T Q_L^2 \quad (2.50)$$

where \tilde{k} is FkT . Using (2.49) and upon substitution into (2.44) we have,

$$\frac{S}{N} = \tilde{k} \left(\frac{\omega_m}{\omega_o} \right)^2 \frac{(P_T - P_L)^2 P_T}{P_L^2} Q_{UL}^2. \quad (2.51)$$

Then (2.51) is written in a convenient form to permit establishing the total oscillator carrier power for a specified signal-to-noise ratio and for a specified carrier power to be delivered to an

external load. Thus we have from (2.51)

$$\frac{S}{N} = \tilde{k} \left(\frac{\omega_m}{\omega_o} \right)^2 \frac{P_T^2}{P_L^2} \left[\frac{(P_T - P_L)^2}{P_T} \right] Q_{UL}^2. \quad (2.52)$$

Clearly, if $P_T = P_L$, all of the power available to the resonator is delivered to the load, and the signal-to-noise ratio approaches zero dB. Then the question is, what total power delivered by the active device and made available to the resonator is required to satisfy a specific signal-to-noise ratio, while still delivering a specified power to an external load? Let $P_x = \frac{(P_T - P_L)^2}{P_T}$, where P_x is the minimum power required for the oscillator to satisfy the oscillator signal-to-noise ratio. Then using (2.52), we form a quadratic equation in terms of the total power P_T , the external load power P_L , and the minimum required power, P_x given by,

$$P_T^2 - (2P_L + P_x) P_T + P_L^2 = 0. \quad (2.53)$$

Selection of the positive root results in the required oscillator total power in terms of the the load power and the minimum power to preserve the signal-to-noise ratio. Thus we have from (2.53) the required total power as

$$P_T = P_L + \frac{P_x}{2} + \sqrt{P_L P_x + \frac{P_x^2}{4}}. \quad (2.54)$$

A graph of this relationship is given in Figure 2.16. As the power required by the load increases, the required power that must be delivered to the resonator increases accordingly, so as to maintain the desired signal-to-noise ratio. The initial estimates of resonator power are first driven by (2.44) and are directly a function of operating frequency and loaded Q . As the external load impedance decreases, the effective loaded Q will decrease. Thus an increase in available resonator power is required to meet the target signal-to-noise ratio.

Next, we consider the possibility of implementing the power oscillator as a cascade of a low power source followed by a suitable power amplifier. The relationships of the signal-to-noise

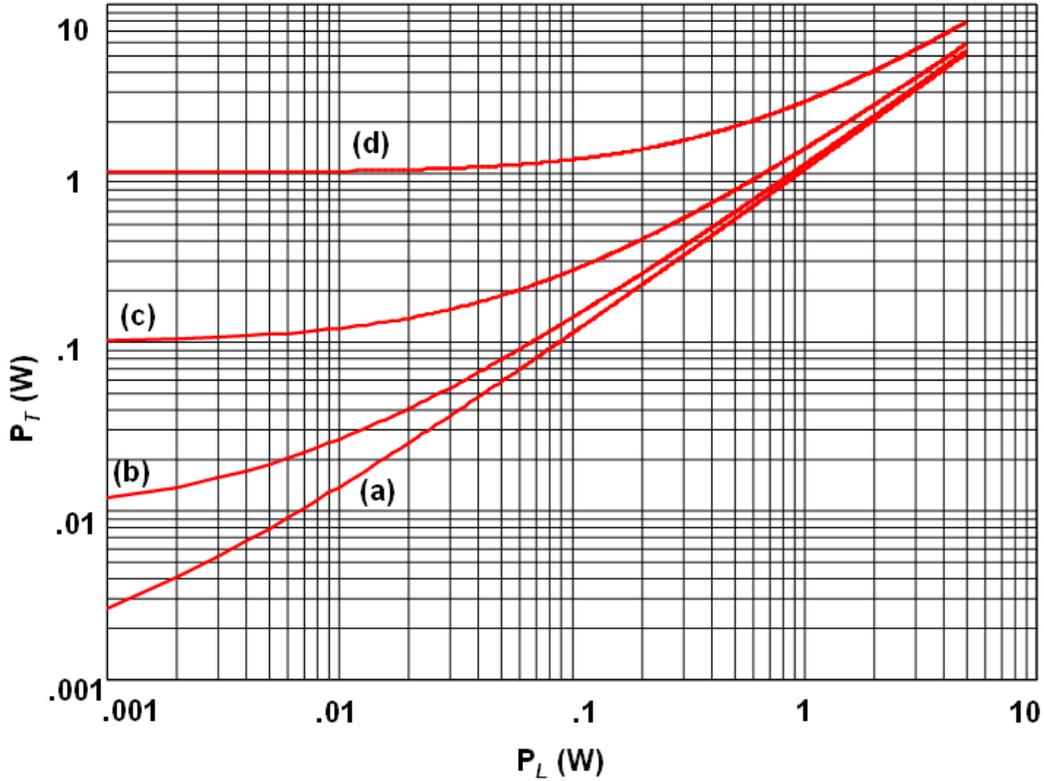


Figure 2.16: Oscillator total power required versus load power for resonator power of: (a) 1 mW; (b) 10 mW; (c) 100 mW; and (d) 1 W.

ratio for an amplifier and an oscillator source, permits us to investigate the cascade performance of this system.

Consider the requirement for a small compact frequency source to deliver 33 dBm power to a load at 6 GHz. The desired signal-to-noise ratio is 85 dBc/Hz at an offset frequency of 10 kHz. The oscillator will be realized in hybrid form, a mixture of thick and thin-film components. Key components to the realize the oscillator performance are obtained from equation (2.44) and includes the oscillator signal power and the resonator loaded Q . As an estimate to the loaded Q value, we will begin with the evaluation of representative unloaded Q values of compact networks at 6 GHz.

Resonators implemented in short quarter wavelength microstrip or as discrete inductors will exhibit reactance values of 75 ohms or greater at 6 GHz. A transmission line with a

Z_o of 75 ohms will also exhibit a reasonable unloaded Q . Thin-film inductors were used in several oscillators and demonstrated high self-resonant frequency and low equivalent series resistance loss [81]. The interconnection of the supporting printed trace lines and pads of the hybrid oscillator must be considered, as they add additional lossy connections to the inductor, microstrip transmission line, and varactor combination forming the resonator. An equivalent series resistance of 1 ohm or less is reasonable, and therefore an unloaded Q at 6 GHz of the resonator only is 75. Additional reduction in unloaded Q is expected as the device transformed impedance and external load are added. However, this initial value is adequate for purposes of estimation.

An additional term required from (2.44) is the noise factor, F . This factor is required before arriving at the required minimum resonator power. Although the noise factor F is occasionally referred to as a “fitting” parameter, it nevertheless serves well in establishing a baseline estimate for the oscillator noise floor. We can use the signal-to-noise ratio reported on a number of small signal oscillators to arrive at a reasonable value for F . Unfortunately, for much of the oscillator work, reports of loaded Q are either not provided or not known. However, we consider a different approach to arrive at F .

We find that the operation of the resonator loaded Q at 50% of the unloaded Q value is appropriate to maximize the signal-to-noise ratio. This is based on the relation of resonator loss, which is a function of the loaded to unloaded Q ratio. Since losses in the resonator must be accounted for by an increased open loop gain to satisfy the condition of oscillation, one cannot arbitrarily increase Q_L without an increase in insertion loss. The consequence is a need for larger power gain. These two competing effects result in an optimum Q_L with an associated resonator loss of 6 dB [88, 89]. So the assumption is that phase noise values given are at least measured at offsets less than the half power bandwidth of the loaded resonator, and extrapolation to an offset frequency of $f_o/2Q_L$ will provide a maximum noise floor parameter. Relative to $kTB/2$, this parameter permits an estimate of F . As an example, the oscillator reported in [91] demonstrates a phase noise value of -80 dBc/Hz at 10 kHz offset at 6 GHz.

With an unloaded Q of 38, the noise floor is at 80 MHz.

The slope of the phase noise is initially flicker of frequency, giving rise to a 30 dB/decade noise slope. At approximately 100 kHz offset, the trend line of noise slope changes over from flicker of frequency to white frequency. Thereafter, the noise slope is 20 dB/decade [82]. A Bode point-slope approximation to the noise slopes would place the noise floor value at -166 dBc/Hz. However, the trend line from the flicker of frequency to white frequency of noise is not distinct, and without an abrupt transition at 100 kHz. So a better estimate of the noise floor is approximately 3 dB less. We will assume that the noise floor consists of equal parts of AM and PM. This assumption is based on the idea that at large offset frequencies from the carrier, the loop gain is reduced to the point that the self-limiting gain function of the oscillator is not present. Therefore, there is little suppression to the AM component of noise. The total noise power at the floor is -163 dBc/Hz. With the assumption that this single sided noise power consists of equal parts AM and PM noise, the noise factor of the oscillator is the difference between the associated kTB power and our estimated noise floor, or a noise factor, F equal to 12.6, an effective noise figure of 11 dB.

Next, we apply all our known quantities, the loaded Q , the offset and carrier frequency, the oscillator noise factor and the desired signal-to-noise ratio to establish the required total power, P_T . Using (2.44) we therefore have,

$$P_T = -20 \log(Q_L) + 20 \log(\omega_m/\omega_o) - 177 + F_{\text{dB}} + SNR_{\text{dB}}. \quad (2.55)$$

Recall, the loaded Q is 38 and the the offset frequency, ω_m , is 10 kHz, while the carrier frequency is 6 GHz. Finally our effective oscillator noise figure is 11 dB and the desired signal-to-noise ratio, SNR, is 85 dBc/Hz. The resulting required total power, P_T , is 6 dBm.

From a practical viewpoint, oscillator output power is not provided directly available from the resonator or the active device. Instead, to minimize the problems of load pulling the source frequency [83], an isolator is included. A straight forward attenuator pad is selected and for convenience, a 3 dB attenuation factor is used. This would insure a minimum of 6 dB

isolation. Finally, to accommodate this loss, we elect to increase the total required power by 3 dB. If the power amplifier gain is 20 dB, the required oscillator power delivered must be 13 dBm. Therefore, from Figure 2.16 (b), the total oscillator power to be made available to the resonator must exceed 40 mW. Consequently, the power delivered to the power amplifier is the required 13 dBm.

Next, our attention turns to the oscillator source cascaded with the power amplifier. The power amplifier input power level is 13 dBm. The small signal noise figure of a 20 dB gain power amplifier [84] is nominally 7 dB with a $P_{-1\text{ dB}}$ level of 11 dBm. At the required oscillator power level, with the assumption that the oscillator noise factor F remains the same, the oscillator-amplifier cascaded SNR at will meet the target specification at 33 dBm output power. However, this requires the power amplifier to contribute no additional noise power. Although the small signal noise figure of the amplifier is 7 dB, a significant issue arises at the desired input power level to the amplifier of 13 dBm. This input power level is 3 dB in excess of the input compression point. Furthermore, at 7 dB noise figure, the PM noise floor of the amplifier is -170 dBc/Hz , just 7 dB below that of the oscillator broadband noise floor. Therefore, a small degradation in the total cascaded noise floor of 0.8 dB will occur. However, if the input power of the power amplifier is increased beyond the $P_{-1\text{ dB}}$ point, further noise floor degradation will occur. As much as a 5 dB shift in noise figure from small signal measurements is reported in [85]. This causes a significant noise floor degradation, just under 4 dB. Although, the focus is on the noise floor degradation, close to the carrier noise power will also shift accordingly with input power and care is required in these measurements, see [86].

In this section, the oscillator power required to meet a specified signal-to-noise ratio while providing a specified power to an external port is derived. The problem was initially defined in terms of the LTI model for power spectral density of oscillator phase noise and recognizing the need to meet a total signal-to-noise power ratio for a subsequent active device; for example a power amplifier. Therefore, both the oscillator noise factor as well as the amplifier noise factor must be considered. First, the required resonator power must be found to meet the intrinsic

oscillator signal-to-noise ratio and then the required extracted power must be added to this based on the noise factor of subsequent stages. A graphical solution to the problem is provided.

2.5.2 Active device-resonator interaction and tunability

In this section we develop the relationships that define the tuning of the oscillator. The key interface to review is between the active device, the resonator, and adjustments to the resonator as opposed to the active device to permit stable tuning. We review the adjustment of the resonator frequency in the context of the varactor parameters and develop a set of parametric equations which link the varactor characteristics to two key performance metrics of the oscillator; tuning sensitivity and phase noise.

It was shown that an important objective in the design of tunable oscillators is adequate frequency agility while not affecting other parameters such as phase noise, frequency stability, power output, harmonic content, and efficiency. The frequency agility and frequency stability characteristics are closely coupled. As an example, an oscillator which is tuned via a sweeping voltage in time, should remain stable at any preset swept voltage when the sweep function is removed. The frequency shift with time ceases. A continued movement in frequency is addressed by post tuning drift [93].

In this section we consider the definition of oscillator tuning gain from the perspective of the varactor capacitance change, resonator topology and varactor Q . The influence of the varactor Q , resonator unloaded Q , and oscillator tunability are considered. The effects on oscillator phase noise and the trade-off between noise performance and frequency agility are highlighted. The C-V relation and unloaded varactor Q of a MIM BST-based varactor is shown in Figure 2.17.

Explicit tuning sensitivity equations are derived in terms of the varactor parameters C_V , frequency, and tuning voltage and the relation given by the basic tuning sensitivity relation, $\frac{\partial C_V(V)\partial\omega(C_V)}{(\partial V\partial C_V)}$. We note that this relation does not contain the parameters of the active device and it should. The tuning sensitivity equations are highly idealized and the device

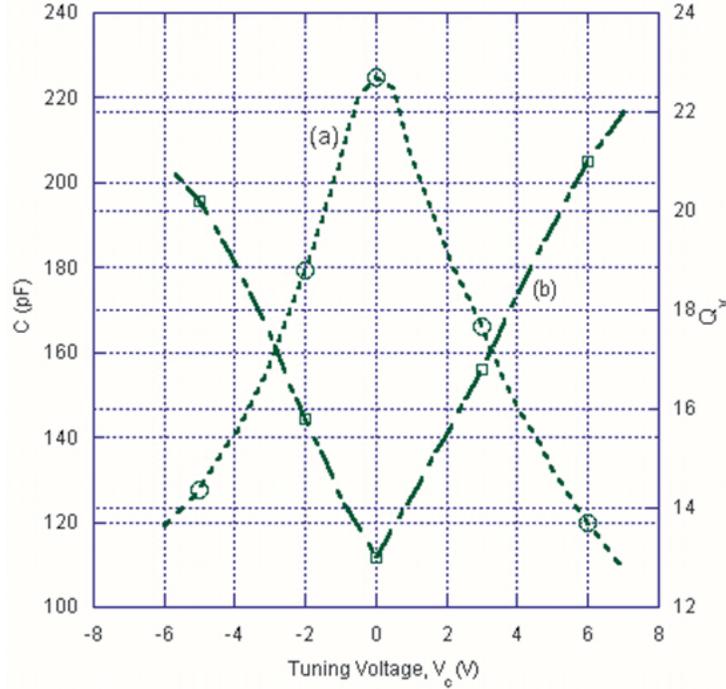


Figure 2.17: Characteristics of a BST-based MIM Varactor as a function of tuning voltage: (a) Capacitance; (b) Q

parameters play a major role in determining the profile of frequency versus tuning voltage. Nevertheless, the idealized approach does provide insight into improving tuning sensitivity. For example, the BST varactor, the characteristics of which are shown in Figure 2.17 does not exhibit significant change in capacitance versus tuning voltage near zero volts, and so techniques for increasing the reactance change with voltage, paramount to improving tuning sensitivity, is investigated.

Although oscillator phase noise is not the highest priority in power oscillator design, levels of phase noise commensurate with reasonable loop gain must be achieved. Of course at some point in the PLM, the required SNR must be met for a given objective, as the loop will have a finite bandwidth. A finite bandwidth is essential, if for no other reason than meeting a degree of stability margin. A fundamental set of concerns for the varactor performance and those requirements are reviewed in [92]. Maximizing the product PQ^2 of (2.44) is of principal

importance and therefore in [92] the emphasis is the reduction of the varactor equivalent series resistance. In addition, to maximize P_T requires maximizing the RF voltage across the resonator and hence the varactor. Therefore, the ability to operate the varactor at high voltage is an asset. Finally, raising the self-resonator frequency of the varactor through reduction in series inductance and improved packaging is vital. Absent in [92], is a definitive relation between noise and varactor tuning capability. One of the objective of this section is the development of a normalized tunability reduction factor in terms of the varactor capacitance tuning range, a normalized frequency tuning variable, and a factor q [94]. Here q is a normalized Q which provides the ratio of the Q of the resonator without the varactor, essentially Q_{UL} , to the minimum varactor Q , Q_{VM} ,

$$q = Q_0/Q_{VM} . \quad (2.56)$$

First consider the varactor tuning range of a resonant network and the application of the resonant network with an ideal device. The ideal active device, has a constant phase shift independent of the device signal level and frequency. Then the resonant network embedded in the feedback path of an active device must meet the Barkhausen criteria; that is the resonator in conjunction with the active device must satisfy the appropriate open loop gain, greater than unity, and a permit a phase shift which supports positive feedback for all frequencies within the passband of the resonator. If this is the case over the tuning range of the resonator, than the oscillator tuning frequency would be determined by the junction varactor capacitance, characterized from zero volts of reverse bias to the varactor breakdown voltage. This tuning range is defined by α , where

$$\alpha \equiv (C_{V0}/C_{VB}) \quad (2.57)$$

where C_{V0} is the varactor capacity at tuning voltage of zero volts and C_{VB} is the varactor capacity at the breakdown voltage. When a varactor is operating well below its self resonance frequency, it is modeled as a series R-C network. The Q of the varactor, designated as Q_V , is

dominated by its series resistance, R_S . Then, the varactor Q is given by

$$Q_V(V) = Q_{VM} \frac{C_{V0}}{C_V} \quad (2.58)$$

where Q_{VM} is designated as the minimum varactor Q , obtained at zero tuning voltage. The varactor is modeled here as a series R-C network. Resonators used with microwave oscillators can generally be modeled as parallel circuits so it is convenient to transform to a parallel form as shown in Figure 2.18(b). Using a series to parallel transformation permits an equivalent network with the shunt varactor elements

$$R_P = R_S(Q_V^2 + 1) \text{ and } C_{VP} = C_{VS}/(1 + 1/Q_V^2). \quad (2.59)$$

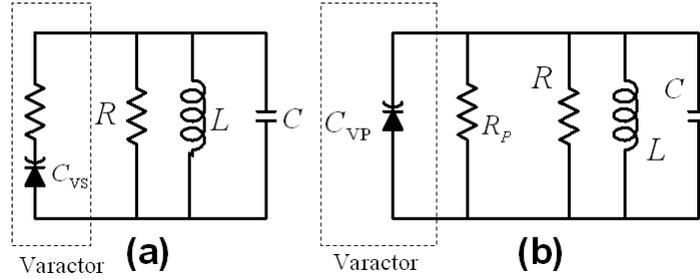


Figure 2.18: Equivalent network representation of a resonator with a varactor: (a) simplified resonator and active device network with series varactor resistance R_s ; and (b) transformed equivalent network with all elements in shunt.

The unloaded Q of the varactor is $Q_V \geq Q_{VM}^2 \gg 1$ and replacing Q_V in (2.59) with the expression in (2.58) we have

$$C_{VP} \approx C_{VS} \text{ and } R_P = R_S Q_{VM}^2 (C_{V0}/C_V)^2. \quad (2.60)$$

The effect of the resonator or tank circuit is obtained by including the value of Q of the tank

and the resonant frequency of the tank circuit. The parallel circuit of Figure 2.18 (b) without the varactor has a radian resonant frequency $\omega_o = 1/\sqrt{LC}$ and a Q , defined as $Q_o = \omega_o CR$. The value of Q_o will be used as a measure of the Q degradation by the varactor. With the varactor present, the resonant frequency is $\omega_{oV} = 1/\sqrt{L(C + C_{VP})}$ and this can be varied from ω_1 to ω_2 ($\omega_2 > \omega_1$) by tuning the varactor from zero volt bias to the breakdown bias V_B so that

$$\omega_1 = 1/\sqrt{L(C + C_{V0})} \text{ and } \omega_2 = 1/\sqrt{L(C + C_{VB})}. \quad (2.61)$$

This leads to the resonator tuning range χ defined as $\chi = (\omega_2 - \omega_1)/\omega_1$, which becomes, using (2.57),

$$\chi = \left[\frac{C/C_{VB} + \alpha}{C/C_{VB} + 1} \right]^{1/2} - 1. \quad (2.62)$$

The tuning range, χ , must be reduced to avoid excess shot noise. This is a common situation if a semiconductor junction varactor is used. Thus, in practice, a semiconductor junction varactor is not biased at zero volts. In addition, the consequence of zero bias operation is potentially excessive shot noise of current when the RF voltage swing drives the varactor into forward conduction. However, excess shot noise is not a problem when a BST varactor is biased at zero volts. The effect on the tuning capacitance achieved at low bias is captured by the parameter ε_1 so that the effective maximum capacitance is $\hat{C}_{V0} = C_{V0} - \varepsilon_1$. Both the BST and semiconductor junction varactor produce excess phase noise at high bias voltage near voltage breakdown. Thus the effective minimum capacitance is $\hat{C}_{VB} = C_{VB} + \varepsilon_2$. Then the minimum and maximum VCO tuning frequencies, respectfully, are

$$\hat{\omega}_1 = \frac{1}{\sqrt{L(C + \hat{C}_{V0})}} \text{ and } \hat{\omega}_2 = \frac{1}{\sqrt{L(C + \hat{C}_{VB})}}. \quad (2.63)$$

We can define the effective normalized tuning variable as

$$\chi = (\hat{\omega}_2 - \hat{\omega}_1)/\hat{\omega}_1 \quad (2.64)$$

and therefore using (2.63) we have

$$\hat{\chi} = \left[\frac{\left(\frac{C}{\hat{C}_{VB}} + \frac{\hat{C}_{V0}}{\hat{C}_{VB}} \right)}{\left(\frac{C}{\hat{C}_{VB}} + 1 \right)} \right]^{1/2} - 1. \quad (2.65)$$

The significance of this expression is that the fractional frequency tuning range is put in terms of the capacitances at the extremes of the tuning range plus the capacitance of the tank circuit. A more convenient form for design is obtained by defining the effective varactor tuning capacitance ratio as

$$\hat{\alpha} = \frac{\hat{C}_{V0}}{\hat{C}_{VB}} \quad (2.66)$$

and so (2.65) using (2.66) is written as

$$\hat{\chi} = \left[\frac{\frac{C}{\hat{C}_{VB}} + \alpha}{\frac{C}{\hat{C}_{VB}} + 1} \right]^{1/2} - 1. \quad (2.67)$$

Hence, $\hat{\chi}$ is less than χ reduced by the size of the RF swing and by shot noise considerations when the instantaneous voltage across the varactor approaches forward conduction (for a junction varactor) or breakdown (for both the junction and BST varactors). Starting with the key expression of (2.67), we expand this in terms of the resistance ratio R/R_S and note that $R/R_S = Q_o Q_V C_V / C$. In the same step we use the relation that the Q of the tank circuit is $Q_o = \omega_{0V} RC$ at the resonant frequency, ω_{0V} of the varactor-loaded tank circuit. The minimum and maximum resonator Q 's occur at the maximum and minimum varactor capacitance which are bounded by the forward bias and breakdown voltages respectfully. Varactors have limited Q and generally much less than that of the tank circuit (i.e. $Q_{VM} \ll Q_o$ and $q \gg 1$). Therefore, from a design perspective, it is key to understand the trade-off in oscillator tuning bandwidth with varactor available Q , since the varactor Q directly influences the oscillator phase noise.

In [94], we define a Q degradation factor, introduced as ρ , which provides the ratio of the tank Q with the varactor, to the tank Q without the varactor. However, unlike the parameter q , introduced earlier in (2.56), ρ provides the Q reduction factor explicitly in terms of the

tunability of the oscillator. These tunability parameters are the available capacitance shift of the varactor, α , and $\hat{\chi}$, a normalized tuning range which is a design parameter. Therefore, $\rho = f(\alpha, \hat{\chi}, q)$.

The development of this relation begins by expanding (2.65) in terms of the resistance ratio R/R_S and noting that $R/R_S = Q_0 Q_V C_V / C$. In the same step we use the relation that the Q of the tank circuit is $Q_0 = \omega_{0V} RC$ at the resonant frequency, ω_{0V} of the varactor-loaded tank circuit. This results in

$$Q_{0V} = \frac{Q_0}{1 + \frac{Q_0 C_V}{Q_V C}} + \frac{Q_0 (Q_V / Q_0)}{1 + \frac{Q_V C}{Q_0 C_V}}. \quad (2.68)$$

The minimum value of this Q_{0VM} occurs when the varactor Q is minimum, i.e. $Q_V = Q_{0VM}$, which corresponds to maximum varactor capacitance, i.e. $C_V = C_{VM}$. Thus

$$Q_{0VM} = \frac{Q_0}{1 + \frac{Q_0 \hat{C}_{V0}}{Q_{VM} C}} + \frac{Q_0 (Q_{VM} / Q_0)}{1 + \frac{Q_{VM} C}{Q_0 \hat{C}_{V0}}}. \quad (2.69)$$

Applying the effective varactor capacitance tuning factor from (2.66) results in

$$Q_{0VM} = \frac{Q_0}{1 + \frac{\hat{\alpha} Q_0 \hat{C}_{VB}}{Q_{VM} C}} + \frac{Q_0 (Q_{VM} / Q_0)}{1 + \frac{Q_{VM} C}{\hat{\alpha} Q_0 \hat{C}_{VB}}}. \quad (2.70)$$

The next step is to remove specific reference to capacitance values and instead introduce the normalized tuning variable $\hat{\chi}$. Upon rearrangement and using (2.66), (2.62) becomes

$$(\hat{\chi} + 1)^2 = \frac{C / \hat{C}_{VB} + \hat{\alpha}}{C / \hat{C}_{VB} + 1}. \quad (2.71)$$

Rearranging again we obtain

$$\frac{C}{\hat{C}_{VB}} = \frac{\hat{\alpha} - (\hat{\chi}^2 + 2\hat{\chi} + 1)}{\hat{\chi}^2 + 2\hat{\chi}}. \quad (2.72)$$

Using the Q load factor from (2.56), we can now write the Q degradation factor in terms of the oscillator tuning parameters, $\hat{\alpha}$ and $\hat{\chi}$ and the Q loading factor, q . Consequently we can

write the Q degradation factor as

$$\rho = \frac{Q_{0VM}}{Q_0} = \frac{1}{k} + \frac{k}{q} \quad \text{where } k = \left(\frac{q\hat{\alpha}(\hat{\chi}^2 + 2\hat{\chi})}{\hat{\alpha} - (\hat{\chi} + 2\hat{\chi} + 1)} + 1 \right). \quad (2.73)$$

This is a central result of this work, as the factor $1/\rho^2$ is directly proportional to the phase noise shown in (2.44) in the absence of excess noise sources. In summary, (2.73), provides the ratio of the minimum Q , (Q_{0VM}) of the tank circuit with the varactor to the Q , (Q_0), without the varactor for a specified normalized frequency tuning factor, $\hat{\chi}$, and available capacitance tuning range, $\hat{\alpha}$. The factor q is a design parameter, while Q_{0VM}/Q_0 determine phase noise degradation through the oscillator signal-to-noise equation of (2.44) which is directly impacted by the tank or resonator Q . Therefore, ρ , is an important parameter in design.

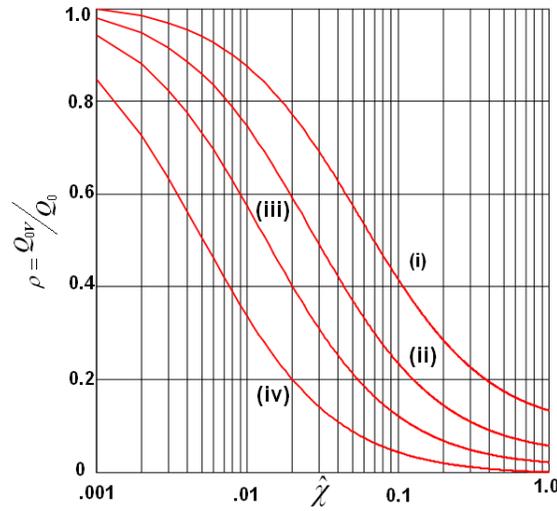


Figure 2.19: The calculated Q reduction factor versus the normalized tuning variable, $\hat{\chi}$, for $\hat{\alpha} = 2$ for various normalized quality factors: (i) $q = 5$; (ii) $q = 10$; (iii) $q = 20$; (iv) $q = 50$.

In Figure 2.19 the relation between the available tuning range and the reduction in phase noise is illustrated. The set of four parametric plots hold $\hat{\alpha}$ constant at a value of 2. This represents the effective capacitance change from a tuning voltage of zero volts to the varactor

breakdown voltage and implies a varactor change in capacitance of 2:1 in all four cases. The family of four plots provide for a range of normalized Q where the normalized Q is defined as the ratio of the varactor Q at minimum capacitance (approaching the breakdown voltage) to that capacitance at zero volt bias. Therefore, line plot (i) would represent the lowest Q reduction factor by virtue of a varactor with a Q $1/5^{\text{th}}$ of that at breakdown voltage while operating at zero volt bias. Hence, line plots (ii) through (iv) represent correspondingly worse case varactor Q 's in so far as the corresponding reduction in tuning range is apparent in $\hat{\chi}$ as this continually lessens for a specific Q reduction factor.

Tunability, the interaction of the resonator with the active device, and developing sufficient stable output power over a bandwidth of 10% or greater of the operating frequency are addressed in Sections 2.5.2, 4.4.2, 4.6.6, and 5.1.3. There are a number of clear attributes associated with the BST varactor, and a number of these are addressed and compared with other varactor types and specifically with the semiconductor junction varactor.

In this section we addressed the physical characteristics of the varactor required to achieve a specified tuning range while targeting a required carrier signal-to-noise ratio. These parameters are interrelated and the relationships will change if the oscillator architecture is changed. Examples of alternative architectures are ones that include switched reactance resonators, multiple resonator cores, and power combining of multiple sources. In this section the resonator with varactor was in shunt with a single active device. The ultimate result of this section was a formulation relating the tunability, phase noise, and the ratio of the loaded to the unloaded resonator Q .

2.6 A resonator-device interface for improved phase noise

Wide tuning range and operating phase noise are at opposition for performance. Nevertheless, there are some advantageous topologies which provide a reasonable trade-off. In this section we identify the problem of optimizing the loaded impedance of the resonator, delivering sufficient power from the resonator to the active device to maximize signal-to-noise ratio, and finally

extending the tuning range.

We would like to find an explicit expression between the required impedance transformation between the resonator, device, and the tuning range for a specific set of component values. In essence, a synthesis procedure. One such topology is presented in [95]. In this work a discussion of a transmission line with adjustable tap position permits optimizing the impedance transformation between the resonator and the active device. The same effect could be implemented with an adjustable reactance network, for example, capacitive tap, so-called Colpitts configuration, or inductive tap, Hartley configuration. The Hartley configuration is advantageous, since this topology minimizes the capacitive loading and the dilution of varactor tuning effectiveness however, it is difficult to implement at high frequencies. Hence realizing the network in a transmission line format is preferred. Shown in Figure 2.20 is the proposed network. A variation of the network was presented in [96]. A simplified form of the network permits increasing the effective Q of the varactor. A series capacitor with the varactor with a larger reactance and larger unloaded Q will improve the composite Q of the capacitive branch. This is at the expense of a reduced tuning range. The derivation of the Q improvement is in the literature [104], although the results are inverted. Therefore, we restate the results here and briefly present the derivation.

The unloaded Q of a single capacitor Q_1 is given by $Q_1 = 1/\omega C_1 R_1$. The effective capacitance of series capacitors is $C_t = C_1 C_2 / (C_1 + C_2)$ and the effective series R is $R_t = R_1 + R_2$. Therefore, the total Q is

$$Q_t = \left(\frac{1}{\omega \frac{C_1 C_2}{C_1 + C_2} (R_1 + R_2)} \right). \quad (2.74)$$

This is written in a more convenient form in terms of the individual capacitors and their unloaded Q values as

$$Q_t = \frac{(C_1 + C_2) Q_1 Q_2}{C_2 Q_2 + C_1 Q_1}. \quad (2.75)$$

An example, if equal capacitors are used with identical Q then the effective Q is doubled, a significant improvement.

The series stacking or “anti-series” connection of varactors permits the reduction of signal voltage developed across each varactor. If the varactors are matched in value and tuning characteristic, then the voltage is divided equally, $1/n^{\text{th}}$ of the impressed RF voltage delivered from the resonator, where n is the number of stacked varactors. This action reduces signal distortion and increases the AC voltage breakdown, however not the DC breakdown. Nevertheless, improved oscillator tunability and reduction of signal distortion is achieved. The design task is to identify the required resonator embedding element values to realize a specified tuning range given, the varactor properties, resonator reactance, and the active device present with feedback. The solution is fairly straightforward for a simplified form of the network of Figure 2.20, whereby C_1 is eliminated. In this case no impedance transformation between the resonator

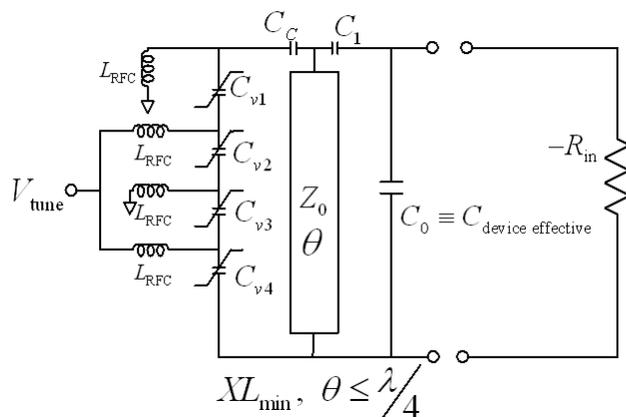


Figure 2.20: Varactor anti-series stack and capacitive tapped transmission line resonator

and the active device is implemented. However, the effective Q of the varactor is improved as discussed earlier. We address this design problem firstly and then consider the second case where both C_1 and C_c are both present. In this analysis it is understood that the device active reflection coefficient is well behaved and appropriately complements the resonator tuning characteristic. That is, there are no secondary resonances, or non monotonic reactance changes over the tuning frequency range of interest. These issues are addressed in more detail in Section

4.4.2. Consider the case where the device effective input impedance is large, this includes the input reactance and consequently the device input capacitance is neglected. For convenience C_c is identified as simply C and the entire varactor stack has total capacitance C_v , which is a function of the incremental AC RF voltage plus the DC component of the tuning voltage. In this discussion, the incremental AC component is much less than the DC component. Furthermore, the varactor capacitance range extends from $C_{v\min}$ to $C_{v\max}$, a direct function of the tuning voltage. Then the resonator radian frequency is proportional to the range of C_v as

$$\omega_0^2 \propto \frac{1}{C_v} + \frac{1}{C} = \frac{1}{C_T} \quad (2.76)$$

$$\omega_{\max}^2 \propto \frac{1}{C_{v\min}} + \frac{1}{C} = \frac{1}{C_{T\min}} \quad (2.77)$$

$$\omega_{\min}^2 \propto \frac{1}{C_{v\max}} + \frac{1}{C} = \frac{1}{C_{T\max}}. \quad (2.78)$$

Let the tuning ratio, x , define the ratio of the maximum and minimum carrier frequency. Therefore,

$$x^2 = (\omega_{\max}/\omega_{\min})^2 \geq 1 \quad (2.79)$$

and from (2.76),(2.77),(2.78) it follows:

$$x^2 = \frac{\frac{1}{C} + \frac{1}{C_{v\min}}}{\frac{1}{C} + \frac{1}{C_{v\max}}}. \quad (2.80)$$

As in (2.57), will explicitly define α as a function of $C_{v\max}$ and $C_{v\min}$ and not necessarily include the extreme limit points of zero volts and breakdown, however in general, we have $\alpha = C_{v\max}/C_{v\min}$ and (2.80) is conveniently written as

$$x^2 = \frac{C_{v\max} C_{v\min} + C}{C_{v\min} C_{v\max} + C} = \alpha \frac{C_{v\min} + C}{C_{v\max} + C}. \quad (2.81)$$

The results of (2.81) provide the required varactor coupling capacitance explicitly as a function of the desired tuning ratio. We therefore see as the desired tuning ratio approaches the root of the varactor capacitance change, the value of the coupling capacitance approaches infinity or a short circuit as we have,

$$C = C_{v \min} \frac{x^2 - 1}{1 - x^2/\alpha} . \quad (2.82)$$

The tuning sensitivity of an oscillator, K_o , is a function C and α , both terms are expressed in terms of the tuning ratio, x . The oscillator tuning gain is given by

$$K_o = \frac{\omega_{\max} - \omega_{\min}}{V_{\max} - V_{\min}} = \frac{\omega_{\max} - \omega_{\min}}{\Delta V} . \quad (2.83)$$

This is rewritten in terms of the tuning ratio, x and thus

$$K_o = \omega_{\min} \frac{x - 1}{\Delta V} . \quad (2.84)$$

The maximum frequency of oscillation is defined as

$$\omega_{\max}^2 = \frac{1}{L_{\min} C_{T \min}} . \quad (2.85)$$

Now using (2.77) and (2.82) substitution into (2.85) yields the required minimum resonator inductance in terms of all the other predefined element values associated with the oscillator and resonator design. We have therefore,

$$L_{\min} = \left(\frac{x^2}{x^2 - 1} \right) \left(\frac{\alpha - 1}{\alpha} \right) \left(\frac{1}{C_{v \min} \omega_{\max}^2} \right) . \quad (2.86)$$

This result is central to the design of the resonator. However, its imperative that the active device interface as stated earlier is appropriately designed to provide stable loop gain. This is irrespective of how the loop gain is provided, either by an open loop two-port amplifier with

corresponding open loop phase shift and gain, or secured via a negative reflection coefficient one port implementation.

Next, the previous development is extended to include the composite Q of the varactor and series varactor coupling capacitance, all in terms of the parameters x and α . The effective Q of the composite, comprising a series varactor and series coupling capacitor, was developed earlier as Q_t . We will refer to the effective Q of the composite as the enhanced Q or Q_i . Then using the previous development for the improved Q we have

$$Q_i = \frac{Q_v \left(1 + \frac{C_v}{C}\right)}{1 + \frac{C_v Q_v}{C Q_C}} \approx Q_v \left(1 + \frac{C_v}{C}\right) \text{ for } Q_C \gg Q_v \quad (2.87)$$

where Q_C is the varactor coupling capacitance Q evaluated at the mean oscillator frequency, and the varactor Q , Q_v , is taken at the same mean oscillator frequency, however at V_{tune} specified at V_{min} . Now the coupling capacitance, C takes on the value specified by (2.82). Substitution into (2.87) yields

$$Q_i = Q_v \left(1 + \frac{C_v}{C_{v \min}} \frac{\left(1 - \frac{x^2}{\alpha}\right)}{(x^2 - 1)}\right) . \quad (2.88)$$

The highest varactor Q occurs at $C_{v \max}$ and the lowest at $C_{v \min}$. Then using (2.88) and α , expanding and simplifying, a set of enhanced low and high Q values are found as

$$Q_{iL} = Q_{v \min} \left(\frac{\alpha - 1}{x^2 - 1}\right) \quad (2.89)$$

and

$$Q_{iH} = Q_{v \max} \left(\frac{x^2}{\alpha}\right) \left(\frac{\alpha - 1}{x^2 - 1}\right) . \quad (2.90)$$

If we investigate the ratio of the high and low Q values we have the following:

$$\frac{Q_{iH}}{Q_{iL}} = \frac{Q_{v \max}}{Q_{v \min}} \left(\frac{x^2}{\alpha}\right) \text{ if } \alpha \geq x^2 . \quad (2.91)$$

Hence, we find for the enhanced Q operating condition, that the Q of the resonator established

by the varactor Q tends in fact to be constant, dependent on the varactor Q vs. tuning voltage curve. An appreciation of the improved Q and the insensitivity to Q reduction using the series coupling capacitance is noted if we compare two varactor types with tuning ratios of 2 and 8 respectfully. However, for this case study, consider that we have two varactors with appropriate differences in minimum Q 's of 75 and 15 respectfully. For example, let $Q_{v \min} = 75$, $\widehat{Q}_{v \min} = 15$, $\widehat{\alpha} = 8$, and $\alpha = 2$. Then we have

$$\frac{Q_i}{\widehat{Q}_i} = \frac{Q_{v \min} \alpha - 1}{\widehat{Q}_{v \min} \widehat{\alpha} - 1} = 1.25 . \quad (2.92)$$

A varactor Q variation of 5:1 produces a variation of 1.25:1 in over-all Q of the capacitor network. Hence, a low Q varactor does not necessarily limit the over-all resonator Q and in fact the combination of inductive reactance of the resonator in combination with the dynamic impedance of the active device usually plays the dominant role in setting the loaded resonator Q .

Consider the case where the shunt capacitance C_o is not neglected. As an example, this capacitance could be due to the active device input capacitance in a common collector series feedback oscillator. Therefore, a shunt input capacitance is present which consists of the device capacitance plus the series feedback capacitance and all associated parasitic capacitance. The resulting total parallel capacitance is C_o . Therefore, (2.82) must be modified. A similar analysis is followed and the value of the coupling capacitance is found in terms of the varactor parameters and the tuning range. The value of C_o will influence the required coupling C and the x attainable for a given α . The coupling C is now the solution to a quadratic and is written as

$$C_{\text{coupling}} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \quad (2.93)$$

where $a = x^2 \left(1 + \frac{C_o}{C_{v \min}}\right) - \left(\alpha + \frac{C_o}{C_{v \min}}\right)$, $b = (x^2 - 1) \alpha C_{v \min} + \alpha C_o + C_o$ and $c = (x^2 - 1) C_{v \min} C_o \alpha$. The value of L_{\min} is solved in a same manner to that used in developing (2.86). The derivation of the complete network of Figure 2.20 is similar in approach. The network shown in Figure

2.20 is flexible in that it provides impedance transformation between the resonator and the active device, as well as establishing the improvement in varactor Q , varactor linearity, and reduction in distortion. The resulting solution is involved and the result for the varactor coupling capacitance is found using Maple©. The resonant frequency of the network shown in Figure 2.20 is straightforward. The oscillator tuning ratio, x^2 , is found by the same process previously used in developing 2.81 and is given by,

$$x^2 = \frac{\frac{C\alpha C_{v\min}}{C+\alpha C_{v\min}} (C_o + C_1) + C_1 C_o}{\frac{C C_{v\min}}{C+C_{v\min}} (C_o + C_1) + C_1 C_o}. \quad (2.94)$$

The resonator minimum inductance is found as in the prior analysis and is a function of all of the resonator capacitances and the maximum required operating frequency, ω_{\max} . The varactor minimum and maximum capacitance are known, the shunt capacitance, C_o is known, and C_1 is chosen to provide an appropriate impedance transformation between the device and resonator. Therefore, the only variable needed is $C_{\text{coupling}} = C_c$. This expression involves x^2 , α and all remaining network capacitance. Finally, the minimum inductance is found from the maximum operating frequency and the total resonator capacitance. The value of the coupling capacitance is again a solution to a quadratic equation,

$$C_{\text{coupling}} = \frac{(1 + \alpha) (C_1 C_o - x^2 C_1 C_o) - (x^2 \alpha C_{v\min} - \alpha C_{v\min}) (C_o + C_1)}{2(x^2 C_{v\min} - \alpha C_{v\min}) (C_o + C_1) + C_1 C_o (x^2 + 1)} \pm \gamma \quad (2.95)$$

where the value γ is the discriminate of the quadratic solution and is given by the **square root** of the sum of 8 consecutive terms as follows:

$$\gamma = -2C_1^2 C_o^2 x^2 + C_1^2 C_o^2 + x^4 C_1^2 C_o^2 + 2C_1 C_o^2 \alpha C_{v\min} + \gamma_2 \quad (2.96)$$

$$\gamma_2 = \alpha^2 C_{v\min}^2 C_1^2 + C_o^2 \alpha^2 C_{v\min}^2 - 4x^2 \alpha^2 C_{v\min}^2 C_o C_1 - \gamma_3 \quad (2.97)$$

$$\gamma_3 = 2x^4 \alpha C_{v\min} C_o^2 C_1 - 2x^2 \alpha^2 C_{v\min}^2 C_1^2 - 2x^2 \alpha^2 C_{v\min}^2 C_o^2 + \gamma_4 \quad (2.98)$$

$$\gamma_4 = 2x^4\alpha^2C_{v\min}^2C_oC_1 + x^4\alpha^2C_{v\min}^2C_1^2 + 2C_1^2C_o\alpha C_{v\min} + \gamma_5 \quad (2.99)$$

$$\gamma_5 = x^4\alpha^2C_{v\min}^2C_o^2 - 2x^4\alpha C_{v\min}C_1^2C_o + 2C_o\alpha^2C_{v\min}^2C_1 - \gamma_6 \quad (2.100)$$

$$\gamma_6 = 2x^4C_1^2C_o^2\alpha - 2C_o^2\alpha^2C_{v\min}C_1 + x^4\alpha^2C_1^2 - 2\alpha^2C_{v\min}C_1^2C_o + \gamma_7 \quad (2.101)$$

$$\gamma_7 = 2x^4\alpha^2C_{v\min}C_o^2C_1 + 2x^4\alpha^2C_{v\min}C_1^2C_o + 4C_1^2C_o^2x^2\alpha - 2C_1^2C_o^2\alpha^2x^2 - \gamma_8 \quad (2.102)$$

$$\gamma_8 = 2C_1^2C_o^2\alpha + C_1^2C_o^2\alpha^2 \quad (2.103)$$

The resulting value for the varactor coupling capacitance is a positive real value and is normalized to $C_{v\min}$.

An example is instructive. Consider device plus feedback capacitance totaling 3.9 pF. The varactor has the following parameters: $\alpha = 11.5$ and a given $C_{v\min} = 1.4$ pF, and a $C_{v\max} = 16.1$ pF. The desired maximum and minimum frequency range is 0.96 GHz to 1.33 GHz and therefore $x = 1.39$. An impedance transformation consists of increasing the parallel equivalent real part of the active device Z_{in} at .96 GHz. So with a given open loop gain, the doubly loaded Q of the resonator meets a particular objective, for example loaded Q or tuning range. The doubly loaded Q comes about due to a portion of the loading contributed directly by the resonator, as well as the loading by the active device. For the purpose of this discussion we will neglect the unloaded Q of the varactor and the inductive reactance portion of the resonator. Since the reactance of the resonator is not completely known at this point, i.e. L_{\min} has not been determined, this process is iterative. If a series C_1 of 5.1 pF is chosen, then to meet all other objectives, the required varactor coupling capacitance is 5.6 pF and the minimum inductance is 4.3 nH. This is readily obtained using a shorted transmission line or using a discrete inductor.

A detailed treatment of the open and closed loop Q including analysis is addressed in [106], while the resonator-device interface are treated in Chapter 5 and Section 4.4.8. Briefly, the transformation Q is initially dependent on the open loop device small signal input impedance, and then the large signal input impedance as the device self limits. Upon the oscillator loop

closing, the required loaded Q results.

The series feedback capacitance in the common collector configuration provides a reflection coefficient greater than unity and consequently a negative input real component shunted by capacitance. The transformation Q depends on what portion of the real series positive impedance is presented to the device. A value which is excessively large will reduce the loop gain and ultimately prevent the oscillator from starting up. For example, a series capacitance, C_1 of 5.1 pF presents an equivalent reactance at 0.96 GHz of $33\ \Omega$. A series resonator resistance must have a positive resistive loss less than the negative resistance associated with the active device. A typical negative R value from the active device is $-30\ \Omega$. If we permit the series resonator and associated interconnect losses to be a third of the device maximum negative resistance, R_{loss} is $10\ \Omega$. Then the series capacitance supports a transformation resistance of 119 ohms and the loaded Q is 4 at 0.96 GHz. A reduction in C_1 value will increase the transformation R and increase the resulting loaded Q . If a value of 2.2 pF is used for C_1 , the varactor coupling capacitance required is 4.2 pF and L_{min} increases to 5.8 nH. All other parameters remaining the same, the maximum and minimum tuning range are exactly met. The loaded Q then increases to 17. As the coupling is decreased the loaded Q potentially increases however, the signal-to-noise ratio will not necessarily improve. In part this is due to the reduction in extracting power from the active device and delivering increased power to the resonator. So an optimum trade-off exists and an approach presented in reference [105] is discussed in Section 4.4.8. There we see that for an optimum power match between resonator and device, optimum loaded Q is 1/2 the resonator unloaded Q . This approximation was used earlier in estimation of the oscillator noise floor.

The relationship among the parameters becomes quickly apparent and combinations of varactor α with the desired x can lead to resonator reactance which is either impractical or unrealistic. In the case of the coupling capacitor elements, the transformed Q values are too low or the varactor coupling forces the resonator signal voltage to exceed varactor breakdown. If the oscillator tuning ratio, x , required increases relative to the α accommodated by the

given varactor, then the varactor coupling capacitance increases and the loaded Q reduces accordingly. Nevertheless, the ability to vary the loaded resonator Q while meeting the tuning agility requirements of the oscillator in design is key.

2.7 Conclusions and summary

This chapter provides the ground work in understanding the system issues and motivation for alternative RF architectures. Specifically the need to address the noise in cascaded systems and why a feedback architecture such as the phase lock system would be an attractive solution to the transmitter function. The phase lock multiplier and the power transfer oscillator are identified as two architectures amenable to a direct RF carrier approach. The power oscillator is key to their implementation and therefore discussions of the active device and the resonator interface are developed. A proper resonator- device interface is necessary to permit stable tuning of the oscillator and equations derived for synthesis of a suitable topology are developed.

In addition, this chapter focused on the comparison of several implementations for realizing the microwave transmitter functions. The heterodyne, homodyne, and variations which rely on frequency translation networks are contrasted against the method of direct carrier generation. The analysis of both systems requires the ability to process various types of noise, AM, PM, and the composite of both or pure noise. We find these noise levels must be base lined against the relative signal levels in order to find the desired carrier power and modulation to meet a prescribed dynamic range. The primary system blocks involved in frequency translation systems include amplifiers which may need to operate near compression, power amplifiers, mixers, and attenuators. While similar system blocks are available in direct carrier generation architectures, such as the PLM, the use of translation networks is minimized. Instead, the phase lock system is emphasized as this function provides intrinsic selectivity, minimum generation of intermodulation and potentially higher efficiency.

While noise is one underlying limitation in translation systems, direct carrier generation must contend with a second, microphonics. A PLM network is characterized for microphonics

and the relation between phase lock loop dynamics and the reduction of mechanically induced vibrations is noted. Details of this treatment are in Section 5.1.5.

The introduction of modulation is efficiently accomplished by introducing baseband signals directly into the locked frequency multiplier and permitting the loop to provide compensation for the frequency response directly. Multiple loops can be cascaded. Each loop transfers noise characteristics of that loop to the next provided the bandwidth of the loops are appropriately set. For the case of identical operating frequency loops, each loop transfers the power from one source to the next. In effect a small signal tunable oscillator whose phase noise is significantly better by virtue of optimizing the power is transferred to a larger power oscillator device where efficiency is optimized. Cascaded loops are not unlike cascaded amplifiers however without the impediment of intermodulation. The need to extract power from an oscillator and maintain a given signal-to-noise ratio is addressed. An explicit relation between the desired load power and the required signal power to meet objectives is found. The relation of varactor Q and resonator tuning range is described in terms of the physical parameters of the varactor and emphasized in our work is the BST varactor. In addition, we investigate the unloaded Q characterization of the varactor. The Q of the BST-IDC varactor follows an inverse frequency curve and a packaged unit is investigated with a self resonant frequency greater than a 1 GHz, and a Q of 12. Our goal is finding techniques to improve the Q , however, without significant reduction in tuning. A resonator network is presented that is used to improve the device-resonator interface with a given varactor specified and the solution to element values specific to set of design goals is found.

In summary, we found an explicit expression in terms of the required tuning range of the resonator. This expression included the varactor capacitance ratio between zero applied tuning voltage and the maximum permitted; a key design parameter. Using these parameters, we are able to find the required enhanced Q of the varactor and the interface between the resonator and the active device. The central result yields an exact solution to the transmission line resonator reactance required, and the coupling reactance between the varactors, the transmission line,

and the interface to the active device. We find that there is a clearly defined trade-off between the decrement in the unloaded Q of the resonator to the loaded Q value for a given phase noise performance and desired tuning range. If the reduction in phase noise performance is to be minimized, and the tuning range is to be maximized, then clearly the reduction in unloaded to loaded resonator Q must be minimized. For the varactors studied here, the acceptable range in capacitance and eventually range of the Q value, is constrained by a tuning voltage near zero volts and voltage breakdown. In the case of the BST varactor, we will find that in system applications of BST based tunable oscillators, the lower bound of tuning voltage must be actually greater than zero volts.

Chapter 3

Alternative Architectures, Circuit Topologies, and Related Work

3.1 Introduction

Systems planning is key to current microwave transmitter designs which are based on heterodyne or low IF architectures. However these systems are costly, demonstrate efficiencies as low as a couple of percent to achieve linearity, and involve multiple hardware disciplines in order to best balance tradeoffs. In these sections we review several alternative architectures which aim to address these problems. Currently both baseband and intermediate frequency conversion stages are amenable to IC techniques. This includes both lower frequency RF and modulation sections of the transmit function. The majority of the additional design overhead and challenges are in terms of power consumption and complexity which comes about through managing the power amplifier, controlling amplifier linearity, calibration, gain control of lower level RF stages and finally in frequency generation circuitry. Emphasis in this work is to minimize and potentially eliminate heterodyne systems in favor of direct carrier modulation and generation. This approach reduces the potential generation of spurious signals and the power consumption overhead of multiple frequency generation circuits. The power oscillator and interface network

are a key focus element. This includes the choice of active device, topology, structure of the resonator, and tuning control.

In addition to focusing on block architectures, we also find the need to consider alternative circuit topologies. Device technology for RF power generation encompassing FET and bipolar devices appears in various configurations; the most popular of which is the series feedback common gate or common base. This is due to the ease of achieving wide frequency tuning bandwidth [116]. Other avenues consider multiple tuning ports utilizing both the resonator branch and feedback port and arranged in a series feedback configuration [117]. However at high RF power levels, above several watts, these configuration are challenging to design. This is particularly an issue in packaged form as opposed to chip and die format where package parasitics will limit bandwidth. In either form, the challenge is the extraction of heat. Several approaches include operation of the FET in inverse mode permitting grounding both thermally and electrically the drain branch of the FET. Circuits were investigated in [118]. The common source or common emitter and specifically the grounded source or common emitter bipolar with resistor ballasting is the most widespread topology used for power amplifier devices. Low inductance common node via's (source or emitter) to the substrate and ground are efficient for the removal of heat and for maximizing power gain. These attributes and differences from other oscillator topologies must be properly handled to permit realizing a stable tunable power oscillator in a *grounded* source or emitter configuration. Tuning range and the tradeoff in phase noise performance is addressed in section 2.5.2. Achieving adequate stable bandwidth, without abrupt changes in output power or frequency is required. In section 2.5.2 and future sections discussion of the varactor and tuning range is fundamental and the prior work of addressing stable oscillator tuning is emphasized.

In these sections we consider alternative direct and phase locked sources. The fundamentals of oscillator operation and their applications are applicable to all of the alternative systems highlighted in this chapter however, the use of the power oscillator is unique in that the requirement for linear high power amplifiers is removed. Also the main attraction of the PLM

architecture is minimizing and possibly elimination of frequency translation networks. Thus the reduction of spurious signal generation is another additional benefit.

3.1.1 Overview of specific techniques studied...alternatives to direct carrier generation transmit function

Various forms of direct carrier generation and direct carrier launch systems are available. A basic form uses translation “mixer mix-up” topology. In this arrangement the local oscillator source is nearly at carrier frequency and the modulation function is essentially operating at baseband. The mixer topology utilizes a set of in-phase and quadrature channels, so-called IQ format in design and directly supports complex modulation. The associated problem with this architecture is the need for low level power gain stages, buffer amplifiers, followed by high linearity power amplifiers. The introduction of spurious via mixers discussed earlier in this work is still present and the choice of the location of the IF channel critical. Maintaining linearity is essential in the following gain stages, while also maintaining an IQ mixer circuit function which achieves a large dynamic range.

A constant phase shift modulator, gaussian minimum shift keying with reference modulation and multiplication is introduced in [119]. This system relies on the phase lock loop to provide tracking but modulation is not introduced into this loop for compensation. Instead modulation and compensation is introduced and restricted to the reference oscillator. An extension to complex modulation in these particular phase locked systems is introduced via envelope modulation outside the loop, utilizing a PIN modulator, or the use of polar modulation [120]. However, this system relies on the introduction of the modulation via the power amplifier.

Pulse-injection locking and injection locked oscillators (ILO), are historic and applicable as direct carrier generation systems. The ILO is a first order phase lock system. Introduction of modulation and phase noise performance are not primarily addressed, while locking bandwidth control is primary focus. Pulse-injection ILO attempts to reduce power consumption compared to a PLM and is operated as phase lock multiplier. Phase noise of the open loop ILO is large

but corrected in the ILO condition as a first order loop however, the degree of noise correction is usually inadequate as there is insufficient open loop gain. Hence, noise is still excessive for complex modulation systems. Introduction of modulation is not discussed in current literature.

Direct conversion transmitters, offset phase lock systems, and methods of wide band phase locking with the reduction in noise are addressed by a number of authors. The main focus of these works is providing an integrated circuit design. The addition of a high power amplifier is required in all of these systems to achieve sufficient power output.

Parallel locking of multiple sources, each individually phase locked systems, is applicable from nano-scale sources to high power. The topology is analogous to power combining networks via corporate combining. Introduction of complex modulation needs attention.

3.2 GMSK constant phase modulators by reference multiplication

A GMSK modulator with a phase lock loop operates as a phase locked source with multiplication of unity. The reference operates at carrier frequency. An integral part of the reference source is the implementation of a linear phase shifter. This is accomplished by using a frequency multiplier at the output of a highly linear fractional phase shifter. Linear narrow phase range, phase modulation, is introduced by the method of indirect FM. A multiplication value of $N \geq 5$ is selected to minimize the phase distortion and achieve the required final deviation. Larger values of N are appropriate to extend linearity. Increased division prior to the phase detector reduces the required linear region required by the detector, however phase noise is increased. Consequently, the tracking phase lock loop bandwidth is not free to choose as noise power increases and there is crucial tradeoff between linearity, signal to noise ratio, and compromising loop bandwidth and consequently output VCO stability. The linearity of the phase detector plays an essential role in minimizing modulation distortion, and the transfer function of the loop is tailored to provide a desired closed-loop Gaussian filter response. The block diagram of

the system as compared to a system where modulation is introduced at multiple points within the same loop is highlighted in Figure 3.1.

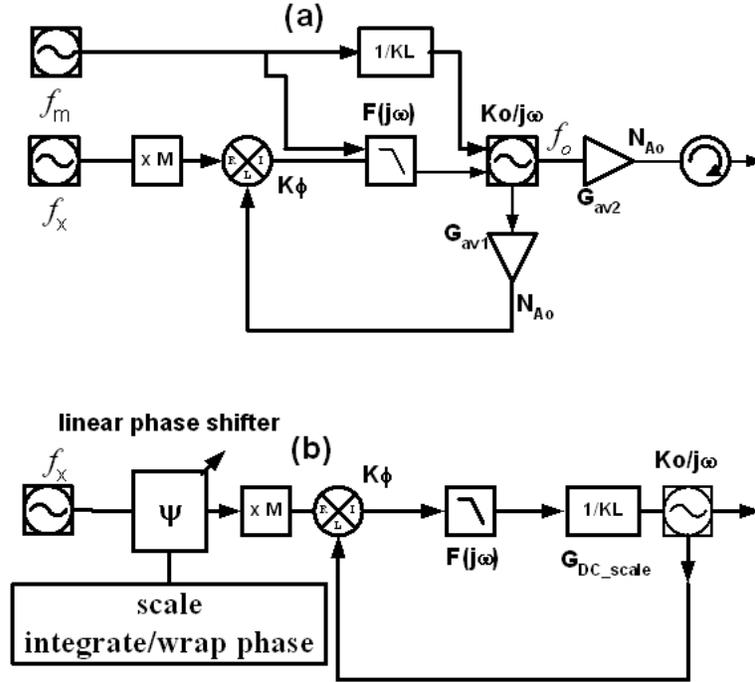


Figure 3.1: Phase locked power oscillators (a) this work using multi-point modulation in multiply loop, (b) a GMSK modulator with linear phase modulator introduced via the reference source.

While both loops require scaling and some form of compensation, the multi-modulation points within a single loop permits the loop to provide the compensation. The only scaling required is if modulation were introduced instead at point (b), at the reference oscillator port. The frequency deviation will be potentially different as the VCO tune gains are different. Care is required in both systems to tailor loop response, peaking should be kept to a minimum as distortion rises near the loop bandwidth frequency in the single loop modulation method. This is detailed in Section 2.4.

3.3 Injection locked oscillators and pulse-injection locking

An injection locked oscillator is a first order phase lock loop. The oscillator resonator double duties as the source resonator and the baseband equivalent of the resonator operates as the loop compensator. The lockup of the oscillator (referred to as the slave oscillator, and in our case the VCO) to the master (in prior referrals, the reference) is a function of the relative powers of each source, the Q of the slave oscillator resonator, and the operating frequency [121, 122]. The relation for determination of the locking range of source to master is an extension to Adler's work and is,

$$\Delta\omega \leq \frac{\omega_o\rho}{Q} \frac{1}{1-\rho^2}. \quad (3.1)$$

The Q is defined as the external quality factor of the slave oscillator resonator, and ω_o is the resonant frequency of the slave oscillator. In the context of the injection locked oscillator, the value of ρ represents the ratio of the level of the injection master oscillator voltage to that of the slave oscillator voltage level. Therefore, ρ is a voltage reflection coefficient and the locking frequency range, $\Delta\omega$ is a function ρ . Therefore, the locking range increases as the injection level increases. Injection locked oscillators can also be phase locked (ILPLL) within the same system with the apparent advantage of improving phase noise. In our work, the phase lock systems addressed, find the free running power oscillator phase noise better than required for complex modulation systems and better than reported in the ILPLL application of [123]. In addition, further improvements are possible with reasonable phase lock loop bandwidth.

3.4 Parallel locking of multiple sources

Multiple sources are coupled or combined to increase output power. They may be individually locked from a common reference or locked to each other as mutual coupled sources, or spatially combined. The use of a corporate combiner topology and directional couplers, similarly applied in PA systems, and injection lock among a plurality of oscillators are the basic techniques. The challenge is obtaining proper phase relationship among a family of sources. A method for

combining the microwave and millimeter-wave power generated by many two or three terminal devices has been investigated. This method forms a single resonant structure from many active devices, and therefore the combiner is stable and does not suffer from simultaneous multimode difficulties. Other technique produces compact structures and are readily adaptable to monolithic integration. Conditions are set to obtain the maximum combining efficiency and a key approach is developed to control the frequency of the combiner. It is shown that the performance of the system is not seriously affected by the dissimilarity of the oscillators used in the combiner. A prototype 84-diode power combiner is constructed and total output power of 1.72 W with combining efficiency of 98.3 percent is obtained at 9.7 GHz. No fundamental limiting factor for the maximum number of devices to be combined was found. These systems do not treat introduction of modulation and only a few were concerned with phase noise levels and none address the presence of spurious signals.

3.5 Offset phase lock loops and sampling (SPD) phase detectors

Offset loops utilize at least one frequency translator. The main motivation is to reduce the counter value N in the main phase lock system and thus improve phase noise, since the counter value multiplies the reference loop single sided phase noise, $L(f)$, discussed earlier via $N \cdot L(f_{\text{ref}})$. Consequently we see potentially a degradation of the VCO noise by the reference phase noise given by $20 \log_{10} L(f_{\text{ref}})$. Nevertheless, value of the offset loop is the advantage of minimizing discrete filters. The offset approach provides the potential for an improved frequency plan. However, the frequency plan of the loops, offset loop and so called output loop, must be arrived at with care if the use of the phase lock loop operating in the role of a filter is to be realized. Multiple phase lock loop systems share a theme which is to “divide and conquer” to achieve technical performance improvements. Each loop operates over a smaller percentage bandwidth than otherwise, and at a lower operating frequency, tending to improve carrier-to-noise ratio. To achieve final operating frequency and required bandwidth, the loops are combined. Final output power levels still require adding power gain stages and power amplifiers with sufficient

linearity. Linearity of phase detector operation and frequency response is key in wideband loops. Digital phase detectors and sinusoidal phase detector-multipliers are available at multi-GHz ranges, However for improvement in operating efficiency, sampling phase detectors provide an advantage. Since they operate on harmonics of the reference and the slaved oscillator, higher operating frequency digital counters can be minimized as well as their larger power consumption.

3.6 Direct conversion transmitters (DCT)

DCT converts the baseband signal directly to carrier frequency. Fundamental are IQ modulators, frequency dividers, and power gain amplifiers. Operating frequency of the VCO is not equal to the final output frequency to prevent load pull modulation while the loops are made as wide as possible to gain noise improvement while also minimizing load pull. An RF PA is required [124].

3.7 Wideband phase locking

Systems providing broadband tracking and locking of oscillators in frequency and phase with additive modulation require the application of careful compensation techniques. Injection lock loops, depending on the frequency tolerance of the slave oscillator and associated temperature drift, requires careful compensation and use of special analog techniques. These include linear voltage-to-current converters, for example when operating with YTO (yig-tuned oscillators). PLL systems utilizing fractional N division are difficult to broadband due to conflicting requirements. First, there is the conflict of spurious signal reduction, requiring a narrow loop, while we desire to minimize higher frequency offset phase noise which would benefit from a wider loop. Various phase noise cancelation techniques are developed through phase detector compensation and linearizing the design of the charge pump operating after the phase detector[125]. Loop bandwidths on the order of under 1 MHz are reported and suppressed spurious signals are demonstrated. Phase noise reported is -106 dBc/Hz at 1 MHz offset from the carrier, which is

not sufficient for microwave QAM systems, but is sufficient for Bluetooth LAN systems.

3.8 Polar modulation

Polar modulation follows the prior architectures discussed, super-heterodyne with IF quadrature modulation and direct upconversion with quadrature modulation. Reducing the complexity and improving the efficiency while maintaining high carrier-to-noise (-162 dBc/Hz at 20 MHz offset) prompt another architecture. Polar modulation prior to the PA, divides the modulation signal into amplitude and phase components. Phase modulation, such as GMSK, is introduced directly through a phase lock loop, while the output of the loop is frequency translated via a mixer and delivered to the PA. At the mixer port, amplitude modulation is delivered. Of course amplitude modulation could also be introduced directly to the PA via supply line variation. The “open loop” form of polar modulation has drawbacks, especially when a significant variation in output power is required. A closed loop polar architecture [126] overcomes these drawbacks.

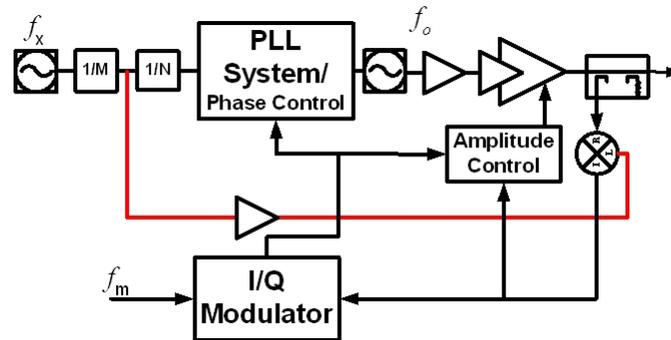


Figure 3.2: Polar modulation system with control loops for amplitude and phase correction.

Closed loops for phase and amplitude are provided by translating the PA output obtained from a directional coupler and translating the IF derived signal as signal inputs to a PLL loop for phase control and a leveling loop for AM control. The PA required must have linearity capabilities comparable to those required for an open loop polar modulation system. The block

diagram as realized is shown in Figure 3.2. Details of limiter amplifiers, bandpass filters, voltage controlled gain amplifiers and detectors required to implement the control loops for amplitude and phase are not shown.

3.9 Summary of related approaches

The basic transmitter architectures all contain in some form frequency translation. The IF channel if chosen low in frequency is integrated with the oscillator source and modulation is dedicated to another circuit function area. A low IF or near zero IF frequency is up-converted via complex modulation with the IQ modulator the basic circuit function. These architectures share a common theme as they are cascaded systems that will require filtering forward of the up-converter output and care in frequency planning. A power amplifier is a separate function and must include all pre-driver amplification stages. Significant on going effort is dedicated to the improvement in the efficiency of the amplifier function. The other “family” of circuit architectures contain a common theme of incorporating some form of feedback system; the phase lock method the most common. Of course combinations of cascade and translate with feedback phase lock are possible, for example the offset phase lock transmitter. The polar modulation approach introduces the modulation in a form that should assist in meeting the goal of power amplifier efficiency. Since the introduction of modulation is subdivided into phase and amplitude components and routed to circuits which favor the processing of those respective signals, DC efficiency is improved. Again, a major advantage of the PLM architecture is minimizing the number of additional sources required, beyond the one only needed to generate the carrier operating frequency.

Chapter 4

Theory of Systems, Power Oscillator Synthesis, and Components

4.1 Introduction

This chapter is first devoted to discussing a methodology of system analysis, based on a circuit block functional contribution method. The details of specific circuit design and synthesis techniques applied to the development of these blocks are then presented. These include oscillator tuning network design via termination mapping, the inclusion of co-simulation designs incorporating electromagnetic (EM) and harmonic balance (HB), and maximizing oscillator instability and oscillator load efficiency.

Additional focus is on oscillators utilizing the BST varactor and their unique properties when applied in a phase lock loop system. The intrinsic tuning linearity of an oscillator which incorporates a BST varactor is highlighted and discussed, and contrasted against the junction varactor when specifically applied in voltage tuned oscillators.

4.2 Overview of theoretical discussions

Circuits, systems, and architectures are inter-twined areas, each dependent on the other for driving electrical performance in the proper direction to achieve an electrical design goal. In this work, the desire is to simplify and improve operating efficiency of microwave transmitters in communication links. The techniques developed are multi-functional and applicable to several diverse areas of RF architecture. Consequently, the theoretical areas to be discussed are both system oriented and circuit oriented, and draw upon several disciplines. These areas include the treatments of noise, control systems, and electromagnetic properties of networks. System analysis targets block RF architectures and their performance for the transmitter function. However, circuit analysis targets the individual aspects such as the RF power oscillator design and synthesis; tuning varactors, the properties of the phase lock loop, and feedback and stability.

In Section 4.3.1 we develop the notion of linking together the RF architectural topology and the system equations describing RF performance. Central to the approach is the idea of an equal stage performance contribution methodology. A receiver preselector is chosen as an example, however the techniques are found to be equally applicable to an up conversion transmitter function.

Oscillator design and the synthesis of appropriate networks to terminate and embed the device are treated in Section 4.4.2. In this section, we find the magnitude of the reflection coefficient of the negative resistance oscillator, a key quantity in satisfying the condition for oscillation at oscillator start-up, as it is correlated with open loop feedback gain [26]. However, the reflection coefficient trajectory versus active device input drive are also important, as it is required to meet specific conditions to insure stable tuning.

As the operating frequency increases, the need to accurately integrate device interconnections with all circuit elements becomes mandatory [82]. Isolating the dependence of device mounting, printed circuit pads, traces, and interconnecting metal lines on the active circuit operation is virtually impossible. Obtaining high agreement between simulation and measurement requires the use of co-simulation techniques [27]. In the treatment presented in Section

4.4.7, the link between nonlinear harmonic balance of active elements, and the electromagnetic effects of passive circuit interconnects is shown to be essential for accurate circuit simulation.

Oscillator load efficiency is addressed in Section 4.5. Efficiency considers the basic operation of the device from a current-voltage perspective. The conversion process of DC to RF power via a nonlinear self-limiting process in a positive feedback loop is the focus of this section. The discussion focuses on the bipolar oscillator design as this unit block function serves as the reference source in the phase locked multiplier. Modified Bessel functions are used as these functions are appropriate in handling the exponential relationship of terminal voltages and currents in describing the bipolar transistor operation. In the appendix, on page 429, the oscillator load efficiency of the FET is addressed.

The properties of ferroelectric varactors are unique as seen in studying their operation in a phase locked application. In Section 4.6.1, it is seen that the control of a tracking PLL is influenced by the characteristics of the BST varactor based VCO. The oscillator load efficiency, or the relationship between converting DC input power to fundamental RF power output, and the excess noise associated with the BST varactor in voltage controlled oscillators are discussed.

The treatment of excess noise considers noise above the level produced by thermal or other methods of noise generation [28]. Therefore, excess noise is defined as levels of noise above and beyond what one would expect from noise generated by nominal levels of voltage or current when impressed across the active device. Oscillator tuning linearity, and the modification of linearity due to leakage current are also treated.

Measurements and characterization of networks and systems are key to the validation of theory. Therefore, a number of special measuring techniques are discussed prior to introducing architectures and synthesis of these networks. This is particularly true in the case of the measurement of the noise in amplifiers and oscillators. In Section 7.2, we discuss two techniques to address measurements of these principal blocks.

4.3 Systems architecture design

4.3.1 Transceiver cascade system synthesis via an equal contribution method

Optimization of the dynamic range of RF systems is treated in this section. Although the target application is the cascade system, the approach is applicable to a cascade with feedback. An algorithm is outlined based on an equal stage by stage contribution method. In lieu of a single stage performance dominance, we consider the concept of balancing the contribution of each of the stages parameters, in order to maximize the system dynamic range. This technique is also identified as an improved point to start further system optimization. In this section we review the treatment of noise and identify the need to separate the properties of noise into a set of orthogonal components. This is required in order to gain a better understanding of how the various system functions will affect the signal and the noise under both small and large signal operation.

The pure noise factor and the AM and PM noise factor of individual contributors of noise must be treated appropriately. A cascaded system consisting of single response transducers, filters, and gain stages was presented in section 2.3. White phase noise power permits the application of the Friss formula in cascaded systems, and the Friss equation is derived based on the assumption that the signal available gain is equal to the noise gain of each of the stages in the cascade [29]. White noise power is additive at the input of each device and in a small signal regime is independent of the carrier power. Thus, the total added noise power when referred to the input of the cascade is used to calculate the noise factor F . The shape of the flicker phase noise spectrum is independent of carrier power. However flicker noise is larger at increased carrier power levels. This is also true of white phase noise when operation of the device deviates from small signal. Thus noise figure and noise output power will depend on signal input power.

Generally, not only will the available power gain change under large signal conditions, however also the noise power generated within a two port. Two elements are responsible for

this change in noise operation of the two port. One is due to physical parameters which are directly influenced by the power level of the input signal; for example, resulting from the shift in the bias currents, increases in temperature, and the onset of shot noise. Second, nonlinear operation leads to frequency conversion. Generally, large signal operation leads to angular shifts in the frequency of noise, a similar action as displayed in the frequency mixer. Due to frequency translations, noise power which is totally uncorrelated at one input signal power, may become fully correlated at another input power. This correlation occurs when the origins of the noise have the same originating physical source. The conversion of low frequency baseband noise events in the active device, operating in the oscillator mode, to spectral noise power in the RF region, is a good example.

Flicker noise adds stochastically. In a cascaded system each stage contributes its own phase noise. Cascaded stages operate independently, the noise adds stochastically and statistically, and the noise power is the sum of the individual noise powers. Therefore, the Friss formula does not apply [160].

However, consideration of additive white noise power for the small signal case, and in the application of the Friss formula, clearly illustrate the cascaded noise power outcome. In a cascaded system noise power is dominated by the first few stages of the cascade, as the noise power of the cascade is governed by,

$$F_T = F_1 + \frac{F_2 - 1}{G_{1av}} + \frac{F_3 - 1}{G_{1av}G_{2av}} + \dots + \frac{F_n - 1}{\prod_1^{n-1} G_{nav}} \quad (4.1)$$

where the gain is defined as the available gain of each I^{th} stage, G_{Iav} , and the stage noise factor of the K^{th} stage is F_K . In terms of the output carrier signal-to-noise power ratio for white phase noise we recast (4.1) and have

$$\frac{C_{out}}{N_{out}} = \frac{P_{out}}{F_T k T_o B} \quad (4.2)$$

where B is the noise bandwidth normalized to a 1 Hz bandwidth and T_0 in this case is the ambient temperature in Kelvin, and k is Boltzmann's constant. If the gain of the first stage is large, then the value of F_T is dominated by the first stage or F_1 . If noise power is the only consideration, and the system is void of large signal perturbations, then application of the Friss equation is appropriate. Generally, the goal is to maximize dynamic range. In general, the spurious free dynamic range (SFDR) is to be maximized. The SFDR is a function of the intermodulation distortion level, the noise power level, and the total real signal power. Simultaneously, we also want to maximize large signal performance. Therefore, the noise power is to be minimized commensurate with low distortion and large output power.

In a cascade system, subsequent stage distortion increases as the signal input power to that stage increases. Therefore, we are motivated to reduce the gain of the prior stage or improve the linearity of the offending stage. Adding feedback at the expense of gain is appropriate, as opposed to increasing operating power. Another method cited in this work is to adjust the level of gain, noise factor, and linearity of every stage in the cascade, so that all stages degrade equally throughout the cascade. In this case no single stage dominates. This technique would apply to the noise factor and the intermodulation as both factors are linked on a stage by stage basis through successive stage gain. To see this, consider coupling the intermodulation distortion of each stage as described by the 3rd order input intercept (IIP3) with that of the noise factor. In Figure 4.1 a preselector cascade is shown which is applicable to either a receive or transmit

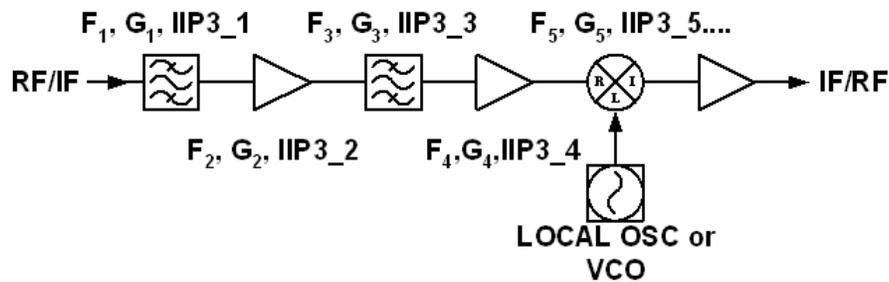


Figure 4.1: Up/Down conversion preselector transceiver cascade

function. Each stage is associated with a noise factor, available gain, and intercept value. The intercept level characterized by IIP3 of each stage, is an approximation of the degree of device nonlinearity. Nevertheless, it provides a reasonable correlation of distortion levels introduced by multi-tone signals distributed throughout the cascade [8, 24]. In the following we develop the relationships which describes the noise and distortion contribution on a stage by stage basis in a system cascade. The cascade noise relationships presented here were developed earlier and previously presented in section 7.2. Recall that the total noise power output of the m^{th} stage where all stage gains, G , are defined as available gain is

$$N_{o,m}^T = \sum_{n=2}^m \left[(F_n - 1) kT_0 B \prod_{i=2}^n G_i \right] + F_1 kT_0 B \prod_{n=1}^m G_n . \quad (4.3)$$

Therefore, the noise contribution, C_j^N , of the j^{th} stage is given by,

$$C_j^N = \text{j}^{\text{th}} \text{stage noise contribution} \equiv \left(\frac{F_{j-1}}{(G_j^A / G_j) F_T} \right) \quad (4.4)$$

where $G_j^A = \prod_{n=1}^j G_n$ and $F_T = F_1 + \sum_{n=2}^m \frac{F_n - 1}{\prod_{i=n}^m G_{i-1}}$. Then (4.4) provides the fractional noise contribution of the j^{th} stage to the total output noise.

The distortion contribution is developed in a similar manner. The intermodulation distortion of a cascade is assessed using the cascade intercept method, and noting that for narrow channel bandwidth relative to the operating frequency, a worst-case additive distortion scenario is justified [8]. For receiver systems, the contribution to nonlinear distortion is captured by IIP3, and for all stages this will be referred back to the input of the cascaded system. In a transmit cascade it is customary to capture the distortion by the third output intercept, OIP3, however, they are interdependent as they are related through stage gain, see page 11. Keeping with the nomenclature developed for the noise contribution previously, this leads to the definition of the

fractional contribution of the j^{th} stage to the system IIP3 as,

$$C_j^{\text{IP3}} = \text{IIP3 contribution} \equiv \frac{\text{IIP3}^{\text{T}}}{\text{IIP3}_j^{\text{A}}} \quad (4.5)$$

where the accumulated IP3 of the j^{th} stage referred to the system input is

$$\text{IIP3}_j^{\text{A}} = \text{IIP3}_j / G_{j-1}^{\text{A}} \quad (4.6)$$

and is $\text{IIP3}_{\text{dBm}, j}^{\text{A}}$ when expressed in dBm. Note all prior gain and loss up to the j^{th} stage modifies the intercept when it is referred to the input of the cascaded stages. Combining the contribution of individual stages yields the total system IIP3 given as,

$$\text{IIP3}^{\text{T}} = \left(\sum_{n=1}^m 1/\text{IIP3}_n^{\text{A}} \right)^{-1}. \quad (4.7)$$

Intermodulation distortion (IMD) is the upper bound for the total system undistorted response, while noise sets the lower bound. So C_j^{IP3} , (4.5) and C_j^{N} (4.4), denote the contributions of each stage to the dynamic range. In this development, the contributions of individual stages to noise and intermodulation levels are both referred to the input of a cascade, although they can certainly be referenced to the output. Consequently, the dynamic range is defined as (see appendix page 441).

$$\text{SFDR}_{\text{dB}, i} = \frac{2}{3} (\text{IIP3} - N_i) . \quad (4.8)$$

Using these parameters a stage contribution graph is produced providing a clear picture of the impact of various stages on overall performance, and identifying the stage or stages that dominate noise, distortion, and dynamic range performance of the system, see Figures 1.5 and 1.6.

Redistribution of the gain, noise, or distortion contributions of the stages alters the overall SFDR and the correlation of these changes are clearly seen. The cascade system shown in Figure 4.1 represents an RF preselector, or down converter module, and will be used as an example

of converter design using the contribution method. Stage assignment progresses from the filter input and terminates at the IF mixer output. Note, the same system cascade diagram, Figure 4.1, is applicable in reverse in transmit mode using up-conversion. Inspection of (4.4) shows, that if each of the stage parameters are appropriately chosen, a balanced noise contribution can be achieved whereby C_j^{IP3} has the same value for all j . In so doing, the required gain and noise factor is distributed and not necessarily bundled in the first few stages. The intent here is to couple the cascaded noise factor with the distortion of the cascade. The result of this procedure is that the minimum required gain is found for a given noise factor. As a result, the intermodulation target is met with the lowest possible individual intercepts assigned to each stage. This is a key result of the work presented in this dissertation. A further consequence is that this action generally leads to minimized power consumption, a particularly important attribute of a transmitter cascade. In general, it is possible to change the relative contributions of stages through choice of gain, however sometimes changes in architecture are necessary. For the preselector case study to be discussed in Section 6.3, the initial assignment of stages is straightforward, however further optimization and trade-off analysis is possible. For example, the usual approach of establishing signal-to-noise in the early stages of the cascade results in stages further down the cascade requiring higher intercept values. Consequently, these stages will generally have additional power consumption. Trade-offs of the contributions of individual stages to distortion and noise will lead to constrained total power consumption, while still achieving the required system SFDR.

At this juncture we will develop a design-methodology for creating a trade-off assessment in maximizing SFDR of an RF receiver, or transmitter front end, consisting of cascaded stages. The distortion intercept of the cascade is either referenced to the input port for a receiver, or to the output for a transmitter. The noise factor, or noise power of the cascade, uses the same reference port. Not unlike distortion in the receive function, the input referred noise figure is of interest in receiver development, while in transmit the output noise power is of interest. Once again these are interdependent and coupled through the cascade system gain.

As mentioned earlier, for a relatively narrowband channel a worst case additive distortion scenario is justified, and represents an upper bound on the total system distortion. In particular, this means that the distortion intercept of the various stages are directly combined to yield the overall intercept. In the case study, we specifically address a receiver system however, with minor changes, the discussion also relates to a transmitter system. A central component of the methodology is the use of a stage contribution graph that provides a clear picture of stage performance, identifying which stage or stages in the cascade dominate performance. Calculations of noise and distortion contributions provide an indication of which stage tends to raise the total noise factor or distortion, compared to all others in the cascade. Redistribution of gain, noise, or distortion will alter this relationship and lead to changes in the system SFDR. Passive stages generally do not restrict nonlinearity however, they do contribute noise. So to simplify the following discussion, passive stages immediately preceding an active stage are combined. The active and passive stage are combined into a single stage with available gain

$$G_{av, i} = L_{n-1} + G_{av, n} \quad (4.9)$$

and composite noise factor of

$$F_i = \frac{1}{L_{n-1}} + F_n \quad (4.10)$$

for $n \geq 2$, for $i = 1$ to n , where the passive loss of the stage is L and G_{av} is the available gain of the gain stage.

First consider the conventional system design approach whereby the noise figure of the receiver cascade is established on the premise of maximizing the gain of the first stage and the first stage establishes the signal-to-noise ratio of the system. The system target SFDR is determined by the overall IIP3 performance. Also, in the conventional design approach, the first stage usually has negligible impact on IIP3 by virtue of the excessively large gain. However, a reasonable choice in the design process is to select stages following the first as contributing equally to the reduction in IIP3. Thus, the minimum acceptable $IIP3_{dBm}$ of the j^{th} stage is

obtained from IIP3_j^A and $\overline{\text{IIP3}}_{\text{dBm}}^T$ as

$$\text{IIP3}_{\text{dBm},j} = \text{IIP3}_{\text{dBm},j}^A + G_{\text{dB},(j-1)}^A \quad (4.11)$$

$$\text{IIP3}_{\text{dBm},j}^A = \overline{\text{IIP3}}_{\text{dBm}}^T + 10 \log n \quad (4.12)$$

where $\text{IIP3}_{\text{dBm},j}$ is the required intercept of stage j to meet the minimum acceptable IIP3, $\text{IIP3}_{\text{dBm},j}^A$. The factor $\overline{\text{IIP3}}_{\text{dBm}}^T$ is the target total IIP3 in dBm. The factor n , is the number of stages in the cascade, and the acceptable gain, G^A , is defined as the available gain in dB.

In addition, the gain or loss of the preceding stages will modify this IIP3 as mentioned earlier. These modifications include any stage filter insertion loss, L_j , for meeting selectivity requirements such as image rejection, while contributing a predictable loss based on resonator unloaded Q and bandwidth. In addition, L_j will reflect added losses to the adjacent and alternate channels if a suitable filter is used, thus further modifying the required contribution factor of the latter stages. For a preselector, this arrangement provides for equal IMD contribution of each stage, that is each stage has the same input intercept when referred to the system input. As an example, with a cascade of three stages, each stage would need to meet a minimum system IIP3 of $10 \cdot \log_{10}(3)$ dB or 4.8 dB in excess of the target system IIP3. If the noise cascade were based on a balanced stage-noise contribution, with C_j^N being the same for all stages and associated gains with G_j being the same for all stages, then the required individual IIP3 values will tend to be a minimum. In assigning the noise contribution of each stage, consider partitioning the noise power contribution of each stage so that each stage is permitted to add to the total noise power in proportion to $(F_T - F_1)/N_{\text{stages}}$, where N_{stages} is the total number of stages in the cascade. The first stage would contribute F_T/N_{stages} , the second $[(F_T/N_{\text{stages}})G_1] + 1$, the third $[(F_T/N_{\text{stages}})(G_1G_2)] + 1$ and so on. Clearly, if the total number of stages present is large and the required total noise factor is less than N_{stages} ; then the noise factors of the first, or possibly the first couple of stages dominate. The smallest possible noise factor for any single stage is unity. For example, based on an equal stage noise contribution basis, it is not possible to have

Table 4.1: Cascade-stage assignments based on balanced contribution

Preselector System Cascade Parameters						
stage n	description	Gain _{<i>i</i>} (dB)	NF _{<i>i</i>} (dB)	IIP3 _{<i>i</i>} (dBm)	<i>G_i</i>	<i>F_i</i>
1	Filter	-3.97	3.97	xx	0.4	2.5
2	Preamplifier	1.761	3.01	0.969	1.5	2
3	Filter	-3.97	3.97	xx	0.4	2.5
4	Mixer	xx	2.041	-3.18	xx	1.6

Note: In some cases there is no contribution or it is not required, xx.

each stage of a four stage cascade meet a total target noise figure of less than 6.02 dB. For that case, each stage would be permitted to contribute a noise factor of just unity. Clearly, for this to occur, first stage noise dominance is required. If the equal stage contribution method is to be applied to the entire cascade, then the requirement for the system noise figure can be no less than $10 \cdot \log_{10}(N_{\text{stages}})$ dB. In any case, the architectural topology and the target specifications of the cascade network will drive the linkage among each stage via an equation or a tabular relation. For example, in the preselector system, stage 1 is a lossy filter, therefore, the noise factor, F_1 is defined accordingly as $F_1 \equiv (1/G_1)$. Thus F_1 , G_1 and F_2 are found. Completing the preselector function, F_3 and G_3 are linked for the same reasoning and with equal noise power partitioning, the value of G_2 is determined. From the array of values obtained for G and F , available gain and noise factor, the use of (4.12) permits the initial required values for each stage IIP3. Then the intercept values are appropriately scaled throughout the cascade as required, and adjusted in value by including required available gain of each stage, see Table 4.1.

The solution to meeting the design objectives of specified total noise factor and distortion are exact. The preselector architecture leads to a convenient set of coupled equations. This is not always possible, in which case a tabular set of trade-off tables are developed. Thus, this approach permits a set of noise, gain and loss relations to be developed, which are totally tractable. The case study of Section 6.3, will detail an architecture example with a complete set of values.

Central to the approach outlined, is establishing a baseline for further optimization of the cascade. In addition, the contribution diagram as opposed to the budget-level diagram permits

immediate feedback as to which stages serve as the limiting contributor in the cascade. Budget diagrams tend to be based on ad-hoc assumptions and prior experience, with little basis for a mathematical starting point for which to begin optimization. The approach we introduce here and develop further, is aimed at reducing a somewhat subjective approach to the system design.

4.4 Oscillator synthesis

In the following sections we present an integrated approach to oscillator synthesis. Oscillators are designed to meet a number of conflicting criteria. Power output, efficiency, noise, and tuning agility are some of the mainline specifications. A subset of problems includes minimum sensitivity to power supply variation, changes in load impedance and the consequences of altering the frequency and the available power, manufacture ability, circuit tolerance, size, weight and cost.

During the synthesis process, one would like to use a one or two port device and find an embedding network which drives the design in the proper direction to meet the mainline specifications optimally. If not optimal, then reasonably close so that appropriate trade-offs can be studied. In this section we discuss a mapping technique which incorporates the Smith[®] chart, or the reflection coefficient plane (chart). We identify regions of the chart appropriate for both the series and shunt forms of tuned oscillators. Then we further develop maps for the terminations and feedback element values, so as to position the device input reflection plane optimally with respect to the resonator reflection coefficient. This design process provides for a reactance compensation technique, which permits proper termination by the active device for a non ideal resonator. An approach to oscillator design must include active device and resonator with their associated parasitics. This problem has been overlooked in prior work.

Maximizing oscillator instability is discussed, and the requirement to bound instability in the approach to oscillator design is raised. We further develop the technique with emphasis on visualizing the active device performance as a power oscillator. The central goal is find-

ing suitable active device modifications and achieve device port reflection coefficients that are compliant to stable oscillator tuning.

4.4.1 The conditions for sustained oscillation

In this section we need to address this deceptively simple question, will it oscillate? An answer to this question must first clarify what sort of oscillation are we considering? In this work the oscillators are sinusoidal, the resonators or timing elements are solely reactive, a pair of complex poles are involved in the timing mechanism, and we contend that our amplifiers or active devices are operated in a linear fashion. We need to differentiate our oscillators from those which are strongly nonlinear, switching or pulse like in operation. Although there is an associated timing mechanism involved in those oscillators, its timing is provided by a single pole response. Therefore, our oscillators are linear 2nd order complex-pole oscillators, however, this does not preclude the need to somehow limit or dampen the developing signal voltage, assuming oscillations start. Therefore, by linear oscillators we imply oscillators which develop signal voltage levels that are not so large that we need to deal with large signal effects such as intermodulation of signals with noise, noise conversion, and active device excess noise. These topics were addressed in treating large signal input levels to amplifiers of Chapter 2, however they are not considered in this discussion [46].

Sinusoidal oscillators rely on the ability of our circuit to place a set of complex poles in the complex plane, on the $j\omega$ axis, and sustain their location as close as possible to the imaginary axis. It is worthy of a note, that any movement by those complex pole pair from their location on the imaginary axis, constitute the phase noise that we associate to a less than perfect oscillator [47]. So, will it oscillate?

Sinusoidal complex pole pair oscillator networks, operate as systems and are broadly classified into two network types; one-port and two-port. Furthermore, the one-port oscillator implementation is subdivided into negative conductance or shunt configuration and negative resistance or series configuration circuit topologies. These categories are relevant as they de-

scribe the interconnection between the resonator and the active device. The operation of the series oscillator is such that the active device senses the loop current through the resonator, and adjusts the applied incident voltage returned to the resonator. For limiting to occur in the series oscillator, the incident voltage must decrease. The process by which this occurs is controlled by the active device, as the active device negative resistance must decrease. The shunt oscillator is the dual of the series oscillator. In this configuration, we sense the resonator node voltage, and adjust the incident current accordingly. For limiting to occur, the incident current must decrease. The process by which this occurs requires the active device negative conductance to increase. It is useful to look at the operation of the negative oscillator configurations from the perspective of the active device. Since the resonator, either series or shunt, is described by an impedance or admittance function, these oscillators are acutely described as complex-pole one-zero oscillators. The presence of this zero is key in driving the complex pole pair towards the imaginary axis. The zero is intrinsic to the resonator-active-device interface. Preserving high operating Q requires the zero in the complex plane to be located as close to the origin as possible. In this manner, the amount of loop gain provided by the active device to restore the complex pole pairs back to their desired location is minimal.

For a series oscillator, the negative resistance must decrease. For the shunt oscillator, we must see an increase in the negative conductance. Both operations which occur are accompanied by the rising input signal levels delivered by the resonator to the active device input. Therefore, there are at least two key operations in sinusoidal, second-order, complex-pole, one-zero, oscillator operation. One, secure the conditions for starting oscillation, and two, sustaining oscillation through controlled limiting. The function of both starting and controlling oscillation is a process by which the complex poles are firstly located on the right side of the complex plane. Then as signal amplitude increases, the active device limiting moves the poles from the right half side of the complex plane onto the imaginary axis. If the oscillator were a no-zero system, then a form of controlled damping would be required to accomplish the limiting function.

Although the one and two-port oscillator systems are distinctly different in circuit imple-

mentation, they nevertheless share a number of common elements to ensure stable oscillation. Stable oscillation in our work implies single frequency, nearly sinusoidal generation of voltage or current.

The active device is a three-port element. The oscillator configurations discussed here utilize one or two of the available three ports. The negative resistance one-port oscillator can be envisioned as a two-port feedback oscillator. The incident and reflected waves associated with the active device and resonator, as configured in a one-port oscillator, provide an equivalent transfer function to that obtained with a two-port oscillator network. The two-port oscillator system requires the signal path in the feedback network to transverse the round path trip between the active network output and the input port. While in the one-port oscillator, we need only to support the travel of an incident and reflected wave between one of the available three ports. We will see the similarity in the transfer functions upon comparing the network analysis of a distinct two-port with external feedback oscillator, with that of the one-port oscillator.

A microwave oscillator is conveniently described by a signal-flow graph, see Figure 4.2 and [169], [174], [175].

The active device and resonator reflection coefficients are designated as Γ_{Dev} and Γ_{Res} with incident waves into node b_D and node b_C . The connections b_D - a_C and b_C - a_D represent the one-port negative resistance and resonator interface. The active device must contain a description for the active generation of a signal from either a noisy input or a small voltage transient, for example when DC power is first applied, b_n . Furthermore, we assign a nonzero reflection coefficient to the resonator at all frequencies, however, we define a linear operator Γ_{Dev} so that we may relate the fundamental component of b_D to the fundamental component of a_D . The device, resonator, and noise generator circuit then form a closed-loop regime given by the set of wave equations,

$$a_D = b_n + \Gamma_{\text{Dev}} b_C \quad (4.13)$$

$$a_D = b_n + \Gamma_{\text{Dev}} \Gamma_{\text{Res}} a_D \quad (4.14)$$

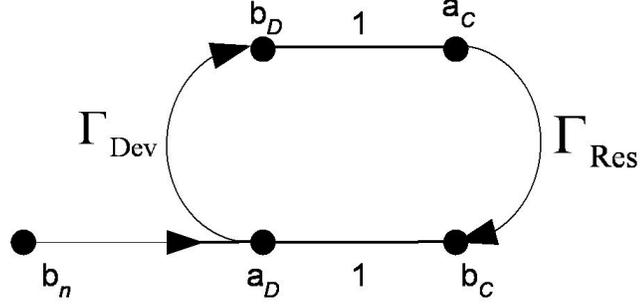


Figure 4.2: The negative resistance one-port oscillator signal flow diagram. The resulting signal flow transfer function is analogous to a two-port, external feedback, closed loop system transfer function.

and therefore we have

$$b_n = [1 - \Gamma_{\text{Dev}}(A) \Gamma_{\text{Res}}(\omega)] a_D \quad (4.15)$$

where we have noted that the resonator reflection coefficient is strictly a function of frequency, ω , and the device reflection coefficient is strictly a function of signal amplitude, A . These assumptions are justified on the basis of maintaining the signal amplitude of the fundamental and harmonics to be small.

Therefore, a closed loop description for the negative resistance oscillator is given by (4.15) recast by,

$$\frac{a_D}{b_n} = \frac{1}{[1 - \Gamma_{\text{Dev}}(A) \Gamma_{\text{Res}}(\omega)]}. \quad (4.16)$$

Next, we consider the two-port feedback system with positive feedback, see Figure 4.3.

If the ideal active device, $G(A)$ provides zero phase shift with respect to frequency, then the feedback network must provide 360° to support positive feedback. Otherwise, whatever phase shift the active device provides, the remaining difference from 360° must be provided by the feedback network, $H(j\omega)$. It is important to provide this emphasis, which also will

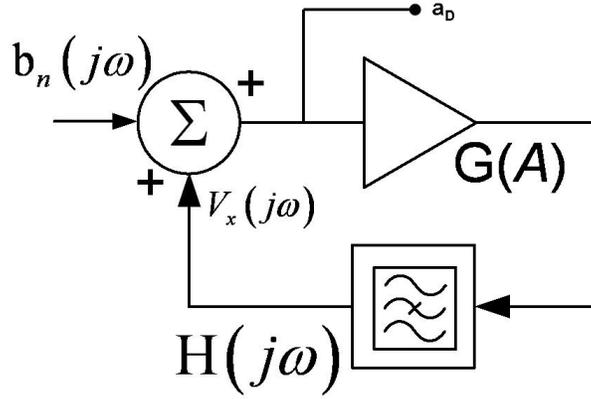


Figure 4.3: The two port oscillator consists of an active feed forward path with an active device, $G(A)$. The active device limiting function is controlled by the feedback resonator, $H(j\omega)$, whose added function is to also lock in the feedback phase.

also be stressed for the one-port feedback system. These arguments are necessary to introduce instability, however not necessarily sufficient to guarantee self-sustained oscillation. In the two-port oscillator system, we feed back a loop voltage, $V_x(j\omega)$. This is our control voltage sensed from the series resonator, $H(j\omega)$. A control voltage and a noise voltage, $b_n(j\omega)$, are summed and are analogous with our incident wave flowgraph of Figure 4.2 at port a_D . Hence, writing feedback loop equations we have,

$$a_D G(A) H(j\omega) = V_x \tag{4.17}$$

and

$$V_x(j\omega) + b_n(j\omega) = a_D. \tag{4.18}$$

Recast (4.18) and this result is exactly analogous to our (4.15) given by,

$$b_n(j\omega) = [1 - G(A) H(j\omega)] a_D. \tag{4.19}$$

The resulting two-port positive feedback transfer function is given by,

$$\frac{a_D}{b_n(j\omega)} = \frac{1}{[1 - G(A)H(j\omega)]} \quad (4.20)$$

and should be compared to that of Equation (4.16).

At this juncture, we are in a better position to address the question, will it oscillate? Investigation of either the two-port feedback oscillator, or the one-port reflection oscillator transfer functions, illustrate the key element for determination of instability. The zero's of of either system provided by,

$$\begin{aligned} G(A)H(j\omega) &= 1 \\ \Gamma_{\text{Dev}}\Gamma_{\text{Res}} &= 1 \end{aligned} \quad (4.21)$$

provide a necessary condition. The condition though provided by (4.21) is neither sufficient nor easy to interpret. In addition, a number of references have addressed the incorrect application of (4.21); in addition to the previously cited, [169], there are [168], [170], [176], [180]. The central theme in these works is identifying if the oscillator system is unstable, if it will support oscillation, and the performance outcome for the chosen topologies. The correct application of the conditions stated in (4.21) is central, for example, in applying Bode's criterion for establishing the stability of an open loop control system. If the open loop gain of a system is sufficiently large, that is very much greater than unity, and the phase shift around the open loop system is -179° , this does not imply an unstable nor oscillatory system. In the same vein, the knowledge of the value of the loop transfer function at one frequency provides us with no information about the stability of the system. The system could contain a number of both right half plane poles and zeros. More to the point, we must ascertain that the loop gain is -1 at a specific frequency. This is fairly easy to apply to the two port feedback oscillator system as we can utilize the methods of Bode, Nyquist, or Black. However, the application of the Barkhausen

stability criterion is problematic. The difficulty is particularly troublesome in determination of the stability and meeting the conditions for sustained oscillation for the one-port oscillator system. The application of the product of the reflection coefficients and the prerequisite that their magnitude must be greater than unity is fraught with error. For example, a one-port series resonator oscillator system whereby the active device provides a negative resistance of -20 ohms is interfaced with a resonator with a resonant impedance of 7 ohms. Both the device and resonator are characterized in a system with a Z_0 of 10 ohms. Clearly, the system has a total resistance of -13 ohms and should support instability. However, the product of the reflection coefficients are less than unity. Part of the problem is related to the choice of the reference impedance. Another part, is not reconciling the phase of the reflection coefficient. In one case, the interface may prove to provide instability if the oscillator-resonator interface were configured in shunt form as opposed to series form, or visa-versa.

Consider, a negative series generator with a value of -75 ohms. An external load of 25 ohms is connected and the system is potentially generative. However, consider the system configured as a shunt oscillator, then the negative conductance is $-13.3\text{ m}\Omega$. If the load were left the same, that is 25 ohms, the oscillator system clearly would never start. Similar errors occur in switching to other reference impedance systems and therefore, gauging the stability of a system needs to be invariant to the system reference impedance.

Although several techniques exist for circumventing these analytic shortcomings, we have found that a simplified application of the mapping technique, discussed next in Section 4.4.2, is straight forward to implement and accurately addresses the question.

The use of the reflection coefficient plane permits plotting the locus of the active device and the resonator reflection on a single chart. There is no need to resort to a compressed chart for Γ_{Dev} much greater than unity, as we will plot its inverse. Therefore, the device and the resonator occupy the same space on the chart. A simplified mapping technique directly answers the questions, will the system start oscillation and the frequency of the oscillation. The active device reflection coefficient can be simple or complex, that is to say, contain reactive

elements either in shunt or series with the negative resistance (conductance). The resonator can contain parasitic elements and therefore, although the oscillator may start, it may not sustain oscillation. The mapping will illustrate visually if this can occur.

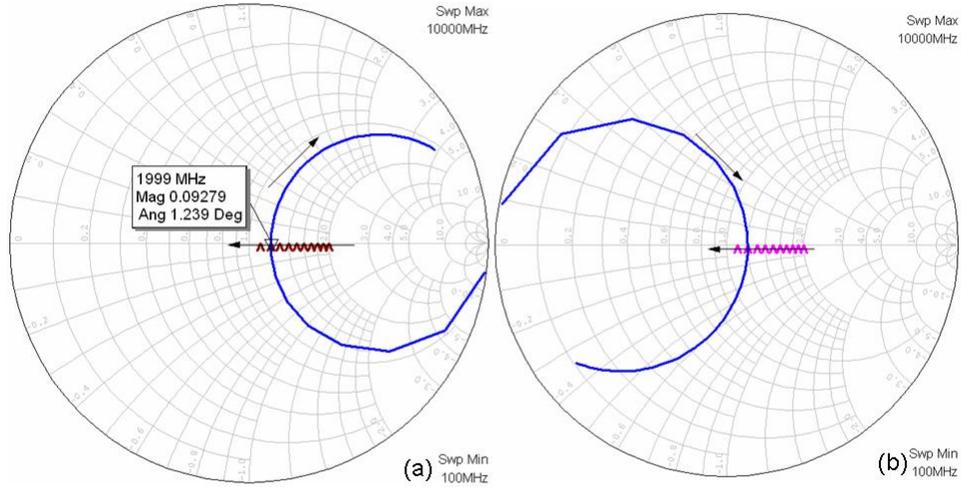


Figure 4.4: The negative resistance and conductance one port map: (a) The case for oscillator startup, Γ_{Dev} is contained within the series resonator locus; (b) Oscillator startup is not possible for the shunt oscillator configuration map; the initial Γ_{Dev} is outside the resonator locus.

An example of the application of mapping for the case of both series and shunt type, one-port oscillators, is seen in Figure 4.4. The cases illustrated are a series oscillator-resonator interface, Figure 4.4 (a), while in (b), the interface is that of a parallel equivalent resonator with identical loaded Q . Both resonators are resonant at 2 GHz and both active devices have identical values of negative resistance, -70 ohms. For purposes of examination of the technique, the active device negative resistance is swept, from -100 ohms to -51 ohms and the resistance sweep models the case of ideal series limiting. A real active device and resonator would have

additional parasitic components forcing curvature of the active device limiting characteristics with frequency and signal amplitude while additional loops could be present in the resonator locus. However, the condition of instability, the frequency of oscillation, and the potential for multiple frequency of oscillation is available from this map. The construction of the map and the interpretation is as follows:

1. Construct the locus of the resonator from calculations of the reflection coefficient versus frequency. The unloaded Q of the resonator is determined by all known dissipative losses. Therefore, the inductive reactance of the resonator is calculated based on the ratio of Q and dissipative losses. The assumption here is that inductive losses are dominant. In effect, this sets the diameter of the resonator reflection coefficient locus. Plot $\Gamma_{\text{Res}}(\omega)$, and note the direction of movement of the reflection coefficient is clock-wise. This is the usual case, unless parasitic resonant loops are present.
2. The active device inverse reflection coefficient, as a function of amplitude and frequency, is plotted on the reflection plane. Therefore, we require $\frac{1}{\Gamma_{\text{Dev}}(A, \omega)}$. For the ideal case, we may suppress the dependency of the device reflection on frequency. However, this parameter is handled in the map analysis, and will provide information on the possibility for multiple-oscillations.
3. If the *trajectory* of the locus of $\frac{1}{\Gamma_{\text{Dev}}(A, \omega)}$ lies *inside* the locus of $\Gamma_{\text{Res}}(\omega)$, oscillation startup will occur at a frequency nearly equal to their intersection. The assumptions here are restricted by assuming small signal conditions. However, if the loaded Q is reasonably large, sinusoidal single frequency analysis permits a good approximation to oscillator operation, specifically the operating frequency.
4. If the *trajectory* of the locus of $\frac{1}{\Gamma_{\text{Dev}}(A, \omega)}$ lies *outside* the locus of $\Gamma_{\text{Res}}(\omega)$, for all A and ω , oscillation startup will not occur.

4.4.2 Oscillator tuning synthesis via termination mapping and maximum instability

In this section and subsequent sections, Section 4.4.7 and Section 4.6, we address approaches to power oscillator synthesis which incorporate a combination of circuit techniques developed in this work. In these sections we lay the ground work for coupling the graphical design of active networks with simulation. Graphical analysis readily handles the small signal operation of the active device, while an understanding of how large signal and parasitics and their cumulative affects modify small signal operation. The techniques for oscillator synthesis and the operation of both small signal level and power oscillators are further validated with electromagnetic and harmonic balance (EM-HB) co-simulation.

A classical treatment of oscillators first focuses on single oscillator frequency realizations [33], the required embedding and feedback form, and the matrix requirements to meet the conditions to support sustained oscillation. The embedding networks which provide feedback have reactance levels which dominate the device intrinsic parameters so that the active element contribution is neglected. The addition of tunable reactance, either inductive, so called permeability tuned oscillators, or capacitive, varactor tuned oscillators, considers the device as supporting only the required loop gain. That is to say, the active device is applied to overcome resonator losses and this action is frequency and amplitude independent. So in the case of an ideal oscillator, a real negative resistive component would exist, or sufficient loop gain would be provided. However, none of the active frequency dependent elements of the device are present to alter the resonator or phase shift network parameters. Limiting the amplitude of the oscillator, a necessary ingredient to carefully place the poles of the network response precisely on the $j\omega$ axis, could be done external to the device. The active oscillator element would not provide the self-limiting function as limiting could be done externally, via an ALC or AGC, automatic gain control network. The oscillator tuning would be a sole function of the resonator, as long as the resonator alone provided the proper magnitude and angular relationship to meet the criterion for oscillation. Furthermore, the tuning range and tuning stability of the oscillator

must be free of spurious points of operation introduced by the active device. The active device would only need to assist the resonator in providing the proper magnitude of gain through the adjustment of the active device transconductance, and overcome circuit losses. Finally, the active device gain is under the control of an external peak signal detector, and control of the active device transconductance is accomplished by control of the active device current. Again, the motivation is to position a pair of complex poles, solely provided by the resonator, on the $j\omega$ complex plane axis.

The oscillators studied here are designed utilizing the self limiting process of the active component. The device and resonator interface are not easily separated, and the ability to provide broadband stable tuning is not solely determined by the resonator. If the oscillator is the reflection type, the locus of the device input and output reflection coefficient is controlled by the device intrinsic parameters, including device packaging, both internal and external feedback, and port terminations.

As part of the design process of synthesizing circuit topologies for amplifiers, including the need for feedback and selecting port terminations, referred to as device modification, the designer must first consider device stability. Although it would appear as an oxymoron, the same is true of oscillators. If the active device has a Rollet stability factor $K < 1$ [164], then external feedback is not required. However, the investigation of the instability condition must be accomplished over the frequency range of interest. In particular, for a given load termination, we first investigate the input reflection coefficient given by

$$S'_{11} = S_{11} + \chi \text{ with } \chi = \frac{S_{12}S_{21}\Gamma_t}{1 - S_{22}\Gamma_t} \quad (4.22)$$

where S_{ij} are the 2 port S-parameters of the active device, and Γ_t is the load termination reflection coefficient.

If we desire to maximize S'_{11} , then the phase condition of χ must permit constructive addition of the magnitude of χ with the magnitude of S_{11} . Again this condition must be observed over the entire frequency range of interest. Clearly, as Γ_t approaches $1/S_{22}$, the value of χ and S'_{11}

are maximized. If we solve for Γ_t in terms of χ we have

$$\Gamma_t = \frac{1}{\frac{S_{12}S_{21}}{\chi} + S_{22}}. \quad (4.23)$$

The S-parameters are a function of frequency, and therefore at each frequency a sweep of χ from 0 to ∞ is performed. We therefore seek a map of Γ_t , which is bounded to be less than unity for a range of χ evaluated at each frequency. The appropriate value of Γ_t and topology, which in itself is a frequency dependent load, must permit S'_{11} to take on a magnitude and angular range which properly terminates the resonator reflection coefficient over frequency. If the oscillator configuration is series type, then the resonator might be series as well. In this case, the real part of negative input resistance of the active device would be less than the series loss of the resonator. This is required in part to ensure oscillator startup. For the shunt oscillator, a parallel tuned resonator is appropriate. Another aspect of this requirement considers the change in the reflection coefficient of the device input as self limiting occurs. In the series oscillator, the imaginary portion of Z_{in} moves along constant reactance contours, while in the shunt mode oscillator the imaginary component of Y_{in} moves along a constant susceptance contour. If the resonator reflection coefficient is ideal and free of parasitics, then the series resonator reflection coefficient will move clockwise with increasing frequency, crossing the short circuit side of the reflection coefficient plane at resonance. A parallel or shunt tuned resonator will move in the same clockwise direction, however crossing the open circuit side of the chart at resonance. These directional characteristics of the resonator reflection with increasing frequency are of fundamental importance when addressing the resonator interface to the active device. If single frequency oscillation is to occur, then clearly the series limiting characteristics of the series type oscillator will intersect the locus of the series resonator at one point. If the shunt oscillator configuration is used, then a shunt or parallel tuned resonator reflection coefficient would ideally be intersected also at a single point. Intermixing these resonator-oscillator configurations will potentially promote satisfying the angle criterion for oscillation at multiple frequency points.

The active device trajectories can be altered. The active device limiting trajectory of input

reflection coefficient is reshaped with frequency dependent embedding elements connected to the active device. Consider for example the series type oscillator. As the amplitude input drive level to the device increases, the device negative input impedance will decrease. This action in conjunction with the shunt reactance added to the device modifies the input reflection coefficient. This concept is key to mitigating the problems of multi-oscillations introduced by the presence of parasitics associated with the resonator. The resonator is usually optimized for tunability and unloaded Q . If this is accomplished in the presence of parasitics, then the design has successfully absorbed these stray elements. Instead, we turn to the active device for compensation. This is a key point developed in this work and in Section 5.1.3. In this section we develop the ground work.

4.4.3 The conditions for sustained oscillation

In this section we need to address this deceptively simple question, will it oscillate? An answer to this question must first clarify what sort of oscillation are we considering. In this work the oscillators are sinusoidal, the resonators or timing elements are solely reactive, a pair of complex poles are involved in the timing mechanism, and we contend that our amplifiers or active devices are operated in a linear fashion. We need to differentiate our oscillators from those which are strongly nonlinear, either switching or pulse forming operation, the so called relaxation oscillator. Although there is an associated timing mechanism involved in relaxation oscillators, the timing is provided by a single pole response. Therefore, our oscillators are linear 2nd order complex-pole oscillators, however, this does not preclude the need to somehow limit or dampen the developing signal voltage, assuming the oscillations start. Furthermore, by linear oscillators we imply oscillators which develop signal voltage levels that are not so large that we need to deal with large signal effects such as intermodulation of signals with noise, noise conversion, and active device excess noise. These topics were addressed in treating large signal input levels to amplifiers of Chapter 2, however they are not considered in this discussion [46].

Sinusoidal oscillators rely on the ability of our circuit to place a set of complex poles into the

complex plane, on the $j\omega$ axis, and sustain their location as close as possible to that location on the imaginary axis. It is worthy of a note, that any movement by those complex pole pair from their location on the imaginary axis, constitute the phase noise that we associate to a less than perfect oscillator [47]. So, will it oscillate?

Sinusoidal complex pole pair oscillator networks, operate as systems and are broadly classified into two network types; one-port and two-port. Furthermore, the one-port implementation is subdivided into negative conductance and negative resistance devices. Although the one and two-port oscillator systems are distinctly different in circuit implementation, they nevertheless share a number of common elements to ensure stable oscillation. Stable oscillation in our work implies single frequency, nearly sinusoidal generation of voltage or current.

First, consider both oscillator configurations, series and shunt, and the location of the input reflection coefficient locus. Shown in Figure 4.5 are the active device negative resistance parameters for a $|\Gamma_{in}|$ held constant and set equal to 1.4. These parameters include (a), the input series Q , (b) the equivalent series reactance, (c) the series real impedance, and (d), the parallel equivalent real resistance. All parameters are plotted as a function of the reflection coefficient angle, Γ_θ . The sweep in angular reflection coefficient is over one half of the reactance plane of the chart, as the other half is the mirror image. The equivalent reactance is zero at both extremes of the reflection angle as this places the reflection coefficient at either a perfect open or perfect short. For the series form of oscillator, forcing the angle of Γ_{in} close to the short circuit side of the reflection plane is preferred, as this matches the series resonator locus crossing near resonance. The series reactance is minimized permitting greater tuning range and the equivalent series resistance is small enough to insure startup. In addition, reference to Figure 4.6 illustrates that for varying values of the magnitude of Γ_{in} , minimum sensitivity occurs in the region of 80–120 degrees, see region (e) in Figure 4.6. However, the angle of the reflection coefficient of the active device is also located in a region of maximum input Q , thus limiting tuning bandwidth. Moving towards the shorted side of the reflection plane is preferred, where variation in the input negative resistance is less and the input Q is lower. This permits wider tuning range. For the

case of the shunt mode oscillator, see Figure 4.7, the negative real part of the equivalent parallel resistance rises near zero degrees and the reactance is minimum. Conversely, changes in $|\Gamma_{in}|$ give rise to large changes in the equivalent R_p . Again, an optimum is found near a region of 140° , see Figure 4.7. For this phase range of Γ_{in} , the equivalent value of the active device R_p is sufficiently negative to insure startup for resonators with an equivalent R_p of $50\ \Omega$. Reflection coefficient angles less than 140° will require resonators with a corresponding higher unloaded Q , as the corresponding device negative conductance decreases. This raises an interesting point from a measurement and validation point of view. The vector network analyzer, VNA, is a useful tool for device characterization and validation that a given device will meet the objectives outlined and satisfy the condition of oscillator startup. However, reflection coefficients that give rise to input resistance near $-50\ \Omega$ are difficult to measure, because a system operating within a $50\ \Omega$ environment produces an infinite reflection coefficient. Therefore, a stable reading from the VNA is not possible. Hence, to obtain measurements in this case, it is beneficial to insert a small resistance in series with the device, perform composite measurements of the input or output reflection, and then de embed the resistor, and parasitics such as PC trace and pads from the measured values of the network for the final result.

The problem of synthesis is first the evaluation of the stability of the two port. If the two port is unconditionally stable for all passive port terminations, then feedback is required. Selection of a suitable feedback network, if required, is next. This feedback network needs to provide a degree of instability and position the input reflection coefficient in a region of the reflection plane that provides the correct termination for the resonator. A combination of feedback, termination selection, and circuit topology, are involved in the process. Small signal S -parameters are converted to floating 3-port S parameters. The three-port parameters are subsequently converted to Z or Y parameters and thus permit series or shunt feedback to be added [9].

All of the three ports are designated as termination ports. The resonator is in effect a termination element. The feedback element and finally the output load provide the other

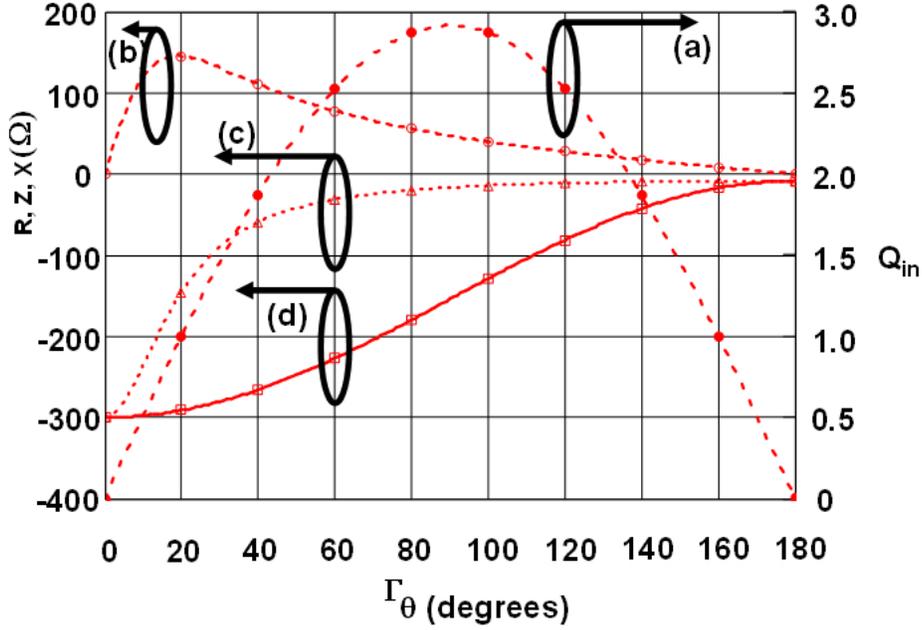


Figure 4.5: Active device input parameters: (a) Q as a function of the input reflection coefficient angle; (b) the equivalent reactance, X ; (c) the equivalent $|Z_s|$; (d) the equivalent $|R_p|$

terminations. However, two of the three ports could operate strictly as termination ports, the third port as the resonator, and none of the ports could be termed as an output port. This is possible, for example, if one of the ports also provided a point for delivery of power. The resonator for example could provide this capability. The main point, the oscillator configuration is quite non specific, quite general in configuration. Many orientations are possible. There are three ports available, any one of which can be considered common. Two reactance elements of one type, and a third which must be of opposite sign to support the minimum condition necessary for oscillation. Finally, these reactance elements can be in shunt or series with each active device branch. Hence, the resultant oscillator topologies number at least 12.

The selection of the feedback in itself is sufficient to provide a degree of instability, for example generate suitable negative resistance. However, the termination port also influences not only the magnitude of the reflection coefficient, however also the trajectory with frequency. Therefore, the selection of these elements is interactive. Hence, 2 of the 3 ports are “tuned” in

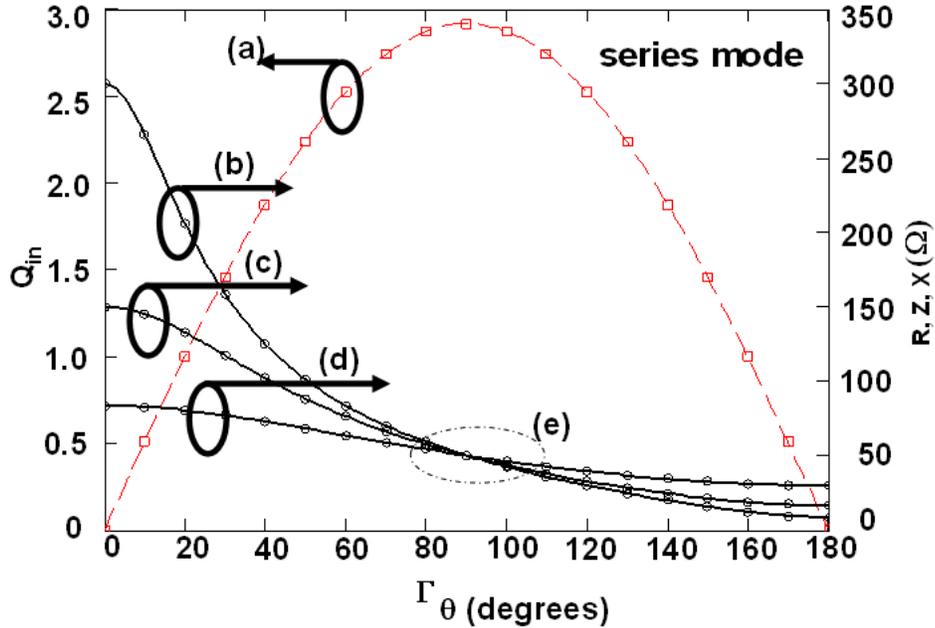


Figure 4.6: Series mode oscillator (a) device port input Q ; and (b)–(d) reference series real $|Z|$ for (b) $\Gamma = 1.2$ (c) $\Gamma = 1.4$ and (d) $\Gamma = 2$ (e) the convergence of variations in Γ is in the region 90° , near the maximum input Q . Hence the series mode oscillator has a more restrictive tuning bandwidth. Attempts to improve tuning bandwidth will result in higher variation in $|\Gamma|$.

the process of design while monitoring the third ports compliance to interface with the chosen resonator frequency response. Usually, the termination port could be set to maximize power output at a single frequency, in which case the feedback or termination of the second port is used to alter the third port input [34], [35] reflection coefficient. However, invariably this technique leads to trouble in tunability, the introduction of multi-oscillations over a wide tuning range, and the inability to start oscillation. There are several root causes for these conditions. One, is the ill conditioned input reflection coefficient phase with respect to the phase of the resonator, particularly if the resonator is plagued with additional resonate points due to parasitics. Second, the choice of the magnitude of the load may be sufficient for one oscillator type and permit oscillator starting (series oscillator form), while in the other configuration (shunt oscillator form), insufficient conditions occur. The nature of this problem is best understood by again considering the necessary magnitude of negative resistance, and the negative conduc-

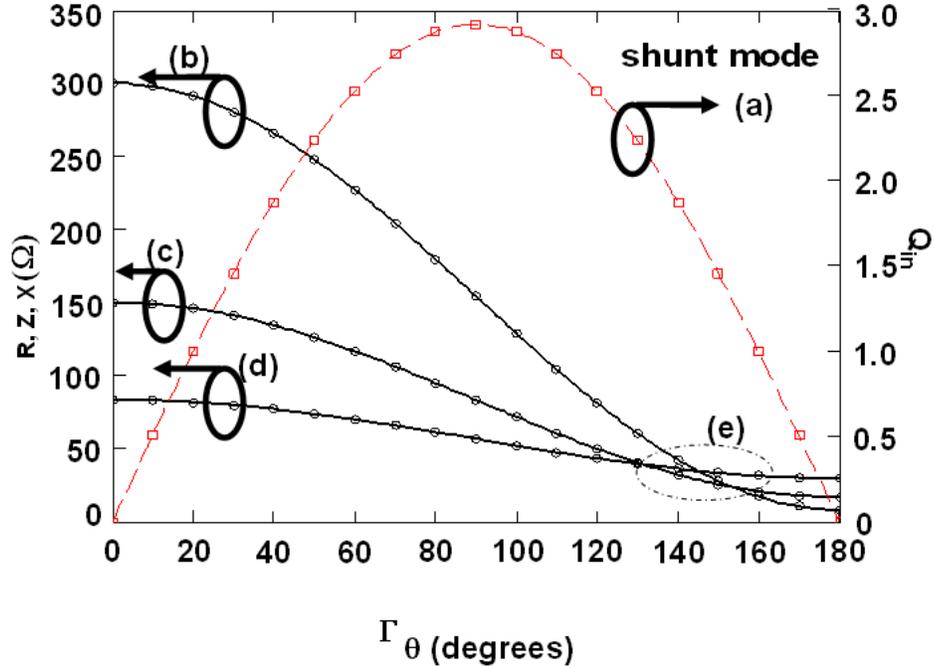


Figure 4.7: Shunt mode oscillator (a) device port input Q ; and (b)–(d)reference shunt real $|Z|$ for (b) $\Gamma = 1.2$ (c) $\Gamma = 1.4$ (d) $\Gamma = 2$ (e) the convergence of variations in Γ is in the region 140° , near the minimum input Q . Hence the shunt mode oscillator is less restrictive for tuning bandwidth and the variation in Γ is small.

tance required for each oscillator configuration to secure startup, and finally the trajectory of the reflection coefficient with frequency.

Maximizing the port Γ which terminates the resonator is not necessarily appropriate, however it does provide a reasonable starting point for design. However, more appropriate than maximization of Γ_{in} , is achieving the appropriate angle of the input reflection coefficient particularly as self limiting occurs. Another objection to an excessive Γ_{in} value, is the large variation in angular shift in the input reflection coefficient as device limiting occurs. The application of a large Γ_{in} , is analogous to applying excessive open loop gain. Just such a condition could apply in the two-port power amplifier feedback configuration. We find that under the condition of excessive large open loop gain, both the starting and final operating frequencies are not well predicted by small signal analysis. However, this situation is particular to the class of oscil-

lators which possess a large starting negative device component. An excellent example of this case is discussed in the appendix, see page 418. Fundamental to the visualization of the various feedback and termination circuit topologies surrounding the active device, is mapping. These various feedback and termination networks provide a means of active device modification and render a desired magnitude and phase response for the active device reflection coefficient versus frequency.

4.4.4 Device mapping and modification

In this section we treat the key concepts of active device mapping. We address the process by which an active device reflection coefficient versus frequency may be favorably modified through selective terminations and feedback. We then find that the resulting active network will properly terminate a given resonator, and eliminate the potential for multi-oscillations over a broad frequency range. Furthermore, proper manipulation of the active device reflection coefficient can improve oscillator phase noise.

Simple arrangements of series and shunt feedback when added to an active device require no complex transformations. For example, shunt networks can be converted to their Y parameter set and added term for term to the converted device S-to- Y parameters. Series networks are converted to their Z parameter matrix set and added term for term to the converted device S-to- Z parameters. In both instances, the composite Y or Z parameters are then converted back to a set of composite S parameters. These S parameters are then projected onto the reflection coefficient plane and permit the correspondence of the active device reflection coefficient movement with changes in the termination or the feedback element values. This case of either shunt or series feedback added to the active device is shown in Figure 4.8.

Series or shunt networks connected to the active device in either series or shunt form, can be simply added term for term to the appropriate converted device matrix. When this is not the case, and networks need to be concatenated that are of different forms, a different tactic is required. As an example, a $[Z]$ matrix two-port network that is in shunt with a second

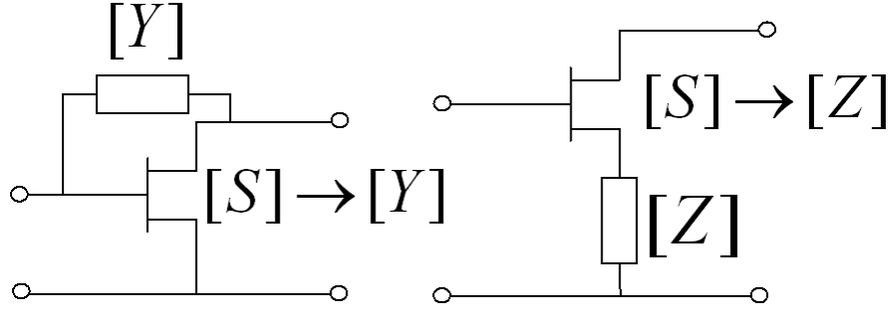


Figure 4.8: The shunt feedback configuration adds the Y matrix to the converted $S - Y$ matrix of the active device, while series feedback adds the Z matrix.

network. For this case, the transmission parameters, T matrix, of each network are used and the overall resultant matrix obtained by their product. Hence, the combination of Y , Z , and T matrix descriptions of two ports, permits complex terminations and feedback configurations to be reduced to a single matrix form. As an example, the network shown in Figure 4.9, with a single active device with network description $[S_1]$, and surrounded by a number of feedback and termination networks is reduced in the following manner:

$$Z_4 \rightarrow S_4 \rightarrow T_1$$

$$[S_1] \rightarrow Z_2$$

$$Z_2 + Z_1 = Z_3$$

$$Z_3 \rightarrow S_2 \rightarrow Y_2$$

$$Y_2 + Y_1 = Y_3 \rightarrow S_3$$

$$Y_3 \rightarrow S_3 \rightarrow T_2$$

$$T_1 \cdot T_2 = T_3$$

$$T_3 \rightarrow S'_{i,j}$$

(4.24)

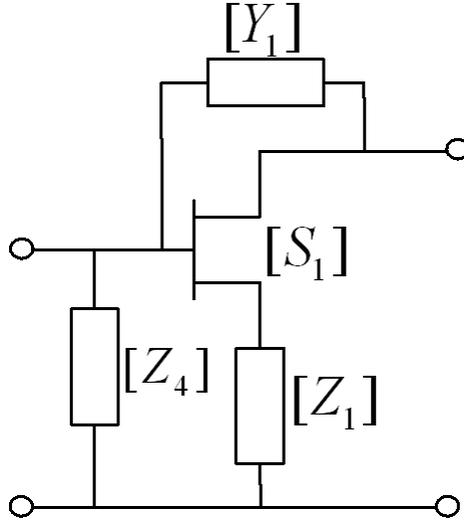


Figure 4.9: Transforms for each of the matrix types permit consolidating all combinations of feedback into a single matrix format.

In the above sequence, the right arrow implies transform, the matrices are conformable, they are all two-ports, and proper matrix multiplication must be observed. In addition, we need to be sure that the behavior of each individual series connection of two-port networks, is not modified under interconnection. It is necessary and sufficient to establish that after the interconnection is made, the current which enters the terminal of a port is identical with the current which emerges from the other terminal of the port in question [178]. If this is not the case, then the simple addition of matrix terms is not permitted. This validity test is similarly applied to all two port interconnections.

The matrix operation sequence is left to right, top to bottom. In network reduction 4.24 we have at the first line the conversion of Z_4 to S_4 and then T_1 . This action is in preparation to cascade this composite network with the final reduction of all the remaining networks. The remaining networks are the device, $[S_1]$, to Z_2 , to be added to the series feedback element, Z_3 . Then conversion of this composite to Y so that the shunt network feedback of Y_1 is added. The final composite is then transformed to T_2 and pre-multiplied by our T_1 network. The final result emerges as T_3 , and this is transformed to a two-port S-matrix.

The manipulation of series and shunt networks when added to two-port give the designer valuable information on the behavior of a circuit with network modifications. The utility of $[S]$, $[Y]$, $[Z]$, and $[T]$ matrix descriptions enable complex networks to be studied with a variety of terminations and feedback. However, an easier and streamlined approach is provided through mapping of network parameters. This mapping is achieved by permitting the availability of network values such as reflection coefficient and gain as a function of a variable impedance placed anywhere in the circuit.

The expression that relates any n -port S-parameter to a one port termination at port k is a variation of (4.22), however written here in a more general form as,

$$S'_{ij} = S_{ij} + \frac{S_{ik}S_{kj}}{\frac{1}{\Gamma_k} - S_{kk}}. \quad (4.25)$$

This expression permits the mapping of the Γ complex reflection plane onto the S plane. The terms S_{ij} , S_{ik} , S_{kk} , and S_{kj} are complex and assume different S-parameter quantities depending on the application. As an example, the earlier introduction of (4.22), permitted the input reflection coefficient of a two-port with arbitrary termination Γ_t to be given by,

$$\Gamma_{\text{in}} = S_{11} + \frac{S_{12}S_{21}}{\frac{1}{\Gamma_t} - S_{22}}. \quad (4.26)$$

If $|\Gamma_{\text{in}}| = 1$ for all possible reflection angles, then we have,

$$1 = \left| S_{11} - \frac{S_{12}S_{21}\Gamma_t}{1 - S_{22}\Gamma_t} \right| = \left| \frac{S_{11} - \Delta\Gamma_t}{1 - S_{22}\Gamma_t} \right| \quad (4.27)$$

with Δ the determinant of the S matrix and (4.27) is recognized to be a bilinear transform [179]. For $|\Gamma_{\text{in}}| = 1$ we are able to find values of termination, Γ_t , that will fulfil the requirement of forcing $|\Gamma_{\text{in}}| = 1$. An identical situation exists for the output plane provided by the calculation of S'_{22} and fulfilling the condition of $\Gamma_{\text{out}} = 1$. Therefore, we are able to find a map for the input and output reflection coefficient plane for a two-port network, where the map is a contour of

all available magnitudes and angles of Γ_t that will force Γ_{in} or Γ_{out} to unity. The description of this process is shown in Figure 4.10.

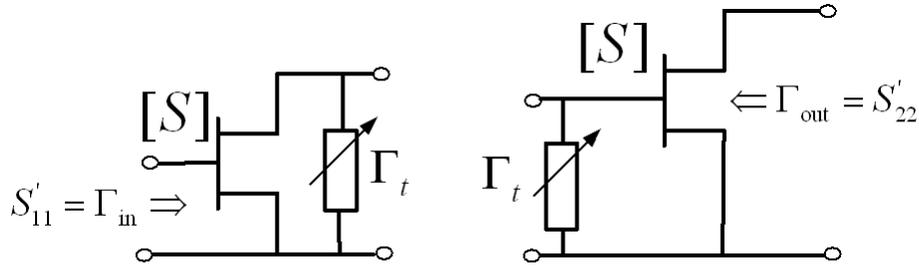


Figure 4.10: The input and the output reflection coefficient is found for all values of Γ_t and is a function of the device two-port $[S]$ parameters. The values that Γ_t will take on will be unique, as the desired values of Γ_{in} and Γ_{out} must be unity.

Complete mapping solutions for a two-port S -parameter set are available for all possible one port termination topologies. This includes series, shunt, and their connection between any set of two-port terminals. The following networks can all be mapped as a function of a one-port with reflection coefficient, Γ_t :

The active two-port can assume any terminal as the reference terminal, therefore, producing maps for common source, gate, and drain configurations. Our work focuses on the common source configuration.

Assessing maps for series and shunt feedback configurations, as shown in Figure 4.8, requires the two-port S -parameters to be transformed to three-port S -parameters, described by (4.28). There are two formats required for the transformations. One provides for a common reference node, usually designated as the signal ground, and supports series mapping. The second transformation provides for no reference point, the so-called floating three-port or indefinite S -parameters. This transformation supports the mapping of a shunt connected one-port which may be connected to any set of two-port terminals.

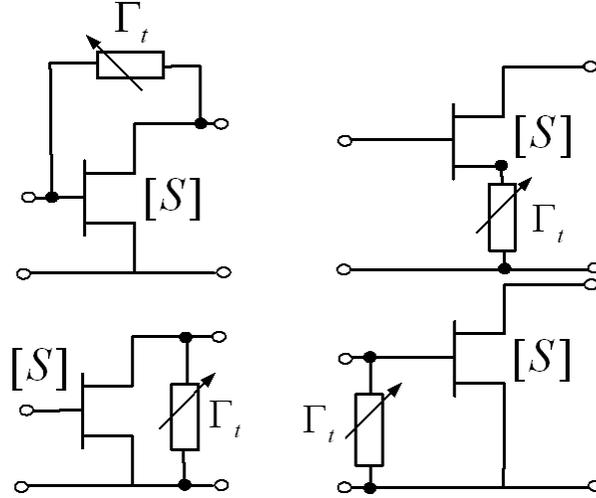


Figure 4.11: An active two-port network with S -parameters, $[S]$, is modified with the placement of a one-port network with reflection coefficient Γ_t . It is important to note, no reference terminal is delineated, or is required.

$$S_{ij}^{3-port} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{gg} & S_{gs} & S_{gd} \\ S_{sg} & S_{ss} & S_{ds} \\ S_{dg} & S_{ds} & S_{dd} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \quad (4.28)$$

The transformation to common ground three-port S -parameters is determined by converting the two-port S -parameters to Y -parameters. The transformation to floating three-port S parameters is determined by converting the two-port S -parameters to Z parameters. These transformations are found first by conversion of the two-port S -parameters to two-port Y -parameters or Z -parameters, followed by conversion to the three-port S -parameters by use of a set of nine equations. For a HFET device in any configuration, embedded in a three-port common ground structure as shown in Figure 4.12 we have,

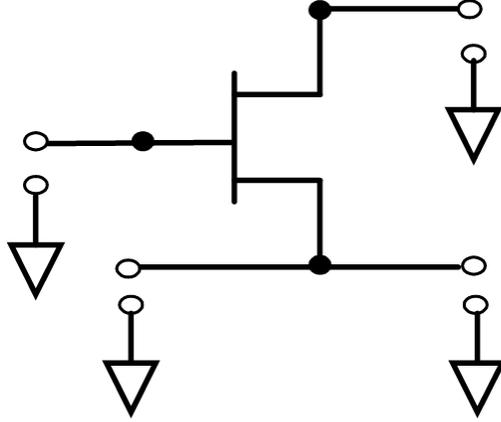


Figure 4.12: The common ground three port S -parameters can be used in conjunction with the mapping function to evaluate the effects of series feedback of an HFET device.

$$\begin{aligned}
 S_{gg} &= \frac{1}{2\Delta} [(1 + Y_{12})(1 + Y_{21}) + Y_{22}(2 - Y_{11})] \\
 S_{gs} &= \frac{1}{\Delta} [Y_{11}(1 + Y_{22}) + Y_{12}(1 - Y_{21})] \\
 S_{gd} &= \frac{1}{\Delta} [Y_{11}Y_{22} - Y_{12}(1 + Y_{21})] \\
 S_{sg} &= \frac{1}{\Delta} [Y_{11}(1 + Y_{22}) + Y_{21}(1 - Y_{21})] \\
 S_{ss} &= \frac{1}{2\Delta} [(1 - Y_{12})(1 - Y_{21}) - Y_{11}Y_{22}] \\
 S_{sd} &= \frac{1}{\Delta} [Y_{22}(1 + Y_{11}) + Y_{12}(1 - Y_{21})] \\
 S_{dg} &= \frac{1}{\Delta} [Y_{11}Y_{22} - Y_{21}(1 + Y_{12})] \\
 S_{ds} &= \frac{1}{\Delta} [Y_{22}(1 + Y_{11}) + Y_{21}(1 - Y_{12})] \\
 S_{dd} &= \frac{1}{2\Delta} [(1 + Y_{12})(1 + Y_{21}) + Y_{11}(2 - Y_{22})] \\
 \Delta &= (1 + Y_{11})(1 + Y_{22}) - Y_{12}Y_{21} + \frac{1}{2} [Y_{11}Y_{22} - (1 - Y_{12})(1 - Y_{21})]
 \end{aligned}
 \tag{4.29}$$

where the Y parameters are obtained from the corresponding two-port S parameters. The two-port Y -parameters of (4.29) must be normalized for the above equations to be valid.

Normalized values are obtained by multiplying each Y -parameter by Z_0 . The two-port configuration of the device prior to transformation may be common source, gate, or drain. Hence, the ground referenced three-port parameters support series feedback either in the source, gate, or drain lead after the transformation is completed.

For a HFET device in any configuration, a floating three-port S -parameter set is used in the mapping process to evaluate the effects of shunt feedback. The HFET embedded in a floating three-port structure is shown in Figure 4.13 and we have,

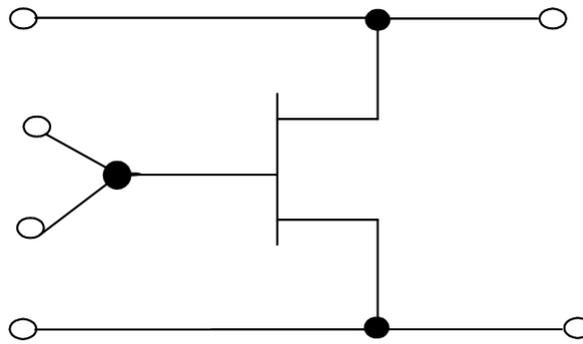


Figure 4.13: The common ground three port S -parameters can be used in conjunction with the mapping function to evaluate the effects of series feedback of an HFET device.

$$\begin{aligned}
S_{gg} &= \frac{1}{2\Delta} [(1 - Z_{12})(1 - Z_{21}) + Z_{22}(2 - Z_{11})] \\
S_{gs} &= \frac{1}{\Delta} [Z_{11}(1 + Z_{22}) - Z_{12}(1 + Z_{21})] \\
S_{gd} &= \frac{1}{\Delta} [Z_{11}Z_{22} + Z_{12}(1 - Z_{21})] \\
S_{sg} &= \frac{1}{\Delta} [Z_{11}(1 + Z_{22}) - Z_{21}(1 + Z_{21})] \\
S_{ss} &= \frac{1}{2\Delta} [(1 + Z_{12})(1 + Z_{21}) - Z_{11}Z_{22}] \\
S_{sd} &= \frac{1}{\Delta} [Z_{22}(1 + Z_{11}) - Z_{12}(1 + Z_{21})] \\
S_{dg} &= \frac{1}{\Delta} [Z_{11}Z_{22} + Z_{21}(1 - Z_{12})] \\
S_{ds} &= \frac{1}{\Delta} [Z_{22}(1 + Z_{11}) - Z_{21}(1 + Z_{12})] \\
S_{dd} &= \frac{1}{2\Delta} [(1 - Z_{12})(1 - Z_{21}) + Z_{11}(2 - Z_{22})] \\
\Delta &= Z_{12}Z_{21} - (1 + Z_{11})(1 + Z_{22}) - \frac{1}{2} [Z_{11}Z_{22} - (1 + Z_{12})(1 + Z_{21})]
\end{aligned} \tag{4.30}$$

where the Z parameters are obtained from the corresponding two-port S parameters. The two-port Z -parameters of (4.30) must be normalized for the above equations to be valid. Normalized values are obtained by dividing each Z -parameter by Z_0 . The two-port configuration of the device prior to transformation may be common source, gate, or drain. Hence, the floating three-port parameters support shunt feedback either in parallel with the source-gate, gate-drain, and drain-source leads after the transformation is completed.

In the design of negative resistance and negative conductance oscillators, the maps associated with Γ_{in} and Γ_{out} are desired. Therefore, the series and shunt feedback configurations are addressed by application of (4.29) and (4.30) with (4.25). For the common source, series feedback network the mapping equations for the input and output reflection coefficient are given

by,

$$\Gamma_{\text{in}} = S_{gg} + \frac{S_{gs}S_{sg}}{\frac{1}{\Gamma_e} - S_{ss}} \quad (4.31)$$

and

$$\Gamma_{\text{out}} = S_{dd} + \frac{S_{ds}S_{sd}}{\frac{1}{\Gamma_e} - S_{ss}}. \quad (4.32)$$

The common source shunt feedback network is given by the identical mapping equations with Γ_e replaced with Γ_s . The configurations discussed are shown in Figure 4.14 and Figure 4.15.

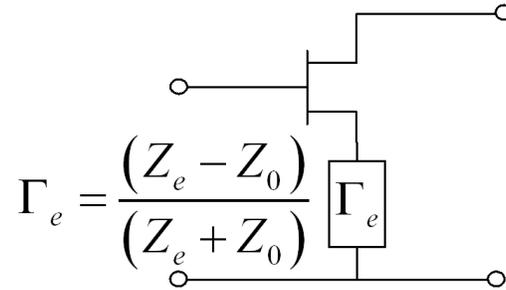


Figure 4.14: The active device with series feedback impedance, Z_e . If the impedance is provided by a capacitive reactance, we find that the map contour for the Γ_{in} and Γ_{out} trajectory are maximized outside the unit reflection coefficient plane.

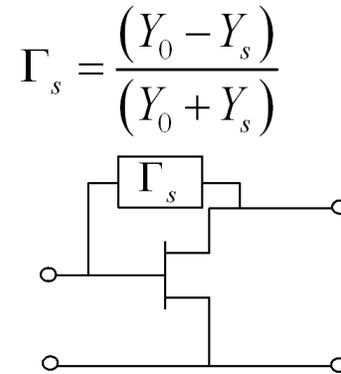


Figure 4.15: The active device with shunt feedback and the source is grounded. Maximizing the reflection coefficient outside the unit chart with either capacitive or inductive reactive feedback depends on the device two port S -parameters.

Application of series or shunt feedback clearly modifies the active device scattering parameters. The design process is to provide a suitable set of feedback and termination values or embedding elements for the active two-port. The goal is a network whose resulting two-port parameters should have a prescribed reflection coefficient greater than unity and within a targeted angular region on the reflection plane. Mapping on the chart will produce either a single trajectory or locus of points from the solution of (4.31) and (4.32). For each discrete values of series impedance or admittance, a single value of Γ_{in} or Γ_{out} is returned. However, the functions describing Γ also provide for a bilinear transform or conformal map, transferring linear line segments in the normalized complex z -plane, to regions of circles in the complex s -plane. The Smith chart is just one of those maps. The relationships provided by (4.31) and (4.32) are bilinear transformations and therefore circular regions or disks [41] are projected onto the chart. These regions of circular disks have center and radius locations with reference to the center of the chart. The locus of all points which produce a complete “map”, consists of subjecting Γ_s or Γ_e to all values encompassing the unit chart, and returning Γ_{in} or Γ_{out} . The reflection oscillator design needs regions which fall outside the unit circle of the chart. Therefore, only sectors of the circles are required. Sectors projected inside the chart, by utilizing the reciprocal of the reflection coefficient, produces families of swept arcs. Their magnitude and phase directly a function of the feedback value.

4.4.5 The mechanics of mapping applied to oscillator synthesis

In this section we investigate a fundamental approach to oscillator design, determining port termination values and feedback topology by applying mapping. The mapping process continues for each frequency of interest and feedback value. Ideally, a single feedback element value will have a suitable reactance versus frequency, and thus provides a mapping which provides the required active device input or output reflection coefficient with frequency. It is possible to find a feedback element value that is reasonably constant by adding another dimension to the problem. The selection of the termination which is frequency dependent is used to assist in

shaping the input reflection coefficient with frequency. Therefore, the goal is to maintain a fixed feedback element value, although this element may be tuned, and find the appropriate termination that gives the desired input reflection. The resulting input reflection coefficient will be a function of the termination, frequency, and the active two-port S-parameters. This process is accomplished in a Mathcad script, and is graphed as a family of loci shown in Figure 4.16.

First the active device is modified with the addition of two elements, shunt C at the gate and series C at the source. The development for the required shunt C value at the gate is discussed in Section 5.1.3. The subsequent two-port active S-parameters are again modified by the addition of series C to maximize Γ_{in} . The resulting S-parameters of the modified device are now subject to a termination other than $50\ \Omega$. Three consecutive ranges of Γ_t are displayed for three different ranges of $|\Gamma_{in}|$; at (a) $|\Gamma_{in}| = 1$, at (b) $|\Gamma_{in}| = 2$, and at (c) $|\Gamma_{in}| = 3$. The corresponding map of the required load-termination, Γ_t , is swept over the chart as a function of the desired reflection coefficient input angle, Γ_θ , discussed in Figure 4.6. The angular range of Γ_{in} is confined to zero through 180° . Due to the series feedback and shunt capacitance input termination, for $\Gamma_{in} = 1$, the termination shown in Figure 4.16 (a) is able to generate a unity input reflection for a wide range of load terminations. Both capacitive, inductive and a real terminations are included. As the required magnitude of Γ_{in} increases, the region of Γ_t shifts, rotates, and compresses as seen for Figure 4.16 (b) and (c). In (c), the load termination is confined to be inductive for $\Gamma_{in} = 3$. From (4.23), the magnitude of $\Gamma_{in} \rightarrow \infty$ as $\Gamma_t \rightarrow \frac{1}{S_{22}}$. For this specific case study, the load termination of $\Gamma_t = (0.77, \angle 124^\circ)$, or an inductive termination provides the maximum reflection coefficient. For a specific termination, shown as (ii), a series inductance with a 50 ohm termination will create a suitable $1/\Gamma_{in}$, seen as (i). For convenience, $1/\Gamma_{in}$ is plotted by placing it within the unit circle of the chart. Therefore, an appropriate termination provided by the resonator is series inductance. The simplest network for tuning would consist of a variable series inductance implemented via a series transmission line with varactor and the net R_s of the network must be less than $25\ \Omega$.

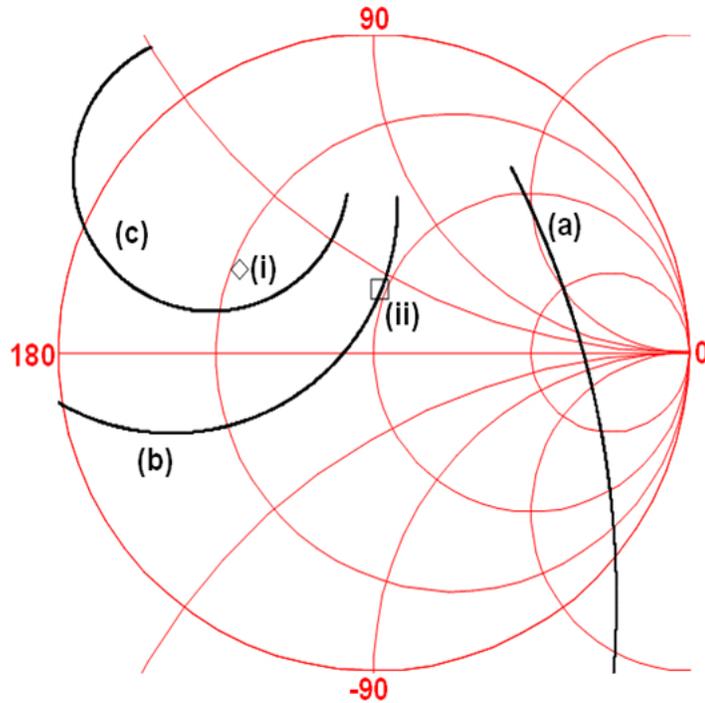


Figure 4.16: The load termination loci for three values of $|\Gamma_{in}|$: (a) unity; (b) two; and (c) three. A specific load termination at (ii) gives rise to an inverse input reflection at (i). Therefore, the series equivalent resistance for the modified active two-port is $-25\ \Omega$.

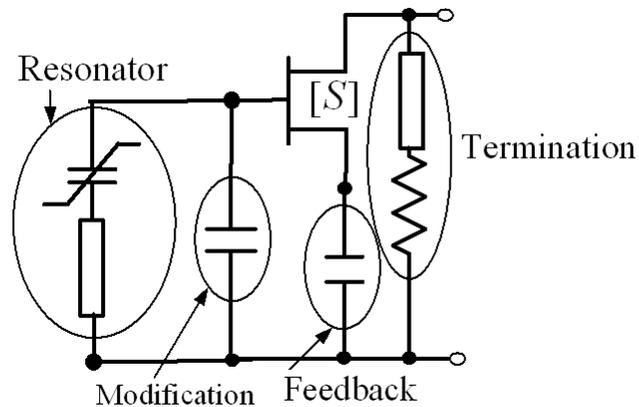


Figure 4.17: The HFET active device is modified with capacitance in shunt with the gate. Capacitance in series with the source lead provides feedback via the source lead. A series R-L termination at the drain, in conjunction with the modified shunt and series feedback elements, permits an L-C resonator at the gate to complete the oscillator termination.

4.4.6 Summary

In this section, primary focus is the interface between the resonator and the active device. Consider the ideal case, where the active portion of the oscillator has characteristics which are frequency independent and sufficiently negative in magnitude with respect to the resonator. In this case, the design of the resonator follows the classical approach whereby the resonant frequency of the frequency determining network is solely responsible for the operating frequency and the active device simply provides the required gain to overcome losses in the resonator. For many cases, this approach is adequate and is one of the primary reasons for operating a resonator with a large C/L ratio, so the active device contributes very little in determining the frequency of oscillation. Unfortunately, as the operating frequency increases the available gain decreases. The reduced gain in conjunction with the decrease in reactance of the resonator proves to create difficulty in permitting the oscillator to start. In addition, the tuning range and operating bandwidth suffer. Therefore, the focus in this section was to find an acceptable modification of the active device impedance and reflection coefficient with frequency, which are inseparable from the resonators reflection coefficient locus as it is adjusted with tuning voltage.

Consequently, these ideas lead this section into the concept where the active device, resonator, and interface must be co-simulated, ideally in unison. This design approach is similar in scope to a co-design methodology [10]. Dissimilar circuit functions must be brought together to complement each other to achieve improved system performance.

The next section therefore zeros on this technique of co-simulation. The key concept to develop is that the active device impedance locus should not be considered independent of the resonator reflection coefficient.

4.4.7 Co-design techniques using EM-Harmonic balance applied to hybrid VCOs

In this section we detail the concepts fundamental to first pass success of tunable oscillators based on oscillator synthesis. The approach requires integration of the design flow from circuit

analysis and synthesis, circuit artwork layout and generation, and co-simulation of EM and large signal analysis. The design process is iterative. However, quick convergence is realized if the approach to design and synthesis is completed correctly. The approach we take is original in scope and ties together a number of key elements associated with the critical resonator-active device interface.

Obtaining first time success of a design without network adjustment requires attention to several details. A co-design methodology is essential; coupling the active network operation, artwork of supporting element pads and lines, and the coupling between circuit elements and the resonator characteristics. In this work, we introduce a design flow technique that permitted first pass success of a C-band oscillator for 3.8 to 5.8 GHz operation. Final design and simulation showed excellent agreement, whereby prediction of tuning, output power, and harmonics were within a few per-cent of each other. Central to the technique is coupling electromagnetic and harmonic balance simulation analysis, and design methods introduced in various sections of this dissertation.

The development of this oscillator carries through on the concept introduced in Section 2.4.1: design of the power transfer oscillator. In the oscillator developed here, lower power device technology demonstrates wide tuning characteristics with excellent phase noise. The oscillator is operating at carrier frequency or at the final channel however with substantially lower phase noise and lower power levels while still maintaining high efficiency. The role of this source then is to phase lock the subsequent power oscillator via the use of a low noise high injection level phase detector and a phase lock loop.

The C band oscillator designed here utilized the mapping techniques discussed earlier in Sections 4.4.2 and further discussed in Section 5.1.3, and is shown in Figure 4.19. A Si-Ge HBT was selected for this work. The design incorporated identical circuit core topologies, except for the resonators, whose two transmission line lengths are unique, as seen in the left side of the photo of Figure 4.19. These oscillator topologies are both shunt configurations and are operated as negative conductance oscillators. The reference node is the base and therefore, this

oscillator configuration uses series feedback. However, the feedback is applied in series with the base (gate) as opposed to the emitter (source). The circuit topology is the dual of Figure 4.10, with the active device rotated. Consequently, the base (gate) is common in lieu of the emitter (source). The mapping is accomplished via the application of the ground referenced three-port scattering parameters. However, the common node is the base not the emitter. Therefore, a prior transformation is required, translating the common emitter scattering parameters to the common base. This configuration including the elements that are the basis for the mapping is seen in Figure 4.18.

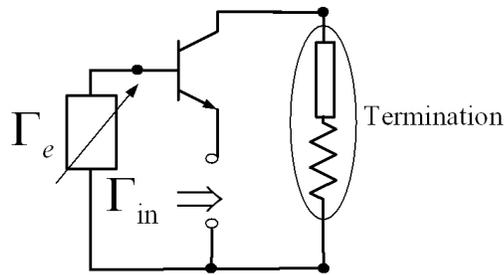


Figure 4.18: A reflection oscillator using a HBT in common base configuration. An input reflection coefficient map is generated from a set of series base feedback reflection coefficients and collector terminations versus frequency. In this design synthesis, two unique values of Γ_e are found to uniquely center Γ_{in} over the operating frequency range.

The mapping calculation used in this design is similar to the mechanics discussed in Section 4.4.4. The mapping process assisted in identifying the limits in achieving tuning bandwidth and therefore, the motivation in selecting the specific topology and active device.

The selection of the series feedback element value and the load termination values are used to modify the device input reflection coefficient, as discussed earlier. The selection of the series base inductance, (c) and (d) of Figure 4.19 must factor in the parasitic of the printed circuit board (PCB) traces and pads, and the self resonant effect of the capacitor body and case dimensions. This element, although a capacitor, is actually providing the role of series base inductance. The capacitor element is operating above its self-resonant frequency and

this design choice is deliberate. The mapping process provided the insight into the selection of the Γ_e magnitude and phase in order to properly orient the magnitude and phase of Γ_{in} . Consequently, the physical size of the capacitor is different for each oscillator core circuit as the inductive reactance which determines Γ_e is unique. Furthermore, without recourse to printing the inductance as a microstrip line, the capacitor serves a dual role. One as the desired series feedback reactance and at the same time, the capacitor also provides a DC block. Although the base series feedback capacitor elements are identical in value, their physical size and therefore inductance is not. This is due in part to the differences in actual value of the capacitor, functioning beyond its self resonant frequency as a series inductor. The differences in inductive value arising from the variation of the self-inductance of the capacitor due to its body size and construction. The result of careful selection of the capacitor is a frequency dependent Γ_e whose reflection coefficient trajectory is appropriate to provide the desired input Γ . The lower frequency oscillator core, operating 3.8 to 4.7 GHz required a larger series reactance as compared to the oscillator operating from 4.6 to 5.8 GHz. Therefore, as seen in Figure 4.19, the physical size of the capacitors reflects in the difference in the required reactance.

The circuit diagram is presented in Figure 4.20. The resonator is very similar to the resonator detailed in the analysis of Section 2.6 and Figure 2.20. The major differences lie in the varactor position and the DC return path for the varactor. In this design, in order to minimize the introduction of parasitics, the varactor DC return is through the transmission line inductor. The coupling of the varactor which defines the sensitivity of the resonator frequency with respect to tuning voltage is still determined by the value of the series capacitor, C_c however repositioned. The coupling of the resonator to the active device, and the impedance of the transformation that results, is not controlled by a series capacitor, C_1 of Figure 2.20. Instead, the transformation is implemented by tapping the resonator and the tap position serves as the DC return path for the active device, see Figure 4.20. The load reflection coefficient is dominantly inductive, and is provided by a series combination of transmission line and lumped element inductance. Power is available from the collector, reduced in magnitude by a 6 dB

attenuator, and is low pass filtered. In the dual-core version of the oscillator, an RF switch is added to provide selection of the frequency band, and additional power amplification is added via a separate amplifier. Although this circuit is not a power oscillator, it represents a number of oscillator design techniques and measurement approaches, applicable to power oscillator development. The fundamental output power of this oscillator, prior to amplification is 6 dBm. A MMIC with a gain of 17 dB gain follows providing a total output power of 23 dBm. Operation voltage is 5 V and 3 V with a total current consumption of 110 mA. The 3 V supply predominantly serves the role of bias supply and this current consumption is low. Nevertheless, including the bias current consumption, the total load efficiency is approximately 35%.

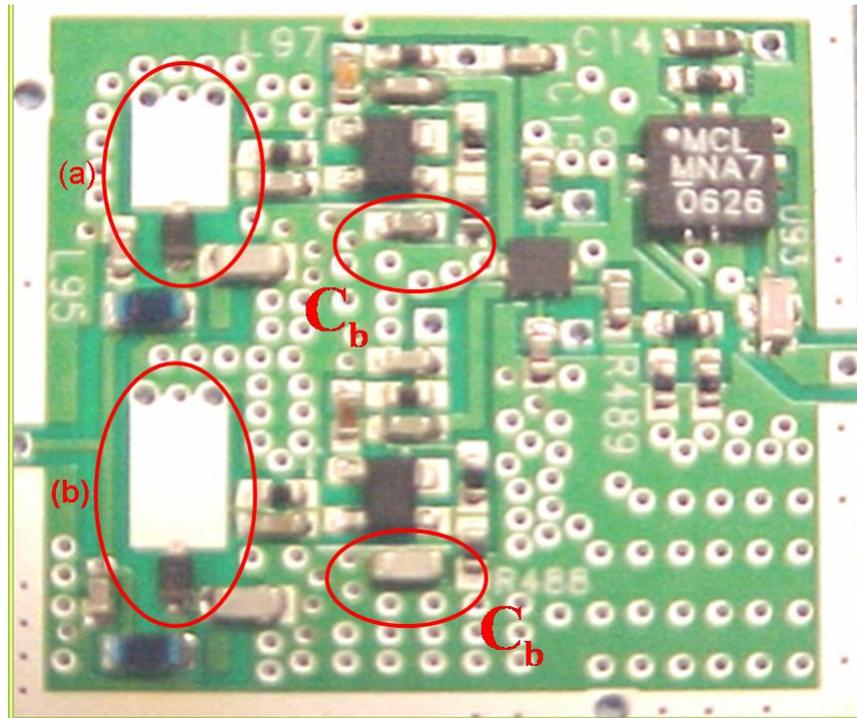


Figure 4.19: A pair of oscillators at 3.8 to 5.8 GHz. Resonators are at (a) and (b), and series feedback is provided by the self inductance of capacitors marked C_b at two locations, one for each oscillator core.

To accomplish first time success requires interaction between layout and simulation. Elec-

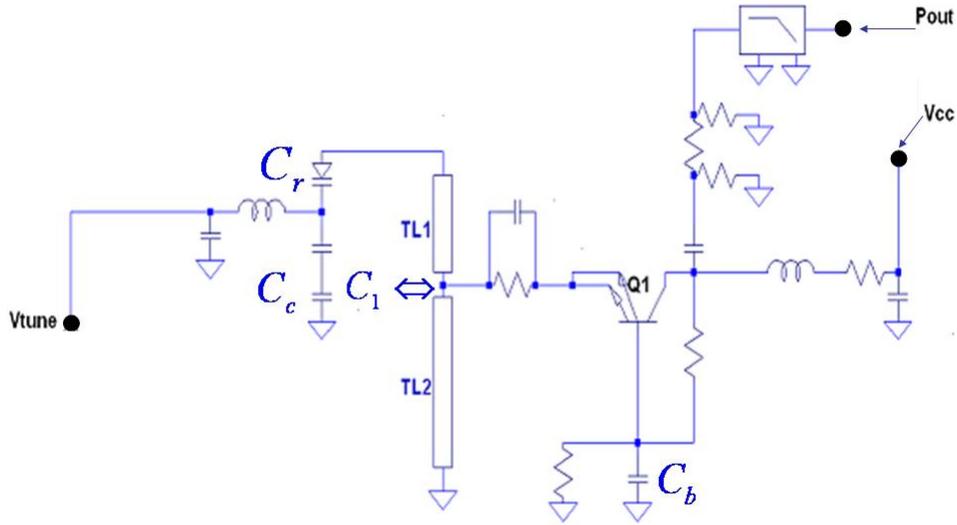


Figure 4.20: Schematic of an oscillator. Unit core oscillators are identical except for the resonators, and the oscillators combined output is accomplished via a GaAs switch and low pass filter.

Electromagnetic (EM) simulation of a hybrid layout is essential. An initial layout is driven heavily based on prior experience. Closed form EM and approximations to full EM analysis are warranted in the interest of speed. Therefore, for a first pass design, lumped element approximations are used with simplified discontinuity models of interconnects and disregard of coupled line interactions. Using initial analysis to gauge component placement and circuit sensitivity, component value, location, and the effect on oscillator performance is determined. Final placement is then supported with full EM analysis. For the network studied in this work, planar and 2.5D EM analysis are found to agree well with each other, and provide excellent agreement with measurements. The outline of a design flow is shown in Figure 4.21.

Accurate verified device models are critical to this process. Since an oscillator operating condition moves from a small signal regime to large signal self limiting operation, node voltages

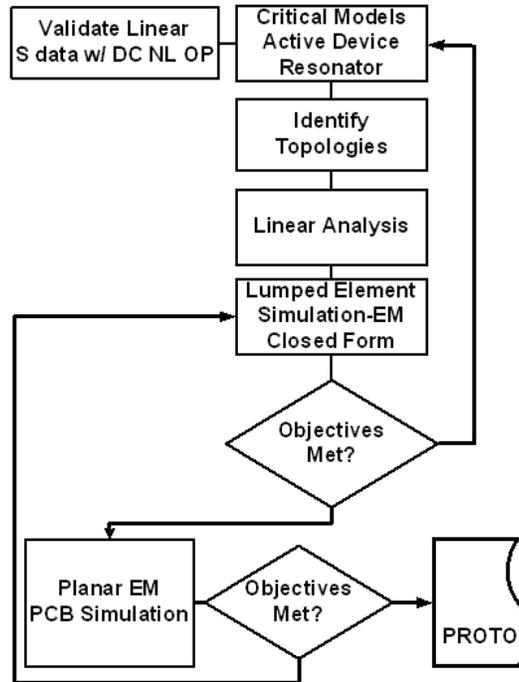


Figure 4.21: Design flow for the voltage controlled oscillator.

and bias shifts in current will occur. Unless a form of constant current bias is used, or DC feedback stabilization invoked, the operating point will shift. Therefore, the nonlinear model of the active two port must agree with small signal parameters measured over the complete operating bias regime. This is a central ingredient for the agreement of oscillator design synthesis with measurements. Many of the devices initially investigated did not meet this condition. Most device models agreed well at a fixed operating conditions, that is with a specific bias voltage and bias current. However, significant error between linear S-parameters and S-parameters derived from a nonlinear model and small signal level measured S-parameters existed over variations in bias. Therefore, significant disparity between measured and nonlinear large signal simulation occurred. To rectify this situation, alterations to the device package model were made, that permitted reasonable fitting of nonlinear derived S-parameters to small signal S-parameters over the entire bias and frequency range of interest.

Obtaining S-parameters of the printed card required importing the card DXF file and man-

ually applying ports to all component nodes. Although the transfer function between large “distantly” separate nodes is not necessarily required, it was nevertheless accomplished to insure completeness. A more significant aspect in computation time is performing EM at frequencies that are at least 5 times the fundamental operating frequency. In oscillators, significant harmonic power is present, and for accurate modeling, the EM effects at frequencies above the fundamental are key. A total analysis of 46 ports is required or just over 2100 scattering parameter terms over a frequency span of 20 GHz. The computation time is 20 hours on a dual-core Intel Xeon Machine with 4 GB of RAM. Depending on the EM simulation algorithm, the execution time may be significantly reduced. The porting of the network is shown in Figure 4.22

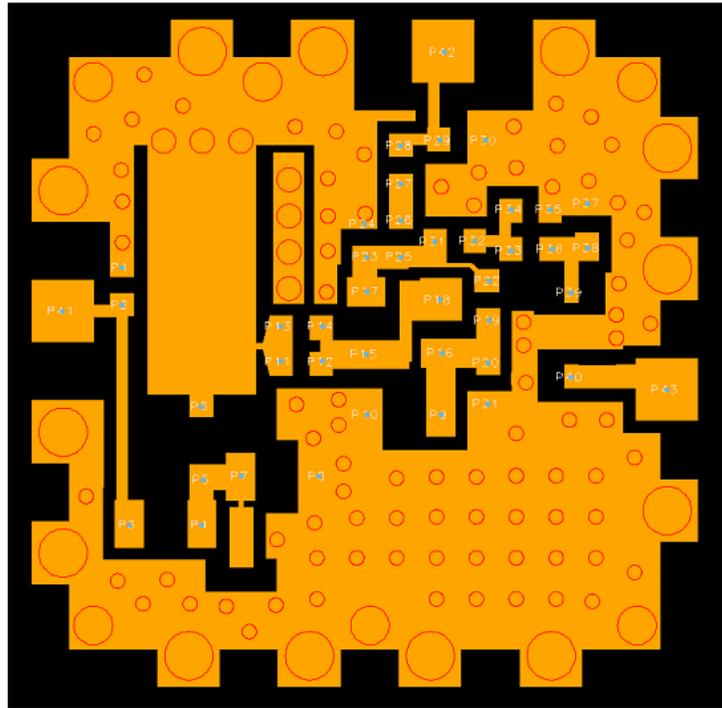


Figure 4.22: EM ports for the hybrid VCO PC Card. This card is 1/2 of the total card, however because of symmetry only one VCO core needed simulation. The only adjustment required was the trimming of the transmission line length of the resonator.

EM simulation output produces an S-parameter file, a 46x46 port matrix which is imported as an “*n*-port” network for connection to all oscillator components, see Figure 4.23. EM-Harmonic balance co-simulation is brought into Microwave Office[®], and HB simulation is conducted. The resulting measured and simulated tuning curve, and power output including harmonic levels is in excellent agreement. The agreement in tuning frequency of 4.3 to 5.4 GHz for example, is within 100 MHz of measurements, corresponding to an error of less than 2%. In addition, agreement of measured and simulated results at the fundamental, and 2nd harmonic and spectral content, is excellent. Compare Figures 4.24, 4.25, and 4.26.

The varactor model is voltage and frequency dependent and is simulated in Spice2 using the D level 1 model [11]. Verification of the model was accomplished by VNA measurement of the varactor mounted on the supporting PC card pads including interconnects. Finally, the resonator and transmission line inductor are placed together, their reflection coefficient measured on one channel of the VNA. The active circuit including emitter by pass capacitor and bias resistor are returned to a second channel of the VNA via a bias tee. In this manner both the resonator and active device small signal reflection coefficients are monitored for compliance to oscillation. Voltage tuning of the resonator permitted matching points on the resonator locus with corresponding points of the active input reflection coefficient. By performing this intermediate test step, it is possible to validate frequency tunability, and if there is a disparity in this function, the problem is isolated by separation of the resonator from the active device. This technique is exploited in Section 5.1.3 to assist in uncovering parasitics which introduce multi-oscillations in tunable oscillators.

The transistor model is based on a Gummel-Poon model with significant package parasitics added. The Gummel-Poon model is an implementation of the G-device level 1 model of SPICE2. It was progressively enhanced in the simulation tool to the point that it includes all of the HSPICE extensions to the original bipolar junction model [12]. The package model is shown in Figure 4.27. The package consists of a pair of opposed emitter pair lead frames and bond wire coupling. The supporting printed pads and interconnecting metal represent a significant

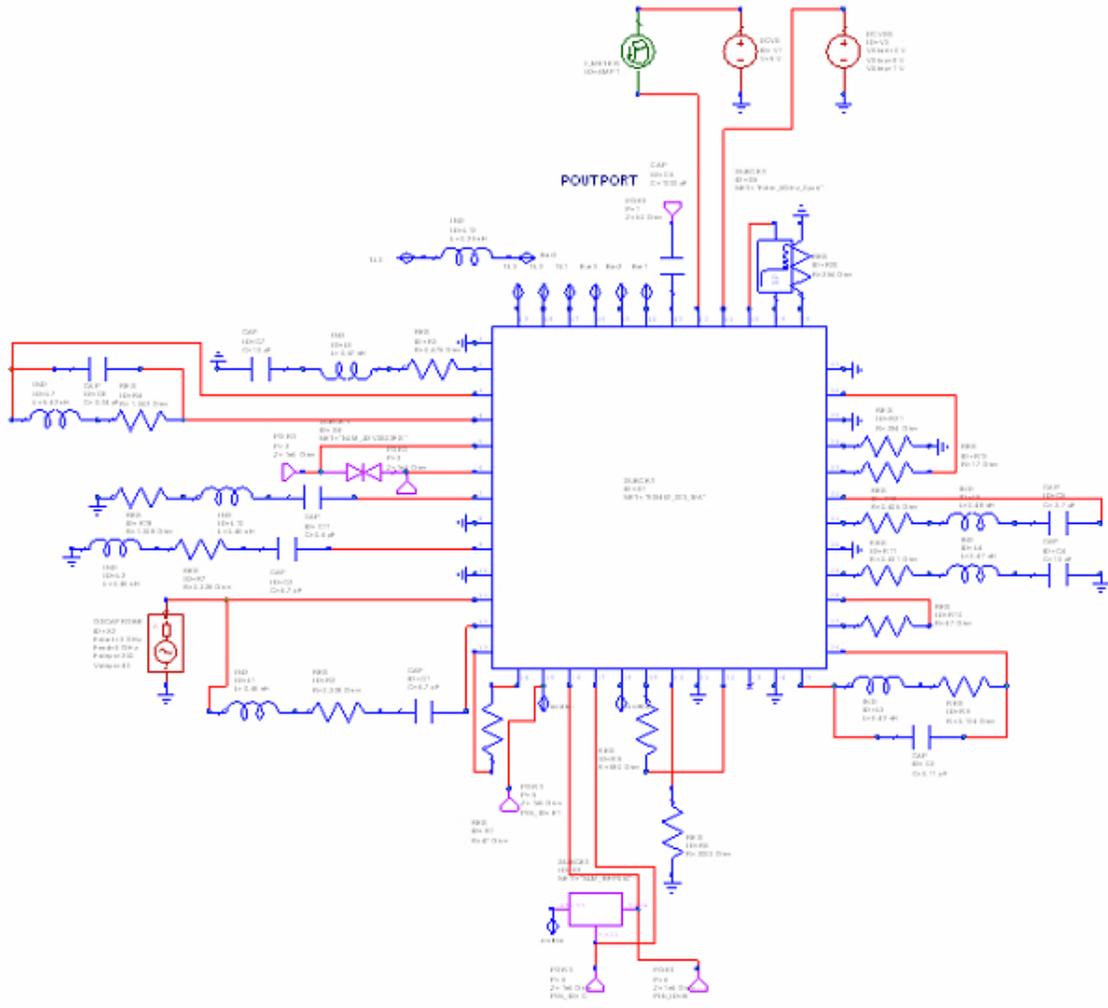


Figure 4.23: The EM-HB co simulation network. The imported 42 port network is centered, surrounding components attached to the appropriate ports per figure 4.20 and Figure 4.22.

part of the package which is not readily modeled. Therefore, capturing the composite device microstrip interconnections through EM analysis is important. During early development of this design, location of the reference planes proved vital in rapid iteration of the hybrid layout. Lumped element approximations are used with closed form EM expressions for individual lines and line-to-line coupling. Care must be exercised in determining where a component placement is made so proper port location could be assigned prior to a full EM analysis of the card. Initial analysis placed the center of the edge of the component pad centered with the PC pad.

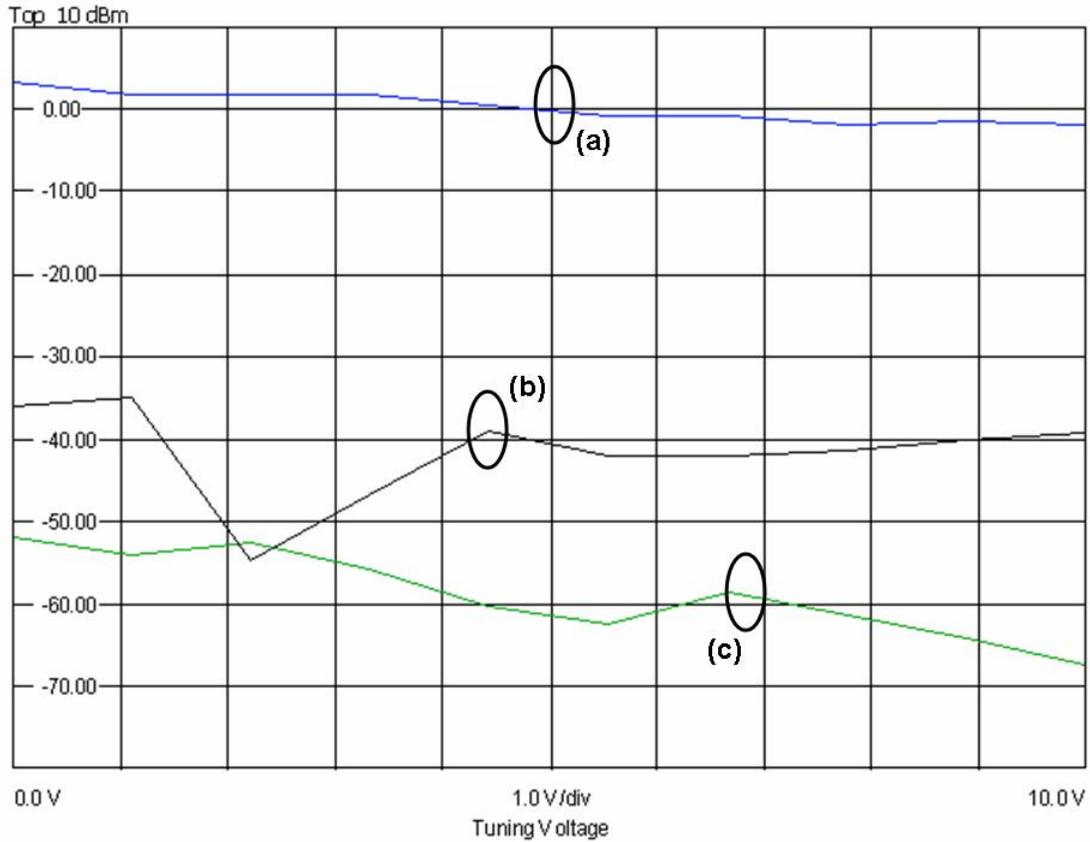


Figure 4.24: Measured oscillator output power: (a) fundamental; (b) 2nd harmonic; (c) and 3rd harmonic power. The tuning voltage range is 0 V to 10 V. The slope in fundamental power output is in good agreement with simulation; 4 dB across the tuning range and is attributed to the low cut off frequency of the filter. The notch in the second harmonic response is also attributed to the filter.

Variations of 5% in component placement contributed to less than 2% in tuning frequency error at 5.8 GHz. Several different active devices were tried during the development of these oscillators. As mentioned earlier, the disparity between linear S-parameter data and data extracted from the nonlinear model at identical bias points is a major issue. Only after the addition of proper package inductance and coupling between transistor ports did we obtain agreement between small signal and nonlinear models over a complete family of bias voltages and currents. The package model incorporated was obtained for a SOT-353 package. The mechanical drawing of the lead frame and bond wire assembly assisted in obtaining additional

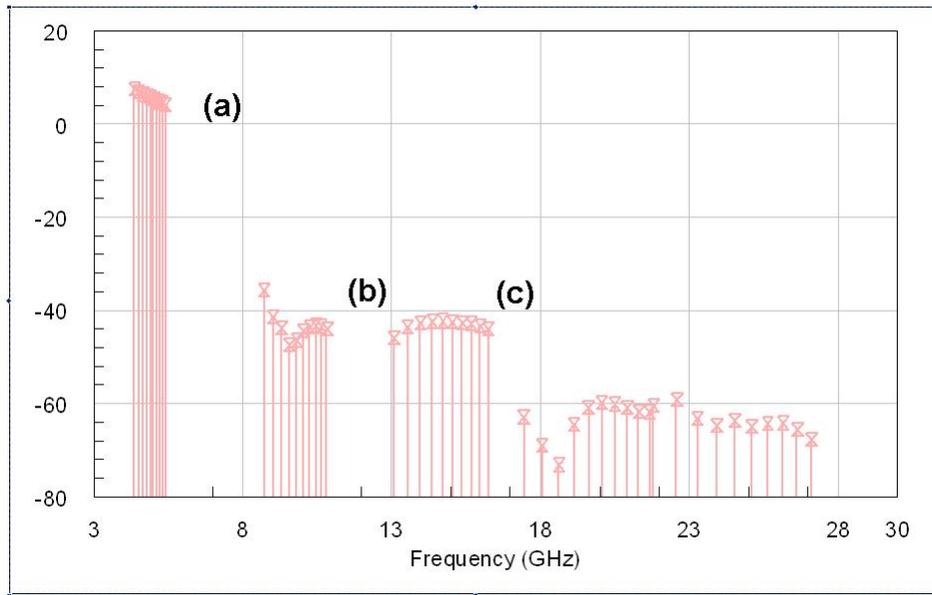


Figure 4.25: Simulated fundamental power: (a) fundamental; (b) 2nd harmonic; (c) 3rd harmonic. The agreement with notch in 2nd harmonic level is evident. Agreement beyond the 2nd harmonic is not as good since low pass filter data is extrapolated and was not measured for the filter.

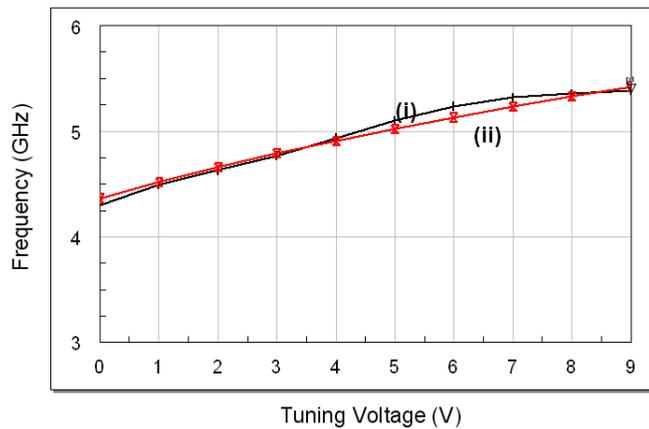


Figure 4.26: The oscillator tuning characteristic curve: (i) measured; (ii) simulated. The error between measured and simulated is less than 2.5% or less than 100 MHz frequency error at 5.4 GHz.

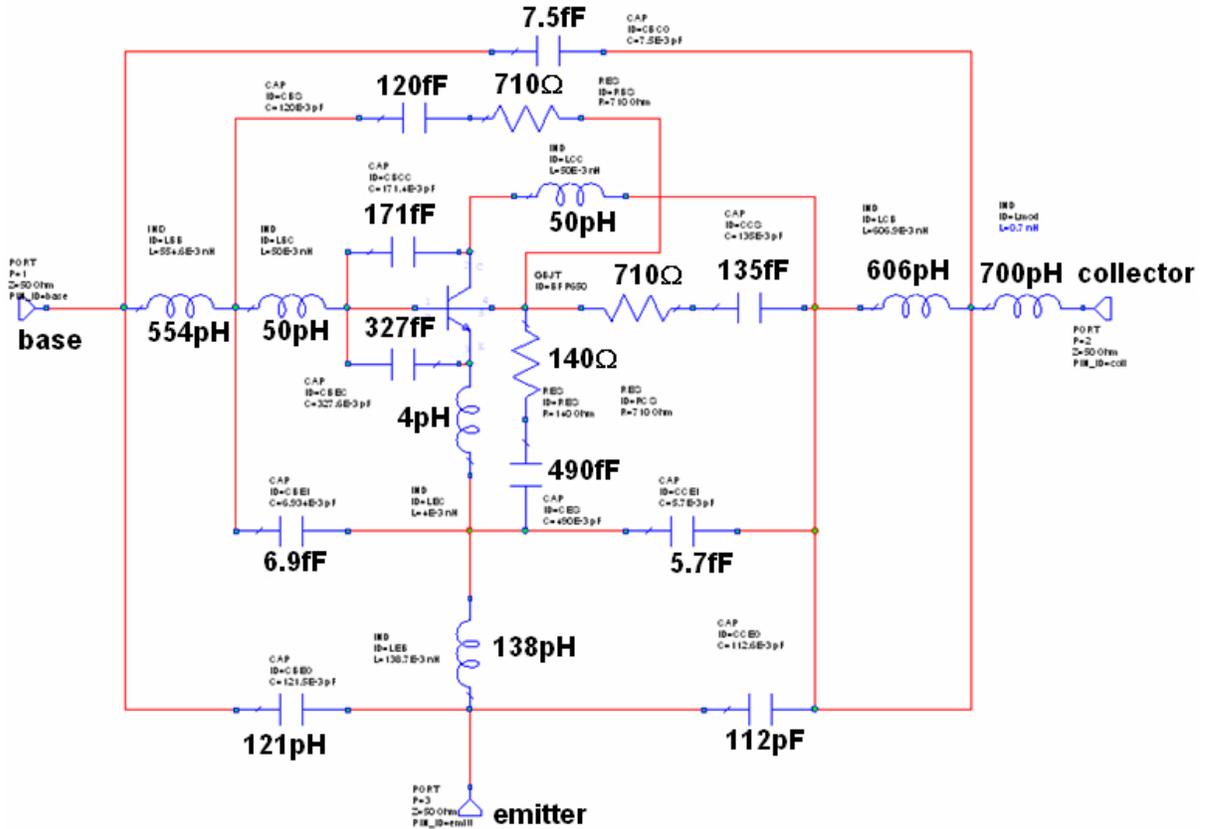


Figure 4.27: The SOT353 package model. Opposed emitter structure lead frame and differing widths of the leads must be accounted for in model development.

data to support the model process. Series inductance is added to the collector output port connection to improve modeling agreement through 6 GHz. The electrical reference plane for the package is defined at the edge of the package not including the lead. Therefore, the lead to hybrid card interface forms a step discontinuity and it is necessary to capture this element in preliminary analysis. The complete package model is shown in Figure 4.27 and the agreement between linear (measured) and nonlinear model derived, (NLM), S-parameters provided over a range of bias voltage and current are demonstrated in Figure 4.28 and Figure 4.29. In the S-parameter data shown in the figures, bias operation is shifted from 3 V and 9 mA to 3 V and 30 mA. The data presented on each chart is the nonlinear packaged modeled S-parameters

from simulation, overlaid with that of measured. Agreement and tracking of the two data sets over the complete bias range is quite good. This agreement in two-port scattering parameter values obtained from the nonlinear model with that obtained from measurement at the same bias points, is key in obtaining agreement between measured and simulated results. This is particularly true in the case of oscillator simulation. The self-limiting operation of the active device is directly linked to the change in active device impedance with changes in device voltage and current. Therefore, to capture this impedance shift accurately in nonlinear simulation requires the linear scattering parameters to be accurately portrayed in nonlinear simulation.

In addition, by capturing the Rollets stability factor K , we capture all of the two-port S-parameters. This additional calculation of K is an added test on the agreement of small signal measurements to that of the non-linear model. The numeric difference in the stability factor K , simulated versus measured, is less than .07 over the frequency span of 10 MHz to 6 GHz.

4.4.8 Resonator loaded Q in oscillators, the complex Q , and active Q measurement

The tunable oscillators developed in the previous sections serve as the reference source to the power oscillator. Therefore, in wideband phase lock systems based on the PLM architecture, the power oscillator will acquire many of the attributes of the lower power sources. For example, the noise performance of the power oscillator is partially contingent on the noise performance of the oscillators designed using the previous techniques developed in Section 4.4. Two of the key parameters in setting oscillator performance are captured in the product $P_s Q_L^2$, see (2.44). In this section, we focus on improving the loaded Q , verifying this improvement through measurement and simulation, and collaborating the changes in oscillator signal-to-noise ratio with changes in the loaded Q .

Two unique circuit design concepts are introduced in the oscillator design presented in Section 4.4.7. First is the application of a common DC return of two key RF elements, the varactor and the active device. Second, is the method of providing impedance transformation

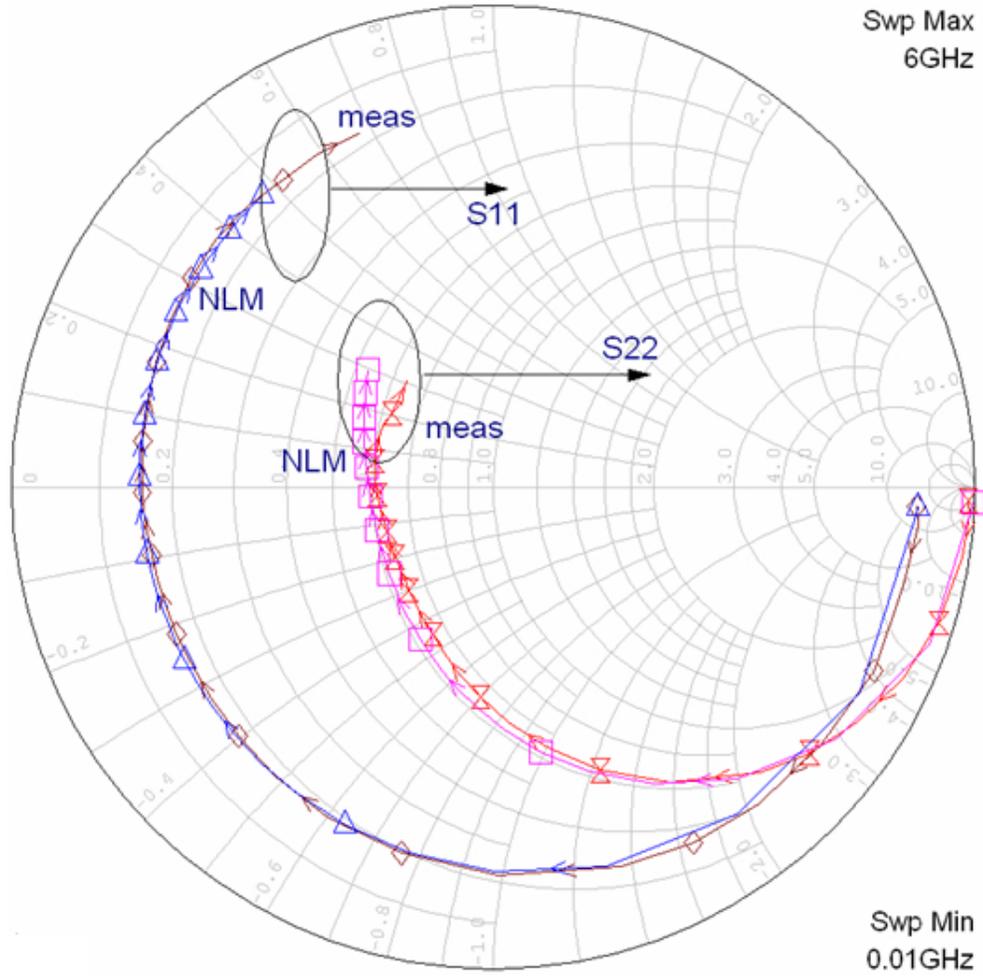


Figure 4.28: S-data captured from measurements and nonlinear simulation at 3-V and 9 mA.

between the active device and the resonator without the introduction of new circuit elements. The varactor and the emitter of the active device are returned to a common reference node via a common branch, the resonator transmission line. This topology minimizes the addition of parasitics and provides a convenient method for varying the impedance translation between the resonator and the active device input. This is accomplished by tapping the resonator. The position of the tap on the resonator influences the loaded Q and the resulting phase noise.

Reference [13] discusses the relationship between the oscillator phase noise, the influence of the open loop gain and the unloaded Q , and the location of the tap point on the transmission

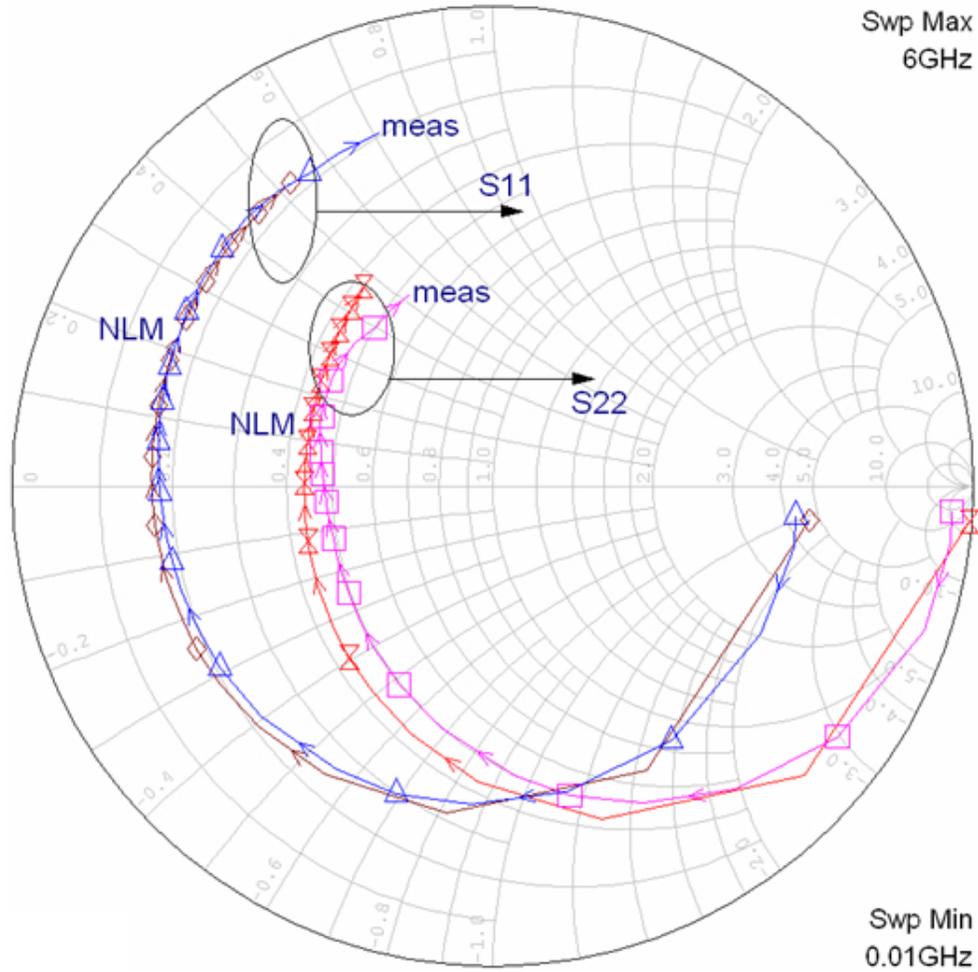


Figure 4.29: S-data captured from measurements and nonlinear simulation at 3-V and 30 mA.

line resonator, see Figure 4.20. The tap point is provided by the adjustment of lengths of transmission line, designated as TL1 and TL2. The tap points and the transmission line together with the remaining tuning elements which compose the resonator, see Figure 4.20, C_r and C_c , provide the reflection coefficient, Γ_e .

Circuit analysis provides the evaluation of the loaded Q [42]. This is accomplished by recasting the closed loop oscillator as an open loop system and utilizing the open loop S-parameters to calculate the open loop gain.

The circuit analysis process begins by application of the floating point three-port S-parameters

introduced in Section 4.4.4. Feedback and terminations, other than the external load where power is delivered, are added to the active device. The composite active subnetwork is subsequently converted back to a set of modified two-port scattering parameters. The feedback and termination elements are then optimized to obtain the desired reflection coefficients for this subnetwork as discussed in Section 4.4.5. The analysis of this subnetwork is ideal in the sense that all necessary support components are absent, for example bias and decoupling networks.

The external load impedance, all bias elements, the varactor tuning network and resonator, and all decoupling elements are then incorporated back into a representative oscillator network, whereby the network remains in an open loop condition. The active subnetwork including the active device, feedback, and terminations, is disassembled. The terminations and feedback elements are noted and to be reincorporated into the open-loop system. Next is the evaluation of the loaded Q , Q_L .

The open loop loaded Q is accomplished first through small signal linear analysis, applying the scattering parameters to the open loop cascade of network elements, and evaluating the open loop two-port transmission gain, S_{21} . A key question is, where to break the closed loop oscillator? Since the oscillator is an autonomous system there is no need to identify a reference point, an input, or an output node. The closed loop condition forces the input impedance at some point in the loop, to adopt the self impedance at the same connecting node, and this influence around the loop migrates in both directions, backwards and forward. One approach, that is reasonable, is upon opening the loop, replace the open loop nodes with equivalent terminating impedances which existed when the loop was closed [44]. However, the impedance analysis would be evaluated at signal levels commensurate with oscillator operation.

A key assumption therefore, is that the active device is unilateral, or sufficiently unilateral, such that the break point is not an issue. If this is not the case, than an alternative open loop gain expression is used, [43]. However, the formulation as to where to break the loop remains the same. In the ideal case, where perfect unilateral conditions are assumed, the open loop gain

is provided by the simplified expression given as,

$$G_{\text{OL}} = \frac{S_{21}}{1 - S_{11}S_{22}}. \quad (4.33)$$

If the assumption of a unilateral active two-port is unacceptable, then we consider an approach whereby the open-loop transmission model consists of an infinite cascade of identical networks, each section having an input impedance equal to the previous stage output impedance. In this case, each stage is loaded at its input and output by an identical impedance. Therefore, the reflection coefficients are identical. The open-loop gain is then calculated by finding the open loop output and input signal voltages. The resulting open-gain equation is an extension of (4.33) and includes the characteristic impedances of the open-loop network to ensure that the open-loop gain expression does not depend on the characteristic impedances used in defining the S-parameters. For this case, as cited by [43] and also in [48], the open-loop gain is given by,

$$G_{\text{OL}} = \frac{S_{21}}{1 - S_{22}\Gamma_{\text{in}}^{\text{OL}}} \quad (4.34)$$

where $\Gamma_{\text{in}}^{\text{OL}}$ is given by,

$$\Gamma_{\text{in}}^{\text{OL}} = \frac{1 + \Delta \pm \sqrt{(1 + \Delta)^2 - 4S_{11}S_{22}}}{2S_{22}} \quad (4.35)$$

with Δ the determinant of the composite S-matrix of the open-loop system.

The necessary terms needed for evaluation of the open loop loaded Q are a function of the open-loop transmission gain and phase and are calculated from the oscillator open-loop S-parameters. An expression for the loaded Q , applicable to a generalized complex overall network, is provided by the complex Q factor, Q_{sc} . The complex Q factor as applied to oscillator networks is referred to as the spectrum-based quality factor [14]. This particular definition of Q factor is signaled out as it is specifically targeted to noise analysis [45] and the oscillator configuration. A complete and generic expression for the loaded Q of the oscillator network is

therefore given by Q_{sc} as,

$$Q_{sc} = \frac{\omega_0}{2} \left(\frac{\partial G_{OL}}{\partial \omega} \right) + j \frac{\omega_0}{2} \left(\frac{\partial \varphi_{OL}}{\partial \omega} \right) \quad (4.36)$$

where G_{OL} and φ_{OL} are the open loop gain and phase of the oscillator network respectfully. The second term of (4.36) is of particular interest since it is accurately and readily calculated in simulation.

The loaded Q of a resonant network is evaluated by either the inspection of the incremental change in the magnitude or the phase of its impedance transfer function with respect to frequency. A series $L - C - R$ network is described by an impedance function, $Z(j\omega) = j\omega L - j/\omega C + R_s$. If we calculate the change in reactance with frequency, $X(j\omega)$, we have, $dX/d\omega = 2L$. This differential is written in terms of the resonator Q as we have $Q = \omega_0 L/R_s$. Therefore, upon substitution,

$$Q = \left\langle \frac{\omega_0}{2R_s} \frac{dX}{d\omega} \right\rangle_{\omega=\omega_0} . \quad (4.37)$$

However, for a small incremental shift in frequency about the resonant frequency ω_0 , the phase shift of the network is $\Delta\theta = \Delta X/R_s$. Therefore, upon substitution into (4.37), we have

$$Q = \frac{\omega_0 \Delta\theta}{2d\omega} . \quad (4.38)$$

The term $\frac{\Delta\theta}{d\omega}$ is recognized as the group delay, τ_g , evaluated as a small incremental frequency shift about the resonant frequency, ω_0 and therefore, the resonator Q is given as,

$$Q = \frac{\omega_0 \tau_g}{2} . \quad (4.39)$$

The second term of (4.36) contains the group delay term, and in our network predominates in the oscillator design. In this work, we found the second term is over four times larger than the first, with the open loop gain quite flat over the operating frequency range of the oscillator.

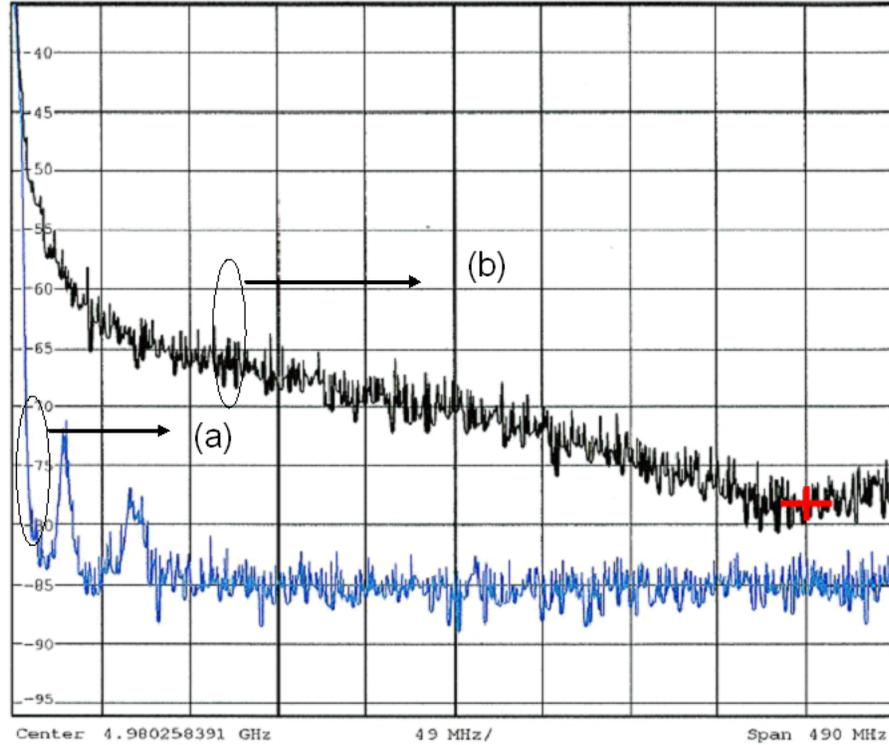


Figure 4.30: Broadband noise is injected into the oscillator via a three-port circulator. Injected noise: (a) OFF; (b) ON. The resonator embedded in the positive feedback loop of an oscillator is Q multiplied. However, at frequency offsets far away from the carrier, oscillator loop gain is negligible. Therefore, actual loaded Q is readily observed with its associated noise shaping. Observed here, the loaded Q is approximately 6, as the half power bandwidth is 414 MHz at 4.98 GHz, see fiducial marker.

Therefore, the approximation of using group delay only as a measure of loaded Q , Q_L , is appropriate and we have

$$Q_L = -\frac{\omega_o}{2} \frac{\partial \varphi_{OL}}{\partial \omega}. \quad (4.40)$$

All of these parameters are obtained from a linear analysis, whereby operating frequency and network group delay ($\partial \varphi / \partial \omega$) are part of the reserved variables in simulation tools [15]. During the design phase, the evaluation of loaded Q obtained from linear open-loop analysis is correlated with the nonlinear analysis of oscillator phase noise. This technique, served as an invaluable tool in assessing the varactor and the interconnecting metal losses, and desired impedance

transformation, that is the tap location between the active device and the resonator. This tapped position is refined in EM and HB simulation by adding additional ports to the EM imported layout file to facilitate the operation.

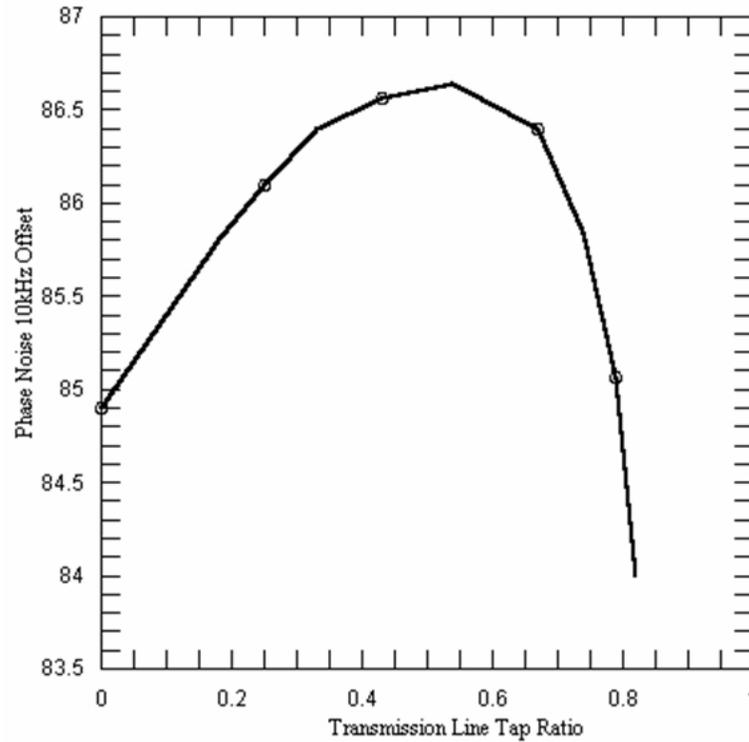


Figure 4.31: Phase noise simulated as a function of the resonator tap ratio. The associated loaded Q is 6 as measured from the noise power intersection with the noise floor, see Figure 4.30.

The combination of simulation and verification of the loaded Q is used during the design phase to set the tap position. Measurement of the loaded Q is accomplished by observing the noise half power bandwidth; either directly on a signal analyzer, if the range of the analyzer permits this measurement, or by injection of broadband noise power into the oscillator output port via a broadband circulator, see Figure 4.30. Measurement of this loaded Q permits verification of the relationship between the tap positions on the transmission line resonator and its influence on operating phase noise of the oscillator. Using this technique, it is easy to

observe in the frequency domain the intersection of the noise floor of the oscillator with that of the oscillator noise which is visible on the noise slope. Application of the power spectrum relationship gives loaded Q [16] through

$$\frac{B_{\text{osc}}}{2} = \frac{f_o}{2Q_L} \quad (4.41)$$

where $B_{\text{osc}}/2$ is the half noise power bandwidth of the oscillator.

Simulation in HB provided an assessment of the resonator tap position, the loaded Q , and the spot oscillator phase noise at 10 kHz offset. A reasonable location for the tap ratio is 0.5. This result is in good agreement with the theory for the required coupling factor for a single resonator interface to an active device. There is approximately a 3 dB shift in phase noise from the minimum at tap positions above and below the optimum value of 0.5, see [95] and Figure 4.31.

4.4.9 Summary

The integrated synthesis method for oscillator design was presented in several sections. Central to this development is the process of mapping. This graphical technique is applied to both the resonator, the active device, and their interface. In Section 4.4.1 we present a technique for identifying if a system configured as an oscillator will start and sustain stable oscillation. The technique is significantly more straight forward to apply than techniques outlined in prior work. Integration of the mapping techniques presented in Sections 4.4 through 4.4.5 with those of circuit co-simulation lead to first pass success of a C-band oscillator highlighted in Section 4.4.7.

The design flow technique outlined in these sections permitted successful absorption of parasitics and first past design success. Very good agreement in oscillator tuning gain and operating frequency is found. Less than 2% error in predicting operating frequency and tuning gain occurred at 6 GHz. In addition, harmonic spectrum, output power, and frequency response are also in good agreement with simulation.

4.5 Oscillator load efficiency

In this section we develop the guidelines for maximizing oscillator efficiency. We first review the characteristics needed to maximize the efficiency for the bipolar active device and then follow up in the Appendix D on page 429, addressing the FET device. Our approach in calculating the efficiency is based on the selection of an appropriate describing function. These describing functions are chosen in a manner which best defines the input-output control operation of the active device. In this section we first review the modeling process for the shunt feedback oscillator, laying the required ground work to address the oscillator load efficiency analysis. However, to accomplish this task requires a model which permits moving from a closed loop positive feedback system to an accurate open loop representation. First we address the migration from a closed to an open loop model, and then second we address the load efficiency calculation for the resulting open loop system.

4.5.1 Closed loop-to-open loop oscillator model

Oscillator efficiency, tuning range, and power output are key parameters to meet in order to fulfill the role of a power amplifier replacement in the transmitter function. Oscillator efficiency is categorized into three different cases. The applicability of each case is dependent on the intended circuit function, the requirements of the designer, and the information needed to gather an accurate assessment of oscillator circuit operation. Oscillator efficiency is characterized as either load, conversion, or circuit efficiency. The conversion and circuit efficiency emphasize both the resonator and load impedance in relation to the active device parameters. The load efficiency targets the AC RF power delivered to the coupled load in comparison to the total DC input power required by the oscillator. In Section 2.5.1, the oscillator power was targeted to meet a specified load power while meeting a minimum phase noise. In this section, the emphasis is on maximizing load efficiency. The analysis is ideal as it does not factor in device parasitics, however weak nonlinearities are incorporated. The trend lines provided by the analysis are useful indicators for design work.

The oscillator model investigated includes the closed loop configuration of Figure 4.32 and the open circuit equivalent of Figure 4.33. The load efficiency is defined as

$$\eta_o = \frac{P_o}{P_{in}} = \frac{V_o^2}{2R_L V_{DC} I_{DC}} \quad (4.42)$$

where V_{DC} and I_{DC} are the oscillator quiescent operating voltage and current and V_o is the peak AC output signal voltage across the oscillator equivalent load circuit, R_L , see Figure 4.33. The transformer secondary winding, L_R , in conjunction with C_R , form the resonator, see Figure 4.32. In addition, L_R also serves as the secondary winding, L_{sec} in Figure 4.33. Therefore, the resonator implemented as an ideal transformer also provides an impedance transformation. Hence, the feedback factor is directly a function of the turns ratio, N .

The circuit model in Figure 4.32, provides for the application of DC power via a bias tee. The impedance transformation provided by the ideal transformer with turns ratio N , transforms the external load, R_E , and the dynamic input impedance of the active device. The dynamic input impedance of the device is controlled by α , where $\alpha \equiv i_c/i_e$, the ratio of the total collector to emitter current.

At resonance, the total impedance across the resonator is real and is assigned the value R_{EQ} . This impedance includes the transformed external load, R_E , and the transformed device input impedance. The ideal transformer, although assumed lossless, could take on a lossy form. In this manner, a finite unloaded Q resonator is modeled, and an additional R in shunt with R_{EQ} is added. The total collector DC input power is measured through the bias tee, see Figure 4.32, and the device base bias DC input power is assumed negligible.

The total equivalent model is reduced upon impedance transforming the external load and subsequently opening the loop of Figure 4.32 at point -X- as shown in Figure 4.33. We have replaced the active device by a current controlled current generator, αI_{in} , a resonant structure tuned to resonance, C_R and L_{sec} , and a load, R_L . The load R_L now models the transformed external load and any other losses associated with the resonant structure if added. The input diode model located at the ideal transformer winding, L_{pri} , models the dynamic relationship

between the device input voltage, V_{in} , and the device input current, I_{in} .

This class of oscillator shown in Figure 4.32, is shunt tuned. Consider first we are sensing the voltage across the resonator, V_o . Subsequently this voltage is transformed and fed back as a controlled feedback current, αI_{in} , provided to the resonator, see Figure 4.33. However, the feedback current to the resonator is dynamic. The transformed voltage, V_o , is the base-emitter input voltage V_{in} , which controls the damping or limiting function required for self-sustained oscillation. The voltage, V_{in} , will consist of a DC voltage (the base-emitter potential), and a small AC incremental voltage, v_{in} .

The factor α is expressed in terms of the active device transconductance at the device operating point. The small signal AC operation for the bipolar device provides the describing functions given by,

$$\frac{\partial i_c}{\partial v_{in}} = \alpha \frac{\partial i_e}{\partial v_{in}} = \alpha \frac{\partial I_{es} \exp\left(\frac{qV_{in}}{kT}\right)}{\partial v_{in}} \quad (4.43)$$

where I_{es} is the emitter saturation current and kT/q is the thermal voltage, a value of 25.87 mV at room temperature. Expanding on Equation 4.43 we have,

$$\alpha \frac{\partial I_{es} \exp\left(\frac{qV_{in}}{kT}\right)}{\partial v_{in}} = \frac{\alpha I_E}{kT/q} \quad (4.44)$$

where $i_e = I_{es} \exp\left(\frac{qV_{in}}{kT}\right)$. Hence, we identify the transconductance, which is evaluated at the quiescent point of operation of the device and is directly proportional to α , given by,

$$\frac{\alpha I_e}{kT/q} = \frac{I_c}{kT/q} = g_{mQ} \cdot \quad (4.45)$$

The transformer feedback models the extent of coupling between the output port (collector) and the level of feedback to the input (base-emitter) junction. The range of N is $0 < N < 1.0$ and $I_S = NI_{in}$ and $V_o = V_{in}/N$. Therefore,

$$\alpha I_{in} = V_{in}/(NR_L) + NI_{in} \cdot \quad (4.46)$$

The bipolar device is operated below the α cutoff frequency, therefore, the emitter and collector current are essentially identical, with $i_e = -i_c$. Hence, the ideal transformer-resonator combination provide a feedback voltage which is in-phase with the input current, I_{in} . Using (4.46), we obtain an equivalent input resistance, R_{in} given by,

$$R_{in} = V_{in}/I_{in} = NR_L(\alpha - N). \quad (4.47)$$

The resistance, R_{in} , is dynamic, as its value is dependent on α and therefore g_m and the feedback voltage, V_o . The oscillator self-limiting function is therefore the dynamic input conductance of the device. The device input conductance increases with increasing feedback voltage, and subsequently limiting the current available to the resonator.

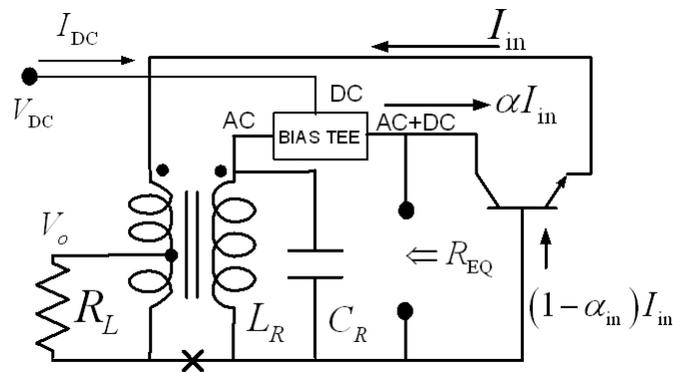


Figure 4.32: The closed loop, AC equivalent common base oscillator configured with transformer feedback. This model representation is used to develop an expression for the oscillator load efficiency. The secondary portion of the transformer with the reflected device input impedance forms a portion of the output resonator. The final output load is transformed via a tap on the transformer-resonator.

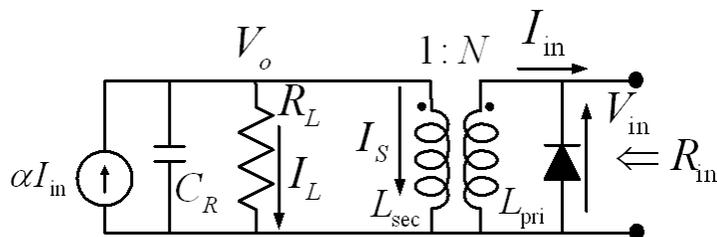


Figure 4.33: The open-loop circuit model for the common base transformer feedback oscillator uses a current controlled current source, α generator. The load and finite resonator Q losses are lumped together as an equivalent total load resistance, R_L . All reactive elements are tuned at resonance and the final network equivalent impedance is real.

4.5.2 Oscillator load efficiency analysis

The load efficiency is calculated by finding a suitable describing function for the I-V characteristic of the device and resonator network in a positive feedback loop. If a one port oscillator such as a negative resistance oscillator is chosen, a suitable I-V characteristic is derived from the static device characteristics, again with positive feedback applied. The resulting polynomial fitted to a curve demonstrating negative resistance permits finding oscillator signal voltage vs. the negative resistance, and with the oscillator signal voltage found, we find the converted power as a function of the device operating current. Although this approach is sound, it is specific to a particular device since the polynomial is unique. In lieu of this method, a more general approach is found by identifying a suitable description for the bipolar junction device which is described by an exponential characteristic and the FET, described by a square law characteristic. We will consider the bipolar device first. The FET is treated in Appendix D.

As previously discussed in Section 4.5.1, a suitable current-voltage describing function for the bipolar transistor is governed by,

$$I_{\text{in}} = I_{\text{es}} \exp\left(\frac{qV_{\text{in}}}{kT}\right) \quad (4.48)$$

and V_{in} is given by $V_{in} = [V_{DC} + V_s \cos(\omega t)]$. Upon substitution into (4.48) we have

$$I_{in} = I_{es} \exp\left(\frac{V_{DC} + V_s \cos(\omega t)}{kT/q}\right). \quad (4.49)$$

Assigning γ to the thermal voltage, kT/q , and $x = \frac{V_s}{\frac{kT}{q}}$ and rewriting we have,

$$I_{in} = I_{es} \left[\exp\left(\frac{V_{DC}}{\gamma}\right) \right] \exp[x \cos(\omega t)]. \quad (4.50)$$

The key variable x is a measure of the degree of non-linearity, as x is a ratio of the amplitude of the signal voltage to the device thermal voltage. The function $\exp[x \cos(\omega t)]$ has a known Fourier series expansion [17], given by the modified Bessel function of the first kind with order n and argument x . Describing the load efficiency of the oscillator requires the zero and first order modified Bessel functions and their derivatives. These are tabulated and have closed form properties.

Equation (4.50) has a known Fourier series given by

$$\exp[x \cos(\omega t)] = I_0(x) + 2 \sum_{n=1}^{\infty} I_n(x) \cos(n\omega t). \quad (4.51)$$

Therefore, I_{in} is written containing a DC and an AC term after substitution of (4.51) into (4.50) as,

$$I_{in} = I_s \exp\left[\frac{V_{DC}}{\gamma}\right] I_0(x) \left[1 + 2 \sum_{n=1}^{\infty} \frac{I_n(x)}{I_0(x)} \cos(n\omega t) \right]. \quad (4.52)$$

The fundamental ratio of DC to AC current for $n = 1$ is,

$$\frac{I_{DC}}{I_{AC}} = \frac{I_0(x)}{2I_1(x)}. \quad (4.53)$$

Multiplying both sides of (4.53) by x , and recognizing R_{in} is V_{in}/I_{in} with use of (4.47) where I_{in} is I_{AC} we have

$$\frac{2I_1(x)}{xI_0(x)} = \frac{\gamma}{I_{DC}NR_L(\alpha - N)}. \quad (4.54)$$

The average DC term is obtained from (4.54). In addition, we should note that due to feedback, the input voltage, V_{in} , is also given by $V_{\text{in}} = NV_o$ where V_o is the resonator peak fundamental AC voltage. Assuming the resonator Q is sufficiently high permits using the fundamental component of current only. The resonator voltage, V_0 , will be some portion of the DC operating voltage. To prevent collector saturation, V_0 at most would approach V_{DC} . Therefore, setting the product $\Theta \cdot V_{\text{DC}}$ equal to V_0 , we have at most Θ taking on the value of unity. Therefore, $x = N\Theta V_{\text{DC}}/\gamma$. Then rewrite (4.54) as,

$$I_{\text{DC}} = \frac{\Theta V_{\text{DC}} I_o(x)}{2I_1(x)R_L(\alpha - N)}. \quad (4.55)$$

The oscillator load efficiency, as defined, will be maximum if the output power is maximum and the dc input power is minimum. Maximizing P_{out} , implies maximizing ΘV_{DC} and therefore, $\Theta \rightarrow 1$; while maximizing efficiency, η , implies minimizing I_{DC} . The output power is a function of the available supply voltage, as the resonator voltage will be confined to some percentage of the operating voltage, and therefore, R_L is known since $R_L = (V_o)^2/(2P_o) = (\Theta V_{\text{DC}})^2/(2P_o)$. Using the definition of load efficiency, (4.42), we have

$$\eta_o = \frac{P_o}{P_{\text{in}}} = \frac{V_o^2}{2R_L V_{\text{DC}} I_{\text{DC}}} = \frac{\Theta^2 V_{\text{DC}}}{2R_L I_{\text{DC}}}. \quad (4.56)$$

Therefore, the problem of maximizing load efficiency is minimizing I_{DC} given in (4.55). Therefore, we desire a solution to

$$\frac{\partial}{\partial N} \left(\frac{I_0(x)}{I_1(x)(\alpha - N)} \right) = 0. \quad (4.57)$$

Using the properties for the derivative of the modified Bessel functions, we have, $\frac{dI_0(x)}{dx} = -I_1(x)$ and $\frac{dI_1(x)}{dx} = I_0(x) - \frac{I_1(x)}{x}$. Applying these relations to (4.57) and after simplifying, we have,

$$I_1^2(x) - I_0^2(x) + \frac{\alpha}{x(\alpha - N)} I_1(x) I_0(x) = 0. \quad (4.58)$$

A closed form solution with $\alpha = 1$, with N as a function of x , and for a specified V_{DC} is found

as,

$$N(x)_{V_{DC}} = \frac{-J_1^2(x) + xI_0^2(x) - I_0(x)J_1(x)}{(-J_1^2(x) + I_0^2(x))}. \quad (4.59)$$

A graphical plot of this relation is interesting, as the efficiency realized for a given N and the x value chosen for a specified V_{DC} , reveals the advantage of higher operating supply voltage provided the proper N or coupling factor is chosen. The efficiency becomes less sensitive to changes in the transformer coupling factor, N , as the operating voltage increases. Shown in Figure 4.34 is the value of N , which maximizes the efficiency for a given value of x , where $x = Nk$ and $k = V_{DC}/\gamma$ and Θ and α are set to unity. The V_{DC} is fixed to 5 V. In Figure 4.35 the value of the feedback factor N , is shown as a function of x .

These graphs do not maintain a constant x , and consequently the resonator output voltage and feedback input voltage are swept. The results for this case demonstrate an increased efficiency with an increased N and the optimum is broad as V_{DC} is increased. As x increases so does the base emitter junction input voltage for a given N . Relative to the thermal voltage, γ , large x implies a greater degree of nonlinearity and an increased signal distortion. Therefore, the operating Q of the resonator must be sufficiently high to justify the use of sinusoidal voltage and current in our analysis.

As a practical matter, designing for a fixed x is an alternative. The proper feedback factor N , will maximize for a different value and range of x chosen. Plots of load efficiency for this approach, and the required load resistance to realize the output power without voltage saturation for a specified N , are shown in Figure 4.37. In this graphic I_{DC} is set equal to 30 mA. As x increases, so does R_L , so as to maintain the same P_o without voltage saturation.

The required DC operating voltage is constrained by γ , x , and N . In addition, an arbitrary DC voltage of 3 V is added to the calculation of the required DC voltage to ensure no saturation, see Figure 4.36. The oscillator load efficiency as a function of N with x fixed is shown. The required V_{DC} is shown for each value of x and is a function of V_o and N . Efficiency increases with V_{DC} and, the required value of N is broader.

In this section, the modified Bessel functions are used to describe the best case efficiency

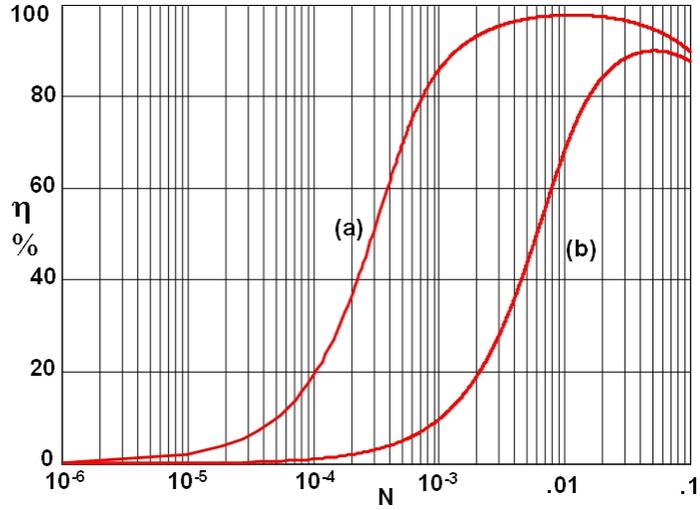


Figure 4.34: The oscillator load efficiency maximizes for specific feedback factor N . In (a) the V_{DC} is 100 V while in (b) 5 V. The broad optimum range in N with $V_{DC} \gg \gamma$ is evident.

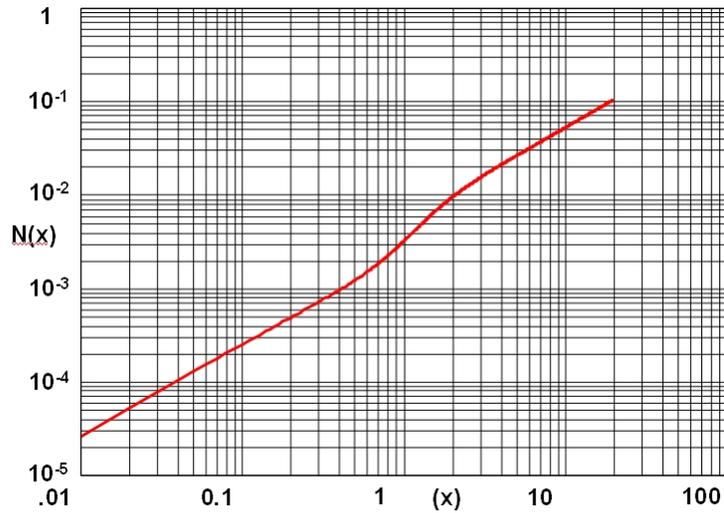


Figure 4.35: Feedback factor $N(x)$ increases nearly linearly with an increase in x . For this case, V_{DC} is 5 V. For x in the range of 1 to 10, N is in the range of 0.003 to 0.05

for a bipolar oscillator. The resulting functions imply a narrow conduction angle as x increases. This is not surprising, as the load efficiency analysis outcome for the oscillator, is analogous to the collector efficiency analysis of class C power amplifiers. The results share the common ingredient of narrow operating conduction operation and the resulting efficiency improvements.

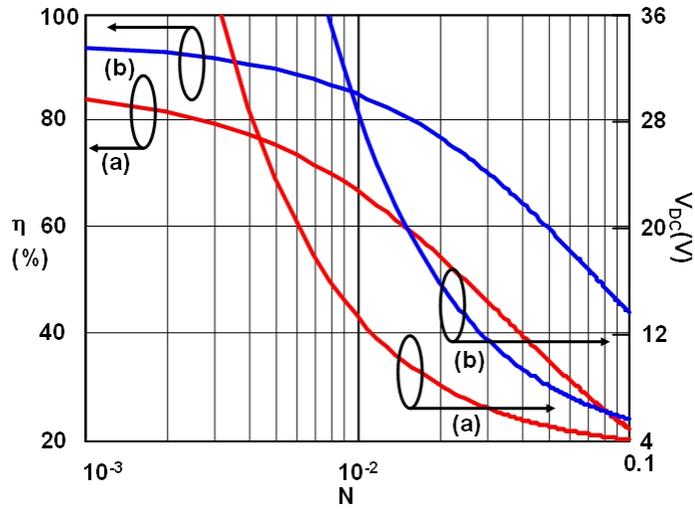


Figure 4.36: The oscillator load efficiency as a function of N with x fixed: (a) $x = 4$; (b) $x = 10$

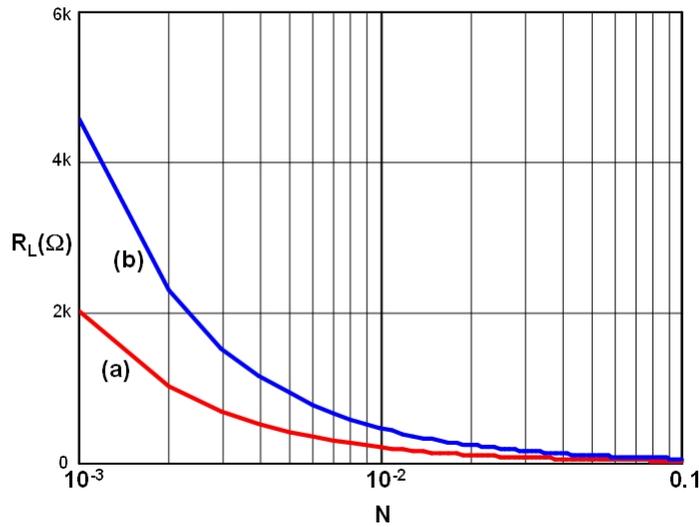


Figure 4.37: The real load impedance to realize P_{out} for case: (a) $x = 4$; (b) $x = 10$

Through several graphical solutions, the range of the feedback factors necessary to realize efficiencies greater than 50% are shown. However, high efficiency conditions are only achieved provided the operating voltage is large, and voltage saturation and current limiting are avoided.

4.6 BST based voltage tuned oscillators

The focus of this section are the circuit properties of the BST varactor when applied to voltage controlled oscillators (VCOs). Geometric implementations of the BST varactor include the interdigital capacitor (IDC) and the metal insulator metal (MIM) configuration, shown in Figures 4.38 and 4.39.

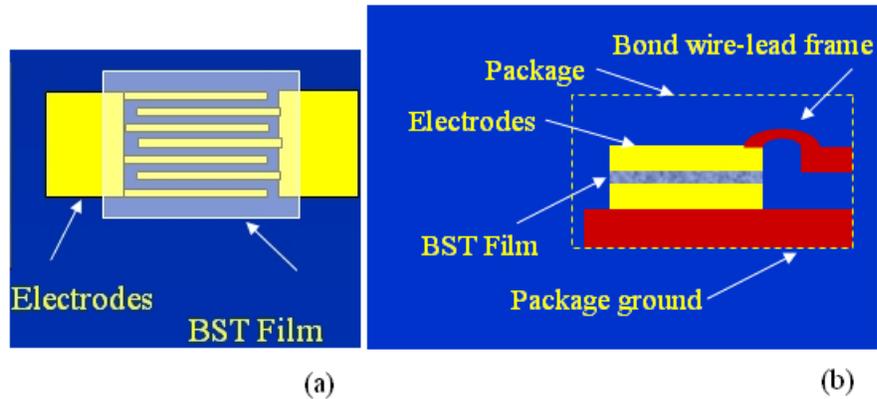


Figure 4.38: The BST varactor geometries investigated: (a) The interdigital (IDC) varactor capacitor; (b) The metal insulated metal or MIM capacitor.

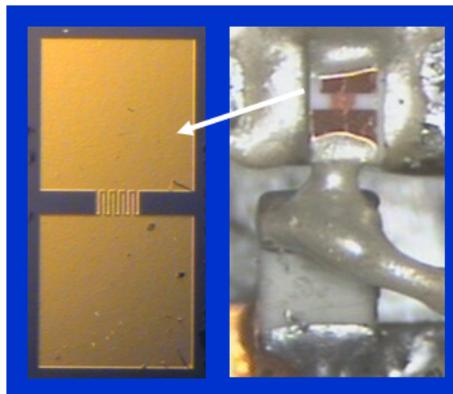


Figure 4.39: The BST IDC varactor shown here, provides for high breakdown voltage operation and smaller capacitor values as compared to the MIM varactor. Shown here the IDC varactor is inserted in series with a higher Q porcelain capacitor to increase total Q .

The emphasis in this and subsequent sections are the unique circuit characteristics of the BST based VCO. In this work, the unique operation of the tracking phase lock loop enabled the BST varactor to be readily measured for several circuit properties. These included varactor noise, tuning gain, tuning linearity, and tuning range limitations.

The consequence of the operation of a closed loop control circuit, is the ability to uncover operating properties of the BST varactor not readily observed in open loop systems. For example, the varactor additive noise and tuning gain nonlinearity as well as tuning range limitations are detected with less effort. Since the frequency drift of the oscillator is minimized and frequency stability is improved, measurement accuracy is increased. The varactor induced tuning range restrictions addressed in Section 2.5.2 are readdressed in this section. The consequences of the application of the BST based VCO in specific systems, such as the PLL, requires modification of the parameter ε_1 and is new development associated with our work.

Due the $C - V$ square law characteristics [97], the BST varactor demonstrates a number of different circuit responses as contrasted to the junction varactor. Significant effort has focused on exploiting the square law characteristics for filter and phase shifter applications. This is to be expected, as the multi-signaling handling properties of devices with nearly square law voltage characteristics minimizes multi-tone distortion. However, surprisingly little investigation was expended utilizing those same attributes and their associated benefits when applied to the oscillator circuit function. Investigators were surprised with the little effort required to obtain nearly linear frequency tuning, and failed to mention despite this benefit, the issue of reduced tuning gain and subsequent ramifications in specific circuit applications, see [98], [99], [140], and [101]. The resulting circuit response and performance is somewhat more benign when the tuning linearity influenced by the BST varactor is applied to phase shifters and filter networks. This is not because the circuit functions are any less involved, however it is due to the impact of the operation of the completed circuit as embedded in a particular system. Two resulting operating parameters stand out in this section, the phase lock hang problem addressed in this work and the intrinsic tuning linearity of a voltage controlled oscillator which benefits both

the frequency and phase-locked loop operating as a demodulator [102]. If the VCO tuning gain is linear, then the frequency demodulator implemented with a phase lock loop has low demodulation distortion.

Primarily our focus investigation of the BST varactor will include tuning characteristics, linearity, and noise. Our secondary focus is device measurement, bias tee development for operation of a high voltage varactor, varactor leakage current, and the effect of leakage current on tuning linearity and excess noise in the varactor.

4.6.1 Properties of BST VCO in tracking phase lock loop

Adjustable circuit functions utilizing BST such as filters, matching networks, and phase shifters, are well documented. However, there is an absence in the literature of the investigation of closed loop control systems utilizing the BST element. In this section, we developed a number of original circuit functions to explore the properties of BST while operating under large signal conditions, in a control system, and the noise properties germane to oscillator operational performance. This section and Sections 4.6.2 and 4.6.7 present the noise characteristics of voltage tuned oscillators incorporating a BST varactor and their properties of linear tuning afforded by BST.

The BST varactor is unique with a capacitance voltage dependency which is doubled sided and approximately symmetric. Details of oscillator tuning linearity and sensitivity are covered in 4.6.6. The tuning gain of an oscillator will go to zero as the tuning voltage goes to zero. In effect, the operation of the device capacitance vs. voltage is the dual of the junction varactor. In the junction varactor, the differential change of junction varactor capacitance with voltage increases significantly. So while the tuning gain rises with the junction varactor, it decreases with the BST varactor. An increase in tuning gain is compensated by simply applying a fixed series capacitance in line with the junction varactor. In the case of the BST varactor, the best practice is to avoid the zero tuning line point. This is unfortunate, since the ability to extend the tuning range to include zero volts is attractive, since no forward bias junction exists. However,

the voltage at zero, forces two issues to occur. One, the loss of tuning gain reduces the tracking and the ability of phase noise correction to occur in a phase lock loop. Second, if the peak value of the RF excursion voltage in conjunction with the tuning voltage bias is net positive, then the phase slope of the feedback changes “sign”. That is to say, the feedback control now represents positive feedback. This leads to a VCO push away from a stable lock point and eventually phase lock hang as demonstrated in [146]. The oscillator “push-away”, which occurs, forces the voltage controlled oscillator to move to the extreme value of the tuning range. To reacquire in a PLL, with frequency-phase detector acquisition mode, requires forcing the master or reference oscillator to move above the unlocked oscillator and to recapture phase lock. Therefore, additional circuitry is required in addition to the usual phase lock implementation of frequency steering and phase locking.

To evaluate the operation of a BST varactor used in a VCO embedded in a phase lock loop, we design an under damped loop deliberately to emphasize noise peaking which will occur with a reduction of loop gain. The oscillator is constructed as a microstrip resonator small signal design, utilizing a single interdigital thin-film BST varactor and SiGe HBT bipolar transistor. BST is used to form an interdigitated capacitor in a standard surface mount 0603 (60x30 mil) form. A 600 nm (Ba_{0.6}Sr_{0.4}) TiO₃ thin-film was deposited on a polished alumina substrate using a radio frequency magnetron sputtering technique [158]. An array of discrete interdigitated capacitors with 4.5 μm finger width and spacing and 200 μm finger length is fabricated using a two-layer metallization, 20 nm of Cr and 500 nm of Cu process, and a photolithographic metal lift-off technique. The varactor tuning and loss curve with the functional oscillator is shown in Figure 4.40. The varactor breakdown voltage exceeded 100 V in operation.

The nature of the resonator is identical to the design discussed in Section 2.6. A phase lock multiplier architecture is used, operating at 2.7 GHz, and is phase locked to a low noise 675 MHz source in a x4 configuration. Noise peaking in a locked state occurs for two reasons. First, the loop compensator is designed with the VCO and charge pump phase detector to form a dominant type II-second order or approximately third-order PLL, or the system is constructed

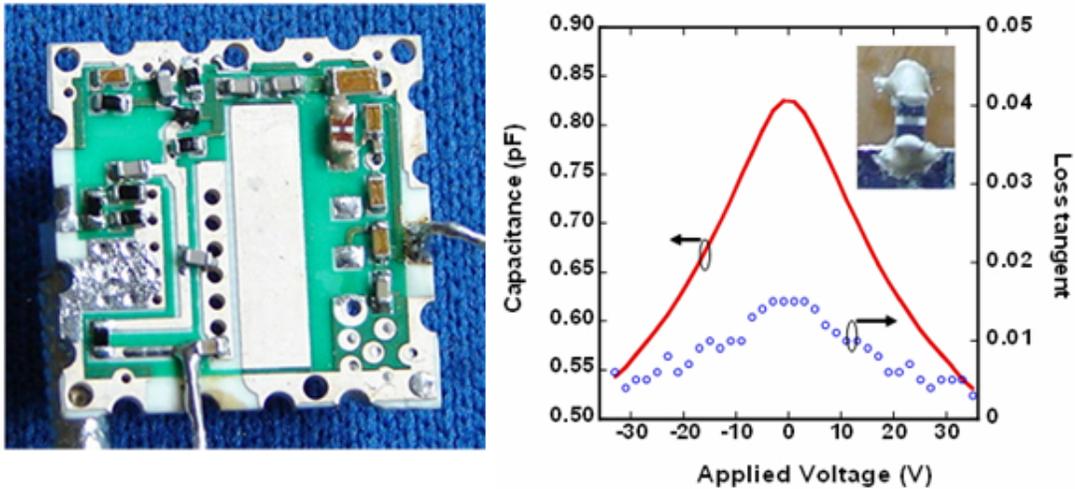


Figure 4.40: A 2.7 GHz microstrip oscillator with IDC BST varactor (located immediate right side of microstrip) and transmission line form resonator. Overall hybrid card dimension is 0.2 cm square.

with the cascade of two perfect integrators. The tendency towards third-order loop operation, is a function of the placement of the third pole location relative to the unity gain crossover frequency of the loop.

Phase lock loops operate as negative feedback control systems and to maintain stability we must prevent the open loop gain from falling at a rate of -12 dB/octave through the unity gain open loop frequency. If an excessive rate of phase shift is permitted, then the total phase shift around the closed loop approaches 360° , and loop oscillation will occur. The nature of a properly designed compensator forces an attenuation rate of -6 dB/octave through the unity gain point. Consequently, a stable feedback system is assured. Therefore, the location of any compensating zero must be prior to the open loop gain achieving zero dB on a -12 dB/octave slope. The location of any additional pole must be beyond the unity gain frequency point and a decade is desirable however, sometimes this is not possible if proper noise shaping of the controlled oscillator is desired. The effects of the pole-zero locations and loop gain are easily visualized using a simplified Bode plot, see Figure 4.41. The nominal loop gain is demonstrated

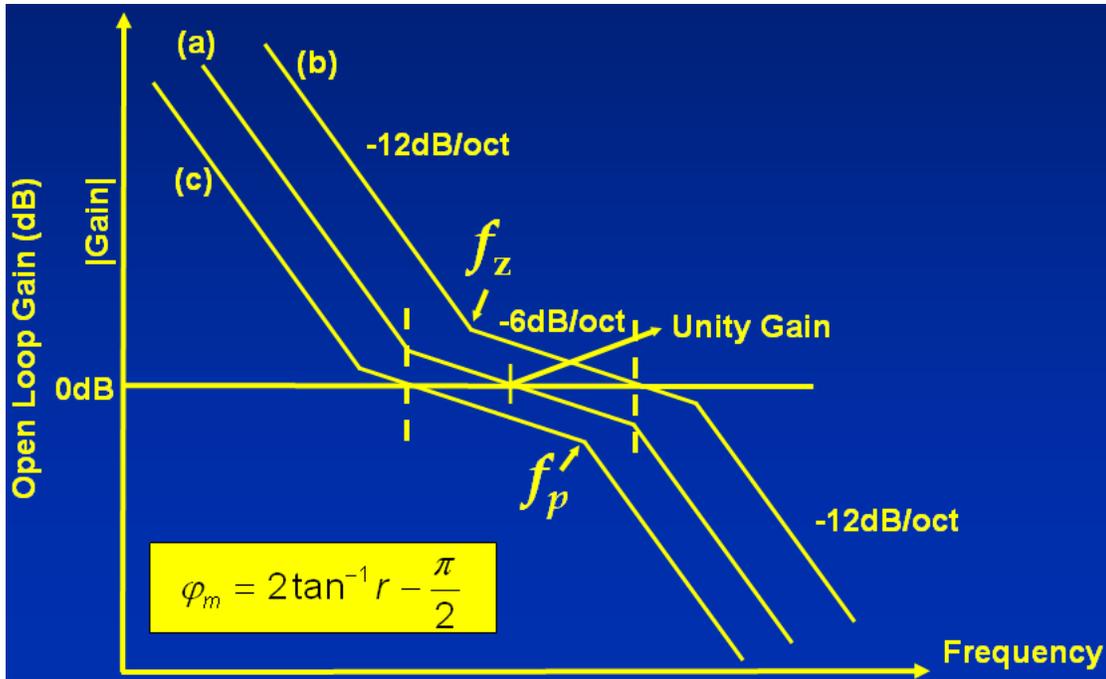


Figure 4.41: The open loop gain Bode plot for a type II PLL system due to the presence two perfect integrators.

in line plot 4.41(a). Clearly, the location of the poles and zeros are appropriate for gain setting in 4.41(a) as the open loop gain crosses zero on a 6 dB/octave slope. The issue which occurs, is that an increase in loop gain, case 4.41(b), or a decrease in loop gain, case 4.41(c), both demonstrate the location of zero crossings close to the 12 dB/octave slope.

A second-order loop with no right half plane poles is conditionally stable. The existence of two poles at DC frequency and permitting the loop to exhibit a -12 dB/octave rate of roll off of loop gain, is readily compensated by the addition of one zero. The degree of phase compensation and the reduction of phase margin with the rise and fall of loop gain is found from the following function given as

$$\varphi_m (K_o) = 2 \tan^{-1} (r) - \frac{\pi}{2} \quad (4.60)$$

where φ_m is the phase margin relative to 180° . Since the loop feedback is intrinsically negative,

180° is already imposed. The ratio of the pole to zero frequency location is given by r . Therefore, the phase margin is bounded between 0° and 90° as $0 \leq r \leq \infty$. An r value of 1.4 or just under 20° phase margin is illustrated in Figure 4.42. For a loop to be reasonably damped, an r value of 3 would be used, providing a phase margin of just over 50°. In general, the open loop phase shift of the phase lock system controls the phase margin. The open loop phase shift of the system portrayed in Figure 4.41, is described by the existence of two DC poles, a single compensation zero, and a third higher frequency pole. Therefore, the open loop phase shift is given by,

$$\phi_{OL}(s) = -\pi + \tan^{-1}(\omega\tau_2) - \tan^{-1}(\omega\tau_1) - \sum_n \tan^{-1}(\omega\tau_n). \quad (4.61)$$

The pole and zero time constants are related to their radian frequency location and are given by τ_1 and τ_2 respectfully. Additional poles are added as required for higher frequency attenuation with time constants τ_n .

The open loop phase shift is a function of frequency, $s = j\omega$. When evaluated at a radian frequency where the open loop gain goes to zero, (4.61), provides the phase margin. Therefore, the phase margin is clearly a function of the number of poles and zeros, and their location and open loop gain.

Peaking follows the two cases represented in Figure 4.41, for case (b), an increase in loop gain, and for 4.41(c), a decrease in loop gain. In either case, excessive peaking will give rise to an increase in phase noise, particularly close the carrier. In addition, the rise in phase noise is predominate at the same time as the loss in loop gain. This rise in phase noise is to be expected, since the noise correction which comes about due to tracking from adequate loop gain is gradually lost. In simulation, the peaking is readily seen with the loss of VCO tuning gain, and is accomplished by the use of a macro-model created in SPICE, see figure 4.42. In this simulation the VCO gain is the swept parameter. As the VCO gain is reduced, the loop bandwidth decreases, and the loop peaking increases.

In Figure 4.43, the open loop single sided phase noise is shown, and since the loop is open, shows no peaking. Detailed phase noise measurements, close to the carrier, are accomplished

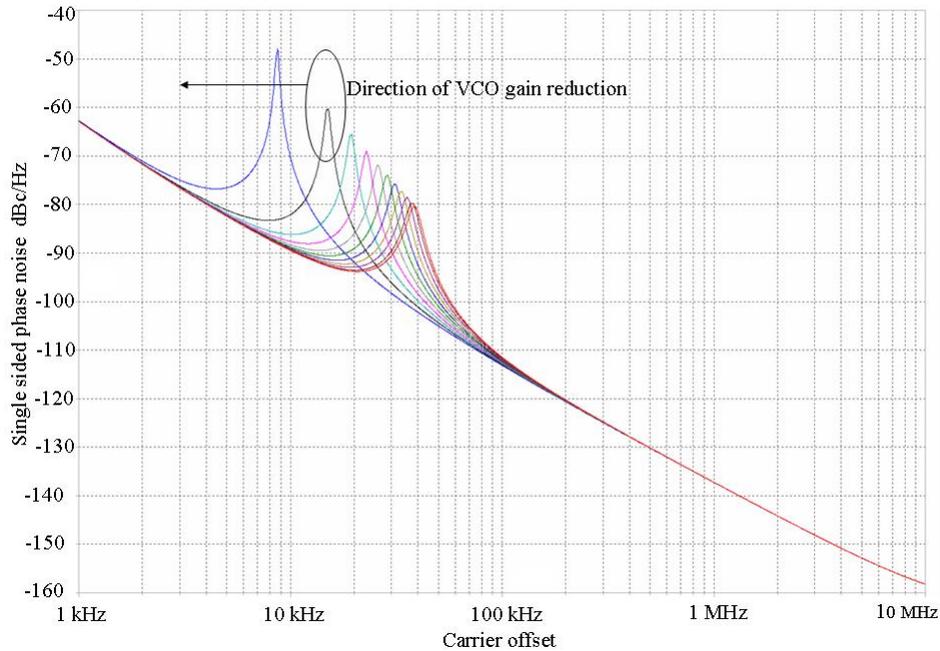


Figure 4.42: Closed loop phase noise simulation with decrease in loop gain. The same VCO open loop phase noise is shown in Figure 4.43. Without peaking the phase noise improvement is approximately 10 dB.

at baseband. The BST oscillator is translated to baseband via a signal analyzer. However, our phase noise measurement are conducted at the carrier frequency instead, as opposed to the baseband equivalent frequency. The main advantage, is the real time rapid sweep of the signal-to-noise peaking which occurs as the loop gain decreases, see Figure 4.45. The agreement with simulation, see Figure 4.42 is quite good and the trend line with loss of loop gain, and the onset of instability is evident; see this illustrated in Figure 4.45(a).

Modulation sidebands are displayed in Figure 4.45 and accompany the BST VCO and are evidence of loop instability although tracking of the BST oscillator to the reference oscillator is still in progress. The spacing of the modulation sidebands, due to the instability of the loop, are closely tied to the natural frequency of the loop, see Figure 4.45(b). The loop, if properly compensated, yields an open loop unity gain crossing frequency closely aligned with the open

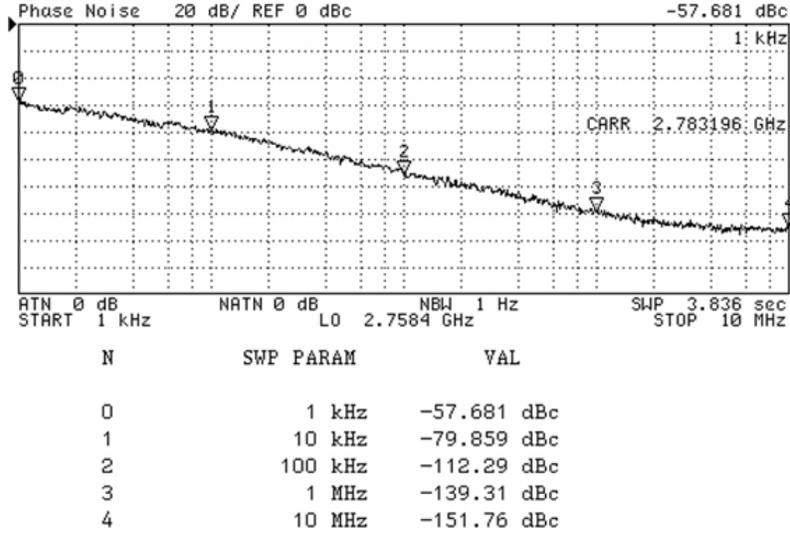


Figure 4.43: BST IDC VCO measured open loop phase noise at 2.7 GHz. Simulation of the same VCO in Figure 4.42 shows good agreement with the measurements with 10 dB of loop corrective gain present. Noise peaking is not seen in an open loop measurement.

loop product of the phase detector gain and the VCO gain, and reduced by the feedback counter value, N . In addition, the frequency response of this system is also dictated by the response of the phase detector. These parameters are readily obtained from the measurements of the VCO tuning gain, see Figure 5.22 and the phase detector response. In the absence of the loop compensator, $F(j\omega) = 1$, the loop bandwidth is obtained from

$$\omega_n = \frac{K_o K_d}{N}. \quad (4.62)$$

If the phase detector is co-sinusoidal or a ring-diode based detector, the frequency response is that of a single pole network, given by,

$$|H(j\omega)_{OL}| = \frac{K_o K_d}{\omega N}. \quad (4.63)$$

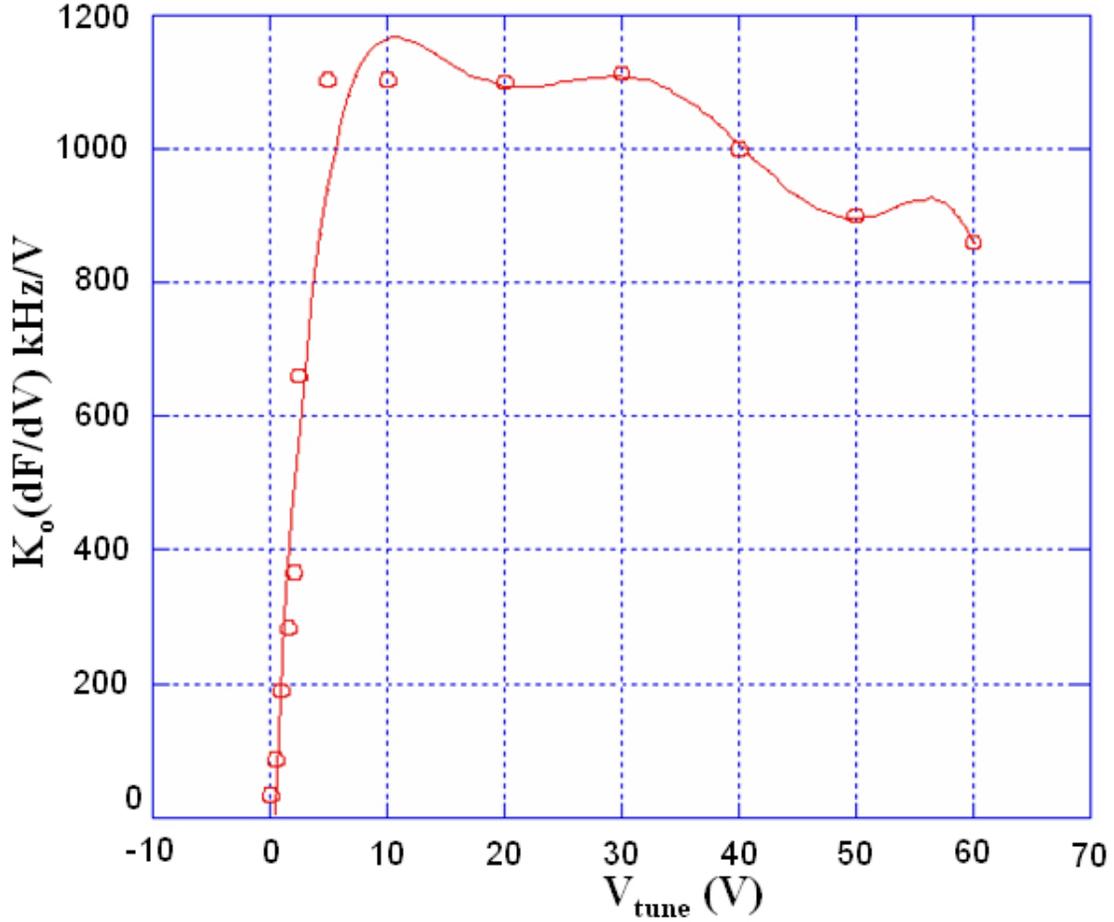


Figure 4.44: The 2.7 GHz BST varactor VCO tuning gain vs. tuning voltage. The slope in tuning gain steeply falls below 10 volts of tuning voltage and approaches zero at zero volts. At tuning values above 10 V, tuning gain approaches a constant of 1 MHz/V.

While the digital implementation tri-state phase detector gives,

$$|H(j\omega)_{OL}| = \frac{K_o K_d}{\omega^2 N}. \quad (4.64)$$

An important observation is the additional pole present and an intrinsic second-order, type II (2-poles located at DC frequency) system with this particular phase detector [103]. Therefore, because of the significant loss of loop gain in the BST based VCO as the tuning voltage approaches zero, it would appear that a second-order type I phase lock tracking loop would

be preferred. A higher order phase lock system could be designed, provided additional pole locations are placed sufficiently high in frequency. Consequently, the resulting open loop response with the BST based VCO would be at a rate of -6 dB/octave up through the unity gain frequency point. This would alleviate the loop peaking and instability [141]. However, the phase lock hang event would not be eliminated.

Higher order phase lock systems such as the type III loop are attractive in frequency discriminator functions. As used in tracking receiver applications, the tracking loop will minimize frequency error and will minimize phase error while tracking an input signal such as a frequency ramp[142]. Since the linearity of the BST varactor based oscillator is quite good, see Section 4.6.5, the ability to provide a low distortion integrated frequency discriminator is compelling. Again, care in exercising a third-order system and a type III loop is required. As reduction in loop gain will force the slope of the open loop gain response to occur on a -18 dB/octave slope, a drop in open loop gain will again lead to an unstable system.

This is a key principal observation for phase locked systems incorporating a BST varactor based VCO. Phase locked systems incorporating a junction varactor based VCO must contend with rising loop gain with decreasing VCO frequency. A fixed reference source frequency requires a decrease in the control counter N as the VCO frequency decreases. Therefore, the increase in VCO tuning gain accompanied by a decrease in N significantly increases the loop gain and the opportunity for control loop instability. However, this is not the case with a BST based VCO. As the control counter N decreases, the VCO frequency again decreases. However, the BST varactor based VCO gain decreases, offsetting the decrease in N . Therefore, a form of self compensation for the loop gain is achieved. Any further decrease in VCO control frequency will inevitably reduce the loop gain further reducing phase margin. Therefore, the compensation zero in a BST varactor based VCO phase lock loop system should be located at a frequency lower than the geometric mean frequency illustrated in Figure 4.41.

From inspection of our measurements, the tuning gain of the BST based VCO is 1 MHz/Volt. The phase detector gain is measured at 0.2 V/radian, and $N = 4$. For the phase lock frequency

multiplier investigated here, a radian frequency of 314 k radians/sec, or a natural loop bandwidth frequency of 50 kHz is found. This agrees well with the measured response and the noise peaking shown in Figure 4.45.

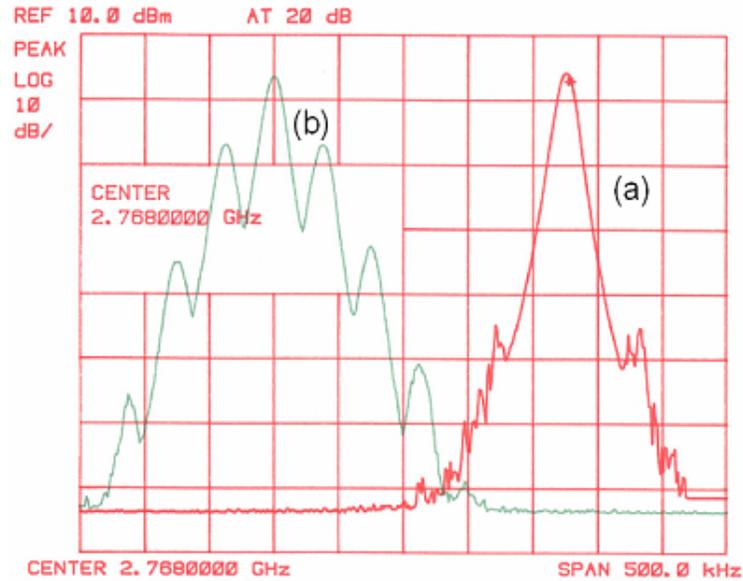


Figure 4.45: Phase locked IDC BST VCO with noise peaking. Tuning gain for case (a) is much greater than for case (b)

Phase lock hang and possible oscillator latch-up occur in a PLL utilizing a BST varactor. The circuit anomalies are avoidable, however, requiring additional circuitry to eliminate the hang event. High voltage charge pumps in the PLL comparator circuit are a requirement and the benefit would be excellent tuning linearity. In the case of the implementation of the power oscillator, the high voltage charge pump could be obtained from the oscillator resonator. Here is a case of bootstrapping, whereby the BST varactor embedded in the VCO, is used to generate its own voltage supply. However, this does require the leakage current of the varactor to be small, otherwise there is the possibility of significant Q reduction. Despite the reduction in tuning gain with the BST based varactor VCO, there is an offsetting advantage for PLL networks utilizing the BST based VCO in synthesizer architectures. As the loop bandwidth

could remain virtually constant if the remaining elements of the loop were to track accordingly. For example, the decrease in operating frequency of a PLL synthesizer, requires a decrease in the feedback counter value, N . This would increase loop gain, however, the reduction in VCO gain, counters the reduction in N . Visa-versa, as the operating frequency increases, again the rise in tuning gain would offset the increase in the counter value. An additional benefit consequently, is maintaining a constant loop phase margin. Although a more complex loop compensator may be used to maintain constant phase margin with variations in N , [143], [144], it is not amenable to integration. In our work, N is held constant, and a 2.7 GHz PLM was implemented as the design and evaluation vehicle. Altering the VCO frequency is accomplished by modifying the reference oscillator frequency.

4.6.2 Phase noise characterization of a BST based oscillator

The principal application of the BST varactor in our work is in power oscillators. We know that maximizing the product of the oscillator output power and the resonator Q is desirable, as this improves the oscillator carrier signal-to-noise ratio. In addition, if resonator unloaded Q , Q_{UL} , is high, then large RF voltage excursions are developed across the resonator in direct proportion to the resonator Q . Finally, if large tuning range is desired, then the varactor may have to be tightly coupled to the resonator. Therefore, there is the potential problem for varactor voltage breakdown and in the introduction of excess noise.

Although low phase noise is not the primary concern in power oscillator design, excessive phase noise is problematic. We need to understand what if any noise limitations are imposed on the designer utilizing BST varactors, as there is likely to be limited available loop gain in the PLM to provide for excessive noise correction.

This section studies the noise performance and the noise characteristics of the BST varactor when applied to tunable oscillators. There are three voltage operating regions that we will focus on which potentially impact oscillator noise. The extremes at zero volts and near the maximum breakdown voltage are two of the regions. The third region is the nominal tuning voltage range

which is below the breakdown voltage and at least a diode junction voltage above zero volts for the junction varactor. The BST varactor is not limited by the zero tuning voltage restriction. However, as previously discussed in Section 4.6.1, the BST varactor limits may be imposed by the specific application. The “near” breakdown voltage will also need qualification, as this voltage is highly dependent on the peak RF voltage developed across the resonator. Both the IDC and the MIM BST varactors are investigated.

Noise measurements of the MIM varactor are conducted by utilizing a comparative measurement technique. Our investigation of noise performance is via comparative analysis with a set of baseline noise measurements. These baseline noise measurements are conducted by utilizing identical oscillators. Phase noise measurements are first conducted with a junction varactor in place of the BST device, and then noise measurements are followed up with the MIM BST varactor. The known parametric relations between oscillator phase noise and the varactor properties are then subsequently used to account for differences in phase noise measurements. This is possible since resonator, active device, and circuit topology are all identical.

The IDC varactor is characterized directly through low frequency baseband spectral analysis. The influence of leakage current is clearly noted in our measurement study. Low frequency noise measurements and application of the oscillator noise model lead to estimates of the influence of BST varactor noise. The model based on the modulation of the tuning line discussed in Section 2.3.7 permits phase noise estimates based on low frequency noise measurements.

The IDC BST varactor configuration demonstrates high voltage breakdown, and measurements as high as 100 V-DC were readily achieved. In order to judge their high voltage capability and study any issues that may arise, active operation near breakdown is required. Sufficient RF voltage is obtained either by providing an impedance transformation of the varactor, or by embedding the varactor in a resonator where the voltage developed is proportional to the network Q . Clearly, this is straightforward in an oscillator operating at lower frequencies since the influence of parasitic capacitance is minimized. Minimizing stray shunt capacitance permits the ability to generate sufficient peak RF voltages with moderately larger inductors with higher

unloaded Q . Thus low frequency oscillators operating under 200 MHz, coupled with sufficient DC tuning voltage permitted studying the BST varactor operation to a high composite voltage. For example, consider a DC tuning value of 100 volts applied to the IDC BST varactor. If the resonator loaded Q is nominally 5, then the potential RF voltage, V_{peak} of Figure 4.46, is available across the varactor at resonance. This peak RF voltage is $Q_L V_{\text{peak}}$, and oscillators constructed at 10 MHz demonstrated greater than 50 volts peak across the resonator. Therefore, when added to the DC tuning voltage, as high as 350 volts peak is available to the BST varactor.

The oscillator circuit topologies chosen permitted the BST varactor, both the IDC and MIM configurations, and a comparable junction varactor to achieve nearly identical tuning characteristics and tuning gain. The BST based varactor oscillator [145] is a Metal-Insulator-Metal (MIM) configuration and the breakdown voltage of this varactor is limited to 10 V. While its break down voltage is lower than the IDC varactor, its capacitance is significantly larger, 200 pF versus under 10 pF for the IDC topology. The capacitance and Q versus tuning voltage of the MIM BST-varactor measured at 50 MHz are shown in Figure 2.17. The varactor versus frequency at a fixed reverse bias of 4 volts is calculated from the measured reactance and resistance versus frequency and is shown in Figure 4.51. The capacitance and unloaded Q were measured on a Hewlett Packard Model 4191A impedance analyzer.

The oscillators incorporated fixed inductive reactive resonators which are identical. The Q_{UL} values are therefore identical since identical resonators were incorporated with identical active device and coupling factor. Therefore, any differences in loaded Q for the resonators are directly linked to varactor unloaded Q , since the same active device and feedback factor are maintained amongst the oscillators studied. The effect of varactor breakdown voltage, and the influence on oscillator phase noise induced by the varactor operating near voltage breakdown. In the case of the BST varactor, we carefully applied DC operating voltage to the tuning line, while continuously monitoring the phase noise. Sustained operation of the BST varactor at breakdown voltage is catastrophic. No recovery of the capacitor is possible. In the case of

the junction varactor, we observe the sum total of the DC operating voltage plus peak RF voltage equal to the breakdown voltage. This is easy to monitor, as there is definitive increase in the tuning line bias current. This is a non destructive event, as long as varactor diode power dissipation is not exceeded during breakdown.

Operating frequencies were significantly less in comparison to the active device f_{τ} . Therefore, active device voltage gain and large resonator Q permitted resonator peak voltages close to 100 volts to be coupled to the varactor. At the same time, the voltage transformation to the active device through the appropriate shifting of impedance levels prevents the active device from breaking down.

Reverse voltage breakdown is one noise factor contributor. The noise mechanism occurring via avalanche current. Excessive forward bias junction voltage is another. In the case of the junction varactor the noise mechanism is due to shot noise of current. A third noise mechanism is $1/f$ and previously reported in semiconducting BST [156]. Although shot noise of current should be absent in the BST varactor, noise characteristics of an oscillator operating near zero volts with the BST varactors are nevertheless of interest, particularly if any changes in leakage current were to occur. Therefore, two main sources of noise are studied. First, shot noise which would occur under a forward biased junction where DC or forward conduction current exists and second, avalanche noise, present in semiconductors operating near voltage breakdown. Note, noise induced by voltage breakdown will occur when the peak value of the RF voltage plus DC varactor bias is at breakdown. Therefore, it is not necessary to apply a DC tuning voltage just equal to the breakdown voltage. If the peak AC resonator voltage plus DC tuning voltage is equal to the breakdown voltage, the onset of oscillator phase noise degradation will be noticed. Adding identical varactors in an anti series stack up increases AC breakdown voltage since the voltage across each varactor is reduced. However, the anti series varactor stacking topology has no effect on the DC breakdown voltage value.

Oscillators are constructed at frequencies covering 10 to 50 MHz, and are confined to low frequencies to simplify measurements and minimize the effects of parasitics. The schematic of

the oscillator is shown in Figure 4.46 where the emitter coupled pair oscillator provides test ports at (A), the resonator, and at location (B), the varactor. The tuning voltage is applied to port (C) through a suitable bias tee from an adjustable low noise power supply. This oscillator provided a tuning range of 30 MHz to 50 MHz. In our work, the central point of the investigation is based on comparative measurements of junction versus BST varactors. A key observation is in time domain measurements of the voltage across the resonator and the voltage coupled to the varactor. Measurements were conducted with a 1 GHz digital storage scope and a 3 GHz GaAs active FET probe through a suitable voltage divider network to protect the active probe from the excessive large RF peak voltage.

The respective tuning characteristics of the junction varactor VCO and the BST based VCO are shown in Figure 4.47. In Section 4.6.7 we discuss further the improved linearity for the tuning characteristic of the BST device as compared to a non-compensated abrupt junction varactor in this same circuit. Tuning characteristics are for the same VCO with only the varactor coupling capacitor altered to obtain nearly the same operating frequency range. Measurements of the resonator, junction, and BST varactor voltages are shown in Figure 4.48, see voltage measurement points (A) and (B). The resonator voltage is nearly 100 volts peak-to-peak as measured at V_A , curve (a), while at zero volts tuning the junction varactor shows significant clamping with a peak voltage of 14 volts, curve (b) at V_B . However, the voltage across the BST varactor is nearly sinusoidal with a peak to peak voltage swing equal to the clamped voltage shown by the junction varactor or, 7 volts peak-to-peak at V_B , see curve (c). The unloaded Q of the resonator is several hundred and the varactor is coupled lightly to the resonator. Coupling is in the neighborhood of a 1:4 capacitance ratio between nominal varactor C and the coupling C to the resonator. Therefore, the resonator voltage remains sinusoidal, as the loaded Q remains sufficiently large to suppress higher frequency harmonics, see Figure 4.48 curve (a).

Oscillator phase noise was briefly discussed in Section 1.3. The phase noise of an oscillator is found to correlate with the frequency noise as the oscillator contains an amplifier-resonator

combination within a feedback loop. The relationship of the noise associated with the resonator, the active device, and their interface was introduced in Section 2.5.1. The resonator noise was restricted to thermal noise due to the finite unloaded Q of the resonator or the associated real resistive loss of the tank. The approach to noise analysis is no different if additional points of noise entry are added to the resonator. Examples of sources of noise are due to the varactor shot noise of current, external noise modulation introduced to the varactor control line, noise introduced into the oscillator supply line, and noise sources of the active device. Ideally, the varactor adds no noise other than thermal, which is directly attributed to Q and dissipative losses.

In our work, additional focus is on the additive noise or excess noise of the BST varactor, and is noise above and beyond thermal, shot, and avalanche noise. This is discussed in Section 4.6.3. If such noise exists, we refer to this noise as excess noise. Both shot and avalanche noise will normally only occur in varactors if the varactor is exposed to non-normal operation. In the case of a junction varactor, the bounds are set as discussed in Section 2.5.2, with $V_o \leq V_T \leq V_B$, where V_T is the tuning voltage, V_o is tuning voltage at zero volts, and V_B is tuning voltage at breakdown. The issue investigated in this work attempts to expand this voltage range in the application of the BST varactor as there is no junction voltage limitation. Therefore, V_o can go to zero. There are unfortunate limits imposed here depending on system implementation and these are discussed in Section 5.1.4. However, both varactors are limited by voltage breakdown and excessive leakage current. In addition, depending on the degree of varactor coupling, avalanche noise will occur prior to setting the tuning voltage to the breakdown point, if the level of peak RF signal plus DC tuning voltage approaches the voltage breakdown point, see Figure 4.53.

Apart from the tuning range, the most important characteristic of a VCO is phase noise. Oscillator phase noise is a single-sided power spectral density of phase fluctuation, and for this work measurements were performed using an Agilent Model 4352S Phase Noise test set. During noise measurements, the circuits were operated on battery and shielded to eliminate extraneous

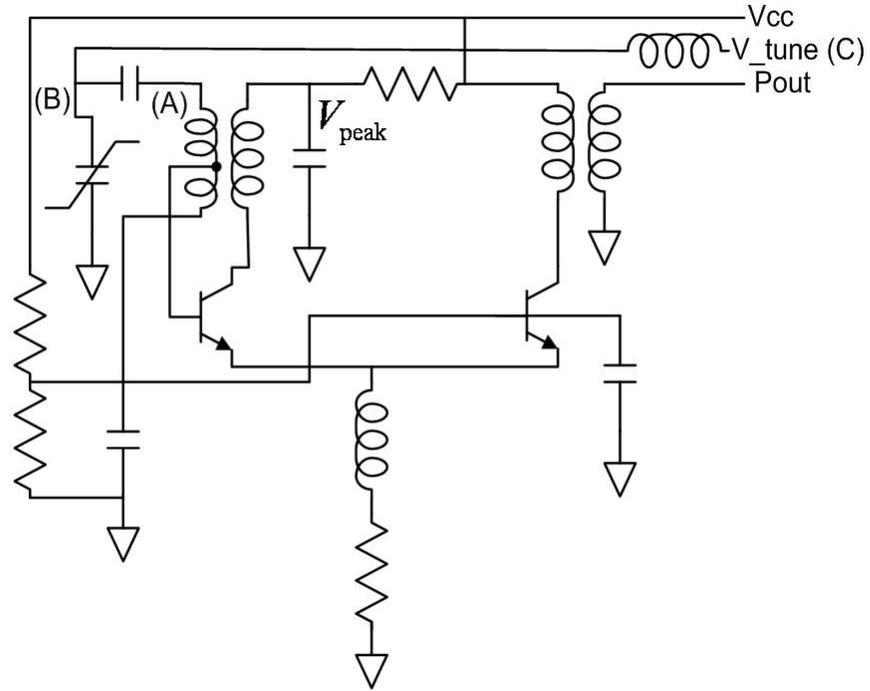


Figure 4.46: Circuit diagram of VCO for varactor test. The emitter coupled pair provides a 2nd stage buffer isolating the oscillator output.

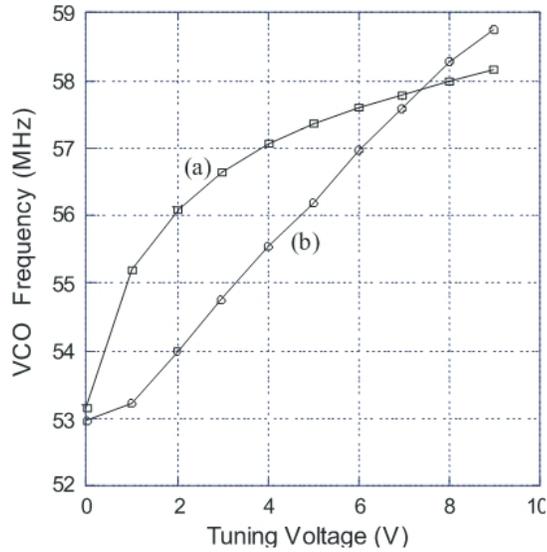


Figure 4.47: VCO tuning curves. The VCO circuit topologies were identical with (a) a junction varactor; and (b) the BST tuning curve.

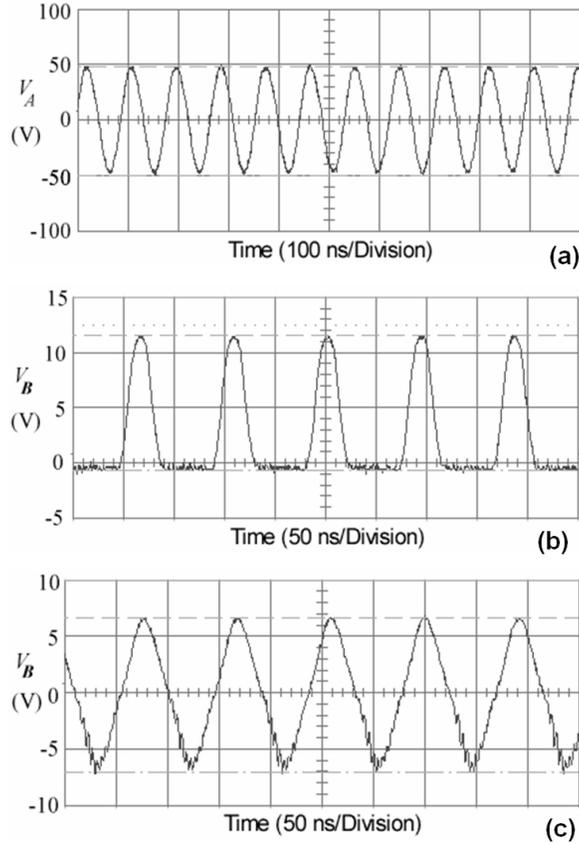


Figure 4.48: Resonator voltage measurements of Figure 4.46: (a) at point (A); (b) at point (B) for the junction varactor; while (c) at point (B) for the BST varactor.

sources of noise. Single-sided phase noise measurements were taken at offset frequencies of 100 Hz to 1 MHz, while spot noise measurements were taken at 1 and 10 kHz. The single-sided noise power spectra of the oscillators were measured against their respective tuning voltage, particularly in three regions of interest; at zero volt bias, normal mode at mid-point bias, and near varactor voltage breakdown. As an example, shown in Figure 4.49, is the junction-varactor VCO operating in normal mode or at mid-tuning voltage range, at 0 V bias, and near reverse breakdown.

The phase noise of the junction varactor based VCO is shown in Figure 4.49. Under similar operating conditions, the phase noise of the BST varactor based VCO is shown in Figure 4.50.

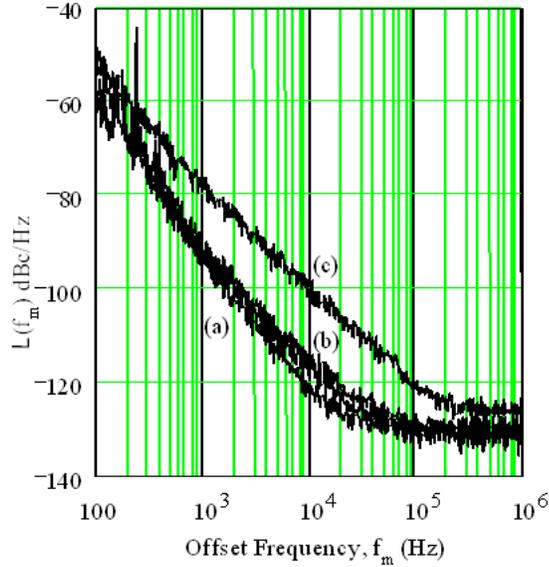


Figure 4.49: Measured single-sided phase noise of the VCO with the **junction** varactor against tuning voltage at: (a) 6 V; (b) 0 V; (c) 18 V

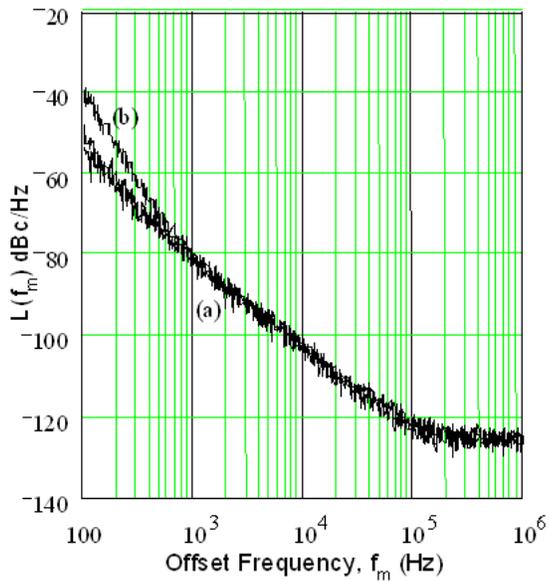


Figure 4.50: Single-sided phase noise **BST** varactor based VCO versus tuning voltage at: (a) 0 V and 3V overlap; (b) 6 V

The phase noise responses of the two VCO's have different characteristics. These differences are noted and interpreted in terms of the variation of the noise slopes, and degree of excess

shot noise. Some of these differences might be expected as the degree in varactor and oscillator tuning linearity are significantly distinct. We will focus on the overall noise characteristics and then we will address the phase noise slopes in detail.

In Figure 4.49, the phase noise of the junction VCO is seen to be a strong function of tuning voltage. Curve (c) corresponds to operating the varactor near reverse breakdown voltage, where excess avalanche noise leads to significantly higher phase noise. At 0 V bias, curve (b) of Figure 4.49, the excess shot noise of current comes about with forward diode conduction, and is seen to increase the phase noise. In contrast, excess phase noise at 0 V bias is not seen with the BST-based VCO, see Figure 4.50 curve (a), since there is no junction and therefore, no forward conduction of current. It is observed, for this particular oscillator circuit, that phase noise degradation occurs at a tuning voltage of less than 1 V for the semiconductor junction varactor-based VCO. This phase noise degradation, is attributed to the RF voltage across the varactor, adding to the DC tuning voltage, and resulting in forward bias conduction during a portion of the RF cycle. The net resultant phase noise degradation is two-fold. One, forward conduction of the varactor causes resonator Q reduction and two, shot noise of current occurs.

Note, that the oscillator topology which was chosen in Figure 4.46, is in part because a much larger voltage swing of 90 V peak-to-peak is developed across the resonator, and not totally across the varactors, see Figure 4.48. The oscillator phase noise in the mid range tuning voltage region, is partially dependent on resonator Q , and the oscillator phase noise variations should match the varactor loss trends discussed in Figure 2.17 and Figure 4.51.

In the region where tuning voltage is bounded and shot and avalanche noise are avoided, the single sided phase noise, $L(f)$, predicts an oscillator phase noise, proportional to $(\omega_o/2Q)^2$ [36]. Therefore, we would expect to see an accountable difference in operating phase noise between the junction varactor based oscillator and the BST MIM based oscillator due to differences in the varactor unloaded Q . In Figure 4.52, we see this is the predicted trend. For the BST-based VCO, the correlation of the oscillator noise with ΔQ is very good for tuning voltages between 1 and 6 volts. In particular, the agreement between measured and predicted changes in phase noise

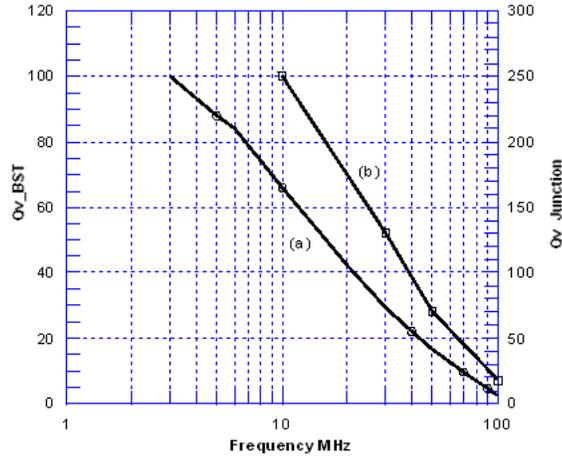


Figure 4.51: Calculated Q as a function of frequency: (a) BST varactor; (b) junction varactor

based on measured differences in the Q values alone are within 2 dB over this range, see Figure 4.52 (a). Significant departure in agreement occurs above 6 V as the BST MIM breakdown voltage of 10 volts is approached. Above 6 V tuning voltage, the phase noise increases rapidly as the BST breakdown voltage is approached, curve (b) in Figure 4.52. Rapidly increased phase noise is seen in Figure 4.53, curve (a) for the junction varactor-based VCO. It is important to note, in Figure 4.53, the rapid rise in phase noise which occurred well in advance of reaching actual reverse voltage breakdown of the junction varactor. In this particular oscillator, coupling of the varactors into the resonator is not tight. However, the resonator loaded Q is sufficiently large enough to support a significant peak AC RF voltage. Therefore, the increase in varactor unloaded Q with the increasing reverse tuning voltage, gives rise to a higher loaded Q resonator and a larger peak RF voltage. The sum total of DC and RF voltage was more than sufficient to force junction varactor voltage breakdown. In addition, forward-bias conduction in the junction varactor also contributes to phase noise degradation. We see this next in Figure 4.52, as there is a departure in predicted versus measured phase noise based only on the difference in varactor Q . In this case, the departure occurs due to the forward biased junction and the increase of shot noise of current. Hence, Figure 4.52, provides the tie between the measurements of the junction varactor based oscillator and the BST MIM varactor based oscillator. The respective

oscillators unloaded Q resonator differences are contingent on the unloaded varactor Q . The differences in the varactor unloaded Q values are shown in Figure 4.51 and collaborate well with the variation in the measured phase noise.

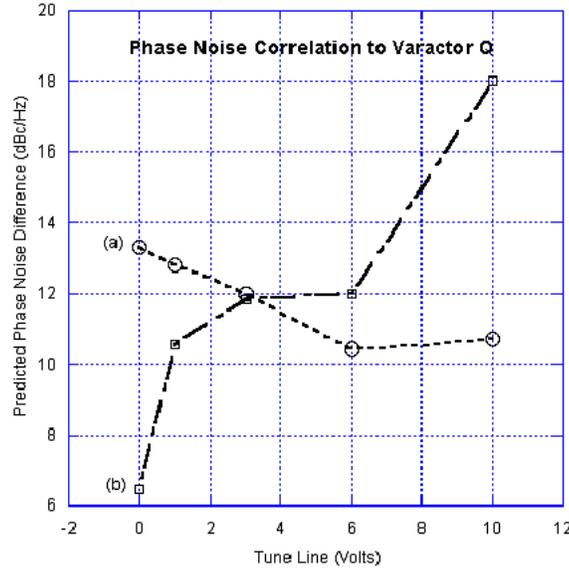


Figure 4.52: Relative phase noise against tuning voltage for the BST varactor based VCO: (a) predicted from oscillator phase noise model; (b) measured.

This is seen by contrasting curves (a) and (b) in Figure 4.50. The phase noise at 6 V bias, curve (a), corresponds to the no conduction condition, however curve (b), the phase noise at 0 V bias, has excess noise resulting from shot noise of current. The corresponding results for the BST varactor, the superimposed curves in (a) of Figure 4.49, show no difference between the zero-bias voltage condition and the moderately-biased, 3-V condition. The above discussions are supported by the measured resonator and varactor voltages obtained using high impedance probes. The resonator voltages for both the BST and junction varactor-based VCOs were 90 V peak-to-peak. The voltages are identical as circuit conditions were adjusted to achieve this operation. The voltage across the junction varactor is clearly limited by forward conduction to approximately 0.7 V. There is significant harmonic content at this tuning voltage. The

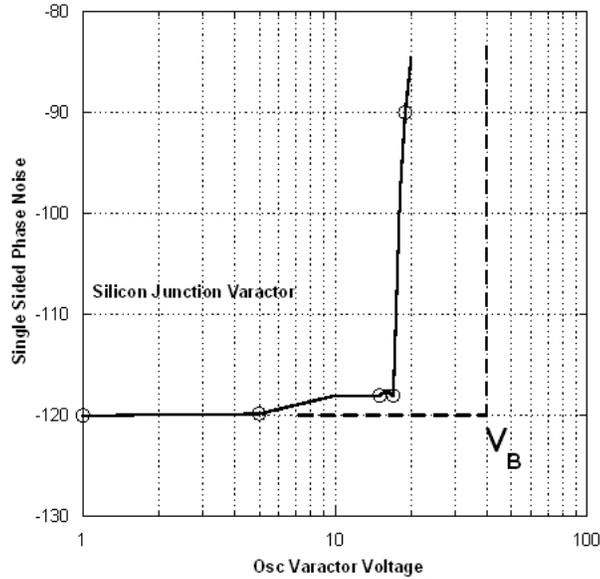


Figure 4.53: The measured junction varactor phase noise degradation versus tuning voltage, see Figure 4.46 point (C). The junction varactor breakdown voltage, V_B , at point (B) is also indicated on the graph for comparison.

voltage across the BST varactor, at 0 V bias, demonstrates less harmonic content. Spectrum analysis of the VCO output also demonstrates that the harmonic content of the BST-based voltage controlled oscillator to be much less than that with the junction varactor [145], for this specific oscillator topology, and degree of varactor coupling. The phase noise plots of Figures 4.50 and 4.49 describe the oscillator condition at 0 V, in the mid tuning range, and near breakdown. There is no excess shot noise from forward conduction of current or reverse breakdown avalanche noise in the mid tuning range. This is seen in curve (a) in Figure 4.50 for the junction varactor-based VCO, and curve (a) in Figure 4.49 for the BST varactor-based VCO.

The oscillator single sided spectral phase noise is described by a family of distinct break or corner frequencies. Indeed, the phase noise slope with respect to frequency tracks that expected of a low loaded Q oscillator, as the phase noise is Q dependent. The classic theory for a low Q resonator is that close to the carrier frequency, flicker noise dominates and the phase noise will

have a slope of -30 dB/decade, i.e. a $1/f_m^3$ dependence. At a second oscillator corner frequency, the slope changes to -20 dB/decade, i.e. there is a $1/f_m^2$ dependence. Eventually at frequencies further from the carrier the noise floor dominates [37]. These characteristics are seen for both VCO types. Slopes drawn for both VCO's biased in the mid tuning voltage region demonstrate a corner frequency where the slope of phase noise shifts from -30 dB/decade to -20 dB/decade, and this is approximately at 1 kHz. When shot noise becomes significant, the characteristic changes.

First consider the junction varactor-based VCO. At 0 V tuning the sum of the DC voltage and the RF peak voltage will lead to forward conduction, at least for part of the RF cycle. This results in excess phase noise as seen in curve (b) of Figure 4.50. As reverse breakdown is approached, avalanche noise dominates, see curve (c) in Figure 4.50. The slope of the phase noise above the noise floor is -20 dB/decade over the whole range, and flicker noise is not evident. With the BST varactor-based VCO, the phase noise at 0 V bias is identical to that in the mid tuning range, curve (a) in Figure 4.49, as there is no shot noise of current at maximum capacitance. However, there is an increase in noise at high bias when the BST-varactor enters the avalanche regime during part of the RF voltage swing. Curiously, the slope of the phase noise is -40 dB/decade, i.e. a $1/f_m$ dependence close to the carrier. Such a slope is encountered with a phase noise process associated with a random walk of frequency [38], [39]. Therefore, this regime could be partially due to self heating in the dielectric as leakage current is also seen to increase. This self heating and increased leakage current, lead to frequency drift as the effective capacitance is altered. In addition, since random walk in frequency is usually correlated with increased flicker noise, it is suspected that this noise would have its origin in variation of processes and material migration in the BST film. This should be a topic for future work.

Two Voltage Controlled Oscillators (VCOs) based on the junction varactor semiconductor and BST varactors were contrasted. The development of design formulas for the oscillator tuning range enabled near optimum and closely matched VCO's to be designed leading to a fair

comparison of the two technologies. This work showed that a VCO utilizing a BST varactor is viable with interesting phase noise characteristics. In particular, the absence of excess shot noise at maximum tuning capacitance, since there is no forward conduction, makes it a particularly attractive component. The early onset of avalanche noise is noted in the junction varactor, and to a similar degree excess noise in the BST varactor. It was not necessary to apply DC tuning voltages beyond 6 volts in the case of the BST varactor, as the peak RF voltage plus DC tuning voltage already approach the breakdown voltage.

4.6.3 Excess varactor noise

This section emphasizes the possibility of excess noise in the BST varactor. The predominate factor would appear to be leakage current and this is studied in some detail through direct noise measurements of the varactor. Instrumentation is developed for this work and is highlighted in the Appendix B section. In addition, indirect noise measurement investigation is conducted through oscillator phase noise measurements and several conclusions are drawn.

In the discussion of noise factor, see Section 7.2, the variable F was defined as $F \equiv$ input SNR/output SNR where the signal-to-noise is conventionally defined as the ratio of the signal power to the noise power. We noted noise measurements are independent of the signal level, provided the input signal level is small relative to the DC quiescent conditions. The measurement of the output noise power is within a bandwidth B_s , there is no signal applied to the input, and the input is terminated in a specified source impedance. The excess noise figure is interpreted as the output noise power within the bandwidth B_s , divided by the gain, and normalized to the thermal noise power kT_oB_s at standard room temperature. The excess noise factor is then defined as

$$F - 1 = \frac{\text{device noise power added}}{GkT_oB_s} . \quad (4.65)$$

Therefore, the excess noise of the amplifier is above and beyond what the source would contribute had the amplifier been perfect and noise free. Furthermore, for small signal conditions, the noise figure is assumed to be independent of the input signal level. Under certain operating

conditions, this was shown not to be true, and the increased noise power due to large signal, that is large in the context of the DC quiescent operating point, leads to excess noise due to avalanche multiplication or a rise in shot noise due to excessive junction current. So, a further definition of excess noise may be noise power which is in excess of that obtained from small signal operating conditions. That is, noise present in addition to the thermal and background noise. The excess noise typically found, follows a $1/f^\alpha$ characteristic [38]. Noise processes that are $1/f^\alpha$ in voltage noise spectra, as well as generation-recombination noise and noisy leakage current are identified [152]. In GaAs oscillators, the use of hyper abrupt or super hyperabrupt GaAs varactors are incorporated and significantly high tuning gains are possible; several hundred MHz/volt. When compared to Silicon or BST varactors, the excess contributions of noise such as $1/f$ (flicker) is significant, as the modulation through the tuning line port occurs. In the case of the varactor, the ideal varactor would be noise free and contribute no additional noise as the device is operating with a reverse bias voltage and zero device current. This is usually the case and as cited in [152], the up conversion of noise seen in the oscillator is mostly due to the active device alone and not a combination of the varactor and active device. This leads to a simplified explanation to the noise conversion process. The varactor noise, if of sufficient spectral content, needs only to modulate the tuning line of the oscillator. If the tuning gain of the oscillator is very large, then the noise modulation, which is a baseband noise spectra, is up-converted in the FM process, see Section 2.3.7 and Figure 2.7. If the tuning range is small, the noise voltage and the consequential phase noise contributed by the varactor is not noticed. So, in the context of oscillator phase noise, we may interpret the definition of excess noise contributed by the varactor as a spectral noise degradation that cannot be traced to noise associated with just the Q degradation of the resonator, or shot noise of current due to a forward biased diode junction or avalanche noise associated with device voltage breakdown.

Not unlike BST, tantalum capacitors, (Ta-Ta₂O₅-MnO₂) demonstrate excess noise due to self heating. Self heating effects demonstrate time dependent noise values and the result of stochastic processes as charge carrier trapping, free charge carrier avalanche, thermal instabil-

ities in microbreaks, and isolation layer thickness variations occur. These noise processes in the low frequency range, may be considered a superposition of flicker, burst, shot, and thermal noise. In addition, fluctuation of polarization and fluctuation of mechanical strain may cause other kinds of noise. Finally, there is a contact resistance noise component, see [155]. In BST material, type BaSrTiO₃, reports in [156] and [157] point to excess noise in the material inversely proportional to the volume of the material and directly proportional to the bias current. Further follow up research, provided for a physical model for the excess noise, and relates the cause to high-resistance fluctuations between the semiconducting grains of BST within a given volume of material. Around each grain of BST, a depletion layer develops because of the presence of surface states.

Resistors are also known to produce excess noise. In this case, noise that is more than the noise voltage attributable solely to temperature. The excess noise arises as a function of DC bias, frequency, due to the shunting effect of the resistor body capacitance, wattage rating and material composition. The excess noise again has a $1/f$ frequency spectrum and is specified by a noise index, NI and is given by,

$$E^2_{\text{excess}} = \frac{10^{NI} 10^{-12} V_{dc}^2}{\ln 10} \frac{1}{f} \quad \text{V}^2/\text{Hz}. \quad (4.66)$$

Consider the case of excessive BST leakage current. We find that a direct correlation exists between the leakage current and the unloaded Q of the varactor, as well an increase in the noise voltage available from the varactor. Without monitoring the leakage current of the diode, we might speculate that high spectral phase noise power for an oscillator with a high leakage varactor is due only to the low Q of the varactor. However, measurements demonstrated excess noise in both the MIM and the IDC BST units where high leakage current is present.

Measurements are conducted with a narrow band spectral analyzer, an HP4195A. A slow sweep is used with a narrow resolution bandwidth, 10 Hz or less, and equipped with a low noise audio instrumentation preamplifier. In addition, lower frequency and higher sensitivity audio spectrum analyzers and wave analyzers, type, HP3581A are also used. Noise equivalent

voltage measurements better than $0.5\text{nV}/\sqrt{\text{Hz}}$ or less than -180 dBV , dB below 1 V referenced in a 600 ohm system impedance, are possible for this system measurement. Validation of the measured values are accomplished by a substitution method. In the substitution method, the device under test is replaced by either a noise generator or signal generator of known output power level or voltage amplitude level which matches the rms noise levels measured. The preamplifier spectrum analyzer are cascaded with an adjustable step attenuator matched in an audio baseband system impedance of 600 ohms, and a variable attenuation pad setting is used to avoid amplifier saturation if a large discrete signal is present. All measurements are conducted in a screen room. The low noise audio preamplifier had a power gain of 67 dB and a bandwidth of 100 kHz. It is preceded by a 1 MHz low pass LC input filter and a 70 dB stepped pad, so the net power gain of the amplifier, filter, pad combination is adjustable to 50 dB. If no spectrum analyzer overload condition is noted, the attenuator is set to zero. This cascaded system is input to the low noise spectrum analyzers via a switched attenuator, permitting checking the noise sensitivity level and voltage gain of the system. The noise equivalent bandwidth and the analyzer detector characteristics must be considered, and corrected for proper noise measurement levels. Initial measurements of Silicon, Schottky, Zener, and varactor diodes, provided a check on the test set operation. Known prescribed DC operating current and voltages applied to various diode structures permitted pretesting of the test set as discussed in references [152, 153, 154].

The BST MIM varactors that were the basis of the prior oscillators studied earlier, operated at low RF frequencies, less than 200 MHz, and were investigated for excess noise voltage. Not all BST MIM varactors demonstrated high levels of leakage current. We see this must be the case, otherwise the power spectrum of phase noise reported earlier would have reflected a significantly higher level of phase noise. For example, consider the tuning gain of these oscillators, from Figure 4.47, the tuning gain is 375 kHz/V. At an offset frequency of 10 kHz, the single sided measured phase noise is -106 dBc/Hz . To degrade this phase noise value just 3 dB, the noise voltage would need to be greater than $188\text{nV}\sqrt{\text{Hz}}$. Thus, representing a larger

noise voltage and therefore, a large leakage current than previously reported. As is evident in our next discussion, based on the correlation of noise voltage and leakage current, we see these specific varactors were not present in the oscillators studied earlier. Important to emphasize, these phase noise degradation calculations are based on a specific tuning gain, (K_o), and offset frequency. Therefore, the magnitude of these values would change accordingly.

Leakage current and noise voltage of the BST MIM capacitor is measured as a function of applied bias voltage. A bias tee is used to apply a voltage provided by an adjustable NiCd power pack which is subsequently filtered via a 1000 uF electrolytic capacitor. The BST varactors which were not tested and had no prior applied voltage are examined. Observed is an apparent soakage trait, whereby both the leakage current and associated noise voltage are initially large however, subsequently drop significantly over time. As the applied bias voltage is increased, a similar effect is noticed. Permitting the varactor to soak at a specific voltage, and then returning to that voltage, finds a newer lower leakage current and lower noise value as compared to the initial measurements. This effect is plotted via the spectrum analyzer output to a pen recorder, and is conducted over an approximate 1 hour time period as the measurement bandwidth is small, 1 to 10 Hz, see Figure 4.54.

In curve Figure 4.54 (a), the noise voltage is much less than $2 \text{ nV}/\sqrt{\text{Hz}}$ out to a frequency of 100 Hz. The preamplifier gain during these measurements is 50 dB. At higher offset frequencies, oscillator phase noise would not be effected by upconverted excess noise associated with the BST varactor. This is particularly true at large carrier offsets and with lower tuning gain. However, inspection of Figure 4.54 (b) shows a different issue. This curve demonstrates a condition of higher leakage current, where no prior soakage of the BST varactor was provided. Significantly higher noise is noted, $\sim 800 \text{ nV}/\sqrt{\text{Hz}}$ at the same frequency offset as in (a), at this new higher bias voltage.

Consider a higher offset frequency but close to the carrier at 100 Hz. Curve (b) indicates a noise voltage of $32 \text{ nV}/\sqrt{\text{Hz}}$ after correcting for preamplifier gain and attenuation. If this noise voltage level were present in the oscillators measured at the onset, and dominated the

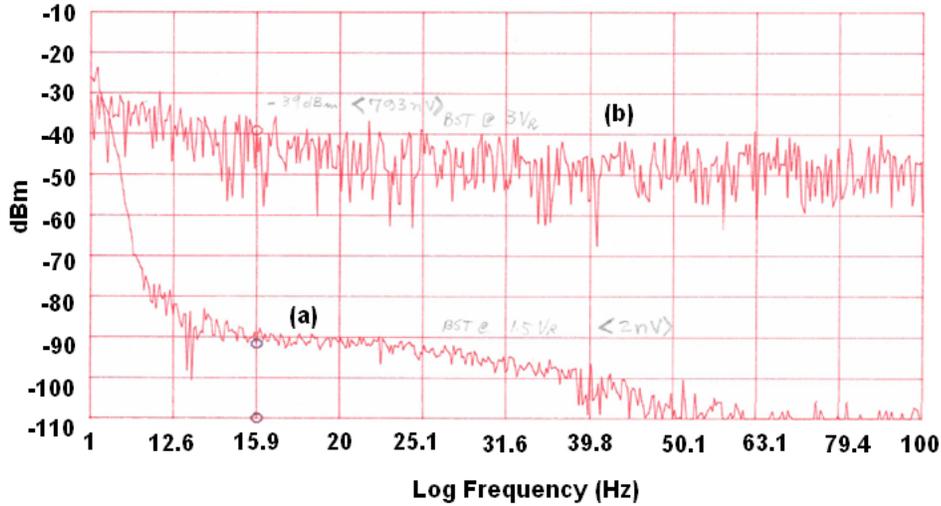


Figure 4.54: BST MIM noise voltage vs. log frequency sweep: (a) after initial bias soakage at 1.5 V of greater than 1 hr; (b) stepping to a new higher bias voltage of 3 V no significant soakage time accrued.

noise contribution, single sided phase noise would have been -78 dBc/Hz versus -58 dBc/Hz at 100 Hz offset. Although this is not the case, there is evidence from this calculation that close to the carrier phase noise could be limited by varactor excess noise if larger tuning gain existed. The noise shape unlike Figure 4.54(a), is quite flat and although roll off of noise voltage spectrum eventually occurs, this level of excess noise would degrade sideband phase noise to a much greater extent in oscillators with a larger tuning gain. The leakage current magnitudes that lead to this higher level of excess noise are shown in Figure 4.55 and in addition the Q_v for the same varactor under test is shown, Figure 4.56. Since the leakage current to a first-order is modeled as a shunt R_p with the dielectric loss, the varactor Q will decrease as leakage current increases.

4.6.4 Conclusions on excess noise in BST varactor

Excess noise in metal-insulated-metal (MIM) and interdigitated or IDC BST varactors exists and is traceable to the first-order to leakage current. Oscillators which maintain low K_o reduce the likelihood of phase noise degradation occurring due to varactor excess noise. However,

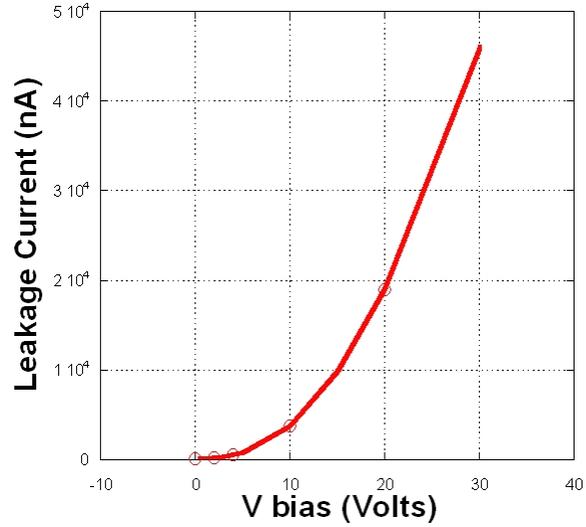


Figure 4.55: Measured BST MIM varactor leakage current versus applied bias voltage.

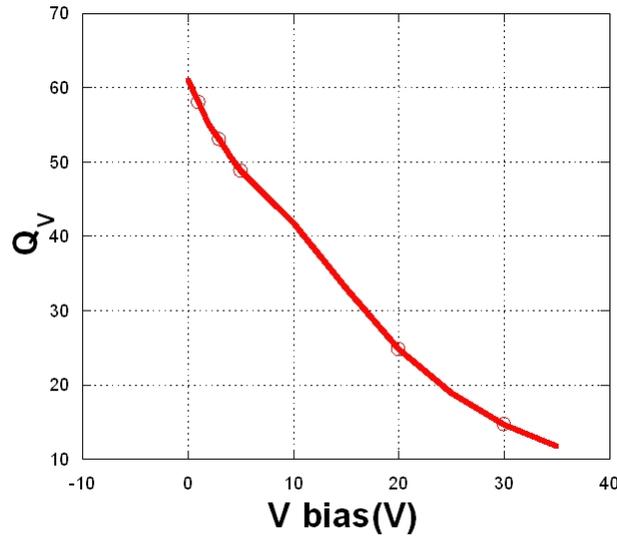


Figure 4.56: Measured BST MIM varactor Q_v vs. applied bias voltage for the associated varactor of Figure 4.55.

if varactor coupling is increased or the resonator RF voltage swing plus DC voltage is large, then phase noise degradation is likely. As demonstrated in Figure 4.49, phase noise increased significantly at higher tuning voltages and is in accordance with increasing leakage currents. The excess noise noted, was directly linked with increasing leakage current of the varactor.

Low frequency DC leakage current measurements were not conducted under the additional condition of RF excitation being present. However, had this been the case, it is suspected that the correlation between the baseband excess noise measurement of the BST varactor and the RF phase noise measurement illustrated in Figure 4.49, would have been aligned. Similar measurements should be conducted on the IDC varactor and is left for future work.

4.6.5 BST Oscillator tuning gain, linearity and stability

A tunable oscillator is either current driven, by altering the magnetic field or flux of an inductive element, or voltage tuned by altering the electrostatic field or voltage of a capacitive element. Magnetic tuning provides lower noise power, and the carrier signal-to-noise ratio, (C/N_o) , is significantly better due to the higher unloaded Q . However, the focus of this work is capacitive tuning as the size, power consumption, and tuning speed is superior. In this section we review the background work for modeling and verification of BST varactor tuning frequency characteristics and the tuning gain. We investigate the MIM and IDC geometry and note the inability of accurate modeling if leakage current is prevalent and is not accounted for in the modeling process.

Oscillator tunability and frequency agility are major design points in applications of controlled oscillators. Tunability assesses the oscillator to be free of frequency jumps and discontinuities in both power and frequency, while agility refers to the operating bandwidth of the source. Coupled with these elements is a linearity measure of frequency versus the VCO tuning control signal. The oscillator tuning gain or K_o is a measure of the oscillator frequency change with respect to a change in voltage. The tuning linearity is defined as the deviation of the gain slope from best straight line fit (BSL). Dependent on the oscillator application, the tuning profile may require a specific shape for purpose of compensation. However, in many applications good tuning linearity and control of the tuning slope with frequency is desirable, for example, low distortion frequency modulation and de-modulation, in a phase lock loop (PLL) maintaining constant loop bandwidth and CW radar [127]. Although YIG-tuned oscillators have excellent linearity as well as wide tuning range, they also have low tuning speed restricting their usefulness. Varactor tuned oscillators or VCO's feature high speed tuning although their intrinsic linearity is inferior to YIG based sources. Hence considerable work investigating circuits, techniques, and devices to accomplish oscillator tuning linearization exists [128, 129, 135]. In this section, we characterize oscillator tuning gain and linearity with emphasis on the control element, a barium strontium titanate (BST) varactor [130]. Both MIM (metal-insulate-metal)

and IDC (inter-digital capacitor) varactors are investigated. The test vehicles are low frequency FET and insulated gate FET oscillators which assure high open loop gain and accurate device measurements without the burden of significant parasitic effects. Using a field dependent model [136], in conjunction with a polynomial fitting function, we characterize the frequency, tuning gain, and linearity of two VCO's. The MIM varactor based oscillator with an E-field derived C-V model from [136] permitted an accuracy within 2% of measurements for frequency characteristic and tuning gain. The IDC based varactor VCO required both the E-field and polynomial fitting function to the C-V curve. However, the resulting agreement with measurements is excellent, less than 1% error in assessing frequency, tuning gain, and linearity. In addition, the IDC linearity or fit to best straight line is less than 4%, and intrinsic to the varactor device. In a large portion of the tuning range, we measured and predicted linearity better than 0.5% without the use of reactance correction networks. This is an important note, as the linearity provided in the oscillator, and more important the control function of frequency slope with tuning frequency, is well behaved. This is intrinsic to the BST varactor without the complication of linearizing circuits. To investigate this further, we considered the junction varactor firstly and the prior work in providing tuning slope compensation.

4.6.6 Definition of tuning linearity and tuning gain

The voltage controlled oscillator is a voltage to frequency converter. In the context of the phase lock multiplier (PLM) architecture discussed in Chapter 1, it is also a voltage controlled integrator. In the treatment of both applications, the relationship between the frequency or the phase of the oscillator with respect to the control voltage is characterized for at least three parameters, tuning gain, tuning linearity, and tunability. Tuning gain and tunability are somewhat interchangeable terms since in effect a high tuning gain is associated with a wide tuning range for a small change in input voltage. This tuning must be continuous with no jumps or discontinuity in output power or frequency. So the word tunability is better described by the terms tuning and stability. In addition, the tuning profile should display

no hysteresis, positioning the oscillator frequency at the same frequency with respect to the periodic application of identical and repetitive tuning voltage and void of memory effects or post tuning drift[40]. All of these items taken together would imply “good” oscillator stability. A fundamental difference though in our treatment of K_o in this section, is the tuning gain must be found for a small change in incremental tuning voltage, V_T . Hence, the oscillator tuning gain is better expressed here as an incremental or small deviation K_o , in order to differentiate that requirement. Then K_o is defined as,

$$K_o \equiv \Delta f / \Delta V_T \quad (\text{Hz/volt-sec}) . \quad (4.67)$$

An equivalent form in terms of radian frequency is

$$K_o \equiv \Delta \omega / \Delta V_T \quad (\text{radians/volt-sec}) \quad (4.68)$$

and the conversion simply requires the relation $1\text{Hz} = 2\pi$ radians . Hence, the tuning gain is the derivative of the tuning characteristic curve. If the oscillator displays linear frequency change with tuning voltage, then K_o , tuning gain, is constant with a slope equal to the gain. A signal analyzer provides both measurements as displayed in Figure 4.57. Tuning linearity is obtained from an incremental derivative of the tuning gain. The ΔV steps must be small as the frequency difference is evaluated. Otherwise, frequency discontinuities, deviations from monotonicity, and tuning hysteresis are missed. The result of these aberrations, is misbehavior in the phase lock system leading to increased noise, peaking, and loop instability. As a rule, incremental frequency differences of less than 2% of the fundamental oscillator frequency are desired. So at 1 GHz, incremental derivative evaluation of K_o would occur every 10-15 MHz, less is desirable. This definition suffices from a test and measurement perspective. From a circuit analysis perspective we find the tuning linearity by the evaluation of two derivatives. First, we require the change in operating frequency with variable capacitance, C_V only, and

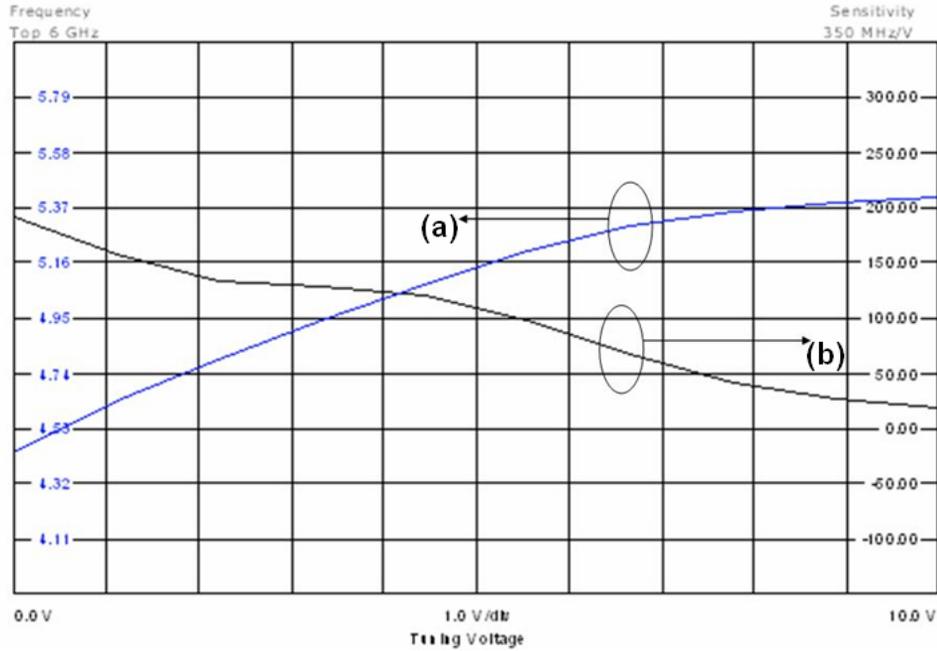


Figure 4.57: VCO frequency characteristic curves: (a) Tuning curve; (b) tuning gain or K_o .

then the change in the capacitance with voltage. In terms of radian frequency this is

$$K_o = \frac{\partial \omega}{\partial V_T} = \frac{\partial \omega}{\partial C_v} \frac{\partial C_v}{\partial V_T}. \quad (4.69)$$

In determination of the oscillator operating frequency, we will use small signal sinusoidal analysis and apply a small incremental change in tuning voltage, V_T . We reserve C_v as the varactor capacitance and note that $C_v(V_T)$ is a dependent variable.

The semiconductor junction varactor displays a C-V relation given by

$$C_V \propto (V_R + \varphi_{bi})^{-\gamma}. \quad (4.70)$$

Here V_R is the reverse bias tuning voltage, or V_T , and φ_{bi} is the built-in diode junction potential. The reverse bias voltage is a negative quantity and the capacitance is bound between a maximum value at 0 volt reverse bias and the breakdown voltage at $-V_{BV}$ as discussed in Chap-

ter 2. Including the bounds of reverse bias voltage then, the semiconductor junction varactor capacitance $C_V(V_T)$ relationship is given by

$$C_V(V_T) = C_{\min} \left(\frac{\varphi + V_T}{\varphi + V_{BV}} \right)^{-\gamma}. \quad (4.71)$$

For the purpose of AC circuit analysis, we will describe this relation by

$$C_v = C_o V_T^{-\gamma} \quad (4.72)$$

where C_v is the varactor capacitance which takes on a maximum value at zero volts, C_o and follows a C-V curve dictated by the doping profile described by γ . The range of γ is usually between 0.3 and 3 as described by the doping profile; from linear graded junction to abrupt and extending to hyper-abrupt [133]. Consider the tunable resonator as a stand alone network, separated from the active device, and the feedback loop is open. The semiconductor varactor is usually biased via a bias-tee network, providing a DC low resistance path, however a high impedance open circuit path for RF current. In addition, the varactor DC block from the remaining half of the resonator, inductor or series transmission line, serves a three prong function. First, providing a Q transformation and raising the effective Q_{VM} , second reducing the RF voltage swing across the varactor and the possibility of forward conduction, and finally, setting the tuning gain value. The network represented here is first analyzed for $d\omega/dC_v$, while the inductance, L_T , is held constant with voltage and frequency. This is a reasonable assumption, however, this assumes the inductance is operating well below self-resonant frequency. The resonator frequency is given by

$$\omega_o = \left(\frac{C + C_v}{L_T C C_v} \right)^{1/2}. \quad (4.73)$$

The inductor L_F provides the dc return for the varactor path, sets the feedback voltage level, and has an inductive reactance which is small compared to L_T . Taking a partial derivative of

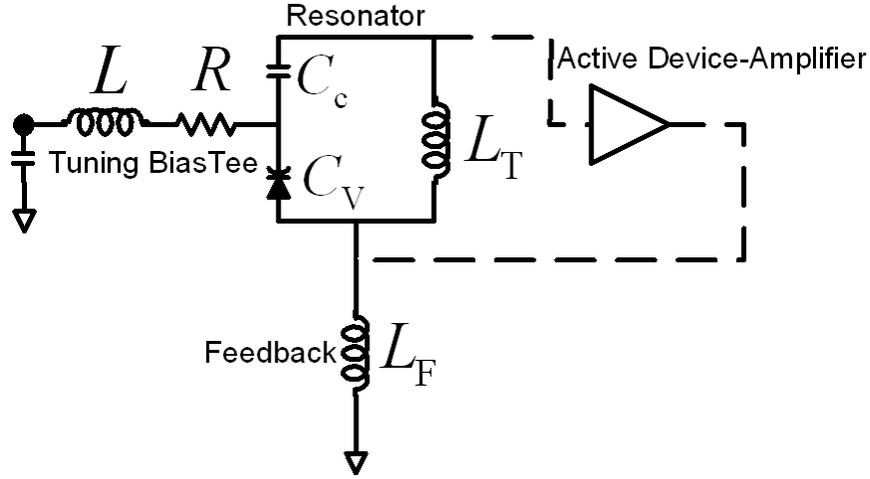


Figure 4.58: Varactor with bias tee line, resonator-inductor with tuning varactor, and ideal feedback amplifier void of parasitics provide the ideal tuning characteristics.

(4.73) with respect to C_V gives

$$\frac{\partial \omega_o}{\partial C_v} = -\frac{1}{2} \frac{1}{LC_v^2} \frac{1}{\omega_o}. \quad (4.74)$$

Using (4.73) and simplifying gives

$$\frac{d\omega_o}{\omega_o} = -\frac{dC_v}{2C_v} \left(\frac{C}{C + C_v} \right). \quad (4.75)$$

Using $C_v = C_o V_T^{-\gamma}$ we find next

$$dC_v = -\gamma C_o V_T^{-(\gamma+1)} dV_T \quad (4.76)$$

and substitution into (4.75) and simplifying gives the desired tuning gain equation as

$$K_o = \frac{\gamma}{2} \frac{1}{V_T} \frac{\omega_o C}{(C + C_v)} \text{ radians/volt-sec.} \quad (4.77)$$

Consider a case where C is large and consequently, the varactor is tightly coupled. This condition imposed for the purpose of simplification. We will dispense with the concern of nonlinear

effects as treated in [134], however, recognize this as assessing the effective capacitance of the varactor without altering the sensitivity of the varactor, γ . As long as the tuning voltage plus RF voltage is bounded, that is $0 \ll (V_T + v_{\text{sig}}) \ll V_{BV}$, the tuning gain equation is valid. Then, for $C > C_v$ the tune gain equation is written as

$$K_o = \frac{\gamma}{2} \frac{1}{V_T} (LC_o V_T^{-\gamma})^{-1/2}. \quad (4.78)$$

The central point, given a hyper-abrupt junction varactor with $\gamma = 2$, linear tuning gain is possible as (4.78) reduces to $(LC_o)^{1/2}$ and K_o is a constant independent of the tuning voltage, V_T . Therefore, the deviation of the tuning curve from the best straight line (BSL) fit is zero, and the linearity which is a measure of deviation from BSL is excellent. Although the analysis is simplified, as it does not include the reactance contour associated with the active device, parasitics, or non-linear affects, the central idea is clear. A varactor C-V relation if properly augmented will provide linear and wide band tuning [135].

4.6.7 Uniqueness of BST applied to linear tuning

The BST varactor operates with a high permittivity thin-film dielectric and depends on a strong electric field to alter the dielectric property. There is no junction and the peak capacitance occurs at zero applied field, that is at $V_T = 0$. The field can be applied across the dielectric film with either polarity, and therefore the C-V characteristic displays a symmetric profile about zero tuning voltage. In [136], modeling of the capacitance nonlinearity is found by assuming a power series expansion for the field-polarization relationship of the material permittivity and nonlinearity. The basis of the polynomial in the context of ferroelectric films is called the Landau-Devonshire-Ginzburg (LDG) model. The central result of [136] given is

$$C(V_T) = \frac{C_{\text{max}}}{2 \cosh \left[\frac{2}{3} \sinh^{-1} \left(\frac{2V_T}{V_2} \right) \right] - 1} \quad (4.79)$$

where V_2 is defined the voltage that produces a capacitance value of $\frac{1}{2}C_{\max}$. Further investigation of (4.79), shows an asymptotic behavior in the low-field, $V_T \ll V_2$, and the high field, $V_T \gg V_2$ and an empirical expression that provides a good match to these extreme asymptotes is given by

$$C_V(V_T) = \frac{C_{\max}}{\left[1 + \left(\frac{2V_T}{V_2}\right)^2\right]^\gamma} . \quad (4.80)$$

The result provided by (4.80) is key to understanding the inherent linearity observed in voltage tuned oscillators utilizing BST [94, 138, 139, 140] as the varactor element. Designating C_{\max} at zero volts as C_o and following the same line of reasoning as before, we find dC_v/dV_T as

$$\frac{dC_v}{dV_T} = -\frac{8V_T\gamma C_o}{V_2^2} \left[1 + \left(\frac{2V_T}{V_2}\right)^2\right]^{-(\gamma+1)} \quad (4.81)$$

and for the same network per figure 4.58 we have using (4.75) and $C \gg C_v$ the tuning gain K_o with a BST varactor as

$$K_o = \frac{4\gamma V_T}{V_2^2} \frac{1}{\sqrt{LC_o}} \left[1 + \left(\frac{2V_T}{V_2}\right)^2\right]^{-\left(\frac{2-\gamma}{2}\right)} . \quad (4.82)$$

For $\frac{2V_T}{V_2} > 1$ and $\gamma = 1$, we have independent of tuning voltage

$$K_o = \left(\frac{2}{\sqrt{LC_o}V_2}\right) . \quad (4.83)$$

Thus, the intrinsic property of BST permits linear tuning to be realized. For tuning voltage $V_T \gg V_2/2$, linear tuning is assured for a wide range of γ , i.e., we find this is the case for values of γ of 0.25 to just over unity. At $\gamma = 1$ linear tuning is exact. Although many of the BST based oscillators implemented to date reported linear tuning, it has not been the primary focus of the work. Interesting to note that this effect is independent of the geometry of the capacitor, as the linear effect is observed in both the MIM and IDC designs. So the resulting linearity would appear to be primarily an outcome of the behavior of the property of the dielectric film

and the associated C-V relation. It is important to note, that no implicit minimum capacitance is stated for the BST varactor. However it must exist as V_T is limited to V_{BK} the dielectric breakdown voltage. A plot of (4.82) demonstrates the tuning gain achieved as a function of γ with V_2 set to 45 V. The linearity achieved requires the derivative of this function. As γ approaches unity, in the range of 0.75 to 1.0, the tuning gain is flat above $V_T = 20$ volts. Even at $V_T = 10$ volts, an inherent linearity of less than 4%, BSL, is demonstrated. The transition point of the tuning curve providing constant K_o is a function of V_2 . Important to note, that as V_T goes to zero, so does K_o . The consequence from (2.31) is for a phase lock loop gain to go to zero. Prior to this event, loop peaking, instability, and eventually loop hang will occur [146]. The tuning voltage of zero volts should be avoided in phase lock applications. A discussion of this in detail is in Section 5.1.4.

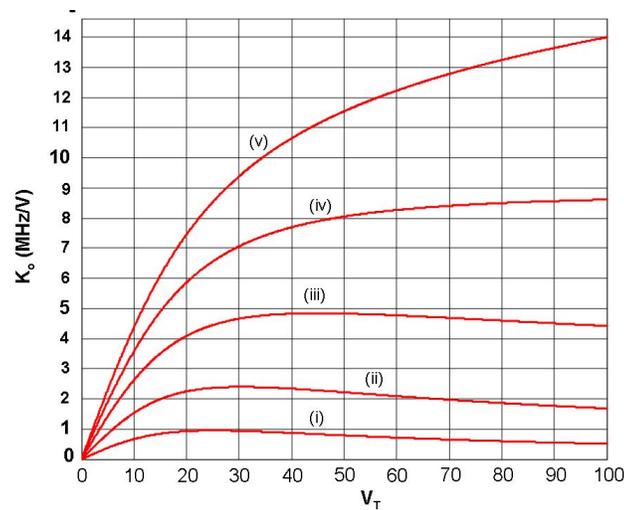


Figure 4.59: The computed oscillator tuning gain K_o in MHz/V with an IDC BST varactor. Parasitic capacitance of the circuit is neglected and V_2 is 45 volts. The values of γ are: (i) 0.2; (ii) 0.45; (iii) 0.75; (iv) 1.0; and (v) 1.2

4.6.8 Experiment, observation and data

An experiment to verify and detail these observations is conducted in the 90-200 MHz range with the construction of a set of VHF tunable oscillators. The choice of low frequency oscillators is deliberate. Parasitic elements are readily checked, and the influence of large signal operating voltages on the behavior of the varactor is monitored. Two configurations utilizing the BST varactor are incorporated in each oscillator. An interdigital finger form (IDC) capacitor and a metal-insulated-metal form or MIM. Measurements included the frequency versus tuning voltage, frequency characteristic, VCO K_o or tuning gain, and finally linearity obtained from the derivative of the tuning gain. This data included a 1000 point measurement of K_o to assure proper oscillator tuning stability and a smaller collection of frequency characteristics. The data is imported and overlaid with calculated results of the predicted oscillator frequency range and tuning gain using various methods to obtain C-V characteristics. These methods included polynomial fitting to the C-V data and the use of [136] and (4.80). We note that unlike the junction varactor, the range of γ applied to the C-V relation describing the BST tuning linearity characteristic is greater. Not until γ is sufficiently larger than unity is there a dramatic departure from tuning linearity. Our fitting of all the measured data to the Figure 4.58 curve demonstrated a slightly different trend line to tune gain. Main differences noted were the V_T point of departure from nonlinear to linear tuning and the rate or slope in which this transition occurred, both controlled by γ and V_2 . Both of these elements therefore, effect the resulting K_o . An increase in V_2 or in γ decreases K_o . Part of the measurement problem is finding the value of V_2 . It is not readily measured for our sample of IDC capacitors due to the rise in leakage current. Leakage current tends to rise at increased applied voltage and there is concern for operation past breakdown voltage. So instead, we attempt to find the value of V_2 from extrapolation of a 5th order and 9th order polynomial and subsequently use this polynomial to fit the C-V curve of (4.80). Unfortunately, the nature of the polynomial fit to a symmetric parabolic function will quickly diverge at the end of the known terminations points. Therefore, accurate extrapolation is not possible. So instead, an exponential fit is

used to describe the half-sided C-V curve description of the BST varactor. For the case of the IDC varactor, we find $C_V(V_T) = 6.572 \exp(-.014235V_T)$. Extrapolation to $C_{\max}/2$ was straightforward and predicted value of $V_2 = 50V$ is obtained. At this point, two functions are available to predict the C-V curve. One, is Equation (4.80), and the other a higher order polynomial. These methods for fitting the C-V data are found successful and the quality of fit is shown in Figure 4.60.

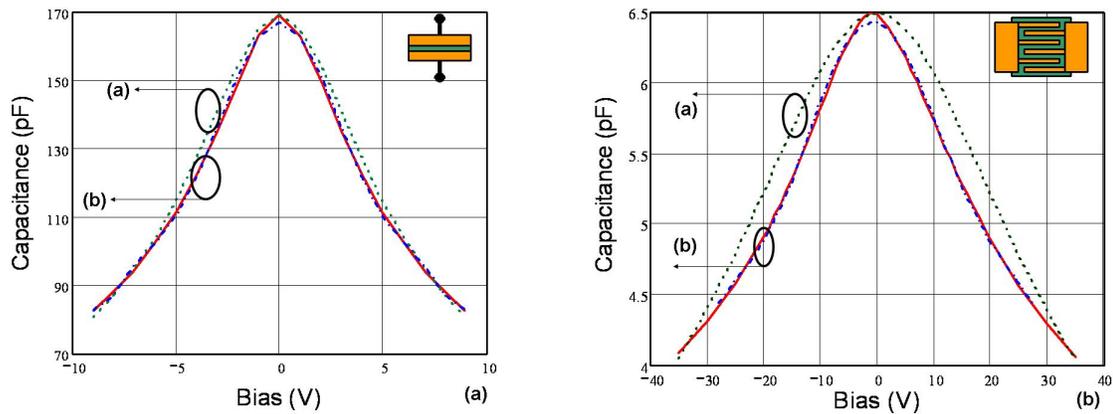


Figure 4.60: BST MIM C-V curve (a) and IDC C-V curve (b). The (a) arrow is fit using (4.80) while (b) arrow is fit from the appropriate polynomial, see (4.87) and (4.86). Measurements are conducted at 10 MHz.

The next step forward is to use these fitting functions to calculate the operating frequency versus V_T , including parasitic capacitance for both varactor types. This would include the input capacitance of the FET devices and parasitic capacitance of the dc feed inductor chokes, which are operating past their self-resonant frequency. The IDC test circuit schematic is shown in Figure 4.65 and the test card photo in Figure 4.66. The calculation for the frequency characteristic curve for both measured and calculated results of the IDC varactor is shown in Figure 4.61. This data demonstrates reasonable agreement between the polynomial generated C-V curve and measurement. However, the error between using the field dependent equation

of (4.80) and measurement data is worse. Nevertheless, the worst case frequency error for both measurement data and all calculations is less than 2% over the measured frequency range.

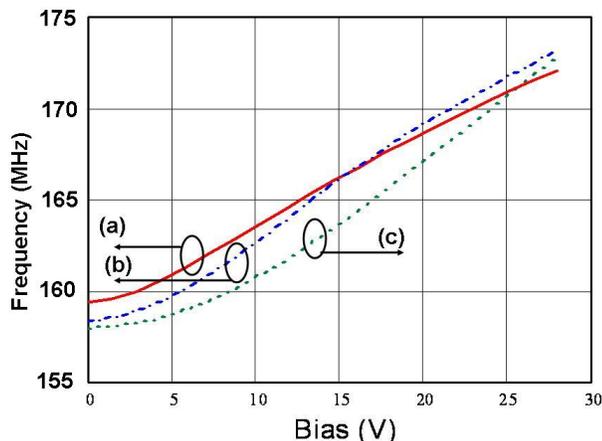


Figure 4.61: The BST IDC varactor tuned oscillator frequency characteristic: (a) measured; (b) applying polynomial derived C-V; (c) applying field based model.

The K_o or tuning gain is the derivative of the frequency characteristic. The IDC measured and modeled fitting to measured data is shown in Figure 4.62. This plot consists of 20 measurement points so the initial zero data point is absent. This is corrected in the plot of MIM K_o and as expected both devices have a zero tune gain as V_T passes through zero. The polynomial data fit of the C-V characteristic curve used in the frequency calculation and then in the first derivative evaluation agree very well with the measured data in the low field regime, that is from 0-5 volts. For tuning voltage values above 5 volts, there is divergence in the fit to measured data and both models predict a tuning gain higher than realized. Below 5 volts the fit to K_o using the polynomial derived C-V curve is very good, less than 0.5% error. However, the fit to (4.80) is worse. Nevertheless, again the slope and reduction in the tuning gain above 10 volts using the polynomial derived C-V follows the trend line. Measurements correlate well with the lower value of γ presented in Figure 4.59. In that case, $\gamma \sim 0.5$ and operation is in

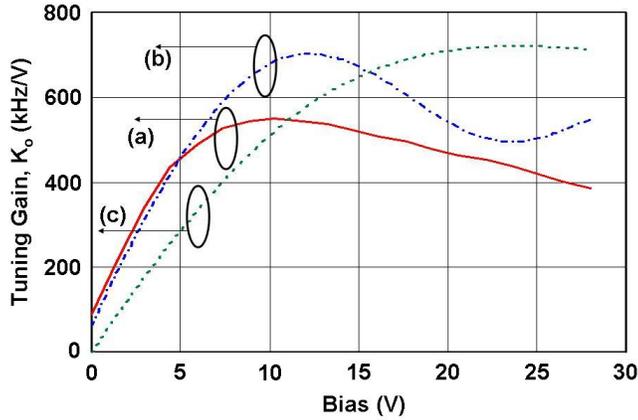


Figure 4.62: The BST IDC varactor tuned oscillator frequency characteristic: (a) measured; (b) applying polynomial derived C-V; (c) applying field based model of (4.80).

the higher field regime, $V_T > 5V$. Any attempt to fit the measured tuning gain data to either model over the entire range was met with difficulty. Either the match of the slope in the low field regime is met with a considerable overestimate of tuning gain in the high field regime, or fitting the tuning gain in the high field regime is met with an inadequate slope of gain in the low field regime. It appears there are two distinct field effects taking place and therefore, a need for modeling these two regions distinctly for the IDC varactor. In a separate treatment, we believe this anomaly is due to the excessive varactor leakage in the BST IDC varactor case, and a consequential reduction in K_o . See Section 4.6.9. A main point of interest in [136] is the presence of a fringe capacitance which reduces tunability. The effect of this capacitance is not unlike a shunt parasitic capacitance and is particularly an issue in smaller area devices. The value of the fringe C, C_f , is fixed, not a function of tuning voltage and is given by $C_f = \kappa(P/d)$. The value κ is a constant with the dimensions of capacitance and is independent of field and material thickness d and directly proportional to the device periphery area, P . At first glance this fringe capacitance would tend to compensate and reduce the overestimate of tune gain by virtue of the dilution of the C-V sensitivity. The modification of the C-V function

due to fringing is

$$C_V(V_T) = \frac{C_{\max} - C_f}{2 \cosh \left[\frac{2}{3} \sinh^{-1} \left(\frac{2V}{V_2} \right) \right] - 1} + C_f \quad (4.84)$$

and unfortunately does not provide an improved fit to our IDC C-V measured data. It does however provide a better fit in the higher field regime for the MIM varactor. However, the improved fit is minor and does not influence or improve what is already a reasonable fit to measured data for the tuning frequency and the tuning gain for the BST MIM varactor tuned oscillator.

As previously stated, in the case of the MIM varactor better agreement between measured and modeled characteristic frequency is found. Again both a C-V polynomial and E-field model are generated to fit the measured data subsequent to finding the operating frequency and the tuning gain. The agreement with both models and methodology is good, with error in prediction of operating frequency less than 1%. The tuning gain also demonstrated good agreement although the polynomial fit over and under estimates beyond a tune voltage of 4 volts, while the E-field model provided a better agreement over most of the tuning range. Since the data collection consisted of 100 measurement points, the fit to a tuning gain value of zero at V_T equal to zero is clear, see Figure 4.64. A review of the modeling steps and the process is briefly discussed next. Reference to schematic Figure 4.65 is used.

The total parasitic capacitance contributed by the network is 4.5 pF, designated C_d . The operating frequency and the derivative includes the varactor coupling C , C_c , the varactor C_v , and the resonator inductance, L . Included in the coupling capacitance to the varactor, C_c , is a portion of the capacitance associated with the shunt C-series L-C resonator network. Therefore the calculated operating frequency is

$$f_o = \frac{1}{2\pi} \left[\frac{C_c + C_v}{L(C_c C_v + C_d(C_c + C_v))} \right]^{1/2}. \quad (4.85)$$

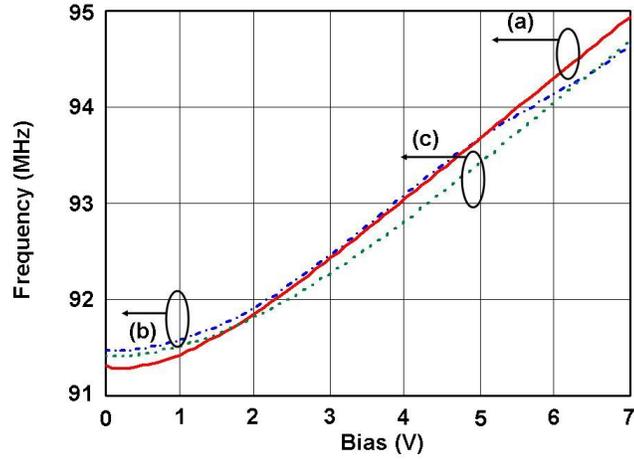


Figure 4.63: The BST MIM varactor tuned oscillator frequency characteristic: (a) measured; (b) applying polynomial derived C-V; (c) applying field based model of (4.80).

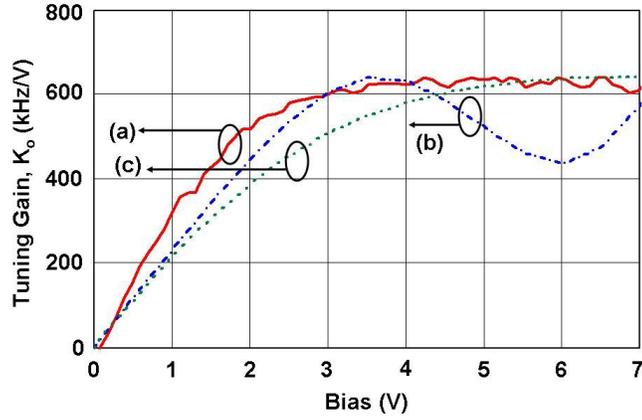


Figure 4.64: BST MIM varactor tuned oscillator frequency characteristic: (a) measured; (b) applying polynomial derived C-V; (c) applying field based model of (4.80).

The fitting polynomial for the IDC varactor is found as

$$C_{poly}^{IDC}(V_T) = 6.4296 - .008V_T - .0111V_T^2 + .00063921V_T^3 - 1.5659 \times 10^{-5}V_T^4 + 1.451 \times 10^{-7}V_T^5 \quad (4.86)$$

with a regression coefficient of $R = 0.99998$. While the polynomial fitting function for the

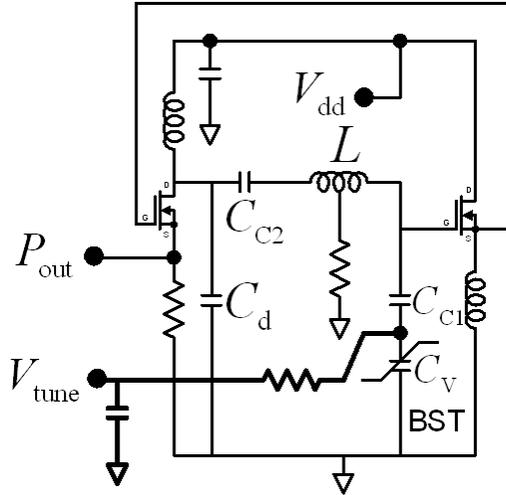


Figure 4.65: Schematic tunable oscillator dual FET test card with IDC BST varactor

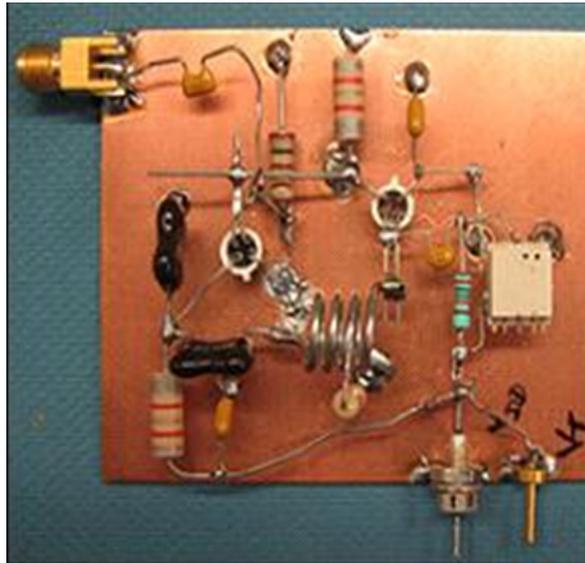


Figure 4.66: Photo of test card. Packaged IDC BST varactor center right. Package contains 4 varactors in anti-series configuration, only one unit in use in this test card. The tapped resonator and dual insulated FET devices are located in center of card.

MIM varactor is found to be

$$C_{poly}^{MIM}(V_T) = 166.91 - 4.4237V_T^2 + .123V_T^4 - .0016893V_T^6 + 8.4783 \times 10^{-6}V_T^8. \quad (4.87)$$

Noteworthy, is the IDC polynomial has both odd and even coefficients of V_T . Measurements below and above zero volts were not absolutely symmetric. In fact, drift was noted to be deliberate, and returning to previously measured values of capacitance yielded slightly different values. This is reflected in the slight asymmetric nature of the IDC polynomial function. The aim now is to use C-V equations to assist in finding the operating frequency versus tuning voltage and the derivative to assess tuning gain and BSL fit. With this data in hand, fitting the varactor C-V curve is again done with the use of (4.79) or (4.80), both providing good fit to each other however not necessarily the problem at hand, or the polynomial function of (4.86). We use these C-V relations in conjunction with (4.85) and its derivative and plot predictive results against measurements. A similar process is carried forward with the BST MIM varactor. The varactor used was documented in [145] and bench-marked along side a hyper-abrupt junction varactor. At the time of this publication, no effort was made to document the tuning linearity, however, it was noted on the aside and similar observations in follow up by other researchers [138, 139, 140]. We returned to the circuit used in this publication and the same MIM varactor. Our study included applying the model of [136] without recourse to the polynomial function to fit the C-V curve. Unlike the IDC varactor, measurements of the C-V curve demonstrated larger C-V change, better than 2 : 1 and the ability to obtain a voltage for $C_{\max}/2$ was easier. Therefore, the need to generate a polynomial and extrapolate to the required $C_{\max}/2$ value is not needed. The test set circuit for the MIM varactor is a Hartley configuration, the inductive feedback formed by a tap position on a toroid wound inductor partly forming the resonator. The active device is a junction FET. The network is shown in Figure 4.67 and the test set in Figure 4.68.

4.6.9 The reduction of tuning gain due to varactor leakage

Investigation of the tuning linearity and tuning gain of the IDC varactors revealed a disparity. When compared to the MIM varactor we found a deviation in tuning gain and reduction in K_o above 10 volts tuning and as much as 40% deviation from predicted at 25 volts. We believe this

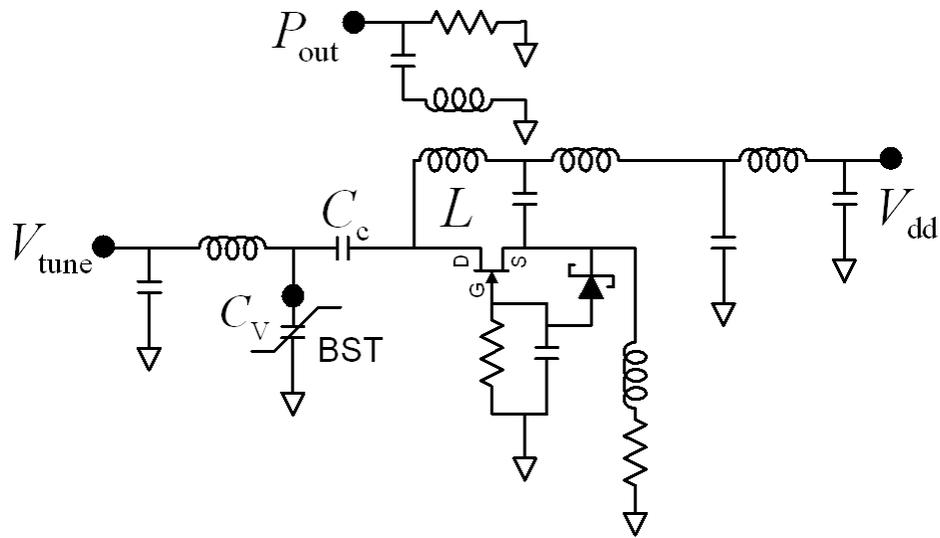


Figure 4.67: The VCO using the BST MIM varactor. The configuration is Hartley with a tapped toriod inductor and MIM coupled varactor forming the resonator.

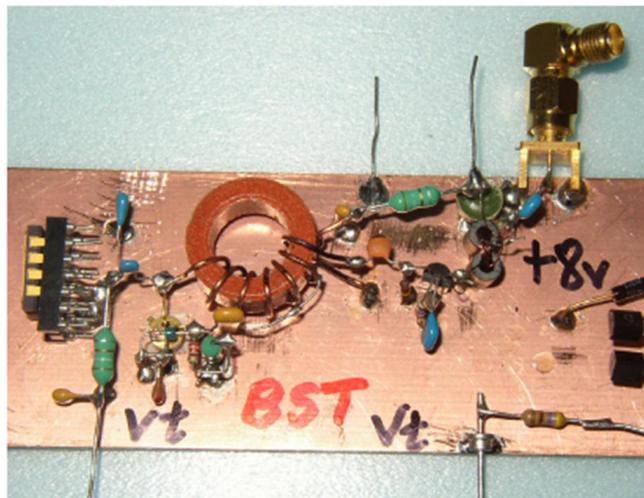


Figure 4.68: VCO using the BST MIM varactor, the packaged MIM varactor on left, the tapped toroid resonator and the coupling of the MIM varactor are visible center and to the left of the toroid.

drop in tuning gain, see Figure 4.62, is due to increased leakage current. This may be explained by considering the dilution in the capacitance term with decreasing varactor Q ; the unloaded Q_{UL} , a function of the leakage resistance. Particularly acute at higher tuning voltages, the

combination of peak RF signal voltage and the larger DC bias, raises the leakage value. In order to capture this factor we need to express the series varactor capacitance and leakage as an equivalent parallel network. Will consider the junction varactor however the same trend applies to the BST varactor except the gain reduction event would occur at higher tuning voltage instead at zero tuning voltage values. We have for the equivalent network equation for the varactor capacitance as

$$C_V = C_{P_V} (1 + 1/Q_V^2) . \quad (4.88)$$

Then recognize that the tuning gain is defined from (4.68) and these terms goes to zero as the Q_V goes to zero. The net effect is that a reduction in K_o occurs. Substitution for each of the partial derivatives in (4.68) in terms of the varactor Q and using (4.88) leads to

$$K_o(Q_V) = \frac{\gamma V_T^{\gamma/2}}{2V_T \left(L_T C_{P_o} \left(1 + \frac{1}{Q_V^2} \right) \right)^{1/2}} \quad (4.89)$$

where C_{P_o} is the equivalent parallel varactor capacitance due to finite varactor Q_V at zero tuning volts. For the special case where $\gamma = 2$ we have the simpler expression, plotted in Figure 4.69 and given by

$$K_o = \frac{1}{(L_T C_{P_o} (1 + 1/Q^2))^{1/2}} . \quad (4.90)$$

In general the reduction in K_o with other γ values as a function of the varactor Q_V will be dependent on the tuning voltage. A smaller change in K_o is noted with decreased Q_V since there is already a gain reduction with the increased tuning voltage. A check of this problem is verified in harmonic balance where a junction varactor with leakage is modeled via a series resistance component and varied. In addition a frequency sweep is conducted and the tuning characteristic generated. The flattening of the gain curve occurs quite rapidly at zero volts and above and is clear in Figure 4.70.

If we investigate the BST parametric properties we find an interesting dual to the junction varactor. Again Q degradation comes about due to leakage current. However, in the BST

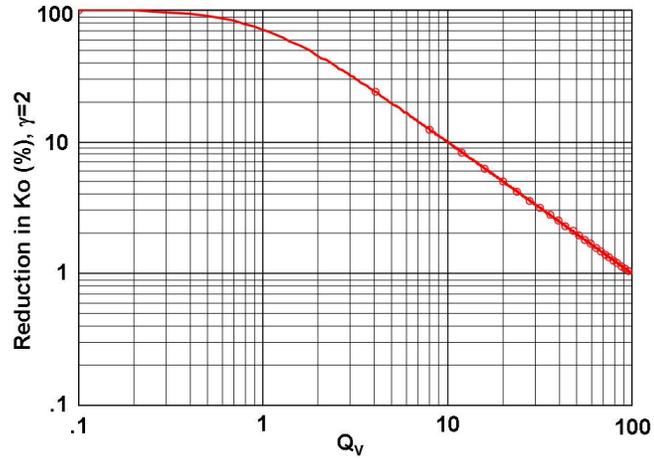


Figure 4.69: Tuning gain reduction due to varactor loss and leakage.

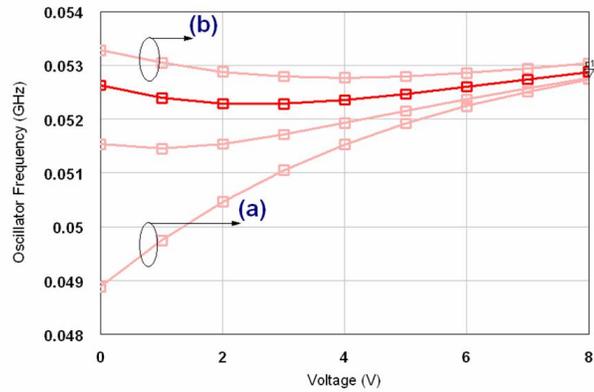


Figure 4.70: Harmonic balance simulation for a lossy junction varactor: (a) maximum varactor Q ; (b) minimized varactor Q .

varactor, the pivotal point for gain reduction is pushed out, beyond 0 volts and is a distinct function of γ . If $\gamma = 1$, no pivot point occurs. The tuning gain simply collapses, however tuning linearity is maintained! The function for tuning gain, under the influence of leakage in BST is

given by

$$K_o(Q_V) = \frac{4\gamma V_T \omega_o \left[1 + \left(\frac{2V_T}{V_2} \right)^2 \right]^{-\left(\frac{2-\gamma}{2}\right)}}{V_2^2 (1 + 1/Q_V^2)} \quad (4.91)$$

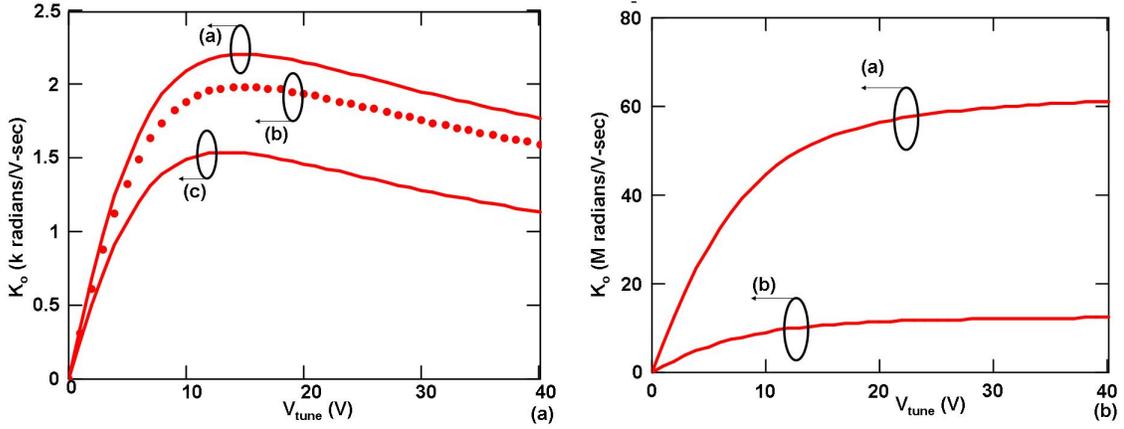


Figure 4.71: The BST tuning gain modeled with a leakage term. Shown in Figure 4.71(a), varying leakage and γ values lead to the gradual roll of in K_o as seen in measurement. In Figure 4.71(b), γ is fixed at unity. See text for the cases studied

In Figure 4.71 (a) the graphs (a) through (c) vary the leakage via the varactor Q degradation as before, from 100 in (a) to (3) in (b) and (c). In addition, slight changes in the fitting parameter γ , demonstrate decreased tuning gain as tuning values increase above 5 volts. In (a) and (b) $\gamma = .55$ while in (c) $\gamma = .45$. Departure in tuning gain at higher tuning values, as in the measured data, is in good agreement. In Figure 4.71 (b), the γ is maintained at unity, however the equivalent leakage is increased 200 fold. There is simply a uniform drop in tuning gain.

4.6.10 Summary and conclusions of this section

Initial work with these circuits and fitting predicted and measured results with only the model of [136] was met with some difficulty. Although the frequency tuning curve for both cases of

varactors is close, the error is significant enough to affect the accuracy of the predicted K_o or tuning gain measurement. A portion of the problem is traced to the accuracy of the C-V curve fit provided by the model. The other source of error is the presence of leakage current. The first issue leads to frequency error and subsequently error in the derivative function, as error is magnified in the prediction of the tuning gain. To this end, to improve the match between measured and predicted results, two areas were investigated. The first is the accuracy of the measured data. Deembedding of the parasitic C of the test set is crucial especially in the case of the IDC varactor. Although the parasitic C is accounted for in calibration, the $\Delta C_V/\Delta V_T$ or sensitivity of the varactor change with voltage is not. A separate calculation is required. A low shunt capacitance bias tee is required for accurate BST measurements. This is true even at low frequencies. A further low frequency measurement problem is identified in [159]. Bias tee networks constructed for low frequency AC coupling require large value blocking capacitors. These capacitors are not free of the pyroelectric effect and the capacitance value shifts with applied bias voltage. To this end, a low shunt parasitic capacitance bias tee fixture incorporating NPO 100 WVDC blocking capacitors are used in bias tee configurations, see Figure 4.72. The

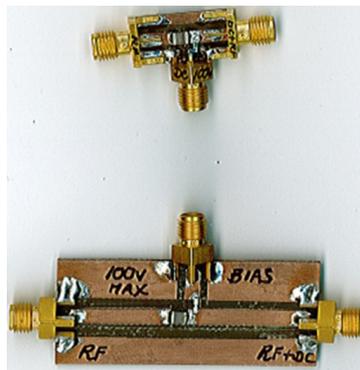


Figure 4.72: High Voltage Bias Tee, use of 100 WVDC NPO 6800 pF series block capacitor and series pair of 470 k Ω resistors. This arrangement in lieu of an inductor bias choke to minimize self resonant effects.

second is varactor leakage. Particularly with large RF voltage across the varactor, the sum of

DC and peak RF voltage will increase the leakage current and the reduction in varactor Q . The resulting effect will be a shift in the operating frequency. Both effects were verified by first remeasuring the C and V values at multiple points and extending the voltage points up to however not beyond the breakdown voltage. This data is subsequently used in the modeling process. Second, the reduction of the RF voltage across the varactor by reducing the coupling of the varactor to the resonator. An improved and more consistent match in measured versus predicted data occurs when the value of the varactor coupling capacitance is reduced in value to a value between 1 and 1/2 of the varactor minimum capacitance. Larger values of coupling will increase leakage current as the RF plus DC voltage applied across the varactor increases.

The BST thin-film varactor provides an intrinsic linear tuning frequency property in voltage controlled oscillators. This property is a function of the C-V characteristic curve dependent on the operating electric field regime. In the low field regime, at tuning voltages much less than V_2 , a good fit between model C-V and tuning sensitivity is found. In this region tuning linearity is not yet established and of course at zero volts tuning gain is zero. For several tuning volts above zero, in our case at approximately 10 volts, we find the measured data follows a polynomial generated C-V curve and leaves the regime of the model purposed in [136], and shown in Figure 4.62. Agreement is good and demonstrates tracking of measured data well into the higher field regime as the tuning gain begins a tendency to roll off. An analogous relation between the C-V fitting parameter γ for BST and the junction varactor is noted. While a γ of 2 is noted for linear tuning of LC networks the power coefficient in BST is nearly unity. Although both gamma values are associated with two different physical origins, it is interesting to note that the power coefficient in the BST formulation is somewhat gentler or more forgiving in realizing linear tuning than the junction varactor. A range of 5:1, or γ of 0.2-1.0, provides for a reasonable linear tuning capability. The MIM varactor was readily modeled with the E-field dependent relation alone, using (4.79). Leakage current in the varactor is found to be a significant cause of error in initial measurements and is verified by further decoupling

the varactor from the resonator network. The analysis presented here is straightforward and invoked no nonlinear treatment of the varactor characteristics or operation and the agreement is good provided the C-V generating curve fits properly over the measured tuning voltage range. These requirements are met provided that the bounds of the tuning voltage and the signal are within prescribed limits for both varactor types and excess leakage does not exist. In closing this section, it is instructive to study the sensitivity of the deviation of the tuning gain from best straight line fit for the BST varactor and the junction varactor. This is accomplished by comparing the derivative of the functions given by (4.77) and (4.82) for the case of identical resonators and feedback oscillator configurations. Adjustment in tuning voltage, breakdown voltage, the voltage V_2 , and contact potential voltage ϕ are made so that the identical tuning voltage scales are used. Finally the deviation in tuning gain is normalized to the maximum common operating frequency for both oscillators. Thus, the ΔK_o , on the y-axis, are identical. The family of curves are swept functions of γ from 0.1 to 1.8 and normalized tuning voltage V_{Tune} . The deviation of tuning gain is normalized to the operating frequency of the oscillator. Also to facilitate the comparison the plot of K_o deviation is plotted as an absolute value for the junction varactor as the slope of K_o is negative. The direction of increasing γ arrow, denotes the trend line for both the junction varactor and the BST varactor. That is, an increase in gamma to unity for the BST and 2 for the junction varactor, we see a trend line demonstrating improved tuning linearity. A key central point from Figure 4.73, we see that the deviation from BSL fit is less sensitive for the BST varactor. A result that bodes well for manufacturable linear tuned oscillators.

4.7 Conclusion

The behavior of a VCO which uses a thin-film ferroelectric varactor locked in a PLL is unique. Because the tuning gain approaches zero as the tuning voltage goes to zero, the VCO is subject to noise peaking and instability. This is particularly a problem in type-II systems which consist of two cascaded integrators since the rate of phase closure approaches 180° as the loop crosses

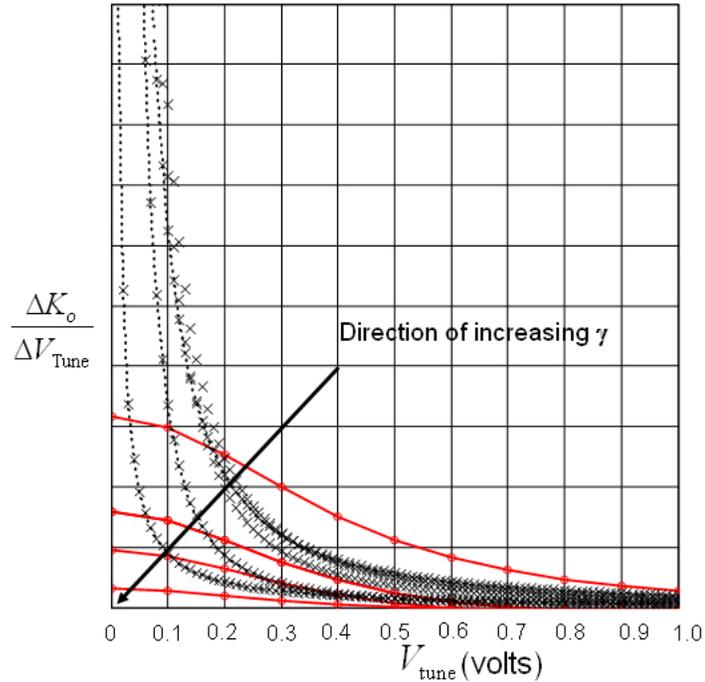


Figure 4.73: The junction varactor and BST varactor change in K_o with tuning voltage versus a family of γ values. The junction varactor denoted in hash line with -x- and the BST varactor in solid line with -o-.

unity gain. A loop which does not contain a cascade integrator topology, for example utilizing a passive ring-diode type phase detector or balanced mixer, would not suffer this drawback. However, such a system would require additional circuitry to support frequency acquisition. Noise correction and phase noise improvement is accomplished through proper design of the loop compensator-filter combination. The noise correction achieved is in line with the open loop gain available and the phase noise of the reference source and the open loop BST varactor controlled oscillator phase noise as addressed in Section 2.3.5.

No significant excess noise was seen in either the BST MIM or IDC varactors provided the leakage current and quality factor of the varactor is low, high respectfully. The presence of leakage current is potentially trackable to surface contamination. As leakage current sets in we see a slow degradation in unloaded Q , a rise in excess noise, and a significant drop in tuning gain.

Chapter 5

Implementation of Circuits and Systems

5.1 Overview of circuit implementations

The emphasis in this chapter is to present validation through the implementation of the concepts developed in earlier chapters. Power oscillator designs utilizing both internally matched FETs (IMFET) and Si-GaN HFETs are presented. The feasibility of utilizing an IMFET in a power oscillators is covered because it is an attractive solution with a minimum number of additional components. The oscillators implemented are negative resistance in topological form while latter in Section 6.2, we discuss an approach which focuses on the closed loop feedback power oscillator configuration. The circuit topologies discussed here demonstrate power devices in a common source configuration and will permit stable sources with good load conversion efficiency which are also thermally stable. Detailed work of a co-simulation design approach is presented and the accuracy and minimization of error from design to functional hardware is significant.

In Section 4.6.1, we discussed the phase lock acquisition problem incorporating a BST based varactor controlled oscillator. In this chapter, we highlight the noise correction properties of the loop with this same voltage controlled oscillator. A secondary circuit affect is presented,

which is associated with a circuit subtlety in the oscillator tuning line decoupling network of the locked oscillator. The resulting problem creates significant loop gain peaking and can lead to phase noise degradation in a phase locked system.

5.1.1 Negative resistance IMFET and GaN power oscillators

In this section we utilize the background material developed in Section 4.4 to synthesize power oscillators based on both GaN and GaAs FET devices. We demonstrate implementation of high efficiency oscillators at power levels that are competitive with power amplifiers, thus reinforcing the view of the PLM as a viable efficient transmit architecture. Further substantiation of the approach is found in Section 5.1.4 where the tracking phase lock loop is discussed. The test vehicle in this study consisted of power oscillators at 1.6 GHz and small signal oscillators at 2.7 GHz. Both sources implemented utilizing the BST varactor.

Stable amplifiers will provide stable oscillation if correct conditions are provided. First, the application of proper terminations are required, second, correct amplitude and phase feedback must be applied, and finally, a means of locking in the phase while maintaining the loop gain just above unity is necessary. Although this is a simplification of the processes, the main elements that contribute to stable oscillation system are covered. In developing power oscillators, the primary concern is device operating temperature and the removal of heat. Three terminal active devices permit the application of shunt or series embedding or feedback to any of the three nodes or branches of the active device. Oscillators, as a class of autonomous networks, have no specific input, output, or datum port. As such, the freedom to choose topologies is open to meet specific design objectives, such as maximizing output power, minimizing phase noise, increasing tunability, and optimizing efficiency. One approach to oscillator circuit synthesis, chooses one of the branches of the three port as a reference, and constructs embedding networks to permit a predetermined level of instability; whereby stability is characterized by small signal S or Y parameters. This methodology is carried forward in [6, 137, 174].

In this work, the motivation is to incorporate a packaged device for two primary reasons.

First, the ability to rapid prototype and second, the ability to readily investigate different type devices, for example, SiGe HBT, GaAs, and GaN. The downside of this approach is the introduction of package parasitics and the limitation in the topologies that may be constructed. For example, the packaged device structure for most power FETS investigated is optimized for the common source configuration. The device is composed of multiple unit cells, which are small geometry FETs, that are drain bussed in parallel. Each unit cell consists of an array of source via's, whereby the via's are the principle means of extraction of heat from the active device. This is accomplished through a grounded pad at the backside of the chip or substrate, making connection to the via array. In turn, the device sits atop a low thermal resistance heat paddle, providing the substrate with a low thermal resistance path to an external heat sink. The thermal resistance of this entire path is reduced by the addition of the heat sink. In the grounded source configuration, the heat profile tends to be largest under the gate, near the device centered on the array, with the device middle gate-source fingers the hottest. Therefore, the configuration of the power devices investigated did not permit a common gate connection, and with the principal mode of operation power gain, a common source configuration is required [181]. Thus, our focus is the power FET operating in a grounded source configuration, however configured as an oscillator. Two device types are investigated, a GaAs power FET which uses an internally matched structure (IMFET) [182] and a Gallium Nitride on Silicon, GaN-HFET. In [118], the author addresses the operation of the power FET oscillator utilizing the FET in the reverse channel mode. However, application of this configuration is not possible with the Si-GaN HFET as the transconductance is significantly reduced.

Transformation from a set of two port to three port S parameters are generated. This permits load and source impedances to be placed in series with any terminal. Shunt or series feedback is added to any set of terminals, and monitoring the small signal stability of the power FET is required. The majority of possible configurations must be dismissed, since a low thermal resistance path is disrupted. A new set of S parameters are continually calculated as terminations are varied and mapped onto the Smith chart. The generation of these maps on

the chart converts the 3-port resulting network with feedback into a two-port form, from which conditions for oscillation are validated. In light of the low thermal resistance path requirements, it is helpful to investigate the instability of the device from a nodal circuit and loop analysis point of view. Using this analysis approach initially, assists in identifying both the electrical and thermal paths clearly.

The grounded common source configuration is the preferred device orientation from a thermal perspective. Series feedback is applicable, however thermal ground must be maintained. The ability to generate a negative input resistance is studied and obtained from an analysis of figure 5.1(a). The usual case in providing instability in this two-port configuration is observed for the common source configuration, whereby a series source capacitive reactance, provided by C_E , is introduced. However, thermal ground is broken. We find it is possible though, to support negative input impedance using the same common source configuration, however with inductive series reactance in the source terminal. This is a configuration normally associated with degenerative feedback. Nonetheless, we show in this dissertation that regenerative feedback is readily possible if the other branches of the active network are suitably modified.

Normally, the inductive reactance is carefully selected to achieve an appropriate positive real impedance, for example in the design of low noise amplifiers. Furthermore, for the case of providing noiseless feedback via inductive degeneration, we find that there is a range of active device intrinsic properties which significantly benefit from inductive series feedback. In these specific cases, the noise figure and input mismatch losses are minimized. An optimum condition for providing nearly simultaneous conjugate match with minimized noise figure is possible [183]. The motivation in these design cases is not to promote instability, however to modify the input impedance to permit a favorable input impedance for noise matching while simultaneously improving the return loss [184]. However, in our application the motivation is to introduce instability while simultaneously providing for a low thermal impedance.

A device which is unconditionally stable will not be active generative and support the condition of oscillation for all passive real terminations [83]. A simplified model of the FET

and the circuit analysis of 5.1, with Z_E zero, demonstrates that a positive real impedance is always present. However, as additional circuit elements are added to the device model, providing local feedback connections, we see that the generation of a negative real impedance component is possible. For example, we select to extract output power from the drain network. Therefore, a requirement for the load termination is a finite impedance. A short circuited drain is not permitted. Therefore investigation of instability would include the affect of terminations. For the simpler configurations shown in Figure 5.1, the input impedance is not influenced by the drain termination. However, as additional feedback paths are added this situation is subject to change. Furthermore, other ports are available, and power is also available from the source or the gate terminal. Finally, as other feedback paths are added, for example with the presence of the drain-gate feedback capacitance, the possibilities to enhance instability while preserving the thermal conductivity path becomes more evident.

Consider inductive series feedback located in the source branch. The nature of this feedback is to first lead to degeneration. Then as the inductive series reactance increases, regenerative feedback occurs. Investigation of simplified models for both types of feedback, series C and series L, controlled by the AC series impedance Z_e is helpful. The goal is to find an input impedance, Z_{in} , for a common source configuration, which readily supports a negative resistance component while maintaining a high thermal conductivity path.

Consider Figures 5.1 (a) and (b). Writing an input loop current equation for both networks in 5.1 (a) and (b) gives,

$$V_{in} = I_{in} \left(\frac{1}{sC_{gs}} + \frac{1}{sC_E} \right) + g_m V_x \frac{1}{sC_E} \quad (a) \quad (5.1)$$

and

$$V_{in} = I_{in} \left(\frac{1}{sC_{gs}} + sL_E \right) + g_m V_x sL_E \quad (b) \quad (5.2)$$

where $s = j\omega$.

For the case of a short circuited output termination of the drain, the results are distinct

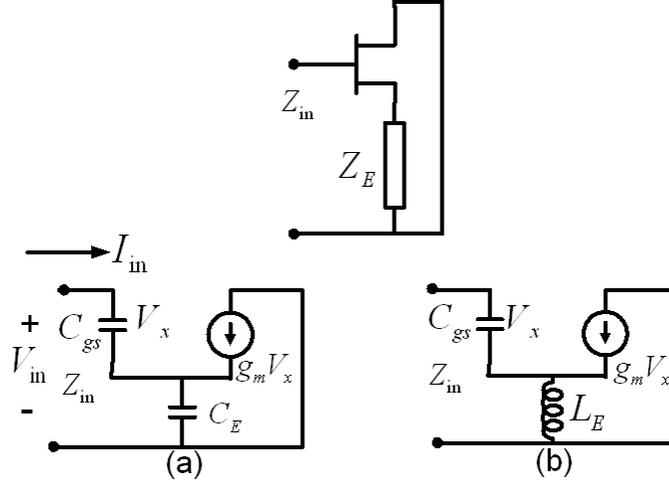


Figure 5.1: A HFET with a short circuit termination and source terminal returned through a series impedance Z_E displays: (a) negative real impedance with C_E while; (b) a real positive input impedance is displayed with L_E . The termination is a short circuit.

for the two types of lossless reactive series feedback conditions. The equivalent input circuit of the HFET is modeled as a parallel RC network. For simplification, the HFET active device real input component is neglected. The control voltage in both cases is identical, and we use a voltage controlled current source generator, with transconductance set to g_m . Then we have for both cases,

$$V_x = I_{in}/sC_{gs} . \quad (5.3)$$

Using Figure 5.1(a), the series feedback due to C_E provides negative input impedance component. Substitution for V_x using (5.3) into (5.1) gives

$$Z_{in} = \left(\frac{1}{sC_{gs}} + \frac{1}{sC_E} - \frac{g_m}{s^2C_{gs}C_E} \right) . \quad (5.4)$$

The imaginary terms due to input and feedback capacitance are resonated or impedance matched and therefore removed, leaving a negative real input impedance of

$$Z_{in} = -g_m/(\omega^2C_{gs}C_E) . \quad (5.5)$$

For the case of inductive series feedback, refer to Figure 5.1 (b) and (5.2). Substitution for V_x from (5.3) gives a positive real component for the input impedance given as

$$Z_{\text{in}} = +g_m L_E / (C_{gs}). \quad (5.6)$$

These simplified models show that a negative real component exists for series capacitive feedback and a positive real component exists for series inductive feedback. Investigation of the simplified analysis demonstrates that the level of negative resistance in Figure 5.1(a) increases with g_m , and decreases with increasing radian frequency, $s = j\omega$. In 5.1(b), we have an increase in input impedance with an increase in g_m and L_E . Both of these results are found for the case of a short circuited termination. However, changes in the load termination and introducing shunt capacitive feedback, C_{gd} , will alter the results.

Consider a model which takes into account the finite real output impedance of the device, R_o . This adds a shunt resistance in parallel with the controlled source. If L_L is zero, R_o is also in shunt with the series feedback inductance, L_E , shown in Figure 5.2. As L_L increases in value, the affect is to remove the shunting effect of R_o . For the moment, let us simplify and neglect the gate-drain feedback capacitance. Then the termination load L_L and the finite output resistance influence the input impedance despite the absence of C_{gd} . Finding I_{in} and using (5.3) gives

$$Z_{\text{in}}(s) = \frac{1}{sC_{gs}} + \frac{sL_E(R_o + sL_L)}{sL_E + R_o + sL_L} + \frac{g_m}{sC_{gs}} \frac{sL_E(R_o + sL_L)}{s(L_E + L_L) + R_o} \quad (5.7)$$

and is positive real for all $s = j\omega$. If the input is resonated, the imaginary reactance terms are canceled. The magnitude of the real input impedance is reduced relative to that obtained from (5.2) and potentially goes to zero as R_o and L_L go to zero.

The results of an analysis with series inductive feedback all returned positive real input impedance. Now consider the addition of shunt feedback, C_{gd} , in the form of gate-drain capacitance, see Figure 5.4. This feedback is either intrinsic to the device or may be deliberately

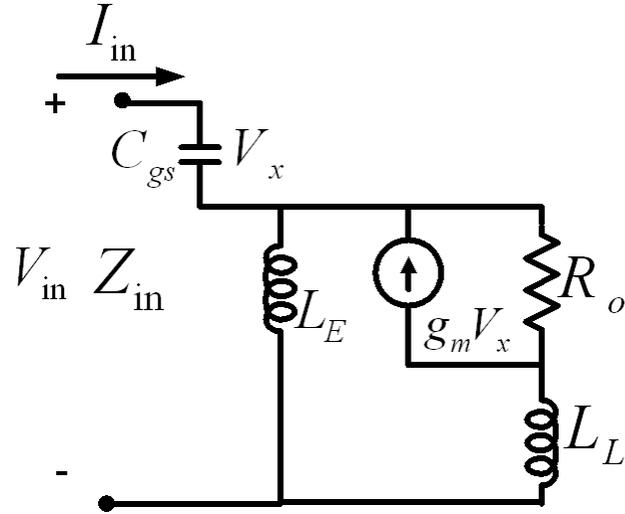


Figure 5.2: The HFET with a controlled generator with a finite output resistance, R_o , and inductive load L_L . Absent is the shunt feedback provided by the shunt gate-drain capacitance, C_{gd} .

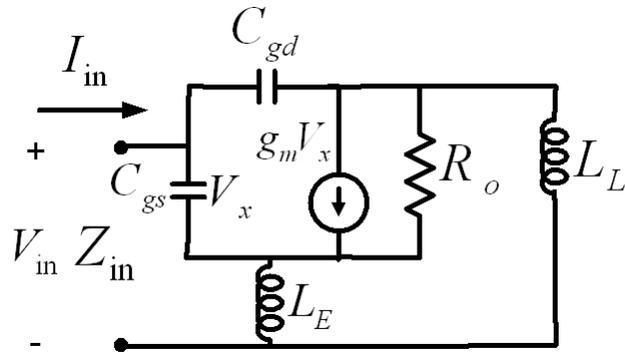


Figure 5.3: The HFET with addition of gate-drain shunt feedback capacitance. Despite the degenerative feedback provided by L_E , negative resistance is now plausible. The range and conditions for Z_{in} are shown in Figure 5.5.

added to the circuit. If the output termination is a short circuit and R_o is neglected, then a simple current divider is formed as seen in Figure 5.4. Using (5.2) and finding I_x as,

$$I_x = I_{in} \frac{\frac{1}{sC_{gd}}}{\frac{1}{sC_{gd}} + \frac{1}{sC_{gs}} + sL_E} \quad (5.8)$$

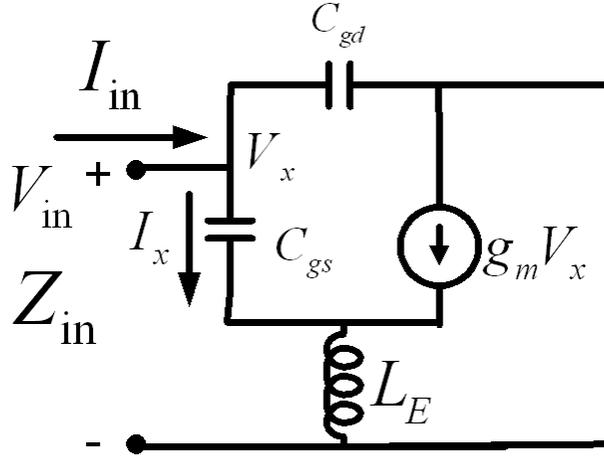


Figure 5.4: The HFET with shunt and series feedback with a shorted load. This configuration provides negative input resistance provided sufficient transconductance is available beyond a critical frequency.

we have the input impedance after substitution and simplification as,

$$Z_{in}(s) = \frac{1}{sC_{gs}} + sL_E - \frac{g_m L_E}{\omega^2 L_E C_{gs} C_{gd} - (C_{gs} + C_{gd})}. \quad (5.9)$$

The real part of $Z_{in}(s)$ leads to a negative resistance if $g_m L_E$ is sufficiently large and for radian frequencies greater than ω given by

$$\omega = \left(L_E \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} \right)^{-1/2}. \quad (5.10)$$

Hence, series inductive feedback will support a real negative input resistance. We find that contingent on the termination, device, and shunt and series feedback parameters, a range of real negative input resistance is supported.

The results are complicated by the relative values of each of the circuit elements. Again, characterizing the network via a parameter set such as S, Y or Z and applying the appropriate stability criteria or mapping, permits assessment and the validation of meeting a condition of instability. However, again in lieu of two-port network parameters, investigation of how

the various element values interact is helpful from a circuit perspective. The benefit of this approach is the ease in identifying the contribution that individual model elements play in producing instability. A nodal analysis returning the complex variable $Z_{in}(s)$ is desirable. The variability of the terms C_{gd} , L_E , g_m and the magnitude of the load reactance, Z_L , are studied for the complete network, shown in Figure 5.3. A plot of the real part of $Z_{in}(s)$ vs. frequency and the variability of the circuit parameters are shown in Figure 5.5. The input impedance for the most general case of Figure 5.2 is found as

$$Z_{in}(s) = \frac{s^4 (C_{gs}C_{gd}L_L L_E) + s^3 (g_m L_E L_L C_{gd}) + s^2 (L_E C_{gs} + L_L C_{gd}) + s (g_m L_E) + 1}{s^3 C_{gs} C_{gd} (L_E + L_L) + s^2 g_m C_{gd} (L_E + L_L) + s (C_{gs} + C_{gd})} . \quad (5.11)$$

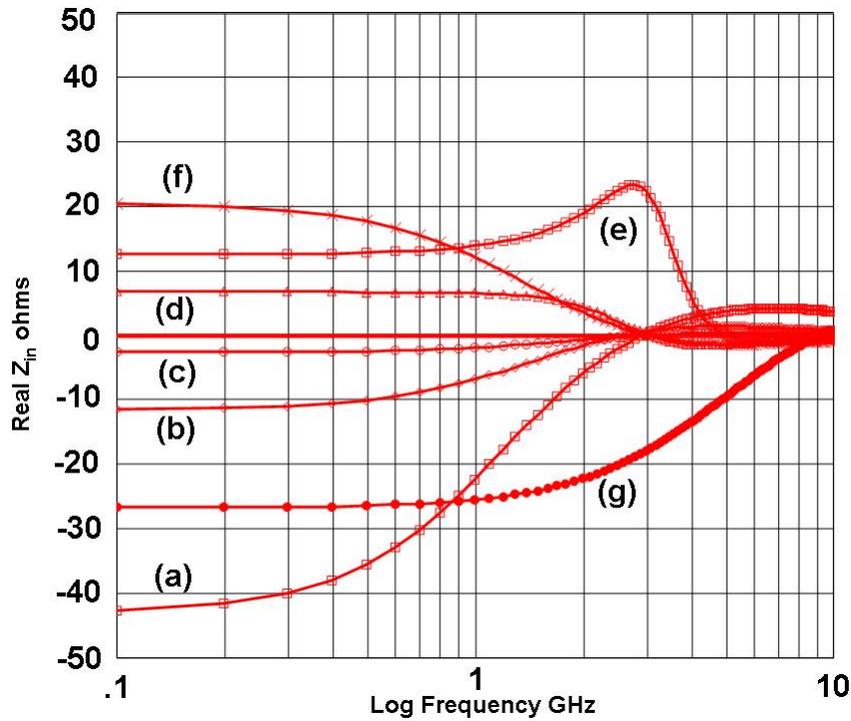


Figure 5.5: Z_{in} real vs. frequency (GHz) for the circuit modeled FET of Figure 5.2 with device and embedding values from Table 5.1

We now study various cases of (5.11), and consider the element values listed in Table 5.1. First in general, an increasing g_m , all other model parameters held constant, will result in an increase in the negative real part of Z_{in} . However, this statement will need to be further quantified. While, a decrease in g_m decreases instability, this trend may be offset with an increase in C_{gd} which increases instability. Furthermore, an increase in C_{gs} decreases the instability. A device with lower R_o will decrease the real part of the input impedance. However, a decrease in R_o can also lead to an increase in the real part of the input impedance along with a resonant peak in the real input impedance if the proper value of L_E is chosen, see Figure 5.5 (e). Table 5.1 along with Figure 5.5, illustrate some of the required conditions to promote instability through the introduction of negative input resistance. In addition, the required topology providing for a thermal conductive path is also investigated through alteration of the magnitude of L_E . Figure 5.5 (g) is particularly interesting, as this case supports a broadband negative resistance of nearly 2 decades, with a moderate value of g_m . Here is a case whereby a moderate g_m permits a wide frequency range of negative resistance to be supported providing the terminations and feedback are appropriate.

Utilizing a simple model, and studying the variability of the real part of Z_{in} , we can conclude that several circuit embodiments are required. First, an inductive termination is desirable. Second, adjustments in C_{gs} will position the magnitude of the negative real component, and third, the magnitude of the source inductance can be increased at sufficiently high frequencies, if a large g_m is maintained. However, if care is exercised in the selection of the terminations, a moderately low g_m supports a broad frequency range of negative resistance. For example, shown in Figure 5.6 is a case for g_m of 30,000 μmhos , with shunt and series feedback capacitances of 0.5 pF, and series feedback inductance of 0.8 nH. The load inductance is set to 3 nH. Through a frequency of 3 GHz, despite the minimal g_m , the device will support low series resonator Q as the series resistance is less than $-10\ \Omega$.

Mapping on a chosen plane, for example Y , Z or S , is also insightful. The frequency sweep for a given set of measured S parameters for the two port is as accurate as the model and all

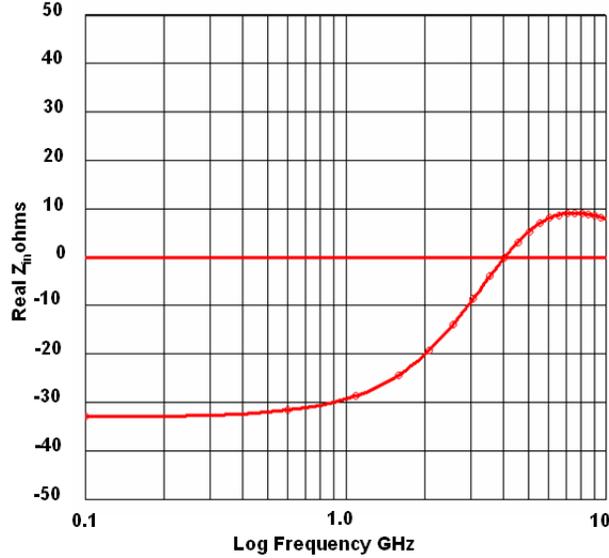


Figure 5.6: An active device with small g_m , less than $.040 \text{ } \Omega$, will readily support negative resistance through 4 GHz, provided proper feedback and terminations are incorporated.

known embedding element values. For a power FET device, we have found that it is possible to obtain the necessary conditions to support oscillation with the source both DC and thermally grounded. That is to say, since the real part of the input impedance demonstrates a negative real component with source inductance alone, both S_{11} and S_{22} are potentially greater than unity and the support for the condition of oscillation is satisfied. Therefore, inductive feedback, placed in series with a power FET source lead will provide conditions favorable for oscillation and satisfy the requirement for the necessary heat spreader.

We demonstrate next that this is indeed possible. Investigation of a power GaAs FET, an internally matched FET, IMFET, and Gallium Nitride on Silicon, GaN-Si HFET, all permit DC-thermally grounded source connections that will oscillate in a stable mode. S parameters are obtained from measurements which validate nonlinear models. The IMFET linear S data is provided by the manufacture for this device, and this data is also validated through measurements and mapping for instability. This mapping then drives the value and physical shape of the inductance used to return the device source to DC and thermal or ambient ground. Physical shape, reactance vs. frequency, and losses of the inductance plate are available through

Table 5.1: FET circuit modeled parameters

FET device parameters and embedding circuit elements					
Plot Line	L_L (nH)	L_E (nH)	C_{gs} (pF)	C_{gd} (pF)	g_m (mhos)
a	2.9	.75	1	1	.08
b	3.7	1.2	2	1	.08
c	2.7	1.2	2	1	.08
d	2.7	1.2	4	1	.08
e	1	2	3	1	.04
f	2.7	2.5	2	1	.08
g	1.5	.25	.50	.20	.075

EM-simulation.

Copper is the desired material to operate as the heat spreader, and provide the series inductive source plate. Brass, although not as good as Copper, has a reasonable thermal heat transfer coefficient. Brass, with over 4500 times better thermal conductivity compared to air is fashioned into a rectangular plate and attached to the back of the lead frame of the HFET. The aspect ratio of the plate and height in air above a perfect conductor is modeled in a two dimension, 2.5D, EM simulator.

Shown in Figure 5.7 and 5.8 are the EM simulation setup and the S_{11} port reflection coefficient versus frequency. The inductive source plate for the Si-GaN HFET and the active device attachment are shown in Figure 5.7. The plate is bent and mounted above a perfect electric conductor and separated by an air dielectric layer of 160 mils. Therefore, there is also a small distributed capacitance. The consequence of this capacitance is the plate operates as a tuned network and is parallel resonant at 11.2 GHz, see Figure 5.8. Below resonance, the plate operates as the required inductive reactance, with 1.35 nH of inductance over the 4–6 GHz frequency span. This inductance, when placed in the source lead with proper load termination in the drain, is used to generate a range of $\Gamma_{in} > 1$ in magnitude and phase and has the requisite negative resistance as a function of the load termination. A lossless termination is used in simulation, first with a constrained magnitude equal to 1 and the phase adjusted -180° to $+180^\circ$. In harmonic balance, the input signal power is increased to force limiting and the trajectory

of the input reflection coefficient is noted, see Figure 5.10 (ii). The limiting trajectory of Γ_{in} , as a function of frequency and amplitude is along the lines of a constant reactance contour when mapped on the chart. Therefore, a series resonator is appropriate. Since the imaginary component for the termination is inductive, a series resonator with a net capacitive reactance at the desired frequency is appropriate. In this case, a series line with a BST termination or a capacitive open stub less than $\lambda/4$ is chosen. Since the required active device termination is a simple single valued reactance, a one port providing the correct value of net capacitive reactance is sufficient to lock the phase and satisfy the condition for oscillation. Furthermore, this reactance could be satisfied by either a series or parallel resonator topology.

Shown in Figure 5.9 and Figure 5.10, are the results for both the measured and simulated input reflection coefficient for the inductive source plate configuration attached to the Si-GaN HFET. During development, the active device and suitable resonator are displayed together on the chart via a VNA. The resonator reflection coefficient must rotate in a clockwise motion, while the device has a counter-clockwise motion with frequency when plotted on the inside circle of the reflection plane. This is a necessary condition to insure stable oscillation at a single frequency.

Results of the simulation and measurement are displayed. The load termination is inductive and tuned to maximize the power output. The fashioned inductive plate is shown for a Si-GaN power HFET, model NPTB00004 from Nitronex Corporation, and the IMFET, Mitsubishi MGFC36V4450, GaAs FET, see Figure 5.7 right inset and Figure 5.11.

The inductive source plate fashioned for the IMFET is similar to the unit used for the GaN HFET, however wider to accommodate the larger flanged packaged. Adjustments in length and height of the plate are made to accommodate the larger width of the larger power FET. In Figure 5.9, we have measurements of the Si-GaN HFET with the inductive plate attached to the source. The distributed capacitance of the plate expands the input reflection coefficient and compresses the bandwidth. Simulation seen in Figure 5.10, is the large signal power FET model with the inductive source plate attached. The composite network is subject to a large

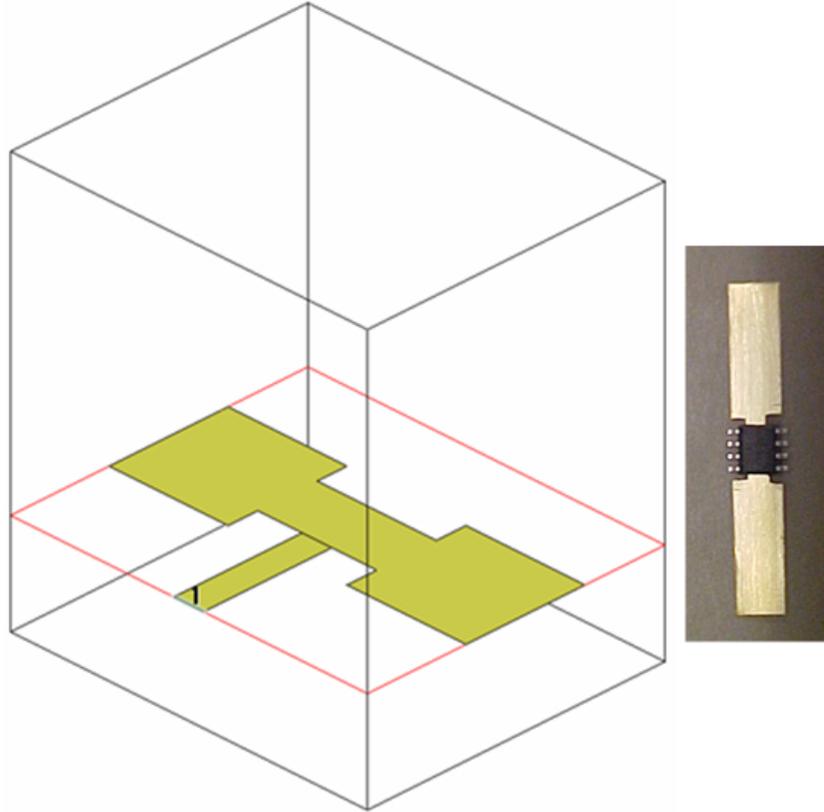


Figure 5.7: An EM model setup. A brass plate serves as a low series inductance with the backside substrate of the power FET. The required thermal conductivity is also provided. There is distributed capacitance from the plate relative to ground, so the plate itself appears as a tuned network

input power sweep from 0 to 35 dBm. The angular location of the composite network input reflection coefficient is in good agreement with measurements. In Figure 5.10 (i), the contours simulated are found as a function of large signal input drive. At 30 dBm input we have the $1/S_{11}$ just touching the unit chart. Contours in Figure 5.10 (ii) are those of the active device with source plate, an inductive input, requiring a capacitive termination.

In Figure 5.11, the IMFET is shown, attached to the inductive plate and heat sink. Bias stub and resonator stub are provided by 50 ohm semi-rigid coaxial lines, type Micro-coax UT-141A-TP, 3.58 mm (141 mil) OD with PTFE dielectric [186].

Oscillator output spectrum for both devices is similar in power and harmonic content, see

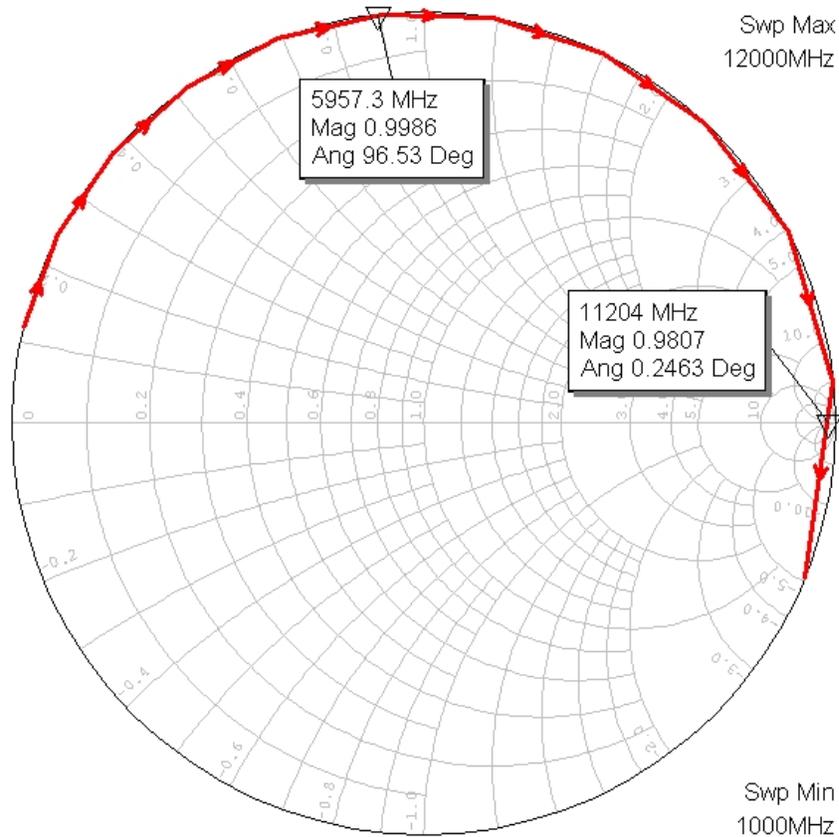


Figure 5.8: The frequency response, S_{11} of the brass backside plate for the power FET. The plate is 63mm (160 mils) above ground and fashioned to attach to the FET backside exposed paddle.

Figure 5.12. The spectrum at 4.8 GHz is attenuated by 13 dB prior to the analyzer input, therefore, the corrected output power is just over 30 dBm or 1 watt. This spectrum for the IMFET is obtained at 12 V and 400 mA and therefore, represents a load efficiency of 21%. Both the GaN HFET and the IMFET demonstrated similar efficiencies with this configuration. However, the main concern is the narrow negative resistance bandwidth as shown in Figure 5.13 and Figure 5.14 and discussed earlier in reference to Figure 5.9. In both cases, negative resistance bandwidth is less than 10% at 6 GHz. Simulation demonstrates agreement with this constraint, and is partly due to the combination of distributed C and L associated with the source inductance plate, and the potential instability that is supported by a device with

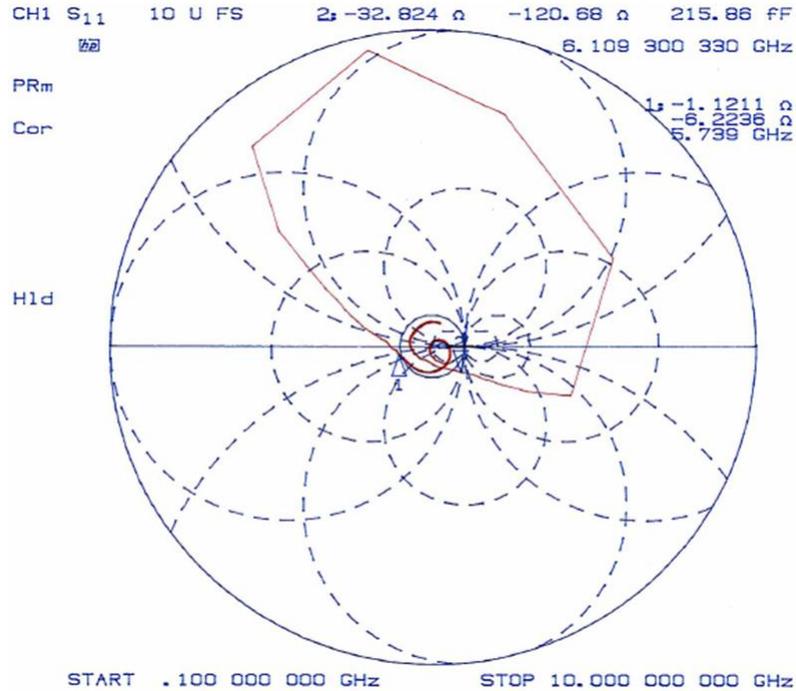


Figure 5.9: The measured input reflection coefficient, S_{11} , of the Si-GaN HFET with inductive source plate. Measurements were conducted at a drain voltage of +28 V and a quiescent drain current between 50 and 150 mA. The input reflection coefficient leave the unit circle at 5.7 GHz and returns to the unit circle at 6.1 GHz.

an internal matching network in place. In addition, the operation of the inductive plate is a tuned L-C network in the source lead forming a selective series feedback branch. This would also explain the harmonic rejection displayed, as harmonics are better than 35 dBc, see Figure 5.12. The high harmonic rejection is a consequence of a tuned network in the source branch, in conjunction with the internal match network, both which lead to selective gain and feedback with operating frequency.

5.1.2 Design overview and summary

The inductive source plates used for the Si-GaN HFET and the IMFET are shown in Figure 5.7 and Figure 5.11. The IMFET source plate is placed in an EM simulation model, shown in Figure 5.15. The resulting simulation for the input reflection coefficient for the device based on

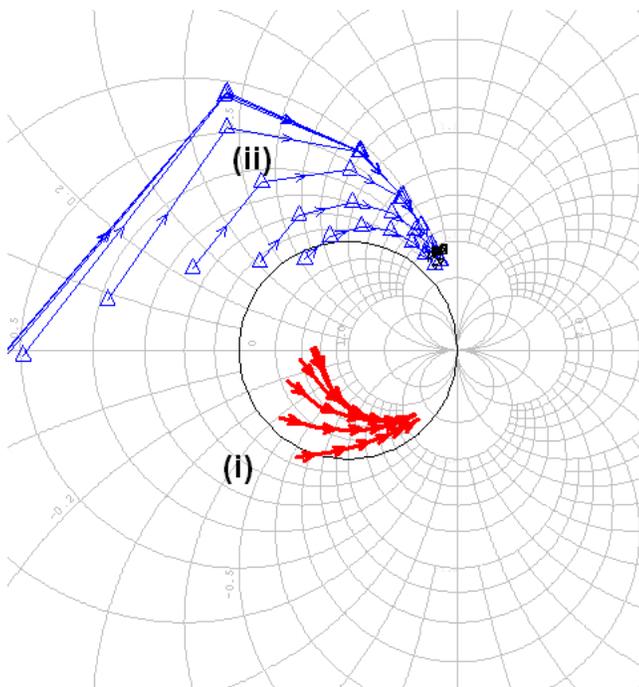


Figure 5.10: The simulated Si-GaN HFET nonlinear model with source inductance plate attached. The limiting characteristics of the composite circuit are found as a function of the input power level.

linear S parameters of the GaAs FET and coupled to the inductive plate is illustrated in Figure 5.16. This compares well with the results shown in Figure 5.13 and Figure 5.14, where both the input reflection coefficient and its reciprocal are plotted. Again, the clockwise rotation of $1/S_{11}$ on the chart is key for stable operation with the resonator, however the “loop” seen in the inverse reflection coefficient constrains the tuning range. A possibility of multi-oscillation is seen as the device reflection coefficient can intersect a resonator reflection coefficient locus at more than one point. In addition to the LC nature of the source plate, the IMFET due to internal matching further constrains the operating bandwidth. Reference to Figure 5.14 illustrates the constraint. The plot of the reciprocal active device reflection coefficient is bound inside the chart. A distinct set of points separated by approximately 200 MHz, from 4.65–4.85 GHz is seen. No varactor is added to the resonator used in this network, however the small number of circuit elements needed to support the power oscillator function at 4.8 GHz is attractive.

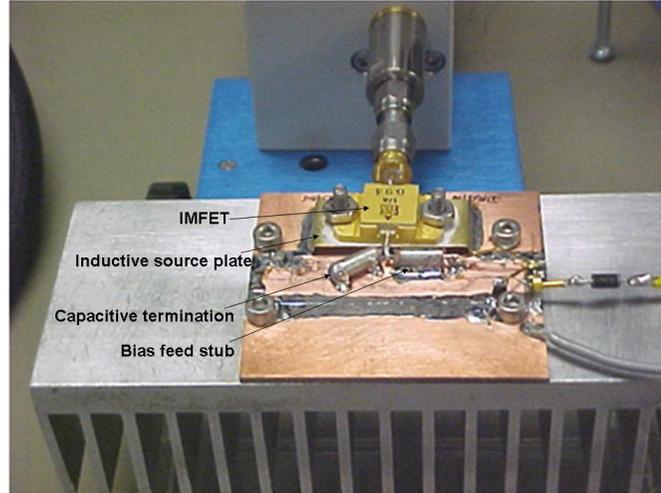


Figure 5.11: GaN and IMFET measurement test set for the negative resistance power oscillator. This particular arrangement permits the use of a power IMFET to be both DC and thermally attached via the source to ground, while permitting the generation of negative resistance. The inductive source plate also operates as the heat spreader.

The simulation conducted for the GaAs IMFET is linear as only linear two port S parameter data was available. For this case, conversion to three port S data is used and floating 3-port parameters permit the one port EM simulation data of the inductive plate to be added to the source terminal. A model for the shunt semi-rigid coax bias stub and shunt open circuit capacitance stub is added to the active device model. Finally, the output network which is a stub tuner, is adjusted for maximizing the output power based on a class A operating point, discussed further in Section 6.2. A similar method is applied to the GaN HFET, however a nonlinear model is available. To incorporate this model, the package effects on the device first had to be first removed. This is necessary as the nonlinear model did not permit the generation of the third floating port. After the device is isolated, the third port, source terminal, could be added back in conjunction with the EM model of the inductance plate. The final cascaded system is then applied to a harmonic balance simulation.

In this development, the feasibility of providing series feedback as regeneration in the source terminal is investigated. The feedback reactance in the source terminal is inductive, and would

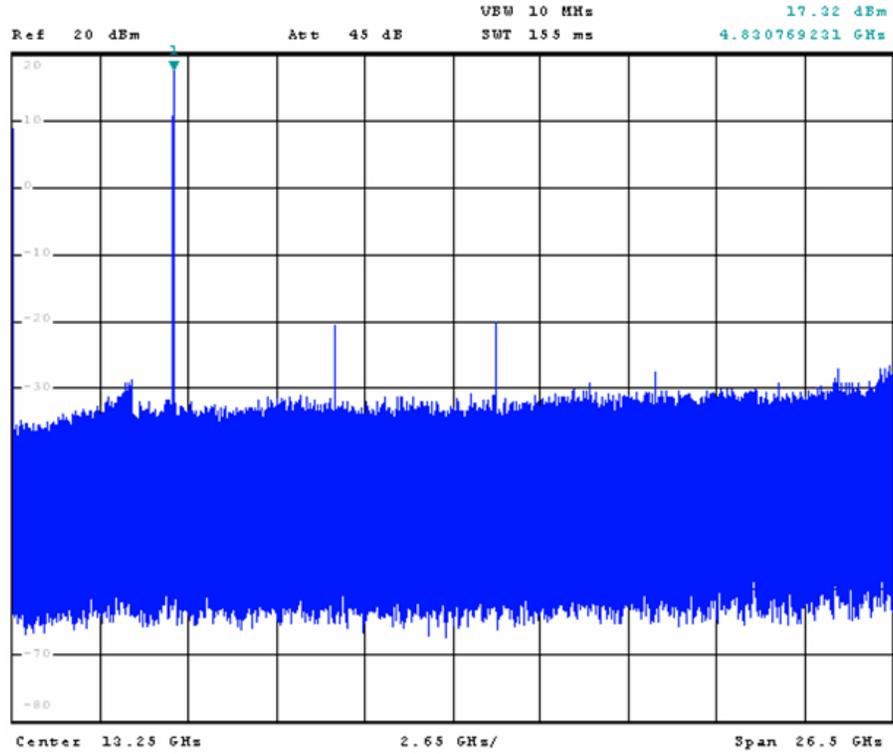


Figure 5.12: The power output spectrum at 4.8 GHz. Output power is over 1 watt and the harmonics are greater than 35 dBc through 26.5 GHz.

normally lead to degenerative feedback. We demonstrated in this section that by augmenting the other branches of the active device, regeneration is possible. At the same time, this feedback element serves as an effective conductor of heat. Using techniques discussed, a power oscillator with 21% efficiency at 1 watt and 4.8 GHz is realized. All oscillator harmonics were better than 35 dBc. A draw back to the configuration though, is limited tuning bandwidth.

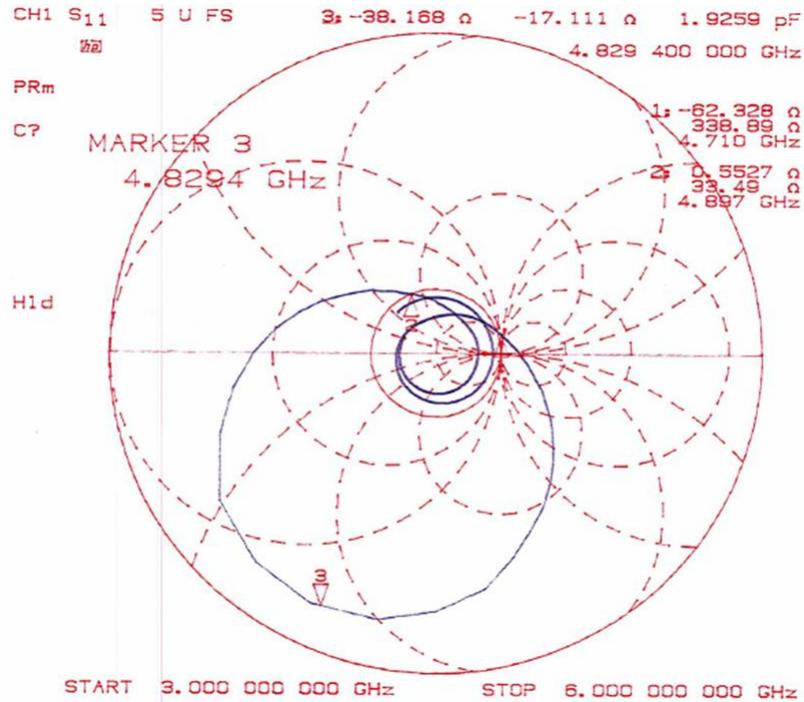


Figure 5.13: The input reflection coefficient, S_{11} of the IMFET measured at 12 V and between 200-400 mA of quiescent current. The frequency sweep is 3-6 GHz and the maximum Γ occurs at 4.8 GHz. The reflection coefficient displayed implies a nearly a -50 ohms real input impedance. Without the addition of a suitable series gate resistor, larger values of Γ would be difficult to measure.

5.1.3 Reflection coefficient shaping

Parasitics must be managed in circuit design. If correctly handled these parasitics may be beneficial and the techniques involved are an extension to the co-design methodology discussed earlier in Section 4.4.7. A so-called chip package co-design method provides for example, the high frequency impedance matching of a MESFET in a package. The bond wires in conjunction with the lead frame and package air capacitance are used to lower the Q of an external matching network. A controlled Q design results, and assists in meeting broadband frequency requirements.

In this section, we discuss an approach to successfully absorb the parasitics of the tunable resonator. Since the resonator was successfully designed to maximize unloaded Q , and tuning

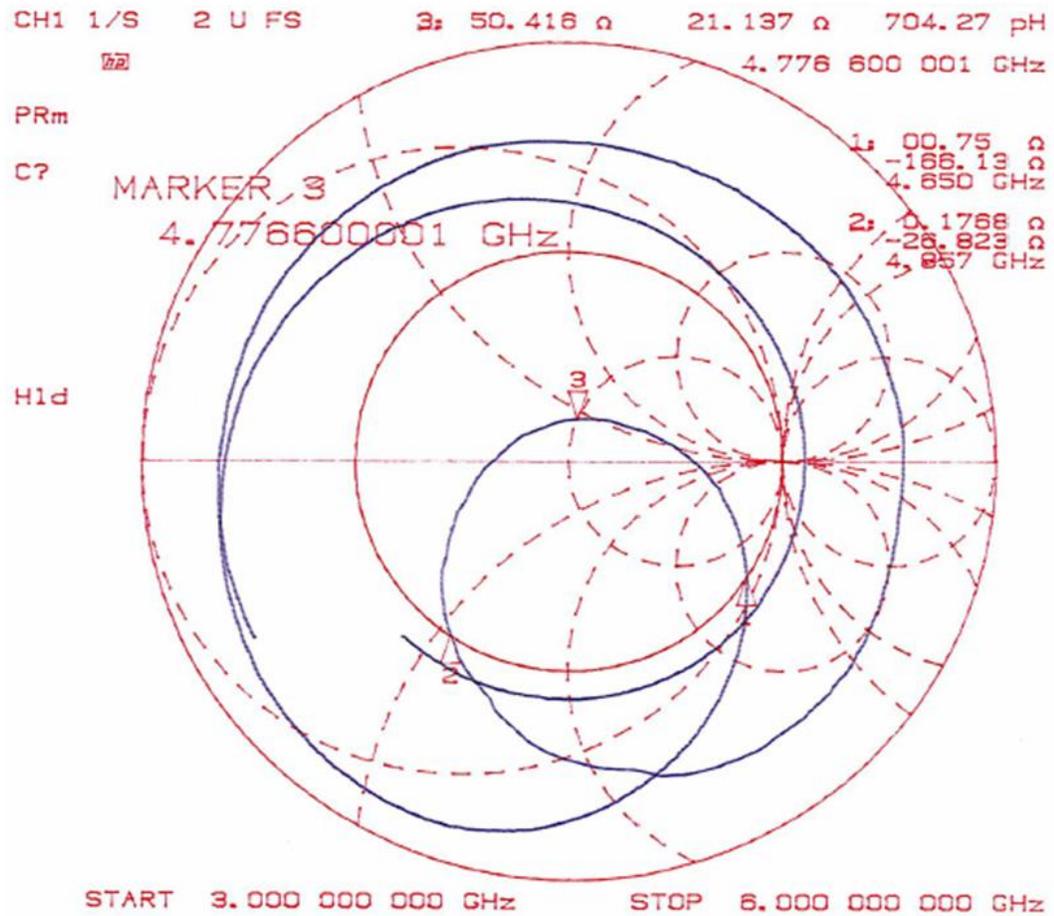


Figure 5.14: The reciprocal S_{11} of Figure 5.13. The supporting negative resistance bandwidth is just over 200 MHz, or 5% at 4.8 GHz.

range, we are reluctant to alter those characteristics to reduce or eliminate the parasitics. Instead, we approach the active device and modify the corresponding reflection coefficient. This modification method is dynamic, as it occurs automatically as the device self limits. This is the principal concept developed and the contribution of this section.

The application of resonators used in hybrid packaged oscillators are not ideal. A combination of varactor package inductance in conjunction with the supporting interconnects and pad capacitance will shift the normal resonance curve in a clockwise movement on the reflection plane. In addition, losses will significantly compress the opening of the resonator curve further,

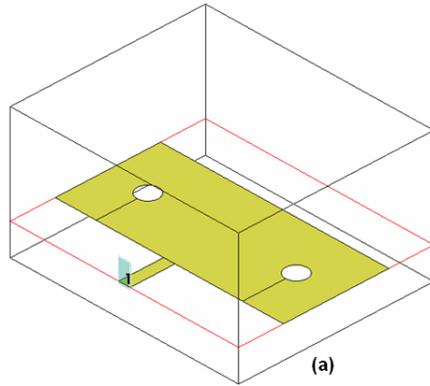


Figure 5.15: EM simulation model of the inductive plate for the IMFET (internally matched) GaAs FET. Two mounting holes for the device are required to affix the device to the plate and then to the heat sink.

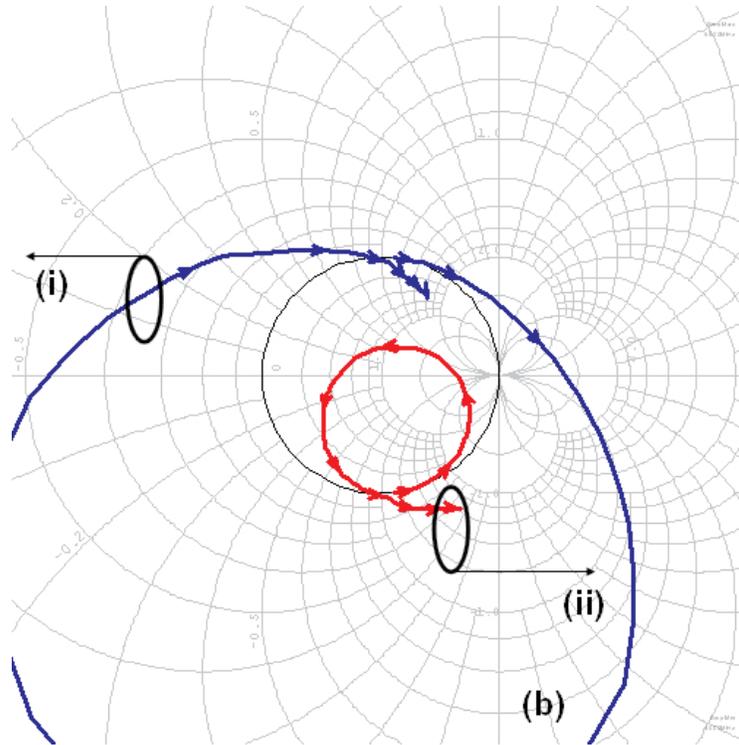


Figure 5.16: The S_{11} input of the device (i) and the reciprocal $1/S_{11}$ (ii) for the IMFET

adding difficulty to meet the condition for oscillation. A good example of this effect is shown in Figure 5.17. At point (a), a series resonator with the varactor and transmission line modeled with parasitics and losses is resonate at 6 GHz. The network demonstrates an open contour

with low series resistance and high unloaded Q . As the tuning voltage is decreased, the varactor is tuned and increases its capacitance. The combination of the increased varactor capacitance with the fixed parasitics surrounding the resonator, coupled with the decreased varactor Q , demonstrate a significant rotation and compression of the resonator curve as shown in Figure 5.17 (b). While the device reflection coefficient is considered appropriate for the interface to the resonator at point (a), as a single point of intersection between the device reflection and resonator reflection coefficient occurs, it is problematic at point (b). On the contour associated with Figure 5.17 (b), multiple intersections may occur at a single tuning voltage and therefore satisfying the condition for oscillation at multiple frequencies. Adaptation of the device Γ_{in} , or $1/\Gamma_{in}$ if the locus is placed on the same reflection plane as the resonator locus, must be modified to accommodate point (b). The incorrect intersection of the reflection coefficient pair is further illustrated in the small signal analysis shown in Figure 5.18.

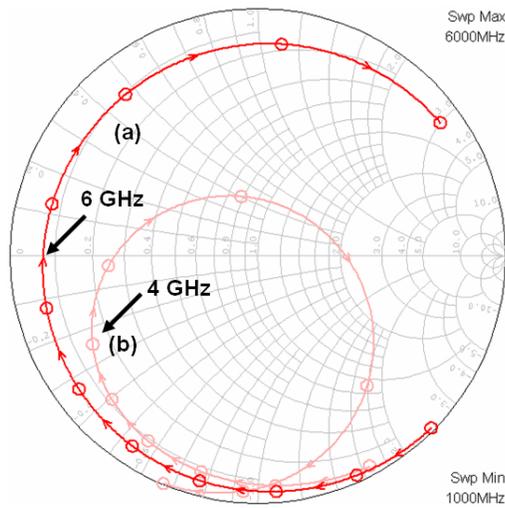


Figure 5.17: Series transmission line resonator with varactor at (a) high tuning line-V and (b) near zero volts. The varactor and line model are complete with interconnection lines and pad capacitance present.

In Figure 5.17 (a) the varactor transmission line resonator is modeled with the losses of the microstrip line and varactor Q . In addition, package parasitics including package effects of

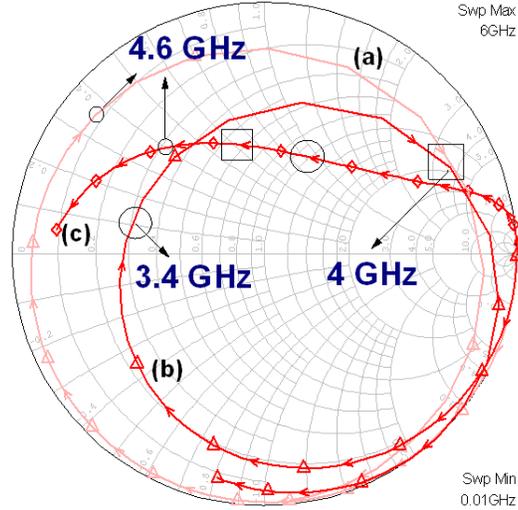


Figure 5.18: The parasitics of interconnection and component pads are added to the resonator model and overlaid with the device active input reflection coefficient. At (a) and (b) resonator, while at (c) $1/\Gamma_{in}$ of device.

inductance and interconnection of pads supporting the components are included. Additional varactors may be series stacked in an anti-series back to back configuration to improve AC breakdown voltage, however, additional parasitics are introduced. The effect of the parasitics on the resonator are seen in Figure 5.17 as the varactor capacitance is increased. In this particular instance, the parasitic is the lossy series resistance of the varactor. The additional problem of resonator parasitics and the introduction of multi-oscillation is clear in Figure 5.18 (b), the resonator locus and (c), the active device locus. In simulation, the design at high varactor tuning voltage is set to 4.6 GHz. As device large signal self limiting occurs the direction of $1/\Gamma_{in}$ seen in (c) moves along a line of constant series reactance. Correct, single point of intersection of the device locus with the resonator locus is assured. However, as the resonator is tuned to a lower operating frequency, multiple crossing points of the two loci occur. The result as self limiting of the devices occurs is violation of a single point response of the function [171]

$$\frac{\partial G_d}{\partial V_r} \frac{\partial B_o}{\partial \omega_r} - \frac{\partial B_d}{\partial V_r} \frac{\partial G_o}{\partial \omega_r} > 0 \quad (5.12)$$

see appendix on page 418 and further discussion in Section 6.1.2, where we address extensions to the techniques discussed here.

Multiple points of simultaneous oscillation occur in addition to self-mixing. The resulting spectra are shown in figure 5.19.

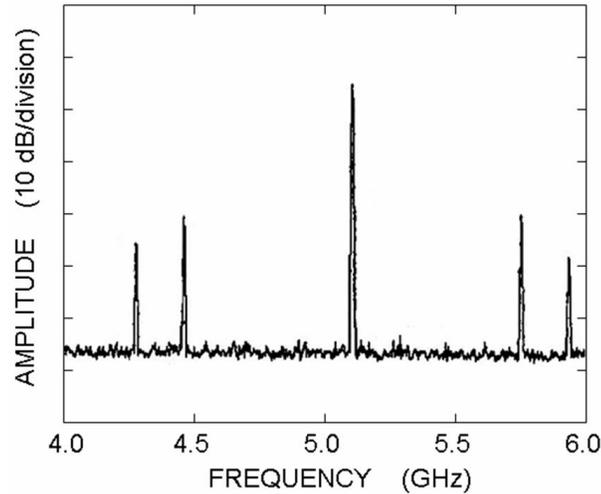


Figure 5.19: Multiple oscillations result in additional signals created about the carrier frequency due to self mixing in the active device. The origin of the multi carrier signals is satisfying the condition of oscillation at more than one frequency point.

We note that the device conductance and susceptance, G_d and B_d , are functions of the operating point while the resonator susceptance and conductance are functions of the operating frequency. This is true at a single frequency point of analysis. However, over a range of frequencies, the affects of parasitics will influence the devices, permitting G_d and B_d to both become functions of frequency. In addition, unless we prevent large RF signal voltage coupling to the varactor, the resonator terms, G_o and B_o , would be functions of the operating point. Large signal input to the varactor and resonator network is usually avoided for reasons of noise degradation. Therefore, we proceed with investigating the manner in which we may best modify the active device terms.

For stable tuning to occur at all possible frequencies, ω_r , we require (5.12) to be compliant

for all ω_r and V_r conditions. Our problem is with the resonator and if its Q reduction then the $\frac{\partial G_o}{\partial \omega_r}$. Otherwise, if its reactive parasitics, then $\frac{\partial B_o}{\partial \omega_r}$. To prevent (5.12) from being satisfied at multiple frequency points we must manipulate the locus of the either the resonator or the device reflection coefficient on the chart, in effect the product of $\frac{\partial G_d}{\partial V_r} \frac{\partial B_o}{\partial \omega_r}$. If the unloaded Q of the resonator was previously maximized and the tuning range adequate including any added parasitics, then there is little desire to redesign the resonator. Rather, we will absorb the parasitics into the resonator design. However, we have the ability of adding an element to the device to either alter the $\frac{\partial G_d}{\partial V_r}$ or $\frac{\partial B_d}{\partial V_r}$. We accomplish this as we can modify $1/\Gamma_{in}$ as the device self limiting occurs. Self limiting is an autonomous process and as such the device locus moves along lines of constant reactance or constant susceptance contours as limiting occurs altering the real component of the active device as required. Altering the active device real component of input impedance outside the oscillator system is not desired, as this adds circuit complexity and the possibility of noise degradation. However, we can manipulate the $\frac{\partial B_d}{\partial V_r}$ and affect both terms of the active device, firstly B_d and secondly G_d .

The addition of a lossless series or shunt reactance at the device input and output permits the modification of the device reflection coefficient. For example, The addition of shunt capacitance at the device input and output permits the rotation of the device $1/\Gamma_{in}$ as self limiting occurs. This rotation compensates for the movement of the resonator reflection coefficient locus induced by the parasitics. In the schematic of Figure 5.20, the capacitors added at points (a) and (b) modify the load and input reflection coefficient and subsequently the contour of $1/\Gamma_{in}$ at the onset of device self limiting. Since the self limiting process is autonomous, so is the device modification of the device. The degree of reflection coefficient compensation and adjustments are accomplished automatically by the element values of the additional reactance [96].

Monitoring the condition for meeting single frequency of oscillation over the complete tuning range requires careful calibration of the VNA. Separation of the resonator and active device again facilitates this operation, see Section 4.4.7. The use of dual channel receiver on the VNA, one channel monitoring the resonator input with the second monitoring the device input

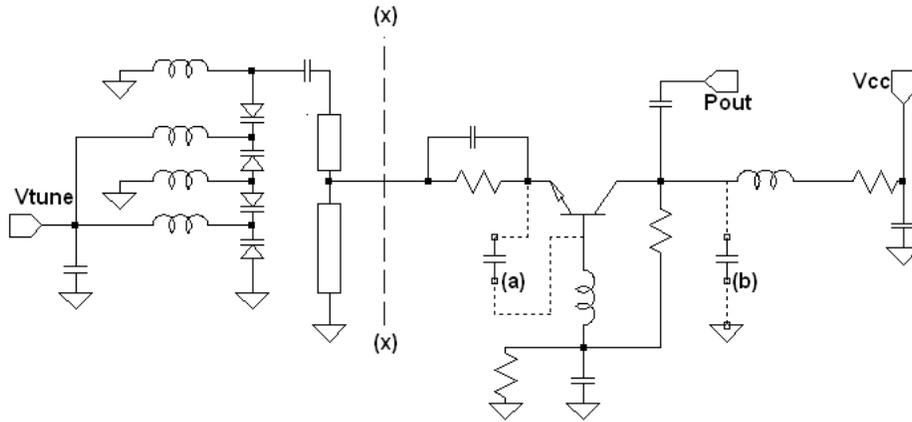


Figure 5.20: Schematic of the oscillator with both input and output capacitive terminations. Rotation of the input impedance subsequent to self limiting compensates for an improperly tuned resonator with associated parasitics.

are required. Although a small signal level is used for initial calibration of the VNA and measurements, the ability to increase RF drive level into the active device is necessary. It is precisely the increased input drive level, just prior to self limiting, with the added capacitive loading, that permits the active device input to properly terminate the resonator with associated parasitics. The oscillator is shown in Figure 5.21 and the cutaway delineated by x-x. The varactor anti-series stack is left of the resonator center and the active device to the right of the resonator. Although compensation capacitor values are initially determined through simulation, final values located at (a) and (b) in Figure 5.20 are finalized by measurement. Precise reference plane calibration is required and established, once at the resonator tap, and at a second point located at the physical pad that was tied to the resonator. The point tied to the resonator was the DC return for the active portion of the oscillator, and therefore, must be provided with an external bias tee to complete the DC return. Therefore, calibration for this port must include the bias tee.

Compensation capacitor values are between 0.5-1 pF and values larger than 1 pF cause the reflection coefficient prior to limiting to “turn in” meeting the resonator locus tangentially instead of intersecting orthogonally. Consequently, we find the phase noise is degraded as the

conversion in active device gain variation, leads to AM-PM noise conversion in the oscillator.

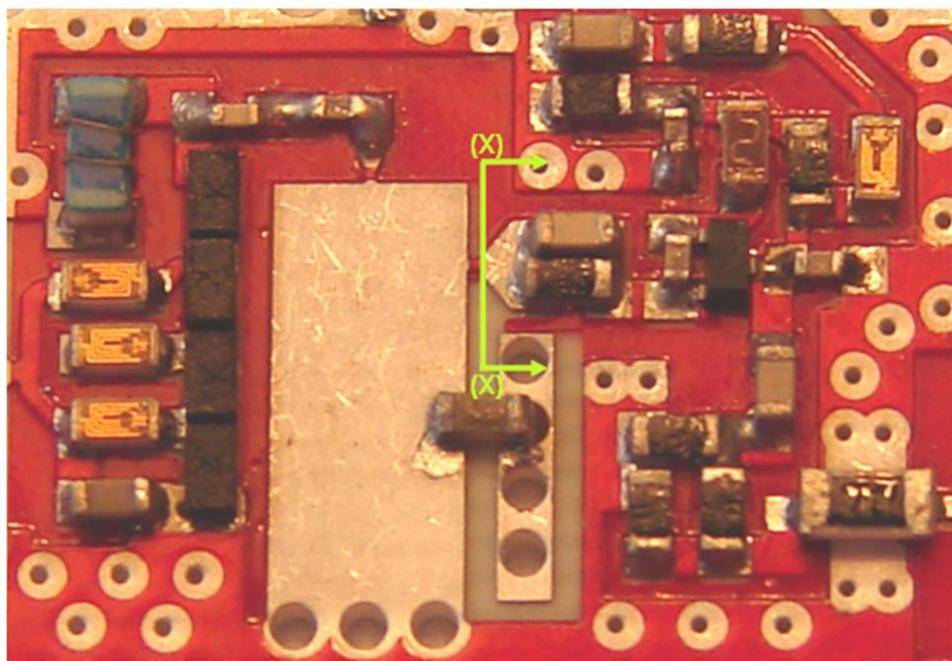


Figure 5.21: The completed hybrid oscillator which is cut away from the resonator at location x-x to validate resonator active device interface. The varactor anti-series stack-up is clearly seen to the left of the transmission line resonator.

In bench marking the design technique, we drew upon several key parameters including tuning range, efficiency and phase noise. The performance was evaluated against similar oscillators in terms of operating frequency and tuning techniques. The evaluation included both hybrid and monolithic forms and encompassed SiGe HBT's, MESFET, CMOS, GaN/SiC and GaInP/GaAs HBT's. This particular design reported a tuning range of 4.5 to 5.3 GHz and was rated highest when utilizing a figure of merit function, FOM, expressed as dBc/Hz given by

$$\text{FOM} = L(f_m) + 10 \log \left(\frac{f_m}{f_o} \right)^2 - 10 \log \left(\frac{f_{\text{BW}}^{\text{tuning}}}{f_{\text{ref}}} \right). \quad (5.13)$$

The tuning range is normalized to 1 MHz and the offset frequency, f_m , is normalized to the carrier frequency f_o . The term $L(f_m)$ is a positive value as it is the signal- to-noise ratio and not the inverse. Therefore, a positive value results and the FOM is 243. We also compared this design against a similar FOM provided by [191], which also included tuning range, however, expressed as a percentage of operating frequency. In their design a switched reactance resonator is used via a switched capacitor bank and this is analogous to the design discussed in Section 4.4.7, where the resonator was replicated for the second oscillator. In their FOM we have

$$\text{FOM} = \text{CNR}_{\text{design}} + 10 \log \left(\frac{f_m}{f_o} \right)^2 + 10 \log \left(\frac{P_{\text{DC}}}{1 \text{ mW}} \right) - 20 \log \left(\frac{\text{TR}}{10} \right). \quad (5.14)$$

where the value of TR is expressed as the percentage tuning range. To be consistent with their work, the CNR, or signal-to- noise ratio is expressed as a negative value and the tuning range is expressed as a percentage of the operating frequency. Again, bench marking the designs, using the FOM reported in [96] we have an FOM of -194 versus their -198 reported in [191]. If the work of Section 4.4.7 is used as outlined in the concept of a switched reactance resonator, than the tuning bandwidth is significantly increased. In that case, the FOM of [191] yields a FOM of -199 and therefore, further supports the idea of reactance switching of the resonator.

In this section, we introduced an approach which is a form of dynamic device modification. Dynamic in the sense that under large signal drive, the port input reflection coefficient shifts in a desirable manner to provide beneficial feedback. In this case, a rotation of the input reflection coefficient occurs, which properly terminates the resonator. A switched oscillator configuration was demonstrated in this dissertation and has a tuning bandwidth of over 1 GHz and a FOM of nearly 200.

5.1.4 Tracking phase lock loop with BST

This section extends the investigation of a PLL operating with a BST varactor based VCO. Addressed in this section is the issue of excessive noise peaking. Origins of noise peaking are partly varactor, partly control system, and partly resonator decoupling network based. Each

of these elements and the approaches to their solution are discussed. This investigation in conjunction with the material presented in Section 4.6.1 is original content. It will provide the required background material for further investigation into the circuit properties of BST when applied in a control system environment. A tracking loop in lieu of the choice of a frequency lock loop, tuned discriminator, or an AFC system is preferred, as it closely matches the operation of our PLM.

The VCO in this work operates at 2.7 GHz and was shown in Figure 4.40. The inductive portion of the resonator consists of a 60 degree shorted 30-ohm microstrip line fabricated on Roger 4350 material. The coupling elements to the active device and varactor network are also mounted on the same card. This implementation uses a single IDC BST varactor located in the upper right corner of the card. The design card provides for additional series stacked BST varactors, as well as additional tuning line bias RF choke decoupling components. This configuration will reduce the RF voltage across each varactor by a factor of N , where N is the total number of varactors in the stack, and hence improve linearity, see section 4.6.6. The average oscillator tuning gain, K_o , for $0V \ll V_{\text{tune}} \leq 30V$, with tuning voltage limited by the active loop compensator, is 1 MHz/volt. Open loop measurements to 60 V also demonstrate good linearity. Although the breakdown voltage of the BST varactor is 200 V, measurements are limited to 60 V due to on chip COG (ceramic on glass) chip capacitor voltage breakdown. The adjustment of the capacitive coupling between the varactor, transmission line, and active device, will set K_o and linearity. The incremental K_o , is evaluated by measuring a small deviation in tuning voltage about a nominal value, and is 400–500 kHz/V below a tuning voltage of 10 V. As the tune voltage approaches zero this gain is reduced. It is possible to extend the tuning voltage to lower values while maintaining K_o , however, this depends on resonator topology, the varactor index of nonlinearity, γ for junction varactor, or the power law coefficient of the junction, and the resonator interface to the active device. Nevertheless, eventually K_o must go to zero as the tuning voltage goes to zero in the BST varactor. Evidence of the reduction in tuning gain near zero volts for the VCO studied in this work is clear, see Section 4.6.8 and the

measured data in Figure 5.22 and 5.23.

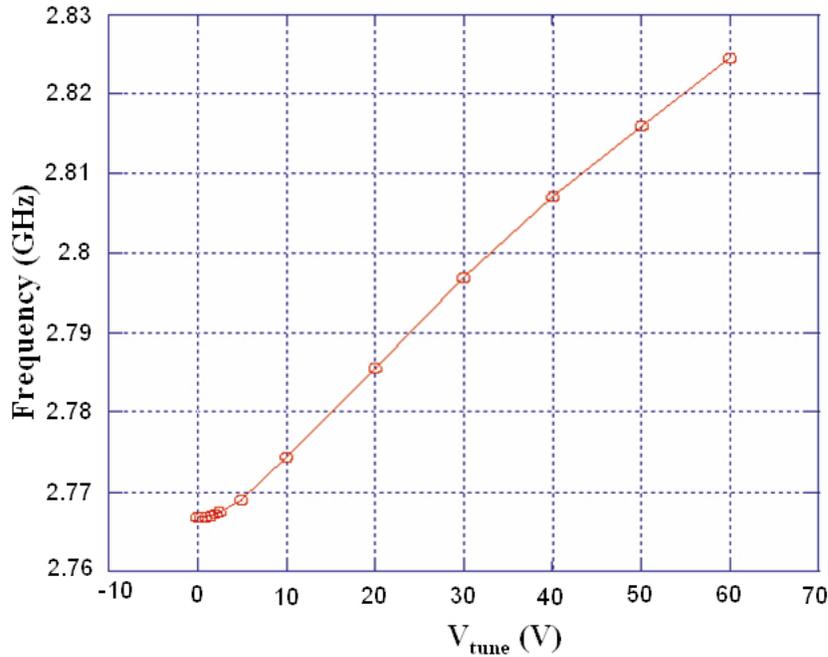


Figure 5.22: The oscillator tuning characteristic. The slope of the oscillator sensitivity drops below 10 V. Reduction in K_o not apparent until the derivative function of the tuning curve is calculated from the tuning characteristic.

The uncorrected oscillator, see center power spectrum and Figure 5.24 and corrected, left sided power spectrum of Figure 5.24 are shown. The spectrum is obtained with an over damped loop and the loop compensator adjusted accordingly for a loop bandwidth of 220 KHz. The close to carrier signal-to-noise ratio for the locked loop is therefore improved. The loop compensator is then reset for a dampening factor less than 0.7, see section 4.6.1 and 10 dB of noise peaking occurs at approximately the loop bandwidth, 220 kHz, see Figure 5.25.

Adjusting the reference frequency forces the VCO to track. The comparison frequency is 690 MHz with a multiplication of four. As the tuning line voltage decreases, the BST varactor operates on a lower sensitivity portion of the C-V curve. The VCO and loop gain drop. Because the loop transfer function is second-order, the reduction in loop gain will force the dampening

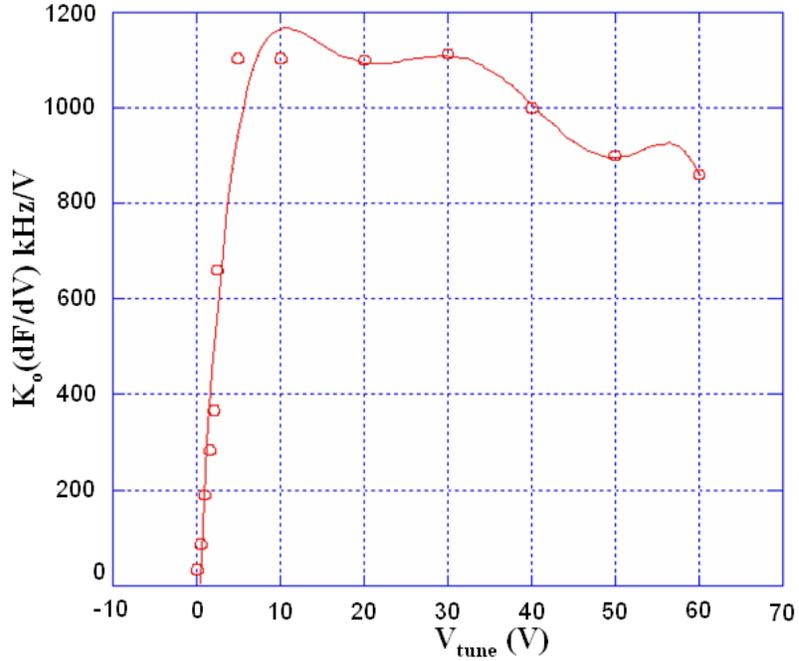


Figure 5.23: The 2.7 GHz BST varactor VCO tuning gain vs. tuning voltage. The slope in tuning gain steeply falls below 10 volts of tuning voltage and approaches zero at zero volts. At tuning values above 10 V, tuning gain approaches a constant of 1 MHz/V.

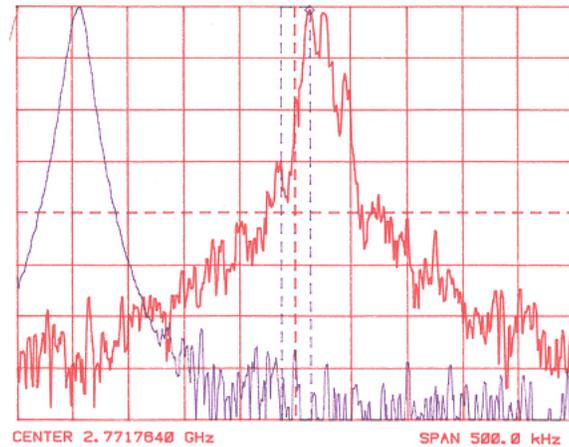


Figure 5.24: The uncorrected VCO spectrum, center and corrected left for the 2.7 GHz BST VCO. The dampening factor is approximately 1.0 and the loop $BW \sim 100$ kHz

factor to decrease. Severe reduction in loop gain will eventually allow the open loop gain to cross unity gain at a rate of 12dB/octave. The loop will be unstable as discussed in Section

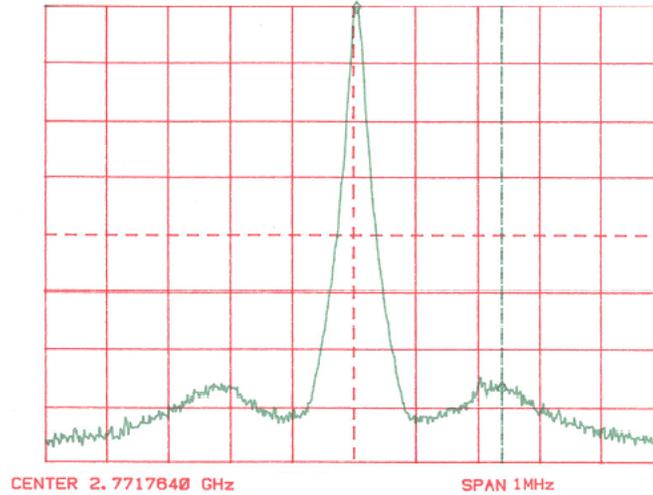


Figure 5.25: The loop compensator is adjusted so that as the VCO tuning gain drops, the loop noise peaking is clear, dampening < 0.7 . The loop bandwidth is set at 220 kHz

4.6.1. Prior to instability, additional noise peaking occurs.

An observation in this work relates to noise peaking, and the the need to avoid a resonant condition in the tuning line of the varactor network. In addition, monitoring the input reflection coefficient of the device vs. frequency is required. Prior to adding the resonator, the Γ_{in} of the device needs to follow a monotonic trajectory which is free of frequency and power discontinuities, and jumps. The load termination as discussed earlier will contribute to this profile and is monitored on a vector network analyzer. These concerns are addressed in Chapter 6.

The varactor network is normally decoupled in a manner that removes RF from the DC control line. In addition, the DC control line at the operating frequency of the oscillator must appear as an open circuit. This is essential to minimize any Q reduction of the resonator network due to the bias network. The bias network is a bias tee composed of a series inductance and a shunt capacitance. These elements are in parallel with the resonator and resonance in the bias tee will severely effect the oscillator tuning gain. The problem is readily noted in oscillators with high tuning gain, or large K_o , where slight variations in the resonator frequency response give rise to variations in the active device operating point, necessary to accommodate resonator

phase shift. When the tuning gain is large, this phase shift will occur over a small frequency span. Consider the networks involved and their equivalent form. The application of series to parallel transformation and redrawing the network equivalents highlights the issue.

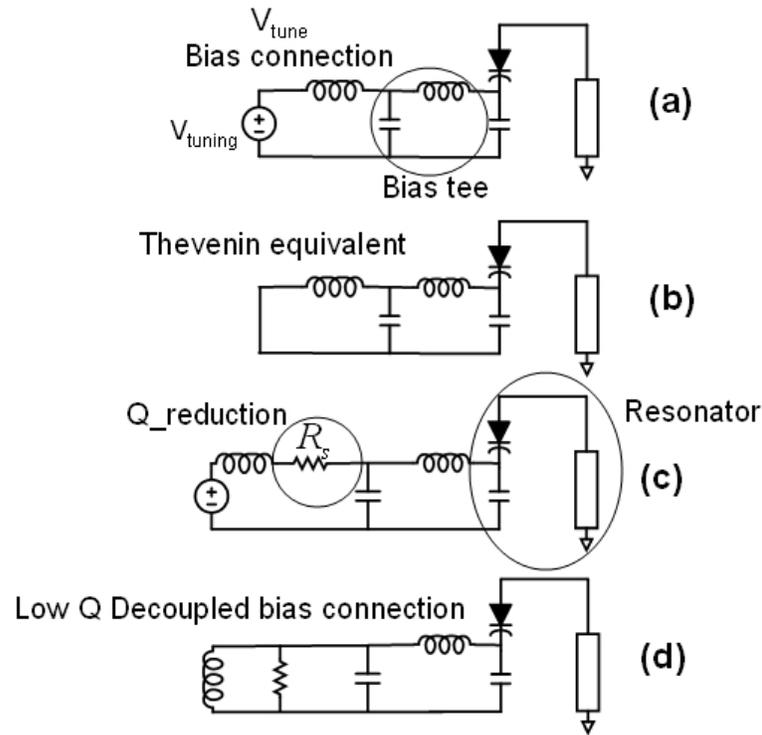


Figure 5.26: The transformation of the varactor decoupling: (a) The bias tee with small inductance connected to the tuning line voltage; (b) The Thévenin equivalent of (a) leads to a high Q in shunt with the bias tee, the result is a non-decoupled resonator; (c) and (d); The transform with a small series R_s provides a network with a reduced Q and no resonance.

In each case, the $Q^2 + 1$ method provides the equivalent network as the series resistance and decoupling capacitance are moved through the network since, $R_p = R_s(Q^2 + 1)$ and $L_p = L_s(1 + 1/Q^2)$. The resulting de- Q -ing of the network in shunt with the bias tee permits the bias tee to function properly. This eliminates a second tunable resonance which is in addition to the main one provided by the transmission line inductor with the varactor. The series resistance, R_s , on the order of 10-20 ohms, is inserted immediately before the bias tee shunt capacitance,

see Figure 5.26. Larger resistor values must be checked as noise modulation is introduced as defined by (2.34), where the Johnson noise voltage, $\overline{V_n^2(t)}$, is the open circuit applied noise voltage associated with R_s . This voltage generated by a resistor R_s is, $\overline{V_n^2(t)} = \sqrt{kTR_s\Delta f}$. The results of the problem of improper decoupling, and the reduction of the problem are shown in Figures, 5.27.

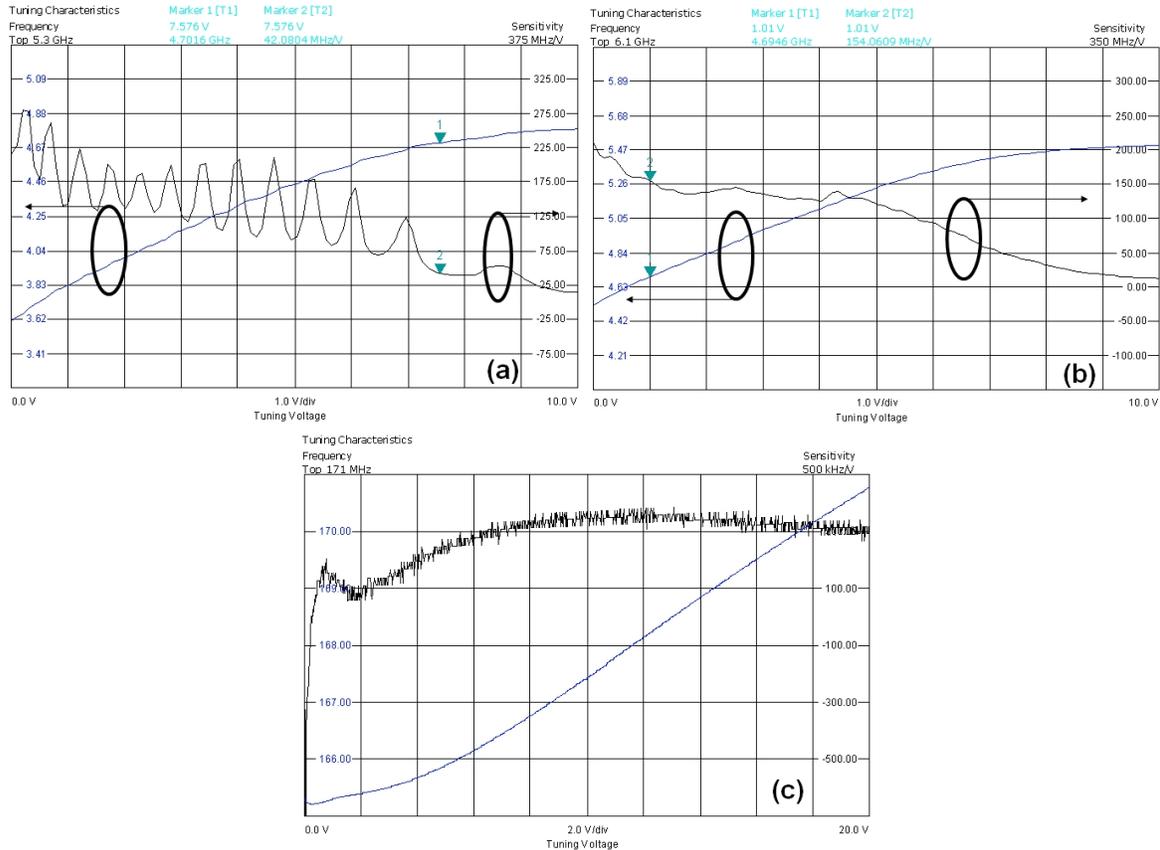


Figure 5.27: Improper tuning line decoupling results in large variations in tuning gain: (a) Significant tuning gain ripple is noted; (b) a 47 ohm series resistor is inserted in the tuning line with the varactor bias tee network significantly reducing the tuning gain ripple; (c) a 1000 point data collection for a BST varactor based VCO, shows good linear tuning characteristics above 4 volts and no tuning gain ripple.

Worthy to note, this problem is easy to miss if the measurement “aperture” or size of the

frequency step or window is large relative to the operating frequency. In effect, if only a few frequency samples are taken over the operation range of the oscillator, no problem is seen. This problem is analogous to measuring the group delay in filters. The step size in frequency in relation to the operating frequency must be small in order to resolve the phase shift with respect to frequency ($d\phi/d\omega$), not unlike a group delay measurement, otherwise the accuracy of the derivative function is compromised.

5.1.5 Mechanically Induced Modulation

Measurements are conducted on a small signal low power BST varactor based VCO. The oscillator is similar to the unit reported in [146]. A multi-axis vibration table producing sinusoidal vibrations is used and provides in excess of 6G's over a broad swept frequency range. A pair of oscillators form the PLM system. Two phase locked loops are involved. One is a reference narrow bandwidth sampling loop while the second is the multiplier loop. The PLM architecture demonstrated transients and microphonics which were suppressed better than 80 dB below the carrier power (80 dBc) while the loop is operating with a wide loop mode at approximately 1 MHz of bandwidth. In this study, PLM loop bandwidths were confined to a minimum of 1 MHz. The impact force, natural frequency, and transmission of mechanical vibrations are a function of the mechanics of the test set. These results are therefore, dependent on the mechanics of the device under test, in our case an 8x10 cm card, 1.6 mm thick, see Figure 5.28. Shown in the bottom view, the supply and RF cables must be harnessed under Kapton tape to prevent microphonics from being transmitted to the lower frequency narrower sampling frequency loop; at f_x .

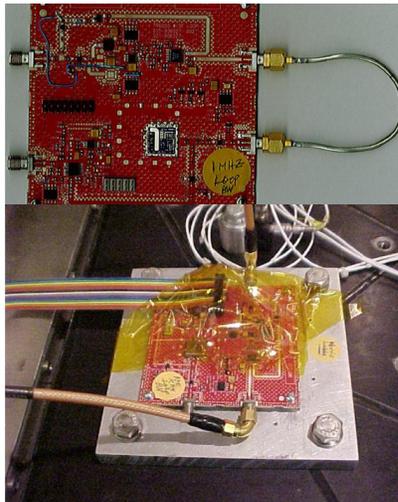


Figure 5.28: PLM test card (top) and card under test attached to shock and vibration table (bottom view).

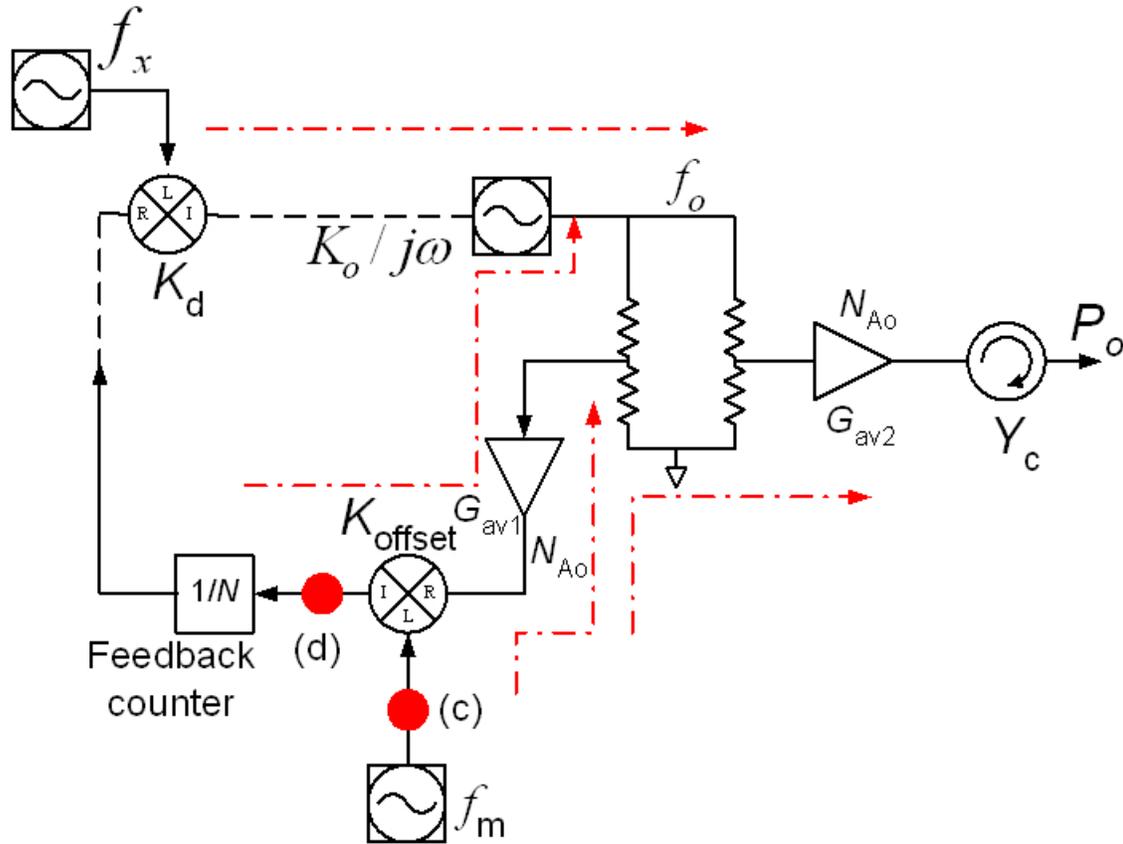


Figure 5.29: PLM signal spurious and isolation paths, highlighted. Included here are the reference source external PLL, f_x , and an offset source, f_m .

The implementation of a quadruple multiplier using a phase lock system operating at 4–6 GHz is shown in Figure 5.29. Repeated here for convenience however, with the added reference source and offset source shown, f_x and f_m respectfully. In addition is shown the offset mixer with gain, K_{offset} and associated amplifiers-buffers and an isolator, Y_c to minimize frequency pulling of the tunable oscillator with external modulation [147]. Although the multiplier loop will suppress vibration induced modulation into the loop associated with f_o , it will directly pass disturbances associated with f_x and f_m . However, these sources operate at substantially lower frequency and require less incremental movement in their frequency range. Therefore, if the mechanics and frequency and loop dynamics work well together, it is possible to suppress

these particular sources of mechanical modulation to an acceptable level.

The spurious content under vibration and operation is demonstrated in the spectrum photograph insets in figure 5.30. Loop bandwidths are set at (a) open loop, (b) 100 kHz, and (c) 1 MHz. The immediate suppression of the vibration spurious are evident in Figure 5.30(c). In this test, a secondary loop is also on the same card serving as the reference or source frequency of f_x for the wider loop. Dependent on the required resolution and architecture of the reference loop, this loop could be directly subjected to the microphonic disturbance we are highlighting in the wideloop. Fortunately, the operating frequency is lower and the required tunability less. Therefore, the sensitivity to mechanical inputs and the translation to an electrical disturbances is reduced accordingly.

In these sections we treated the PLM under the influence of noise and potential introduction of spurious modulations. Since the locked oscillator under investigation is a power oscillator, there are a number of unique consequences brought about by the incorporation of a high power device. Mechanically induced modulation is addressed. This is a topic which is acute to the varactor used in the tuning of the oscillator source and investigation of the properties of BST in isolation under mechanical stress is warranted [151].

Although not treated in detail up to this point, it is important to mention some observations when dealing with oscillator microphonics, particularly in the case of the power oscillator where some form of forced air versus convection cooling may be required, see Figure 5.31. Again, influential control by the loop, if sufficiently wide should provide the necessary corrections to suppress vibration and thermally induced fluctuations of the oscillator. In our measurements, we see at a minimum 15 dB carrier-to-noise degradation of phase noise at 10 kHz offset from the carrier at 6 GHz. For the cases studied in our work, the integrated phase jitter was found to degrade from 1.2 pS at 6 GHz to over 40 pS with the presence of a Rotortron fan mounted 3 inches above the oscillator.

At offset frequencies below 10 kHz, as much as 30 dB degradation is noted and therefore, sufficient loop gain must be present to insure suppression of this noise. Finally, as a topic for

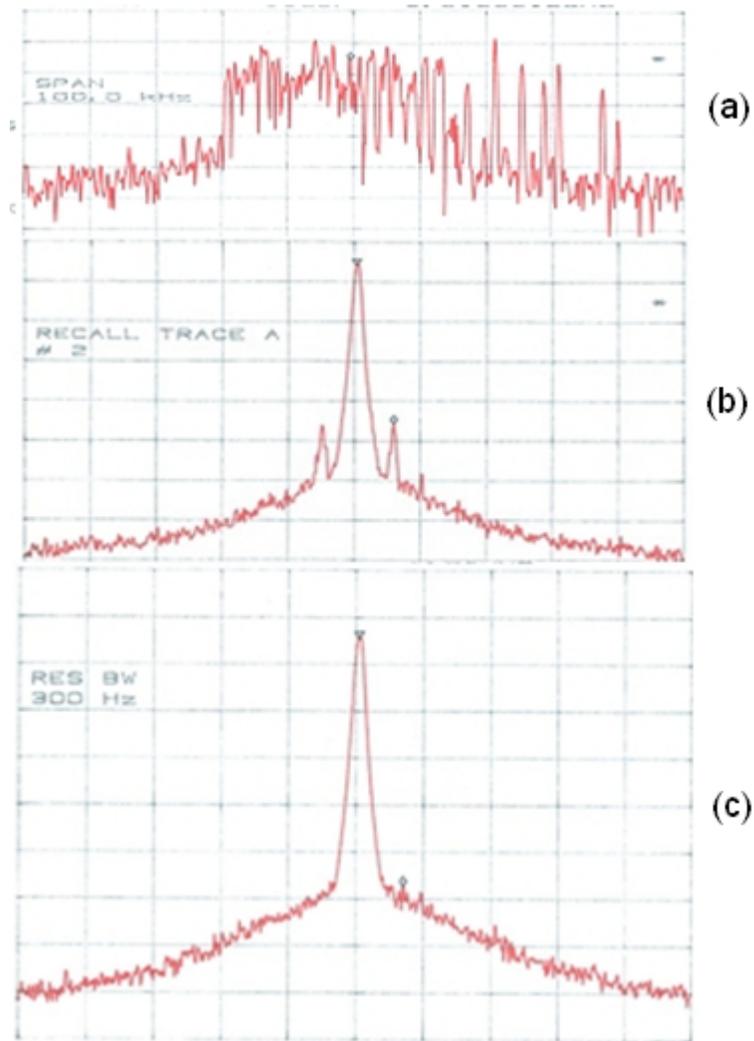


Figure 5.30: The 4 GHz PLM under shock and vibration at 6 G's: (a) open loop; (b) PLM loop set to 100 kHz bandwidth; (c) PLM loop set to 1 MHz bandwidth. All measurements are with horizontal divisions at 10 kHz/division and vertical at 10 dB/division.

future work, microphonic susceptibility of the BST varactor warrants investigation. In this study, there was no attempt to isolate the cause of microphonics. For example, isolation of the active device from resonator or the BST varactor itself from the resonator were not pursued.

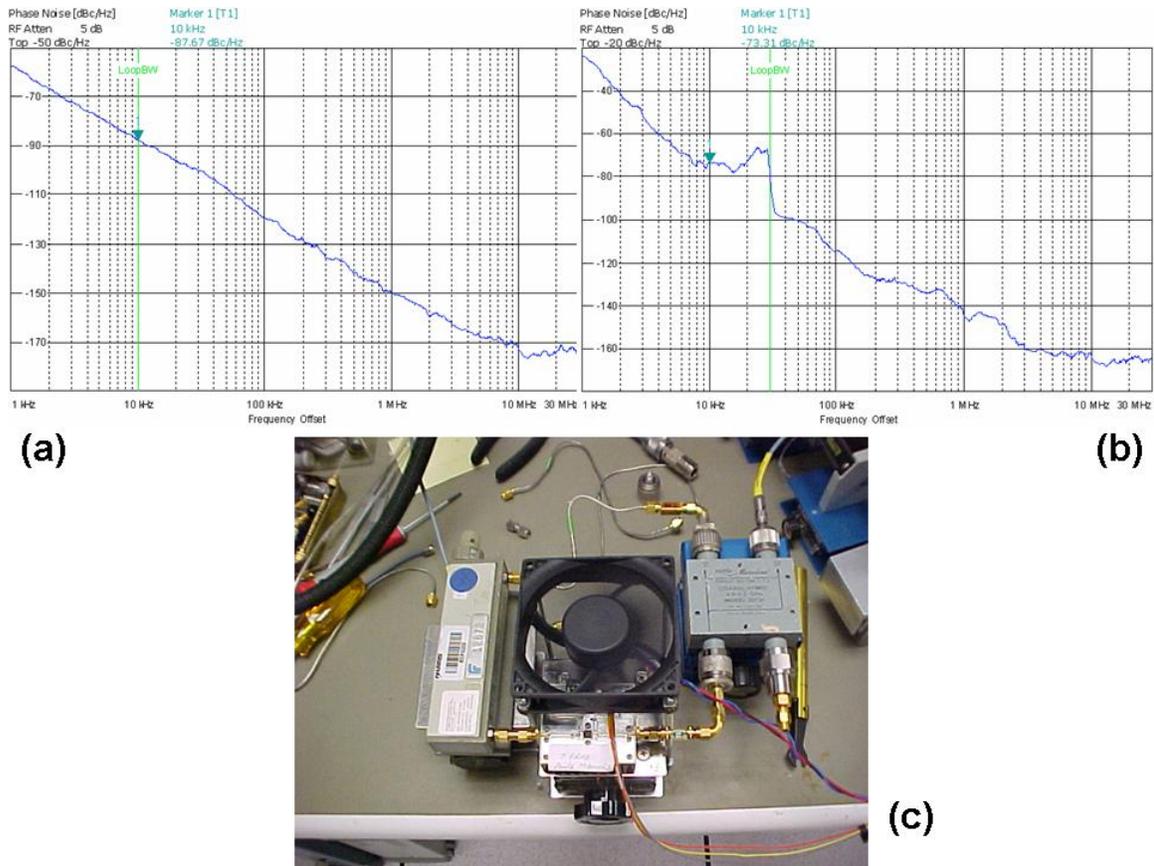


Figure 5.31: Oscillator microphonics, in this case a 6 GHz power oscillator with FAN cooling in (c) with single sided phase noise shown in (a) FAN off and (b) FAN on.

5.2 Summary of Results

The implementation of both small and large signal oscillators is addressed via two design techniques. In this chapter, emphasis is on the one port negative resistance approach. Very simple and yet highly efficient power oscillators are presented based on HFETs which are either internally matched or not. The key idea, the ability of heat transfer from the power oscillator package to the heat sink via a branch that also serves to introduce positive feedback. Although the design implementation is simple, unfortunately, the technique has limited tuning bandwidth, about 5% at 6 GHz. For power oscillator applications, we will see that the two port feedback technique is alternatively a better approach. While for lower power sources, the

negative resistance design if interfaced with a properly compensated active device operates over a wide bandwidth with high signal-to-noise capability. Compensation of either the active device or resonator is addressed through a co-design approach and EM-HB are further stressed here.

Operation of the oscillator as a VCO with a BST varactor is presented. The phase locking characteristics are unique and issues of oscillator push-away and latch up are addressed. In the implementation of the BST based VCOs in phase lock systems, additional watchdog circuitry needs consideration. Not unlike the junction varactor, however for different reasons, tuning voltages near zero volts applied to the BST varactor should be avoided in a phase lock system.

Chapter 6

Case studies, Power Oscillators and System Optimization

Four case studies are detailed, adding supplemental material to our prior discussions. A review of the issues addressed in realizing the negative reflection coefficient power oscillator are discussed. New approaches to a mapping study are provided to the configurations presented in Chapter 5. The constrained operating bandwidth of the common source power oscillator configuration is addressed, however with differing feedback topologies and termination networks. This discussion leads us into exploring an alternative arrangements based on common source, Class A, power amplifiers configured with external feedback. This class of oscillators prove to be highly efficient with excellent signal-to-noise characteristics, despite the fact that their synthesis is rooted first in a Class A approach to design. Their performance is bench marked against prior work and rate highest among other GaN power oscillator implementations.

First, a pair of power oscillators are developed at operating frequencies of 2 and 5 GHz. The designs utilize a Silicon GaN HFET for the active device. These oscillators are first based on a power amplifier design with the addition of an external phase shift, delay network, and terminating load impedance in order to control frequency and amplitude of the oscillation. The realization of these power-feedback oscillators permits us to contrast the design technique of

the power amplifier configured as a two port feedback oscillator with the negative $-R$ (NR), reflection amplifier type oscillator.

Additional details will also be provided on the topic of maximizing RF system cascaded dynamic range. A detailed set of case studies are provided. The first, is the bandpass preselector briefly covered in Section 4.3.1. The second, discusses a 15 GHz transmitter cascade using an up conversion mixer and RF power amplifier. The purpose of these investigations and forthcoming sections is to add more depth to previous coverage of these subjects, and draw upon experimental laboratory results and problems identified along with their solutions which occurred as part of this work.

6.1 Highlights of the case studies

These case studies focus on oscillator synthesis for optimized efficiency and output power. Also we highlight the improved phase noise obtained as compared to our earlier prior work utilizing a Si-GaN HFET. These designs are performance bench marked against both earlier and current design work of similar power oscillators where the primary goals are operating frequency, efficiency, power output, and tunability. These examples help demonstrate the viability of the design approaches developed in this dissertation.

In addition, we study the case of maximizing the system dynamic range of a down-converter through the contribution method previously outlined in Section 4.3.1. Measurements of the system dynamic range for an identical cascade preselector architecture is discussed. The test vehicle utilizes a set of commercial filters and MMIC's, with the ability to provide modification of their parameters in accordance with the contribution method discussed previously. A 3 dB improvement in dynamic range with no additional expenditure in operating power is accomplished through a straight forward modification of each of the stage parameters.

6.1.1 One port negative reflection coefficient vs. PA closed loop power oscillator

In Section 5.1.1, and further detailed in the appendix on page 418, we discuss the relationship and contrast oscillators realized via the generation of negative resistance with those which rely on an external feedback path. The negative resistance oscillator is realized through proper selection of an active device and its terminations. This is contrasted to that of the addition of a feedback network to an otherwise stable, non-generative, active two port network.

The reflection type oscillator, either negative resistance or negative conductance (NG), and the feedback two port oscillator have two associated sub-circuits. In the case of the reflection oscillator, the sub circuits consist of the negative resistance generator and the resonator. While in the feedback oscillator, the two sub circuit components are the amplifier and the feedback loop. Although not strictly necessary, we will distinguish the difference between the negative $-G$ (shunt form) and negative $-R$ (series form) negative resistance generator in so far as the resonator types should be complimentary to the device as the device self-limits. In the case of the NR generator a series resonant resonator is desired while in the case of the negative conductance $-G$, a parallel resonate resonator is preferred. The primary reason for these choices of resonator topologies is to preserve tunability and minimize the potential of multi-oscillations. Each respective oscillator demonstrates self-limiting reflection coefficient trajectories which either follow contours of constant reactance, (type-NR), or constant susceptance, negative $-G$ (NG). The discussion of multi-oscillation is focused on in Section 5.1.3 and further discussion is presented in Section 6.1.2.

In either case, both oscillator types require careful control of the circuit parasitics of the resonator network in order to maintain stable tuning and power output over a specified tuning range. Consequently, the characteristics of the BST varactor with DC and impressed RF voltage as well as the topology of the resonator network are key to proper oscillator operation.

For the NG network, a combination of a single element one port feedback components (L or C) with the active network appropriately terminated is sought. The reflection coefficient

(or inverse reflection coefficient) measured versus frequency must interface with the selected resonator in a manner which insures that the provision

$$\Gamma_{\text{res}}\Gamma_{\text{d}} \geq 1 \quad (6.1)$$

is satisfied, where Γ_{res} is the resonator and Γ_{d} is the active device reflection coefficient. Care must be exercised to not loosely misinterpret this definition. The angle of the reflection coefficient associated with the active device and the angle associated with the passive network, resonator, must be carefully considered. In addition, it should be understood, that in case of the negative resistance associated with the reflection oscillator, the termination provided by the resonator is in series form, while in the negative conductance oscillator it is in parallel form. Therefore, perhaps it is easier to envision these requirements by conversion from the reflection plane to the equivalent impedance and admittance plane for the two oscillator types. In that case we have

$$-[Z_{\text{d}} + Z_{\text{r}}] \geq Z_{\text{d}} + Z_{\text{r}} \quad (6.2)$$

and

$$-[G_{\text{r}} + G_{\text{d}}] \geq G_{\text{r}} + G_{\text{d}}. \quad (6.3)$$

When converted to an equivalent set of impedances, the net result of adding the impedances must be less than unity. When converted to a set of conductances, the sum must also be less than unity. The magnitude of the resonator reflection coefficient is bounded to a maximum value of unity in all cases. In the case of a series oscillator, the device input reflection coefficient angle is nearest the short circuit side of the reflection plane. In the case of the shunt oscillator, the angle is nearest the open circuit side of the reflection plane. These situations are the preferred so as to meet the requirements set out by (6.2) and (6.3). Attention usually turns to satisfying the active network portion of the design for a Γ_{d} larger than unity. The resonator section is readily altered within a range of inductive and capacitive reactance values and topologies,

assuming parasitics of the resonator are not dominant. However, the device has a maximum g_m at start-up, and a required minimum g_m is needed to satisfy the condition to support oscillation. The Γ_d value attained is a function of the embedding network, for example a series capacitor in the emitter or source lead or a series inductor in series with the base or gate lead for the respective oscillator types. These device modifications, will alter the device input reflection coefficient appropriately. In addition, terminations at other ports will further modify this value as the input reflection coefficient is given by,

$$\Gamma_{in} = S_{11d} + \frac{S_{12d}S_{21d}\Gamma_t}{1 - S_{22d}\Gamma_t} \quad (6.4)$$

where Γ_t is the reflection coefficient of the termination and $S_{ij d}$ are the two-port S-parameters of the active device. In the work which follows, we will reference Γ_d as Γ_{in} of the active device. The small signal device S-parameters are represented without the addition of feedback and are those only of the intrinsic device. Depending on the active device construction and composition, it is possible that the intrinsic device is sufficient to provide oscillation without additional feedback or component embedment. This would represent a potentially broader tuning range oscillator when capacitive tuning is used as no additional feedback capacitance is required. Depending on the configuration of the resonator, the additional capacitance further reduces varactor tuning ability.

Therefore, to ensure that oscillations build initially, the circuit is designed such that the product of $\Gamma_{in}\Gamma_{res} > 1$. This requirement is predicated upon the prior clarifications of feedback type and location, that is either the source or gate terminal, and is based on the small signal S-parameters. A particularly desirable value of the termination reflection coefficient is one in which $\frac{\partial}{\partial \omega} (\Gamma_{in}\Gamma_{res})$ is maximized. This guarantees oscillator startup. However, to realize a wider stable tuning range, the termination port impedance in conjunction with the device must provide an input reflection coefficient versus frequency which meets two requirements. First, it must readily support the appropriate resonator reflection coefficient versus frequency, thus satisfying (6.2) or (6.3) and second, it must be single valued at each frequency tuning point.

These topics are addressed in more detail in the appendix on page 418 and Section 6.1.2.

A disadvantage of series feedback in a power oscillator is the inability to remove heat from the device. Since the source terminal or the emitter periphery is the main channel for heat removal, providing a low thermal path is desired, see section 5.1.1. Therefore, shunt feedback is also investigated permitting the source to be DC grounded. Distinguishing these two oscillator network types is shown in Figure 6.2. Highlighting the various feedback configurations to realize the reflection oscillator is developed Figure 6.1.

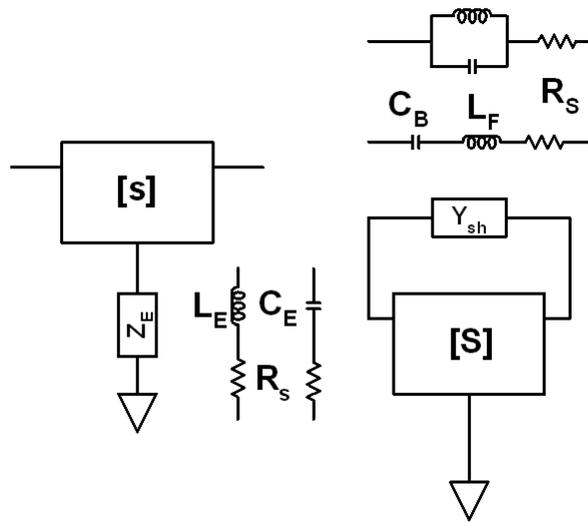


Figure 6.1: An arrangement of series or shunt feedback topologies are selected, based on the terminations chosen, see Figure 6.2. The combination of feedback and termination networks sets the magnitude and angular range of the active device input reflection coefficient.

While adding series feedback to a power GaN HFET, and providing a low thermal resistance is possible, the tuning range is found to be confined, see Section 5.1.1. The operating bandwidth is limited. The question of using shunt admittance and a combination of terminating reflection coefficients are addressed in this section. This approach returns the source or emitter terminal through a low RF and thermal impedance, ideally zero ohm for both the AC and thermal resistance. A combination of mapping the load termination along with the addition of shunt

admittance to the active device are presented as a possible solution. The question is therefore, given a termination bounded on the unit reflection plane, is there an appropriate shunt admittance, which when added to the active device provides a favorable input reflection coefficient for the resonator, and satisfies the condition of oscillation? To address this we consider a small signal analysis first.

The device S-parameter matrix is converted to Y-parameters. The identical row-column terms of the device Y-matrix and feedback matrix are added and then the total matrix converted back to S. The modified S-parameters then mapped with the termination as a variable using (6.4). Restricting ourselves to only shunt feedback and permitting the datum terminal (source) to be grounded, we investigate a power Si-GaN HFET for meeting the conditions to support stable oscillation. The shunt feedback topology selected, shown as Y_{sh} in Figure 6.2 is a series R-L-C network and to provides a DC open circuit between gate and drain terminals. Studies are performed at 2.4 and 5 GHz with a 2 mm device packaged in a PSOP2 package and surface mounted on a printed card with a heat sink attached. For the HFET studied, a Nitronex Corporation NPTB00004 [185], series R-C feedback is preferred. This is based on investigating the range of input reflection coefficients created, both magnitude and angle, as a function of the termination impedance. This is readily apparent after rewriting (6.4) and applying the feedback network and sweeping the load reflection coefficient angle. We constrained the magnitude of Γ_{in} to 1.5, which is a reasonable value to meet startup conditions. Then we considered the angle of the load termination $|\Gamma_t|$ as the value of its magnitude is bounded to unity. Finally, we seek the angular range of Γ_{in} and we ask the question, is this input angle located near the open circuit side or the short circuit side of the reflection plane?

From (6.4) we have,

$$\Gamma_t = \frac{S_{11}^f - \Gamma_{in}}{S_{11}^f S_{22}^f - S_{12}^f S_{21}^f - \Gamma_{in} S_{22}^f}, \quad (6.5)$$

where the device S-parameters are noted as modified values due to the addition of shunt feedback. Reference to Figure 6.1 and Figure 6.2 are helpful. If the feedback is inductive, a plot of the criteria previously established gives Figure 6.3, where the inductance of the gate-drain is

0.82 nH and the the desired input reflection coefficient is 1.5. No value of termination less than 0.95, nearly unity, will meet the requirements for an input reflection coefficient magnitude of 1.5 for all ranges of input phase, $-180^\circ \leq \alpha \leq +180^\circ$, using the desired feedback inductance. In addition, no range of feedback inductance would provide for the required input reflection coefficient requirements. Therefore, the use of R-C feedback, either R//C, where // implies a parallel connection, or a series R-C topology is preferred. The series arrangement also provides a DC block which is required if inductive feedback is needed. However, the parallel form of R//C feedback is possible particularly if incorporated into the biasing of the active device. Finally, some series inductance is already present without any effort, as parasitic L is already present in the form of interconnecting trace lines and pads, requiring modeling and the addition into simulation and design. Hence, we consider the case of a series R-C network with two different C-feedback values. We will first evaluate the requirements at a single frequency. Then subsequent analysis requires a swept frequency response followed by a large signal analysis in order to evaluate the self limiting characteristics of $|\Gamma_{in}|$ with varying input drive level.

The cases for 0.5 pF and 2.0 pF are shown in Figure 6.4 and 6.5. These graphs detail the values of input and output reflection coefficients based on the following settings for the analysis listed in 6.6.

$$\Gamma_{in} \sim 1.5 \tag{6.6}$$

$$\Gamma_t \leq 1$$

$$-180^\circ \leq \alpha \leq +180^\circ$$

$$0.5 \text{ pF} \leq C_{FB} \leq 2.0 \text{ pF}$$

$$V_{dd} = 28 \text{ V}, I_{ds} = 100 \text{ mA}$$

The resulting rectilinear plots may be projected onto the Smith chart at a single frequency. In this case the contours are circles on the reflection plane, whose center location and radius are

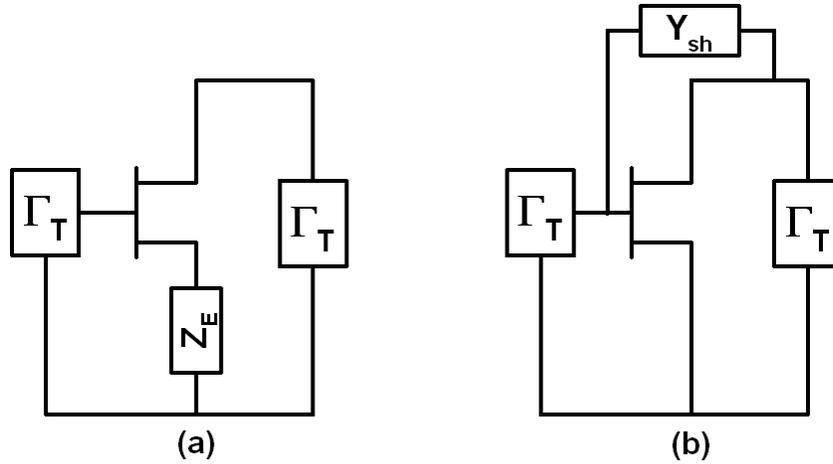


Figure 6.2: The series feedback oscillator using: (a) Z_E with terminations, Γ_T , creates difficulty in achieving an adequate thermal pathway for the device; (b) while the shunt feedback oscillator, using Y_{sh} , thermal grounding of the source (emitter) contact is directly accessible.

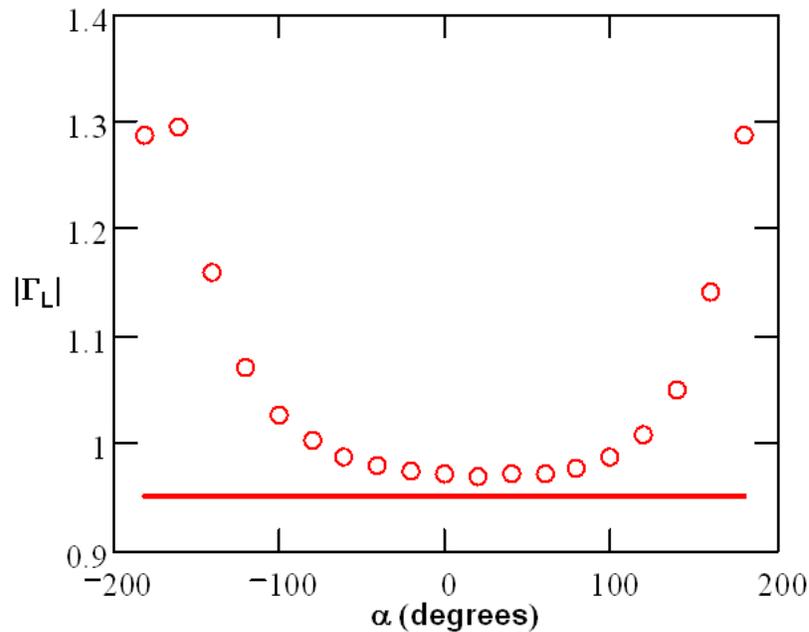


Figure 6.3: A plot of the required value for the termination $|\Gamma_L|$ vs. the input angle, α , of Γ_{in} . For this case, L_F is .82 nH and the $|\Gamma_{in}|$ is constrained to 1.5. The demarcation line is $|\Gamma_L| = 0.95$

a function of the feedback capacitance, termination magnitude, and angle. However, obtaining a clear perspective and understanding of the network operation requires a family of these

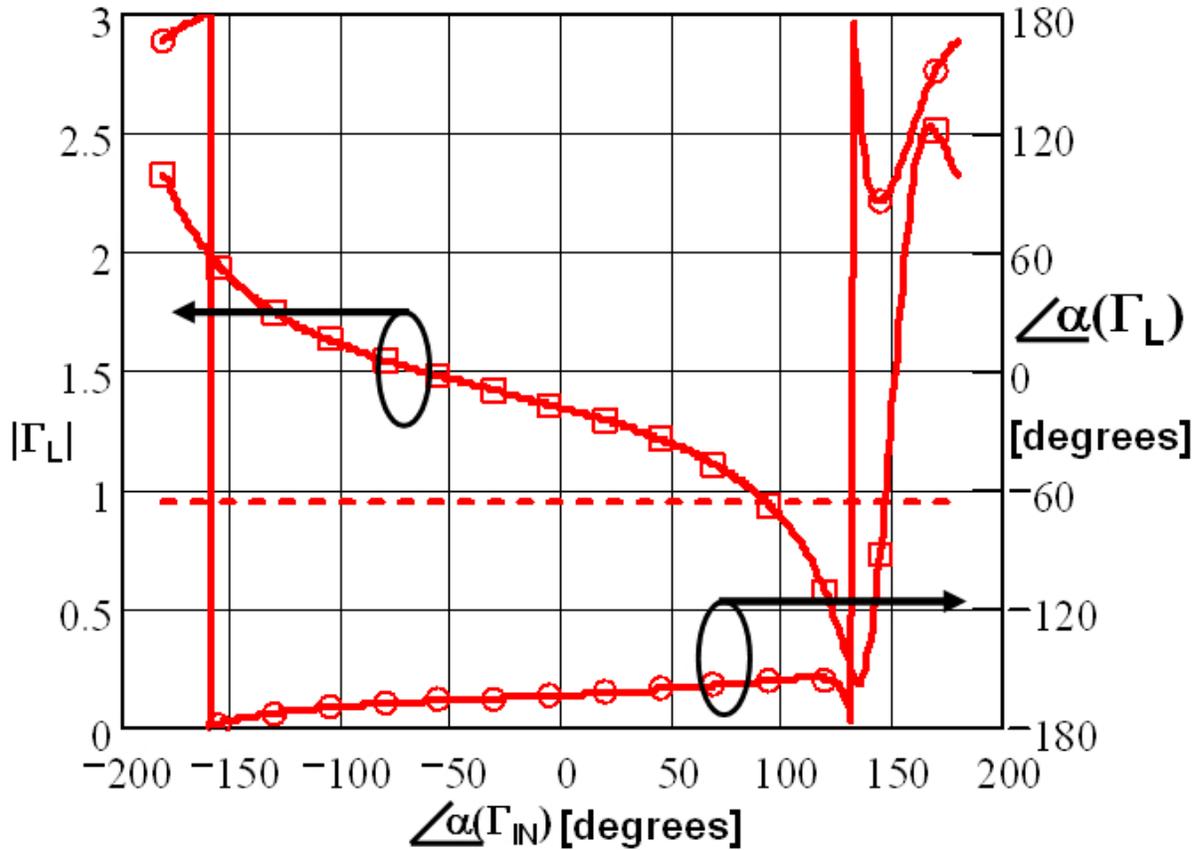


Figure 6.4: A graphic of the angle of Γ_{in} in degrees versus $|\Gamma_L|$ and argument of Γ_L . Shunt feedback $C_{FB} = 0.5\text{pF}$, magnitude of Γ_{in} restricted to 1.5

contours which are a function of frequency and would be overlaid. Such an arrangement of data eventually becomes cluttered and difficult to interpret. Therefore, we elect the rectilinear view.

In Figure 6.4, a shunt feedback capacitance of 0.5 pF is chosen. The termination reflection coefficient for this condition is less than unity over a small angular region between 100° and 150° . This implies the resonator reflection coefficient must be net capacitive and favors the short circuit side of the reflection plane. The load reflection coefficient angle is free to choose, and a choice of this parameter would be based on the ability to transfer maximum power from the oscillator system to an external load. Outside of this region, the termination reflection

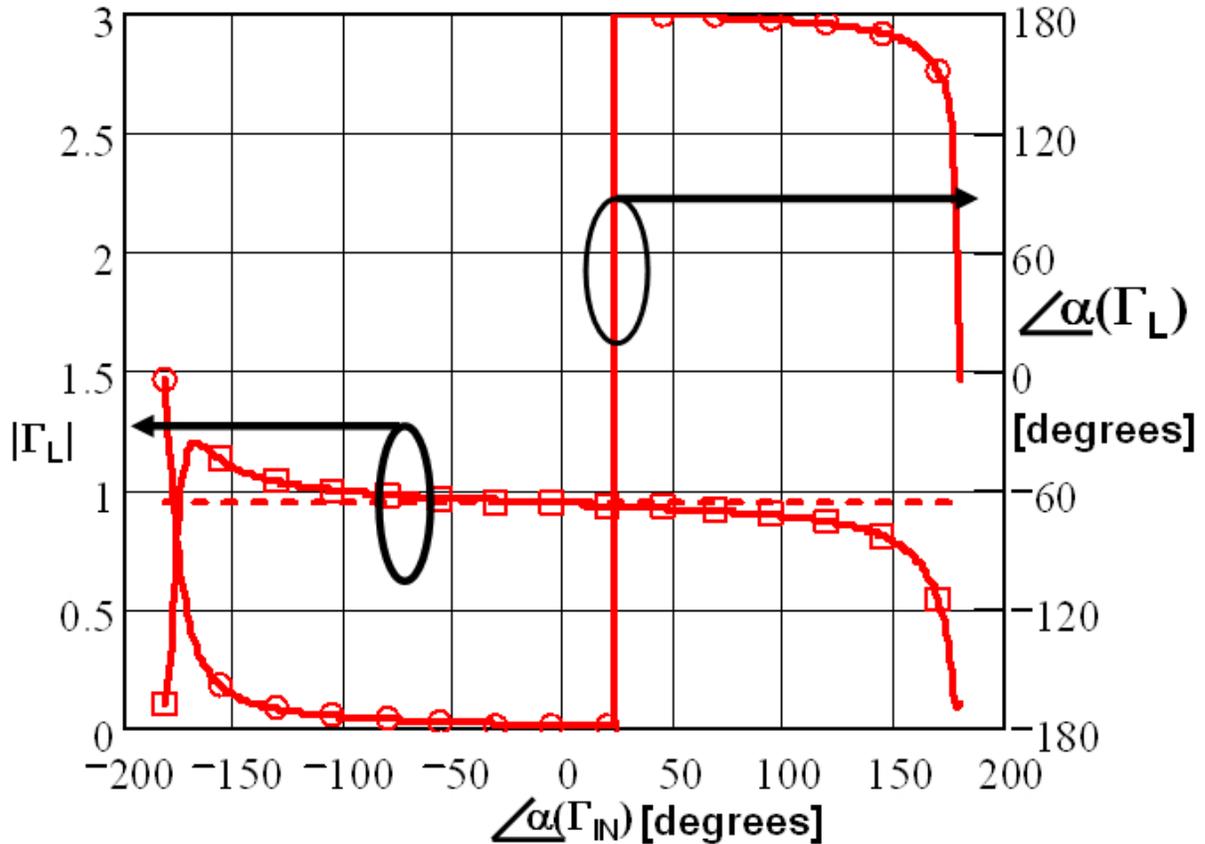


Figure 6.5: A graphic of the angle of Γ_{in} in degrees versus $|\Gamma_L|$ and argument of Γ_L . Shunt feedback $C_{FB} = 2.0\text{pF}$, magnitude of Γ_{in} restricted to 1.5

coefficient quickly increases to near unity and no possibility exists for providing an input angle near the open side of the chart with 0.5 pF of feedback capacitance. Therefore, this resonator topology and active device feedback configuration will not accommodate a parallel tuned topology. A series resonator topology is preferred. As the feedback capacitance increases to 2 pF, see Figure 6.5, the value of the magnitude of the required termination reflection coefficient increases to nearly unity over most of the angular region of Γ_{in} . In addition, the magnitude specified for Γ_{in} of 1.5, is achieved. Over a limited region, between 160° and 180°, the load reflection coefficient required to meet the Γ_{in} requirements decreases significantly below unity, and both inductive and capacitive input angles of Γ_{in} are accommodated. However, the required

angular termination of the load is not very selective, we note the steep slope at nearly 30° of input angle, highlighted in Figure 6.5, whereby the angular value of the termination may be selected anywhere over the $\pm 180^\circ$ range. Consequently, a load termination would be selected to maximize power output or load efficiency.

6.1.2 Addressing a reflection coefficient problem

These graphs represent a single frequency calculation at 4 GHz. If the oscillator is to be tuned, 4–6 GHz, then additional plots at 4.5, 5, 5.5 and 6 GHz for example, are required. As the termination is frequency dependent, a linear simulation of the complete network is used. With the setting of the termination of $\Gamma_t = 0.5$ and $\angle\Gamma_t = 115^\circ$ and with feedback capacitance of 1 pF, we have an active device input reflection that is bounded between 1.1 to 1.5 and peaks to a value of 2.3, see Figure 6.6. The input reflection coefficient with a sweep in frequency is located on the short side of the reflection plane as desired. Once again, plotting the inverse device reflection coefficient permits positioning the active device reflection coefficient locus within the unit circle of the chart. The chart center normalized to $-Z_o$ for inverse reflection coefficients. Next, we need to address if the entire tuning range of the active device, which is terminated by a series resonator permits a stable tuning condition to exist between points X_1 and X_2 . These inverse reflection coefficient points and all points in between, provide a necessary condition for oscillator startup. That is, the active device negative resistance that is sufficiently large relative to the resonator losses. The resonator losses apparent from the diameter of the resonator reflection coefficient and hence the resonator unloaded Q . It is interesting to note, that the active device reflection coefficient is circumscribed by the resonator locus. This feature is treated in detail in Appendix C. Nevertheless, this locus of the active device inverse reflection coefficient is still problematic.

Over a narrow frequency range, beginning at location X_1 and in the region about frequency points near X_1 , there is no problem, see Figure 6.6. However, evaluation of the derivative products given by (5.12) is required for the entire active device locus range, between region

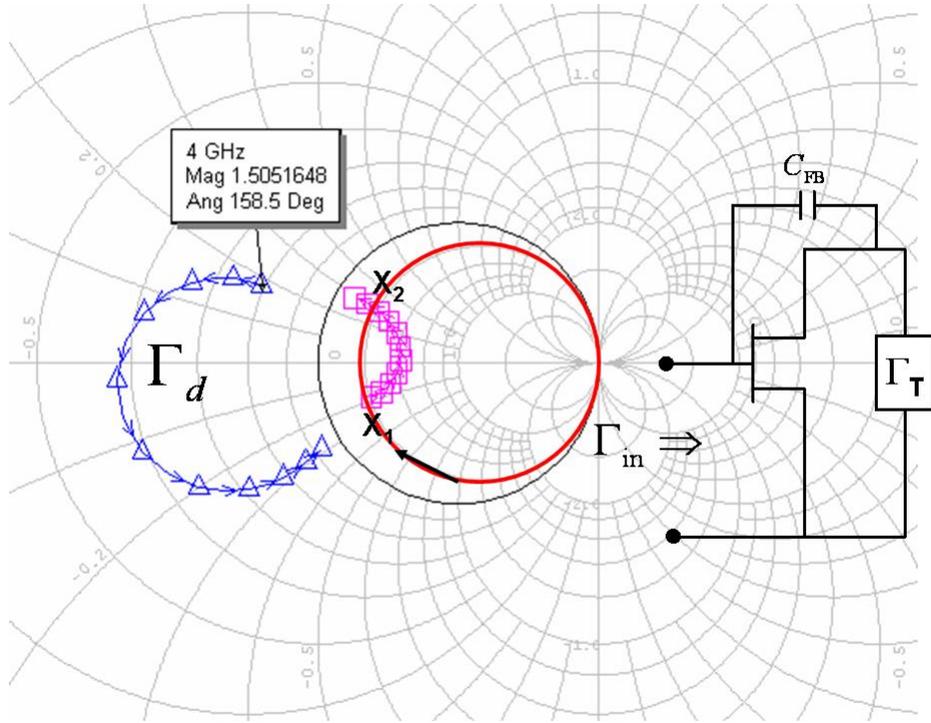


Figure 6.6: The swept frequency active device input reflection coefficient for the GaN FET and its inverse from 4-6 GHz, from design. The input reflection coefficient, marker noted at 4 GHz, and at 6 GHz, is slightly lower than the criteria set for Γ_{in} . The inverse input reflection is plotted with a representative finite unloaded Q series resonator. Multiple resonator crossings are noted, see text.

X_1 and X_2 . We see in this case, the device conductance is a function of operating point and frequency. While the product of the second term of (5.12) is zero, the product of the first term must be positive if stable tuning is to be assured. This implies that the $\frac{\partial G_d}{\partial V_r}$ and $\frac{\partial B_o}{\partial \omega_r}$ must both be negative or both be positive for all operating conditions of frequency and amplitude. Herein lies the problem. Our specified resonator is a series topology. Therefore, $\frac{\partial B_o}{\partial \omega_r}$ is a decreasing function with increasing frequency. Hence, the $\frac{\partial G_d}{\partial V_r}$ must also decrease with an increase in amplitude. While this condition is met at frequencies near location X_1 , it is not met at frequencies approaching X_2 . Reference to Figure 6.7 is helpful.

In this figure, the movement of the reflection coefficient value of the series resonator with increasing frequency is noted in a clockwise direction. The active device limiting characteristics

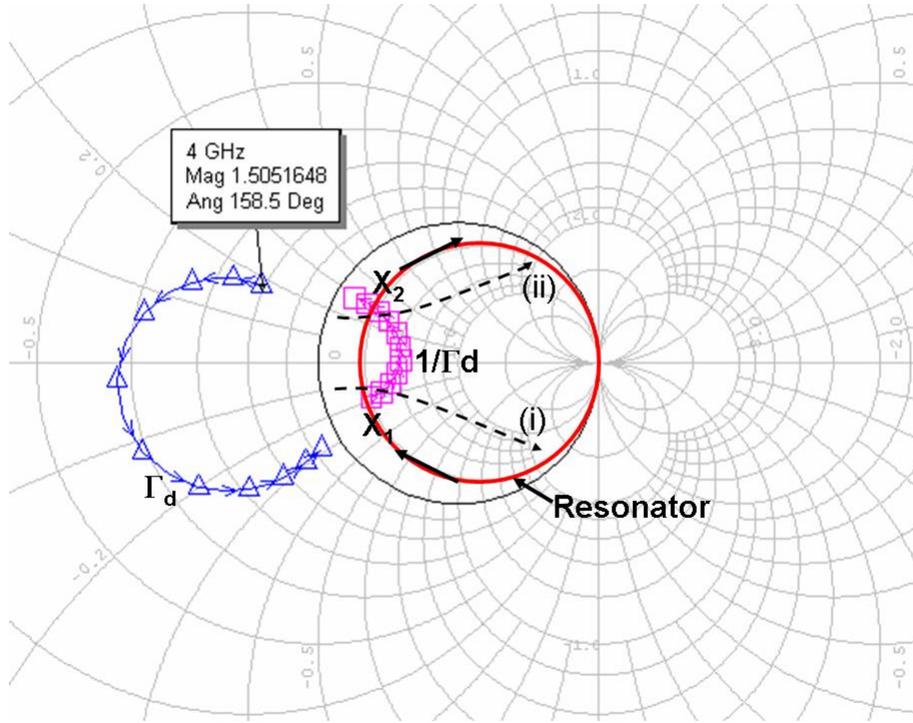


Figure 6.7: The limiting characteristics of the GaN FET are along lines of constant susceptance. Shown at (i) the limiting vector will provide stable tuning, while at location (ii), stable tuning will not occur.

are also noted, see Figure 6.7 (i) and (ii). The limiting characteristics are those of a shunt type oscillator as their self limiting trajectory vector is along a line of constant susceptance. Our intention is to operate the device with a series resonator termination. However, if we operate the resonator below its series resonance point, the first two product terms of (5.12) are satisfied. Any attempt to force the active device to move towards a higher frequency associated with point X_2 will be unsuccessful. Instead, the condition of oscillation will more than likely be met by a jump to lower frequency as the resonator is tuned. The only viable frequency-active device and resonator reflection coefficient pairs that are viable, must be constrained near region X_1 . Another observation to note, is the rotation of the active device inverse reflection coefficient must be opposite to that of the resonator reflection coefficient with change in frequency. This is necessary in order to satisfy the required angular relationship between the active device inverse

reflection coefficient and the resonator reflection coefficient to meet a condition for oscillation. The sum total of reactance of this reflection coefficient pair, at each radian frequency ω_r , must be zero, see Section 5.1.1. Clearly this is not the case near the region X_2 . Inspection of the resonator susceptance with increased frequency and the limiting trajectory for the active device, Figure 6.7 (ii), are both moving clockwise.

Clearly, a key issue in successfully synthesizing a stable tuning range for the oscillator system, resides in properly combining the active device limiting characteristics over the operating frequency range, with that of the resonator locus. We need to consider a catalog of the oscillator-resonator configuration pairs, which will always result in a stable oscillator tuning condition. There are two resonator possibilities and two active device topologies. Therefore, two principal configurations are available. However, the resonators may be operated either above or below their intrinsic resonate points. As far as the active device is concerned, the resonator is a termination network whose phase is adjustable. Therefore, two additional possibilities exist which permit the series oscillator configuration to be used with a parallel resonator and a shunt oscillator configuration to be used with a series resonator.

If a shunt oscillator active device inverse reflection coefficient limits in the capacitive region of the chart, and a series resonator is used, then its tuning must be confined below its series resonance point and remain capacitive reactive. If a series oscillator active device inverse reflection coefficient limits in the inductive region of the chart, and if a parallel resonator is used, its used below its parallel resonant point where its reactance remains inductive. However, we recognize that these are conditionally stable tuning configurations as previously discussed. A configuration which interfaces the series oscillator with the series resonator and its dual, the shunt oscillator with the parallel resonator, are considered unconditionally stable tuning configurations as they meet the conditions of (5.12) over the entire possible tuning range. The “entire possible tuning range”, defined here as the range in frequencies whereby the resonator unloaded Q is sufficiently large with respect to the real part of the active device reflection coefficient. Therefore, meeting the conditions for oscillator start up.

In Figure 6.8 and 6.9, we diagrammatically display the possible conditions for assuring a stable oscillator tuning system. Figure 6.6 shows unconditional stable tuning. The series oscillator inverse reflection coefficient trajectory will limit via the path described by the vector V_r and intersect the series resonator locus always above the self resonant frequency, ω_s . This is true for all values of ω_r in Figure 6.8 (a). While in Figure 6.8 (b) the same conditions hold true for the shunt configuration oscillator and the parallel tuned resonator. Again, operation of the resonator provides all the needed termination phases for the active device, while operation is confined above the parallel resonant frequency of the resonator.

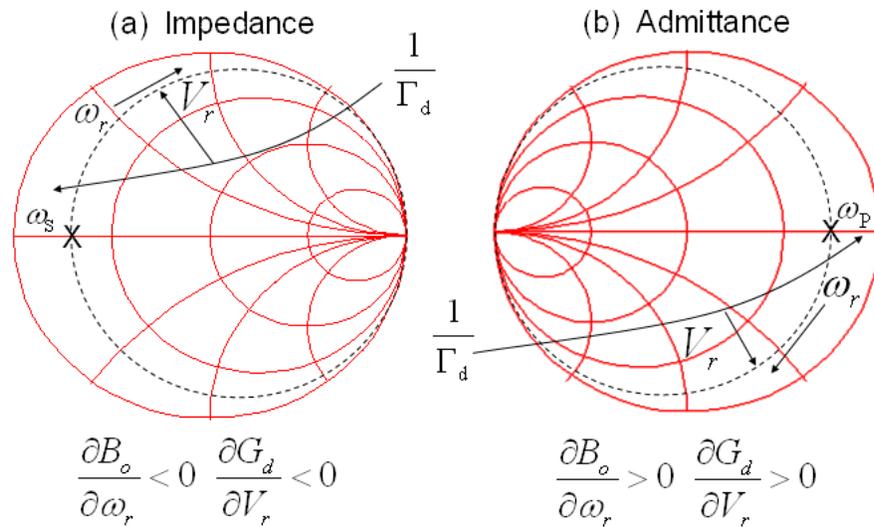


Figure 6.8: Unconditional stable tuning is assured on the reflection plane where we:(a) consider the impedance of the series resonator and the limiting characteristics of the series oscillator; (b) the admittance of the parallel resonator and the interface to the shunt oscillator.

Conditional stable tuning occurs when the series oscillator type is interfaced to a parallel tuned resonator. Provided operation of the resonator is confined to tuning points below the intrinsic parallel resonant frequency of the resonator stable tuning is assured. The case of the shunt oscillator configuration is satisfied by a series tuned resonator. Again, stable tuning is provided if the desired oscillator tuning frequencies are obtained by operation of the resonator

below its series resonant frequency.

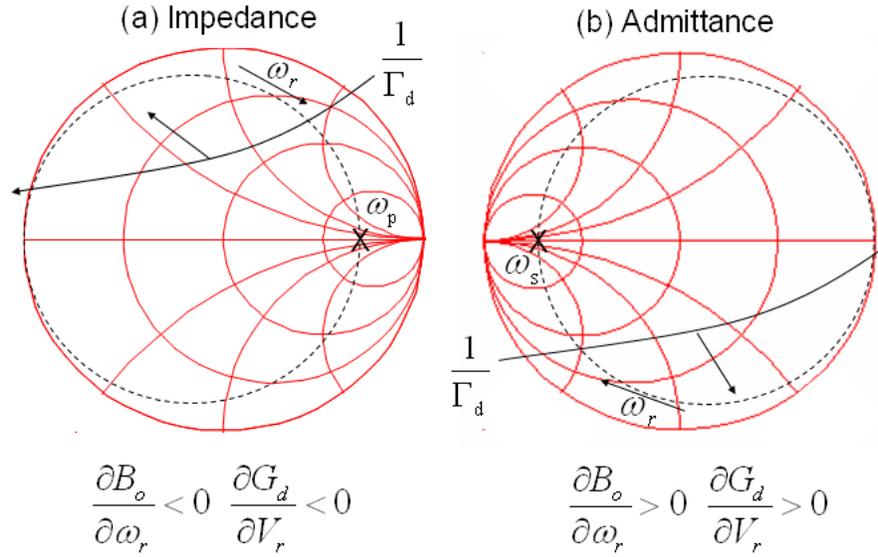


Figure 6.9: Conditional stable tuning occurs when the interface between the active device and the resonator are mixed, that is in: (a) the parallel resonator terminates the series oscillator while; (b) the series resonator terminates the shunt oscillator.

If the desired resonator is not amenable to modification, then modification of the active device reflection coefficient is available as discussed in Section 5.1.3. Our requirement is to maintain the magnitude of the input reflection coefficient near 1.5 along with a smaller variation in Γ_{in} . In addition, we require a broader stable tuning range. Hence, either a different network or a modified topology is required. Similar to the technique discussed in Section 5.1.3, we may force the rotation of the inverse reflection coefficient counter clockwise by adding a shunt input capacitance to the gate, shown in Figure 6.10. The result rotates $\frac{1}{\Gamma_{in}}$ into the inductive region of the chart, the device input reactance is capacitive, and the modified HFET device will now accept a series resonator. The active device limiting characteristics are along lines of constant capacitive reactance contours, shown in Figure 6.10 as the limiting trajectory. The counter clockwise direction of motion of $\frac{1}{\Gamma_{in}}$, as required with increasing frequency, is also shown. Each sweep of $\frac{1}{\Gamma_{in}}$ is shown versus incident power, P_{in} with $P_{in3} > P_{in1}$.

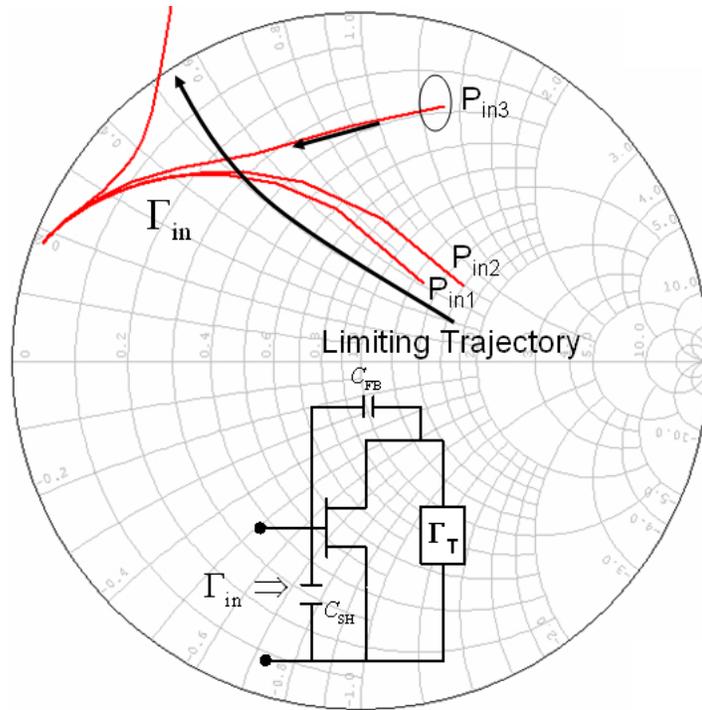


Figure 6.10: Provision for stable tuning over an increased tuning range requires device modification. The addition of a shunt capacitor, C_{sh} rotates the active device inverse reflection coefficient counter clockwise into the region where a series resonator termination is accommodated.

These techniques are applied in the design of a Si-GaN-HFET oscillator utilizing an IDC-BST thin-film varactor, as shown in Figure 1.8. The schematic with highlight on the termination and feedback elements is shown in Figure 6.11. This device is packaged in thermally conductive CuW singled-ended package using an AuSi eutectic process that grounds the source vias to the package. Nevertheless, due to the size of the package and lead frame, the parasitics of the package are significant. These package parasitics in themselves further modify the active-device two-port die parameters, since the source lead is actually returned to ground via additional series inductance as well as shunt capacitance. Modeling the source return to ground through this parallel LC network demonstrates that gate-drain inductive feedback, L_{fb} as opposed to gate-drain capacitive feedback, C_{fb} , is now sufficient to generate an inverse Γ_{in} greater than unity, see Figure 6.12. The input termination required is capacitive and a series resonator is

completed with the addition of a varactor coupled to the gate terminal.

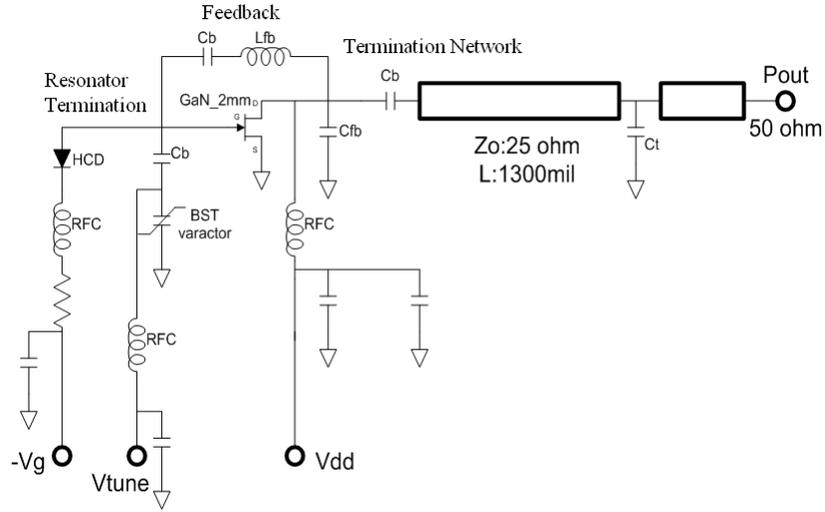


Figure 6.11: A Si-GaN-HFET power oscillator. The load termination provided output power match and an appropriate input reflection coefficient to form a shunt tuned oscillator.

The resonator is operating as a gate termination network and is implemented with a series coupled BST varactor in shunt with the gate. The varactor network operation with the GaN-HFET creates a shunt configuration oscillator which is series tuned as shown in Figure 6.9 (b). Therefore, from inspection of the inverse reflection coefficient versus frequency seen in Figure 6.12, the available tuning range is constricted.

However, the specific case shown in Figure 1.8 is constrained first by the $C - V$ range of the IDC BST varactor as this particular varactor had less than a 1.5:1 capacitance change with tuning voltage and furthermore, is also decoupled from the gate terminal through a series capacitance, C_b further restricting the tuning range. Nevertheless, a 5% tuning range is obtained with an output power of 1.6 W and a conversion load efficiency of 25%.

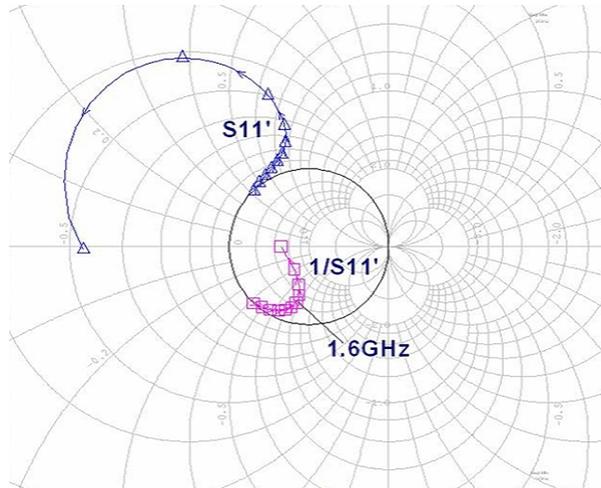


Figure 6.12: The inverse input reflection coefficient for a 1.6 GHz Si-GaN-HFET power oscillator. The self limiting trajectory for this power oscillator is along a constant susceptance line.

6.1.3 Conclusions on resonator and active device interface

In this section we extended the work presented in Section 4.4 and 5.1.3 and addressed other combinations of the resonator and the active device interface for stable tuning. The resonator is considered a termination network, however providing an adjustable phase with an applied tuning voltage. The active device is generative with the ability to provide negative resistance and a reflected voltage larger than the incident. The resonator then provides the correct phase relationship to sustain oscillation. Therefore, providing a synthesis approach to the interconnect between the resonator and the active device was the focus of this section. A catalog of possible interconnections between resonator and active device was presented and two additional configurations are provided. These additional networks extend the operation of the shunt and series oscillator to resonator topologies that are the dual of the intended networks. The series resonator connection to the shunt oscillator and the shunt resonator connection to the series oscillator are discussed as additional configurations. However, the stable tuning bandwidths may be limited.

The catalog of these possible interconnections is driven by the self-resonant frequency of the

resonator. That is to say, where the resonator is inherently resonate without the presence of the active device. Operation of oscillators can be confined to the intrinsic resonant frequency of the resonator, for example crystal oscillators, although this is not necessary. Hence, operation above below, or at resonance is readily achieved and serves as a metric for consideration in describing the tuning ability of a VCO.

Additionally, in this section, we recast the oscillator mapping approach discussed in Section 5.1.1 into one in which we must first meet the impedance or admittance trajectory of a selected resonator. This approach is preferred for realizing stable tuning, as opposed to independently maximizing the magnitude of the input reflection coefficient or the active device output reflection coefficient for maximum output power.

In the case of a design for which a specified selected output power is required, the load reflection coefficient would take precedence. This process is then followed by the selection of a combination of device topology and feedback, and then both feedback and load termination are adjusted to meet the required resonator port reflection coefficient versus frequency. Such an approach is discussed next in Section 6.2.

6.2 GaN and IMFET power oscillators from power amplifiers

The load pull technique is a measurement methodology for characterizing and designing power amplifiers, low noise amplifiers and oscillators [147]. The basis for the methodology is rooted in characterizing the device under actual operating conditions and finding termination from measured performance. If the device models are accurate, then the results of the calculated terminations should agree with the results obtained from the load pull measurement for the same performance metric.

Oscillator design based on power amplifier design is an approach which is amenable to small signal analysis. This is fortuitous, since nonlinear device models are not widely available. Therefore, the synthesis of class A power amplifiers can proceed from small signal measurements obtained from a vector network analyzer.

In this section we develop a technique for class A amplifier design which is subsequently used to synthesize the oscillator embedding elements. We begin by synthesizing a set of terminations that maximize the class A amplifier output power, while providing an appropriate input and output amplifier impedance, characterized by the return loss. Then we embed a passive matched feedback network which operates as the resonator and locks in the phase shift of this open loop system. Additional phase shift as needed to satisfy the conditions of sustained oscillation when the loop is closed, is added with a length of series transmission line. Output power from the closed loop system is provided by sampling the available power at selected points and is conveniently obtained by the use of a coupler [148].

Optimization of the power oscillator load efficiency proceeds by adjusting the open loop gain and subsequently the closed loop gain. At the same time, we adjust the gate to source voltage relative to the pinch off voltage. Per the development of the FET conversion efficiency discussed in Appendix D, we find oscillator load efficiency will improve in accordance with the loop gain, the gate-source voltage relative to the active device pinch off voltage, and the peak RF feedback voltage.

A Silicon GaN HFET is operated in a grounded source configuration, thus achieving our required thermally stable system. Linear S-parameters are obtained for a packaged HFET device using a set of TRL calibration kits developed to measure the packaged device. Small signal S-parameters are obtained at 28 V_{dc} drain voltage at various drain bias currents from 50 to 200 mA . The input signal power for measurements is 0 dBm. In addition, a nonlinear model is provided. However, its operation is over a limited frequency, less than 1.5 GHz, and bias range. Nevertheless, the nonlinear model is used in simulation to assist in collaboration with measured data small signal S-data.

There are a number of disparate differences between S-parameters obtained from the nonlinear model and the S-parameters obtained from linear small signal measurements. These issues and the approaches taken to resolve them are discussed and then applied to the power oscillators designed over the frequency range of 2 through 6 GHz.

The small signal S-parameters, both linear and those derived from nonlinear simulation are shown in Figure 6.13. The sweep range is 0.23 to 6 GHz.

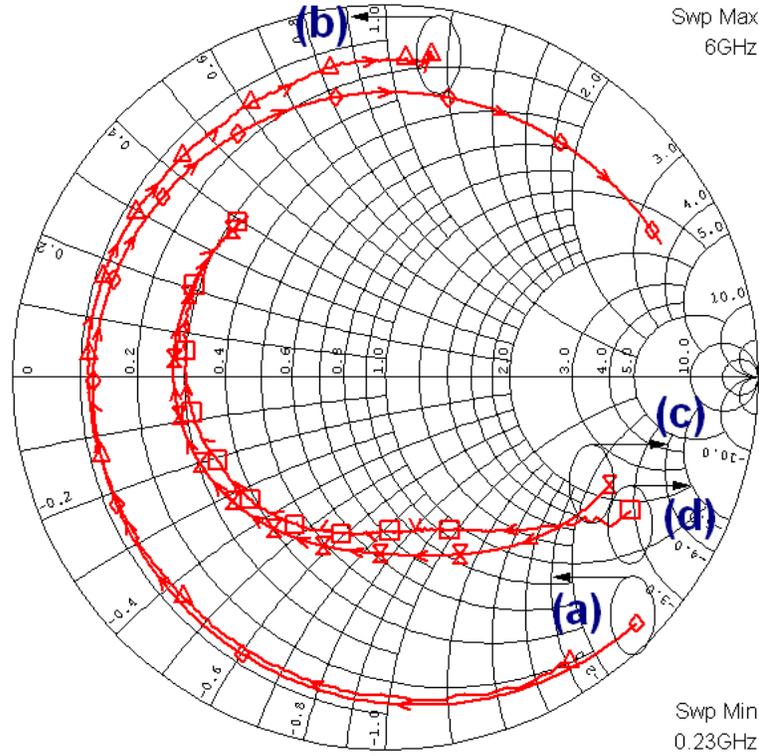


Figure 6.13: (a) Measured and calculated from nonlinear and small signal S-parameters at V_{dd} of 28 V and I_{dd} of 100 mA for: (a) S_{11} nonlinear model; (b) S_{11} measured ; (c) S_{22} nonlinear model; (d) S_{22} measured.

Although the data sets for S_{11} and S_{22} appear to match well, there are differences that cause problems in amplifier synthesis. Particularly the case for developing the matching network to maximize output power and the required device terminations. If the Rollet stability factor k is evaluated, all S-parameters including their magnitude and phase are accounted for in calculation as k is given by,

$$k = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \quad (6.7)$$

where Δ is the determinant of the two port s-matrix. With $k < 1$, the ability to synthesize

terminations for a feedback oscillator based on power amplifier design is limited to select regions of the chart. These regions are provided by stability planes and are readily mapped onto the chart.

A plot of k from the measured device S-parameters, S-parameters extracted from the nonlinear model, and from the stabilized nonlinear model are presented in figure 6.14. The lack of good agreement of k which is extracted from calculations using the linear and nonlinear model poses difficulty in developing and then testing networks intended for the oscillator implementation.

Oscillator simulation requires a valid nonlinear model if output power and efficiency are to be validated. Therefore, we need to achieve stability and agreement with the linear S-parameter measured data. Our interest is in maximizing the output power and the load efficiency. Therefore, device stabilization using dissipative losses needs to be confined to the input networks connected to the device. An easy method for moving the device input stability plane outside the chart is achieved by the addition of a resistance in series with the gate terminal. The addition of a $6.8\ \Omega$ resistor in series with the gate permits $k > 1$. The resulting graphs for k vs. frequency, see Figure 6.14, illustrate the small signal, nonlinear, and the stabilized nonlinear k derived values with a series gate resistance added. After the addition of the series gate resistor, the agreement between nonlinear and small signal k factor is reasonable. If a slight increase in circuit complexity is applied, a parallel RL network in series with the gate terminal permits very good agreement, see inset plot of Figure 6.14. In addition to the agreement in k , all four S-parameters agree well over a frequency range of 0.2 through 6 GHz. Using this modified nonlinear model, port terminations are then sought to find the maximum linear output power.

The optimum load conductance termination, is a function of the quiescent drain to source voltage and the active device operating current. If neither current or voltage clipping or saturation are to occur, then the optimum load conductance, G_o , is formed by an output load line with slope given by

$$G_o = I_{ds}/V_{dd} \quad (6.8)$$

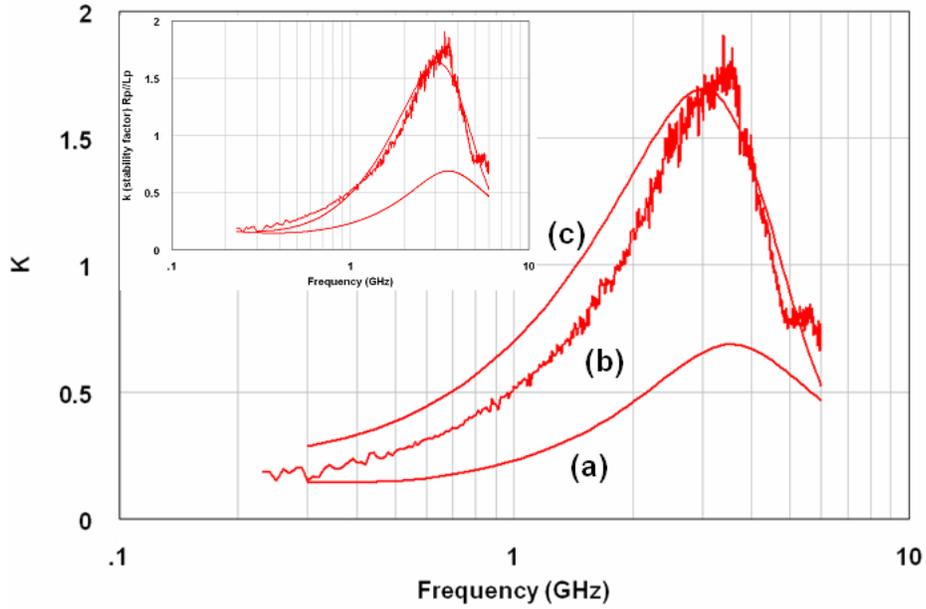


Figure 6.14: Power amplifier stability factor: (a) stability factor k from nonlinear model; (b) k from small signal measured S-parameters and; (c) k from nonlinear model with series gate R of 6.8Ω added, (inset graph $7\Omega // 1.2\text{ nH}$).

and with a maximum output power for class A operation of

$$P_{\max} = I_{ds}^2 / 2G_o . \quad (6.9)$$

A load conductance with a slope which is greater than or lesser than that given by (6.8) will provide less output power. If the chosen load conductance, G_L , is larger than the optimum, current clipping will occur. However, too small a load conductance leads to early output voltage saturation. Consequently, a family of output load contours are found normalized to an optimum load conductance, G_o , and demonstrate the decrease in power output with subsequent changes in power gain. The resulting output power capability of the active device, as a function of the load terminations which deviates from the optimum is summarized as,

$$|G_o| < |G_L| \Rightarrow P_L = I_{ad}^2 / 2G_L \quad (6.10)$$

Table 6.1: Power amplifier configured for maximum output power

Si-GaN-HFET S-parameters, stability and terminations										
$ S_{11} $	$\angle S_{11}$	$ S_{12} $	$\angle S_{12}$	$ S_{21} $	$\angle S_{21}$	$ S_{22} $	$\angle S_{22}$	k	Z Source Ω	Z Load Ω
0.58	162	.02	-0.8	5	34	.49	-124	2.3	$10 - j8$	$16 + j24$
-	-	-	-	-	-	-	-	-	* $5.4 - j10$	* $14.75 + j10$

The impedances listed for comparison are CW, 28 V at 50 mA obtained from an active load pull for P_{out} and efficiency(*)

$$|G_o| > |G_L| \Rightarrow P_L = \left[\frac{V_{dd}^2}{2} \right] G_L \quad (6.11)$$

$$G_L = G_o \left[\frac{P_L}{P_{max}} \right] . \quad (6.12)$$

Therefore, the problem is one of mapping a family of power gain contours onto the reflection plane, along with the appropriate load conductance termination contours. These contour intersections, provide a map of output power capability along with the associated power gain which is achieved.

Maximum power gain and maximum output power usually do not occupy the same set of port terminations. Therefore, a mapping solution is used for the calculation of the power gain for the two port network while applying the load termination which maximizes the output power. The resulting input reflection coefficient results in an input impedance which is subsequently conjugate matched. Finally, the resulting output reflection coefficient must not be too large as to severely mismatch the resonator at the output port. The open and closed loop networks under consideration, including the matching sections and phase shift networks are shown in Figure 6.15. With the loop closed, power is extracted from an in-line coupler via CL_OUT, while with the loop open at -X-, the input and output measurements permit assessing open loop gain and phase.

The design begins at a single frequency, 2.4 GHz. The S-parameters provided by the non-linear model and the computed k factor are displayed in Table 6.1. A Mathcad script is written to provide a single frequency solution with graphical output, see Figure 6.16. Shown in the figure are the instability planes and with $k > 1$ and are outside the chart as desired, Figure

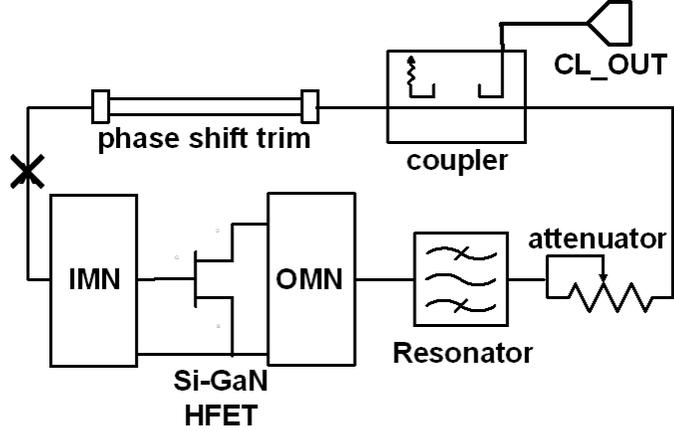


Figure 6.15: The feedback loop oscillator provides an open loop point at **X** to assess conditions for meeting oscillation. Closed Loop output is extracted from an in line coupler while the loop is closed. Open loop gain and phase is adjustable through selection of the transmission line lengths (phase shift trim). Input and output matching networks (IMN, OMN), control loop phase shift and output power.

6.16 (a) and (b). The plots shown are obtained by working with the two-port S-parameters of the active device and the bilateral relationship of the reflection coefficients between the input and output ports of the active device [150] given by,

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (6.13)$$

and

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \quad (6.14)$$

Therefore, at the design frequency, the entire region of the chart is stable, implying the active device is stable for all real-complex terminations. Points along the Figure 6.16 (c) contour provide constant power output as this contour is one of constant conductance, while points along Figure 6.16 (d) provide a specific constant gain, 14 dB in this case. The use of this chart is extended to power oscillator synthesis based on power amplifier design and is discussed next in developing Figure 6.17.

The active device amplifier transducer gain, G_T , is a function of both the source and load

terminations and the active device S-parameters. Consequently, the transducer gain provides the most complete gain definition as it includes the affect of input and output terminations and the terms Γ_s and Γ_L are included. An active device which is unconditionally stable can be terminated with any source or load reflection coefficient within the unit chart. The transducer gain is given by,

$$G_T = |S_{21}|^2 \frac{1 - |\Gamma_s|^2 (1 - |\Gamma_L|^2)}{|1 - S'_{11}\Gamma_s|^2 |1 - S_{22}\Gamma_L|^2}. \quad (6.15)$$

While the transducer power gain depends on the power available from the source, the power gain depends on the power input to the network. In both cases, the gain definitions depend on the measurement of power delivered to the load. The power gain, G_P is expressed as,

$$G_P = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{(1 - |\Gamma_{in}|^2) |1 - S_{22}\Gamma_L|^2}. \quad (6.16)$$

However, with Γ_{in} given by (6.13) and with the load termination set to the optimum for maximum output power, we have

$$G_P = |S_{21}|^2 \frac{1 - |\Gamma_o|^2}{|1 - S_{22}\Gamma_o|^2 - |S_{11} - \Delta\Gamma_o|^2} \quad (6.17)$$

where Δ is the determinate of the $[S]$ matrix. With the input matched and the termination chosen to maximize the output power, $\Gamma_t = \Gamma_L = \Gamma_o$.

The mapping process for the construction of the chart contours which are used in power amplifier design and subsequently in power oscillator synthesis are described next. The location of optimum source and load reflection coefficients for the conjugate matched and maximum output power points are also plotted within the Mathcad script. The distinct values are tabulated in Table 6.1. The load termination, $\Gamma_t = \Gamma_L = \Gamma_o$ is found first. The real value of Γ_o is found based on maximizing the class A output power given by (6.8) and (6.9). While every point on the load conductance contour will provide the maximum output power, only one unique point will also provide the maximum power gain. A point of tangency exists between the real

part of Γ_o or G_o , which coincides with the maximum power gain contour. These points of tangency which exist among a family of conductance values and power gain contours, fall along a trajectory which is a constant susceptance contour with center location and radius given by, $(-1, 1/B_n)$ and $(1/B_n)$, where B_n is given by,

$$jB_n = -j \frac{2 |\Gamma_{o,\text{gain}}| \sin(\angle \Gamma_{o,\text{gain}})}{1 + 2 |\Gamma_{o,\text{gain}}| \cos(\angle \Gamma_{o,\text{gain}}) + |\Gamma_{o,\text{gain}}|^2} \quad (6.18)$$

and $\Gamma_{o,\text{gain}}$ is the output reflection coefficient which provides maximum power gain, [179] defined by

$$\Gamma_{o,\text{gain}} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}. \quad (6.19)$$

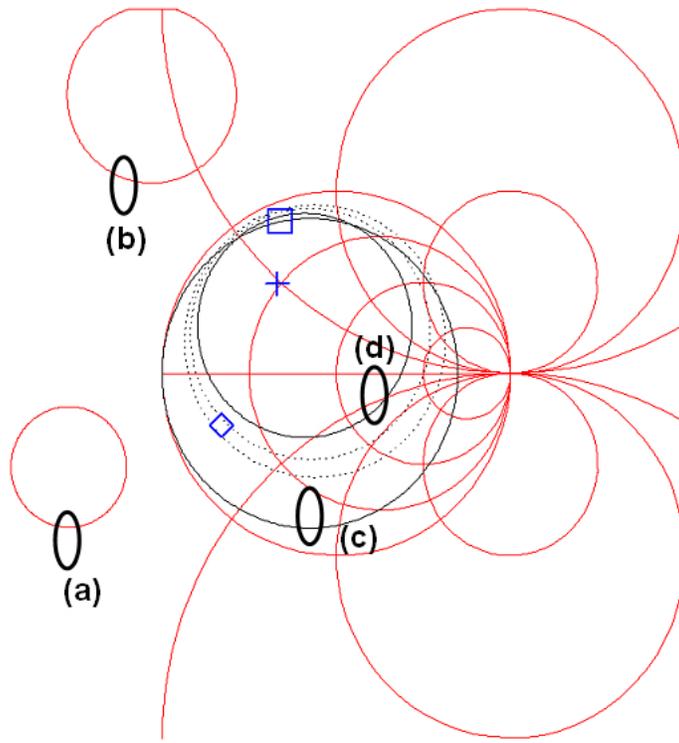


Figure 6.16: Amplifier circle contours suitable for oscillator synthesis include: (a) input stable plane; (b) output stable plane; (c) load conductance contour; (d) 14 dB power gain contour.

The terms C_2 and B_2 are given by, $C_2 = S_{22} - \Delta S_{11}^*$ and $B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$. Our aim however, is to maximize output power commensurate with as a high a power gain as possible. Therefore, we find an output load reflection coefficient composed of a real part given by the conductance G_o and an imaginary part given by the susceptance B_n . Therefore, Γ_o is given by,

$$\Gamma_o = \frac{1 - (G_o + jB_n)}{1 + G_o + jB_n}. \quad (6.20)$$

Utilizing Γ_o as the termination to the active device results in an input reflection coefficient which is subsequently conjugate matched and presented to the resonator.

Illustrated in the contour map on the chart, there is trade-off between power gain and power output. Successively higher power gain contours will decrease in radius with centers offset with the center of the power output conductance contour. Correspondingly higher output power gain with lower maximum power output results. See Figure 6.17 for discussion.

The maximum power output contour is a constant conductance contour and is plotted in Figure 6.17 (a). This contour is a function of the quiescent drain current and in our study the drain current is between 100 and 250 mA at 28 V. This positions the conductance contour between a value of 4 and 9 m Ω obtained from (6.8). Assuming the entire drain supply voltage is available and a load conductance of 9 m Ω is used, the maximum class A output power is approximately 1.7 W at 175 mA of drain current. Based on a nominal DC drain current of 100 mA, a maximum transducer gain of 18 dB is possible and is denoted at point (b). However, the output power is significantly reduced to less than 100 mW. As we progress away from the maximum power gain point at (b), we intersect decreasing power gain contours, however increasing power output. At point (c), the power gain is reduced 1 dB and the locus of triangle (Δ) points outlines a 17 dB power gain contour. The optimum output power point is arrived at point (d), denoted with a cursor box (\square) and is coincident with a 15 dB power gain contour. Therefore, for the specific device, a 3 dB reduction in power gain is required to maximize the output power. Establishing the Γ_o at point (d) and providing that particular termination, results in an input reflection coefficient at point (e), the diamond (\diamond) cursor. The difference between the

location of the load termination set by Γ_o and the actual output reflection coefficient, circle, represents a mismatch. The resulting input and output return losses associated with each of the port reflection coefficients are 15 dB and 6 dB for the input and the output ports respectfully. Although these ports are not precisely equal to the resonator port impedances, to be discussed next, they are sufficient and acceptable as the loop gain achieved is more than required to meet the start up condition for oscillation.

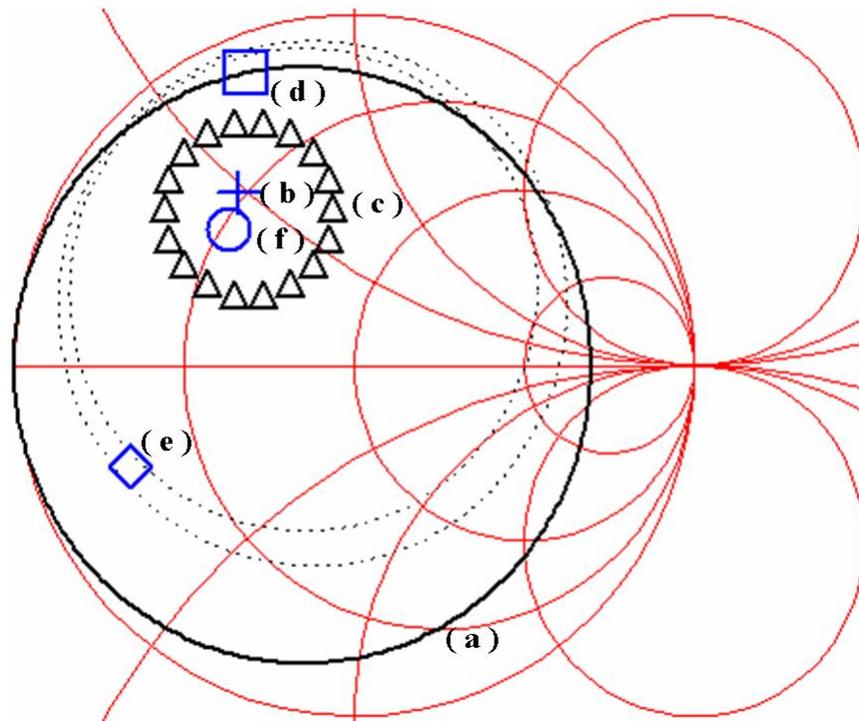


Figure 6.17: Reflection coefficient loci for maximum power gain and maximum output power. Contours are offset from each other: (a) constant load conductance contour; (b) maximum power gain point; (c) 17 dB power gain contour; (d) the optimum power output reflection coefficient; (e) the input reflection coefficient with the output terminated in Γ_o and (f) the resulting output reflection coefficient with the input terminated in the conjugate port reflection coefficient.

A stable power amplifier is established and the procedure continues towards closing the loop. An open loop response of the amplifier provides the open loop gain and phase, see Figure 6.18.

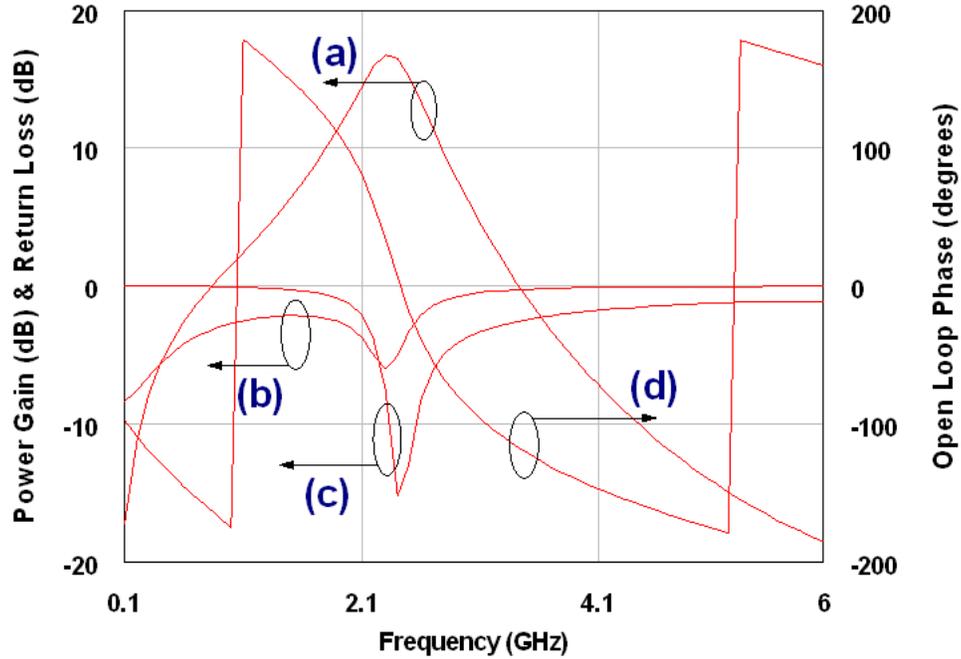


Figure 6.18: Power amplifier with matching networks showing (a) power gain (b) output return loss (c) input return loss and (d) open loop phase shift

If the loop gain is reduced 3 dB, then without a resonator to fix the phase, oscillation could occur at approximately 2.3 GHz. The frequency of oscillation is a function of the remaining loop gain and the extent of device impedance shift with large signal input. However, both phase noise and frequency stability are compromised. To this end, a resonator is inserted and the desired phase shift trimmed, either by altering the resonator series capacitance or adding an additional phase shift element with the addition of a series transmission line. The resonator is a conventional shunt C-series L-C network. The loaded Q is set by the shunt C elements and the resonator frequency set by their series equivalent form, in series with the remaining series L-C network. The series network is formed by a short series transmission line, a lumped series L and a varactor. Phase shift is controlled by C_v in lieu of C_1 and C_2 , as varying these elements significantly varies the loop gain as these capacitors form a voltage divider. Any additional trim in phase range required is accommodated by adding a low loss series line with a delay proportional to the physical line length and the operating frequency. The resulting

network is shown in figure 6.19. The loaded Q values investigated were between 5 and 10. The concatenated response of the device, matching networks, resonator, and phase shifter are shown in Figure 6.20.

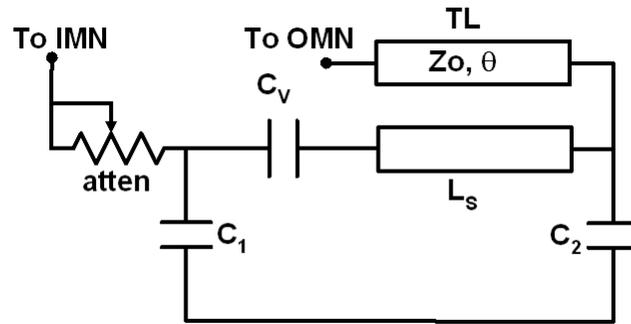


Figure 6.19: Oscillator resonator with attenuator and phase delay line. Connection of the resonator network is between input (IMN) and output (OMN) matching networks and the attenuator adjusted to control the open loop gain. The series line trims the open loop phase.

Reference to Figure 6.20, demonstrates that oscillation should occur at a single signal frequency without risk of locking at the first zero phase crossing point at 1.3 GHz, as the loop gain is insufficient. A similar condition occurs at 3 GHz, and higher multiple zero phase crossing points. If the loop gain is insufficient, and $\frac{\partial \phi(A, \omega)}{\partial \omega} > 0$, then these points will not provide stable oscillation. The inverse requirement is also required, that is for example, at 2 GHz; the open loop gain is sufficient, however the phase slope is incorrect. Therefore, for the case studied here steady-state single signal oscillation should occur near 2.4 GHz; nearly in line with the peak response of the open loop gain shown in Figure 6.20 and with the appropriate phase slope present.

The amplifier, matching networks, resonator and phase shift line were designed as outlined above and then cascaded. Designs are conducted at 2.4 and 5 GHz. A family of phase shift lines were assembled to provide a few hundred degrees of phase shift from 2–3 GHz and 4–6 GHz. These are short sections of semi-rigid 50 Ω coaxial cables and provided for the connections to complete the closed loop. The cables provided for the interconnection of the amplifier-resonator

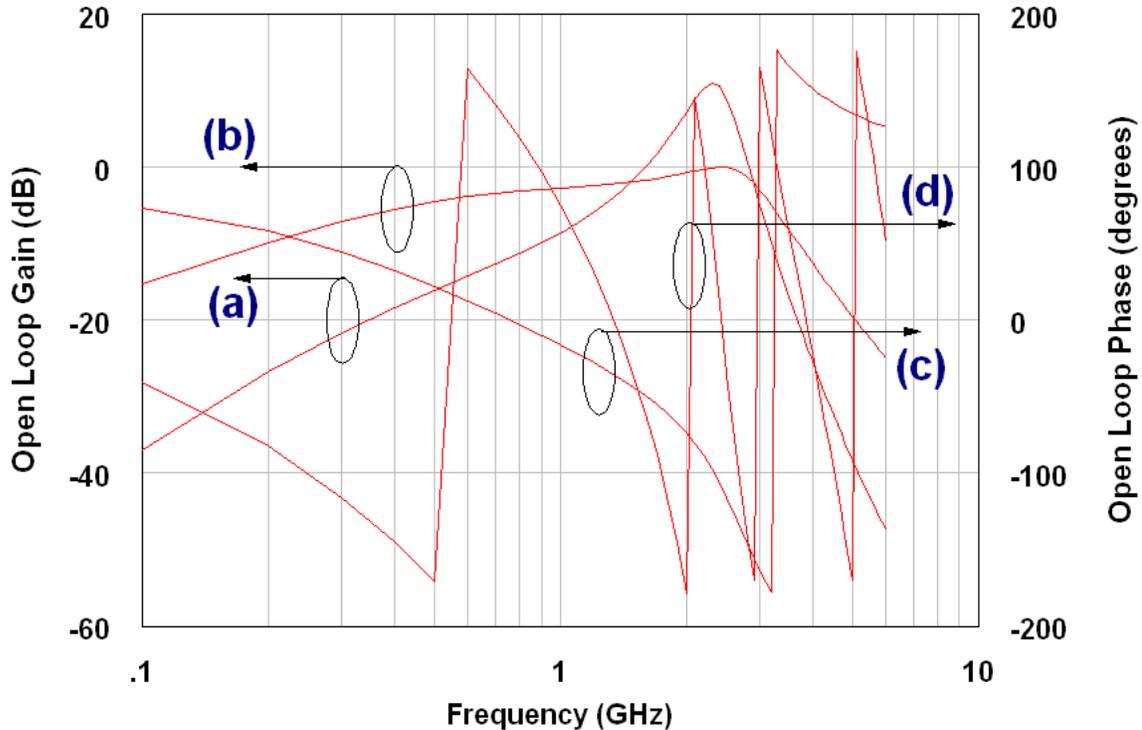


Figure 6.20: Complete open loop system response: (a) cascaded system magnitude response; (b) resonator response; (c) resonator phase shift; (d) complete cascade system phase response.

combination and a 6 dB coupler. The system test set is shown in Figure 6.21.

The power spectrum, phase noise and load efficiency are investigated for the system shown in figure 6.21. The load efficiency is of particular interest since the pinch off voltage bias setting should affect the performance as outlined in the appendix section on page 429. This is indeed the case, and we present here the results.

Firstly, the power spectrum is reported in Figure 6.22 and the phase noise in Figure 6.23. Note worthy is the low harmonic level of the 5 GHz oscillator and the phase noise of the 2.4 GHz oscillator which is dominantly $1/f$ in origin with a slope of -9 dB/octave. The 5 GHz power oscillator is similar with a 4 dB degradation in phase noise as compared with the 2.4 GHz design. This is interesting in itself, since one would expect, all elements equal, a 20 log reduction in phase noise as opposed to an approximately 10 log reduction as seen here. In

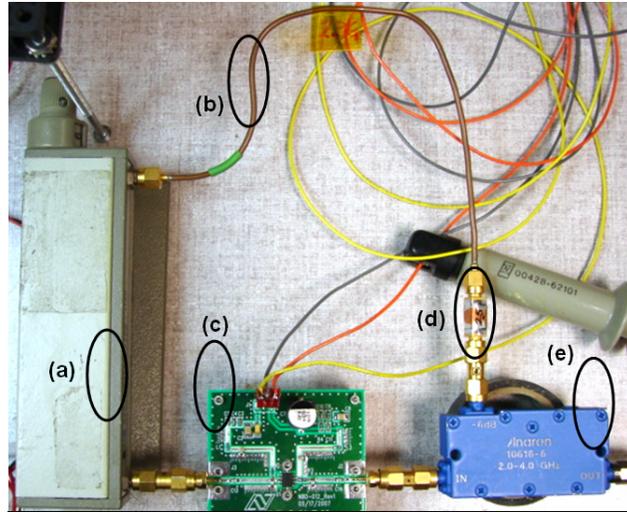


Figure 6.21: The power oscillator implementation has 5 principle elements: (a) adjustable pad for setting loop gain; (b) phase shift line; (c) power amplifier with matching networks; (d) resonator; and (e) -6 dB coupler.

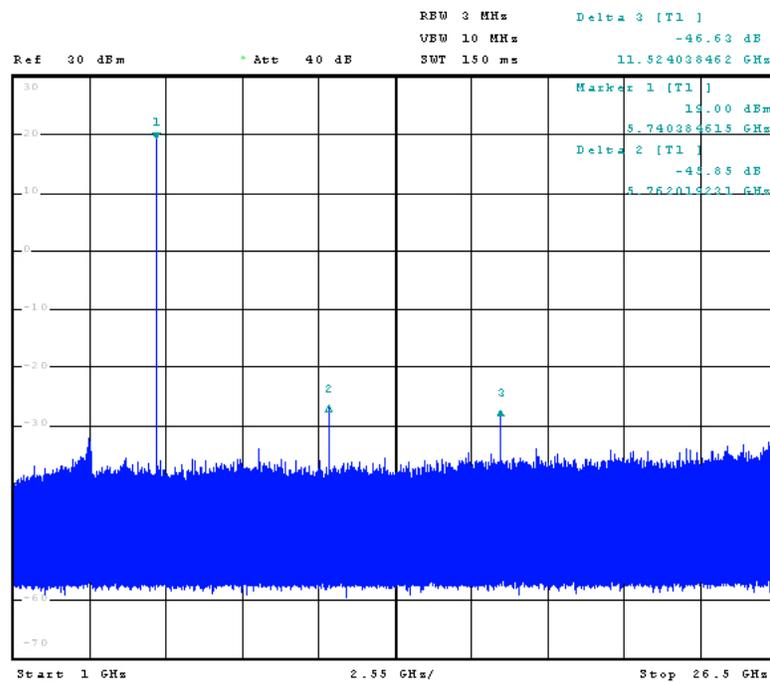


Figure 6.22: The fundamental, 2nd and 3rd harmonic of a 5 GHz power oscillator. Fundamental output power is 33 dBm at 5.74 GHz. Harmonics are measured to 26.5 GHz and all are greater than 40 dBc.

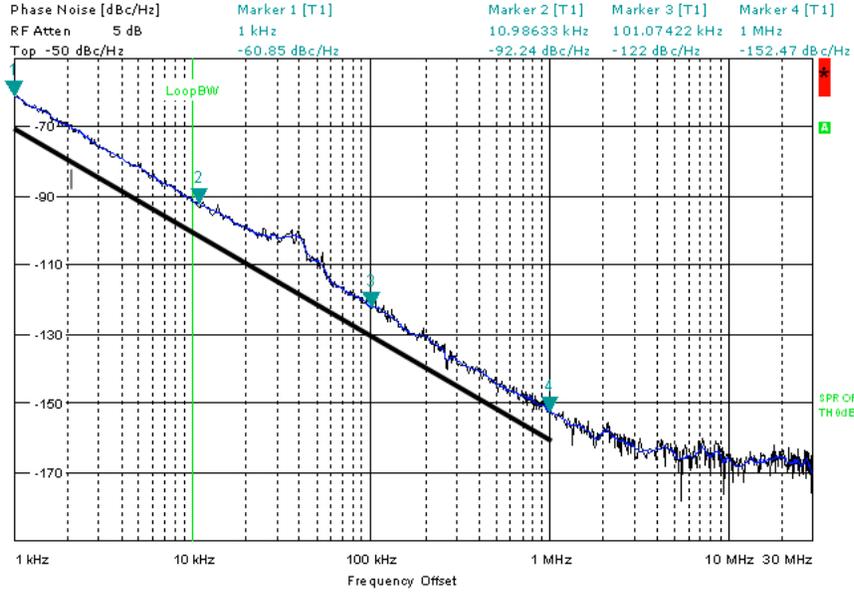


Figure 6.23: Phase noise at 2.4 GHz. The output power is 34.5 dBm. The spectral noise is $1/f$ in origin and the -9 dB/octave slope is noted out to 1 MHz. Phase noise at 10 kHz offset is better than 90 dBc.

effect, the loaded Q of the 5 GHz resonator is somewhat greater than in the 2.4 GHz design. A detailed comparison of phase noise measurements is shown in Figure 6.24. Measurements with and without a varactor, either junction or BST, showed no difference in phase noise profile. Although the magnitude of the phase noise seen here is significantly less than reported in [187]; at 100 kHz offset at -123 dBc/Hz versus -81 dBc/Hz. Nevertheless, the phase noise is still dominantly $1/f$. A major difference in the designs is associated with the active device. In this current design, the presence of a source connected field plate, which runs parallel to the channel is incorporated in the Si-GaN HFET. Similar improvements in phase noise with a properly scaled field plate element are reported in [188]. Therefore, it is reasonable to assume that the reduction of noise events including trapping, and the increased breakdown voltage via reduced field peaking with a field plate, improves power oscillator phase noise. Nevertheless, the low frequency noise, is dominantly $1/f$ -noise in slope, and affects the oscillator phase noise close to the carrier and out to at least 1 MHz offset when a low loaded Q resonator is used

in the power oscillator design. This is particularly true, as lower $1/f$ noise is found in devices operating at lower values of V_{DS} voltage, however, this is contrary to high efficiency power oscillator design.

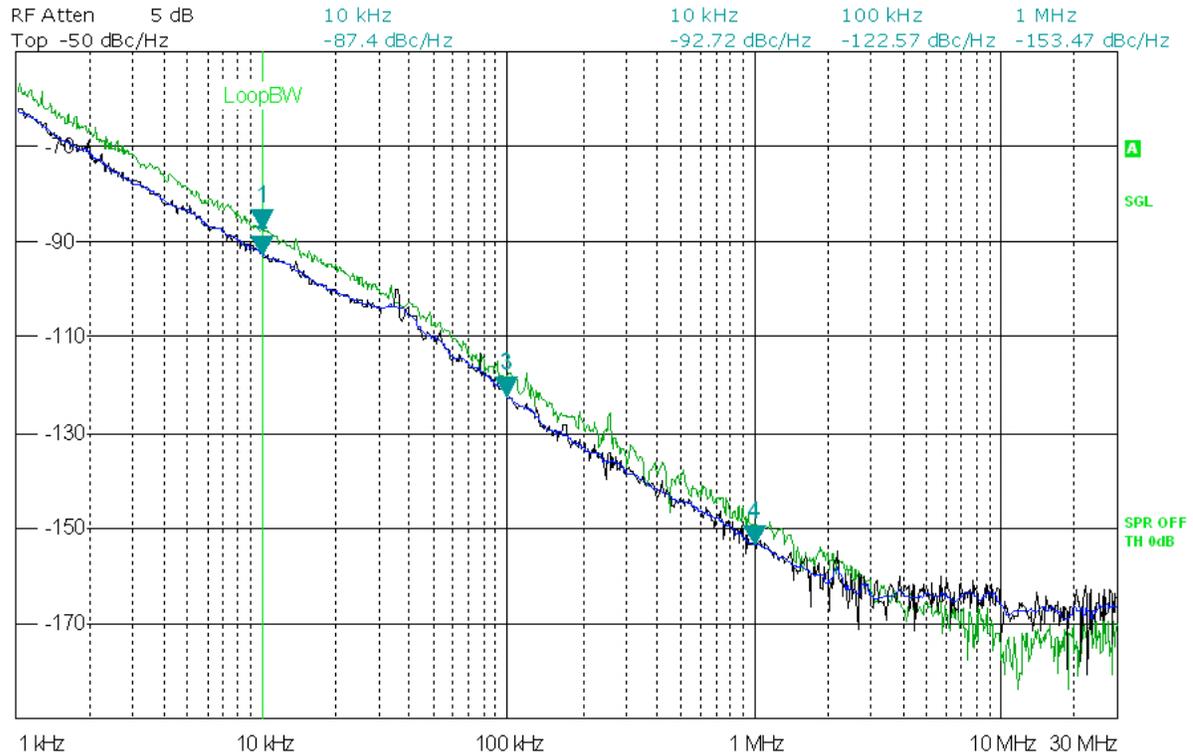


Figure 6.24: Si-GaN power oscillator phase noise comparison at 2.42 and 5.75 GHz. A 4 dB delta in single sided phase noise vs. carrier frequency is noted. Noise spectrum is predominately $1/f$ -noise in slope.

6.2.1 Si-GaN HFET power oscillator efficiency

A detailed investigation of the efficiency of the Si-GaN HFET power oscillator operating at 2.4 GHz is first conducted in simulation. Guidelines for both simulation and experiment in this work are based on developments highlighted in the appendix D, see 429. Key elements from Appendix D point to maximizing the resonator voltage and permitting this voltage to

approach twice the supply voltage, while optimizing the feedback factor. The feedback factor of the oscillator loop, must be adjusted along with the the DC operating point. In this case, adjustment in V_{gs} in relation to the pinch off voltage of the HFET. Our adjustment in loop gain was most easily accomplished by a controlled attenuator in cascade with the resonator and delay line.

The gate voltage is fixed with respect to the pinch off voltage and the gate voltage set for a quiescent current drain of 110 mA at 28 V drain voltage. Dynamic measurement probes of drain current and drain voltage are converted to RMS values and along with harmonic power spectrum readings, used to calculate load conversion efficiency. Successive simulations were run while decrementing only the loop gain. The general trend line is improved conversion efficiency with increased available open loop gain. Similar results were obtained in test but with one alteration. In one case the gate voltage is adjusted with respect to the value of the pinch off voltage, so as to optimize the efficiency at the **lowest** loop gain setting. The gate voltage is not readjusted as the loop gain is varied. A second test adjusts the level of gate voltage as open loop gain is adjusted, peaking the efficiency as feedback voltage increases with increasing loop gain. Using this method, a peak load efficiency of 40.3% at 2.4 GHz is realized and at 5.8 GHz, 26%, at an output power of just over 33 dBm. The results of measurements and simulation are shown in Figure 6.25. Simulation of load efficiency vs. open loop gain is shown for gate-to-source voltage fixed, while varying the open loop gain. Good agreement occurs at low loop gain, while increased loop gain required an adjustment in V_{GS} to match the same efficiency. Care must be exercised to avoid device thermal limits, and an external fan is operated during this measurement to prevent the loop gain from varying. In a second measurement, V_{gs} is peaked for maximum efficiency at 7 dB loop gain, and then fixed. Next, the efficiency is measured with a varying increase of open loop gain. Although at low loop gain the agreement is not as good, increased loop gain quickly tracks prior simulation and measurements. Part of the difference in agreement at low loop gain, could be accounted for by the passive circuit losses not modeled in the simulation. Therefore, the actual loop gain is somewhat lower than the amplifier alone

would provide, for example, the losses of the resonator and the coupler insertion loss.

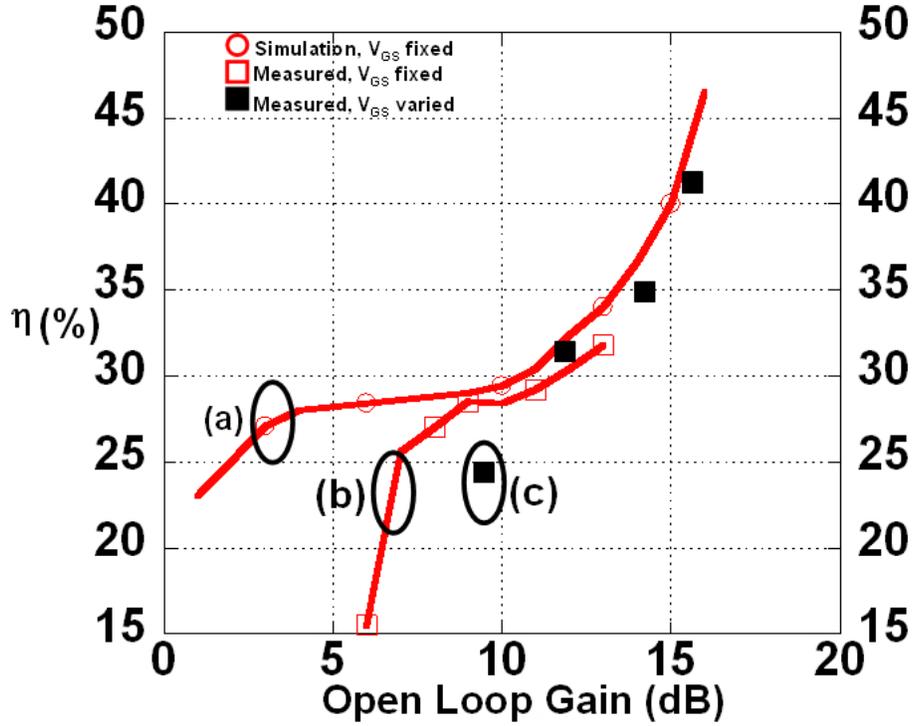


Figure 6.25: Si-GaN power oscillator load efficiency vs. open loop gain, conducted at ≈ 2.4 GHz: (a) Measurements; (b) simulation; (c) V_{GS} is varied to maximize efficiency for each setting of open loop gain.

The technique outlined here is bench marked by comparison to other GaN oscillator implementations. A figure of merit (FOM) is used which is a variation of the one discussed in [189], however with FOM targeting power oscillators. Instead of utilizing the normalized power term $P_{DC}/1mW$, we use the load efficiency since P_{out} is contained in the calculation. Therefore, the FOM used here is given as

$$FOM = CNR_{dB}^{design} + 20 \log \left(\frac{\Delta f}{f_o} \right) - 10 \log (\eta) \quad (6.21)$$

where CNR is the carrier signal-to- noise ratio of the design, expressed as a negative single-sided

phase noise value, Δf is the offset from the carrier for the CNR measurement, and is usually 100 kHz or 1 MHz, f_o is the carrier frequency, and η , the load conversion efficiency in decimal form. We applied (6.21) to 10 designs over a frequency range of 0–60 GHz and the results are graphed, as an absolute value of FOM, in Figure 6.26. In addition, the technique developed here and the FOM are applied to several MESFET oscillators [190]. The resulting efficiency, phase noise, and load efficiency commensurate with output power and operating frequency again exceeded those incorporating a MESFET device. This data is provided along with design reference matrix tables, see Tables 6.2 and 6.3. Results thus validate a straight forward design technique, which permits a high efficiency power oscillator to be realized based on an approach which first synthesizes a stable power amplifier.

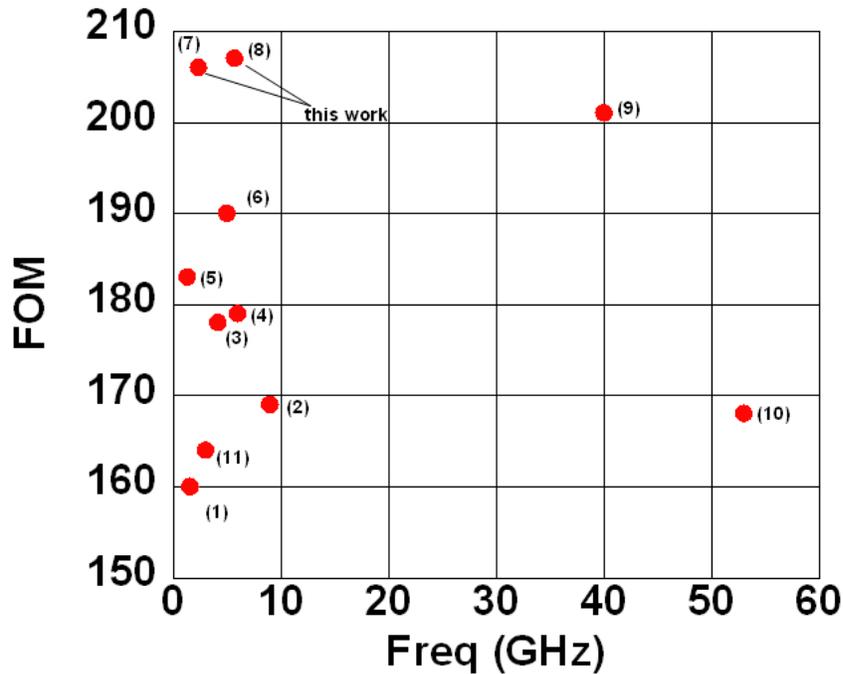


Figure 6.26: FOM for GaN power oscillators

The presence of the field plate significantly improved the phase noise of the oscillator and the breakdown voltage of the active Si-GaN HFET device [188]. Although the phase noise is

still predominately 1/f-noise, the reduction in the common source configuration we investigated here is better than 40 dB compared to our prior work. Although not all of the improvement can be assumed to be due to the addition of the field plate. Oscillator resonator loaded Q_L , is expected to be different, and if greater can partially contribute to the improved measured value.

The trend line with higher operating frequency is reduced efficiency and this is tagged to devices operating closer to their f_T mark [29]. In the case of our device, while the device in die form has measured f_T of 15–18 GHz, the packaged PSOP2 device calculated f_T is 8.6 GHz. This f_T mark is obtained from extrapolation of the h-parameters from S-parameters and finding the unity gain point of h_{21} . While the earlier work with Si-GaN HFET did not have a field plate [187], the device discussed here does. The field plate is source connected and spans half the gate-drain channel, $1.5\ \mu$. The device uses a 2 mm gate periphery consisting of 10 fingers each $0.5\ \mu$ long by $200\ \mu$ wide.

Power oscillators which are designed firstly as power amplifiers are realized at 2.4 and 5.8 GHz respectfully. Conversion efficiency, power output, and phase noise permitted a high FOM factor to be realized for both designs. Phase noise is among the lowest reported for this class of oscillator. However, this is contingent on meeting a specific tuning bandwidth and the relationships discussed in Section 2.5.2 are drawn upon to access the impact.

Table 6.2: GaN FET power oscillators, performance matrix

Performance table matrix and reference designator					
Center freq. (GHz)	P_o (dBm)	Efficiency (%)	Phase noise (dBc/Hz)	FOM	Reference
1.6	32	25.5	-81.4	-160	(1)
9	31.8	21	-77	-169	(2)
4.16	22.9	9.4	-86.3	-178	(3)
6	27	14	-92	-179	(4)
1.33	21	40.5	-97	-183	(5)
5	32.8	21.5	-103	-190	(6)
2.4	34.5	40.3	-122	-206	(7)
5.7	33	26	-118	-207	(8)
40	25	8.1	-92	-201	(9)
53	11	.53	-97 (1MHz)	-168	(10)
3	34.3	27	-80	-164	(11)

phase noise is single sided at 100 kHz offset unless noted

Table 6.3: GaN FET power oscillators, reference works

Reference table	
Reference	Notes
(1)	Victor, EuMC 2005, Si-GaN common source
(2)	Kaper, MTT-S 2004, AlGaIn/GaN HEMT common gate
(3)	Sanabria, MTT-S 2004, AlGaIn/GaN HEMT differential
(4)	Shealy, MWCL 2001, AlGaIn/GaN HEMT common gate
(5)	Kim, APMC 2006, GaN/ AlGaIn HEMT common source
(6)	Xu, MTT-S 2005, AlGaIn/GaN HEMT field plate
(7)	Victor, dissertation 09, Si-GaN HFET common source field plate
(8)	Victor, dissertation 09, Si-GaN HFET common source field plate
(9)	X. Lan, MWCL 2006, AlGaIn/GaN HEMT common gate
(10)	X. Lan, MWCL 2008, AlGaIn/GaN HEMT common gate push-push
(11)	Shealy, MTT-S 2001 AlGaIn/GaN HEMT common gate non-optimized surface passivation

6.3 Maximizing RF system dynamic range

The treatment of maximizing dynamic range of a preselector through an equal stage contribution methodology was previously discussed in Section 4.3.1. The down-converter is a characteristic design problem and the work discussed here illustrates that the approach of the stage contribution method applied to either the receive or transmit function is no different. In this treatment, conditions are simplified, as only small input signal levels are considered. No distinction between AM and PM noise is made and the operation of stages which would favor processing one type noise versus the other, as an example, through self-limiting is not considered. Clearly, as discussed in Chapter 2, these operating conditions must be considered if accurate and complete cascaded operation is required. Nevertheless, the objective of demonstrating the method of equal stage contribution, and the direction towards optimization of the cascaded dynamic range provided by the algorithm is useful. An application of the algorithm is presented using hardware which is modified as dictated by the algorithm process. Dielectric filters are re-tuned by removal of metallization and altering the coupling coefficient. The down conversion mixer is modified as required by adding DC bias to the ring-diode array and adjusting the LO input power to the mixer. Finally, the low noise amplifier is modified as required by adjusting the bias current.

A preselector down-converter with an architecture similar to that of Figure 4.1 is designed. Will omit the stage 4 post amplifier for simplicity, and consider the first four stages only, and use the balanced contribution method for the initial stage assignment. The block diagram is shown in Figure 6.27 for reference. The system operates at 1.5 GHz with a first Intermediate Frequency (IF) of 250 MHz. The system third-order input intercept, IIP3, design target is 0 dBm with a noise figure target of 10 dB. The initial stage assignments for balanced noise and IMD contributions are shown in Table 6.4. The stage assignments shown in Table 1 meet the target specifications exactly, with no single stage contributing any more than the required noise factor or nonlinear distortion. The required LNA gain is found to be low, permitting a significant reduction in mixer IP3. Conversely, the mixer noise figure could potentially be

higher than found here. With this in mind, the process of system cascade noise figure and available gain trade-offs, and a selection of actual element parameters continues.

The design proceeds with a selection of available modules for each stage and continuous, however limited variation of stage parameters is possible. For example, through bias control we can effect stage gain and noise figure. The following devices were chosen for the stages: a MMIC amplifier for stage 2 (NEC part UPC2745) and a thick film hybrid SMD mixer for stage 4 (MCL part SYM-2500). Bandpass dielectric resonator filters were chosen for stages 1 and 3. In particular, a dielectric tuned and a lumped-element Tchebychev band-pass filter with 0.1 dB ripple at 1.5 GHz was used to provide prescribed loss in stage 3, and this proved to be important in establishing balanced stage contribution and improved dynamic range.

Continuous control parameters included controlling the mixer IMD contribution, by changing the LNA gain which is prior to the mixer. The LNA performance is readily altered through bias control. Changes in the operation parameters of the mixer IIP3, are possible by varying the LO drive level, and operating the mixer in a “starved LO” configuration. This starved LO configuration is readily configured in the ring mixer by adding a small DC voltage across the diode array in conjunction with the LO RF voltage. The tuning of the stage 1 and 3 filter is accomplished by a trim of the resonator length and controlling the filter coupling. All of these variable elements were investigated under the guidance of an equal contribution methodology. Table 6.4 provides data based on the initial contribution and a progression of the designs. The noise and distortion contributions of each stage with the initial stage assignment, initial MMIC performance, and optimized design are shown in Figure 6.28 and Figure 6.29. Figure 6.30 depicts the dynamic range as calculated using the definitions for SFDR. Based on the balanced contribution method, the SFDR is 109.5 dB normalized in a 1 Hz bandwidth. The initial value provided by the devices selected is 108 dB. After appropriate trade-offs and adjustable losses in stage 3, the final dynamic range achieved is 111 dB. The design is facilitated by monitoring the SFDR continuously throughout the process. Now, the same system design could be achieved using budget assignment, however with much greater design effort.

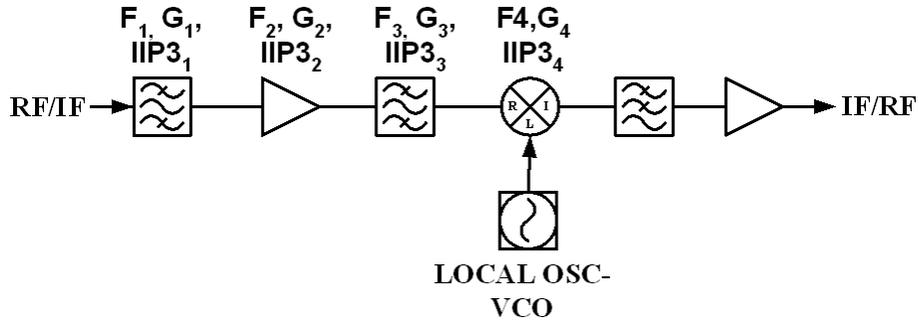


Figure 6.27: RF preselector cascades are configured by the mixer application, either down conversion for the receive or upconversion for the transmit function.

Table 6.4: Cascade-stage assignment based on balanced contribution

System Cascade Parameters						
stage n	description	Gain _i (dB)	NF _i (dB)	IIP3 _i (dBm)	Gain _i	F _i
1	Bandpass Filter	-3.97	3.979	99	0.4	2.5
2	RF Amplifier	1.761	3.01	.969	1.5	2
3	Bandpass Filter	-3.97	3.979	99	0.4	2.5
4	Balanced Mixer	-	2.041	-3.18	-	1.6

NOTE: In some cases there is no contribution or it is not required.

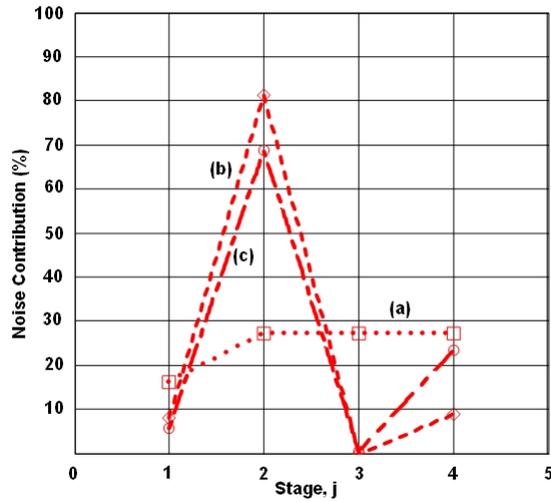


Figure 6.28: Noise-figure contribution: (a) initial calculation of balanced noise figure contribution; (b) measured MMIC contribution under nominal operating contributions; (c) and final settings after altering bias, filter loss, and mixer LO drive levels for improved dynamic range.

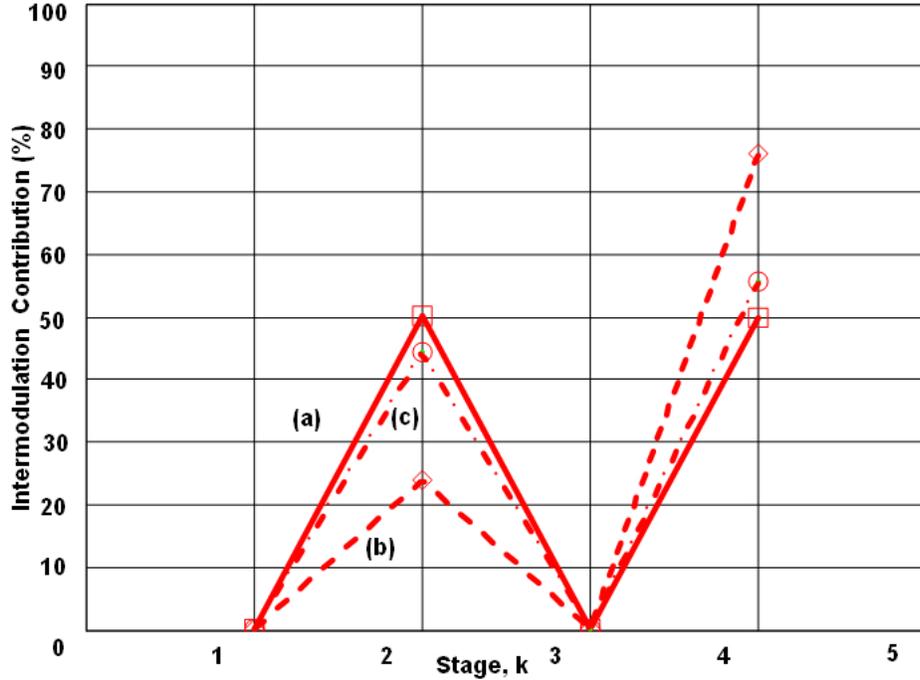


Figure 6.29: Input intercept (IP3) contribution: (a) initial calculation; (b) original measured MMIC devices; and (c) final performance after alteration of bias, LO drive, and filter loss adjustment in stage 3. Final settings in (c) led to highest dynamic range for the MMIC set chosen.

The method discussed here is based on a stage contribution technique and is useful for assessing the performance requirements in receiver and transmitter cascade design. Compared to a budget-analysis method, a contribution technique permits better initial insight into appropriate distribution of stage gain, loss, noise, and distortion in order to meet a particular target specification and indicates the trade-offs involved in design. The balanced-contribution assignment defines a system that meets the noise-figure target value exactly, albeit with no system margin. Specifically, the gain assignments are exactly the minimum required to meet the system goal, and no excess gain, which would tax linearity requirements and increase power consumption, are necessary. Thus, the contribution approach highlights the minimum required stage intermodulation performance and serves as a good baseline for trade-off analysis. The validity of the method has been demonstrated by the design of a receiver down-converter.

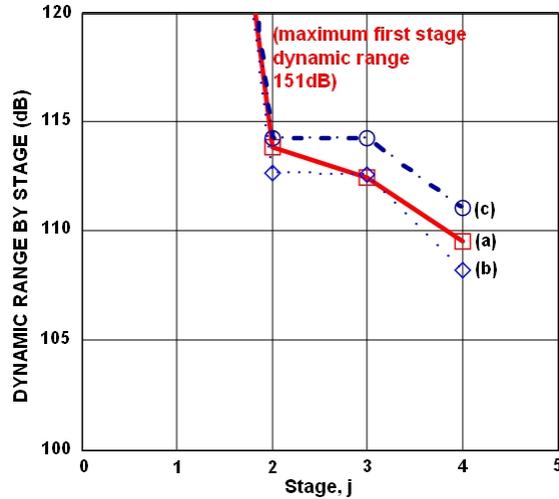


Figure 6.30: SFDR by stage: (a) initial assignment; (b) initial system performance after selection of modules but before optimization; (c) final performance after setting bias, LO drive, and filter loss in stage 3.

The contribution technique is particularly insightful if applied to complex systems. It is virtually impossible to judge the effects of single or even multiple changes in parametric blocks in a cascade system. For example, in complex modulation systems such as QAM, the use of voltage controlled attenuators, variable gain amplifiers, and fixed loss pads are scattered throughout the cascade. The purpose of these attenuators is to control gain and power output distribution throughout the cascade, while maintaining linearity and compensation for changes in stage performance due to changes in temperature, frequency, or modulation format. Monitoring power levels is conducted through a directional coupler via an ALC (automatic level control) port, and microprocessor control with algorithm is used to control a feedback voltage to set the various gain and attenuator settings throughout the system.

This section discusses in more detail the calculations for a 15 GHz transmitter cascade. The application of the contribution concept to assessing the signal-to-noise plus distortion is highlighted. The system consists of gain blocks, attenuators, an up conversion mixer, filters, and a power amplifier. In lieu of using an Excel spread sheet, a Mathcad script is written to find the total output noise power of the system and the distortion via the third-order output

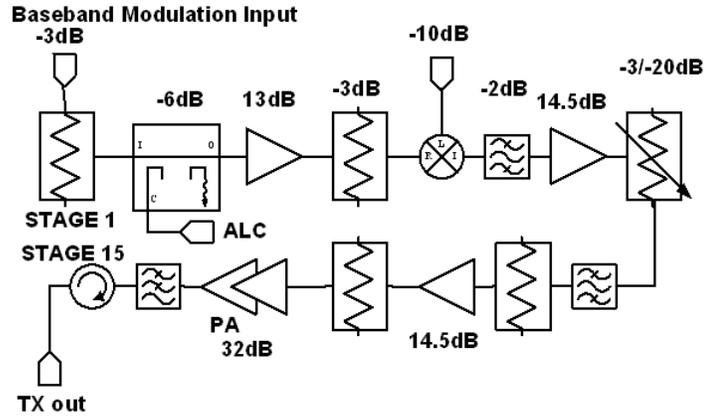


Figure 6.31: The 15GHz transmitter cascade. Up-conversion mixer stage 5 is treated as a single response element. PA driver stage 11 and PA stage 13 are most prevalent contributors to noise and distortion. Stage 8, variable attenuator is used to control output power and linearity.

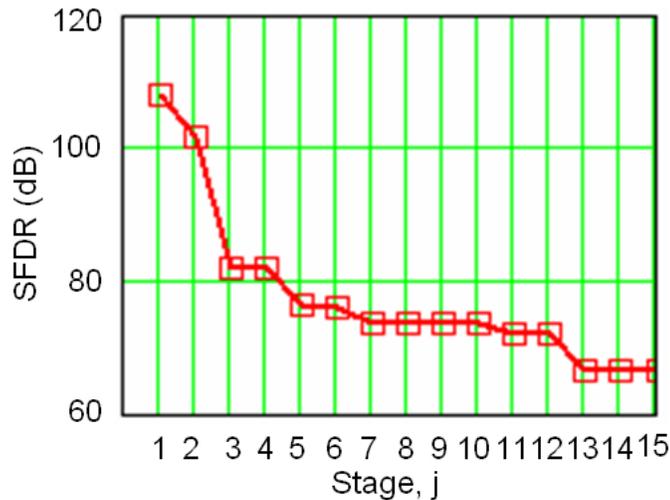


Figure 6.32: The SFDR for a 15 GHz transmitter cascade. Range value extends from stage 1 at the IQ modulator port introduced at the IF to Stage 15 at low pass filter PA-Circulator output.

intercept. Each stage noise and intermodulation contribution is graphed along with the spurious free dynamic range for the transmitter cascade, providing a means of visualizing the effects of gain, noise, and linearity distribution. A review of the fundamentals used in this analysis are treated in several parts. This is followed by the analysis results from the Mathcad routine. The approach outlined is applicable to receiver and transmitter lineups. The equations developed

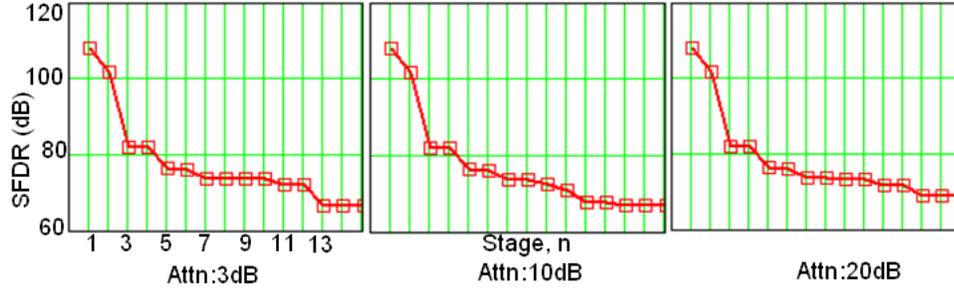


Figure 6.33: The SFDR for the transmitter cascade for 3 attenuator settings. Ideal case results in an SFDR that is maintained constant regardless of the attenuator setting. In this system, despite the significant change in gain, the dynamic range remains at approximately 70 dB.

assume a small signal analysis. Firstly, will identify the excess noise of attenuators, then the amplifier, and finally multi-response elements; the mixer, all applied in cascaded systems. A table for gain, noise figure (dB) and input intercept is listed, see Table 6.5. Additional tables may be added to provide a double check with output intercept and P_{-1} dB. The stage numbering is from the first stage prior to up conversion through the power amplifier and ending with the circulator at stage 15. We note that the power amplifier has the largest contribution to third-order intercept, IP3 degradation, while the up-converting mixer is next at 10%, see Figure 6.34.

The two ports considered and the main parameters that are available are the power gain, noise factor, and distortion. The two-port amplifier is fundamentally single signal in nature, unlike the mixer, which is a “multi-response” three-port. For this discussion, we will limit the analysis to network systems such as amplifiers and attenuators.

The definition of the available power gain (G_{av}) of a two port and the definition for noise factor are key for a two-port noise analysis. When a load is conjugate matched to a source, the power delivered to that load is called the available power from the source. When the two-port is conjugately matched simultaneously at its input and output ports, the power gain is called the available power gain. The noise power P_n is defined by the rms thermal noise voltage V_n of an internal resistance R_s associated with the source. The noise voltage is a function of R_s and the ambient temperature T in degrees Kelvin. When the source is matched to a load via a

Table 6.5: 15 stage 15 GHz Transmitter cascade

System Cascade Parameters				
Stage n	Description	Gain (dB)	Noise figure (dB)	Distortion (dBm)
1	IF attenuator	-3	3	48
2	IF coupler	-6	6	51
3	IF amplifier	13	4	13
4	IF attenuator	-3	3	48
5	up-converter mixer	-10	10	17
6	RF bandpass filter	-2	-2	47
7	RF buffer amplifier	14.5	5	12.5
8	RF variable attenuator	-3	3	28
9	RF bandpass filter	-2	2	47
10	RF attenuator	-3	3	48
11	driver amplifier	14.5	5	12.5
12	attenuator	-3	3	48
13	power amplifier	32	7	12
14	RF low pass filter	-0.4	0.4	60
15	circulator	-0.5	0.5	60

Note: stage 8 also set to -5,-10,-20 dB attenuator setting

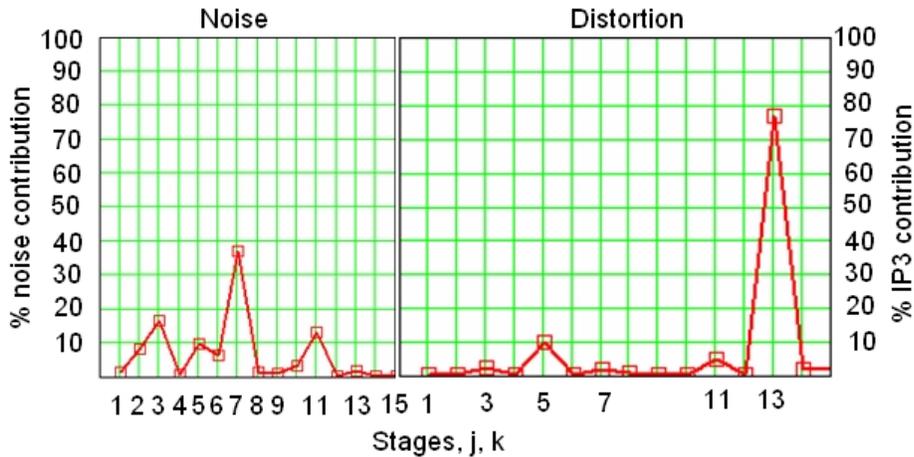


Figure 6.34: The noise and distortion stage-by-stage contribution with stage 8 attenuator set at gain=-5 dB. The up-converter mixer stage is 5, stage 7, pre-driver amplifier, stage 13 the power amplifier.

lossless matching network with noise bandwidth B , and $R_L = R_s$, the voltage divider provides a noise power, P_n given as

$$P_n = \left(\frac{V_n}{2}\right)^2 \frac{1}{R_L} \quad (6.22)$$

where V_n is given as

$$V_n = \sqrt{4kTR_sB}. \quad (6.23)$$

After substitution of V_n and with $R_s = R_L$ we have the noise power independent of the resistance and P_n is given as

$$P_n = kTB. \quad (6.24)$$

Therefore, the available noise power, kTB watts, is independent of the actual value of R , so long as a conjugate match is maintained between the source resistance and the load resistance. The noise factor F , is defined at a specific frequency and is independent of the termination resistance. Thus, $F \equiv \frac{\text{output noise power of the actual noisy system}}{\text{output noise power caused by thermal noise in the source resistance at T}}$. The value of P_n provides the denominator of F , and if the matched two port has available power gain G_{av} , then the denominator is given by $P_n \cdot G_{av}$. The noise power P_n , is given by kTB , and is available from any resistive source expressed as N_i . Then the output noise power is $G_{av} \cdot N_i$. Using this notation, the numerator of F is simplified to just N_o .

The value of F is then expressed as

$$F = \frac{N_o}{GN_i}. \quad (6.25)$$

The available power gain G_{av} , is the ratio of the signal output power to the input power or

$$G_{av} = \frac{S_o}{S_i}. \quad (6.26)$$

After substitution for F , we obtain the familiar definition for the noise factor F , as a ratio of ratios; namely the signal-to-noise ratio or SNR of the input divided by the SNR of the output and

$$F = \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}}. \quad (6.27)$$

Now N_o is separated into two components, one associated with the input noise power, $G_{av} \cdot N_i$ imposed by the source, and the other imposed by thermal noise power associated with

the remaining system noise, N_s . Then F is rewritten as

$$F = \frac{N_i G_{av} + N_s}{N_i G_{av}}. \quad (6.28)$$

Since G_{av} , N_i , and F are either known or measured parameters, the thermal noise power that the system contributes; N_s is found from

$$N_s = (F - 1) N_i G_{av}. \quad (6.29)$$

The noise power N_s is the excess noise above and beyond that contributed by the source alone. The term $(F - 1)$ is referred to as the excess noise power contribution. In cascaded systems each successive n^{th} stage will contribute a noise term of $(F_n - 1)$ and each term will be multiplied by all $(n - 1)$ following stages of gain or attenuation. For example, consider a three-stage cascade. The total excess output noise power is given by

$$N_s = (F_3 - 1) N_i G_{av3} + (F_2 - 1) N_i G_{av2} G_{av3} + (F_1 - 1) N_i G_{av1} G_{av2} G_{av3}, \quad (6.30)$$

Depending on the available gain or loss distribution in the cascade, the total output noise power will always be in excess of N_i or kTB . If there is significant gain followed by much more significant loss, then the total output noise power could approach kTB . For example, consider a matched attenuator which is a passive network with numeric loss $L > 1$ and or gain $G = 1/L$. Because the attenuator is matched, the thermal noise power delivered to R_L is the available power kTB . The output noise provided by the source, R_s , is the available noise power kTB times G . Therefore, the noise factor of a lossy passive network is $F = \frac{kTB}{kTBG} = \frac{1}{G}$.

Consider the excess output noise of a single attenuator with $F = 1/G$, we have, $N_s = (1 - G)kTB$. The excess output noise power for large attenuation is therefore bounded by kTB .

Next consider, the amplifier and mixer. Gain stages are handled in a similar manner as

the attenuator. In this situation, noise output power is increased by the sum of all forward gain. In the case of the attenuator, noise power is reduced however, to a level no less than kTB . Mixer noise factor is assumed signal sided and the noise figure of the mixer is specified as a single sideband (SSB) noise factor. Sufficient filtering at the image frequency of the mixer will guarantee that the noise factor is single-sided. For example, a 6-dB rejection at the image frequency will permit the noise figure of the mixer to approach the SSB value to within 1 dB.

In the Mathcad script all noise and distortion is referred to the last stage in the transmitter. As this noise is calculated, the routine keeps a tabular check on each stage noise contribution relative to the total. The same is true with distortion. Distortion calculations are based on the correlation of the two tone IMD performance of active devices with their P_{-1dB} value. Amplifiers and mixers take on a user input value for the correlation of P_{-1dB} with the intercept point. A nominal value is 10 dB, whereby the intercept point is taken 10 dB above the P_{-1dB} compression point. Passive elements, filters, and attenuators are assumed to be free of intermodulation. If this is not the case, then the appropriate correction for their IP3 must be made. Then the third-order input intercept value, IIP3, is related to the third-order output intercept, OIP3, through the relation $OIP3 = IIP3 + \text{available gain}$, cited earlier.

Given the total output noise and the intercept value, the spurious free dynamic range of the transmitter line up is set. This is not unlike the receiver, except the minimum noise level and distortion is referenced to the output not the input of the cascade. The stage contribution data plot provides a clear picture of the offending stage performance. In other words, which stage or stages in the cascade dominate the reduction in performance. Calculations for noise and distortion contribution will provide a clear view of which stages tend to raise the total noise figure or distortion compared to all other stages in the cascade. Redistribution of gain, noise, or distortion will alter this picture. Will now discuss the method for finding the noise contribution.

First, each stage gain is converted from dB to numeric. Second, the total accumulated

numeric gain is found from the product of all n stage gains and is expressed as

$$G_j^{\text{accum}} = \prod_{j=1}^n G_j^{\text{num}} \quad (6.31)$$

where all the individual gain elements are in an array j . Third, the gain term and hence the noise contribution of any stage is found from the accumulated gain up to and including stage j and dividing the result into the noise factor of stage j less unity. Finally the contribution of stage j is found by dividing this result by the total noise factor F_T . Therefore, the stage noise factor contribution is defined as

$$F_j^c = \frac{(F_j - 1)}{\left(\frac{G_j^{\text{accum}}}{G_j^{\text{num}}}\right) F_T}. \quad (6.32)$$

Another interpretation to the contribution concept and approach, with regard to noise power, is to consider the cumulative available power gain of all prior stages. If we consider the cascade noise formulation of (4.1) again, and subtract one from both sides we have,

$$F_T - 1 = F_1 - 1 + \frac{F_2 - 1}{G_{1\text{av}}} + \frac{F_n - 1}{\prod_1^{n-1} G_{n\text{av}}}. \quad (6.33)$$

Therefore, $\frac{F_n - 1}{\prod_1^{n-1} G_{n\text{av}}}$, becomes a specification of importance for a given stage in the cascade. In words, the ratio of the total noise factor less unity to the total “prior” available power gain becomes the specification of importance for each stage. Reference to Figure 6.35 illustrates that in the context of the noise figure definition of a single stage, such a specification makes sense. A noisy amplifier is modeled as a noise free network, with an additive noise power of $(F-1)kTB$, and is the noise contribution of that specific stage.

The distortion and intermodulation contribution are calculated in a similar manner. The intercept method is used and may be referred to the input or output. For input referenced IP3, the value of each stage past the first is referenced to the input of the first stage. Adjustments

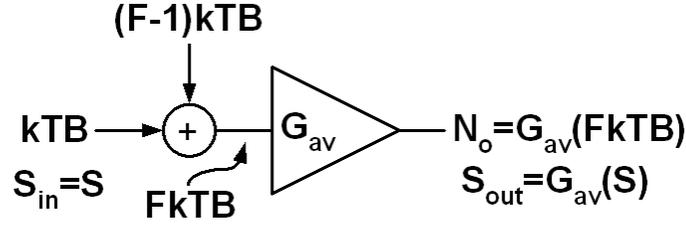


Figure 6.35: A noisy amplifier is modeled as a noise free amplifier with an input noise power of $(F-1)kTB$. This model provides the notion of noise contribution.

for gain, loss, or selectivity are made at each point along the cascade. Hence,

$$IP3_k^{\text{ref}} = IP3_k^{\text{dBm}} - \sum_{j=1}^{k-1} G_j^{\text{dB}}. \quad (6.34)$$

The first stage IP3 is simply referred to itself. Therefore,

$$IP3_1^{\text{ref}} = IP3_1^{\text{dBm}}. \quad (6.35)$$

All IP3 values are converted to numeric and then the total IP3 is found simply from the inverse of the sum of the reciprocal IP3 values. Hence,

$$IP3_k^{\text{ref.numeric}} = 10^{\frac{IP3_k^{\text{ref}}}{10}}. \quad (6.36)$$

Therefore,

$$IP3_T = \frac{1}{\sum_{k=1}^n \frac{1}{IP3_k^{\text{ref.numeric}}}}. \quad (6.37)$$

Finally the contribution of each stage distortion in terms of IP3 is compared to the total. These calculations again assume the worse case addition of distortion terms. Also it is assumed that the IP3 tracks the predicted IMD and P_{-1} dB correlation throughout the cascade. In some instances the IMD could be a better value to judge distortion and then conversion to IP3 is made and the same sequence is used as outlined above. In the final analysis, more precise

non-linear metrics should be used if available, such as AM -to-AM and AM-to-PM conversion and the effect on modulated carrier, for example the QAM constellation. Finally, the IP3 contribution is defined as

$$IP_3^c = \frac{IP_3^T}{IP_3^{\text{ref.numeric}}} \cdot \quad (6.38)$$

A transmit cascade is arranged in a Mathcad script. The entries are in a tabular array and the values are operated on by the cascade noise and distortion equations.

A set of graphic plots provides a clear picture of the design trade-off and points to stages in the cascade, which can contribute significantly to performance change. In dealing with signal-to-noise ratio in a receiver, we normally refer all calculations to the input stage. The same approach may be applied to the transmit cascade, since the output performance is related to the input through the linear available gain. Nevertheless, we calculate both input and output distortion levels, third-order intercept, and keep track of each stage contribution as we migrate these intercept numbers through the cascade and modify their values by the appropriate cascaded gain and loss. The two-tone intercept values may be obtained directly from the manufacture data sheet, P_{-1} dB measurements, or correlations may be used between the intercept point and the point of 1 dB power compression. In the examples outlined here, we have used a 10 dB correction factor to predict a stage intercept level from the measured 1 dB compression point. This is a generalization, and is obtained from a mild non-linear describing function of the form

$$v_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 \quad (6.39)$$

where only the first three terms of a power series expansion of the input signal v_i are retained. If input signal v_i is expressed as a sinusoidal voltage, we can expand the function (6.39) and find a relation amongst the power series coefficients, k_n , $n = 1, 2, 3$, the 1 dB compression point, and the intercept point, see [162]. The exact value obtained for this mild nonlinearity and assuming a perfectly matched device is 10.643 dB, see again [162]. Note, the value listed in [162] is in error. However, we warn that this value must be checked, as many devices can provide a

significantly higher extrapolation point; a 12 to 20 dB relationship between the intercept point and the 1 dB power compression point is not uncommon. Also, the actual statistics of the modulation signal are not accounted for in these calculations.

The Mathcad script provides the following data and graphical plots: First, total noise figure and noise figure contribution in relation to the total noise power are provided for based on a stage-by-stage contribution. Second, total intermodulation distortion and IIP3 contribution, again based on a stage-by-stage contribution calculation. Third, total excess noise power output on a stage-by-stage basis. Fourth, spurious free dynamic range, which is a measure of the difference between the noise floor at a given point in the cascade and the intercept at that same location. This provides a benchmark in estimating compliance to meeting a telecommunication spectral emission template, for example the European Telecommunications Standards Institute, [163]. The bandwidth used in calculation is input to the Mathcad script and should match the same bandwidth used in the emission test or required by the modulation bandwidth. The relevance of the fourth item, is based on the fact that for a signal to be detectable, the signal output power level must be above the level of thermal noise power. Also, the dual requirement, in the transmitter function we must meet acceptable alternate and adjacent channel noise power. The higher the noise power level is, the higher the input signal required to obtain a predetermined signal-to-noise ratio. However, in the transmit function, the signal power is limited by regulatory requirements. In addition, increased signal power in turn increases the third-order intermodulation distortion. If the third-order intermodulation product level is set equal to the noise level, then the dynamic range is established. Raising the noise level or lowering the intercept point leads to a signal-to-noise ratio reduction, and possible non-compliance to the telecommunication authority emission level. The calculation is an estimation, in so far as the true modulation is complex, and not simply two-tone. However if the two-tone dynamic range is not at least compliant with the emission limits, it is unlikely that the statistics of the complex modulation are going to be favorable. Next we present the Mathcad graphics.

The set of graphs presented demonstrate the results for attenuator settings of -3 , -10 ,

and -20 dB for stage 8. The listing of noise, gain, input intercepts, the corresponding output intercepts, and P_{-1} dB compression point are also provided. It is interesting to note the change in the performance as a function of attenuator settings. For example, if the particular attenuator stage 8 is at a setting of -5 dB, the second amplifier, stage 7, has the largest noise contribution in the cascade, see Figure 6.34.

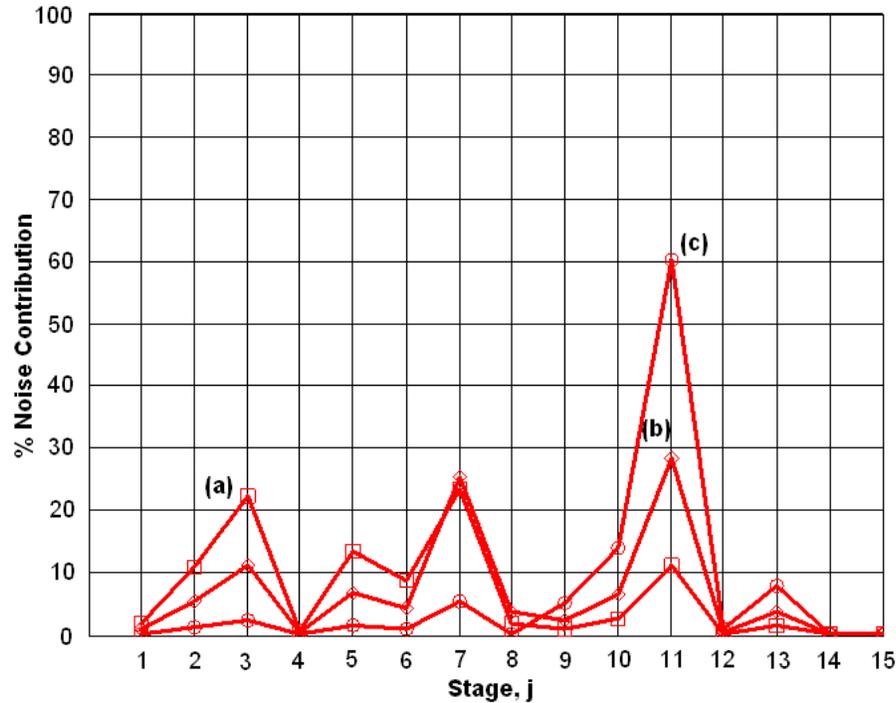


Figure 6.36: The noise figure stage-by-stage contribution with stage 8 attenuator set at gain values: (a) -3 ; (b) -10 ; (c) -20 dB.

The stage numbering is from the first stage prior to up-conversion, through to the power amplifier, and ending with the circulator at stage 15. Here it is noted that the power amplifier had the largest contribution to IP3 degradation, while the up-converting mixer was next at 10%, see Figure 6.34.

We recast this graph totally in terms of third-order output intercept, referred to the output, see Figure 6.37. It is clear from this graph how the mixer, stage 5, follows behind the power

amplifier, stage 13 in distortion contribution. While other stages are significantly less. Cascaded excess noise output power is plotted on a stage-by-stage basis, see Figure 6.38. The final level is shown at -68 dBm with the noise equivalent bandwidth set at 100 KHz. Third-order output intercept at each stage is presented on a stage-by-stage basis, see right Figure 6.38. When this is combined with the excess noise output power, the SFDR and an approximation to the emission template is created. This particular line up shows a two tone OIP3 of 42 dBm, see panel Figure 6.38 right.

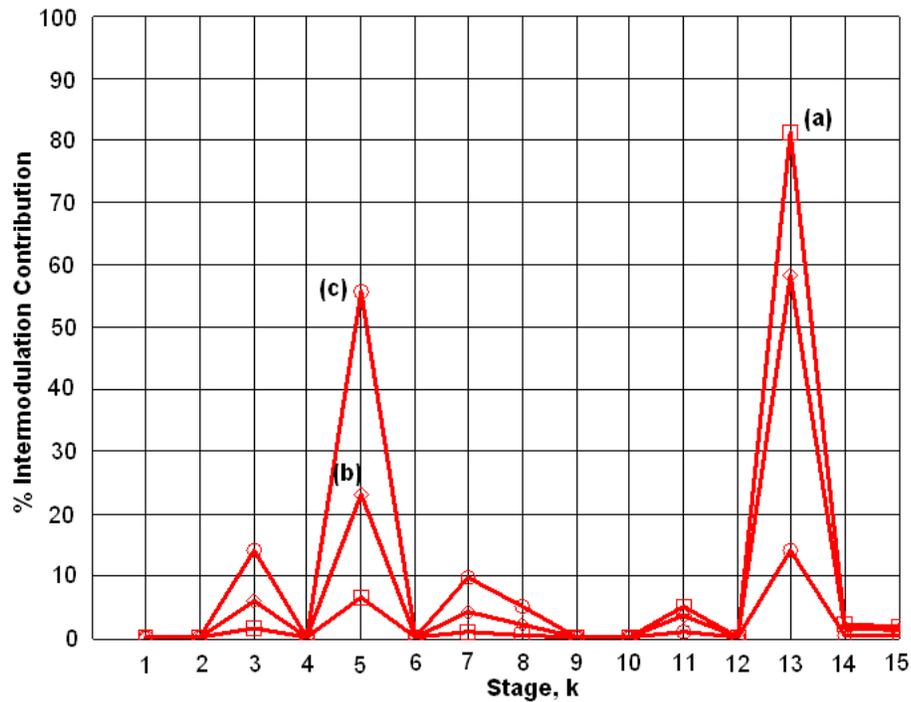


Figure 6.37: The distortion from IP3 on a stage-by-stage contribution with stage 8 attenuator set at gain values: (a) -3 ; (b) -10 ; (c) -20 dB.

The final signal to distortion ratio is 75 dB, see Figure 6.32, and is in essence a composite graphic of both panels in Figure 6.38. Comparison to an emission template, such as ETSI, implies that this cascade should provide greater than 10 dB of signal-to-noise margin in relation to the specification. In the previous figure panel, see Figure 6.33, we presented the trend of

the cascade performance as a function of the attenuator settings of 3, 10, and 20 dB. Although the noise and distortion contributions vary widely through the cascade system, the SFDR is insensitive and remains virtually constant. In a properly designed cascade system, this is the desired outcome. Although the noise power through the system may vary widely, by the appropriate placement of attenuation and prior gain and loss distribution, the distortion level will migrate in a manner that maintains the desired signal-to-noise ratio.

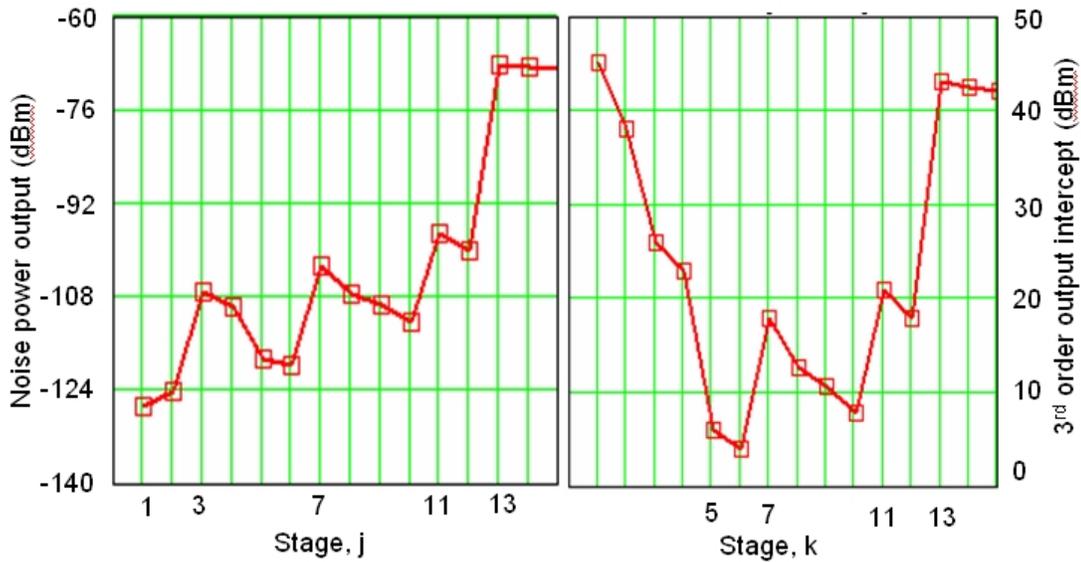


Figure 6.38: The stage by stage noise power output in dBm (left) coupled with the total output intercept accumulated at each stage (right), provides a dynamic range picture throughout the cascade. See Figures 6.32 and 6.33

6.4 Conclusions

It is clear from the representative plots that the distribution of noise and distortion varies as a function of the calibration attenuation setting. Noise figure contribution is significant from stages 7, and 11, and distortion contribution from the power amplifier at stage 13, as the attenuation values vary. The mixer conversion loss at stage 5 is not nearly as significant due to

prior amplifier gain. From a distortion perspective, the mixer and power amplifier are the largest contributors with their contribution varying, as the attenuator level is reset. It is interesting to note how the distortion migrates from low to high attenuator settings; first from the power amplifier then to the mixer as the attenuation value increases. Despite the alteration in the noise and distortion throughout the cascade, the system dynamic range remains reasonably constant and implies at least from a signal plus noise and distortion perspective, that the emission mask should be met for this line-up. Slight improvements may be possible in redistributing the gain-loss, however the predominant limits are the power amplifier and up conversion mixer, and to a lesser degree the remaining buffer amplifiers and low level drivers.

With respect to the oscillator work, we confirm a workable solution to high efficiency power FET oscillators by utilizing a class A power amplifier design approach, maximizing available voltage supply and current excursions without voltage clipping or current saturation. The design of the resonator is applied to a synthesized power amplifier network after proper selection of the load termination network. Subsequently, a confirmation through stability analysis must validate that only a single stable point of oscillation exists at each frequency point. Optimization of the gate voltage relative to the pinch off voltage, and the available open loop gain, maximizes the conversion efficiency. Over 40% efficiency is realized at 2.4 GHz, at an output power of approximately 3 W.

Chapter 7

Applied Measurements and Theory to Noise and Components

In this chapter we lay the ground work for the measurement of noise in devices and networks, and the electrical characterization of components. The potential excess noise of the BST varactor is investigated. While accurate measurement systems and techniques often exist, we however were compelled to look at simplified techniques and measurement analysis. This motivation is partly due to first, the difficulty in providing an in-situ measurement condition, and second, the inability of providing the desired measurement with the equipment at hand. Generally this is due to the inability of fitting a slight variation of a specific measurement to a task, however that small variation in the measurement task introduces a significant error. A case in point is the measurement of phase noise of drifting oscillators. A number of research publications have reported fanciful measurement results, which were seriously jeopardized due to the misapplication of the spectrum analyzer. Other measurements include microwave device noise figure without the assistance of a noise figure test set, however a spectrum analyzer is capable of such a measurement and quite accurately. Similar parallel issues abound for passive devices. In this first section we address the measurement of capacitance and unloaded Q accurately by the application of straight-forward impedance measurements. Then we follow this section with

a number of unique approaches to the measurement of noise of active and passive networks. These measurements include the ability to capture the noise of vibration sensitive or drifting oscillator sources, low frequency noise, and active device small-signal noise figure.

7.1 Characterization of varactor Q and C ... addressing a measurement problem

Key to maximizing the resonator loaded Q is maximizing the unloaded Q prior to device embedding. Accurate oscillation frequency and tuning gain predictions require the BST varactor capacitance to be known accurately, particularly at the intended frequency of operation; this includes secondary resonant effects due to packaging and mounting of the BST die. In this section, we develop a number of measurement techniques for the characterization of varactor Q and the accurate measurement of capacitance and Q with frequency. We find that separate measurement techniques are required as one alone is insufficient to maintain the desired accuracy. A calibration technique applicable to both vector network analyzers and impedance analyzers is a SOL, (short, open, load) method. However, the calibration and measurements are performed in situ. The important key point is that in situ requirements provide a measurement which represents the device in the actual application. This is particularly the case when the measurement of the varactor Q is desired. As an example, measurement of a varactor attached to an Alumina substrate makes no sense, if the intended application is on a much lossier substrate material.

Measurements of unloaded Q are supported by a variety of established techniques and the use of the vector network analyzer, impedance analyzer, and Q -meter are documented, [107, 108, 109]. An interesting limitation in all these techniques is the problem of measuring in situ environments. This is partly the commonly occurring problem of establishing a non coaxial measurement reference plane. In addition the complexity of the package interface forces a connectivity limitation that further aggravates the problem and can introduce significant

error. For example, consider the need to measure a varactor with 2 pF of capacitance at 100 MHz. If the varactor Q is only 50, the required fixture series resistance must be less than one-tenth of the resistance of the device under test so that the deembedding of the fixture loss is not necessary. Then R_s must be less than 1.6Ω . As the frequency increases and with increased size varactors and the larger associated capacitance, the problem escalates.

In this work a straight forward technique permits calibrated in situ measurements. In addition, a convenient and improved accuracy in characterizing the capacitance is discussed and applied to a fixture connection attached to an impedance analyzer.

For Q measurements, a resonator is formed using the varactor under test in conjunction with a high Q solenoid air inductor. Depending on the value of the capacitor, its reactance and Q , either a parallel or series L-C network is used. If the measurement for a small capacitance is desired, the R_p is the significant contributor to Q and therefore, a parallel tuned network is appropriate. For moderately larger capacitors, R_s is the key element and Q measurements are best accomplished with a series resonant network.

First, a solenoid inductor is optimized for Q commensurate with a high self resonant frequency by adjusting the inductor form factor, length/diameter ratio and pitch or turns per inch. These techniques are well documented in the text by Grove [110] and [111]. Although deembedding is required, the error in this process is minimized by having a low loss inductor. The measurement can use a RF voltmeter, spectrum analyzer with directional coupler, or a vector network analyzer (VNA). If a signal generator is available, then a standard receiver, either AM or FM is used in lieu of the RF voltmeter since the signal-to-noise ratio is readily available at the audio transducer output. All of these devices provide a means of measuring a carrier notch level as the $L - C$ network is formed into a trap or bandstop filter. The depth of the notch is directly linked to the Q of the varactor as the notch is directly correlated to the series resistance of the varactor and therefore Q . Figure 7.1 shows the test set, while the condition of resonance and the notch depth is illustrated in 7.2.

An important first step is to determine the quality factor of the inductor. Clearly, accurate

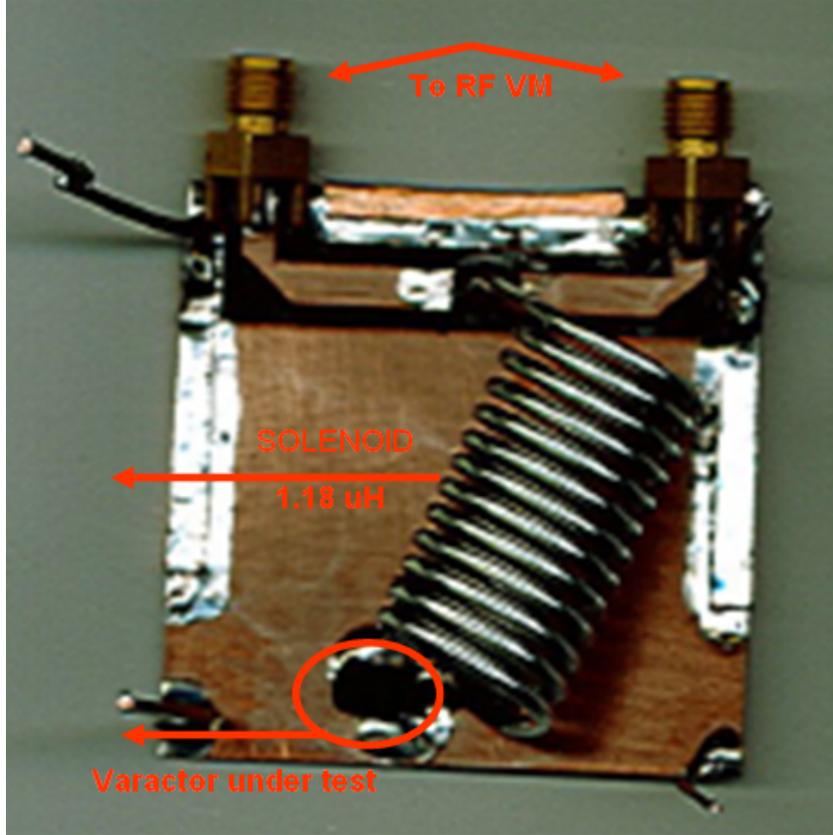


Figure 7.1: Varactor Q Test set based on series resonance measurement.

unloaded Q measurement of a device under test is limited by the unloaded Q of the test inductor. In the test set we need to establish the series equivalent R_s of the solenoid, the varactor is replaced by a porcelain capacitor, an ATC 180R 5.1 pF is used [112]. This unit has an estimated Q of greater than 5000 and consequently adds less than 50 m Ω of series resistance. The depth of the notch is given by,

$$V_{\text{atten}} = 20 \log \left(\frac{R_x}{2R_x + 50} \right) - 20 \log (0.5) \quad (7.1)$$

where R_x is the unknown series resistance associated with the lossy varactor and attenuation is expressed in dB as $20 \log (V_{\text{atten}})$. The additional $20 \log (0.5)$ is required since in the limit as $R_x \rightarrow \infty$ the finite notch depth must approach -6.02 dB. Since the inductor self resistance is

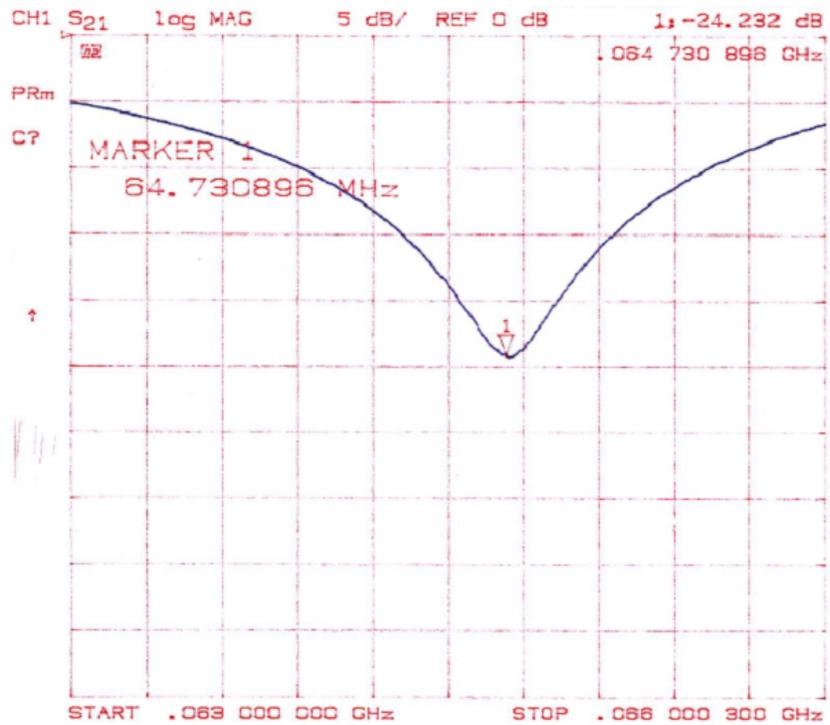


Figure 7.2: Measured S_{21} vs. frequency. The notch depth is indicative of an R_s of the inductor of 1.6 ohms at 64.7 MHz

1.6 ohms, this value must be removed from the element under test.



Figure 7.3: Packaged BST-IDC varactor for measurement as one port with VNA.

A packaged BST-IDC (interdigitated capacitor) varactor, see Figure 7.3, is added next and

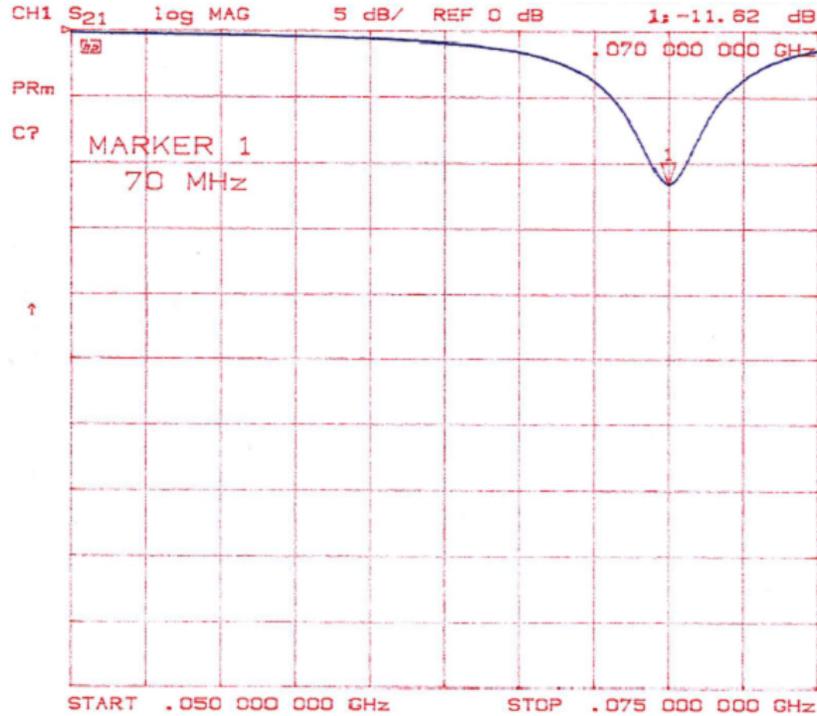


Figure 7.4: The series resonance of the packaged BST-IDC varactor with solenoid inductor, 70 MHz.

the swept resonance response is shown in Figure 7.4. Based on the notch depth of -11.52 dB, the series resistance from this measurement using (7.1) is found to be 8.89Ω . After deembedding the 1.6Ω of the solenoid, what remains is 7.29Ω for the BST-IDC varactor. The computed Q therefore, at 70 MHz for the BST-IDC varactor is 62. This measurement is conducted with an applied bias voltage of 25 volts. An expression for Q as a function of frequency that applies to lumped elements is $Q(f) = \left(\frac{f}{FQ}\right)^\alpha$. If we assume a linear Q frequency model, $\alpha = 1$, then at 10 MHz Q is 434 which is in good agreement with low frequency measurements conducted directly on an impedance-analyzer, but not particularly in good agreement with direct VNA measurements, shown in Figure 7.5.

At 70 MHz reasonable agreement is seen, a Q value of 66, although the noise in the data is evident. Extrapolation of this Q to 1 GHz and assuming the same linear frequency model gives, a Q value of 4.34 while measurements from the VNA, indicates a value of Q of 12.7. In the

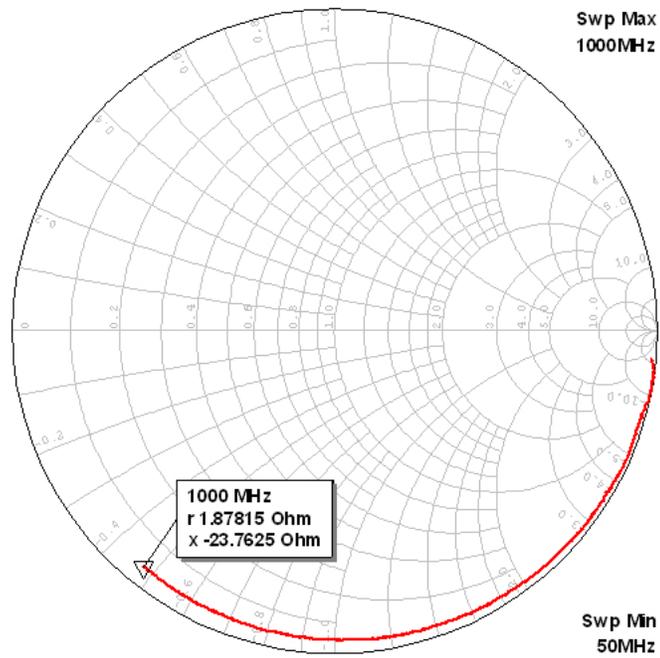


Figure 7.5: One port measurement, S_{11} of the BST-IDC packaged varactor, sweep .050-1 GHz.

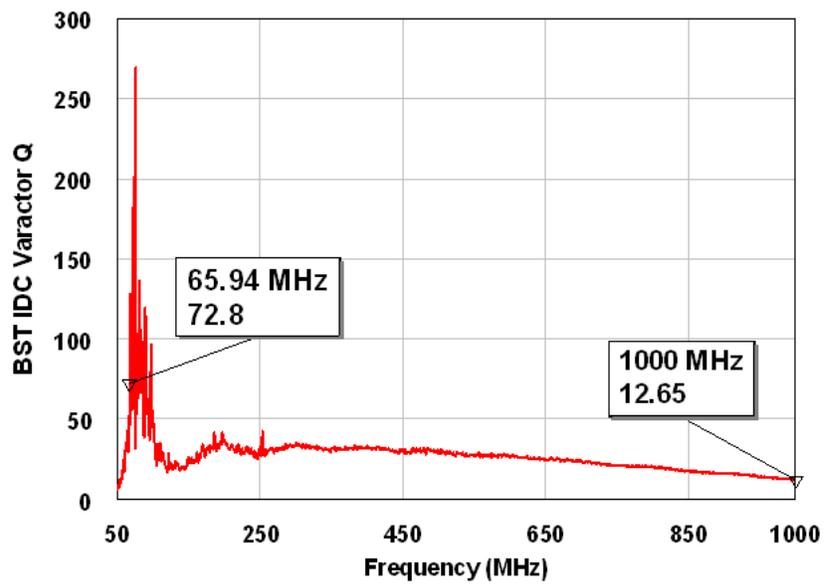


Figure 7.6: Computed Q of the BST-IDC varactor from measured VNA Real and Imaginary impedance data.

frequency range of 50–200 MHz it appears that the series resonant method of measurements will provide an accurate assessment of Q . Computed VNA data of Q from the real and imaginary values is subject to significant error in this frequency range as the measured reflection coefficients are nearly unity. This is evident in the data collection, see Figure 7.8. However, above 200 MHz, collected data shows good agreement with $1/f$ slope in Q through 1 GHz, in agreement with [115] whereby the authors highlight the Q dependency on ferroelectric geometries due to the presence of a geometry independent series resistance. Despite the difference in device geometry of their work with ours, similar high frequency Q slope frequency dependency is noted that is essentially $1/f$. If a $1/f$ dependency of Q is assumed from 1 GHz then at 70 MHz the Q should be 180, and so there is this disparity between the two measurements, between 66 and 180. We expect the actual Q at 70 MHz is more in line with the measured value of 66 as opposed to the backward interpolated value for the following reasons.

First, part of the error is associated with the difference in fixtures. The difference in these two Q values represents a difference in R_s of only 4 ohms. In addition, measurements conducted on the VNA are at 30 volts while on the series resonance test set, 25 volts. Another difference is the dominance of the R_p value of the varactor below a critical high frequency point, versus R_s . The series model is appropriate for a very high frequency model, while a parallel model incorporating the more dominate dielectric film losses as opposed to the electrodes DC resistance losses is required at lower frequencies. Finally, another significant contributor to error is less obvious. This is leakage current and is addressed briefly in treating excess noise. As the applied BST varactor voltage is increased so is the leakage current and the associated loss. The Q vs. bias voltage should follow the curve in Figure 2.17 for a metal-insulated-metal or MIM capacitor. However, with leakage current present, the Q shows a definite peak value, followed by a steep decline as breakdown is approached in some varactors; see Figure 7.7.

The leakage current is time dependent, a function of “soakage” of the dielectric vs. applied voltage over time, and a property of the quality of the film deposition. Leakage currents associated with the these varactors was in the range of a few nano-amps to several micro-amps

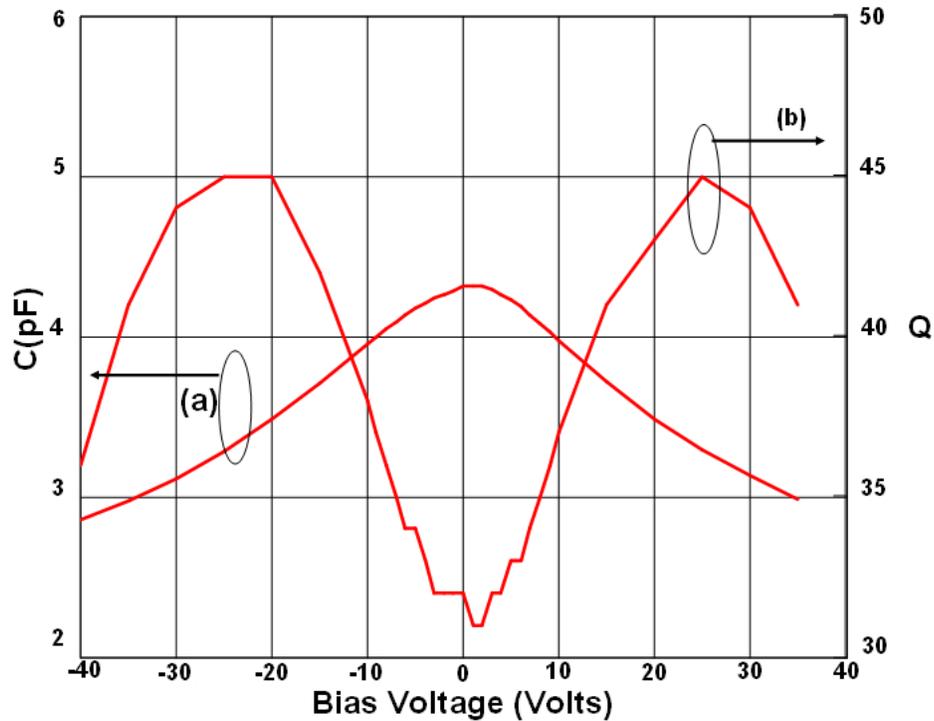


Figure 7.7: An IDC varactor which displays leakage, shows an increase in Q with bias voltage and then a steep decline as the breakdown voltage is approached

and clearly needs to be sub-nano amp to maximize unloaded Q . The time dependence of the leakage current in measurements, particularly at the higher bias voltages, 25–30 volts, adds non-systematic errors. It is equally important to note, that these extrapolations are only permitted based on an assumption that the packaged BST varactor is operating below self-resonance and reference to Figure 7.5 demonstrates that this is the case.

Characterization of the BST capacitance value is readily accomplished using an impedance analyzer. Although the measurement technique is unique, based on an RF I-V technique in lieu of a bridge system or a directional coupler voltage-reflection coefficient system, corrections are still required to remove errors introduced by the fixture. Accuracy of measurements is partially defined by the component value of the device under test (DUT) and the frequency and measurement topology. Measurement topology defines the orientation of the in-circuit capacitor, i.e. is placement in series or in shunt with respect to the measurement source. If the impedance is

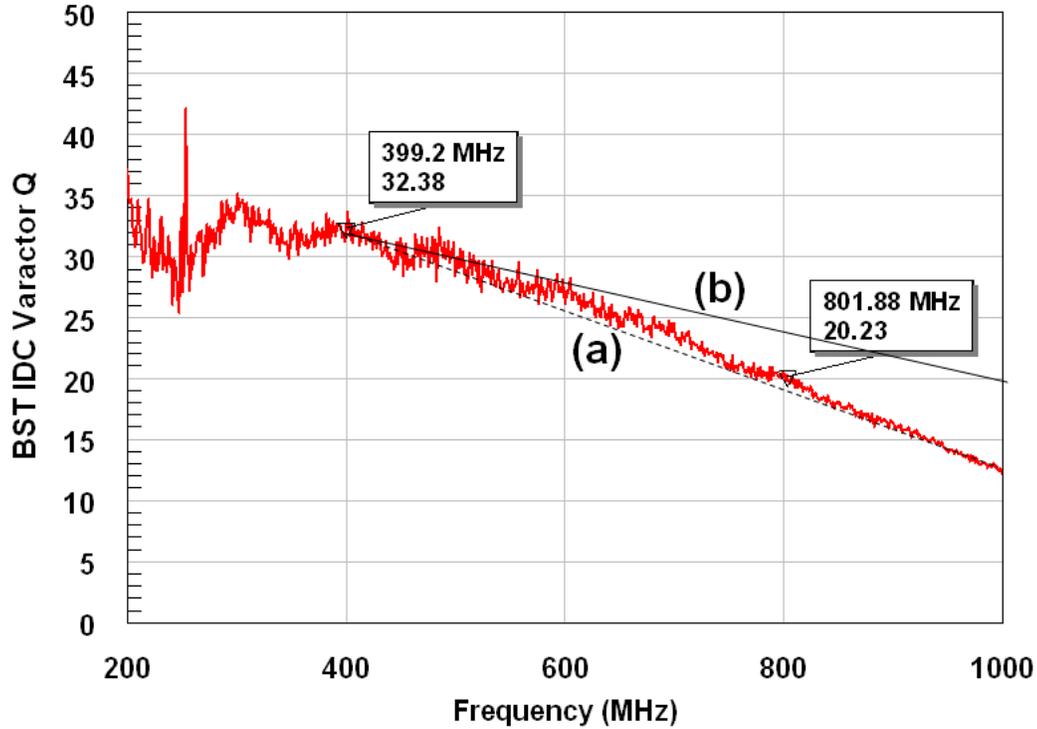


Figure 7.8: BST-IDC Q from measured VNA one-port S-data. In (a) a slope of $1/f$ while in (b) $1/\sqrt{f}$ slope. The noise in the data below 400 MHz, in particular below 200 MHz is evidence of measurement uncertainty with the VNA.

large, small varactors measured at low frequencies are best characterized with the RF I-V measurement based system. This measurement system is appropriate for devices with impedances up to about $20\text{ k}\Omega$ and as little as $1\ \Omega$. Therefore, this measurement technique is more appropriate than the S-parameter method provided by the VNA [109]. In many cases, the fixture is not part of the formal calibration and a method of compensation must be introduced to the measured impedance values. In lieu of this, without knowledge of the fixture characteristics, we introduce a second method. In effect a form of fixture compensation and we provide the results of this technique and application in this dissertation. One method of fixture compensation is presented in [113] and a form of open and short load compensation is discussed. In the discussion the load termination is ideally known. If this is not the case, then load terminations that are at least $1/100^{\text{th}}$ the impedance of the lowest impedance to be measured and 100 fold larger

than the highest impedance to be measured are sufficiently accurate. We consider a approach applied to a one port device, the capacitor. Testing is accomplished by placing the capacitor in the shunt mode and obtaining one port data. The series mode whereby the capacitor is terminated requires a known termination impedance accurately. Otherwise a two-port S-parameter measurement is an alternative using for example a TRL (through-reflect-line) calibration, but the accuracy of the reflection measurement system particular for high impedance elements is again an issue.

Therefore, the one port shunt measurement system is used and consists of a calibrated reference plane-extension and a measurement plane that is launched to the DUT. The problem is shown in Figure 7.9. Calibration is provided by APC-7 SOL (short-open-load) calibration at the test set panel. The APC-7 calibration standards are known and the calibration table for these standards are used in the instrument or used manually (type Agilent E4991A or HP4191A). Therefore, at the analyzer test port, if an exact APC-7 launch to the DUT is provided, accurate measurements within the variance permitted by the test set are sufficient. For the case where this fixture interface is not available, a second measurement test is required. A set of PC mount SMA connectors, type male are used. Each of the center pins are reduced in length by cutting and filing to a length of 1.5 mm. An open and short are created in this manner. For the short a circular copper plate is attached over the center pin with the goal of constructing a short circuit with an inductance of less than 120 pH ($1/100^{\text{th}}$) of the reactance of the largest varactor capacitance anticipated at 1 GHz. The open is constructed identical to the short in so far as the pin location and the length, the open and the short lengths, should be identical. The DUT capacitor or a mounted varactor, are also handled in the same manner.

Compensation for this fixture interface is next. From the calibration plane, an APC-7 to SMA launch represents a cascade transmission line with impedance Z_o . The line or extension should be as short as possible, in our case the extension length is 6.06 cm. At this point the addition of the terminations add complex shunt admittance. Correction for the fixture which provides mounting of the test unit capacitor is required. Therefore, the network added by the

SMA panel mount port is an additional complex series impedance plus an additional shunt admittance. The network we have is shown in Figure 7.10.

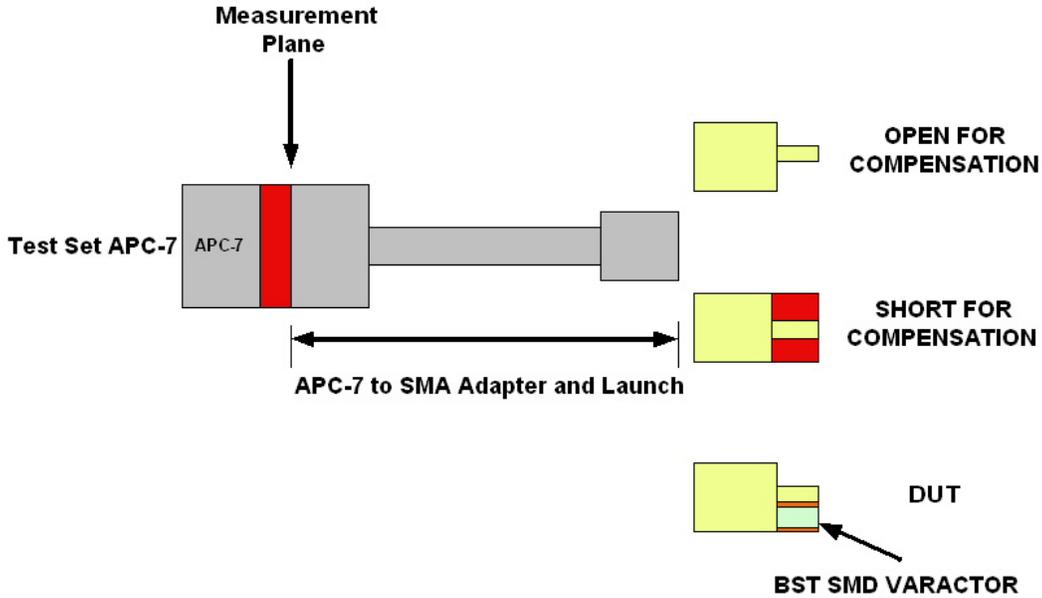


Figure 7.9: One port measurement using RF I-V and fixture launch compensation

If the short is ideal and applied, then an impedance measurement at the test port provides the series impedance of the APC-7 adapter, line, and transition and SMA panel mount connector series inductance term. Reference this measure as Z_{meas}^{sc} . If the short is removed, then a second measurement at the test port provides the prior series impedance and the shunt admittance of an attached open SMA panel mount connector. Reference this measure as Z_{meas}^{oc} . If the open circuit measurement is subtracted from the short circuit measurement then the remaining element is the shunt open capacitance of the SMA panel mount fixture. Next connect the DUT and the measured result in terms of all prior measurements is expressed as

$$Z_{\text{meas}} = Z_{\text{meas}}^{sc} + \frac{(Z_{\text{meas}}^{oc} - Z_{\text{meas}}^{sc}) Z_x}{(Z_{\text{meas}}^{oc} - Z_{\text{meas}}^{sc}) + Z_x} \quad (7.2)$$

where Z_x is the DUT impedance. Solving for the DUT impedance then gives

$$Z_x = \frac{(Z_{\text{meas}} - Z_{\text{meas}}^{sc}) Z_\gamma}{(Z_\gamma - (Z_{\text{meas}} - Z_{\text{meas}}^{sc}))} \quad (7.3)$$

where Z_γ is $Z_{\text{meas}}^{oc} - Z_{\text{meas}}^{sc}$.

Validation with measurements is key. Investigating potential error via simulation is straight forward and permits quickly checking assumptions. A known porcelain monolithic capacitor, an ATC100B, 2.2 pF is investigated, and is chosen since data is available including Q , parasitics, and capacitance tolerance. The fixture hardware is shown in Figure 7.11.

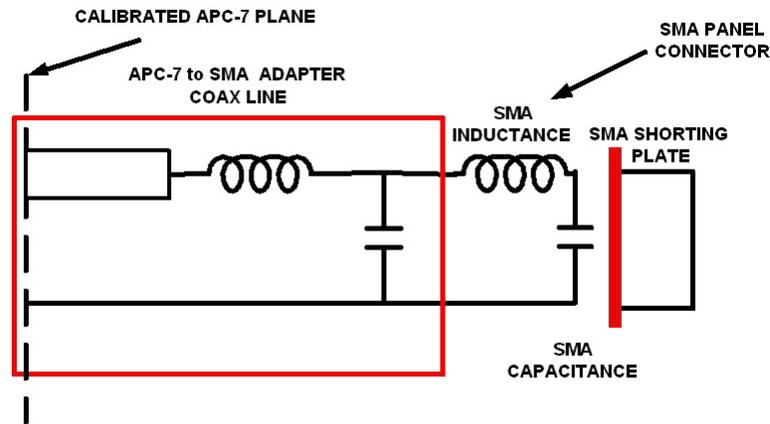


Figure 7.10: One port measurement using RF I-V and fixture launch compensation

The measurements are conducted at spot frequencies of 50, 100, 500 MHz, and 1 GHz. See Tables 7.1 and 7.2. Measurement data is placed into a Mathcad routine as a table entry and the calculations for the measured test capacitance provided by the solutions to (7.2) and (7.3). The measured capacitance difference is less than 0.12 pF from the data sheet stated value and within the tolerance of 5% for this capacitor unit. A slight increase in capacitance value at 1 GHz is noted as is contributed by the package series inductance, additional measured values are required to confirm the self resonant frequency.

Next is the addition of the bias tee which utilizes 3.5 mm connector fittings. Now port

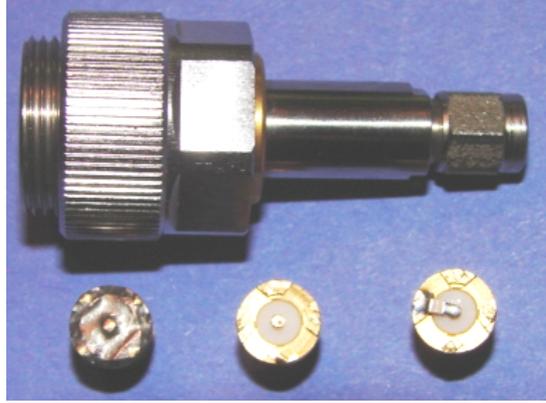


Figure 7.11: The one port test set. The short, open, and capacitor mounted component along the bottom row. The APC-7 to SMA interconnect at top requires an extension of the test set reference plane.

Table 7.1: Measurement test data

Fixture compensation data								
Freq.(MHz)	$ Z_{oc} \Omega$	$\angle Z_{oc}$	$ Z_{sc} \Omega$	$\angle Z_{sc}$	$ Z_m \Omega$	$\angle Z_m$	$\text{Re}(Z_\gamma)\Omega$	$\text{Im}(Z_\gamma)\Omega$
50	59000	-90°	.148	39°	67.22	-89.19°	-.115	$-j5900$
100	3500	-80°	.206	41°	141.25	-89.4°	6078	-34470
500	5700	-81°	.309	23°	722	-89.7°	891.392	-5630
1000	2840	-78°	.319	5°	1440	-90°	590.151	-2778

extension from the calibrated APC-7 reference plane must be invoked. This is required as the port at the end of the APC-7 to SMA adapter is extended to accommodate the introduction of the physical length of the bias tee. The new system fixture is shown in Figure 7.12. The addition of the bias tee, type MCL ZFBT-4R2G-FT, requires the extension of the reference plane and to increase the reference plane by an additional 13.36 cm. As the extension increases so does the possibility of increased error. Care is required in each calibration step as the rotation of the termination impedance angle is potentially larger as the line extension increases. A smaller physical size bias tee is desired as presented in Figure 4.72. Of course all of this is circumvented if calibration standards are available at the final (bias tee) measurement port, and this is the preferred method.

The measured open, short, and DUT terminations are shown in Table 7.3 for the case of

Table 7.2: Calculated component impedance and value

Capacitor measured and calculated data after fixture compensation			
Freq.(MHz)	Re(Z_x) Ω	Im(Z_x) Ω	Capacitance (pF)
50	21.33	$-j1480$	2.151
100	5.02	$-j737.116$	2.159
500	-0.98	$-j144.92$	2.196
1000	-0.68	$-j68.837$	2.312

Table 7.3: Measurement test data

Fixture compensation data								
Freq	$ Z_{oc} \Omega$	$\angle Z_{oc}$	$ Z_{sc} \Omega$	$\angle Z_{sc}$	$ Z_m \Omega$	$\angle Z_m$	Re(Z_γ) Ω	Im(Z_γ) Ω
50 MHz	1289	-31.2°	.312	36°	790	-58.4°	1102	$-j667.92$
100 MHz	855	-32.8°	.453	34.7°	452	-63.8°	718.313	$-j463.418$
500 MHz	1380	2°	.840	-11.8°	142.6	-84.4°	1378	$j48.333$
1000 MHz	843	-34.2°	2.57	0.9°	68	-87.55°	649.659	$-j473.877$

Table 7.4: Calculated component impedance and value, bias tee in place

Capacitor measured and calculated data after fixture compensation			
Freq.(MHz)	Re(Z_x)	Im(Z_x)	Capacitance(pF)
50	-1.599	$-j1479$	2.153
100	-4.562	$-j739.852$	2.151
500	-1.592	$-j142.422$	2.235
1000	-4.594	$-j70.927$	2.244

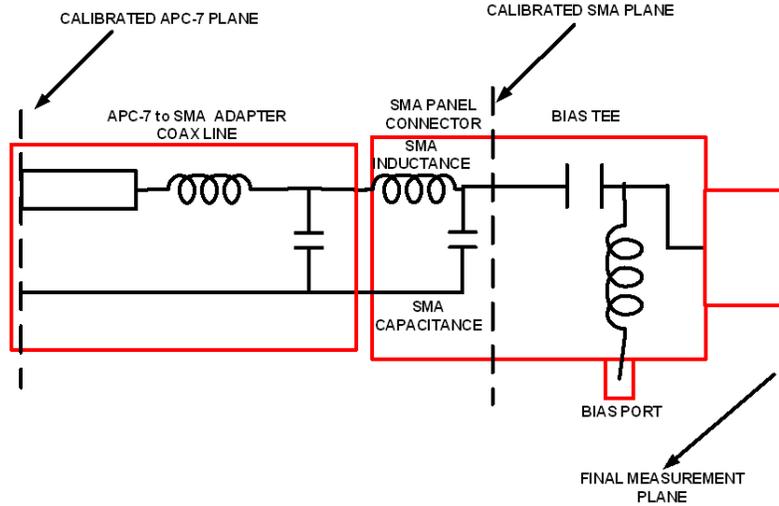


Figure 7.12: The one port test set with bias tee added. The calibrated reference plane needs extension through the bias tee; at the final measurement plane.

the added bias tee. The port extension length is set in increments of 0.01 cm from the initial 6.06 cm length prior to adding the bias tee. The length adjustment is set by monitoring the angle of the impedance of the returned measurement as opposed to the angle of the reflection coefficient. Ideal case, the magnitude of the measured impedance will minimize (go to zero) while the angle also goes to zero. Since reflection is modulus ± 180 it is difficult to zero. The measured capacitance with bias tee in place is in Table 7.4 and the maximum error is 2.2% from nominal capacitance. The negative resistive component is calibration, port extension and set up issue and speaks to the fact that extraction of unloaded Q is not appropriate for this measurement system. Particularly challenging in the case of a low loss high- Q component in that the resistance value is very small relative to the reactance value. For the test capacitor used here the unloaded Q is several 1000 below .15 GHz. Therefore small changes in the resistance value will result in large changes in Q . Since the measurement error is on the order of the measured resistance value, the result can lead to negative Q values. The test set extension with a particular bias tee (not suitable for high voltage) is shown in Figure 7.13.

The technique discussed provides reasonable accuracy after reference plane calibration, port

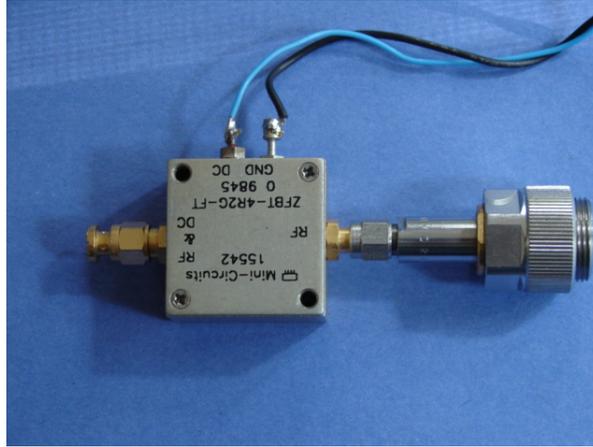


Figure 7.13: The one port test set with bias tee added. The capacitor under test is attached to the modified SMA panel connector on the extreme left.

extension and fixture compensation. Key to the success though is uniform discontinuity and low loss port extensions. Unfortunately this is not always the case. For the discrete measurement frequencies reported here peaked resonant responses were avoided and are not easily removed. The resulting problem in the measurement process is chiefly found in the bias tee. The frequency response of the bias tee is not uniform or monotonic and several resonances occur. A major contributor is the self resonance of the DC blocking capacitor, chosen to be high-voltage and NPO (ceramic on glass) to avoid ferroelectric effect of the bias tee as a function of the applied bias. To circumvent this problem, calibration is moved completely to the end of the bias tee including the APC-7 to SMA extension. In doing so, the need to correct for the response errors that occur after the calibrated APC-7 port are removed. First, important in this measurement process is the **identical** properties of the calibration and DUT fixtures. Second, the quality of the short and open and again the identity of the fixture used to construct the open and short calibration pieces and the fixture piece holding the DUT sample. Under the assumption again that the short is nearly perfect, i.e. the reactance of the short and of the open is orders of magnitude smaller and larger respectfully compared to the DUT. This as opposed to knowing precisely what are the calibration pieces.

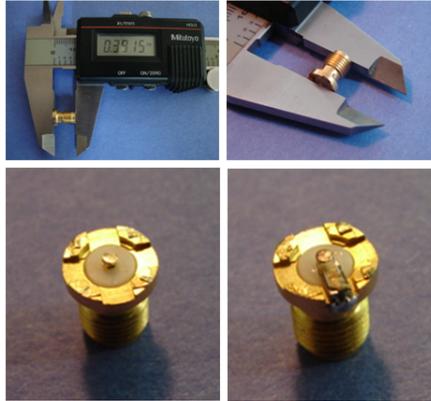


Figure 7.14: The open calibration piece and the DUT fixture are identical 3.5 mm connectors with identical mechanical dimensions. Identical connector lengths, measured from the edge of the connector center pin to the outside shell of the connector, is mandatory in order to maintain accurate measurements.

After calibration a new and identical open is constructed and tested. From this measurement the open capacitance vs. frequency; 1 MHz-1 GHz, is less than 85 fF. This confirms the assumption that the open reactance is small as compared to the DUT. Nevertheless, with this reactance known, it should be removed from the final measurement of the capacitor on the fixture using $Z_{\text{actual}} = Z_{\text{meas}}Z_{\text{open}}/(Z_{\text{open}} - Z_{\text{meas}})$.

The results of the 2.2 pF test capacitor and a small BST IDC, less than 1 pF capacitor over the frequency range of 10 MHz-1 GHz; show no error due to the inability to remove resonant effects created by the bias tee, see Tables 7.5, 7.6, and 7.7. This data includes the APC-7 to SMA adapter and extension connector, the HV bias tee, and the fixture pieces to house the DUT as shown in Figures 7.14 and 4.72.

These measurements are extended to 3 GHz using the technique outlined. The impedance analyzer, Agilent E4991A, is setup with no extension correction and the fixture coefficients are those of the front panel reference plane, APC-7. Calibration is not conducted at the instrument measurement reference plane. Instead, one calibration is completed using our defined standards as shown in Figure 7.14. In essence we default to the APC-7 test set calibration values and use the measurements of our standards to aid in the de embedding of our device under test.

Table 7.5: Measurement test data, calibration at SMA bias tee port

Measurements of 2.2 pF test capacitor using fixture elements as CAL set						
Freq.(MHz)	$ Z_{oc} \Omega$	$\angle Z_{oc}$	$ Z_{DUT} $	$\angle Z_{DUT}$	C_{DUT}	C_{CORR}
10	32000	+70°	9500	-83°	1.688 pF	2.131 pF
50	35000	-86°	1428	-90°	2.229 pF	2.138 pF
100	22000	-78°	715	-90.1°	2.226 pF	2.155 pF
300	6500	-89°	236.8	-90.49°	2.24 pF	2.172 pF
500	3830	-90.1°	140.47	-90.75°	2.266 pF	2.183 pF
1000	2020	-89.6°	66.78	-91.3°	2.384 pF	2.305 pF

Calibration again includes the 100 working volt DC (WVDC) bias tee and the APC-7 to SMA extension. The 2.2 pF sample test capacitor that is tested, clearly shows the self resonant effect. Indeed, if we correct for the capacitance value measured, by the series addition of 720 pH, we will compensate nearly perfectly the measured capacitance and obtain 2.2 pF. The capacitor measured is approaching the self resonant frequency, near 3 GHz, and the measured capacitance on the impedance analyzer rises significantly in value as 3 GHz is approached. The predicted resonant frequency is approximately 4 GHz. In Figure 7.15(a)-(c) we show the measured, corrected for an open fixture, and compensated for self resonance due to 720 pH respectfully. While in (d) the open fixture shows 85 fF of capacitance as discussed earlier.

Following through are measurements of a small IDC BST capacitor The capacitor is mounted on a ceramic thermal bridge [114], a 1206 block size ceramic material with palladium silver terminations. Therefore a portion of the device capacitance is contributed by the thermal bridge as well a reduction in the capacitance change with bias voltage. The change in capacitance for the measured unit for Table 7.6 for a bias voltage change of 0 to 30-V is 15%. The capacitance change measured at 50 MHz and 1 GHz is virtually identical implying no resonance effects through at least 1 GHz, see Table 7.7.

Measurements of the varactor are best accomplished in an in situ environment as this best emulates the actual application. The resonator Q is dominated by the varactor and therefore the varactor is evaluated as close to the actual application as possible. This is accomplished with accuracy by a resonance method which evaluates the series equivalent resistance of the varactor.

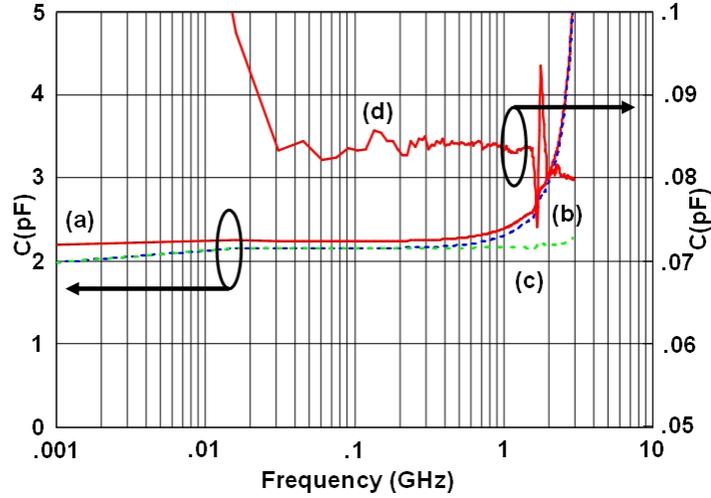


Figure 7.15: Measured 2.2 pF test capacitor through 3 GHz. The capacitor clearly shows the self-resonant effect of the 720 pH package inductance.

Table 7.6: Measurement test data, calibration at SMA bias tee port

Measurements of BST IDC varactor using fixture elements as CAL set				
Freq.(MHz)	Re[Z_{open}]	Im[Z_{open}]	Open Value	BST IDC Corrected C
10	10.26 k Ω	+ $j28.2k\Omega$	450 μ H	.7696 pF
50	1.43 k Ω	- $j40.98k\Omega$.07768 pF	.7781 pF
100	4.574 k Ω	-21.52 $k\Omega$.07396 pF	.7756 pF
500	-6.685 Ω	- $j3.83k\Omega$.08311 pF	.7636 pF
1000	14.102 Ω	- $j2.02k\Omega$.07879 pF	.7779 pF

The technique shows good agreement with both the VNA and reactance bridge methods and has the further benefit of an in situ measurement. Accurate capacitance measurements are accomplished on an impedance analyzer and use a SOL method. One port characterization is obtained. The fixture calibration tool created included a verification element and the process uses a straight forward de embedding process for obtaining the device under test parameters. Conversion from one port S-parameters to y-parameters or z-parameters are used since the device investigated is a portion of parallel susceptance which exists as part of the calibration and fixture. Then eventually the series equivalent impedance of the DUT is found after importing the parameter data set and solving explicitly for the DUT self impedance.

Table 7.7: Measurement test data, varactor C vs. bias-V and frequency, failed: varactor failed to change capacitance with voltage, suspect damage due to low breakdown voltage in this sample

Measurements of BST-IDC varactor C vs. V and frequency on thermal bridge carrier			
Bias voltage-V	Capacitance (pF) 50 MHz	Capacitance (pF) 1 GHz	
0	.7646	.7725	
5	.7558	.763	
10	.7325	.7379	
15	.7007	.7099	
20	.6767	.682	
25	.6525	.6584	
30	failed	.6732	

7.2 Special techniques applied to noise measurements of two ports

Noise measurements and signal-to-noise ratio are fundamental to system design and evaluation [25]. In instances where the required measurement equipment is not available, requirements to devise other techniques are desired. In addition, the ultimate limitation to characterizing noise in microwave amplifiers derives from the noise inserted by the front end of the measurement test set. Typically, a high-gain low noise preamplifier is used in the measurement set to improve accuracy. Even then there is a limit to the minimum noise factor that can be measured. In this section, an extended Y-factor noise measurement technique is presented, that utilizes an amplifier stage identical and in addition to the amplifier under test, to enhance measurement accuracy. Utilizing a calibrated noise source, the output noise power of first a forward cascade of the two amplifiers is measured and then that when the amplifiers are arranged in reverse cascade. The use of a spectrum analyzer or power meter, with a readily measured change in noise power reading is required as well as a calibrated noise source.

We discuss and develop here several approaches to the measurement of noise at microwave frequencies. This includes pure noise, a composite of AM and PM, and to a greater degree phase noise, PM only, which is dominant in self-limiting oscillators. These techniques are

best characterized as “bootstrap” in nature, as they take a measurement problem and use this problem to an advantage to secure a measurement [53]. For example, in the application for quantifying the noise in amplifiers and mixers, we use a modification of the Y-factor principle [49] and a variation of the cascaded noise equation to achieve accurate measurements without resorting to frequency translation networks [5]. Consequently, direct noise measurement at microwave frequencies is straightforward. Oscillator noise measurements and the measurement of phase noise again utilizes the problem itself as a solution. Here we discuss a method of phase noise measurement utilizing receiver desensitization; a problem that exists due to finite phase noise.

Modern automatic noise figure meters and microwave spectrum analyzers both provide the capability of pure noise measurement [49]. However, these instruments are either limited in frequency range or not readily available with the required measurement accuracy without the addition of special firmware options. We address these issues by introducing a technique which is limited only by the noise source. Furthermore, the DUT serves the role of test apparatus in the process. So it is a component already on hand. The pure noise factor, noise figure in dB format expressed as numeric, is defined as

$$F \equiv \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} = \frac{S_{\text{in}}/S_{\text{out}}}{S_{\text{out}}/N_{\text{out}}} . \quad (7.4)$$

Here SNR, N and S are the signal-to-noise ratio, noise power, and signal power respectfully. The available gain of an amplifier, G_{av} , in terms of signal power is

$$G_{\text{av}} = \frac{S_{\text{out}}}{S_{\text{in}}} . \quad (7.5)$$

Substitution into (7.4) gives the noise factor F as

$$F = \frac{N_{\text{out}}}{G_{\text{av}}N_{\text{in}}} . \quad (7.6)$$

Therefore, the output noise power of an amplifier or a chain of amplifiers with total available gain G_{av} is

$$N_{\text{out}} = FG_{\text{av}}N_{\text{in}} . \quad (7.7)$$

The total output noise power arrives from two parts; the noise associated with the input termination and the noise contributed by the device alone (N_D). Therefore, N_{out} is composed of two terms given as

$$N_{\text{out}} = N_{\text{in}}G_{\text{av}} + N_D . \quad (7.8)$$

Noise power is proportional to noise temperature, $N \sim kTB$, where k is the Boltzmann constant, T in degrees Kelvin, and B is the system bandwidth in Hz. Now equating (7.7) and (7.8), and for convenience, labeling the available gain as G only; we have

$$N_D = kT_oBG(F - 1) . \quad (7.9)$$

In (7.9), the noise temperature is chosen for convenience as an ambient value at T_o , the so called cold temperature. Our goal is to extract the noise factor F , and therefore, a second value of noise power is measured at a different source termination temperature, T_2 , the so called hot temperature. We now rewrite (7.9) in a form identifying the output noise power due to the input termination, noise power contributed by the device with noise factor F , and the noise power engendered by the available gain of the device. These noise output powers are taken at temperatures T_o and T_2 and expressed as,

$$N_1 = kT_oBG + kT_oBG(F - 1) \quad (7.10)$$

and

$$N_2 = kT_2BG + kT_oBG(F - 1) . \quad (7.11)$$

A ratio of these noise powers is provided by

$$\frac{N_2}{N_1} = \frac{kT_2BG + kT_oBG(F-1)}{kT_oBG + kT_oBG(F-1)}. \quad (7.12)$$

Then the noise factor F and the Y factor are readily found from (7.12) as

$$F = \left(\frac{T_2}{T_o} - 1\right) \left(\frac{1}{\frac{N_2}{N_1} - 1}\right) = \left(\frac{T_2 - T_o}{T_o}\right) \left(\frac{1}{Y - 1}\right) \quad (7.13)$$

where Y is the ratio of noise power measured, $Y = N_2/N_1$, at the respective input noise temperatures, T_2 and T_o , provided by the noise source termination. The noise power associated with temperature T_2 relative to T_o , is considered an excess noise power and referred to as the excess noise ratio (ENR) of the source; usually expressed in dB [30]. The application of this development is germane to both down conversion and up conversion systems, assumes small signal operation, and a given constant bandwidth B for the cascade. No translation networks are present, although this does not hamper the measurement technique, however the development must be slightly modified if frequency translation networks are present. Finally, the available gain must be large enough relative to the noise power of the measurement test set, so that the accurate ratio of noise power is established. Here resides the key problem; the ability to measure accurately the noise power ratio with a device under test which has limited available gain. The solution resides in using “N” cascaded devices under test, (DUTs), as required to establish sufficient gain to overcome the internal noise floor of the test set. Two sets of noise measurements are conducted at noise temperatures T_o and T_2 , with a forward and reverse cascade connection of the DUTs. We refer to the new measurement as extending the Y factor technique. The extended Y -Factor technique utilizes two DUTs in a two-stage cascade, first with one arrangement of the DUTs, and then with the alternative or reverse cascade. The technique makes use of the cascaded noise factor operation twice. Figure 7.16 illustrates the test setup with two possible arrangements of the cascaded DUTs. In Figure 7.16, the spectrum analyzer is configured to measure noise power (normalized to a 1 Hz bandwidth) using the

marker noise mode [50]. Measurements utilizing this mode provide proper correction factors including noise equivalent bandwidth (NEBW), correction for detector characteristics with a noisy input signal, and normalization of noise power to a 1 Hz bandwidth. In our work, 10

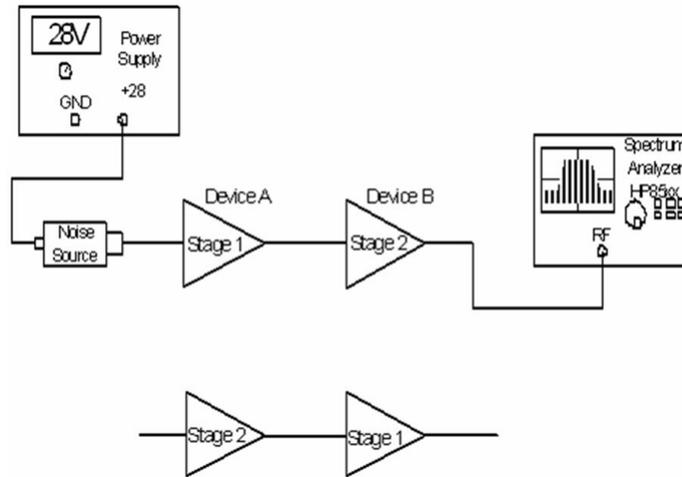


Figure 7.16: Y-factor test set actively incorporating the second stage contribution effect

readings are averaged to obtain a stable value. Other methods for reading noise power can be used, however, the marker noise mode is quick, convenient, and a standard option on spectrum analyzers. The individual noise factors of the DUTs for a cascaded system with DUT A followed by DUT B are denoted by F_{1A} and F_{2B} , and the cascade with DUT B followed by DUT A is identified by F_{1B} and F_{2A} . Correspondingly, the total noise factors of the two-cascaded systems are denoted F_{TA} and F_{TB} according to whether DUT A or DUT B is the first stage. Using Friis' formula we can write

$$F_{TA} = F_{1A} + (F_{2B} - 1) / G_{1A} \quad (7.14)$$

and

$$F_{TB} = F_{1B} + (F_{2A} - 1) / G_{1B}. \quad (7.15)$$

Here the first subscript refers to the position in the cascade (either first or second stage),

and the second subscript identifies the particular DUT (either A or B). Also G_{1A} , and G_{1B} , are the available gain of each individual stage. The technique presumes that the parameters of the DUTs are invariant to their position in the cascade, so that $F_{1A} = F_{2A} = F_A$ and $F_{1B} = F_{2B} = F_B$, as well as $G_{1A} = G_{2A} = G_A$ and $G_{1B} = G_{2B} = G_B$. Equations (7.14) and (7.15) can now be solved simultaneously for the unknown noise factors of the two stages as

$$F_B = \frac{[F_{TB}G_A G_B - G_A(1 - F_{TA}) - 1]}{(G_A G_B)} \quad (7.16)$$

and

$$F_A = \frac{[F_{TA}G_A - F_B + 1]}{G_A}. \quad (7.17)$$

So with the gains of the two stages measured independently, the noise factors of the two stages can be determined from the measured noise factors, F_{TA} and F_{TB} , of the stages arranged in first one cascade, and then in the reverse cascade arrangement respectively. From these measurements, the noise factors of each of the stages can be derived. In the special situation of matched DUTs, where the noise and gain of the two stages are identical (so that $F_A = F_B = F$ and $G_A = G_B = G$), then we will have $F_{TA} = F_{TB} = F_T$ and the calculations simplify to yield the noise factor of a single stage as

$$F = \frac{GF_T}{G^2 + 1}. \quad (7.18)$$

One of the assumptions of the augmented Y-factor approach is that the gain and noise factor of the stages are invariant with the position of the stages in the cascade. Any departure will result in an error. One manner to reduce sensitivity to matching conditions is to provide one device with either small attenuators or low loss isolators at the input and output. Another method is to use a test set amplifier with good input and output return loss commensurate with low noise factor [54].

The procedure requires accurate measurement of gain and noise power ratio. In common with the conventional Y-factor noise characterization procedure, a well-calibrated noise source is essential. The method has been used routinely to characterize the noise performance of a

variety of microwave and millimeter-wave amplifiers. In this section, we compare noise characterizations obtained using the augmented Y-factor method and the conventional approach using an automated noise measurement system.

The validity of the method was explored using a 1.5 GHz GaAs MMIC devices with a total gain of 28 dB. The MMIC incorporated a band pass input match to optimize return loss and noise figure. Two noise sources with different ENR were used for the "on" state and these sources functioned as ambient sources in the "off" state. Two MMICs were used to realize the two amplifier stages. The noise factors of the forward and reverse cascades were nearly identical. Comparisons of the noise figure extracted using the augmented Y-factor method and that measured using an automated noise measurement are presented in Figure 7.17. It is noted

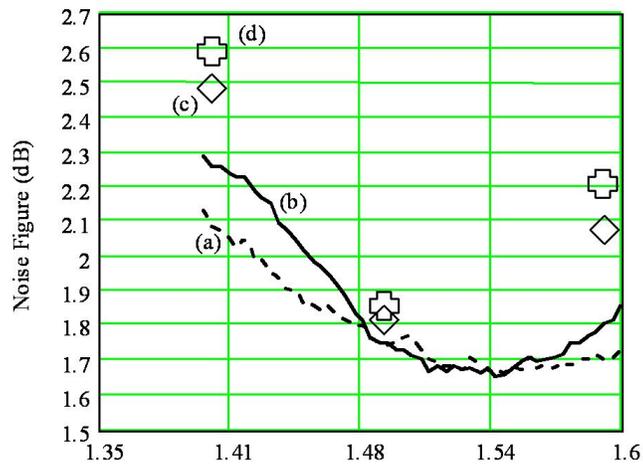


Figure 7.17: Measured noise figure (dB) vs. frequency (GHz) obtained with the automated noise measurement set, (a) low ENR (=5.2dB) noise source, and (b) high ENR (=15.1 dB) noise source; and obtained using the augmented Y-factor method, (c) the augmented Y-factor method with the low ENR source, and (d) with the high ENR source.

that good agreement is obtained in the automated noise figure measurement for both the low and high ENR noise sources at amplifier band center. As well, there is good agreement between the results obtained using the extended Y-factor method and that from the automated test set.

The agreement is particularly good near the band center, where return loss of the amplifiers under test is also at a minimum. Near the band edges, the agreement is not as good, as return loss degrades, and presumably, noise characteristics are dependent on the order of the stages in the cascade. The disparity is partly attributed to the dependency of the impedance of the noise source. A noise source with low ENR is preferred, as relative to the high ENR source, it has an input impedance that deviates less between the on and off states [52].

In a second test, an amplifier with 28 dB gain was used instead of the second matched MMIC. This amplifier corresponds to an instrumentation amplifier that is commonly used as a pre driver before a noise measurement system. In this case, the Y-factor method alone provided a minimum noise figure of 4.1 dB at 1.49 GHz. In contrast, the augmented Y-factor method yielded a noise figure of 1.8 dB, which is in close agreement to the other measurements of noise figure shown in Figure 7.17. This significant discrepancy is an indication that the second stage contribution effect is significant.

7.3 Special techniques applied to the noise measurements of sources

The operational characteristics of specific components will restrict the type of noise present, and influence the requirements and techniques of the noise measurement. In self-limiting oscillators the AM component of noise is usually less than the PM component and therefore a test set which targets this specific noise property is desired [59]. One of the major issues addressed in transmitter and receiver architecture is how to obtain the largest dynamic range while still obtaining either a low noise power floor or high receiver sensitivity. The dynamic range as discussed earlier, is best described as the difference between the largest signal allowable and the smallest signal discernable before distortion or noise degrades intelligibility. A measurement which characterizes the dynamic range in receivers is desensitization performance [31]. The main causes of low desensitization level are strong adjacent channel signals causing overload or

saturation in the early stages of the receiver or the intermediate gain stages (IF). As discussed earlier, the optimization and assignment of gain distribution to permit appropriate distortion contribution on a stage by stage basis is key. Another cause of reduced dynamic range, is local oscillator noise mixing with the adjacent channel signal, translating noise to the IF channel, and increasing the channel noise power. This noise is in no way distinguishable from the noise normally produced by the injection signal mixing with the noise on the desired channel. The effect of noise conversion is applicable in an up conversion transmitter and the resulting noise degradation manifests itself as a rise in the noise floor of the signal, and the regulatory failure of the “transmitter mask”. The main regulatory concern is the effect of the rise in noise power on neighboring channels. The phase noise measurement of oscillators is critical, and central to understanding the limitations due to oscillator source noise. Although signal analyzers for phase noise characterization are significantly powerful test sets, they are not always available and this motivates researchers to consider alternative techniques [60]. However, some of these techniques are paved with significant pitfalls, with the end result fanciful nonsense measurements and alternative approaches are in demand, [61]

The desensitization level is established through the measurement parameter “SINAD” [62], or the ratio of signal, noise, and distortion power to that of noise and distortion power only. Therefore, the SINAD level is defined as

$$\text{SINAD} = \frac{S + N + D}{N + D} . \quad (7.19)$$

The SINAD level is conveniently written to emphasize that a reduction in the desired signal power will cause a direct reduction in the SINAD level. This level is measured in a straight forward manner using a distortion analyzer, whereby a selective notch filter permits rejection of the signal modulation, leaving only the noise plus distortion terms. Therefore, we have

$$\text{SINAD} = 1 + \frac{S}{N + D} . \quad (7.20)$$

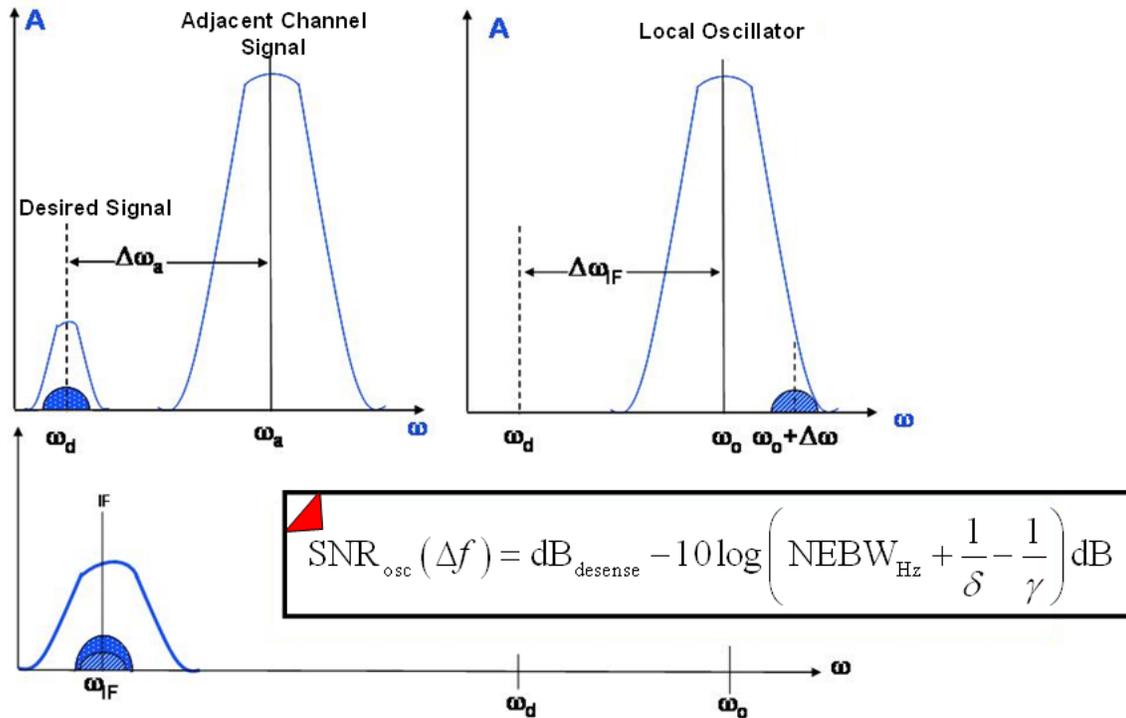


Figure 7.18: Noise spectrum from left to right at RF port, LO injection port, and IF port. The relation given in the inset is derived in the text.

The reduction in desired signal level occurs in an FM communications system utilizing a limiter prior to detection. The limiter provides constant output power. If inadequate IF selectivity is present, then reduction in the desired signal power occurs as the adjacent signal power is increased. If the adjacent channel signal is too close to the carrier frequency, and the IF selectivity is inadequate, then further distortion terms are produced due to nonlinearity in the discriminator. Desensitization due to oscillator noise is best described by reference to figure 7.18.

An increase in the IF noise, as the adjacent channel signal level increases, transfers noise power from the local oscillator noise located at an adjacent channel frequency, i.e. at some Δf offset. The intent of our analysis, is to relate the level of oscillator noise required for a specific desensitization level. This level, is defined as the value of adjacent channel power required to reduce 12 dB SINAD to 6 dB SINAD. The SINAD level is then expressed as a dB ratio,

between the power level of the desired on channel generator with signal amplitude V_D , which established the 12 dB SINAD level, and the power level of the adjacent channel signal at an offset Δf which degrades 12 dB SINAD to 6 dB SINAD. This measurement is conducted at the baseband port of the receiver with the aid of a distortion analyzer which uses an average responding voltmeter. The voltages are a function of time and their values are corrected by the presence of any post filtering. The correction of noise voltage readings in the time domain, from an average responding meter to a root-mean-square value is circumvented here, since all measurements are measurements of ratios.

Assuming a multiplicative mixer, for example an ideal balanced mixer, the inputs are defined as shown in Figure 7.19. All voltages are function of time and V_1 is represented as the sum

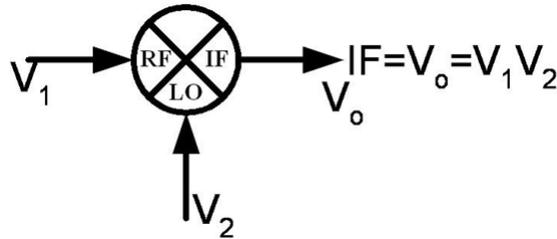


Figure 7.19: An ideal multiplicative mixer, all signal voltages a function of time.

of the desired signal voltage, V_D , and the interfering signal voltage, V_A , at an arbitrary offset signal channel. The voltage V_2 , is comprised of the L.O. carrier and a noise voltage. Therefore, we have

$$V_1 = V_D \cos(\omega_D t) + V_A \cos(\omega_A t) + \bar{V}_{ND}^2 \cos[\omega_D t + \theta(t)] \quad (7.21)$$

and

$$V_2 = V_o \cos(\omega_o t) + \bar{V}_{No}^2 \cos[(\omega_o t + \Delta\omega)t + \theta_2(t)] \quad (7.22)$$

with the following definitions: $V_D \equiv$ desired signal voltage, $V_A \equiv$ offset signal voltage, $\bar{V}_{ND}^2 \equiv$ input noise on channel, $V_o \equiv$ oscillator injection signal voltage, $\bar{V}_{No}^2 \equiv$ oscillator noise voltage,

and radian frequencies $\Delta\omega \equiv$ offset channel measured from the oscillator mean carrier frequency, $\Delta\omega_o \equiv$ oscillator mean carrier frequency, $\Delta\omega_A \equiv$ offset mean carrier frequency, and $\Delta\omega_D \equiv$ desired mean carrier frequency. All signal voltages are RMS (root mean square) values and for convenience, the noise bandwidth is normalized and understood to be 1 Hz. The multiplication and collection of terms transferred to the IF channel are obtained from equations (7.21) and (7.22) and give,

$$V_o = \frac{V_D V_o}{2} \cos(\omega_D - \omega_o) t + \frac{V_A \bar{V}_{No}^2}{2} \cos[\omega_A - (\omega_o + \Delta\omega) t] + \bar{V}_{ND}^2 \frac{V_o}{2} \cos(\omega_D - \omega_o) t. \quad (7.23)$$

The first term represents the desired output voltage, the second term the additive noise of the injection oscillator, and the third is the normal noise term present on channel at the RF port. Since the noise terms are statistically independent, the noise powers at the IF are added, hence the IF power is

$$P_{IF} = \frac{1}{4} (V_D^2 V_o^2 + \bar{V}_{ND}^2 V_D^2 + \bar{V}_{ND}^2 V_A^2). \quad (7.24)$$

Let the offset signal or adjacent channel signal be in the off state. Let the signal-to-noise ratio for 12 dB SINAD be defined as γ . Then, the total signal power measured in a linear part of the IF channel, with a normalized bandwidth of 1 Hz prior to limiting, and after the IF selectivity, is defined as $\gamma \equiv (S/N)_{IF}$ for 12 dB SINAD. From (7.24) we have

$$\gamma = \frac{V_D^2 V_o^2}{\bar{V}_{ND}^2 V_o^2} = \frac{V_D^2}{\bar{V}_{ND}^2}. \quad (7.25)$$

Next, the offset signal is applied, and the signal power adjusted until the added noise power degrades the SINAD level from 12 dB to 6 dB. Define $\delta \equiv (S/N)_{IF}$ as the level set for 6 dB SINAD. Therefore, with the offset signal or adjacent signal power applied, we define the variable δ as

$$\delta = \frac{V_D^2 V_o^2}{\bar{V}_{ND}^2 V_o^2 + \bar{V}_{No}^2 V_A^2}. \quad (7.26)$$

Substitution of (7.25) in (7.26) we have

$$\delta = \frac{V_D^2 V_o^2}{\frac{V_D^2 V_o^2}{\gamma} + \overline{V_{N_o}}^2 V_A^2} . \quad (7.27)$$

Rearranging (7.27), the desensitization level is expressed in terms of the oscillator signal-to-noise ratio and the signal-to-noise ratio in the IF with a specified noise equivalent bandwidth (NEBW) for 6 and 12 dB SINAD, both measurable quantities. The noise equivalent bandwidth provided by any class of low pass filters of bandwidth B and amplitude $H(0)$, is said to be equivalent, provided the same output noise power N_o is available. The application of noise equivalency in our case is applied to any class of bandpass filters provided that $H(0)$ is replaced by $H(\omega)$. Therefore, to have the same noise output we must have

$$N_o = n_o H^2(0) B = n_o \int_0^{\infty} |H(\omega)|^2 df \quad (7.28)$$

and therefore, we have the noise equivalent bandwidth defined as

$$B \equiv \frac{1}{H^2(0)} \int_0^{\infty} |H(\omega)|^2 df . \quad (7.29)$$

Therefore, from (7.27) we have

$$\frac{V_A^2}{V_D^2} = \frac{V_o^2}{\overline{V_{N_o}}^2} \left(\frac{1}{\delta} - \frac{1}{\gamma} \right) . \quad (7.30)$$

The results of (7.30) are written in dB format with the signal-to-noise ratio of the oscillator uniquely identified with the desensitization level found for the specific SINAD values of 6 and 12 dB. Hence we have

$$\text{dB}_{\text{desense}} = \text{SNR}_{\text{osc}}(\Delta f) + 10 \log_{10} \left(\text{NEBW}_{Hz} + \frac{1}{\delta} - \frac{1}{\gamma} \right) \text{ dB} . \quad (7.31)$$

As an example, let the noise equivalent bandwidth be 10 kHz. The 12 and 6 dB SINAD values provide a 4.2 dB signal plus noise to noise ratio and a 5.9 dB signal plus noise to noise ratio respectfully. The desensitization level is measured at 90 dB with an offset between the mean carrier frequency of the oscillator under test and the L.O. frequency of 20 kHz. Therefore, with the understanding that the difference in the test oscillators signal-to-noise ratio and the device under test signal-to-noise ratio are at least 10 dB (less than a 0.42 dB error), the oscillator under test signal-to-noise ratio is at least -139.1 dBc/Hz at 20 kHz offset. A corresponding measurement, conducted in the phase domain, using a signal analyzer and a phase lock mode method of measurement, yielded measurement agreement within 0.5 dB for the same oscillator and carrier offset.

In the appendix, on page 408, we present an extension to this technique. The measurement of baseband audio hum and noise permits relating the oscillator phase noise measured at large carrier offsets to low frequency effects, such as the measurement of microphonics through baseband noise measurements. Capturing these events via this technique is far less difficult than by the method of phase discrimination using a PLL. This is due to the inability of the phase lock loop method to track these disturbances when utilizing a narrow loop bandwidth [32]. Tracking accurate large noise variations of an oscillator, close to the carrier frequency, is better suited to a direct receiver measurement method.

In this section, we discuss a number of measurement techniques that are significantly less complex to implement and yet provide accurate results. The approaches outlined are based on a bootstrap method to the measurement problem. That is to say, we use the actual measurement problem to identify a measurement solution, which is not unlike the problem itself. This is particularly the case in oscillator phase noise characterization, as the problem created by the presence of oscillator noise and jitter, is used directly to quantify the device under test in an otherwise perfect noiseless converter system.

7.4 Conclusions and summary

Proper design of the resonator is contingent on having correct parameters for the varactor. Briefly discussed are simplified techniques for extracting the varactor Q and capacitance vs. bias voltage. These are two separate measurements as the accuracy obtained by a single measurement is a compromise. The unloaded Q measurement is limited by the quality of the inductive portion of the resonator and instrument variance and the capacitance measurement accuracy limited by the instrument variance and accuracy of the calibration standards. This technique lead to error in line with the tolerance of the device under test. Unavoidable resonance and excessive shift in phase over specific frequencies are introduced by the bias tee. If calibration is accomplished with a precisely known calibration set and the extension of the calibration plane is accomplished with a uniform discontinuity, including the bias tee, then those errors may be removed. Otherwise, high Q resonant effects in the bias tee present difficulties in deembedding this error from measurement. In lieu in setting the reference plane at the measurement test set plane, the reference plane is set at the port of the bias tee. Thus allowing the bias tee to be part of the calibration process. The accuracy of this measurement technique is contingent on the identical makeup, construction, and parasitics of the DUT with those of the calibration fixture elements.

Chapter 8

Conclusions

In this dissertation we considered the application of the thin-film varactors to power oscillators. The underlying motivation is to seek alternative higher efficiency microwave sources, with operation of these sources from high voltage. Furthermore, we investigate alternative transmit system architectures that would benefit from higher power sources. Consequently, the motivation is to consider a direct carrier launch transmit function. Direct carrier generation demonstrates the advantage of lower cost and potentially higher performance as opposed to heterodyne schemes. For example, the minimization of spurious responses. However, to be certain that this statement has validity requires the development of a number of methods to quantify our analytic approaches and then back up these assumptions with measurements. To quantify our system analysis we considered a different tactic to approach both cascade and feedback RF transmitter functions. A contribution methodology is developed which readily sites offending stages in a given system architecture. In addition, the technique provided for an optimization and a less ad-hock approach to a stage by stage block assignment. The technique is applicable to both open loop cascaded as well as feedback systems. An experiment based on a front end preselector included band pass filters, low noise amplifier (LNA) and balanced mixer. Adjustments in the filter response by slight retuning of the input and output ports, bias control of the LNA and adjustment of the LO injection level into the mixer provided a 3 dB

increase in dynamic range. The process is tractable, accountable to network block adjustments in parameters, and could serve as an algorithm in computer aided system design.

Although optimization of the cascade system for a transmit function is always open to improvement, we decided to select a different topology based on simplicity and the potential for improved efficiency. Therefore, a phase locked power oscillator is investigated. This topology reduces the risk to the generation of spurious and is amenable to integration. The phase lock arrangement permits a one to one correspondence in the behavior of a locked power oscillator against a corresponding lower power, lower noise source. The power output and locked frequency characteristics are directly obtained from the lower power source, or a harmonic when operated as a phase locked multiplier. Thus tunable power oscillators are a main focus in this investigation, and due to the higher efficiency of high voltage devices, a focus on higher voltage tunable resonators is also pursued. Therefore, an investigation of thin-film ferroelectric varactors with high breakdown voltage is warranted. This investigation targets tunability, excess noise, unique properties of ferroelectric devices near 0 Volts operation when applied in phase lock systems, operation near voltage breakdown, and finally linearity when applied in voltage controlled oscillators. While the MIM BST varactor showed tunability in excess of 25 % the IDC BST varactor was less than 5 %. Nevertheless, the operation of these varactors at large incidental RF voltages and power, over 1.5 W at 1.6 GHz, demonstrated no degradation of noise or signal distortion, and the oscillators proved to be quite linear in tuning. Without resorting to linearizing techniques, the BST varactor permitted less than a 3% variation in best straight line fit of output frequency versus tuning voltage. In addition, when the BST varactor is not limited by leakage current, at higher applied tuning voltages, tuning linearity was better than 1%.

The assessment of excess noise in BST varactors and the implication in phase noise degradation in oscillators is investigated. The various sources of noise in oscillators must be categorized, as noise in oscillators is dependent on the varactor type, the active device, i.e. FET versus bipolar, and the quality of the varactor and resonator element. Since oscillator tuning gains utilizing

BST varactors were quite moderate, for example, 300 kHz/volt to 1 MHz/volt, it was difficult to isolate excess noise specifically from the BST varactor or from the additive noise of the active device. However, there are a number of distinguishing noise characteristics that are obtained clearly irrespective of tuning gain. First, operation of the BST varactor near zero tuning volts, demonstrates no significant shot noise of current, as there is no forward biased junction effect. Further investigation shows prior to BST varactor voltage breakdown, and not unlike the junction varactor, appreciable increase in oscillator phase noise approaching the carrier frequency is noted. In the circuits studied in this dissertation, an increased noise slope approaching 40 dB/decade was documented. This result, measured in the phase noise domain, demonstrates a slope in noise that is not unlike random walk in frequency. Consequently, our conjecture is this noise event could be due to self heating of the dielectric as well as the top metal plate and interdigital fingers, as leakage current is present in these devices. This raises a note associated with the surface quality of the BST, as some IDC units and to a limited extent MIM devices showed significant leakage current at initial application of voltage and a corresponding increase in baseband low frequency noise. This leakage current, and corresponding rise in noise density demonstrated a hysteresis property. As an example, initial application of voltage V_1 showed a large low frequency noise density. Subsequent soakage of the BST dielectric at a second higher voltage, V_2 , and subsequent return to V_1 reduced the noise voltage density and leakage current. This was particularly prevalent for the MIM topologies. To the extent that leakage current and noise density rise significantly, it is difficult to verify this in an oscillator function. The rapid increase in leakage current is directly linked to startup resistance. Consequently, increased leakage current is accompanied by a resonator Q degradation and finally we find the case where the oscillator open loop gain is insufficient to permit oscillator startup. An increased $C - V$ slope with an increased tune gain, K_o , would help isolate varactor excess noise just as it does in the junction varactor based oscillators, see Figures 2.7 and equation (2.34).

Key to the phase lock multiplier is the development of efficient power oscillators. In this work we reported higher efficiency power oscillators based on Si-GaN HFETs and IMFETs coupled

with BST varactors. In addition, we outlined an integrated design flow that couples printed circuit card layout with active components, non linear harmonic balance and electromagnetic simulation. The resulting hybrid network which is synthesized from mapping routines developed for the reflection plane, permitted first pass success of a 3.8 to 5.4 GHz oscillator. These oscillators represent wide range, low noise references, and are subsequently applied to the PLM network for the purpose of phase locking the power oscillator.

The design of high efficiency power oscillators is approached from two points of view. One, by using the description for the limiting function of the oscillator, the exponential characteristic for the bipolar and the square law characteristic for the FET. The other approach is through optimization of the load termination to maximize output power. We applied this technique in a straightforward manner to realize optimum terminations for class A power amplifiers. Low loaded Q_L resonators, between 5 and 10, are placed in the feedback loop with an adjustable delay. Then we proceeded to tune the gate voltage relative to the pinch off voltage of the HFET, using the results provided by the describing function for a FET to maximize efficiency. Permitting V_o to approach twice the supply voltage, and then providing for a narrow conduction angle maximizes conversion efficiency. These techniques lead to power oscillators at 6 GHz and 2.4 GHz with output powers of 33 dBm and 34.5 dBm respectfully at efficiencies of 26% and 40.3%. The unlocked, free running phase noise of both oscillators exceeded -150 dBc/Hz at 1 MHz offset from the carrier. Bench marked against several power oscillators based on AlGaIn/GaN device technology, these designs presented in this work rated highest for the composite output power, efficiency, operating frequency and phase noise per the figure of merit discussed in section 6.2.

The phase lock multiplier utilizing a power oscillator which is BST varactor based, a low noise reference oscillator developed using a co-design technique, and the unique issues which exist in applying BST based oscillators in a PLL environment are discussed. Avoidance of phase lock hang requires careful control of tuning near zero volts as the oscillator control sense reverses and the loop is forced to hang. Fortunately, for voltages above zero volts, the BST varactor embedded in a VCO provides excellent tuning linearity. This property of varactor

tuning linearity is intrinsic to the ferroelectric varactor. As the capacitance dependency on the electric field and the field relation to the applied voltage is a square law, all of the tuning oscillators realized in this work had nearly linear tuning. Investigation of the field based model was pursued for both the MIM and IDC varactors and variations from the physics based model are noted. For the MIM varactor we found reasonable agreement without supplementing the equation with a curve fitting polynomial based on C-V measurements. This was also true with the IDC varactor although in the high field, high tuning voltage regime, we were forced to use the polynomial derived C-V curve. We show that the need for this correction and the affect are due to excessive device leakage current which must be part of the device model. Nevertheless, with good tuning linearity present, it is therefore possible to monitor the tune line and the near zero tune line condition in applications, and avoid the phase lock latch up issue.

The co-design technique which couples electromagnetic and harmonic balance analysis proved to be an excellent tool to permit design and first pass success to meeting the tuning characteristics for a VCO. The co-design method is further supplemented with an active device modification technique. This approach demonstrates the ability to successfully modify the transistor limiting characteristic to effectively absorb resonator parasitics. The resulting hybrid VCO, previously discussed, was implemented as a switched oscillator pair and demonstrated the application of these ideas. The figure of merit reported, based on current accepted definitions or modified to include the tuning range which was latter introduced in [191], are bench marked. As a result, the oscillators discussed in this work scored among the highest merit function.

A number of different measurement techniques are required in assessing the designs discussed in this work. Some simplified, nevertheless accurate methods were developed to assist in that effort. Varactor capacitance, Q , and noise were addressed with measurement procedures specific to the problem at hand and using the actual measurement problem in a “bootstrap” form to assist in the measurement process. This was particularly the case for the characterization of oscillator phase noise especially close to the carrier and for microphonics. Although the signal

analyzer is documented here for the observation of power oscillator microphonics, see Figure 5.31, the issue is significantly easier to identify in a measurement receiver, converting a 6 GHz RF channel to baseband audio. Finally, properties of the PLM germane to modulation and distortion are highlighted.

Chapter 9

Future Work

Additional work improving the $C - V$ sensitivity of the BST varactor is desirable. This would include optimizing the geometry of the device layout, attempts to minimize the fringe coupling and perfecting mounting techniques. Specifically, any reduction in parasitics and raising the self resonant frequency of the device, perhaps by flip chip techniques and adding solder bumps, or edge plating the ceramic substrate. The excess noise, if it is significant, should further be addressed. However, this is secondary to first, improving the C-V sensitivity followed by improving the unloaded, Q_{UL} , of the varactor and subsequently obtaining very low leakage current. This is acutely important as the demands by the BST components should be very low supply current however, operating at high voltage. The requirement for high voltage in itself is a problem, that is only further complicated if the current demands are high. The motivation for high voltage is the need for the tuning line requirements of BST and any technique used must be extremely efficient and represent simple hardware. The generation of low current high voltage techniques fall into the class of voltage charge pump circuits. One circuit technique is based on switching charge storage in a ladder bank of capacitors, and the other technique, the reversal of switching current through an inductor. Capacitive voltage multipliers are particularly attractive as it is possible to integrate these into BST technology and embed the technique into the construction of the varactor itself. A technique of bootstrapping is applicable whereby the high

RF power generated by the oscillator itself, under BST varactor control, is used to clock an external diode-capacitance charge pump voltage multiplier. Thereby generating the required high voltage tuning line potential.

The current BST breakdown voltage is sufficient, at 100-200 volts this is adequate to entertain most power oscillator applications. Comparative dielectric technologies such as alumina, ceramic, and porcelain, which have DC working voltages upwards of 250 volts and greater currently operate in small dense packages. This should be a reasonable target goal for BST, especially if BST varactors are to be incorporated into high power amplifier amplifier tunable matching networks.

Development of efficient power oscillators beyond 6 GHz with output power of 37 dBm find applications where tower mount systems are not desired. High efficiency with no forced cooling is the goal as these units would be located at the base site. The required added power is driven by the length of waveguide or coax loss which is distant from the antenna, up to 300 meters distance is not uncommon.

The approach to power oscillator development when utilizing a two port power amplifier with resonator feedback is based on load selection for maximizing voltage and current swing at the drain. This approach proved effective for achieving oscillator load efficiency up to 40%. Further improvements would require modeling the intrinsic port impedances of the active device, particularly the active device output.

Introduction of modulation and the measured frequency response of the BST varactor port should be completed. Modulation port time constants, post tuning drift, memory effects and modulation hysteresis should be addressed. The same conditions apply to the tuning port. Therefore a nonlinear model for the BST varactor is desirable. The current physics based model discussed in this work appears to be adequate for addressing tuning linearity except for the absence of the necessary leakage term. Additional terms would add elements that would capture increased excess noise near breakdown and capacitance drift due to self heating that could lead to post tuning drift problems. This would be in addition to phenomena such as

dielectric absorption and memory effects which are best captured in phase lock loop work.

Envelope modulation of the power oscillator outside the loop needs study. Circuit design of PIN modulators and the required oscillator load isolation should be evaluated. The desire is to minimize the frequency correction required by the phase lock loop. The envelope modulation rate would be bounded by the loop closed loop bandwidth and modulation rates greater than this would not be corrected by the system.

REFERENCES

- [1] Roger L. Freeman, *Telecommunication System Engineering*. New York, NY: Wiley-IEEE Press, 2004.
- [2] Michael F. Young. June (2004) Planning a Microwave Link [Online]. Available: URL <http://www-ydi.com>
- [3] Rahul Magoon, Alyosha Molnar, Jeff Zachan, Geoff Hatcher, Woogeun Rhee, "A Single-Chip Quad-Band (850/900/1800/1900 MHz) Direct Conversion GSM/GPRS RF TRansceiver with Integrated VCOs and Fractional-N Synthesizer," *IEEE Journal of Solid State Circuits.*, vol. 37, no. 12, pp. 1710–1720, 2002
- [4] H.T. Friss, "Noise figure of radio receivers," *Proc. IRE.*, vol. 32, no. 6, pp. 419–422, July, 1944.
- [5] R.Pettai, *Noise in Receiving Systems*. New York, NY: John Wiley and Sons, 1984.
- [6] Kenneth M. Johnson, "Large signal GaAs MESFET oscillator design," *IEEE Trans. on Microwave Theory and Techniques*, Vol. MTT-27, March 1979, pp.217–227.
- [7] R.C. Sagers, "Intercept point and undesired responses," *IEEE Trans. Veh. Technol.*, vol. 32, no. 1, pp. 121–133, February, 1983.
- [8] S.A. Maas "Third-order intermodulation distortion in cascaded stages ," *IEEE Microw. Guid. Wave Lett.*, vol. 5, no. 6, pp. 189–191, June, 1995.
- [9] G. Gonzalez, O. J. Sosa, "On the design of a series-feedback network in a transistor negative-resistance oscillator,," *IEEE Trans. On Microwave Theory and Techniques*, vol. 47, no. 1, Jan. 1999, pp. 42–47.
- [10] Jae-Ho Yoon, Nam-Young Kin, "A new harmonic noise filtering vco and mixer co-design", *Proceedings of the 1st European Microwave Integrated Circuits Conference*, Sept. 2006, pp. 352–355.
- [11] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE*, New York: McGraw-Hill, 1988.
- [12] H. K. Gummel and H. C. Poon, "An Integral Charge Control Model of Bipolar Transistors," *Bell Sys. Tech. J.*, vol. 49, p. 827, May/June, 1970.
- [13] A.Victor, J. Nath, "Circuit co-simulation and measurement techniques applied to voltage-controlled oscillator design," *IET Microw. Antennas Propagation.*, vol. 2, no. 8, December 2007, pp. 922–928.
- [14] Ohira T., Araki K, "Oscillator frequency spectrum as viewed from resonant energy and complex Q factor," *IEICE Electron. Exp.*, 2006, 3, no. 16, pp. 385–389.

- [15] Microwave Office, "MWO/VSS Getting Started Guide". Applied Wave Research. El Segundo, California. July 2005. accessed October 2005. <http://www.appwave.com>.
- [16] Fuchs M., "Simple and accurate measurement of loaded Q factor of microwave oscillators using thermal noise injection," *20th European Microwave conf.*, October 1990, vol. 1, pp. 512–516.
- [17] Kenneth K. Clarke, "Design of self limiting transistor sine-wave oscillators" *IEEE Transactions on Circuit Theory*, vol. 13, no. 1, March 1966, pp. 58–63.
- [18] Clarke-Hess, *Communication Circuits Analysis and Design*, Addison-Wesley, 1971.
- [19] W.N Cheung, "The effect of saturation on transistor oscillators," *International Journal Electronics*, Vol. 39, No. 1, pp. 17–28
- [20] Kwok-Keung M. Cheng, Kwok-Po Chan, "Power optimization of high-efficiency microwave MESFET oscillators," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 48, May 2000, pp. 787–790.
- [21] Max W. Medley, *Microwave and RF Circuits: Analysis, Synthesis and Design.*, Norwood MA: Artech House, 1993
- [22] Hati, A.; Howe, D.A.; Walls, F.L; Walker, D. "Noise figure vs. PM noise measurements: a study at microwave frequencies ," *IEEE Frequency Control Symposium.*, pp. 516–520, May 4–8, 2003.
- [23] Garmendia, N.; Portilla, J.; "Study of PM noise and noise figure in low noise amplifiers working under small and large signal conditions," *IEEE Microwave Theory and Techniques Symposium.*, pp. 2095–2098, June 3–8, 2007.
- [24] A.M. Victor and M.B. Steer, "Transceiver cascade system analysis and design via a contribution method," *Int. J. on RF and Microwave Computer Aided Engineering.*, pp. 338–345, July 2006.
- [25] W.W. Mumford and E.H. Schelbe, *Noise Performance Factors in Communication Systems.*, Horizon House, 1968.
- [26] Xing Wang, Pearson, L.W., "Design of coupled-oscillator arrays without a posteriori tuning," *IEEE Trans. on Microwave Theory and Techniques*, vol, 53., Issue 1., 2005, pp. 410–413.
- [27] S. Wane, "Partition and global methodologies for IC, package and board co-simulation In SiP applications," *IEEE European Microwave Conference, 2007*, Oct. 9–12, pp. 1249–1252.
- [28] Lawson, M.F. Spooner, T. Ficaiora, P.J., "Excess noise induced in metal resistors as a result of dynamic processes," *Journal of Applied Physics*, vol. 71, Iss. 7, Apr. 1992, pp. 3623–3625.

- [29] Pekau, H.; Haslett, J.W., "Cascaded noise figure calculations for radio receiver circuits with noise-aliasing properties," *IEEE Proceedings Circuits, Devices and Systems*, vol. 153, Iss. 6, Dec. 2006, pp. 517–524.
- [30] Richard Q. Lane, "A simple calibrator for noise figure/gain meters," *ARFTG Conference Digest-Spring, 39th*, June 1992, pp. 63–70.
- [31] Hansen, F. "Desensitization in transistorized PM/FM-receivers," *Vehicular Technology Conference, 1967. 18th IEEE*, Dec. 6–8, 1967, Page(s):78 – 86.
- [32] Gros Lambert, J.; Rubiola, E.; Brunet, M.; Giordano, V.; "Frequency flicker limitation in dual oscillator phase noise measurement instruments," *Precision Electromagnetic Measurements Digest, 2000 Conference*, 14–19 May 2000, Page(s):449 – 450.
- [33] A.J. Cote, Jr., "Matrix analysis of oscillators and transistor applications," *IRE Trans. on Circuit Theory*, vol. CT-5, Sept. 1958, pp. 181–188.
- [34] Nielinger, N; "Three-port oscillator design with PUFF," *IEEE Transactions on Education*, Vol. 42, Iss. 4, Nov 1999, pp. 344–348.
- [35] Mediavilla, A., Tazon, A., Garcia, J.L., "An improved transient characterization of three terminal microwave oscillators," *International Journal of electronics*, Vol. 63, Oct 87, Issue 4, pp. 533–540.
- [36] Jean-Christophe Nallatamby, Michel Prigent, Marc Camiade, Juan J. Obregon, "Extension of the Leeson formula to phase noise calculation in transistor oscillators with complex tanks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 3, March 2003, pp. 690–696.
- [37] Lindsey, William C.; Chie, Chak Ming; "Identification of power-law type oscillator phase noise spectra from measurements," *IEEE Transactions on Instrumentation and Measurement*, Volume 27, Issue 1, March 1978 Page(s):46 – 53.
- [38] Arsenia Chorti, Mike Brookes, "A spectral model for RF oscillators with power-law phase noise," *IEEE Transactions on Circuits and Systems–I*, Vol. 53, No. 9, Sept. 2006, pp. 1989–1999.
- [39] T.E. Parker, "Random walk frequency fluctuations in SAW oscillators," *IEEE Frequency Control Symposium-40th*, 1986, pp. 241–251.
- [40] Harris, M.V., "An investigation into the frequency-settling time and post-tuning drift of broadband microwave varactor-tuned oscillators," *Second International Conference on Frequency Control and Synthesis*, April, 1989, pp. 97–102.
- [41] Yun Li, Shichang Feng, Yashua Luo, "Conformal mapping of S-parameters of a three-terminal network from its feedback impedance admittance," *IEEE International Symposium on Circuits and Systems*, pp. 545–548, May 8–11, 1989.

- [42] K. Harada, "An S-parameter transmission model approach to VCO analysis," *RF Design*, March, 1999, pp. 32–42.
- [43] Lucia Cascio, "Comments on "general oscillator characterization using linear open-loop S-parameters,"" *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, January 2002, pp. 226–228.
- [44] Edward M. Cherry, "Loop gain, input impedance and output impedance of feedback amplifiers," *IEEE Circuits and Systems Magazine*, vol.8, no.1, 2008, pp.55–71.
- [45] Takashi Ohira, "Rigorous Q-factor formulation for one- and two-port passive linear networks from an oscillator noise spectrum viewpoint," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 52, Dec. 2005, pp. 846–850.
- [46] Jan R. Westra, Chris J.M. Verhoeven, Arthur H.M. van Roermund, *Oscillators and Oscillator Systems, Classification, Analysis, Synthesis*, Kluwer Publishing, 1999.
- [47] Johan Kwon, I.S. Kim, "Oscillation condition and the uncertainty principle," *IEEE International Microwave Symposium*, June 3–8, 2007, pp. 2161–2164.
- [48] D.M. Pozar, *Microwave Engineering*, Reading, MA. Addison-Wesley, 1990.
- [49] "Noise Figure Measurement Accuracy—The Y-Factor Method," Agilent Technologies, Application Note 57-2
- [50] Agilent Technologies, "Spectrum and Signal Analyzer Measurements and Noise Note 1303," July 2, 2009. accessed October 2009. <http://www.cp.literature.agilent.com/litweb/pdf/5966-4008E.pdf>.
- [51] Nitronex Corporation, "NPTB0004 Data Sheet", NDS-002 Rev.3, May 2009, accessed December, 2009. http://www.nitronex.com/design_support.html#NPTB00004.
- [52] W.E. Pastori, "A Review of Noise Figure Instrumentation," *Microwave Journal*, pp.50–60, April 1983.
- [53] Alan M. Victor, Michael B. Steer, "Improved Y factor noise measurement using the second stage contribution to advantage," *Automatic Radio Frequency Group 65th Conference*, June 17, 2005.
- [54] Juan-Mari Collantes, Roger D. Pollard, Mohamed Sayed, "Effects of DUT mismatch on the noise figure characterization: A comparative analysis of two Y-factor techniques," *IEEE Trans. Instrumentation and Measurements*, pp. 1150–1156, Vol51, No.6, December 2002.
- [55] J. Riordan, *Combinatorial Identities*. New York, NY: John Wiley and Sons, 1968.
- [56] B. Cantrell, J. McConnell, A. Thurber, D. Newton, "Low spurious signal homodyne digital receiver," *IEEE Proceedings Intl. Circuits and Systems, ISCAS '04.*, vol. 4, pp. 153–156, May 23–26, 2004.

- [57] Silvio A. Cardero, "Calculate the effect of RF building blocks on AM and PM Noise," *Microwaves and RF.*, pp. 56–63, Dec. 2000.
- [58] Kenneth V. Puglia, "Phase noise analysis of component cascades," *IEEE Microwave Magazine.*, pp. 71–75, Dec. 2002.
- [59] Alan Victor, "Phase noise characteristics and measurements for wireless and microwave systems," *IEEE International Microwave Symp Workshop.*, Session–WSH, June 2008.
- [60] Hoi-Yee Ng, Kim-Fung Tsang, Chug-Ming Yuen, "Phase-noise measurement of free-running microwave voltage-controlled oscillators," *Microwave and Optical Technology Letters.*, Vol.45, No.3, May 5,2005,pp.216–217.
- [61] Chung Ming Yuen, Kim Fung Tsang, "Automated tracking system for phase-noise measurement," *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, Vol. 52, Issue 5., May 2005, pp. 834–836.
- [62] Mark Roos, "SINAD and BER for production testing of RFICs" *ARFTG Conference Digest- Fall 48th*, Vol.30, Dec 1996,pp. 94–98.
- [63] C. Lanschutzer, A. Springer, L. Mauer, Z. Boos, R. Weigel, "Integrated adaptive LO leakage cancellation for W-CDMA direct upconversion transmitters," *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE*, June 2003, pp. 19–22.
- [64] Shuhei Yamada, Olga Boric-Lubecke, Victor M. Lubecke, "Cancellation technique for LO leakage and DC offset in DC systems," *IEEE MTT-S 2008*, pp.1191–1194.
- [65] Ali Boudiaf, Dider Bachelet, Christian Rumelhard, "A high-efficiency and low-phase-noise 38-GHz pHEMT MMIC tripler," *IEEE Microwave Theory and Techniques*, vol.48, Dec 2000, pp.2546–2553.
- [66] Camilla Karnfelt, Rumien Kozhuharov, Herbert Zirath, Ilcho Angelov, "High-purity 60-GHz-band single-chip x8 multipliers in pHEMT and mHEMT technology," *IEEE Microwave Theory and Techniques*, vol 54, June 2006, pp.2887–2898.
- [67] Eric W. Strid, "Measurement of losses in noise-matching networks," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-29, March, 1981, pp. 247–252.
- [68] W.P. Robins, *Phase Noise in Signal Sources.*, Peter Peregrinus Ltd.,1982.
- [69] Kyoo Hyun Lim, Chan-Hong Park, Dal-Soo Kim, Beomsup Kim, "A low-noise phase-locked loop design by bandwidth optimization," *IEEE Journal of Solid-State Circuits*, Vol.35, June 2000, pp. 807–815.
- [70] William F. Egan, "Modeling Phase Noise in Frequency Dividers," *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol.37, No.4, July 1990, pp.307–315.
- [71] M.M. Driscoll, "Phase noise performance of analog frequency dividers," *IEEE Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 37, Issue 4, July 1990, pp. 295–301.

- [72] Matthias Rudolph, Fabrizio Bonani, "Low-frequency noise in nonlinear systems," *IEEE Microwave Magazine*, Feb. 2009, pp. 84–92.
- [73] Eva S.Ferre-Pikal, Fred L. Walls, Craig W. Nelson, "Guidelines for designing BJT amplifiers with low 1/f AM and PM noise," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol.44, no.2, March 1997, pp.335–343.
- [74] M.A. Do, J.J. Liu, K.S. Yeo, J.G. Ma, "Analysis of LO leakage in CMOS mixer by cadence spectreRF direct conversion application," *IEEE Circuits and Systems, 2004 Asia-Pacific Conference*, Dec. 6–9, 2005, 309–312, Vol. 1.
- [75] Shuhei Yamada, Loga Boric-Lubecke, Victor M Lubecke, "Cancellation techniques for LO leakage and DC offset in direct conversion systems," *IEEE MTT-S International*, June 2008, pp.1191–1194.
- [76] Danny Elad, A.P.S. Khanna, Irene Armenta, Jerry Quibuyen, Robert Pumares, "Low cost Ka band transceiver for digital radios," *IEEE 29th European Microwave Conference 1999*, Oct 1999, Vol.3, pp.287–290. Munich.
- [77] Rick Poore, "Accurate simulation of mixer noise and oscillator phase noise in large RFICs," *IEEE Asia Pacific Microwave Conference*, 1997, session 3P01–11, pp.357–360.
- [78] Website, "Signal Source Analyzer for Phase Noise and VCO test, 1MHz to 26GHz with integrated Spectrum Analyzer", *Rhode and Schwarz FSUP Signal Source Analyzer*, 06.02, accessed December, 2009, <http://www.rohde-schwarz.com>
- [79] A. Hajimiri, "Noise in phase-locked loops," *IEEE 2001 Southwest Symposium on Mixed-Signal Design*, 2001, pp. 1–6.
- [80] L.D. Cohen "Low phase noise oscillator with flicker noise suppression circuit," *IEEE Microwave Symposium Digest 1992*, Jun 1–5, 1992, vol. 2, pp. 1081–1084.
- [81] H.M. Greenhouse, "Design of planar rectangular microelectronic conductors," *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. PHP-10, June 1974, pp. 101–109.
- [82] Behzad Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, Vol. 31, March, 1996, pp. 331–343.
- [83] J.Obregon, A.P.S. Khanna, "Exact derivation of the non-linear negative resistance oscillator pulling figure," *IEEE Trans. Microwave Theory and Tech.*, vol. 30, 1982, pp. 1109–1111.
- [84] "5.0–14.0 GHz GaAs MMIC Packaged Driver Amplifier", February 2008, Rev 03-Feb-08. December, 2009. <http://www.mmixbroadband.com/Data/Document-Library/CMM0511-QT.pdf>.
- [85] A. Hati, D.A. Howe, F.L. Walls, D. Walker, "Noise figure vs. PM noise measurements: A study at microwave frequencies," *IEEE International Frequency Symposium 2003*, pp. 516–520.

- [86] C.W. Nelson, F.L. Walls, C.K. Boggs, "Extending the range for precision AM noise measurements," *IEEE International Frequency Control Symposium*, 1996, pp. 854–857.
- [87] J.-C. Nallatamby, M. Progent, M.Camiade, J.J. Obregon, "Phase Noise in Oscillators—Leeson formula revisited," *IEEE Trans. Microwave Theory Tech.*, MTT-51, 2003, pp.1386–1394.
- [88] H.J. Siweris, B. Schiek, "Analysis of noise upconversion in microwave FET oscillators," *IEEE Transactions Microwave Theory and Techniques*, MTT-33, Match, 1985, pp.232–242.
- [89] G.Sauvage, "Phase noise in oscillators:A mathematical analysis of Leeson's model," *IEEE Transactions Instrumentations Measurements*, IM-26, 1977, pp.408–410.
- [90] W.A. Edson, "Noise in oscillators," *Proceedings of the IRE*, vol.48, August 1960, pp. 1454–1466.
- [91] "HMC358MS8G / HMC358MS8GE - MMIC VCO SMT w/ Buffer Amp, 5.8 - 6.8 GHz," V04.0607., September 2,2007. *HMC358*. Hittite Microwave Corporation. <http://www.hittite.com/products/view.html/view/HMC358MS8G>.
- [92] M.J.Underhill, "The need for better varactor diodes in low phase noise tunable oscillators," *Microwave and Millimeter-Wave Oscillators and Mixers, IEE Colloquim*, Dec 1, 1998, pp.5/1–5/6.
- [93] M.V. Harris, "An investigation into the frequency-settling time and post-tuning drift of broadband microwave varactor-tuned oscillators," *IEEE Frequency Control and Synthesis Intl. Conf. 1989*, Apr. 1989, pp. 97–102.
- [94] A. Victor, J. Nath, D. Ghosh, B. Boyette, J.-P.Maria, M.B. Steer, A.I. Kingon, G.T. Stauf, "Noise characteristics of an oscillator with a barium strontium titanate (BST) varactor," *IEE Proc.-Microw. Antennas Propag.*, Vol.153, No.1, February 2006, pp.96–102.
- [95] Alan Victor, Jayesh Nath, "Design of a C-band voltage controlled oscillator using and electromagnetic–harmonic balance co-design technique," *Proceedings of Asia-Pacific Microwave Conference 2007*, December 11–14, 2007, pp.1–4
- [96] Alan Victor, Michael B. Steer, "Reflection coefficient shaping of a 5–GHz voltage tuned oscillator for improved tuning," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 55, December 2007, pp. 2488–2494.
- [97] A. Jamil, T.S. Kalkur and N. Cramer, "A Verilog-A modeling of ferroelectric high-K capacitors for tunable circuit applications," *Integrated Ferroelectrics*, 66, 2004, pp. 163–170.
- [98] A. Kabir, A. Jamil, Y. Zhang, T. S. Kalkur, "Voltage Controlled Oscillators with Ferroelectric Capacitors," *IEEE Freq. Control. Sym.*, May 2008, pp 414–417.

- [99] A. Jamil, T. S. Kalkur, N. Cramer, "Tunable Ferroelectric capacitor-based Voltage Controlled Oscillator," *IEEE Trans. Ultrason. Ferroelect. Freq. Cntrl.*, vol. 54, no. 2, Feb. 2007, pp. 222–226.
- [100] M. Al-Ahmad, C. Loyez, N. Rolland, P. A. Rolland, "Wideband BST-based Tuning of Voltage Controlled Oscillator," *Proceedings Asia Pacific Microw. Conf.*, Dec. 2006, pp. 468–471.
- [101] M. Norling, A. Vorobiev, H. Jacobsson, S. Gevorgian, "A low-noise K-band VCO based on room-temperature ferroelectric varactors," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 2, Feb. 2007, pp. 361–368.
- [102] D.T. Hess, "Equivalence of FM threshold extension receivers," *IEEE Trans. on Communications Technology*, COM-16, No. 5, Oct 1968, pp. 946–948.
- [103] Floyd M. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Transactions on Communications*, COM-28(11), Nov. 1980, pp. 1849–1858.
- [104] *The RF Capacitor Handbook*, American Technical Ceramics, 5th printing, 1997
- [105] J.K.A. Everad, "A review of low noise oscillator theory and design," *IEEE International Frequency Control Symposium 1997*, 1997, pp. 909–918.
- [106] M. Randall, T. Hock, "General oscillator characterization using linear open-loop S-parameters," *IEEE Transactions on Microwave Theory and Techniques*, vol 49, June 2001, pp. 1094–1100.
- [107] A. Asija, A. Gundavajhala, "Quick measurement of unloaded Q using a network analyzer," *RF design*, October 94, pp. 48–52.
- [108] D. Kajfez, E.J. Hwan, "Q-factor measurement with network analyzer," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, July 84, pp. 666–670.
- [109] Agilent, "Advanced impedance measurement capability of the RF I-V method compared to the network analysis method," *Agilent Application Note 1369-2*
- [110] Frederick W. Grover, *Inductance Calculations: Working Formulas and Tables*, Dover Publishing, Inc., New York, 1946
- [111] R. Lundin, "A handbook formula for the inductance of a single-layer circular coil," *Proceedings of the IEEE* Sept. 1985, Volume:73, Issue 9 pp.1428– 1429.
- [112] "ATC 180 R series NPO porcelain ultra-low ESR multilayer capacitors", American Technical Ceramics, ATC 001-810 Rev. E 12/00; pp. 1-8, May 2009. www.icquest.ru/tech/atc/180r.pdf.
- [113] Agilent Technologies, "8 hints for successful impedance measurements-Application Note 346-4".©2000. January 2008, http://www.agilent.com/find/component_test.

- [114] “Therma-Bridge AlN Thermal Management Device”, B-series ver4. 9/09. April 2009. http://www.ims-resistors.com/Therma_bridge.html
- [115] Nadia K. Pervez, Robert A. York, “Geometry-dependent quality factors in $Ba_{0.5}Sr_{0.5}Ti_{0.3}$ parallel-plate capacitors,” *IEEE Trans. on Microw. Theory and Techs.*, Vol. 55, February 2007, pp.410–417.
- [116] A.Adar, R. Ramachandran, “An HBT MMIC wideband VCO,” *IEEE MTT-S Digest 91*, 1991, Session E-1, pp. 247–250.
- [117] M.P. Sinha, “A study on broad-banding the tuning ratio for varactor -tuned oscillators,” *Microwave and Optical Technology Letters*, John Wiley, Vol. 5, Issue 13, Dec. 5, 1992, pp. 671–673.
- [118] Paul C. Wade, “Novel F.E.T. power oscillator,” *Electronics Letters*, Vol.14, No. 20, Sept. 28, 1978, pp.672-674.
- [119] Klymyshyn, D.M.; Kumar,S.; Mohammadi,A., “Frequency stabilized direct GMSK modulator ,” *The Ninth IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, Vol.3, 8–11 Sept. 1998, pp.1319 – 1324.
- [120] Sowlati, T. Rozenblit, D. Pullela, R. Damgaard, M. McCarthy, E. Dongsoo Koh Ripley, D. Balteanu, F. Gheorghe, “ Quad-band GSM/GPRS/EDGE polar loop transmitter,” *Solid-State Circuits, IEEE Journal of*, Dec. 2004 Volume: 39, pp. 2179– 2189.
- [121] R. Adler, “A study of locking phenomena in oscillators,” *Proc. IRE*, Vol. 34, 1946, pp.351–357.
- [122] Xianyang Zhu; Lang Jen, “Phase-locking of high power microwave oscillators with no limitation to injection power ratios” *Microwave Conference Proceedings, 1997. APMC '97*, 1997 Asia-Pacific Volume 1, 2–5 Dec. 1997 pp.345 – 348 vol.1.
- [123] Fotis Plessas, Grigorios Kalivas, “A 5-GHz injection-locked phase-locked loop,” *Microwave and Optical Technology Letters*, vol. 46, no.1, July 5, 2005, pp. 80-84.
- [124] Chen, S.F.; Lee, Y.B.; Bosen Tzeng; Tang, C.C.; Chiu, C.; Yu, R.; Lin, O.; Ke, L.W.; Wu, C.P.; Yeh, C.W.; Chen, P.Y.; Dehng, G.K., “GSM/EDGE transmitter in 0.13-um CMOS using offset phase locked loop and direct conversion architecture,” *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, June 17 2008–April 17 2008, pp.581 – 584.
- [125] Pamarti, S. Jansson, L. Galton, “I. A wideband 2.4-GHz delta-sigma fractional-NPLL with 1-Mb/s in-loop modulation,” *Solid-State Circuits, IEEE Journal of Publication*, Vol. 39, January 2004, pp.49–62.
- [126] Sowlati, T. Rozenblit, D. Pullela, R. Damgaard, M. McCarthy, E. Dongsoo Koh Ripley, D. Balteanu, F. Gheorghe, “ Quad-band GSM/GPRS/EDGE polar loop transmitter,” *Solid-State Circuits, IEEE Journal of*, vol. 39, Dec. 2004, pp. 2179–2189.

- [127] P. Denniss, S.E. Gibbs, "Solid-state linear FM/CW radar systems:their promise and their problems," *IEEE MTT-S International Microwave Symposium*, 1974, pp. 340–342.
- [128] E. Marazzi, V. Rizzoli, "The design of linearizing networks for high power varactor-tuned frequency modulator," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-28, July 1980, pp. 767–773.
- [129] D. Kajfez, "Linearity limits of the varactor-controlled oscillator-modulator circuits," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-33, July 1985, pp. 620–625.
- [130] Alan Victor, Jayesh Nath, Peter G. Lam, Vrinda Haridassan, Zhiping Feng, Jon-Paul Maria, Michael B. Steer, "Investigation and modeling of tuning linearity of voltage controlled oscillators using BST thin-film varactors," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, to be submitted for publication, April 2009.
- [131] Dean F. Peterson, "Varactor properties for wide-band linear-tuning microwave VCO's" *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-28, Feb. 1980, pp.110–119.
- [132] David R. Chase, Lee-Yin Chen, Robert A. York, "Modeling the capacitive nonlinearity in thin-film BST varactors," *IEEE Transactions on Microwave Theory and Techniques*, vol.53, no.10, Oct 2005, pp. 3215–3220
- [133] S.M. Sze, Kwok K. NG *Physics of Semiconductor Devices*, New York, NY: Wiley-Interscience, 2007.
- [134] Emad Hegazi, Asad A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE Journal of Solid State Circuits*, vol. 38, no. 6, pp. 1033–1039, June 2003.
- [135] Dean F. Peterson, "Varactor properties for wide-band linear-tuning microwave VCO's" *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-28, Feb. 1980, pp.110–119.
- [136] David R. Chase, Lee-Yin Chen, Robert A. York, "Modeling the capacitive nonlinearity in thin-film BST varactors," *IEEE Transactions on Microwave Theory and Techniques*, vol.53, no.10, Oct 2005, pp. 3215–3220
- [137] G.R. Basawapatna, R.B. Stancliff, "A unified approach to the design of wide-band microwave solid-state oscillators," *IEEE Trans. Microwave Tech.*, MTT-27, vol. 5, no. 5, May 1979, pp.379–385.
- [138] Abu Kabir, Asad Jamil, Yulan Zhang, T.S. Kalkur, "Voltage controlled oscillators with ferroelectric capacitors," *IEEE Frequency Control Symposium*, May 19–21, 2008, pp. 414–417.

- [139] Asad Jamil, Thottam S. Kalkur, Nicholas Cramer, “Tunable ferroelectric capacitor-based voltage controlled oscillator,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 54 no. 2, Feb 2007, pp. 222–226.
- [140] M. Al-Ahmad, C. Loyez, N. Rolland, P.-A. Rolland, “Wide BST-based tuning of voltage controlled oscillator,” *Proceedings of the Asia-Pacific Microwave Conference 2006*, Dec 12–15, Dec, 2006, pp. 468–471.
- [141] B.P. Lathi, *Signals, Systems, and Controls*, Intext Publishers, 1974, Chapter 5.
- [142] S.C. Gupta, “Transient analysis of a phase-locked loop optimized for a frequency ramp input,” *IEEE Trans. SET-10*, June 1964, pp. 79–83.
- [143] T.F. Haggai, “Phase lock receiver with a constant phase slope,” *U.S. Patent Office no. 3,551,829*, Dec. 29, 1970.
- [144] James A. Crawford, *Advance Phase-Lock Techniques*, Artech House Inc., 2008.
- [145] Alan Victor, Jayesh Nath, Dipankar Ghosh, Brian Boyette, Jon-Paul Maria, Michael Steer, Angus I. Kingon, Gregory Stauf, “A voltage controlled oscillator using Barium Strontium Titanate (BST) thin film varactor,” *IEEE Proceedings 2004 Radio and Wireless Conference*, Sept. 19–22, 2004, pp. 91–94.
- [146] A. Victor, J. Nath, K.G. Gard, J.-P Maria, A.I. Kingon, M.B. Steer, “Tracking phase-lock loop characteristics with a VCO using a barium strontium titanate (BST) thin-film varactor,” *IEEE Radio and Wireless Symposium Rawcon 2007*, Jan 9–11, pp. 289–292.
- [147] T. Christos, “Oscillator load pull measurements using a computer controlled tuner,” *IEEE ARFTG Conference Digest-Spring 35th*, Vol.17, May 1990, pp. 12–18.
- [148] B. Meskoob, S. Prasad, “Loop-gain measurement and feedback oscillator design,” *IEEE Microwave and Guided Wave Letters*, vol. 2, no. 9, September 1992.
- [149] P.M. Cabral, J.C. Pedro, N.B. Carvalho, “Nonlinear device model of microwave power GaN HEMTs for high power-amplifier design”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 11, November 2004, pp. 2585–2592.
- [150] G. Gonzalez, *Microwave Transistor Amplifier Analysis and Design*, 2nd edition, Prentice Hall, Englewood Cliffs, NJ., 1997.
- [151] A. Hati, C.W. Nelson, D.A. Howe, N. Ashby, J. Taylor, K.M. Hudek, C. Hay, D. Seidef, D. Eliyahu, “Vibration sensitivity of microwave components,” *IEEE International Frequency Control Symposium*, May 29–June 1, 2007, pp. 541–546.
- [152] Volker Gungerich, Franz Zinkler, Werner Anzill, Peter Russer, “Noise calculations and experimental results of varactor tunable oscillators with significant reduced phase noise,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, February 1995, pp. 278–285.

- [153] A. Michael Cowley, Robert A. Zettler, "Shot noise in silicon schottky barrier diodes," *IEEE Trans. on electron devices*, Vol. ED-15, October 1968, pp. 761–769.
- [154] Robert A. Zettler, A. Michael Cowley, "p-n Junction–Schottky barrier hybrid diode", *IEEE Trans. on electron devices*, Vol. ED-16, January 1969, pp. 58–63.
- [155] J. Sikula, J. Hlavaka, J. Pavelka, V. Sedlakova, L. Grmela, M. Tacano, S. Hashiguchi, "Low frequency noise of tantalum capacitors," *Active and Passive Electronic Components*, Vol. 25, 2002, pp. 161–167.
- [156] Rajendra P. Agarwal, Andras Ambrozy, Hans L. Hartnagel, "Excess noise in semiconducting BaSrTiO₃," *IEEE Trans. on Electron Devices*, Vol. ED-24, December 1977, pp. 1337–1341.
- [157] A. Ambrozy, "A model for excess noise of semiconducting BaSrTiO₃," *IEEE Trans. on Electron Devices*, Vol. ED-26, September 1979, pp. 1368–1369.
- [158] D. Ghosh, B. J. Laughlin, J. Nath, A. I. Kingon, M. B. Steer, and J.-P. Maria, "Tunable high-quality-factor interdigitated (Ba, Sr)TiO₃ capacitors fabricated on low-cost substrates with copper metallization," *Thin Solid Films*, vol. 496, issue 2, pp. 669–673, Feb 21, 2006.
- [159] M.P.J. Tiggelman, K. Reimann, J. Schmitz, "Reducing AC impedance measurement errors caused by the DC voltage dependence of broadband high-voltage bias-tees," *2007 IEEE International Conference on Microelectronic Test Structures*, March 19–22, pp. 200–205.
- [160] Enrico Rubiola, *Phase Noise and Frequency Stability in Oscillators*. Cambridge, United Kingdom: Cambridge University Press, 2009.
- [161] S. A. Maas, "Third-order intermodulation distortion in cascaded stages," *IEEE Microwave and Guided Wave Letters*, Vol. 5, No. 6, June 1995, pp. 189–191.
- [162] Tri T. Ha, *Solid-State Microwave Amplifier Design*, Wiley-Interscience, 1981, Chapter 6.
- [163] European Telecommunications Standards Institute, "ETSI EN300 197", December 2009. <http://www.etsi.org>
- [164] J.M. Rollet, "Stability and power gain invariants of linear twoports," *IRE Trans. Circuit Theory*, vol. CT-9, no. 3, pp. 29–32, Mar. 1962.
- [165] M.L. Edwards, J.H. Sinsky, "A new criterion for linear 2-port stability using a single geometrically derived parameter," *IEEE Trans. Microw. Theory and Techniques*, vol. 40, no. 12, pp. 2303–2311, Dec. 1992.
- [166] Rizkalla, M.E.; Archer, B.K.; Gundrum, H.C., "Linville power plane stability and bandwidth improvements in a minimum-drift video amplifier," *IEEE Proceedings of the 34th Midwest Symposium on Circuits and Systems*, pp. 863 – 865, May 14–17, vol. 2, 1991.
- [167] Ernest S. Kuh, R.A. Roher, *Theory of Linear Active Networks*, Holden-Day, 1967.

- [168] Robert W. Jackson, "Criteria for the onset of oscillation in microwave circuits," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 3, March 1992, pp. 566–569.
- [169] Robert W. Jackson, "Comments on "Criteria for the onset of oscillation in microwave circuits", " *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, Sept., 1992, pp. 1850–1851.
- [170] R.D. Martinez, R.C. Compton, "A general approach for the S-parameter design of oscillators with 1 and 2-port active devices," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 3, March 1992, pp. 569–574.
- [171] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits," *The Bell System Technical Journal*, July–August 1969, pp.1937–1955.
- [172] K. Kurokawa, "Injection locking of microwave solid-state oscillators ," *The Proceedings of the IEEE*, vol. 61, no. 10, October 1973, pp.1386–1410.
- [173] C.-H. Lee, S. Han, B. Matinpour, J. Laskar, "A low phase noise X-band MMIC GaAs MESFET VCO," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 10, No. 8, August 2000, pp. 325–327.
- [174] D.J. Esdale, M.J. Howes, "A reflection coefficient approach to the design of one-port negative impedance oscillators," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-29, no.8, August 1981, pp.770–776.
- [175] S.J. Mason, "Feedback theory-some properties of signal-flow graphs," *Proc. I.R.E.* 44, 1956, pp. 920.
- [176] M. Monni, G. Martines, "A novel approach to determine the start-up conditions in microwave negative impedance oscillator design," *Proceedings of the 37th European Microwave Conference*, Oct. 2007, pp. 1397–1400.
- [177] R.L. Clark, "Oscillator insights based on circuit Q," *IEEE Proceedings of the 45th Annual Frequency Symposium on Frequency Control*, May 29–31, pp. 352–359.
- [178] E.A. Guillemin, *Communication Networks*, vol. 2., Wiley, 1935.
- [179] G.E. Bodway, "Two port power flow analysis using generalized scattering parameters," *Microwave Journal*, vol.10, no.6., May 1967.
- [180] Nguyen, N.M., R.G. Meyer, "Start-up and frequency stability in high-frequency oscillators," *IEEE Journal of Solid-State Circuits*, vol. JSSC-27, May 92, pp. 810–819.
- [181] Ali Mohamed Darwish, Andrew J. Bayba, H. Alfred Hung, "Accurate determination of thermal resistance of FETs," *IEEE Trans. Microwave Theory and Tech.*, vol. 53, no. 1 , January, 2005, pp. 306–313.

- [182] Mitsubishi Electric Semiconductors High Frequency Devices, “MGFC36V4450 4.4 5.0 GHz BAND 4W INTERNALLY MATCHED GaAs FET”, June 2004. February 2006, <http://www.mitsubishichips.com/Global/common/cfm/eProfile.cfm?FOLDER=/product/hf/gaastransistor/cband/cb>.
- [183] Alan Victor, Jayesh Nath, “An analytic technique for trade-off of noise measure and mismatch loss for low noise amplifier design”, *IEEE WAMICON 2010 Conference*, Melbourne, FL., April 2010, accepted for publication.
- [184] J. Enberg, “Simultaneous input power match and noise optimization using feedback,” *Fourth European Microwave Conference*, Switzerland, Sept, 1974.
- [185] “Si-GaN HFET NPTB00004 device data sheet”, NDS-002, Rev. 3, May 2009, December 2009, http://www.nitronex.com/design_support.html#NPTB00004.
- [186] Micro-Coax Corporation, “UT-141AA Semi-Rigid Coaxial Cable”. December 2009, <http://www.micro-coax.com>.
- [187] Alan Victor, Jayesh Nath, Dipankar Ghosh, Seymen Aygun, Walter Nagy, Jon-Paul Maria, Angus I. Kingon, Michael Steer, “Voltage controlled GaN-on-Si HFET power oscillator using thin-film ferroelectric varactor tuning,” *IEE Proceedings of the 36th European Microwave Conference*, September 2006, pp. 87–90.
- [188] Hongtao Xu, Christopher Sanabria, Sten Heikman, Stacia Keller, Umesh K. Mishra, Robert A. York, “High power GaN oscillator using field-plate HEMT structure,” *IEEE MTT-S International Microwave Symposium Digest*, June 12–17, pp.1345–1348.
- [189] J. van der Tang, D. Kasperkovitz, “Oscillator design efficiency: a new figure of merit for oscillator benchmarking,” *IEEE International Symposium on Circuits and systems 2000*, Vol. 2, May 2000, pp. 533–536.
- [190] Eric W. Bryerton, Wayne A. Shiroma, Zoya B. Popovic, “A 5-GHz high-efficiency class-E oscillator”, *IEEE Microwave and Guided wave Letters*, vol. 6. no. 12, December 1996, pp. 441–443.
- [191] Dongmin Park, SeongHwan Cho, “Design techniques for a low-voltage VCO with wide tuning range and low sensitivity to environmental variations,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, April 2009, pp. 767–774.

APPENDICES

Appendix A

Phase Noise Measurements from Low Frequency Hum and Noise Measure

The treatment and discussion here presents a measurement of oscillator phase noise at a given carrier offset frequency $\Delta\omega_o$. The technique is based on a low frequency baseband measurement. The audio hum and noise level measurement is significantly less complex than the phase lock method and provides a phase noise measurement from a conventional frequency discriminator detector. The dynamic range of the measurement is limited as in the case of the phase lock method, on the noise quality of a single source. In the case of this measurement, the local oscillator used in down converter process associated with the FM detector. However the baseband measurement equipment is easily satisfied with an audio notch filter and audio voltmeter.

The essence of the measurement is that the signal-to-noise ratio in an audio measurement bandwidth of B , offset from baseband-DC by ΔHz , is directly correlated with the residual noise of the unmodulated source under test at the same offset. The reference for the test, i.e. the signal term in the signal-to-noise ratio value, is determined by establishing a base line audio recovery signal when the source under test is modulated with a deviation δf . The source under

test with noise level at an offset is shown in Figure A.1

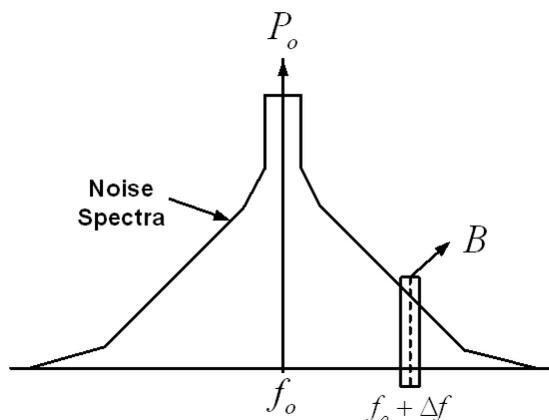


Figure A.1: The carrier signal with signal power P_o and noise at offset Δf is to be characterized at audio frequencies in a bandwidth, B .

The total noise power at the carrier frequency f_o in B consists of AM and PM components. If a FM receiver with a limiting IF channel is used, then the noise power input to a discriminator has components of PM noise only or AM noise which is converted to PM, for example audio modulation of the source is translated to phase modulation through the mechanism of microphonics. Our base band discriminator method will respond therefore to both noise and noise induced hum (hum and noise) and the total noise power will be associated with the quadrature term of the carrier as discussed in section 2.3. Consider first the technique implemented by a phase lock loop operating as a phase discriminator. Using (2.5) with the phase offset $\phi(t)$ set to zero and the signal is noise free, we have

$$x(t) = A_o \sin(\omega_o t) \quad (\text{A.1})$$

and the addition of in-phase and quadrature noise gives the composite signal, $S(t)$ as $S(t) = x(t) + n(t)$ or

$$S(t) = A_o \sin(\omega_o t) + n_x(t) \cos(\omega_o t) + n_y(t) \sin(\omega_o t). \quad (\text{A.2})$$

Collecting terms we have

$$S(t) = [A_o + n_y(t)] \sin \omega_o t + n_x(t) \cos \omega_o t. \quad (\text{A.3})$$

Multiplication of $S(t)$ with a noise free signal, $V_{LO} \sin \omega_o t$, which is placed and held in quadrature by a phase lock loop in relation with $S(t)$ gives

$$[V_{LO} \sin \omega_o t] S(t) = V_{LO} [A_o + n_y(t)] \sin^2 \omega_o t + V_{LO} n_x(t) \sin(\omega_o t) \cos(\omega_o t). \quad (\text{A.4})$$

Expanding A.4, using trigonometric identities and low pass filtering the double frequency terms gives

$$[V_{LO} \sin \omega_o t] S(t) = \frac{V_{LO}}{2} [A_o + n_y(t)] + \frac{V_{LO} n_x(t)}{2}, \quad (\text{A.5})$$

In a phase lock system the in-phase term $n_x(t)$ is suppressed and the ratio of the unlock to locked amplitude of the remaining quadrature term provides the phase noise sideband to carrier ratio or the signal-to-noise ratio as

$$S/N = A_o/n_y(t). \quad (\text{A.6})$$

Consider now replacing the phase lock detector system with the frequency discriminator preceded by a limiting IF amplifier channel. While suppression of the in-phase noise term requires holding the source under test and a reference source in quadrature, by use of a PLL; the discriminator method does away with this by utilizing a high gain limiter in front of a frequency discriminator. Let the discriminator input signal from the IF channel be

$$V_{IF}(t) = A(t) \cos(\omega_o t + \varphi(t)). \quad (\text{A.7})$$

The in-phase and quadrature noise terms give

$$V_{IF}(t) = [V_s + n_x(t)] \cos \omega_o t - n_y(t) \sin \omega_o t \quad (\text{A.8})$$

and where

$$\varphi(t) = \tan^{-1} \left(\frac{n_y(t)}{V_s(t) + n_x(t)} \right) \approx \frac{n_y(t)}{V_s(t)} \text{ for } V_s \gg n_x(t) . \quad (\text{A.9})$$

The discriminator output is equal to the time derivative of the phase, therefore from (A.9),

$$\frac{d\varphi(t)}{dt} = \frac{dn_y(t)}{V_s(t)} . \quad (\text{A.10})$$

However this is directly related to the S/N ratio of the oscillator obtained from the phase lock method shown in (A.6). Therefore if the discriminator output spectrum of (A.8) is found then the phase noise of the oscillator spectrum is also available.

Let $n_y(t)$ now the IF or baseband equivalent of the noise spectra about f_o be composed of a series of single sinusoids at frequencies f_m offset from a carrier single at f_o and having known spectral density, $S_y(f_m)$. Then the noise power of $n_y(t)$ is $S_y(f_m)\Delta f$. Noise power above and below f_o contributes to the total measured and we have $n_y(t)$ expressed in terms of its double sided noise power as

$$n_y(t) = \sum_m \sqrt{2S_y(f_m)\Delta f} \sin(2\pi f_m t + \theta_m) . \quad (\text{A.11})$$

Then from (A.10) we have

$$\frac{d\varphi(t)}{dt} = \frac{2\pi f_m}{V_s} \sum_m \sqrt{2S_y(f_m)\Delta f} \cos(2\pi f_m t + \theta_m) . \quad (\text{A.12})$$

Then the power spectral density of phase noise is written as

$$S_{\dot{\varphi}}(f_m) = \frac{8\pi^2 f_m^2}{V_s^2} S_y(f_m)\Delta f . \quad (\text{A.13})$$

From (2.44), the noise density, $S_y(f_m)$ is obtained from the noise to signal ratio of the oscillator

given as

$$\frac{N}{S} = \frac{f_o^2 kT}{f_m^2 Q_L^2 P_s}. \quad (\text{A.14})$$

Note, additive device noise is not present, noise is introduced only via the finite Q resonator, so $F = 1$ and frequency is used in lieu of radian frequency. Substitution for the noise density portion of (A.14) only, into (A.13), gives

$$S_{\varphi}^{\bullet}(f_m) = \frac{8\pi^2 f_o^2 kT}{V_s^2 Q_L^2}. \quad (\text{A.15})$$

Discriminator signal power, $V_s^2/(2R_L)$, is proportional to the oscillator output power, therefore let $P_{osc} \equiv V_s^2/2$ (R_L arbitrary) in (A.15). Then from (A.15) we have

$$S_{\varphi}^{\bullet}(f_m) = \frac{4\pi^2 f_o^2 kT}{P_s Q_L^2}. \quad (\text{A.16})$$

Next, the noise power output of the discriminator is found. The noise power output is a function of the discriminator audio noise equivalent bandwidth relative to the IF bandwidth, the discriminator gain which is a measure of the conversion of input frequency deviation to output voltage and spectral density of input phase. Therefore we have,

$$N_o = \frac{k_d^2}{B_{IF}} \int_{f_{m1}}^{f_{m2}} S_{\varphi}^{\bullet}(f_m) df_m. \quad (\text{A.17})$$

Upon substitution and setting $\Delta f_m = (f_{m2} - f_{m1})/B_{IF}$ and using (A.16) we have

$$N_o = \frac{k_d^2 4\pi^2 kT f_o^2}{P_s Q_L^2} (\Delta f_m). \quad (\text{A.18})$$

Our reference signal for establishing a signal-to-noise ratio from the discriminator and eventually a measure of the oscillator phase noise is established by introducing modulation to the source under test. With frequency modulation applied to the carrier signal, the modulated IF

signal is

$$\tilde{V}_{IF}(t) = V_s \cos \left(2\pi f_o t + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \right), \quad (\text{A.19})$$

and the discriminator output after differentiating and applying low pass filtering is

$$V_o = k_d \frac{d\varphi}{dt} = k_d \frac{d}{dt} \tilde{V}_{IF}(t) \rightarrow k_d 2\pi \Delta f. \quad (\text{A.20})$$

Therefore the signal output power with modulation is

$$S_o = 2(k_d \pi \Delta f)^2. \quad (\text{A.21})$$

From (A.21), the discriminator gain is found in terms of the signal power out. Substitution into (A.18) and simplifying we have

$$N_o = \frac{2S_o k T f_o^2}{\Delta f^2 P_s Q_L^2} (\Delta f_m). \quad (\text{A.22})$$

Using the oscillator noise to signal ratio from (A.14) we have from (A.22)

$$N_o = \frac{2S_o}{\Delta f^2} \left(\frac{N}{S} \right)_{\text{osc}} \Delta f_m f_m^2. \quad (\text{A.23})$$

Then the discriminator signal-to-noise ratio is found in terms of the oscillator signal-to-noise and the various bandwidths which are all know quantities. Using the previous definition for Δf_m we have,

$$\left(\frac{S_o}{N_o} \right)_{\text{disc}} = \frac{\Delta f^2}{2} \left(\frac{S}{N} \right)_{\text{osc}} \left[\frac{B_{IF}}{f_{m2} - f_{m1}} \right] \frac{1}{f_m^2}. \quad (\text{A.24})$$

Therefore, given the IF and audio bandwidth or the pre-detection and post-detection bandwidths, the set oscillator deviation, and the desired channel offset from the oscillator under test carrier frequency, the signal-to-noise ratio of the discriminator is found. Complimentary

to this of course is the measured discriminator signal-to-noise ratio is known and with all other parameters known, the oscillator signal-to-noise ratio is found. As a specific example consider the following: IF Bandwidth: $B_{IF} = 10$ kHz Audio Bandwidth: $f_{m2} - f_{m1} = 3$ kHz Carrier offset frequency: $f_m = 10$ kHz Deviation: $\Delta f = 5$ kHz. Solving from (A.24) the signal-to-noise ratio of the discriminator is found as

$$\left(\frac{S_o}{N_o}\right)_{\text{disc}} = .15 \left(\frac{S}{N}\right)_{\text{osc}} \rightarrow \left(\frac{S}{N}\right)_{\text{osc.dB}} - 8.3 \text{ dB}. \quad (\text{A.25})$$

Dependent on the desired spot offset frequency from the oscillator carrier and measurement bandwidths, this correction factor will change. It is important to mention in these calculations and in measurements, the conversion oscillator input to any mixer prior to input to the discriminator is assumed noise free.

Appendix B

Excess Noise in Varactors

A diode noise current, shot noise, is associated with current flow across a potential barrier. The mean square shot noise voltage caused by thermally generated minority carriers and diffusion of majority carrier across the barrier add on a mean square basis. This noise current is given by

$$I_{\text{sh}}^2 = 4qI_o\Delta f. \quad (\text{B.1})$$

For the case of a fully forward-biased *pn* junction diode the shot noise of current is given by,

$$I_{\text{sh}} = \sqrt{2qI_d\Delta f}, \quad (\text{B.2})$$

where q is electron charge, I current, and Δf the bandwidth. To obtain the noise equivalent voltage, used for calibration purposes, we find the dynamic resistance of the diode at the operating current. This is a noiseless resistance given by

$$r_d = kT/qI_d. \quad (\text{B.3})$$

The test configuration is shown in Figure B.2. A stepped attenuator is adjusted to prevent overload of the spectrum analyzer particularly at line related frequencies, 60-240 Hz. Measurements must be conducted in a screen cage. A low pass filter may also be used in front of the LNB and a 7 section 1 MHz cutoff L-C filter was constructed to minimize higher frequency signals, particularly FM broadcast signals from overloading the spectrum analyzer. In combination of the spectrum analyzer, lower frequency wave analyzers are used to confine the measurement frequency response below 100 kHz.

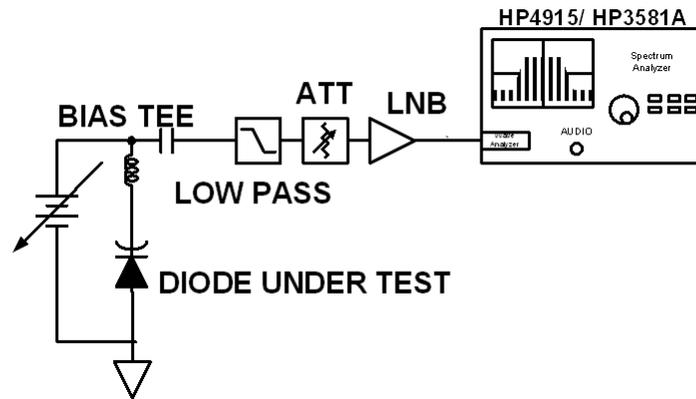


Figure B.2: Diode noise test set.

Appendix C

Mapping Analysis Applied to Oscillator Synthesis

A two port amplifier is characterized accurately when operating in a small signal regime by a set of two port small signal S-parameters. Feedback is intrinsic to the device and stability is dependent on the load and source terminations applied to the device. The device may be active-generative if the appropriate set of passive termination(s) are found. The existence of possible terminations are readily found through a variety of various means, including the Rollet stability factor, k or the μ factor from [164, 165] and the C factor from Linville [166] if Y parameters are used. If these terminations exist the device will display negative resistance[167]. The two port network output and input reflection coefficients are governed by a set of bilateral equations which are a function of the device s parameters and the terminations, Γ_S and Γ_L as given by:

$$S'_{22_{2port}} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (\text{C.1})$$

and

$$S'_{11_{2port}} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (\text{C.2})$$

In general the bilateral relations are extended to an “N” port network and written as,

$$S'_{iN} = S_{iN} + \frac{S_{iN}S_{Ni}\Gamma_N}{1 - S_{NN}\Gamma_N} \xrightarrow{3port} S'_{ij} = S_{ij} + \frac{S_{i3}S_{3i}\Gamma_3}{1 - S_{33}\Gamma_3}. \quad (\text{C.3})$$

Here we highlight the case for $N = 3$ as the generalized active devices considered are active three terminal devices. Given the 2 port parameters it is straightforward to obtain the 3 port parameters, (referred to as the floating 3 port parameters), as the sum of the rows and columns of the 3 port matrix must sum to unity. Therefore, both a 2 port or a 3 port network is capable of the realization of an oscillator. In the case of the 2 port, from inspection of C.1 or C.2, as $S_{11}\Gamma_L$ or $S_{22}\Gamma_S$ approaches unity, the input reflection coefficients will exceed unity. This requires the product of $S_{12}S_{21}$ to be non zero. In the case of the two-port a map is created which provides all possible values of S_{ii} or S_{jj} as a function of all real values of Γ_L or Γ_S . Thus, for example, a map of the input reflection coefficient is created for all Γ_L which lie on the unit circle Smith chart $1\angle -180^\circ \leq \Gamma_L \leq 1\angle 180^\circ$. A reflection for such a map for several devices is shown in Figure C.1. The extended Smith chart includes the unit circle and magnitude reflection extending to 4. In this display three contours for three different sets of s parameters are shown. In case (a) the $|k|$ is .22 while in (b) and (c) 0.56 and 1.1 respectfully. Although the difference in k for (a) and (b) is small the magnitude and angular range of load reflection coefficients permitting an input reflection coefficient greater than unity and the resulting input reflection coefficients is significant. The two port s parameters are identical in case (a) and (b) except for the magnitude of S_{22} in case (b). The case (c) map is clearly representative of an unconditionally stable 2 port as no combination of load or source reflection coefficient creates an input reflection coefficient greater than unity. For case (b) the range of load reflection coefficient is inductive $+52.5^\circ$ to $+102.5^\circ$, while in case (a) $+45^\circ$ to $+125^\circ$ is required. Most important are the required terminations to satisfy the condition of oscillation, which is discussed in detail in 4.4.2. We have, in the case of (a) a capacitive termination required, while in the case of (b) we have predominantly an inductive termination. As a conjugate termination is required by the resonator, whose imaginary component must match that of the resonator reactance, we see

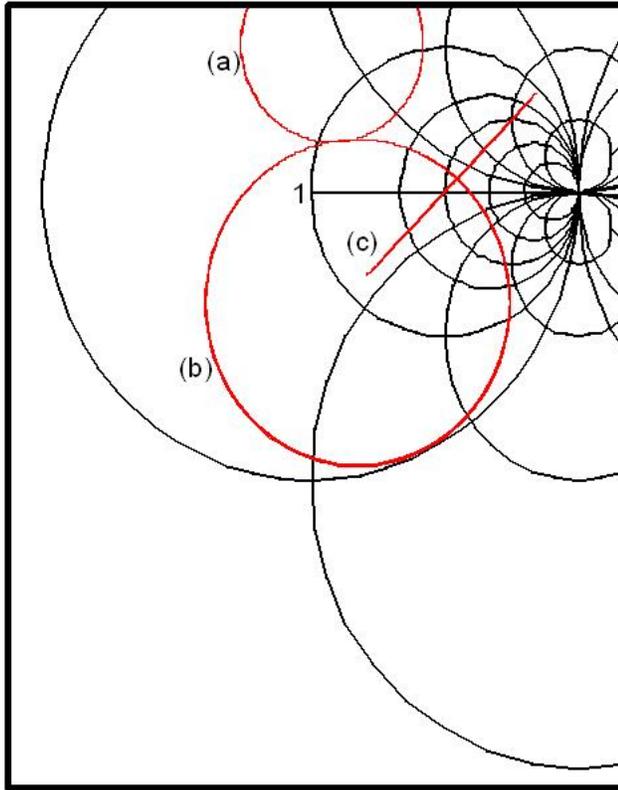


Figure C.1: Input reflection coefficient for a set of devices with all possible real terminations confined to the unit circle on the Smith Chart. In case (a) $k=.22$, (b) $k=.56$ and (c) $k > 1$.

that a varactor termination could be used directly with case (a). However, a series resonator consisting of a series $L - C_V$ could be used for case (b), whereby the inductive reactance is modified by the varactor reactance. In this case the varactor “tunes” the required series inductive reactance component to the appropriate value by modifying the series reactance and it is the shift in the magnitude of the reactance change that contributes to the tuning sensitivity of the resonator. Both cases (a) and (b) will provide a unique single frequency of oscillation provided that the terminations are properly chosen and the terminations associated with the active device resonator interface do not satisfy conditions for oscillation at other frequencies as well. This is key and leads us to further investigate the conditions for a single frequency of oscillation. As well, the conditions for stable tuning with no discontinuities, jumps, or abrupt

changes in tuning slope warrant investigation.

If the device is potentially unstable, $k < 1$ or either of the port parameters, S_{11} or S_{22} are greater than unity, then oscillation is assured without the addition of external feedback. If the device is unconditionally stable then the need for adding additional feedback is required. Either series or shunt or a combination are added to the active network and an appropriate imbedding network is found which can maximize any number of different parameters, for example maximum output power, tuning bandwidth, or phase noise. To meet the condition of oscillation, we introduced the need to generate sufficient loop gain, through the ability to provide a negative resistance. Such a network is classified active generative and therefore able to support the regeneration of an incident wave from a resonator after loss. As long as the round trip, between resonator and active device, are supported with appropriate gain after any losses and the correct phase shift, instability will exist and oscillation will occur. Furthermore, it is not sufficient to obtain a reflection coefficient greater than unity. Although this condition is necessary as this supports a negative resistance, the other half circuit, resonator, must have sufficiently large unloaded Q so that the net total circuit R is negative. In the case of the series type oscillator this is easy to see as the individual values of resistance as added. In the parallel type oscillator, total conductance of the network must be less than zero.

Two concepts which tie the treatment of a one port oscillator analyzed via incident and reflected waves between active device and passive resonator and the analysis of an oscillator from a two port feedback perspective are actually one in the same. If the transfer function of a general feedback system is inspected and compared to a generic wave driven microwave system we see they are quite similar [168, 169]. Consider a feedback system as a two-port with input and output signal voltages, V_i and V_o and feed-forward and feedback blocks $A(s)$ and $B(s)$. Normally these blocks have an open loop forward gain $G(s)$ and a passive feedback function $H(s)$. The $G(s)$ block is characterized by the insertion gain in a matched system, an amplifier

and the feedback block $H(s)$ insertion loss for a resonator filter. The transfer function given by

$$V_o = \frac{G(j\omega) V_i}{[1 + (G(j\omega) H(j\omega))]} \quad (\text{C.4})$$

is characterized as a control system with negative feedback. If the system were constructed with positive feedback then the denominator term is simply $GH - 1$ in lieu of $GH + 1$, all a function of the complex variable $j\omega$. This distinction is made only to reinforce the subtle difference between a system which we desire to be stable and wish to investigate what is required to force the system to be unstable, and one in which an unstable system is deliberate and desired. The Nyquist test is applied to a stable open loop, GH , and the closed loop system defined by (C.4) unstable if encirclement of the -1 point at least once by the polar plot $GH(j\omega)$ for $-\infty < \omega < \infty$. Since the system is one in which negative feedback is desired, the open loop phase shift is constrained to 180° and any additional phase shift simply reduces the phase margin. Hence encirclement of the -1 point implies an additional 180° of phase shift and positive feedback occurs. Correspondingly, we can investigate the encirclement of the open loop gain for a positive feedback system. In this case encirclement of the +1 point enforces positive feedback for a specific GH product at a radian frequency ω . Either system when completely specified, that is the complete GH product, will display right hand plane poles if encirclement of the -1 or +1 point occurs for the representative system and hence instability exists. In the case of a wave driven microwave system, feedback is also present, although it is described in terms of incident and reflected wave voltages, in lieu of feed forward and feedback signal voltages. Consider the equivalent representations shown in Figure C.2. The device and resonator reflection coefficients are expressed in terms of the incident and reflected wave signal voltages, a_S, b_S, a_L, b_L respectfully and the device and resonator reflection coefficients, Γ_d and Γ_r . Although no datum node or ground is needed to describe the oscillator connectivity, if it were and the branch b_S and a_L were grounded, the configuration would be representative of a one-port reflection oscillator. The noise or a transient voltage which starts the oscillator is modeled with an ideal series coupler with V_i added to the device input along with the

reflected voltage from the resonator, b_L . Therefore $b_S = \Gamma_d(b_L + V_i)$. With $b_L = \Gamma_r a_L$ we have $b_S = \Gamma_d \Gamma_r a_L + \Gamma_d V_i$. However a_L , the incident voltage to the resonator is just the reflected voltage from the device, b_S . Hence, $a_L = \Gamma_d \Gamma_r a_L + \Gamma_d V_i$. Collecting terms and simplifying,

$$a_L = \frac{\Gamma_d}{1 - \Gamma_d \Gamma_r} V_i . \quad (\text{C.5})$$

Compare this result with the two-port positive feedback configuration and take the output signal a_L directly from the device. As $a_L = b_S$ will identify this signal voltage as the output V_o . Then compare this to the positive feedback two port arrangement if we move the output point after the device gain block, $G(j\omega)$; note the similarity.

$$V_o = \frac{\Gamma_d}{1 - \Gamma_d \Gamma_r} V_i \text{ and } V_o = \frac{G(j\omega)}{1 - G(j\omega)H(j\omega)} V_i . \quad (\text{C.6})$$

The similar form obtained from the one port wave analysis for the negative resistance (conductance) microwave driven system and the two port positive feedback topology enforces the application of a single technique for analysis for both. In this case, determining the conditions for instability and self-sustained oscillation. Although the Nyquist technique provides a criteria for gauging oscillation it does not provide the frequency of oscillation. The critical information missing is the phase relationship for the signals between the active device and the passive resonator. Several approaches outlined in [168, 170] use either graphical evaluation of the trajectory angles of the device and resonator reflection coefficient or circular functions which describe the manner in which signals circulate through a network with the network modeled using signal flow graphs. The goal is to unify the design phase for both the generic one port and two port oscillator topologies. Prior to fast integrated linear and nonlinear analysis these techniques were very useful. In this work the desire is to take these steps further by coupling harmonic balance simulation with mapping as we desire to vary the oscillator terminations or imbedding network. The advantage of such an approach is the ability to use available small signal S-parameters to validate the ability to meet the oscillation criteria and then apply large

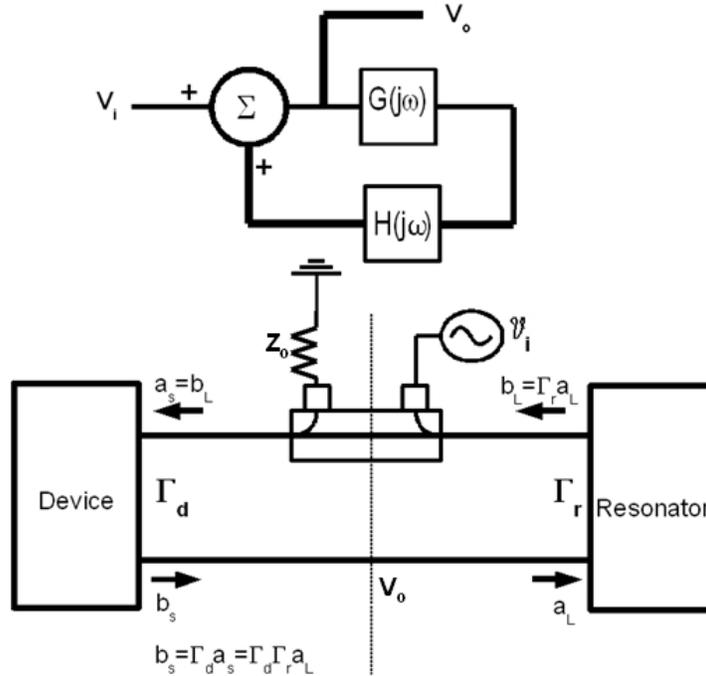


Figure C.2: A Control system positive feedback loop and wave equivalent representative for a negative resistance one port. The transfer functions are identical in form.

signal analysis to monitor the trajectory of the input or output reflection coefficient with signal level and variations in imbedding. A variation of the Nyquist technique is to use the Bode criteria to establish the open loop gain and phase. Then, either open the feedback path of the 2 port oscillator or as in [170], split a node in a negative resistance one port oscillator between the negative generator and the resonator.

To convey this technique and results, shown in Figure C.3 and Figure C.4, are the limiting characteristics based first on small signal S-parameters and then large signal with imbedding variation. To display the complex reflection coefficient a compressed Smith chart is used and the inverse S_{ii} plotted.

Small signal S-parameters provide operating frequency by finding the angular intersection of the device reflection coefficient with the resonator trajectory vs. frequency. In this case a series type oscillator as the large signal limiting characteristics move along a family of constant

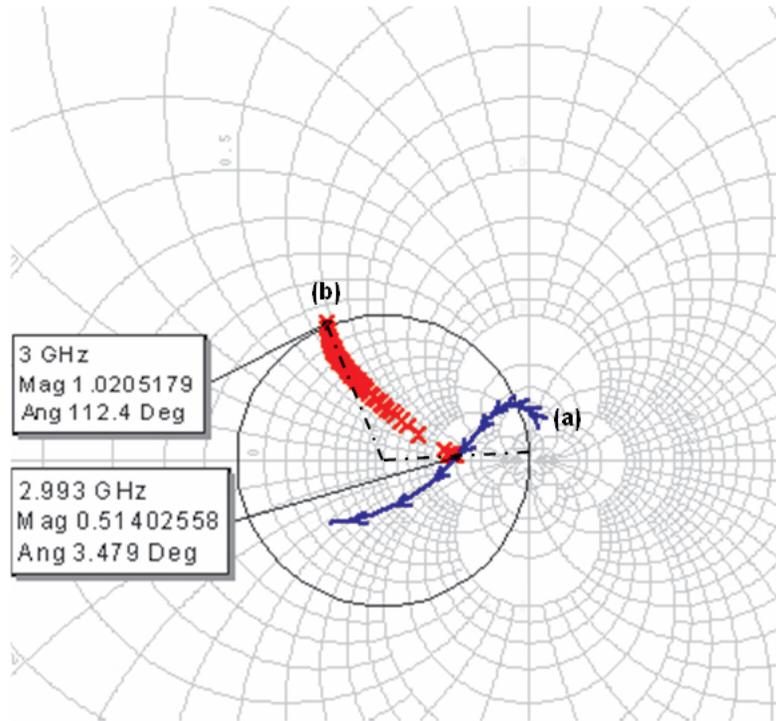


Figure C.3: The small signal Γ_{in} prior to self-limiting (a) and the limiting case (b). The small signal $\Gamma_{in} \gg 1$. For this case the variation in frequency from start-up to final steady state oscillation is significantly different as the phase shift is over 100° .

resistance contours. Therefore a series resonator with clockwise sweep through the short circuit side of the chart is appropriate. If we compare the angular movement of Figure C.3 with that of Figure C.4 we see that the larger Γ forces a significantly larger sweep angle (110°) vs. (10°) as limiting occurs. Therefore the start-up frequency and the final operating frequency would be significantly different between the two cases. $\Gamma_d^{in}(A, \omega)$ There are a number of key aspects to manipulating the shape of the Γ irrespective of either Γ_{in} or Γ_{out} . Reference to Γ_{in} or Γ_{out} is the reciprocal of S_{ii} and so by plotting $1/S_{ii}$ we confine the device, Γ_d , within the unit circle of the Smith chart. Therefore, we are able to monitor the progress of the magnitude and angle of the device dynamic input impedance relative to the resonator, see Figure C.5. This is particularly useful as the trajectory of $1/S_{ii}$ is modified as self-limiting occurs and the dynamic input resistance or conductance reduces or increases respectfully. The path of Γ_d as a function

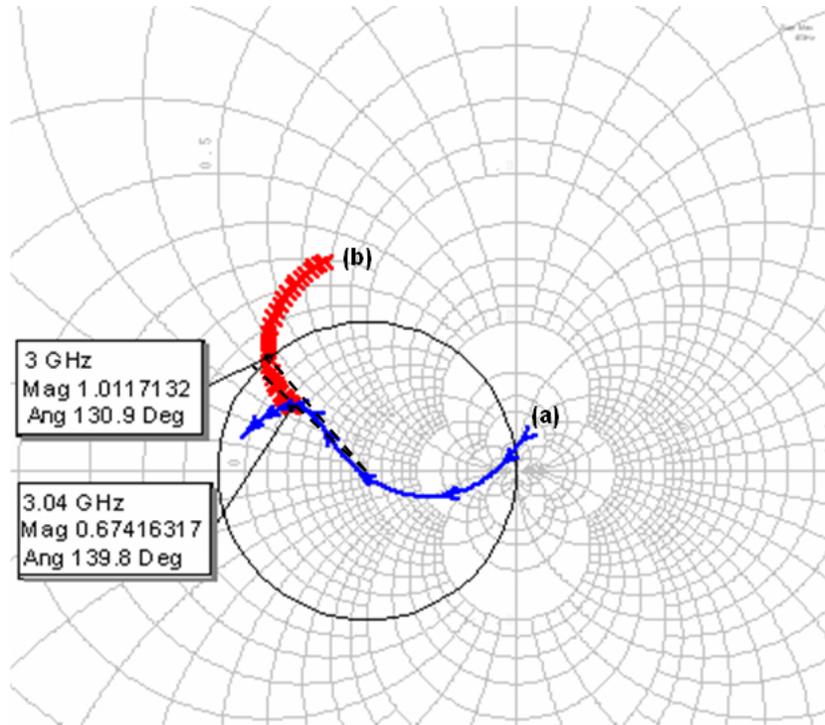


Figure C.4: The small signal Γ_{in} prior to self-limiting (a) and the limiting case (b). The small signal $\Gamma_{in} \geq 1$. For this case the variation in frequency from start-up to final steady state oscillation is small as the the phase shift is less than 10° .

of input signal level and frequency relative to the path of the resonator, Γ_r , with respect to frequency influences oscillator phase noise, tune range, and tunability [171, 172]. An example of mapping which includes the amplitude and frequency dependence along with resonator response is shown in Figure C.5. An important distinction made here is the contour of the vector associated with device limiting. The vector which is formed is along constant frequency points as Γ_d is a function of radian frequency ω and amplitude A . These constant frequency points form a contour as device self limiting occurs and input signal amplitude, V_i increases. The result is the outward movement of the locus of reciprocal device input impedance points, represented by $\Gamma_d(A, \omega)$. This figure is in contrast to [173] which displays Γ_d as the device frequency locus alone without displaying the function of amplitude level. The intersection at each frequency point associated with Γ_d should be distinct and unique with a corresponding point on the

Kurokawa oscillator condition, [171] establishes that for stable oscillation at the operating point of a negative conductance oscillator that

$$\frac{\partial G_d}{\partial V_r} \frac{\partial B}{\partial \omega_r} - \frac{\partial B_d}{\partial V_r} \frac{\partial G}{\partial \omega_r} > 0 . \quad (\text{C.7})$$

where the subscript r refers to the operating point. In the standard approach to oscillator design the device susceptance is assumed to be independent of signal amplitude, i.e. $\partial B_d / \partial V_r = 0$, and the loaded resonator conductance to be independent of frequency, i.e. $\partial G / \partial \omega_r = 0$, so that the stability condition becomes the much simpler

$$\frac{\partial G_d}{\partial V_r} \frac{\partial B}{\partial \omega_r} > 0 . \quad (\text{C.8})$$

The focus of this section was managing the third term of C.7, $(\partial B_d / \partial V_r)$, while the fourth term, $(\partial G / \partial \omega_r)$ is addressed by proper design of the resonator.

Appendix D

DC-RF Load-Conversion Efficiency in FET Oscillators

Oscillators using the FET can achieve self limiting by clamping the gate voltage to nearly zero volts and permitting a peak drain current limited to I_{DSS} . As opposed to a reduction in α in the prior case, the FET will be characterized by a reduction in g_m . An identical treatment could be applied to the bipolar case but the α model is convenient. The FET nonlinear characteristic is described by a peak clamped sine wave driven input to a half-square-law amplifier. Where as the bipolar is characterized by the exponential dependence per (4.48), the FET is characterized by a square law dependence,

$$I_D = I_{DSS} \left(1 - \frac{V_{gs}}{V_P}\right)^2 \quad V_P < V_{gs} < 0. \quad (\text{D.1})$$

In this case the gate-source voltage is subject to a quiescent DC potential with an input signal, $V_1 \cos(\omega t)$, $V_{gs} = V_{GSQ} + V_1 \cos(\omega t)$. Substitution of this function into (D.1) and expanding gives rise to at least three terms, DC, fundamental, and second harmonic. Additional terms will occur and are dependent on the signal input voltage V_1 in relation to the pinch off voltage, V_P . Operation within the square law region of the FET will confine the drain current expression

to the first three terms. Deviation from square law occurs as the magnitude of the peak input voltage, V_1 , exceeds V_P . Provided operation of the FET in the saturation region is maintained and $V_{DG} > -V_P$, for all V_1 , high efficiency is achieved. However, not unlike the bipolar, the supply voltage need not be any greater than required and cutoff or saturation must be avoided as efficiency quickly drops as peak amplitude is limited [19]. As $\left| \frac{V_1}{V_P} \right| \gg 0.5$, the load efficiency will increase for the appropriate supply voltage and load impedance. Operation outside the square law region give rise to additional coefficients which are written in a Fourier series given by $I_n(\phi)$ for $n = 0$ to ∞ as a function of the half-conduction angle ϕ and tabulated for the first $n = 3$ terms [18]. Both the fundamental and DC term where the DC term utilizes a portion of the second harmonic value, assist in calculation of the DC operating point, and the fundamental load efficiency. This Fourier series is applicable to the class of self limiting FET oscillators which provide the limit function by clamping the gate-source voltage to zero. This is a preferred technique for higher efficiency as no expenditure is made for a drain quiescent current in the oscillator off-state.

A particular attractive FET configuration is a connection where the source is common and the auto transformer function is achieved by the ratio of a set of capacitive reactance elements. The load is across the resonator as in the prior bipolar analysis and is coupled to the resonator through an auto transformer. We distinguish this topology form from the case where the load is across a device terminal or a single reactance, for example one of the feedback elements and not part of the resonator network. The configuration and circuit model is shown in Figure D.1 and ??.

The admittance branches given by Y_{ij} provide input, output and feedback elements of

$$Y_{11} = g_{11} + j\omega C_g \quad Y_{22} = g_{22} + j\omega C_d \quad Y_{21} = G_L + 1/j\omega L_d. \quad (\text{D.2})$$

A set of nodal equations at the gate and drain and eliminating the drain term gives,

$$Y_{22} + Y_{11} + (Y_{11}Y_{22})/Y_L = -\overline{g_m}. \quad (\text{D.3})$$

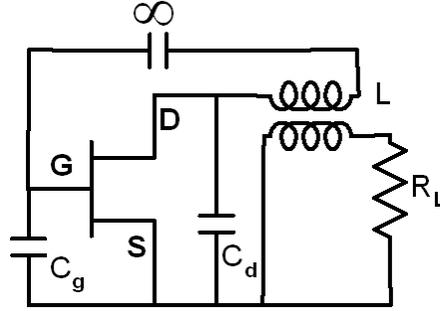


Figure D.1: FET oscillator circuit, feedback factor set by C_g and C_d with operating frequency set with L as part of a load transforming network.

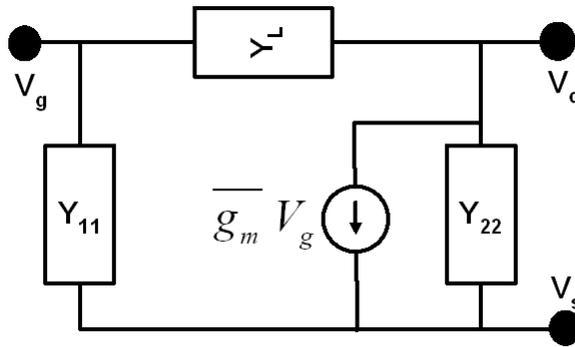


Figure D.2: The circuit simplified with the use of a Y-parameter model. The value of g_m will start at g_m^0 and migrate to a large signal value, $\overline{g_m}$.

The term $-\overline{g_m}$ is a modified small signal g_m , where g_m is given by $g_m = \frac{2I_{DSS}}{-V_p}$ and $-\overline{g_m}$ is the limited g_m . The reduced g_m accounts for the reduction in small signal transconductance and is based on describing the operation of a clamp-biased FET. The effective large signal transconductance is given by

$$\overline{g_m} = \frac{I_{DSS} I_1}{I_p V_1} \rightarrow I_1 / V_1 \text{ as } I_p \rightarrow I_{DSS}, \quad (\text{D.4})$$

where I_1 is the fundamental current, V_1 is the peak value of the fundamental input voltage and I_{DSS} is the short circuit drain-source current with the gate voltage set to zero. The transconductance of the FET under large signal conditions implies that the gate-source voltage

is the sum total of the quiescent DC gate voltage and the sinusoidal input voltage V_1 ; the total which can exceed the pinch off voltage. The peak current is related to the peak gate voltage and the pinch off voltage as $I_p = (V_g - V_p)I_{DSS}^2/V_p^2$.

Finding the real and imaginary part of (D.3) gives the approximate conditions for the start of oscillation and the operating frequency. Upon substitution of the terms from (D.2) we have

$$-\overline{g_m} = g_{11} + j\omega C_g + g_{22} + j\omega C_d + \frac{(g_{11} + j\omega C_g)(g_{22} + j\omega C_d)}{G_L + 1/j\omega L_d}. \quad (\text{D.5})$$

Assuming G_L and the product of $g_{11}g_{22}$ are small, the real and imaginary parts of (D.5) give

$$-\overline{g_m} \approx g_{11} + g_{22} - \omega^2 L (C_g g_{22} + C_d g_{11}) + \omega^4 C_g C_d L^2 G_L \quad (\text{D.6})$$

and the frequency of oscillation

$$\omega_o^2 \approx \frac{C_g + C_d}{C_g C_d L}. \quad (\text{D.7})$$

To satisfy the condition of oscillation at $\omega = \omega_o$ we have from (D.6),

$$\overline{g_m} = a g_{22} + \frac{g_{11}}{a} + \frac{G_L(a+1)^2}{a} \quad (\text{D.8})$$

where a is C_g/C_d and is related to the feedback factor as $N = 1/(1+a)$ with $0 \leq N \leq 1$ and $0 \leq a \leq \infty$. If G_L is small then there is an a factor found which minimizes the required starting g_m to achieve a final $\overline{g_m}$ and is

$$\frac{\partial \overline{g_m}}{\partial a} = g_{22} - g_{11}/a^2 = 0 \quad (\text{D.9})$$

and an optimum a is given by the ratio of the input and output device conductances as

$$a = \sqrt{\frac{g_{11}}{g_{22}}}. \quad (\text{D.10})$$

For the case studied here, where the common terminal is the source, g_{11} and g_{22} are small

relative to G_L and approximately the same. Then for $a = 1$ and from (D.8) we have

$$a_{opt} = 1 \text{ and } \overline{g_m} = 4G_L. \quad (\text{D.11})$$

For this case, $G_L = \overline{g_m}/4$ represents the maximum load conductance permissible. Larger values of load conductance may not allow the oscillator to start. For the efficiency study, consider $\overline{g_m}$ to take the starting value of $g_m = g_m^0$ which is the small signal g_m prior to the FET device self limiting.

In stabilizing the FET oscillator via a clamp gate bias method, will consider assigning the feedback voltage normalized to the pinch off (V_p) voltage. Then as in the bipolar oscillator efficiency study, $x = k(V_g/V_p)$ in contrast to $k(V_{DC}/\gamma)$ for the bipolar case. Here V_g is the peak value of the gate feedback voltage and in both cases the constant k a function of the feedback factor. The resonator power for optimum P_o given for $a = 1$ by

$$2(xV_p)^2G_L. \quad (\text{D.12})$$

Substitution for G_L from (D.11) into (D.12) gives

$$P_o = (g_m(V_p x)^2)/2. \quad (\text{D.13})$$

The fundamental operating g_m is related to the zero bias ($V_g = 0$) g_m , g_m^0 ; and the duration the device is operating (the conduction angle) by expanding the fundamental and average current into a Fourier series [18]. The fundamental current I_1 and DC I_o are expressed as a Fourier series for a square law device with sine wave tips as

$$I_1 = \frac{2I_p \left[\frac{3}{4} \sin(\phi) + \frac{1}{12} \sin(3\phi) - \phi \cos(\phi) \right]}{\pi(1 - \cos(\phi))^2} \quad (\text{D.14})$$

and the average current is

$$I_0 = \frac{I_p [\phi - \frac{3}{4} \sin(2\phi) + \frac{\phi}{2} \cos(2\phi)]}{\pi(1 - \cos(\phi))^2}, \quad (\text{D.15})$$

where $\phi = \cos^{-1}(V_p/V_g)$. As the half conduction angle, ϕ , approaches zero the ratio of the harmonic currents to the DC approaches two, a property of a narrow pulse train. The fact that sinusoidal analysis is permitted at all is predicated on the reasonable assumption that the resonator Q is large enough to restore a sinusoidal voltage from harmonic current. Now, for small ϕ , $I_1 \approx 2I_0$ and for $a = 1$, $V_g = V_o/2$. Then the fundamental operating transconductance is given by $g_m = I_1/xV_p$. Also, if $V_g \gg V_P$ then $I_p \sim I_{DSS}$. Then we can re write (D.14) and (D.15) in an abbreviated form as

$$I_1 \sim I_{DSS}k_1(\phi) \quad (\text{D.16})$$

and

$$I_0 \sim I_{DSS}k_0(\phi). \quad (\text{D.17})$$

Upon substitution for the fundamental g_m we have

$$g_m = \frac{2I_{DSS}k_1(\phi)}{2xV_p} = g_m^0 \frac{k_1(\phi)}{2x} \quad (\text{D.18})$$

where g_m^0 is g_m at I_{DSS} . Using (D.13) and simplifying we have

$$P_o = (V_p x I_{DSS} k_1(\phi))/2. \quad (\text{D.19})$$

Now P_{DC} is expressed in terms of the average current and the conducting angle ϕ as $P_{DC} = I_0(\phi)V_{DD} = I_{DSS}k_0(\phi)V_{DD}$ and the load efficiency is therefore given by

$$\eta = \frac{V_p x k_1(\phi)}{2k_0(\phi)V_{DD}}. \quad (\text{D.20})$$

However, $V_{p,x} = V_g$ and $V_o = 2V_g$ for $a = 1$, therefore,

$$\eta = \frac{V_o}{2} \left(\frac{k_1(\phi)}{2k_0(\phi)V_{DD}} \right) \rightarrow \frac{V_o}{2V_{DD}}. \quad (\text{D.21})$$

Main point, as the resonator voltage is permitted to approach twice the supply voltage, the conversion efficiency will approach 100%. In general for the conditions stated, selection of an optimum feedback factor, $a = 1$ and $N = 1/2$, small G_L , permitting a clamp gate bias topology which gives way to a narrow conduction angle, we have,

$$\eta_o = \left(\frac{k_1(\phi)}{2k_0(\phi)} \right). \quad (\text{D.22})$$

Shown in Figure D.3 the ideal conversion efficiency, no circuit losses or finite resonator Q and extraction of power to a secondary load are included. Although the efficiency does improve with narrow conduction angle, the fundamental output power decreases. So the goal re stated should read, meet the required output power while maximizing the load efficiency. This will require selection of the feedback factor and the selection of the real load impedance as outlined in this procedure.

However the possible efficiency that is appreciated for a mild conduction angle, $\sim 120^\circ$, is significant. Achieving efficiency provided in Figure D.3 requires that the selected real load impedance and the chosen FET drain voltage (V_{DD}) are such that the device operates in the saturation region, i.e. $V_{ds} - V_{gs} > -V_P$ over the complete oscillation time span. The conversion efficiency must add the finite unloaded Q of the resonator in addition to the power contributed to the load. To the extent that the total loaded Q is high enough to support sinusoidal voltage from sine-tipped current, the Figure D.3 is applicable.

As an example, consider a MESFET oscillator whose topology is similar to Figure D.1, [20]. An extensive analysis for this configuration is presented for efficiency. We find that a treatment and approach based on the gate clamp bias configuration and utilizing the first three terms of the Fourier series provides similar results to reported measurements. The configuration studied

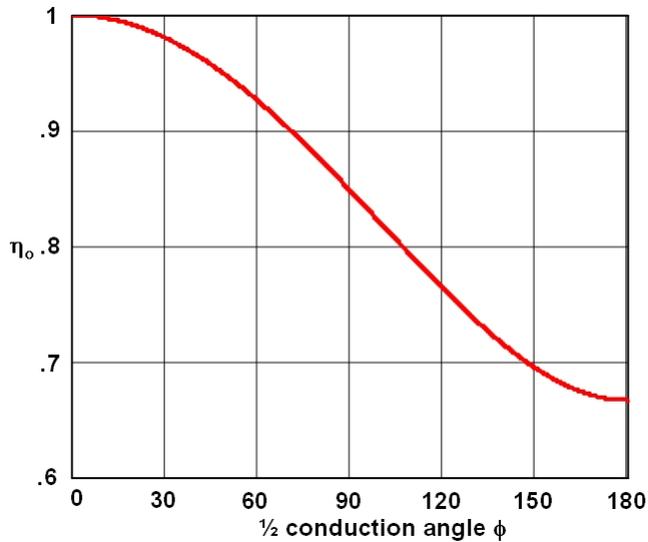


Figure D.3: Efficiency expressed as a ratio of the Fourier component of the fundamental drain current to the average dc value.

is shown in Figure D.4. While it is not necessary to show specific datum node or ground, an oscillator has no input or output, it facilitates recognition of the feed forward and feedback path as well as the resonator elements. An open loop arrangement is shown in D.5 where the network is re drawn placing the datum node at the source. No bias network is shown for simplicity and all reactance values that are either in series or shunt with bias networks are replaced by their single element equivalents at RF. Although C_f is selected to provide the negative resistance via series feedback and control output power; the gate and drain capacitors, C_g and C_d also contribute to the drain output voltage and load efficiency. In our analysis, we have C_g and C_d setting the feedback factor and use the Fourier components of the fundamental and DC to find the gate, drain, and output voltage. The external load is R_L . The elements L_R and C_f set operating frequency and reflected load impedance is controlled by L_M and C_M and will also contribute to setting the operating frequency but to a much lesser degree than L_R and C_f . This is not clear until the open loop gain network is re drawn in Figure D.5. Although the feedback network is low pass in topology, the response is bandpass by virtue of the order of the network and frequency response peaking is present. The peaking controlled by the reflected impedance

transformation of the gate and drain impedances accomplished by C_g and C_d . Therefore, an approximate resonant frequency is found as

$$\omega_o \approx \sqrt{\frac{1}{[(C_g + C_f) // C_d] L_R}}. \quad (\text{D.23})$$

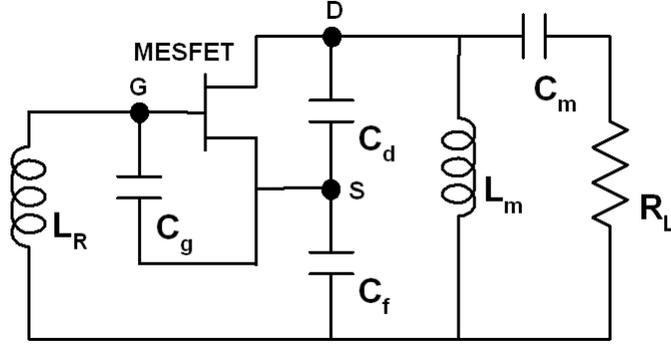


Figure D.4: MESFET oscillator circuit, feedback factor set by C_g and C_d with C_f and operating frequency set with L_R and L_M as part of a load transforming network.

For the designated device, V_P is -1.25 V and I_{DSS} is 45 mA. From the open loop gain network the requirement for loop gain greater than 1 implies that $\overline{g_m} R_T (C_g + C_d) / (C_g) \geq 1$. Here R_T is the total load impedance which includes the transformed output load, the resonator unloaded Q , and the device reflected input impedance to the output. The total load impedance is approximated from the parallel combination of the matching network transformation impedance, given by $(Q_T^2 + 1) R_L$, where $Q_T = X_{C_m} / R_L$ (~ 191 ohms) given at 950 MHz (the operating frequency) and the reflected input impedance from $1/g_m [(C_g + C_d) / C_g]^2$. The value of R_T is 91 ohms. Then from the open loop requirement we have,

$$\overline{g_m} \geq \frac{C_g}{C_g + C_d} \frac{1/R_T}{g_{mo}}. \quad (\text{D.24})$$

The fundamental g_m is a function of the fundamental current I_1 and the fundamental gate input

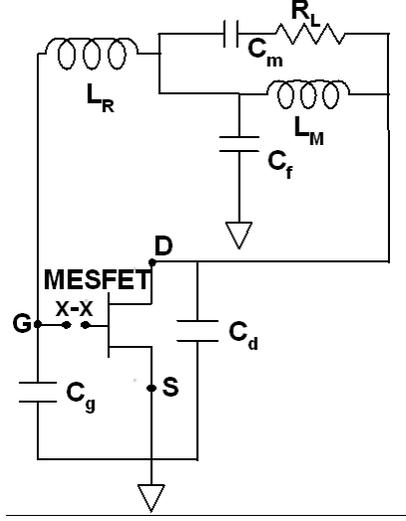


Figure D.5: The circuit re drawn with the datum node selected at the source

voltage, V_1 , i.e. $\bar{g}_m = I_1/V_1$. However $I_1 = I_{DSS}I_1/I_p$ if $I_p = I_{DSS}$. Therefore the fundamental g_m is conveniently re written as,

$$\bar{g}_m = \frac{I_1}{V_1} = \frac{I_{DSS} \left(\frac{I_1}{I_p} \right) (2)}{-V_p \left(\frac{-V_1}{-V_p} \right) (2)}. \quad (\text{D.25})$$

The motivation, in this form we form the ratio between the fundamental large signal g_m and the zero gate-bias g_m . Therefore, recognizing the small signal g_m as $g_m^0 = 2I_{DSS}/-V_P$ we have,

$$\bar{g}_m = g_m^0 \frac{\left(\frac{I_1}{I_p} \right)}{2 \left(\frac{-V_1}{-V_p} \right)}. \quad (\text{D.26})$$

A plot of normalized transconductance as function of peak gate voltage relative to the pinch off voltage is shown in Figure D.6. The plot emphasizes the high efficiency region and therefore the $V_1/-V_P$ begins for normalized values above 0.5-V, beyond the square law region. For a given set of parameters, V_P, I_{DSS}, R_L and feedback factor a , the ratio of \bar{g}_m/g_m^0 is found. Subsequently, so is V_1 and the resonator voltage as $V_o = NV_1$.

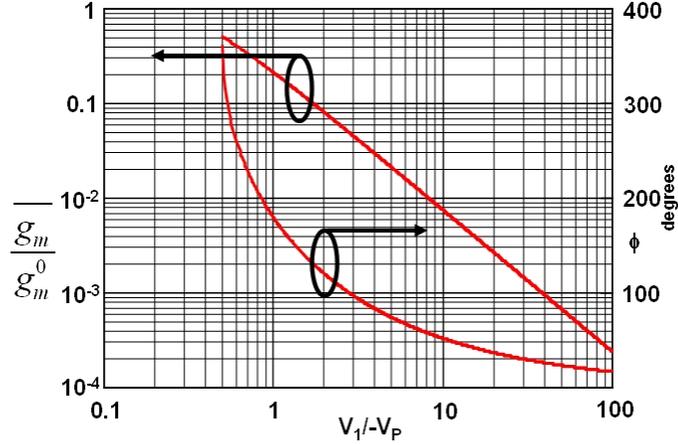


Figure D.6: Normalized fundamental g_m and conduction angle in degrees ϕ , vs. V_1/V_P

The peak output load voltage is then found appropriately scaled for the load impedance vs. the drain termination impedance. For Figure D.4, the parametric table is provided in Table D.1.

Therefore, the calculated output power is 16.7 dBm and is in good agreement with the results reported at 950 MHz in [20].

The DC value of device current has contributions from the average value of the Fourier series of the drain current and the second harmonic term. These terms are obtained from the calculated conduction angle, approximately 134° , given by

$$I_{DC} = \left(\frac{I_2(\phi)}{2} + I_0(\phi) \right) I_p. \quad (\text{D.27})$$

For the case investigated here, with I_p of 45-mA, $I_0 = .338$ and $I_2 = .167$, we have $I_{DC} = 18.97 - \text{mA}$ and is in good agreement with the reported 18-mA in [20]. The calculated load efficiency with a $V_{DS} = 5 - V$ is 49.3%.

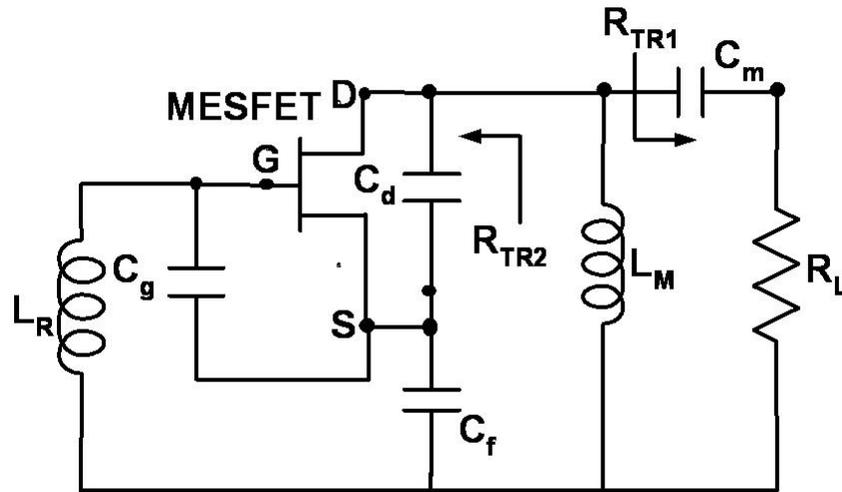


Figure D.7: The FET circuit emphasizing the two sided impedance transform, R_{TR1} and R_{TR2} , and components from Table D.1.

Table D.1: FET circuit parameters

FET circuit elements and calculations		
Parameter	value	calculated
V_P	1.25-V	—
I_{DSS}	45-mA	—
C_g	6 pF	—
C_d	1.5 pF	—
C_f	15 pF	—
L_m	8.2 nH	—
C_m	2 pF	—
R_L	50 ohm	—
g_m^0	—	$57.6 \cdot 10^{-3}$
$-V_1/V_P$	—	1.65
N	—	19/13
a	—	0.68
V_g	—	2.063-V peak
V_d	—	3.014-V peak
V_o	—	2.153-V peak
R_T	—	91 ohm

Appendix E

Spurious Free Dynamic Range

In a linear system one representation for the relation of the output and input power is via a slope intercept plot. The power gain for the fundamental signal shows a slope of unity, a dB for dB change is expected with an offset associated with the power gain, G . Small deviations from linearity occur while operating in a small signal regime. Harmonic signals present in relation to the fundamental are observed with a slope intercept greater than the fundamental. In the case of the presence of two tones at the input of an active device, linear multiplication will give rise to a third tone. This third tone can be forced identical to f_o as $f_o = 2f_1 - 1f_2$ if $f_1 = (f_o + \Delta f)$ and $f_2 = (f_o + 2\Delta f)$. This particular tone (actually a set of identical *two tones*) rise at a slope intercept rate of 3:1. Consequently we would expect at a specific input power the linear slope power and the two tone slope power would be equal. An expression for spurious free dynamic range is readily obtained from graphical relationship of these parameters. The relationship for SFDR and the intercept point (IP3), (recall OIP3 is readily obtained from IIP3) is obtained from a slope diagram shown and detailed in Figure E.1. The input power along the x-axis and the output power along the y-axis provide the following set of equations. First, the linear gain has a slope of 1:1 therefore

$$\frac{(P_o - IP3)}{(P_1 - IP3 - G)} = 1 \quad (\text{E.1})$$

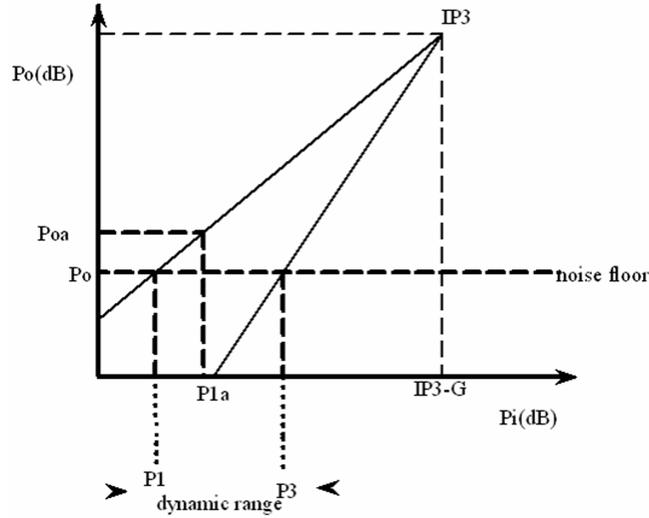


Figure E.1: Slope intercept graph...Output power vs. input power of a stage or system. Extrapolation of the 1:1 linear response and the 3:1 third-order intermodulation response intersect at the IP3 point

and it follows simply,

$$P1 = P_o - G . \tag{E.2}$$

The third order intermodulation distortion slope intercept form is

$$\frac{(P_o - IP3)}{(P_3 - (IP3 - G))} = 3 \tag{E.3}$$

and it follows then that we have,

$$P_3 = \frac{(P_o + 2IP3 - 3G)}{3} \tag{E.4}$$

and the dynamic range is obtained from $P_3 - P_1$, equation (E.4) and equation (E.2). Thus,

$$DR = \frac{2}{3} (IP3 - P_o) . \tag{E.5}$$

Note that we have conveniently placed P_o equal to the level of the noise floor. Since no spurious power level was considered, the level associated with P_{oa} is the same as the noise power. The dynamic range defined (DR) is limited only by the noise power. For discrete signals at the level of P_{oa} and with $P_{oa} > P_o$, the DR is further limited to the SFDR. Normally the case of the existence of discrete tones is not considered. However it is a very real situation, for example in hybrid analog-digital systems and therefore for completeness is included. So in this analysis the SFDR is defined for the case where the 3rd order distortion level is equal to the noise power level. This is the maximum SFDR. If the requirement for the signal-to-noise ratio or SNR is larger, ($SNR = P_{oa} - P_o$), then the dynamic range is correspondingly smaller. Note, if the power is referred to the input, P_i and this is just equal to the noise floor or a SNR_{min} of 0 dB, then this level is defined as the minimum detectable signal (MDS). Our expression for DR is modified accordingly as

$$DR = \frac{2}{3}(IP3 - MDS) . \quad (E.6)$$

Depending on our reference, either input or output cascade power level, distortion, and noise, the input and output dynamic ranges are appropriately defined but are equal as:

$$DR_o = DR_i = \frac{2}{3}(OIP3 - MDS_{dBm,o}) = \frac{2}{3}(IIP3 - MDS_{dBm,i}) . \quad (E.7)$$

Appendix F

Oscillator Equivalent Input Noise

The time representation of the oscillator signal is given by

$$f(t) = A(t) (\cos \omega_o t + \varphi(t)) \quad (\text{F.1})$$

where $f(t)$ represents a voltage or current, and for an ideal oscillator $A(t)$, $\varphi(t)$, and $\omega_o t$ are constant. However, for a noisy oscillator $A(t)$ and $\varphi(t)$ are slowly varying real functions of time. Without a mechanism for the conversion of amplitude variations to phase variations, $A(t)$ will be neglected and we will assume it does not contribute to fluctuations in frequency. It is customary to represent $\varphi(t)$ as zero-mean stationary process with an instantaneous phase departure described by

$$\varphi(t) = \int_0^{\infty} \dot{\varphi}(t) dt + \varphi(0) \quad (\text{F.2})$$

and instantaneous angular frequency by the sum of the derivative of (F.2) and the steady state angular frequency given by

$$\frac{d}{dt} (\omega_o t + \varphi(t)) = \dot{\varphi}(t) + \omega_o. \quad (\text{F.3})$$

Thus, (F.3) represents the instantaneous departure from an otherwise constant carrier frequency ω_o . Consequently, the ideal noise-free oscillator frequency is characterized by a single spectral

line in which both the amplitude and frequency (or phase) of this component is modulated by random functions of time. The process described by $f(t)$ is assumed to be a narrowband stationary Gaussian random process since an oscillator is characterized by a relatively selective circuit, and all the effects of interest are concentrated in a relatively narrow region of frequencies.

An aid in characterizing $\varphi(t)$ is spectral analysis. The frequency domain information about frequency or phase fluctuations is contained in the power spectral density of phase fluctuations, $S_\varphi(\omega)$. These fluctuations in phase can be measured directly at the carrier frequency via a spectral analyzer, as they appear as modulation sideband lines about the carrier, or at baseband, at low frequency offsets from the carrier, $S_\varphi(\omega_m)$. Low frequency measurement is accomplished through frequency translation of the carrier (presumably through a mixing process with another oscillator with significantly less fluctuations in phase than the device under test), to a low frequency phase discriminator for measurement.

Measurement of $S_\varphi(\omega_m)$ is accomplished via phase or frequency detection. Noise modulation of the carrier frequency is considered a narrowband frequency modulation (FM) process. Therefore, the power spectral of phase is related to the power spectral density of frequency.

Consider sinusoidal frequency modulation, given by,

$$\omega(t) = \omega_o + \Delta\omega_{\text{peak}} \cos \omega_m t. \quad (\text{F.4})$$

Then

$$\varphi(t) = \int \omega(\alpha) d\alpha = \omega_o t + \frac{\Delta\omega_{\text{peak}}}{\omega_m} \sin \omega_m t \quad (\text{F.5})$$

or simply

$$\varphi(t) = \omega_o t + \Delta\varphi_{\text{peak}} \sin \omega_m t. \quad (\text{F.6})$$

Substitution of (F.6) into (F.1) gives the time representation for the frequency modulated signal. Expansion of the time representation of this signal and employing trigonometric identities, yields the familiar FM representation for a signal. If this signal is subject to modulation, either in frequency or phase, with a very small deviation of the carrier frequency in relation to

the carrier frequency, the so-called narrowband FM approximation yields $f(t)$ as

$$f(t) = A_c \left[\cos(\omega_c t) + \frac{\beta}{2} \cos(\omega_c + \omega_m)t - \frac{\beta}{2} \cos(\omega_c - \omega_m)t \right], \quad (\text{F.7})$$

where β is defined as the modulation index, the ratio of the carrier deviation to the deviation rate, and must be small, i.e. $\beta \ll \pi/2$ radians. The Fourier transform of $f(t)$ permits describing the signal in the frequency domain. The Fourier transform of (F.7) results in the n^{th} order Bessel function of the first kind with argument β . In the frequency domain, the spectral content of $f(t)$ is completely described by a pair of single sidebands whose amplitude in relation to the carrier signal is $\beta/2$, see Figure F.1. The amplitude of these spectral lines are uniquely defined by the zeroth order and first order Bessel functions of the first kind, $J_0(\beta)$, $J_1(\beta)$, and for $J_n(\beta) \approx 0$ for all $n > 1$.

The single sideband or one sided noise to signal power ratio is expressed as $(V_n/V_s)^2$ and from Figure F.1 and the defining amplitude of the spectral lines we have,

$$\frac{\beta^2}{4} = (V_n/V_s)^2. \quad (\text{F.8})$$

The random phase fluctuation, $\Delta\varphi$, is a RMS measured value. The spectral density of phase noise is the ratio of the total mean square noise voltage normalized to the mean square signal voltage. Therefore, using (F.8) and the definition of spectral density, we have

$$\Delta\varphi_{\text{rms}}^2 = 2 \left(\frac{V_n}{V_s} \right)^2 \equiv S_\varphi(\omega_m). \quad (\text{F.9})$$

The function $L(f_m)$ used in our work and characterized for the oscillators measured, is also defined as the ratio of the noise power to the carrier power. Therefore, the power spectral density of phase noise is twice $L(f_m)$, and we have the spectral density of phase noise as:

$$S_\varphi(\omega_m) = \Delta\varphi_{\text{rms}}^2 = 2L(\omega_m). \quad (\text{F.10})$$

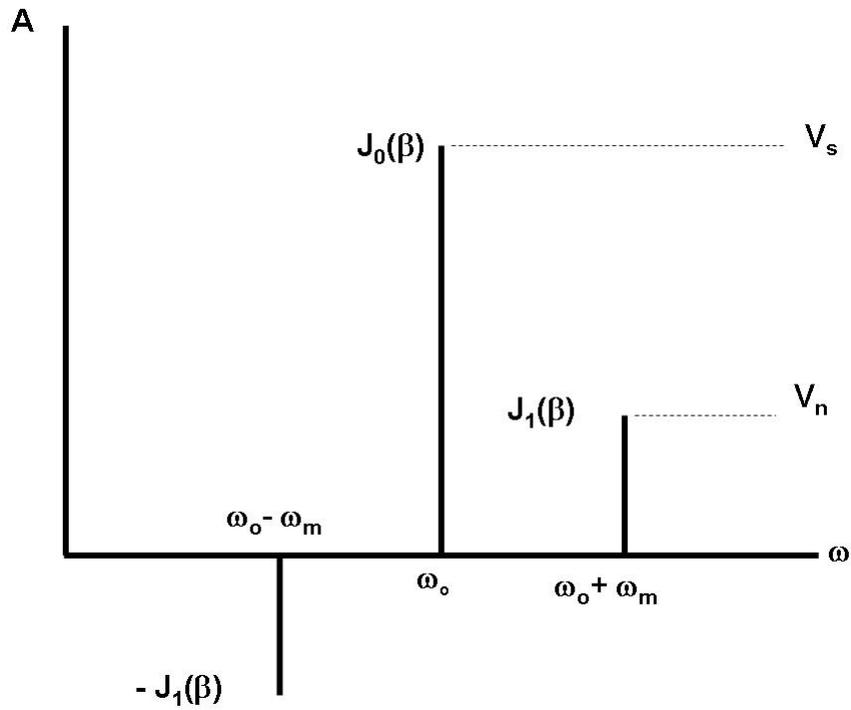


Figure F.1: Narrowband single tone FM modulation spectrum, V_s and V_n are signal voltage and noise voltage respectively which give rise to carrier and noise power levels in the frequency domain.