

ABSTRACT

WHEELER, VIRGINIA DANIELLE. Structure and Properties of Epitaxial Dielectrics on GaN. (Under the direction of Mark Johnson).

GaN is recognized as a possible material for metal oxide semiconductor field effect transistors (MOSFETs) used in high temperature, high power and high speed electronic applications. However, high gate leakage and low device breakdown voltages limit their use in these applications. The use of high- κ dielectrics, which have both a high permittivity (ϵ) and high band gap energy (E_g), can reduce the leakage current density that adversely affects MOS devices. La_2O_3 and Sc_2O_3 are rare earth oxides with a large E_g (6.18 eV and 6.3 eV respectively) and a relatively high ϵ (27 and 14.1 respectively), which make them good candidates for enhancing MOSFET performance. Epitaxial growth of oxides is a possible approach to reducing leakage current and Fermi level pinning related to a high density of interface states for dielectrics on compound semiconductors. In this work, La_2O_3 and Sc_2O_3 were characterized structurally and electronically as potential epitaxial gate dielectrics for use in GaN based MOSFETs. GaN surface treatments were examined as a means for additional interface passivation and influencing subsequent oxide formation.

Potassium persulfate ($\text{K}_2(\text{SO}_4)_2$) and potassium hydroxide (KOH) were explored as a way to achieve improved passivation and desired surface termination for GaN films deposited on sapphire substrates by metal organic chemical vapor deposition (MOCVD). X-ray photoelectron spectroscopy (XPS) showed that KOH left a nitrogen-rich interface, while $\text{K}_2(\text{SO}_4)_2$ left a gallium-rich interface, which provides a way to control surface oxide formation. $\text{K}_2(\text{SO}_4)_2$ exhibited a shift in the O1s peak indicating the formation of a gallium-rich GaO_x at the surface with decreased carbon contaminants. GaO_x acts as a passivating layer prior to dielectric deposition, which resulted in an order of magnitude reduction in leakage current, a reduced hysteresis window, and an overall improvement in device performance. Furthermore, $\text{K}_2(\text{SO}_4)_2$ resulted in an additional 0.4 eV of upward band bending at the surface, which should be considered when determining heterojunction band offsets with GaN.

Epitaxial La_2O_3 and Sc_2O_3 were successfully deposited on GaN by molecular beam epitaxy (MBE). Sc_2O_3 exhibited a cubic bixbyite crystal structure, while La_2O_3 had a mix of

both cubic and hexagonal crystal structures. A highly defective structure was observed for La_2O_3 , compared to Sc_2O_3 , which results from its larger mismatch with GaN (14.5% and 8.9%, respectively). TEM images indicated an abrupt atomic interface for Sc_2O_3 films, but an interfacial layer was observed for La_2O_3 on GaN. Additionally, La_2O_3 was shown to be extremely reactive with water and carbon dioxide in air, forming both hydroxides and carbonates within 15 minutes of exposure. Therefore, tantalum and silicon were investigated as *in-situ* capping metals to prevent these deleterious effects.

XPS was utilized to determine a valence band offset (VBO) and conduction band offset of 1.9 ± 0.1 eV and 0.9 ± 0.1 eV for La_2O_3 on GaN. Similarly, Sc_2O_3 had a VBO and CBO of 0.8 ± 0.1 eV and 2.1 ± 0.1 eV, respectively. Both oxides exhibited sufficient band offsets to prevent thermionic emission of carriers, even at high operation temperatures, making them good candidates for insulator layers in high temperature, high power applications.

Preliminary C-V curves, for La_2O_3 and Sc_2O_3 MOS capacitors, showed large charge accumulation layers, extremely high permittivity values, and low hysteresis windows indicative of low density of interface traps and fixed oxide charges. I-V curves showed a reduction in leakage current density for both oxides compared to Si_3N_4 , a readily used gate dielectric for GaN devices. The larger reduction achieved with La_2O_3 films is attributed to a passivating interfacial layer that minimizes the amount of dislocations propagating into the oxide. These preliminary results point to the viability of these gate oxides in GaN MOSFET devices.

Structure and Properties of Epitaxial Dielectrics on GaN

by
Virginia Danielle Wheeler

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APPROVED BY:

Dr. Mark Johnson
Associate Professor of Material Science
Chair of Advisory Committee

Dr. Doug Barlage
Associate Professor of Electrical and
Computer Engineering

Dr. Jon-Paul Maria
Associate Professor of Material Science

Dr. Zlatko Sitar
Professor Material Science

Dr. Douglas L. Irving
Assistant Professor of Material Science

BIOGRAPHY

From the day Virginia (Ginger) Wheeler was born in 1983, she was either in the lab or on the playing fields. Having been born to two research scientist, her “play-pen” was the lab floors, desks, and offices, while her “dolls” were the graduate students, scientist, and any piece of equipment she was allowed to touch. Though this environment cultivated her love of science and curiosity for learning at an early age, it also developed a desire to enjoy time away from the lab and school. Generally, this meant time spent outdoors or playing one of many sports including soccer, basketball, baseball, and eventually running.

Her parents have always taught her the importance of education, hard work, diversity, commitment, and giving back to the community. Even during her elementary years, she was involved in a variety of activities including girl scouts, sports, music lessons, and student government. As a 5th grader she was elected student body president of her elementary schools, giving her an opportunity to cultivate her leadership skills that has proved to be essential to her success in life.

Unlike many students, Ginger spent many of her middle school afternoons in a lab carrying cell line stocks. For her 6th grade science fair project, she studied the effect of temperature and radiation on the growth of different types of tumor cells. This not only helped her get 3rd place in the NC state science fair, but got her name (with her parents) on her first publication. This sense of accomplishment helped her realize she had a future in science. It was also during her middle school years that she found her knack for running. Though reluctant to join the team at first, she found she enjoyed pushing herself to her limits and seeing the success of hard-work. During this time, she began to dream of becoming a collegiate-athlete and getting a scholarship to school.

In high school, she was fortunate to make the soccer, basketball, cross country and track varsity teams as a freshman. Her success on the teams lead to her being elected captain as only a sophomore. Over three years, she learned the importance of caring and putting teammates first for the overall success of the team. Achieving on the playing field

was not the only priority in her life, as she obtained her goal of graduating with academic honors. In addition, her parents believed she should learn the importance of financial responsibility by working to pay for the expenses of her car. Therefore, if she wasn't at practice or in class, she was working at a local restaurant. Though overwhelming at times, this busy schedule taught her how to be efficient and organized which has proved vital to achieving her goals.

In her junior and senior years, Ginger began to achieve statewide and national running success. Her hard work and determination paid off when she was offered a scholarship to run on the cross-country and track team at North Carolina State University. The opportunity to earn an engineering degree and participate on a nationally ranked top 10 team was more than she had ever dreamed. Although she came to NCSU expecting to get a degree in chemical engineering, she was persuaded by a teammate to explore material science and engineering. It took only one class for her to know that this was what she wanted to pursue as a career.

Though most of her time was spent either running or in the classroom, she also found time to hold internships with the PET lab at Wake Forest School of Medicine and Kucera Pharmaceuticals on NCSU's centennial campus. Throughout her undergraduate career she obtained several awards including: Academic All-ACC, All-Regional cross country team, NCAA regional competitor, and graduating magna cum laude. She spent two years on the Student Athlete Advisory Committee (SAAC), including her final year as the Vice President and chair of the community service committee. As a liaison between the athletes and those in charge of the athletic department, she was afforded an opportunity to observe and impact the way a department within the university was run. This fostered her love of universities and her hope to one day give back by teaching as a professor.

Initially, Ginger believed that graduate school was not an immediate goal, but her desire to use her last year of running eligibility convinced her to at least get a Masters degree. With a little persuasion from Dr. Johnson, she decided to strive for a PhD so that she could one day become a professor and make an impact on the next generation. She was awarded the GAANN fellowship for studies in microelectronics, which provided the

funding for her work on GaN electronic devices. Through this fellowship she was also able to spend a year observing and teaching in the Preparing for the Professoriate program. During her graduate career, she continued to pick up new duties including sitting on the newly awarded NSF FREEDM center's student leadership council. Though more time was spent on research and science, she still found time to compete for the NCSU cycling club and in many triathlons. These extra curricular activities have fed her need for competition and provide a healthy outlet in very stressful times.

After graduating, Ginger is lucky enough to have been offered a Postdoctoral Fellowship with the power electronics group at the Naval Research Labs in Washington, DC working on improving the growth of SiC for high power devices. She looks forward to a new challenge in a new environment, but will never forget the experiences, family and friends she is leaving behind in North Carolina.

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I would not have been able to complete this doctoral degree without the support, encouragement and assistance of many people. Most importantly, I would have never even considered a doctoral degree if it weren't for the persuasion of my advisor Dr. Johnson. I am undoubtedly indebted to him for his constant encouragement, advice, and belief in me. Significant recognition is also due to Dr. Barlage who is always willing to stop for discussions and questions about my work. His humorous personality has often provided comic relief in stressful situations, which makes me look forward to group meetings no matter what the topic. I am also very grateful to the rest of my committee: Dr. Maria – who has provided many resources and suggestions without which I would not have been able to complete my research, Dr. Sitar – for asking the tough questions that challenge me to review my research and become a better scientist, and Dr. Irving – for his willingness to join my committee on a short notice and the new ideas he brings to the table.

My research would not have been possible without the help of Dan Litchenwalner, Jesse Jur, Matt Veety, and Mike Morgensen who helped with the deposition of oxides and the fabrication and testing of devices. All of these people have been willing to provide expert advice, and put up with the pushy-side of me at one time or another, for which I am truly grateful. A special thanks to Jess for helping get my thesis project moving in the right direction, providing much needed guidance at times, challenging me to be a better researcher, and reminding me to breathe at the most opportune times.

I would also like to thank my many collaborators including: (i) Fred Stevie, Chuck Mooney, Dale Batchler, Wingo Wong, and Roberto Garcia at NCSU's AIF center for all their help on XPS, AFM, SEM, and TEM sample preparation and imaging; (ii) Mark Walters and Michelle Gignac at Duke's SMIF facility for training and use of the XPS, XRD, and TEM equipment; and (iii) Keith Evans, Drew Hanser, and Tonya Paskova for their help and substrate wafers needed for on-going research. Special thanks is also owed to Edna Deas, who keeps our department running and who is solely responsible for making sure my funding and paperwork is always completed.

Many thanks are also owed to my group members Alvin and Judy, who are always there to help with the MOCVD or any other question or problems that arise. I will miss the many conversations, smiles and laughs shared while doing maintenance and other odd jobs. Thanks for your support! Also to Niv, thanks for being so patient with me as I am trying to finish up the doctoral work, and good luck with the MOCVD next year.

I would like to thank my friends Sarah Haney, Michelle Casper, and Sarah Arvidson who have made my graduate experience more satisfying. I appreciate all the talks, bike rides, swims, dinners, advice and support each of you has provided me over the last few years. I would not be the person I am today without each of you, and for that I will always be grateful. Also, to Dr. Maria's electronics group thank you for "adopting" me and allowing me to tag along to various events. I have enjoyed getting to know all of you and hope the best for you in your future endeavors.

Finally, I would like to thank my family for their unending support and guidance over the last 26 years. Without you I would not have achieved the successes I have. To my parents Anne and Ken, thanks for being such wonderful role models, believing in me and teaching me that striving for excellence doesn't require sacrificing a balanced life. I hope that I continue to make you proud in my future endeavors. To my brother Trey, thanks for being my best friend and confidant. I know you've been there for some ranting and tears throughout my graduate career, but luckily you always know what to say to make me feel like I can accomplish anything. I am so proud of you and though I may not be able to fly helicopters around the world, I will always be here if you need to remember what home is like. To Chad (yes you are family), thank you for always being by my side through all the highs and lows. I look forward to the day when the distance between us is only a couple of feet. Until then I know you will continue to encourage me to step outside of my comfort zone and take on all the challenges life hands me.

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LIST OF PAPERS AND PRESENTATIONS

1. "Characterization of acidic and basic wet etches for surface passivation of GaN for FET applications." V.D. Wheeler, J.S. Jur, M.A.L. Johnson, M.T. Veety, M.P. Morgensen, D.W. Barlage. Resubmitted to *Materials Letters* May 2009.

2. "Characterization of epitaxial gate oxides used for GaN passivation." V.D. Wheeler, J.S. Jur, D. Lichtenwalner, M.A.L. Johnson, M.P. Morgensen, D.W. Barlage. Submitted to *Physica Status Solidi (a)* Apr. 2009.

Oral presentation of paper given at IWN conference Montreux, Switzerland October 6-10, 2008.

3. "Enlargement of bulk non-polar GaN substrates by HVPE regrowth." K.Y. Lai, V.D. Wheeler, J.A. Grenko, M.A.L Johnson, A.D. Hanser, E.A. Preble, L. Lui, T. Paskova, and K.R. Evans. Submitted to *Physica Status Solidi (c)* Sept. 2008.

4. "Epitaxial rare earth oxide growth on GaN for enhancement-mode MOSFETs." J.S. Jur, V.D. Wheeler, M.T. Veety, D.J. Lichtenwalner, D.W. Barlage, M.A.L. Johnson. *CSMANTECH Conference 2008* paper 7.4.

5. "Gallium Nitride surface treatment study for FET passivation process flow applications." M.T. Veety, V.D. Wheeler, M.P. Morgensen, M.A.L. Johnson, D.W. Barlage. *CSMANTECH Conference 2008* paper 11.2.

6. "Fabrication and Characterization of Native Non-Polar GaN Substrates." D. Hanser, L. Lui, E.A. Preble, K. Udwary, T. Paskova, R. Kroeger, P. Paskov,

K-Y Lai, V.D. Wheeler, M.A.L. Johnson, W. Everson, I. Agafonov, O. Kordina, and G. Reitano. *5th IWBNs 2007* paper.

7. "Characterization of non-polar surfaces in HVPE grown Gallium Nitride." Kun-Yu Lai, Judith A. Grenko, V.D. Wheeler, Mark Johnson, E.A. Preble, N. Mark Williams, and A.D. Hanser. ***Mater. Res. Soc. Symp. Proc.*** 955, 095-I09-05, 2007.

Poster presentation of paper given at 2007 NCSU Women in Science conference.

1. GaN Solid-State Devices

Traditionally, silicon is the choice of semiconductor for high-voltage power electronic applications ¹. Yet recently, new attention has been brought to wide band gap semiconductor materials whose material properties allows the potential for better efficiencies, higher linearity, ultra-high power, and higher temperature operation than silicon ². Table I compares the intrinsic materials properties of various semiconductors. As shown below, nitrides exhibit both wide band gaps (E_g) and low intrinsic carrier concentrations (n_i), which make them suitable for high temperature applications. In addition, their high electron mobilities (μ_e) create large sheet carrier densities useful for faster response and better efficiency in high frequency applications. GaN and AlN also have very high breakdown fields (E_b), which allow them to support large voltages for high power operation. SiC is also well-suited for similar high temperature, high frequency, and high power applications and has been developed over a longer period than the nitrides. However, GaN still has greater potential due to its larger band gap, higher saturation velocity (v_{sat}), and higher electron mobilities ³. The III-N family also offers the possibility of even higher mobilities and sheet carrier densities by implementing AlGaN/GaN heterojunctions with a 2D electron gas.

Table I: Material properties of various semiconductors for power electronic devices ^{1,3-4}

	E_g (eV)	μ_e at 300K (cm ² /Vs)	Electron v_{sat} (cm ² /s)	E_b (MV/cm)	$\lambda_{therm.}$ (W/K-cm)	ϵ	n_i (cm ⁻³)	Ultimate Operation Temp.(°C)
Si	1.1	1350	1×10^7	0.3	1.5	11.8	1.5×10^{10}	200
4H-SiC	3.3	720	2×10^7	2.0	4.5	10	8.2×10^{-9}	>350
6H-SiC	3.0	600	2×10^7	3.0	4.5	9.7	2.3×10^{-6}	>350
GaAs	1.4	8500	2×10^7	0.4	0.5	12.8	1.8×10^6	350
GaN	3.4	1350	3×10^7	3.3	1.7	9.5	1.9×10^{-10}	700
AlN	6.2	1100	1.8×10^7	11.7	2.7	8.7	$\sim 10^{-31}$	--

GaN-based devices were initially developed and commercialized for optoelectronic devices, such as light emitting diodes (LEDs) and lasers ²⁻³. The direct band gap can be tuned with varying amounts of Al, Ga, and In to achieve green, blue, and UV LEDs, which previously were unattainable. Recently, this material system has been explored for use in two new electronic applications: (i) high-power radio/microwave frequency (rf) amplifiers (up to 10 GHz) for radar, satellite, and wireless broadband communication ^{3, 5-6}, and (ii) ultra-high power switches for distribution control on electric grid networks and electric vehicles ^{3, 6-7}. AlGaN/GaN high electron mobility transistors (HEMTs) have lead the way in high power rf-applications, but have been plagued by high gate leakages which severely increase power loss of these devices. Therefore, it is adventitious to incorporate an insulated gate structure, such as the metal-oxide-semiconductor field effect transistor (MOSFET), to reduce parasitic gate leakage. This thesis will focus on the use of high-k oxides in GaN-based MOSFETs for improved device performance and reliability for the high temperature, high frequency, and high power applications discussed above.

1.1 Figure of Merit Comparison with Silicon

Several figures of merit (FOM) have been established to quantify intrinsic performance potential for various power devices. With all the figure of merits described below, higher values indicate better predicted device performance. In 1965, Johnson derived a figure of merit (JFOM) that defines the power-frequency product for a low voltage device, as indicated by the equation ⁸

$$JFOM = \left(\frac{E_b V_{sat}}{2\pi} \right)^2. \quad (1.1)$$

This equation accounts for the trade off between the time a carrier spends gaining speed in an electric field as it drifts through an intrinsic device and the response time of the device ⁹. However, it does not consider thermal effects.

In 1972, Keyes defined a figure of merit (KFOM) that considered the thermal limitation on the switching behavior (or speed) of a transistor ¹⁰. In his derivation, it was assumed that smaller devices have faster responses at a fixed-electronic input impedance

level. Yet, device size cannot be reduced without increasing power losses due to a higher thermal resistance. As thermal resistances increase, it is more difficult to remove heat from the device and increases the operation temperature ⁹⁻¹⁰. Thermal resistance is inversely proportional to the thermal conductivity (λ) of the semiconductor. Therefore, the materials dependent KFOM can be expressed as

$$KFOM = \lambda \left(\frac{c V_{sat}}{4\pi\epsilon} \right) \quad (1.2)$$

where c is the velocity of light, and ϵ is the dielectric constant of the semiconductor.

In 1983 and 1989, Baliga defined a figure of merit for low frequency power switching (BFOM) and high frequency power switching (BHFFOM) respectively ¹¹⁻¹². The BFOM assumes that power losses are due solely to power dissipation by current flow through the on-resistance of the transistor. Therefore, it only holds true for low frequencies where the conduction losses dominate. Material parameters that minimize conduction losses, such as mobility and band gap energy, were used to derive the BFOM.

$$BFOM = \epsilon \mu_e E_g^3 \quad (1.3)$$

For high frequency power devices, it is necessary to include the switching losses that were neglected in the previous case. It is assumed that the switching losses result from the charging and discharging of the input capacitance of the transistor ¹¹. The BHFFOM is expressed as

$$BHFFOM = \mu_e E_b^2. \quad (1.4)$$

Table II shows all figures of merits for a variety of promising semiconductor materials normalized to silicon. For the JFOM, the higher breakdown electric field of the wide band gap materials dominates, making them more promising than silicon and GaAs. SiC has the highest KFOM, due to its large thermal conductivity, which makes it appealing for devices whose operation is thermally limited, such as bipolar transistors. The nitrides have the highest values for both BFOM and BHFFOM as a result of their large band gaps and high electron mobilities. Therefore, devices with electronic limitations, like field effect transistors (FETs) should benefit from the higher power density provided by these materials. Based on Table II, GaN is predicted to have superior performance over silicon and SiC in high power,

high frequency and high temperature applications. For this reason, the research in this thesis focuses on improving the reliability and performance of GaN-base FETs for use in integrated circuit technology.

Table II: Comparison of Normalized Figure of Merits for Various Semiconductor Materials ⁹

	<i>JFOM</i>	<i>KFOM</i>	<i>BFOM</i>	<i>BHFFOM</i>
<i>Si</i>	1	1	1	1
<i>GaAs</i>	11	0.45	28	16
<i>4H-SiC</i>	410	5.1	290	34
<i>6H-SiC</i>	260	5.1	90	13
<i>GaN</i>	790	1.8	910	100
<i>AlN*</i>	5.1	2.6	32000	1100

*High electron mobility AlN

1.2 GaN Deposition

GaN films are typically grown by several techniques including: metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), halide vapor phase epitaxy (HVPE), and pulsed laser deposition (PLD). Commercially, MOCVD and MBE are preferred for the growth of GaN electronic device structures. GaN substrates for this thesis were prepared by MOCVD; therefore, this is the technique that will be focused on in this section.

1.2.1 Substrate Availability for Deposition

One of the biggest obstacles to improving the performance of GaN electronic devices is the lack of single crystal substrates. GaN is typically grown on sapphire or silicon carbide substrates due to their similar crystallographic symmetry and non-reactivity under growth conditions ¹³. Both of these substrates have substantial lattice mismatches with GaN (Al_2O_3

= 15%, SiC = 3% ⁶), which can produce a high density of misfit threading dislocations and small-angle grain boundaries that can degrade the optical and electrical performance of GaN devices. Full relaxation occurs within the first monolayer of deposition by forming misfit dislocations. However, the remaining strain energy increases with film thickness and must be relaxed with a secondary set of threading dislocations throughout the GaN film ¹³. Along with lattice matching, thermal expansion coefficients of the substrate and GaN should be closely matched to reduce the amount of thermal stresses during growth ^{14, 15}. Although SiC has better thermal matching to GaN, sapphire substrates are generally used due to their availability, low cost, larger wafers, and simple pre-growth cleaning requirements.

More recently, advances have been made in producing free-standing bulk GaN wafers. Though the majority of these are used for growth of laser diodes, there is potential for these to make an impact in electronic devices as well (Fig. 1.1). Companies such as Sumitomo, Hitachi-cable, Mitsubishi Chemical, and Kyma Technologies have produced 2"-3" wafers with at least three-four orders of magnitude reduction in dislocation densities ($<5 \times 10^6 \text{ cm}^{-2}$) ¹⁶. With perfect lattice and thermal matching, only the dislocations present in the substrates should be replicated into epitaxial GaN films. Therefore, the active region of devices built on bulk GaN substrates will have fewer dislocations which should result in better device performance. Already vertical Schottky rectifiers have shown vast improvement using this homoepitaxial approach and point to the viability of GaN substrates in power devices ¹⁷. Though the results presented in this thesis are from GaN MOSFETs on sapphire substrates, current investigation is on-going to produce similar devices on bulk GaN substrates.

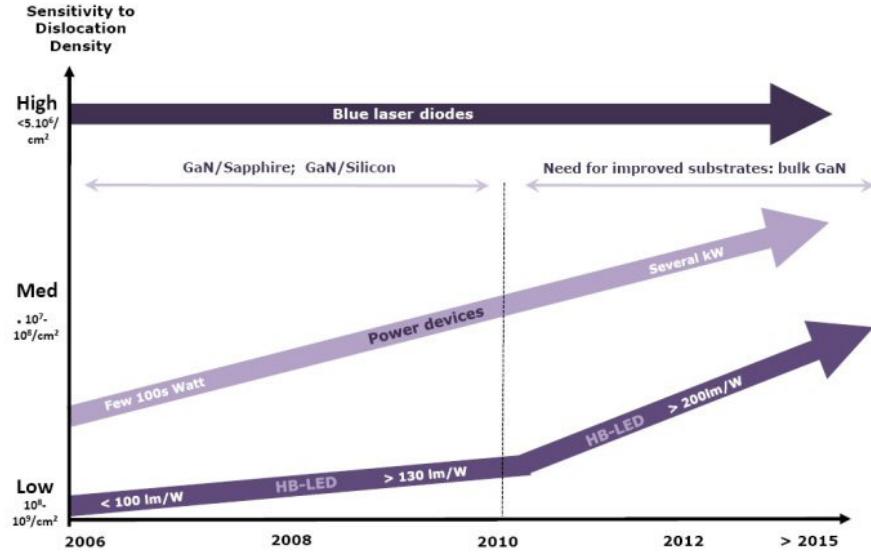


Figure 1.1: Sensitivity to dislocation density in the active layer for various nitride devices as reported by Yole Developpement¹⁶.

1.2.2 Metal Organic Chemical Vapor Deposition (MOCVD)

Deposition of GaN by MOCVD is a high temperature, non-equilibrium process. The metal cation species is delivered by a metal organic precursor in a dispersed gas, while the anion species is supplied by either an elemental gas or precursor molecule. Generally, the precursors used for GaN are trimethylgallium and ammonia, though any precursor with good reactivity, full pyrolysis, and transportability are suitable for growth. The chemical reaction occurring at the surface responsible for GaN deposition can be expressed as ^{18,19},



To achieve high quality crystalline films, the growth process must proceed at temperatures greater than 900 °C ²⁰. These high temperatures increase pyrolysis of ammonia, but also promote decomposition of the deposited films. Therefore, controlling deposition versus decomposition rates is critical to the success of GaN growth.

Although both horizontal and vertical chambers are used, they have the common requirement that reactants must only be allowed to interact on the surface of the substrate.

Any premature reactions can cause adduct formation that could possibly suffocate the growth or cause harmful contaminants within the film. Therefore, MOCVD reactors incorporate laminar flow at high operating pressures with separate precursor injection sites to minimize predeposition reactions. Uniform wafer coverage is obtained by rotating the substrate during deposition.

Due to the lack of lattice-matched substrates, a low temperature AlN or GaN buffer layer is deposited directly on the substrates. Before buffer layers were employed, poor quality GaN films were grown directly on sapphire resulting in high background carrier concentrations (up to 10^{20} cm^{-3}) and rough surface morphologies ²¹⁻²³. This is due to the fact that GaN nucleates as islands when grown directly on highly mismatched substrates, which once coalesced, result in polycrystalline structures with a high defect density. By using a buffer layer to initiate uniform two dimensional nucleation, step-wise growth of GaN can be achieved, which yields a less defective film.

Generally, the buffer layers are deposited at a temperature of 480-600 °C to a thickness of 20-50 nm ²⁰. This highly defective AlN buffer layer is known to contain both cubic and wurtzite phases, but during the transition to the high growth temperatures the buffer is converted to a highly oriented film ^{24, 25}. Processing conditions and thickness can greatly affect the quality and effectiveness of this low temperature buffer. Therefore, for each system some optimization must be completed in order to achieve high quality GaN films. For this thesis, an optimized AlN buffer grown at 500 °C was utilized for the growth of GaN films on sapphire.

The three general thin film growth modes shown in Fig. 1.2 include: Frank-van der Merwe (FM) 2D layer-by-layer growth, Volmer-Weber (VW) 3D island growth, and Stranski-Krastanow (SK) combination growth. In the SK mode, growth is initially layer-by-layer followed by island growth, which forms as a result of strain relief within the film.

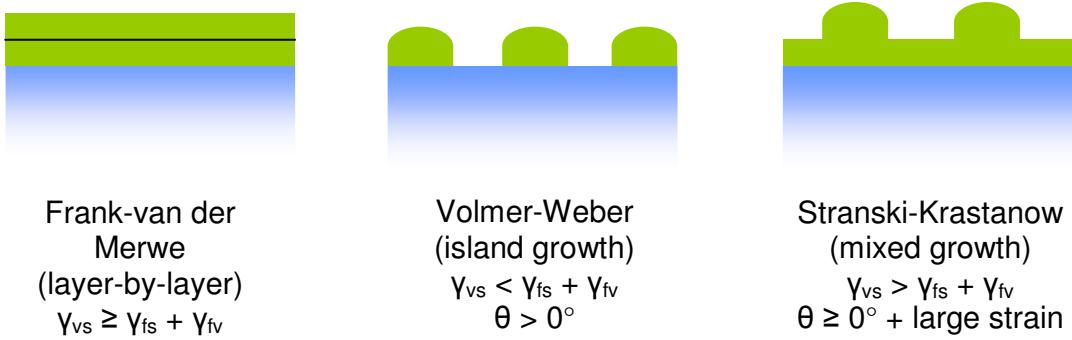


Figure 1.2: Simple schematic showing the three thin film growth modes and the conditions under which they can be achieved.

If thermodynamics are considered, the equilibrium growth mode is determined by the relative free energies of the substrate surface (γ_{vs}), the deposited film (γ_{fv}), and the substrate-film interface (γ_{fs}) ²⁶. This relationship is depicted in Fig. 1.2, where θ is the contact or “wetting” angle.

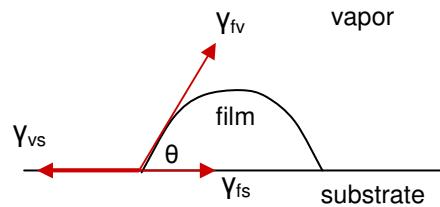


Figure 1.3: Schematic of a thin epitaxial island where the free energies and contact angle can be used to determine the equilibrium growth mode.

From this schematic, the expression used to determine equilibrium growth modes can be written as,

$$\gamma_{vs} = \gamma_{fs} + \gamma_{fv} \cos(\theta). \quad (1.6)$$

For θ between $0-180^\circ$, island growth is preferred, while when $\theta \approx 0^\circ$ layer-by-layer growth is preferred. SK growth generally occurs when there is wetting of the substrate along with a large strain energy in the film. Deposition of low-temperature buffer layers on sapphire substrates occur by VW island growth, which must be annealed to obtain adequate quality for GaN deposition. High-temperature GaN films contain a large amount of strain from the lattice mismatch with the buffer layers, which results in a SK growth mode.

1.2.3 Polarity and Surface Termination

Surface atomic configuration, composition, and chemical properties all depend on the polarity of the deposited film. Therefore, it is important to introduce briefly the polarity with MOCVD GaN films. Since there is often inconsistency in the definition of GaN polarity and termination, a little bit of time will be spent here clarifying these terms for the purpose of this thesis work.

Unlike most other III-V compounds, the equilibrium crystal structure of GaN is hexagonal wurtzite ($P6_3mc$). Fig. 1.4 shows this structure consist of two interpenetrating hexagonal close-packed lattices, each with different atoms, ideally displaced from one another by $5/8c$ along the z-axis ²⁰.

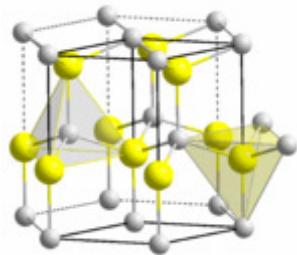


Figure 1.4: Basic hexagonal wurtzite structure

The $+c$ or [0001] direction is conventionally defined as the direction from the nitrogen plane to the gallium plane, and results in Ga-face or Ga-polar films. This terminology can be clearly understood when looking the tetrahedrally coordinated parts of the GaN crystal structure (Fig. 1.5). Nitrogen-centered tetrahedrons with gallium atoms at the corners have a face perpendicular to the c-axis in the $+c$ direction relative to its nitrogen core, resulting in the Ga-face polarity term ^{27, 28}. Similarly, gallium-centered tetrahedrons result in a nitrogen face perpendicular to the $-c$ direction, yielding the N-face polarity term.

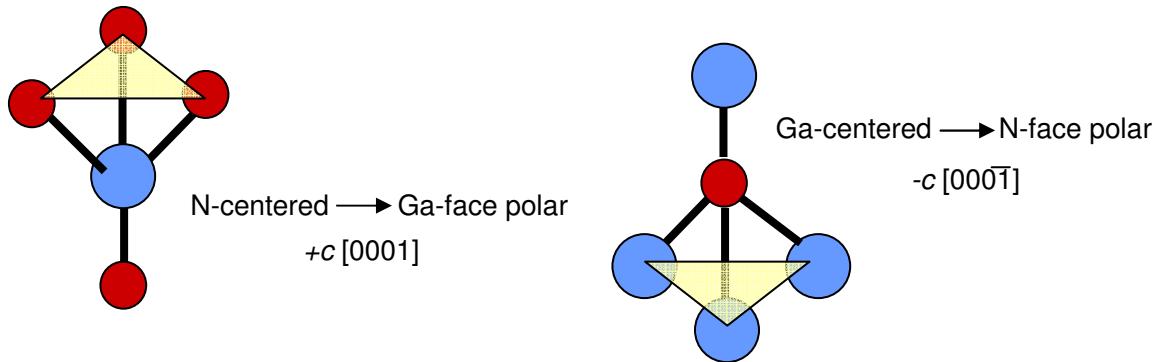


Figure 1.5: Schematic for clarification of polarity in GaN. N-centered tetrahedrals and Ga-centered tetrahedrals which lead to the “Ga-face” and “N-face” polarity are shown. The red circles are Ga atoms and the blue circles are N atoms.

Recent studies have shown that the polarity of MOCVD grown GaN can be influenced by growth with and without an AlN buffer layer. When the AlN buffer layer is deposited on sapphire, the first monolayer of film growth is a nitrogen monolayer²⁹. This results in an N-centered tetrahedron which according to Fig. 1.5 yields an Al-polar film. The polarity of this film is replicated into the subsequent film, producing a Ga-polar GaN film. However, when a GaN film is deposited without a buffer, the first nitrogen monolayer is tetrahedrally bonded to the Ga atoms as in the right-hand case of Fig. 1.5. This results in an N-polar GaN film. Until recently, N-face films grown by MOCVD were characterized by the large hexagonal hillocks and poor surface morphology.

Spontaneous and piezoelectric polarization of GaN leads to a polarized bound charge at the surface and GaN interfaces. The Ga-face surface exhibits negative bound charge, while N-face has positive bound surface charges³⁰. This surface charge must be compensated either by surface Fermi level pinning, surface reconstruction, or absorption of adatoms. Surface Fermi level pinning is known to result in band bending, which leads to an accumulation or oppositely charged layer that compensates the polarization-induced surface charge. This means that for Ga-face GaN films an upward band bending is expected, while N-face GaN films should exhibit downward band bending. The surface pinning caused by polarization can negatively affect the electronic properties of GaN-based devices. This thesis will continue to address Fermi-level pinning and its effect on MOSFET devices.

While polarity is a bulk property, termination refers to the surface of the GaN. Most GaN films are Ga-terminated, meaning that the last layer consist of gallium atoms. However, this does not change the polarity of the crystal. The films prepared in this thesis by MOCVD are Ga-polar with Ga-termination. The effect of surface treatment on termination will be explored, but the polarity of all the films will remain Ga-polar.

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2. GaN Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)

MOSFETs are the corner stone of intergrated circuit technology. The incorporation of enhancement-mode MOSFETs can be used to form single supply voltage control circuits for power transistors ¹. In addition, it allows the use of complementary devices which reduce power consumption ². MOSFETs also have the added benefit of an integrated oxide layer which provides passivation and a barrier to leakage. Therefore, these device exhibit lower leakage currents, greater voltage swings, lower power losses, and improved thermal stability over their Schottky gated device counterparts. This chapter will introduce the basics of MOSFET device structure and operation. Both Tsividis ³ and Streetman ⁴ provide and in-depth description of MOS transistors that can be referred to for addition information about the device discussed in this chapter.

2.1 Device Structure

MOSFETs are four terminal devices that have a gate electrode to regulate the flow of minority carriers through a channel from source to drain by varying the gate potential. This control gives the ability to amplify small a-c signals or switch the device off and on ³. Fig. 2.1 shows a schematic of a typical enhancement-mode MOSFET structure with a lightly doped substrate, highly doped contacts and a gate oxide. Enhancement-mode refers to the device being “normally off” or having negligible current at zero gate voltage. This is the safest mode in that high currents are only flowing once a voltage has been applied. The other mode of operation is a depletion-mode device which is a “normally on” device or one that has a channel at equilibrium or zero bias and requires a reverse bias to turn the device off.

The structure shown in Fig. 2.1 is an n-MOSFET since it will have electrons as the minority carriers through the p-type semiconductor substrate, resulting in what is termed an n-channel. Similarly, a p-channel device consists of an n-type semiconductor substrate through which minority hole carriers are conducted from the p-type source and drain

regions. In general, n-channels are preferred because of the higher mobility of electrons than holes in the semiconductor material. The lightly doped p-type channel (10^{16} - 10^{18} cm^{-3}) has a high electrical resistivity, which prevents the flow of carriers under zero bias. The source and drain regions are highly doped with silicon for GaN devices. This is done either by selective-area regrowth, ion implantation, or relatively recently Schottky metal contact such as Ni. Ion implant is not as easy for GaN as it is for silicon device, because it requires a long, extremely high temperature, high pressure anneal to recover the lattice and activate the silicon.

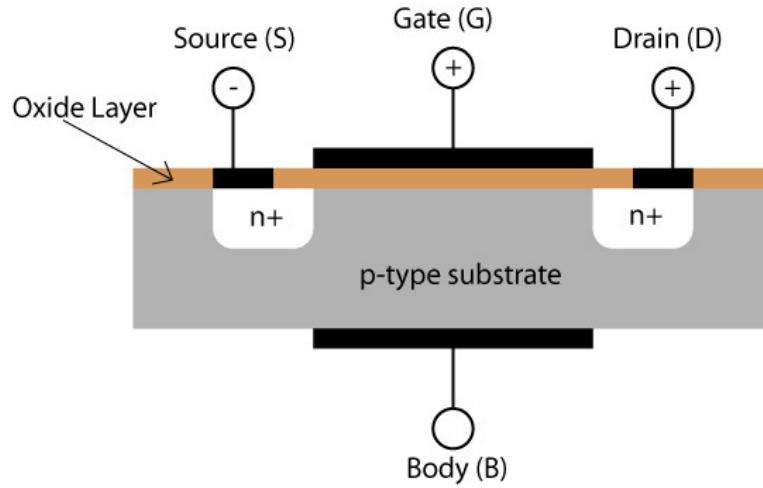


Figure 2.1: General schematic of an n-channel MOSFET with the four terminals labeled.

2.2 MOSFET Operation

The operation of MOSFETs will be discussed in this section considering a n-MOSFET as shown in Fig. 2.1 above. When a positive voltage is applied to the gate relative to the substrate, holes are repelled from the surface creating a depletion region of negatively charged acceptor ions (Fig. 2.2). This is what forms the channel and allows electrons to flow from source to drain. Sufficiently large positive biases can even attract free electrons to the surface, which can easily enter the channel region from either one or both of the highly doped source and drain regions. The depleted region that forms extends to both the n and

p sides of the junctions, but the part within the n region is much shallower due to the higher doping found there. Therefore, it is often not shown to simplify the structure. In addition, the depletion region around the drain junction is much deeper than the source because of the larger reverse bias applied.

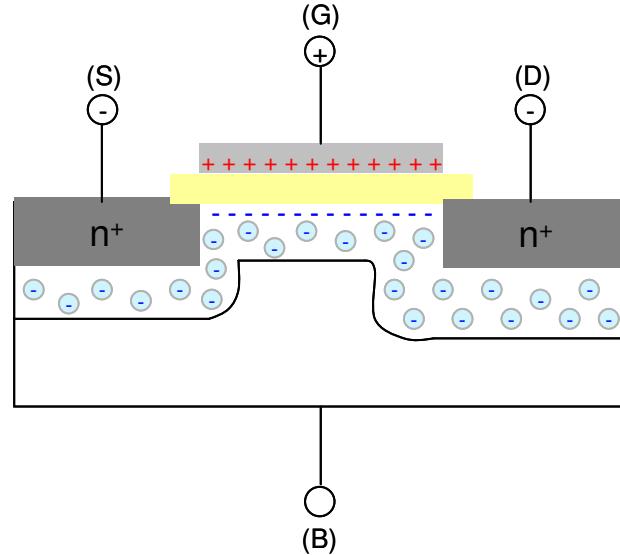


Figure 2.2: An n-MOS transistor under positive bias showing the depleted channel region and induced electronic charges.

The threshold voltage (V_T) is defined as the minimum gate voltage required to induce a channel. If a voltage is applied which is greater than the threshold voltage, a large current flow from source to drain is produced due to the lowering of the band barrier between the source and channel. Therefore, it is of utmost importance to have a high quality, low leakage p-n junction which can ensure a low leakage current in the off-state.

There are four modes of operation shown in Fig. 2.3 and will be discussed briefly here. Although an n-MOSFET will be considered here, the same concepts work with a p-MOSFET just oppositely applied voltages and band bending will occur. In essence the MOS structure shown in Fig. 2.1 works exactly like a capacitor.

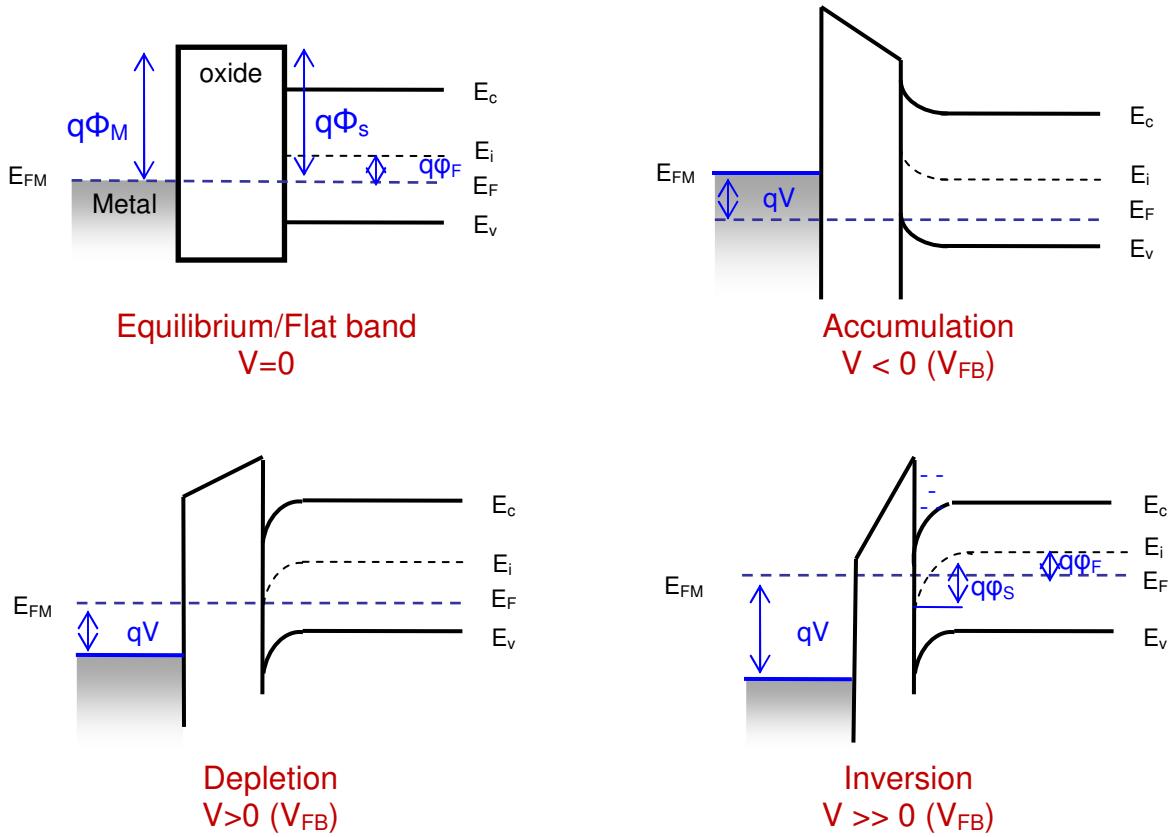


Figure 2.3: Four modes of operation for an n-MOSFET with a p-type doped substrate.

When no bias is applied the Fermi levels are aligned in all three materials, resulting in what is considered the flat band equilibrium condition. Remember that if this were a depletion mode device, a negative bias must be applied to reach this condition. If a negative gate voltage is applied, it induces a net positive charge on the semiconductor surface via hole accumulation. This causes the bands to bend upward at the surface to accommodate for the accumulation of holes. From the equation for hole concentration,

$$p = n_i e^{(E_i - E_F)/kT} \quad (2.1)$$

it can be seen that the band bending increases by an amount $E_i - E_F$. It is important to notice that the shift in the metal Fermi level compared to the semiconductor Fermi level causes a tilt in the oxide conduction band. This is expected because an electric field causes a gradient in the conduction, valence, and intrinsic Fermi energies.

Applying a positive voltage to the gate effectively raises the potential of the metal, which lowers the metal Fermi level by qV relative to its equilibrium position and tilts the conduction band of the oxide layer. Similarly to the previous case, the positive voltage causes a negative charge accumulation at the surface. Effectively the holes are depleted away from this area and leave behind ionized acceptors which account for the negative charge at the surface. As the holes concentration in this region is reduced, the bands bend downward to bring E_i closer to E_F .

If an even larger positive voltage is applied to the gate, the bands at the interface will bend more sharply and will eventually bring E_i below E_F , as depicted above. The larger positive potential attracts free electrons to the surface creating the case shown in Fig. 2.2. This extremely large electron concentration essentially acts as a n-type conduction layer. Although any time φ_s is greater than φ_F this inversion layer will be formed, but only under strong inversion ($\varphi_s \geq 2\varphi_F$) does a true n-type conducting channel exist. The total charge per unit area (Q_C) below the oxide during inversion is the sum of the charge due to the electrons in the inversion layer and the ionized acceptor atoms in the depletion region. This can be approximated by the equation,

$$Q_C = -\sqrt{2q\epsilon_s N_A} \sqrt{\varphi_s + \frac{kT}{q} e^{\frac{q(\varphi_s - 2\varphi_F)}{kT}}} \quad (2.2)$$

where ϵ_s is the semiconductor permittivity, N_A is the acceptor concentration, k is the Boltzmann constant, and q is the electron charge. This thesis will only test the accumulation region of devices for the purposes of determining the quality of the oxide layer.

2.3 General MOSFET Characteristics

Fig. 2.4 shows a typical current-voltage (I-V) family of curves for different gate biases. At small gate or drain biases, the current in the channel can become so small that it is masked by the leakage current of the reverse-biased drain-body junction, seen at the bottom of the plot³. At all applied gate voltages, the current saturates at the point where the differential channel resistance becomes too high to sweep anymore carriers through the

channel. This is generally considered the pinch-off voltage and is depicted by the dotted line in Fig. 2.4.

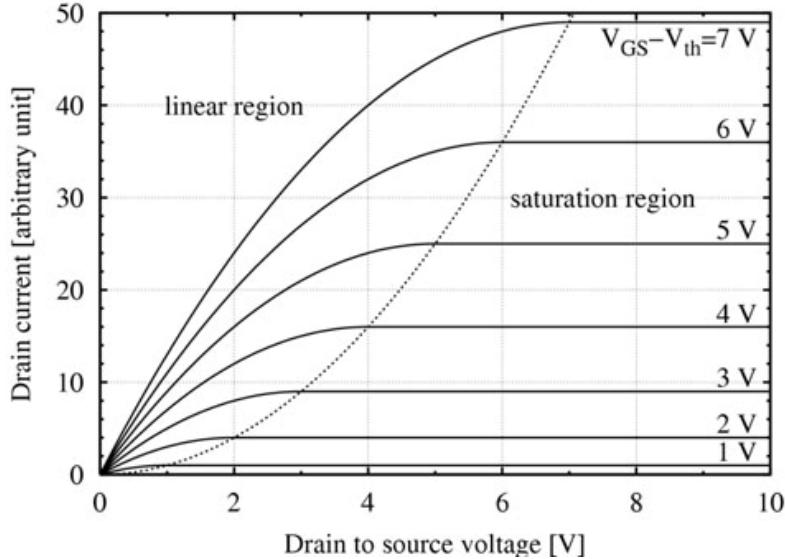


Figure 2.4: Typical MOSFET I_{DS} - V_{DS} characteristic showing gate control ability ⁵.

Current saturation is a function of gate bias as shown in Fig. 2.4. The current saturation can be expressed as ³

$$I_{DS} = \frac{W}{L} \mu_{eff} C_{ox} \frac{(V_G - V_T)^2}{2} \quad (2.3)$$

where W is the width of the depletion region, L is the channel length, μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, V_G is the gate bias, and V_T is the threshold voltage. Both the current and capacitance in this equation are per unit area quantities. The threshold voltage in this sense is defined as the voltage required for strong inversion. From Eq. 2.3, it can be seen that the saturation current is dependent on effective mobility and threshold voltage, which can be engineered through use of different materials. The quality of the oxide and interface contributions to threshold voltage will be discussed in Section 2.4 below.

A typical MOS capacitance-voltage curve is shown in Fig. 2.5 below. The three regions of operation illustrated in Fig. 2.3 are shown on the C-V curve below. While C-V curves are obviously voltage dependent, they also depend on the measurement frequency.

High frequencies are generally considered $> 1\text{MHz}$ and low frequency measurements are typically between $1\text{-}100\text{Hz}$. The terms “high” and “low” refer to the generation-recombination rate of the minority carriers within the inversion layer⁴.

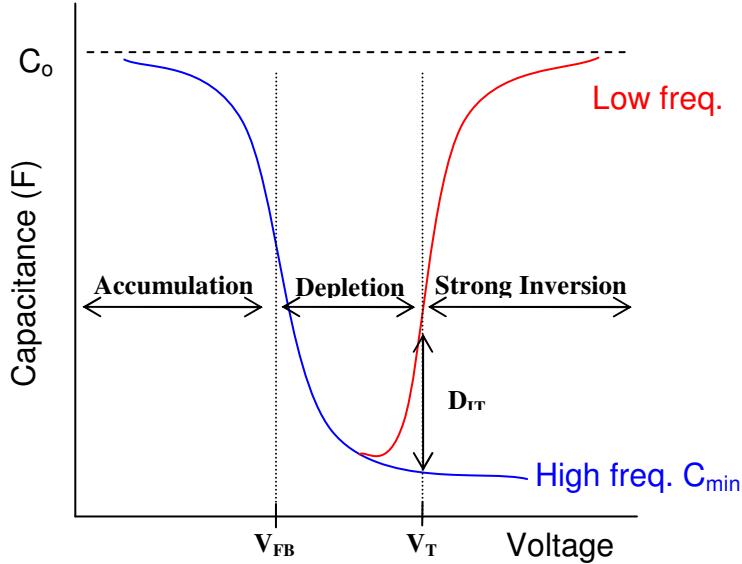


Figure 2.5: Typical MOSFET C-V curve showing both high frequency and low frequency response.

At high frequencies the charges in the inversion layer do not have time to respond to the rapidly changing gate voltage. The electron concentration within a MOS capacitor can only be changed by thermal generation and recombination, which is a slow process resulting from the growth of the depletion region. Therefore, at high frequencies the electrons do not contribute to the capacitance and the capacitance is at a minimum (C_{\min}), which corresponds to a maximum depletion width. While the high frequency capacitance for MOS capacitors is low, in MOSFETs it is high because the electrons can flow fast and easily from the source and drain regions rather than having to be created by generation-recombination in the bulk.

At low frequencies, the minority carriers have time to be generated in the bulk, drift across the depletion region into the inversion layer, or go back to the substrate and recombine. Therefore, in strong inversion the maximum capacitance can be reached (C_{ox}). This variation with frequency is not observed for the accumulation region of operation. This

is because the majority carriers in the accumulation layer can respond much faster than the minority carriers.

The capacitance for each region can be defined using the general equation ⁴

$$C = \frac{dQ}{dV_G} = \frac{dQ_s}{d\varphi_s} \quad (2.4)$$

where Q_s is the charge at the semiconductor surface. Since the gate-to-substrate voltage change will be distributed partly across the oxide and partly across the surface of the semiconductor the total capacitance can be rewritten in terms of the oxide capacitance and the semiconductor capacitance ³.

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \quad (2.5)$$

The semiconductor capacitance can also be separated into two components related to the depletion region charge (C_d) and the inversion region charge (C_i).

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d + C_i} \quad (2.6)$$

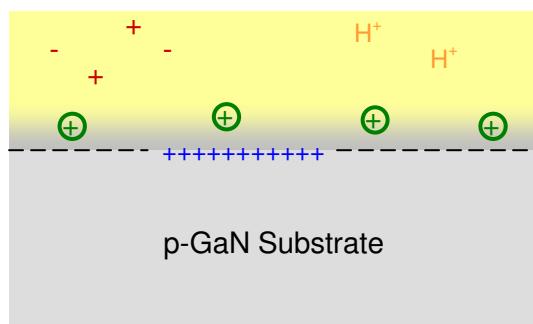
From Eq. 2.6 and the curve in Fig. 2.5, we can describe the capacitance in each region. For accumulation, C_s is very large which reduces the capacitance to approximately C_{ox} . When the gate bias is less than the flat-band voltage, the negative surface potential attracts holes to the surface directly under the oxide and the total incremental capacitance between these holes and the gate contact is essentially C_{ox} . In depletion and weak inversion, C_i is negligible and the resulting total capacitance is simply a series combination of C_{ox} and C_d . As the gate bias increases, the depletion capacitance decreases, accounting for the decrease in total capacitance seen in Fig. 2.5. During strong inversion, C_i increases rapidly and becomes the significant factor in the semiconductor capacitance. Since C_i is in parallel with C_d , the second term in Eq. 2.6 drastically decreases and the total capacitance will approach C_{ox} .

2.4 Interface and Oxide Charges

The previous sections assumed an ideal MOS transistor with no imperfections. However, there are inherently imperfection in the semiconductor, contacts, and oxide. This

section will discuss the effects of the imperfections within the oxide and at the oxide/semiconductor interface on the operation of the device.

Figure 2.6 shows the possible charges that can arise at the oxide/semiconductor interface and within the oxide. The four major charges include: (i) mobile ionic charge, (ii) oxide trapped charge, (iii) oxide fixed charge, and (iv) interface trap charge. Mobile ionic charges result from contaminants introduced by the environment during growth and processing. These ions can move freely within the oxide in the presence of an electrical field. The use of clean chemicals, gases, water, and processing environment greatly reduce these parasitic oxide charges. Oxide trapped charge usually exist at the interface of the oxide with either the semiconductor or the gate and are a consequence of oxide imperfections, ionizing radiation, high-energy carrier injection via avalanche or tunneling from the substrate. Oxide fixed charges are located in the transition area near the semiconductor interface. These charges are a product of the oxide formation mechanism (ie. in SiO_2/Si the ionic Si leftover at interface) and are independent of oxide thickness, substrate doping type, or doping concentration. Interface trap charges exist at the oxide/semiconductor interface and are caused by defects at the interface such as dangling bonds from the sudden termination of semiconductor crystal lattice. These traps can exchange mobile carriers with the semiconductor substrate, acting as donors or acceptors³.



1. Mobile ionic charge
2. Oxide trapped charge
3. Oxide fixed charge
4. Interface trap charge

Figure 2.6: Types of fixed charge that can negatively affect the electrical properties of MOSFETs

2.4.1 Interface Charge Affect on Threshold Voltage

All of these oxides charges will induce opposite charges within the semiconductor so that at equilibrium ($V=0$) the flat-band condition seen in Fig. 2.3 is no longer achieved. A potential must be applied simply to return the MOS device back to flat-band condition. In essence this shifts the entire C-V curve the amount needed to overcome the oxide charges. As was discussed above, the threshold voltage affects the saturation current and defines the region of strong inversion. The additional oxide charges must be included when calculating the threshold voltage as shown in the expression ⁴,

$$V_T = \Phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2\varphi_F \quad (2.7)$$

where Φ_{MS} is the work function potential difference between the gate metal and semiconductor, and Q_i and Q_d are the interface and depletion charges, respectively. The first two terms arise due to real surfaces created by the metal gate and the oxide charges discussed above and can be adjusted with choice of gate electrodes, fabrication techniques, and oxide material and thickness. Eq. 2.7 can be used for either n-type or p-type substrates. While this equation predicts negative threshold voltages for typical p-channel (n-type substrates) devices, n-channel (p-type substrates) devices may have either a positive or negative threshold. A negative threshold in an n-MOSFET means that a channel exists at zero bias and the device is a depletion-mode device. Thus, a positive voltage would indicate an enhancement-mode device. I-V or C-V curves can be used to determine the threshold voltage and verify the mode of operation and illustrate the oxide charges affect on threshold voltage shifts.

2.4.2 Interface Charge Affect on I-V Characteristics

Unlike ideal oxides, real oxides have some leakage current that passes from the channel to the gate and varies with voltage or electric field across the oxide. Oxides with band offsets greater than 1 eV with the semiconductor substrate should provide a sufficient barrier to thermionic excitation of carriers through the oxide layer ^{6, 7}. However, extremely thin oxides can still have leakage through the oxide via direct and Fowler-Norheim (F-N)

tunneling (Fig. 2.7). F-N tunneling is defined as tunneling that occurs through a triangle barrier into the oxide conduction band where it can drift⁸. This type of barrier can arise from large applied gate voltages across thin oxides and the tunneling current that is produced can be expressed as function of the electric field in the gate oxide⁴:

$$I_{FN} = \xi_{ox}^2 \exp\left(\frac{-B}{\xi_{ox}}\right) \quad (2.8)$$

where B is a constant of effective mass of an electron and the barrier height. As oxides become thinner for the next generation of MOSFETs, the electrons from the semiconductor can tunnel through the gate oxide without going through the conduction band. This is considered direct tunneling and occurs through a trapezoidal barrier. The transition between direct tunneling and F-N tunneling generally occurs at lower electric fields and oxide thicknesses of ~5 nm⁹. The direct tunneling current can be expressed as a function of the electrical field in the gate oxide¹⁰:

$$I_{DT} = \exp\left(\frac{-B}{\xi_{ox}}\right) \quad (2.9)$$

By using gate oxides with higher dielectric constants, thicker oxides can be used to achieve similar effective oxide thicknesses. In addition, oxides at the same thickness with a higher dielectric constant can achieve higher gate capacitances which increase the drain current.

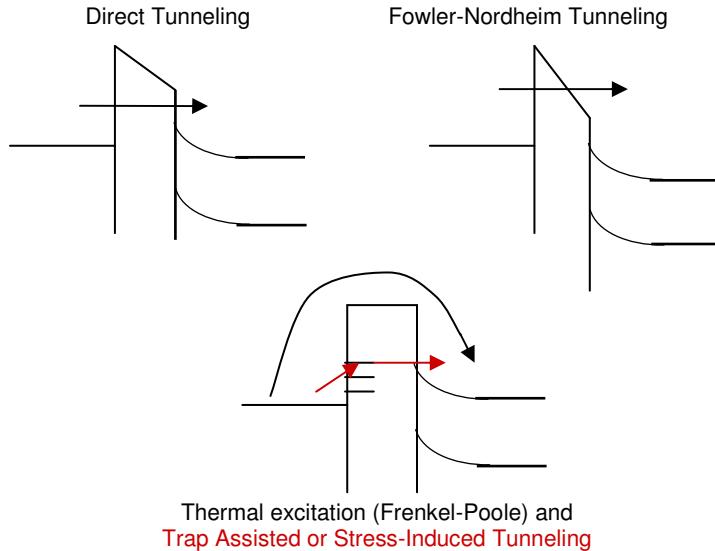


Figure 2.7: Schematic of types of leakage tunneling mechanisms.

The final type of tunneling that can occur is via defects within the oxide. If these defects are an effect of oxide deposition, radiation, and other structural defects, then this tunneling is referred to as trap-assisted tunneling (TAT). However, similar deep level traps can occur within an oxide by prolong exposure to high electric fields, which is referred to as stress-induce leakage current (SILC) ¹¹. The rate limiting step of the TAT process is the tunneling of charge carriers from the deep level traps to the oxide conduction band. Therefore, it is important to limit the number of traps available for assisting carriers through the oxide. Since the trap induced and thermal excitation leakage current are temperature dependent, one way of determining leakage current mechanisms is via temperature dependent I-V curves.

2.4.3 Interface Charges Affect on C-V Characteristics

The density of interface states or charges (D_{IT}) at the oxide/semiconductor interface can greatly affect C-V curves at varying frequencies and biases. These traps can change their charge state relatively fast in response to gate biases, moving above or below the Fermi level. Those below the Fermi level have a high probability of being occupied, while those above the Fermi level tend to be unoccupied. Therefore as the bias is changed, traps above the Fermi level give up their electrons to the semiconductor, while those below tend to trap an electron from the semiconductor. This charge storage results in a capacitance which is in parallel with the depletion capacitance and in series with the oxide capacitance. These interface traps can contribute to the low frequency capacitance (up to 1kHz) but not at extremely high frequencies (~1MHz). Therefore, the difference between the two curves in Fig. 2.5 is related to the D_{IT} following the equation ⁴

$$D_{IT} = \frac{1}{q} \left(\frac{C_{ox}C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{ox}C_{HF}}{C_{ox} - C_{HF}} \right) \quad (2.10)$$

While this method is acceptable, generally the conductance method is used to determine D_{IT} since it gives the trap density as a function of location in the band gap. This method uses plots the conductance (g_m) versus frequency for an applied gate voltage. The interface trap density can then be determined using the expression ¹²

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \text{ where } D_{it} = \frac{2G_p}{q\omega} \quad (2.11)$$

All oxide charges will shift the C-V curve due to a shift in threshold voltage. This can be seen in a hysteresis curve where the forward and reverse bias capacitance is not the same. Temperature C-V curves can determine the impact of mobile ion charges by activating them at higher temperatures but not at lower temperatures. This will create a large hysteresis and the two threshold voltages in positive and negative biases can be used to determine the amount of charge present.⁴

$$Q_m = C_{ox}(V_{FB}^- - V_{FB}^+) \quad (2.12)$$

Therefore, both C-V and I-V characteristics are very dependent on the quality of gate oxide within MOSFET devices. This thesis will be investigating the interface between La_2O_3 or Sc_2O_3 and GaN to determine its quality as a passivation and gate dielectric for GaN-base MOSFET devices.

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3. Dielectric Selection for GaN MOSFETs

The use of gate insulators to realize GaN-based MOSFETs would provide many advantages over the commonly used Schottky gate devices. These advantages include: lower leakage currents, greater voltage swing, and improved thermal stability against reaction in the gate region ¹. In addition, the incorporation of dielectrics could increase channel charge and decrease current collapse by passivating surface state that are the major cause of the deleterious effects.

The success of GaN MOSFETs has been limited due to its lack of a good quality native oxide. However, the decrease in silicon MOSFET device dimensions has led to a need to replace the SiO_2 gate oxide with a high-k oxide in order to maintain a small gate leakage current ^{2, 3}. By replacing SiO_2 with a high dielectric constant oxide, silicon loses some of its dominance which opens the way for wide band gap semiconductors with superior material properties. A significant aspect of high-k oxides is that they are deposited oxides, not native, and in principle could be deposited on any semiconductor ⁴. There are several criteria to consider when selecting a dielectric including: (i) high dielectric constant, (ii) large band gaps that result in sufficient band offsets ($> 1 \text{ eV}$), (iii) thermal stability, and (iv) good passivation abilities as indicated by low interface trap densities ⁴⁻⁶. Rare earth oxides are of particular interest due to their combination of large dielectric constants, large bandgap, good thermal stability, and the ability to be grown epitaxially on GaN to provide additional passivation of the interface.

This chapter will focus on previous dielectric studies on GaN followed by a discussion on the benefits and potential of rare earth oxides in GaN devices. There will be a focus on La_2O_3 and Sc_2O_3 since they were the oxides investigated in this thesis.

3.1 Types of Heterojunction Band Alignments

The band alignment across the dielectric/GaN interface is of great importance since it defines the electrical properties of the devices. A potential gate oxide must have a large

conduction and valence band offset to prevent the injection of free electrons and holes. Although a significantly larger oxide band gap than the semiconductor generally results in sufficient band offsets, it is not always the case. The potential band alignments will be briefly discussed here.

When two crystalline semiconductors come in contact a heterojunction is formed. The band alignment that occurs can be classified into one of three possible configurations or types including: (i) straddling gap – “type I”, (ii) staggered gap – “type II”, and (iii) broken gap – “type III”⁷. These three band alignments are shown with electrical isolation in Fig. 3.1.

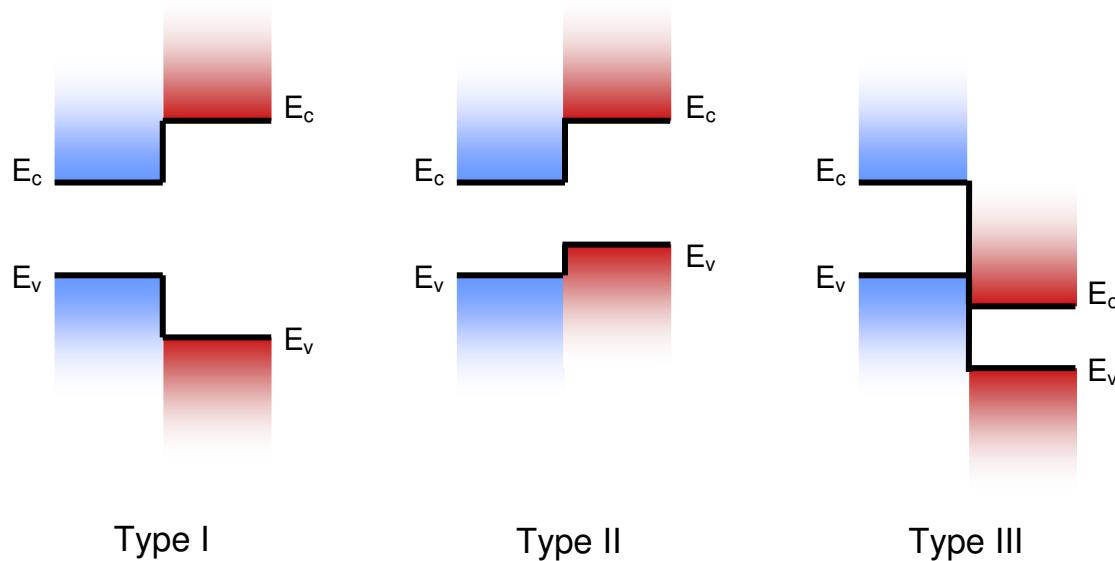


Figure 3.1: Possible heterojunction band alignments for adjacent isolated semiconductors

Direct interaction between semiconductors results in a space charge redistribution that causes band bending near the interface, which was not considered in the figure above. In the III-N family, the most common AlGaN/GaN heterojunction represents a type I band alignment. This is also the type required for a reduction in leakage current in MOSFET devices.

3.2 Previous Studies of Dielectrics on GaN

The amount of research done in this area is too vast to adequately review in this thesis. Therefore, a brief review is given for the most successful, promising, and widely used oxides.

3.2.1 Native Ga_2O_3 and Gallium Gadolinium Garnet (GGG)

Thermal oxidation of GaN surface to form Ga_2O_3 has been conducted under both dry and wet atmospheres. Dry oxidation at temperatures above 900 °C resulted in minimal polycrystalline monoclinic Ga_2O_3 layers that formed at a growth rate of 5.0 nm/h⁸. This is too slow for any viable processing step. Wet oxidation showed some improvement with a order of magnitude increase in growth rate at 900 °C. These native oxide layers were non-uniform and had a rough faceted surface. A breakdown of only 0.2 MV/cm was obtained by either of these methods⁸.

Gallium gadolinium garnet (GGG) first had success as a dielectric in GaAs MOSFETs, but has been recently incorporated in to GaN transistors. Ren et. al.⁹ deposited GGG via MBE for depletion mode MOSFETs, which showed 3 to 4 order of magnitude reduction in gate leakage compared to conventional GaN MESFET. However, the fact that it could not be modulated about 3V suggests that there is still significant leakage at the dielectric/GaN interface.

3.2.2 Amorphous SiO_2 and Si_3N_4

SiO_2 has an extremely large band gap (9.0 eV) that yield a valence and conduction band offset with GaN of 2.0 and 3.6 eV, respectively¹⁰. PECVD has been used to achieve a density of interface traps (D_{IT}) as low as $1 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ ¹¹, and Casey et al.¹² found no observable hysteresis in room temperature C-V measurements. Yet, the low dielectric constant means that high gate voltages (above 3-4V) are required to generate minority carriers. While some of the best electrical performances for GaN MOSFETs and

MOSFETs to date have been accomplished with this oxide, its deficiencies suggest the need for other dielectrics.

Amorphous Si_3N_4 , while widely used to passivate HFET surfaces, shows large flat band voltage shifts (3.07 V) and low breakdown voltages (1.5 MV/cm) in GaN MISFETs ⁸. Lee et al. ¹³ showed Si_3N_4 could produce reasonable device performance in that current saturation was achieved, but the device still exhibited a turn-on voltage of 2.7 V. The lowest D_{IT} ($5 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$) was achieved by treating the GaN surface with a N_2 plasma just prior to the dielectric deposition by electron cyclotron resonance assisted plasma chemical vapor deposition (ECR-PCVD) ¹⁴. However, it was found that Si_3N_4 had a type II band alignment with GaN, which limits its use to only as a barrier for n-channels ¹⁰. This band offset and the low dielectric constant (5) limit its viability in device structures.

3.2.3 Epitaxial Rocksalt Oxides (MgO , and CaO)

MgO and CaO offer some advantages over the previously discussed dielectrics. They have considerably higher dielectric constants (9.8 and 11.8, respectively), but still maintain large band gaps (~8 eV). In addition, a ternary oxide consisting of MgO and CaO can be lattice matched to GaN, which would prevent the formation of misfit dislocations that act as leakage paths through the oxide ¹⁵. While MgO exhibited good band valence and conduction band offsets (1.2 and 3.2 eV respectively ¹⁶), both ZnO and CaO had type II alignment with valence band offsets above GaN ¹⁷. It has been reported that MgO films on HEMTs reduced drain current collapse, as well as both forward and reverse leakage currents ¹⁸. One of the problems with these films is their instability. However, capping them with more stable oxides, like Sc_2O_3 , has been shown to limit this degradation.

3.3 Rare Earth Oxides

For distinction, the lanthanide metals are the 15 elements from lanthanum to lutetium, while the rare earth metals include the lanthanides as well as scandium and yttrium.

All rare earth elements are extremely reactive with oxygen and readily form thermally stable sesquioxides¹⁹. The rare earth ions in the oxides hold a trivalent state resulting in the general formula R_2O_3 . For the sake of this thesis, only the cubic and hexagonal phases of the rare earth oxides will be discussed, but it is worth mentioning that a metastable monoclinic phase and extremely high temperature slightly skewed hexagonal phase also exists for this system.

The rare earth oxides with smaller ionic radii (such as Sc_2O_3) crystallize in the cubic bixbyite structure containing 32 metal atoms and 48 oxygen atoms per unit cell. Fig. 3.2 shows that the bixbyite structure is related to the double-edge fluorite structure with $\frac{1}{4}$ oxygen sites vacant and regularly ordered¹⁹. All of the cations in this structure are in 6-fold coordination. Specifically for Sc_2O_3 , the cubic bixbyite structure is the stable structure up until the melting point²⁰.

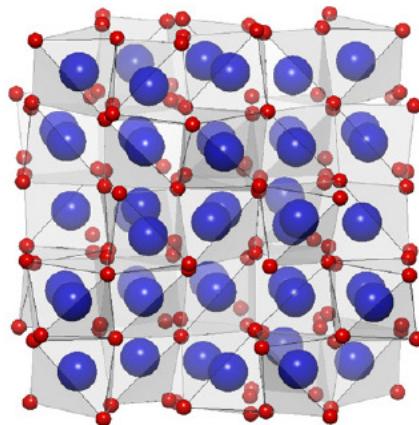


Figure 3.2: The polyhedral representation of the cubic bixbyite structure of R_2O_3 , where the large and small spheres represent the R and O atoms, respectively²⁰.

The rare earth oxides with larger ionic radii tend to crystallize in the hexagonal structure with 7-fold coordination. This means that each cation is surrounded by 7 anions, of which 4 are somewhat closer than the other 3^{19, 21}, as shown in Fig. 3.3 (a) and (b). Pauling compared the ideal close-packed octahedral layering to that observed large cations

like lanthanum resulting in the structure seen in Fig. 3.3(b). He noted that so much deformation had occurred that each cation is closer to one anion of a different layer than it is to three of the anions at the corners of the original octahedron²¹.

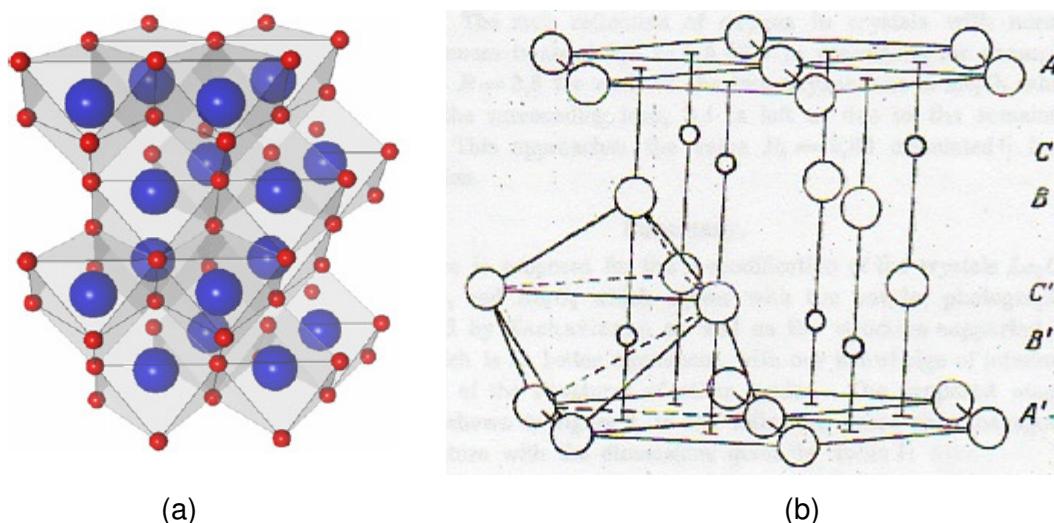


Figure 3.3: Hexagonal structure for R_2O_3 , where the large and small spheres represent the R and O atoms respectively. (a) the polyhedral representation and (b) shows the deformed octahedral close-packed stacking with 7-fold coordination ^{20, 21}.

La_2O_3 is an attractive dielectric choice due to its high- κ value (27), which is higher than HfO_2 , Sc_2O_3 (14) and any other lanthanide oxide. The dielectric constant decreases along the lanthanide series due to the decrease in metal ionic radius ². In addition, rare earth oxides exhibit band gap energies close to 6 eV, which should result in large band offsets. In the lanthanide series, a band gap maxima is realized for La, Gd, Lu suggesting that the 4f-5d transition is responsible for the band gap characteristics ¹⁹. Adachi et. al. ¹⁹ also reported that the position of the 4f level is more important for stability than the 5d level. For La_2O_3 , the 4f level is empty and therefore exists at a much higher level compared to the bottom of the 5d band. This results in good stability and a large band gap (6.2 eV).

Previous reports for Sc_2O_3 conduction band offsets with GaN were ~ 2 eV ^{1, 22, 23}. These numbers correlate well with those determined theoretically by Robertson and Falabretti ⁴. Fig. 3.2 shows their calculated band offsets for potential dielectrics with GaN,

including La_2O_3 , using the charge neutrality level model (CNL). Roberston attributed the larger band gap of the rare earth oxides, as compared to ZnO_2 and HfO_2 , to the smaller metal valence which effectively reduces the oxygen states in the valence band and pushes the CNL lower in the band gap ². A lower CNL has been shown to result in higher conduction band offsets. In order to give adequately low leakage current, the band offsets must be greater than 1 eV. This will prevent thermionic emission of carriers into the oxide at high temperatures.

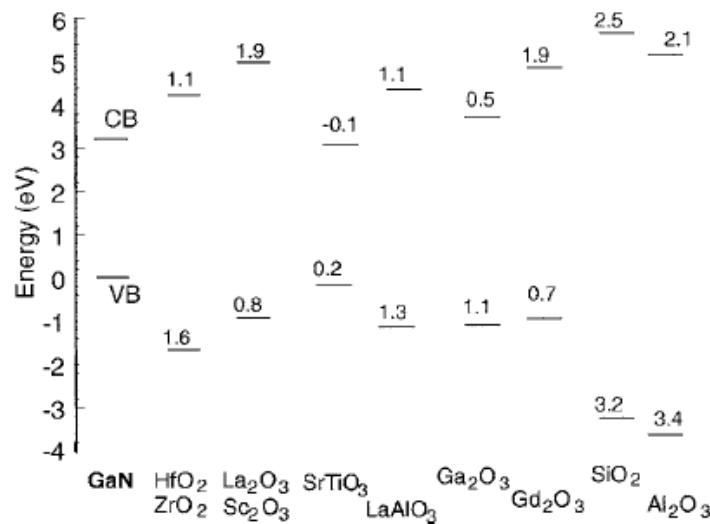


FIG. 9. Calculated band offsets of dielectrics on GaN.

Figure 3.4: Predicted band offsets of a variety of dielectrics on GaN ⁴.

It should be noted that these offsets were determined using the charge neutrality level method and specific interface bonding was not considered. Though not as important in silicon, GaN is a polar crystal which could cause larger errors using this model. Even considering the errors, this is a good prediction of the beneficial band alignments between GaN and Sc_2O_3 and La_2O_3 .

One of the biggest problems with sesquioxides is that they are hygroscopic and become hydrated and carbonated in the presence of atmospheric carbon dioxide and water at ambient temperature and pressure ¹⁹. The large ionic radius and low electronegativity of

these oxides allows $(OH)^-$ to bond easily with the rare earth atom ²⁴. Since La_2O_3 has the largest ionic radius and lowest electronegativity, it is the most hygroscopic of the rare earth oxides. Lanathum films with hydroxide contamination result in degraded density, dielectric constant, and overall electrical performance. This makes the processing of devices with these oxides extremely difficult, and may ultimately prevent their integration into GaN-based MOSFETs.

3.4 Statement of Purpose

The purpose of this work is to epitaxially deposit La_2O_3 and Sc_2O_3 on GaN to determine their potential as gate dielectrics for GaN-based MOSFETs. Theoretically predicted large band offsets, high dielectric constants, and good thermal stability all point to the viability of these oxides as passivation and insulating layers in high frequency, high temperature applications. Surface preparation is critical since the surface structure will define the subsequent layer quality and structure. Therefore, the effect of KOH and $K_2(SO_4)_2$ on the surface termination, clean, and subsequent oxide deposition will be investigated as well.

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4. Experimental Procedures

This chapter will outline the details for each of the experiments carried out in this thesis. It will be divided into four sections: (i) general details of all GaN film growth by MOCVD, (ii) surface treatment experiments to determine termination and cleaning ability of GaN prior to oxide deposition, (iii) MBE oxide deposition, and (iv) equipment and techniques used for structural and electrical characterization of La_2O_3 and Sc_2O_3 as potential gate oxides. Any variation or details specific to single samples will be included in the results discussion.

4.1 GaN Film Growth

For this thesis, all (0001) GaN films were heteroepitaxially deposited on 2" c-plane sapphire substrates in a vertical cold-walled MOCVD reactor. Films were grown using trimethylgallium, trimethylaluminum, and ammonia precursors at 1040 °C with a chamber pressure of 0.1 atm. A low temperature AlN buffer was deposited as a nucleation layer for the GaN films, which is known to facilitate the growth of Ga-face polar films¹. The quality and thickness of the buffer layer is known to have a dramatic effect on the surface morphology and dislocation density of subsequent films. Therefore, optimum AlN buffers were grown at 500 °C to a thickness of approximately 30-40 nm, which yielded GaN films with ω -rocking curve FWHM value of 0.42°. Intrinsic GaN films were determined to have a free carrier concentration of 10^{15} - 10^{16} cm⁻³, while silicon doped n-type films had carrier concentrations of 1×10^{18} cm⁻³. Details about specific GaN films used in each experiment will be discussed in Sect. 4.2 and 4.3 below.

4.2 Surface Preparation Prior to Oxide Deposition

Previous work done by Lei Ma at NCSU, showed that GaN could be etched by sequentially submersing the films in a strong oxidizing reagent, rinsing and then placing in a strong reducing reagent². His results suggested that each type of chemical preferentially etched one layer of either Ga or N atoms. Therefore, using either potassium hydroxide

(KOH) or potassium persulfate ($K_2(SO_4)_2$), GaN could be N-terminated or Ga-terminated. The experiment presented here looks at the effect of these chemical etches on the surface chemistry and ability to passivate the GaN surface in electrical devices.

This study used 0.5 μm thick n-type GaN (0001) films with Si doping concentrations of $1 \times 10^{18} \text{ cm}^{-3}$. Samples were saw-cut into 16 mm squares and solvent cleaned with trichloroethylene, acetone, and methanol. Since MOCVD grown films are not completely uniform, variation was minimized by using samples taken from one wafer. The resulting quarter wafers were dipped in either 5% hydrofluoric acid (HF), 50% aqueous KOH solution, or 5% $K_2(SO_4)_2$ solution for 30 seconds and rinsed in DI water for 30 seconds. All samples were blown dry with high purity nitrogen gas. Samples were then immediately transferred into the x-ray photoelectron spectroscopy (XPS) chamber to minimize the atmospheric exposure time. Surfaces were then analyzed by XPS to determine the termination and contamination cleaning ability of each chemical etch.

To determine the passivation ability of the acid surface treatment, GaN metal insulator semiconductor field effect transistors (MISFETs) were fabricated in a split experiment: one wafer with $K_2(SO_4)_2$ treatment before silicon nitride (Si_3N_4) deposition and one without acid treatment before deposition. All other processing steps were identical for both wafers. Si_3N_4 was deposited via PECVD at 300 °C with a thickness of 60nm. Titanium (15nm) / Aluminum (65nm) / Nickel (35nm) / Gold (50nm) ohmic contacts were deposited using electron beam deposition and lift-off. Ohmic contacts were subsequently annealed at 850 °C for 60 seconds. Following rapid thermal annealing at 750 °C for 40 seconds, a typical specific contact resistance of $10^{-5} / \text{ohm}\cdot\text{cm}^2$ has been measured in independent experiments. Similarly, Nickel (100nm) / Gold (100nm) gate contacts were fabricated with a 50 μm gate length. A cross-sectional schematic of these devices can be seen in Fig. 4.1 below.

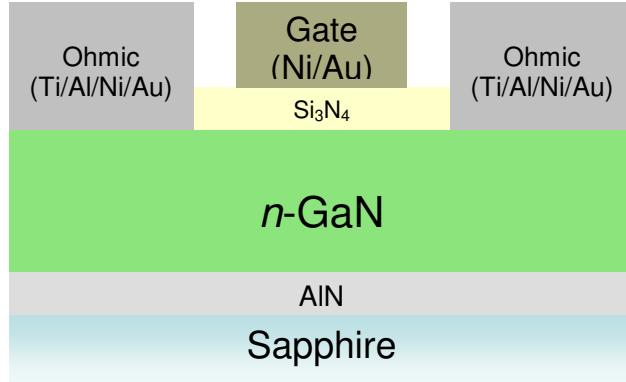


Figure 4.1: Cross-sectional schematic for MISFETs prepared with and without acid pretreatment for determination of passivation ability³.

4.3 Oxide Deposition

Rare earth oxide deposition was carried out on 16 mm square samples with 1 μm intrinsic (0001) GaN films. Prior to oxide deposition, the GaN surface was treated with a $\text{K}_2(\text{SO}_4)_2$ acid solution (as described in Sect. 4.2) to yield a cleaned Ga-terminated surface. Samples were transferred immediately into the MBE chamber to limit the amount of atmospheric exposure to the surface. La_2O_3 and Sc_2O_3 films of varying thicknesses (15-350 \AA) were deposited by thermal evaporation of elemental high purity La (1700 °C) and Sc (1245 °C) in an ultra-high vacuum SVT Associates MBE system ($P_{\text{background}} = 5 \times 10^{-10}$ Torr)^{4,5}. During deposition the substrate temperature was 400-500 °C for all growths. Ultra-high oxygen was delivered to the growth chamber to assist oxide formation at a pressure of 5×10^{-7} Torr. Using a quartz crystal monitor, the deposition rates under these growth condition was determine to be 1.4 $\text{\AA}/\text{min}$. and 3.5 $\text{\AA}/\text{min}$ for La_2O_3 and Sc_2O_3 , respectively. After growth of the oxide, the substrate was cooled under the oxygen flux, which was removed when the substrate temperature reached 200 °C. Since La_2O_3 is known to have a propensity for hydroxide formation, an *in-situ* cap of either tantalum or amorphous silicon was deposited after oxide growth to prevent water and carbon monoxide contamination⁶⁻⁸.

Epitaxial quality was monitored during the deposition of each oxide by *in-situ* RHEED. XPS was used after oxide growth to determine the surface chemistry and band offsets with GaN for both La_2O_3 and Sc_2O_3 , while *ex-situ* crystal quality and structural

analysis was performed with XRD and TEM. In order to study the oxide potential as gate oxides in GaN-base FETs, MOS capacitors were formed and electrically tested. The structural and electrical characterization techniques employed will be discussed in detail in Sect. 4.4.

4.4 Structural and Electrical Characterization Equipment and Techniques

A variety of characterization techniques were used to analyze the structural and electrical properties of oxide films deposited on GaN substrates. The conditions and equipment for each technique will be briefly explored here with more details provided in subsequent chapters when needed.

4.4.1 Reflection High Energy Electron Diffraction (RHEED)

A RHEED system is incorporated directly into the MBE chamber, allowing *in-situ* examination of the GaN surface prior to oxide growth and real-time analysis during growth. An electron gun operated at an acceleration voltage of 8 kV, filament current of 2.2 mA, and an emission current of 2.1-2.3 mA was used to characterize all films. Beams diffracted across the sample surface are imaged with a phosphor screen, and digitally captured with a k-Space acquisition system (kSA 400). The extremely low angle of the incident beam allows for good surface sensitivity but little knowledge about the bulk structure of the deposited films.

4.4.2 X-Ray Diffraction (XRD)

Epitaxial quality and phase determination was completed for GaN substrates, La₂O₃ films with varying thicknesses, and a 350 Å Sc₂O₃ film on two different XRD systems. Initially, high resolution θ -2 θ (5-75° scans) and ω -rocking curve spectra were collected using a Philips X'Pert PRO MRD HR x-ray diffraction system housed in the Shared Materials Instrumentation Facility (SMiF) at Duke University. A Cu K α (1.5405 Å) x-ray source operated at 45 kV/40 mA was used with an x-ray mirror to create a monochromatic parallel

beam. Measurements were collected with a parallel plate collimator containing 0.4 rad. soller slits, which yielded a resolution of 0.27 °. The peak positions and full-width at half maximum (FWHM) were recorded using the X'Pert software for each sample and compared with JCPDF files to determine the phases present. The in-plane lattice parameter was calculated based on Bragg's law,

$$n\lambda = 2d \sin \theta \quad (4.1)$$

where n is an integer determined by the order given (usually n=1), λ is the wavelength of the copper source x-rays, d is the spacing between the planes in the atomic lattice, and θ is the angle between the incident x-ray and the scattering planes (Fig. 4.2). The d-spacing is then related to the in-plane lattice parameter (a) by,

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \quad (4.2)$$

where h, k, and l are the Miller indices of the Bragg plane.

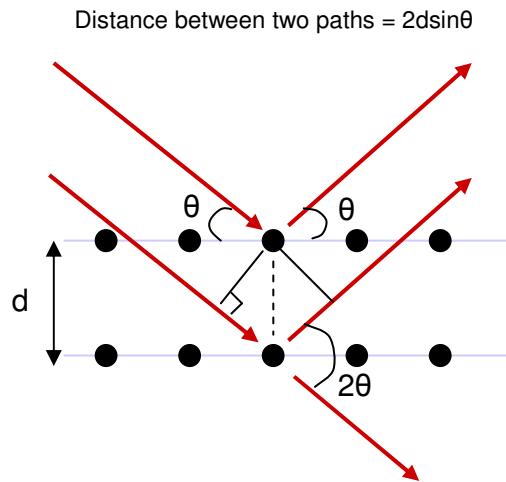


Figure 4.2: Schematic showing the Bragg's law derivation to determine the d-spacing between planes by XRD.

For the rare earth oxide films, further analysis was done with a Bruker AXS D-5000 XRD system equipped with a High-Star area detector ¹. The area detector has a better signal to noise ratio than the Philips system, allowing for better analysis of the thin oxide film. This setup also uses a Cu K α (1.5405 Å) source operated at 40 kV/30 mA. The Bruker system contains a single, front-end monochromator with a 0.8 mm aperture collimator tube.

In the normal setup, the area detector can collect a range of approximately 30° in 2θ . Therefore, full θ - 2θ spectra can be collected at a fixed ω value aligned to the film's on-axis reflection. Since the area detector collects a range of data, the spots representing the 2θ peaks can also be integrated to yield chi spectra. More detail about the XRD setup can be found in Mark Losego's thesis ¹.

The Bruker XRD system was used to determine oxide crystal symmetry by scanning along the phi axis. Fig. 4.3 shows the different XRD axes. Samples are tilted in chi, to bring an off-axis plane into alignment with the detector, which is then rotated about the phi axis. This will allow the planes to come in and out of phase with the detector based on the symmetry of the crystal. The angle separating the peaks will indicate the crystal symmetry of the sample.

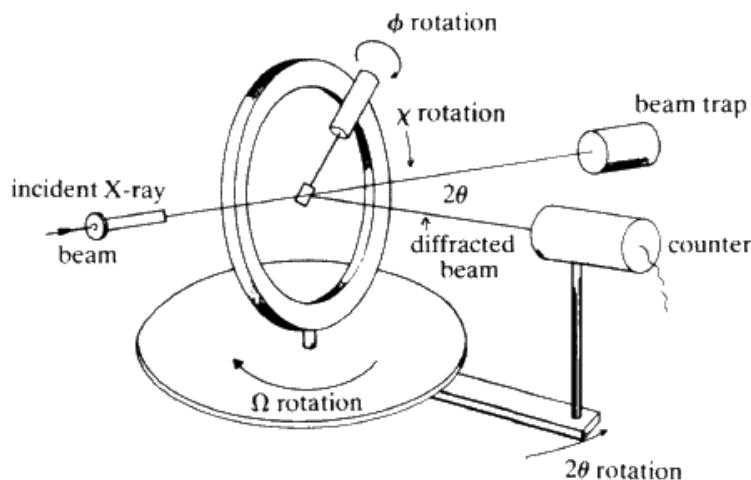


Figure 4.3: Schematic of four circle diffractometer with the 4 angles between the incident beam, sample and detector (ω , χ , ϕ , 2θ) are labeled ⁹.

4.4.3 Transmission Electron Microscopy (TEM)

TEM samples of 300 \AA La_2O_3 and 350 \AA Sc_2O_3 films on GaN were prepared with a FEI Quanta 200 3D focused ion beam (FIB) at NCSU's Analytical Instrumentation Facility (AIF). Both films were capped with a 600 \AA amorphous silicon layer to prevent hydroxide formation in the La_2O_3 and to compare equally deposited oxide structures. Samples were

milled with a gallium liquid metal ion source. TEM images were collected under bright field conditions using AIF's Hitachi HF2000 cold field emission TEM. This particular microscope is capable of achieving 0.2 nm point resolution. Images were collected at both low and high magnifications (10kx-700kx) with an acceleration voltage of 200kV. The best contrast and lattice imaging was achieved by tilting to the nearest zone axis using a double-axis sample holder. In order to explicitly define the layers present, the Oxford Link INCA EDS system was used in conjunction with the TEM images. The EDS spectrums were collected for 120 seconds with a 1nm point resolution.

4.4.4 X-Ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) surface chemistry analysis of the surface-treated GaN and oxide films was performed using a Riber LAS3000 analytical system equipped with a two-stage cylindrical mirror-style analyzer. Spectra were acquired with a Mg K α (1253.6 eV) non-monochromatic x-ray source, with a spot size of 2-3 mm, and take off angle of 75° from surface. The Mg source was chosen over an Al source to prevent the overlap of Ga Auger peaks with the O1s and N1s photoelectron peaks.

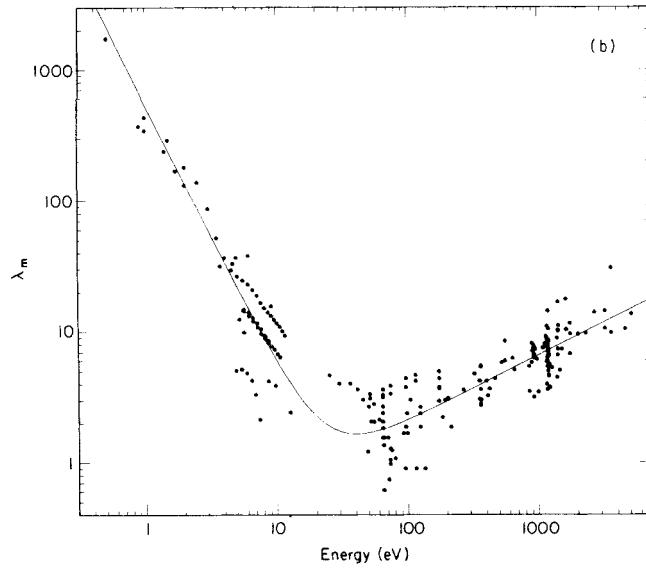


Figure 4.4: Universal inelastic mean free path curve for escape depth in all materials. As can be seen the escape depth for XPS (12kV) is between 1-5 nm ¹⁰.

The surface sensitivity of XPS results from the limited escape depth (or inelastic mean free path – IMFP) for non-scattered electrons. All samples have an IMFP of approximately $3\lambda\sin\theta$ or about 1-5 nm as shown in Fig. 4.4. To account for sample charging induced energy offset in the instrument, each spectrum was calibrated by assigning the C-1s binding energy to a value of 285.0 eV.

Lower resolution (~2 eV) survey scans were collected from 1200-0 eV for all samples. Non-scattered electrons emitted by the photoelectron effect have a materials characteristic kinetic energy associated with them. While kinetic energies are detected, most XPS spectra are presented in terms of binding energies. The relationship between the two is,

$$KE = h\nu - BE - \phi_s \quad (4.3)$$

where $h\nu$ is the energy of the photon, BE is the binding energy of the atomic orbital from which the electron originates, and ϕ_s is the spectrometer work function. From the survey spectra, molar ratios are determined by the equation ¹¹,

$$X_n = \frac{\frac{I_n}{S_n}}{\sum \frac{I_j}{S_j}} \quad (4.4)$$

where n is the chemical species of interest, I is the integrated peak intensity, S is the atomic sensitivity factor, and the summation in the denominator is for all chemical species being compared. Atomic ratios between two chemical species can then be calculated using the expression,

$$\frac{n_1}{n_2} = \frac{\frac{I_1}{S_1}}{\frac{I_2}{S_2}} \quad (4.5)$$

High resolution scans were performed on peaks of interest for all samples. Chemical bonding states were determined using the CASA XPS peak fitting software. Restraints for the fittings included a max FWHM determined from the FWHM of the C-1s alignment peak and a Shirley background subtraction was used for all peak fitting.

XPS was utilized to determine the presence of surface band bending resulting from chemical surface treatments prior to oxide deposition. The amount of band pinning present at the surface of GaN samples treated with various surface cleans was determined using the technique laid out by Chambers et. al ¹². Valence band maximums (VBMs) values were obtained from the intersection of the linearly fitted leading valence band edge and the background. By definition the Fermi level corresponds to zero binding energy ¹¹. Therefore, the intersection value defining the VBM lies much below the Fermi level. The amount of band bending (Δ) can then be obtained with the expression,

$$\Delta = E_g - VBM . \quad (4.6)$$

A positive value resulting from this equation represents upward band bending, while a negative value indicates downward band bending.

Band offsets were determined using the method developed by Waldrop, Grant and Kraut in the late 1970's ¹³. XPS provides sufficient resolution and energy needed to excite core-level electrons to achieve complete band alignment measurements with good accuracy (± 0.1 eV) ¹⁴. Three samples are needed to discern the band discontinuities with this method: (i) bulk substrate (GaN) sample, (ii) thick oxide film (> 50 Å) which contains no signal from underlying substrate, and (iii) thin oxide film (< 50 Å) that exhibits signals from both layers. By referencing a core-level to the VBM in the first two samples, and finding the difference between these core-levels in the third sample, the valence band offset (VBO) can be determined using the following equation,

$$VBO = (E_{core}^{oxide} - E_{core}^{GaN})_{oxide/GaN} - (E_{core} - E_v)_{oxide} + (E_{core} - E_v)_{GaN} \quad (4.7)$$

where E_v is the valence band maximum. Since XPS is unable to probe states above the Fermi level, the conduction band offset (CBO) cannot be determined independently. Therefore, the CBO is determined using the relation,

$$CBO = E_g^{oxide} - E_g^{GaN} - VBO . \quad (4.8)$$

Band alignment between two materials is the crucial parameter in predicting the electronic behavior across a device interface.

4.4.5 MOS capacitor fabrication and device testing (C-V, I-V experiments)

Simple metal-oxide-semiconductor (MOS) gate stacks were fabricated with 50 and 100 Å oxides. Platinum was deposited as the gate electrode, while Indium was used as the ohmic contact to the *n*-type GaN substrate (Fig. 4.5).

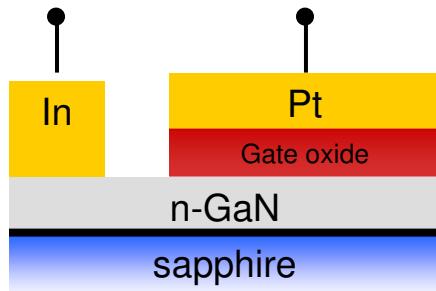


Figure 4.5: Cross-sectional schematic of fabricated MOS capacitors use to test the potential of La_2O_3 and Sc_2O_3 as gate oxides.

An Agilent 4248 and 4155C meter was used to collect capacitance-voltage (C-V) and current-voltage data (I-V), respectively. C-V measurements were collected at frequencies from 50 kHz to 1 MHz for all samples. To correct for high series resistance and leakage due to such a thin oxide, C-V curves were corrected using the three-element model (more details in Section 7.1). Rare earth oxide leakage currents were compared with the more common Si_3N_4 (600 Å) dielectric deposited by PECVD with a fabricated structure shown in Fig. 4.1.

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5. Surface Treatments of GaN

GaN has been discussed as a semiconductor material which is advantageous for high-power, high-frequency, and high temperature device applications such as metal-oxide-semiconductor field effect transistors (MOSFETs). Reproducibility of device fabrication processes and reliability of device operation are essential in realizing the full potential of these GaN-base devices. A critical step in device fabrication is surface cleaning, since the resulting structure has significant influence on surface energy states, epitaxial defects, metal contact resistance, passivation of the channel and overall semiconductor device quality¹. In MOSFETs, a clean smooth surface prior to gate dielectric deposition is necessary since incorporation of impurities and introduction of interface states lead to degradation of device properties such as threshold voltage, breakdown voltage, leakage current, and peak mobility²⁻³. Dry etching methods, such as plasma etching, have shown success at removing contaminants; however, they are known for introducing damage to the surface making the material electrically unsuitable for reliable devices⁴⁻⁵. Chemical wet etches are a typical way of achieving clean GaN surfaces with a low degree of surface damage as needed for semiconductor device fabrication. However, many wet etches are followed by a high temperature anneal or desorption step that can introduce defect sites without removing all of the contaminants on the surface¹.

Along with surface chemistry, electronic structure of a film's surface is important to consider when developing a cleaning procedure. The removal or addition of charge in the valence band following a change in bonding state, like through oxidation, can alter the electron shielding and change the surface Fermi level band bending⁶. In order to accurately predict heterojunction band offsets or Schottky barrier heights, the changes in band bending due to surface cleaning must be taken into account³. Therefore, the criteria for surface cleanliness must consider the entire electrical, structural, and physical state of the surface¹.

The study presented in this chapter focuses on enhanced understanding of simple acidic and basic chemical etches, without annealing, to passivate, clean, and provide a reproducible GaN surface prior to dielectric and metal deposition. X-ray photoelectron

spectroscopy (XPS) is used to analyze the effects of potassium persulfate ($K_2(SO_4)_2$) and potassium hydroxide (KOH) wet etches on GaN surface termination, chemistry and subsequent oxide formation. Initial I-V electrical data is provided to support the effectiveness of the chemical etching step.

5.1 Results and Discussion

5.1.1 XPS Surface Chemistry Analysis

The effects of the acid ($K_2(SO_4)_2$) and base (KOH) chemical surface treatments on the location of the Ga 3d peak are shown in Fig. 5.1 below. The as-grown sample shows a spectral peak position of 19.7 eV, which is consistent with previous findings for GaN^{1,7}.

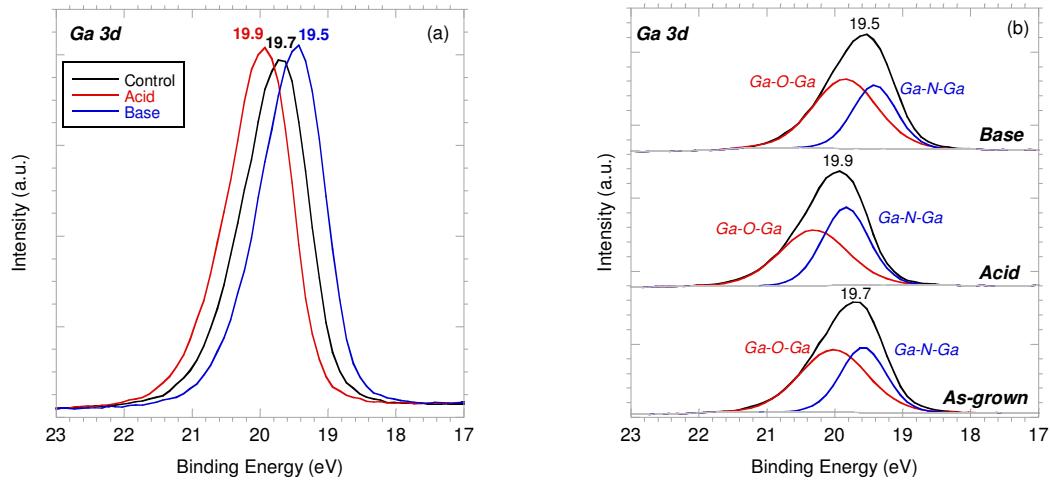


Figure 5.1: The effects of the acid and base surface treatments on (a) the shift in the Ga 3d peak and (b) the amount of Ga-O and Ga-N bonding present in the Ga 3d peak.

With the acid treatment, this peak shifts towards higher binding energies suggesting the existence of Ga-terminated surface that would produce more Ga-O bonding. Conversely, the base treated sample shifts to a lower binding energy suggesting the presence of an N-terminated face which would yield less Ga-O bonding. The termination predictions were further verified by calculating the ratios of the Ga-O:Ga-N bonding using the deconvoluted

integrated peak areas as shown in Fig. 5.1(b). The as-grown, base and acid treated samples had ratios of 1.4, 1.0, and 1.6, respectively. The full-width-at-half maximums (FWHM) for the Ga-O peaks and the Ga-N peaks are 1.1 and 0.8. The broader Ga-O peak is due to variation in stoichiometry and structural quality known to exist with this state⁷.

Fig. 5.2 shows the affect of $K_2(SO_4)_2$ and KOH on oxidation of the GaN surface. Previous works have shown that hydrofluoric acid (HF) is effective at removing carbon and oxygen from the surface without leaving fluorine residues^{1, 8}. Therefore, a HF treatment followed by atmospheric exposure for more than 48 hours was used to determine the binding energy of the native equilibrium oxide. This resulted in a low intensity single peak at an energy of 532.1 eV, correlating with previous findings for stoichiometric β - Ga_2O_3 GaN^{3,9-10}. Monoclinic β - Ga_2O_3 is well-known as the stable native oxide of GaN^{7, 11-13}.

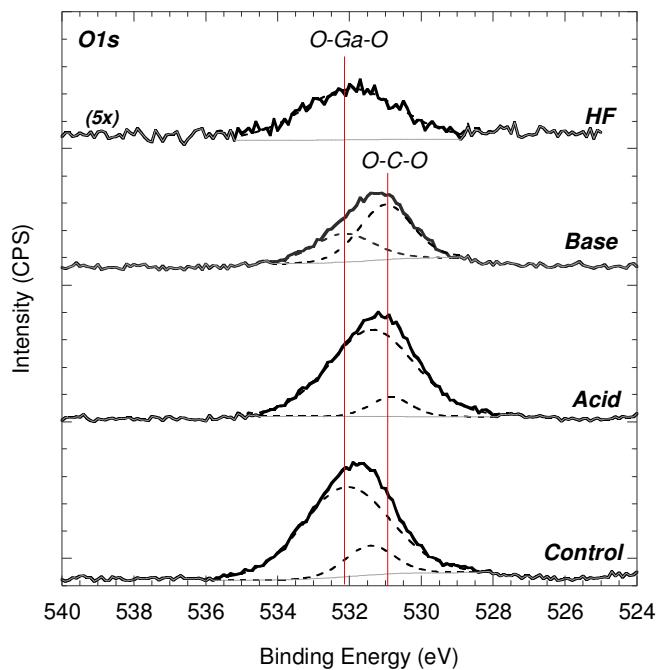


Figure 5.2: O1s peak comparing different GaN surface treatments. The HF, as-grown, and base samples all except the stable native oxide β - Ga_2O_3 , but the acid sample exhibits a shift in binding energy due to a composition change in the oxide.

The peak in the acid and base samples at 530.9 eV and the peak in the as-grown sample at 531.1 eV have been attributed to carboxides based on differences in electronegativities. This is supported by the lack of a C-O peak for clean GaN surface following the HF dip

The as-grown and base treated samples exhibit the native Ga_2O_3 peak at 532.1 eV, but the acid treated sample shows an apparent shift in this peak to a lower binding energy of 531.4 eV attributed to a change in Ga-O bond configuration or stoichiometry. It is proposed that the acid treatment strips the stable native Ga_2O_3 oxide and etches the surface such that the gallium surface concentration higher. This gallium-rich surface subsequently forms a metastable nonstoichiometric oxide (GaO_x). Multiple oxidation states within the Ga-O feature have been observed in GaAs, and have been related to Ga_2O , GaO_2 , and Ga suboxides¹⁴. Diale et. al.¹⁵ showed that heating between 40-500°C greatly reduces the oxygen concentration on the surface while increasing the carbon concentration. Since epitaxial oxides used in this thesis will be deposited within this range, it is important to remove as much carbon as possible prior to deposition. From Fig. 5.2 this would indicate that the acid treatment would be most effective prior to oxide deposition.

Table I summarizes the affect of different treatments on the amount of Ga and N present at the surface as determined by XPS using their atomic sensitivity factors (N1s = 0.42, O1s = 0.78, and $\text{Ga}2\text{p}^{3/2} = 3.34$)^{11, 16}. Previous *in situ* studies by Munkholm et. al.¹⁷ showed that MOCVD prepared GaN resulted in (1x1) surface termination. Smith et. al.¹⁸ and Feenstra et. al.¹⁹ theoretically showed that the ideal (1x1) surface is unstable for GaN, and is immediately stabilized by surface adsorbents, vacancies, or by faceting. Based on their findings, it is likely that the (1x1) surface is stabilized by adsorbents that remain after the MOCVD growth process. In our growth process, an overpressure of ammonia remains flowing after the removal of the gallium precursors and throughout the sample cool down. Therefore, the surface is most likely stabilized by a layer of absorbed N leading to the nonstoichiometric ratios presented in Table I.

Table I: Area ratios of N/Ga and O/Ga for different chemical treatments

Sample	Ga/N ratio	Ga/O ratio	O/N ratio
As grown	0.30 ± 0.01	0.66 ± 0.1	0.45 ± 0.05
$\text{K}_2(\text{SO}_4)$	0.39 ± 0.02	0.86 ± 0.3	0.46 ± 0.03
KOH	0.34 ± 0.04	0.89 ± 0.2	0.38 ± 0.02

The KOH etch greatly reduces the O/N ratio indicating that the native oxide is removed leaving a more nitrogen rich surface. The removal of surface oxide is expected since it is well known that gallium oxide can be dissolved in alkali solutions ²⁰. Though gallium is still detected, it is more bound to nitrogen atoms than oxygen atoms as verified by the reduction of Ga_2O_3 in the O1s peak and the shift in towards Ga-N bonding in the Ga 3d peak. Dongsheng et.al. ²⁰ indicated that the hydroxide ions in the KOH solution cannot attack the N-terminated surface because of the large repulsion between OH^- and three occupied dangling bonds of nitrogen. Therefore, the +c surface becomes resistant to etching in KOH once the first layer of gallium and oxygen atoms is removed. This self-termination could explain the results in Fig. 5.1 and Table I. In addition, King et. al. ¹ proposed that the ionic bonding within GaN can lead the formation of strong bonds with adventitious carbon especially for nitrided surfaces. This could account for the much larger carboxide peak for the base treated sample with nitrogen-rich surfaces.

A gallium-rich surface is created by the $\text{K}_2(\text{SO}_4)_2$ treatment. A Ga-rich surface is more likely to bond with oxygen explaining the increase in both the Ga/N and the O/N ratios. This is verified by the large amounts of GaO_x found in the O1s peak and the shift towards Ga-O bonding in the Ga 3d peak. Therefore, these two simple chemical etches provide a way to control the GaN surface chemistry and oxide formation prior to dielectric deposition.

5.1.2 XPS Analysis of Surface Band Bending

Chamber's method of linear extrapolation²¹ was used to determine the valence band maximum (VBM) for both HF and $\text{K}_2(\text{SO}_4)_2$ treated GaN (Fig. 5.3). The samples throughout this experiment were *n*-type GaN with a doping of $1 \times 10^{18} \text{ cm}^{-3}$, making E_F approximately 0.08 eV below the conduction band minimum at room temperature. For HF treated samples,

the VBM was determined to be 2.7 ± 0.1 eV below the Fermi level indicating 0.6 eV upward band bending. This value is in agreement with many other papers reporting the VBM for atomically clean GaN^{11, 13, 22}. The VBM turn-on was verified since the Ga 3d peak lays 17.6 eV below the VBM, which is consistent with Grant and Waldrop studies²³.

The Ga-face of GaN (0001) is a polar surface that through spontaneous polarization will lead to negative bound charge at the film surface. These effects can lead to upward band bending due to polarization bound charge screened by ionized donors^{3, 9}. This suggests that even a perfectly cleaned surface would have some band bending present.

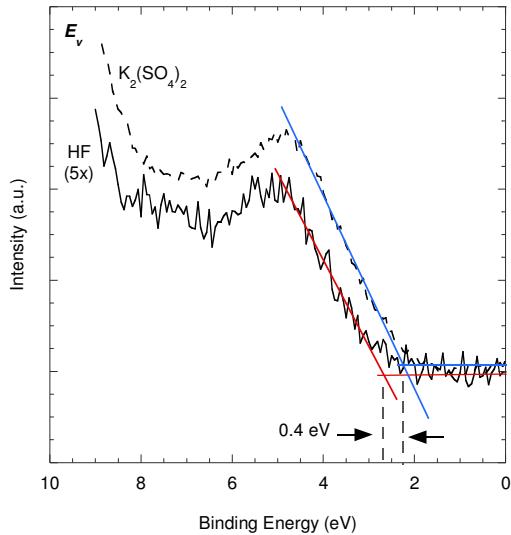


Figure 5.3: Linear extrapolation of the VBM for HF was at 2.7 ± 0.1 eV and for $K_2(SO_4)_2$ at 2.3 ± 0.1 eV leading to an increase in upward band bending of 0.4 eV.

After the acid treatment, the VBM was determined to be 2.3 ± 0.1 eV below the Fermi level resulting in an additional 0.4 eV of upward band bending due to the surface treatment. This is consistent with Wu et. al. ²² observations for exposed GaN surfaces. Fermi band pinning can be a result of oxide formation, dislocation densities, surface strain, and other surface contaminates. However, Fig. 5.2 shows a significant oxide layer is created due to the acid treatment, compared to the HF surface, which is most likely the origin of the addition pinning. Fig. 5.4 shows the proposed band diagram post surface treatment and prior to gate dielectric deposition.

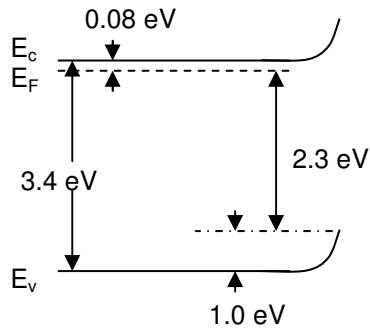


Figure 5.4: Schematic of band bending in n-type GaN after $K_2(SO_4)_2$ treatment

5.1.3 I-V Characteristics for Surface Treatments

The nonstoichiometric gallium oxide formation with the acid treatment could be utilized to facilitate surface passivation of the channel under the gate in GaN FETs. To study this effect, metal-insulator-semiconductor (MIS) test structures were fabricate using Si_3N_4 as the gate dielectric. Presumably, an improvement in surface preparation would lead to a reduction in leakage current. Fig. 5.5 (a) shows an order of magnitude improvement in leakage current for dielectrics deposited following the $K_2(SO_4)_2$ pretreatment. The reduction in leakage current is attributed to the acid pretreatment creating a thin GaO_x buffer layer that passivates the surface while still allowing or even promoting quality deposition of dielectric films. The acid treated samples also exhibit increased source-to-drain current, increased subthreshold slope, increased peak transconductance, and better pinch-off as shown in Fig. 5.5 (b)-(d). This indicates the usefulness in the pretreatment prior to dielectric deposition to improve reliability and performance of GaN FET devices.

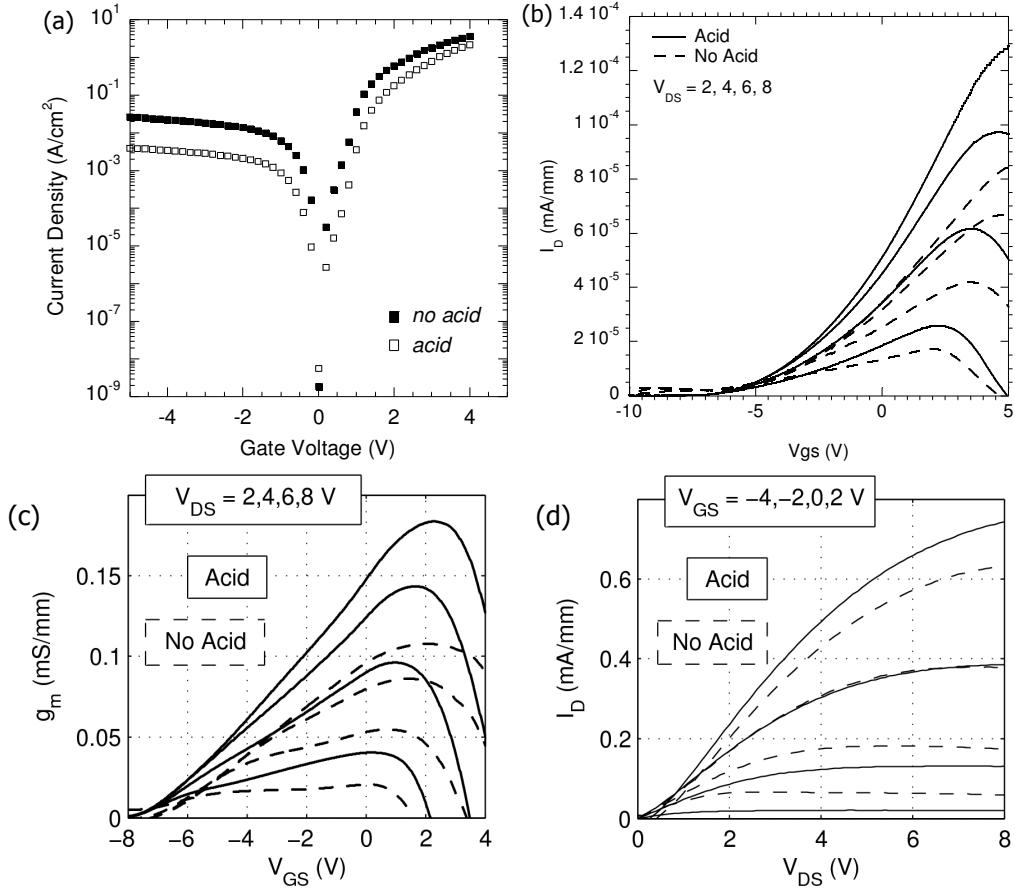


Figure 5.5 (a)-(d): I-V data for MISFETs prepared with and without the $K_2(SO_4)_2$ pretreatment prior to dielectric deposition to show the impact of this GaO_x passivation layer created.

5.1.4 C-V Characteristics for Surface Treatments

In the following chapters Sc_2O_3 and La_2O_3 will be explored as gate dielectrics. Therefore, Sc_2O_3/n -GaN MOS structures with 50-200 μm guard rings were fabricated with Sc_2O_3 thicknesses of 50 and 100 \AA , both with and without the acid pretreatment. Ti/Al and Ni/Au metals were used for the ohmic and gate contacts, respectively. Fig. 5.6 shows that the sample with the $K_2(SO_4)_2$ clean exhibits better C-V characteristics as compared to those without the pretreatment. The large hysteresis observed for the samples without the pretreatment is indicative of a high density of interface states (D_{IT}). The hysteresis window at the flat band voltage is reduced from 1.1 V to 0.3 V with the $K_2(SO_4)_2$ treatment.

Therefore, it is believed that the GaO_x layer formed by the surface treatment passivates the interface resulting in a reduced D_{IT} .

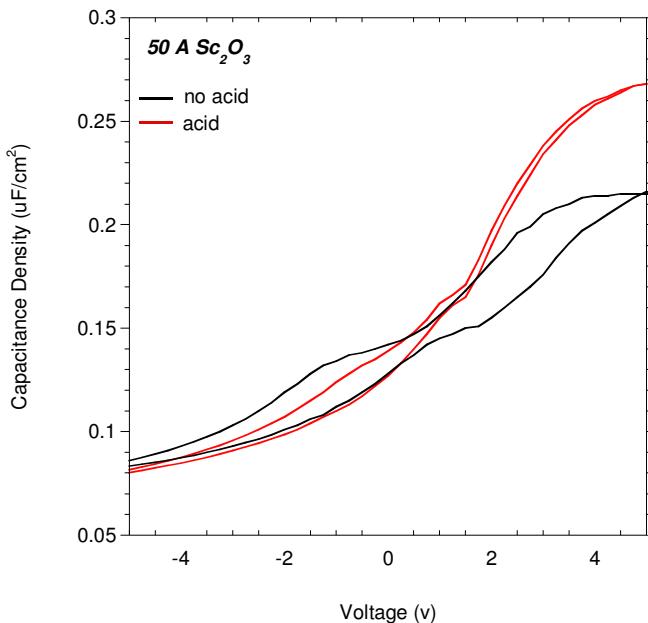


Figure 5.6: C-V data for n-GaN MOS capacitors with 50 Å Sc_2O_3 both with and without the acid pretreatment

5.2 Conclusions

Simple room temperature $\text{K}_2(\text{SO}_4)_2$ and KOH etches were investigated as possible processes for cleaning and passivating the GaN surface in FET devices. The basic treatment left a nitrogen-rich surface that limited oxidation and retained other contaminants making it a poor choice for device fabrication. The acidic treatment produced a gallium-rich interface that allowed for subsequent oxidation while reducing other contaminants at the surface. A shift in oxygen binding energy was observed after the $\text{K}_2(\text{SO}_4)_2$ etch that correlated with the replacement of stoichiometric Ga_2O_3 with a nonstoichiometric GaO_x oxide. The formation of this new oxide acts as a passivating layer prior to dielectric deposition, which resulted in an order of magnitude reduction in leakage current, a reduced hysteresis window, and an overall improvement in device performance. However, the acid treatment produced an additional 0.4 eV of upward band bending prior to dielectric

deposition. While this does not appear to negatively affect device performance, it needs to be considered when looking at heterojunction band offsets in MOS devices.

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6. Structural Characterization of Sc_2O_3 and La_2O_3 on GaN

GaN-based MOSFETs provide several advantages over metal-gated high electron mobility transistors (HEMTs) including lower leakage currents, greater voltage swings, lower power consumption, and improved thermal stability within the gate region ^{1, 2}. Dielectrics can also effectively passivate surface states, which are a major cause of current collapse in HEMTs ². Previously, the limiting factor in GaN FETs has been the poor quality of their native oxides, which can leave their Fermi level pinned ³. Yet, recent advances in deposition of high- κ oxides in silicon technology provide a pathway for the realization of similar devices on semiconductors with high electron mobilities and wider band gaps.

Achieving the full potential of GaN MOSFETs requires a dielectric oxide which exhibits low gate leakage, low interface trap density, and a high breakdown voltage when deposited on GaN. High- κ dielectrics, which have both a high permittivity (ϵ) and high band gap energy (E_g), can reduce the leakage current density and withstand high breakdown voltages in MOS devices. Both La_2O_3 and Sc_2O_3 , explored in this chapter, have a large E_g (6.18 eV and 6.3eV respectively), high theoretical conduction band offsets, and a relatively high ϵ (27 and 14.1 respectively), making them good candidates for GaN MOSFET insulator layers ^{4, 5}.

Epitaxial growth of the oxides is an encouraging route to reduce leakage current and/or minimize the Fermi level pinning related to a high density of interface states for dielectrics on compound semiconductors ^{6, 7}. However, a significant lattice mismatch between semiconductor and epitaxial dielectric can lead to a high generation of structural defects which can negatively affect these properties. In this chapter, epitaxially grown Sc_2O_3 and La_2O_3 are structurally characterized as potential gate dielectrics for use in GaN based MOSFETs.

6.1 Scandium Oxide

6.1.1. XPS Surface Chemistry Analysis

The O1s spectrum (Fig. 6.1) illustrates the presence of both gallium and scandium bonding to oxygen in a 50 Å Sc_2O_3 film on GaN. Two deconvoluted peaks are located at 532.1 eV and 530.1 eV corresponding with the native stoichiometric Ga_2O_3 and Sc_2O_3 respectively⁸⁻¹¹.

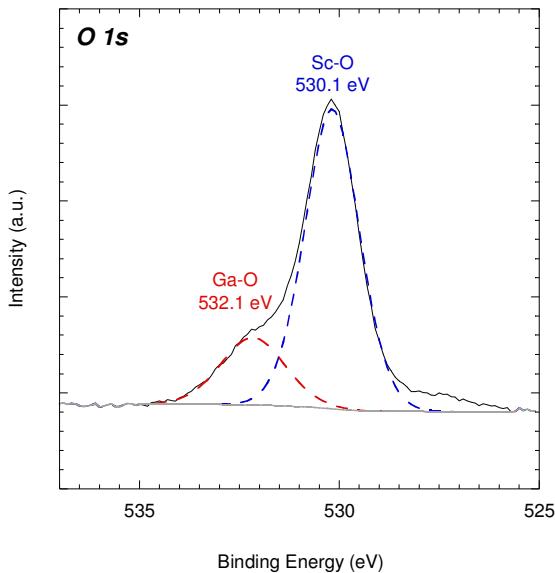


Figure 6.1: XPS spectrum of the O1s peak shows the presence of stoichiometric Sc_2O_3 and native Ga_2O_3 .

Since the sampling depth of XPS is approximately 10 nm for oxides¹², the presence of Ga-O could be a result of bonding at the interface or incomplete coverage of the GaN layer. Thicker oxide samples still exhibit this peak, which suggests Ga-O bonding at the interface. In addition, TEM images show uniformly coalesced Sc_2O_3 , verifying complete GaN coverage (discussed in Sect. 6.1.4). The position of Ga-O peak is shifted from the acid pretreated GaO_x at 531.1 eV to 532.1 eV after Sc_2O_3 deposition. Presumably, the GaO_x layer is desorbed upon heating to the deposition temperature, allowing a new oxide to form when oxygen is introduced in the initial stages of Sc_2O_3 growth.

The O:Sc ratio was found to vary between 2.3-2.4 eV for all samples. Sesquioxides are known to have oxide ions migrate even at relatively low temperatures, which can produce large variations of oxygen content in these oxides¹³. Adachi et. al.¹³ noted that the final stoichiometry is largely dependent on the temperature and oxygen pressure in the ambient atmosphere. Therefore, the observed ratios greater 1.5 are possibly a by-product of MBE growth conditions or simply extra oxygen that has bonded to the surface after exposure to air.

6.1.2. *In-situ* RHEED Analysis

Epitaxial Sc_2O_3 was successfully grown on $\text{K}_2(\text{SO}_4)_2$ cleaned GaN with varying thicknesses, as shown in Fig. 6.2. The narrow streak pattern of GaN, taken at 500 °C prior to oxide deposition, is indicative of an atomically smooth oxide-free surface¹⁴. This is consistent with the findings of Diale et. al.¹⁵, which showed a dramatic reduction in oxygen surface concentrations at temperatures above 100 °C.

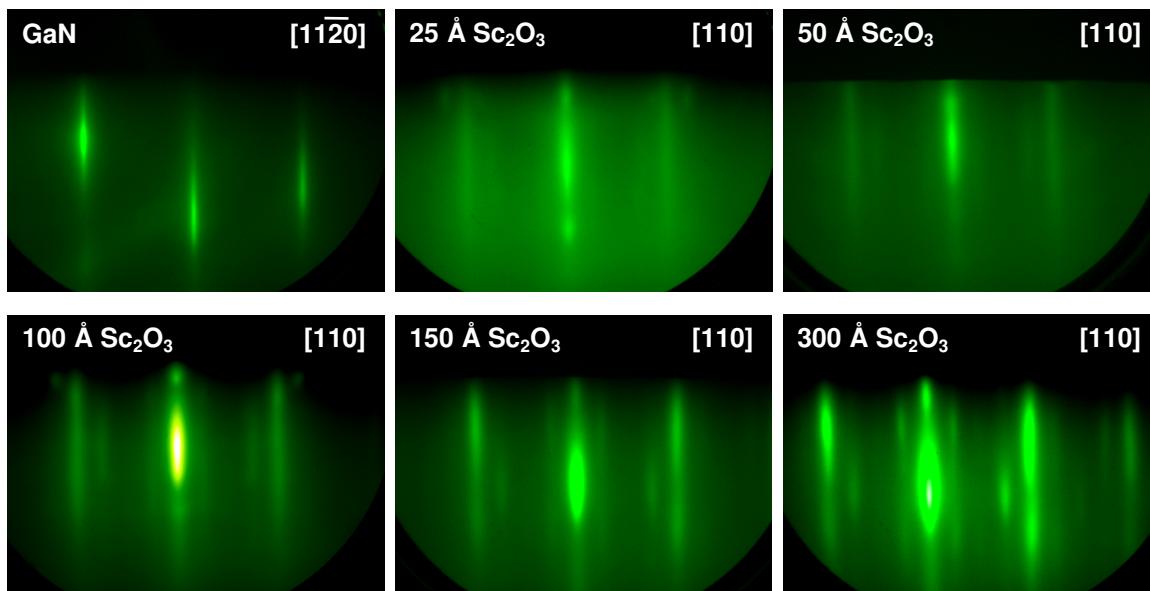


Figure 6.2: *In-situ* RHEED patterns of Sc_2O_3 with different thickness on $\text{K}_2(\text{SO}_4)_2$ cleaned GaN substrates. Thicker samples show 2D reconstruction or twinning as well as increased roughness.

RHEED patterns show the deposited Sc_2O_3 consists of the cubic bixbyite structure (space group Ia3⁶). Thermodynamically, the cubic phase is the stable structure for this oxide¹⁶. The cubic bixbyite structure consists of an fcc array of scandium atoms with oxygen occupying $\frac{3}{4}$ of the tetrahedral sites^{1, 5, 6, 17-19}. The symmetry of the (111) fcc array is identical to the GaN (0001) basal plane, making the (111)//(0001) the lowest energy configuration for the interface of these materials^{1, 5, 17-18}. Observation of [110]//[11-20] in the RHEED images above show the preferred growth direction was realized. The in-plane lattice parameter was measured to be between 10.1-10.4 Å, which is slightly larger than the established 9.845 Å²⁰. This increases the amount of mismatch with GaN, 10.7-13.2%, considering domain matching with double the GaN unit cell. A larger mismatch suggests an epitaxial oxide with a higher density of misfit dislocations, which act as leakage paths to produce lower breakdown voltages in crystalline gate dielectrics⁵. Gila et. al.¹⁷ also showed that as the lattice mismatch between dielectrics and GaN increases, the interface trap density is amplified due to more broken bonds.

Sc_2O_3 exhibits 60° rotational symmetry at all thickness. Normally, cubic crystal structures have 3-fold symmetry, but the observed 6-fold symmetry indicates the presence of 180° rotational twins. The additional streaks seen in Fig. 6.2 could either be an effect of twinning or surface reconstruction. As oxide thickness increases, the RHEED reflections broaden representing an increase in surface roughness. Atomic force microscopy (AFM) was used to measure the root mean square (RMS) roughnesses of the deposited films. All RMS values were between 0.7-1 nm, consistent with previous findings for MBE grown Sc_2O_3 ^{6, 18}. Thus, the extra reflections are likely to be a result of surface reconstruction, suggesting a 2D superstructure indicative of an atomically smooth surface. The smoothness of the surface should prevent localized high breakdown fields, decrease density of interface states, and yield high carrier mobility in Sc_2O_3 gated GaN-based FET devices⁵.

6.1.3 X-Ray Diffraction Analysis

The Philips X’Pert PRO MRD High Resolution X-Ray diffraction system was used to obtain the θ-2θ scan shown in Fig. 6.3. A single Sc_2O_3 peak was observed at 31.35° corresponding to the (222) reflection⁶, which supports the cubic bixbyite crystal structure

determined by RHEED. Using the Bragg diffraction law (Eq. 4.1), the lattice constant calculated was 9.90 Å. This is much closer to the reported value of 9.845 Å than the lattice parameter determined by RHEED. However, this indicates there is still strain within this film. The full width at half maximum (FWHM) for the Sc_2O_3 (222) peak was 0.42°, while the GaN (002) peak had a FWHM of 0.32°. This implies an out-of-plane crystalline quality of about 0.10°, which was verified by ω -2θ scan (0.13°, not shown). Therefore, high-quality Sc_2O_3 can be deposited on GaN by this method.

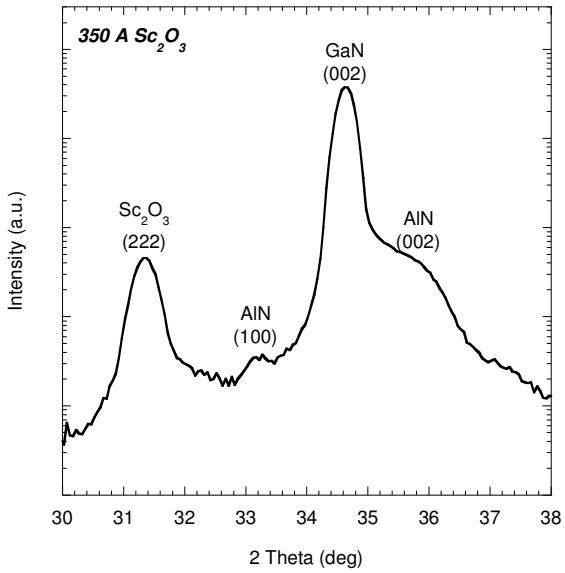


Figure 6.3: XRD scan showing the cubic phase for a 350 Å Sc_2O_3 film on GaN. AlN peaks seen come from the buffer layer used to grow GaN on the sapphire substrate.

The symmetry of the oxide was studied by conducting a phi scan about the Sc_2O_3 (400) peak. Fig. 6.4 shows the cubic peaks are separated by 60° representing 6-fold symmetry, similar to RHEED results. The existence of the extra peaks confirms in-plane twinning of the (111) plane, while the relative intensity of the peaks indicates equal amounts of both orientations in the film. The origin of this twinning could be due to a variation in stacking sequence of the oxide film. Considering the oxide cubic bixbyite structure as an fcc array of scandium atoms, the closed-packed stacking arrangement on the GaN unit cell is equally favorable in both the ABCABC... and the ACBACBA... sequences ⁵. Each stacking sequence results in a different in-plane orientation, which produces the observed twinning.

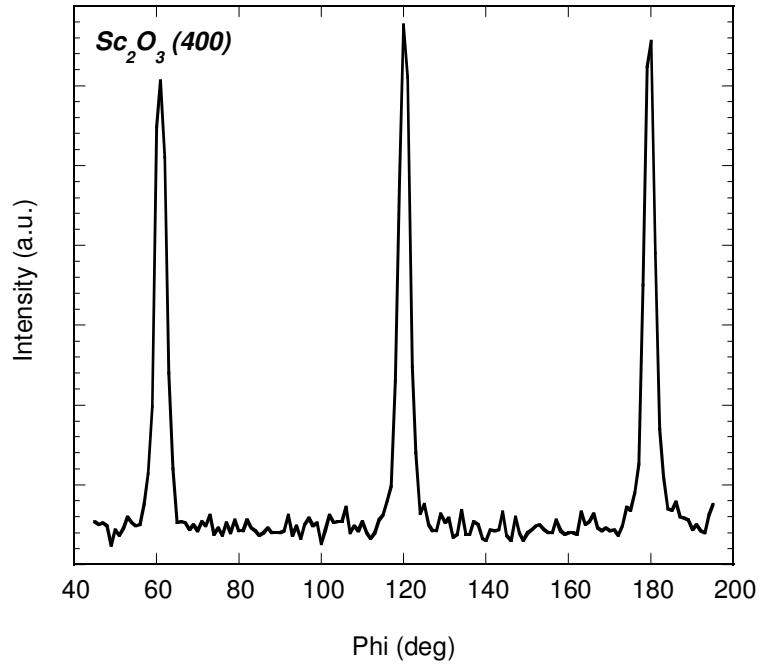


Figure 6.4: *Phi* scan about the (400) Sc_2O_3 peak, where 6-fold symmetry indicates in-plane twinning.

6.1.4 High-Resolution TEM Analysis

Epitaxial and structural quality suggested by *in-situ* RHEED and XRD is verified by TEM images in Fig. 6.5. Sc_2O_3 exhibits an abrupt interface with GaN and a very uniform high-quality crystalline structure, indicating that Sc_2O_3 is relatively thermodynamically stable with GaN up to 500 °C. Liu et. al.⁶ showed that Sc_2O_3 is stable in temperatures up to 700 °C, well above what we have attempted here. The TEM images show no indication of a gallium oxide transition layer at the interface suggested by XPS.

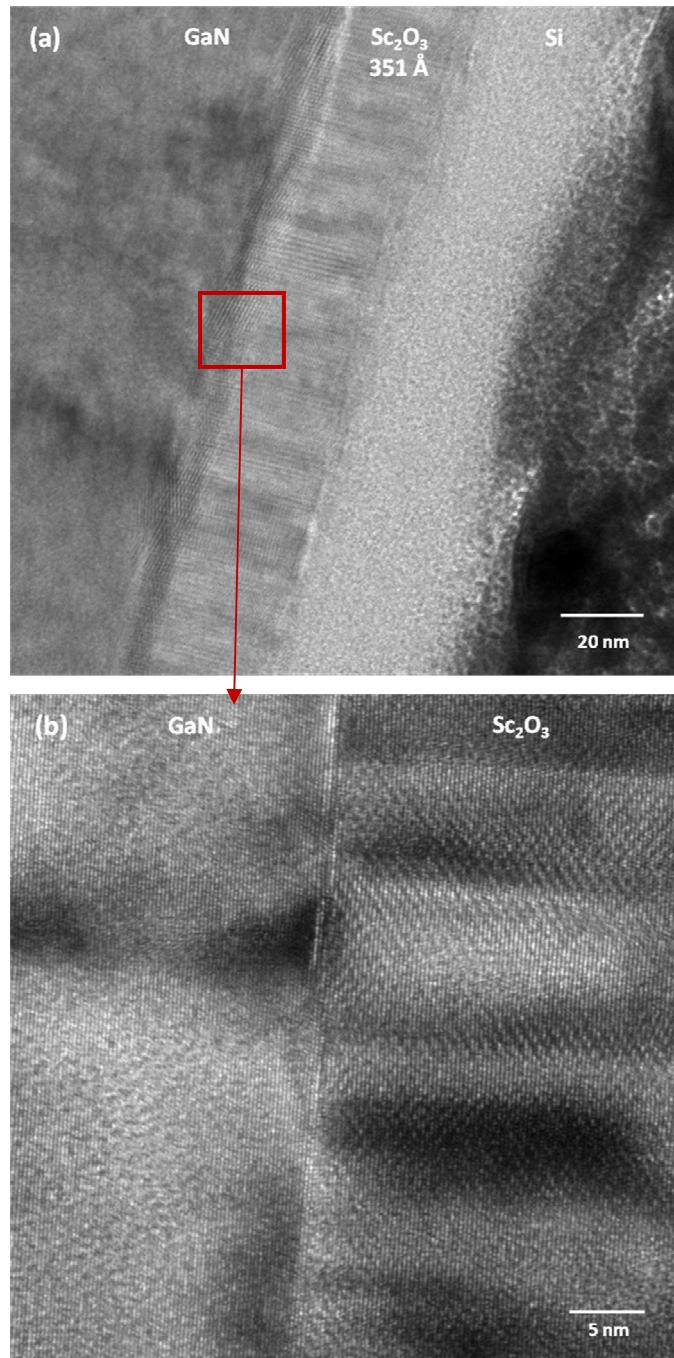


Figure 6.5: Cross sectional HR-TEM of the $\text{Sc}_2\text{O}_3/\text{GaN}$ interface showing (a) at uniformly deposited oxide, and (b) the crystalline lattice of Sc_2O_3 .

Though the deposited film shows good single crystal quality, defects are still seen nucleating from the interface at periodic distances as illustrated in the lattice image (Fig.

6.5(b)). Most likely these are misfit dislocations arising from the large lattice mismatch between Sc_2O_3 and GaN (10.7-13.2%). The low magnification image shows areas with moiré fringes. Herrero et. al.⁵ suggested that these fringes result from in-plane twinning; however, it is more likely that the fringes seen here are a product of a highly strained interface. Fig. 6.6 shows a slightly off-axis image that illustrates the strained interface more clearly.

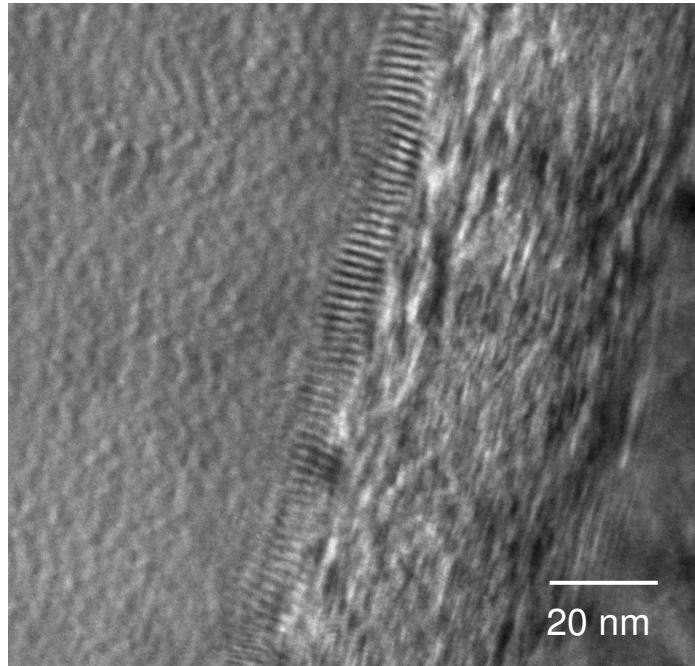


Figure 6.6: Cross-section TEM image slightly off-axis showing the highly strained interface that results from Sc_2O_3 being deposited on GaN.

6.1.5 Sc_2O_3 Band Offsets with GaN

The band alignment across the $\text{Sc}_2\text{O}_3/\text{GaN}$ interface was determined based on the photoemission method developed by Kraut, Grant and Waldrop²¹ (Fig. 6.7). Valence band maximums for the bulk GaN and thick Sc_2O_3 film were obtained by the intersection between the linearly fitted leading valence band edge and the flat energy distribution²². Since the XPS sampling depth of oxides is about 10 nm, a 15 Å Sc_2O_3 film was prepared in order to obtain information from each layer simultaneously.

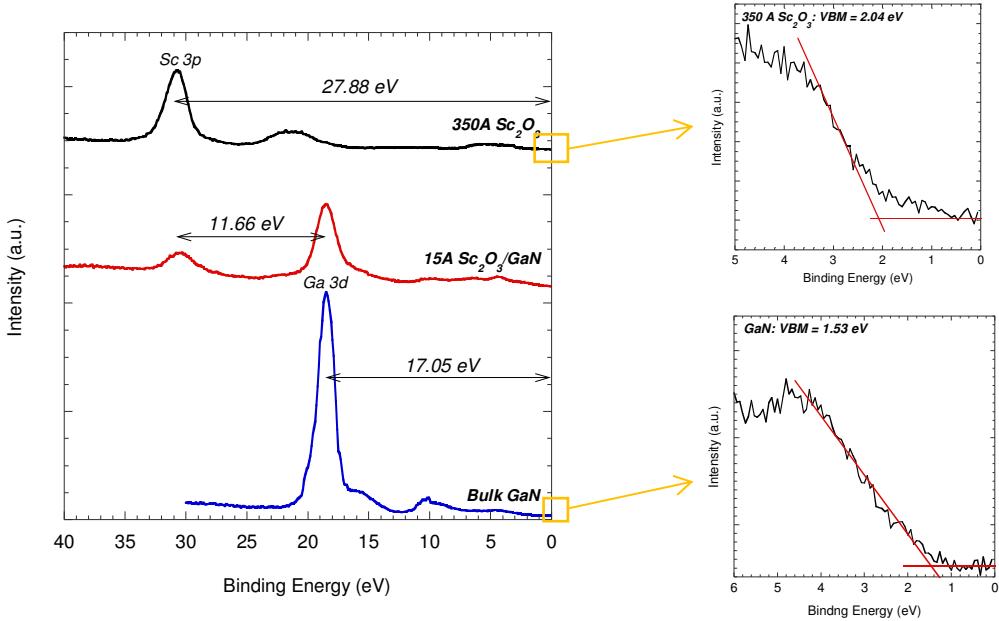


Figure 6.7: Valence band offset between Sc_2O_3 and GaN was determined using the standard core-level photoemission-based method.

The valence band offset (VBO) was calculated using the expression:

$$VBO = (E_{\text{Sc}3p} - E_{\text{Ga}3d})_{\text{Sc}_2\text{O}_3/\text{GaN}} - (E_{\text{Sc}3p} - E_v)_{\text{Sc}_2\text{O}_3} + (E_{\text{Ga}3d} - E_v)_{\text{GaN}} \quad (6.1)$$

Using the measured values shown in Fig. 6.6, the VBO was determined to be 0.8 ± 0.1 eV. The conduction band offset (CBO) can then be ascertained using the equation:

$$CBO = E_g^{\text{Sc}_2\text{O}_3} - E_g^{\text{GaN}} - VBO \quad (6.2)$$

Given band gap energies of 6.3¹⁷ and 3.4 eV for Sc_2O_3 and GaN respectively, the CBO was evaluated as 2.1 ± 0.1 eV. These values correlate well with both band offsets predicted by Robertson and Falabretti³ using the charge neutrality method, and with previous experimental reports^{1, 4, 12}. The large conduction band offset should be sufficient for minimizing carrier thermionic emission during high temperature applications^{3, 12}. While the VBO is slightly less than the 1 eV generally required for ample carrier confinement, GaN-based MOSFETs currently utilize an electron channel needing a large CBO barrier^{3-4, 23}. The VBM of the 15 Å film was determined to be 2.9 ± 0.1 eV, indicating that there is still

interface pinning following Sc_2O_3 deposition. The following chapter will discuss the band alignment in conjunction with collected leakage current data to establish the potential of Sc_2O_3 as gate oxides in GaN-base devices.

6.2 Lanthanum Oxide

6.2.1. XPS Chemical Surface Analysis

Fig. 6.8 shows the O1s spectrum for a 200 Å La_2O_3 film on GaN substrate. Three deconvoluted peaks located at 528.9, 530.8, and 532.0 eV are related to La_2O_3 , $\text{La}(\text{OH})_3$, and the $\text{La}-\text{CO}_3^{2-}$ species respectively²⁴⁻²⁶.

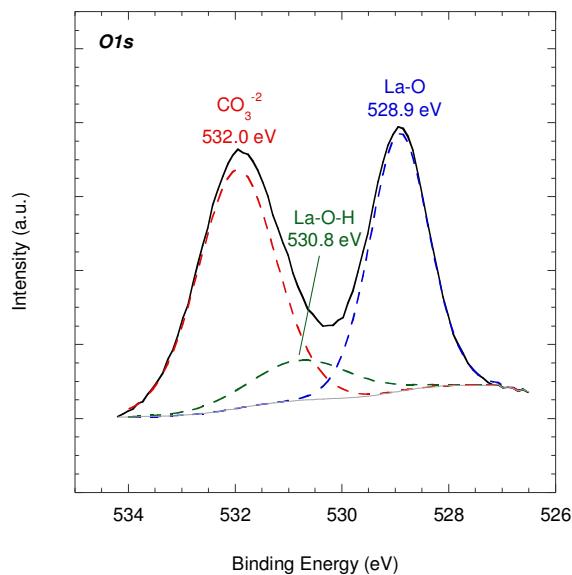
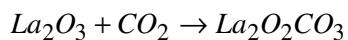


Figure 6.8: XPS O1s spectrum showing the presence of La_2O_3 , $\text{La}(\text{OH})_3$ and a lanthanum carbonate species.

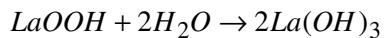
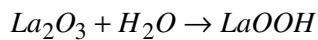
Due to large ionic radii and low electronegativities, sesquioxides are known to react with atmospheric water and carbon dioxide to form hydroxides and carbonates at ambient temperature and pressure^{7, 13, 26-27}. La_2O_3 has the largest ionic radius and lowest electronegativity of these oxides, which makes it the most reactive in air²⁶. The hydroxide peak in Fig.6.8 is located about 2 eV above La-O bonding, consistent with previous findings

²⁵. While the peak located at 532 eV is consistent with Ga-O bonding in Ga_2O_3 , the thickness of this sample makes it more likely that this peak results from the lanthanum carbonate species reported at 532.6 eV ²⁶. Even though this sample was immediately transferred from the MBE chamber to the XPS chamber, it was exposed to air for approximately 15 minutes. Gougousi and Parsons ²⁸ conducted an in-depth study on lanthanum hydroxide and carbonate formation and found both are formed within 10 minutes of exposure to air. They also showed that the carbonate species is a one step reaction, while hydroxide formation takes two steps as shown below.

Carbonate Species:



Hydroxide Species:



Formation of hydroxides and carbonates lead to degradation in permittivity, surface roughness, and density of La_2O_3 films ^{24-25, 28-29}. Therefore, *in-situ* capping can be used to suppress diffusion of air through the epitaxial film ^{25, 28}. The two different capping metals explored in this research were tantalum and amorphous silicon.

6.2.2. *In-Situ* RHEED Analysis

Epitaxial La_2O_3 was successfully grown on $\text{K}_2(\text{SO}_4)_2$ cleaned GaN with varying thicknesses, as shown in Fig. 6.9. Like Sc_2O_3 , the GaN substrate prior to oxide deposition had a narrow streak pattern indicative of an atomically smooth, oxide-free surface. While oxide-free silicon substrates exhibit an arched spot pattern, GaN layers will exhibit a streak pattern due to the imperfections resulting from heteroepitaxial growth on sapphire substrates.

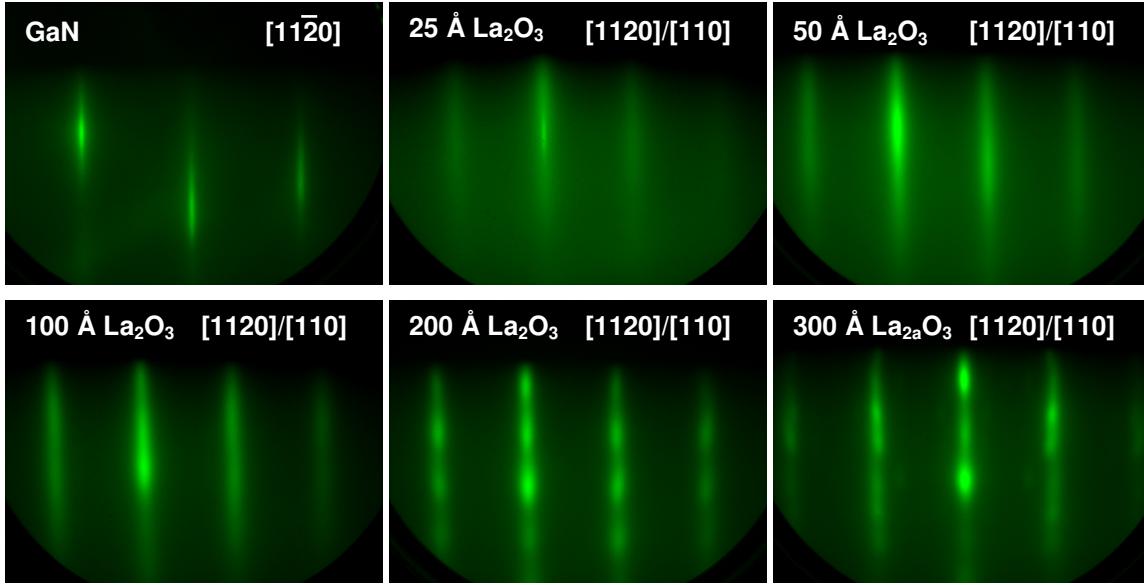


Figure 6.9: *In-situ* RHEED patterns of La_2O_3 with different thickness on $\text{K}_2(\text{SO}_4)_2$ cleaned GaN substrates. Cubic phase would result in $[110]/[11-20]$ while hexagonal phase would yield $[11-20]$. Thicker samples show increase in surface roughness.

The crystal structure of the deposited La_2O_3 films cannot be explicitly determined from the RHEED patterns shown in Fig. 6.9. The streak patterns could be a result of either a cubic bixbyite or hexagonal crystal structure. Previous phase diagrams describing the lanthanide sesquioxides do not have a clearly defined transition temperature for the cubic to hexagonal transition¹³. Initially, it was thought that the cubic phase was a metastable state which could not exist at room temperature; however, recent experimental results for various deposition techniques have shown the existence of the cubic phase up to 700 °C^{24, 26-27, 30}. Therefore, both phases could be present in the RHEED images and explicit determination must be done via x-ray diffraction (Section 6.2.3).

All La_2O_3 films had 60° rotational symmetry indicative of either hexagonal symmetry or in-plane twinning of the cubic (111) plane. The in-plane lattice parameters were calculated considering both phases as shown in Table I below. For the cubic crystal structure, the lattice mismatch was calculated using domain matching with triple the GaN unit cell.

Table I: In-plane lattice parameters and mismatch for La_2O_3 on GaN evaluated from RHEED

	<i>In-plane lattice parameter (\AA)</i>	<i>Reported lattice parameter (\AA)</i> ¹³	<i>Lattice mismatch with GaN (δ)</i>	<i>Predicted δ with GaN*</i>
<i>Cubic</i>	11.7-11.8	11.36	14.5-15.4%	19.1%
<i>Hexagonal</i>	3.90-3.93	3.94	18.2-18.8%	19.0%

Despite the structure of the La_2O_3 , it has a larger lattice mismatch than Sc_2O_3 with GaN, which would suggest the presence of more misfit dislocations. Therefore, a higher leakage current and lower breakdown voltage is expected with a La_2O_3 gate dielectric as compared to Sc_2O_3 .

Films with thickness less than 150 \AA showed streak patterns indicative of smooth 2D growth. However, the slight increase in observed streak widths signifies a minor increase in surface roughness with thickness. Films thicker than 200 \AA exhibit a more spot-like pattern implying a 3D textured film, which is expected with larger mismatches. No surface reconstruction is seen in these RHEED patterns, as was seen in the Sc_2O_3 films.

6.2.3. X-Ray Diffraction Analysis

XRD was conducted on a 250 \AA La_2O_3 film with tantalum capping using an area detector as shown in Fig. 6.10 below. The θ - 2θ spectrum exhibited peaks at 27.2° and 28.7° correlating to the cubic (222) and hexagonal (0002) phases (JCPDF files 40-1284 and 05-0602). Mixed phases have been seen before in MOCVD films deposited on silicon at similar growth temperatures³⁰.

Since XPS showed the formation of hydroxide which would exhibit an XRD peak only 0.2° above the cubic (222), the sample was tilted to the (400) peak to verify the presence of the (222) peak. Using the Bragg diffraction law (Eq. 4.1), the lattice constants of the cubic and hexagonal phases were calculated to be 11.35 \AA and 3.59 \AA respectively. Both values are similar to those obtain by RHEED and reported previously (Table I).

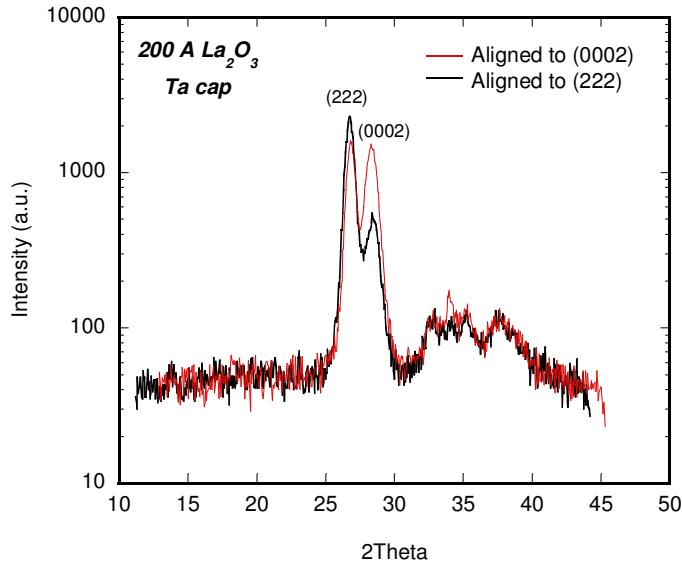


Figure 6.10: Both cubic and hexagonal phases observed in θ - 2θ spectrum. Scans were taken aligning to each phase to show relative amounts of each in the 200 \AA sample.

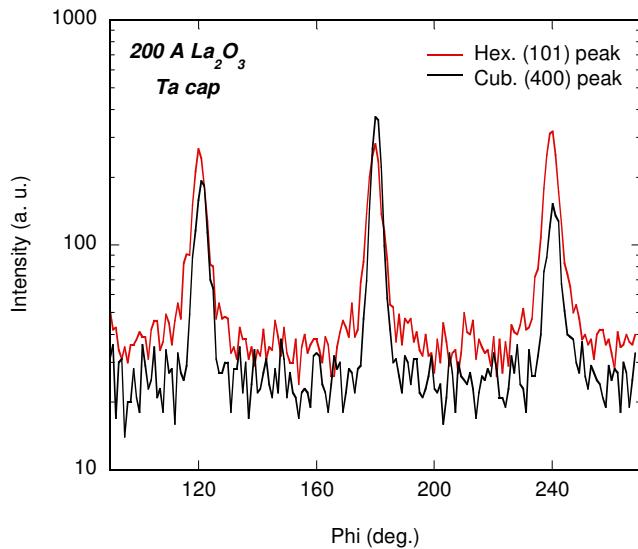


Figure 6.11: Phi scans showing the 6-fold symmetry for both hexagonal and cubic peaks. For the cubic peak this verifies in-plane twinning within the film.

Fig. 6.12(a) shows the stability of the Ta capped film over a three month period. Zhao et. al. ²⁹ observed that an uncapped La_2O_3 film exposed to air will exhibit an increase of the hydroxide peak at the expense of the hexagonal La_2O_3 peak. The decrease shown in

Fig. 6.12(a) does not correspond with an increase in intensity, increase in width, or a shift of the peak at 27.2° , which would suggest a lack of hydroxide formation. Therefore, the reduction in the hexagonal peak is attributed by the partial transformation to an amorphous layer, which cannot be clearly detected by XRD ²⁷.

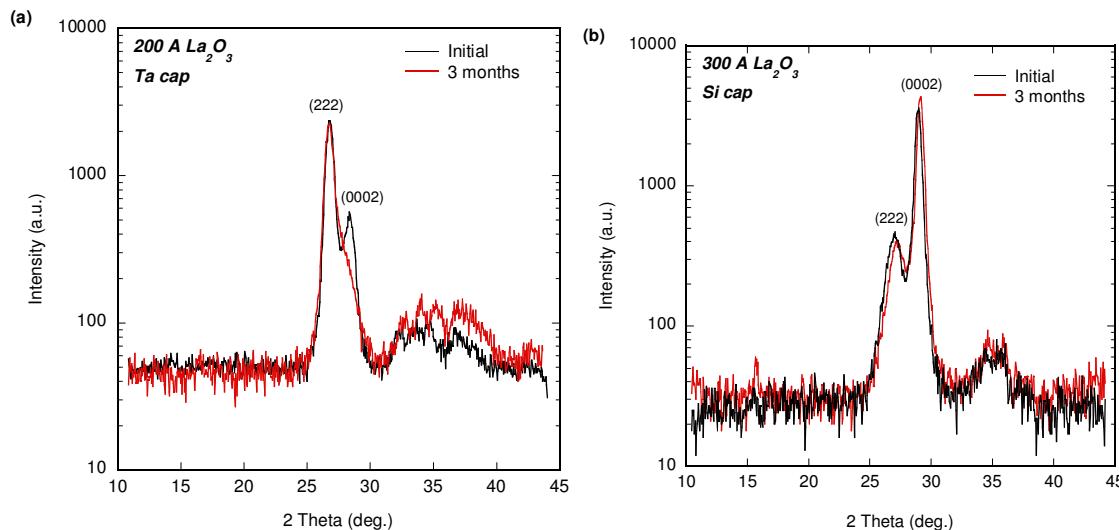


Figure 6.12: θ - 2θ scans aligned to the (222) for (a) Ta capped film over a 3 month span, and (b) Si capped film over a 1 month span.

In order to determine if the reduction of the hexagonal peak is a result of poor capping, an amorphous silicon cap was deposited on a 300 Å La₂O₃ and scanned over a one month period. Fig. 6.12(b) shows that there is negligible change with the silicon cap compared to the tantalum cap. Therefore, the previous change in the hexagonal peak is most likely due to reactions with species from air overtime, which could include the formation of impurities such as lanthanum carbonates.

Scarel et al. ³¹ proposed that preferential growth of the cubic or hexagonal phase resulted from variation in film thickness. Thicker samples tended to exhibit the hexagonal structure. Therefore, θ - 2θ scans were performed on 100-300 Å films with silicon capping to test this hypothesis. Fig. 6.13 shows both the cubic (222) and hexagonal (002) peaks are present in the 100 Å and 300 Å films. However, the 200 Å sample exhibited only the hexagonal peak. Previous reports indicated that even a slight increase in growth

temperature or pressure can cause films to change from cubic to hexagonal in the temperature range 500-550 °C ²⁷. Recently, Fedorov et. al. ³² showed that the transition was accompanied by the removal of volatile impurities and therefore not a polymorphic transition. Since both peaks are observed in the 300 Å sample, it is assumed that the preferential growth of the hexagonal phase was an effect of slight variations in the growth conditions rather than thickness variation.

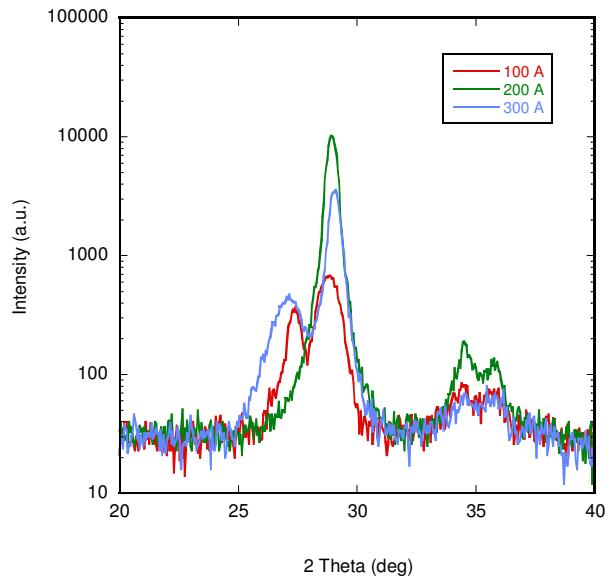


Figure 6.13: θ - 2θ scans for varying La_2O_3 film thicknesses (aligned to the (222) peak).

The increase in both peak intensities with increasing film thickness implies both cubic and hexagonal phases are nucleated at the interface. The lattice mismatch difference between the two phases is only about 3%, further suggesting that neither would be preferred at the interface with GaN.

The quality of the (222) and (0002) peaks with thickness were evaluated by chi scans shown in Fig. 6.14.

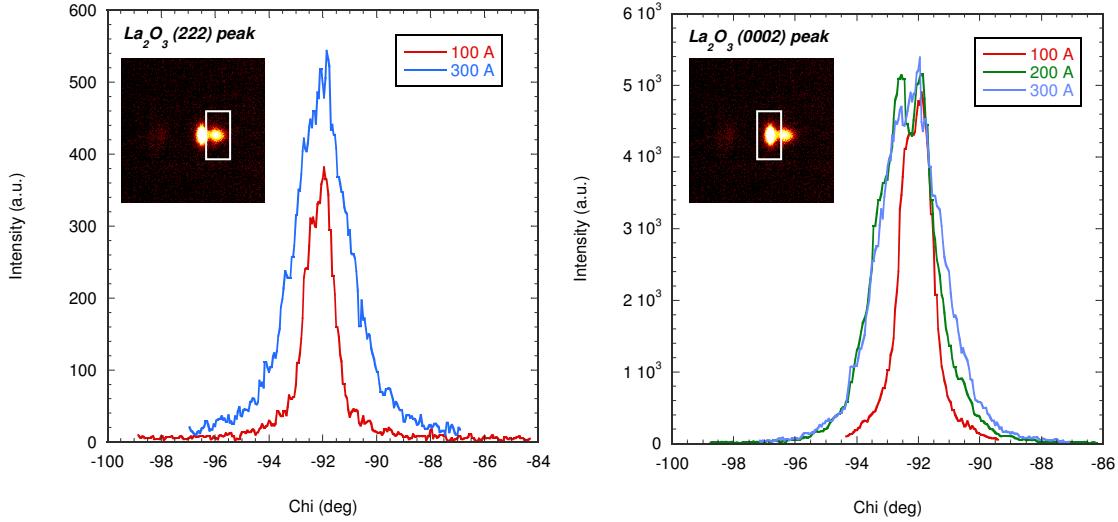


Figure 6.14: Chi scans for both the (222) and (0002) peaks with varying film thickness.

For both peaks, the 100 Å exhibits a smaller FWHM than the thicker samples as a result of less tilt, twist, and defects within sample. While the 100 Å cubic and hexagonal peaks both have a FWHM of 1.2°, the 300 Å film exhibits an increase to 2.1° and 2.5° respectively. Hexagonal La_2O_3 has a larger mismatch (Table I) which would cause more misfit dislocations or low angle grain boundaries consistent with the wider chi peak. The out-of-plane crystal quality is substantially worst for La_2O_3 than seen in Sc_2O_3 films.

6.2.4. High-Resolution TEM Analysis

Cross sectional high-resolution TEM images showed the existence of an interfacial layer between the GaN and deposited La_2O_3 (Fig. 6.15). This layer was uniform across the surface and consisted of approximately four atoms or 12 Å. When La_2O_3 is deposited on silicon substrates, a lanthanum silicate interfacial layer is known to form ²⁴. Zinkevich et. al. ³³ did an in-depth study on the phase diagram and thermodynamics of the $\text{La}_2\text{O}_3\text{-Ga}_2\text{O}_3$ system, which showed the formation of LaGaO_3 (LGO) at 400-500 °C. Therefore, it is likely that the interfacial layer seen here is the orthorhombic LGO.

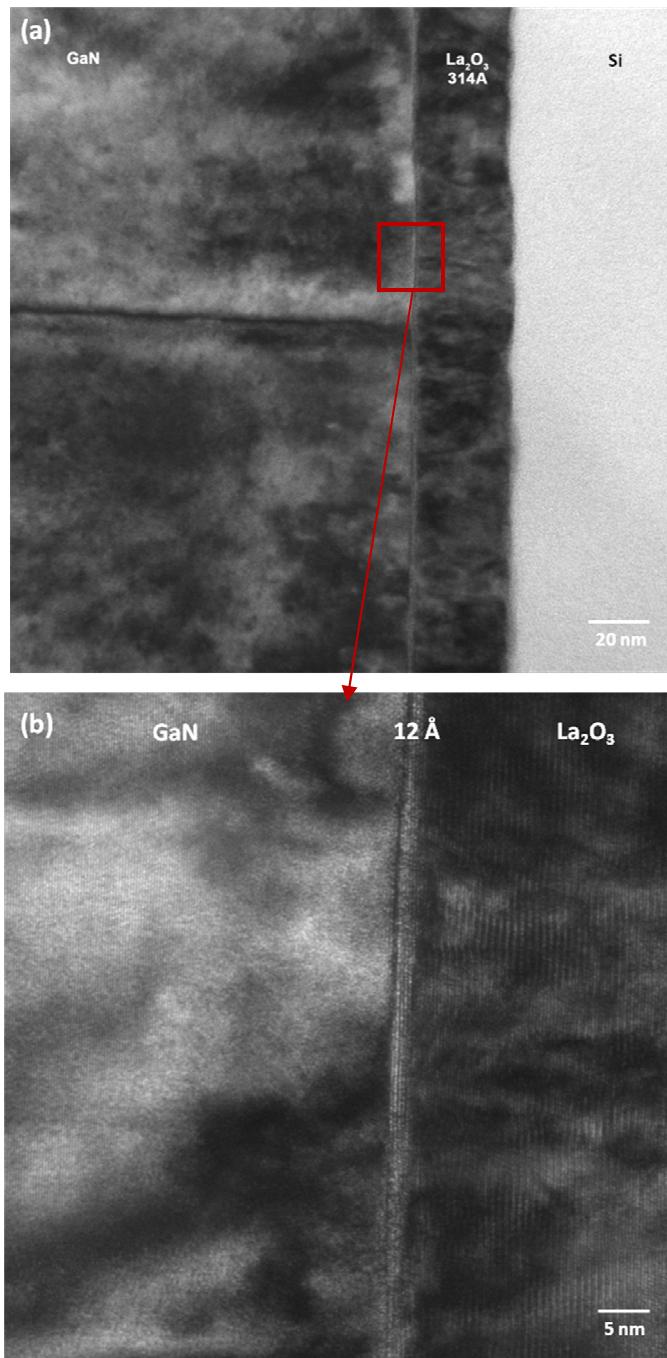


Figure 6.15: Cross-sectional TEM of the $\text{La}_2\text{O}_3/\text{GaN}$ interface showing (a) uniform oxide layer and (b) the existence of a crystalline interfacial layer.

Fig. 6.16 shows the uniform epitaxial polycrystalline structure of the La_2O_3 on GaN. The grains exhibit different orientations and most likely are different crystal structures. This would explain the occurrence of both cubic and hexagonal peaks detected by XRD. Furthermore, the highly defective nature of the film shown is consistent with the large FWHM of the chi peaks in Fig. 6.14.

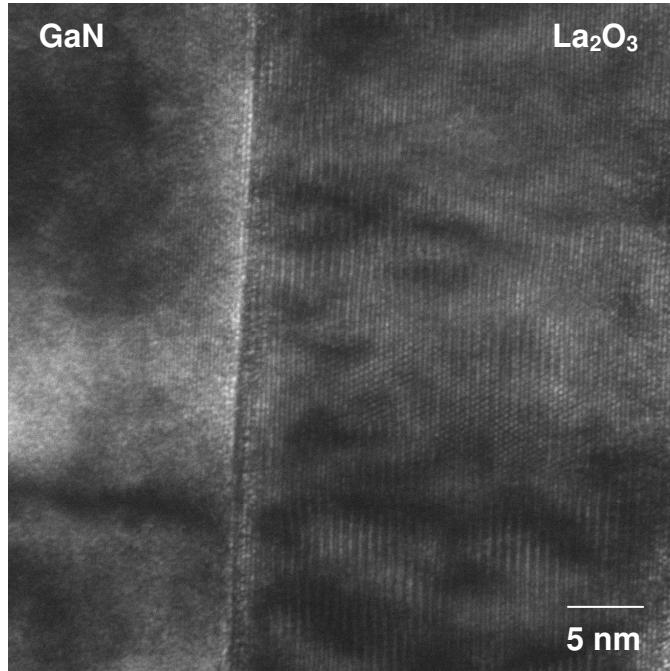


Figure 6.16: Cross-sectional TEM showing the polycrystalline structure of the 300 \AA La_2O_3 .

6.2.5 La_2O_3 Band Offset with GaN

The band alignment across the $\text{La}_2\text{O}_3/\text{GaN}$ interface was determined by XPS following the method described above in Section 6.1.5. Fig. 6.17 shows the spectra for 200 \AA La_2O_3 , 15 \AA La_2O_3 , and bulk GaN samples. The VBO was calculated using the expression:

$$\text{VBO} = (E_{\text{La}5p} - E_{\text{Ga}3d})_{\text{La}_2\text{O}_3/\text{GaN}} - (E_{\text{La}5p} - E_v)_{\text{La}_2\text{O}_3} + (E_{\text{Ga}3d} - E_v)_{\text{GaN}} \quad (6.3)$$

The measured values, shown in Fig. 6.17, resulted in a VBO of 1.9 ± 0.1 eV. Using Eq. 6.2 and a La_2O_3 band gap energy of 6.2 eV ^{24, 34}, the CBO was calculated to be 0.9 ± 0.1 eV. These values are inconsistent with those predicted by the charge neutrality method ³. This

inconsistency most likely arises since the charge neutrality method neglects specific interface bonding; therefore, polar semiconductors could exhibit much larger errors³. Both the VBO and the CBO meet the requirements for ample carrier confinement at high temperature, which is needed to minimize leakage in GaN MOSFETS^{3-4, 23}. The confinement of both hole and electron injection suggest this oxide could be used in complementary MOS devices. In addition, the 15 Å VBM was found to be 3.4 ± 0.1 eV indicating that the deposition of La_2O_3 leaves an unpinned GaN interface, which helps achieve larger channel charges by minimizing the density of interface traps under the gate. The electrical effects resulting from this structure will be discussed in the next chapter.

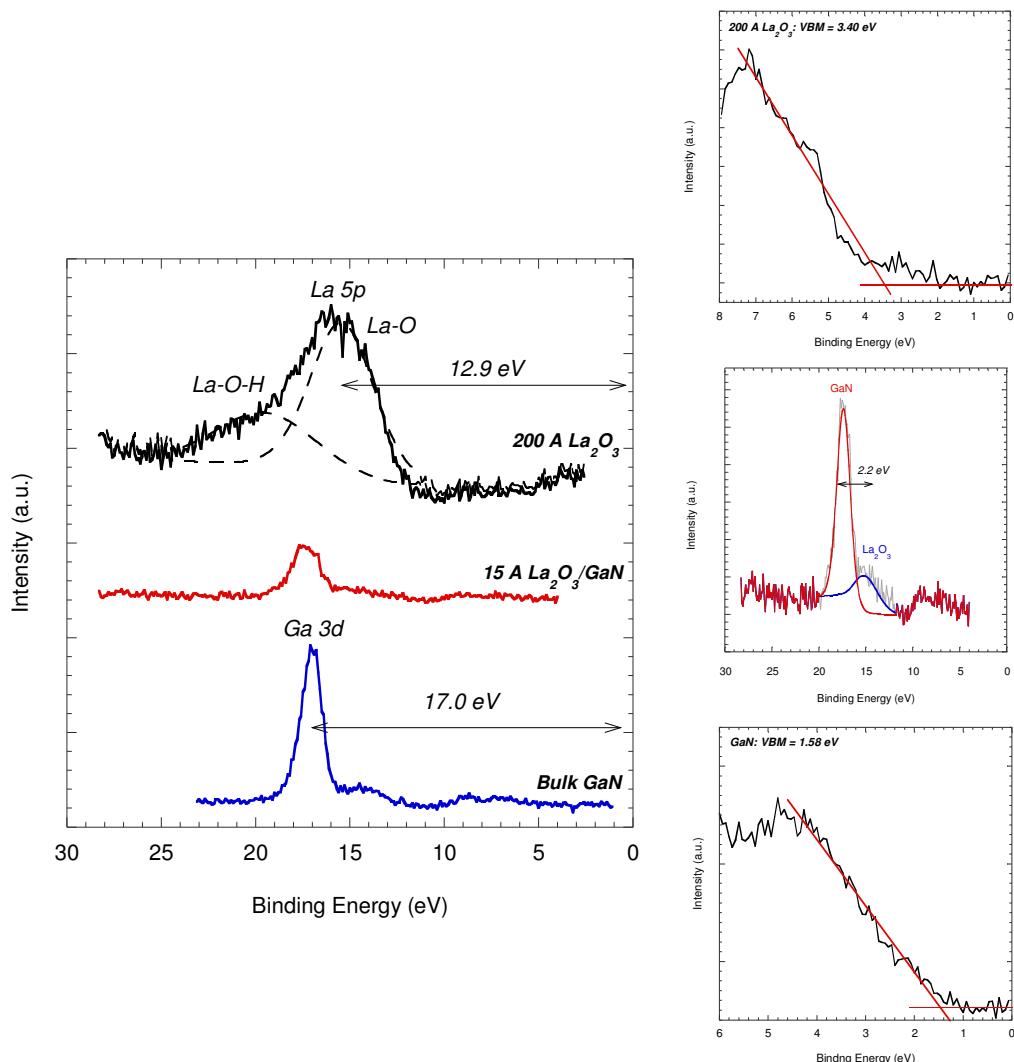


Figure 6.17: Valence band offset between La_2O_3 and GaN was determined using the standard core-level photoemission-based method

6.3 Conclusions

Epitaxial La_2O_3 and Sc_2O_3 were successfully grown on GaN. Sc_2O_3 exhibited the stable cubic bixbyite crystal structure, while La_2O_3 had a mix of both cubic and hexagonal crystal structures. XRD and RHEED proved the existence of in-plane twinning within the cubic phase of both oxides. TEM images showed an abrupt atomic interface for Sc_2O_3 films,

but the formation of an interfacial layer between La_2O_3 and GaN films. This suggests better thermal stability for Sc_2O_3 films up to 500 °C.

La_2O_3 was found to be extremely reactive with water and carbon dioxide in air, which formed both lanthanum hydroxides and carbonates within 15 minutes of exposure. Therefore, tantalum and silicon were explored as *in-situ* capping metals to prevent these deleterious effects. Tantalum showed some inability as a barrier to diffusion of contaminants, while silicon exhibited good stability over at least a month.

Table II summarizes the structural properties determined in this chapter. The larger mismatch of La_2O_3 suggests the formation of a more defective oxide than Sc_2O_3 , which was verified by XRD and TEM. Both oxides had sufficiently large band offsets, which should prevent thermionic emission of carriers at high device operation temperatures. La_2O_3 provides a more effective barrier to holes, while Sc_2O_3 is a better barrier for electrons. Therefore, both oxides are good candidates for gate dielectrics in GaN-based MOSFETs. The next chapter will explore the relationship between the structural and electrical properties to further verify the potential of Sc_2O_3 and La_2O_3 as gate oxides.

Table II: Structural Properties of Sc_2O_3 and La_2O_3 on GaN

	<i>In-plane lattice parameter (Å)</i>	<i>Lattice mismatch with GaN (δ)</i>	<i>VBO (eV)</i>	<i>CBO (eV)</i>
Sc_2O_3	9.9-10.4	8.9-13.2%	0.8 ± 0.1	2.1 ± 0.1
La_2O_3	11.35-11.8 (c)	14.5-19% (c)		
	3.90-3.93 (h)	18.2-19% (h)	1.9 ± 0.1	0.9 ± 0.1

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7. Preliminary Electrical Results for Oxides as Gate Dielectrics in GaN MOS devices

In the previous chapter, the structural properties of Sc_2O_3 and La_2O_3 were analyzed in detail. However, for implementation into GaN enhancement-mode MOSFETs, the electrical properties of these oxides and their interface with GaN must be determined. This chapter will take a look at preliminary electrical results of MOS capacitors, which can indicate the behavior of these rare earth oxides as gate dielectrics in power devices. When possible, the relationship between oxide microstructure and observed electrical properties will be discussed.

7.1 Three-Element Circuit Model

Accurate measurement of device capacitance is critical for determination of oxide thickness, mobility, and density of interface traps ¹⁻³. For thin oxides, the direct tunneling leakage current is very large, making accurate capacitance measurements difficult. Deleterious leakage effects can be overcome by collecting the capacitance at high frequencies where the capacitance current dominates ⁴. However, at higher frequencies the series resistance becomes substantial and can result in decreased measured capacitance (Fig. 7.1).

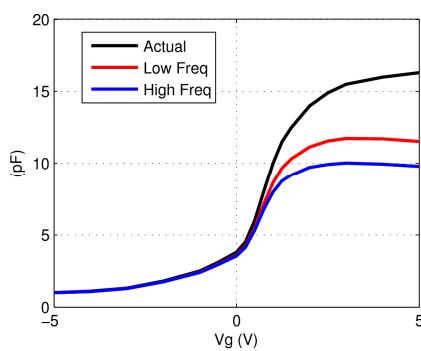


Figure 7.1: Example C-V curves where the high frequency capacitance is reduced as an effect of leakage and large series resistance.

C-V measurements can be expressed with either a two-element parallel or two-element series circuit model. In this thesis and in general, C-V measurements are collected using the two-element parallel circuit, which neglects series resistance. Therefore, Yang et al.⁴ proposed a three-element circuit model to correct for the significant series resistance that causes a decrease in capacitance at high frequencies. Fig. 7.2 shows both the measured two-element circuit and the proposed three-element circuit, where subscripts p and m denote parallel and measured values respectively, r_s is the series resistance, and C is the corrected capacitance (discussed below).

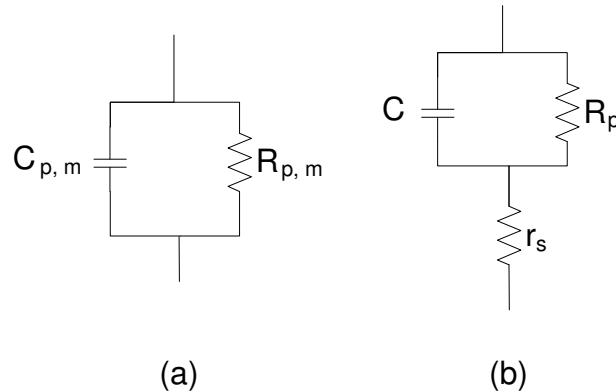


Figure 7.2: (a) Parallel circuit model for low series resistance devices, (b) corrected model accounting for series resistance

7.1.1 Derivation of Corrected Capacitance and Series Resistance

From the circuits above, the measured two-element impedance is given by

$$Z_m = \frac{1}{G_{p,m} + j\omega C_{p,m}} = \frac{R_{p,m}}{1 + j\omega R_{p,m} C_{p,m}}. \quad (7.1)$$

This impedance can then be rewritten in terms of the dissipation factor (D_m) resulting in

$$Z_m = \frac{D_m - j}{\omega C_{p,m} (D_m^2 + 1)} \text{ where } D_m = \frac{1}{\omega C_{p,m} R_{p,m}}. \quad (7.2)$$

Similarly, the three-element circuit model impedance can be expressed as

$$Z_3 = r_s + \frac{1}{G_p + j\omega C} = r_s + \frac{R_p(1 - j\omega C R_p)}{1 + \omega^2 C^2 R_p^2}. \quad (7.3)$$

Equating the imaginary parts of the measured impedance (Eq. 7.2) and the true impedance (Eq. 7.3), an expression for the true capacitance as a function of the measured capacitance can be derived.

$$\frac{1}{CR_p^2} + \omega^2 C = \omega^2 C_{p,m}(D_m^2 + 1) \quad (7.4)$$

The true capacitance is experimentally determined by measuring the capacitance and dissipation at two different frequencies, substituting each into Eq. 7.4, and subtracting.

$$C = \frac{\omega_1^2 C_{p,m1}(D_{m1}^2 + 1) - \omega_2^2 C_{p,m2}(D_{m2}^2 + 1)}{\omega_1^2 - \omega_2^2} \quad (7.5)$$

Series resistance can be found in a similar manner by equating the real part of the measured and true impedances.

$$r_s + \frac{R_p}{1 + \omega^2 C^2 R_p^2} = \frac{D_m}{\omega C_{p,m}(D_m^2 + 1)} \quad (7.6)$$

Inserting either of the frequencies used to calculate the true capacitance, the series resistance is given by

$$r_s = \frac{D_{m1}}{\omega_1 C_{p,m1}(D_{m1}^2 + 1)} - \frac{R_p}{1 + \omega_1^2 C^2 R_p^2}. \quad (7.7)$$

7.1.2. Systematic Error Analysis for Three-Element Model

The technique developed by Yang et.al ⁴ is employed in this thesis to correct for the high series resistance seen in the C-V measurements. The resulting frequency-independent capacitance is then used to determine parameters such as dielectric constant and channel charge. Therefore, it is important to note the systematic error that is associated with the corrected capacitance.

Based on Fig. 3, the capacitance component of the complex impedance is related to the phase angle by the equation

$$j\omega C_p = |Z_i| \cos(\theta). \quad (7.8)$$

At very small or very large angles, error is minimized which makes the measured capacitance fairly accurate. The dissipation factor, D_m , is related to the phase angle by,

$$\tan(\theta) = D_m \quad (7.9)$$

Therefore, the error for capacitance components is simply $(\Delta\theta/\theta)$.

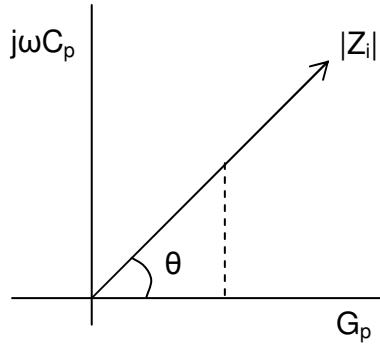


Figure 7.3: Concept of the complex impedance considered for progression of error in the three-element model.

Using Eq. 7.5 for the true capacitance, the progression of error can be calculated using the standard assessment. Only the capacitance components contain error (including D_m), while frequency is assumed to be correct. Therefore, Eq. 7.5 can be rewritten in a simplified form to observe the affect of only the error components,

$$\sum C_{true} = \sum x^3 - \sum y^3 \quad (7.10)$$

where \sum is the standard deviation, x is first frequency capacitance components, and y is the second frequency capacitance components. The progression of deviation for power factors (ie. $Q = x^n$) can be expressed in general terms as ⁵

$$\frac{\sum Q}{Q} = \left(\frac{n \sum x}{x} \right)^n \quad (7.11)$$

where Q is the overall variation and x is the quantity being raised to the n th power. In a similar fashion, the progression of error when added or subtracted can be expressed as ⁵

$$\sum Q = \sqrt{\sum x^2 + \sum y^2}. \quad (7.12)$$

Thus, the error in the three-element true capacitance is simply a combination of Eq. 7.10-7.12. As can be seen by this analysis, the error can increase rapidly for this model and it is

not unusual to encounter errors as large as 10-20%. This needs to be kept in mind when analyzing parameters derived from the corrected capacitance.

7.2 Capacitance-Voltage (C-V) Results and Discussion

Preliminary C-V results for MOS capacitors comprised of 100 Å La_2O_3 and Sc_2O_3 films are shown in Fig. 7.4. The La_2O_3 sample was capped with a 200 Å tantalum layer to limit hydroxide formation as discussed in Chapter 6. The capacitance for both films has been corrected using the three-element model to correct for leakage and high series resistance. A larger capacitance was observed for La_2O_3 , while Sc_2O_3 exhibited a larger positive flat band voltage shift.

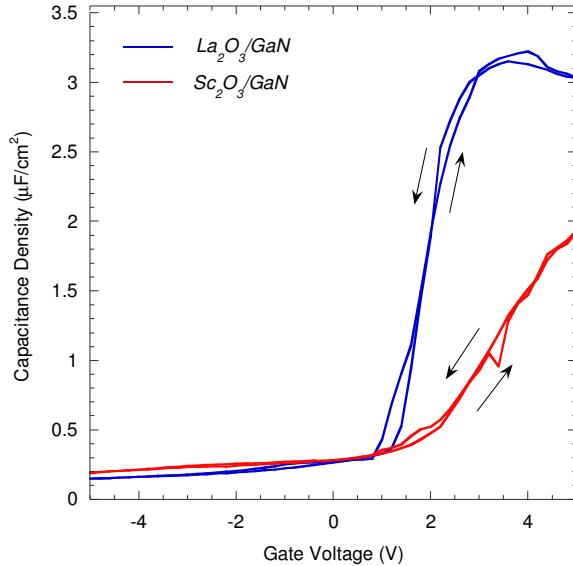


Figure 7.4: Corrected C-V measurements for MOS capacitors with 100 Å La_2O_3 and Sc_2O_3 .

Based on the systematic error analysis for the capacitance obtained via the three-element model, Fig. 7.5 a-b shows the corrected capacitance with error bars for both La_2O_3 and Sc_2O_3 , respectively. The error associated with the Sc_2O_3 film capacitance ranged between 5-15.9%, while La_2O_3 film error was much larger and ranged between 5-80%.

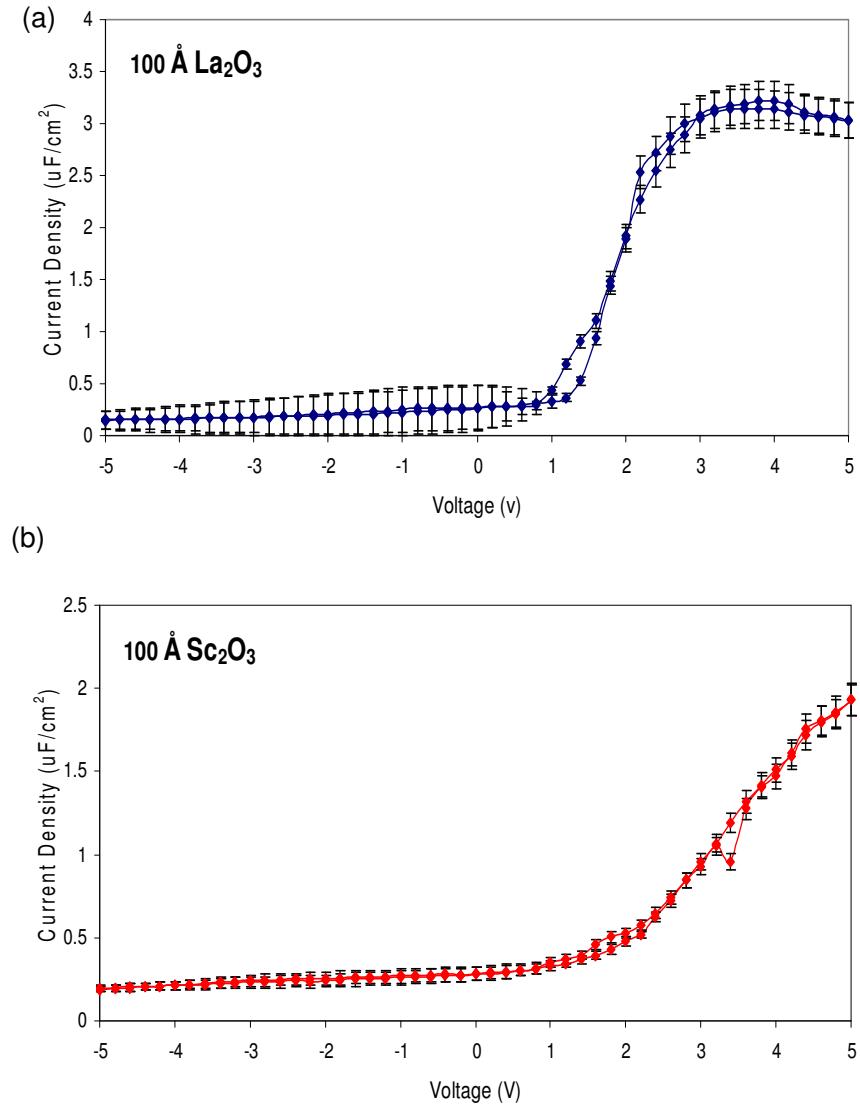


Figure 7.5: Error in C-V measurements resulting from three-element model correction for (a) 100 Å La_2O_3 and (b) 100 Å Sc_2O_3 .

Dielectric constants were determined for the films using the equation,

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox} A}{t_{ox}} \quad (7.13)$$

where ϵ_0 is the permittivity in a vacuum, C_{ox} is the oxide capacitance, A is the cross-sectional area of the oxide, and t_{ox} is the oxide thickness. Table I shows the calculated dielectric constants for Sc_2O_3 and La_2O_3 were 21.1 and 35.6 respectively, which are much larger than

the previously reported values ⁶⁻¹². Along with error in the capacitance, error in the dielectric constant also arises from the measurements of the device area and oxide thickness. The device area error analysis results in 6% error from the measurement of the diameter and determination of where the diameter was on the circular device. In addition, TEM images show that observed oxide thicknesses vary approximately 3% from the expected values. Again using the progression of standard error, the total deviation for the dielectric constants is 7.8% for Sc_2O_3 and 9.0% for La_2O_3 .

Table I: Electrical properties for Sc_2O_3 and La_2O_3 determined from C-V measurements

	ϵ predicted	ϵ measured	$Q_{chan.}(\text{cm}^2)$
Sc_2O_3	14	21 ± 2	2E13
La_2O_3	25-28	36 ± 3.5	5E13

Even with error taken into account, La_2O_3 still has a dielectric constant of at least 32.5, which is higher than the theoretical value of 27. Cubic and hexagonal La_2O_3 have been shown to exhibit dielectric constants of $\epsilon = 16\text{-}17$ and 25-27 respectively ⁹. Thus, the presence of the cubic phase in these films, confirmed by XRD, should result in a lower than theoretical dielectric constant. Zhao et. al. ¹³ also showed that La(OH)_3 has an even lower dielectric constant of 10. In the previous chapter, it was shown that the tantalum cap was not an effective barrier to atmospheric water and carbon dioxide over time. Therefore, the La_2O_3 film could possibly contain some hydroxide, which should also reduce the dielectric constant. The fact that a higher dielectric constant is noticed for this sample could be an effect of two structural properties. Jun et. al. ¹⁴ showed that when oxygen is absorbed by La_2O_3 films, the films become denser and result in an increase in dielectric constant. XPS ratios for La_2O_3 showed an oxygen-rich film, which could account for the higher permittivity value. In addition, an interfacial layer was produced during deposition of the oxides. It is possible that this layer (most likely lanthanum-gallium oxide) may have an influence on the permittivity causing it to appear higher than theoretical values. Further C-V testing is needed to explicitly determine the effect of structural properties on the dielectric constant.

Table I also shows a large channel charge associated with both La_2O_3 and Sc_2O_3 . These values were obtain using the expression,

$$Q_{chan.} = \int CdV . \quad (7.9)$$

The larger channel charge seen for La_2O_3 could be a result of its higher dielectric constant. Yet, Gila et. al.¹⁵ suggested that the increase in sheet carrier density is an effect of reducing surface traps, effectively allowing more carriers in the channel. The hysteresis window for both films is approximately 0.3 V, indicating good film quality. This is consistent with previous reports for $\text{Sc}_2\text{O}_3/\text{GaN}$ capacitors⁶. Even though La_2O_3 was shown to have a more unordered defective structure than Sc_2O_3 , the hysteresis windows are the same. La_2O_3 was also previously shown to leave GaN unpinned, suggesting good passivation of interface traps, which is consistent with the C-V results. The interfacial layer seen in La_2O_3 TEM images may also play a role in reducing the number of interface charges. Therefore, it is unlikely that a variation in interface trap densities is responsible for the channel charge difference between the two films.

Large accumulation channel charges are vital to the operation of rf-devices where high-speed switching is needed. Presently, AlGaN/GaN high electron mobility transistors (HEMTs) with channel charges of $1.5 \times 10^{13} \text{ cm}^{-2}$ are being investigated and manufactured for these high frequency applications¹⁶. MOSFETs with equivalent channel charges would be adventitious since appropriate gate oxides could provide larger barriers to minority carrier injection, resulting in lower leakage currents than the Schottky-gated HEMTs. Therefore, the presence of a substantial charge accumulation layer and small hysteresis window points to the viability of these films in enhancement-mode MOSFETs.

7.3 Current-Voltage (I-V) Results and Discussion

Preliminary I-V results are shown for 50 Å La_2O_3 and Sc_2O_3 films in Fig. 7.6. In Fig. 5.5a, it was observed that the use of a $\text{K}_2(\text{SO}_4)_2$ clean prior to oxide deposition resulted in an order of magnitude reduction in leakage current. Therefore, all the samples discussed in this section have the acid pretreatment.

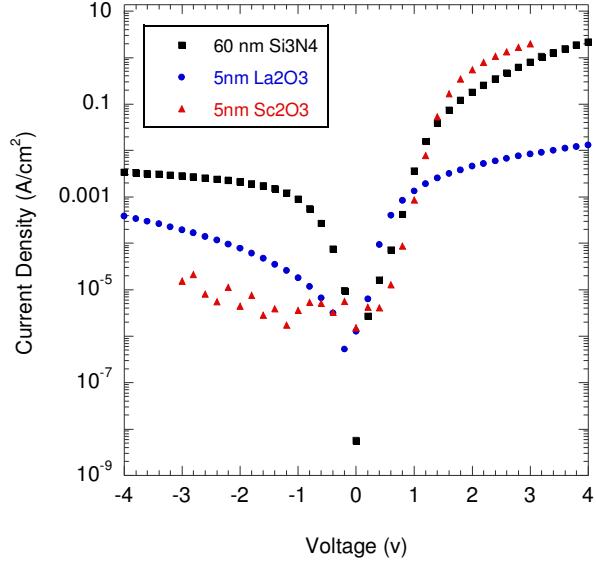


Figure 7.6: I-V leakage currents for 50 Å La_2O_3 and Sc_2O_3 films compared to 600 Å Si_3N_4 films.

Both Sc_2O_3 and La_2O_3 exhibit better leakage than Si_3N_4 when thicknesses of the film are taken into account. Comparison of the leakage current density at 1V with previous reports for $\text{Sc}_2\text{O}_3/\text{GaN}$ can be seen in Table II below. The only current density data reported for La_2O_3 is on silicon and therefore not pertinent to this discussion. Sc_2O_3 data reported in this work is reasonable with previous work considering the inverse linear relationship between leakage current density and oxide thickness. Therefore, for a much thinner oxide tested here a much larger current density is expected.

Table II: Comparison of $\text{Sc}_2\text{O}_3/\text{GaN}$ leakage current with previous reports

Reference	Sc_2O_3 thickness (nm)	Current Density (A/cm^2)
Liu et. al. ⁶	120	~1E-8
Mehandru et.al. ⁷	100	~1E-7
<i>This work</i>	5	8E-4

Since Sc_2O_3 has a larger conduction band offset than La_2O_3 , a lower leakage current would be expected from these films. TEM images (Fig. 6.5) show that the Sc_2O_3 has

periodic dislocations propagating from the interface with GaN, which was assumed to be between the twinned domains. However, in the La_2O_3 TEM images (Fig. 6.16) the dislocations and grain boundaries seemed to be blocked from the interface by an interfacial layer between La_2O_3 and GaN. Therefore, this interfacial layer is assumed cause the lower leakage current seen in Fig. 7.6. In addition, La_2O_3 was shown to effectively leave an unpinned GaN interface, while the Sc_2O_3 films still had a slight bit of pinning present. This pinning is indicative of traps or charges within the oxide film. Trapped charges within the oxide can distort the band edges, and increase the electric field in the oxide near the gate¹⁷. Therefore, the tunneling barrier is effectively less than with an unpinned interface (Fig. 7.7). In reality there is no immediate need for oxides this thin in GaN-based power devices. Thus, the leakage currents in functional devices should be much smaller than illustrated here. Leakages current densities exhibited by both ultra thin La_2O_3 and Sc_2O_3 indicate their potential as gate oxides in GaN-based MOSFETs.

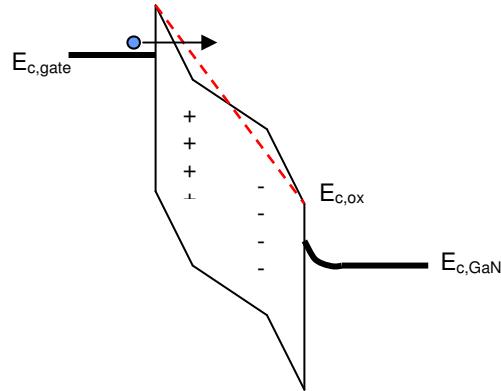


Figure 7.7: Effect of trapped charges (or pinned interface) on the oxide barrier to tunneling. The dashed line represents tunneling barrier without charge when biased.

7.4 Conclusions

MOS capacitors were fabricated with both La_2O_3 and Sc_2O_3 gate oxides. C-V curves showed large charge accumulation layers, extremely high permittivity values, and low hysteresis windows indicative of low density of interface traps and fixed oxide charges. I-V curves showed a reduction in leakage current density for both oxides when compared to Si_3N_4 , which is readily used as a gate dielectric for GaN devices. The greater reduction

achieved with La_2O_3 films is attributed to an interfacial layer that passivates the interface with GaN and minimizes the amount of dislocations propagating into the oxide. The preliminary results presented in this chapter point to the viability of these gate oxides in MOS devices.

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8. Conclusions and Future Work

In this thesis, rare earth oxides, La_2O_3 and Sc_2O_3 , were explored as potential gate dielectrics for GaN-based MOS devices. Surface treatments were tested as means of controlling GaN surface termination and contamination prior to oxide deposition. Structural and electrical characterization of La_2O_3 and Sc_2O_3 was conducted by a variety of analysis techniques. Therefore, this chapter presents a compilation of results and conclusions, as well as offers suggestions for future work.

8.1 Conclusions

GaN surface preparation experiments were conducted using KOH and $\text{K}_2(\text{SO}_4)_2$ to test their ability to effectively passivate, clean, and leave a reproducible GaN surface termination. The conclusions of this work are as follows:

- KOH chemical treatment resulted in a nitrogen terminated surface that limited oxidation and retained other contaminates, making it a poor choice for device fabrication.
- $\text{K}_2(\text{SO}_4)_2$ chemical etch produced a gallium terminated surface that increased oxidation while reducing other contaminates. The resulting oxide was shifted to a lower binding energy indicating a change in bonding that yields a gallium-rich GaO_x layer.
- HF was used to produce a clean GaN surface that exhibited 0.6 eV of upward band bending. By treating the GaN with the $\text{K}_2(\text{SO}_4)_2$ upward band bending was increased by 0.4 eV. This increase in barrier should result in lower leakage currents, and should be considered when determining dielectric band offsets with GaN.
- MISFETs fabricated with the $\text{K}_2(\text{SO}_4)_2$ treatment resulted in an order of magnitude reduction in leakage current, increased source-to-drain current, increased

subthreshold slope, increased peak transconductance, reduced hysteresis windows, and better pinch-off. These improvements in device performance was attributed to the thin GaO_x layer passivating the surface while still allowing or even promoting quality deposition of dielectric films.

Rare earth oxides have a combination of large band gaps, permittivity, and thermal stability making them a good candidate for GaN-based MOS devices. Therefore, the majority of this thesis was spent structurally and electrically characterizing La_2O_3 and Sc_2O_3 as potential insulator layers on GaN. The conclusions of this work are as follows:

- Epitaxial La_2O_3 was grown for the first time on GaN by MBE.
- Sc_2O_3 was also successfully grown on GaN by MBE.
- Sc_2O_3 exhibited the stable cubic phase with 6-fold symmetry indicative of in-plane twinning. Equal amounts of both twins were observed throughout the film. La_2O_3 exhibited both the stable hexagonal phase and the metastable cubic phase. 6-fold symmetry was acquired across the film verifying the hexagonal phase and indicating twinning within the cubic phase.
- The lattice mismatch with GaN was calculated to be 8.9%, 14.5%, and 18.2% for Sc_2O_3 , cubic La_2O_3 , and hexagonal La_2O_3 , respectively. While Sc_2O_3 showed periodic misfit dislocations, La_2O_3 exhibited a polycrystalline, defective film. This was expected based on the lattice mismatches and phase results.
- An abrupt $\text{Sc}_2\text{O}_3/\text{GaN}$ interface indicates thermal stability on GaN up to 500 °C. Unlike Sc_2O_3 , deposition of La_2O_3 on GaN resulted in an interfacial layer that was presumed to be the orthorhombic LaGaO_3 .
- As-grown La_2O_3 was shown to be very reactive with atmospheric water and carbon monoxide to form lanthanum hydroxides and carbonates. Tantalum and silicon were

explored as *in-situ* capping metals to prevent contamination of La_2O_3 films. Tantalum capped films showed some degradation over time, while silicon capped films provide to be a sufficient barrier for at least one month. A good capping layer must be easily incorporated into the device structure, which has yet to be tested for the superior silicon cap.

- Band offsets for Sc_2O_3 were determined by XPS to be 0.8 eV and 2.1 eV for valence and conduction band offsets, respectively. La_2O_3 exhibited a valence band offset of 1.9 eV and conduction band offset of 0.9 eV. La_2O_3 provides a more effective barrier to holes, while Sc_2O_3 is a better barrier for electrons. Yet, both oxides exhibit sufficient barriers to prevent thermionic emission of carriers at high operation temperatures.
- Preliminary C-V data corrected with the three-element model was used to calculate a dielectric constant of 21 ± 2 and 36 ± 3.5 for Sc_2O_3 and La_2O_3 , respectively. These are larger values than previously reported and could indicate a textured film. The high dielectric constant of La_2O_3 could be a result of an oxygen-rich film that was observed with XPS or the interfacial layer that was not considered in these calculations.
- Large accumulation layers ($2 \times 10^{13} \text{ cm}^{-2}$ and $5 \times 10^{13} \text{ cm}^{-2}$) were found for both oxides. This is a result of high dielectric constants and low density of interface traps. Both of these oxides have larger charge densities than current commercialized AlGaN/GaN HEMTs, which points for the viability of these oxides for high frequency switching devices.
- Preliminary I-V data shows improved leakage currents for both Sc_2O_3 and La_2O_3 compared to the more conventional Si_3N_4 dielectric. This improvement is a result of large band offsets and good epitaxial passivation of the interface. La_2O_3 shows a larger reduction in leakage current than Sc_2O_3 , which is assumed to be a result of the interfacial layer form during deposition. XPS showed that the interface was left unpinned after La_2O_3 deposition.

These results show the potential of both Sc_2O_3 and La_2O_3 as gate oxides in GaN MOSFETs. Recently, gate dielectrics have been incorporated in HEMT devices to reduce the current collapse and leakage current that inhibit the success of these devices. Therefore, these oxides could be incorporated not only MOSFETs, but other GaN devices to improve reliability and performance.

8.2 Future Work

Further investigations should be conducted on oxide/GaN interface by TEM to determine the nature of the defects within the oxides. This could illicit the crystal structures of the grains within La_2O_3 and determine if the misfit dislocations are occurring between oppositely twinned domains in Sc_2O_3 . In addition, the character of the interface formed as La_2O_3 is deposited could be determined. XPS on La_2O_3 films with small increments in thickness should also be used to verify the stoichiometry and bonding of the interfacial layers.

Presently, MOSFET devices are being fabricated on bulk GaN and GaN template (thick HVPE GaN layers on sapphire) substrates with varying thicknesses of La_2O_3 and Sc_2O_3 gate oxides. The results presented in Chapter 7 are merely preliminary, so the electrical characterization of these new devices would offer further details of the oxide behavior in MOSFETs. These devices could provide the means for calculating effective mobility and density of interface traps (D_{IT}), which is a clear indicator of passivation ability that cannot be obtained from MOS stacks. In addition, these substrates should result in lower dislocation densities within the active gate region leading to better device performance. Various *in-situ* capping materials for La_2O_3 could also be explored to systematically define the best gate stack for preventing contamination and yielding a good work function. This could either be a better metal or a combination of various oxides. La_2O_3 could be incorporated with other rare earth oxide get both a good interfacial layer and a sufficient barrier to atmospheric contaminates that could cause degradation in these films. This would be beneficial in achieving good gate control that would produce a viable MOSFET device for high frequency, high temperature, and high power devices.

APPENDICES

The basic operating procedures for XPS and XRD are contained within the following appendices. These procedures will also be discussed in terms of sampling needs for similar samples to those discussed in this thesis.

A. XPS Operation Procedures

XPS spectra were collected using the Analytical Instrumentation Facility at North Carolina State University. The basic operation procedure supplied by AIF is the first section of this appendix. This procedure is directly from Fred Stevie at AIF and can be obtained by contacting him at fred_stevie@ncsu.edu. The second section will provide general suggestions for the spectra collected pertaining to GaN, Sc₂O₃, and La₂O₃.

A.I. XPS Basic Operation procedures for Riber LAS-3000:

BASIC XPS OPERATION

Spot size: 2-3 mm diameter **Version: 7/7/06**

Max # of samples per load: 5

Sample size: ~1cm square

Sample positions:

Load/Exchange: Θ=~227 degrees, X=20.66, Y=12.84, Z=17.67

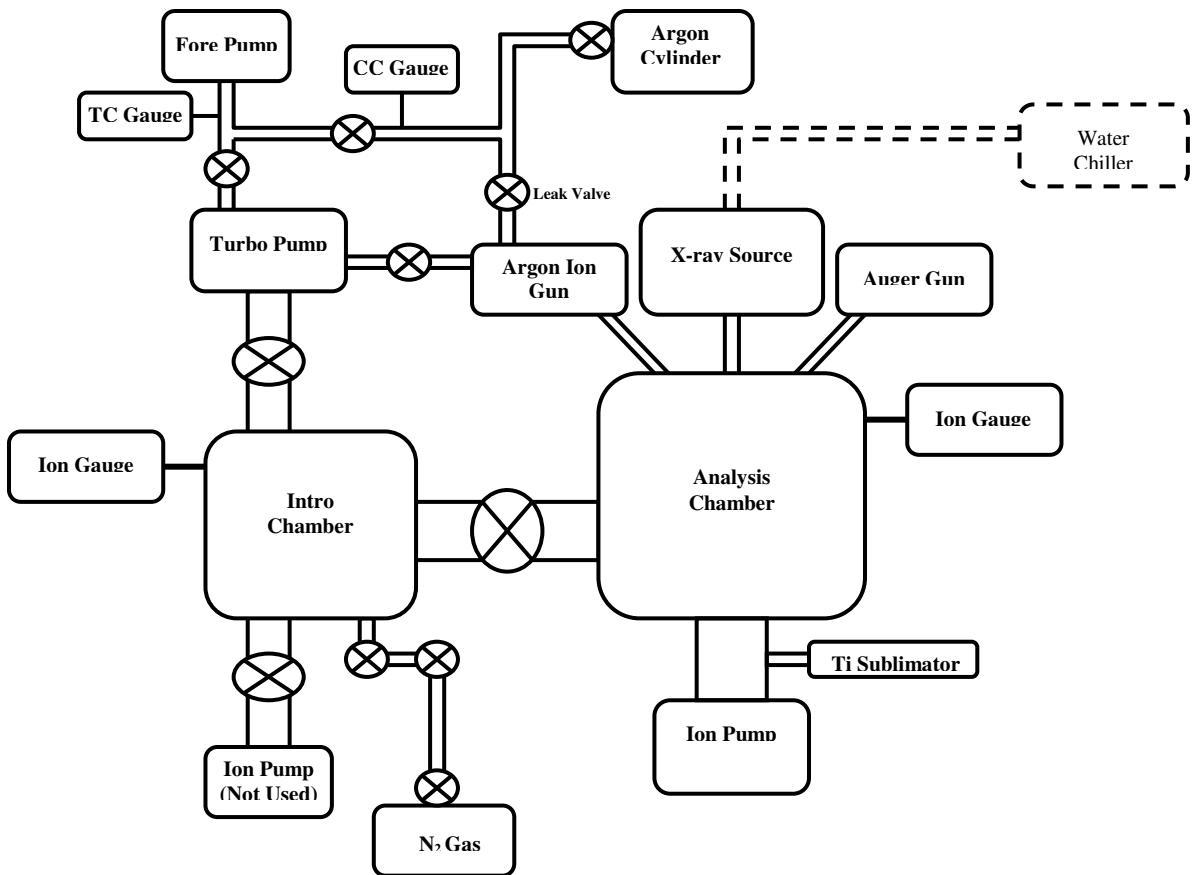
Analyze center of holder: Θ=0 degrees, X=20.0, Y=13.32, Z=17.5

Paper Holders (center): Θ=0 degrees, X=19.0, Y=13.32, Z=18.0

Top Corner: Θ=0 degrees, X=18.3, Y=13.32, Z=14.25

Procedure Outline

- A. Sample Exchange
- B. Electron Gun Operation (image sample –beware electron damage)
- C. Ion Gun Operation (sputter sample)
- D. X-ray Operation
- E. Data Acquisition
- F. Shutdown



A. Sample Introduction / Exchange

Make certain each sample is firmly mounted to holder. Sample cannot extend past edge of holder. Optimum analysis location is edge opposite transfer pin.

- 1) Turn off introduction chamber gauge controller filament (switch under green light). Wait 3 min for filament to cool.
- 2) Close valve to turbo pump. Make certain gate valve to analyzer chamber is closed.
- 3) Open nitrogen tank (cylinder and delivery valves, normally left open) ~1psi, open lower N₂ valve, unscrew sample window knob, then open upper vent valve with torque wrench.
- 4) Wait till chamber fills with N₂, then open window and load samples. Verify that samples fit firmly into sample holder; if not, raise clips on both sides of sample with a clean screw driver.

- 5) Check o-ring on sample window and remove any particles, then replace o-ring, center window top to bottom, close window, tighten knob finger tight
- 6) Close lower N₂ valve. Close upper vent valve, torque upper valve to 100 in-lbs.
- 7) Turn off turbo (**Stop** button on turbo controller). Slowly and carefully open the gate valve to the turbo (open until the gate clicks and the turbo slows down in response to the new pressure; then **slowly** open the valve the rest of the way). Then turn on turbo (**Start** button), wait for turbo to reach full speed (normal operation LED will light). Turbo normally reaches full speed in about two minutes. If turbo is not at full speed in 3 minutes, o-ring is probably leaking (if so, need to close turbo gate valve and vent sample chamber again).
- 8) After 5 min, turn on the filament on the introduction chamber ion gauge. If pressure reaches 10⁻⁶ torr range, leave filament on, otherwise turn off and try again in about 5 min.
- 9) Note: the ion pump gate valve is always kept closed (the ion pump is not used).
- 10) Wait for introduction ion gauge pressure reading to reach less than 5x10⁻⁷ torr before transferring sample into the analysis chamber.
- 11) Put sample on rod. Loosen set screw on rotation stage. The stage must be free to rotate.
- 12) Open gate valve between intro and analysis chambers.
- 13) Move rod in and insert sample into the slot on the rotation stage (firmly but without significant force) which must be at the extraction position. Both hands are required – one hand on the rotation stage and one hand on the transfer rod at the same time. Remove rod from sample; retract rod fully into introduction chamber. Close gate valve between intro and analysis chambers. Move sample to analysis position. Tighten set screw.

B. Image Sample: E-BEAM OPERATION (to align sample on video monitor) (optional)

- 1) Turn on monitor. Make sure electron multiplier (V. Multi on the TCE300) is **OFF!**

- 2) Turn Auger HV on. (Riber E-gun power supply chassis, "H-V" button)
- 3) Press Reset button near 2707 gauge on tan Brandenburg controller panel. Should read 5 kV.
- 4) Turn on Auger filament. (E-gun power supply, "Filament" button) (0.4 mA emission)
- 5) Turn on ABC 50 Auger Scan Power Supply
- 6) Turn High Voltage up until you obtain secondary e^- image on video monitor. (noisy potentiometer)
- 7) Align sample with stage translation Z and X knobs until sample is aligned with marks on monitor. **Do not adjust Y-axis or θ to align sample to avoid striking analyzer.**
- 8) Turn High Voltage down. Turn off ABC50 to avoid interference. Turn off filament (push and pull button). Turn off HV (push and pull button). Turn off monitor.

C. ION GUN OPERATION (optional)

- 1) Electron Multiplier must be off. X-ray source must be shut down: Turn X-ray anode filament current down (use emission current). Turn HV down. Turn power off ("Power" button on X-ray control).
- 2) Turn off intro ion gauge filament.
- 3) (If the gas line has already been pumped and pressurized with Ar, skip to 5. If not, proceed with the following)

Pump out gas line:

Close turbopump foreline valve, check that Argon gas cylinder valve is closed, open Ar ion gun pump line valve and pump Ar gas line up to the regulator. Pump until vacuum is better than 5×10^{-2} Torr as measured on Leybold foreline gauge. Close Ar ion gun pump line valve.

- 4) Open Ar delivery valve and Ar tank valve (on floor below Ion Gun) to pressurize the regulator and gas line. Ar regulator should go to about 10 psi. Close Ar tank valve (pressure in lines should be enough for one day of operation). Leave Ar delivery valve open. **Open turbopump foreline valve.**

- 5) Close turbopump gate valve. Open ion gun differential gate valve to turbopump
- 6) Adjust leak valve on Ion Gun to admit Argon Gas to Ion Gun at a pressure of about 1.3×10^{-6} . Pressure will equilibrate at about 1.5×10^{-6} torr. Analysis chamber pressure will be around 1×10^{-7} Torr. Open carefully, flow increase is almost exponential with valve opening past a certain point (If you hear buzzing noise, pressure is too high- **REDUCE!**).
- 7) Ensure 8015 Power Supply FILAMENT CURRENT controls set for normal (this is maximum value). Electron Energy = 70 V.
- 8) Ensure 8015 Power Supply EMISSION CURRENT control is set to $50\mu\text{A}$. (% of range = 100)
- 9) Set 8015 Power Supply to ON.
Set EXTRACTOR to HIGH
Set ION ENERGY to suit application. (two full turns per kV, 6.0=3kV, usually set to 10.0 turns or 5kV)
- 10) Set 346 SAX to ON (Beam energy) and adjust front panel controls as follows:
Mode switch to AUGER
SWEEP switch to INT
(MAGNIFICATION switch to Var (5.2 turns for X and 0 turns for Y, for 3 mm x 3 mm area – Page 75 in lab notebook for other settings).
Typical values: X shift = 5.00 and Y shift = 4.00.)
- 11) Setup 8015 Power Supply as follows:
Set FILAMENT switch to ON, the indicator will illuminate.
Increase EMISSION CURRENT to 5 mA.
Set HV switch to ON, the indicator will illuminate.
To sputter: move switch from PC to beam on (beam on light will come on) ~2 min to clean carbon off surface, ~7 min to remove native oxide
- 12) Ion Gun shutdown (set switch on box to beam off)
On 8015:
Set EMISSION CURRENT RANGE switch to $50\mu\text{A}$ position
Set Filament switch to OFF, the indicator will extinguish
Set HV switch to OFF, the indicator will extinguish
Set POWER switch to OFF, the indicator will extinguish
On 346 SAX:
Turn power off
After 1 minute turn the gas supply OFF (close Ar leak valve)

After 2 minutes close gate valve between differential line and turbo
(Ar ion gun differential valve)
Open turbo gate valve. Turn on intro ion gauge filament.

D. X-Ray Operation

Make sure MAC2 sweep switch is on COMPUTER (not MANUAL).

Ensure that the [Scan generator MAC2] power supply is on for 0.5 hour warm-up (usually the chassis is left on, so this step is not required). To turn on, flip red toggle switch on controller. (rack next to Intro chamber)

- 1) Need water flow and vacuum for x-ray source (otherwise X-Ray HV will not turn on)
 - (1) Vacuum – on analysis gauge controller, set power knob below red LED from AUTO to ON, then set scaling knob on right to “ESCA log”.
 - (2) Water – turn toggle switch named “cooler” (top of vacuum rack at right of system) to “on” position. (red light on wall over flow meter must go on and flow meter will spin to indicate water is circulating) Pressure normally about 30 psi.
- 2) X-RAY STARTUP

First zero filament and emission current knobs and HV knob (turn all the way CCW). Turn on two lighted switches on controllers:

Power on X-ray control.

HV ON on X-ray supply.

(Power on X-ray supply normally left ON)

If X-ray controller light doesn't light – vacuum problems

If X-ray HT supply doesn't light – water problems

Turn large black HV knob to 12kV.

Turn "MODE" switch to left.

Increase "FILAMENT CURRENT" knob first until you see an emission current of about 5mA. (~3.4A filament current.) DO NOT GO HIGHER THAN 3.8A!!!!!!

Make 1 blind turn on "EMISSION CURRENT" knob, then turn "MODE" switch to the right.

Turn up emission current to red dot (~15mA).

Correct X-ray HV power supply voltage to 12kV.

Turn on electron multiplier (push in V. Multi. Button)

3) SHUT DOWN

Turn off electron multiplier ("V-Multi" on TCE-300) and shut down X-ray gun when exchanging samples.

- 1) Turn down Emission Current.
- 2) Zero Filament Current knob then switch mode to left (Filament Current)
- 3) Turn down big black HV knob to zero.
- 4) Turn off power switch.

E. Data Acquisition

- 1) When using Spectra for the first time, move open window and read Labbook instructions in window.
- 2) Default directory for data storage is C:\Wspectra unless you specify a different directory – **it is highly recommended that you save your data in a folder in C:\XPSdata.**
- 3) Load in a file before starting.
Select "Edit Region" icon on toolbar (toggles the "Edit Regions" window).
Energy window 1 is commonly used for survey scans 1200-0 (Mg) or 1400-0 (Al).
Energy windows 2-9 are for specific analysis regions you set up.
Enter values for Start, End, Step size, #scans, Dwell time, and label the region under Tag column for clarity when analyzing data.
Close by icon on toolbar.
Toggle check marks in toolbar for windows you have set up to run.
- 4) Typical resolution energies for Analyzer are VF1 = 2.0 (VF2 = 4.75) for survey scan (~ 2eV) and for subsequent energy windows VF1 = 1.0 (VF2 = 3.0) for ~ 1eV resolution.

Typical Settings for Survey and Window Scans							
	Start	End	Step	Scans	Dwell	Pass	Tag
Survey	1200.0	1.0	-1.0	3	0.1	20.0	Survey
Window	540.0	520.0	-0.1	3	0.5	20.0	O -1s
Window	295	275	-0.1	3	0.5	20.0	C – 1s

- 5) Turn on the electron multiplier (“V.Multi” on the TCE300) for data acquisition.
Press GO icon on toolbar.
If you need to pause or abort, press “Kill” icon on toolbar.
Use the “Rescale” icon on toolbar for full scale presentation.
- 6) Position mouse cursor over peaks of interest to read coordinates in toolbar during acquisition.
Use “Edit Regions” button on toolbar to select energy windows.
- 7) When data capture is complete, press “SAVE DATA” icon in toolbar and enter lab book name.
Enter comments about scan (anode, survey or window, sample name) and press “OK”.
- 8) From Windows taskbar, select lab book.
Verify file and comments, then press CLOSE LABBOOK icon on toolbar (writes data to disk, doesn't exit program).
- 9) Continue collection of data for desired number of windows and samples.
Turn off electron multiplier (“V.Multi” on the TCE300) when not acquiring data.
- 10) When finished with analysis for the day, turn off TCE300 V.Multi and from lab book window press CLOSE LABBOOK to verify data is stored.
- 11) Exit software.

F. Shut-down Procedures

- 1) Turn off electron multiplier (“V. Multi” button on the TCE300).
- 2) Turn down X-ray emission current; Turn down X-ray filament current; switch mode
- 3) Turn down X-ray HV.

- 4) Turn off X-ray filament power switch, (this turns off X-ray HV switch).
- 5) Ensure that the e-gun filament and HV are turned off. Make sure that filament current, emission current, and X-Ray HV are turned all the way CCW (reset to zero).
- 6) Ensure that the secondary electron detector HV is turned off ("High Voltage" knob on ABC50).
- 7) MAC2 Analyzer Scan Generator switch to left Manual (Interne).
- 8) Switch Analysis chamber vacuum gauge controller knob under red LED to AUTO, then move the scaling knob on the right from the "ESCA log" setting to enable auto scale for chamber vacuum. Leave the X-ray water cooling running for ~20 minutes after shutdown.
- 9) Switch OFF X-ray cooling water after 20 minutes.
- 10) Remove sample from analysis chamber (reverse of procedure A steps 15-16).
- 11) Put information in XPS users log, including the date of analysis, your name, phone number, charge account number, and time spent on instrument.

G. Computer

After turn on: cd windows
 Win Password: dale

H. Instrument Specifications (RIBER LAS-3000)

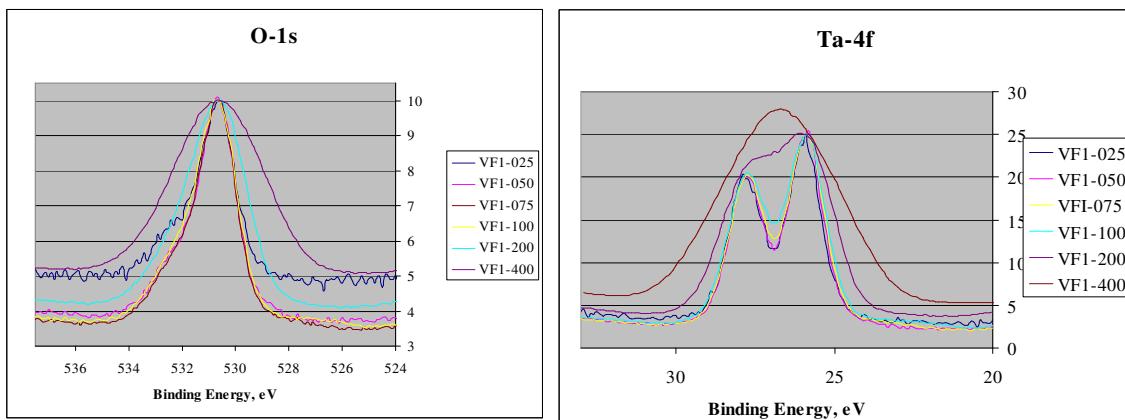
- 1) Take off angle: $\sim 75^0$ from surface (typical designation), 15^0 from normal
 Based on theta= 356^0 . Actual angle is 360^0 . MAC-2 Analyzer (similar to CMA).
- 2) Information depth (X-ray depth): $1-5 \text{ nm } 3\lambda\sin\theta$ (λ -mean free path)
- 3) Angle at which X-rays hit sample: $\sim 20^0$, $\sim 55^0$ x-ray source to analyzer
- 4) Detection limits: 0.1 to 1%
- 5) X-ray source: Mg K α (1253.6 eV)
- 6) Focusing Information (for O-1s peak and Ta-4f peak): use 2, 4.75 for survey

VF1	VF2	FWHM (eV)	Intensity (k)
4	7	3.8038	142
2	4.75	2.5735	76
1	3	1.9017	28.3
0.75	2.25	1.7335	16.87
0.5	1.8	1.6817	7.53
0.25	1.5	1.5984	2

VF1= 2, VF2= 4.75 is for typical survey.

VF1= 1, VF2= 3 is a typical higher resolution energy range

VF1= .5, VF2= 1.8 is the maximum useful energy resolution



NIST Database

srdata.nist.gov/XPS/index.htm

A.II. XPS Considerations for the Materials in this Thesis

A. Survey Scans:

Survey scans were taken with the analyzer set to VF1=2.0 and VF2= 4.75, which yields a resolution of ~2 eV. All survey scans have an energy range of 1200-0 eV with a step size of -1.0 and a dwell time of 0.1. Three scans are taken for each sample to produce the survey scan. Casa XPS software is then used to determine and label the elements present.

B. High Resolution Scans for GaN:

Typical high resolution scans were taken with the analyzer set to VF1 = 1.0 and VF2 = 3.0 to yield a resolution of ~1 eV. The table below shows the range of energies scanned for each necessary GaN peak and the number of scans needed for that energy range. The O1s peak is included since this was often considered for Ga_2O_3 surface bonding with MOCVD grown GaN. In addition, surface cleans looked at the O1s peak for cleaning ability and remaining oxide bonding. A high resolution carbon peak is needed in order to calibrate the sample since GaN is an insulating sample in which binding energies are shifted as the sample charges. Valence band maximum scans for all samples can be done in the range noted in the table below. More scans are needed for this measurement to ensure a smooth linear turn on region, which is needed to determine the presence of surface band bending and correct band offset measurements.

	<i>Start</i>	<i>End</i>	<i>Step</i>	<i># of Scans</i>	<i>Dwell time</i>	<i>Pass</i>
$\text{Ga } 2p_{3/2}$	1125	1110	-0.1	10	0.5	20
$\text{Ga } 3d$	25	15	-0.1	10	0.5	20
$N1s$	405	390	-0.1	10	0.5	20
$O1s$	540	520	-0.1	10	0.5	20
$C1s$	292	277	-0.1	8	0.5	20
$VBM (E_v)$	15	0	-0.1	15-20	0.5	20

C. High Resolution Scans for Sc_2O_3 :

Similar analyzer settings were used for high resolution Sc_2O_3 scans as for GaN samples. A calibration C1s spectrum was taken for each sample using the conditions in the table above. For band offset measurements a valence band maximum spectra was taken under the conditions in the previous table.

	<i>Start</i>	<i>End</i>	<i>Step</i>	<i># of Scans</i>	<i>Dwell time</i>	<i>Pass</i>
$\text{Sc } 2p_{3/2}$	415	390	-0.1	8	0.5	20
$\text{Sc } 2s$	510	495	-0.1	10	0.5	20
$\text{Sc } 3s$	57	47	-0.1	12	0.5	20
$\text{Sc } 3p$	35	25	-0.1	12	0.5	20
$O1s$	540	520	-0.1	10	0.5	20

D. High Resolution Scans for La_2O_3 :

La_2O_3 high resolution spectra were taken in a similar method using the conditions and ranges below. A calibration spectrum was taken for each spectrum and those used for band offset measurements also had the VBM measured using the conditions list in the section for GaN scans.

	<i>Start</i>	<i>End</i>	<i>Step</i>	<i># of Scans</i>	<i>Dwell time</i>	<i>Pass</i>
$\text{La } 3d_{5/2}$	865	830	-0.1	8	0.5	20
$\text{La } 4d_{5/2}$	110	90	-0.1	10	0.5	20
$\text{La } 5s$	42	32	-0.1	12	0.5	20
$\text{La } 5p_{1/2}$	30	10	-0.1	10	0.5	20
$O1s$	540	520	-0.1	10	0.5	20

B. XRD Operation Procedure

XRD is a characterization tool with several different setups, in order to collect a variety of data. The following sections will describe the procedure for the basic θ - 2θ spectra that will give the sample crystal structure, ω - θ rocking curve scan that shows crystal quality, and phi scans that give the crystal symmetry. The first section will include θ - 2θ and ω - θ rocking curve instructions for the Philips X'Pert PRO MRD HR-XRD system which was described in Ch. 4 and available for general use at the Shared Materials Instrument Facility at Duke University. These operating procedures can be obtained from the SMIF website at <http://smif.lab.duke.edu/>. The second section will give the θ - 2θ procedure for the Bruker XPS system described in Ch. 4 and give a brief description of how to obtain phi scans.

B.I. θ-2θ Setup and Procedure using the Philip X'Pert PRO HR-XRD system:

Phase Analysis

1. Log into the User Log System on the SMIF web site

Hardware Setup

2. *X-Ray Tube*

Traditionally the line focus of the x-ray tube is used to collect phase measurements because the line focus has less divergence than the point focus and allows a larger area of the sample to be covered.

Note on Optics:

There are two options for the incident and diffracted optics:

Standard Configuration (for powder samples or samples with rough surfaces)

- Mirror on the incident side and parallel plate collimator (PPC) on the diffracted side
 - The mirror produces a parallel beam onto the sample, and a parallel beam out of the sample. The mirror also reduces the K-beta X-rays better than the FDS.
 - This set of optics results in higher intensities, but lower resolution (0.27 degrees)

For extremely flat and reflective samples:

- Fixed divergence slit (FDS) on the incident side and programmable receiving slit (PRS) on the diffracted side
 - The FDS produces a divergent beam and relies on the sample to focus the beam into the PRS.
 - This set of optics gives higher resolution (0.02 degrees), but results in lower intensities.

The rest of the procedure is written assuming the Mirror and PPC optic modules are used.

3. *Incident Beam Optics*

- Mount the mirror on the incident beam PREFIX. Make sure that the attenuator cable is plugged into the mirror.
- Insert the $\frac{1}{2}$ degree slit in the mirror optics, and verify that there is no manual beam attenuator in place.
- If the sample height is less than 25 mm insert an appropriate beam mask.

4. *Diffracted Beam Optics*

- Mount the parallel plate collimator (PPC) PREFIX
 - Verify that the 0.04 rads soller slits are behind the collimator and that detector 1 is present.

User Setup

5. Open the X'Pert Data Collector program.
6. Enter your user name and password.
7. Select **Instrument/Connect** from the pull down menu. The Connect box will appear.
8. Select the "Generic" configuration. Click the OK button
9. Click the OK button to close the status messages that appear
10. Click Yes on the message box that asks if you want to apply the sample offsets

Optics Setup

11. Select the **incident beam optics** tab. Double click on any item in the list.
 - The X-ray mirror should be selected as the PREFIX module.
 - The $\frac{1}{2}$ degree divergence slit, and the used mask size (if any) should be selected.
 - The beam attenuator will be the Ni 0.125mm automatic with a usage of preset intensity, an activate level of 550,000, and a deactivate level of 400,000. Check that the correct attenuation factor is displayed for the mirror attenuator. If not, select the correct attenuation factor.
 - All other selectable optics components will be set to none.
 - Click OK.
12. Select the **diffracted beam optics** tab. Double click on any item in the list.
 - The parallel plate collimator (PPC) should be selected as the PREFIX module.
 - The soller slits will be set to 0.04 rads,
 - The detector will be mini prop large window 1 and the wavelength should be K alpha,
 - All other selectable optics components will be set to none.
 - Click OK
13. Select the **Instrument Settings** tab. Double click on any item related to the generator settings. Set the generator to 45 kV and 40 mA. Then, press OK.

Sample Mounting

14. Double click an item related to the positions.
 - Select the **position** tab
 - Enter 90 degrees in the *psi* field so the sample can be easily mounted on the stage.

- Press the *Apply* button to move the stage. (*Note – the enclosure doors must be closed for the stage to move*)
15. Open the enclosure doors and mount the sample as flat as possible on the stage.
16. Optimize the Z position of the sample using either the dial gauge method, or the beam bisection method as explained below.

Dial Gauge Method for Sample Z position optimization

- Mount the dial gauge on the stage and close the enclosure doors.
- Return the stage to its upright position by setting *psi* to 0 degrees and pressing the *Apply* button.
- Move the z position of the sample stage until the dial gauge reads 1.0. (The small inner dial will read 1 and the large outer dial should point to the 0 at the top of the dial gauge.) Press the *OK* button to close this window.
- Remove the dial gauge and close the doors.
- Return *psi* to 0 degrees
- Click *OK* to close the instrument settings window
- Proceed to Step 17

Beam Bisection Method for Sample Z position optimization

- Make the following changes to the incident beam optics:
 - Remove the ½ degree slit and insert a 1/32 degree slit
 - Select the **incident beam optics** tab. Double click any item to prompt another window.
 - Enter 1/32 for the divergence slit
 - Set the beam attenuator to ‘do not switch’ and ‘activated’. (This will protect the detector during the direct beam intensity measurement).
 - Click the **OK** button.
- Close the enclosure doors and select the **instrument settings** tab. Double click on an item related to the positions. Enter 0 in all fields and click **OK**.

Detector (2theta) Alignment

- Select **Measure/ Manual Scan** from the main menu.
- Enter the following parameters: 2theta in the *scan axis* field, enter 2 in the *range* field, 0.01 in the *step size* field, and 0.1 in the *time per step* field, then click the start button.
- After the measurement is completed, you will find the peak in the scan data and move the goniometer to this position. If two main peaks are present, choose the midpoint between the two peaks. This can be done in one of two ways:
 - Method 1: Allow the software to determine the peak position
 - Press the right mouse button and select **Peak Mode**
 - The software will automatically determine the peak position.
 - Press the “*move to*” button to move the goniometer to the selected position, then click close.
 - Method 2: Manually determine the peak position

- Press the right mouse button and select **Move mode**
- Press and hold the left mouse button until the cursor is placed over the maximum of the peak (or the midpoint between the two main peaks). This will move the goniometer to the selected position.
- Select the **Tools/ Sample Offsets** from the main menu. Enter 0 in the *2theta* field. Press *OK*.

Sample Height (Z) Alignment

- Double click an item related to the **sample stage positions** and enter an approximate position for the Z height. (e.g., 7.5mm for a Si wafer) and click **OK** to move the sample stage..
- In the **manual scan window**, enter the following parameters: Z in the **scan axis** field, 2 in the **range** field, 0.01 in the **step size** field, and 0.1 in the **time per step** field. Then click the start button.
- After the measurement is completed press the right mouse button and select Move mode. The graph will look like two plateau regions connect through a gradual decrease.



- Press and hold the left mouse button until the cursor is placed in the middle of the plateau region where the intensity is half of the full intensity. This will move the sample to bisect the main beam.

Sample Tilt (Omega) Alignment

- Back in the Manual Scan window, enter the following parameters: omega in the *scan axis* field, 4 in the *range* field, 0.01 in the *step size* field, and 0.1 in the *time per step* field, then press the start button.
- After the measurement is completed find the peak in the scan data and move the goniometer to this position as was done for the 2theta scan
- Select Tools/sample offset from the main menu. Enter zero into the *omega* field. Close the window.
- Repeat another Z scan as before and move the sample to bisect the main beam. You do not have to repeat another omega scan after the second Z scan.
- Return the incident beam optics to their original state:
 - Remove the 1/32 degree slit and insert a 1/2 degree slit
 - Select the incident beam optics tab and double click any item
 - Enter 1/2 for the divergence slit
 - The beam attenuator will be the Ni-Foil with a usage of preset intensity, an activate level of 550,000, and a deactivate level of 400,000
 - Click the *OK* button

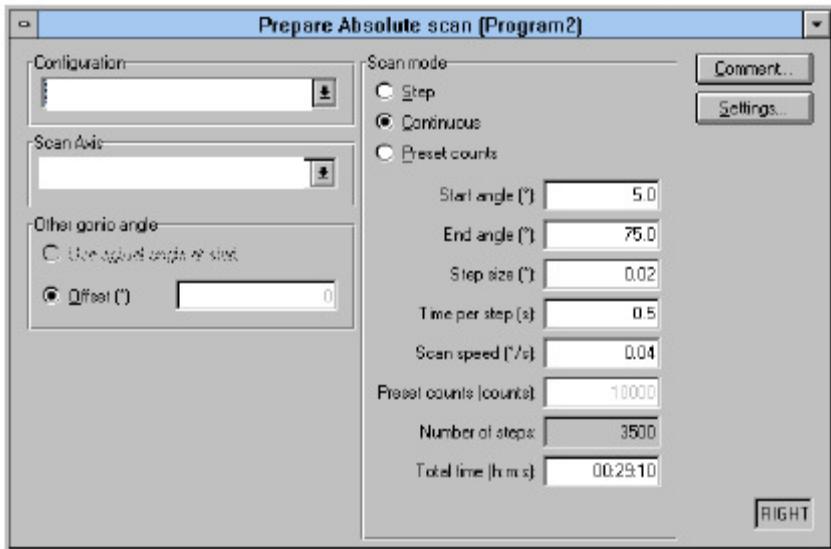
Measurement Programs

XDIF1 Phase Analysis Measurement Instructions

Revision 7
M. Walters
12/21/2007

17. Select **File/New Program/Absolute scan** to create a new program, or **File/Open Program** to load and edit an existing program

18. The window shown below will appear. Enter the information as explained below



- Select the Generic configuration
- The scan axis will be Gonio
- The scan mode should always be continuous.
- The start and end angle should be values based on where peaks of interest are expected for the material being studied. (e.g., 20 degrees to 80 degrees)
- The step size should be chosen based on the resolution of the diffracted beam optics. The time per step should also be determined by the diffracted beam optics. See the table below for recommended step sizes and times per step.

diffracted beam PREFIX	step size	time per step
parallel plate collimator	0.05	0.5 – 1.0
PRS	0.02	0.5 – 1.0

19. Select **File/Save as** and enter a name and description for this scan program and then click the OK button. Close this window.

Measuring

20. Select **Measure/Program/Absolute scan** and the program name used in step 19.
21. Enter a data set name, folder name and sample ID. Click the OK button and the measurement will begin
22. When the measurement is completed, you can view and process the data using the X'Pert Data Viewer Program

Shut Down

23. Unmount your sample from the stage
24. Return the generator settings to the idle values (40kV and 10mA)
25. Exit the software
26. Log out of the User Log System on the SMIF web site

B.II. Rocking Curve Setup and Procedure for the Philip X'Pert PRO HR-XRD System:

ROCKING CURVES WITH A HYBRID

1. Log into the User Log System on the SMIF web site

Hardware Setup

2. *X-Ray Tube*

The system must be setup with the x-ray tube using the line source.

3. *Incident Beam Optics*

- Mount the hybrid monochromator on the incident beam side.
- Make sure the attenuator cable is plugged in.
- Insert the $\frac{1}{2}$ degree divergence slit, and verify that there is no manual beam attenuator in place.
- If the sample height is less than 25 mm insert an appropriate beam mask.

4. *Diffracted Beam Optics*

- Mount the rocking curve + triple axis optics on the diffracted beam side.
- Make sure no slit is present in the receiving slit holder and that detector 2 is behind the receiving slit position.

User Setup

5. Open the X'Pert Data Collector program.
6. Enter your user name and password.
7. Select **Instrument/Connect** from the pull down menu. The Connect box will appear.
8. Select the High Resolution configuration and choose the rocking curve beam path by selecting the "RC" radio button. Press the *OK* button.
9. Click the *OK* button to close the status messages that appear
10. Click Yes on the message box that asks if you want to apply the sample offsets
11. Select **Customize/Options** from the pull down menu. Verify or click on the "single crystal" box

Optics Setup

12. Select the **incident beam optics** tab and double click on one of the items.

- Select the Hybrid Monochromator as the *PreFIX* module.
 - Set the *divergence slit* to $\frac{1}{2}$ degree.
 - Set the *beam mask* to the size that is being used.
 - The *beam attenuator* should be set to Ni 0.125 mm automatic. The usage should be “Do Not switch” and activated should be checked. Check that the correct attenuation factor is displayed for the mirror attenuator. If not, select the correct attenuation factor.
13. Select the **diffracted beam optics** tab, and double click on one of the items.
- *PreFIX module* should be set to Triple axis (Rocking curve optics).
 - *Receiving Slit* should be set to none.
 - On the **Detector** tab:
 - *Wavelength* should be set to $K_{\alpha 1}$
 - *Detector 2* should be selected
14. Select the **Instrument Settings** tab. Double click on an item related to the generator.
- Set the *generator* to 45 kV and 40 mA.

Sample Mounting

15. Double click an item related to the sample stage.
- Select the **position** tab
 - Enter 90 degrees in the *psi* field so the sample can be easily mounted on the stage.
 - Press the *Apply* button to move the stage. (*Note – the enclosure doors must be closed for the stage to move*)
16. Open the enclosure doors and mount the sample as flat as possible on the stage. *You should wear gloves when handling the sample stage*
17. Optimize the Z position of the sample using either the dial gauge method, or the beam bisection method as explained below.

Dial Gauge Method for Sample Z position optimization

- Mount the dial gauge on the stage and close the enclosure doors.
- Return the stage to its upright position by setting *psi* to 0 degrees and pressing the *Apply* button.
- Move the z position of the sample stage until the dial gauge reads 1.0. (The small inner dial will read 1 and the large outer dial should point to the 0 at the top of the dial gauge.) Press the *OK* button to close this window.
- Remove the dial gauge and close the doors.
- Return *psi* to 0 degrees

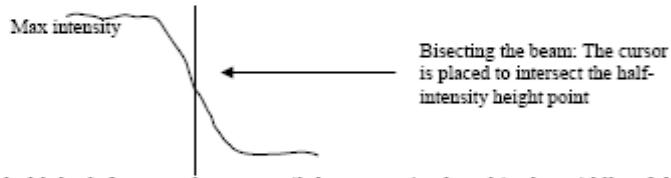
- Click OK to close the instrument settings window
- Proceed to Step 18

Beam Bisection Method for Sample Z position optimization (Z only)

- Make the following changes to the incident beam optics:
 - Remove the $\frac{1}{2}$ degree slit and insert a $1/32$ degree slit
 - Select the **incident beam optics** tab. Double click any item to prompt another window and enter $1/32$ for the divergence slit.
 - Click the **OK** button.
- Close the enclosure doors and select the **instrument settings** tab. Double click on an item related to the **positions**. Enter 0 in all fields and click **Apply**.

Sample Height (Z) Alignment

- In the **positions** table, enter an approximate position for the Z height. (e.g., 7.5mm for a Si wafer) and click **OK** to move the sample stage.
- Select **Measure/Manual Scan** from the pull down menu.
- In the **manual scan** window, enter the following parameters: Z in the **scan axis** field, 2 in the **range** field, 0.01 in the **step size** field, and 0.1 in the **time per step** field. Then click the **start** button.
- After the measurement is completed press the right mouse button and select **Move mode**. The graph will look like two plateau regions connect through a gradual decrease.



- Press and hold the left mouse button until the cursor is placed in the middle of the plateau region where the intensity is half of the full intensity. This will move the sample to bisect the main beam.
- Close the shutter by pressing the close shutter button on the upper menu bar or by closing the manual scan graph window.
- Make the following changes to the incident beam optics:
 - Remove the $1/32$ degree slit and insert a $1/2$ degree slit
 - Select the **incident beam optics** tab. Double click any item to prompt another window and enter $1/2$ for the divergence slit.

Angle Optimizations

Before a rocking curve is collected for an extended measuring time, preliminary scans are usually done to optimize the peak(s) of interest.

18. Click on the **instrument settings** tab and double click on an item related to the **positions** and select the **position** tab

19. Enter the substrate material in the *unit cell* field.

- *If the substrate material you are using is not in the database, you will need to set up a custom unit cell as follows:*
 - a. Select **Customize/Options**
 - Make sure the radio button in front of *Single crystal mode* is checked.
 - Close this window
 - b. Select **Customize/Unit cells**
 - Press the *insert* button
 - c. Enter all the requested information for the unit cell. The primary and secondary hkl are the growth vector and a wafer flat vector respectively. (If no wafer flat is present any vector perpendicular to the growth vector is sufficient.) The hkl values must be entered as integers with spaces between them.
 - d. After entering all the information click the *OK* button and notice the new cell added to the list. Then click the *OK* button.
 - e. Enter this new cell in the *unit cell* field
- *Alternatively, instead of entering unit cell information you may enter the 2theta value for a peak of interest in the 2theta field and 0 in the offset field. Click the OK button then continue with step 24*

20. Enter the plane of interest in the *HKL* field. Type the hkl values with a space in between the numbers. (e.g., 1 1 1) This will set all the angles to the theoretical values for this reflection.

- Click the *OK* button.

Omega Optimization

21. Select **Measure/Manual Scan** from the main menu.

22. Prepare an omega optimization scan as follows:

- Select *omega* in the *scan axis* field.
- Enter 6 in the *range* field.
- Enter 0.01 in the *step size* field.
- Enter 0.1 in the *time per step* field.
- Click the *start* button

23. If an omega peak is found, perform the following steps to move the goniometer to the peak angle position and then skip to step 25 (Psi Optimization). *If an omega peak is not found, skip to step 24 to execute a phi optimization scan.*

After the measurement is completed, you will find the peak in the scan data and move the goniometer to this position. This can be done in one of two ways:

- Method 1: Allow the software to determine the peak position
 - Press the right mouse button and select **Peak Mode**
 - The software will automatically determine the peak position.
 - Press the “*move to*” button to move the goniometer to the selected position
- Method 2: Manually determine the peak position
 - Press the right mouse button and select **Move mode**
 - Press and hold the left mouse button until the cursor is placed over the center of gravity of the peak. If more than one peak is present choose the narrowest, most intense peak. This will move the goniometer to the selected position

Phi Optimization

24. If an omega peak is not found, execute a phi optimization scan (for asymmetric scan plane)
- Enter phi in the *scan axis* field.
 - Enter 200 in the *range* field.
 - Enter 0.1 in the *step size* field.
 - Enter 0.1 in the *time per step* field.
 - Click the *start* button
 - After the measurement is completed find the peak in the scan data and move the goniometer to this position as in step 26.
 - Return to step 22 to perform another omega optimization scan.

Psi Optimization

25. Back in the **manual scan** window, enter the follow parameters for a psi optimization scan: (This is in the case of a symmetric reflection. If an asymmetric reflection is being studied, enter phi for the *scan axis* and leave all the other scan parameters as suggested here.)
- Enter psi in the *scan axis* field.
 - Enter 8 in the *range* field.
 - Enter 0.05 in the *step size* field.
 - Enter 0.1 in the *time per step* field.
 - Click the *start* button.

26. After the measurement is completed find the peak in the scan data and move the goniometer to this position as in step 23. If two peaks occur, select the lowest intensity point between the two peaks.

Verification of Optimizations

27. Back in the **manual scan** window, enter the following parameters to verify that the peak value of omega scan has not changed:
 - Enter omega in the *scan axis* field
 - Enter 1 in the *range* field.
 - Enter 0.002 in the *step size* field
 - Enter 0.1 in the *time per step* field.
 - Click the *start* button.
28. If the omega peak position has not changed since the first omega scan executed in step 22, then continue with step 29. (The peak is in the same position if the center of gravity of the current peak on the screen is located at the omega position of the instrument at the completion of the measurement.) If the omega peak position has changed, move the goniometer to the peak position as in step 23 and then return to step 25 and repeat the psi optimization scan.

Measurement Set-Up

29. Close the shutter by pressing the close shutter button on the upper menu bar  or by closing the manual scan graph window.
30. Insert the 1.0 mm receiving slit in front of the detector, and enter “1mm slit” in the receiving slit tab of the diffracted beam optics.
31. Back in the **manual scan** window, enter the following parameters for a 2theta optimization scan (this optimizes the detector position):
 - Enter 2theta in the *scan axis* field.
 - Enter 3 in the *range* field.
 - Enter 0.01 in the *step size* field.
 - Enter 0.1 in the *time per step* field.
 - Click the *start* button.
32. After the measurement is completed find the peak in the scan data and move the goniometer to this position as in step 23.

Setting the Attenuator

33. Select the *Incident Beam* optics tab. Set the attenuator to ‘preset intensity’. The in level should be 550,000 and the out level should be 400,000. Press the OK button.
34. **OPTIONAL:** If desired, perform a quick omega-2theta scan to determine the angular range for your measurement program. (If you already know the desired measurement

range, then proceed to step 36) Back in the **manual scan** window, enter the follow parameters:

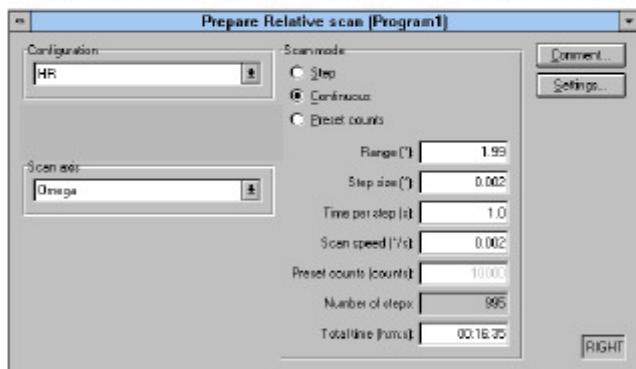
- Enter omega/2theta in the *scan axis* field.
- Enter 5 in the *range* field. (You may need to enter a larger value if you believe that measurement peaks will be present over a range greater than 5 degrees)
- Enter 0.005 in the *step size* field.
- Enter 0.2 in the *time per step* field.
- Click the *start* button.
- Note the angular range over which counts above background occur (x-axis in the plot).

35. Close both the *display manual scan* and the *scan dialog* windows.

Measurement Program

36. Select **File/New Program/Relative scan** to create a new program, or **File/Open Program** to load and edit an existing program

37. The window shown below will appear. Enter the information as explained below



- Configuration: High Res. Configuration
- Scan axis: *Omega -2theta*
- Range: Set to the desired range (as determined in step 34)
- Step size: Use 0.002 as the step size (suggested value).
- Time per step: Use 0.5 seconds/step or greater.

38. Select **File/Save as** and enter a name for the program. Click the *OK* button and close this window.

Measuring

39. Select Measure/Program/Relative scan.
40. Enter the program name chosen in step 38 if it does not already appear. Enter a data set name and sample identification. **Do not modify any of the angular fields, the HKL field or the Unit cell field.** Click the OK button and the measurement will begin.
41. When the measurement is completed, you can view and process the data using the X'Pert Data Viewer Program

Shut Down

42. Unmount your sample from the stage
43. Return the generator settings to the idle values (40kV and 10mA)
44. Exit the software
45. Log out of the User Log System on the SMIF web site