ABSTRACT

LOTHEY, SHRIDEVI. Simulation of Digital Circuits based on Amorphous Indium Gallium Oxide Thin Film Transistors. (Under the direction of Dr. Leda M. Lunardi.)

In the last years there have been significant advances in optoelectronics especially related to communications, display technologies, and optical memories. One of these remarkable technologies called Transparent Electronics relates to the idea of complete ‘see through’ electronic systems related to integrated on 'glass' or flexible substrates. Applications include transparent displays, 'smart' glass windows, and sensors.

Thin Film Transistors (TFTs) have been in use in display technology for years. To realize transparent circuits, Transparent Thin Film Transistors (TTFTs) are being explored. The advent of this technology has motivated research in transparent materials that can act as channel layers. Semiconductor oxides like ZnO and amorphous oxides such as InGaZnO$_4$ (IGZO) have surfaced as good candidates because of their superior transport qualities when compared to those of amorphous silicon. Transparent electronics require interfacing of transparent analog/digital driver circuitry along with storage of data (memories), all made of TTFTs. To develop functionally viable circuits, study of the dynamic characteristics and stability of the underlying active transistor is required. At the time of this work, very few functional circuits have been reported employing ZnO, or IGZO as the active channel material, namely - inverters, ring oscillators and pixel driving circuits. Hence, a step ahead would be to explore basic digital circuits. The goal of this work is to provide a pool of simple but fundamental logic circuits based on a-IGZO n-channel TFTs that can serve as building blocks for more complex digital systems.
An experimental extraction model based on the existing a:Si RPI TFT Level 61 model was developed to suit a-IGZO TFTs fabricated at NC State University. Using the adapted a-IGZO n-type TFT model, digital logic gates and clocked circuits including D-Latch, D Flip-flop and 3-bit Counter were designed. The simulated circuits were optimized to achieve maximum frequency of operation, and an output swing of at least 75% of the voltage supply. A Pseudo-Complementary Inverter design was employed as level-shifter yielding up to 45% increase in the output swing in the case of D Flip-Flop. All obtained results demonstrate the feasibility of complex a-IGZO TFT circuits as peripheral driver circuits in display applications.
Simulation of Digital Circuits based on Amorphous Indium Gallium Zinc Oxide Thin Film Transistors

by
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A thesis submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the degree of Master of Science

Electrical Engineering

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DEDICATION

I dedicate this thesis to my loving parents and sister who is also my best friend. This experience was possible only because of them.
BIOGRAPHY

Shridevi Lothey was born on 19th October 1985 in Bangalore, India. She received her Bachelor of Technology degree in Electronics and Communication from Visvesvaraya National Institute of Technology in Nagpur, India in year 2007. In August 2008, she joined North Carolina State University in Electrical Engineering department to study Analog/Digital Circuit Design. Since Fall 2009, she has worked under the guidance of Dr. Leda Lunardi on simulation of digital circuits based on transparent thin film transistors.
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First and foremost, I would like to thank my parents and my sister, who have loved and cared for me and blessed all my decisions. This work is dedicated to my family and friends.

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I am grateful to Dr. John Muth for all the beneficial advice and valuable discussions that helped me organize my work. I also want to thank his group members, specifically Haojun Luo for all the valuable experimental data, which formed the basis of this project. I want to thank Patrick Wellenius and Kanupriya Sharma for their support.

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CHAPTER 1

1. INTRODUCTION

1.1. Overview

Transparent Electronics is the emerging technology that deals with the development of optically transparent circuits. It has the potential to realize applications such as electronic paper or displaying news on a transparent and flexible material that can refresh the contents automatically. Another application could be solar cells embedded in the window panes of a building storing the incident solar energy.

The first major advancement in the history of transparent circuits took place in the year 1997 when Kawazoe et al. [1] reported p-type electrical conduction in CuAlO$_2$ transparent thin films. Since then, several materials have surfaced as candidates for the current-carrying layer of the transistor device. By the year 2003, three groups namely Masuda et al. [2], Hoffman et al. [3] and Garcia et al. [4] had reported fabrication of transparent ‘thin film’ transistor using ZnO. A year later, Nomura et al [5] demonstrated the use of an amorphous oxide semiconductor (AOS) as channel-layer for the transparent device on a flexible substrate. It was amorphous Indium Gallium Zinc Oxide (InGaZnO$_4$), or a-IGZO for short, a material with direct bandgap of >3.5 eV supporting both transparency and semi-conducting nature. It is well suited for transparent circuit applications, and is expected to bring
improvements in applications that don’t require transparency immediately. One potential application is display technology such as active-matrix liquid crystal displays (AMLCDs).

1.2. Motivation for thesis

The applications mentioned in the overview would require transparent circuitry, possibly integrated with a transparent display laid out on a system-on-glass arrangement. To make functionally viable transparent circuits, a thorough analysis of the dynamic characteristics of transparent device is required.

This thesis mainly focuses on design, simulation and investigation of the dynamic characteristics of circuits made using transparent a-IGZO TFTs. It involves preparing an HSPICE® model for simulation of the circuit building blocks. It also explores simple topologies within the scope that a-IGZO n-type material presents, typical transparent digital circuits and comparison of measured and simulated device characteristics.

1.3. Outline

This thesis has been written with a view of presenting the most basic circuit components designed using a-IGZO TFTs, while also providing a brief history and characteristics of the TFT itself. Chapter 2 gives background of transparent electronics and pertaining information about TFTs made out of amorphous oxide semiconductors (AOS). It
also throws light on the AOS circuits that have been reported so far. Chapter 3 discusses how the existing a-Si:H TFT HSPICE® model has been adapted to represent a real a-IGZO TFT device.

Chapter 4 gives the details of design of standard circuit components including inverter and logic gates. Chapter 5 discusses the design of frequency divider and flip-flop circuits. Both these chapters also give details about the performed simulations and the obtained results. Lastly, Chapter 6 concludes with a brief summary and suggestions for future work.
CHAPTER 2

2. BACKGROUND

This chapter offers brief history of thin film transistors (TFTs) along with some technical background on a common TFT device structure and its operation. The properties of transparent conducting oxides (TCOs) as current-carrying channel layers are discussed. The main focus of this thesis is a-IGZO TFT circuits; hence the a-IGZO material is presented in detail. Finally, the chapter explores various transparent TFT circuits that have been reported by various groups till the time of this study.

2.1. Thin Film Transistors (TFTs)

A thin-film transistor (TFT) is a special class of field-effect transistor whose current-carrying layer is a thin film of semiconductor material. To realize transparent circuits, transparent thin film transistors (TTFTs) are being explored. To this end, the substrate used to fabricate the devices is glass or plastic, whereas in a conventional transistor silicon wafer is used. There have been major advances in research for channel materials that would make possible transparent TFTs. Several semiconductor oxides like ZnO and amorphous oxides such as InGaZnO$_4$ (a-IGZO) have surfaced as good candidates. The following sections discuss these materials, TFT device structure and operation.
2.1.1. History

The first thin film transistor was reported by P. Weimer [6] in as early as 1962. It was fabricated via vacuum evaporation using cadmium sulphide (CdS) as a channel layer. Since then, several compounds like CdSe, organic materials viz. polymer, hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) have been explored as channel materials. The trend of using TFTs in high resolution/high performance liquid crystal displays took off in early 1980’s, and since then hydrogenated a-Si has become the dominant technology. In recent years, the research in this field has been motivated by need for TFT technology that can provide low-cost logic circuits on possibly flexible and (or) transparent substrates like plastic (glass).

2.1.2. Device Structure

The TFTs are fabricated in four common structures on basis of the order in which the layers are deposited. Fig 2-1 shows the TFT structures; staggered bottom-gate, co-planar bottom-gate, staggered top-gate and co-planar top-gate. The placement of terminals is also different for the structures, i.e. Source/Drain are placed on opposite sides of the semiconductor-insulator interface for staggered structures, while for the co-planar structures electrodes are placed on the same side of the interface.
2.1.3. TFT Operation

The basic thin film transistor operation for an n-type device is discussed in this section. A thin film transistor belongs to the class of *unipolar* field effect transistors (FETs). It has one controlling terminal called ‘gate’ to which the control voltage is applied, and two other terminals ‘source’ and ‘drain’ that allow the flow of current through the transistor. Depending on the gate to source bias $V_{GS}$ applied, the TFT exhibits three regions of operation subthreshold, linear and saturation (active) mode. Whereas in n-type TFTs, the electrons form an ‘accumulation’ layer which starts conducting when a gate bias of more than the ‘turn-on voltage’ ($V_{ON}$) is applied. Fig 2-2 illustrates the energy-band diagram of metal-insulator-semiconductor stack and three different scenarios are considered- zero, negative, and positive applied gate voltages [7].
Fig 2-2 Idealized energy band diagrams for an n-type, accumulation-mode TFT (a) Zero gate bias $V_G = 0$ V (b) Negative gate bias, $V_G < 0$ V (c) Positive gate bias, $V_G > 0$ V.

When zero bias voltage is applied ($V_{GS} = 0$), the energy bands stay in equilibrium and the concentration of negative charge carriers does not change. A negative gate bias ($V_{GS} < 0$) repels the electrons from the semiconductor-insulator interface and forms a depletion region devoid of any majority carriers. Since the depletion region is positively charged, the bands show an upward bending at the interface as shown in Fig 2-2(b). The depletion region can extend inside the semiconductor layer if more and more negative gate bias is applied. In this case, no channel layer is formed, and the TFT is said to be in cut-off region of operation. On the other hand, with a positive voltage bias on the gate ($V_{GS} > 0$), delocalized electrons are attracted towards the interface and this creates an accumulation layer of free majority carriers. Since there is accumulation of negative charge, the bands bend downward at the insulator-semiconductor interface as shown in Fig 2-2(c). Once the channel (accumulation) layer is formed, and if a positive drain to source ($V_{DS} > 0$) bias is applied, the transistor is said to be in active ‘on’ state.
Fig 2-3 Transparent thin-film transistor (TTFT) operation (for n-type channel) (a) Zero drain current ($I_D=0$). No electron accumulation layer exists at the channel-gate insulator interface. (b) $I_D$ follows Ohm’s law [$I_D=V_{DS}/R_C (V_{GS})$] at low $V_{DS}$ voltage [$V_{DS} \ll V_{GS}-V_{ON}$]. A uniform electron accumulation layer is formed at the channel-gate insulator interface from the source to the drain. (c) $I_D$ becomes sub-linear with respect to $V_{DS}$ and then saturates when $V_{DS}=V_{DSAT}=V_{GS}-V_{ON}$ because of the depletion or ‘pinch-off’ of the electron accumulation layer at the channel-gate insulator interface near the drain. Illustration based on [7].

As the majority carriers start populating near the interface when $V_{GS} > 0$. This provides scope for three regions of operation. When $V_{GS} < V_{ON}$ the transistor is said to be in ‘cut-off’ region. Since there is no electron accumulation layer, no drain current (drain current $I_D = 0$) flows through the TFT as shown in Fig 2-3(a). Now, if $V_{GS} > V_{ON}$, the TFT turns on and electrons start forming channel layer at the insulator interface. In this case, if a positive drain to source bias ($V_{DS} > 0$) is applied, the TFT starts conducting ($I_D > 0$) between source and
drain terminals. For the case \((V_{DS} < V_{GS} - V_{ON})\), the current \(I_D\) has an almost linear relationship with the drain to source voltage \(V_{DS}\), which is shown in equation 2-1.

\[
I_{DS} = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{ON}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (V_{DS} > 0, \ V_{DS} \leq V_{GS} - V_{ON})
\] (2-1)

During channel pinch-off, the region of the channel nearest the drain is depleted of electrons, and the drain current is independent of \(V_{DS}\) at this voltage denoted by \(V_{DSAT}\), \(V_{DSAT} = V_{GS} - V_{ON}\). The current value now changes to:

\[
I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left[ V_{GS} - V_{ON} \right]^2 \quad (V_{DS} > V_{DSAT}, \ V_{DSAT} = V_{GS} - V_{ON})
\] (2-2)

Once the drain-to-source voltages exceed the pinch-off condition, the TFT operates in the saturation region. Equations 2-1 and 2-2 comprise the ideal “square-law” theory for transparent TFT device equations. A summary of the terminal voltages and drain current values is presented in Table 2-1.
Table 2-1 Square Law Theory for ideal thin film transistors. Equations based on [7]

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<tbody>
<tr>
<td>Cut-off ((V_{GS} &lt; V_{ON}))</td>
<td>(I_{DS} = 0)</td>
</tr>
<tr>
<td>Linear (pre-pinchoff) ((V_{GS} &gt; V_{ON}); (V_{DS} \leq V_{GS} - V_{ON}))</td>
<td>(I_{DS} = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{ON}) V_{DS} - \frac{V_{DS}^2}{2} \right] )</td>
</tr>
<tr>
<td>Saturation (post-pinchoff) ((V_{DS} &gt; V_{GS} - V_{ON}))</td>
<td>(I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left[ V_{GS} - V_{ON} \right]^2 )</td>
</tr>
</tbody>
</table>

Where
\(V_{DSAT} = V_{GS}-V_{ON}\) = drain-source voltage during at pinch-off condition (V)
\(V_{GS}\) = gate-source voltage (V)
\(V_{ON}\) = turn-on voltage (V)
\(W\) = gate width (um)
\(L\) = gate length (um)
\(C_{ox}\) = oxide /insulator capacitance density (F cm\(^2\))
\(V_{DS}\) = drain-source voltage (V)

2.2. Transparent Conducting Oxides (TCO)

Transparent Conducting Oxides are the basic constituents of transparent electronics. TCOs are doped metal oxides largely used in passive applications (transparent coatings) and active (optoelectronic) applications such as flat-panel displays and photovoltaic cells that include organic and inorganic devices. They belong to the class of oxides which are both transparent (>80%) over the visible spectrum and electrically conductive in nature. For a material to be optically transparent in the visible region (400 to 700nm), it should possess
wide band gap (> 3.1 eV) [7, 8]. In general, wide band gap is associated with low conductivity. But since TCOs exhibit high carrier density (> $10^{19}$ cm$^{-3}$) they are viable for fabrication of transparent devices.

Some examples of oxides are indium oxide (In$_2$O$_3$), tin oxide (SnO$_2$), cadmium tin oxide (Cd$_2$SnO$_4$) and zinc oxide (ZnO). Good conductivity in these materials is usually obtained by chemical doping, for e.g. In$_2$O$_3$ doped with tin. The research on conductive oxides is largely limited to oxides of tin, indium and a combination of their oxides [7, 8, 9]. The table below summarizes the band gap and conductivity values for the above mentioned oxides. The mobilities reported here are all n-type. As clearly seen, indium oxide is superior to zinc and tin oxides in all the three shown figures of merit.

<table>
<thead>
<tr>
<th>Material</th>
<th>Band gap (eV)</th>
<th>Conductivity (S cm$^{-1}$)</th>
<th>Electron concentration (cm$^{-3}$)</th>
<th>Mobility (cm$^2$ V$^{-1}$ s$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In$_2$O$_3$</td>
<td>3.7- 4.4</td>
<td>10,000</td>
<td>&gt; $10^{21}$</td>
<td>35</td>
</tr>
<tr>
<td>ZnO</td>
<td>~3.3</td>
<td>8,000</td>
<td>&gt; $10^{21}$</td>
<td>20</td>
</tr>
<tr>
<td>SnO$_2$</td>
<td>3.9- 4.6</td>
<td>5,000</td>
<td>&gt; $10^{20}$</td>
<td>15</td>
</tr>
</tbody>
</table>

The most extensively used TCO so far has been indium tin oxide (ITO) as conductive coating in LCD and flat-panel displays, and as heat-reflective coating for architectural glasses. It is a homogeneous mixture of 90% indium oxide (In$_2$O$_3$) and 10% tin oxide (SnO$_2$) by weight. Owing to limited availability of indium, there have been attempts in finding alternative materials to replace ITO, some of which include SnO$_2$:Sb [10], ZnO:In [11] and ZnO:Al [12].

Table 2-2 Electrical properties of common transparent conducting oxides (TCOs) [7].
2.3. Amorphous Oxide Semiconductors

Amorphous oxide semiconductors (AOSs) can be classified as the semiconducting oxides composed of post-transition metal cations with \((n-1)d^{10}ns^0\) \((n \geq 4)\) electronic configurations. They possess high electron mobilities as compared to a-Si:H TFTs [13]. It also makes them attractive for manufacturing because of their low temperature process cycles and surface smoothness. A few examples include indium tin oxide (ITO), zinc oxide (ZnO) and zinc tin oxide (ZTO) for which amorphous-state mobilities as large as \(~40\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}\), \(~23-29\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) and \(~25\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) respectively, have been reported. These mobilities are relatively high when compared to those of a-Si by an order of magnitude and to those of most organic materials by a factor of two orders of magnitude.

Amorphous materials provide a means to eliminate the effects of grain boundaries that affect properties of polycrystalline materials, especially for devices covering large areas. Transparent AOSs share several properties that are generally not observed in conventional amorphous semiconductors. Also for AOSs, an effective way to control carrier concentration is by adjusting the oxygen vapor pressure during deposition and post-deposition processing [17].

Several AOS materials including zinc indium oxide Zn-In-O (a-ZIO), zinc tin oxide (a-ZTO), and indium gallium zinc oxide (IGZO) have been proposed for application as the channel material for thin film transistors. Since a-IGZO TFTs are subject of main focus in this thesis, it is discussed in detail in the next section.
2.3.1. TFTs made using Indium Gallium Zinc Oxide (a-IGZO)

Indium gallium zinc oxide (IGZO) is a wide band gap (~ 3.5 eV), n-type semiconductor containing three component oxides, In$_2$O$_3$, Ga$_2$O$_3$ and ZnO whose stoichiometry can be generally described as In$_{2x}$Ga$_{2-2x}$Zn$_{k}$O$_{k+3}$, where $0 < x < 1$ and k is an integer greater than 0 [18].

In 2003, Nomura et al. first reported the fabrication of a transparent TFT using a single crystalline thin-film transparent oxide semiconductor, InGaO$_3$(ZnO)$_5$, as an electron channel, 80 nm thick amorphous hafnium oxide (HfO$_2$) as a gate insulator and a coplanar top-gate structure [15]. The device exhibited an on-to-off current ratio of ~10$^6$, a field-effect mobility of ~80 cm$^2$ V$^{-1}$ s$^{-1}$ at room temperature and threshold voltage ($V_T$) of 3V. The operation was insensitive to visible light irradiation. The IGZO channel was deposited by pulsed laser deposition (PLD) on single-crystal yttria stabilized zirconia substrate and annealed at 1400 °C to undergo a reactive solid-phase epitaxy process.

In the following year, Nomura et al. fabricated transparent TFTs using a-IGZO for the active channel on a flexible polyethylene terephthalate substrate and yttrium oxide as the gate insulator [19]. The a-IGZO was deposited at room temperature via pulse laser deposition (PLD) and exhibited Hall Effect mobilities exceeding 10 cm$^2$ V$^{-1}$s$^{-1}$, which is an order of magnitude larger than those reported for hydrogenated amorphous silicon. The TTFTs exhibited saturation mobilities of 6-9 cm$^2$ V$^{-1}$s$^{-1}$, $I_{on}/I_{off}$ ratio of 10$^3$ and a threshold voltage $V_T$ of 1.6 V. The device characteristics were stable during repetitive bending of the TTFT sheet.
In 2007, Iwasaki et al. [20] used a combinatorial approach for thin-film transistors (TFTs) fabricated using amorphous IGZO channels. A large number of TFTs, having n-type channels with different chemical compositions, were fabricated simultaneously on a substrate. A systematic relation was clarified among the compositional ratio of In:Ga:Zn, oxygen partial pressure in film deposition atmosphere, and TFT characteristics. The experimental setup indicated that the optimal O\textsubscript{2} partial pressure employed during deposition changes for different stoichiometries. A lower O\textsubscript{2} partial pressure is required to produce functioning TFTs (i.e., TFTs that switch from well-defined on to off regions) when the Ga content of films increases. In contrast, a higher O\textsubscript{2} partial pressure is required to produce functioning TFTs when the In content of films increases. In:Ga:Zn ratios of 37:13:50 resulted in the best performance, where the channel mobility, $V_T$, and $I_{on}/I_{off}$ are $\sim$ 12 cm$^2$ V$^{-1}$ s$^{-1}$, 3V and $10^7$, respectively.

2.4. Transparent TFT Circuits

Discrete transparent TFTs fabricated using ZnO as the channel layer were first reported by three groups Masuda et al. [21], Hoffman et al. [22] and Garcia et al. [23] concurrently in the year 2003. Since the first appearance of transparent thin film transistors (TTFTs) made using transparent conducting oxides, there have been various groups reporting similar results, and a few attempts have been made to fabricate functional integrated circuit components such as inverters and ring oscillators. These transparent circuits are not expected to become complete products to start with, but may appear as circuit components on integrated ‘on-
glass’ electronics, or pixel switches in AMLCDs. This section reviews the previously reported TTFT based circuits.

Presley et al. [24] used indium gallium oxide (IGO) TFTs to fabricate the first transparent five-stage ring oscillator circuit. The n-channel was deposited by RF magnetron sputtering with SiNₓ and ITO serving as the gate insulator and the source/drain electrode, respectively. The TTFTs exhibited a peak incremental mobility of \( \sim 7 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1} \) and turn-on voltage of \( \sim 2 \, \text{V} \). The 5-stage ring oscillator circuit exhibited an oscillation frequency of \( \sim 2.2 \, \text{kHz} \) when the gate and drain of the load transistor were biased at 30 V and the maximum oscillation frequency observed was \( \sim 9.5 \, \text{kHz} \) if the gate and drain of the load transistor were biased at \( \sim 80 \, \text{V} \).

Recently, Suresh et al. [25] demonstrated ring oscillators and logic inverters with IGZO as channel layer and indium tin oxide (ITO) as contacts fabricated using pulsed laser deposited (PLD) at room temperature. Low-temperature (200 °C) atomic-layer-deposited Al₂O₃ was used as the gate dielectric in bottom-gated thin-film transistors with measured field-effect mobility of 15 \( \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1} \). The 7-stage ring oscillators operated at frequencies as high as 2.1 MHz, corresponding to a propagation delay of 48 ns/stage with a supply voltage of 25 V.

The above mentioned inverters and ring-oscillators are the only fully transparent AOS TFT circuits reported till date. Some of the circuits reviewed in the later section have used either opaque contacts or opaque substrates, rendering them only partially transparent.

IGZO-based integrated circuits (inverters and ring oscillators) were demonstrated by Ofugi et al. [26]. These TFTs used a 100 nm SiOₓ gate insulator deposited by RF sputtering
and were patterned using standard photolithography techniques. The field-effect mobility and the threshold voltage of the TFTs that were the members of the ring oscillators were estimated to be 2.7 cm² V⁻¹ s⁻¹ and +7.1 V, respectively. The maximum oscillation frequency of the fabricated 5-stage ring oscillator circuit was reported as ~21.5 kHz with 18 V supply voltage.

In 2008, Yin et al. [27] described the design and fabrication of high performance 5-stage ring oscillator with the standard 0.5μm bottom-gate amorphous Ga₂O₃-In₂O₃-ZnO TFT technology. The propagation delay time of 0.94ns/stage for a supply voltage of 9V was observed in the 5-stage ring oscillator and a novel 3TFTs bootstrapped inverter structure was achieved.

TFTs have been in action in display technology, particularly as switching transistors and rivers for pixels in LCD displays. Amorphous oxides have been proposed as the replacement material for a-Si:H TFTs- the dominant technology for the past two decades in this field. In 2006, Görrn et al. [28] demonstrated transparent OLED pixels by integrating transparent OLEDs on top of TTFTs. The devices exhibited an average transmittance of more than 70% in the visible part of the spectrum (400–750 nm), and the drivers in the transparent active pixel used entirely transparent TFTs based on zinc tin oxide (ZTO) deposited by oxygen-plasma-assisted pulsed-laser deposition (PAPLD).

Jeong et al. [29] (Samsung SDI) reported a full-color 12.1-inch Wide Extended Graphics Array WXGA (1280 x 768 pixels) active matrix OLED (AMOLED) display driven by an IGZO backplane. A commonly used two-transistor, one-capacitor (2Tr-1C) pixel circuit was employed to turn ‘on’ the electroluminescent (EL) device, OLED in this case. An
active matrix pixel was demonstrated by Wellenius et al. [30] using IGZO as the TFT channel layer and as the TFEL phosphor layer with europium as a dopant. IGZO TFTs were pulsed at 120 Hz with good transient response, demonstrating IGZO as a viable material for active matrix backplanes. The transparent TFEL device was implemented using novel amorphous Eu:IGZO wide band gap thin film as a phosphor. The results indicated viability of IGZO TFTs for active matrix display applications.

Until recently, the research groups focused on inverters and ring oscillators as means to study the dynamic characteristics of various amorphous oxide TFTs. In 2009, Lim et al. [31] fabricated and demonstrated the operation of logic OR gate using transparent dual-gate (DG) InGaZnO$_4$ thin film transistors on a glass substrate. A 100-nm-thick SiO$_2$ layer used as both top and bottom gate dielectrics was deposited by plasma enhance chemical vapor deposition (PECVD) at 200 °C. Dual-gate TFTs exhibited saturation mobility of 16.9 cm$^2$ V$^{-1}$s$^{-1}$, drain current on-to-off ratio of $\sim$1×10$^6$, subthreshold gate-voltage swing of 0.33 V decade$^{-1}$, and threshold voltage of $\sim$1.25 V respectively which was significantly better that their bottom-gate and top-gate counterparts.

Additionally, McFarlane et al. [32] fabricated AC to DC rectifying circuits in full-bridge and cross-tied configurations. The TFTs were implemented using indium gallium oxide (IGO) and zinc tin oxide (ZTO) as the channel layer and indium tin oxide ITO as contact material. With an input of 7.07 V$_{\text{rms}}$ at a frequency of 1 MHz, output voltages of $\sim$9 and $\sim$10.5 V, respectively, were observed. The channel length used was 15 μm, and both circuits of either material were shown to operate successfully up to 20 MHz.
In April 2010, Hatalis et al. [33] demonstrated a ten-stage half-bit shift register utilizing amorphous In–Ga–Zn–O (a-IGZO) thin-film-transistor (TFT) technology. The TFTs employed staggered bottom-gate structures with aluminum source, drain, and gate electrodes and RF-sputtered a-IGZO as the active channel material. The field-effect mobility was reported as 16 cm$^2$ V$^{-1}$s$^{-1}$. The half-bit shift register circuit consisted of seven transistors per stage and successfully operated at a maximum clock frequency of 40 kHz at a supply voltage of 20 V, which is sufficient to drive a full video graphics array (VGA) display at a frame rate of more than 80 kHz.
CHAPTER 3

3. SIMULATION MODEL FOR a-IGZO TFTs

This chapter first analyzes the current-voltage characteristics of the a-Si:H TFTs and presents the Level 61 a-Si:H TFT HSPICE® model in detail. Then it presents a detailed evaluation of the device structure and characteristics of fabricated a-IGZO TFTs at NC State University. Extraction of model parameters from the fabricated a-IGZO TFT characteristics is carried out, and finally a comparison of simulation results (model) and the fabricated a-IGZO TFT device characteristics (measured) is given.

3.1. The a-Si TFT device structure and current-voltage characteristics

The hydrogenated amorphous silicon thin-film transistor (a-Si:H) was first described by LeComber et al. in 1979 [34]. In the 1990’s, it became the industry standard for switching devices in large area electronics such as active-matrix liquid crystal displays (AMLCDs). Amorphous silicon has the advantage of being highly scalable to accommodate the large LCD display dimensions [35]. It also achieves uniformity and reproducibility in transistor performance across the entire substrate. The undoped amorphous silicon serves as an n-channel current-carrying layer, and hence the a-Si TFTs operate as n-type TFTs. Several groups have analyzed the characteristics of a:Si TFTs and reported the mobility values between 0.3-1 cm² V⁻¹ s⁻¹ [36, 37, 38]. The best-case mobility reported for a-Si:H TFTs for n-
type channel has been $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is two orders less than that of single-crystal silicon [39].

The most popular structure for a-Si TFTs is the inverted-staggered TFT, which uses silicon nitride (SiN$_x$) as the gate insulator. In 1989, Powell [40] discussed the basic physics underlying the operation of a-Si TFTs for inverted-staggered device structure and analyzed their static behavior. These TFTs used Cr metal for the gate electrode, silicon nitride as gate insulator, and Cr/AI double layer metallization for the source-drain contacts. The thickness of a-Si layer of is 2000 Å and that of SiN$_x$ layer is 4000 Å.

![Inverted-staggered structure for a-Si TFTs](image)

**Fig 3-1** Inverted-staggered structure for a-Si TFTs [40].
Fig 3-2 shows the current-voltage output characteristics for the referenced a-Si TFT, indicating good saturation and can be reasonably well described by the standard MOSFET equations for the above threshold characteristics. The field effect mobility can also be deduced from the saturated region by plotting the square root of the source-drain current against the gate voltage, which in this case is $0.6 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [40].

![Diagram](image1)

(a)

![Diagram](image2)

(b)

**Fig 3-2** (a) Transfer characteristics of a:Si TFT with $W/L = 7.5$ and (b) Drain current values for the same TFT [40].
3.2. The Level 61 RPI a-Si:H TFT model

Level 61 is the AIM-SPICE® MOS15 amorphous silicon (a-Si) thin-film transistor (TFT) model developed at Rensselaer Polytechnic Institute [41]. It is a three-terminal model without any bulk node. The following sections present the Level 61 model, underlying circuit diagram and related device equations to define some of the a:Si TFT model parameters that will be used later.

3.2.1. Model parameters

Some features of the Level 61 a-Si TFT model include [41]-

- The model includes induced charge trapped in localized states.
- Above threshold includes:
  - Field effect mobility becoming a function of gate bias.
  - Band mobility dominated by lattice scattering.
- Below threshold includes:
  - Fermi level located in deep localized states.
  - Relate position of Fermi level, including the deep DOS, back to the gate bias.
Table 3-1  Default values and description of Level 61 model parameters [41].

<table>
<thead>
<tr>
<th>Name</th>
<th>Unit</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALPHASAT</td>
<td>-</td>
<td>0.6</td>
<td>Saturation modulation parameter</td>
</tr>
<tr>
<td>CGDO</td>
<td>F/m</td>
<td>0.0</td>
<td>Gate-drain overlap capacitance per meter channel width</td>
</tr>
<tr>
<td>CGSO</td>
<td>F/m</td>
<td>0.0</td>
<td>Gate-source overlap capacitance per meter channel width</td>
</tr>
<tr>
<td>DEF0</td>
<td>eV</td>
<td>0.6</td>
<td>Dark Fermi level position</td>
</tr>
<tr>
<td>DELTA</td>
<td>-</td>
<td>5</td>
<td>Transition width parameter</td>
</tr>
<tr>
<td>EL</td>
<td>eV</td>
<td>0.35</td>
<td>Activation energy of the hole leakage current</td>
</tr>
<tr>
<td>EMU</td>
<td>eV</td>
<td>0.06</td>
<td>Field effect mobility activation energy</td>
</tr>
<tr>
<td>EPS</td>
<td>-</td>
<td>11</td>
<td>Relative dielectric constant of substrate</td>
</tr>
<tr>
<td>EPSI</td>
<td>-</td>
<td>7.4</td>
<td>Relative dielectric constant of gate insulator</td>
</tr>
<tr>
<td>GAMMA</td>
<td>-</td>
<td>0.4</td>
<td>Power law mobility parameter</td>
</tr>
<tr>
<td>GMIN</td>
<td>m⁻³eV⁻¹</td>
<td>1E23</td>
<td>Minimum density of deep states</td>
</tr>
<tr>
<td>IOL</td>
<td>A</td>
<td>3E-14</td>
<td>Zero bias leakage current parameter</td>
</tr>
<tr>
<td>KASAT</td>
<td>1/° C</td>
<td>0.006</td>
<td>Temperature coefficient of ALPHASAT</td>
</tr>
<tr>
<td>KVT</td>
<td>V/° C</td>
<td>-0.036</td>
<td>Threshold voltage temperature coefficient</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>1/V</td>
<td>0.0008</td>
<td>Output conductance parameter</td>
</tr>
<tr>
<td>M</td>
<td>-</td>
<td>2.5</td>
<td>Knee shape parameter</td>
</tr>
<tr>
<td>MUBAND</td>
<td>m²/Vs</td>
<td>0.001</td>
<td>Conduction band mobility</td>
</tr>
<tr>
<td>RD</td>
<td>m</td>
<td>0.0</td>
<td>Drain resistance</td>
</tr>
<tr>
<td>RS</td>
<td>m</td>
<td>0.0</td>
<td>Source resistance</td>
</tr>
<tr>
<td>SIGMA0</td>
<td>A</td>
<td>1E-14</td>
<td>Minimum leakage current parameter</td>
</tr>
<tr>
<td>TNOM</td>
<td>°C</td>
<td>25</td>
<td>Parameter measurement temperature</td>
</tr>
<tr>
<td>TOX</td>
<td>M</td>
<td>1E-7</td>
<td>Thin-oxide thickness</td>
</tr>
<tr>
<td>V0</td>
<td>V</td>
<td>0.12</td>
<td>Characteristic voltage for deep states</td>
</tr>
<tr>
<td>VAA</td>
<td>V</td>
<td>7.5E3</td>
<td>Characteristic voltage for field effect mobility</td>
</tr>
<tr>
<td>VDSL</td>
<td>V</td>
<td>7</td>
<td>Hole leakage current drain voltage parameter</td>
</tr>
<tr>
<td>VFB</td>
<td>V</td>
<td>-3</td>
<td>Flat band voltage</td>
</tr>
<tr>
<td>VGSL</td>
<td>V</td>
<td>7</td>
<td>Hole leakage current gate voltage parameter</td>
</tr>
<tr>
<td>VMIN</td>
<td>V</td>
<td>0.3</td>
<td>Convergence parameter</td>
</tr>
<tr>
<td>VTO</td>
<td>V</td>
<td>0.0</td>
<td>Zero-bias threshold voltage</td>
</tr>
</tbody>
</table>
Fig 3-3 Circuit diagram representation of Level 61 a-Si TFT model

Model Equations

\[ I_{ds} = I_{leakage} + I_{ab}, I_{ab} = g_{ch} V_{ds} (1 + \text{LAMBDA}V_{ds}) \]

\[ V_{dse} = \frac{V_{ds}}{1 + \left( \frac{V_{ds}}{V_{sate}} \right)^M} \]

\[ V_{sate} = \alpha_{sat} V_{gte} \]

\[ g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}, g_{chi} = qn_e W.MUBAND / L \]

\[ n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}} \]

\[ n_{sa} = \frac{EPSI V_{gte} \left( \frac{V_{gte}}{V_{aat}} \right)^{\text{GAMMA}}}{q \cdot TOX} \]
\[ n_{sb} = n_{so} \left( \frac{t_m V_{gbe} \text{EPSI}}{V_0 \text{EPS}} \right) \frac{2V_0}{V_c} \]

\[ n_{so} = N_c t_m \frac{V_c}{V_0} \exp \left( -\frac{\text{DEF}_0}{V_{th}} \right), N_c = 3 \cdot 10^{25} m^{-3} \]

\[ V_g = \frac{2 \cdot V_0 \cdot V_{th}}{2 \cdot V_0 - V_{th}}, I_m = \sqrt{\frac{\text{EPSI}}{2q \cdot \text{GMIN}}} \]

\[ V_{gbe} = \frac{V_{MIN}}{2} \left[ 1 + \frac{V_{gs}}{V_{MIN}} + \sqrt{\text{DELTA}^2 + \left( \frac{V_{gs}}{V_{MIN}} - 1 \right)^2} \right] \]

\[ V_{gs} = V_{gs} - V_T \]

\[ V_{gbe} = V_{gs} - V_{FB}, I_{leakage} = I_{kl} + I_{min} \]

\[ I_{kl} = I_{OL} \left[ \exp \left( \frac{V_{ds}}{V_{DSL}} \right) - 1 \right] \exp \left( -\frac{V_{gs}}{V_{GSL}} \right) \exp \left[ \frac{EL}{q} \left( \frac{1}{V_{tho}} - \frac{1}{V_{th}} \right) \right] \]

\[ I_{min} = \text{SIGMA}0 \cdot V_{ds} \]

25
Temperature Dependence

\[ V_{tho} = k_B \cdot \text{TNOM} / q, V_{th} = k_B \cdot \text{TEMP} / q \]

\[ V_{aat} = V_{AA} \exp \left[ \frac{\text{EMU}}{q \cdot \text{GAMMA}} \left( \frac{1}{V_{th}} - \frac{1}{V_{tho}} \right) \right] \]

\[ V_T = V_{TO} + KVT(\text{TEMP} - \text{TNOM}) \]

\[ \alpha_{sat} = \text{ALPHASAT} + KASAT(\text{TEMP} - \text{TNOM}) \]

Capacitance

\[ C_{gs} = C_f + \frac{2}{3} C_{gc} \left[ 1 - \left( \frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}} \right)^2 \right] \]

\[ C_{pd} = C_f + \frac{2}{3} C_{gc} \left[ 1 - \left( \frac{V_{sate}}{2V_{sate} - V_{dse}} \right)^2 \right] \]

\[ C_f = 0.5 \cdot \text{EPS} \cdot W, C_{gs} = q \frac{dn_{sc}}{dV_{gs}} \]

\[ n_{sc} = \frac{n_{sac} \cdot n_{sbc}}{n_{sac} + n_{sbc}}, n_{sac} = \frac{\text{EPSI} \cdot V_{gte}}{q \cdot \text{TOX}} \]

\[ n_{sbc} = n_{sb} \]
3.2.2. Sensitivity of the model parameters

This section discusses the sensitivity of TFT output characteristics (drain current $I_D$) to change in Level 61 model parameters previously explained. The impact of varying the model parameters on simulation results was studied. The output current $I_D$ can be partitioned into two regions based on the operation regimes: subthreshold (leakage) and post-threshold regions respectively.

It was duly observed from the results (as shown in Fig 3-4) that the parameters associated with leakage current and density of states viz. $G_{\text{MIN}}$ (minimum density of deep states), $V_{\text{MIN}}$ (Convergence parameter) and $\Delta L$ (Transition width parameter) affected the current in the subthreshold region. While the mobility parameters viz. $\gamma$, $\mu_0$ and $V_{\text{AA}}$ are used to model the mobility dependence on gate bias voltage. These parameters along with the zero bias threshold voltage ($V_{\text{TO}}$) influenced the linear and saturation (post-threshold) region of the curve. In the following plots, the output currents $I_D$ (A) have been plotted for different values of the most significant model parameters mentioned above.

(a) 

(b)
Fig 3-4 Sub-threshold regime- Sensitivity of output current with change in model parameters is plotted. (a) delta  (b) vmin  (c) gmin

Fig 3-5 Post-threshold regime- Sensitivity of output current with change in model parameters is plotted.  (a) alphasat (b) gamma (c)  muband (d) vto
3.3. Fabrication and characterization of a-IGZO TFT device

The transparent a-IGZO TFT used in this study has an inverted-staggered structure and was fabricated on commercially available Corning 7059 glass substrate with a 250 nm (8 Ω/□) sputtered indium tin oxide (ITO) layer [42]. The ITO layer constituted the gate electrode of the bottom-gate TFT. A 100 nm thick layer of Al₂O₃ as the gate dielectric was deposited at 200 °C using atomic layer deposition (ALD). The IGZO channel of thickness 35 nm and ITO source and the drain electrodes of thickness 150 nm each were then deposited at room temperature by pulsed laser deposition technique (PLD) technique. The gate, channel and the source/drain electrode layers were patterned using standard photolithography and liftoff techniques. This transistor has a channel width of 200 μm and a channel length of 20 μm respectively. Both the gate-drain and gate-source overlap regions are 3μm wide.

![TFT structure used as device under test (DUT) used in this thesis-a fully-transparent a-IGZO thin film transistor [42].](image)

**Fig 3-6** TFT structure used as device under test (DUT) used in this thesis- a fully-transparent a-IGZO thin film transistor [42].
Fig 3-7 Layout for the device under test (DUT) with W/L ratio = 200µm/20µm.

3.3.1. Current Voltage characteristics

The current voltage characteristics or I-V curves are generally used to describe the electrical performance of a transistor. The output current was measured for the fabricated a-IGZO TTFT with W/L = 200µm/20µm and the curves were used to derive the important figures of merit for the transistor. A set of $I_D$-$V_{DS}$ plots was taken with varying drain-source voltage $V_{DS}$ and values of $V_{GS}$ fixed at 0 V, 6 V, 12 V and 18 V. The transfer characteristics were plotted for varying gate-source bias and $V_{DS}$ fixed at 20 V. Both these curves are shown in Fig 3-7.
Fig 3-8 Output characteristics of a-IGZO TFT with W/L = 200µm/20µm (a) Drain current $I_D$ versus $V_{GS}$ at $V_{DS} = 20$ V. (b) Drain current $I_D$ plotted against $V_{DS}$ for different values of gate voltage bias $V_{GS}$.

### 3.3.2. Figures of merit

In this section the a-IGZO TFT characterization is performed by extracting data to assess its performance. Some main figures-of-merit are threshold voltage ($V_{TH}$), turn-on voltage ($V_{ON}$), drain current on-to-off ratio ($I_{on/off}$), field effect mobility $\mu_{EF}$ and sub-threshold swing ($S$). Threshold voltage $V_{TH}$ is defined as the minimum voltage that is required to make the transistor conducting (‘ON’ state). Applying the square law model for ideal thin film transistors, the following equation gives current-voltage characteristics:

$$I_D = \frac{1}{2} \mu C_{ins} \frac{W}{L} (V_{GS} - V_{TH})^2$$  \hspace{1cm} (3-1)

where $C_{ins}$ is the capacitance per unit area of the insulator layer. Taking square root of both sides gives the following-
\[
\sqrt{I_D} = \sqrt{\frac{\mu C_{ins} W}{2L}} (V_{GS} - V_{th})
\]

(3-2)

The above expression is valid for values of \( V_{GS} \geq V_{TH} \). By plotting \( \sqrt{I_{DS}} \) vs. \( V_{GS} \) and by extrapolating down to the x-axis, the threshold voltage can be determined. Since TFTs are accumulation mode devices, another parameter \( V_{ON} \) (similar to \( V_{TH} \)) is used to assess their performance. \( V_{ON} \) is defined as the gate voltage at which there is a sharp increase in the channel conduction which corresponds to the formation of the accumulation layer. Consequently, a sharp increase in the drain current \( I_D \) of thin film transistor is observed. For the fabricated device used in this thesis, both \( V_{TH} \) and \( V_{ON} \) are extracted. Fig 3-9 shows the extrapolation technique for \( V_{TH} \) extraction.

\[\text{Fig 3-9 } \sqrt{I_D} \text{ vs. } V_{GS} \text{ curve of a-IGZO TFT of } W/L = 100\mu m/20\mu m \text{ at drain to source bias of } V_{DS} = 20 \text{ V. The tangent to the curve is extrapolated till it meets the x-axis at } I_D=0. \text{ The threshold voltage is } V_{TH} = 0.1 \text{ V} \]

The channel mobility is one of the most important semiconductor parameters because it is directly related to TFT frequency response. There are two types of mobilities explained in
this section- saturation mobility, $\mu_{\text{sat}}$, and average mobility, $\mu_{\text{ave}}$. To obtain the saturation mobility, we consider the square law model equation 3-3.

$$I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} [V_{GS} - V_{ON}]^2 \quad (V_{DS} > 0, V_{DS} \geq V_{GS} - V_{ON}) \quad (3-3)$$

Differentiating with respect to $V_{GS}$ and rearranging the terms, we get the following expression-

$$\mu_{\text{sat}} = \left( \frac{d\sqrt{I_D}}{dV_{GS}} \frac{1}{C_{\text{ins}} \frac{W}{2L}} \right)^2 \quad (3-4)$$

This value represents the saturation mobility $\mu_{\text{sat}}$, which is graphically determined from the slope of the $\sqrt{I_{DS}}$ vs. $V_{GS}$ graph shown in Fig 3-10. Using a dielectric constant of 9.1 for Al$_2$O$_3$ layer with a thickness of 100 nm, the typical saturation mobility value obtained for TFT under consideration is 2 cm$^2$ V$^{-1}$ s$^{-1}$. 

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Fig 3-10 $\sqrt{I_D}$ vs. $V_{GS}$ curve of a-IGZO TFT with $W/L = 200\mu m/20\mu m$ at drain to source bias of $V_{DS} = 20$ V. The tangent to the curve is extrapolated till it meets the x-axis at $I_D = 0$. The slope of the tangent is then used to calculate the saturation mobility.

On the other hand, average mobility, $\mu_{ave}$ takes into account the mobilities of all the carriers in the channel. To determine $\mu_{ave}$ the channel conductance of the TFT is considered and is given by,

$$G_{CH}(V_{GS}) = \lim_{V_{th} \to 0} \frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}}$$  \hspace{1cm} (3-5)$$

Using the above equation for channel conductance, we get the following equation for average mobility-

$$\mu_{ave}(V_{GS}) = \frac{G_{CH}(V_{GS})}{C_{ds} \frac{W}{L} (V_{GS} - V_{TH})}$$  \hspace{1cm} (3-6)$$
The subthreshold swing (S) is a measure of how fast the transistor can turn on when gate bias is applied. It can be estimated from the TFT transfer characteristics in subthreshold regime, using the following equation:

\[
S = \left( \frac{\partial \log(I_D)}{\partial V_{GS}} \right)_{\text{max}}^{-1}
\]

(3-7)

Figure 3-11 illustrates the extraction of subthreshold swing (S) value. The extracted value is 0.43 V/decade for device with W/L = 200µm/20µm. It also shows the maximum drain current on-to-off ratio, \(I_{on/off}\), at high \(V_{DS}\) voltage (20 V in this case).

![Fig 3-11 \(I_D\) vs. \(V_{GS}\) curve of a-IGZO TFT with W/L = 200µm/20µm at drain to source bias of \(V_{DS} = 20\) V to extract sub-threshold slope.](image)
3.4. Model validation using the measured a-IGZO TFT device data

In this section, the intrinsic a:Si RPI TFT Level 61 model is tailored to match the fabricated a-IGZO TFT device characteristics, as shown in Fig 3-7. The current-voltage characteristics of a-IGZO TFTs are reasonably close to those of a:Si TFTs shown in Fig 3-2. Apart from both materials being amorphous and n-type, the respective TFTs have similar geometries and device structures. Also, the TFT operation for both a:Si and a-IGZO is based on the formation of accumulation layer for conduction. The required a-IGZO TFT model parameters have been extracted from the measured data of the fabricated device in order to obtain accurate representation of the results.

CGSO and CGDO are Level 61 model parameters that represent the gate-source and gate-drain overlap capacitances per meter channel width, respectively. The capacitance of a parallel plate capacitor is given by the following expression:

\[
C = \frac{\varepsilon_r \varepsilon_o A}{d}
\]

where \(\varepsilon_r\) is the relative dielectric constant and \(\varepsilon_o\) is the permittivity of space, which is equal to \(8.854 \times 10^{-12}\) F/m. In the case of pertinent a-IGZO TFT device, the dielectric is alumina (Al\(_2\)O\(_3\)), of which the dielectric constant \(\varepsilon_r\) is equal to 9.1. The variable \(A\) from Eq. 3-1 represents cross-section area of the plates, and \(d\) is the separation between them. To calculate the overlap capacitances, consider the cross section of a-IGZO device shown in Fig 3-6. We can deduce the area \(A\) to be (gate-source/drain overlap) \(\times W\) (width of the channel). The thickness of dielectric in given TFT is 100 nm. The value of overlap capacitance per meter
channel width comes out to be 2.4 nF/m. The source/drain resistances have been calculated using the sheet resistance of indium tin oxide (ITO) which is equal to 35 Ω/□. The estimated value for a TFT (Device A) with W/L = 200µm/20µm is $R_{SD} = 525 \, \Omega$. Normalizing the resistance (multiplying the resistance $R_{SD}$ by width $W$) value with respect to length, we obtain 10.5 Ω cm. A summary of parameters extracted from a-IGZO TFT dc characterization is shown in Table 3-2. As clearly seen, the TFT exhibits high quality device characteristics and is suitable for use in simple digital circuit components. A comparison of this device with another TFT fabricated in-house (device B) [25] with different set of conditions is shown in the Table 3-2.

**Table 3-2** Comparison of extracted parameters after characterization of a-IGZO TFT with W/L 200µm/20µm

<table>
<thead>
<tr>
<th>Device</th>
<th>Threshold voltage</th>
<th>Turn on voltage</th>
<th>Mobility</th>
<th>Sub-threshold Swing</th>
<th>$I_{on}/I_{off}$</th>
<th>$C_{GS}; C_{DS}$</th>
<th>$R_{SD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.1 V</td>
<td>-4 V</td>
<td>2 cm²/Vs</td>
<td>0.43 V/decade</td>
<td>$\approx 1.27 \times 10^8$</td>
<td>2.4 nF/m</td>
<td>10.5 Ω cm</td>
</tr>
<tr>
<td>B</td>
<td>1 V</td>
<td>-2.5 V</td>
<td>12 cm²/Vs</td>
<td>0.2 V/decade</td>
<td>$&gt; 1 \times 10^8$</td>
<td>2.4 nF/m</td>
<td>10.5 Ω cm</td>
</tr>
</tbody>
</table>

The parameters for device A VTH, MUBAND, CGS, CGD, RS and RD were taken from Table 3-2, and used as initial values for the Level 61 model. The parameter ‘eps’ (relative dielectric constant of the substrate) is taken as 5.8 from [43]. The other leading model parameters were then adjusted separately in sub-threshold and post-threshold regions
by keeping in mind their trends observed in Fig 3-4 and 3-5. Several iterations were performed and the parameter values were modified to match the simulation results with measured drain current $I_D$. The parameters that fit closest to the measured data are summarized in Table 3-3.
Table 3-3 Parameters used to model the transparent a-IGZO TFTs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alphasat</td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Cgdo</td>
<td>F/m</td>
<td>2.4e-9</td>
</tr>
<tr>
<td>Cgso</td>
<td>F/m</td>
<td>2.4e-9</td>
</tr>
<tr>
<td>def0</td>
<td>eV</td>
<td>0.6</td>
</tr>
<tr>
<td>Delta</td>
<td>-</td>
<td>12</td>
</tr>
<tr>
<td>El</td>
<td>eV</td>
<td>0.35</td>
</tr>
<tr>
<td>Emu</td>
<td>eV</td>
<td>0.1</td>
</tr>
<tr>
<td>Eps</td>
<td>-</td>
<td>5.84</td>
</tr>
<tr>
<td>Epsi</td>
<td>-</td>
<td>9.1</td>
</tr>
<tr>
<td>Gamma</td>
<td>-</td>
<td>0.06</td>
</tr>
<tr>
<td>Gmin</td>
<td>m⁻³eV⁻¹</td>
<td>3e22</td>
</tr>
<tr>
<td>Iol</td>
<td>A</td>
<td>3e-15</td>
</tr>
<tr>
<td>Kasat</td>
<td>1/° C</td>
<td>0.006</td>
</tr>
<tr>
<td>Kvt</td>
<td>V/° C</td>
<td>-0.036</td>
</tr>
<tr>
<td>Lambda</td>
<td>I/V</td>
<td>0.0001</td>
</tr>
<tr>
<td>M</td>
<td>-</td>
<td>2</td>
</tr>
<tr>
<td>Muband</td>
<td>m²/Vs</td>
<td>0.0002</td>
</tr>
<tr>
<td>Rd</td>
<td>m</td>
<td>105</td>
</tr>
<tr>
<td>Rs</td>
<td>m</td>
<td>105</td>
</tr>
<tr>
<td>sigma0</td>
<td>A</td>
<td>1e-15</td>
</tr>
<tr>
<td>Tnom</td>
<td>°C</td>
<td>27</td>
</tr>
<tr>
<td>Tox</td>
<td>M</td>
<td>1e-7</td>
</tr>
<tr>
<td>v0</td>
<td>V</td>
<td>0.12</td>
</tr>
<tr>
<td>Vaa</td>
<td>V</td>
<td>1e3</td>
</tr>
<tr>
<td>Vdsl</td>
<td>V</td>
<td>11</td>
</tr>
<tr>
<td>Vfb</td>
<td>V</td>
<td>0.01</td>
</tr>
<tr>
<td>Vgsl</td>
<td>V</td>
<td>11</td>
</tr>
<tr>
<td>Vmin</td>
<td>V</td>
<td>0.15</td>
</tr>
<tr>
<td>Vto</td>
<td>V</td>
<td>0.1</td>
</tr>
</tbody>
</table>
3.4.1. Comparison of model to measured data

Comparison between the measured and simulated drain current $I_D$ (A) was carried out for two fabricated a-IGZO TFT devices, namely ‘T1’ and ‘T2’. The device T1 has W/L ratio of 100µm/20µm, whereas T2 has W/L ratio of 200µm/20µm. Results of comparison between the modeled and measured a-IGZO TFT transfer and output characteristics are shown in both semi-log and linear scales in Fig 3-12 and 3-13 respectively.

![Comparison of model to measured data](image)

**Fig 3-12** Comparison between the simulation (red circles) and measurement (black line) for TFT devices with (a) T1 device, W/L = 100µm/20µm (b) T2 device, 200µm/20µm on a semi-log scale.

Figure 3-12 shows that the adapted model cannot fit the measured data in regions below $V_{ON}$, but it represents the data well for higher values of $V_{GS}$. Additional comparison was performed for drain currents $I_D$ (A) in the linear scale for the same TFTs as given in Fig
3-13. The plot shows a greater mismatch in current for T2 device out of the two TFTs. The error margin for simulated current as compared to the measured current for T1 is presented in Fig 3-13. The deviation is calculated for values of $V_{GS}$ when the transistor is in ‘ON’ state, which remains within ±15% of measured value. Deducing from the comparisons, the adapted a-IGZO TFT model is fitted better for post-threshold $V_{GS}$ bias voltage.

**Fig 3-13** Comparison between the simulation and measurement for TFT devices with (a) T1 device, W/L = 100µm/20µm (b) T2 device, 200µm/20µm on linear scale.
CHAPTER 4

4. DESIGN AND SIMULATION OF a-IGZO CIRCUIT COMPONENTS

The following chapter presents the design and simulations of the digital circuit components and analyzes the results obtained for each of them. The limitations faced while designing the circuits for the a-IGZO TFT technology at its current state are discussed. The performance of simulated inverters is examined in detail under different loads and beta ratios. Subsequently the circuits of a-IGZO TFT digital logic gates are simulated and various circuit parameters are studied.

4.1. Introduction

Simulators like HSPICE® help the circuit designers to verify designs of the integrated circuits before layout, fabrication and testing process. Essential figures of merit like frequency, propagation delay, output swing and power consumption can be predicted by simulations. We have duly employed the intrinsic a:Si TFT model to simulate a-IGZO TFT circuits. This thesis aims at designing some of the basic digital a-IGZO TFT circuits that can be utilized to build more complex circuits. This process serves as the basic step required to understand the device and circuit-level limitations that may arise while doing small-scale integration of a-IGZO TFT circuits.
4.1.1. Limitations of the present a-IGZO technology

There are key limitations in the existing a-IGZO technology due to lack of availability of p-type a-IGZO material. In this chapter, digital circuits and logic gates have been implemented using n-channel TFTs. The major limitation with n-channel implementation is that a DC current flows through the logic gate even when the output is in steady state. This leads to static power dissipation. A voltage supply ($V_{DD}$) of 20 V has been used for all the TFT circuits demonstrated in further sections.

4.1.2. Simulation Setup

Design of all the integrated circuits was done using Cadence® Virtuoso 2008. The inbuilt Cadence ‘analogLib’ library was used to prepare circuit schematics using n-type transistors. HSPICE® was used to carry out device level transient and DC simulations, as it is the easiest method to observe experimental results. The adapted a-IGZO TFT model was incorporated in simulations as a TFTNMOS.m file. All the waveforms were viewed in Cosmoscope tool. Table 4-1 shows the commands used in circuit HSPICE® netlists for nature of analysis.
**Table 4-1** Syntax and examples of typical HSPICE® commands used to perform simulations in this thesis.

<table>
<thead>
<tr>
<th>Function</th>
<th>Command</th>
</tr>
</thead>
</table>
| DC simulation for variable var1; may also include sweep for var2 | Syntax-  
  .DC var1 start1 stop1 incr1 <SWEEP var2 type np start2 stop2>  
  Example-  
  .DC vdc lin 100 -5 20 SWEEP vdd 5 20 5 |
| Transient simulation for specified duration | Syntax-  
  .TRAN tincr1 tstop1 <SWEEP var start_expr stop_expr step_expr>  
  Example-  
  .tran 1p 200u SWEEP beta 5 20 5 |
| Measurement or calculation of parameters from the circuit netlist | Syntax-  
  .MEAS .MEASURE <TRAN > varname TRIG_SPEC TARG_SPEC <or>  
  .MEASURE <DC | AC | TRAN> result TRIG … TARG …  
  + <GOAL = val> <MINVAL = val> <WEIGHT = val>  
  Example-  
  .MEAS TRAN Qtot INTEGRAL i(v0) FROM=0 TO=100u |
4.2. Inverter

An inverter is the core of digital circuit design. Once the properties and operation of an inverter is clearly understood, designing of more complex digital circuits can be simplified. The most common inverter structure is the static complementary MOSFET inverter shown in Fig 4-2.

![Fig 4-1 Typical CMOS Inverter with $V_{IN}$ as the input and $V_{OUT}$ as the output load voltage.](image)

The CMOS inverter uses PMOS as pull-up system and NMOS as pull-down system to obtain inversion of the input voltage level. It serves as building block for bigger circuits, and is used to study the DC characteristics of the contained transistors. The voltage transfer characteristic (VTC) shows the response of an inverter $V_{OUT}$ to specific input voltages $V_{IN}$. It is a figure of merit for the static behavior of the inverter.
Noise margin is a parameter critical for good design of digital circuits. It determines the allowable noise voltage limit on the input of a gate so that the output will be unaffected. Noise margin (NM) is specified in terms of the low noise margin $NM_L$ and high noise margin $NM_H$. Any rectangle that can be drawn inside the characteristic loop (overlap of VTC while interchanging the $V_{IN}$ and $V_{OUT}$ voltages) represents a set of noise voltages and corresponding $V_{IL}$, $V_{IH}$, $V_{OL}$ and $V_{OH}$ which are at the limits of inverter stability. From Fig 4-2(b), $V_{IL}$ is the smallest input voltage recognized as logic ‘0’, and $V_{IH}$ is the smallest input voltage recognized as logic ‘1’. When the rectangle becomes a square, one has the worst case equal noise margins (i.e., $NM_H = NM_L$). Figure 4-2(b) illustrates the technique to extract noise margin from inverter transfer characteristics.

![Diagram of CMOS inverter transfer characteristics and noise margin](image)

**Fig 4-2** (a) Voltage transfer characteristics of a CMOS inverter, where $V_{DD} = 2.5$ V. The operation region of PMOS and NMOS transistors are given as cutoff, resistive and saturation. (b) Valid noise margins for a given inverter characteristic, using an area embedded within the transfer curve loop [44].
4.2.1. Inverter using only n-type TFTs

Oxide semiconductor based TFTs are unipolar in nature, hence two enhancement-mode transistors (load and control) are connected in series as shown in Figure 4-3 to produce an inverter action. The load transistor is diode driven (in saturation) and this configuration is commonly used in unipolar TFT circuits. The VTC for TFT inverter with widths $W_L=20\mu m$, $W_D=100\mu m$ and lengths $L_L=L_D=10\mu m$ is shown in Fig 4-4.

![Diagram of Inverter Using Only n-type TFTs](image.png)

**Fig 4-3** Saturated load inverter using enhancement mode n-type TFTs. Beta ratio = 

$$\frac{W_D}{L_D} / \frac{W_L}{L_L}$$
In Fig 4-3, the inverter uses transistor in saturation region as load. When the input level is high (i.e., $V_{DD}$), due to positive $V_{TH}$, both load and driver transistors are conducting and the output level is gradually pulled to close to low (i.e., ground: GND) depending on the sizing ratio ‘beta’. The beta ratio describes the relationship between the width/length ratios of driver and load transistors:

$$\beta = \frac{W_D/L_D}{W_L/L_L}$$

When the input level is low, load provides a strong pull-up force and pulls the output level close to $V_{DD}$. The key drawbacks for this design are poor noise margin due to asymmetric transfer characteristics and slow switching speed. Noise margin for the inverter
The circuit can be graphically extracted from the Fig 4-5 as explained previously. The worst case scenario of $\text{NM}_H = \text{NM}_L$ is considered here and width of the square comes out to be 0.8 V.

![Voltage transfer characteristics of inverter with noise margin extraction using maximum area (square) embedded within the VTC curve loop. Widths $W_L=20\mu\text{m}$, $W_D=100\mu\text{m}$ and lengths $L_L=L_D=10\mu\text{m}$.

**Fig 4-5** Voltage transfer characteristics of inverter with noise margin extraction using maximum area (square) embedded within the VTC curve loop. Widths $W_L=20\mu\text{m}$, $W_D=100\mu\text{m}$ and lengths $L_L=L_D=10\mu\text{m}$.

### 4.2.2. Inverters with different types of loads

An n-type only inverter can be implemented in multiple configurations depending on the type of load used. The most commonly used arrangement is the saturated load inverter where the load is a diode-connected transistor which always remains in saturation. Both the driver and the load transistors are operating in enhancement mode in the case considered. The
drawback of this structure is that the output reaches a maximum voltage of $V_{DD} - V_T$ due to the threshold voltage drop across the load transistor. An alternate configuration is achieved when the active load is supplied separate gate bias $V_G$ which is at least $V_{TH}$ volts more than $V_{DD}$. In this case, the load operated in linear regime, since $V_G > V_{DD} + V_{TH}$.

Both the above examples used active loads for inverter. A resistor is the simplest type of passive load. As shown in Fig 4-6(c), resistor ‘Res’ is used to pull the output high, whereas $M_D$ is the driver transistor used to pull the output low. The key drawbacks of using resistive load are higher power consumption and increased area required to implement the resistor on-chip. All the three cases mentioned belong to the ‘Ratioed Logic’ category, since the output level depends on the ratio of the impedances (and hence W/L ratios) of the pull-up and the pull-down devices.
**Fig 4-6** Inverter circuits with different loads (a) transistor in saturation regime (b) transistor in linear regime (c) resistive load.

**Fig 4-7** Comparison between transient responses of the different inverter loads.
The rise time, fall time, propagation delay and power consumption of inverters with different loads was measured from Fig 4-6 and is summarized in Table 4-2. Propagation delay is specified for both rising and falling edges of the pulse. As indicated, the rise and fall times are asymmetric for all loads, rise time being much higher. Also, the propagation delay on rising edge is greater than that for falling edge. This depicts that the pull-down strength of the inverters is larger than the pull-up strength. A beta ratio of $\beta=5$ was chosen to achieve good output voltage swing. Several simulation cycles with gradually increasing value of resistive load ‘Res’ were performed, and the value $0.6M\Omega$ was selected upon obtaining a good output swing. The resistive load exhibits least propagation delay for both rising edge and falling edge, whereas it consumes the most power.
Fig 4-8 Transient response of the inverter with resistive load with changing ‘Res’ value.

4.2.3. Effect of varying beta ratio ‘β’ and voltage supply $V_{DD}$

The propagation delay and output voltage swing of an inverter is influenced by the sizing of the driver and load transistors. The larger the beta ratio, the greater is the pull down strength of an inverter as a result of which the output swing decreases. In Fig 4-9(a), transient responses of inverter are compared at 0.1 MHz frequency. The output voltage level can be regulated and shifted up by decreasing the beta ratio. At the value $β=5$ optimum result in terms of output swing is obtained. As seen from the Fig 4-9(b), $β=20$ gives a sharper voltage transfer characteristic and consequently improved noise margins as compared to lower beta values.
Fig 4-9 (a) Transient response (b) Voltage transfer characteristics. The figure shows performance comparison of inverter with varying beta ratio. The lengths are $L_D = L_L = 10\mu m$ and width $W_L$ is constant at $20\mu m$. $W_D$ is equal to $\beta \times W_L$.

**Figure 4-10** Comparison of transfer characteristics of the inverter with increasing values of voltage supply $V_{DD} (V)$
The effect of varying voltage supply $V_{DD}$ is depicted in Fig 4-10. The transfer characteristics have the same shape, but the ‘low’ output stabilizes at different voltage levels. In the case of $V_{DD} = 5$V, the output stabilizes at nearly 0.43 volts at $V_{IN} = 20$ V. With higher $V_{DD}$ values, the output keeps increasing, and at $V_{DD} = 20$ V, the ‘low’ output saturates at nearly 1.5 V. The voltage transfer characteristics are largely skewed for a-IGZO TFT since they have very low $V_{IL}$. For these types of TFTs, n-type logic is the preferred circuit topology.

In 2009, Huang et al. [45] proposed a novel circuit topology for a-Si TFTs in the form of pseudo-C inverter. The pseudo-C inverter consists of only mono-type (p-type or n-type) TFTs and relies on a level-shifting stage ($M_I/M_D$) to improve the output voltage swing. As a result, voltage transfer characteristics tend to become symmetrical, and noise margin improves significantly. Motivated by the proposed circuit [45] and limited by non-availability of p-type a-IGZO TFTs, n-type pseudo-complementary (pseudo-C for short) inverters using n-type a-IGZO TFTs were designed. Fig 4-11 illustrates the circuit schematic of pseudo-C inverter.
For pseudo-C inverters, with the additional terminal that is set at approximately $V_{DD} + 2V_{TH}$, the required area can be greatly reduced to achieve a rail-to-rail voltage swing. Figure 4-11 shows the pseudo-C inverter design using n-type TFTs. For an n-type inverter, $V_{SS}$ is set to be no lower than $V_{DD}$. When the $V_{IN}$ level is low, both $M_D$ and $M_{Dn}$ are switched OFF and $V_{IM}$ is pulled to approximately $V_{DD}-V_{TH}$. $M_{Up}$ is then switched ON and $V_{OUT}$ is pulled to approximately $V_{DD}-2V_{TH}$. To make $V_{OUT}$ as high as $V_{DD}$, $V_{SS}$ can be set higher than $V_{DD}+2V_{TH}$. For the purpose of comparison between saturated load inverter and pseudo-C inverter both the circuits have been designed using the same $\beta$ ratio. The widths $W_D/W_L=100\mu m/20\mu m$ have been used for both type of inverters. For pseudo-C inverter the level shifter stage has widths $W_{Up}/W_{Dn} = 50\mu m/20\mu m$ and $V_{SS}$ is held at 20.5 V, which is greater than $(V_{DD} + 2V_{TH})$ or $(20 + 2\times0.1)$ volts. All the gate lengths are fixed at 10\mu m. Fig 4-12(a) shows the comparison of voltage transfer characteristics. The output voltage for
‘low’ binary state for a pseudo-C inverter is 0.2 V, which is more than 80% improvement from the saturated load inverter, which stabilized at 1.5 V. Fig 4-12 (b) also shows the noise margin of pseudo-C inverter, which is an improvement of almost 200% over saturated load inverter.

**Fig 4-12** (a) Comparison between a saturated load inverter and a pseudo-C inverter with the same beta ratio (β=5) (b) Improved noise margin of pseudo-C inverter.

**Fig 4-13** Comparison for pseudo-C inverter VTCs as a function of voltage supply $V_{SS}$. 
The voltage transfer characteristic of pseudo-C inverter and noise margin depends on another factor; $V_{SS}$. DC simulation was performed for three $V_{SS}$ values, 20.5 V, 22 V and 24 V. For higher $V_{SS}$ value, VTC shifts and exhibits more symmetrical behavior, while output ‘low’ level worsens. The overall pseudo-C inverter performance improves, since noise margins are better. This inverter circuit has been used as part of some Boolean gates contained in section 4.3.

4.2.4. Ring Oscillators

A ring oscillator is a circuit composed of an odd number of inverters whose output oscillates between high and low binary voltage levels. Since an inverter computes the logical NOT of its input, the last output of a chain of an odd number of inverters is the logical NOT of the first input. Ring oscillators are often used to demonstrate the speed performance of a new circuit technology. In this section, a-IGZO TFT saturated load inverters were used to construct the ring oscillator. The schematic of a simple 7-inverter ring oscillator (RO) is depicted in Fig 4-14. The output frequency of a RO with ‘n’ stages is given by:

$$f_{out} = \frac{1}{2n \times \text{delay}}$$
A 7-stage ring oscillator formed using saturated load inverter (circuit diagram of inverter in Fig 4-3).

Fig 4-15 (a) Transient response of the 7-stage ring oscillator. (b) Plot showing variation of frequency of the 5-stage ring oscillator with increasing β ratio of the inverters.

The transient response of 7-stage and 5-stage ring oscillators is shown in Fig 4-15 (a). Both the ROs are made of saturated load inverters using transistor widths $W_D/W_L=100\mu m/20\mu m$, while the lengths are kept constant at $L_D=L_L=10\mu m$. For simulation, nominal load capacitances of value 1fF were used in all the intermediate nodes. The 7-stage RO has larger total propagation delay (time period) and hence lesser frequency, while it has larger output voltage swing. The output swing decreases with increasing frequency of the
ring oscillator. The ring oscillators were also simulated with increasing beta ratio of the constituent inverters. Figure 4-15(b) shows the trend in frequency with increase in the beta ratio, attributed to increased pull-down strength of the inverters, and therefore the loading effect on consequent stages. Simulations were performed for high mobility devices to compare the results obtained with DUTs used in the thesis. Table 4-3 and 4-4 show the frequency values obtained.

**Table 4-3** Comparison showing frequency and output swing observed for ring oscillators using saturated load inverters and pseudo-complementary inverters.

<table>
<thead>
<tr>
<th>No. of stages</th>
<th>Type of inverter</th>
<th>Delay per stage (µs)</th>
<th>Frequency (KHz)</th>
<th>Voltage Swing (V)</th>
<th>Power consumed (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 stage</td>
<td>Saturation load</td>
<td>4.6</td>
<td>200</td>
<td>7.6</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>Pseudo-C</td>
<td>13.1</td>
<td>76.3</td>
<td>16.7</td>
<td>2.3</td>
</tr>
<tr>
<td>7 stage</td>
<td>Saturation load</td>
<td>7</td>
<td>140</td>
<td>10.1</td>
<td>2.8</td>
</tr>
<tr>
<td></td>
<td>Pseudo-C</td>
<td>18.6</td>
<td>54</td>
<td>18</td>
<td>3</td>
</tr>
</tbody>
</table>

**Table 4-4** Frequency and output swing observed for ring oscillators using saturated load inverters for device with high mobility of 12 cm²/Vs.

<table>
<thead>
<tr>
<th>No. of stages</th>
<th>Type of inverter</th>
<th>Delay per stage (µs)</th>
<th>Frequency (MHz)</th>
<th>Voltage Swing (V)</th>
<th>Power consumed (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 stage</td>
<td>Saturation load</td>
<td>530</td>
<td>1.8</td>
<td>10.5</td>
<td>1.3</td>
</tr>
<tr>
<td>7 stage</td>
<td>Saturation load</td>
<td>1</td>
<td>1</td>
<td>11.0</td>
<td>1.1</td>
</tr>
</tbody>
</table>
4.3. Digital logic gates

In the previous sections, a complete analysis of a-IGZO TFT inverter was done. This section takes a step further and discusses simulation results for digital circuits made using a-IGZO TFTs. A digital circuit is usually built from small electronic circuits called logic gates. Each logic gate represents a function of Boolean logic and is an arrangement of electrically controlled switches. The different types of inverters presented earlier have been used as components in some of the logic gates wherever NOT operation is required. There are two types of circuit topologies employed to build the Boolean logic gates, and their performance is compared to evaluate which style of circuits would suit a-IGZO TFTs best.

To achieve functionality in digital form, the output is required to achieve ‘rail-to-rail’ swing that represents binary logic, which is difficult to achieve in the case of a-IGZO TFT circuits due to non-availability of p-type TFTs. Hence all the circuits were optimized by altering the widths of the TFTs to achieve best possible frequency, while maintaining an output voltage swing of at least 15 V. Propagation delay is measured from mid-point of the inputs (VDD/2) to the mid-point of the observed output. It has been measured for both rising and falling edges of the pulses. Rise time refers to the time required for a signal to change from a specified low value to a specified high value. Typically, these values are 10% and 90% of the step height. For each circuit, rise and fall times are reported, and power consumption is computed using .MEAS commands in HSPICE®. The gates simulated are described briefly along with their logic functions and schematic diagrams below. The simulation results are reported in tables 4-3, 4-4 and 4-5.
4.3.1. N-type only logic

In n-type only logic, the n-channel TFTs are arranged in a pull-down network (PDN) between the logic gate output and ground, while active/passive load is placed between the logic gate output and the positive supply voltage $V_{DD}$. The circuit is designed such that if the desired output is low, then the PDN will be active, creating a direct current path between the ground and the output. Using this topology, the gates designed are AND2, OR2, NAND2 and NOR2. The truth tables and standard symbols of the gates are given in Table 4-5.

4.3.1.1. AND2 Gate

The AND2 gate implements AND function between 2 inputs A and B, which means the value is ‘high’ if both of its operands are true; otherwise the output value is ‘low’. The gate uses saturated load transistor $M_L$ as active load, and incorporates n-type only inverter for NOT operation. The inputs A and B are respectively attached to the gates of two n-type TFT transistors arranged in a stack. As a result the output becomes ‘high’ only when both $M_1$ and $M_2$ are ‘on’. The output is loaded with a small capacitance of value $C_L = 50 \, \text{fF}$. A comparison of output waveforms at two different frequencies 50 KHz and 0.2 MHz is presented in Fig 4-16. As indicated by the figure, the output wave is sharper for lower frequency (50 KHz) and exhibits an output voltage swing of about 15.25 V, whereas it reduces to 15 V for 0.2 MHz. The frequency 0.2 MHz is reported as maximum frequency for AND gate, since beyond this value the output wave starts to produce glitches and distortions.
**Fig 4-16** Transient responses of digital AND gate at (a) 50 KHz (b) 0.2 MHz

**Fig 4-17** Transient response of digital AND gate at various rise times (0.5µs, 2µs and 4µs) of the input pulses.
All the simulated digital gates including AND gate exhibit large output voltage overshoot and undershoot peaks when the input voltage pulse begins to transition from 0–1 and 1–0 V, respectively. This may be due to the presence of gate-to-drain capacitance $C_{GD}$ of the pull-down transistors, as confirmed by a transient analysis shown in Fig 4-17. The $C_{GD}$ capacitance acts in parallel to the load capacitance $C_L = 50\text{fF}$. Considering the AND gate schematic from fig 4-18, when the inputs become ‘LOW’, $V_A$ and $V_B$ are suddenly pulled down, while the output node $V_{OUT}$ is still at ‘high’ potential. Due to the sudden change in voltage across gate to drain of $M_1$ transistor, Miller capacitance comes into effect, due to which the spikes or overshoot is observed.

4.3.1.2. OR2 Gate

The OR gate is a digital logic gate implementing a function that results in 'high' output if one or both the inputs to the gate are 'high'. If neither input is 'high', a 'low' output level results. This gate also uses saturated load transistor $M_L$ as active load, and incorporates n-type only inverter for NOT operation. The inputs A and B are connected to the gates of NMOS transistors $M_1$ and $M_2$ arranged in parallel fashion. The output becomes ‘low’ only when both $M_1$ and $M_2$ are ‘off’. The output is loaded with a small capacitance of value 50 fF.
4.3.1.3. NAND2 Gate

NAND gate implements the negation of AND gate. It is a universal gate, since combinations of NAND gate can be used to accomplish any of the basic operations. The output is high when either of inputs is 'high', or if neither is 'high'. In other words, it is normally high, going low only if both the inputs become 'high'. It uses diode-connected transistor as active load. The output is loaded with a small capacitance of value 50 fF.

4.3.1.4. NOR2 Gate

The NOR gate is a digital logic gate that implements logical NOR. A 'high' output results if both the inputs to the gate are 'low'. If one or both input is 'high', a 'low' output results. NOR is the result of the negation of the OR operator. It is a functionally complete operation gate just like NAND gate; combinations of NOR gates can be combined to generate all possible truth tables. It uses diode-connected transistor as active load. The output is loaded with a small capacitance of value 50 fF.

Table 4-5 Truth Table for digital logic gates made using n-type only topology.

<table>
<thead>
<tr>
<th>Input $V_A$</th>
<th>Input $V_B$</th>
<th>Output $V_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>AND2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

65
Fig 4-18 Schematics of digital logic gates (a) AND2 (b) OR2 (c) NAND2 (d) NOR2

Fig 4-19 Transient responses of digital logic gates at 0.2 MHz, maximum achieved frequency for robust output (a) AND2 (b) OR2 (c) NAND2 (d) NOR2
Table 4-6 Various figures of merit observed for n-type only logic a-IGZO TFT circuits.

<table>
<thead>
<tr>
<th>Circuit</th>
<th># TFTs</th>
<th>Max frequency (MHz)</th>
<th>Propagation delay (µs)</th>
<th>Power (µW)</th>
<th>Output Swing (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rising edge</td>
<td>Falling edge</td>
<td></td>
</tr>
<tr>
<td>AND2</td>
<td>5</td>
<td>0.2</td>
<td>0.56</td>
<td>0.08</td>
<td>221.3</td>
</tr>
<tr>
<td>OR2</td>
<td>5</td>
<td>0.2</td>
<td>0.36</td>
<td>0.04</td>
<td>463</td>
</tr>
<tr>
<td>NAND2</td>
<td>3</td>
<td>0.2</td>
<td>0.5</td>
<td>1.4</td>
<td>771.3</td>
</tr>
<tr>
<td>NOR2</td>
<td>3</td>
<td>0.2</td>
<td>0.4</td>
<td>0.9</td>
<td>813</td>
</tr>
</tbody>
</table>

4.3.2. Pass transistor (PT) logic

Pass transistor logic uses transistors in series that whose gates act as select lines between possible output values of the logic. The output drives an inverter to generate the non-inverted output signal. To obtain the inverted values of inputs ‘a’ and ‘b’ which are ‘abar’ and ‘bbar’ respectively, saturated load inverters described previously are employed. Using this topology, the gates designed using this topology are XOR2, XNOR2, NAND2 and NAND3. The truth table and standard symbols of these gates are given in Table 4-7.
4.3.2.1. XOR2 gate

The XOR gate is a digital logic gate that implements an exclusive OR function. A 'high' output results if one, and only one, of the inputs to the gate is true 'high'. In case both inputs are 'low', or both inputs are 'high', a 'low' output results. In other words XOR is "one or the other but not both". Considering two inputs ‘a’ and ‘b’, it implements the following expression-

\[ ab + abar \cdot bbar \]

The expression inside the NOT operation (bar) is realized using the pass transistors M₁ and M₂, after which a saturated load inverter is used to negate the value to give the final output.

4.3.2.2. XNOR2 gate

The XNOR gate is a digital logic gate whose function is the inverse of the exclusive OR (XOR) gate. It results in 'high' output if both the inputs to the gate are equal. If one but not both inputs are 'high', a 'low' output results. It has two inputs ‘a’ and ‘b’; it implements the following expression-

\[ a \cdot bbar + b \cdot abar \]

The expression inside the NOT operation (bar) is realized using the pass transistors M₁ and M₂, after which a saturated load inverter is used to negate the value to provide the final output.
4.3.2.3. NAND2 and NAND3 gates

The two input NAND gate was again realized using pass transistor logic. This was done in order to compare the simulation results of the same logic gate using two different topologies. Also, a three-input NAND3 gate was implemented that uses two n-type transistors in series between ground and output inverter. The output inverter used for these two circuits was pseudo-C type inverter. As a result, the output swing is much higher as compared to n-type only gates.

Table 4-7 Truth Table for digital logic gates made using pass transistor logic.

<table>
<thead>
<tr>
<th>Input $V_A$</th>
<th>Input $V_B$</th>
<th>Output $V_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>XOR2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
**Fig 4-20** Schematics of digital logic gates (a) XOR2 (b) XNOR2 (c) NAND2 (d) NAND3

**Table 4-8** Various figures of merit observed for Pass transistor logic a-IGZO TFT circuits.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Max frequency (KHz)</th>
<th>Rise time (µs)</th>
<th>Fall time (µs)</th>
<th>Propagation delay (µs)</th>
<th>Power (mW)</th>
<th>Output Swing (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Rise edge</td>
<td>Fall edge</td>
<td></td>
</tr>
<tr>
<td>XOR2</td>
<td>400</td>
<td>1.1</td>
<td>0.26</td>
<td>0.5</td>
<td>0.3</td>
<td>0.2</td>
</tr>
<tr>
<td>XNOR2</td>
<td>400</td>
<td>0.9</td>
<td>0.56</td>
<td>0.6</td>
<td>0.3</td>
<td>0.5</td>
</tr>
<tr>
<td>NAND2</td>
<td>143</td>
<td>1.3</td>
<td>0.4</td>
<td>1.2</td>
<td>1.2</td>
<td>0.8</td>
</tr>
<tr>
<td>NAND3</td>
<td>143</td>
<td>1</td>
<td>0.6</td>
<td>0.9</td>
<td>0.36</td>
<td>1</td>
</tr>
</tbody>
</table>
**Fig 4.21** Transient responses of digital logic gates (a) XOR2 (b) XNOR2 (c) pass transistor NAND2 (d) pass transistor NAND3
CHAPTER 5

5. DESIGN OF Clocked a-IGZO TFT CIRCUITS

This chapter presents the design and simulations of clocked digital circuits made using a-IGZO TFTs. It also analyzes the results and various performance parameters obtained for each of them. An effort has been made to keep the total number of transistors in each design to a minimum figure in order to keep the design simple.

5.1. Synchronous circuits

In the logic circuits previously considered such as inverters, NAND or XOR logic gates, the output is directly related to the input by some logic combination. The circuits are therefore classified as combinational logic circuits.

There is a different class of circuits called ‘sequential’ logic circuits. The output depends not only on the present inputs, but also on the history of the inputs. Most of the sequential circuits contain a 'clock' signal, and all nodal voltages change only on a clock edge. The basic storage element in sequential logic is the flip-flop. The circuits simulated using a-IGZO TFTs in the following section are the D-Latch, D Flip-flop, frequency divider and three-bit counter.
5.1.1. D Latch

The D latch is used to capture, or ‘latch’ the logic level which is present on the Data line when the clock input is high. In the D latch, when the CLK input is logic 1, the Q output will always reflect the logic level present at the D input. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch, for use by the next circuit stage that may need this signal. Fig 5-1 illustrates the timing diagram of the D Latch.

![Timing diagram for the D Latch.](image)

**Fig 5-1** Timing diagram for the D Latch.

![Circuit diagram for the D Latch.](image)

**Fig 5-2** Circuit diagram for the D Latch.
The circuit design of D-Latch implemented using a-IGZO TFTs is given in Fig 5-2. The latching function is realized by pass transistors M₁ and M₂ as follows. When the positive CLK pulse arrives at the input, M₁ is turned on and M₂ turns off. The value at D input is transferred to node Vₓ. The CLK now becomes ‘LOW’, turning on M₂ and turning off M₁. The node Vₓ is now isolated from the input D, and since the M₂ transistor is conducting, inverters I₂ and I₃ form a pair of cross-coupled inverters and preserve the voltage value at output Q. The inverters I₁, I₂, I₃ and I₄ have been implemented in two forms: n-type only logic and pseudo-complementary inverter. The transient responses of D Latch using the two styles are shown in Fig 5-3 and various circuit parameters compared are given in Table 5-1. As seen from the table, the use of pseudo-complementary inverter as level shifter gives a higher maximum frequency and improves the output swing by 30%. The Vₛₛ value used as extra power supply in the case of pseudo-C inverters is 20.5 V.

### Table 5-1 Performance measure of the D Latch in terms of frequency achieved and power consumed.

<table>
<thead>
<tr>
<th>Type of inverter used</th>
<th># TFTs</th>
<th>Max frequency (KHz)</th>
<th>Rise time (µs)</th>
<th>Fall time (µs)</th>
<th>Propagation delay (µs)</th>
<th>Power (mW)</th>
<th>Output Swing (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturated load</td>
<td>12</td>
<td>100</td>
<td>1.1</td>
<td>1.9</td>
<td>0.8</td>
<td>2.1</td>
<td>14.0</td>
</tr>
<tr>
<td>Pseudo-C</td>
<td>22</td>
<td>143</td>
<td>2.6</td>
<td>1.2</td>
<td>2.2</td>
<td>2.2</td>
<td>18.2</td>
</tr>
</tbody>
</table>
**Fig 5-3** Comparison of the transient response of D Latch output Q1 (saturated load inverters) and Q2 (pseudo-complementary inverters) at frequency 100 KHz.

### 5.1.2. D Flip-flop

A D-type flip-flop is a clocked circuit used to provide delay and its main functions include data storage and frequency division. It is treated as a basic memory cell, and is used to construct counters and shift registers. The D flip-flop tracks input, making transitions which match those of the input D at the active edge of the clock. Q stores the data until the next active edge of the clock, when new data is available. The timing diagram for a positive edge triggered flip flop is shown in Fig 5-4.
Fig 5-4 Timing diagram for the positive-edge triggered D Flip-flop

Fig 5-5 Circuit diagram for the D Flip-flop using a-IGZO TFTs.

The circuit design of D flip-flop made using a-IGZO TFTs is given in Fig 5-5. It can be divided into three parts- master latch, slave latch and level shifters. The master latch is
transparent for positive CLK level, whereas the slave latch is transparent for the negative CLK level. This circuit uses pass transistor logic (\(M_1, M_2, M_3\) and \(M_4\)), and the voltage supply is needed only for the inverters. Transistors \(M_1\) and \(M_2\) have width 100\(\mu\)m, whereas \(M_3\) and \(M_4\) have widths 20\(\mu\)m. All the lengths are 10\(\mu\)m. The inverters \(I_1\) and \(I_2\) form a cross-coupled pair and preserve the voltage before it is captured in the other cross-coupled pair \(I_3\) and \(I_4\). The output level shifters use voltage supply of \(V_{D1} = V_{D2} = 20\) V. To improve performance of the circuit, pseudo-complementary inverters were employed in place of saturated load inverters \(I_1, I_2, I_3\) and \(I_4\). In this case, improvement in the output swing up to 45% was observed. The voltage supply \(V_{SS}\) used is 20.5 V. The transient responses of D flip-flop in the two cases were compared and are as shown in Fig 5-6 and various circuit parameters measured are given in Table 5-2.

### Table 5-2 Performance measure of the D flip-flop.

<table>
<thead>
<tr>
<th>Type of Inverter</th>
<th># TFTs</th>
<th>Max frequency (KHz)</th>
<th>Rise time ((\mu)s)</th>
<th>Fall time ((\mu)s)</th>
<th>Propagation delay ((\mu)s)</th>
<th>Power (mW)</th>
<th>Output Swing (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturated Load</td>
<td>20</td>
<td>100</td>
<td>3.5</td>
<td>2.5</td>
<td>3.1</td>
<td>2.8</td>
<td>2.17</td>
</tr>
<tr>
<td>Pseudo-C</td>
<td>32</td>
<td>100</td>
<td>2.6</td>
<td>1.9</td>
<td>6.6</td>
<td>5.9</td>
<td>2.7</td>
</tr>
</tbody>
</table>
Fig 5-6 Comparison of the transient response of D Flip-flop output Q1 (saturated load inverters) and Q2 (pseudo-complementary inverters) at frequency 100 KHz.

5.1.3. Frequency divider and 3-bit counter

A frequency divider is a circuit that takes an input signal of a frequency, $f_{IN}$, and generates an output signal of a frequency-

$$f_{OUT} = \frac{f_{IN}}{n}$$

where $n$ is an integer. An arrangement of D flip-flops in series can be used for integer-$n$ division. The easiest configuration is a series where each D flip-flop is a divide-by-2. Here
the inverted output terminal Qbar is connected directly back to the Data input terminal D giving the device "feedback" as shown in fig 5-7. By doing this, the output pulses at Q with frequency that is exactly one half \( (f/2) \) that of the input clock frequency. In other words the circuit produces frequency division and can work as a counter. This type of counter called a "ripple counter" and in ripple counters, the clock pulse triggers the first flip-flop whose output triggers the second flip-flop, which in-turn triggers the third flip-flop and so on through the chain. For a series of three of such flip-flops, such system would be a divide-by-8.

![Diagram of a divide-by-two counter or a frequency divider](image)

**Fig 5-7** Representation of a divide-by-two counter or a frequency divider.

![Block diagram of a 3 bit counter](image)

**Fig 5-8** Block diagram representation of the 3 bit counter.
Table 5-3 Power and Output Swing observed for Frequency Divider.

<table>
<thead>
<tr>
<th>Power (mW)</th>
<th>Output Swing (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.3</td>
<td>16</td>
</tr>
</tbody>
</table>

**Fig 5-9** Measured frequency and output swing for the 3-bit counter circuit at 50 KHz.

The D flip-flop explained in previous section was first modified into a divide-by-two counter circuit. This structure was repeated thrice in a series till divide-by-8 operation or a 3-bit counter circuit was achieved. All the inverters used in this structure are saturated load type and have beta ratio of 6, \( W_D/W_L \) being 120\( \mu \text{m} \)/20\( \mu \text{m} \). The pass transistors \( M_1 \) and \( M_3 \)
used in the 3-bit counter (refer to Fig 5-5) have widths equal to 120µm, and transistors $M_2$ and $M_4$ have widths equal to 30µm respectively. The input CLK period was 20µs with a rise time of 100ns. The outputs of the frequency divider were tapped at nodes $Q_1$, $Q_2$ and $Q_3$ which are divide-by-2, divide-by-4 and divide-by-8 respectively. The output swing was measured for all three transient outputs as 16 V, and the circuit dissipated more than thrice the amount of power than a D flip-flop analyzed in previous section.
CHAPTER 6

6. CONCLUSIONS AND FUTURE WORK

The focus of thesis has been to showcase performance and dynamic characteristics of a-IGZO TFT circuits simulated using adapted a-Si Level 61 TFT model. This chapter summarizes the conclusions drawn from the experimental data of the fabricated amorphous IGZO TFTs, the adapted a-Si TFT model and a-IGZO TFT circuits designed using the model. In addition, this chapter also discusses suggestions for future work.

6.1. Conclusions

This thesis presented a technique to simulate n-type a-IGZO TFT circuits by studying their dynamic characteristics, performance and encountered limitations. Since currently there is no simulation model available for a-IGZO TFTs, the semi-empirical a-Si RPI TFT (Level 61) model has been adapted to suit the current-voltage characteristics of a fabricated a-IGZO TFT device.

In Chapter 3, DC characterization and analysis of the electrical performance of fabricated inverted-staggered, n-type enhancement mode a-IGZO TFTs was presented. The required a-IGZO TFT SPICE parameters were extracted from measured data and plugged in the model parameters. The resultant simulated I-V curves matched within ±15% of the measured data in post-saturation region.
In chapter 4, design of a-IGZO TFT circuits using two different topologies: n-type only logic and pass transistor (PT) logic was shown. The major limitations of a-IGZO technology include low mobility (as compared to MOSFETs), requirement of high voltage supply and non-availability of p-type devices. The Pass Transistor logic style was demonstrated to suit better than n-type only topology for a-IGZO circuit design in terms of speed performance and output voltage swing. Design and simulations based on complex circuits like D flip-flop and 3-bit counter have been demonstrated, which show the ability of a-IGZO TFT devices to be used in transparent circuit applications. All a-IGZO TFT circuits exhibited >75% $V_{DD}$ output swing. It also demonstrated the level of performance expected from a-IGZO TFTs.

6.2. Future Work

Amorphous IGZO is a relatively new material with research in progress for better understanding of the TFT operation, the physics behind it, processing steps and its applications. Further investigation of the a-IGZO TFT characterization for the instability mechanisms is required. The work presented here in terms of fitting model to measured data requires better modeling and curve-fitting techniques for $V_{GS}$ bias voltages below threshold. However the simulation results indicate that a-IGZO TFTs are very suitable as technology for faster display rates.
REFERENCES


1. **Device Dimensions used in the Circuits**

The following section gives details about parameters used in HSPICE® simulations and the dimensions of the transistors used in digital logic gates and circuits designed in the thesis.

For all circuits:

- Power Supply $V_{DD} = 20$ V.
- Logic ‘HIGH’ = 20 V.
- Logic ‘LOW’ = 0 V.

1.1. **Saturated load inverter**

$M_L$: $W_L = 20 \mu$m, $L_L = 10 \mu$m  

$M_D$: $W_D = 100 \mu$m, $L_D = 10 \mu$m  

$C_L = 50$ fF

1.2. **Linear load inverter**

$M_L$: $W_L = 20 \mu$m, $L_L = 10 \mu$m  

$M_D$: $W_D = 100 \mu$m, $L_D = 10 \mu$m  

$C_L = 50$ fF  

$V_G = 20.5$ V
1.3. Resistive load inverter

Res = 6 \times 10^5 \Omega

M_D: W_D = 100 \mu m, L_D = 10 \mu m

C_L = 50 fF

1.4. Pseudo-complementary inverter

M_L: W_L = 20 \mu m, L_L = 10 \mu m

M_D: W_D = 100 \mu m, L_D = 10 \mu m

M_{Up}: W_1 = 50 \mu m, L_1 = 10 \mu m

M_{Dn}: W_2 = 20 \mu m, L_2 = 10 \mu m

C_L = 50 fF

V_{SS} = 20.5 V

1.5. AND gate

M_L: W_L = 20 \mu m, L_L = 10 \mu m

M_1: W_1 = 400 \mu m, L_1 = 10 \mu m

M_2: W_2 = 400 \mu m, L_2 = 10 \mu m

C_L = 50 fF

Sub-circuit inverter I_1:

M_L: W_L = 20 \mu m, L_L = 10 \mu m

M_D: W_D = 80 \mu m, L_D = 10 \mu m
1.6. OR gate

\[ \text{M}_L: \ W_L = 20 \ \mu m, \ L_L = 10 \ \mu m \]
\[ \text{M}_1: \ W_1 = 175 \ \mu m, \ L_1 = 10 \ \mu m \]
\[ \text{M}_2: \ W_2 = 175 \ \mu m, \ L_2 = 10 \ \mu m \]
\[ C_L = 50 \ \text{fF} \]

Sub-circuit inverter I₁:

\[ \text{M}_L: \ W_L = 20 \ \mu m, \ L_L = 10 \ \mu m \]
\[ \text{M}_D: \ W_D = 100 \ \mu m, \ L_D = 10 \ \mu m \]

1.7. NAND gate

\[ \text{M}_L: \ W_L = 20 \ \mu m, \ L_L = 10 \ \mu m \]
\[ \text{M}_1: \ W_1 = 100 \ \mu m, \ L_1 = 10 \ \mu m \]
\[ \text{M}_2: \ W_2 = 150 \ \mu m, \ L_2 = 10 \ \mu m \]
\[ C_L = 50 \ \text{fF} \]

1.8. NOR gate

\[ \text{M}_L: \ W_L = 20 \ \mu m, \ L_L = 10 \ \mu m \]
\[ \text{M}_1: \ W_1 = 50 \ \mu m, \ L_1 = 10 \ \mu m \]
\[ \text{M}_2: \ W_2 = 50 \ \mu m, \ L_2 = 10 \ \mu m \]
\[ C_L = 50 \ \text{fF} \]
1.9. XOR gate

M₁: \( W_1 = 200 \, \mu m, \, L_1 = 10 \, \mu m \)

M₂: \( W_2 = 200 \, \mu m, \, L_2 = 10 \, \mu m \)

\( C_L = 50 \, fF \)

Sub-circuit inverter \( I_1 \):

\( M_L: \, W_L = 20 \, \mu m, \, L_L = 10 \, \mu m \)

\( M_D: \, W_D = 100 \, \mu m, \, L_D = 10 \, \mu m \)

1.10. XNOR gate

M₁: \( W_1 = 120 \, \mu m, \, L_1 = 10 \, \mu m \)

M₂: \( W_2 = 120 \, \mu m, \, L_2 = 10 \, \mu m \)

\( C_L = 50 \, fF \)

Sub-circuit inverter \( I_1 \):

\( M_L: \, W_L = 20 \, \mu m, \, L_L = 10 \, \mu m \)

\( M_D: \, W_D = 80 \, \mu m, \, L_D = 10 \, \mu m \)

1.11. Pass transistor NAND2

M₁: \( W_1 = 100 \, \mu m, \, L_1 = 10 \, \mu m \)

M₂: \( W_2 = 100 \, \mu m, \, L_2 = 10 \, \mu m \)

\( C_L = 50 \, fF \)
Sub-circuit pseudo-C inverter I₁:

Mₐ: Wₐ = 30 µm, Lₐ = 10 µm
Mᵦ: Wᵦ = 120 µm, Lᵦ = 10 µm
Mᵢᵢ: Wᵢᵢ = 150 µm, Lᵢᵢ = 10 µm
Mᵦᵦ: Wᵦᵦ = 20 µm, Lᵦᵦ = 10 µm

1.12. Pass transistor NAND3

M₁: W₁ = 100 µm, L₁ = 10 µm
M₂: W₂ = 100 µm, L₂ = 10 µm
M₃: W₃ = 100 µm, L₃ = 10 µm
M₄: W₄ = 100 µm, L₄ = 10 µm
Cᵢ = 50 fF

Sub-circuit pseudo-C inverter Iᵢ:

Mₐ: Wₐ = 30 µm, Lₐ = 10 µm
Mᵦ: Wᵦ = 120 µm, Lᵦ = 10 µm
Mᵢᵢ: Wᵢᵢ = 150 µm, Lᵢᵢ = 10 µm
Mᵦᵦ: Wᵦᵦ = 20 µm, Lᵦᵦ = 10 µm
1.13. D Latch

$M_1$: $W_1 = 300 \mu m$, $L_1 = 10 \mu m$

$M_2$: $W_2 = 300 \mu m$, $L_2 = 10 \mu m$

$C_L = 50 \text{ fF}$

Sub-circuit inverter $I_1$ through $I_5$:

$M_L$: $W_L = 20 \mu m$, $L_L = 10 \mu m$

$M_D$: $W_D = 200 \mu m$, $L_D = 10 \mu m$

1.14. D Flip-flop

$M_1$: $W_1 = 100 \mu m$, $L_1 = 10 \mu m$    $M_5$: $W_5 = 30 \mu m$, $L_5 = 10 \mu m$

$M_2$: $W_2 = 20 \mu m$, $L_2 = 10 \mu m$    $M_6$: $W_6 = 120 \mu m$, $L_6 = 10 \mu m$

$M_3$: $W_3 = 100 \mu m$, $L_3 = 10 \mu m$    $M_7$: $W_7 = 30 \mu m$, $L_7 = 10 \mu m$

$M_4$: $W_4 = 20 \mu m$, $L_4 = 10 \mu m$    $M_8$: $W_8 = 120 \mu m$, $L_8 = 10 \mu m$

$C_L = 50 \text{ fF}$

$V_{D1} = V_{D2} = 24 \text{ V}$
Sub-circuit inverter I₁ through I₆:

M₄: W₄ = 20 µm, L₄ = 10 µm
M₅: W₅ = 70 µm, L₅ = 10 µm

1.15. Frequency divider and 3-bit counter

Sub-circuit D flip-flop D₁ through D₃:

Same as in 1.14 above.

Sub-circuit inverter I₁ through I₆:

M₄: W₄ = 20 µm, L₄ = 10 µm
M₅: W₅ = 70 µm, L₅ = 10 µm
2. **HSPICE® simulation files**

The extracts presented in this segment are taken from the HSPICE® files used for simulation.

2.1. **Inverter (saturated load)**

```verbatim
.GLOBAL vdd!
.PARAM vd=20 vdc=20 b=5
.TEMP 25
.OPTION
   + ARTIST=2
   + INGOLD=2
   + PARHIER=LOCAL
   + PSF=2
   + POST

.include '/afs/eos.ncsu.edu/lockers/research/ece/llunard/users/slothey/final_circuits/hspice_sims/tftnmos.m'

v0 vdd! 0 20
.VEC 'inv_invec.dat'
.tran 1p 200u SWEEP b 5 20 5
.MEAS TRAN Qtot INTEGRAL i(v0) FROM=0 TO=100u
.MEAS Etot PARAM='20*Qtot'
.MEAS Power PARAM='Etot/(100u)'

** Library name: Circuits
** Cell name: Inv
** View name: schematic
m0 vout vin 0 0 TFTNMOS L=10e-6 W=100e-6
m8 vdd! vdd! vout 0 TFTNMOS L=10e-6 W=200e-6
c0 vout 0 50f
.END
```
2.2. AND gate

.GLOBAL vdd!

.TEMP 25
.OPTION
+   ARTIST=2
+   INGOLD=2
+   PARHIER=LOCAL
+   PSF=2
+   POST

.include '/afs/eos.ncsu.edu/lockers/research/ece/llunard/users/slothey/final_circuits/hspice_sims/tftnmos.m'
Vdd VDD! 0 20
.VEC 'd_invec.dat'
.tran lp 100u

.MEAS TRAN Qtot INTEGRAL i(Vdd) FROM=0 TO=100u
.MEAS Etot PARAM='20*Qtot'
.MEAS Power PARAM='Etot/(100u)'

** Library name: Circuits
** Cell name: Inv
** View name: schematic
.subckt Inv vin vout inh_bulk_n
m0 vout vin 0 inh_bulk_n TFTNMOS L=10e-6 W=80e-6
m8 vdd! vdd! vout inh_bulk_n TFTNMOS L=10e-6 W=20e-6
.ends Inv

** End of subcircuit definition.

** Library name: Circuits
** Cell name: and
** View name: schematic
m0 net6 b 0 0 TFTNMOS L=10e-6 W=400e-6
m8 vdd! vdd! net12 0 TFTNMOS L=10e-6 W=20e-6
m1 net12 a net6 0 TFTNMOS L=10e-6 W=400e-6
xi0 net12 out 0 Inv
c0 out 0 50f
.END
### 2.3. Input vectors for AND gate

; Define the radix for each pin (1 for each pin)
radix 1 1

; List the pin names
vname a b

; Define pin I/O (i for each pin)
io i i

; Define time unit
tunit us

; Define slope of signal edge
slope 0.5

; Define high voltage
vih 20

; Define low voltage
vil 0

; Time delay
tdelay 0

; Define the period for the vectors
period 5

0 1
1 1
0 0
1 1
0 0
0 1
0 1
1 1
1 1
0 0
1 1
0 0
0 0
0 1
0 1
0 0
1 1
0 0
2.4. D flip-flop

```plaintext
 GLOBAL vdd!
.PARAM vd1=24 vdd=20 clkperiod=10u clkrise=500n

.TEMP 25
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST

Vdd VDD! 0 20
Vclk clk 0 PULSE 20 0 0 'clkrise' 'clkrise' 'clkperiod/2-clkrise' 'clkperiod'
.VEC 'dff_input.dat'
.include '/afs/eos.ncsu.edu/lockers/research/ece/llund/llund/users/slothey/final_circuits/hspice_sims/tftnmos.m'
.tran lp 400u

.MEAS TRAN Qtot INTEGRAL i(vdd) FROM=0 TO=100u
.MEAS Etot PARAM='20*Qtot'
.MEAS Power PARAM='Etot/(100u)'

** Library name: TFT_circuits
** Cell name: Inv
** View name: schematic
.subckt Inv vin vout inh_bulk_n
 m0 vout vin 0 inh_bulk_n TFTNMOS L=10e-6 W=70e-6
 m8 vdd! vdd! vout inh_bulk_n TFTNMOS L=10e-6 W=20e-6
.ends Inv
** End of subcircuit definition.

** Library name: TFT_circuits
** Cell name: dff
** View name: schematic

 v1 vd1 0 DC=vd1
 xi24 clk clb 0 Inv
 xi46 clb cl 0 Inv

 m4 d cl net14 0 TFTNMOS L=10e-6 W=100e-6
 m0 net11 clb net14 0 TFTNMOS L=10e-6 W=20e-6
 xi16 net14 l 0 Inv
 xi17 l net11 0 Inv

 m1 l clb net019 0 TFTNMOS L=10e-6 W=100e-6
 xi21 net019 net043 0 Inv
 xi36 net043 net020 0 Inv
 m2 net019 cl net020 0 TFTNMOS L=10e-6 W=20e-6

 m8 vd1 vd1 qb 0 TFTNMOS L=10e-6 W=30e-6
 m3 qb net043 0 0 TFTNMOS L=10e-6 W=120e-6
 m5 vd1 vd1 q 0 TFTNMOS L=10e-6 W=30e-6
 m6 q net020 0 0 TFTNMOS L=10e-6 W=120e-6

.END
```