ABSTRACT

MEITL, RYAN THOMAS. Gate Drive Circuits for High Voltage Power Converters using Coreless PCB Transformers. (Under the direction of Alex Q. Huang.)

With increasing availability of high voltage semiconductor switching devices, switching power converters are appearing in higher and higher voltage applications. In these higher voltage applications, the safe switching of these devices becomes increasingly important and expensive. Designing a reliable, inexpensive, versatile and high performance gate drive system is a significant challenge.

Most IGBT or power MOSFET switching devices in this new high voltage paradigm are operating in tandem with other similar devices, and thus are mutually reliant on their correct switching behaviour. In these modes of operation incorrect switching of one device can inflict significant capital damage and even result in death. It is therefore very important that gate drive systems contain features that increase safety and reliability. In inverter applications specific challenges that these features must meet include drive signal isolation and shoot-through protection.

In this thesis each function of a complete gate drive system will be analysed. Methods of isolation, protection, switch driving and providing power to the driver will be discussed. The noise effect of floating drivers during switching $dV/dt$ will be analysed and design guidelines established. A driver system utilizing core-less transformers for both signal isolation and power delivery will be presented and a simulation to predict the drivers performance will be shown. Then a program will be presented that easily predicts the characteristics of an arbitrary planar core-less transformer. Finally, a prototype is built to verify operation and four key functions are demonstrated: power and signal transfer, transformer isolation, transformer efficiency and $dV/dt$ performance.
Gate Drive Circuits for High Voltage Power Converters
using Coreless PCB Transformers

by
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Alex Q. Huang
Chair of Advisory Committee
DEDICATION

To my parents and my wife. Without your support I would not be where I am today. I am truly blessed.
The author, Ryan Meitl, was born in Davenport Iowa in 1985. He received his B.S. in Physics from Illinois State University in Spring 2009 and started to pursue his M.S. in Electrical Engineering at North Carolina State University in Fall 2009. He is passionate about technology and is specifically driven to reducing energy consumption and make alternative sources of energy more affordable and practical.
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Chapter 1

Introduction

1.1 Background

In today’s power power industry there is a drive towards continually growing integration of renewable energy sources, primarily wind and solar. In the automotive sector there is also a strong drive towards electric vehicles. Today’s legacy grid is ill-equipped to handle these highly erratic and somewhat unpredictable sources, in addition to the load challenges of massive fleets of electric vehicles connected to the grid. Today’s grid is also ill-equipped to take advantage of large banks of energy storage distributed throughout the grid from both electric vehicles and stationary distributed energy storage devices (DESDs). Successful integration of renewable energy sources into the grid requires DESDs and electric vehicle storage to make up for the intermittent nature of these sources. This requires major advances in the field of power electronics including advanced semiconductor devices, new topologies, and new control and protection schemes.

1.2 Motivation for higher voltage semiconductors

Since the development of widely available commercial IGBTs in the 1980’s power electronics practices for power management has slowly moved into higher and higher voltage ranges. The most common commercial IGBT’s are rated for 1kV and 1.2kV. Devices are available operating at 6kV and higher; however the upper limit for most industrial applications are in the 3kV - 4kV range. With the push to integrate renewables into the grid the need for higher devices has become immediate, because most primary distribution lines in the United States operate at around 13kV. These higher voltage semiconductor devices require gate drivers with higher isolation ratings, lower isolation capacitances and higher $dV/dt$ ratings.
1.3 Thesis Outline

In this thesis methods for driving IGBT and MOSFET power semiconductor devices are analysed. The impact of high voltage switching converters on gate driver operation is investigated and a driver system utilizing coreless PCB transformers is proposed that can drive devices at both current and future voltage levels. A prototype driver is built to verify the proposed system and experimental results are analysed to further improve performance.

In chapter 2 the fundamentals of gate drive circuits are reviewed. The purpose of the gate drive is explained and the challenges facing new high voltage gate drives shown. Finally, different methods for implementing the various stages in a gate drive system are shown and discussed.

In chapter 3 the coreless PCB transformer is presented. Principles of operation are reviewed and compared to a traditional core-wound transformer. Several methods for predicting the characteristics of arbitrary winding structures are discussed and compared. Finally, optimizations, EMI issues and the various applications of coreless transformers are shown.

In chapter 4 the Hurley and Duffy method for predicting characteristics of planar winding structures is explained in detail. An algorithm is built around their equations that allows for iterative design of arbitrary multi-layer multi-winding planar PCB transformers. The structure of this algorithm is explained and experimental verification of the predictions shown.

In chapter 5 the floating driver capacitive $dV/dt$ ground loop current is presented. A model is presented to simulate the effect of this current on the driver’s performance and the voltage disturbance is shown as a function of several circuit parameters. Finally, recommendations are made to minimize $dV/dt$ driver noise and a simple analysis method is shown to find the drivers $dV/dt$ rating.
Chapter 2

Gate drive circuit basics

2.1 Description

Gate drive circuits are integral parts of modern power electronics converters. The most common active switching devices used in modern power electronics are MOSFETs (metal oxide field effect transistors) and IGBTs (insulated gate bipolar transistors). Both of these devices are voltage controlled via the gate capacitance; specifically the gate-source capacitance for the MOSFET and the gate-emitter capacitance for the IGBT. Conduction begins when the gate reaches a certain threshold voltage relative to the source or emitter. The gate drive is responsible for turning these devices on and off.

![Mosfet and IGBT with parasitic capacitances](image.jpg)

Figure 2.1: Mosfet (left) and IGBT (right) with parasitic capacitances
The basic MOSFET and IGBT circuit models are shown with their parasitic capacitances in Figure 2.1. The gate-source and gate-emitter capacitances of the MOSFET and IGBT are much larger than the other parasitic capacitances.

The role of the gate drive is multi-faceted:

1. Mediate information between the control circuit and the switching device
2. Charge and discharge the gate capacitance, inducing switching
3. Isolate the volatile switching ground from the control ground
4. Act as the first line of defence against faults from incorrect switching or short circuits

The first two roles should be considered the gate drive core functions, and all practical drive circuits should have them. The second two roles can considered ancillary functions, and their requirement is set by the intended application. As the voltage level of switching converters increases, so does the critical nature of these ancillary functions. In very high voltage applications, gate drive circuits should perform all four of these functions. In medium and low voltage applications, gate drive circuits should perform all of these functions when the source/emitter is not tied to ground.

2.2 Applications

Gate drive circuits are needed wherever MOSFETs or IGBTs are utilized for power applications. In simple applications where the source/emitter of the switching device is shorted to ground, the drive system can be very simple and need only perform the core functions mentioned in the previous section. The need for the additional functions arises when a converter topology or application includes floating devices. This occurs whenever the source/emitter is not at the same potential as the bus ground during normal operation. Examples are the bridge configurations in VSIs (voltage source inverters) and other AC converters. This becomes particularly evident in high voltage applications, where the potential of the source/emitter of a single device can vary by close to the bus voltage. Traditionally in these situations substantial time and cost resources are spent developing an adequate drive system.
Consider the simple VSI in Figure 2.2 when switches BP and CN are conducting but all other switches are not conducting. Table 2.1 details this condition. The emitter of switch AP will be floating at half the bus voltage and the emitter of BP will be at the bus voltage. This occurs when AP and AN are in a switching transition, and AP has to be completely off before AN can conduct to avoid shoot-through. Neglecting on-state voltage drop all three high-side switches will have their emitter voltages swing from ground to the bus voltage during normal operation. This makes gate drives for a high-side switches far more complex than for low-side switches, especially in very high voltage applications.
2.3 System Overview

A full featured gate drive circuit consists of four distinct subsystems:

1. Logic Subsystem
   The logic subsystem processes control signals and reported faults

2. Driver Stage Subsystem
   The drive stage subsystem charges and discharges the power device’s gate capacitance

3. Isolation Subsystem
   The isolation subsystem provides protection and level shifting from the control ground to floating device ground

4. Fault Subsystem
   The fault detection subsystem takes measurements to determine the state of the power device and sends them to the logic subsystem for processing

Figure 2.3: A typical high-side gate driver system

These subsystems operate together in a straightforward manner.
Figure 2.4: Example system operation
2.4 Logic

The logic subsystem can consist of multiple discrete components or a programmable logic controller. The logic subsystem processes, buffers, filters and modulates control and state signals. A simple example would be a NOT and AND gate.

![Diagram of logic configuration](image)

Figure 2.5: Example logic configuration

The control signal for the power device is the first input for the AND gate in Figure 2.5. The state signal for a complementary device is high when on and low when off. This signal is inverted and sent to the second input of the AND gate. The control signal for the power device will pass when the complimentary device is off, and will be blocked when the complimentary device is on.

2.5 Driver

The driver subsystem can consist of either discrete semiconductor devices or ICs. Most modern drivers utilize ICs, which can offer similar or better performance while also offering a smaller PCB footprint. In this section we will consider basic topologies that that may be implemented discretely or on an IC.

2.5.1 Totem-Pole

The fundamental driver stage topology is the totem-pole.

This arrangement of two semiconductors in a bridge configuration allows the gate of the power device to be connected to either the positive drive voltage or the floating ground. Earlier drivers used two BJTs, an NPN and a PNP. Now many drivers use two MOSFETS, a PMOS and an NMOS. Both of these configurations usually contain a gate resistor network, which limits the turn-on/off rate of the power device. In most applications resistors of different values
are used for charge and discharge of the gate capacitance. This is due to the unique turn-on/off characteristics of MOSFETs and IGBTs. Typically the device should be turned on slowly to prevent turn-on induced oscillations from the miller effect; however, oscillations are less of an issue during turn off and therefore the gate can typically be discharged quickly. These oscillations are not the only limiting factor for turn-on and turn-off. The rate of discharge directly affects the device $dV/dt$ and will cause noise in connected circuits. This noise is discussed in Chapter 5.

### 2.5.2 Parallel Totem-Pole

Some newer drive topologies combine the benefits of BJTs and MOSFETs by having two totem-poles in parallel. This allows the BJTs to source current during the miller plateau while the MOSFETs provide low on-resistance during normal charging [7].

### 2.5.3 Current-Source

Another category of drive stages to be considered are resonant and current-source drivers. These still utilize the totem-pole configuration previously discussed, but with added inductive components to precisely control the charge and discharge current. These circuits can have the advantage of increased efficiency and easily adjustable turn-on and off times, at the cost of increased complexity [12].
2.6 Isolation

Isolation in drivers for medium to high voltage converters come in two different forms: signal isolation and power supply isolation. All converters utilizing high-side NMOS switches require drive signal isolation. Power supply isolation can come in several different forms, a few of which will be discussed in this section.

2.6.1 Optically Isolated Drive

One of the most common methods of signal isolation is through use of optocouplers. Optocouplers utilize light emitting and light sensitive materials to transmit a command signal across an air gap. An LED is utilized on the primary side and either a photo-diode or photo-transistor is turned on by the incident light on the secondary side. Signal propagation delay across optocouplers increases with isolation requirements. This delay becomes substantial at higher voltages, where the delay approaches 1 \mu s. Optocouplers with isolation ratings above 7kV are not
common and where available come at significant cost. Optocouplers are also not economical for power transmission, and therefore a floating power supply must provide the necessary drive current in a system utilizing optocouplers for signal isolation.

The primary method of providing power to a high-side switch is with a boot-strap power supply. A boot-strap supply is advantageous in that it has a low parts count and is simple. It’s primary disadvantage is that it has a limited power capacity and therefore cannot hold a switch on indefinitely.

![A simple bootstrap power supply](image)

Figure 2.9: A simple bootstrap power supply

The standard alternative to a boot-strap supply is a transformer isolated DC-DC converter [1]. This can however be very costly to implement at high voltages through design or off-the-shelf solutions. These isolated converters must be carefully designed or chosen for the given application, as $dV/dt$ noise can become a significant issue as will be discussed in Chapter 5.

### 2.6.2 Direct Transformer Drive

One transformer isolated method is to directly drive the power device from the transformer. The drive stage in this arrangement is on the control ground. In this arrangement the duty cycle is limited by the operational limits of the transformer, which must be kept from saturation. The transformer must also operate at the switching frequency of the converter.

### 2.6.3 Modulated Transformer Drive

Modulating the drive signal can allow more flexibility in the duty cycle. The command signal is modulated into an AC waveform on the low-side and de-modulated back into the original command signal on the floating side. A modulated transformer drive topology must include
either a rectifier for the floating supply or a separate isolated DC-DC converter. Boot-strap supplies are used in designs with modulated signals, but are not ideal for systems that require protection circuitry on the floating ground. The design demonstrated in this thesis utilizes a modulated drive signal.
2.7 Protection

There are three operational areas of protection for an IGBT or MOSFET: current, voltage and temperature. In this section over-voltage and over-current protection will be briefly presented.

2.7.1 Over Voltage

Stray inductance during device turn-off can induce voltage spikes that can exceed voltage ratings. There are several methods to mitigate this.

1. Minimize bus and lead stray inductance
2. Choose device ratings to handle turn-off voltage spikes.
3. Set turn-off speed by choosing gate resistors that lower turn-off voltage spikes.
4. Design an avalanche feedback circuit to slow device turn-off during over voltage conditions.

![Figure 2.12: A voltage clamping circuit](image)

An example of 3 is shown in Figure 2.12. The avalanche voltage of diode $D_z$ is set below the rated voltage, and if the device voltage $V_{ce}$ exceeds this value current will flow into the gate and slow device turn-off [6]

2.7.2 Over Current

Over current occurs in bridge configurations when both devices conduct current at the same time, causing a supply short. Over current can also occur if a short occurs at the load. In
Table 2.2: Overcurrent logic

<table>
<thead>
<tr>
<th>Situation</th>
<th>Comparator output</th>
<th>Gate Voltage</th>
<th>NAND output</th>
<th>Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT ON</td>
<td>LOW</td>
<td>HIGH</td>
<td>HIGH</td>
<td>ON</td>
</tr>
<tr>
<td>IGBT OFF</td>
<td>HIGH</td>
<td>LOW</td>
<td>HIGH</td>
<td>ON</td>
</tr>
<tr>
<td>Over current</td>
<td>HIGH</td>
<td>HIGH</td>
<td>LOW</td>
<td>OFF</td>
</tr>
</tbody>
</table>

the over current protection circuit of Figure 2.13 a current is injected across the IGBT during its on-state. If the device is on, a voltage drop occurs across resistor $R_1$ and the comparator will output low, the gate voltage will be high, and therefore the NAND gate will output high keeping the driver enabled. When the device is off the comparator will output high, and the gate voltage will be low, and therefore the NAND gate will output high keeping the driver enabled. If the device is undergoing over-current the voltage $V_{ce}$ will be large enough that the voltage drop across $R_1$ will trigger the comparator to output high, the gate voltage will be high, and therefore the NAND output will be low and the driver will be disabled. This is detailed in Table 2.2.

![Figure 2.13: An overcurrent protection circuit](image)

The output of the comparator may also be sent to a complimentary driver for the other bridge device to act as an enable signal [11].
2.8 Summary

In this chapter the fundamentals of gate drive design were presented. The logic, driver, isolation, and protection subsystems were each discussed and possible implementations shown.
Chapter 3

Coreless Planar Transformers

In Chapter 2 several methods for isolating control ground from the floating ground of a power device was presented. In this chapter the focus is on one particular method of isolation, coreless PCB transformers.

3.1 Benefits

Coreless PCB transformers offer significant cost and manufacturing advantages, and until recently they were tedious to model, design and implement. They can be fabricated on the same PCB with additional components, and they can utilize FR4’s very high dialectic strength (typ. > 20kV/mm) to achieve high voltage isolation. Because of their low profile, planar transformers are ideally suited for gate drives and low power isolated DC-DC, AC-DC and AC-AC converters.

3.2 Structure

Planar transformers can be printed on opposite sides of a multi-layer PCB and utilize FR4 as the insulator, or they can be printed on different PCB boards vertically separated by an air-gap as shown in Figure 3.1. Coupling becomes very weak when the distance becomes large, so the primary and secondary windings are typically in close proximity.

3.3 Planar Transformer Model

Planar coreless transformers behave in a very similar manner to conventional transformers. The circuit model is the same as shown in Figure 3.2 and Table 3.1.

The primary difference between coreless and cored transformers is that coreless transformers have a very low coupling coefficient. The coupling coefficient can be easily understood as the
fraction of the total primary current that is transferred to the secondary. It is defined as the relationship between the magnetizing inductance and the primary and secondary inductances.

\[ k = \frac{L_m}{\sqrt{L_p L_s}} \]  

(3.1)

The coupling coefficient is a measure of how efficient the transformer is. In a circular planar transformer the parameters that contribute most to the coupling coefficient are the separation between primary and secondary and the outermost radius of the windings. The relationship

Table 3.1: Transformer model parameters

<table>
<thead>
<tr>
<th>Variable</th>
<th>Definition</th>
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<tr>
<td>Cp</td>
<td>Primary capacitance</td>
</tr>
<tr>
<td>Cs'</td>
<td>Secondary capacitance referred to primary</td>
</tr>
<tr>
<td>Rp</td>
<td>Primary resistance</td>
</tr>
<tr>
<td>Rs'</td>
<td>Secondary resistance referred to primary</td>
</tr>
<tr>
<td>Lkp</td>
<td>Primary leakage inductance</td>
</tr>
<tr>
<td>Lks'</td>
<td>Secondary leakage inductance referred to primary</td>
</tr>
<tr>
<td>Lm</td>
<td>Magnetizing inductance</td>
</tr>
<tr>
<td>Cis</td>
<td>Primary to secondary coupling capacitance</td>
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</tbody>
</table>
between the coupling factor and the outermost radius with a fixed separation distance roughly follows $a + \frac{b}{x}$. With the coupling increasing as the outermost radius increases.

The relationship between the coupling factor and the separation distance with a fixed outermost radius roughly follows $a + e^{-x}$. With the coupling increasing as the separation between primary and secondary sides decreases.

This relationship is shown for a single winding primary and secondary. In Figure 3.3a the separation is 1mm and in Figure 3.3b the radius is 5mm.

PCB transformers are by nature 3-D structures. The windings must be represented in a 3-D coordinate system to account for conductor height and vertical separation between coils. Therefore methods of determining inductances for core-based transformers are not suitable for coreless transformers [9]. A method for determining the transformer inductances will be

Figure 3.3: Coupling coefficient vs. radius (a) and separation (b)
discussed in Chapter 4.

## 3.4 Optimizations

It is important to operate a coreless transformer at the maximum impedance frequency, this occurs just below the resonant frequency [3]. At this frequency the voltage gain of the transformer will be high and the phase shift will be low, despite low coupling compared with cored transformers. The voltage gain transfer function is given in [2].

\[
\frac{V_s}{V_p} = \frac{1}{n} \left( \frac{1}{R_p + sL_{lkp}} + \frac{sC_m'}{(R_s' + sL_{llks}') + \frac{1}{sL_m}} \right)
\]

\[\quad + \left( \frac{1}{R_s + sL_{lkp}} + sC_m + sC_s' + \frac{1}{n^2 R_L} \right) \left( \frac{1}{R_p + sL_{lkp}} + \frac{1}{sL_m} \right) + 1 \]

The transformer voltage transfer function is shown in Eq. 3.2, where the variables are those from Table 3.1 and \( R_L \) is the time-average load. The resonant frequency of the transformer is given by

\[
f_{res} = \frac{1}{2\pi \sqrt{L_{eq} C_{eq}}}.
\]

Where the equivalent inductance is

\[
L_{eq} = L_{llks}' + \frac{L_{lkp} || L_m}{(3.4)}
\]

and the equivalent capacitance is

\[
C_{eq} = C_s' + 2C_{is}.
\]

If the transformer resonant frequency is much higher than the desired operating frequency, a capacitor can be added in parallel with \( C_s' \) on the secondary to move the resonant frequency down to the desired location.

The transformer efficiency is a function of voltage gain, load, and effective input impedance. The efficiency of the transformer is

\[
\eta = \frac{P_{out}}{P_{in}} = \frac{(\frac{V_s}{V_p})^2}{R_L R E [\frac{1}{Z_{in}}]} \times 100,
\]

19
where
\[
Z_{in} = \frac{1}{sC_m(1 - n\frac{V_s}{V_p}) + \frac{1 - A}{X_p} + sC_p}
\]  
(3.7)
and
\[
A = \frac{sC_m + \frac{X_s}{X_p} Y_s}{Y},
\]
\[
Y = -\frac{1}{X_s} + Y_p Y_s,
\]
\[
Y_p = X_s \left[ \frac{1}{X_p} + \frac{1}{sL_m} \right] + 1,
\]
\[
Y_s = \frac{1}{X_s} + sC_m + sC'_m + \frac{1}{n^2 R_L},
\]
\[
X_p = R_p + sL_{lpk},
\]
\[
X_s = R'_s + sL'_{lks}.
\]

3.5 Electromagnetic Interference

In [4] the author examines the coreless PCB transformer as both an emitter and receiver of electromagnetic interference (EMI). Through simulations in Ansoft 3-D EM Field Solver and application of basic antenna theory it was found that a coreless transformer of outer radius 5mm was both a poor antenna and poor receiver of stray electromagnetic radiation. It was concluded that the transformer was not a significant source of EMI and produced less EMI than the device gate driver IC.

3.6 Summary

In this chapter the use of coreless pcb transformers for signal and power isolation was explored. The benefits, structure, and equivalent circuit model were discussed.
Chapter 4

Determining Planar Transformer Parameters

In chapter 3 we described coreless planar transformers and their applications. In this chapter an algorithm for designing coreless planar transformers will be developed around the Hurley and Duffy method for calculating mutual inductances of planar structures.

4.1 The Hurley and Duffy Method

The Hurley and Duffy method of calculation planar magnetic inductances is derived from the formula for mutual inductance between two filaments given by Maxwell,

\[
M = \mu_0 \pi ar \int_0^\infty J_1(kr)J_1(ka)e^{-k|z|} dk \tag{4.1}
\]

and the derivation can be found in [5]. The mutual inductance between two planar coils is given by

\[
M_{ij} = \frac{\mu_0 \pi}{\ln\left(\frac{r_{2i}}{r_{1i}}\right)\ln\left(\frac{a_{2j}}{a_{1j}}\right)} \int_0^\infty S(kr_{2i}, kr_{1i})S(ka_{2j}, ka_{1j})Q(\kappa h_i, \kappa h_j)e^{-kZ} dk \tag{4.2}
\]

where \(Z\) is the vertical separation between tracks,

\[
S(kr_{2i}, kr_{1i}) = \frac{J_0(kr_{2i}) - J_0(kr_{1i})}{k}, \tag{4.3}
\]

\[
S(kr_{2i}, kr_{1i}) = \frac{J_0(ka_{2j}) - J_0(ka_{1j})}{k}. \tag{4.4}
\]
Table 4.1: Hurley/Duffy method variables

<table>
<thead>
<tr>
<th>Variable</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$J_0$</td>
<td>zeroth order Bessel function of the first kind</td>
</tr>
<tr>
<td>$a_{1j}$</td>
<td>$j$th coil innermost radius</td>
</tr>
<tr>
<td>$a_{2j}$</td>
<td>$j$th coil outermost radius</td>
</tr>
<tr>
<td>$r_{1i}$</td>
<td>$i$th coil innermost radius</td>
</tr>
<tr>
<td>$r_{2i}$</td>
<td>$i$th coil outermost radius</td>
</tr>
<tr>
<td>$h_i$</td>
<td>$i$th coil copper thickness</td>
</tr>
<tr>
<td>$h_j$</td>
<td>$j$th coil copper thickness</td>
</tr>
<tr>
<td>$Z$</td>
<td>vertical separation between $i$th and $j$th coils</td>
</tr>
<tr>
<td>$N_p$</td>
<td>number of turns on primary</td>
</tr>
<tr>
<td>$N_s$</td>
<td>number of turns on secondary</td>
</tr>
</tbody>
</table>

and

$$Q(kh_i, kh_j) = \begin{cases} 
\frac{2}{k^2} \left( \cosh k \frac{h_i + h_j}{2} - \cosh k \frac{h_i - h_j}{2} \right) & \text{if } Z > \frac{h_i + h_j}{2} \\
\frac{k}{2} \left( h + e^{-kh} - 1 \right) & \text{else, } h_i = h_j = h. 
\end{cases} \quad (4.5)$$

These equations must be integrated computationally and therefore it is not possible to integrate to infinity. The upper limit of integration in the the algorithm is 5000, at which point the solutions tend to oscillate about the mean and not yield more precise results. The optimum upper-limit of integration is a problem for computational Mathematics.

4.2 Structure

4.2.1 Inductance Matrix

Iterating $M_{ij}$ over a winding structure yields a matrix of order $m \times m$ where

$$m = N_p + N_s.$$ 

The matrix structure is such that the primary self inductance is given by

$$L_p = \sum_{i=1}^{N_p} \sum_{j=1}^{N_p} M_{ij}, \quad (4.6)$$
the secondary self inductance is given by

\[ L_s = \sum_{i=N_p+1}^{N_p+N_s} \sum_{j=N_p+1}^{N_p+N_s} M_{ij}, \]  

and the mutual inductance is given by

\[ L_m = \sum_{i=1}^{N_p} \sum_{j=N_p+1}^{N_p+N_s} M_{ij}. \]  

The leakage inductance on the primary is therefore

\[ L_{lkp} = L_p - L_m \]  

and the leakage inductance on the secondary is

\[ L_{lks} = L_s - L_m. \]

Eq. 4.8, Eq. 4.9 and Eq. 4.10 can be used in Eq. 3.1 to determine the coupling coefficient of the transformer, as discussed in Chapter 3. Concerning strictly the primary, secondary, and mutual inductances the matrix structure is

\[ M_{ij} = \begin{pmatrix} L_p & L_m \\ L_m & L_s \end{pmatrix}. \]

In the matrix above, if the transformer primary and secondary contains two layers, \( L_p, L_s \) and \( L_m \) become tensors within \( M_{ij} \) and have the structure

\[ L_p = \begin{pmatrix} L_{ply1\leftrightarrow1} & L_{ply1\leftrightarrow2} \\ L_{ply2\leftrightarrow1} & L_{ply2\leftrightarrow2} \end{pmatrix}, \]

where \( L_{ply1\leftrightarrow1} \) is the inductance of layer one to itself, and \( L_{ply1\leftrightarrow2} \) is the mutual inductance of layer one to layer two. Consequently, \( L_s \) contains a similar structure and \( L_m \) has two structures that are transposes of one another. \( M_{21} \) is

\[ L_m = \begin{pmatrix} L_{ply1\leftrightarrowsly1} & L_{ply1\leftrightarrowsly2} \\ L_{ply2\leftrightarrowsly1} & L_{ply2\leftrightarrowsly2} \end{pmatrix}, \]

where \( L_{ply1\leftrightarrowsly1} \) is the mutual inductance between primary layer one and secondary layer one. If each transformer layer contains multiple windings, each layer’s mutual and self inductance becomes a tensor within \( L_p, L_s \) and \( L_m \). In a transformer with 2 windings per layer
\[ L_{\text{ply}1\leftrightarrow1} = \begin{pmatrix} L_{\text{ply}1\text{w}1\leftrightarrow\text{w}1} & L_{\text{ply}1\text{w}1\leftrightarrow\text{w}2} \\ L_{\text{ply}1\text{w}2\leftrightarrow\text{w}1} & L_{\text{ply}1\text{w}2\leftrightarrow\text{w}2} \end{pmatrix}, \]

where \( L_{\text{ply}1\text{w}1\leftrightarrow\text{w}2} \) is the mutual inductance between layer one winding one, and layer one winding two. For a transformer with primary and secondary windings of one layer each with two windings per layer the inductance matrix is

\[
M_{ij} = \begin{pmatrix}
L_{\text{ply}1\text{w}1\leftrightarrow\text{w}1} & L_{\text{ply}1\text{w}1\leftrightarrow\text{w}2} & L_{\text{ply}1\text{w}1\leftrightarrow\text{sl}y\text{w}1} & L_{\text{ply}1\text{w}1\leftrightarrow\text{sl}y\text{w}2} \\
L_{\text{ply}1\text{w}2\leftrightarrow\text{w}1} & L_{\text{ply}1\text{w}2\leftrightarrow\text{w}2} & L_{\text{ply}1\text{w}2\leftrightarrow\text{sl}y\text{w}1} & L_{\text{ply}1\text{w}2\leftrightarrow\text{sl}y\text{w}2} \\
L_{\text{sl}y\text{w}1\leftrightarrow\text{ply}1\text{w}1} & L_{\text{sl}y\text{w}1\leftrightarrow\text{ply}1\text{w}2} & L_{\text{sl}y\text{w}1\leftrightarrow\text{w}1} & L_{\text{sl}y\text{w}1\leftrightarrow\text{w}2} \\
L_{\text{sl}y\text{w}2\leftrightarrow\text{ply}1\text{w}1} & L_{\text{sl}y\text{w}2\leftrightarrow\text{ply}1\text{w}2} & L_{\text{sl}y\text{w}2\leftrightarrow\text{w}1} & L_{\text{sl}y\text{w}2\leftrightarrow\text{w}2}
\end{pmatrix}.
\]

### 4.2.2 Model Inputs

The model inputs are shown in Table 4.2. The vertical separation \( Z \) is a function of the PCB board thickness and air gap distance. For the 4-layer PCB in Figure 4.1 with the primary winding on the top copper and the secondary winding on the bottom copper

\[
Z = 2h + 2ld + l_{\text{core}}. \tag{4.11}
\]

### 4.2.3 Capacitance

The capacitance between primary and secondary is calculated via the equation for a parallel plate capacitor

\[
C = \frac{\epsilon A}{d}. \tag{4.12}
\]

The area of a vertically separated winding is equal to the area enclosed by a circle with the radius of the outer edge of the track minus the area enclosed by a circle with the radius of the inner edge of the track.

\[
A_{\text{vertical}} = \pi(r_{\text{outer}}^2 - r_{\text{inner}}^2) \tag{4.13}
\]

To calculate the area for capacitance between concentric windings the diameter of the winding is multiplied by the thickness of the track.

\[
A_{\text{concentric}} = 2\pi rh \tag{4.14}
\]

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For air gap separation $\epsilon = \epsilon_0$; however, for capacitance between concentric windings and capacitance for vertical windings with FR4 isolation $\epsilon \simeq 4.5\epsilon_0$. While the dialectic strength
Table 4.2: Algorithm inputs

<table>
<thead>
<tr>
<th>Variable</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_p$</td>
<td>number of turns on primary</td>
</tr>
<tr>
<td>$N_s$</td>
<td>number of turns on secondary</td>
</tr>
<tr>
<td>$n_l$</td>
<td>number of layers on primary and secondary</td>
</tr>
<tr>
<td>$l_d$</td>
<td>inner layer dialectic thickness (mm)</td>
</tr>
<tr>
<td>$l_{core}$</td>
<td>inner layer core thickness (mm)</td>
</tr>
<tr>
<td>$z_{dia}$</td>
<td>solder mask thickness (mm)</td>
</tr>
<tr>
<td>$z$</td>
<td>air gap (mm)</td>
</tr>
<tr>
<td>$h_p$</td>
<td>copper thickness of primary (µm)</td>
</tr>
<tr>
<td>$h_s$</td>
<td>copper thickness of secondary (µm)</td>
</tr>
<tr>
<td>$d_p$</td>
<td>distance between concentric windings on primary (mm)</td>
</tr>
<tr>
<td>$d_s$</td>
<td>distance between concentric windings on secondary (mm)</td>
</tr>
<tr>
<td>$w_p$</td>
<td>width of windings on primary (mm)</td>
</tr>
<tr>
<td>$w_s$</td>
<td>width of windings on secondary (mm)</td>
</tr>
<tr>
<td>$r_{in_p}$</td>
<td>radius of the innermost winding on primary (mm)</td>
</tr>
<tr>
<td>$r_{in_s}$</td>
<td>radius of the innermost winding on secondary (mm)</td>
</tr>
</tbody>
</table>

of FR4 is much higher than air, the permeability is also higher leading to larger coupling capacitance.

4.3 Computational Structure

The algorithm was implemented in Wolfram Mathematica, and outputs input variables and inductance values as comma separated (.csv).

4.3.1 Computation

Figure 4.3 illustrates the basic computational structure of the algorithm.
Figure 4.3: Algorithm flow chart
4.3.2 Variable Structure

The vertical separation distance \( Z_{ij} \) is represented by a \( n \times n \) matrix of the same form and order as the inductance matrix \( M_{ij} \), where \( n = N_p + N_s \). For a transformer with primary and secondary windings of one layer each with two windings per layer the separation matrix is

\[
Z_{ij} = \begin{pmatrix}
Z_{ply1w1++w1} & Z_{ply1w1++w2} & Z_{ply1w1++sly1w1} & Z_{ply1w1++sly1w2} \\
Z_{ply1w2++w1} & Z_{ply1w2++w2} & Z_{ply1w2++sly1w1} & Z_{ply1w2++sly1w2} \\
Z_{sly1w1++ply1w1} & Z_{sly1w1++ply1w2} & Z_{sly1w1++w1} & Z_{sly1w1++w2} \\
Z_{sly1w2++ply1w1} & Z_{sly1w2++ply1w2} & Z_{sly1w2++w1} & Z_{sly1w2++w2}
\end{pmatrix}.
\]

Calculation of the \( Z_{ij} \) matrix is a significant undertaking for multi-layer winding structures. The track height of the primary and secondary are represented by \( 1 \times n \) matrices, where \( n = N_p + N_s \).

\[
h_i \simeq h_j = \begin{pmatrix} h_1 & \ldots & h_n \end{pmatrix}.
\]

The inner radii \( a_1, r_1 \) and outer radii \( a_2, r_2 \) are also represented by \( 1 \times n \) matrices, where \( n = N_p + N_s \).

\[
a_1 = r_1 = \begin{pmatrix} r_1 & \ldots & r_n \end{pmatrix}.
\]

All other variables are scalars.

4.4 Experimental Verification

The PCB board in Figure 4.4 featuring various winding structures was constructed and measured using an RLC meter to verify the algorithm’s accuracy.

Figure 4.4: Test inductance board
Table 4.3: Transformer parameters

<table>
<thead>
<tr>
<th>Transformer</th>
<th>$z$ (mm)</th>
<th>$N_p$</th>
<th>$N_s$</th>
<th>$n_t$</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>10</td>
<td>20</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>T2</td>
<td>10</td>
<td>24</td>
<td>24</td>
<td>1</td>
</tr>
<tr>
<td>T3</td>
<td>1.49</td>
<td>10</td>
<td>10</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 4.4: Inductance measurements

<table>
<thead>
<tr>
<th>Variable</th>
<th>Trans 1</th>
<th>Trans 2</th>
<th>Trans 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calc. $L_p(\mu H)$</td>
<td>7.92</td>
<td>11.93</td>
<td>1.85</td>
</tr>
<tr>
<td>Meas. $L_p(\mu H)$</td>
<td>7.94</td>
<td>11.99</td>
<td>1.70</td>
</tr>
<tr>
<td>Calc. $L_m(\mu H)$</td>
<td>1.30</td>
<td>2.33</td>
<td>1.20</td>
</tr>
<tr>
<td>Meas. $L_m(\mu H)$</td>
<td>1.28</td>
<td>2.47</td>
<td>1.25</td>
</tr>
<tr>
<td>Trans.</td>
<td>Rin (mm)</td>
<td>Np/Ns</td>
<td>Lp/Ls (µH)</td>
</tr>
<tr>
<td>-------</td>
<td>---------</td>
<td>-------</td>
<td>------------</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>1</td>
<td>0.02441</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>2</td>
<td>0.09016</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>3</td>
<td>0.18798</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>4</td>
<td>0.31947</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>5</td>
<td>0.48511</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>6</td>
<td>0.69423</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>7</td>
<td>0.91552</td>
</tr>
<tr>
<td>8</td>
<td>5</td>
<td>8</td>
<td>1.19180</td>
</tr>
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<td>9</td>
<td>5</td>
<td>9</td>
<td>1.50197</td>
</tr>
<tr>
<td>10</td>
<td>5</td>
<td>10</td>
<td>1.85252</td>
</tr>
<tr>
<td>11</td>
<td>5</td>
<td>11</td>
<td>2.24452</td>
</tr>
<tr>
<td>12</td>
<td>5</td>
<td>12</td>
<td>2.67558</td>
</tr>
<tr>
<td>13</td>
<td>5</td>
<td>13</td>
<td>3.15995</td>
</tr>
<tr>
<td>14</td>
<td>5</td>
<td>14</td>
<td>3.68653</td>
</tr>
<tr>
<td>15</td>
<td>5</td>
<td>15</td>
<td>4.26173</td>
</tr>
<tr>
<td>16</td>
<td>5</td>
<td>16</td>
<td>4.88729</td>
</tr>
<tr>
<td>17</td>
<td>5</td>
<td>17</td>
<td>5.56453</td>
</tr>
<tr>
<td>18</td>
<td>5</td>
<td>18</td>
<td>6.23676</td>
</tr>
<tr>
<td>19</td>
<td>5</td>
<td>19</td>
<td>7.08272</td>
</tr>
<tr>
<td>20</td>
<td>5</td>
<td>20</td>
<td>7.92683</td>
</tr>
</tbody>
</table>

Figure 4.5: Example Algorithm Printout
4.5 Summary

In this chapter a method for calculating the inductance of a planar transformer was presented. An algorithm built on method and its structure was developed and the successful implementation shown.
Chapter 5

Characterizing $dV/dt$ Performance

5.1 The Capacitive Current Path

Providing a high dialectic strength galvanic isolation does not guarantee a drive system will perform well at the rated isolation voltage. Another important consideration is the capacitive current path. There is always capacitive coupling across any form of galvanic isolation, and this capacitance provides a path for ground loop currents in floating ground systems. In high voltage and high frequency systems where the rate of change of the voltage between the floating ground and the system ground can be very large, these currents can become a major concern.

The ground plane can be modeled as a network of inductors with a values in $nH/mm$. This is shown in Figure 5.1.

During the high-side switching transient the ground loop equivalent circuit looks like Figure 5.2 [10]. Current flows in the path shown until the series combination of capacitors in the loop are charged to the bus voltage. The voltage will be split across the transformer isolation capacitor $C_{is}$ and the two capacitors $C_{gnd}$. The $C_{gnd}$ capacitors represent the control isolation from earth and the bus ground isolation from earth. The model is simplified showing two signal gates. In a real driver circuit this combination of gate input/output can be repeated many times along a signal path, and therefore each of their performances must be considered. The signal gates may also be on the high or low side, and several other factors effect the current flowing through each section of the ground path.

5.2 Simulation

A MATLAB PLECS simulation was built upon the model in Figure 5.2. During each iteration of the simulation the peak voltage across the signal capacitor $C_{sig}$ was measured. The simulation is shown in Figure 5.4.
Figure 5.1: Example distributed ground plane circuit

Figure 5.2: Equivalent single path capacitive circuit as $dV/dt$ begins
5.2.1 Circuit Operation

The chronological events of the voltage transient are detailed below:

1. The ground voltage first begins to rise, and current begins to flow in the ground loop. This change in current causes a voltage drop across the parasitic ground inductance between the two signal gates.

2. The voltage drop across the ground inductance causes current to flow counter-clockwise into signal input capacitor $C_{\text{sig}}$. The signal capacitor voltage is altered, potentially
Table 5.1: Default parameters

<table>
<thead>
<tr>
<th>Description</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver isolation capacitance</td>
<td>$C_{is}$</td>
<td>5 pF</td>
</tr>
<tr>
<td>Control/Bus isolation capacitance</td>
<td>$C_{gnd}$</td>
<td>100 pF</td>
</tr>
<tr>
<td>Signal gate input capacitance</td>
<td>$C_{sig}$</td>
<td>20 pF</td>
</tr>
<tr>
<td>Parasitic ground inductance connecting signal gates</td>
<td>$L_{gnd}$</td>
<td>4 nH</td>
</tr>
<tr>
<td>Parasitic signal path inductance</td>
<td>$L_{sig}$</td>
<td>9 nH</td>
</tr>
<tr>
<td>Signal gate output impedance</td>
<td>$R_{sig}$</td>
<td>100 Ω</td>
</tr>
<tr>
<td>Power device voltage rise/fall time</td>
<td>$dV/dt$</td>
<td>6000V/µs</td>
</tr>
</tbody>
</table>

affecting the control signal.

3. The capacitive current reaches its steady state value during the voltage transient. The constant current causes the voltage drop across the ground inductance to be zero, and the voltage across $C_{sig}$ returns to its commanded value.

4. The voltage transient ends and the capacitive current becomes zero. This change in current causes a voltage drop across the ground inductance, which induces current flow clockwise into the signal input capacitor $C_{sig}$. The signal capacitor voltage is again altered, potentially affecting the control signal.

5.2.2 Results

Single Path Model

The simulations default parameters are shown in Table 5.1. During each series of iterations one parameter was varied and the rest were held at the default values.

In Figure 5.5 the signal disturbance is shown as a function of both the isolation capacitance $C_{is}$ and the ground path parasitic inductance $L_{gnd}$. The effect on signal voltages can be significant. When $C_{is}$ is increased the magnitude of the disturbance increases as a decaying polynomial approaching an asymptote set by the additional ground isolation $C_{gnd}$. This exemplifies how important it is to understand the isolation levels; if any, from controller and converter bus to earth. When $L_{gnd}$ is increased the magnitude of the disturbance increases pseudo-linearly, since the voltage drop across the inductance is

$$V_{L_{stray}} = L_{gnd} \frac{dI}{dt}.$$
In Figure 5.6 the signal disturbance is shown as a function of the signal gate input capacitance $C_{\text{sig}}$, and the signal gate output impedance $R_{\text{sig}}$. For both $C_{\text{sig}}$ and $R_{\text{sig}}$ increasing their value decreases output voltage disturbance exponentially like $e^{-x}$. Unfortunately, these parameters are strictly properties of the selected gate components. It can therefore be advantageous in floating drivers to use larger, slower components to reduce conductive EMI disturbances.

In Figure 5.7 the signal disturbance is shown as a function of the signal path parasitic inductance $L_{\text{sig}}$ and the voltage transient $dV/dt$ during switching. When $L_{\text{sig}}$ is increased the voltage disturbance decreases very slightly, because the parasitic inductance acts as an impedance to the charging or discharging of the signal capacitor $C_{\text{sig}}$. Increasing $L_{\text{sig}}$ is not advantageous as it increases propagation delay and distorts the output. Increasing $dV/dt$ increases the signal disturbance linearly, as one would expect since the steady state current during the $dV/dt$ transient is

$$I_{\text{cap}} = C_{\text{eq}} \frac{dV}{dt}.$$
Figure 5.7: Signal Disturbance vs. $L_{\text{sig}}$ (a) and $dV/dt$ (b)

Figure 5.8: Signal Disturbance vs. $dV/dt$ varying $C_{\text{is}}$

Figure 5.8 shows the signal disturbance as a function of $dV/dt$ for several values of $C_{\text{is}}$. As noted in Figure 5.5a, the disturbance voltage increases linearly with $dV/dt$. The slope of this increase varies with the isolation capacitance $C_{\text{is}}$. Figure 5.9 shows the slope $\frac{\text{Disturbance}}{dV/dt}$ as a function of isolation capacitance $C_{\text{is}}$. This slope increases as a decaying polynomial approaching an asymptote set by the additional ground isolation $C_{\text{gnd}}$, similar to Figure 5.5a.
Figure 5.9: Slope of Signal Disturbance vs. $dV/dt$ varying $C_{ts}$

Figure 5.10: Signal Disturbance vs. $dV/dt$ varying $L_{gnd}$

Figure 5.11: Slope of Signal Disturbance vs. $dV/dt$ varying $L_{gnd}$
Figure 5.10 shows the signal disturbance as a function of $dV/dt$ for several values of $L_{gnd}$. As noted in Figure 5.5b, the disturbance voltage increases linearly with $dV/dt$. The slope of this increase varies with the stray ground inductance $L_{gnd}$. Figure 5.11 shows the slope $\frac{\text{Disturbance}}{dV/dt}$ as a function of stray ground inductance $L_{gnd}$. This slope pseudo-linearly, similar to Figure 5.5b.

Distributed Model

Simulations were ran in the distributed model in Figure 5.1. The inductance nodes can be represented by a matrix $Node_{dist}$ and are arrayed visually in Figure 5.1 identically to the structure of $Node_{dist}$.

$$Node_{dist} = \begin{pmatrix} 1,1 & \ldots & 1,n \\ \vdots & \ddots & \vdots \\ m,1 & \ldots & m,n \end{pmatrix}.$$  

Two circuits were used, in the first the isolation is located in the center of the board as per the design outlined in Chapter 6. In the second an optocoupler was used for signal isolation, and the ground-path is through a floating power supply not located in the signal path. These two circuits are shown in Figure 5.12 and Figure 5.13 respectively.

![Figure 5.12: Model from design presented in Chapter 6](image-url)
The shortest path to ground is shown in red and the isolation capacitance is circled in blue. The node distribution is shown in Figure 5.14.

Figure 5.13: Model with external isolated supply

Figure 5.14: Nodes in the distributed model
Table 5.2: Distributed model parameters

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{is}$</td>
<td>13 pF</td>
</tr>
<tr>
<td>$L_{m,n}$</td>
<td>5 nH</td>
</tr>
<tr>
<td>$R_{sig}$</td>
<td>100 Ω</td>
</tr>
<tr>
<td>$C_{sig}$</td>
<td>20 pF</td>
</tr>
<tr>
<td>$L_{sig}$</td>
<td>9 nH</td>
</tr>
<tr>
<td>$dV/dt$</td>
<td>6000 V/μs</td>
</tr>
</tbody>
</table>

In the following plots the input is considered to be the input of Gate 2 and the output is considered to be the output of Gate 1 from Figure 5.2. The same RLC path is used to show signal noise as in Figure 5.2. The model parameters are shown in Table 5.2. the distance between each node is considered to be 1cm, and the inductance per unit length of 5 nH/cm is a conservative application of the value given in [8].

![Signal Distortion](image)

Figure 5.15: Disturbance (V) vs. Time (s) for output at 4,6 and input at 4,10

In Figure 5.15, Figure 5.16 and Figure 5.17 the circuit of Figure 5.12 is used. In Figure 5.15 the components are directly in the shortest ground path and therefore the signal disturbance is greatest. In Figure 5.16 and Figure 5.17 the components are not in the shortest ground path and therefore the signal disturbance is better than in Figure 5.15. Because these nodes
represent physical dimensions on the board you can conclude that proximity to the shortest ground path affects the magnitude of signal disturbance. This implies that careful location of the shortest path to ground is important in high ground \(dV/dt\) systems.
Figure 5.18: Disturbance ($V$) vs. Time ($s$) for output at 4,6 and input at 4,10

Figure 5.19: Disturbance ($V$) vs. Time ($s$) for output at 4,6 and input at 8,6
In Figure 5.18, Figure 5.19 and Figure 5.20 the circuit of Figure 5.13 is used. The conclusions are similar to the those stated previously. The primary difference is that in this topology the low-side logic is largely unaffected by the $dV/dt$ induced ground currents, because there is virtually no path to ground through the low-side logic. In this topology it is still very important to place the shortest ground path away from sensitive components.

5.3 Minimizing Conductive EMI

These results illustrate several ways to realistically minimize the signal disturbance across an arbitrary signal capacitor $C_{\text{sig}}$:

1. Decrease $C_{ls}$
2. Decrease $I_{\text{gnd}}$
3. Decrease $C_{\text{gnd}}$
4. Increase $C_{\text{sig}}$
5. Increase $R_{\text{sig}}$
6. Minimize $I_{L\text{gnd}}$ between components

These can be realized by following several recommendations. They are ranked by order of impact.
1. $C_{is}$ can be minimized by maximizing the driver transformer’s isolation distance and minimizing its parallel surface area.

2. $L_{gnd}$ can be minimized by using large ground planes between components and placing the components as close together as possible.

3. $I_{Lgnd}$ can be minimized between components by placing them away from the lowest impedance ground path, or strategically placing the shortest ground path away from components.

4. $C_{gnd}$ can be reduced by having additional series isolation in the full ground loop.

5. $C_{sig}$ and $R_{sig}$ can be reduced by carefully selecting gates and amplifiers for the intended application. Applications with large $dV/dt$ transients should use high output impedance devices with larger input capacitances. This comes at the cost of propagation delay.

### 5.4 Validation

To validate the effect of $dV/dt$ change a high frequency pulse generator was used to induce $dV/dt$ on the prototype board in Figure 5.22. The primary capacitive current path is shown in red. The devices between which $dV/dt$ noise is measured is shown in blue and orange, where the blue device is a driver-stage IC and has input capacitance of 10$\mu$F and the orange device is a D flip-flop and has output impedance of 100$\Omega$. The equivalent circuit discussed earlier in this chapter is shown in white to illustrate its application to this test. Two similar waveforms of varying maximum $dV/dt$ were applied and the voltage across the input capacitance of driver-stage IC was measured. The measurements were taken on a 100MHz Tektronix Oscilloscope. The test setup is shown in Figure 5.21.
Figure 5.21: $dV/dt$ noise setup

Figure 5.22: Board used to test $dV/dt$ noise

Figure 5.23 shows the voltage waveforms that were applied across the board ground planes and Figure 5.24 shows the resultant $dV/dt$. For test waveform one the maximum $dV/dt$ value is 7500 V/µs and for test waveform two the maximum $dV/dt$ value is 13,000 V/µs.
In Figure 5.25 and Figure 5.26 the second derivative of the ground waveform was obtained by applying interpolation and smoothing functions in Mathematica prior to taking the second derivative. The resultant waveforms are good enough for qualitative understanding but not for precise quantitative analysis. A higher resolution Oscilloscope may yield cleaner waveforms.
The noise voltage on the plots in this section are multiplied by 10 for clearer comparison on the plots.

![Figure 5.25: Test waveform one](image)

Considering again the equivalent circuit of Figure 5.2, the highest impedance in the ground loop is the isolation capacitance \( C_{is} \). This capacitance limits the ground current and therefore the noise. Capacitive current from basic circuit theory is

\[
I_{gnd} = C_{is} \frac{dV}{dt}.
\]  

(5.1)

This alone does not explain the induced noise. The voltage across a stray inductance interconnecting two devices is

\[
V_{Lgnd} = L_{gnd} \frac{dI_{gnd}}{dt}.
\]  

(5.2)

Taking the derivative of Eq. 5.1 and plugging it into Eq. 5.2 yields

\[
V_{Lgnd} = L_{gnd} C_{is} \frac{d^2V}{dt^2}.
\]  

(5.3)

At this instantaneous point in time the voltage across the signal capacitor \( C_{\text{sig}} \) can be modeled as a simple series \( R - C \) circuit where the applied voltage is \( V_{Lgnd} \). This can be seen

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in Figure 5.25 and Figure 5.26, where the ground voltage derivative waveform leads the signal voltage.

![Test waveform two](image)

Figure 5.26: Test waveform two

The relationship between the ground plane voltage and the induced noise voltage can also be seen by looking at the waveforms in Figure 5.27. When the slope of the ground voltage is constant, the capacitor will be discharging and the noise voltage will be approaching the x-axis. When the slope of the ground voltage is increasing the noise voltage will have a positive slope and when the slope of the ground voltage is decreasing the noise voltage will have a negative slope.

5.5 Summary

In this chapter the noise induced by ground plane $dV/dt$ was examined. Two models were presented to study the effect of the driver design on the noise immunity. Several recommendations were made to limit $dV/dt$ noise on isolated drivers and experiments were conducted to verify that the problem exists.
Figure 5.27: Noise voltage and test waveform 2
Chapter 6

Demonstration Driver System

The culmination of the previous 5 chapters is a demonstration driver utilizing a coreless PCB transformer for signal and power isolation. The driver features high voltage isolation, low isolation coupling capacitance, and standard protection features.

6.1 Driver System

6.1.1 Low side logic

The driver system has 2 signal inputs and two power inputs. The signal inputs are the commanded drive signal and the on-state of a complimentary device. If there is no complimentary device then this input can be tied to ground or left floating.

![Image of the logic subsystem]

Figure 6.1: The logic subsystem
In Figure 6.1 the schematic for the logic subsystem is shown. When switch 2 is in the on-state, the PWM for switch 1 will not pass through $AND_1$, and the output of $AND_1$ will be low to prevent bus shoot-through. This low signal will be inverted and modulated into a 4MHz signal at the output of $AND_{off}$. When switch 2 is in the off-state the PWM for switch 1 will pass through $AND_1$ and modulated into an 8MHz signal at the output of $AND_{on}$. In summary, a 4MHz signal is sent to the isolation subsystem if switch 1 is commanded off and an 8MHz signal is sent to the isolation subsystem if switch 1 is commanded on.

6.1.2 Isolation

High voltage isolation is achieved through a coreless planar PCB transformer as described in Chapters 3 and 4. The signal from the low-side logic is buffered in an H-bridge comprised of two separate driver ICs and sent across the transformer to the high-side. Both drivers are capable of 9A output, both power device drive signal and high-side power are sent across the same transformer.

![Figure 6.2: The isolation subsystem](image)

6.1.3 High-side rectifier

The high-side rectifier subsystem extracts power from the isolation transformer and extracts the high frequency command signals. The rectifier circuit is shown in Figure 6.3 and consists of two opposite polarity voltage doublers, and two resonant capacitors. The resonant capacitors lower the resonant frequency of the transformer to increase the voltage gain of the transformer as explained in Chapter 3. Two linear regulators are used to provide stabilized +5V and +15V
to the high-side components.

The signal is extracted from the junction of the anode of diode $D_3$ and the cathode of diode $D_1$. The signal floats $V_{c_1}$ plus $V_{c_2}$ plus a diode drop above high-side ground.

### 6.1.4 Demodulation

The demodulation circuit consists of a signal level-shift, voltage reference, comparator, buffer, delay element, D flip flop and a reset circuit.
If the commanded signal is greater than the combined avalanche voltage of $D_{z1}$ and the forward drop of $D_{2}$ a signal of magnitude greater than $V_{dz3}$ will enter the comparator at the positive input. The comparator will output high because

$$V_{on} - V_{fd2} - V_{dz1} > V_{dz3}.$$  

The signal passes through a buffer and enters the clock input of the D flip flop. The same signal passes through a delay element into the D input of the D flip flop. The delay is set between the half periods of the 8MHz and 4MHz signal. The half periods for these signals are

$$T_{8MHz} = \frac{0.5}{8MHz} = 62.5\, ns$$  \hspace{1cm} (6.1)  

$$T_{4MHz} = \frac{0.5}{4MHz} = 125\, ns.$$  \hspace{1cm} (6.2)  

Setting the time delay between these two values ensures that while the 8MHz signal is propagating the flip flop will always output high, and while the 4MHz signal is propagating the flip flop will always output low. This demodulates the high frequency carrier into the original signal. The flip flop also has a CLR input, which must be high for the IC to output high. A simple capacitor circuit charges a capacitor at the input of the CLR to 5V as long as a signal,
4MHz or 8MHz is propagating. This ensures that the flip flop will not continue to output high if there is a failure elsewhere on the circuit.

6.1.5 Driver

The driver is a Texas Instruments IC that contains a hybrid BJT MOSFET output shown in Figure 2.7. In addition to the driver IC, a blanking circuit is included to prevent the driver IC from converting incorrect drive signals into actual IGBT switching during the high-side voltage rise time.

![Figure 6.5: The driver stage](image)

In the circuit of Figure 6.5 the blanking circuit sinks any drive signal from the demodulation stage until a set time has passed, determined by the values of $R_{c1}$ and $C_1$. At this time the voltage across $C_1$ causes the NMOS to turn on, which applies a positive voltage to the gate of the PMOS and opens the circuit path that is sinking the signal current.
6.1.6 Resistor network

The driver IC is connected to a resistor network that limits the gate current during both turn-on and turn-off. The on resistance is the series combination

\[ R_{on} = R_1 + R_2 + R_3 + R_4. \]

The turn off resistance is the parallel combination of \( R_{on} \) and \( R_{off} \) after considering the diode drop.

\[ R_{off} = R_5 + R_6 + R_7 + R_8. \]

There is also a resistor attached from gate to emitter to ensure device turn-off in the case of a driver failure.

![Diagram of the turn-on/off resistor network](image)

Figure 6.6: The turn-on/off resistor network

6.1.7 Device state

The power device state is measured utilizing a combination of two techniques. The first method involves forcing a current across the IGBT collector to emitter during its on-state, the second is by measuring the gate emitter voltage \( V_{ge} \).
As shown in Figure 6.7, if either the gate voltage is above threshold or there is a voltage drop across $R_1$ due to the device being on, the state will output as on.

### 6.1.8 Feedback modulation

The state signal is then modulated in the same manner as Figure 6.1.

![Figure 6.7: Measuring device state](image)

![Figure 6.8: Modulating device state signal](image)
6.1.9 State demodulation

The signal is demodulated using the same circuit as in Figure 6.4. Because there is no power or voltage gain required on low-side, there is no need for a voltage doubler or supply capacitance.

![Diagram of the demodulation circuit](image)

**Figure 6.9: Rectifying state signal**

The simple circuit in Figure 6.9 is used to rectify the signal. This signal is used as the input in a complimentary bridge driver to prevent shoot-through.

6.2 Transformer

A significant advantage of this topology is the elimination of the need for an isolated DC-DC converter. The same transformer that carries the drive signal pulse carries power from the low-side to the high-side; however, the power transfer is open-loop and the output voltage is dependant on the load. High-side linear regulators mitigate this effect, but induce additional losses.

6.2.1 Principles

Power transfer across the isolation transformer is a function of the load, desired output voltage, and frequency. It can be widely variable based on the operating conditions of the coreless transformer. The transformer used in the this driver design is shown.

6.2.2 Transformer Performance

Transformer performance can be characterized in two ways, efficiency and voltage gain. Both of these are variable with both frequency and load, and therefore ideal operation requires a careful balance between the two.
Table 6.2: Implemented transformer design parameters

<table>
<thead>
<tr>
<th>$z$ (mm)</th>
<th>$N_p$</th>
<th>$N_s$</th>
<th>$n_l$</th>
<th>$w_{p/s}$</th>
<th>$h_{\mu m}$</th>
<th>$d_p$ (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.494</td>
<td>15</td>
<td>15</td>
<td>1</td>
<td>0.254</td>
<td>35</td>
<td>0.2</td>
</tr>
</tbody>
</table>

Table 6.3: Implemented resultant transformer parameters

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calc. $L_p(\mu H)$</td>
<td>4.32</td>
</tr>
<tr>
<td>Meas. $L_p(\mu H)$</td>
<td>4.11</td>
</tr>
<tr>
<td>Calc. $L_m(\mu H)$</td>
<td>3.14</td>
</tr>
<tr>
<td>Meas. $L_m(\mu H)$</td>
<td>3.11</td>
</tr>
<tr>
<td>Calc. $L_{lk}(\mu H)$</td>
<td>1.17</td>
</tr>
<tr>
<td>Meas. $L_{lk}(\mu H)$</td>
<td>1.00</td>
</tr>
<tr>
<td>Meas. $R_p(\Omega@1MHz)$</td>
<td>6.00</td>
</tr>
<tr>
<td>Calc. $C_{is}(pF)$</td>
<td>5.27</td>
</tr>
<tr>
<td>Meas $C_{is}(pF)$</td>
<td>6.00</td>
</tr>
</tbody>
</table>
To determine the operating range of the transformer the voltage gain must be considered for the average power load. If the high-side supply is regulated by a linear-regulator or a DC-DC converter the average output power should be constant at a given switching frequency. Using this power an equivalent steady-state resistance can be calculated to model voltage gain and efficiency of the transformer using Eq. 3.2 and Eq. 3.6.

Figure 6.10: Transformer voltage gain vs. frequency in MHz

Figure 6.11: Transformer voltage gain vs. load
Using the data in Figure 6.10, Figure 6.11 and Figure 6.12 the appropriate operating point for the designed transformer can be selected.

6.3 Simulation

The primary drive system including signal modulation and signal quality was simulated in MATLAB Simulink PLECS.

6.3.1 Model

The power and signal simulation circuits are the same as those shown earlier in this Chapter, with two exceptions.
Figure 6.13: Simulation PWM generator and signal modulation model

The modulation block diagram in Figure 6.13 was built using MATLAB Simulink. If the drive signal is high the modulation block outputs an 8MHZ signal; if the drive signal is low the modulation block outputs a 4Mhz signal.
The demodulation block in Figure 6.14 includes a comparator to level-shift the input signal and a 'sample and hold' block from Simulink as the D flip flop.

### 6.3.2 Simulation Results

The modulated signal on the high-side in Figure 6.15 floats above ground by half the supply voltage minus a diode drop.
The high-side supply and gate voltage are shown in Figure 6.18. The instantaneous power is provided by the supply capacitance and the voltage ripple correlates with the charging of the gate capacitance.
6.4 Prototype

The prototype board described in this section was built around the design constructed earlier in this chapter.

Board Design

The driver was designed on a 4-layer PCB where the high and low side are placed so that the capacitive coupling between the two ground planes is very low. This is shown in Figure 6.19.

![Transformer primary side](image)
![Transformer secondary side](image)
![High-side](image)
![Low-side](image)

Figure 6.19: Board cross-section

The first version of the board used vias to connect both sides of the transformer to the low and high-side, but this lowered the isolation rating due to surface arcing. This board is shown in Figure 6.20.
The use of non-buried vias limits the isolation capability of the board to 7kV, where arcing between the via and the transformer trace occurred. Future designs should include buried vias for inter-layer connections. Another alternative is to connect the inside of the transformer to the H-bridge by using a pad and external wire.

6.5 Results

Three elements of driver operation were tested to confirm the claims of this design.

1. Efficiency
2. Isolation
3. Power and signal transfer

6.5.1 Efficiency

For the efficiency tests a function generator applied a sinusoidal voltage to the transformer primary, and a resistive load and resonant capacitor were paralleled across the transformer secondary. The RMS voltage and current were measured on both sides and the average power calculated.
6.5.2 Isolation

For the isolation test a 30kV supply was used to provide pulses to the transformer primary referenced to the transformer secondary. The low-side ground plane was tied to the transformer primary and the high-side ground plane was tied to the transformer secondary.
When vias were used in testing surface arcing occurred at 4kV in one transformer design and 7kV in another.

### 6.5.3 Power and Signal

Finally, high-side power and signal transfer was demonstrated. A 10kHz drive signal was successfully modulated on the low side, transferred to the high-side through the designed planar transformer, and demodulated using the scheme shown in this chapter. The modulated waveforms were generated using on-board oscillators and amplified across the transformer using two Texas Instruments driver ICs acting as an H-bridge.
The test setup is shown in Figure 6.24. A function generator was used to generate the desired 10KHz drive signal.

![Figure 6.25: Low and high-side signals](image)

Figure 6.25: Low and high-side signals

Figure 6.25a is the H-bridge input signal and the resulting signal on the high-side is shown in Figure 6.25b. The high-side signal floats above ground by roughly half the high-side bus voltage as designed and has to be level shifted for demodulation. The AC transformer waveform is shown in Figure 6.26a and the resultant high-side bus voltage is shown in Figure 6.26b.

![Figure 6.26: Low-side transformer voltage and high-side bus voltage](image)

Figure 6.26: Low-side transformer voltage and high-side bus voltage
The d flip flop inputs for both off and on are shown in Figure 6.27a and Figure 6.27b respectively. The flip flop output or demodulated drive signal is shown in Figure 6.28. Noise on the demodulated signal comes from stray inductances and can be reduced by locating the flip flop closer to the comparator. It could also be reduced by using a larger device; the flip flop in this design was contained in an SC70 package and therefore had a very small input capacitance making it more vulnerable to noise.
6.5.4 Takeaways

Experimental validation of the driver in this Chapter illustrated considerations that must be taken during implementation.

1. The reverse bias capacitance for rectifier diodes must be taken into careful consideration when setting the resonant point of the transformer.

2. The average load point of the transformer should be set above the equivalent gate charge load to ensure a consistent demodulation of the high frequency signal. The load can be set by using a zener diode to latch the high-side voltage and therefore the load point.

3. Buried vias or surface pads should be used to connect the inner portion of the primary and secondary side transformer to the H-bridge. When vias are used the voltage isolation level is no longer a function of the dielectric strength of FR4 but instead the dielectric strength of air.
Chapter 7

Conclusion and Future Work

7.1 Conclusion

Due to the accelerating global adoption of renewable energy sources power electronic converters are being driven into higher voltage ranges. Key to the continued success of this effort is the ability to safely and reliably drive high-voltage semiconductor devices. A sustained effort is required to develop drivers that can operate in these high-voltage applications. In this thesis a driver topology using high frequency coreless PCB transformers was proposed. Advantages of this design can include:

1. Low profile
2. Flexible switching commutation
3. High voltage isolation
4. Low coupling capacitance

Also in this thesis an algorithm for calculating inductances of planar transformer structures was demonstrated. This method for determining inductances is a key ingredient for successful implementation of these winding structures in driver systems.

Finally, a model to explain $dV/dt$ induced noise for high-side drivers was shown and investigated. The model expanded upon previous work and recommendations were developed for reducing $dV/dt$ induced noise based on the work done.

In all three of these parts both simulations and experiments were done to verify the concepts introduced. The results show that this topology and these systems are feasible for use on future and present high-voltage converters.
7.2 Future work

In addition to the work accomplished, several improvements and advances can be made.

1. Optimize transformer parameters by balancing operating frequency, voltage gain and efficiency.

2. Introduce over-current protection utilizing the miller effect. This can be accomplished by tracking gate charge as power device current increases.

3. Implement the proposed drive system on a high voltage converter.

4. Condense the proposed drive system into an SOC, or system on chip.
REFERENCES


