ABSTRACT

XIAOPENG, WANG. Power Efficiency Conscious Design and Implementation of High Frequency Integrated Synchronous Buck DC-DC Converters for Portable Electronics Applications. (Under the direction of Dr. Alex. Q. Huang.)

This dissertation focuses on the efficiency analysis, efficiency conscious design, and silicon implementation of integrated synchronous Buck DC-DC converters (ISBC) with switching frequencies equal to or larger than 4MHz. Using switching frequencies in this range makes the ISBC compact enough to satisfy the component size specifications required by modern portable electronic devices such as smartphones, laptops, tablet computers, and personal satellite navigation systems.

The dissertation first details the development of a general switching loss analysis method for the ISBC. State-of-art switching loss analysis methods are based on two assumptions about MOSFET parasitic capacitance parameters. These assumptions are not true for implementations of ISBCs that have inactive power FET sub-cells due to the application of the power stage width segmentation technique. The power stage width segmentation method dynamically adjusts the number of power FET subcells with respect to the magnitude of the load current. This dissertation emphasizes loss analysis inside the chip from the viewpoint of an IC design engineer, breaks down the components of the power FET channel current for each switching event, and completely defines the physical difference between the charging/discharging loss and overlap loss. The dissertation evaluates the charging/discharging loss by individually calculating each parasitic capacitor's energy variation for each switching event, and by classifying the ratio of loss relative to the energy variation in different charging/discharging circuit loops. The dissertation also develops equations to predict the onset of the Miller plateau and calculate the overlap loss. The research explains why in some applications there is no Miller plateau during the PFET turn-off event. With the aid of the aforementioned concepts and analysis, load efficiency curves with respect to different numbers of active power FET cells can be calculated for the first time, as can the optimal number of active

subcells for a specified load current. The predicted results correctly explain the characteristics of efficiency improvement via segmentation.

The second part of the dissertation focuses on the implementation and its control algorithm used for automatic segmentation in a 4MHz ISBC. State-of-art automatic segmentation techniques use a current sensor to adjust the number of active power FET subcells, causing the obtained efficiency will deviate from the designed value because of MOSFET Rdson variations in a practical environment. The implementation of an on-chip current sensor is another challenge in >4MHz ISBCs. Moreover, decreasing the silicon area and current consumption of the high resolution A/D converter, the smooth transfer between pulse width modulation (PWM)/pulse frequency modulation (PFM), and the safe operation of the segmented power stage during load transients all are practical issues that are under-addressed by state-of-art designs. The dissertation proposes a Vsw pinning automatic segmentation technique (VswPS). VswPS maintains the time sampled value of Vsw (the phase node voltage of the ISBC) in a voltage band for all load conditions by turning on or off a given number of power FET subcells. It is concluded from the viewpoint of the algorithm that VswPS not only ensures optimal segmentation but also automatically accounts for Rdson variations. From the viewpoint of implementation, as there is no need for a current sensor or an A/D converter, the challenges of circuit design are significantly reduced, and the segmentation technique can be applied to a >4MHz ISBC. VswPS also efficiently supports the automatic mode shift between PWM and PFM. The silicon circuit schematic and layout of the ISBC with VswPS are introduced in the dissertation and the performance of the ISBC is verified by simulation.

The third part of the dissertation uses a fanout-of-4 metric (FO4) to analyze the semiconductor process (SP) dependent maximum switching frequency (MSF) of a digital pulse-width modulator (DPWM). State-of-art DPWM architectures and various improvement measures upon them are discussed and compared. After revealing the choke effect in the self-oscillating hybrid DPWM (SOH) and its impact on MSF, the dissertation shows that separating the voltage controlled oscillator (VCO) and delay_mux line is an effective way to relax the choke effect so that MSF can be nearly doubled while achieving 40% power savings. Taking the low cost AMI06 SP and a 9-bit resolution specification as an example, the dissertation uses the developed equations to conclude

that an 8MHz switching frequency may be achievable with the proposed Choke-Relaxed self-oscillating hybrid architecture (RSOH), which is a value that has never been approached before by other researchers using similar semiconductor technology. The RSOH chip was designed and fabricated on a 0.703mm^2 die via the MOSIS educational program. Chip test results demonstrate that the MSF is 7.4MHz with 1.07mA power consumption and the adjustable switching frequency range is from 1.8MHz to 7.4MHz.

Power Efficiency Conscious Design and Implementation of High Frequency Integrated Synchronous Buck DC-DC Converters for Portable Electronics Applications

by
Xiaopeng Wang

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APPROVED BY:

_____	_____
Dr. Paul D. Franzon	Dr. W. Rhett Davis
_____	_____
Dr. Srdjan Lukic	Dr. Alex. Q. Huang Chair of Advisory Committee

DEDICATION

To my wife,

Li Yang

my son,

Chengzhi Wang

And my parents,

Jingkai Wang and Lichun Yang

BIOGRAPHY

The author, Xiaopeng Wang, was born in Guizhou, China, in 1972. He received a B.S. in Mechanical Engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1993 and a M.S in Electrical Engineering from China Aerospace Science and Industry Corporation (CASIC), Tsunyi, China, in 1996. From 1993-1995, he studied in the Department of Electrical Engineering at the National University of Defense Technology, Changsha, China. From 2002-2006, he studied in the Department of Electrical Engineering at Shanghai Jiao Tong University, Shanghai, China. From 2006 to present, the author works towards a Ph.D degree as a research assistant in the Power Management Microsystem Group in the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh, NC. His research interests include the analog and mixed signal IC design for power management applications, digital power conversion and advanced integrated power conversion systems.

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Chapter 1

Introduction

The dissertation's focus is the power efficiency analysis and improvement of the high frequency (in the range of several megahertz) integrated DC-DC synchronous Buck converters (ISBC), which are widely utilized as power supply modules for portable digital devices, such as global positioning system (GPS) receivers, laptop computers, personal digital assistants (PDA) and smart phones.

1.1 Background

Portable digital devices have many performance expectations to the ISBC [1-1] [1-2] [1-3] [1-4] [1-5] [1-6] and the most important four of them are respectively,

1) Power supply quality

An ISBC with the performance as close as an ideal voltage source is expected by advanced digital devices. In state-of-art electronics market, an example expectation for the ISBC is that the worst case voltage perturbation should be less than 50mV when the load current varies [1-5] in the full range.

2) Component size

ISBC has the highest power conversion efficiency (>80%) among several DC step-down power supply solutions [1-6] [1-7]. However, ISBCs requires a discrete power inductor and capacitor which will to some extent sacrifice the power density of portable

devices. Increasing the switching frequency of ISBC to several megahertz is the solution adopted by recent commercial ISBC designs [1-26] [1-27] [1-28] [1-29] [1-30] [1-31] to minimize the size of these discrete components.

3) Wide range load current and dominant time for light load condition

More and more functional blocks are being integrated into portable devices so that the customers is able to use the portable devices for various kinds of activities, such as browsing websites, communication, watching movies, playing games and operating office software. The current demands of these functional blocks are significantly different, so the ISBC load current is supposed to vary in a wide range. At the same time, though how long each functional block will be in the work mode heavily depends on the customer's personal interest, a popular fact is that during most of its operation time the portable devices will operate in light load (<0.1A) or deep light load condition (<0.01A).

4) Power conversion efficiency

Both switching frequency and load current influence ISBC power conversion efficiency.

Switching frequency is determined from the consideration of power supply quality and component size. In theory, the higher the switching frequency is, the higher the bandwidth of ISBC regulator can be designed to be and the smaller the power component is. However, parasitic components in MOSFET and its package impede the trend towards high switching frequency in the respect of power efficiency and switching noise.

When the switching frequency is determined, the width of power FET in the ISBC will be optimized to achieve peak power conversion efficiency in a specified load current condition. Consequently, in other load conditions, the efficiency will be to some extent lower and the extent will become more significant when the switching frequency approaches several megahertz or higher. Figure 1-1 illustrates the efficiency of a 4MHz

ISBC in a wide range of load current. The power FET width of the ISBC is optimized at 1A load current. The efficiency will achieve a peak value of 91.51% at the optimized load condition but drop to 21.54% when the load current is 0.02A.

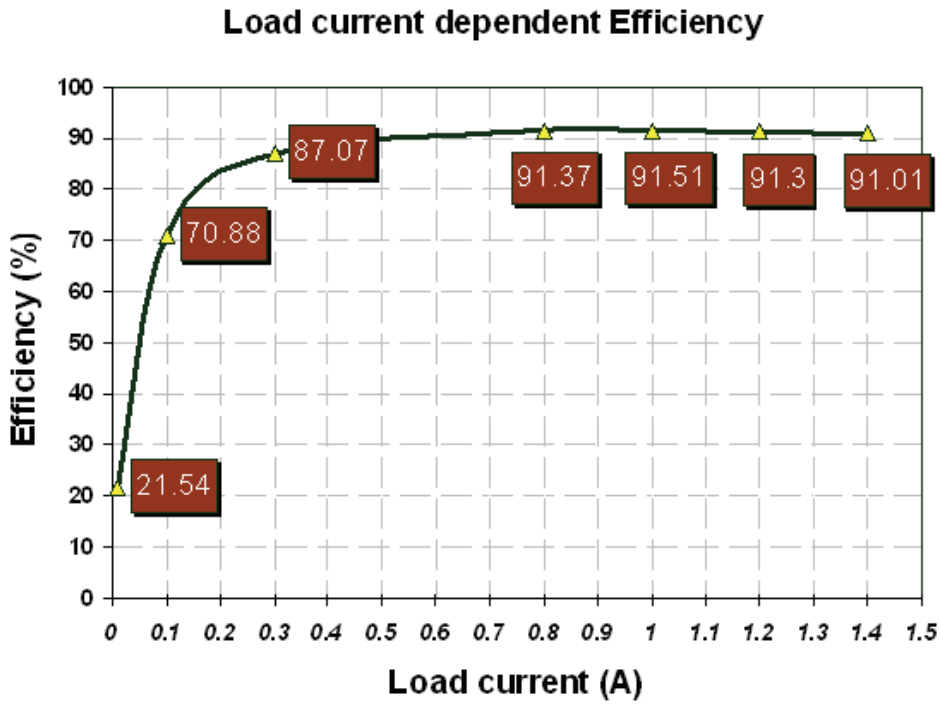

Figure 1-1. Power efficiency curve in wide range load current

The above four important expectations of the ISBC conclude that the development trend of portable devices will require a high switching frequency ISBC and the efficiency of the ISBC is required to have high power conversion efficiency in a wide load range. An ideal solution is a constant efficiency value or a flat efficiency curve independent of load current. ***The desire towards the ideal solution motivates the research in the dissertatio***n, which includes developing a switching loss analysis method so that it is possible to explain how well some nowadays technologies can improve the efficiency; proposing a better solution in both the temperature compensation and the silicon implementation; and modifying the state-of-art architecture of some component to doubly increase its capacity for high switching frequency implementation without sacrifice of power loss.

1.2 ISBC operation and power efficiency

1.2.1 CCM mode and PWM modulation

There are many commercial ISBC products on the market [1-26] [1-27] [1-28] [1-29] [1-30] [1-31]. The basic ISBC schematic is illustrated in Figure 1-2. The battery is the power source and a functional chip in the portable device is the power load. The function of the ISBC is to realize step-down DC voltage level conversion, that is, change the battery's DC voltage level V_{in} to a lower DC voltage level V_o specified by the function chip in the portable device. The ISBC adopts high frequency switching mode energy transfer to achieve larger than 80% power conversion efficiency. The operational principle of the ISBC is firstly using two power MOSFET switches to periodically chop the power source voltage so that the voltage at the phase node denoted by V_{SW} is a pulse type square signal with an expected duty cycle, then using a power filter composing of a power inductor and capacitor to obtain a DC output voltage for the functional chip in the portable device.

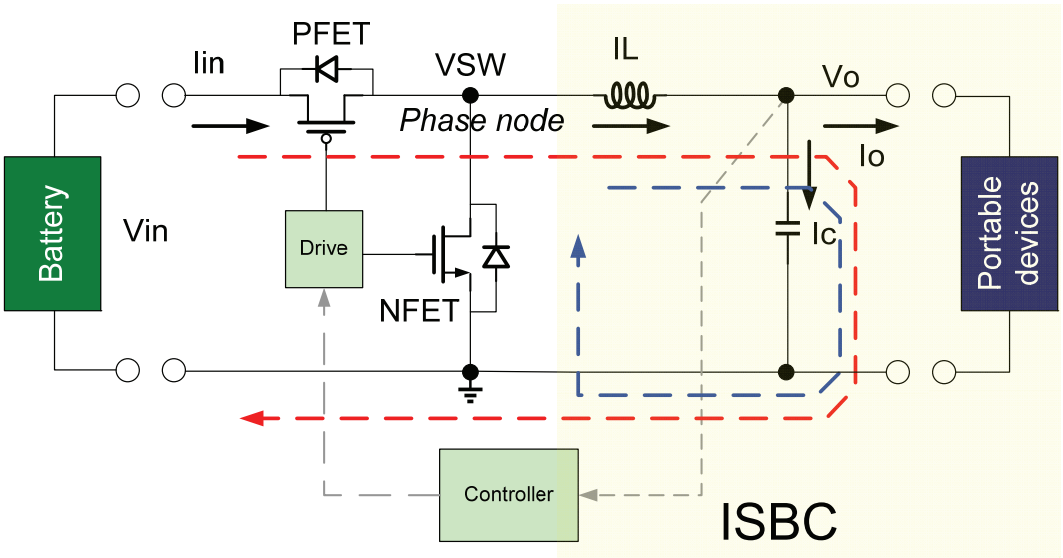

Figure 1-2 Basic schematic and operation of the ISBC

The output DC voltage level of the ISBC is tightly regulated with the aid of feedback control. The controller in Figure 1-2 compares the output voltage of ISBC with a reference voltage which represents the expected output voltage of the ISBC and utilizes control algorithm to generate a periodic square wave signal with adjustable pulse width at the input of the driver. This kind of output voltage regulation implementation is called pulse width modulation (PWM). The driver will sufficiently strengthen the driving capacity of the periodical square wave so that it is strong enough for turning on and off two big power MOSFETs. For the ISBC fabricated in standard CMOS technology, two power MOSFETs include a PFET as the control (top) power FET and a NFET as the synchronous (bottom) power FET.

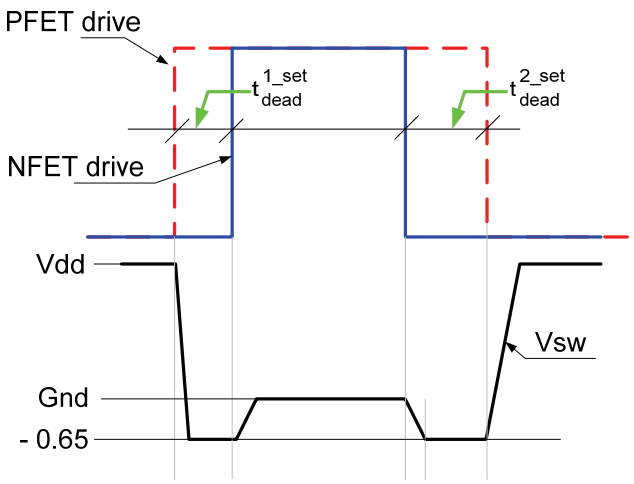

Figure 1-3. Synchronous driver signal and dead-time setting

Figure 1-3 illustrates the turn on sequence of the two power FETs and an ideal voltage waveform V_{SW} at the phase node of the ISBC due to the switching. As illustrated in Figure 1-3, the two power FETs are alternately turned on so that in theory there is no direct shoot through route between the power source and the ground in the ISBC. Furthermore, on consideration of the existence of parasitic component, two dead-time

intervals $t_{dead}^{1\_set}$ and $t_{dead}^{2\_set}$ are artificially inserted in the time sequence of the driver signal to avoid parasitic induced direct shoot through in a practical product.

When the control power FET and the synchronous FET are driven in the above alternating way, the ISBC is called to work in a continuous conduction mode (CCM). The simulation waveforms of the ISBC working in the CCM are illustrated in the subsection 4.3.2.

When the control FET turns on, the input voltage will appear at the phase node. As the input voltage is higher than the output voltage, the power inductor and capacitor will be charged and store energy. When the control FET turns off, the electrical connection between the battery and the load device is cut off and the output energy is maintained by the discharge of the power inductor and capacitor. If the synchronous FET is not immediately turned on after the control FET turning off because of the deadtime or vice versa, the synchronous FET's body diode will help transfer the current discharged by the power inductor with a forward voltage drop as 0.6-0.7V. As the output voltage V_o is only around 1V in nowadays low power portable devices, the body diode conduction implies significant power loss. The body diode conduction will be eliminated when the deadtime passes and the synchronous FET is completely turned on.

Because the energy transfer in the ISBC is completed by the inductor and capacitor, the power efficiency of the ISBC is usually much larger than 80%. However, the continuous charging and discharging process of the inductor and capacitor determine that the inductor current is a triangle wave type signal and the output voltage is a quadratic curve type signal [1-7] as illustrated in the subsection 4.3.2. The averaging value of the inductor current equals the load current and the averaging value of the output voltage equals the voltage reference. Also, in order to ensure ISBC's output voltage ripple being an acceptable value for portable devices (an example is <5mV), switching frequency of the ISBC, power inductance and capacitance should be systematically designed with high enough values.

1.2.2 DCM mode and PFM modulation in light load

In subsection 1.2.1, the CCM operation of ISBC is introduced. However, the ISBC does not always work in the CCM and sometimes it will prefer to work in a discontinuous conduction mode (DCM) so as to improve power conversion efficiency when the load current is very small (light or deep light load condition).

Because of the existence of the inductor current ripple, the valley value of inductor current in CCM might be negative when the load current is very small. The negative inductor current implies over-charging/discharging of the inductor and a deficient efficiency. DCM is generated with the aid of an inductor current sensor or directly comparing the phase node voltage V_{SW} with the ground as V_{SW} will change from a negative voltage to a positive one when the inductor current goes from positive to negative. When the inductor current zero crossing happens, the synchronous NFET will be turned off to terminate the further discharge of inductor current and the inductor current is maintained at zero until the next period of charging process begins. The ISBC in DCM is typical of the periodic inductor current waveform illustrated in the subsection 4.3.2. Also, the critical load current between CCM and DCM is usually selected as a value a little higher than half of the inductor current peak-to-peak ripple.

The avoidance of the over-charging/discharging of the inductor significantly benefits the power efficiency, as the switching frequency of the ISBC in DCM will be roughly linear proportional to the load current to ensure that the averaging inductor current equals the load current. The equation is derived in the subsection 4.3.2.

As the switching frequency is load dependent and the inductor current is no longer a simple triangle wave, the transfer function of the ISBC in DCM operation is much different from that of the ISBC in CCM. Furthermore, a linear controller developed on small signal modeling theory might not work correctly for the ISBC in DCM operation, when the switching frequency keeps decreasing to become close or even smaller than the corner frequency of the power filter. On the basis of the above consideration, a popular

implementation is to develop two kinds of controller for the ISBC in wide range of load current. The first one is the PWM linear regulator introduced in subsection 1.2.1 for the normal load condition, and the second on is a pulse frequency modulation (PFM) nonlinear controller for the light load condition. In the PFM regulation, various kinds of output voltage ripple hysteresis controller [1-8] are applied and the switching frequency is modulated according to the load current. The PFM regulation method in this dissertation is constant on-time control in which the turn on time of the control FET is set to be a constant value [1-8]. It should be mentioned that PFM regulation is not a good choice for the normal or heavy load condition, as the switching frequency might become very high and finally lose control in the situation [1-8] [1-9] [1-10] [1-11] [1-12].

1.2.3 Loss breakdown in high frequency ISBC

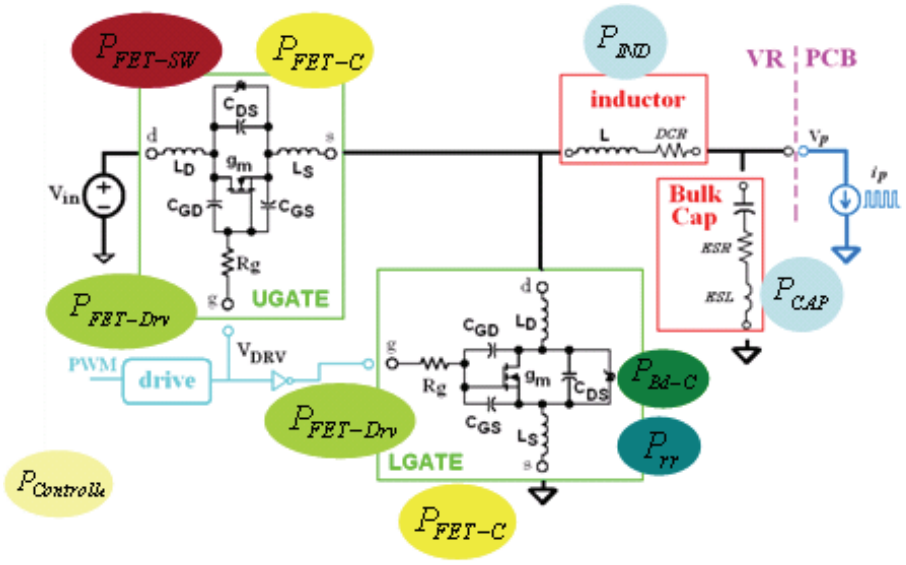

Figure 1-4. Losses generated in the ISBC

The energy conversion efficiency of ISBC will be 100% if all components are ideal ones. However, there is no ideal component in the world. The parasitic capacitance of the

power MOSFET will generate charging/discharging loss and the Rdson of the power MOSFET in the linear region will generate conduction loss. Besides, as the power MOSFET is loaded by a power inductor, the power FET will temporally work in the saturation region during the switching transient. Thus, overlap loss as the times of Vds and Ids in the short period will exist in the ISBC.

Figure 1-4 illustrates the possible sources of power losses in the ISBC. P_{FET-C} refers to the conduction loss of the power FET which is generated by the rdson of the power MOSFET working in the linear region. P_{FET-SW} indicates the switching losses of the power FET including the charging/ discharging loss of its parasitic capacitance and the overlap loss generated during the swithcing. $P_{FET-Drv}$ refers to the charging and discharging losses in the power FET driver. P_{IND} is related to the direct current resistance (DCR) of the power inductor and P_{CAP} indicates the losses generated by equivalent series resistance (ESR) of power capacitor. P_{Bd-C} refers to the NFET body diode conduction loss during the dead-time and P_{rr} accounts for body diode's reverse recovery energy loss.

Among the aforementioned losses, the conduction loss, the switching loss and the driver loss are dominant and directly related to the width of the power MOSFET. Furthermore, the switching losses and the driver loss are positively linear proportional to the power MOSFET width; while the conduction loss is inversely proportional to the width. Thus, there is a power loss tradeoff process when we determine the width of the power FET and the process is called power FET sizing. The optimal efficiency will be achieved when a power FET width makes the switching and driving loss exactly 50% to 50% balanced with the conduction loss. The power FET sizing is usually carried out at a normal load condition so that the power efficiency of the ISBC will be the highest when the load current equals its normal value

The aforementioned losses have various kinds of relationships against load current. The conduction loss is positively related to the load current in a quadratic law, the overlap loss is related to the load current in a roughly positive linear relationship, and the

charging/discharging loss is independent of the load current. As a result, when ISBC works at a load current in different from the normal one, either the conduction loss or the switching and driver loss will be larger than the other and the efficiency drops down because of the broken balance. For example, when the load becomes heavier, the conduction loss will be dominant. On the contrary, when the load current is lighter, the switching and driver loss becomes dominant.

One 4 MHz ISBC is utilized as an example to visualize the aforementioned efficiency character, in which Vin=3.6V and Vout=1.2V. The ISBC's power FET is optimized at the maximum load current 1.4A. Figure 1-5, Figure 1-6 and Figure 1-7 respectively show the power loss breakdown of the ISBC when load current is 1.4A, 1A and 0.1A and the ratio of the switching loss over conduction loss. From Figure 1-5, we observe that the ratio of switching loss to conduction loss is 39:42 in the load current for efficiency optimization. When the load current is decreased to 1A, the ratio becomes 52:35. If we further decrease the load current to 0.1A, the dynamic loss is significantly larger than the conduction loss with a ratio 92:2 illustrated in Figure 1-7.

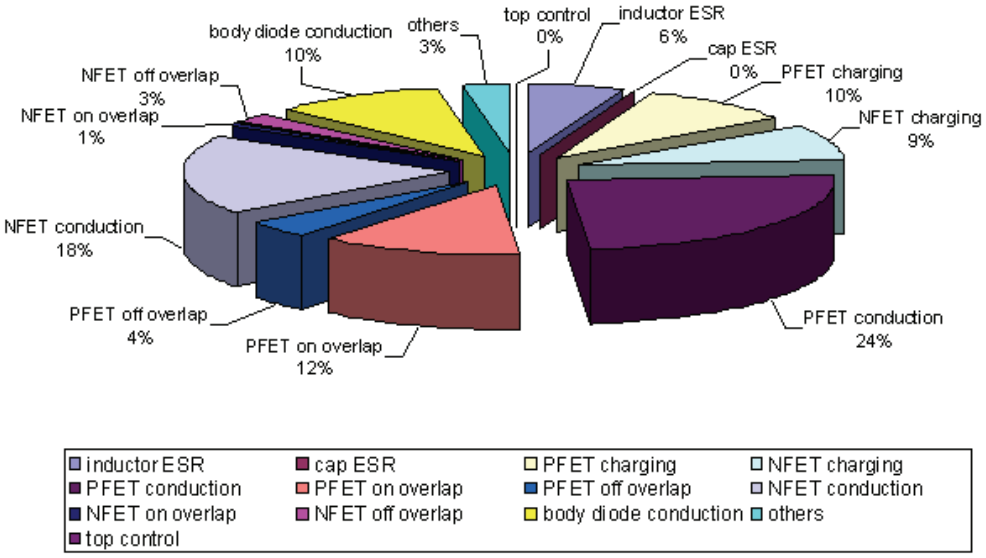

Figure 1-5. Power loss breakdown in the maximum load current with optimal efficiency (1.4A)

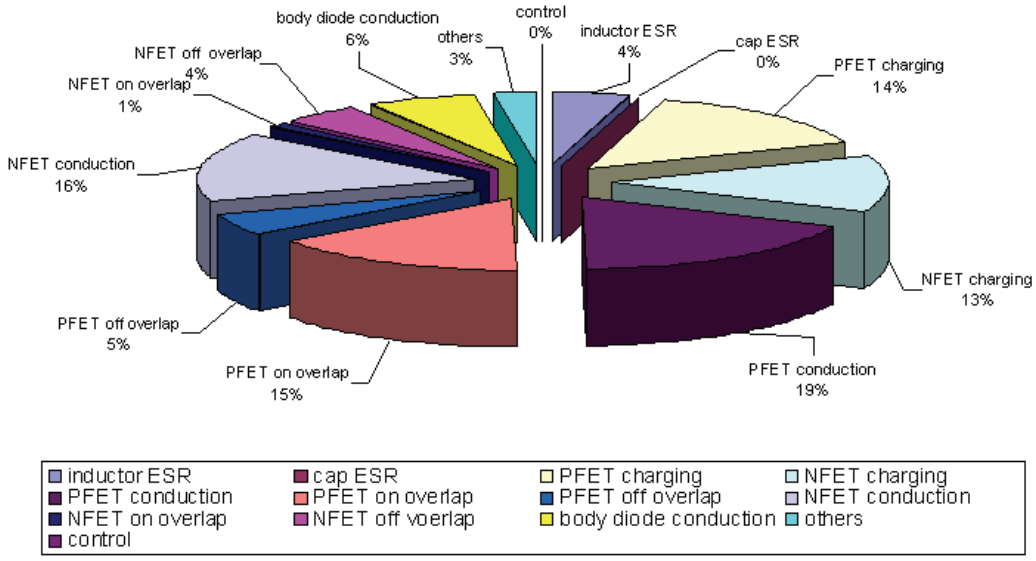

Figure 1-6. Power loss breakdown in a slightly lighter load current (1A)

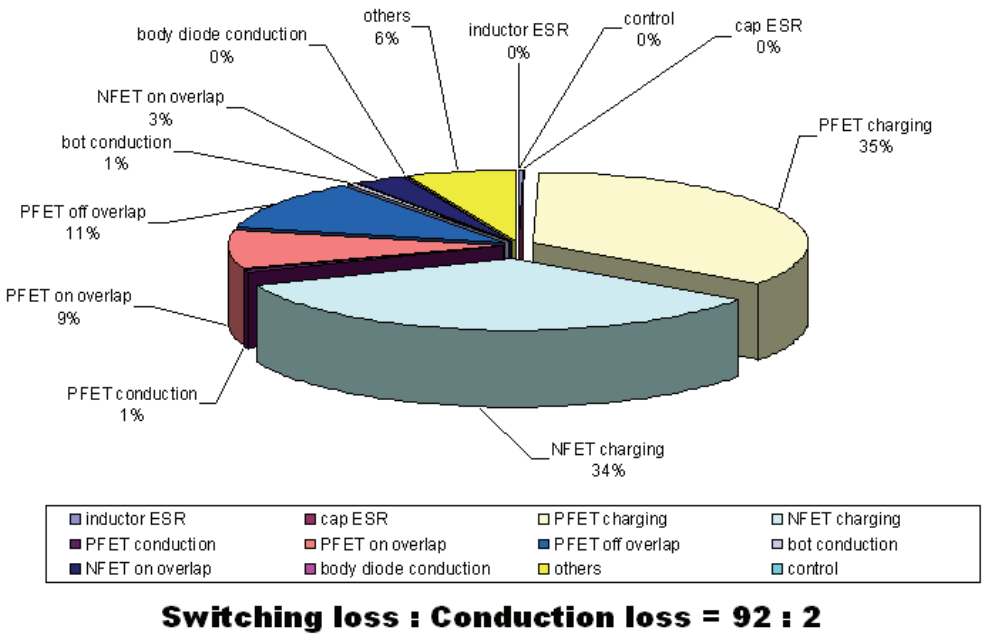

Figure 1-7. Power loss breakdown in a deep light load current (0.1A)

1.2.4 Power efficiency improvement techniques

There are many techniques to improve the efficiency of the ISBC working in a wide range of load current and the subsection will introduce several major circuit design related techniques.

1.2.4.1 Dynamic gate voltage

Increasing the gate voltage can decrease the rdson of the power MOSFET so as to decrease the conduction loss. However, the practice will at the same time increase the switching and driver loss. On the other hand, decreasing the gate voltage will increase the conduction loss but decrease the switching and driver loss. Thus, if the gate voltage were able to be dynamically adjusted with the load current, the balance between the switching and the conduction loss might be improved to some extent. Texas instruments applied the technique in a commercial product [1-13] and the reported maximum efficiency difference between two different gate voltages ($V_{GS} = 9V$ and $V_{GS} = 5V$) is 4% at 20A load current and 8% at 2A load current.

The dynamic gate voltage technique requires extra circuits for example charge pumps or DC/DC boost converters to supply multiple levels of driver vdd DC voltages higher than Vin.

1.2.4.2 Gate swing control

The gate swing control technique [1-14] proposed by Stanford University is another way to adjust the balance of losses via changing the gate voltage. In different from the multiple levels of driver vdd in the dynamic gate voltage technique, the driver vdd is constant in the gate swing control technique. However, the NMOS and PMOS at the final stage of the driver are separately driven so that a voltage controlled RC delay circuit can adjust the swing of the driver's output voltage. For example, the power PFET's driver

voltage does not swing between zero and driver vdd, while swing between some voltage level and driver vdd.

With the technique, 2% efficiency improvement was reported in the light load condition when the load current is 0.03A and 7% efficiency improvement was reported in the deep light load condition when the load current is 0.01A [1-14].

1.2.4.3 PFM modulation

PFM mode is an imperative choice when the ISBC works in a deep light load condition. However, PFM mode is not a good choice when the ISBC works in the normal load condition as discussed in subsection 1.2.2.

1.2.4.4 Power width segmentation

Power width segmentation technique means that the number of active power FET subcells in the ISBC is controllable and is regulated when the load current changes [1-15] [1-16] [1-17] [1-18] [1-19]. Figure 1-8 illustrate the layout of the ISBC power FET subcells with the segmentation technique. The power width segmentation technique can increase the power efficiency by 3%-8%. From the load efficiency curve reported in [1-15], the maximum efficiency improvement was 8% at the critical load current before the ISBC entered into PFM mode operation.

In the dissertation, the total number of ISBC power FET subcells is determined from the optimal efficiency in the heaviest load condition and part of the power FET subcells will be gradually turned off when load current decreases.

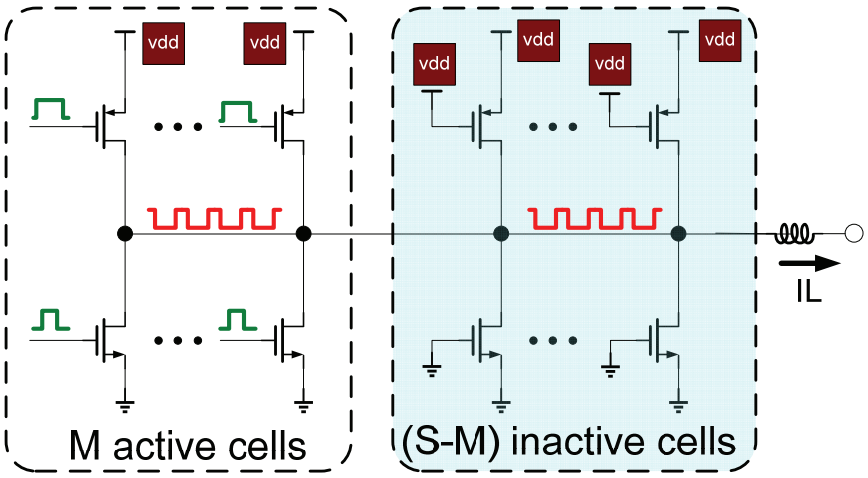

Figure 1-8. Power FET subcells with segmentation technique

1.2.4.5 Dithering skip modulation

The dithering skip modulation [1-20] technique changes the modulation of the ISBC so that digital signal processing technique can be utilized to equivalently decrease the switching frequency in a sequence of many switching cycles so that power efficiency is improved. The technique had issues on the output voltage regulation and small signal modeling. There is still a long way to go for applying digital signal processing to control or modulate the ISBC - a high frequency real time system.

The reported maximum efficiency improvement [1-20] is 8%, when both the dithering skip modulation and the dead-time adjustment technique are adopted.

1.2.4.6 Dead-time adjustment

As introduced in subsection 1.2.1, the insertion of $t_{dead}^{1\_set}$ and $t_{dead}^{2\_set}$ between PFET and NFET driver signal are imperative to avoid the parasitic induced shoot through in the ISBC. If the shoot through happens because of too small values of deadtime, efficiency will be hugely degraded and the safe operation of the ISBC is also in doubt. On the other hand, the existence of deadtime indicates that ISBC will have certain time of body diode

conduction and the larger deadtime implies larger period of body diode conduction. For low voltage ISBC applications such as portable applications, the body diode conduction degrades the efficiency significantly too. Thus, in order to obtain an optimal efficiency, we need to select the minimum values of $t_{dead}^{1\_set}$ and $t_{dead}^{2\_set}$ which is large enough to avoid the parasitic induced shoot through.

The issue is that the switching transient depends on the load current, so the minimal required values of $t_{dead}^{1\_set}$ and $t_{dead}^{2\_set}$ are load current dependent too. The dependence will be details analyzed in Chapter 2 and the conclusion there is that the required deadtime will be increased when the load current is decreased. Thus, if we select the values of $t_{dead}^{1\_set}$ and $t_{dead}^{2\_set}$ to satisfy the minimum deadtime requirement in the light load condition, in the heavy load condition the selected values are too conservative and a long period of body diode conduction will be generated.

On the basis of the discussion, if we can adjust the values of $t_{dead}^{1\_set}$ and $t_{dead}^{2\_set}$ in different load condition, the load efficiency will be obviously improved. Many industrial practices verified the analysis [1-20] [1-21] [1-22] [1-23] [1-24].

The implementation of dead-time adjustment is easy in theory but severely difficult in practice. As the value of deadtime is usually several nanoseconds, if the deadtime is aggressively adjusted, the existence of uncertain factors including switching noise, temperature variation, technology corner and packaging might make the parasitic induced shoot through happen in the ISBC and hereby the damage of the ISBC chip.

Some authors also discussed the impact of dead-time on stability [1-25].

1.3 Dissertation outline

Among those efficiency improvement approaches introduced in subsection 1.2, the power width segmentation and the PFM operation will be selected in the dissertation for a 4MHz ISBC for portable applications. The dissertation includes three research topics to improve the selected technologies. As there is no method available now to analyze how well the efficiency can be improved by power width segmentation technique, the first topic is to develop a general power efficiency analysis which can be used for the ISBC with the power width segmentation technique. The second topic is to overcome several implementation issues existing in the state-of-art automatic segmentation technique and effectively integrate the segmentation technique and the PFM technique in one chip. The dissertation also has a topic about the digital version of the ISBC, which will make efforts on how to improve the maximum switching frequency of a digital ISBC.

In the Chapter 2, an event based switching loss analysis method will be introduced. The method will physically separate the charging/discharging loss and the overlap loss. Two criteria for Miller plateau in PFET switching will be developed. A hypothesis about parasitic capacitor energy variation will be proposed and its verification will be implemented with 12 different fabrication processes, working conditions, or design corners. Charging/discharging losses for all switching events will be classified for each parasitic capacitor so that the losses can be calculated with the capacitor energy variation. Equations for dead-time setting and gate driver optimization will also be developed in the Chapter 2.

One 4MHz ISBC design for a portable application is detailed in Chapter 3. PID control will be selected for realizing output voltage regulation in CCM operation. With the aid of the switching losses equations, the power FET width will be optimized. Furthermore, the efficiency improvement due to segmentation will be theoretically calculated and compared with simulation data.

Chapter 4 will focus on the design and silicon implementation of automatic segmentation in an ISBC. With the developed switching loss analysis equations in Chapter 2, the optimal number of active power FET cells in a specified condition will be derived. The challenges of the state-of-art segmentation implementation will be discussed and a novel segmentation technique will be proposed to overcome the challenges. All power FET cells will be managed with state machine. Moreover, some specific techniques to ensure the safe operation of automatic segmentation during load transient and the smooth mode shift between PWM and PFM will be developed.

Chapter 5 will be involved in the analysis and design of a digital pulse width modulator (DPWM). The chapter discusses why DPWM determines the maximum switching frequency (MSF) of a digital ISBC. Fan-out-of-4 (FO4) metric will be utilized to predict the MSF of different state-of-art DPWM architectures in a specified semiconductor technology. Also, different approaches to improve the MSF will be discussed. Furthermore, the MSF limitation of self-oscillation hybrid DPWM architecture (SOH) will be investigated, which is the most popular architecture in current practice. A novel architecture will be proposed to doubly improve the MSF in SOH through architecture modification without sacrifice of silicon area and power.

Chapter 6 will summarize the contributions of the dissertation in respect to the aforementioned three research topics.

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Chapter 2

Switching events based switching loss analysis

In this chapter, the switching losses of ISBC will be reconsidered and systematically investigated on the basis of switching events. Many concepts will be further clarified or developed for the first time including breakdown the transient current, the Miller plateau, capacitor energy variation during a switching event, parasitic capacitance extraction, driver optimization, dead-time setting and optimal segmentation curve. To make the analysis directly applicable for ISBCs with a segmentation function, the existence of inactive power MOSFET cells will be considered in this chapter.

2.1 Introduction

MOSFET are not an ideal component. The MOSFET parasitic capacitors illustrated in Figure 2-1 set a limit on the switching speed and create associated charging and discharging losses.

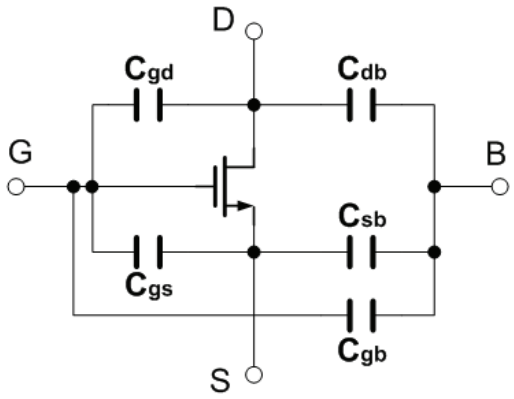


Figure 2-1. Parasitic capacitors in a MOSFET in standard CMOS technology

For the case of ISBCs in standard CMOS technology, C_{gs} , C_{gd} and C_{ds} are of particular interest. The values of C_{gd} and C_{gs} heavily depend on the operation region of the power MOSFET. In this dissertation, when MOSFET works in the cut-off region as illustrated in Figure 2-2, C_{gs} and C_{gd} are respectively represented with unit width capacitance $C_{gs}^{(C)}$ and $C_{gd}^{(C)}$. The values of $C_{gs}^{(C)}$ and $C_{gd}^{(C)}$ satisfy $C_{gs}^{(C)} = C_{gd}^{(C)} = C_{gdo} = C_{gso} = C_{ox} x_d$ in which C_{GDO} and C_{GSO} are unit width overlap oxide capacitance, C_{ox} is unit width oxide capacitance and x_d is called the lateral diffusion coefficient [2-1]. However, when the MOSFET works in the linear region as illustrated in Figure 2-3, C_{gs} and C_{gd} are respectively represented with unit width capacitance $C_{gs}^{(L)}$ and $C_{gd}^{(L)}$. As gate oxide capacitance should be included, the values of $C_{gs}^{(L)}$ and $C_{gd}^{(L)}$ become $C_{gs}^{(L)} = C_{gd}^{(L)} = C_{gdo} + 0.5 C_{ox} L_{eff}$ where L_{eff} is the effective gate length. When the MOSFET works in the saturation region as illustrated in Figure 2-4, C_{gs} and C_{gd} are respectively represented with unit width capacitance $C_{gs}^{(S)}$ and $C_{gd}^{(S)}$. The values of $C_{gs}^{(S)}$ and $C_{gd}^{(s)}$ change to be $C_{gs}^{(S)} = C_{gdo} + \frac{2}{3} C_{ox} L_{eff}$ and $C_{gs}^{(d)} = C_{gdo}$.

C_{db} is the junction capacitance and is a value determined by V_{ds} .

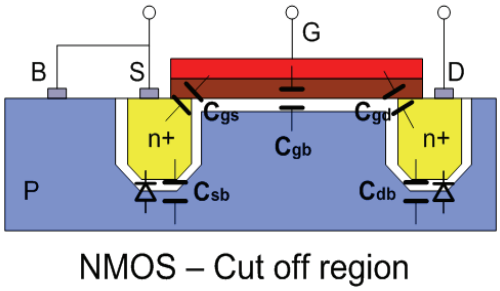


Figure 2-2. Cross section of NMOS working in the cut-off region

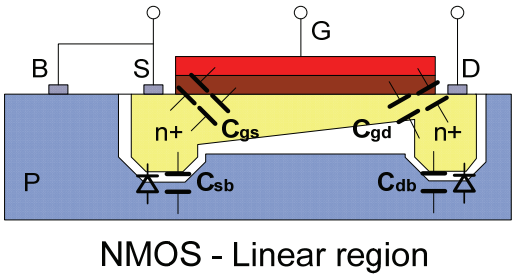


Figure 2-3. Cross section of NMOS working in the linear region

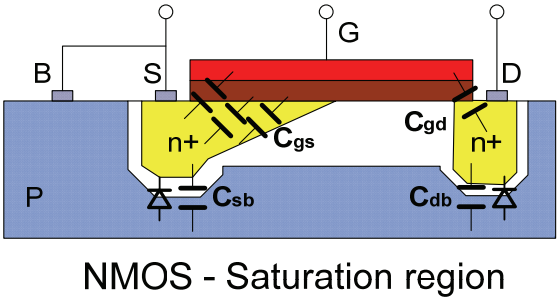


Figure 2-4. Cross section of NMOS working in the saturation region

Switching losses of the ISBC consist of overlap loss (O-loss), parasitic capacitors charging and discharging loss (C-loss) and gate driver dynamic loss (D-loss).

2.1.1 Present state of switching loss analysis

There are hundreds of papers and application notes that discuss switching loss analysis of discrete synchronous Buck converter (SBC) and the representative papers include [2-2] [2-3] [2-4] [2-5] [2-6] [2-7] [2-8] [2-9] [2-10] [2-11] [2-12] [2-13] [2-14] [2-15] [2-16]. There are also many papers focused on ISBCs [2-17] [2-18] [2-19] [2-20] [2-21] [2-22] [2-23] [2-24] [2-25].

All of these papers adopted a common approach to investigate the switching losses in a SBC or ISBC and their applications are limited by the characteristics of the approach.

The common approach for the switching loss analysis consists of two steps. Parameters of the power FET are measured via experiment or simulation in the first step. Time domain behaviors of the ISBC in a switching transient are analytically investigated and the switching loss is calculated using the measured power FET parameters in the second step.

The assumptions behind the approach include that all power FET subcells parasitic capacitors are assumed to be identical and the flowing directions of charging/discharging currents in all power FET subcells are the same.

2.1.1.1 Power FET parameters measurement

The values of gate charge Q_g, parasitic capacitance C_{gd}, C_{gs} and C_{db} are usually used to calculate the switching losses. However, the values of C_{gd}, C_{gs} and C_{db} cannot be directly measured via experiment and are in fact derived from three other measurable parameters including C_{iss}, C_{oss} and C_{rss} [2-26]. C_{iss} is defined as the input capacitance of the power FET and $C_{iss} = C_{gs} + C_{gd}$; C_{oss} is defined as the output capacitance and $C_{oss} = C_{gd} + C_{ds}$; C_{rss} is defined as the reverse transfer capacitance and $C_{rss} = C_{gd}$.

The parameters measurement schematic is illustrated in Figure 2-5 for an experimental measurement carried out on a discrete FET component and is illustrated in Figure 2-6 for a four-dimensional finite element analysis simulation measurement carried out on a power FET device model.

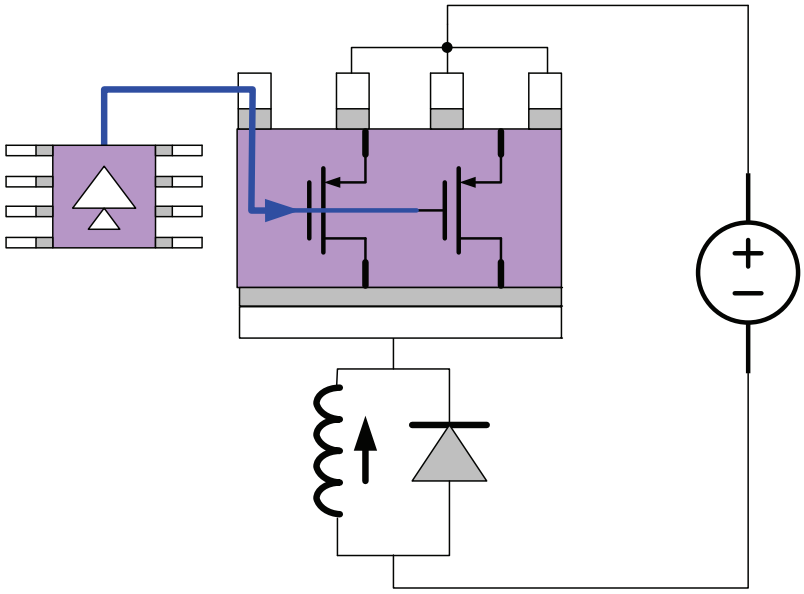


Figure 2-5. Experimental measurement with a discrete power FET component

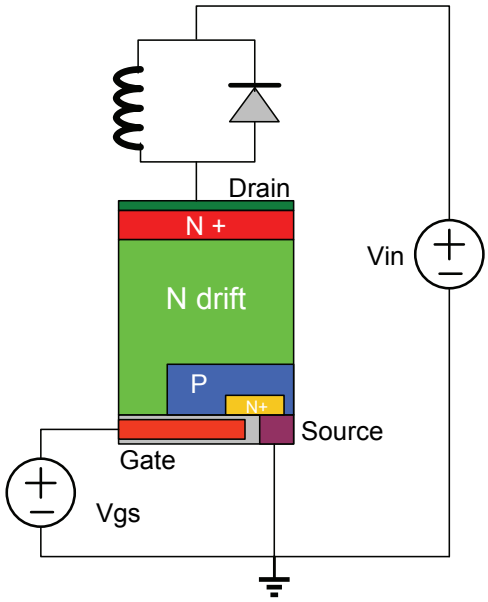


Figure 2-6. Simulation measurement with a power FET device model

2.1.1.2 Power FET time domain behavior based switching loss calculation

Switching waveforms of a practical ISBC product are complicated due to the existence of various kinds of parasitic components. In present, there are two typical ways to calculate the switching loss.

The first typical way [2-12] simplifies the waveforms as piecewise linear ones so that the switching loss calculation becomes straight. Figure 2-7 illustrates the waveforms which are simplified from the experimental observation and can concisely explain the time domain behavior of the power FET during switching transient.

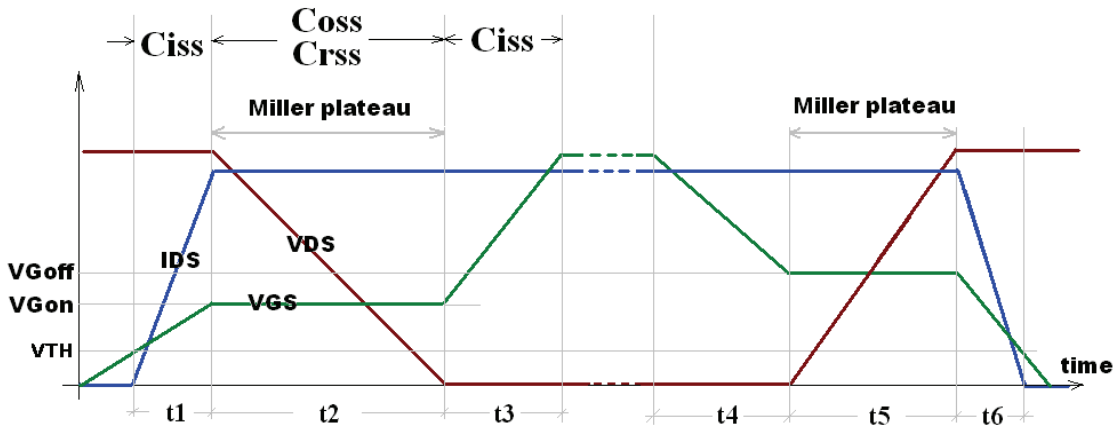


Figure 2-7. Piecewise linear waveforms of the power FET during switching

During the time interval t1, the power FET transits from cut-off region to the saturation region. The gate voltage of the power FET increases linearly until it reaches a Miller plateau voltage and the input capacitance C_{iss} is partially charged. The Ids current of the FET linearly increases too until it equals the total inductor current. During the time t2, the power FET transits from saturation region to linear region. The reverse transfer capacitance C_{rss} and the output capacitance C_{oss} are completely charged and the gate voltage remains constant as the Miller plateau voltage. The vds of the power FET linearly decreases until it equals the times of rdson and inductor current which approximately

approaches zero. During the time t3, the power FET works in linear region. The input capacitance C_{iss} charging continues until it is complete and the gate voltage equals vdd. Similar discharging process happens in the time periods t4, t5 and t6 when the power FET is turned off.

Figure 2-7 provides a straight way to calculate the switching loss. The values of t1, t2, and t3 can be calculated with the parameters in datasheet to conclude the switching loss during the power FET turn-on. So do the values of t4, t5, t6 and the switching loss during turn-off process.

The extent that the piecewise linear waveforms deviates from the practical ones has a positive relationship with the switching frequency. Figure 2-8 shows the turn-off waveforms of a ISBC operating with four megahertz switching frequency. In comparison with Figure 2-7, it is observed that the most obvious difference lies on the shape and magnitude of transient current. Thus, the first typical way is in fact a static analytical method to calculate the switching loss in empirically.

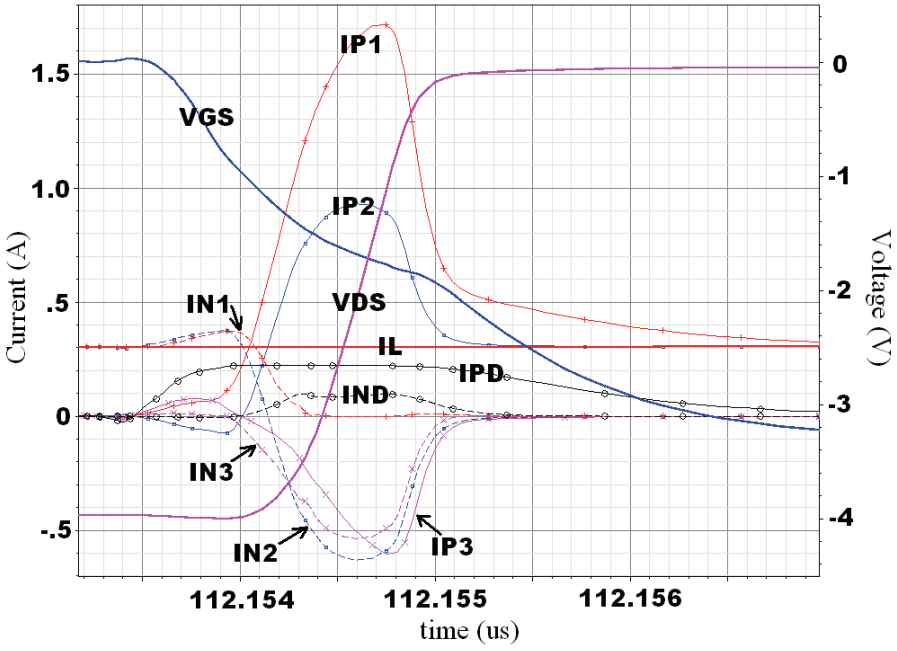


Figure 2-8. Switching waveforms of a 4MHz ISBC in transistor level simulation

Another typical way [2-3, 2-4] addresses the dynamic analysis of ISBC's switching behavior via building up the RLC equations of the ISBC during switching transient. The parameters C_{gd}, C_{gs} and C_{db} obtained from datasheet are used in the switching loss analysis. Also, the developed equations are expected to conclude time domain behaviors similar to the experimental switching waveforms.

2.1.1.3Assumptions violation

The present switching loss analysis methods have two assumptions. The first one is that all power FET subcells parasitic capacitors are assumed to be identical; the second one is that the flowing directions of charging/discharging currents in all power FET subcells are assumed to be the same.

The two assumptions are violated when the power width segmentation technique discussed in subsection 1.2.4.4 is adopted for the sake of light load efficiency.

Figure 2-9 shows an ISBC chip without the segmentation technique. The two power FET subcells are identical so the present switching loss analysis methods is applicable. Figure 2-10 shows an ISBC chip with the segmentation technique and the power FET subcell on the right hand is inactivated to save power in the light load condition. Thus, the difference between the ISBC in Figure 2-9 and Figure 2-10 lies on the power FET subcell on the right hand. For the convenient of explain, we name the power FET subcell on the right hand of Figure 2-9 and Figure 2-10 as ***topic cell***.

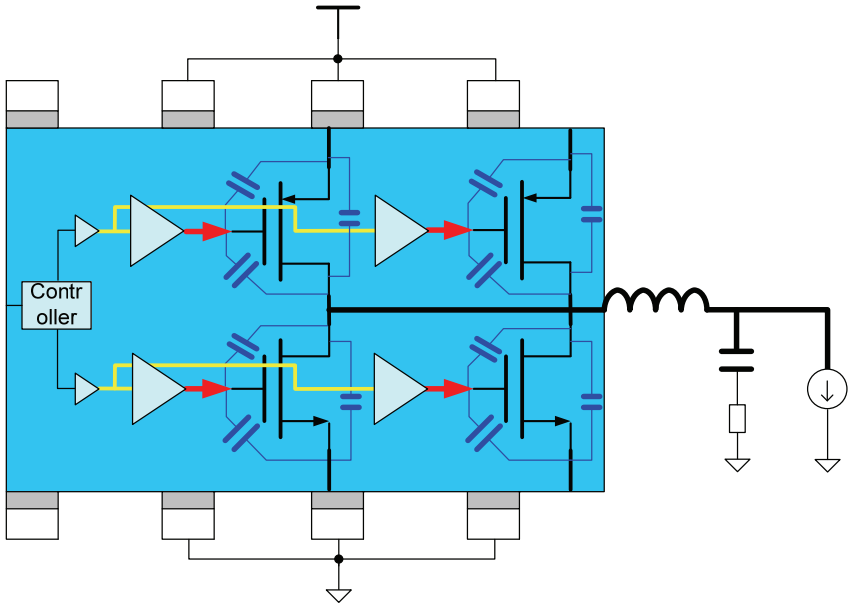


Figure 2-9. Parasitic capacitors in ISBC with two active power FET subcells.

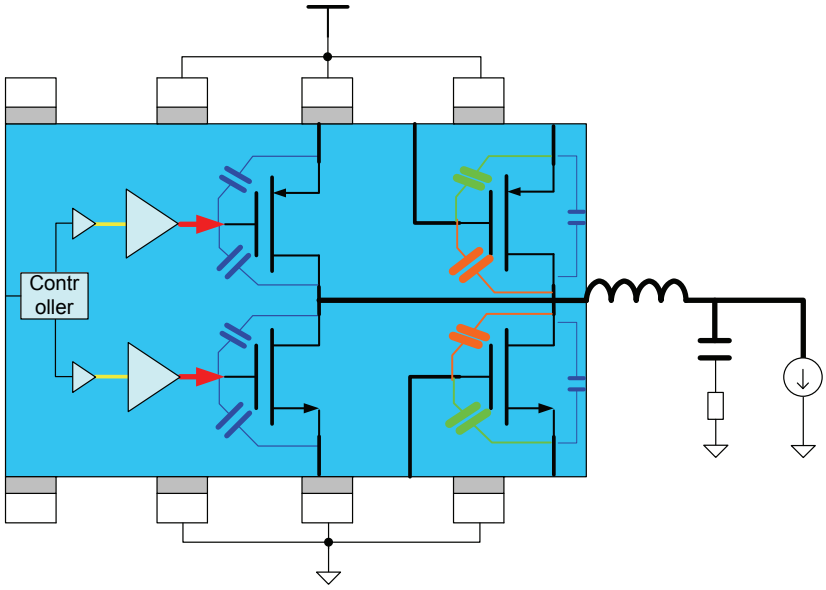


Figure 2-10. Parasitic capacitors in ISBC with one active and one inactive power FET subcells.

a). Violation of the first assumption

The topic cells in Figure 2-9 and 2-10 have the same C_{db}. However, their C_{gd} are much different. C_{gd} in Figure 2-9 is the Miller capacitance C_{rss} discussed in subsection 2.1.1.2, while C_{gd} in Figure 2-10 is the $C_{gd}^{(C)}$ clarified at the beginning of subsection 2.1. C_{gs} in the topic cells are also different. C_{gs} in Figure 2-9 is part of input capacitance C_{iss}, while C_{gs} in Figure 2-10 does not have charging/discharging process and vanishes in the respect of electric analysis.

Thus, when the segmentation technique is applied in the ISBC, the power FET subcells parasitic capacitors are possible to be different. Some parasitic capacitances of the active power FET subcells are significant different from those of the inactive ones.

b). Violation of the second assumption

Another assumption of the present switching loss analysis is that the flowing directions of charging/discharging currents in all power FET subcells are assumed to be the same. Figure 2-11 shows the flow directions of transient charging/discharging currents in an ISBC with two active power FET subcells when the control power FET turns on. Figure 2-12 shows the flow directions in an ISBC with one active and one inactive power FET subcells.

It is observed that the control FETs C_{gs} charging/discharging current of the topic cell in Figure 2-11 flows into the gnd, while that in Figure 2-12 flows back to the vdd.

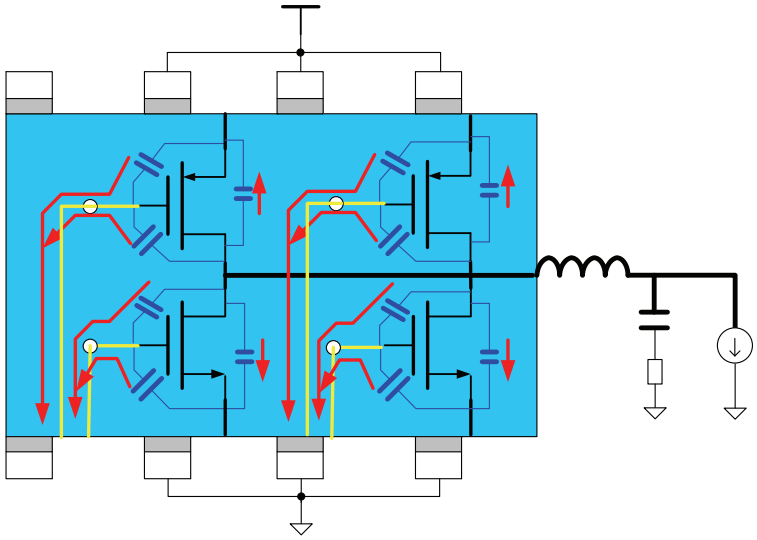


Figure 2-11. Charging/discharging current in ISBC with two active FET subcells

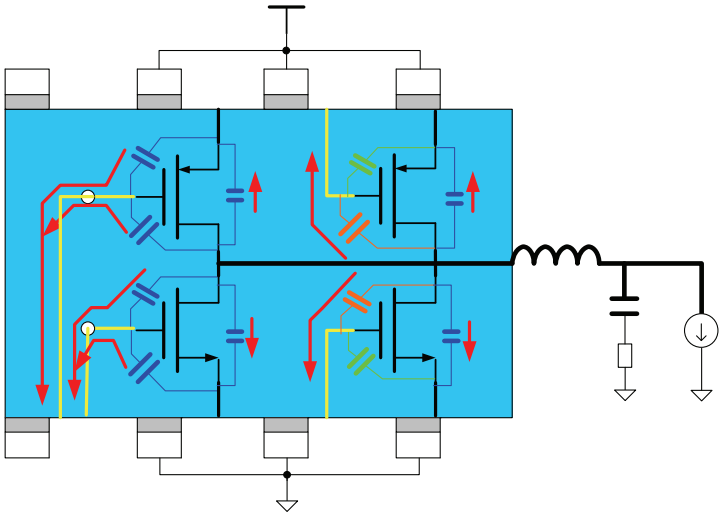


Figure 2-12. Charging/discharging current in ISBC with one active and one inactive FET subcells.

2.1.1.4 Other comments

The previous analysis manifests that the present power losses analysis cannot be utilized to investigate the variation of power losses due to the inaction of some power FET subcells. The reason behind the fact is that the present power losses analysis methods were developed to explain the time domain behaviors of Buck converter in switching transient, while they did not address the insight physical mechanism of the losses. In another word, the present power losses analysis methods were various kinds of behavior explanation of losses and they were weak in providing theoretical guidance for the power stage design and efficiency optimization.

Several other comments for the present power losses analysis include:

- Vaguely physical separation of charging/discharging and overlap loss;
- Miller plateau was assumed to always exist in the control FET turn-on and tunr-off events;
- No equation for calculating the Miller plateau voltage or the equations did not pay attention to the difference between the control PFET turn-on and turn-off event;
- No equation for explaining the variation of the deadtime to the load current;
- No equation for the determination of the driver size or the driver optimization and the power FET optimization are totally separated.

2.1.2 What is expected in a novel switching loss analysis

In the Chapter, the previous approaches were reconsidered and a novel one is proposed to satisfy the following expectations.

From the subsection 2.1.1.3, we realize that the first thing we want to do is to breakdown the power FET transient current and the related losses and analyze each component's generation mechanism. The second thing we want do is to pay attention to the capacitance variation of the parasitic capacitor during the switching event when the

operation region of the power FET changes, and investigate the energy variation of the parasitic capacitor in each switching event. The third thing we want to do is to develop a criterion to predict the onset of Miller plateau and explain why in some applications we cannot observe Miller plateau in control FET turn-on off event.

Another expectation for the novel switching loss analysis method is that we hope the proposed method not only can explain the physical mechanism of switching loss, but also is a handful too for a complete and systematic power stage optimization design. For example, with the aid of the novel concepts and methods, we can do the following design:

1). Determine the minimum value of dead-time and predict the dead-time conduction loss in different load condition;

2). Determine the optimal driver width from total loss optimization in ISBC;

3). Determine the number of active power PFET cells in different load conditions for the minimum energy loss.

2.2 Breakdown of switching loss

Figure 2-13 illustrates breakdown of the current in a ISBC when the power PFET is turned on and Figure 2-14 illustrates the current flow physical route in the cross section of ISBC. The current conducted by the power PFET includes four parts.

In Figure 2-13, from left to right, the first component is the discharging current of C_{gd_p}, the second component is the charging current of C_{gd_n} and C_{db_n}, the third component part is the inductor current I_L and the forth component is the current to charge the C_{db_p}. Thus, the total physical loss dissipated in the channel of the power PFET should be divided into four components too and only the third one will be calculated as $V_{ds} * I_L$.

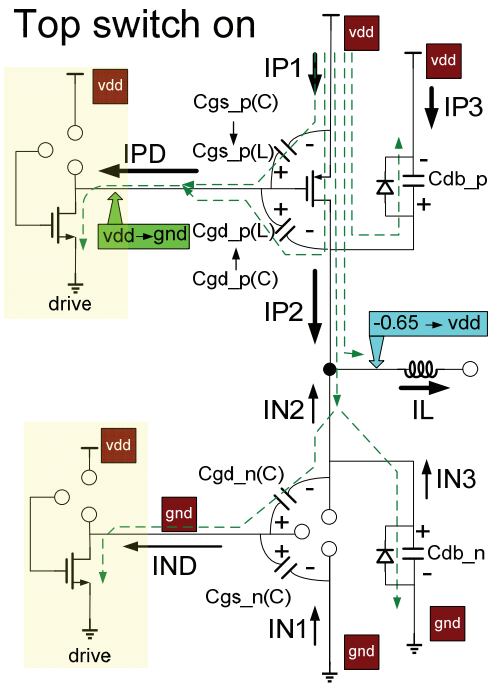


Figure 2-13 Breakdown analysis of current flowing during power PFET turn-on

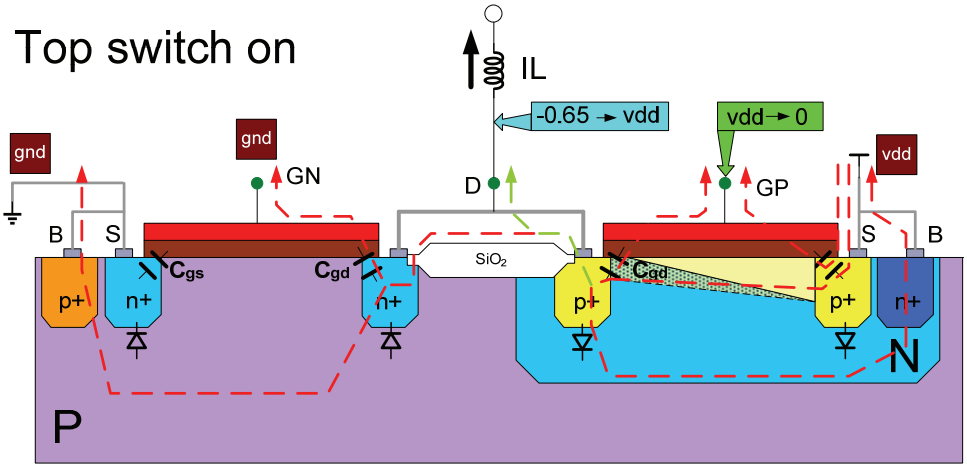


Figure 2-14. Current flowing in the cross section of ISBC

On the basis of the above physical loss breakdown concepts, in the dissertation, the switching losses in an ISBC are specified as three parts respectively being C_loss, O_loss and D_loss.

C_loss specifies all of the losses related to the charging and discharging current of the power FET parasitic capacitors. C_loss is created by the resistive components included in the charging/discharging loop. For example, power FET rdson, metal wire resistor, driver rdson, substrate or well resistor.

O_loss specifies other part of losses generated in the power FET channel without relationship to the charging/discharging current. As the O_loss will be calculated in the format of IL*Vds, it is also called overlap loss sometimes.

D_loss specifies the charging/discharging losses relative to the power FET driver's parasitic capacitance. In much different from the power FET which is loaded by inductance current source, the driver FET is loaded by pure capacitance. Thus, there is no O_loss in the driver.

2.3 O_loss analysis

For the ISBC, we are used to only caring about the overlap loss of the control power PFET (top switch) and ignoring that of the synchronous power NFET (bottom switch). The subsection will investigate when the power PFET will work in the saturation region through developing criterion for the onset of the Miller plateau. Also, the subsection will explain why we can ignore the overlap loss in the power NFET. Furthermore, how to properly set the value of dead-time is introduced.

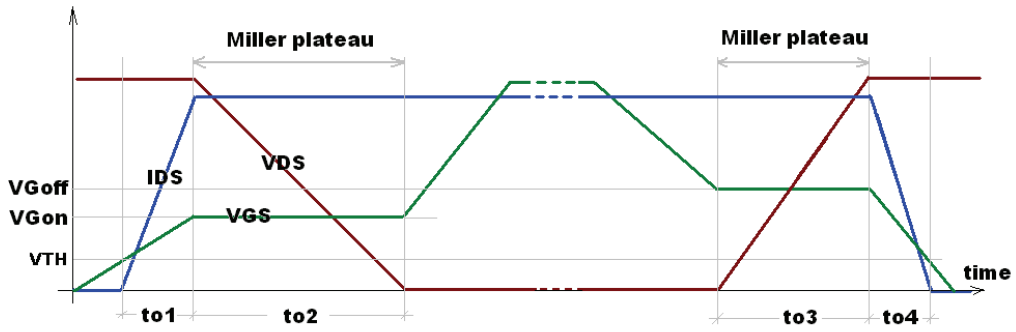


Figure 2-15. Miller plateau when the power FET turns on and off

O_loss becomes significant when the power FET operates in the saturation region during switching events. The simplified piecewise linear voltage and current waveforms when O_loss is significant are illustrated in Figure 2-15. It should be mentioned that Figure 2-15 is only suitable for conceptual explanation. The turn-on transient is in fact much different from the turn-off transient and the difference will be discussed later.

t_{o1} is the time between $v_g = V_g^{P\_on}$ and $v_g = V_{dd} - V_{TH}^P$, during which the PEFT turns on and Ids rises from zero to the peak value. t_{o2} is the sustaining time of the turn-on Miller plateau, during which the switching node voltage changes from 0V to Vdd.

t_{o3} is the sustaining time of turn-off Miller plateau, during which the switching node voltage changes from vdd to 0V. t_{o4} is the time between $v_g = V_g^{P\_off}$ and $v_g = V_{dd} - V_{TH}^P$, during which Ids returns to zero.

Therefore, O_loss related energy loss can be calculated with equations (2-1) and (2-2).

$$E_{overlap}^{PFET\_on} = \frac{1}{2} V_{dd} \left(I_o - \frac{1}{2} \Delta I_L \right) (t_{o1} + t_{o2}) \tag{2-1}$$

$$E_{overlap}^{PFET\_off} = \frac{1}{2} V_{dd} \left(I_o + \frac{1}{2} \Delta I_L \right) (t_{o3} + t_{o4}) \tag{2-2}$$

O_loss analysis will be carried out for all four switching events.

2.3.1 PFET turn-on event

2.3.1.1 Miller plateau equations

The Miller plateau is a distinctive characteristic of gate driver voltage. During the Miller plateau, the gate driver voltage first rapidly drops from Vdd then remains constant with a value of $V_g^{P\_on}$ for certain time until the switch node voltage V_{SW} approaches some value realizing PFET conduction in linear region. Thus, in the Miller plateau region, equations (2-3), (2-4), (2-5), (2-6) are applied using the variables depicted in Figure 2-16, which depicts the equivalent circuit of the ISBC power stage in the Miller plateau region.

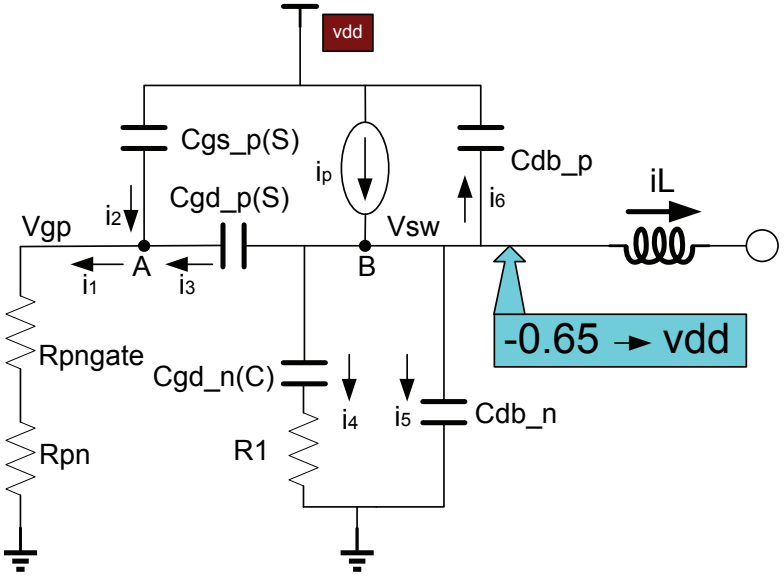


Figure 2-16 Miller plateau onset analysis in the power PFET turn-on transient

$$i_2 = 0 \tag{2-3}$$

$$i_1 = i_3 = \frac{V_g^{P\_on}\varphi_{P\_N}W_P^{active}}{\left(R_{unit}^{N} + R_{gate}^{PN}\varphi_{P\_N}W_P^{active}\right)} = \frac{V_g^{P\_on}\varphi_{P\_P}W_P^{active}}{\left(3R_{unit}^{N} + R_{gate}^{PN}\varphi_{P\_P}W_P^{active}\right)} \tag{2-4}$$

$$i_3 + i_4 + i_5 + i_6 + \left(I_o - \frac{\Delta I_L}{2} \right) = i_P \tag{2-5}$$

$$i_P = KW_P^{active} \left(V_g^{P\_on} - V_{dd} + V_{TH}^P \right)^2 \tag{2-6}$$

in which $K_P = \frac{\mu_P \varepsilon_{ox}}{t_{ox} L_{AMI06}}$. R_{gate}^{PN} is determined by the metal sheet resistance and route layout of the power PFET driver in the ISBC.

The values of i_3, i_4, i_5 and i_6 should satisfy equation (2-7) as $C_{gd\_p}^{(S)}$, $C_{gd\_n}^{(C)}$, C_{db_p} and C_{db_n} all have the switching node as one terminal and their other terminals have a constant voltage level.

$$\frac{i_3}{C_{gd\_P}^{(S)} W_P^{active}} = \frac{i_4}{C_{gd\_N}^{(C)} W_N} = \frac{i_5}{C_{db\_N} W_N} = \frac{i_6}{C_{db\_P} W_P} \tag{2-7}$$

We notice that $C_{gd\_P}^{(S)} = C_{gd\_P}^{(C)}$ is true in the saturation region, so we conclude (2-8),

$$i_3 \frac{\left(C_{gd\_P}^{(C)} W_P^{active} + C_{gd\_N}^{(C)} W_N + C_{db\_N} W_N + C_{db\_P} W_P \right)}{C_{gd\_P}^{(C)} W_P^{active}} + \left(I_o - \frac{\Delta I_L}{2} \right) = \tag{2-8}$$

$$= K_P W_P^{active} \left(V_g^{P\_on} - V_{dd} + V_{TH}^P \right)^2$$

Substituting $i_3 = \frac{V_g^{P\_on} \varphi_{P\_P} W_P^{active}}{\left(3R_{unit}^N + R_{gate}^{PN} \varphi_{P\_P} W_P^{active} \right)}$ into the above equation, we obtain (2-9).

$$\frac{V_g^{P\_on} \varphi_{P\_P}}{\left(3R_{unit}^N + R_{gate}^{PN} \varphi_{P\_P} W_P^{active} \right)} \frac{\left(C_{gd\_P}^{(C)} + C_{gd\_N}^{(C)} \frac{W_N}{W_P^{active}} + C_{db\_N} \frac{W_N}{W_P^{active}} + C_{db\_P} \frac{W_P}{W_P^{active}} \right)}{C_{gd\_P}^{(C)}}$$

$$+\frac{\left(I_o-\frac{\Delta I_L}{2}\right)}{W_P^{active}}=K_P\left(V_g^{P\_on}-V_{dd}+V_{TH}^P\right)^2 \qquad (2\text{-}9)$$

We introduce two intermediate variables z_1 and z_2 to simplify the equation's expression.

$$z_1^{(1)}=\frac{\varphi_{P\_P}}{\left(3R_{unit}^N+R_{gate}^{PN}\varphi_{P\_P}W_P^{active}\right)}\frac{\left(C_{gd\_P}^{(C)}+C_{gd\_N}^{(C)}\frac{W_N}{W_P^{active}}+C_{db\_N}\frac{W_N}{W_P^{active}}+C_{db\_P}\frac{W_P}{W_P^{active}}\right)}{C_{gd\_P}^{(C)}}$$

$$z_2=V_{dd}-V_{TH}^P \qquad (2\text{-}10)$$

Now, we get $z_1^{(1)}V_g^{P\_on}+\frac{\left(I_o-\frac{\Delta I_L}{2}\right)}{W_P^{active}}=K_P\left(V_g^{P\_on}-z_2\right)^2 \qquad (2\text{-}11)$

2.3.1.2 Miller plateau criterion

The solution of $V_g^{P\_on}$ is given by equation (2-12),

$$V_g^{P\_on}=\frac{z_1^{(1)}+2K_Pz_2\pm\sqrt{z_1^{(1)2}+4K_P\left[z_1^{(1)}z_2+\frac{\left(I_o-\frac{\Delta I_L}{2}\right)}{W_P^{active}}\right]}}{2K_P} \qquad (2\text{-}12)$$

As $V_g^{P\_on}$ should be located in the range $\left[0,V_{dd}-V_{TH}^P\right]$, a reasonable solution is (2-13),

$$V_g^{P\_on} = \frac{z_1^{(1)} + 2K_P z_2 - \sqrt{z_1^{(1)2} + 4K_P\left[z_1^{(1)} z_2 + \frac{\left(I_o - \frac{\Delta I_L}{2}\right)}{W_P^{active}}\right]}}{2K_P} \tag{2-13}$$

The equation implies us several characteristics of the design:

1) An important inference from the above equation is that there is always a solution for $V_g^{P\_on}$ independent of the operation condition, power stage and driver design, provided that $\left(I_o - \frac{\Delta I_L}{2}\right) > 0$ is satisfied. The criterion is in general met because we will usually put a Buck converter work in the DCM mode in the light load condition to improve power efficiency. Thus, we can conclude that the Miller plateau is inevitable for the PFET turn-on event.

2) If we do not apply a power stage segmentation technique, that is, $W_P^{active} = W_P$ is always true, the value of $V_g^{P\_on}$ will increase as the load current decreases. If we apply a power stage segmentation technique, the sensitivity of $V_g^{P\_on}$ to load conditions can be decreased to some extent.

3) The impact of segmentation (active PFET width W_P^{active}) to $V_g^{P\_on}$ is not straightforward. $z_1^{(1)}$ is inverse proportional to W_P^{active} but in the right hand side of the equation (2-13) we observe that the impact of W_P^{active} is cancelled to some extent. Ignoring some less significant items, we rewrite the equation (2-13) as (2-14) and (2-15)

$$V_g^{P\_on} = z_2 - \sqrt{\frac{z_1^{(1)} z_2}{K_P} + \frac{\left(I_o - \frac{\Delta I_L}{2}\right)}{K_P W_P^{active}}} \tag{2-14}$$

From the equation, we find that $V_g^{P\_on}$ is directly proportional to W_P^{active} and inversely proportional to $z_1^{(1)}$.

2.3.1.3 O_loss during PFET turn-on

The sustaining time of the Miller plateau t_{o2} can be approximately calculated by the time needed to charge the switching node from zero to V_{dd} as given in (2-15).

$$i_3 = C_{gd\_P}^{(S)} W_P^{active} \frac{V_{dd}}{t_{o2}} = \frac{V_g^{P\_on} \varphi_{P\_P} W_P^{active}}{\left(3R_{unit}^N + R_{gate}^{PN} \varphi_{P\_P} W_P^{active}\right)} \tag{2-15}$$

So we conclude (2-16).

$$t_{o2} = \frac{C_{gd\_P}^{(S)} V_{dd} \left(3R_{unit}^N + R_{gate}^{PN} \varphi_{P\_P} W_P^{active}\right)}{V_g^{P\_on} \varphi_{P\_P}} \tag{2-16}$$

The falling time t_{o1} is calculated with the simplification that the switch node voltage variation is ignored. The gate driver voltage v_g can be predicted by (2-17).

$$v_g = V_{dd} e^{-\frac{t \varphi_{P\_N}}{\left(R_{unit}^N + R_{gate}^{PN} \varphi_{P\_N} W_P^{active}\right)\left(C_{gd\_p}^{(S)} + C_{gs\_P}^{(S)}\right)}}. \tag{2-17}$$

t_{o1} is the time that the gate voltage v_g needs to change from $v_g = V_{dd} - V_{TH}^P$ to $v_g = V_g^{P\_on}$ and is calculated by (2-18).

$$t_{o1} = \frac{\left(3R_{unit}^N + R_{gate}^{PN} \varphi_{P\_P} W_P^{active}\right)\left(C_{gd\_p}^{(C)} + C_{gs\_P}^{(S)}\right)}{\varphi_{P\_P}} \ln\left(\frac{V_{dd} - V_{TH}^P}{V_g^{P\_on}}\right) \tag{2-18}$$

From (2-1), we conclude the overlap loss for the PFET turn-on events in (2-19).

$$E_{overlap}^{PFET\_on} = \frac{1}{2}V_{dd}\left(I_o - \frac{1}{2}\Delta I_L\right)\frac{\left(3R_{unit}^{N} + R_{gate}^{PN}\varphi_{P\_P}W_P^{active}\right)}{\varphi_{P\_P}} \left[\left(C_{gd\_p}^{(C)} + C_{gs\_P}^{(S)}\right)\ln\left(\frac{V_{dd} - V_{TH}^{P}}{V_g^{P\_on}}\right) + \frac{C_{gd\_P}^{(C)}V_{dd}}{V_g^{P\_on}}\right] \quad (2\text{-}19)$$

2.3.2 PFET turn-off event

The difference between the PFET turn "***off***" and "***on***" event is given by the opposite directions of the parasitic capacitors' charging and discharging currents during the switching event as that shown in Figure 2-17.

When there is a Miller plateau in the turn-off event, the gate driver voltage first rapidly rises from zero then remains constant with a value of $V_g^{P\_off}$ for certain time until the switch node voltage V_{SW} approaches some value stopping PFET conduction. Thus, for the Miller plateau condition, equations (2-20), (2-21), (2-22) and (2-23) apply, using the variables depicted in the Figure 2-17.

$$i_2 = 0 \quad (2\text{-}20)$$

$$i_1 = i_3 = \frac{\left(V_{dd} - V_g^{P\_off}\right)\varphi_{P\_P}W_P^{active}}{\left(R_{unit}^{P} + R_{gate}^{PP}\varphi_{P\_P}W_P^{active}\right)} \quad (2\text{-}21)$$

$$i_3 + i_4 + i_5 + i_6 + i_P = \left(I_o + \frac{\Delta I_L}{2}\right) \quad (2\text{-}22)$$

$$i_P = KW_P^{active}\left(V_g^{P\_off} - V_{dd} + V_{TH}^{P}\right)^2 \quad (2\text{-}23)$$

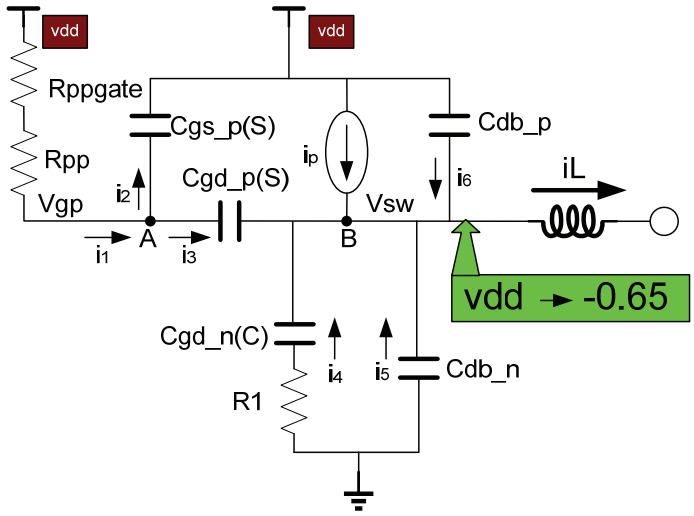


Figure 2-17. Miller plateau onset analysis in the power PFET turn-off transient

2.3.2.1 Miller plateau analysis

Similar to the turn-on event, the values of i_3, i_4, i_5 and i_6 should satisfy the equation (2-24) as $C_{gd\_p}^{(S)}$, $C_{gd\_n}^{(C)}$, C_{db_p} and C_{db_n} all have the switching node as one terminal and their other terminals have a constant voltage level.

$$\frac{i_3}{C_{gd\_P}^{(S)} W_P^{active}} = \frac{i_4}{C_{gd\_N}^{(C)} W_N} = \frac{i_5}{C_{db\_N} W_N} = \frac{i_6}{C_{db\_P} W_P} \tag{2-24}$$

Because $C_{gd\_P}^{(S)} = C_{gd\_P}^{(C)}$ is true in the saturation region, we obtain (2-25).

$$i_3 \frac{\left(C_{gd\_P}^{(S)} W_P^{active} + C_{gd\_N}^{(C)} W_N + C_{db\_N} W_N + C_{db\_P} W_P\right)}{C_{gd\_P}^{(C)} W_P^{active}} + K_P W_P^{active} \left(V_g^{P\_off} - V_{dd} + V_{TH}^P\right)^2 =$$

$$= \left(I_o + \frac{\Delta I_L}{2}\right) \tag{2-25}$$

in which $K_P = \dfrac{\mu_P \varepsilon_{ox}}{t_{ox} L_{AMI06}}$.

Substituting $i_3 = \dfrac{\left(V_{dd} - V_g^{P\_off}\right)\varphi_{P\_P} W_P^{active}}{\left(R_{unit}^P + R_{gate}^{PP}\varphi_{P\_P} W_P^{active}\right)}$ into the above equation, we obtain,

$$\frac{\left(V_{dd} - V_g^{P\_off}\right)\varphi_{P\_P}}{\left(R_{unit}^P + R_{gate}^{PP}\varphi_{P\_P} W_P^{active}\right)} \frac{\left(C_{gd\_P}^{(S)} + C_{gd\_N}^{(C)} \dfrac{W_N}{W_P^{active}} + C_{db\_N} \dfrac{W_N}{W_P^{active}} + C_{db\_P} \dfrac{W_P}{W_P^{active}}\right)}{C_{gd\_P}^{(C)}} +$$

$$+ K_P W_P^{active} \left(V_g^{P\_off} - V_{dd} + V_{TH}^P\right)^2 = \left(I_o + \frac{\Delta I_L}{2}\right) \tag{2-26}$$

We use the intermediate variables $z_1^{(2)}$ in (2-27) and z_2 in (2-10) to simplify the equation's expression and get (2-28).

$$z_1^{(2)} = \frac{\varphi_{P\_P}}{\left(R_{unit}^P + R_{gate}^{PP}\varphi_{P\_P} W_P^{active}\right)} \frac{\left(C_{gd\_P}^{(C)} + C_{gd\_N}^{(C)} \dfrac{W_N}{W_P^{active}} + C_{db\_N} \dfrac{W_N}{W_P^{active}} + C_{db\_P} \dfrac{W_P}{W_P^{active}}\right)}{C_{gd\_P}^{(C)}} \tag{2-27}$$

$$z_1^{(2)}\left(V_{dd} - V_g^{P\_on}\right) + K_P\left(V_g^{P\_off} - z_2\right)^2 = \frac{\left(I_o + \dfrac{\Delta I_L}{2}\right)}{W_P^{active}} \tag{2-28}$$

2.3.2.2 Miller plateau criterion

The solution of $V_g^{P\_off}$ is given in (2-29).

$$V_g^{P\_off} = \frac{z_1^{(2)} + 2K_P z_2 \pm \sqrt{z_1^{(2)^2} + 4z_1^{(2)} z_2 K_P + 4K_P \frac{\left(I_o + \frac{\Delta I_L}{2}\right)}{W_P^{qctive}} - 4z_1^{(2)} V_{dd} K_P}}{2K_P} \tag{2-29}$$

As $V_g^{P\_off}$ should be located in the range $\left[0, V_{dd} - V_{TH}^P\right]$, a reasonable solution is given by (2-30).

$$V_g^{P\_off} = \frac{z_1^{(2)} + 2K_P z_2 - \sqrt{z_1^{(2)^2} - 4z_1^{(2)} V_{TH}^P K_P + 4K_P \frac{\left(I_o + \frac{\Delta I_L}{2}\right)}{W_P^{qctive}}}}{2K_P} \tag{2-30}$$

The equation gives us several possibilities for the design:

1) An important inference from the above equation is that there might not have a solution of $V_g^{P\_off}$ even when the Buck converter works under a heavy load condition, as the existence of $V_g^{P\_off}$ depends on whether the inequality equation (2-31) is satisfied.

$$MPoff = \frac{z_1^{(2)^2}}{K_P} - 4V_{TH}^P z_1^{(2)} + 4\frac{\left(I_o + \frac{\Delta I_L}{2}\right)}{W_P^{active}} \geq 0 \tag{2-31}$$

If there is no solution of $V_g^{P\_off}$, this indicates there will be no Miller plateau and no overlap loss when PFET turns off. This situation is an ideal case from the consideration of power efficiency. We will naturally approach the condition when I_o is low or we can artificially realize it through the design. As K_P is much larger than $z_1^{(2)}$, an efficient way to violate the inequality equation is to increase $z_1^{(2)}$ via an increase of φ_{P_P}.

2) If we do not apply the power stage segmentation technique, that is, $W_P^{active} = W_P$ is always true, the value of $V_g^{P\_off}$ will increase as the load current decreases.

If we apply the power stage segmentation technique, the sensitivity of $V_g^{P\_off}$ to load conditions can be decreased to some extent.

3) The impact of segmentation (active PFET width W_P^{active}) on $V_g^{P\_off}$ is more complex than $V_g^{P\_on}$. Ignoring some less significant items, we rewrite the equation as

$$V_g^{P\_off} = z_2 - \sqrt{\frac{1}{K_P}}\sqrt{\frac{\left(I_o + \frac{\Delta I_L}{2}\right)}{W_P^{active}}} - z_1^{(2)} V_{TH}^P \tag{2-32}$$

From the equation, we realize that the relationship between $V_g^{P\_off}$ and W_P^{active} depends on the load condition I_o.

2.3.2.3 O_loss during PFET turn-off

The sustaining time of the Miller plateau t_{o3} can be approximately calculated with the time which is needed to charge the switching node from zero to V_{dd} as given in (2-33).

$$i_3 = C_{gd\_P}^{(S)} W_P^{active} \frac{V_{dd}}{t_{o3}} = \frac{\left(V_{dd} - V_g^{P\_off}\right)\varphi_{P\_P} W_P^{active}}{\left(R_{unit}^P + R_{gate}^{PP}\varphi_{P\_P} W_P^{active}\right)} \tag{2-33}$$

So we conclude (2-34).

$$t_{o3} = \frac{C_{gd\_P}^{(S)} V_{dd}\left(R_{unit}^P + R_{gate}^{PP}\varphi_{P\_P} W_P^{active}\right)}{\left(V_{dd} - V_g^{P\_off}\right)\varphi_{P\_P}} \tag{2-34}$$

The rising time t_{o4} is calculated with the simplification that the switch node voltage variation is ignored. The gate driver voltage v_g can be predicted by (2-35)

$$v_g = V_{dd} - V_{dd} e^{-\frac{t\,\varphi_{P\_P}}{\left(R_{unit}^{P} + R_{gate}^{PP}\varphi_{P\_P}W_P^{active}\right)\left(C_{gd\_p}^{(C)} + C_{gs\_P}^{(S)}\right)}} \tag{2-35}$$

t_{o4} is the time that the gate voltage v_g needs to change from $v_g = V_g^{P\_off}$ to $v_g = V_{dd} - V_{TH}^{P}$ and is calculated by (2-36)

$$t_{o4} = \frac{\left(R_{unit}^{P} + R_{gate}^{PP}\varphi_{P\_P}W_P^{active}\right)\left(C_{gd\_p}^{(C)} + C_{gs\_P}^{(S)}\right)}{\varphi_{P\_P}} \ln\left(\frac{V_{TH}^{P}}{V_{dd} - V_g^{P\_off}}\right) \tag{2-36}$$

From (3-2) we can compute the overlap loss during the PFET turn-off events, which is given by (2-37).

$$E_{overlap}^{PFET\_off} = \frac{1}{2}V_{dd}\left(I_o + \frac{1}{2}\Delta I_L\right)\frac{\left(R_{unit}^{P} + R_{gate}^{PP}\varphi_{P\_P}W_P^{active}\right)}{\varphi_{P\_P}} \left[\left(C_{gd\_p}^{(C)} + C_{gs\_P}^{(S)}\right)\ln\left(\frac{V_{TH}^{P}}{V_{dd} - V_g^{P\_off}}\right) + \frac{C_{gd\_P}^{(C)}V_{dd}}{\left(V_{dd} - V_g^{P\_off}\right)}\right] \tag{2-37}$$

If we eliminate the Miller plateau in the PFET turn-off event via appropriate choice of φ_{P_P} to violate the criterion given by (2-31), the overlap loss in the event is negligible.

2.3.2.4 Dead time $t_{dead}^{2\_set}$ setting

In the case that the Miller plateau is eliminated by design, t_{o3} is the time that the gate voltage of the power PFET needs to be charged from zero to $V_{dd} - 0.5V_{TH}^{P}$. During this time, the switching node voltage remains constant at V_{dd} and the power PFET works in the linear region.

$$t_{o3} = \frac{\left(R_{unit}^{P} + R_{gate}^{PP}\varphi_{P\_P}W_{P}^{active}\right)}{\varphi_{P\_P}}\left(C_{gd\_p}^{(L)} + C_{gs\_p}^{(L)}\right)\ln\frac{2V_{dd}}{V_{TH}^{P}} \tag{2-38}$$

t_{o4} is the time that the switching node voltage v_{SW} needs to be discharged from V_{dd} to -0.65. During this time, the gate voltage remains constant at V_{dd} and the power PFET is turned off.

$$t_{o4} = \frac{\left(C_{gd\_p}^{(C)}W_P + C_{gd\_n}^{(C)}W_N + C_{db\_p}W_P + C_{db\_n}W_N\right)\left(V_{dd} + 0.65\right)}{\left(I_o + \frac{1}{2}\Delta I_L\right)} \tag{2-39}$$

The value of t_{o3} and t_{o4} will impact the power efficiency as they will decrease the dead-time time. As the value of t_{o4} is inversely proportional to the load current, the dead-time t_{dead}^{2} should be chosen for the minimal load current in CCM to avoid the condition that the switching node voltage had not dropped below $0V$ when power NFET begins conducting, otherwise, the power NFET might work in an abnormal mode and switching node voltage oscillation is more severe. On the basis of this consideration, the value of t_{dead}^{2} is selected as $t_{dead}^{2\_set}$ in (2-40).

$$t_{dead}^{2\_set} = t_{o3} + \frac{\left(C_{gd\_p}^{(C)}W_P + C_{gd\_n}^{(c)}W_N + C_{db\_p}W_P + C_{db\_n}W_N\right)\left(V_{dd} + 0.65\right)}{\left(I_o^{(CCM\_critical)} + \frac{1}{2}\Delta I_L\right)} \tag{2-40}$$

2.3.3 NFET turn-on event

In general, we seldom care about the overlap loss and Miller plateau during either the NFET turn-on or turn-off events. One popular explanation for the fact is that the synchronous NFET experiences a zero-voltage-switching. The subsection and the subsection 2.3.4 will explain the fact in another way.

We first investigate the NFET turn-on case. Because of the flow direction of the inductor current, the NFET's body diode will conduct if the switching node voltage is less than -0.65V. Thus, when the NFET works in the saturation region, the gate node voltage has to be in the range of $\left[-0.65+V_{TH}^{N}, V_{TH}^{N}\right]$.

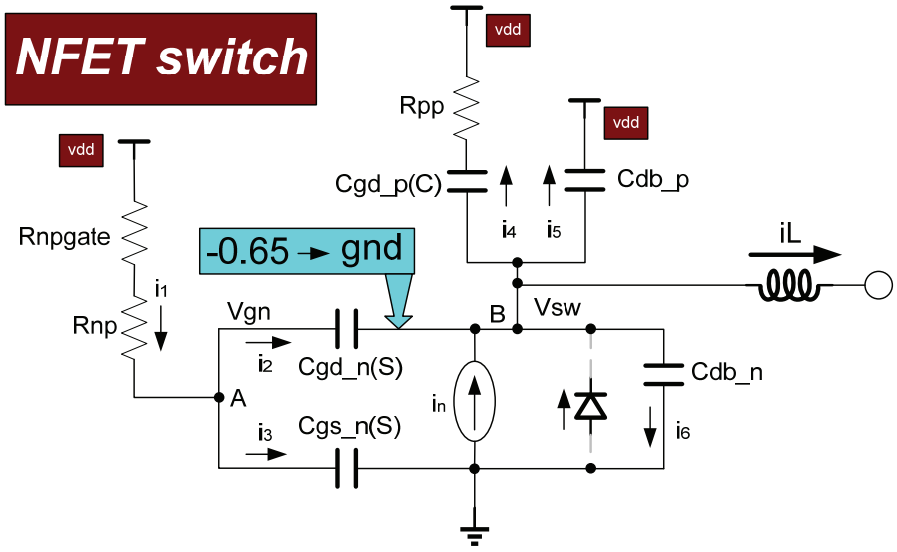


Figure 2-18. Miller plateau onset analysis in the power NFET turn-on transient

$$i_3 = 0 \tag{2-41}$$

$$i_1 = i_2 = \frac{\left(V_{dd} - V_g^{N\_on}\right)\varphi_{N\_P} W_N^{active}}{\left(R_{unit}^{P} + R_{gate}^{NP}\varphi_{N\_P} W_N^{active}\right)} = \frac{3\left(V_{dd} - V_g^{N\_on}\right)\varphi_{N\_N} W_N^{active}}{\left(R_{unit}^{P} + 3R_{gate}^{NP}\varphi_{N\_N} W_N^{active}\right)} \tag{2-42}$$

$$i_4 + i_5 + i_6 + \left(I_o + \frac{\Delta I_L}{2} \right) = i_2 + i_n \tag{2-43}$$

$$i_n = KW_N^{active} \left(V_g^{N\_on} + 0.65 - V_{TH}^N \right)^2 \tag{2-44}$$

Notice that there is a sign confliction here for i_2. Under the assumption that the switching node voltage level is rising and there is a constant gate voltage, i_2 should flow in the direction from right to left in the Figure 2-18 and $i_1 = i_2$ is true. However, as the gate voltage for the saturation region is limited in the range of $\left[-0.65 + V_{TH}^N, V_{TH}^N \right]$, i_1 should flow from high potential to low potential, that is, i_2 should flow in the direction from left to right in the Figure 2-18. Thus, we conclude that the assumption that there is a Miller plateau during the NFET turn-on is not true.

2.3.4 NFET turn-off event

We will also investigate whether there will be a Miller plateau during the NFET turn-off event. Similarly, to make sure that the NFET works in the saturation region, the gate node voltage has to be in the range of $\left[-0.65 + V_{TH}^N, V_{TH}^N \right]$.

$$i_3 = 0 \tag{2-45}$$

$$i_1 = i_2 = \frac{V_g^{N\_off} \varphi_{N\_N} W_N^{active}}{\left(R_{unit}^N + R_{gate}^{NN} \varphi_{N\_N} W_N^{active} \right)} \tag{2-46}$$

$$i_4 + i_5 + i_6 + i_n = i_2 + \left(I_o - \frac{\Delta I_L}{2} \right) \tag{2-47}$$

$$i_n = KW_N^{active} \left(V_g^{N\_off} + 0.65 - V_{TH}^N \right)^2 \tag{2-48}$$

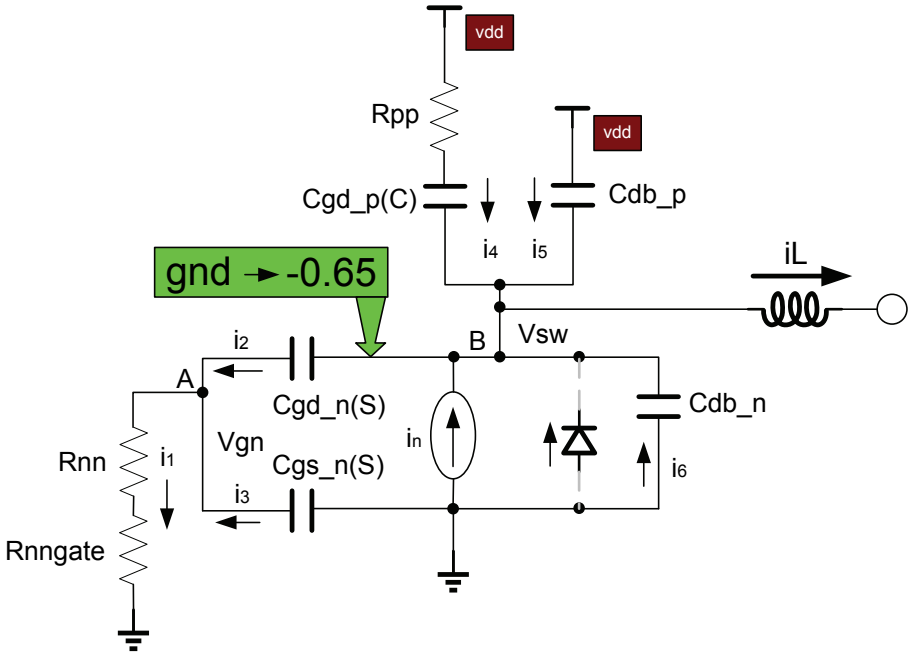


Figure 2-19. Miller plateau onset analysis in the power NFET turn-off transient

2.3.4.1 Sign confliction

We can observe a similar sign confliction of i_2 for the NFET turn-off event. Under the assumption that the switching node voltage level is dropping and there is a constant gate voltage, i_2 should flow in the direction from left to right in the Figure 2-19 and $i_1 = i_2$ is true. However, as the gate voltage for the saturation region is limited to the range of $\left[-0.65 + V_{TH}^N, V_{TH}^N\right]$, the gate voltage will be a positive value and i_1 should flow from high potential to low potential. Thus, i_2 should flow in the direction from right to left in the Figure 2-19. Thus, we also must eliminate the assumption that there is a Miller plateau during the NFET turn-off event.

2.3.4.2 Dead time $t_{dead}^{1\_set}$ setting

As the power NFET turn-on does not have a Miller plateau, the value of time t_{o1} (when the power NFET gate voltage drops from V_{dd} to zero) and t_{o2} (when the switching node voltage v_{SW} is discharged from zero to -0.65) can be calculated respectively with equations (2-49) and (2-50). In the calculation of t_{o1}, the switching node voltage is simplified as zero and the gate voltage drops from V_{dd} to $0.5V_{TH}^{N}$. In the calculation of t_{o2}, the gate voltage will remain constant at zero and the power NFET is already turned off.

$$t_{o1} = \frac{\left(R_{unit}^{N} + R_{gate}^{NN}\varphi_{N\_N}W_{N}^{active}\right)}{\varphi_{N\_N}}\left(C_{gd\_n}^{(L)} + C_{gs\_n}^{(L)}\right)\ln\frac{2V_{dd}}{V_{TH}^{N}} \tag{2-49}$$

$$t_{o2} = \frac{\left(C_{gd\_p}^{(C)}W_P + C_{gd\_n}^{(C)}W_N + C_{db\_p}W_P + C_{db\_n}W_N\right)0.65}{\left(I_o - \frac{1}{2}\Delta I_L\right)} \tag{2-50}$$

In a similar fashion to t_{o3} and t_{o4}, the value of t_{o1} and t_{o2} will impact the power efficiency as it will decrease the dead-time time. As the value of t_{o2} is inversely proportional to the load current, the dead-time t_{dead}^{1} should be set for the minimal load current in CCM to avoid the condition that the power NFET is not completely turned off when power PFET begins conducting, otherwise, there will be a current shoot through in power PFET and NFET. Furthermore, $C\frac{dv}{dt}$ phenomenon [2-27, 2-28] should be sufficiently considered to eliminate false turn-on of the power NFET but this analysis is complicated. Thus, a simplified design for $t_{dead}^{1\_set}$ is given in (2-51).

$$t_{dead}^{1\_set} = t_{o1} + 2.5\times10^{-9}\ (s) \tag{2-51}$$

2.4 C_loss classification

The losses related to the parasitic capacitor charging/discharging are difficult to analyze with time domain differential equations as multiple capacitors are connected to the same switching node and the capacitances will vary when the operation region of the power FET changes during switching. The section summarizes the characteristics of all charging/discharging loops, each of which is specified for an individual parasitic capacitor. The section concludes that there are totally five typical kinds of charging/discharging loops and each of them has an either one or zero ratio of C_loss.

The ratio of loss in a charging/discharging loop is defined as the ratio between the charging/discharging loss in the loop and the total energy variation of the capacitor during a complete switching event. The ratio of loss will be symbolized by λ.

2.4.1 Typical cases and the ratio of C_loss

If we analyze all of the charging/discharging loops for all of the parasitic capacitors in four switching transients of an ISBC, we find that there are in fact five typical loops accomplishing the capacitor's charging and discharging as illustrated in Figure 2-15. In the Figure 2-15, we assume that one terminal of the capacitors changes from V_A to V_B in a certain period of time.

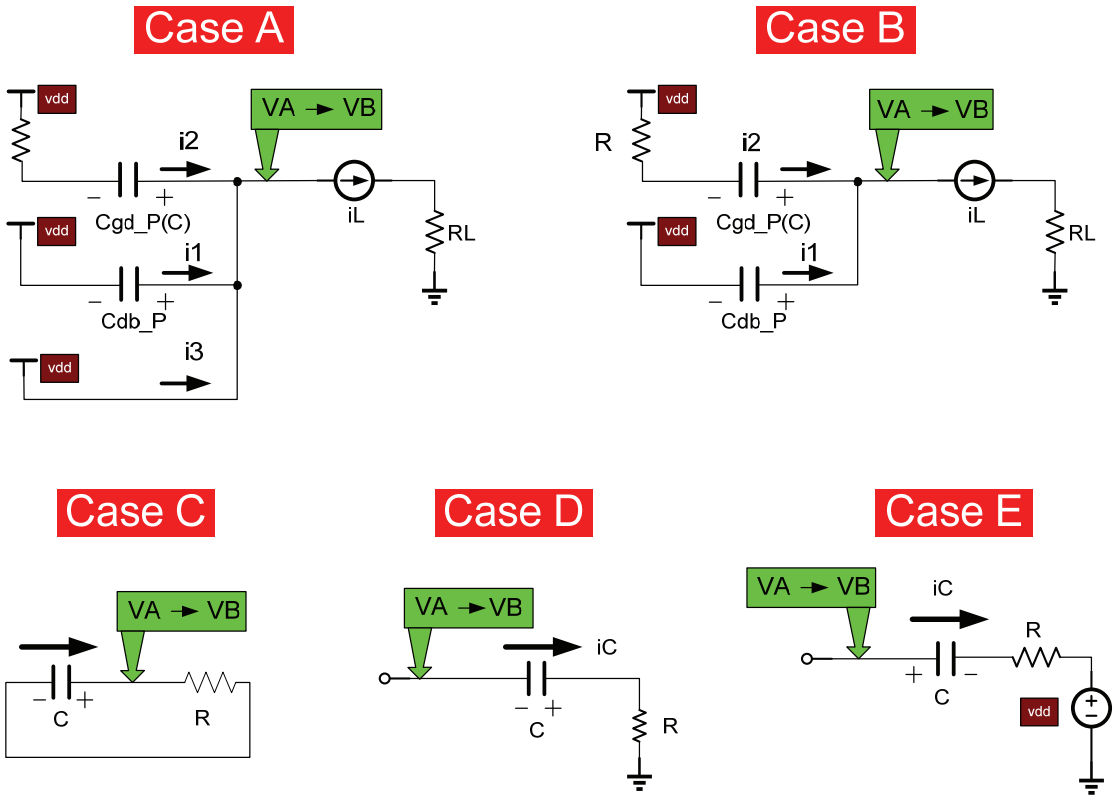


Figure 2-20. Five typical loops accomplishing the capacitor charging and discharging

In the case-A, a constant current is divided into three parts, two of which are the capacitors' charging/discharging currents, and the other one is supplied by Vdd. Thus, there is no limitation on the magnitudes of the capacitors' charging/discharging currents. Similar to a simple two components RC charging process, the generated heat dissipation in the case-A will be equal to the energy variation of the capacitor. Thus, in the case-A, we can obtain the C_loss from the energy variation of the capacitor, which is $0.5\left(C_{gd\_p}^{(C)}+C_{db\_p}\right)W\left[\left(V_{dd}-V_A\right)^2-\left(V_{dd}-V_B\right)^2\right]$ and will be in details discussed in subsection 2.5.3. The ratio of loss and capacitor energy variation is given in (2-52).

$$\lambda_A = 1 \tag{2-52}$$

Case-B is different from the case-A based on the fact that the constant current is only supplied by the charging/discharging currents of two capacitors. Thus, there is a magnitude constraint on the capacitor charging/discharging current. In this situation, the capacitor with larger capacitance will take a larger current in the relationship $i_2 = \frac{C_{gd\_p}^{(C)}}{C_{db} + C_{gd\_p}^{(C)}} I_L$. As C_{db} is a value significantly larger than $C_{gd\_p}^{(C)}$, the charging/discharging current flowing through $C_{gd\_p}^{(C)}$ will be much smaller than I_L. On the consideration that the well or substrate resistance is usually negligible and the transient will be completed in several nanoseconds, the energy loss in the charging/discharging loop can be ignored in comparison to the energy variation of the capacitors. The ratio of loss and capacitor energy variation is given in (2-53).

$$\lambda_B = 0 \tag{2-53}$$

Case-C and case-D are simple two components RC charging/discharging loops and their ratios of loss and capacitor energy variation are directly given in (2-54) and (2-55).

$$\lambda_C = 1 \tag{2-54}$$

$$\lambda_D = 1 \tag{2-55}$$

In case-E, the voltage across the parasitic resistor R will be much smaller than Vdd, so the energy dissipation due to R can be ignored and the energy recovered by the voltage source is almost equal to the energy variation of the capacitor. The ratio of loss and capacitor energy variation is given in (2-56).

$$\lambda_E = 0 \tag{2-55}$$

2.4.2 C_loss analysis in ISBC

Using the typical C_loss classification illustrated in the Figure 2-20, we investigate the type of C_loss in the ISBC for each parasitic capacitor in each switching event. The active and inactive power FET cells are separately discussed.

2.4.2.1 Active power FET cells

During different switching events, the parasitic components may have different types of charging/discharging loops. Thus, we will carry out C_loss breakdown analysis event by event.

1) Top switch turn-on

The power PFET turn-on event includes three sub-stages illustrated in Figure 2-21 and Figure 2-22. The c_loss classification is shown in Figure 2-23.

Cgs_p, Cgd_p, Cgd_n and Cdb_n have the case-D charging/discharging loops. Cdb_p has the class-C loop, so the energy losses equal the capacitor energy variation.

Cgs_n does not have capacitor energy variation, so there is no C_loss.

2) Top switch turn-off

Figure 2-24 illustrates the PFET turn-off event's two sub-stages and the related C_loss classification. Cgd_p(L) and Cgs_p(L) have the case-A charging/discharging loops, so the energy losses equal the capacitor energy variation. Cgd_p(C), Cdb_p, Cgd_n(C) and Cdb_n have the case-B charging/discharging loops so there is no energy loss during the capacitor energy variation. Cgs_n has no energy variation, so there is no loss.

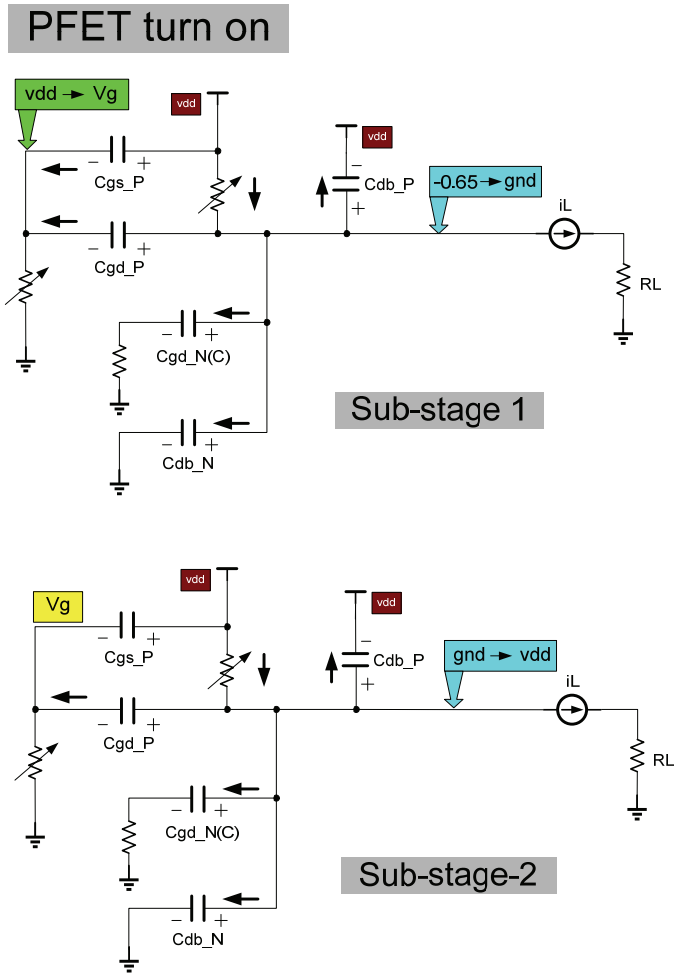


Figure 2-21 First two sub-stages in PFET turn-on event

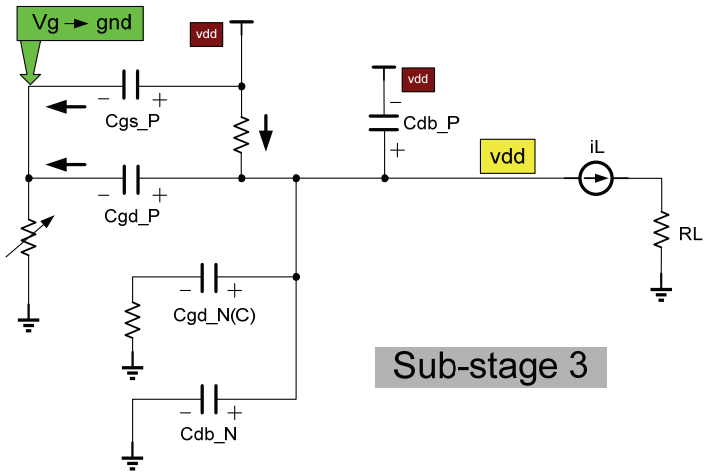


Figure 2-22 Third sub-stage in PFET turn-on event

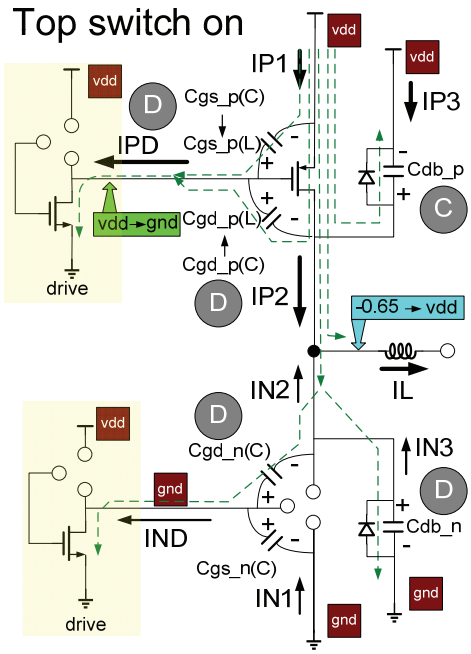


Figure 2-23 C_loss classification in PFET turn-on event

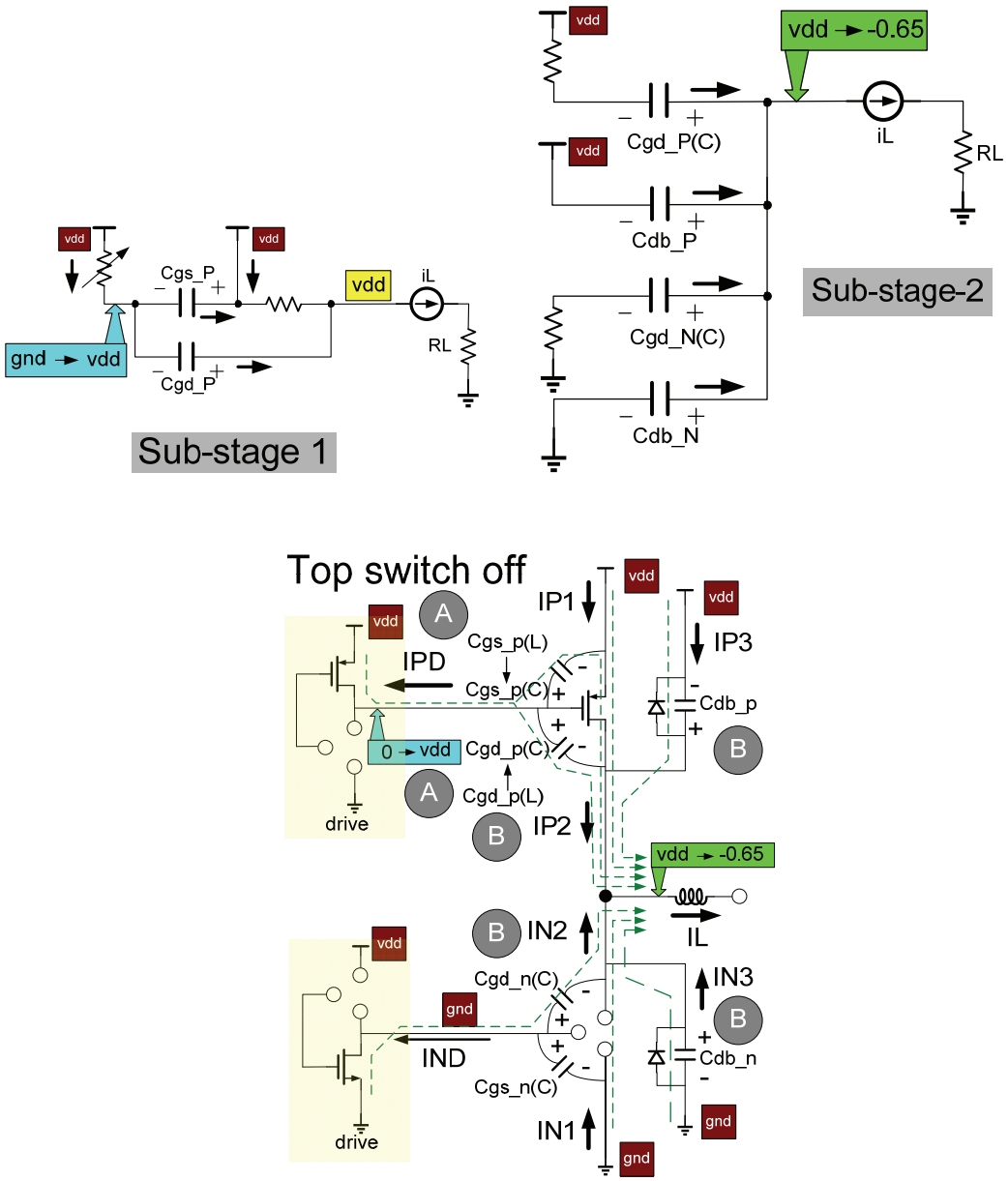
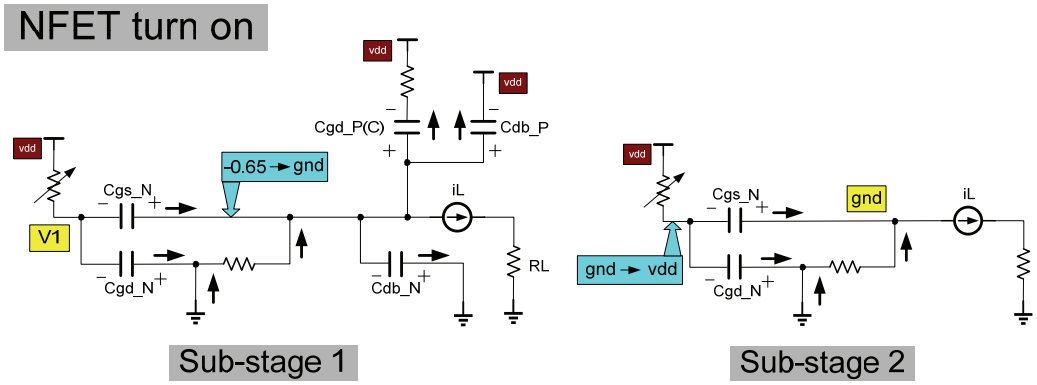


Figure 2-24 Two sub-stages in PFET turn-off event and C_loss classification

3) Bottom switch turn-on



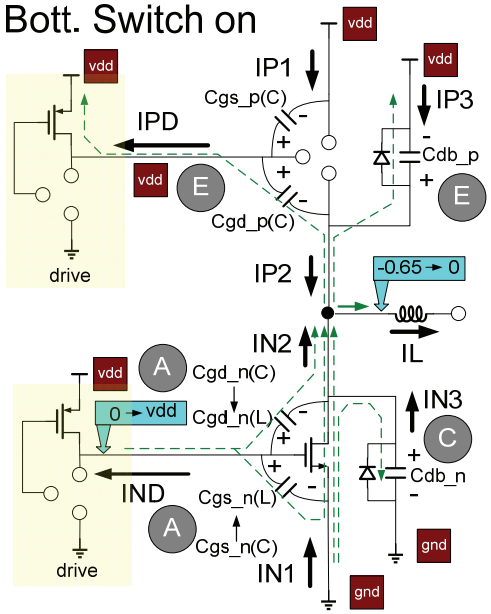


Figure 2-25 Two sub-stages in NFET turning on event and C_loss classification

Figure 2-25 illustrates the NFET turn-on event's two sub-stages and the related C_loss classification. Cgd_p(C) and Cdb_p have the case_E charging/discharging loops and zero C_loss. Cgd_n and Cgs_n have the case_A charging/discharging loops. Cdb_n has the case-C charging/discharging loop. Thus, the four capacitors' energy losses equal to their capacitor energy variation.

Cgs_p does not have energy variation, so there is no loss.

4) Bottom switch turn-off

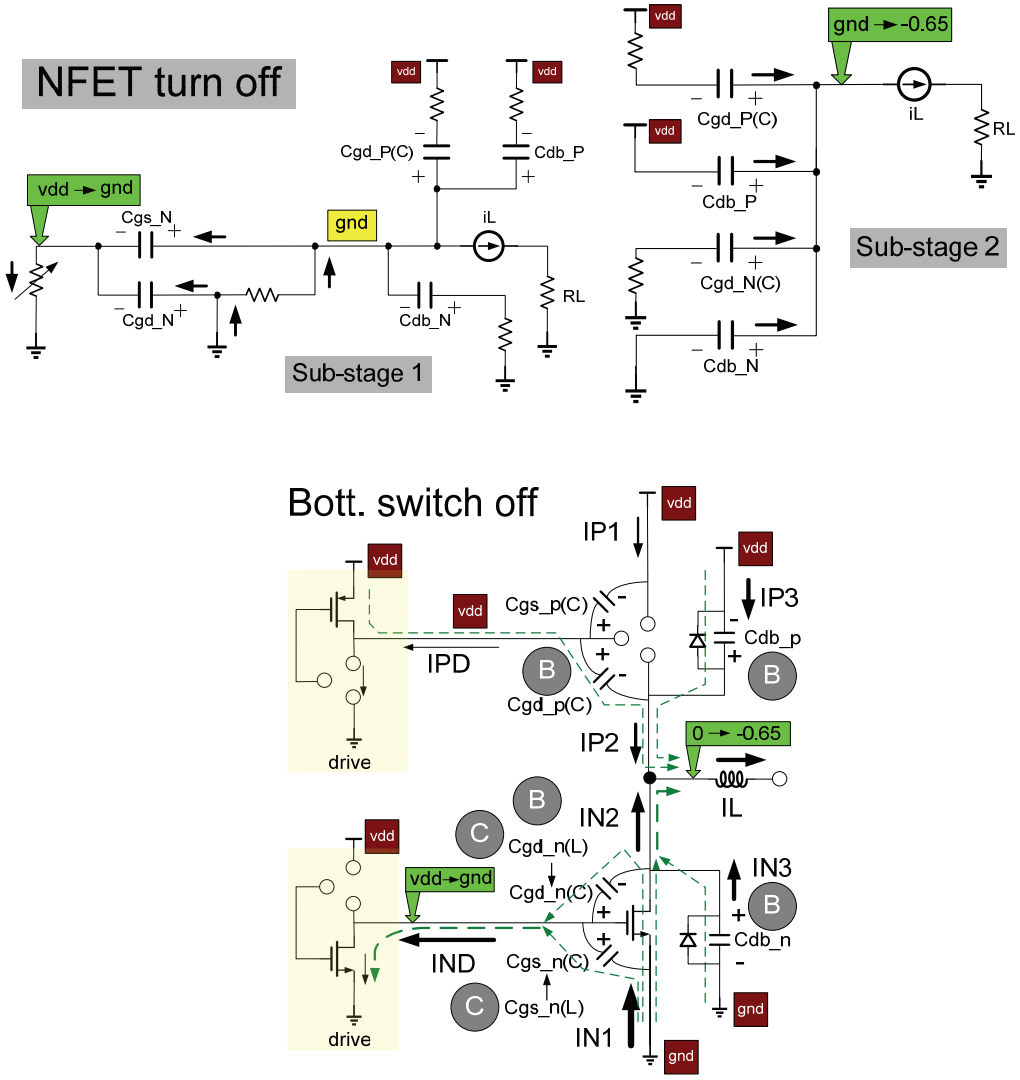


Figure 2-26 Two sub-stages in NFET turn-off event and C loss classification

Figure 2-26 illustrates the NFET turn-off event's two sub-stages and the related C_loss classification. Cgd_n(L) and Cgs_n(L) have the case-C charging/discharging loops, so the energy losses equal the capacitor energy variation. Cgd_p(C), Cdb_p, Cgd_n(C) and Cdb_n have the case-B charging/discharging loops, so the four capacitors have zero energy loss during the capacitor energy variation. Cgs_p does not have energy variation, so there is no loss.

2.4.2.2 Inactive power FET cells

The C_loss breakdown analysis for the inactive power FET cells is also carried out event by event.

1) Top switch turn-on

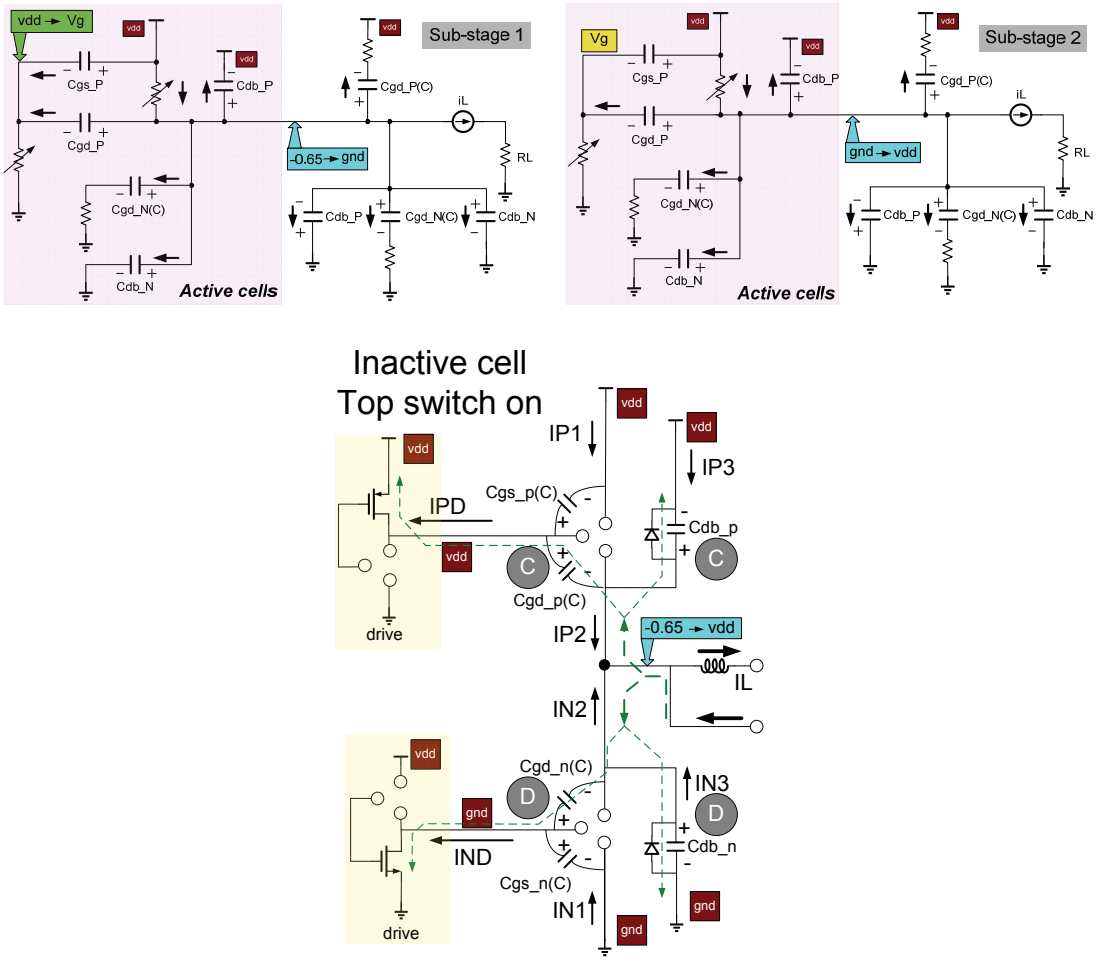


Figure 2-27 Inactive cells two sub-stages and C_loss classification when PFET turns on

Figure 2-27 illustrates the inactive power FET cells' two sub-stages and the related C_loss classification. Cgd_p(c) and Cdb_p have the case-C charging/discharging loops. Cgd_n(c) and Cdb_n have the case-D charging/discharging loops. Thus, the energy losses equal the capacitor energy variation.

2) Top switch turn-off

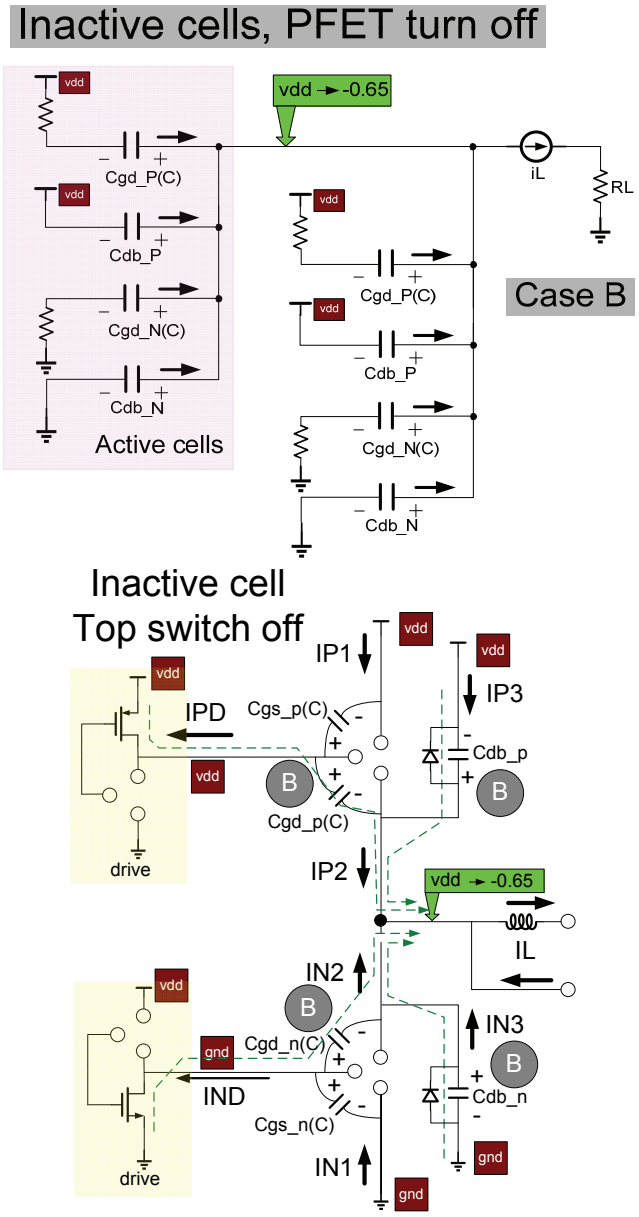


Figure 2-28 Inactive cells two sub-stages and C_loss classification when PFET turns off

Figure 2-28 illustrates the inactive power FET cells' two sub-stages and the related C_loss classification. Cgd_p(c), Cdb_p, Cgd_n(c) and Cdb_n all have the Case-B charging/discharging loops. Thus, the four capacitors have zero C_loss.

3) Bottom switch turn-on

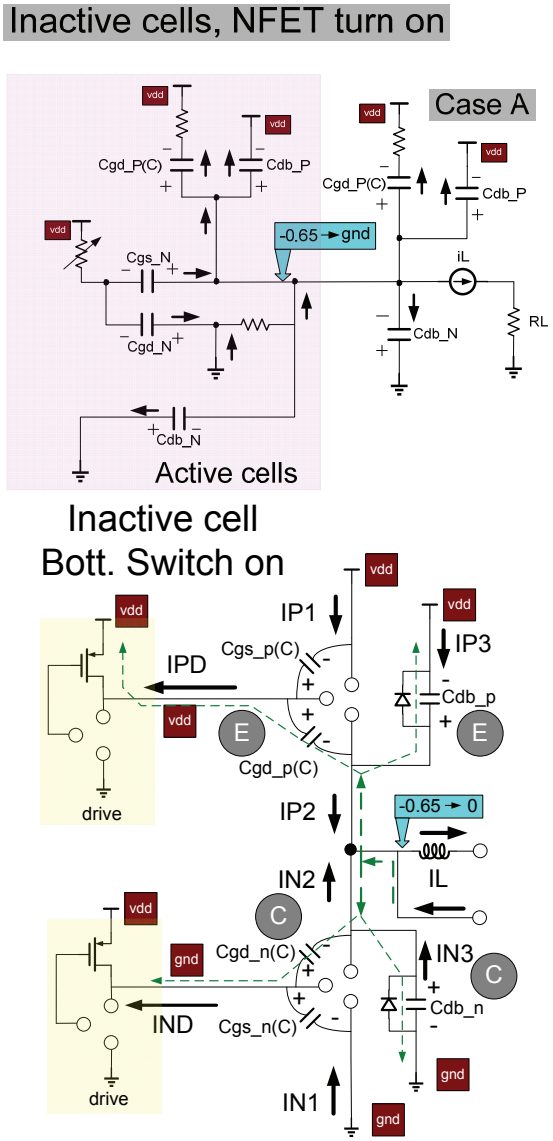


Figure 2-29 Inactive cells two sub-stages and C_loss classification when NFET turns on

Figure 2-29 illustrates the inactive power FET cells' two sub-stages and the related C_loss classification. Cgd_p(c) and Cdb_p have the case-E charging/discharging loops, so they have zero C_loss. Cgd_n(c) and Cdb_n have the case-A charging/discharging loops, so the energy losses equal the capacitor energy variation.

4) Bottom switch turn-off

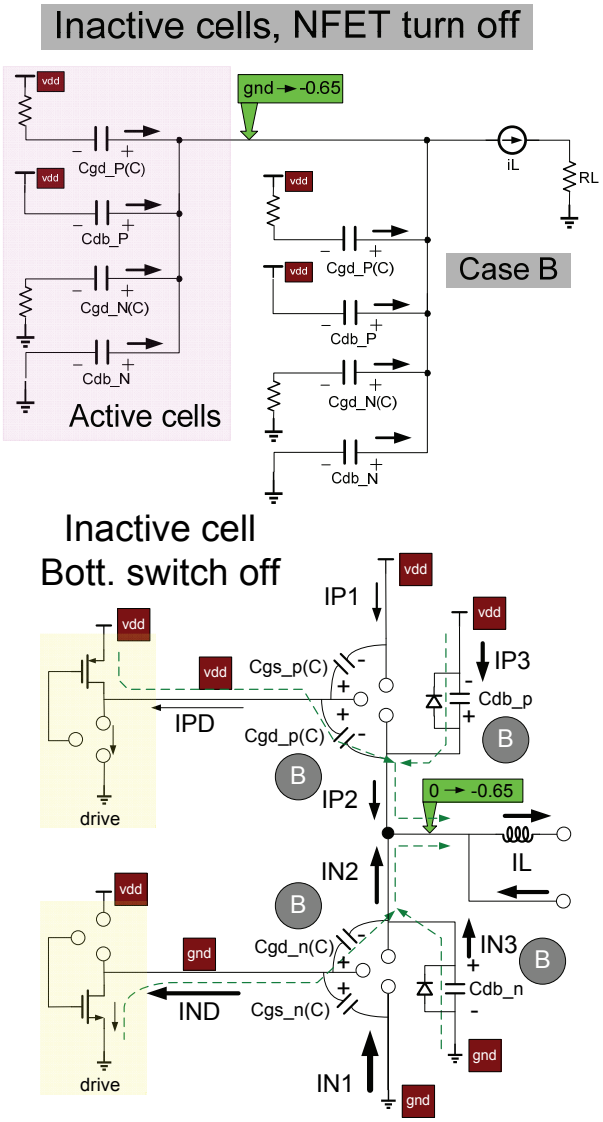


Figure 2-30 Inactive cells two sub-stages and C_loss classification when NFET turns off

Figure 2-30 illustrates the inactive power FET cells' two sub-stages and C_loss classification. Cgd_p(c), Cdb_p, Cgd_n(c) and Cdb_n all have the Case-B charging/discharging loops, so they have zero C_loss.

Table 2-1. ISBC unit width C_loss summary for active power FET subcells

Cap.	C_{gd_p}	C_{gs_p}	C_{db_p}	C_{gd_n}	C_{gs_n}	C_{db_n}
NFET Swi. off	0	0	0	$0.5C_{gd\_n}^{(L)}V_{dd}^2$	$0.5C_{gs\_n}^{(L)}V_{dd}^2$	0
PFET Swi. On	$0.5\left[C_{gd\_p}^{(C)}\left(V_{dd}+0.65\right)^2 + C_{gd\_p}^{(L)}V_{dd}^2\right]$	$0.5C_{gs\_p}^{(L)}V_{dd}^2$	$0.5C_{db\_p}$ $\left(V_{dd}+0.65\right)^2$	$0.5C_{gd\_n}^{(C)}$ $\left(V_{dd}^2+0.423\right)$	0	$0.5C_{db\_n}V_{dd}^2$ $+Err$
PFET Swi. Off	$0.5C_{gd\_p}^{(L)}V_{dd}^2$	$0.5C_{gs\_p}^{(L)}V_{dd}^2$	0	0	0	0
NFET Swi. on	0	0		$0.5\left[C_{gd\_n}^{(L)}V_{dd}^2 - C_{gd\_n}^{(C)}0.423\right]$	$0.5C_{gs\_n}^{(L)}V_{dd}^2$	Err
Total	$C_{gd\_p}^{(L)}V_{dd}^2+0.5C_{gd\_p}^{(C)}$ $\left(V_{dd}^2+1.3V_{dd}+0.423\right)$	$C_{gs\_p}^{(L)}V_{dd}^2$	$0.5C_{db\_p}$ $\left(V_{dd}^2+1.3V_{dd}+0.423\right)$	$C_{gd\_n}^{(L)}V_{dd}^2$ $+0.5C_{gd\_n}^{(C)}V_{dd}^2$	$C_{gs\_n}^{(L)}V_{dd}^2$	$0.5C_{db\_n}V_{dd}^2$ $+2Err$

Table. 2-2. ISBC unit width C_loss summary for inactive power FET subcells

Cap.	C_{gd_p}	C_{gs_p}	C_{db_p}	C_{gd_n}	C_{gs_n}	C_{db_n}
NFET Swi. off	0	0	0	0	0	0
PFET Swi. On	$0.5C_{gd\_p}^{(C)}\left(V_{dd}+0.65\right)^2$	0	$0.5C_{db\_p}$ $\left(V_{dd}+0.65\right)^2$	$0.5C_{gd\_n}^{(C)}$ $\left(V_{dd}^2+0.423\right)$	0	$0.5C_{db\_n}V_{dd}^2$ $+Err$
PFET Swi. Off	0	0	0	0	0	0
NFET Swi. on	0	0	0	$0.5C_{gd\_n}^{(C)}0.423$	0	Err
Total	$0.5C_{gd\_p}^{(C)}\left(V_{dd}+0.65\right)^2$	0	$0.5C_{db\_p}$ $\left(V_{dd}^2+1.3V_{dd}+0.423\right)$	$0.5C_{gd\_n}^{(C)}$ $\left(V_{dd}^2+0.845\right)$	0	$0.5C_{db\_n}V_{dd}^2$ $+2Err$

2.4.2.3 C_loss summary

The switching event based ISBC C_loss analysis results are summarized in Table 2-1 and Table 2-2 for the active power FET subcells and the inactive power FET subcells, respectively. On the basis of the unit width values in the Table 2-1 and Table 2-2, equations (2-56), (2-57), (2-58), (2-59), (2-60) and (2-61) further provide the total C_loss energy in each parasitic capacitor of an active power FET cell. At the same time, equations (2-62), (2-63), (2-64), (2-65), (2-66) and (2-67) provide the total C_loss energy for the inactive cells.

// Charging loss analysis for active cells. //

$$E_{C_{gd\_p}}^{active} = \left[V_{dd}^2\, C_{gd\_p}^{(L)} + 0.5\left(V_{dd}^2 + 1.3V_{dd} + 0.423\right)C_{gd\_p}^{(C)}\right]W_P^{active} \tag{2-56}$$

$$E_{C_{gs\_p}}^{active} = V_{dd}^2\, C_{gs\_p}^{(L)} W_P^{active} \tag{2-57}$$

$$E_{C_{db\_p}}^{active} = 0.5\left(V_{dd}^2 + 1.3V_{dd} + 0.423\right)C_{db\_p} W_P^{active} \tag{2-58}$$

$$E_{C_{gd\_n}}^{active} = V_{dd}^2\left[C_{gd\_n}^{(L)} + 0.5C_{gd\_n}^{(C)}\right]W_N^{active} \tag{2-59}$$

$$E_{C_{gs\_n}}^{active} = V_{dd}^2\, C_{gs\_n}^{(L)} W_N^{active} \tag{2-60}$$

$$E_{C_{db\_n}}^{active} = \left(0.5V_{dd}^2\, C_{db\_n} + 2E_{rr}\right)W_N^{active} \tag{2-61}$$

// Charging loss analysis for inactive cells. //

$$E_{C_{gd\_p}}^{inactive} = 0.5C_{gd\_p}^{(C)}\left(V_{dd} + 0.65\right)^2 \tag{2-62}$$

$$E_{C_{gs\_p}}^{inactive} = 0 \tag{2-63}$$

$$E_{C_{db\_p}}^{inactive} = 0.5\left(V_{dd}^2 + 1.3V_{dd} + 0.423\right)C_{db\_p} W_P^{inactive} \tag{2-64}$$

$$E_{C_{gd\_n}}^{inactive} = 0.5\left(V_{dd}^2 + 0.845\right)C_{gd\_n}^{(C)} W_N^{inactive} \tag{2-65}$$

$$E_{C_{gs\_n}}^{inactive} = 0 \tag{2-66}$$

$$E_{C_{db\_n}}^{inactive} = \left(0.5V_{dd}^2\, C_{db\_n} + 2E_{rr}\right)W_N^{inactive} \tag{2-67}$$

2.5 Capacitor energy variation hypothesis and parasitic capacitance extraction

To calculate the values of the aforementioned C_loss in subsection 2.4, we need extract the parasitic capacitance. Parasitic capacitances vary during a switching transient. C_{gd} and C_{gs} are determined by the operational mode of the power FET while C_{db} is V_{ds} dependent. There are many academic papers that focus on the development of an analytical expression reflecting the parameter dependence from the viewpoints of semiconductor physics. However, for a circuit designer, simpler equations which only require few parameters that are not difficult to extract from device models utilized in transistor level circuit simulation are preferable.

2.5.1 *Capacitor energy variation hypothesis*

The first challenge we will meet with is to determine the capacitor energy variation in a switching event, if the capacitance and the voltage drop across the capacitor simultaneously change during a switching event. We assume the capacitance and the voltage drop across the capacitor are respectively C_1 and V_1 before a switching event and the values are respectively C_2 and V_2 after a switching event. This variation is depicted in Figure 2-31.

The capacitor energy variation is evaluated with the equation in (2-68).

$$E = \int_{V_1}^{V_2} C(v)\, v\, dv \tag{2-68}$$

Complicated physics theories and models have to be involved [2-28] [2-29] [2-30] if we expect an accurate analysis, as the capacitance will change during a switching transient when the conduction mode of the MOSFET varies. However, we notice that

despite the effort expenditure for an accurate analysis, this does not mean that we can get a general solution satisfying all semiconductor technologies, fabrication processes and operation environments. One set of accurate physics models developed for one kind of technology might have to be significantly modified to work for another.

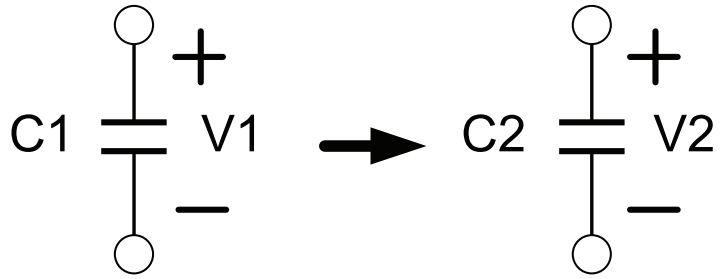


Figure 2-31. Capacitor energy variation in a switching transient

We propose a hypothesis that the capacitor energy variation in a switching event might be evaluated with the equation (2-69).

$$E = \int_{V_1}^{V_2} C(v)\, v\, dv = \begin{cases} \frac{1}{2}\left(C_2 V_2^2 - C_1 V_1^2\right) & sign(V_1) = sign(V_2) \\ \frac{1}{2}\left(C_2 V_2^2 + C_1 V_1^2\right) & sign(V_1) \neq sign(V_2) \end{cases} \tag{2-69}$$

We will verify the hypothesis with the simulation results obtained in BSIM3V3.1 level 49 model and Cadence Spice simulator. We first extract parasitic capacitances with one set of data measured in one operation condition, then compare the difference encountered in other operation conditions between the measured data and the calculated values on the basis of the extracted capacitances. This kind of process will be applied to all parasitic capacitances' four different switching events in a synchronous Buck converter. For the ease of comparison and showing the difference, $\pm 20\%$ error bars will be depicted in all figures and the error bars take the calculated data as the center point.

We assume that $MPoff < 0$ is satisfied via design so that there is no Miller plateau in the PFET turn-off event.

2.5.2 *Capacitance extraction*

AMI06 is a standard CMOS technology, so the device is symmetrical. The parasitic capacitances for extraction are investigated with the equations [2-1]. In this dissertation, several unit width variables will be introduced for the feasibility of capacitance extraction, which include K_{GDO}, K_{ox} K_{db}^{1}, K_{db}^{2} and K_{rr}. The relation between the variables and the unit parasitic capacitance are given in (2-70), (2-71), (2-72), (2-73), (2-74) and (2-75).

$$C_{gd}^{(C)} = C_{gd}^{(C)} = C_{gdo}W = C_{gso}W = K_{GDO}W \tag{2-70}$$

$$C_{gd}^{(S)} = C_{gd}^{(C)} = K_{GDO}W \tag{2-71}$$

$$C_{gs}^{(S)} = C_{gs}^{(C)} + \frac{2}{3} C_{ox} W L_{eff} = \left(K_{GDO} + \frac{2}{3} K_{ox} \right) W \tag{2-72}$$

$$C_{gd}^{(L)} = C_{gs}^{(L)} = C_{gd}^{(C)} + \frac{1}{2} C_{ox} W L_{eff} = \left(K_{GDO} + \frac{1}{2} K_{ox} \right) W \tag{2-73}$$

$$C_{db} = \frac{K_{db}^{1} W}{\sqrt{K_{db}^{2} + V_{dd}}} \tag{2-74}$$

$$E_{rr} = K_{rr}W \tag{2-75}$$

Thus, parasitic capacitance extraction is in fact the extraction of unit width variables including K_{GDO_P}, K_{GDO_N}, K_{ox_P}, K_{ox_N}, $K_{db\_P}^{1}$, $K_{db\_P}^{2}$, $K_{db\_N}^{1}$, $K_{db\_N}^{2}$, and K_{rr}. In order to obtain the unit width variable, all measured energy variation data will be divided by the corresponding FET width. From now on, all of the mentioned energy in this section implicitly refers to the unit energy.

The operation conditions for capacitance extraction are described in Table 2-3.

Table 2-3. Working condition of ISBC for parasitic capacitance extraction

Vdd	***Temp.***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
2.4V-3.6V	100°C	TT	0.4A	80%	20%	0.037	0.0247

The circuit schematic for parasitic capacitance extraction is depicted in Figure 2-32.

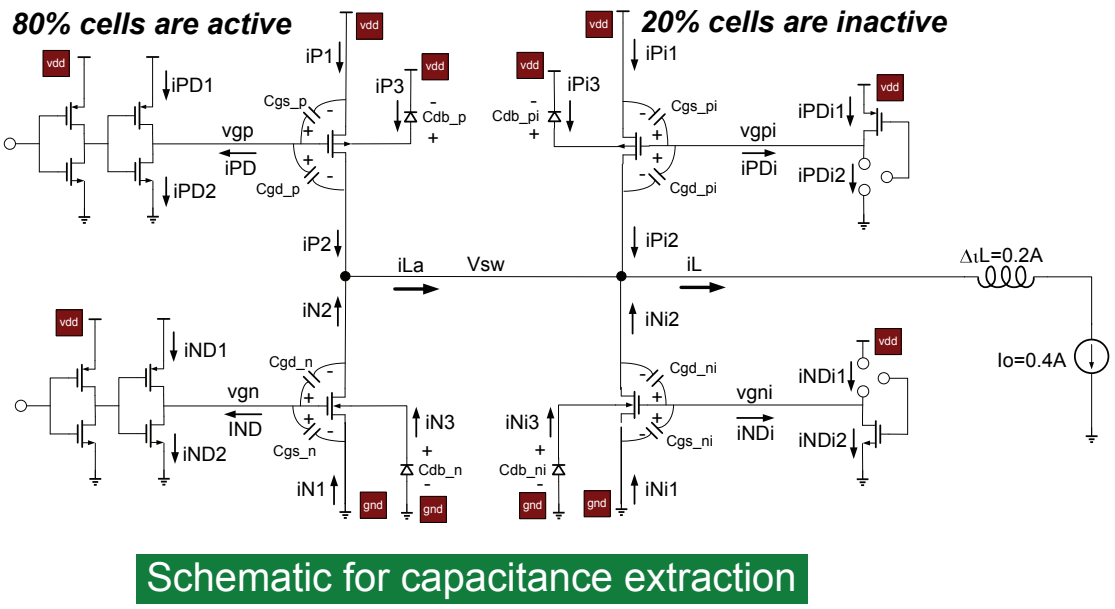


Figure 2-32. The ISBC schematic for capacitance extraction

To simplify the expression, the four switching events are labeled in time sequence as case 1 – NFET turn-off, case 2 – PFET turn-on, case 3 – PFET turn-off and case 4 – NFET turn-on. Figure 2-33 shows the sequence of the four cases.

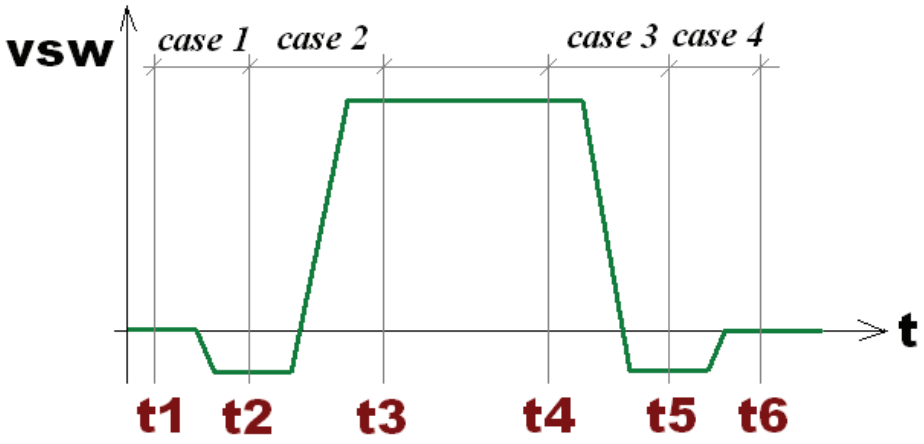


Figure 2-33. Four switching events labeled in time sequence.

2.5.2.1 K_{db}

Energy variation data relative to K_{db} is measured by the time integration of current and voltage given in the following equations. All symbols are shown in Figure 2-32.

$$E_{db\_P}^{case\_1\_active} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_1}^{t_2}\left|\, i_{P3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{active}} \tag{2-76}$$

$$E_{db\_P}^{case\_2\_active} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left(V_{dd}+0.65\right)^2 = \frac{\int_{t_2}^{t_3}\left|\, i_{P3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{active}} \tag{2-77}$$

$$E_{db\_P}^{case\_3\_active} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left(V_{dd}+0.65\right)^2 = \frac{\int_{t_4}^{t_5}\left|\, i_{P3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{active}} \tag{2-78}$$

$$E_{db\_P}^{case\_4\_active} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_5}^{t_6}\left|\, i_{P3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{active}} \tag{2-79}$$

$$E_{db\_P}^{case\_1\_inactive} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_1}^{t_2}\left|\, i_{Pi3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{inactive}} \tag{2-80}$$

$$E_{db\_P}^{case\_2\_inactive} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left(V_{dd}+0.65\right)^2 = \frac{\int_{t_2}^{t_3}\left|\, i_{Pi3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{inactive}} \tag{2-81}$$

$$E_{db\_P}^{case\_3\_inactive} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left(V_{dd}+0.65\right)^2 = \frac{\int_{t_4}^{t_5}\left|\, i_{Pi3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{inactive}} \tag{2-82}$$

$$E_{db\_P}^{case\_4\_inactive} = 0.5\frac{K_{db\_P}^{1}}{\sqrt{K_{db\_P}^{2}+V_{dd}}}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_5}^{t_6}\left|\, i_{Pi3}\left(V_{dd}-V_{SW}\right)\right| dt}{W_P^{inactive}} \tag{2-83}$$

$$E_{db\_N}^{case\_1\_active} = K_{rr} = \frac{\int_{t_1}^{t_2}\left|\, i_{N3}V_{SW}\,\right| dt}{W_N^{active}} \tag{2-84}$$

$$E_{db\_N}^{case\_2\_active} = K_{rr} + 0.5\frac{K_{db\_N}^{1}}{\sqrt{K_{db\_N}^{2} + V_{dd}}} V_{dd}^{2} = \frac{\int_{t_2}^{t_3} \left| i_{N3} V_{SW} \right| dt}{W_N^{active}} \tag{2-85}$$

$$E_{db\_N}^{case\_3\_active} = K_{rr} + 0.5\frac{K_{db\_N}^{1}}{\sqrt{K_{db\_N}^{2} + V_{dd}}} V_{dd}^{2} = \frac{\int_{t_4}^{t_5} \left| i_{N3} V_{SW} \right| dt}{W_N^{active}} \tag{2-86}$$

$$E_{db\_N}^{case\_4\_active} = K_{rr} = \frac{\int_{t_5}^{t_6} \left| i_{N3} V_{SW} \right| dt}{W_N^{active}} \tag{2-87}$$

$$E_{db\_N}^{case\_1\_inactive} = K_{rr} = \frac{\int_{t_1}^{t_2} \left| i_{Ni3} V_{SW} \right| dt}{W_N^{inactive}} \tag{2-88}$$

$$E_{db\_N}^{case\_2\_inactive} = K_{rr} + 0.5\frac{K_{db\_N}^{1}}{\sqrt{K_{db\_N}^{2} + V_{dd}}} V_{dd}^{2} = \frac{\int_{t_2}^{t_3} \left| i_{Ni3} V_{SW} \right| dt}{W_N^{inactive}} \tag{2-89}$$

$$E_{db\_N}^{case\_3\_inactive} = K_{rr} + 0.5\frac{K_{db\_N}^{1}}{\sqrt{K_{db\_N}^{2} + V_{dd}}} V_{dd}^{2} = \frac{\int_{t_4}^{t_5} \left| i_{Ni3} V_{SW} \right| dt}{W_N^{inactive}} \tag{2-90}$$

$$E_{db\_N}^{case\_4\_inactive} = K_{rr} = \frac{\int_{t_5}^{t_6} \left| i_{Ni3} V_{SW} \right| dt}{W_N^{active}} \tag{2-91}$$

K_{db} is able to be extracted in all cases. In the situation, we notice that the capacitor energy variation in PFET switching cases (case 2 and 3) is much larger than that in NFET switching cases (case 1 and 4) for both power PFET and power NFET. For the case of the power PFET, the energy variation in the case 2 or case 3 is the multiplication of capacitance by $\left(V_{dd} + 0.65\right)^2$ but that in the case 1 or case 4 is the multiplication of the identical capacitance by $\left(1.3V_{dd} + 0.425\right)$. For the case of power NFET, the energy variation in the case 2 or case 3 includes the multiplication of capacitance by V_{dd}^2 and the reverse recovery energy K_{rr} but the energy variation in the case 1 or case 4 is only equal

to the reverse recovery energy K_{rr}. After noticing the difference, we take the average value of eight sets of energy variation data measured in case 2 and 3 for both active and inactive cells and utilize the average value to extract coefficients. After obtaining the coefficients, we use the coefficients to emulate the energy variation in case 1 and 4 and observe the error between the measured data and the emulated data.

The normalized energy data measured for PFET in the case 2 and 3 and the emulated data with the extracted coefficients are depicted in Figure 2-34. The corresponding data for NFET are depicted in Figure 2-35. The extracted values are respectively listed as:

$$K^1_{db\_P} = 2.4062\times10^{-9}\ F\cdot V^{1/2}\cdot m^{-1},\ K^2_{db\_P} = 1.5334 V^{1/2}; \tag{2-92}$$

$$K^1_{db\_N} = 3.3486\times10^{-9}\ F\cdot V^{1/2}\cdot m^{-1},\ K^2_{db\_N} = 9.5271 V^{1/2}; \tag{2-93}$$

$$K_{rr} = 4.8521\times10^{-10}\ J\cdot m^{-1}. \tag{2-94}$$

The normalized energy data measured for the PFET in the case 1 and 4 and the emulated data with the extracted coefficients are depicted in Figure 2-36. The corresponding data sets for the NFET are depicted in Figure 2-37.

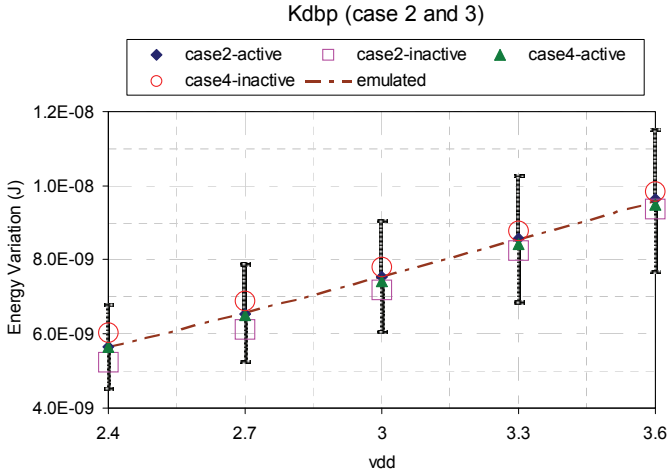


Figure 2-34. K_{db_P} related unit energy in the work condition for extraction (case 2 and 3)

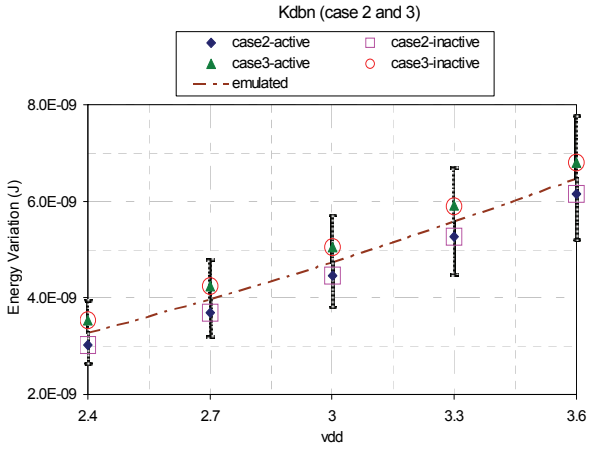


Figure 2-35. K_{db_N} related unit energy in the work condition for extraction (case2 and 3)

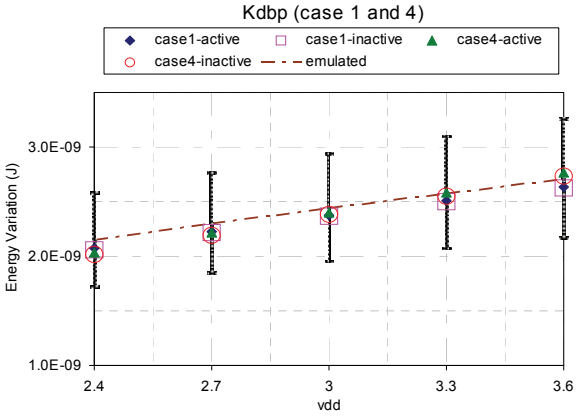


Figure 2-36. K_{db_P} related unit energy in the work condition for extraction (case1 and 4)

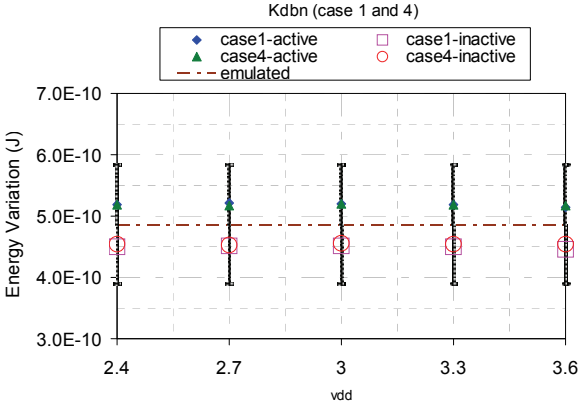


Figure 2-37. K_{db_N} related unit energy in the work condition for extraction (case1 and 4)

2.5.2.2 K_{GDO}

Energy variation data relative to K_{GDO} is measured in the schematic with the equations,

$$E_{GDO\_P}^{case\_1\_active} = 0.5K_{GDO\_P}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_1}^{t_2}\left| i_{PD}\left(V_{gP}-V_{SW}\right)\right| dt}{W_P^{active}} \quad (2\text{-}95)$$

$$E_{GDO\_P}^{case\_4\_active} = 0.5K_{GDO\_P}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_5}^{t_6}\left| i_{PD}\left(V_{gP}-V_{SW}\right)\right| dt}{W_P^{active}} \quad (2\text{-}96)$$

$$E_{GDO\_P}^{case\_1\_inactive} = 0.5K_{GDO\_P}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_1}^{t_2}\left| i_{PDi}\left(V_{gPi}-V_{SW}\right)\right| dt}{W_P^{inactive}} \quad (2\text{-}97)$$

$$E_{GDO\_P}^{case\_2\_inactive} = 0.5K_{GDO\_P}\left(V_{dd}+0.65\right)^2 = \frac{\int_{t_2}^{t_3}\left| i_{PDi}\left(V_{gPi}-V_{SW}\right)\right| dt}{W_P^{inactive}} \quad (2\text{-}98)$$

$$E_{GDO\_P}^{case\_3\_inactive} = 0.5K_{GDO\_P}\left(V_{dd}+0.65\right)^2 = \frac{\int_{t_4}^{t_5}\left| i_{PDi}\left(V_{gPi}-V_{SW}\right)\right| dt}{W_P^{inactive}} \quad (2\text{-}99)$$

$$E_{GDO\_P}^{case\_4\_inactive} = 0.5K_{GDO\_P}\left[\left(V_{dd}+0.65\right)^2 - V_{dd}^2\right] = \frac{\int_{t_5}^{t_6}\left| i_{PDi}\left(V_{gPi}-V_{SW}\right)\right| dt}{W_P^{inactive}} \quad (2\text{-}100)$$

$$E_{GDO\_N}^{case\_2\_active} = 0.5K_{GDO\_N}\left(V_{dd}^2+0.423\right) = \frac{\int_{t_2}^{t_3}\left| i_{ND}\left(V_{gN}-V_{SW}\right)\right| dt}{W_N^{active}} \quad (2\text{-}101)$$

$$E_{GDO\_N}^{case\_3\_active} = 0.5K_{GDO\_N}\left(V_{dd}^2+0.423\right) = \frac{\int_{t_4}^{t_5}\left| i_{ND}\left(V_{gN}-V_{SW}\right)\right| dt}{W_N^{active}} \quad (2\text{-}102)$$

$$E_{GDO\_N}^{case\_1\_inactive} = 0.5K_{GDO\_N}0.423 = \frac{\int_{t_1}^{t_2}\left| i_{NDi}\left(V_{gNi}-V_{SW}\right)\right| dt}{W_N^{inactive}} \quad (2\text{-}103)$$

$$E_{GDO\_N}^{case\_2\_inactive} = 0.5K_{GDO\_N}\left(V_{dd}^2+0.423\right) = \frac{\int_{t_2}^{t_3}\left| i_{NDi}\left(V_{gNi}-V_{SW}\right)\right| dt}{W_N^{inactive}} \quad (2\text{-}104)$$

$$E_{db\_N}^{case\_3\_inactive} = 0.5K_{GDO\_N}\left(V_{dd}^2 + 0.423\right) = \frac{\int_{t_4}^{t_5}\left| i_{NDi}\left(V_{gNi} - V_{SW}\right)\right| dt}{W_N^{inactive}} \quad (2\text{-}105)$$

$$E_{db\_N}^{case\_4\_inactive} = 0.5K_{GDO\_N}0.423 = \frac{\int_{t_5}^{t_6}\left| i_{NDi}\left(V_{gNi} - V_{SW}\right)\right| dt}{W_N^{active}} \quad (2\text{-}106)$$

K_{GDO} is different from K_{db}, as its measurability in all cases is only available for the inactive cells. For active cells, the measurability is only available in two cases. Furthermore, K_{GDO} is the coefficient which is most difficult to extract, because its value is very small and the measurement data is easily polluted by charge sharing effects due to coupled parasitic capacitors during node voltage oscillation.

To improve the creditability of the coefficient extraction, we average the energy data relative to K_{GDO_P} in case 1 and 4 for both active and inactive cells to extract K_{GDO_P}, and average the energy data relative to K_{GDO_N} in case 2 and 3 for both active and inactive cells to extract K_{GDO_N}. The reason is that we found in those cases the measured data is very close as illustrated in Figure 2-39 and Figure 2-40. On the contrary, when we investigated the unit energy measured in other cases (case 2 and 3 for an inactive PFET, case 1 and 4 for an inactive NFET), we observed significant deviation as illustrated in Figure 2-38 and Figure 2-41.

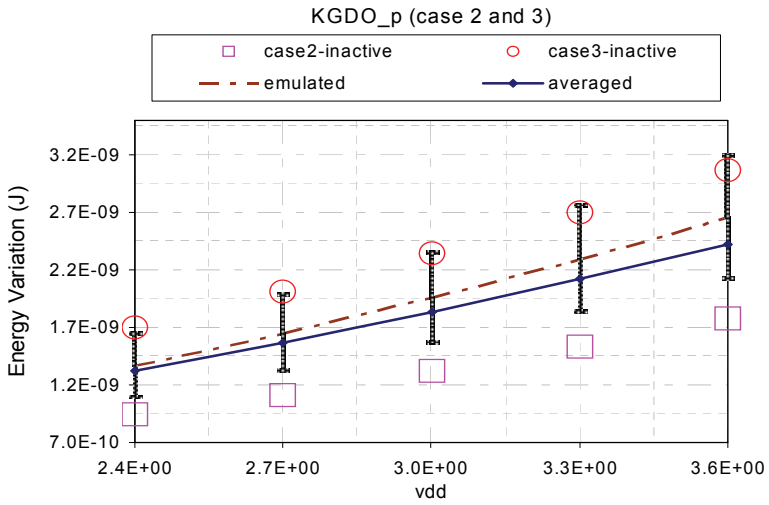


Figure 2-38. K_{GDO_P} related unit energy in the work condition for extraction (case2 and 3)

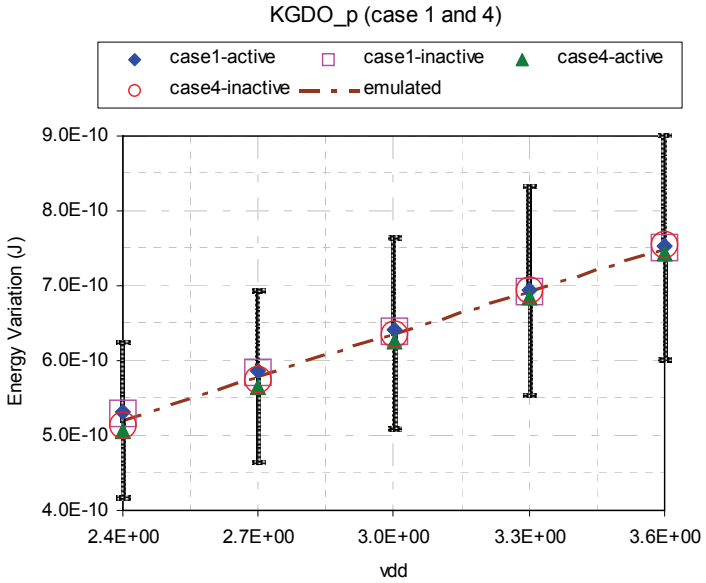


Figure 2-39 K_{GDO_P} related unit energy in the work condition for extraction (case1 and 4)

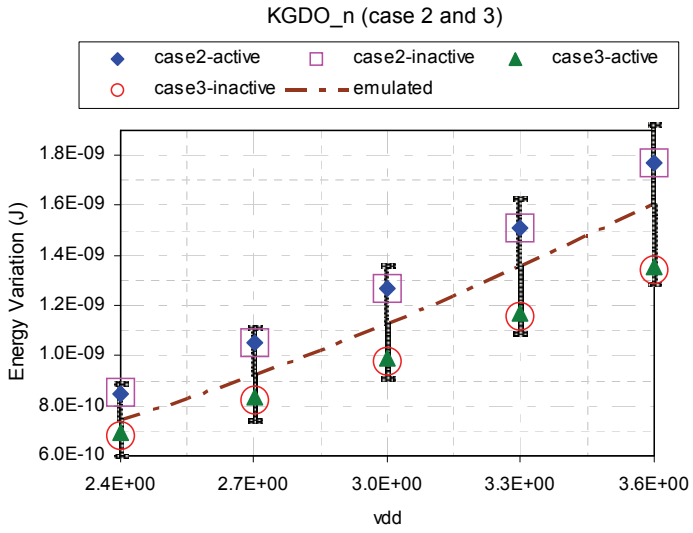


Figure 2-40. K_{GDO_N} related unit energy in the work condition for extraction (case2 and 3)

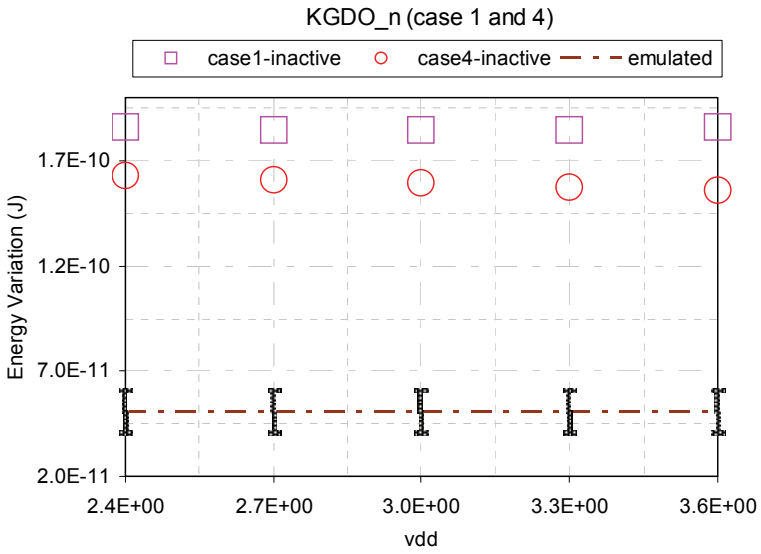


Figure 2-41. K_{GDO_P} related unit energy in the work condition for extraction (case1 and 4)

The extracted values are respectively:

$$K_{GDO\_P} = 2.9376\times10^{-10};\ K_{GDO\_N} = 2.3924\times10^{-10};\qquad (2\text{-}107)$$

Despite that the data errors in Figure 2-38 and Figure 2-41 are out of the $\pm 20\%$ error range, two reasons favor the hypothesis. The first reason is that in Figure 2-38 the average energy values are in $\pm 20\%$ error range and the average energy values are what we are interested in. The second reason is that the energy scale in Figure 2-36 is remarkably smaller than others making its impact negligible.

2.5.2.3 K_{ox}

Energy variation data relative to K_{ox} are measured in the schematic with the equations,

$$E_{ox\_P}^{case\_3\_active} = 0.5\left[\left(K_{ox\_P} + 2K_{GDO\_P}\right)V_{dd}^2 + K_{GDO\_P}\left(V_{dd} + 0.65\right)^2\right] = \frac{\int_{t_4}^{t_5}\left| i_{PD}\left(V_{gP} - V_{SW}\right)\right| dt}{W_P^{active}} \tag{2-108}$$

$$E_{ox\_P}^{case\_4\_active} = 0.5\left[\left(K_{ox\_N} + 2K_{GDO\_N}\right)V_{dd}^2 + K_{GDO\_N}\ 0.65^2\right] = \frac{\int_{t_5}^{t_6}\left| i_{ND}\left(V_{gN} - V_{SW}\right)\right| dt}{W_N^{active}} \tag{2-109}$$

From the analysis in this section, the active cells' PMOS turn-off is a good case for the extraction of coefficient K_{ox_P} ($C_{gd\_P}^{(L)}$ and $C_{gs\_P}^{(L)}$) when the Miller plateau is eliminated. For K_{ox_P}, the case 4 is a better candidate than the case 1 for coefficient extraction, as in the former one the body diode of the NFET conducts forward recovery while in the latter the body diode conducts reverse recovery. The data sets are depicted in Figure 2-42 and Figure 2-43.

The extracted values are respectively:

$$K_{ox\_P} = 1.2005 \times 10^{-9};\ K_{ox\_N} = 1.2335 \times 10^{-9}; \tag{2-110}$$

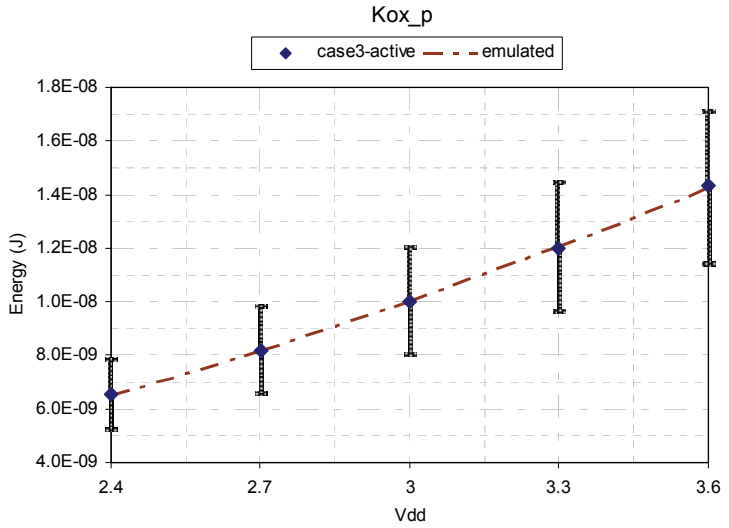


Figure 2-42. K_{ox_P} related unit energy in the work condition for extraction (case3)

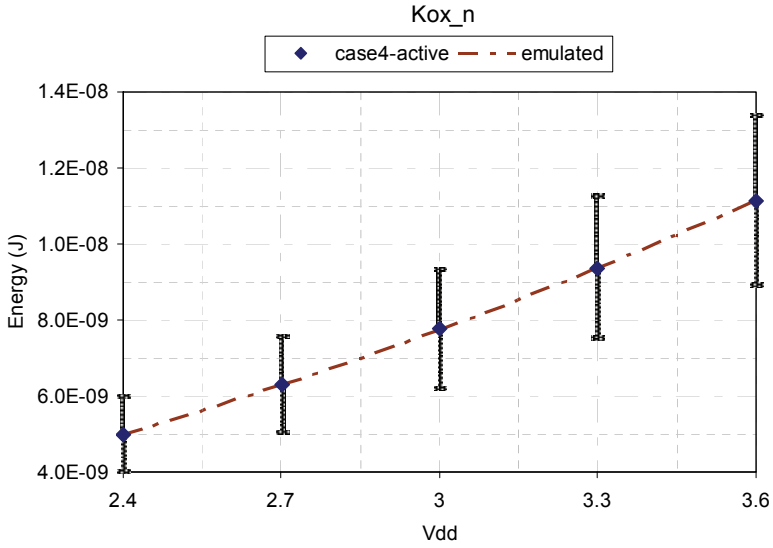


Figure 2-43. K_{ox_N} related unit energy in the work condition for extraction (case 4)

2.5.3 *Hypothesis verification*

We apply twelve different kinds of operation conditions to verify the hypothesis about the capacitor energy variation in the subsection 2.5.1. The conditions utilized for the verification are listed in Table 2-4.

Table 2-4. Working conditions of ISBC for hypothesis verification

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V1	100°C	TT	0.25A	80%	20%	0.037	0.0247
V2	100°C	TT	0.1A	80%	20%	0.037	0.0247
V3	100°C	TT	0.4A	50%	50%	0.037	0.0247
V4	100°C	TT	0.4A	20%	80%	0.037	0.0247
V5	100°C	FF	0.4A	80%	20%	0.037	0.0247
V6	100°C	FS	0.4A	80%	20%	0.037	0.0247
V7	100°C	SF	0.4A	80%	20%	0.037	0.0247
V8	100°C	SS	0.4A	80%	20%	0.037	0.0247
V9	50°C	TT	0.4A	80%	20%	0.037	0.0247
V10	0°C	TT	0.4A	80%	20%	0.037	0.0247
V11	100°C	TT	0.1A	50%	50%	0.037	0.0247
V12	100°C	TT	0.4A	80%	20%	0.03	0.01

2.5.3.1 Verification case 1

Table 2-5. First verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V1	100°C	TT	***0.25A***	80%	20%	0.037	0.0247

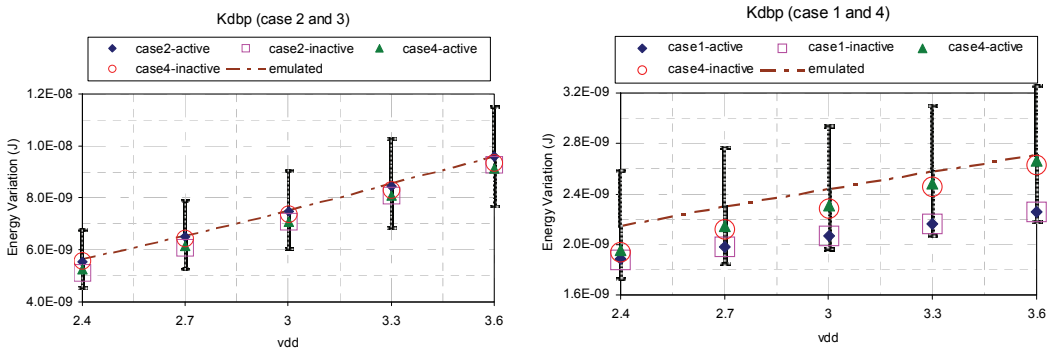


Figure 2-44. K_{db_P} related unit energy in 1st working condition for hypothesis verification

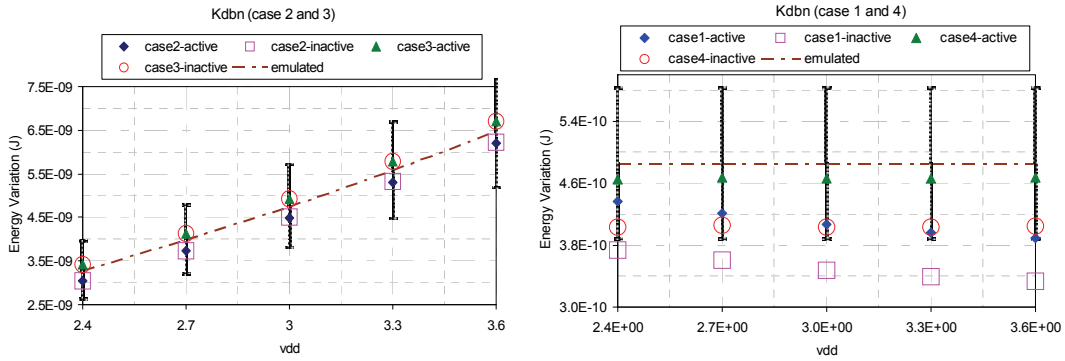


Figure 2-45. K_{db_N} related unit energy in 1st working condition for hypothesis verification

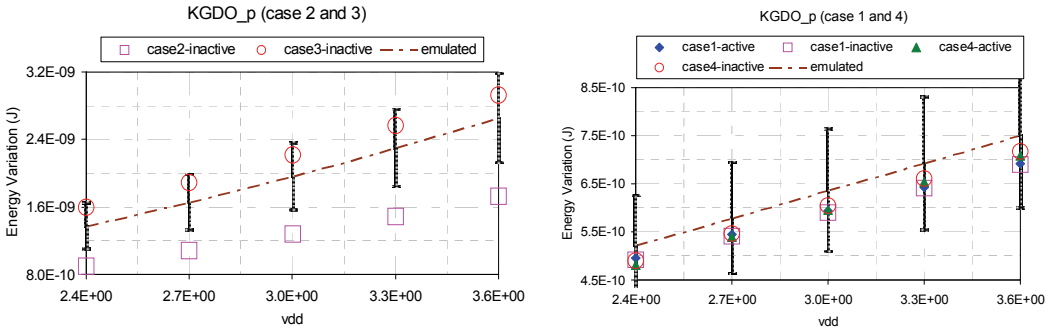


Figure 2-46. K_{GDO_P} related unit energy in 1st working condition for hypothesis verification

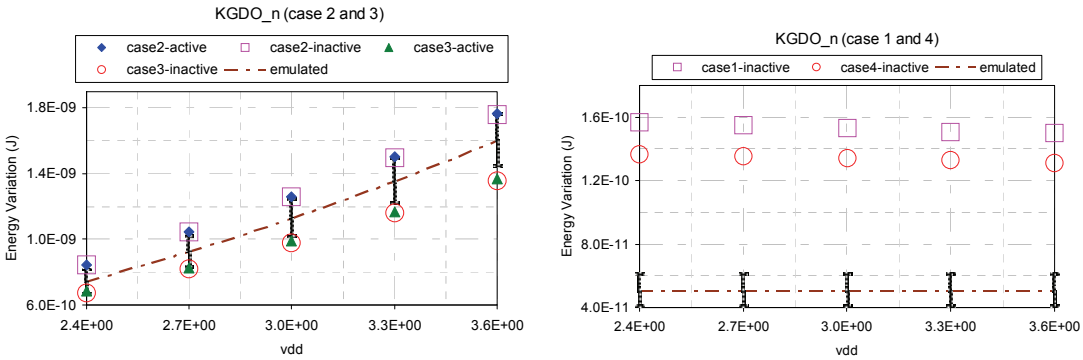


Figure 2-47. K_{GDO_N} related unit energy in 1st working condition for hypothesis verification

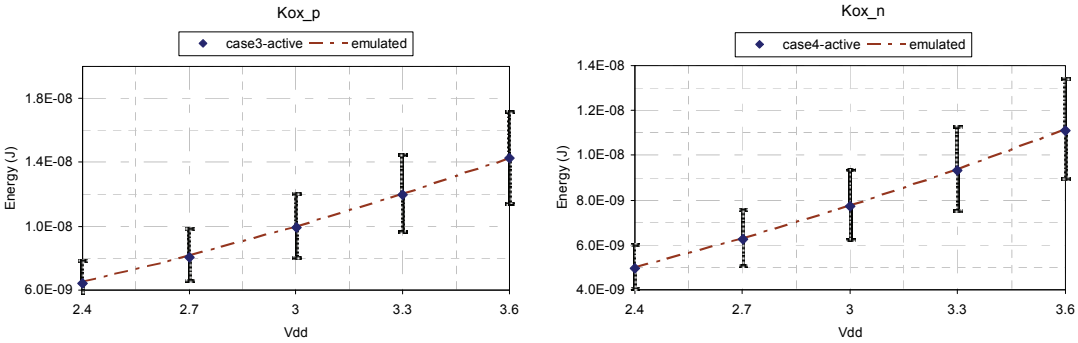


Figure 2-48. K_{ox} related unit energy in 1st working condition for hypothesis verification

2.5.3.2 Verification case 2

Table 2-6. Second verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V2	100°C	TT	***0.1A***	80%	20%	0.037	0.0247

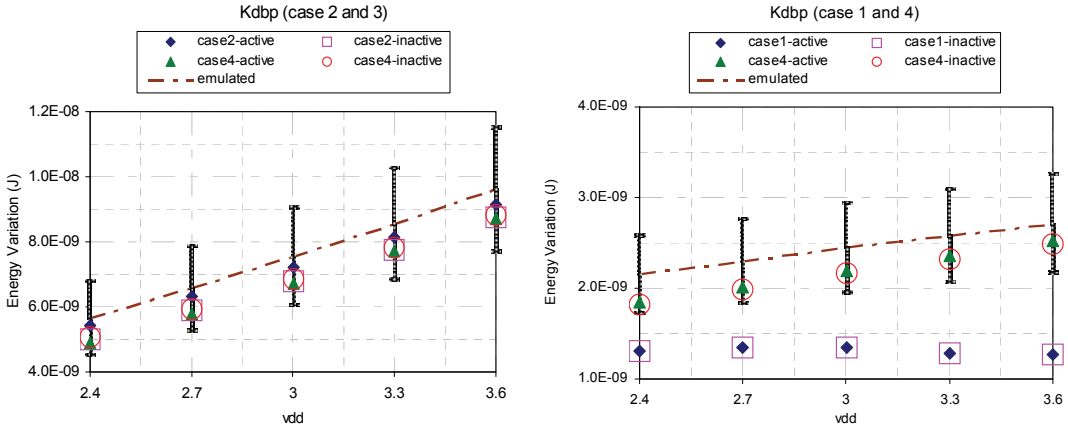


Figure 2-49. K_{db_P} related unit energy in 2nd working condition for hypothesis verification

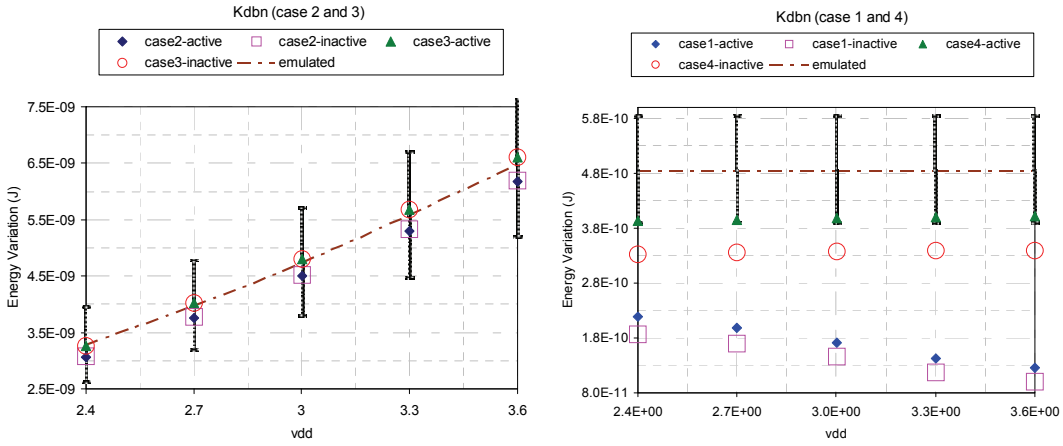


Figure 2-50. K_{db_N} related unit energy in 2nd working condition for hypothesis verification

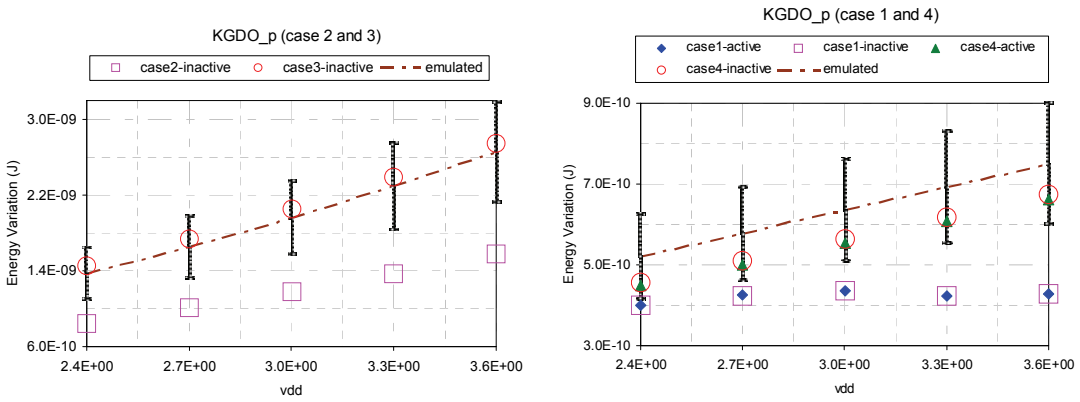


Figure 2-51. K_{GDO_P} related unit energy in 2nd working condition for hypothesis verification

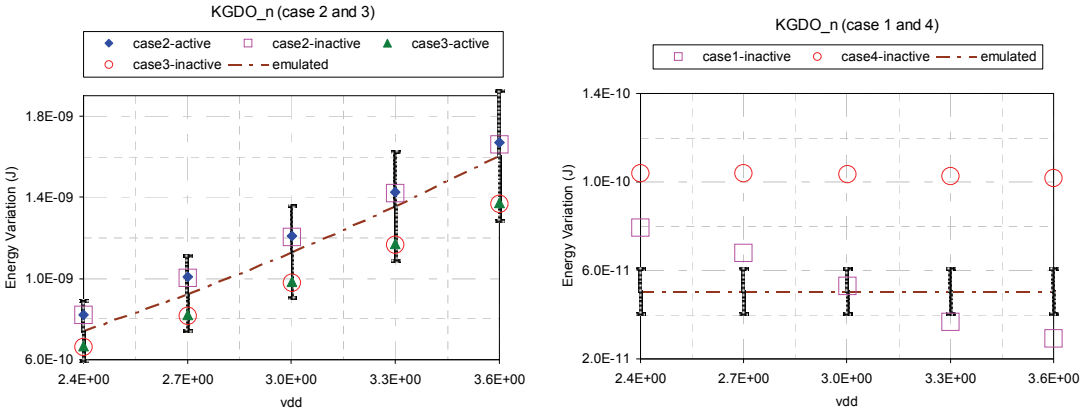


Figure 2-52. K_{GDO_N} related unit energy in 2nd working condition for hypothesis verification

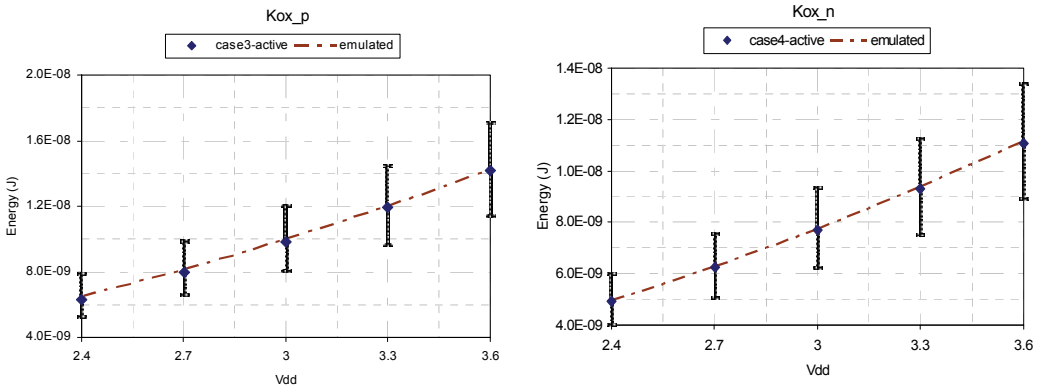


Figure 2-53. K_{ox} related unit energy in 2nd working condition for hypothesis verification

2.5.3.3 Verification case 3

Table 2-7. Third verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V3	100°C	TT	0.4A	***50%***	***50%***	0.037	0.0247

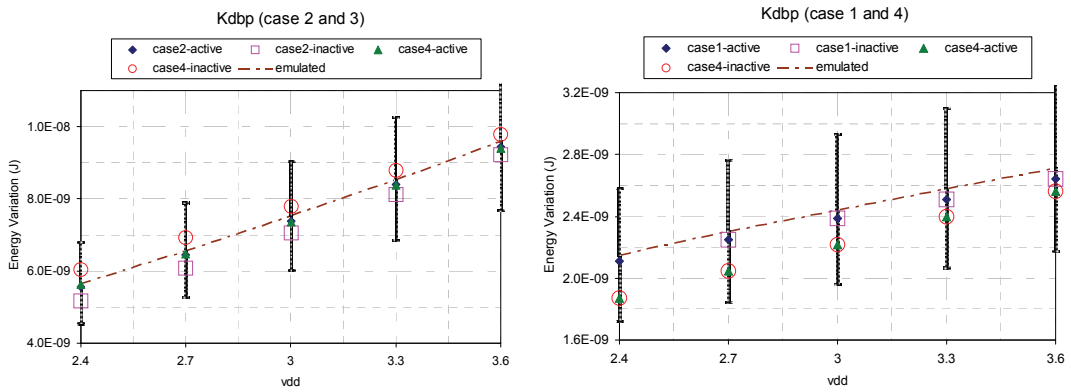


Figure 2-54. K_{db_P} related unit energy in 3rd working condition for hypothesis verification

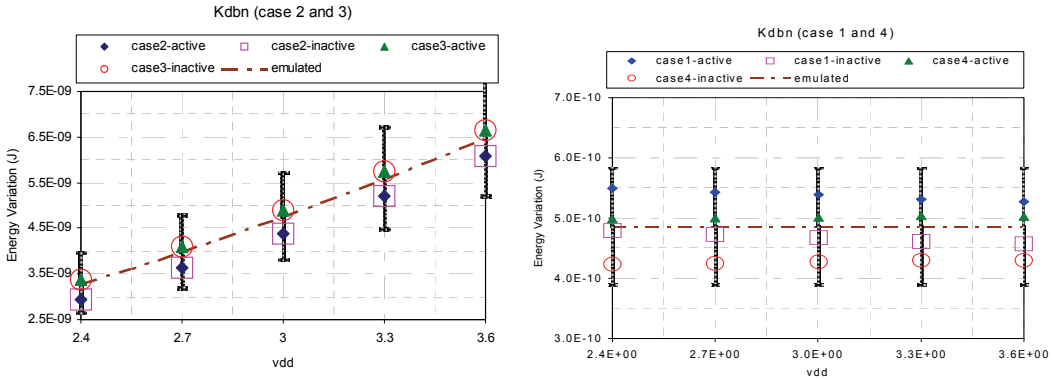


Figure 2-55. K_{db_N} related unit energy in 3rd working condition for hypothesis verification

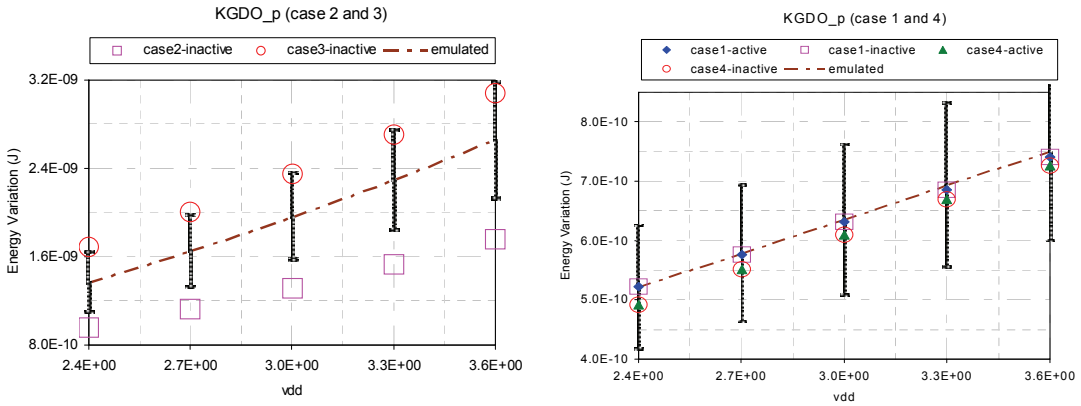


Figure 2-56. K_{GDO_P} related unit energy in 3rd working condition for hypothesis verification

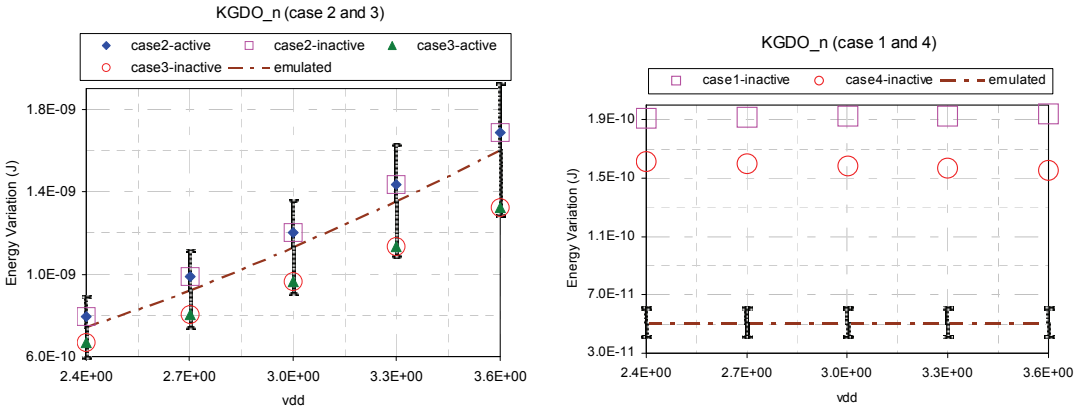


Figure 2-57. K_{GDO_N} related unit energy in 3rd working condition for hypothesis verification

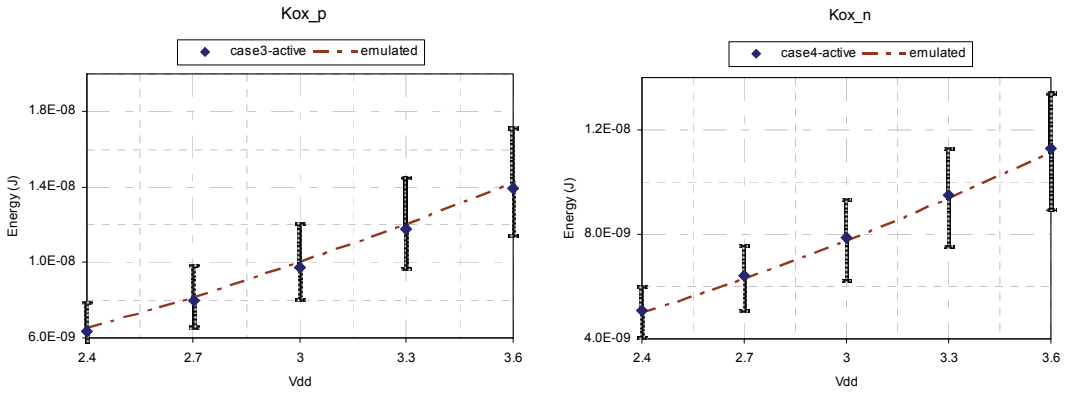


Figure 2-58. K_{ox} related unit energy in 3rd working condition for hypothesis verification

2.5.3.4 Verification case 4

Table 2-8. Forth verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V4	100°C	TT	0.4A	***20%***	***80%***	0.037	0.0247

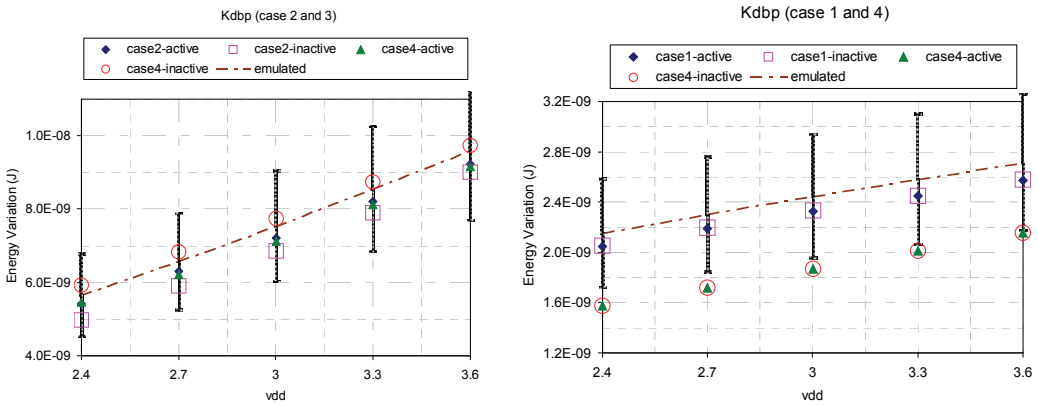


Figure 2-59. K_{db_P} related unit energy in 4th working condition for hypothesis verification

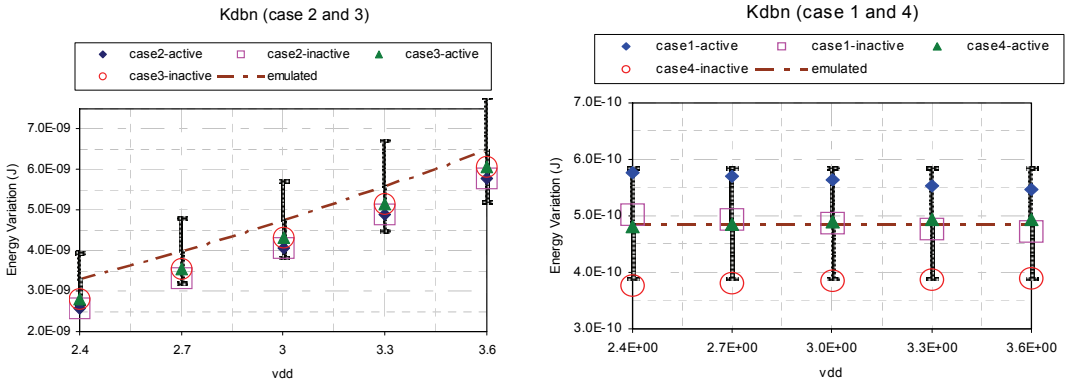


Figure 2-60. K_{db_N} related unit energy in 4th working condition for hypothesis verification

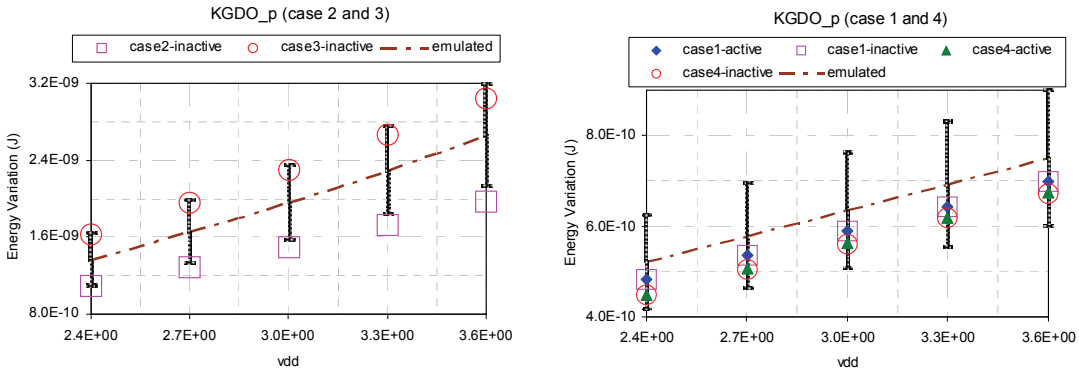


Figure 2-61. K_{GDO_P} related unit energy in 4th working condition for hypothesis verification

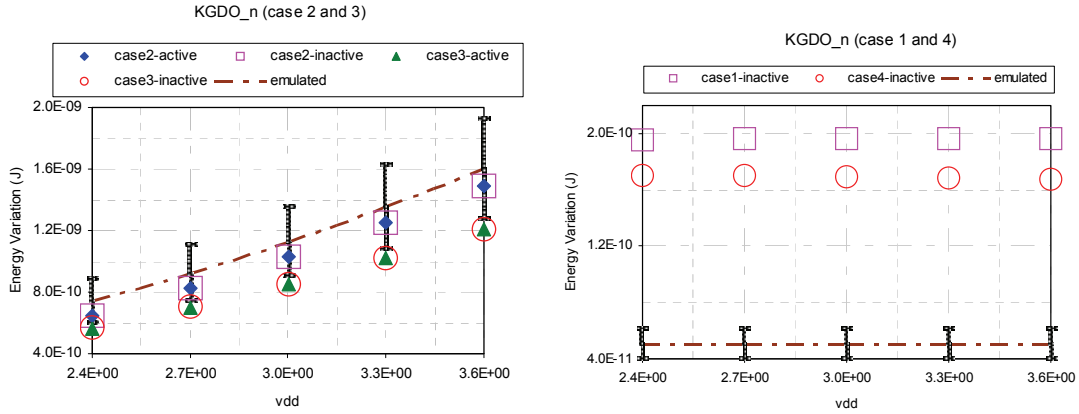


Figure 2-62. K_{GDO_N} related unit energy in 4th working condition for hypothesis verification

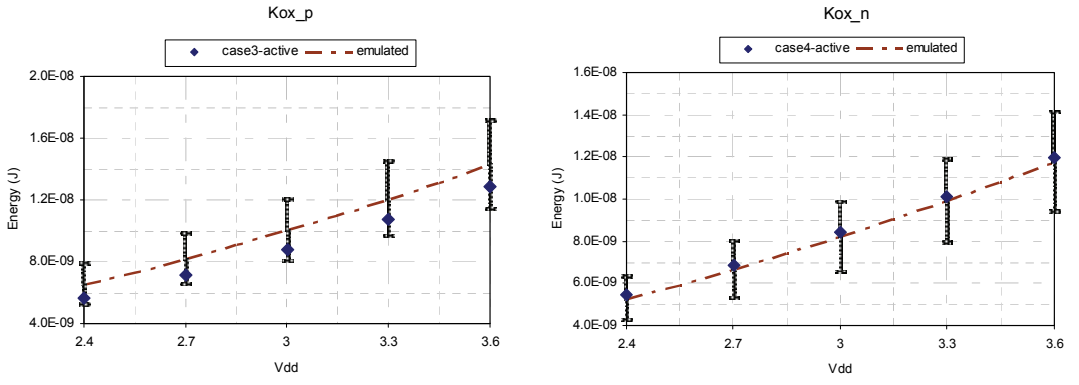


Figure 2-63. K_{ox} related unit energy in 4th working condition for hypothesis verification

2.5.3.5 Verification case 5

Table 2-9. Fifth verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V5	100°C	***FF***	0.4A	80%	20%	0.037	0.0247

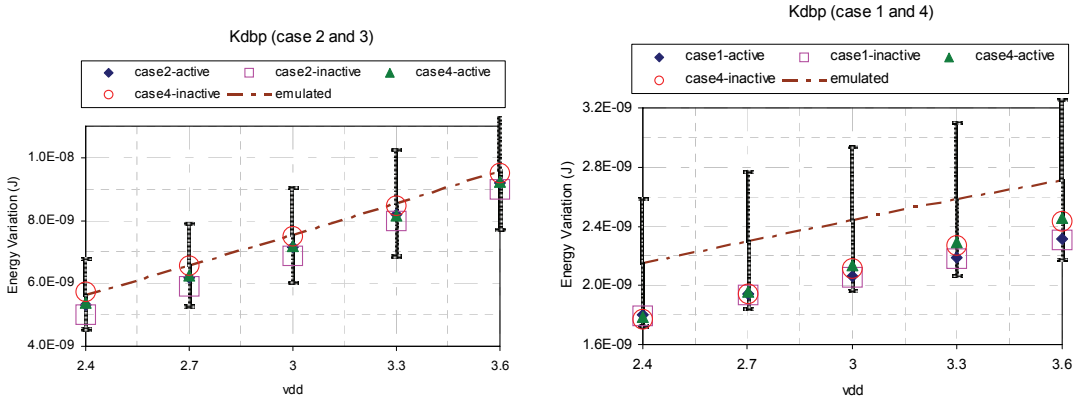


Figure 2-64. K_{db_P} related unit energy in 5th working condition for hypothesis verification

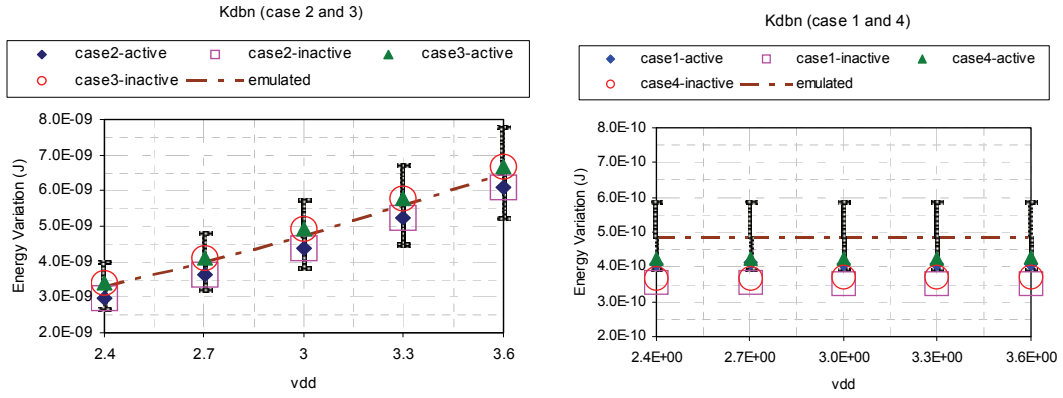


Figure 2-65. K_{db_N} related unit energy in 5th working condition for hypothesis verification

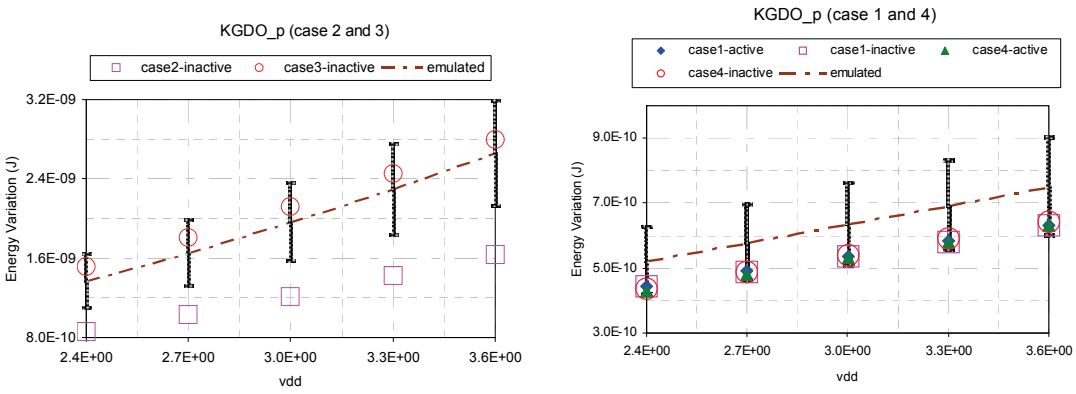


Figure 2-66. K_{GDO_P} related unit energy in 5th working condition for hypothesis verification

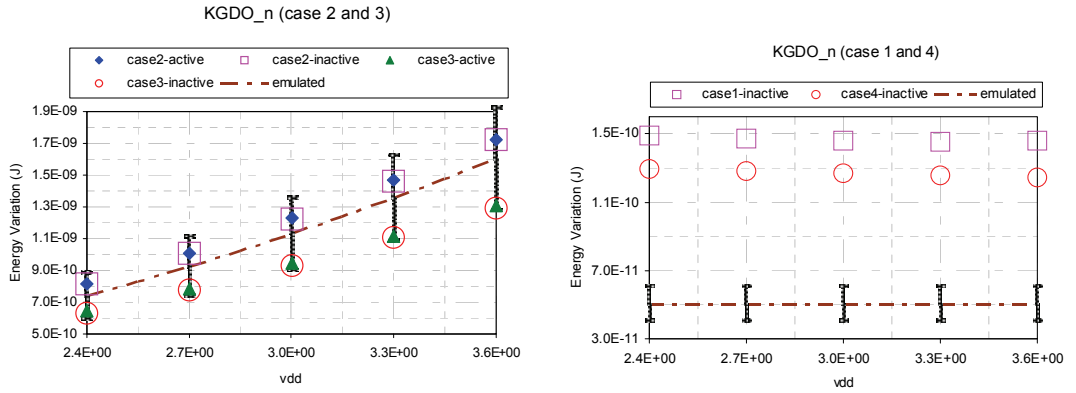


Figure 2-67. K_{GDO_N} related unit energy in 5th working condition for hypothesis verification

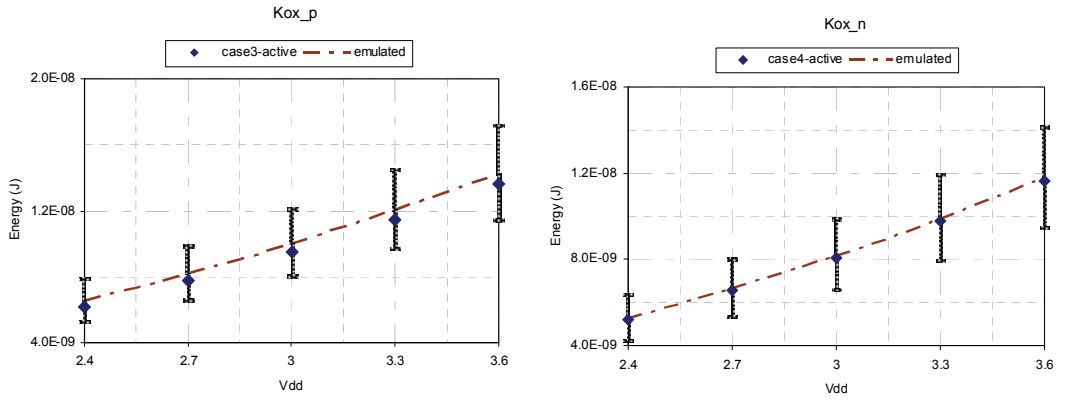


Figure 2-68. K_{ox} related unit energy in 5th working condition for hypothesis

2.5.3.6 Verification case 6

Table 2-10. Sixth verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V6	100°C	***FS***	0.4A	80%	20%	0.037	0.0247

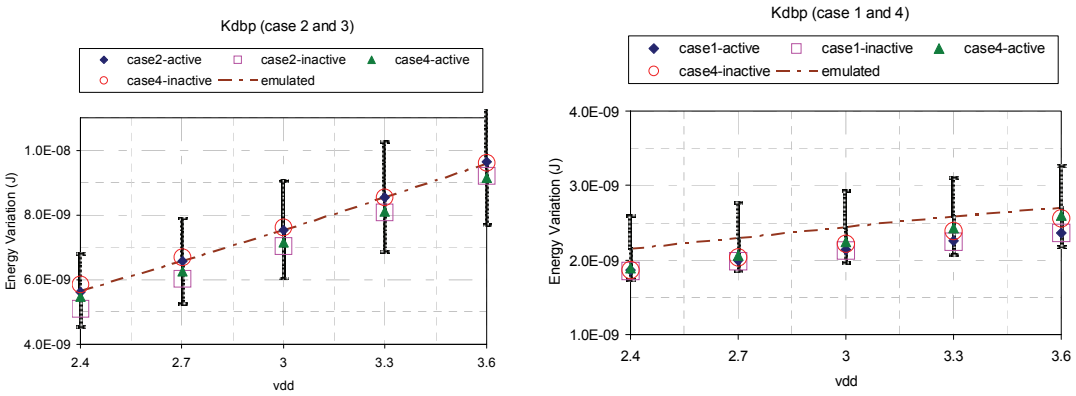


Figure 2-69. K_{db_P} related unit energy in 6th working condition for hypothesis verification

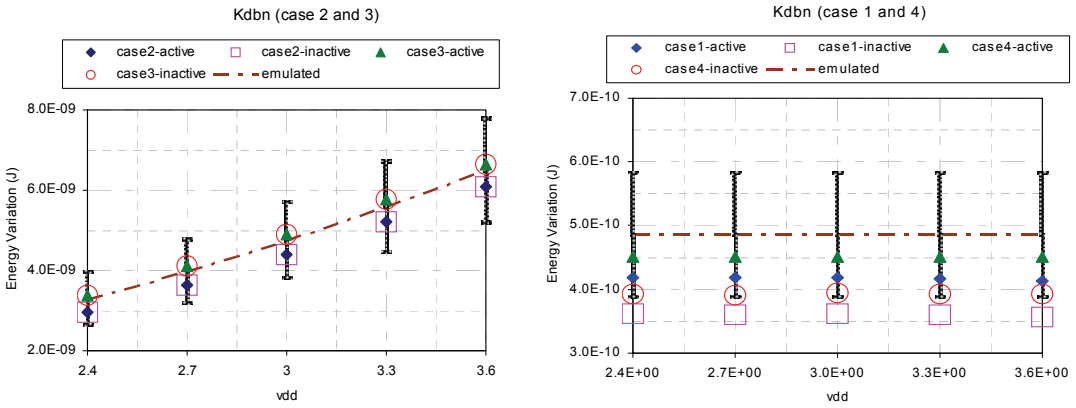


Figure 2-70. K_{db_N} related unit energy in 6th working condition for hypothesis verification

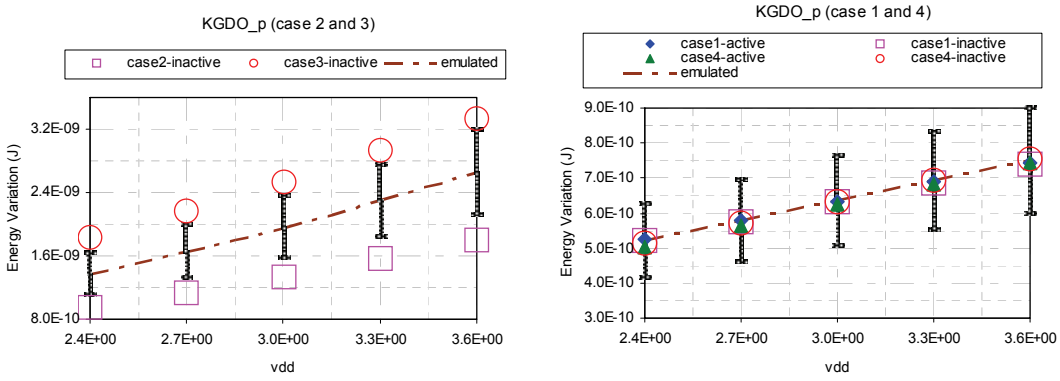


Figure 2-71. K_{GDO_P} related unit energy in 6th working condition for hypothesis verification

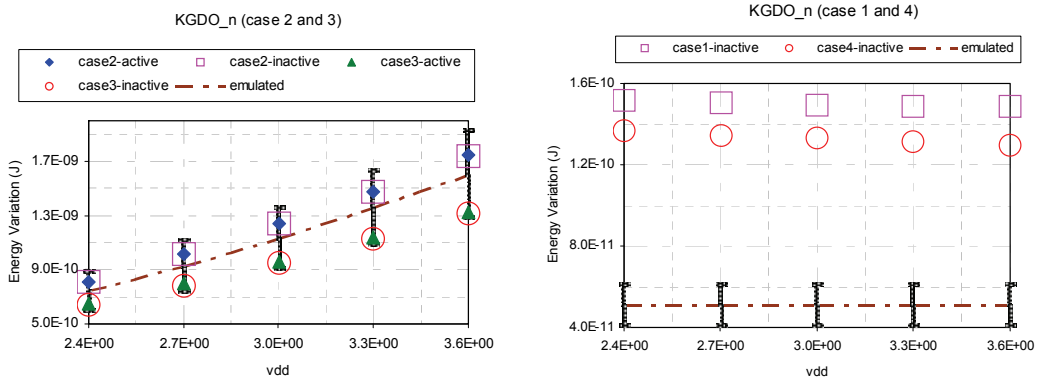


Figure 2-72. K_{GDO_N} related unit energy in 6th working condition for hypothesis verification

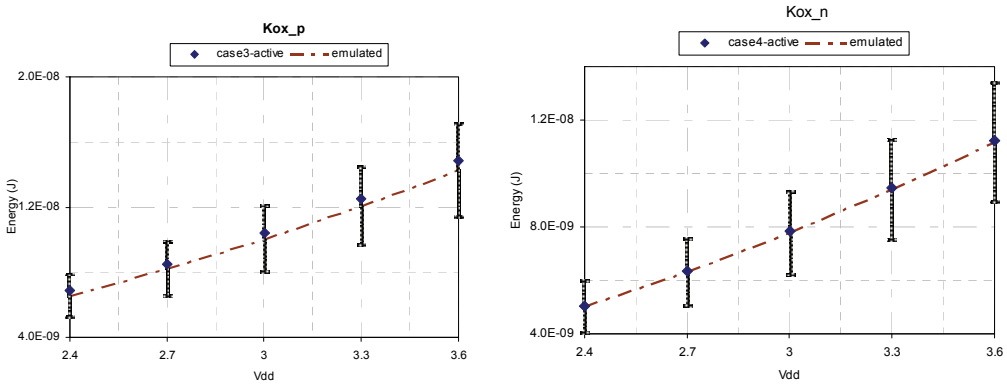


Figure 2-73. K_{ox} related unit energy in 6th working condition for hypothesis

2.5.3.7 Verification case 7

Table 2-11. Seventh verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V7	100°C	***SF***	0.4A	80%	20%	0.037	0.0247

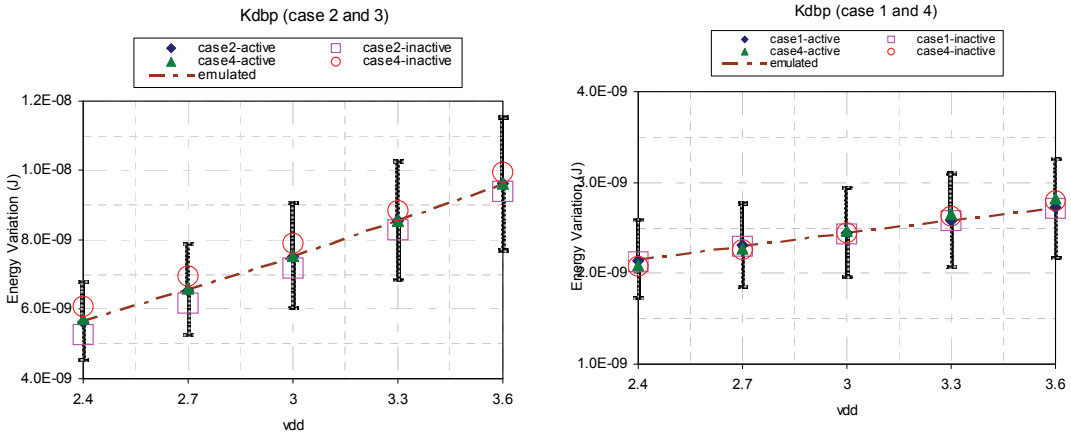


Figure 2-74. K_{db_P} related unit energy in 7th working condition for hypothesis verification

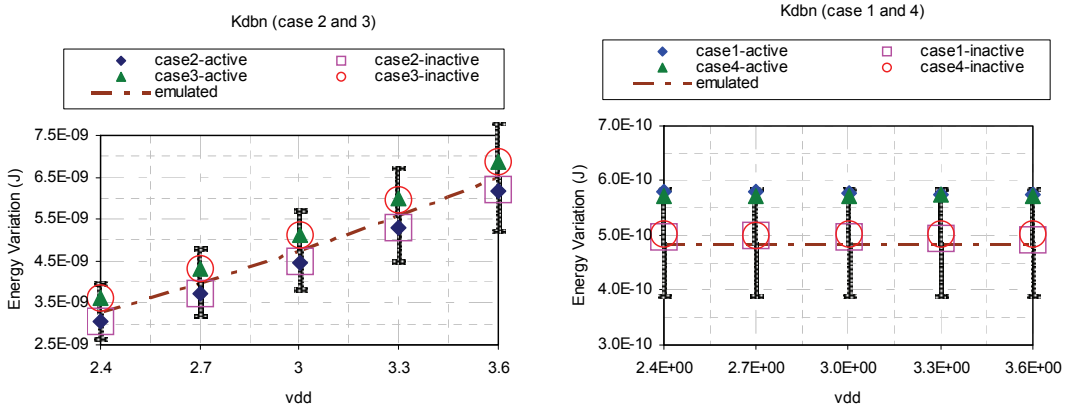


Figure 2-75. K_{db_N} related unit energy in 7th working condition for hypothesis verification

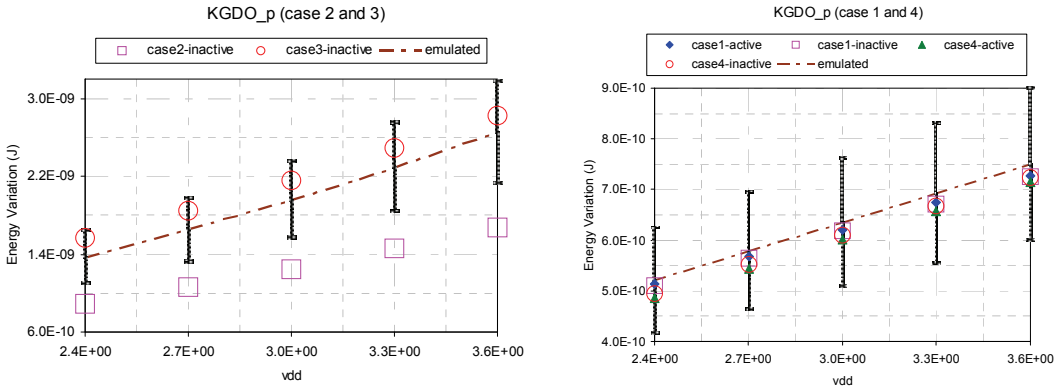


Figure 2-76. K_{GDO_P} related unit energy in 7th working condition for hypothesis verification

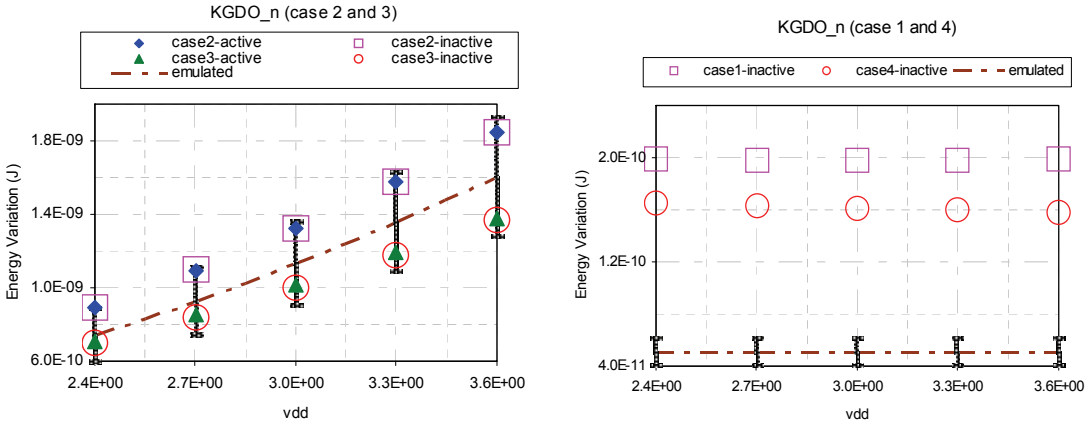


Figure 2-77. K_{GDO_N} related unit energy in 7th working condition for hypothesis verification

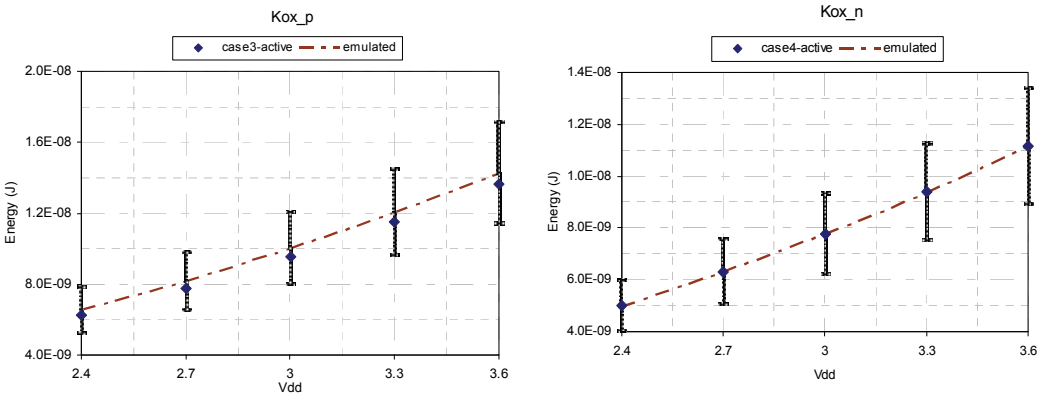


Figure 2-78. K_{ox} related unit energy in 7th working condition for hypothesis verification

2.5.3.8 Verification case 8

Table 2-12. Eighth verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V8	100°C	***SS***	0.4A	80%	20%	0.037	0.0247

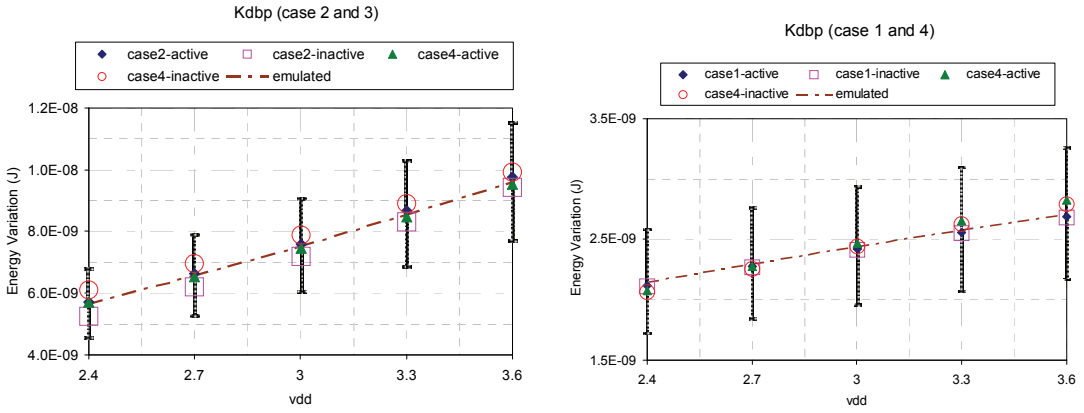


Figure 2-79. K_{db_P} related unit energy in 8th working condition for hypothesis verification

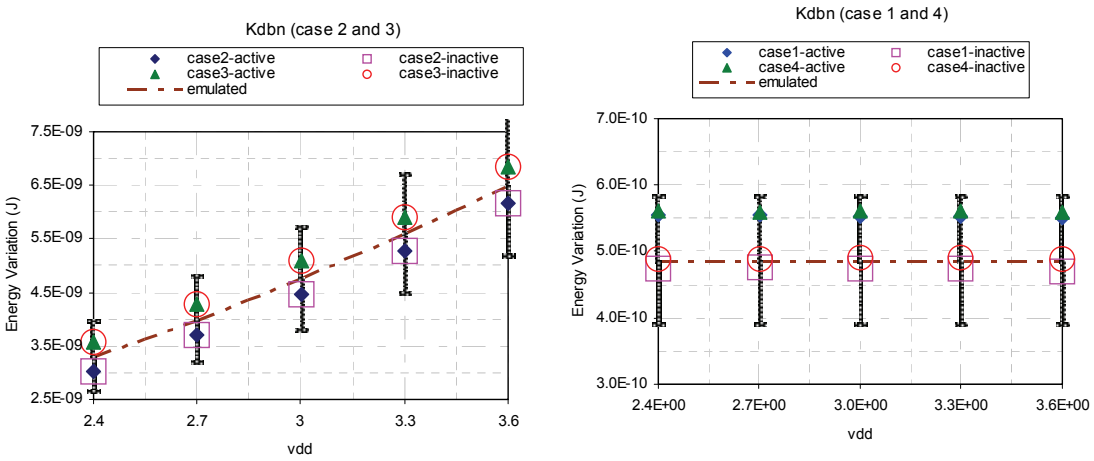


Figure 2-80. K_{db_N} related unit energy in 8th working condition for hypothesis verification

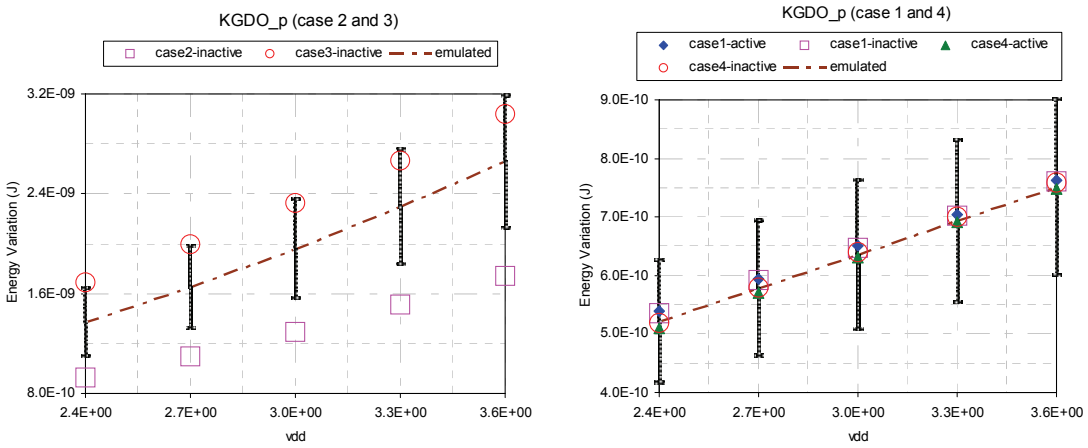


Figure 2-81. K_{GDO_P} related unit energy in 8th working condition for hypothesis verification

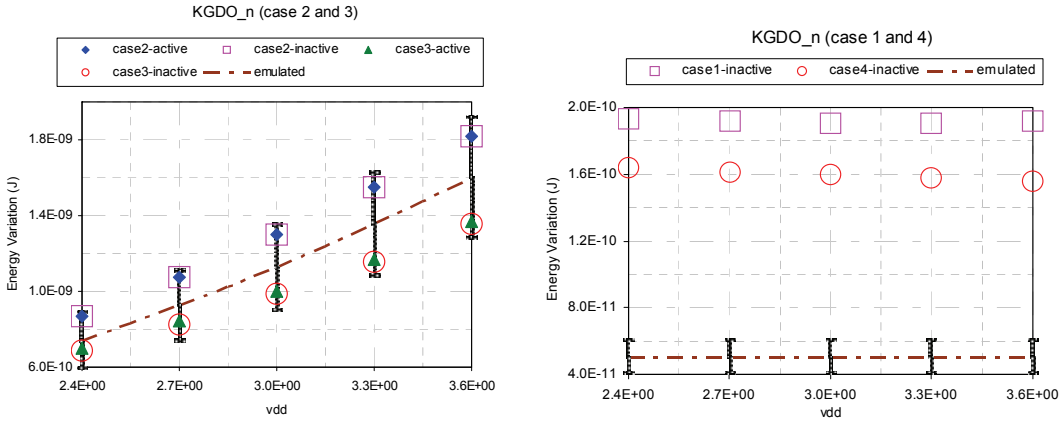


Figure 2-82. K_{GDO_N} related unit energy in 8th working condition for hypothesis verification

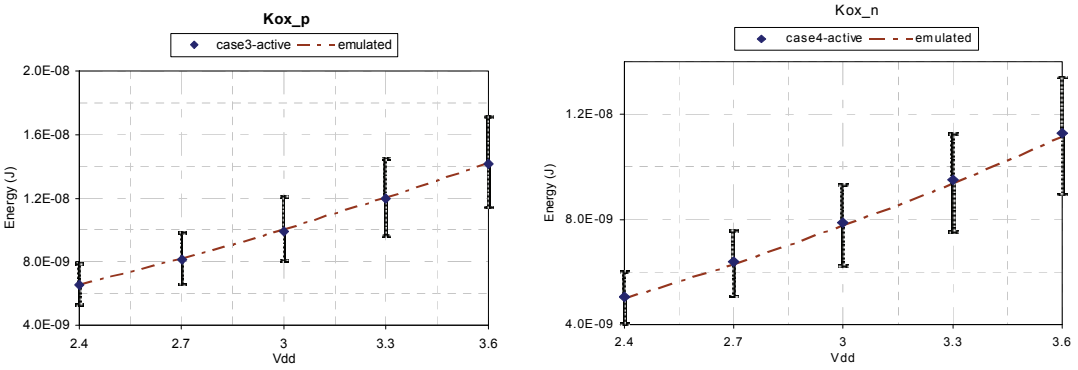


Figure 2-83. K_{ox} related unit energy in 8th working condition for hypothesis verification

2.5.3.9 Verification case 9

Table 2-13. Ninth verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V9	***50°C***	TT	0.4A	80%	20%	0.037	0.0247

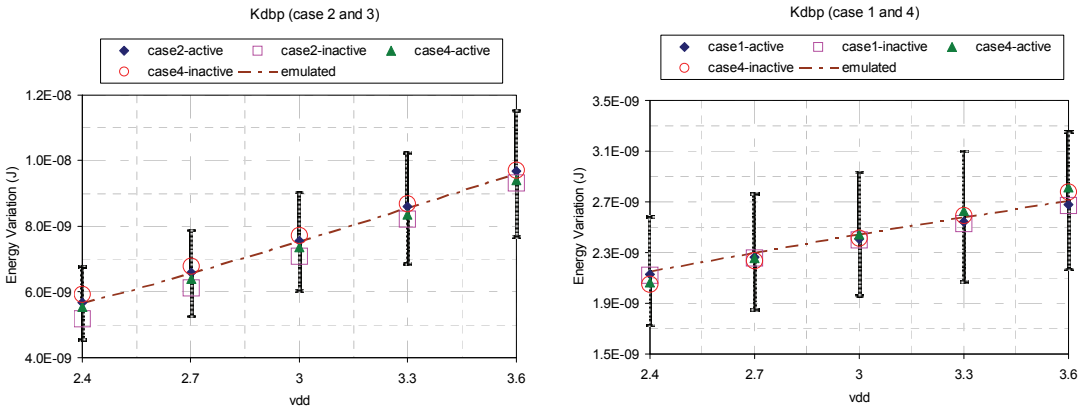


Figure 2-84. K_{db_P} related unit energy in 9th working condition for hypothesis verification

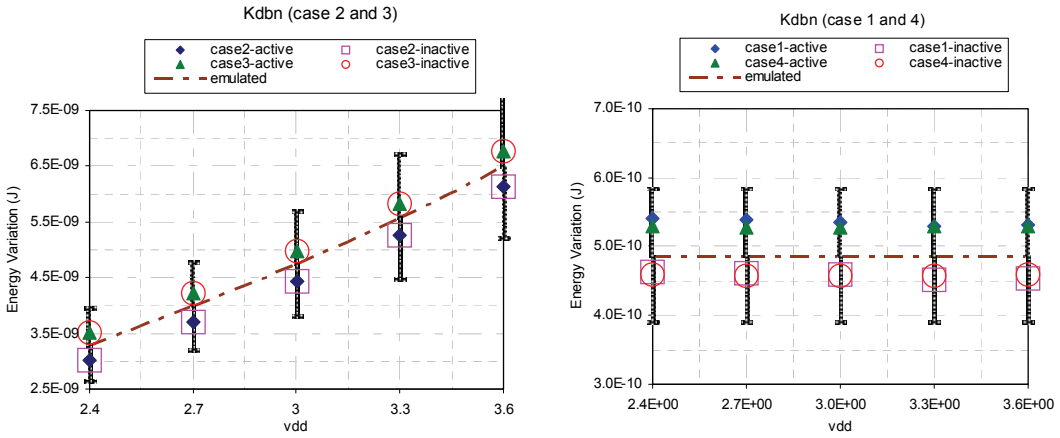


Figure 2-85. K_{db_N} related unit energy in 9th working condition for hypothesis verification

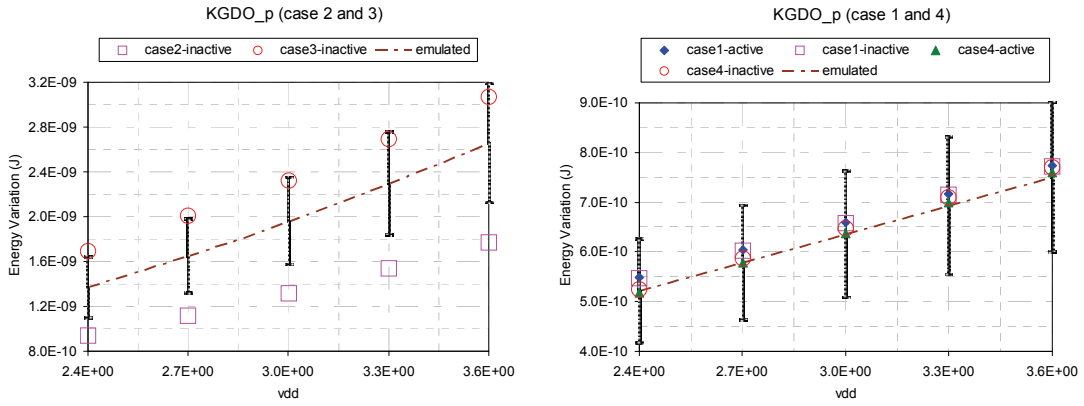


Figure 2-86. K_{GDO_P} related unit energy in 9th working condition for hypothesis verification

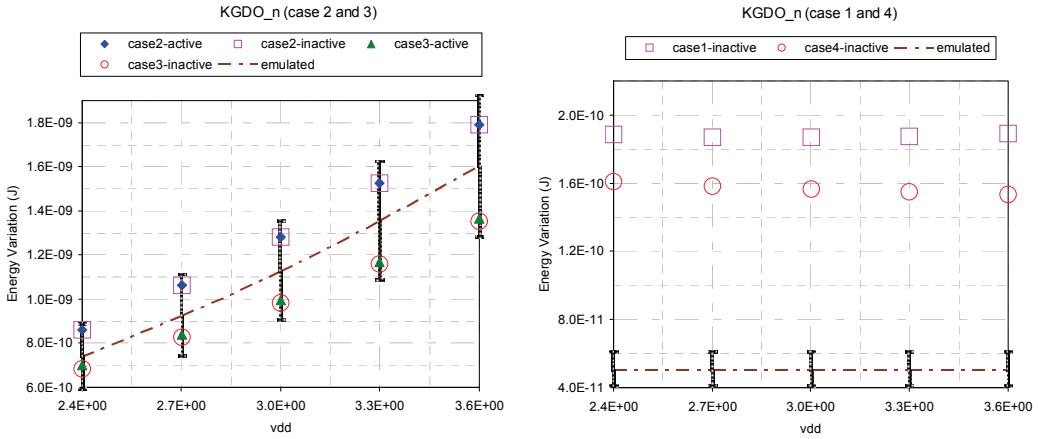


Figure 2-87. K_{GDO_N} related unit energy in 9th working condition for hypothesis verification

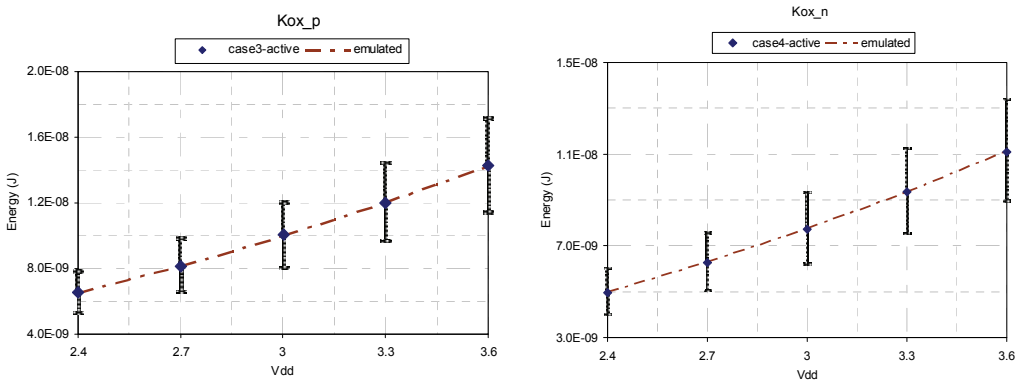


Figure 2-88. K_{ox} related unit energy in 9th working condition for hypothesis verification

2.5.3.10 Verification case 10

Table 2-14. Tenth verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V10	***0°C***	TT	0.4A	80%	20%	0.037	0.0247

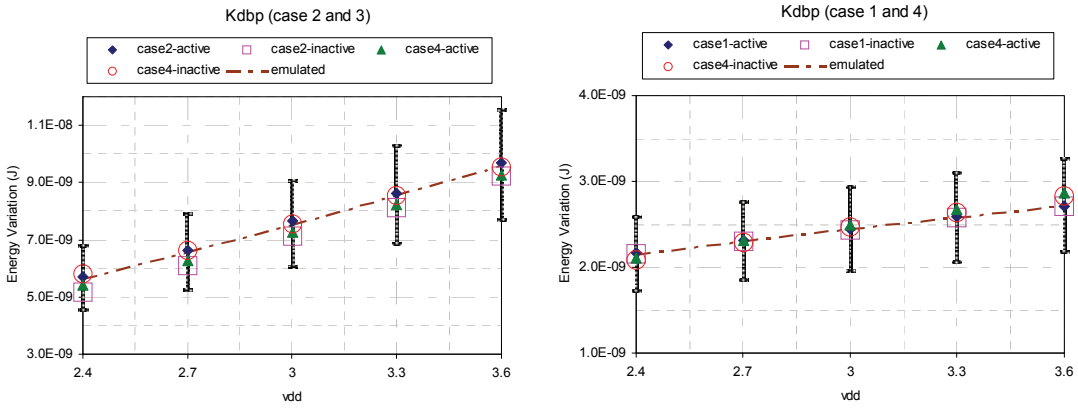


Figure 2-89. K_{db_P} related unit energy in 10th working condition for hypothesis verification

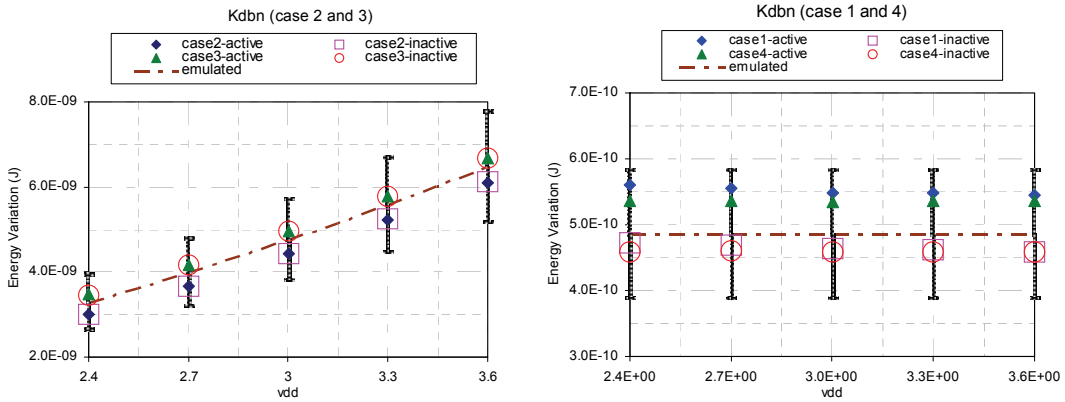


Figure 2-90. K_{db_N} related unit energy in 10th working condition for hypothesis verification

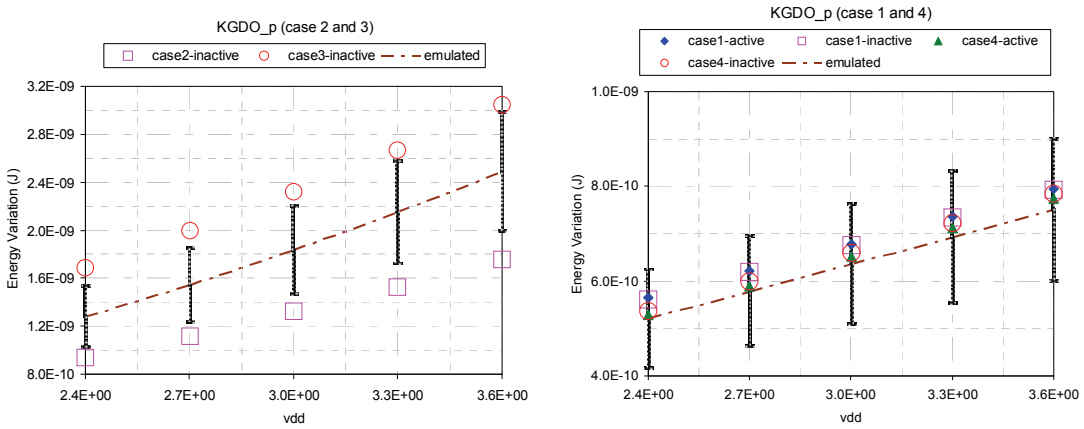


Figure 2-91. K_{GDO_P} related unit energy in 10th working condition for hypothesis verification

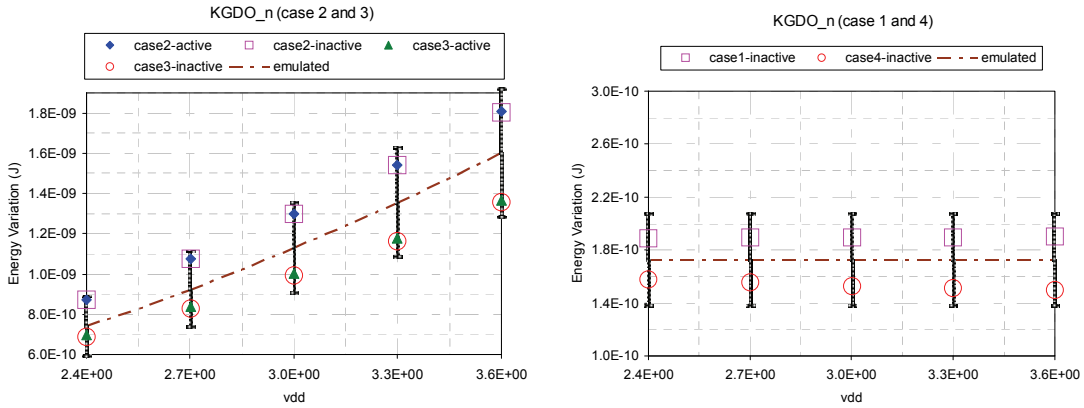


Figure 2-92. K_{GDO_N} related unit energy in 10th working condition for hypothesis verification

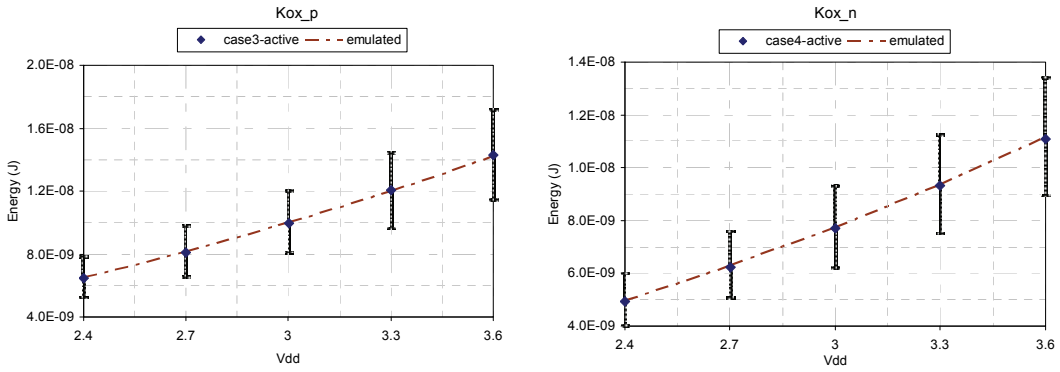


Figure 2-93. K_{ox} related unit energy in 10th working condition for hypothesis verification

2.5.3.11 Verification case 11

Table 2-15. Eleventh verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V11	100°C	TT	***0.1A***	***50%***	***50%***	0.037	0.0247

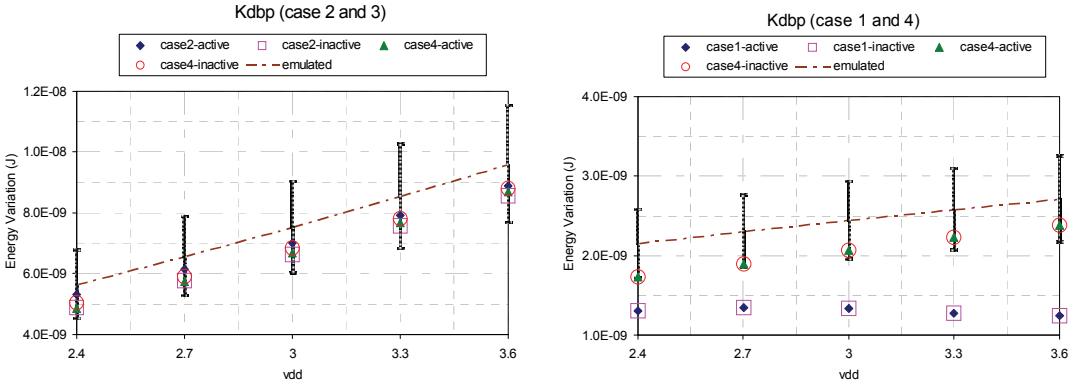


Figure 2-94. K_{db_P} related unit energy in 11th working condition for hypothesis verification

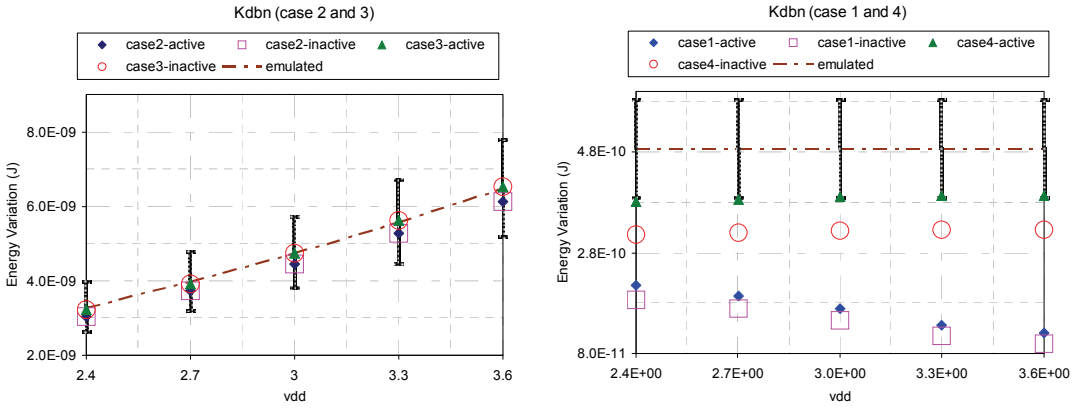


Figure 2-95. K_{db_N} related unit energy in 11th working condition for hypothesis verification

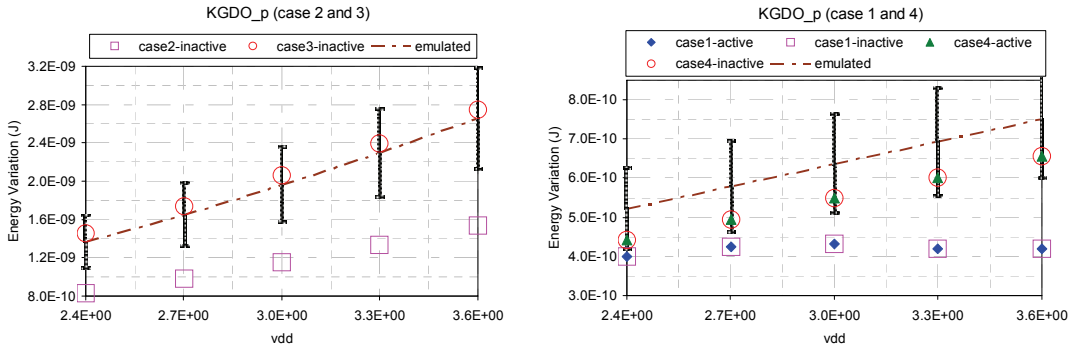


Figure 2-96. K_{GDO_P} related unit energy in 11th working condition for hypothesis verification

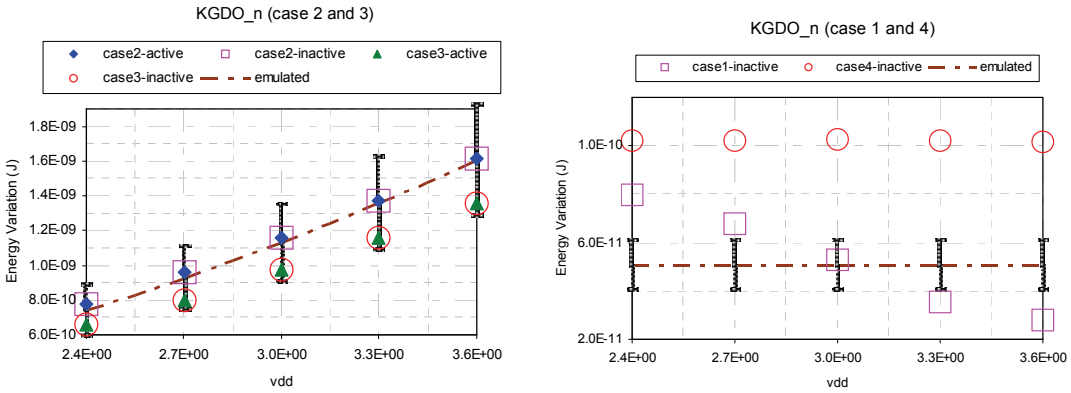


Figure 2-97. K_{GDO_N} related unit energy in 11th working condition for hypothesis verification

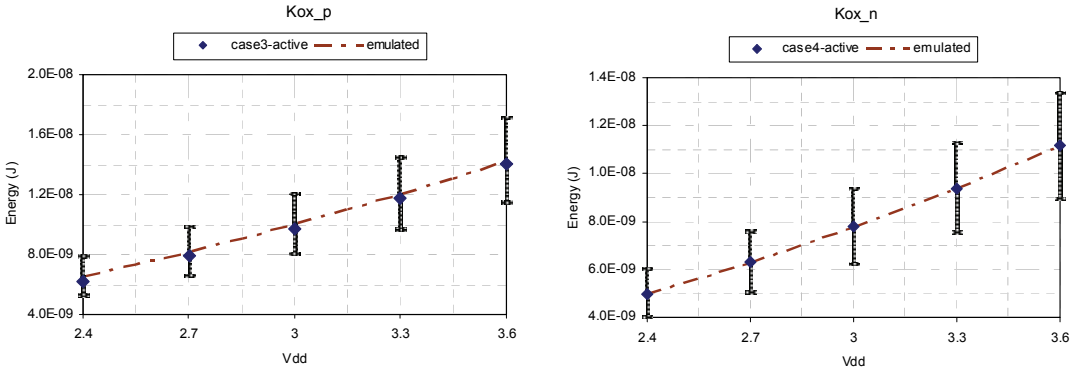


Figure 2-98. K_{ox} related unit energy in 11th working condition for hypothesis verification

2.5.3.12 Verification case 12

Table 2-16. Twelfth verification case of ISBC hypothesis

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247
V12	100°C	TT	0.4A	80%	20%	0.03	0.01

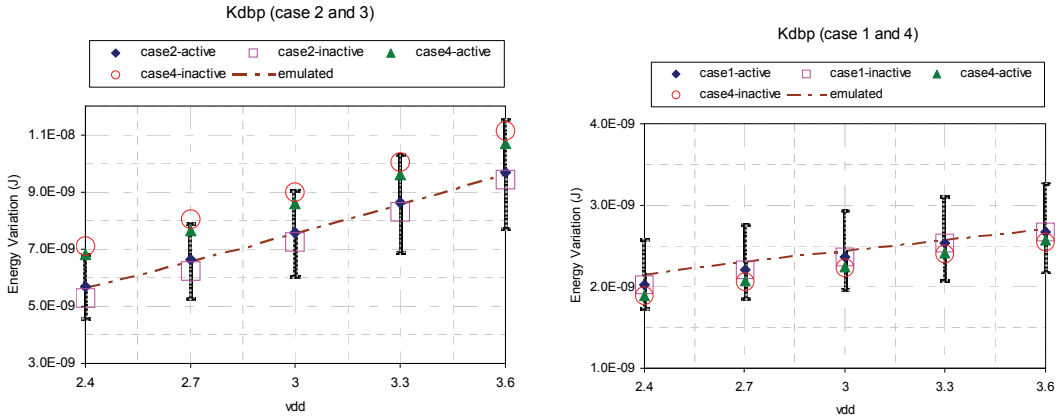


Figure 2-99. K_{db_P} related unit energy in 12th working condition for hypothesis verification

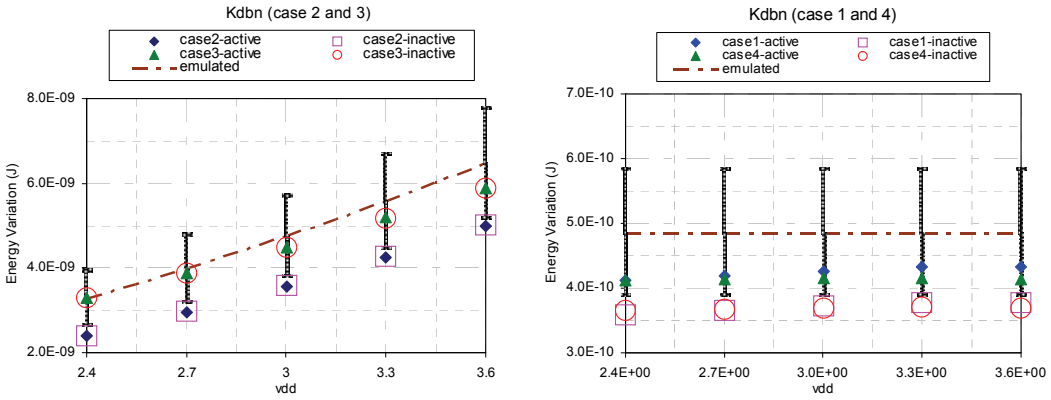


Figure 2-100. K_{db_N} related unit energy in 12th working condition for hypothesis verification

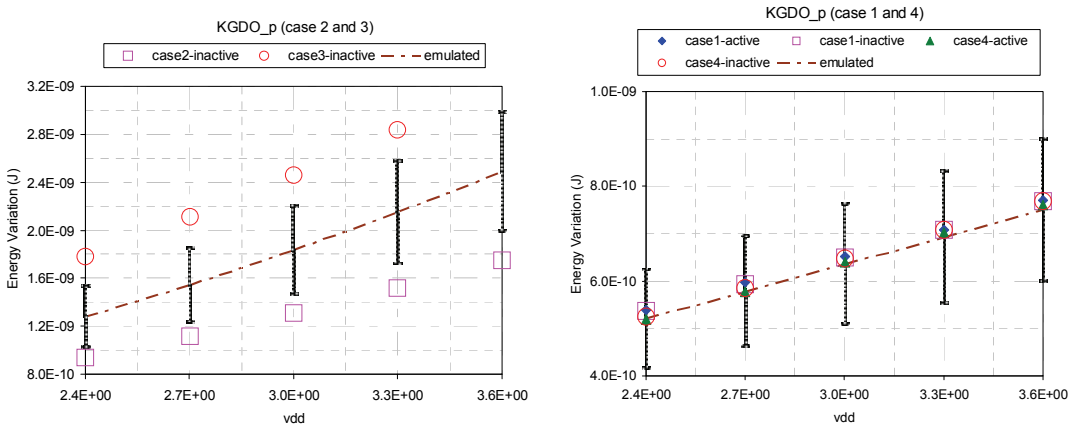


Figure 2-101. K_{GDO_P} unit energy in 12th working condition for hypothesis verification

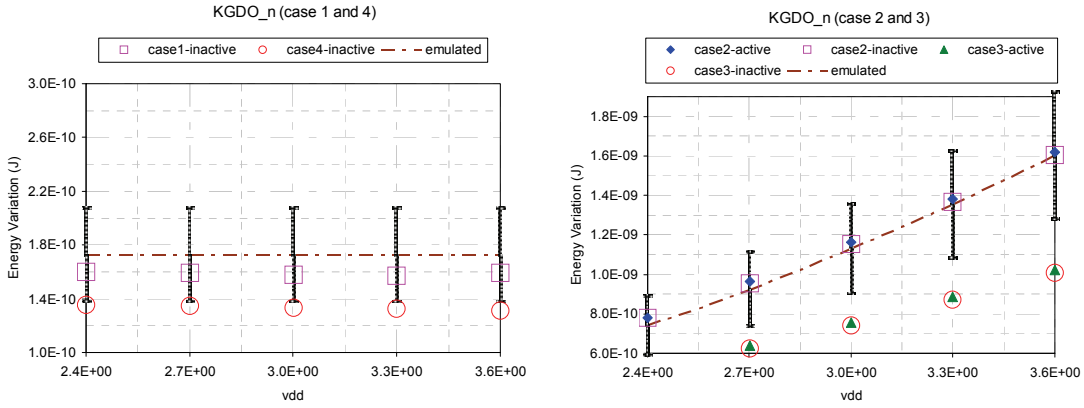


Figure 2-102. K_{GDO_N} related unit energy in 12th working condition for hypothesis verification

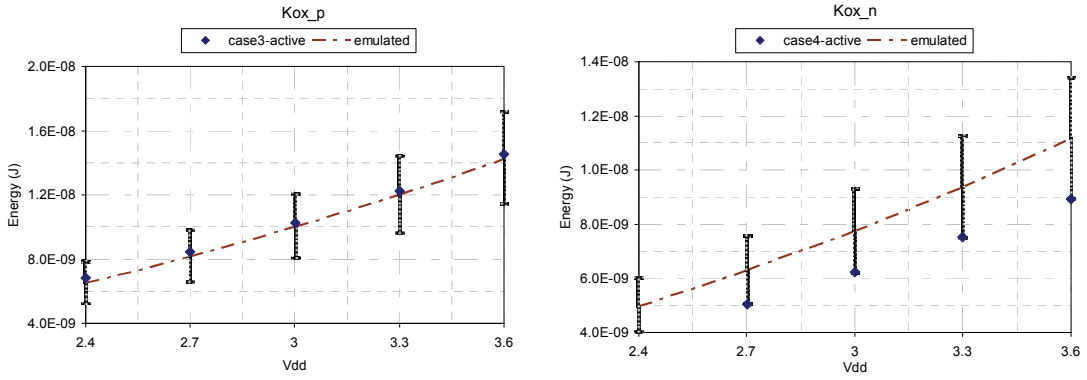


Figure 2-103. K_{ox} related unit energy in 12th working condition for hypothesis verification

From the above data analysis, we observe that the hypothesis gives a correct result for twelve different simulation corners. Thus, within a certain tolerance, the hypothesis is a handy tool for parasitic capacitor energy variation analysis.

Table 2-17. Hypothesis verification results summary

Condition No.	***Temp***	***Corner***	***Load***	***Active cells***	***Inactive cells***	φ_{P_P}	φ_{N_N}	***Pass or fail***
Extraction	100°C	TT	0.4A	80%	20%	0.037	0.0247	-
V1	100°C	TT	0.25A	80%	20%	0.037	0.0247	***Pass***
V2	100°C	TT	0.1A	80%	20%	0.037	0.0247	***Pass***
V3	100°C	TT	0.4A	50%	50%	0.037	0.0247	***Pass***
V4	100°C	TT	0.4A	20%	80%	0.037	0.0247	***Pass***
V5	100°C	FF	0.4A	80%	20%	0.037	0.0247	***Pass***
V6	100°C	FS	0.4A	80%	20%	0.037	0.0247	***Pass***
V7	100°C	SF	0.4A	80%	20%	0.037	0.0247	***Pass***
V8	100°C	SS	0.4A	80%	20%	0.037	0.0247	***Pass***
V9	50°C	TT	0.4A	80%	20%	0.037	0.0247	***Pass***
V10	0°C	TT	0.4A	80%	20%	0.037	0.0247	***Pass***
V11	100°C	TT	0.1A	50%	50%	0.037	0.0247	***Pass***
V12	100°C	TT	0.4A	80%	20%	0.03	0.01	***Pass***

The extracted coefficients are listed in (2-111) and the capacitances are in Table 2-18.

$$K_{GDO\_P} = 2.9376\times10^{-10}\,F\cdot m^{-1}, \qquad K_{GDO\_N} = 2.3924\times10^{-10}\,F\cdot m^{-1} \tag{2-111}$$

$$K_{ox\_P} = 1.2005\times10^{-9}\,F\cdot m^{-1}, \qquad K_{ox\_N} = 1.2335\times10^{-9}\,F\cdot m^{-1}$$

$$K^{1}_{db\_P} = 2.4062\times10^{-9}\,F\cdot V^{1/2}\cdot m^{-1}, \quad K^{2}_{db\_P} = 1.5334\,V^{1/2}$$

$$K^{1}_{db\_N} = 3.3486\times10^{-9}\,F\cdot V^{1/2}\cdot m^{-1}, \quad K^{2}_{db\_N} = 9.5271\,V^{1/2}, \; K_{rr} = 4.8521^{-10}\,J\cdot m^{-1}$$

The rdson coefficients of MOSFET is also extracted and given in (2-112).

$$R^{P}_{unit} = \frac{0.197}{1+4.54V_{dd}}\Omega\cdot m\,; \qquad R^{N}_{unit} = \frac{0.0122}{1+0.625V_{dd}}\Omega\cdot m \tag{2-112}$$

Table 2-18. Parasitic component values extracted in BSIM3V3.1 level 49 model of AMI06 process (T=100oC, TT corner)

Unit value	Conduction mode	Vdd	Vdd=3V
PFET C_{gd_p} (F*m^{-1})	Cutoff region $C_{gd\_p}^{(C)}$	2.9376×10^{-10}	2.9376×10^{-10}
	Linear region $C_{gd\_p}^{(L)}$	0.8940×10^{-9}	0.8940×10^{-9}
	Saturation region $C_{gd\_p}^{(S)}$	0.8940×10^{-9}	0.8940×10^{-9}
PEFT C_{gs_p} (F*m^{-1})	Cutoff region $C_{gs\_p}^{(C)}$	2.9376×10^{-10}	2.9376×10^{-10}
	Linear region $C_{gs\_p}^{(L)}$	0.8940×10^{-9}	0.8940×10^{-9}
	Saturation region $C_{gs\_p}^{(S)}$	1.0941×10^{-9}	1.0941×10^{-9}
PFET C_{db_p} (F*m^{-1})	-	$\frac{2.4062\times10^{-9}}{\sqrt{V_{dd}+1.5334}}$	1.1301×10^{-9}
PFET R_{unit}^{P} ($\Omega\cdot m$)	Linear region, 100°C, TT corner, 0.4A.	$\frac{0.197}{1+4.54V_{dd}}$	0.0135
NFET C_{gd_n} (F*m^{-1})	Cutoff region $C_{gd\_n}^{(C)}$	2.3924×10^{-10}	2.3924×10^{-10}
	Linear region $C_{gd\_n}^{(L)}$	0.8560×10^{-9}	0.8560×10^{-9}
	Saturation region $C_{gd\_n}^{(S)}$	0.8560×10^{-9}	0.8560×10^{-9}
NFET C_{gs_n} (F*m^{-1})	Cutoff region $C_{gs\_n}^{(C)}$	2.3924×10^{-10}	2.3924×10^{-10}
	Linear region $C_{gs\_n}^{(L)}$	0.8560×10^{-9}	0.8560×10^{-9}
	Saturation region $C_{gs\_n}^{(S)}$	1.0616×10^{-9}	1.0616×10^{-9}
NFET C_{db_n} (F*m^{-1})	-	$\frac{3.3486\times10^{-9}}{\sqrt{V_{dd}+9.5271}}$	9.4610×10^{-10}
NFET R_{unit}^{N} ($\Omega\cdot m$)	Linear region, 100°C TT corner, 0.4A.	$\frac{0.0122}{1+0.625V_{dd}}$	0.0042
Err (J*m^{-1})	Reverse recovery Energy	4.8521^{-10}	4.8521^{-10}

2.6 Driver design and D_loss

A cascade tapered driver is constructed with multi-stage inverters and is designed using the following constraints:

1). In each stage, the ratio of PMOS to NMOS is set to be 3:1.

2). The PFET driver's last stage has a PMOS width of $\varphi_{P\_P}W_P$ and a NMOS width of $\varphi_{P\_N}W_P = \frac{\varphi_{P\_P}W_P}{3}$.

3). The NFET driver's last stage has a NMOS width of $\varphi_{N\_N}W_N$ and a PMOS width of $\varphi_{P\_N}W_N = 3\varphi_{N\_N}W_N$.

4). The tapered driver has a size ratio of 4:1 between two cascaded inverter stages.

5). The gate resistance is estimated to be $R_{gate}^{PP} = R_{gate}^{PN} = R_{gate}^{NP} = R_{gate}^{NN} = 0.4\Omega$.

Table 2-19. Driver sizing symbols

Symbol	φ_{P_P}	φ_{P_N}	φ_{N_P}	φ_{N_N}
description	PFET driver's PMOS width to PFET width	PFET driver's NMOS width to PFET width	NFET driver's PMOS width to NFET width	NFET driver's NMOS width to NFET width

2.6.1 D_loss

The gate driver loss is given in (2-113)

$$P_{drive}^{loss} = \tag{2-113}$$

$$\frac{5}{4}V_{dd}^2\left[\varphi_{P\_P}\left(C_{gd\_p}^{(L)}+C_{gd\_p}^{(C)}+C_{gs\_p}^{(L)}+C_{db\_p}\right)+\varphi_{P\_N}\left(C_{gd\_n}^{(L)}+C_{gd\_n}^{(C)}+C_{gs\_n}^{(L)}+C_{db\_n}\right)\right]W_P^{active}*f$$

$$+\frac{5}{4}V_{dd}^2\left[\varphi_{N\_P}\left(C_{gd\_p}^{(L)}+C_{gd\_p}^{(C)}+C_{gs\_p}^{(L)}+C_{db\_p}\right)+\varphi_{N\_N}\left(C_{gd\_n}^{(L)}+C_{gd\_n}^{(C)}+C_{gs\_n}^{(L)}+C_{db\_n}\right)\right]W_N^{active}*f$$

$$=\frac{5}{4}V_{dd}^2\left[\left(C_{gd\_p}^{(L)}+C_{gd\_p}^{(C)}+C_{gs\_p}^{(L)}+C_{db\_p}\right)+\frac{1}{3}\left(C_{gd\_n}^{(L)}+C_{gd\_n}^{(C)}+C_{gs\_n}^{(L)}+C_{db\_n}\right)\right]*$$

$$*\left(\varphi_{P\_P}W_P^{active}+3\varphi_{N\_N}W_N^{active}\right)*f$$

2.6.2 φ_{P_P} selection

The driver is optimized for normal working conditions and is designed with the parameters $V_{dd}=3V$, $W_P=W_P^{active}=110mm$, $W_N=W_N^{active}=55mm$, $V_{TH}^P=0.92V$, $V_{TH}^N=0.67V$, $K_P=82.63A/m\cdot V^2$.

We observe from (2-20), (2-31) and (2-37) that φ_{P_P} will impact the O_loss. Figure 2-104 illustrates the relation between φ_{P_P} and z_1 in (2-10). The relationship between φ_{P_P} and $V_g^{P\_on}$ is described in (2-13) and is depicted in Figure 2-105. The criterion *MPoff* in (2-31) for PFET turn-off loss is depicted in Figure 2-106.

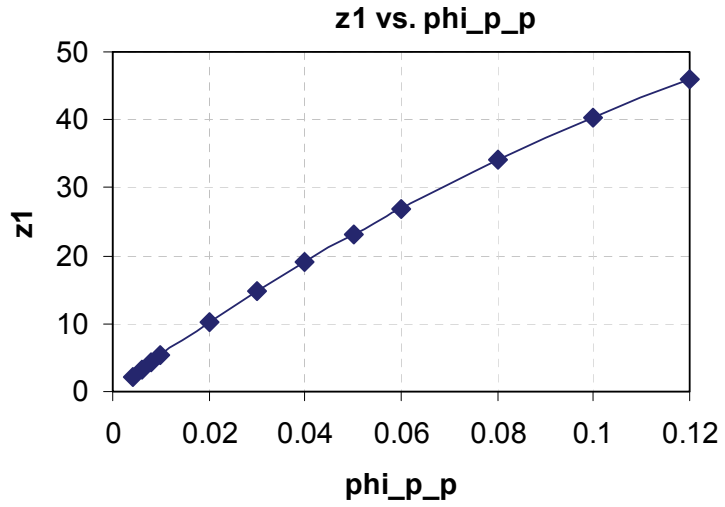


Figure 2-104. The impact of φ_{P_P} on z_1

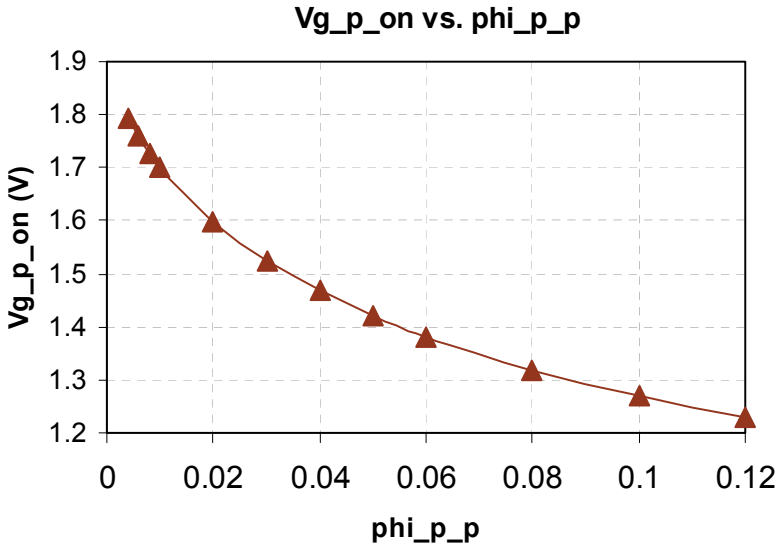


Figure 2-105. The impact of φ_{P_P} on $V_g^{P\_on}$

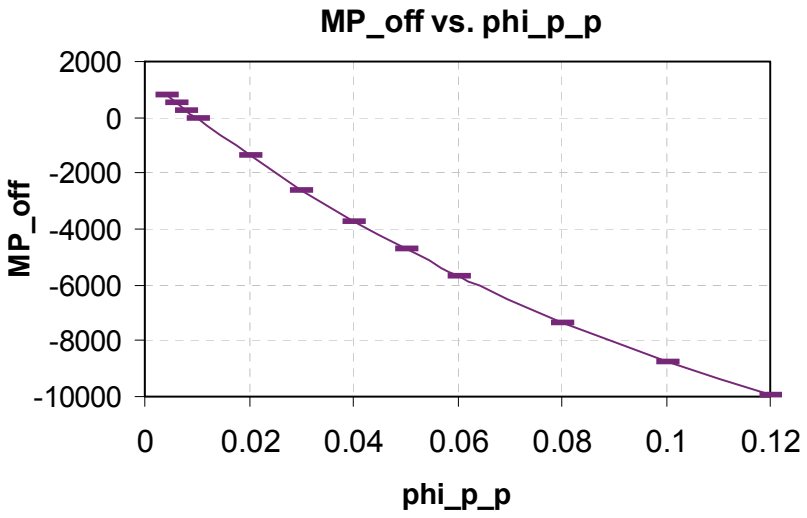


Figure 2-106. The impact of φ_{P_P} on PFET turn-off *MPoff*

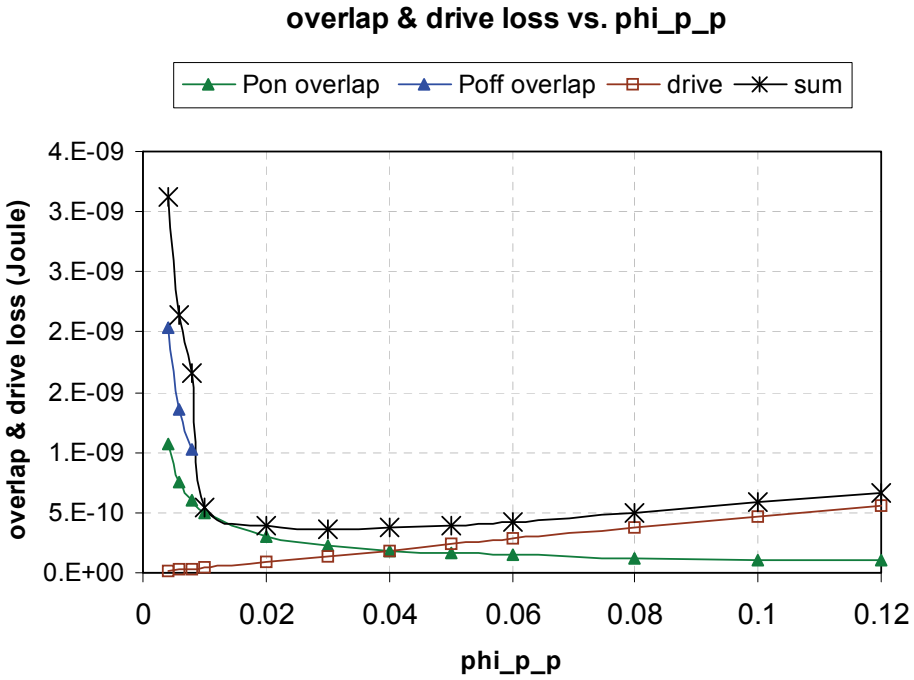


Figure 2-107. The impact of φ_{P_P} on power loss

φ_{P_P} not only impacts the O_loss, it is also linearly proportional to D_loss as given by (2-113). In Figure 2-107, the O_loss for the PFET turn-on event, the O_loss for the PFET turn-off (if $MPoff > 0$ is true) and the D_loss are calculated for different φ_{P_P}. From the Figure 2-107, we realize that the energy loss relative to φ_{P_P} will be the minimum when $\varphi_{P\_P} = 0.05$ and the valley value is 5.6178e-10J.

Beyond the implications of the losses, the impact of the current pulse generated during the transient should also be considered. The larger φ_{P_P} is, the sharper the transient current pulse will be; this implies a higher device rating requirement, worse switching node voltage oscillation, and switching noise due to the presence of package inductance. The Figure 2-108 illustrates the comparison of i_{P1}, v_{SW} and v_g^P when φ_{P_P} is 0.02, 0.03 and 0.06 during the power PFET turn-on event. Figure 2-109 illustrates the comparison during the power PFET turn-off.

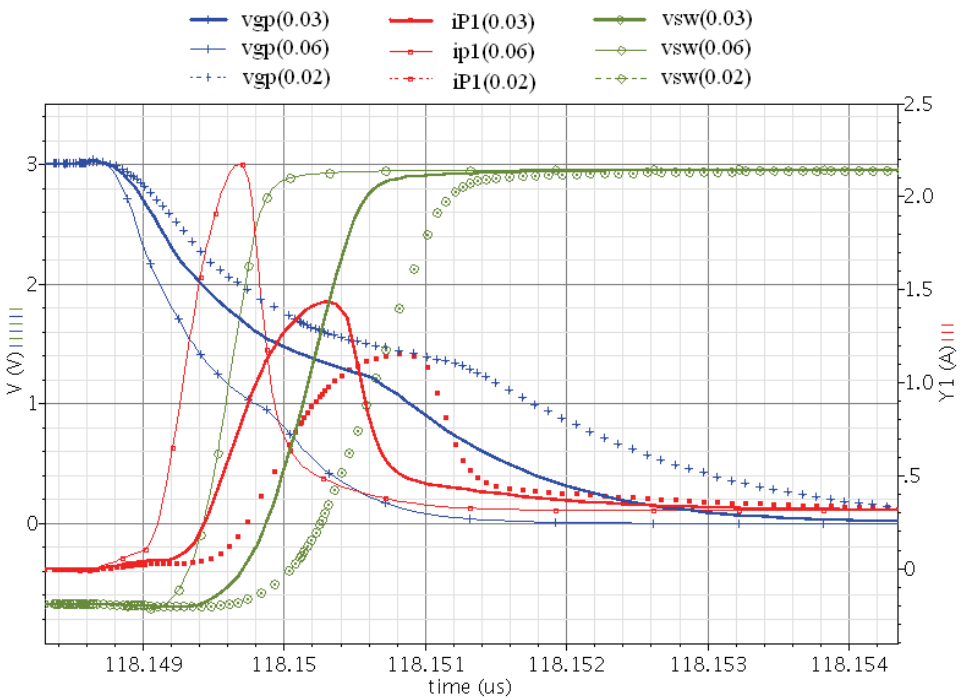


Figure 2-108. Transient current pulse and switching delay when PFET turns on

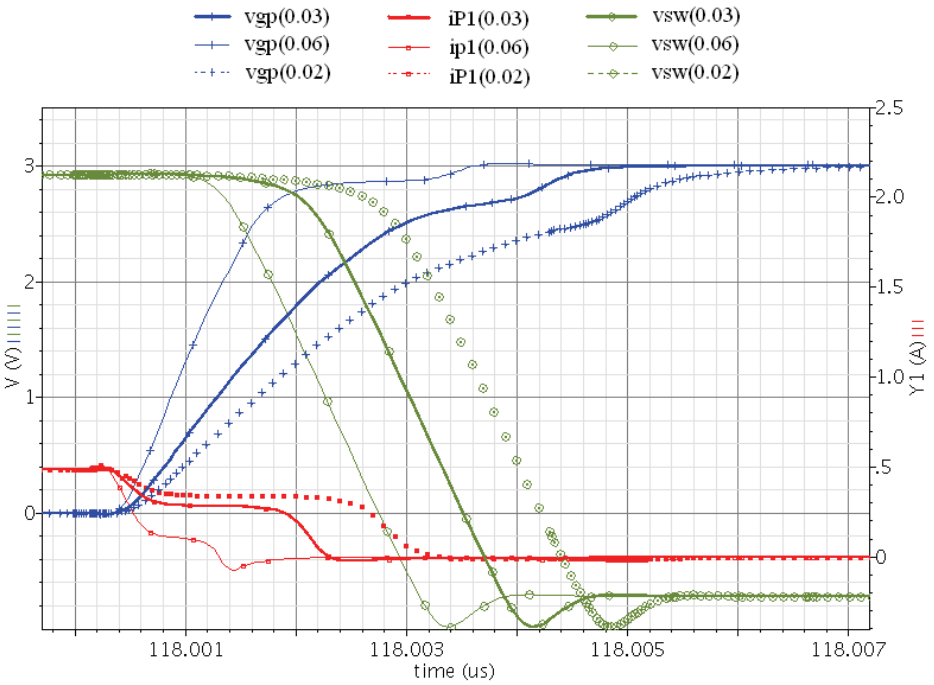


Figure 2-109. Transient current pulse and switching delay when PFET turns off

At the same time, the larger φ_{P_P} is, the larger the switching delay will be. Table 2-20 listed the detailed comparison of ISBC performance when φ_{P_P} is 0.02, 0.03 and 0.06.

Table 2-20. φ_{P_P} impact on ISBC switching performance

	$\varphi_{P\_P} = 0.02$	$\varphi_{P\_P} = 0.03$	$\varphi_{P\_P} = 0.06$
Peak PFET ids (A)	2.2	1.4	1.2
Settling time of V_{SW} when PFET turns on (ns)	2.5	1.8	1
Overlap and driver loss when PFET turns on (10^{-10} J)	8.39	6.68	5.69
Settling time of V_{SW} when PFET turns off (ns)	4.6	3.8	3

Different applications call for different FOM (Figures of merits) considerations. I selected $\varphi_{P\_P} = 0.03$. Thus, $\varphi_{P\_N} = 0.01$. The data calculated given the parameters is given in Table 2-21.

Table 2-21. Parameters relative to the selected φ_{P_P} value

φ_{P_P}	0.03		$V_g^{P\_off}$	-
$z1$	5.98		$E_{overlap}^{P\_on}$	$5.42*10^{-10}$ (J)
$z2$	2.08		$E_{overlap}^{P\_off}$	0
$V_g^{P\_on}$	1.67 (V)		E_{drive}^{P}	$1.25*10^{-10}$ (J)
MPoff	-3063		$E_{overlap}^{P\_on}$	$6.68*10^{-10}$ (J)

2.6.3 φ_{N_N} selection

As there is no Miller plateau in the power NFET, from the viewpoint of D_loss consideration, we should decrease the NFET driver size as much as possible. However, this is not good practice for the overall system design; several other factors should also be considered.

- The power NFEF conduction loss is inversely proportional to the applied gate voltage. If the NFET driver is too small, the gate voltage rise will be very slow and the consequent increase of Rdson loss might significantly overweight the possible savings in driver loss. Thus, there will be a tradeoff between the power NFET conduction loss and driver loss;
- The Power NFET dv/dt [2-26] [2-27] false turn-on will generate temporary shoot through when the power PFET is in the turn-on transient. There are many techniques to minimize the risk of the false turn-on via device or circuit design [2-

10]. The most simple and effective method is to strengthen the power NFET driver capacity through decreasing the driver's conduction resistance in the linear region.

- Careful deadtime setting is necessary to avoid power FET parasitic induced shoot through. From (2-49) and (2-51), we notice that $t_{dead}^{1\_set}$ is inversely proportional to φ_{N_N}. If we notice the difference between the dead time setting value and the effective value under different load conditions, we realize that too small a NFET driver will result in a large deadtime setting values $t_{dead}^{1\_set}$ resulting in an efficiency drop under heavy load conditions.

The value of φ_{N_N} we used for the 4MHz synchronous Buck converter in AMI06 was selected to be $\varphi_{N\_N} = 0.01$. Thus, $\varphi_{N\_P} = 0.03$

2.7 Conclusions and future work

In this chapter, a novel switching event based switching loss analysis approach was developed. This method physically and completely classified the charging/discharging loss and overlap loss. Furthermore, it classified the ratio of charging/discharging loss to capacitor energy variation in all switching events for each parasitic capacitor. In order to calculate the energy variation of a parasitic capacitor with varying capacitance during a complete switching event, a hypothesis was proposed and a parasitic capacitance extraction process was generated. The hypothesis was verified with different designs, operation conditions, and process corners.

This chapter also developed criteria to analyze the existence of Miller plateau in a switching event. These criteria indicated that PFET turn-on overlap always exists while PFET turn-off overlap has the possibility to be eliminated in portable applications. The

reason why there is no Miller plateau in NFET turn-on or turn-off transients was also explained.

With the aid of the above analysis and the extracted capacitance, a complete set of equations to calculate the switching loss were developed. The equations will be utilized in chapter 3 to predict the load efficiency curve and the efficiency improvement after the power FET segmentation technique is applied.

This chapter also provided theoretical equations for dead-time setting and gate driver optimization.

This chapter focused on the ISBC in CMOS technology. In the future, it is necessary to extend the analysis to the ISBC in BiCMOS technology where the maximum load current might be larger than 20A.

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Chapter 3

Power stage design and optimization

In this chapter, a 4MHz ISBC power stage is designed for a portable application and the power FET is optimized on the basis of the switching loss analysis introduced in the chapter two. The switching loss analysis is also utilized to predict the power efficiency of the ISBC when segmentation technique is implemented and the results are compared with the simulation data.

3.1 Power filter and PID control

3.1.1 System Specification

The system specification is proposed based on the datasheets of several commercial products developed in the recent years for portable applications, which are listed in Table 3-1.

Table 3-1. System specifications collection in several commercial products

Company	Part number	Vin (V)	Vou (V)	Maximum output current (A)	Maximum frequency (MHz)	Inductor μH	Capacitor μF	package
Texas Instru.	***TPS62260 [3-1]***	***2.3-6.0***	***0.6-Vin***	***0.6***	***2.25***	***2.2***	***10***	***BYK***
Texas Instru.	***TPS62600 [3-2]***	***2.3-5.5***	***1.0-2.5***	***0.5***	***6***	***0.47***	***4.7***	***YFF-6***
Fairchild	***FAN5361 [3-3]***	***2.3-5.5***	***1.0-1.82***	***0.6***	***6***	***0.47***	***4.7***	***WLCSP***
Intersil	***ISL9104 [3-4]***	***2.7-6.0***	***0.8***	***0.5***	***4.3***	***1.0***	***4.7***	***uTDFN***
National Semicon.	***LM3691 [3-5]***	***2.3-5.5***	***0.75 -3.3***	***1***	***4***	***1***	***4.7***	***6-Bump Thin Micro***
Micrel	***MIC2285 [3-6]***	***2.7-5.5***	***1.0-2.5***	***0.5***	***8***	***0.47***	***10***	***MLF***

The developed system is to be designed with AMI06 standard CMOS process and fabricated by the MOSIS educational program using the SCN3ME_SUMB technology [3-7].

The proposed system specifications are listed below:

	Min	***Max***	***Nominal (CCM)***
Input voltage:	2.4V	3.6V	3V
Output voltage:	0.8V	1.8V	1.5V
Output current:	0	0.4A	0.4 A
Switching frequency:	50kHz	4 MHz	4 MHz
Output voltage ripple:	-	25mV	5mV
Transient voltage deviation:		< 50mV	50mV
Controller bandwidth:		>200KHz	>200KHz
Phase Margin:		>45°	>45°

(* 80mA load current is selected as the mode transfer point between PWM and PFM)

3.1.2 Output Filter

3.1.2.1 Power Inductor

To ensure that the inductor current remains larger than zero for CCM operation in all possible working conditions, when the average inductor current is as low as 0.08A, the value of the power inductance should satisfy equation (3-1).

$$80mA \geq \frac{(V_g - V_o)D}{2\,L\,f_S} = \frac{\left(V_0 - \frac{V_0^2}{V_g}\right)}{2\,L\,f_S} \tag{3-1}$$

Because $Max\left[\left(V_0 - \frac{V_0^2}{V_g}\right)\right] = \left(1.8 - \frac{1.8^2}{3.6}\right) = 0.9$, we get $L \geq \frac{0.9}{0.16 \times f_S} = 1.41\mu H$.

We used a Murata Power solutions $1.5\mu H$ 35152C (INDUCTOR 1.5UH 6.5A SMD FLAT) (6.80mm x 6.80mm x 3.20mm) with a maximum direct current resistance (DCR) $19\,m\Omega$.

3.1.2.2 Power Capacitor

The output filter's capacitance is selected to make the output voltage ripple smaller than 5mV when the ISBC works in CCM operation. The output voltage ripple equation is given in equation (3-2)

$$\Delta V_o = V_o \frac{1-D}{L\, f_S}\left(\frac{1}{8\, C\, f_S} + ESR\right) \leq 5mV\,. \tag{3-2}$$

Because $Max\left[V_o\,(1-D)\right] = 0.9$, we need the capacitance to satisfy (3-2).

$$\left(\frac{1}{8\, C\, f_S} + ESR\right) \leq 33.33mV \tag{3-3}$$

Two SMD type $4.7\mu F$ capacitors are selected; the equivalent series resistance (ESR) is expected to be around $5\,m\Omega$.

The resonant frequency of the output filter satisfies controllability consideration as specified in (3-4).

$$f_o = \frac{1}{2\pi\sqrt{LC}} = 42{,}385 < 0.05\, f_S = 200{,}000 \tag{3-4}$$

3.1.2.3 Ripple and RMS value calculation

Inductor current ripple for CCM operation conditions is calculated with (3-5).

$$\Delta i_L = \frac{D'\,V_{out}}{L\,f_s} = \frac{\left(1-\frac{V_{out}}{V_{in}}\right)V_{out}}{L\,f_s} = \frac{(1-\frac{1.5}{3})\,1.5}{1.5\mu H * 4\times 10^6\,Hz} \approx 0.125A \tag{3-5}$$

Output voltage ripple for CCM operation conditions is calculated with (3-6)

$$\Delta V_o = V_o \frac{1-D}{L\,f_S}\left(\frac{1}{8\,C\,f_S} + ESR\right)$$

$$= 1.5\frac{1-\frac{1.5}{3}}{1.5\mu H * 4\times 10^6\,Hz}\left(\frac{1}{8 * 9.4\mu F * 4\times 10^6\,Hz} + 5m\Omega\right) \approx 1.0mV \tag{3-6}$$

The RMS current values of the PFET and NFET power switches current are calculated with (3-7) and (3-8).

$$I_{rms}^{PFET} \approx \sqrt{D}\sqrt{I_o^2 + \frac{\Delta i_L^2}{12}} = \sqrt{\frac{1.5}{3}} * \sqrt{0.4^2 + \frac{0.125^2}{12}} \approx 0.284A \tag{3-7}$$

$$I_{rms}^{NFET} \approx \sqrt{D'}\sqrt{I_o^2 + \frac{\Delta i_L^2}{12}} = \sqrt{\frac{3-1.5}{3}} * \sqrt{0.4^2 + \frac{0.125^2}{12}} \approx 0.284A \tag{3-8}$$

The power stage schematic of the designed 4MHz ISBC is illustrated in Figure 3-1.

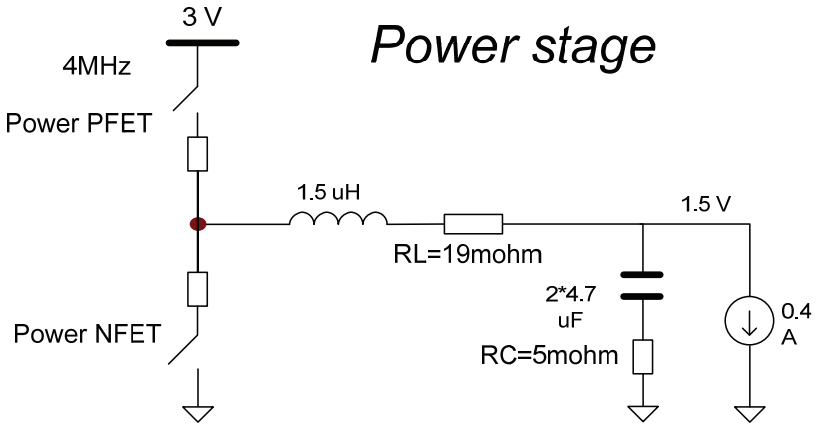

Figure 3-1. 4MHz ISBC power stage for a portable application.

3.1.3 PID controller

The ISBC will use a proportion-integral-difference (PID) controller when the output current is larger than 0.08A. If the output current is smaller than 0.08A, the ISBC will utilize another kind of controller - constant on-time control (output voltage hysteresis control) [3-8] and the ISBC will work in DCM mode with PFM modulation. This subsection will detail the design of a PID controller for the ISBC with Bode diagram analysis in the frequency domain.

3.1.3.1 Small signal transfer function

The symbols of components in the power stage for the small signal model of the power stage of an ISBC are illustrated in Figure 3-2.

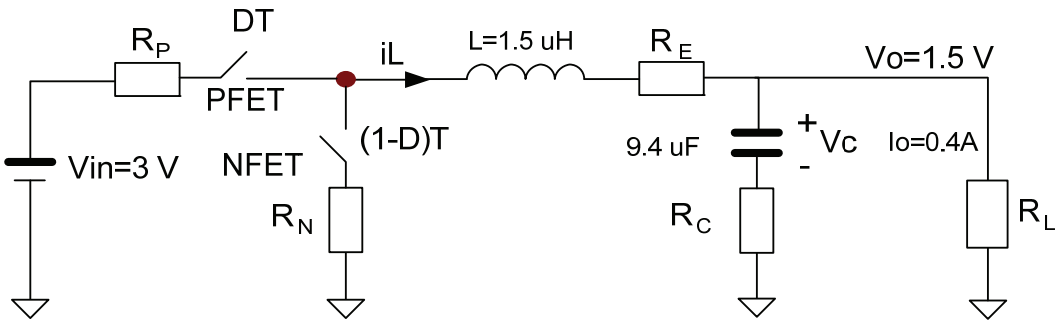

Figure 3-2 ISBC components for small signal modeling

V_{in} is the input voltage, V_o is the output voltage, R_L is the load resistance, i_o is the load current. L is the inductance of the power stage output filter, C is capacitance of the power stage output filter, D is the duty cycle. T is the switching period. i_L is the inductor current. V_C is the capacitor voltage. R_C is the ESR of the output capacitor, R_E

is the ESR of the output inductor, R_P is Rdson of the PFET, and R_N is Rdson of the NFET.

When the PFET switches on for a time period DT, equation (3-9) can be derived,

$$L\frac{di_L}{dt} = V_{in} - v_o - i_L\left(R_P + R_E\right), \quad C\frac{dv_C}{dt} = i_L - i_o, \;\; v_C = v_o - R_C C\frac{dv_C}{dt} \tag{3-9}$$

When the NFET switches on for a time period $(1-D)T$, equation (3-10) can be derived,

$$L\frac{di_L}{dt} = -v_o - i_L\left(R_N + R_E\right), \quad C\frac{dV_C}{dt} = i_L - i_o, \;\; V_C = v_o - R_C C\frac{dv_C}{dt} \tag{3-10}$$

Thus, the averaged equations for one period are,

$$L\frac{di_L}{dt} = DV_{in} - v_o - i_L\left(DR_P + D'R_N + R_E\right) \tag{3-11}$$

$$C\frac{dv_o}{dt} = i_L - i_o + R_C C\frac{d\left(i_L - i_o\right)}{dt} \tag{3-12}$$

$$i_o = \frac{v_o}{R_L} \tag{3-13}$$

The steady state solutions of duty cycle and inductance current are given by (3-14) and (3-15).

$$V_o = \frac{DV_{in}R_L}{R_L + DR_P + D'R_N + R_E} \;\Rightarrow\; D = \frac{V_o\left(R_L + R_N + R_E\right)}{V_{in}R_L + V_o\left(R_N - R_P\right)}, \text{ if } R_P = R_N. \tag{3-15}$$

$$I_L = I_o = \frac{V_o}{R_L} = \frac{DV_{in}}{R_L + DR_P + D'R_N + R_E} \tag{3-16}$$

The small signal transfer function around the steady state value will be derived by the linear perturbation theory, and are given in (3-17) and (3-18).

$$L\frac{d\hat{i}_L}{dt}+\hat{i}_L\left(DR_P+D'R_N+R_E\right)=D\hat{v}_{in}-\hat{v}_o+\hat{d}\left[V_{in}+I_L\left(R_N-R_P\right)\right] \tag{3-17}$$

$$\left(1+\frac{R_C}{R_L}\right)C\frac{d\hat{v}_o}{dt}=\hat{i}_L+R_CC\frac{d\hat{i}_L}{dt}-\frac{\hat{v}_o}{R_L}+\frac{V_o}{R_L^2}\hat{R}_L \tag{3-18}$$

The small signal transfer function in the S-domain is given as:

$$A_{\hat{v}_o\hat{d}}=\frac{R_L\left[V_{in}+I_L\left(R_N-R_P\right)\right]\left(R_CC\,s+1\right)}{A_{11}\,s^2+A_{12}\,s+A_{13}} \tag{3-19}$$

$$A_{\hat{v}_o\hat{R}_L}=\frac{\dfrac{DV_{in}}{R_L+DR_P+D'R_N+R_E}\left(L\,s+DR_P+D'R_N+R_E\right)}{A_{11}\,s^2+A_{12}\,s+A_{13}} \tag{3-20}$$

in which $A_{11}=\left(R_L+R_C\right)LC$, $A_{12}=[L+R_LR_CC+(R_L+R_C)\left(DR_P+D'R_N+R_E\right)C]$,

$A_{13}=\left(R_L+DR_P+D'R_N+R_E\right)$

For the nominal working condition $V_{in}=3$, $V_o=1.5$, $R_L=3.75$, $L=1.5\times10^{-6}$, $C=9.4\times10^{-6}$, $R_C=5\times10^{-3}$, $R_E=19\times10^{-3}$, $R_P=50\times10^{-3}$, $R_N=50\times10^{-3}$. We obtain that $D=0.5092$, and $I_L=0.4$. The duty cycle to output voltage small signal transfer function, given these parameters, is listed in (3-21).

$$A_{\hat{v}_o\hat{d}}=\frac{11.25\left(4.7\times10^{-8}\,s+1\right)}{5.29\times10^{-11}s^2+4.11\times10^{-6}\,s+3.82}=\frac{1.0\times10^4\left(s+2.13\times10^7\right)}{s^2+7.77\times10^4\,s+7.22\times10^{10}} \tag{3-21}$$

When $L=1.2\times10^{-6}$ and $R_E=21\times10^{-3}$,

$$A_{\hat{v}_o\hat{d}}=\frac{11.25\left(4.7\times10^{-8}\,s+1\right)}{4.24\times10^{-11}s^2+3.88\times10^{-6}\,s+3.82}=\frac{1.25\times10^4\left(s+2.13\times10^7\right)}{s^2+9.15\times10^4\,s+9.01\times10^{10}}$$

The Bode diagram of the transfer function is depicted in Figure 3-3.

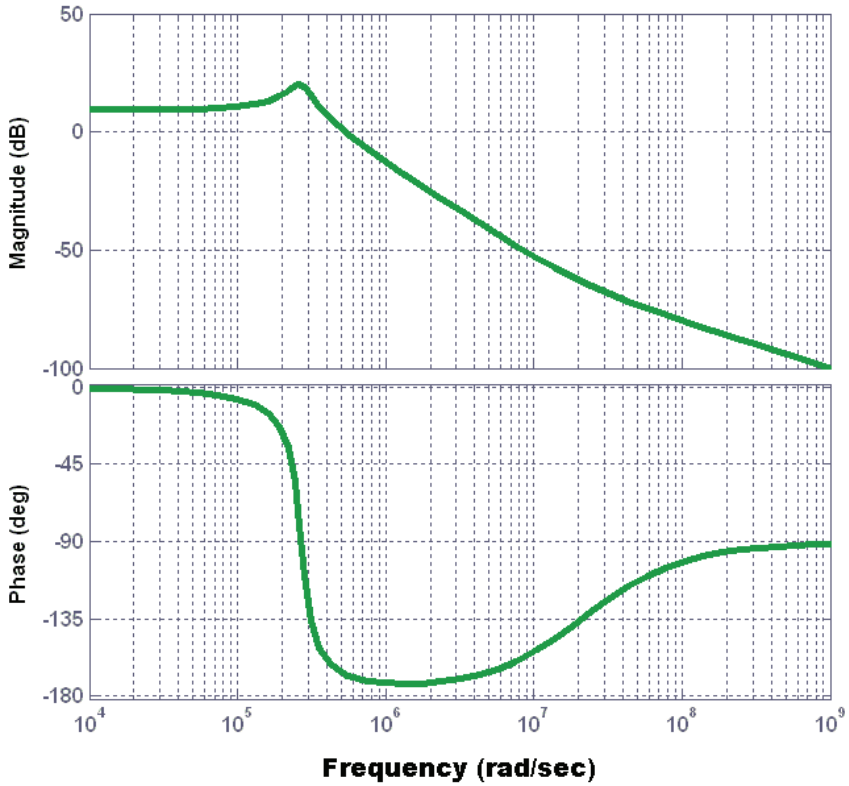

Figure 3-3. Bode diagram of the ISBC power stage

3.1.3.2 PID compensator

The PID compensator is implemented with a type 3 filter and an operational amplifier (Opamp) as illustrated in Figure 3-4.

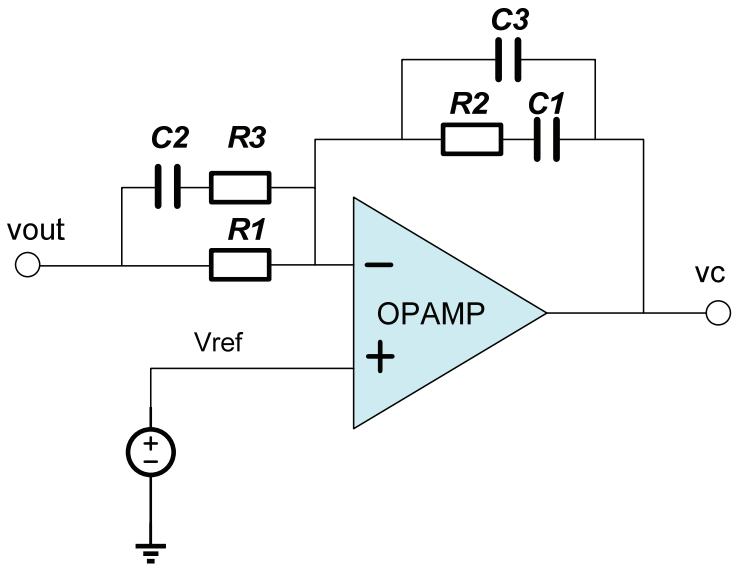

Figure 3-4. Type-III PID compensator and parameters

The transfer function of the PID controller is given in (3-22).

$$C(s)=\frac{\omega_1\left(1+\frac{s}{\omega_{Z1}}\right)\left(1+\frac{s}{\omega_{Z2}}\right)}{s\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)}, \tag{3-22}$$

in which $\omega_1=\frac{1}{R_1(C_1+C_3)}$, $\omega_{Z1}=\frac{1}{R_2C_1}$, $\omega_{Z2}=\frac{1}{C_2(R_1+R_3)}$, $\omega_{P1}=\frac{1}{R_3C_2}$, and $\omega_{P2}=\frac{1}{R_2\frac{C_1C_3}{C_1+C_3}}$.

Utilizing Matlab simulator, the controller is designed with the coefficients given in (3-23), and the loop gain transfer function Bode diagram of the ISBC with the controller is

shown in Figure 3-5. The phase margin is 61.2° and the crossover frequency is 34,537Hz, both of which satisfy the system specification.

$R_1 = 1M\Omega$, $R_2 = 5M\Omega$, $R_3 = 50K\Omega$, $C_1 = 1pF$, $C_2 = 2pF$, $C_3 = 10fF$, $\omega_1 = 9.9\times10^5\, rad/\sec$, $\omega_{Z1} = 2\times10^5\, rad/\sec$, $\omega_{Z2} = 4.76\times10^5\, rad/\sec$, $\omega_{P1} = 1\times10^7\, rad/\sec$, $\omega_{P2} = 2.02\times10^7\, rad/\sec$

$$C(s) = \frac{9.9\times10^5\left(1+\frac{s}{2\times10^5}\right)\left(1+\frac{s}{4.76\times10^5}\right)}{s\left(1+\frac{s}{1\times10^7}\right)\left(1+\frac{s}{2.02\times10^7}\right)} \tag{3-23}$$

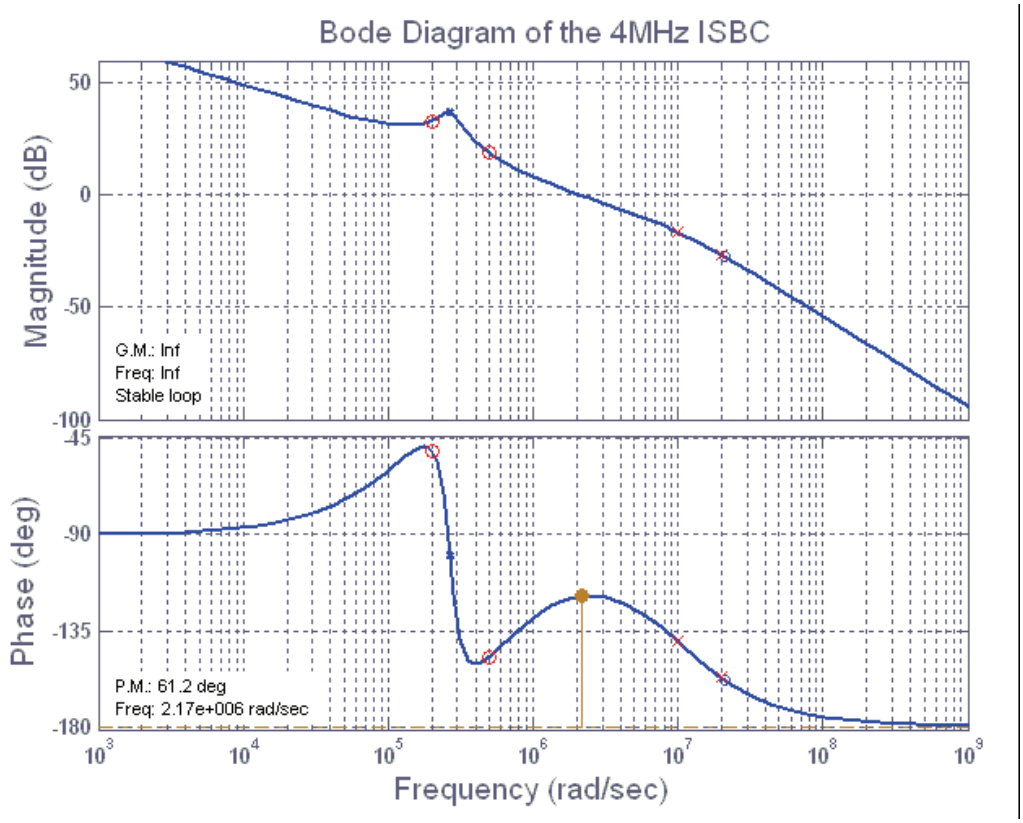

Figure 3-5. Bode diagram of loop gain transfer function

3.1.3.3 Transient response simulation

The transient response of the ISBC with the controller designed in subsection 3.1.3.2 was tested with up and down load current steps with a slew rate of $32A/\mu s$. The test result is shown in Figure 3-6. The maximum output voltage deviation is 27 mV, which satisfies the specification.

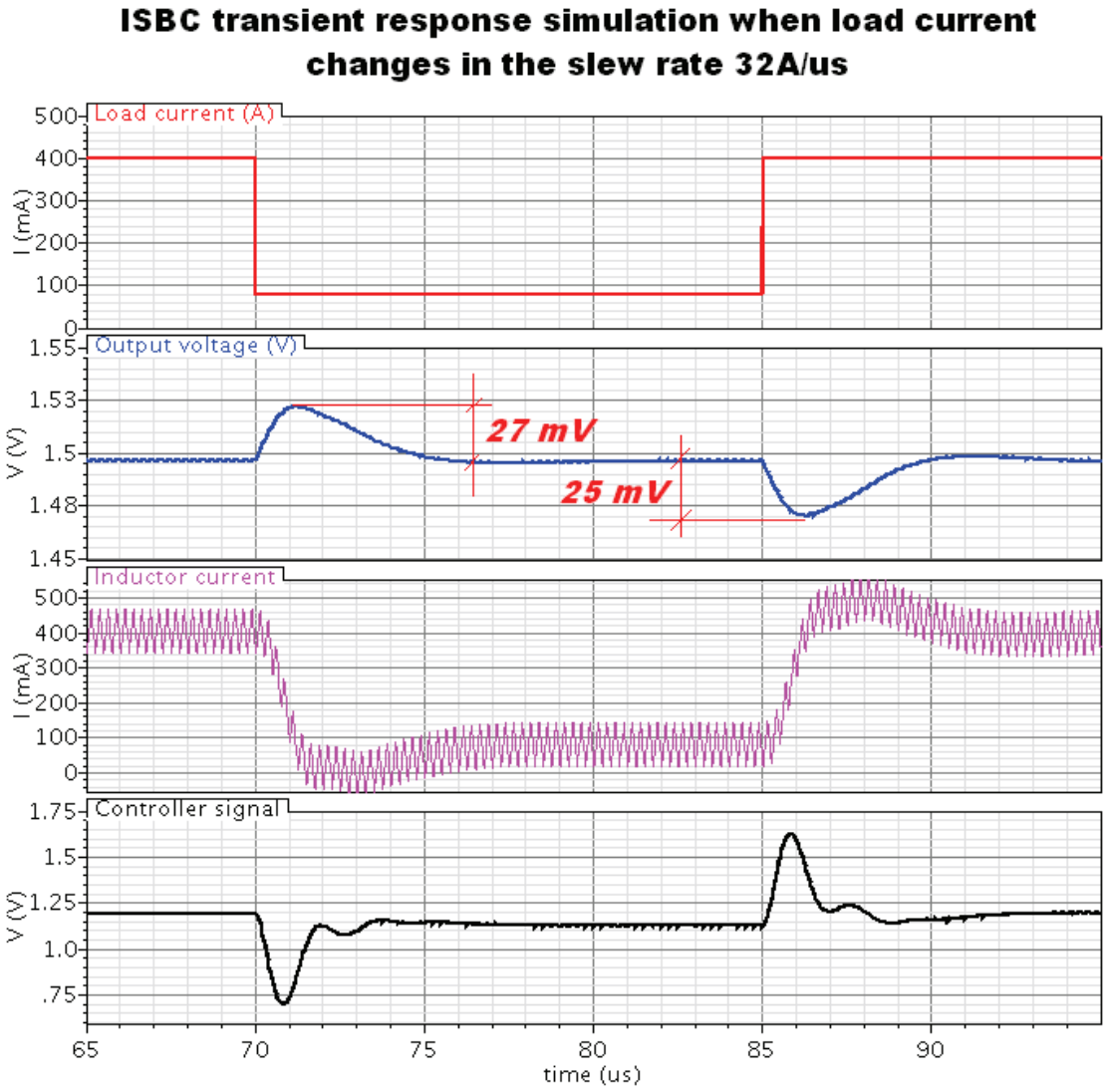

Figure 3-6. Transient response of the ISBC when load current step changes up and down

3.2 Power FET optimal sizing

In order to maximize operation time of the battery in portable devices, the power conversion efficiency of ISBC will be optimized in the whole range of load current.

In the dissertation, the power FET size is designed to achieve the maximum power efficiency at the working condition with the maximum load current, because in the situation the absolute value of power loss is the highest in comparison with other load conditions. When the load current is lower than the maximum one, we can improve the efficiency via some circuit techniques introduced in the subsection 1.2.4. In the dissertation, we will use both the power width segmentation technique and the PFM mode technique to improve the ISBC efficiency when the load current is smaller than the maximum one.

From the chapter 1, it is introduced that the major two power losses components relative to the power FET width include the switching loss and the conduction loss. Thus, the optimal sizing of the power FET is in fact the process minimizing the sum of the switching loss and the conduction loss or 50%-50% balancing two of them.

3.2.1 Switching loss

Following the analysis in Chapter 2, the switching loss consists of O_loss, C_loss and D_loss. In this subsection, the coefficients in the Chapter 2 will be specified with the extracted parameters in Table 2- for AMI06 standard CMOS technology.

3.2.1.1 O_loss

Equation (3-24) is the specified version of the equation (2-20) for O_loss energy loss calculation for unit power FET width. The analysis does not include the O_loss when the

PFET turns off, as the PFET driver is deliberately designed to eliminate the Miller plateau for the PFET turn-off event.

$$E_{O\_loss} = \frac{3}{2}V_{dd}\left(I_o - \frac{1}{2}\Delta I_L\right)\frac{R_{unit}^{P}}{\varphi_{P\_P}}\left[\left(C_{gd\_p}^{(C)} + C_{gs\_P}^{(S)}\right)\ln\left(\frac{V_{dd} - V_{TH}^{P}}{V_g^{P\_on}}\right) + \frac{C_{gd\_P}^{(C)}V_{dd}}{V_g^{P\_on}}\right]$$

$$= \frac{3}{2}3\left(I_o - 0.0625\right)\frac{0.0135}{0.03}\left[\left(0.29376 + 1.0941\right)\ln\left(\frac{3 - 0.92}{V_g^{P\_on}}\right) + \frac{0.29376 * 3}{V_g^{P\_on}}\right]\times 10^{-9}$$

$$= 2.025\left(I_o - 0.0625\right)\left[1.3879\ln\left(\frac{2.08}{V_g^{P\_on}}\right) + \frac{0.8813}{V_g^{P\_on}}\right]\times 10^{-9} \quad J\cdot m^{-1} \tag{3-24}$$

Equation (3-25) is the power loss calculation.

$$P_{O\_loss} = W_P^{active}E_{O\_loss}f_{SW} = W_P^{active}0.0081\left(I_o - 0.0625\right)\left[1.3879\ln\left(\frac{2.08}{V_g^{P\_on}}\right) + \frac{0.8813}{V_g^{P\_on}}\right] \quad W \tag{3-25}$$

The gate voltage level for the Miller plateau is calculated with (3-26).

$$V_g^{P\_on} = \frac{z_1 + 2K_P z_2 - \sqrt{z_1^{\,2} + 4K_P\left[z_1 z_2 + \frac{\left(I_o - \frac{\Delta I_L}{2}\right)}{W_P^{active}}\right]}}{2K_P} \tag{3-26}$$

$$= \frac{z_1 + 2*82.63*z_2 - \sqrt{z_1^{\,2} + 4*82.63*\left[z_1 z_2 + \frac{\left(I_o - 0.0625\right)}{W_P^{active}}\right]}}{2*82.63}$$

in which,

$$z_1 = \frac{\varphi_{P\_P}}{3R_{unit}^{P}}\frac{\left(C_{gd\_p}^{(C)} + C_{gd\_n}^{(C)}\frac{W_N}{W_P^{active}} + C_{db\_n}\frac{W_N}{W_P^{active}} + C_{db\_p}\frac{W_P}{W_P^{active}}\right)}{C_{gd\_p}^{(C)}}$$

$$= \frac{0.03}{3*0.0135}\frac{\left(0.29376 + 0.23924\frac{W_N}{W_P^{active}} + 0.9461\frac{W_N}{W_P^{active}} + 1.1301\frac{W_P}{W_P^{active}}\right)}{0.29376}$$

$$= 0.7407 + \frac{\left(2.9889\,W_N + 2.8496\,W_P\right)}{W_P^{active}} \tag{3-27}$$

$$z_2 = V_{dd} - V_{TH}^P = 3 - 0.92 = 2.08 \tag{3-28}$$

$$K_P = \frac{\mu_P \varepsilon_{ox}}{t_{ox} L} \approx \frac{202.454 cm^2/V\cdot s * 3.9 * 8.854\times10^{-12} F/m}{1.41\times10^{-8} m * 0.6\times10^{-6} m} = 82.63\, A/m\cdot V^2 \tag{3-29}$$

3.2.1.2 C_loss

Equation (3-30) is the equation for total C_loss energy calculation for unit power FET width.

$$E_{C\_loss} = W_P^{active} E_{C\_loss}^{P\_active} + W_N^{active} E_{C\_loss}^{N\_active} + W_P^{inactive} E_{C\_loss}^{P\_inactive} + W_N^{inactive} E_{C\_loss}^{N\_inactive} \tag{3-30}$$

Substituting the extracted parameters in Table 2-, the items in (3-30) are calculated by,

$$E_{C\_loss}^{P\_active} = C_{gd\_p}^{(L)} V_{dd}^2 + 0.5 C_{gd\_p}^{(C)} \left(V_{dd}^2 + 2V_{diode}^{Forward} V_{dd} + V_{diode}^{Forward\,2}\right) + C_{gs\_p}^{(L)} V_{dd}^2 + 0.5 C_{db\_P}\left(V_{dd} + V_{diode}^{Forward}\right)^2 \tag{3-31}$$

$$= \left[0.894*9 + 0.5*0.29376*\left(9 + 1.3*3 + 0.423\right) + 0.894*9\right]\times10^{-9} + 0.5*1.1301*\left(9 + 1.3*3 + 0.423\right)\times10^{-9}$$

$$= 25.5768\times10^{-9}\ J\cdot m^{-1}$$

$$E_{C\_loss}^{P\_inactive} = 0.5\left(C_{gd\_p}^{(C)} + C_{db\_P}\right)\left(V_{dd} + V_{diode}^{Forward}\right)^2 = 9.4847\times10^{-9}\ J\cdot m^{-1} \tag{3-32}$$

$$E_{C\_loss}^{N\_active} = C_{gd\_n}^{(L)} V_{dd}^2 + 0.5 C_{gd\_n}^{(C)} V_{dd}^2 + C_{gs\_n}^{(L)} V_{dd}^2 + 0.5 C_{db\_n} V_{dd}^2 + 2E_{rr} \tag{3-33}$$

$$= \left(0.856*9 + 0.5*0.23924*9 + 0.856*9 + 0.5*0.9461*9 + 2*0.48521\right)\times10^{-9}$$

$$= 21.7132\times10^{-9}\ J\cdot m^{-1}$$

$$E_{C\_loss}^{N\_inactive} = 0.5C_{gd\_n}^{(C)}\left(V_{dd}^2 + 2*V_{diode}^{Forward\,2}\right) + 0.5C_{db\_n}V_{dd}^2 + 2E_{rr} \quad (3\text{-}34)$$

$$= \left[0.5*0.23924*(9+0.845) + 0.5*0.9461*9 + 2*0.48521\right]\times 10^{-9}$$

$$= 6.4055\times 10^{-9}\ J\cdot m^{-1}$$

The relative power loss is calculated with (3-35).

$$P_{C\_loss} = E_{C\_loss} f_{SW} \quad (3\text{-}35)$$

$$= \left(25.5768 W_P^{active} + 21.7132 W_N^{active} + 9.4847 W_P^{inactive} + 6.4055 W_N^{inactive}\right)\times 10^{-9} * f_{SW}$$

$$= 0.1023\, W_P^{active} + 0.0869\, W_N^{active} + 0.0379 W_P^{inactive} + 0.0256\, W_N^{inactive} \quad W$$

3.2.1.3 D_loss

Equation (3-36) is from equation (2-113) to calculate D_loss energy for unit power FET width.

$$P_{D\_loss} = \quad (3\text{-}36)$$

$$= \frac{5}{4}V_{dd}^2\left[\left(C_{gd\_p}^{(L)} + C_{gd\_p}^{(C)} + C_{gs\_p}^{(L)} + C_{db\_p}\right) + \frac{1}{3}\left(C_{gd\_n}^{(L)} + C_{gd\_n}^{(C)} + C_{gs\_n}^{(L)} + C_{db\_n}\right)\right] *$$

$$* \left(\varphi_{P\_P} W_P^{active} + 3\varphi_{N\_N} W_N^{active}\right) * f_{SW}$$

$$= \frac{5}{4} * 9 * \left[\left(0.894 + 0.29376 + 0.894 + 1.1301\right) + \frac{1}{3}\left(0.856 + 0.23924 + 0.856 + 0.9461\right)\right]\times 10^{-9}$$

$$* 0.03\left(W_P^{active} + W_N^{active}\right) * 4\times 10^6$$

$$= 0.0056\left(W_P^{active} + W_N^{active}\right) \quad W$$

3.2.1.4 Total switching power loss

The total switching power loss is the sum of (3-25), (3-35) and (3-36). It is listed in (3-37).

$$P_{SW} = P_{O\_loss} + P_{C\_loss} + P_{D\_loss} \tag{3-37}$$
$$= (0.1023 + \alpha_P) W_P^{active} + 0.0925\, W_N^{active} + 0.0379 W_P^{inactive} + 0.0256\, W_N^{inactive}$$

in which $\alpha_P = 0.0081(I_o - 0.0625)\left[1.3879 \ln\left(\frac{2.08}{V_g^{P\_on}}\right) + \frac{0.8813}{V_g^{P\_on}}\right]$ (3-38)

3.2.2 Power FET conduction loss

The power FET conduction loss is calculated with the RMS value of current conducted in the power FET. The RMS value was introduced in (3-7) and (3-8). The conduction loss is given in (3-39)

$$P_{conduction} = P_{conduction}^{P} + P_{conduction}^{N} = I_{rms}^{PFET\,2} R^P + I_{rms}^{NFET\,2} R^N \tag{3-39}$$
$$= \left[\frac{0.197 * 0.5}{(1 + 4.54 * V_{dd}) W_P^{active}} + \frac{0.0122 * 0.5}{(1 + 0.625 * V_{dd}) W_N^{active}}\right] * \left(I_o^2 + \frac{\Delta I_o^2}{12}\right)$$
$$= \left[\frac{0.0067}{W_P^{active}} + \frac{0.0021}{W_N^{active}}\right] * (I_o^2 + 0.0013) \quad W$$

3.2.3 Optimal power FET sizing

We optimize the value of W_P and W_N in the ISBC for the heaviest load condition ($I_o = 0.4$). The optimal power FET size results in the minimal value of equation (3-40)

$$P_{loss}^{optimize} = P_{SW} + P_{conduction} \tag{3-40}$$

$$= \left(0.1023 + \alpha_P^{(op)}\right) W_P + 0.0925 W_N + \left[\frac{0.0067}{W_P} + \frac{0.0021}{W_N}\right]\left(I_o^2 + 0.0013\right) \quad W$$

$$= \left(0.1023 + \alpha_P^{(op)}\right) W_P + \frac{0.0011}{W_P} + 0.0925\, W_N + \frac{0.00034293}{W_N}$$

in which

$$\alpha_P^{(op)} = 0.0034 \ln\left(\frac{2.08}{V_g^{P\_on(op)}}\right) + \frac{0.0021}{V_g^{P\_on(op)}}$$

$$V_g^{P\_on(op)} = 2.08 + \frac{z_1^{(op)} - \sqrt{z_1^{(op)2} + 330.52 * \left[2.08\, z_1^{(op)} + \frac{0.3375}{W_P}\right]}}{165.26}$$

$$z_1^{(op)} = 3.5903 + 2.9889 \frac{W_N}{W_P}$$

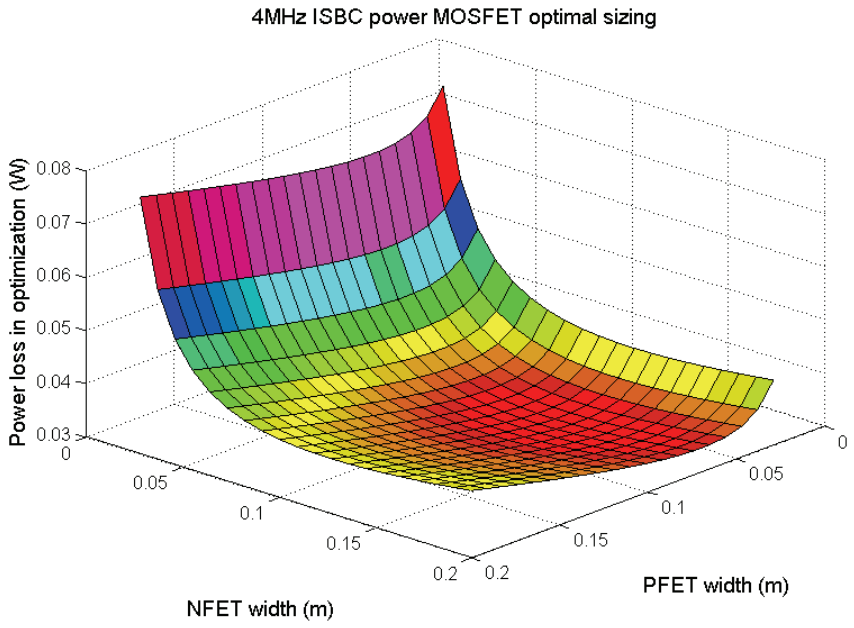

Figure 3-7. 3-dimension value of the power loss specified in (3-40)

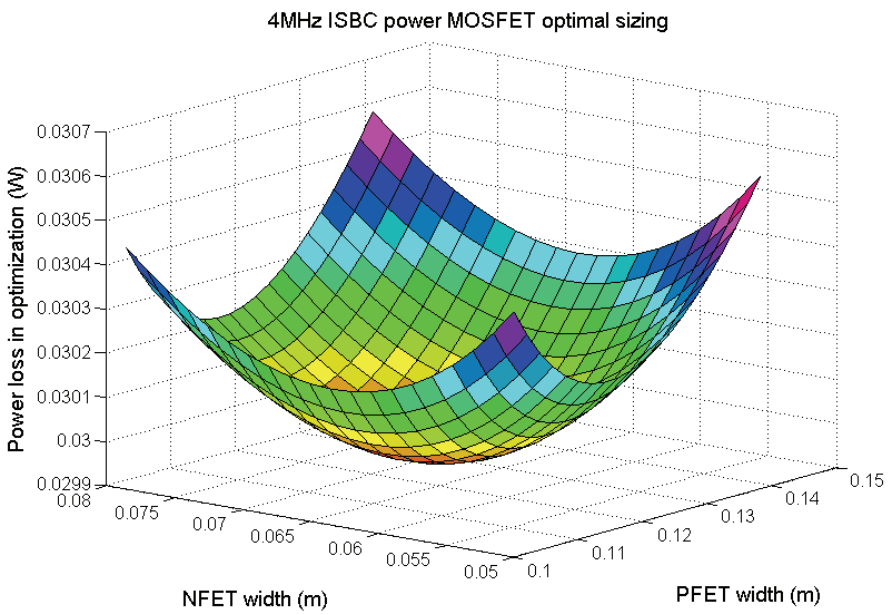

Figure 3-8. Zoomed-in version of Figure 3-7.

Figure 3-7 shows the 3-dimension surface of the power loss specified in (3-40) and Figure 3-8 is the zoomed-in version of Figure 3-7. The valley of the power loss surface indicates the optimal size of power FET and the corresponding values are given by (3-41).

$$W_P = 0.110 \quad m\,,\ W_N = 0.055 \quad m \tag{3-41}$$

We notice that the power loss surface in Figure 3-7 looks like a bowl with almost flat bottom. Thus, there will be not much difference about the value of the power loss, provided that the power FET widths are located in a region in corresponding to the bottom of the bowl in the Figure3-8. This observation explains the fact why in present there are so many different versions of power loss calculation equations in other works even if in these equations the O_loss, C_loss and D_loss had not been separated. Some of the equations might provide good power losses prediction for one ISBC in a given working condition and a given semiconductor technology, but have to be remarkably modified in other working conditions or other semiconductor technologies.

3.3 Load efficiency curve

The optimal power FET width is determined in subsection 3.2. On the basis of the optimized size, this subsection will investigate the power conversion efficiency of the ISBC for a wide range of load currents, detailing all of major power losses components. In order to improve power efficiency, the ISBC has been intentionally designed to eliminate the PFET turn-off O_loss. In this subsection, segmentation technique will not be included.

3.3.1 Switching loss

The power loss relative to O_loss is given in (3-42)

$$P_{O\_loss} = W_P^{active}\, 0.0081\left(I_o - 0.0625\right)\left[1.3879\ln\left(\frac{2.08}{V_g^{P\_on}}\right) + \frac{0.8813}{V_g^{P\_on}}\right] \tag{3-42}$$

$$= 9.639\times 10^{-4}\left(I_o - 0.0625\right)\left[1.3879\ln\left(\frac{2.08}{V_g^{P\_on}}\right) + \frac{0.8813}{V_g^{P\_on}}\right] \quad W$$

in which $z_1 = 0.7407 + \dfrac{\left(2.9889\, W_N + 2.8496\, W_P\right)}{W_P} = 5.085$,

$$z_2 = V_{dd} - V_{TH}^P = 3 - 0.92 = 2.08$$

$$V_g^{P\_on} = \frac{z_1 + 2*82.63*z_2 - \sqrt{z_1^{\,2} + 4*82.63*\left[z_1 z_2 + \dfrac{\left(I_o - 0.0625\right)}{W_P^{active}}\right]}}{2*82.63}$$

$$= 2.1108 - \sqrt{0.1221 + 0.11*I_o}$$

The power loss relative to C_loss is given in (3-43)

$$P_{C\_loss} = 0.1023\, W_P^{active} + 0.0869\, W_N^{active} + 0.0379 W_P^{inactive} + 0.0256\, W_N^{inactive} \quad (3\text{-}43)$$
$$= 0.016 \quad W$$

The power loss relative to D_loss is given in (3-44)

$$P_{D\_loss} = 0.0056\left(W_P^{active} + W_N^{active}\right) = 0.000924 \quad W \quad (3\text{-}44)$$

3.3.2 Power FET Conduction loss

The power MOFET conduction loss is calculated with (3-45)

$$P_{conduction} = \left[\frac{0.0067}{W_P^{active}} + \frac{0.0021}{W_N^{active}}\right] * \left(I_o^2 + \frac{\Delta I_o^2}{12}\right) = 0.0991 * \left(I_o^2 + 0.0013\right) \quad W \quad (3\text{-}45)$$

3.3.3 Dead-time conduction loss

The dead-time setting is an important design parameter for an ISBC to avoid power FET shoot through or malfunction due to severe voltage oscillations; the two parameters $t_{dead}^{1\_set}$, $t_{dead}^{1\_set}$ have been introduced in the chapter 1. There is a tradeoff involved in choosing the value of $t_{dead}^{1\_set}$, $t_{dead}^{1\_set}$. On one hand, a conservative setting of $t_{dead}^{1\_set}$ and $t_{dead}^{1\_set}$ will result in too much conduction time of the NFET body diode resulting in a degraded efficiency. On the other hand, an aggressive setting of $t_{dead}^{1\_set}$ and $t_{dead}^{1\_set}$ increases the risk of shoot through for some operating conditions. If we can develop a theoretical analysis for dead-time, it is possible for us to apply an optimal design for an ISBC for a specific semiconductor technology. Unfortunately, a method to analytically derive suitable values for $t_{dead}^{1\_set}$, $t_{dead}^{1\_set}$ has not been discussed in detail. A popular way to set deadtime values is to follow a thumb rule (for example, 10ns for a >1MHz ISBC) and

then to apply a trial-by-trial modification on the basis of simulation or experimental measurement.

In subsection 2.3.2.4 and 2.3.4.2, a theoretical method has been developed to determine the minimal value of $t_{dead}^{1\_set}$ and $t_{dead}^{2\_set}$. The value of $t_{dead}^{1\_set}$ is calculated with (2-51) and $t_{dead}^{2\_set}$ is calculated with (2-40). We substitute the ISBC data into (2-51) and (2-40) and obtain the specific value of $t_{dead}^{1\_set}$ and $t_{dead}^{1\_set}$ in (3-46) and (3-49).

$$t_{dead}^{1\_set} = t_{o1} + 2.5\times10^{-9} = 3.08\times10^{-9}\ s \tag{3-46}$$

$$= \frac{0.0042}{0.01} * 2 * 0.856\times10^{-9} * \ln\left(\frac{2*3}{0.67}\right) + 2.5\times10^{-9} = 4.08\times10^{-9} s$$

$$t_{o3} = \frac{R_{unit}^{P}}{\varphi_{P\_P}}\left(C_{gd\_p}^{(L)} + C_{gs\_p}^{(L)}\right)\ln\frac{2V_{dd}}{V_{TH}^{P}} \tag{3-47}$$

$$= \frac{0.0135}{0.03} * 2 * 0.894\times10^{-9} * \ln(\frac{2*3}{0.92}) = 1.51\times10^{-9}\ s$$

$$t_{o4} = \frac{\left(C_{gd\_p}^{(C)}W_P + C_{gd\_n}^{(C)}W_N + C_{db\_p}W_P + C_{db\_n}W_N\right)\left(V_{dd} + V_{diode}^{Forward}\right)}{\left(I_o^{(CCM\_critical)} + \frac{1}{2}\Delta I_L\right)} \tag{3-48}$$

$$= \frac{\left(0.29376*0.11 + 0.23924*0.055 + 1.1301*0.11 + 0.9461*0.055\right)\times10^{-9} * 3.65}{0.08 + 0.0625}$$

$$= 5.68\times10^{-9} \quad s$$

$$t_{dead}^{2\_set} = t_{o3} + t_{o4} = 1.51\times10^{-9} + 5.68\times10^{-9} = 7.19\times10^{-9}\ s \tag{3-49}$$

The dead-time conduction loss should be calculated with the practical value of power NFET body diode conduction time. t_{o1} and t_{o3} are values independent of the load current, so they will not make a contribution for the practical power NFET body diode conduction time. On the contrary, t_{o2} in (2-50) and t_{o4} in (2-39) are approximately inversely proportional to the load current, and will generate a dead-time difference.

When the load current is larger than $I_o^{dead\_1}$ in (3-50), the value of t_{o2} will become smaller than $2.5\times10^{-9}\ s$ and the t_{dead}^1 will be generated as given in (3-51).

$$I_o^{dead\_1} = \frac{\left(C_{gd\_p}^{(C)}W_P + C_{gd\_n}^{(C)}W_N + C_{db\_p}W_P + C_{db\_n}W_N\right)V_{diode}^{Forward}}{2.5\times10^{-9}} + \frac{\Delta I_L}{2} \tag{3-50}$$

$$t_{dead}^1 = \begin{cases} 2.5\times10^{-9} - t_{o2} & I_o > I_o^{dead\_1} \\ 0 & I_o \le I_o^{dead\_1} \end{cases} \tag{3-51}$$

In contrast to t_{dead}^1, t_{dead}^2 always exists until the load current is equal to its minimal value 0.08A in CCM. The value of t_{dead}^2 is given in (3-52).

$$t_{dead}^2 = \frac{\left(C_{gd\_p}^{(C)}W_P + C_{gd\_n}^{(C)}W_N + C_{db\_p}W_P + C_{db\_n}W_N\right)\left(V_{dd} + V_{diode}^{Forward}\right)}{\left(I_o^{CCM\_critical)} + \frac{1}{2}\Delta I_L\right)\left(I_o + \frac{1}{2}\Delta I_L\right)}\left(I_o - I_o^{(CCM\_critical)}\right) \tag{3-52}$$

The dead-time conduction loss is calculated with t_{dead}^1 and t_{dead}^2 as in (3-53).

$$P_{deadtime} = \left(t_{dead}^1 + t_{dead}^2\right) I_o f_{SW} V_{diode}^{Forward} \tag{3-53}$$

For the particular ISBC in this dissertation and the AMI06 technology with the coefficients extracted in Table 2-18, we specify the concrete value of t_{dead}^1, t_{dead}^2 and $P_{deadtime}$ respectively in (3-54), (3-55) and (3-56).

$$t_{dead}^{1}=\begin{cases}2.5\times10^{-9}-\dfrac{1.442\times10^{-10}}{\left(I_o-0.0625\right)} & I_o>0.12A\\ 0 & I_o\le 0.12A\end{cases} \tag{3-54}$$

$$t_{dead}^{2}=\frac{5.68\times10^{-9}\left(I_o-0.08\right)}{\left(I_o+0.0625\right)} \tag{3-55}$$

$$P_{deadtime}=\left[t_{dead}^{1}*\left(I_o-\frac{\Delta I_L}{2}\right)+t_{dead}^{2}*\left(I_o+\frac{\Delta I_L}{2}\right)\right]*4\times10^{6}*0.65\quad W \tag{3-56}$$

3.3.4 Copper loss

The copper loss refers to conduction loss of the power inductor's parasitic direct current resistance and is calculated with (3-57).

$$P_{copper}=\left(I_o^2+\frac{\Delta I_o^2}{12}\right)R_E=0.019*\left(I_o^2+0.0013\right)\quad W \tag{3-57}$$

3.3.5 Circuit power loss

Circuit power loss refers to the total power consumption of all circuit function blocks when the ISBC works in CCM. The circuit power loss is calculated with (3-58).

$$P_{circuit}=I_{circuit}V_{dd}^{circuit} \tag{3-58}$$

in which $V_{dd}^{circuit}$ is the power supply voltage level of the circuits.

3.3.6 Total power loss and efficiency

The capacitor AC loss is significantly smaller than the other loss components and is not discussed here. The wire parasitic loss is out of the scope of this dissertation. Thus, the total power loss is given in (3-59)

$$P_{total} = P_{SW} + P_{conduction} + P_{deadtime} + P_{copper} + P_{circuit} \tag{3-59}$$

The power efficiency is calculated with equation (3-60).

$$\eta = \frac{P_{output}}{P_{input}} = \frac{V_o * I_o}{V_o * I_o + P_{total}} \tag{3-60}$$

The load efficiency curves of the 4MHz ISBC for three different working conditions listed in Table 3-2 are shown in Figure 3-9 on the basis of the transistor-level Cadence simulation data (Spectre simulator, BSIM3V3.1 level 49 Spice model, 100°C, TT corner) and the prediction data calculated with the proposed switching loss model. In the three working conditions, all power FET subcells are in active mode and the ISBC works in CCM operation mode.

Table 3-2. Three different working conditions for the comparison of the load efficiency curves based on model prediction and simulation.

	#1 condition	#2 condition	#3 condition
Vin (V)	3.0	3.0	2.4
Vout (V)	1.5	1.0	0.8

In Figure 3-9, the load efficiency curves on the basis of the simulation data are labeled with rectangle symbols, while the curves on the basis of the prediction data are labeled with star symbols.

It is observed in Figure 3-9, the curves on the basis of the prediction data have a very close match with those on the basis of the simulation data for the #1 and #2 test working conditions. In comparison with the #1 and #2 conditions, the matching is a little bit worse for the #3 test working condition. The reason is that the diode forward voltage in the ISBC had been assumed to be a constant value 0.65V without relation to the load current when we did the losses analysis. The assumption will degrade the matching accuracy when the input voltage and output voltage of the ISBC are not far larger than 0.65V.

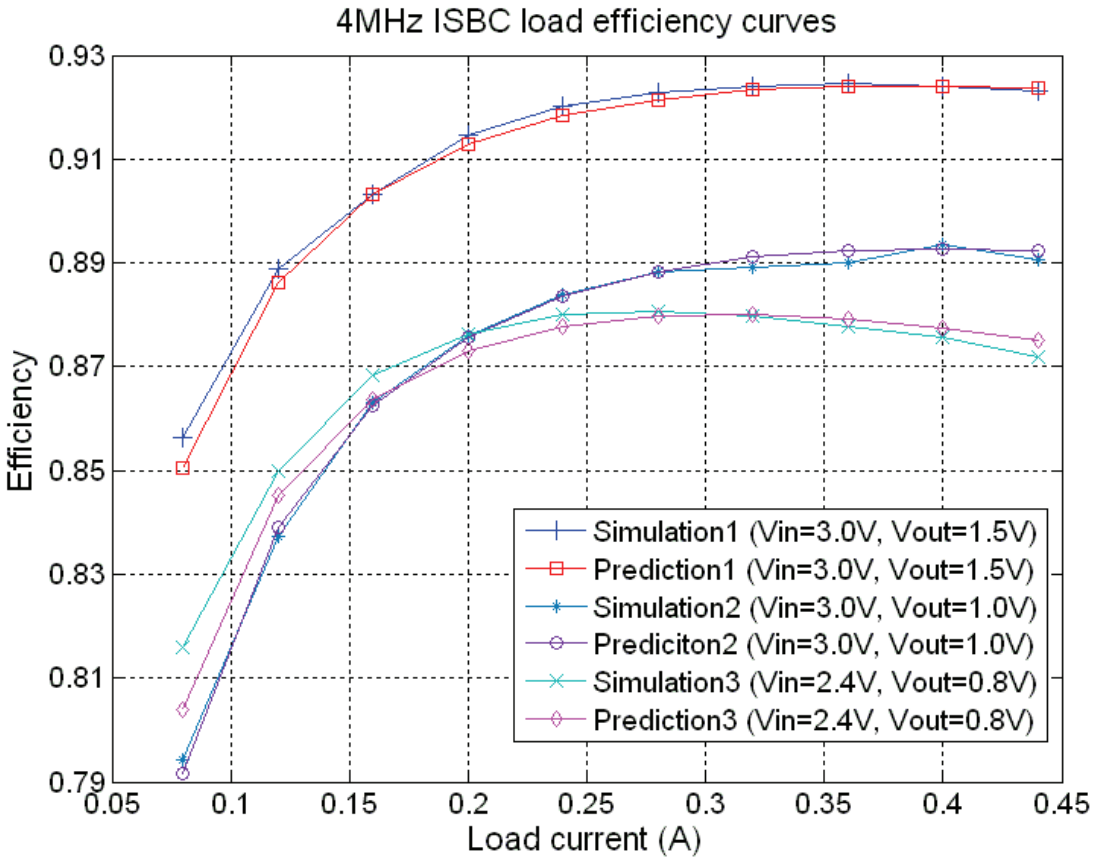

Figure 3-9 Model prediction and simulation based load efficiency curves of 4MHz ISBC for three different working conditions

3.4 Segmentation and power loss

Turning off part of power FET subcells is beneficial for the improvement of power conversion efficiency when load current decreases.

If only m power FET cells are active, the active power FET width will be given by (3-61) and (3-62) for the PFET and NFET respectively. Consequently, the inactive power FET width will be given by (3-63) and (3-64).

$$W_P^{active} = \frac{m}{32} W_P \tag{3-61}$$

$$W_N^{active} = \frac{m}{32} W_N \tag{3-62}$$

$$W_P^{inactive} = \frac{32-m}{32} W_P \tag{3-63}$$

$$W_N^{inactive} = \frac{32-m}{32} W_N \tag{3-64}$$

3.4.1 Switching loss

Substituting (3-61) into (3-25), O_loss is calculated with (3-65)

$$P_{O\_loss} = W_P^{active} E_{O\_loss} f_{SW} = \frac{m}{32} W_P 0.0081 \left(I_o - 0.0625\right) \left[1.3879 \ln\left(\frac{2.08}{V_g^{P\_on}} \right) + \frac{0.8813}{V_g^{P\_on}} \right] \tag{3-65}$$

$$V_g^{P\_on} = \frac{z_1 + 2*82.63*z_2 - \sqrt{z_1^{\,2} + 4*82.63*\left[z_1 z_2 + \frac{\left(I_o - 0.0.625\right)}{W_P^{active}} \right]}}{2*82.63} \tag{3-66}$$

$$= \frac{z_1 + 2*82.63*z_2 - \sqrt{z_1^{\,2} + 4*82.63*\left[z_1 z_2 + \dfrac{32(I_o - 0.0625)}{mW_P}\right]}}{2*82.63}$$

$$z_1 = \frac{\varphi_{P\_P}}{3R_{unit}^{P}} \frac{\left(C_{gd\_p}^{(C)} + C_{gd\_n}^{(C)} \dfrac{W_N}{W_P^{active}} + C_{db\_n} \dfrac{W_N}{W_P^{active}} + C_{db\_p} \dfrac{W_P}{W_P^{active}}\right)}{C_{gd\_p}^{(C)}} \tag{3-67}$$

$$= \frac{0.03}{3*0.0135} \frac{\left(0.29376 + 0.23924 \dfrac{W_N}{W_P^{active}} + 0.9461 \dfrac{W_N}{W_P^{active}} + 1.1301 \dfrac{W_P}{W_P^{active}}\right)}{0.29376}$$

$$= 2.5216\left(0.29376 + 37.9309 \frac{W_N}{mW_P} + \frac{36.1632}{m}\right)$$

Substituting (3-61), (3-62), (3-63) and (3-64) into (3-35), C _loss is calculated with (3-68)

$$\begin{aligned} P_{C\_loss} &= E_{C\_loss} f_{SW} \\ &= 0.1023\, W_P^{active} + 0.0869\, W_N^{active} + 0.0379 W_P^{inactive} + 0.0256\, W_N^{inactive} \\ &= (0.0379 + 0.0020m)W_P + (0.0256 + 0.0019\, m)\, W_N \end{aligned} \tag{3-68}$$

Substituting (3-61) and (3-62) into (3-36), D _loss is calculated with (3-69)

$$P_{D\_loss} = 0.0056\left(W_P^{active} + W_N^{active}\right) = 1.8 \times 10^{-4}\, m\, (W_P + W_N) \tag{3-69}$$

The total switching loss is in (3-70).

$$P_{SW} = P_{O\_loss} + P_{C\_loss} + P_{D\_loss} \tag{3-70}$$

$$= mW_P \frac{\alpha_P}{32} + (0.0379 + 0.0020m)W_P + (0.0256 + 0.0019m)W_N + 1.8 \times 10^{-4} m(W_P + W_N)$$

$$= m\left[\left(\frac{\alpha_P}{32}+0.00218\right)W_P + 0.00208W_N\right] + 0.0379W_P + 0.0256W_N$$

in which $\alpha_P = 0.0081\left(I_o - 0.0625\right)\left[1.3879\ln\left(\frac{2.08}{V_g^{P\_on}}\right)+\frac{0.8813}{V_g^{P\_on}}\right]$.

3.4.2 Conduction loss

Conduction loss for the ISBC with m active power FET cells is given in (3-71).

$$P_{conduction} = \left[\frac{0.0067}{W_P^{active}}+\frac{0.0021}{W_N^{active}}\right] * \left(I_o^2 + \frac{\Delta I_o^2}{12}\right) = \frac{1}{m}\left(\frac{0.2144}{W_P}+\frac{0.0672}{W_N}\right)\left(I_o^2 + 0.0013\right) \tag{3-71}$$

3.4.3 Total loss

The total losses of an ISBC with m active power FET cells is calculated in (3-72).

$$P_{loss}^{total} = m\left[\left(\frac{\alpha_P}{32}+0.00218\right)W_P + 0.00208W_N\right] + 0.0379W_P + 0.0256W_N \tag{3-72}$$
$$+\frac{1}{m}\left(\frac{0.2144}{W_P}+\frac{0.0672}{W_N}\right)\left(I_o^2 + 0.0013\right) + P_{deadtime} + P_{copper} + P_{circuit}$$

in which $P_{deadtime}$, P_{copper}, and $P_{circuit}$ are given in (3-56), (3-57) and (3-58).

3.4.4 Load efficiency curves for ISBC with segmentation

The power stage width have been optimized to be $W_P = 0.110m$, $W_N = 0.055m$.

The three different working conditions of the ISBC listed in Table 3-2 were utilized again in this subsection. The data calculated from the developed switching loss analysis

method and the data calculated from an incorrect W/N assumption are compared with the transistor level Cadence simulation results (Spectre simulator, BSIM3V3.1 level 49 Spice model, 100°C, TT corner).

3.4.4.1 Incorrect W/N assumption

The present switching loss methods were not able to predict the load efficiency curves when the segmentation technique is adopted except that we followed an incorrect assumption. The incorrect assumption means that inactive power FET subcells are ignored in the loss analysis so that we do not need to care about the impact of the parasitic capacitors in the inactive power FET subcells. In the dissertation, we name the incorrect assumption as W/N assumption. Though the W/N assumption is incorrect, it was the only tool in the previous works [3-11, 3-12] to determine the optimal width in ISBC with segmentation technique.

3.4.4.2 Load efficiency curves

For the #1 working condition, the measured load efficiency curves for seven segmentation cases (the number of active power FET subcells is 8, 10, 12, 14, 18, 24, 32) are shown in Figure 3-10. The predicted load efficiency curves on the basis of the novel switching losses analysis method are shown in Figure 3-11. The predicted load efficiency curves on the basis of the W/N assumption are shown in Figure 3-12.

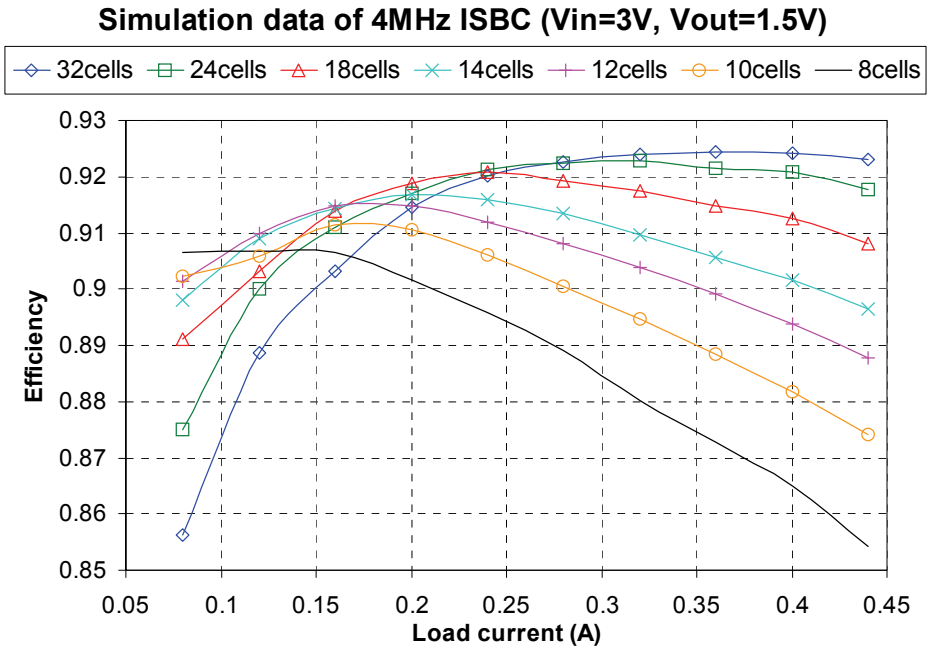

Figure 3-10. Simulation measured load efficiency curves for seven kinds of segmentation when the ISBC operates in the #1 working condition.

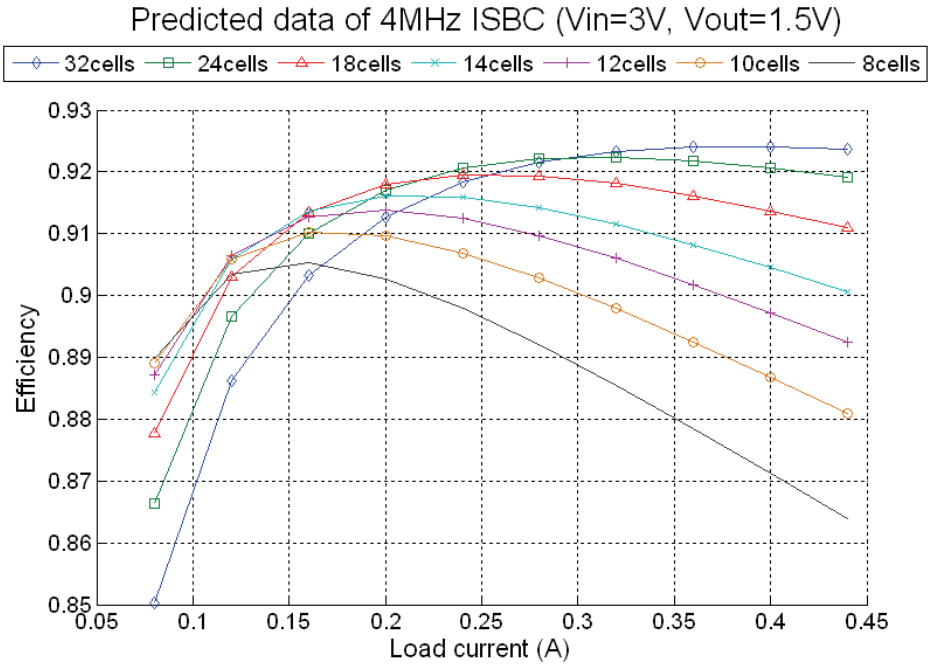

Figure 3-11. Predicted load efficiency curves for seven kinds of segmentation when the ISBC operates in the #1 working condition.

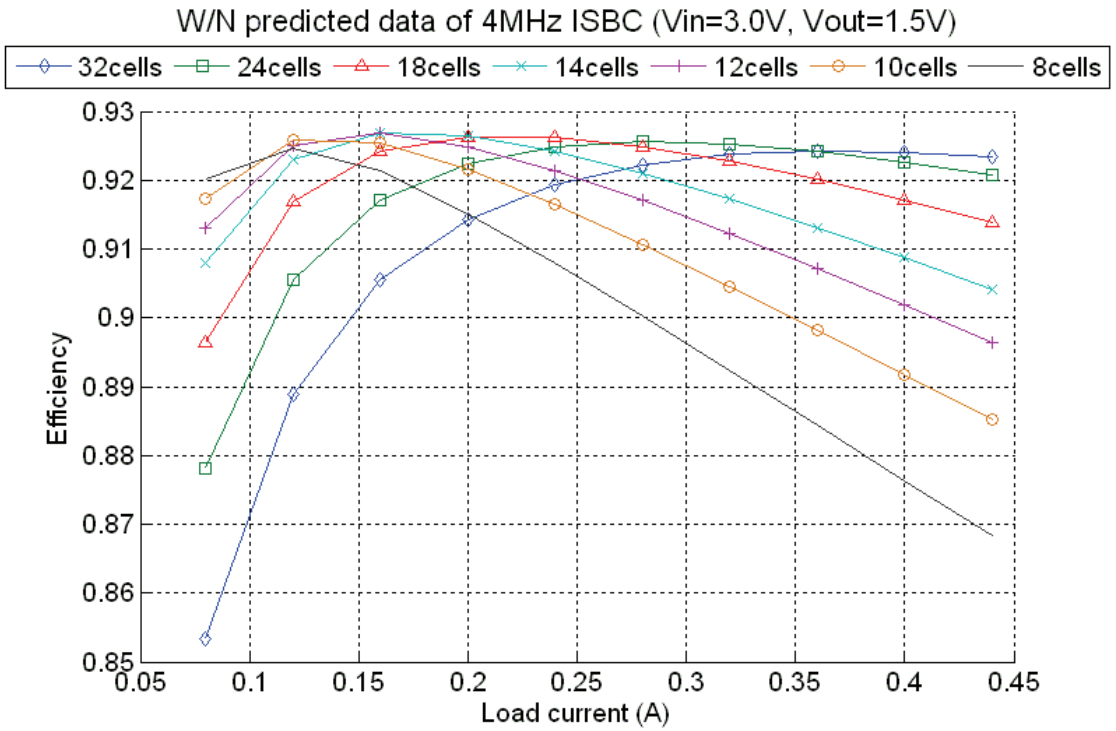

Figure 3-12. Incorrect W/N predicted load efficiency curves for seven kinds of segmentation when the ISBC operates in the #1 working condition.

From Figure 3-10 we observe that the peak values in the seven groups of load efficiency curves will continuously drop when the load current decreases even if the segmentation technique is adopted. The observation had also been separately reported by Dr. Trescases [3-9] and Mr. Lorentz [3-10] in their chip experimental or simulation measurements. The physical reason behind the observation is that the Cds and Cgd of the inactive power FET subcells are not eliminated despite that theses subcells had been disabled.

Comparing Figure 3-11 and Figure 3-12 with Figure 3-10, we find that the proposed loss analysis method successfully predicts the developing trend of the load efficiency curves when the segmentation technique is implemented, while the incorrect W/N assumption gives a wrong prediction in which the peak values of the efficiency curves is said to be higher when the load current decreases.

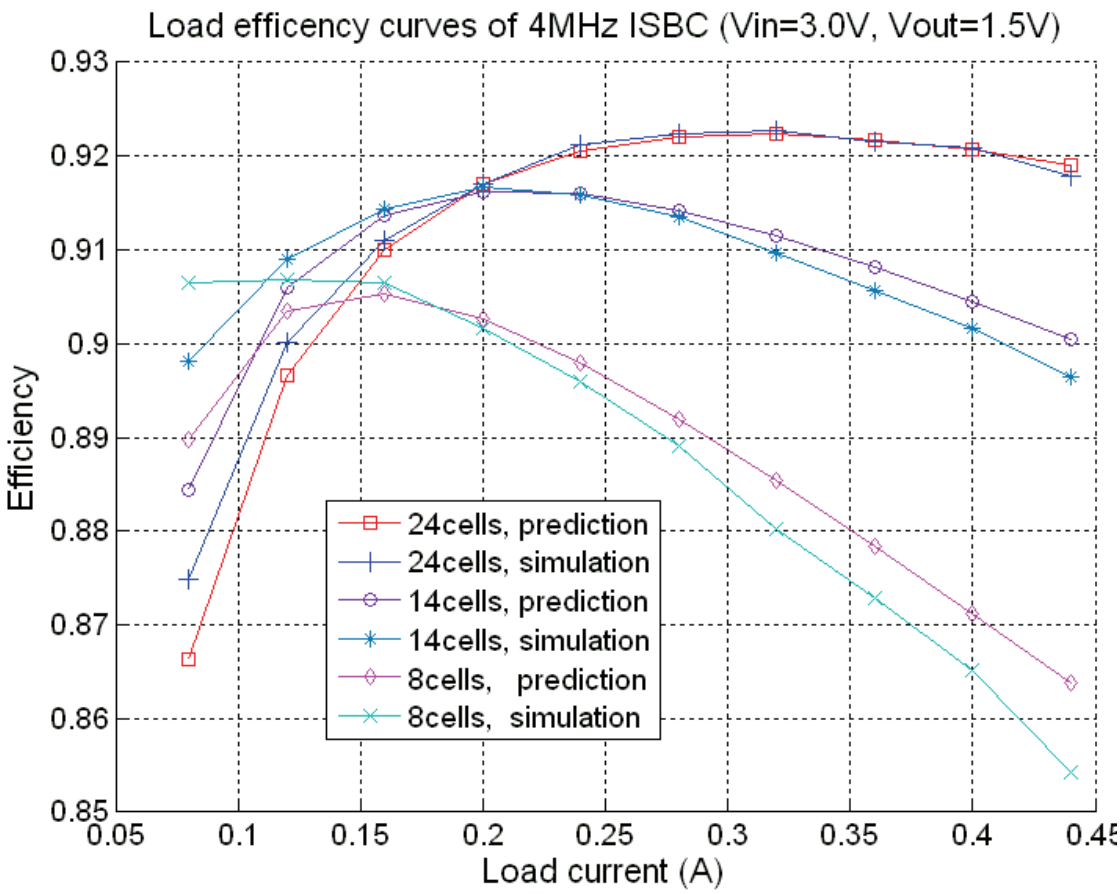

Figure 3-13. Simulation and prediction based load efficiency curves for three kinds of segmentation when the ISBC operates in the #1 working condition.

For the convenience of comparing the difference between Figure 3-10 and Figure 3-11, we select the efficiency curves in respect to 24, 14, and 8 active subcells out of total 32 subcells shown in Figure 3-10 and Figure 3-11 and repeat them in Figure 3-13.

In Figure 3-13, we observe that the prediction error due to the assumption of a constant diode forward voltage 0.65V will be more significant when the number of active subcells is smaller and the maximum absolute prediction error is 1.7% which appears when the number of active subcells is eight and the load current equals 0.08A.

We repeat the aforementioned process for the #2 working condition. The measured load efficiency curves for seven segmentation cases (the number of active power FET

subcells is 8, 10, 12, 14, 18, 24, 32) in the #2 working condition are shown in Figure 3-14. The predicted load efficiency curves for the same cases are shown in Figure 3-15. The predicted load efficiency curves on the basis of the W/N assumption are shown in Figure 3-16. The sampled load efficiency curves in Figure 3-14 and Figure 3-15 are shown in Figure 3-17.

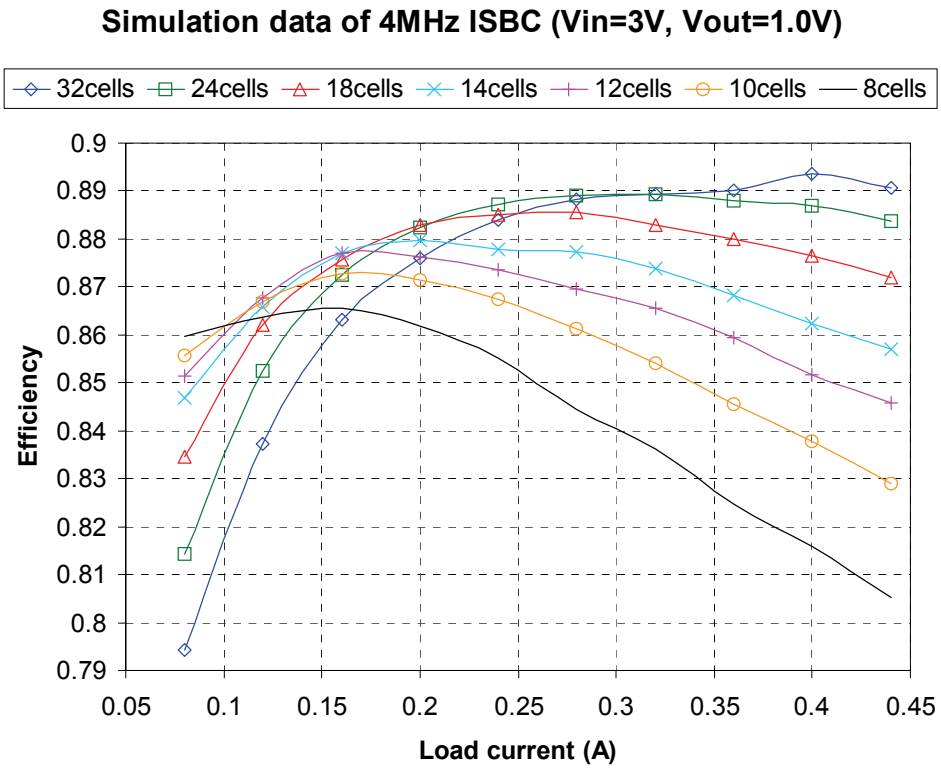

Figure 3-14. Simulation measured load efficiency curves for seven kinds of segmentation when the ISBC operates in the #2 working condition.

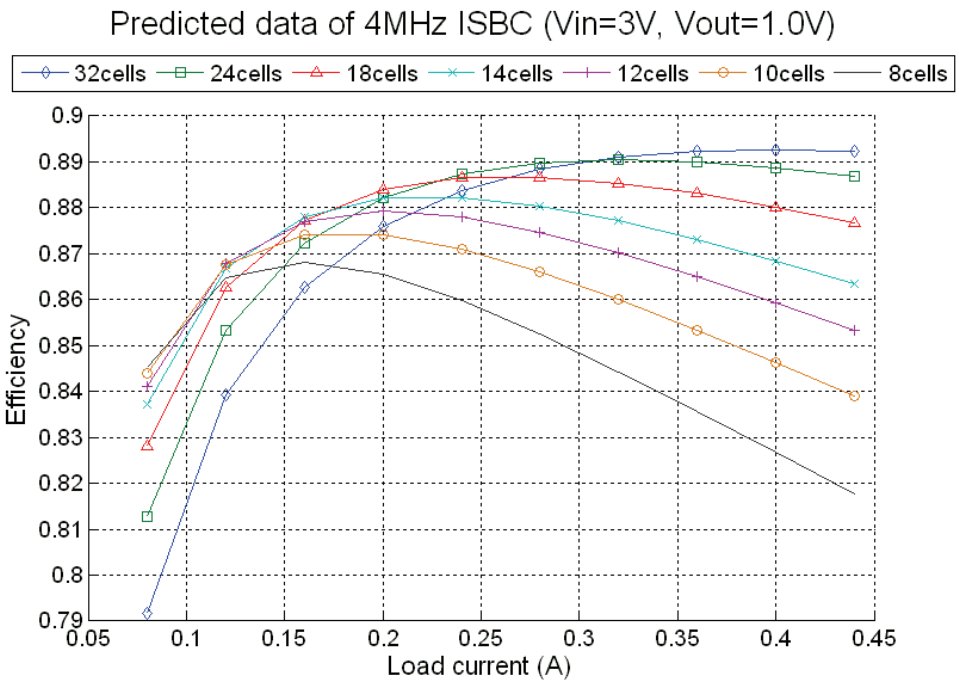

Figure 3-15. Predicted load efficiency curves for seven kinds of segmentation when the ISBC operates in the #2 working condition.

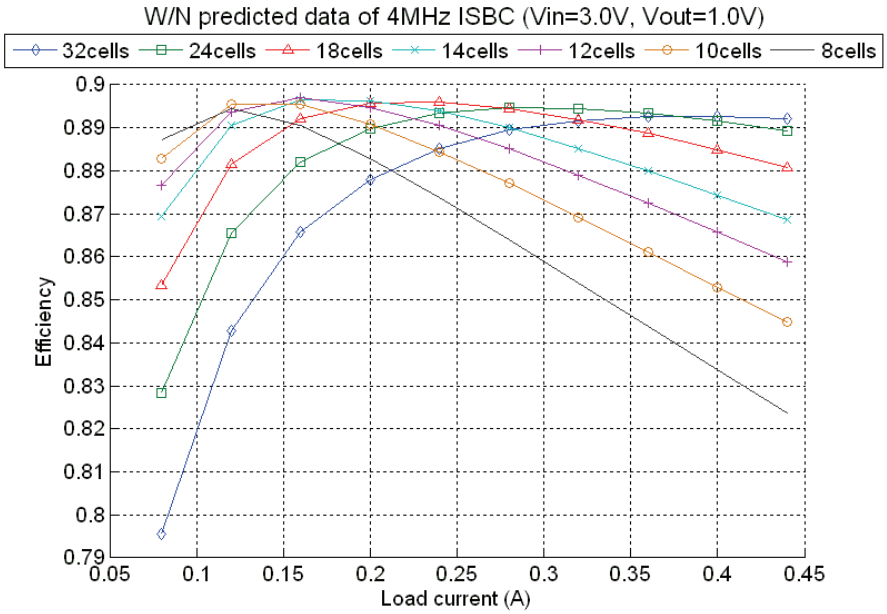

Figure 3-16. Incorrect W/N predicted load efficiency curves for seven kinds of segmentation when the ISBC operates in the #2 working condition.

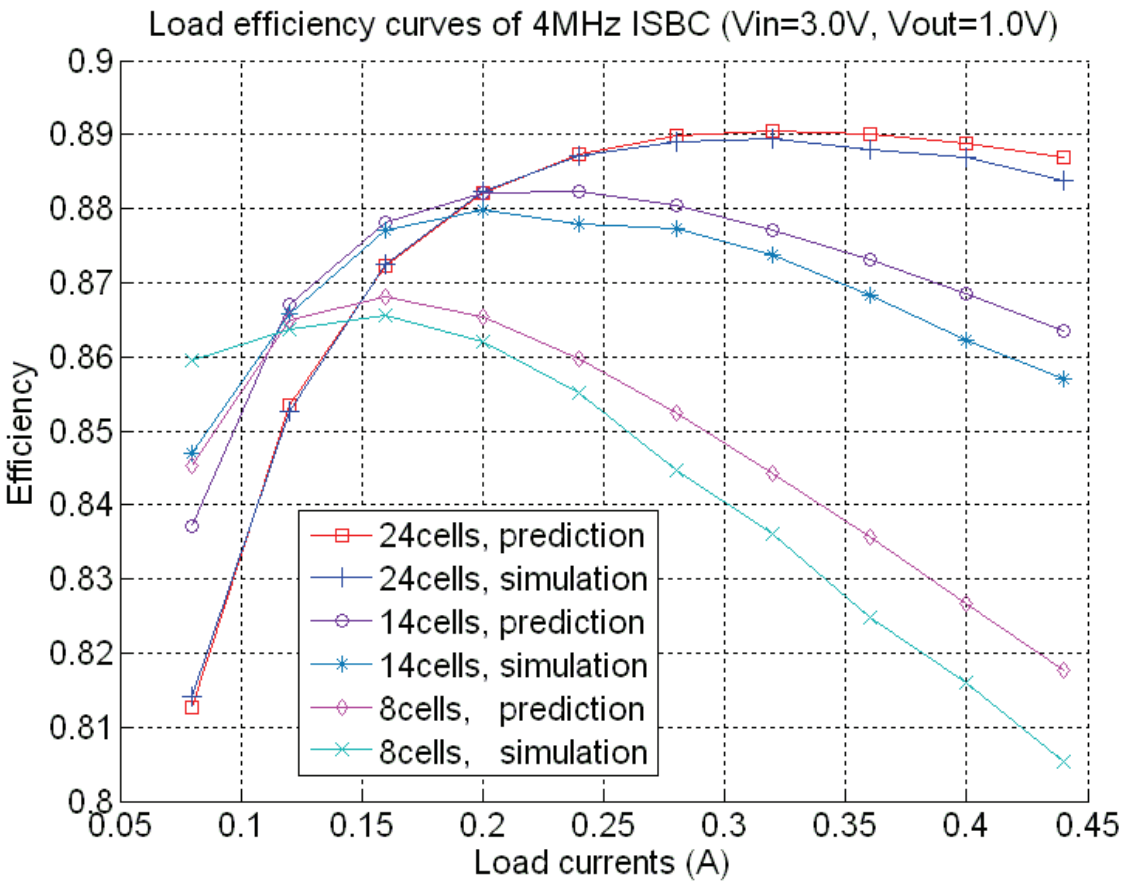

Figure 3-17. Simulation and prediction based load efficiency curves for three kinds of segmentation when the ISBC operates in the #2 working condition.

We also repeat the aforementioned process for the #3 working condition. The measured load efficiency curves for seven segmentation cases (the number of active power FET subcells is 8, 10, 12, 14, 18, 24, 32) in the #3 working condition are shown in Figure 3-18. The predicted load efficiency curves for the same cases are shown in Figure 3-19. The predicted load efficiency curves on the basis of the W/N assumption are shown in Figure 3-20. The sampled load efficiency curves in Figure 3-18 and Figure 3-19 are shown in Figure 3-21.

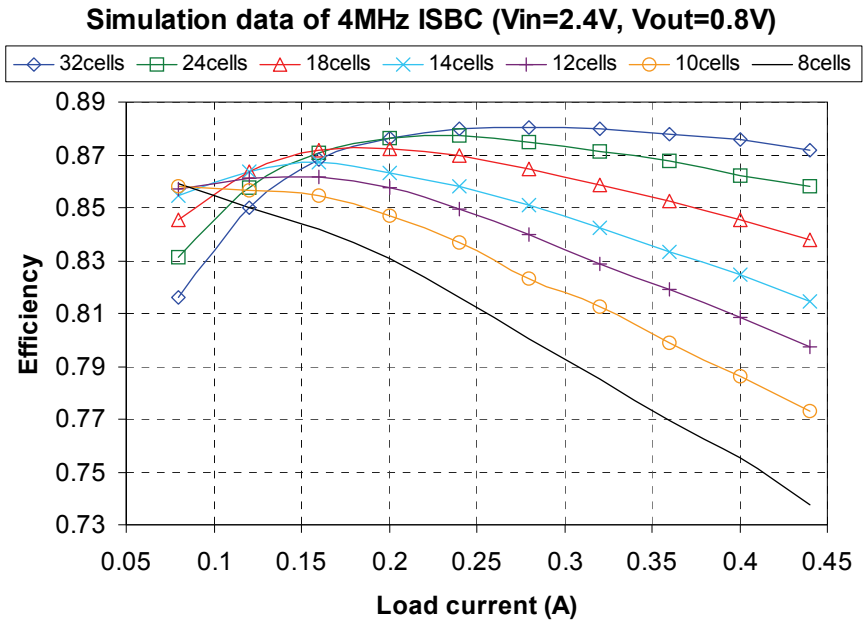

Figure 3-18. Simulation measured load efficiency curves for seven kinds of segmentation when the ISBC operates in the #3 working condition.

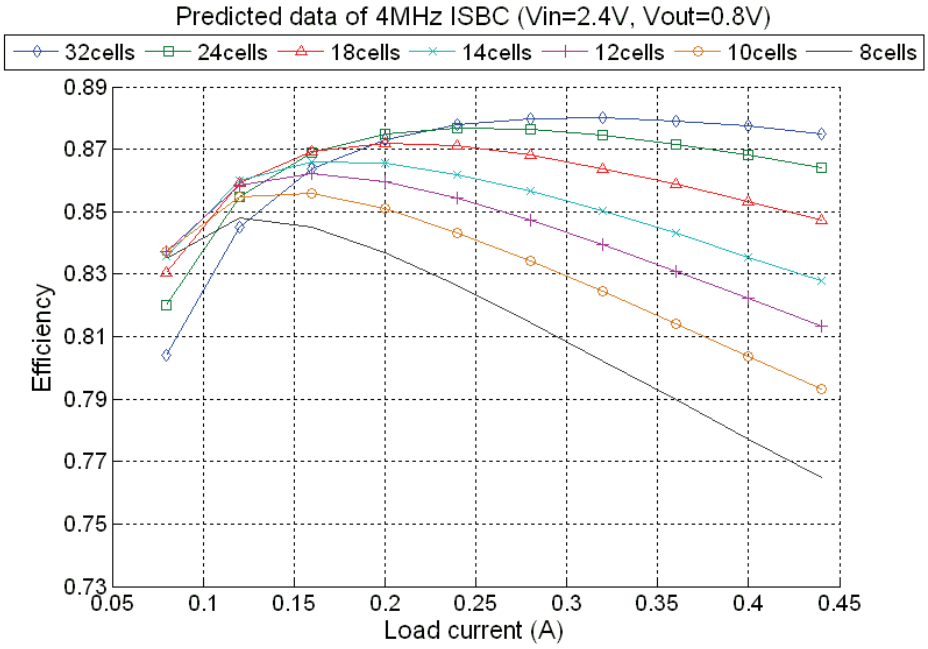

Figure 3-19. Predicted load efficiency curves for seven kinds of segmentation when the ISBC operates in the #3 working condition.

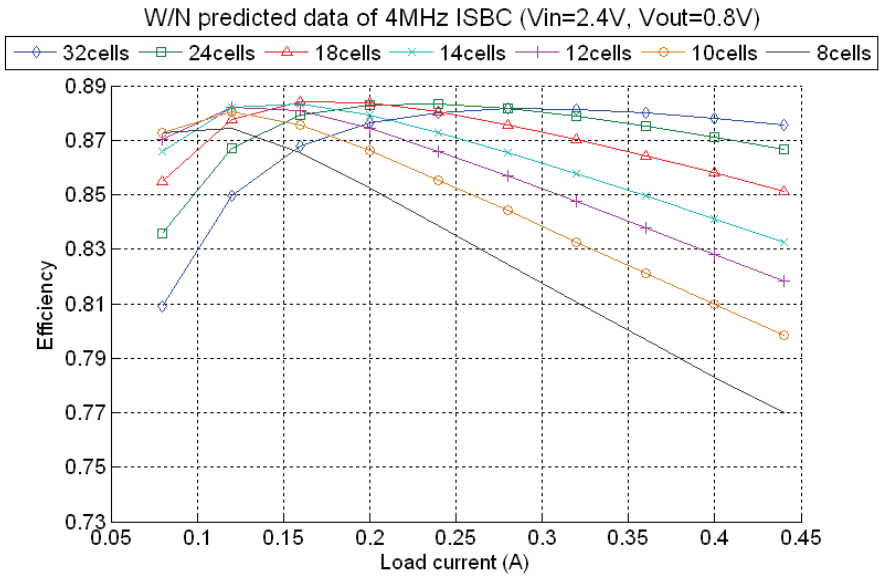

Figure 3-20. Incorrect W/N predicted load efficiency curves for seven kinds of segmentation when the ISBC operates in the #3 working condition.

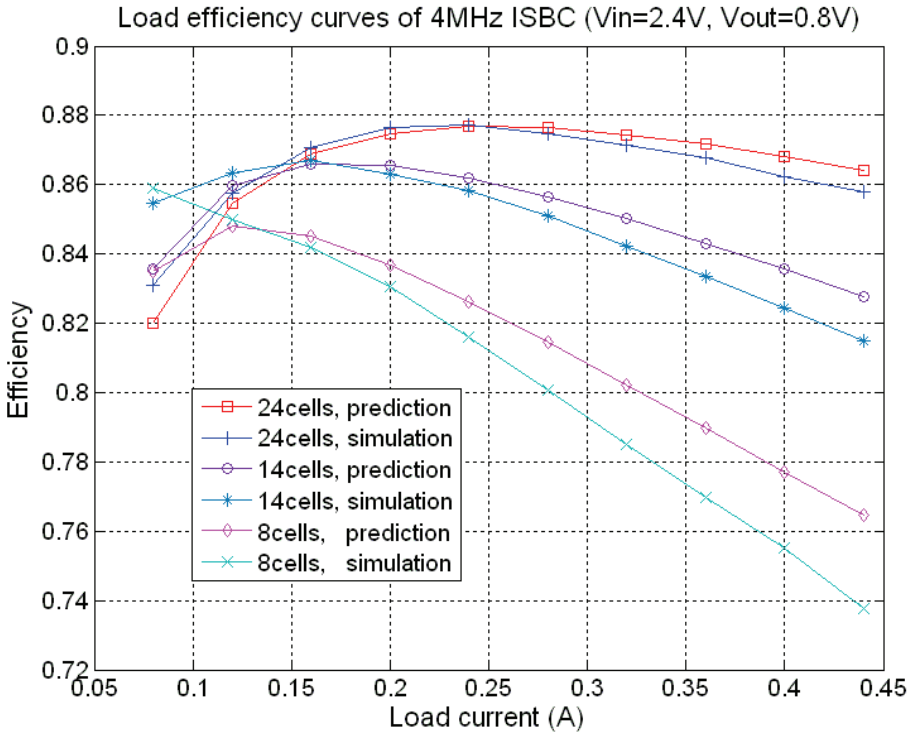

Figure 3-21. Simulation and prediction based load efficiency curves for three kinds of segmentation when the ISBC operates in the #3 working condition.

Figure 3-17 and Figure 3-21 verify the observation from Figure 3-13; the predicted error due to the assumption of a constant diode forward voltage 0.65V will be more significant when the number of active subcells is smaller. The maximum absolute prediction error is 1.3% in the #2 working condition and 2.4% in the #3 working condition, both of which appear when the number of active subcells is eight and the load current equals 0.08A.

3.4.5 Chip test

An ISBC chip is implemented in silicon for verifying the loss analysis method introduced in chapter 2. The total power stage width implemented in silicon is $W_P = 0.110592m$ and $W_N = 0.055296m$, which is constituted by seven groups of power FET subcells respectively having 8, 2, 2, 2, 4, 6, 8 standard subcells. Thus, with the aid of the logic circuit in Figure 3-15 realizing the truth table in Table 3-3, we can test the load efficiency of the ISBC due to different segmentation as that carried out in subsection 3.4.4 via simulation.

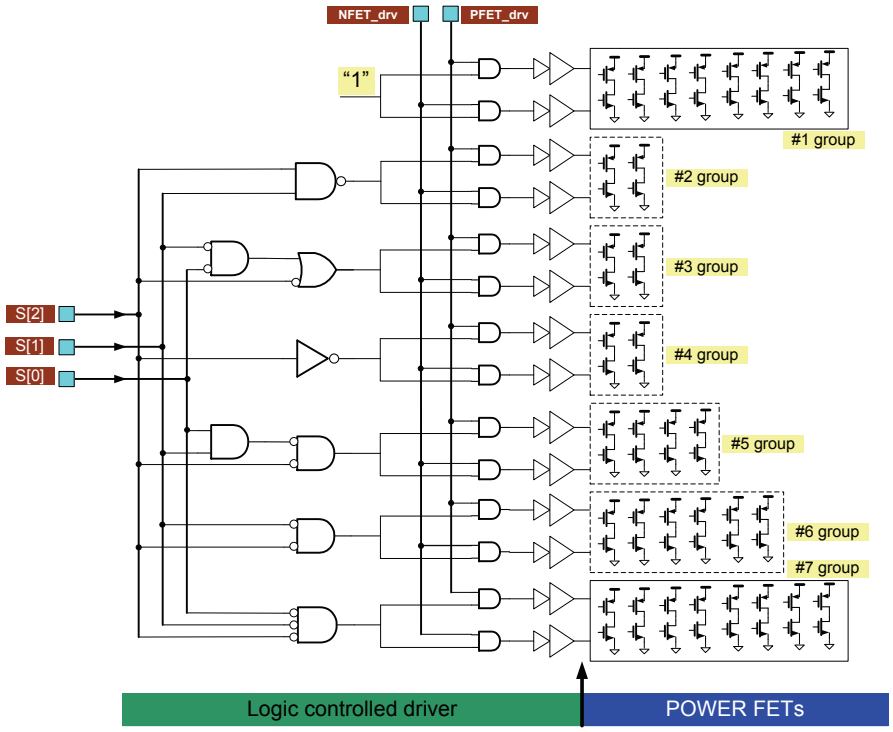

Figure 3-22. ISBC using logic controlled driver to realize segmentation

Table 3-3. The truth table of the driver logic

	#1 group (8 cells)	#2 group (2 cells)	#3 group (2 cells)	#4 group (2 cells)	#5 group (4 cells)	#6 group (6 cells)	#7 group (8 cells)	Total power FET subcells
000	1	1	1	1	1	1	1	***32***
001	1	1	1	1	1	1	0	***24***
010	1	1	1	1	1	0	0	***18***
011	1	1	1	1	0	0	0	***14***
100	1	1	1	0	0	0	0	***12***
101	1	1	0	0	0	0	0	***10***
110	1	0	0	0	0	0	0	***8***
111	1	0	0	0	0	0	0	***8***

The silicon layout of the power FET and the logic controlled driver in Figure 3-15 is shown in Figure 3-16.

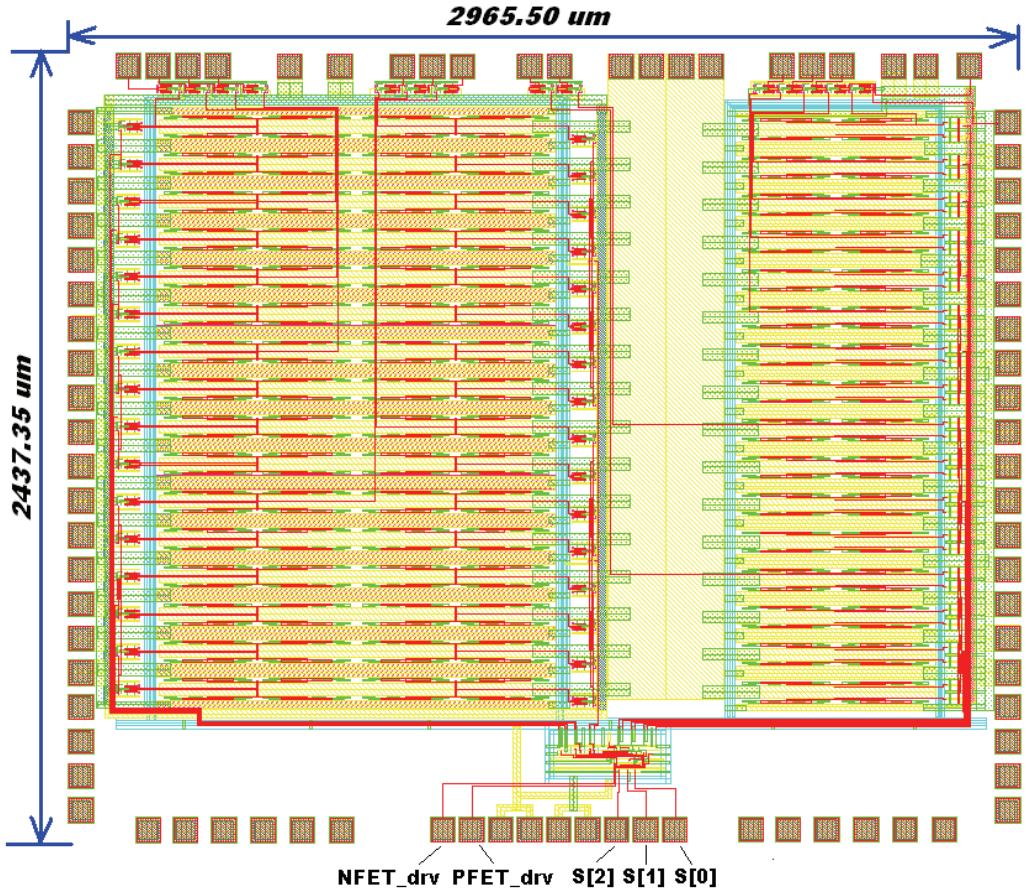

Figure 3-23. Silicon layout of the ISBC chip for loss analysis verification

3.5 Conclusions and future work

In this chapter, a 4MHz ISBC for a portable application was designed. PID control was selected for CCM and constant on-time control was selected for DCM. The transfer load current between CCM and DCM is 0.08A.

With the aid of the switching losses analysis developed in chapter 2, a complete set of power loss calculation equations were developed in this chapter. On the basis of these equations, the power FET of the ISBC was optimized at the maximum load current of 0.4A and the load efficiency curves of the ISBC were analyzed. The calculated values agreed very well with the simulation data. Also, it was found that the prediction error increased when the input voltage and output voltage decreased.

With the aid of the switching losses analysis developed in chapter 2, a complete set of power loss calculation equations for the ISBC with the segmentation technique were developed in this chapter. Seven kinds of segmentation cases and three different working conditions were utilized to compare the predicted load efficiency curves and the simulation load efficiency curves. The predicted values agreed very well with the simulation data. Also, it was found that the assumption of a constant diode forward voltage in chapter 2 induced prediction error and the prediction error increased when the load current is smaller, the input and output voltages are smaller or the number of active subcells decreased.

At the final part of the chapter, the designed ISBC chip is implemented on silicon. The ISBC chip had been submitted for fabrication in the MOSIS run V07G with the Fab-ID V07GBJ. The chip is expected at MOSIS on Jan. 31. 2011 and is planned to be tested in the spring 2011. The test results will be compared with the analytical and simulation results.

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Chapter 4

Silicon implementation of automatic segmentation

The load efficiency curves of the ISBC in chapter 3 corresponding to seven different numbers of the active power FET subcells highlight the necessity of introducing the segmentation technique into ISBCs that undergo a wide range of load current variations.

Automatic segmentation implies that the number of active power FET subcells in the ISBC will be dynamically regulated in response to load current changes so that the ISBC power efficiency can be maintained at a level as high as possible.

This chapter will focus on how to automatically implement the segmentation in the aforementioned ISBC in a transistor level circuit design. In section 4.1, state-of-art solutions [4-1, 4-2, 4-3] for automatic segmentation are introduced. These solutions obtain the load current information via a current sensor or predictor, then uses an A/D converter to realize digitization and outputs the "on" or "off" signal to the drivers of different power FET subcells. As the segmentation action depends on the load current information, we denote the solution as current information based segmentation (CIS). Section 4.1 will also discuss the challenges for CIS from the viewpoint of both implementation and segmentation algorithm. Section 4.1 will utilize the developed switching loss analysis in chapter 2 to calculate the optimal segmentation in the viewpoint of power efficiency. Furthermore, the impact of power FET parameter mismatch due to manufacturing and temperature variations will be investigated. Section 4.2 introduces a control power FET Vsw pinning automatic segmentation (VswPS) which not only does not need either a current sensor or an A/D converter but also can provide automatic temperature compensation. In comparison with CIS, VswPS will improve the accuracy, speed, chip area and power consumption of the segmentation circuits at the same time. The advantage will become more significant when the switching frequency of

the ISBC is beyond 4MHz or the number of segmentation bit is increased. Section 4.3 introduces the circuit schematics of the VswPS, a practical measure to cope with load transient events, and circuits to realize smooth mode transfer between PFM and PWM. Section 4.4 shows the performance simulation result of an ISBC with VswPS and PFM technique. Section 4.5 shows the simulation results to verify the Rdson compensating ability of the VswPS technique. Section 4.6 is the conclusion and discusses future work.

4.1 State-of-art techniques

In the published papers about the segmentation, [4-1], [4-2] and [4-3] presented state-of-art solutions for automatic segmentation, while [4-4] and [4-5] did not. This subsection will introduce the automatic segmentation described in [4-1, 4-2, 4-3] and discuss why these implementations might not achieve the expected optimal power efficiency for some practical cases. At the same time, the possible challenges and complexity in the IC circuit design are addressed.

4.1.1 Load current information based segmentation

To realize automatic segmentation, state-of-art automatic segmentation techniques utilize either current sensors [4-2, 4-3] or current predictors [4-1] to obtain load current information, then digitize the signal via analog/digital (A/D) conversion and follow the segmentation algorithm shown in Figure 4-1 to implement power FET subcells management. As the number of active power FET subcells is determined by the value of load current, we denote the state-of-art automatic segmentation techniques as current information based segmentation (CIS). The difference between the state-of-art automatic

segmentation techniques is the details implementation of current sensor, A/D converter and other safe operation blocks.

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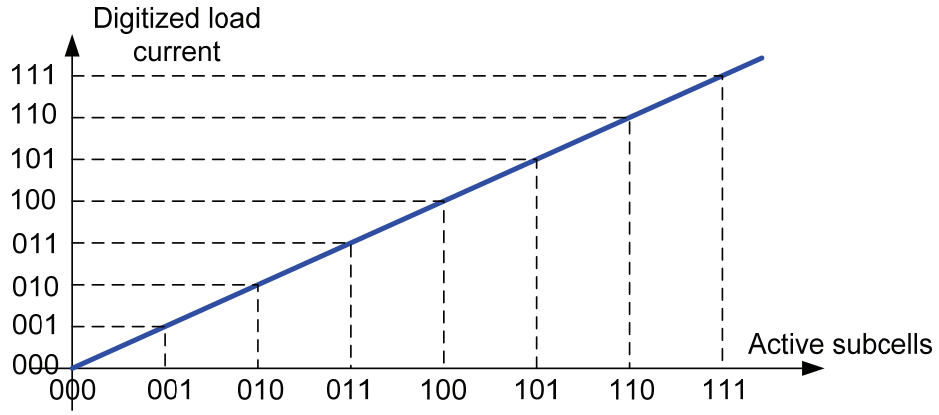

Figure 4-1. Segmentation algorithm in CIS

Figure 4-2 shows a load current predictor based CIS [4-1]. $S[m]$ is the information code representing the activity of the ISBC loaded electronic devices. $S[m]$ is utilized to predict how many load current that the electronic devices is sinking from the ISBC when the electronic devices implement the monitored activity. A 3-bit flash A/D converter digitizes the predicted load current to be a 3-bit digital thermometer code and the code is feed into a segmentation logical circuit block to generate a 3-bit segmentation management signal for the ISBC gate driver. In the implementation, the power FET subcells were segmented into seven identical groups, the number of active subcells was managed to be linearly proportional to the predicted load current, and the ISBC gate drives were connected in a binary weighted fashion to achieve 3-b control of power FET.

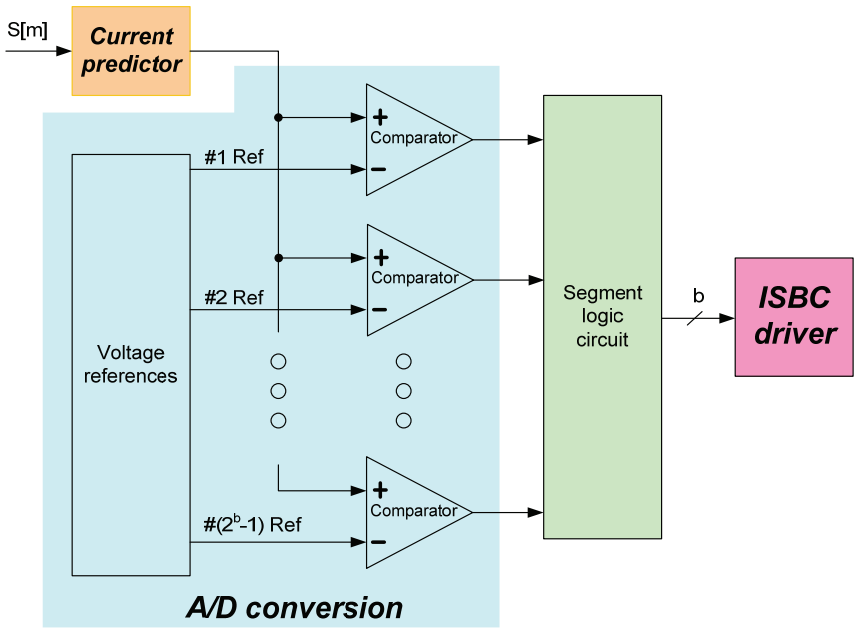

Figure 4-2. CIS implementation based on current predictor [4-1]

The load current predictor [4-1] requires the communication between ISBC and its loaded electronic devices. In most of practical ISBC applications, there is no such kind of communication link. Also, the load current predictor needs signal processing technique which seriously impedes the real-time response of the current sensing.

Figure 4-3 shows another implementation of CIS [4-2] which utilizes an on-chip sense-FET current sensor to obtain load current information. The flash A/D converter in [4-1] is substituted by a delay-line A/D converter for saving power and chip area.

There is also a discrete implementation of CIS [4-3] where the power FET subcells are replaced by discrete power FET components on a printed circuit board. In the design, the safe operation of the CIF in the step load transient is discussed.

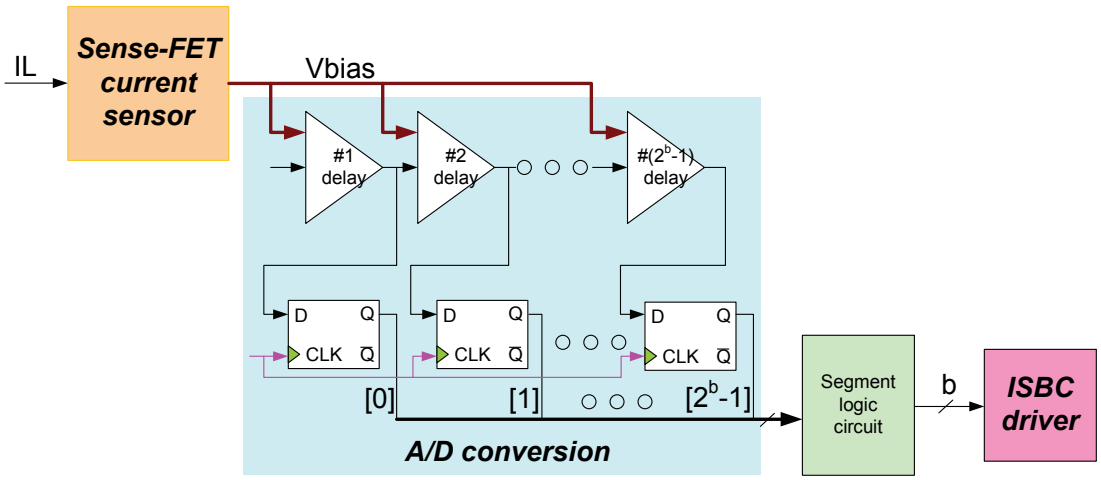

Figure 4-3. CIS implementation based on sense-FET current sensor [4-2]

4.1.2 Challenges

4.1.2.1 Optimal segmentation

Optimal segmentation refers to the situation that the ISBC has a power FET width which is dynamically adjusted to exactly arrive at the maximum power efficiency for any load condition.

Due to the lack of loss analysis method for segmentation, the adjustment of the active power FET width in previous implementations [4-1, 4-2, 4-3] followed the algorithm shown in Figure 4-1. The algorithm was developed by [4-4] [4-27] under the incorrect W/N assumption in subsection 3.4.4.1. Another way to realize an optimal segmentation is with the aid of experiment measurement. The designer first designs an open-loop ISBC chip with only the power stage and manufactures the first-round chip. Then the technician sequentially enables different numbers of active power FET subcells on the first-round chip and measures the corresponding load efficiency curves. From the measurement data, the exact number of active subcells for the optimal segmentation in a specified load current is deduced and the optimal segmentation algorithm is achieved. The design-

tapeout-test-design-tapeout process is remarkably inconvenient and significantly increases the design cost and period of the ISBC.

The loss analysis method in the chapter 2 and the equations in the chapter 3 solve the aforementioned issues. With the aid of these equations, we can analytically conclude the optimal number.

As the dead-time conduction loss, the quiescent current loss and the copper loss are less dependent of segmentation implementation, the optimal value of m is the solution in equation (4-1) which looks for the minimum loss with m as the variable.

$$m^{(opt)} = \min\left(P_{loss}^{(seg)}\right) \tag{4-1}$$
$$= \min(R_{dson}\left(I_o^2 + \frac{\Delta I^2}{12}\right) + K_{Cap}W_P m) = \min(\frac{K_{Rdson}}{mW_P}\left(I_o^2 + \frac{\Delta I^2}{12}\right) + K_{Cap}W_P m)$$

in which K_{Cap} and K_{Rdson} are respectively the coefficients relative to the parasitic capacitance and the hybrid Rdson of PMOS and NMOS power FET.

The expression of the R_{dson} is given in (4-2).

$$R_{dson} = R^{P\_seg}D + R^{N\_seg}\left(1 - D\right) \tag{4-2}$$

If we ignore the contribution of the inductor current ripple, the value of $m^{(opt)}$ can be concluded from (4-1) and is given in (4-3). The approximation is acceptable for the ISBC, as all of the analysis in Chapter 2 and 3 is based on an assumption that the ISBC works in the CCM or the load current is larger than 0.08A. Thus, for the ISBC in high frequency operation, $I_o^2 >> \frac{\Delta I^2}{12}$ will be satisfied for the segmentation analysis in CCM operation.

$$m^{(opt)} = \sqrt{\frac{K_{Rdson}}{K_{Cap}}}\frac{I_o}{W_P} \tag{4-3}$$

For the ISBC introduced in the chapter 3 with $V_{dd} = 3.0V$, $D = 0.5$ and 32 power FET subcells, the values of R_{dson}, K_{Rdson}, and K_{Cap} are derived in (4-4), (4-5) and (4-6) from (3-72).

$$R_{dson} = \frac{32 * 0.197 * D}{(1 + 4.54\, V_{dd})\, mW_P} + \frac{32 * 0.0122 * (1 - D)}{(1 + 0.625\, V_{dd})\, mW_N} \tag{4-4}$$

$$K_{Rdson} = (0.2156 + 0.0679 K_W) \tag{4-5}$$

$$K_{Cap} = \left(\frac{\alpha_P}{32} + 0.00218\right) + \frac{0.00208}{K_W} \tag{4-6}$$

in which $K_W = W_P / W_N$.

If we further ignore the impact of overlap loss (setting $\alpha_P = 0$), we can get the specified $m^{(opt)}$ in (4-7).

$$m^{(opt)} = \sqrt{\frac{(0.2156 K_W + 0.00679 K_W^2)}{(0.00218 K_W + 0.00208)}}\, \frac{I_o}{W_P} \tag{4-7}$$

The practical value of m is an integer, so it will be the rounded value of $m^{(opt)}$. At the same time, it should be smaller than the number of available subcells. For example, the maximum number of available subcells in the ISBC in the chapter 3 is 32, so the real optimal value of m is $m^{(opt\_real)}$ in (4-8).

$$m^{(opt\_real)} = \begin{cases} round(m^{(opt)}) & if\ round(m^{(opt)}) \le 32 \\ 32 & if\ round(m^{(opt)}) > 32 \end{cases} \tag{4-8}$$

The value of $m^{(opt)}$ in (4-7) and $m^{(opt\_real)}$ in (4-8) are depicted in Figure 4-5, from which we notice that both $m^{(opt)}$ and $m^{(opt\_real)}$ are almost linearly proportional to the load current. Thus, (4-7) and (4-8) provide a theoretical basis for the CIS implementation in an ideal condition.

If we compare (4-7) (4-8) with the segmentation algorithm in Figure 4-1 derived by the equations in [4-4] [4-27] under the incorrect W/N assumption, we find that the incorrect W/N assumption also concluded the linear relationship between $m^{(opt)}$ and load current. The reason is that C_{db} is independent of $m^{(opt)}$ optimization and the value of $C_{gd}^{(L)}$ is limited. An important difference between (4-7), (4-8) and the results from the incorrect W/N assumption is that the latter cannot find the nonlinear saturation phenomenon shown in Figure 4-4, which implies the existence of inactive subcells parasitic capacitors and their contribution to the losses.

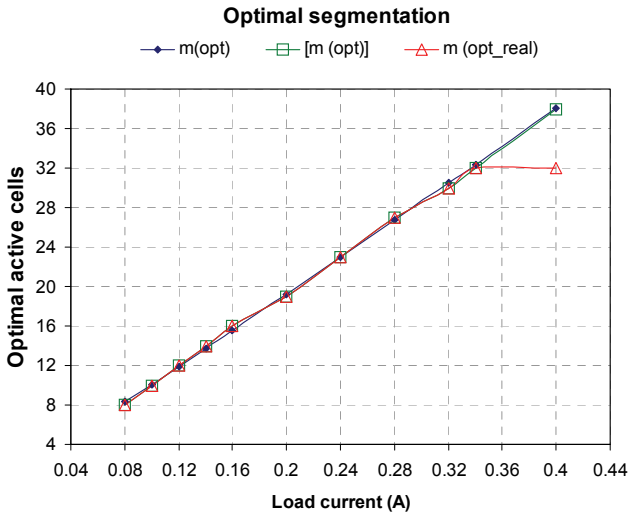

Figure 4-4. Calculated optimal number of active power FET cells

From chapter 3 and (4-1), it can be concluded that the maximum efficiency implies the exact balance of switching loss and conduction loss at a specified load current. Thus, if in a practical case where either one or both of the power FET Rdson and parasitic capacitance deviate from their expected values claimed in the power FET size

optimization, the practical ISBC will have a different balance of the switching and conduction loss.

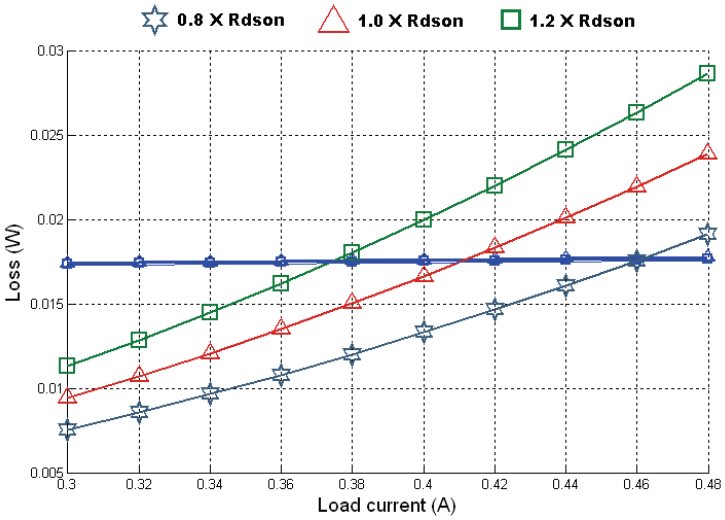

Figure 4-5. The shift of loss balance point due to Rdson variation

Figure 4-5 illustrates the switching loss and conduction loss in the ISBCs whose Rdson is either the normal value or deviates from the normal value by $\pm 20\%$. The blue curves with circle symbols are the switching loss curves which are almost the same in three different Rdson cases. The green rectangles curve depicts the conduction loss for 1.2 times larger Rdson, the red triangles for 1.0 times Rdson and the blue stars for 0.8 times Rdosn. It is shown that the relative balance points are respectively 0.373A, 0.411A and 0.462A.

Figure 4-6 illustrates the switching loss and conduction loss in the ISBCs that has parasitic capacitance that is either the normal value or deviates from the normal value by $\pm 20\%$. The green curves with circle symbols are the conduction loss curves which are almost the same in three different parasitic capacitance cases. The curve with pink rectangles depicts the switching loss for 1.2 times larger capacitance, the blue triangles for 1.0 times capacitance and the blue stars for 0.8 times smaller capacitance. It is shown that the relative balance points are respectively 0.367A, 0.411A and 0.451A.

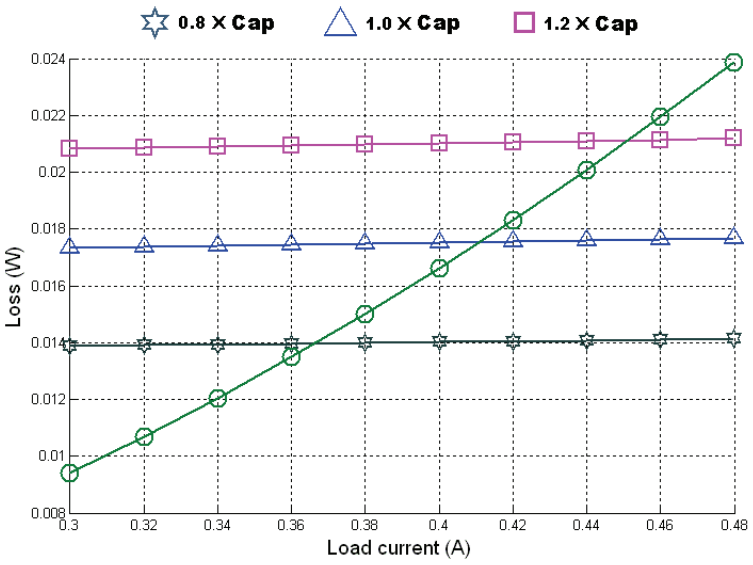

Figure 4-6. The shift of loss balance point due to parasitic capacitance variation

Figure 4-6 and Figure 4-7 show that when either one or both the Rdson and MOSFET parasitic capacitance deviate from their expected values due to some practical factors, if current information is still be used to implement the automatic segmentation at some load condition, the obtained efficiency will not be the optimal one.

In the following subsections, several practical factors contributing to the variations of the power FET Rdson and parasitic capacitance are discussed.

4.1.2.2 Parameter variation due to manufacturing

Due to manufacturing errors, the MOSFET's Rdson and parasitic capacitance will be somewhat different from the specified values. Utilizing the BSIM model or physical equations [4-6, 4-7] to analytically investigate the variation of Rdson and parasitic capacitance is beyond the scope of the dissertation. This subsection focuses on the data statistics of the reported manufacture parameters to conclude the maximuml magnitude and characterization of the parameter deviation. The subsection uses ***AMI06 (ON-SEMI) SCN05*** standard CMOS technology as an example. The data publically reported by the

vendor ***(ON-SEMI)*** is collected together to summarize how many variations happened to the Rdson and parasitic capacitance.

Table 4-1 lists two groups of parameters' values reported by MOSIS [4-8] for one run (V03M) of the SCN05 technology. The first group is relative to the MOSFET parasitic capacitance and the second group is relative to Rdson.

Table 4-1. MOSIS wafer acceptance tests report for V03M run [4-8]

AMI06 (ON-SEMI) SCN05 technology V03M run (type: SKD)				
Capacitance parameters	Value		Capacitance parameters	Value
Area (N+/Poly)	2453 aF/um^2		Area(Sub/P+)	721 aF/um^2
Overlap(N+/Poly)	182 aF/um		Area(Sub/Poly)	84 aF/um^2
Area(P+/Poly)	2357 aF/um^2		Fringe(Sub/N+)	356 aF/um
Overlap(P+/Poly)	234 aF/um		Fringe(Sub/P+)	227 aF/um
Area(Sub/N+)	415 aF/um^2			
Transistor parameters	Value		Transistor parameters	Value
Vth (N)	0.65 V		Vth (P)	-0.87 V
K' (N)	58.4 uA/V^2		K' (P)	-19 uA/V^2

If we regard the parameter values in the Table 4-1 as average values denoted with K_{AVG}^{XX} and the values in other seven runs (named by MOSIS as V01B, V01W, V01V, T9CW, T9CU, T9CR, T99J) as sampled ones denoted with K_{sample}^{XX}, the equation in (4-9) is utilized to calculate each sample's deviation error E_{sample} from the average ones.

$$E_{sample} = \frac{K_{sample}^{XX} - K_{AVG}^{XX}}{K_{AVG}^{XX}} \tag{4-9}$$

The results of (4-9) for the parasitic capacitance related parameters are shown in Figure 4-7. The results of (4-9) for the Rdson related parameters are shown in Figure 4-8.

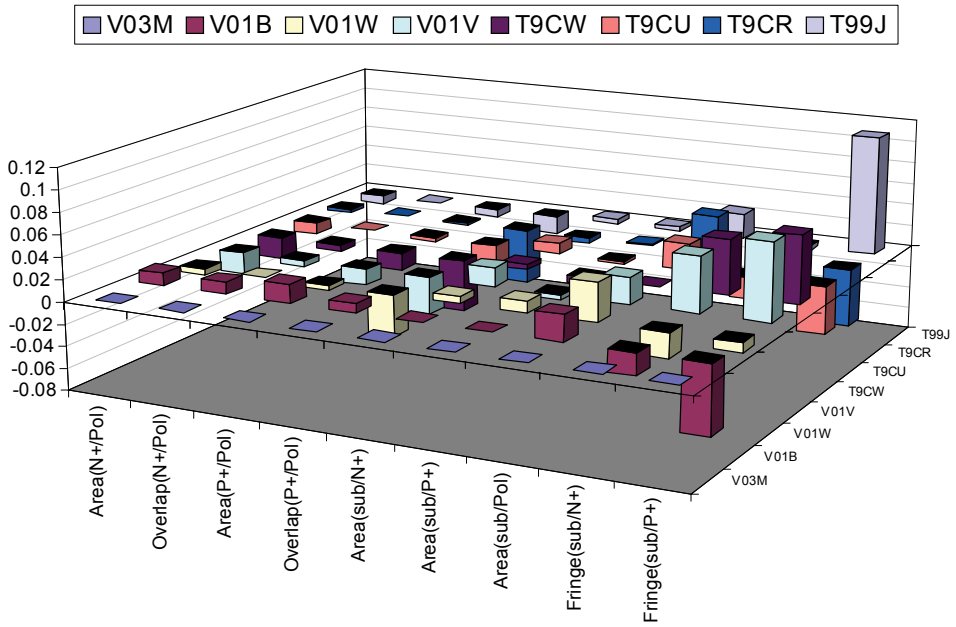

Figure 4-7. Deviation of parasitic capacitance relative parameters in AMI06 SCN05 technology's different manufacturing runs

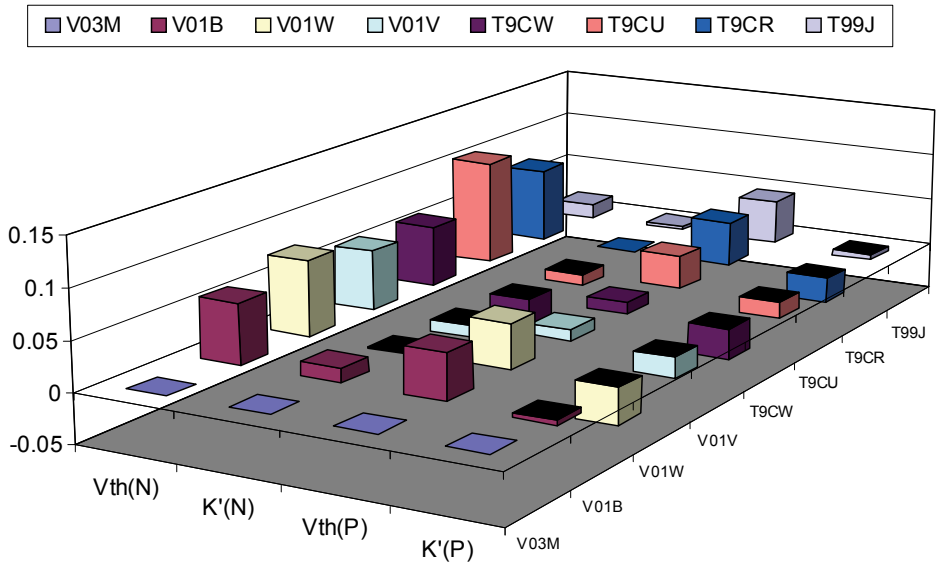

Figure 4-8. Deviation of Rdson relative parameters in AMI06 SCN05 technology's different manufacturing runs

From Figure 4-7 and Figure 4-8, we notice that MOSFET Rdson has larger manufacturing deviation in comparison with the MOSFET parasitic capacitance. Also, the maximum deviation of both groups of parameters is in the range of ±10% (a value tolerable for design engineers) and the deviation is random. Thus, we ignore the impact of the manufacturing deviation on the automatic segmentation.

Another way to review the possible deviation of Rdson and parasitic capacitance is to observe the parameters values specified in the BSIM3V3.1 level 49 Spice corner models provided by the MOSIS [4-9]. Table 4-2 lists the corner data of several parameters which will have major impact on the Rdson and parasitic capacitance. From Table 4-2, we notice that the parameters variations are in the range of ±10% (a value tolerable for design engineers) and the variation is of random character, so we ignore its impact on the automatic segmentation. Figure 4-9 further illustrates the values of Rdson in PMOS which are measured in simulation from which it is confirmed that Rdson variation due to the change of corner models is limited.

Table 4-2. Major parameters relative to
Rdson and capacitance in MOSIS BSIM3V3.1 level 49 Spice corner models [4-9]

corner	Tox (m)	VTHO (V)	UO (cm^2/V-s)		CGDO (F/m)	CGSO (F/m)	CJ (F/m^2)	CJSW (F/m)
TT(P)	1.39E-8	-0.9214	212.02		2.9E-10	2.9E-10	7.24E-4	2.69E-10
FF(P)	1.39E-8	-0.8880	211.68		2.75E-10	2.75E-10	7.24E-4	2.69E-10
FS(P)	1.39E-8	-1.0173	213.22		3.18E-10	3.18E-10	7.24E-4	2.69E-10
SF(P)	1.39E-8	-0.8558	211.06		2.64E-10	2.64E-10	7.24E-4	2.69E-10
SS(P)	1.39E-8	-0.9223	211.83		2.84E-10	2.84E-10	7.24E-4	2.69E-10
TT(N)	1.39E-8	0.6696	458.44		2.00E-10	2.00E-10	4.19E-4	3.24E-10
FF(N)	1.39E-8	0.6253	461.23		1.98E-10	1.98E-10	4.20E-4	3.24E-10
FS(N)	1.39E-8	0.6407	459.88		2.03E-10	2.03E-10	4.20E-4	3.24E-10
SF(N)	1.39E-8	0.7149	457.72		2.03E-10	2.03E-10	4.20E-4	3.24E-10
SS(N)	1.39E-8	0.7087	459.67		2.02E-10	2.02E-10	4.20E-4	3.24E-10

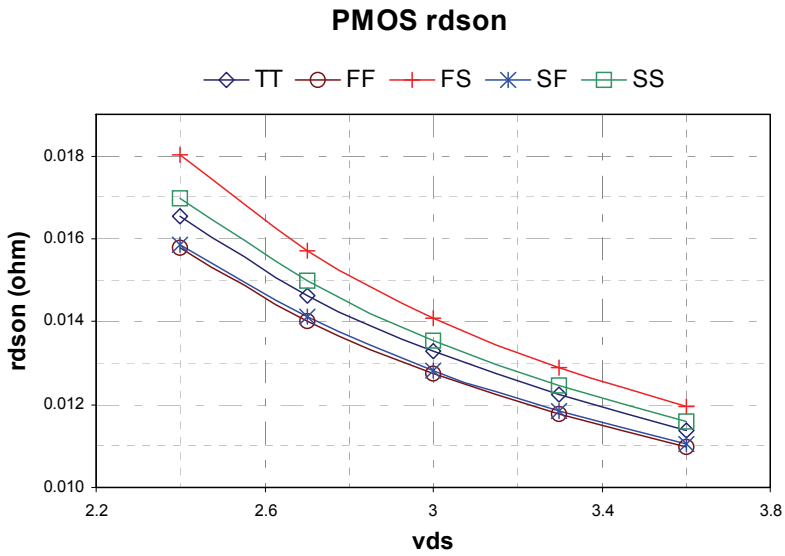

Figure 4-9 PMOS Rdson with MOSIS BSIM3V3.1 level 49 Spice corner models

4.1.2.3 Temperature variation and self-heating effect

The range of temperature variation in the ISBC chip is possible to be higher than 100°C [4-10, 4-11, 4-13] and the thermal image in [4-10] for a practical 500KHz switching frequency ISBC product illustrated that the temperature of the MOSFET is 93°C for its specified load operation. Thus, we should consider the change of Rdson and parasitic capacitance when a 100°C temperature change occurs on the ISBC.

Figure 4-10 shows the measured Rdson in the simulation with MOSIS BSIM3V3.1 level 49 Spice models [4-9] for different Ids, Vds, corner models and temperatures which can appear in the specified operation of the ISBC in the Chapter 3.

It is observed that Rdson has more than 50% of change in the simulation when the temperature shifts from 0°C to 100°C; the Rdson deviation is in the range of 4% when Ids changes from 0.1A to 0.4A; The maximum Rdson deviation is in the range of 10% when the process corner changes. Thus, temperature presents the dominant influence on the Rdson in comparison with other factors.

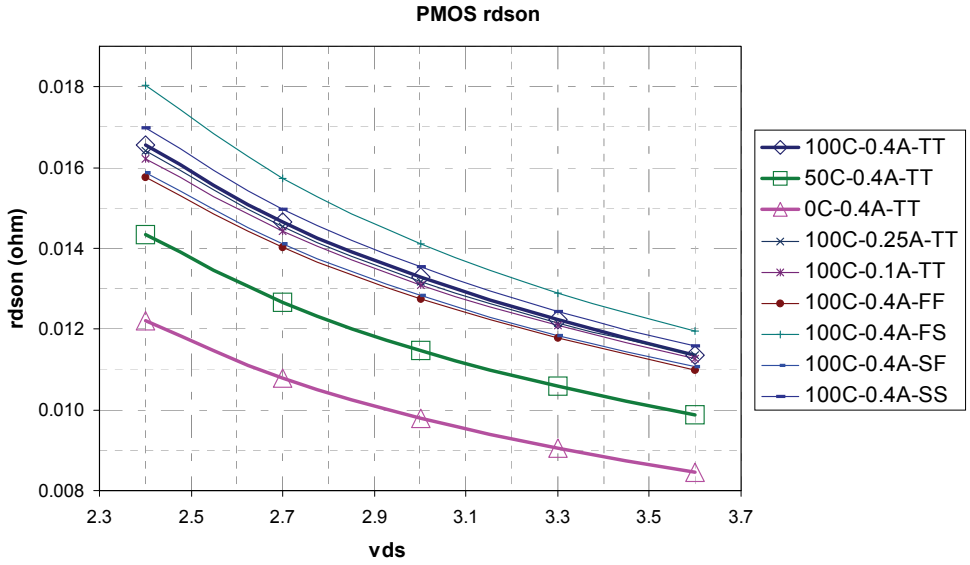

Figure 4-10 PMOS Rdson variation due to Ids, Vds, corners and temperatures

Figure 4-10 is still in fact an underestimation of the temperature effect, as the self-heating effect [4-11, 4-12, 4-13] is not included in the BSIM3V3.1 level 49 Spice model [4-7]. The experimentally measured Rdson for some power FETs was reported in [4-12] and repeated in Table 4-3. Same scale temperature varying effects on Rdson were introduced in [4-13].

Table 4-3. Experimental measured Rdson via temperature variation [4-12]

Temperature (K)	77	173	243	295
Rdson (ohm) [4-12]	0.001	0.005	0.008	0.016

Temperature effects are a big issue in the CIS which applies automatic segmentation on the information of the load current, and the issue had not yet been in attention. In order to solve the issue, the CIS needs extra specific circuits in the current sensor to compensate the temperature effect of MOSFET Rdson. The temperature effect and its compensation were not mentioned in [4-1], [4-2] and [4-3].

4.1.2.4 Circuit challenges

Lossless implementation, integration, and pin-less design are the important performance factors for the current sensors in the ISBCs [4-14, 4-15, 4-16, 4-17, 4-18], so the state-of-art current sensors popularly use the sense-FET method as illustrated in Figure 4-11.

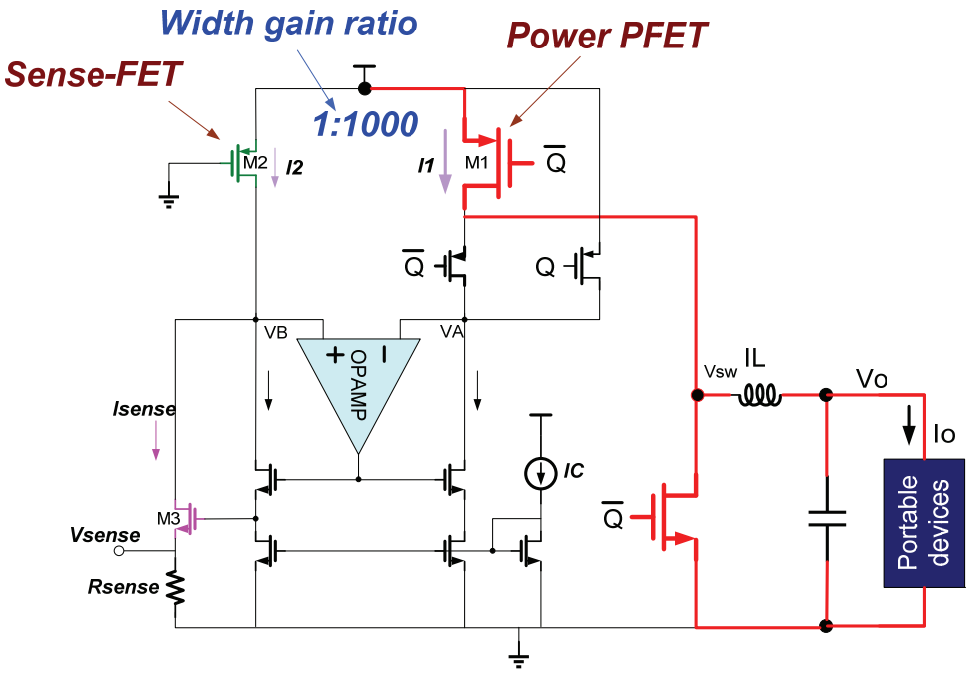

Figure 4-11. On chip sense-FET current sensor [4-14]

In the sense-FET method, a mirror transistor (sense FET, M2) to the power PFET (M1) with a width gain ratio of 1:1000 or a smaller value is placed close to the power PFET with a common drain terminal. An operational amplifier (opamp) is utilized to adjust the source voltage of the sense FET to be approximately equal to the phase node of the ISBC so that the Vds of the sense FET and the power FET are almost same. As a result, the current I_2 flowing through the sense FET will be related to the current I_1 flowing through the power FET with the same gain ratio if the opamp is ideal. If we ignore the branch currents in the control loop, we obtain $I_L = I_1$, $I_{sense} = I_2$. Thus, the inductor

current of the ISBC is reduced by the ratio of 1000:1 to be the Ids current I_{sense} of the output transistor (M3). I_{sense} is finally converted to a voltage signal V_{sense} at the output terminal of the current sensor.

Challenges with the sense-FET method are significant when the switching frequency is beyond 4MHz [4-17, 4-18] and the turn-on time of the control power FET is in the range of one hundred nanoseconds. Because the Vds of the power FET is only several tens of milli-volts, in order to ensure that the sense accuracy stays larger than 90% in a wide range of load current, the opamp meets a severe limitation between the speed and accuracy. Furthermore, the design of output transistor (M3) and R_{sense} is difficult when the ISBC load current variation is in a wide range. In addition, if the quiescent current of the sensor is too large, the sense accuracy will be degraded and the efficiency of the ISBC in the light load condition will be sacrificed too. Up to now, the reported maximum switching frequency utilizing the sense FET technique is 2.5MHz [4-18] with a quiescent current of $43\mu A$.

Utilizing the sense-FET method for the CIF has one more design issue about the maintenance of the current gain ratio 1:1000 when some of the power FET subcells are disabled.

The $2^b - 1$ high resolution comparators in the flash A/D converter are another circuit issue in the CIF implementation. The delay-line A/D converter [4-2] in Figure 4-3 is a good substitute from the view point of power consumption and area. However, the delay cell's performance is remarkable sensitive to the variation of process and temperature, so the period of the sampling clock is prone to mismatch that of the delay line.

4.1.2.5 Summary

In summary, there are three issues that CIF needs to address to make the automatic segmentation practical.

1). Temperature compensation.

The load current does not provide temperature information, so CIF cannot compensate the change of Rdson because of temperature from the algorithm point of view.

2). Constant current gain ratio

The power FET width of the ISBC will dynamically change due to segmentation which simultaneously changes the current gain ratio of the sense-FET current sensor. Maintaining current sensing accuracy in a wide range of load current adds significant difficulty to the circuit design.

3). High switching frequency and efficiency at light load condition

In chapter 1, we mentioned that the power width segmentation is particularly preferred in the applications who address both high switching frequency and power efficiency in the light load condition. However, both of the application specifications seriously challenge CIF implementation. The current sensor circuit design will become extremely tough when the switching frequency is beyond 4MHz and the on time of the control power FET is less than one hundred nanoseconds. The maximum switching frequency among the reported on chip current sensors is 2.5MHz [4-18]. At the same time, CIF requires a high performance opamp and $2^b - 1$ high performance comparators to obtain a b-bit digital segmentation. The quiescent current of CIF is hard to control because many high performance circuits are necessary.

4.2 Vsw pinning segmentation

In order to overcome the aforementioned issues in CIF and efficiently implement the automatic segmentation in a 4MHz ISBC, a Vsw pinning segmentation (VswPS) technique is proposed and its principle is introduced in this subsection.

4.2.1 VswPS concept

Vsw is the voltage level of the phase node in the ISBC illustrated in Figure 1-2 and its value is given in (4-10).

$$V_{SW} = \begin{cases} V_{in} - R^{P\_seg}\left(I_o - \dfrac{\Delta I_L}{2} + \dfrac{\Delta I_L}{DT}t\right) & t \in [0,\ DT_{SW}] \\ -0.65 & t \in [DT_{SW},\ T_{SW}] \end{cases} \tag{4-10}$$

in which $T_{SW} = 1/f_{SW}$ is the switching period of the ISBC and the body diode forward voltage is assumed to be 0.65V.

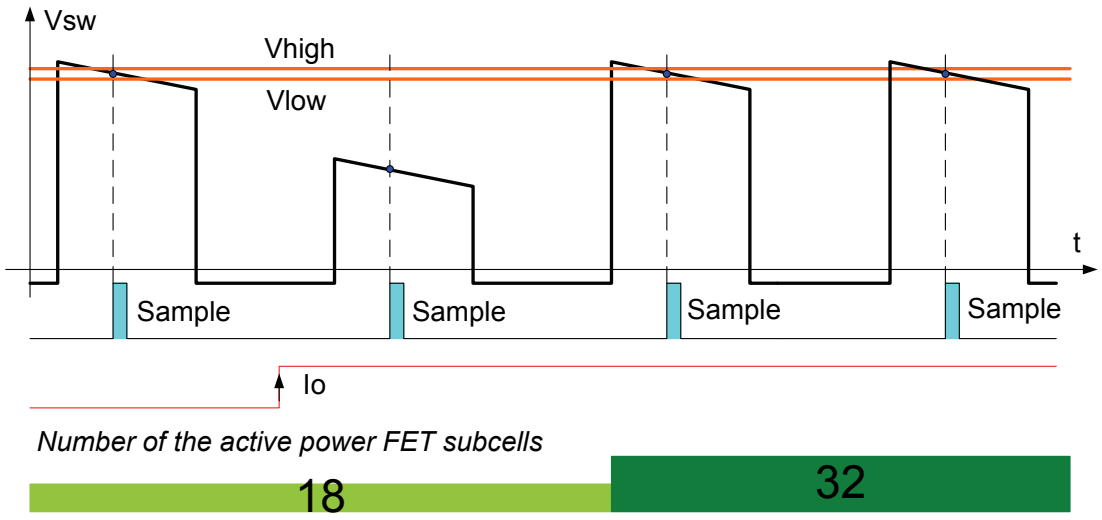

Figure 4-12. Concept of Vsw pinning automatic segmentation

The concept of the VswPS is to keep the sampled value of V_{SW} in a specific zone illustrated in Figure 4-12 in all load conditions via adjusting the value of R_{dson} with the power width segmentation technique. The sampling time is set in the period when the control power FET (PMOS) turns on. The specific zone is characterized by two threshold voltages V_{high} and V_{low} provided by the bandgap voltage generator.

Figure 4-12 illustrates the conceptual adjustment process when the load current suddenly increases at some moment. When the load current increases, from (4-10) Vsw will drop and in Figure 4-12 Vsw drops below both the V_{high} and V_{low}. The value of Vsw is recorded at the sampling moment and compared with V_{high} and V_{low} and the comparison result is transmitted to the power FET manager. Consequently, in order to return the Vsw back to the zone, 14 more power FET subcells are activated. As a result, the Vsw is pinned again in the zone between the V_{high} and V_{low}. For the sake of circuit design, the power FET width adjustment process is synchronous with the switching clock of the ISBC.

Figure 4-12 shows an ideal adjustment of the power stage width in which the adjustment is completed in one clock period. In the practical case, the adjustment process is in fact processed by a state machine illustrated in Figure 4-13. For the VswPS technique in the Figure 4-13, there are seven groups of power FET subcells as that described in the subsection 3.4.4 and Figure 3-15.

$k0$ in Figure 4-13 is the comparison result between the sampled value of Vsw denoted by V_{SW}^{Sample} and the V_{low} in Figure 4-12 and its definition is given in (4-11). $k1$ is the comparison result between V_{SW}^{Sample} and the V_{high} in Figure 4-12 and its definition is given in (4-12).

$$k0 = \begin{cases} 0 & V_{SW}^{Sample} \geq V_{low} \\ 1 & V_{SW}^{Sample} < V_{low} \end{cases} \tag{4-11}$$

$$k1 = \begin{cases} 0 & V_{SW}^{Sample} \geq V_{high} \\ 1 & V_{SW}^{Sample} < V_{high} \end{cases} \tag{4-12}$$

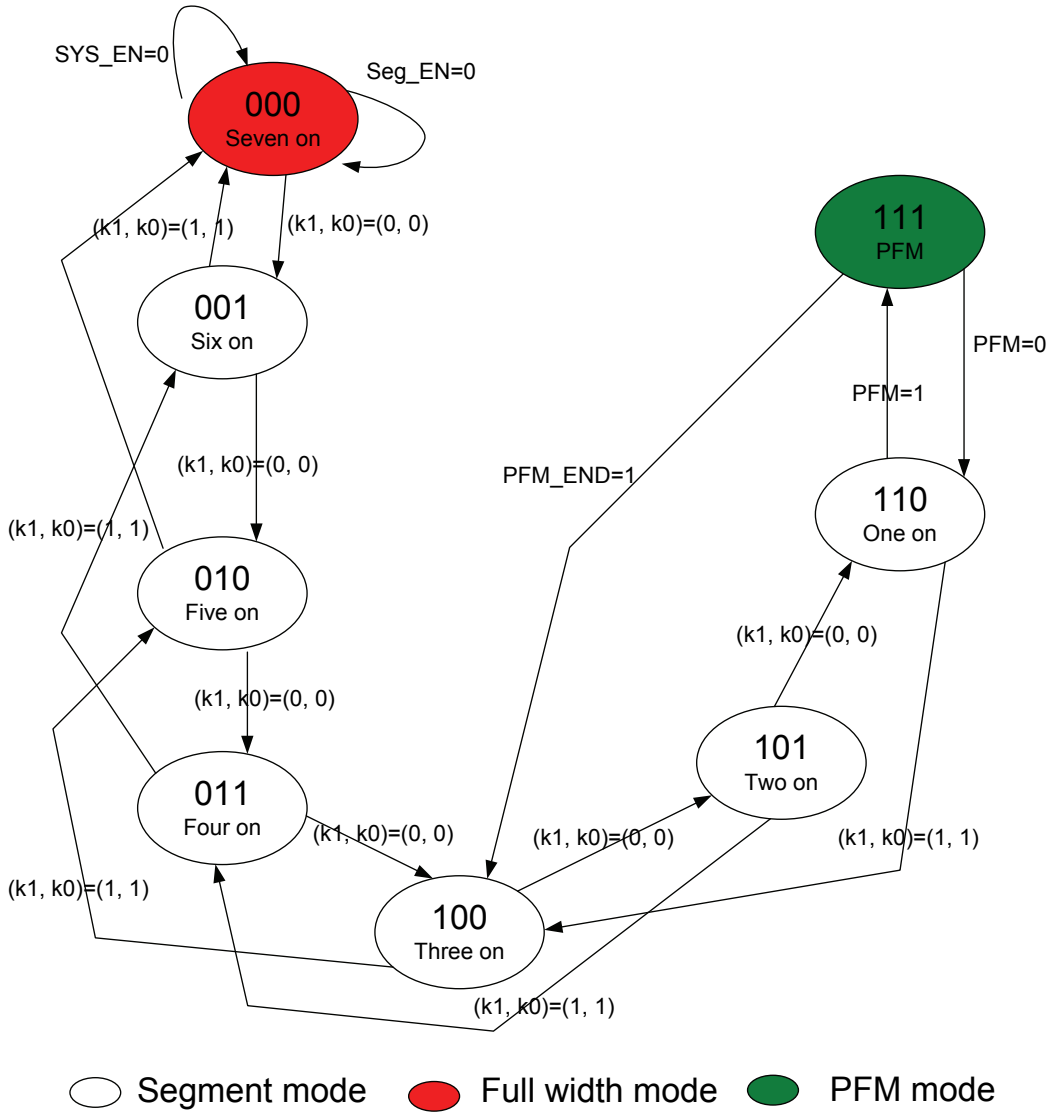

Figure 4-13 State machine to support the VswPS technology

The general segmentation actions in the Figure 4-12 and Figure 4-13 are summarized in the Table 4-4.

Table 4-4. General segmentation actions to the result of Vsw comparison.

[k0, k1] status	[0,0]	[0,1]	[1,0]	[1,1]
Segment action	**Disable one active group labeled by the minimal number until all groups are disabled.**	**No action**	**No action**	**Enable two inactive groups labeled by the maximal number until all groups are enabled.**

4.2.2 VswPS principle and parameter setting

4.2.2.1 VswPS principle

Following the definition of $R_{dson} = \frac{K_{Rdson}}{mW_P}$ in (4-1) and the equation (4-2), the equation (4-3) is rewritten in (4-13) for the case of the optimal segmentation.

$$R^{P\_seg} I_o = \frac{\sqrt{K_{Rdson}\ K_{Cap}}}{D + (1-D) K_{Rdson}^{N/P}} \tag{4-13}$$

in which

$$K_{Rdson}^{N/P} = \frac{R^N}{R^P} = \frac{0.0619(1 + 4.54\, V_{dd})}{(1 + 0.625\, V_{dd})} K_W \tag{4-14}$$

Thus, if we ignore the variations of the coefficients K_{Rdson} and K_{Cap} due to load current and segmentation and ignore the impact of current ripple, the optimal segmentation means that the value of $R^{P\_seg} I_o$ is constant in a wide range of load current.

The difference between VswPS and CIF from an algorithm perspective is that the former tries to maintain a constant value of $R^{P\_seg} I_o$ in (4-13) via adjusting m while the

latter adjusts m in (4-3) to be linearly proportional to I_o. Thus, in theoretical and ideal condition, there is no difference between VswPS and CIF. However, when we consider the practical implementation and the impact of Rdson deviation, VswPS will be a much better solution than CIF. The comparison will be clarified in the next subsections.

4.2.2.2 Segmentation resolution bits

Segmentation resolution bit determines how many segmentation options are implemented in ISBC and is denoted by b in the previous subsections. For example, in subsection 3.4.4, seven groups of power FET subcells provide seven kinds of options for segmentation, so the segmentation resolution bit is $b = 3$.

The zoning band width setting depends on the resolution bit of segmentation and grouping of the subcells. Assuming segmentation resolution bit is b and the total subcells are evenly distributed in 2^b groups, the required zoning band width is given in (4-15). The band width is the minimal Vsw variation when a b-bit evenly distributed segmentation is applied.

$$V_{high} - V_{low} = \frac{1}{2^b - 1} R^{P\_seg} I_o^{set} = \frac{1}{2^b - 1} \frac{\sqrt{K_{Rdson} K_{Cap}}}{\left[D + (1-D) K_{Rdson}^{N/P}\right]} \tag{4-15}$$

in which I_o^{set} is the load current value where all power FET subcells are expected to be activated. In this dissertation, I_o^{set} is chosen to be the maximum load current and equals 0.4A.

For the specified ISBC in the Chapter 3 with $V_{in} = 3.0V$, $D = 0.5$, $K_W = 2$ and $W_P = 0.11m$, we obtain $K_{Rdson} = 0.3514\Omega \cdot m$ from (4-5), $K_{Cap} = 0.0032\, W/m$ from (4-6) and $K_{Rdson}^{N/P} = 0.6295$ from (4-14). Applying (4-15) to the ISBC, the relationship between the segmentation resolution bit and the zoning band width is listed in Table 4-5.

Table 4-5. Zoning band width for different segmentation bit
in the case of power FET subcells even distribution

b-bit	1	2	3	4	5
Zoning band width $V_{high} - V_{low}$ (mV)	41.2	13.7	5.9	2.7	1.3

The table 4-5 implies the difficulty encountered in the implementation of a comparator when the segmentation bit is larger than 2, if we apply the even distribution segmentation.

The even distribution segmentation is in fact not a correct choice. First, all of the analysis on segmentation is based on the assumption of CCM operation and the assumption will be violated when the load current is smaller than 0.08A. Second, the R_{dson} in (4-2) is inversely proportional to the number of active subcells. Thus, if we evenly distribute the subcells, the R_{dson} variation between two groups will be very different. Third, if we return to the Figure 3-10 and Figure 3-11, we notice that the efficiency improvement headroom in the heavy load range is far less than that in the light load range. These considerations will be detailed in the next subsections.

4.2.2.3 Permanently active subcells

Permanently active subcells refer to the subcells which are always in the active condition regardless of the load condition. The permanently active subcells constitute the #1 group in Figure 3-22. The number of permanently active cells is based on the critical load current for CCM operation.

All of the aforementioned discussions about the segmentation are based on two assumptions. The first one is that the ISBC works in the CCM operation and the second one is that the current ripple is ignorable. For the ISBC application in the dissertation, the critical load separating the CCM and the DCM is 0.08A. From (4-2) or (4-13), we conclude that the corresponding optimal number of subcells will be 6 or 7 at the critical

load condition 0.08A, provided that we select 32 subcells for the maximum load condition of 0.4A.Thus, in this dissertation we select 8 out of total 32 subcells to be permanently active subcells.

4.2.2.4 VswPS convenient grouping

Assuming for some specific load condition the number of active subcells is m and the equation (4-13) is satisfied due to automatic segmentation, the Vsw difference due to the addition of one more active subcell is given by (4-16).

$$\Delta V_{SW} = \frac{\sqrt{K_{Rdson}\ K_{Cap}}}{(m+1)\left[D+(1-D)K_{Rdson}^{N/P}\right]} \tag{4-16}$$

The equation (4-16) indicates that if we evenly distribute subcells, the resultant Vsw difference per one active subcell will be inversely proportional to the number of active subcells. In another words, the zoning band width set for a large m might be much smaller than that for a small m. And, a width set for large m is used to determine the performance specification of the comparator as that discussed in Table 4-5.

In order to reduce the resolution expectation on the comparator and make the Vsw difference per group well balanced for the whole load range under consideration, a VswZS convenient grouping strategy is adopted.

The principle of VswZS convenient grouping is very simple. On the basis of the discussion in the subsection 4.2.2.2, we intentionally select more subcells in the group labeled with smaller number so as to sufficiently enlarge the Vsw variation between two succeeding groups. The rule applies to all groups except the last group reserved for the permanently active subcells. The VswZs convenient grouping is characterized by (4-17) and (4-18) for a segmentation ISBC with g subcell groups, where we denote the number

of subcells in the i th group with m_i and the number of total subcells with M . The g th group is denoted as the last group reserved for the permanently active subcells.

$$M - m_g = \sum_{i=1}^{g-1} m_i \tag{4-17}$$

$$m_1 \geq m_2 \geq \cdots \geq m_{g-1} \tag{4-18}$$

One kind of VswZS is implemented in the Figure 3-22 and Chapter 3. The first group includes 8 active subcells so $m_1 = 8$; the second group includes 6 active subcells so $m_2 = 6$; the third group includes 4 active subcells so $m_3 = 4$; the forth, fifth and sixth groups separately includes 2 subcells so $m_4 = m_5 = m_6 = 2$; and the final seventh group includes 8 permanently active subcells so $m_7 = 8$.

4.2.2.5 Threshold voltage setting

When the VswPS convenient grouping method is determined, the two threshold voltages V_{high} and V_{low} for the VswPS technique are set together. V_{low} is selected to be 6mV less than the Vsw value when all power FET subcells are active and the load current is the maximum, which is listed in (4-19). V_{high} given in (4-20) is selected to be the 6mV larger than the Vsw value of the ISBC when only the group including the permanently active subcells is active and the load current is the critical current for CCM.

$$V_{low} = V_{dd} - R^P \; I_o^{\max} - 6mV \tag{4-19}$$

$$V_{high} = V_{dd} - R^P \frac{M}{m_g} I_o^{Critical} + 6mV \tag{4-20}$$

in which $I_o^{\max}$ is the maximal load current.

For the ISBC application in the dissertation, $V_{in} = 3.0$ V, $I_o^{\max} = 0.4$ A, $M = 32$ and $m_g = 8$. R^P is calculated from (3-9) as $\frac{0.197}{(1 + 4.54 * V_{dd})W_P} = 122.5 m\Omega$. Thus, from (4-19) and (4-20) we conclude that $V_{high} = 2.967V$, $V_{low} = 2.945$ V and the zone band width is 22mV. Comparing the zone band width with the value in Table 4-5, we conclude that the band width will be improved by 267% for a 3-bit segmentation, provided that the VswPS convenient grouping discussed in the subsection 4.2.2.4 is adopted.

The existence of two thresholds implies that the ranges of load current in respective to the active power FET subcells will present a hysteresis type difference between the load current increasing case and the decreasing case. Figure 4-14 depicts the range of load currents for the load current decreasing case, while Figure 4-15 illustrates the range for the load current increasing case. The red circles in Figure 4-14 and the green circles in Figure 4-15 indicates the load current at which the number of active subcells will change in response to the comparators' output signal. After the change, the value of Vsw will suddenly dip or rise as shown in Figure 4-14 and Figure 4-15. The load ranges in Figure 4-14 and Figure 4-15 are summarized in Table 4-6. The four blue dashed lines in blue color in Figure 4-14 and Figure 4-5 highlights the $\pm 2mV$ dead-zone of the comparator, which may slightly changes the data reported in the Table 4-6.

Table 4-6. Load range of different subcells in the ISBC with VswPS technique

	32 cells	24 cess	18 cells	14 cells	12 cells	10 cells	8 cells
Drop case (Typical & selected)	0.269-0.4A	0.202-0.269A	0.152-0.202A	0.118-0.152A	0.101-0.118A	0.084-0.101A	<0.084A
Rise case (Typical)	0.337-0.4A	0.253-0.337A	0.196-0.253A	0.168-0.196A	0.140-0.168A	0.112-0.140A	<0.112A

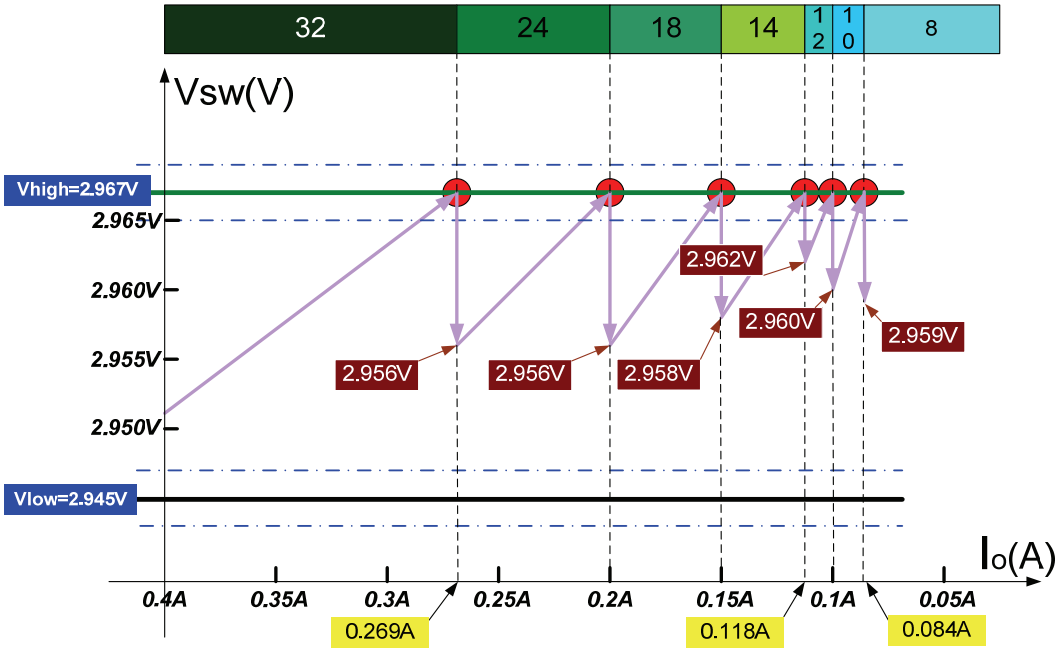

Figure 4-14. The ranges of load current for different number of active subcells when the load current decreases

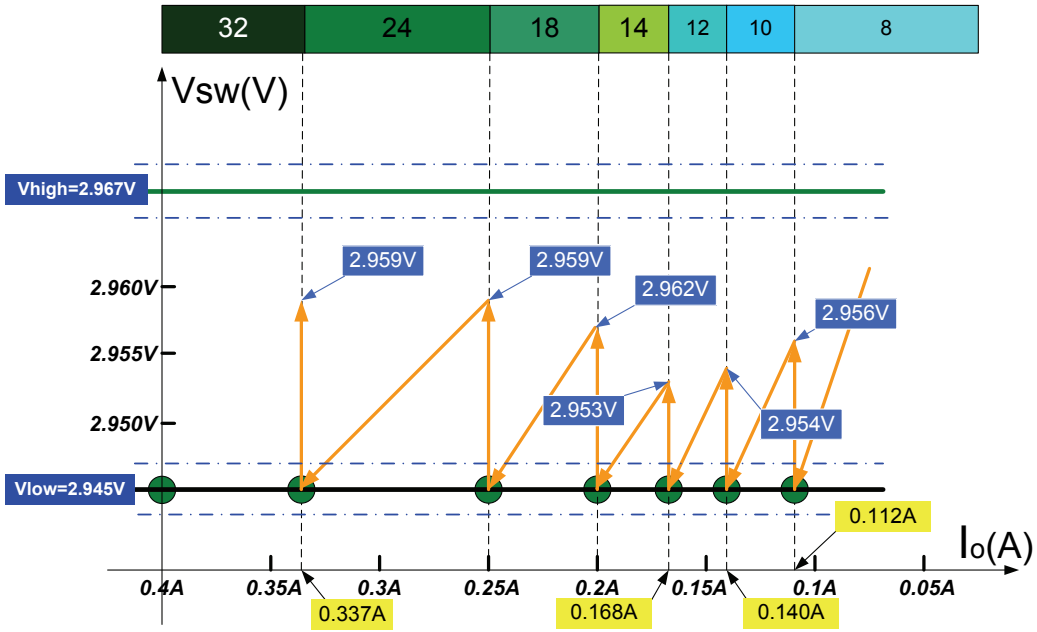

Figure 4-15. The ranges of load current for different number of active subcells when the load current increases

4.2.2.6 VswPS typical operation

Figure 4-16 illustrates the typical operation of the VswPS technique in the time domain when the load current decreases from $I_o^{\max} = 0.4$ A to $I_o^{Critical} = 0.08$ A. The subcells group's disabling actions follow the state machine introduced in Figure 4-13. From Figure 4-16, it is observed that six switching periods are needed to change the number of active subcells from 32 to 8.

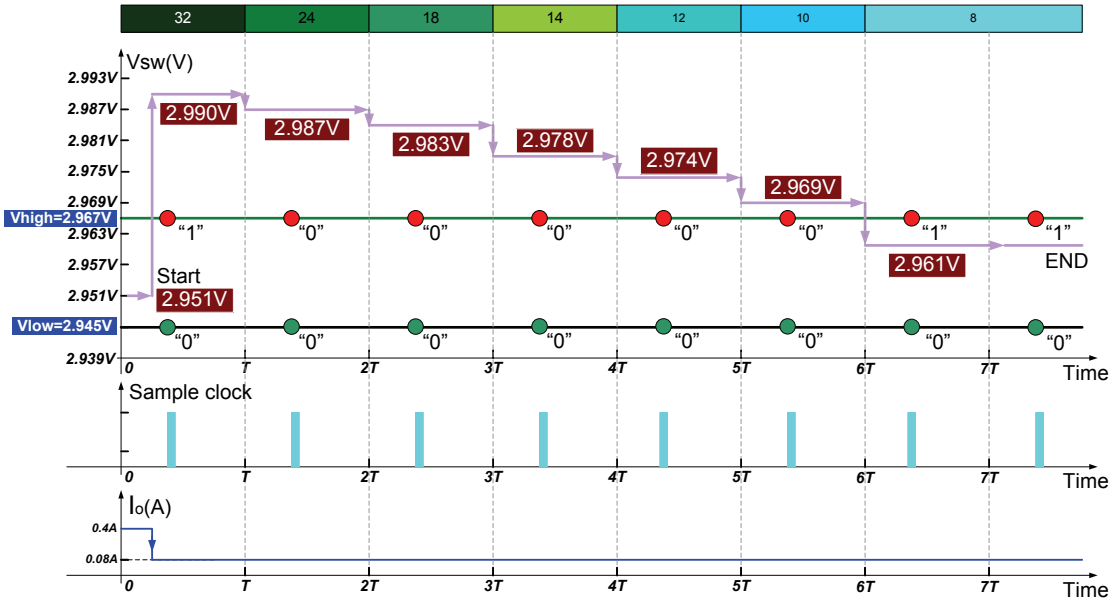

Figure 4-16. Typical VswPS operation when the load current decreases.

The typical operation of the VswPS technique in the time domain is illustrated in Figure 4-17 when the load current increases from $I_o^{Critical} = 0.08$ A to $I_o^{\max} = 0.4$ A. From Figure 4-17, it is observed that six switching periods are needed to change the number of active subcells from 8 to 32.

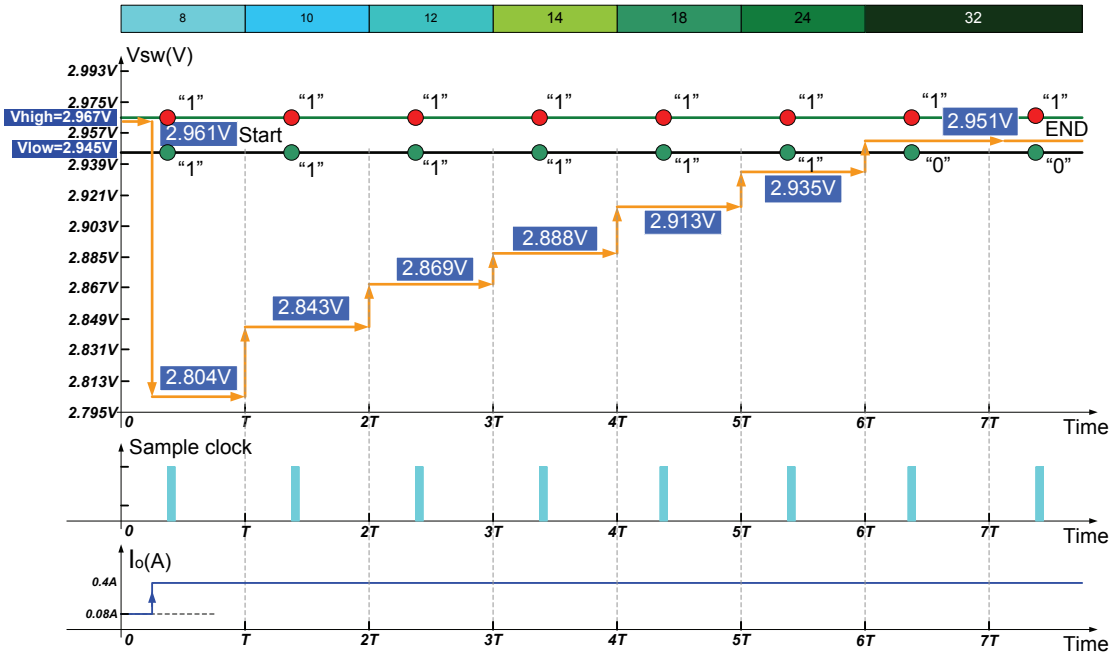

Figure 4-17. Typical VswPS operation when the load current increases.

The typical operation in Figure 4-17 conflicts with the action clarified in the state machine in Figure 4-13. The motivation for the action design in the state machine is to quickly turn on more power FET subcells when the load current suddenly increases so as to avoid the overheating of the metal due to a large value of R_{dson} and benefit the safe consideration of ISBC. Thus, the finally selected operation of the VswPS technique in the time domain follows the state machine in Figure 4-13 and is illustrated in Figure 4-18 when the load current increases from $I_o^{Critical} = 0.08\,\text{A}$ to $I_o^{\max} = 0.4\,\text{A}$. In contrast to the load current decreasing case, two groups of subcells are simultaneously activated when Vsw is smaller than V_{low}. In comparison with Figure 4-17, the number of switching period in Figure 4-18 to complete the change of the number of active subcells from 8 to 32 is improved from 6 to 3.

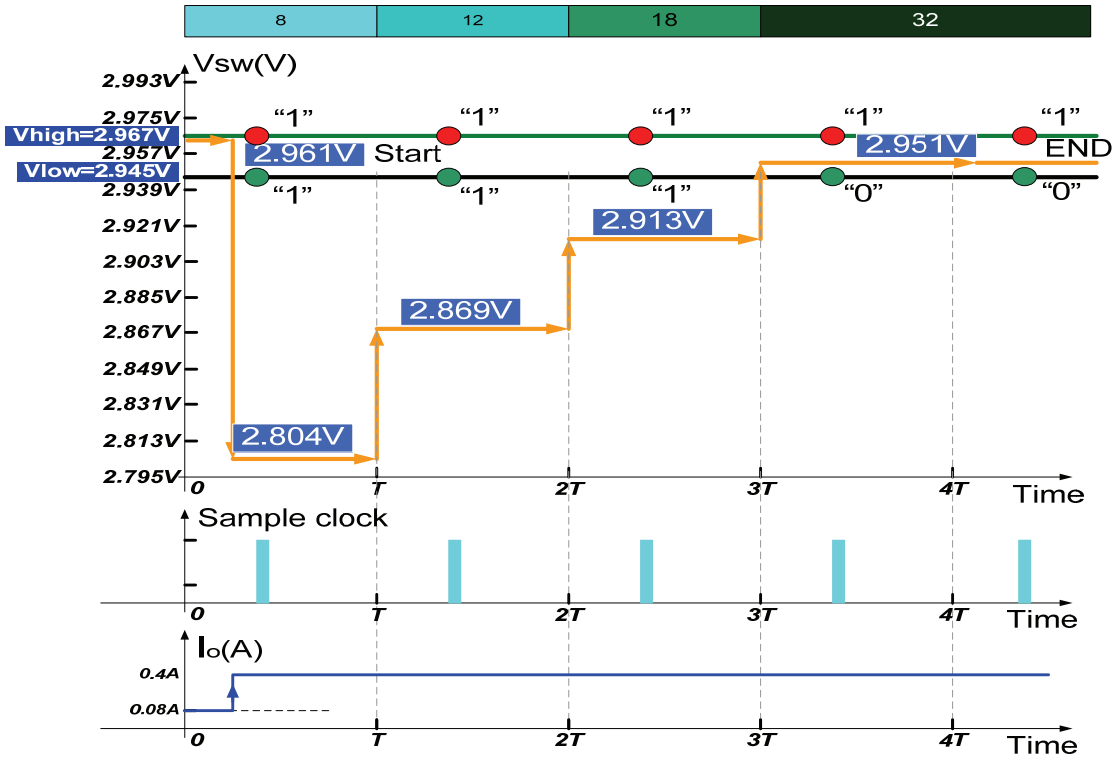

Figure 4-18. Selected VswPS operation when the load current increases.

4.2.3 Rdson compensation

The VswPS technique has automatic temperature compensation to approach the optimal segmentation in a real case. As discussed in subsection 4.1.2, the CIF only does segmentation action according to the load current information and the action follows (4-3). Thus, the number of subcells in CIF will not change when the R_{dson} changes because of the temperature variation.

The VswPS technique maintains the product of R^{P_seg} and I_o to be a constant value and the action follows (4-13). If we denote the constant value in the right hand part of the (4-13) with X_{seg} and relate R^{P_seg} to $m^{(opt)}$ and M, (4-13) is rewritten in (4-21).

$$m^{(opt)} = \frac{M}{X_{seg}} R^{P\_seg}\ I_o \tag{4-21}$$

in which $X_{seg} = \frac{\sqrt{K_{Rdson}\ K_{Cap}}}{D + (1-D)K_{Rdson}^{N/P}}$ is the constant value implemented by two temperature independent threshold voltages V_{high} and V_{low}.

(4-21) shows that when R^{P_seg} increases because of high temperature, more subcells will be turned on to maintain the existence of (4-13). Consequently, the dependence of R^{P_seg} due to temperature is degraded by an increasing number of active subcells in parallel.

4.3 VswPS solid state circuit

The simplified functional diagram of an ISBC with the VswPS technique applied is illustrated in Figure 4-19. The pins in Figure 4-19 are described in Table 4-7.

This subsection will introduce two specific functional blocks in the Figure 4-19. The first one is a segment sensor and the second one is a PWM/PFM mode shifter.

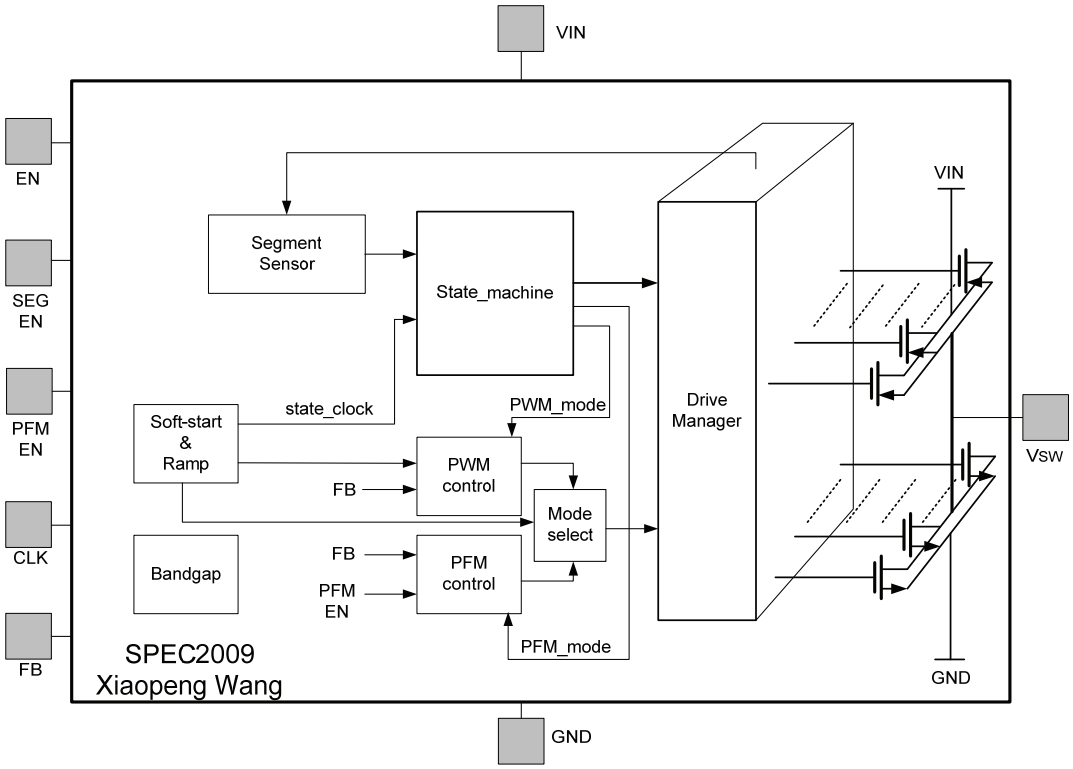

Figure 4-19. Simplified functional diagram of the ISBC chip with VswPS technology

Table 4-7. Pin description of the ISBC chip with VswPS technique

Pin	***description***
"EN"	enable signal of the ISBC
"SEG_EN"	enable signal of the VswPS technique
"PFM_EN"	enable signal of the PFM mode;
"CLK"	input clock signal toggling with a frequency expected as the switching frequency of the ISBC
"FB"	Output voltage feedback
"VIN"	input voltage of the ISBC
"GND"	Ground of the ISBC
"Vsw"	Phase node of the ISBC

The ramp block in Figure 4-19 simultaneously generates a ISBC system clock for mixed-signal timing and a ramp signal for PWM control. An analog phase locked loop is included in the ramp clock to synchronize the two aforementioned signals with an input clock signal with a specified ISBC switching frequency.

The PWM control block integrates a type-III compensator on chip and the opamp uses a two stage Folded cascode architecture. The PFM control block integrates a regular type of constant on-time controller. The on time is set to be 240 nanoseconds. The driver manager integrates the logic circuit in Figure 3-22 with a soft start compatible circuit and a 6 nanosecond dead-time setting circuit.

4.3.1 Segment sensor

The function block diagram of the segment sensor is illustrated in Figure 4-20. The input signals are V_{high}, V_{low}, V_{SW} and the ISBC system clock denoted by ***SYS_CLK***. The output signals are $k1$ and $k0$ shown in the state machine in Figure 4-13. The 2-bit delay controller provides the flexibility to adjust the start moment of the sampling pulse in Figure 4-12 and its output is denoted by the ***Seg_CLK***. The output signals of the latched pipeline comparator are respectively ***K1_com*** and ***k0_com***. The timing shift matches the worst-case conversion delay of the comparators so that the D-Q flip-flop can record the output signals (***K1_com*** and ***k0_com***) of the comparators properly and output ***K1_pre*** and ***k0_pre***. The output of the timing shift is denoted by ***Rec_CLK***. The reliable operation block is designed to ensure safe operation of the VswPS technique during load transient events.

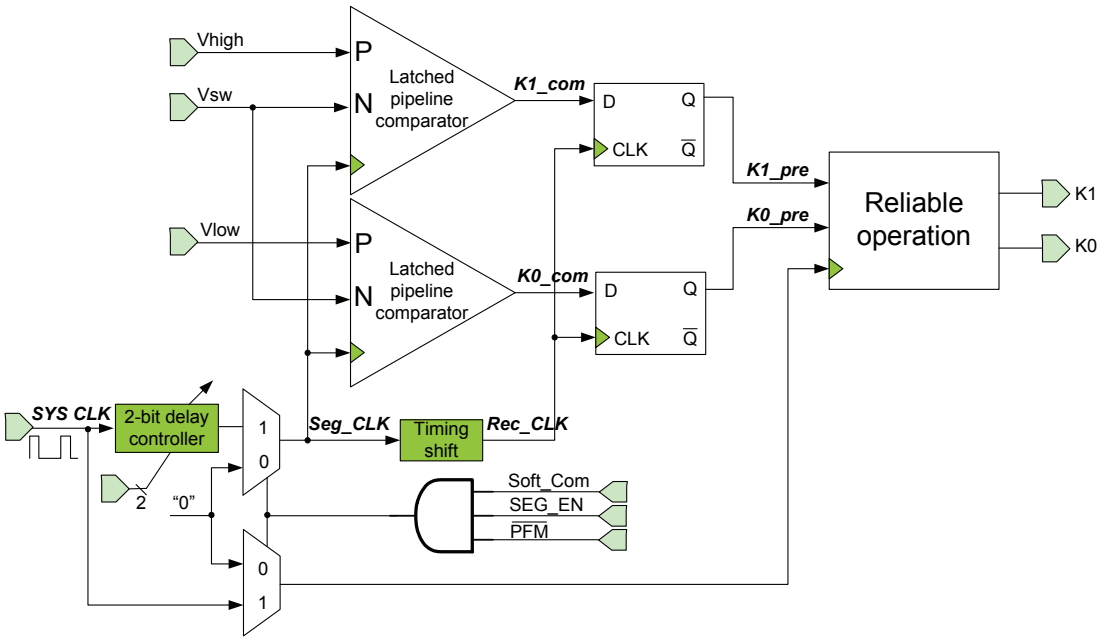

Figure 4-20. Simplified functional diagram of segment sensor

4.3.1.1 Latched pipeline comparator

The power-delay products in different architectures of comparator were compared in [4-19] and the impact of offset and its cancellation were introduced in [4-20]. In order to meet the $\pm 2mV$ resolution expectation defined in subsection 4.2, the two-stage latched pipeline comparator architecture [4-19] illustrated in Figure 4-21 is selected together with an input sample circuit to remove the common-mode input voltage of signals to be compared.

The schematic of the input sample circuit, type-A sense amplifier and type-B sense amplifier are respectively given in Figure 4-22, Figure 4-23, and Figure 4-24.

As the 1st stage sense amplifier is the downstream cascaded stage of the input sample circuit, there is an equivalent load circuit at the output terminals of the input sampling circuit. From the Figure 4-23, when ***Latch (Seg_CLK)*** signal is "gnd", a common mode negative feedback loop is formed which forces the voltage levels of the nodes ***Arm_L*** and

Arm_R to be identical. Nodes ***Leg_L*** and ***Leg_R*** are also subject to this behavior. Thus, the equivalent load circuit of the input sampling circuit behaves like the transmission gate in Figure 4-22.

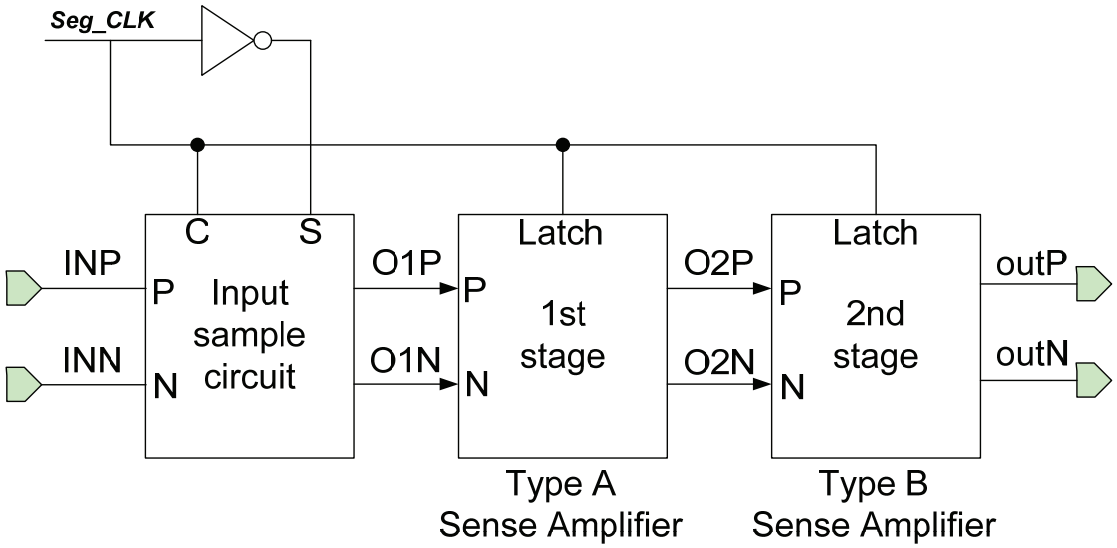

Figure 4-21. Two stage latched pipeline comparator architecture

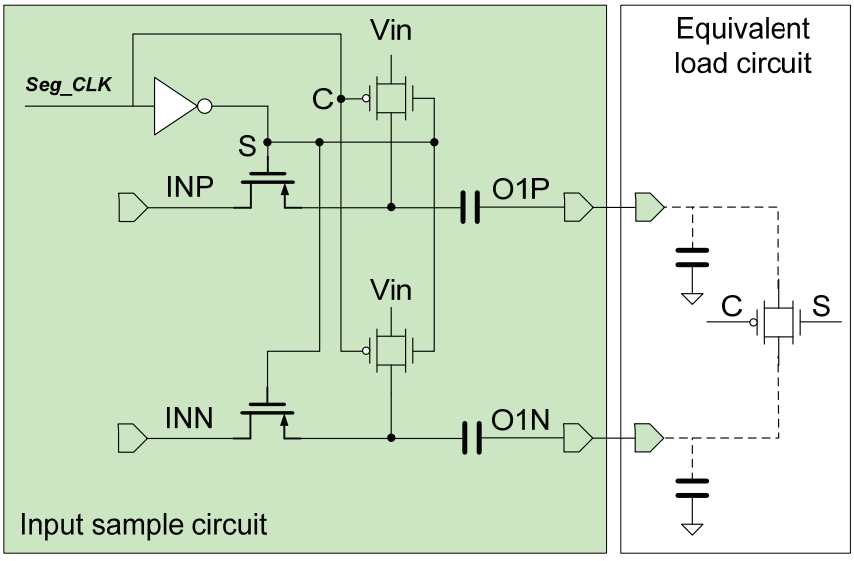

Figure 4-22. Schematic of input sampling circuit

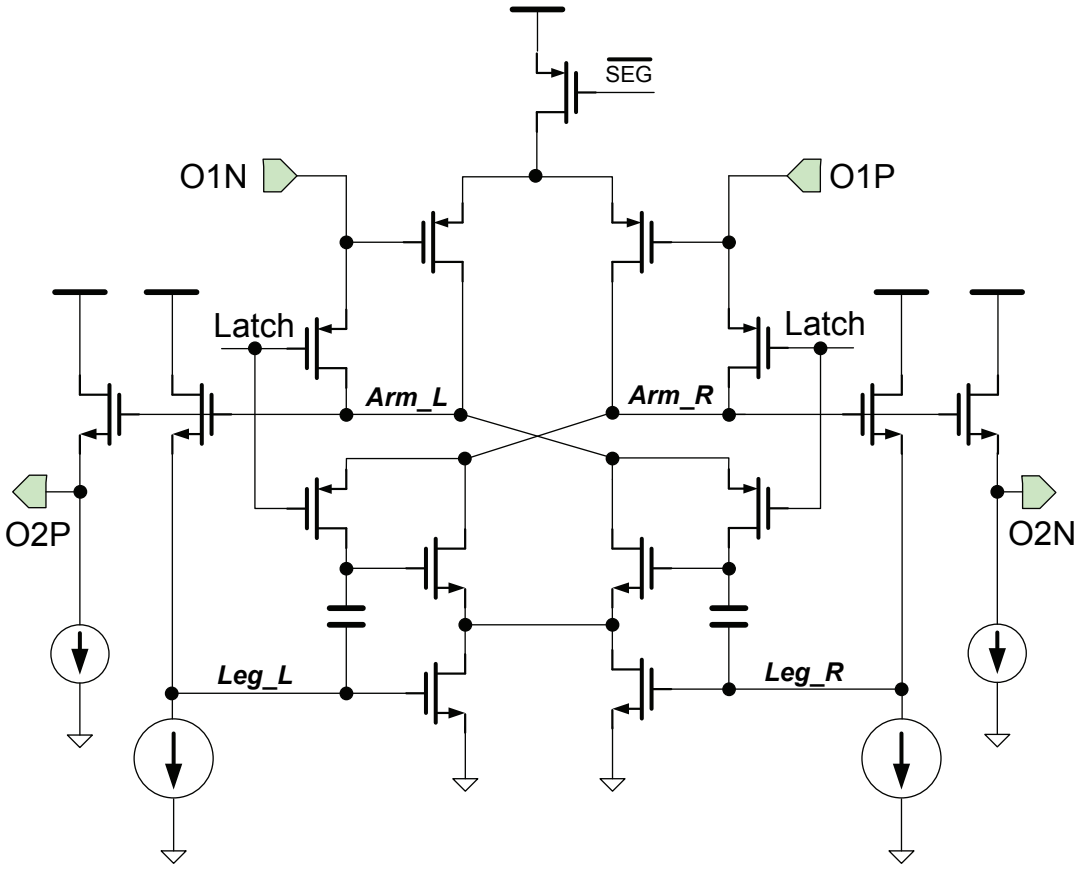

Figure 4-23. Schematic of type A sense amplifier

When the ***Latch (Seg_CLK)*** signal is "Vdd", the aforementioned negative feedback loop in Figure 4-23 will be disabled because the four PMOS gates are turned off. At the same time, a positive feedback loop is formed with the help of two floating capacitors so that the slight difference between the two input signals O1P and O1N can be effectively amplified. The $\overline{SEG}$ signal in the Figure 4-23 will decrease power leakage when the ISBC works in extremely light load conditions where the duty cycle is modulated by PFM and the SEG (segmentation function) is disabled.

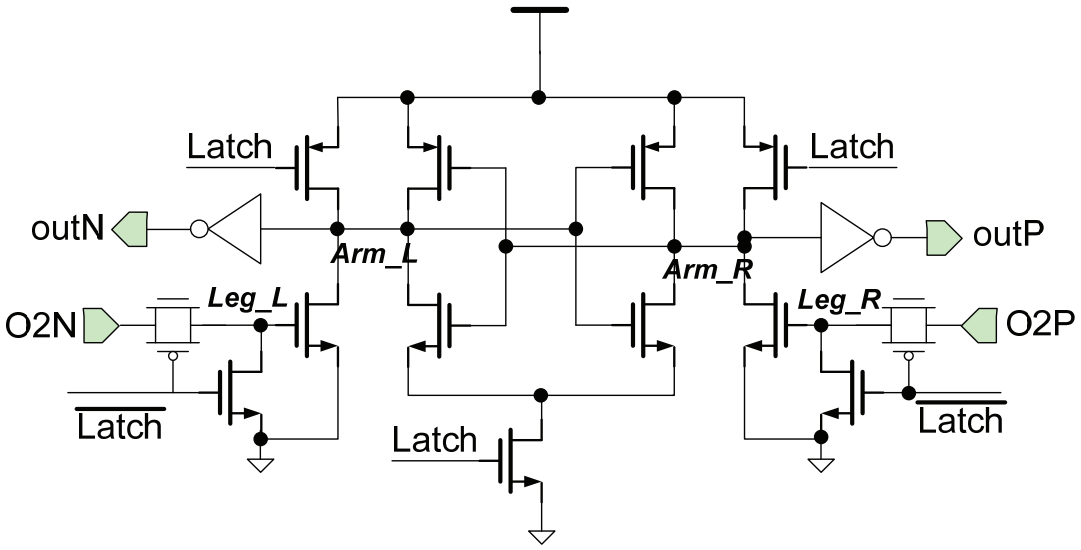

Figure 4-24. Schematic of type B sense amplifier

The type B sense amplifier in Figure 4-24 does not use negative feedback to cancel offset, but instead directly charges or discharges the junction nodes to "Vdd" or "gnd". When the ***Latch (Seg_CLK)*** signal is "gnd", the two nodes ***Arm_L*** and ***Arm_R*** in Figure 4-24 will be charged to "Vdd" and the other two nodes ***Leg_L*** and ***Leg_R*** in Figure 4-24 will be discharged to "gnd" at the same time. The input signal's difference is full swing amplified when the ***Latch (Seg_CLK)*** signal is "Vdd" with the aid of the cross coupled regenerative inverters.

The comparator is simulated with Spectre simulator and the BSIM3V3.1 level 49 Spice model [4-7] in a 100°C environment, and "TT" as the selected process corner. The Vsw signal is connected to the "N" in Figure 4-23 ("INN" terminal in Figure 4-21), and the threshold voltage V_{high} or V_{low} is connected to the "P" in Figure 4-23 ("INP" terminal in Figure 4-21). The segmentation function (SEG) is intentionally disabled for the first two second out of every ten seconds. Figure 4-25 shows the output signals of two comparators in Figure 4-20 when the Vsw shifts among four different values, respectively being 2mV larger or smaller than V_{high} and 2mV larger or smaller than V_{low}.

Figure 4-26 is the zoomed in view of the Figure 4-25 at time interval between 15.5us and 16.5us.

From Figure 4-25 and Figure 4-26, we conclude that the comparator works correctly when the Vsw deviates from V_{high} or V_{low} by $\pm 2mV$. Thus, the designed comparator can satisfy the technical specifications given by the VswPS technique in subsection 4.2.2.

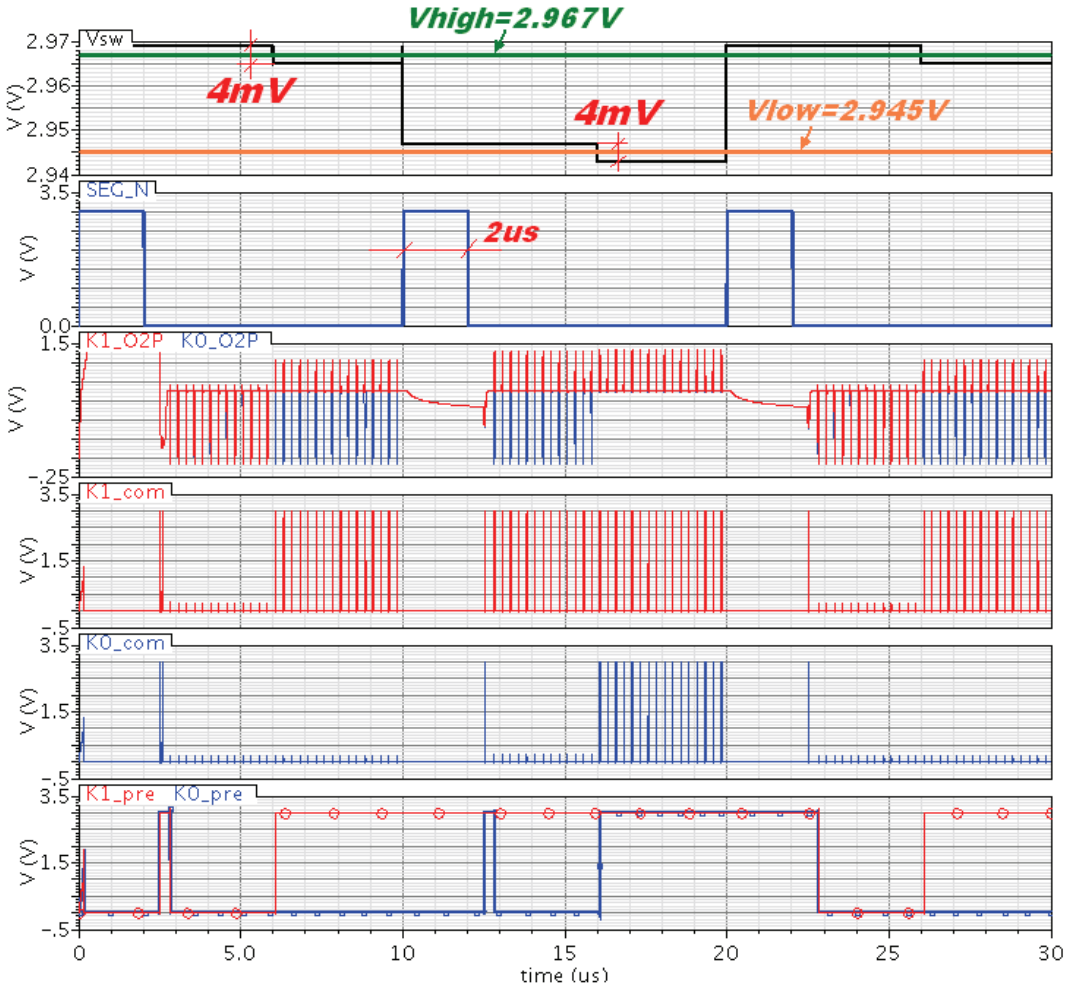

Figure 4-25. Performance verification of the comparator in 100°C and TT corner.

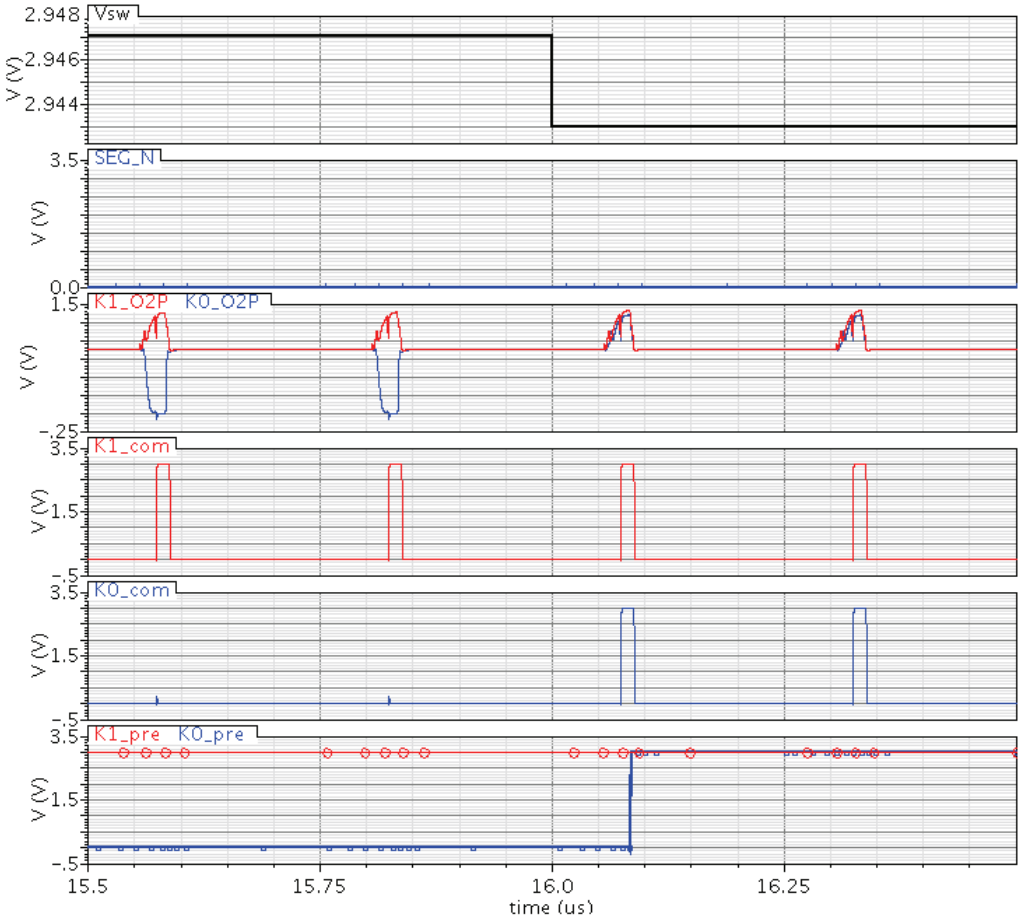

Figure 4-26. Zoomed in view of Figure 4-28.

The simulation in Figure 4-25 is repeated in a different environment where the temperature is 0°C and the selected corner mode is “FF”. The simulation results are shown in Figure 4-30. From Figure 4-27, we verify that the designed comparator can also satisfy the technical specifications given by the VswPS technique in subsection 4.2.2 when the temperature is 0°C and the corner mode is “FF”.

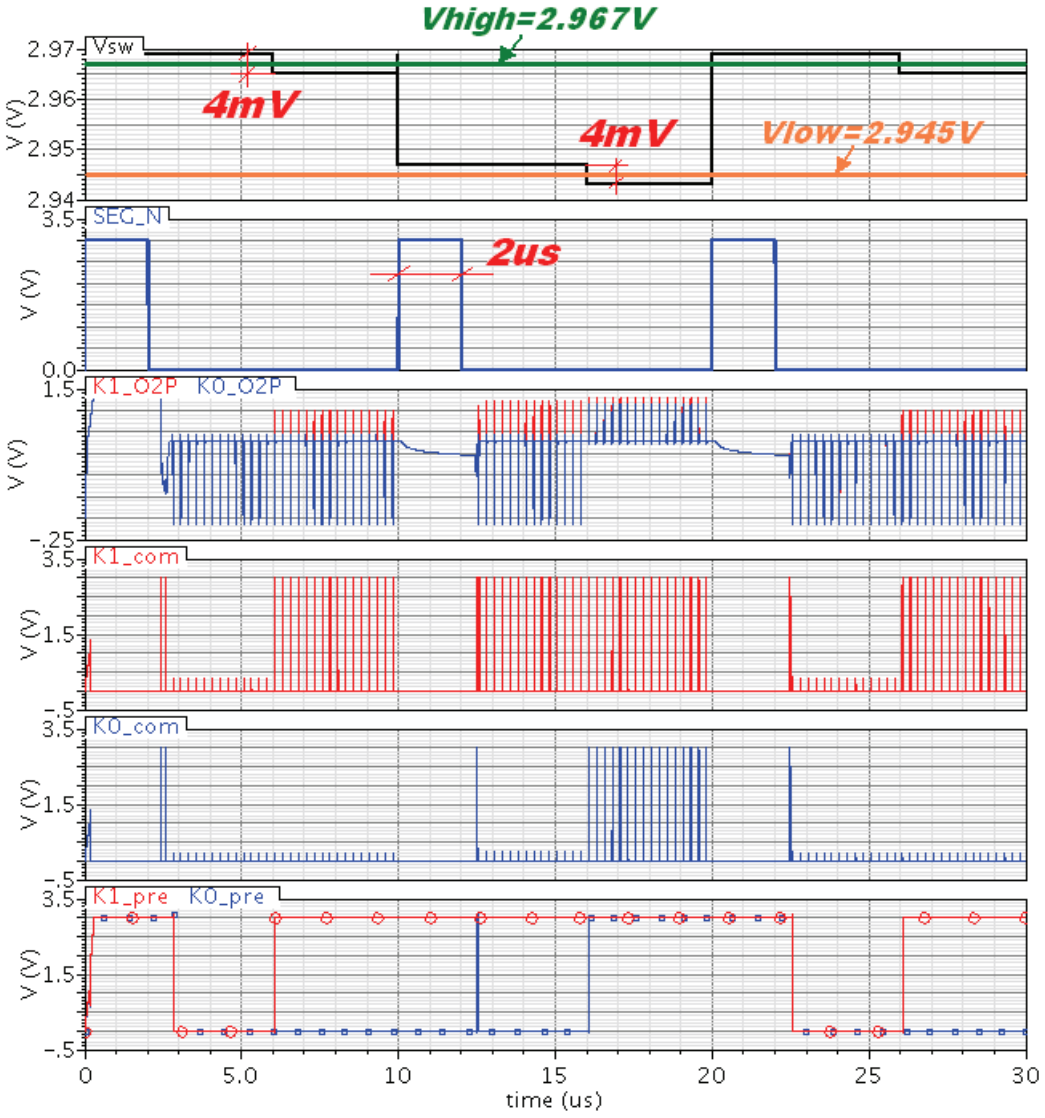

Figure 4-27. Performance verification of the comparator in 0°C and FF corner.

4.3.1.2 Reliable operation block

The duty cycle of the ISBC will temporarily oscillate around its steady state value when the load current changes. On the basis of the operation principle of the VswPS technique in Figure 4-12, in the worst case, there might be several switching periods during which the sampled Vsw value does not correctly represent the practical inductor current. In order to avoid the malfunction of the segmentation circuit because of these false sampling values, the sampling values should be screened completely.

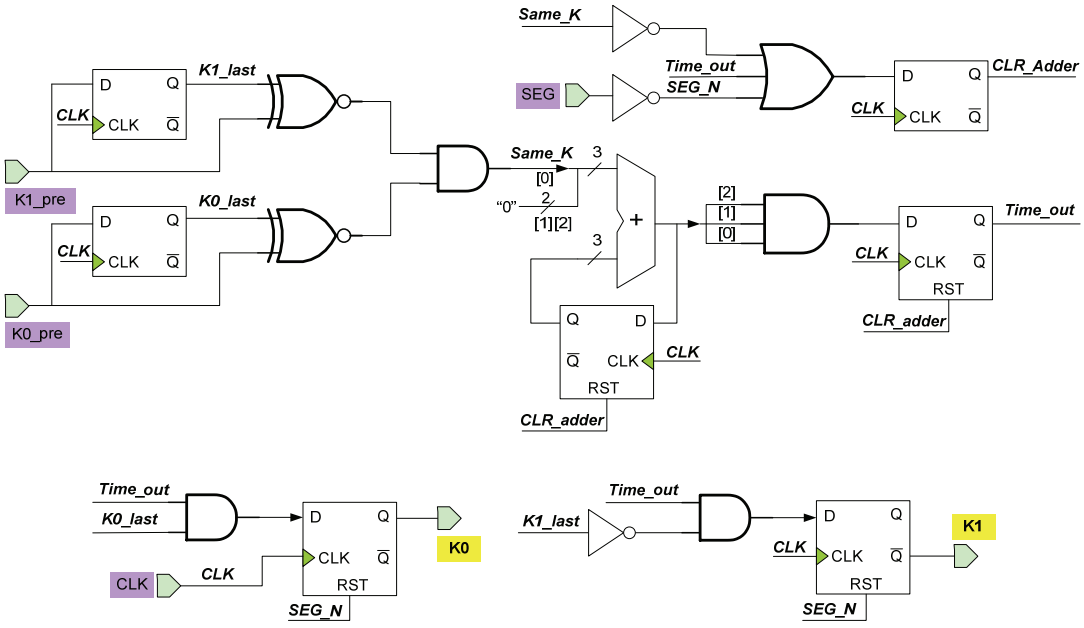

Figure 4-28. Functional diagram of the reliable operation block

The reliable operation of the VswPS technique during the load transient events is ensured by a reliable operation block. The block is one component of the segment sensor shown in Figure 4-20 and its functional diagram is shown in Figure 4-28. The function of the reliable operation block is to count the number of clock in which both $K1\_pre$ and $K0\_pre$ do not change. If the number is larger than nine, the output signal $K1$ will take

the value of $K1\_pre$ and the output signal $K0$ will take the value of $K0\_pre$. Otherwise, $K1$ will be "1" and $K0$ will be "0". According to the state machine in Figure 4-13 and Table 4-4, the case when $K1$ is "1" and $K0$ is "0" implies power FET width locking.

We repeat the simulation in the subsection 4.3.1.1 in an environment with 100°C temperature and TT corner model and show the output signals of the reliable operation block in Figure 4-29.

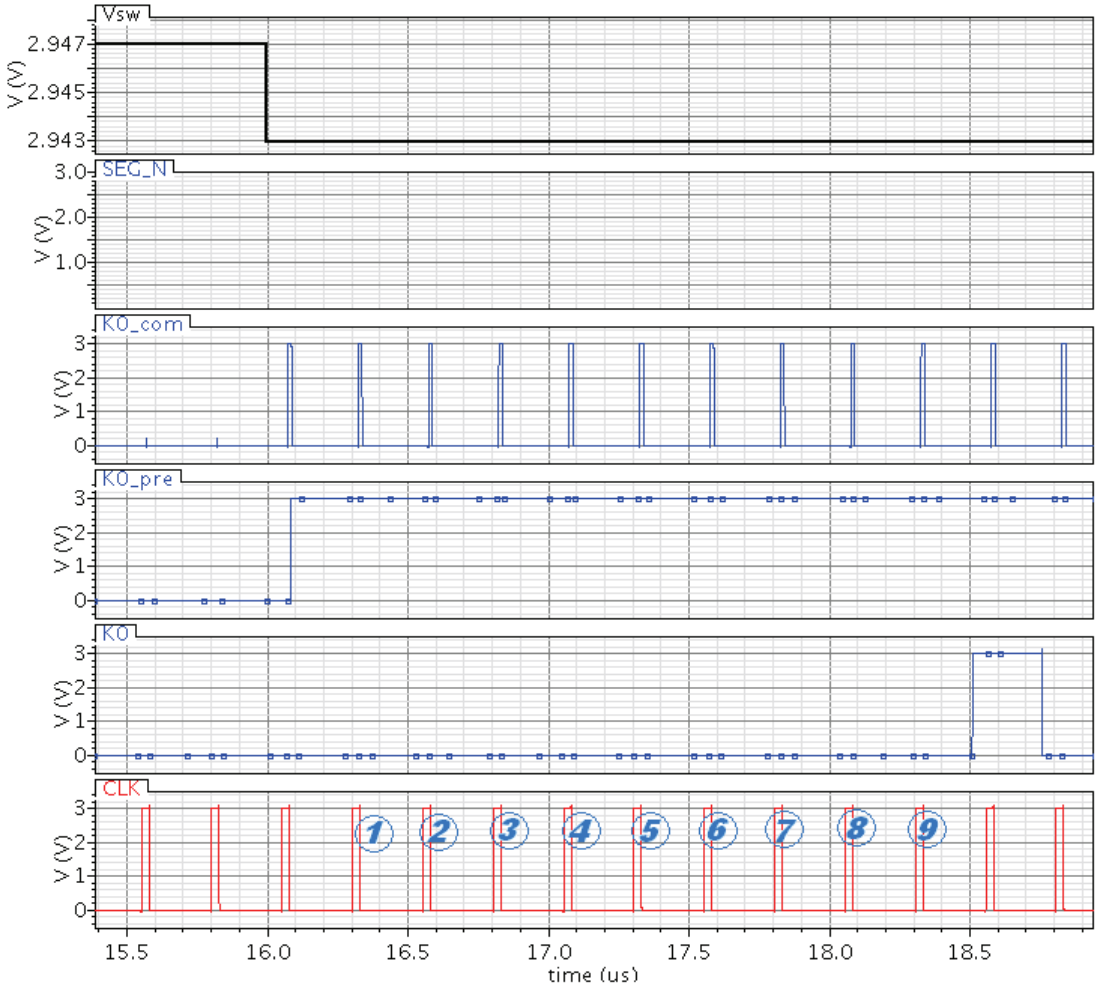

Figure 4-29. Example waveforms of the reliable operation block

4.3.1.3 Current consumption and silicon layout

The current consumption of the segment sensor is reported in Table 4-8.

Table 4-8 Current consumption of the segment sensor

Block name	Two latched pipeline comparators	Reliable operation	Other delay and timing shift blocks
Segment Turn on (PWM mode)	97.5uA	23.6uA	155.8uA
Segment Turn off (PFM mode)	4.26uA	2.7uA	8.84uA

The silicon layout of the segment sensor is shown in Figure 4-30.

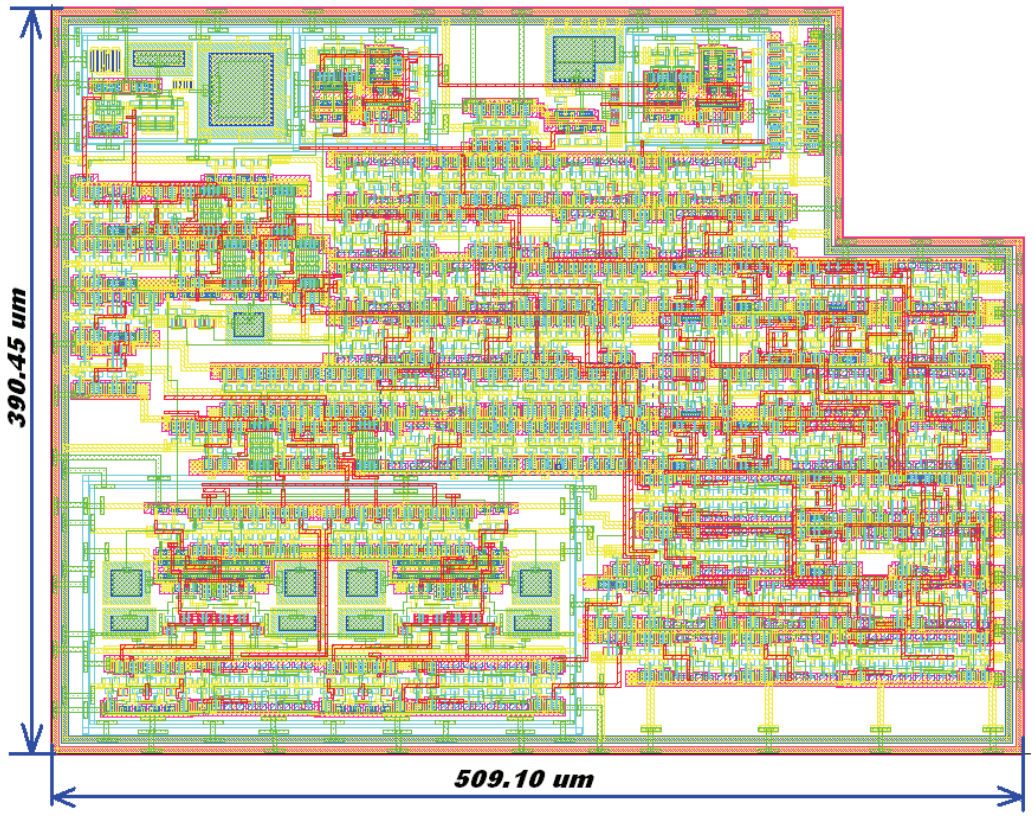

Figure 4-30. Silicon layout of the segment sensor for VswPS technology.

4.3.2 PFM/PWM mode transfer

The PFM operation of the ISBC is imperative for the benefit of power efficiency when the load current is extremely low as discussed in subsection 1.2.2. On the other hand, the characteristic of the PFM determines that its switching frequency will increase when the load current increases. When the load current is high enough, the on time of the PFM might no longer be small enough to keep the power inductor current in the discontinuous conduction mode (DCM). Thus, PFM mode usually is used alongside with PWM mode. PFM applies when the load current is low and PWM applies when the load current is high. In this dissertation, the critical load current between the PFM and PWM is designed to be 0.08A.

The mode transfer between PFM and PWM is a design issue in practical. The reason is that the small signal transfer function and inductor current waveform of the ISBC in PFM are significantly different from those in PWM. Thus, we cannot apply a linear controller simultaneously for both of them. [4-21]

There are several papers focusing on the mode transfer between PFM and PWM [4-2, 4-22, 4-23, 4-24, 4-25]. Most of them [4-2, 4-22, 4-23, 4-24] used current sensor to determine the moment of mode transfer. As we discussed in the subsection 4.2, the implementation of a lossless on-chip sense-FET current sensors is difficult when the switching frequency of the ISBC is higher than 2MHz. Therefore, the state-of-art current sensor based implementations are only implemented to the ISBC where the switching frequency is in the range between 200KHz and 2MHz. In contrast to the other implementations, [4-25] measures the duty cycle width to indirectly obtain the current to determine when to transfer from PWM to PFM. However, the duty cycle width is weakly dependent on the load current unless that the power efficiency of the ISBC is very poor. Furthermore, the duty cycle width is difficult to measure in practice because of the switching noise pollution on the board. Thus, when the switching frequency is larger than 1MHz, the design in [4-25] is difficult to implement.

This subsection will introduce a mode transfer method between the PFM and PWM which does not need the current sensor but utilizes the VswPS technique. The state machine in Figure 4-13 manages the transfer from PWM to PFM. At the same time, a counter records the number of switching periods in a specified time interval. When the number exceeds six, the ISBC activates the transfer from PFM to PWM.

4.3.2.1 PWM operation

The functional blocks to implement PWM operation for the ISBC are illustrated in Figure 4-31. The silicon layout of the integrated type-III PID compensator is shown in Figure 4-32, which is designed in chapter 3. The typical waveforms of the ISBC in PWM operation are illustrated in Figure 4-33 in which the load current changes between 0.1A and 0.02A.

From Figure 4-33, it is observed that in PWM operation, the inductor current shape is constant in two load conditions and the inductor current will go to negative when the load current is as small as 0.02A. Also, the switching frequency is constant in two different load conditions.

The constant inductor current shape and constant switching frequency ensure that the small signal transfer function of the ISBC will not change in all load current conditions so that only one PID linear regulator is enough for the ISBC. However, from the viewpoint of efficiency, PWM operation is not a good choice for the light load condition. The charging/discharging and driver loss will be the same as that in the heavy load condition because of the constant switching frequency, though the output load current is much smaller. Furthermore, a negative inductor current in the light load condition implies that extra loss will be generated during the charging/discharging of the inductor.

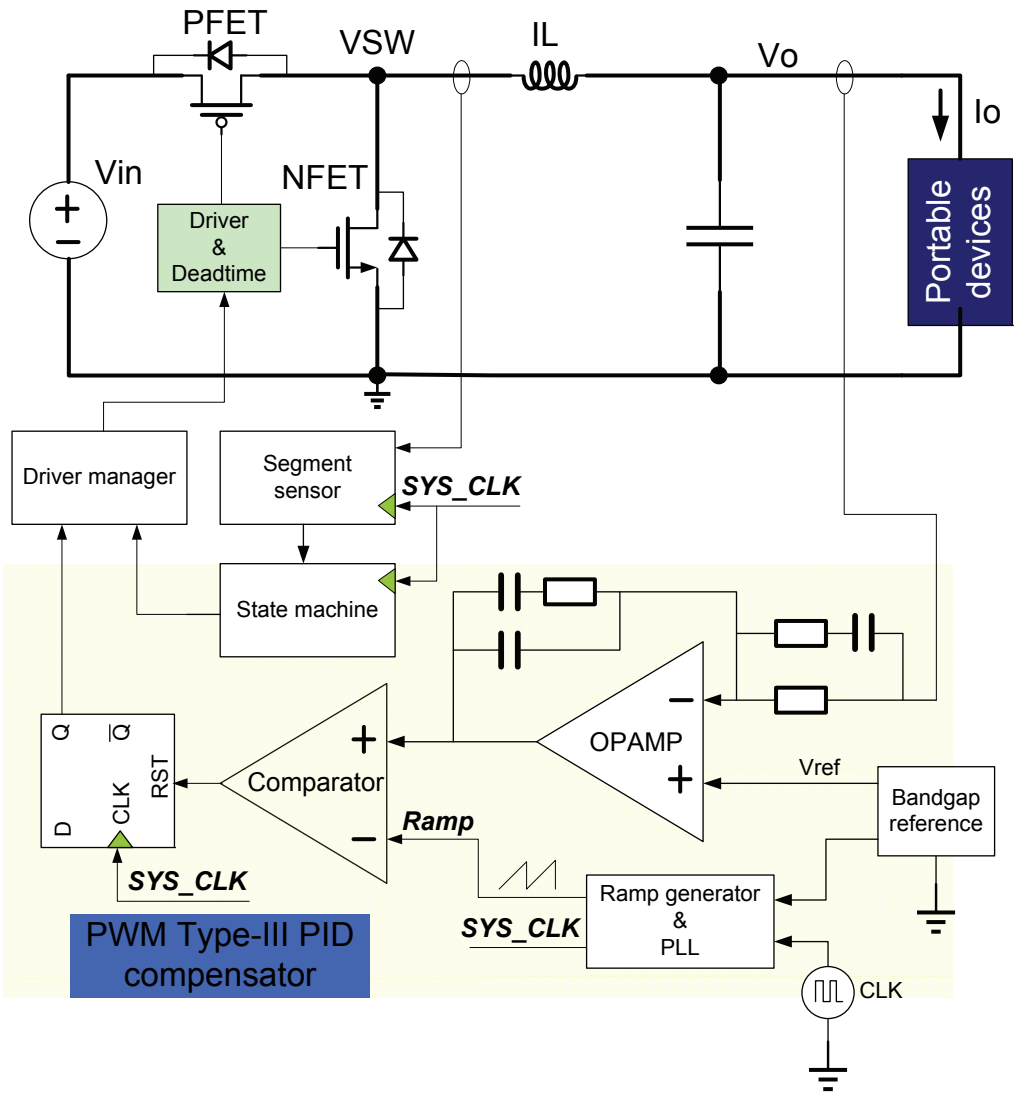

Figure 4-31. Functional blocks to implement the PWM operation

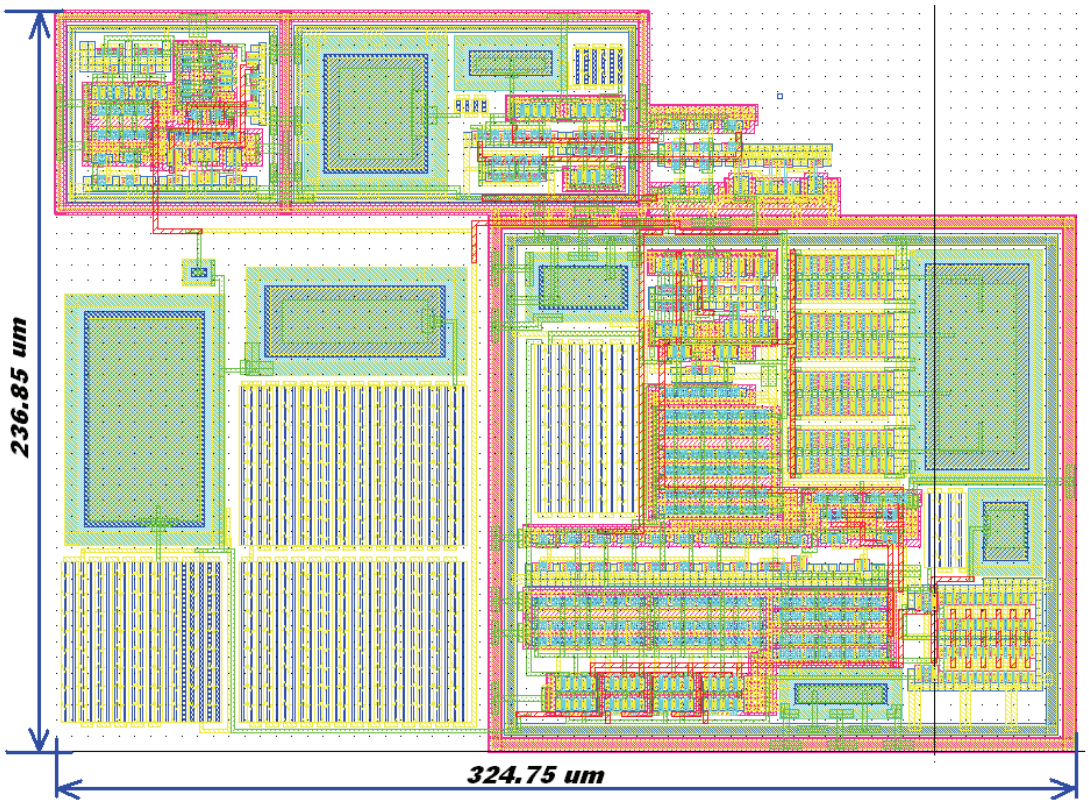

Figure 4-32. Silicon layout of the integrated type-III PID compensator

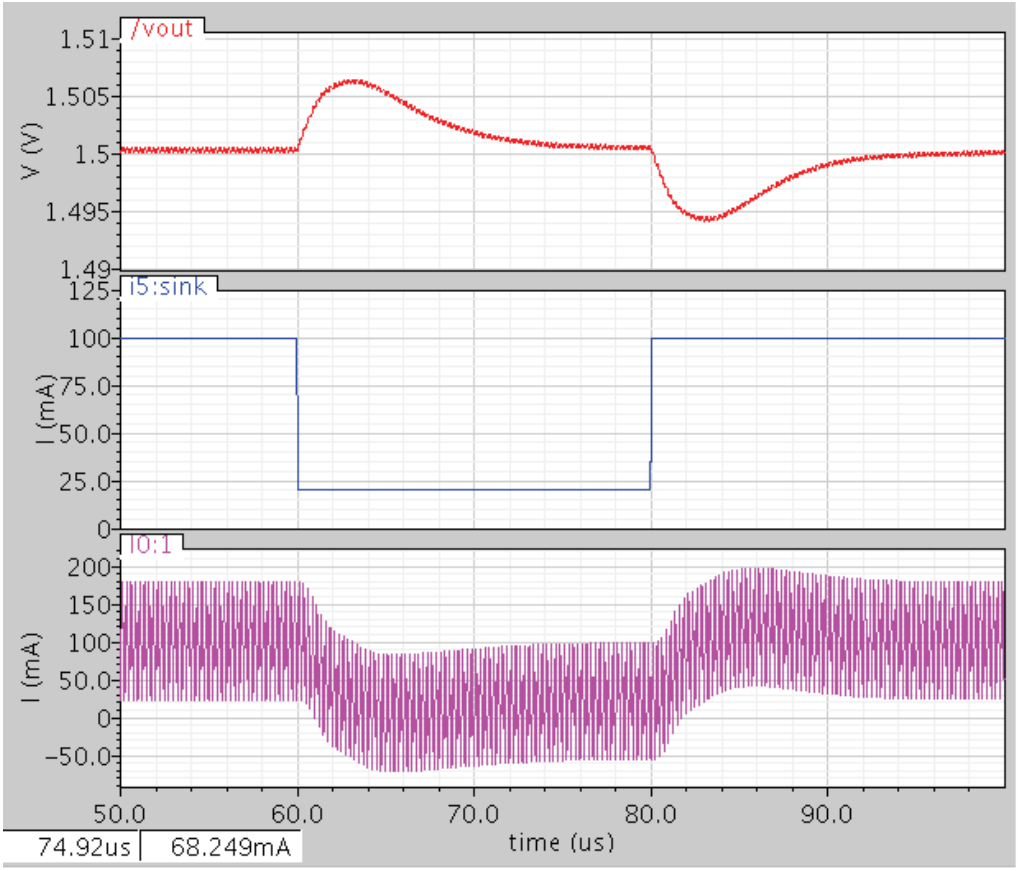

Figure 4-33. Typical waveforms in PWM operation

4.3.2.2 PFM operation

In PFM operation, the ISBC will work in discontinuous conduction mode (DCM) [4-26] so as to avoid forming a returning current loop which degrades power efficiency. The DCM is realized by turning off the synchronous power NMOS FET when the inductor current is smaller than zero. The typical inductor and load current waveforms in DCM are shown in Figure 4-34. I_L is the power inductor current; I_o is the load current; T_{SW} is the switching period; t_{on} is the on time of the control power PMOS which is a constant value set by designer when the ISBC is regulated by the constant on-time control; t_{off} is the on

time of the synchronous power NMOS, after which the inductor current discharging is terminated via turning off the synchronous power NMOS.

If we ignore the power loss, the average inductor current in one switching period should be equal to the load current. Thus, the switching frequency of the ISBC will present a linearly proportional relationship with the load current as the equation in (4-22).

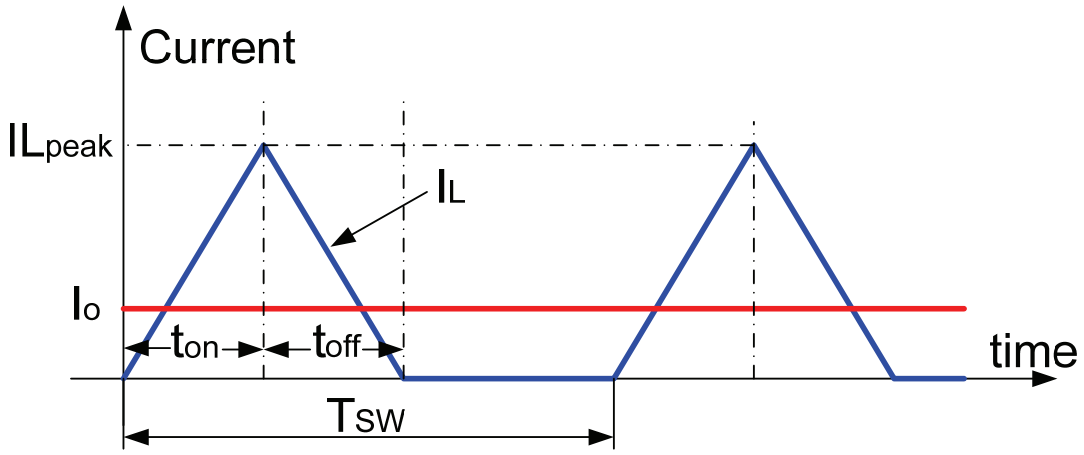

Figure 4-34. Typical inductor and load current waveforms in DCM

$$f_{SW} = \frac{2 V_o L}{(V_{in} - V_o) V_{in} t_{on}^2} I_o \tag{4-22}$$

Because the conduction times of power PMOS and power NMOS are constant and the switching frequency is load current related as that given in (4-22), the conduction loss will be linearly proportional to the load current. The same conclusion can be made for the switching loss which is linearly proportional to switching frequency. Thus, in DCM operation, the power efficiency of the ISBC will remain constant if we ignore the quiescent current of the circuits [4-22].

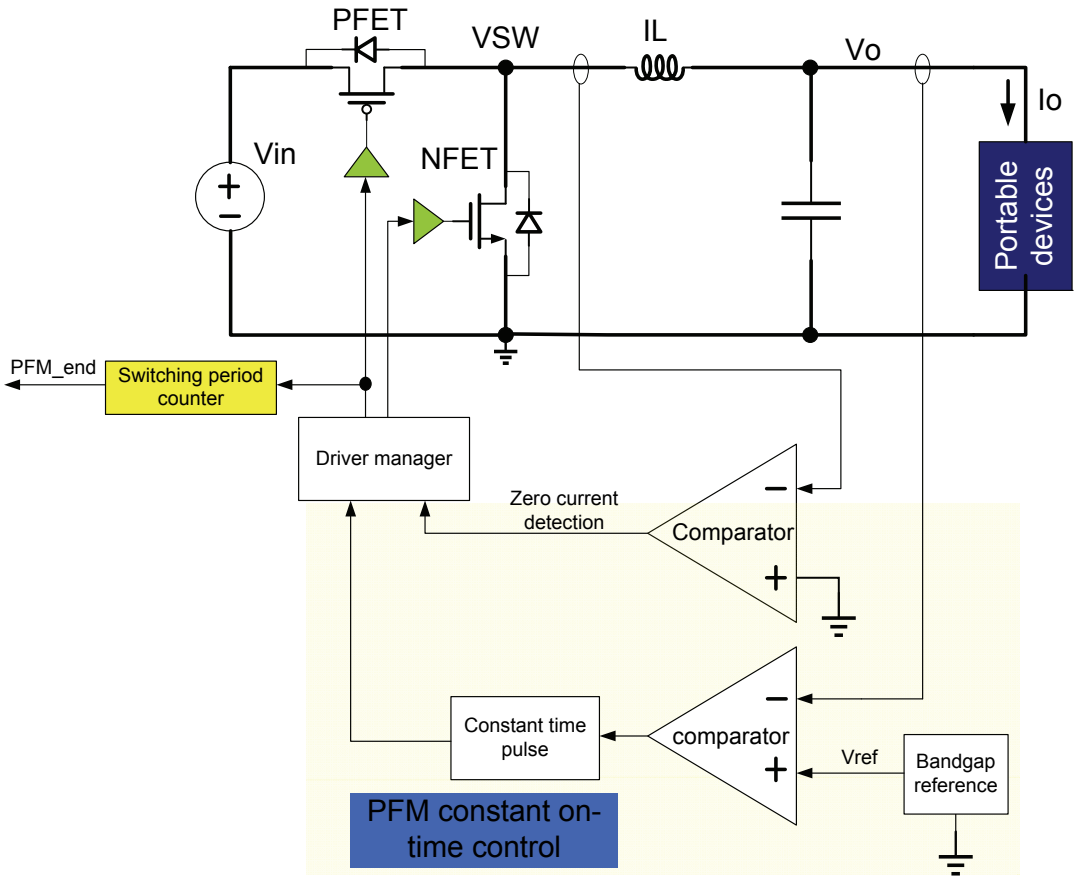

Figure 4-35. Functional blocks to implement the constant on-time PFM operation

The functional blocks to implement PFM operation are illustrated in Figure 4-35 and the silicon layout is shown in Figure 4-36. The ISBC output voltage is compared with the expected reference voltage. When the output voltage is smaller than the reference voltage, a pulse with constant on time will be generated which turns on the control power PMOS so that the power inductor is charged and the output voltage is able to be increased. For the ISBC application in this dissertation, the on-time is set to be 240us. From (4-22), the switching frequency of the ISBC is calculated to be 1.39MHz when the load current is equal to $I_o^{Critical}$=0.08A. After the constant on time pulse, the control power PMOS will be disabled and the inductor current is discharged via the synchronous power NMOS until the Vsw voltage drops below zero. When zero current is detected, the power NMOS

will be turned off to eliminate the retuning current loop for the benefit of power efficiency.

The typical waveforms of the ISBC in the PFM operation are illustrated in Figure 4-37.

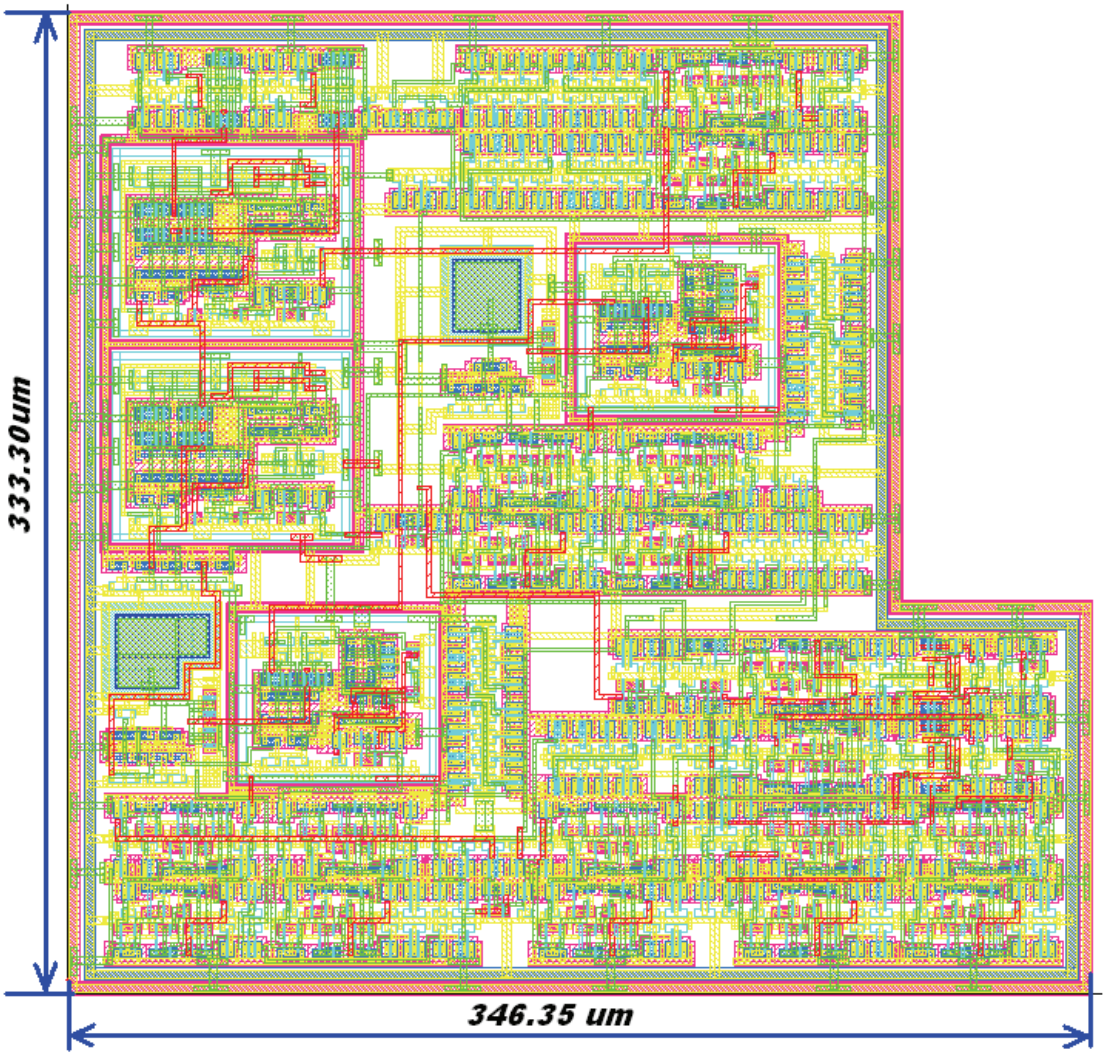

Figure 4-36. Silicon layout of the constant on-time PFM control

It is observed from Figure 4-37 that the inductor current shape significantly changes when the load current shifts between 100mA and 20mA. The reason is that the synchronous power FET will be disabled when the inductor current drops below zero.

Also, the switching frequency becomes load current dependent. From (4-22), the frequency is predicted to be 1.74MHz in 100mA and 350KHz in 20mA, which is illustrated by the simulation waveforms in Figure 4-37.

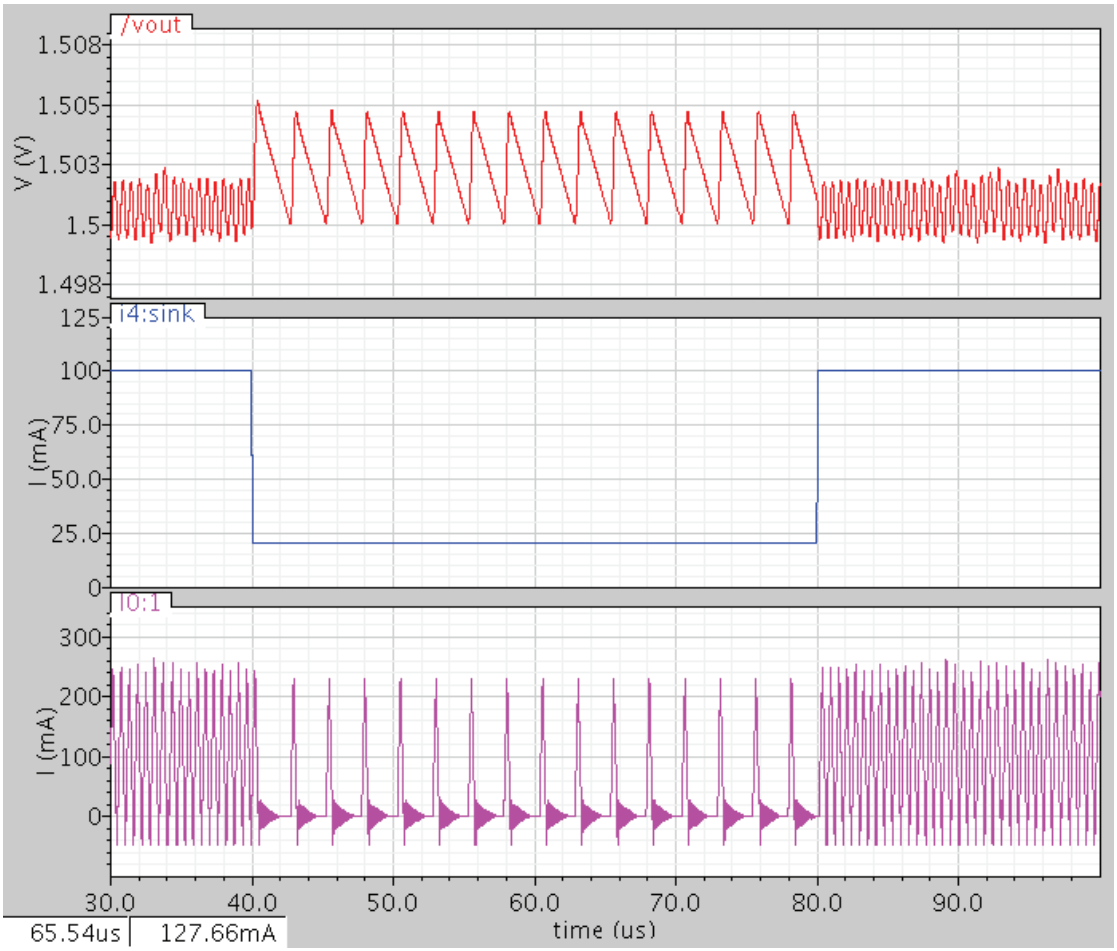

Figure 4-37. Typical waveforms in PFM operation

As both the inductor current shape and the switching frequency are load current dependent, the small signal transfer function and the relative linear regulator cannot be utilized as basic assumptions behind the two design methods are violated. The popular practice is to use output voltage ripple control (nonlinear control) such as the constant on-time control used in the dissertation. Another issue with PFM control is that the switching

frequency will lose stability for the heavy load condition and will present the limit cycle phenomenon [4-21].

From the viewpoint of the efficiency, the PFM operation is the best choice for the light load condition. If we ignore the quiescent current, the efficiency will be a constant value regardless of the load current [4-22, 4-26].

4.3.2.3 From PWM to PFM

When the load current decreases and the Vsw is higher than the two threshold values in the segment sensor, both $k1$ and $k0$ will be set to zero. As a result, the 3-bit state in the state machine will increase. At the same time, some group of the power FET subcells will be disabled. If the load current continuously decreases to approach $I_o^{Critical}$, only the group for the permanently active subcells will be active and the 3-bit state is equal to "110". If the load current continues to decrease, Vsw will stay above the band zone in Figure 4-14 as there is no more candidate groups of subcells to be disabled. When this situation occurs, the ISBC will remain the PWM mode except that the PFM_EN pin in Figure 4-19 has a high input signal to activate the PFM operation and change the 3-bit state from "110" to "111". State "111" indicates that the ISBC has entered into PFM mode operation. In the PFM mode, the output voltage will be regulated by the constant on-time control as illustrated in Figure 4-37. Also, the segment sensor will be disabled to save power.

The schematic of the state machine is shown in Figure 4-38 and its silicon layout is shown in Figure 4-39. The typical waveforms relative to the shift from the PWM to the PFM mode are illustrated in Figure 4-40.

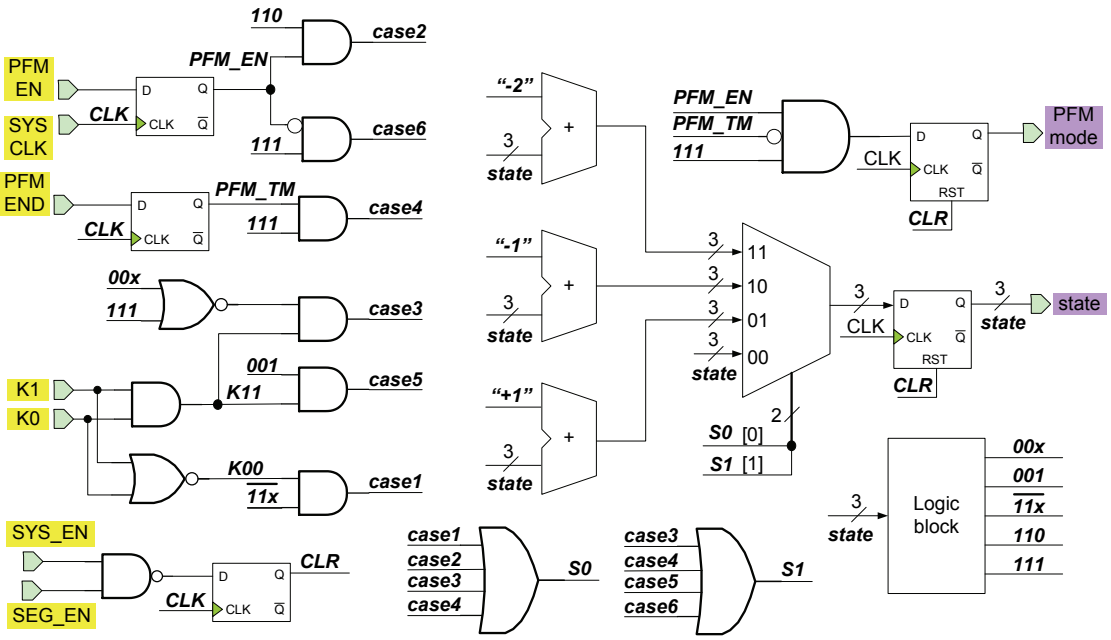

Figure 4-38. Schematic of the state machine

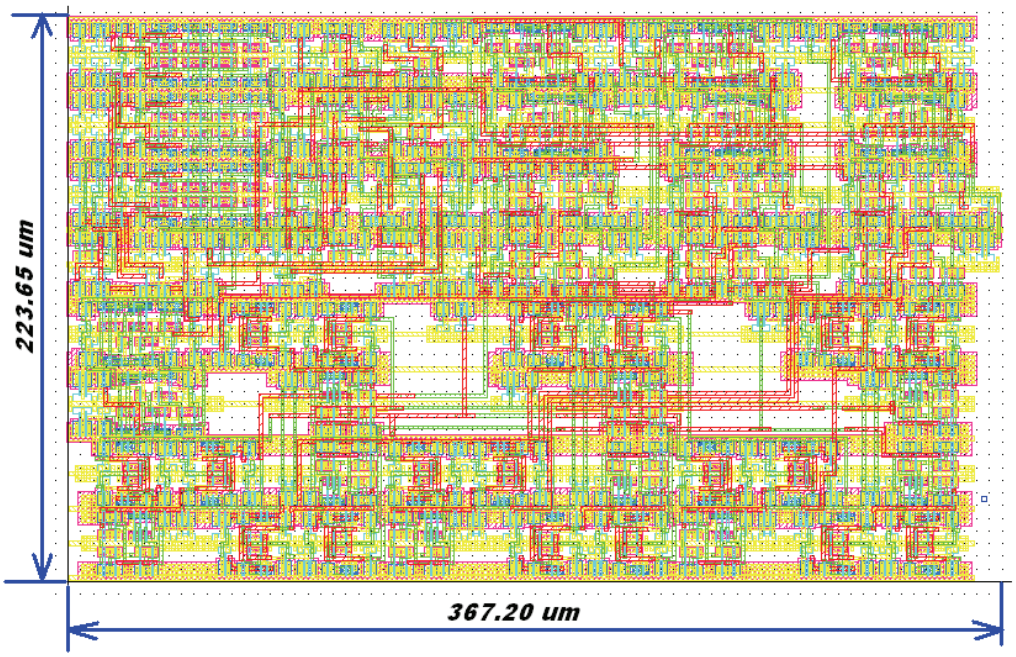

Figure 4-39 Silicon layout of the state machine.

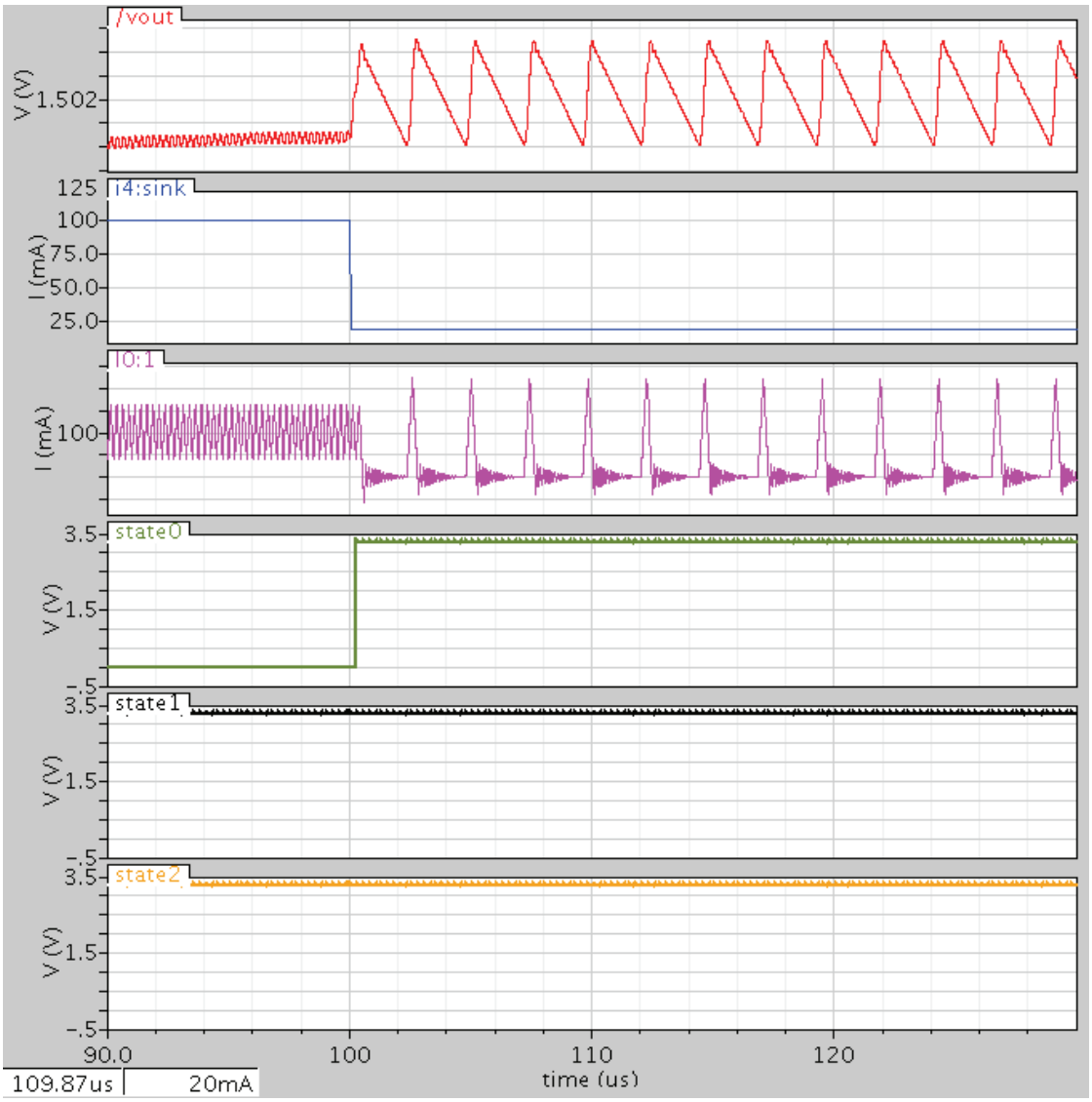

Figure 4-40. Typical waveforms from PWM to PFM operation

4.3.2.4 From PFM to PWM

When the ISBC works in PFM mode, a switching pulse counter will record the number of switching pulses in 4us time interval. In subsection 4.3.2.2, the switching frequency of the ISBC is calculated to be 1.39MHz when the load current is equal to $I_o^{Critical}$=0.08A. Thus, there should be 6 switching pulses to be detected in the 4us time interval when the ISBC load current is slightly larger than $I_o^{Critical}$.

When the counted number of switching pulse is larger than six, a PFM_end signal will be generated which indicates that the load current is larger than $I_o^{Critical}$ and the PFM mode should be terminated. The ISBC returns to PWM mode and the ISBC output voltage will begin to be regulated by the type-III PID compensator. Furthermore, following the state machine in Figure 4-13, the 3-bit state will be changed to "100" and four more power FET subcells are enabled.

The schematic of the switching pulse counter is illustrated in Figure 4-41 and the typical waveforms related to the shift from the PFM to the PWM mode are illustrated in Figure 4-42.

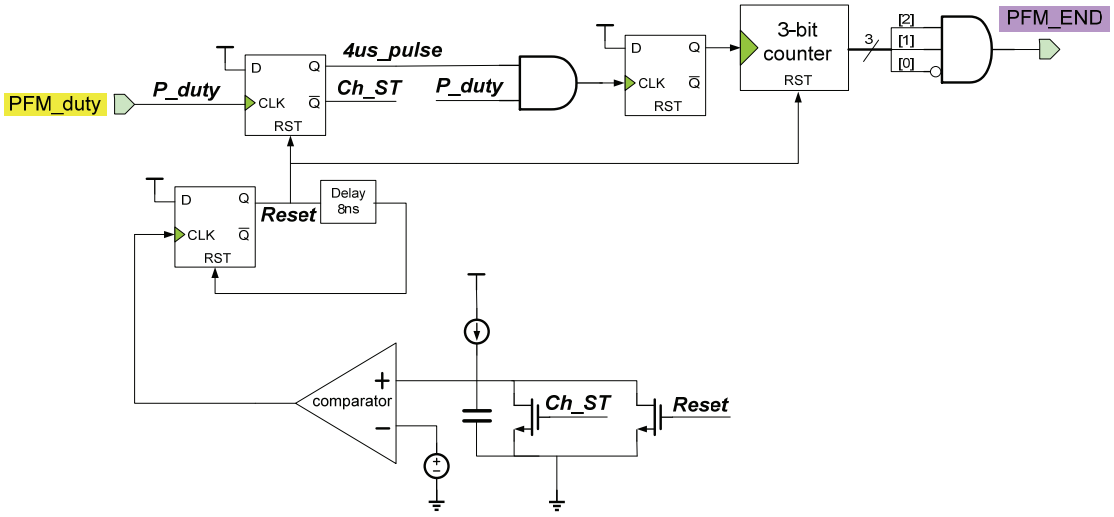

Figure 4-41. Schematic of the switching pulse counter

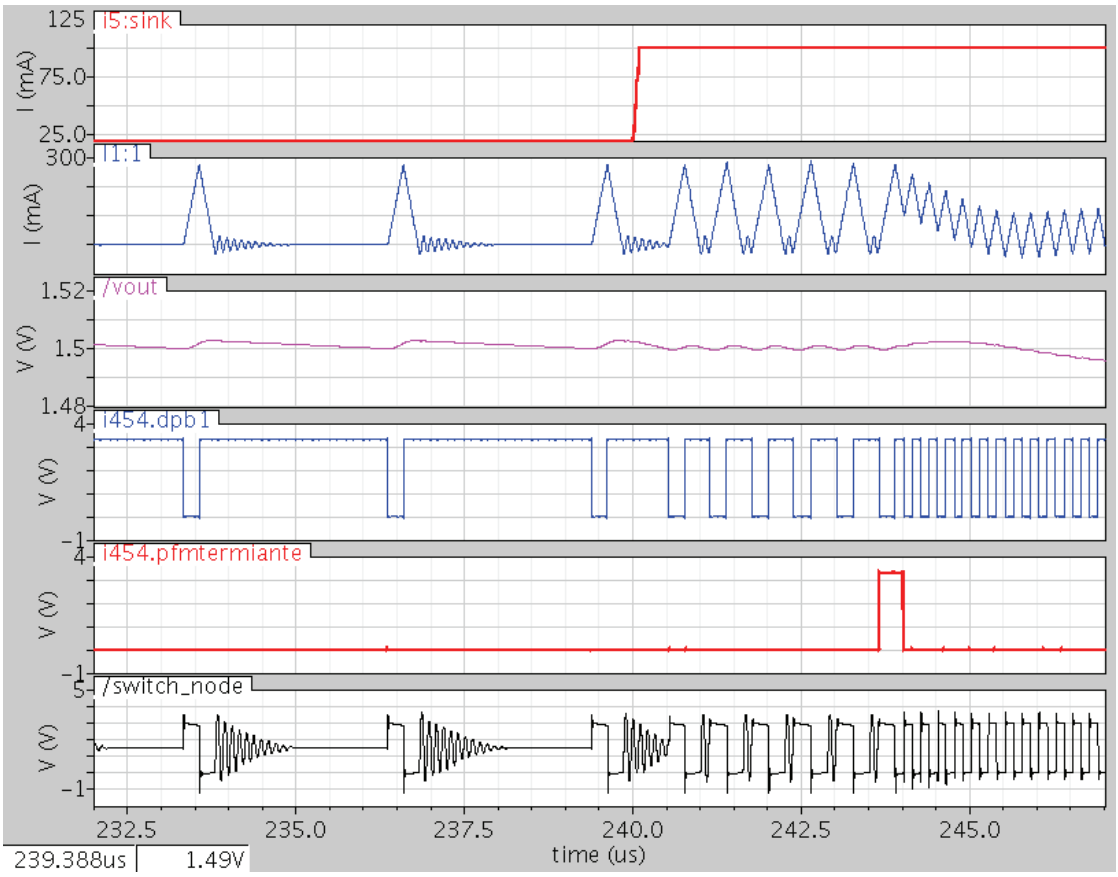

Figure 4-42. Typical waveforms from PFM to PWM operation

4.4 Segmentation/PFM verification

The whole ISBC chip's silicon layout is shown in the Figure 4-43.

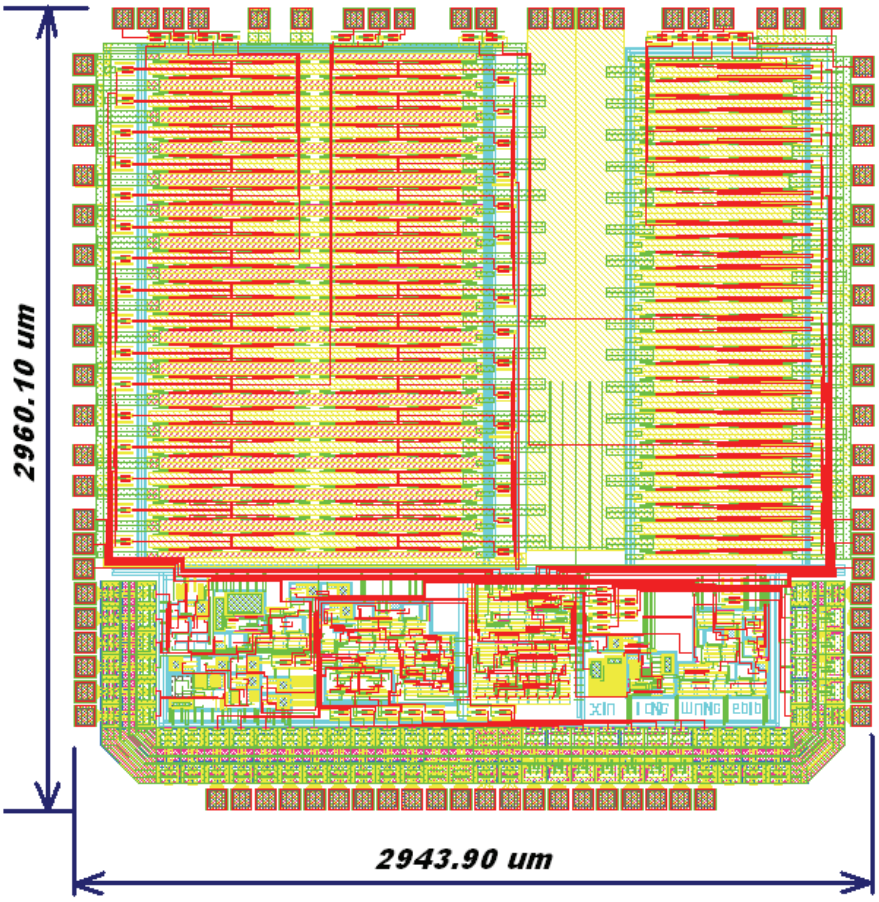

Figure 4-43. Silicon layout of the ISBC with the VswPS technology

Four simulations are carried out to verify the performance of the VswPS and the PFM/PWM mode shift silicon circuit introduced in subsection 4.3. In each simulation, the load current change is the same, but the ISBC is designed with one of four combinations of the PFM and segmentation technique. The four simulation results are compared at the end of the subsection.

The load current changes from 0.4A to 0.1A at 60us, from 0.1A to 0.02A at 100us and from 0.02A to 0.4A at 180us.

4.4.1 No segmentation & no PFM

Figure 4-44 illustrates the waveforms when neither segmentation nor PFM is selected.

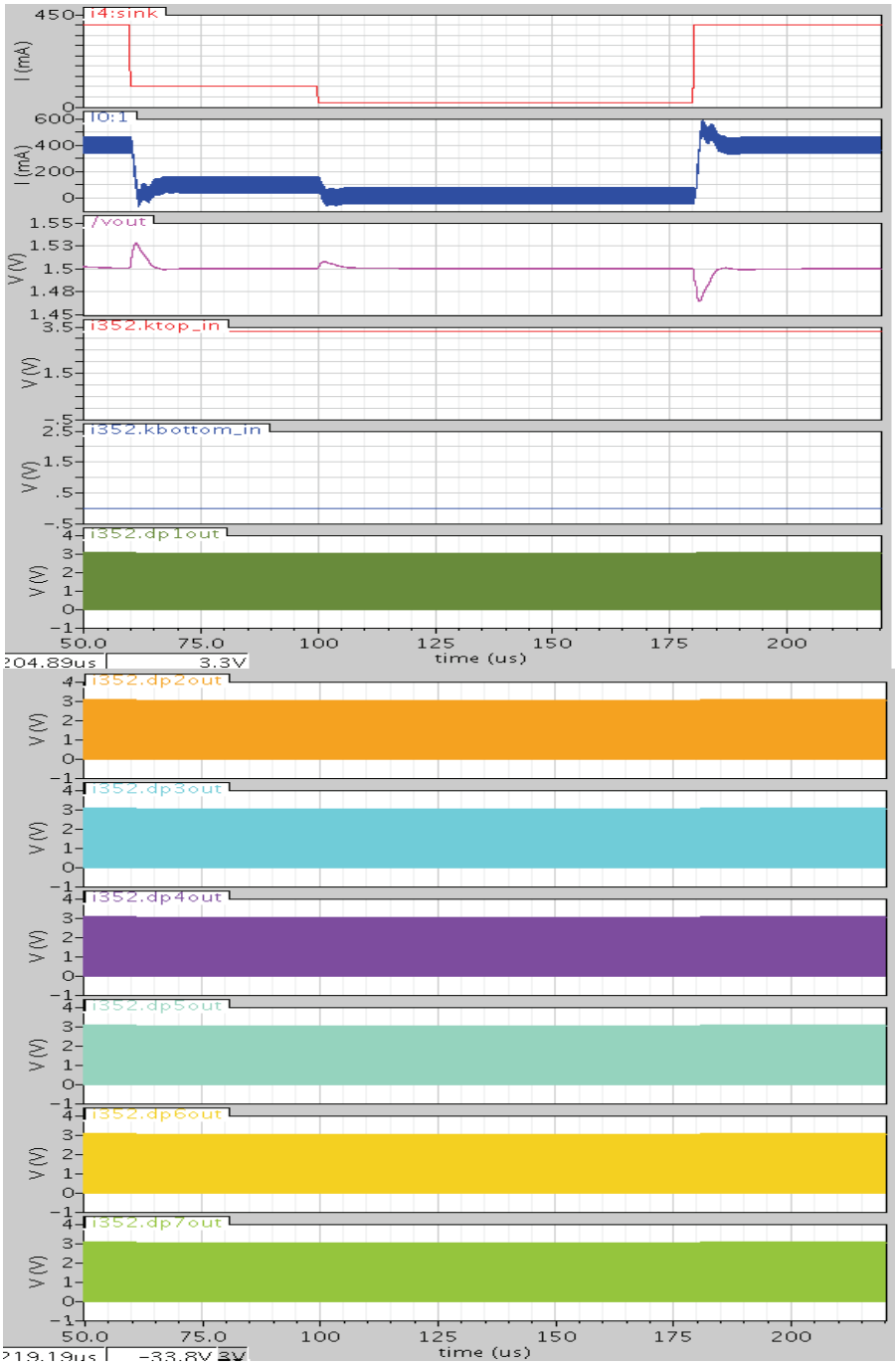

Figure 4-44. Waveforms when no segmentation and no PFM

4.4.2 Segmentation & no PFM

Figure 4-45 illustrates the waveforms when only segmentation is selected.

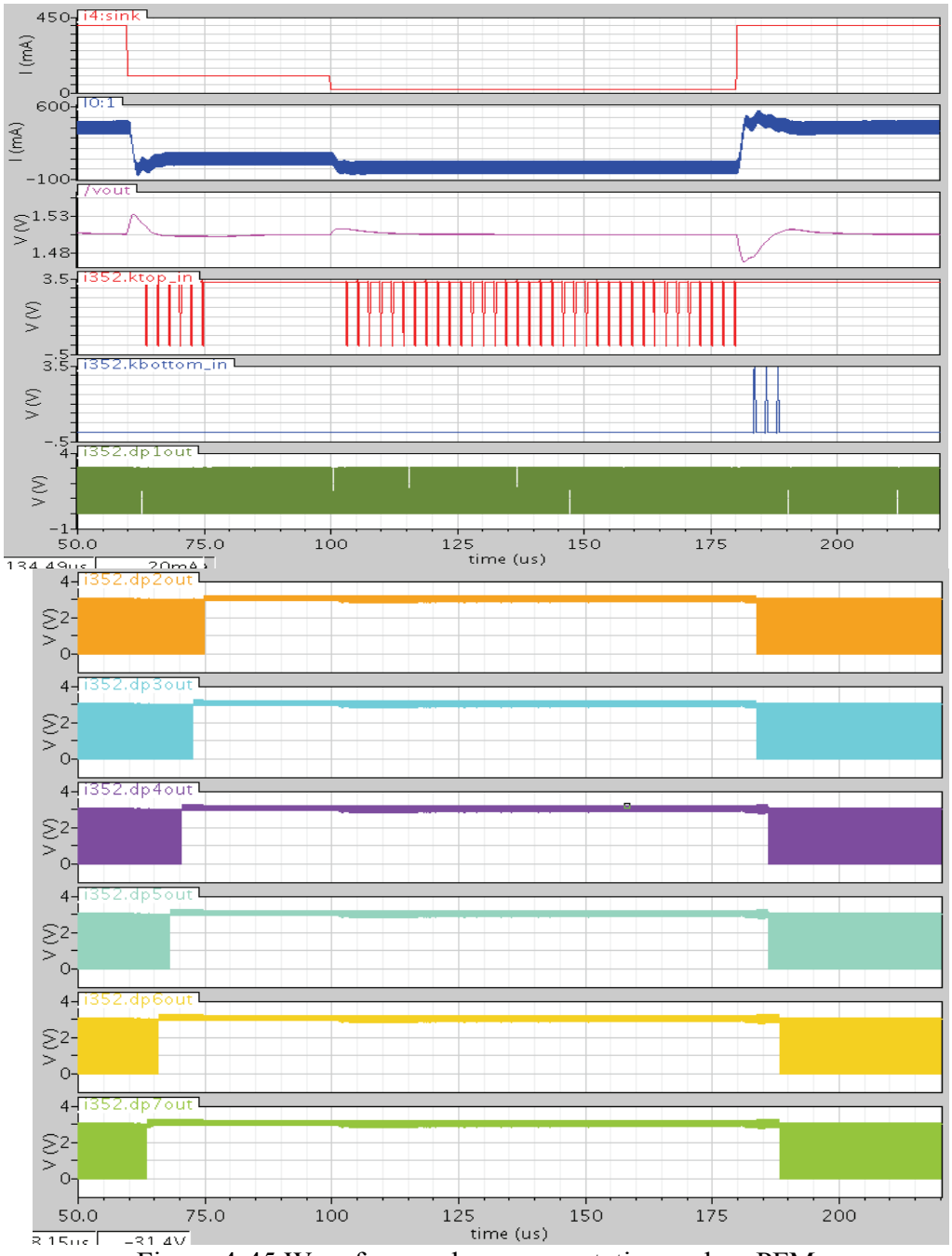

Figure 4-45 Waveforms when segmentation and no PFM

4.4.3 PFM & no segmentation

Figure 4-46 illustrates the waveforms when only PFM is selected.

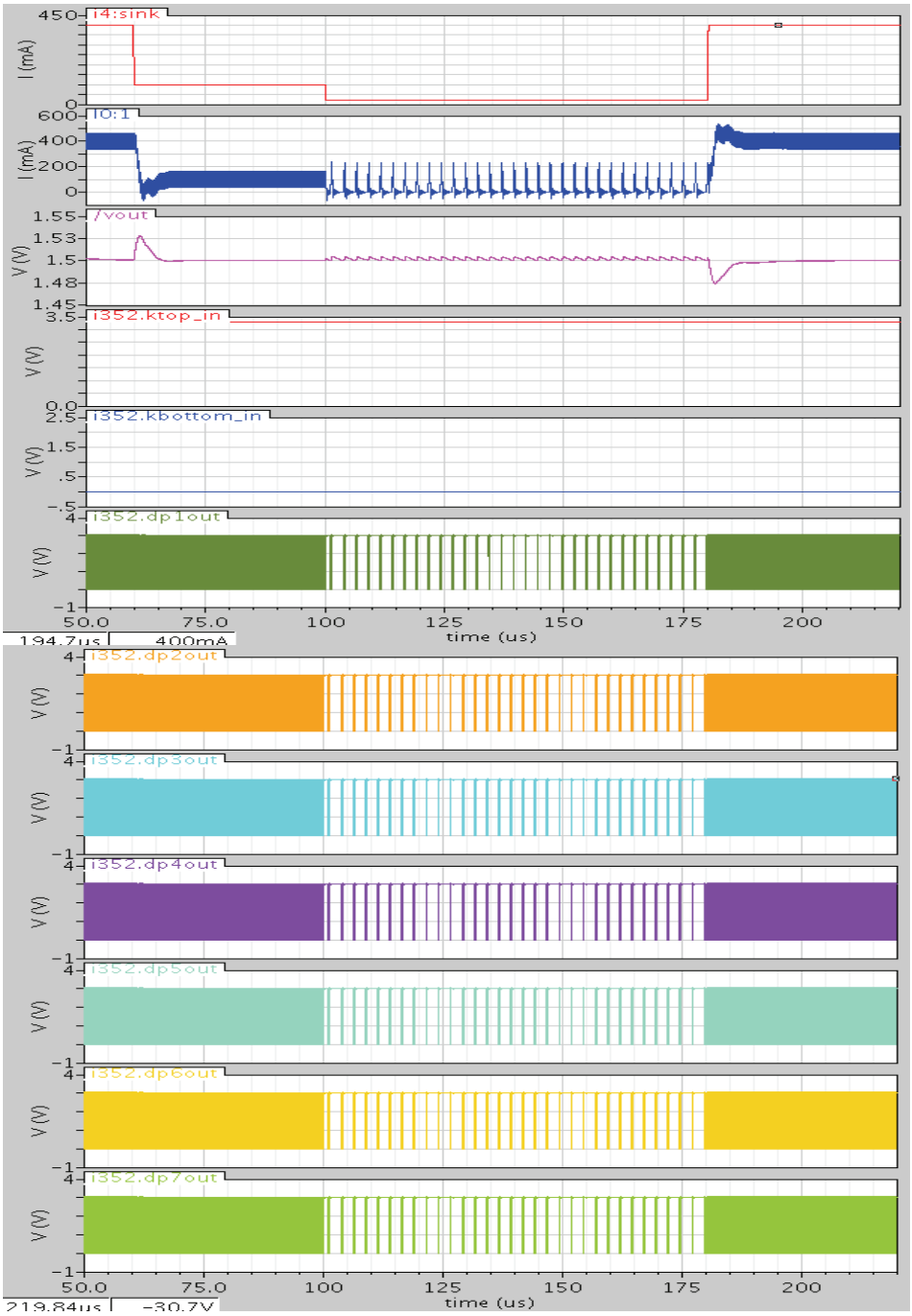

Figure 4-46. Waveforms when PFM and no segmentation

4.4.4 Segmentation & PFM

Figure 4-47 illustrates the waveforms when both segmentation and PFM are selected.

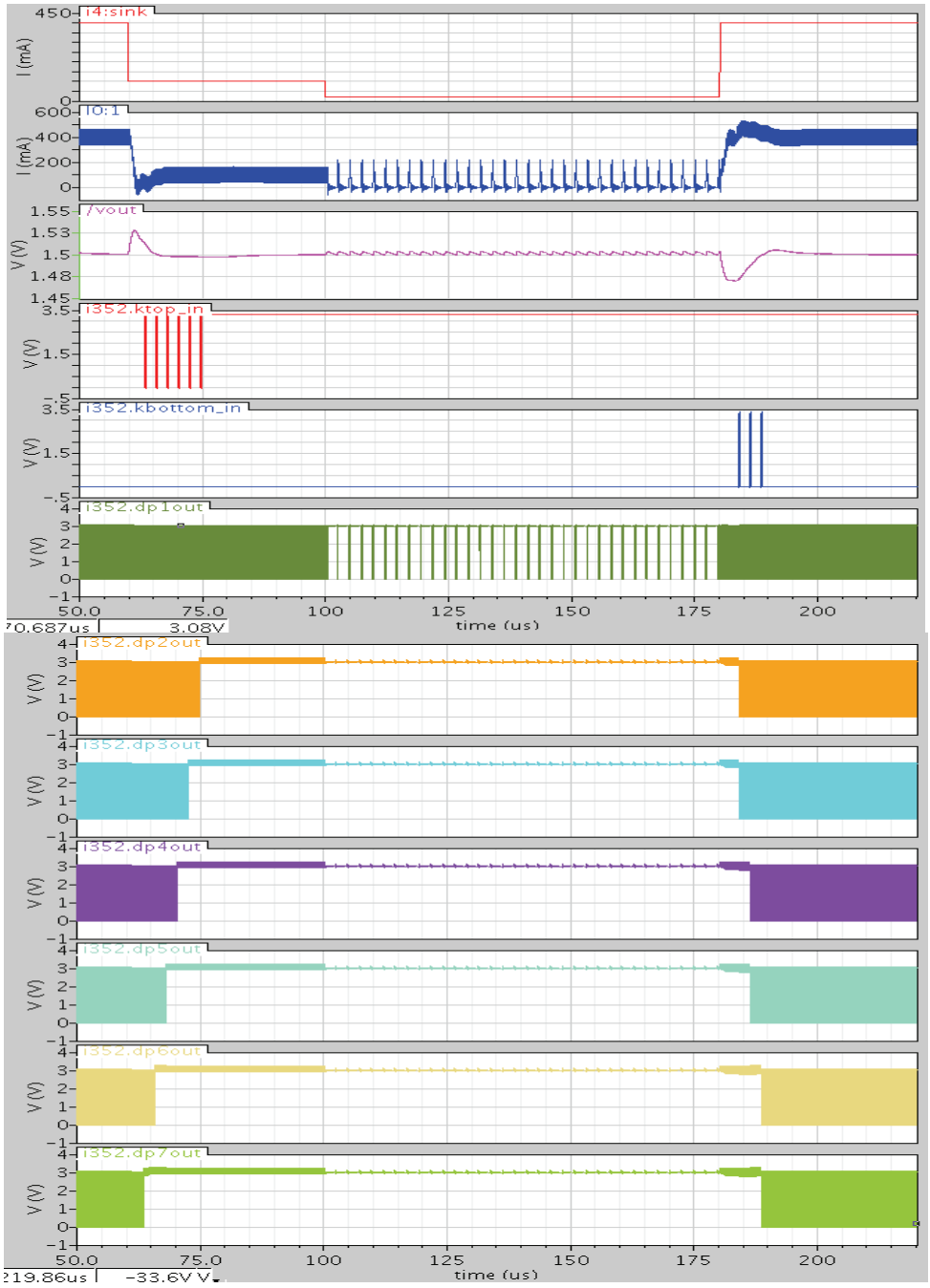

Figure 4-47. Waveforms when segmentation and PFM

4.4.5 Efficiency comparison

Figure 4-44, 4-45, 4-46 and 4-47 verify the performance of the ISBC chip with the VswPS and PFM techniques. The efficiency data for the four simulations are shown in Figure 4-48.

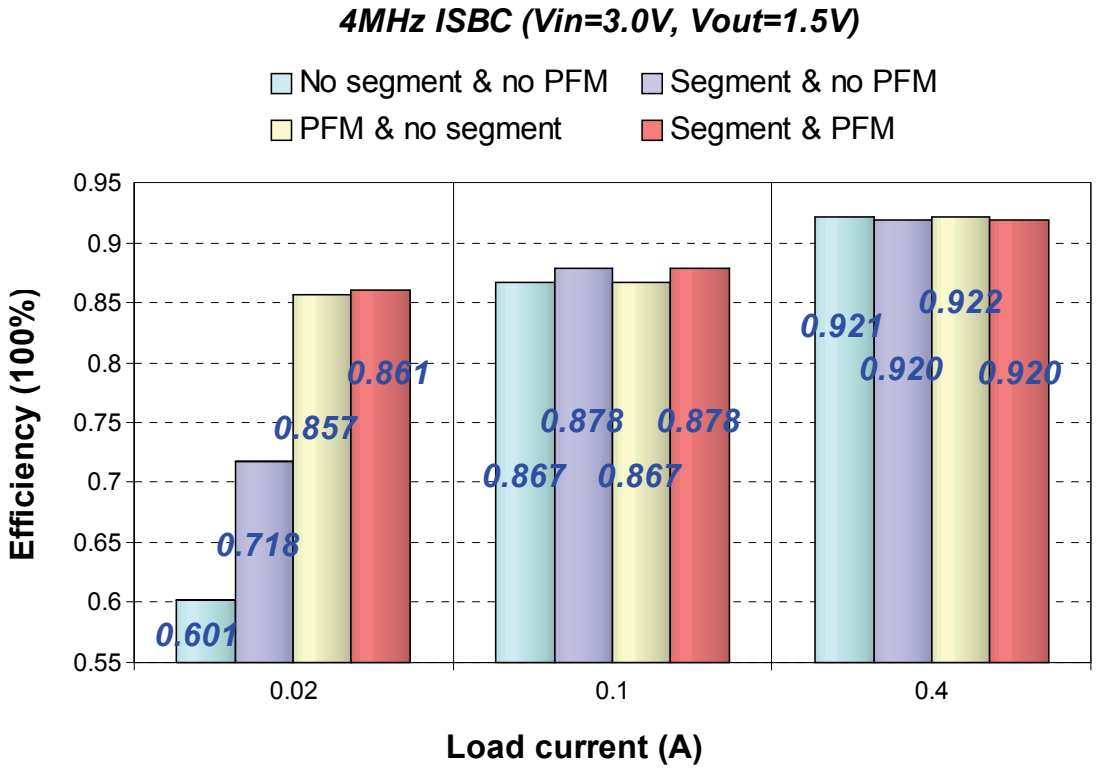

Figure 4-48. 4MHz load efficiency for different combinations of PFM & segmentation

Figure 4-48 shows that, among the four different combinations of the segmentation and PFM technique, the integrated one of both segmentation and PFM technique is able to achieve the flattest efficiency curves in a wide range of load current. Though the combination design's efficiency at the maximum load current 0.4A is 0.2% lower than the efficiency of the design with only PFM technique because of the quiescent current of circuit, the combination design's efficiency is 1.1% higher at 0.1A load current and 0.4% higher at 0.02A load current than the efficiency of the design with only PFM technique.

It is introduced in chapter 1 that the segment technique's contribution for efficiency will become more significant when the switching frequency increases. In order to verify the advantage of the segmentation technique in a high frequency ISBC, we repeat the aforementioned four simulations for the same ISBC except that the ISBC operates in 8MHz switching frequency. The efficiency data are shown in Figure 4-49.

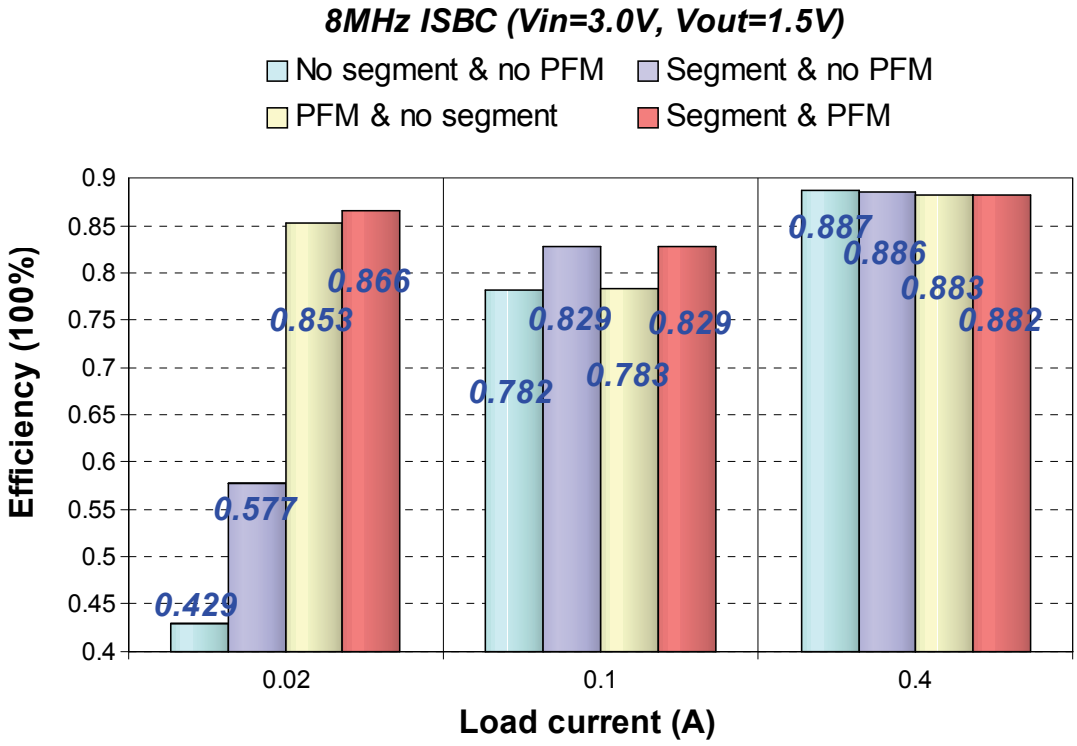

Figure 4-49. 8MHz load efficiency for different combinations of PFM & segmentation

Figure 4-49 shows that, among the four different combinations of the segmentation and PFM technique, the integrated one of both segment and PFM is able to achieve the flattest efficiency curves in a wide range of load current. Also, though the combination's efficiency at the maximum load current 0.4A is 0.1% lower than the efficiency of the design with only PFM technique because of the quiescent current of circuit, its efficiency is 4.6% higher at 0.1A load current and is 1.3% higher at 0.02A load current than the efficiency of the design with only PFM technique.

4.5 VswPS compensation verification

The VswPS segmentation technique is able to compensate the Rdson variation due to temperature. In this sunsection, the VswPS technique is compared with the CIS technique in respect to their efficiency variation because of temperature. For the convenient of comparison, the CIS for simulation is a modified version of the VswPS in which the active sub cells adjustment function is disabled and the number of active sub cells is regulated according to the value of load current. This process equalizes the circuit current consumption of CIS and VswPS so that the comparison on the measured efficiency exactly refers to the efficiency of the ISBC power stage. Because CIS implementation needs a sense-FET current sensor and an A/D converter, the efficiency of the ISBC with CIS will be worse than the reported value in this subsection.

The comparison is implemented in three steps:

1). In 0°C temperature environment, we use the VswPS technique to conclude the optimal number of active subcells when the load current is respectively 0.36A, 0.24A, 0.16A, 0.12A, 0.10A, and 0.08A. The waveforms of the ISBC are shown in Figure 4-50 and the optimal numbers of active sub cells are listed in Table 4-9.

Table 4-9. Optimal active sub cells determined in 0°C temperature environment

Load current	0.36A	0.24A	0.16A	0.12A	0.1A	0.08A
The optimal number of active subcells	24	14	10	8	8	8

2). Setting up two ISBC schematics. The first one is the ISBC with the VswPS technique; the second one is the ISBC whose active subcells are adjusted in according to the load currents on the basis of the information achieved in the first step;

3). In 200°C temperature environment, we run the simulation in the load conditions in step 1) and compare the number of active subcells and the efficiency obtained in the two ISBC schematics. The waveforms of the ISBC with the VswPS technique are shown in Figure 4-51 and Figure 4-52.

4.5.1 ISBC with VswPS in 0°C temperature

Figure 4-50 illustrates the waveforms when the ISBC works in 0°C temperature.

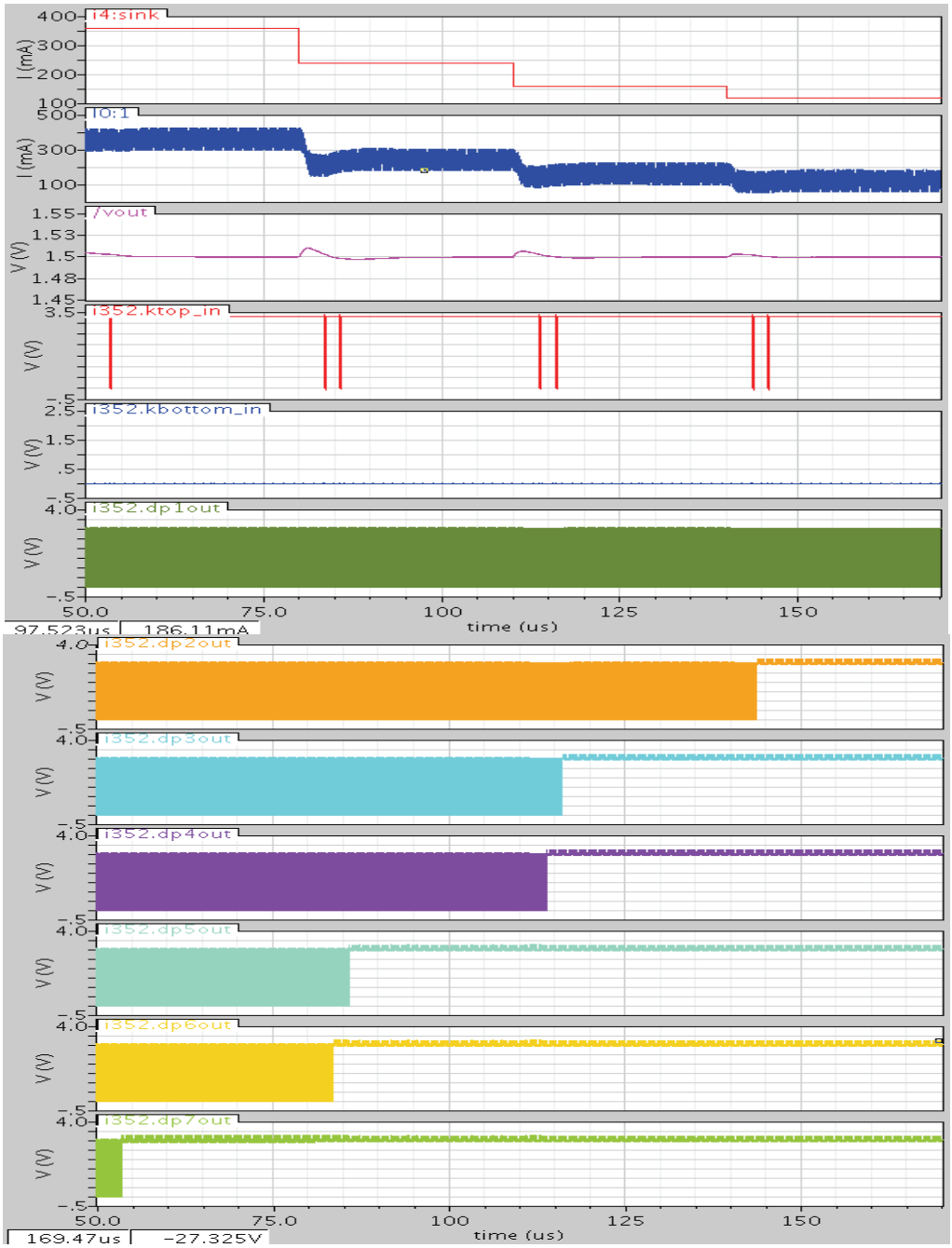

Figure 4-50. Waveforms when ISBC with VswPS works in 0°C temperature

4.5.2 ISBC with VswPS in 200°C temperature

Figure 4-51 illustrates the waveforms when the load current is 0.36A, 0.24A and 0.16A.

Figure 4-51. Part1 waveforms when ISBC with VswPS works in 200°C temperature

Figure 4-52 illustrates the waveforms when the load current is 0.12A, 0.1A and 0.08A.

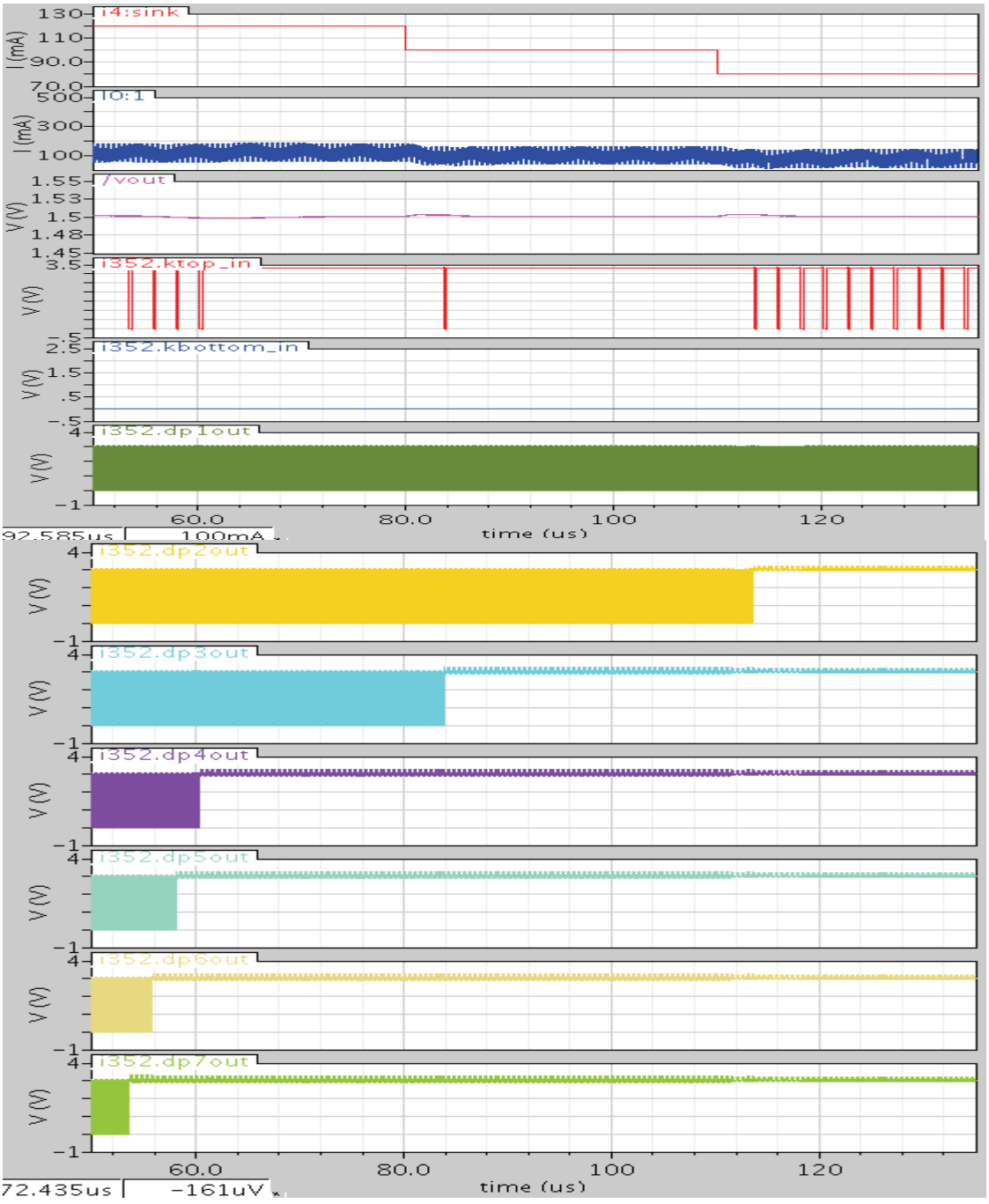

Figure 4-52. Part2 waveforms when ISBC with VswPS works in 200°C temperature

4.5.3 Comparison of CIS and VswPS

Figure 4-53 shows the number of active sub cells and Figure 4-54 shows the efficiency of the ISBC with CIS and VswPS. From Figure 4-53, we notice that VswPS is able to increase the number of active sub cells when the temperature changes. Also, thanks to the number's adjustment, VswPS obtains a 1% efficiency advantage in comparison with CIS. Figure 4-53 and Figure 4-54 verified the Rdson compensation ability of the VswPS technique and the necessity of the Rdson compensation.

It should be mentioned that when the load current is smaller than 0.12A, Figure 4-54 shows that CIS has a better efficiency than VswPS. This data is not true for the real system. The reason for the data is that we turned off segment sensor in VswPS to create a pseudo CIS here. Thus, in comparison with VswPS, the pseudo CIS has less quiescent power and might have a better efficiency when the load current is very small and the values of their losses are very close. On the basis of the consideration, we shade the region in Figure 4-54 which might not be true.

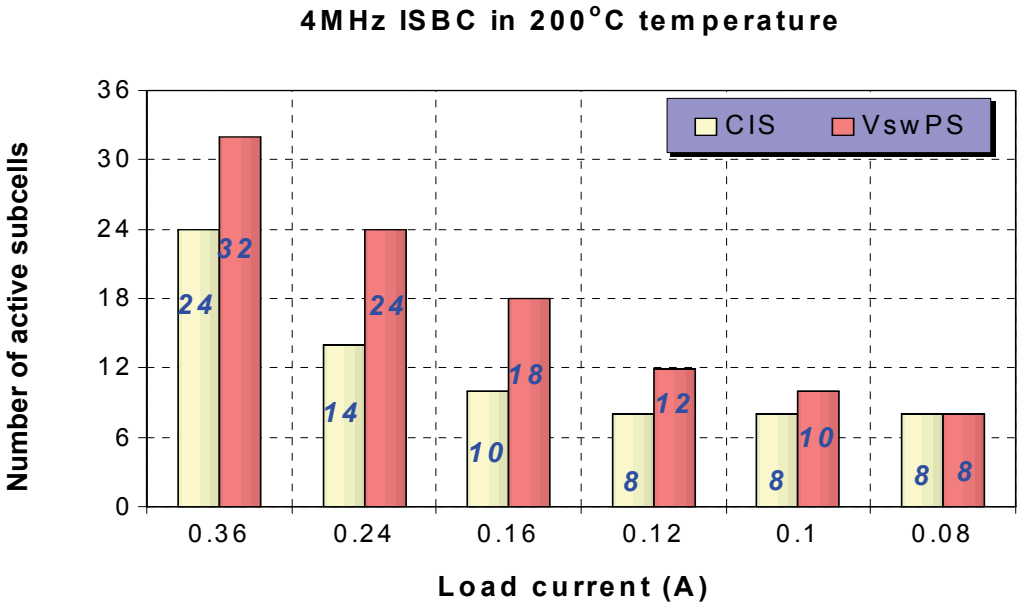

Figure 4-53. Number of active subcells in ISBCs with CIS and VswPS techniques

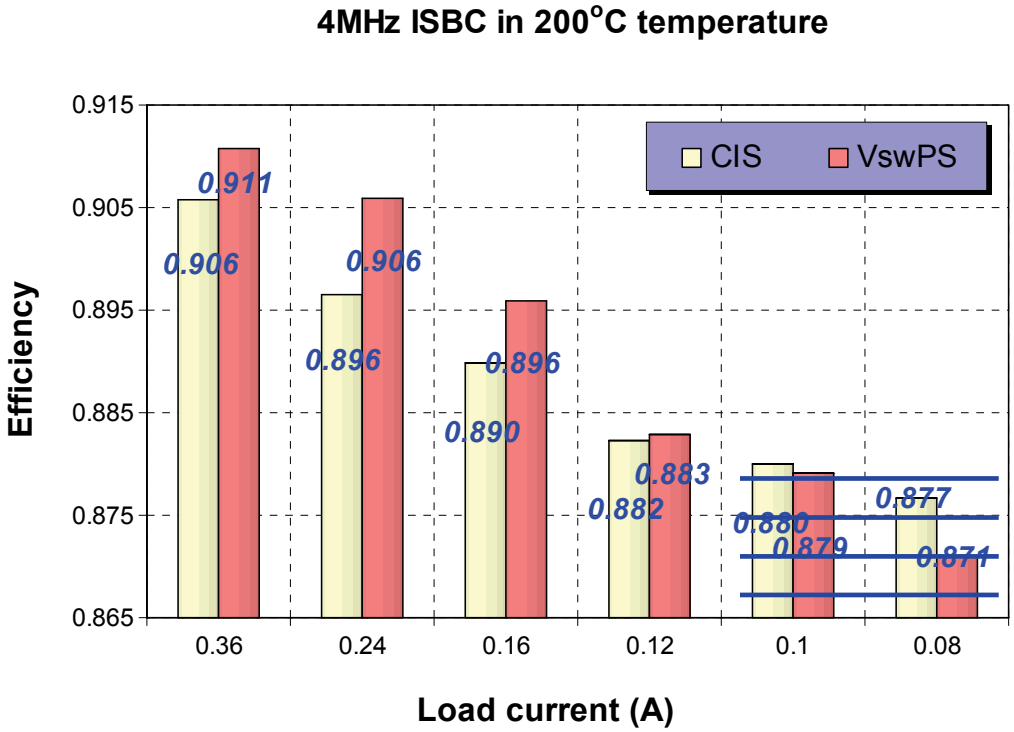

Figure 4-54. Efficiency of ISBCs with CIS and VswPS techniques

4.6 Conclusions and future work

This chapter utilizes the switching loss analysis method in chapter 2 to analyze the optimal number of the power FET subcells for a specified load current. The research shows that the optimal number is linearly proportional to the load current in certain range of load current. The research also shows that there is a saturation phenomenon when the load current is close to the value which is utilized for power FET width determination. The reason for the saturation phenomenon is that Cdb of the inactive sub cells does not appear in (4-1). Thus, if we use (4-7) to calculate the optimal number of active sub cells,

we do not include the effect of Cdb of the inactive sub cells and the calculated value will be a number larger than the largest number; in this dissertation, the largest number is 32.

The chapter utilizes the data reported by the MOSIS to observe that the variation of Rdson and FET capacitor due to manufacturing error is random in nature and the values are located in the ± 20% range. However, temperature will cause a significantly variation in rdson.

The chapter introduces a VswPS technique and its silicon implementation. The VswPS uses a state machine to manage the power FET sub cells and can automatically implement the segmentation of the ISBC when the load current changes. In contrast to the state-of-art CIF technique which implements automatic segmentation on the basis of load current sensing, the VswPS does not need a sense FET current sensor or an A/D converter. Therefore, the high switching frequency application of the automatic segmentation will no longer be limited by a sense FET current sensor and an A/D converter. Furthermore, the VswPS can automatically compensate the temperature effect on the Rdson which is not possible in the CIF.

The chapter also introduces a specific circuit to ensure the safe operation of the segmentation during the load current transients and another circuit to realize the smooth mode shift between the PFM and PWM.

There is still much work to do in the future on the VswPS technique.

a). Chip test

The ISBC chip with the VswPS technique had been submitted for fabrication in the MOSIS run V07G with the Fab-ID V07GAU. The bonding diagram of the chip is shown in Figure 4-55. The chip is expected at MOSIS on Jan. 31. 2011.

The chip is planned to be tested in the spring 2011.

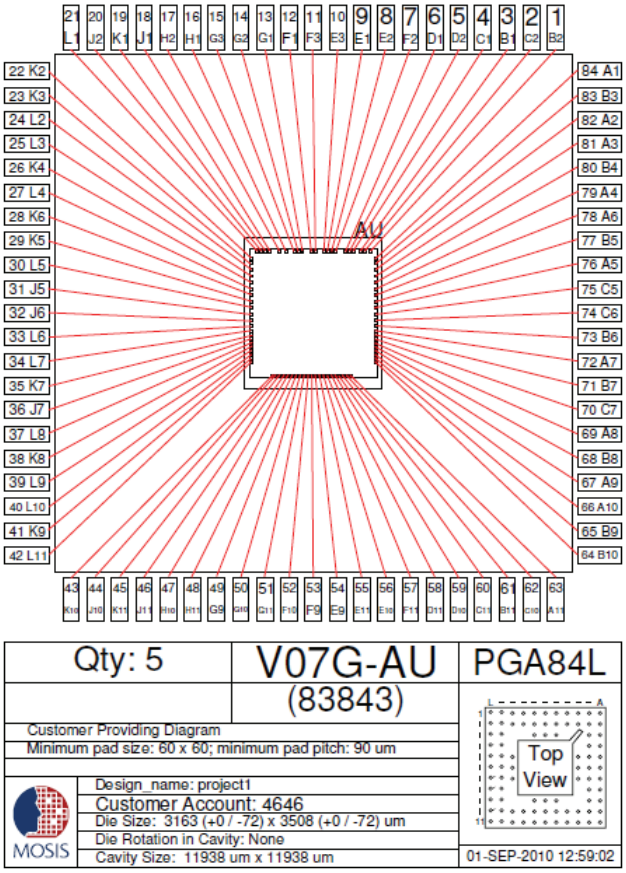

Figure 4-55. Bonding diagram of the ISBC chip to be fabricated

b). Varying duty cycle

(4-3) and (4-13) shows that the varying of the input and output voltage will change the duty cycle and thereby the optimal number of subcells in both the CIF and VswPS technique. It may be a good topic in future to investigate adaptively compensating for the change of input and output voltage by adjusting the threshold voltage level. Another topic is to individually manage the NMOS and PMOS power FET. In the dissertation it is assumed that the power FET subcell includes a pair of control power FET and synchronous power FET and the two FETs are simultaneously managed by the VswPS technique. In some applications addressing the wide range of input and input voltages, the assumption might need to be reconsidered.

c). Low power design in extremely light load

When the ISBC works in PFM, decreasing the quiescent current of circuit block is an important measure for improving efficiency. Some current-demanding blocks such as the opamp and bandgap need to work in a low power mode. The wake up sequence circuit is another area to be investigated in future.

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Chapter 5

Maximum switching frequency, choke effect and its solution in digital pulse width modulator

This chapter is devoted to the performance analysis and optimization of ***a standalone but very important component*** (digital pulse width modulator (DPWM)) in a ***digital*** DC-DC power converter.

In section 5.1, some background behind the DPWM is introduced. For example, I will discuss the characteristics of a digital DC-DC power converter as well as its potential advantages catering to portable electronic applications. Despite the aforementioned advantages, however, we cannot ignore a fact that a digital DC-DC power converter is not a general power supply solution for all portable applications. Some possible reasons are discussed in [5-2] to explain why the market and engineers hesitated in embracing this technology. It is recognized that many important technologies relative to a digital DC-DC power converter did not prove themselves better than their analog counterparts. Particular to portable devices applications, the maximum switching frequency implementation bottleneck, component power loss, and fast load regulation are potentially three major reasons.

The DPWM resolution's requirements and circuit implementation are introduced in section 5.2, in which the number of bits devoted to representing the duty cycle, the so-called "hardware resolution" and "soft resolution" are described. In section 5.3, I clarify the concept of the maximum switching frequency (MSF) in a digital DC-DC converter and discuss why the DPWM is the component of greatest concern to the MSF. In section 5.4, the Fan-out-4 (FO-4) is mentioned. In this chapter, FO-4 is suggested as a metric to analyze the MSF, so that the obtained analytical results can be directly applicable to all

semiconductor process technologies. Equations to calculate the MSF in four commonly used DPWM architectures are given in section 5.5. Furthermore, the choke effect is proposed to explain the MSF limit in a self-oscillation hybrid DPWM (SOH). Following this, a choke relaxed SOH (CR-SOH) is presented in section 5.6. In comparison with SOH, CR-SOH has a 100% improved MSF and significant power and silicon area savings. Section 5-7 introduces a circuit and chip implementation of the CR-SOH. Section 5-8 presents the test bench set up and test results.

5.1 Background

5.1.1 Digital DC-DC converter

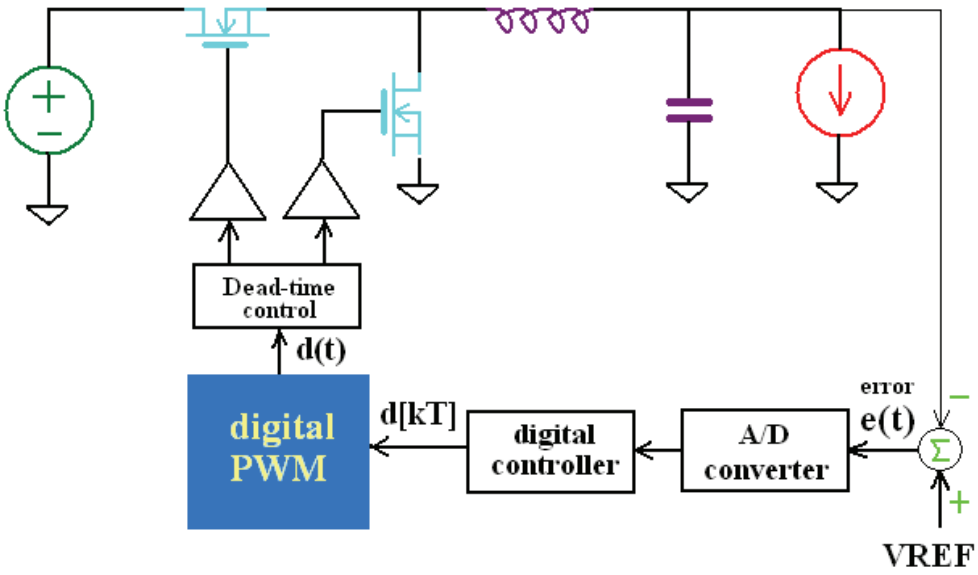


Figure 5-1. Digital DC-DC Synchronous Buck Converter

As illustrated in Figure 2-1, a digital DC-DC converter is distinguished from a conventional analog DC-DC converter with two particular function blocks, which are an analog-to-digital (A/D) converter and a DPWM. Furthermore, a digital controller

characterized by an arithmetic logic unit (ALU) replaces an analog controller characterized by passive components and operational amplifiers.

From 1990s, there have been thousands of academic papers focusing on the design and performance analysis of digital DC-DC converters, among which [5-24, 5-64, 5-7, 5-52, 5-34, 5-65, 5-68, 5-35, 5-8, 5-47, 5-44, 5-45, 5-4, 5-41, 5-70, 5-49, 5-56, 5-60, 5-42, 5-30, 5-75, 5-50, 5-22, 5-74, 5-6] are a representative subset. Every year the IEEE power electronics society will host two to three technical sections in two of its major academic conferences – applied power electronics conference (APEC) and Energy Conversion Congress and Exposition (ECCE) – to report the latest technical progress on digital DC-DC converters.

Two paragraphs in a white paper published in 2004 [5-46] are a good example to illustrate the expectations towards digital DC-DC power converters from many companies, engineers, and professors in power electronics field.

"Applying digital methods to the control of power converters, in particular board-mounted dc/dc converters, offers a rich set of possibilities from which to create new features, improved performance, and much greater product flexibility, and all at lower cost. Power converter operating characteristics dictated by a stored program, rather than the parameters of a set of discrete components, can mean tremendous cost and space savings as well as capacity for real time adaption of those characteristics, greater sophistication in control algorithms and the ability to generate, store and recall valuable real-time functional data"

"Digital signal processors, micro-controllers, flash memory and fast A/D converters will soon do to ***power conversion technology*** ***what they did to 35mm cameras****"*

5.1.2 Potential advantages

Some advantages of a digital DC-DC converter are briefly summarized:

1). Advanced Digital Control Algorithms

1.1) Programmable Proportional-Integral-Derivative (PID) control;

1.2) Application of Modern Control Theory, such as System Identification, Parameter Estimation, Self-Tuning Adaptive Control and Model Reference Adaptive Control;

1.3) Fuzzy Control and Intelligent Control;

2). Advanced Digital Power Management

2.1) Power Stage Segmentation;

2.2) Deadtime Optimization;

2.3) Complex Sequencing and Systematic Protection;

3). Enhanced Interface Communication, Monitoring and Diagnostic Capacities;

4). Digital Circuit Design Period, Integration, Cost and Protection

4.1) Much improved noise rejection ability in comparison with analog circuits;

4.2) Register-Transfer-Level (RTL) design significantly shortens design and test period and makes function verification much cheaper;

4.3) Simplify integration of different function blocks;

4.4) Easily extended to different Semiconductor Process;

4.5) Intelligent Property Protection;

5). System-on-chip integration with digital load

A converter can be transistor-level integrated with its digital device loads on a chip. This saves silicon area, decreases parasitic effects, improves transient performance, and drops the system cost.

6). No passive component and their related lifespan issues.

5.1.3 Issues for portable applications

Taking portable device applications into consideration, most of the above merits are very attractive. However, there are also many technical limitations of digital power converters which hinder their immediate application to portable devices. For example:

1). Maximum Switching Frequency (MSF)

When the digital resolution of a DPWM is a large value (for example, nine bits), today's DPWM architectures have difficulty supporting 10 MHz switching frequency operation if we adopt a 5V semiconductor process technology for the convenience of system integration. Though some digital signal processing technologies such as dithering and sigma-delta can provide soft resolution [5-44, 5-30], that is, an equivalent resolution in a sequence of cycles, the impacts of these technology on transient performance and controller stability is still questionable [5-44, 5-38]. The MSF of the hardware resolution DPWM had been reported in [5-63] and will be in investigated in detail in this chapter.

2). Component Power Loss

The DC-DC power converter output voltage's accuracy requirement necessitates the use of a high resolution A/D conversion, which is accompanied by significant power loss [5-39]. Furthermore, in order to prevent the limit cycle phenomena [5-44, 5-42], the resolution of the DPWM has to be higher than that of the A/D converter. Consequently the DPWM may present the highest power demand of any block in a digital DC/DC converter [5-8, 5-17, 5-54, 5-30].

The component's power loss is a significant issue for battery based portable applications.

3). Accurate and fast output voltage regulation

Digital control is prominent in modern industrial process applications where process parameters vary slowly (on a millisecond scale) [5-26]. Digital control also finds successful applications in high power conversion applications where the switching frequency is in the range from several 10 KHz to several 100 KHz [5-31]. However, it is difficult to apply digital control to integrated DC-DC converters with switching frequencies of more than 1 MHz and a tight output voltage regulation requirement. First, as digital control bandwidth depends on the clock, when the parameter variation speed and the component delay time are not much smaller than the scale of clock period, the stability of the digital control theory is questionable [5-14, 5-31], Second, in high frequency operation, a digital controller's robustness analysis is a challenge as the associated noise characteristics are difficult to predict and control; the problem is similar to a problems seen in flight control [5-18].

The chapter is devoted to the DPWM architecture analysis and improvement to alleviate the MSF limitation and to improve power dissipation, as well as to reduce silicon area.

5.2 DPWM resolution

5.2.1 Least resolution

The DPWM is regarded as having the highest power demand of any block in a digital DC/DC converter [5-8, 5-17, 5-54, 5-33, 5-30]. The DPWM is one factor in determining the MSF of an integrated high frequency digital DC-DC converter for portable

applications. The reason for this is that the resolution of the A/D converter needs to be high enough to ensure the output voltage's accuracy [5-39, 5-44, 5-41, 5-70, 5-56], and the resolution of the DPWM has to be higher than the resolution of the A/D converter to avoid a well known limit cycle phenomenon [5-44, 5-42]. Thus, for a digital DC-DC buck converter, the minimum resolution of the DPWM can be calculated with equation (5-1) [5-56].

$$n_{DPWM} > \log_2\left(\frac{V_g}{q_{A/D}}\right) \tag{5-1}$$

in which V_g is the maximum value of the input voltage, $q_{A/D}$ is the precision of the output voltage defined by the system specifications. For example, a typical high performance digital DC-DC buck converter is specified with $q_{A/D} = 10mV$ and $V_g = 5V$, so the minimum resolution of the DPWM is calculated to be $n_{DPWM} = 9 > 8.97$.

5.2.2 Hardware resolution

The DPWM resolution can be either the hardware resolution immediately available during each switching cycle or the soft resolution only available during a sequence of switching cycles. To make the resolution identical in each switching cycle, the hardware resolution should be generated either from the clock or from the components' delay accumulation.

5.2.2.1 Counter hardware resolution

A DPWM circuit using a counter to generate the hardware resolution was firstly reported in [5-64]; its operation principle is illustrated in Figure 5-2.

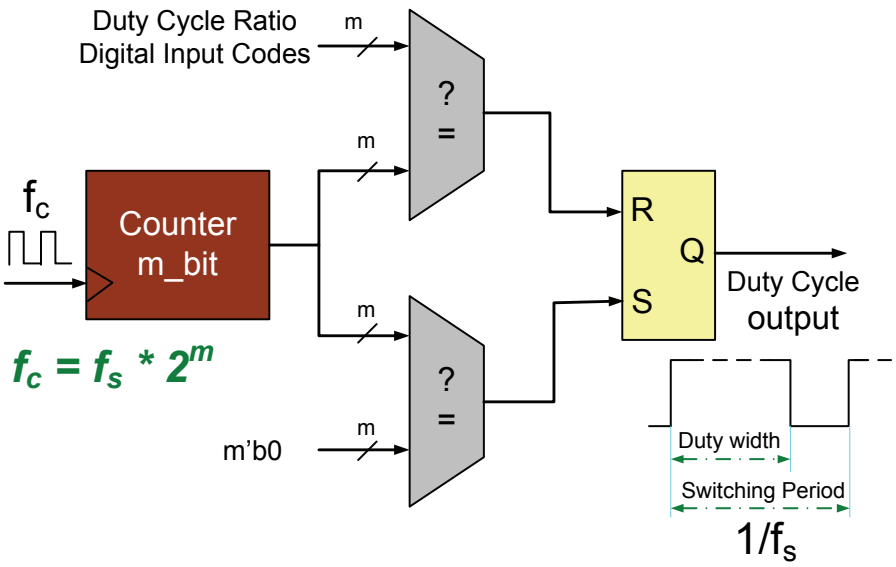


Figure 5-2. Counter based hardware resolution

If we use a clock with a frequency equal to f_C as the input of a m-bit binary counter, at the output of the counter we obtain m signals having different periods and the associated frequencies of the m periodic signals would differ in a relationship specified by the 2 power series, that is, distributed in a sequence of the form $\frac{f_C}{2^1}, \frac{f_C}{2^2}, \ldots, \frac{f_C}{2^m}$.

To ensure the moment of rising edge is constant, we use m'b0 as one input of a m-bit digital comparator and use the aforementioned m periodic signals as another input of the comparator. The output of the comparator is then connected to the "S" terminal of a latch. Thus, when all of the m periodic signals simultaneously are in the "0" state, the comparator will output "1," then the latch's output will be set to "1". As a result, a periodic constant rising edge of the duty cycle output is generated.

To generate the duty cycle, we introduce another m-bit comparator and repeat the above process except replacing the m-bit "0" with a m-bit digital input signal which represents the binary value of an expected duty cycle ratio. The output of the comparator is connected to the "R" terminal of the latch. When the number of the counted clock

periods is equal to the m-bit input digital signal, the output of the second comparator will be "1" and the duty cycle output signal is reset to "0" to get the desired duty cycle width.

Therefore, by counting clock periods, we can accomplish the data conversion from the duty cycle's m-bit digital signal to a continuous pulse signal with the desired pulse width. The finest resolution time will be the input clock's period and the output duty cycle's frequency will be $\frac{f_C}{2^m}$.

In summary, in order to generate a duty cycle signal with a m-bit resolution and a switching frequency of f_S, we have to input a clock with a frequency that can satisfy (5-2).

$$f_C = 2^m \cdot f_S \tag{5-2}$$

5.2.2.2 Delay_mux hardware resolution

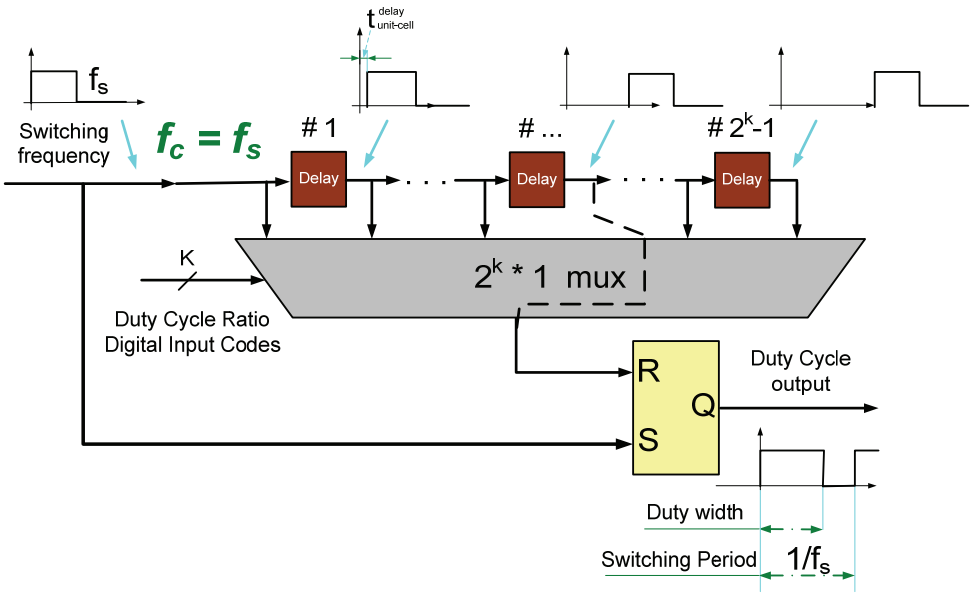


Figure 5-3. Delay_line based hardware resolution

A DPWM circuit using a delay cell and multiplexer (mux) to generate a hardware resolution was first reported in [5-7]; its principle of operation is illustrated in Figure 5-3.

If we use a clock with a frequency equal to f_C as the input of a delay chain consisting of p identical delay cells cascade connected, at the outputs of the delay cells we obtain a sequence of signals which have the same period but are delayed by different amounts of time. Furthermore, the values of the delay time will scale in integer times of a unit delay time $t_{unit-cell}^{delay}$, that is, the values will be distributed in a sequence of the form $t_{unit-cell}^{delay}$, $2 \cdot t_{unit-cell}^{delay}$, …, $p \cdot t_{unit-cell}^{delay}$. $t_{unit-cell}^{delay}$ is the propagation delay time of a unit delay cell.

To generate a periodic constant rising edge of the duty cycle, the input clock is connected to the "S" terminal of a latch. Thus, the latch's output will toggle to "1" when on the input clock's rising edge, so the periodic rising edge of the output duty cycle is formed. The output of each delay cell is individually connected to a terminal of a $p:1$ multiplexer which is controlled by a k-bit digital input signal representing a desired duty cycle ratio. The output of the multiplexer is connected to the "R" terminal of the latch. Thus, the duty cycle output signal will be reset to "0" by the output of the multiplexer.

Therefore, with the aid of the delay chain and the mux, we can accomplish the data conversion from the duty cycle's k-bit digital signals to a continuous pulse signal with the desired pulse width. The finest time resolution is the delay time $t_{unit-cell}^{delay}$ of a unit delay cell and the total delay time of the delay chain will be one $t_{unit-cell}^{delay}$ less than the input signal's period $1/f_C$.

In summary, in order to generate a duty cycle signal with a k-bit resolution and switching frequency f_S, we need to input a clock with a frequency that satisfies (5-3) and also need p identical delay cells satisfying both (5-4) and (5-5).

$$f_C = f_S \tag{5-3}$$

$$p = 2^K - 1 \tag{5-4}$$

$$\frac{1}{f_S} = (p+1) \times t_{unit-cell}^{delay} = 2^K \times t_{unit-cell}^{delay} \tag{5-5}$$

5.2.3 Soft resolution

The hardware resolution discussed in subsection 5.2.2 originates from a physical metric such as a clock period or a propagation delay. In contrast, the soft resolution depends on the averaged effect of a sequence of switching cycles, i.e., an equivalent resolution existing over multiple switching cycles. In another word, the soft resolution is one kind of application of the digital signal processing technique in the DPWM to improve the bit of resolution.

5.2.3.1 Dither soft resolution

A technique using a digital dither to improve the resolution of a DPWM was applied in [5-43, 5-44]. The principal of the digital dither is to randomly select a cycle or several cycles in a sequence of switching cycles and increase the pulse width of the cycle or cycles by a small pulse. The width of the pulse equals the finest time resolution determined by the hardware resolution.

A 1-bit dither and a 2-bit dither are shown in Figure 5-4 to illustrate the principle of the digital dither. Before the digital dither, the resolution of the duty cycle signal is generated from one of the hardware resolution methods discussed in subsection 5.2.2; its LSB is determined by either the clock period in Figure 5-2 or the delay time of a unit delay cell in Figure 5-3. As a result, we obtain the duty cycle sequence labeled as the “original duty cycle” in Figure 5-4.

When we apply a 1-bit digital dither with a dither number of "1", a pulse with width identical to the LSB of the hardware resolution will be added to the original duty cycle sequence at the (a) or (b) position (indicated in Figure 5-4) so that the consequent duty cycle width is on average 0.5 LSB larger than the original one in two switching periods. If the 1-bit dither number is "0", the original duty cycle sequence will be kept. Therefore, with the aid of 1-bit dither technique and taking two switching periods into consideration, we can get one equivalent resolution bit improvement over the hardware resolution.

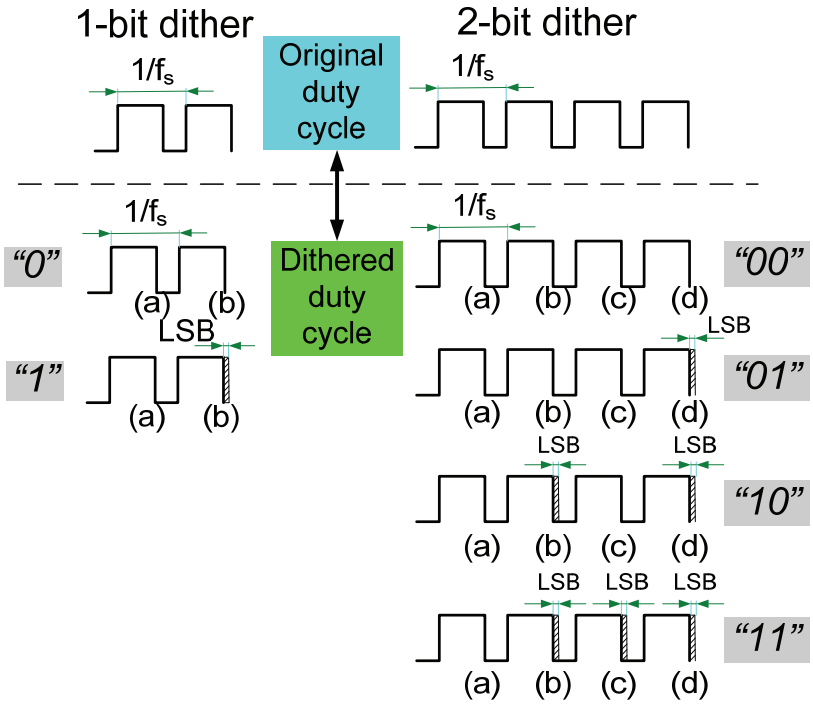


Figure 5-4. Principle of a 1-bit dither and a 2-bit dither

For the 2-bit dither case, the LSB pulse will be added at position (a), (b), (c) and/or (d) in Figure 5-4, dependent on the concrete 2-bit dither signal. Taking the 2-bit dither signal "11" as an example, one LSB pulse will be added at (b), (c) and (d) position. As a result, the equivalent duty cycle width in four switching periods is on average 0.75 LSB larger than the original duty cycle sequence. For the "11" dither signal, we an also put the LSB

pulse at (a), (c) and (d). The different locations of the LSB pulse will result in a performance difference in the output voltage ripple and the circuit implementation. Thus, with the aid of the 2-bit dithering and taking four switching periods into consideration, we can get a two-bit equivalent resolution improvement over the hardware resolution.

The steady state output voltage ripple from the digital dither had been analyzed in detail in [5-44], but the influence of the dither on the load transient and the control system stability is still not clear. For many control methods based on the output voltage ripple such as hysteresis control, in particular, the impact of the low frequency oscillation due to dither may become important As these kinds of control methods are usually preferred in the portable applications, the soft resolution from dither is not used.

5.2.3.2 Sigma-delta soft resolution

Sigma-Delta signal processing is another way to provide soft resolution. This method was applied in [5-56, 5-30, 5-27]. [Fig.7, 5-30] showed a 6-bit soft resolution sigma-delta DPWM and explained how the sigma-delta filter is integrated with a hardware resolution DPWM so as to create additional bits of equivalent soft resolution,

$d[n]$ in [Fig.7, 5-30] refers to a 10-bit digital input signal that represents a desired duty cycle ratio and is the input of a sigma-delta filter. $d_H[n]$ is the output of the sigma-delta filter and is a 4-bit digital signal being the input of a 4-bit hardware resolution DPWM. Thus, sigma-delta processing is utilized to alleviate the hardware resolution load from 10-bits to 4-bits. $e_a[n]$ and $d_H[n]$ are the 6-bit LSB and the 4-bit maximum significant bit (MSB) of the 10-bit $X[n]$, respectively. The function of the limiter is to eliminate the risk of a signal overflow.

More performance discussion on topics such as idle tones, DPWM linearity, output voltage noise and ripple amplitude in a sigma-delta DPWM were reported in [5-38]. It was also reported in [5-38] that a typical resolution improvements range from 3 to 4 bits for a 1st order modulator to around 6 to 7 bits for a 2nd or 3rd order modulator.

However, like the digital dithering technique, unfortunately, up to now there has been no theoretical analysis or experimental investigation on the impact of the sigma-delta modulator on the control system stability and the load transients of a high frequency DC-DC converter. Furthermore, we also do not know how much additional noise in the output voltage will be present due to the sigma-delta modulator that can deteriorate control methods based on the output voltage ripple such as hysteresis control. Therefore, generating soft resolution from the sigma-delta will not be considered in the chapter.

5.3 MSF in a digital DC-DC converter

An integrated digital DC-DC converter, as illustrated in Figure 5-1, is composed of a power stage and three on chip function blocks: the A/D converter, the digital controller, and the DPWM. The power stage further includes on chip power MOSFETs, the associated drive covering the dead time control and the bootstrap circuit if necessary, and the off-chip LC output filter. In order to supply a desired output voltage level to portable electronic devices, the power MOSFET driver will require a continuous pulse input, which toggles at the switching frequency and has a pulse width or duty cycle ratio tightly controlled by the three on chip function blocks. Thus, the power stages can be regarded as a plant to be regulated, and the three on chip function blocks can be regarded as a generalized regulator (GR).

5.3.1 Top level architectures

Five typical top-level IC architectures from different research groups [5-54, 5-1, 5-30, 5-45, 5-33, 5-5] are utilized to discuss the MSF in a digital DC-DC converter. From the five top-level architectures, we notice that the GR processes the signal in a unidirectional three-stage sequence. At the first stage, the A/D converter samples and

holds the power stage's output voltage and load current level, converts the sampled values to digital signals, and then outputs the signals to the digital controller; at the second stage, the digital controller's arithmetic and logic unit (ALU) applies arithmetic and logical operations on the input signals to implement a selected controller algorithm, and then outputs the digital signals of the generated duty cycle ratio; at the final stage, the DPWM converts the digital signal of the duty cycle ratio to a continuous pulse signal and outputs the signal to the driver of the power MOSFETs. Though the GR executes in a three-stage pipeline, in current designs, the GR is implemented as a one stage hardware architecture [5-32]. The samplers (the equivalent inputting Flop-Flop registers) are located in the A/D converter and the outputting Flip-Flop registers are located at the digital controller. On the basis of the five aforementioned architectures, a generalized top level architecture is given in Figure 5-5, with which we can investigate the timing and the MSF of a digital DC-DC converter.

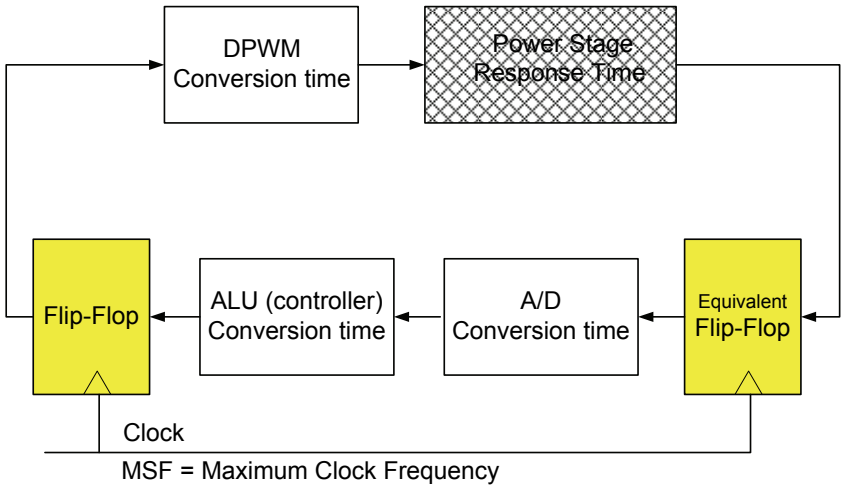


Figure 5-5. A generalized top level architecture for timing analysis

The conversation time in Figure 5-5 refers to the maximum delay throughout a function block from the input signal to the output signal for the worst case, and will be used to calculate the critical path delay for the system in Figure 5-5. The clock in Figure

5-5 not only sets the moment for the sampling in the A/D converter and the duty cycle renew in the digital controller, but also sets the switching frequency of the power stage. Thus, the maximum clock frequency is exactly the MSF we can approach in the system in Figure 5-5.

5.3.2 MSF limitations

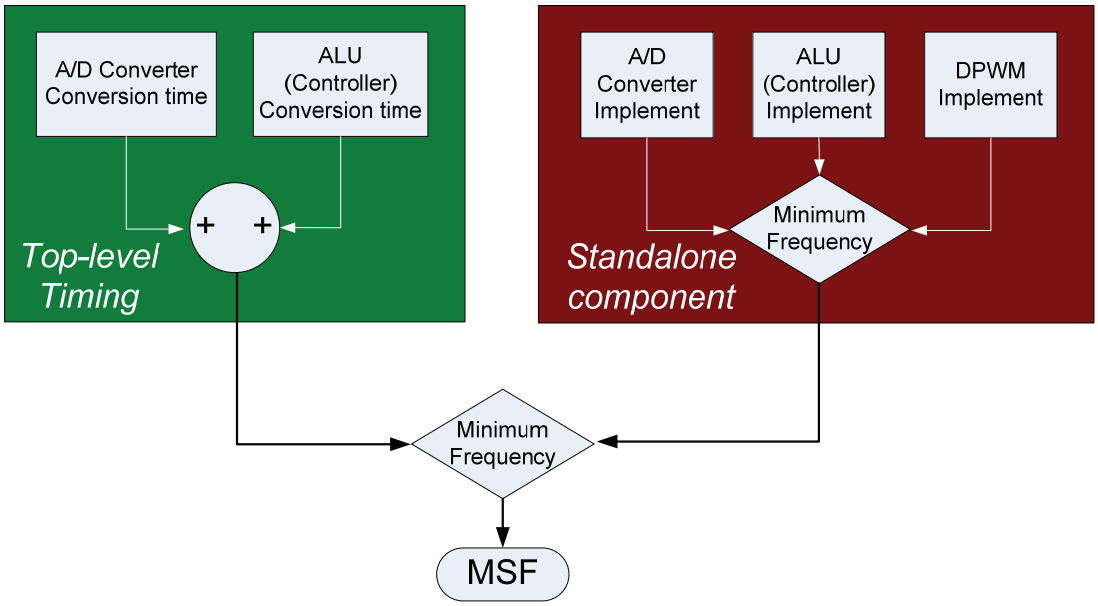


Figure 5-6. Flow chart to analyze the MSF in a digital DC-DC converter

The flow chart in Figure 5-6 is utilized to analyze the two factors that determine the MSF and the mechanisms by which they affect the MSF. The right hand factor refers to the limitation from the hardware implementation of a standalone component, i.e., the maximum signal output frequency that is able to be processed in a function block when it operates individually. The frequency is be determined by the critical delay path in the hardware architecture as well as the semiconductor process. The right part is looking for is the minimal value among three maximum output frequencies for the three function blocks in a digital DC-DC converter. The left part investigates the top level timing

constraint in the system in Figure 5-5, i.e., the maximum frequency ensuring a correct top-level logic function in the worst case. Therefore, the final MSF is chosen to be either the left frequency or the right frequency, whichever is less.

5.3.2.1 Top-level timing constraint

For the system in Figure 5-5, from viewpoint of the timing constraint, the minimum clock period should satisfy the equation (5-6) [5-15].

$$t_{clock} \geq t_{clock-Q-\max} + t_{\log ic-\max} + t_{set-up} + t_{skew} \tag{5-6}$$

where $t_{\log ic-\max}$ is the maximum logic delay given in (5-7).

$$t_{\log ic-\max} = t^{A/D}_{conversion\_time} + t^{ALU}_{conversion\_time} \tag{5-7}$$

where the conversation time refers to the maximum delay throughout a function block from the input signal to the output signal in the worst case.

Table 5-1. Delay metric in FO-4

Delay	inverter	1-adder	2-Nand	2-Mux	Flip-Flop $t_{clock-Q}$	Flip-Flop t_{set-up} , t_{hold}	Skew	Jitter
FO-4	***1***	***10***	***2***	***4***	***4***	***2***	***4***	***2***

Fanout-of-4 (FO-4), to be introduced in subsection 5.3, is a very handful tool to predict the gate delay [5-19]. We use the equation (5-8) [5-15] to evaluate the worst case value of the FO-4.

$$t^{worst-case}_{FO-4} \approx 600 \times 0.7 \times L_{drawn} \ (ps) \tag{5-8}$$

where L_{drawn} is the drawn gate length in the unit of μm.

Furthermore, for the AMI06 process we could derive a concrete value of $t_{FO-4}^{worst-case}$ in (5-9).

$$t_{FO-4\_AMI06}^{worst-case} = 252\,(ps) \tag{5-9}$$

The delay metric of some popular gates [5-15] is repeated in Table 5-1 for a conceptual estimation and analysis with the aid of (5-6) and (5-7).

Inputting (5-7) and the associated data in Table 5-1, we can rewrite (5-6) in (5-10).

$$t_{conversion\_time}^{A/D} + t_{conversion\_time}^{ALU} \le t_{clock} - 10 \times t_{FO-4}^{worst-case} \tag{5-10}$$

If we assume the AMI06 process and a 10MHz clock, to satisfy the timing constraint in (5-10), the conversion time of the A/D and the ALU of needs to be smaller than a scaled FO-4 value in (5-11) or 97.48 nanoseconds.

$$t_{conversion\_time}^{A/D} + t_{conversion\_time}^{ALU} \le 386 \times t_{FO-4}^{worst-case} \tag{5-11}$$

As $386 \times t_{FO-4}^{worst-case}$ provides a large headroom for the conversion time, Equation (5-11) implies that the timing constraint will not be a problem for a normal high performance digital DC-DC converter as verified in the example implementations [5-8, 5-56, 5-30], where the A/D converter is with a practical resolution less than 9-bit and is popularly implemented in a windowed flash architecture as that illustrated in Figure 5-13. The ALU is a look-up-table (LUT) PID compensator illustrated in Figure 5-14 which computations are executed with approximately 12 -15 bit precision.

5.3.2.2 Hardware implementation limitation

In the AMI06 process, a 10 MHz clock period is equivalent to $396 \times t_{FO-4}^{worst-case}$ with the aid of (5-9). Thus, from the viewpoint of a windowed flash A/D converter, 10 MHz is not a challenge for the standalone hardware implementation of the A/D converter. Similarly, we will not meet a challenge to implement a 10 MHz 15-bit look-up table type ALU [5-67] in AMI06 process. The above inference is verified by the example implementations [5-56, 5-30, 5-33]. However, 10 MHz is an aggressive value for a 9-bit hardware resolution DPWM implementation. To avoid the limitation, [5-56] weakened the hardware resolution requirement to 7 bits via decreasing the input voltage range and used 3-bit soft resolution. [5-30] only selected 4-bit hardware resolution and [5-33] decreased the hardware resolution specification to 6-bit when approaching 15MHz. In subsection 5.5, we will investigate why it is difficult to implement a 10MHz 9-bit hardware resolution DPWM.

5.4 Fan-out-of 4

The speed of a logic gate's dependence on technology can be found with Fan-out-of 4 (FO-4) [5-19]. FO-4 is the delay through an inverter that has to provide the output drive for other four identical inverters. As the value of FO-4 is fairly stable through process corners, temperature, voltage variations, and, most importantly, its value is linearly proportional to process technology with regards to gate length, FO-4 is recognized as a very helpful tool for digital architects to predict the delays of complicated logic gates for a specified semiconductor process.

An equation was provided by Dr. Horowitz [5-19], where the feature size equals $0.36 \times L_{drawn}$ and L_{drawn} refers to the drawn gate length of a specified semiconductor process technology. In the chapter, we will use another equation (5-8) provided by Dr. Franzon to evaluate the worst case FO-4 value [5-15].

5.5 MSF & DPWM architecture

In subsection 5.2.2, we present the principle of two kinds of hardware resolution in the DPWM. In subsection 5.2.3, we introduce the soft resolution and why we do not prefer it in portable applications. Furthermore, in subsection 5.3, we mention that the MSF of a digital DC-DC converter will be determined by the DPWM, if 10 MHz is the maximum output frequency of a 9-bit hard resolution DPWM with the AMI06 process. In this subsection, we will systematically investigate the maximum output frequencies in various DPWM architectures and the results will be scaled by FO-4 so that they can be directly applicable to all semiconductor processes. We will also comprehensively discuss other performance issues of the DPWM such as the choke effect in a hybrid DPWM, frequency control, the relative matching error, the power dissipation, and the silicon area.

5.5.1 Counter DPWM

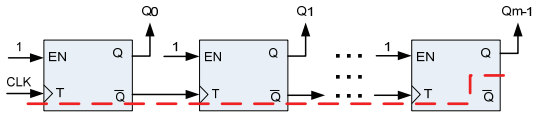
Counter DPWM is one of the first generation DPWM architectures [5-64]; its resolution completely comes from the counter type hardware resolution introduced in subsection 5.2.2.1. Counter DPWM has advantages such as a simple design, a minimized silicon area, a well controlled frequency, and a good linearity. However, Counter DPWM is the most power hungry architecture and its MSF is extremely low, which makes it only applicable for the high power applications where switching frequency is in the range 10 KHz to 100 KHz, or other applications typical of a low resolution requirement.

Equation (5-2) concludes that the input clock frequency should be 2^m times larger than the output frequency in a m-bit DPWM. Thus, if we assume a 9-bit Counter DPWM with 10MHz output frequency, the input clock frequency should be $2^9 \times 10MHz = 5.12GHz$. This is the reason why members of the power supply field have stressed Counter DPWM's power consumption, as it is almost linearly proportional to frequency.

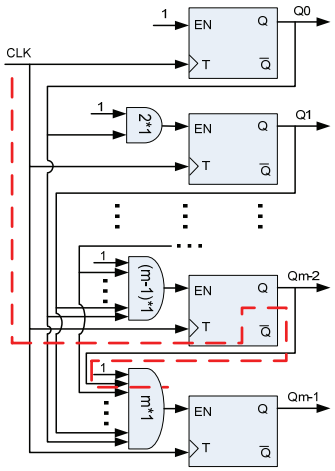
Another drawback of Counter DPWM is its extremely low maximum output frequency. To determine the maximum output frequency in Counter DPWM, we need to investigate the maximum clock frequency that the counter can sustain in a semiconductor process, i.e., the critical path delay in the counter, and if it is possible to implement a counter having a 5.12 GHz input clock in AMI06 process?

5.5.1.1 Maximum clock frequency

Let us compare the critical path in two different implementations of a m-bit binary counter illustrated in Figure 5-7. The left part (a) is a ripple carry counter while the right part (b) is a synchronous counter with parallel enables [5-61]. In Figure 5-7, enable signals are simplified with "1". CLK denotes clock. Q0, Q1, …, Qm-1 denote the outputs of the counter. The critical path is highlighted with a dashed line.



(a) m-bit ripple counter



(b) m-bit synchronous counter

Figure 5-7. Critical path in two m-bit binary counters with different implementation

The maximum counter clock frequency in the ripple carry and the synchronous counter could be calculated respectively in (5-12) and (5-13).

$$f_{clock\_\max}^{ripple} = \frac{1}{t_{clock\_\max}^{ripple}} = \frac{1}{m \times t_{clock-Q-\max} + t_{set-up} + t_{skew}} \tag{5-12}$$

$$= \frac{1}{(4m+6) \times t_{FO-4}^{worst-case}}$$

$$f_{clock\_\max}^{syn} = \frac{1}{t_{clock\_\max}^{syn}} = \frac{1}{1 \times \left(t_{clock-Q-\max} + t_{set-up} + t_{skew}\right) + t_{\log ic\_\max}^{n\_And}} \tag{5-13}$$

$$= \frac{1}{\alpha \times t_{FO-4}^{worst-case}}$$

where the propagation delay of the m-bit "And" gate is scaled by $t_{\log ic\_\max}^{n\_And} = m \times t_{FO-4}^{worst-case}$, the propagation delay of the Flip-Flop is scaled by $t_{clock-Q-\max} = 4 \times t_{FO-4}^{worst-case}$ and α represents the speed of the synchronous counter and is further explained in (5-14).

$$\alpha = \begin{cases} 10 & when\ m = 1 \\ (m+10) & when\ m > 1 \end{cases} \tag{5-14}$$

From the viewpoint of gate timing, the synchronous counter will be much faster than the ripple counter; this kind of advantage will become more significant when the number of bits increases. As the maximum clock frequency is constrained by the counter, if we want to design a DPWM with higher maximum output frequency, we need to select a fast counter. Therefore, the synchronous counter with parallel enable logic [5-61] illustrated in Figure 5-7 is recommended.

We notice that α in (5-14) will increase with m. For the simplicity of analysis and from a practical implementation point of view, we usually prefer to make the design a little bit conservative, so a larger α should be selected. Thus $\alpha = 20$ is suggested for designs satisfying $m < 10$ as given in (5-15).

$$\alpha = 20 \quad when \quad m < 10 \tag{5-15}$$

5.5.1.2 MSF analysis

From equations (5.2) and (5-13), we can derive the maximum frequency of a general m-bit Counter DPWM in (5-16).

$$f_{\max\_frequency}^{counter} = \frac{f_{clock\_\max}^{syn}}{2^m} = \frac{1}{2^m \times \alpha \times t_{FO-4}^{worst-case}} \tag{5-16}$$

Assuming the AMI06 process, m=9 and a synchronous counter, we substitute (5-15) into (5-16) to derive the maximum output frequency in the Counter DPWM as in (5-17).

$$f_{\max\_frequency}^{counter} = \frac{1}{2^9 \times 20 \times 252\,ps} = 0.39 \quad MHz \tag{5-17}$$

On the basis that $f_{\max\_frequency}^{counter}$ is a value less than 10 MHz, following the discussion in subsection 5.3.2, we will conclude that the MSF of a digital DC-DC converter with the 9-bit Counter DPWM will be limited as the maximum output frequency of the DPWM $f_{\max\_frequency}^{counter}$. The same conclusion exists when m>4. In summary, a general equation for the maximum output frequency in the Counter DPWM is given in (5-18), a particular version of (5-18) is given in (5-19) for the AMI06 process and the synchronous counter where $t_{FO-4}^{worst-case} = 252\,(ps)$ and $\alpha = 20$ when m is less than 10, and a complete equation to describe the MSF in a digital DC-DC converter with the Counter DPWM and AMI06 technology will be given by (5-20).

$$f_{\max\_frequency}^{counter} = \frac{1}{2^m \times \alpha \times t_{FO-4}^{worst-case}}\ Hz \tag{5-18}$$

$$f_{\max\_frequency}^{counter} = \frac{1}{2^m \times 20 \times 252 ps} = 2^{(27.56-m)}\ Hz \tag{5-19}$$

$$MSF^{counter} = \begin{cases} f_{\max\_frequency}^{counter} = 2^{(27.56-m)}\ Hz & when\ 4 < m < 10 \\ > 10\ MHz & when\ m \le 4 \end{cases} \tag{5-20}$$

5.5.1.3 Frequency control

Switching frequency control is very important in DC-DC power converters as discussed in chapter 1. To obtain a desired system performance including power stage efficiency optimization, the switching frequency is usually designed to be a constant value or a series of selectable values in some advanced power management ICs.

The switching frequency control is a potential problem in the digital DC-DC converter. If the DPWM does not have frequency synchronization ability, there might be two different clocks in the whole system. A desired clock is set by system to time the two groups of the flip-flops in Figure 5-11, and another clock determined by the DPWM practical implementation will time the power stage switching. This kind of bi-clock operation will deteriorate the control performance and result in system instability. An engineering method to ensure one clock operation is to use the DPWM clock as a system clock [5-41]. However, the DPWM clock frequency can be sensitive to many factors such as process corners, temperature, voltage, and layout, so this technique is not a good solution for a high performance digital DC-DC converter. Based on the discussion, most of the recent DPWM designs stress their frequency control ability.

Switching frequency control is not an issue in a Counter DPWM. We can use a voltage controlled oscillator (VCO), a charge pump, and another m-bit counter to construct a phase locked loop (PLL) to generate a clock with frequency 2^m times larger than a desired system clock and use the clock as the input of the counter in the DPWM.

5.5.1.4 Revised version

Four-phase Counter DPWM [5-21] [5-3] [5-33] is a revised version of the Counter DPWM. The counter clock, which is utilized as the input of a counter for generating the MSB counter hardware resolution, is 90° phase shifted to generate a 2-bit LSB resolution with the aid of a 4:1 multiplexer. Thus, on the basis of phase allocation, the hardware resolution of the Counter DPWM can be improved by 2 bits.

In order to match delays and ensure a correct timing, however, many extra logic gates are required. The issue will become more serious when we stress the frequency control. Furthermore, as all of the gates including the Flip-Flop and mux are toggling at the counter clock, the power dissipation in the DPWM will be very significant. In summary, it is possible that the phase shift DPWM can improve the MSF by four times. However, the complex hardware implementation and large power consumption will prevent the revised counter DPWM from being adopted in a high performance digital DC-DC converter.

5.5.2 Delay_mux DPWM

Delay_mux DPWM is another type of first generation DPWM architecture [5-7]; its resolution completely comes from the Delay_mux hardware resolution introduced in subsection 5.2.2.2. Delay_mux DPWM has advantages such as a simple design, high MSF, low power dissipation, good linearity, and good frequency control. However, the Delay_mux DPWM will consume too much silicon area due to requiring a large multiplexer. Equation (5-4) concludes that in a k-bit DPWM the number of the delay cells in the delay chain illustrated in Figure 5-3 would be $2^{k}-1$. Thus, for a 9-bit DPWM, the required number of the delay cell will be $\left(2^{9}-1\right)=511$ and the associated multiplexer will be a 512:1 mux. This is the reason why a pure Delay_mux DPWM is not utilized in a high resolution DPWM implementation and its practical application is

always accompanied with soft resolution [5-45], [5-30] or the segmentation technique [5-54] [5-58].

5.5.2.1 Fastest delay chain

To determine the maximum output frequency in a Delay_mux DPWM, we need to investigate the minimum delay that a unit delay cell can provide in a semiconductor process. An inverter may be the fastest delay cell, i.e., the delay cell with the minimum propagation delay. In order to implement frequency control, the inverter should be a current starved type so that its delay can be regulated by a PLL. Furthermore, to correct the phase inversion at two neighboring output nodes in the delay chain, two types of cells with an identical propagation delay - a "N" inverter type cell and a "P" buffer type cell - are alternatively added at all output nodes in the delay chain. The aforementioned fastest Delay_mux DPWM is illustrated in Figure 5-8.

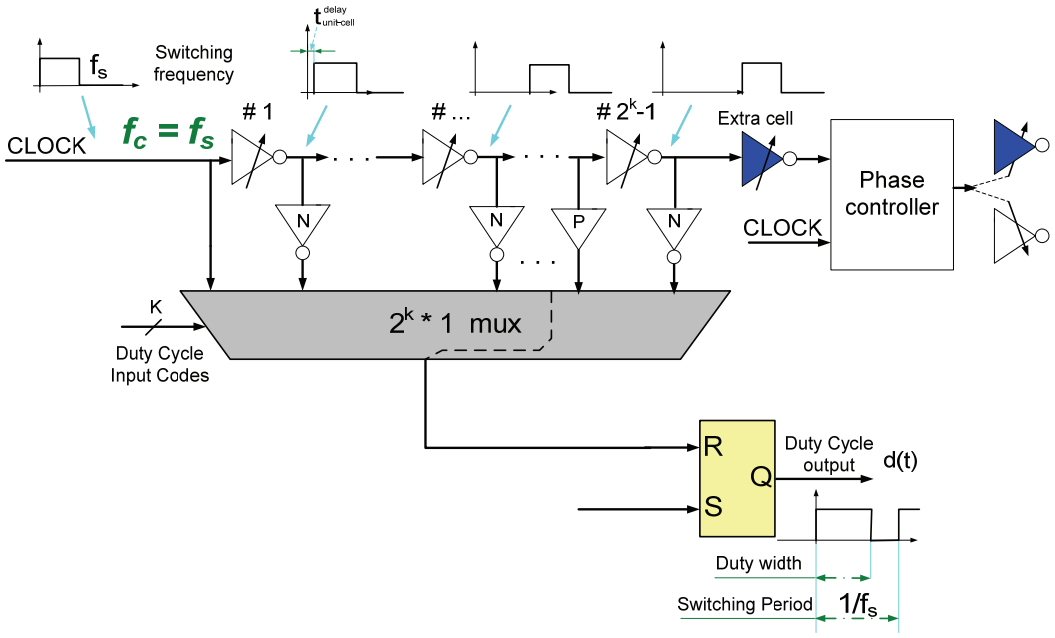


Figure 5-8. Delay_mux DPWM with the fastest delay chain

5.5.2.2 MSF analysis

For the Delay_mux in Figure 5-18, the number of total delay cells is 2^k including $2^k - 1$ delay cells in the delay chain, and one extra cell added for the implementation of frequency control. Assuming the frequency control is well applied, we will get two equations in (5-21) and (5-22).

$$f_{\max\_frequency}^{Delay\_mux} = f_C^{Delay\_mux} = f_S^{Delay\_mux} \tag{5-21}$$

where $f_C^{Delay\_mux}$ is the input clock frequency, $f_S^{Delay\_mux}$ is the desired switching frequency, and $f_{\max\_frequency}^{Delay\_mux}$ is the maximum output frequency of the Delay_mux DPWM.

$$f_{\max\_frequency}^{Delay\_mux} = \frac{1}{2^k \times t_{unit-cell}^{delay}} = \frac{1}{2^k \times t_{FO-4}^{worst-case}} \tag{5-22}$$

For a 9-bit Delay_mux DPWM in the AMI06 process, substituting (5-9) into (5-22), we an conclude a concrete value of $f_{\max\_frequency}^{Delay\_mux}$ in (5-23).

$$f_{\max\_frequency}^{Delay\_mux} = \frac{1}{2^9 \times 252(ps)} = 7.75 \quad MHz \tag{5-23}$$

As $f_{\max\_frequency}^{Delay\_mux}$ is less than 10 MHz, following the discussion in the subsection 5.3.2, we will conclude that the MSF of a digital DC-DC converter with the 9-bit Delay_mux DPWM is limited being the maximum output frequency $f_{\max\_frequency}^{Delay\_mux}$ of the DPWM. This conclusion may be questionable when $k \le 8$, as in the case $f_{\max\_frequency}^{Delay\_mux} > 10MHz$ exists and there is a possibility that other limitations discussed in subsection 5.3.2 become dominant. In summary, a general equation for the maximum output frequency in a

Delay_mux DPWM is given in (5-24), a particular version of (5-24) is given in (5-25) for the AMI06 process and the inverter delay cell where $t_{FO-4}^{worst-case} = 252\,(ps)$, and a complete equation to describe the MSF in a digital DC-DC converter with the Delay_mux DPWM and AMI06 technology is (5-26).

$$f_{\max\_frequency}^{Delay\_mux} = \frac{1}{2^k \times \beta \times t_{FO-4}^{worst-case}}\ Hz \tag{5-24}$$

where β scales the delay of the unit delay cell with the FO-4. For an inverter, $\beta = 1$.

$$f_{\max\_frequency}^{Delay\_mux} = \frac{1}{2^k \times 252\,ps} = 2^{(31.89-k)}\ Hz \tag{5-25}$$

$$MSF^{Delay\_mux} = \begin{cases} f_{\max\_frequency}^{Delay\_mux} = 2^{(31.89-k)}\ Hz & when\ k > 8 \\ > 10\ MHz & wehn\ k \le 8 \end{cases} \tag{5-26}$$

5.5.2.3 Frequency control

Figure 5-8 in the subsection 5.5.2.2 illustrates a simple digital locked loop (DLL) to implement a narrow-range frequency control in the Delay_mux DPWM. To make sure that the DPWM works through process, voltage, and temperature (PVT) variations, however, a DLL supporting wide-range frequency control is imperative which will be discussed in subsection 5.5.4.5 and 5.6.1. Frequency control is not a design issue in the Delay_mux DPWM, but its implementation may sacrifice silicon area and power to a noticeable extent.

5.5.2.4 Revised version

One segmentation technique [5-54] [5-58] was proposed as a solution to significantly decrease the silicon area in the Delay_mux DPWM and its principle is explained with (5-27).

$$\Delta t_i = 2^j \times \Delta t_{i-1} \tag{5-27}$$

where Δt_i is the propagation delay time of the unit delay cell in the (i) stage, Δt_{i-1} is the time in the $(i-1)$ stage, and j is the resolution bit number in each stage.

All of the unit delay cells in a segmented DPWM are grouped into several stages and the delay time of the unit delay cell in different stages will differ by a 2 power exponential relationship. The exponential index is equal to the bit of resolution designed in each segmentation stage. For example, in [5-54] [5-58], there are three stages of segmentation and each stage is designed with 2-bit resolution, so the total resolution bits will be 6, and the exponential index is 2.

On the basis of the segmentation, the most significant area saving is from the multiplexer. Without the segmentation, for a 6-bit Delay_mux DPWM, a 64:1 mux is necessary. On the contrary, three 4:1 muxes will be enough with segmentation. Another kind of area saving is in the required delay cells. First, the total number of the delay cells is significantly decreased. Second, if we can effectively control the unit delay cell's delay time, then the unit delay cells with much larger delay time may be the same size as those with small delay time. Thus, a significant area reduction is obtained

The segmentation DPWM has a significant issue with frequency control, i.e., satisfying (5-27) in all segmented stages for a wide-range frequency. A solution was proposed in [5-58], where three sets of DLLs were applied to control the frequency. As a wide-range DLL's implementation [5-16] typically requires a large silicon area and high power consumption, the practical area saving through segmentation may not be as good as

expected. Furthermore, the existence of multiple DLL's makes the dynamic performance of the frequency regulation difficult to analyze.

In summary, the segmentation technique does not improve the MSF capacity of the Delay_mux DPWM, as the total delay time of all the delay cells does not change. The segmentation technique can significantly decrease the silicon area occupied. However, the advantage may be seriously degraded when frequency control is stressed.

5.5.3 Self-oscillation hybrid DPWM

Self-oscillation Hybrid (SOH) DPWM is a hybrid integration of the Counter DPWM and the Delay_mux DPWM; it was proposed to obtain a tradeoff between power dissipation and silicon area as discussed in [5-8, 5-17, 5-66]. A typical SOH DPWM is illustrated in [5-41]. Other similar architectures can be found in [5-6, 5-8, 5-11, 5-17, 5-66]. The unit delay cell in [5-41] is a resettable Flip-Flop. Other versions of the unit delay cell include the ring oscillator in [5-6] and the buffer in [5-8, 5-11, 5-17, 5-66]. The SOH DPWM is one of the popularly selected architectures for a high frequency high resolution DPWM design.

In the SOH DPWM, an expected hardware resolution will be divided into two parts and distributed separately to the counter and the Delay_mux. Let us assume that the total resolution is R bits: the MSB m-bit will be distributed to the counter to generate the coarse resolution and the LSB k-bit will be assigned to the Delay_mux to generate the fine resolution. The relationship of m, k and R will satisfy the equation (5-28). Furthermore, a large m value implies more power consumption as introduced in subsection 5.5.1, while a large k value implies more silicon area occupied. Thus, some combination of the m and k may be an optimized solution for a specified application.

$$R = m + k \tag{5-28}$$

where R is the total resolution bit of the SOH DPWM, m is the number of resolution bits of the counter, and k is the number of resolution bits of the Delay_mux.

5.5.3.1 Restraint clock frequency

We have derived $f_{\max\_frequency}^{counter}$ of a standalone Counter DPWM in (5-18) and $f_{\max\_frequency}^{Delay\_mux}$ of a standalone Delay_mux DPWM in (5-24). In this subsection, we will derive the MSF in a hybrid DPWM.

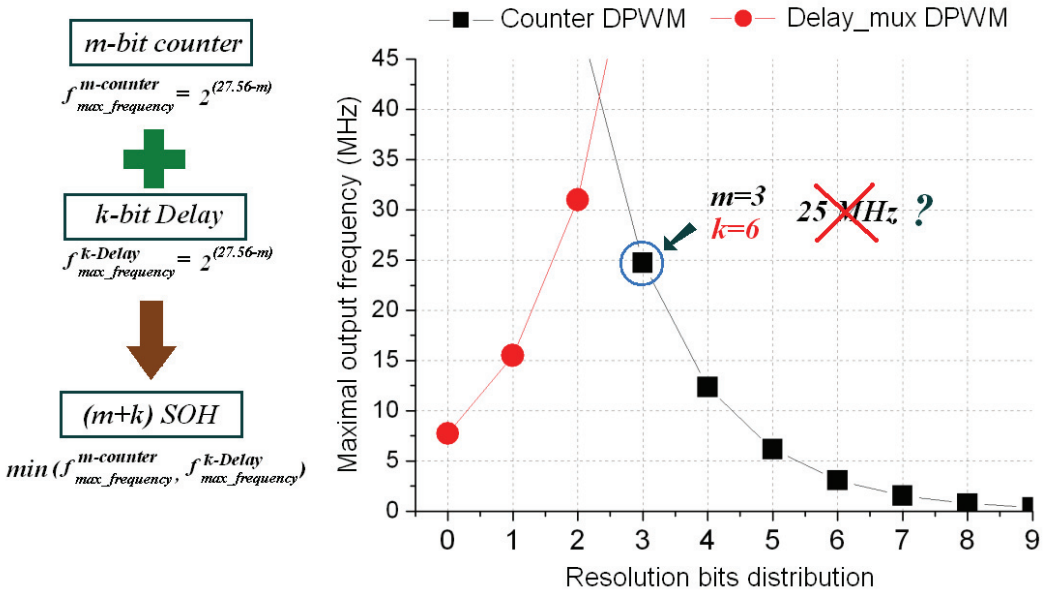


Figure 5-9. Trial analysis of the maximal output frequency in a SOH DPWM

Figure 5-9 illustrates a trial analysis of the maximum output frequency in a 9-bit hardware resolution SOH DPWM. The X-axis gives different sets of m and k combinations where m will increase along the x-axis and as a consequence k will

decrease following (5-28) in which R equals 9 in the example. The black rectangle shows the maximum output frequency $f_{\max\_frequency}^{m-counter}$ in a standalone Counter DPWM for different values of m, which are calculated with (5-18). The red dot shows the maximum output frequency $f_{\max\_frequency}^{k-Delay\_mux}$ in a standalone Delay_mux DPWM for different values of k, which are calculated with (5-24). For a SOH DPWM consisting of both the m-bit counter and the k-bit Delay_mux, we can directly conclude the maximum output frequency $f_{\max\_frequency}^{SOH}$ as shown in equation (5-29).

$$f_{\max\_frequency}^{SOH} = \min\left(f_{\max\_frequency}^{m-counter}, f_{\max\_frequency}^{k-Delay\_mux}\right) \tag{5-29}$$

If we follow equation (5-29), with the aid of Figure 5-9 we will conclude that $f_{\max\_frequency}^{SOH}$ is equal to 25MHz for the case m=3, k=6, and R=9. In practice, unfortunately, we cannot approach 25 MHz in a standalone 9-bit hardware resolution SOH DPWM with the AMI06 process, which implies that there may be something unclear behind the SOH DPWM.

Let us reconsider the principle of SOH DPWM and focus our attention on the relationship between the counter and the delay chain in the typical SOH DPWM illustrated in [5-41]. We notice that the clock input of the counter will be generated by the delay chain, i.e., the clock input of counter is ***not an independent signal as the one*** we had discussed in subsection 5.5.1. As a result, the clock frequency value may be restrained by the delay chain.

As the Flip-Flop delay cells are cascaded connected in a closed loop, the maximum clock frequency $f_{clock\_\max\_ideal}^{SOH\_FF}$ generated by the delay chain in the typical SOH DPWM illustrated in [5-41] can be calculated with (5-30).

$$f_{clock\_\max\_ideal}^{SOH\_FF} = \frac{1}{2^k \times t_{unit-cell}^{delay\_FF}} = \frac{1}{2^{k+2} \times t_{FO-4}^{worst-case}} \tag{5-30}$$

where k is the resolution bit of the Delay-mux in the SOH DPWM, and $t_{unit-cell}^{delay\_FF}$ is the propagation delay of the Flip-Flop. From Table 5-1, $t_{unit-cell}^{delay\_FF} = t_{clock-Q} = 4 \times t_{FO-4}^{worst-case}$.

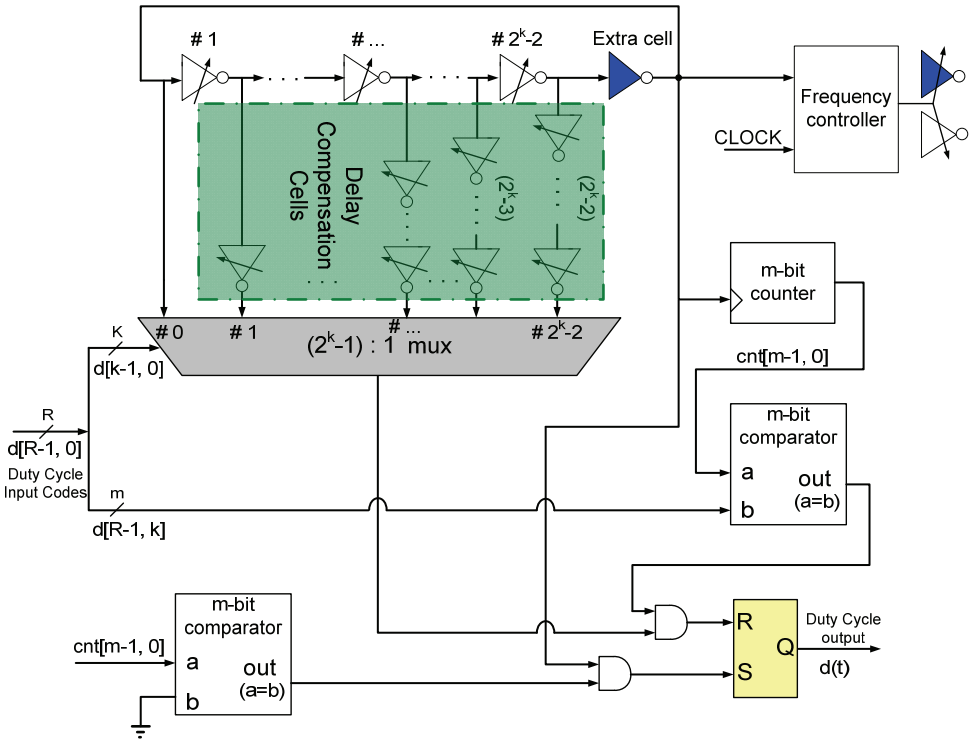


Figure 5-10. SOH DPWM with an improved maximum clock frequency

A Flip-Flop is typically four times the FO-4 delay, so the delay chain in the typical SOH DPWM illustrated in [5-41] is not fast enough to approach the maximum clock frequency in the SOH DPWM. If we replace the Flip-Flop type unit delay cell with an inverter type delay cell, we will get an SOH DPWM illustrated in Figure 5-10 with the fastest delay chain and an improved maximum clock frequency. However, in Figure 5-10 we will meet with another challenge: the delay time of the unit delay cell in the delay chain is only half of the fine resolution value expected. To compensate the large delay gap, we have to add many branches of delay compensation cells between the nodes of the delay chain and the input terminals of the multiplexer so that in each branch the total

delay time equals the value expected. For example, as illustrated in Figure 5-10, $2^k - 2$ unit inverter delay cells are added between the last node of the delay chain and the associated multiplexer's input terminal so that the total delay time in the branch is $2 \times \left(2^k - 2\right) \times t_{unit-cell}^{delay\_INV}$. $t_{unit-cell}^{delay\_INV}$ is the delay time of an inverter. From Table 5-1, $t_{unit-cell}^{delay\_INV} = t_{FO-4}^{worst-case}$.

The maximum clock frequency $f_{clock\_\max\_ideal}^{SOH\_INV}$ that the delay chain could support is given in (5-31). The total number of delay cells N_{cells} is counted in (5-32).

$$f_{clock\_\max\_ideal}^{SOH\_INV} = \frac{1}{2 \times \left(2^k - 1\right) \times t_{unit-cell}^{delay\_INV}} = \frac{1}{\left(2^{k+1} - 2\right) \times t_{FO-4}^{worst-case}} \tag{5-31}$$

$$\begin{aligned} N_{cells} &= N_{delay\_chain} + N_{compensation\_cells} = \left(2^k - 1\right) + \sum_{i=1}^{2^k - 2} (i) \\ &= \left(2^k - 1\right) + \left(2^k - 1\right) \times \left(2^{k-1} - 1\right) = \left(2^k - 1\right) \times 2^{k-1} \end{aligned} \tag{5-32}$$

where N_{delay_chain} is the total number of the unit delay cells in the delay chain and $N_{compensation\_cells}$ is the total number of the delay compensation cells in all $2^k - 2$ branches.

5.5.3.2 Choke effect and choke region

By replacing the Flip-Flop type delay cell with the inverter type delay cell, we can increase the maximum clock frequency of the SOH DPWM by almost two times. As the output frequency in the SOH DPWM in Figure 5-10 is determined by the output signal of the m-bit counter, if we assume that the m-bit counter is an ideal component, the maximum output frequency of the SOH DPWM could be given by (5-33).

$$f_{\max\_frequency\_ideal}^{SOH\_INV} = \frac{1}{2^m \times \left(2^{k+1}-2\right) \times t_{FO-4}^{worst-case}} = \frac{1}{\left(2^{R+1}-2^{m+1}\right) \times t_{FO-4}^{worst-case}} \quad (5\text{-}33)$$

where $f_{\max\_frequency\_ideal}^{SOH\_INV}$ refers to the maximum output frequency in the SOH DPWM when the counter is an ideal component.

After calculating out the values of $f_{\max\_frequency\_ideal}^{SOH\_INV}$ for different set of m and k, and plotting them with green inverse triangles, we will get Figure 5-11. In Figure 5-11, we can notice an intersection point of the green inverse triangle curve and the black rectangle curve. The intersection point is highlighted with a red star. As introduced in subsection 5.5.3.1, the black rectangle curve represents the maximum output frequency in a standalone Counter DPWM. Thus, the intersection point in fact reflects the impact from the limitation of the counter's implementation.

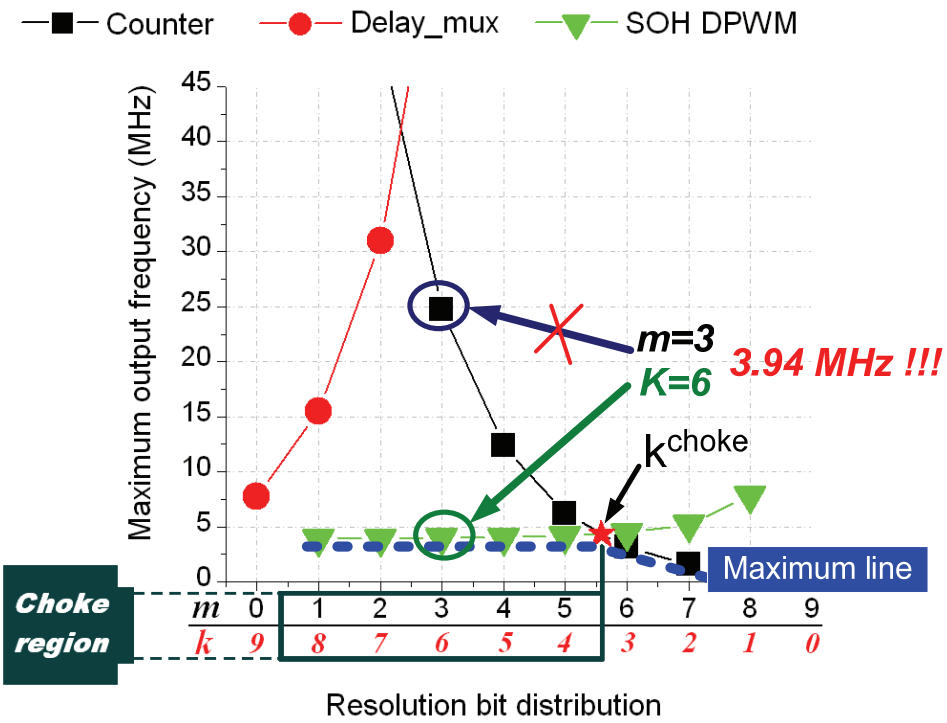


Figure 5-11. Choke effect in the SOH DPWM

Realizing that $f_{clock\_\max\_ideal}^{SOH\_INV}$ in (5-31) is the maximum clock frequency generated by the delay line and $f_{clock\_\max}^{syn}$ in (5-13) is the maximum clock frequency acceptable to the m-bit counter, we could derive a complete equation in (5-34) to calculate the maximum clock frequency $f_{clock\_\max}^{SOH\_INV}$ in the SOH DPWM.

$$f_{clock\_\max}^{SOH\_INV} = \min\left(\frac{1}{\left(2^{k+1}-2\right)\times t_{FO-4}^{worst-case}}, \frac{1}{\alpha \times t_{FO-4}^{worst-case}} \right) \tag{5-34}$$

It is safe for us to conclude that the maximum output frequency $f_{\max\_frequency}^{SOH\_INV}$ in the SOH DPWM can be calculated with (5-35).

$$f_{\max\_frequency}^{SOH\_INV} = \frac{f_{clock\_\max}^{SOH\_INV}}{2^m} = \min\left(\frac{1}{\left(2^{R+1}-2^{m+1}\right)\times t_{FO-4}^{worst-case}}, \frac{1}{2^m \times \alpha \times t_{FO-4}^{worst-case}} \right) \tag{5-35}$$

For the SOH DPWM with a synchronous counter, i.e., $\alpha = 20$, we can outline the maximum output frequency curve in Figure 5-11 with a blue dashed line. The blue dashed line is in fact the bottom line of three curves . We can observe that part of the blue dashed line located at the left hand of the red star is very ***flat along the X-axis***, which demonstrates that the maximum output frequency of the SOH DPWM is insensitive to the combination of m and k. This is the reason why we claim there is a "***choke effect***" in the SOH DPWM which will make the maximum output frequency almost constant [5-63]. The intersection point denoted with k^{choke} is "start point" of the choke effect and its value can be calculated with (5-36). When one set of resolution combinations is located at the left hand side of the starting point, i.e., when k is larger than k^{choke}, the maximum output frequency of the SOH DPWM will be restraint by the clock frequency generated by the delay line so that the SOH DPWM works in a "***choke region***".

$$k^{choke} = \log_2\left(\frac{\alpha + 2}{2}\right) \tag{5-36}$$

In summary, the SOH DPWM has four different operating regions as shown in Figure 5-11. When $k = 0$, the SOH DPWM will degenerate into a Counter DPWM; when $0 < k < k^{choke}$, the SOH DPWM works in a normal mode where the maximum output frequency will vary as k increases; when $k^{choke} < k < R$, the SOH DPWM works in the choke mode where the maximum output frequency remains almost constant with k variation; and when k satisfies $k = R$, the SOH DPWM will degenerate into a Delay_mux DPWM. The length of the choke region is denoted by $Lengh^{choke}$ in (5-37).

$$Lengh^{choke} = R - k^{choke} - 1 \tag{5-37}$$

If we assume a 9-bit resolution DPWM with the synchronous counter, we can use (5-36) and (5-37) to get $k^{choke} = 3.46$ and $Lengh^{choke} = 4.54$ as shown in Figure 5-11.

5.5.3.3 MSF analysis

From Figure 5-11, we observe that the maximum output frequency remains smaller than 10 MHz no matter how we distribute m and k. The peak value is 4.13 MHz which happens when m=5 and k=4. In the example case where m=3 and k=6, the maximum output frequency is 3.94 MHz. In comparison with 25 MHz which is inferred in the trial analysis shown in Figure 5-9, the maximum output frequency concluded in (5-35) is reduced by six times.

As $f_{\max\_frequency}^{SOH\_INV}$ in the 9-bit DPWM is less than 10 MHz, following the discussion in the subsection 5.3.2, we can conclude that the MSF of a digital DC-DC converter with the 9-bit SOH DPWM will be limited to the maximum output frequency of the DPWM

$f_{\max\_frequency}^{SOH\_INV}$. This conclusion exists for all sets of m and k combinations when $R \geq 8$ exists, i.e., a high resolution DPWM. Thus, a complete equation to describe the MSF in a digital DC-DC converter with the SOH DPWM and AMI06 technology will be in (5-38).

$$MSF^{SOH\_INV} = \frac{f_{clock\_\max}^{SOH\_INV}}{2^m} \tag{5-38}$$

$$= \begin{cases} \min\left(\frac{1}{\left(2^{R+1} - 2^{m+1}\right) \times t_{FO-4}^{worst-case}}, \frac{1}{2^m \times \alpha \times t_{FO-4}^{worst-case}} \right) Hz & when\ R \geq 8 \\ > 10\ MHz & when\ R < 8 \end{cases}$$

To test the feasibility of the proposed equation in (5-38), I list the MSF value reported in [5-8] [5-17] [5-41] [5-66] and compare them with a predicted value from (5-30) or (5-38) or its modified version.

Case 1): Chip implementation, m=4, k=6 (2 segmentation stage), R=10, $0.6\mu m$ CMOS process, buffer type delay cell [5-8] [5-17].

The reported MSF is 0.5 MHz in test. As the delay cell is the buffer, so we need a minor modification of the (5-38) and the modified equation is $\frac{1}{2 \times \left(2^{R+1} - 2^{m+1}\right) \times t_{FO-4}^{worst-case}}$. Thus, the predicted MSF is 0.98 MHz and the reported 0.5 MHz is a reasonable number.

Case 2): Chip implementation, m=5, k=4, R=9, $0.8\mu m$ CMOS process, buffer type delay cell [5-66].

The reported MSF is 1 MHz in test. As the delay cell is the buffer, so we use $\frac{1}{2 \times \left(2^{R+1} - 2^{m+1}\right) \times t_{FO-4}^{worst-case}}$ for prediction and the predicted MSF is 1.55 MHz. Thus, the reported 0.5 MHz is a reasonable number.

Case 3): Chip implementation, m=3, k=5, R=8, $0.5\mu m$ CMOS process, Flip-Flop type delay cell [5-41].

The reported MSF is 1 MHz in test. As the delay cell is the Flip-Flop, so we use (5-30) for prediction of the maximum clock frequency and the equation for MSF would be $\frac{1}{2^{R+2} \times t_{FO-4}^{worst-case}}$. From the equation, the predicted MSF is 4.65 MHz. Thus, the reported 1 MHz is a conservative number.

5.5.3.4 Relative matching error

For an ideal hybrid DPWM, the total delay time from the input terminal of the delay chain to the last input terminal of the mux (including the total delay time of the delay compensation cells in the last branch) should be exactly one time step less, as defined by the finest resolution, than the period of the counter clock. The requirement guarantees a seamless transition between the Delay_mux fine resolution and the Counter coarse resolution.

The relative matching error refers to the worst case relative error between the period of the counter clock and the sum of one time step and the total delay time from the input terminal of the delay chain to the last input terminal of the mux (including the total delay time of the delay compensation cells in the last branch). If we denote the relative matching error as δ, the error can be calculated with (5-39).

$$\delta = \left| \frac{t_{clock\_period}^{counter} - (M+1) \times t_{unit-cell}^{delay}}{(M+1) \times t_{unit-cell}^{delay}} \right|_{worst-case} \tag{5-39}$$

where M denotes the number of unit delay cell in the delay chain between the input terminal of the delay chain and the last input terminal of the mux. $t_{clock\_period}^{counter}$ denotes the period of the counter clock.

For the typical SOH DPWM in [5-41] or the architecture in Figure 5-10, we can observe that the architecture of the SOH DPWM guarantees a perfect matching between the fine and coarse resolution. Thus, the relative matching error of the SOH DPWM is zero.

5.5.3.5 Frequency control

The typical SOH DPWM in [5-41] does not support the switching frequency control. The SOH DPWM in Figure 5-10 can realize the switching frequency control with the aid of a PLL.

5.5.3.6 Power dissipation

We notice that the delay chain in both the typical SOH DPWM in [5-41] and the architecture in Figure 5-10 accomplishes two functions. The first one is to output signals with the finest resolution time difference and the second one is to generate the counter clock. Thus, all of the delay cells and the compensator cells will be toggling at the counter clock frequency which will be 2^m times larger than DPWM output frequency.

If we set up a unit power dissipation scale $Power_{unit}$ which denotes the dynamic power dissipation of one unit delay cell toggling at the DPWM's output frequency, according to [5-44], the total dynamic power dissipation for all of the unit delay cells and compensator cells in Figure 5-10 can be approximately estimated by (5-40).

$$Power_{cells}^{SOH\_INV} = 2^m \times \left(2^k - 1\right) \times 2^{(k-1)} \times Power_{unit} \tag{5-40}$$

(5-40) implies that $Power_{cells}^{SOH\_INV}$ may be a very large number. If m=3 and k=6, a particular value of $Power_{cells}^{SOH\_INV}$ is calculated in (5-41).

$$Power_{cells}^{SOH\_INV} = 16{,}632 \times Power_{unit} \tag{5-41}$$

If we use the Flip-Flop type SOH DPWM in Figure 5-19, (5-30) implies that the maximum output frequency will be 50% lower than the DPWM in Figure 5-21. Furthermore, its total dynamic power dissipation for all of the delay cells can be approximately calculated by (5-42).

$$Power_{cells}^{SOH\_FF} = 2^m \times \left(2^k - 1\right) \times \eta_{FF} \times Power_{unit} \tag{5-42}$$

where η_{FF} is a normalized value of the Flip-Flop dynamic power to an inverter's dynamic power. In the Table 5-6, I will assume $\eta_{FF} = 40$.

5.5.4 Non-self-oscillation hybrid DPWM

(5-41) and (5-42) indicate that the power dissipation in the SOH DPWM may be significant and a large power reduction can be realized by eliminating the right hand first item 2^m in (5-41) and (5-42). This is what has been done in the non-self-oscillation Hybrid (NSOH) DPWM architectures [5-56] [5-71] [5-29] [5-30] recently developed and a representative NSOH DPWM is illustrated in [5-71].

The motivation of the NSOH DPWM [5-71] is to develop a distinctive digital programmable delay cell so as to provide the frequency control capacity for those hybrid DPWMs designed with a standard synthesizable hardware description language and without a synthesizable design for an analog PLL. Another advantage along with the NSOH DPWM is that it greatly slows down the delay chain and makes the delay cells in the delay chain toggle at the output frequency of DPWM, but not at the 2^m times larger counter clock frequency. As a result, the power dissipation of the DPWM can be significantly decreased. As shown in [5-71], the frequency of the input signal in the delay

line is determined by the counter's output "cnt_out;" it equals the output frequency of the DPWM.

If we compare the NSOH DPWM architecture [5-71] with the typical SOH DPWM in [5-41] (or Figure 5-10), we notice that the first major difference is that the counter is moved from the output terminal of the delay chain in the typical SOH DPWM in [5-41] (or Figure 5-10) to a place before the input terminal of the delay chain in the NSOH DPWM architecture [5-71]. As a result, the relationship between the counter and the delay chain is much simplified as a "first counter then delay chain" series link. In another word, the counter clock in the typical SOH DPWM in [5-41] (or Figure 5-10) is generated by the delay chain. On the contrary, in the NSOH DPWM [5-71] the counter clock comes from an external signal. Thus, the SOH architecture is a self oscillation system but the NSOH architecture is a non-self-oscillation system requiring an external clock. The second major difference is that the total delay time in the delay chain in the NSOH DPWM [5-71] is assumed to be exactly one of the finest resolution time-steps less than $1/2^m$ of the period of the signal propagating in the delay chain, but in the SOH architecture in [5-41] the total delay time in the delay chain is naturally and exactly to be one of the finest resolution time step less than the period. For the architecture in Figure 5-10, the total delay time in the delay chain is naturally and exactly one finest resolution time step less than one half of the period. Thus, the NSOH DPWM architecture requires the matching of the fine and coarse resolution with the aid of digital programming as well as phase control and thereby has a relative matching error, but the SOH DPWM ensures a naturally seamless match and the relative matching error is zero.

The aforementioned comparison is important for the following performance analysis.

5.5.4.1 Digital programmable delay cells

In order to provide a good match between the fine resolution in the delay chain and the coarse resolution in the counter, the total delay time throughout the delay chain should be exactly one of the finest resolution time step less than the period of the counter clock, i.e.,

the delay time of one delay cell $t_{unit\_cell}^{delay}$ in the delay chain should satisfy equation (5-43) for a specified switching frequency f_S.

$$t_{unit\_cell}^{delay} = \frac{t_S}{2^{m+k}} = \frac{1}{2^R \times f_S} \tag{5-43}$$

The architecture of the NSOH DPWM implies that its fine-coarse resolution match heavily depends on the unit delay cell's delay programming. Furthermore, its maximum output frequency will be heavily impacted by the delay offset in one delay cell, as the minimum delay time in one cell will be the sum of the delay resolution time – the delay time of the delay element - in the delay cell and the delay offset. On the contrary, in an ideal case, the programming delay cell will not have delay offset, so the maximum output frequency will be determined only by the delay resolution time and the output frequency will be inversely proportional to the decimal value of the programmed code.

5.5.4.1.1 One kind of delay cell

[5-71] shows one example of a g-bit digitally programmed delay cell, in which 2^g parallel branches connect the input i_{k-1} to the output i_k and the delay difference between two neighbor branches is the delay resolution time $t_{element}^{delay}$ in one delay cell. Here, two 2-bit Nor gates constitute a delay element and the delay resolution time $t_{element}^{delay}$ is the propagation delay of the two 2-bit Nor gates.

The delay time of a unit delay cell in [5-71] will be the sum of the logic effort of the delay cell, the intrinsic propagation time of the delay elements and the intrinsic propagation time of the constant delay path. The delay offset t_{offset}^{delay} comes from the sum of the logic effort and the intrinsic propagation time of the constant delay path. The constant delay path includes a 2-bit Nor gate and a 2^g-bit Nand gate and will be identical

in all branches. The logic effort is determined by the number of the branches. Thus, the total delay time of a delay cell is given in (5-44)

$$t_{unit\_cell}^{delay} = t_{offset}^{delay} + t_{element}^{delay} \tag{5-44}$$

where t_{offset}^{delay} denotes the delay offset in (5-45) and $t_{element}^{delay}$ is given in (5-46).

$$t_{offset}^{delay} = t_{\log ic\_effort}^{delay} + t_{cons\tan t\_delay\_path}^{delay} = 3 \times 2^{g} \times t_{FO-4}^{worst-case} \tag{5-45}$$

where the propagation delay of a 2^{g} -bit Nand gate is approximately estimated as $2^{g} \times t_{FO-4}^{worst-case}$ and the logic effort of 2^{g} parallel 2-Nor is approximately estimated as $2 \times 2^{g} \times t_{FO-4}^{worst-case}$ [5-9].

$$t_{element}^{delay} = 2 \times 2 \times N \times t_{FO-4}^{worst-case} = 4 \times N \times t_{FO-4}^{worst-case} \tag{5-46}$$

where N denotes which branch is selected by the programmed code and is in the range [0: $2^{g} - 1$].

The delay cell's minimum delay time is given on (5-47) and the maximum delay time is $\left[3 \times 2^{g} + 4 \times \left(2^{g} - 1\right)\right] \times t_{FO-4}^{worst-case}$ which is available in the 2^{g} branch.

$$t_{unit\_cell\_(a)}^{delay\_\min} = 3 \times 2^{g} \times t_{FO-4}^{worst-case} \tag{5-47}$$

The total number of the delay elements in 2^{g} parallel branches is $2^{(g-1)} \times \left(2^{g} - 1\right)$. Besides, $\left(2^{g} + 1\right)$ standard 2^{g} -bit Nand gates and $\left(2^{g}\right)$ standard 2-bit Nor gates are necessary to implement the digital programming. In summary, the total gates needed in one unit delay cell are in Table 5-2.

Table 5-2. Gates Breakdown in a programming delay cell [5-56], [5-71]

[5-56] [5-71]	2* 2-bit Nor	2^g -bit Nand	2-bit Nor
function	Delay element	logic	Logic
number	$2^{(g-1)} \times (2^g - 1)$	$(2^g + 1)$	2^g

5.5.4.1.2 Another kind of delay cell

[5-29] and [5-30] shows another kind of digitally programmed delay cell in which one elemental and four binary-weighted current mirrors can provide 4-bit delay time resolution. Each delay cell is constructed in two stages. The first stage is a current starved inverter, and the second stage is a regular inverter. The pull up network (PUN) of the first stage is a PMOS, but the pull down network (PDN) includes five parallel branches and in each branch two NMOS are series connected. In order to realize a quantized resolution, the bottom NMOS transistor in the PDN is binary sized. For example, Q11 in [5-29] [5-30] is 8 times larger than Q7. The total gates needed for one unit delay cell are given in Table 5-3.

Table 5-3. Gates Breakdown in a programmable Delay Cell [5-29], [5-30]

[5-29] [5-30]	2-And	Standard NMOS	5 binary-sized-NMOS	Inverter
function	Logic	PDN-Delay-control	PDN-Delay-generation	conditioner
number	$(g+1)$	$(g+1)$	$(g+1)$	**1**

The delay resolution path in [5-29] [5-30] shows that the delay resolution time is the pull down time of the unit delay cell's first stage when all branches switch on. Unlike the delay element in [5-71], the delay element in [5-29] [5-30] is not straight. Also, the delay

time of the unit delay cell will be increased to some extent if partial branches are switched off.

Two-stage architecture is imperative for the delay cell in [5-29] [5-30]. Furthermore, in order to have a better controllability of the pull down time, the aspect ratio of the top NMOS in the PDN has to be much bigger [5-36] than that of bottom NMOS; a recommended value of the aspect ratio is 3. The PMOS in the PUN is usually sized two to three times larger than the top NMOS in the PDN to balance the pull up and the pull down time. Thus, the total delay time of a delay cell is the same as (5-44) but t_{offset}^{delay} is given in (5-48) and $t_{element}^{delay}$ is given in (5-49).

$$t_{offset}^{delay} = t_{pull\_up}^{delay} + t_{inverter}^{delay} = \frac{(g+5)}{2} \times t_{FO-4}^{worst-case} \tag{5-48}$$

where the propagation delay of a inverter is estimated as $t_{FO-4}^{worst-case}$ and the pull up time is estimated as one half of the first stage's logic effort being calculated by $\frac{3\times(g+1)+3}{3} \times t_{FO-4}^{worst-case} = (g+2) \times t_{FO-4}^{worst-case}$ [5-9].

$$t_{element}^{delay} = t_{pull\_down}^{delay} = \frac{(g+2)}{2} \times N \times t_{FO-4}^{worst-case} \tag{5-49}$$

where N denotes the PDN operating condition dependent on the programmed code and is in the range [1: 2^g].

In summary, the programmed delay cell's minimum delay time is given in (5-50) and the maximum delay time is $\left[\frac{(g+5)}{2} + \frac{(g+2)}{2} \times 2^g\right] \times t_{FO-4}^{worst-case}$. The digitally programmed delay cell is noticeable in area.

$$t_{unit\_cell\_(b)}^{delay\_\min} = (g+3.5) \times t_{FO-4}^{worst-case} \tag{5-50}$$

The programmable delay cell in [5-29] [5-30] has several performance issues including the delay time linearity, large power dissipation, and asymmetric rising and falling response [5-36] [5-30]. However, comparing Table 5-3 to Table 5-2, we notice that the delay cell in [5-29] [5-30] is better than the delay cell in [5-71] from the viewpoint of the number of components, structure complexity, and delay cell speed.

5.5.4.2 Maximum output frequency

In subsection 5.5.4.1, the minimum delay time for two kinds of digitally programmable delay cells had been respectively concluded as $t_{unit\_cell\_(a)}^{delay\_\min}$ and $t_{unit\_cell\_(b)}^{delay\_\min}$. Substituting the two equations in (5-43), we can obtain the maximum output frequency in (5-51) for the NSOH DPWM in [5-71]. Similarly, the value for the NSOH DPWM in [5-29] [5-30] is given in (5-52).

$$f_{\max\_frequency\_ideal}^{NSOH\_(a)} = \frac{1}{3\times 2^{(R+g)}\times t_{FO-4}^{worst-case}} \tag{5-51}$$

$$f_{\max\_frequency\_ideal}^{NSOH\_(b)} = \frac{1}{2^{R}\times (g+3.5)\times t_{FO-4}^{worst-case}} \tag{5-52}$$

Therefore, if g is increased to improve the range of the programmable frequency, the maximum output frequency will drop as shown in (5-51) and (5-52).

5.5.4.3 MSF analysis

For the case of a 9-bit hardware resolution and the AMI06 process, if we assume that $g=2$, we can derive the value of the maximum output frequency of the NOSH DPWM as 646 KHz for the delay cell in [5-71] and 1.41 MHz for the delay cell in [5-30]. As

both $f_{\max\_frequency\_ideal}^{NSOH\_(a)}$ and $f_{\max\_frequency\_ideal}^{NSOH\_(b)}$ in the 9-bit NSOH DPWM are less than 10 MHz when g=2, from discussion in subsection 5.3.2, we would conclude that MSF of a digital DC-DC converter with the 9-bit NSOH DPWM (2-bit programmability) will be equal to the maximum output frequency of the NSOH DPWM.

For the NSOH in [5-71], the aforementioned conclusion exists when $R+g \geq 7.05$. For the NSOH in [5-30], the same conclusion exists when $R+\log_2(g+4) \geq 8.63$. Thus, a complete equation to describe the MSF in a digital DC-DC converter with the NSOH DPWM in [5-71] and the AMI06 technology will be in (5-53). A complete equation to describe the MSF in a digital DC-DC converter with the NSOH DPWM in [5-30] and AMI06 technology is given by (5-54).

$$MSF^{NSOH\_(a)} = \begin{cases} = \dfrac{1}{3\times 2^{(R+g)}\times t_{FO-4}^{worst-case}}\ Hz & when\ (R+g) \geq 7 \\ > 10\ MHz & when\ (R+g) < 7 \end{cases} \tag{5-53}$$

$$MSF^{NSOH\_(b)} = \begin{cases} = \dfrac{1}{2^{R}\times (g+2)\times t_{FO-4}^{worst-case}}\ Hz & when\ (R+\log_2(g+2)) \geq 9 \\ > 10\ MHz & when\ (R+\log_2(g+2)) < 9 \end{cases} \tag{5-54}$$

To test the feasibility of the proposed equation in (5-51) and (5-52), I will list the MSF value reported in [5-56] [5-71] [5-30] and compare them with a predicted value from (5-51) or (5-52).

Case 1): Chip implementation, m=2, k=5, R=7, g=1, 0.35μm CMOS process, delay cell [5-56].

The reported MSF is 10 MHz in simulation. From (5-51), we conclude that the MSF will be 8.86 MHz. Thus, the reported 10 MHz is an aggressive value and might be only available in simulation.

Case 2): FPGA implementation, m=5, k=5, R=10, g=1, Xilinx Virtex IV, delay cell [5-71].

The reported MSF is 781 KHz from a test. From (5-51), we conclude that the MSF will be 4.35 MHz for $0.09\mu m$ gate length. Thus, the reported 781 KHz is a reasonable value.

Case 3): Chip implementation, m=0, k=4, R=4, g=4, $0.18\mu m$ CMOS process, delay cell [5-30].

The reported MSF is 16 MHz in test and 150 MHz in simulation. From (5-52), we conclude that the MSF would be 110.23 MHz. Thus, the reported 16 MHz is a reasonable value, and that 150 MHz is an aggressive value and is only available in simulation.

5.5.4.4 Relative Matching Error

The matching between the fine and the coarse resolution is a big issue in the NSOH DPWM. In an ideal case, there is no delay offset and the relative matching error due to digital programming will be 0.5. However, the delay offset changes the result. The associated relative matching error δ can be derived in (5-55) for the delay cell in Figure 5-26 (a) and in (5-56) for the delay cell in Figure 5-26 (b).

$$\delta^{NSOH\_(a)} = \frac{\frac{t_{element}^{delay}}{2}}{t_{unit\_cell}^{delay}} = \frac{1}{2\times\left[1+\frac{3\times 2^{(g-2)}}{N}\right]} \tag{5-55}$$

$$\delta^{NSOH\_(b)} = \frac{\frac{t_{element}^{delay}}{2}}{t_{unit\_cell}^{delay}} = \frac{1}{2\times\left[1+\frac{(g+3)}{(g+1)\times N}\right]} \tag{5-56}$$

From (5-55) and (5-56), we observe that the relative matching error will be decreased by the delay offset.

5.5.4.5 Frequency control

In the NSOH DPWM, both the phase control and frequency control are needed. The phase control is implemented with DLL to digitally program the delay time of a unit delay cell so that the difference between the total delay time and the period of the counter clock can be minimized. Two kind of specific DLLs [5-30, 5-71] had been developed for the DPWM. The frequency control is simple in implementation.

5.5.4.6 Power dissipation

In comparison with the SOH DPWM in Subsection 5.5.3, there may be a significant saving in power dissipation, thanks to the fact that all delay cells in the delay chain are oscillating in the switching frequency but not in the counter clock frequency. However, from Table 5-2, Table 5-3 and Figure 5-11, we can recognize that the power dissipation in the NSOH might not be good if the delay cell's digital programming bits g are larger than 4. If we use the unit power dissipation scale $Power_{unit}$, the dynamic power dissipation in all of the unit delay cells in [5-71] can be approximately estimated by (5-57).

$$Power_{cells}^{NSOH\_(a)} = \left(2^{k}-1\right)\times\left[2^{2g}\times\eta_{2-Nor}+\left(2^{g}+1\right)\times\eta_{2^{g}-Nand}\right]\times Power_{unit} \tag{5-57}$$

where η_{2-Nor} is the normalized power dissipation of a 2-Not gate to an inverter and $\eta_{2^{g}-Nand}$ is the normalized power dissipation of a 2^{g}-Nand gate to an inverter.

In the Table 5-6, I conclude $\eta_{2-Nor}=4$ and $\eta_{2^{g}-Nand}=4\times 2^{g}$.

The power dissipation analysis for [5-30] is complex and heavily depends on the detailed circuit design. The unit power dissipation scale $Power_{unit}$ may not be a good tool because the static power dissipation is no longer negligible. According to the discussion in [5-36] and [5-30], the delay cell in [5-30] is typically power hungry.

5.6 Choke relaxed SOH DPWM

In section 5.5, I discussed performance of four major DPWM architectures. Though the NSOH DPWM does not have the choke effect addressed in the SOH DPWM and significantly decreases the toggling frequency in the delay chain, its phase control and the digitally programmed delay cells introduce four other issues. The first one is a significant delay offset in each delay cell discussed in subsection 5.5.41; the second one is the relative matching error discussed in subsection 5.5.4.4; the third one is the tradeoff between the MSF and the frequency regulation range discussed in subsection 5.5.4.2; the forth is the significant silicon area occupied and power dissipation brought by a complicated digitally programmed delay cell.

5.6.1 Choke relaxed SOH DPWM

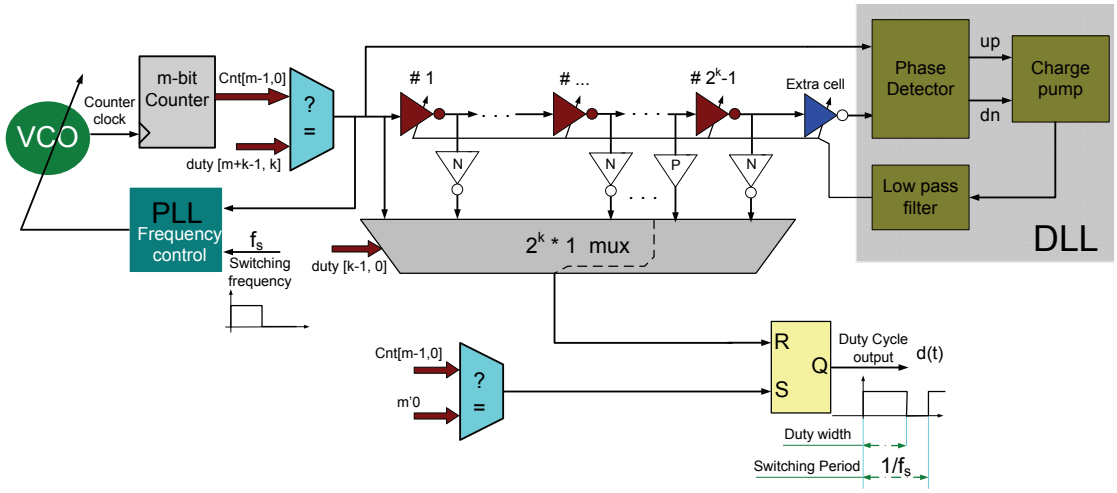


Figure 5-12. A DPWM with continuously regulated delay line

One idea to improve the SOH DPWM is to use a charge pump based DLL [5-25] and a current starved inverter as the delay cell so that the delay time of the delay cells can be continuously regulated. If the idea is applicable, we can overcome the aforementioned issues in the NSOH DPWM without scarifying its advantages. On the basis of the idea, a SOH DPWM architecture is outlined in Figure 5-12.

When designing a DLL for the DPWM, the following considerations are necessary. One specification in Figure 5-12 is that the total delay in the delay line should be regulated be $1/2^m$ times of the toggling signal's period. Another is that the number of the delay cells in the delay chain is a constant value equaling 2^k and the signal for the phase comparison is always the delay chain's last stage output. The third is that the DLL should have a wide-range frequency tracking capacity to work through PVT variations. The three specifications are excluded in most current DLL designs, for example, the conventional DLL [5-37], the phase shading based digital DLL [5-16] [5-10], and Dual-loop DLL [5-51].

The analog DLL in [5-37] may be a feasible solution. We assume that the "DC" in [5-37] represents the delay line in Figure 5-12, the "ICLK" and "QCLK" are respectively the input and output signal of the delay line. The charge pump will be intentionally designed with different pull down and pull up currents. Here, the pull up current I_p is designed to be $\left(2^{m-1}-1\right)$ times larger than the pull down current I_n. The asymmetric charge pump determines that its input signal V_X will have a $1/2^{m-1}$ duty ratio in steady state so that the total delay time of the delay line will approach $1/2^m$ of the cycle period.

The SOH DPWM in Figure 5-12 still has two factors to improve. The first is that there is one PLL frequency controller and one DLL phase controller in the architecture, so the architecture is not compact. The second is that the phase control would bring in the relative matching error which is directly dependent on the duty cycle accuracy of V_X. If we want to maintain a low relative matching error through PVT variation and a wide range frequency regulation, the analog design difficulty will be significant.

Based on the aforementioned considerations, we proposed an optimized solution [5-62] [5-63] – Choke Relaxed SOH (CR-SOH) DPWM - illustrated in Figure 5-13.

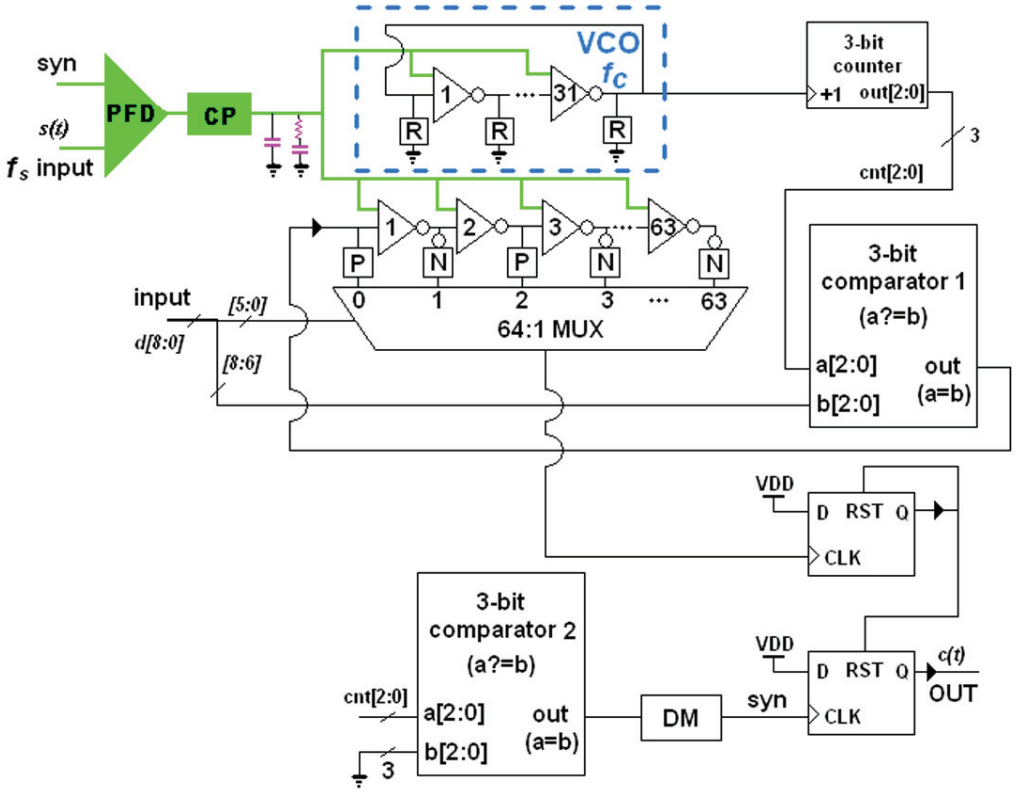


Figure 5-13. Choke-relaxed SOH DPWM architecture [5-62] [5-63]

The abbreviations in Figure 5-13 are explained as follows: “PFD” denotes a phase frequency detector; “DM” denotes a delay match block; “CP” denotes a charge pump; “R” denotes a replica block; “P” and “N” respectively denotes a non-inverting type and an inverting type buffer block and the two blocks are designed to have the same propagation delay; “syn” denotes the signal utilized to accomplish frequency compare and implement switching frequency control; “d[8:0]” denotes the 9-bit digital signal of the duty cycle which is the input signal of the DPWM; “s(t)” denotes another input of the

DPWM, which is an external systematic clock signal toggling at a desired switching frequency to realize frequency synchronization and the consequent single-clock operation in a digital DC-DC converter as discussed in subsection 5.5.1.3; “c(t)” is the output signal of the DPWM; “RST” denotes the reset terminal of a Flip-Flop.

The CR-SOH DPWM integrates the advantages of both the architecture in Figure 5-10 and the architecture in Figure 5-12. In similar to the architecture in Figure 5-10, the CR-SOH only needs one PLL to realize frequency control. Thus, we do not need to implement a wide-range frequency tracking DLL. As a result, the architecture and design are greatly simplified, and silicon area and power dissipation can be also obviously reduced. At the same time, similar to the architecture in Figure 5-12, the CR-SOH effectively relaxes the choke effect in the SOH DPWM and uses a current starved inverter as the delay cell so that the maximum output frequency of the DPWM can be obviously improved. Furthermore, as all of the delay cells in the delay chain will be toggling at the switching frequency and a large number of delay compensation cells are eliminated, we can obtain additional significant silicon area and power dissipation reduction.

5.6.2 Counter clock frequency

There is a VCO in the CR-SOH DPWM to generate a counter clock - the input of an m-bit counter. The VCO consists of $2^{(k-1)}-1$ cascaded current starved inverter in a closed loop and the biasing voltage of the inverters is set up by the “CP” charge pump with a charging or discharging operation depending on the output of the “PFD” – phase frequency detector. The two input signals of the “PFD” are the external systematic clock “s(t)” and “syn”, where “syn” is an intentionally delayed output of an m-bit digital comparator which will determine the rising edge of “c(t)”. The intentional delay is implemented by the “DM” – delay match block and can minimize the phase offset between “c(t)” and “s(t)” due to the gate propagation delay. The m-bit digital comparator

has two inputs, one of which is the output of an m-bit counter and another one is an m-bit zero.

On the basis of the aforementioned description, we recognize that the counter clock frequency will satisfy (5-58).

$$f_{clock}^{CR\_SOH} = 2^m \times f_S \tag{5-58}$$

Where $f_{clock}^{CR\_SOH}$ and f_S respectively denote the counter clock frequency and the desired switching frequency.

The counter clock frequency $f_{clock}^{CR\_SOH}$ will be determined by the $2^{(k-1)}-1$ series connected current starved inverters in the VCO closed loop as that in (5-59) and its maximum value $f_{clock\_\max}^{CR\_SOH}$ is in (5-60).

$$f_{clock}^{CR\_SOH} = \frac{1}{2\times\left[2^{(k-1)}-1\right]\times t_{unit-cell}^{delay\_INV}} = \frac{1}{\left[2^k-2\right]\times t_{unit-cell}^{delay\_INV}} \tag{5-59}$$

where $t_{unit-cell}^{delay\_INV}$ denotes the delay time of one inverter type delay cell.

$$f_{clock\_\max\_ideal}^{CR\_SOH} = \frac{1}{\left[2^k-2\right]\times t_{FO-4}^{worst-case}} \tag{5-60}$$

where the inverter's minimal delay time is approximately estimated as $t_{FO-4}^{worst-case}$.

5.6.3 Maximum output frequency

From (5-60), we can conclude that when the counter is an ideal component, the maximum output frequency in the CR-SOH DPWM can be calculated with (5-61).

$$f_{\max\_frequency\_ideal}^{CR\_SOH} = \frac{1}{\left[2^R - 2^{m+1}\right] \times t_{FO-4}^{worst-case}} \tag{5-61}$$

On recognition that f_{clock}^{syn} in (5-12) is the maximum clock frequency acceptable to the m-bit counter, a complete equation can be derived in (5-62) to calculate the maximum counter clock frequency $f_{clock\_\max}^{CR\_SOH}$ available in the CR-SOH DPWM.

$$f_{clock\_\max}^{CR\_SOH} = \min\left(\frac{1}{\left[2^k - 2\right] \times t_{FO-4}^{worst-case}}, \frac{1}{\alpha \times t_{FO-4}^{worst-case}} \right) \tag{5-62}$$

Based on (5-62), the maximum output frequency $f_{\max\_frequency}^{CR\_SOH}$ in the CR-SOH DPWM can be calculated with (5-63).

$$f_{\max\_frequency}^{CR\_SOH} = \min\left(\frac{1}{\left[2^R - 2^{m+1}\right] \times t_{FO-4}^{worst-case}}, \frac{1}{2^m \times \alpha \times t_{FO-4}^{worst-case}} \right) \tag{5-63}$$

5.6.4 Choke effect and choke region

After calculating out the values of $f_{\max\_frequency\_ideal}^{CR\_SOH}$ for different set of m and k, and plotting them with light blue triangles, we will get Figure 5-31 on the basis of Figure 5-24. For the synchronous counter, i.e., $\alpha = 20$, with (5-61) we can outline the maximum output frequency curve of the CR-SOH DPWM in Figure 5-31 with a blue dashed line. The blue dashed line is the bottom line of three curves.

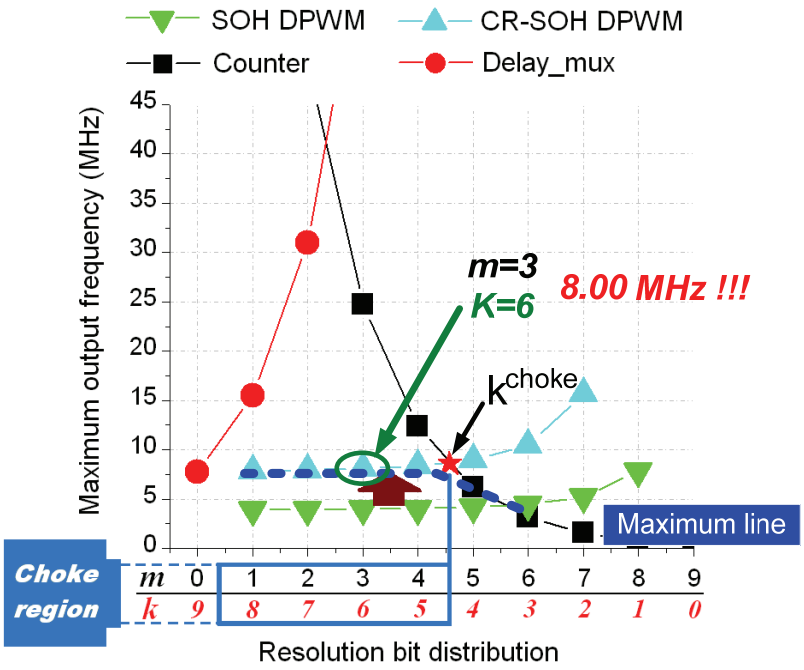


Figure 5-14. Relaxed choke effect in the CR-SOH DPWM [5-63]

From Figure 5-14, we notice that the CR-SOH DPWM has four different operation modes and the choke effect characters similar to the SOH DPWM. For the CR-SOH DPWM, the "start point" of the choke effect is the intersection point of the light blue triangle curve and the black rectangle curve and is highlighted with a red star.

In comparison Figure 5-14 with Figure 5-11, we notice two changes. The first change lies in that the maximum line of the CR-SOH DPWM in the choke region is around 100% higher than that of SOH-DPWM. In the example case that m=3 and k=6, the maximum output frequency is 8.00 MHz which is around double the value of 3.94 MHz in the SOH DPWM. The second change lies in that the "start point" of the choke effect is moved towards left by one bit so that the length of choke region is decreased by one bit. Therefore, CR-SOH DPWM has a relaxed choke effect in comparison with SOH DPWM.

The "start point" of the choke region $k^{relaxed\_choke}$ can be calculated with (5-64) and the length of the choke region $Lengh^{relaxed\_choke}$ is given in (5-65).

$$k^{relaxed\_choke} = \log_2(\alpha + 2) \tag{5-64}$$

$$Lengh^{relaxed\_choke} = R - k^{relaxed\_choke} - 1 \tag{5-65}$$

For a 9-bit resolution DPWM with the synchronous counter, from (5-64) and (5-65) we can obtain $k^{relaxed\_choke} = 4.46$ and $Lengh^{relaxed\_choke} = 3.54$ as shown in Figure 5-14.

5.6.5 MSF analysis

From Figure 5-14, we observe that the maximum output frequency is still smaller than 10 MHz no matter how we distribute m and k. The peak value is 8.27 MHz which happens when m=4 and k=5. As $f_{\max\_frequency}^{CR\_SOH}$ in the 9-bit DPWM is less than 10 MHz, following the discussion in subsection 5.3.2, we can conclude that MSF of a digital DC-DC converter with the 9-bit CR-SOH DPWM is limited being the maximum output frequency of DPWM $f_{\max\_frequency}^{CR\_SOH}$. This conclusion exists for all sets of m and k combination when $R \geq 9$, i.e., a high hardware resolution DPWM. Thus, a complete equation to describe the MSF in a digital DC-DC converter with the CR-SOH DPWM and AMI06 technology will be given by (5-66).

$$MSF^{CR\_SOH} = \frac{f_{clock\_\max}^{CR\_SOH}}{2^m} \tag{5-66}$$

$$= \begin{cases} \min\left(\dfrac{1}{\left(2^R - 2^{m+1}\right) \times t_{FO-4}^{worst-case}}, \dfrac{1}{2^m \times \alpha \times t_{FO-4}^{worst-case}}\right) Hz & when\ R \geq 9 \\ > 10\ MHz & when\ R < 9 \end{cases}$$

5.6.6 Relative matching error

The inverter in the delay chain is identical to the inverter in the VCO and both of the inverters will be regulated by the same PLL or the output voltage of the charge pump. Thus, the delay time of the inverters in the delay chain will be identical to that of the inverter in the VCO.

The delay time of the inverter will determine the finest resolution time of the CR-SOH DPWM. Let us analyze the total delay time in the delay chain in Figure 5-13. For the DPWM having k-bit Delay_mux hardware resolution, there will be $2^k - 1$ series connected current starved inverters in the delay chain. Thus, the total delay time available in the delay chain $t_{delay\_chain}^{total\_delay}$ is $2^k - 1$ times of the delay time of one inverter as that given in (5-67).

$$t_{delay\_chain}^{total\_delay} = \left(2^k - 1\right) \times t_{unit-cell}^{delay\_INV} \tag{5-67}$$

Comparing (5-67) with (5-59), we find that the former is one finest resolution timestep larger than the latter, which violates the desire for a hybrid DPWM as we discussed in the subsection 5.5.3.4, i.e., the former should be one finest resolution timestep smaller than the latter. However, the violation does not imply the existence of relative matching error in the CR-SOH DPWM. If we notice that the inverter in the delay chain is identical to the inverter in the VCO, we recognize that the signal at the output of the #62 inverter in the delay chain is exactly one counter clock period later than the input signal of the delay chain. Thus, we do not need the last two inverters in the delay chain and the last two terminals of the 64:1 mux can be left floating. After the simple process, a general CR-SOH DPWM is illustrated in Figure 5-15, which will satisfy the desire for a hybrid DPWM discussed in the subsection 5.5.3.4.

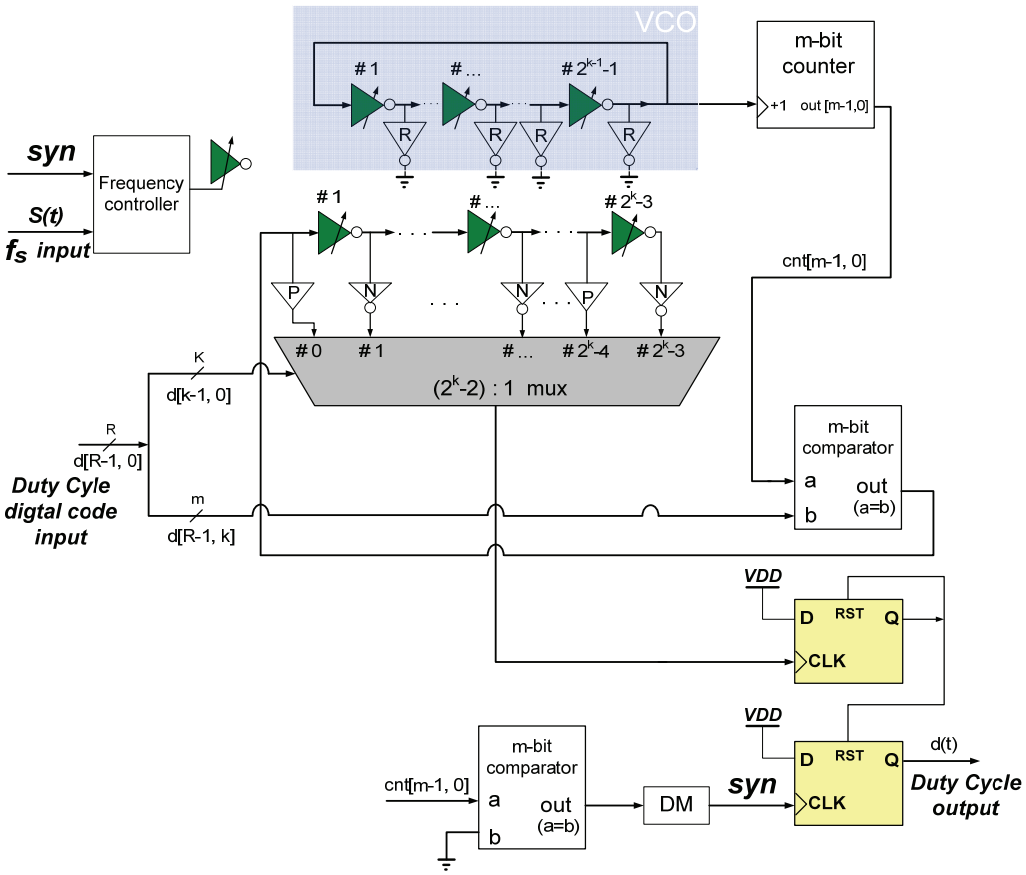


Figure 5-15. A general CR-SOH DPWM architecture

Thus, in similar to the SOH DPWM, the CR-SOH DPWM guarantees a seamless transition between the Delay_mux fine resolution and the Counter coarse resolution.

5.6.7 Effective delay_mux hard resolution

From subsection 5.6.6 and Figure 5-15, we notice that the multiplexer utilized in the CR-SOH DPWM is not a $\left(2^k\right):1$ mux but in fact a $\left(2^k-2\right):1$ mux. The fact implies that

the effective Delay_mux hardware resolution $k_{effective}^{CR-SOH}$ in the CR-SOH DPWM does not exactly equal k and is a value a little bit smaller than k as that given in (5-68).

$$k_{effective}^{CR-SOH} = \log_2\left(2^k - 2\right) \tag{5-68}$$

A similar phenomenon exists in Figure 5-21, where $k_{effective}^{SOH\_INV} = \log_2\left(2^k - 1\right)$.

5.6.8 Frequency control

Frequency control is not an issue in the CR-SOH DPWM. The PLL illustrated in Figure 5-15 can simultaneously adjust the counter clock frequency in the VCO and the delay time in the delay chain. As there is no relative matching error in the CR-SOH DPWM as discussed in the subsection 5.6.6, the CR-SOH DPWM only needs one set of PLL so it has a very compact silicon implementation.

5.6.9 Power dissipation

In Figure 5-15, we notice that all of the delay cells in the delay chain are toggling with the DPWM output frequency and the cells in the VCO are toggling at counter clock frequency.

If we follow the way we did for the SOH DPWM in subsection 5.5.3.6, the total dynamic power dissipation for all of the unit delay cells and VCO cells in Figure 5-15 can be approximately calculated by (5-69).

$$Power_{cells}^{CR\_SOH} = \left[2^m \times \left(2^{k-1} - 1\right) + \left(2^k - 1\right)\right] \times Power_{unit} \tag{5-69}$$

In comparison with (5-40), we notice that $Power_{cells}^{SOH\_INV} \approx 2^k \times Power_{cells}^{CR\_SOH}$. Thus, the CR-SOH has significant advantage in power savings. If m=3 and k=6, a specific value of $Power_{cells}^{CR\_SOH}$ is calculated in (5-70) and the relationship between $Power_{cells}^{CR\_SOH}$ and $Power_{cells}^{SOH\_INV}$ is given in (5-71). If we compare the CR-SOH DPWM with the Flip-Flop based SOH DPWM [5-41], we will get (5-72).

$$Power_{cells}^{CR\_SOH} = 279 \times Power_{unit} \tag{5-70}$$

$$Power_{cells}^{SOH\_INV} = 59.61 \times Power_{cells}^{CR\_SOH} \tag{5-71}$$

$$Power_{cells}^{SOH\_FF} = 1.8 \times \eta_{FF} \times Power_{cells}^{CR\_SOH} \tag{5-72}$$

where η_{FF} is a value to scale the Flip-Flop dynamic power with inverter dynamic power.

5.7 Silicon implementation

When we implement the CR-SOH DPWM in Figure 5-13, we select m=3 and k=6. In this subsection, I will introduce several important function blocks' schematics and the die micrograph of the CR-SOH DPWM. There is no novel or specific circuit design in the implementation and most of the function blocks are standard logic gates.

The semiconductor process technology utilized in the design and layout is $0.6\mu m$ AMI06 which has three metal layers, two poly-silicon layers and one high resistance layer. We only used two metal layers in layout.

The chip was fabricated in MOSIS educational program using SCN3ME_SUMB technology and is ceramic DIP-40 packaged.

5.7.1 Top level schematic and die micrograph

The top level schematic of the CR-SOH DPWM was built in the Cadence 2005 environment and is shown in Figure 5-16. The top level layout, the DIP-40 package pad connection and the fabricated die micrograph are respectively shown in Figure 5-17, Figure 5-18 and Figure 5-19. The actual die size of the chip is 0.85*0.83 mm^2.

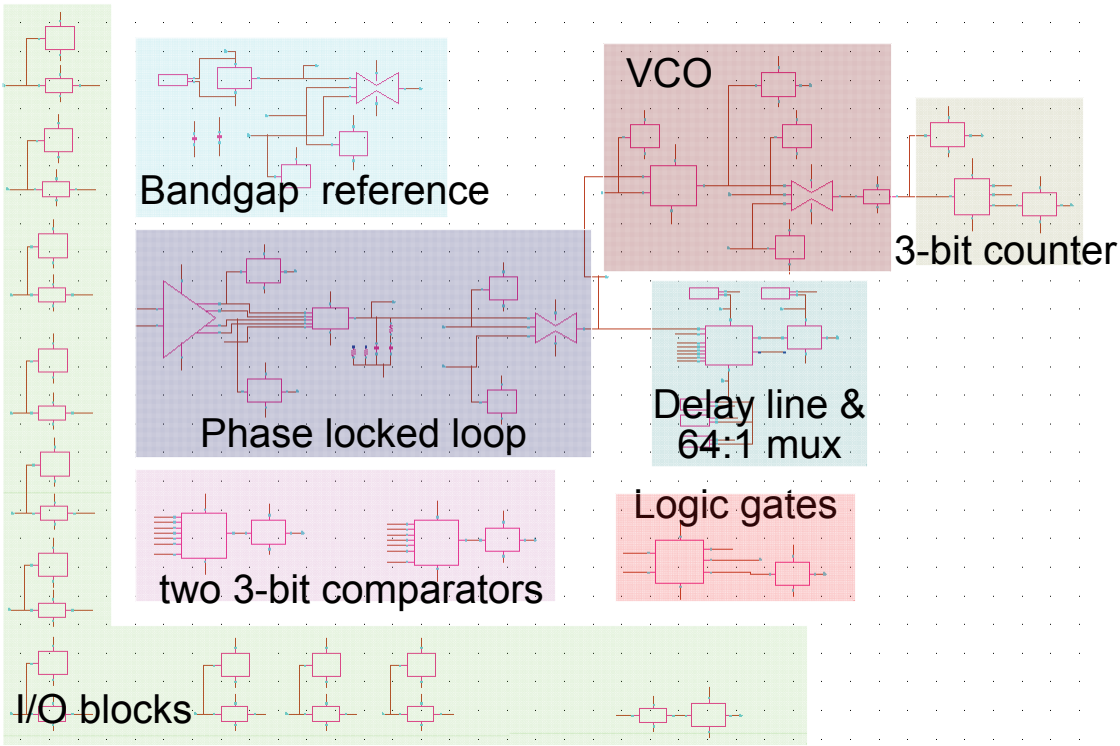


Figure 5-16 Top level schematic in Cadence (m=3, k=6)

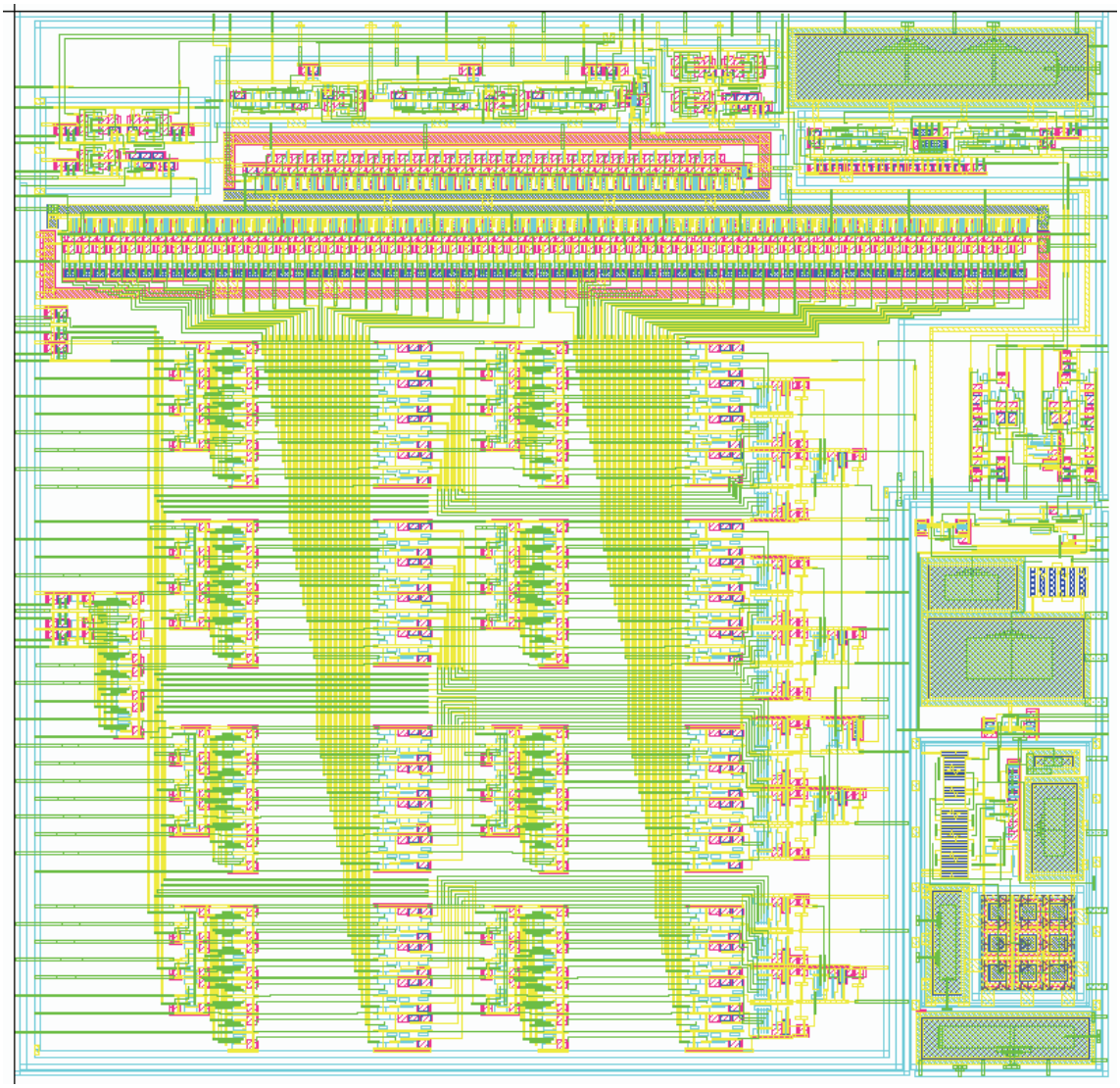


Figure 5-17. Top level layout of the CR-SOH DPWM (m=3, k=6)

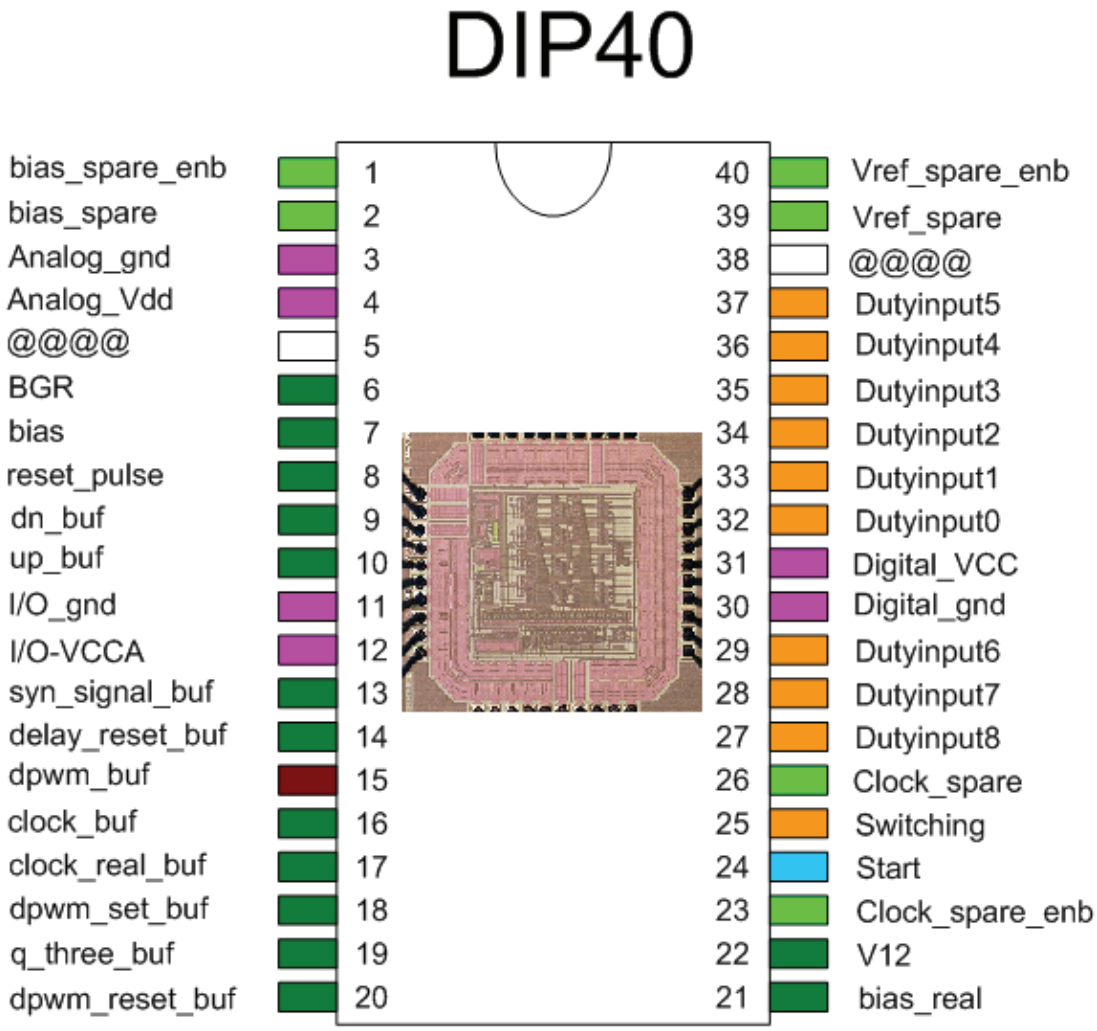


Figure 5-18. DIP40 package pad connection guide

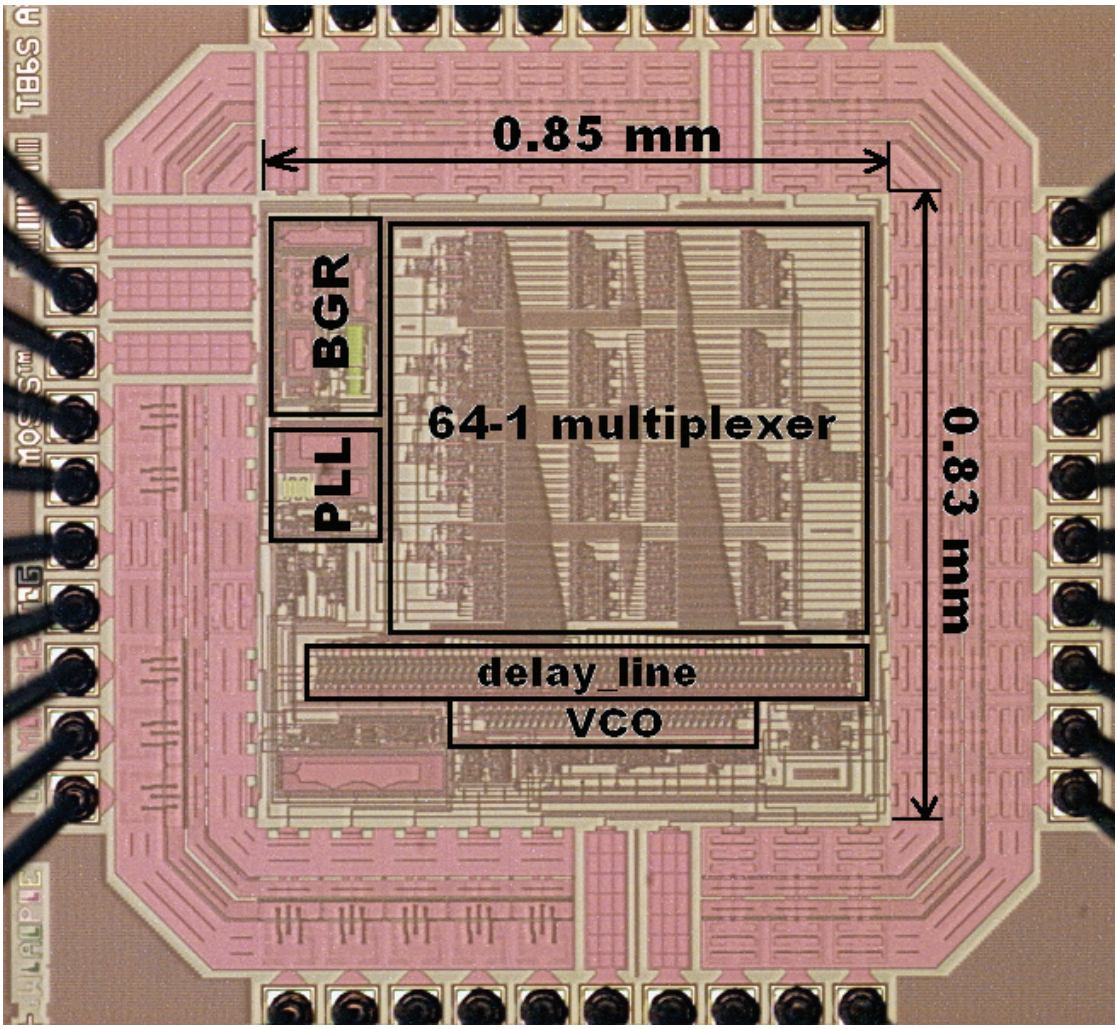


Figure 5-19. Die micrograph of the CR-SOH DPWM (m=3, k=6)

"BGR" in Figure 5-19 denotes Bandgap reference. The logic gates, 3-bit counter, I/O blocks and two 3-bit comparators are not outlined in Figure 5-19.

Because only two metal layers were used in the layout, the silicon area of the 64:1 multiplexer (mux) appears dominant.

5.7.2 Current starved delay cell

For the convenience of exploring the maximum output frequency in the CR-SOH DPWM, one kind of current starved inverter shown in Figure 5-20 is selected as the delay cell to constitute the VCO and the delay line in Figure 5-16.

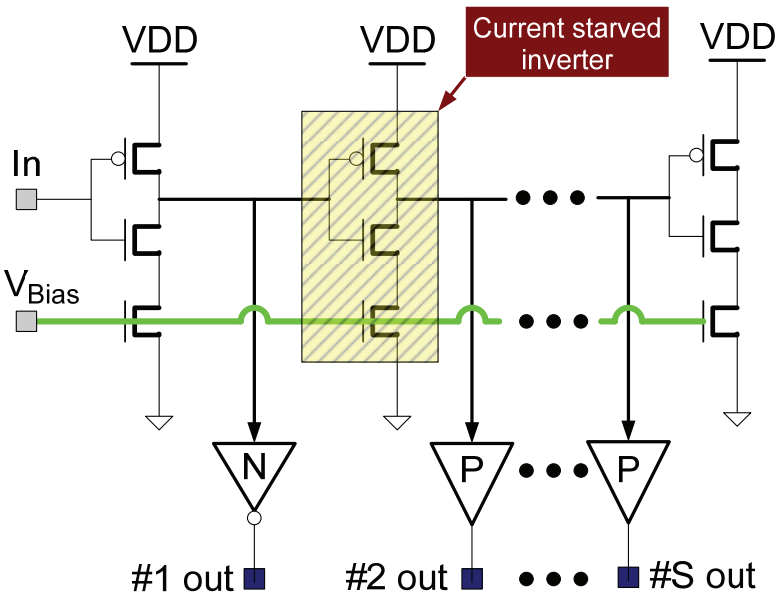


Figure 5-20. Current starved inverter type delay cell

Two kinds of buffers alternatively connect the output nodes of the cascaded connected current starved inverters to the output terminals, which are the inverting type buffer "N" and non-inverting type buffer "P". The two buffers "P" and "N" are designed to have identical propagation time.

The relationship between the inverter's propagation delay time and the biasing voltage V_{Bias} is represented by simulation data illustrated in Figure 5-21. "FF" denotes one of process corner – fast NMOS and fast PMOS; "TT" denotes the second corner – normal

NMOS and normal PMOS; “SS” denotes the third corner – slow NMOS and slow PMOS. The environment temperature is 27° and VDD is 3.3V.

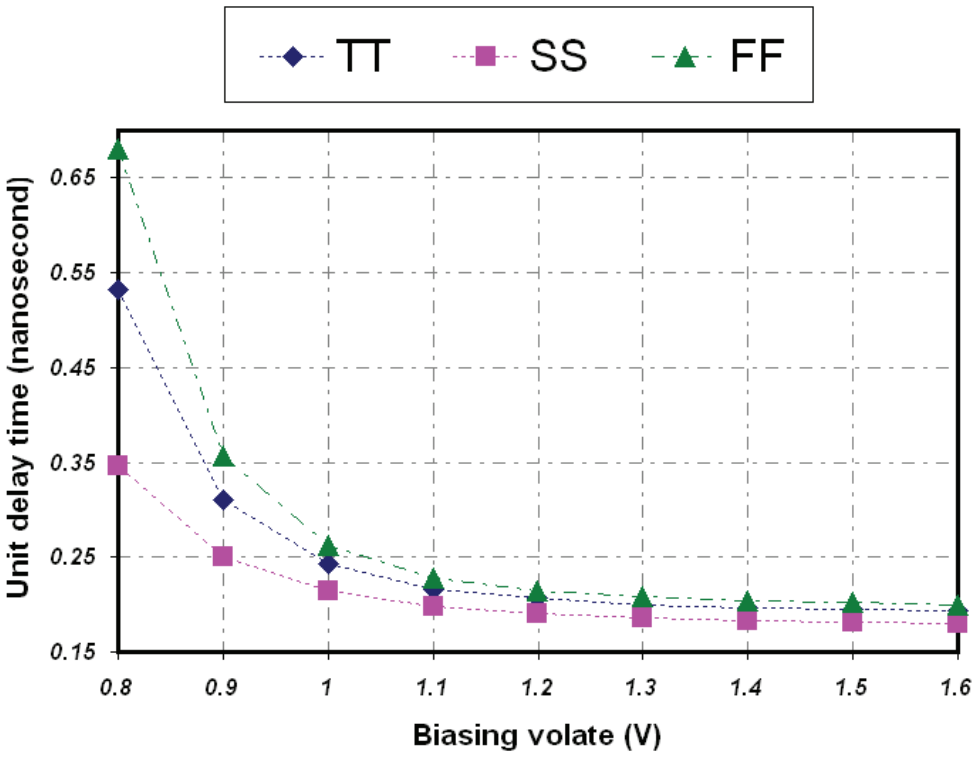


Figure 5-21. Inverter delay time regulation character

5.7.3 Synchronous counter

The synchronous counter with parallel enable selected to implement the 3-bit counter is illustrated in Figure 5-7(b).

5.7.4 Phase locked loop

The PLL includes a phase frequency detector (PFD), charge pump (CP), and low pass filter (LPF) as illustrated in Figure 5-22.

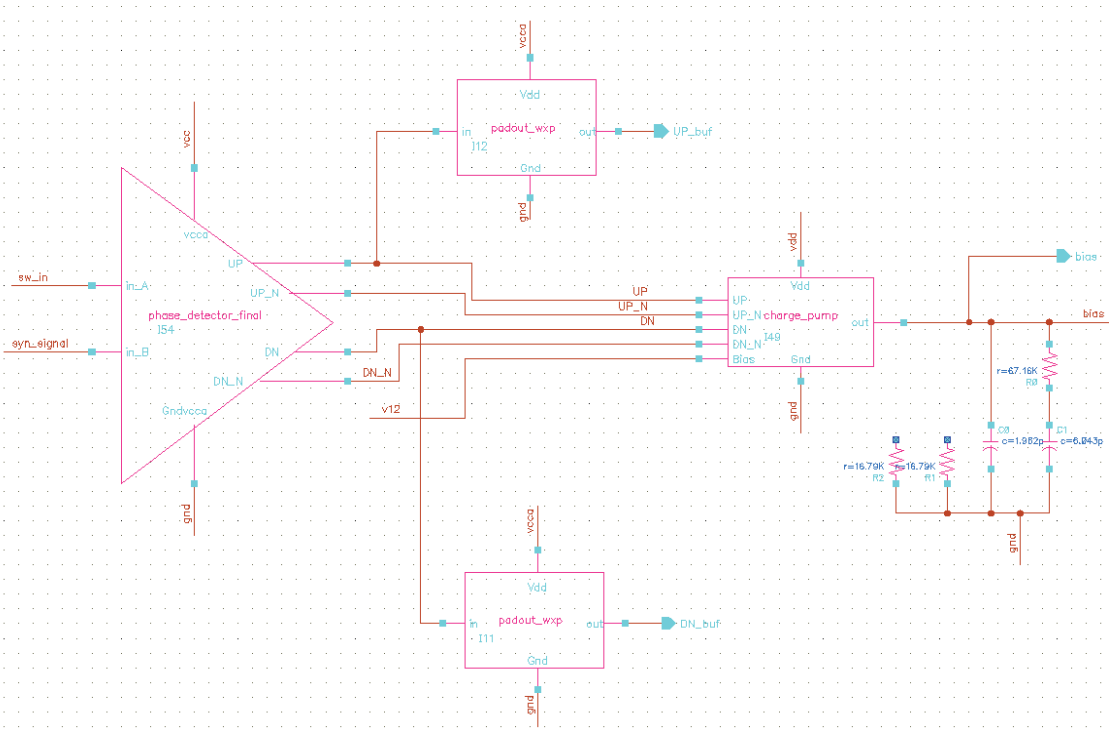


Figure 5-22. Phased locked loop schematic

5.7.4.1 Phase frequency detector

The phase frequency detector is same to the circuit in [5-57].

5.7.4.2 Charge pump

The charge pump selected is illustrated in Figure 5-23

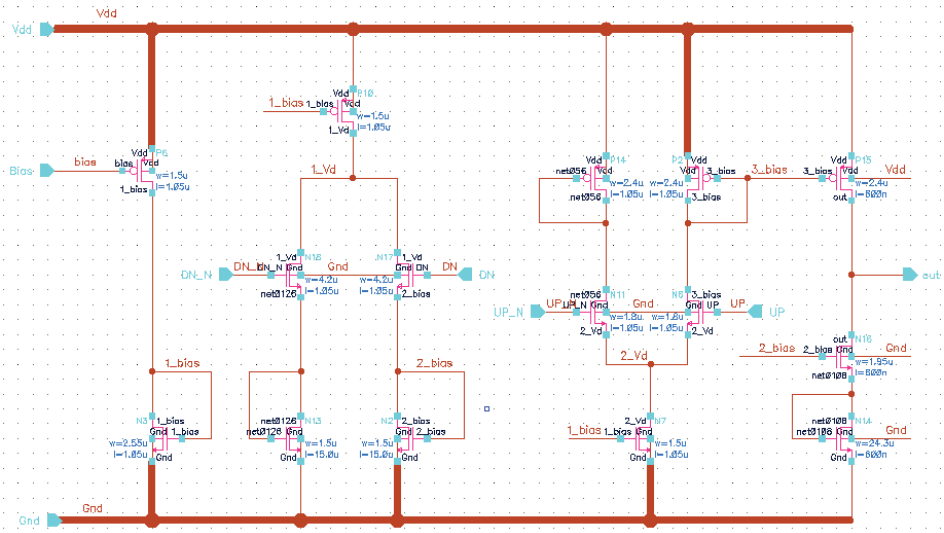


Figure 5-23. Charge pump schematic

5.7.5 64:1 multiplexer

The 64:1 mux includes one 64-Or gate, one 3-decoder, eight 3-enable-decoders, and 64 2-Nand gates. The top level schematic is shown in Figure 5-24.

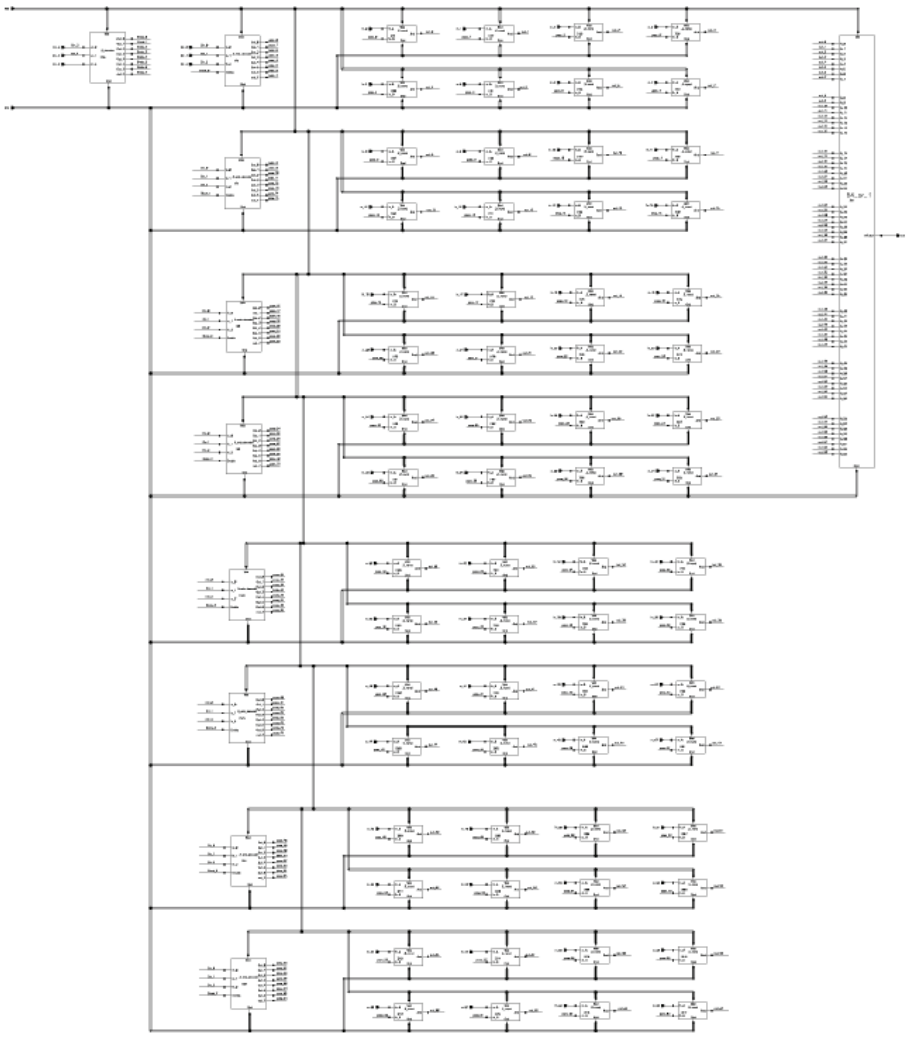


Figure 5-24. 64:1 multiplexer implementation

5.8 Performance test

As illustrated in Figure 5-1, the DPWM is a complete and independent function block in a digital DC-DC converter. Thus, its performance test does not need building up a closed loop digital DC-DC converter. Figure 5-25 presents the test architecture [5-62] for the CR-SOH DPWM chip which has a die micrograph shown in Figure 5-19.

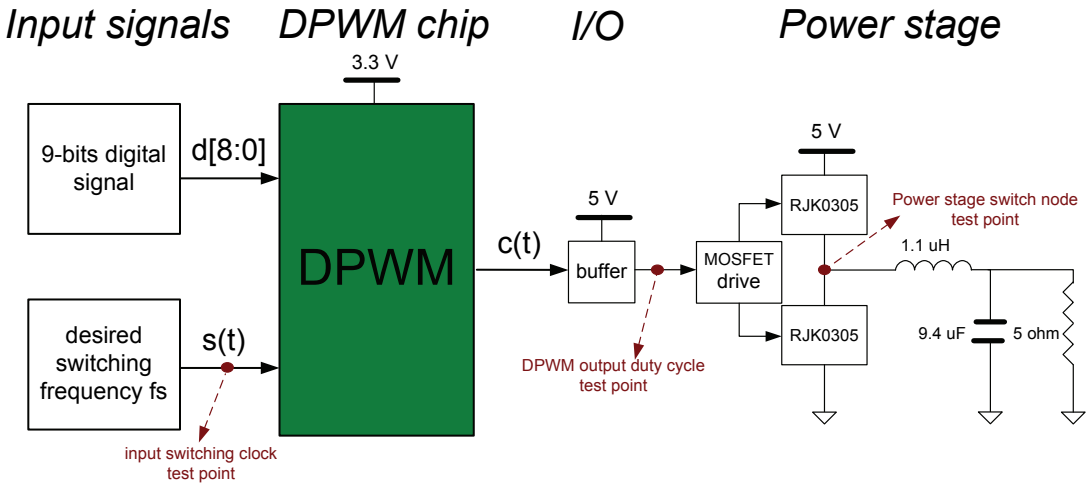


Figure 5-25. CR-SOH DPWM test architecture [5-62]

We will input a 9-bit digital code and a clock with a desired switching frequency into the chip. The output signal of the chip should be a periodic signal which frequency is identical to the input clock and which duty cycle ratio should be identical to the normalized value of the input 9-bit digital code. The output signal will be first buffered to 5 V then connected to MOSFET drive, and the driver's output will be utilized to drive power MOSFETs in a Buck DC-DC converter.

The chip performance test includes four parts. The first is the maximum output frequency and the range of frequency regulation; the second is the duty cycle input response; the third is the linearity and monotonic; and the forth is the power dissipation.

All components in Figure 5-25 will be the discrete commercial products except the CR-SOH DPWM chip and some of important components in power stage are listed in Table 5-4.

Table 5-4. Test bench power stage components

Power MOSFET	Top	1* RJK0305DPB
	Bottom	2* RJK0305DPB
Synchronous MOSFET driver	TPS28225	
Inductor	$1.1\mu H$, Two parallel LQM2HPN2R2MG0L	
Filtering capacitor	$9.4\mu F$, Two parallel GRM188F51A475ZE20D	
Load	5Ω , 5W, DALE RE60G5R00	

5.8.1 Test circuit and bench

To satisfy the test architecture in Figure 5-25 and the desired test content, a two-layer printed circuit board (PCB) was designed and fabricated. The schematic, detailed DPWM chip pad connection and the layout of the board are shown in Figure 5-26, Figure 5-27 and Figure 5-28. The fabricated PCB board with the soldered CR-SOH DPWM chip and other discrete components is shown in Figure 5-29, and the test bench ready for performance test is shown in Figure 5-30.

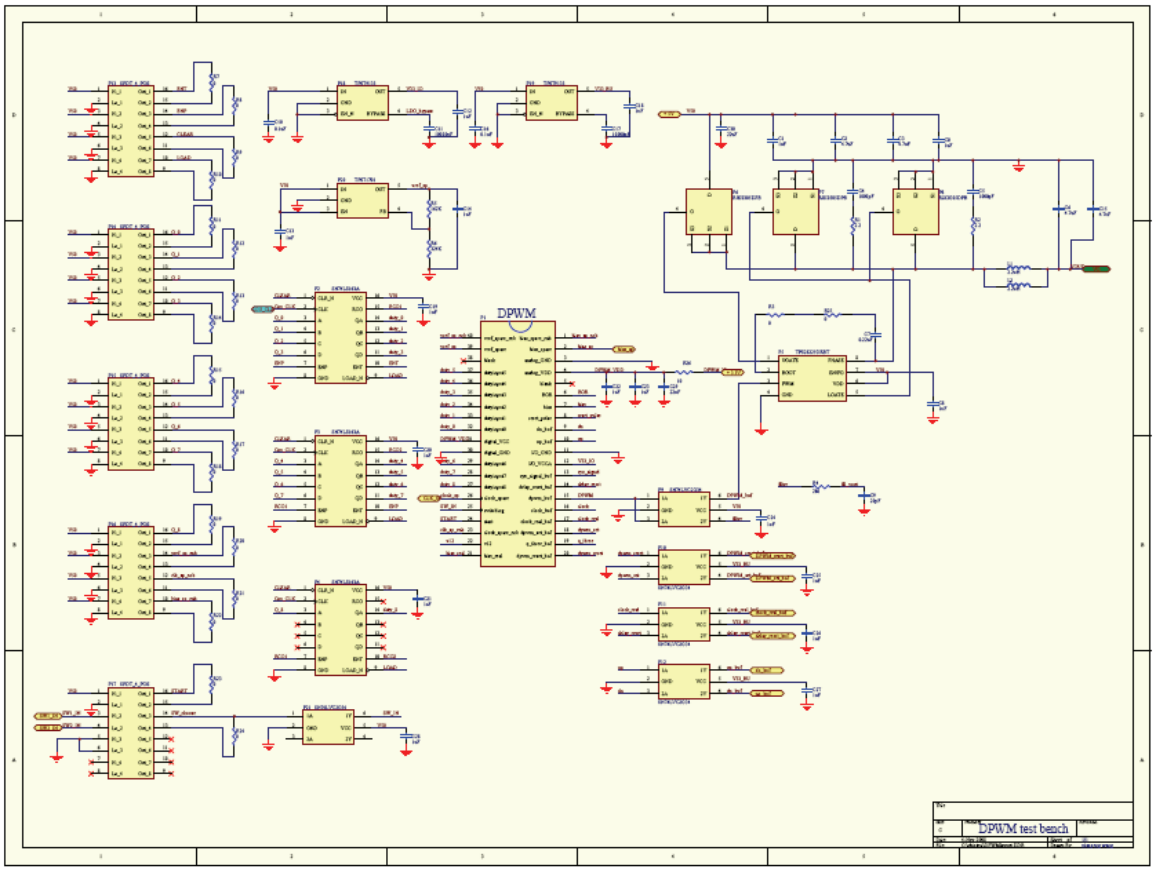


Figure 5-26. Schematic of the test bench PCB

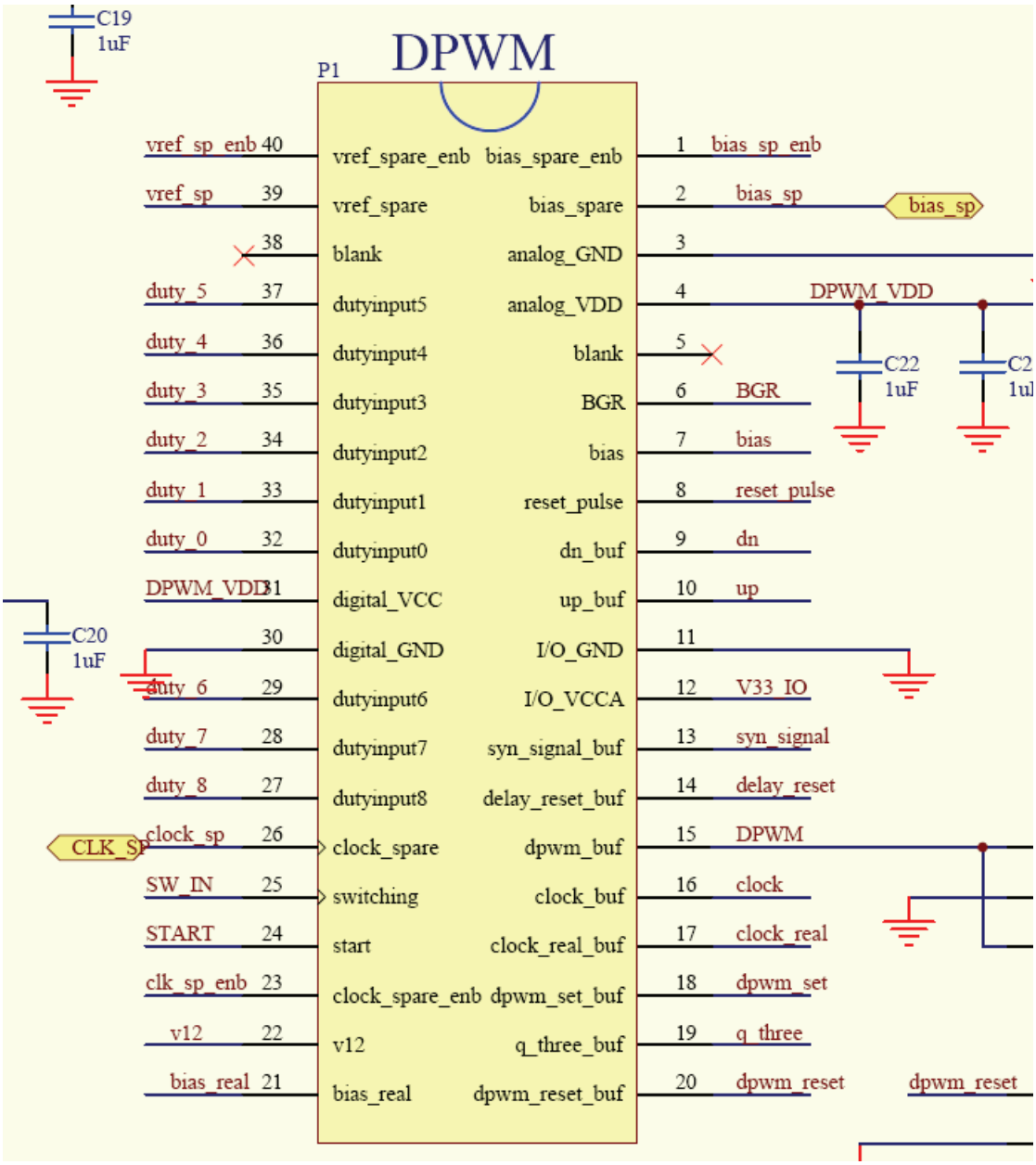


Figure 5-27. Detailed DPWM chip pad connection

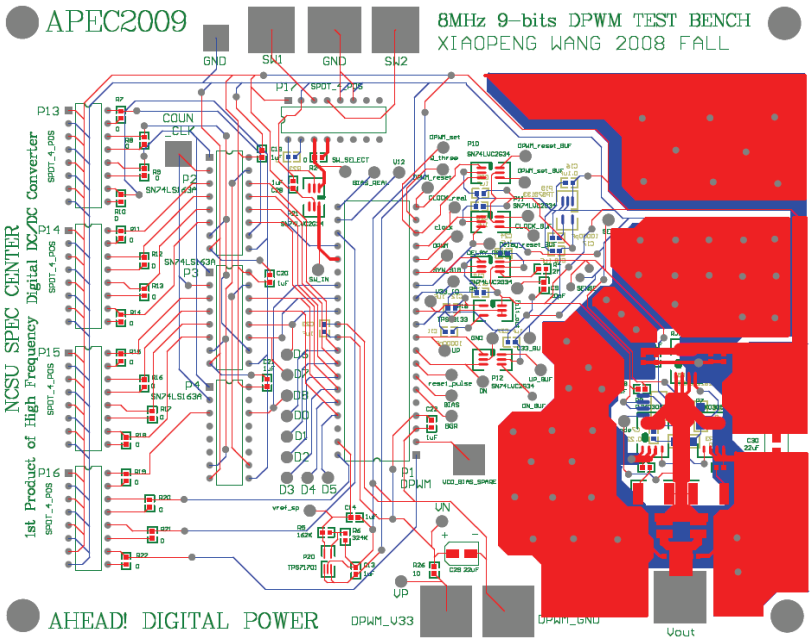


Figure 5-28. Layout of the test bench PCB

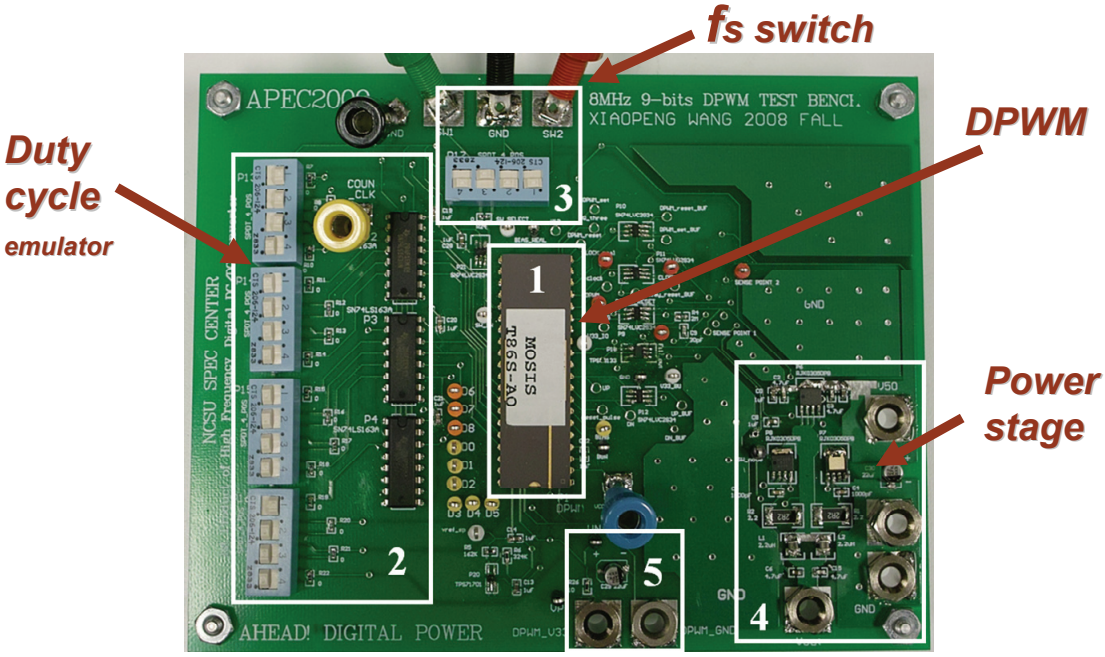


Figure 5-29. Fabricated PCB with soldered components

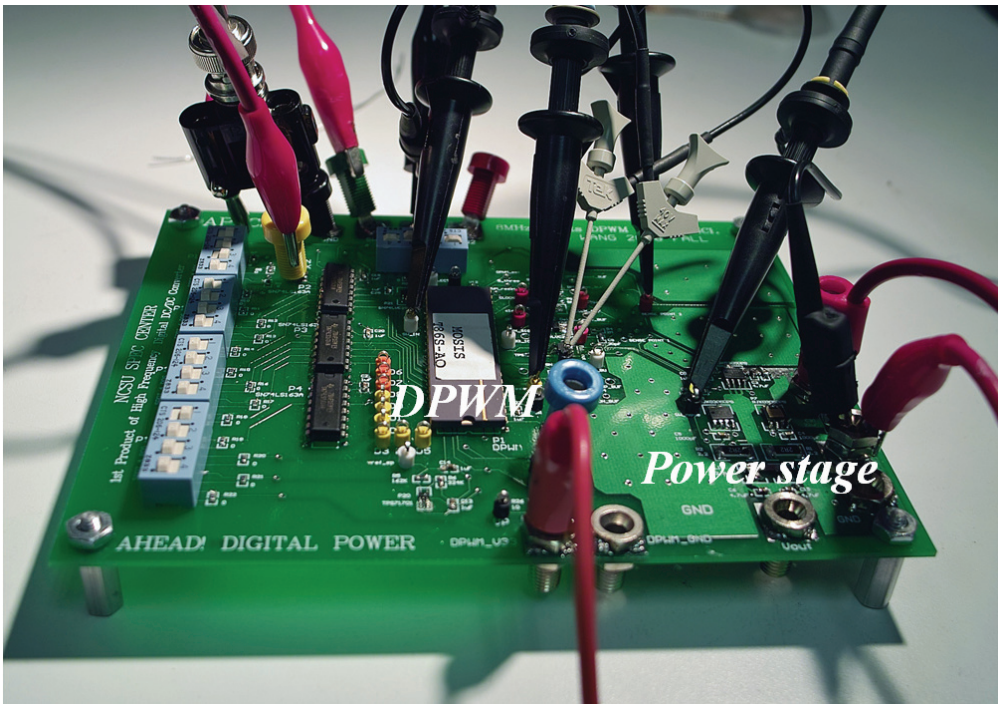


Figure 5-30. Test bench ready for test

5.8.2 Maximum and minimum output frequency

With the aid of (5-63), we can predict that the 9-bit CR-SOH DPWM's maximum output frequency will be around 8.00 MHz when m=3 and k=6.

Both the maximum frequency and the minimum frequency are tested when 9-bit duty cycle digital code is 9'h100. Figure 5-31 demonstrates that the DPWM can function well when the input frequency approaches 7.4 MHz, and we would notice that V_{Bias} is approaching its maximal value of 3.3V. Figure 5-32 demonstrates that the minimum frequency that the DPWM could function well is 1.8 MHz, and we notice that V_{Bias} is around 1.0V. Thus, the frequency range of the DPWM is 1.8MHz – 7.4 MHz.

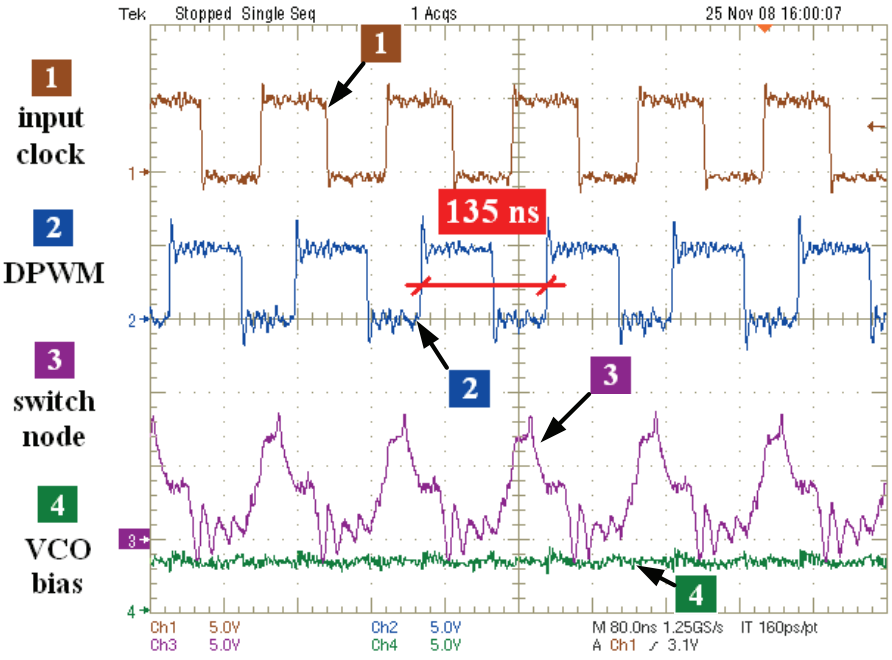


Figure 5-31. Maximum output frequency of the CR-SOH DPWM

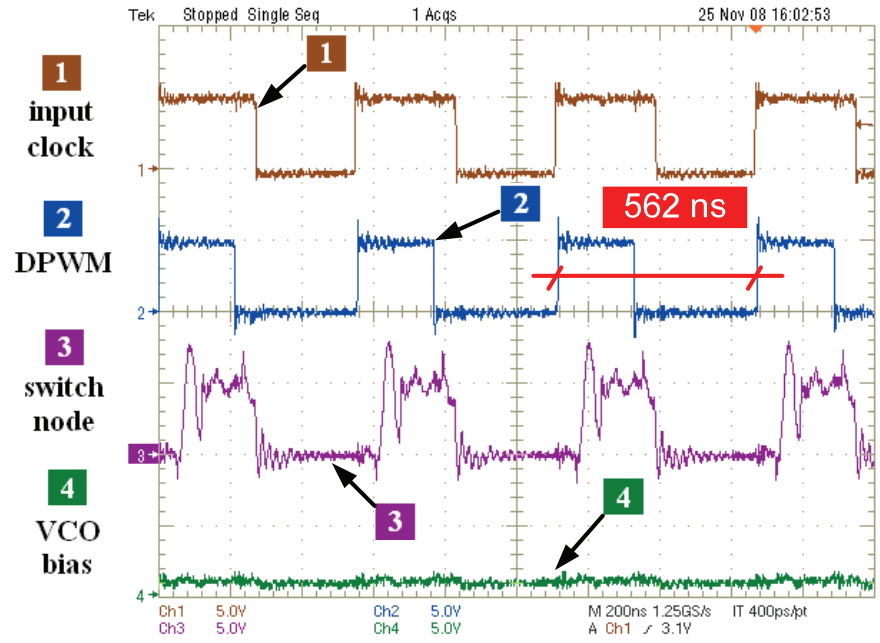


Figure 5-32. Minimum output frequency of the CR-SOH DPWM

5.8.3 Duty cycle input response

An ideal duty cycle input response indicates that output duty cycle ratio should immediately follows the input digital codes when the code arrives between the input clock's two sequential rising edges. Its operation looks like a rising edge Flip-Flop and the input code here is similar to the "D" in Flip-Flop. We test the duty cycle input response when the DPWM works at its maximum switching frequency 7.4MHz. In the test, the 9-bit duty cycle digital code will be shifted between 9'h102 and 9'h002, i.e., the highest MSB will change between 0 and 1 while other bits remain constant. Figure 5-33 demonstrates the test result when the highest MSB d[8] changes from 1 to 0. Figure 5-34 demonstrates the test result when the d[8] changes from 0 to 1.

The test result shows that the output duty cycle ratio exactly follows the input digital code's change. More detailed analysis in parallel to Flip-Flop design has not yet been carried out.

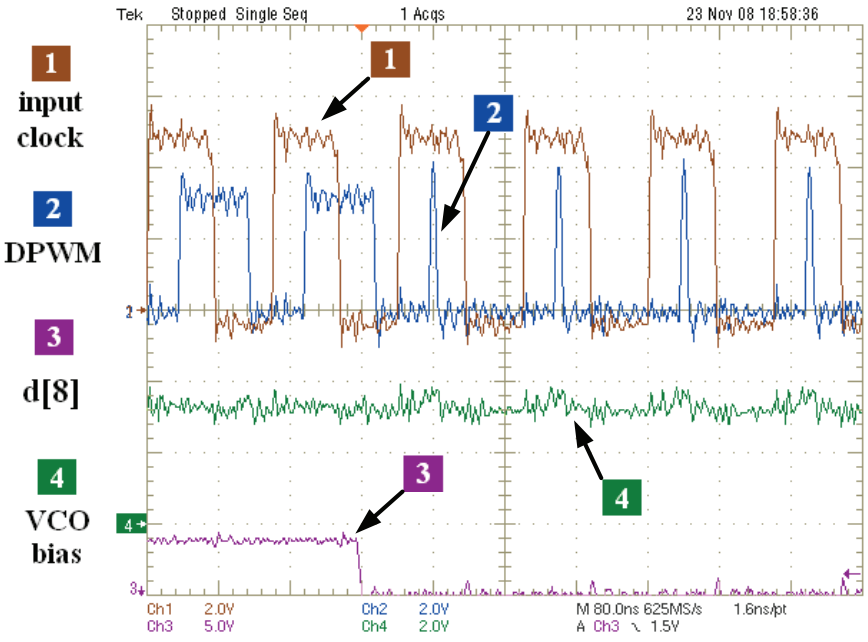


Figure 5-33. Duty cycle input dropping down response

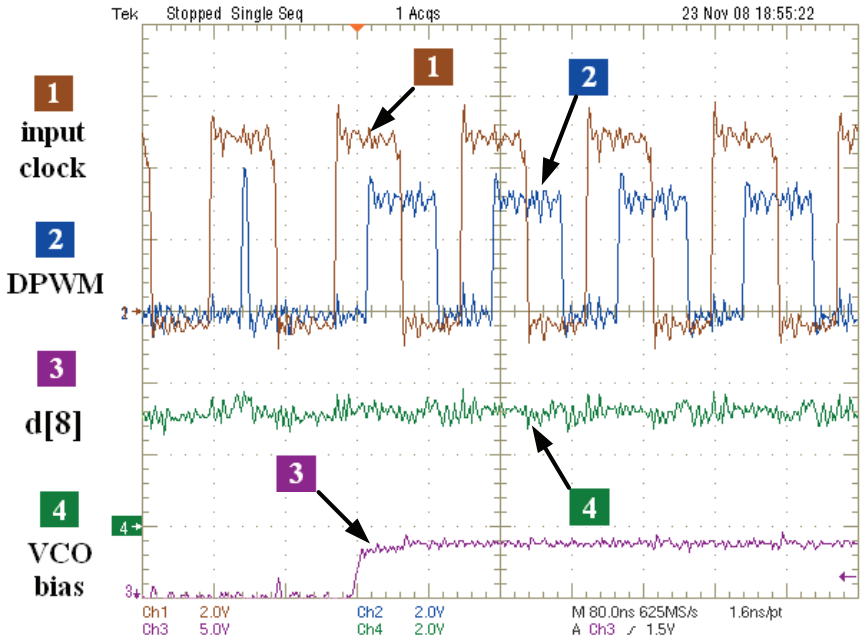


Figure 5-34. Duty cycle input rising up response

5.8.4 Linearity and monotonicity

An ideal linearity indicates a linear relationship between the input code's decimal value and the output duty cycle ratio, as the latter is supposed to be a normalized value of the former by a coefficient of 512 in a 9-bit DPWM. In comparison with linearity, the monotonicity requirement is much simpler, which only stresses that duty cycle ratio should increase when the input code increases.

The test includes four parts ranging from the finest code to the coarsest one. In the finest part, I set the 6-bit MSB (d[8:3]) of the duty cycle code into 0 and incrementally increased the 3-bit LSB (d[2:0]). Thus, the decimal value of the code will increase from 0 to 7 by 1 for each step. In the finer part, I set both d[8:6] and d[2:0] to 0 but incrementally increased d[5:3] so that the decimal value increases from 0 to 56 by 8 in each step. Similarly, for the coarse part, d[5:0] is set to be 0 and d[8:6] is increased incrementally so

that the decimal value increases from 0 to 448 by 64 in each step. In the coarsest part, all bits in d[8:0] are set to 1 to test the DPWM output duty cycle ratio when the duty cycle code's decimal value is 511.

The measured data for the aforementioned finest part, the finer part and the coarse part are respectively given in Figure 5-35, Figure 5-36, and Figure 5-37. The red dot denotes the ideal data, the green triangle denotes the simulation data and the black rectangle denotes the measured data.

The observed duty ratio errors in Figure 5-35, Figure 5-36 and Figure 5-37 are not from the DPWM architecture, while they are generated by the parasitic components and component mismatch in silicon layout.

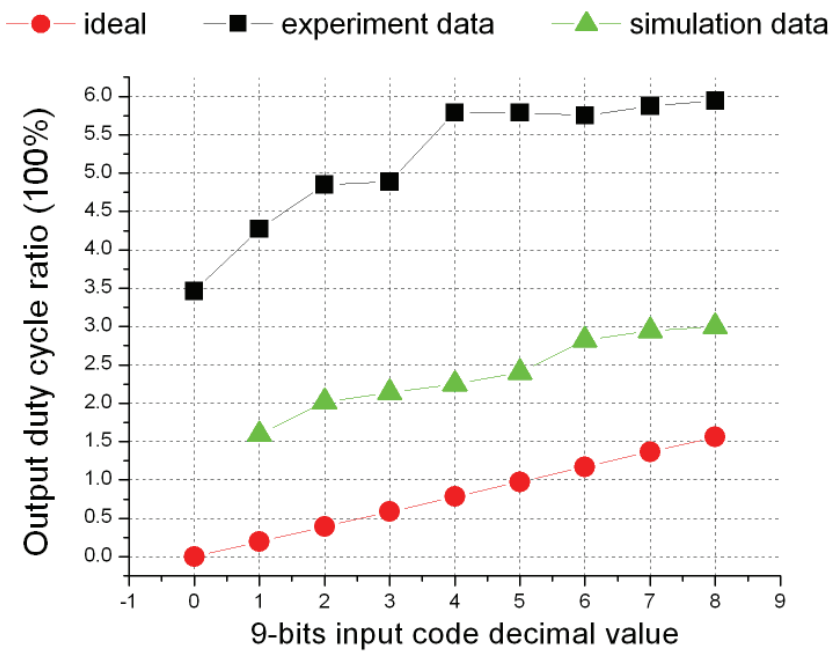


Figure 5-35. Finest level linearity and monotonicity test result

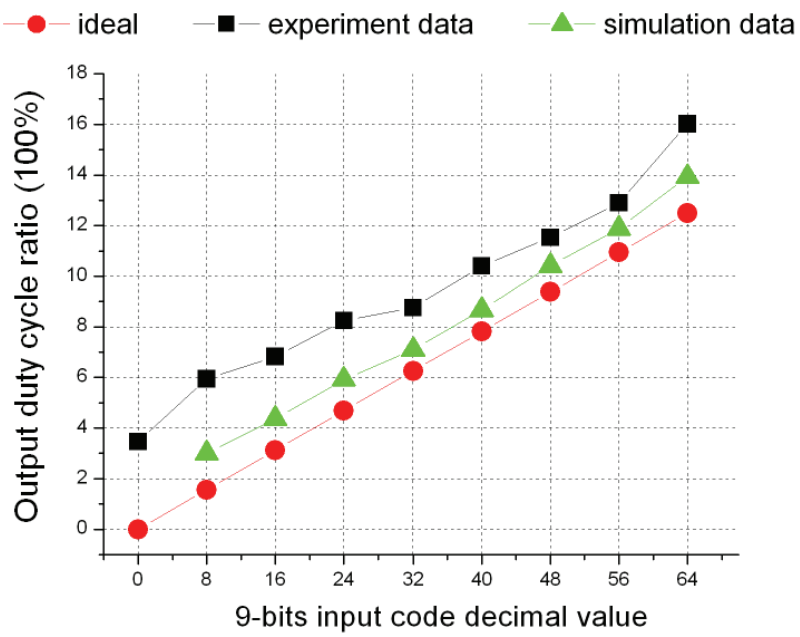


Figure 5-36. Finer level linearity and montonicity test result

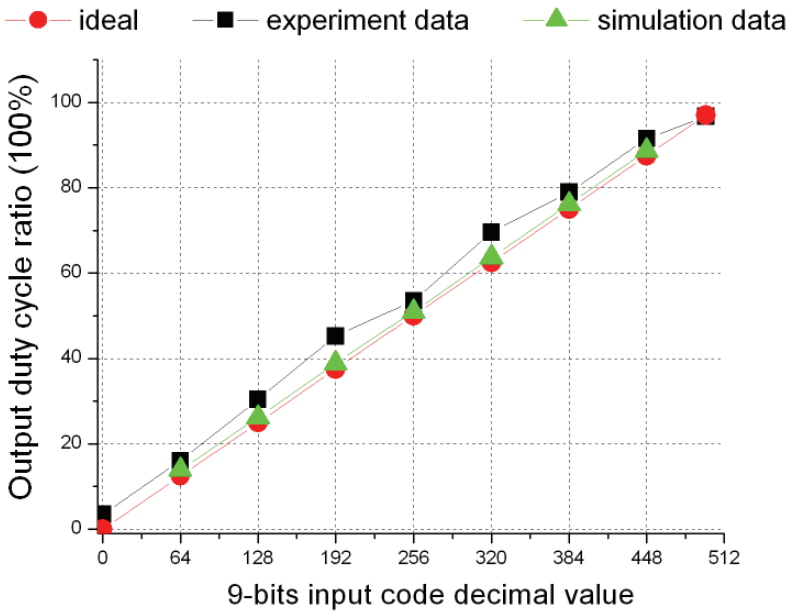


Figure 5-37. Coarse level linearity and monotonicity test result

The following factors contribute to the linearity error.

- The largest difference between simulation and fabricated chip comes from the lack of the after-layout simulation due to time pressure;
- Two-metal-layer layout and the large 64:1 mux are the major sources of linearity mismatch. Because we only used two metal layers in 64:1 mux layout, the metal route length difference might be significant. The longest metal route is around 2-3 micrometers and the shortest one is around 0.5-0.6 micrometers;
- DM in Figure 5-13 does not completely compensate the delay mismatch;
- In order to explore the maximum output frequency, we use the inverter type delay cell in the delay chain. As a result, "P" and "N" in Figure 5-20 are needed to fit the signal's alternatively phase change in the delay chain. Thus, the propagation difference between "P" and "N" block is another source of delay mismatch;

Based on all the measured data in Figure 5-35, Figure 5-36 and Figure 5-37, the linearity is investigated with coefficient ρ_i in equation (5-73) and the result is illustrated in Figure 5-38.

$$\rho_i = \frac{d_i(t)_i - d_{i-1}(t)}{d_i^{ideal}(t) - d_{i-1}^{ideal}(t)} \tag{5-73}$$

where $d_i(t)$ and $d_{i-1}(t)$ represent the normalized values of the duty cycle ratio corresponding to two input codes sequential in test. $d_i^{ideal}(t)$ and $d_{i-1}^{ideal}(t)$ represent the ideal value of $d_i(t)$ and $d_{i-1}(t)$. An example is that, 9'h080 and 9'h0c0 are two sequential input codes in the coarsest test part, their corresponding ideal values will be $d_{i-1}^{ideal}(t) = \frac{128}{512} = 0.25$ and $d_i^{ideal}(t) = \frac{192}{512} = 0.375$.

An ideal linearity indicates that coefficient ρ_i will be one for any value of i. The measured ρ_i are reported in Figure 5-38.

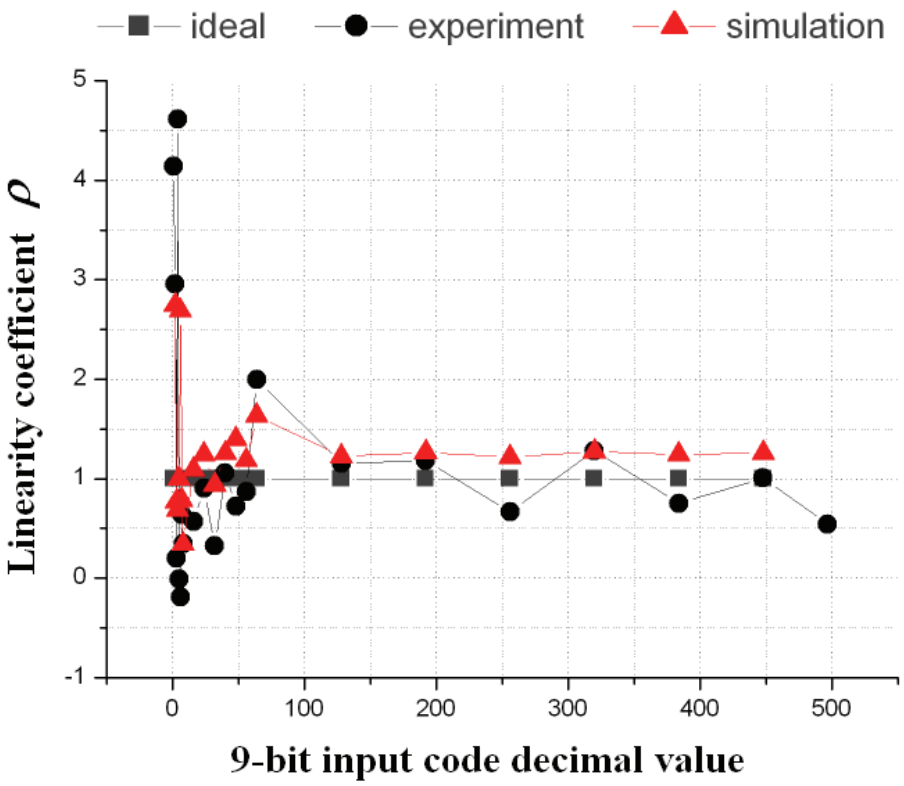


Figure 5-38. Linearity report for the fabricated chip

5.8.5 Power dissipation breakdown

From Figure 5-27 and Figure 5-29, we notice that the power supply of DPWM is separated from the power supplies of other components and the I/O interface. The total current consumption is measured when the DPWM chip operates at the maximum frequency 7.4MHz and the associated data is 1.07mA, i.e., 143.8 $\mu A/MHz$. The

measured value is around 10% larger than the simulation data. The current consumption breakdown is given in Figure 5-39 with the aid of simulation data.

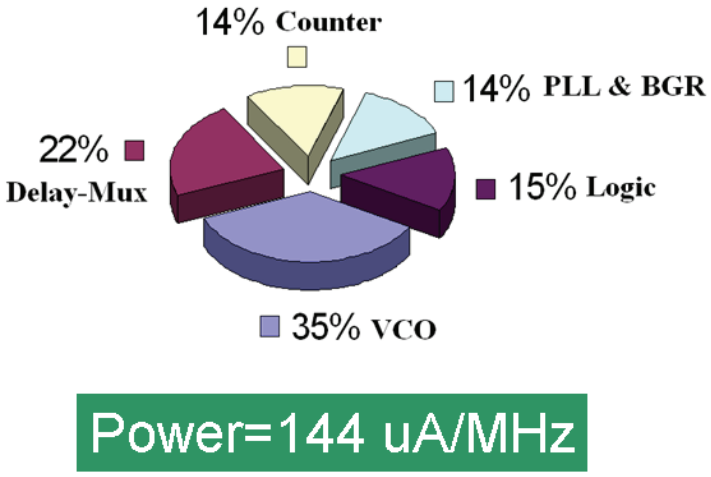


Figure 5-39. Current consumption breakdown (VDD=3.3V)

5.8.6 Silicon area breakdown

The actual chip area is 0.703 mm^2. In Figure 5-36, we notice that more than 50% silicon area is consumed by the 64:1 mux which is routed with only two metal layers. The details silicon area breakdown is given in Figure 5-40.

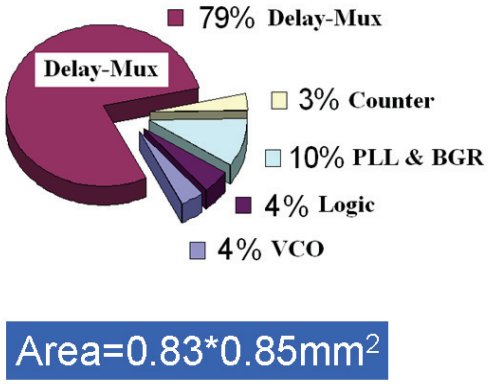


Figure 5-40. Chip area breakdown

5.9 Conclusion and future work

In this chapter, we systematically investigate the performance of present DPWM architectures and in particular focus on the maximum output frequency achievable in the architectures. The relationship between the maximum output frequency of the DPWM and the MSF in the digital DC-DC converter is also comprehensively discussed, with which we can see the importance of the DPWM implementation in digital DC-DC converter's portable application. Furthermore, in recognition of the choke effect in the SOH DPWM and the delay cell digital programming feature in the NSOH DPWM, the CR-SOH DPWM is proposed. This chapter also discusses in detail power consumption, silicon area, and frequency control in the DPWM architectures and the relative matching accuracy in the hybrid DPWM. Moreover, many equations are proposed for the analysis of the aforementioned performance.

In the conclusion, we will summarize the performance comparison of the mentioned DPWM architecture and give some suggestions on the future research work.

5.9.1 Architectures comparison

5.9.1.1 MSF comparison

MSF of the digital DC-DC converters heavily depends on the maximum output frequency of the DPWM, because the maximum output frequency is usually far less than other limitations in a high performance digital DC-DC converter.

Let us focus on the case with AMI06 technology and 9-bit resolution requirement. In the particular case, no matter which kind of the present DPWM architecture we try, the maximum output frequency of the DPWM cannot exceed 10 MHz. Thus, there is a MSF limitation in DPWM from the viewpoint of hardware architecture. The MSF available in all mentioned DPWM architectures are summarized in Figure 5-41, in which we assume

g=2 exists for the NSOH DPWM. Table 5-5 lists the equations for calculating the MSF in different DPWM architectures.

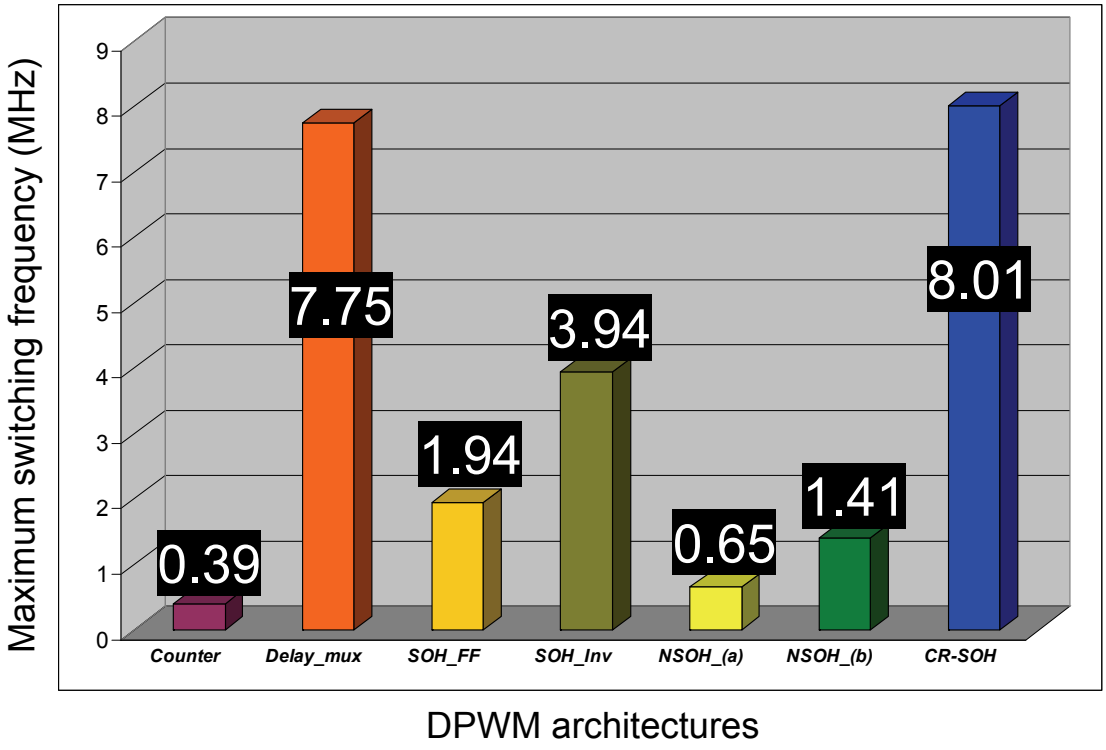


Figure 5-41. MSFs in 9-bit hard resolution DPWMs with AMI06 technology

5.9.1.2 Relative matching error comparison

The relative matching error δ is an issue addressed in the hybrid DPWM. There is no relative matching error in the SOH DPWM and the CR-SOH DPWM. However, for the NSOH DPWM, the relative matching error does exist.

Table 5-5 shows the difference among all mentioned DPWM architecture.

5.9.1.3 Frequency control comparison

The difference on the frequency control is how many PLLs and DLLs the architecture needs to implement frequency control and how accurate the frequency control can be. The frequency control applies only to the NSOH-DPWM with digitally programmed delay cells.

Table 5-5 shows the differences between all mentioned DPWM architectures.

5.9.1.4 Power dissipation comparison

As mentioned before, it is only reasonable to compare the dynamic power dissipation consumed by all of the delay cells in the delay chain, the delay compensation cells, the counter, and the multiplexer. I had utilized $Power_{unit}$ to scale the dynamic power dissipation in the first two items. In order to investigate the dominant power consumption scale in the DPWM, as to the third items, I approximate the dynamic power of a h-bit counter as $40 \times 2^{(h+1)} \times Power_{unit}$. Furthermore, I approximate the dynamic power of a h-bit multiplexer as $8 \times 2^{h} \times Power_{unit}$. Table 5-5 shows the dominant power scale estimated in the mentioned DPWM architecture.

From Table 5-5, we conclude that: 1) either the Counter DPWM or the SOH-Inv will be the most power hungry architecture; 2) the CR-SOH will lead the best power saving performance.

5.9.1.5 Silicon area comparison

The component breakdown in the delay chain, counter, and multiplexer of the DPWM is reported in Table 5-5.

From the Table 5-5, we conclude that: 1) the Delay_mux DPWM occupies the largest silicon area because it is a $2^{R}:1$ mux; 2) the NSOH DPWM with delay cell in Figure 5-24 (a) may be another candidate of the largest silicon area when the number of delay cell

resolution bits g is larger than 4; 3) the CR-SOH is the best silicon area saver. If we take the whole DPWM architecture into consideration, the CR-SOH's advantages will be strengthened because it only has one simple PLL implementation for frequency control.

5.9.2 Chip data collection

The performance data of several public reported DPWM chips are collected in Table 5-6. There is an extra column in Table 5-6 which predicts what would be the limit of the maximum switching frequency of the associated DPWM in the particular specification. The prediction is accomplished with the equations developed in this chapter.

5.9.3 Future work

5.9.3.1 Wide range frequency control

The range of the switching frequency regulation depends on the PLL and the delay cell's regulation curve illustrated in Figure 5-38. To support the power optimization of the DC-DC converter in the light load operation, the power stage will work in the discontinuous conduction mode and the associated switching frequency could be 10-50 times lower than its normal value. Thus, it is imperative that the relative DPWM has whole range frequency control capacity. Besides the availability of the whole range frequency regulation, other important characteristics in the whole range frequency control should include: 1) VCO delay regulation sensitivity; 2) scalable PLL filter design; 3) scalable offset and delay compensation; 4) acceptable sacrifice of power dissipation and silicon area; It is obvious from Figure 5-38, Figure 5-49 and Figure 5-50 that the current CR-DPWM design does not consider the aforementioned whole range frequency control.

There are already several interesting works covering this topic [5-29, 5-48, 5-53].

5.9.3.2 DPWM soft resolution

The soft resolution is very helpful to improve the MSF without sacrifice of power and silicon area. However, the current performance investigation only focuses on steady state, which is not helpful to understand the impact of the soft resolution on the closed loop control performance and the trend when the switching frequency continuously increases.

5.9.3.3 Linearity improvement

The CR-SOH DPWM should have a perfect linearity if its layout is done well. Unfortunately, the linearity of the test chip is not good due to layout time constraints and other external factors. Thus, linearity improvement is a possible topic for the future, if there is another chance to implement the CR-DPWM.

5.9.3.4 Multi-phase implementation

Multi-phase operation of several DC-DC power converters benefits power rating, transient performance, and reliability. Compactly implementing it in the DPWM [5-12, 5-13] is a challenge, especially when the whole range frequency control is also desired.

5.9.3.5 Integration of the dead time optimization

The ability to digital program the dead time to achieve some extent power optimization is one of the advantages of the digital DC-DC converter [5-73, 5-20]. However, its implementation becomes difficult when we stress the whole range frequency control.

5.9.3.6 Digital DC-DC converter

A high performance digital DC-DC converter for portable applications should have a DPWM with maximum output frequency limitation, whole range frequency control,

perfect linearity, and power and silicon savings. It should also have a compact A/D converter and a multi-functional digital controller.

Accurate and fast output voltage regulation, the component's power dissipation, and the MSF limitation will be the dominant bottlenecks for portable applications.

At present, a full digital DC-DC converter may not be a good candidate for portable applications. However, as we know, a fully analog converter is also not a good candidate for aggressive power management. Thus, the power supply solution in the portable applications may be a hybrid solution.

Table 5-5. Summary of the analyzed DPWM architecture performance

Type		MSF * $t_{FO-4}^{worst-case}$	δ	Choke Effect	Resolution	Freq. cont.	Dominant scale power ($Power_{unit}$)	The delay chain, counter and multiplexer components breakdown
Counter		$\frac{1}{2^R \times \alpha}$ *(5-18)*	-	-	R=m+k	PLL	$2^R \times 80$ (counter)	R -bit counter
Delay_ mux		$\frac{1}{2^R \times \beta}$ *(5-24)*	-	-	R=m+k	DLL	$2^R \times 9$ (mux)	2^R * delay cells + 2^R :1 mux
SOH*	Flip-Flop	$\frac{1}{2^{R+2}}$ *(5-30)*	0	Y	m+k	-	$2^R \times 40$ (Flip-Flops)	m -bit counter + 2^k :1 mux +$\left(2^k - 1\right)$ * Flip-Flops
	Inverter	$\frac{1}{\left(2^{R+1} - 2^{m+1}\right)}$ *(5-33)*	0	Y	m+ $\log_2\left(2^k - 1\right)$	PLL	2^{R+k-1} (Inverters)	m -bit counter + 2^k :1 mux +$\left(2^k - 1\right)\times\left(2^{(k-1)} + 1\right)$*Inverters
NSOH*	[R5' 71]	$\frac{1}{3 \times 2^{(R+g)}}$ *(5-51)*	*(5-55)*	-	m+k	DLL PLL	2^{k+2g+3} (Nand, Nor)	m -bit counter + 2^k :1 mux +$\left(2^k - 1\right)\times 2^{2g}$ * 2-Nor +$\left(2^k - 1\right)\times\left(2^g + 1\right) * 2^g$ -Nand
	[R5' 30]	$\frac{1}{2^R \times \left(g + 3.5\right)}$ *(5-52)*	*(5-56)*	-	m+k	DLL PLL	- (delay cells)	m -bit counter + 2^k :1 mux +$\left(2^k - 1\right)\times\left(g + 1\right)$ * 2-Nand + $\left(2^k - 1\right)\times\left(g + 1\right)$ * (5 binary-sized NMOS)
CR-SOH*		$\frac{1}{\left[2^R - 2^{m+1}\right]}$ *(5-61)*	0	R	m+ $\log_2\left(2^k - 2\right)$	PLL	2^{m+7} (counter) or 2^{R-1} (VCO inverters)	m -bit counter + 2^k :1 mux +$\left(2^k - 1\right)$ * Inverters (delay chain) + $\left(2^{k-1} - 1\right)$ * Inverters (VCO)

Table 5-6. Summary of the reported DPWM chip performance

Papers	Univ.	Type	Year	Process tech.	Hard resolution		Reported Frequency (MHz)	The maximum frequency predicted by the equations in this work (MHz)	VDD (V)	Current dissip. (uA)	Silicon Area (mm2)
					Counter (m-bit)	Delay_mux (k-bit)					
[R5'08] [R5'17]	M.I.T	SOH (Buf.)	2000	$0.6\mu m$ CMOS	4	6 (2-seg.)	0.5	1.94	2.05	199.3	-
[R5'65]	St. U.	SOH (Buf.)	2001	$0.8\mu m$ CMOS	5	4	1	1.55	-	-	-
[R5'40] [R5'41]	U. Co.	SOH (F.F.)	2003	$0.5\mu m$ CMOS	3	5	1	4.65	5	7,700	-
[R5'69] [R5'70]	U. Be.	Delay (R.Os.)	2004	$0.25\mu m$ CMOS	0	5	1	74.4 ($\beta = 4$)	0.75	10	0.084
[R5'58] [R5'59]	U. To.	Delay (Domi.)	2005	$0.13\mu m$ CMOS	0	8 (4-seg.)	11.6	14.3 ($\beta = 5$)	1.2	190	0.0075
[R5'56] [R5'71] [R5'72]	U. Co.	NSOH (g=1)	2006	$0.35\mu m$ CMOS	2	5	10 (Sim.)	8.86	2	-	-
[R5'28] [R5'30]	U. To.	NSOH (g=2)	2007	$0.18\mu m$ CMOS	0	4	16 150 (Sim.)	150.31	1.8	880	0.028
[R5'62] [R5'63]	NCSU	CR-SOH (Inv.)	2009	$0.6\mu m$ CMOS	3	6	7.4	8.0	3.3	1,070	0.703

St. U.: Stanford Univ.; U. Co.: Univ. Colorado; U. Be: Univ. Calif. Berk.; U. To.: Univ. Toronto; Buf: Buffer; F.F.: Flip-Flop; R.Os: Ring oscillator; Domi: Domino; Inv.: Invereter; Sim: Simulation; dissip.: dissipation; seg.: segmentation.

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Chapter 6

Summary of contributions

This dissertation considered the efficiency analysis, efficiency conscious design, and silicon implementation of high frequency integrated synchronous Buck DC-DC converters (ISBC). This dissertation proposed an event based switching loss analysis method, a Vsw pinning automatic segmentation technique, and a choke relaxed self-oscillation hybrid digital pulse width modulator architecture. The detailed contributions are summarized in this Chapter.

6.1 Event based switching losses analysis

The state-of-art switching analysis methods analyzed the switching loss from outside the ISBC chip and from the viewpoint of an application engineer. The state-of-art analysis depended on two assumptions about MOSFET parasitic capacitance parameters. The first assumption is that there is a constant relationship between the parameters for loss analysis including cgd, cgs, and cdb and the parameters measured from MOSFET device including ciss, coss, and crss. The second assumption is that the values of the parameters including cgd, cgs, and cdb are constant during the switching transient. Also, the methods ignored variation of the power FET channel current in different switching events. Thus, the state-of-art methods failed for applications where some of the power FET subcells inside the ISBC chip are disabled for the benefit of efficiency in light load conditions.

This dissertation investigated the switching loss from inside the ISBC chip and from the viewpoint of an IC design engineer. The dissertation emphasized the breakdown of

switching loss according to the physical mechanism of loss generation and suggested a thorough classification between charging/discharging loss and overlap loss. The dissertation also made efforts to relate the loss analysis model to the technology process parameters, rather than test data measured outside the chip. Several contributions of the dissertation to the switching loss analysis in the ISBC are listed as:

6.1.1. Suggested simultaneously break-down the four-terminal currents of two power FETs in each switching event. If only one power FET is involved or substrate terminal is ignored, the analysis deviates from the case in a practical ISBC.

6.1.2. Physically clarified and completely separated the charging/discharging loss and overlap loss. Any loss generated by the charging/discharging current of parasitic capacitors is attributed to the charging/discharging loss. The overlap loss refers to the loss generated in power FET physical channel by the current component irrelevant to the charging/discharging process. In different switching events, the overlap loss will be different due to the fact that parasitic capacitor's charging/discharging currents change their flowing direction.

6.1.3. Suggested to evaluate the charging/discharging loss in four steps. The first step is to evaluate the energy variation of one capacitor in a switching event. The second step is to calculate the ratio of loss in the charging/discharging loop. The third step is to repeat the practice to all parasitic capacitors in the ISBC in all switching events. The final step is to add the loss together.

6.1.4. Proposed a hypothesis to approximately evaluate the energy variation of a parasitic capacitor in a switching event. During the switching event, the capacitance will change along with the shift of operation mode of the power FET. The hypothesis is verified to be effective for twelve different working conditions.

6.1.5. Suggested a parasitic capacitance extraction method in Cadence simulation environment;

6.1.6. Found that the charging/discharging loops in the ISBC can be classified into five types. The ratio of loss with respect to the energy variation of a capacitor is almost one in three types of loops, while it is ignorable in other two types of loops. The difference lies on the restriction placed on the magnitude of charging/discharging current and whether the capacitor energy is recovered. If the current is magnitude free like a standard R-C loop, the ratio of loss will be almost one. On the contrary, if the magnitude of the current is limited by the power inductor current, the loss will be negligible.

6.1.7. Developed onset criteria of the Miller plateau which theoretically explain the principal difference between the control power FET turning on and off, and why there is no Miller plateau in some applications when the synchronous FET turns off.

6.1.8. Developed equations for calculating the overlap loss, the optimal dead-time value and the optimal sizing of power FET drivers.

6.1.9. The proposed model matched very well with the simulation data. Also, it correctly explained the data reported by other researchers. The silicon layout of a 4MHz ISBC chip with 3-bit logically controlled active power FET subcells was completed. The chip has been submitted for fabrication in the **MOSIS** *run* **V07G** *with the Fab-ID* **V07GBJ**. *The chip is expected at MOSIS on Jan.31.2010.*

6.1.10. The proposed switching loss analysis method had four assumptions. The first one is that forwards voltage drop of the power NMOS is constant in all load conditions for the sake of simplifying analysis. The assumption generates a minor

prediction error in some working conditions; The second one is that the power inductor current never goes negative and the ISBC works in CCM; The third one is that the package inductance is very small as the practice in the commercial products so that its impact is ignorable. The forth one is that the ISBC is correctly designed and there is no extra loss induced by power FET shoot through or cdv/dt false turn-on.

6.2 Vsw pinning automatic segmentation

State-of-art techniques used a current sensor and an A/D converter to implement the automatic segmentation. Furthermore, due to the lack of a loss analysis method, there is no equation relating the optimal number of power FET subcells to the load current, so the segmentation algorithm in the state-of-art techniques was from some equations developed on the basis of an incorrect W/N assumption. Utilizing the proposed switching loss analysis method in this dissertation, it is predicted that the optimal number of power FET subcells will be almost linearly proportional to load current when the load current is in certain range. The prediction explained the observations and practices of other researchers. The developed equations also for the first time indicated a saturation phenomenon about the linear relationship between the optimal number of power FET sub cells and the load current, which happens when the load current is close to its maximum value utilized for the power FET width optimization. The physical explanation of the saturation phenomenon is that the power losses contribution of Cdb in the inactive power FET sub cells is not included in the optimization process of the number of active power FET sub cells. Thus, the optimization process concludes that the optimal number of active sub cells is larger than the total number of power FET sub cells when we do the optimization process in the maximum load condition.

Good efficiency is the result of balancing switching loss and conduction loss. If we use the state-of-art techniques to implement automatic segmentation on the basis of load

current information, the expected efficiency might not be met in practice because of Rdson variation due to temperature or other reasons. At the same time, when switching frequency is beyond 2.5MHz, the on-chip current sensor's accuracy requirement is very difficult to satisfy and the quiescent current of opamp and high resolution A/D converters degrades the ISBC efficiency in the deep light load condition. Also, the big silicon area consumed by the current sensor and A/D converter is also not good for portable applications. Another challenge with the state-of-art techniques is how to maintain constant current gain when the number of power FET subcells significantly changes.

The dissertation proposed a Vsw pinning automatic segmentation technique (VswPS) which does not need on-chip current sensor and A/D converter. Furthermore, VswPS provides automatic Rdson compensation. Several contributions of the dissertation to automatic segmentation in ISBCs are listed as:

6.2.1. Concluded that the optimal number of active power FET subcells is almost linearly proportional to load current when the load current is in certain range. The derived equation explains the practice behind state-of-art techniques. The derived equations also reveals that when the load current is close to the maximum load current utilized to determine the power stage width, there is a saturation effect about the number of optimal active cells. On the contrary, when the load current is close to half of the peak-to-peak inductor current, the linear relationship is distorted.

6.2.2. Emphasized the impact of Rdson variation because of temperature and other practical factors on the ISBC efficiency. If the load current is used to implement segmentation as did in the state-of-art techniques, the obtained result will deviate from an expected one because of the temperature or other reasons.

6.2.3. Proposed a VswPS technique which adjusts the number of power FET subcells in a novel algorithm. The proposed algorithm does not force the number of active

sub cells to be linear with load current, but forces the Vsw voltage level to be pinned in a band for various load conditions.

6.2.4. *Suggested using two latched pipeline comparators and a 3-bit state machine to implement the VswPS technique. There is no need for a current sensor and no need for an A/D converter. The change makes the implementation of segmentation technique available and efficient in >2.5MHz switching frequency application.*

6.2.5. *Proposed a reliable operation block to ensure safe operation of VswPS for load transients.*

6.2.6. *Suggested using the state machine to implement the smooth mode shift from PWM to PFM.*

6.2.7. *Proposed a switching pulse counting block for the smooth mode shift from PFM to PWM*

6.2.8. *The performance of the VswPS technique had been verified with simulation. The silicon layout of a 4MHz ISBC chip with the VswPS technique was completed. The chip had been submitted for fabrication in the* **MOSIS** *run* **V07G** *with the Fab-ID* **V07GAU**. *The chip is expected at MOSIS on Jan.31.2010.*

6.3 Choke-relaxed self-oscillation hybrid DPWM

The maximum switching frequency of state-of-art digital DC-DC converters is reported be around 16MHz with 0.18um CMOS technology. The switching frequency is much lower than that in analog DC-DC converters where 300MHz switching frequency has been reported. This dissertation focused on investigating the reason behind that fact

and made efforts to improve the state-of-art techniques. Several contributions of the dissertation to the DPWM in a digital ISBC are listed as:

6.3.1. *Utilized FO4 to investigate the MSF of state-of-art DPWM architectures so that the architectures' MSF values are predictable for any semiconductor technology.*

6.3.2. *Discussed various state-of-art solutions to improve the resolution of DPWM and classified the hardware resolution and soft resolution.*

6.3.3. *Discussed various state-of-art hybrid DPWM architectures and compared the MSF, relative matching error, frequency control ability and power consumption.*

6.3.4. *Indicated that the bottleneck of MSF in the self-oscillation hybrid DPWM (SOH) is relative to a choking phenomenon.*

6.3.5. *Suggested separating the VCO and the delay_line chain in the SOH to relax the choked effect. The modified solution is named as relaxed self-oscillation hybrid DPWM (RSOH). In comparison with SOH, the MSF in RSOH can be 100% higher together with 40% power saving.*

6.3.6. *Predicted that the DPWM with RSOH architecture is able to approach 8MHz switching frequency when it is implemented with AMI06 process.*

6.3.7. *The silicon layout of an 8MHz DPWM chip with RSOH architecture was completed. The chip had been submitted for fabrication in the* **MOSIS** *run* **T86S** *with the Fab-ID* **T86SAQ.** *The chip arrived at NCSU in Sep.2008 and was tested in Oct.2008. The test results verified that the chip has good performance and the MSF is 7.4MHz.*