ABSTRACT

ZHIGANG, LIANG. High Efficiency Distributed Solar Energy Conversion Techniques. (Under the direction of Dr. Alex Q. Huang)

The global demand for electric energy has continuously increased over the last few decades. Photovoltaic (PV) sources are predicted to become one of the biggest contributors to electricity generation among all renewable energy generation candidates by 2040.

At the meanwhile, the emerging distributed solar power conversion technologies, i.e., string inverter, multi-string inverters and micro-inverters, are widely adopted in the present photovoltaic (PV) applications, particularly for the residential level roof-top application and commercial PV applications. The core technology associated with the distributed solar energy conversion remains the distributed MPPT stage and the inverter control.

This research work focuses on development of high efficiency DC/DC converters for distributed MPPT stage as well as low cost single chip maximum power point tracking (MPPT) solution for the distributed solar energy conversion.

The resonant DC/DC converters, which are widely used as the front end stage in many applications, are also good candidates for the distributed MPPT stage application due to their simple structure, soft switching features and high efficiency. However, the design challenge is how to obtain a high efficiency over wide input voltage range under different load conditions. In this work, two kinds of high efficiency resonant DC/DC converter topologies are proposed in Chapter 3 and Chapter 4. Both of them may be designed to cope with a wide input range voltage and they may change the operation modes based on the sensor information to optimize the conversion efficiency. And the soft switching features for the
MOSFETs in the primary side and ZCS for the diodes in the secondary side are still preserved. The performance of proposed converters is validated by both of the simulation and experimental results.

For the distributed MPPT application, it requires a MPPT controller to generate a proper reference signal for the DC/DC controller in order to ensure the PV module operating at its maximum power point. In Chapter 5, a cost-effective analog MPPT controller is proposed to form a single chip controller solution for the distributed MPPT stage. The operation of proposed MPPT controller is based on a logic truth table extracted from the perturbation and observation (P&O) algorithm. The capacitor based storage cell concept is proposed to store the $V_{pv}$ and $P_{pv}$ in the last perturbation cycle. The perturbation frequency and step size may be adjusted by the user. The operation principle of the new controller is explained and the parameter design procedure is presented. The tracking performance of the proposed controller has been validated by both of the simulation and experimental results with 200W PV panels under different sun irradiance level and temperature.
High Efficiency Distributed Solar Energy Conversion Techniques

by
Zhigang Liang

A dissertation submitted to the Graduate Faculty of North Carolina State University in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering

Raleigh, North Carolina
2011

APPROVED BY:

Dr. Alex Q. Huang
Committee Chair

Dr. Mesut Baran

Dr. Subhashish Bhattacharya

Dr. Srdjan Lukic
DEDICATION

TO MY PARENTS

MINGYUAN LIANG AND CHONGXIN MA
BIOGRAPHY

The author, Zhigang Liang, was born in Sichuan, China. He received B.S. and M.S in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2003 and 2006, respectively. He started to pursue the Ph.D. degree in North Carolina State University in 2007. He worked as a system engineer in Monolithic Power Systems (MPS) Inc Hangzhou from 2006 – 2007. He was a Co-op of Texas Instruments in 2010.
ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my advisor, Dr. Alex Huang, for his support, guidance and encouragement. Dr. Huang’s broad knowledge, great intuition and accurate judgment have been the source of inspiration for my research in North Carolina State University during the past several years. The most precious things I have learned from him are the ability of independent research and also a long-term vision in the research.

I am grateful to my committee members, Dr. Mesut Baran, Dr. Subhashish Bhattacharya, Dr. Srdjan Lukic for their valuable suggestions and help. Also I would like to thank Dr. Celeste Sagui for her service as the Graduate School Representative of my defense.

It has been a great pleasure to work in the Semiconductor Power Electronics Center (SPEC) as well as in the National Science Foundation (NSF) newly funded Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. The FREEDM Center provides a world-class research environment for the power electronics and renewable energy utilization and management. I would like to thank my colleagues in the Utility Power Electronics (UPE) group, DC Microgrid group and all members of SPEC and FREEDM Systems Center, including Dr. Chong Han, Dr. Bin Chen, Dr. Yu Liu, Dr. Wenchao Song, Dr. Tiefu Zhao, Dr. Yan Gao, Dr. Jinseok Park, Dr. Xiaojun Xu, Dr. Jiwei Fan, Dr. Liyu Yang, Dr. Xin Zhou, Dr. Sungkeun Lim, Dr. Xiaopeng Wang, Dr. Jun Wang, Dr. Jeesung Jung, Dr.
Parkhideh Babak, Dr. Jun Li, Dr. Xiaohu Zhou, Mr. Jifeng Qin, Ms. Juming Lai, Mr. Gangyao Wang, Mr. Qian Chen, Mr. Woongje Sung, Ms. Zhengping Xi, Ms. Zhan Shen, Mr. Zhuoning Liu, Mr. Sanzhong Bai, Mr. Xunwei Yu, Mr. Yen-Mo Chen, Mr. Li Jiang, Mr. Xu She, Ms. Jerry Hu, Mr. Yalin Wang, Mr. Xingchen Yang, Ms. Mengqi Wang, Mr. Pochih Lin, Mr. Fei Wang, Mr. Kai Tan, Mr. Xin Huang, Mr. Jiadi Jiang, Mr. Yizhe Xu, Mr. Rui Wang, Mr. Rui Gao, Ms. Xuansu Guo, Mr. Xiang Lu, Mr. Edward van Brunt, Mr. Anand Ramamurthy, Mr. Arvind Govindaraj, Mr. Baek Seunghun, Mr. Habiballah Rahimi-Eichi and Mr. Hesameddin Mirzaee Teshnizi. Also I would like to thank several visit scholars of the FREEDM Systems Centers, including Dr. Jiangjiang Shi, Dr. Wenxi Yao and Dr. Wu Chen.

I appreciate the assistance from the staff members of the SPEC and FREEDM Systems Center. They are Mr. Anousone Sibounheuang, Ms. Karen Autry, Ms. Colleen Reid, Mr. Rogelio Sullivan, Mr. Ewan Pritchard, Mr. Seth Crossno and Mr. Hulgize Kassa.

I also would like to give my special thanks to the North Carolina Solar Center for their donation of solar panels to my research and experiment.

My heartfelt appreciation goes toward my parents, Mingyuan Liang and Chongxin Ma, who have always supported and encouraged me during my study life.

Finally, with the deepest love, I would like to thank my wife, Rong Guo, for your love, encouragement and helpful suggestions for my research.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>LIST OF TABLES</th>
<th>ix</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIST OF FIGURES</td>
<td>xi</td>
</tr>
<tr>
<td>Chapter 1. Introduction</td>
<td>1</td>
</tr>
<tr>
<td>1.1. Research Background</td>
<td>1</td>
</tr>
<tr>
<td>1.2. Dissertation Outline</td>
<td>6</td>
</tr>
<tr>
<td>Chapter 2. Grid-tied Solar Inverter Technologies: An Overview</td>
<td>11</td>
</tr>
<tr>
<td>2.1. Basic Demands for PV Inverters</td>
<td>11</td>
</tr>
<tr>
<td>2.2. Evolution of PV Converters: Past Present and Future</td>
<td>17</td>
</tr>
<tr>
<td>2.3. Energy Yield Comparison of Different PV Inverter Technologies</td>
<td>32</td>
</tr>
<tr>
<td>2.4. Category of PV Inverter Topologies</td>
<td>35</td>
</tr>
<tr>
<td>2.4.1. Number of Power Processing Stages</td>
<td>35</td>
</tr>
<tr>
<td>2.4.2. Transformers and Grounding</td>
<td>38</td>
</tr>
<tr>
<td>2.4.3. Trends and Present Development</td>
<td>48</td>
</tr>
<tr>
<td>2.5. Summary</td>
<td>66</td>
</tr>
<tr>
<td>Chapter 3. “Hybrid Bridge” High Efficiency Resonant DC/DC Converter for String Level Distributed MPPT Applications</td>
<td>68</td>
</tr>
<tr>
<td>3.1. Research Motivation</td>
<td>68</td>
</tr>
<tr>
<td>3.2. Operation Principle of “Hybrid Bridge” Resonant Converter</td>
<td>74</td>
</tr>
<tr>
<td>3.3. Analysis of Proposed Converter Operation with PV Modules</td>
<td>82</td>
</tr>
<tr>
<td>3.4. Design Considerations for “Hybrid Bridge” Resonant Converter</td>
<td>85</td>
</tr>
<tr>
<td>Chapter</td>
<td>Title</td>
</tr>
<tr>
<td>---------</td>
<td>----------------------------------------------------------------------</td>
</tr>
<tr>
<td>3.5</td>
<td>Simulation and Experiment Verification</td>
</tr>
<tr>
<td>3.6</td>
<td>Summary</td>
</tr>
<tr>
<td>4</td>
<td>Variable Resonant Tank (VRT) High Efficiency DC/DC Converter for</td>
</tr>
<tr>
<td></td>
<td>Module Level D-MPPT Application</td>
</tr>
<tr>
<td>4.1</td>
<td>Research Motivation</td>
</tr>
<tr>
<td>4.2</td>
<td>Comparison of MICs in Series and Parallel Connections</td>
</tr>
<tr>
<td>4.3</td>
<td>Proposed VRT Resonant Converter and Its Operation Principle</td>
</tr>
<tr>
<td>4.4</td>
<td>DC Gain Analysis for VRT Converter Operation in Mode II</td>
</tr>
<tr>
<td>4.5</td>
<td>DC Gain Verification and Comparison</td>
</tr>
<tr>
<td>4.6</td>
<td>Design Example and Efficiency Analysis</td>
</tr>
<tr>
<td>4.7</td>
<td>Experiment Verifications</td>
</tr>
<tr>
<td>4.8</td>
<td>Summary</td>
</tr>
<tr>
<td>5</td>
<td>Low Cost Analog MPPT Controller for Single Chip “MPPT Regulator”</td>
</tr>
<tr>
<td>5.1</td>
<td>Research Motivation</td>
</tr>
<tr>
<td>5.2</td>
<td>New Analog MPPT Controller and Its Operation Principle</td>
</tr>
<tr>
<td></td>
<td>5.2.1. Concept for Single Chip MPPT Solution</td>
</tr>
<tr>
<td></td>
<td>5.2.2. The Truth Table Extracted from P&amp;O Algorithm</td>
</tr>
<tr>
<td></td>
<td>5.2.3. The Storage Cells</td>
</tr>
<tr>
<td></td>
<td>5.2.4. Circuit Diagram of New Analog MPPT and Its Operation Principle</td>
</tr>
<tr>
<td></td>
<td>5.2.5. Requirements for the Analog Multiplier</td>
</tr>
<tr>
<td>5.3</td>
<td>Design Considerations</td>
</tr>
<tr>
<td>5.4</td>
<td>Simulation and Experiment Verifications</td>
</tr>
</tbody>
</table>
5.5. Summary .................................................................................................................. 183

Chapter 6. Conclusions and Future Work ................................................................. 184

6.1. Conclusion of Present Work ............................................................................. 184

6.2. Future Work ....................................................................................................... 185

References ................................................................................................................ 187
LIST OF TABLES

Table 2.1 Summary of the Standards Related to Grid-tied PV Application .............. 12
Table 2.2 Inverter Response to Abnormal Grid Voltage ...................................... 13
Table 2.3 Inverter Response to Abnormal Grid Frequency ................................. 13
Table 2.4 Advantages of Micro-inverters and Module Level Distributed MPPT ...... 26
Table 2.5 Efficiency Data of Micro-inverters ................................................... 29
Table 2.6 Efficiency Data of Distributed MPPT Stage + Centralized Inverter ........ 30
Table 2.7 Inverter Company Global Market Shares (2006 ~ 2009) ...................... 31
Table 2.8 Annual Energy Yield Increase from Partial Shading for Si Module Plant .... 32
Table 2.9 Annual Energy Yield Increase from Partial Shading for High Voltage Thin Film Module Plant ................................................................. 33
Table 2.10 Leakage Current Mean Levels and Response Time ............................ 42
Table 2.11 Leakage Current Comparison Results .............................................. 43
Table 2.12 Comparison between High-Side Active Clamp and Low-side Active Clamp ............................................................................................................. 61
Table 2.13 Summary of AC Module Inverters ..................................................... 65
Table 3.1 Circuit Parameters of Proposed Converter in Simulation and Experiment .. 88
Table 4.1 Comparisons of Two Types of DC MIC Structure ................................. 102
Table 4.2 A Summary of Operation Modes for Proposed Resonant Converter .......... 105
Table 4.3 DC Gain Comparison Between Simulation and Calculation ................. 124
Table 4.4 A List of Parameters of Proposed Converter for Gain Analysis ............ 126
Table 4.5 Comparison of MOSFET Parameters for Prototype Design ................ 129
Table 4.6 Circuit Parameters for Experiment .................................................. 131
Table 4.7 Loss Break-down of Mode II Operation with $10\%P_{\text{rated}}$ ($V_{pv}\leq32V$) .......... 135
Table 4.8 Loss Break-down of LLC Converter with $10\%*P_{\text{rated}}$ ($V_{pv}\leq32V$) ............. 135
Table 5.1 PV Cell Typical Temperature Characteristic ..................................... 153
Table 5.2 Major Characteristics of the Popular MPPT Techniques ....................... 157
Table 5.3 A Summary of P&O Algorithm ....................................................... 161
Table 5.4 Derived Truth Table for Analog Implementation of P&O Algorithm ......... 162
Table 5.5 Circuit Parameters for Simulation ................................................... 176
Table 5.6 A Summary of the Simulation Results .............................................. 177
Table 5.7 Circuit Parameters and Components for MPPT Experiment .................. 178
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 1.1</td>
<td>Global PV Installation</td>
<td>2</td>
</tr>
<tr>
<td>Fig. 1.2</td>
<td>IMS Research Forecasts-Installation Growth in 2011 by System Size</td>
<td>2</td>
</tr>
<tr>
<td>Fig. 1.3</td>
<td>Part of the FREEDM System Diagram</td>
<td>3</td>
</tr>
<tr>
<td>Fig. 1.4</td>
<td>Architecture of KW-MW Scale PV Application with Distributed MPPT</td>
<td>5</td>
</tr>
<tr>
<td>Fig. 2.1</td>
<td>Historical Overview of PV Inverters</td>
<td>18</td>
</tr>
<tr>
<td>Fig. 2.2</td>
<td>Characteristic I-V and P-V Curves against Incident Radiation</td>
<td>20</td>
</tr>
<tr>
<td>Fig. 2.3</td>
<td>Characteristic P-V Curve of PV Panels under Different Conditions</td>
<td>21</td>
</tr>
<tr>
<td>Fig. 2.4</td>
<td>A Picture of Distributed MPPT Stage for Structure in Fig. 2.1 (d)</td>
<td>24</td>
</tr>
<tr>
<td>Fig. 2.5</td>
<td>A Picture of Distributed MPPT Stage for Structure in Fig. 2.1 (e)</td>
<td>25</td>
</tr>
<tr>
<td>Fig. 2.6</td>
<td>A Picture to Demonstrate the AC Module Concept</td>
<td>26</td>
</tr>
<tr>
<td>Fig. 2.7</td>
<td>Sunsil 300 PV Module with Cell Level Nano-converter</td>
<td>28</td>
</tr>
<tr>
<td>Fig. 2.8</td>
<td>Inverter Firm Market Share 2009</td>
<td>31</td>
</tr>
<tr>
<td>Fig. 2.9</td>
<td>Three Types of PV Inverters: (a) Single Stage (b) Dual Stage (c) Dual Stage</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>with Paralleled DC/DC Stage</td>
<td></td>
</tr>
<tr>
<td>Fig. 2.10</td>
<td>Different Locations for the Power Decoupling Capacitor: (a) in Parallel with</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>PV Modules (b) in Parallel with PV Modules or in DC Link</td>
<td></td>
</tr>
<tr>
<td>Fig. 2.11</td>
<td>Single Phase System with Parasitic Capacitances</td>
<td>41</td>
</tr>
</tbody>
</table>
Fig. 2.12 Several Transformerless Inverter Topologies Used for Evaluation .......... 45
Fig. 2.13 Accelerated Test Results in NREL Report ........................................ 47
Fig. 2.14 HBDC Inverter Topology ................................................................. 49
Fig. 2.15 PV Inverter with GCC ................................................................. 50
Fig. 2.16 HERIC Topology ................................................................. 51
Fig. 2.17 H5-Topology ................................................................. 51
Fig. 2.18 Simulation Results to Verify PV Module Side Voltage Fluctuation of HERIC and H5 Topologies ......................................................... 52
Fig. 2.19 Karschny Topology ................................................................. 54
Fig. 2.20 Transformerless Inverter Proposed in [50] ........................................... 54
Fig. 2.21 One Phase Connection of Inverter in [50] ........................................... 55
Fig. 2.22 Two Possible Connections between Inverter and Grid ......................... 56
Fig. 2.23 Common Structure for Multi-string Inverters Without/With a Transformer.... 58
Fig. 2.24 Low-Side Active Clamped Flyback Converter .................................. 60
Fig. 2.25 High-Side Active Clamped Flyback Converter .................................. 61
Fig. 2.26 Several Inverter Topologies for AC Module Application ....................... 64
Fig. 3.1 String Level Distributed MPPT Technology Depicted in Fig. 2.1 (c)............. 69
Fig. 3.2 Circuit Diagram of a Half Bridge LLC Resonant DC/DC Converter ............ 70
Fig. 3.3 DC Gain Characteristic of the Half Bridge LLC Resonant DC/DC Converter... 71
Fig. 3.4 Key Waveforms of LLC Resonant Converter for Three Operation Cases ........ 73
Fig. 3.5 DC Gain Characteristic of a LLC Converter for PV Application ............... 76
Fig. 3.6 Proposed Hybrid Bridge Converter and Its Dual Mode Operation .......... 77
Fig. 3.7 $f_s$ for Different $V_{in}$ under Various Load Conditions of Proposed Converter .... 78
Fig. 3.8 Examples of an Unsafe Mode Transition Versus a Safe Mode Transition .... 79
Fig. 3.9 Controller Structure for Proposed DC/DC Converter ....................... 81
Fig. 3.10 Key Waveforms of Controller for Proposed Converter ....................... 81
Fig. 3.11 Characteristic Curves of a Group of PV Panels .......................... 82
Fig. 3.12 An Example Plot of M Curve in a 3D Plane ............................... 85
Fig. 3.13 Simulation Results: $V_{in}=180V$, $V_o=500V$, $P_o=2kW$, FB Mode .......... 89
Fig. 3.14 Simulation Results: $V_{in}=250V$, $V_o=500V$, $P_o=2kW$, FB Mode .......... 89
Fig. 3.15 Simulation Results: $V_{in}=360V$, $V_o=500V$, $P_o=2kW$, HB Mode .......... 90
Fig. 3.16 Simulation Results: $V_{in}=550V$, $V_o=500V$, $P_o=2kW$, HB Mode .......... 90
Fig. 3.17 Picture of 2kW Solar Inverter Prototype .................................. 91
Fig. 3.18 FB Mode Operation of Proposed Converter: $V_{in}=180V$, $V_o=500V$, $P_o=1kW$ .... 92
Fig. 3.19 HB Mode Operation of Proposed Converter: $V_{in}=360V$, $V_o=500V$, $P_o=1kW$ .... 92
Fig. 3.20 Gate Signals for Proposed Converter during Mode Transition ............. 93
Fig. 3.21 Mode Transition Test Result of Proposed Converter with PV Panel ........ 94
Fig. 3.22 Measured Efficiency of DC/DC Stage ..................................... 95
Fig. 4.17 The Flowchart of Converter Operation after Start-up ............................ 138

Fig. 4.18 A Picture of 240W MIC Prototype .................................................. 139

Fig. 4.19 Waveforms of MIC in Mode I (ch1: 10V/div; ch4: 10A/div; t=4µs) .............. 142

Fig. 4.20 Waveforms Mode II Operation (ch1:50V/div; ch2: 200V/div; ch3: 1A/div; ch4: 10A/div) .................................................. 143

Fig. 4.21 Waveforms to Verify the ZVS Operation in Mode II (ch1:10V/div; ch2: 20V/div; ch4: 10A/div) .................................................. 144

Fig. 4.22 Waveforms to Verify the ZVS Feature of MIC Prototype in Mode II Operation (ch1:10V/div; ch2: 20V/div; ch4: 10A/div) .................................................. 145

Fig. 4.23 Waveforms to Verify the MPPT Function .......................................... 146

Fig. 4.24 Measured Efficiency Improvements with HWR (Mode II) for 5%~50% $P_{\text{rated}}$ ................................................................. 147

Fig. 4.25 Weighted Efficiency Improvements with HWR in Mode II ................. 148

Fig. 4.26 Efficiency Measurement Results for Designed MIC Prototype ............. 148

Fig. 4.27 Weighted Efficiency Data for Proposed MIC Prototype ..................... 149

Fig. 5.1 Simplified Circuit Model for PV Cell................................................. 151

Fig. 5.2 PV Panel Typical Characteristic Curve under Different Irradiance Levels... 153

Fig. 5.3 Distributed MPPT System with the Proposed Analog MPPT Controller ...... 159

Fig. 5.4 Typical P-V Curve of a PV Panel ..................................................... 160
Fig. 5.5 Symbol of XNOR Gate and Its Logic Truth Table ................................. 162
Fig. 5.6 Three Capacitor Based Storage Cell Structures ................................. 163
Fig. 5.7 Circuit Diagram of Proposed Analog MPPT Controller ..................... 167
Fig. 5.8 Timing Diagram of Proposed MPPT Controller ............................... 167
Fig. 5.9 Key Operation Waveforms for the Main Block ................................. 170
Fig. 5.10 Key Operation Waveforms of (a) Control block for Storage Cell I (b) Timer Control Block (c) Control Block for Storage Cell II ................................. 170
Fig. 5.11 An Example of Low Cost Analog Multiplier ................................. 172
Fig. 5.12 Analog MPPT Controller with External Components ..................... 173
Fig. 5.13 Simulation Results from Saber ...................................................... 177
Fig. 5.14 Pictures of the Analog MPPT Controller Based on Discrete Components .... 178
Fig. 5.15 PV Panel Characteristic Curves During the Experiment Test ............. 180
Fig. 5.16 The Experimental Verification of the Analog MPPT Controller Performance ................................................................. 181
Fig. 5.17 Start-up Operation Waveforms of the MPPT Controller .................. 182
Chapter 1. Introduction

1.1 Research Background

The global demand for electric energy has increased continuously over the last few decades. Energy and the environment have become serious concerns in the today’s world [1]. Alternative sources of energy generation have drawn increasing attention in recent years. Among a variety of the renewable energy sources, PV sources are predicted to become the biggest contributors to electricity generation among all renewable energy generation candidates by 2040 [2] [3]. Fig. 1.1 gives the PV installation data for the recent two years and also predicts the installed capacity for each year until 2014 [5]. In 2009, 7.4 GW of new PV capacity was added worldwide and new PV installations grew by a massive 130% to reach 17.5GW in 2010 [5]. Installations in 2011 are expected to increase by a double-digit percentage to reach 20.5GW, culminating a total installed capacity of 58GW by the end of this year [5]. And it is predicted by IMS Research that installations of 35GW in 2014 now look achievable [5].
Fig. 1.1 Global PV Installation

Fig. 1.2 IMS Research Forecasts-Installation Growth in 2011 by System Size [5]
Fig. 1.2 shows the forecasts of installation growth in 2011 by system size. It is predicted that the very large scale utility PV plants will continue to dominate approximately 48% of the market share; small scale PV installations (<10kW) will account for about 33% of the total installation which implies that the residential scale of distributed PV energy generation will become increasingly important and popular with end users in the near future.

Meanwhile, large scale utilization of distributed renewable energy depends upon an advanced smart grid infrastructure where the users have the ability to manage their energy consumption as well as the use of plug-and-generate and plug-and-store energy devices at home and in industrial applications [6][7].

Fig. 1.3 Part of the FREEDM System Diagram [7]
The FREEDM system is an intelligent electric power grid integrating highly distributed and scalable alternative generating sources and storage with existing power systems to facilitate a renewable energy based society [7]. The 400V DC bus in the FREEDM system provides an alternative interface for solar energy. Fig.1.3 shows part of the FREEDM system including an Intelligent Energy Management (IEM) module. As a result, PV converters in FREEDM system need only to have a DC/DC stage to perform Maximum Power Point Tracking (MPPT) and have a proper voltage conversion gain to interface with the DC bus.

The Solid State Transformer (SST) in IEM acts as an “energy hub” to do advanced power flow control as well as DC bus voltage regulation [7]. Generally, this structure has several advantages:

1. Since the SST is the component interfacing with the electric grid, the PV converters’ controller does not require a phase locked loop (PLL), current regulator, or anti-islanding controller. Thus, the control task becomes much simpler.

2. The PV converter can be comprised of a single power stage. Therefore, it is very likely to reduce the system cost for end users.

Obviously, the core technology associated with solar energy harvest in FREEDM system remains the DC/DC converters. In some ways, the PV application in FREEDM system can be categorized into grid-tied PV application.
Moreover, from a system architecture point of view, this application has a similar structure as the advanced KW-MW scale PV application with central inverters (Fig.1.4) [8] [9]:

1. In the advanced central inverter based PV plant, the centralized inverter collects the harvested energy from all the PV strings and delivers it to the grid. In the FREEDM system, energy is delivered to grid by IEM.
In both applications, distributed MPPT (D-MPPT) technology is utilized to optimize the power output for each string (string-level D-MPPT) or even for each PV module (module-level D-MPPT). And the key element associated with the D-MPPT is the DC/DC converter.

Generally, the D-MPPT stage is usually comprised of a single DC/DC power stage with a MPPT controller. And the performance of the D-MPPT stage is critical to both systems. As a result, it becomes very important to research possible high performance solutions for the D-MPPT stage and this is also the key technology associated with the high efficiency power conversion in FREEDM systems.

1.2 Dissertation Outline

This research work focuses on development of high efficiency DC/DC converters as well as high performance power point tracking (MPPT) solution for distributed solar energy conversion in FREEDM systems and various scale PV applications.

The dissertation consists of six chapters. They are organized as follows:

Chapter I introduces background information and the motivation for this research.

Chapter II discusses the roadmap for the development of grid-tied solar inverters at the beginning of this chapter. Then various solar inverter architectures and topologies are
reviewed and evaluated in terms of their efficiency, components count & size and other factors. These inverters are categorized from different points of view, such as the number of power processing stages and whether a transformer is used. Several important standards related to PV applications, i.e., IEEE 1547 [10] and the U.S. National Electrical Code (NEC) [11], are discussed and summarized. Also after the discussion of the requirements from the standards and the panel characteristics, a conclusion is drawn about whether PV panel side grounding is required. The objective of this part of work is to understand the requirements, challenges and new trends for solar energy conversion in the future.

Chapter III proposes a “hybrid bridge” high efficiency resonant DC/DC converter to interface with a string of PV modules whose power rating is usually 2-3kW with a string voltage of 150V ~ 450V DC. This wide operation range is a challenge for converter design and efficiency usually drops. For resonant converters, the tradeoff between efficiency optimization and input range is always there and sometimes the DC gain may not be high enough for the low input voltage case even if the design sacrifices a great deal of efficiency. To address this problem, the proposed “hybrid bridge” converter employs a mode change controller to command the converter to operate in either full bridge (FB) mode or half bridge (HB) mode depending on the PV string input voltage. The mechanism to achieve zero voltage switching (ZVS) in the two operation modes is the same. The proposed converter can be designed to cope with a much narrower operation range and it changes to FB mode when
\( V_{PV} \) drops below a threshold voltage. Therefore, an efficiency-oriented design can be executed and the converter can maintain high efficiency over an extended operation range. Both of the simulation and test results are provided to verify the feasibility of proposed converter. The results show that the experimental prototype’s weighted efficiency can reach 98%.

Chapter IV proposed PV module integrated converters (MICs) as a module-level D-MPPT stage which may result in a significant increase in the annual energy yield of this system. Mainly, there are two kinds of structures for PV-MICs: parallel connected structure and its counterpart, the series connected structure. A thorough comparison between these two structures is presented at the beginning of this Chapter. From the presented analysis, the parallel connected architecture was shown to have more advantages. But the challenge is also obvious: how to achieve high conversion gain with high efficiency. In this Chapter, a variable resonant tank (VRT) high efficiency resonant DC/DC converter is proposed for parallel connected DC MICs. This new topology may adapt resonant modes, depending on the panel operation conditions. By alternating the resonant tank structure, the converter may work at high efficiency in the low \( V_{PV} \) condition and support a 400V DC bus with the help of an added half wave rectifier (HWR). The converter achieves ZVS for primary side switches and zero current switching (ZCS) for secondary side diodes in both resonant modes. The circulation energy is minimized, especially for 5% to 50% of the rated power level. The
operation principle of the proposed converter is explained in detail and a DC gain analysis is presented based on the fundamental harmonic analysis (FHA) method. The performance of the proposed VRT resonant converter was demonstrated on a 240W prototype when $V_{PV}$ varies from 25V to 40V. The prototype’s maximum efficiency reaches 96.5% and an efficiency increase of more than 10% under light load conditions is shown when compared with a conventional LLC resonant converter.

Chapter V proposes a cost-effective analog MPPT controller for a single chip controller solution in the D-MPPT stage. As discussed in Chapter I, The D-MPPT stage is usually comprised of a single DC/DC converter with a MPPT controller. Considering the major control task for the D-MPPT stage is just to regulate the PV side voltage according to the reference from MPPT controller, a low cost analog DC/DC controller IC may be used instead of a dedicated digital controller. Thus, there is a demand for an analog MPPT solution which may be integrated with the existing DC/DC controller chip, for a single chip solution, in order to further reduce the cost. After a review of existing MPPT methods, especially analog MPPT techniques, a new universal analog MPPT controller is proposed. The proposed MPPT solution utilizes several general circuit blocks and it may work with both PWM converters and resonant converters. The operation of proposed MPPT controller is based on a logic truth table extracted from the perturbation and observation (P&O) algorithm. The capacitor based storage cell concept is proposed to store the $V_{pv}$ and $P_{pv}$ in the last perturbation cycle. The
perturbation step size and speed can be adjusted by the user. The operation principle of the new controller is explained and the cost evaluation is presented. The tracking performance of the proposed controller has been validated by both simulation and experimental results from a PV converter with 200W PV panels under different sun irradiation levels and temperatures.

Chapter VI is the summary of present work and a brief introduction of the future work.
Chapter 2. Grid-tied Solar Inverter Technologies: An Overview

2.1 Basic Demands for PV Inverters

Since the grid-tied inverters are interfacing the PV modules with the grid, the standards given by the utility companies must be followed. At present, several particular standards and sections in U.S. National Electrical Code (NEC) [11] put more strict regulations for grid-connected solar inverters. For a solar inverter design, standards EN61000-3-2 (applied in Europe) [14], IEEE1547 [10] and UL1741 [13] are worth considering. A summary of the requirements is listed in Table 2.1.

As seen in Table 2.1, the present EN standard is easier to cope with, regarding current harmonics, than the corresponding IEEE and IEC standards. The requirement on the current harmonics has significant impact on the inverter structure: IGBT/MOSFET-equipped inverters operating at a high switching frequency dominate the inverter markets, other than those inverters with thyristors operating at much lower frequencies. Also these standards put limitations on the maximum allowable amount of injected dc current into the grid. The
purpose is to avoid saturation of the distribution transformers [16].

Table 2.1 Summary of the Standards Related to Grid-tied PV Application [12]

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal power</td>
<td>10 kW</td>
<td>30 kW</td>
<td>16 A × 230 V = 3.7 kW</td>
</tr>
<tr>
<td>Harmonic currents (Order - h) Limits</td>
<td>(3-9) 4.0%</td>
<td>(2-10) 4.0%</td>
<td>(3) 2.30 A</td>
</tr>
<tr>
<td></td>
<td>(11-15) 2.0%</td>
<td>(11-16) 2.0%</td>
<td>(5) 1.14 A</td>
</tr>
<tr>
<td></td>
<td>(17-21) 1.5%</td>
<td>(17-22) 1.5%</td>
<td>(7) 0.77 A</td>
</tr>
<tr>
<td></td>
<td>(23-33) 0.6%</td>
<td>(23-34) 0.6%</td>
<td>(9) 0.40 A</td>
</tr>
<tr>
<td></td>
<td>(~ 35) 0.3%</td>
<td></td>
<td>(11) 0.33 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(13) 0.21 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(15-39) 2.25/h</td>
</tr>
<tr>
<td>Even harmonics in these ranges shall be less than 25% of the odd harmonic limits listed.</td>
<td></td>
<td></td>
<td>Approximately 30% of the odd harmonics -see standard.</td>
</tr>
<tr>
<td>Maximum current THD</td>
<td>5.0%</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power factor at 50% of rated power</td>
<td>0.90</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>DC current injection</td>
<td>Less than 1.0% of rated output current.</td>
<td>Less than 0.5% of rated output current.</td>
<td>&lt; 0.22 A -corresponds to a 50 W half-wave rectifier.</td>
</tr>
<tr>
<td>Voltage range for normal operation</td>
<td>85% - 110% (196 V – 253 V)</td>
<td>88% - 110% (97 V – 121 V)</td>
<td>-</td>
</tr>
<tr>
<td>Frequency range for normal operation</td>
<td>50 ± 1 Hz</td>
<td>59.3 Hz to 60.5 Hz</td>
<td>-</td>
</tr>
</tbody>
</table>

According to IEEE1547 [10], the inverter should respond to abnormal grid conditions
including voltage disturbance and frequency disturbance. Table 2.2 and Table 2.3 below summarizes the required response time for inverters whose power ratings are less than 30kW.

### Table 2.2 Inverter Response to Abnormal Grid Voltage [17]

<table>
<thead>
<tr>
<th>Voltage Range (% of base voltage)</th>
<th>Clearing time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;50</td>
<td>0.16</td>
</tr>
<tr>
<td>50≤V&lt;88</td>
<td>2</td>
</tr>
<tr>
<td>110&lt;V&lt;120</td>
<td>1</td>
</tr>
<tr>
<td>V&gt;120</td>
<td>0.16</td>
</tr>
</tbody>
</table>

### Table 2.3 Inverter Response to Abnormal Grid Frequency [17]

<table>
<thead>
<tr>
<th>Size</th>
<th>Frequency Range (Hz)</th>
<th>Clearing time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>≤30kW</td>
<td>&gt;60.5</td>
<td>0.16</td>
</tr>
<tr>
<td></td>
<td>&lt;59.3</td>
<td>0.16</td>
</tr>
<tr>
<td>&gt;30kW</td>
<td>&gt;60.5</td>
<td>0.16</td>
</tr>
<tr>
<td></td>
<td>{59.8-57.0} adjustable set-point</td>
<td>adjustable 0.16 to 300</td>
</tr>
<tr>
<td></td>
<td>&lt;57.0</td>
<td>0.16</td>
</tr>
</tbody>
</table>

The inverter should also be able to detect an islanding situation and take proper measures in order to protect people and equipment. Islanding is the continued operation of the inverter when the grid has been removed; on purpose, by accident or because of damage [12]. The available detection schemes normally fall into two groups: active detection methods and passive detection methods [18] [19]. Basically the passive method does nothing more to the grid than monitor grid parameters. On the contrary, the active schemes introduce a
disturbance (usually a current injection) into the grid and monitor the corresponding effect. This may affect the power quality and produce problems when large numbers of inverters are connected with the grid in parallel [18] [19]. IEEE Std.929-2000 [20] and IEEE Std. 1547 [10] both define several requirements for anti-islanding purposes. Several passive and active methods have been analyzed and tested in [18] and [19]. A drawback shared by all of these methods (except for the communication based ones) is that their successful detection rate is heavily load dependant and they may fail under certain load conditions. Only the communication based method is load independent. Considering that almost all of the solar inverters on the market have the communication capability, the cost to implement the communication based anti-islanding method into the inverter may be negligible. But a central monitoring system may be required to monitor the status of the grid and send out the commands to the solar inverters within range.

The NEC 690 standard [11] deals with the grounding requirement for grid-connected PV systems. In NEC before 2005, un-grounded PV systems are not allowed in U.S. for residential application if the system has a voltage over 50 volts [12] [21]. The 2005 version NEC [11], ungrounded photovoltaic systems claim to meet the U.S standards for residential application when a number of conditions are met, such as, over-current protection and disconnects on all circuit conductors, ground-fault protection on all systems, etc [11] [21]. This change implies certain transformer less inverters can be sold on the U.S. market and
this may have significant impact on inverter design. These effects will be discussed later in this chapter.

For grid-connected inverters, there are two basic requirements for their functions: one is to ensure that the PV module(s) operates at the maximum power point; the other is to inject a sinusoidal current into the grid. In addition, inverters’ efficiency is quite an important index to evaluate an inverter’s performance. Usually efficiency is calculated according to the definition of European efficiency below:

\[
\eta_{EU} = 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} + 0.1 \cdot \eta_{50\%} + 0.48 \cdot \eta_{50\%} + 0.2 \cdot \eta_{100\%}
\]  

(2.1)

Another popular method to evaluate efficiency is based on the California Energy Commission (CEC) weighted efficiency formula:

\[
\eta_{CEC} = 0.04 \cdot \eta_{10\%} + 0.05 \cdot \eta_{20\%} + 0.12 \cdot \eta_{30\%} + 0.21 \cdot \eta_{50\%} + 0.53 \cdot \eta_{75\%} + 0.05 \cdot \eta_{100\%}
\]  

(2.2)

Where the index value is equal to the percent of rated power [22]. For both calculation methods, the purpose for performing the six operating point efficiency calculation is to make a fair comparison of the inverters, under partial load conditions.

The end users of the PV systems demand cost effective inverters which should also have
high efficiency over a wide range of input voltage and input power since these variables are defined in very wide range as functions of solar irradiation and ambient temperature [12]. At present, inverters represent about 8% of the cost of a solar installation, a significant portion [23]. The small size inverter (below 5kW) pricing is in the $0.8 to $1.0 per Watt range. Large size inverter pricing is about half of that [23]. Furthermore, the inverter must be highly reliable (long operational lifetime) since most PV module manufacturer offer a warranty of 25 years on 80% of initial efficiency, and a materials and workmanship warranty of five years [25]. The main limiting components inside the inverters are the electrolytic capacitors used for power decoupling between the PV module and the single-phase grid [26]. The operational lifetime for electrolytic capacitors can be estimated by the capacitor vendor’s lifetime curve or equations. Generally, the ripple current through the capacitor, voltage stress on capacitor, and operation temperature all have effect on its lifetime. Using de-rating factors during the inverter design or using non-electrolytic capacitors can lead to a longer lifetime inverter, but usually also increases the cost. Another lifetime limitation component in the system is the cooling fan. Commercialized fan products can meet the 10 year lifetime requirement but it’s difficult to extend its lifetime to 20+ years [27]. Therefore, it’s very important to reduce the heat generated from inverter circuitry such that the inverter may control the temperature rise by natural convection cooling without the cooling fan. At present, a large portion of solar inverter products on the market utilize advanced low loss power
devices, soft switching techniques, and larger size heat-sinks to control the temperature rise, rather than using a fan.

2.2 Evolution of PV Converters: Past, Present and Future

The PV converter technology has a history of over half a century and is the key technology to power up satellites through PV panels in the aerospace application. In recent years, it has received considerably increasing attention worldwide due to the large demand for high efficiency solar energy application. There is a large amount of published literature related to PV converter technology.

Fig.2.1 illustrates a roadmap of the development of PV inverters. The past technology was based on single centralized inverters that interfaced with a large group of PV modules [28]. Large amounts of PV modules are connected in series and parallel to form PV arrays which have sufficiently high voltage and reach high power levels.
Fig. 2.1 Historical Overview of PV Inverters: (a) Centralized Technology; (b) String Technology; (c) Multi-string (String Level Distributed MPPT) Technology; (d) (e) Module Level Distributed MPPT Technology; (f) AC Module Technology
The power rating of this centralized inverter is usually in the range of hundreds of KW or even MW. The centralized inverter usually has two kinds of DC bus voltage: 575V or 750V, depending on the grid side voltage. The advantage of this technology is the inverter’s high conversion efficiency and low cost per watt of produced electricity. However, this structure has several well known drawbacks, such as PV module mismatch losses, less flexibility to deal with partial shading and soiling conditions. In general, this architecture does not extract the maximum available energy that can be generated by the PV modules due to these drawbacks. The highest energy output is achievable only when all of the PV modules are exactly the same and the sun irradiation seen by each PV module is equal. Unfortunately, these conditions may never be met in practical solar applications due to variations of PV module parameters caused by temperature, aging and dust on the surface of modules. Also, partial shading caused by clouds, trees, and obstacles cannot be avoided completely. As a result, energy loss is relatively high in such a system, although the centralized inverter itself has a very attractive high efficiency.

Fig. 2.2 shows the typical characteristic curves of a PV panel. For a large group of panels, their P-V curve may become very complex in partial shading conditions, as shown in Fig. 2.3. In addition to the global MPP (GMPP), it is possible that several local MPPs (LMPPs) may appear, hence the MPPT controller may not find the real MPP in practice. In this case, advanced MPPT algorithms may need to be implemented. These are usually complicated and
will increase the complexity and cost of the system.

![Characteristic I-V and P-V Curves against Incident Radiation](image)

**Fig. 2.2 Characteristic I-V and P-V Curves against Incident Radiation**

In the past, the grid-connected stage was usually line commutated by means of thyristors, resulting in poor power quality [12]. At present, the centralized inverters are still available on the market and they still dominate the utility scale solar applications. The popularity of centralized inverter in this specific application is due to the fact that the utility scale solar plant is usually built in an open field without obvious obstacles for shading the PV panels. Thus, partial shading caused by trees, chimneys and other buildings is not likely to happen. However, the partial shading created by cloud pattern still exists.
Fig. 2.3 Characteristic P-V Curve of PV Panels under Different Conditions

The present PV inverter technologies consist of the following: the string inverters (Fig. 2.1 (b)), the multi-string inverters (Fig. 2.1 (c)), the series/parallel connected power optimizer with centralized inverter (Fig. 2.1 (d) and Fig. 2.1 (e)), and the ac modules (Fig. 2.1 (f)).

As shown in Fig. 2.1(b), the string inverter is a reduced version of the centralized inverter, where only a single string of PV modules is connected to the inverter [16]. No string diodes are required in this case and separate MPPTs can be applied to each string. The string inverter is a common solution for commercial and residential level PV applications. Usually the string inverter contains only a single power stage since the string voltage is high enough for the
inverter to interface with the electric grid. However, the negative effect of leakage current for the single stage solution should be evaluated in some cases. In practice, either advanced topology (i.e., H5 topology from SMA Inc) [29] or a low frequency transformer is used to solve the leakage current issue. More detailed discussion about leakage current’s impact on PV inverter design is presented in the next section.

The PV converter system structure shown in Fig. 2.1 (d), also known as the multi-string inverter, may increase year-round power generation in commercial or utility scale applications by taking advantage of string level distributed MPPT technology. A DC/DC converter is connected to a string of PV modules to fulfill the MPPT control for that string. The string level MPPT is achieved and it ensures that the negative effects of module shading, soiling, and aging mismatch, are minimized and contained within the string [30]. The DC/DC converter for each string may also boost the voltage to a higher level to allow the inverter to operate more efficiently. It is claimed that for this structure, the balance of system expense (BOS) may be reduced by 20-25% while gaining greater design flexibility [30]. Moreover, this solution is widely used in utility scale applications and it is receiving more attention from those solar inverter companies whose main products are high power centralized inverters.

As shown in Fig. 2.1 (d) and Fig. 2.1 (e), the module level distributed MPPT technology has two types of connections: series connected structures and parallel connected structures.
The DC/DC converters in both types of structures may be called PV module integrated DC/DC converter (DC MIC). And particularly, the DC/DC converters in series connected structures are usually called solar power optimizers [31]. As shown in Fig. 2.1 (d), several DC MICs must form a series connection to obtain a voltage high enough for interfacing with the DC bus of the centralized inverter. The output current of the series connected DC MICs in a string remains the same. But their output voltage varies based on the amount of energy they can deliver. Assume only two DC MICs in series supporting DC bus in Fig. 2.1 (d), the following equations are valid:

\[ V_{BUS} = V_1 + V_2 \]  
\[ P_{total} = V_{BUS} \times I = P_1 + P_2 = (V_1 + V_2) \times I \]

Where, I is the output current of MICs in this string; the \( P_{total} \), \( P_1 \) and \( P_2 \) represent the total generated power, output power of MIC 1 and output power of MIC 2, respectively. Apparently, the output voltage of MIC 1 and MIC 2 is proportional to its output power:

\[ \frac{V_1}{V_2} = \frac{P_1}{P_2} \]

Further, for MIC 1,2,… N in a string, their output voltage meets the following equation:
\[ V_1 : V_2 : \ldots : V_N = P_1 : P_2 : \ldots : P_N \] (2.6)

For the paralleled structure in Fig. 2.1 (e), multiple parallel connected MICs may interface with the DC bus directly. The basic requirement for MICs in this structure is that they need to have high conversion gain to support the DC bus considering the voltage for the single PV module is low. Fig. 2.4 and Fig. 2.5 present the pictures of both kinds of DC MICs products from Tigo Energy Inc.

Fig. 2.4 A Photograph of Distributed MPPT Stage for Structure in Fig. 2.1 (d) [32]
Generally, both series and parallel structures provide high flexibility in system design. The module level MPPT may greatly reduce the loss from partial shading and panel mismatch. Thus, optimized operation for each PV module may ensure the achievement of much better energy gain in practice. On the other hand, the two structures also differ in many ways and they have different features. A detailed analysis and comparison of their characteristics will be given in Chapter 4.

The ac module depicted in Fig. 2.1 (f), also known as micro-inverter, is the integration of the inverter and PV module into one electrical device for a “plug and play” solution [16]. Fig.2.6 shows a photo of the micro-inverter product from Enercsys Inc.
Table 2.4 Advantages of Micro-inverters and Module Level Distributed MPPT [23]

<table>
<thead>
<tr>
<th>MICROINVERTERS</th>
<th>DC-TO-DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>No specialized DC wiring or high-voltage components</td>
<td>Higher voltages=lower resistive losses in copper</td>
</tr>
<tr>
<td>Strong monitoring capabilities</td>
<td>Strong monitoring capabilities</td>
</tr>
<tr>
<td>No single point of failure</td>
<td>Not necessary on every panel</td>
</tr>
<tr>
<td>Enables DIY home owner and consumer sales channels</td>
<td>High efficiency</td>
</tr>
<tr>
<td>Reduces cost of installation</td>
<td></td>
</tr>
</tbody>
</table>

The main challenge for an AC module is to amplify the lower voltage to a proper level for the grid in a more efficient way [12]. With the remarkable improvement of their conversion efficiency in recent years, micro-inverters become very attractive for residential and commercial PV applications and as a result, they become the major competitor for string
inverters. Moreover, with continuous research effort and more companies entering this business field, the cost of micro-inverters is expected to decrease in the near future. Table 2.4 summarized the advantages of both micro-inverters and module level distributed MPPT technology.

The future technologies of PV inverters are a further extension of the development of present technologies, particularly, the PV converter structure (c), (d), (e), (f) in Fig. 2.1. The structure (c) may dominate the utility scale and commercial scale of PV applications in the future. The structure (d), (e) and (f) may receive large market shares in the residential and small commercial PV applications. Although it is hard to conclude which type of structure will prevail and dominate the market in the long run, it is pretty clear that the trend for PV converter technology is trying to squeeze out more energy from PV modules and reduce avoidable power loss. Although structure (c) has superior performance compared with conventional centralized structure, the system design and installation is still complex and expensive, requiring the installation site without any obvious obstacles and the PV modules in string should face the sun in a unified format. In such a system, maximum energy harvesting occurs only when every module in a string is matched exactly and the same amount of solar radiation reaches each solar cell in very module. From this point of view, this technology is realistically not a promising solution.

On the contrary, the module level MPPT and the newly emerged cell level MPPT
technologies are promising for future PV applications. The cell-level MPPT began to capture the public’s attention in the year 2010. Figure 2.7 shows the Sunsil’s 300W PV module with integrated micro-inverter and cell-level nano-converter. The concept behind this product is very similar to that of the micro inverter: plug-and-play. This PV module consists of 48 cells, divided into 12 groups. Each group of cells, has its own MPPT controller and, as a result, the operation of each group may be optimized. The conversion efficiency data and price for this solution are not published yet. But these data are key factors in determining whether this new solution may succeed on the market. Moreover, the reliability of the nano-converter may be a bottleneck for the entire system. In the case where one of 12 nano-converters fails, the user has to discard the entire PV module because the nano-converter is implanted into the module and it is not replaceable.

Fig. 2.7 Sunsil 300 PV Module with Cell Level Nano-converter [34]
Considering that conversion efficiency is a primary concern for solar energy applications, it is worthwhile to compare the efficiency of these promising solutions. Table 2.5 and Table 2.6 summarize the efficiency data based on datasheet of inverter products categorized in structures (c) ~ (f). Some companies in this area, like Tigo Energy Inc, Accurate Solar Inc and MPPC Inc, are not listed in the table because the efficiency data for their products are not published. In addition, the communication methods implemented in different micro-inverter products are also listed in Table 2.5.

Table 2.5 Efficiency Data of Micro-inverters

<table>
<thead>
<tr>
<th>Micro Inverter</th>
<th>Company</th>
<th>P_{\text{rated}} (W)</th>
<th>\eta_{\text{SYS}} (CEC/EU)</th>
<th>Communication Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enphase</td>
<td>230/240</td>
<td>96%</td>
<td></td>
<td>Powerline Carrier</td>
</tr>
<tr>
<td>Eneecsys</td>
<td>200/240/280</td>
<td>94%</td>
<td></td>
<td>Wireless IEEE. 15.4</td>
</tr>
<tr>
<td>Solar Bridge</td>
<td>235</td>
<td>94.2%</td>
<td></td>
<td>Powerline Carrier</td>
</tr>
<tr>
<td>Petra Solar</td>
<td>200</td>
<td>93%</td>
<td></td>
<td>Zigbee based Cellular Network</td>
</tr>
</tbody>
</table>

From Table 2.6, module level DMPPT solution has similar \( \eta_{\text{SYS}} \) as the string level DMPPT solution. Another conclusion is that the micro inverters have a lower efficiency compared
with the DMPPT + Centralized Inverter solution. For the recently released Enphase products, their efficiency is about only 0.5% lower than the distributed MPPT solution.

Table 2.6 Efficiency Data of Distributed MPPT Stage + Centralized Inverter

<table>
<thead>
<tr>
<th>Company (DMPPT)</th>
<th>Company (Inverter)</th>
<th>Structure</th>
<th>$P_{\text{rated, DMPPT}}$ (W)</th>
<th>$\eta_{\text{DMPPT}}$ (CEC/EU)</th>
<th>$\eta_{\text{INV}}$ (CEC/EU)</th>
<th>$\eta_{\text{SYS}}$ (highest)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Satcon SMA/ PV</td>
<td>Powered/ Satcon Inc</td>
<td>Fig. 2.1 (c)</td>
<td>2.2K/2.9K</td>
<td>98.5%</td>
<td>97% ~</td>
<td>96.5%</td>
</tr>
<tr>
<td>Solar Edge</td>
<td>Fig. 2.1 (d)</td>
<td>250/350</td>
<td>97.8%</td>
<td>98%</td>
<td>95.8%</td>
<td></td>
</tr>
<tr>
<td>Azuray Solar Magic</td>
<td>Fig. 2.1 (e)</td>
<td>230</td>
<td>98.5%</td>
<td>96%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 2.8 below gives the inverter firm market share 2009 and Table 2.7 gives the global inverter market share data from 2006 to 2009. The micro inverter began to seize market share from 2009 and its market share is expected to grow continuously in the future with the improvement of its efficiency and reduction of cost. Meanwhile, the utility scale centralized inverter will continue to dominate the market and will become increasingly attractive through integration of the string/module level distributed MPPT technologies.
Fig. 2.8 Inverter Firm Market Share 2009 [23]

Table 2.7 Inverter Company Global Market Share (2006 ~ 2009) [23]

<table>
<thead>
<tr>
<th>Inverter Manufacture</th>
<th>2006 MS%</th>
<th>2007 MS%</th>
<th>2008 MS%</th>
<th>2009 MS%</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMA</td>
<td>24%</td>
<td>33%</td>
<td>38%</td>
<td>40%</td>
</tr>
<tr>
<td>Ingeteam</td>
<td>3%</td>
<td>10%</td>
<td>6%</td>
<td>6%</td>
</tr>
<tr>
<td>Kaco</td>
<td>6%</td>
<td>7%</td>
<td>8%</td>
<td>8%</td>
</tr>
<tr>
<td>Fronius</td>
<td>10%</td>
<td>9%</td>
<td>8%</td>
<td>8%</td>
</tr>
<tr>
<td>Enphase</td>
<td>NA</td>
<td>NA</td>
<td>0%</td>
<td>1%</td>
</tr>
</tbody>
</table>
2.3 Energy Yield Comparison of Different PV Inverter Technologies

The Energy yield is the key metric to compare the performance of different PV inverter technologies. Previous discussion pointed out that the distributed MPPT technologies may lead to lower conversion efficiency. However, placing the MPPT control at each module maximizes the power extraction and this begins to decrease as we move the MPPT closer to the central inverter. For systems with longer strings of series modules, partial shading has a more significant impact on the total generated power as compared to massively paralleled plants with high voltage PV modules, i.e., tandem amorphous silicon modules ($V_{OC} \sim 240V$) [24]. Also the annual energy yield increase by using distributed MPPT technologies is analyzed and quantified for several case studies in [24]. Table 2.8 ~ Table 2.9 gives the annual energy yield increase from partial shading for PV plants which consist of two types of PV modules: low voltage Si module or high voltage thin film module.

Table 2.8 Annual Energy Yield Increase from Partial Shading for Si Module Plant [24]

<table>
<thead>
<tr>
<th>MPPT Location</th>
<th>Central DC/DC Converter</th>
<th>String Combiner</th>
<th>String</th>
<th>Module</th>
<th>System Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy (kWh)</td>
<td>2,675,055</td>
<td>2,681,674</td>
<td>2,692,368</td>
<td>2,698,570</td>
<td>Phoenix, AZ</td>
</tr>
<tr>
<td>% Yield Increase</td>
<td>-</td>
<td>0.25%</td>
<td>0.65%</td>
<td>0.88%</td>
<td>Phoenix, AZ</td>
</tr>
<tr>
<td>% Yield Increase</td>
<td>-</td>
<td>0.43%</td>
<td>1.10%</td>
<td>1.50%</td>
<td>Newark, NJ</td>
</tr>
</tbody>
</table>

32
Table 2.9 Annual Energy Yield Increase from Partial Shading for High Voltage Thin Film Module Plant [24]

<table>
<thead>
<tr>
<th>MPPT Location</th>
<th>Central DC/DC Converter</th>
<th>Array Combiner</th>
<th>String Combiner</th>
<th>String Module</th>
<th>System Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy (kWh)</td>
<td>2328391</td>
<td>2336349</td>
<td>2338915</td>
<td>2338915</td>
<td>Phoenix, AZ</td>
</tr>
<tr>
<td></td>
<td>1704986</td>
<td>1715765</td>
<td>1719167</td>
<td>1719167</td>
<td>Newark, NJ</td>
</tr>
<tr>
<td>% Yield Increase</td>
<td>-</td>
<td>0.34%</td>
<td>0.45%</td>
<td>0.45%</td>
<td>0.54%</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>0.63%</td>
<td>0.83%</td>
<td>0.83%</td>
<td>1.01%</td>
</tr>
</tbody>
</table>

Where the “array combiner”, “string combiner”, “string” and “module” mean to different MPPT locations. For example, if several PV arrays share a common MPPT, this arrangement is called “array combiner”. Similarly, if each PV string has its own MPPT, it is marked “string” in the table above.

The data in these table clearly show that by using distributed MPPT technologies, the annual energy yield increases in the range of 0.25% ~1.5% and for the plant with low voltage modules, the energy gain is even larger. This is because more low voltage modules are required to form a string with a designed output voltage rating. And one key advantage of using distributed MPPT technologies is the increased availability of a power plant, since a failure in a single DC/DC converter does not lead to a complete plant shutdown [24].

Other factors affecting energy yield include:

- Cable loss, which may account for up to 0.5% of extra energy gain by using string
level distributed MPPT.

✧ Module mismatch, which may account for 0.5% ~ 1% gain in energy yield for distributed MPPT.

✧ Converter efficiency. The drop in energy yield due to lower power conversion efficiency is estimated to range from 0.2% at the string combiner level to 1.9% for module level distributed MPPT.

✧ MPPT algorithm, which may account for up to 2% of extra energy gain by moving it to a module converter.

Adding the different factors that affect the energy yield, it is concluded in [24] that an energy gain in the range of 4% ~ 12% can be obtained for distributed MPPT technologies over central inverter systems. And the range is dependent on the geographic location of the plant which has a great effect on its operation. Generally the selected distributed MPPT architecture needs to generate enough energy yields in order to compensate for the increased cost for implementing the distributed MPPT technology.
2.4 Category of PV Inverter Topologies

PV inverter topologies can be categorized in terms of the number of power processing stages and whether a high frequency (HF) or low frequency (low frequency) transformer is utilized or not.

2.4.1. Number of Power Processing Stages

Fig. 2.9 depicted basic structure of single stage and multiple stage inverters.

Fig. 2.9 Three Types of PV Inverters: (a) Single Stage (b) Dual Stage (c) Dual Stage with Paralleled DC/DC Stage [12]

The inverter of Fig. 2.9 (a) is a single-stage inverter, which must handle all the control tasks by itself, i.e., MPPT control, grid current shaping and, for some, voltage amplifications. Assuming that both the grid and grid current only contain the fundamental component and they are in phase due to current control, the instantaneous power injected into the grid may
be calculated by:

\[ p_{\text{grid}} = 2 \cdot P_{\text{grid}} \cdot \sin^2(\omega_{\text{grid}} t) \]  

(2.7)

Where \( P_{\text{grid}} \) is the average injected power, \( \omega_{\text{grid}} \) is the angular frequency, and \( t \) represents time. Since the \( p_{\text{grid}} \) varies at a frequency \( \omega_{\text{grid}} \) and has a peak value of \( 2 \cdot P_{\text{grid}} \), the inverter must be designed to handle a peak power level of twice the nominal power, according to equation (2.7). This structure is the typical configuration for a centralized inverter. At a certain maximum power point, since the power from the PV module is expected to be constant but the power delivered to the grid varies at a frequency of \( 2 \omega_{\text{grid}} \), power decoupling capacitors must be added somewhere in the system. Fig. 2.10 shows possible power decoupling capacitors position in a system.

![Fig. 2.10 Different Locations for the Power Decoupling Capacitor: (a) in Parallel with PV Modules (b) in Parallel with PV Modules or in DC Link [12]](image)

Basically the size of the decoupling capacitor can be expressed as

\[ C = \frac{P_{\text{pv}}}{2 \cdot \omega_{\text{grid}} \cdot U_c \cdot \dot{u}_c} \]  

(2.8)
Where $P_{pv}$ is the nominal power of the PV modules, $U_C$ is the mean voltage across the capacitor, and $\hat{u}_C$ is the allowed amplitude of the ripple voltage. Equation (2.8) is based on the fact that the current from the PV modules is pure dc and the current drawn from the grid-connected inverter follows a $\sin^2(\omega_{grid}t)$ waveform, assuming $U_C$ is constant. Therefore, having a higher $U_C$ and larger allowable voltage variation at this decoupling capacitor is beneficial to reduce the required capacitor size and extend the inverter’s lifetime.

For a single stage inverter, $C_{PV}$ is the decoupling capacitor. In order to extract the maximum possible energy from the PV modules, PV side voltage should be maintained at MPPT and does not allow for a large variation. Moreover, the single stage solution usually has a lower mean voltage on its decoupling capacitor $C_{PV}$ than the two stage solution where the DC link capacitor $C_{DC}$ is chosen as the decoupling capacitor. These factors limit the capacitor size reduction in the single stage inverter. For example, if $U_{mpp}=360V$, $\hat{u}_C$ is 2%*$U_{mpp}=7.2V$, $P_{mpp}=2200W$, a $C_{PV}$ of 1.15mF is required. On the contrary, if the capacitor is placed in the dc link in two stage inverter ($C_{DC}$ in Fig. 2.10), it becomes 290µF at 500V with $\hat{u}_C=20V$ (peak-peak voltage ripple). The capacitor for the latter case is only 1/4 of the former case.

Fig. 2.10 (b) depicts a two stage inverter. The dc-dc converter is performing the MPPT. Depending on the control of the inverter, the output from the dc-dc converter is either a pure dc current or its output current is modulated to follow a rectified sin wave which is usually in phase with grid voltage. In the former case, the dc-ac stage aims to shape the output current
into sinusoidal waveform through SPWM modulation or space vector modulation [35] and the decoupling capacitor is usually placed at the DC link side. In the latter case, the dc-dc converter should be designed to handle a peak power of twice the nominal power; the required decoupling capacitor size is usually much larger since these capacitors are located at the PV module side (similar to the single stage inverter case). Obviously, there is no real DC bus at the DC link side for this case.

2.4.2. Transformers and Grounding

For commercial PV inverters, some of them utilize a transformer (either a high frequency transformer or a line frequency transformer). The transformer is a paradox inside the PV inverters. The answer to the question whether the transformer is required can have three aspects:

- For the inverter itself: adding a transformer can be helpful to boost input voltage to a proper value when the input voltage is extremely low, such as in the AC module application; whereas the transformer is superfluous when the input voltage is sufficiently high.

- Regarding the standards requirement: none of the standards related to the PV system specify whether or not an electrical isolation between the PV modules and the grid is necessary. But several of these standards deal with grounding, such as European standards and NEC690. In fact, if grounding of the negative conductor of PV module is required, the
most straightforward solution is to add a transformer.

It should be pointed out that the grounding requirement for Europe and the U.S is different. Floating PV systems are allowed in Europe and the filed application records show that such floating system is as safe as other grounding systems [21]. Usually a ground fault protection device (GFPD) is required for both the photovoltaic source and the output circuits. This device can detect a ground fault and automatically disconnects the conductors and /or shuts off the utility-interactive inverter or charge controller for that portion of the faulted array [11]. In the U.S. market, transformerless inverters are rare, particularly before 2005, since NEC690 (before 2005) requires all the PV systems should be grounded. It clearly pointed out that for residential applications, one of the conductors from the PV modules to the inverter circuit should be grounded. Since the neutral of either split phase transformer or 3-phase distribution transformer is grounded, one of the inverter’s output conductors connected with the grid is grounded when the inverter interfaces one phase in both cases. This kind of connection may bring trouble for the inverter design since a normal full-bridge inverter cannot be used as grid phase if there is not a transformer somewhere in the system. A few transformerless topologies can be grounded both at the input and at the output. These topologies will be discussed later.

As stated earlier, NEC690 2005 version has made changes in the grounding requirement: section 690.35 claims ungrounded PV system shall be allowed in U.S. only if it can meet
several conditions. These changes further confirm that un-grounding PV system can be safe. Therefore from the standards point of view, grounding is no longer a requirement for the PV inverter design.

✧ For the PV panel: basically, PV panels in the present market can be categorized into two types: Si crystalline type and thin film type. The crystalline type includes mono-crystal silicon and poly-crystal silicon. The mono-crystal technology is the oldest and its typical conversion efficiency is around 16%. Poly-crystal panels are widely used in today’s PV applications and its efficiency is approximately 15%. Compared with a crystalline panel, the thin film panel is less difficult to manufacture and exhibits relatively lower energy consumption. Thus the cost for manufacture of a thin film panel is lower than that of a crystalline one. Currently, thin film technology is more attractive and is expected to be used widely in the future after improvement of its conversion efficiency [36].

Since the PV inverter is the interface between the PV panels and the grid, the panel features must be taken into account during the inverter design. The main requirement is that the PV inverter circuitry can operate with the PV panel properly and cannot impose negative effect on PV panels. The primary concern is that the leakage current flowing through the cells to the ground may shorten the PV module’s lifetime and produce some other problems [37][38]. As shown in Fig. 2.11, between the PV array positive/negative conductors and the ground (or the metallic frame because frame must be grounded), there is parasitic capacitance
\((C_{p1}, C_{p2})\) whose value is in the range of 50-150nF/kW, depending on the weather conditions and panel structure [37].

In Fig. 2.11, the \(V_{PV^+}\) and \(V_{PV^-}\) represents voltage potential applied to the positive and negative conductors of the PV module. Although the differential voltage across the two conductors is constant DC in steady state, the \(V_{PV^+}\) and \(V_{PV^-}\) themselves are not constant voltage. Instead, \(V_{PV^+}\) and \(V_{PV^-}\) may vary and contain high frequency components which are highly dependent on the inverter circuit topologies and modulation methods. In other words, there is dv/dt between the module conductors and module frames since the frame is always firmly grounded. The leakage current can be calculated by the equations below:

\[
i_{\lambda 1} = C_{p1} \cdot \frac{d(V_{PV^+})}{dt}
\]  (2.9)
\[ i_{l2} = C_{p2} \frac{d(V_{pv})}{dt} \]  

(2.10)

Apparently, once a high enough \( \frac{dv}{dt} \) exists on the two conductors of PV module, a high leakage current will be induced which may flow between conductors and the ground. If the leakage current is sufficiently high, the GFPD may be triggered. Table 2.10 below gives the GFPD response time required by DIN VDE0126-1-1.

<table>
<thead>
<tr>
<th>Leakage Current Average Value (mA)</th>
<th>Disconnect Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>0.3</td>
</tr>
<tr>
<td>60</td>
<td>0.15</td>
</tr>
<tr>
<td>100</td>
<td>0.04</td>
</tr>
</tbody>
</table>

Table 2.10 Leakage Current Mean Levels and Response Time [38]

To limit the leakage current as well as to avoid the potential problems arises from high leakage current, the following solution may be considered:

- Grounding one of the conductors of PV module. For most PV modules, the negative conductor may be grounded. The grounding may bring two advantages. First, the parasitic capacitance \( C_{p2} \) is eliminated. Second, the \( \frac{dv}{dt} \) on the positive conductor can be greatly reduced because it is only related to the voltage ripples on the PV side filter capacitor \( C_{pv} \). In an ideal case (i.e., \( C_{pv} \) size is infinite large), the \( \frac{dv}{dt} \) should go to zero. In practice, its value becomes rather small, hence the leakage current.
Eliminate or reduce the $dv/dt$ applied to the parasitic capacitors. This may be achieved by elimination/reduction of the high frequency components in $V_{PV+}$ and $V_{PV-}$.

Generally, both solutions mentioned above are based on modification of the inverter circuit. To achieve the PV module side grounding, adding a transformer is a common solution otherwise advanced transformerless inverter topologies with grounding capability need to be developed. Similarly, in order to eliminate/reduce the $dv/dt$, advanced new inverter topologies are required.

<table>
<thead>
<tr>
<th>Table 2.11 Leakage Current Comparison Results [37]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
</tr>
<tr>
<td>----------</td>
</tr>
<tr>
<td>Nr. Of Input Capacitors</td>
</tr>
<tr>
<td>Nr. Of Switches</td>
</tr>
<tr>
<td>Bypass Diodes</td>
</tr>
<tr>
<td>DC to Ground voltage (peak value and frequency)</td>
</tr>
<tr>
<td>Leakage Current (peak values)</td>
</tr>
</tbody>
</table>

Several transformers-less inverter topologies have been investigated in [37] to evaluate their leakage current and the voltage imposed at the PV module conductors. Fig. 2.12 below shows topologies evaluated in [37] and Table 2.11 summarized the evaluation results.

Where, $FB$ bip: Full Bridge Inverter with Bipolar Modulation; $FB$ unip: Full Bridge Inverter with Unipolar Modulation; $NPC$: Neutral-Point-Clamped Multilevel Inverter; $3FB$: 3-phase
Full Bridge Inverter; 3xNPC: 3-phase NPC Inverter; 3xHB: 3-phase Half Bridge Inverter.

Fig. 2.12 (a) Full Bridge Topology

Fig. 2.12(b) NPC Inverter

Fig. 2.12(c) Three-phase Full-Bridge (FB) topology
All of these simulations/experiments are based on the same filter parameters. The switching frequency and the grid were set to be pure sinusoidal. As detailed in Table 2.11, the
single phase full-bridge topology can only use bipolar PWM strategy because using unipolar switching will produce $\pm V_{dc}$ voltage jump at the switching frequency on the PV module conductors, generating high leakage currents. Same results have been seen on the 3-phase FB. Better results are achieved with NPC, 3xNPC and 3xHB because of the grounding of the middle point of the input capacitors. In this case, the voltage fluctuation is reduced to only several volts [37].

Further studies have shown that more attention should be put onto those applications with thin film PV modules since these types of PV modules are much more sensitive to the leakage current [39]. This is because of the lack of additional isolation from the outside environment afforded by the “ethylene vinyl acetate” (EVA) encapsulate between the Si solar cells and the top glass sheet [40]. Researchers in NREL applied voltage, water vapor and light stresses to thin-film PV modules with SnO$_2$F transparent conducting oxides (TCOs) deposited on the soda-lime glass super-stratum and evaluated the corrosion of the thin-film layers under different conditions.

In the NREL’s test, two identical a-Si modules were placed into an environmental chamber set for an ambient temperature of 85 degrees Celsius and a relative humidity (RH) of 85%. With the output leads of the modules shorted, $+600V$ relative to the aluminum frame was applied to one module and $-600V$ to the other module. Results showed that $-600V$ polarity caused a large amount of so-called “bar-graphing”, as shown in Fig. 2.13 (a), but $+600V$
showed no visible corrosion. Also Fig. 2.13 (b) shows the damage area percentage increases more rapidly with higher ambient temperature. The formation of this corrosion is due to the transport of positive charged sodium ions from a module front glass into the TCO layer in thin film panels.

![bar-graphing](image1.jpg) ![corrosion comparison](image2.png)

(a) bar-graphing (b) corrosion comparison

Fig. 2.13 Accelerated Test Results in NREL Report [40].

In summary, two conclusions can be drawn from the above discussion:

✧ The floating PV system is allowed and no grounding requirement is from the electrical standards & codes point of view.

✧ High negative voltage potential between PV module conductors and ground is not allowed for thin-film modules. If possible, grounding the negative conductors of thin-film modules can avoid any cell damage completely due to the negative voltage. Moreover, if
grounding of the negative conductor cannot be achieved, eliminating/reducing the \( \text{dv/dt} \) on the conductors may also benefit PV modules, including crystalline and thin-film modules.

For some other special PV modules, such as highly efficient back-side contact cells developed by Sun-Power in 2005, there may be special requirements. This kind of module needs the positive conductor grounded, in order to eliminate negative charges in the panel front surface [41].

2.4.3. Trends and Present Development

Since thin-film modules (or other newly developed PV modules) may become more important in the future PV module market, a PV inverter should have the capability to make one pole from the panel side to be grounded; or the \( \text{dv/dt} \) on the conductor poles of PV module can be controlled to be in an acceptable range. Considering these facts, the development of future PV inverter may follow two different trends:

✧ transformerless inverters: it is easier to realize high efficiency. Thus the objective for transformerless inverters is to reduce the PV module side voltage fluctuation (\( \text{dv/dt} \)) or, if possible, achieve PV side positive/negative pole grounding.

✧ For inverters with transformer: The advantage to this kind of inverter is that galvanic isolation is inherently realized and as a result, it is very easy for PV module side grounding. Therefore, the objective for PV inverters with transformer is to achieve a higher efficiency
which can be compared with that of transformerless inverters.

In recent years, several transformerless PV inverter topologies have been proposed to achieve panel side grounding. Fig. 2.14 below shows a grid connected half-bridge 3-level NPC inverter (HBDC) [28] [42], which is the same as the one in Fig. 2.13 (b). As stated previously, the middle-point of the capacitor can be grounded and thus the voltage fluctuation and parasitic capacitance can be reduced. In HBDC, one of the PV modules’ positive conductors is grounded and both the DC side and the AC side can be grounded. This connection is safe for crystalline modules but is not allowed for thin-film PV modules and thus the use of this topology is limited. Another drawback of this topology is the two PV strings are loaded alternatively with line frequency rather than continuously. Thus the decoupling capacitor size should be enlarged.

![HBDC Inverter Topology](image)

Fig. 2.14 HBDC Inverter Topology [28] [42]

Similarly, Fig. 2.15 shows a grid interactive photovoltaic inverter with generation control.
circuit (GCC) which can load each PV string independently [43] [44]. The advantage of GCC is that individual MPPT can be applied to each string. Actually, one of the PV strings can be removed and sinusoidal current can still be injected into the grid. In this case, this structure can be used with various types of PV panels and realize grounding for both DC side and AC side.

![Fig. 2.15 PV Inverter with GCC](image)

Two patented inverter structures which may reduce the DC side voltage fluctuation are identified as highly efficient and reliable inverter concept (HERIC) and H5-topology, as shown in Fig. 2.16 and Fig. 2.17 respectively [39] [45] [46]. The concept of these topologies is to disconnect to DC-side from AC-side during the freewheeling periods of the inverter such that a fluctuating potential of the PV-generator is avoided. S1-S4 in Fig. 2.16 is operated in HF while S5 & S6 are operated in LF. In Fig. 2.17, all of these switches are operated in HF. Circuit simulation has been done with SIMetrix to evaluate the voltage fluctuation at the PV
module side. Fig. 2.18 gives the simulation results.

Fig. 2.16 HERIC Topology [32]

Fig. 2.17 H5-Topology [32]
It can be seen from the simulation results that HERIC topology has line frequency voltage fluctuation only:
\[ V_+ = \frac{V_{PV} + \sqrt{2} \cdot V_m \cdot \sin(wt)}{2} \]  

\[ V_- = \frac{-V_{PV} - \sqrt{2} \cdot V_m \cdot \sin(wt)}{2} \]

In the case of H5 topology, it has the same component of line frequency voltage with a small amount of high frequency ripple. Therefore, both of these two topologies may reduce the leakage current. However, since the negative conductor has a negative voltage potential relative to the ground, these topologies cannot be used with thin-film panels. The commercialized product from Sunways has 2-5kW inverters with euro-efficiency around 95%. Product SB8000TL (8kW power rating) from SMA using H5 topology has a CEC weighted efficiency of approximately 98%.

Another topology named “Karschny-topology” (Fig. 2.19) can achieve both DC side and AC side grounding [39] [47] [48] [49]. Switches S1 and S2 are operated with HF, S3 and S4 are switched with the grid frequency. The inverter can operate in buck or boost mode depending on the input side voltage. The drawback of this topology is that the energy storage inductor may reduce efficiency. Also, the decoupling capacitor placed at the PV module side must be larger to meet the ripple voltage requirement for the lowest input voltage case. In [49], the equation to calculate capacitor size does not take into account the low frequency component. The highest efficiency for a 1kW prototype with 25 kHz switching frequency is
up to 97% [49].

Another promising transformerless converter is proposed recently [50] and depicted in Fig. 2.20. The switch Q1&D1, D3 and L1 forms a typical buck-boost converter rotated by 90 degree counterclockwise. The sum of the voltage applied to C4 and C5 is the DC bus voltage, which supports a normal single phase or three phase inverter in a cascaded connection. This topology can support both the DC side and AC side grounding.
Based on the analysis above, the converters in Fig. 2.14 and Fig. 2.15 can be used with the panels which require one of the conductors grounded. Moreover, converters in Fig. 2.19 and Fig. 2.20 may only support negative conductor grounding.

Compared with the transformerless inverters summarized above, the inverters with transformers are more popular and widely adopted by the industry, particularly for low power AC module application and high power rating inverters for large scale PV plants. For the AC module application, high frequency transformer is usually used to achieve a high efficiency, light weight, smaller size and higher power density design. For high power PV inverters, adding a line frequency transformer between the inverter and the grid is the conventional architecture and there are at least two advantages for this configuration compared with the transformerless structure. One major benefit is the elimination of the DC current injected into the grid which may saturate the distribution transformer. Another benefit is that this configuration allows for a more flexible inverter design to optimize inverter efficiency by
utilizing the step up/down feature of the transformer. Besides the line frequency transformer, high frequency transformers are also widely used in high power PV inverters.

In the case of string/multi string inverters for residential application (power rating below 10kW), most are connected to one phase and the neutral is at the grid side. In the U.S., they are typically connected with two phases of a split-phase distribution transformer with a typical RMS voltage equal to 240V, as shown in Fig. 2.22. In this case, several modifications should be added to the transformers-less inverters shown in Fig. 2.19 ~ Fig. 2.20. Otherwise they will not work properly if the PV side negative conductor is grounded.

![Fig. 2.22 Two Possible Connections between Inverter and Grid](image)

In general, present PV inverter topologies with a transformer may be divided into two groups according to different PV applications: inverters for string/multi-string application and inverters for AC modules. The inverter’s power rating in the former case is usually higher than 2kW and in the latter case is lower than 300W [12].

56
Due to the differences in power ratings of these two applications, the inverter structure differs. The most commonly used topology with a transformer for string/multi-string applications is a half bridge or a full bridge type isolated DC/DC converter cascaded with a single/three phase full bridge inverter. For the DC/DC converter stage, typical high efficiency half/full bridge topologies, such as an asymmetrical half bridge topology and a phase-shifted full bridge topology, etc, are good candidates for this application [51]. Fig. 2.23 shows two typical topologies used for multi-string inverters. The boost DC/DC converter (Fig. 2.23 (a)) is a common solution for the distributed non-isolated MPPT stage in a multi-string inverter, i.e., SB 5000TL from SMA. The topology shown in Fig. 2.23 (b) has been used in commercial products, PowerLynx Powerlink PV 4.5kW [12]. Each DC/DC converter can provide 1.5kW power output and it is based on a current source full bridge converter with embedded HF transformer, which is also known as “isolated boost” and may step up the input voltage to an appropriate value. Efficiency for this converter is 94.5%, which is close to the efficiency of the SB 5000TL transformerless inverter from SMA with a power rating of 4.6kW [12].
(a) Topology for Multi-String Inverter in [12]: Sunny Boy 5000TL

(b) Topology of the Three-String Inverter with a Transformer [12]

Fig. 2.23 Common Structure for Multi-string Inverters Without/With a Transformer
Most of the inverters for AC module application are based on a typical Flyback converter or its enhanced versions. Fig. 17 depicts several topologies proposed for AC module [12]. The reasons for using this type of topology are as follow:

✧ Flyback converter inherently can boost the input voltage and meet the voltage requirement for grid connecting since the module side voltage is only 25V~ 55V.

✧ Considering the topology limitations [62], the power rating of Flyback converter is usually in the range of several hundred watts, which is a good match of that of AC module.

✧ Only one transistor is required on the primary side and no inductor is required at the Flyback output. Thus, it results in a lower cost design.

✧ Like the Flyback application in power factor correction (PFC), it may regulate the output current in a way that the envelop line of output current becomes a rectified sine wave. After unfolding circuitry and filters, a sinusoidal current is reproduced which may be fed into the grid.

The disadvantages of this type of inverter are as follow:

✧ The voltage stress of the switch in primary side is equal to the sum of the input voltage and the output voltage divided by transformer’s turn ratio, which is usually 2-3 times of input voltage.

✧ The energy stored in the leakage inductance of the transformer needs a circulation path; otherwise a large voltage spike will be imposed onto the switch when it is turned-off.
Thus, several voltage clamp circuits or enhanced version Flyback converters are proposed to clamp the voltage. The active clamp transformer reset technique offers many well-documented advantages over traditional single-ended reset techniques, including lower voltage stress on the main MOSFET, the ability to switch at zero voltage, reduced EMI and duty cycle operation above 50%. The active clamp circuit may be applied to either the low side of the transformer (Fig. 2.24) or the high side of the transformer (Fig. 2.25). The differences between the two types of circuit are analyzed in [52] and Table 2.12 gives a summary of the comparison results.

Fig. 2.24 Low-Side Active Clamped Flyback Converter [52]
Some other Flyback type topologies are illustrated in Fig. 2.26. For the converters in Fig. 2.26 (a) ~ Fig. 2.26 (d), Fig. 2.26 (g), the output current from the Flyback converter or isolated boost converter is modulated to a half-wave sine wave and then it is unfolded into a
full sine wave. The first three utilize an additional secondary winding of the transformer together with several more switches to rebuild the sinusoidal current. For the last two in Fig. 2.26 (d) and Fig. 2.26 (g), the AC module utilizes a thyristor or MOSFET bridge to unfold the current. The added switches or the thyristors are switched at the line frequency and as a result, there is no apparent additional switching loss. Another topology proposed for AC module is the one shown in Fig. 2.26 (f): a series-resonant dc-dc converter with bang-bang dc-ac inverter [1]. The advantages of this topology are soft-switching for $S_{PV1}$ and $S_{PV2}$ and the compact design of the transformer due to its ability to operate at a much higher switching frequency.

![Fig. 2.26(a) 100W Flyback-Type HF-Link Inverter [53]](image-url)
Fig. 2.26(b) Modified Shimizu Inverter [54]

Fig. 2.26(c) Dual Transistors Flyback-Type Inverter [55]

Fig. 2.26(d) Flyback dc/dc with an Unfolding dc/ac Inverter [56]
A comprehensive comparison of these AC modules has been done in [12] and Table 2.13 summarizes the result. Table 2.13 shows the resonant converter has the smallest transformer
<table>
<thead>
<tr>
<th>Fig. No.</th>
<th>Decoupling capacitor</th>
<th>lifetime</th>
<th>Grid interface</th>
<th>European Efficiency</th>
<th>Cost [Euro]</th>
<th>Component ratings (besides EMI filter)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>T [cm³] S+D [KVA]</td>
</tr>
<tr>
<td>Fig. 2.23(a)</td>
<td>2.2mF@45V</td>
<td>Medium</td>
<td>2 transistor CSI</td>
<td>91.4%</td>
<td>19.6</td>
<td>0.0115 12.3</td>
</tr>
<tr>
<td>Fig. 2.23(b)</td>
<td>68uF@160V</td>
<td>Short</td>
<td>2 transistor CSI</td>
<td>69.7%</td>
<td>27.6</td>
<td>0.0173 36.5</td>
</tr>
<tr>
<td>Fig. 2.23(c)</td>
<td>2.2mF@45V</td>
<td>Medium</td>
<td>2 transistor CSI</td>
<td>92%</td>
<td>22.6</td>
<td>0.0115 13.7</td>
</tr>
<tr>
<td>Fig. 2.23(d)</td>
<td>2.2mF@45V</td>
<td>Medium</td>
<td>4 transistor CSI</td>
<td>92.4%</td>
<td>20.7</td>
<td>0.0115 16</td>
</tr>
<tr>
<td>Fig. 2.23(e)</td>
<td>33uF@400V</td>
<td>Long</td>
<td>4 transistor VSI</td>
<td>90.3%</td>
<td>19.4</td>
<td>0.0081 14</td>
</tr>
<tr>
<td>Fig. 2.23(f)</td>
<td>33uF@400V</td>
<td>Long</td>
<td>4 transistor VSI</td>
<td>90.5%</td>
<td>25.3</td>
<td>0.0041 13.3</td>
</tr>
<tr>
<td>Fig. 2.23(g)</td>
<td>2.2mF@45V</td>
<td>Medium</td>
<td>4 transistor CSI</td>
<td>95.4%</td>
<td>21.1</td>
<td>0.0115 18.5</td>
</tr>
</tbody>
</table>

(Notes: T → Transformer, S+D → Semiconductors)
since the magnetic component size is minimized. The Flyback based converter attains a good balance between the efficiency and cost, and the topology in Fig. 2.26 (d) has a very practical value. The converter in Fig. 2.26 (b) has lowest efficiency and largest device rating. Also, the typical efficiency of these AC modules is around 90%-95.4% (except converter in Fig. 2.26 (b)).

2.5 Summary

This chapter discussed the roadmap for development of grid-tied solar inverters. The evolution of the solar inverter technologies has two aspects: system structures and inverter topologies. Therefore, the content of this chapter may be divided into two parts.

In the first part of this chapter (Section 2.1 ~ 2.3), The PV inverter technologies have been categorized and compared thoroughly, mainly in terms of the inverter system structures. Although the inverter topology has direct impact on the inverter performance and they have gained increasing attention in recent years, the system structure is the most important factor affecting the energy yield of the PV system. It is clear that the most important progress in PV inverter technologies in recent years is related to the innovation and investigation of system structures. The conversion efficiency data of corresponding PV inverter products with different system structures have been documented and compared for an overall evaluation of
the advantages as well as disadvantages of different structures. The energy yield for different PV inverter structures is compared and energy gain is listed in the second section. The comparison showed that a year round energy yield gain in the range of 4% ~ 12% may be obtained for the system using distributed MPPT technologies over centralized inverter systems.

In the second part of this chapter (Section 2.4), various PV inverter topologies are reviewed and evaluated in terms of their efficiency, component count & size and other factors. These inverters are categorized according to different aspects, such as the number of power processing stages and whether a transformer is used. Several important standards related to PV applications are discussed and summarized. Also after the discussion of the requirements from the standards and the panel characteristics, a conclusion is drawn about whether PV panel side grounding is required.

The objective of this part of the project is to understand the requirements, challenges and new trends for solar energy conversion in the future. Generally, future research related to high efficiency PV energy conversion will focus on the following aspects:

✧ The investigation and development of new PV system structures.

✧ Development of advanced high efficiency inverter topologies which may fit into the new system structures to boost the energy yield.
3.1 Research Motivation

The discussion in Chapter 2 pointed out that although PV module side grounding is not required by the corresponding standards both in Europe and the U.S., a versatile PV inverter should have the capability of PV module side grounding or at least, have the capability to control the dv/dt on the PV module conductors to avoid excessive leakage current.

Generally, for string level distributed MPPT (D-MPPT) structures, the transformer-less inverter achieves higher efficiency more easily, but it is difficult to achieve PV module grounding with them; whereas inverters with transformers achieve PV side grounding more easily but they may suffer from lower efficiency. Thus, the future trends for PV inverters lie in two directions: for inverters with a transformer, research may focus on the improvement of its efficiency; for transformer-less inverters, the major challenge is to achieve panel side grounding while maintaining high efficiency.
As shown in Fig. 3.1, for commercial and utility scale PV applications, string level distributed MPPT technology (also referred as multi-string inverter), may increase the year-round energy yield by utilizing individual MPPT controller for each PV string. The string level MPPT ensures that the negative effects of module shading, soiling, aging and mismatch are minimized and contained within the string.

For this structure, the key component is the DC/DC converter connected to a PV string to accomplish MPPT control. The DC/DC converter for each string will usually boost the voltage to a higher level allowing the inverter to operate more efficiently when the string voltage is not sufficiently high. The common topology used for this DC/DC converter is a Boost converter which may support a wide input voltage range and the efficiency may be high as a result of using modern power semiconductor devices, i.e., high voltage SiC.

Fig. 3.1 String Level Distributed MPPT Technology Depicted in Fig. 2.1 (c)
Schottky Diodes. However, this solution may require an additional line frequency transformer at the output of the inverter stage if it is the objective of the PV system to achieve the PV module side grounding [63]. Apparently, the line frequency transformer will arrive at a solution which is both more expensive and heavier.

In fact, there are bundles of isolated DC/DC converters may be used for this application [64] [65]. One promising topology is the LLC resonant DC/DC converter. Its soft switching characteristics, wide operation range, high efficiency conversion and simple structure have already achieved wide use as front end DC/DC stage in distributed power supplies [66] [67]. These features also make it a good candidate for the DC/DC stage in the distributed MPPT application. Fig.3.2 displays the circuit diagram of a half bridge LLC resonant DC/DC converter. Fig.3.3 shows its typical DC gain curves under different load conditions.

![Fig.3.2 Circuit Diagram of a Half Bridge LLC Resonant DC/DC Converter](image)
During each switching cycle, the resonant component $L_m$ joins the resonance between $L_r$ and $C_r$ only for a part time. Thus, the LLC resonant converter has two resonant frequencies shown as below [67]:

$$f_s = \frac{1}{2\pi \sqrt{L_r \cdot C_r}}$$  \hspace{1cm} (3.1)

$$f_m = \frac{1}{2\pi \sqrt{(L_m + L_r) \cdot C_r}}$$  \hspace{1cm} (3.2)

The existence of two resonant frequencies leads to unique DC gain features of LLC resonant
converter. The operation region 1 and region 2 marked in Fig. 3.3 constitute the ZVS region where the ZVS turn-on of the switches may be achieved; whereas region 3 is called the ZCS region where ZCS of the switches is obtained. For most applications with MOSFET switches, making the converter operate in the ZVS region is preferred. For a certain load condition, the converter’s DC gain decreases with the increase of the switching frequency in the ZVS region. However, at frequency $f_s$, the converter has unity gain independent of the load condition. Fig.3.4 shows the key waveforms to illustrate the converter operation at different switching frequencies in the ZVS region.

Fig.3.4 (a) Case I: $f_m < f_{sw} < f_s$
Fig. 3.4 (b) Case II: $f_{sw} = f_s$

Fig. 3.4 (c) Case III: $f_{sw} > f_s$

Fig. 3.4 Key Waveforms of LLC Resonant Converter for Three Operation Cases
Fig. 3.4 shows that a considerable amount of magnetizing current $I_{Lm}$ freewheels on the primary side of the transformer without being involved in the power transfer. This part of reactive power will generate conduction losses and transformer loss which may dramatically reduce the converter’s efficiency, particularly for light load conditions. Circulating energy is minimized when operating the converter at a frequency approximating $f_s$.

### 3.2 Operation Principle of “Hybrid Bridge” Resonant Converter

The major challenge of the DC/DC converter for DMPPT application comes from the wide input voltage range. For the front end power supply application, the optimal design methodology proposed in [66] may lead to a high efficiency LLC converter with a wide operation range. However, for PV inverter application, the required operation range is even wider. For example, the commercialized 2kW PV inverter is usually designed to operate with an input voltage in the range of 150V-450V DC. This wide range of operation is a challenge for converter design and it’s difficult to maintain high efficiency in such a wide range. For resonant converters, the tradeoff between efficiency optimization and input range is always there. Equation (3.3) defines the DC gain for a typical LLC resonant converter [67]:
\[
\begin{aligned}
M(h, Q_r, \Omega) &= \frac{V_o}{V_{in}/(2N)} = \frac{1}{\sqrt{\left(1 + \frac{1}{h} - \frac{1}{\Omega^2 h}\right)^2 + Q_r^2 \left(\frac{1}{\Omega} - \Omega\right)^2}} \\
N &= \frac{N_p}{N_S}; Q_r = \frac{\pi^2}{8 N^2 R} \sqrt{L_r / C_r}; \quad \Omega = \frac{f_s}{f_0} \quad ; \quad f_0 = \frac{1}{2 \pi \sqrt{L_r C_r}} \quad ; \quad h = \frac{L_m}{L_r}
\end{aligned}
\]

\[(3.3)\]

Where \( N \) is the turn ratio of primary winding and secondary winding; \( L_m \) is the magnetizing inductance of the transformer; \( L_r \) and \( C_r \) are resonant inductance and capacitance; \( R \) is the load resistance; \( f_0 \) is the characteristic frequency of the resonant tank; \( f_s \) is the switching frequency. Basically, low \( Q_r \) and higher \( h \) lead to a wider regulation range but higher circulating current because of a smaller \( L_r \). As a result, higher resonant current appears and larger amount of reactive power is circulating in the circuit. The converter’s efficiency will be affected and a trade-off will be made between amplitude of resonant current and efficiency.

Fig. 3.5 shows a series of typical DC gain curves of a LLC converter with different load resistance from 125Ω (curve \( M_{real1} \)) to 2500Ω (curve \( M_{real5} \)). In fact, the DC gain may not be high enough for the low input voltage case even if a great deal of efficiency is sacrificed in the design. In order to resolve the conflict between converter operation range and efficiency optimization, a “hybrid bridge” two modes LLC converter is proposed, as shown in Fig. 3.6. When \( V_{in} > V_{th} \) (\( V_{th} \) is pre-set threshold voltage), \( S_3 \) stays off and \( S_4 \) stays conducting. In this case, the converter behaves as a half bridge (HB) LLC converter; when \( V_{in} < V_{th} \), both \( S_3 \) and
S₄ are commanded to turn on and off alternatively. V₉₃ is identical to V₉₁ and V₉₄ is identical to V₉₂. In the ideal case, all these signals are frequency varied square waveform with a 50% duty cycle. The converter behaves as a full bridge (FB) LLC converter and, naturally, the DC gain doubles compared with the HB LLC resonant converter.

Fig. 3.5 DC Gain Characteristics of an LLC Converter for PV Application

For the proposed resonant converter, the mechanism to achieve ZVS in the two operation modes is not changed: it utilizes the resonance of the same passive components. Therefore, “hybrid bridge” structure is exclusively suitable for a resonant converter. Theoretically the converter may achieve best efficiency at two operation points: \( V_{in} = V_{nom} \) in HB mode and \( V_{in} = 1/2 \) \( V_{nom} \) in FB mode. The converter can be designed to cope with a much narrower
Fig. 3.6 Proposed Hybrid Bridge Converter and Its Dual Mode Operation
operation range and it changes to FB mode for a low input voltage case. Therefore, the converter design may be optimized and maintain a high efficiency in an extended operation range. The curves in Fig. 3.5 are from a design with $V_{\text{nom}}=360\text{V}$ and $V_{\text{inmax}}=450\text{V}$. Thus, converter may have high efficiency in full bridge mode when $V_{\text{in}}$ drops to 180V and it also can accept a $V_{\text{in}}$ as low as 150V.

Fig. 3.7 shows the switching frequency of this converter with different input voltage under several load conditions. From Fig. 3.7, the operation frequency for $V_{\text{in}}=200\text{V}$ and $V_{\text{in}}=400\text{V}$ are close under various kinds of load conditions. This implies that much lower reactive power will exist when the converter operates with low input voltage. The conduction loss will be reduced and, as a result, the converter efficiency is improved.

![fs Variation Vs. Different Vin](image)

**Fig. 3.7** $f_s$ for Different $V_{\text{in}}$ under Various Load Conditions of Proposed Converter
Due to the change of circumstances, the PV panel’s $V_{MPP}$ may vary due to differences in temperature and sun irradiation. The converter may need to change operation mode adaptively to accommodate different $V_{MPP}$.

Fig. 3.8 Examples of an Unsafe Mode Transition Versus a Safe Mode Transition
For most applications, it’s rare for the occurrence of a mode change because the change of $V_{MPP}$ year round is limited. However, for the system with a $V_{MPP}$ close to the $V_{th}$, frequent mode change may be observed. It is feasible to disable all the gate signals before mode change and then enable the converter in the desired operation mode. However, it is better to change the mode “on the fly”, particularly in the event that mode changes happen frequently.

Fig. 3.8 (a) shows an example of mode transition. Once $V_{pv} < V_{th}$, signal CMD jumps from low to high at $t=t_1$. According to the switching patterns in Fig. 3.6 (b), gate signals $S_3$ should follow $S_2$ and $S_4$ should follow $S_1$ as well. Then signal $S_3$ starts to rise and $S_4$ begins to fall. This will introduce an overlapping period during which switch $S_4$ is not fully turned off but switch $S_3$ has already been turned on. A shoot-through may occur and both of the switches $S_3$ and $S_4$ may be damaged. Similarly, the shoot-through may happen during a mode change from FB to HB at $t=t_2$. Therefore, how to achieve a safe transition is worth considering. Fig. 3.8 (b) depicts a simple solution: the gate signals transition is only allowed when $V_{gs1}$ is high. As a result, the inherent dead-time between gate signal $S_1$ and $S_2$ may be used to avoid the shoot-through between $S_3$ and $S_4$.

A special gate logic generator is designed to achieve safe mode transition by generating proper gate drive signals. Fig. 3.9 shows the controller structure for proposed DC/DC converter. Fig.3.10 depicted the operation waveforms of the gate logic generator.
Fig. 3.9 Controller Structure for Proposed DC/DC Converter

Fig. 3.10 Key Waveforms of Controller for Proposed Converter
3.3 Analysis of Proposed Converter Operation with PV Modules

The typical characteristic curve of a group of PV modules is plotted in Fig. 3.11.

For a single cell in a PV module, the relationship between its output current and terminal voltage may be described by equation (3.4) [68]:

\[ i(v) = I_g - I_{sat}\left\{ \exp\left(\frac{q}{AKT}(v + iR_s)\right) - 1 \right\} \]  

(3.4)
Where, \( I_g \) – light-generated current (A)

\( I_{\text{sat}} \) – saturation current (A)

\( q \) – 1.6*10^{-19} \text{ Coulomb}

\( A \) – Ideality factor

\( K \) – Boltzmann constant

\( T \) – cell absolute temperature, Kelvin

\( i \) and \( v \) – panel current and voltage

Once a group of PV modules are connected with the D-MPPT stage, the I-V curve and P-V curve of this group of modules have defined the input voltage range and possible output power for a specific environmental condition. For the D-MPPT stage, it should have the capability to regulate the PV modules’ voltage to be their \( V_{\text{mpp}} \). More specifically, the basic requirement for the converter is that it should have a proper DC gain for a certain operation point. For example, the \( V_{\text{mpp}} \) shown in Fig. 3.11 is around 360V. If the DC bus voltage is 400V, the conversion gain for this D-MPPT stage should be 400/360=1.11. Since \( V_{\text{mpp}} \) is greater than \( V_{\text{th}} \), the proposed converter will operate in the half bridge mode. From Fig. 3.5, a proper operation frequency for the converter should exist at which the converter has a DC gain equal to 1.11. Considering the required DC gain (defined as M) will change when the input voltage or the delivered power varies, M may be defined as a function of \( V_{\text{pv}} \) and \( P_{\text{pv}} \)
and $P_{pv}$ is also a function of $V_{pv}$:

$$
P_{pv}(v) = i(v) \cdot v = v \cdot I_g - v \cdot I_{sat} \left\{ \exp \left[ \frac{q}{AKT} (v + iR_s) \right] - 1 \right\} \quad (3.5)
$$

The $I_g$ and $I_{sat}$ may be solved by the equation (3.4) by asserting the PV module parameters from its datasheet. Then equation (3.6) may be derived by a combination of (3.3) ~ (3.5) for proposed dual mode converter in HB mode:

$$
\begin{align*}
M(h, Q_n, \Omega, v) &= \frac{V_o}{V_m/(2N)} = \frac{1}{\sqrt{(1 + \frac{1}{h} - \frac{1}{\Omega h})^2 + Q_{new}^2 \left( \frac{1}{\Omega} - \Omega \right)^2}} \\
N &= \frac{N_f}{N_s} ; Q_{new} = [\pi^2 \cdot v \cdot i(v) \cdot \sqrt{L_s/C_s}]/[2 \cdot V_{R_s}^2] ; \\
\Omega &= \frac{f_s}{f_o} ; f_o = \frac{1}{2\pi \sqrt{L_s C_s}} ; h = \frac{L_m}{L_s}
\end{align*}
\quad (3.6)
$$

From (3.6), the DC gain $M$ is a function of $f_o$ and $V_{PV}$ once the circuit parameter is chosen. An example plot of $M$ curve in a 3-D plane is shown in Fig. 3.12. The characteristics of the group of PV modules follow the curves in Fig. 3.11. When the $V_{PV}$ is very low or very high, the DC gain is largest because the $P_{PV}$ is small in both cases. With the help of Fig. 3.12, the possible operation area of the converter in HB mode may be examined for a specified
operational circumstance, i.e., under certain sun irradiation and/or temperature. Similarly, the operation of the converter in FB mode may be analyzed and the only difference is that its DC gain doubles.

![M Curve in a 3D Plane](image)

Fig. 3.12 An Example Plot of M Curve in a 3D Plane

### 3.4 Design Considerations for “Hybrid Bridge” Resonant Converter

Before the power stage starts running, the controller of the proposed converter should check the open circuit voltage \( V_{OC} \) of connected PV panel. It may share the voltage sensor which is implemented for MPPT. Thus, the voltage check will not add additional cost to the
system. The MPPT controller will generate a reference signal corresponding to 75% $V_{OC}$ as
the initialized operation point for PV panel. In this case, the DC/DC controller may use this
signal to determine in which mode the converter should be operated at the beginning. This
procedure may prevent unnecessary mode transitions during start-up. Additionally, mode
transition after start-up will not occur frequently since the PV inverter restarts every morning
and $V_{OC}$ will be checked at that time.

At the moment when the mode change takes place, the DC/DC controller may observe a
sudden change of the DC gain and will respond to this transition accordingly. Depending
on the control loop’s response and the converter’s dynamic behavior, the PV panel output
power and voltage will experience overshoot (undershoot) during mode transition. Moreover,
the MPPT controller’s operation may, in some cases, be affected by the mode transition. If
the transition time period is long enough and the converter fails to re-enter steady-state
operation when the MPPT controller starts to sense the $V_{PV}$ and $I_{PV}$ with its analog to
digital (A/D) converter, the MPPT controller will make a wrong decision and the converter may
deviate from the true maximum power point for a certain time. In order to avoid malfunction
of MPPT controller during the mode transition period, it’s reasonable to suspend the MPPT
controller until the transition period ends. In other words, the reference signal or operation
frequency to set the PV panel operation point will remain unchanged. In practice, the DC/DC
controller needs to notify the MPPT controller before mode transition begins. And after a
certain delay period, the MPPT will resume updating the reference signal. Since the MPPT is
disabled during mode change, the PV panel cannot be guaranteed to operate at \( V_{\text{MPP}} \).
However, because the transition can be finished in dozens of milliseconds and it will not
occur frequently, the power loss from operation without MPPT is quite small and it may be
ignored. Considering the required cooperation between DC/DC controller and MPPT
controller, a digital controller is preferred.

When designing the proposed DC/DC converter, it is important to choose a proper
threshold voltage \( V_{\text{th}} \). The basic rule for selecting \( V_{\text{th}} \) is that the converter’s efficiency may be
optimized throughout the whole input voltage range. Ideally, \( V_{\text{th}} \) should be the voltage at
which the converter may have identical efficiency no matter in which mode it operates. For
practical design, the half of the highest \( V_{OC} \) (happens in cold weather) of PV panel can be
chosen as \( V_{\text{th}} \) for initial evaluation. Then design the resonant converter parameters with input
range of \( 1/2 \, V_{OC} \sim V_{OC} \) and optimize efficiency at point \( V_{\text{nom}} \), where \( V_{\text{nom}} \) is equal to \( V_{\text{MPP}} \)
specified in panel’s datasheet. The power loss should be analyzed for converter operating in
both FB mode and HB mode with \( V_{\text{in}} = V_{\text{th}} \). In this condition, suppose \( \eta_1 \) represents efficiency
in HB mode and \( \eta_2 \) is efficiency in FB mode. If \( \eta_1 > \eta_2 \), \( V_{\text{th}} \) should decrease; otherwise, \( V_{\text{th}} \)
increases. An optimal point can be obtained for \( V_{\text{th}} \) after several iterations.
3.5 Simulation and Experiment Verification

Following the design procedure as introduced in the last section, a converter is designed. Fig.3.13 ~ Fig.3.16 give the key operation waveforms of the designed converter operating in either full bridge mode or half bridge mode with different input voltage.

| Table 3.1 Circuit Parameters of Proposed Converter in Simulation and Experiment |
|-------------------------------------------------|-----------------|-----------------|
| **Input voltage**                               | 125V~ 450V      | **L<sub>r</sub>** | 39uH |
| **DC bus voltage**                              | 500V            | **C<sub>r</sub>** | 180nF |
| **f<sub>s</sub> range**                         | 40kHz ~ 120kHz  | **L<sub>m</sub>** | 117uH |
| **All switches**                                | IPW47N65C3      | **C<sub>in</sub>** | 220uF |
| **Transformer**                                | E653227-3C92    | **DC bus capacitor** | 1mF |
|                                                 | Np: 10; Ns: 28  |                  |      |


Fig. 3.13 Simulation Results: $V_{in}=180\text{V}, V_o=500\text{V}, P_o=2\text{kW}$, FB Mode

Fig. 3.14 Simulation Results: $V_{in}=250\text{V}, V_o=500\text{V}, P_o=2\text{kW}$, FB Mode
Fig. 3.15 Simulation Results: $V_{in}=360\text{V}$, $V_o=500\text{V}$, $P_o=2\text{kW}$, HB Mode

Fig. 3.16 Simulation Results: $V_{in}=450\text{V}$, $V_o=500\text{V}$, $P_o=2\text{kW}$, HB Mode
To examine the performance of the designed converter, a prototype has been built in the lab. Fig. 3.17 gives a picture of 2kW DSP controlled single phase solar inverter prototype which utilized the proposed dual mode LLC resonant converter as the MPPT stage.

![Fig. 3.17 Picture of 2kW Solar Inverter Prototype](image)

Figs. 3.18 and 3.19 give the experimental waveforms for proposed converter operating in HB mode and FB mode. From Fig.3.18, ZVS is achieved for MOSFET switches. Fig. 3.19 gives the voltage waveform $V_{cr}$ of resonant capacitor, resonant current waveform $I_{Lr}$ and switching node voltage $V_{SW}$. Fig. 3.20 shows the CMD signal and gate signals during mode transition to verify the operation of gate logic generator.
Fig. 3.18 FB Mode Operation of Proposed Converter: $V_{in}=180\text{V}$, $V_o=500\text{V}$, $P_o=1\text{kW}$

Fig. 3.19 HB Mode Operation of Proposed Converter: $V_{in}=360\text{V}$, $V_o=500\text{V}$, $P_o=1\text{kW}$
Fig. 3.20 Gate Signals for Proposed Converter during Mode Transition
Fig. 3.21 Mode Transition Test Result of Proposed Converter with PV Panel
Fig. 3.21 shows the mode transition waveforms of the MPPT stage when it operates with 200W solar panels. The overshoot and undershoot of $I_{PV}$ and $V_{PV}$ are due to the dynamic behavior of the MPPT stage. The mode transition shown in Fig. 3.21 is intentionally made for the test. It’s not based on comparison between of $V_{PV}$ and $V_{th}$.

Fig. 3.22 gives the tested efficiency curves of the converter with different input voltage under several load conditions. It shows that the converter has highest efficiency with $V_{in}=360V$ and $V_{in}=180V$. The highest efficiency from the measurement is around 98.8%. Fig. 3.23 shows the weighted CEC efficiency for different input and for $V_{in}=180V$, it has the highest CEC efficiency which is around 98%.

![DC/DC Stage Efficiency Measurement](image)

Fig. 3.22 Measured Efficiency of DC/DC Stage
Fig. 3.23 Calculated CEC Weighted Efficiency based on Measured Data

Fig. 3.24 MPPT Tracking Results with PV Panels
Fig. 3.24 shows the PV panel voltage is regulated based on the command from an MPPT controller. The panel output power $P_{pv}$ is maintained at the maximum point in steady state.

### 3.6 Summary

A “hybrid bridge” resonant converter is proposed as the MPPT stage for string level D-MPPT application. The proposed “hybrid bridge” converter employs a mode change controller to command the converter operating in either full bridge (FB) mode or half bridge (HB) mode depending on the PV string input voltage. The mechanism to achieve zero voltage switching (ZVS) in the two operation modes is the same. The proposed converter may be designed to cope with a much narrower operation range and it changes to FB mode when $V_{PV}$ drops below a threshold voltage $V_{th}$. Therefore, an efficiency-oriented design can be performed and the converter can maintain high efficiency in an extended operation range. Both the simulation and test results are provided to verify the feasibility of proposed converter. The results show that the experimental prototype’s weighted efficiency reached 98%.
Chapter 4. Variable Resonant Tank (VRT) High Efficiency DC/DC Converter for Module Level D-MPPT Application

4.1 Research Motivation

Fig. 4.1 Part of the FREEDM System Diagram [7]
As discussed in Chapter 1, the 400V DC bus in the FREEDM system provides an alternative interface for PV converters. Fig. 4.1 shows part of the FREEDM system including an Intelligent Energy Management (IEM) module. As a result, PV converters in FREEDM system need to have only a DC/DC stage to do MPPT and have a proper voltage conversion gain to interface with the DC bus.

The module level D-MPPT technology brings a specific kind of PV converter for this application: the PV module integrated DC/DC converters (DC MICs). At present, they are gaining an increasing amount of attention due to their distinctive features [3] [12] [48] [69] [70–76]:

(3) The DC MIC is an integrated part of the PV-panel. DC MICs remove losses due to the mismatch between panels and it supports panel level MPPT. For a string inverter or centralized inverter, a string or multi-string of PV modules share a single MPPT controller, but the mismatch loss is serious in partial shade conditions [68]. In practical application, the PV system based on module level MPPT technology may have higher year round energy yield than those systems with string level technology or centralized technology, although the latter system achieves higher conversion efficiency (efficiency of the power conversion circuit).

(4) Panel level hot-spot risk is removed [69] and panel lifetime may be improved. Hot-spot takes place when a shaded cell within a partially-shaded panel becomes reverse
biased and dissipates power in the form of heat [77]. For series connected PV panels used with a string or centralized inverter, a bypass diode is added to each PV module during manufacturing. For the DC MIC solution, the bypass diode is not necessary because there is no direct electrical connection between PV modules. Instead, each PV module has its own DC MIC which allows for more flexible PV project planning and multi-faceted PV panel installation.

In summary, the advantages of module level D-MPPT technology ensure higher energy yield in complex terrain environments and make it very suitable for roof-top PV applications.

4.2 Comparison of MICs in Series and Parallel Connections

In Fig. 2.1 (d) and Fig. 2.1 (e), two kinds of connection structures for DC MICs are shown. The Fig. 4.2 below redrew the connection structures. Fig. 4.2 (a) shows a type I DC MIC configuration, consisting of multiple parallel connected MICs directly interfaced with a DC bus. Type II DC MICs, shown in Fig. 4.2 (b), need to form a series connection to obtain a voltage high enough to interface with the DC bus. The two system structures have different features. Table 4.1 summarizes the comparison results of the two MIC structures from several aspects.
The power rating of both types of DC MICs is approximately 200W~300W. Considering that the MPP voltage ($V_{mpp}$) varies with different types of PV module and it may also vary with environmental change, both types of DC MICs need to operate in a wide input range at high efficiency. Moreover, since the generated power of PV modules is changes continuously throughout the day, it is important to obtain high efficiency for both types of DC MICs in different output power conditions. The efficiency of the converter operating at low to medium power conditions is important for efficiency evaluation [12] but is usually difficult to optimize. Generally, the parallel connection is more flexible due to its stronger anti-partial cloudy capability, and the fact that any single failure of a MIC will not impact any other part of the system. As a result, MICs in a parallel configuration have higher fault tolerance and result in higher system reliability.
<table>
<thead>
<tr>
<th>Items for Comparison</th>
<th>Parallel Connection</th>
<th>Series Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Panel Level MPPT</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>High Conversion Gain requirement</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Isolated Topology</td>
<td>Required to satisfy conversion gain requirement</td>
<td>unnecessary</td>
</tr>
<tr>
<td>Power Device voltage rating</td>
<td>High voltage devices (MOSFETs or diodes) are required</td>
<td>Only low voltage devices are used</td>
</tr>
<tr>
<td>Capacitors</td>
<td>High voltage capacitors are required; but less output capacitance is required for same power rating.</td>
<td>All low voltage capacitors; but more output capacitance are required due to their series connection.</td>
</tr>
<tr>
<td>Flexibility</td>
<td>More flexible; no limitation on system power level. Different types of panels can be mixed in the system.</td>
<td>Less flexible; there is minimum quantity limitation of panels in a string due to limited conversion gain.</td>
</tr>
<tr>
<td>Anti-partial cloudy capability</td>
<td>Very good. The rest part of the system will not be affected</td>
<td>Has potential issue when partial cloudy happens to large part of panels in a string. Energy from un-shaded panels in this string cannot be harvested if string voltage is too low.</td>
</tr>
<tr>
<td>Impact of a single MIC failure</td>
<td>No impact on the rest part of the system</td>
<td>Potential problem exists since the failed module still need provide current path for the string.</td>
</tr>
<tr>
<td>Commercialized product Efficiency and challenges for efficiency improvement</td>
<td>Efficiency data unavailable. Efficiency improvement is a challenge.</td>
<td>European weighted efficiency is around 98%. Easier for efficiency improvement</td>
</tr>
</tbody>
</table>
From this point of view, the MICs connected in parallel are more promising for module level D-MPPT applications. However, the high conversion gain requirement brings challenges for parallel connected MIC design which usually compromises its efficiency.

The topologies suitable for this application may be categorized in two groups: non-isolated topologies and isolated topologies. For non-isolated topologies, Boost, Buck-Boost, Zeta, Cuk, or their derivatives [78–85] are commonly used. Isolated topologies mainly include Flyback [53] [57] [58] [88–89] [90–91], current-fed push-pull [92] [93], and resonant converters [59] [94]. The typical maximum efficiency of these converters is between 80%–97% [12] [48] [75].

Among these topologies, the half bridge LLC resonant converter is a good candidate due to its soft switching feature for the MOSFET on the primary side and diodes on the secondary side. The converter’s structure is simple and it has the capability to achieve a compact design with high efficiency [66–67] [95]. However, it is difficult for an LLC resonant converter to maintain high efficiency for a wide input range under different load conditions.

The focus of the following part of this chapter is to improve the efficiency of parallel connected MICs. In the next section, a new resonant DC/DC converter topology is proposed. An additional half-wave-rectifier (HWR) is added to a conventional LLC resonant converter. This HWR may be enabled or disabled for different operation conditions. Thus, the converter
has two operation modes. By changing operation modes adaptively according to PV module voltage $V_{PV}$ and output power $P_{PV}$, the converter’s efficiency is improved. Since the value of $V_{PV}$ and $P_{PV}$ may be obtained from the MPPT controller, no additional sensors are required. The operation principle of proposed resonant converter is explained in detail. A method is developed for deriving the converter’s DC gain with the fundamental harmonic approximation (FHA) method. A sample design is presented to demonstrate the design procedure of proposed converter. To evaluate the performance of the proposed MIC topology, loss analysis and efficiency estimation are performed based on circuit simulation. The experimental results from a 240W prototype are presented. They show that the proposed resonant converter can increase efficiency under low $P_{PV}$ conditions by more than 10% compared to a conventional LLC resonant converter. The maximum efficiency of the design reached 96.5%, and a European weighted efficiency of 95.8% for $V_{PV} = 36V$ was achieved on the prototype.

**4.3 Proposed VRT Resonant Converter and Its Operation Principle**

Fig. 4.3 shows a circuit diagram of the proposed resonant converter. $S_1$ and $S_2$ are two power MOSFETs; $D_{S1}$, $C_{S1}$ and $D_{S2}$, $C_{S2}$ are the body diodes and parasitic capacitances of $S_1$ and $S_2$, respectively. $C_r$ is the resonant capacitor; $L_r$ and $L_m$ are the magnetizing inductance of
transformers $T_{x2}$ and $T_{x1}$, respectively. $L_{\text{lkg}}$ is the sum of leakage inductance of $T_{x1}$ and $T_{x2}$.

The $D_1$, $D_2$ and $C_{o1}$, $C_{o2}$ form a voltage doubler at the secondary side of $T_{x1}$. A HWR formed by $D_3$, $S_3$, $D_4$ and $C_{o3}$ is added to the secondary side of transformer $T_{x2}$. Diode $D_3$ blocks the conductive path of the body diode of $S_3$. Thus, $D_3$ and $S_3$ form a unidirectional switch to enable or disable the HWR. When the HWR is enabled, the HWR and voltage doubler will support the 400V DC bus with their summed outputs.

![Fig. 4.3 Circuit Diagram of Proposed Resonant Converter](image)

<table>
<thead>
<tr>
<th>PV Panel Operation Condition</th>
<th>Converter Operation Modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1: $V_{PV}&gt;V_{th}$; $P_{PV}&gt;50% \ P_{\text{rated}}$</td>
<td>Mode I; HWR disabled</td>
</tr>
<tr>
<td>#2: $V_{PV}&gt;V_{th}$; $P_{PV}&lt;50% \ P_{\text{rated}}$</td>
<td>Mode I; HWR disabled</td>
</tr>
<tr>
<td>#3: $V_{PV}&lt;V_{th}$; $P_{PV}&gt;50% \ P_{\text{rated}}$</td>
<td>Mode I; HWR disabled</td>
</tr>
<tr>
<td>#4: $V_{PV}\leq V_{th}$; $P_{PV}\leq 50% \ P_{\text{rated}}$</td>
<td>Mode II; HWR enabled</td>
</tr>
</tbody>
</table>
As shown in Table 4.2, the operation of the new resonant converter has two modes depending on the PV panel’s working condition. For the first three operation conditions, the HWR is disabled by turning off switch $S_3$. As a result, the converter behaves like a traditional LLC resonant converter with a voltage doubler.

Fig. 4.4 shows the equivalent circuit for this mode. An equivalent resonant inductor $L'_r$, comprised of $L_r$ and $L_{lkg}$, participates in the resonant circuit formed by $L_m$ and $C_r$. Diode $D_4$ and is conducting to provide a path for the load current. The detailed analysis of this operation mode may be found in [95].

![Fig. 4.4 The Equivalent Circuit for Proposed Converter Operation in Mode I](image)

Once $V_{PV}$ is smaller than $V_{th}$ and $P_{PV}$ is lower than 50% of the rated power ($P_{rated}$), the PV panel is working in condition #4 and the converter will operate in mode II. The $V_{th}$ is a
predefined threshold voltage which is usually equal to the nominal voltage \( V_{\text{nom}} \). For one switching period, the operation of the converter in this mode may be divided into nine stages. The equivalent circuit for each stage is shown in Fig. 4.5. Fig. 4.6 depicts the key waveforms for the stages shown in Fig. 4.5. For the description of circuit operation (and for the subsequent DC gain derivation in the next section), the following assumptions are made:

(1) All the components are ideal. The body diodes and parasitic capacitance of \( S_1 \) and \( S_2 \) have been taken into account. The output capacitors have equal values. \((C_{o1}=C_{o2}=C_{o3})\).

(2) Inductor \( L_{\text{kg}} \) includes the leakage inductance of \( T_{X1} \) and \( T_{X2} \); it also includes the parasitic inductance of the wire.

(3) The turn ratio \( N_{TX2} \) \((N_{\text{pri}}: N_{\text{sec}})\) of transformer \( T_{X2} \) is half of \( N_{TX1} \). Define \( N_{TX2}=1/2 \) \( N_{TX1}=N \).

The operation processes are described as follows:

**Stage 1 \((t_0-t_1)\):** When \( S_2 \) is turned off at \( t=t_0 \), stage 1 begins. Since \( I_{\text{pri}} \) is negative, capacitor \( C_{s2} \) \((C_{s1})\) will be charged \((\text{discharged})\) and switching node voltage \( V_{\text{sw}} \) will increase accordingly. Inductors \( L_m, L_r \) and \( L_{\text{kg}} \) are all in resonance with \( C_r \). \( V_{cr} \) continues to decrease and no current flows through the secondary side of either transformer. The output capacitors \( C_{o1}, C_{o2}, \) together with \( C_{o3} \) supply the load current and \( V_{Co1} \sim V_{Co3} \) all decrease in this period.
**Stage 2 (t_1~t_2):** At time t=t_1, V_{sw} reaches V_{pv}. D_{s1} is forward biased and starts to conduct a current I_{pri}. I_{pri} starts to decrease. Once I_{pri} becomes smaller than the magnetizing current I_{Lr} and I_{lm}, the resonance of [L_m, L_r, L_{kg}] and C_r is stopped. L_r and L_m will be out of resonance following this time period. The difference between I_{pri} and I_{lm} will flow into the secondary side of T_{x1}. Similarly, the secondary side of T_{x2} will conduct the current difference between I_{pri} and I_{Lr}. Thus, the voltage across the primary side of T_{x1} and T_{x2} is clamped by V_{out}. I_{Lr} and I_{Lm} start to decrease linearly.

**Stage 3 (t_2~t_4):** This stage begins when S_{1} is turned on at t=t_2. At this moment, the primary side current I_{pri} is negative and flows through the body diode of S_{1}. Thus, ZVS turn on of S_{1} can be achieved at t_2. The current I_{pri} continues to decrease and changes its direction at t=t_3. The leakage inductor L_{kg} still resonates with C_r, and I_{pri} keeps increasing. The magnetizing currents I_{Lr} and I_{Lm} continue increasing with the same slope as in mode 2. The rectifier diodes D_{1} and D_{3} conduct current and power is delivered to the load. This stage ends when I_{pri} is equal to I_{Lm}.

**Stage 4(t_4~t_5):** At t=t_4, I_{pri} and I_{Lm} are equal. The output current of transformer T_{x1} reaches zero. Transformer T_{x1}’s secondary voltage is lower than output voltage. The output is separated from transformer T_{x1}. Meanwhile, since I_{pri} is still larger than I_{Lr}, the output current
of \( T_{x2} \) is not zero and power is delivered to the load through \( T_{x2} \). During this stage, \( L_m \) participates in the resonance again and the resonance between \([L_{lk}, L_m]\) and \( C_r \) begins.

**Stage 5 (t5~t6):** Switch \( S_1 \) is turned off at \( t=t_5 \). The current \( I_{pri} \) is positive and switching node voltage will decrease due to charging (discharging) of \( C_{s1} \) \( (C_{s2}) \).

**Stage 6 (t6~t7):** At the time \( t=t_6 \), \( V_{sw} \) drops to zero which causes the conduction of body diode \( D_{s2} \). With the drop of \( V_{sw} \), the voltage applied to \( L_m \) \( (V_{Lm}) \) decreases to zero and continues to become more negative. Once \( V_{Lm} \) is higher than a certain level, diode \( D_2 \) on the secondary side of \( T_{x1} \) will be forward biased. Thus, voltage applied to \( L_m \) is clamped and \( I_{Lm} \) will drop linearly. \( L_m \) is out of resonance with \( C_r \). Instead, only \( L_{lk} \) resonates with \( C_r \) and \( I_{pri} \) decreases sharply. This stage ends when \( I_{Lr} \) is equal to \( I_{pri} \).

**Stage 7 (t7~t8):** At time \( t=t_7 \), \( I_{Lr} \) is equal to \( I_{pri} \); no more current will flow in the secondary side of \( T_{x2} \). The output is separated from \( T_{x2} \). \( D_3 \) is turned off with ZCS. The voltage applied to \( L_r \) is not clamped and \( L_r \) once again participates in the resonance with \( C_r \) and \( L_{lk} \). The current \( I_{pri} \) is positive and continues flowing through \( D_{s2} \), which creates the ZVS condition for \( S_2 \) if \( S_2 \) is turned on at this moment.
**Stage 8 (t₈~t₁₀):** At \( t = t₈ \), \( S₂ \) is turned on with ZVS. The current \( I_{pri} \) continues to decrease due to the resonance between \([L_r, L_{lkg}]\) and \( C_r \). The transformer \( T_{x1} \) delivers power to the output. This stage ends when current \( I_{pri} = I_{Lm} \).

**Stage 9 (t₉~t₁₁):** At \( t = t₉ \), \( I_{pri} = I_{Lm} \). No more current will flow in the secondary side of \( T_{x1} \). The voltage applied to \( L_m \) is no longer clamped and \( L_m \) participates in the resonance again with \( L_r, L_{lkg} \) and \( C_r \). At \( t = t₁₁ \), \( S₂ \) is turned off and a new switching cycle begins.

![Fig.4.5 (a) Stage 1: \( t₀~t₁ \)](image)

![Fig.4.5 (b) Stage 2: \( t₁~t₂ \)](image)
Fig. 4.5 (c) Stage 3: $t_2 \sim t_4$

Fig. 4.5 (d) Stage 4: $t_5 \sim t_6$
Fig. 4.5 (f) Stage 6: \( t_6 \sim t_7 \)

Fig. 4.5 (g) Stage 7: \( t_7 \sim t_8 \)

Fig. 4.5 (h) Stage 8: \( t_8 \sim t_{10} \)
Fig. 4.5 Equivalent Circuits for Each Stage (Mode II Operation)

Fig. 4.6 Key Waveforms of Proposed Converter (Mode II Operation)
From the above analysis, the energy transferred by transformer $T_{x1}$ and $T_{x2}$ is different. The positive part and negative part of current $I_{pri}$ is asymmetrical. However, the voltage-second balance of the transformer $T_{x1}$ and $T_{x2}$ is still preserved. Further, if a full-wave-rectifier (FWR) is added instead of the HWR, the $I_{pri}$ will become symmetrical and other characteristics of the converter will remain. The theoretical analysis of Mode II operation above has been verified by the simulation with SIMetrix®. Fig. 4.6 shows the simulation results of proposed converter under following operation conditions: $V_{pv}=22V$, $V_{out}=400V$, $P_{out}=120W$ (50% $P_{rated}$), $f_s=83$ kHz. The simulation waveforms match with the previous theoretical analysis well.

![Fig. 4.7 Simulation Results of Proposed Converter Operating in Mode II](image)

Fig. 4.7 Simulation Results of Proposed Converter Operating in Mode II
4.4 DC Gain Analysis for VRT Converter Operation in Mode II

Understanding of the DC gain characteristic for a resonant converter has importance equal to knowing its operation principle. Some discussion is developed in this section for DC gain estimation of the proposed converter. Since the DC gain characteristic for Mode I operation is the same as that for a LLC resonant converter, only Mode II operation requires a new analysis to develop its DC gain characteristic. The method widely used for DC gain analysis of resonant converters is called the fundamental harmonic analysis (FHA) method [62] [96–98] and it will be used for the analysis developed in this chapter. The FHA approach is based on the assumption that the power transfer from the source to the load through the resonant tank is almost completely dependent on the fundamental harmonic of the Fourier expansion of the currents and the voltage involved. The voltage at the input of the two rectifiers $V_{osq}(t)$ can be expressed as:

$$V_{osq}(t) = V_{ab}(t) + V_{cd}(t) \quad (4.1)$$

Where $V_{ab}(t)$ and $V_{cd}(t)$ are secondary side terminal voltage of transformer $T_{X2}$ and $T_{X1}$ (Fig. 4.3). Like the conventional LLC resonant converter, the current in the secondary side is quasi-sinusoidal and the voltage $V_{osq}(t)$ reverses when the current becomes zero. Therefore
$V_{osq}(t)$ is an alternative square wave in phase with the rectifier current. The Fourier expression of $V_{osq}(t)$ is:

$$V_{osq}(t) = \frac{4}{\pi} V_{out} \sum_{n=1,3,5,...} \frac{1}{n} \sin(n2\pi f_{sw} t) \quad (4.2)$$

For convenience, the phase angle of $V_{osq}(t)$ is assumed to be zero in (4.2). Its fundamental component $V_{o\_FHA}(t)$ is:

$$V_{o\_FHA}(t) = \frac{4}{\pi} V_{out} \sin(2\pi f_{sw} t) \quad (4.3)$$

The RMS amplitude of $V_{o\_FHA}(t)$ is:

$$V_{o\_FHA} = \frac{2\sqrt{2}}{\pi} V_{out} \quad (4.4)$$

Define the fundamental part of the rectifier current to be:

$$i_{rec}(t) = \sqrt{2} I_{rec} \sin(2\pi f_{sw} t) \quad (4.5)$$
The phase angle of \( i_{\text{rect}} \) is also zero since it is in phase with \( V_{o,FHA}(t) \).

Thus, the average value of \( i_{\text{out}} \) can be calculated:

\[
I_{\text{out}} = \frac{2}{T_{\text{SW}}} \int_{0}^{T_{\text{SW}}} i_{\text{rect}}(t) dt = \frac{2\sqrt{2} I_{\text{rect}}}{\pi} \tag{4.6}
\]

\( I_{\text{out}} \) can be expressed by (4.7):

\[
I_{\text{out}} = \frac{V_{\text{out}}}{R_{\text{out}}} \tag{4.7}
\]

Equation (4.8) can be derived by combining (4.6) and (4.7):

\[
I_{\text{rect}} = \frac{\sqrt{2}\pi V_{\text{out}}}{4R_{\text{out}}} \tag{4.8}
\]

Insert (4.8) into (4.5):

\[
i_{\text{rect}}(t) = \sqrt{2} \left( \frac{\sqrt{2}\pi V_{\text{out}}}{4R_{\text{out}}} \right) \sin(2\pi f_{\text{sw}}t) = \frac{\pi V_{\text{out}}}{2R_{\text{out}}} \sin(2\pi f_{\text{sw}}t) \tag{4.9}
\]
The equivalent AC output impedance $R_{o\_ac}$ can be derived by combining (4.4) and (4.8):

$$
R_{o\_ac} = \frac{V_{o\_FHA}}{I_{\text{rect}}} = \frac{8R_{\text{out}}}{\pi^2}
$$  \hspace{1cm} (4.10)

The expression for $R_{o\_ac}$ is the same as the one for conventional LLC resonant converter.

With the known $R_{o\_ac}$, the equivalent FHA resonant circuit model can be obtained, as shown in Fig. 4.8.

![Fig. 4.8 The Equivalent FHA Model for Proposed Converter Operation in Mode II](image)

In this model, $V_{1\_FHA}$ is the RMS value of fundamental component of the voltage at the switching node SW ($V_{SW}$). The voltage $V_{SW}$ is generated by the controlled switches $S_1$ and $S_2$. The output current $I_{out}$ is produced from $I_{\text{rect}}$ after the processes of the rectifier network and filter capacitors. From a turn ratio perspective, the conversion gain of a transformer with turn
ratio 2N followed by a voltage doubler is equal to the gain of a transformer with turn ratio N. Therefore, transformer $T_{x1}$ together with voltage doubler may be substituted by an equivalent transformer $T_{xe}$ with turn ratio N. The resulting expression for the DC gain of the converter can be derived through a circuit analysis based on the linear model in Fig. 4.8.

Define the DC gain:

$$M = \frac{N V_{o,FHA}}{V_{i,FHA}}$$  \hspace{1cm} (4.11)

Considering:

$$V_{SW}(t) = \frac{V_{dc}}{2} + \frac{2}{\pi} V_{dc} \sum_{n=1,3,5,...}^{\infty} \frac{1}{n} \sin(n2\pi f_{sw} t)$$  \hspace{1cm} (4.12)

$v_{i,FHA}(t)$ is the fundamental part of $V_{SW}(t)$:

$$v_{i,FHA}(t) = \frac{2}{\pi} V_{dc} \sin(2\pi f_{sw} t)$$  \hspace{1cm} (4.13)

$V_{i,FHA}$ can be derived:
\[ V_{i,FHA}(t) = \frac{\sqrt{2}}{\pi} V_{dc} \quad (4.14) \]

Combining with (4.4), (4.11) and (4.14), the input-to-output voltage conversion ratio is:

\[ \frac{V_{out}}{V_{dc}} = \frac{1}{2N} |M| \quad (4.15) \]

From FHA model, the \( Z_{out} \) is the impedance seen from the primary side of the two transformers:

\[ Z_{out} = \frac{N^2 R_{o,ac} \cdot L_{mr} \cdot S}{N^2 R_{o,ac} + L_{mr} \cdot S} \quad (4.16) \]

Where, \( L_{mr} = L_m + L_r \). The DC gain \( M \) can be derived:

\[ M(S) = \frac{Z_{out}}{\frac{1}{S \cdot C_r} + S \cdot L_{lkg} + Z_{out}} \quad (4.17) \]

By substituting \( S = j2\pi f_{sw} \), the amplitude of \( M(S) \) is:
For convenience, equation (4.18) can be re-written as (4.19) below:

\[
M(f_n) = \frac{1}{\sqrt{(1 + \lambda - \frac{\lambda}{f_n^2})^2 + Q^2 (f_n - \frac{1}{f_n})^2}}
\]  

(4.19)

The parameters in (4.19) are defined as follows:

\[
f_r = \frac{1}{2\pi \sqrt{L_{lkg} \cdot C_r}}
\]  

(4.20)

\[
Q = \frac{Z_0}{N^2 \cdot R_{o_{ac}}}
\]  

(4.21)

\[
\lambda = \frac{L_{lkg}}{L_m + L_r}
\]  

(4.22)

\[
Z_0 = \sqrt{\frac{L_{lkg}}{C_r}}
\]  

(4.23)
Equations (4.19) ~ (4.24) reveal the DC gain characteristics for Mode II operation. It is interesting that Mode II operation has similar DC gain expression as Mode I but with different parameters for the resonant tank. A series of example DC gain curves of Mode II operation under different load condition (with different Q values) are plotted in Fig. 4.9. For very light load conditions (small Q), the gain has a large peak. On the contrary, the gain becomes flat under heavy load conditions (large Q). Similar to a LLC converter, the DC characteristic of Mode II operation may be divided into ZVS and ZCS regions, and the converter should be prevented from entering the ZCS region. With proper choice of the resonant tank, Mode II operation can stay in the ZVS region when \( V_{pv} \) and \( P_{pv} \) vary. The ZVS region can be further divided into region I and region II due to slightly operation differences. In practical designs, the converter has unity gain at \( V_{pv} = V_{nom} \) and the converter enters mode II operation only when \( V_{pv} \leq V_{nom} \). Therefore, it is impossible for the proposed resonant converter to work in region I after entering Mode II operation. Mode II operation can only be active in region II. Furthermore, the discussion about Mode II operation in the last section is dedicated for region II. On the contrary, Mode I operation can only be active in region I (Fig. 4.10) because the required DC gain should be lower than 1 in Mode I (\( V_{pv} > V_{nom} \)).
Fig. 4.9 Example DC Gain Curves of New Resonant Converter (Mode II)

Fig. 4.10 Example of DC Gain Curves for New Resonant Converter (Mode I)
4.5 DC Gain Verification and Comparison

To verify the DC gain expression derived in section IV, a series of simulations have been performed for different $V_{pv}$ under a given load condition. The converter’s switching frequency $f_s$ is recorded. Equation (4.19) is used to calculate the DC gain result at a given $f_s$ for the same operation condition. Through the comparison between the DC gain from simulation and theoretical analysis result, the accuracy of (4.19) may be evaluated. Table 4.3 shows the comparison results for a 50% load condition. The DC gain in simulation $M_{\text{simulation}}$ is calculated by:

$$M_{\text{simulation}} = \frac{V_{\text{out}} \cdot N}{V_{pv} / 2}$$

(4.25)

<table>
<thead>
<tr>
<th>$V_{pv}$ (V)</th>
<th>$V_{out}$ (V)</th>
<th>$f_s$ (kHz)</th>
<th>$M_{\text{simulation}}$</th>
<th>$M_{\text{calculation}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>404</td>
<td>81</td>
<td>1.53</td>
<td>1.50</td>
</tr>
<tr>
<td>25</td>
<td>400.5</td>
<td>93</td>
<td>1.33</td>
<td>1.32</td>
</tr>
<tr>
<td>29</td>
<td>398.6</td>
<td>120</td>
<td>1.14</td>
<td>1.14</td>
</tr>
<tr>
<td>32</td>
<td>401.6</td>
<td>155</td>
<td>1.04</td>
<td>1.05</td>
</tr>
</tbody>
</table>
From Table 4.3, the DC gain from theoretical analysis matches with the simulation result very well for a given frequency. Therefore, the DC gain expression derived in last section is accurate enough for engineering design of the proposed converter.

Furthermore, a comparison of the DC gain between Mode I and Mode II operation is conducted in order to reveal the general DC gain features of proposed converter. The normalized frequency \( f_n \) has different base for Mode I and Mode II operation since they have different \( f_r \):

\[
f_{n_{\text{ModeI}}} = \frac{f_{SW}}{f_{r_{\text{ModeI}}}}, \text{ where } f_{r_{\text{ModeI}}} = \frac{1}{2\pi \sqrt{(L_{ijk} + L_r) \cdot C_r}} \quad (4.26)
\]

\[
f_{n_{\text{ModeII}}} = \frac{f_{SW}}{f_{r_{\text{ModeII}}}}, \text{ where } f_{r_{\text{ModeII}}} = \frac{1}{2\pi \sqrt{L_{ijk} \cdot C_r}} \quad (4.27)
\]

For further analysis, the \( f_n \) needs to be unified using the same base, for \( f_{n_{\text{Model}}} \):

\[
f_{n_{\text{Model}}} = \frac{f_{SW}}{f_{r_{\text{ModeII}}}} \cdot \frac{f_{r_{\text{ModeII}}}}{f_{r_{\text{ModeI}}}} = f_{n_{\text{ModeII}}} \cdot \frac{f_{r_{\text{ModeII}}}}{f_{r_{\text{Model}}}} = \alpha \cdot f_{n_{\text{ModeII}}} \quad (4.28)
\]

Both of the DC gain expressions for Mode I and Mode II can be written as functions of \( f_{n_{\text{ModeII}}} \):
\[ M_{\text{ModeI}} (f_{n_{\text{ModeI}}}) = \frac{1}{\sqrt{(1 + \lambda_{\text{ModeI}} - \frac{\lambda_{\text{ModeI}}}{\alpha \cdot f_{n_{\text{ModeI}}}})^2 + Q_{\text{ModeI}}^2 \left(\frac{\alpha \cdot f_{n_{\text{ModeI}}}}{\alpha \cdot f_{n_{\text{ModeI}}}} - 1\right)^2}} \] (4.29)

\[ M_{\text{ModeII}} (f_{n_{\text{ModeII}}}) = \frac{1}{\sqrt{(1 + \lambda_{\text{ModeII}} - \frac{\lambda_{\text{ModeII}}}{f_{n_{\text{ModeII}}}})^2 + Q_{\text{ModeII}}^2 \left(\frac{f_{n_{\text{ModeII}}}}{f_{n_{\text{ModeII}}}} - 1\right)^2}} \] (4.30)

**Table 4.4 A List of Parameters of Proposed Converter for Gain Analysis**

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>Mode I</th>
<th>Mode II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant tank parameters</td>
<td>N=1/24; L_{lkg}=200nH; L_r=600nH; L_m=1.85uH; C_r=3.4uF</td>
<td></td>
</tr>
<tr>
<td>Key Parameters</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| \( f_r\text{_{-ModeI}} \) | \( \frac{1}{2\pi \sqrt{(L_r + L_{lkg}) \cdot C_r}} \) | \( \frac{1}{2\pi \sqrt{L_{lkg} \cdot C_r}} \)
| \( Q_{\text{ModeI}} \) | \( \frac{Z_{0_{\text{ModeI}}}}{N^2 \cdot R_{0_{\text{ac}}}} \) | \( \frac{Z_{0_{\text{ModeII}}}}{N^2 \cdot R_{0_{\text{ac}}}} \)
| \( \lambda_{\text{ModeI}} \) | \( \frac{L_r + L_{lkg}}{L_m} \) | \( \frac{L_{lkg}}{L_m + L_r} \)
| \( Z_{0_{\text{ModeI}}} \) | \( \sqrt{\frac{L_r + L_{lkg}}{C_r}} \) | \( \sqrt{\frac{L_{lkg}}{C_r}} \)
| \( f_{n_{\text{ModeI}}} \) | \( \frac{f_{SW}}{f_r\text{_{-ModeI}}} \) | \( \frac{f_{SW}}{f_r\text{_{-ModeII}}} \)
Table 4.4 gives the resonant tank parameters for an example design. For comparison, the equations for calculating several key parameters are also listed in Table 4.4. The gain curves for the two operation modes can be plotted in the same figure, as shown in Fig. 4.11.

![DC gain comparison between Mode I and Mode II](image)

**Fig. 4.11 DC Gain Comparison between Mode I and Mode II at 50% Rated Power**

From Fig. 4.11, the two curves reach their peaks at the same frequency \( f_{n,M} \) defined by (4.31):

\[
f_{n,M} = \frac{f_M}{f_{n,ModeII}} = \frac{1}{2\pi \sqrt{(L_r + L_{kg} + L_m) \cdot C_r \cdot f_{n,ModeII}}}
\]  

(4.31)
Similar to the LLC resonant converter, operation in the region where \( f_n < f_{n,M} \) is forbidden. In the region \( f_{n,M} < f_n < f_0 \), \( M_{\text{model}} \) is always higher than \( M_{\text{modelI}} \). On the contrary, \( M_{\text{model}} \) becomes lower than \( M_{\text{modelII}} \) in region \( f_n > f_0 \). For a desired DC gain in the latter region, the following conclusions can be drawn:

1. Mode II operation requires a higher switching frequency than Mode I.
2. The frequency difference becomes larger with higher input voltage. Fig. 4.11 takes \( V_{pv} = 22 \text{V} \) and \( V_{pv} = 32 \text{V} \) as examples. It shows the switching frequency almost doubles if the converter operates in Mode II with 32V input.
3. The gain curve of Mode II becomes much flatter as frequency increases. The gain is almost constant and stops decreasing. Considering that higher \( V_{mpp} \) requires smaller DC gain, this implies the PV panel voltage may be out of regulation in mode II when \( V_{mpp} \) is too high. Therefore, it is reasonable to keep the converter operating in Mode I when \( V_{mpp} \) is higher than a predefined threshold voltage.

4.6 Design Example and Efficiency Analysis

The MIC will be operated with 60 or 72 cell crystallized PV panels which normally have a \( V_{mpp} \) of around 22V~45V. The nominal input voltage \( V_{nom} \) for this design is selected as 32V.
It will face a 400V DC bus with $P_{\text{rated}}=240\text{W}$.

<table>
<thead>
<tr>
<th>Manufacture/Part Number</th>
<th>Voltage Rating (V)</th>
<th>Current Rating (A)</th>
<th>25°C 100°C</th>
<th>Static on resistance(mΩ)</th>
<th>25°C 100°C</th>
<th>Total gate charge $Q_g$ (nc)</th>
<th>Body diode $t_{rr}$ (ns)</th>
<th>Body diode $Q_{rr}$ (nc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Infineon IPP034 NE7N3</td>
<td></td>
<td>100 100</td>
<td>3.0–3.4</td>
<td>4.0–4.7</td>
<td>88–117</td>
<td>50</td>
<td>76</td>
<td></td>
</tr>
<tr>
<td>Infineon IPP023 NE7N3</td>
<td></td>
<td>120 120</td>
<td>2.1–2.3</td>
<td>2.8–3.2</td>
<td>155–206</td>
<td>72</td>
<td>129</td>
<td></td>
</tr>
<tr>
<td>ST STP14 0NF75</td>
<td></td>
<td>120 100</td>
<td>6.5–7.5</td>
<td>9.75–1 1.25</td>
<td>160–218</td>
<td>115</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td>ST STP16 0N75F 3</td>
<td></td>
<td>120 120</td>
<td>3.5–4.0</td>
<td>5.25–6. 0</td>
<td>85</td>
<td>70</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>Fairchild FDP04 5N08</td>
<td></td>
<td>90 90</td>
<td>5.6–8.4</td>
<td>8–11</td>
<td>92–138</td>
<td>53</td>
<td>54</td>
<td></td>
</tr>
<tr>
<td>Fairchild FDB03 2N08</td>
<td></td>
<td>120 120</td>
<td>2.5–3.2</td>
<td>3.5–4.5</td>
<td>169–220</td>
<td>53</td>
<td>77</td>
<td></td>
</tr>
<tr>
<td>Vishay SUP90 N08-4 m8P</td>
<td></td>
<td>90 90</td>
<td>4–4.8</td>
<td>&lt;9.6</td>
<td>105–160</td>
<td>68–1 00</td>
<td>88–132</td>
<td></td>
</tr>
<tr>
<td>IR IRF775 9L2TR</td>
<td></td>
<td>160 113</td>
<td>1.8–2.3</td>
<td>2.7–3.4 5</td>
<td>200–300</td>
<td>64–9 6</td>
<td>150–225</td>
<td></td>
</tr>
</tbody>
</table>

The transformer primary side is the low voltage side and it has high resonant current circulating. On the contrary, the secondary side is the high voltage side with much smaller output current. Thus, the conduction loss mainly comes from the on-resistance $R_{\text{dson}}$ of
MOSFET and the copper loss of the transformers. In order to minimize the conduction loss, a MOSFET with low $R_{d\text{son}}$ is preferred and multi-strand Litz wire should be used to reduce the AC resistance of the primary winding of transformer. Switching loss is produced when MOSFETs are turned off. To reduce the switching loss, an additional snubber capacitor may be added in parallel with each MOSFET to reshape the MOSFET voltage trajectory during turn off. For the given input voltage range, a 75V power MOSFET can be used; this rating has enough voltage margin since soft switching dramatically reduces the voltage spike applied to the MOSFET. In addition, the energy stored in the leakage inductance of transformers will help create a soft switching environment instead of voltage spikes for MOSFET. Table 4.5 summarizes key parameters of several 75V MOSFETs from different manufacturers. The body diode performance is also regarded as an evaluation indicator since it has direct impact on the converter efficiency. From Table 4.5, MOSFETs IPP023NE7N3G from Infineon and FDP032N08 from Fairchild are good candidates due to low $R_{d\text{son}}$ and balanced performance. FDP032N08 was chosen for this design.

There is no strict limitation on volume and size for MICs. Thus, a lower switching frequency $f_s$ (<200 kHz) can be adopted to enhance converter efficiency. There is, however, a limitation for the converter height because the MIC should be mounted on the back of the PV panel. The module height cannot exceed the thickness of the panel rack or frame.
A proper core material is vital for transformer performance. Since the highest expected operation temperature of the transformer in a MIC should be lower than 100°C, high temperature cores like 3C93 from Ferroxcube are not necessary. For $f_s < 200$kHz, the core material 3C96 from Ferroxcube and N97 from EPCOS are both good candidates. They have lowest core loss in this frequency range. Finally N97 was chosen for this design. The threshold voltage $V_{th}$ for the operation mode decision is chosen to be equal to $V_{nom}$. One can design $C_r$, $L_r$, $L_m$ and $T_{x1}$ with a conventional design procedure for a LLC converter. Then a secondary winding is added to $L_r$ such that it forms the transformer $T_{x2}$. The devices $D_3$, $D_4$ and $S_3$ in HWR have the same current rating as $D_1$ and $D_2$ in voltage doubler. Considering that a practical transformer has a certain leakage inductance, the value of $L_{lkg}$ can be chosen to be 5%~15% of $(L_r+L_m)$. Table 4.6 gives component parameters for the MIC prototype.

<table>
<thead>
<tr>
<th>Design Parameter/component</th>
<th>Parameter Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant capacitor $C_r$</td>
<td>3.3uF/100V film capacitor</td>
</tr>
<tr>
<td>Magnetizing inductance of $T_{x1}$: $L_m$</td>
<td>1.85uH, ELP43/10/28-N97</td>
</tr>
<tr>
<td>Magnetizing inductance of $T_{x2}$: $L_r$</td>
<td>600nH, ELP43/10/28-N97</td>
</tr>
<tr>
<td>Turn-ratio of $T_{x1}$</td>
<td>2:24</td>
</tr>
<tr>
<td>Turn-ratio of $T_{x2}$</td>
<td>1:24</td>
</tr>
<tr>
<td>Leakage inductance: $L_{lkg}$</td>
<td>200nH</td>
</tr>
<tr>
<td>Primary MOSFET: $S_1$&amp;$S_2$</td>
<td>FDP032N08</td>
</tr>
<tr>
<td>Secondary Rectifier Diodes: $D_1$~$D_4$</td>
<td>STTH312</td>
</tr>
<tr>
<td>Secondary MOSFET: $S_3$</td>
<td>STP4N150</td>
</tr>
<tr>
<td>Gate driver for primary side MOSFET</td>
<td>ISL2110</td>
</tr>
<tr>
<td>Gate driver for secondary side MOSFET</td>
<td>ACPL-312U</td>
</tr>
<tr>
<td>Output Capacitors: $C_{o1}$~$C_{o3}$</td>
<td>1uF/630V film capacitor</td>
</tr>
</tbody>
</table>
A comprehensive loss analysis has been conducted to evaluate the efficiency of the designed converter for different input voltages under various load conditions. For comparison, the efficiency of a traditional LLC resonant converter with the same circuit parameters is also analyzed. Fig. 4.12 gives the estimated efficiency of this LLC converter. It can be seen that the converter efficiency drops quickly when generated power decreases from 50% $P_{\text{rated}}$ to 5% $P_{\text{rated}}$.

Fig. 4.12 Estimated Efficiency of Conventional LLC Converter with Same Parameters as used in the proposed converter
Fig. 4.13 Estimated Efficiency of Proposed Resonant Converter

Fig. 4.13 shows the estimated converter efficiency of the proposed converter. The efficiency curve becomes much “flatter” in Fig. 4.13 which indicates that the efficiency drop under 50%~5% $P_{\text{rated}}$ condition has been reduced significantly. For example, the efficiency improvement for $V_{\text{pv}}=22\text{V}$, $P_{\text{pv}}=10\% \ P_{\text{rated}}$ is around 8%; for $V_{\text{pv}}=32\text{V}$, $P_{\text{pv}}=5\% \ P_{\text{rated}}$, efficiency is increased by 14%.

From Fig. 4.12 and Fig. 4.13, the efficiency improvement can be calculated and is plotted in Fig. 4.14. The efficiency improvement drops when $P_{\text{pv}}$ increases. When $P_{\text{pv}}$ approaches 50% of $P_{\text{rated}}$, the efficiency improvement is reduced to almost zero. Meanwhile, $I_{\text{pri}}$ has a large current peak in positive cycle due to the output power increase. Therefore, there is no benefit to keep converter running in Mode II when $P_{\text{pv}}>50\%P_{\text{rated}}$ and mode change is
To gain a better understanding of the efficiency improvement in Mode II operation, a loss break-down is conducted for both Mode II operation and normal LLC operation with $V_{pv}<32V$ and $P_{pv}=10\%P_{\text{rated}}$.

Table 4.7 and Table 4.8 give the analysis results. As discussed in previous section, Mode II operation will increase the switching frequency. Thus, the switching loss of MOSFET may increase due to the increase in the number of switching events. However, the data in Table 4.8 shows a significant decrease in the total switching loss. This is because higher frequency operation leads to a much lower resonant current through the MOSFET during its turn-off event. For the same reason, the MOSFET conduction loss and transformer copper loss are
also greatly reduced. Moreover, the higher frequency operation reduces the transformer core loss by causing smaller variation of the magnetic field strength during a switching cycle. As a result, the total loss is dramatically reduced by Mode II operation.

Finally, Fig. 4.15 shows the weighted efficiency comparison results between the LLC resonant converter and the proposed converter. For $V_{pv} < 32V$, the weighted efficiency is increased by 1.5%~2% for proposed converter. This efficiency improvement is mainly due to the Mode II operation when $P_{pv} < 50\% P_{\text{rated}}$.

<table>
<thead>
<tr>
<th>$V_{pv}$ (V)</th>
<th>Switching frequency (kHz)</th>
<th>MOSFET Conduction Loss (W)</th>
<th>MOSFET Switching Loss (W)</th>
<th>Transformer Loss</th>
<th>Diodes Loss (W)</th>
<th>Total Loss (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>90</td>
<td>0.21</td>
<td>0.793</td>
<td>0.135</td>
<td>0.1</td>
<td>1.8</td>
</tr>
<tr>
<td>25</td>
<td>105</td>
<td>0.15</td>
<td>0.786</td>
<td>0.1</td>
<td>0.4</td>
<td>1.53</td>
</tr>
<tr>
<td>29</td>
<td>150</td>
<td>0.06</td>
<td>0.54</td>
<td>0.08</td>
<td>0.29</td>
<td>1.07</td>
</tr>
<tr>
<td>32</td>
<td>185</td>
<td>0.03</td>
<td>0.32</td>
<td>0.06</td>
<td>0.20</td>
<td>0.71</td>
</tr>
</tbody>
</table>

Table 4.8 Loss Break-down of LLC Converter with 10%*P_{\text{rated}} (V_{pv}\leq32V)

<table>
<thead>
<tr>
<th>$V_{pv}$ (V)</th>
<th>Switching frequency (kHz)</th>
<th>MOSFET Conduction Loss (W)</th>
<th>MOSFET Switching Loss (W)</th>
<th>Transformer Loss</th>
<th>Diodes Loss (W)</th>
<th>Total Loss (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>76</td>
<td>0.61</td>
<td>1.21</td>
<td>1.09</td>
<td>1.49</td>
<td>4.46</td>
</tr>
<tr>
<td>25</td>
<td>81.6</td>
<td>0.52</td>
<td>1.22</td>
<td>0.873</td>
<td>1.41</td>
<td>4.07</td>
</tr>
<tr>
<td>29</td>
<td>91</td>
<td>0.45</td>
<td>1.22</td>
<td>0.75</td>
<td>1.34</td>
<td>3.82</td>
</tr>
<tr>
<td>32</td>
<td>106</td>
<td>0.34</td>
<td>1.16</td>
<td>0.46</td>
<td>0.98</td>
<td>3.01</td>
</tr>
</tbody>
</table>
4.7 Experiment Verifications

An experimental prototype has been built to verify the performance of proposed converter. Fig. 4.16 depicts the system diagram for experiment.

Three PV panels “MSX77S” in series connection are used as the input source. An electronic load running in constant voltage mode is connected to the output of the converter to emulate the 400V DC bus. A maximum power point tracking (MPPT) controller is
implemented using a microcontroller. The MPPT controller provides a reference voltage $V_{pv \_ref}$ to the DC/DC controller which has a compensator loop and will regulate the PV panel voltage according to $V_{pv \_ref}$. The DC/DC controller contains a mode change controller which will determine the operation mode based on the criteria in Table 4.2. An auxiliary power supply is implemented to power up the control circuitry. A protection block will continuously monitor $V_{pv}$, $V_{DC \_bus}$, $I_{pri}$ and heat-sink temperature. It will respond to several kinds of unusual situations, such as an abnormal DC bus voltage, over current, or over temperature conditions.

![System Diagram for the Experiment](image)

Fig. 4.16 System Diagram for the Experiment

Once the converter is connected with the PV panels and the DC bus in the IEM, it will start
to operate following the procedure shown in Fig. 4.17. The DC/DC controller will check $V_{pv}$ and $P_{pv}$ every few minutes to decide in which mode the converter should operate. The unwanted $V_{pv}$ undershoot/overshoot during the mode transition may lead to an erroneous response of the MPPT controller since the MPPT may determine the variation of $V_{pv}$ during transition is due to an environmental change. To avoid this problem, the MPPT controller is suspended prior to mode changes. The latest value of $V_{pv\_ref}$ is recorded and will be used as the initialized operation point for PV panels after a mode change.

![Flowchart of Converter Operation after Start-up](image-url)

Fig. 4.17 The Flowchart of Converter Operation after Start-up
Fig. 4.18 shows a picture of the 240W MIC prototype. The converter uses natural convection cooling. Several flat copper bars are used to conduct the primary side resonant current for loss reduction purposes.

Fig. 4.18 A Picture of 240W MIC Prototype

Fig. 4.19 and Fig. 4.20 show the operation waveforms of MIC prototype in Mode I and Mode II with different input voltages ranging from 5% $P_{\text{rated}}$ to 100% $P_{\text{rated}}$. Only the positive part of current $I_{\text{sec}_\text{TX1}}$ will flow through the HWR. Since $I_{\text{sec}_\text{TX1}}$ returns to zero before each half cycle ends, ZCS turn off of diodes $D_1$~$D_3$ is realized. Fig. 4.21 verifies the ZVS feature of the proposed converter for Mode II operation. It clearly shows that ZVS turn on is achieved for both the high side and the low side MOSFET in Mode II. Fig. 4.22 shows how
the converters will respond to two types of protection: slow protection and fast protection. Slow protection is particularly designed for over temperature protection. Once the slow fault protection mechanism is triggered, the converter will enter “burst” mode operation several times and then shut down if the slow fault signal still exists. The fast fault protection attempts to protect the converter from severe damage when over current or over voltage conditions occur. Once the fast fault protection is triggered, the converter will shut down immediately.

Fig. 4.23 demonstrates the MPPT function of designed MIC. During start up, the MPPT controller will send \( V_{pv, \text{ref}} \) to initialize \( V_{pv} \) to a predefined value. Then at the time \( t=t_s \), the MPPT algorithm starts to search the maximum power point and finally \( V_{mpp} \) is reached. In the experiment, the perturbation & observation method [99] is implemented for MPPT. As shown in Fig. 4.23, the \( I_{pv} \) and \( V_{pv} \) will oscillate around the \( V_{mpp} \) in steady state.
Fig. 4.19 (a) $V_{in}=36\, \text{V}, 10\% \, \text{Load}$

Fig. 4.19 (b) $V_{in}=36\, \text{V}, 100\% \, \text{Load}$
Fig. 4.19 Waveforms of MIC in Mode I (ch1: 10V/div; ch4: 10A/div; t=4µs)
Fig. 4.20 Waveforms Mode II Operation (ch1:50V/div; ch2: 200V/div; ch3: 1A/div; ch4: 10A/div)
(a) Verification of ZVS of Upper Side Switch: $V_{in}=22V$, 20% Load

(b) Verification of ZVS of Lower Side Switch: $V_{in}=22V$, 20% Load

Fig. 4.21 Waveforms to Verify the ZVS Operation in Mode II (ch1:10V/div; ch2: 20V/div; ch4: 10A/div)
(a) Verification of Slow Fault Protection

(b) Verification of Slow Fault Protection

Fig. 4.22 Waveforms to Verify the ZVS Feature of MIC Prototype in Mode II Operation

(ch1:10V/div; ch2: 20V/div; ch4: 10A/div)
(a) Startup (ch1: 50V/div, ch2: 1A/div, ch3: 20V/div, M1:40W/div)

(b) Steady-state (ch1: 50V/div, ch2: 500mA/div, ch3:2V/div, AC coupled)

Fig. 4.23 Waveforms to Verify the MPPT Function
The efficiency of proposed converter under different $V_{pv}$ and $P_{pv}$ is measured in the experiment. For comparison, the efficiency of operation without the HWR (normal LLC operation) is also recorded. Fig. 4.24 shows the efficiency difference between Mode II operation and normal LLC operation. From Fig. 4.24, maximum efficiency improvement happens at 5% of $P_{\text{rated}}$ for all input conditions. For this condition, greater than 10% efficiency improvement is achieved. With an increase of the load, efficiency improvement drops. Fig. 4.25 gives the weighted efficiency improvement based on the data in Fig. 4.24: at least 2% improvement is observed in the experiment for $V_{pv}<32V$. Fig. 4.26 and Fig. 4.27 give the complete efficiency measurement results and weighted efficiency data for the MIC prototype, respectively. A high efficiency of 96.5% occurs in Mode II with $V_{pv}=32V$ and 50% load condition. The highest weighted efficiency reached in the experiment is 95.8%.

![Measured Efficiency Improvement with HWR (5%-50% load)](image)

Fig. 4.24 Measured Efficiency Improvements with HWR (Mode II) for 5%~50% $P_{\text{rated}}$
Fig. 4.25 Weighted Efficiency Improvements with HWR in Mode II

Fig. 4.26 Efficiency Measurement Results for Designed MIC Prototype
Fig. 4.27 Weighted Efficiency Data for Proposed MIC Prototype

4.8 Summary

The FREEDM system provides an advanced renewable energy management platform. PV converters can take advantage of the 400V DC bus in FREEDM systems to reduce the PV converter’s complexity and costs to the end user. In fact, the PV power generation in the FREEDM system has features similar to those of the distributed MPPT technology. The DC MICs are good candidates for module level D-MPPT structure. In order to obtain a high energy yield, DC MICs need to maintain high efficiency for a wide input range under different load conditions. The comparison in this Chapter shows that the parallel connected
DC MICs have more advantages than the series MICs. However, the high conversion gain required by parallel structure is the major factor limiting its efficiency. In this Chapter, a high efficiency dual mode resonant converter topology is proposed for paralleled connected DC MICs. The new resonant converter may change resonant modes adaptively depending on the PV panel operation conditions. In both resonant modes, zero-voltage switching (ZVS) for the primary side switches and ZCS for the secondary side diodes are achieved. A detailed theoretical analysis of the converter operation and its DC gain features are presented and verified in this Chapter. The new converter’s performance has been validated by the experimental results from a 240W prototype with an embedded MPPT controller. The highest weighted efficiency of the proposed prototype is around 96% and big efficiency improvement for low input, low output power level condition is observed, which makes this topology a promising candidate for this specific application.
Chapter 5. Low Cost Analog MPPT Controller for Single Chip “MPPT Regulator” Solution

5.1 Research Motivation

Making the PV panel work at its maximum power point (MPP) is always important for any PV applications for three reasons:

(1) The PV panel’s unique characteristics [68]. The PV cell is a specially designed PN junction or Schottky barrier device. Fig. 5.1 gives the simplified circuit model of the PV cell.

Fig. 5.1 Simplified Circuit Model for PV Cell
The cell may be regarded as a voltage controlled current source whose output current is a function of the terminal voltage. The two resistors, $R_s$ and $R_{ph}$ are lumped resistors to represent the series and parallel resistance. The $R_s$ is pretty small whereas $R_{ph}$ is very large. Hence, both of them may be removed from the model in the ideal case. Without considering the resistance, the operation characteristic of the PV cell may be described by the equation below [68]:

$$I = I_{ph} - I_o \left(e^{qV/kT} - 1\right)$$  \hspace{1cm} (5.1)

Where, $I_{ph}$ – light-generated current (A)

$I_o$ – saturation current (A)

$q$ – $1.6*10^{-19}$ Coulomb

$K$ – Boltzmann constant

$T$ – cell absolute temperature, Kelvin

$i$ and $v$ – panel current and voltage

Fig. 5.2 shows a PV panel and its characteristic curves under different irradiance levels. The voltage at the maximum power point ($V_{mpp}$) varies a little with the change of irradiance.
However, the $V_{\text{mpp}}$ is strongly dependant on cell temperature. Table 5.1 gives several typical temperature coefficients to describe the PV panel temperature characteristics. The $P_{\text{max}}$ is the maximum output power at $V_{\text{mpp}}$; $V_{\text{oc}}$ is the PV panel open circuit voltage; $I_{\text{sc}}$ is the
PV panel short circuit current. Both $P_{\text{max}}$ and $V_{oc}$ will decrease with the temperature rise but $I_{sc}$ has a positive temperature coefficient.

(2) The PV panel’s high price [103] contributes more than 50% to the total system installation cost. To make the solar power a viable and economic source for future power needs, the total system cost should be reduced by about 75% before the end of the decade [101]. It is estimated by the U.S. Department of Energy (DOE) that a $1/Watt$ (peak) installed PV energy system-equivalent to 5-6 cents/kWh, would make solar, without additional subsidies, competitive with electric generating systems using fossil fuels, nearly everywhere in the U.S [102].

(3) The MPPT tracking accuracy has direct impact on the energy yield of the PV system. At present, many MPPT methods have been developed and they are reviewed in [99]. Most of them are implemented digitally, either in a microcontroller (MCU) or Field Programmable Gate Array (FPGA). The benefit from digital implementation is that those advanced MPPT algorithms may be used and better tracking performance may be achieved. Alternatively, the MPPT can be implemented by analog circuitry [99] [104-109]. The potential benefit from analog solution is that the MPPT can be integrated with a DC/DC controller to form a single chip solution “MPPT Regulator” which may reduce the development complexity and system cost. The MPPT Regulator is able to be widely used in the DC/DC stage in module level or string level distributed MPPT applications. As discussed
in chapter II, the module level and string level distributed MPPT stage is usually comprised of a single DC/DC stage with an MPPT controller and the control task for the DC/DC controller is greatly reduced. As a result, a low cost analog DC/DC controller IC chip may be used instead of a dedicated digital controller. Thus, there is a demand for an analog MPPT solution which can be integrated with the existing DC/DC control IC chip to achieve a single chip low cost solution. It may also be used for those off grid low power PV applications, such as PV powered battery chargers. In fact, integration of certain functions into a normal DC/DC controller chip is the most desirable way for special applications to reduce the implementation complexity and system cost. For example, the analog control chip for cold cathode fluorescent lamp (CCFL) has several circuit blocks dedicated to CCFL application, such as lamp ignition control block, dimming control block and a PM-Bus communication block to receive the control command from the system controller. Another example is the single phase power factor correction (PFC) control chip. A current regulation block inside this chip will generate proper reference signals based on the sensed grid side voltage and current. Generally, these kinds of specially designed control ICs greatly reduce the design difficulty and as a result, the corresponding system cost is reduced.

Among these existing analog MPPT solutions, however, some of them are unable to find the real MPP. The approach in [104] will do a voltage sweep from 0V to $V_{OC}$ periodically to obtain the $I_{PV}$-$V_{PV}$ characteristic curve first in order to find the MPP, where $V_{OC}$ is open
circuit voltage of the PV panel. This voltage sweep will be repeated frequently in order to update the $V_{\text{MPP}}$ because $V_{\text{MPP}}$ is changing due to the variation of environmental temperature and sun irradiance. Apparently, it cannot make instantaneous response to these variations during two sweep intervals. Also the periodic sweep may cause significant power loss in practice. The method in [105] calculates the $V_{\text{mpp}}$ by equation $V_{\text{mpp}} = M_V * V_{\text{oc}}$, where $M_V$ is a pre-defined coefficient (approximately 0.7~0.8) from the PV panel datasheet. Other than directly checking the $V_{\text{mpp}}$, the method will measure the $V_{\text{oc}}$ periodically such that the $V_{\text{mpp}}$ is also regularly updated. Similar to the previous method in [104], this method still cannot respond to $V_{\text{mpp}}$ change instantaneously and usually the operation point is shifted away from the real MPP because the $M_V$ also varies. In [106], the MPPT controller is integrated with a PWM controller successfully but its algorithm is the same as that in [105]. In [107] the MPPT is based on one-cycle control (OCC) and it functions well as long as the panel temperature variation is small [99].

In addition, some of the existing analog methods depend on the converter topologies or their control method. The approach in [107] can only work with OCC and approach in [108] can only be used for SEPIC, Cuk converter or their derived circuits. The performance of RCC method in [109] works well and it is unique. However, it may not function well if the voltage or current ripple of the converter is too small. As a result, there is an inherent limitation of the MPP tracking accuracy.
Moreover, Table 5.2 [99] indicates that only three types of MPPT technique which may find the accurate MPP is able to be implemented by analog circuitry. These techniques are Hill-climbing/P&O, RCC and State-based MPPT. Considering the high complexity of State-based MPPT and the drawbacks of the RCC method mentioned above, neither of them are good candidates.

<table>
<thead>
<tr>
<th>MPPT Technique</th>
<th>PV Array Dependent?</th>
<th>True MPPT?</th>
<th>Analog or Digital?</th>
<th>Speed</th>
<th>Implementation Complexity</th>
<th>Sensed Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&amp;O</td>
<td>No</td>
<td>Yes</td>
<td>Both</td>
<td>Varies</td>
<td>Low</td>
<td>V, I</td>
</tr>
<tr>
<td>IncCond</td>
<td>No</td>
<td>Yes</td>
<td>Digital</td>
<td>Varies</td>
<td>Medium</td>
<td>V, I</td>
</tr>
<tr>
<td>Fractional Voc</td>
<td>Yes</td>
<td>No</td>
<td>Both</td>
<td>Medium</td>
<td>Low</td>
<td>V</td>
</tr>
<tr>
<td>Fractional Isc</td>
<td>Yes</td>
<td>No</td>
<td>Both</td>
<td>Medium</td>
<td>Medium</td>
<td>I</td>
</tr>
<tr>
<td>Fuzzy Logic Control</td>
<td>Yes</td>
<td>Yes</td>
<td>Digital</td>
<td>Fast</td>
<td>High</td>
<td>Varies</td>
</tr>
<tr>
<td>Neutral Network</td>
<td>Yes</td>
<td>Yes</td>
<td>Digital</td>
<td>Fast</td>
<td>High</td>
<td>Varies</td>
</tr>
<tr>
<td>RCC</td>
<td>No</td>
<td>Yes</td>
<td>Analog</td>
<td>Fast</td>
<td>Low</td>
<td>V, I</td>
</tr>
<tr>
<td>Current Sweep</td>
<td>Yes</td>
<td>Yes</td>
<td>Digital</td>
<td>Slow</td>
<td>High</td>
<td>V, I</td>
</tr>
<tr>
<td>DC Link Capacitor Droop Control</td>
<td>No</td>
<td>No</td>
<td>Both</td>
<td>Medium</td>
<td>Low</td>
<td>V</td>
</tr>
<tr>
<td>Load I or V Maximization</td>
<td>No</td>
<td>No</td>
<td>Analog</td>
<td>Fast</td>
<td>Low</td>
<td>V, I</td>
</tr>
<tr>
<td>dP/dV or dP/dV Feedback Control</td>
<td>No</td>
<td>Yes</td>
<td>Digital</td>
<td>Fast</td>
<td>Medium</td>
<td>V, I</td>
</tr>
<tr>
<td>Array Reconfiguration</td>
<td>Yes</td>
<td>No</td>
<td>Digital</td>
<td>Slow</td>
<td>High</td>
<td>V, I</td>
</tr>
<tr>
<td>Linear Current Control</td>
<td>Yes</td>
<td>No</td>
<td>Digital</td>
<td>Fast</td>
<td>Medium</td>
<td>Irradiance</td>
</tr>
<tr>
<td>$I_{MPPT}$ &amp; $V_{MPPT}$ Computation</td>
<td>Yes</td>
<td>Yes</td>
<td>Digital</td>
<td>N/A</td>
<td>Medium</td>
<td>Irradiance, Temperature</td>
</tr>
<tr>
<td>State-based MPPT</td>
<td>Yes</td>
<td>Yes</td>
<td>Both</td>
<td>Fast</td>
<td>High</td>
<td>V, I</td>
</tr>
<tr>
<td>OCC MPPT</td>
<td>Yes</td>
<td>No</td>
<td>Both</td>
<td>Fast</td>
<td>Medium</td>
<td>I</td>
</tr>
<tr>
<td>BFV</td>
<td>Yes</td>
<td>No</td>
<td>Both</td>
<td>N/A</td>
<td>Low</td>
<td>None</td>
</tr>
<tr>
<td>LRCM</td>
<td>Yes</td>
<td>No</td>
<td>Digital</td>
<td>N/A</td>
<td>High</td>
<td>V, I</td>
</tr>
<tr>
<td>Slide Control</td>
<td>No</td>
<td>Yes</td>
<td>Digital</td>
<td>Fast</td>
<td>Medium</td>
<td>V, I</td>
</tr>
</tbody>
</table>
Concluding the above discussion, the most desirable approach for universal analog MPPT is the P&O method. Moreover, for the target PV applications, particularly for the module level distributed MPPT application, the P&O method is capable of obtaining a satisfactory tracking result. However, there is an implementation problem with this method dealing with how to implement the algorithm with simple circuits and how to store the value of \( V_{pv} \) and \( P_{pv} \) in last perturbation cycle. This is a challenge for analog MPPTs.

In this Chapter, a truth table is extracted from the P&O algorithm. Based on this table, the analog MPPT controller may only need to use several logic gates to realize the tracking algorithm. Meanwhile, the concept of a capacitor based storage cell is proposed to save the value of \( V_{pv} \) and \( P_{pv} \) in the last perturbation cycle. In one of the storage cells, the capacitor voltage is proportional to the PV panel voltage and it may be adjusted in each perturbation cycle. The minimum voltage step of perturbation may be set by the combination of amplitude of charge (discharge) current and the time duration of charge (discharge) action. The cost of the proposed solution is evaluated and design considerations are suggested. The tracking performance of the proposed technique has been verified by both the simulation and experimental results with 200W PV panels at different irradiance levels.
5.2 New Analog MPPT Controller and Its Operation Principle

5.2.1 Concept for Single Chip MPPT Solution

Fig.5.3 depicts the system diagram of the distributed MPPT application with single chip MPPT solution.

In this System, the output voltage of the DC/DC converter is equal to battery voltage or it is regulated by a cascaded grid-tied inverter based on power transfer balance [3] [12]. For the DC/DC converter, it will regulate the PV panel side voltage $V_{pv}$ to a desired value according to the reference signal from MPPT controller such that the PV panel is made to operate at its...
MPP. The DC/DC converter should have a proper conversion gain to satisfy the voltage conversion ratio set by the $V_{\text{mpp}}$ and $V_{\text{out}}$ [110~111]. The proposed analog MPPT controller may be integrated with any kind of existing DC/DC controller chips to form a single chip MPPT solution: the MPPT Regulator.

As shown in Fig. 5.3, the analog MPPT controller has two input signals: PV panel voltage $V_{\text{pv}}$, panel current $I_{\text{pv}}$. The output signal from MPPT controller is a reference signal for DC/DC controller and its value will keep updating once MPPT starts running.

### 5.2.2 The Truth Table Extracted from P&O Algorithm

Fig. 5.4 redraws the PV panel’s characteristic curve. When operating on the left side of the MPP, incrementing the panel voltage will increase the power; whereas operating on the right side of MPP, incrementing the panel voltage will decrease the power.

![Fig. 5.4 Typical P-V Curve of a PV Panel](image)

---

160
By continuously injecting perturbation onto the panel voltage or current and observing the variation of output power, the MPP may be reached when following the algorithm summarized in Table 5.3, which is also known as the P&O method.

<table>
<thead>
<tr>
<th>Present Perturbation</th>
<th>Change in Power</th>
<th>Next Perturbation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive</td>
<td>Positive</td>
<td>Positive</td>
</tr>
<tr>
<td>Positive</td>
<td>Negative</td>
<td>Negative</td>
</tr>
<tr>
<td>Negative</td>
<td>Positive</td>
<td>Negative</td>
</tr>
<tr>
<td>Negative</td>
<td>Negative</td>
<td>Positive</td>
</tr>
</tbody>
</table>

In Table 5.3, if “positive” is defined as logic “1” and “negative” is defined as logic “0”, a truth table (Table 5.4) may be derived which implies that the algorithm may be implemented by simple logic circuitry. Moreover, if we take “perturbation” and the “change in power” as two inputs and the “next perturbation” as output, the logic relationship between the inputs and output matches that of an XNOR gate, as shown in Fig. 5.5. The only difference is that the P&O method is a sequential logic which is time dependant; but the XNOR gate is operated based on the combination logic which does not have time constraints [112]. This is because for P&O method, the next perturbation is based on direction of the previous perturbation. As a result, with the derived truth table, the P&O algorithm may be implemented around an XNOR gate with some other logic circuitry.
Table 5.4 Derived Truth Table for Analog Implementation of P&O Algorithm

<table>
<thead>
<tr>
<th>Present Perturbation</th>
<th>Change in Power</th>
<th>Next Perturbation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Fig. 5.5 Symbol of XNOR Gate and Its Logic Truth Table

5.2.3 The Storage Cells

As mentioned before, the P&O method is a sequential logic. Therefore, the values of $V_{pv}$ and $P_{pv}$ in the last perturbation cycle need to be saved and they will be used to determine the next perturbation direction. These values may be converted by an A/D converter and saved in the memory of a microcontroller. Alternatively, a low cost storage cell may be implemented with a capacitor where the capacitor voltage is proportional to the $V_{pv}$ and $P_{pv}$. It is true that a capacitor may not hold a level of voltage constantly for a long time due to its inherent characteristics. However, the capacitor voltage may be nearly constant for a short time period,
i.e., several milliseconds. By properly choosing the circuit parameters, capacitor based storage cells may be used in the analog implementation of P&O method. Fig. 5.6 depicted several kinds of capacitor based storage cells for this application.

Fig. 5.6 Three Capacitor Based Storage Cell Structures

The simplest structure (Fig. 5.6(a)) uses two constant voltage sources to charge (discharge) the capacitor through a resistor $R$. The charge current $I_{\text{charge}}$ and discharge current $I_{\text{discharge}}$ may be calculated easily by equation (5.2):
\[
\begin{align*}
    i_{\text{charge}} &= \frac{V_1 - V_C}{R} \\
    i_{\text{discharge}} &= \frac{V_C - V_2}{R}
\end{align*}
\] (5.2)

$I_{\text{charge}}$ and $I_{\text{discharge}}$ are equal only when equation (5.3) is satisfied:

\[ V_2 = 2V_C - V_1 \] (5.3)

Obviously, the $I_{\text{charge}}$ and $I_{\text{discharge}}$ will be unequal for most cases in practice and large oscillation around $V_{\text{mpp}}$ may occur. As a result, the MPPT performance will be affected. In order to solve this issue, a voltage feedback circuit is added, as shown in Fig. 5.6(b). In this case, $V_2$ is no longer constant and equation (5.3) may be satisfied. Thus, $I_{\text{charge}}$ is equal to $I_{\text{discharge}}$ in the adjacent two cycles. However, the current still varies with different $V_C$ which leads to the change of perturbation voltage step. To obtain a constant perturbation step, a current mirror based storage cell is proposed, as shown in Fig. 5.6 (c). The benefit from this structure is that $I_{\text{charge}}$ and $I_{\text{discharge}}$ are constant and it may be controlled precisely by properly sizing the transistors. The transistors N5 and P5 are switches related to discharge (charge)
action. In an ideal case [113], the $I_{\text{charge}}$ and $I_{\text{discharge}}$ may be calculated by equation (5.4), where $W_N$ and $L_P$ represent the width and length of the corresponding transistors.

$$
\begin{align*}
I_{\text{charge}} &= \frac{V_{cc}}{R_i} \cdot \frac{R_{s1}}{R_{s1} + R_{s2}} \cdot \frac{(W_{P3})/(W_{P4})}{L_{P3}/L_{P4}} \\
I_{\text{discharge}} &= -\frac{V_{cc}}{R_i} \cdot \frac{R_{s3}}{R_{s3} + R_{s4}} \cdot \frac{(W_{N3})/(W_{N2}) \cdot (W_{P2})/(W_{P1})}{L_{N3}/L_{N2} \cdot L_{P2}/L_{P1}}
\end{align*}
$$

Define current mirror conversion gain $G_{M1}$ and $G_{M2}$:

$$G_{M1} = \frac{(W_{P3})/(W_{P4})}{L_{P3}/L_{P4}}$$  

(5.5)

$$G_{M2} = \frac{(W_{N3})/(W_{N2}) \cdot (W_{P2})/(W_{P1})}{L_{N3}/L_{N2} \cdot L_{P2}/L_{P1}}$$  

(5.6)

For convenience, $R_{S1}$ is selected to be equal to $R_{S3}$ and $R_{S2}$ is equal to $R_{S4}$. Thus, $I_{\text{charge}}$ matches with $I_{\text{discharge}}$ when $G_{M1}$ is the same as $G_{M2}$. The third storage cell structure has been chosen for the analog MPPT implementation. In total two cells are used to store scaled $V_{pv}$ and $P_{pv}$ value. The capacitor voltage in these storage cells may be initialized to a
predetermined value before MPPT starts. For example, in the storage cell for $V_{pv}$, the capacitor voltage is initialized to the scaled $V_{mpp}$ from PV panel datasheet in order to reduce the searching time before reaching $V_{mpp}$.

5.2.4 Circuit Diagram of New Analog MPPT and Its Operation Principle

Fig.5.7 depicts the circuit diagram of the proposed analog MPPT controller. The PV panel voltage and current must be sensed and then filtered by a low pass filter (LPF) such that those switching frequency ripples may be removed. An analog multiplier is used to calculate the instantaneous output power of the PV panel. The frequency of CLK signal is usually divided by a frequency divider “Fre_Div” if CLK comes from SYNC signal of a PWM controller considering the frequency of SYNC signal is in the range of dozens ~ hundreds of kHz. Another reason for the frequency division is that the limited bandwidth of a DC/DC converter will not allow the MPPT controller to update $V_{pv,ref}$ at the switching frequency. The control loop bandwidth of DC/DC converter is usually 1/5~1/10 of the switching frequency. Thus the CLK is usually divided by 16~256 to ensure the converter has already entered steady-state operation before next perturbation cycle comes.
Fig. 5.8 Timing Diagram of Proposed MPPT Controller

Fig. 5.8 gives the timing diagram of the MPPT controller. Each perturbation cycle may be divided into 3 phases. The operation in each phase is described below:
**Phases 1 (t0~t1):** A new perturbation cycle begins at the rising edge of CLK_0. The \( P_{pv} \) will be sampled using sample and hold \( S_H \) during this period.

**Phases 2 (t2~t3):** The perturbation direction for next cycle will be determined based on the comparison results of \( P_{pv}(k) \) and \( P_{pv}(k-1) \), where \( P_{pv}(k) \) represents the sampled result of \( P_{pv} \) in the present cycle and \( P_{pv}(k-1) \) is the stored \( P_{pv} \) value in the last cycle. Also the \( C_{V_{pv}} \) (the capacitor in the storage cell for \( V_{pv} \)) will be charged (discharged) once Timer is high such that the voltage reference \( V_{pv,ref} \) is updated. The duration time for high level of Timer is determined by the block III in Fig. 5.7. The minimum voltage step change of PV panel voltage can be calculated by the equation 5.7 below:

\[
\Delta V_{pv} = K \cdot \frac{I_{p1}}{C_{V_{pv}}} \cdot \Delta t
\]  

(5.7)

Where \( K \) is a constant scaling factor; \( I_{p1} \) is the amplitude of the current for charge (discharge) capacitor; \( C_{V_{pv}} \) is the storage capacitor value and \( \Delta t = t_3 - t_2 \). The gate signals for the storage cell I are generated by block IV in Fig. 5.7.

**Phases 3 (t4~t5):** During this period, the \( C_{P_{pv}} \) will be charged (discharged) such that its voltage is updated to be equal to the present value of \( P_{pv} \) and will be referred as \( P_{pv}(k-1) \) for the next cycle. The logic circuit in block II will generate proper gate signals for storage cell II. Basically, the operation of the new MPPT controller follows the flow chart of the standard
P&O method. The intentional delays inserted between \( t_1 \sim t_2 \) and \( t_3 \sim t_4 \) will help the controller meet the timing requirement. The circuit blocks I~IV in Fig. 5.7 have different functions. The block I (main block) will decide the perturbation direction for next cycle. Fig. 5.9 displays the key waveforms to illustrate its operation. In this case, the MPPT starts with a voltage higher than \( V_{mpp} \) and \( V_{pv\_ref} \) continues to decrease until \( V_{mpp} \) is reached. Finally the \( V_{pv\_ref} \) oscillates around \( V_{mpp} \). The time period \( t_0 \) represents the initialization period. The comparator output CMD is updated at the rising edge of CLK_0 and the outputs of the two flip-flops are refreshed at the rising edge of CLK_2. The period \( \alpha \) indicates the time required to update the \( C_{ppv} \)'s voltage after the rising edge of CLK_2. If the \( P_{pv}(k) \) is greater (smaller) than \( P_{pv}(k-1) \), the \( C_{ppv} \) will be charged (discharged). And once its voltage is higher (lower) than \( P_{pv}(k) \), the CMD will toggle and discharge/charge ends. The time period \( \delta \) means the time delay between CLK_2 rises and D updates. Block II and IV are control blocks for storage cells. They will generate corresponding signals to update the voltage of storage capacitors. Block III will control the time length \( \Delta t \) in equation (5.7). Fig. 5.10 gives the key waveforms for block II~IV.
5.2.5 Requirements for the Analog Multiplier

In the proposed MPPT controller, an analog multiplier is necessary and it is a major concern from the point of view of cost. Usually a multiplier which can work in 4 quadrants with high accuracy and high speed will add high cost to the system. For this application, the multiplier works only in the first quadrant. Considering the P&O algorithm makes decisions...
according to the variation trend of $P_{pv}$ other than accurate $P_{pv}$ in the adjacent two perturbation cycles, high accurate multiplier is unnecessary. But the linearity of the multiplier is an important parameter. Additionally, the proposed solution is not intended to be used in a satellite system or PV powered racing car where sun irradiance level varies rapidly. Therefore, the required perturbation frequency of P&O algorithm is not very high. Meanwhile, a DC/DC converter with lower switching frequency (dozens of kHz) is preferred for this application since the size is not the major concern and the converter will not face extremely fast load transition. Consequently, the converter’s bandwidth is usually several kHz for this case. If the perturbation of $V_{pv_{-}ref}$ is regarded as a disturbance to the converter’s control loop, the perturbation frequency cannot exceed the converter’s bandwidth. Otherwise, the control loop cannot follow the reference and PV panel voltage will be out of regulation. Therefore, from this point view, the MPPT block’s highest clock frequency should be around hundred Hertz. This result also implies that the analog multiplier will not work at a high speed.

To summarize the discussion above, the analog multiplier for this application does not need 4 quadrants of operation, high accuracy or high speed; but it must have satisfied linearity. Similar to the PFC controller, a low speed low cost multiplier will be used and one of these kinds of multipliers is depicted in Fig. 5.11 [114].
5.3 Design Considerations

To achieve satisfactory tracking performance, the parameters for the proposed MPPT controller, such as initial value for storage cells, minimum perturbation voltage step and clock frequency, need to be properly selected. As discussed above, the clock frequency should be lower than the bandwidth of DC/DC converter. Other parameters may be adjusted by changing the value of the resistors shown in Fig. 5.12. These are all external resistors and may be set by the user. Once the manner of the PV modules connected to the distributed MPPT stage is determined, the parameters for the MPPT controller may be designed.
accordingly. Here is a design example for module level districted MPPT application. The PV module datasheet usually will list following parameters:

- $V_{oc}$: module open circuit voltage
- $V_{mpp}$: module voltage at the MPP specified in datasheet.
- $P_{mpp}$: module output power at the MPP specified in datasheet.

And some other circuit parameters are listed here also:

- $G_V$: voltage sensor gain for $V_{PV}$
- $G_I$: current sensor gain for $I_{PV}$
- $G_{M1}$ and $G_{M2}$: current mirror conversion gain, $G_{M1} = G_{M2} = G_M$
- $t_{timer}$: high duration of signal “Timer” in each cycle
- $ΔV$: minimum perturbation voltage step

Fig. 5.12 Analog MPPT Controller with External Components
Then the MPPT controller’s parameters may be calculated by following the 4 step design procedure below:

(1) Choose a proper $\Delta V$. $\Delta V=0.5\% V_{oc}$ is valid for most cases.

(2) Choose resistors $R_{s5}$~$R_{s8}$ and $C_{_V pv}$ based on $\Delta V$. Usually choose $R_{s5}=R_{s7}$ and $R_{s6}=R_{s8}$.

The following equation may be derived:

$$\frac{R_{s5}}{R_{s5} + R_{s6}} \times \frac{1}{C_{_V pv}} = \frac{\Delta V}{G_M \times t_{_timer}} \times \frac{R_i}{V_{CC}} \quad (5.8)$$

Once $R_{s5}$ and $R_{s6}$ are defined, capacitor $C_{_V pv}$ can be calculated by (5.8).

(3) Set the initial value for storage cells. Choose resistor $R_1$ and $R_3$ first. And then $R_2$ and $R_4$ can be calculated by:

$$\begin{align*}
R_2 &= \frac{V_{mpp} \times G_V}{V_{CC} - V_{mpp} \times G_V} \times R_1 \\
R_4 &= \frac{P_{mpp} \times G_V \times G_I}{V_{CC} - V_{mpp} \times G_V \times G_I} \times R_3 \\
\end{align*} \quad (5.9)$$

In this case, voltage of $C_{_P pv}$ and $C_{_V pv}$ are initialized to $P_{mpp} \times G_V \times G_I$ and $V_{mpp}$ respectively.
(4) At the end of each cycle, the voltage of capacitor $C_{P_{pv}}$ in “$P_{pv\_storage}$” must be updated to latest $P_{pv\_max}G_vG_i$. Assume the maximum power change in the adjacent two cycles are $\Delta P_{max}$, then the ratio between the amplitude of the charge (discharge) current and capacitor $C_{P_{pv}}$ in this cell must satisfy the relationship below:

$$\frac{|i|}{C_{P_{pv}}} \geq \frac{\Delta P_{max} \times G_v \times G_i}{\alpha \times 1/2 \times T_{CLK}}$$

(5.9)

Where $T_{CLK}$ refers to the clock period; $\alpha$ is a fraction of the half clock period for changing (discharging) $C_{P_{pv}}$. $\alpha$ is less than one and it is in the range of 0.6~0.8. This design constraint ensures that the voltage of $C_{P_{pv}}$ will reach the desired value after each cycle.

For practical design reasons, resistors $R_{s1}$–$R_{s8}$ may also be integrated into the MPPT controller chip. In this case, the end user only needs to set $R_1$–$R_4$, $C_{P_{pv}}$ and $C_{V_{pv}}$ according to the design procedure.

### 5.4 Simulation and Experiment Verification

System simulation with Saber® has been conducted to verify the operation of the new analog MPPT controller. The designed controller sent $V_{pv\_ref}$ to a buck converter in the simulation. The storage cell in Fig. 5.6(c) is used. Table 5.5 gives the circuit parameters for
simulation. Fig. 5.13(a) gives the characteristic curves of modeled PV panel under different circumstances of sun irradiation: 500W/m², 840W/m² and 1kW/m². It can be seen from Fig. 5.13(b) that the MPPT controller can find the MPP and it can make correct response to irradiance level change. Table 5.6 gives a summary of the simulation results.

Table 5.5 Circuit Parameters for Simulation

<table>
<thead>
<tr>
<th>V_{pv} range (V)</th>
<th>Buck V_{out} (V)</th>
<th>F_{sw} (kHz)</th>
<th>CLK freq (Hz)</th>
<th>MPPT Voltage Step</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–43</td>
<td>12</td>
<td>40</td>
<td>1K</td>
<td>0.5% V_{OC}</td>
</tr>
</tbody>
</table>

(a) P_V and I_V Curves for PV Panel Model in Saber
Fig. 5.13 Simulation Results from Saber®

Table 5.6 A Summary of the Simulation Results

<table>
<thead>
<tr>
<th>Irradiance Level (W/m²)</th>
<th>$P_{PV_THEO}$ (W)</th>
<th>MPP Point (A,V)</th>
<th>$P_{PV_track}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>118.39</td>
<td>(3.352, 35.166)</td>
<td>117.86</td>
</tr>
<tr>
<td>840</td>
<td>202.35</td>
<td>(5.616, 36.216)</td>
<td>202.13</td>
</tr>
<tr>
<td>1000</td>
<td>242.16</td>
<td>(6.637, 36.527)</td>
<td>241.93</td>
</tr>
</tbody>
</table>
To examine the proposed analog MPPT controller’s performance for practical applications, it is implemented with discrete components in the experiment, as shown in Fig. 5.14. Table 5.7 gives the circuit parameters and components used for the experiment.

Table 5.7 Circuit Parameters and Components for MPPT Experiment

<table>
<thead>
<tr>
<th>V_{pv} range (V)</th>
<th>DC/DC V_{out} (V)</th>
<th>Fsw (kHz)</th>
<th>CLK freq (Hz)</th>
<th>MPPT Step</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–55.6</td>
<td>80</td>
<td>40–160</td>
<td>1K</td>
<td>0.5% V_{OC}</td>
</tr>
<tr>
<td><strong>Multiplier</strong></td>
<td><strong>Comparator</strong></td>
<td><strong>Sample &amp; Hold</strong></td>
<td><strong>PNP: P1–P4</strong></td>
<td><strong>NPN: N1–N5</strong></td>
</tr>
<tr>
<td>MPY634</td>
<td>LM311</td>
<td>LF398N</td>
<td>MMBT3906</td>
<td>MMBT3904</td>
</tr>
</tbody>
</table>

The DC/DC stage is a resonant converter which may use the V_{pv,ref} from an MPPT controller as a reference signal. An electronic load running in “constant voltage” mode is
connected to the output of DC/DC converter such that converter’s output voltage will remain constant. Three PV panels MSX77S from SOLAREX are connected in series and Fig. 5.15 gives their P-V and I-V curve.

The storage cells in the experiment are also based on structure in Fig. 5.6(c). Fig. 5.16(a) shows the averaged PV panel voltage stays around 36.01V and output power is around 116W in the experiment. The surface temperature of these panels is around 60°C during the experiment. Further, Fig. 5.16(b) gives the track results for a single day. From these test results, the averaged tracking error between tracked power and real power is smaller than 0.5%. To verify the MPPT controller’s start-up operation, Fig. 5.17 shows its operation waveform during startup with (a) $V_{\text{initial}} < V_{\text{mpp}}$ and (b) $V_{\text{initial}} > V_{\text{mpp}}$. An intentional delay time $t_1$ is added before MPPT starts in order to allow for clear observation of the startup operation. In both cases, the panel voltage is initialized to a constant value during $t_1$ and finally MPP is reached.
Fig. 5.15 PV Panel Characteristic Curves During the Experiment Test

(a) The P-V Curve of the PV Panels Under Test

(b) The I-V Curve of the PV Panels Under Test
(a) Experimental Waveforms with Analog MPPT Controller

(b) Tracking Performance Test Results for Analog MPPT

Fig. 5.16 The Experimental Verification of the Analog MPPT Controller Performance
Fig. 5.17 Start-up Operation Waveforms of the MPPT Controller

(a) MPPT Controller Starts with $V_{\text{initial}} < V_{\text{mpp}}$

(b) MPPT Controller Starts with $V_{\text{initial}} > V_{\text{mpp}}$
5.5 Summary

A new analog MPPT controller is proposed in this paper. Its operation is based on a truth table derived from the P&O method. Due to its simple structure, it is attractive for the industry to integrate with any kind of DC/DC controller to form a single chip “MPPT Regulator”. Theoretically, there is no speed limit for this MPPT controller but the DC/DC converter’s bandwidth puts limitation on the perturbation frequency. The capacitor based storage cell is proposed to store required information for the P&O method and several different cell structures are discussed. The operation of the proposed MPPT controller is explained in detail and a design procedure is given for choosing proper controller parameters. A system level simulation proved the operation of the new analog MPPT controller. The controller is also implemented with discrete components and its tracking performance has been verified by the experiment results.
Chapter 6. Conclusion and Future Work

6.1 Conclusion of Present Work

This research work focuses on development of high efficiency distributed MPPT stage with low cost single chip maximum power point tracking (MPPT) solution for distributed solar energy conversion systems. The motivation for this research work is introduced in the first Chapter and detailed at the beginning of Chapters 3 ~ 5.

In Chapter II, the roadmap for development of grid-tied solar inverters is discussed and various solar inverter topologies are reviewed and evaluated in terms of their efficiency, component count & size and other factors. The objective of this part of work is to understand the requirements, challenges and new trends for future solar energy conversion.

Chapters 3 and 4 proposed two kinds of high efficiency resonant DC/DC converter topologies for distributed MPPT stage application and they have several common features:

(1) Both can be designed to cope with a wide range of input voltage and they can change the operation modes based on sensor information to optimize conversion efficiency.

(2) Both topologies can achieve ZVS for the MOSFETs in the primary side and ZCS for
the diodes in the secondary side.

The operation principle of the proposed converters has been described in detail. The corresponding theoretical circuit analysis is given to disclose the features of the proposed converter. The converter performance has been verified by both simulation and experimental results.

Chapter 5 proposed a cost-effective analog MPPT controller to form a single chip controller solution for the distributed MPPT stage. The operation principle of the new controller is explained and the cost evaluation is presented. The tracking performance of the proposed controller has been validated by both simulation and experimental results from a PV converter with 200W PV panels under different sun irradiation level and temperature.

6.2 Future Work

To make the proposed analog MPPT controller suitable for integration, its circuit parameters should be further tuned and designed. At the meanwhile, there is interaction between the MPPT loop and DC/DC converter’s regulation loop in the MPPT stage. In practice, large oscillation on $V_{PV}$ (or $I_{PV}$) may be observed under certain circumstances. Therefore, it is necessary to investigate the relationship between these two loops and develop design criteria to address this relationship. Thus, the future work includes the following:

1. Integration of the MPPT controller with a DC/DC controller for a single chip solution.
(2) Investigation and analysis of the interaction between the DC/DC converter’s bandwidth and the MPPT tracking loop’s speed in the MPPT stage.
References


[8] Solar Edge system overview, available:


[9] Satcon Solstice 100KW System Solution Datasheet, available:


IEEE Std. 1547, 2003


2005.


grid-connected inverters for photovoltaic modules”, IEEE Transactions on Industry


[14] Limits for Harmonic Current Emission (Equipment Input Current<16A per Phase),

EN61000-3-2, 1995


Systems. International Energy Agency Photovoltaic Power Systems, IEA PVPS T5-01:


[34] Available: http://www.sunsil.dk


Industrial Electronics, June 9-11, 2008


[60] S.B. Kjaer, “Design and control of an inverter for photovoltaic applications”, Ph.D
dissertation, Institution of Energy Technology, Aalborg University, Denmark, 2004/2005


http://w5jgv.com/hv-ps1/pdf/topologies_for_switched_mode_power_supplies.pdf


http://www.onsemi.com/pub_link/Collateral/SMPSRM-D.PDF


[76] Solar Edge System Overview, available:


[100] SunTech STP-280-24/VD PV panel datasheet, available: www.suntech-power.com


[103] Online Resources, available: http://www.pv-tech.org


