ABSTRACT

LIN, POCHIH. A High Fidelity Wide Bandwidth (HWFB) Buck Converter for Wireless Communication Applications. (Under the direction of Dr. Alex Q. Huang).

This dissertation proposes a ripple based variable frequency control scheme for a high bandwidth power converter. The converter is for wireless communication applications. The goal is to provide a buck converter design solution for the system application, to improve efficiency and linearity simultaneously. To enhance linearity, the theoretical derivation of switching ripple cancellation in frequency domain is given and modeled. The simulation results match the Cadence simulation and the experimental results. From the envelope tracking point of view, to support FCC power emission mask, a high-speed synchronized buck with switching ripple cancellation technique for the envelope tracking transmitter architecture is designed, measured and thoroughly derived. Detailed large and small signals analyses of the modulator design are carried out to study the effects of the parameters and to prove the system stability and high control bandwidth. The derivation results are modeled to the control theory and measurement results; they do match. A preliminary analysis of Device Segmentation strategy is also proposed for HFWB buck converter to enhance the efficiency over a wide load range. A monolithic HFWB buck converter is fabricated using the AMI 05 CMOS process. The test results show that output ripple has a significant decrease from 1.2V to 200 mV; the spectrum is spread out over a wide frequency band.
A High Fidelity Wide Bandwidth (HWFB) Buck Converter for Wireless Communication Application

by
Pochih Lin

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Electrical Engineering

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APPROVED BY:

__________________________
Dr. Alex Q. Huang
Committee Chair

__________________________
Dr. Rhett W. Davis

__________________________
Dr. Brian A. Floyd

__________________________
Dr. John Mackenzie
DEDICATION

To my parents

Pichu Liao and EnSheng Lin
BIOGRAPHY

The author, Pochih Lin, was born in Taipei, Taiwan. He has a Bachelor of Science degree from the National Central University in Jhong Li, Taiwan and a Master of Science from The Ohio State University (2005) in Electrical engineering. He started to pursue a Ph.D. at the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh in January 2006. His research interests include Analog, Mixed Signal, Power Management, and RF IC Design.
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# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TABLE OF CONTENTS</strong></td>
<td>vi</td>
</tr>
<tr>
<td><strong>LIST OF TABLES</strong></td>
<td>viii</td>
</tr>
<tr>
<td><strong>LIST OF FIGURES</strong></td>
<td>ix</td>
</tr>
<tr>
<td>Chapter 1 Introduction</td>
<td>1</td>
</tr>
<tr>
<td>1.1 Background: Trends of Handheld Devices</td>
<td>1</td>
</tr>
<tr>
<td>1.2 Research Motivation</td>
<td>4</td>
</tr>
<tr>
<td>1.3 Overview of Thesis</td>
<td>6</td>
</tr>
<tr>
<td>Chapter 2 High Efficiency Linear Transmitter</td>
<td>8</td>
</tr>
<tr>
<td>2.1 Literature Review on Linearity and Efficiency Enhancement Schemes</td>
<td>8</td>
</tr>
<tr>
<td>2.1.1 Envelope Tracking</td>
<td>8</td>
</tr>
<tr>
<td>2.1.2 Cartesian Feedback</td>
<td>10</td>
</tr>
<tr>
<td>2.1.3 Polar Modulation</td>
<td>12</td>
</tr>
<tr>
<td>2.1.4 Envelope Elimination Restoration</td>
<td>14</td>
</tr>
<tr>
<td>2.1.5 Dynamic Voltage Scaling (DVS)</td>
<td>16</td>
</tr>
<tr>
<td>2.2 Challenge of Implementing High Efficiency Linear Transmitter</td>
<td>17</td>
</tr>
<tr>
<td>2.2.1 Issues of Amplitude Phase Separation Modulation Scheme</td>
<td>18</td>
</tr>
<tr>
<td>2.3 Summary</td>
<td>21</td>
</tr>
<tr>
<td>Chapter 3 Ripple Cancellation Technique</td>
<td>22</td>
</tr>
<tr>
<td>3.1 Time Domain Ripple Cancellation Derivation</td>
<td>23</td>
</tr>
<tr>
<td>3.2 Frequency Domain Ripple Cancellation Derivation</td>
<td>25</td>
</tr>
<tr>
<td>3.3 Summary</td>
<td>31</td>
</tr>
<tr>
<td>Chapter 4 High Fidelity Wide Bandwidth (HFWB) Buck Converter</td>
<td>32</td>
</tr>
<tr>
<td>4.1 Review of Control Topologies</td>
<td>32</td>
</tr>
<tr>
<td>4.1.1 Current Mode Control and Voltage Mode Control</td>
<td>32</td>
</tr>
<tr>
<td>4.1.2 Hysteretic Control</td>
<td>34</td>
</tr>
<tr>
<td>4.1.3 Hybrid Switching Modulator</td>
<td>37</td>
</tr>
<tr>
<td>4.2 Topology of High Fidelity Wide Bandwidth (HFWB) Buck Converter</td>
<td>39</td>
</tr>
<tr>
<td>4.3 Switching Frequency Analysis of HFWB Buck Converter</td>
<td>42</td>
</tr>
<tr>
<td>4.4 Steady State Error Analysis of HFWB Buck Converter</td>
<td>46</td>
</tr>
<tr>
<td>4.5 Small Signal Analysis of HFWB Buck Converter</td>
<td>47</td>
</tr>
<tr>
<td>4.5.1 Transfer function of the power stage</td>
<td>48</td>
</tr>
<tr>
<td>4.5.2 Transfer function of the DDA loop</td>
<td>52</td>
</tr>
<tr>
<td>4.5.3 Transfer function of the duty ripple loop</td>
<td>55</td>
</tr>
<tr>
<td>4.5.4 Transfer function of the modulator</td>
<td>57</td>
</tr>
<tr>
<td>4.5.5 Small Signal Model of the HFWB Buck Converter</td>
<td>59</td>
</tr>
<tr>
<td>4.6 Summary</td>
<td>64</td>
</tr>
<tr>
<td>Chapter 5 Monolithic Implementation of HFWB Buck Converter with Ripple Cancellation</td>
<td>65</td>
</tr>
<tr>
<td>5.1 Differential Difference Amplifier reviews and design</td>
<td>65</td>
</tr>
<tr>
<td>5.2 Constant Input gm Stage</td>
<td>68</td>
</tr>
<tr>
<td>5.3 A fixed on Time Generator Circuit</td>
<td>72</td>
</tr>
<tr>
<td>5.4 Dead Time Generator Circuit</td>
<td>73</td>
</tr>
</tbody>
</table>
5.5 Rail-to-rail Comparator Circuit ................................................................. 77
5.6 Level Shifter Circuit ............................................................................ 80
5.7 Power Stage implementation of HFWB ................................................. 82
5.8 Simulation, Layout, Packaging, Evaluation Board Design and Measurement Results of HFWB Buck Converter .......................................................... 89
  5.8.1 Simulation .......................................................................................... 89
  5.8.2 Layout ............................................................................................... 92
  5.8.3 Packaging ......................................................................................... 93
  5.8.4 Evaluation Board Design and Setup .................................................. 95
  5.8.5 Measurement Result ........................................................................ 99
Chapter 6 Power Efficiency Improvement for Light Load for HFWB Buck Converter for Wireless Communication Application ........................................................ 109
  6.1 Loss Breakdown in HFWB Buck Converter ........................................... 109
  6.2 Device Segmentation Technique in wireless communication application ........ 112
    6.2.1 Active Filter ................................................................................ 113
    6.2.2 Lossless Inductor Current Sensing ................................................ 114
    6.2.3 Simulation Result of Device Segmentation .................................... 117
  6.3 Summary .............................................................................................. 121
Chapter 7 Scope of Future Work .................................................................. 123
  7.1 Complete System Level Demonstration with RF PA in Discrete version ................ 123
  7.2 Implement a Two Stage Envelope Tracking Structure for CDMA Wireless Communication Applications ........................................................ 123
References ................................................................................................. 125
LIST OF TABLES

Table 1-1 Summary of 2G and 3G System Characteristics [2] ........................................... 3
Table 2-1 System Transmitter Architecture Comparison ...................................................... 21
Table 4-1 Comparison between Different Control Methods .................................................. 42
Table 5-1 HFWB Buck Converter Post Layout Simulation Result ........................................ 92
Table 5-2 HFWB Buck Converter Pin Description .............................................................. 94
Table 6-1 HFWB Buck System Loss Breakdown over Load Condition ......................... 113
LIST OF FIGURES

Figure 1-1 Generic Handheld Portable System [1] .................................................................................. 2
Figure 1-2 Output Power Probability Distribution Function of CDMA Cellular Phone [5] ........ 4
Figure 1-3 Power Added Efficiency (PAE) Variations in a Two-Mode W-CDMA RFPA [5] .... 5
Figure 2-1 Conceptual Block Diagram of Envelope Tracking ...................................................... 9
Figure 2-2 Cartesian Feedback Transmitter Conceptual Block Diagram[14] ................................. 10
Figure 2-3 Simplified Control Scheme of Cartesian Feedback[2] .................................................. 11
Figure 2-4 Conceptual Block Diagram of Polar Modulation Transmitter[2] ............................... 12
Figure 2-5 Conceptual Block Diagram of EER[7] .......................................................................... 14
Figure 2-6 Power Added Efficiency of Dual-Mode W-CDMA RFPA (Black Curve) Compared to a Single-Mode RFPA Using Dynamic Voltage Supply (Blue Curve)[5] .......... 17
Figure 2-7 Spectra Re-growth Demonstration[19] ........................................................................ 18
Figure 2-8 EDGE Signal Bandwidth[9] .......................................................................................... 19
Figure 2-9 Simulated Output Spectrum for a 1-MHz envelope filter, with and without Delay Compensation[16] ........................................................................................................ 20
Figure 3-1 Ripple Cancellation Circuit [20] .................................................................................... 24
Figure 3-2 Key Waveform of Ripple Cancellation Circuit [20] ..................................................... 24
Figure 3-3 Eq3.4 in Frequency Domain ......................................................................................... 25
Figure 3-4 Eq 3.4 in Time Domain ................................................................................................. 25
Figure 3-5 Eq 3.5 in Frequency Domain ........................................................................................ 26
Figure 3-6 Eq 3.5 in Time Domain ................................................................................................. 26
Figure 3-7 Simulation Result of the Output of Auxiliary Branch and Vout ..................................... 27
Figure 3-8 Second Harmonic of Eq. 6.4 ....................................................................................... 28
Figure 3-9 Third Harmonic of Eq 6.4 ............................................................................................ 28
Figure 3-10 Simulation Result of the Output of Auxiliary Branch and Vout .................................. 28
Figure 3-11 (a)Comparison with and without Ripple Cancellation in Time Domain (b) Zoom In ................................................................................................................................. 30
Figure 3-12 Output Impedance Plot of Z1 and Z2 ........................................................................ 31
Figure 4-1 Voltage Mode Control [24] .......................................................................................... 33
Figure 4-2 Current Mode Control[24] ........................................................................................... 34
Figure 4-3 Hysteretic Control[34] ................................................................................................ 35
Figure 4-4 Output Ripple of Buck Converter[33] ........................................................................ 36
Figure 4-5 Improved Hysteretic Control[36] ............................................................................... 37
Figure 4-6 Hybrid Switching Amplifier with the Third Order Ripple Filter and the Current Feedback[39] ...................................................................................................................... 38
Figure 4-7 Conceptual Block Diagram of HFWB Buck Converter ................................................ 41
Figure 4-8 output voltage waveform through different load conditions (a) 4ohm (b)11ohm (c)22ohm (d)47ohm (e)100ohm (f) 200ohm ................................................................. 45
Figure 4-9 Waveform of the Control Ripple Voltage and Vn for Offset Analysis .......................... 46
Figure 4-10 CCM PWM Switch Model[24] ................................................................................ 49
Figure 4-11 Ripple Cancellation Technique[20] .......................................................................... 49
Figure 4-12 Transfer Function from Duty Cycle to Output .......................................................... 51
Figure 4-13 Transfer Function from Duty Cycle to Output with and without Cancellation Branch

Figure 4-14 Closed Loop of DDA Circuit

Figure 4-15 Transfer Function from Switch Node to RC Control Ripple Voltage Output

Figure 4-16 Transfer Function from Vout to DDA Output

Figure 4-17 Small Signal Blocks of HFWB Buck Converter

Figure 4-19 Open Loop Transfer Function of HFWB Buck Converter

Figure 4-20 Open Loop Transfer Function without Cancellation Branch

Figure 4-21 DC Gain and Phase Margin with and without Ripple Cancellation

Figure 5-1 Model of DDA

Figure 5-2 Basic Structure of the DDA

Figure 5-3 The Generalized DDA Topology

Figure 5-4 Class AB Amplifier - Second Stage

Figure 5-5 Rail-to-Rail with gm-Control by Three Times Current Schematic

Figure 5-6 Transistor Level of DDA

Figure 5-7 Fixed on Time Generator

Figure 5-8 Simulation Result of Control Ripple Voltage and Vn

Figure 5-9 Effect of the Dead Time Control

Figure 5-10 Conceptual Block Diagram of Dead Time Generator Circuit

Figure 5-11 Multi-level of the Delay Times by Dead Time Generator (a) Top Switch turns on (b) Top Switch turns off

Figure 5-12 Rail-to-Rail Comparator

Figure 5-13 Simulation Result of the NMOS Level Shifter and PMOS Level Shifter

Figure 5-14 Layout Illustration

Figure 5-15 Power Stage de-biasing Effect Modeling

Figure 5-16 Equivalent Resistance Relationship for Adjacent Finger for de-biasing Effect Modeling

Figure 5-17 Optimized Power Stage Width for HFWB Buck Converter

Figure 5-18 Optimized Ratio of NMOS/PMOS Width for Power Stage for HFWB Buck Converter

Figure 5-19 Optimized No. of Fingers for Power Stage for HFWB Buck Converter

Figure 5-20 HFWB Buck Converter System Power Breakdown

Figure 5-21 HFWB Buck Converter Power Stage Loss Breakdown

Figure 5-22 Vref (IS95 CDMA Baseband Signal) V.S. Vout

Figure 5-23 Frequency Domain Simulation Plot (full range)

Figure 5-24 Frequency Domain Simulation Plot (near band)

Figure 5-25 Layout of HFWB Buck Converter

Figure 5-26 Bond Diagram of HFWB Buck Converter

Figure 5-27 Evaluation Board of HFWB Buck Converter

Figure 5-28 Functional Blocks HFWB Buck Converter Chip

Figure 5-29 Test Schematic of HFWB Buck Converter

Figure 5-30 Test PCB Board for HFWB Buck Converter

Figure 5-31 Measurement Result of DDA
Figure 5-32 Measurement Result of DDA ................................................................. 101
Figure 5-33 Measured Waveform of the Vref, Vout, Inductor Current Ripple and Switching Nodes Waveform with 200 KHz ................................................................. 101
Figure 5-34 Measurement of the Vout, Vref, Inductor Current Ripple and Switching Node Waveform with 100KHz Sinusoidal Reference with Different Amp Vpp (a) Amp = 1V Vpp (b) Amp = 2V Vpp (c) Amp = 3V Vpp ......................................................... 103
Figure 5-35 Measurement of the Vout, Vref, Inductor Current Ripple and Switching Node Waveform with Different Sinusoidal Reference Vref with Amp =3V Vpp (a) Vref = 1KHz (b) Vref = 10 KHz (c) Vref = 40KHz Amp = 4V (d) Vref = 100KHz ......................................................... 104
Figure 5-36 Measurement of the Vout, Inductor Current Ripple with Triangle Reference Vref=100KHz and Amp = 2V ........................................................................ 105
Figure 5-37 Vref With and Without Switching Ripple Cancellation Technique for 100Hz Sinusoidal Input Signal ................................................................. 106
Figure 5-38 Without Switching Ripple Cancellation Technique Output Spectrum for 100 KHz Amp 3V Vpp Sinusoidal Input Signal ......................................................... 107
Figure 5-39 Frequency Spectrum of a 10MHz Fully Differential High Frequency Class D Modulator [7] ........................................................................ 108
Figure 5-40 Spectrum Plot of a 10MHz Current Mode 4 Switch Buck Boost Converter (4SBBC) for Polar Modulation [51] ......................................................... 108
Figure 6-1 HFWB Buck Converter with Device Segmentation Technique ............. 115
Figure 6-2 Connection Diagram of AD830[54] ......................................................... 117
Figure 6-3 Step Down Key Waveform-1 .................................................................. 118
Figure 6-4 Step Down Key Waveform -2 .................................................................. 119
Figure 6-5 Step Down Key Waveform -3 .................................................................. 120
Figure 6-6 Step Down Key Waveform -4 .................................................................. 120
Figure 6-7 HFWB Buck Converter Load Efficiency Curve ...................................... 121
Chapter 1 Introduction

1.1 Background: Trends of Handheld Devices

Technological advances in the cellular phone industry have caused user interests and industry trends to shift rapidly. Because of this, data-centric handsets like smart phones are popular in the market today. This is contrary to the voice-centric phones available during the time of GSM (Global System for Mobile Communication) and CDMAOne (Code Division Multiple Access One) (IS-95) 2G wireless communication systems in the 1990s.

The following major trends are visible in handheld devices:

- The usability and the complexity aspect: addressing the need of power efficiency of the handheld device.
- The signal characteristic: addressing the major issues that would be encountered in the radio frequency (RF) transmitter for the next generation handheld communication device.

Nowadays multiple devices are merged into a single handheld unit[1]. A handheld unit can have in-built RF transceiver, FM radio, WIFI, video, games, music, TV encoder, GPS, SD Memory port, LCD display, LED light, and cameras. The functionalities are continuously increasing, but they have a downside: more power consumption. This in turn requires better power management. Figure 1-1[1] shows a generic power management scheme for a portable device. Almost every major circuit block in the device needs a specified power supply. Moreover, each of these circuit blocks has its own optimized semiconductor process and
operating voltage requirements in order to improve the efficiency of the handheld device. The power amplifier (PA), which is the most energy-consuming component, should come with a solution to optimize its efficiency to extend the connection time. However, the power resource is still solely the battery and therefore cannot satisfy customer requirements. Consequently, in order to keep up the battery life of a 2G wireless system, a unit with a much higher power-efficiency is required for optimally using the available power resource.

The other trend as mentioned is the signal characteristic because of the demand for speed. Table 1-1[2] is the roadmap of the developments in wireless communication. It also serves as a comparison table between different communication systems indicating the increase in peak to average ratio (PAR).
In order to send a large amount of data within a limited bandwidth, the complex and non-constant envelope modulation scheme has emerged as a viable solution. This is primarily because it helps increase the data rate. For instance, Table 1-1[2] shows that, in order to pack as many bits as possible in a given bandwidth, GSM system started changing by adopting GPRS. In 2001, Gaussian Minimum Shift Keying (GMSK) was adopted; in late 2003, a non-constant envelope as against a constant envelope was adopted, (example: Enhanced Data GSM Environment-EDGE). EDGE employs 8PSK modulation scheme to increase bandwidth efficiency.

<table>
<thead>
<tr>
<th>Year</th>
<th>Communication System</th>
<th>Generation</th>
<th>Modulation Scheme</th>
<th>Envelope Characteristic</th>
<th>Multiple Access Type</th>
<th>PAR</th>
<th>PA Maximum Output Power (dBm)</th>
<th>Bandwidth (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1991</td>
<td>GSM</td>
<td>2G</td>
<td>GMSK</td>
<td>Constant</td>
<td>TDMA</td>
<td>0</td>
<td>33</td>
<td>0.2</td>
</tr>
<tr>
<td>2001</td>
<td>GPRS</td>
<td>2.5G</td>
<td>GMSK</td>
<td>Constant</td>
<td>TDMA</td>
<td>0</td>
<td>33</td>
<td>0.2</td>
</tr>
<tr>
<td>2003</td>
<td>EDGE</td>
<td>2.75G</td>
<td>8PSK</td>
<td>Non-constant</td>
<td>TDMA</td>
<td>3.2</td>
<td>33</td>
<td>0.2</td>
</tr>
<tr>
<td>1995</td>
<td>CDMA1(IS-95)</td>
<td>2G</td>
<td>QPSK/OQPSK</td>
<td>Non-constant</td>
<td>CDMA</td>
<td>3.5-12</td>
<td>27-30</td>
<td>1.25</td>
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<tr>
<td>2000</td>
<td>CDMA 2000</td>
<td>3G</td>
<td>QPSK/HPSK</td>
<td>Non-constant</td>
<td>CDMA</td>
<td>4-9</td>
<td>27-30</td>
<td>1.25</td>
</tr>
<tr>
<td>2001</td>
<td>WCDMA(UMTS)</td>
<td>3G</td>
<td>QPSK/HPSK</td>
<td>Non-constant</td>
<td>CDMA</td>
<td>3.5-7</td>
<td>35</td>
<td>5</td>
</tr>
<tr>
<td>1999/2003</td>
<td>802.11 a/g</td>
<td>N/A</td>
<td>OFDM</td>
<td>Non-constant</td>
<td>CSMA</td>
<td>8-10</td>
<td>30</td>
<td>20</td>
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<tr>
<td>2005</td>
<td>WiMax (802.16e)</td>
<td>N/A</td>
<td>OFDM</td>
<td>Non-constant</td>
<td>OFDMA</td>
<td>8-10</td>
<td>27-29</td>
<td>20</td>
</tr>
</tbody>
</table>

As Table 1-1 shows, the modulation schemes of today’s wireless systems such as EDGE, CDMA, WCDMA (Wide-band Code Division Multiple Access) and OFDM (Orthogonal Frequency Division Multiplexing) exploit the non-constant envelope modulation scheme. These have high PAR ratios when compared to the constant envelope modulation scheme,
and hold the information in both amplitude and phase. Needless to say, the next generation systems are truly expected to possess high complexity signal processing techniques [3, 4]

1.2 Research Motivation

As the previous section mentioned, the linear RF power amplifier becomes necessary because of the high PAR signal characteristic. Thus, an inevitable trade-off between linearity and efficiency occurs. In addition, because of the high PAR, the PA needs to be designed for peak power. However, it operates predominantly at average power only. Figure 1-2 shows the Output power vs. Power distribution function of a typical CDMA cellular phone (Output power refers to the output port of the PA). The average value of the output power level is 30 dBm below its maximum instantaneous power[3, 5]. Therefore, the back-off operation results in poor power efficiency for the PA and the transmitter.

Figure 1-2 Output Power Probability Distribution Function of CDMA Cellular Phone [5]
As shown in Figure 1-3, at peak power, the PAE (Power Added Efficiency) is above 30%. Nonetheless, when it enters light load or extreme light load condition, the PAE collapses. In such conditions, PAE drops from 30% to 2%. Therefore, the industry solution is to adopt different bias modes to improve the efficiency by adjusting the DC power consumption.[5]

The major portion of the energy consumption occurs in the power amplifier of the RF transmitter. In brief, the device functionalities constantly increase causing energy consumption, and because the available power resource is only the battery, the situation deteriorates further.

As mentioned earlier, for the handheld device, each circuit block has its own supply voltage and design to optimize the efficiency, so does the RFPA block, which is the most power-
consuming block in a handheld device. The target of this research is to provide a solution from the buck converter design, in order to improve both efficiency and linearity.

1.3 Overview of Thesis

This dissertation consists of six chapters organized as follows:

- **Chapter 1**: It gives an introduction of the background and the motivation of the research.

- **Chapter 2**: It reviews various linearity and efficiency improvement techniques, including the tradeoff of each architecture and a cross comparison between various system architectures. It also mentions the challenges in implementing an amplitude phase separation modulation scheme, which needs to be overcome for next generation wireless communication applications.

- **Chapter 3**: It introduces the inductor switching ripple cancellation method and presents a novel derivation of a ripple cancellation concept in frequency domain for the buck converter.

- **Chapter 4**: It first reviews various control schemes of the buck converter. Secondly, it introduces the proposed novel buck converter. Thirdly, it includes a thorough analysis and derivation of small and big signals of HFWB buck converter with switching ripple cancellation. The tradeoff with and without an auxiliary branch is modeled and compared in MATLAB.

- **Chapter 5**: It reports the transistor level design detail of the functional blocks, simulation and measurement results. Secondly, the energy dissipation of HFWB buck
converter is analyzed and discussed, which is mainly at MOSFET. MOSFET-related power reduction technique for wireless communication application is introduced in this chapter. The transistor level simulation result indicates the efficiency has 7% improvement at light load

- **Chapter 6:** It summarizes the HFWB buck converter control scheme and the future of work on this new control method
Chapter 2 High Efficiency Linear Transmitter

2.1 Literature Review on Linearity and Efficiency Enhancement Schemes

Efficiency and the linearity are the two major specifications for the radio frequency (RF) transmitter. These specifications should be enhanced from the perspectives of the circuit as well as the system. A lot of research work has been conducted in the past to enhance the efficiency and linearity at the system level. This chapter reviews all the techniques used in the research. It also presents a comparison between the techniques used in the research and elicits the traits and drawbacks of each of these techniques.

2.1.1 Envelope Tracking

Envelope Tracking[6, 7] is a technique very similar to EER[8] and Polar modulation[9]. The architecture of the envelope tracking technique is shown in Figure 2-1. The RF input signal is sent directly to the PA and the envelope signal is tracked to provide just enough voltage to keep the transistor from clipping.
Following are the advantages of Envelope Tracking over Envelope Elimination Restoration[7]:

- As the RF input signal bandwidth is lesser than that of the phase signal, the bandwidth requirement of RF PA is lesser as compared to EER.
- It alleviates the issue of time alignment requirement when compared to precise time alignment required in the case of EER and polar modulation.
- Bandwidth requirement of the envelope path is lesser than that of EER since amplitude information is present in the RF input signal; however, the bandwidth requirement is greater than that of I-Q.

This arrangement tries to alleviate the time alignment pressure yet preserves the efficiency of polar modulation PA. The envelope tracking PA is a linear amplifier (e.g. class A, or class
AB) rather than an efficient switching mode amplifier because of the non-constant envelope RF signal. This renders the envelope tracking technique to be less efficient as the PA is operating at its peak power. To save power, the varying supply voltage is typically achieved through a class D modulator, which has efficiency in the region of 70-90% [10-12]. The average efficiency can still be 1.4 times [11, 13] or even 5 times[10] depending on the statistical profile of the signal power.

### 2.1.2 Cartesian Feedback

Cartesian feedback[2, 14] is a technique which takes negative feedback in I and Q form as opposed to the polar coordinates. It has the name Cartesian for this reason. Figure 2-2 and Figure 2-3 display the conceptual and modeled control block diagrams of the Cartesian feedback transmitter.

![Figure 2-2 Cartesian Feedback Transmitter Conceptual Block Diagram[14]](image)

> Figure 2-2 Cartesian Feedback Transmitter Conceptual Block Diagram[14]
Figure 2-3 Simplified Control Scheme of Cartesian Feedback[2]

Figure 2-2 shows that I and Q are orthogonal and two completely independent paths. In Figure 2-3, Sin(s), Sout(s), DA(s) and DF(s) represent baseband input, output, distortion from DA and distortion from feedback path respectively. Eq. 2.1 shows the input to output transfer function. It can be seen from Eq. 2.1 that DA(s) is greatly reduced by the loop gain. However, the Cartesian feedback transmitter requires a predominantly linear feedback because the DF(s) is not highly reduced by the loop gain. This limits the linearity improvement and the stability is constrained by the open loop bandwidth and loop delays. [14]

\[
S_{out}(s) \approx \frac{S_{in}(s)}{\beta} + \frac{D_A(s)}{\alpha \beta} - \frac{D_F(s)}{\beta}
\]

(2.1)

In the publication, the feasible reduction of IMD3 are in the order of 10-30 dB with up to a few MHz bandwidth range [2, 15][14]. However, the suppression of higher order IMDs is not
obvious because of the bandwidth limitations. In addition, the achievable bandwidth is higher than that of the polar modulation scheme. This is because there is no spectrum re-growth of I and Q signals. However, unlike the polar modulation, the Cartesian PA is not efficient in power owing to the non-constant I and Q signal.

2.1.3 Polar Modulation

Polar modulation is popular as a scheme for amplitude phase separation. Its concept is similar to EER except that the magnitude and phase signals are generated directly at baseband and not from RF. This eliminates the necessity of an envelope detector and a limiter, as shown in Figure 2-4:

![Figure 2-4 Conceptual Block Diagram of Polar Modulation Transmitter][2]

[2]Polar modulation is preferable to PA (a switching device) because of its superior noise performance. It emits lower noise than linear PAs. This reduction of noise allows the system to eliminate the SAW filter needed for linear PAs, which results in cost savings.
From the PA point of view, polar modulation is more suitable because of its efficiency. The fundamental principle[8] of the polar modulated PA is to decompose the RF signal into amplitude and phase path. Two very different amplifiers amplify the amplitude and phase path. The phase path is amplified by a switch mode FET without loss of information and a linear regulator or DC-DC converter tracks the amplitude path. The amplitude path later modulates the phase path to recover the original signal. Since efficient non-linear amplifiers for the phase path can be used, the efficiency of the polar modulated PA can be much higher than that of a conventional linear PA. Moreover, an efficient class D converter achieves the amplitude path. The average efficiency can ideally be very high. Polar modulated PA is regarded more as an efficiency enhancement PA.

Theoretically, the polar modulated PA can achieve linearity and efficiency simultaneously. However, many avoidable factors in the circuit contribute to various sources of non-linearities. Major among them is the non-linear drain to source on resistance of the switching mode amplifier and the AM-PM distortion because of the feed forward from gate-drain capacitor of the device[16]. Another undesirable factor is the delay mismatch of the phase and amplitude path[17]. Furthermore, the strongly nonlinear extraction process of the phase and amplitude generates a much wider bandwidth (of the phase and amplitude path) than the original.

This requires a very wide bandwidth performance of these paths to ensure there is no degradation of linearity[9, 17]. Unfortunately, excessive bandwidth tends to deteriorate the
noise performance. These are the major limitations of the polar loop transmitter. These issues can be resolved partially by using the envelope tracking technique or the polar loop modulation transmitter.

2.1.4 Envelope Elimination Restoration

EER (Envelope elimination and restoration) is a technique proposed by Kahn[7, 9]. The EER separates amplitude and phase to achieve high power efficiency, when using non-constant envelope modulation scheme.

![Conceptual Block Diagram of EER](image)

Figure 2-5 Conceptual Block Diagram of EER[7]

The conceptual block diagram of an EER system is shown in Figure 2-5. [7] The concept of EER is that a limiter first eliminates the envelope signal to generate a constant amplitude phase signal. Concurrently, an envelope detector extracts the magnitude information. The
phase information passes through a non-linear switch-mode RF amplifier, which amplifies it. An envelope amplifier, which can be either a linear or a switch-mode type, amplifies the magnitude separately. The amplified magnitude and phase signals are then modulated to re-establish the desired RF output signal. The amplitude and phase signals can be easily recombined if the amplified magnitude signal directly modulates the power supply of the switch-mode RF PA.

In theory, using a switch-mode envelope amplifier and switch mode RF PA will enable to achieve 100 % overall efficiency.

The linearity of the EER transmitter is not determined by RFPA but by the following two major factors:

- The time misalignment issue. The signal coming from the switch-mode RF PA path versus the signal coming from the envelope-tracking amplifier.
- Bandwidth of the envelope-tracking amplifier, which limits the linearity improvement of EER. In [7, 9, 17, 18], the inter-modulation distortion can be quantized as:

\[
IMD \approx 2\pi B_{RF}^2 \Delta \tau
\]

(2.2)

\(B_{RF}\) is the bandwidth of the RF signal. \(\Delta \tau\) is the delay mismatch.
2.1.5 Dynamic Voltage Scaling (DVS)

The DVS [5] technique scales the power supply level of the RFPA output stage along with the output RF power level using a high-efficiency DC-to-DC converter to improve the overall power efficiency and increase the average talk-time in 3G handsets. The WCDMA/UMTS RFPA is the biggest source of power consumption in a 3G phone because it is continuously enabled during the communication and can drain up to 650mA rms in poor connection conditions, which discharge any Li-ion battery in less two hours.

DVS is a practical solution for the industry. Figure 2-6 shows typical variations of the supply voltage used for WCDMA RFPA to achieve an ACLR of -36dBc. The RFPA is maintained in high-power mode and the supply voltage is varied using FAN5902. There is a significant battery current saving between 16dBm and 24dBm, which is valuable for data communications or for voice communications in suburban areas. When the RFPA output power is 20dBm, the talk or connection time can extend by more than 1 hour (112mA savings).

Factually, DVS topology is inferior to Polar Transmitter scheme. However, because of the time alignment and spectrum re-growth issues, it is a very practical solution because a very slow DC-to-DC converter can be implemented. The DC-to-DC converter saves the power on switching and it does not need to follow a very fast envelope signal, which is one major design challenge for class D modulator. However, it can still save power in some way.
Moreover, the simplicity of this topology and its avoidance of complicated implementations, leads to savings in area and component costs.

![Diagram showing RF Power Level vs. Power Added Efficiency](image)

**Figure 2-6** Power Added Efficiency of Dual-Mode W-CDMA RFPA (Black Curve) Compared to a Single-Mode RFPA Using Dynamic Voltage Supply (Blue Curve)[5]

### 2.2 Challenge of Implementing High Efficiency Linear Transmitter

Section 2.1 reviews many schemes for enhancing system efficiency. Theoretically, high power efficiency is achievable. However, there are many issues, which make the concept impractical. These include spectrum re-growth, stringent time alignment specification, and non-linearity inconsistency over the application bandwidth.
2.2.1 Issues of Amplitude Phase Separation Modulation Scheme

There are many challenges in implementing an amplitude phase separation modulation scheme. When splitting a complex modulated signal into its amplitude and phase components, the bandwidth of each individual component becomes wider as compared to the original signal. This is because of non-linearity as shown in Eq. 2.3, and Eq. 2.4. The components typically require five times larger bandwidth as compared to their baseband modulation as shown in Figure 2-7. This makes the design of high linearity modulator of the order of 10s of MHz of bandwidth very challenging for 3G application.

\[ A(t) = \sqrt{I(t)^2 + Q(t)^2} \]

(2.3)

\[ \phi(t) = \tan^{-1}\left( \frac{Q(t)}{I(t)} \right) \]

(2.4)

Figure 2-7 Spectra Re-growth Demonstration[19]
In [19], it was mentioned that one of the key challenges in the amplitude phase separation architecture is the tradeoff between RF spectrum and noise. For instance, a system-level analysis of a polar modulator reveals that inadequate bandwidths in the PM and AM paths result in spectral re-growth that can violate the transmit mask requirement imposed by the standard.

Figure 2-8 can help in understanding the spectrum degradation by comparing the amplitude and phase components of the signal to the composite signal and the transmit mask. Note that the phase component of the signal exceeds the mask requirement by over 25 dB at 400-kHz offset from the carrier.

![Figure 2-8 EDGE Signal Bandwidth](image-url)

Figure 2-8 EDGE Signal Bandwidth[9]
Secondly, there is always a time alignment issue in the amplitude phase separation scheme, especially when the occupied bandwidth is huge. Consistent delay is very hard to achieve over the occupied bandwidth because of non-linearity. It requires a very accurate time alignment between amplitude and phase signals to avoid out of phase distortion. This is a very challenging.

![Simulated Output Spectrum](image)

**Figure 2-9** Simulated Output Spectrum for a 1-MHz envelope filter, with and without Delay Compensation[16]

Figure 2-9 indicates the simulated RF output spectrum when the envelope signal is filtered by a second-order Butterworth low-pass filter with a 3-dB frequency of 1 MHz. [16]The output spectrum at 400 and 600 kHz frequency offset are the most critical points and at these points, the spectral mask is violated. With delay compensation, the corresponding EVM is 1.7%, which is well below the required 9%.
2.3 Summary

This chapter conducts a literature review of efficiency and linearity enhancement schemes and all techniques used in the research. It also mentions the challenges in implementing an amplitude phase separation modulation scheme, which needs to be overcome for next generation wireless communication applications.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Time Misalignment</th>
<th>Bandwidth Requirement</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVS</td>
<td>No</td>
<td>Low</td>
<td>Lowest (decent)</td>
</tr>
<tr>
<td>ET</td>
<td>Yes (fixed pre-distortion)</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>EER</td>
<td>Yes</td>
<td>Highest</td>
<td>High</td>
</tr>
<tr>
<td>Polar Modulation</td>
<td>Yes (fixed delay compensation)</td>
<td>High</td>
<td>Highest</td>
</tr>
</tbody>
</table>
Chapter 3 Ripple Cancellation Technique

For power supplies in power management IC applications, switching power converters for high frequency application requires a fast transient response and tight tolerance. Therefore, in such cases, using a smaller output filter inductor is the most effective solution. However, the smaller output filter inductor causes a large ripple current in an output filter capacitor and induces an output voltage ripple. The large current and voltage ripple may affect the reliability and durability of electronic equipment.

Furthermore, the FCC has a very tight power spectral density emission mask to avoid the interference with other users in other frequency spectrums. The buck converter for CDMA application requires high linearity and high bandwidth. The distortion is mainly from inductor ripple, which is contributed by the inter-modulation products of harmonic clocks and the signal itself.

[20]first introduces the ripple cancellation technique. An additional auxiliary branch is added in parallel with the original stage to reduce inter-modulation products, which exhibit excellent noise performance. This chapter presents a derivation of this technique and proves it in time and frequency domains for a more thorough understanding of noise analysis.
3.1 Time Domain Ripple Cancellation Derivation

Figure 3-1, shows a step down buck converter. The auxiliary branch[20] is added to help cancel inductor current ripple during the switching. Figure 3-2 shows the key waveforms to demonstrate the ripple cancellation circuit.

At steady state, the voltage across capacitor C and capacitor C₂ can be expressed as below:

\[ V_C = D \times V_{in} \]

\[ V_{C2} = (1 - 2D) \times V_{in} \]

Inductor current can then be expressed as:

\[ i_L = \frac{V_{in} - V_C}{L} \times t + I_{L0} \]  
(3.1)

\[ i_{L2} = -\frac{V_{C2} + V_C}{L} \times t + I_{L20} \]  
(3.2)

The current shown at the load is the sum of equations (3.1) and (3.2)

\[ i_L + i_{L2} = \left( \frac{1 - D}{L} \right) \times V_{in} + I_{L0} - \left( \frac{1 - D}{L} \right) \times V_{in} + I_{L20} = I_{L0} + I_{L20} \]  
(3.3)

Equation (3.3) can be true if the same inductor values are chosen for the two branches. In time domain point of view, the ripple current would be cancelled fully.
Figure 3-1 Ripple Cancellation Circuit [20]

Figure 3-2 Key Waveform of Ripple Cancellation Circuit [20]
3.2 Frequency Domain Ripple Cancellation Derivation

A novel derivation of Ripple Cancellation Technique in frequency domain is proposed in this section. This derivation can indicate the magnitude of noise at any particular frequency. It also provides a more comprehensive analysis of noise in all aspects.

For the HFWB Buck Converter, a fixed on-time modulation scheme is chosen, which exploits a varying off-time duty cycle to realize negative feedback. As shown in Figure 3-3 and Figure 3-4, when a 10 KHz cosine $V_{\text{ref}}$ signal is sent with the sampling frequency $f_{\text{sw}}$ of 10MHz at point A, the signal in the Fourier series expansion [21] [22] [23]is as shown in the following equation:

$$F_{\text{NADS - powersage}} (t) = DC + M \cos(y) + 2 \sum_{m=1}^{\infty} \frac{1 - J_m(m\pi M)}{m\pi} \sin(m\pi) - 2 \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{J_m(m\pi M)}{m\pi} \sin(mx + ny - m\pi - \frac{n\pi}{2})$$

(3.4)

![Figure 3-3](image1.png)  ![Figure 3-4](image2.png)

- Figure 3-3  Eq3.4 in Frequency Domain
- Figure 3-4  Eq 3.4 in Time Domain
For the signal at point A, see Figure 3-3 for display in frequency domain and Figure 3-4, for display in time domain.

Assuming a square wave with maximum amplitude \( M \), the signal before the inverter is \( x(t) \) and the signal at the output of the inverter is \( y(t) \). It has a relationship such that

\[
y(t) = M - x(t),
\]

so \( x=M \) corresponds to \( y=0 \)

In addition, when \( x=0 \) then \( y=M \).

The same applies to Fourier series expansions of \( x(t) \) and \( y(t) \). So if

\[
x(t) = \text{sum of terms},
\]

\[
y(t) = M - \text{sum of terms}
\]

Therefore, the signal after the auxiliary branch at point B in Fourier series expansion expression is as shown in:

\[
F_{\text{NADS auxiliary branch}}(t) = M1 - DC - M \cos(y) + 2 \sum_{m=1}^{\infty} \frac{1-J_m(m\pi M)}{m\pi} \sin(m\pi) + 2 \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} J_{m+n}(m\pi y) \sin(mx - m\pi - \frac{n\pi}{2})
\]

\[(3.5)\]

Figure 3-5 Eq 3.5 in Frequency Domain

Figure 3-6 Eq 3.5 in Time Domain
Figure 3-5 displays the signal at point B in frequency domain and Figure 3-6, at the same point in time domain. It can be seen from Figure 3-4 and 3-6 that the DC offset at point A plus the DC offset at point B is constant and the amplitude of both the signals are the same, but out of phase with each other.

Figure 3-7 Simulation Result of the Output of Auxiliary Branch and Vout

Figure 3-7 displays the simulation result of the auxiliary output and that of Vout in the Cadence Specter. The result is identical to that obtained in MATLAB. The duty ratio of both the signals is different; the phases of the signals differ by 180 degrees.

Fourier expansion can help in performing many more functions. It can single out the intermodulation between certain signals at certain harmonic terms. Figure 3-8 displays the intermodulation products with all harmonics of Vref at second harmonics switching frequency; Figure 3-9 displays the same at third harmonics switching frequency.
Fig. 3-8 Second Harmonic of Eq. 6.4  

Fig. 3-9 Third Harmonic of Eq 6.4

Fig.3-10 is the simulation result of auxiliary output and of Vout in Cadence Spectre in the frequency domain.

Figure 3-10 Simulation Result of the Output of Auxiliary Branch and Vout
As shown in Figure 3-10, the magnitude of the signals is the same. As compared to Figure 3-3 and Figure 3-5, there is no distinguished noise at certain frequencies in Figure 3-10. This is because of the effect of the fixed-on-time control scheme.

The impedance at point A can be derived and is equal to:

$$Z_1 = \frac{1}{sC_{out}}R_{load} + \frac{1}{sC_{out}}sL_o + \frac{1}{sC_{out}}R_{load} sL_o \approx R_{load} + sL_o$$

(3.6)

The impedance at point B is derived and is equal to:

$$Z_2 = \frac{1}{sC_{out}}R_{load} + \frac{1}{sC_{out}}sL_{cancel} + \frac{1}{sC_{out}}R_{load} sL_{cancel} + \frac{1}{sC_{out}}sC_{cancel} + \frac{1}{sC_{cancel}}R_{load} + \frac{1}{sC_{cancel}}$$

$$\approx R_{load} + sL_{cancel} + \frac{1}{sC_{cancel}}$$

(3.7)

$L_{cancel}$ and $C_{cancel}$ form a band pass filter followed by auxiliary branch. The inductor current ripple shown at the output can be expressed as follows:

$$-2 \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{J_n(m\pi M)}{m\pi} \sin(mx + ny - m\pi - \frac{n\pi}{2}) \frac{A||B||D}{Z_1} + 2 \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{J_n(m\pi M)}{m\pi} \sin(mx + ny - m\pi - \frac{n\pi}{2}) \frac{A||B||C}{Z_2}$$

(3.8)

$$A = \frac{1}{sC_{OUT}}$$

$$B = R_{load}$$

$$C = I_{out}$$
\[ D = I_{\text{cancel}} \]

It can be seen that the high frequency inter-modulation term is cancelled optimally when

\[ sC_{\text{cancel}} \text{ is large and when } L_{\text{cancel}} = L_0. \]

Figure 3.11 shows the comparison of the output waveform (i) with ripple cancellation branch and (ii) without ripple cancellation branch. The inductor ripple reduces from 70mV to 12mV.

Figure 3-11 (a)Comparison with and without Ripple Cancellation in Time Domain (b) Zoom In
Figure 3-12 shows the complete transfer function plot of $Z_1$ and $Z_2$ over the frequency range. It indicates that when frequency increases, then $Z_1$ equals $Z_2$.

**3.3 Summary**

This chapter presents thorough derivations of the ripple cancellation technique in time and frequency domains and its simulation in MATLAB. The frequency domain derivation of the technique is novel. The simulation results in MATLAB concur with those in Cadence Specter, demonstrating that the equation derivations are correct.
Chapter 4 High Fidelity Wide Bandwidth (HFWB) Buck Converter

This chapter gives a review of control topologies. It introduces the proposed novel HFWB Buck Converter, describing all functional blocks including the control logic of the converter. Thirdly, it gives a thorough derivation of large and small signal analysis to observe the depth of the parameter impact on switching frequency, DC Offset, transfer function from error amplifier loop, transfer function from duty ripple loop, transfer function from input to output, transfer function from duty to the output, and the transfer function of the entire modulator. Fourthly, it presents the tradeoff and comparison with and without an auxiliary branch modeled in MATLAB.

4.1 Review of Control Topologies

4.1.1 Current Mode Control and Voltage Mode Control

Figure 4-1 shows the conventional voltage mode control. The output voltage is sensed to compare with the ramp; when the ramp signal is bigger than the sensing voltage, it turns on the switch; when the clock pulse is high, the switch is turned off. It is a two poles system and requires a complicated PID compensator design. Because of the clock pulse and artificial ramp, harmonic noise is always present.
Figure 4-2 is a conventional current mode control. [25-29] There are two loops in the control system: a voltage loop and a current loop. The error signal is compared with the inductor current to turn on the switch; the clock pulse turns the switch off. The advantage of the current mode control is that when the current loop is closed the system becomes a first order system. One of the poles moves to a higher frequency, which eases the compensator design compared to the voltage mode control. When the ratio of duty is greater than 0.5, the system grows to be unstable. A small noise in the control loop would lead to a big perturbation in the duty cycle. The common solution to this issue is to add an artificial ramp. When an artificial ramp is added with the current signal, it provides an additional degree of freedom to avoid potential instability. Normally PI compensator is necessary to improve DC accuracy. Regarding the current mode control, if the switching frequency is less than 1MHz, the current sensor can easily be designed but not for a value higher than this. The downsides of the
current mode control are that its noise immunity is unsatisfactory. The switching noise can prematurely reset the latch and disrupt the operation. Furthermore, an additional current sensing circuit is necessary to obtain current information. From the harmonic noise perspective, the harmonic terms can be composed by viewing the periodic artificial ramp and clock pulse in frequency domain. When the signal from the voltage loop is compared against the sensed inductor current signal, (which adds with the artificial ramp), inter-modulation product generates. Especially, a negative feedback loop causes deterioration by generating harmonic noise.

Figure 4-2 Current Mode Control[24]

4.1.2 Hysteretic Control

Figure 4-3 shows the conventional hysteretic control [30-32]. Hysteretic control depends on output ESR to perform the regulation. It feeds the ripple back to compare with the Vref
voltage, so that the duty cycle can be generated. Its output voltage ripple is vulnerable. Therefore, the ESR needs to be large. As Figure 4-4 [33] shows when the inductor current changes, ESL will generate a signal as shown in Figure 4-4(b). If the sum of $v_{ESL}$, $v_{ESR}$, and $v_{C_0}$ is in phase with the inductor current, then the feedback of the hysteretic control can be realized. If the ESR ripple is quite small, then no ripple is available for use as feedback. The reason is that the duty cycle is used to control the current. The switching frequency of this topology varies when Vref is an AC signal because the duty ratio is not fixed. In addition, this topology gives an excellent dynamic characteristic. A compensator is not necessary. As the switching frequency is not fixed, there will be no harmonics concentrated at the particular frequency. This means that the noise will spread out. The drawback of this topology is that the switching frequency is fully dependent on the Vref voltage, which is not controllable by any means.

Figure 4-3 Hysteretic Control[34]
Figure 4-5 is the improved version of hysteretic control [35-38]. It senses the inductor current to add a ramp with the output voltage ripple. The noise immunity can be improved with this additional ramp. There is a trade-off between noise sensitivity and transient response. The added ramp cannot be too large, otherwise DC Offset and transient response...
get worse. The reason is that when the ramp is large, no duty cycle can be generated. The transient response would be very slow.

![Diagram of a circuit](image)

Figure 4-5 Improved Hysteretic Control[36]

4.1.3 Hybrid Switching Modulator

As the earlier section mentions, the Polar Transmitter is being amply researched, for achieving a high data rate and high efficiency. [39]When a complex signal is split into its amplitude and phase components, the bandwidth of each component becomes wider than that of the original. Because of this, in spite of its low efficiency, a wideband low-dropout (LDO) linear amplifier is most often used in the amplitude path.

The conceptual Hybrid switching amplifier [39, 40]consists of a master-slave structure as Figure. 4-6 shows. The idea is based on the difficulty of designing a linear amplifier with
wide bandwidth, low output impedance, and high current-driving capability. It has a wideband linear amplifier as a voltage source and a switching amplifier as a current-controlled current source. The wideband linear amplifier accurately controls the output voltage, which requires high linearity. The switching amplifier efficiently supplies most of the output current by sensing and amplifying the current from the feed forward path.

A third order LC filter is used in the current loop and an additional zero is added from the loop compensation. This is because there are two poles, resulting from the integrator and the inductor.

Figure 4-6 Hybrid Switching Amplifier with the Third Order Ripple Filter and the Current Feedback[39]
[39] shows that the Hybrid Switch Amplifier is able to improve and achieve 88% efficiency by following the EDGE signal. It also follows the EDGE signal through different load conditions, varying from 4 ohm to 50 ohm. However, [39] also mentions that unresolved noise is concentrated at 2MHz and the switching frequency, and other noise at 3MHz resulting from the DAC on the DSP board.

4.2 Topology of High Fidelity Wide Bandwidth (HFWB) Buck Converter

Because the application is for wireless communication, in order to deal with the noise issue and to achieve high speed, an HFWB Buck Converter is proposed. It eliminates the need for a compensator and an external clock; it has a fixed on time control scheme to spread out the noise. An auxiliary branch (introduced in Chapter 3) helps further reduce the noise up to 15 to 20 dB.

Figure 4-7 shows the conceptual block diagram of a High Fidelity Wide Bandwidth (HFWB) Buck Converter. \( V_g \), \( V_{ref} \), and \( V_{out} \) refer to the Input voltage, Reference voltage and Output voltage respectively. It is a synchronized buck. The power stage consists of a high side PMOS switch and a low side NMOS switch. The gate drive has a level shifter and a dead time control generator. At point A, the half bridge converts the input voltage to the switch node voltage. The output filter comprises the power inductor (\( L_o \)) and output capacitor (\( C_{F1} \)). The other notations are:
R_{DCR}: DCR resistance of the inductor

R_{ESR}: Equivalent series resistance of the output capacitor

R_{ESL}: Equivalent series inductance of the output capacitor.

R_{D1} and R_{D2} form a voltage divider to sense the output voltage.

As Figure 4-7 shows, to avoid having an active block (to sense the inductor current), an RC network (R_{SENSE} & C_{SENSE}) is formed, for the same purpose. A square wave at point A would be converted to a triangle wave when the sensing time is much smaller than the RC time constant; this generates a control ripple voltage to be compared with the signal coming out from the voltage loop. The DDA (Differential Different Amplifier) [41-44] is adopted as an error amplifier at the feedback loop because it has excellent noise performance. The Differential Different Amplifier amplifies the voltage difference and adds it back to V_{OUT}. H is the gain of the V_{OUT} sensing network. As the control ripple voltage meets the edge of the signal coming from the DDA, the fixed on-pulse is generated. By design, the on-pulse width satisfies the switching frequency requirement and the off-pulse regulates V_{OUT}. In general, using fixed on time control scheme is discouraged, because the switching frequency is not fixed like the cutoff frequency of the output filter; this could cause the filter factor to be inconsistent. Yet this design uses a fixed on-time control scheme, placing it after the comparator to further spread out the switching frequency. Use of hysteretic control reveals that the varying switching frequency tends to spread out the harmonic noise. Secondly, in the current publication, the PFC application employs a fixed on-time used control scheme.
Thirdly, there is an additional auxiliary, which is always off phase to help reduce the ripple. Thus, the non-constant switching frequency issue can be ignored.

Figure 4-7 Conceptual Block Diagram of HFWB Buck Converter
Table 4-1 Comparison between Different Control Methods

<table>
<thead>
<tr>
<th>Control Method</th>
<th>Speed</th>
<th>Noise</th>
<th>Harmonics Noise</th>
<th>Compensation</th>
<th>Switching Frequency</th>
<th>DC Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Mode Control [24]</td>
<td>slow</td>
<td>Good</td>
<td>Yes</td>
<td>PID</td>
<td>Controllable</td>
<td>Good</td>
</tr>
<tr>
<td>Current Mode Control [29]</td>
<td>Medium</td>
<td>Bad</td>
<td>Yes</td>
<td>PI</td>
<td>Controllable</td>
<td>Good</td>
</tr>
<tr>
<td>Hysteretic Control [34]</td>
<td>Fast</td>
<td>Bad</td>
<td>Good</td>
<td>None</td>
<td>Not in control</td>
<td>Medium</td>
</tr>
<tr>
<td>Hybrid Switching Modulator [39]</td>
<td>Medium</td>
<td>Good</td>
<td>Bad</td>
<td>Required</td>
<td>Controllable</td>
<td>Good</td>
</tr>
<tr>
<td>Present Work (HFWB Buck)</td>
<td>Fast</td>
<td>Good</td>
<td>Better</td>
<td>None</td>
<td>Controllable</td>
<td>Medium</td>
</tr>
</tbody>
</table>

Table 4-1 compares various control methods for topology selection. The proposed HFWB buck converter is like an advanced version of conventional hysteretic control. It retains the existing functionalities and improves with features such as controllable switching frequency, greater speed than current mode and voltage mode, improved noise immunity, and capability to spread out the harmonics noise.

4.3 Switching Frequency Analysis of HFWB Buck Converter

FCC has a stringent emission mask. The major portion of the noise from the conventional buck converter is concentrated at the switching frequency and its harmonic terms. This provides a hint that spreading out the switching frequency can ease this major noise problem caused by the switching frequency.

For fixed on-time scheme, the switching frequency is the factor of duty cycle, input voltage, output voltage, and load current. The following paragraph derives the relationship among
them. It also takes into account and derives the impact of the parasitic resistance on the switching frequency.

For the fixed on-time scheme[45], the relationship between duty cycle, input voltage, and output voltage can be expressed as

\[ D = \frac{T_{ON}}{T_S} = T_{ON} \ast f_s = \frac{V_{out}}{V_g} \]  

(4.1)

The switching frequency can be expressed as

\[ f_s = \frac{V_{out}}{V_g T_{on}} \]  

(4.2)

Eq.4.4 shows that during on time the voltage across the inductor is

\[ 0 + V_g - I_O \ast R_{ON} - I_O R_L - V_{OUT} - V_{Loss} = 0 \]  

(4.3)

\[ 0 + V_g - I_O \ast R_{ON} - I_O R_L - V_{OUT} = V_{Loss} \]  

(4.4)

Eq.4.6 shows that the voltage across the inductor during off time is

\[ 0 - I_O \ast R_{ON} - V_{Loss} - I_O R_L - V_{OUT} = 0 \]  

(4.5)

\[ 0 - I_O \ast R_{ON} - I_O R_L - V_{OUT} = V_{Loss} \]  

(4.6)

Eq.4.8 shows that, by the inductor volt-second balance principle,
\[ T_{ON} * V_{LON} + T_{OFF} * V_{Loff} = 0 \]

(4.7)

\[
 f_s = \frac{V_{Loff}}{T_{ON} * (V_{Lon} - V_{Loff})} = \frac{V_{OUT} + I_Q R_L + I_Q R_{ON}}{V_g - I_Q R_{ONPMOS} + I_Q R_{ONN}} \cdot \frac{1}{T_{ON}}
\]

(4.8)

From Eq. 4.8, it can be inferred that when load current increases, switching frequency also increases. Figure 4-8 is the summary lot of output waveforms versus load line variation. It can be observed that the output ripple increases while the load decreases. This is because, when the load decreases, the switching frequency decreases. Therefore, the output ripple increases.
Figure 4-8 output voltage waveform through different load conditions (a) 4ohm (b) 11ohm (c) 22ohm (d) 47ohm (e) 100ohm (f) 200ohm
4.4 Steady State Error Analysis of HFWB Buck Converter

The accuracy of the DC output is a major concern. Based on the derivation below, we can conclude that circuit delay, control ripple amplitude, and the offset of DDA and Comparator can cause DC offset. This section analyzes offset of the output DC.

In Figure 4-9, let us assume that there is a voltage drop between $V_{rd}$ and $V_{out}$ (because of the DCR of the power inductor). $V_{rd}$ is the average of the control ripple voltage. An RC network senses the control ripple voltage. The control voltage can be written as Eq.4.9.

![Figure 4-9 Waveform of the Control Ripple Voltage and Vn for Offset Analysis](image)

$$V_c(t) = (V_c(t) - V_g)e^{-t_{on}} + V_g = V_{co} \frac{T_{on}}{RC} + V_g \frac{T_{on}}{RC} + V_{co}$$

(4.9)
There is a slight voltage difference between the sensed voltage and $V_{out}$ of $Io*R_{DCR}$

$$V_{out}(t) = V_{co} \left( \frac{2RC - T_{on}}{2RC} \right) + \frac{T_{on}V_{g} - 2RCI_{o}R_{DCR}}{2RC}$$

(4.10)

$$V_c = V_{out} - K(HV_{out} - V_{ref}) = V_{out} - KHV_{out} + V_{ref}$$

(4.11)

The steady state error is the difference between $V_{out}$ and the expected output from $V_{ref}$.

Eq.4.12 shows that

$$Steady\_State\_Error = \frac{V_{ref}(2RC - T_{on})T_{on}V_{g} - 2RCI_{o}R_{DCR} - (KV_{ref})(2RC - T_{on})}{(KH)(2RC - T_{on})}$$

(4.12)

Eq.4.12 shows that when load increases, DC offset decreases; again, when the gain of the DDA increases, the DC offset decreases. In addition, the DC offset drops when the amplitude of the control ripple voltage decreases.

**4.5 Small Signal Analysis of HFWB Buck Converter**

This section develops a thorough small signal model for the HFWB buck converter to observe the effect of duty cycle and input line on the output. It also derives the following:

- Transfer function from input to duty ripple
- Transfer function from duty cycle to duty ripple
- Transfer function of the modulator
• Modulation gain $F_m$

• Coefficient of input voltage $F_g$

The HFWB buck converter has an additional auxiliary branch in parallel with the original stage to reduce the inter-modulation products and harmonics.

The section also compares the transfer function with the cancellation branch (and without) to observe the tradeoff with the ripple cancellation technique (and without). The transfer function plots in this section are for proving that the derivation is correct. The parameters for the transfer function plots are not the exact values used for the design.

4.5.1 Transfer function of the power stage

Figure 4-7 shows the power stage of the synchronized buck with ripple cancellation branch [20, 45]. Figure 4-10 shows the CCM PWM switch model for the power stage. By replacing the power stage model with the synchronized buck having ripple cancellation branch, the perturbation is applied. From Figure 4-11, we can obtain the transfer function of the power stage by superimposing and adding them up. The transfer functions from input to output can be expressed as below

$$V_{out} = D \times G_{v1} + (1 - D) \times G_{v2}$$

(4.13)

The final transfer function from input to output is

$$G_v = G_{v1} - G_{v2}$$

(4.14)
Figure 4-10 CCM PWM Switch Model[24]

Figure 4-11 Ripple Cancellation Technique[20]
The transfer function from the main power stage can be expressed as:

\[
G_{v1}(s) = \frac{D \cdot R_{\text{load}} (s^2 C_{\text{cancel}}^{-1} + 1)}{R_{\text{load}} + sL_O + s^2 (C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}) + s^2 C_{\text{cancel}}^{-1} + s^2 C_{\text{cancel}} C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}}
\]

(4.15)

The transfer function of the ripple cancellation branch can then be obtained:

\[
G_{v2}(s) = \frac{(1 - D) \cdot s^2 C_{\text{cancel}}^{-1} R_{\text{load}}}{R_{\text{load}} + sL_O + s^2 (C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}) + s^2 C_{\text{cancel}}^{-1} + s^2 C_{\text{cancel}} C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}}
\]

(4.16)

The transfer function from the input voltage to the output voltage can be obtained as

\[
G_{vg} = G_{v1} - G_{v2}
\]

(4.17)

The transfer function of the main power stage from duty to the output voltage can be expressed as

\[
G_{d1}(s) = \frac{V_g \cdot R_{\text{load}} (s^2 C_{\text{cancel}}^{-1} + 1)}{R_{\text{load}} + sL_O + s^2 (C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}) + s^2 C_{\text{cancel}}^{-1} + s^2 C_{\text{cancel}} C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}}
\]

(4.18)

The transfer function of the ripple cancellation branch from duty to the output voltage can be expressed as

\[
G_{d2}(s) = \frac{V_g \cdot s^2 C_{\text{cancel}}^{-1} R_{\text{load}}}{R_{\text{load}} + sL_O + s^2 (C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{cancel}} L_{\text{cancel}} R_{\text{load}} + C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}) + s^2 C_{\text{cancel}}^{-1} + s^2 C_{\text{cancel}} C_{\text{OUT}} L_{\text{cancel}} R_{\text{load}}}
\]

(4.19)

\[
G_{vd} = G_{d1} - G_{d2}
\]

(4.20)
Figure 4-12 Transfer Function from Duty Cycle to Output

Figure 4-13 Transfer Function from Duty Cycle to Output with and without Cancellation Branch
Figure 4-12 and Figure 4-13 demonstrate the feature and the tradeoff of HFWB with and without auxiliary cancellation branch. From Figure 4-12 and Figure 4-13, it can be seen that the entire system is still stable. However, initially there is a double pole peaking at 2 MHz, which shifts to 900K on adding the cancellation branch. Bandwidth is sacrificed to improve the linearity.

### 4.5.2 Transfer function of the DDA loop

This section shows the derivation of the transfer function from $V_{\text{out}}$ to DDA output.

\[
T = \frac{T_m C_s R}{R_g + 1}
\]

(4.21)

![Figure 4-14 Closed Loop of DDA Circuit](image-url)
\[ V_n = -K_n \ast (HV_{out} - V_{ref}) + V_{out} \]

(4.22)

\[ \frac{V_{out}}{V_n} = \frac{-1}{1 - K_n H} \]

(4.23)

\[ G_{cv}(s) = \frac{g_m R_T}{1 + sR_T C_T} \approx g_m R_T \frac{1 - K_n H}{(1 + sR_T C_T) (1 - K_n H)} + g_m R_T = \frac{(1 - K_n H)g_m R_T}{s_m R_T - K_n (1 + sR_T C_T)} \]

(4.24)

The positive control signal is the control ripple voltage sensed by the RC network. The transfer function from the switch node to the RC control ripple voltage output is

\[ G_{\text{sense-}d}(s) = V_s \frac{1}{sC_T} + V_s \frac{1}{R_T + 1 + sR_T C_T} \]

(4.25)

The total control signal transfer function is

\[ TF_{\text{total-control-voltage}} = G_{cv}(s) - G_{\text{sense-}d}(s) \]

(4.26)
Figure 4-15 Transfer Function from Switch Node to RC Control Ripple Voltage Output

Figure 4-16 Transfer Function from Vout to DDA Output
Figure 4-15 and Figure 4-16 show the bode plots of the transfer functions of the control signal from the negative loop (RC sensing network) and of the control signal from the positive loop (DDA error amplifier). The RC low pass filter contributes a 90-degree phase delay; there is a right hand pole at DDA, which gives a 90-degree phase at very high frequency. The gain of DDA does not break.

### 4.5.3 Transfer function of the duty ripple loop

There are two loops in the HFWB Buck Converter: an inner current loop and an outer voltage loop. The inner current loop causes the buck converter to change from a second order system to a first order system.

The derivation of transfer function from input to duty ripple and from duty cycle to duty ripple follows below: [24, 46, 47]

According to the charge balance on $C_{\text{sense}}$,

$$\frac{C_{\text{sense}}}{v_{\text{sense}}} \frac{d(v_{\text{sense}})}{dt} = \frac{Dv_{g} - v_{\text{sense}}}{R_{\text{sense}}}$$

(4.27)

After perturbation,

$$C_{\text{sense}} \frac{d(v_{\text{sense}})}{dt} + \frac{d(v_{\text{sense}})}{dt} = (\frac{Dv_{g} - v_{\text{sense}}}{R_{\text{sense}}} + (d \frac{\hat{v}_{g}}{R_{\text{sense}}} + D \frac{\hat{v}_{g}}{R_{\text{sense}}} - \frac{\hat{v}_{\text{sense}}}{R_{\text{sense}}} - \frac{\hat{v}_{g}}{R_{\text{sense}}}) \frac{d\hat{v}_{g}}{R_{\text{sense}}})$$

(4.28)

Keeping the first order term,
\[ C_{\text{sense}} \frac{d v_{\text{sense}}}{dt} = (d \frac{V_g}{R_{\text{sense}}} + D \frac{v_{\text{sense}}}{R_{\text{sense}}} - v_{\text{sense}}) \]

(4.29)

From the input line to the sensing ripple voltage

\[ C_{\text{sense}} v_{\text{sense}} = \frac{D v_g}{R_{\text{sense}}} - \frac{v_{\text{sense}}}{R_{\text{sense}}} \]

(4.30)

\[ v_{\text{sense}} \left( s C_{\text{sense}} R_{\text{sense}} + 1 \right) = \frac{D v_g}{R_{\text{sense}}} \]

(4.31)

\[ G_{\text{sense}}(s) = \frac{D}{(s C_{\text{sense}} R_{\text{sense}} + 1)} \]

(4.32)

From duty cycle to the sensing ripple voltage

\[ C_{\text{sense}} d v_{\text{sense}} = \frac{\dot{V}_g}{R_{\text{sense}}} - \frac{v_{\text{sense}}}{R_{\text{sense}}} \]

(4.33)

\[ v_{\text{sense}} \left( s C_{\text{sense}} R_{\text{sense}} + 1 \right) = \frac{\dot{V}_g}{R_{\text{sense}}} \]

(4.34)

\[ G_{\text{sense}}(s) = \frac{V_g}{(s C_{\text{sense}} R_{\text{sense}} + 1)} \]

(4.35)
4.5.4 Transfer function of the modulator

In order to design the feedback circuit and apply it to a DC-DC converter, it is necessary to develop a small signal model of hysteretic control scheme with an average power stage model. To obtain the transfer function of the modulator, the modulation gain $F_m$ \cite{24} can be defined as the ratio of the current duty perturbation to the difference of the current control signal perturbation. The derivation of $F_m$ and the coefficient for the input voltage $F_g$ is shown below:

$$\langle v_r(t) \rangle_{T_x} = \langle v_c(t) \rangle_{T_x} + \frac{dm_1 \frac{T_{on}}{2} + d m_2 \frac{T_{off}}{2}}{d + (1 - d)}$$

(4.36)

$$T_{off} = (1 - d) T_s = (1 - d) \frac{T_{on}}{d}$$

(4.37)

$$\langle v_r(t) \rangle_{T_x} = \langle v_c(t) \rangle_{T_x} + \frac{dm_1 \frac{T_{on}}{2} + d m_2 \frac{1 - d}{d} T_{on}}{d + (1 - d)}$$

(4.38)

$$\hat{v}_r(t) = \hat{v}_c(t) + \frac{\hat{d}(t) M_1}{2} + \frac{\hat{d}(t) M_2 T_{on}}{2 D^2} + \frac{(D - 1)(D + 1) \hat{d}(t) M_2 T_{on}}{2 D} + \frac{(1 - D)^2 M_2(t) T_{on}}{2 D}$$

(4.39)

$$M_1 = \frac{V_g - V_o}{R_{sense} C_{sense}}$$

(4.40)
\[ M_2 = \frac{V_o}{R_{\text{sense}}C_{\text{sense}}} \]  

(4.41)

\[ m_1 = \frac{\hat{v}_g - \hat{v}_o}{R_{\text{sense}}C_{\text{sense}}} \]  

(4.42)

\[ m_2 = \frac{\hat{v}_o}{R_{\text{sense}}C_{\text{sense}}} \]  

(4.43)

When considering \( \hat{v}_c \) alone, keep the value of other derivatives at zero (except that of DC).

Replacing \( V_O \) by \( DV_g \), the modulation gain and the coefficient for the input voltage \( F_g \) can be obtained:

\[ F_m = \frac{2DR_{\text{sense}}C_{\text{sense}}}{T_{\text{on}}V_g(1-D)} \]  

(4.44)

\[ F_s = \frac{DT_{\text{on}}}{2R_{\text{sense}}C_{\text{sense}}} \]  

(4.45)
4.5.5 Small Signal Model of the HFWB Buck Converter

Figure 4-17 shows the complete small signal modeling blocks of HFWB buck converter:

![Small Signal Blocks of HFWB Buck Converter](image)

Figure 4-17 Small Signal Blocks of HFWB Buck Converter
\[ M_1(s) = \frac{sT_m(1-D)(1-e^{-sT_s})}{2D(sT_s + e^{-sT_s} - 1)} \]  
(4.46)

\[ M_2(s) = \frac{sT_m(D)(1-e^{-sT_s})}{2(1-D)(sT_s + e^{-sT_s} - 1)} \]  
(4.47)

\( F_m \) is the modulator gain[24]. It is the coefficient between \( d \) and \( c \). \( M \) is the sampling and hold to model SR latch. In continuous time interval, it is a term of \( e^{-sT_s} \). The input coefficient \( F_g \) is also present in the equation \( d = F_mF_g \), which is the coefficient of \( V_g \) to \( d \). In Figure 4.18, it can be seen that the delay from sampling and hold is little.

Figure 4-19 and Figure 4-20 show the transfer functions of \( G_{vd} \) and loop gain comparison, with auxiliary cancellation branch and without auxiliary cancellation branch respectively. It can be seen that when the loop is closed the pole moves to a higher frequency. In Figure 4-19, with the ripple cancellation branch, the pole moves to a higher frequency because of the closed current loop. In Figure 4-20, without the cancellation, it exhibits an excellent single pole response.

The open loop transfer function of HFWB Buck Converter is the calculation from where the point is broken in the loop back to where the point originally was.

\[ T(s) = \frac{F_m[M_1(s)G_{vd}(s) - M_2(s)G_{vd2}(s)]G_{cv}(s)}{1 + F_mM_1(s)G_{sense ... d}(s)} \]  
(4.48)

The open loop transfer function without a cancellation branch is:
\[ T(s) = \frac{E_m \left[ M(s)G_{vd}(s) \right] G_{es}(s)}{1 + E_m M(s) G_{sense,d}(s)} \]

(4.49)

Figure 4.18 SR latch transfer function of HFWB Buck Converter
Figure 4-19 Open Loop Transfer Function of HFWB Buck Converter

Figure 4-20 Open Loop Transfer Function without Cancellation Branch
Figure 4-21 is the simulation plot from Simplis[48]. Its POP analysis and AC analysis rapidly locate the steady state operating point of a switching system and emulate a frequency sweep measurement as might be conducted on real hardware producing gain and phase plots without small signal model derivation and startup transient conditions. It can be seen that the simulation result matches the plots from MATLAB. Yet the phase margin is reduced. It can be understood that when pushing the bandwidth to a higher frequency, the phase margin reduces because of the high frequency pole. Without the cancellation branch, its bandwidth can be pushed to 11MHz and there is a double pole peaking at 2MHz. However, with the cancellation branch, its bandwidth reduces it to 3MHz and the double poles are shifted to 900KHz.

![Figure 4-21 DC Gain and Phase Margin with and without Ripple Cancellation](image-url)
4.6 Summary

Buck converters are popular because of their high efficiencies and other qualities. This chapter conducts a literature review of the buck converter. It points out the advantages and disadvantages between the topologies. The chapter proposes an HFWB buck converter with an inductor switching ripple cancellation technique. It also presents a thorough derivation of large and small signal analysis of the HFWB buck converter with auxiliary branch. This is for studying the effects of the parameter on: switching frequency, DC Offset, transfer function from error amplifier loop, transfer function from duty ripple loop, transfer function from input to output, transfer function from duty to the output, etc. The derivation results are modeled in MATLAB and matched to the control theory; the measurement and simulation results in Chapter 5 match the derivation results.
Chapter 5 Monolithic Implementation of HFWB Buck Converter with Ripple Cancellation

5.1 Differential Difference Amplifier reviews and design

In the control scheme of the HFWB buck converter, the Differential Difference Amplifier (DDA)[41-43, 49] is a key block. Because of high speed application and wide input and output voltage applications, a rail-to-rail DDA becomes a suitable candidate to sense the voltage difference between $V_{OUT}$ and $V_{ref}$.

Differential Difference Amplifier though an old technique, is very well developed. It is also known as Active Feedback Amplifier. Figure 5-1 and Figure 5-2 show the model and basic structure of the Differential Difference Amplifier. The inputs have a relationship as shown in Eq.5.1 when the loop is closed; this relation is always true.

![Figure 5-1 Model of DDA][43]
\[(X_1 - X_2) = (Y_2 - Y_1)\]

(5.1)

In Figure 5-2, the current at point A = \(g_m \cdot (X_1 - X_2) + g_m \cdot (Y_1 - Y_2) = 0\), which means \((X_1 - X_2) = (Y_2 - Y_1)\). This can be understood from Figure 5-3. For a closed loop, because of the negative feedback network and the infinite gain of the second stage, the output is being locked at a certain value; the very tiny value at the input after passing through an infinite gain will reach this value. Because the gain is infinite, the input of the signal should be extremely small; this means \((X_1 - X_2) = (Y_2 - Y_1)\). If for both input stages the value \(g_m\) is the same, it follows that \((X_1 - X_2) = (Y_2 - Y_1)\).
DDA has a distinct input output common mode level. It has an advantage that it separates the signal input and the feedback network whenever it is required to sense a differential voltage at the input whose common mode level is different from that at the output. Normally the error of the Opamp at unity frequency is 50%. DDA can provide accurate performance right up to its unity-gain frequency.

Figure 5-6 shows the transistor level DDA. It consists of three parts: $g_{m1}$, $g_{m2}$, and a class AB amplifier stage. Because of a wide input and output range, the transconductance stage $g_{m1}$ and $g_{m2}$ is a rail-to-rail input stage by having both NMOS and PMOS differential pairs. The second stage of DDA is a class AB amplifier. Figure5-4 shows the second stage of a class AB amplifier. Four currents are summed up at the input of the class AB amplifier. It directs
the gate voltage of MP25 & MN26 towards the same direction by push-pull. The output is therefore allowed to swing from rail to rail.

![Figure 5-4 Class AB Amplifier - Second Stage](image)

### 5.2 Constant Input gm Stage

A downside of the rail-to-rail input stage is that its $g_m$ is not consistent over the entire common-mode input range; it varies by a factor of two over the range. To avoid a near band distortion, it requires a constant $g_m$ in the input stage. For this, the $g_m$ at the lower and upper part of the common mode input range needs to be increased by a factor of two. The reason is that the $g_m$ of a MOSFET transistor that operates at strong inversion is proportional to the square root of its drain current; the tail current of the actual active input pairs needs to increase by a factor of four.
The above concept can be realized by adding two \( g_m \) -control switches and two current mirror pairs as the topology in Figure 5-5 [42] shows. M5 and M8 are the two switches; M6 - M7 and M9 – M10 are the two current mirror pairs, having a gain of three.

Figure 5-5 Rail-to-Rail with \( g_m \)-Control by Three Times Current Schematic [42]

The concept is to divide the common-mode input range into three parts as follows [46]:

1. Low common-mode input voltages (between VSS and VSS + 1 V):
   At this point only the P-channel input pair is conducted. The NMOS current switch is on. The N-channel current switch directs the current \( I_{ref1} \) to the current mirror, M6 - M7. Here it is multiplied by a factor three and added to \( I_{ref2} \). Since \( I_{ref1} \) and \( I_{ref2} \) are equal, the tail-current of the P-channel input equals 4 \( I_{ref1} \).

2. Middle common-mode input voltages (between VSS + 1.3 V and VDD - 1.3 V):
The input pairs of both P and N channels operate; both current switches are off. The consequence is that the tail currents of the N-channel diff input pair and that of the P-channel diff input pair are equal to Iref.

3. High common-mode input voltages (between VDD - 1 V and VDD):
In this case, only the N-channel input pair operates. The P-channel current switch solely conducts the current. The P-channel current switch feeds the current $I_{ref2}$ into the current mirror, M9 – M10. Here it is multiplied by a factor of three and added to the current $I_{ref1}$. The result is that the tail-current of the N-channel input pair equals $4I_{ref2}$. 
Figure 5-6 Transistor Level of DDA
5.3 A fixed on Time Generator Circuit

FCC has a stringent power spectral density emission mask to avoid interference with users in other frequency spectrums. The buck converter for CDMA application requires high linearity.

The distortion occurs mainly from inductor ripples; these are because of clock harmonics, the inter-modulation products of harmonic clocks, and the signal itself. A fixed on-time buck converter was considered to avoid noise power being concentrated at the harmonics of the switching frequency.

Figure 5-7 shows the on-pulse generator. The control ripple voltage is sensed by an RC low pass filter and compared with the signal from the DDA. As the control ripple voltage meets the edge of the signal coming from the DDA, a continuous pulse is generated. When $V_{\text{sen}} < V_{\text{ref}}$, the controller charges it up. $V_n > \text{input}_p \Rightarrow \text{period}_{\text{finish}}=1 \Rightarrow R=1$. When the controller starts, $S=0, \Rightarrow Q=0$. (The NMOS switch is turned off). Figure 5-8 shows the simulation result waveform sent by the IS-95 CDMA baseband signal.
5.4 Dead Time Generator Circuit

Dead time is used for pulse width-modulation (PWM)-controlled inverter/converter control, to avoid “shoot through” of the high-side and low-side power devices. The dead time mainly depends upon the characteristics of the power devices and the gate drive circuit. Shoot through current can be eliminated by creating a dead time such that PMOSFET and NMOSFET do not run at the same time. Figure 5-10 shows the dead time generator circuit.
The input comes directly from the output of the comparator. The signal, because it has to pass through a series of CMOS inverters, creates a delay.

The dead time control is for ensuring that when the PMOS switch is on, it (the PMOS switch) will turn off before the NMOS switch turns on; and when the NMOS switch is on, it (NMOS switch) will turn off before the PMOS switch turns on. The concept can be explained as shown below in Figure5-9. Initially when the top switch is on, the current flows from $V_{dd}$ to the load. Dead time control is certain when the top switch turns off before the bottom switch turns on. Because the inductor current has to be continuous, it forces $V_o$ to drop below ground so that the body diode of the bottom switch is in forward bias. When the bottom switch is on, the body diode of the bottom switch becomes reverse biased and turns off. Dead time control is again certain: bottom switch turns off before the top switch turns on. At this time, it forces $V_o$ below ground so that the body diode of the bottom switch is forward biased; this is for maintaining the continuity of the inductor current before the top switch can again be turned on.
In the delay cell, there are digital bits to fine tune the delay time over the corner variation. Multi-level delay can be generated as shown in Figure 5-11. It has a trade-off that introducing dead time into the circuitry results in signal dependant delay in the power stage, resulting in linearity degradation.
Figure 5-10 Conceptual Block Diagram of Dead Time Generator Circuit

Figure 5-11 Multi-level of the Delay Times by Dead Time Generator (a) Top Switch turns on (b) Top Switch turns off
In Figure 5-11, fine time n and fine time p blocks can adjust the delay individually to overcome the corner variation so that equal delay can be obtained between the rising and falling edges.

### 5.5 Rail-to-rail Comparator Circuit

The presented design provides the combination of a rail-to-rail comparator with an enable pin function. It was designed to fit the requirements for processing a wide swing CDMA signal for wireless communication applications. Its goal is to detect signals so that when the control ripple voltage is lower than $V_n$, a fixed on-time pulse can properly be generated.

Wide CDMA input voltage and minimum delay time availability are the factors that determine the comparator topology. One of the signals going into the comparator comes from the DDA, which follows Eq.5.1. It has wide voltage swing: from 1V to 5V. Because of the high-speed application, the link budget of the delay for the control loop is 25ns in total. The delay caused by the comparator should be reduced to a minimum.

Hence, an op-amp based comparator topology was selected. The input stages of the op-amp were determined by the rail-to-rail input requirement. The parallel combination of NMOS and PMOS differential pairs was selected. Regarding the high-speed requirement, a single stage topology is inappropriate because of the slow transition response (when the status of
the output transistor is changing from weak inversion to strong inversion). Therefore, a latch pair of the second stage topology is chosen as Figure 5-12 shows.
Figure 5-12 Rail-to-Rail Comparator
5.6 Level Shifter Circuit

Power transistors are typically large with high parasitic capacitance. A series of MOSFET gates are required. The gate driver are tapered. The gate drivers are controlled by a PWM, which generates the necessary control signals for the power MOSFETs such that a series of square pulse with an proper duty cycle is produced at node A (Figure 4-7). The duty cycle and/ or switching frequency are modified in order to maintain output voltage at the desired value.

The optimum gate voltage swing of a power MOSFET and its gate driver, which maximizes efficiency [50] is shown to be lower than a standard full voltage swing. A MOSFET gate drive with a lower swing is preferred.

At a reduced gate voltage, the effective series resistance of a MOSFET increases. Tapering factors are independent variables. A research study [50] has shown the optimum tapering factors for the full swing and low swing circuits to be 10 and 16 respectively. This design adopts a tapering factor of eight.

Power Transistor PMOS and NMOS ratio is also an independent variable in the efficiency. The optimum width ratio b of the PMOS and NMOS transistors within each MOSFET gate driver is found to be two as Figure 5-18 shows.
As the gate voltages are reduced from the full swing voltage, the effective series resistance of a MOSFET is increased; the total dynamic switching energy is decreased with reduced gate voltage.

A level shifter is used to reduce $V_{gs}$ across the gate drive in order to reduce switching loss. When $V_{gs}$ is reduced, $R_{on}$ increases, which forces an increase in size of the power stage. This is the tradeoff of the level shifter circuit. Level shifters are preferred for low load applications where power loss is dominated by switching loss. Optimum $V_{gp}$ $V_{gn}$, the power ground of PMOS gate driver and the power supply of NMOS gate driver respectively that maximize the efficiency.

The NMOS level shifter translates voltage from 0 - 3 volt to 0 - 2.5 volt; the PMOS level shifter translates voltage from 0 - 3 volt to 2.5 - 5 volt (Figure5-13). The implemented level shifter has improved power efficiency by 1%. 


5.7 Power Stage implementation of HFWB

The power stage implementation uses Synchronous buck topology. There is a high side PMOS switch and a low side NMOS switch. Because the load current has target at 1A, load impedance is low (only 5ohm). In addition, because the device is large-sized, parasitic resistance can create a larger problem because it can be comparable to load impedance. Therefore, the top priorities are sizing the power stage, creating the layout for the power stage to minimize its parasitic resistance, and making the layout size compact. The following layout approach is based on three metal layers available in the AMI 0.5um process and 1A load current condition.
The Multiple-finger method has been adopted to make the layout size compact. If \( n \) number of fingers is used, the advantage is that \( R_g \) becomes \( 1/n^2 \), which is a much smaller value (the width of each finger is \( n \) times smaller and \( n \) number of fingers is in parallel). Moreover, a large number of transistors are in parallel and share a junction; all gates are connected together; all sources are connected together, and all drains are connected together—this brings the capacitance down. This in turn reduces the switching loss.

As discussed earlier, the parasitic resistance is critical in this application. In order to reduce the conduction loss, the parasitic resistance at the drain and source of these two switches needs to be reduced to a minimum.

As illustrated in Figure 5-14, M2 & M3 are used in overlap in parallel, to route to VIN and GND pad. Since the current flows towards VIN and GND, parasitic resistance needs to be the lowest possible. Therefore M2 & M3 are used in parallel when routing the trace to the pad (with multiple pads as well) and the trace being kept as close to the pad as possible.
Fundamentally, from the layout point of view, the total $R_{eff}$ can be considered as the sum of parasitic resistance per finger. The parasitic resistance per finger is primarily by M1 & contact, with M2&M3&VIA of M1&M2, and M2&M3. When the width of a finger increases, the corresponding resistance contributed by M1 and contact also increases and the corresponding resistance contributed by M2&M3 decreases. An optimum finger number is required for this reason.

The effect is modeled using an iterative technique to simplify this network. The equivalent layout parasitic resistance is then modeled as a variable of the finger width included in the
parasitic resistance calculation; then the ideal width and number of finger for maximum efficiency are determined. In order to avoid a de-biasing effect, the remote source and drain effect can be modeled by a resistor network as shown in Figure 5-15.

Figure 5-15 Power Stage de-biasing Effect Modeling

\[
R_{i_{-1}} = \left( \frac{R_{i_{-1.2} + r}}{R + 2r} \right) R_{i_{-1.2} + R_{i_{-1.5}}}
\]
\[
R_{i_{-2}} = \left( \frac{R_{i_{-2.2} + r}}{R + 2r} \right) R_{i_{-2.2} + R_{i_{-2.5}}}
\]
\[
R_{i_{-3}} = \left( \frac{R_{i_{-3.2} + r}}{R + 2r} \right) R_{i_{-3.2} + R_{i_{-3.5}}}
\]
\[
R_{\text{tot}} = R_{i_{-1.1}} + R_{i_{-2.1}} + \ldots + R_{i_{-n.1}} + \left( R_{i_{-n.3} + r + R} \right) \left( R_{i_{-1.3} + r} \right)
\]

Figure 5-16 Equivalent Resistance Relationship for Adjacent Finger for de-biasing Effect Modeling
The equation shown in Figure 5-16 is the equivalent resistance relationship between two adjacent fingers. The iterative approach and the corresponding resistance calculation shown in Figure 5-16 made use of excel spreadsheet. The spacing of contact & poly&m1 sizing calculation follows the DRC rule as shown below to be the most compact. The width ratio of these two switches is set as a parameter and the optimized number was obtained through Parametric Analysis as shown in Figure 5-17 & Figure 5-18.

The number of the finger and the length per finger are relevant because of the fixed number of the total width. The effect of metal de-biasing is taken into account when determining the finger number. The values of Ron for the two MOSFETS are also determined as shown in Figure5-17. The width of PMOS is 41mm and that of NMOS is 20mm; PMOS and NMOS have 200 fingers each. The effective Ron values obtained though the de-biasing calculation are 300m ohm and 200m ohm respectively.

Parasitic inductance from the packaging is accounted for with a 2nH parasitic inductance at each source side of the top and bottom switches of the power stage. The gate resistance was calculated based on the number of fingers, the length of the finger, and the sheet resistance of poly. A 300m ohm, 200 m ohm gate resistance is used as the appendix shows.
Figure 5-17 Optimized Power Stage Width for HFWB Buck Converter

Figure 5-18 Optimized Ratio of NMOS/PMOS Width for Power Stage for HFWB Buck Converter
Figure 5-19 Optimized No. of Fingers for Power Stage for HFWB Buck Converter

Figure 5-20 shows a breakdown of system power loss.

Figure 5-20 HFWB Buck Converter System Power Breakdown
Figure 5-21 shows the breakdown of power loss inside the power stage.

Figure 5-21 HFWB Buck Converter Power Stage Loss Breakdown

5.8 Simulation, Layout, Packaging, Evaluation Board Design and Measurement Results of HFWB Buck Converter

5.8.1 Simulation

The design was implemented and simulated by AMI 05um technology in the Cadence Specter. Figure 5-22 compares $V_{\text{ref}}$ against $V_{\text{out}}$ in time domain. The $V_{\text{out}}$ curve follows $V_{\text{ref}}$ throughout the output voltage range of 1 - 5 volt. When the output voltage level is low, the voltage ripple is more noticeable because of the drop in switching frequency. Figure 5-23 & Figure 5-24 show the simulation results in frequency domain under emission mask while sending IS-95 baseband signals. With reference to the terms of the entire spectrum, there are no distinguished harmonics terms and inter-modulation terms. The cancellation shows the
improvement of linearity to be in the range 15dB - 20dB. However, at 1.98MHz, the output voltage does not fall within the emission limit by a slight margin. This is because of the design imperfection of the DDA for a combination of feedback signals and baseband signals. The simulation results show an average power efficiency of 78.9% with switching frequencies varying within 7.5MHz to 12.5 MHz. This proves that the proposed buck converter can be a suitable candidate for envelope tracking transmitter architecture.

![Figure 5-22 Vref (IS95 CDMA Baseband Signal) V.S. Vout](image-url)
Figure 5-23 Frequency Domain Simulation Plot (full range)

Figure 5-24 Frequency Domain Simulation Plot (near band)
### Table 5-1 HFWB Buck Converter Post Layout Simulation Result

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>Output voltage</td>
<td>Vout</td>
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<td>Switching Frequency</td>
<td>fsw</td>
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<tr>
<td>Output capacitor</td>
<td>Cout</td>
</tr>
<tr>
<td>Load resistance</td>
<td>Rload</td>
</tr>
<tr>
<td>Output Inductance</td>
<td>Lout</td>
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<tr>
<td>Switching Frequency Spur Suppression</td>
<td>&gt;50dBc/30KHz</td>
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<tr>
<td>Second Harmonic Spur Suppression</td>
<td>&gt;70dBc/30KHz</td>
</tr>
<tr>
<td>Load Current</td>
<td>Iout</td>
</tr>
<tr>
<td>Modulation Type</td>
<td>Hysteretic</td>
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<tr>
<td>Efficiency</td>
<td>78.9%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
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<tr>
<td>Switching Frequency</td>
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<tr>
<td>Load resistance</td>
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<tr>
<td>Output Inductance</td>
<td>180nH</td>
</tr>
<tr>
<td>Switching Frequency Spur Suppression</td>
<td>By sending IS-95met FCC emission mask</td>
</tr>
<tr>
<td>Second Harmonic Spur Suppression</td>
<td>By sending IS-95met FCC emission mask</td>
</tr>
<tr>
<td>Load Current</td>
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<tr>
<td>Modulation Type</td>
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<tr>
<td>Efficiency</td>
<td>78.9%</td>
</tr>
</tbody>
</table>

### 5.8.2 Layout

Figure 5-25 shows the layout of the entire HFWB Buck Converter chip. Multi-pad in parallel for the Power stages Vdd, Vout, and Gnd reduces the parasitic resistance. In order to reduce the noise caused by the digital part, all sensitive analog circuits (such as comparator, bias circuitry, and DDA) are placed at the farthest from the digital circuit to minimize the impact.

To separate the noise, there are multiple Vdd for Analog, Digital, and Power stages.

Digital bits such as miller capacitor, dead time delay cell, dead time fine_n cell, dead time fine_p cell, and the bias circuitry can fine-tune the circuits.
5.8.3 Packaging

The chip is packaged by a 56 pins QFN package for high-speed application. QFN package offers various benefits including reduced lead inductance, a small "near chip scale" footprint, thin profile, and reduced weight. It also uses perimeter I/O pads to relieve PCB trace routing, and the exposed copper die-pad technology provides excellent thermal and electrical performance. QFN packages also minimize the lead resistance and bond wire inductance, and simultaneously provide sufficient power dissipation capability. All of the above are reasons for selecting a QFN package here.

The pin description of the test chip is shown in Table 5-2. Figure5-26 is the bond diagram of the HFWB Buck Converter.
<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Description</th>
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<tbody>
<tr>
<td>bit 5</td>
<td>bias_circuit_trim_bit</td>
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<tr>
<td>p_miller_bit3</td>
<td>miller capacitor_tuning_bit</td>
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<td>p_miller_bit2</td>
<td>miller capacitor_tuning_bit</td>
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<td>bias_circuit_trim_bit</td>
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<td>bias_circuit_resistor</td>
</tr>
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<td>isenbot</td>
<td>bias_circuit_resistor</td>
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<td>eEnable_pulse</td>
</tr>
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<td>miller capacitor_tuning_bit</td>
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<td>control_ripple_voltage</td>
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<td>vn</td>
<td>DDA output</td>
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<td>bias_voltage_DDA__g_m__control_switch</td>
</tr>
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<td>analog VDD</td>
</tr>
<tr>
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<td>DDA Input_p1</td>
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<tr>
<td>input_n1</td>
<td>DDA Input_n1</td>
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<tr>
<td>vbias_30</td>
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<td>DDA Input_n2</td>
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<td>DDA Input_p2</td>
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<td>auxiliary_vdd</td>
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<td>deadtime_fine_n_bit</td>
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<td>fine_n_bit00</td>
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<td>top_switch_test_point</td>
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<tr>
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</tr>
<tr>
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<td>level_sifter_Supply_voltage</td>
</tr>
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<tr>
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<tr>
<td>deadtime_bit01</td>
<td>deadtime_trim_bit</td>
</tr>
<tr>
<td>deadtime_bit10</td>
<td>deadtime_trim_bit</td>
</tr>
<tr>
<td>deadtime_bit11</td>
<td>deadtime_trim_bit</td>
</tr>
<tr>
<td>fine_p_bit11</td>
<td>deadtime_fine_p_bit</td>
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<tr>
<td>fine_p_bit00</td>
<td>deadtime_fine_p_bit</td>
</tr>
</tbody>
</table>
5.8.4 Evaluation Board Design and Setup

Figure 5-29 is the test schematic and Figure 5-27 shows the evaluation board of the HFWB Buck Converter. Figure 5-28 is the functional block diagram of the chip. Regarding the board design, for safety, the wavelength in the media should be ten times longer than the trace. The decoupling capacitor design uses the principle of making the ac impedance (beyond the decoupling capacitor) equal to zero for power supply. The larger the size of the decoupling
capacitor, the further it is placed from the pin. This is because the larger decoupling capacitor handles the low frequency part of the impedance; when the frequency is low, the wavelength is large.

In Figure 5-27, it can be seen that the Vdd of the power stage is placed as close to the pin as possible. This is from the consideration of the parasitic inductance (not from that of parasitic resistance). The evaluation board is made of four layers. Traces on different layers should be made orthogonal to minimize the coupling parasitic capacitance.

From the nominal impedance point of view, \( Z_O \) is a function of width, height, and thickness for the micro-strip line. If \( Z_L = Z_O \), there is no reflection, regardless of the length of the trace. In the design, this translates to the switching frequency being taken as less than 10GHz and \( Z_O \) as resistive. This means that as long as \( Z_L = Z_O \), there is no reflection, which implies that the impedance remains always the same (if voltage does not change, current is a constant).

For this prototype chip, the gain-setting resistor of the DDA, the bias circuitry resistor, and the fixed on-time capacitor are surface mounted. For the future chip with full functionalities, they will all be integrated on silicon to reduce the cost and board area.
Figure 5-27 Evaluation Board of HFWB Buck Converter

Figure 5-28 Functional Blocks HFWB Buck Converter Chip
Figure 5-29 Test Schematic of HFWB Buck Converter
5.8.5 Measurement Result

Figure 5-31 shows the measurement results of the DDA.

Figure 5-31 Measurement Result of DDA (ps : CH1: Vout (input_p2), CH2: Vsen (input_n1), CH3: Vref(input_n2), CH4: DDA_Vout, Vref=0.522V(input_p1) , input_n1=0.594V Vout=3.02(input_p2), Input_n2=3V, DDA_Vout =3.21V)
In Figure 4-14 with the feedback network,

\[ V_{fb} = \frac{(DDA\_V_{out} - V_{out}) * R_1}{R_1 + R_2} + V_{out} \]

(5.2)

\[ V_{sen} = H * V_{out} \]

(5.3)

\[ H = \frac{R_{D2}}{R_{D2} + R_{D1}}, \quad K = \frac{R_2 + R_1}{R_1} \]

(5.4)

Where H and K are the divider gain and the DDA closed loop gain respectively.

The output of the DDA can be expressed as

\[ DDA\_V_{out} = -K * (H * V_{out} - V_{ref}) + V_{out} \]

(5.5)

This proves that the DDA is functional.

Eq.5.5 describes the relationship between the signals of the inputs and the output.

Figure5-32 shows that the proposed HFWB buck converter is functional. The yellow curve denotes \( V_{out} \) and the pink curve, the DDA output. From Eq.5.5, it can be inferred that, if the gain of the DDA were sufficiently large, subsequently it would turn DDA output in the opposite direction of \( V_{out} \).
Figure 5-32 Measurement Result of DDA

Figure 5-33 Measured Waveform of the Vref, Vout, Inductor Current Ripple and Switching Nodes Waveform with 200 KHz
Figure 5-33 demonstrates that the waveform of the designed HFWB buck converter follows closely a fast envelope signal of 200 KHz, which has a swing of more than 2 V_{pp}. The inductor current ripple curve is in blue color and the test point curve of the switching mode is in pink. It can be observed that the switching frequency varies. Hypothetically, the inductor current ripple (blue curve) must compare with the brown curve at the bottom of the blue curve waveform. When the sinusoidal signal swings upward, the switching frequency increases as shown in Eq.4.1. The switching frequency of the buck converter is at most 30MHz, which is beyond the delay budget of 15 – 20 ns. Therefore, it can be seen that the brown curve was not compared with the bottom of the inductor current signal (blue curve). Nevertheless, the modulator followed closely the reference signal. More importantly, the switching frequency has been distributed.
This can be observed clearly in Figure 5-34, because of the delay budget. The modulator follows the signals faithfully when the $V_{pp}$ amplitude varies in the range 1-3 V. Yet as the $V_{pp}$ amplitude of the reference signal increases, at the top portion of the sinusoidal waveform, the blue curve inductor waveform starts shifting below the brown curve. This is because of increasing switching frequency.
Figure 5-35 Measurement of the Vout, Vref, Inductor Current Ripple and Switching Node Waveform with Different Sinusoidal Reference Vref with Amp =3V Vapp (a) Vref = 1KHz (b) Vref = 10 KHz (c) Vref = 40KHz Amp = 4V (d) Vref = 100KHz

In Figure 5-35, the modulator was able to follow the envelope signal while the frequency varies from 1 KHz to 100 KHz. In Figure 5-35(c), it can be seen that at the bottom portion of the green colored curve, the ripple is more obvious. The Output voltage is a function of frequency. The bottom portion of the green curve has the lowest switching frequency. When frequency is lower, the ripple is more obvious, especially when the voltage swing is large. The $V_{pp}$ amplitude in Figure 5-35 (c) is 4V.
In Figure 5-36, the reference signal is a periodic triangle wave. The Triangle wave contains only odd harmonics. However, the higher harmonics roll off much faster than in a square wave. It is possible to approximate a triangle wave with additive synthesis by adding odd harmonics of the fundamental, multiplying every \((4n-1)\)th harmonic by \(-1\) (or changing its phase by \(\pi\)), and rolling off the harmonics by the inverse square of their relative frequency to the fundamental. The Fourier series of a triangle wave can be expressed as Eq.5.6.

\[
x_{\text{triangle}}(t) = \frac{8}{\pi^2} \sum_{k=0}^{\infty} (-1)^k \frac{\sin((2k+1)wt)}{(2k+1)^2} = \frac{8}{\pi^2} \left[ \sin(wt) - \frac{1}{9} \sin(3wt) + \frac{1}{25} \sin(5wt) - \ldots \right]
\]

(5.6)
As can be observed in Eq. 5.6, the triangle wave contains all high frequency terms, therefore, the distortion can be observed at the following waveform. It indicates a lack of bandwidth.

![Graph showing comparison between with and without ripple cancellation]

**Figure 5.37** Vref With and Without Switching Ripple Cancellation Technique for 100Hz Sinusoidal Input Signal

Figure 5.37 shows the result of comparison measurement with and without ripple cancellation branch. The reference is a 100Hz sinusoidal wave with amplitude $2 \ V_{pp}$. It can be observed that the output ripple is greatly reduced from 1.2V to 200 mV. It is also observed that the bottom of the red wave has a larger ripple compared to top of the red wave.
Figure 5-38 Without Switching Ripple Cancellation Technique Output Spectrum for 100 KHz Amp 3V Vpp Sinusoidal Input Signal

In Figure 5-38, a 100 KHz sinusoidal wave with amplitude 3Vpp is followed. The switching ripple cancellation was not applied. In the frequency spectrum, it can be observed that the switching frequencies were concentrated at two ranges: 24–26 MHz and 29–31 MHz. Switching frequency was not being concentrated at a particular frequency; also, harmonic terms were not observed in the spectrum. This proves the theory. Compared to Figure 5-39 [7] & Figure 5-40 [55], it can be inferred that the variable switching frequency control scheme has a superior noise performance and outperforms even without an auxiliary branch.
Figure 5-39 Frequency Spectrum of a 10MHz Fully Differential High Frequency Class D Modulator [7]

Figure 5-40 Spectrum Plot of a 10MHz Current Mode 4 Switch Buck Boost Converter (4SBBC) for Polar Modulation [51]
Chapter 6 Power Efficiency Improvement for Light Load for HFWB Buck Converter for Wireless Communication Application

As Chapter 1 mentions, the cellular phone industry has a trend towards demand for speed. Because of this, integrated circuits have a high switching frequency as the key design parameter, another reason being that it (high switching frequency) enables full integration of active and passive devices. This chapter discusses the loss mechanism of the HFWB buck converter. It also proposes the realization of device segmentation technique for wireless communication applications to enhance the efficiency of HFWB buck converter over a wide load range.

6.1 Loss Breakdown in HFWB Buck Converter

There are many factors that can affect power efficiency. Gate drive tapering factors, voltage swings, ratio of the power MOSFET, and shoot through current are some of them. Typically, the power consumed by the pulse width modulation feedback circuit is small. At high switching frequencies, the energy dissipation occurs mainly in the Power MOSFET and its gate drives. If the feedback circuit loss is neglected, the loss can be broken down into dynamic switching loss, gate drive loss, and the conduction loss as shown below. [50]
\[ P_{P \text{TOTAL}} = \frac{R_{0PMOS}}{W_{P1}} i_{rms}^{2} PMOS + W_{P1} E_{P\text{TOTALswitc \_hing}} f_s \] 

(6.1)

where \( P_{P \text{TOTAL}} \) is the total power dissipation related to P1 (Power MOSFET).

\[ P_{N \text{TOTAL}} = \frac{R_{0NMOS}}{W_{N1}} i_{rms}^{2} PMOS + W_{N1} E_{N\text{TOTALswitc \_hing}} f_s \] 

(6.2)

where \( P_{N \text{TOTAL}} \) is the total power dissipation related to N1 (Power MOSFET).

\[ E_{PMOS\text{driver}} E_{NMOS\text{driver}} \] denote power dissipated in the drivers of P1 and N1, respectively.

\[ E_{P1} E_{N1} \] denote the dynamic switching loss in P Power MOSFET and N Power MOSFET respectively.

\[ E_{P\text{TOTALswitc \_hing}} = E_{P1} + E_{PMOS\text{drivers}} \] 

(6.3)

where \( E_{P\text{TOTALswitc \_hing}} \) is the total switching power dissipation related to P1.

\[ E_{N\text{TOTALswitc \_hing}} = E_{N1} + E_{NMOS\text{drivers}} \] 

(6.4)

where \( E_{N\text{TOTALswitc \_hing}} \) is the total switching power dissipation related to N1.

\[ E_{PMOS\text{driver}} \approx \frac{1}{ap-b-1} (bC_{0PMOS} + C_{0NMOS}) (V_{DD} - V_{gs})^{2} \] 

(6.5)
\[ E_{\text{NMOSdrivers}} \equiv \frac{1}{ap - b - 1}(bC_{0\text{PMOS}} + C_{0\text{NMOS}})(V_{g})^2 \]

\[(6.6)\]

\[ E_{P1} = \{(C_{0\text{PMOS}} + C_{0\text{PMOS}})(V_{DD1} - V_{gs})^2 + 2C_{gdo\text{PMOS}}(-V_{DD1}V_{gs} + V_{DD1}^2 + \frac{V_{gs}^2}{2}) + C_{db0\text{PMOS}}V_{DD1}^2 \} \]

\[(6.7)\]

\[ E_{N1} = \{(C_{0\text{NMOS}} + C_{0\text{NMOS}} + C_{gdo\text{NMOS}})(V_{gs}V_{gs})^2 + (C_{gdo\text{PMOS}} + C_{db0\text{NMOS}})V_{DD1}^2 \} \]

\[(6.8)\]

\[ C_{o0}, \ C_{g0}, \ C_{gd0}, \ \text{and} \ C_{db0} \ \text{denote the gate oxide, gate-to-source overlap, gate-to-drain overlap, and the drain-to-body junction capacitances respectively.} \]

\[ C_{0\text{PMOS}} = C_{o\text{PMOS}} + 2C_{gdo\text{PMOS}} + C_{gso\text{PMOS}} + C_{db0\text{PMOS}} \]

\[(6.9)\]

\[ C_{0\text{NMOS}} = C_{o\text{NMOS}} + 2C_{gdo\text{NMOS}} + C_{gso\text{NMOS}} + C_{db0\text{NMOS}} \]

\[(6.10)\]

As given by (6.1) and (6.2), because of the combination of conduction losses (caused by parasitic resistive impedance) and switching loss (caused by parasitic capacitive impedance), the conduction power is dissipated in the series resistance when the transistors operating at the active region. Dynamic power is dissipated in each switching cycle while charging/discharging the gate oxide, gate to source/drain overlap, and drain to body junction capacitance of the MOSFETs. Increasing the MOSFET transistor width reduces the
conduction losses, but increases the switching losses. The optimum width[50] for MOSFET is shown below:

\[ W_{N_{opt}} = \sqrt{\frac{R_{0_{NMOS}}}{f_s E_{N_{TOTAL}}}} \frac{i_{ms_{NMOS}}^2}{\text{hing}} \]  
(6.11)

\[ W_{P_{opt}} = \sqrt{\frac{R_{0_{PMOS}}}{f_s E_{P_{TOTAL}}}} \frac{i_{ms_{PMOS}}^2}{\text{hing}} \]  
(6.12)

### 6.2 Device Segmentation Technique in wireless communication application

Figure 1-2 displays the output power vs. power distribution function of a typical CDMA cellular phone (output power refers to the output port of the PA). The average value of the output power level is 30 dBm below its maximum value. Therefore, RF PA employs more than one operating mode with different bias points to save DC power consumption. Moreover, saving the DC power consumption extends connection time.

Table 6-1 displays the load efficiency of the HFWB buck converter and the system power breakdown over the load. It can be observed that at full load (750mA), it has the best efficiency of 82%. Efficiency is designed at the point where switching loss is equivalent to conduction loss (as the previous section concluded). When load decreases, efficiency drops.
The switching loss becomes significant as shown in Eq. 6.3 & 6.4 and is mainly dominated. Improving efficiency at light loads is very important when the HFWB buck converter needs to work over a very wide load range for multi-operating-mode RF PA[5]. According to the gate driving loss equations Eq6.3 & 6.4, there are several methods to reduce the gate driver loss. Device Segmentation[52] is adopted in this design to improve efficiency over light loads along with multi-mode operating RFPA.

### Table 6-1 HFWB Buck System Loss Breakdown over Load Condition

<table>
<thead>
<tr>
<th>Load current</th>
<th>Output resistance</th>
<th>vout (V)</th>
<th>auxiliary</th>
<th>analog vdd55</th>
<th>digital vdd55</th>
<th>digital vdd30</th>
<th>analog vdd30</th>
<th>vdd25</th>
<th>vdd15</th>
<th>vin</th>
<th>efficiency (%)</th>
<th>switching freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.272</td>
<td>1ohm</td>
<td>0.875</td>
<td>-0.06824</td>
<td>-0.0133</td>
<td>-1.13</td>
<td>-0.0166</td>
<td>-0.001857</td>
<td>-0.006645</td>
<td>0.010902</td>
<td>-1.26743</td>
<td>0.687879</td>
<td>9.6MHz~19MHz</td>
</tr>
<tr>
<td>0.136</td>
<td>2.2ohm</td>
<td>0.442</td>
<td>-0.09492</td>
<td>-0.01339</td>
<td>-0.070395</td>
<td>-0.01581</td>
<td>-0.001857</td>
<td>-0.006404</td>
<td>0.010903</td>
<td>-0.62732</td>
<td>0.534255</td>
<td>9.6MHz~19MHz</td>
</tr>
<tr>
<td>0.063</td>
<td>4.4ohm</td>
<td>0.211</td>
<td>-0.03114</td>
<td>-0.01341</td>
<td>-0.54046</td>
<td>-0.01566</td>
<td>-0.001857</td>
<td>-0.006401</td>
<td>0.010936</td>
<td>-0.63999</td>
<td>0.32185</td>
<td>9.6MHz~19MHz</td>
</tr>
<tr>
<td>0.038</td>
<td>100ohm</td>
<td>0.098</td>
<td>-0.07159</td>
<td>-0.01341</td>
<td>-0.373</td>
<td>-0.01586</td>
<td>-0.001857</td>
<td>-0.006479</td>
<td>0.010917</td>
<td>-0.47988</td>
<td>0.204559</td>
<td>9.6MHz~19MHz</td>
</tr>
<tr>
<td>0.015</td>
<td>200ohm</td>
<td>0.049</td>
<td>-0.03785</td>
<td>-0.01341</td>
<td>-0.36</td>
<td>-0.01571</td>
<td>-0.001879</td>
<td>-0.006469</td>
<td>0.010906</td>
<td>-0.46226</td>
<td>0.106001</td>
<td>9.6MHz~19MHz</td>
</tr>
</tbody>
</table>

### 6.2.1 Active Filter

An active filter is a type of analog electronic filter that uses active components, such as amplifiers. Amplifiers when included in the design can improve performance and predictability of filters. Amplifiers eliminate the need for inductors, which are normally more expensive components. Furthermore, amplifiers prevent load impedance of the succeeding stage from affecting the characteristics of the filter.

An active filter could have complex poles and zeros without having a large or expensive inductor. The shape of the response, the Q (quality factor), and the tuned frequency can be set with inexpensive variable resistors.

However, using active elements has these limitations:
- The limitation of the bandwidth of amplifiers, which is not included in the filter design equations
- Because of the bandwidths limitation, it is not suitable for high frequency application.
- Active filter can possibly create extra noise in the system

6.2.2 Lossless Inductor Current Sensing

To sense the continuous current information, the ‘Lossless-current-sensing[53]’ technique is used. This technique uses an RC network \((R_{\text{sense}}, C_{\text{sense}})\) to filter the voltage across the inductor. It senses the current through the equivalent series resistance \(R_{\text{DCR}}\) of the inductor \(L\) (Figure 6-1).
The design equation [53] of the sensing network can be expressed as follows:

\[ V_{C_{sense}} = V_{sense} = I_L \cdot R_{DCR} \]

(6.13)

\[ \frac{L}{R_{DCR}} = \frac{R_{sense} \cdot C_{sense}}{} \]

(6.14)
Figure 6-1 shows an HFWB buck converter with device segmentation. It has the following loops of current sensing:

- A fast current sensing to compare with the error signal coming from the DDA to realize the hysteretic fixed on-time control scheme based on inductor current
- A slow current sensing to obtain the inductor current information to improve the efficiency at light loads

The CDMA signal has high voltage swing. Figure 5.22 shows that the swing at the output has amplitude $V_{pp}$ of 4V. To sense the differential voltage across $c_{sense}$ with such a wide common mode voltage change, the input stage of the analog adder should cover the rail-to-rail common mode range.

There are various ways to implement a Differential Difference Amplifier. A brief illustration is shown below. Figure 6-2 shows how to realize an analog adder with different connections. Using the connection as Figure 6-2(a) shows, $V_{out}$ becomes equivalent to the product of multiplication of differential voltage and non-inverting gain. Using the connection as shown in Figure 6-2(b), $V_{out}$ becomes equivalent to the differential voltage. Figure 6-2(c) shows a resistless gain of two. Figure 6-2(d) shows a differential voltage with a gain of one.

The Analog adder and the Butterworth filter do not require a large bandwidth because of the slow step change and because of the obtaining load current being in DC. This eases the difficulties in designing the analog blocks.
6.2.3 Simulation Result of Device Segmentation

Figure 6-3 shows that at 20us, the load ($I_{T}/V_{82}$) suddenly steps steeply down from 750mA to 125mA. The sensed differential capacitor voltage ($VT''/filter''$) also changes accordingly. The output voltage ($VT''/vout''$) remains regulated at 3V with amplitude of 2$V_{pp}$. Magnifying the outlined part of Figure 6-3 shows that it has an adequate transient response as the load steps down. It can be seen that the sensed differential capacitor voltage ($VT''/filter''$) is distorted because of the designed small bandwidth of the Analog adder. However, it does not affect the DC sensing signal ($VT''/output_active_filter''$), which was stepping down when step down load transient occurs, as Figure 6-4 shows.
Figure 6-3 Step Down Key Waveform-1
(VT''/output_active_filter") is the output of the active filter. It filters out the high frequency information and retains only the DC information of the load, changing from 3.17V down to 3.07V. Figure 6-4 shows that the responding step change occurring at 210µs (VT''/I0/decision_2''), changes from 5 to 0 V going into the Mode Decision and Driver Sequence Generator block. Figure 6-5 shows the gate drive signals corresponding to (VT''/I0/decision_2''). Based on Eq.6.3 & 6.4, to save the power at light load, C_{ox}, C_{gs}, C_{gd}, and C_{db} need to be reduced. Accordingly, the signal from the “Mode Decision and Driver Sequence Generator” shuts down part of the power stage, based on the load condition that the active filter provides. Figure 6-5 shows that the slave Power MOSFETs remain operating throughout the load condition while the master Power MOSFETs shut down during the light load.
Figure 6-5 Step Down Key Waveform -3

Figure 6-6 Step Down Key Waveform -4

Figure 6-6 shows the low voltage swing of the POWER MOSFET. The NMOSFET swings from 0V to 2.5V and PMOSFET swings from 5V to 1.5V. It can also be observed that there is a dead time generated to avoid shoot-through current. PMOSFET turns off before
NMOSFET turns on; later NMOSFET turns off before PMOSFET turns on again. Figure 6-7 is the load efficiency curve. It shows that by turning off 80% of the power stage at light load, (that is, POWER stage size reduced from 20mm to 4mm), the efficiency can be improved by 7%.

![Figure 6-7 HFWB Buck Converter Load Efficiency Curve](image)

### 6.3 Summary

This chapter introduces the device segmentation technique and demonstrates how it can be applied to an amplitude phase separation scheme for wireless communication. Because of the use of RFPA, amplitude-phase separation schemes normally have various operating modes to save DC power consumption. With the device segmentation technique, the parasitic...
capacitance reduces, resulting in power savings of up to 7% at light loads shown in Cadence preliminary result.
Chapter 7 Scope of Future Work

7.1 Complete System Level Demonstration with RF PA in Discrete version

A high-speed synchronized buck for envelope tracking transmitter architecture is designed, measured, and thoroughly derived in this thesis. It is proven that the switching noise is spread out. However, the system level discrete hardware demonstration (including the integrated class D modulator and external RF PA) is yet to be established.

7.2 Implement a Two Stage Envelope Tracking Structure for CDMA Wireless Communication Applications

The input to the envelope tracking modulator is connected to a lithium ion battery, which is the only power source of the handheld device. The voltage can range from 2.7V to 4.2V based on the charge status of the battery.

For portable applications, compactness and high efficiency are critically important. Currently, Inductor-based converters and charge pump regulators are the main architectures of DC-DC converters for boosting the voltage. For low power driven, highly integrated electronic systems, size is always a concern. This is particularly true while using inductor-based converters (because of their large inductors). The charge pump regulator is popular for its compact size because it avoids the large and expensive magnetic components; also because of the absence of EMI noise from the inductor.
For the above reason, the charge pump circuit is a better candidate for the DC-DC stage in a handheld device. The output of the modulator should follow the fast changing CDMA reference signal. The reference signal changes from 1V to 5V. In order to provide a steady 5V voltage for the following power stage and to improve the efficiency, a two-stage envelope tracking structure is proposed. This two-stage architecture would make the whole converter a sound tracking structure for portable devices. The converter has a multi-mode charge pump as the first stage and a synchronized buck converter as the second stage.
References


