Abstract

CANCHEEVARAM, JAI   KUMARAN KUPPUSWAMY

Design and Performance Characterization of a Test System for Microprocessor Hot Spot Cooling using Thin-film Superlattice Thermoelectrics

(Under the direction of Dr. Winser E. Alexander)

The constant need for higher performance, increased levels of functional integration, as well as die size optimization has led to preferential clustering of higher power units on microprocessors. This causes higher heat flux concentrations in certain areas of the die and lower heat fluxes in certain other regions, which manifest themselves as large temperature gradients on the die surface. These local power densities are commonly referred to as “hot spots”. The thermal cooling solution provided must effectively ensure that junction/die temperatures on the processor do not exceed the rated 90-110 °C range to guarantee device performance and reliability.

The focus of this work is to present Thin-film Superlattice Thermoelectrics [TFST] as an excellent solution for microprocessor die hot spot cooling. TFSTs have measured Figure of Merit [ZT] values of ~2.4 at 300K for p-type superlattices, with potential to pump heat flux of up to 700Wcm⁻². Furthermore, these devices have fast response times, which makes them achieve steady state cooling in 15µs. This is vital in preventing thermal runaway and subsequent failure of microprocessors during rapid load transients.

The primary contribution of this thesis is a test setup and experimental procedure, for characterization of an integrated TFST-processor system. First I identified and isolated the potential hot spot on the processor using infrared (IR) images of the die during operation. The IR images were conclusive in determining the area of the hot spot and its magnitudes in terms of maximum temperatures reached. Next I calculated the
power dissipated by the processor on the basis of the heat absorbed by the cooling system. This involved building a calorimetric system, which cools the processor by circulating water. The system was calibrated with a known load and found to measure within $\pm 3$ watts of the actual power dissipated, for a processor thermal design power of 30 watts. Using this system, calculations of heat dissipated by the processor under both normal clocking and over clocking cases are presented.

The final step in integrating the TFST with the processor involved mounting the TFST module onto the processor hot spot and ensuring safe operation. The TFST module itself was powered by a custom-modified Howland current source circuit, which regulated the amount of cooling. Further contributions of this thesis include evaluating the efficiency of the TFST and the resulting impact on microprocessor performance and reliability. The temperature at the interface of the TFST module and the hot spot was monitored during several stages of CPU operation. Thermal transients at the hot spot, presented in the results, show that active heat spreading using TFST significantly reduces the thermal cooling budget and alleviates constraints on the cooling solution. In the future, with more efficient TFST modules with higher ZT values, these hot spots may be completely eliminated.
Design and Performance Characterization of a Test System for Microprocessor Hot Spot Cooling using Thin-film Superlattice Thermoelectrics

By

Jai Kumaran Kuppuswamy Cancheevaram

A thesis submitted to the graduate faculty of North Carolina State University In partial fulfillment of the requirements of the degree of Master of Science

COMPUTER ENGINEERING

Raleigh

2003

Approved by

_________________________________________

Dr. Winser E. Alexander, Chair of the Advisory Committee

____________________  ________________________

Dr. John F. Muth        Dr. Ronald O. Scattergood
BIOGRAPHY

Jai Kumaran K. Cancheevaram was born on 14th of February 1980 in the city of Chennai, India. In 2001, he graduated with a B.E (Honors) degree in Electrical and Electronics Engineering from the University of Madras, Tamilnadu, India.

He was an intern with the Research and Development Division of TVS Electronics, Chennai, India from August 2000 to May 2001. In the fall of 2001, he enrolled in the Masters program in Computer Engineering (CpE) at North Carolina State University, Raleigh. He has also been functioning as a Co-operative Research Assistant at the Center for Thermoelectrics [CTR], Research Triangle Institute, Raleigh from June 2002 to July 2003.

He has been working under the guidance of Dr. Winser Alexander and Dr. Rama Venkatasubramanian from June 2002 to present, in the field of microprocessor thermal management using Thin-Film Superlattice Thermoelectrics. This thesis is a result of the work done since June 2002.
Acknowledgements

At the outset, I would like to thank my parents Kuppuswamy and Rajeswari and my brother Saravanan for their immense support and affection. I’m greatly indebted to them and cannot in any measure repay all that they have done for me.

I would like to thank my graduate adviser Dr. Winser Alexander. He is a fantastic teacher who exhibits lots of patience and understanding in his interactions with students. During the course of this work, I have benefited immensely from his knowledge and experience. The completion of this thesis is vastly due to his guidance and help during several critical junctures.

I would like to thank Dr. Rama Venkatasubramanian, Director at the Center for Thermoelectric Research, Research Triangle Institute. His dedication to his work and his ability to perpetually extract the best out of himself and also the people whom he works with has to be seen to believe. He has provided me with a rare opportunity to work with eminent scholars and converse in scientific circles.

I also thank Dr. John F. Muth and Dr. Ronald O. Scattergood for having agreed to be on my Graduate Advisory Committee. Their enthusiasm for my work was very encouraging and their suggestions on reviewing my thesis were invaluable.

Sincere appreciation is due to Randall Alley, Research Engineer, RTI. I have been an apprentice under his guidance during the past year. He has directed me towards results and scientific enquiries, which have culminated into this thesis. Edward Siivola, Testing Engineer, RTI deserves very special thanks for his immeasurable help and dexterity in the mounting and testing phase of the thin-film module.

I would like to thank the other members of my group for their support during the course of this work - Brooks ‘O Quinn for his constant help in multiple disciplines. Dr. Mary Napier for generously sharing her Lab space, Dr. Anil Reddy, Brent Ward, Kip Coonley and Dr John Posthill for their help and suggestions in completion of the thesis
document and Ryan Wiitala for his help with the ZT measurements. I also thank Pratima Adepalli, Mike Puchan, Geza Deszi, Tom Colpitts, Paul Crocco and Cherie Warren for their constant support and encouragement. Their critical comments have resulted in a more definitive and complete work. Special thanks to Mike Mantini, Dean Brooks and Bob Hendry in agreeing to help out a guy with two left hands when it comes to machining.

My roommates Srivatsan Ravindran, Sajjan Raghavan, Mohammad Ahraf, Pradeep Mahadevan and Vinay Chandrasekhar have been of great help. They were very understanding to my odd working hours and constant bickering when deadlines approach. They have eased the effort in the completion of this work in very short duration. Aravindh Anantaraman deserves a special mention for his guidance thorough the annals of computer architecture. He along with Vishwanath Sunderaraman and Lashminarayan Venkatesan have been stern, yet supportive during several moments when I have been frivolous with time.

I would like to thank Karthikeyan Loganathan, Deepak Shanmugasundaram, Vinodha Sadasivam, Deepa Ponappan, Anand Sivaraman, and Raghunath Subramanian, for having put up with my antics and for providing me with much needed breaks. Friends who have helped me in numerous ways include Karthikeyan Santhanagopalan, Manukaran Karunakaran, Arianathan Rajagopal, Patrick Hamilton, Yogesh Ramadoss, Deepak Thirumalai, Karthik Chandrasekar and Bhavesh Sampath. I thank them all for their support.

I would also like to thanks the members of the NCSU Cricket Team- Nagendra, Anirudh, Rupali, Nihar, Susheel, Krishna, Sattanathan, Salman and Vishal for their constant encouragement. My association with them and the multiple experiences both on and off field has demonstrated to me, the success that is teamwork.
Table of Contents

List of Figures ................................................................................................................... vii
List of Tables ................................................................................................................... viii
List of Equations ............................................................................................................ ix
List of Symbols ................................................................................................................ x
Glossary of Important Terms [16] ................................................................................... xii

Chapter 1 Introduction..................................................................................................... 1
  1.1 Foreword ............................................................................................................. 1
  1.2 Amount of Heat Transferred from Heat sink ...................................................... 2
    1.2.1 Increasing Surface area of Heat Sink .......................................................... 2
    1.2.2 Forced Convection Airflow ........................................................................ 2
    1.2.3 Acoustics..................................................................................................... 3
    1.2.4 Heat Sink Temperature ............................................................................... 3
    1.2.5 Heat Spreading............................................................................................ 3
  1.3 Alternate Cooling Solutions................................................................................ 4
    1.3.1 Circulated Liquid Cooling and Refrigeration [11]...................................... 4
    1.3.2 Thermoelectrics........................................................................................... 4
  1.4 Thesis Highlights and Contributions .................................................................. 6
  1.5 Thesis Organization ............................................................................................ 6

Chapter 2 Related Work .................................................................................................. 7
  2.1 Chapter 2 Introduction ........................................................................................ 7
  2.2 Analysis of Pentium III Architecture.................................................................. 7
    2.2.1 Architectural Blocks, Description and Function......................................... 8
  2.3 Potential Hot-Spot Locations in Pentium III die............................................... 12
    2.3.1 Infrared Image of Processor die during Startup........................................ 12
    2.3.2 Infrared Image of Processor during Application Load ............................. 13
  2.4 Introduction to Thermoelectrics........................................................................ 14
  2.5 Thermoelectric Effects...................................................................................... 14
  2.6 Peltier Modules ................................................................................................. 17
  2.7 Thermal Parameters and Equations .................................................................. 18
  2.8 Thermoelectricity Theory of Solids.................................................................. 22
    2.8.1 Origin of Charge Carriers ......................................................................... 22
    2.8.2 Mass Spring Model ................................................................................... 23
    2.8.3 Phonons..................................................................................................... 24
    2.8.4 Phonon Scattering Mechanism to Lower Thermal Conductivity ............. 25
  2.9 RTI Thin-film Thermoelectrics......................................................................... 27
    2.9.1 Lattice Thermal Conductivity Reduction in Superlattice Structures ....... 28
    2.9.2 Mean Free Path Reduction........................................................................ 29
    2.9.3 Thermoelectric devices for Localized, Rapid Cooling ......................... 32
  2.10 Summary ........................................................................................................... 35

Chapter 3 Experimental Setup....................................................................................... 36
  3.1 Chapter 3 Introduction ...................................................................................... 36
  3.2 Simulated Aluminum Block 50Watt Load ....................................................... 37
  3.3 Processor Cooling with Independent Peltier Module ....................................... 39
  3.4 Hot Spot Cooling using Integrated TFST Module .......................................... 40
List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Bulk and Thin-film comparison</td>
<td>5</td>
</tr>
<tr>
<td>2-2</td>
<td>IR image of processor die during startup [RTI]</td>
<td>12</td>
</tr>
<tr>
<td>2-3</td>
<td>IR image of processor while loading an application [RTI]</td>
<td>13</td>
</tr>
<tr>
<td>2-4</td>
<td>Cross-section of typical thermoelectric couple [4]</td>
<td>15</td>
</tr>
<tr>
<td>2-5</td>
<td>Basic Thermocouple [6]</td>
<td>16</td>
</tr>
<tr>
<td>2-6</td>
<td>Peltier Coefficient [6]</td>
<td>16</td>
</tr>
<tr>
<td>2-7</td>
<td>Thomson Coefficient [6]</td>
<td>16</td>
</tr>
<tr>
<td>2-8</td>
<td>Peltier Module and its mechanism of heat transfer</td>
<td>18</td>
</tr>
<tr>
<td>2-9</td>
<td>Lattice showing atomic substitutions [9]</td>
<td>23</td>
</tr>
<tr>
<td>2-10</td>
<td>Mass spring model of crystal [9]</td>
<td>24</td>
</tr>
<tr>
<td>2-11</td>
<td>Lattice thermal conductivity and Average phonon mean free path (lmfp) Vs Superlattice period [2]</td>
<td>29</td>
</tr>
<tr>
<td>2-12</td>
<td>Wave reflection at interface of Superlattice [10]</td>
<td>30</td>
</tr>
<tr>
<td>2-13</td>
<td>Low-frequency cut-off wavelength Vs Superlattice period [2]</td>
<td>31</td>
</tr>
<tr>
<td>2-14</td>
<td>Absolute cooling Vs Current [2]</td>
<td>32</td>
</tr>
<tr>
<td>2-15</td>
<td>Current Vs Cooling power density [2]</td>
<td>33</td>
</tr>
<tr>
<td>2-16</td>
<td>Potential COP Vs ZT for various technologies [2]</td>
<td>33</td>
</tr>
<tr>
<td>2-17</td>
<td>Comparison of cooling time response of bulk and thin-film [2]</td>
<td>34</td>
</tr>
<tr>
<td>3-1</td>
<td>50-watt aluminum load setup</td>
<td>38</td>
</tr>
<tr>
<td>3-2</td>
<td>Final setup block diagram</td>
<td>41</td>
</tr>
<tr>
<td>3-3</td>
<td>PCB for Powering TFST module</td>
<td>44</td>
</tr>
<tr>
<td>3-4</td>
<td>TFST module mounted onto Copper block</td>
<td>46</td>
</tr>
<tr>
<td>4-1</td>
<td>Front Panel of Thermocouple Reader with SCXI-1112</td>
<td>50</td>
</tr>
<tr>
<td>4-2</td>
<td>Block diagram of Thermocouple Reader with SCXI-1112</td>
<td>53</td>
</tr>
<tr>
<td>4-3</td>
<td>Front Panel of Read data and write onto a spreadsheet. Vi</td>
<td>57</td>
</tr>
<tr>
<td>4-4</td>
<td>Block diagram of Read data and write onto a spreadsheet. Vi</td>
<td>59</td>
</tr>
<tr>
<td>5-1</td>
<td>Combined plot of CPU temperatures as a function of time for varying frequencies</td>
<td>62</td>
</tr>
<tr>
<td>5-2</td>
<td>Normal processor clocking on-die and interface temperatures</td>
<td>63</td>
</tr>
<tr>
<td>5-3</td>
<td>Schematic of convectional cooling extension using TEC</td>
<td>64</td>
</tr>
<tr>
<td>5-4</td>
<td>TEC input Power VS Delta T across TEC</td>
<td>66</td>
</tr>
<tr>
<td>5-5</td>
<td>Aluminum block load Vs. Delta T</td>
<td>67</td>
</tr>
<tr>
<td>5-6</td>
<td>Delta T across water Vs Total power dissipated</td>
<td>68</td>
</tr>
<tr>
<td>5-7</td>
<td>COP and Power of TEC Vs Input load</td>
<td>68</td>
</tr>
<tr>
<td>5-8</td>
<td>Processor on-die temperature Vs TEC input power (normal clocking)</td>
<td>71</td>
</tr>
<tr>
<td>5-9</td>
<td>Processor power calculated vs TEC input power (normal clocking)</td>
<td>72</td>
</tr>
<tr>
<td>5-10</td>
<td>Processor on-die temperature Vs TEC input power (over clocking)</td>
<td>73</td>
</tr>
<tr>
<td>5-11</td>
<td>Processor power calculated Vs TEC input power (over clocking)</td>
<td>75</td>
</tr>
</tbody>
</table>
List of Tables

Table 1. Measured values from simulated load tests ........................................................ 65
Table 2. Calculated values from simulated load tests ....................................................... 69
Table 3. Measured values under processor normal clocking case .................................... 70
Table 4. Calculated values under processor normal clocking case ................................... 71
Table 5. Measured values under processor over clocking case ....................................... 73
Table 6. Calculated values under processor over clocking case ...................................... 74
Table 7. TFST module testing results ........................................................................... 75
List of Equations

Equation 1-1. Heat Dissipated by Heat sink [18] ............................................................... 2
Equation 2-1. Seebeck Coefficient [6].............................................................................. 16
Equation 2-2. Kelvin Relation 1 [6].................................................................................. 17
Equation 2-3. Kelvin Relation 2 [6]................................................................................. 17
Equation 2-4. Hot side temperature of Thermoelectric [8]............................................... 19
Equation 2-5. Heat released to the hot side [8]................................................................ 19
Equation 2-6 Temperature difference across thermoelectric [7]................................. 20
Equation 2-7. Figure of merit of Thermoelectric [2]......................................................... 20
Equation 2-10. Heat Pumping Capacity of Thermoelectric [8]........................................ 21
Equation 2-12 Coefficient of performance [8]............................................................... 22
Equation 2-13. Mean free path, Lattice thermal conductivity equation [10].................... 30
Equation 2-14. Maximum heat pumping capacity of thermoelectric couple [2].......... 32
Equation 3-1. Voltage output from Op-Amp..................................................................... 43
Equation 3-2. Current through Sense Resistor.................................................................. 43
Equation 3-3. Current in terms of Vin .............................................................................. 43
Equation 4-1. SCXI Temperature Sensor String Syntax ................................................. 49
Equation 5-1. Heat drawn by coolant water................................................................. 66
List of Symbols

- $Z$ = material coefficient of Thermoelectric $\text{deg}^{-1}$ ($^\circ\text{C}^{-1}$)
- $\alpha = \text{Seebeck Coefficient}$ volts/deg ($V/^\circ\text{C}$)
- $I = \text{Current}$ Amps (A)
- $\Pi = \text{Peltier coefficient}$ volts (V)
- $\zeta = \text{Thompson coefficient}$ deg ($^\circ\text{C}$)
- $T_h = \text{Hot surface temperature}$ deg ($^\circ\text{C}$)
- $T_c = \text{Cold surface temperature}$ deg ($^\circ\text{C}$)
- $Q_h = \text{Heat released to the hot side of the thermoelectric}$ watts (W)
- $Q_c = \text{Heat absorbed from the cold side}$ watts (W)
- $P_{in} = \text{Electrical input power to the thermoelectric}$ watts (W)
- $\theta = \text{Thermal resistance of heat exchanger}$ deg/watts ($^\circ\text{C}/\text{W}$)
- $\Delta T = \text{Temperature difference across thermoelectric}$ deg ($^\circ\text{C}$)
- $T = \text{Absolute temperature}$ Kelvin ($^\circ\text{K}$)
- $\rho = \text{Electrical resistivity}$ ohm-cm ($\Omega\text{-cm}$)
- $K_T = \text{Total thermal conductivity}$ watt/cm-deg ($\text{W/cm}^{-\circ\text{C}}$)
- $K_L = \text{Lattice thermal conductivity}$ watt/cm-Kelvin ($\text{W/cm}^{-\circ\text{K}}$)
- $K_e = \text{Electronic thermal conductivity}$ watt/cm-Kelvin ($\text{W/cm}^{-\circ\text{K}}$)
- $\mu = \text{Carrier mobility}$ cm$^2$/Volts ($\text{cm}^2/\text{Vs}$)
- $\partial = \text{Carrier density}$ (Carrier_Num $\times 10^{11} / \text{cm}^2$)
- $L_0 = \text{Lorenz number}$ approximately $1.5 \times 10^{-8} \text{V}^2 \text{K}^{-2}$
- $q = \text{Electronic charge}$ Coulombs (C)
- $\delta = \text{Electrical conductivity}$ ohm$^{-1}$-cm$^{-1}$ ($\Omega^{-1}\text{cm}^{-1}$)
- C.O.P = Coefficient of performance of thermoelectric

- $lmfp = \text{Average phonon mean free path}$ Armstrong ($\dot{\text{A}}$)
- $C = \text{Specific heat}$ (joules / cm$^3$ $^\circ\text{K}$)
• $vt = \text{Average phonon velocity}$ Armstrong/sec ($\frac{\text{A}}{\text{sec}}$)
• $PD = \text{Cooling power density}$ watts/cm$^2$ (W/cm$^2$)
• $Qm = \text{Maximum heat pumping}$ watts (W)
• $a = \text{Area of thermoelectric device}$ (cm$^2$)
• $\ell = \text{Thickness of thermoelectric device}$ (cm)
• $N = \text{Number of couples in thermoelectric module}$
• $h = \text{Heat transfer coefficient of heat sink}$ Watts/cm$^2$°C (W/cm$^2$°C)
• $a = \text{Area of heat sink}$ (cm$^2$)
• $T_S = \text{Heat sink temperature}$ (°C)
• $T_A = \text{Ambient temperature}$ (°C)
• $Q_p = \text{Heat pumping capacity of}$
  Thermoelectric cooling module watts (W)
• $G = \text{Ratio of cross-sectional area/length}$
  of each thermoelectric element (cm)
• $Q_{te} = \text{Amount of heat dissipated by a}$
  thermoelectric cooling module watts (W)
Glossary of Important Terms [16]

**ASPECT RATIO**: The numerical ratio of the length (height) to cross-sectional area of a thermoelectric element. An element’s L/A aspect ratio is inversely proportional to its optimum current

**CALORIMETER**: A scientific apparatus used to measure the evolution or absorption of heat. A calorimetric system can be used to measure the heat dissipated by the Device Under Test (D.U.T)

**COEFFICIENT OF PERFORMANCE (COP)**: A measure of the efficiency of a thermoelectric module, device or system. Mathematically, COP is the total heat transferred through the thermoelectric device divided by the electric input power.

**COLD SIDE OF A THERMOELECTRIC MODULE**: The side of a module that normally is placed in contact with the object being cooled. When the positive and negative module leads are connected to the respective positive and negative terminals of a DC power source, the module’s cold side will absorb heat.

**DELTA-T**: The temperature difference between the cold and hot sides of a thermoelectric module. Delta T may also be expressed as "ΔT"

**EFFICIENCY**: For thermoelectric coolers, mathematical efficiency is the heat pumped by a module divided by the electrical input power; for thermoelectric generators, efficiency is the electrical output power from the module divided by the heat input.

**FIGURE-OF-MERIT (Z)**: A measure of the overall performance of a thermoelectric device or material. Material having the highest figure-of-merit also has the highest thermoelectric performance. The multiple of Z and absolute temperature T is (ZT), a dimensionless quantity, which defines the figure of merit for a given temperature.
**HOT SIDE OF A THERMOELECTRIC MODULE:** The face of a thermoelectric module that usually is placed in contact with the heat sink. When the positive and negative module leads are connected to the respective positive and negative terminals of a DC power source, the module’s hot side will reject heat. Normally, the wire leads are attached to the hot side ceramic substrate.

**JOULE HEATING:** Heat produced by the passage of an electrical current through a conductor or material due to the internal resistance.

**MODULE:** A thermoelectric cooling component or device fabricated with multiple thermoelectric couples that are connected thermally in parallel and electrically in series.

**PELTIER EFFECT:** The phenomenon whereby the passage of an electrical current through a junction consisting of two dissimilar metals results in a cooling effect; when the direction of current flow is reversed heating will occur.

**SEEBECK EFFECT:** The phenomenon whereby an electrical current will flow in a closed circuit made up of two dissimilar metals when the junctions of the metals are maintained at two different temperatures. A common thermocouple used for temperature measurement utilizes this principle.

**THERMAL RESISTANCE (HEAT SINK):** A measure of a heat sink’s performance based on the temperature rise per unit of applied heat. The best heat sinks have the lowest thermal resistance.

**THOMSON EFFECT:** The phenomena whereby a reversible evolution or absorption of heat occurs at opposite ends of a conductor having a thermal gradient when an electrical current passes through the conductor.
Chapter 1 Introduction

1.1 Foreword

The last two decades have seen a steady increase in microprocessor performance as silicon technology continues to scale in accordance to Moore’s law [11]. The constant need for higher performance and an increased level of functional integration, as well as die size optimization has lead to preferential clustering of higher power units on the processor. This in turn leads to higher heat flux concentration in certain areas of the die and lower heat fluxes in certain other regions of the die, which manifest themselves as large temperature gradients on the die. These local power densities, commonly referred to as “hot spots”, are becoming increasingly important as we deal with emerging generations of microprocessor architecture. The thermal designs have to meet stringent heat-flux requirements that are significant multiples of the average heat flux at the silicon-package interface [18]. The thermal cooling solution provided must effectively ensure that the junction/die temperature of the processor does not exceed the rated 90-110 °C range to guarantee device performance and reliability.

There are two major reasons to maintain the operating temperature of the processor below a critical level [18].

1. The reliability of circuits (transistors) is exponentially dependent on the operating temperature of the junction. Even small differences in operating temperature (order of 10–15°C) can result in a ~2X difference in the lifespan of the devices.
2. The other factor is the speed of the microprocessor. At lower operating temperatures, microprocessors can operate at higher speeds due to reduced gate delay. Another secondary effect of lower temperatures is related to a reduction in idle power dissipation (also known as leakage power) of the devices, which manifests itself as reduction in overall power dissipation.

We shall now look at the various options by which the thermal design problem can be solved. The thesis presents several novel methodologies by which these problems can be solved with the integration of an efficient, high ZT thermoelectric device.
1.2 Amount of Heat Transferred from Heat sink.

The amount of heat dissipated by a heat sink \((Q\text{ in joules})\) is given by

\[
Q = h \times A \times (T_s - T_a)
\]

Equation 1-1. Heat Dissipated by Heat sink [18]

It is apparent from the equation that in order to increase the total heat transfer from the heat sink we must increase one or more of the parameters \(h\), \(A\), or \(T_s - T_a\). In the past, forced convection air-cooling passed through extruded heat sinks with copper bases proved adequate to tackle such power densities. Presently with power densities exceeding 200 W/cm\(^2\) in approximately 16mm\(^2\) area on die, system design engineers are investigating more efficient cooling solutions [15]. Furthermore thermal improvement better than 10% is unlikely by convection alone [11]. We shall now look at the various options available to the system designer to increase the heat transfer from the heat sink to the ambient and the problems concerning each of these options.

1.2.1 Increasing Surface area of Heat Sink

An increase in the heat-sink surface area, either by increasing the number of fins or by modifying the shape of the fins, increases the amount of heat that the heat sink can release to the ambient air stream [18]. However, increasing the heat-sink surface area results in an increase in the pressure drop across the heat sink. This is because the viscous shear stress acts over a larger area creating a larger frictional force. The system fan must be capable of generating a large enough pressure head to overcome the frictional resistance to the flow of air across the heat sink.

1.2.2 Forced Convection Airflow

The heat transfer coefficient on the heat-sink fins depends primarily on the airflow rate, the spacing between the fins, and the flow regime (i.e., laminar or turbulent) that exists on the heat-sink fins. A higher airflow results in higher heat transfer coefficients and a correspondingly higher-pressure drop. Increasing the fin thickness would lead to a reduction in the number of fins and heat-transfer area. This implies that there would be an optimum fin thickness at which the increased heat spreading would
offset the contribution from the decreased fin area to provide the maximum heat transfer from the heat sink. Any increase in finned surface area or change in heat-sink base material from aluminum to copper results in an increase in the heat-sink weight.

1.2.3 Acoustics

Any enhancement to the heat transfer from the heat sink is usually accompanied by an increase in the pressure loss across the heat sink. In order to overcome the pressure loss, a larger fan may be required. Increasing the airflow rate to increase the heat-transfer coefficient may also require a larger fan. Increased flow rates and larger fans typically result in increased fan noise. Noise attenuation schemes and larger system fans add to the total cost of the cooling solution.

1.2.4 Heat Sink Temperature

The processor heat dissipation levels set the heat sink temperature and very rarely do cooling solutions control the sink temperature to aid more efficient heat transfer. In [Section 5.2] the thesis presents ways by which the heat sink temperature can be increased by active cooling using thermoelectrics to enable more efficient heat transfer to the ambient. It also presents an effort to extend the performance of forced convection air-cooling to future generations of processors.

1.2.5 Heat Spreading.

The temperature difference between the heat-sink surface and ambient air depends on the efficiency of heat spreading in the heat-sink base and fins. The amount of heat spreading depends primarily on the thermal conductivity of the heat-sink material and on the heat sink geometry. Several attempts have been made to improve the spreading resistance in heat sinks by solid metal or phase change solutions such Thermosyphons or Heat pipes. These face limitations in the form of low through plane conductivity for corresponding high values of in-plane conductivity, increased thermal resistance for low values of wick-thermal conductivity, low vapor pressure and increased resistance in heat pipes below critical temperatures [1].
1.3 Alternate Cooling Solutions

Several other possible cooling solutions can be implemented to solve these problems. These include

1. Circulated liquid cooling and refrigeration
2. Thermoelectrics.

We shall look into the pros and cons of these methods in the following subsections.

1.3.1 Circulated Liquid Cooling and Refrigeration [11]

This involves cooling the processor using water or refrigerant circulated through pipes and pumps. The main advantage of this method is that the heat sink is moved away from the processor and therefore the surface area can be increased. However, there is limited space within the chassis and the cost and reliability of such cooling methods is a big factor that needs to be considered.

Significant advancements have to be made in terms of more efficient and reliable pumps and compressors, Safe and reliable refrigerants with secure hoses and fittings and importantly the weight and cost of the equipment should be reduced before they can become a viable option.

1.3.2 Thermoelectrics

Microprocessor cooling using thermoelectrics offers several advantages over conventional cooling methods. Thermoelectric modules augment the cooling of electronic module packages to reduce chip operating temperatures at a given heat load [1] or allow higher module heat loads at a given chip temperature level. Thermoelectric cooling modules also offer the advantages of being compact, quiet, have no moving parts and a high degree of precise control over the amount of cooling by means of controlling the current supplied to the thermoelectric.

Bulk thermoelectrics used popularly for microprocessor cooling, are severely constrained by their Figure of merit ZT (~ 1.14 max) and their Coefficient of Performance (COP) attained (~1.3). More importantly, Bulk thermoelectrics with 200µm
couple legs can only handle power densities of the order of 50W/cm². In comparison, Thin-film Superlattice Thermoelectrics [TFST] have measured ZT values of ~2.4 at 300K for p-type superlattices, with potential to pump heat flux of up to 700Wcm⁻². Furthermore, these thin-film devices have fast response times, achieving steady state cooling in 15μs [2]. This is vital in preventing thermal runaway and subsequent failure of microprocessors during rapid load transients.

Figure 1-1. Bulk and Thin-film comparison

The objective of this thesis is to apply TFST in efficient cooling of “hot-spots” on processors. The thesis presents an excellent test setup and experimental procedure, for characterization of the integrated TFST system. The tests performed evaluate the efficiency of the TFSTs and the resulting impact on microprocessor performance and reliability. The results show that active heat spreading using TFST significantly reduces the thermal design power and alleviates constraints on the cooling solution.
1.4 Thesis Highlights and Contributions

In the following subsection, I have made an attempt to summarize the important contributions made during this thesis research, which are

- Developing a novel methodology for evaluation of the performance of TFST in cooling hot spots on processor surface.
- Monitoring the performance of the microprocessor under test under various magnitudes of cooling and presenting the results and analyses.
- Writing configuration and run specification files to generate test vectors in SPEC CPU 2000 benchmarks, which create constant processor load over multiple tests.
- Building Modified Howland current source amplifier circuitry to power the TFST module with analog input from the Controller PC.
- Building a comprehensive Lab view platform for monitoring the integrated TFST-processor system. The program also measures the increased reliability due to heat spreading by TFST modules, which are presented in the results and analyses.
- Presenting a study of thermoelectric theory, thin film and bulk thermoelectrics, Peltier module functioning in this document. I also present a brief look at TFST structures and the material physics behind their functioning.

1.5 Thesis Organization

Chapter 2 starts with the description of Intel Pentium III micro-architecture with IR images showing the hot spots on die and the theory behind their occurrence. The chapter then describes the theory of thermoelectrics and the work done by the thermoelectrics research team at Research Triangle Institute [R.T.I] leading to this thesis. Chapter 3 describes in detail the problems in the design of the application system. A complete description of the final setup, which facilitates comprehensive evaluation of the system, is included. Chapter 4 illustrates the LabView front-end environment for the user interface and the supervisory and monitory functions. The results of the test runs with their analyses and conclusions are presented in Chapter 5. Chapter 6 summarizes the conclusions of this thesis and describes future work in this research area.
Chapter 2 Related Work

2.1 Chapter 2 Introduction

The chapter starts with the description of the Intel Pentium III micro-architecture and then moves onto Infrared [IR] images showing these hot spots and the theory behind their occurrence. I have made an attempt to understand the functioning of the processor under the two test cases and to analyze the causes for the images observed.

The focus of this work is to build a test platform for microprocessor cooling using TFST modules. Furthermore upcoming chapters will describe the test set-up and the various parameters that are monitored during the experiments. It is vital for the reader to be acquainted with thermoelectrics and the physical principles that govern their functioning in order to understand the importance of these parameters and the objective behind the construction of this set-up. This chapter presents a brief discussion of thermoelectrics and the commercially available Peltier modules, used for multiple applications.

The thesis puts forth a novel concept of selective cooling of processor die using active thermoelectric components. This is made possible by the research conducted at RTI, which has resulted in efficient thermoelectrics with very small footprints. An insight into these superlattice structures, the scientific theory of solids that explains their high ZT values and a comparison with other state-of–the-art bulk devices is also presented at the end of the chapter.

2.2 Analysis of Pentium III Architecture

A brief look at the layout of the Pentium III die is essential to understand the thermal footprint of the processor during operation [3].
The processor under observation is the Intel Pentium III 850MHz microprocessor. The die has been fabricated using 0.18-micron CMOS process technology, with six metal buildup layers in its packaging. It has a normalized transistor count of 28.1 million transistors over a 106 mm square die-area.

2.2.1 Architectural Blocks, Description and Function

A review of the various architectural components of the processor as shown in Figure 2-1 is presented in this section [3]. I have attempted to describe their description and function and reasons why they could be potential hot spots during processor runtime.

**L2 Cache**: The 256K Level 2 (L2) cache, occupies nearly 30% of the memory area. Applications when started are loaded onto the L2 cache before processing. It is definitely a potential hot spot due to the dynamic nature of the input to the cache and the frequent change in stored values.
**IFU**: - Instruction Fetch Unit. Instructions fetch and 16 K byte 4-way set associative Level 1 (L1) instruction cache resides in this block. Instructions from the IFU are then forwarded into the Instruction Decoder (ID). Each instruction of an application has to pass through the IFU before it can be processed. Additionally, the presence of the L1 instruction cache makes the IFU a potential hot spot.

**ROB**: - Re-order Buffer. This supports a 40-entry physical register file that holds temporary write back results that have completed out of order. These results are then committed to a separate architectural register file during in-order retirement. The Reorder Buffer (ROB) in the processor, buffers the completed micro-ops, updates the architectural state in order and manages the ordering of exceptions.

**BTB**: - Branch Target Buffer. This block is responsible for dynamic branch prediction based on the history of past decision paths. The hardware instruction fetcher brings in instructions along the path predicted by the BTB into the streaming instruction buffers.

**BAC**: - Branch Address Calculator. Static branch prediction is performed here to handle the BTB missed case. If there was no valid entry in the BTB for the branch, the static predictor makes a prediction based on the direction of the branch. The static prediction mechanism predicts backward conditional branches (those with negative displacement), such as loop-closing branches, as taken whereas forward branches are predicted not taken.

**TAP**: - Test Accessibility Port. Various test and debug mechanisms reside in this block.

**ID**: - Instruction decoder. This unit is capable of decoding up to two instructions per cycle. The instruction decoder decodes each CISC-like instruction into RISC-like instructions called micro-ops. All stages after the ID stage of the pipeline process only the micro-ops.
**MS**: - Micro code Sequencer. This unit holds the micro code ROM and sequencer for more complex instructions. The micro code update functionality is also located here.

**RS**: - Reservation Station. Micro-ops and source data are held here for scheduling and dispatch to the execution ports. Dispatch can happen out-of-order and is dependent on source data availability and on the availability of the execution port. The wake-up and select logic consumes a lot of power and hence this is a potential hot spot for all types of applications.

**SIMD**: - Single Instruction Multiple Data integer execution unit. As one of the three performance enhancements of Multimedia Extension (MMX), which are a set of 57 instructions that process video and sound components and enable a richer game playing and graphic design creation experience, SIMD lets one microinstruction operate at the same time on multiple data items. What usually requires a repeated succession of instructions (a loop) can now be performed in one instruction. This is a potential hot spot for streaming applications.

**MIU**: - Memory Interface Unit. This is responsible for data conversion and formatting for floating point data types.

**IEU**: - Integer Execution Unit. This is responsible for ALU functionality of scalar integer instructions. Address calculations for memory referencing instructions are also performed here along with target address calculations for jump related instructions. This is a potential hotspot for integer applications that are compute-intensive.

**FAU**: - Floating point Arithmetic Unit. This performs floating-point related calculations for both existing scalar instructions along with support for some of the new SIMD-FP instructions.
**PFAU:** - Packed Floating point Arithmetic Unit. This contains arithmetic execution data-path functionality for SIMD-FP specific instructions.

**ALLOC:** - Allocator. The Alloc performs allocation of various resources such as ROB, MOB, and RS entries here prior to microinstruction dispatch.

**RAT:** - Register Alias Table. During resource allocation, the renaming of logical to physical registers is performed here.

**MOB:** - Memory Order Buffer. Acts as a separate schedule and dispatch engine for data loads and stores. Also temporarily holds the state of outstanding loads and stores dispatched until completion. This is a potential hot spot in memory intensive applications.

**DTLB:** - Data Translation Look-aside Buffer. Performs the translation from linear addresses to physical address required for support of virtual memory.

**PMH:** - Page Miss Handler. Hardware engine for performing a page table walk in the event of a TLB miss.

**DCU:** - Data Cache Unit. Contains the non-blocking (hit under miss) 16K Byte 4-way set-associative L1 data cache along with associated fill and write back buffering.

**BBL:** - Backside Bus Logic. Logic for interface to the backside bus for accesses to the external unified level two-processor cache.

**EBL:** - External Bus Logic. Acts as logic for interface to external front-side bus.

**PIC:** - Programmable Interrupt Controller. Local interrupt controller logic for multi-processor interrupt distribution and boot-up communication.

**CLK:** - Clock generator/Clock tree is a major contributor to total power of chip.
2.3 Potential Hot-Spot Locations in Pentium III die

Experiments to identify and isolate the hot spots were conducted by infrared imaging the processor die during operation. These experiments were conclusive in determining the area of these hot spots and their magnitude in terms of maximum temperature reached. Analysis of the internal architecture (explained above) justified the occurrence of these hot spots during the experimental conditions.

2.3.1 Infrared Image of Processor die during Startup

The IR image (Figure 2-2) was observed when the heat sink and cooling fan were removed from contact with the processor. The CPU was then started. As expected, we observe that the Instruction Fetch Unit is the hottest spot in the CPU with temperatures reaching 109°C. The reason is due to the fact that the processor is trying to load the
operating system (O/S) and the IFU is converting fetching and converting the instructions of the O/S into micro-ops for processing. The on-die thermal diode exceeds the rated temperature and causes the processor to shut down after a few seconds without completely loading the O/S.

2.3.2 Infrared Image of Processor during Application Load

![Image of processor](image.png)

Figure 2-3. IR image of processor while loading an application [RTI].

The IR image (Figure 2-3) was observed when the heat sink and cooling fan were removed from contact with the processor after it had reached steady state operation. At steady state, the O/S and a few other processes were running in the background. A new application was then started. Compared to the previous figure (Figure 2-2), other components of the core such Reorder Buffer, Micro code sequencer and Instruction
decoder are also seen to be at a higher temperature. This is because the O/S and other applications have already heated the processor core. However, when a new application is started, instructions from the new application are fetched and processed. The O/S instructions for running the new application are being processed by these CPU components. The on-die thermal diode reads temperatures over 119°C as shown by the IR image and shuts the processor down without completely loading the application.

2.4 Introduction to Thermoelectrics

Thermoelectric coolers are solid-state heat pumps used in applications where temperature stabilization, temperature cycling, or cooling below ambient are required. There are many products using thermoelectric coolers, including CCD cameras (charge coupled device), laser diodes, microprocessors, blood analyzers and portable picnic coolers [4].

Thermoelectrics can be used to heat and to cool, depending on the direction of the current. In an application requiring both heating and cooling, the design should focus on the cooling mode. Using a thermoelectric in the heating mode is very efficient because all the internal heating (Joulian heat) and the load from the cold side are pumped to the hot side. This reduces the power needed to achieve the desired heating.

2.5 Thermoelectric Effects

Thermoelectrics are based on the Peltier Effect, discovered in 1834, by Jean Peltier, which is stated as a refrigerating power caused by temperature differential which is obtained by passing current along a circuit containing dissimilar materials [5]. Heat is absorbed at one junction of the two materials and heat is released at the other junction. The transfer of heat is caused by the change in electron energy levels when electrons access the conduction band, as defined by quantum physics. The conduction band varies with each material, which means that conducting electrons in some materials are at a higher energy level than in other materials. When electrons pass down a circuit of dissimilar materials, the electrons alternately extract energy or release energy with each change in conduction band. The desired
refrigerating effect occurs when electrons move to a higher energy level upon change of material. A reverse effect also occurs where electricity is generated from a circuit of dissimilar materials that are exposed to a temperature differential (Seebeck Effect)[6].

![Figure 2-4. Cross-section of typical thermoelectric couple [4].](image)

The Peltier Effect is only one of the three thermoelectric effects, the other two are known as the Seebeck Effect and Thomson Effect. Whereas the last two effects act on a single conductor, the Peltier Effect is a typical junction phenomenon. The three effects are connected to each other by a simple relationship [6]. The Seebeck and Peltier coefficients are called cross effects since they connect an electrical response to a thermal force or a thermal current to an electrical current. The cross effects are the basis for utilizing thermoelectric materials for energy conversion applications. The Seebeck coefficient indicates how large a voltage a material generates in a temperature gradient and the Peltier coefficient indicates how much heat passes through a material for a given current.

Thompson effect [6] asserts that when an electrical current flows through a material, which is also subject to a temperature gradient, heat is generated at a rate proportional to the electrical current and also proportional to the temperature gradient.
Two different conductors, a & b have junctions at W and X. If a temperature difference T is created between W and X, a voltage difference V appears between the two b segments. Upon open circuit conditions, the Seebeck coefficient is defined as

$$\alpha_{ab} = \frac{dV}{dT}$$

Equation 2-1. Seebeck Coefficient [6]

If W is hotter than X, a thermocouple ab would drive a clockwise current and is said to have a positive \(\alpha\). By contrast, if an imposed clockwise current (I) liberates heat at W and absorbs heat at X, then the thermocouple ab has a negative Peltier coefficient \(\Pi\). The rate of heat exchange at the junction is

$$Q = \Pi_{ab} \times I$$

Figure 2-6. Peltier Coefficient [6]

If current is flowing and there is a temperature gradient, there is also a heat generation or absorption within each segment of the thermocouple because \(\alpha\) is temperature dependant. The gradient of the heat flux is given by

$$\frac{dQ}{ds} = \zeta I \frac{dT}{ds}$$

Figure 2-7. Thomson Coefficient [6]

Where s is the spatial coordinate. Both \(\zeta\) and \(\Pi\) can be obtained from \(\alpha\), which is easily measured. Experiments have confirmed the relationships derived by Kelvin:
\[ \zeta_a - \zeta_b = T \frac{d\alpha_{ab}}{dT} \]


And

\[ \Pi_{ab} = \alpha_{ab} T \]


The last equation provides a fundamental link between thermoelectric cooling (\( \Pi \)) and thermoelectric power generation (\( \alpha \)). Thermoelectric cooling and power generation require joining two different materials. Therefore it is \( \Pi \) and \( \alpha \) of the thermocouple that matter in practice.

2.6 Peltier Modules

The typical thermoelectric module is manufactured using two thin ceramic wafers with a series of P and N doped bismuth-telluride semiconductor materials sandwiched between them. The ceramic material on both sides of the thermoelectric adds rigidity and the necessary electrical insulation. The N type material has an excess of electrons, while the P type material has a deficit of electrons. One P and one N make up a thermocouple, as shown in Figure 2-5. The thermoelectric couples are electrically in series and thermally in parallel.
A thermoelectric module can contain one to several hundred couples. As the electrons move from the P type material to the N type material through an electrical connector, the electrons jump to a higher energy state absorbing thermal energy (cold side). Continuing through the lattice of material, the electrons flow from the N type material to the P type material through an electrical connector, dropping to a lower energy state and releasing energy as heat to the heat sink (hot side).

The advantages of mechanical simplicity and suitability for small-scale applications are the principle reasons for selecting thermoelectric cooling instead of compressor-driven refrigeration for several applications. Refrigeration based on the Peltier effect is obtained by arranging a series of such thermoelectric cells in a horizontal array, which is then encased in plates made of an electrical insulator as shown in Figure 2-8. Each thermoelectric cell consists of a pair of dissimilar semi-conductors, which are connected by electrical conductors at either end. The requisite dissimilarity in semi-conductors is obtained not only by using dissimilar materials, but also by using different dopants. The tablet shaped component that is produced by this means is called a module or Peltier module.

2.7 Thermal Parameters and Equations

The appropriate thermoelectric for an application, depends on at least three parameters [7]. These parameters are the hot surface temperature (Th), the cold surface temperature (Tc), and the heat load to be absorbed at the cold surface (Qc). The hot side of the thermoelectric is the side where heat is released when DC power is applied. This side is attached to the heat sink. When using an air-cooled heat sink (natural or forced convection), the hot side temperature can be found by using
\[ T_h = T_{amb} + (\theta)(Q_h) \]

**Equation 2-4. Hot side temperature of Thermoelectric [8]**

\[ Q_h = Q_c + P_{in} \]

**Equation 2-5. Heat released to the hot side [8]**

The thermal resistance of the heat sink causes the temperature to rise above ambient. If the thermal resistance of the heat sink is unknown, then estimates of acceptable temperature rise above ambient are:

- Natural Convection 20°C to 40°C
- Forced Convection 10°C to 15°C
- Liquid cooling 2°C - 5°C (rise above the liquid coolant temperature)

The main advantage of air-cooling is simplicity since only fins and a fan are required but the major disadvantage is reduced thermal efficiency. It is found that the poor thermal conductivity of air causes a high temperature to develop on the hot face and conversely a very low temperature on the cold face for even a moderate level of heat transfer [8].

The main advantage of using water-based cooling systems is that the Peltier module can work at a temperature difference that is far closer to the nominal temperature difference of the system. This is because the convective heat transfer coefficient between water and a solid interface is much higher than air for comparable flow conditions. The Peltier module is then able to work at close to its optimum thermodynamic efficiency thus reducing electricity consumption to practicable levels.

The heat sink is also a key component in the assembly. A heat sink that is too small means that the desired cold side temperature may not be obtained. The cold side of the thermoelectric is the side that gets cold when DC power is applied. This side may
need to be colder than the desired temperature of the cooled object. This is especially true when the cold side is not in direct contact with the object, such as when cooling an enclosure.

The temperature difference across the thermoelectric (ΔT) relates to Th and Tc according to Equation.

\[ \Delta T = T_h - T_c \]

Equation 2-6 Temperature difference across thermoelectric [7]

Estimating Qc, the heat load in watts absorbed from the cold side is difficult, because all thermal loads in the design must be considered. Among these thermal loads are:

- **Active Thermal losses**
  - I²R heat load from the electronic devices
  - Any load generated by a chemical reaction

- **Passive Thermal losses**
  - Radiation losses such as heat loss between two close objects at different temperatures
  - Convection losses such as heat loss through the air, where the air is at a different temperature than the object
  - Insulation Losses
  - Conduction Losses such as heat loss through leads, screws, etc.
  - Transient Load such as time required in changing the temperature of an object. This is related to the latent heat of the object

The performance of thermoelectric devices depends on the figure of Merit (ZT) of the material, given by

\[ ZT = \left( \frac{\alpha^2 T}{\rho K_T} \right) \]

Equation 2-7. Figure of merit of Thermoelectric [2]
$Z$, the material coefficient, can be expressed as

$$Z = \left( \alpha^2 \sigma / (K_L + K_e) \right)$$

Equation 2-8. $Z$ material coefficient [2]

or as

$$Z \approx \alpha^2 \left[ \left( K_L / \mu \Delta q \right) + L_0 T \right]$$


In order to enhance the figure of merit ($ZT$), the Thermal Conductivity ($K_L$) should be reduced more strongly than the carrier mobility ($\mu$), while maintaining the same carrier density ($\sigma$) and absolute temperature ($T$).

The heat pumping capacity, $Q_p$, of a Thermoelectric-cooling module is given by

$$Q_p = 2N \left( \alpha I T C - \frac{I^2 \rho}{2G} - K_1 \Delta T G \right)$$


The amount of heat, $Q_{te}$, dissipated by a thermoelectric cooling module to perform the electronic pumping is given by

$$Q_{te} = 2N \left( \frac{I^2 \rho}{G} + \alpha l \Delta T \right)$$

Equation 2-11. Heat dissipated by thermoelectric [8]

The Coefficient of Performance (COP), a measure of efficiency of the module to cool a specific Heat load is given by
\[ \text{COP} = \frac{Q_p}{Q_t} \]

Equation 2-12 Coefficient of performance [8]

2.8 Thermoelectricity Theory of Solids

It is vital to make a distinction at the outset, between the properties of the lattice and the properties of the electrons. The lattice refers to the positions of the atoms themselves [9]. The atoms are not stationary, but are considered to move only very slightly compared to the distances between the atoms. This is to say that they vibrate about their average position, but do not move throughout the crystal. Most of the electrons are considered localized, always remaining associated with the same particular atom. Localized electrons do not carry any current, even when a force is applied, and may be considered to be part of the lattice. Some of the electrons, however, are essentially "free" and have the ability to move throughout the solid. It is these "free" or valence electrons, which determine the ability of a material to carry an electrical current.

2.8.1 Origin of Charge Carriers

Thermoelectric energy conversion is the creation of charge carriers in insulators. Since insulators ideally have no charge carriers, any defects that are present can be said to be due to defects [9]. When a host atom is replaced by an atom with more valence electrons than the host has, the extra electron is not needed for bonding and enters the next higher available energy state. There is some attraction between the negative electron and the positively charged donor atom left behind, but often the attraction is very weak and the electron is free to move throughout the crystal, much like the electrons in a metal.

When a host atom is replaced by an atom with fewer valence electrons than the host has, a bond is left one short of the ideal. This "shortage" is called a hole and there is some attraction between the hole and the negatively charged ion left behind, which is
called an acceptor. The hole is literally the absence of an electron in one of the bonds and
often the attraction is very weak, allowing the hole to move freely from bond to bond
throughout the crystal.

![Lattice Showing Atomic Substitutions by a Donor, Creating a Free Electron, and by an Acceptor, Creating a Free Hole.](image)

**Figure 2-9. Lattice showing atomic substitutions [9]**

Even in an otherwise perfect crystal, where all the bonds are exactly filled,
electrons and holes are created thermally. A few electrons in the bonding states will
occasionally acquire enough energy to leave the bonding state (leaving behind a hole)
and enter one of the anti-bonding states (creating a free electron). These electron-hole
pairs are constantly being created and destroyed. There are several other mechanisms to
create free charges or holes other than the simple substitution of dopants just described.
Defects such as the absence of atoms (vacancies) or extra atoms occupying positions
between the usual lattice sites (interstitials) can also create carriers. The precise origin of
free charge carriers varies greatly from material to material and the control of doping
levels is a major technical challenge.

### 2.8.2 Mass Spring Model

The kinetic features of a lattice can be represented by a simple mass and spring
model where the atoms are represented by point masses and the bonding between the
atoms are represented by very small springs [9].
In the undisturbed lattice the atoms would be regularly spaced apart with a distance corresponding to a unit cell repeat distance. In fact the atoms will vibrate about their equilibrium positions due to thermal agitation. This motion is not entirely random, however, since the movement of one atom stretches or compresses the springs connecting it to neighboring atoms.

![Mass and Spring Model](image)

**Figure 2-10. Mass spring model of crystal [9]**

### 2.8.3 Phonons

Vibrations, even if initiated at a single atom, will propagate throughout the crystal. Rather than describing the vibrations of the each atom individually, it has been found to be both more convenient and more accurate to speak about regular, sinusoidal disturbances of entire groups of atoms. Such a sinusoidal disturbance is called a phonon. The word phonon means "particle of sound" and is used because sound is precisely an elastic wave of compression and extension which propagates through a solid.

Since a collection of phonons can represent any possible configuration of disturbances from equilibrium, and since individual phonons represent particularly simple motions, which actually do occur in solids, the phonon description has become the most common tool for describing the properties of solids. Each phonon has a characteristic wavelength; the minimum wavelength \((L)\) allowed is one inter-atomic distance. A
phonon will carry a momentum given by $h/L$, where $h$ is the Planck's constant. This principle, first described by de Broglie, assigns a phonon wavenumber, defined by $2\pi/L$. Since there is a minimum allowed wavelength, there is also a maximum allowed momentum ($h/a$) and a maximum allowed wavenumber ($2\pi/a$). The energies of the allowed phonons vary with the direction the phonon moves through the crystal and the momentum (or wavelength) of the phonon [10].

2.8.4 Phonon Scattering Mechanism to Lower Thermal Conductivity

The previous discussion referred to photons as a wave propagating through the crystal. The particle-wave duality of Quantum Mechanics can also let us envision the phonon as a particle moving through the crystal. Any mechanism that absorbs the energy of the phonon or changes the phonon’s direction of propagation is called scattering. Since heat is carried by the phonons, scattering mechanisms that impede the flow of phonons effectively reduce the thermal conductivity. Scattering mechanisms return the distribution function from the state of nonequilibrium to equilibrium values [12]. We shall now look into the different phonon-scattering mechanisms.

2.8.4.1 No Scattering

If the scattering rate were truly and exactly zero, then once a phonon-heat current was established (for example) the heat or phonon current would continue to flow to the end of the solid, even after the temperature gradient was removed. This situation is sometimes said to imply very high thermal conductivity, limited only by the speed of propagation of phonons and is not observed practically.

2.8.4.2 Phonon-Phonon Scattering

Assuming atoms have been disturbed from their ideal positions generating phonons, one phonon represents an obstacle to another. But the scattering rate of one phonon due to collision with another is very small, explaining the very large thermal conductivity values of crystals such as Diamond, Sapphire, which are ideal, insulating crystals. This is called a phonon-phonon interaction and the resulting phonon-phonon scattering rate increases with increasing temperature simply because there are more
phonons around. In the quantum mechanical picture of phonons, this type of phonon-phonon scattering is described as the absorption or emission of one phonon by another phonon.

2.8.4.3 Point Defect and Alloy Scattering

A point defect simply means that one of the atoms making up the crystal is different from all of the others. The most important type of point defect in thermoelectric materials is usually an atom with a mass very different from the host.

2.8.4.4 Phonon-electron (or Hole) Scattering

The shift in the electronic energy levels due to a small deformation of the lattice is called the deformation potential and this provides a link between the system of charge carriers and the system of phonons. Through this interaction, a phonon may deposit its energy and momentum into one of the charge carriers. Or, a charge carrier can lose energy and momentum, creating a phonon. In either case, both the phonon and the charge carrier are scattered.

Conservation of energy and momentum considerations severely restrict which phonons can interact with which charge carriers. Very low energy, long wavelength phonons can interact with essentially all the charge carriers. But above certain phonon energy, there are essentially no charge carriers around to interact with. So, the phonon-electron (or hole) scattering mechanism is much more effective at scattering low energy, long wavelength phonons than it is at scattering high energy, short wavelength phonons.

2.8.4.5 Electronic Energy Bands

Isolated atoms have discrete energy levels, which may be occupied by electrons or may be empty. When two atoms are brought together, these energy levels mix to some extent. All of the valence electrons are consumed by filling the new "molecular energy levels," the lowest energy levels being filled first. The energy levels below the energy of the isolated atoms are called bonding levels and the higher energy levels are called antibonding levels [9].
As more and more atoms are brought together, the atomic energy levels become more and more mixed, but each energy level in the original isolated atoms is still represented in the final energy state-scheme. The individual energy levels of each atom form bands of allowed energies in the final solid.

We discuss the properties in terms of equilibrium and nonequilibrium conditions. The energy states outlined above, which were occupied in equilibrium, become unoccupied and states that were unoccupied become occupied with disturbance. Equilibrium distribution functions provide a statistical probability that a particular energy state is occupied. Such occupation changes transcend as waves moving to the right or left of the lattice.

In equilibrium there are no currents since there are just as many waves moving to the right as are moving to the left. By definition, a current means there are more waves moving in one direction than are moving in the opposite direction. For each energy level, then, there is an average time between changes of occupancy. This time is called the mean free time and is usually represented by the Greek letter Tau \( \tau \). When speaking of a wave (either a phonon or a charge carrier), this is the average time the wave moves until it hits something or otherwise changes into some other type of wave. The same quantity is also called the relaxation time or the collision time. The inverse, \( \tau^{-1} \), is called the collision rate or scattering rate.

2.9 RTI Thin-film Thermoelectrics

A material with a figure of merit of around unity was first reported over four decades ago [2]. Since then, despite investigation of various approaches, there has been only modest progress in finding materials with enhanced ZT values at room temperature.

To summarize, a ZT value significantly greater than one had not been demonstrated at ordinary temperatures (300 K) prior to the break through in research by RTI. Furthermore a one-to-one correlation between lower thermal conductivity (KL) and enhanced ZT had not been established. More importantly, the concept of individually tailoring the phonon properties without producing a deterioration of electronic transport, thereby enhancing ZT, has not been established [2].
RTI reports thin-film thermoelectric materials that demonstrate a significant enhancement in ZT at 300 K, compared to state-of-the-art bulk Bi$_2$Te$_3$ alloys. A ZT at 300 K of 2.4 in p-type Bi$_2$Te$_3$/Sb$_2$Te$_3$ superlattices and a similar, although less dramatic, ZT<1.4 in n-type Bi$_2$Te$_3$/Bi$_2$Te$_{2.83}$Se$_{0.17}$ superlattices has been measured. The enhancement in short, is achieved by controlling the transport of phonons and electrons in the superlattices [2].

Preliminary devices fabricated exhibit significant cooling at around room temperatures and the potential to pump a heat flux of up to 700 W/cm$^2$. Furthermore, the localized cooling and heating occurs some 23,000 times faster than in bulk devices [2]. Generic approaches proposed till date, to enhance ZT in thermoelectrics involve the use of quantum-confinement effects to obtain an enhanced density of states near the Fermi energy. Using such effects, a ZT of 0.9 at 300 K and 2.0 at 550 K, using estimated thermal-conductivity values, has been reported in PbSe$_{0.98}$Te$_{0.02}$/PbTe quantum-dot structures [2].

The second approach involves phonon-blocking/electron-transmitting superlattices. These structures utilize the acoustic mismatch between the superlattice components to reduce KL rather than using the conventional alloying approach, thereby potentially eliminating alloy scattering of carriers. The third thin-film approach is based on thermionic effects in heterostructures. The second approach of phonon-blocking/electron-transmitting superlattice structures forms the basis of the Thermoelectric research at RTI. We shall look into this in greater detail.

2.9.1 Lattice Thermal Conductivity Reduction in Superlattice Structures

The lattice thermal conductivities in short-period superlattices are less than those in homogeneous solid-solution alloys and exhibit a minimum for a period of 50 Å. The dominant state-of-the-art thermoelectric materials are based on solid-solution alloys in the (Bi$_x$Sb$_{1-x}$)$_2$Te$_3$ and Bi$_2$(Se$_y$Te$_{1-y}$)$_3$ system or in the SiGe alloy system. The rationale for solid solution alloying is that the lattice thermal conductivity is reduced much more
strongly than the electrical conductivity so that an overall enhancement in Z can be achieved for certain alloy compositions.

Figure 2-11. Lattice thermal conductivity and Average phonon mean free path (lmfp) Vs Superlattice period [2]

Experimental lattice thermal conductivity ($K_L$) and calculated average phonon mean free path ($l_{mfp}$) as a function of the period in Bi$_2$Te$_3$/Sb$_2$Te$_3$ superlattices and other reference materials. Note: There are three data points, almost on top of each other, at the 60 Å period, corresponding to 30 Å/30 Å, 10 Å/50 Å, 20 Å/40 Å structures.

The variation of the lattice thermal conductivity ($K_L$) as a function of the superlattice period is shown in Figure 2-11. Three points are worth noting:

- The $K_L$ of the superlattice structures shows a minimum for a period of 50 Å. The minimum $K_L$ value is 0.22 W/m °K. This value is nearly a factor of 2.2 smaller than that obtained for solid-solution alloys.
- The $K_L$ of larger-period superlattices exceeds that of the solid-solution alloy but begin to approach that of a weighted average of Bi$_2$Te$_3$ ($K_L = 1.05$ W/m °K) and Sb$_2$Te$_3$ ($K_L = 0.96$W/m °K).
- For superlattice periods of 50Å, $K_L$ begins to increase from the above minimum and starts approaching that of the solid-solution alloy.

2.9.2 Mean Free Path Reduction

Kinetic theory gives the relation between lattice thermal conductivity and average phonon mean free path.
\[ K_L = \frac{1}{3} c \rho (vt) \text{lmfp} \]

Equation 2-13. Mean free path, Lattice thermal conductivity equation [10]

For example, in Sb₂Te₃ an estimated lmfp of 9.6 Å from its \( K_L \) is measured. The value of 9.6 Å is due to the potential anharmonicity along the axis of heat flow, created by the repeat spacing of bonds in the crystal. Similarly, for the BiSbTe₃ alloy film, an estimated lmfp of 4.9 Å from its measured \( K_L \). For superlattices with the lowest \( K_L \), lmfp value of 2.2 Å is obtained. The coherent backscattering of phonon waves at the superlattice interfaces, which are essentially the regions of anharmonicity, is invoked to formulate a physical model for the reduction of lmfp, [12].

![Figure 2-12. Wave reflection at interface of Superlattice [10]](image)

Schematic of (a) an alloy and (b) a superlattice showing the potential for reflection of waves at the interface of a superlattice.

Let us consider a simple picture of a uniform alloy made of two components \( M_1 \) and \( M_2 \) and that of a superlattice consisting of two individual layers of \( M_1 \) and \( M_2 \) as shown. The alloy would exhibit an average "acoustic impedance" \( Z_{ave} \) that is related to the masses \( M_1 \) and \( M_2 \), as described by Brillouin. In the superlattice, each of the two layers has a characteristic impedance \( Z_1 \) and \( Z_2 \), respectively. At first glance it would appear that the specific arrangements of atoms, among the available lattice sites are irrelevant to the propagation of long-wavelength acoustic phonons. However, note that
the acoustic mismatch would lead to reflection of the phonon waves at the interface. Thus, in a superlattice, the acoustic long-wavelength phonons not only “see” the varying composition (as much in the random alloy) but also experience reflection at the periodic interfaces.

![Graph](image)

**Figure 2-13. Low-frequency cut-off wavelength Vs Superlattice period [2]**

The behavior of ultra short period superlattices can be understood by computing the wavelengths using the phase velocity for the cutoff frequencies. The cutoff wavelength ($\lambda_{\text{cutoff}}$) is plotted as a function of the superlattice period. It is observed that near the point where the minimum lattice thermal conductivity (equivalent to minimum average phonon transmission) is approached, the superlattice period is $2\lambda_{\text{cutoff}}$. When the cutoff wavelengths starts approaching and exceeding the individual layer thickness of the superlattice in both layers, the two layers probably become coupled and so the effect of acoustic mismatch starts to disappear. From this viewpoint, the cutoff wavelength would not decrease any further with the reduction of the superlattice period and the long-wavelength phonons would begin to be transported across the surface.
With an ambient temperature $T_{\text{ambient}}$ of about 298 °K, 32.2 °K of cooling (down to -7°C) was measured without any forced heat removal by blowing air or running water at the heat sink. In the linear regime (current $< 1$ A) where heat-sinking considerations are less, the superlattice device shows a factor of 2.2 cooling compared to bulk. Further 40°K of cooling is observed for the superlattice device, when the heat sink is maintained at 353°K using a large-wattage heater, equivalent to a semi-infinite heat source. This is analogous to cooling the heat-sensitive devices in regions adjacent to hotspots in a chip.

### 2.9.3 Thermoelectric devices for Localized, Rapid Cooling

Thin-film thermoelements lead to cooling of large power densities ($P_D$) for similar maximum heat pumping ($Q_m$). As the area of the device, $a$, is reduced proportional to its thickness $l$, $Q_m$ is unaffected. However, cooling power density ($PD \simeq Q/a$) is increased.

$$Q_m = \left( \frac{a}{l} \right) \left\{ 0.5 \alpha^2 T_{\text{cold-side}}^2 / \rho - [K_T (T_{\text{hot-side}} - T_{\text{cold-side}})] \right\}$$

**Equation 2-14. Maximum heat pumping capacity of thermoelectric couple [2]**
In addition to offering low ZT, which translates to low coefficient of performance (COP) in refrigeration, the bulk thermoelectric devices have low PD (~1Wcm⁻²), another disincentive for high-power electronics & microprocessor applications. Using the values of KT and α of the superlattices, available PD as a function of current is shown in Figure 2-15. PD is estimated to be a value 700Wcm⁻² at 353°K and 585Wcm⁻² at 298°K at the measured maximum cooling in superlattice devices compared to a value of 1.9Wcm⁻² in the bulk device.

Figure 2-15. Current Vs Cooling power density [2]

Figure 2-16. Potential COP Vs ZT for various technologies [2]
The effect of higher ZT on COP is shown in Figure 2-16. The translation of the device ZT to COP of refrigeration would involve efficient heat removal at the heat sink, reduction of thermal resistances at the interface between the active device and the two heat-spreaders, and the fabrication of p-n couples with minimal interconnect resistances.

The thin-film devices also allow the concept of localized cooling by matching the footprint of the refrigeration devices to that of thermal load. This is made feasible by the combination of microelectronic processing and the ability to place the thermoelectric devices at points of interest to provide cooling power where required. Furthermore TFST elements are fast acting—about 23,000 times faster than bulk devices. The thin-film device achieves steady state cooling (indicated by the development of cooling-induced Seebeck voltage) in 15ms, while the bulk thermoelement takes about 0.35 s. This is a result of the response time associated with the transport of heat through the thin-film (micrometers) rather than through the millimeters associated with bulk devices.

![Figure 2-17. Comparison of cooling time response of bulk and thin-film [2]](image)

The thermal response time is about $4\ell^2/\pi^2D$, where $\ell$ is the thickness of the thermoelement and $D$ is the thermal diffusivity. This rapid, high performance cooling and heating, capable of high power densities and with the ability to be locally applied, could have applications in technologies ranging from genomic/proteomic chips to fiber-optic switching.
2.10 Summary

On studying the micro-architecture of the Pentium III processor, we identify the Instruction Fetch Unit, the Reservation Station and the Single Instruction Multiple Data integer execution unit as potential hot spots on the processor die. This is due to the dynamic nature of the input to the cache and the frequent change in stored values, especially during streaming applications, which require repeated succession of instructions to be performed. The IR images taken during processor startup and application load were conclusive in determining the area of the hot spot and its magnitude in terms of maximum temperatures reached.

We then looked at the physical principles governing the operation of thermoelectrics such as Seebeck, Peltier and Thompson effects. Next part of the section dealt on the thermal parameters and the equations to determine their values. We looked at the thermoelectric theory of solids and the mass spring model, which explains the occurrence of phonons and their scattering mechanisms. The following chapters discussed RTI thin-film thermoelectrics and lattice thermal conductivity reduction in superlattice structures in detail. The chapter concludes by explaining how these devices are ideally suited for rapid localized cooling. We shall now look at the experimental setup and the results.
Chapter 3 Experimental Setup

3.1 Chapter 3 Introduction

The main objective of the experimental set-up is to show the possibility of hot spot cooling of microprocessors. My procedure to achieve this end is as follows.

• The primary step is to identify the hot spot, its size, location and the magnitude of the maximum temperature reached at the spot. We have already discussed this in Section 2.3.1 and Section 2.3.2 from Chapter 2.

• It is vital to have a measure of the processor power dissipation when it is running the SPEC CPU 2000 benchmarks. It is relatively easy to monitor the voltage supplied to the processor. Several software modules including ASUS probe, supplied by the motherboard manufacturer is capable of doing this. However it is more difficult to monitor or measure the current drawn by the processor, with which power is computed.

• I have adopted an indirect method of measurement to monitor the power dissipated by the processor. By measuring the heat absorbed by the cooling system, we can approximately calculate the heat dissipated by the processor. We build a calorimetric system, which cools the processor by circulating water to measure the heat dissipated. We shall look at this in greater detail in subsequent Section 3.2

• The next step is to verify the accuracy of the calorimetric system by comparing its result with a known load. We do this by substituting the processor with a 50-watt aluminum heater load and supplying it with a known measure of power

• A big factor in this measurement is the heat loss to the ambient air by convection or other methods, which is not accounted for by the system. To reduce this error we insulate the system such that there is minimum loss to the environment and all cooling occurs only through the water that is circulated. We can now safely assume that heat loss to the ambient is zero.

• Once we have calibrated the accuracy of the system, we can swap the simulated load with the actual processor load and measure the heat dissipated by the processor. This is done before the TFST module is integrated into the system as this might lead to additional complications in the calculation.
• The last step in the setup in the design is to integrate the TFST module at the hot spot and to have an accurate measure of processor’s performance and the performance of the system as a whole.

3.2 Simulated Aluminum Block 50Watt Load

The main part of the experimental setup is the Swiftech MCW5000-PT water-cooled thermoelectric assembly, used as a heat sink to cool the aluminum load. The 226-watt, (25Amp at 12 V) Peltier-cooling module was capable of dissipating the heat from the test Intel Pentium processor. The measured ZT of the Peltier module was $ZT = 0.75$. The Peltier cooler was powered by an independent power supply which allows us to accurately determine the power required to cool the processor at varying load conditions and with localized hot-spot cooling using TFST module.

An aluminum block of ½ inch thickness was designed to simulate the processor. A 0.375” diameter hole was drilled into the block to house a 50watt, 125volt resistive load element. The resistive load was then powered by a variable AC transformer and was used to generate load values ranging from 3watts to 54watts simulating the processor output under various usage and stress percentages.

The aluminum block was screwed onto another ½ inch thick copper block with artic silver thermal grease at the interface for more efficient heat transfer across the surface. The aluminum block was attached to the cold side of the Peltier module with the hot side cooled by a copper heat sink with radial fins. Water was pumped across these fins at a known flow rate from the recirculator, which also maintains the water within a given temperature range.

The Peltier cooling module was powered by a switching regulator supply at 320W, 25Amps. The current provided to the Peltier module was of the order of 25 amps. Due to lack of accurate multimeters or DC ammeters, which can measure such high amperage, the current was measured by passing the current carrying conductor through closed loop Hall effect sensors. This produces a value 1/100 times the actual value with less than 0.9% error. The scaled down current, which is output from the Hall-effect sensor, was then passed through a 50Ω-sense resistor and was measured easily with an ammeter.
The entire system was then housed inside an aluminum chassis (as seen on the figure in the top right corner in Figure 3-1) with Styrofoam insulation on the sidewalls and surrounding the system. This ensures minimal heat loss to the ambience and substantiates the argument that the heat dissipated by the cooling water was the same as the heat output by the Aluminum block and the Peltier system.

- The next step was to place thermocouples at the vital points to determine the temperatures at those junctures.
- Two thermocouples, one on the hot side and one on the cold side of Peltier cooler were placed to measure the $\Delta T$ across the Peltier cooler.
• Two more thermocouples, one on inlet of cooling water to thermoelectric water-cooled block and one on the outlet were used to measure the temperature difference between the inlet and outlet water temperatures. This was a direct measure of the heat drawn by the cooling water and was used to compute the heat dissipated by the whole system.

• A thermocouple was placed inside the aluminum block to hypothesize the temperature on the processor surface for varying load and stress conditions and to determine the temperature loss across the thermal grease, if any.

• A thermocouple was also placed inside the aluminum chassis to determine any temperature rise in the ambient due to the system.

    The readings of these thermocouples were amplified with cold junction compensation using an SCXI-1112 module and sent to a supervisory program written in LabView. The results, calculations and analysis from the setup are presented in Chapter 5.

3.3 Processor Cooling with Independent Peltier Module

In this section we replaced the simulated load aluminum block with the actual Pentium III processor. The current setup enables us to determine the power dissipated by the processor under various stress conditions. The difference in the temperatures of the inlet to outlet water is proportional to the power dissipated by the Processor and the Peltier system. The power input to the Peltier module is a known quantity. So we can calculate the power dissipated by the processor with a good measure of accuracy.

    The system, though is an extension of the earlier set-up, required a lot of additional work. The copper block was machined to create a recess to accommodate the elevation in the PGA370 socket on which the processor sits. This ensures complete contact between the die surface and copper block. A custom retention mechanism was made from aluminum strip block and tensile wires, to bind the heat sink to the socket clips. This is shown in the snapshot of the system in Figure 3-2. Final setup block diagram

    Few more parameters in addition to the ones in the earlier setup were introduced in the measurements. The CPU temperature and the motherboard temperature as measured by the ASUS Probe software were included. The Probe software reports the on-die thermal diode, which was placed in the hottest spot on the processor during fabrication. The
processor was stressed using SPEC CPU 2000 benchmarks (A-1 Appendix) and its performance as measured by these benchmarks was reported.

3.4 Hot Spot Cooling using Integrated TFST Module

In the final setup the TFST module was placed at the Hottest spot on the processor as identified by the IR images. The measured figure of merit value for the TFST module was at $ZT = 0.26$. The integration of the TFST module to the processor surface is a problem of multiple magnitudes.

- The location and dimension of the hot spot is vital in the device fabrication. The TFST module fabrication and packaging is determined by these parameters. The hot and cold sides of the module need to be created to the same dimensions as the hot spot. This guarantees that all parts of the processor die are either attached to the TFST module or to the copper heat spreader, which is vital for safe operation.

- A heat sink copper block (heat spreader) needs to be machined such that the TFST module is over the hot spot and copper block covers the rest of the die surface.

- The TFST module requires a custom-made constant current source power supply for reliable and accurate operation.

- And finally, thermocouples need to be placed at the interface to measure the thermal transients at the hot spot in contact with the cold side of the TFST module.
The following figure outlines the final setup in detail.

![Final setup block diagram](image)

**Figure 3-2. Final setup block diagram**

### 3.4.1 Power Circuit for TFST module

A Modified Howland Current source circuit using the OPA548 amplifier powers the TFST module. The capability of the circuit is that output current through the load is independent of the resistance of the load and depends only on the input voltage, $V_{in}$. This is vital for powering thermoelectric modules as their resistance changes with temperature of operation. This causes the current to change which results in varied operation without control. We shall look at the custom circuit and the PCB in greater detail.
Figure 3-3. Schematic of TFST power circuitry
3.4.1.1 Analysis of Schematic for Power Supply to TFST

We now analyze the schematic to show that the current through the TFST is independent of its load characteristics and is constant, even though the TFST module resistance may vary during operation.

**Va**: voltage output from the Op amp can be given as

\[ V_a = \frac{R_4}{R_3} V_{in} + V_b \]

\[ V_a - V_b = \frac{R_4}{R_3} V_{in} \]

*Equation 3-1. Voltage output from Op-Amp*

By Ohm’s law the current \( I_b \), through the Sense resistor \( R_{s1} \) can be written as

\[ I_b = \frac{V_a - V_b}{R_{s1}} \]

\[ I_b R_{s1} = V_a - V_b \]

*Equation 3-2. Current through Sense Resistor*

Substituting Equation 3-1 in Equation 3-2.

\[ I_b = \frac{R_4}{R_3} \frac{1}{R_{s1}} V_{in} \]

*Equation 3-3. Current in terms of Vin*

If \( R_4 \) is much greater than \( R_{s1} \), then \( I_b \) can be assumed to flow through the load. In our case \( R_{s1} \) is 0.1Ω and \( R_4 \) is 20K. The capacitor \( C_1 \) provides a single dominant pole to prevent oscillators. Without a load, the positive feedback will equal the negative feedback when power is first applied to the circuit. Capacitor \( C_2 \) insures that the positive feedback is less than the negative feedback when power is first turned on. If the load is non-linear, it
will essentially be an open circuit until the voltage rise is enough to cause it to start conducting.

3.4.1.2 PCB for Powering TFST module

Figure 3-3. PCB for Powering TFST module

The PCB shown in Figure 3-3 was built housing the amplifier and current sense circuit using LM358 ICs. The measure of the current and voltage supplied to the TFST provides the value of the power input to the module for rated cooling. These measurements were sent back to the supervisory program wherein the COP of the Peltier and the TFST module was computed. Thermocouple readings measured at the interfaces, are sent to the SCXI 1112 8-channel thermocouple amplifier module. They are then amplified and sent back to the 16-Bit, 16 Analog input Data acquisition card (NI PCI-6036E) system with
200kS/sec sampling rate, where the values were used for computation in the supervisory control program.

3.4.2 TFST module Mounting

The TFST Module needs to be mounted onto the processor accurately. My approach to achieve this was as follows

- The Top header of the TFST module needs to be placed such that it is in complete contact with the hot spot on the processor. To achieve this, mark the footprint of the processor on a copper block. Also mark the hot spot location on the processor footprint.
- Machine the copper with counter sunk screw holes to attach to the water cooler. The screw holes need to be counter sunk to ensure that the screw head do not protrude preventing proper contact between the copper surface and processor die.
- Create a recess at one edge to accommodate the rise in the PGA-370 socket. The dimensions of the TFST module are measured to be 4mm by 7mm. Machine a square hole of similar dimensions into the copper such that the Cold side of the TEC is on the same plane as the copper surface. This ensures that while the hot spot is independently cooled by the TFST module the rest of the processor die in contact with the thermal heat spreader.
- Solder Contact onto the module and insulate with strips of Kapton tape, which also serves as a heat sink when the wires get hot, typically when more than 3Amps of current are pumped through them.
- A very tricky part in the mounting is to delicately place a 1-mil thermocouple in contact with the cold side to measure the Hot-spot temperature.
- Attach the copper block housing the TFST module to the water-cooled heat sink.
- Place the entire assembly over the processor and firmly attach to the socket clips using the custom-made retention mechanism.
3.5 Chapter 3 Conclusion

In chapter 3 we have discussed at the various objectives of the Thesis and the approaches taken to achieve them. We have built a system to measure the heat dissipated by the processor under various load and stress conditions. The system has been characterized and calibrated with a known heat load to measure the error percentage. The processor power has been measured with independent Peltier-cooling in effect. The TFST module has been mounted and placed in contact with the hot spot on the processor. The results of all these independent experiments are discussed in detail in Chapter 5.
Chapter 4 LabView Monitor and Control Program

4.1 Chapter 4 Introduction

Chapter 4 describes in detail the Supervisory and control program, which I developed to monitor the various parameters of the set-up. I chose National Instruments Labview to code the required programs due to several reasons.

- It is a highly productive graphical programming environment that combines easy to use graphical developments with the flexibility of a powerful programming language.

- LabView uses a patented dataflow-programming model that frees the programmer from the linear architecture of text-based languages. Because it is the flow of data between objects on a block diagram, and not sequential lines of text, that determines execution order in LabView, the programmer can easily create diagrams that execute multiple operations simultaneously.

- With the LabView Instrument Wizard, you immediately detect any instrument connected to the computer, including GPIB, VXI, Serial, and computer-based instruments. The wizard installs appropriate instrument drivers and in minutes expedites the communication with the connected instruments.

- LabView instrument drivers translate instrument capabilities into a set of high-level functions to reduce development time and simplify instrument control by eliminating the need to learn the complex low-level programming protocol for each instrument.

Furthermore, I built the experimental set-up using National Instruments Data acquisition cards and Thermocouple amplification modules, for which Instrument drivers were already available in Labview. So Labview seems the obvious choice to overlook device protocols and to start programming based on required functionality.

This chapter starts with an introduction to LabView to inform the user of the basic terms used and then moves on to describe the various programs used for monitory and supervisory control.
4.2 Introduction to LabView

Labview is a graphical programming language in which the programs are written using pictures, not words. A VI meaning Virtual Instrument is a software version of instruments found in a laboratory used for scientific measurements and control. In a more general context, a VI is a program module written in Labview [13].

A VI consists of three major parts (1) Front panel, (2) Block diagram and (3) an icon and connector pane. Every front panel has at most one block diagram and every block diagram has exactly one front panel associated with it. The front panel is the interface to the User and sometimes called GUI (Graphical user Interface) and the block diagram is the code or the heart of the program. The Icons in the front panel are called controls or indicators depending on whether data moves into or out of them. When the VI is executed, dataflow occurs on the block diagram through the nodes and the wires that connect them. The data flow ends at the front panel objects, which are essentially nodes with only one terminal, and the data is either displayed or logged.

The Labview Supervisory control program for the current application consists of two separate programs

1. Thermocouple Reader with SCXI-1112
2. Read Data and Write onto Spreadsheet

The following subsections describe these programs in greater detail.

4.3 Thermocouple Reader with SCXI-1112

The VI acquires thermocouple data from an SCXI-1112 amplifier module, averages it, linearizes it, and graphs it on a strip chart. This VI also enables the auto-zero feature of the SCXI-1112 that grounds the inputs. The amplifiers are zeroed and an offset reading is taken. These offsets (which occur due to temperature drift) are then subtracted from subsequent voltage readings. The program also writes a record, including a time stamp string and an array of single-precision numbers, to a datalog file for future reference and analysis.
4.3.1 Front Panel Description

The front panel of the thermocouple reader with SCXI-1112.vi is the user interface, to control the various options such as scan rate and number of samples to average for each data point. The Figure 4-1 is a snapshot of the front panel interface. We now discuss the various Icons, their utility and the syntax for varying their functionality.

- **Cold junction channel**: The cold junction channel specifies the channel string to use when reading the cold junction temperature. By default, this example reads the temperature sensor on the SCXI terminal block.
  
The syntax for the SCXI temperature sensor string is:

  \[ OBn ! SCx ! MDy ! cjtemp \ a:b \]

  **Equation 4-1. SCXI Temperature Sensor String Syntax**

  Where

  - \( n \) is the onboard data acquisition channel
  - \( x \) is the SCXI chassis ID (from the config utility)
  - \( y \) is the SCXI slot number of the module
  - \( a \) is the first cjtemp channel of the SCXI range corresponding to analog channel \( a \)
  - \( b \) is the last cjtemp channel in the SCXI range corresponding to analog channel \( b \)

  The current application uses only one chassis \( n=0 \). Similarly the SCXI chassis ID is 1 (\( x=1 \)) and the SCXI –1112 module is inserted into the slot number 4 (\( y=4 \)) of the chassis. The SCXI-1112 has a cold junction temperature sensor for each of the analog input channels and is selected for the channels mentioned in the command string.
Figure 4-1. Front Panel of Thermocouple Reader with SCXI-1112
• **device(1)**: the number of the plug-in data acquisition device. In this case, it refers to the NI PCI-6036E 200 kS/s, 16-Bit, 16 Analog Input Multifunction DAQ card inserted into the PCI slot of the Supervisory PC.

• **Channels**: specifies the set of analog input channels for a group and task. The default input is channel 0.

• **Offset channels**: This is the auto zero channel string. This function shunts the inputs, takes a reading, and then restores the channel to its original configuration. This offset reading can be subtracted from subsequent voltage readings. Auto zero channels cannot be scanned at the same time as other analog input channels and must be in consecutive order.

• **scan rate**: the number of scans per second to acquire. The VI will collect the given number of scans and average them to produce each point that appears on the strip chart. The strip chart will be updated as follows:

\[
\text{(scan rate / number of samples to average)} \times \text{times per second}
\]

• **TC type (K)**: Specifies the thermocouple type used. The temperature conversion formula depends on the thermocouple type. K type thermocouples made of Chromel-Alumel metal combinations are used in our experiment.

• **CJC Sensor type**: The type of the temperature sensor(s) on the SCXI terminal blocks for the modules to be scanned. The VI will read the temperature sensor, and use it to perform cold-junction compensation for the thermocouple readings. The SCXI 1112 has thermistors.

• **Input limits in deg C (50 to 0 deg C)**: an array of clusters, of which each array element specifies the temperature range limits for the channel(s) in the corresponding element of the channels array. If high and low limits are specified, LabVIEW will select new gain settings based to achieve specified input temperature limits.
• **Number of samples to average for each data point:** This allows you to adjust how many samples the program will average together to generate each point on the strip chart.

• **Error out:** a cluster containing error information. If an error is indicated during program run, error out contains the information on the error. The General Error Handler utility VI is used to check the error at the end of your diagram. The error out cluster contains the following parameters:
  - **Status:** TRUE if an error has occurred.
  - **Code:** The error code associated with an error. A value of 0 means no error, a negative value is an error, and a positive value is a warning.

• **Source:** an indication of where an error occurred, usually the name of the VI.

• **Latest temperature data:** An array containing the last temperature read from each input channel.

• **STOP:** This button is pushed to stop the acquisition.

• **Temperature Strip chart:** (Celsius) plots temperature as a function of time.

### 4.3.2 Block Diagram Description

Before the acquisition is configured, the SCXI module is reset with the Device Reset VI to ensure that the driver knows the gain settings on the module. During the acquisition process, this VI reads the CJC (Cold-Junction Compensation) voltage along with the other channels so that the temperature readings will stay accurate over time.
Figure 4-2. Block diagram of Thermocouple Reader with SCXI-1112
Several readings are taken from the sensor on your SCXI terminal block - indicated by the cold junction channel string. These readings are averaged to yield one value and passed to the next sequence. The program averages many samples for each data point to reduce noise in the temperature signal. This technique is recommended when you are acquiring data from slowly varying input signals. The inter channel delay is the time between any two consecutive channels within a scan. By default, LabView will determine a correct inter channel delay based on the SCXI gain and filter settings.

4.3.2.1. List of Sub VI’s in the Block diagram and their Functions

1. **AI Config.vi**: Configures an analog input operation for a specified set of channels. This VI configures the hardware and allocates a buffer for analog input operation.

2. **AI Start.vi**: Starts a buffered analog input operation. This VI sets the scan rate, the number of scans to acquire and the trigger conditions. The VI then starts acquisition.

3. **Mean.vi**: Computes the mean (average) (µ) of the values in the input sequence X.

4. **AI Clear.vi**: Clears the analog input task associated with taskID input.

5. **Device Reset.vi**  Resets either an entire device or the particular function identified by task ID.
6. **Convert Temp Range to Volt Range.vi** This VI converts a temp range and converts it to the approximate maximum voltage range for the given thermocouple type and temperature range.

7. **Acquire and Average.vi**: Averages the sampled data based on scan rate, inter channel delay and number of samples to average.

8. **Convert Thermocouple Reading.vi**: Converts a voltage read from a thermocouple into a temperature value.

9. **AI Read.vi** Reads data from a buffered analog input data acquisition.

### 4.4 Read Data and Write onto Spreadsheet

This VI reads one record at a time from the datalog file, written by the thermocouple reader with SCXI-1112.vi program, until all values are read. The record in the datalog is essentially a cluster containing a string and an array of single-precision numbers. The record is then separated into measured temperature values and their corresponding time stamps to observe the transient thermal responses. The record is also converted into a text string with tabs as delimiters and stored as a text file for access with spreadsheet programs such as excel. We shall look at the block diagram and the front panel in greater detail.

#### 4.4.1 Front Panel Description

The front panel acts as the user interface to read the datalog file. An important feature incorporated in the program is the capability to read one data at a time from the Datalog file using the STEP function. If the STEP function is ON then the data is read sequentially with every click on the NEXT RECORD key. The date and time string along with the present set of Data is also displayed. We will now look into the various Icons and their functions in greater detail.
• **STOP:** Stop reading records.

• **Step:** Allows Choice between Progressive scan of records by hitting Next record and continuous scan of all records without user input.

• **Next Record:** If Step is enabled, reads the next record in the datalog file if pressed by the user.

• **Format:** Input to the write to spreadsheet file VI. Format specifies how to convert the characters to numbers; the default is %. 3f.

• **Time format String:** Enables output of Time/ date string in required format

• **Waveform Chart:** Progressively plots the temperature records as a function of time.

• **Empty array:** latest temperature data an array displaying the last temperature read from each input channel.
Figure 4-3. Front Panel of Read data and write onto a spreadsheet. Vi
4.4.2 Block Diagram Description

The datalog file is opened and the data is read continuously or progressively based on user input. It is then written or appended onto a spreadsheet for further computing.

4.4.2.1. List of Sub VI’s

1. **General Error Handler.vi** Determines whether an error has occurred. If an error has occurred, this VI creates a description of the error and displays a dialog box.

2. **Write To Spreadsheet File.vi**: Converts a 2D or 1D array of single-precision (SGL) numbers to a text string and writes the string to a new byte stream text file readable by most spreadsheet applications.

3. **File dialog.vi**: Locates the required file based on file refnum.

4. **Open File.vi**: Opens the file specified by file path for reading and/or writing.

5. **Read File.vi**: Reads data from the file specified by refnum and returns it in data.

6. **Close File.vi**: Closes the specified refnum and returns the path to the file associated with the refnum.
Figure 4-4. Block diagram of Read data and write onto a spreadsheet. Vi.
Chapter 5 Tests, Results and their Analysis

5.1 Introduction to Chapter 5

The majority of the original equipment manufacturers (OEM) within the microprocessor industry would like to achieve the required thermal design power for current and future microprocessors by extending the application of forced convection air-cooling technologies. This is due to the fact that air-cooling is the simplest of solutions requiring just a fan and a heat sink with extruded fins. Air-cooling also has minimal impact on system design and compliance requirements [15]. The first part of chapter 5 presents the tests conducted as a part of this thesis to extend forced convection air-cooling, the results obtained and their analysis.

The second part of chapter 5 is on the results obtained with the simulated aluminum block 50-watt load. To restate, the objective of the experiment is to calibrate the error percentage of the calorimetric system with a known heat load. The experiment also characterizes the performance of the bulk Peltier cooler in terms of its COP and efficiency. These results are vital in measuring the heat dissipated by the processor.

The next sub-section of the chapter 5 is a discussion on the processor heat dissipation results obtained from the calibrated calorimetric system. The tests are run for both the normal and the over clocking cases to simulate multiple processors under testing and to directly exhibit enhanced processor performance by over clocking. In this test scenario, the Peltier module independently cools the processor.

The final part of the chapter deals with the test results obtained with the TFST module integrated with the heat sink and mounted on the processor hot spot. The objectives of this test are multifold.

1. To prove that we have accurately identified the processor hot spot and show that the TFST module has immediate effect on the hot spot cooling.
2. To ensure reliable processor operation during startup and when running real time applications like the SPEC CPU 2000 benchmarks
3. To monitor the hot spot temperatures during the entire test run to show a direct relationship between processor task and corresponding changes at the hot spot.

We shall now look at the results from the various setups and their analysis.
5.2 Forced Convection Air-cooling Extension.

From the discussion in section 1.2 we understand that the heat transfer is dependent on the temperature difference between the sink and the ambient air. By increasing the sink temperature by a thermoelectric module placed at the interface of the processor and the heat sink, we increase the magnitude of heat transfer from the heat sink. There is a counter argument that, the added power dissipated by the thermoelectric device (the new resulting Power value $P_{\text{Total}} = P_{\text{processor}} + P_{\text{TFST}}$) will counteract the benefits of the increased sink temperature. But with a TFST cooling device of high COP and ZT values, the resulting improvement in heat sink efficiency overcomes the marginal increase in power due to that dissipated by the TFST.

To further substantiate the argument, I performed the following set of measures.
1. Subject the Pentium III 860MHz processor to vigorous thermal stress tests. Under-clock and over-clock the processor to simulate multiple Device Under Test (D.U.T).
2. The aim of the tests is to seek regions of stable $\Delta T$ operation at varying processor frequencies. Another important goal of these tests is to test the thermal design of the processor and the boundary conditions at which it fails.
3. Extract the processor surface temperature by placing thermocouples in the interface of the heat sink and the CPU and on the ambient. To accomplish this, mill a small groove of 1 mm width and 1 mm depth in the heat sink to accommodate the leads.
4. Fix the thermocouple to the heat sink using Kapton tape and heat sink compound and place it exactly over the hottest spot on the processor.
5. Run tests at various processor frequencies attained by varying the FSB frequency.
6. Run the CPU at maximum percentile usage by using a simple CPU-BURN in software. Observe the response of the system to sudden CPU cooling failure, by removing the cooling fan.
In the under clocking and the normal clocking test runs, i.e. 567.9 MHz, the 705.4 MHz and the 858.5 MHz, the processor operation stabilizes after a period of test run. Observe that the temperature as measured across the interface reaches a stable value and the temperature curve flattens out. In this case, the system does not shutdown, but continues to run uninterrupted.

In the case of over clocking, the processor was run at the maximum capable frequency due to over clocking i.e. topmost curve (1139 MHz). This was done to test the extreme scenario and to have an idea of the heat dissipation of higher end-processors operating at similar frequencies. The system crashed at 64°C after 10mins and 15sec of test run. This maybe due to the fact that some spots on the processor reached critical temperatures causing the system to crash.

The test was continued for another 5 minutes. The interface temperature was monitored during this time. The interface temperature continued to increase during this time at the same rate. This indicates that the processor continues to draw power or the die...
is subject to additional heating due to the thermal momentum, even after the system crashes. This shows a significant failure in Pentium cooling methodology, wherein the processor die in subject to increasing temperatures beyond the critical shutdown temperature.

On close examination of the normal clocking (normal frequency of operation of the processor) test run, steady state functioning of the processor at a maximum temperature of 74°C is observed as seen in Figure 5-2. This run is crucial to the implementation of thermoelectric cooling as a method to extend forced convection air-cooling to future generations of processors.

![Figure 5-2 Normal processor clocking on-die and interface temperatures](image)

We observe that the interface temperature (between the processor and the heat sink) that acts as the input temperature to the heat sink is 78.43°C. So if the input temperature to the heat sink can be maintained at 78.43°C whereas the top of the processor in contact with the TE is maintained at the ambient temperature (25°C), We can completely remove all convectional cooling systems since the heat sink would be able to dissipate the entire heat.
load due to the higher $\Delta T = (78.43^\circ C - 25^\circ C = 53.43^\circ C$) This $\Delta T$ value can be reduced by better heat sink construction or implementation of heat pipe cooling.

The following diagram further explains this:

![Figure 5-3. Schematic of convectional cooling extension using TEC](image)

**5.3 Simulated Aluminum Block 50-Watt load**

These results are based on the setup described in section 3.2. The following list highlights the parameters measured and parameters, which were calculated:

1. Load voltage and load current supplied to the simulated 50-watt aluminum block. These values are used to calculate the power drawn by the heater block which is used to calibrate the calorimetric system.
2. The TEC voltage and the TEC current which are used to calculate the power drawn by the Peltier cooler to perform the required cooling.
3. The flow rate of the cooling water, which is used to calculate the heat absorbed by it.

Please refer to section 3.2 for the thermocouple measurements.

The initial conditions were noted with the TEC and the heater load switched off. Then the voltage supplied to the heater load was varied to simulate the processor under different stress and load conditions. The TEC was first switched off and the heater load temperature was allowed to rise until a steady $\Delta T$ is measured across the TEC. Then TEC
was powered on and the current supplied was slowly increased until the heater load temperature drops to a value around the ambient temperature.

The results from the experiment are shown as a Tabular column.

Measured Values

<table>
<thead>
<tr>
<th>Load Voltage (volts)</th>
<th>Load Current (amps)</th>
<th>TEC voltage (volts)</th>
<th>TEC Current (amps)</th>
<th>Inlet Supply (TC0) °C</th>
<th>Outlet Return (TC1) °C</th>
<th>TEC cold side (TC2) °C</th>
<th>TEC hot side (TC3) °C</th>
<th>Heater Block (TC4) °C</th>
<th>Flow rate (l/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heater load increased incrementally. TEC initially switched off until steady state temp is achieved. Tec is then powered on and progressively increased to bring heater block back to ambient temp</td>
<td>32.7</td>
<td>0.1</td>
<td>TEC OFF</td>
<td>23.09</td>
<td>23.31</td>
<td>22.98</td>
<td>22.78</td>
<td>25.15</td>
<td>2</td>
</tr>
<tr>
<td>32.7</td>
<td>0.1</td>
<td>0.306</td>
<td>0.43</td>
<td>22.57</td>
<td>22.59</td>
<td>20.85</td>
<td>21.04</td>
<td>20.85</td>
<td>2</td>
</tr>
<tr>
<td>53.2</td>
<td>0.2</td>
<td>TEC OFF</td>
<td>22.35</td>
<td>22.39</td>
<td>22.53</td>
<td>27.29</td>
<td>27.18</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>53.2</td>
<td>0.2</td>
<td>0.535</td>
<td>0.92</td>
<td>21.85</td>
<td>21.93</td>
<td>21.76</td>
<td>22.07</td>
<td>21.66</td>
<td>2</td>
</tr>
<tr>
<td>80.1</td>
<td>0.3</td>
<td>TEC OFF</td>
<td>21.86</td>
<td>22.11</td>
<td>34.03</td>
<td>22.18</td>
<td>33.98</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>80.1</td>
<td>0.3</td>
<td>1.094</td>
<td>1.97</td>
<td>21.59</td>
<td>21.76</td>
<td>22.29</td>
<td>22.26</td>
<td>22.36</td>
<td>2</td>
</tr>
<tr>
<td>100.3</td>
<td>0.36</td>
<td>TEC OFF</td>
<td>21.97</td>
<td>22.19</td>
<td>39.71</td>
<td>22.85</td>
<td>39.97</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>100.3</td>
<td>0.36</td>
<td>1.798</td>
<td>3.14</td>
<td>22.3</td>
<td>22.62</td>
<td>21.95</td>
<td>23.49</td>
<td>22.17</td>
<td>2</td>
</tr>
<tr>
<td>112.5</td>
<td>0.4</td>
<td>TEC OFF</td>
<td>22.11</td>
<td>22.47</td>
<td>43.07</td>
<td>23.43</td>
<td>43.39</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>112.5</td>
<td>0.4</td>
<td>2.22</td>
<td>3.94</td>
<td>21.73</td>
<td>21.97</td>
<td>21.78</td>
<td>23.09</td>
<td>22.08</td>
<td>3</td>
</tr>
<tr>
<td>120</td>
<td>0.42</td>
<td>TEC OFF</td>
<td>23.61</td>
<td>23.88</td>
<td>46.2</td>
<td>24.78</td>
<td>46.57</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>120</td>
<td>0.42</td>
<td>2.628</td>
<td>4.65</td>
<td>21.57</td>
<td>21.87</td>
<td>21.79</td>
<td>23.22</td>
<td>22.06</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 1. Measured values from simulated load tests
5.3.1 Sample Calculations for Calorimetric Measurement

Heat drawn by coolant water is given as:

\[
\frac{dQ}{dT} = \dot{m} \cdot c_p (T_{\text{Outlet}} - T_{\text{Inlet}})
\]

Equation 5-1. Heat drawn by coolant water

Where \( \dot{m} \) = mass flow rate (or) mass flux (Kg/sec)

\( \dot{m} = \) Volume flow rate (measured) x Density of water

\( \dot{m} = \) liters/minute x kilograms/liter

\( \dot{m} = \) Kg/minute (If divided by 60secs we get kg/sec.)

cp: - specific heat of water at constant pressure (1Btu/lbm. °F)

The conversion factor into SI units is \( 4.1868 \times 10^3 \) (Joules/ Kg. K)

Performing the calculations for the selected case.

\[
\frac{dQ}{dT} = \dot{m} \cdot c_p (T_{\text{Outlet}} - T_{\text{Inlet}})
\]

\( \dot{m} = 3 \) liters/minute x 1000 gm /liter x 4.1868 Joules/ Kg. K x (21.87 – 21.57)

\( \dot{m} = 3768.12 \) joules/minute

\( \dot{m} = 62.802 \) joules/sec = 62.8 watts.

5.3.2 Graphs and Discussion of Results

![Graph](TEC-Power-vs-deltaT.png)

Figure 5-4. TEC input Power VS Delta T across TEC.
Figure 5-4 plots TEC power supplied Vs the delta T across the TEC. The delta T is measured as the maximum temperature difference developed across the hot side and the cold side of the TEC, for a given input load to the aluminum block when the TEC is switched off. The TEC is then switched ON and its input power is progressively increased until the aluminum block is cooled to ambient temperature. From the graph we observe that as the delta T across the device increases, more input power is required to cool the load.

![Aluminum Load Vs Delta T](image)

**Figure 5-5. Aluminum block load Vs. Delta T**

Figure 5-5 plots the input to the aluminum block as a function of delta T across the TEC in an approximately linear relationship as expected. The graph shows that for increasing loads, the TEC needs to be work harder to cool the aluminum block and bring it back to ambient temperature.

Figure 5-6 plots the difference in temperature across the inlet water supply and the outlet return as a function of the total power dissipated by the system. It is seen that this relationship is also approximately linear as expected.
Figure 5-6. Delta T across water Vs Total power dissipated.

Figure 5-7. COP and Power of TEC Vs Input load.

Figure 5-7 plots the COP of the TEC and the input power to the TEC as a function of the input load to the aluminum block. It is observed that as the delta T across the TEC increases, the COP reduces and settles to a more nominal value approximately equal to four. The graph compares the required TEC power to cool a given value of input load. For example, it requires 12.2 watts to cool a 50.4-watt heat load to ambient temperature, giving a COP value of 4.1.
Table 2 shows the calorimetric value as calculated from the measured values of delta T across the inlet and outlet water lines and the flow rate. The difference between this calorimetric value and the actual total power supplied to the system is used to calibrate the accuracy of the system. Observe that the error percentage never exceeds 10% and also values less than 1% are obtained. This substantiates the argument that the calorimetric system can measure within ±3 watts of the actual power dissipated by the processor for a processor thermal design power of 30 watts. Also notice that the error percentage decreases with increasing load and the TEC input power resulting in a more accurate calorimetric system.

Table 2. Calculated values from simulated load tests

<table>
<thead>
<tr>
<th>Aluminum Load (watts)</th>
<th>TEC Power (watts)</th>
<th>Total Power (watts)</th>
<th>Calorimetric value calculated (watts)</th>
<th>Difference in Input and measured (watts)</th>
<th>Error Percentage (%)</th>
<th>COP of TEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.64</td>
<td>0.49</td>
<td>11.13</td>
<td>11.16</td>
<td>-0.0326</td>
<td>-0.29</td>
<td>21.61</td>
</tr>
<tr>
<td>24.03</td>
<td>2.15</td>
<td>26.18</td>
<td>23.72</td>
<td>2.45998</td>
<td>9.39</td>
<td>11.14</td>
</tr>
<tr>
<td>36.10</td>
<td>5.64</td>
<td>41.75</td>
<td>44.65</td>
<td>-2.904</td>
<td>-6.95</td>
<td>6.39</td>
</tr>
<tr>
<td>45</td>
<td>8.74</td>
<td>53.74</td>
<td>50.24</td>
<td>3.5052</td>
<td>6.52</td>
<td>5.14</td>
</tr>
<tr>
<td>50.4</td>
<td>12.22</td>
<td>62.62</td>
<td>62.8</td>
<td>-0.1818</td>
<td>-0.29</td>
<td>4.12</td>
</tr>
</tbody>
</table>

5.4 Processor cooling with independent Peltier module

This section presents results obtained for the experimental setup discussed in Section 3.3. I attempt to calculate the processor power at two different frequencies (860 MHz and 995 MHz). The higher frequency is obtained by over clocking the processor by varying its Front Side Bus (FSB). This serves two purposes.

- Exhibit increased processor performance by measuring the processor runtime while running the SPEC CPU2000 benchmarks.
- Exhibit the characteristics of the calorimetric system by testing multiple processors.

The overclocking case is assumed to be a separate processor rated for that frequency. We shall now discuss the results obtained for the Normal and the Overclocking cases in the following sub-sections

### 5.4.1 Normal Clocking (860 MHz)

The processor was clocked at its normal operational frequency and the power dissipated from it was calculated using calorimetric measurements. The Table 3 contains the measured and Table 4 contains the calculated values.

**Table 3. Measured values under processor normal clocking case**

<table>
<thead>
<tr>
<th>Processor On-die Temp °C</th>
<th>Inlet/Supply (TC0) °C</th>
<th>Outlet/Return (TC1) °C</th>
<th>Coldside (TC2) °C</th>
<th>Hotside (TC3) °C</th>
<th>Flowrate (litres/min)</th>
<th>TEC voltage (Volts)</th>
<th>TEC Current (Amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>28.31</td>
<td>28.44</td>
<td>37.13</td>
<td>28.69</td>
<td>1.58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>30.39</td>
<td>30.53</td>
<td>37.2</td>
<td>37.73</td>
<td>1.58</td>
<td>0.068</td>
<td>0.25</td>
</tr>
<tr>
<td>61</td>
<td>31.59</td>
<td>31.74</td>
<td>36.64</td>
<td>31.89</td>
<td>1.58</td>
<td>0.173</td>
<td>0.5</td>
</tr>
<tr>
<td>61</td>
<td>32.41</td>
<td>32.57</td>
<td>35.93</td>
<td>33.75</td>
<td>1.58</td>
<td>0.411</td>
<td>0.75</td>
</tr>
<tr>
<td>59</td>
<td>32.91</td>
<td>33.08</td>
<td>34.9</td>
<td>33.28</td>
<td>1.58</td>
<td>0.662</td>
<td>1</td>
</tr>
<tr>
<td>59</td>
<td>33.29</td>
<td>33.47</td>
<td>33.77</td>
<td>33.69</td>
<td>1.58</td>
<td>0.889</td>
<td>1.25</td>
</tr>
<tr>
<td>58</td>
<td>33.58</td>
<td>33.76</td>
<td>32.57</td>
<td>33.98</td>
<td>1.58</td>
<td>1.121</td>
<td>1.5</td>
</tr>
<tr>
<td>64</td>
<td>33.85</td>
<td>34.06</td>
<td>33.18</td>
<td>34.4</td>
<td>1.58</td>
<td>1.299</td>
<td>1.75</td>
</tr>
<tr>
<td>64</td>
<td>34.14</td>
<td>34.36</td>
<td>32.05</td>
<td>34.69</td>
<td>1.58</td>
<td>1.522</td>
<td>2</td>
</tr>
<tr>
<td>60</td>
<td>34.32</td>
<td>34.56</td>
<td>31.24</td>
<td>34.95</td>
<td>1.58</td>
<td>1.755</td>
<td>2.25</td>
</tr>
<tr>
<td>63</td>
<td>34.52</td>
<td>34.77</td>
<td>29.98</td>
<td>35.15</td>
<td>1.58</td>
<td>1.975</td>
<td>2.5</td>
</tr>
<tr>
<td>55</td>
<td>34.65</td>
<td>34.89</td>
<td>27.51</td>
<td>35.25</td>
<td>1.58</td>
<td>2.243</td>
<td>2.75</td>
</tr>
<tr>
<td>52</td>
<td>31.9</td>
<td>32.15</td>
<td>23.66</td>
<td>32.59</td>
<td>1.58</td>
<td>2.373</td>
<td>3</td>
</tr>
<tr>
<td>52</td>
<td>33.4</td>
<td>33.66</td>
<td>23.83</td>
<td>34.07</td>
<td>1.58</td>
<td>2.672</td>
<td>3.25</td>
</tr>
<tr>
<td>52</td>
<td>34.06</td>
<td>34.34</td>
<td>23.49</td>
<td>33.84</td>
<td>1.58</td>
<td>2.826</td>
<td>3.5</td>
</tr>
<tr>
<td>52</td>
<td>32.65</td>
<td>32.94</td>
<td>21.36</td>
<td>33.59</td>
<td>1.58</td>
<td>3.079</td>
<td>3.75</td>
</tr>
</tbody>
</table>

The Calorimetric measure is calculated as per the Equation 5-1 is computed and the processor power is then calculated by subtracting the input power to the TEC.
<table>
<thead>
<tr>
<th>Delta T across water °C</th>
<th>Delta T across TEC °C</th>
<th>TEC Power (watts)</th>
<th>Calorimetric Measure (watts)</th>
<th>Processor Power (watts)</th>
<th>COP</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.13</td>
<td>-8.44</td>
<td>14.32</td>
<td>14.32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.14</td>
<td>0.53</td>
<td>0.017</td>
<td>15.42</td>
<td>15.40</td>
<td>906.35</td>
</tr>
<tr>
<td>0.15</td>
<td>-4.75</td>
<td>0.086</td>
<td>16.52</td>
<td>16.44</td>
<td>190.06</td>
</tr>
<tr>
<td>0.16</td>
<td>-2.18</td>
<td>0.308</td>
<td>17.62</td>
<td>17.32</td>
<td>56.18</td>
</tr>
<tr>
<td>0.17</td>
<td>-1.62</td>
<td>0.662</td>
<td>18.73</td>
<td>18.06</td>
<td>27.29</td>
</tr>
<tr>
<td>0.18</td>
<td>-0.08</td>
<td>1.111</td>
<td>19.83</td>
<td>18.72</td>
<td>16.84</td>
</tr>
<tr>
<td>0.18</td>
<td>1.41</td>
<td>1.681</td>
<td>19.83</td>
<td>18.15</td>
<td>10.79</td>
</tr>
<tr>
<td>0.21</td>
<td>1.22</td>
<td>2.273</td>
<td>23.13</td>
<td>20.86</td>
<td>9.17</td>
</tr>
<tr>
<td>0.22</td>
<td>2.64</td>
<td>3.044</td>
<td>24.23</td>
<td>21.19</td>
<td>6.96</td>
</tr>
<tr>
<td>0.24</td>
<td>3.71</td>
<td>3.948</td>
<td>26.44</td>
<td>22.49</td>
<td>5.69</td>
</tr>
<tr>
<td>0.25</td>
<td>5.17</td>
<td>4.93</td>
<td>27.54</td>
<td>22.60</td>
<td>4.57</td>
</tr>
<tr>
<td>0.24</td>
<td>7.74</td>
<td>6.168</td>
<td>26.44</td>
<td>20.27</td>
<td>3.28</td>
</tr>
<tr>
<td>0.25</td>
<td>8.93</td>
<td>7.119</td>
<td>27.54</td>
<td>20.42</td>
<td>2.86</td>
</tr>
<tr>
<td>0.26</td>
<td>10.24</td>
<td>8.684</td>
<td>28.64</td>
<td>19.96</td>
<td>2.29</td>
</tr>
<tr>
<td>0.28</td>
<td>10.35</td>
<td>9.891</td>
<td>30.85</td>
<td>20.95</td>
<td>2.119</td>
</tr>
<tr>
<td>0.29</td>
<td>12.23</td>
<td>11.546</td>
<td>31.95</td>
<td>20.40</td>
<td>1.76</td>
</tr>
</tbody>
</table>

Figure 5-8. Processor on-die temperature Vs TEC input power (normal clocking)
Figure 5-8 is a plot of the processor on-die temperature Vs the TEC input power. It is seen that the processor temperature decreases for increasing values of TEC input power.

![Graph showing processor on-die temperature vs TEC input power.](image)

**Figure 5-9. Processor power calculated vs TEC input power (normal clocking)**

Figure 5-9 plots the processor power Vs input TEC power. It is seen that processor power, as calculated by the calorimetric measurements remains constant, even though the TEC power increases. This substantiates the conclusion that the processor is dissipating around 20 Watts. This value may have an error of less than 10% as per the error percentage calculated in section 5.3. This error is most likely to be on the positive side due to the lack of complete thermal insulation around the processor and its heat spreader, which causes some amount of heat to be lost to the ambient.
### 5.4.2 Processor over clocking (995MHz)

The Tables for measured and calculated values along with the graph plots are shown.

**Table 5. Measured values under processor over clocking case**

<table>
<thead>
<tr>
<th>Processor On-die Temp °C</th>
<th>Inlet/Supply (TC0) °C</th>
<th>Outlet/Return (TC1) °C</th>
<th>Cold side (TC2) °C</th>
<th>Hot side (TC3) °C</th>
<th>Flow rate (liters/min)</th>
<th>TEC voltage (Volts)</th>
<th>TEC Current (Amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>33</td>
<td>25.68</td>
<td>25.61</td>
<td>27.03</td>
<td>25.69</td>
<td>1.58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>27.4</td>
<td>27.46</td>
<td>36.15</td>
<td>27.88</td>
<td>1.58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>29.77</td>
<td>29.94</td>
<td>39.76</td>
<td>30.31</td>
<td>1.58</td>
<td>0.192</td>
<td>0.25</td>
</tr>
<tr>
<td>68</td>
<td>31.3</td>
<td>31.48</td>
<td>37.99</td>
<td>31.88</td>
<td>1.58</td>
<td>0.112</td>
<td>0.5</td>
</tr>
<tr>
<td>67</td>
<td>32.35</td>
<td>32.55</td>
<td>37.41</td>
<td>32.89</td>
<td>1.58</td>
<td>0.354</td>
<td>0.75</td>
</tr>
<tr>
<td>66</td>
<td>33.05</td>
<td>33.26</td>
<td>36.48</td>
<td>33.59</td>
<td>1.58</td>
<td>0.599</td>
<td>1</td>
</tr>
<tr>
<td>64</td>
<td>33.57</td>
<td>33.82</td>
<td>35.45</td>
<td>35.13</td>
<td>1.58</td>
<td>0.838</td>
<td>1.25</td>
</tr>
<tr>
<td>65</td>
<td>31.8</td>
<td>32.06</td>
<td>32.83</td>
<td>32.43</td>
<td>1.58</td>
<td>1.021</td>
<td>1.5</td>
</tr>
<tr>
<td>59</td>
<td>33.01</td>
<td>33.27</td>
<td>31.23</td>
<td>33.57</td>
<td>1.58</td>
<td>1.323</td>
<td>1.75</td>
</tr>
<tr>
<td>58</td>
<td>33.64</td>
<td>33.9</td>
<td>30.4</td>
<td>34.21</td>
<td>1.58</td>
<td>1.558</td>
<td>2</td>
</tr>
<tr>
<td>56</td>
<td>32.45</td>
<td>32.68</td>
<td>27.83</td>
<td>33.02</td>
<td>1.58</td>
<td>1.77</td>
<td>2.25</td>
</tr>
<tr>
<td>56</td>
<td>33.46</td>
<td>33.71</td>
<td>27.49</td>
<td>34.05</td>
<td>1.58</td>
<td>2.006</td>
<td>2.5</td>
</tr>
<tr>
<td>64</td>
<td>31.99</td>
<td>32.28</td>
<td>27.38</td>
<td>32.85</td>
<td>1.58</td>
<td>2.136</td>
<td>2.75</td>
</tr>
<tr>
<td>58</td>
<td>33.36</td>
<td>33.63</td>
<td>26.13</td>
<td>34.1</td>
<td>1.58</td>
<td>2.41</td>
<td>3</td>
</tr>
<tr>
<td>57</td>
<td>31.91</td>
<td>32.2</td>
<td>23.92</td>
<td>33.03</td>
<td>1.58</td>
<td>2.614</td>
<td>3.25</td>
</tr>
<tr>
<td>57</td>
<td>33.34</td>
<td>33.65</td>
<td>23.74</td>
<td>34.17</td>
<td>1.58</td>
<td>2.845</td>
<td>3.5</td>
</tr>
<tr>
<td>59</td>
<td>32.37</td>
<td>32.7</td>
<td>28.28</td>
<td>33.34</td>
<td>1.58</td>
<td>3.03</td>
<td>3.75</td>
</tr>
<tr>
<td>59</td>
<td>33.41</td>
<td>33.79</td>
<td>22.59</td>
<td>34.43</td>
<td>1.58</td>
<td>3.25</td>
<td>4</td>
</tr>
<tr>
<td>58</td>
<td>33.76</td>
<td>34.16</td>
<td>21.07</td>
<td>32.43</td>
<td>1.58</td>
<td>3.41</td>
<td>4.25</td>
</tr>
</tbody>
</table>

**Figure 5-10. Processor on-die temperature Vs TEC input power (over clocking)**
Figure 5-10 is a plot of the processor on-die temperature vs the TEC input power. It is seen as before that the processor temperature decreases for increasing values of TEC input power. The graph shows a small increase in processor temperature towards the end of the curve, This is the point where the benchmark starts the peak runs which are more compute intensive after completion of the SPEC Base line runs. This accounts for the increase in CPU temperature and also the increased power dissipation values.

Table 6. Calculated values under processor over clocking case

<table>
<thead>
<tr>
<th>Delta T across Water °C</th>
<th>Delta T across TEC °C</th>
<th>TEC Power (watts)</th>
<th>Calorimetric measure (watts)</th>
<th>Processor Power (watts)</th>
<th>COP</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.07</td>
<td>-1.34</td>
<td>-7.71</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.06</td>
<td>-8.27</td>
<td>6.610</td>
<td>6.61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.17</td>
<td>-9.45</td>
<td>0.04</td>
<td>18.73</td>
<td>18.68</td>
<td>389.21</td>
</tr>
<tr>
<td>0.18</td>
<td>-6.11</td>
<td>0.05</td>
<td>19.83</td>
<td>19.77</td>
<td>353.14</td>
</tr>
<tr>
<td>0.2</td>
<td>-4.52</td>
<td>0.26</td>
<td>22.03</td>
<td>21.77</td>
<td>81.99</td>
</tr>
<tr>
<td>0.21</td>
<td>-2.89</td>
<td>0.59</td>
<td>23.13</td>
<td>22.53</td>
<td>37.62</td>
</tr>
<tr>
<td>0.25</td>
<td>-0.32</td>
<td>1.04</td>
<td>27.54</td>
<td>26.49</td>
<td>25.29</td>
</tr>
<tr>
<td>0.26</td>
<td>-0.4</td>
<td>1.53</td>
<td>28.64</td>
<td>27.11</td>
<td>17.70</td>
</tr>
<tr>
<td>0.26</td>
<td>2.34</td>
<td>2.31</td>
<td>28.64</td>
<td>26.33</td>
<td>11.37</td>
</tr>
<tr>
<td>0.26</td>
<td>3.81</td>
<td>3.11</td>
<td>28.64</td>
<td>25.53</td>
<td>8.19</td>
</tr>
<tr>
<td>0.23</td>
<td>5.19</td>
<td>3.98</td>
<td>25.34</td>
<td>21.35</td>
<td>5.36</td>
</tr>
<tr>
<td>0.25</td>
<td>6.56</td>
<td>5.01</td>
<td>27.54</td>
<td>22.52</td>
<td>4.49</td>
</tr>
<tr>
<td>0.29</td>
<td>5.47</td>
<td>5.87</td>
<td>31.95</td>
<td>26.07</td>
<td>4.43</td>
</tr>
<tr>
<td>0.27</td>
<td>7.97</td>
<td>7.23</td>
<td>29.74</td>
<td>22.51</td>
<td>3.11</td>
</tr>
<tr>
<td>0.29</td>
<td>9.11</td>
<td>8.49</td>
<td>31.95</td>
<td>23.45</td>
<td>2.76</td>
</tr>
<tr>
<td>0.31</td>
<td>10.43</td>
<td>9.95</td>
<td>34.15</td>
<td>24.19</td>
<td>2.43</td>
</tr>
<tr>
<td>0.33</td>
<td>5.06</td>
<td>11.36</td>
<td>36.35</td>
<td>24.99</td>
<td>2.19</td>
</tr>
<tr>
<td>0.38</td>
<td>11.84</td>
<td>13</td>
<td>41.86</td>
<td>28.86</td>
<td>2.22</td>
</tr>
<tr>
<td>0.4</td>
<td>11.36</td>
<td>14.49</td>
<td>44.07</td>
<td>29.57</td>
<td>2.04</td>
</tr>
</tbody>
</table>
Figure 5-11 plots the processor power as calculated by the calorimetric measurements versus the TEC input power. As in the normal clocking case we see that the processor power remains constant, even though the TEC input power increases. The increase in power dissipation values towards the end of the curve is because the processor is running SPEC peak benchmarks which are more compute intensive than the base runs.

5.5 TFST module testing

The TFST module was mounted onto the processor as described in the section 3.4.2. The objective of the experiments is to ensure reliable processor operation and to analyze the transients in temperature at the processor hot spot during startup and normal operation.

To set the initial conditions for safe CPU startup, the TEC module was powered on at 2.5 Amps and 1.98 volts. This caused the entire system to cool with the copper heat spreader reaching a steady state temperature of 13.35 °C. The hot spot, which is at the interface between the processor and the cold side of the TFST, was however at 15.16 °C, since the TFST acts as a near insulator when switched off. The TFST module was then powered on at 1.5 Amps and 0.613 volts. This caused the hot spot temperature to lower by an additional 2 °C to reach steady state at 13.92°C. The system was then deemed safe for processor startup.
The CPU loads the operating system and various applications such as ASUS probe software to read the on-die temperature, and the command prompt to run the benchmarks. The benchmarks were then started and immediately the hot spot temperature rises up. When steady state was achieved, it was observed that the hot-spot temperature was at 40.53°C and the copper spreader temperature was at 30.90°C. So there exists a delta T of 9.63 between the hot spot and the rest of the surface of the processor. With a more efficient TFST module, with higher ZT value, we can possibly negate this temperature difference, thus totally removing the hot spot.
Figure 5-12. TFST module test results
5.5.1 TFST Module testing Analysis

One primary question arises in the testing with the integrated TFST module. Has the module been placed accurately at the hot spot on the processors die surface? We verify this from the following figure.

The left figure shows Windows Task manager program showing the current CPU usage percentile and the CPU usage history. The CPU is currently running the SPEC CPU usage benchmarks and is at maximum CPU usage percentile of 100%. However the CPU usage falls form this max value when it completes an iteration of a benchmark and moves onto the next iteration or when it completes one benchmark run and moves onto the next benchmark. We observe this in the CPU usage history when the CPU falls twice to values of around ~20% before reaching max value again.

The right figure shows the temperature of the hot spot as measured by the Labview supervisory control program. It is observed that the temperature read at the interface of the TFST module and the processor varies instantaneously with change in
processor load. From the results obtained in chapter 2 from the study of the processor die with IR images, we know that the hot-spot responds immediately to the processor load variations. Hence we can conclude that the TFST module has been placed accurately at the hot spot. We also observe that active cooling with the TFST module reduces the temperature at the hot spot immediately with fall in CPU usage percentile. This is not possible with passive heat spreaders such as the copper block placed over the rest of the processor die.

5.6 Discussion of results

The flow rate of the cooling water was decreased to reduce the effect of the convection cooling of the total system. This was done to evaluate more precisely the effect of the TFST module at the processor hot spot. The flow rate was calculated accurately by measuring the time it took to fill a 1-liter graduated cylinder. The flow rate was found to be 0.94 liters/minute.

Case 1.

TEC input: 2.147 volts 2.49 Amps => 5.346 watts
TFST input: 0.837 volts 1.99 Amps => 1.665 watts

Heat drawn by cooling water as per equation:
\[ \Delta T \times \text{flow rate (liters/minute)} \times 1000 \times 4.1868 /60 = \text{watts} \]
0.4 x 0.94 x 1000 x 4.1868 /60 = 26.237 watts

Power dissipated by processor:
Heat drawn by processor – (TFST power + TEC power)

This value is in agreement with CPU power dissipation calculation obtained in the tabular column for the normal clocking case.
Case 2:

TEC input: 1.12 volts 1.5 Amps => 1.68 watts
TFST input: 0.837 volts 1.99 Amps => 1.67 watts

Heat drawn by cooling water as per equation:
\[ \Delta T \times \text{flow rate (liters/minute)} \times 1000 \times 4.1868 / 60 = \text{watts} \]
\[ (31.37 – 31.04) \times 0.94 \times 1000 \times 4.1868 / 60 = 21.64 \text{ watts} \]

Power dissipated by processor:
Heat drawn by processor – (TFST power + TEC power)
21.64 – (1.67 + 1.68) = 18.29 watts.

This value is marginally less than the one obtained in case 1. This may be due to the slight reduction in processor load, which is also reflected in the 1°C drop in processor on-die temperature.

5.7 Chapter 5 Conclusion

In this chapter we have shown theoretically how forced convection air–cooling can be extended to cool higher end microprocessors by using TFST modules at the interface between the processor and the heat sink.

We designed and calibrated a calorimetric system, which can measure the power dissipated by the processor under real-time load conditions. Using this system we calculated the heat dissipated under both normal clocking and overclocking the processor.

We mounted the thin-film module onto the processor hot spot and ensured reliable processor operation. We accurately verified the location of the hotspot as observed under infrared images. We also monitored the temperature at the hot spot during processor start-up and when running applications. We analyzed and presented the thermal transients observed at the hot spot. Lastly we showed it appears reasonable that in the future with more efficient TFST modules with higher ZT values, it may be possible to remove the hot spot from the processor surface.
Chapter 6  Thesis Summary and Future Work

This chapter concludes the thesis, presenting once again the objectives that have motivated this work. I direct the reader towards further scientific enquiries and results which extend the ideas put forth in this thesis.

6.1 Thesis Summary

In this Thesis, a discussion of the current microprocessor trends in terms of thermal power design has been presented. We have exhibited the factors that determine the amounts of heat dissipated by the heat sink. We observed that forced convection air-cooling is subject to severe limitations in terms of heat sink weight and dimensions, acoustic noise of the cooling fan, fin dimensions and size etc.

We have reviewed the micro-architecture of the Intel Pentium III processor. We have also identified the individual architectural components, their location and their functions. Components that can be potential hot spots under specific stress or application load on the processor have been classified. We then studied IR images of the processor die during CPU startup and when an application is loaded after the CPU reaches steady state operation. We located the hotspot on the processor die and quantified its magnitude in terms of maximum temperature reached before the system crashes. We also studied the reasons for the occurrence of the hot spot.

A comprehensive review of the basics of thermoelectrics with the physical principles that govern their functioning was presented. The solid-state theory of superlattice structures, different types of phonon blocking and the science behind the RTI Thin-film superlattice structures was discussed. The thesis presented these superlattice structures as ideal solutions for localized, active cooling on processor die.

A calorimetric system was designed to accurately measure the power dissipated by the processor when it’s running real time applications such as the SPEC CPU 2000 benchmarks. The calorimetric system was calibrated and its error percentage was accurately determined. This was done by replacing the processor with a simulated 50-watt aluminum block, which was driven by a known value of current and voltage. The
various parameters involved in the setup, the importance and the precise locations for their measurement were listed. A secondary setup wherein the processor was independently cooled by a Peltier TEC cooler was designed. The amount of heat dissipated under both the normal and overclocking cases was measured. We also measured the efficiency and COP of the Peltier cooler and the increasing power input to the TEC for increasing processor loads.

We then mounted the thin-film module onto the processor hot spot and ensured reliable processor operation. We have accurately verified the location of these hotspots as observed under infrared images. We have also monitored the temperature at the hot spot during processor start-up and when running application. We have analyzed and presented the thermal transients observed at these hot spots.

6.2 Future Work

Foremost, the processor on which the tests were conducted was not the most ideal in terms of its thermal power design and hot spot magnitude. A more ideal choice would have been the 2GHz or greater Pentium 4 processor, which dissipates over 50watts of heat. Unfortunately the Pentium 4 die comes with a thermal interface material (TIM), which is basically a metal cap, placed over the die during the time of fabrication. This prevents direct access to the die and without means to identify the hot spots on the processor. I have not looked at the mobile Pentium processors mainly due to the excessive cost and the space limitations in the construction of the heats sinks. I would recommend repeating all the tests on a higher end processor such as the Pentium 4 with the die exposed.

Further work has to be done in terms of improvement in Thin-film superlattice thermoelectrics. In this case the module tested had a comparatively low ZT and so we did not repeat the testing for the overclocking case.
Bibliography

1. Ioan Sauciuc, Greg Chrysler, Ravi Mahajan, Michele Szleper  Air-Cooling Extension- Performance Limits for processor cooling Applications. 19th IEEE SEMI-Therm Symposium
2. Rama Venkatasubramanian, Edward Siivola, Thomas Colpitts & Brooks O’Quinn Thin-film thermoelectric devices with high room-temperature figures of merit
3. Intel Pressroom archives  
   http://www.intel.com/pressroom/archive/photos/p4_photos.htm
4. Sara Godfrey, Melcor Corporation  An introduction to thermoelectric coolers.
5. Andrew W. Batchelor, David McDonald, Ben Banney and Sam Dawkins, Hydrocool Pty. Ltd., Fremantle, Western Australia.  The application of thermoelectric heat pumps as a practical and energy efficient mode of refrigeration
7. Thermoelectric Fundamentals and Mathematical Modeling  Ferrotec-america  
   http://www.ferrotec-america.com/3ref.htm
8. R.C.Chu and R.E.Simons Applications of Thermoelectrics to Cooling Electronics
9. Cronin B. Vining Thermoelectric Fundamentals and Physical Phenomena  
   1993 ITS Short Course on Thermoelectricity Nov. 8, 1993 Yokohama, Japan
10. Rama Venkatasubramanian  Physics Rev B Volume 61, Num 4  
    Lattice Thermal conductivity reduction and phonon localization like behavior in superlattice structures.
12. L. Brillouin, Wave Propagation in Periodic Structures  
15. Ioan Sauciuc, Greg Chrysler, Ravi Mahajan, Ravi Prasher  
    Spreading in the Heat Sink Base: Phase Change Systems or Solid metals.  
    IEEE transactions on components and packaging Technologies Vol.25, No.4 DEC ’02
16. Glossary of Thermoelectric and Related Terms. FERROTEC  
    http://www.ferrotec-america.com/3refglos.htm
    http://www.tinkersguild.com/sample/SponsorAds/NatInstruments/labview_basics.htm


23. Anand Tech website - Source for Hardware Analysis and news 
   http://www.anandtech.com/
A-1 Appendix

The Standard Performance Evaluation Corporation (SPEC) is a nonprofit organization founded in 1988 to ensure fair, useful and standardized metrics for evaluating modern computer systems’ performance [14]. SPEC CPU2000 is a standardized CPU-intensive benchmark designed to provide a comparative measure of performance across the widest practical range of hardware. SPEC CPU2000 benchmarks are developed from real user applications. These benchmarks measure the performance of the processor, memory and compiler on the tested system.

SPEC CPU2000 is divided into two suites of benchmarks: SPECint and SPECfp. SPECint measures the integer performance of the tested system; word processing, file compression, e-mail and database performance fall into this category. SPECfp measures the floating-point performance of the tested system; audio encoding, certain spreadsheet calculations and 3D games are examples of floating-point applications.

SPEC focuses on two areas for evaluating CPU performance: SPECint_base/SPECint and SPECfp_base/SPECfp. SPECint_base and SPECint metrics indicate the baseline and peak levels of the CPU’s integer prowess, while SPECfp_base and SPECfp metrics indicate the CPU’s floating-point abilities. The baseline method specifies that all programs of the same language within suite be compiled the same way, with the same optimizations. SPEC sees this method reflecting the usage model of someone compiling his or her code using the compiler vendor’s recommendation for achieving better application performance knowing only the application language.

The second method, which is optional for SPEC reporting, is the non-baseline or peak method. This method allows each program to be compiled differently (even with different compilers). This reflects an environment where someone is willing to spend time testing different compilers and compilation options to get the best possible performance.
A-1.1 Reasons for SPEC Usage:

In microprocessor thermal management it is vital to exercise the processor under real time conditions to observe, characterize and solve the thermal problems. The SPEC benchmarks run the CPU at maximum usage percentile and at maximum values of thermal design power. So any hot spots across the thermal footprint of the die are exposed. Secondly, this serves as the most appropriate validation for the cooling system as it tests for reliable processor functioning under real time conditions and extreme stress scenarios.

Lastly, SPEC allows us to detect performance improvements if any, due to improved thermal management. Over clocking the processor, if the surface of the die can be maintained at the same temperature as the normal clocking case, can cause significant performance enhancement while alleviating the effects of over clocking. Due to lack of availability of a Digital FORTRAN Compiler, I have conducted tests only on the SPEC Integer benchmarks.