ABSTRACT

MARKS, JEFFERY EARL. SOI for Frequency Synthesis in RF Integrated Circuits. (Under the direction of Dr. Wentai Liu.)

The purpose of this research has been to explore the use of the Honeywell silicon on insulator fabrication process for use in a frequency synthesizer. The research includes the fabrication of a frequency synthesizer and ring oscillators which are used to evaluate the fabrication process. Experimental results are compared to the theoretical results, providing some insight into circuit design with the silicon on insulator process. Recommendations are presented to enhance the frequency stability of such circuits. A novel method for reducing phase noise in ring oscillators through manipulation of the floating body is also presented.

SOI for Frequency Synthesis in RF Integrated Circuits

by

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A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Department of Electrical and Computer Engineering

Raleigh
2003

Approved By

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Chair of Advisory Committee

Biography

Jeff Marks was born on May 25th 1976 in Port Huron, Michigan. He received his undergraduate degree in Computer Engineering from North Carolina State University in December of 1999. At various times during his academic career, Jeff financed his education by working as an Office Depot merchandise stocker, a bicycle mechanic, courier, computer help desk attendant, an employee of the Intel Corporation and Alcatel Network Systems, a circuits lab teaching assistant, a digital electronics teaching assistant and most recently a research assistant to Dr. Wentai Liu. Jeff will continue on with Dr. Liu to pursue his PhD at North Carolina State University.

Acknowledgements

Most importantly I would like to acknowledge the input and mentoring provided by Dr. Kasin Vichienchom, who patiently provided the guidance that made this work possible. Kasin's knowledge combined with his dedication, patience and humility have set in my mind, and incredibly high standard of what is expected of a scholar.

I also have to give my thanks to the other denizens of the fourth floor of EGRC. Kasin, Rajeev, Ramya, Rizwan and Mustafa have all been my technical advisors, social network, support group and most importantly my friends. These co-workers made spending the insanely long hours in room 429 fun. I don't think I could have asked for a better work environment.

I must also acknowledge Maria, for enduring a long distance relationship for two years when at times the light at the end of the tunnel seemed to be far, far away.

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Chapter 1 Introduction

1.1 Introduction and Motivation

The silicon on insulator (SOI) fabrication process is quickly becoming the answer to the technical challenges facing the integrated circuit (IC) industry. Consumer demands for more integration and high speed operation create a set of problems that SOI technology is uniquely qualified to solve. As the name implies "Silicon on Insulator" refers to the fact that the active MOSFETs are fabricated on an electrically insulating substrate. Some of the advantages (which will be examined in more detail later) include a reduction of substrate noise (allowing higher integration) and a reduction of parasitic capacitance (allowing high operating speed). Producers of high performance digital products (IBM and Intel) have invested in the development of SOI processes to be used in future products. SOI also stands to benefit the aerospace and military as well, for the benefits listed above and the availability of radiation hardening from some of the SOI fabrication facilities.

As of yet, SOI has yet to be embraced by the RF IC industry despite the benefits SOI holds in the form of tight integration of circuit blocks on a single chip, and high quality integrated passive components. Concerns over process maturity and the unique SOI device noise sources, have prohibited the rapid integration of SOI into the RF integrated circuit field. These potential benefits of SOI technology and the desire to spur more widespread acceptance and development of the SOI process motivated NASA to sponsor the research project that has funded this research. The goal of the project has been the development of a fully integrated RF receiver to be used in future missions to the surface of the planet Mars.

1.2 Scope

Specifically, this work explores the use of SOI for the frequency synthesis portion of the receiver. This includes a voltage controlled oscillator (VCO) and a means of synthesizing a high frequency signal through frequency multiplication of a low frequency input signal. The direction taken by me and the others working on this receiver, is to explore both a digital and analog architectures for the receiver. Each of these architectures has its own advantages and disadvantages (not to be discussed in this document) and each has distinct requirements for the frequency synthesizer. Figure 1.1 shows a block diagram of the architecture and the required frequency synthesis for each.

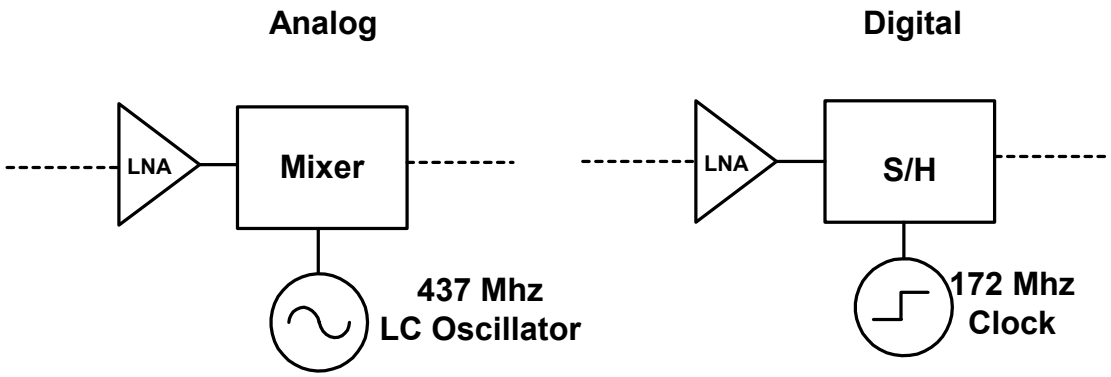


Figure 1.1 Frequency Synthesis Applications

Providing a low-noise low-power local oscillator or clock (depending on the architecture) is one goal of this research. In coordination with the straightforward construction of the frequency synthesizer, it has been the goal of this research to gain some insight into the benefits and disadvantages that SOI technology provides the RF circuit designer. Lastly, this work seeks to provide some characterization of the SOI devices and RF circuits in order to provide other SOI RF circuit designers with additional data about the Honeywell process so that they are able to make more informed design decisions.

At the time the designs fabricated for this work the Honeywell MOI5 process was still an experimental process. The device models and circuit libraries were updated on nearly a weekly basis. There was a distinct lack of support from the foundry with respect to the device models there were no published results of the testing of circuits that had been fabricated in the MOI5 process. This environment had a great influence on the circuits and designs that were chosen for the fist and second fabrications. Instead of pursuing complex designs that would be applicable for the end product, the approach taken in this work was to fabricate circuits that involved the least amount of risk. Most of the circuits are fairly simple in design, and have a minimal amount of supporting circuitry (biasing, buffering etc). The goal of this work was to try to learn as much as possible about Honeywell SOI to lay the groundwork for future circuit designs

1.3 Organization

This work is organized according to the research goals stated above. The literature review section encompasses a summary of recent developments in the area of frequency synthesis for RF receivers and recent developments in the areas that affect frequency synthesis in SOI technology. Chapter three reviews the work that has been done with respect to the development of the frequency synthesis system. Chapters four and five detail the work that has been done on the characterization of SOI technology and the circuit designs that have been implemented to utilize the benefits of SOI

Chapter 2
Literature Review

2.1 Developments In Frequency Synthesis

A search for literature specifically dealing with developments in the area of RF receiver design in SOI, will produce few results. The emergence of SOI into the areas of computing and digital circuit design is still in the beginning stages. While several articles have been published regarding SOI design techniques, or the design of circuit building blocks, there has been only one paper published regarding the development of an RF receiver in SOI [1].Instead of limiting the literature search to the developments in SOI, it makes more sense to review the state of the art in general frequency synthesis for RF applications.

Research in the area of frequency synthesis techniques has developed rapidly over the past ten years. Asynchronous communication, for both board-level and RF systems require a stable clock and/or local oscillator in order to recover the transmitted data. Traditional radios used a resonating crystal to produce such an oscillating signal, but the high-frequency, low-power and small-area requirements of today's applications require a different approach. Frequency synthesis techniques have been investigated for over 40 years [2]. A now popular topic of research in both industry and academia, the recent interest is generated by the capabilities of modern fabrication processes and the desire to integrate communication systems onto a single chip.

As the name implies, frequency synthesis is the creation of an oscillating signal. This process involves taking an input (the reference signal) and multiplying the frequency of this input to create an output signal that is of a higher frequency. Nearly all of the frequency synthesis systems rely on some variation of the fundamental architecture of the

phased locked loop shown in Figure 2.1 below. The system uses a feedback system to turn the low frequency input signal into a high frequency output signal.

2.2 PLL Basics

The input to the system (called the reference frequency) is generated off chip, usually by a resonating crystal that also provides the base frequency of the entire system. In modern consumer and outer-space applications this frequency is usually less than 1 MHz [3]. The output of the system is an oscillating signal produced by an oscillator controlled either by current (ICO) or by voltage (VCO). The output signal ϕ_{Out} is divided by a factor 'N' to become ϕ_{In} where it is compared to the reference $\phi_{\mathrm{Re}f}$.

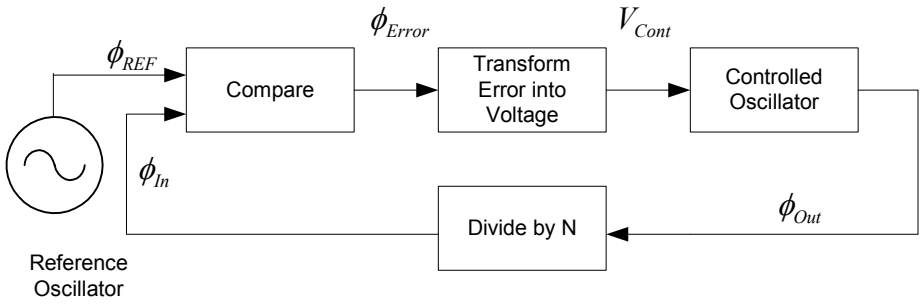


Figure 2.1 Fundamental Frequency Synthesizer Architecture

The comparator generates a signal that reflects the phase error between ϕ_{In} and $\phi_{\mathrm{Re}f}$. This phase error is then converted into a control voltage or current which is used to tune the VCO (or ICO). When f_{In} and $f_{\mathrm{Re}f}$ are equal, the output frequency can be expressed as $f_{Out} = N * f_{REF}$.

2.2.1 Integer N PLL

The easiest of implementation is the "Integer N" PLL where N the divide-by factor is an integer number that can be achieved with a system of flip-flops and digital logic. In order to select a desired f_{Out} the reference frequency must be selected in coordination with the values of N that are available. Many times this is not practical, as the reference oscillator

has other uses in the system and the frequency must be chosen to meet other specifications. Integer N PLLs are limited in their application to systems that require the recovery of data at multiple frequencies or channels. For the Integer N PLL to be effective the channel spacing must be an integer multiple of $f_{\mathrm{Re}f}$. This again places strict requirements on the reference oscillator that might not be practical for the system as a whole.

2.2.2 Fractional N Frequency Synthesis

A solution was proposed [4] to allow the use of a 'fractional' N to be used in the feedback loop. A fractional N allows greater flexibility in the selection of the output frequency and an ability to receive data on channels with closer frequency spacing. A method of achieving this is based on the "pulse swallower" concept [5]. Figure 2.2 below demonstrates the procedure. An input signal with frequency f_{IN} input to a pulse remover that removes one pulse over a period Td. The output contains a total of $Td\,f_{IN}-1$ pulses over a period of Td.

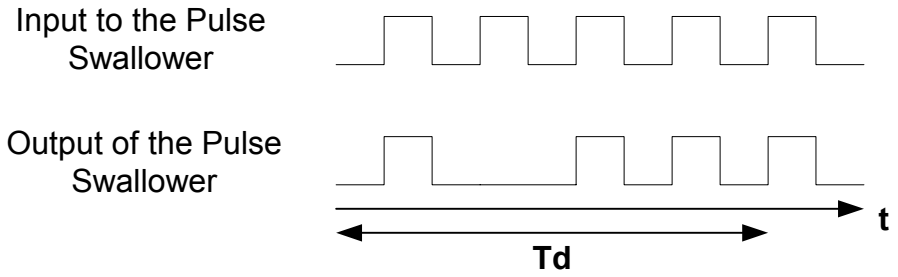


Figure 2.2 Demonstration of Pulse Removal

The resulting output has a frequency which can be represented as $f_{OUT} = f_{IN} - \frac{1}{Td}$. By altering the period Td, f_{OUT} can be adjusted to meet the needs of a multi-channel system.

Modern implementations rely on a slightly different method of producing the fractional N. The dual-modulus synthesizer (Figure 2.3) divides the output signal by one of two factors in order to produce a signal divided by an arbitrarily small fraction of N.

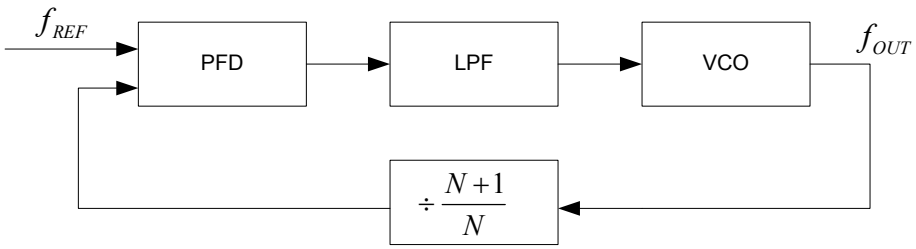


Figure 2.3 Architecture Of A Dual Modulus Synthesizer

If the prescaler divides by N for A output pulses (of the VCO) and by N + 1 for B output pulses, then the equivalent divide ratio is equal to (A+B)/[A/N + B/(N+1)]. This value can vary between N and N + 1 in fine steps by proper choice of A and B. The resulting modulus is sometimes written as N.f, where *N* and *f* represent the integer and fractional parts of the modulus. An example of this process can be seen in Figure 2.4 below. If $f_{\mathrm{Re}\,f} = 1MHz$ and N = 5. Let us assume the presale divides by 5 for 4 reference cycles and divides by 6 for one reference cycle.. The total number of output pulses is therefore equal to 5 x 4 + 6 = 26, whereas the reference produces 5 pulses. In other words, the divide ratio is equal to 5.2 making $f_{\mathrm{Re}\,f} = 5.2MHz$.

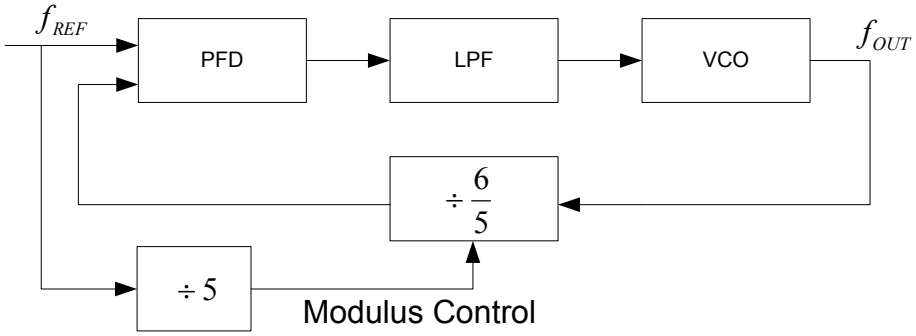


Figure 2.4 Dual Modulus Architecture

Figure 2.5 below displays the waveforms associated with the N.f fractional synthesis. Important to note is the effect on the phase detector throughout the process. The phase error builds with each cycle until it is essentially reset to zero at the end of the period.

Unfortunately this characteristic has an undesired effect of adding noise to the output spectrum.

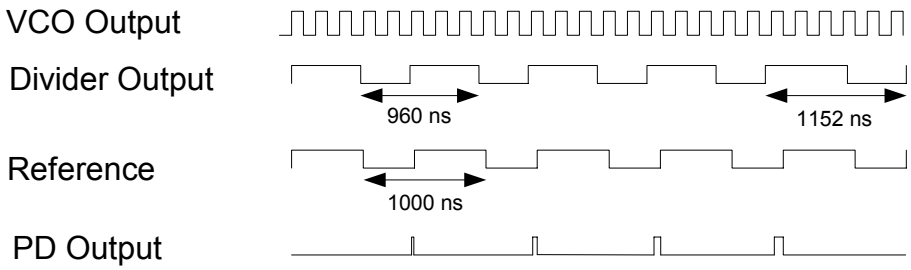


Figure 2.5 Fractional N Frequency Synthesis Operation

Filtering the Fractional Spurs

Fractional spurs are caused by the periodic accumulation of phase error in the system. It is easiest to visualize this concept when the VCO was biased at a constant voltage and disconnected from the LPF. The output frequency for this analysis is $f_{OUT} = 5.2MHz$. In Figure 2.5 each of the first 6 cycles of the divided signal is slightly shorter than the reference period. This causes the phase difference between the reference and the feedback signal grows in every period of $f_{\mathrm{Re}f}$, until it returns to zero when divide-by-11 occurs. This has the effect of creating a ramp waveform at the output of the LPF.

This waveform at the LPF would be repetitive with a period of $1/(\alpha f_{REF})$, given a VCO output frequency of $(N+\alpha)f_{REF}$. In a closed loop, the waveform would modulate the VCO creating sidebands at integer multiples of αf_{REF} offset from the center frequency.. These sidebands are called fractional spurs. These fractional spurs can be severe, but several methods for suppressing these spurs have been suggested [5,6].

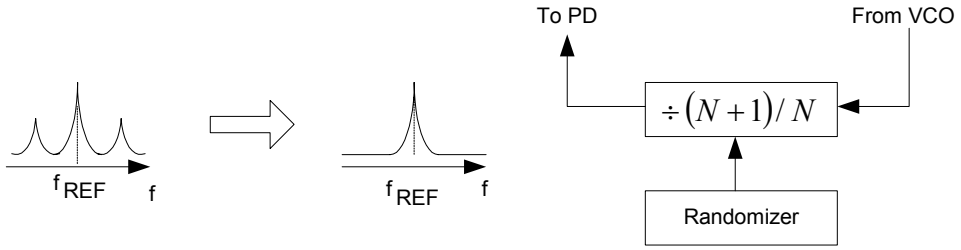


Figure 2.6 Showing the need to reduce spurs

Randomization of the modulus in a way that produces an average division factor $(N+\alpha)$ is one approach to solving this problem. This technique in effect converts the systematic factional sidebands to random noise. The idea can be taken one step further by shaping the resulting noise spectrum such that most of its energy appears at large frequency offsets. Thus the noise in the vicinity of the divided carrier is sufficiently small and the noise at higher offset is suppressed by the low-pass filter after the feedback signal is translated to DC by the phase detector.

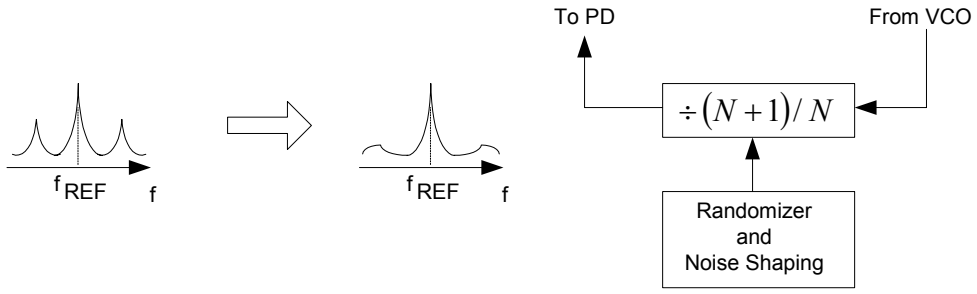


Figure 2.7 Noise Shaping

The noise shaping function required in the above scheme can be realized by use of a $\Sigma-\Delta$ modulator. Depicted in Figure 2.7 the modulator generates a binary stream (in the case of dual modulus divider) representing an average value accompanied by quantization noise. [7]. The $\Sigma-\Delta$ modulator generates a well-defined shape for Q(f), concentrating the noise at high frequencies. Figure 2.8 shows the implementation of this architecture in the frequency synthesizer.

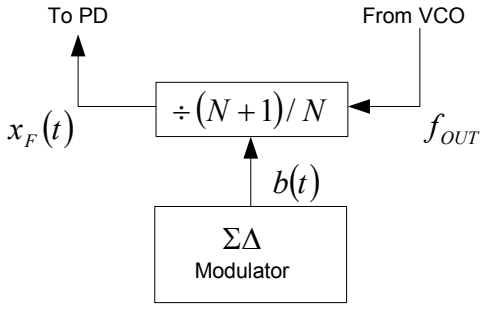


Figure 2.8 SD modulator architecture

The sigma delta modulator can be a very complex circuit and is many times implemented in an FPGA or in a MATLAB program which interfaces with the synthesizer through some control lines.

2.3 Current Developments In Frequency Synthesis for RF Applications

Nearly all of the recent frequency synthesizers developed for wireless applications rely on one of the techniques described in the section above. Over the past two years 14 articles have appeared in the Journal of Solid State Circuits that focus on the application of a frequency synthesis system to an RF front end design. Figure 2.9 below shows a tally of the frequency synthesis methods used in these applications. These papers usually demonstrate the ability of a frequency synthesizer to be implemented with some new encoding scheme (GFSK, GMSK) or some RF communication standard (DCS, CDMA) [31-35]. Other papers explore the abilities of advanced processes in creating improved circuits.

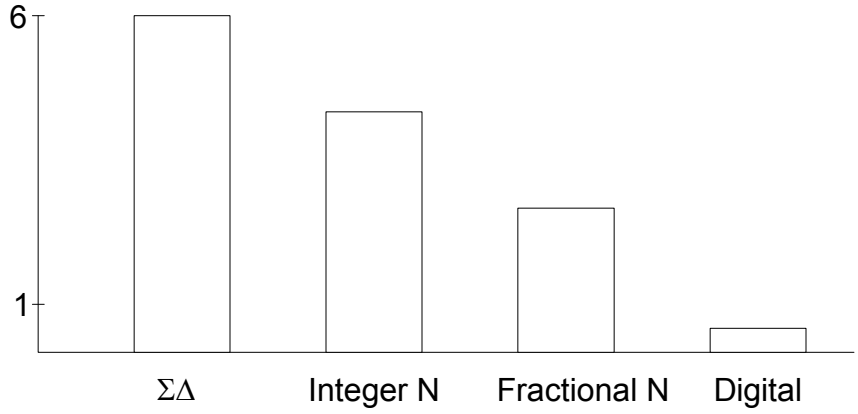


Figure 2.9 Tally of JSSC Results

2.3.1 Developments in VCOs

Of all the components of the frequency synthesizer, the VCO has undergone the most development in recent years. In the last two years alone twenty two articles have appeared in the Journal of Solid State Circuits focusing on the analysis and design of

voltage controlled oscillators. Research in this area can be more intuitively identified as either *analog* or *digital*.

Digital

Digital oscillators are usually based in some form inverter chain as seen in Figure 2.10.

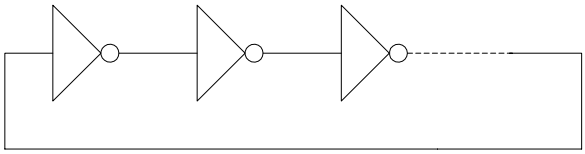


Figure 2.10 Ring Inverter

A simple example of the construction of such an oscillator employs the single stage inverter delay cell as seen in Figure 2.11.a. In order to oscillate, a total phase shift of 360 degrees around the loop at a frequency where the small-signal loop gain is above 0db. In an N-stage ring, each stage contributes a (negative) phase shift of 180/N for a total of 180 degrees.

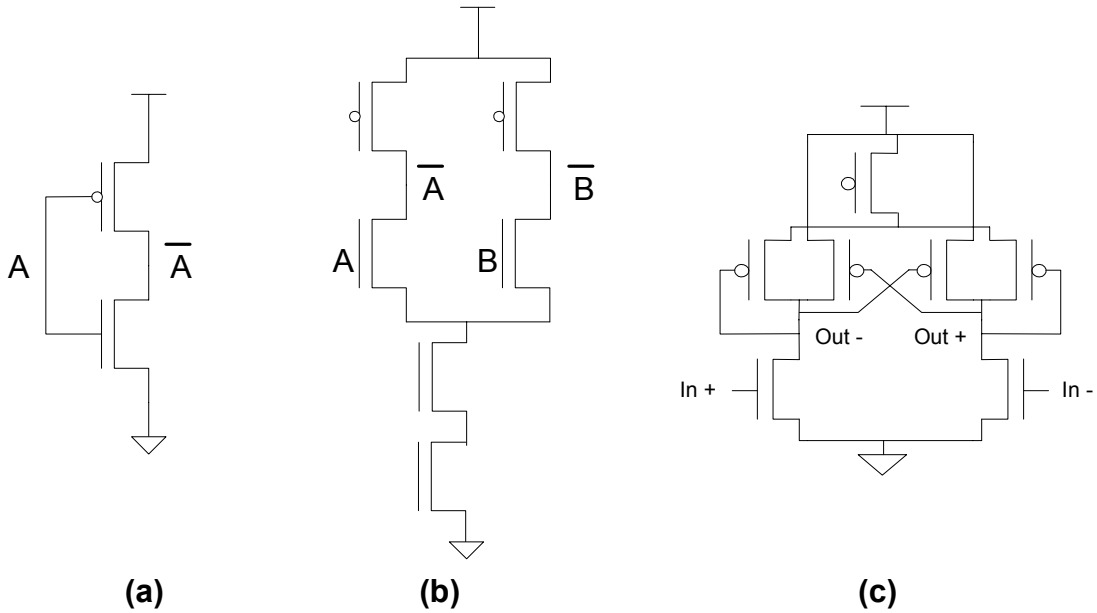


Figure 2.11 Examples of Delay Stages

An additional 180 degrees is provided by the DC phase inversion. The DC phase inversion is automatically achieved by using an odd number of inverting stages called or

by swapping two feedback lines in a differential architecture an using an even number of inverting stages. Figure 2.11.b shows the differential version of the ring oscillator introduced explained in previous literature [8,9]. The differential or *ECL design* shown in Figure 2.11.b offers lower susceptibility to supply noise and easy access to outputs with quadrature phase (for RF communication). The largest disadvantage of this approach is that output amplitude is not full-swing and is dependent on the operating frequency (or bias levels). As the P and N devices are biased to starve the inverter of current, the amplitude of the output waveform will decrease. In digital implementations, additional circuitry is needed to bring the outputs to full-swing, increasing the complexity and power consumption of the circuit. Additionally, as power supply voltages are reduced, the stack-up of the devices poses a problem in the ability to bias the devices into the correct operating region. Figure 2.11.c shows the next step in the evolution of the inversion stage design [10][11]. By cross coupling the PMOS load devices, much like in a differential amplifier, the output voltage swing of the circuit is increased. This design scales easier with process advancement and avoids the complex buffer designs required for the "ECL-like" designs. Nearly all modern frequency synthesis applications use some form of the differential delay stage in the VCO. The superior rejection of noise, and the accessibility to the quadrature outputs makes it more suited to the most common applications [12] [13]. The choice of full-swing or partial-swing must be made with the end application in mind. Partial swing designs are easier to test in high-frequency designs, as a full-swing circuit requires a larger buffer to drive the probe/bonding pad. No one design is superior to the other, and the application and test environment should help to determine the best approach.

Analog

The analog approach to oscillator design differs from digital design only in the design methodology. The operating frequency of the digital oscillator is inversely proportional to the number of stages. Oscillation with the 'delay-stage' approach is difficult to obtain with fewer than 3 stages due to the relatively small delay of the individual stage. In order to produce the higher frequency oscillating signals necessary for current high frequency

applications (1.8 GHz and above) it is necessary to take an analog approach to the design of the oscillator.

Traditional analog approaches rely on the concept of a 'negative resistance' in order to meet Barkhausen's criteria that the loop gain of a feedback system is unity and that the total phase shift around the loop must be equal to zero (or 180 if the dc feedback is negative). The traditional system used to produce these criteria relies on the properties of an LC tank. Figure 2.12 below shows how producing a 'negative' resistance to cancel the parasitic resistance that co-exists with any passive component. By creating a resistance that is equal and opposite to the parasitic resistance a nearly ideal LC tank circuit can be created that oscillates at $\omega = \left(\sqrt{LC}\right)^{-1}$.

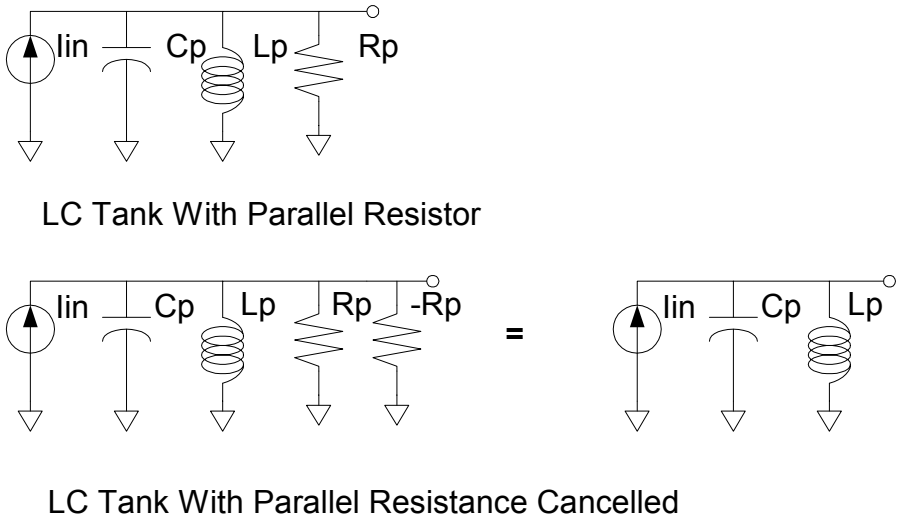


Figure 2.12 Negative Resistance Concept

Figure 2.13 below shows two implementations of this negative resistance concept. Figure 2.13.a is a single ended configuration while Figure 2.13.b is a cross-coupled dual output configuration. In each case, the transistors are sized so that the resistance seen by the LC tank and the associated parasitic resistance (Rp) is -1/gm. This circuit can be viewed as either a feedback system or a negative resistance in parallel with a lossy tank as long as the condition: $Rp \geq \frac{1}{gm}$ is upheld.

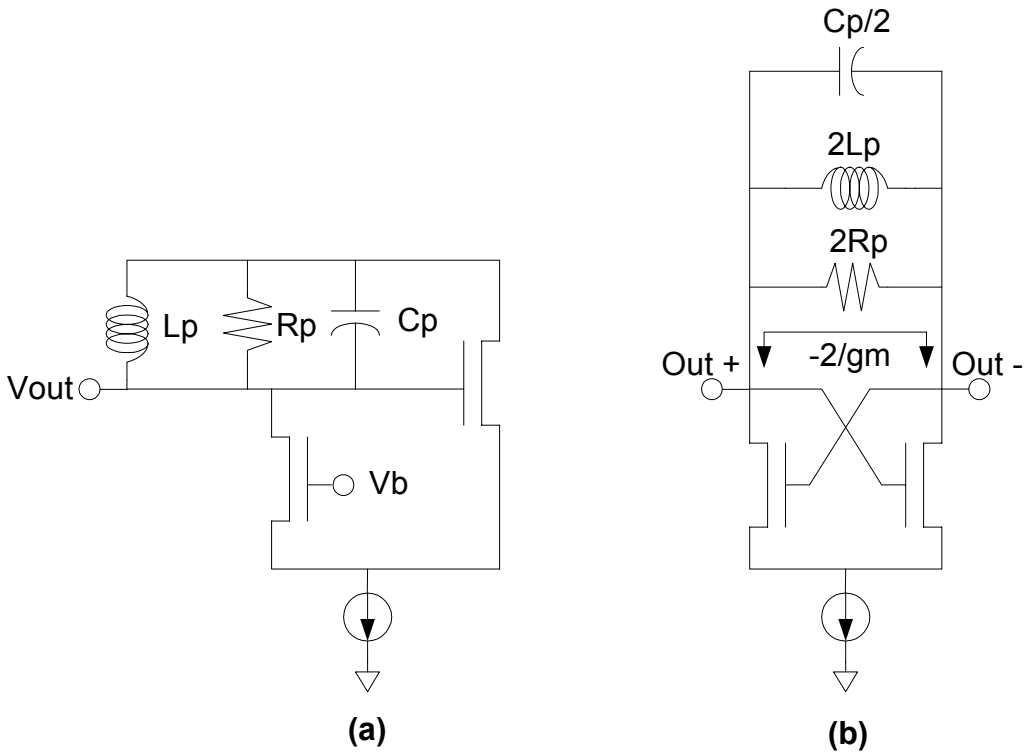


Figure 2.13 Negative gm Oscillators

This approach by far is the most common and straight-forward of the different methods of creating an oscillator. Recent research into VCO design has focused on integrating this fundamental design into new technologies and altering the architecture slightly to meet specific application criteria [14-15]. Other recent works have focused on understanding the effects of the individual circuit components on the phase noise of the oscillator and methods of eliminating this noise [16-17]. Such research is important in the development of VCO's for system implementation, however such considerations were not necessary for this initial work.

Besides the classic LC tank implementation of an analog oscillator, a different implementation has been developed that does not rely on inductors [18,19]. This method uses a differential-amplifier based inverter to produce the necessary phase shift at the output of each stage.

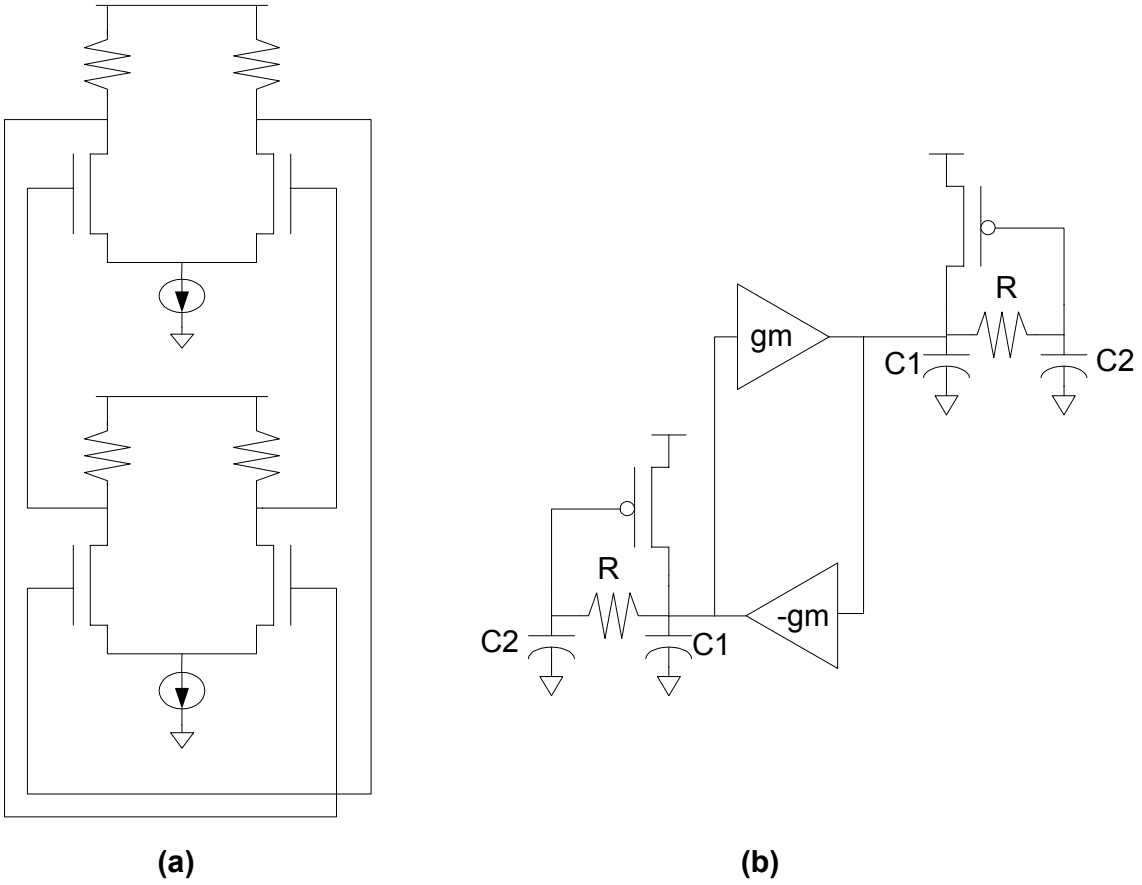


Figure 2.14 Negative gm Oscillator Using Differential Amplifiers

Figure 2.14 above shows the implementation of the cross coupled differential amplifier used as an oscillator. Figure 2.14.a shows a simplified version of the oscillator, while Figure 2.14.b shows the a more accurate representation of the actual circuit. The active load seen at the output of each of the amplifier stages in Figure 2.14.b is inductive and inserts a pole into the transfer function. This pole is necessary to create a unity gain at finite frequencies that allow the circuit to oscillate.

Among the various implementations of the analog oscillator, each has its own benefits and disadvantages. Each implementation has fairly similar noise performance and power consumption. Recent developments in process technology [20-21] have raised the quality factor of integrated inductors, thereby reducing the power consumption of LC type oscillator circuits making them the more popular choice for the RF circuit designer.

Advanced processes allowing the integration of such elements is not always available however, in which case an active inductor implementation is a valid solution.

Chapter 3
Development of an integrated frequency synthesizer in SOI.

As stated in the introduction, the end goal of the NASA SOI project is a fully integrated radio receiver, which includes the frequency synthesizer. The frequency synthesizer is by necessity one of the most area-hungry blocks of a receiver design. The integrated passive components, the VCO and the divide-by-N circuitry consume a large amount of die space. In the first SOI fabrication, the available die space was divided among three students, and as a result there was room for only one attempt at a frequency synthesizer.

The frequency synthesizer chosen for the first SOI fabrication was an integer N PLL that is to supplement the all-digital receiver architecture. A block diagram of the PLL is shown in Figure 3.1 below.

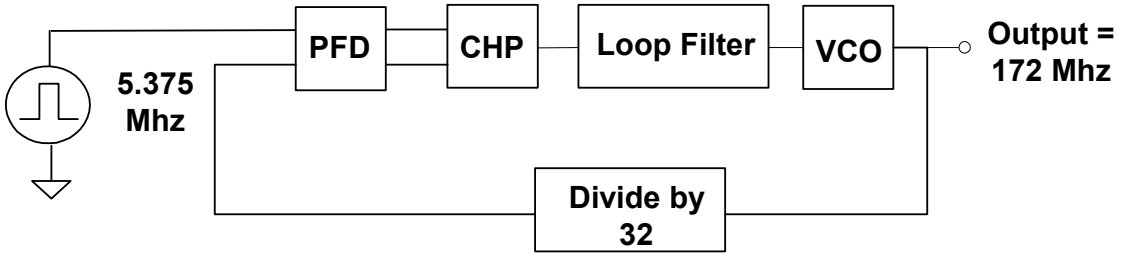


Figure 3.1 Block Diagram of the PLL

3.1 Building Blocks of the PLL

The PLL is a classical integer-N PLL that was described in the literature review. The output was chosen as 172 MHz to meet the requirements of outlined by the NCSU digital receiver specification. The input frequency of 5 MHz was chosen based on two criteria. 1) In the final design a frequency of < 10Mhz will be required per the specifications of

the Jet Propulsion Laboratory [22]. 2) A 5 MHz signal is easy to obtain with the available signal generators. An integer-N architecture was chosen simply because of its relative simplicity compared to any of the fractional N architectures. The integer N design presented the least risk.

Each of the individual blocks of the PLL are best represented in the frequency domain so that the behavior of the system as a whole can be designed intelligently and simulated. The system as a whole can be represented as a feed-back system. Figure 3.2 below shows the block diagram.

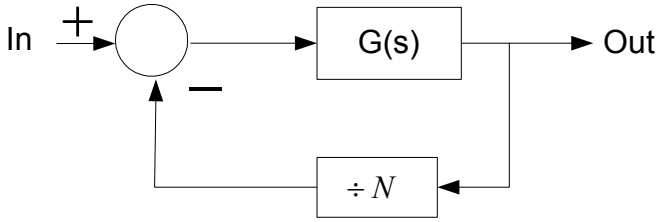


Figure 3.2 System Representation of PLL

The simple transfer function is

$$H(s) = \frac{Out}{In} = \frac{G(s)}{1 + \frac{G(s)}{N}}$$

Each of the individual blocks of the design must be represented in the final equation.

3.1.1 Component: Phase Frequency Detector and Charge Pump

The phase detector and charge pump can be grouped together for easier analysis. Figure 3.3 below shows the block diagram.

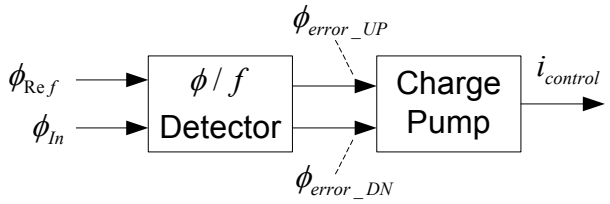


Figure 3.3 Block Diagram of the Charge Pump and Phase Detector

Two signals enter the phase/frequency detector one generated by the off-chip reference crystal ϕ_{Ref} and one generated by the divide-by-N block ϕ_{In}. The phase detector detects the phase difference between the two signals and generates two output signals ϕ_{error_UP} and ϕ_{error_DN}. These signals indicate whether the phase of the clock should be advanced or delayed in order to be synchronized with the reference signal [23]. The relationship in general can be expressed as:

$$\Phi_{error} = \Phi_{Ref} - \Phi_{In}.$$

This error or 'phase difference' signal is then input to the charge pump circuit.

The charge pump circuit can be visualized as two current switches (Figure 3.4) controlled by the phase-error input signals.

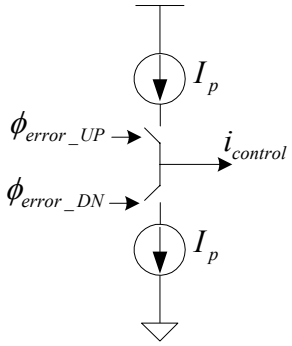


Figure 3.4 Charge Pump

When either the 'up' or 'down' input is asserted the corresponding current source, with current equal to I_p is connected to output $i_{control}$. The transfer function for the combination of the phase/frequency detector and charge pump can be understood as the amount of current that is generated by the phase error between the two input signals

$\phi_{\mathrm{Re}\,f}$ and ϕ_{In} a quantity that was expressed above as ϕ_{error}. A relationship can be established between the phase error and the output current per cycle

$$i_d = \frac{(I_p)(\phi_{error})\tau}{2\pi}$$

or the current per period

$$i_d = \frac{(I_p)(\phi_{error})}{2\pi}.$$

i_d is the average current per period, it would also be the average current over many periods, or over time t. The relation between output current and phase error then becomes

$$\frac{i_d(s)}{\phi_{error}(s)} = \frac{(I_p)}{2\pi} = Kd$$

Where Kd is known as the gain of the phase detector, and can be graphically interpreted as the slope of the relation between the average current i_d and the phase difference $\Delta\phi$ (Figure 3.5).

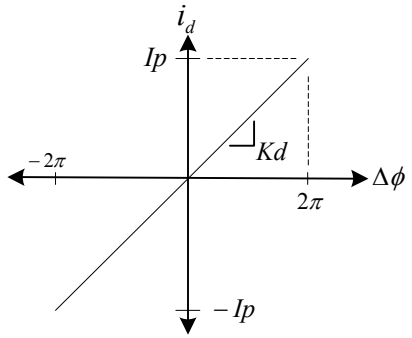


Figure 3.5 Phase Detector Gain

One disadvantage of the charge-pump PLL is that even when loop is 'locked' or synchronized with the input, there will be some switching in phase detector that will cause a small injection of charge into the loop-filter. This injection of charge results in a "ripple" of the control voltage at the output of the loop filter. There are ways, however that the loop filter can be used to minimize this problem.

3.1.1.1 Implementation of the CP and PD

Figure 3.6 and Figure 3.7 show the circuit representation of the phase detector and charge pump respectively.

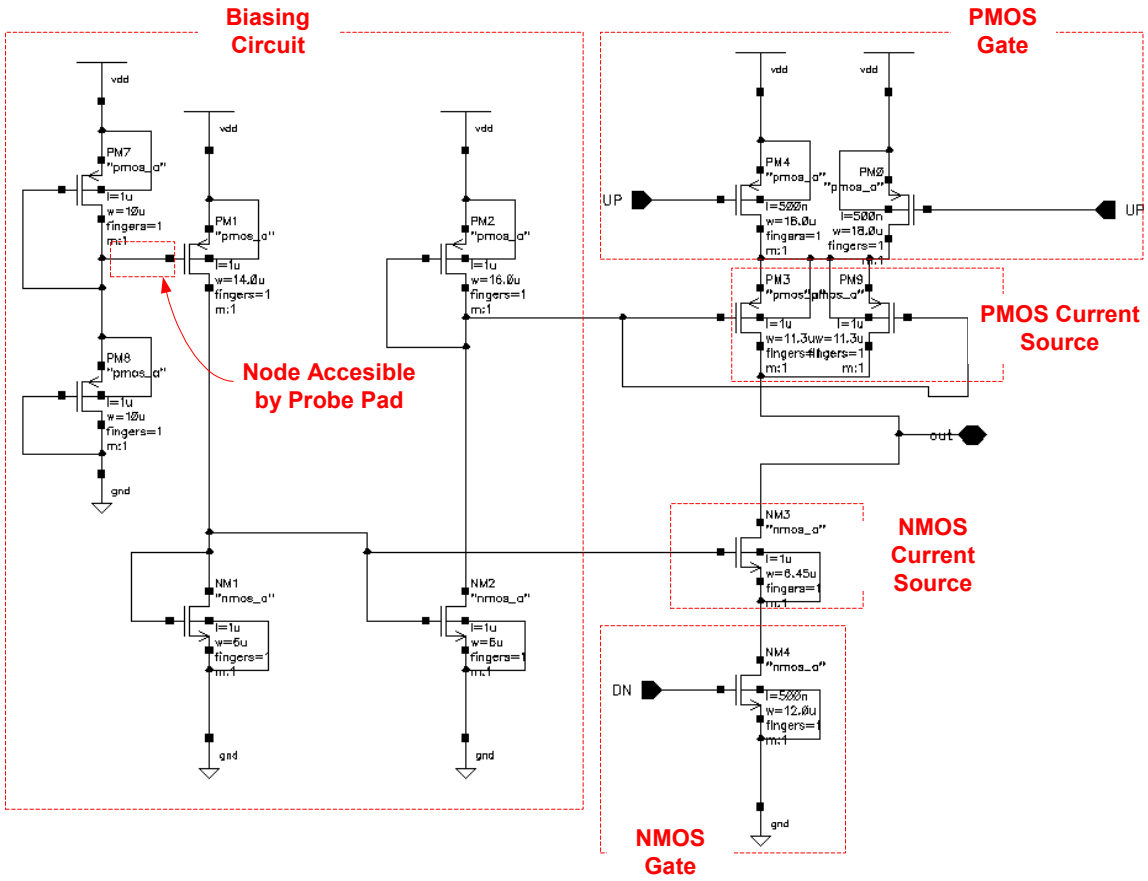


Figure 3.6 Charge Pump Circuit

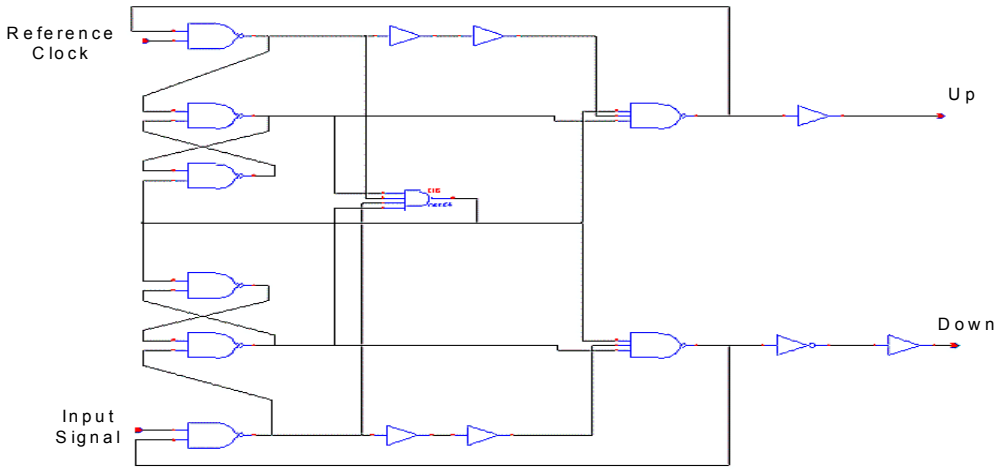


Figure 3.7 Phase Frequency Detector

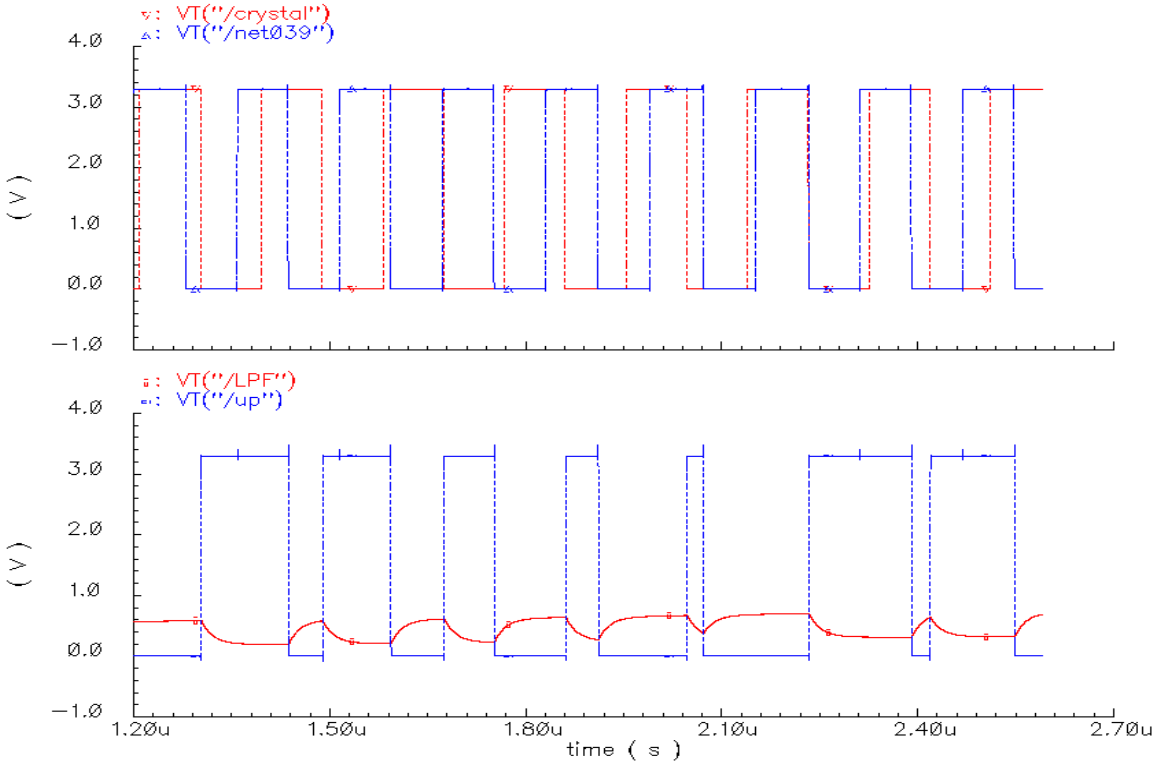


Figure 3.8 Operation of PFD and Charge Pump

Figure 3.8 shows the operation of the charge pump. The top wave form shows the two signals: the reference clock and the divided output of the VCO. In the bottom wave form the operation of the charge pump is seen. When the pulse is 'low' the charge pump is activated and the voltage on the loop filter rises.

3.1.2 Component: Loop filter

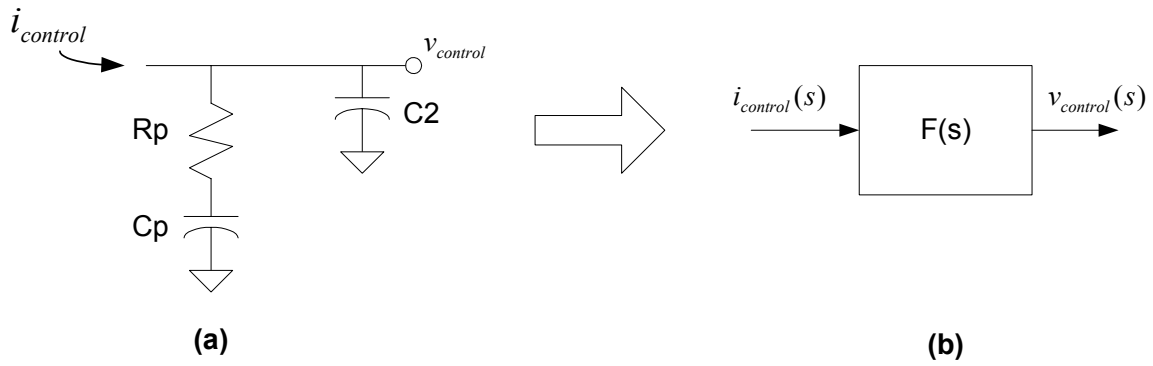


Figure 3.9 Loop Filter Circuit and Block Diagram

The loop filter is represented by the function F(s) in the PLL system equations. The parameters of the loop-filter R, Cp and C2 are easily manipulated by the circuit designer making the loop-filter the instrument by which the PLL is 'tuned' for specific performance standards. The loop filter may be either active or passive [23], but the architectures compatible with charge-pump phase detector PLL's have a similar structure that is driven by their use in transforming the charge pump current into a control voltage for the VCO. A necessary component of such an architecture is a shunt-capacitor as seen in Figure 3.10.a

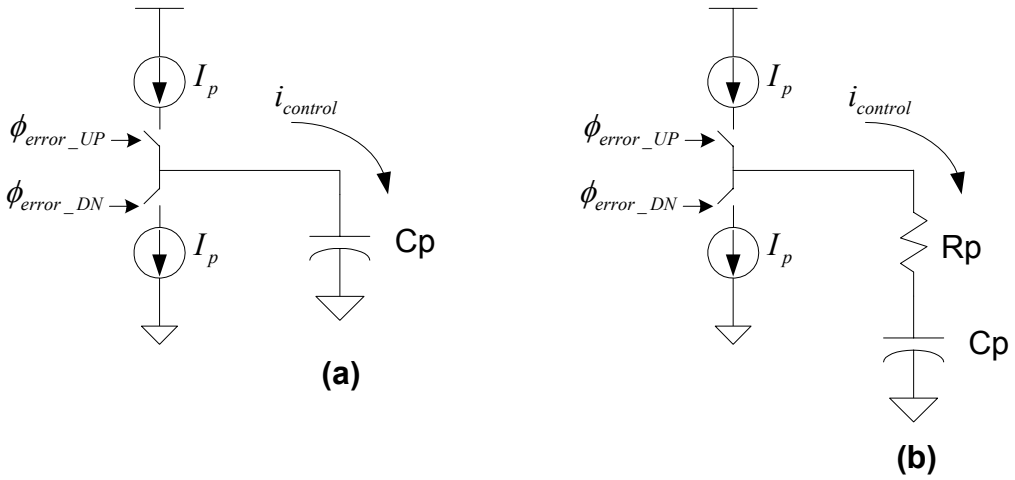


Figure 3.10 Operation of Charge Pump and Loop Filter

The shunt-capacitor 'Cp' provides the charge storage that allows the current $i_{control}$ to become a voltage which controls the VCO.

3.1.3 Component: VCO

The voltage controlled oscillator (VCO) provides an oscillating signal ω_{out}, the frequency of which is governed by the control voltage $v_{control}$. Figure 3.11 shows the block diagram representation of the VCO.

Figure 3.11 Block Diagram of the VCO

An ideal VCO generates a periodic output whose frequency is a linear function of a control voltage $v_{control}$

$$\omega_{out} = \omega_{FR} + KvcoV_{control}$$

Where ω_{FR} is the free-running frequency and Kvco is the "gain" of the VCO (specified in rad/s per volt). Since phase is the time integral of frequency, the output of a sinusoidal VCO can be expressed as

$$y(t) = A\cos(\omega_{FR}\, t + Kvco\int_{-\infty}^{t} v_{control}\, dt)$$

The 'excess' phase can be represented as:

$$\phi_{out}(t) = Kvco\int v_{control}\, dt$$

Which yields the transfer function

$$\frac{\Phi_{out}(s)}{V_{control}(s)} = \frac{Kvco}{s}$$

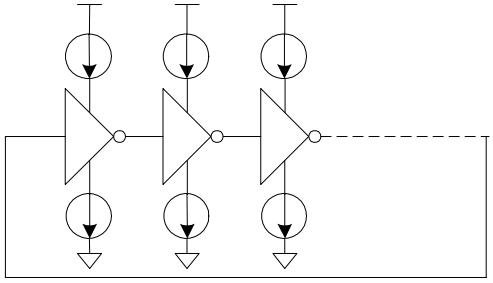


Figure 3.12 Current Starved Voltage Controlled Oscillator

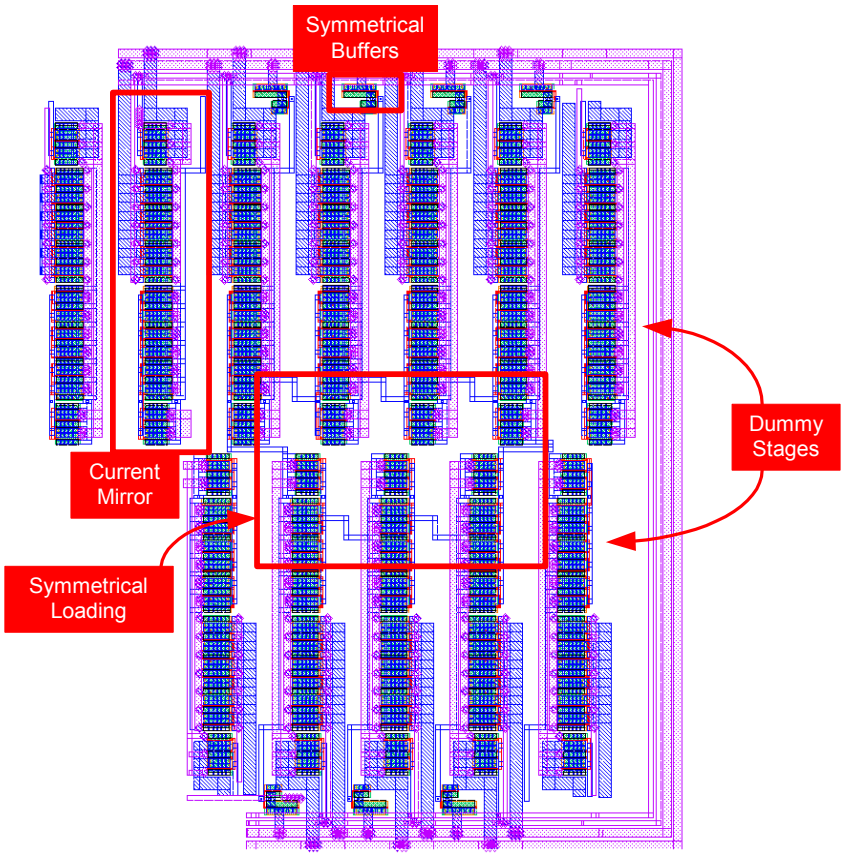


Figure 3.13 Layout of the VCO

The layout of the VCO is employs the basic practices that are standard to reliable analog circuit design. On each side, dummy stages are laid out but not connected. These dummy stages prevent any 'edge effects' from changing the characteristics of one of the stages therefore causing an imbalance.

Another step taken was to make sure that each stage was equally loaded with loading capacitance. To achieve this, equal interconnect between each stage is required, along with the use of 'dummy' buffers, which are not actually connected to any output.

3.1.4 Component: Divide By N

The functionality of the divide by N circuit is fairly straight forward. Each stage of the divide by N requires two rising clock edges in order to produce on single rising edge. Each stage had the effect of dividing the frequency in half.

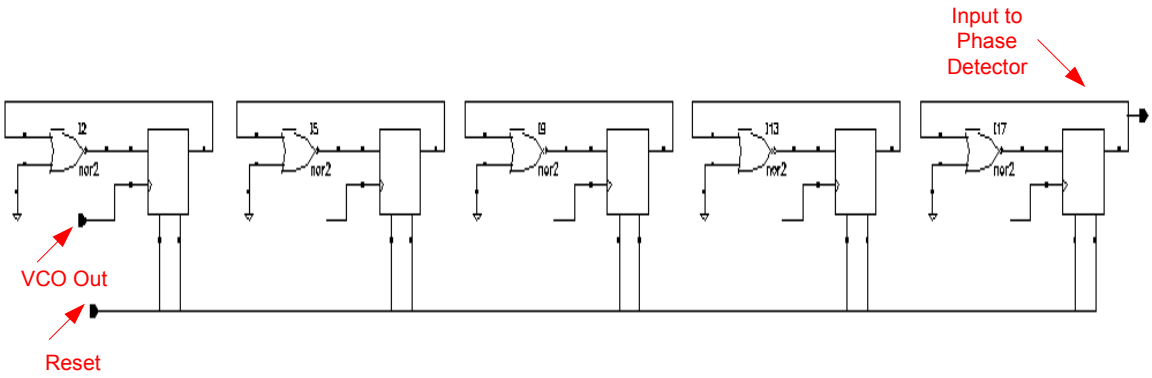


Figure 3.14 Divide By N Circuit

3.2 System Analysis

The contribution of the phase-detector, loop filter, VCO and divide by N circuit is represented as:

$$Kd\,F(s)\,Kvco\,\frac{1}{N}$$

Substituting from the previous equations

$$\frac{Ip}{2\pi}\cdot\frac{1}{C_p s}\cdot\frac{Kvco}{s}\cdot\frac{1}{N}$$

The system equation is now:

$$H(s)=\frac{\frac{IpKvco}{2\pi Cp}}{s^2+\frac{IpKvco}{2\pi Cp}}$$

This means, however, that the closed-loop system contains two imaginary poles at

$$s_{1,2}=\pm\sqrt{\frac{IpKvco}{2\pi Cp}}$$

Which means that the system will be unstable. The instability is caused by the fact that there are two poles at the origin. These two integrators, each providing a $90°$ phase shift, meaning that the phase shift of the system is $180°$ at the gain crossover providing for self oscillation at that point. Figure 3.15.a shows the phase response of this system.

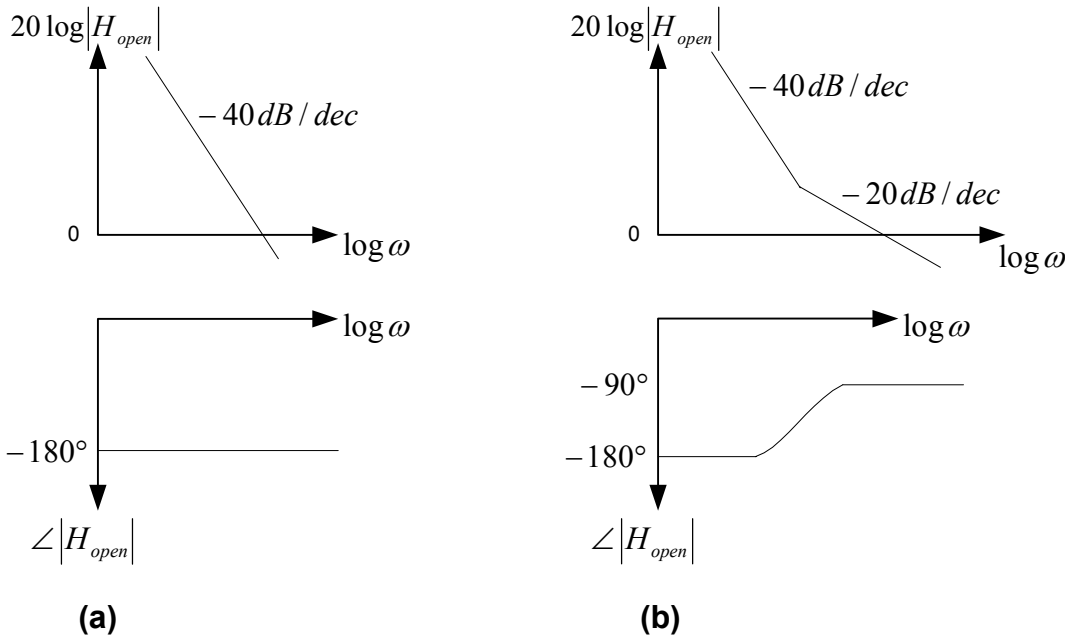


Figure 3.15 Phase and Magnitude Response of the PLL

In order to solve this stability problem, it is necessary to introduce a pole into the system. This can be accomplished by adding a resistor in series with the capacitor (Figure 3.15.b). The system equation now becomes

$$H(s) = \frac{\frac{IpKvco}{2\pi Cp}(RpCps + 1)}{s^2 + \frac{Ip}{2\pi}KvcoRps + \frac{Ip}{2\pi Cp}Kvco}$$

Which is the open loop system equation. The natural frequency ω_n and damping factor ζ can also be found:

$$\omega_n = \sqrt{\frac{IpKvco}{2\pi Cp}}$$

$$\zeta = \frac{Rp}{2}\sqrt{\frac{IpCpKvco}{2\pi}}$$

The improved stability is shown in Figure 3.15.b where a second capacitance 'C2' is shown as a part of the loop filter. This capacitance is used as a way of reducing the ripple at the output of the charge-pump, but is also introduces a third pole ω_p into the system given below.

$$\omega_p = \frac{1}{Rp\dfrac{CpC2}{Cp + C2}}$$

The effect of this additional pole can be seen in the gain and phase plots in Figure 3.16.

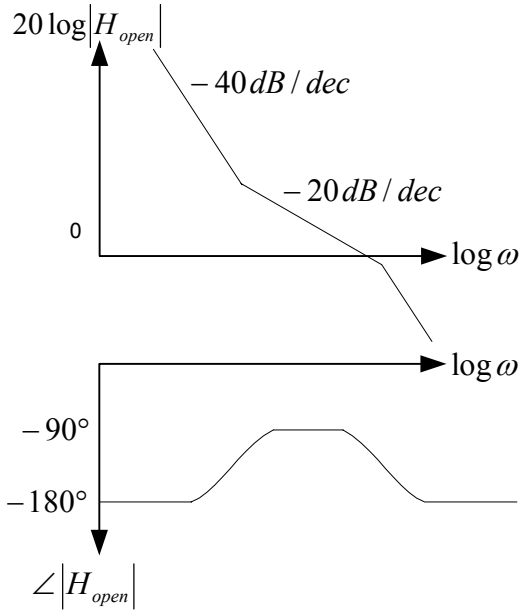


Figure 3.16 Effect of Ripple Capacitor on Phase and Gain

3.3 System Design

The design of the PLL relies on an understanding of the contributions of the individual functional blocks to the system functionality as a whole. The phase detector gain Kd the gain of the voltage controlled oscillator $Kvco$ the transfer function of the loop filter $F(s)$ and the feedback $1/N$ can be combined to form a system transfer function.

$$H(s) = \frac{\dfrac{IpKvco}{2\pi CpN}(RpCps + 1)}{s^2 + \dfrac{Ip}{2\pi}\dfrac{Kvco}{N}Rps + \dfrac{Ip}{2\pi Cp}\dfrac{Kvco}{N}}$$

This system equation can be analyzed to predict the behavior of the system. By nature of the VCO and charge pump phase detector, two poles are located at 0 and a third is created by the loop filter.

$$\omega_{p1}, \omega_{p2} = 0, \qquad \omega_{p3} = \frac{1}{Rp\dfrac{CpC2}{Cp + C2}}$$

One zero is also generated by the loop filter.

$$\omega_z = \frac{1}{RpCp}$$

The natural frequency ω_n and damping factor ζ are also important to the system performance and are given below.

$$\omega_n = \sqrt{\frac{IpKvco}{2\pi Cp\,N}}$$

$$\zeta = \frac{Rp}{2}\sqrt{\frac{IpCpKvco}{2\pi\,N}}$$

And the loop bandwidth *Kloop* can be represented as

$$Kloop = 2\,\zeta\,\omega_n = \frac{RpKdKvco}{N}$$

3.3.1 Determining Design Variables

A circuit designer has control over the following variables in the design process.

$$Rp, Cp, C2, N, Kvco, Kd$$

In practice though, several of these variables are fixed by necessity by the circuit technology or the requirements of the system. This was the case for this work as well.

Table 3.1 Fixed Design Variables for the PLL

$N = 32$	The specification of this PLL called for an output frequency of 172 MHz from a 5.73 MHz clock, this implies that N is fixed at 32
$Kvco = 119.9\,MHz/v$	The low-risk approach of this PLL utilized a ring oscillator composed of single ended inverters. In this case the oscillator is designed to have an output frequency range that is centered at the desired output frequency which is in this case 172 MHz. After designing a VCO to such a specification, the gain *Kvco* is fixed, in this case at 111.9 MHz/v.
$C2 \cong 10\,pF$	Since the loop-filter will be implemented off-chip, there is likely to be significant parasitic capacitance in the i/o pad, the bond-pad and the package lead. Such parasitic capacitance was calculated to be approximately 10pF. Such large parasitic capacitance will most likely make the ripple capacitor unnecessary.

With these values set, it is easier to solve for the remaining variables, a process which employs the use of rules-of-thumb and common-sense to establish the relationship between the system parameters.

3.3.2 Solving the System Equations

It is recommended that the natural frequency be 10 times the input frequency.

$$\omega_n = 10\,\omega_{in}$$

This relation allows us to solve for the value of Cp. Also setting the damping factor ζ can be assumed to be .8 to preserve stability of the system.

$$\zeta = .8$$

This assumption allows the use of the previous equations to find the value of Rp. The value of Kd is fairly flexible, and can be used by the system designer to adjust the loop bandwidth in order to meet the stability criteria. Somewhat arbitrarily, a value should be chosen that is reasonable for the process, meaning that the current does not exceed the

device capabilities, and is reasonable for the power consumption requirements. In this work, the value of $200\mu A$ was chosen as a "first try".

After all the variables have been found, it is necessary to evaluate the system for its stability and performance. It is most efficient to use MATLAB or some other mathematics software package to solve the equations. In this work, MATLAB was used to solve for the system stability and performance using the "control-systems' toolbox. It is not difficult to write a MATLAB program that evaluates the gain-response and phase-response of the feedback system. Through this tool, performance metrics such as phase-margin, and system 'peaking' can easily be measured. The simulation of a PLL at the circuit level is resource intensive, requiring several hours of simulation time to simulate only a few micro-seconds of actual run time. It is therefore necessary to be fairly certain of the system performance before beginning circuit simulations. MATLAB is best used to iteratively change the parameters of the design and view the results. During this iterative process it is necessary to keep in mind several rules of thumb that provide for better system performance and stability.

Table 3.2 Performance Requirements for the System

$\zeta > .7$	$\omega_n > 10\,\omega_{in}$
$Kloop > 4\omega_z$	$\omega_p > 4Kloop$
$PhaseM\arg in > 65°$	

Figure 3.17 is a flow-chart depicting the design flow.

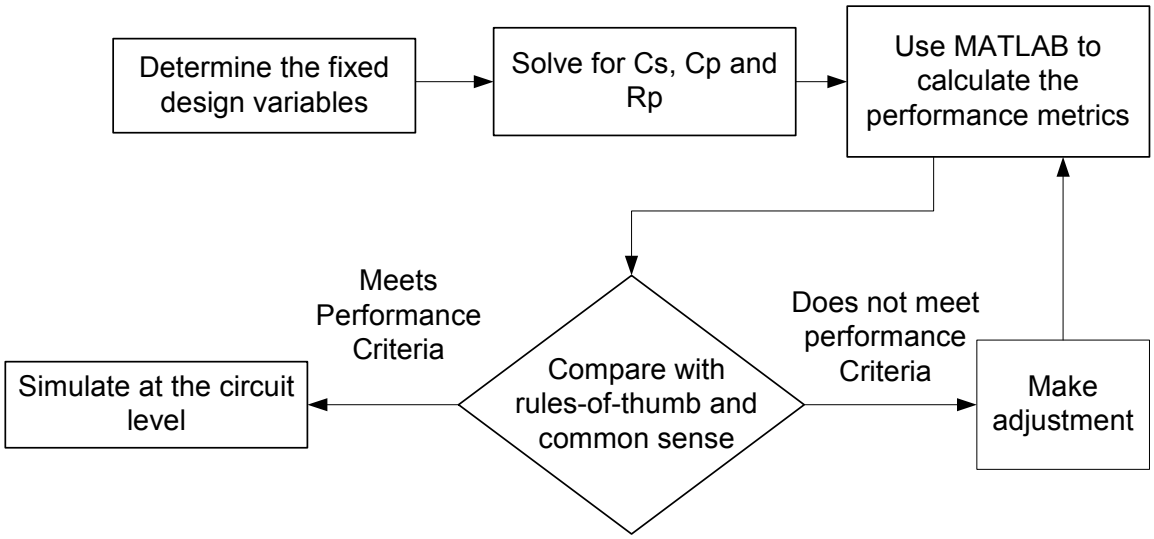


Figure 3.17 Process Design Flow

3.3.3 Design Results

MATLAB was used to calculate the gain, phase-margin and stability of the system. After several iterations, the following values were chosen as the most satisfactory for meeting the system requirements.

Table 3.3 Final Values Chosen for Circuit Implementation

$Rp = 1200\,\Omega$	$Cp = 3nF$
$C2 = 10pF$	$Ip = 250uA$
$N = 32$	$Kvco = 119.9MHz/v$
$Kd = 39\mu$	

Some of the important system characteristics are shown in **Error! Reference source not found.**. All the criteria listed in **Error! Reference source not found.** have been met.

Table 3.4 Performance of Simulated PLL

$Kloop = 1.049Mrad/s$	$\omega_p = 83.3Mrad/s$
$\omega_z = 277.8krad/s$	$\omega_n = 539.8krad/s$
$\zeta = .9717$	$PhaseM\,\mathrm{arg}in = 68°$

Figure 3.18 shows the closed loop phase and gain plots while Figure 3.19 displays the open loop gain plots. These graphs, combined with the information in **Error! Reference source not found.** provides much insight into the performance of the PLL.

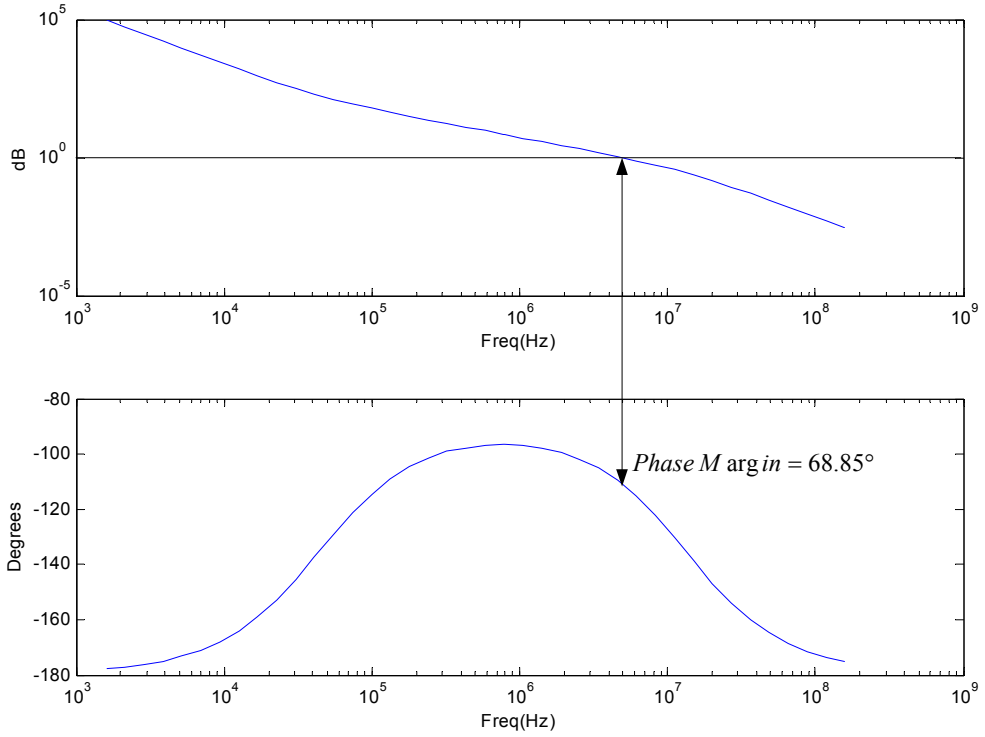


Figure 3.18 Plot of the Phase Response of the Simulated PLL

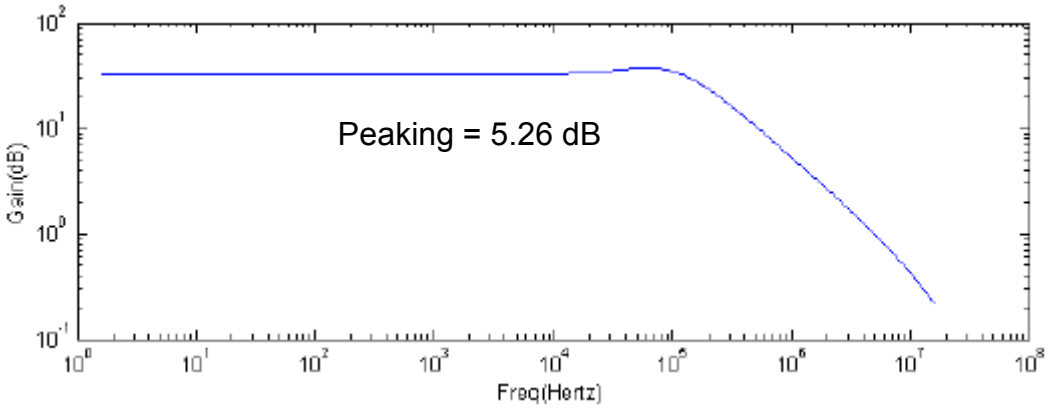


Figure 3.19 Gain of the Simulated PLL

With a phase margin of 68° the system should be quite stable. A damping factor of .9 also means that there will be no oscillations from a step input to the system, although such a large damping factor means that the system will be a bit slow to respond. One important thing that should be noted from this analysis is the dependence of the circuit performance on the actual value of C2. C2 is responsible for the placement of the third pole. Since at the time of simulation, it was unclear (based on the fact that an off-chip loop-filter was used) what the actual value of C2 would be. A rough calculation yields a value close to 10pF, the value that was used in this simulation. This is a fairly large value for the ripple-capacitor, which places the third pole at a fairly low value. In order to achieve the correct spacing of the loop-bandwidth, natural-frequency and the position of the zero, it is necessary to use a large R*Cp value to place the zero at a fairly low frequency. This in turn causes the damping factor to be large, which results in a stable, but slow-locking phase locked loop.

Although this uncertainty of the C2 value is caused by the fact that the loop-filter is placed off chip, the off chip loop-filter also presents us with a solution to the problem. Figure 3.20 shows how the loop filter can be used to adjust the performance of the phase locked loop.

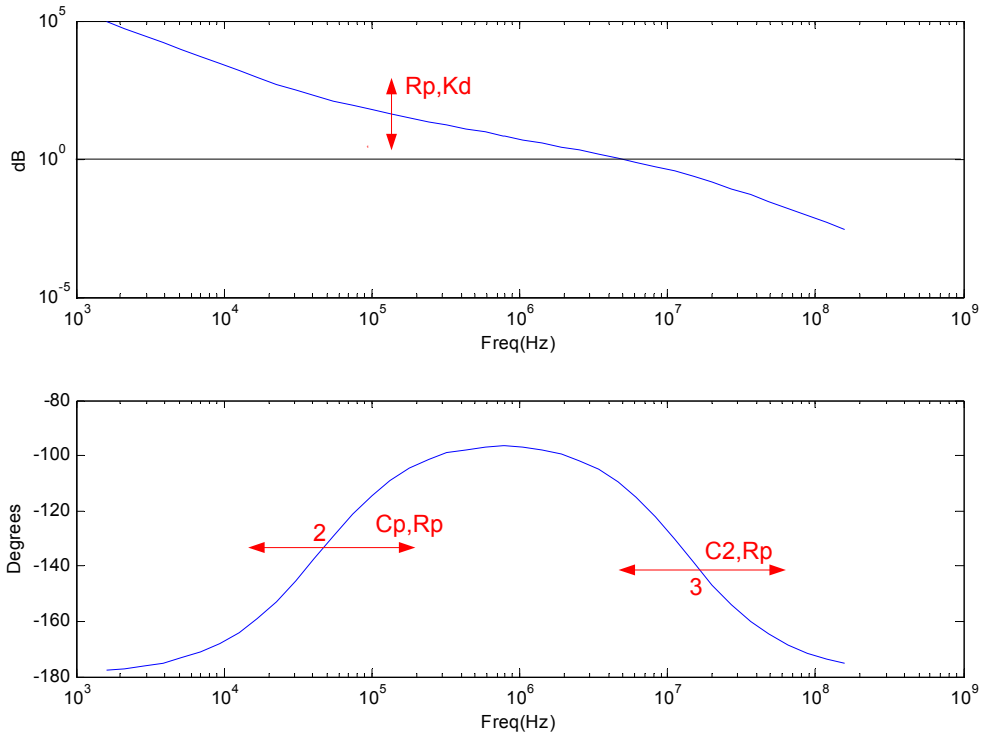


Figure 3.20 Effect of External Loop Filter Adjustment on the PLL

Figure 3.20 shows three vectors 1,2 and 3 that represent the effect of changing the parameters of the PLL. This graph should also give some insight into the benefits of using the off-chip loop-filter to tune the circuit. For example, if the C2 turns out to be much smaller than anticipated, Cp could be reduced and Kd could be increased in order to achieve the best locking-time and stability for the PLL. Likewise, if C2 turns out to be much larger than anticipated, then Cp could be made larger and Rp made smaller in order to preserve a good phase margin.

After calculating the necessary parameters for the PLL, and achieving good results from the numerical simulations, it is safe to attempt a longer circuit level simulation. Circuit simulations require several hours to complete, and take significant computing resources, it is necessary to simulate only sparingly. The PLL system is simulated with both Hspice and Cadence in order to gain confidence in the design. Cadence and Hspice each use different convergence algorithms and it is important to be sure that the circuit works with each. Figure 3.21 shows the result of the PLL circuit simulation. After $23\mu s$ the output

frequency of the PLL is exactly 32x the input frequency. Figure 3.21 depicts the output voltage at the loop-filter and shows the process by which the loop

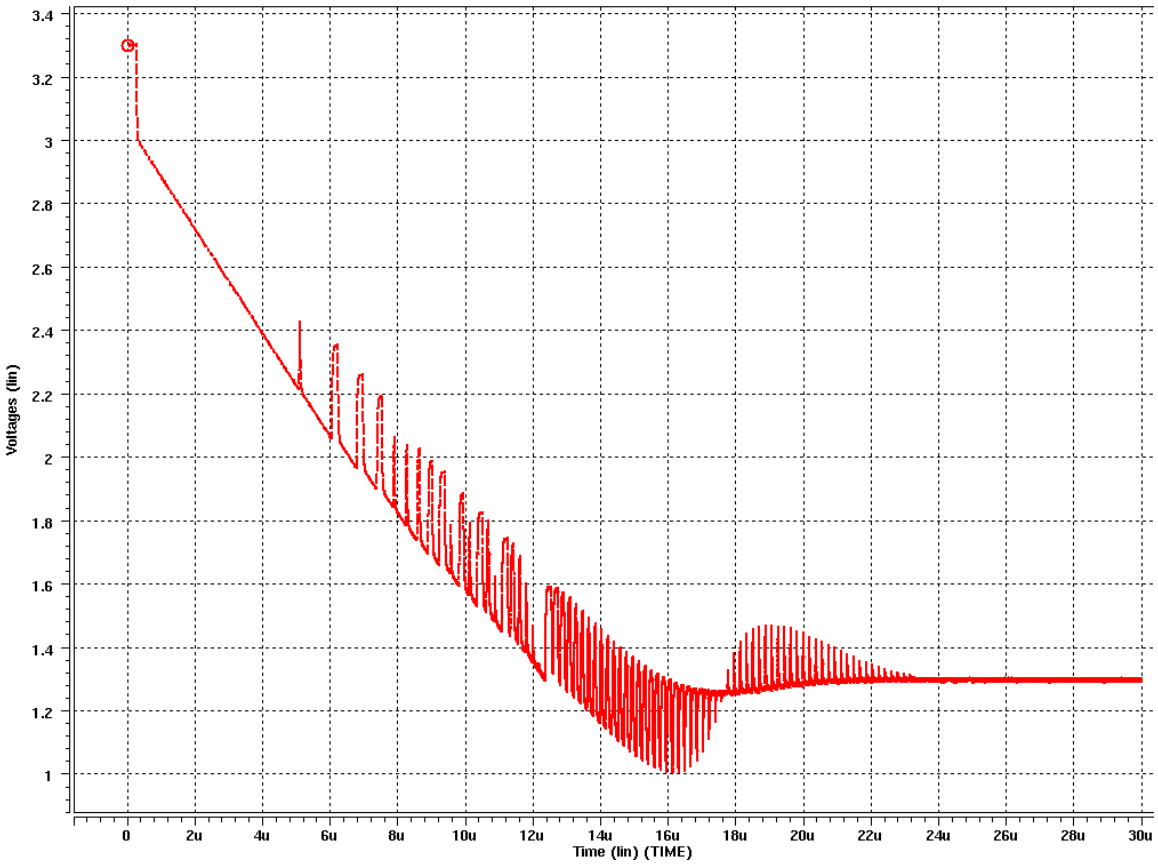


Figure 3.21 Circuit Simulation of the PLL Achieving a Lock

self adjusted the control voltage at the loop-filter in order to set the VCO to the desired frequency.

Simulating the PLL involves a number of different strategies in order to make sure that the final design will work. Usually different process corners are selected, the value of any integrated passive elements is varied by 20% and the effects of packaging are accounted for. In this specific case, limited process corner data was available. Only 'typical' devices were simulated. Bond wire inductance was assumed to be about 1nH and bond-wire pad capacitance was calculated at 10pF. Each I/O line was simulated with a series inductance and parallel capacitance of those calculated values. Since no passive components were integrated into this design, there was no need to take into account a 20% change in order

to accommodate process variation. Time was also spent simulating the effects of "powering-up" the circuit, and the effects of varying initial conditions.

After these circuit level simulations were complete, a silicon layout of the chip was completed. Figure 3.22 shows the layout of the PLL with the major blocks identified.

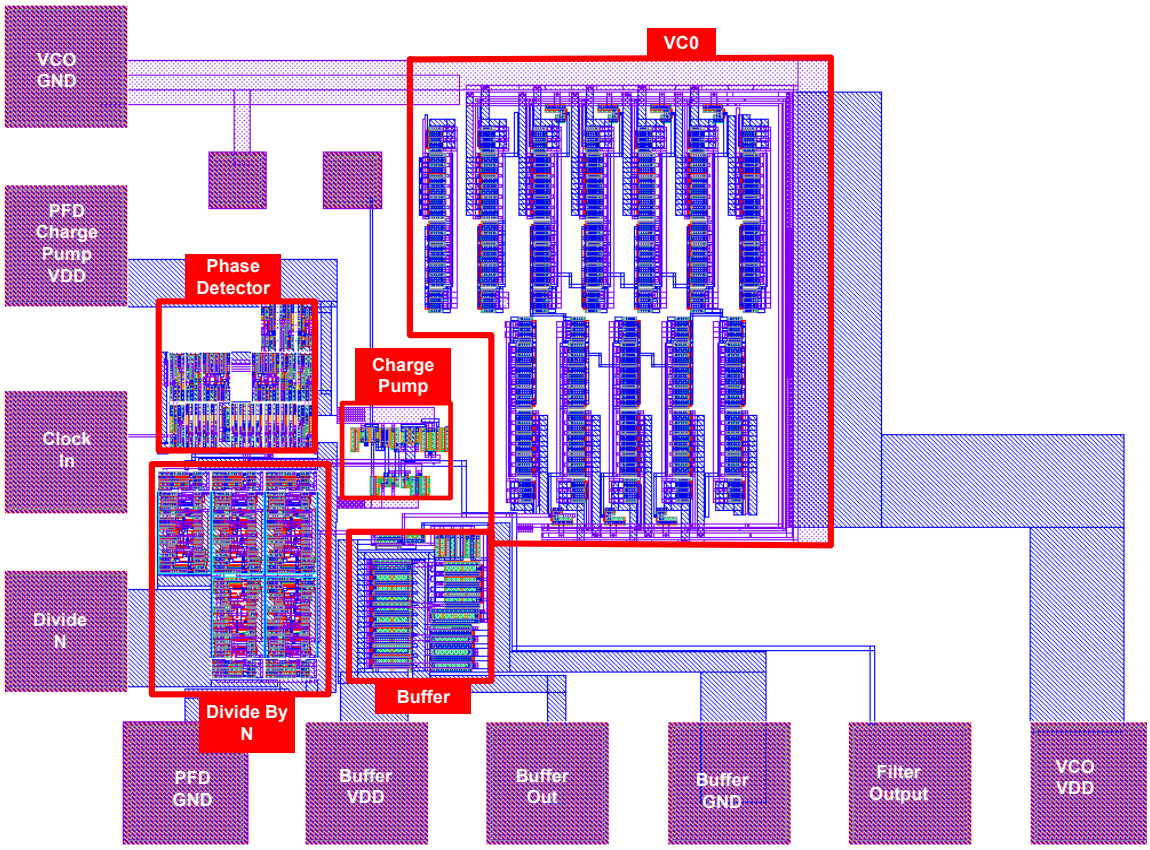


Figure 3.22 Layout of the PLL on the Chip

An important thing to note is the number and placement of the power supply pins. As mentioned before, the layout of this chip was shared with three other students. The division of die-space meant that the PLL was essentially confined to the corner of the die. There was also a constraint on the number of pads that were used, so some power rail 'sharing' between blocks was necessary. **Error! Reference source not found.** shows the assignment of I/O pads.

Table 3.5 Pin Assignments for the PLL

+ 3.3 Volts DC	VCO
	Phase Detector & Charge Pump
	Divide By 32
	Buffer
0 Volts DC	Phase Detector & Charge Pump & Divide by N
	Buffer
	VCO
Input and Output Signals	Clock In
	Buffer Out
	Loop Filter

There were a couple issues that took priority over the layout process. First, it was important to isolate the VCO from the other functional blocks. The VCO is operating at a much higher frequency than the other components and as a result generates 'switching' noise caused by the constant switching of states by the ring oscillator. This is a significant source of noise, and it is important that the other elements of the circuit not be exposed to this. It is also important that the VCO is isolated from the other sources of noise as well. For example, if the VCO were to share a power rail with the divide-by-N circuit you would see a significant voltage ripple on the supply line every 32 cycles when all 8 of the D-Flip Flops switched at the same time. This periodic ripple would actually modulate the frequency of the VCO and would cause a spurious tone to appear at the output of the VCO.

A second very important rule to keep in mind is that the output buffer consumes an incredible amount of power and must therefore also be isolated. In order to drive a 10pf load (pin capacitance) at 172 MHz, a very large output buffer stage is required. The current required to charge and discharge this loading capacitance can reach 40mA peak. Depending on the series inductance of the bond-wire, the package and the socket the

amplitude of the ringing can be large. Large oscillations on either the power or ground rails could prevent the VCO from oscillating and it could reset the values of the flip-flops in the divide-by-N circuit. Isolating the buffer from the other components is commonplace in modern circuit design.

3.4 Fabrication of the PLL

The PLL was one of the designs submitted to Honeywell for fabrication in the MOI5 fabrication in May 2002. The chip was fabricated and returned to NCSU in October of 2002. A package was chosen that accommodated the number of I/O for the chip as a whole, which was then bonded to the die by the technicians at the Jet Propulsion Laboratory. The chips were returned to NC State University in November 2002 to be tested. Figure 3.23 below shows a picture taken at NCSU of the die. One problem that was introduced into this stage was the difficulty in accommodating the large number of I/O pins on the chip. 64 total pins were required, which meant that a package with a large cavity was necessary.

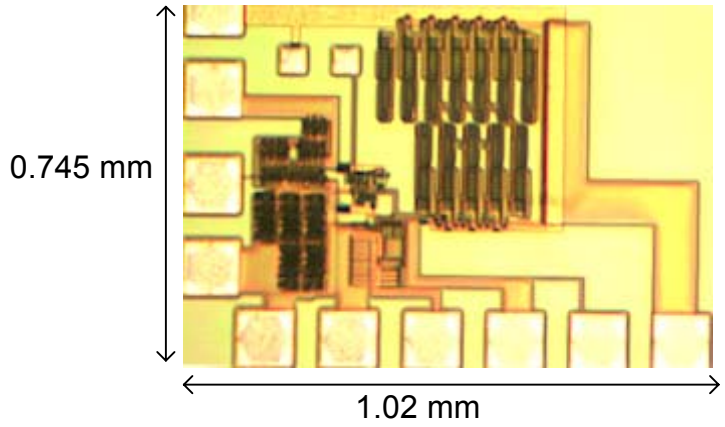


Figure 3.23 Picture of the Fabricated PLL

Unfortunately the size of the die was much smaller than the size of the package, as can be seen in Figure 3.24 .

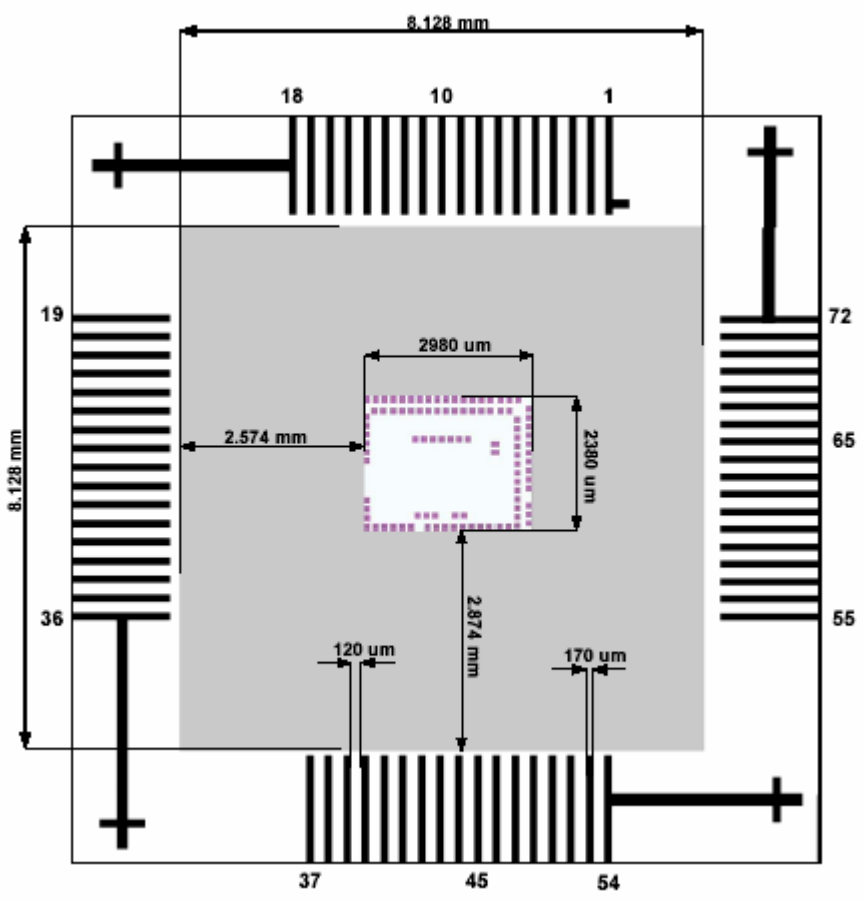


Figure 3.24 Placement of the SOI die in the Package

This large cavity to chip size ratio, necessitates the use of very long bond wires in order to connect the die to the package. These bond wires add series inductance and provide a way for noise to couple to the circuit. The effect of these bond wires on the circuit performance can be observed in the results of the testing.

3.4.1 Testing of the PLL

The PLL was tested in the ERL lab of NC State University. A test fixture was constructed from parts provided by lab. All signals were probed on chip with a high-impedance active probe (GGB Model 34A) affixed to a micro-manipulator. The signals were observed with a HPXX spectrum analyzer, and the 11801 and XXX oscilloscopes both by Tektronix. The test fixture was secured to a probe station, equipped with a video camera for use in guiding the probes.

Several factors greatly complicated the task of verifying the functionality of the PLL. First and foremost was the large series inductance that was introduced by the bond wires and packaging. This series inductance, caused a significant amount of resonance on the power and ground rails of all of the PLL blocks.

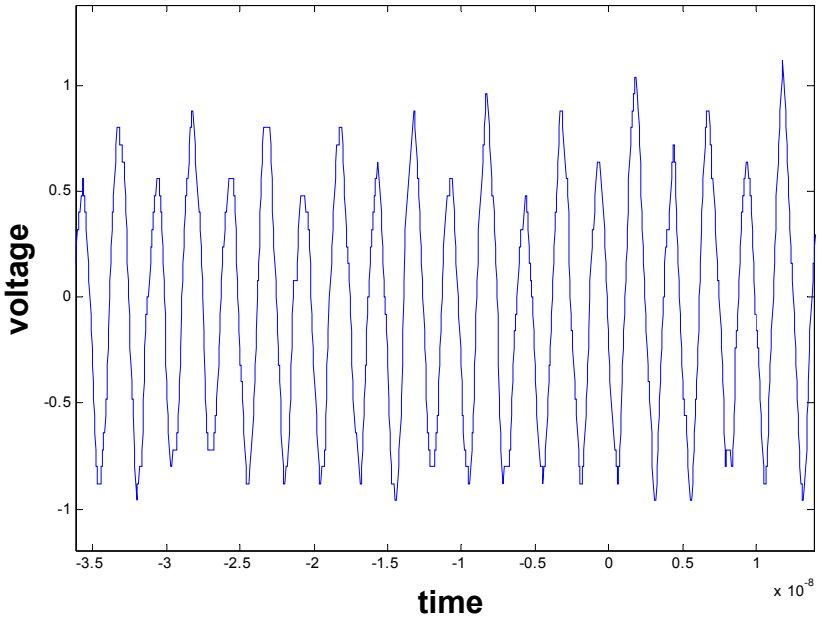


Figure 3.25 Noise on the Power Rail of the Output Buffer

Figure 3.25 shows a plot of the ringing on the ground node of the output buffer. The signal was probed on the bond wire pad on the die. The ringing is 2 volts in magnitude, enough to significantly alter the shape of the waveforms emerging from the output buffer. Since the buffer has it's own power and ground pins, this severe ringing does not prevent the operation of the VCO or digital circuitry. Instead, the rise and fall of the voltage available to the exponentially sized buffers causes the output waveform to bear a faint resemblance to the square wave it is supposed to be. Figure 3.26 shows how this severe ringing effects the output waveform of the buffer.

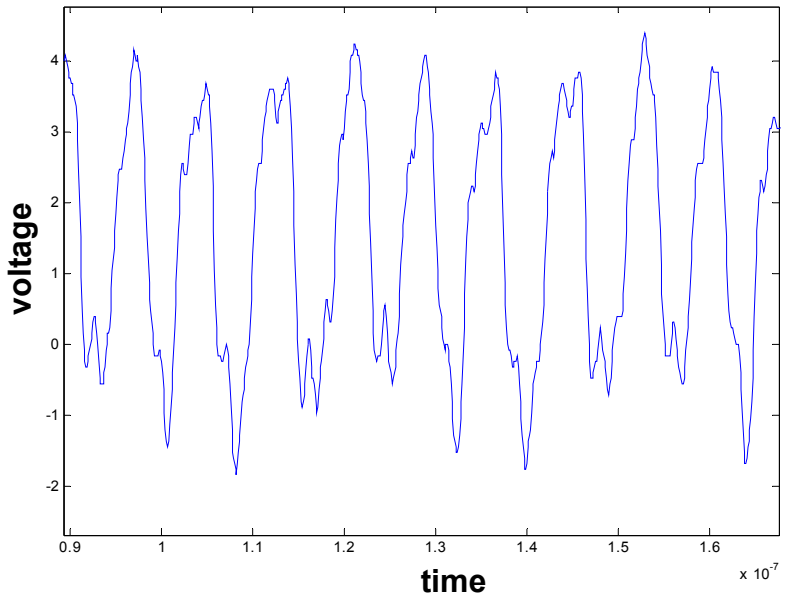


Figure 3.26 Output Signal of the Buffer

Notice that the amplitude of the signal rises and falls above and below the 3.3 voltage limit supplied by the power supply. Also, it is easy to see how the actual pulses vary in their width and shape, indicating that a resonance is taking place that alters the shape of this waveform. Through testing, it was found that the output buffer actually self resonates at frequencies between 120MHz and 135MHz. At self resonance the output waveform became aperiodic and the oscilloscope was unable to track and measure the frequency. This observation is insightful, in that it allows us to make some assumption about the inductive and capacitive elements in the circuit. Using the relation

$$\omega = \frac{1}{\sqrt{LC}}$$

We know that for a resonance frequency of 135MHz implies an LC product of $1.3899E-18$. This is a very large number, which implies that either the value of inductance, the capacitance or both are very large. The parasitic capacitance produced by the bond wire pads and the other metal traces in the circuit, is a fairly controlled and documented value. Based on the values given by the Honeywell electrical rules (a confidential and proprietary document) the total capacitance of a bond wire pad is about 61fF. The pin capacitance of the package could be in the order of 1pF to 20pF [24]. This

means that the series inductance of the package and bond wires would be anywhere from 1uH to 69nH. The inductance of a bond wire should be no more than 1nH per millimeter, which means that the series inductance of the bond wires used in this case should be no more than 3nH which means an package and socket inductance of at leas 66nH. This is an unrealistically large number, which implies that there is some parasitic capacitances unaccounted for on the die. Given the highly resistive substrate of SOI, calculating the parasitic capacitances of the metal layers is an exercise in futility. The capacitance coefficents are so small, that the difference between worst case and best case scenario is a few femto Farads. This leads me to believe that the parasitic capacitance is produced by the packaging and construction of the test fixture.

Figure 3.27 below demonstrated the second problem that complicated the testing process. The signal (between 40mV and 60mV amplitude) is the result of the signal from the output buffer coupling to the other areas of the die. Specifically, Figure 3.27 shows the signal probed at the loop filter, when all the blocks (including the charge pump) are turned on.

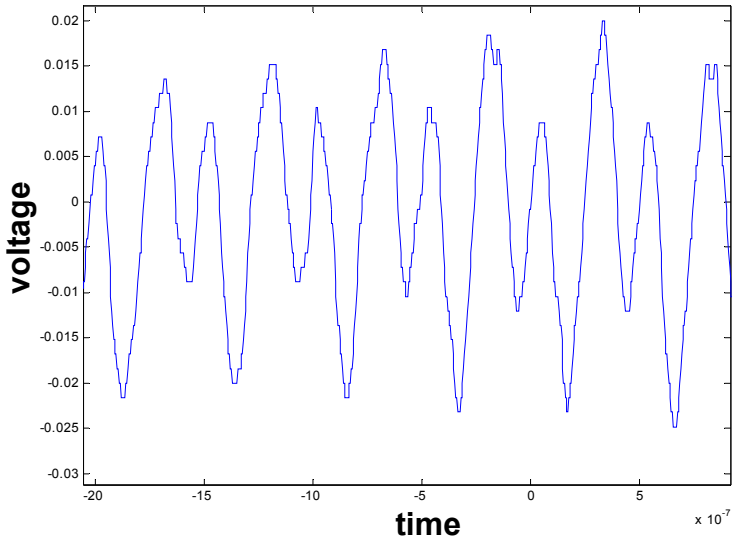


Figure 3.27 Capacitive Coupled Buffer Noise to other Nodes of the Circuit

Exactly twice the frequency of the output signal of the buffer, the peaks of this coupled signal coincide with the rising and falling edges of the output signal of the buffer. Such a

relationship implies that the large amplitude and fast rise time of the signal at the output buffer couples capacitively to the substrate and to other areas of the chip.

This capacitively coupled signal prohibits the correct operation of the PLL. The signal in Figure 3.27 comes from the loop filter, probed on-chip. This large amplitude signal overcomes the ability of the charge pump to correctly control the VCO. Instead, the coupled signal at the loop filter causes the VCO to oscillate around 195MHz (as expected since 195MHz implies a control voltage of 0v). This coupling prohibits the PLL from functioning, regardless of the input signal applied. For example, during normal operation, holding the input signal at Vdd (instead of providing the reference clock) should cause the voltage on the loop filter to rise causing the VCO to cease oscillation. Likewise holding the input signal to 0 volts should have the opposite effect. In the presence of the 'coupling noise' holding the input at either Vdd or Gnd had no noticeable effect on either the signal observed at the charge pump, or the frequency observed at the output of the buffer. Such behavior implies that either the charge pump is unable to overcome the effects of the coupled noise, or the coupled noise is so significant that it disrupts the operation of the phase detector or divide-by-N circuits.

These problems dictated the manner in which the PLL was tested. Since the PLL was unable to function correctly as a whole, it was necessary to validate the individual blocks or a combination of those blocks. For example, in order to observe any oscillation from the VCO it was also necessary to activate the output buffer as there were no internal nodes which could be used to observe the output of the VCO. On the other hand, in order to observe the functionality of the charge-pump, phase-detector and loop filter it was necessary to de-activate the output buffer for reasons listed above, and infer the correct oscillation frequency by observing the signal at an internal node of the loop filter.

3.4.2 PLL Testing Results

The PLL was tested in two phases. Phase one of the testing focused on the verification of the charge pump, phase detector, loop filter and VCO. The output buffer was disabled in

order to prevent the coupling noise from affecting other areas of the design. Since no output frequency was observable in this configuration, it was

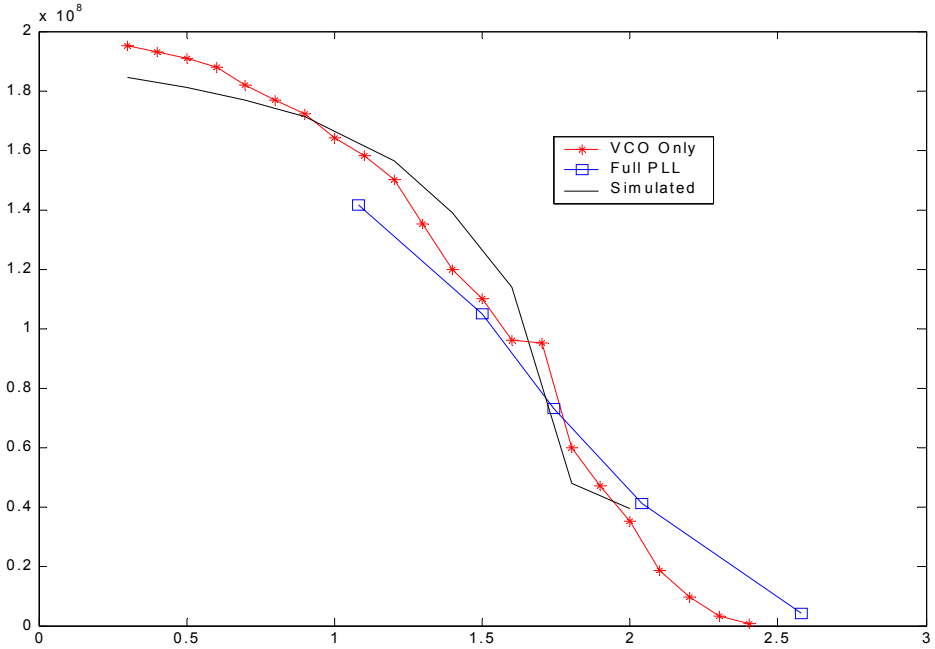


Figure 3.28 Plots of KVCO Based on Measurements and Simulations

necessary to infer the VCO frequency by observing the control voltage generated by the loop filter and charge pump. The reference clock frequency was varied and the changes to the control voltage were noted. A graph of the 'inferred' frequency appears in Figure 3.28 as the "Full PLL" line. Phase two of the testing involved only the VCO and the output buffer. A DC control voltage was supplied to the internal loop filter node by way of a DC probe. This setup allowed the VCO control voltage to be altered while observing the change in signal frequency at the output buffer. Figure 3.28 below shows the results of this experiment as the "VCO Only" curve. Access to the output signal in the second phase of testing also allowed some measurement of the performance. Timing jitter was measured with the 11801 Tektronix Oscilloscope which provides an easy method for measuring timing jitter. Figure 3.29 below shows the measurement screen. The average RMS timing jitter is displayed along with a graphical statistical distribution of the crossing point of the falling edge of the signal.

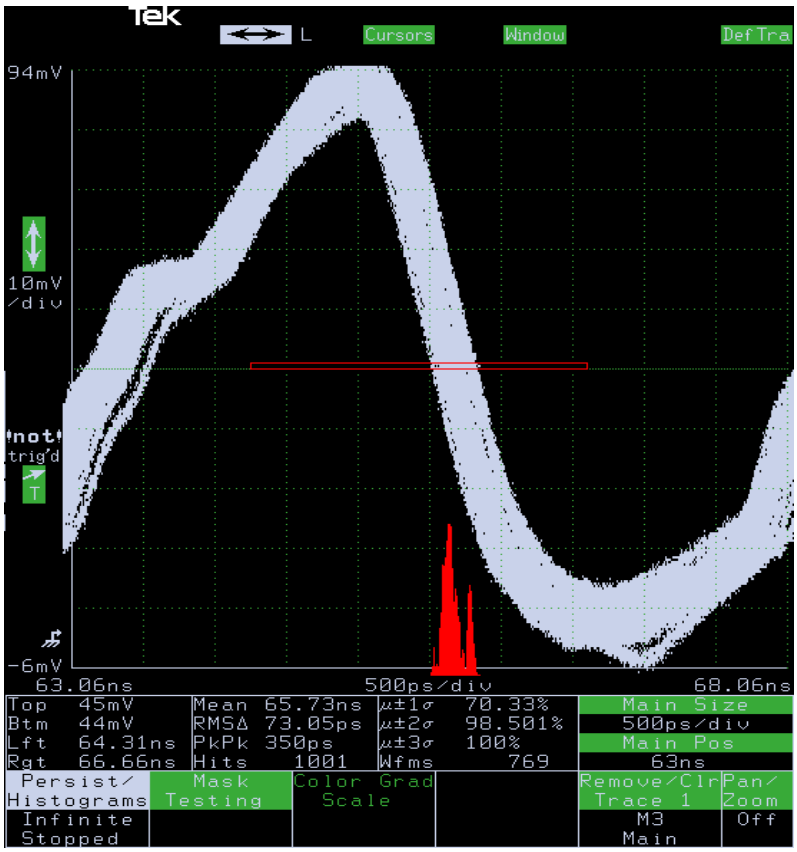


Figure 3.29 Jitter Measurement of the PLL

Error! Reference source not found. shows the results of the VCO jitter measurements. The data indicates that the RMS jitter increases as signal frequency decreases. This is to be expected for a couple of reasons. One, the jitter as a percentage of the period of the signal remains very close.

Table 3.6 Signal Jitter Compared to VCO Control Voltage

Control Voltage	Jitter (ps)	Frequency		Control Voltage	Jitter (ps)	Frequency
0	73.05	200 MHz		1.2	186.6	140 MHz
0.2	96.81	196 MHz		1.4	595.9	120 MHz
0.4	121	190 MHz		1.6	736.8	60 MHz
0.6	165.9	188 MHz		1.8	1046	40 MHz
0.8	132	172 MHz		2.0	1776	20 MHz
1.0	240.5	160 MHz		2.2	7000	5 MHz

With a control voltage of zero, and jitter of 73ps, the jitter is approximately 1.8% of the signal period. A control voltage of 2.2 Volts results in a jitter of 7ns which is approximately 3% of the signal period, not a large difference over the large tuning range of the VCO. Secondly, as signal frequency is reduced the sampling oscilloscope has a difficult time triggering on the signal, hence making the signal appear somewhat aperiodic. This causes significant deviations in the period of the signal displayed which the scope interprets as timing jitter.

3.5 Conclusions

The goal of this design was to investigate whether or not a frequency synthesizer could be fabricated in the Honeywell SOI process. The results obtained from the testing of the fabricated PLL indicate that this experiment successfully met that goal. A working PLL that was able synthesize the desired frequency (172 MHz) from a low frequency clock (~5MHz) was demonstrated. The charge pump, phase detector, VCO and loop filter functioned much as they did in simulation.

Several new techniques (besides the implementation in SOI) were investigated in this fabrication. The use of an off-chip loop filter, separate power and ground pins for each of the different blocks and an off chip signal driver were new techniques for this research group. The results are mixed.

The use of an off-chip loop filter turned out be functional, but not desirable. The fact that a large series inductance was placed in series with the RC elements of the loop filter resulted in a larger amount of jitter than originally anticipated. Since the fabrication of this chip, more confidence has been gained in the fabrication of passive circuit elements in the SOI process. While accessibility of the loop filter allowed greater insight into the functionality of the PLL, in the future it would be better to trade better performance for accessibility.

The use of separate power and ground pins for each of the functional blocks by and large saved this design from certain disaster. Verification of the separate components of this

PLL made this fabrication worth the money spent. Future designs of frequency synthesizers will most definitely include separate power and ground pins

Bringing the output of the VCO off chip through a large buffer turned out to be a mistake. The amplification of a high frequency signal with large buffers that draw current through highly inductive power and ground lines turned out to cause many more problems then it solved. It would have been a much wiser choice to simply include a probe pad at the output of the VCO so that a high impedance probe could be used to verify its functionality without requiring the noisy buffering that was employed in this design. In the future, any output buffers that are used will employ very, very large decoupling capacitors on-chip on the power and ground rails. Also, any off chip signals will use a reduced swing buffer that will allow the tester to reduce the voltage swing of the output signal to reduce the resonance and signal-coupling problems that were observed in this work.

While the PLL fabricated in this exercise would most likely be unsuitable for the requirements of a digital communication architecture, the lessons learned will allow the future successful fabrication of such a component. Layout technique, design procedure and circuit implementation of a frequency synthesizer have been refined as a result of this process.

Chapter 4
Characterization of the Honeywell SOI devices and circuits

As explained in the introduction, one of the main purposes of the first SOI fabrication was to verify the functionality of the devices and circuits that will be used in the later versions of the frequency synthesizer. To this end, various single MOS devices and ring oscillators were fabricated. The results were collected and analyzed provided insight into the abilities of SOI to be used in RF frequency synthesis. One of the primary goals of this characterization of devices and circuits was to determine the effects of device layout technique on the characteristics of the device and the circuits that utilize them. Device layout technique (explained in Appendix 1) is not modeled for in the device libraries, which adds risk to the fabrication of a chip. It is important to find out before fabrication of the final SOI receiver if (for example) one layout technique is more reliable than another or if one layout technique is more sensitive to process variations or has a large un-modeled parasitic capacitance. These factors will greatly affect the matching or performance of the device. The devices and oscillators that were fabricated for this purpose were not randomly chosen. Each oscillator was designed for a possible implementation in a future RF frequency synthesizer. Different device sizing and layout techniques were used for each oscillator to test different concepts. The size and layout technique of the individual devices was also carefully to resemble the devices that were used in the oscillators.

4.1 Individual Device Characterization

Individual MOS devices provide insight into a number of characteristics of the process. With a parameter analyzer the DC characteristics can be measured which provides information on the threshold voltage and the process corner of each device. With more elaborate configurations, A device can be used with off chip passive components to provide information on the AC characteristics and the noise of the device.

4.2 Design and Layout

For the purpose of characterization, it was necessary to fabricate devices with body tied-to-source (SB) and body independently biased (BT) layout techniques. Figure 4.1 shows examples of the layout of each of these devices.

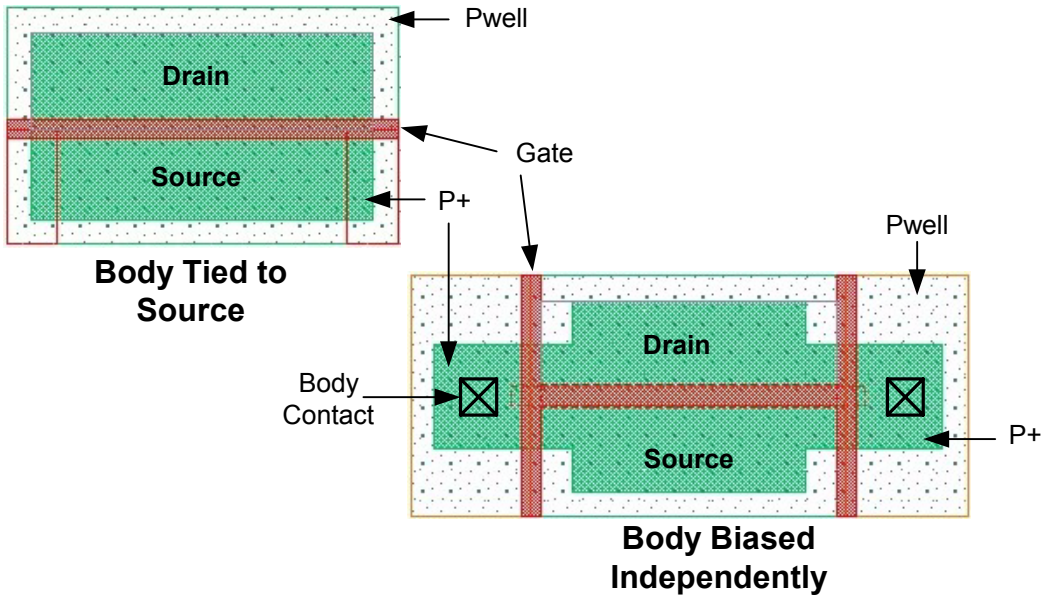


Figure 4.1 Layout of Devices

In order to characterize each device it is necessary to access the gate, source, drain and body (if available). In a chip with limited die area, it was not practical to have separate external gate, source, drain and body pins for each device, so a method of sharing pins was devised. The source of each device is tied to a common node. This source node is tied to an external pin on the package. The gates and bodies (of the BT devices) are also common nodes which are tied to pins on the package. It is necessary, to have the drain of each device on its own pin, so that the device can be tested independently. Figure 4.2 demonstrates how this was done in the layout.

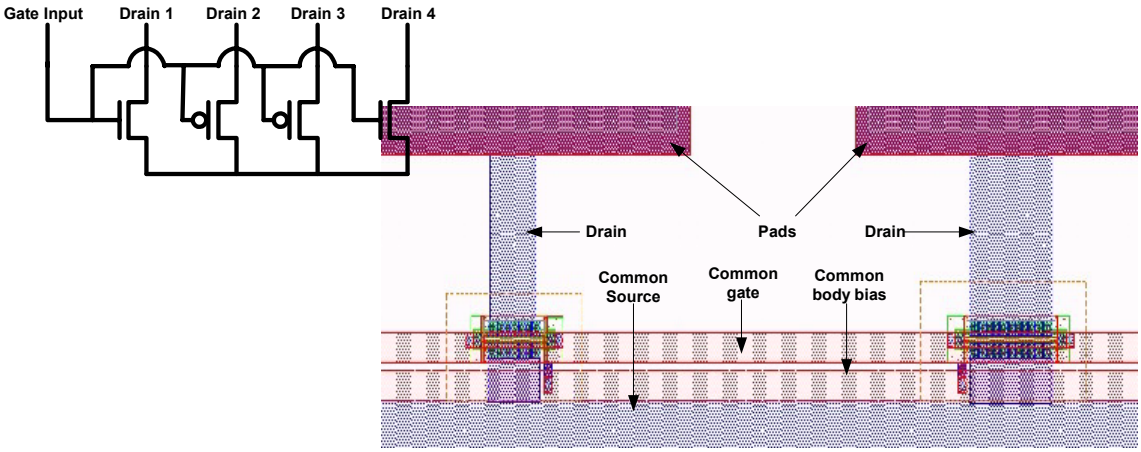


Figure 4.2 Arrangement of Devices on the Die

Many single devices were tested, using more I/O pins than any other design on the die. In order to accommodate this large number of pins and establish some kind of uniformity among the devices, it was necessary to place the devices and their I/O pins on the periphery of the chip. Figure 4.3 shows the location of the individual devices on the final layout.

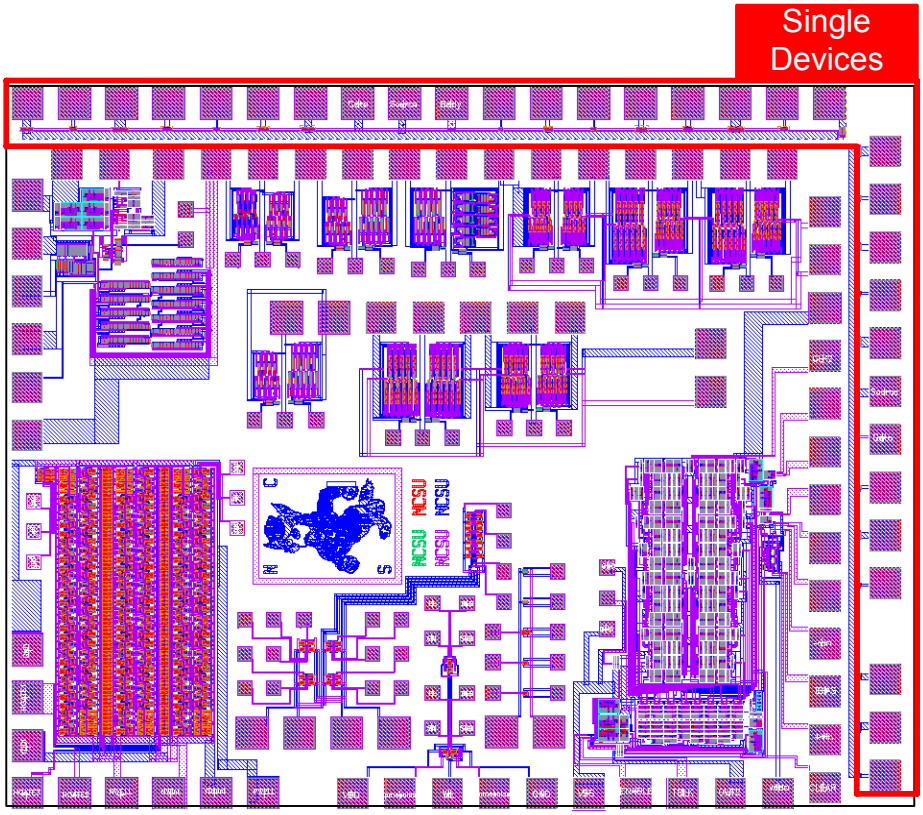


Figure 4.3 Peripheral Location of Individual Devices

The top side of the chip is populated by the SB devices and the right-hand side of the chip is populated with BT devices. Appendix B features a list of the individual devices that were tested.

4.2.1 Individual Device Testing

Analysis of the DC parameters of the devices was accomplished with a Agilent XXX parameter analyzer. A test fixture was designed to interface with the test equipment, and is shown in Figure 4.4.

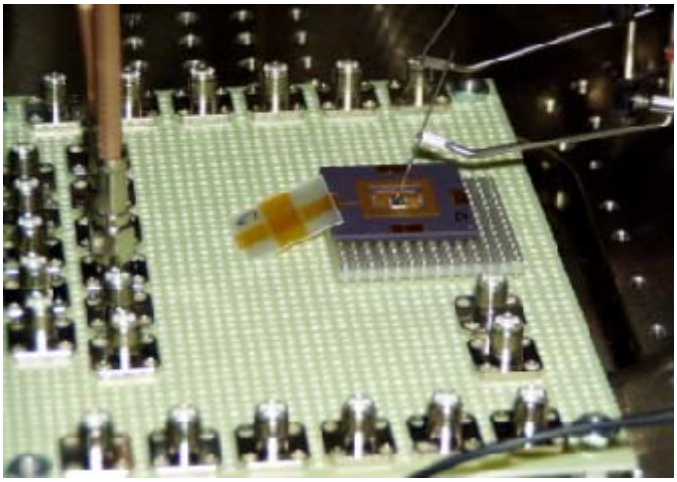


Figure 4.4 Test Fixture

4.2.2 Individual Device Results

Each device on each die was tested. At first, four die were received by NC State University for test, so the test results not only show the results of the device test, but also offer some idea of the process variation that occurred across the wafer. The results obtained were compared to simulated results of the extracted layout simulation. **Error! Reference source not found.** and **Error! Reference source not found.** show the devices that were tested. The Matlab plots of the data from the tests can be found in Appendix B.

Table 4.1 Performance of Body Biased Devices

Device Type	Length	Width	Performance
PMOS bt	600n	27.75u	slow
PMOS bt	600n	13.75u,14u	typical>x>slow
PMOS bt	900n	18u	typical>x>slow
PMOS bt	900n	27u	slow
PMOS bt	900n	18.5u	typical>x>slow
PMOS bt	900n	18.5u	typical>x>slow
PMOS bt	600n	13.5u, 13.5u	typical>x>slow
NMOS bt	600n	4.4u,4.85u	>> fast
NMOS bt	600n	9.25u	fast
NMOS bt	600n	4.85u,4.4u	>> fast
NMOS bt	900n	6u	>> fast
NMOS bt	900n	6u	
NMOS bt	900n	6u	>> fast
NMOS bt	600n	9.25u	fast

Table 4.2 Performance of Source Tied to Body Devices

PMOS sb	950n	19u x 4	<< slow
PMOS sb	600n	27u	<< slow
PMOS sb	900n	18.5u	<< slow
PMOS sb	600n	27.75u	slow
PMOS sb	900n	18u	<< slow
NMOS sb	600n	9.25u	fast>x>typical
NMOS sb	900n	6u	>> fast
NMOS sb	600n	9.25u	typical
NMOS sb	900n	6u	fast
NMOS sb		950n,6u,m=5	fast

Process Corners Revealed

The results of the four chips were averaged and plotted against the 'fast', 'typical' and 'slow' library models. The tables above show these results. In all cases the NMOS devices were in the fast process corner and in all cases the PMOS devices were in the slow

process corner. Figure 4.5 gives a more insightful presentation of that data. On the top the average process corner of the body biased devices appears and on the bottom the average corner of the source - body tied devices are shown.

It was interesting to find that the process variation between the two layout techniques on the same die. While the mean difference between the NMOS and PMOS devices are the same for either of the layout techniques, The 'average' process corner of the body biased devices would be slightly above 'typical' while the average for the source tied devices would be slightly below typical. This wouldn't have too much of an effect on the circuit designer unless they were to 'mix' different layout styles in the same circuit. In which case the circuit would necessarily have to deal with extreme process variation.

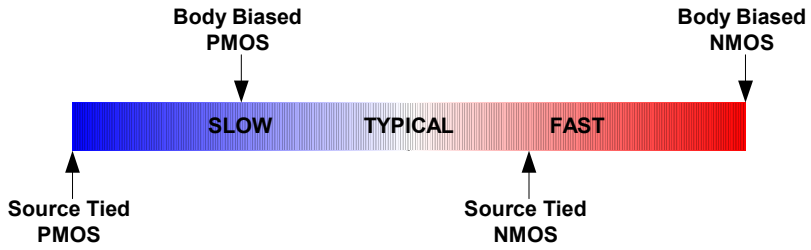


Figure 4.5 Process Corners of the Fabricated Devices

The ratio of β_n to β_p was expected to be between 2.4 and 3 according to the library parameters and simulation. The actual value turned out to be 6 due to a smaller NMOS threshold voltage and a larger PMOS threshold voltage. If circuits were to be mixed with devices of the source tied and body biased layouts, it is possible for a Beta ratio as high as 10. This would be much greater than anticipated by the library and would make oscillator, or any threshold dependent circuits operate poorly.

Variable Threshold Verified

It was hypothesized that adjusting the DC bias of the body in the body biased devices would cause the threshold voltage to scale proportionately. This effect was verified by

measurement Figure 4.6 shows the results.

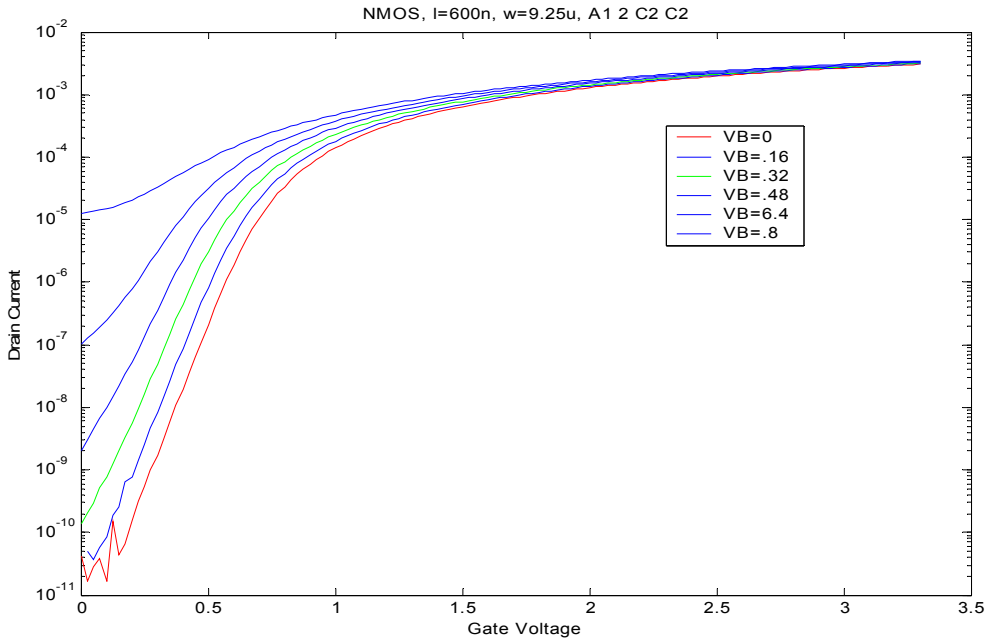


Figure 4.6 Effect of Body Bias on Threshold Voltage

In this experiment, the bias voltage of the body was increased incrementally from 0 to .8 volts. From the graph, it can be seen that the threshold voltage is reduced from a value slightly less than .6 volts to a value of about .3 volts. The subthreshold current slope remains fairly constant throughout this voltage shift, meaning that the device 'off' current is minimized.

Other Observations

Some of the other observations were cause for concern. Because four chips were tested, some insight was gained into the variation of the devices across the wafer. Although it is not known where on the wafer the chips originated, sometimes the variation could be quite bad. In some cases the same device on different chips might have a 4% to 5% variation in the DC current. This could cause significant problems if a variation of this sort were to occur in a current mirror, or in some other circuit where matching is important. Even on chip variations occurred. Figure B.22 and Figure B.25 in Appendix B show the possibilities for on-chip variation. These devices were fabricated on different sides of the die, allowing them to be more susceptible to variations during processing. In

one case, the results are consistent across the four chips measured. For the other device, the results vary among the different chips. Such results reinforce the need for process independent layout

4.3 Individual Device Conclusions

The results gathered from the individual devices was useful in several ways. Most importantly, it was verified that the devices are indeed functional and perform more or less close to what was predicted by the models. Secondly, the functionality of the independent body bias for reducing the threshold voltage was verified. Lastly, insight was gained into what can be expected in the actual fabrication environment. Circuits fabricated in this SOI process can not be sensitive to process corners, or on chip process variation. Knowing this information will allow future versions of the frequency synthesizer to be fabricated much more reliably.

4.4 Oscillator Characterization

The ring oscillator serves as the basic building block of the voltage controlled oscillator that would be used in the digital receiver architecture. In this work, the ring oscillators characterized were simple inverter-chain oscillators, configured as shown in Figure 4.7. The oscillator operates on the principle that that a total phase shift of 360 degrees is established around the loop by each stage contributing a phase shift of (negative) $180° / N$. Additionally, a DC phase shift of $180°$ is provided by each stage, requiring an odd number of stages in order for the system to be unstable (and therefore oscillate).

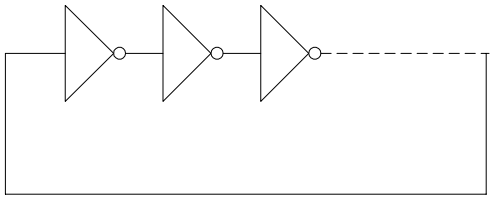


Figure 4.7 Structure of the Fabricated Ring Oscillators

4.4.1 Oscillator Design Overview

The process of designing a ring oscillator to meet the desired frequency with a minimum of noise takes some care. Time must be taken to size each transistor carefully in order to meet the desired free running frequency and time must be taken to insure the best possible 'symmetry' at each node of the oscillator. Symmetry has a significant impact on the operation and performance of the ring oscillator. Chapter 3 contains an in-depth explanation of the impact of symmetry on oscillator performance. Symmetry, in a sense, is the process of insuring that circuit components are balanced. The rise time of a signal should be the same as the fall time. The loading capacitance of each stage of the ring should be the same, and no one stage should have significantly different process variation than any other stage. This quest to obtain a symmetrical oscillator begins at the circuit design stage and is a constant process that continues on through the layout. The combination of all of these concerns, is a sometimes tedious task that required much design and re-design in order to come to a final product.

The simplicity of each stage of the ring oscillator (single inverters) greatly simplifies the circuit design process. It is first necessary to calculate the delay of each stage. The delay of each stage is ultimately a function of the rise and fall time of the output of the stage [25] [26]. The time it takes for the output to go from low to high (or high to low) is governed by the dynamics of an RC circuit were the voltage as result of a step input is a function of time:

$$V(t) = Vdd - Vdd \cdot e^{\frac{-t}{RonCl}}$$

Where it can be assumed that the rise (or fall) time of the signal is the point at which the output is equal to 90% of its final value. Setting Equation XX equal to 90% of the final value and solving for t, yields the rule of thumb regarding the rise/fall time of the signal.

$$2.2 R_{on} C_l = t_{rise}, t_{fall}$$

Based on the assumption either of the transistors in the inverter will spend most of it's switching time operating the saturation region [25] allows the effective 'on' resistance to

be calculated from the small signal circuit model. Assuming the gate to source voltage is approximately Vdd:

$$Ron = \frac{Vds}{gm \cdot Vds} = \frac{1}{gm} = \frac{1}{\beta(Vgs - Vtn)} = \frac{1}{\beta(Vdd - Vtn)}$$

And Cl is the load capacitance at the output of the inverter. The load capacitance (explored in greater detail in Appendix A) can be calculated from the information given in the process library and the device geometry. Given the intrinsically low parasitic capacitance of SOI, it was not necessary to repeat this calculation for each oscillator design. Instead the parasitic capacitance was calculated once, using the standard equation for gate to drain capacitance [27].

$$C_{gd} = Cox \cdot W \cdot Lov$$

Where Lov is the distance that the gate overlaps the highly doped drain region. Since the voltage swing at the input and output of the inverter will be the same, it is possible to 'millerize' the capacitor, and represent the capacitance as a single linear capacitor attached to the output of the inverter with value $2C_{gd}$.

These equations relating the operating frequency of the ring oscillator to the number of inverter stages, and the propagation delay of each stage allows the use of a spreadsheet in the design of the ring oscillator. Known values (such as number of stages, and the device length) can be entered into the spreadsheet, and then the widths of the devices can be adjusted until the specifications are met, then the design can be simulated using a circuit simulator.

4.4.2 Oscillator Simulation and Layout

Although, not 'design by iteration' the simulation process required more adjustments to the circuit parameters. To begin with, it was necessary to verify the exact β_p / β_n ratio in order to guarantee equal rise and fall times for each stage. This verification was done by connecting the output of a single stage inverter to a load capacitance and connecting the input to a square wave generator.

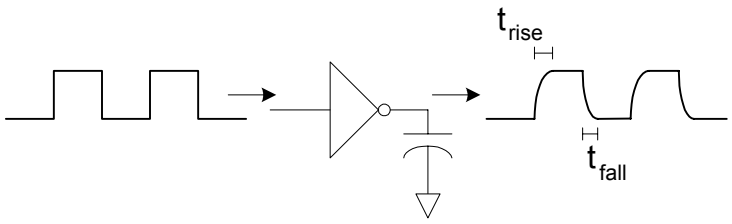


Figure 4.8 Method for Achieving Equal Rise and Fall Time

The width of the N and P were adjusted until the rise and fall times were equal. The resulting β_p / β_n ratio turned out to be greater than 4. However, there was some variation to this depending on the device sizing. It was therefore necessary to go through this rise/fall time testing at the start of the oscillator simulation process.

In order to further insure symmetry, an output buffer was attached to each stage. It is necessary to observe the oscillating signal, however that signal will only be tapped from one node. The desire to equally load each stage means that no one node can be 'probed' otherwise the capacitive load of the probe tip would cause that stage to have a greater load than the others. It is necessary to buffer the output of the stage from which the output signal is tapped, but this buffer will also load the stage. It is therefore necessary to place output buffers at each stage of the ring oscillators, and take only one of those outputs to the probe pad.

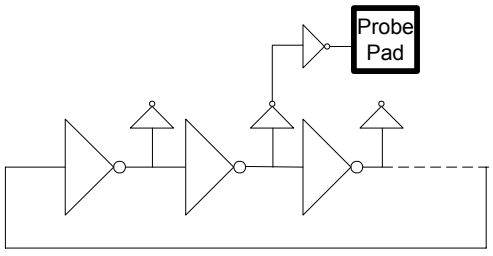


Figure 4.9 Equal Loading of Each Stage

Special care was also taken in the layout to make sure that each stage was identical. One such precaution was the creation of dummy inverter stages (Figure 4.10.a). The Dummy stages prevent any one stage from being on the edge of the circuit and therefore exposed

to different process conditions than the other stages. The Dummy stages contain the same elements of the other stages, but are not connected to a power source.

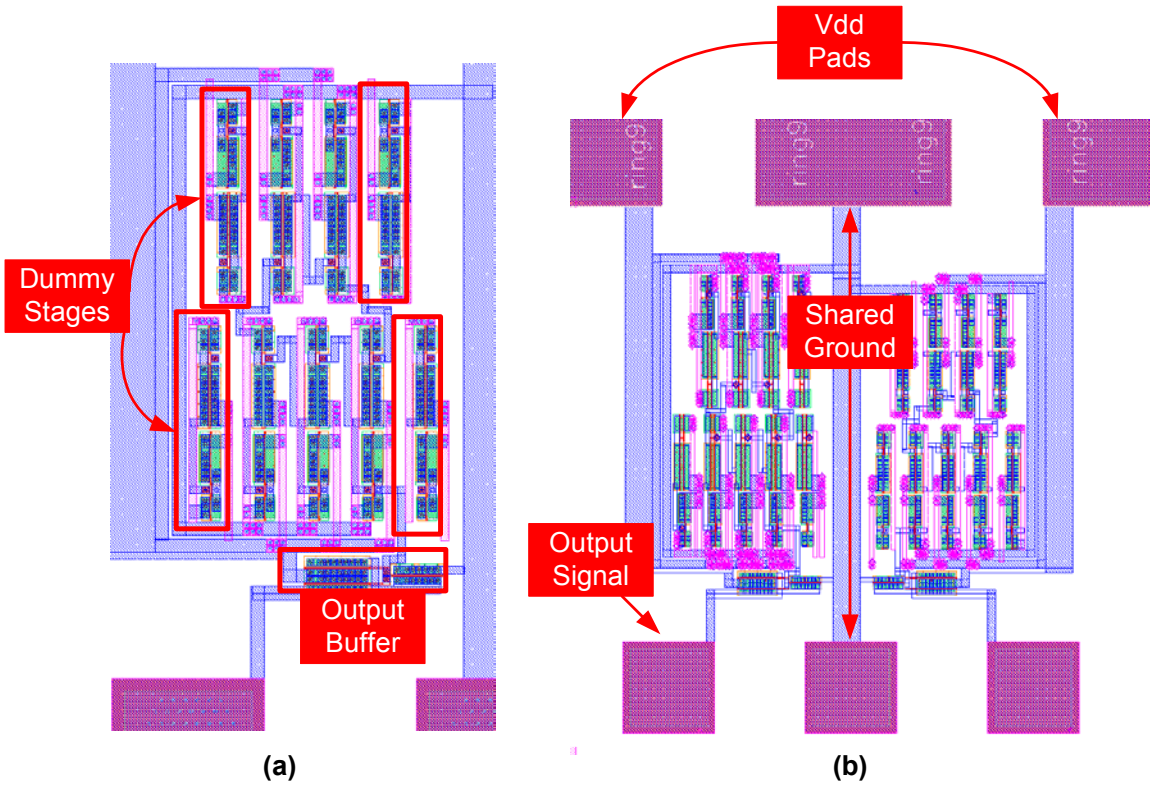


Figure 4.10 Layout of Ring Oscillators

Another precaution taken to assure that each stage was identical, was to carefully make sure that the amount of interconnect (in this case only metal1) is the same at the output of each stage. If there is a significant difference in the amount of interconnect one stage is required to drive, the result is a stage that experiences a higher capacitive load and therefore has a different behavior than the other stages. To insure that the amount of interconnect is the same, it was necessary to orient the inverter stages so metal 1 could be used to connect each stage to the other. Figure 4.10.a and Figure 4.11 show how this results in configuration that has a circular look. In addition, it was necessary to carefully measure the area of metal 1 that each stage had to drive. The process for this, required that the end stages (sides of the rectangle) were connected first, and then measured to be sure that each side had equal metal. These stages were connected first because these sides required the most interconnect to cover the large distance. To connect the other stages it

is a matter of determining how to fit the necessary amount of interconnect into the space provided. This process was one of the more time consuming and tedious tasks of the layout.

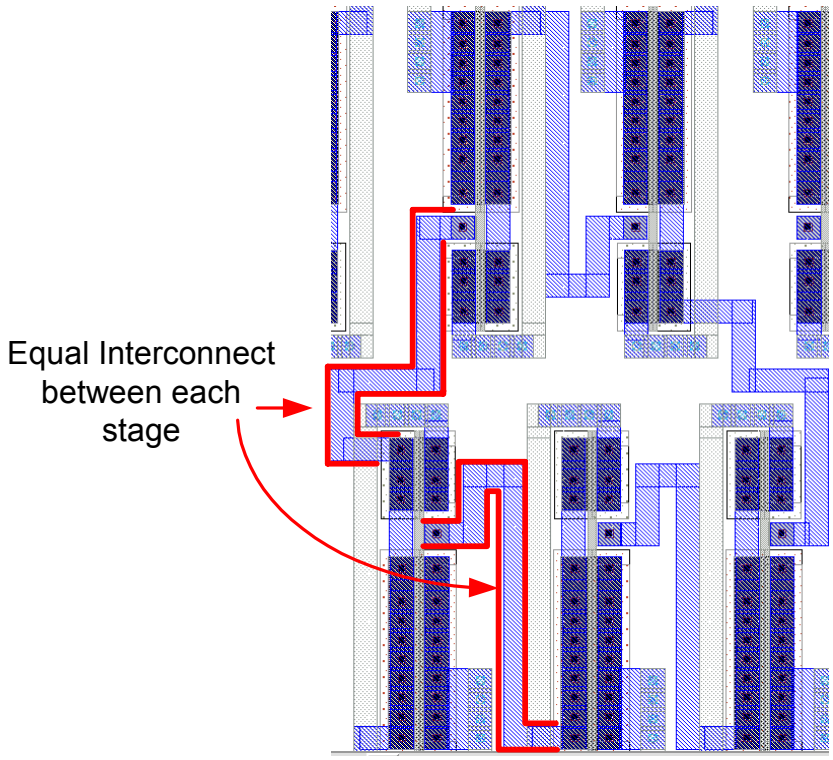


Figure 4.11 Equal Interconnect Between Each Stage

Figure 4.10.a and Figure 4.10.b also show the architecture of the oscillators and these oscillators were constructed on the test chip. Figure 4.10.b shows that the output signal can be observed from a probe pad that is compatible with either the single ended high frequency probe or the 29.a probe which requires a signal pad and a ground pad. The signal is amplified by a pad-driving buffer that takes the signal from the output buffer of the ring oscillator. Figure 4.10.b also shows how pad space was conserved. Since the I/O of the die was limited, it was necessary to share as many pads as possible. In order to make the pad use efficient, each bond wire pad is used by two oscillators. However, no oscillator shares both a power and ground pad with any single other oscillator. An oscillator may share it's Vdd pin with the oscillator to its left, but share its Gnd pin with the oscillator to the right. This means that there will never be an instance where two oscillators are powered on at the same time.

Error! Reference source not found. lists the ring oscillators that were constructed and some notes explaining the purpose of each.

Table 4.3 List of Oscillators Fabricated

	Frequency	Device Length	NMOS Width	PMOS Width	Stages	Layout Technique	Notes
1	355 MHz	.5u	6.75u	21u	5	FB	
2	413 MHz	.95u	4 x 6u	4 x 19u	5	SB	
3	419 MHz	.95u	4 x 6u	4 x 19u	5	BT	
4	352 MHz	.9u	6u	18u	5	BT	
5	365 MHz	.9u	6u	18u	5	SB	
6	364 MHz	.9u	6u	18.5u	5	SB	Large PMOS to test Symmetry
7	352 MHz	.9u	6u	18.5u	5	BT	Large PMOS to test Symmetry
8	546 MHz	.6u	9.25u	27u	7	SB	
9	492 MHz	.6u	9.25u	27u	7	BT	Modified Body tie layout
10	537 MHz	.6u	9.25u	27u	7	BT	
11	545 MHz	.6u	9.25u	27.75u	7	SB	Symmetry Testing
12	490 MHz	.6u	9.25u	27.75u	7	BT	
13	537 MHz	.6u	9.25u	27.75u	7	BT	
14	544 MHz	.6u	9.25u	27.72u	7	BT	Test of new technique
15	544 MHz	.6u	9.25u	27u	7	BT	Test of Pi gate

4.4.3 Oscillator Testing

The test fixture featured in Figure 4.4 was also used for the oscillator testing. The power, ground and body biases were provided off chip by DC power supplies. All signals were probed on-chip with the GGB 34A high impedance probe which was affixed to a micromanipulator. All time domain measurements were made with the Tektronix 11801 oscilloscope and frequency domain measurements were made with the XX.X Spectrum

Analyzer. Frequency measurement was performed with the frequency measurement utility of the Tektronix oscilloscope. Due to the low power consumption of the ring oscillator circuits, there were few problems with the power and ground ringing that was experienced with the VCO in the PLL. Although there was some 'ringing' due to the use of a buffer circuit to drive the probe-pad, for the most part the signals reached their full swing value. One of the most frustrating problems encountered during the testing of the oscillator circuits was the delicacy of the 34A high impedance probes. Slight movements of the probe on the probe pad could either enhance or degrade the signal quality. Sometimes, the difference between a 'good' measurement and a 'bad' measurement was just a slight adjustment of the micromanipulator. This issue will be explored in greater depth in section 4.5.1.

4.4.4 Oscillator Frequency Results

The frequency of each oscillator was measured, and the results along with the simulated frequency appear in Table.

Table 4.4 Frequencies of Fabricated Oscillators

	Oscillator Name	Schematic Simulated Frequency	Extracted Simulated Frequency	Measured Frequency
1	ring9_fb	355.11	330.2	340
2	ring10_sb	413	383.1	460.829
3	ring13_bt	352.7	295	323
4	ring9_sb	365	330	367.647
5	ring 14_sb	364.9	326.6	373.134
6	ring15_bt	352	296	336.7
7	ring11_sb	546	488	515.464
8	ring16_bt	492	368	409.836
9	ring17_bt	537	440	497.512
10	ring12_sb	545	491.2	515.464
11	ring18_bt	490	370	411.523
12	ring19_bt	537	440	512.821

The column labeled 'schematic simulated frequency' contains the results of the first simulations with the oscillators. For these simulations, the delay of each stage of the ring inverter is based on the parameters given in the process library. Variables like source and drain area are estimated and the effects of the layout are not calculated. The column labeled 'extracted Simulated Frequency' contains the results of simulations conducted on the extracted layout. These simulations take into account the various parasitic resistances and capacitances that are introduced by the layout design. The last column the 'measured results' column shows the results that were observed on the actual chip.

These results reveal some interesting information about the oscillators that were fabricated. Ideally, the measured frequency of the oscillators should have been very close to the 'extracted simulated frequency', as this usually gives the circuit designer the best insight into how the circuit will actually function on the die. In the case of this fabrication, that wasn't the case. In every single case the measured frequency of the oscillator was larger than the extracted simulation, and in a few cases this frequency was larger than even the schematic simulation. Rarely is the actual frequency of the oscillator larger than the schematic simulation, since much of the loading capacitance is not figured in to those simulations. Another thing to note about the data presented in **Error! Reference source not found.**, is that proximity of the measured frequency to the simulated frequency has some dependence on the layout technique used and the operating frequency of the circuit. Figure 4.12 tries to make some sense of this.

Figure 4.12 presents three comparisons, to provide some insight into the variations of the predicted and measured frequency. Each column presents a normalized depiction of where the measured oscillation frequency falls between the extracted simulation results and the schematic simulation results. Percentages are used depict the relationship of the measured frequency to these simulations. Based on experiences of others, theoretically, the measured frequency should never exceed 100% of the schematic simulated frequency since the schematic does not have the parasitic loading capacitance that will be experienced in the actual die. Ideally, the measurement frequency should be at 0% which would indicate that the oscillator is functioning at the same frequency as the extracted

simulation. Three different comparisons are provided. Figure 4.12.a shows a comparison of the body biased (BT) devices and the source to body (SB) devices.

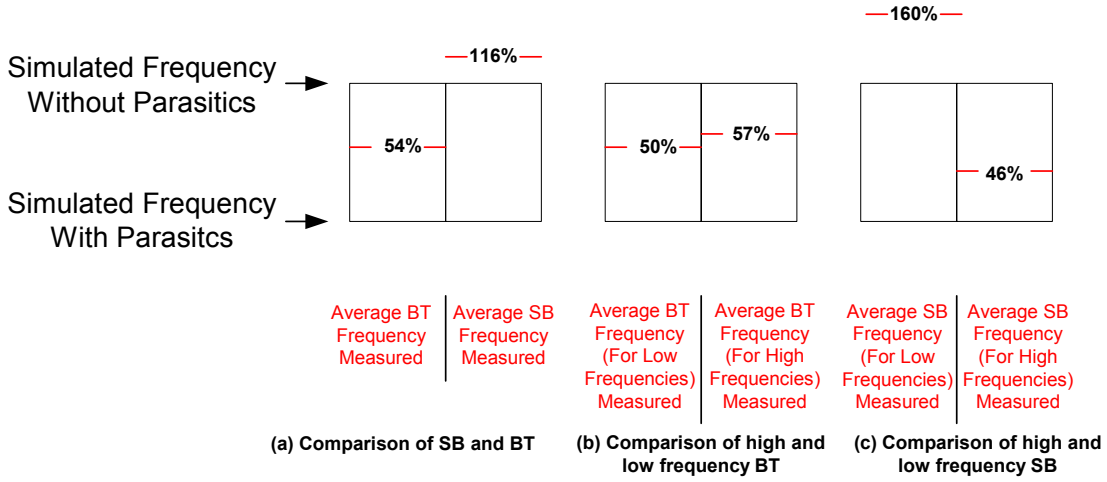


Figure 4.12 Accuracy of Simulations Compared to Measurements

Figure 4.12.b shows the comparison between the low frequency oscillators and the high frequency oscillators that use the body biased (BT) devices. Figure 4.12.c shows the comparison between the low and high frequency oscillators that use the source to body (SB) devices. The goal of this analysis is to give the reader some sense of how close the actual fabricated frequency of the circuit will compare to the simulations. Examination of Figure 4.12.a would lead you to think that the SB devices in general are not as close to the simulations as the BT devices, but that is not a correct assumption. Figure 4.12.b shows that the SB frequency simulations are greatly off for the lower frequency oscillators (less than 400MHz), but when using the SB devices for oscillators that are operating near the 500MHz range, the accuracy of the simulation greatly improves. The results of oscillators using the BT devices (Figure 4.12.b) reveal that the measured frequency will likely be about halfway between the two simulated values regardless of high or low frequency operation.

These measurements run counterintuitive to what is usually experienced in oscillator design and fabrication. In order to try to determine the factors involved in generating these results, both the library model files and the extracted netlist were examined in great detail, and some possible explanations were revealed.

Some investigation into the extracted layout, revealed several possible sauces of error. The cause of these errors could lie in the algorithm that is used to extract the various devices and parasitic capacitances. For example, in the layouts using the SB devices, there is no extraction of the parasitic capacitance between the gate and the source or drain. It seemed, as if the algorithm relies on the model to provide these capacitances. In some cases this would be sufficient, but there are some instances like when the metal layer connected to the gate is in close proximity to the metal layer of the source of the device, that a significant capacitance could exist but would not be modeled with the current extraction rules. In the BT devices however, the capacitance between the gate source, drain and body extracted in the layout and appear as parasitic capacitance in the netlist. This means that whatever device capacitance that is included in the model will be calculated in parallel to this parasitic capacitance from the layout.

These facts in themselves don't explain the discrepancies observed in the frequencies of the oscillators. What this does indicate is there is some variable that is not correctly accounted for in the device model. In the cases where the loading capacitance in simulation is solely determined by the device model, there is a large variance in the results. An example of this is the fact that the accuracy of the SB simulations are highly dependent on frequency, indicating in the higher order models of device capacitance there are some errors. In the oscillators using circuits that are not so dependent on the use of the models to determine loading capacitance (namely the BT devices) There is a rather consistent accuracy with the models.

4.4.5 Implications of the Frequency Results

These results don't directly solve, or provide the tools to solve the problem of a frequency mismatch between the simulated and the measured oscillator behavior. What these results do provide, is a method for insuring that the target frequency of the VCO will be met when the circuit is fabricated. Figure 4.13 shows how this information could insure that the actual performance would be close to the predicted value. By knowing, for example, that the actual oscillation frequency is halfway between the schematic and extracted

simulation values, the designer could be relatively confident that the useful tuning range of the VCO would cover the required frequencies.

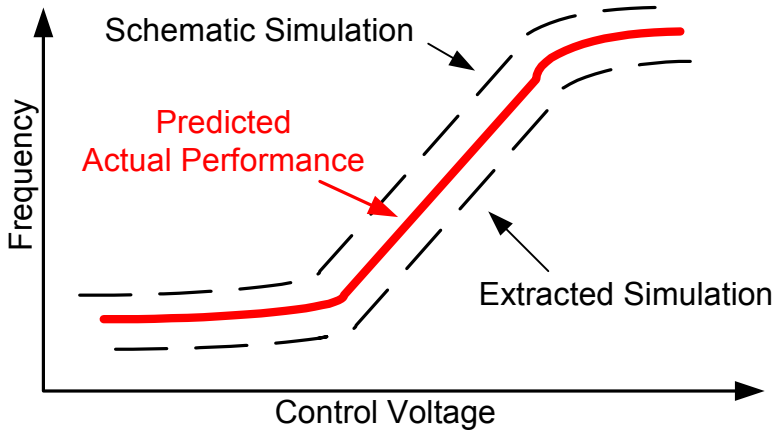


Figure 4.13 Use of Measurements in Achieving Accuracy in Future Fabrications

4.5 Oscillator Timing Jitter

The timing jitter of each of the oscillators in **Error! Reference source not found.** was also measured. Timing jitter (explained more thoroughly in Chapter 5) is the timing uncertainty of a clock signal after some time τ. This work focused on the characterization of the different layout techniques in terms of their affect on an oscillator's timing jitter. This characterization tried to answer several questions. First, if there is any major difference between the performance of the body biased devices (BT) and the source to body tied devices (SB). Secondly, what is the penalty paid verses the benefit gained from using small width body biased devices? And lastly, will intentional asymmetrical oscillator structures suffer from an increased amount of jitter? To answer these questions the 13 oscillators were characterized for their timing jitter performance.

4.5.1 Oscillator Timing Jitter Testing

The Tektronix 11801 Oscilloscope is equipped with a jitter measurement system that computes the RMS jitter over a specified number of cycles, perfectly suited for measuring jitter of these oscillators. Figure 4.14 provides a graphic of the measurement system. Besides showing the measurement data, the software allows the user to specify a

window where each time a rising edge passes through the window, the point where it intersects the window is added to a histogram which appears below the rising edge.

The procedure for generating these curves and obtaining this data proved to be very troublesome and a source of much error in the results. To begin with, the amount of force applied to the probe tip, and the angle of the probe tip to the die had an incredible impact on the jitter performance. Adjustment of the probe tip with the micromanipulator could easily cause the results to be much better or worse. This could be caused by the mechanics of the probe tip itself, that enable it to perform better when the tip is bent in a certain direction. This variance in could also be caused by the quality of the contact between the probe tip and the probe pad. The consistency of the metal layer on the probe pad is very similar to the frosting on a pastry. When the probe tip moves across the surface of the pad, the metal layer is scraped away. After many sessions of probing, it takes considerable more effort to find a good spot on the pad where this signal is of a high quality.

Another source of error in the measurements is the effects of the EM fields and the vibrations that are caused by a human presence in the vicinity of the oscillator under test. Figure 4.14 displays an example of this

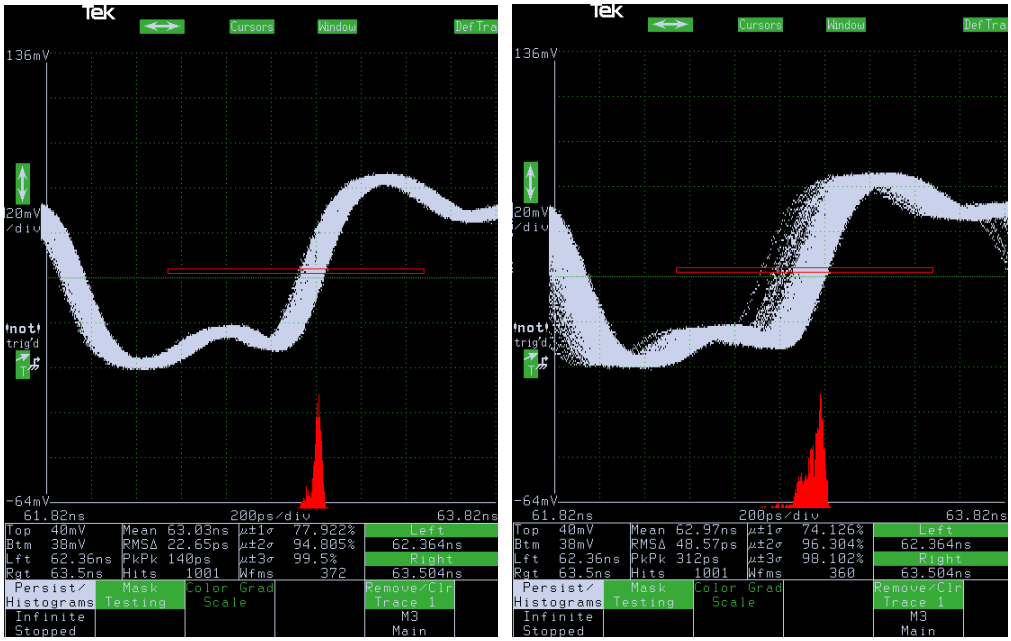


Figure 4.14 Two Jitter Measurements From the Same Oscillator

Figure 4.14 shows two jitter measurements on the same oscillator. In Figure 4.14.a the signal is clean with a jitter of 22ps. In Figure 4.14.b the signal contains twice as much jitter 44ps, which was caused simply by me moving my chair next to the test setup. In order to get consistent results it was very important to keep the disturbances around the testing area to a minimum. In some cases when none of the three measurements were similar, additional measurements would be made until a general trend was noticed.

In order to make sure that the results obtained were somewhat reliable, each measurement was taken at least three times. Also, the measurements were done "blindly" in that, it was not known ahead of time what the jitter should be.

4.5.2 Oscillator Timing Jitter Results

The results of the jitter tests are shown in **Error! Reference source not found.**

Table 4.5 Jitter Measurements of the Ring Oscillators

Oscillator	Measured Frequency (MHz)	Timing Jitter (seconds)			Phase Uncertainty (radians)			Average Phase Uncertainty
		Jitter 1	Jitter 2	Jitter 3	1	2	3	
Ring9fb	350	35.82	24.16	23.64	8.327E-02	5.438E-03	3.589E-03	3.077E-02
Ring10sb	460.83	31.19			9.031E-02			9.031E-02
Ring13bt	322.47	27.78	34.36	33.65	5.629E-02	0.069610	0.0681796	2.365E-02
Ring9sb	367.65	51.58	34.65	36.5	1.191E-01	0.080041	0.084315	9.450E-02
Ring14sb	373.13	53.28	75.1	44	1.249E-01	0.17607	0.103157	1.347E-01
Ring15bt	336.7	7.58	10.38	8.06	1.604E-02	0.021959	0.0170513	1.835E-02
Ring11sb	515.46	72.48	134.2	113.7	2.347E-01	0.434641	0.368247	3.459E-01
Ring16bt	409.84	150.2	71.44	80.21	3.868E-01	0.183963	0.206546	2.587E-01
Ring17bt	497.51	39.1	56.5	42.42	1.222E-01	0.176617	0.132603	1.438E-01
Ring18bt	411.52	45.18	44.96	46.53	1.168E-01	0.116251	0.120311	1.178E-01
Ring12sb	515.46	65.46	97.62	90.36	2.120E-01	0.316167	0.291488	2.732E-01
Ring19bt	512.18	77.66	64.76	69.09	2.499E-01	0.208406	0.22234	2.269E-01

The columns of the table contain the various measurements from different stages of the testing procedure. The timing jitter was measured by the oscilloscope over a period of 1000 rising edges of the input waveform. The phase uncertainty is the preferred method of expressing jitter normalized to the frequency of the clock. Phase uncertainty expressed as 'phase jitter' can be obtained from the frequency of the clock signal and the RMS timing jitter through the following relation.

$$\sigma_{\Delta\phi} = 2\pi \frac{\phi_\tau}{T} = \omega_0 \phi_\tau$$

This is a useful way of expressing the jitter, in that it represents the error in the phase of the signal, which is much more useful in comparing the quality of signals at different frequencies. The oscillators in **Error! Reference source not found.** are grouped by similarity in oscillator function. For example, oscillators with the same number of stages and the same devices sizing are considered part of a group. **Error! Reference source not found.** organizes the phase jitter results by the type of devices oscillators that were tested.

Table 4.6 Jitter Results by Oscillator Group

Measurement	Result
Average Phase Jitter of Body Biased Devices	.1247 radians
Average Phase Jitter of Source-Body tied Devices	.1859 radians
Average Phase Jitter for 'asymmetrical' devices	.1814 radians
Average Phase Jitter for 'symmetrical' devices	.1540 radians
Average Phase Jitter for 'low noise' Body Biased Devices	.1883 radians
Average Phase Jitter for normal Body Biased Devices	.1854 radians

The results are mixed. It was expected that the source to body tied devices overall would experience less jitter then the body biased devices, and the opposite was observed. It was expected that the symmetrical devices would have less jitter than the asymmetrical devices which, given the process corners is what was observed. A 'low noise' oscillator configuration was also tested, but the results indicated that the oscillator was anything but low noise. Each case will be reviewed independently.

Body Biased vs. Source-Body Device Timing Jitter

The indication that the body biased devices have less timing jitter than the source tied devices is a interesting and beneficial find. In an effort to understand why this behavior occurs, unique insight into the SOI circuit design has been gained.

Analysis begins with an understanding of what could have caused this jitter. The answer appears to be related to the supply rail noise. Because of the large series inductance of the bond wires and packaging, significant ringing exists on the supply rails. The ringing (30mV to 40mV) in amplitude can effect the delay of the stages of the oscillator and hence cause jitter. The relationship between supply voltage ringing and stage delay can be seen in the equation for the 'on' resistance of the individual stage. Since the on

resistance influences the rate at which the RC circuit charges and discharges any change to R affects the delay. The equation for the on resistance is repeated below.

$$Ron = \frac{Vds}{gm \cdot Vds} = \frac{1}{gm} = \frac{1}{\beta(Vgs - Vtn)} = \frac{1}{\beta(Vdd - Vtn)}$$

The term Vdd assumes a constant supply voltage. With voltage ringing, this term would have the DC component as well as the AC component of the 'ringing'. This could be expressed below.

$$V_{\sup ply}(t) = Vdd + V_{ring}(t)$$

Substituted into the equation for on resistance

$$Ron = \frac{1}{\beta(V_{\sup ply}(t) - Vtn)} \alpha \frac{1}{(V_{\sup ply}(t) - Vtn)}$$

In the case of a constant body bias voltage the below relationship is true.

$$Ron \alpha \frac{1}{(V_{ring}(t))}$$

Which means that the 'on' resistance, and hence the stage delay varies proportionately to the magnitude of the AC voltage ringing.

If the body of the device is held constant, the above relationship is no longer true. Remember that the threshold voltage of a device contains the term vsb which is the voltage difference between the source and body which can be substituted into the 'on' resistance equation.

$$R_{on} \alpha \frac{1}{Vdd - \left(Vto + \gamma\left(\sqrt{2\phi_f + Vsb} - \sqrt{2\phi_f}\right)\right)}$$

Substituting $V_{ring}(t)$ for Vsb and eliminating the constant terms yields

$$R_{on} \alpha \frac{1}{V_{ring}(t) - \gamma\sqrt{V_{ring}(t)}}$$

Which means that effect of the ringing voltage is reduced because of the constant body voltage. Although an area penalty of about 20% is paid for the use of body biased devices, the measurement data indicates a performance enhancement of about 20dB.

Symmetrical vs. Asymmetrical Device Timing Jitter

This test was engineered to examine the effects of 'asymmetrical' device design on the timing jitter. According to the analysis presented in Chapter 5the greater the difference between the rise and fall times of the stages in the oscillator, the more sensitive that oscillator is to noise. In this particular test, however, the opposite was found to be true. The oscillators that were deliberately sized to have a PMOS gate width larger than what was needed for perfect symmetry (ring18bt, ring12sb, ring19bt) turned out to have a better average phase noise performance than the transistors that were perfectly sized (ring11sb, ring16bt, ring17bt). This is in agreement with the predictions.

Low-Noise and Normal Body Biased Devices

Chapter 5explains the concept of the input sensitivity function (ISF) which can be used to accurately predict the phase noise of an oscillator based on knowledge of the device geometry and noise parameters. Chapter 5 reviews recent research which links the phase noise spectrum of an SOI oscillator to the accumulation of charge in the body of the device. As explained in that appendix, a larger the gate area the more noise that is likely to accumulate unless the body is tied to the source of the device via a low resistive contact. The body bias device presents an opportunity to explore the effects of the device geometry on the device noise induced phase jitter. A SOI device with a wide gate should allow more charge to accumulate than a device with a smaller gate, hence making the device with the large gate more noisy and cause the oscillator using that gate to have more timing jitter.

This idea was tested with the concept of a 'low noise' oscillator using body biased devices. Figure 4.15 shows the layout of the 'low noise' stage compared to the layout of a 'normal' stage. The effective device size of each stage is identical, however , the layout of the 'low noise' stage uses four smaller transistors instead of two larger ones. The result is that the smaller devices have the body contacts closer to the body, so it will be easier for the charge to exit the body. The price paid for this reduced noise, is larger real estate (to

accommodate the extra body ties and metal) and a larger parasitic capacitance caused by the 'extra' polysilicon needed to create the body contact.

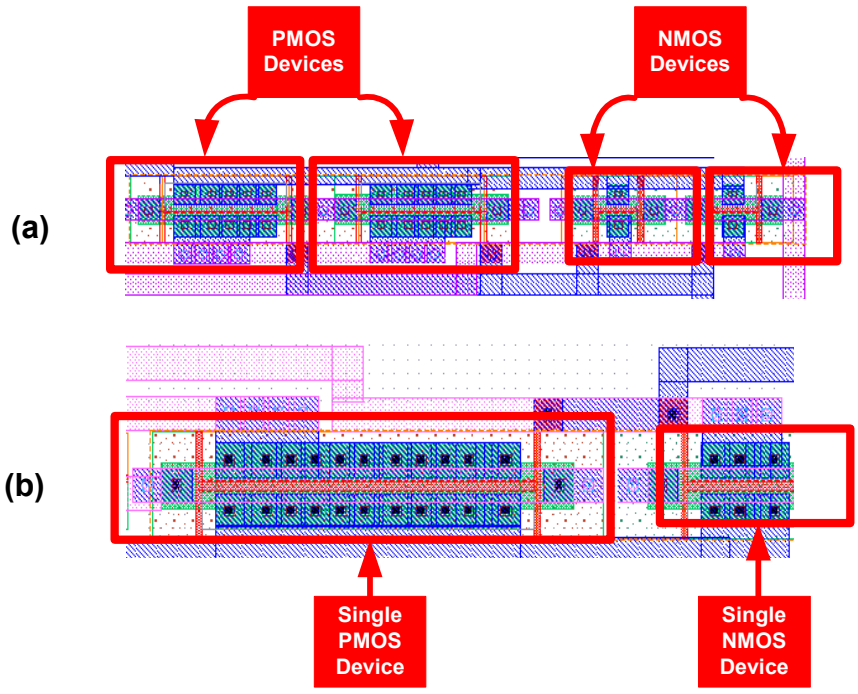


Figure 4.15 Layout of Low-Noise and Normal Inverter Stages

The results did not agree with this hypothesis. According to the measurements the normal body biased devices experienced a phase jitter of .1854 radians, while the 'low noise' devices experienced a phase jitter of .1883 radians, which is not a significant improvement.

An examination of the extracted layout, shows that the load capacitance is greater by approximately 20% for the 'low noise devices'. The actual operating frequency of the 'low noise' oscillator is nearly 20% less than the target operating frequency, however the normal oscillator is only about 5% less than the target operating frequency. This is a stiff penalty to pay in the operation and power consumption of the device, making this an unattractive solution.

4.5.3 SOI Oscillator Conclusions

The oscillators that were characterized in this chip would not be of any use in an RF receiver circuit. As oscillators, they cannot be tuned to accommodate multiple channels,

or meet the requirements of a modern communication system. What these circuits do establish, however, is a baseline of performance to establish what is possible with the Honeywell MOI5 process technology. Several design theories were tested, which were either proven or disproved by the evidence gathered.

The oscillators fabricated in this run were single stage ring oscillators, which generally have poorer performance than the other differential architectures. This is useful, however, in establishing a baseline of what can be expected if an SOI ring oscillator were to be implemented as a component of the digital architecture. The costs to the SNR of a system relying on a sampling clock can be calculated once the jitter is known [28]. Where σ_τ is the RMS timing jitter and $V_0\omega_0\cos(\omega_0 t)$ is the received signal. The standard error in the sampled signal will be

$$\sigma_v = V_0\omega_0\cos(\omega_0 t)\sigma_\tau$$

The SNR introduced by the timing jitter is:

$$SNR = \frac{V_0^2/2}{\sigma_{v,average}^2} = \frac{V_0^2/2}{V_0^2\omega_0^2\sigma_\tau^2/2} = \frac{1}{\omega_0^2\sigma_\tau^2}$$

This SNR figure is useful to the communications system designer who could budget that figure into the system as a whole. The information given by this characterization allows the decision to be made before the design process if a digital ring oscillator is the right solution for the problem.

Chapter 5
Jitter Reduction in SOI Ring Oscillators

5.1 Introduction

Silicon on insulator circuit innovation usually falls into two groups: the design of circuits that are unaffected by the noise and behavior of the SOI device in an effort to enjoy the benefits of SOI without the disadvantages or the use of the floating body for some digital circuit enhancement. Very little innovation has occurred that would exploit the floating body terminal of the device for analog applications. One goal of this work was to contribute to the field of circuit design some new and innovative design. An opportunity to accomplish this is provided by the access that the circuit designer has to the body of the device.

Recent publications have explored the relationship between 'symmetry' and the phase noise or jitter performance of an oscillator. A 'symmetrical' oscillator has a balanced rise and fall time. Symmetry is important in that, it offers the least exposure to the noise of the circuit that can cause fluctuations in the oscillating frequency which is called phase noise. From the viewpoint of this research, the circuit characteristics that determine oscillating frequency (delay, or input impedance) were dependent on circuit characteristics that cannot be changed after fabrication. Process corners, cause the threshold voltage of a device to different than what was observed in the simulation. In the face of a changing threshold value it is nearly impossible for the circuit designer to design a symmetrical oscillator that will retain its symmetry after fabrication.

SOI gives the circuit designer a unique opportunity in this respect. By adjustment of the DC voltage of the body of the device, the threshold voltage of a device can be changed and hence, the device's behavior can be altered post-fabrication. Specifically, this ability offers advantages in the area of frequency synthesis where circuit performance is limited by process variation. This chapter outlines the theory behind this hypothesis and the experimental data that validates it.

5.2 Experiment

In order to verify the hypothesis concerning body bias and the effects of symmetry in general it was necessary to fabricate a variety of oscillators that could be used to gauge the effects of device sizing, and the impact that body bias has on the delay of the stages and as a result the noise of the oscillator.

Devices of both the source-body and independent body bias were used for this experiment. The source-tied devices mainly were there to test the theories of symmetry and the effects that device sizing has on the noise. In addition to the source-tied devices that were fabricated, six body biased oscillators were fabricated. A picture of the layout is shown in Figure 5.1. The top shows the shared power and ground pins that were used in the other oscillator designs fabricated on this chip.

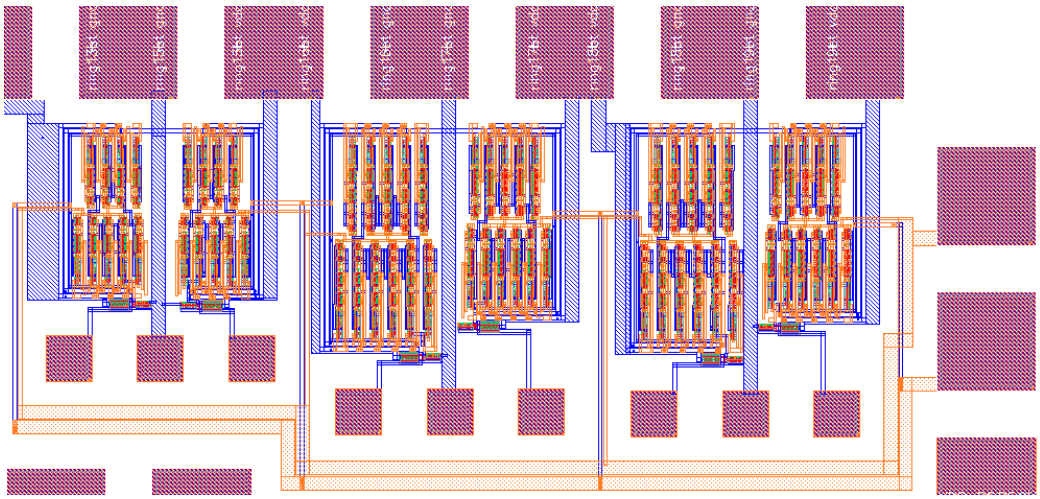


Figure 5.1 Body Biased Oscillator Layout

The body bias pins were also shared among all of the body biased devices in order to conserve pin space. There was some concern before fabrication, that the long wires connecting the body bias pins to the devices would allow noise to couple into the pins and therefore allow noise to be introduced into the device. This problem never materialized though, as all the oscillators performed well. The Tektronix 11801 sampling scope was again used to make the jitter measurements and no fewer than three measurements were taken for every bias point observed.

5.3 Results

The results of the oscillator testing can be seen in **Error! Reference source not found.** Data points were taken on either side of the 'zero bias' point for both the NMOS and the PMOS devices. The data in the table represents the jitter that was observed and the resulting signal to noise ratio that would be caused by a sampling circuit with that level of jitter.

Table 5.1 Results of the Body Bias Testing

Ring16bt						
zero bias	71.74		14.66974		14.66	
P = 3.6	76.53	78.81	14.10833	13.85334	14.66	-0.67917
P = 3.0	47.72	47.63	18.21095	18.22735	14.66	3.559153
N = 0.3	71.54	76.16	14.69398	14.15042	14.66	-0.2378
N = -0.3	63.21	60.79	15.76925	16.10832	14.66	1.278784
Ring17bt						
zero bias	56.5	42.42	15.05957	17.54913	16.30435	0
P = 3.5	126.9	80.41	8.031308	11.99434	16.30435	-6.29153
P = 3.0	70.46	50.41	13.14169	16.05021	16.30435	-1.7084
N = 0.3	72.64	72.8	12.87702	12.85791	16.30435	-3.43688
N = -0.3	48.62	40.81	16.36424	17.88521	16.30435	0.820375
Ring18bt						
zerobias	44.96	46.53	18.69248	18.39434	18.54341	0
P = 3.0	58	51	16.48045	17.5976	18.54341	-1.50439
N = 0.3	56	54	16.78525	17.10113	18.54341	-1.60022
N= -0.3	41	40.19	19.49333	19.66665	18.54341	1.036577
ring19bt						
zerobias	64.76	64	13.61012	13.71266	13.66139	0
P = 3.6	69	72	13.05927	12.68961	13.3347	-0.46026
P = 3.0	54	57	15.18838	14.71876	13.3347	1.618871
N = 0.3	66.45	67.8	13.38636	13.21166	13.3347	-0.03569
N = -0.3	53		15.35074		13.3347	2.016039

An experiment investigating the effect of symmetry on the oscillator timing jitter was conducted in Section 0. This experiment explored the effect of a slight unbalancing of an inverter. It was shown, that a .5u difference in the size of a PMOS transistor caused the fabricated N/P ratio to be 2.0 instead of 1.9. Ideally this would have been 1, but the

process corners that occurred during the fabrication of the chip caused the ratio to be much more skewed than originally thought. The calculated difference in jitter between the 'asymmetrical' and 'symmetrical' oscillators is about 10%, which resulted in a 1dB difference in SNR.

This measurement offers good insight into the effects that process variation has on the jitter of a ring oscillator. The fact that the difference between the two circuits is exactly 10% and the SNR is close to 1dB means that for every 10% difference in the matching of the devices, results in a 1dB penalty in the SNR. The data above shows that body bias can be used to gain more than 6dB in the SNR. which could go a long way towards reclaiming the performance penalty that in the past has been intrinsic to bad process corners.

5.4 Conclusions

The research presented in this section will lay the basis for future research in this area. The idea the circuit designers have some way to compensate for the parameter variation in processes that don't have a tight control of the oxide thickness, will surely enhance existing SOI designs, and will make possible future architectures that may move towards greater manufacturability of frequency synthesizers.

Future work in this area will incorporate advanced control systems, that will be capable of adapting to changes in process or environment and still maintain a high level of performance.

Chapter 6 Conclusion

This thesis poses the question: " Is Silicon on Insulator a suitable technology for frequency synthesis?". The answer to this question based on the experiments and results presented here is yes.

A phase locked loop was designed, fabricated and measured proving that frequency up-conversion and the circuits needed to support this operation can operate effectively in SOI. The process of creating the PLL was quite instructive and offered a glimpse into the pit-falls and problems that await frequency synthesis circuit designers. The results and the experience gained during this process will be invaluable in the next steps of designing a high performance synthesizer that must operate on the surface of the planet Mars.

The characterization of the SOI devices and circuits also lays the ground work for future development in this area. The results presented in this work, allow the circuit designer some method of gauging the reliability of the simulations in predicting the behavior of the circuit after fabrication. The characterization of the oscillators yielded valuable information about the ability of SOI circuits to reject power supply noise, and hence add to the value of this technology.

Finally, a novel technique for reducing timing jitter in SOI ring oscillators was introduced. This novel scheme, has not been explored before and may provide frequency synthesizer circuit designers with a new tool, to make frequency synthesis more precise and manufactuarable.

These three accomplishments should prove that SOI is a perfect match for an RF frequency synthesizer. Hopefully, this work will shed light on the subject and give SOI the boost it needs to become a preferred choice for the RF integrated circuit design industry.

Appendix A
Introduction to SOI

As the name "Silicon on Insulator" implies, SOI devices are field effect transistors (FETs) fabricated on a highly resistive substrate. Three processing options are available for establishing such a highly resistive substrate. This work utilized the Honeywell MOI5 fabrication process, which uses Unibond Smart Cut wafers produced by Soitec. The seven steps in the smart cut process are as follows:

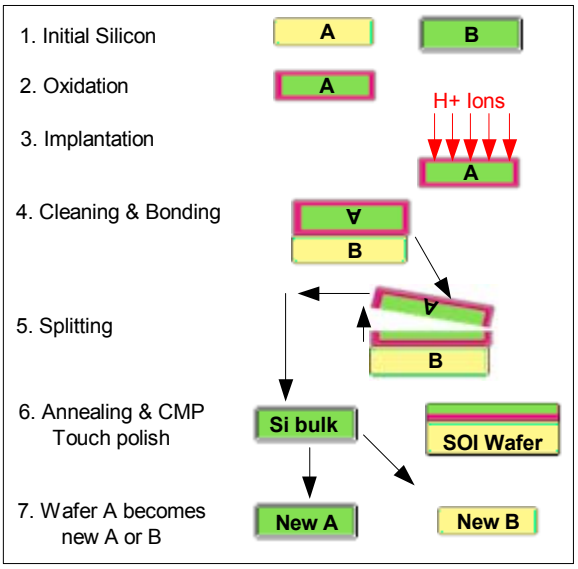


Figure A.1 Processing steps in Soitec Unibond process [29]

Although the methods to create an SOI wafer differ, the end result is a thin substrate bonded to a highly resistive oxidized layer. All FETs are fabricated on the same thin substrate where shallow trench isolation (STI) is used to pattern and isolate the active areas.

Devices are fabricated in either a fully depleted SOI (FDSOI) or partially depleted SOI (PDSOI) process. Full depletion means that the depletion region covers the whole transistor body. The depletion charges is constant and cannot extend according to gate bias and the inversion charge, leading to enhanced drain current []. Figure A.2 below depicts a side view of a fully depleted device.

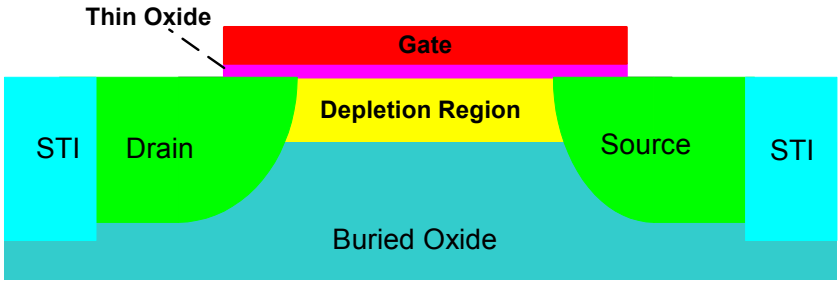


Figure A.2 Side view of a fully depleted SOI device

Although FDSOI is a rapidly advancing area of research, device threshold voltage is extremely dependent on the width of the thin oxide[30], [31], [32]. This poses a major obstacle to the manufacturability of FDSOI devices. Partially depleted devices, in contrast, operate in fundamentally the same way as standard bulk CMOS devices [33]. This makes PDSOI a more viable option in terms of manufacturability and utility in circuit design [32]. Figure A.3 below shows the cross section of a partially depleted SOI device.

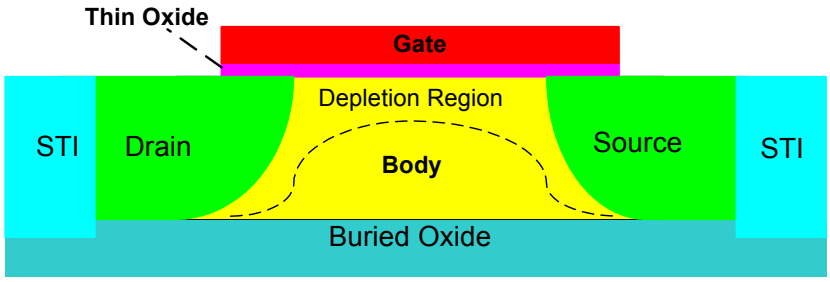


Figure A.3 Cross Section of a partially depleted SOI device

The partially depleted substrate introduces many variables into the circuit design process. These issues will be explored in greater depth in the following sections. Since PDSOI is the exclusive focus of this work, all references to SOI circuit designs are refer to PDSOI devices.

A.1 Devices studied in this work

The size, geometry and layout technique used in SOI circuit design varies based on the design rules of the fabrication process. Before discussing the modeling of the SOI devices, it is helpful to understand the design options available to the circuit designer as the constraints and models can vary drastically among the layout techniques. The term "layout technique" is interpreted as the type of device used by the circuit designer. In the Honeywell MOI5 process, There are three layout techniques available to the circuit designer: body tied to source (SB), body floating (FB), and independent body biased devices (BT). The structure of each device is fundamentally similar to that in figure X above, but each with slight variation.

The layout associated with independently biasing the body voltage is seen in Figure A.4 below. The fact that the gate is layout resembles an "H" has prompted many to refer to this as an "H-gate" device. It is also possible to fabricate this biased body device in the shape of a "T" (called a T-gate device).

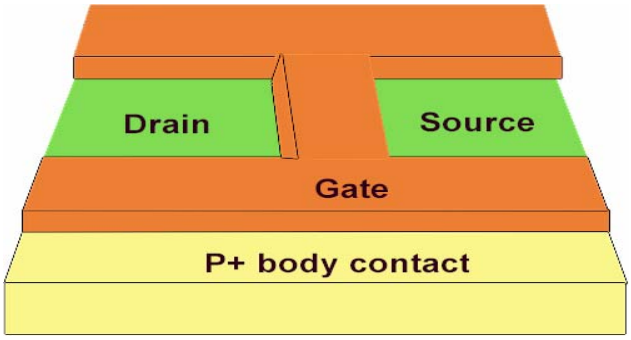


Figure A.4 An independently body biased NMOS device

The body contact provides the means for the designer to influence the body voltage of the device. Control of the body voltage can be a valuable tool for circuit designers. It can provide a means of lowering the threshold voltage of the device by altering the *Vsb* term of the threshold voltage equation. It can also serve as an input terminal, useful to those interested in bulk driven circuit designs. There are several things to be concerned with

while using H-gate or T-gate circuits. Most importantly is the effects of the extra gate capacitance associated with the large amount of polysilicon that is used to isolate the active regions from the body contacts. This increase in capacitance is not currently modeled in the Honeywell process and it is up to the circuit designer to evaluate the magnitude and cost of the increased capacitance to the operation of the circuit. Another disadvantage apparent in Figure A.4 above is the increased area consumption. The H-gate (or T-gate) device requires much more area not only for the layout of the device itself, but also in the care that must be taken in routing the metal for the contacts. SB circuits in general consume about 30% less area. Other problems can be attributed to the lack of study and modeling of this layout style. For example, larger gate widths may allow charge accumulation in the body and therefore an increase in noise. The body contact itself can be a source of noise, as the contact can be a source of noise injection into the device [33]. A careful understanding of the effects of design decisions is required in order to produce an optimal design.

Source to body tied device is the default device of the SOI digital circuit designer.
A view of the device structure is shown in Figure A.5 below.

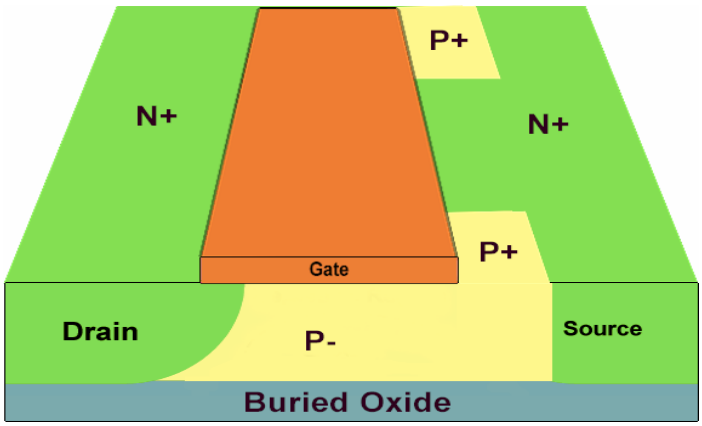


Figure A.5 A Source to Body Tied NMOS device

While SB devices do not have the wide range of applications as the body biased configuration, SB devices offer some of their own advantages. These devices do not suffer from the same problems of charge accumulation in the body of the device [34] as the other device layout techniques. In the Honeywell process, rules governing the

spacing of the body ties are specified so fewer decisions are left to the circuit designer, and performance can be expected to be more or less constant for different device geometries. The devices are also useful in digital logic where devices are connected in series as shown in Figure A.6 below. In such configuration, the *Vsb* term is constant for each device, as opposed to bulk CMOS which means that less care can be taken by the designer to determine the critical path [35].

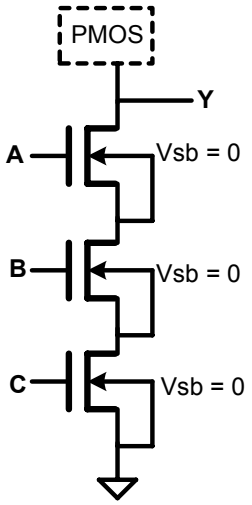


Figure A.6 Transistor stack exploiting SB-tied NMOS devices

The third layout technique available with the Honeywell process is the floating body configuration pictured in Figure A.7 below. The floating body device is one of the first devices to be studied, and as a result much analysis has been done to understand and model the operation of this device [36], [37], [33], [38].

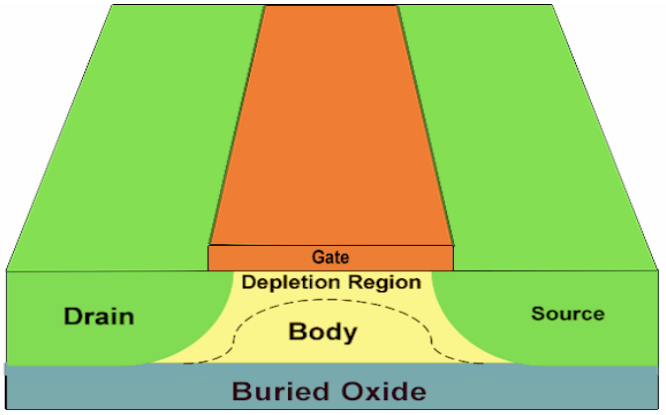


Figure A.7 A floating body transistor

Modeling and operation of this device will be covered in greater depth in the following sections. This is the only of the three devices where in depth modeling of the operation has been done and any attempt to model either the SB or BT devices is an extrapolation of the results gained from the study of the FB device. The layout of this device in the Honeywell design kit is cumbersome and unrefined, and therefore there are no simulated or experimental results from its use. The floating body device remains a study of research as it is usually the "flagship" device of researchers who aggressively seek to shrink the gate length in experimental SOI processes.

A.2 Modeling of SOI device operation

Although the operation of SOI devices are fundamentally the same as bulk MOSFETs, there are several effects of device operation on an insulating substrate that must be studied. Seemingly simple circuits can operate can behave differently in SOI and in order to correctly diagnose and remedy a design, it is necessary for the designer to have an understanding of the dynamics of SOI operation. Figure A.8 below shows a circuit representation of an SOI device [39].

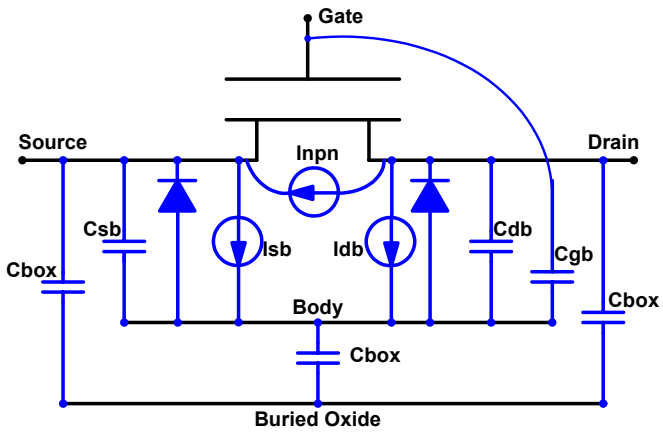


Figure A.8 Circuit representation of SOI device

A.2.1 Parasitic Currents of the SOI device

Isb, Isb is the flow of current from the active region to the body of the device. This happens via two means: junction leakage and impact ionization.

$$Isb, Idb = (I_{\text{Im}\,pact\ Iionizatio\,n} + I_{Junction\ \ Leackage})$$

Junction leakage across the drain-body or source-body N/P diode slowly introduces additional charge into the body. There is only a very slight dependence on the applied voltage, however the reverse-biased current is directly proportional to the area of the diode junction [7]. Over extended intervals, the amount of charge transferred can be substantial [32].

Impact Ionization is the significant contributor of charge to the body of the device, and appears frequently as the root cause of the anomalies prevalent in SOI circuit design. Impact ionization has been studied in great depth and as a result only a brief overview will be presented here although more in depth coverage can be found elsewhere [32],[27].

The electric field in the channel of an active device increases logarithmically as a function of distance from the device and as an example is pictured in Figure A.9below.

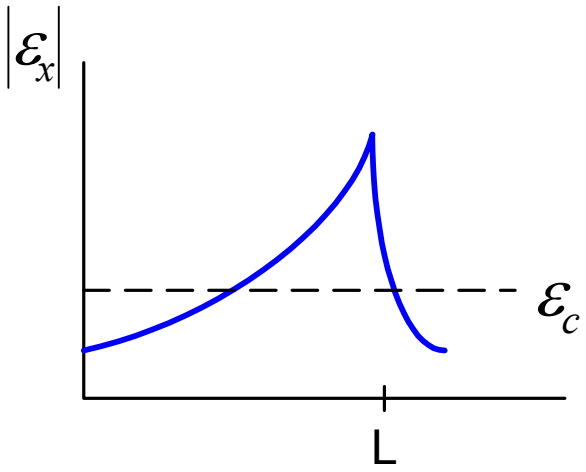


Figure A.9 Magnitude of electric field as a function of channel length.

Although the field increases logarithmically, the speed of the electrons saturates when the magnitude of the field reaches $\mathcal{E}_c$. While the speed saturates, the random kinetic energy of the electrons continues to increase. Depending on the statistics of scattering, a small fraction of the overall carrier population accumulates a significant amount of energy, and these are called "hot carriers. The higher the field, the higher the proportion of hot carriers in the overall population. Some of them acquire enough energy to create impact ionization of silicon lattice atoms, whereby new electrons and holes are created; this effect is also referred to as weak avalanche,. The new electrons join the stream of channel electrons and move on toward the drain. The result of this, is a current Idb which can be modeled as

$$|I_{DB}| = |I_{DS}| K_i (V_{DS} - V'_{DS}) \exp\left(-\frac{V_i}{V_{DS} - V'_{DS}}\right)$$

Where K_i and V_i are parameters that must be fitted empirically to data [32].

Inpn is the current originating from the parasitic bipolar transistor that can be created by the drain-body-source configuration. As far as parasitic bipolar transistors in general are concerned, SOI designers must primarily deal with this one "channel" bipolar device. This is a far cry from the latch-up concerns that plague standard bulk processes with their many opportunities for parasitic bipolar transistors to from between the active devices

and the substrate [24]. The catch, however, is that the SOI parasitic bipolar device is highly dependent on the operation and layout of the device, where as bulk parasitic devices crop up more as an anomaly or rare situation. The key factor, as was alluded to earlier was the combination of impact ionization current and the isolated body of the device. In either the FB or BT layout of the SOI device, the body will be at best resistively coupled to ground. As impact ionization occurs and the holes accumulate in the body of the device (or exit slowly via the resistive body tie) the voltage potential of body will rise and as a result the parasitic bipolar current will increase.

A.2.2 Junction Diodes and Parasitic Capacitance

The characteristics of the junction diode formed by the transition from a body or substrate to a counter-doped source or drain implanted region are central to the behavior of the MOSFET, and have even more significance in the PD-SOI MOSFET. Specifically, diode action , junction capacitance and junction leakage strongly influence SOI 'performance. At the heart of the SOI MOSFET are two junction diodes formed by the counter doped source and drain regions, identical in concept to those in the bulk device. The body-source diode is often weakly forward biased; and the drain-body diode is usually reverse-biased. The capacitance between the source or drain and the body of the MOSFET is a strong function of their difference in potential. When the potential on the drain of an NFET is high and the body is low, the space-charge region surrounding the junction grows, as a larger counter doped P area in the body must be "raided" for its electronics in order to satisfy charge neutrality across the junction. This space charge region acts as the dialectic in the capacitor formed by the drain and body. The dielectric, incidentally is silicon, with dielectric constant Er of approximately 23. At height potentials the two plates are far apart and the capacitance is low, conversely at low differences in potential between drain or source and body the resulting space-charge region is thin, and the capacitance is high.

The parasitic currents Idb and Isb take into account the effects of this junction leakage. Junction leakage refers to the low current passing through a diode even though it may be strongly reverse-biased. Junction leakage arises from three major mechanisms:

Electron/Hole recombination in the space charge region, Defects/impurities in the space charge region which disrupt the diode doping gradient from n-type to p-type. High - energy carriers which exceed the diode's electronic barrier height. Junction leakage is sustained in bulk technologies by the supply rail connection to the substrate or N-well on one terminal, and the source or drain node driven by the preceding circuitry on a second terminal. IN the PDSOI device's isolated floating body, junction leakage directly affect body potential and hence performance, of an extended period. Junction current also has an exponential dependence on voltage and temperature, as represented simplistically in the classic diode current equation,

$$I = I_0\left(e^{qV/KT} - 1\right)$$

Where I_0 is the diode's generation current with 0 volts across its junction, V is the potential across the function, k is Boltzman's constant, and T is temperature in degrees Kelvin.

A.3 SOI Noise and Nuances

Current research into SOI circuit design focuses on either exploiting the positive aspects of characteristics mentioned above and compensating for the negative effects. These papers again fall into one of two categories: analog and digital circuit design. The digital research tends to focus on the effects of SOI devices in on the logic state or performance (noise margins, gate delay etc) [40]. Analog research papers tend to examine the aspects of SOI devices in terms of noise or biasing constraints (noise figure, phase noise etc).

The combination of the parasitic sources (Isb and Idb) with the junction diodes and parasitic capacitances produces the time-varying behavior in the device [41]. The result is that the behavior of the device can be influenced by 1) The previous state of the transistor, 2) The position of the transistor in a circuit, 3) The slew rate of the input and the load capacitance, 4) Channel length and processing corner, 5) Operating supply voltage, 6) Junction temperature, 7) Operating frequency and specific switch factor. The root cause of these effects is the nature of the body contact combined with the effects of impact ionization. Figure A.10 below represents the forces at work . The impact

ionization and junction leakage currents, represented as I(t), provides a time-varying flow of charge into the body of the device. In a bulk CMOS process Figure A.10.a the excess charge flows through the low-resistivity substrate to ground, providing a device body that is held to DC ground (in the absence of substrate noise). In the SOI example in Figure A.10.b excess charge must exit the body through one of two means. 1) As the body slowly rises in potential via junction leakage or ionization charge accumulation, the source-body N/P diode and in some cases the drain-body N/P diode slowly become forward biased, and pass charge. The amount of charge levels off when a balance is achieved. This mechanism varies in its time to convergence, ranging in delay from tens to hundreds of microseconds [32]. 2) A rising gate or drain will capacitively couple the body of the FET higher also. AS the body rises at some fraction of the slew rate, the source-body N/P diode and in some cases the drain-body N/P diode will forward bias and quickly spill charge. This effectively creates a 'body-resistance' which allows the voltage at the body to fluctuate. Since the decay of this body voltage is not instantaneous the system can be classified as a time-variant system.

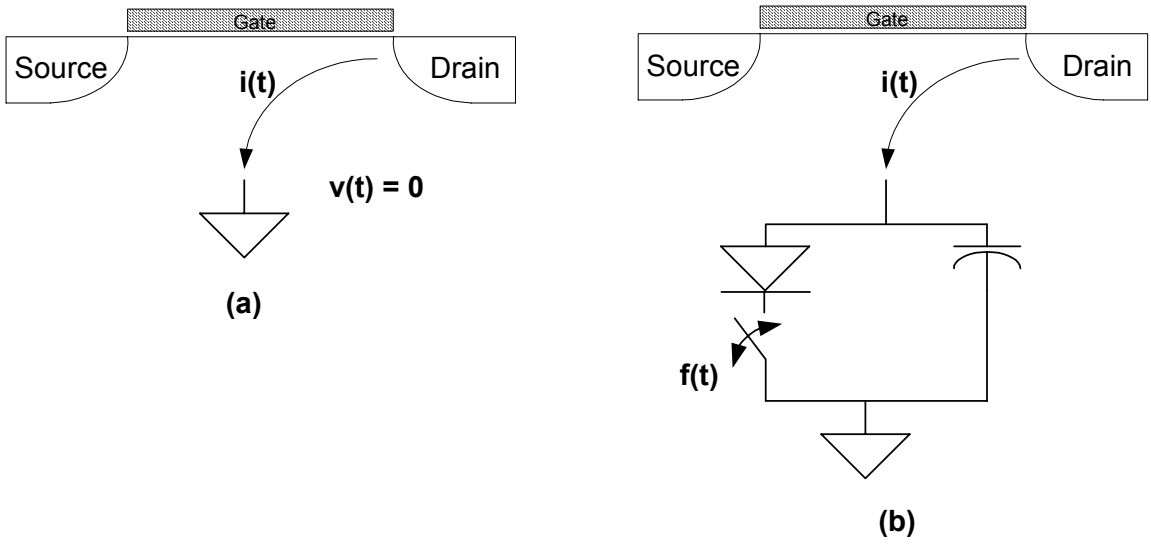


Figure A.10 Path of Body Discharge in Source Tied and Floating Body Devices

Instead of being referred to as a time-variant device, SOI devices are usually said to suffer from "data-dependency" or "history effect" meaning that the data that passed through the circuit at time $t < 0$ will affect the performance of the circuit at time t = 0. Figure A.11 below gives an example. When the output data is stable, at the beginning and

end of the pattern, the body voltage and therefore the device threshold remain at a steady state value. During the rapid switching period α the increased activity generates more body current which in turn raises the NMOS body voltage Figure A.11.b which results in a change in the device threshold value through the relation: $V_{th} = V_{th0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$. Figure A.11.c below graphically depicts this effect.

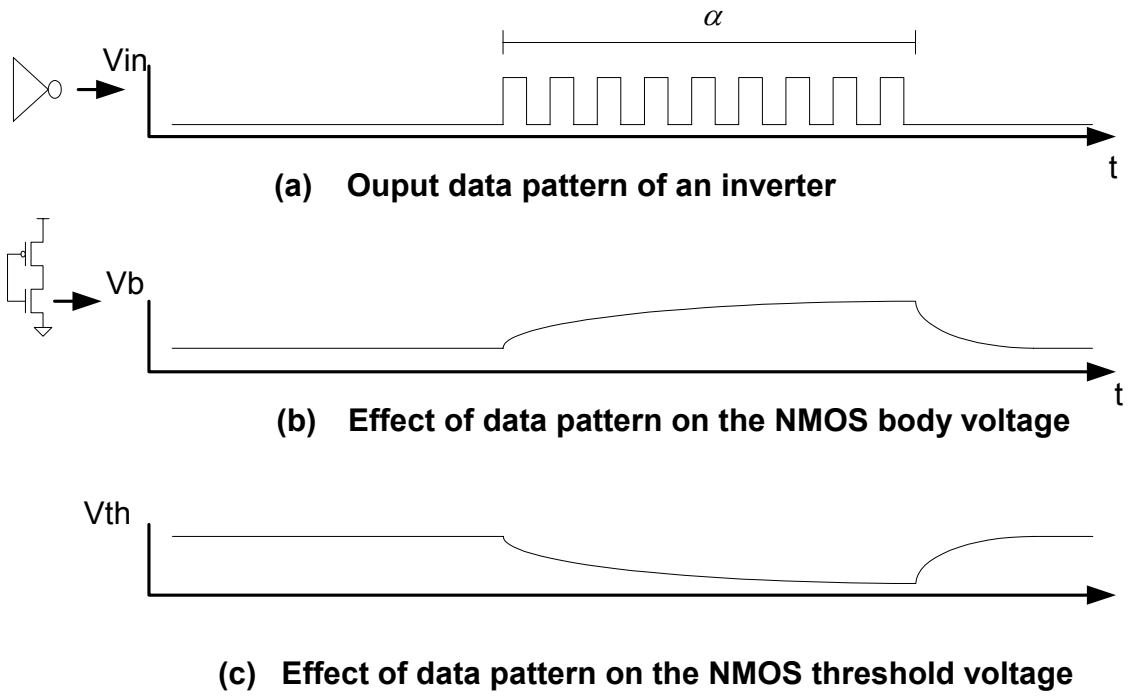


Figure A.11 Demonstration of Data Dependent Behavior of SOI

Appendix B
Individual Device Characterization Data

Table B.1 List of Devices Tested

Device	Device Type NMOS/PMOS	Gate Length (meters)	Gate Width (meters)	Layout Style BT/ SB/ FB
1	PMOS	600n	27.75u	BT
2	NMOS	600n	9.25u	BT
3	PMOS	600n	13.75u, 14u	BT
4	NMOS	600n	4.85u, 4.4u	BT
5	NMOS	900n	6u	BT
6	PMOS	900n	18u	BT
7	PMOS	900n	27u	BT
8	NMOS	900n	6u	BT
9	PMOS	900n	18.5u	BT
10	NMOS	900n	6u	BT
11	PMOS	900n	18.5u	BT
12	NMOS	600n	4.4u, 4.85u	BT
13	PMOS	900n	13.5u, 13.5u	BT
14	NMOS	600n	9.25u	BT
15	PMOS	950n	19u x 4 fingers	BT
16	PMOS	600n	27u	SB
17	NMOS	600n	9.25u	SB
18	PMOS	900n	18.5u	SB
19	NMOS	900n	6u	SB
20	PMOS	600n	27.75u	SB
21	NMOS	600n	9.25u	SB
22	PMOS	900n	18u	SB
23	NMOS	900n	6u	SB
24	NMOS	950n	6u x 5 fingers	SB

25	PMOS	500n	21u x 2 fingers	FB
26	NMOS	500n	6.75u x 2 fingers	

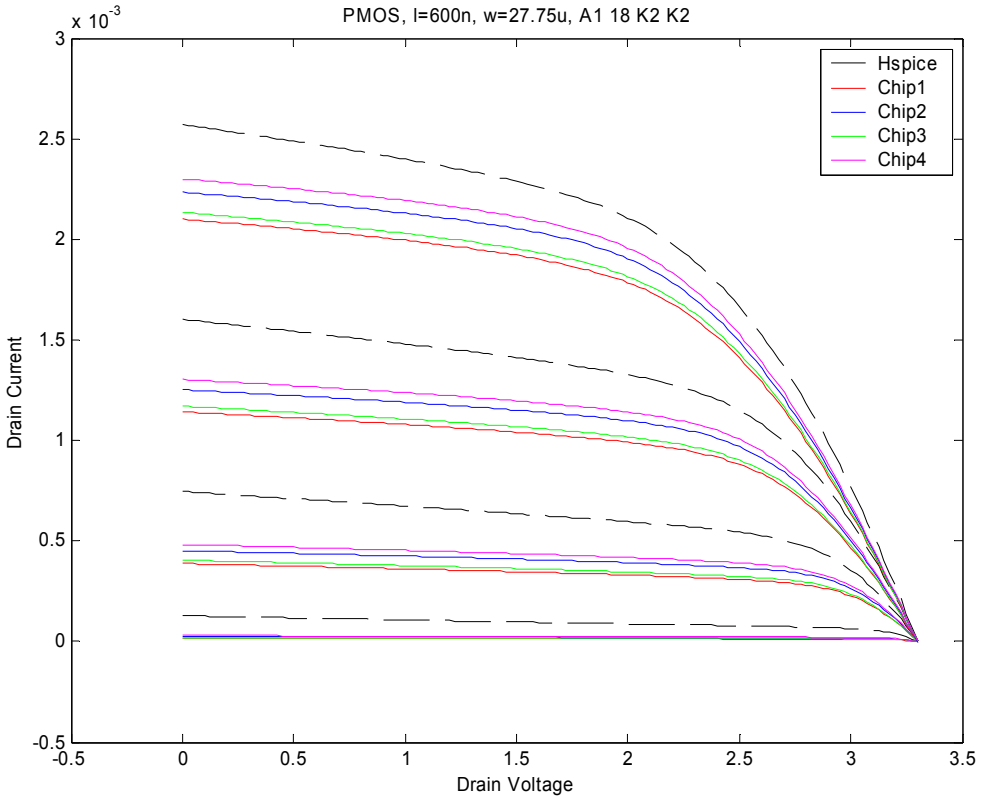


Figure B.1 PMOS BT, l = 600n, w = 27.75u

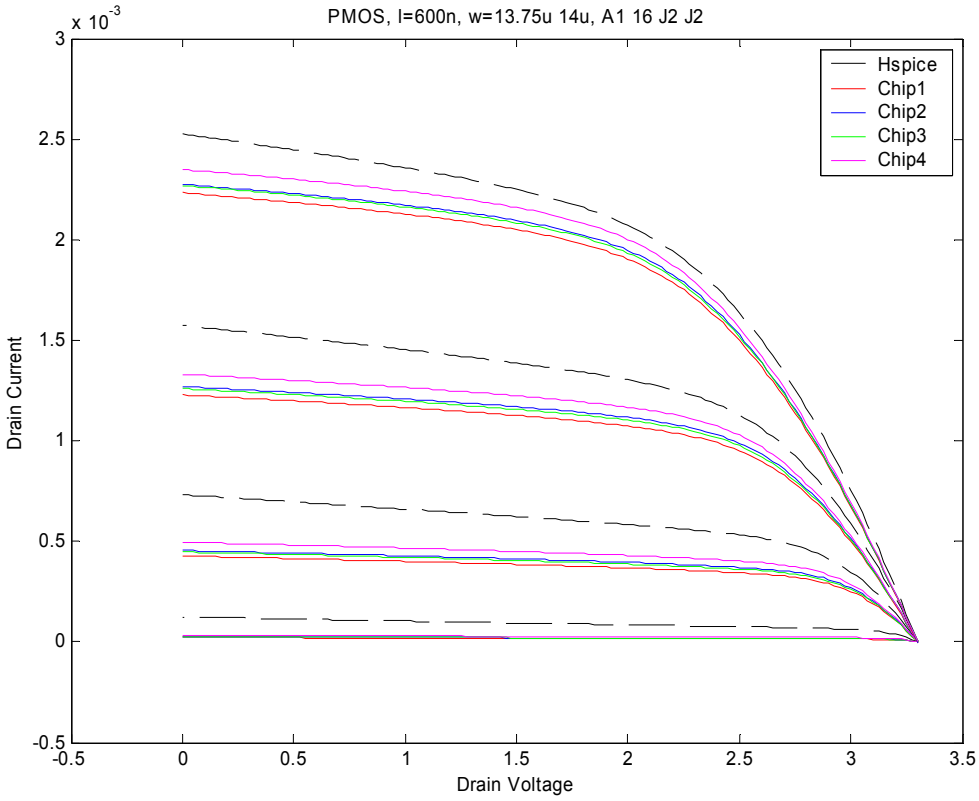


Figure B.2 PMOS, l = 600n, w = 13.75u, 14u

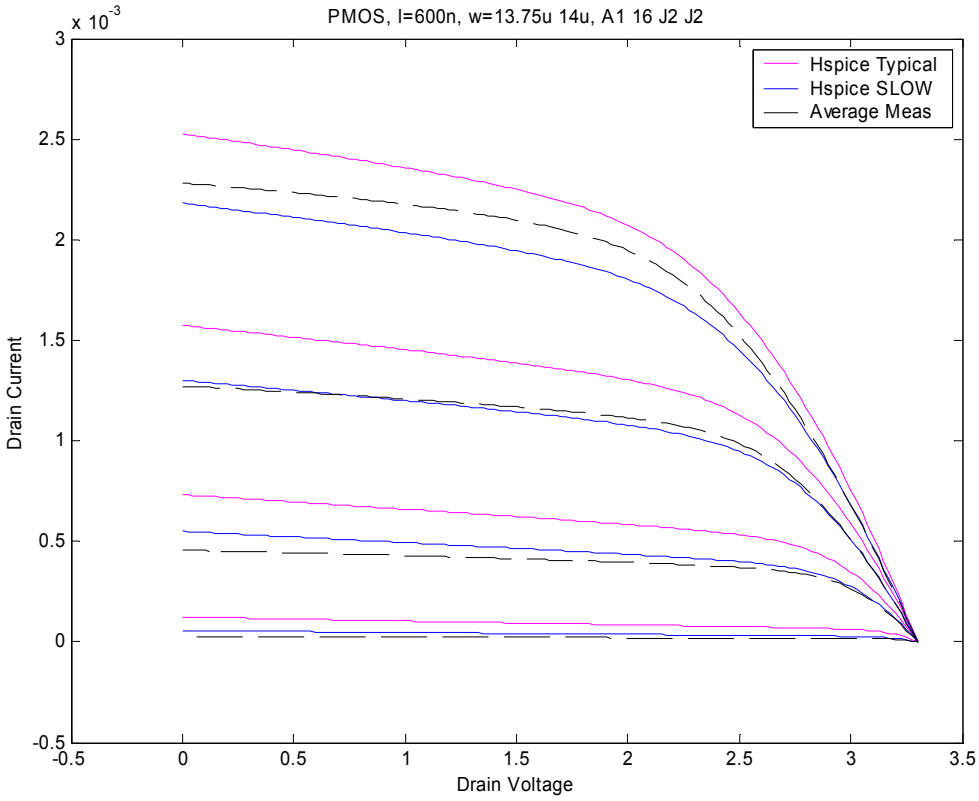


Figure B.3 PMOS, l = 600n, w = 13.75u, 14u

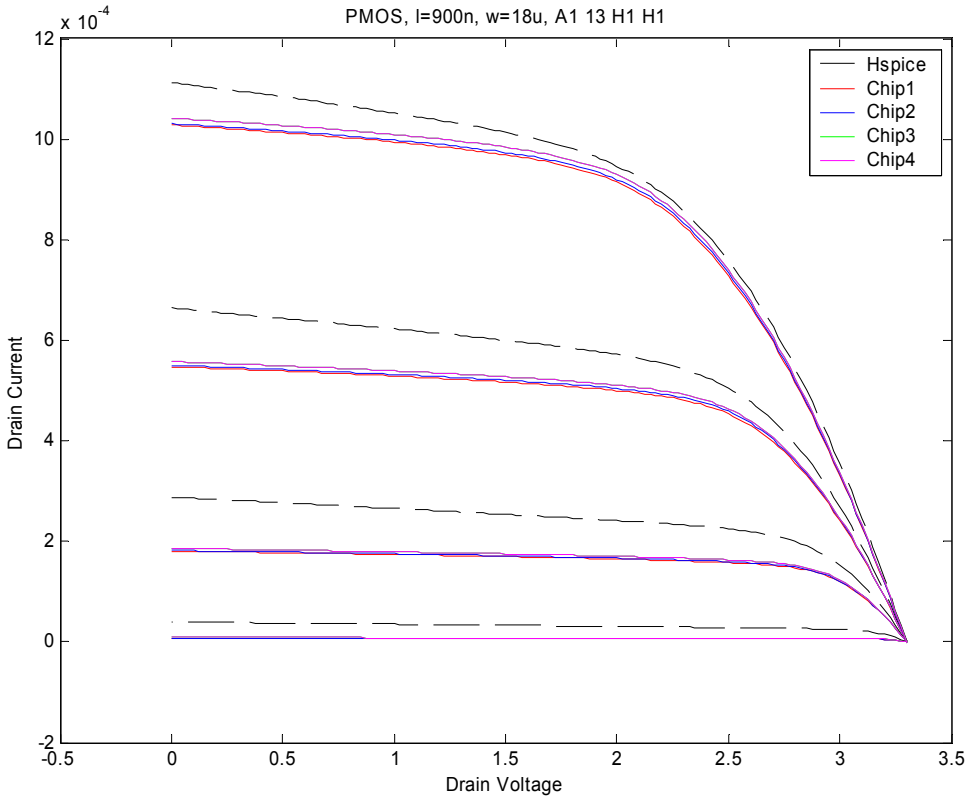


Figure B.4 PMOS, l = 900n, w = 18u

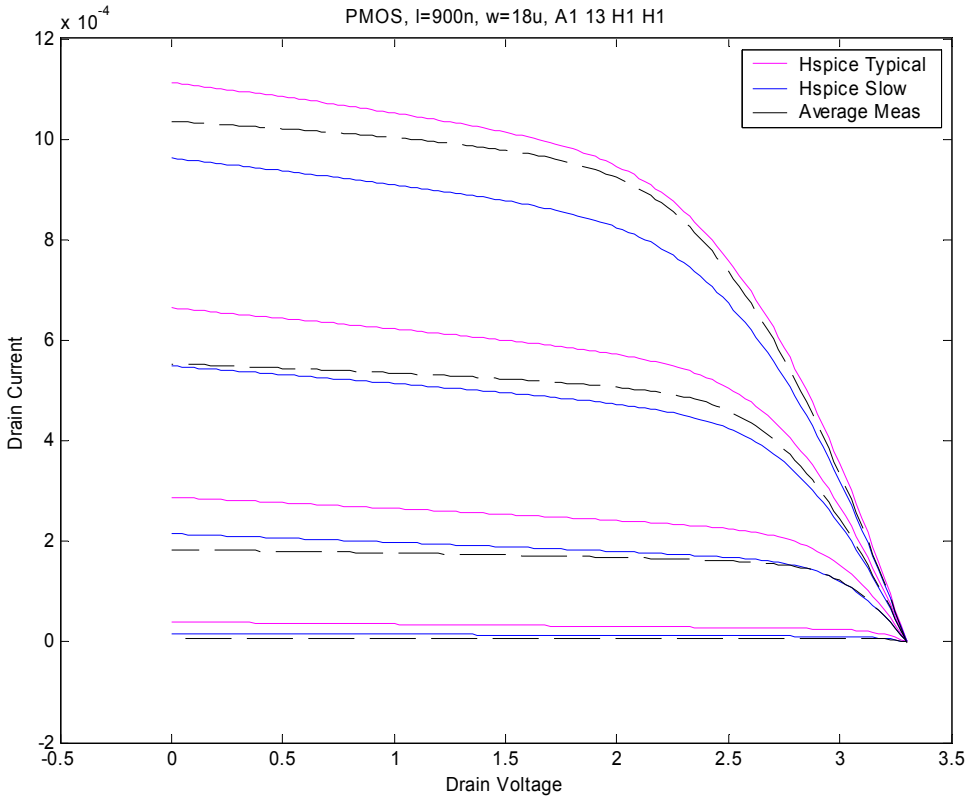


Figure B.5 PMOS, l = 900n, w = 18u

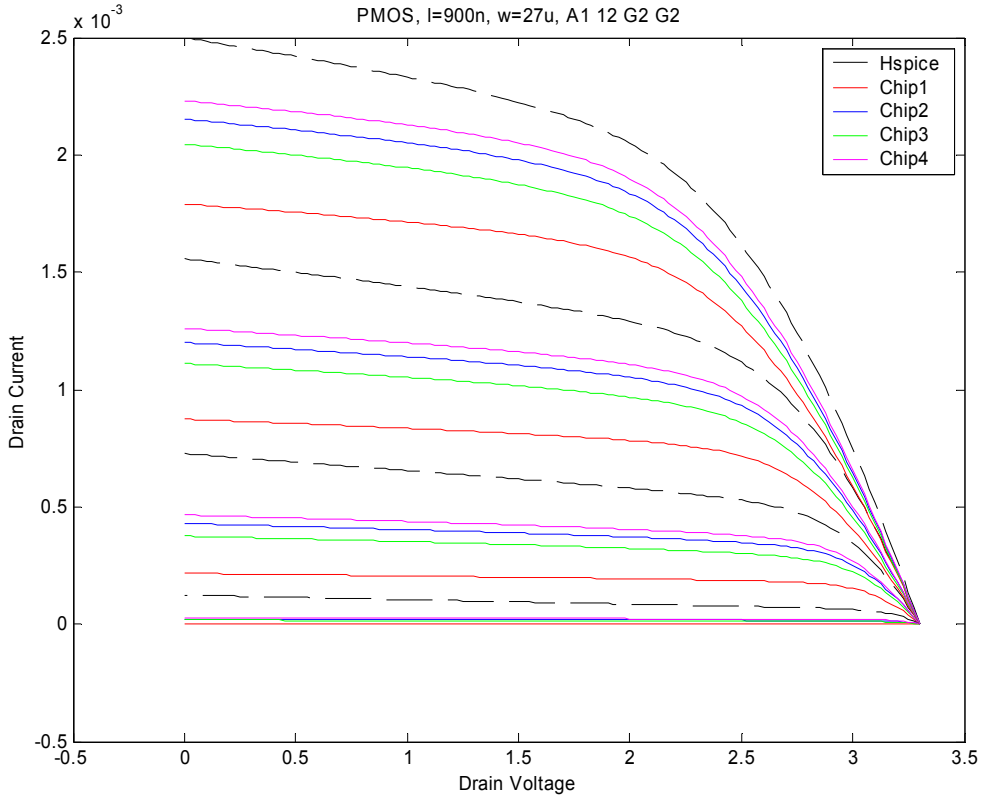


Figure B.6 PMOS, l = 900n, w = 27u

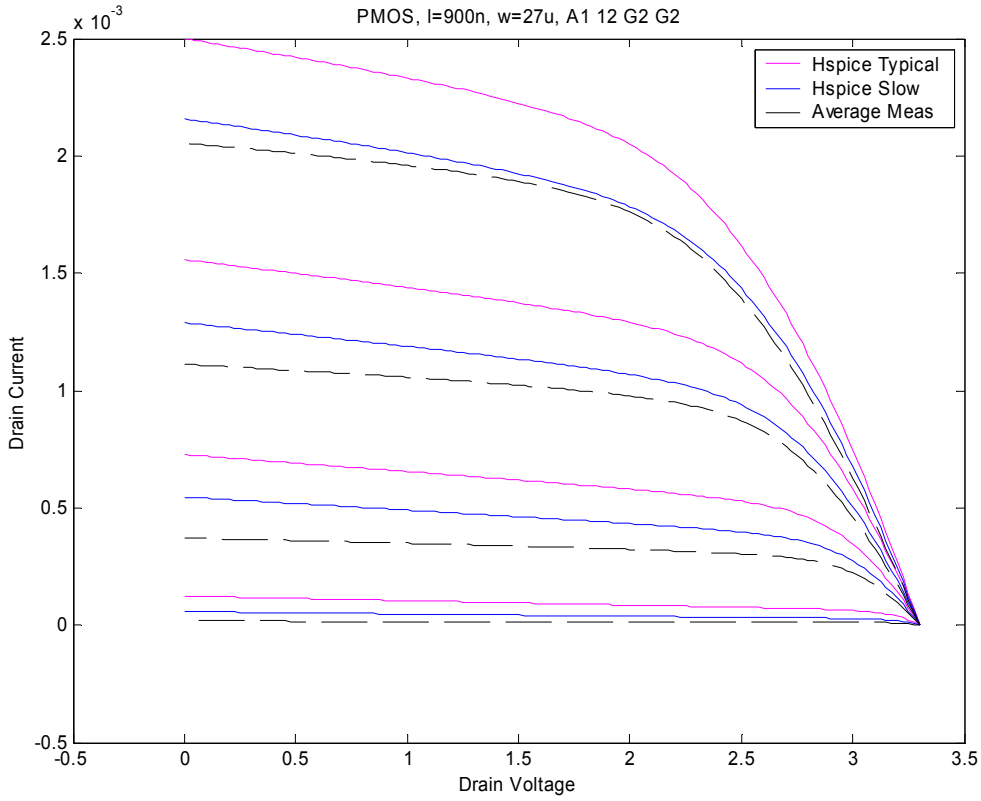


Figure B.7 PMOS, l = 900n, w = 27u

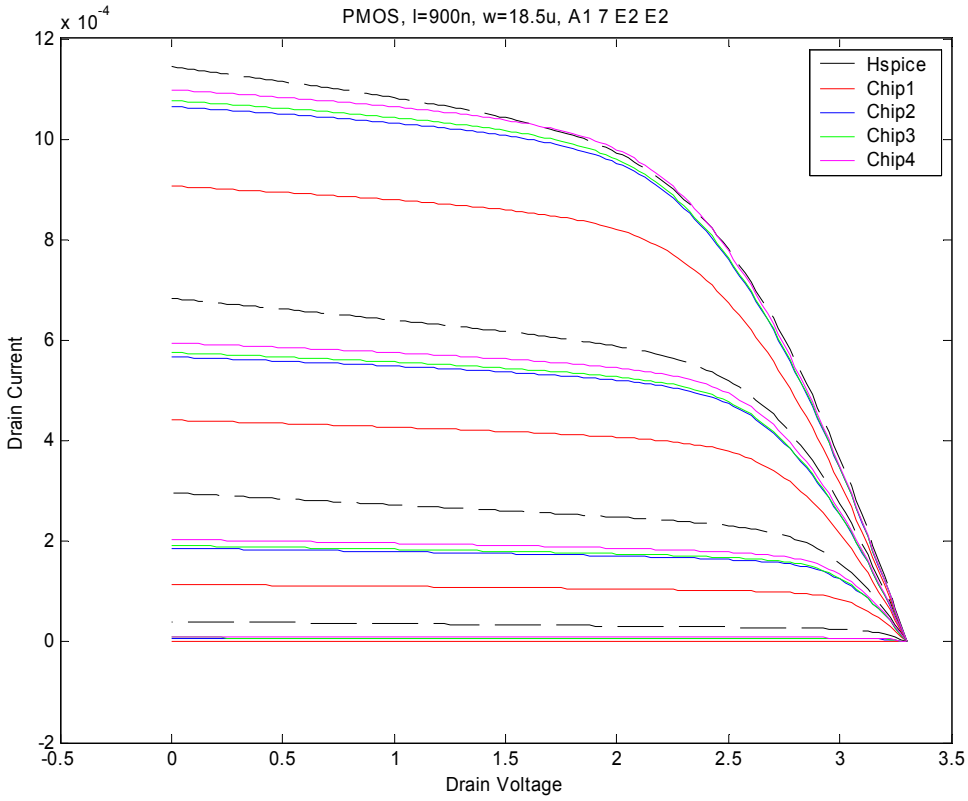


Figure B.8 PMOS, l = 900n, w = 18.5u

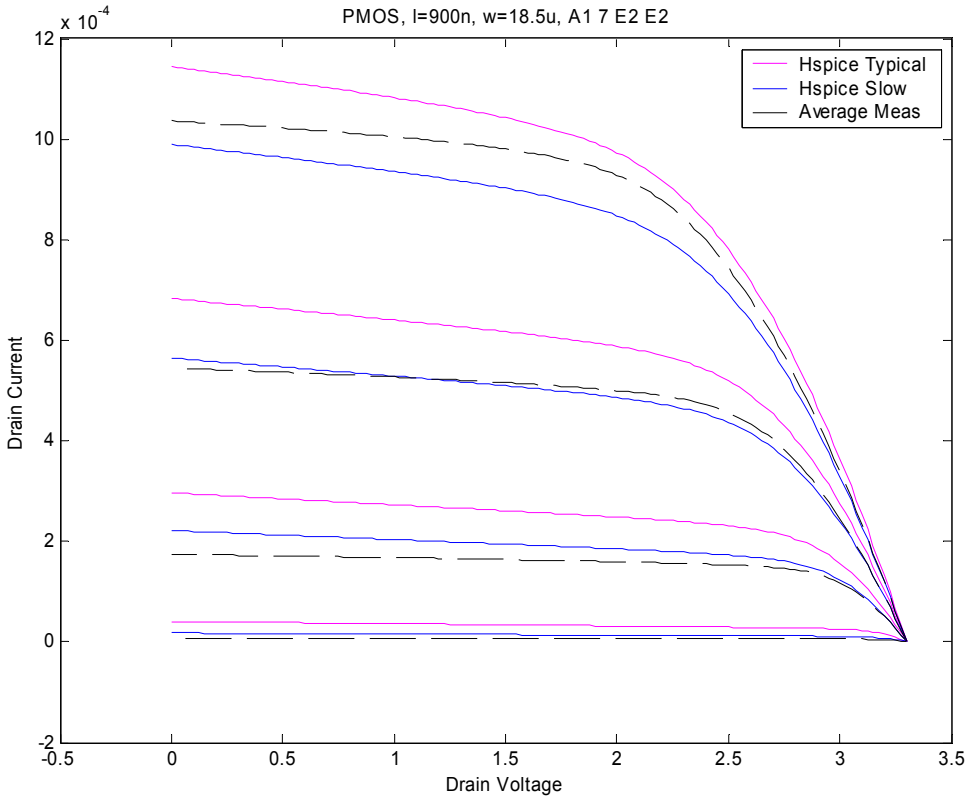


Figure B.9 PMOS, l = 900n, w = 18.5u

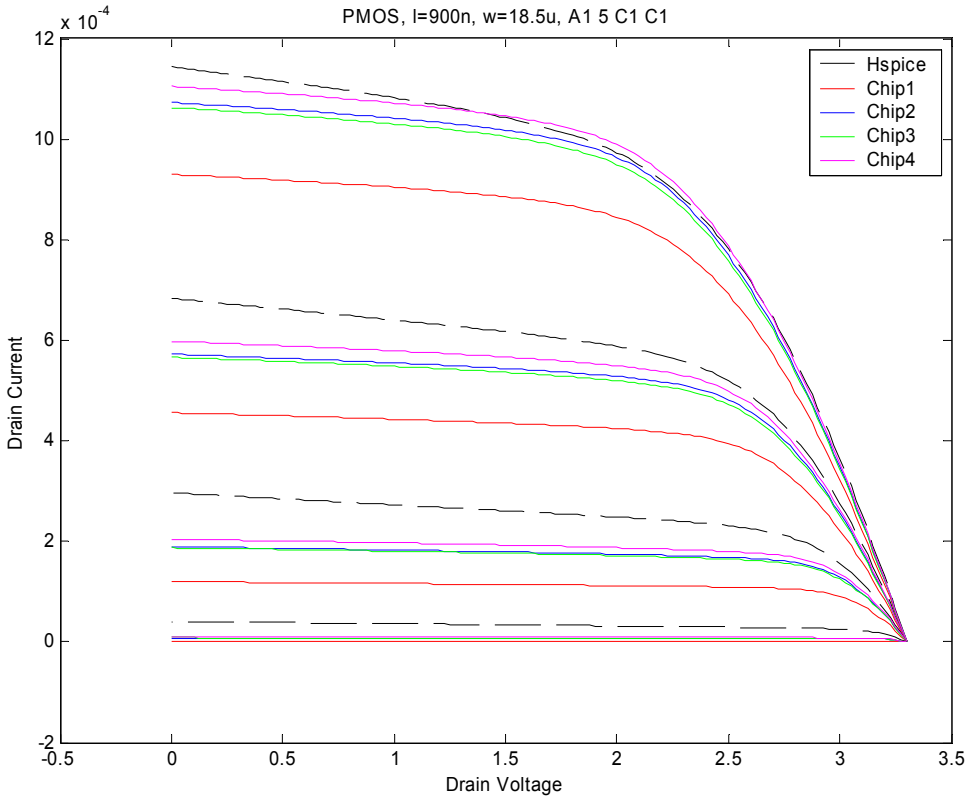


Figure B.10 PMOS, l = 900n, w = 18.5u

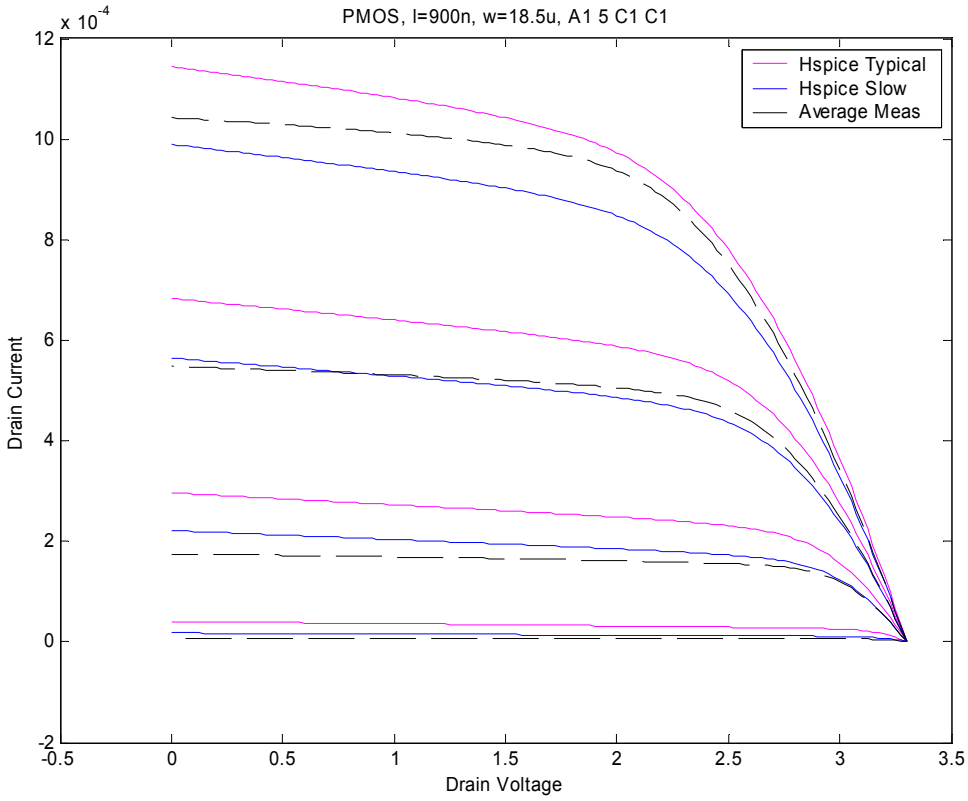


Figure B.11 PMOS, l = 900n, w = 18.5u

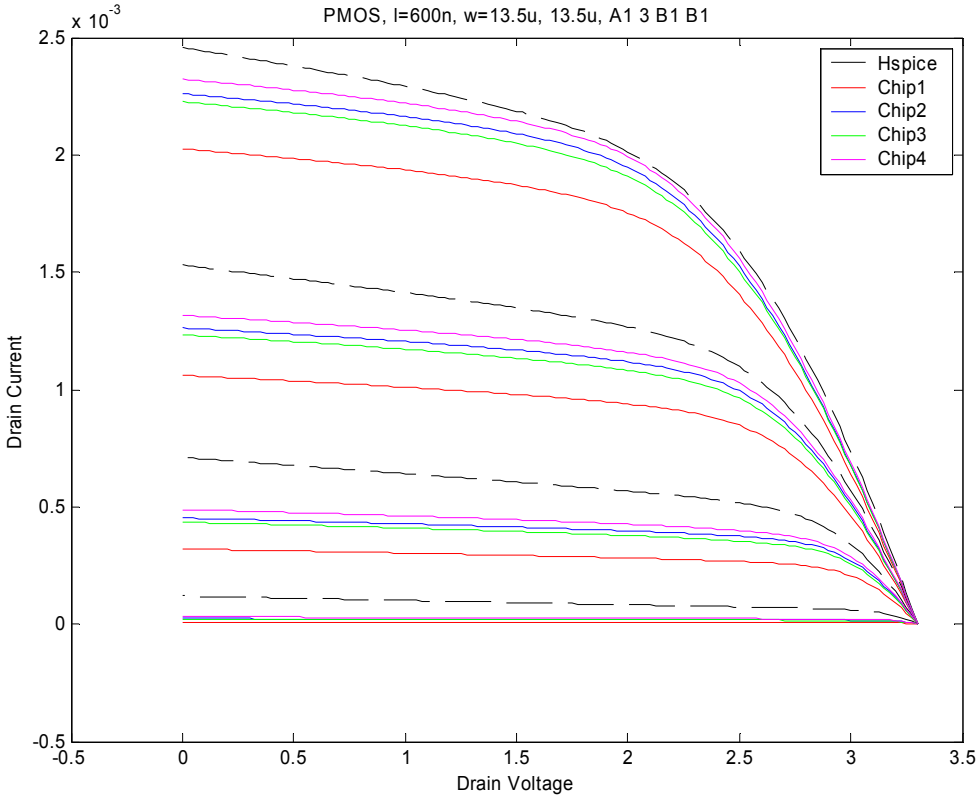


Figure B.12 PMOS, l = 600n, w = 13.5u, 13.5u

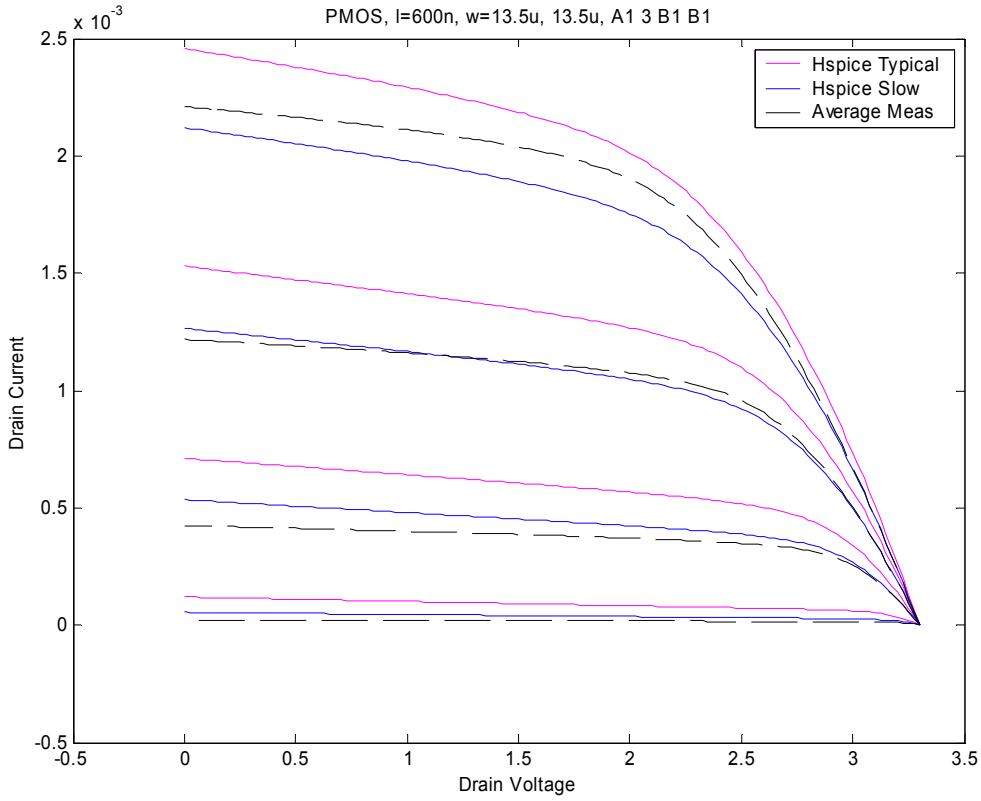


Figure B.13 PMOS, l = 600n, w = 13.5u, 13.5u

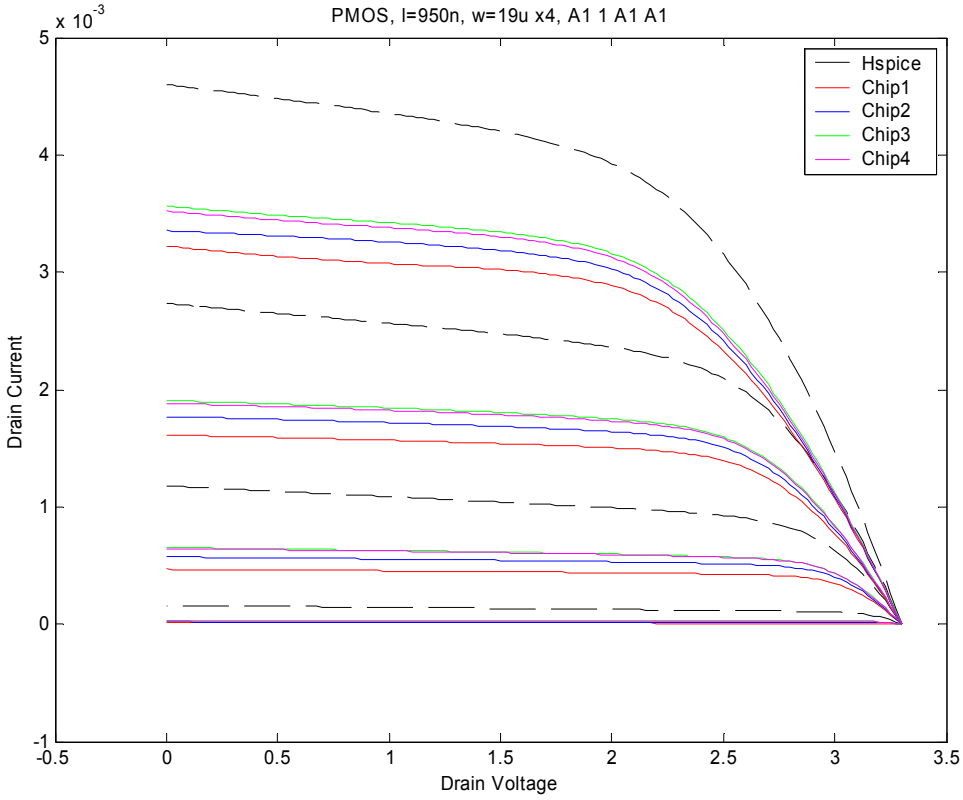


Figure B.14 PMOS, l = 950n, w = 19u x 4

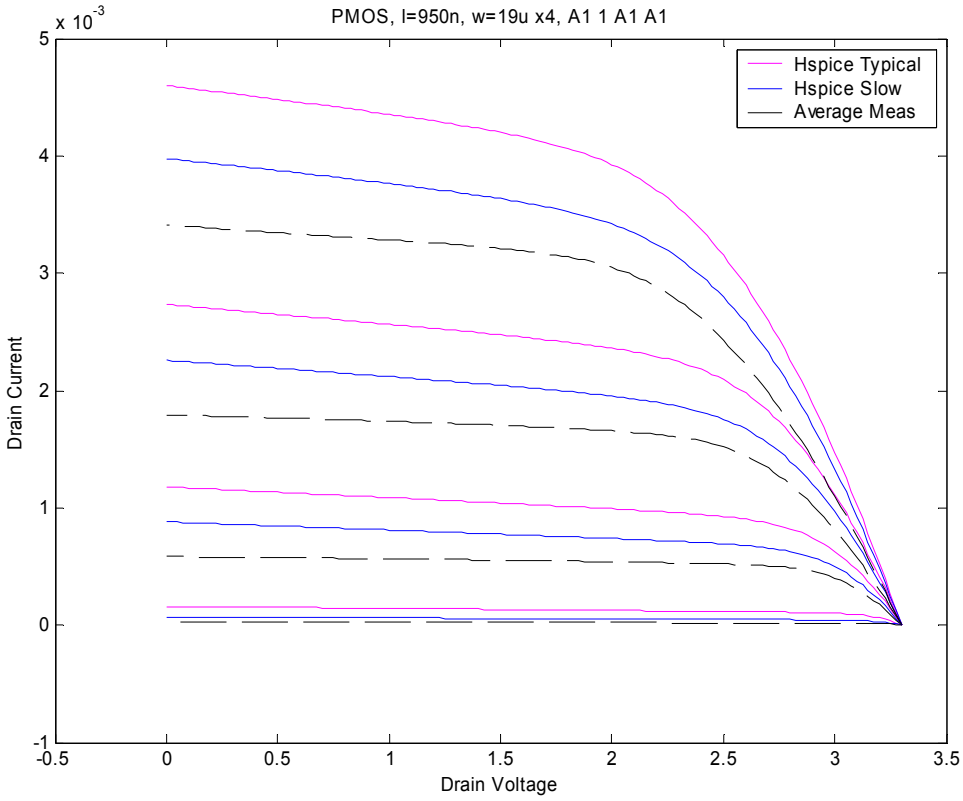


Figure B.15 PMOS, l = 950n, w = 19u x4

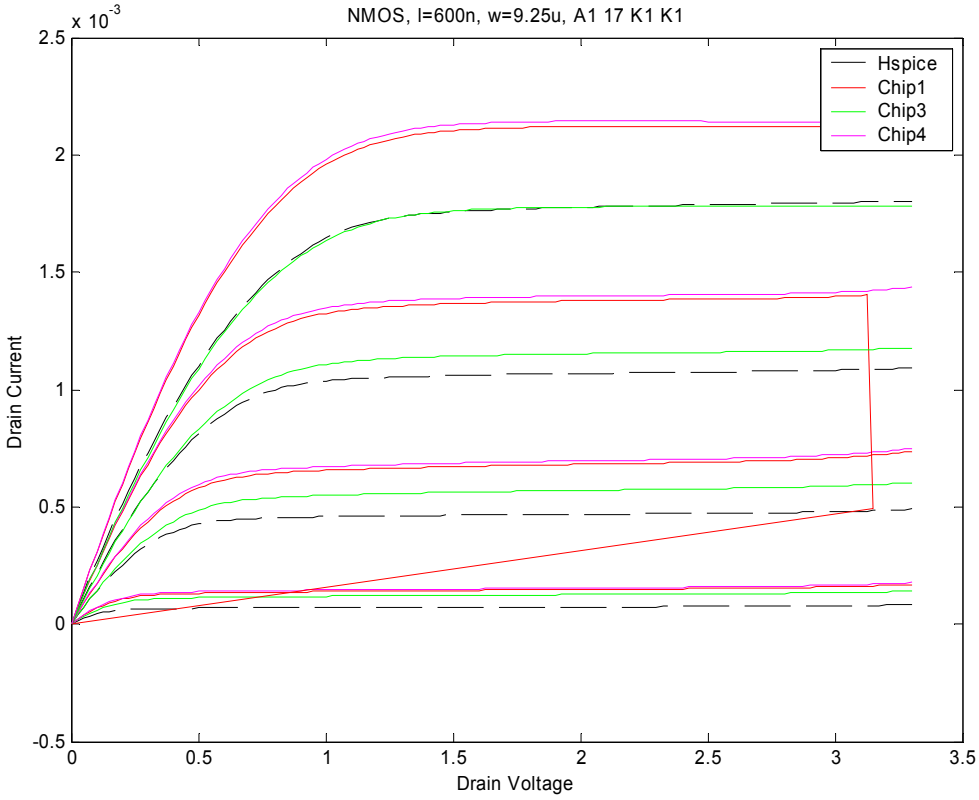


Figure B.16 NMOS, l = 600n, w = 9.25u

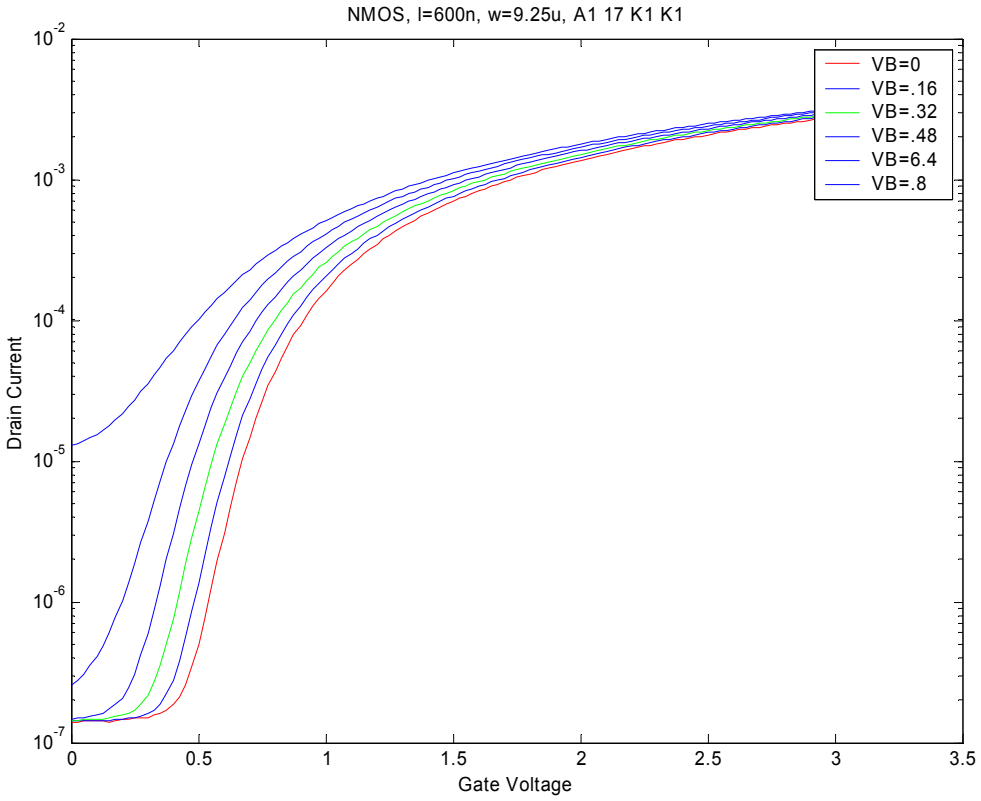


Figure B.17 NMOS, l = 600n, w = 9.25u

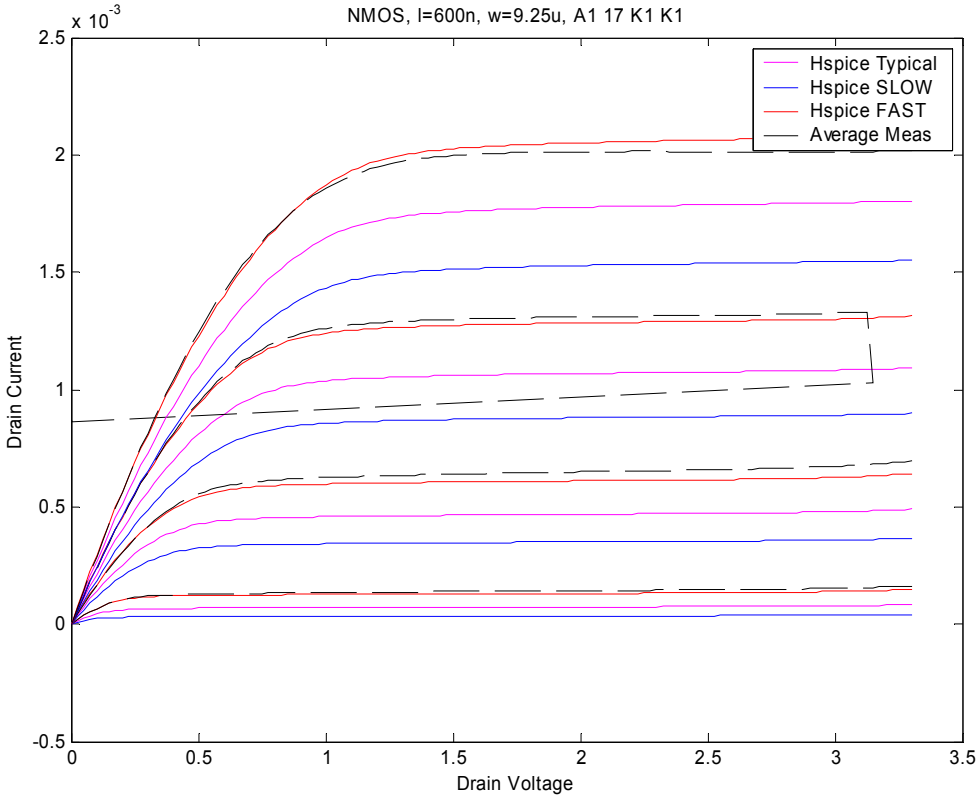


Figure B.18 NMOS, l = 600n, w = 9.25u

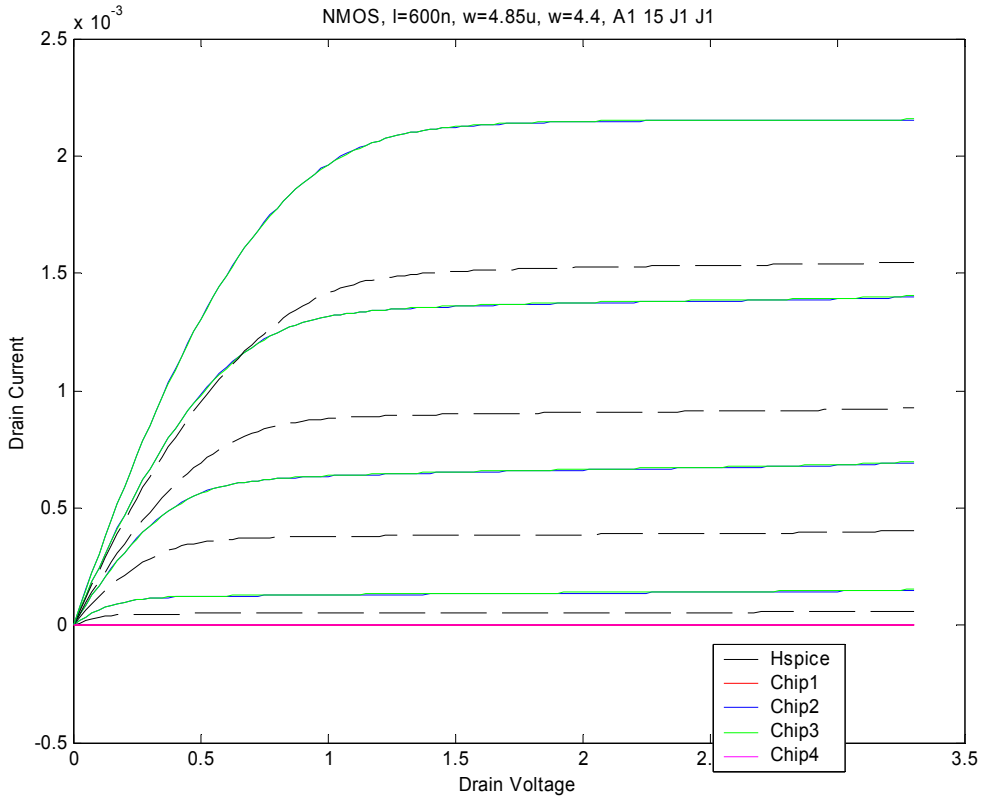


Figure B.19 NMOS, l = 600n, w = 4.85, 4.4u

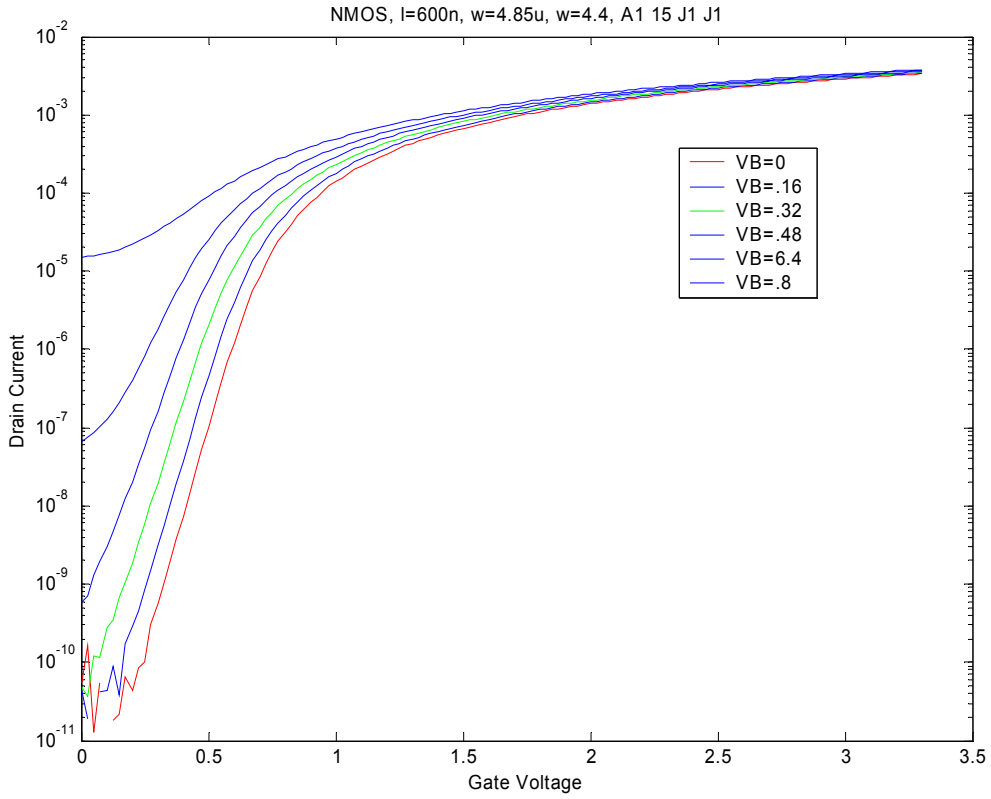


Figure B.20 NMOS, l = 600n, w = 4.85u, 4.4u

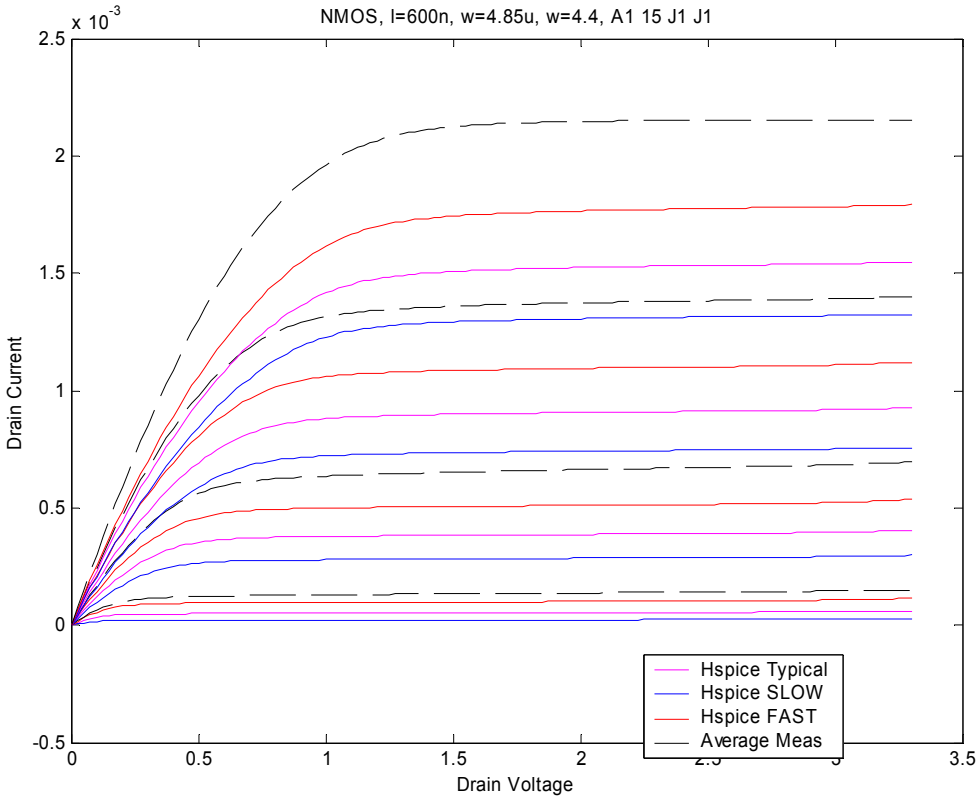


Figure B.21 NMOS, l = 600n, w = 4.85u, 4.4u

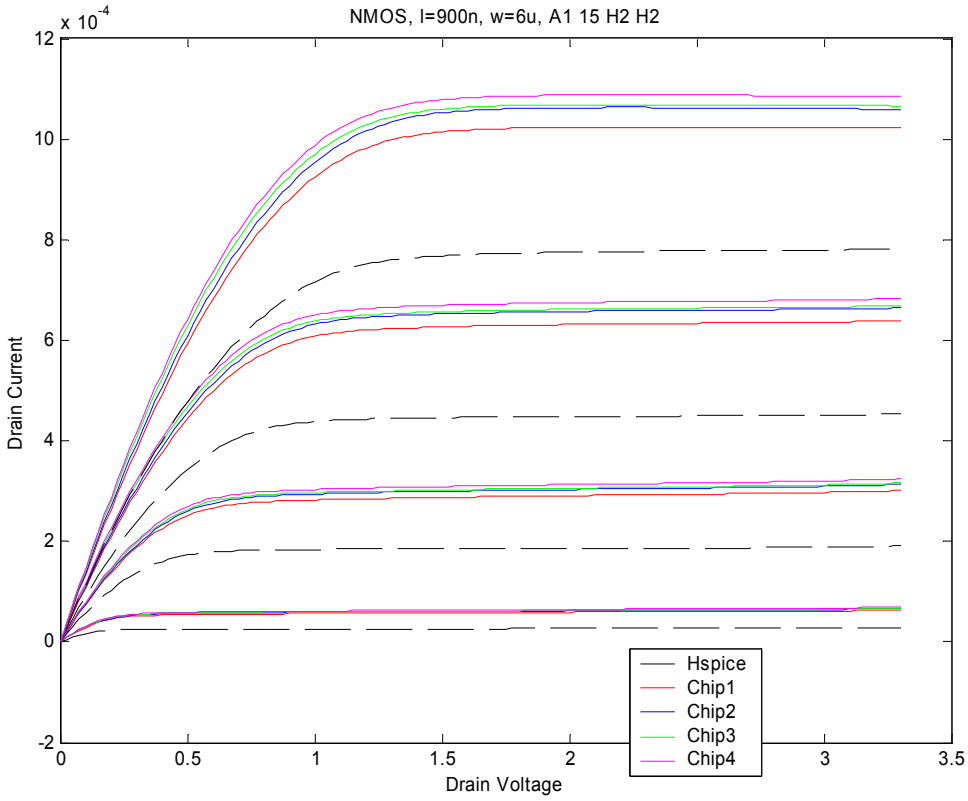


Figure B.22 NMOS BT, l = 900n, w=6u

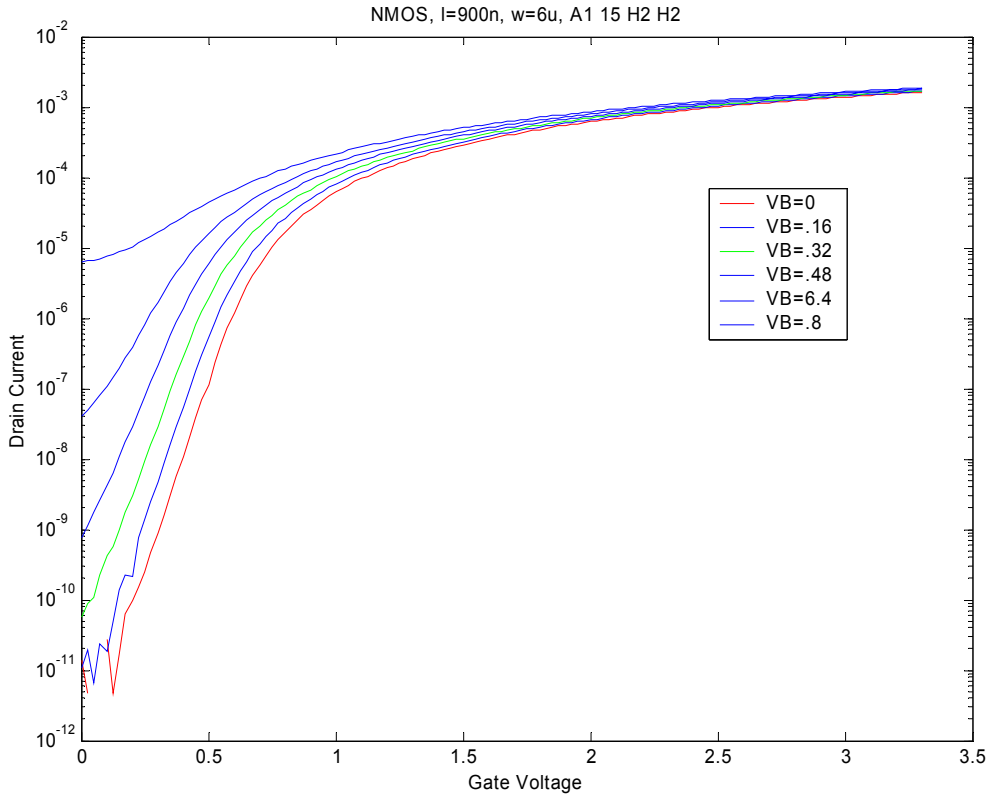


Figure B.23 NMOS, l = 900n, w = 6u

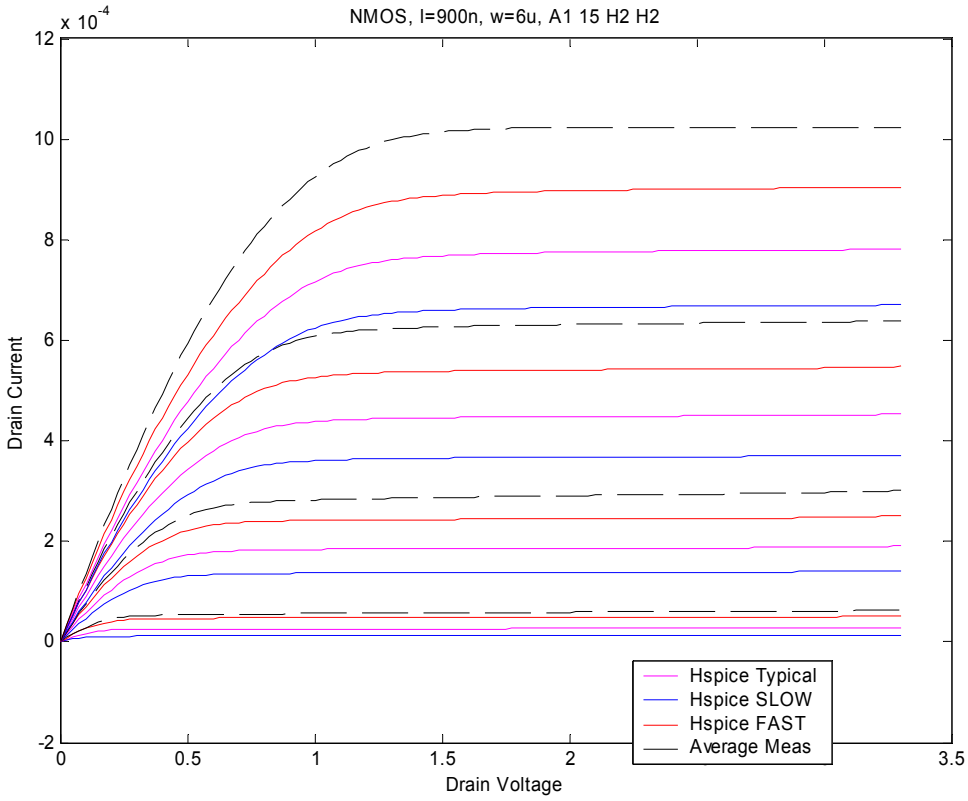


Figure B.24 NMOS, l = 900n, w = 6u

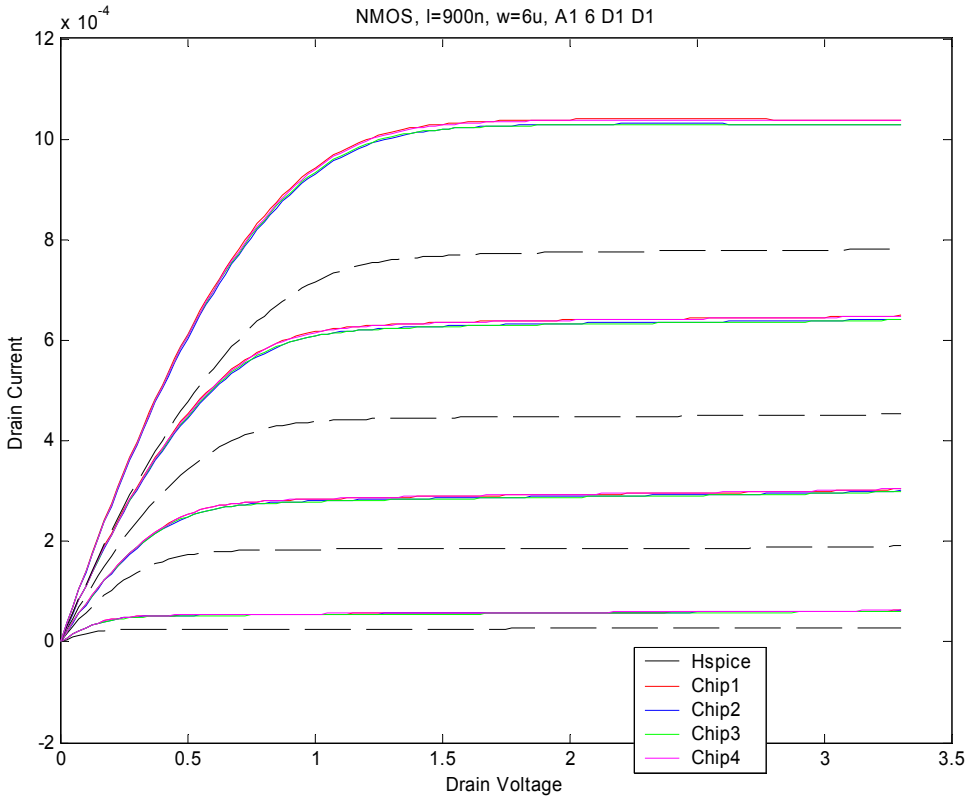


Figure B.25 NMOS, l = 900u, w = 6u

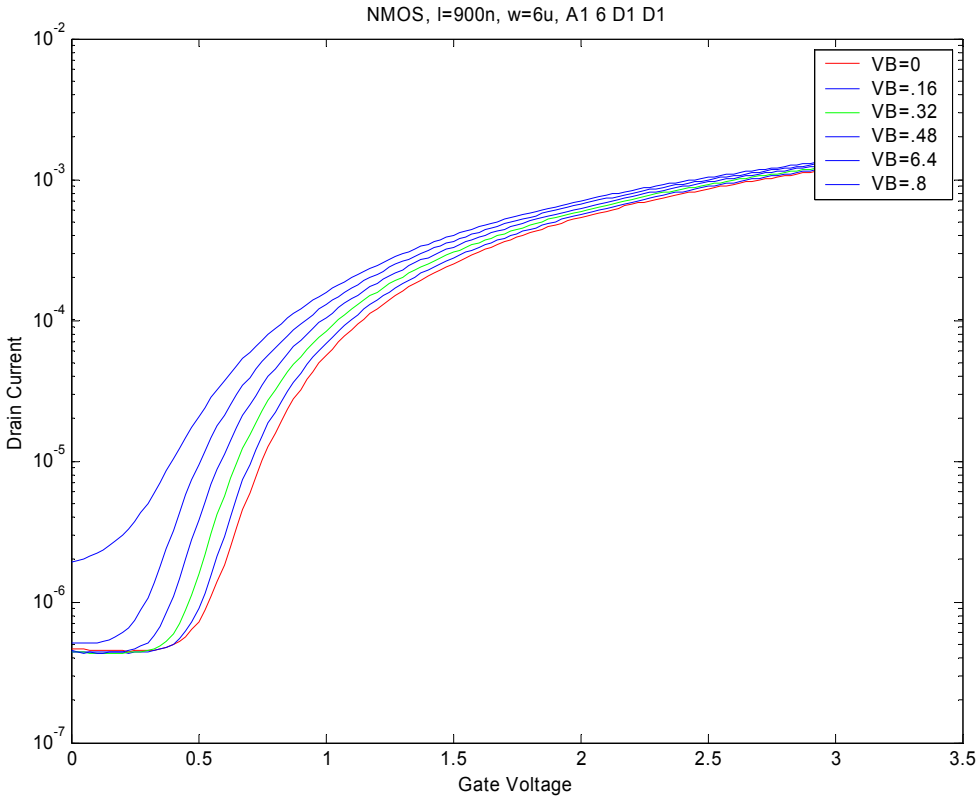


Figure B.26 NMOS, l = 900n, w = 6u

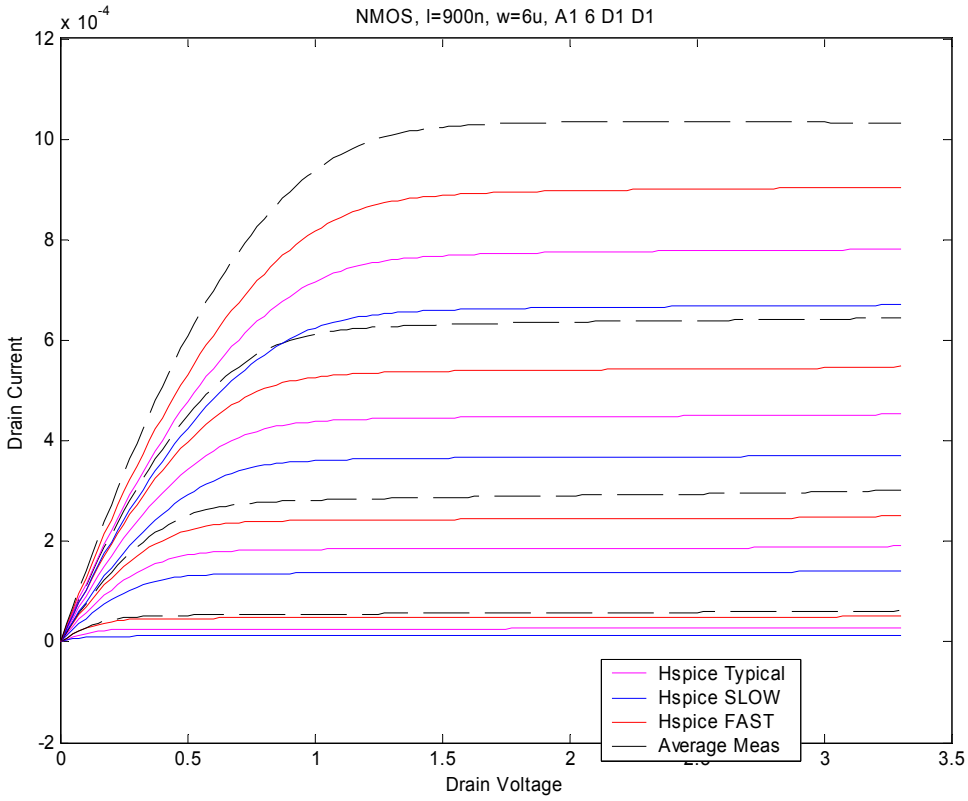


Figure B.27 NMOS, l = 900n, w = 6u

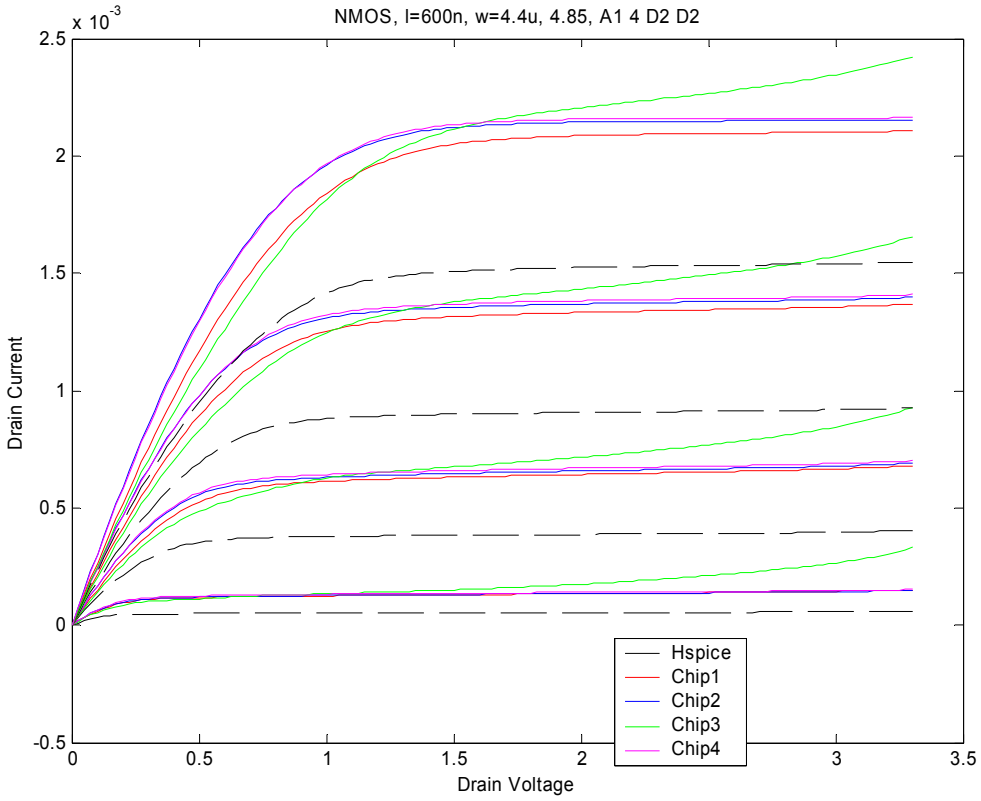


Figure B.28 NMOS, l = 600n, w = 4.4u

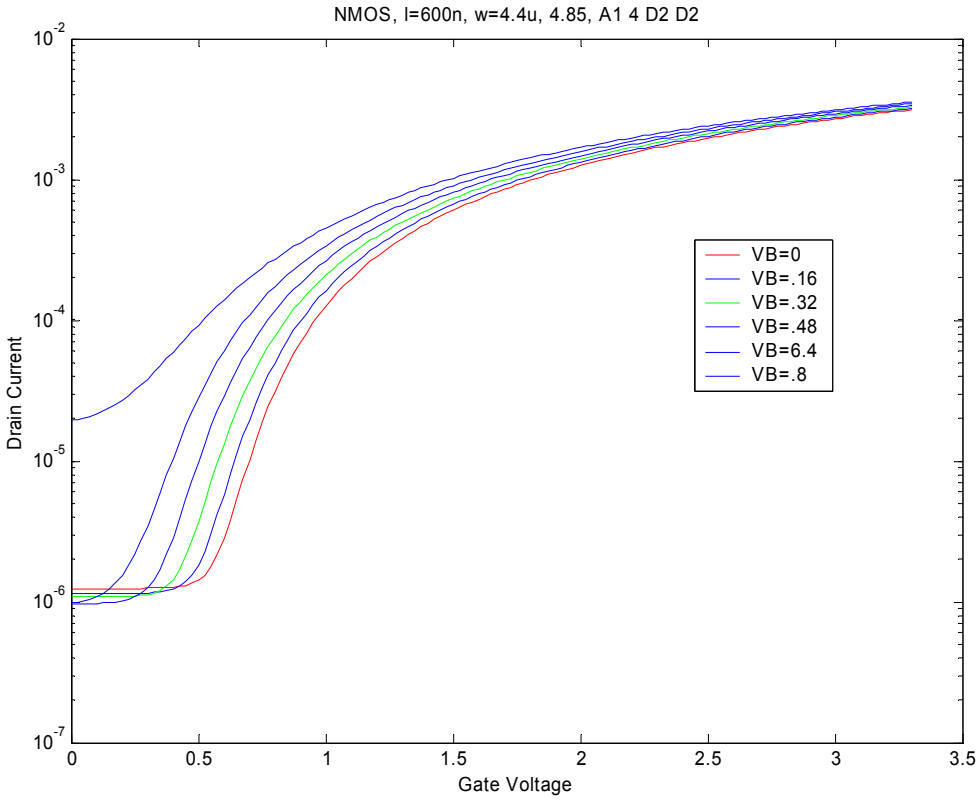


Figure B.29 NMOS, l = 600n, w = 4.4u

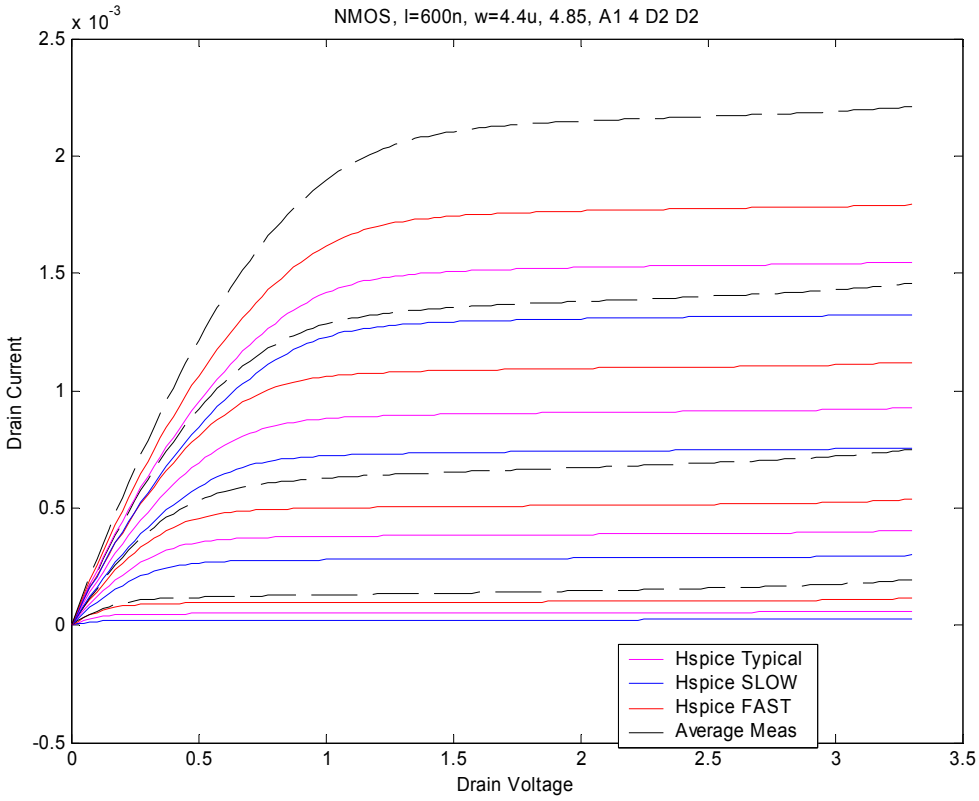


Figure B.30 NMOS, l = 600n, w = 4.4u

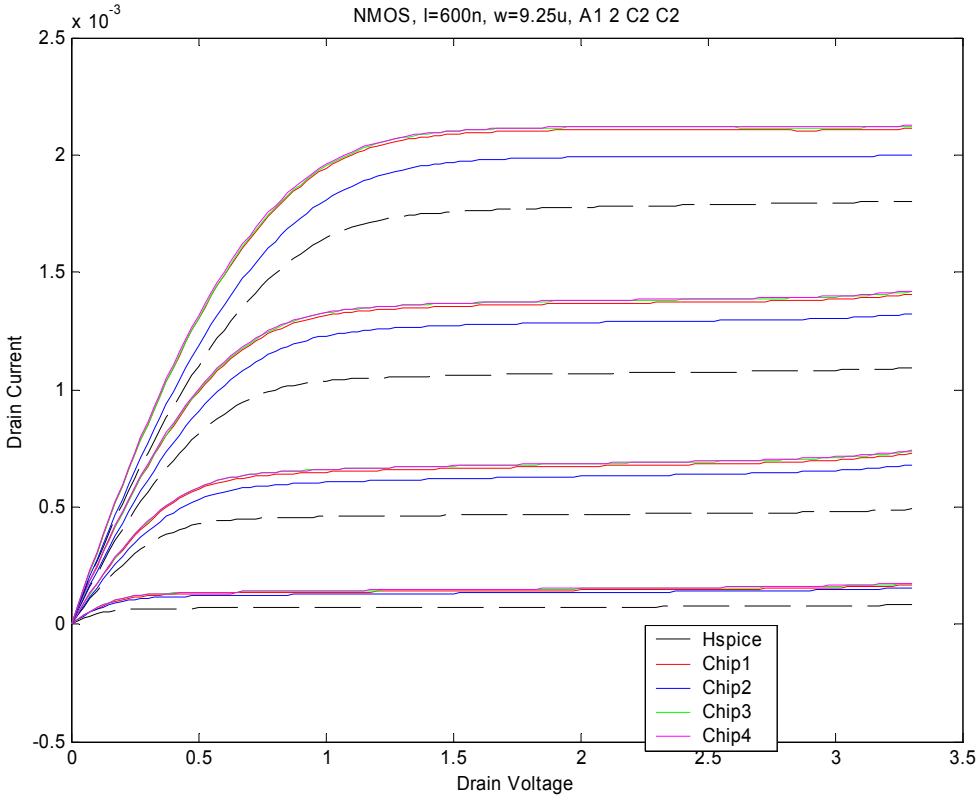


Figure B.31 NMOS, l = 600n, w = 9.25u

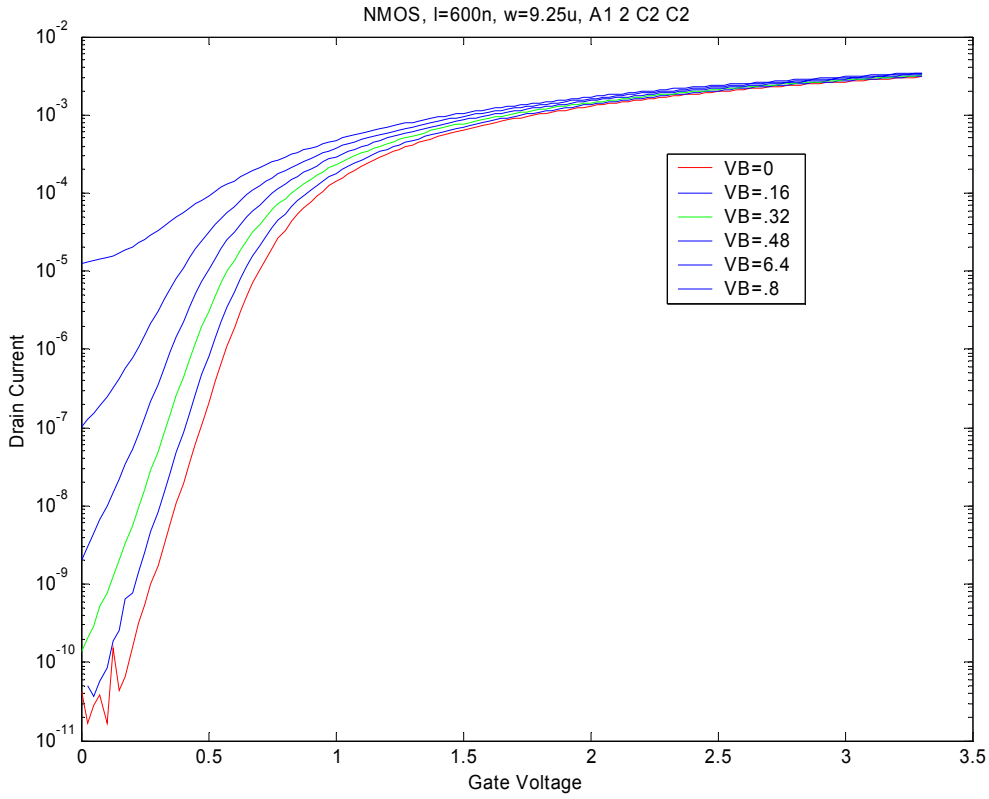


Figure B.32 NMOS, l = 600n, w = 9.25u

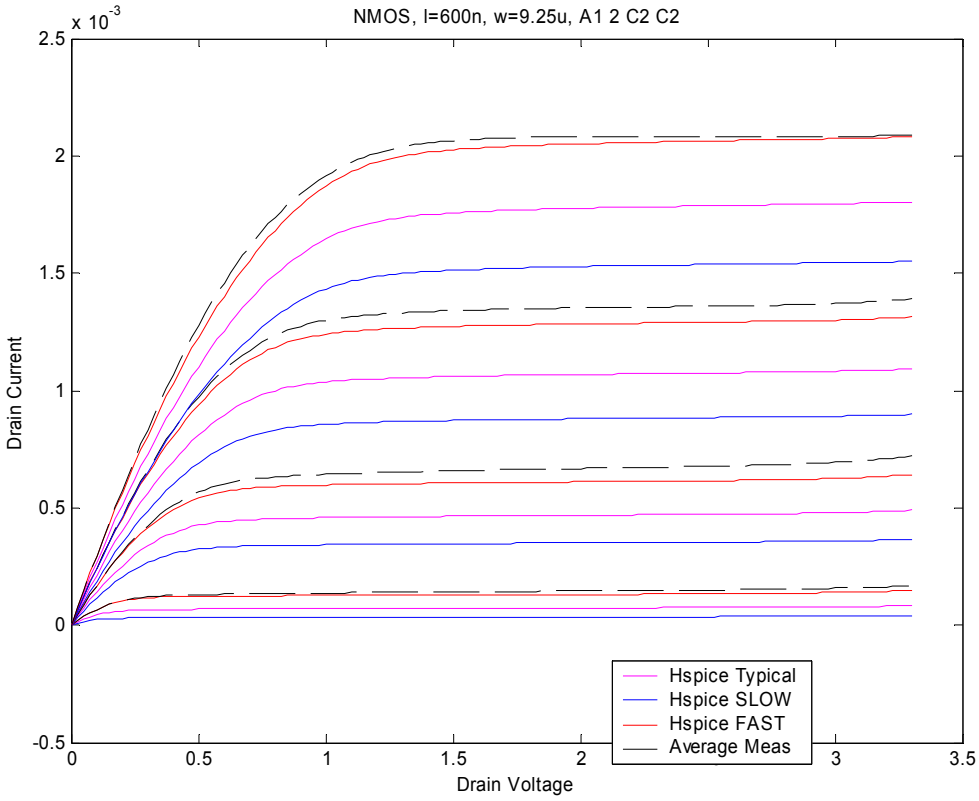


Figure B.33 NMOS, l = 600n, w = 9.25u

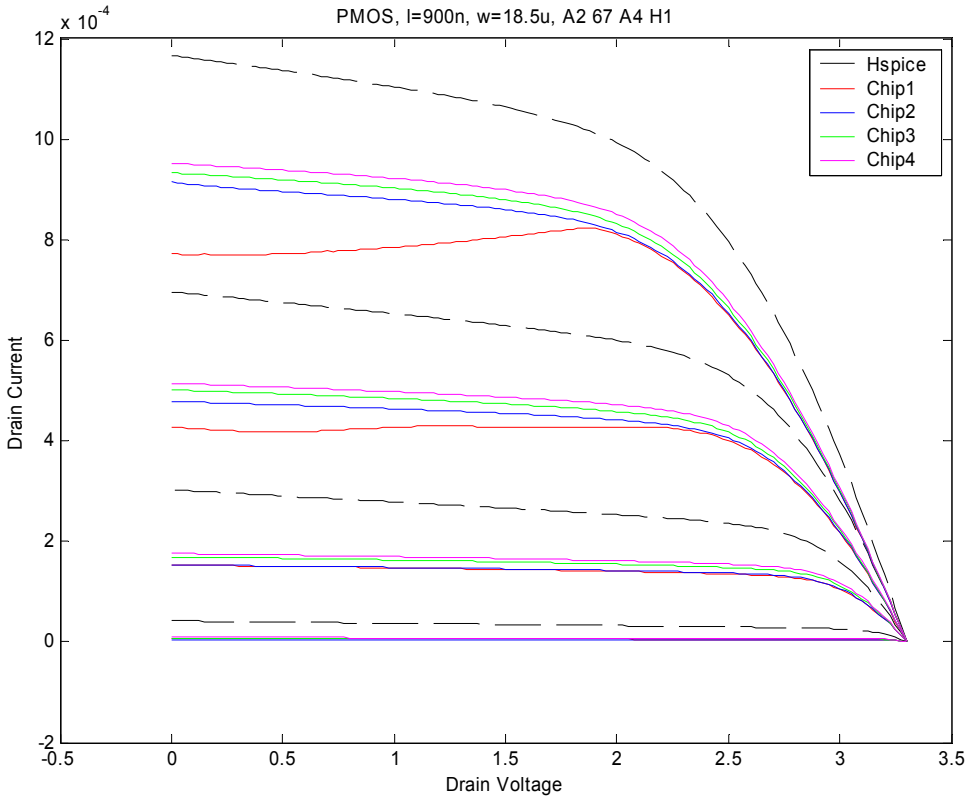


Figure B.34 PMOS, l = 500n, w = 18.5u

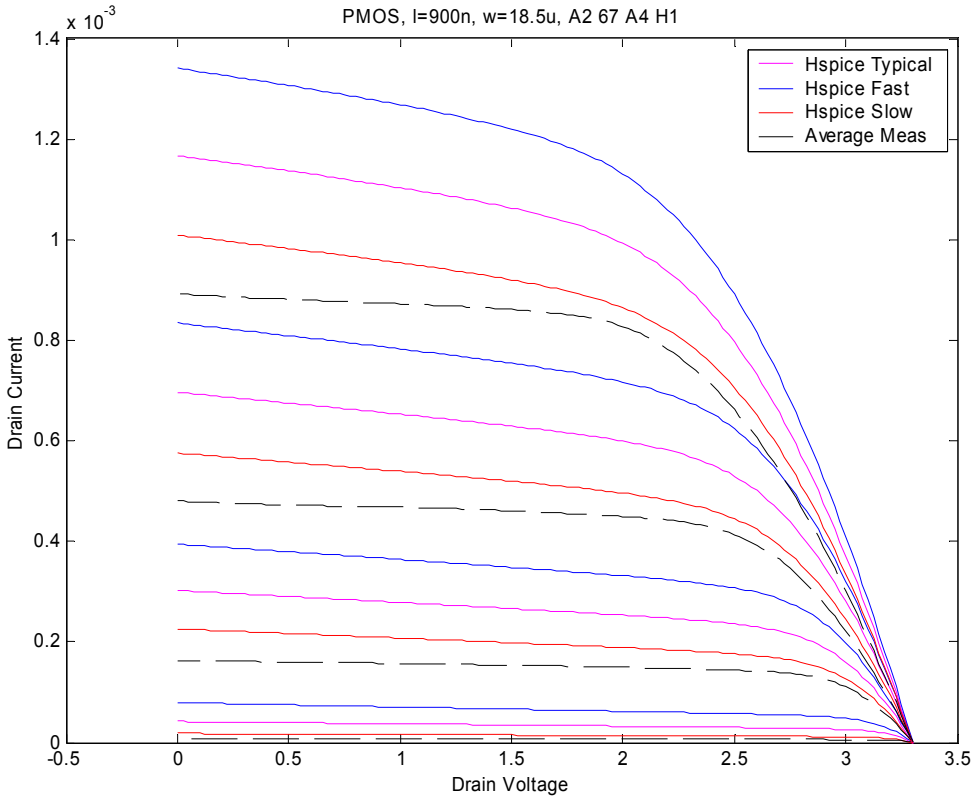


Figure B.35 PMOS, l = 500n, w = 18.5u

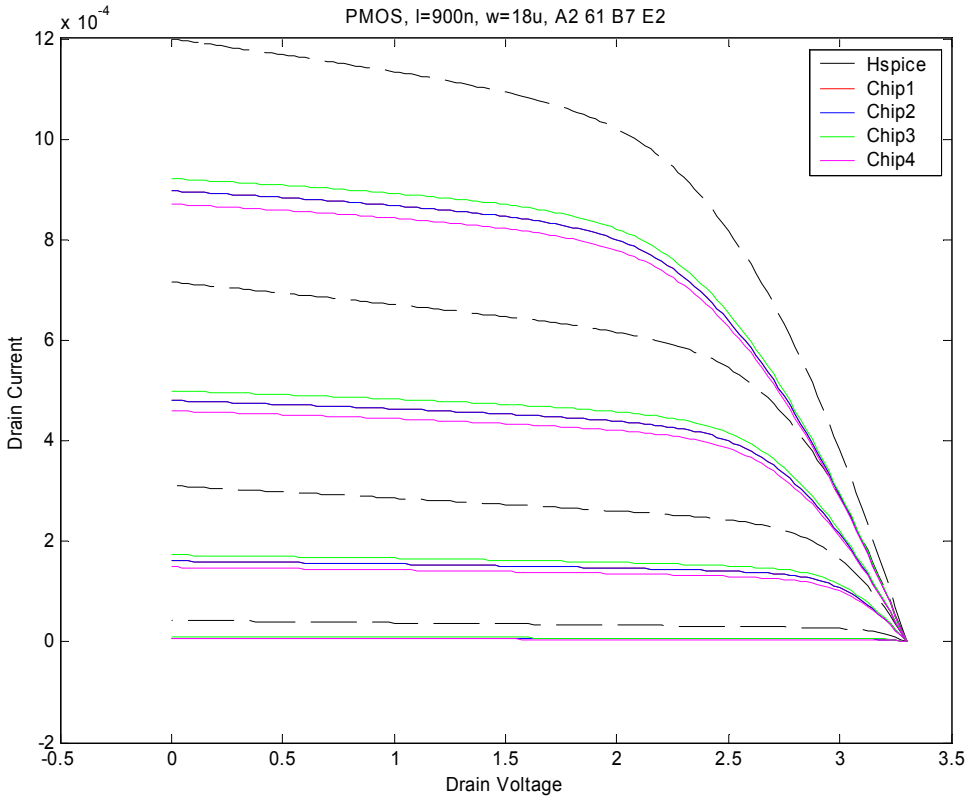


Figure B.36 PMOS, l = 900n, w - 18u

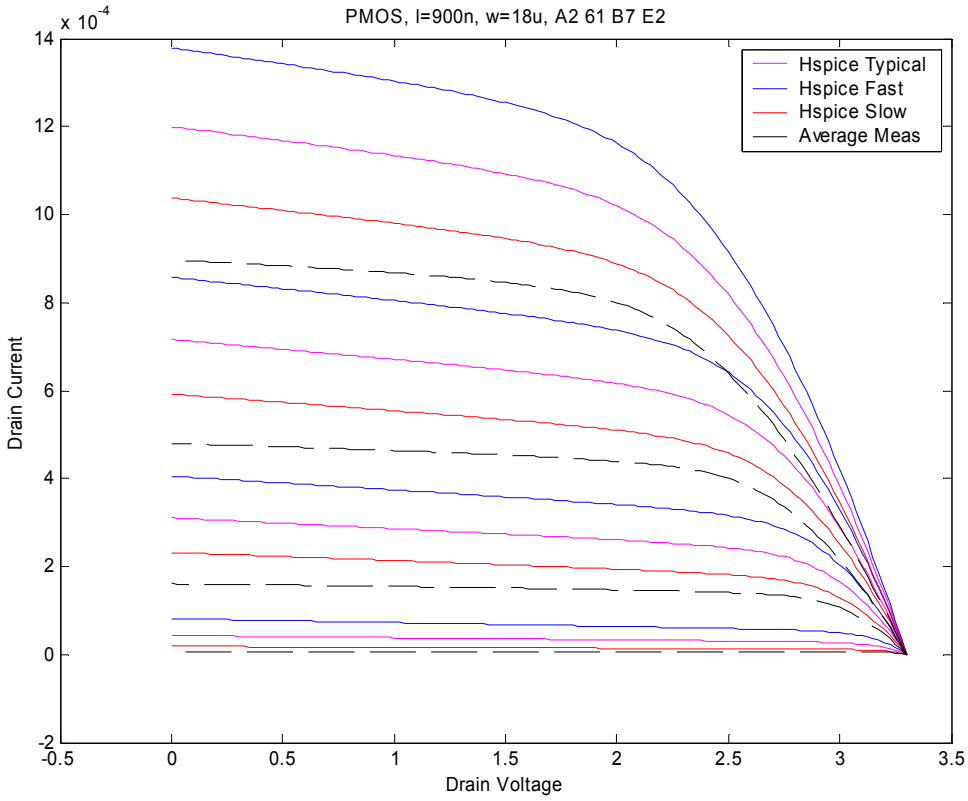
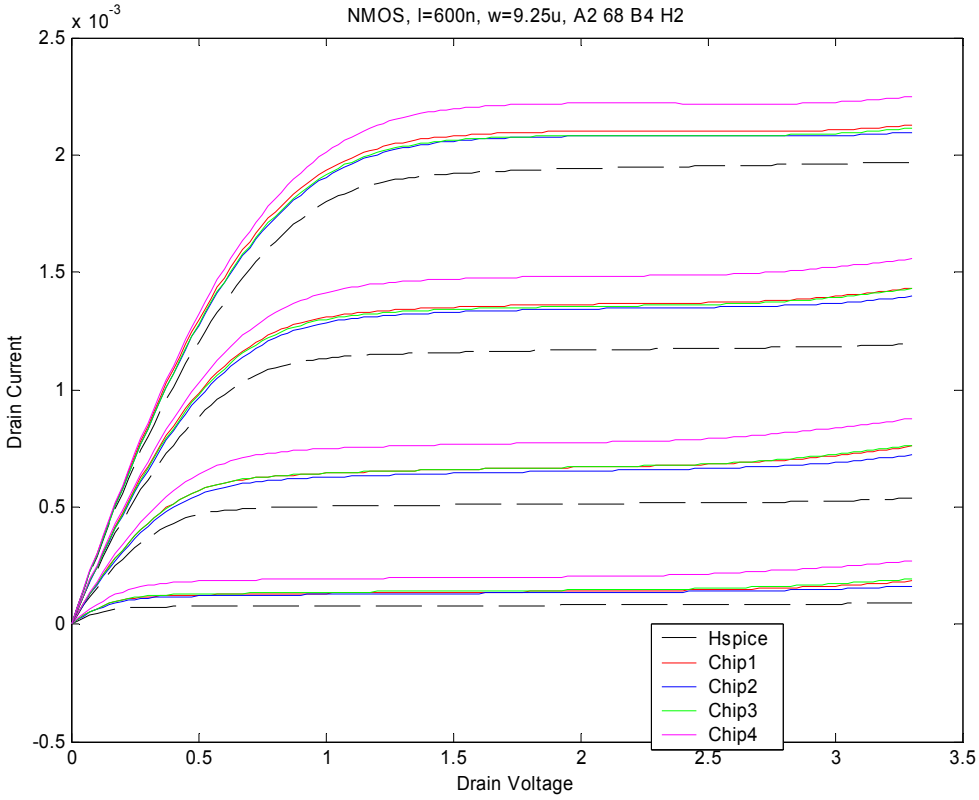


Figure B.37 PMOS, l = 900n, w = 18u


NMOS, l=600n, w=9.25u, A2 68 B4 H2
x 10^-3
Drain Current
Drain Voltage
Hspice
Chip1
Chip2
Chip3
Chip4

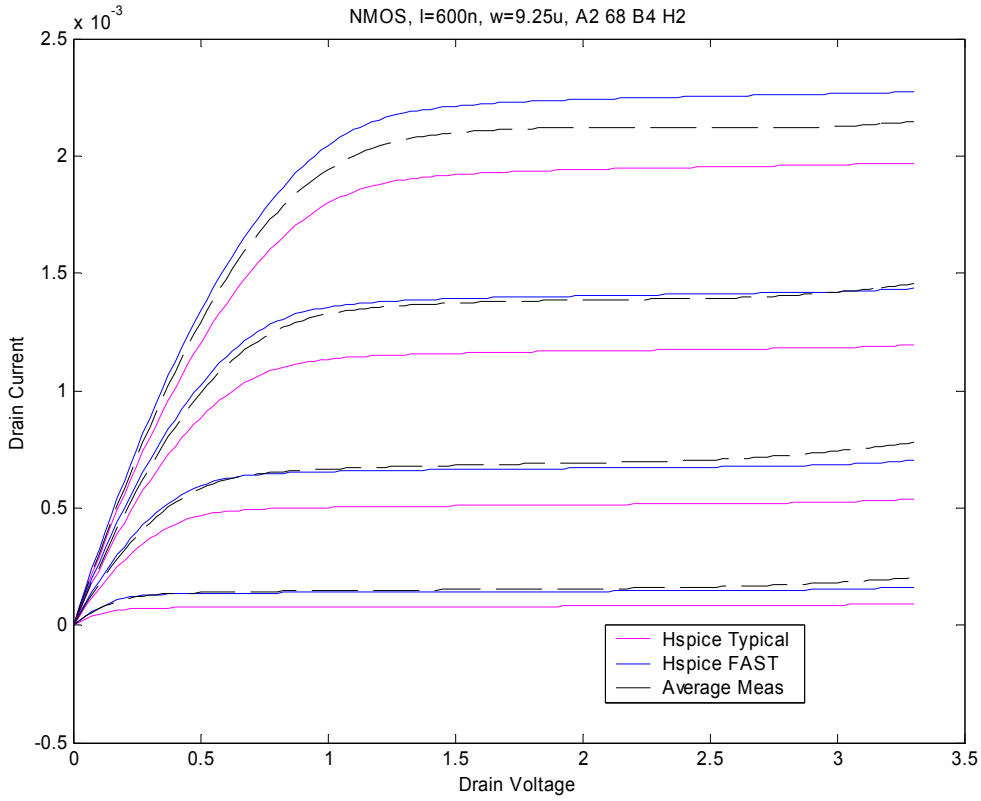


Figure B.38 NMOS, l = 600n, w = 9.25u

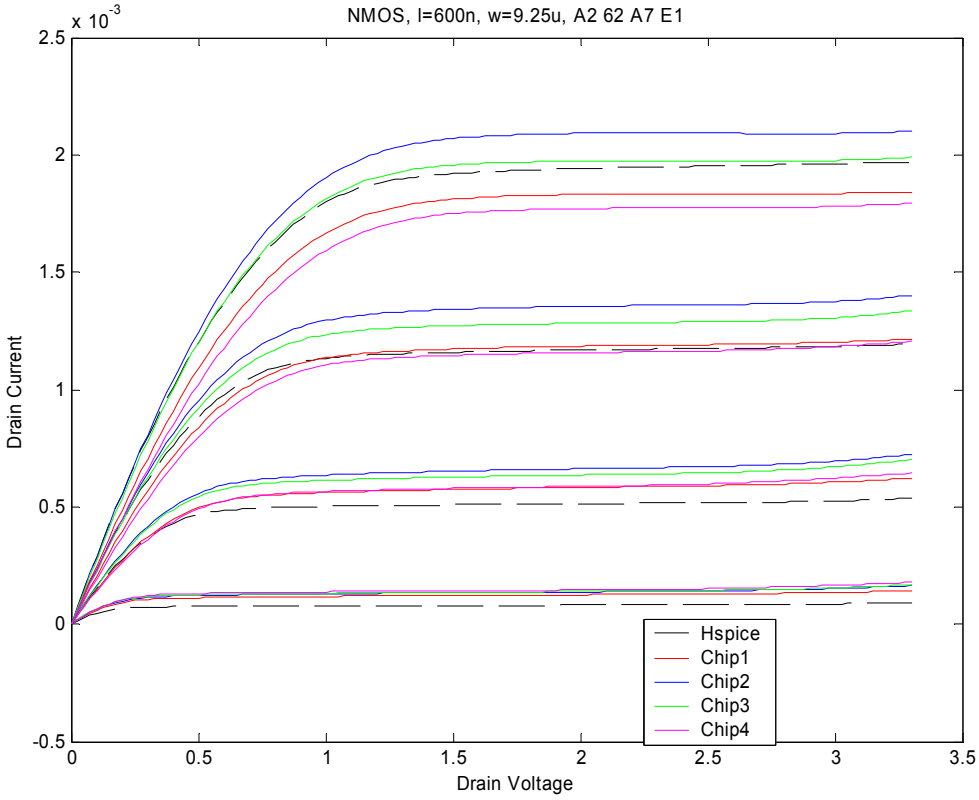


Figure B.39 NMOS, l = 600n, w = 9.25u

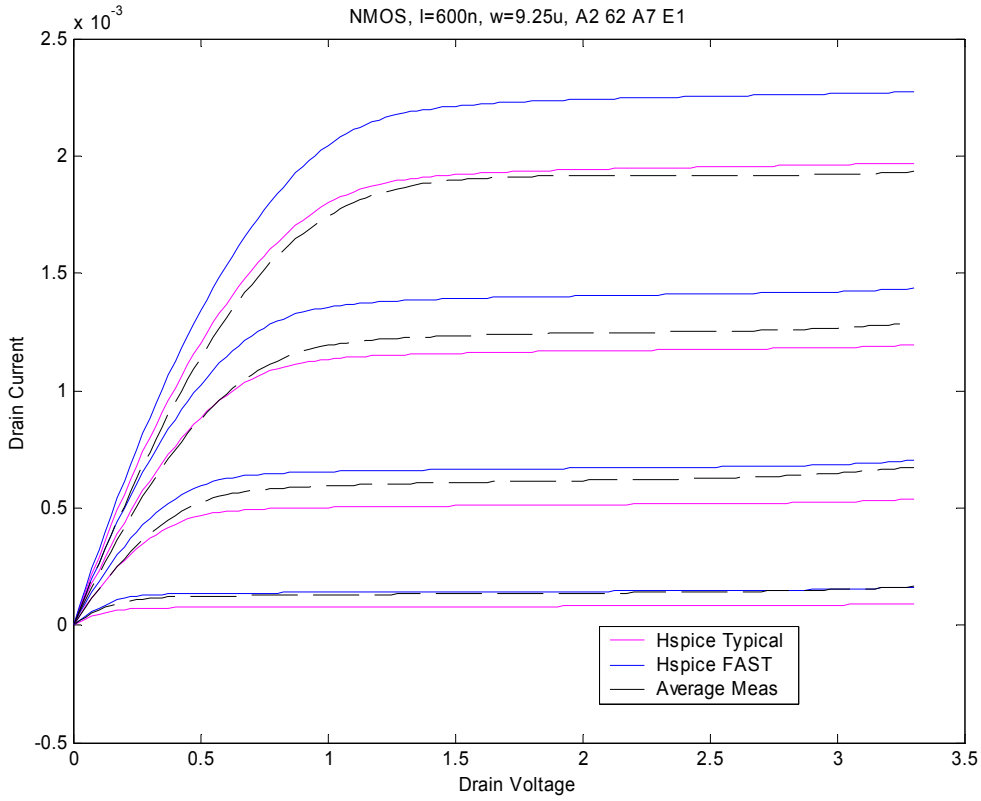


Figure B.40 NMOS, l = 600n, w = 9.25u

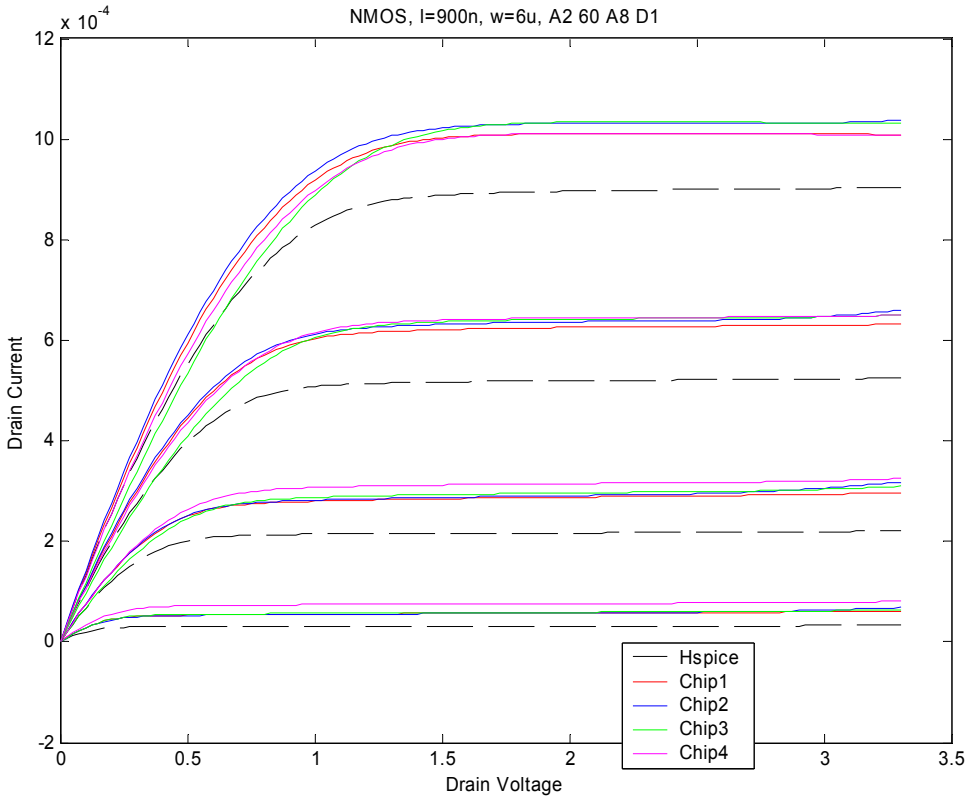


Figure B.41 NMOS, l = 500n, w = 6u

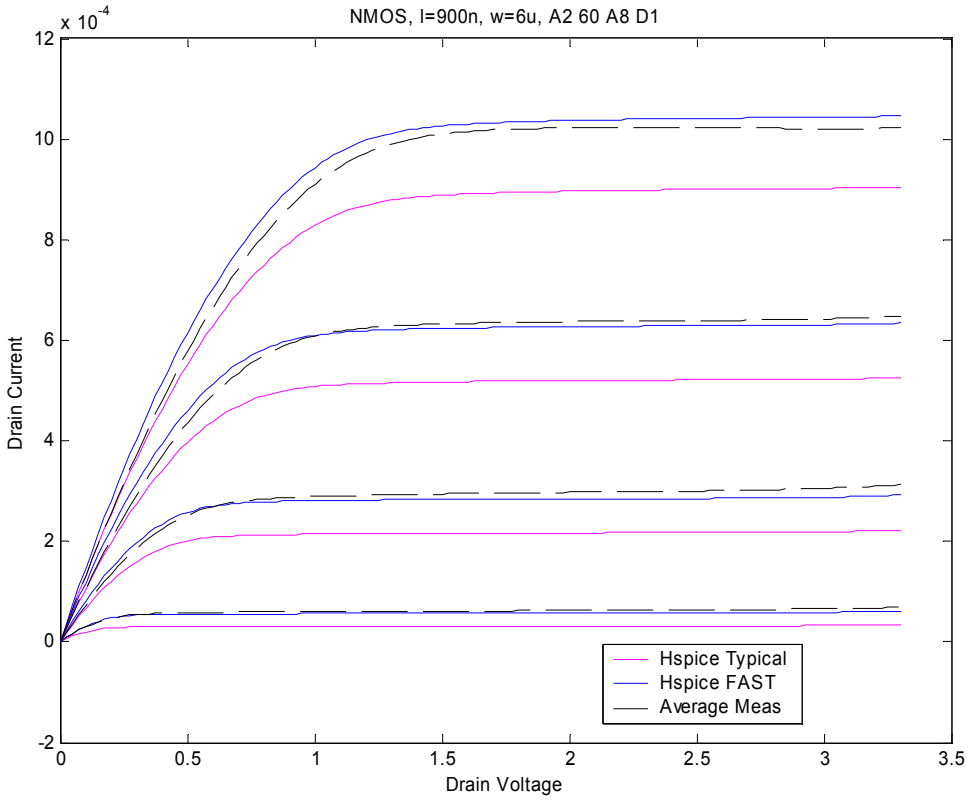


Figure B.42 NMOS, l = 500n, w = 6u

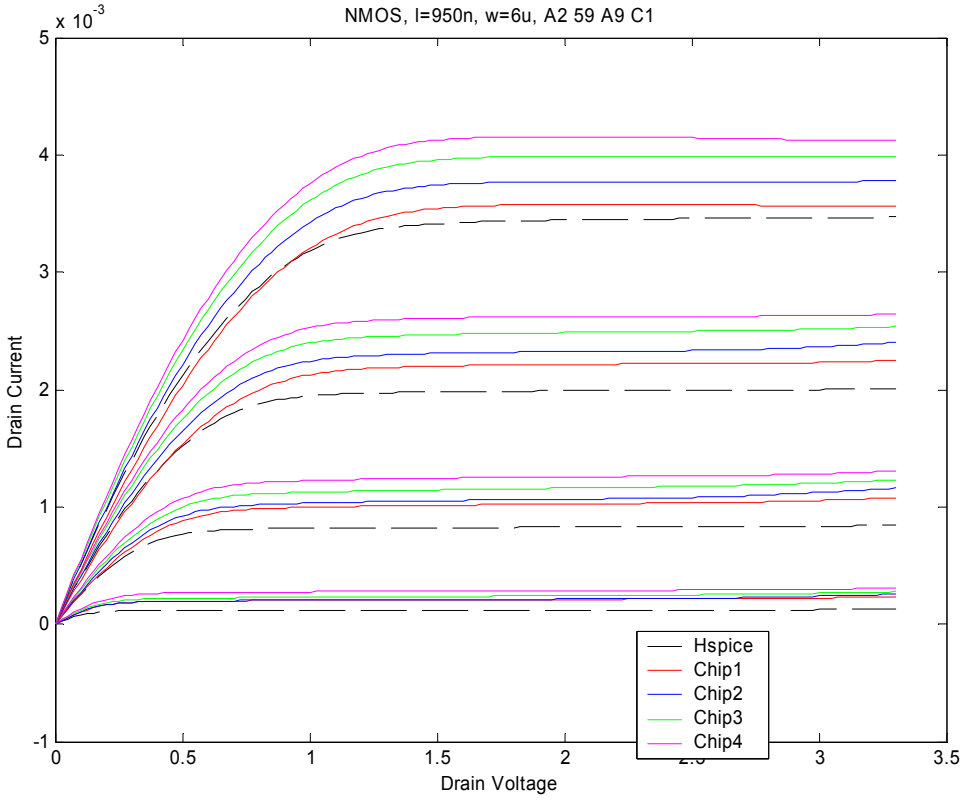


Figure B.43 NMOS, l = 950n, w = 6u

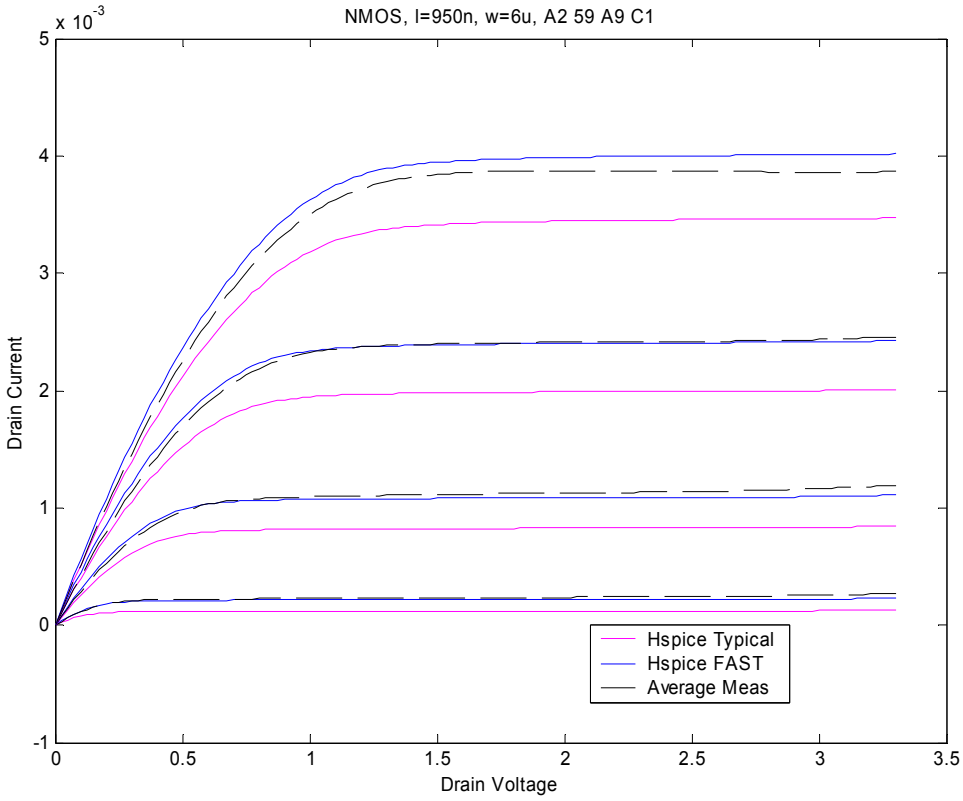


Figure B.44 NMOS l = 950u, w = 6

Appendix C
Oscillator Measurements

This section features a listing of the oscillators fabricated and the frequency and jitter measurements that are associated with each.

		Ring16bt						
409.8	409.8	zero bias	71.74		14.66974		14.66	
409.8	409.8	P = 3.6	76.53	78.81	14.10833	13.85334	14.66	-0.67917
409.8	409.8	P = 3.0	47.72	47.63	18.21095	18.22735	14.66	3.559153
409.8	409.8	N = 0.3	71.54	76.16	14.69398	14.15042	14.66	-0.2378
409.8	409.8	N = -0.3	63.21	60.79	15.76925	16.10832	14.66	1.278784
		Ring17bt						
497.5	497.5	zero bias	56.5	42.42	15.05957	17.54913	16.30435	0
497.5	497.5	P = 3.5	126.9	80.41	8.031308	11.99434	16.30435	-6.29153
497.5	497.5	P = 3.0	70.46	50.41	13.14169	16.05021	16.30435	-1.7084
497.5	497.5	N = 0.3	72.64	72.8	12.87702	12.85791	16.30435	-3.43688
497.5	497.5	N = -0.3	48.62	40.81	16.36424	17.88521	16.30435	0.820375
		Ring18bt						
411.5	411.5	zerobias	44.96	46.53	18.69248	18.39434	18.54341	0
411.5	411.5	P = 3.0	58	51	16.48045	17.5976	18.54341	-1.50439
411.5	411.5	N = 0.3	56	54	16.78525	17.10113	18.54341	-1.60022
411.5	411.5	N= -0.3	41	40.19	19.49333	19.66665	18.54341	1.036577
		ring19bt						
512.87	512.87	zerobias	64.76	64	13.61012	13.71266	13.66139	0
512.87	512.87	P = 3.6	69	72	13.05927	12.68961	13.3347	-0.46026
512.87	512.87	P = 3.0	54	57	15.18838	14.71876	13.3347	1.618871
512.87	512.87	N = 0.3	66.45	67.8	13.38636	13.21166	13.3347	-0.03569
512.87	512.87	N = -0.3	53		15.35074		13.3347	2.016039

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